Model Name : ZIWB0/ZIWB1/ZIWE0
File Name :

Compal Confidential

ZIWB0/ZIWB1/ZIWE0 DIS M/B Schematics Document

Intel Bay Trail M

2014-02-10

REV:1.0

14PCB@
DA1 PCB

Part Number	Description
DA60013Y010	REV1.0 M/B

15PCB@
DA2 PCB

Part Number	Description
DA60013Y110	REV1.0 M/B

Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

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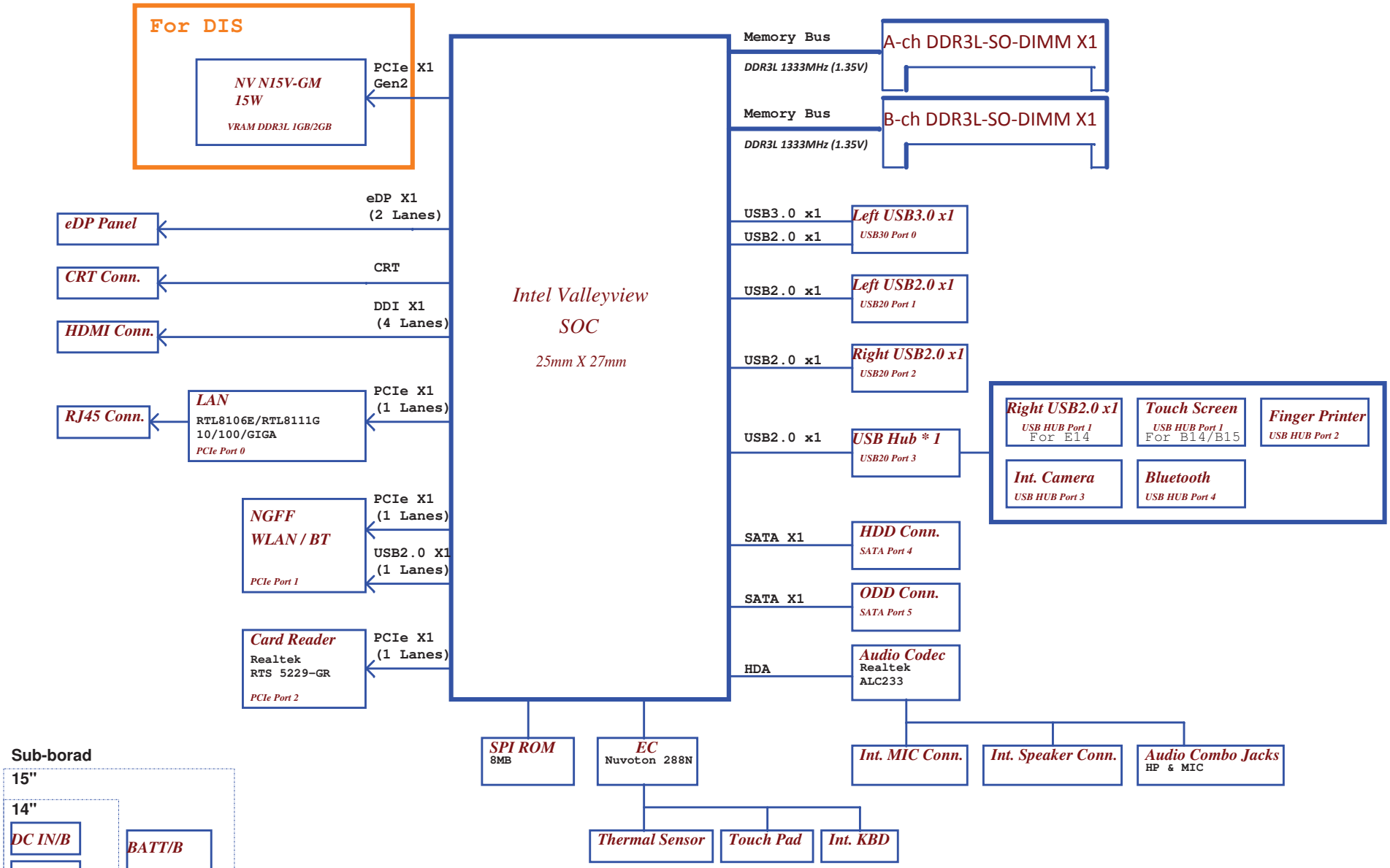
Title: *Cover Page*

Size: Custom | Document Number: *LA-B101P* | Rev: 0.2

Date: Tuesday, February 18, 2014 | Sheet 1 of 47



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	ME@
XDP (Debug Port)	XDP@
EMC requirement	EMC@
EMC requirement unpop	@EMC@
ESD requirement	ESD@
ESD requirement unpop	@ESD@
Touch Screen	TS@
B/E series sku	B14@
B/E series sku	B15@
B/E series sku	E14@

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
Charger	0b00010010 (0x12H)

EC SM Bus2 address

Device	Address
GPU	0x9E
Thermal	1001_101xb

SOC SM Bus address

Device	Address
SO-DIMM A (JDIMM1)	A0h
SO-DIMM B (JDIMM2)	A2h

43 level BOM table

43 Level	Description	BOM Structure

USOC1 N2920@

S IC FH8065301616203 SR1SF B3 1.86G C38!
Part Number = SA00007E860

USOC1 N3520@

S IC FH8065301616103 SR1SE B3 2.17G C38!
Part Number = SA00007E990

USOC1 N2815@

S IC FH8065301619509 SR1SJ B3 1.86G C38!
Part Number = SA00007EO50

Security Classification	Compal Secret Data		
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Title: Notes List

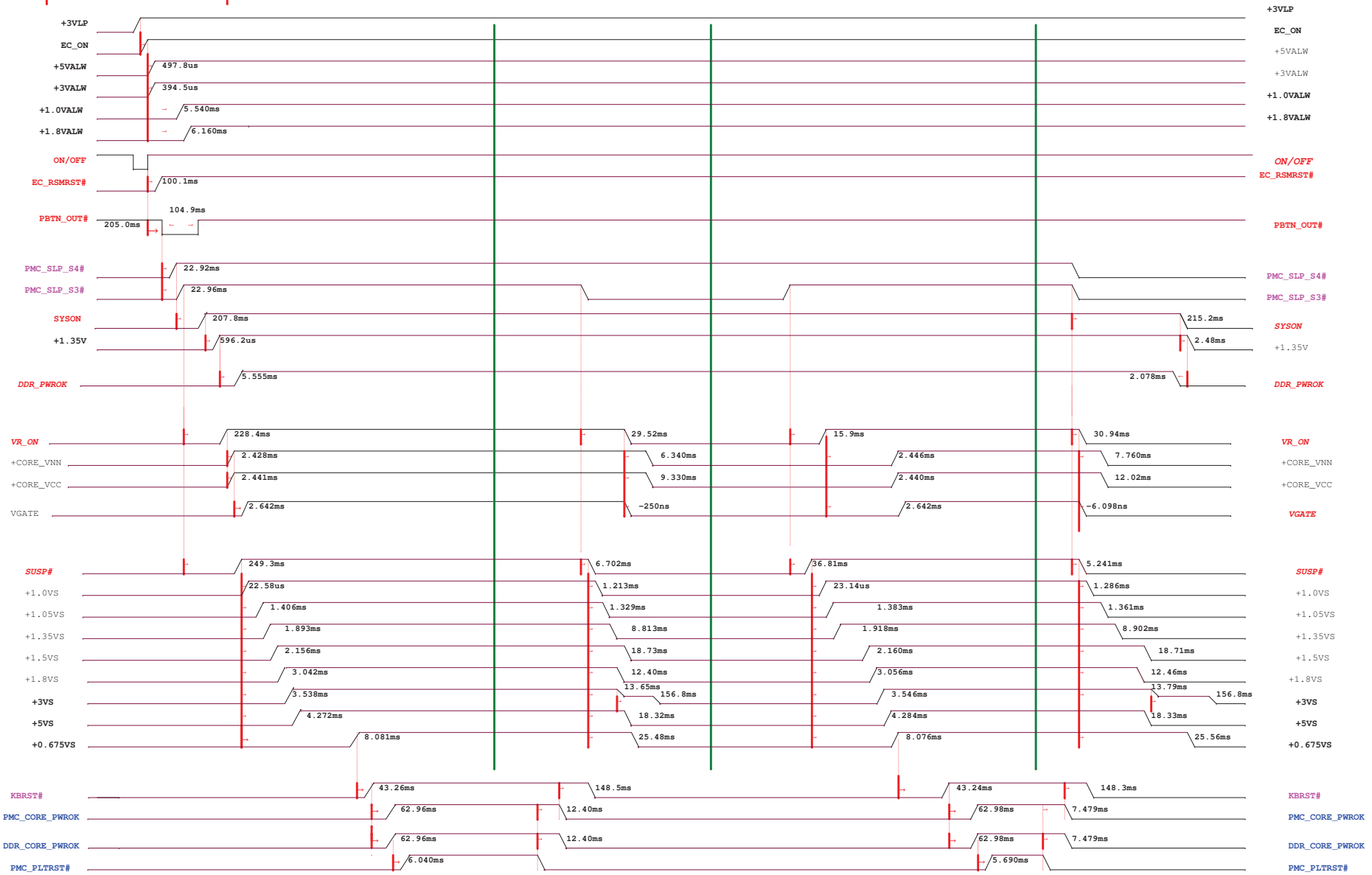
Size: Custom | Document Number: Intel BayTrail-M Platform | Rev: 0.2

Date: Tuesday, February 18, 2014 | Sheet 3 of 47

EVT Power Sequence
2013-06-25_ AC

Power On | S3 | S3 Resume | Power Off

Plug in



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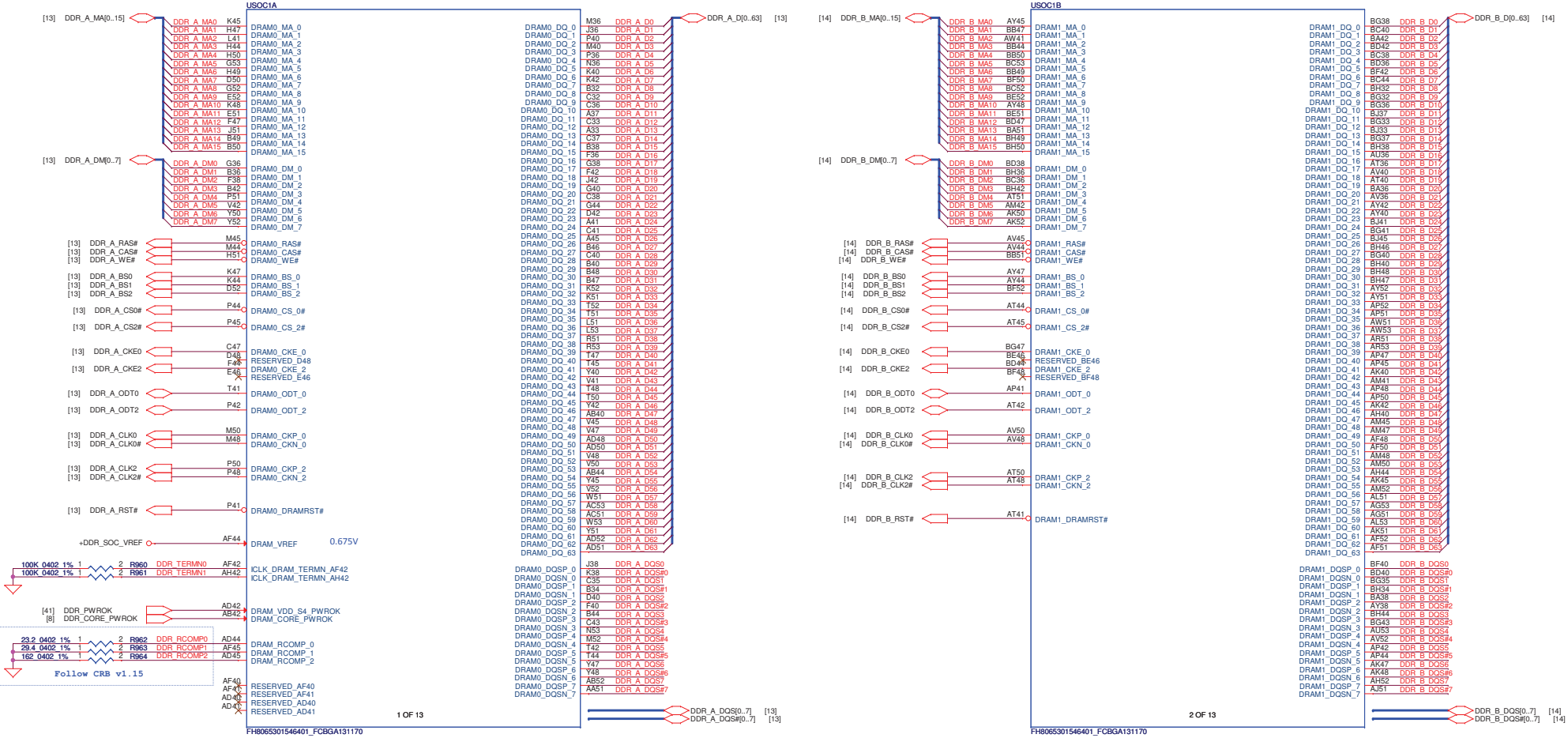
Compal Electronics, Inc.

Title: Power Sequence

Size: Custom | Document Number: Intel BayTrail-M Platform | Rev: 0.2

Date: Tuesday, February 18, 2014 | Sheet 4 of 47



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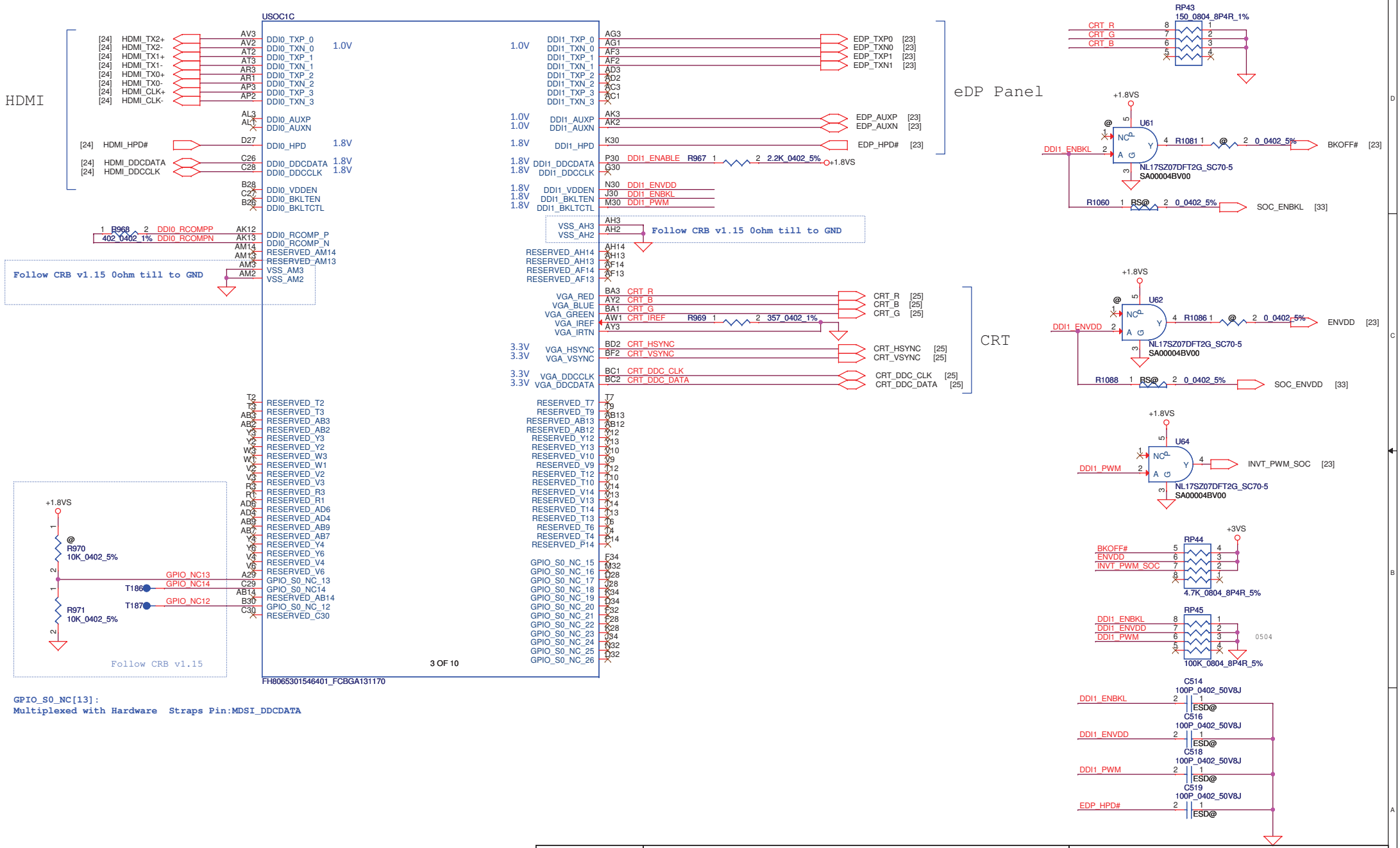
Compal Electronics, Inc.

Title: VLV-M SOC Memory DDR3L

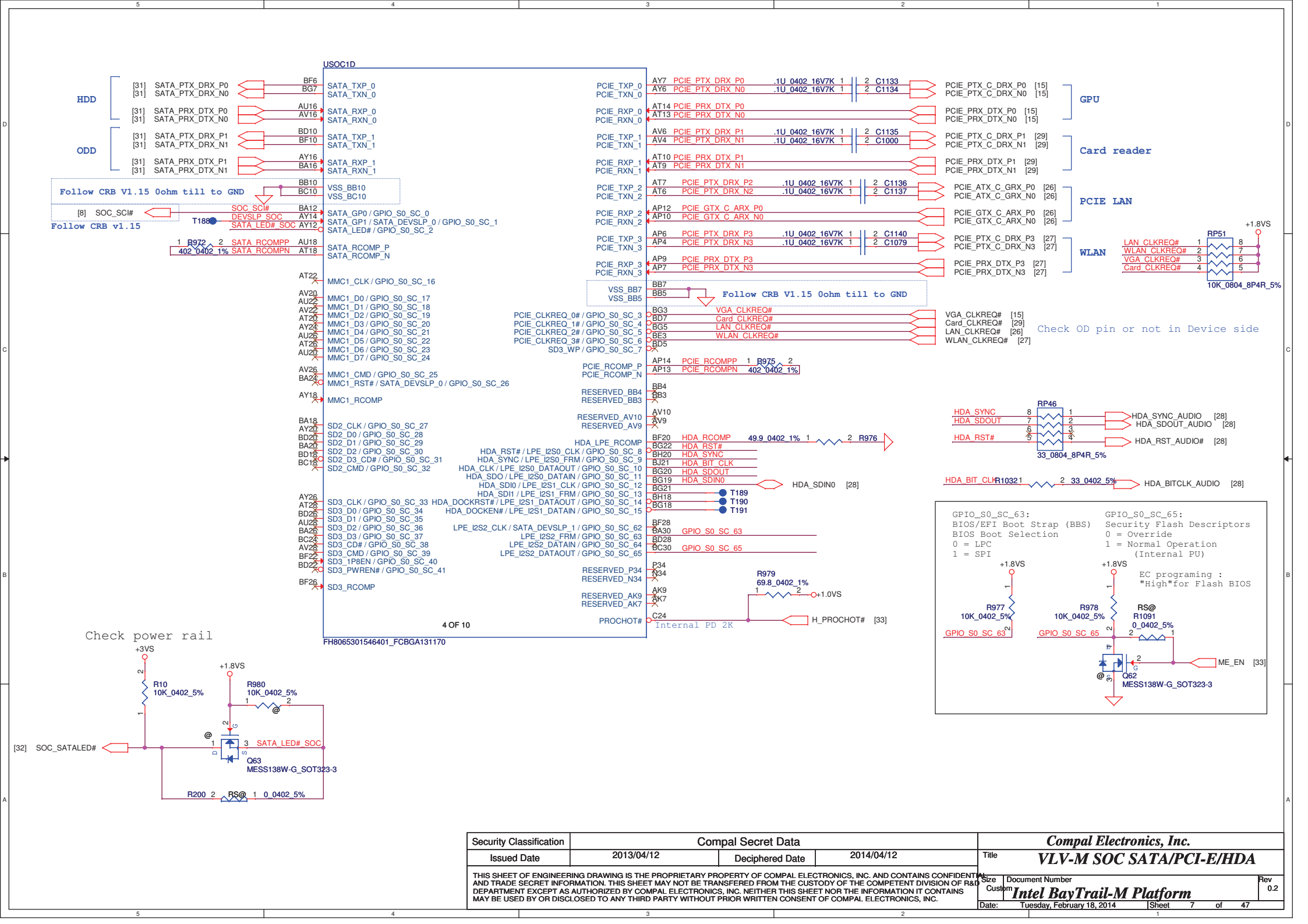
Size: Custom | Document Number: Intel BayTrail-M Platform | Rev: 0.2

Date: Tuesday, February 18, 2014 | Sheet 5 of 47



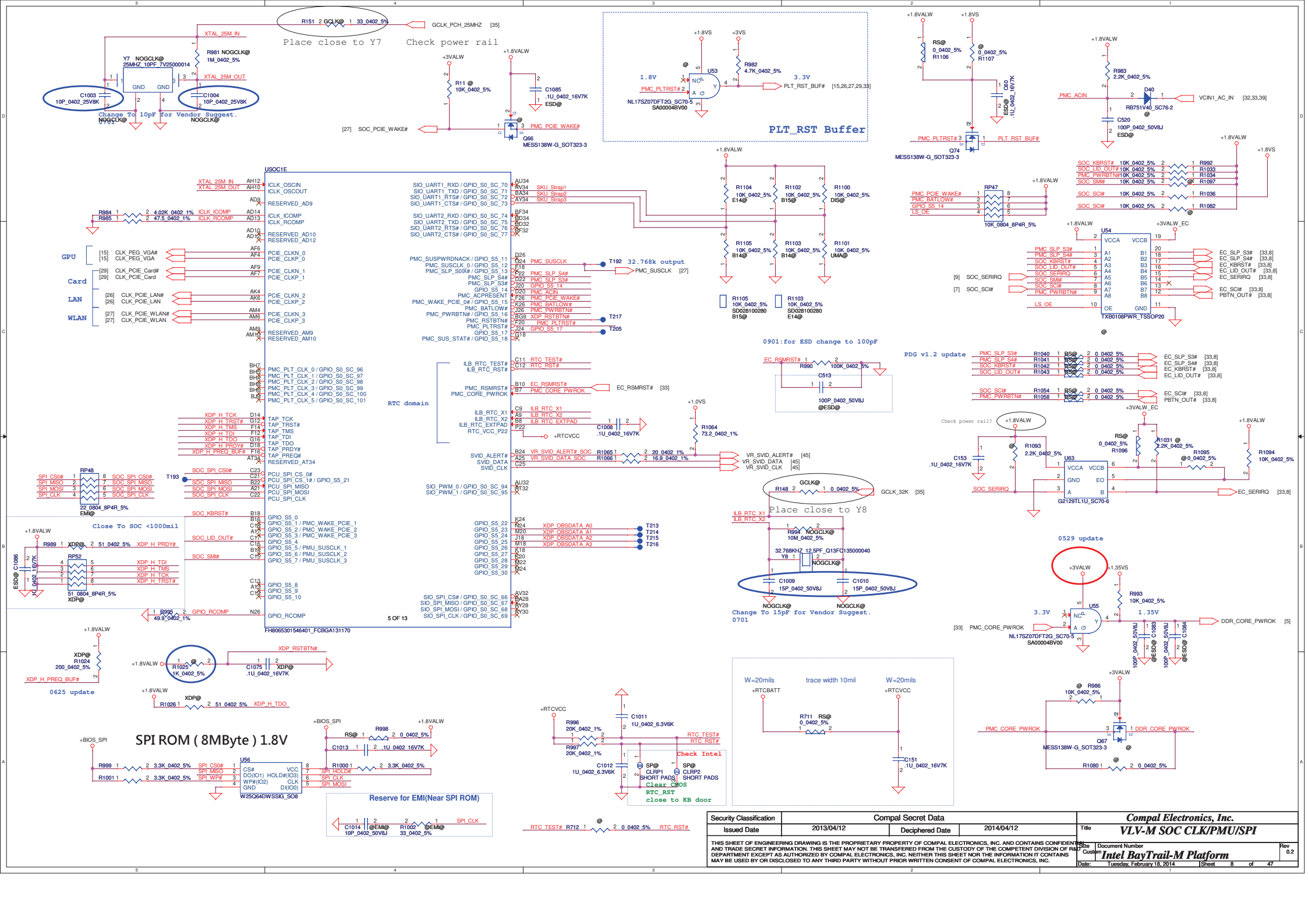
Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.			
Title: VLV-M SOC Display			
Size: Custom	Document Number: Intel BayTrail-M Platform		Rev: 0.2
Date: Tuesday, February 18, 2014	Sheet 6 of 47		



Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.			
Title	VLV-M SOC SATA/PCI-E/HDA		
Size: Custom	Document Number: Intel BayTrail-M Platform		Rev: 0.2
Date: Tuesday, February 18, 2014	Sheet 7 of 47		


USOC1E
FH80653015464O1_FCBGA131170
5 OF 13
RTC domain
GPU
Card
LAN
WLAN
Place close to Y7
Check power rail
Change To 10pF for Vendor Suggest.
0701
Close To SOC <1000mil
Place close to Y8
Change To 15pF for Vendor Suggest.
0701
0901:for ESD change to 100pF
PDG v1.2 update
0529 update
0625 update
PLT_RST Buffer
SPI ROM (8MByte) 1.8V
Reserve for EMI(Near SPI ROM)
Check Intel
RTC_RST
close to KB door
W=20mils
trace width 10mil
W=20mils
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47

Check power rail

USB2 Port 0 (USB3.0 P0)

Left USB Port

Right USB Port

USB HUB

USB3 Port 0

NOTE: Ref checklist rev1.0 p.25
USB_HSIC_RCOMP must NOT float if they are not being used.

ILB_LPC_CLK_0 : Output of 25MHz,
Need Check with EC

ILB_LPC_CLK_1 is for CLK_0 feedback.(Input)
Set to Outpot for Normal Usage

Check Intel for PU

Pull High at EC side

DDR(15,16)
Minicard(21)
EC(24)

GPIO_S0_SC_56:
A16 Swap Override
0 = Enable
1 = Disable
Reference EDS Page 216

0705 : Reserved

PDA (Platform Debug Assistant) Test Points

FH8065301546401_FCBGA131170

6 OF 13

Security Classification	Compal Secret Data		
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Title: VLV-M SOC USB/LPC/SMBus

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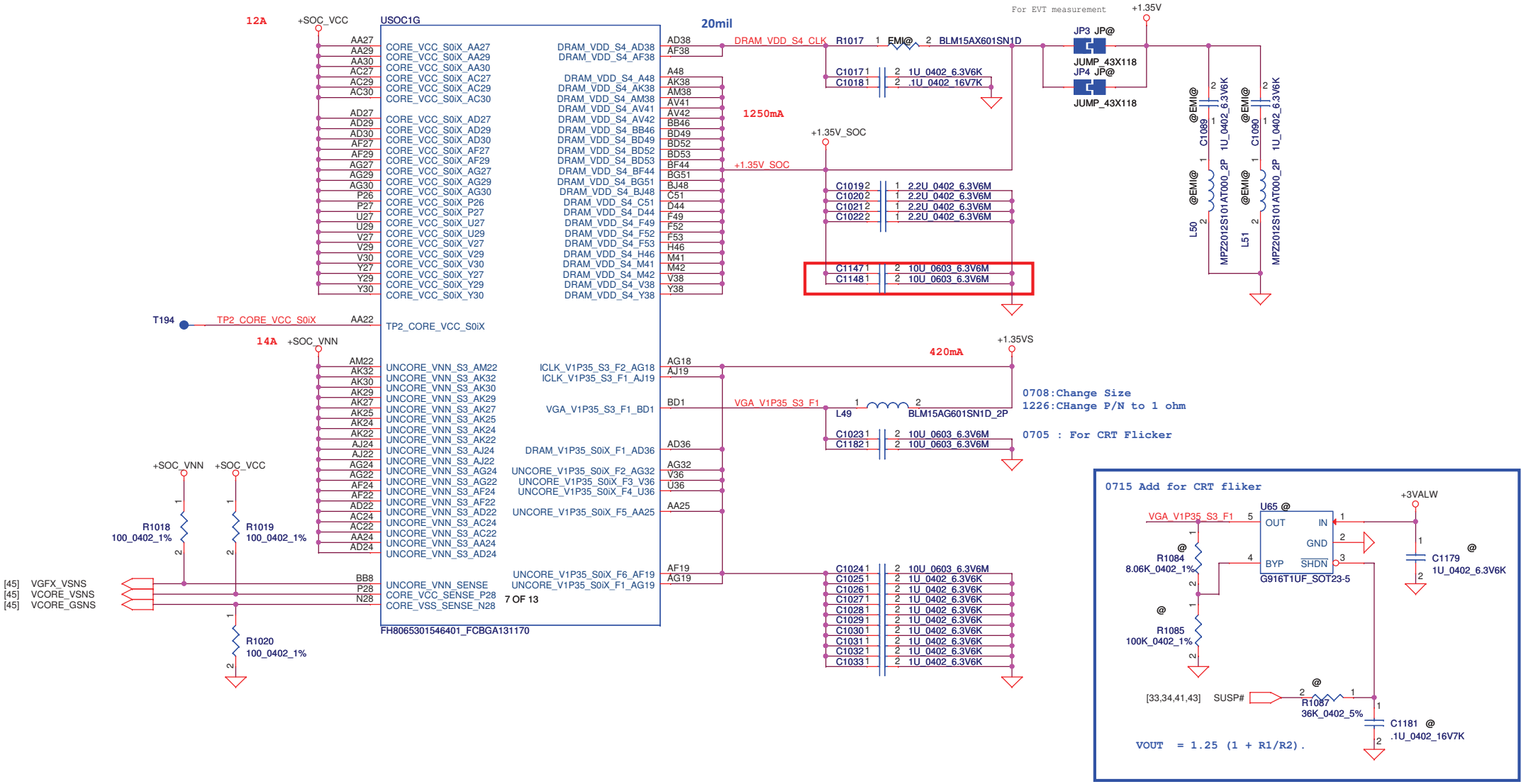

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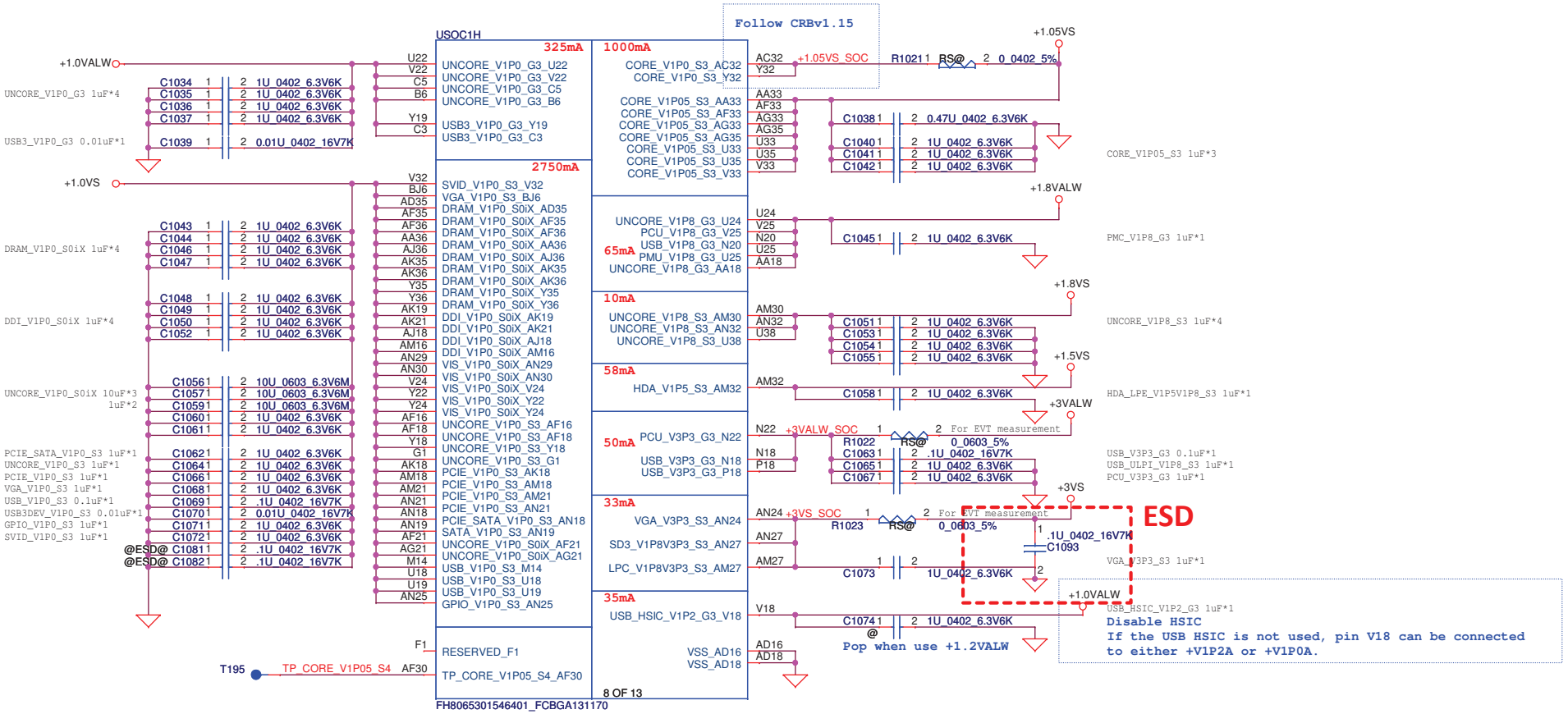
Compal Electronics, Inc.			
Title	VLV-M SOC Power		
Size: Custom	Document Number: Intel BayTrail-M Platform		Rev: 0.1
Date: Tuesday, February 18, 2014	Sheet 10 of 47		



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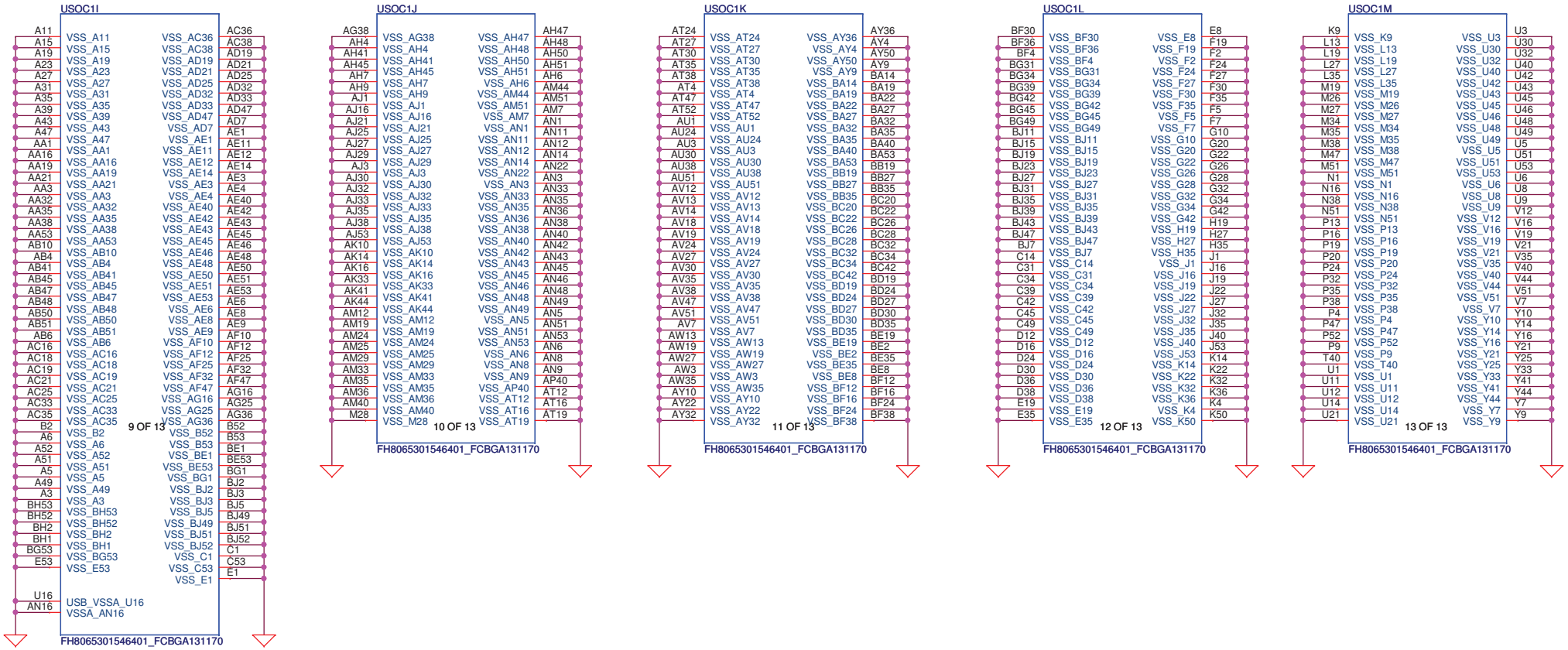
Title: VLV-M SOC Power

Size: Custom | Document Number: Intel BayTrail-M Platform | Rev: 0.2

Date: Tuesday, February 18, 2014 | Sheet 11 of 47



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Issued Date	2013/04/12	Deciphered Date	2014/04/12

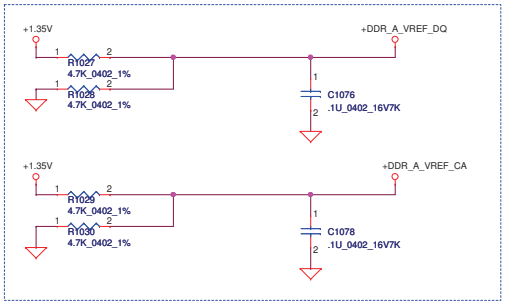
Compal Electronics, Inc.

Title: VLV-M SOC GND

Size: Custom | Document Number: Intel BayTrail-M Platform | Rev: 0.2

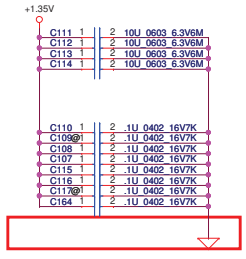
Date: Tuesday, February 18, 2014 | Sheet 12 of 47

Signal voltage level = 0.675 V
PLACE TWO 4.7K RESISTORS CLOSE TO
DIMMS ON DIMM_VREF_CA / DIMM_VREF_DQ
Decoupling caps are needed; one 0.1 µF placed close to VREF pins of each DDR3 SODIMM.

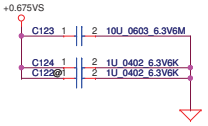


Layout Note:
Place near JDIMM1

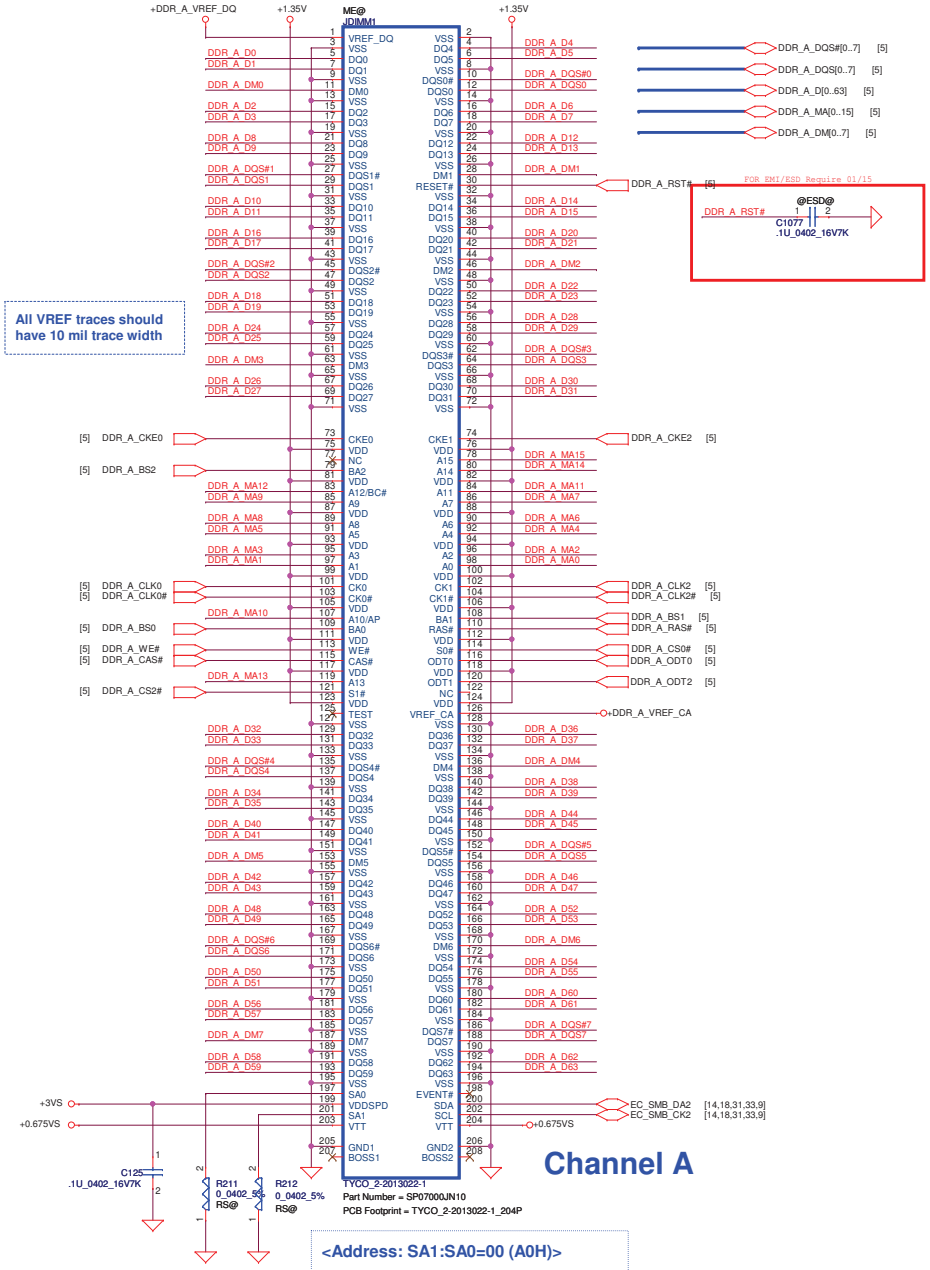
All VREF traces should have 10 mil trace width



0604 Change for layout space limit



Layout Note:
Place near JDIMM1.203,204



Channel A

<Address: SA1:SA0=00 (A0H)>

DIMM_1 STD H:4mm

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Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: DDR3L DIMMA

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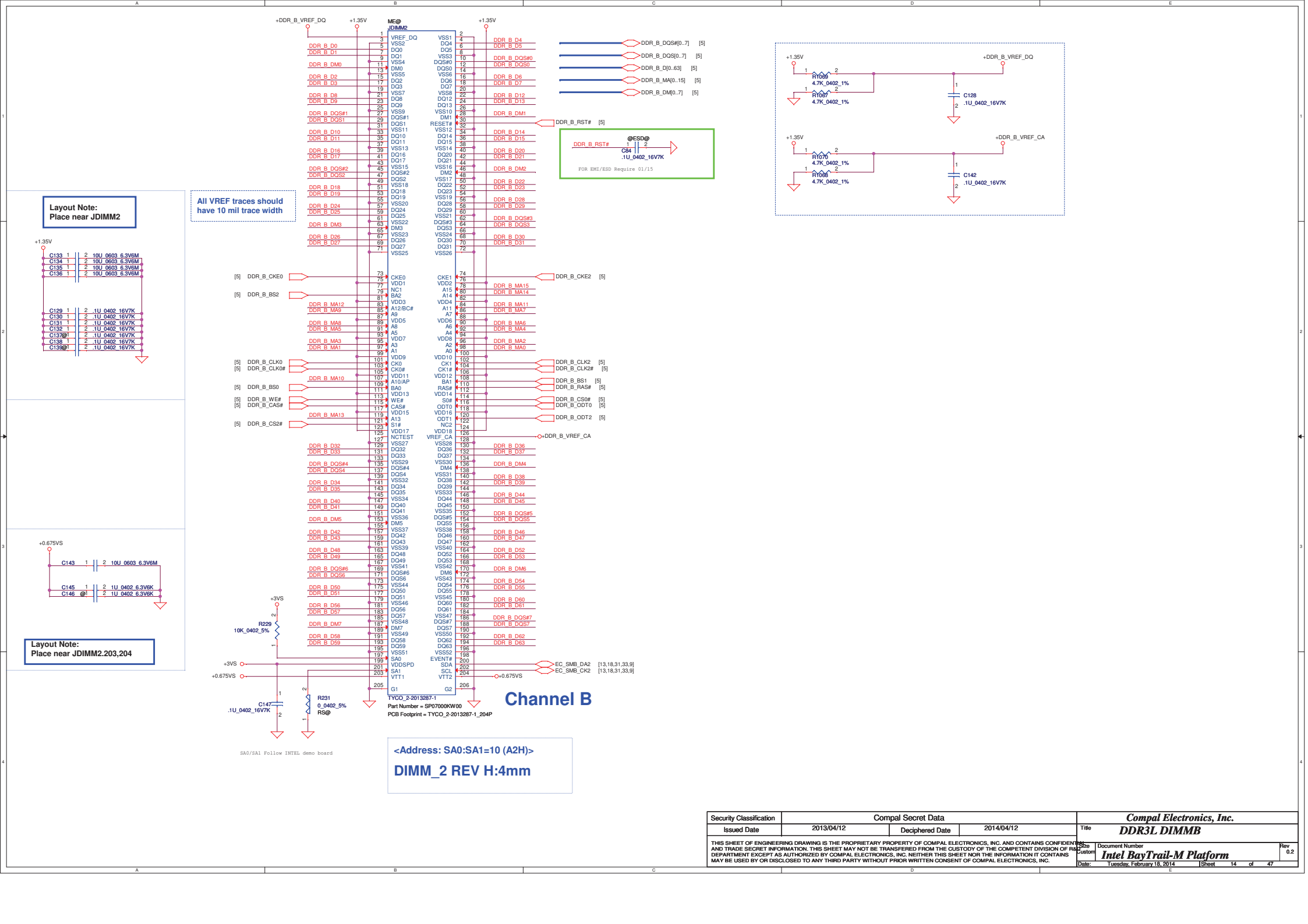
Date: Tuesday, February 18, 2014 | Sheet 13 of 47


Layout Note:
Place near JDIMM2
All VREF traces should have 10 mil trace width
Layout Note:
Place near JDIMM2.203,204
ME@
JDIMM2
TYCO_2-2013287-1
Part Number = SP07000KW00
PCB Footprint = TYCO_2-2013287-1_204P
Channel B
<Address: SA0:SA1=10 (A2H)>
DIMM_2 REV H:4mm
SA0/SA1 Follow INTEL demo board
@ESD@
FOR EMI/ESD Require 01/15
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Title
DDR3L DIMMB
Size
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Document Number
Intel BayTrail-M Platform
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Date:
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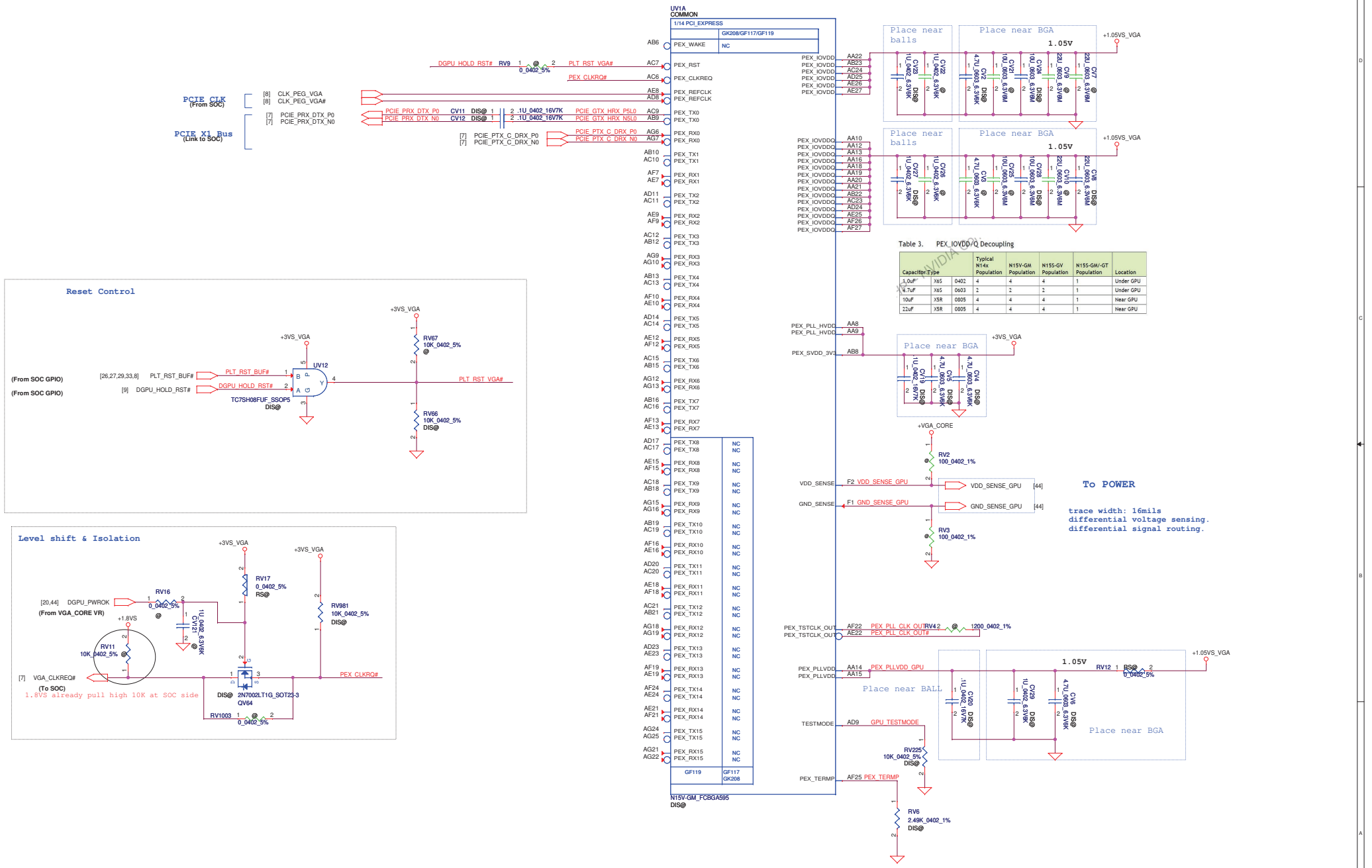

Security Classification	Compal Secret Data		
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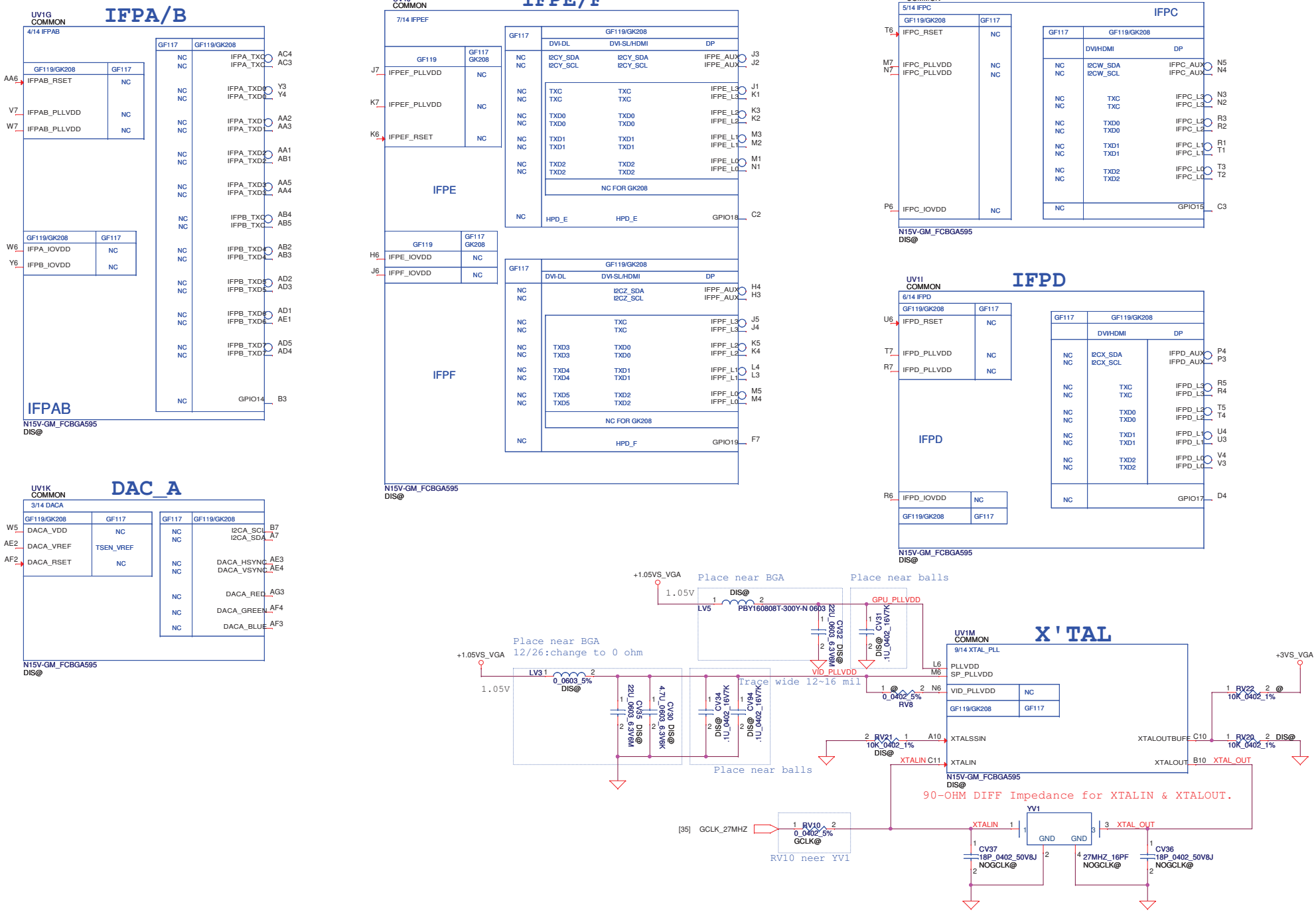
Title	NV(1/5)-PCIE		
Size	Document Number		Rev
D	LA-A721P		0.2
Date:	Tuesday, February 18, 2014	Sheet	15 of 47


IFPA/B
UV1G
COMMON
4/14 IFPAB
IFPAB
N15V-GM_FCBGA595
DIS@
IFPE/F
UV1J
COMMON
7/14 IFPEF
IFPE
IFPF
N15V-GM_FCBGA595
DIS@
IFPC
UV1H
COMMON
5/14 IFPC
N15V-GM_FCBGA595
DIS@
IFPD
UV1I
COMMON
6/14 IFPD
N15V-GM_FCBGA595
DIS@
DAC_A
UV1K
COMMON
3/14 DACA
N15V-GM_FCBGA595
DIS@
X'TAL
UV1M
COMMON
9/14 XTAL_PLL
N15V-GM_FCBGA595
DIS@
Place near BGA
Place near balls
Place near BGA
12/26:change to 0 ohm
Trace wide 12~16 mil
Place near balls
90-OHM DIFF Impedance for XTALIN & XTALOUT.
RV10 neer YV1
+1.05VS_VGA
+3VS_VGA
1.05V
GPU_PLLVDD
VID_PLLVDD
PBY160808T-300Y-N 0603
0_0603_5%
0_0402_5%
10K_0402_1%
18P_0402_50V8J
NOGCLK@
27MHZ_16PF
XTALIN
XTALOUT
XTALOUTBUFF
XTAL_OUT
GCLK_27MHZ
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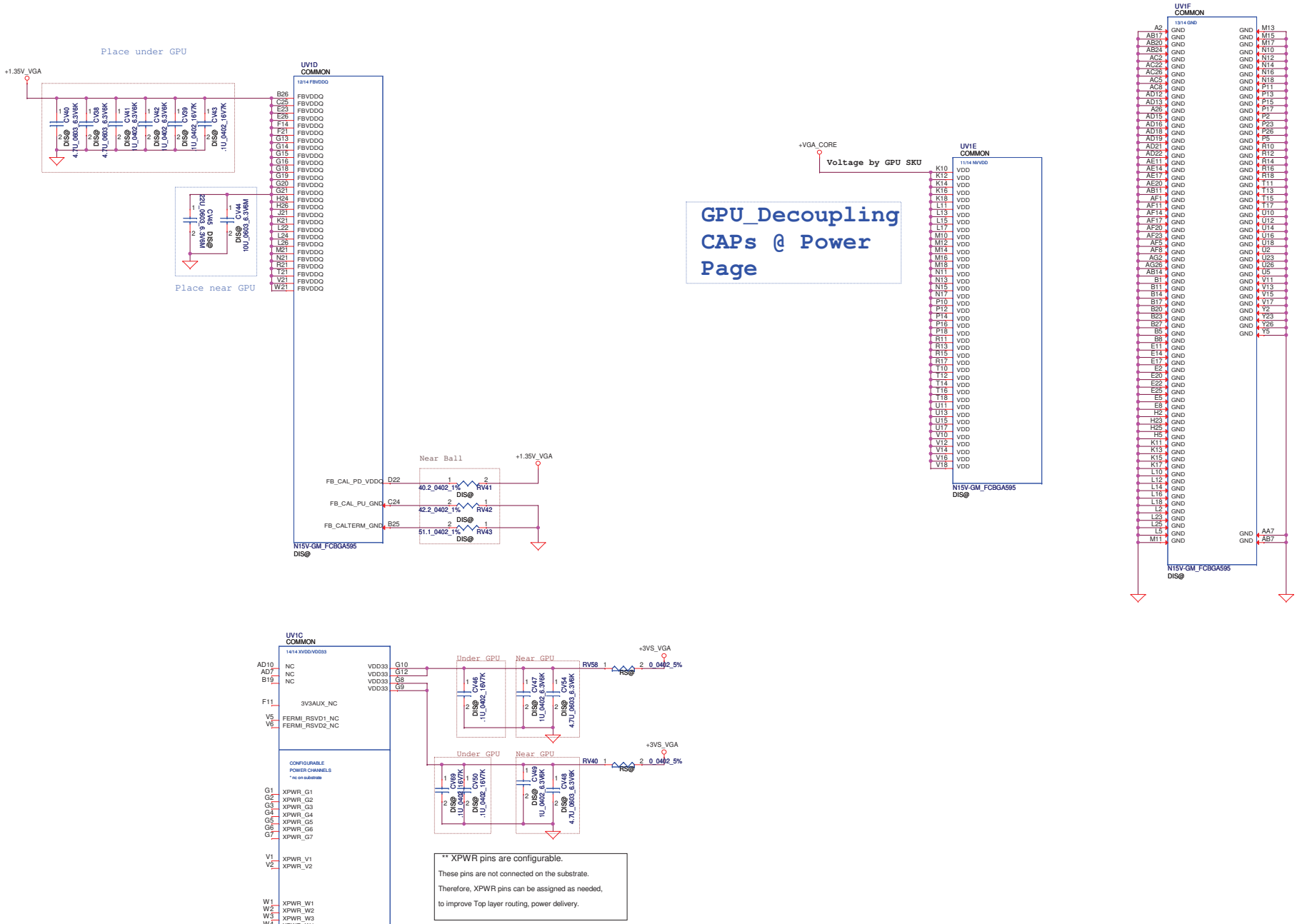
47



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Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.			
Title: NV(3/5)-POWER			
Size: C	Document Number: LA-A721P		Rev: 0.2
Date: Tuesday, February 18, 2014	Sheet: 17 of 47		

GPIO

VGA_THERMDN and VGA_THERMDP:
1. 5mil track width and spacing
2. 5mil grounded gurad tracks width and spacing
3. ground referenced
4. Connect guard tracks to pin5

For BSC using.

UV1N COMMON
8/14 MISC1
N15V-GM_FCBGA595
DIS@

I2CS SMBUS: 0x9E

15.5.6 SMB_ALT_ADDR Strap

This strap is used to configure the I2CS address of a GPU or the I2CS address slave address.

Table 15-8. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

To DGPU VR

To VGA_CORE VR,N15V-GM not support PSI function

+3VS Reserve for leakage issue

From EC

UV1L COMMON
10/14 MISC2
N15V-GM_FCBGA595
DIS@

Internal Thermal Sensor

Link to PCH SML1
PU @ PCH SIDE

L2N7002DW1T1G 2N SOT-363

STRAP

N15V-GM Binary Staps

Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10kΩ	Pull-down to GND
ROM_SI	SUB_VENDOR	10kΩ	•Pull-up to 3V3 if VBIOS ROM exists •Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10kΩ	Pull-down to GND (no display)

STRAP

N15V-GM Binary Staps

Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
STRAP0	RAM_CFG[0]	10kΩ	See note below
STRAP1	RAM_CFG[1]	10kΩ	See note below
STRAP2	RAM_CFG[2]	10kΩ	See note below
STRAP3	RAM_CFG[3]	10kΩ	See note below
STRAP4	PCIE_MAX_SPEED	10kΩ	Pull-down to GND

N15V-GM VRAM Straps: RAM_CFG (3..0)
[ROM_SI (3..0)]

	Hynix 2G	Micron 2G	Samsung 2G	Hynix 1G	Micron 1G	Samsung 1G
	H2G@	M2G@	S2G@	H1G@	M1G@	S1G@
Part Number =	X7654738L01	X7654738L02	X7654738L03	X7654738L04	X7654738L05	X7654738L06

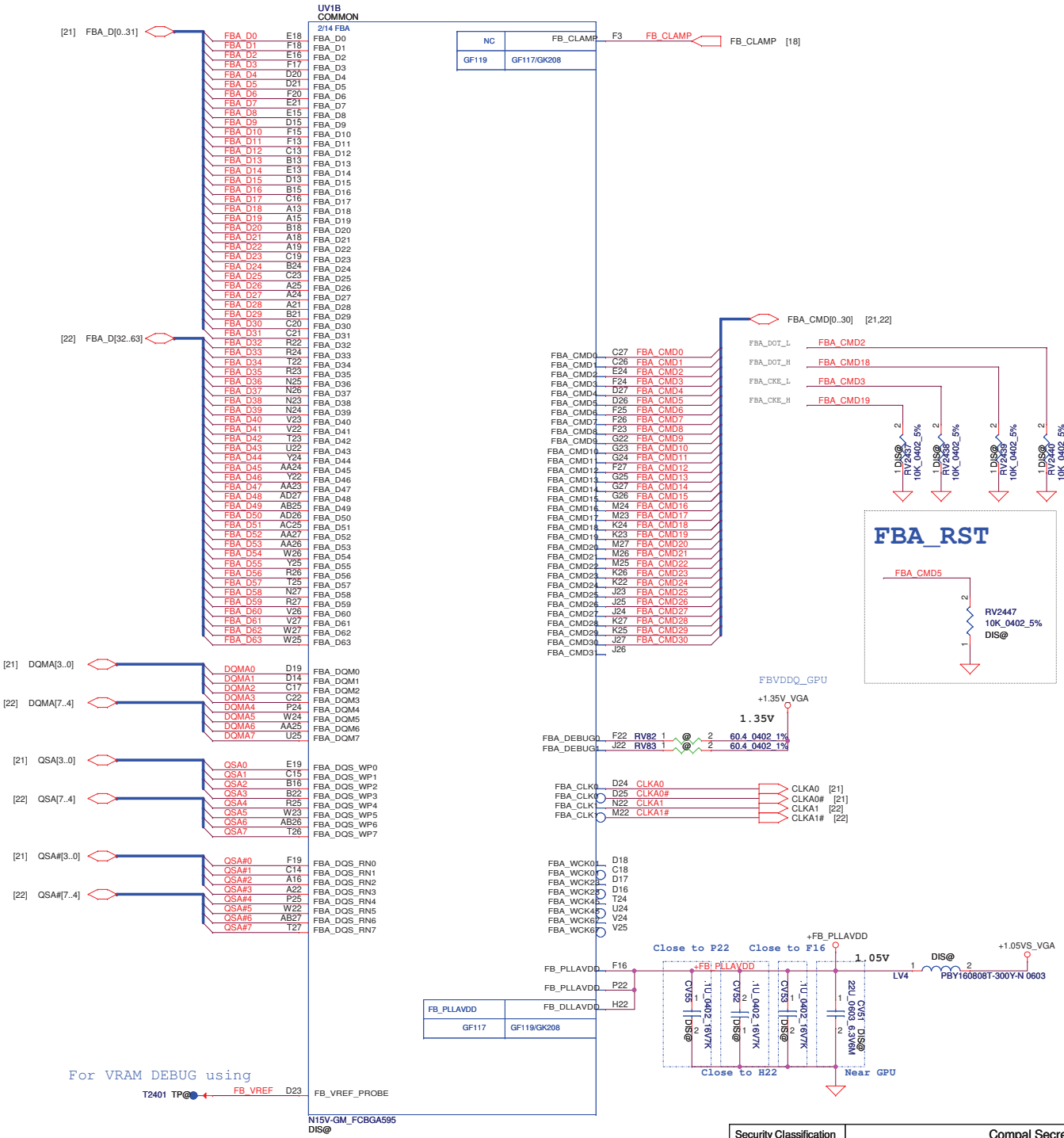
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: NV(4/5)-GPIO/Strap

Size: Custom | Document Number: LA-A721P | Rev: 0.2

Date: Tuesday, February 18, 2014 | Sheet 18 of 47



6.1.10 Memory ODTx, CKEx, and RST Termination

DDR3 requires Memory Termination on CKEx, ODTx and Memory Reset (RST). Table 6-8 describes the required termination.

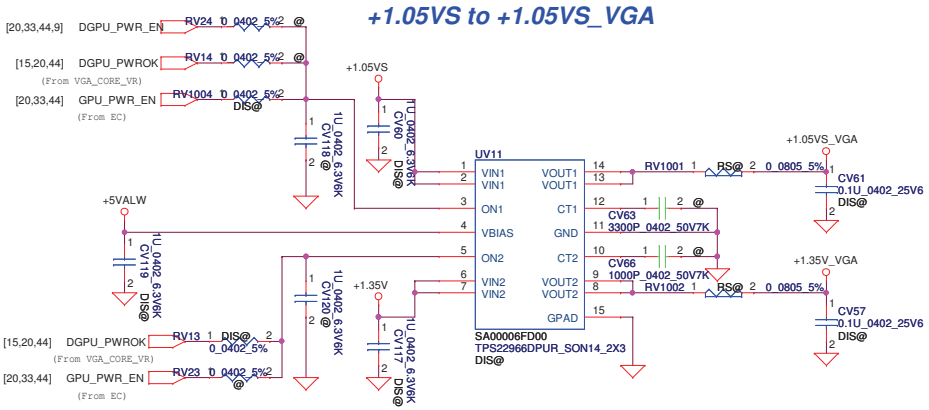
Table 6-8. Memory ODTx, CKEx, and RST Termination

DDR3 Command Bit	Default Pull-Down
ODTx	10 k
CKEx	10 k
RST	10 k
CS*	No Termination

Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

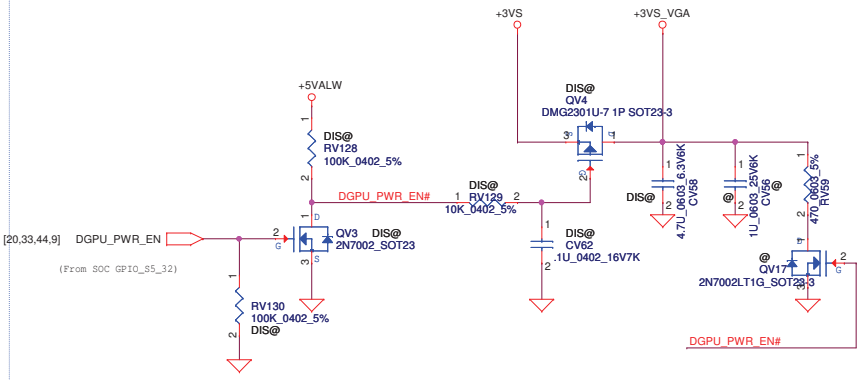
Compal Electronics, Inc.			
Title: NV(2/5)-MEMORY FBA			
Size: Custom	Document Number: LA-A721P		Rev: 0.2
Date: Tuesday, February 18, 2014	Sheet 19 of 47		

+1.05VS to +1.05VS_VGA

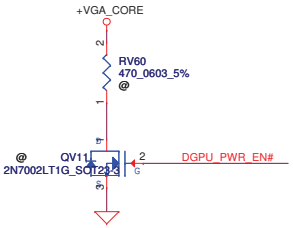


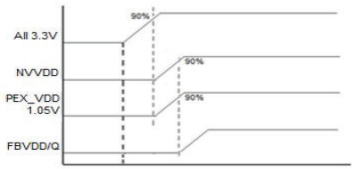
+1.35V_DGPU to +1.35V_VGA

+3VS_DGPU to +3VS_VGA



VGA_CORE discharge





Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-6. Example of Power-up Sequencing Order

Note:

- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.

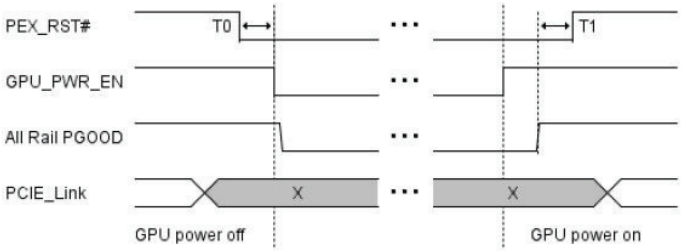


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

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Title: DGPU_DC/DC Interface

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Date: Tuesday, February 18, 2014 Sheet 20 of 47

Memory Partition A – Lower 32 bits [31..0]

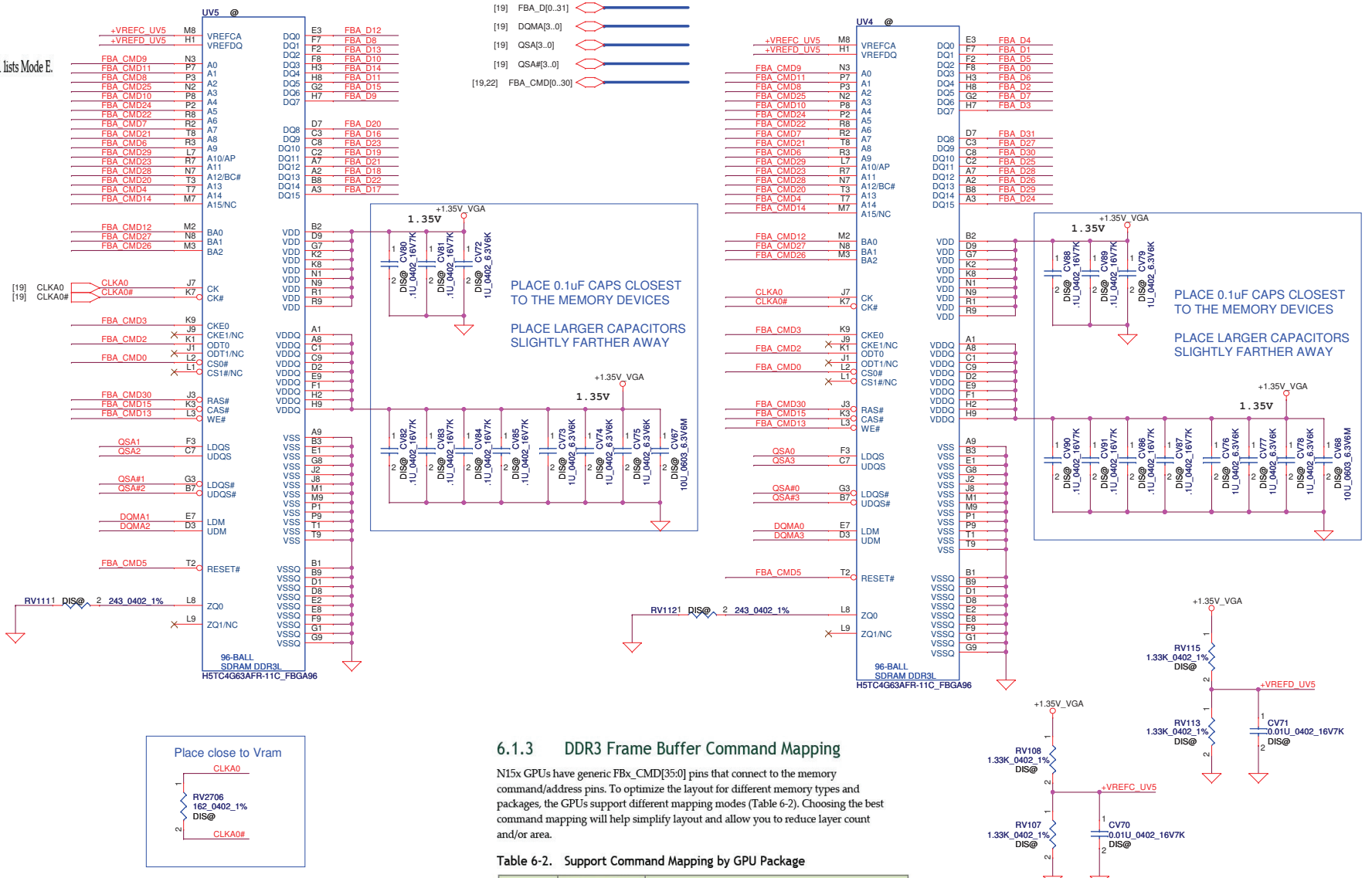
Table 6-3 lists the Mode D command mapping and Table 6-4 on page 91 lists Mode E.

Table 6-3. Mode D Command Mapping

N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*

N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS*	RAS*
FBx_CMD31		
FBx_CMD32		
FBx_CMD33[1]		
FBx_CMD34	DBG0[2]	
FBx_CMD35	DBG1[2]	

Notes:
1. Not available in GB2B-64 package.
2. GPU debug pins; not connected to DRAM. See section 6.1.11



6.1.3 DDR3 Frame Buffer Command Mapping

N15x GPUs have generic FBx_CMD[35:0] pins that connect to the memory command/address pins. To optimize the layout for different memory types and packages, the GPUs support different mapping modes (Table 6-2). Choosing the best command mapping will help simplify layout and allow you to reduce layer count and/or area.

Table 6-2. Support Command Mapping by GPU Package

Packages	Supported CMD Mapping for DDR3	Benefits
GB2B-64 GB4B-128	D	Mode D is optimized for N15x using DDR3 memory in the BGA96 package and is supported for single rank designs. Using this mode will allow routing in four signal layers[1]. This compact layout offers a high level of symmetry allowing higher speeds without requiring termination.
GB2B-64 GB4B-128	E	Mode E is optimized for DDR3 dual rank designs.

Note: [1]Not including two additional layers for power planes.

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Title: VRAM_DDR3_A Lower			
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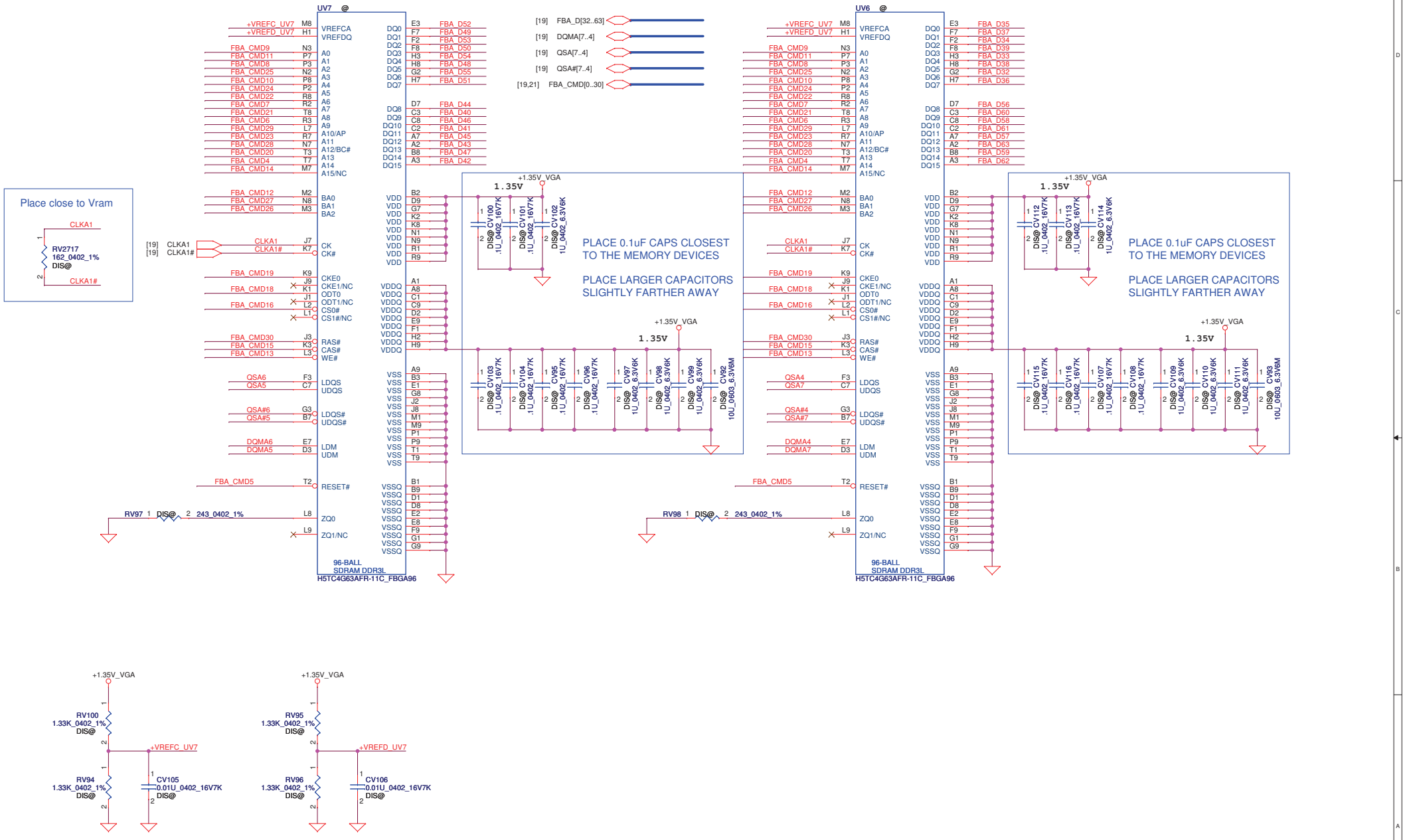
Date: Tuesday, February 18, 2014	Sheet 21 of 47		

Memory Partition A – Upper 32 bits [64..32]



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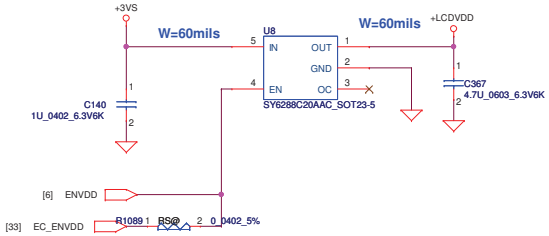
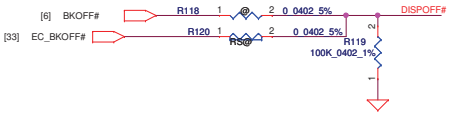
Title: VRAM_DDR3_A Upper

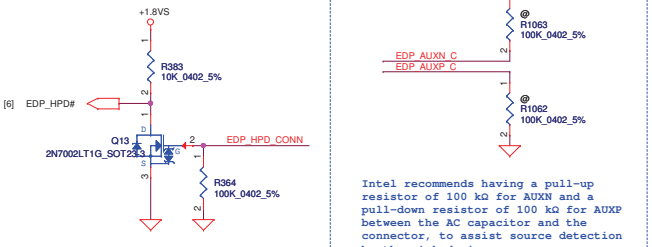
Size: Custom | Document Number: LA-A721P | Rev: 0.2

Date: Tuesday, February 18, 2014 | Sheet 22 of 47

LCD POWER CIRCUIT

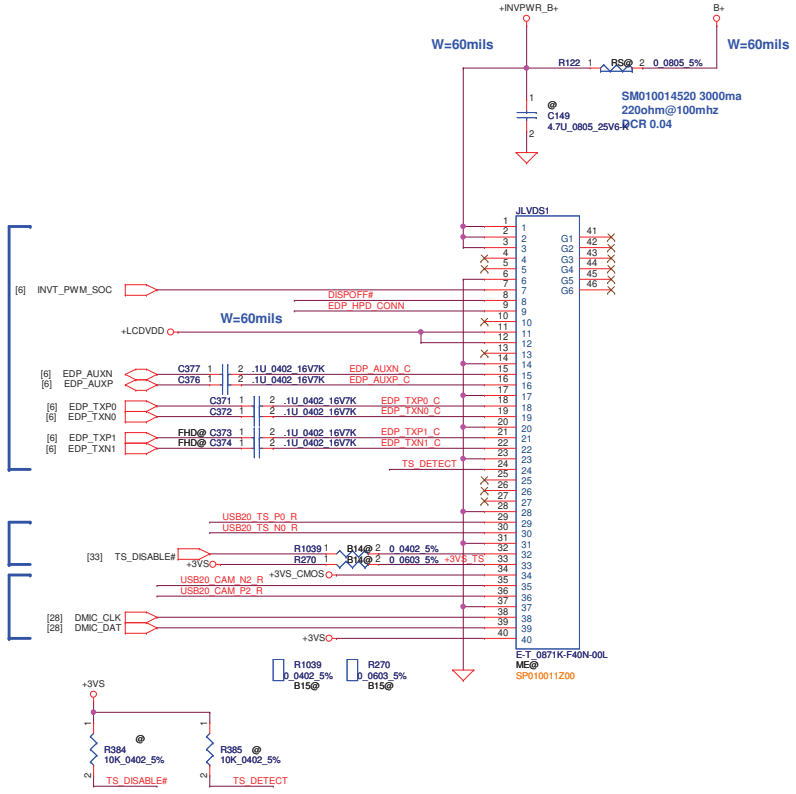




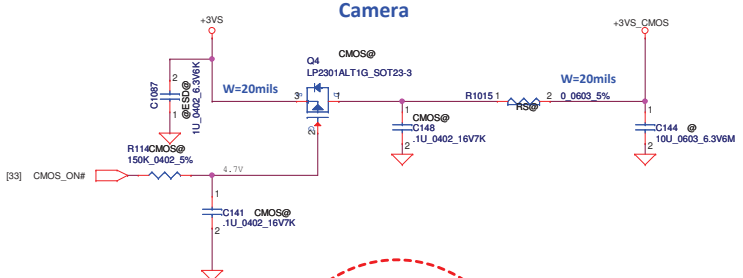


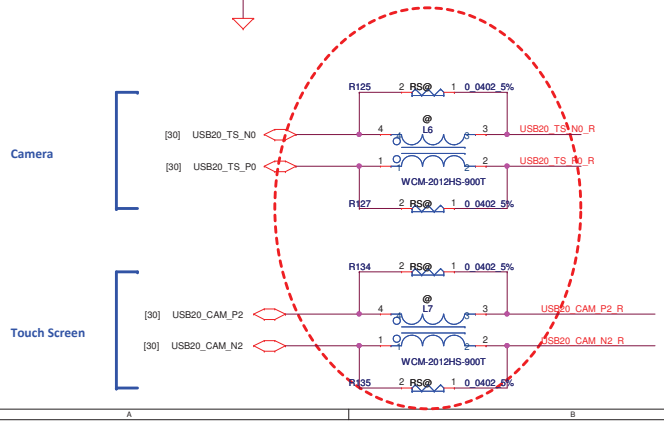
Intel recommends having a pull-up resistor of 100 kΩ for AUXN and a pull-down resistor of 100 kΩ for AUXP between the AC capacitor and the connector, to assist source detection by the sink device.

LCD/ LED PANEL Conn.



Camera





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Title: eDP CONN.

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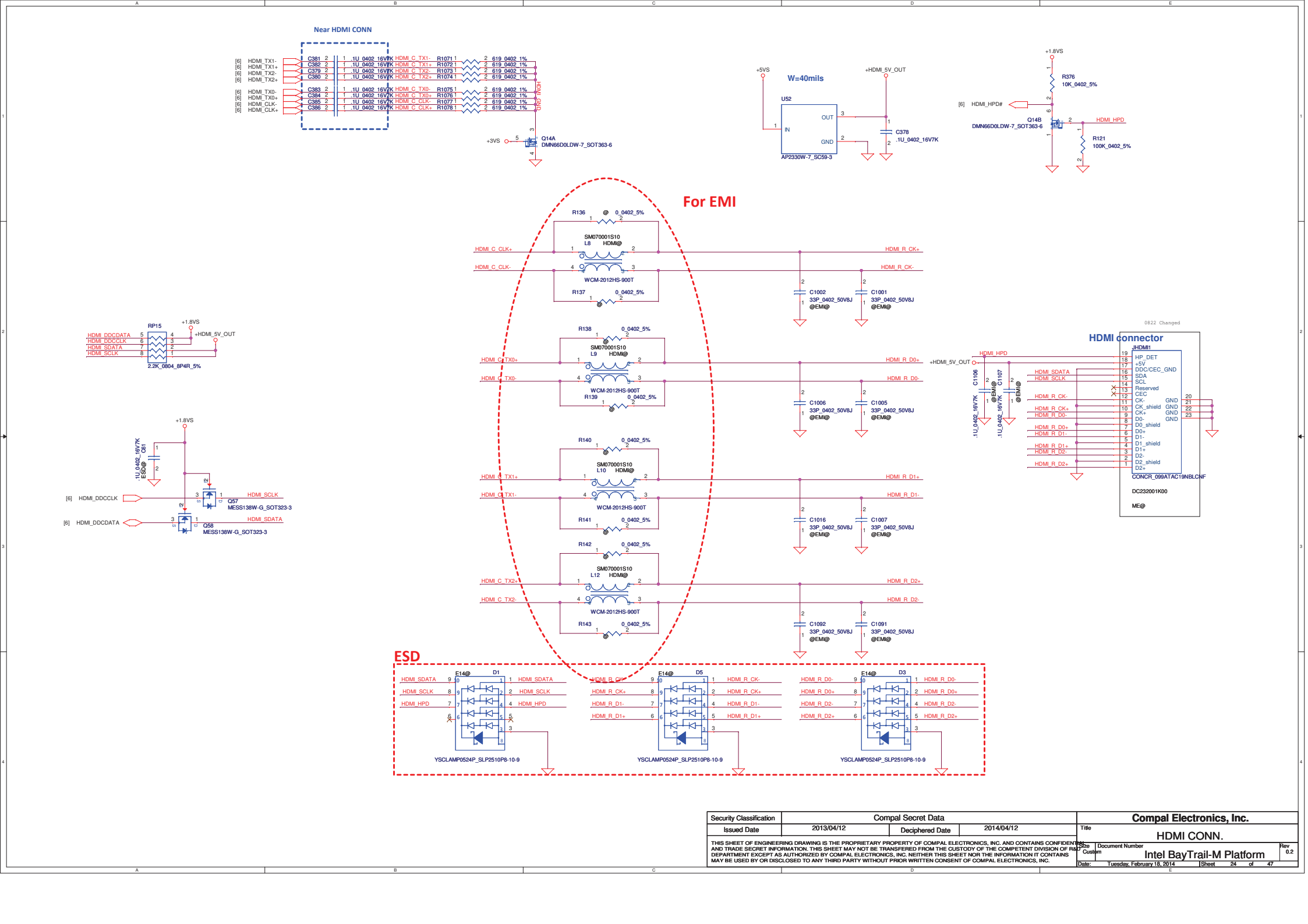

Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: HDMI CONN.

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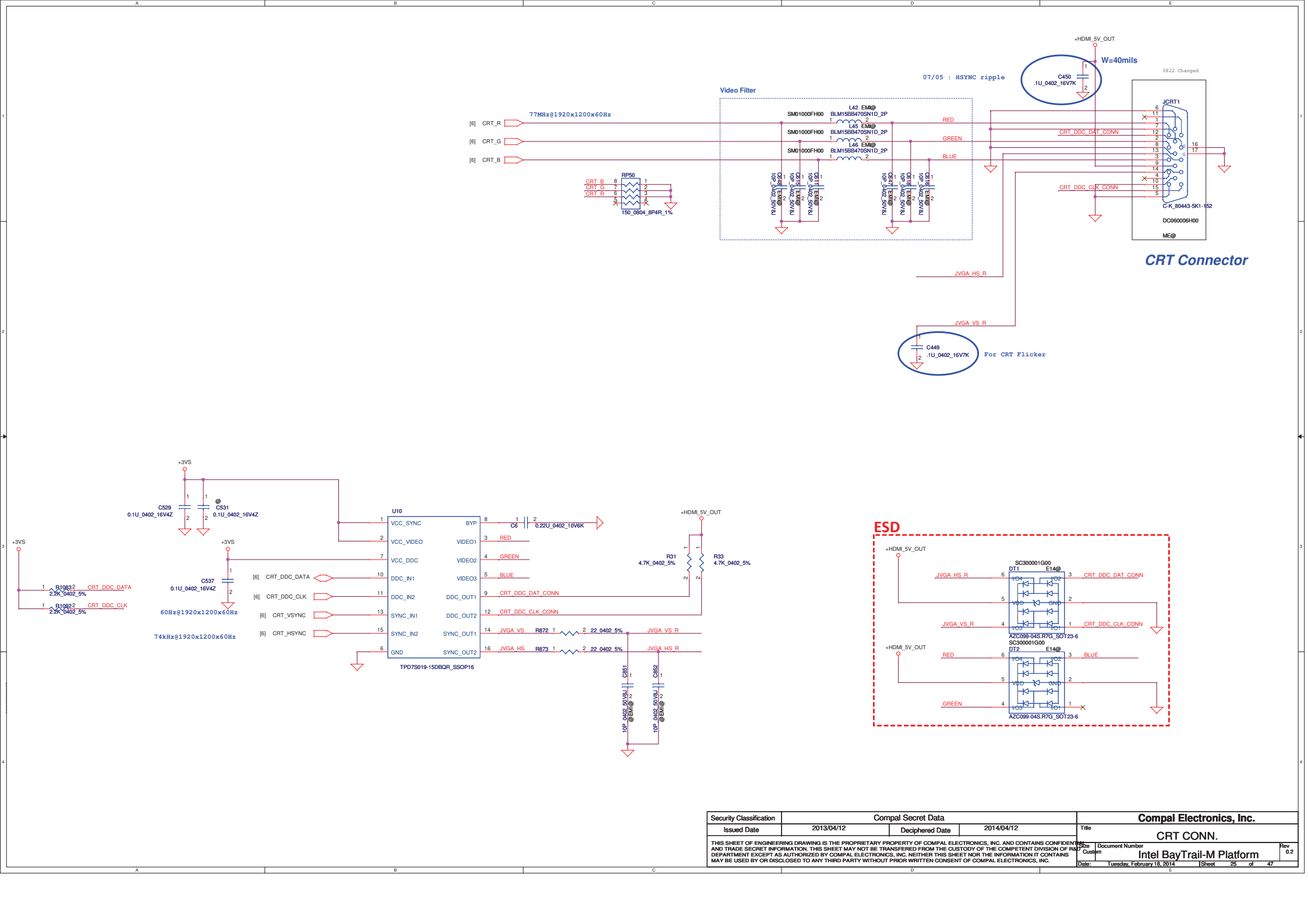

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: CRT CONN.

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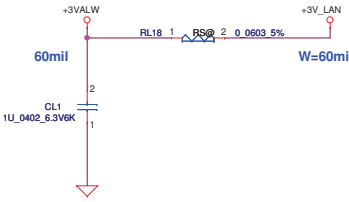
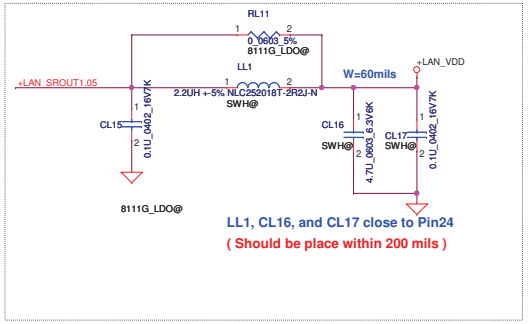
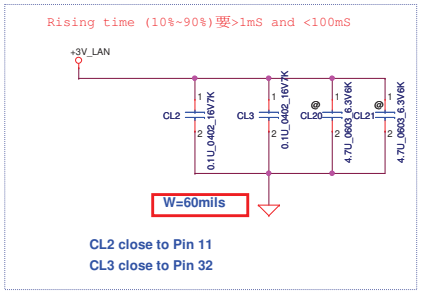
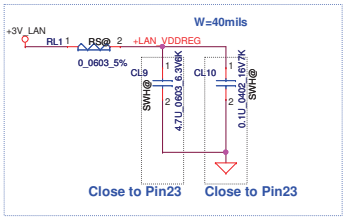


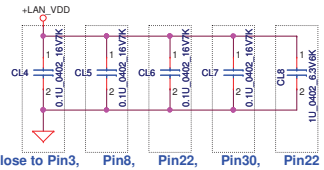


		1.0 V source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
SA00005Y700	RTL8111G	LDO	X	X	X	O	O
	~~RTL8111G~~	~~External~~	~~X~~	~~X~~	~~X~~	~~X~~	~~O~~
	RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X	X
SA00006Y700	RTL8106E	LDO	X	X	X	X	X

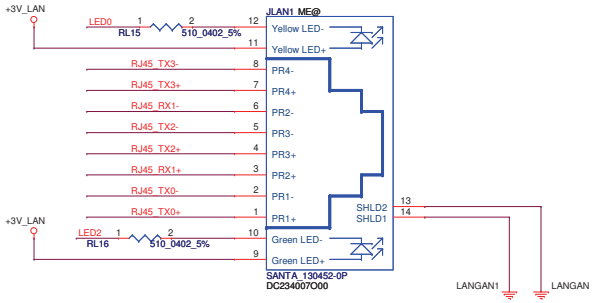
Please refer to the table above when using different 1.0V supply source.
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.

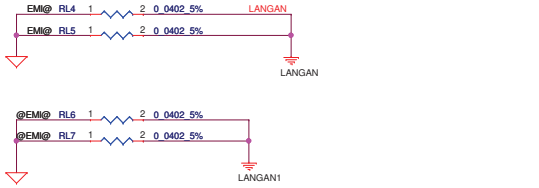


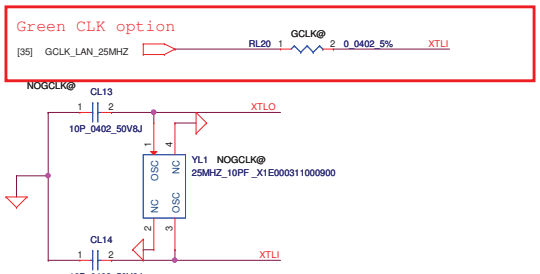


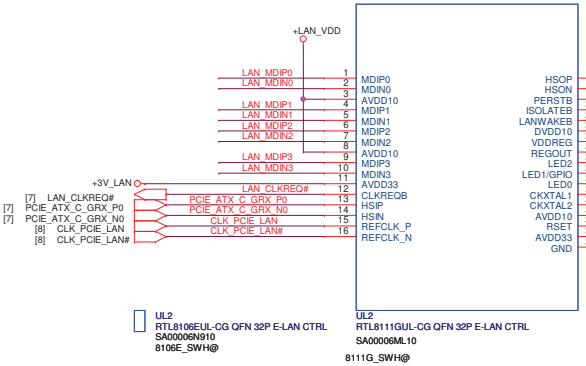


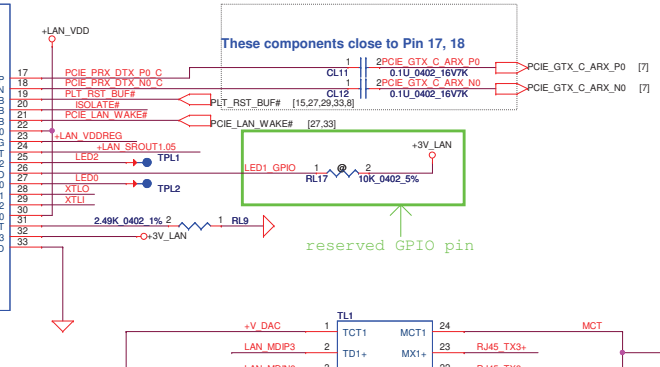
RJ-45 CONN.

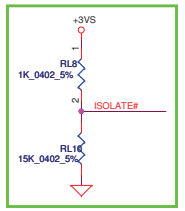


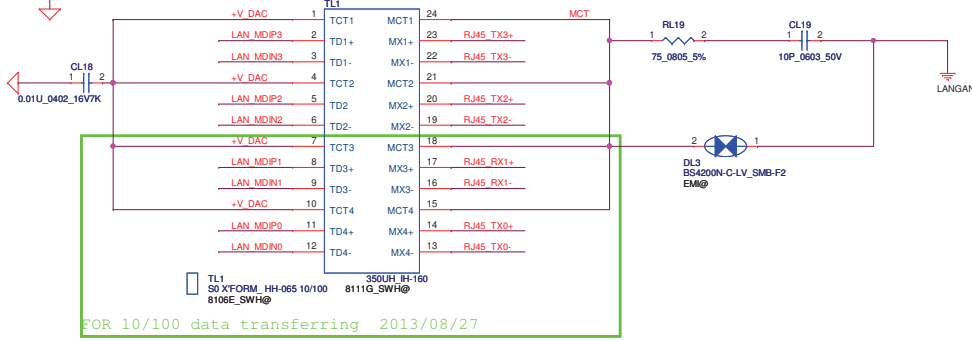


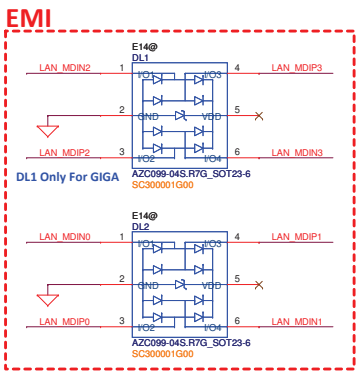












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Title: LAN RTL8111G/8106E

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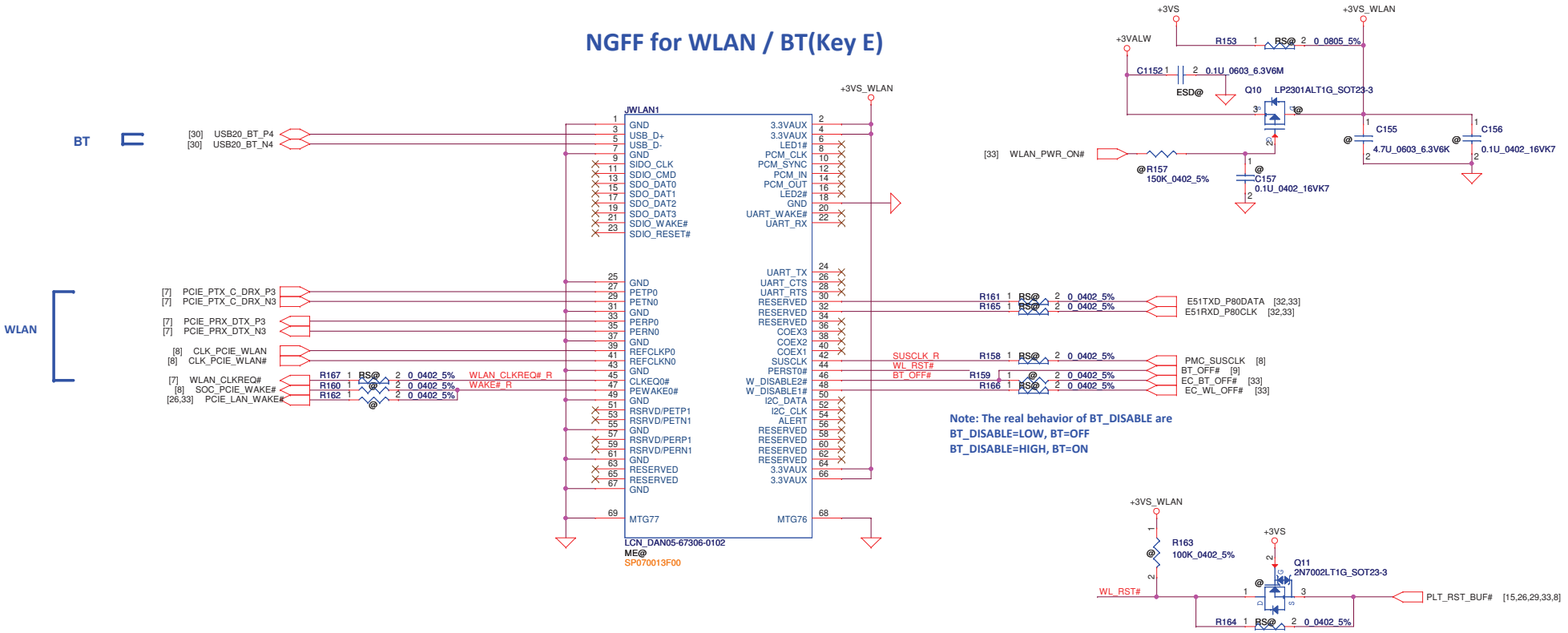
NGFF for WLAN / BT(Key E)



Note: The real behavior of BT_DISABLE are
BT_DISABLE=LOW, BT=OFF
BT_DISABLE=HIGH, BT=ON

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Issued Date	2013/04/12	Deciphered Date	2014/04/12

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Title: Mini PCIE(WLAN)		
Size: Custom	Document Number: Intel BayTrail-M Platform	Rev: 0.2
Date: Tuesday, February 18, 2014	Sheet 27 of 47	

600ohms @100MHz 2A
P/N: SM01000EE00

Place near Pin25

Place near Pin26

Place RA41 on AGND/DGND moat

Place near Pin40

Place near Pin1

Place near Pin9

Change power rail from +CHGRTC to +3VLP

For ALC233 only

wide 40MIL

Headphone

External DMIC

ALC233-CG

RA18 pop on ALC283, NC on ALC233

For EMI

GND GNDA

UA2
ALC233-VB2-CG MQFN 48P
233VB@
SA00007BF10

For ALC233VB only

Combo Jack
(Normal Open)

W=40mils
W=40mils

For Universal Audio Jack

11/20 Change symbol of JSPK1 to SP02000H700

follow vendor suggest
& reserver default design

PC Beep

EC Beep

PCH Beep

wide 40MIL

For EMI

DVT, NO.31

AZC099-04S.R7G_SOT23-6

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Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: HD Audio Codec_ALC3225

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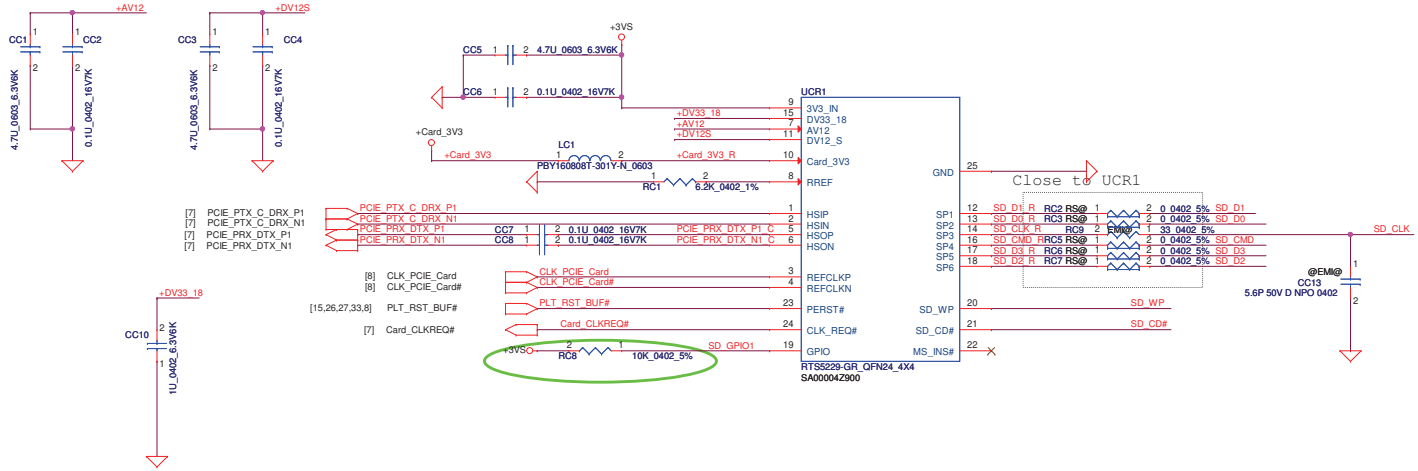
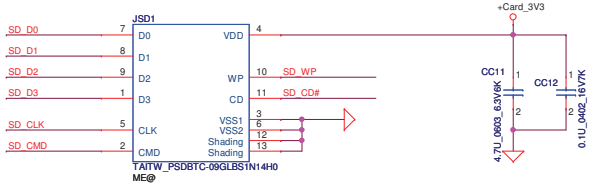


SD/SDXC



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Issued Date	2012/10/11	Deciphered Date	2014/10/11

Compal Electronics, Inc.

Title: P29-CardRead/RTS5229

Size: Custom | Document Number | Rev: 0.2

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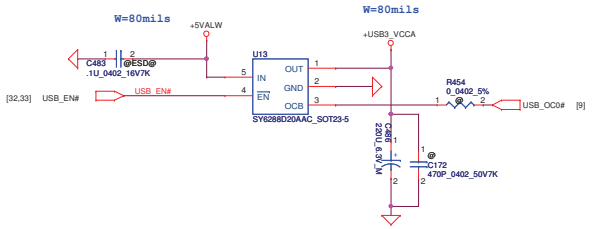
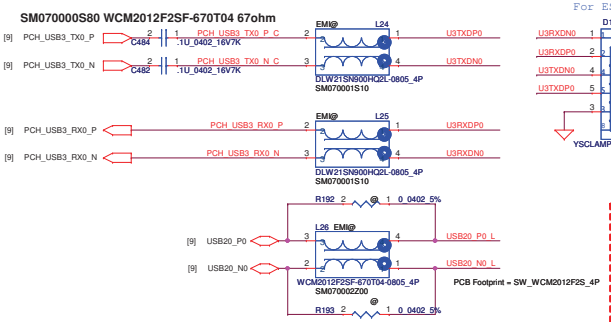
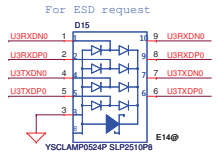
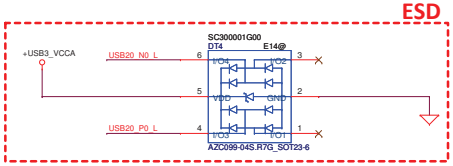
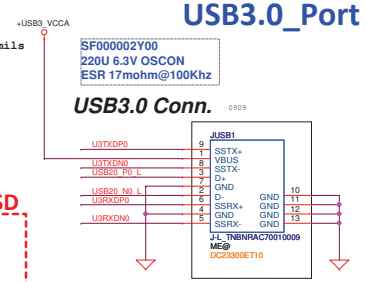
USB3.0_Port



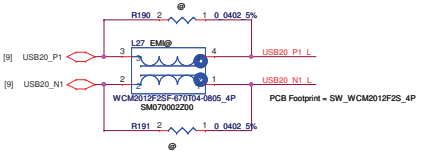


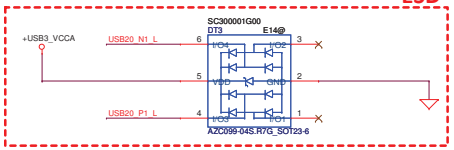


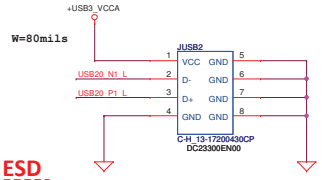




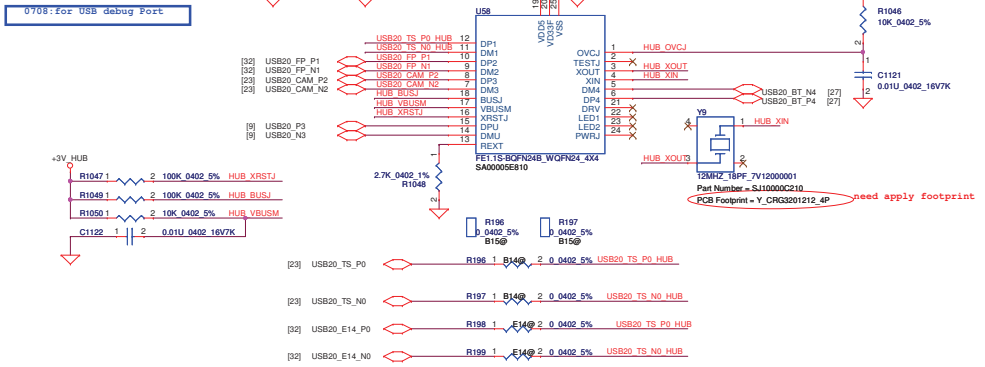
USB2.0_Port







USB2.0 HUB



Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: USB Conn & Hub FE1.1S

Size: Custom | Document Number: Intel BayTrail-M Platform | Rev: 0.1

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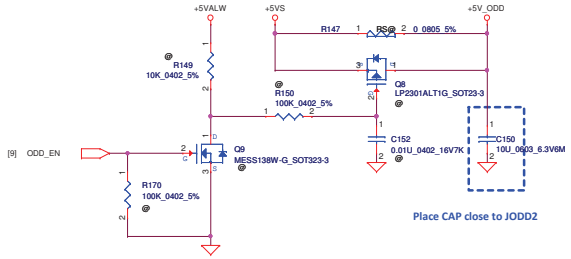
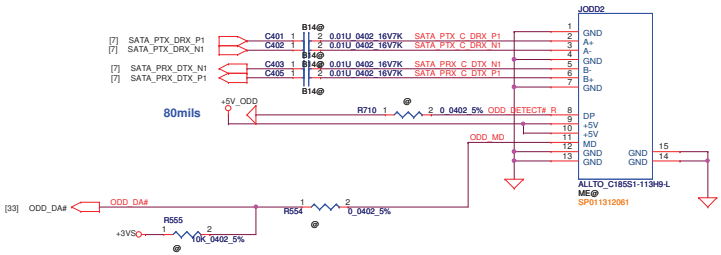
ODD



FOR 14"

C401 B14@ 0.01U_0402_16V7K
C402 B14@ 0.01U_0402_16V7K
C403 B14@ 0.01U_0402_16V7K
C405 B14@ 0.01U_0402_16V7K

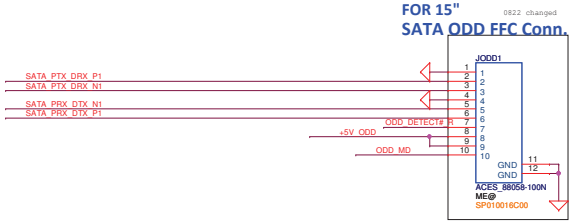
SATA ODD Conn.



FOR 15"

0822 changed

SATA ODD FFC Conn.

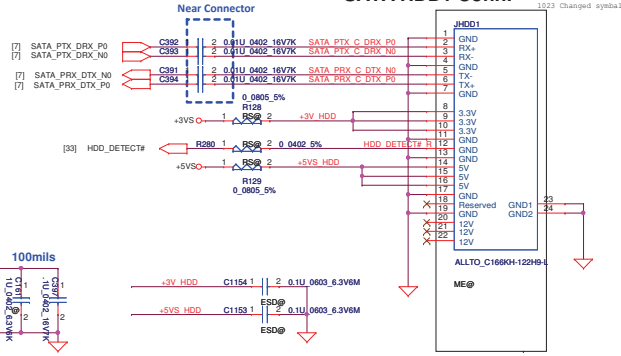


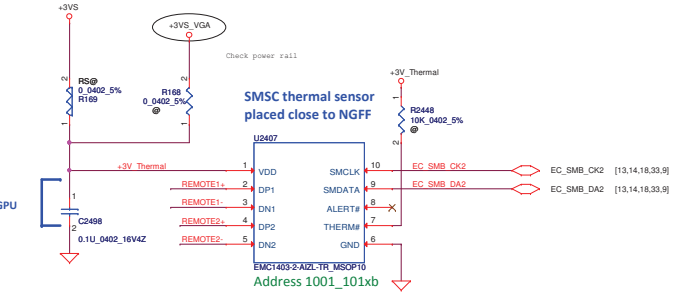
HDD

Near Connector

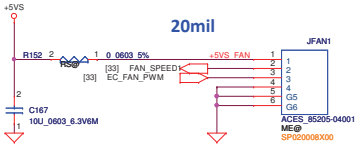
SATA HDD1 Conn.

1023 Changed symbol

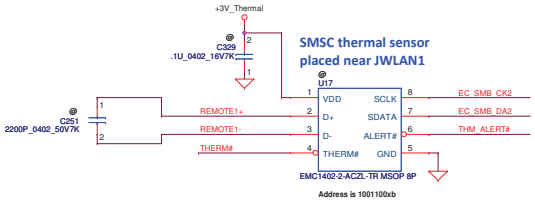


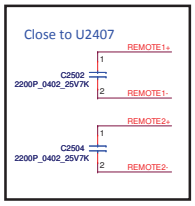


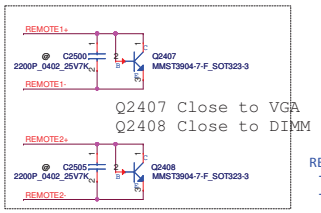
FAN Conn



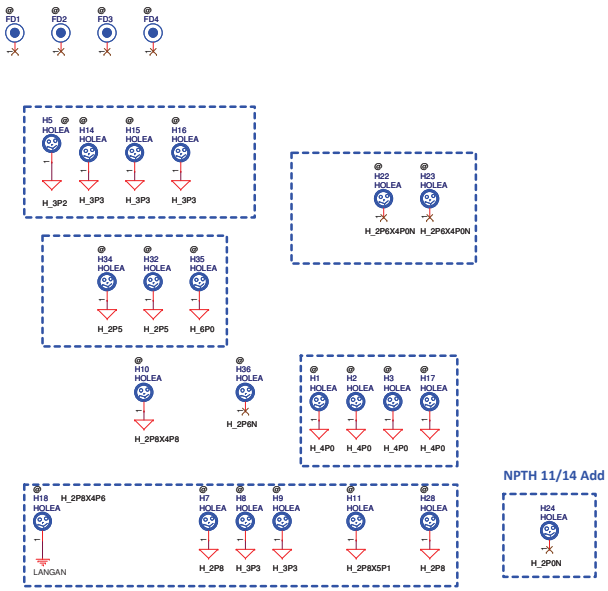
2 Channel





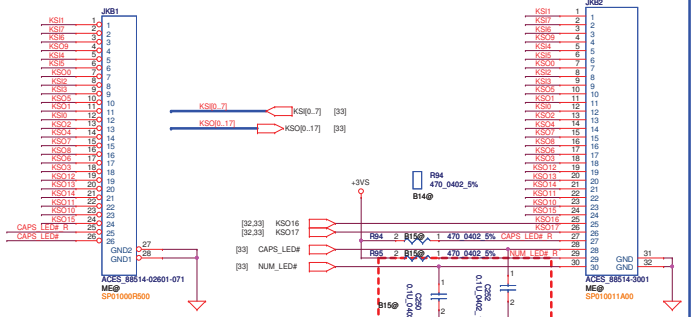


REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"



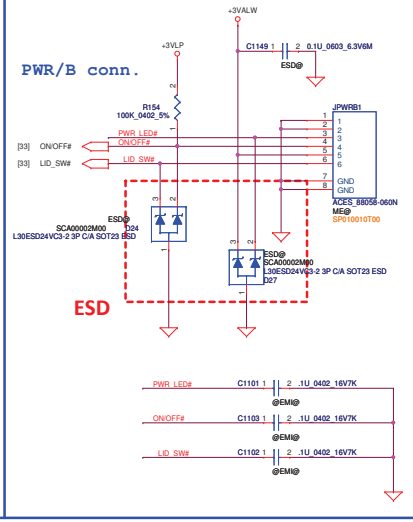
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/04/12	Deciphered Date	2014/04/12
Title	HDD/ODD/FAN/Screw Hole		
Size: Custom	Document Number: Intel BayTrail-M Platform		Rev: 0.1
Date: Tuesday, February 18, 2014	Sheet 31 of 47		

KB For B14/E14

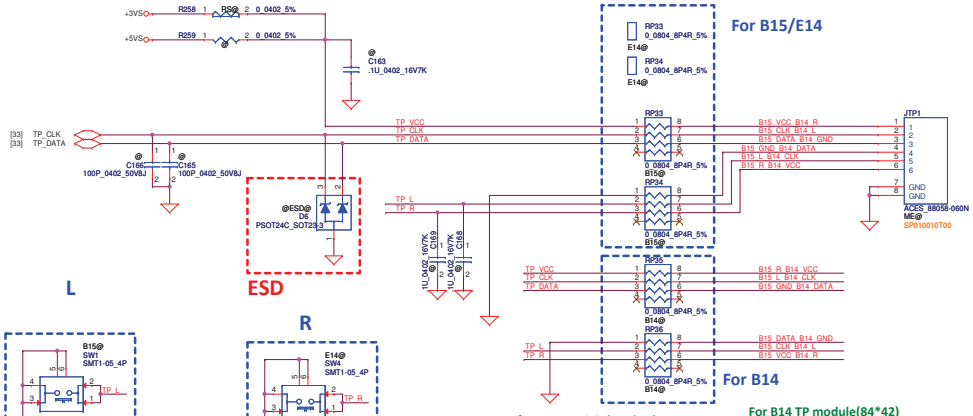


KB For B15

PWR/B conn.



For B15/E14



For B14

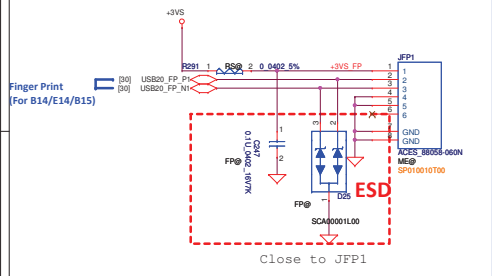
For B15/E14 TP module(100*50)

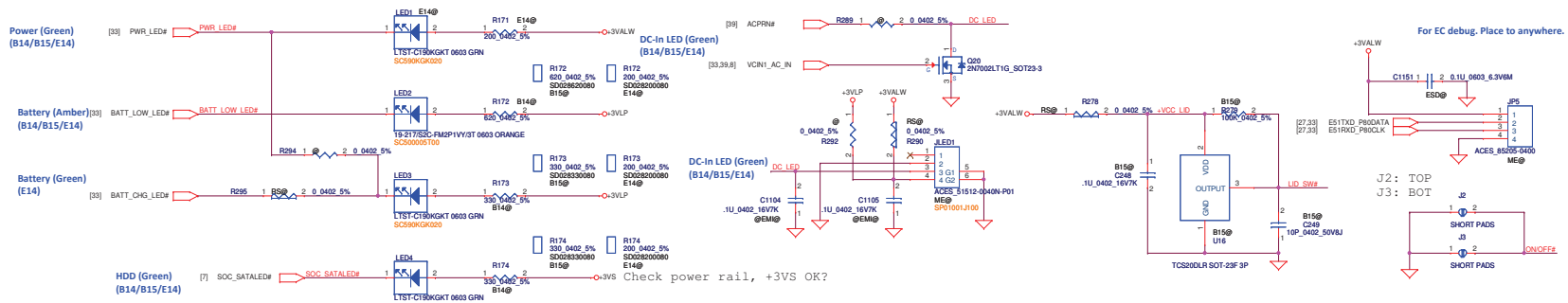
1	1	VCC	1	VCC	
2	2	CLK	2	CLK	
3	3	DAT	3	DAT	
4	4	GND	4	L	
5	5	L	5	R	
6	6	R	6	GND	

For B14 TP module(84*42)

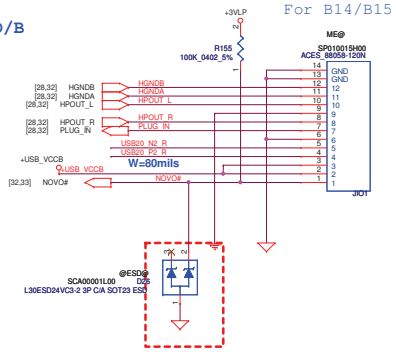
6	1	VCC	1	VCC	
5	2	CLK	2	CLK	
4	3	DAT	3	DAT	
3	4	GND	4	L	
2	5	L	5	R	
1	6	R	6	GND	

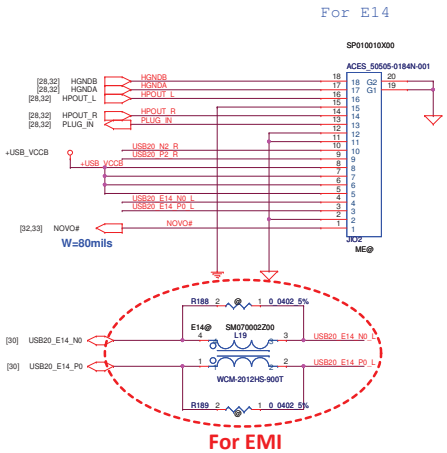
Finger Printer conn.

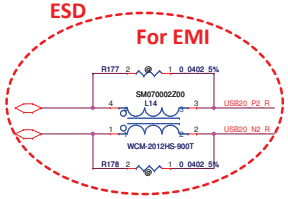


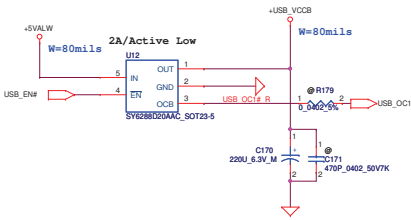


IO/B









Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.	
Title	KB/TP/LED/TPM
Size: Custom	Document Number: Intel BayTrail-M Platform
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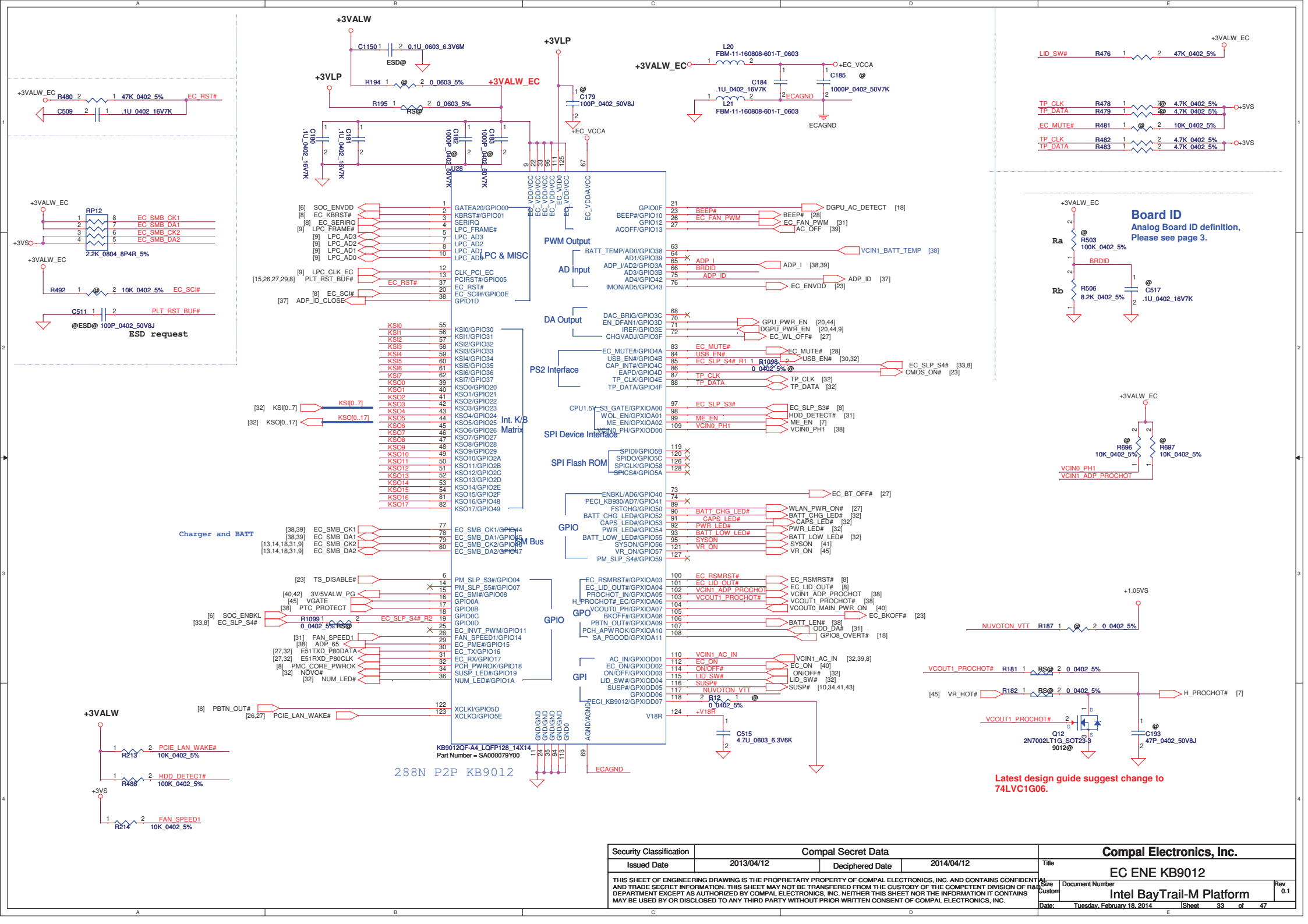
Date: Tuesday, February 18, 2014	Sheet 32 of 47



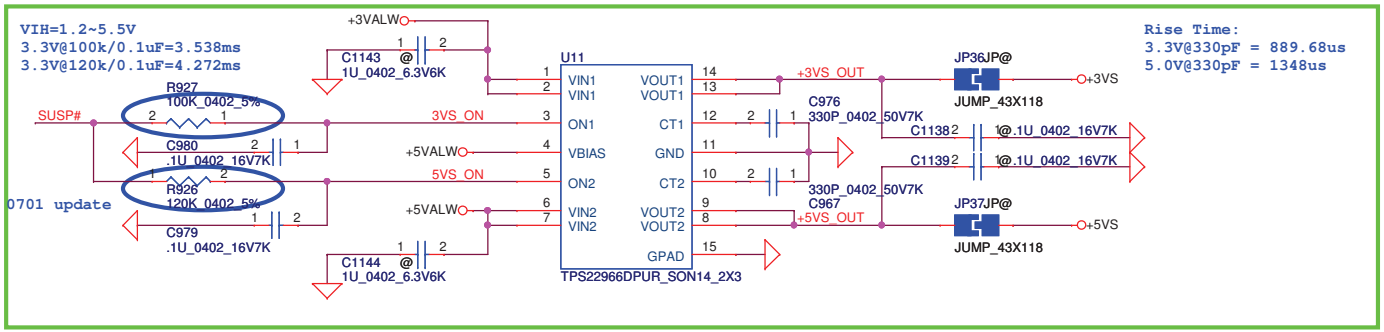
Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

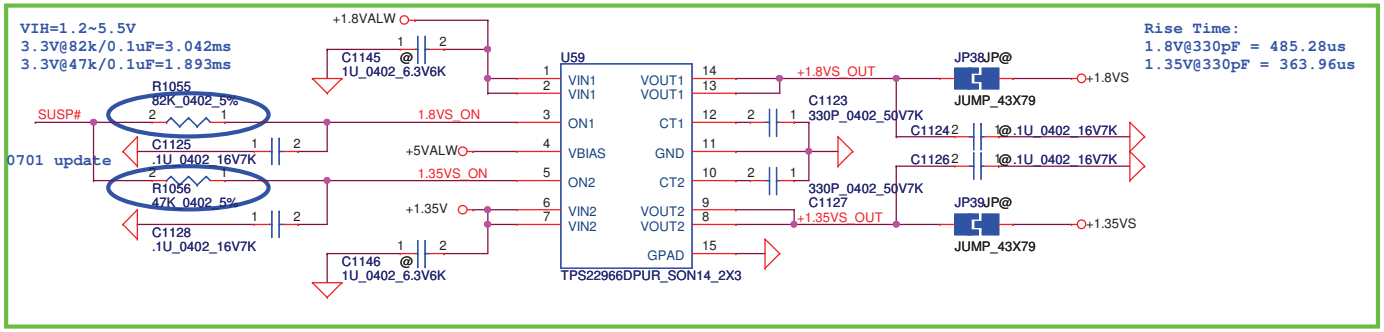
Compal Electronics, Inc.

Title: EC ENE KB9012

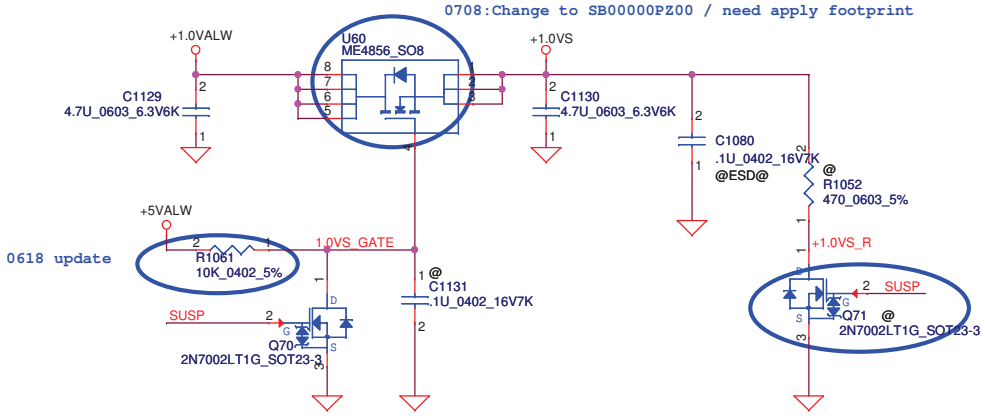
Size: Custom | Document Number: Intel BayTrail-M Platform | Rev: 0.1

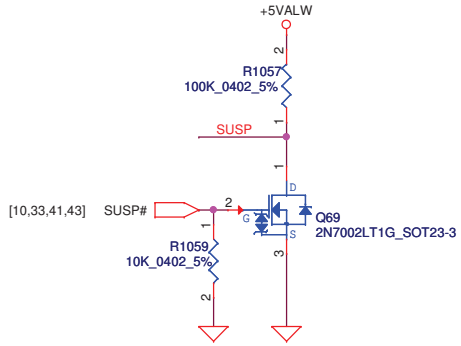
Date: Tuesday, February 18, 2014 | Sheet 33 of 47

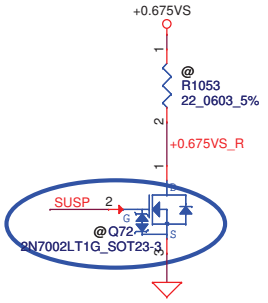




+1.0VALW TO +1.0VS







Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

Compal Electronics, Inc.

Title: DC INTERFACE

Size: Custom | Document Number: Intel BayTrail-M Platform | Rev: 0.1

Date: Tuesday, February 18, 2014 | Sheet 34 of 47

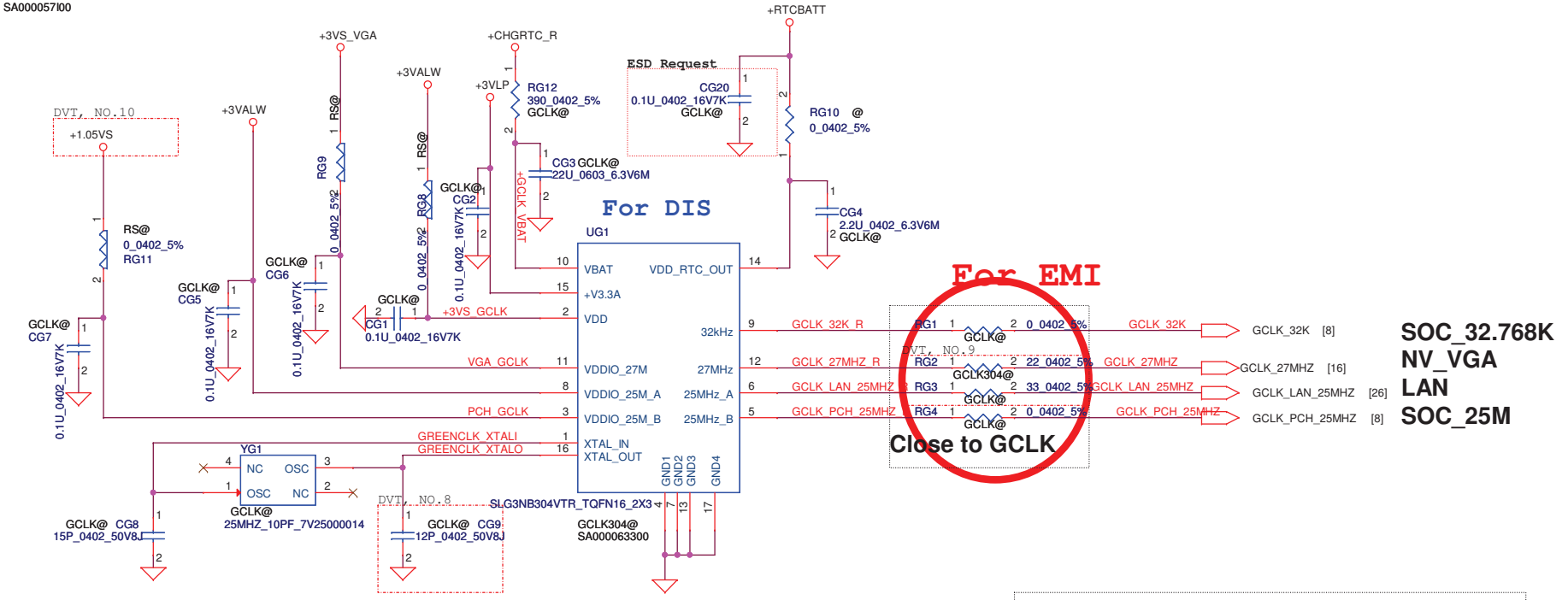
For UMA

UG1 GCLK244@

SLG3NB244VTR_TQFN16_2X3

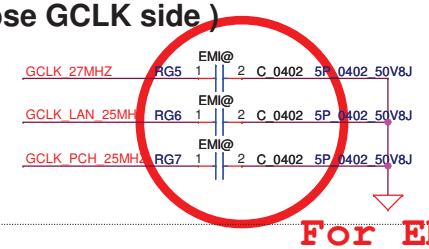
SA000057I00

Every power trace need:
W=20mils



SOC_32.768K
NV_VGA
LAN
SOC_25M

Reserved for Swing Level adjustment
(Close GCLK side)



Security Classification	Compal Secret Data		
Issued Date	2012/10/11	Deciphered Date	2014/10/11

Title: *P35-GCLK*

Size: Custom | Document Number | Rev: 0.3

Date: Tuesday, February 18, 2014 | Sheet 35 of 47

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Rework verify	Phase
1	Add Net "EC_SLP_S4#_R1" and "EC_SLP_S4#_R2 by vendor suggestion	33	Add R1098,R1099	V	SIV
2	Reduce component count,delete 12 pcs resister and add 4 pcs row resister.	32	Delete R311,R312,R313,R265,R266,R298,R316,R315, R314,R302,R303,R304, Add RP33,RP34,RP35,RP36	V	SIV
3	Audio vendor suggestion	28	Change CA16,CA13,CA19,CA14 from 0603 to 0402 Change CA11 from 4.7u to 1u , unpop CA17.	V	SIV
4	Nuvoton suggestion to add resister at PIN118 to GND	33	Add R12	V	SIV
5	ESD Team solution		Add C60,C61,C62,C514,C516,C518,C519,C520,D27(reserve)	V	SIV
6	HW strap pin	8	Add R1100,R1101,R1102,R1103,R1104,R1105	V	SIV
7	VGA sequance tuning	20	Add RV23	V	SIV
8	EMI solution	28 & 29	Change RC9 from 0 ohm to 33 ohm POP CA28,CA29,CA30,CA31	V	SIV
9	ESD solution		Add C1080,C1081,C1082,C1083,C1084,C1085,C1086,C1087,C1088	V	SIV
10	EMI solution for DDR DIMM	10	Reserve C1189,C1190,L51,L52	V	SIV
11	ESD request to delete XDP test point	8	Delete T198,T199,T200,T209,T210,T211,T212	V	SIV
12	EMI request	10	Change R1017 from shortPAD to 0 ohm	V	SIV
13	Delete 0 ohm due to 15'' ODD can short direct	31	Delete R130,R131,R132,R133	V	SIV
14	ME request	31	Modify H35 footprint to H_6P0,H8 & H9 to H_3P3		SIT
15	ME request	31	Change JODD2 P/N from SP01001RS00 to SP011312061		SIT
16	Protect EC	23	JLVDS1 pin 6 pull down	V	SIT
17	Vendor request	33	Modify U11.111 connect to +3VLP only,C179.1 connect to +3VLP	V	SIT
18	Vendor suggestion	20	+1.05VS to +1.05VS_VGA power switch enable pin reserve DGPU_PWR_EN path	V	SIT
19	Sourcer suggestion	31	Change Q2407,Q2408 P/N from SB000008E00 to SB000002R00	V	SIT
20	EMI request		Reserve C1001,C1002,C1005,C1006,C1007,C1016,C1091,C1092,C1101, C1102,C1103,C1104,C1105,C1106,C1107	V	SIT
21	ESD request		Add C1149,C1150,C1151,C1152,C1153,C1154	V	SIT

Compal Electronics, Inc.		
Title: HW RIR		
Size: Custom	Document Number: Intel BayTrail-M Platform	Rev: 0.2
Date: Tuesday, February 18, 2014	Sheet 36 of 47	