MS-7B05

ATX

Ver: 11 gate B

Basinfall Platform

CPU:

Skylake X/Kabylake X

System Chipset:

Kaby Lake PCH-X

Onboard Chip:

HD Audio Codec:ALC1220

LAN-Intel I219

SIO:NTC6795D

Dual Flash ROM: SPI 64 MB X2

Main Memory:

*DDRIV (UP to 2677MHz) * 8DIMM (4 Channel)*

ACPI:

MPS

PWM:

VR13 -IR35201

Expansion Slots:

*PCI Express (X16) Slot * 2*

*PCI Express (X8) Slot * 1*

*PCI Express (X4) Slot * 1*

*PCI Express (X1) Slot * 2*

Other:

*SATA3.0 *8*

*USB2.0 *6 Ports (2R/4F)*

*REAR USB30*5 + USB3.1*1 & TYPEC*1*

*FRONT USB3.0 *4+TYPEC*1*

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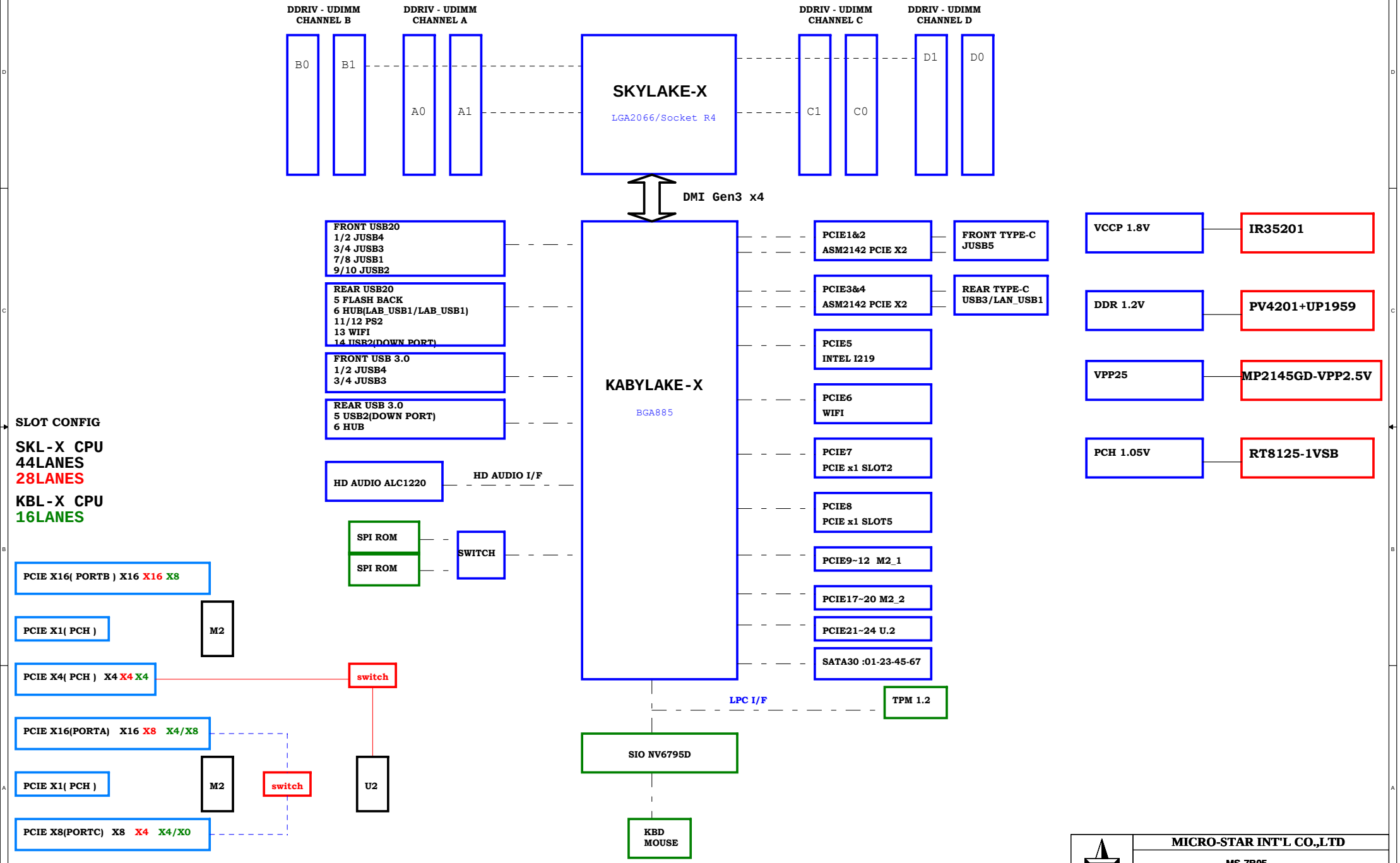
MS-7B05 Block Diagram



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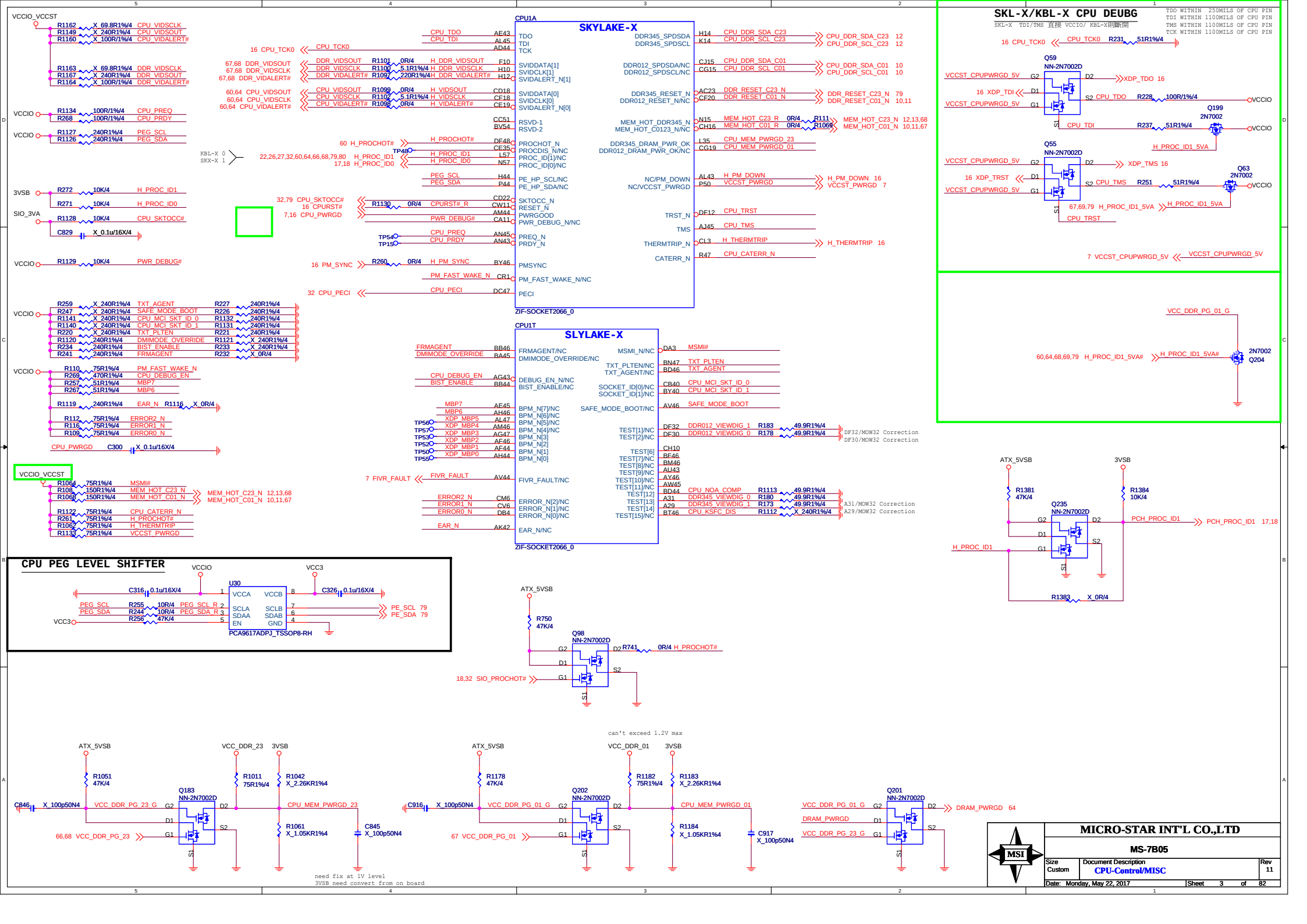
SKL-X/KBL-X CPU DEUBG
SKL-X TDI/TMS 直接 VCCIO/ KBL-X則斷開
TDO WITHIN 250MILS OF CPU PIN
TDI WITHIN 1100MILS OF CPU PIN
TMS WITHIN 1100MILS OF CPU PIN
TCK WITHIN 1100MILS OF CPU PIN
CPU1A
SKYLAKE-X
ZIF-SOCKET2066_0
CPU1T
SLYLAKE-X
ZIF-SOCKET2066_0
CPU PEG LEVEL SHIFTER
PCA9617ADPJ_TSSOP8-RH
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CPU-Control/MISC
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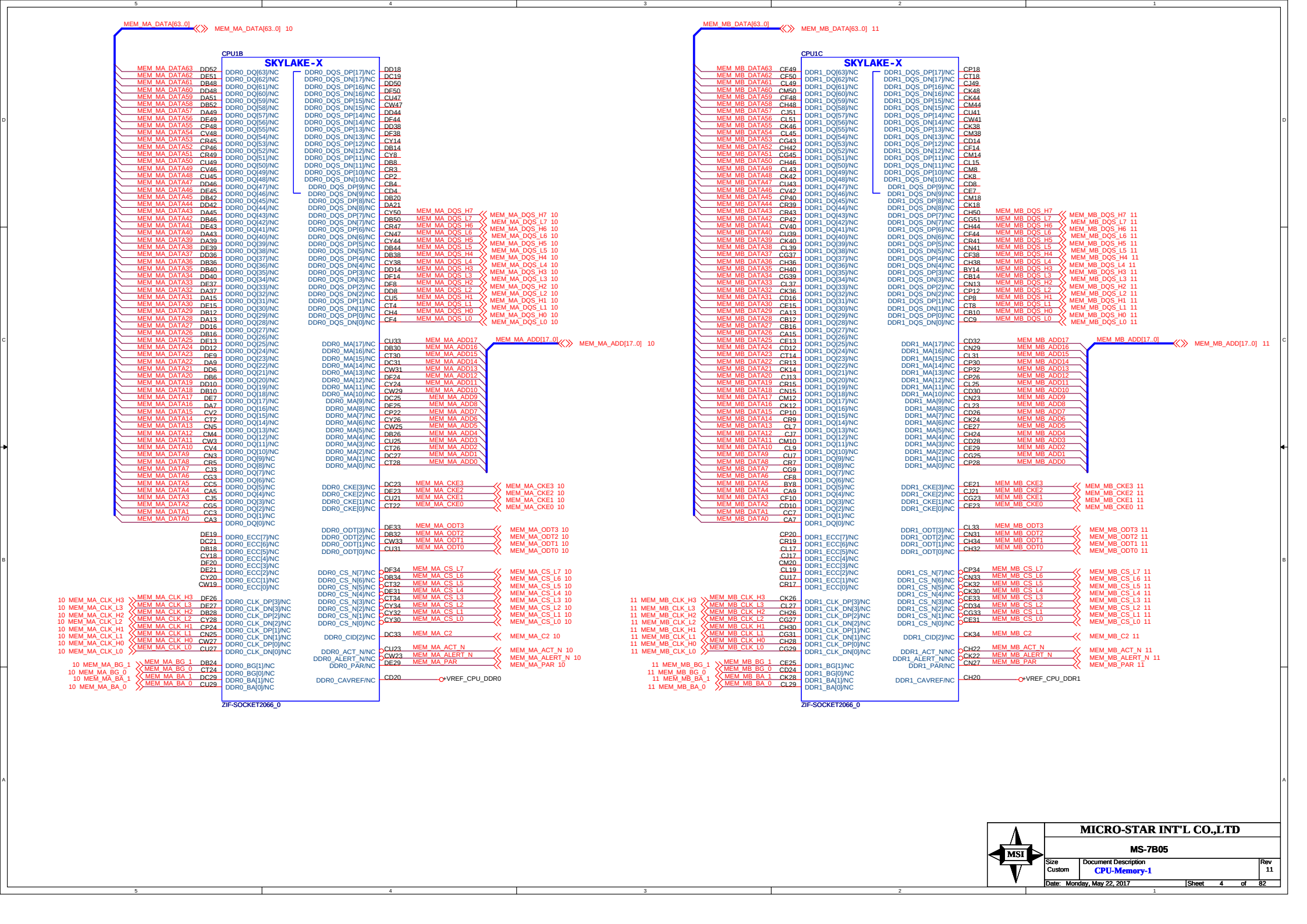
need fix at 1V level
3VSB need convert from on board


CPU1B
SKYLAKE-X
ZIF-SOCKET2066_0
CPU1C
SKYLAKE-X
ZIF-SOCKET2066_0
MEM_MA_DATA[63..0]
MEM_MB_DATA[63..0]
MEM_MA_ADD[17..0]
MEM_MB_ADD[17..0]
MEM_MA_CLK_H3
MEM_MA_CLK_L3
MEM_MA_CLK_H2
MEM_MA_CLK_L2
MEM_MA_CLK_H1
MEM_MA_CLK_L1
MEM_MA_CLK_H0
MEM_MA_CLK_L0
MEM_MB_CLK_H3
MEM_MB_CLK_L3
MEM_MB_CLK_H2
MEM_MB_CLK_L2
MEM_MB_CLK_H1
MEM_MB_CLK_L1
MEM_MB_CLK_H0
MEM_MB_CLK_L0
MEM_MA_BG_1
MEM_MA_BG_0
MEM_MA_BA_1
MEM_MA_BA_0
MEM_MB_BG_1
MEM_MB_BG_0
MEM_MB_BA_1
MEM_MB_BA_0
MEM_MA_CKE3
MEM_MA_CKE2
MEM_MA_CKE1
MEM_MA_CKE0
MEM_MB_CKE3
MEM_MB_CKE2
MEM_MB_CKE1
MEM_MB_CKE0
MEM_MA_ODT3
MEM_MA_ODT2
MEM_MA_ODT1
MEM_MA_ODT0
MEM_MB_ODT3
MEM_MB_ODT2
MEM_MB_ODT1
MEM_MB_ODT0
MEM_MA_CS_L7
MEM_MA_CS_L6
MEM_MA_CS_L5
MEM_MA_CS_L4
MEM_MA_CS_L3
MEM_MA_CS_L2
MEM_MA_CS_L1
MEM_MA_CS_L0
MEM_MB_CS_L7
MEM_MB_CS_L6
MEM_MB_CS_L5
MEM_MB_CS_L4
MEM_MB_CS_L3
MEM_MB_CS_L2
MEM_MB_CS_L1
MEM_MB_CS_L0
MEM_MA_C2
MEM_MB_C2
MEM_MA_ACT_N
MEM_MA_ALERT_N
MEM_MA_PAR
MEM_MB_ACT_N
MEM_MB_ALERT_N
MEM_MB_PAR
MEM_MA_DQS_H7
MEM_MA_DQS_L7
MEM_MA_DQS_H6
MEM_MA_DQS_L6
MEM_MA_DQS_H5
MEM_MA_DQS_L5
MEM_MA_DQS_H4
MEM_MA_DQS_L4
MEM_MA_DQS_H3
MEM_MA_DQS_L3
MEM_MA_DQS_H2
MEM_MA_DQS_L2
MEM_MA_DQS_H1
MEM_MA_DQS_L1
MEM_MA_DQS_H0
MEM_MA_DQS_L0
MEM_MB_DQS_H7
MEM_MB_DQS_L7
MEM_MB_DQS_H6
MEM_MB_DQS_L6
MEM_MB_DQS_H5
MEM_MB_DQS_L5
MEM_MB_DQS_H4
MEM_MB_DQS_L4
MEM_MB_DQS_H3
MEM_MB_DQS_L3
MEM_MB_DQS_H2
MEM_MB_DQS_L2
MEM_MB_DQS_H1
MEM_MB_DQS_L1
MEM_MB_DQS_H0
MEM_MB_DQS_L0
+VREF_CPU_DDR0
+VREF_CPU_DDR1
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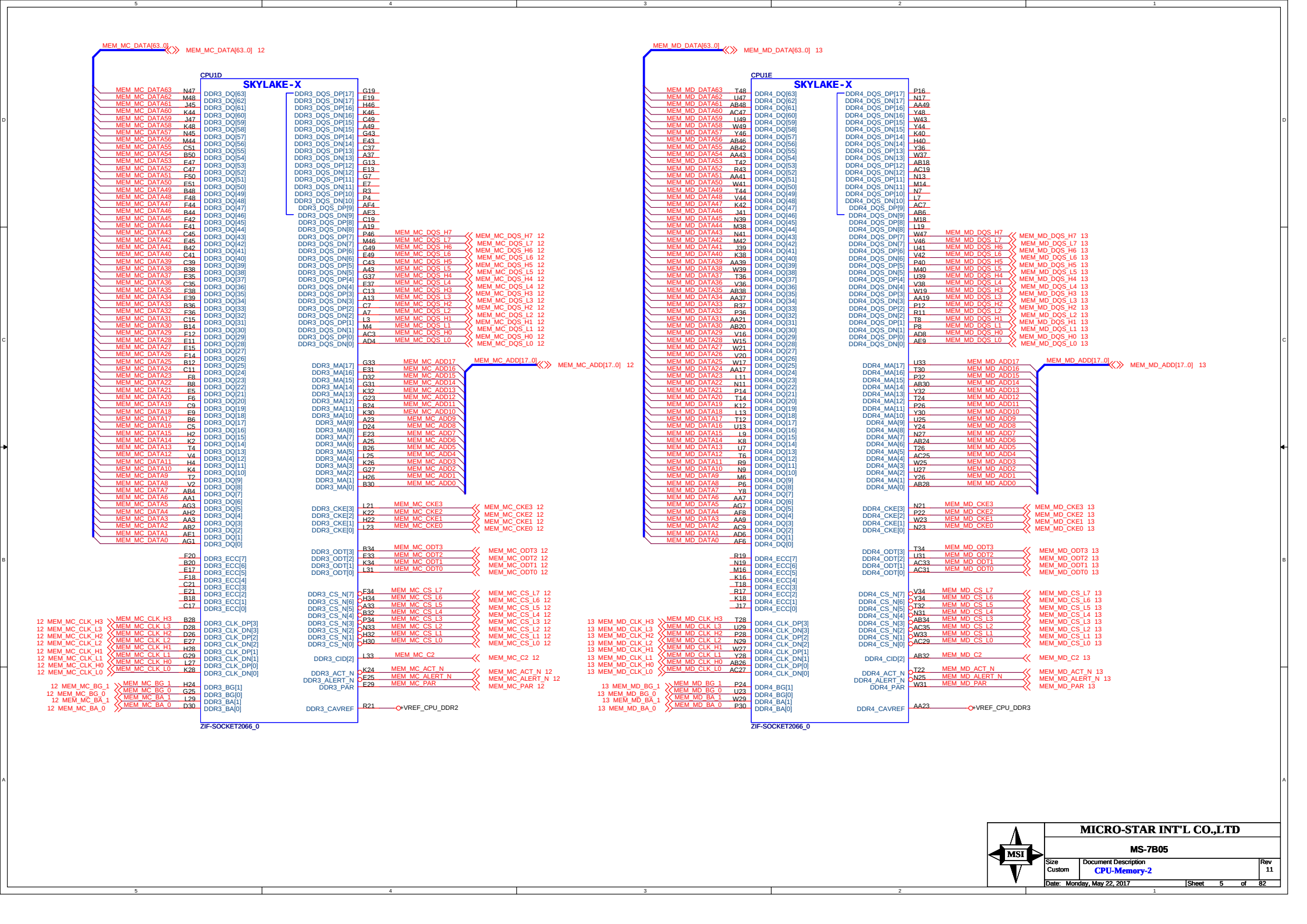

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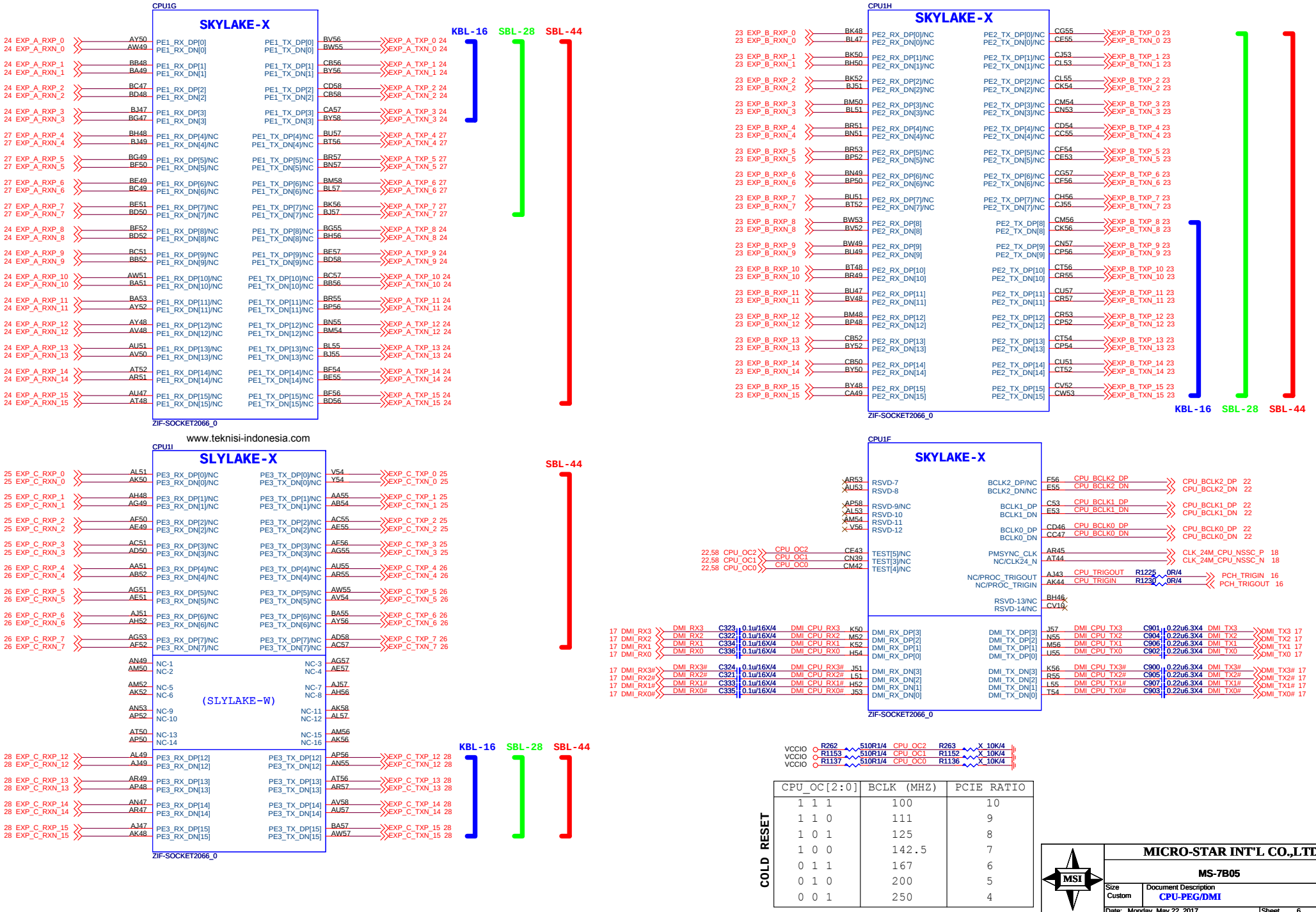

COLD RESET	CPU_OC[2:0]	BCLK (MHZ)	PCIE RATIO
	1 1 1	100	10
	1 1 0	111	9
	1 0 1	125	8
	1 0 0	142.5	7
	0 1 1	167	6
	0 1 0	200	5
	0 0 1	250	4

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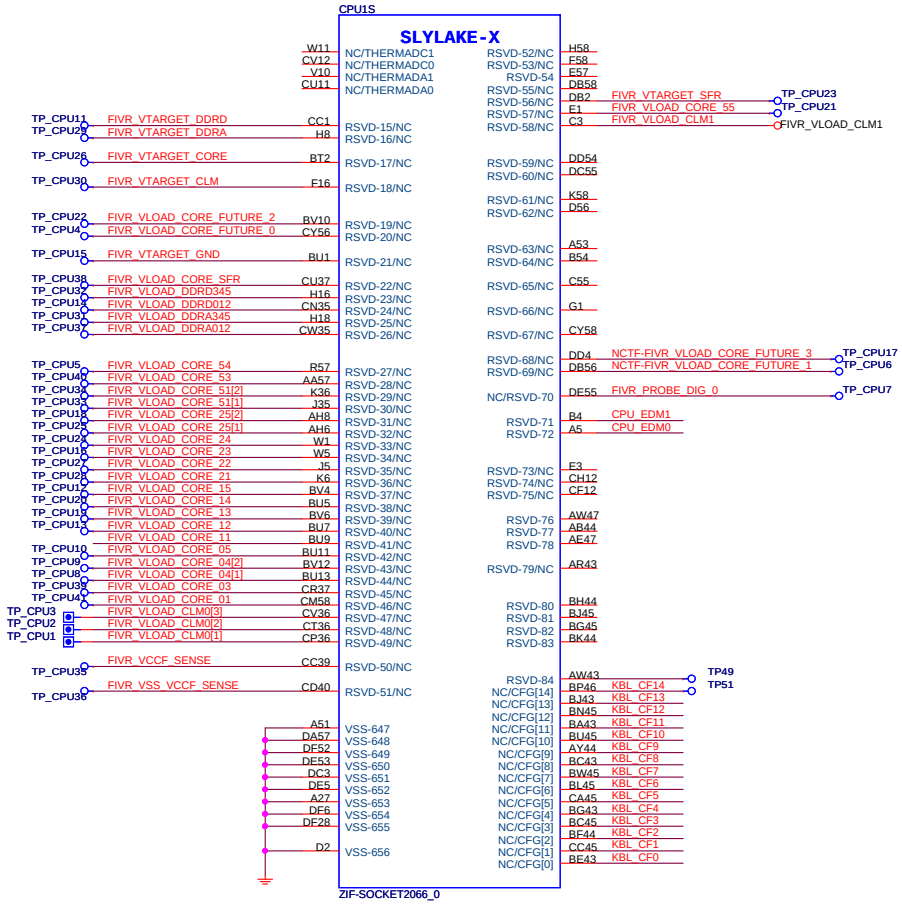
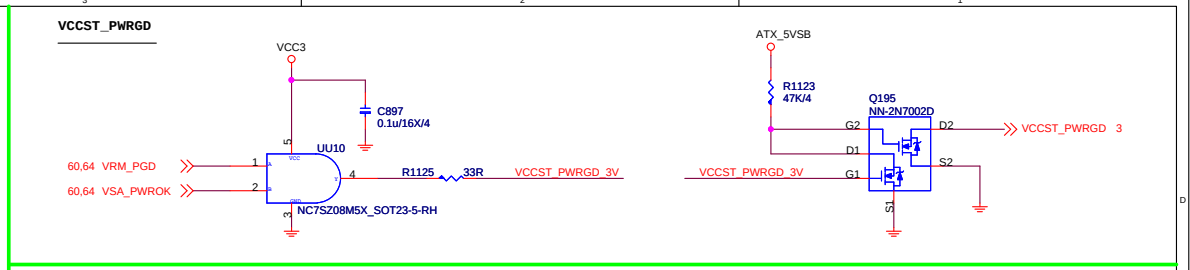
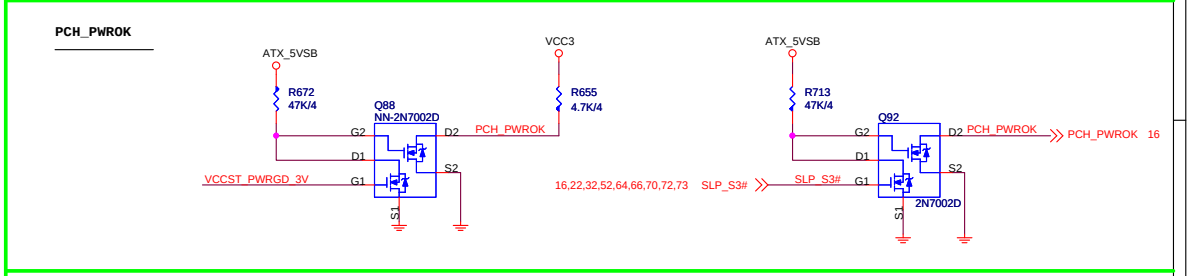
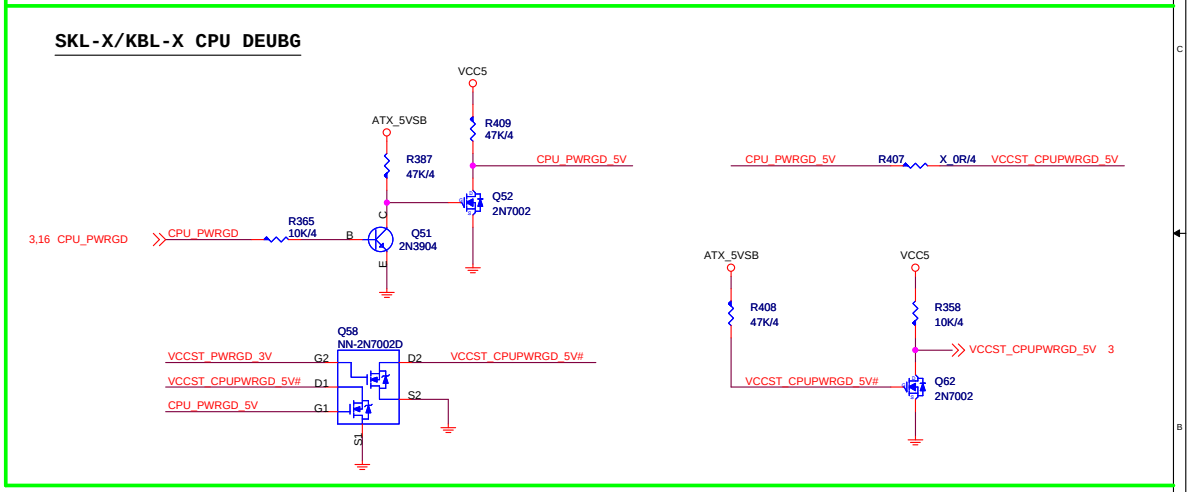
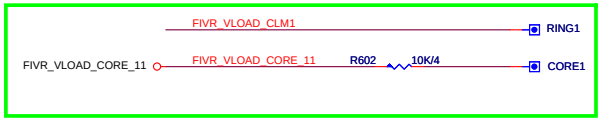
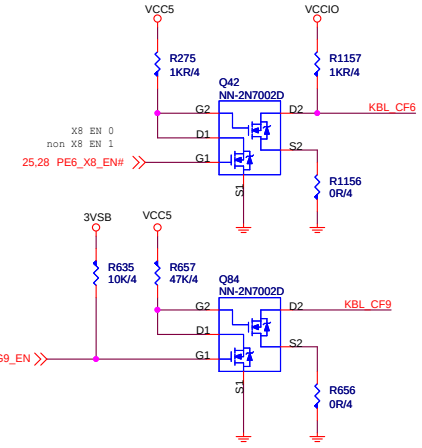












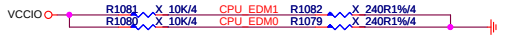
PCIE Strap

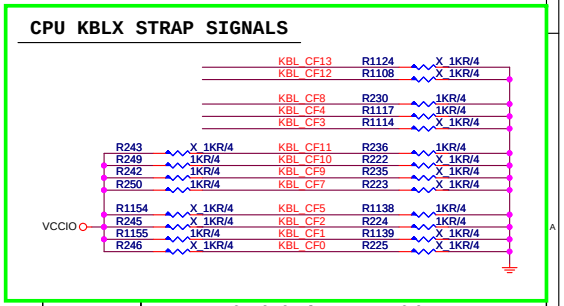
CFG6	CFG5	PCIE
0	0	1x8,2x4
0	1	RSVD
1	0	2x8
1	1	1x16

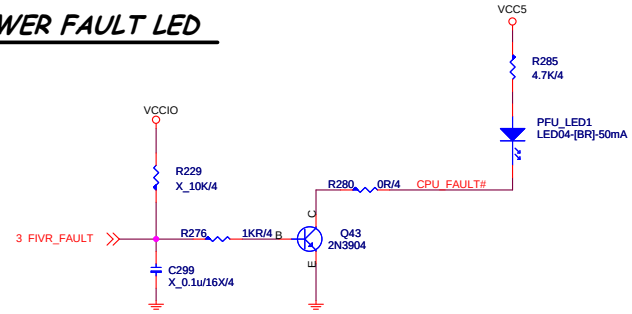
CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEGGOCFGSEL[0]
6	DISABLE	ENABLE	PEGGOCFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		







MSI	MICRO-STAR INT'L CO.,LTD
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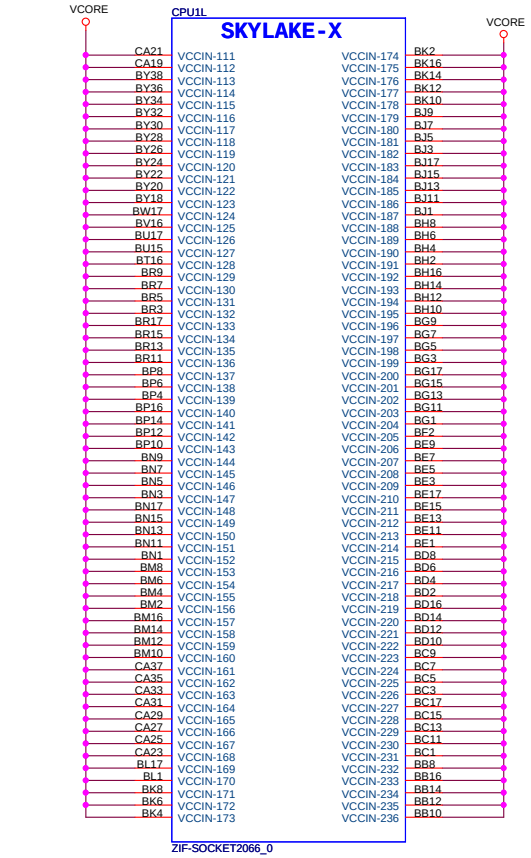
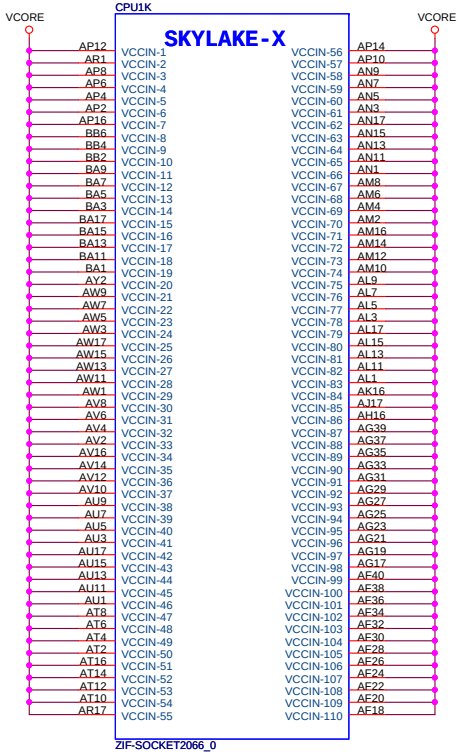
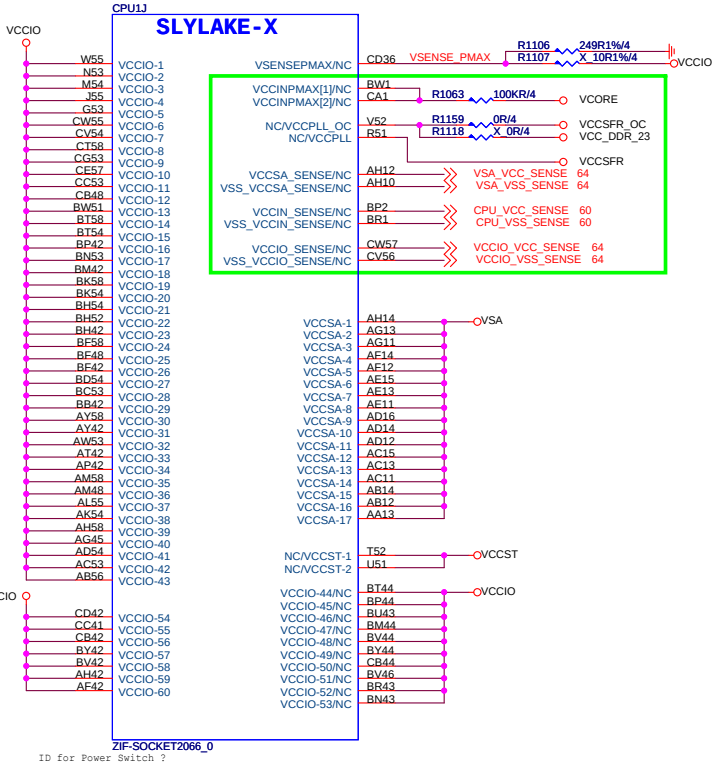
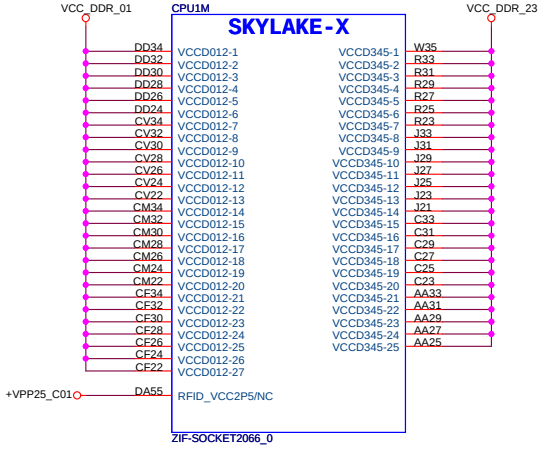
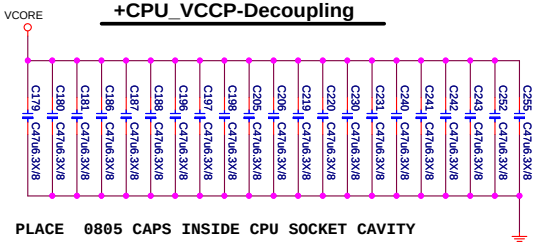




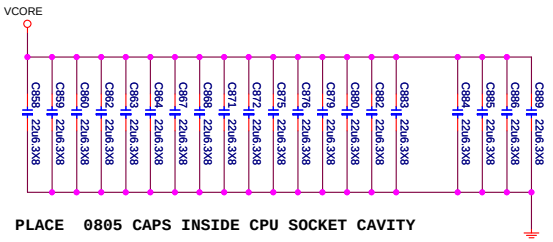




+CPU_VCCP-Decoupling

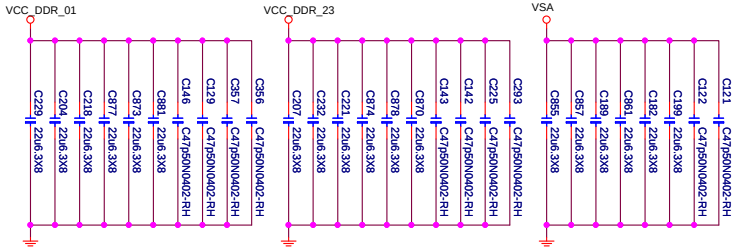


PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

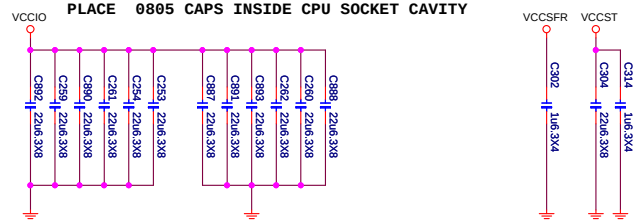


PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

+CPU_DDR-Decoupling



PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY



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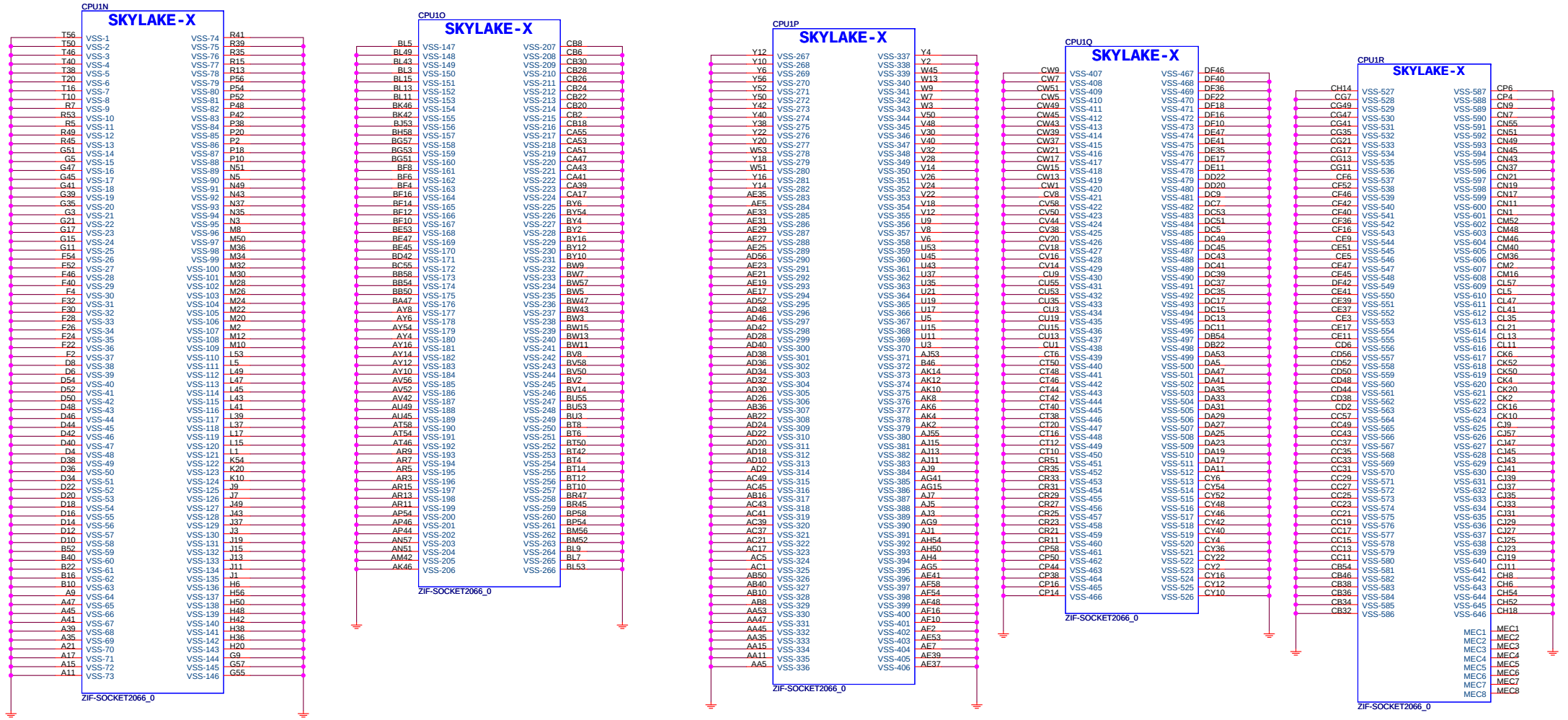

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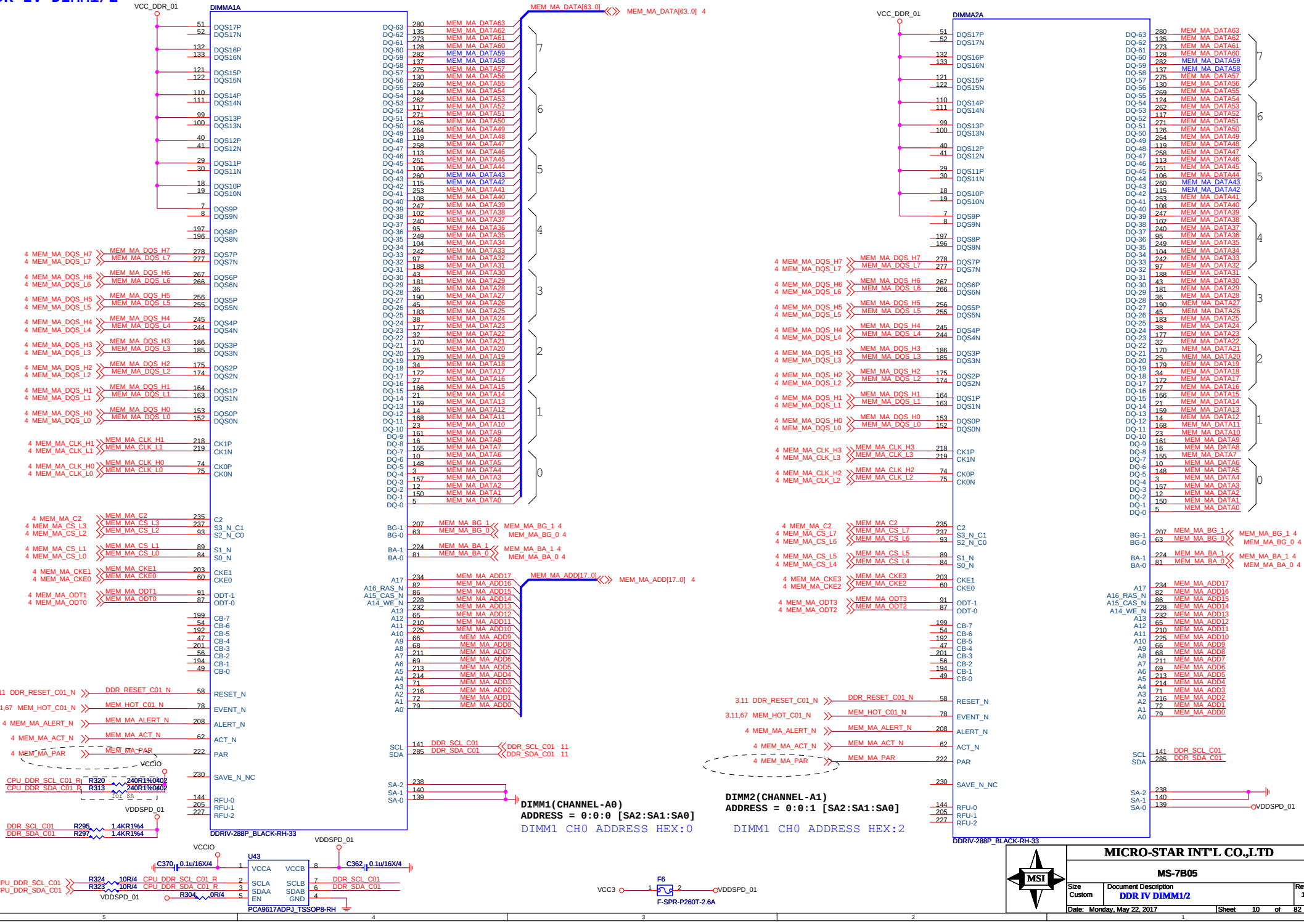
DDR IV DIMM1/2



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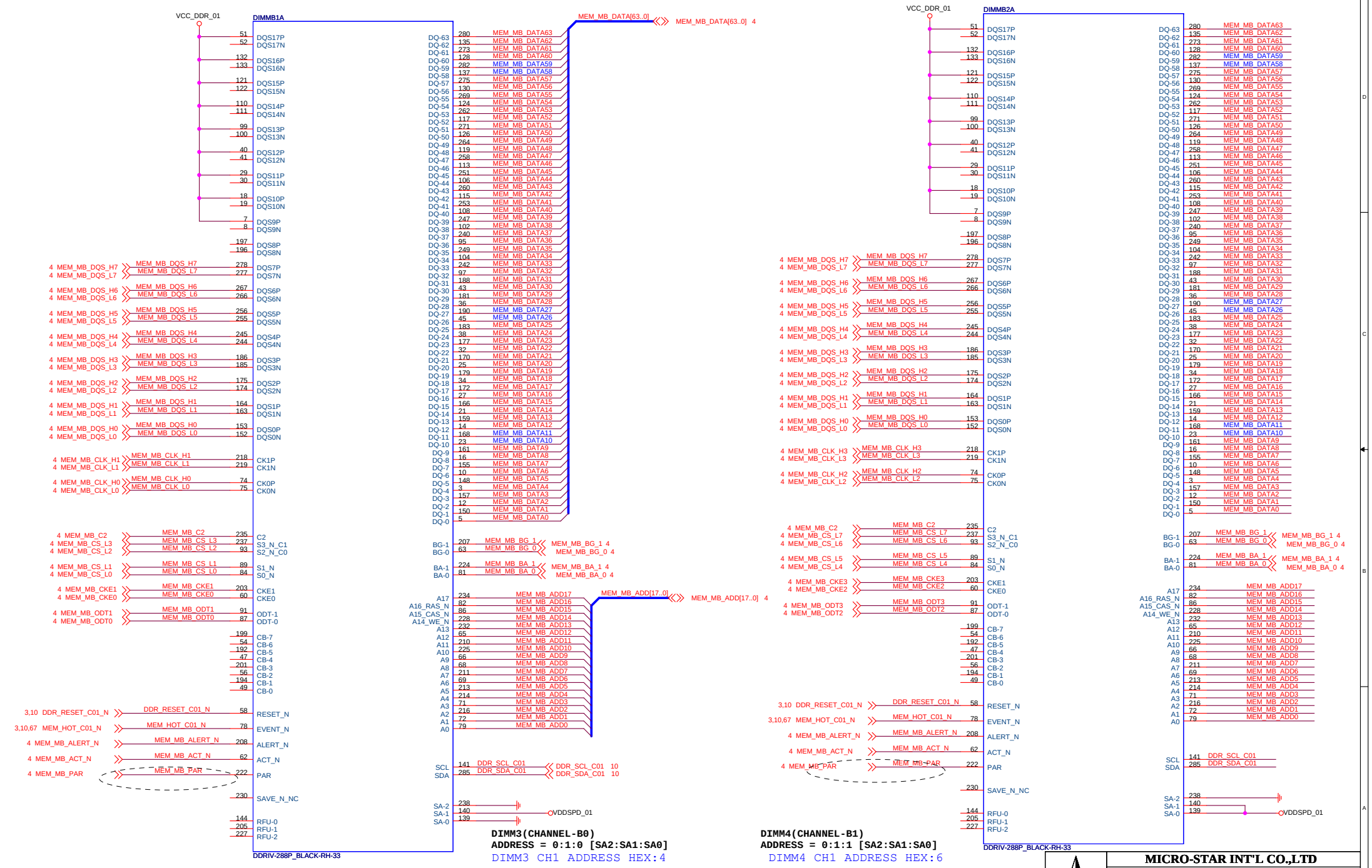
DDR IV DIMM3/4



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DDR IV DIMM5/6

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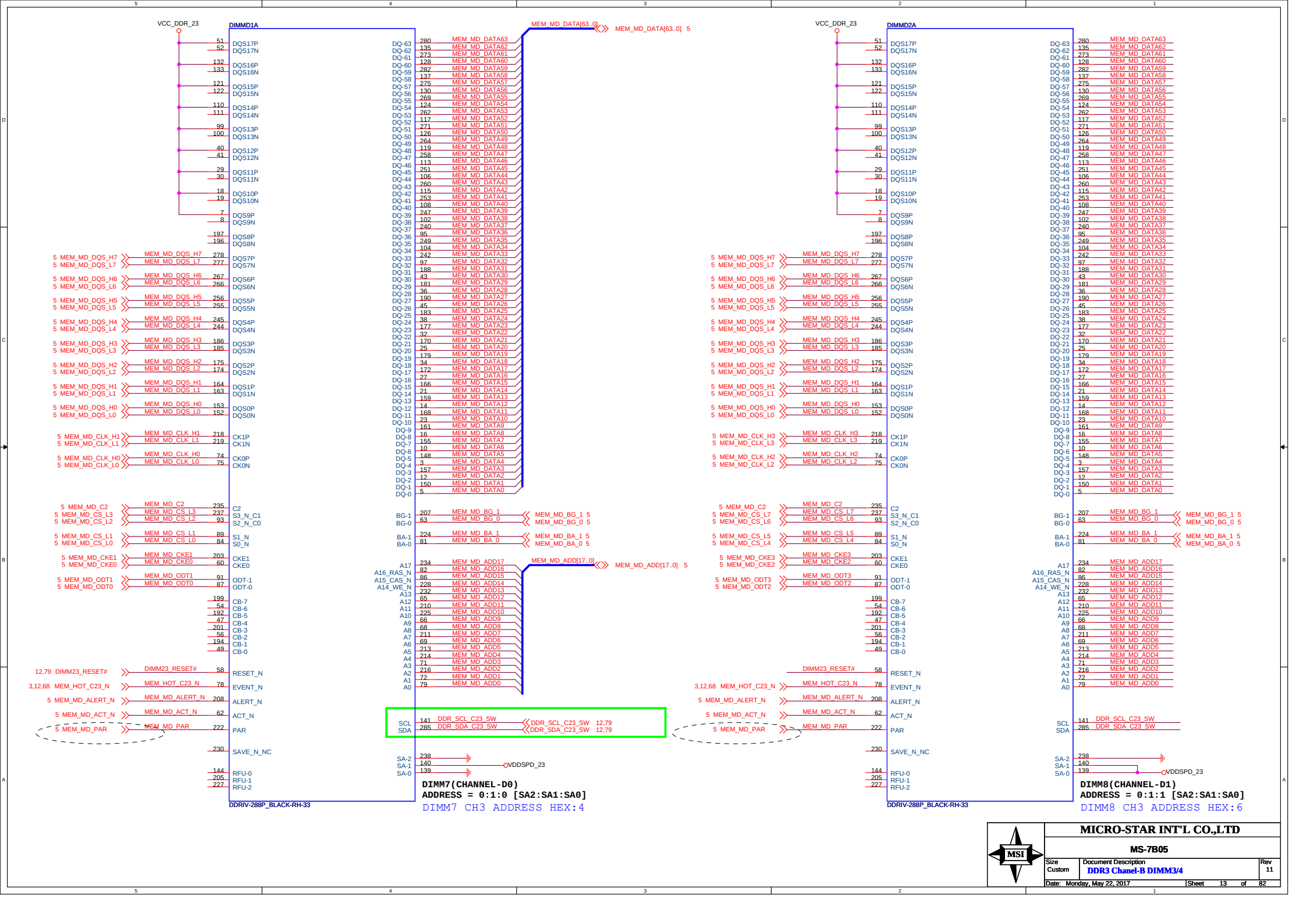
VCC_DDR_23
DIMMD1A
MEM_MD_DATA[63..0]
MEM_MD_DATA[63..0] 5
MEM_MD_ADD[17..0]
MEM_MD_ADD[17..0] 5
DDRIV-288P_BLACK-RH-33
DIMM7(CHANNEL-D0)
ADDRESS = 0:1:0 [SA2:SA1:SA0]
DIMM7 CH3 ADDRESS HEX:4
VCC_DDR_23
DIMMD2A
DDRIV-288P_BLACK-RH-33
DIMM8(CHANNEL-D1)
ADDRESS = 0:1:1 [SA2:SA1:SA0]
DIMM8 CH3 ADDRESS HEX:6
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Custom
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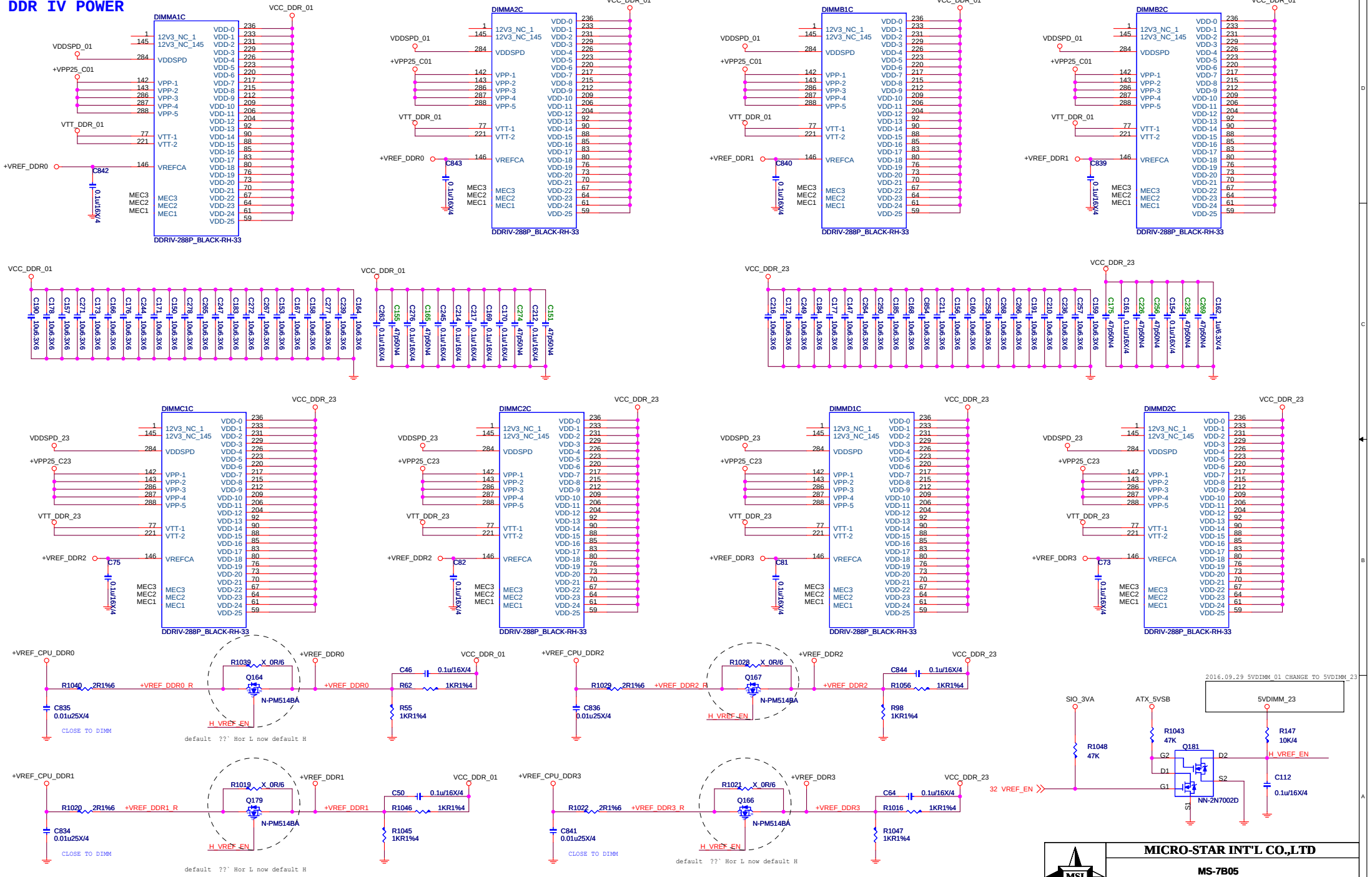
DDR IV POWER



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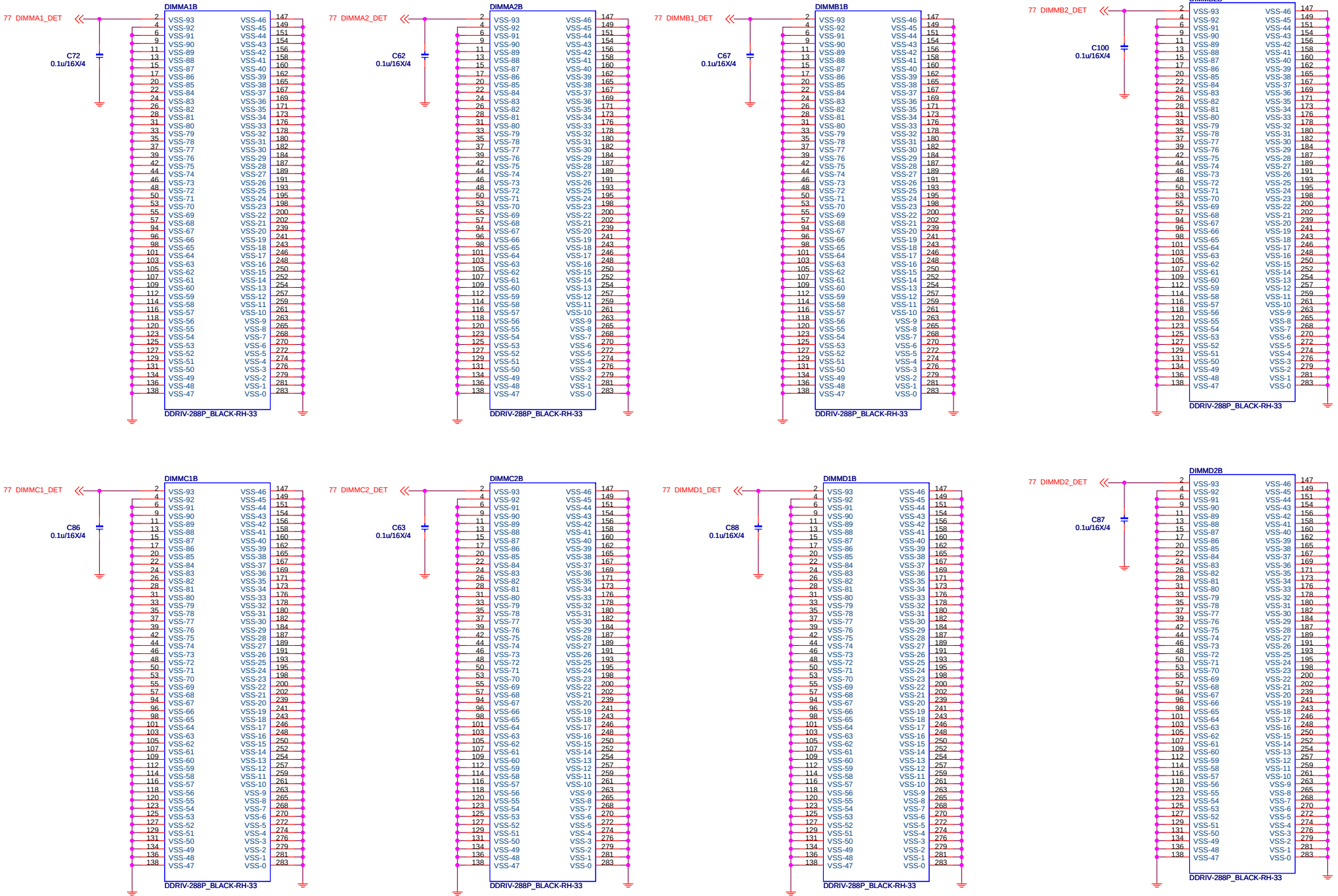
DDR IV GND



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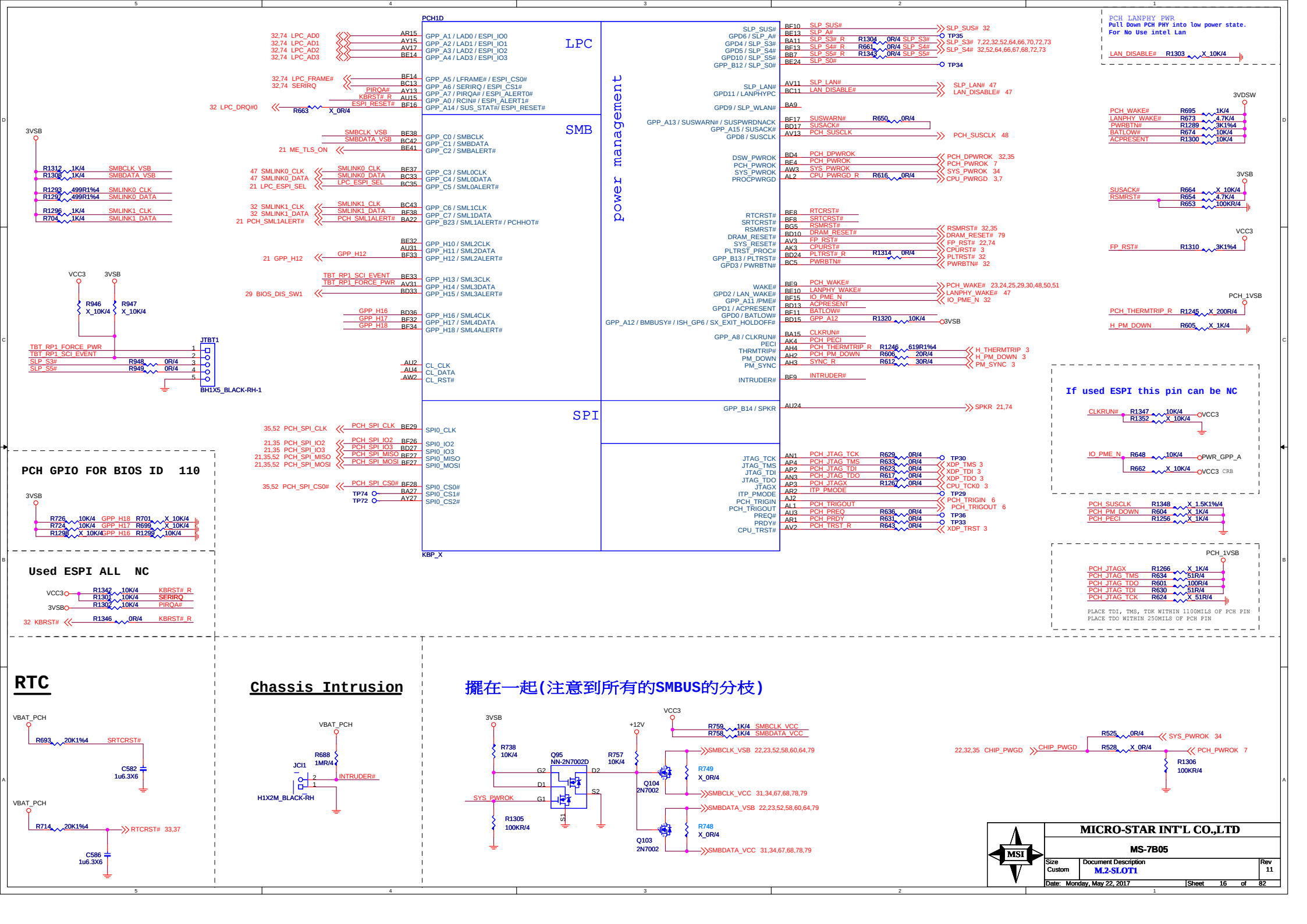
PCH1D
LPC
SMB
SPI
power management
KBP_X
GPP_A1 / LAD0 / ESPI_IO0
GPP_A2 / LAD1 / ESPI_IO1
GPP_A3 / LAD2 / ESPI_IO2
GPP_A4 / LAD3 / ESPI_IO3
GPP_A5 / LFRAME# / ESPI_CS0#
GPP_A6 / SERIRQ / ESPI_CS1#
GPP_A7 / PIRQA# / ESPI_ALERT0#
GPP_A0 / RCIN# / ESPI_ALERT1#
GPP_A14 / SUS_STAT# / ESPI_RESET#
GPP_C0 / SMBCLK
GPP_C1 / SMBDATA
GPP_C2 / SMBALERT#
GPP_C3 / SML0CLK
GPP_C4 / SML0DATA
GPP_C5 / SML0ALERT#
GPP_C6 / SML1CLK
GPP_C7 / SML1DATA
GPP_B23 / SML1ALERT# / PCHHOT#
GPP_H10 / SML2CLK
GPP_H11 / SML2DATA
GPP_H12 / SML2ALERT#
GPP_H13 / SML3CLK
GPP_H14 / SML3DATA
GPP_H15 / SML3ALERT#
GPP_H16 / SML4CLK
GPP_H17 / SML4DATA
GPP_H18 / SML4ALERT#
CL_CLK
CL_DATA
CL_RST#
SPI0_CLK
SPI0_IO2
SPI0_IO3
SPI0_MISO
SPI0_MOSI
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#
GPP_B14 / SPKR
JTBT1
BH1X5_BLACK-RH-1
PCH GPIO FOR BIOS ID 110
Used ESPI ALL NC
RTC
Chassis Intrusion
H1X2M_BLACK-RH
擺在一起(注意到所有的SMBUS的分枝)
Q95 NN-2N7002D
Q104 2N7002
Q103 2N7002
If used ESPI this pin can be NC
PCH_LANPHY_PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan
PLACE TDI, TMS, TDK WITHIN 1100MILS OF PCH PIN
PLACE TDO WITHIN 250MILS OF PCH PIN
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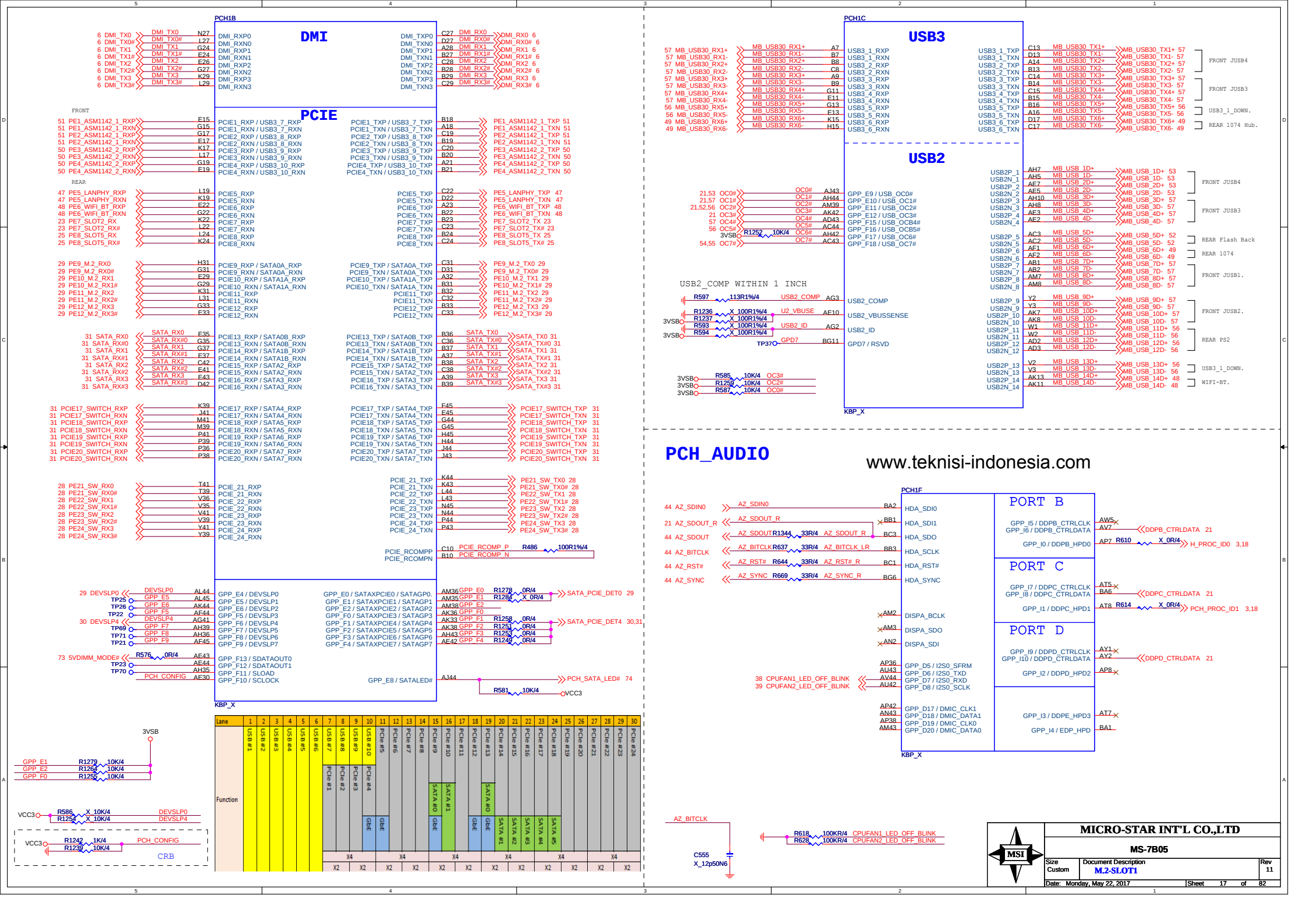
PCH1B
DMI
PCIE
KBP_X
PCH1C
USB3
USB2
KBP_X
PCH_AUDIO
www.teknisi-indonesia.com
PCH1F
PORT B
PORT C
PORT D
KBP_X
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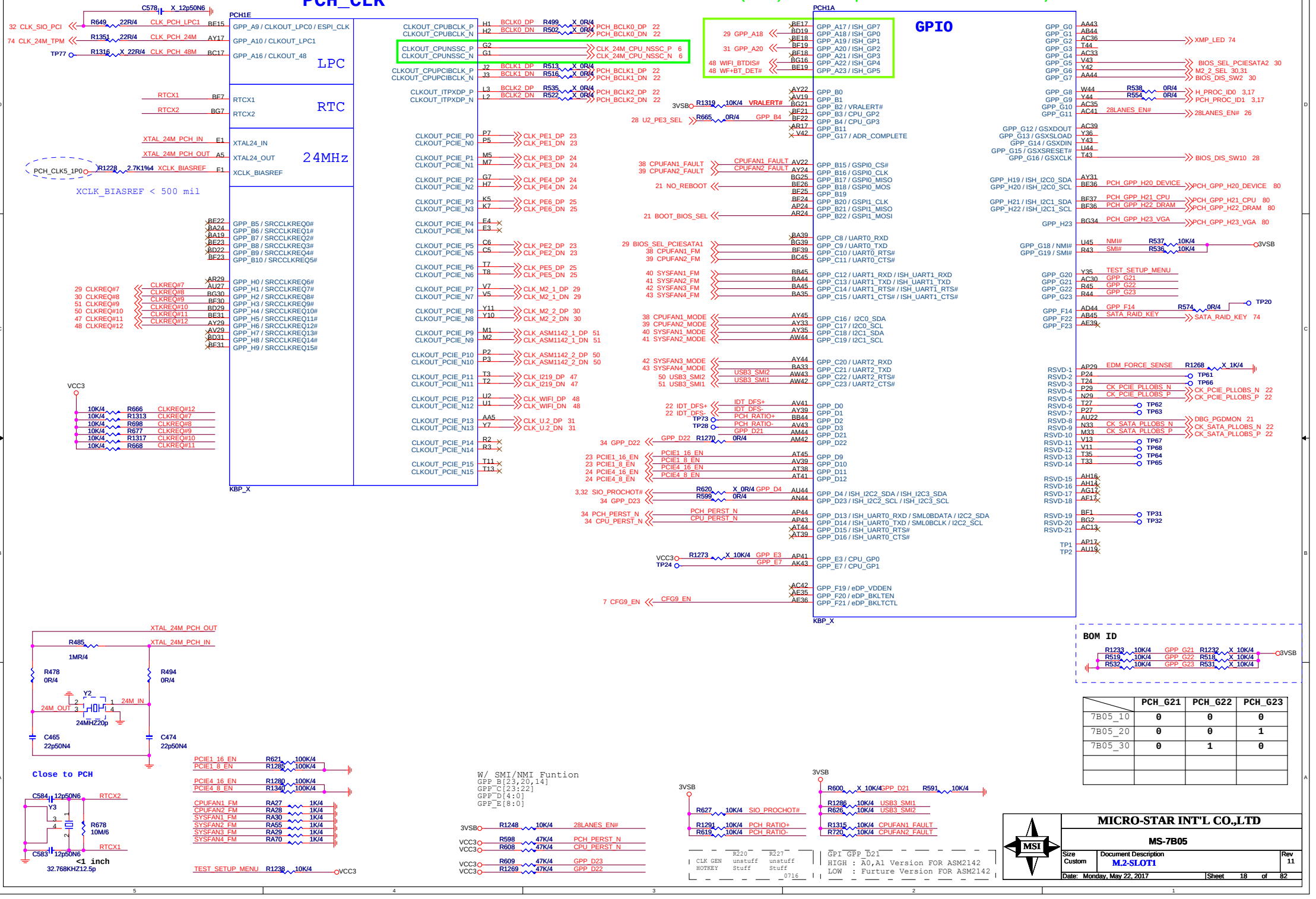
PCH_CLK

Used ESPI(GPPA) GPIO Group A will be come 1.8V leve)



	PCH_G21	PCH_G22	PCH_G23
7B05_10	0	0	0
7B05_20	0	0	1
7B05_30	0	1	0

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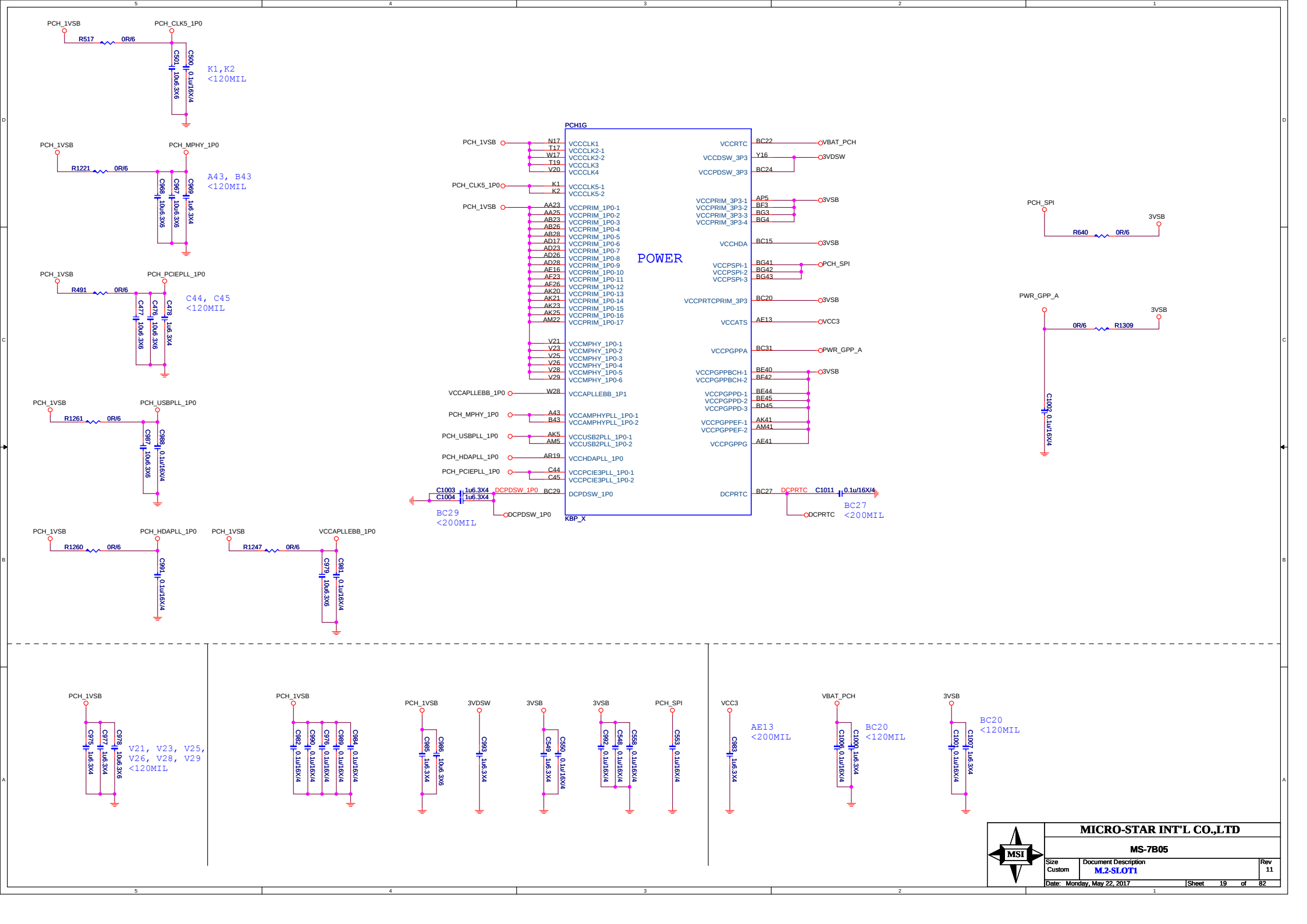
PCH_1VSB
R517 0R/6
PCH_CLK5_1P0
C501 10u6.3X6
C500 0.1u/16X/4
K1,K2
<120MIL
PCH_1VSB
R1221 0R/6
PCH_MPHY_1P0
C988 10u6.3X6
C987 10u6.3X6
C989 1u6.3X4
A43, B43
<120MIL
PCH_1VSB
R491 0R/6
PCH_PCIEPLL_1P0
C477 10u6.3X6
C476 10u6.3X6
C478 1u6.3X4
C44, C45
<120MIL
PCH_1VSB
R1261 0R/6
PCH_USBPLL_1P0
C987 10u6.3X6
C988 0.1u/16X/4
PCH_1VSB
R1260 0R/6
PCH_HDAPLL_1P0
C991 0.1u/16X/4
PCH_1VSB
R1247 0R/6
VCCAPLLEBB_1P0
C979 10u6.3X6
C981 0.1u/16X/4
PCH1G
PCH_1VSB
N17 VCCCLK1
T17 VCCCLK2-1
W17 VCCCLK2-2
T19 VCCCLK3
V20 VCCCLK4
PCH_CLK5_1P0
K1 VCCCLK5-1
K2 VCCCLK5-2
PCH_1VSB
AA23 VCCPRIM_1P0-1
AA25 VCCPRIM_1P0-2
AB23 VCCPRIM_1P0-3
AB26 VCCPRIM_1P0-4
AB28 VCCPRIM_1P0-5
AD17 VCCPRIM_1P0-6
AD23 VCCPRIM_1P0-7
AD26 VCCPRIM_1P0-8
AD28 VCCPRIM_1P0-9
AE16 VCCPRIM_1P0-10
AE23 VCCPRIM_1P0-11
AE26 VCCPRIM_1P0-12
AK20 VCCPRIM_1P0-13
AK21 VCCPRIM_1P0-14
AK23 VCCPRIM_1P0-15
AK25 VCCPRIM_1P0-16
AM22 VCCPRIM_1P0-17
V21 VCCMPHY_1P0-1
V23 VCCMPHY_1P0-2
V25 VCCMPHY_1P0-3
V26 VCCMPHY_1P0-4
V28 VCCMPHY_1P0-5
V29 VCCMPHY_1P0-6
VCCAPLLEBB_1P0
W28 VCCAPLLEBB_1P1
PCH_MPHY_1P0
A43 VCCAMPHYPLL_1P0-1
B43 VCCAMPHYPLL_1P0-2
PCH_USBPLL_1P0
AK5 VCCUSB2PLL_1P0-1
AM5 VCCUSB2PLL_1P0-2
PCH_HDAPLL_1P0
AR19 VCCHDAPLL_1P0
PCH_PCIEPLL_1P0
C44 VCCPCIE3PLL_1P0-1
C45 VCCPCIE3PLL_1P0-2
C1003 1u6.3X4
C1004 1u6.3X4
DCPDSW_1P0
BC29 DCPDSW_1P0
POWER
VCCRTC BC22 VBAT_PCH
VCCDSW_3P3 Y16 3VDSW
VCCPDSW_3P3 BC24
VCCPRIM_3P3-1 AP5
VCCPRIM_3P3-2 BF3
VCCPRIM_3P3-3 BG3
VCCPRIM_3P3-4 BG4 3VSB
VCCHDA BC15 3VSB
VCCPSPI-1 BG41
VCCPSPI-2 BG42
VCCPSPI-3 BG43 PCH_SPI
VCCPRTCPRIM_3P3 BC20 3VSB
VCCATS AE13 VCC3
VCCPGPPA BC31 PWR_GPP_A
VCCPGPPBCH-1 BE40
VCCPGPPBCH-2 BE42 3VSB
VCCPGPPD-1 BE44
VCCPGPPD-2 BE45
VCCPGPPD-3 BD45
VCCPGPPEF-1 AK41
VCCPGPPEF-2 AM41
VCCPGPPG AE41
DCPRTC BC27 DCPRTC C1011 0.1u/16X/4
DCPRTC
KBP_X
BC29
<200MIL
BC27
<200MIL
PCH_SPI
R640 0R/6 3VSB
PWR_GPP_A
0R/6 R1309 3VSB
C1002 0.1u/16X/4
PCH_1VSB
C975 1u6.3X4
C977 1u6.3X4
C978 10u6.3X6
V21, V23, V25,
V26, V28, V29
<120MIL
PCH_1VSB
C982 0.1u/16X/4
C990 0.1u/16X/4
C976 0.1u/16X/4
C980 0.1u/16X/4
C984 0.1u/16X/4
PCH_1VSB
C985 1u6.3X4
C986 10u6.3X6
3VDSW
C993 1u6.3X4
3VSB
C549 1u6.3X4
C550 0.1u/16X/4
3VSB
C992 0.1u/16X/4
C548 0.1u/16X/4
C558 0.1u/16X/4
PCH_SPI
C553 0.1u/16X/4
VCC3
C983 1u6.3X4
AE13
<200MIL
VBAT_PCH
C1006 0.1u/16X/4
C1000 1u6.3X4
BC20
<120MIL
3VSB
C1001 0.1u/16X/4
C1007 1u6.3X4
BC20
<120MIL
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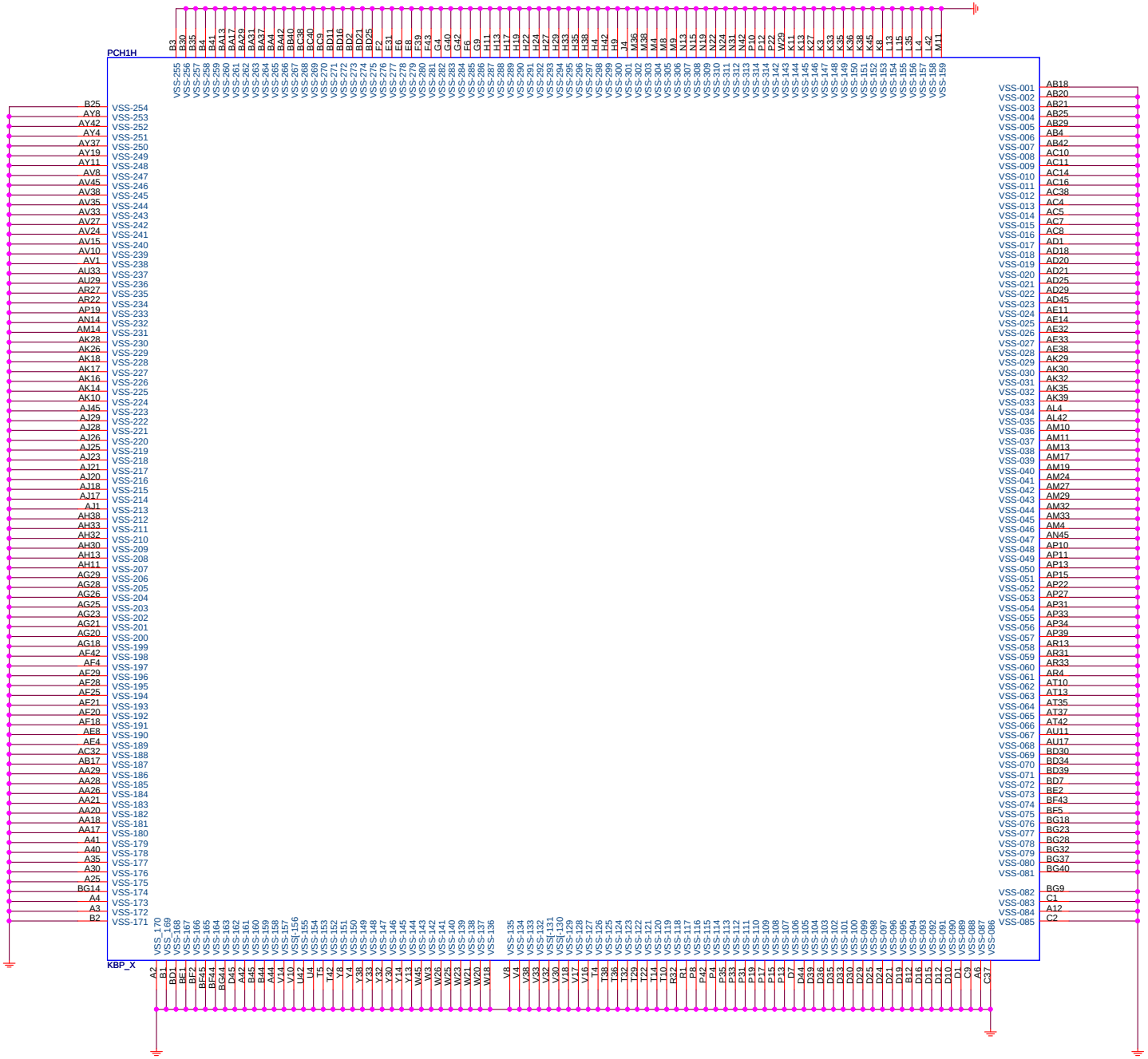

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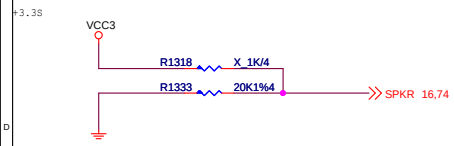
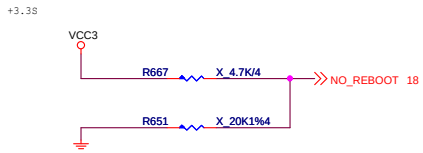
TOP SWAP OVERRIDE STRAP



HIGH: TOP_SWAP ENABLED
LOW : TOP_SWAP DISABLED

PCH HAS INTERNAL WEAK PD

No Reboot OPTION



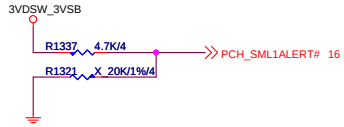
0 : NO-REBOOT (Default)
1 : REBOOT

PCH HAS INTERNAL WEAK PD

AMT and SBA with confidentiality

0 : DISABLE
1 : ENABLE (Default)

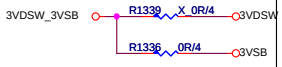
DCI ENABLE



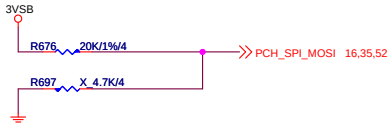
0 : DCI DISABLE
1 : DCI ENABLE (Default)

PCH HAS INTERNAL WEAK PD

CRB

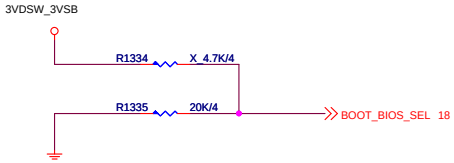


Booot-HALT SEL STRAP



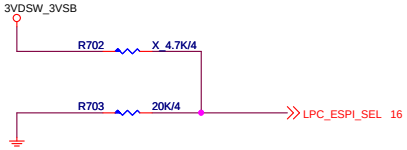
PCH HAS INTERNAL WEAK PU

Boot BIOS



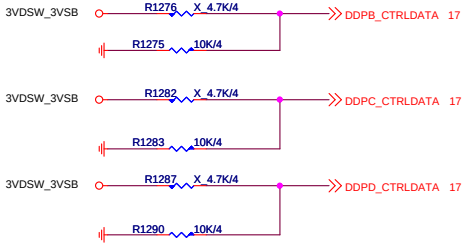
0 : SPI
1 : LPC

LPC eSPI Mode



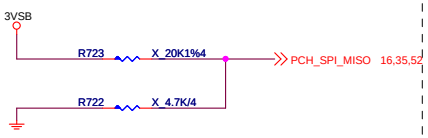
0 : LPC
1 : eSPI

DISPLAY PORT



0 : DISPLAY NOT DETECTED (Default)
1 : DISPLAY DETECTED

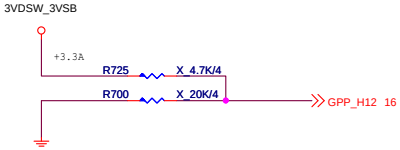
JTAG ODT SEL



HIGH: JTAG ODT ENABLED
LOW : JTAG ODT DISABLED

PCH HAS INTERNAL WEAK PU

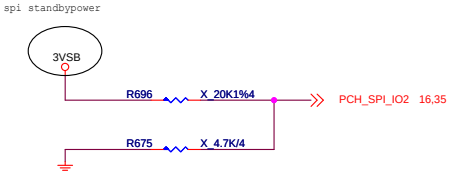
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

PCH HAS INTERNAL WEAK PD

CONSENT



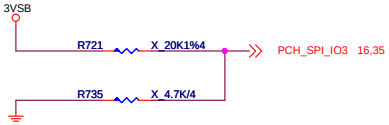
0 : CONSENT STRAP ENABLE
1 : CONSENT STRAP ENABLE

PCH HAS INTERNAL WEAK PU

DFX TEST MODE

UNSRTUFF: NORMAL
STUFF: TEST MODE

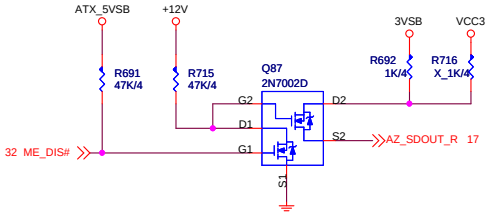
PERSONALITY



HIGH: PERSONALITY ENABLED
LOW : PERSONALITY DISABLED

PCH HAS INTERNAL WEAK PU

HDA_SDO

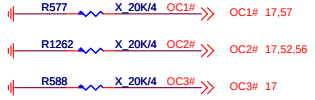


0 : SECURITY MEASURES OVERRIDEN
1 : SECURITY PER FLASH DESCRIPTOR

RING OSCILLATOR BYPASS (DFX)

0 : Ring Oscillator bypass
1 : Normal Mode

XTAL INPUT FREQUENCY [HVM MODE]



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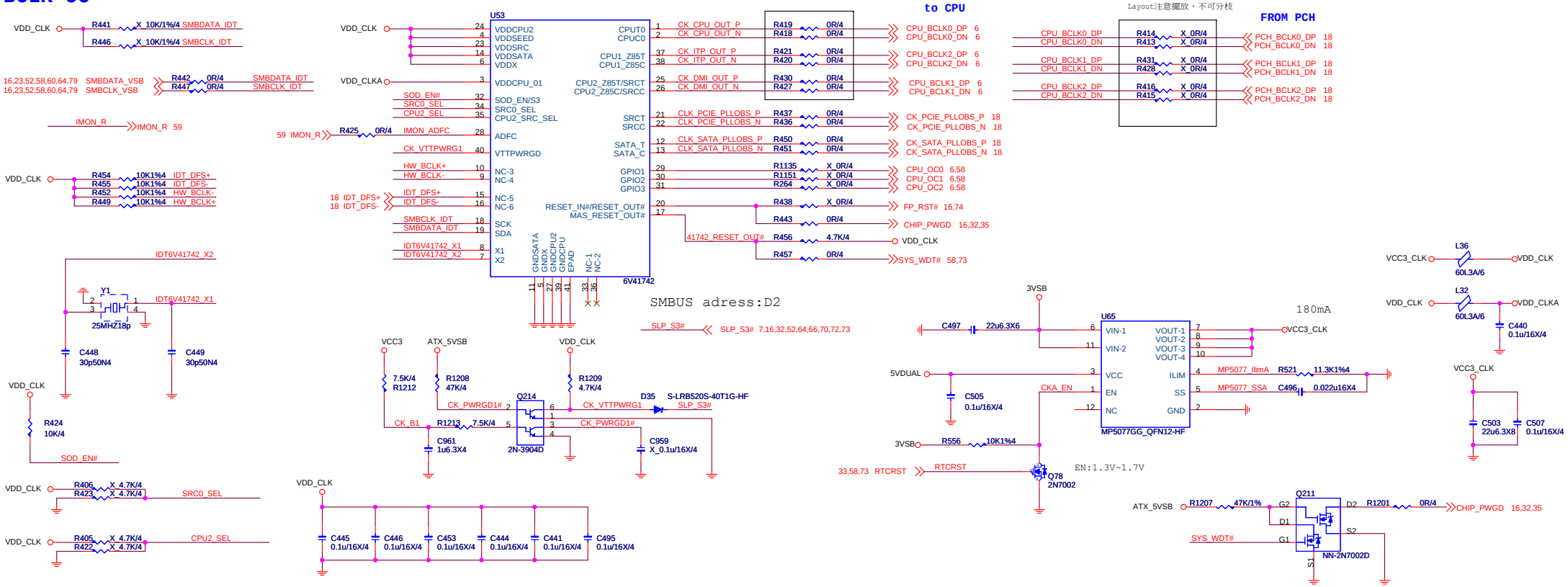
BCLK OC



SRC0_SEL	Description	CPU	H_PROC_ID1
0	Source from CPUPLL	SKX	1
1	Source from PCIEPLL	KBX	0

CPU2_SRC_SEL	Description	CPU	H_PROC_ID1
0	Source from CPUPLL	SKX	1
1	Source from PCIEPLL	KBX	0

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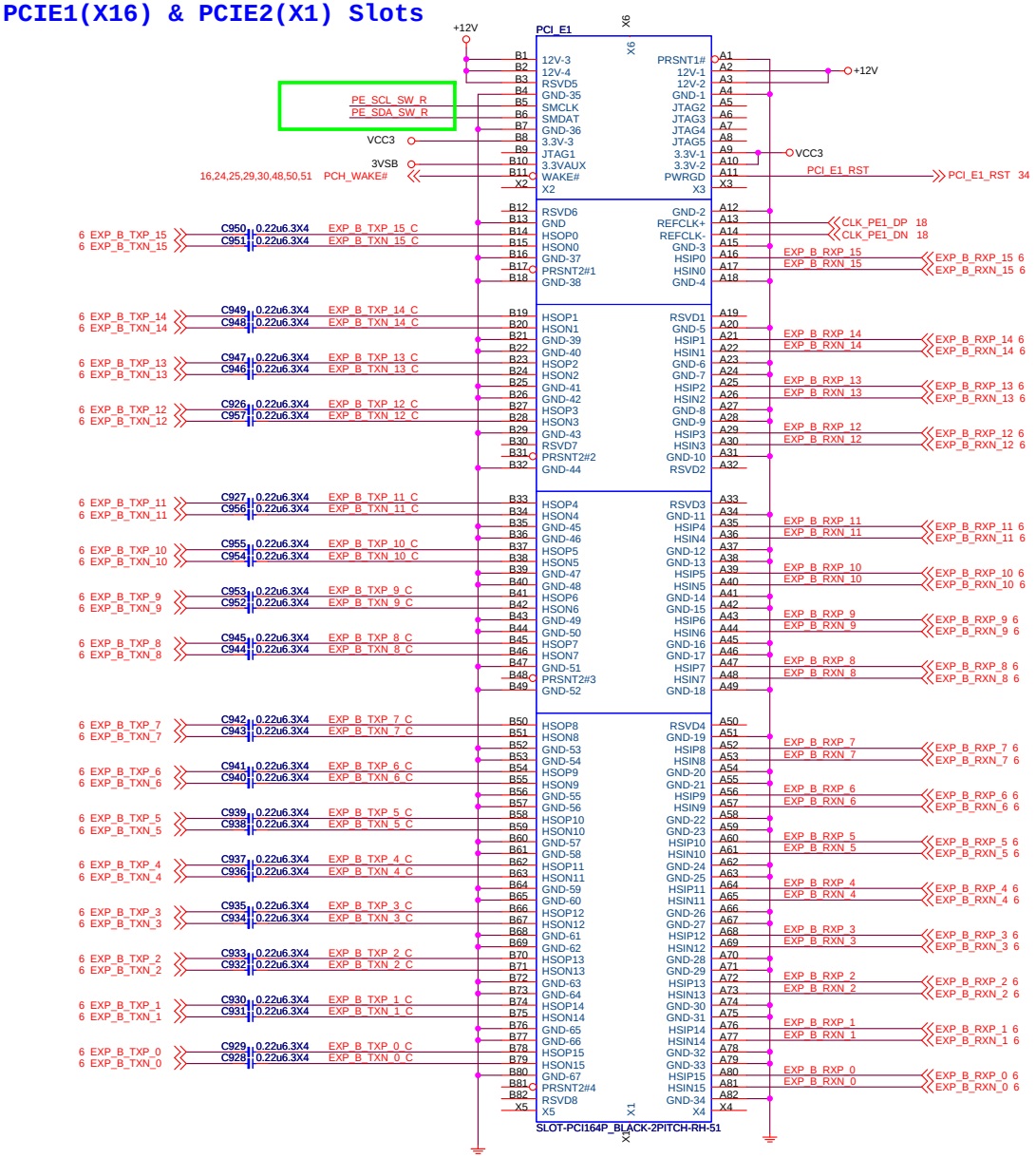
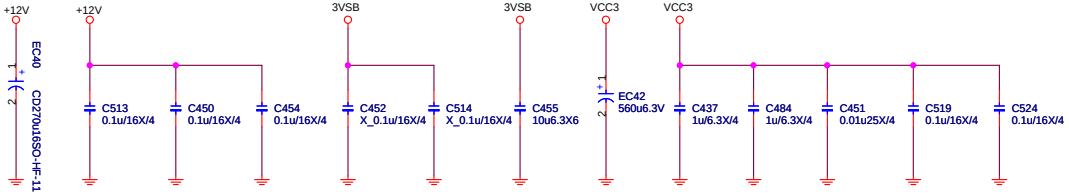
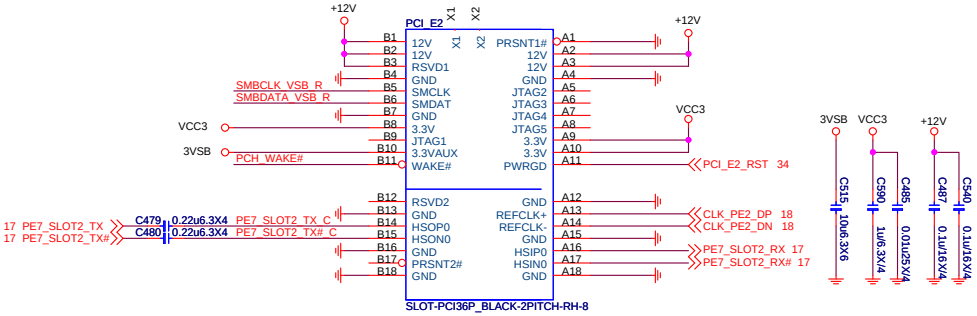
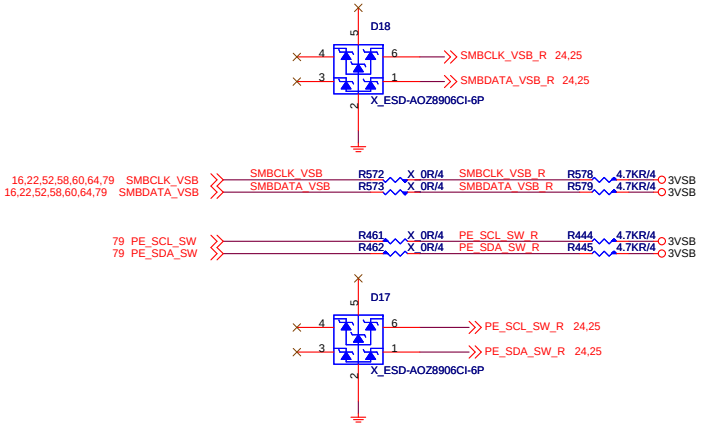
PCIE1(X16) & PCIE2(X1) Slots



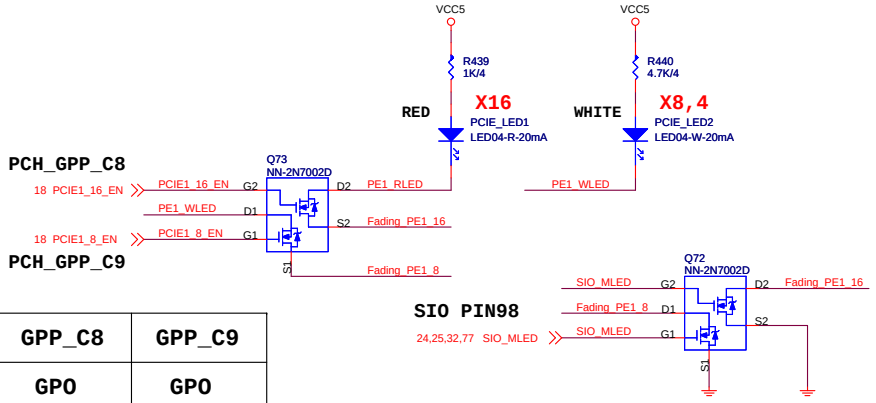




SMBUS ESD



PCIE SLOT LED



GPIO / LED	GPP_C8	GPP_C9
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)

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Size: Custom	Document Description: PCIE1(X16) & PCIE2(X1) Slots
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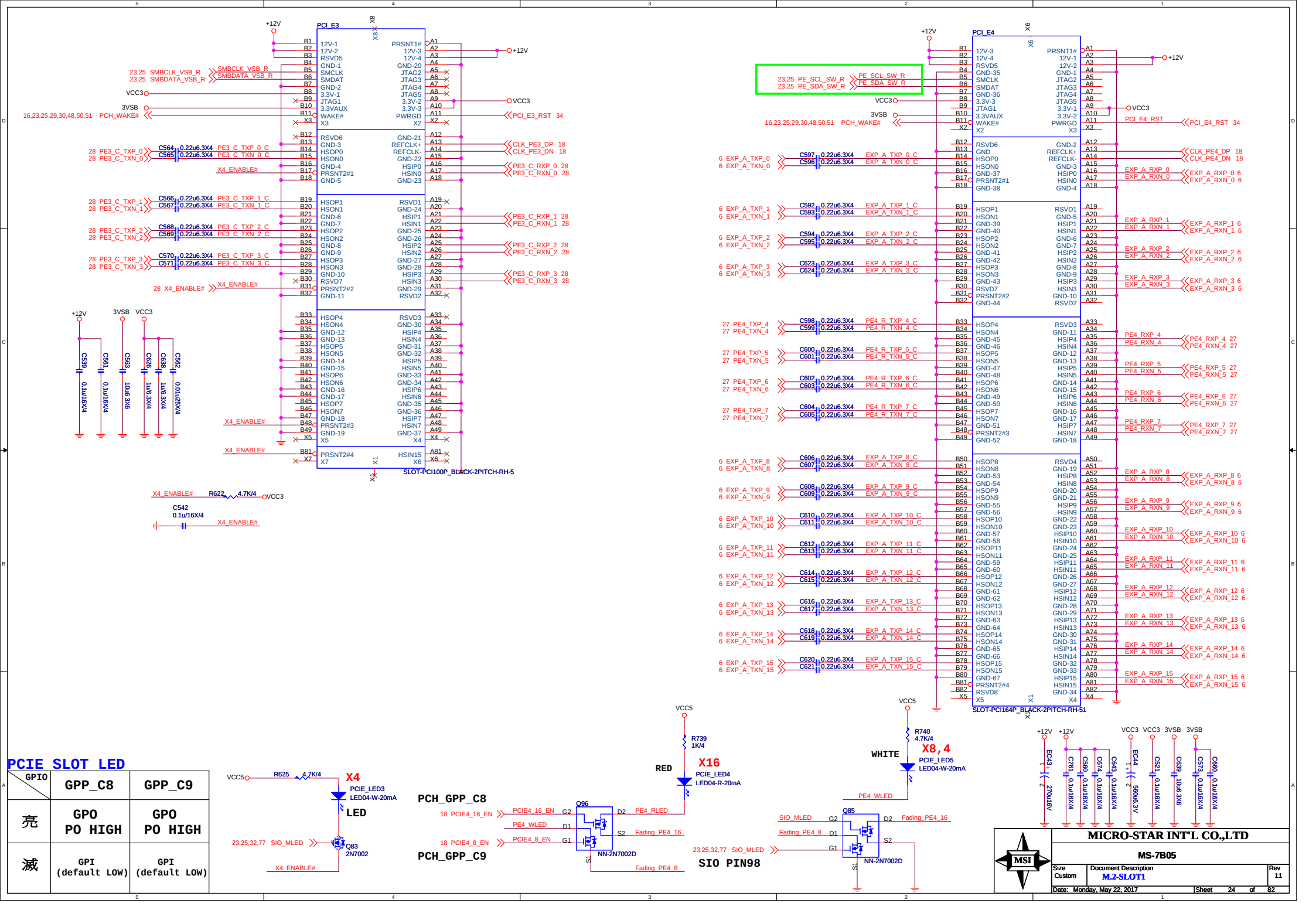
PCI_E3
SLOT-PCI100P_BLACK-2PITCH-RH-5
PCI_E4
SLOT-PCI164P_BLACK-2PITCH-RH-51
PCIE SLOT LED
GPIO | GPP_C8 | GPP_C9
亮 | GPO PO HIGH | GPO PO HIGH
滅 | GPI (default LOW) | GPI (default LOW)
X4
PCIE_LED3 LED04-W-20mA
LED
Q83 2N7002
X16
PCIE_LED4 LED04-R-20mA
RED
X8,4
PCIE_LED5 LED04-W-20mA
WHITE
PCH_GPP_C8
PCH_GPP_C9
Q96
Q85
NN-2N7002D
SIO PIN98
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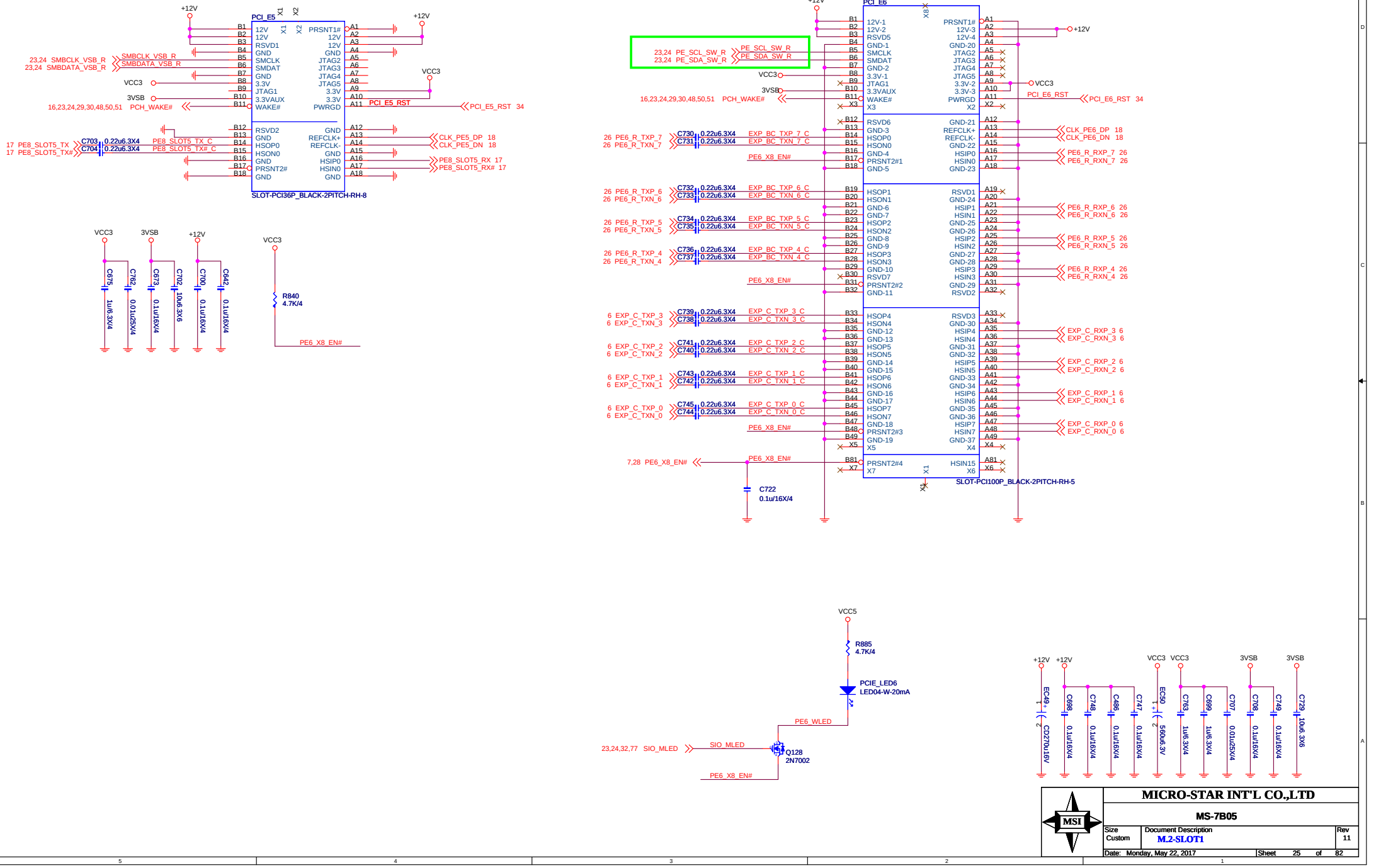

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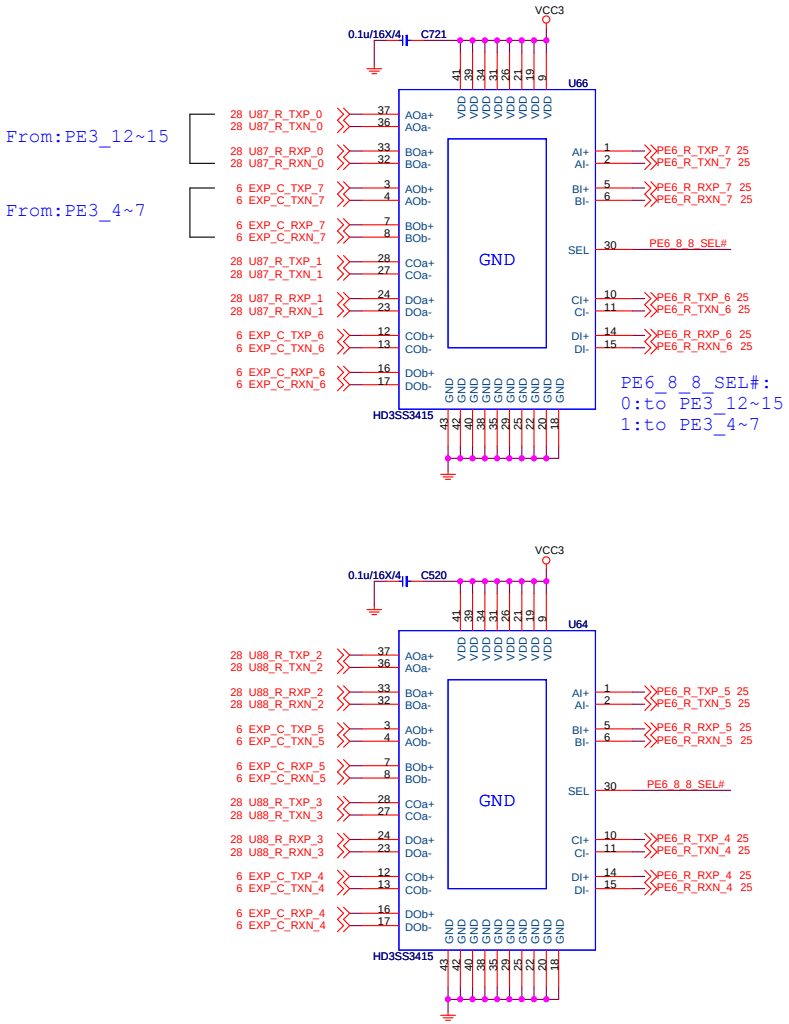

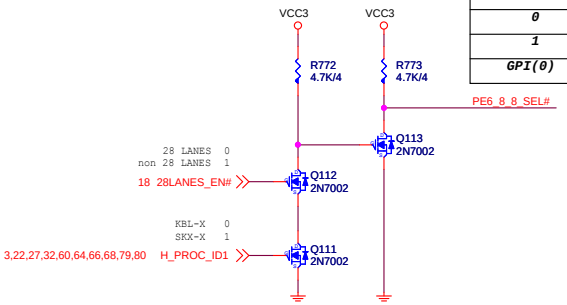

H_PROC_ID1	28LANES_EN#	PE6_8_8_SEL#
1	1	1
0	1	0
1	0	0
GPI(0)	GPI(0)	GPI(0)

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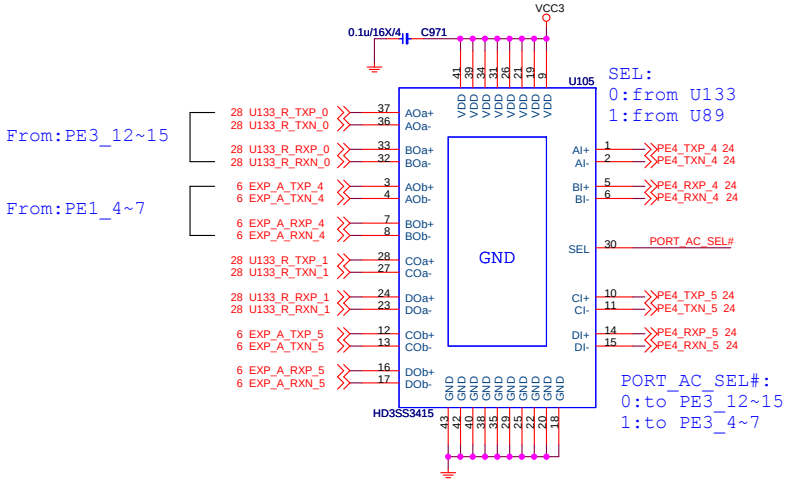
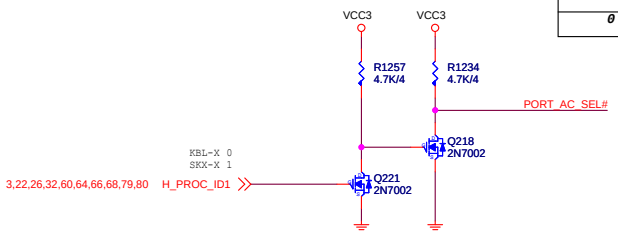
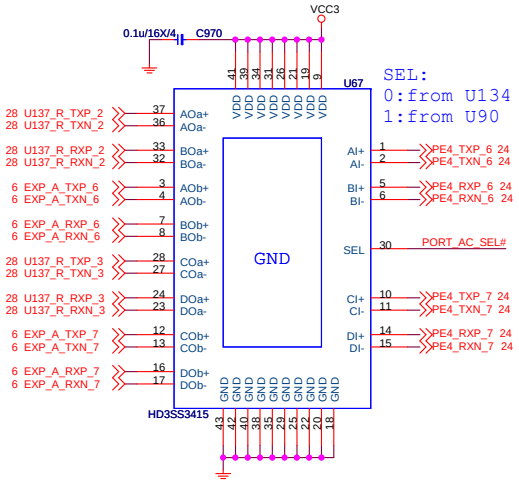




H_PROC_ID1	PORT_AC_SEL#
1	1
0	0



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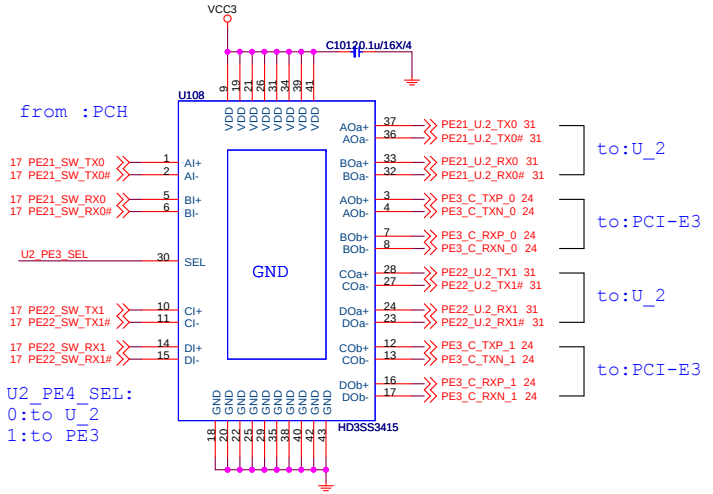
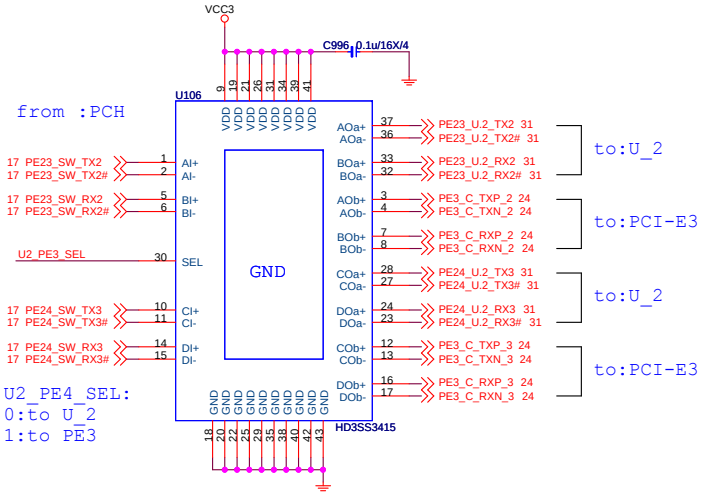
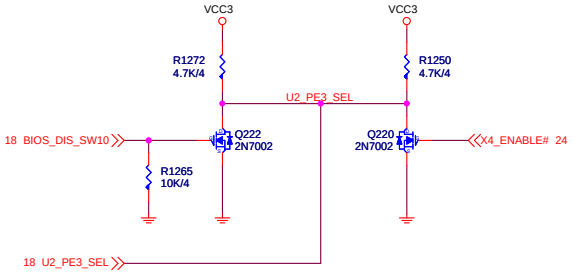




X4_ENABLE#	U.2_DET#	U2_PE3_SEL
1	1	U2
0	1	PE3
1	0	U2
GPI(0)	GPI(0)	GPI(PE3)

X4_ENABLE#:
Low : PCI_E3 connect to device
Hight : PCI_E3 un-device



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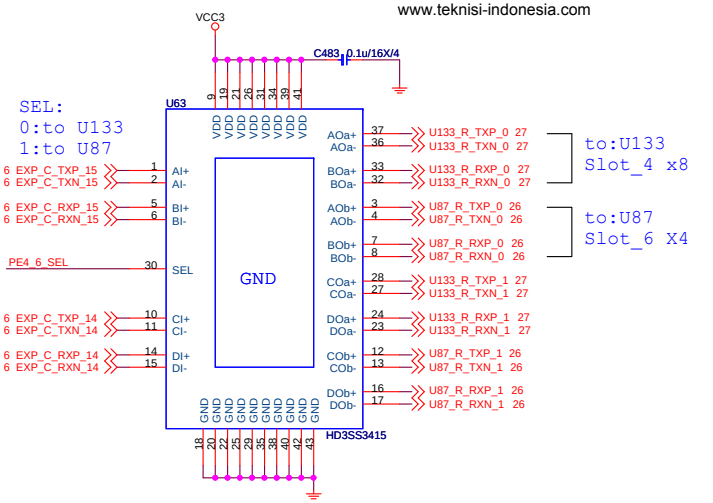
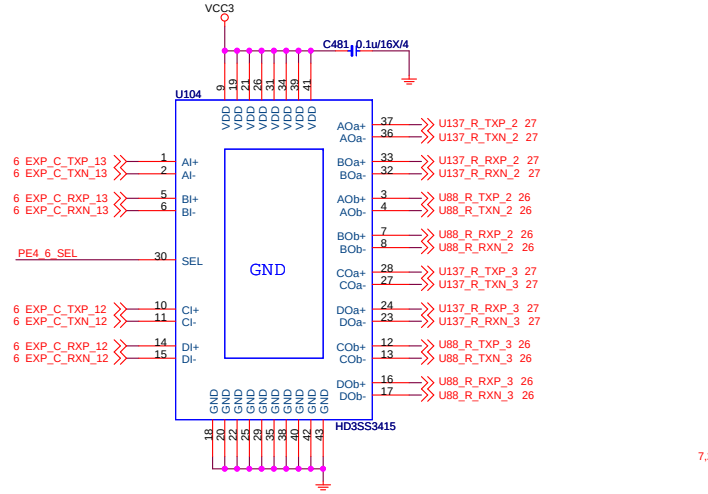
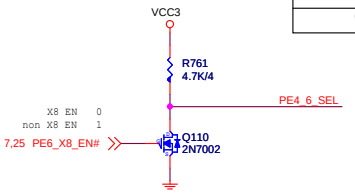
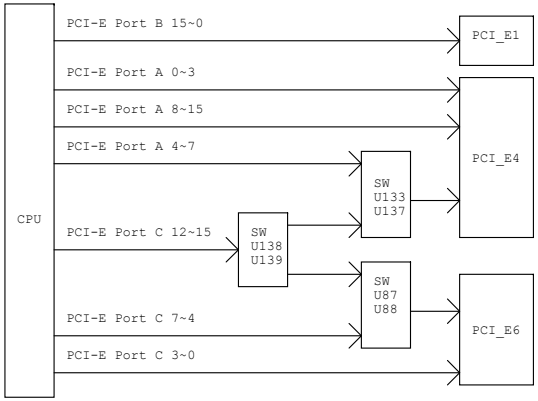




PE4_X8_EN#	PE4_6_SEL
1	0
0	1





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Size: Custom	Document Description: SKX/KBX SWITCH	Rev: 11
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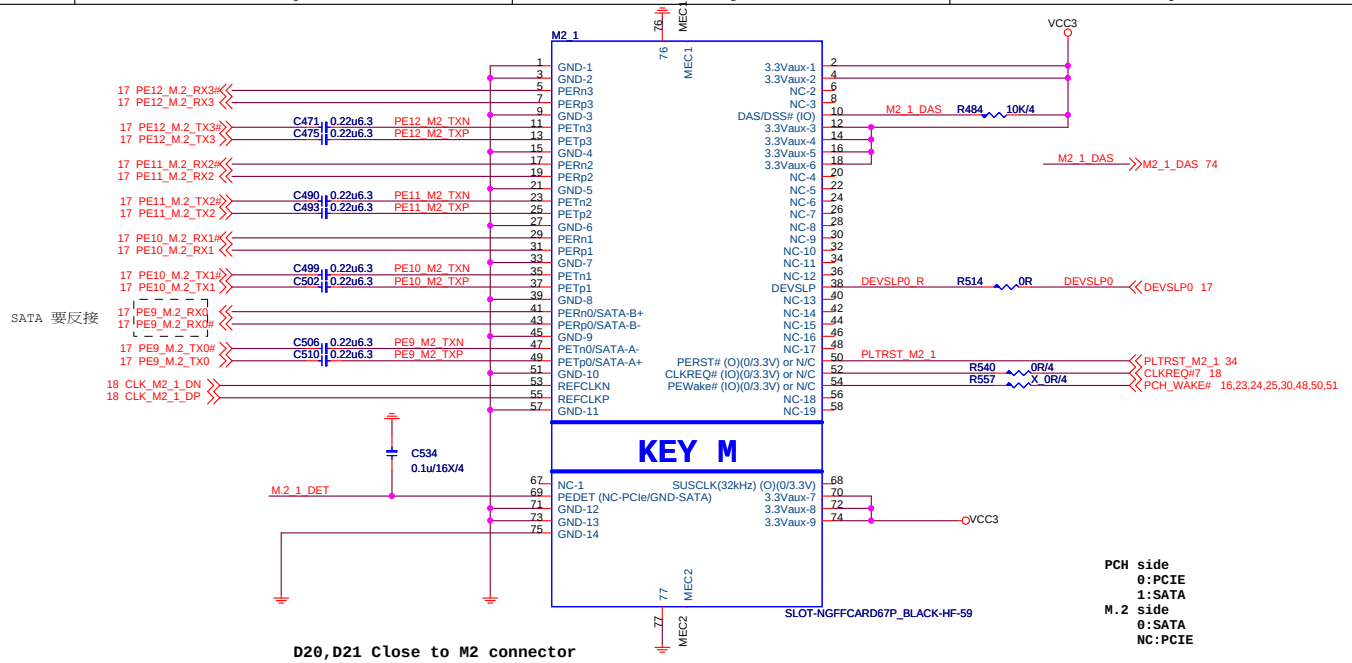
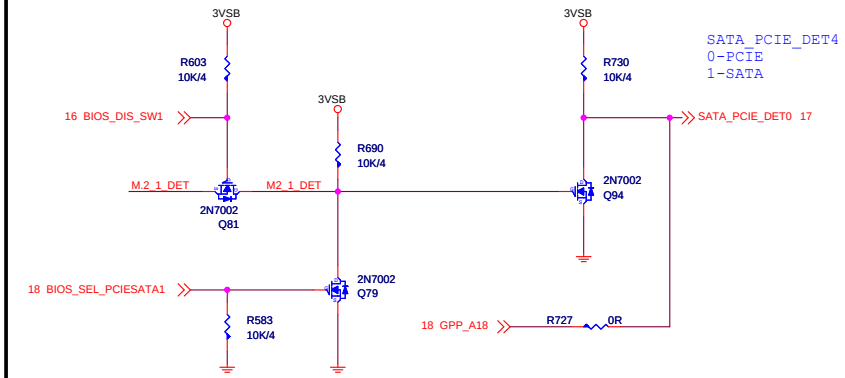


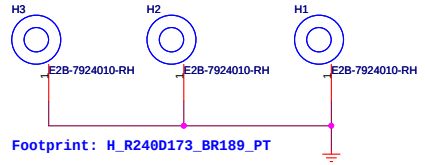
D20,D21 Close to M2 connector

```
PCH side
    0:PCIE
    1:SATA
M.2 side
    0:SATA
    NC:PCIE
```

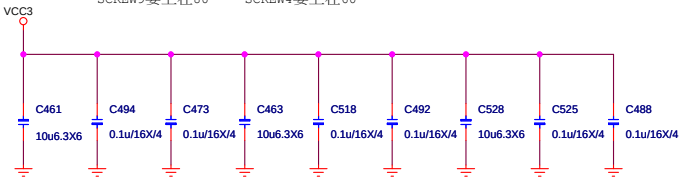


BIOS_MODE

BIOS_DIS_SW1	*BIOS_SEL_PCIESATA0*	*Mode*
0	*1*	*M2-SATA*
0	*0*	*M2-PCIE*
GPI(1)	*GPI(1)*	*AUTO*



Footprint: H_R240D173_BR189_PT



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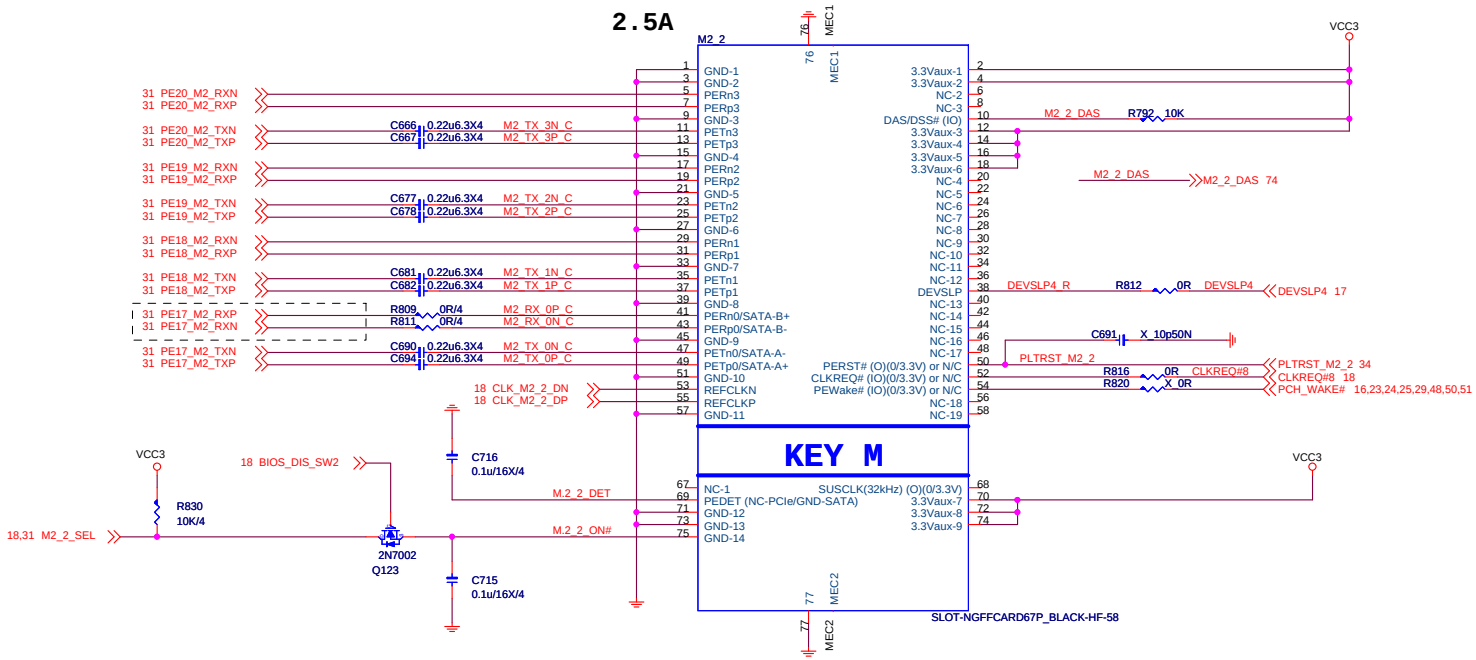
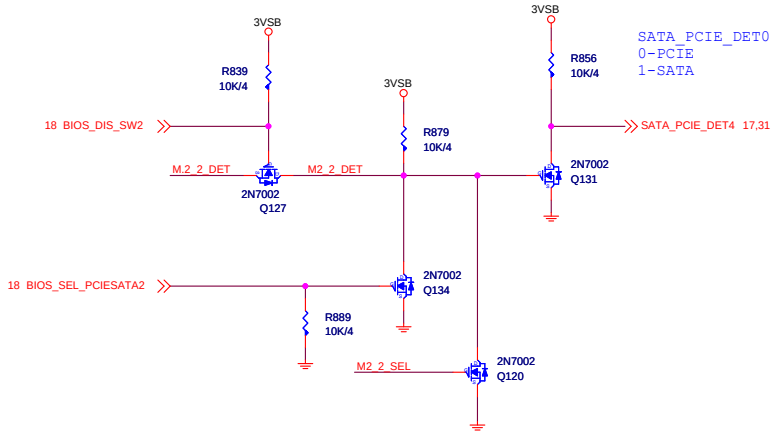
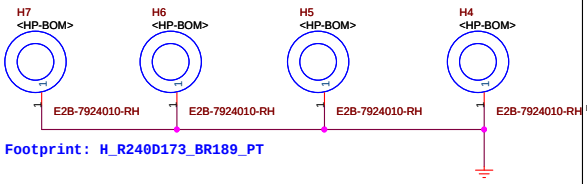
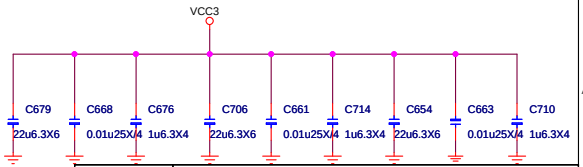




BIOS_MODE

M2_CPUSEL#	BIOS_DIS_SW2	M2_2_SEL	BIOS_SEL_PCIESATA2	Mode
GPI(1)	GPI(1)	GPI(1)	GPI(0)	AUTO
0	0	1	1	M2-CPU
1	0	1	0	SATA
1	0	0	1	M2-SATA
1	0	0	0	M2-PCIE





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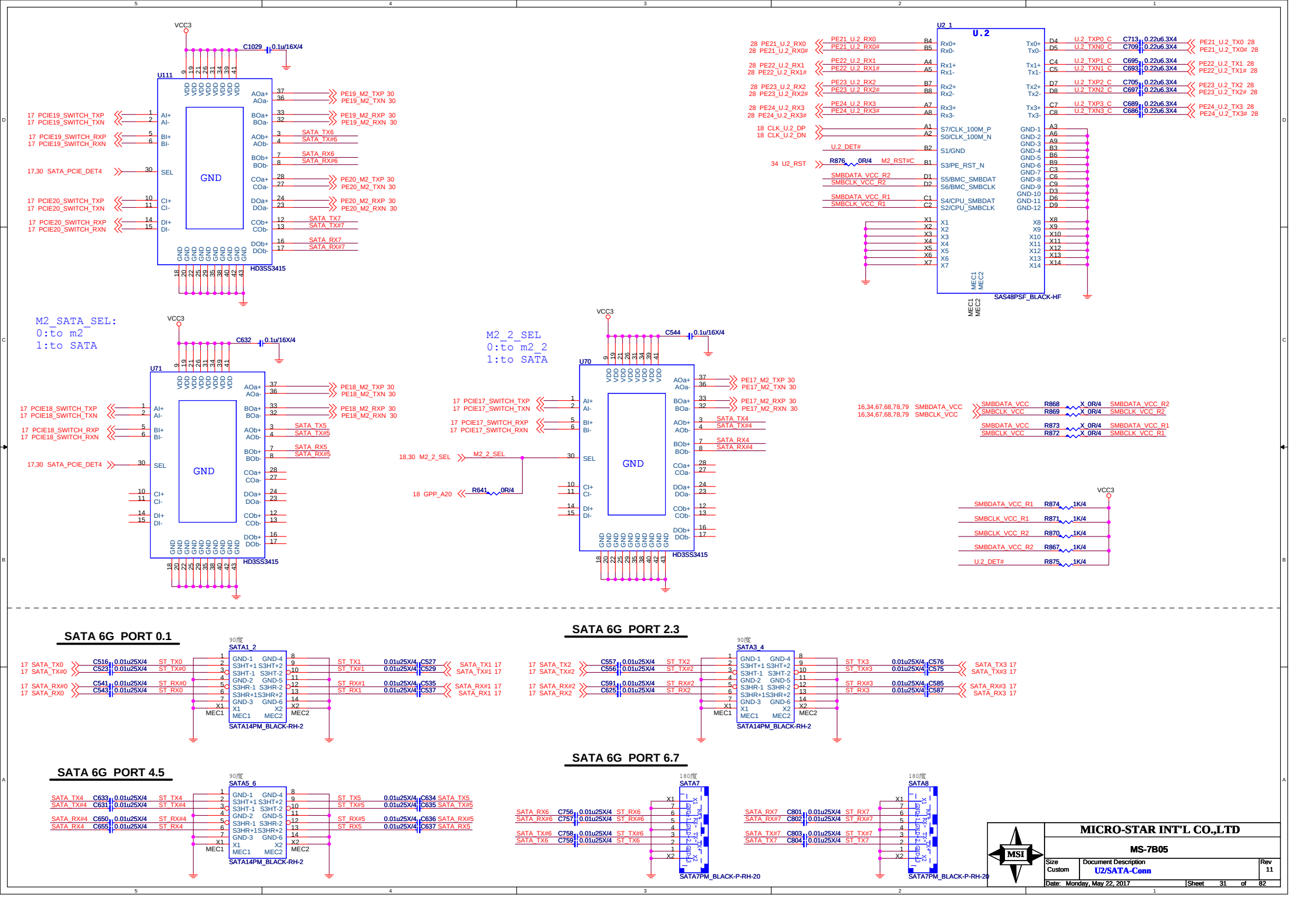
U111
HD3SS3415
U71
HD3SS3415
U70
HD3SS3415
U2_1
U.2
SAS48PSF_BLACK-HF
M2_SATA_SEL:
0:to m2
1:to SATA
M2_2_SEL
0:to m2_2
1:to SATA
SATA 6G PORT 0.1
SATA1_2
SATA14PM_BLACK-RH-2
SATA 6G PORT 2.3
SATA3_4
SATA14PM_BLACK-RH-2
SATA 6G PORT 4.5
SATA5_6
SATA14PM_BLACK-RH-2
SATA 6G PORT 6.7
SATA7
SATA7PM_BLACK-P-RH-20
SATA8
SATA7PM_BLACK-P-RH-20
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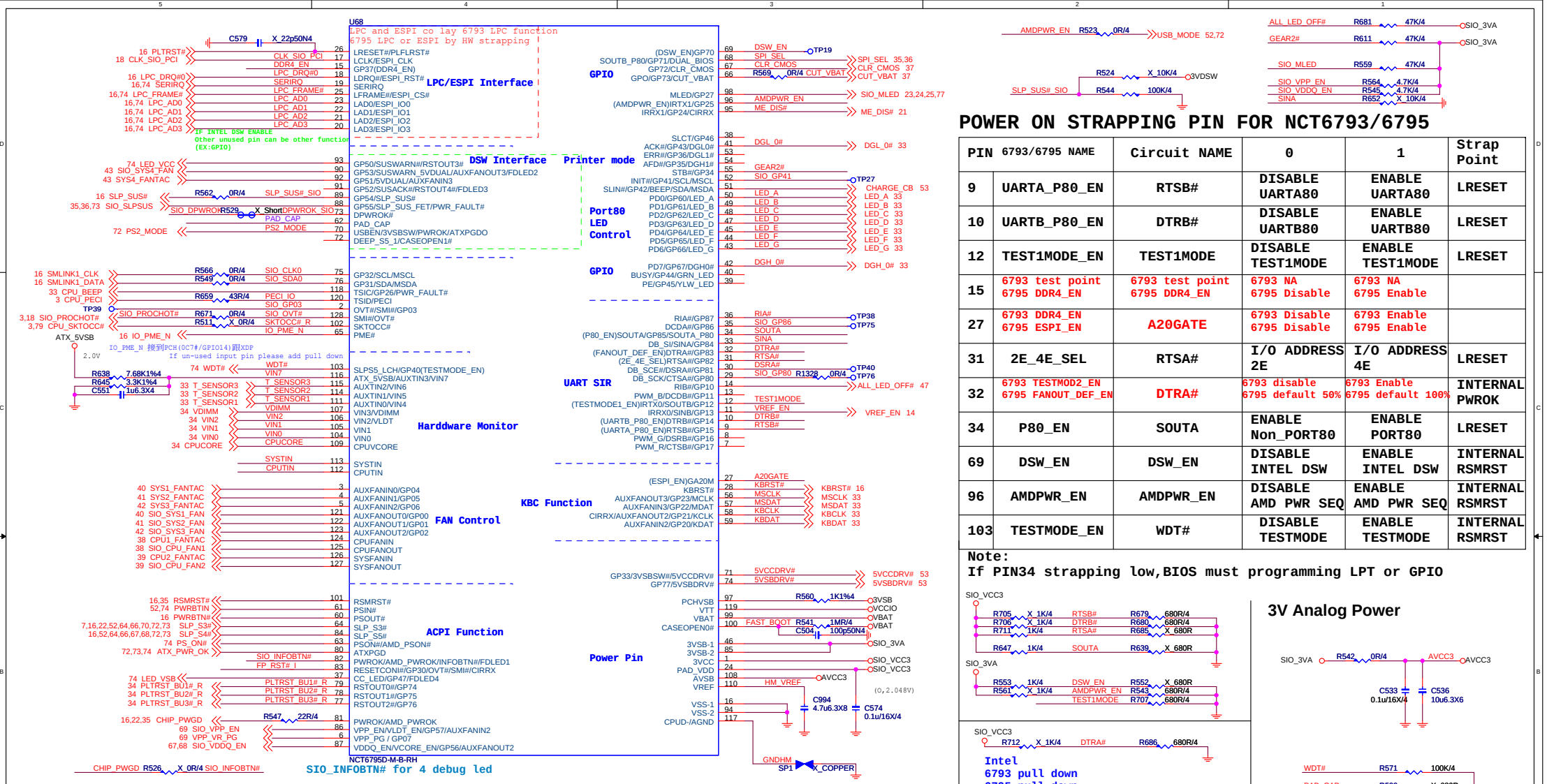
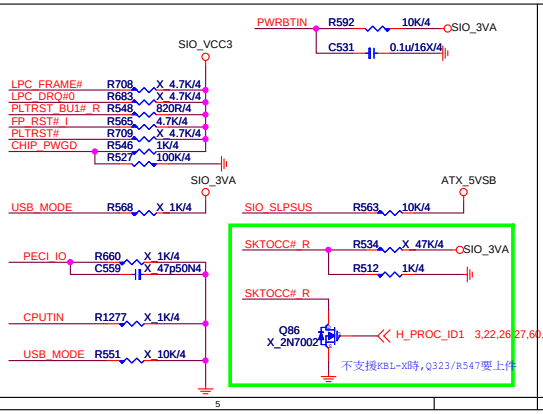
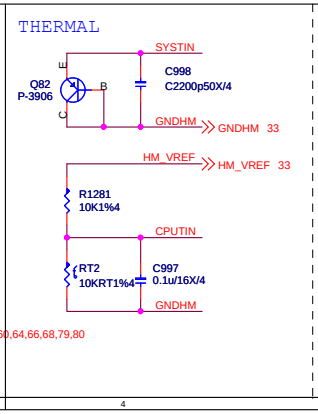
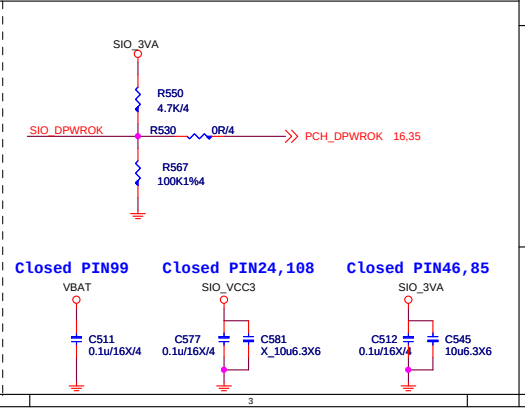
U2/SATA-Conn
Monday, May 22, 2017





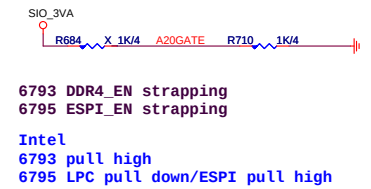


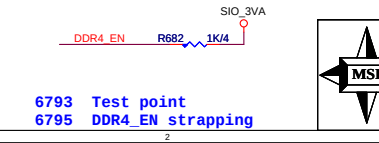


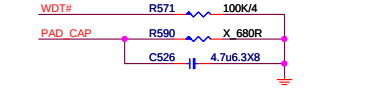
POWER ON STRAPPING PIN FOR NCT6793/6795

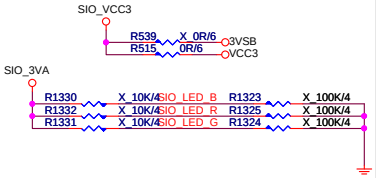
PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO









3V Analog Power

ESPI CONNECT PCH_1P8
LPC CONNECT VCC3 POWER

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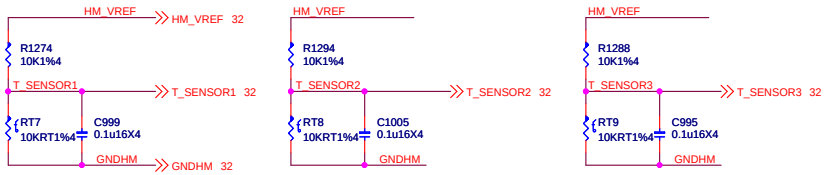
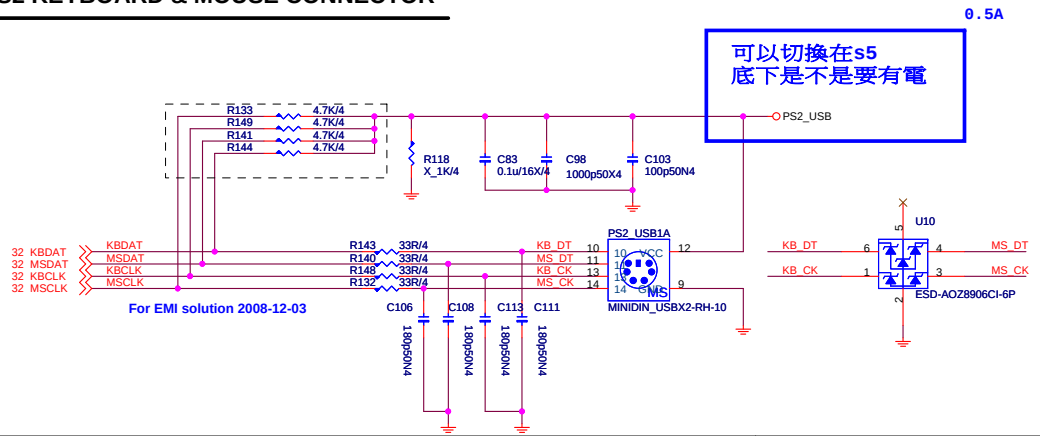
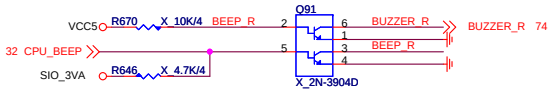
THERMAL



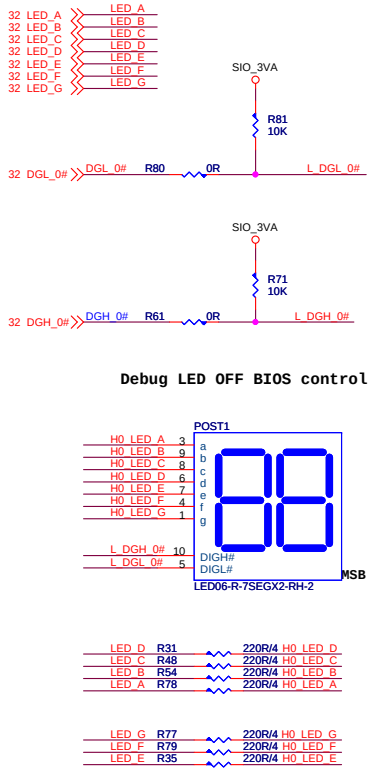
PS2 KEYBOARD & MOUSE CONNECTOR



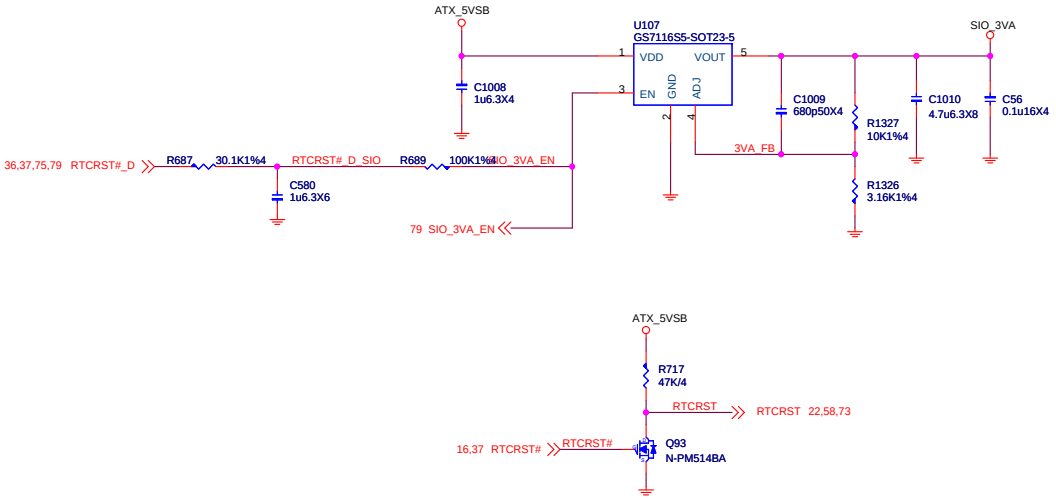
COM Port for BIOS Debug



DEBUG LED



SLP_SUS Co-lay circuit



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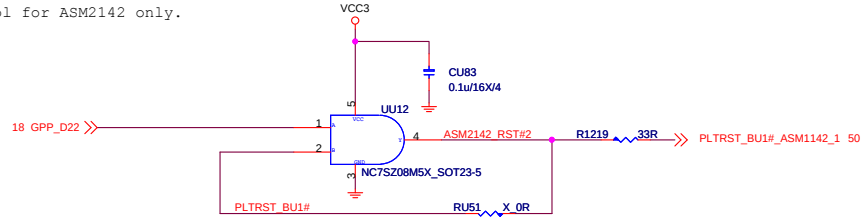
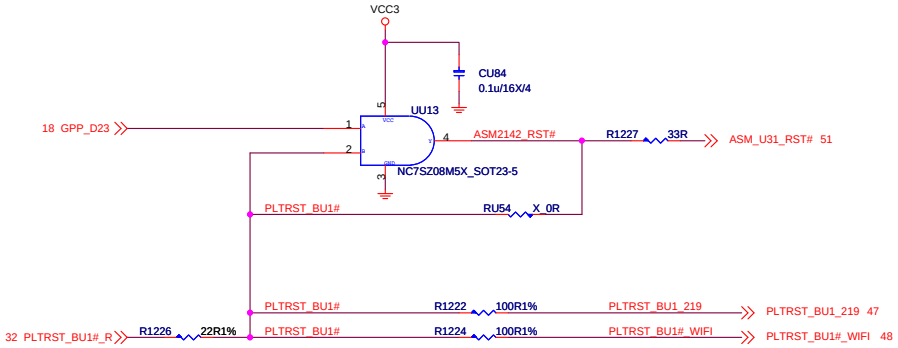
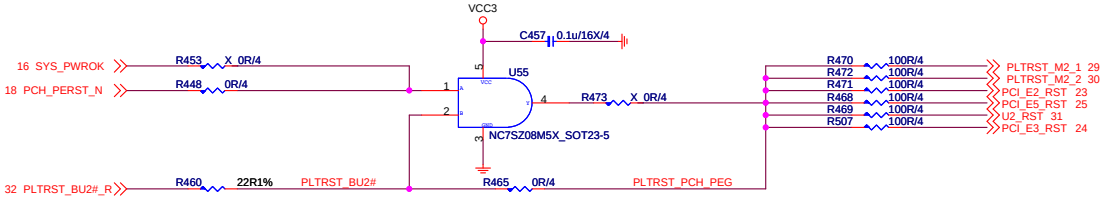
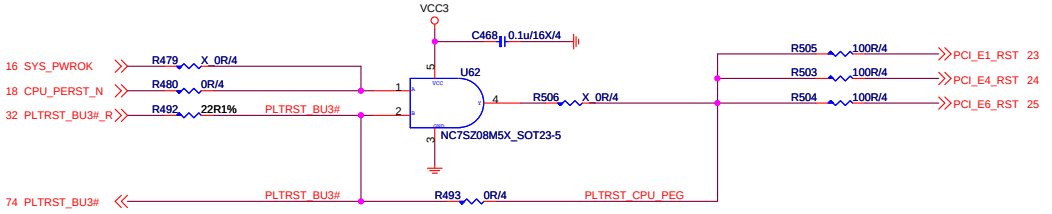
Reset control for ASM2142 only.



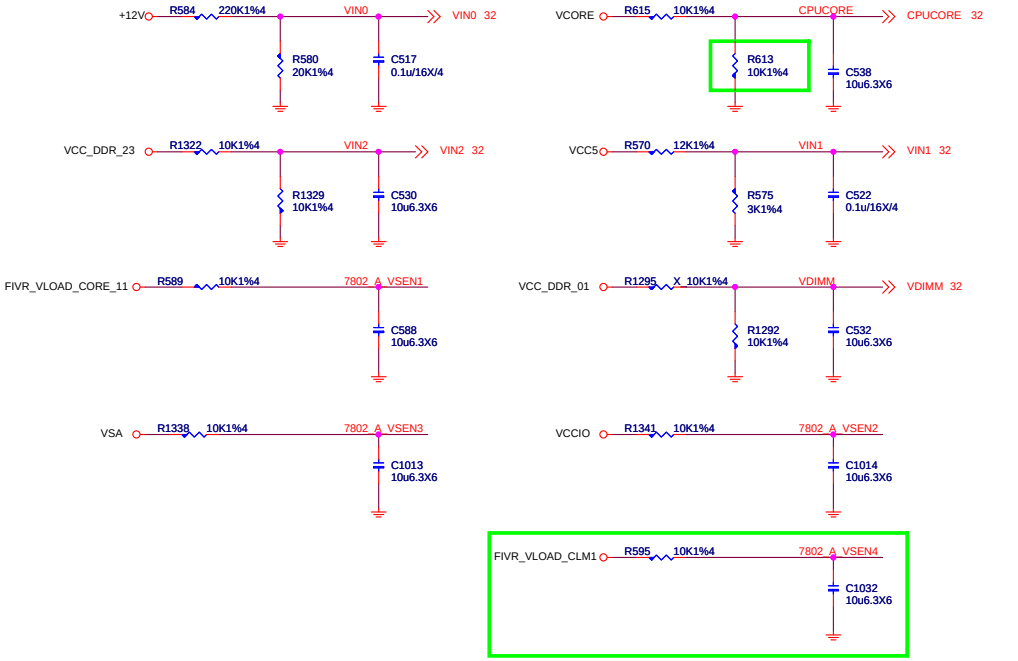


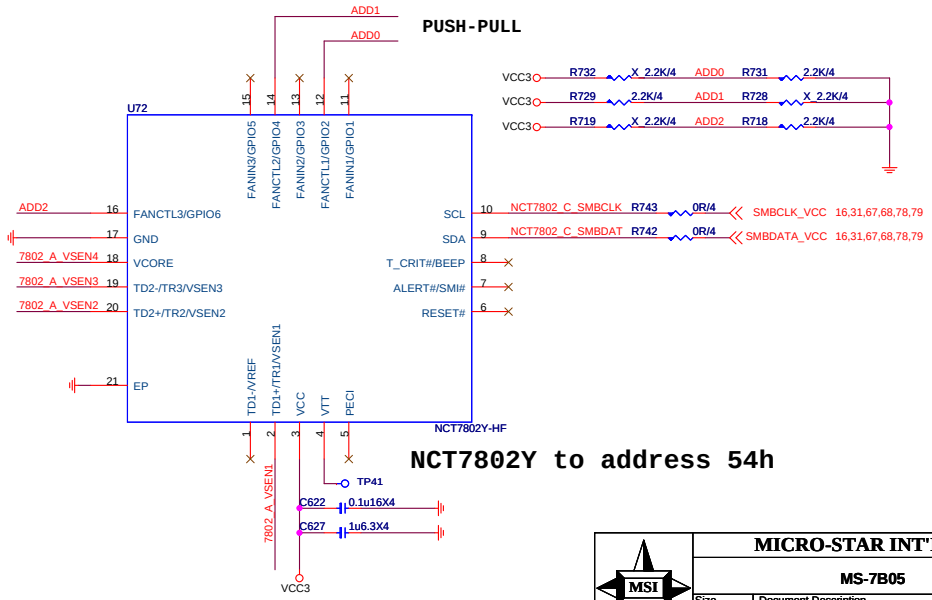




HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect





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Part Number:N31-2061341-H06

16,52 PCH_SPI_CS0# PCH_SPI_CS0#
16,21,52 PCH_SPI_MOSI PCH_SPI_MOSI
16,21,52 PCH_SPI_MISO PCH_SPI_MISO
16,52 PCH_SPI_CLK PCH_SPI_CLK
16,21 PCH_SPI_IO2 PCH_SPI_IO2
16,21 PCH_SPI_IO3 PCH_SPI_IO3

SPI CS# < 25pF
D0G-0402510-SI0

close to JSPI1 for ESD use

SPI_VCC3 R855 0R/6 3VSB

SPI DEBUG PROT
Close to SPI ROM

SPI_VCC3 C726 0.1u/16X/4

JSPI1
PCH_SPI_MISO PCH_SPI_MOSI
PCH_SPI_CS# PCH_SPI_CLK
SPI_SW_SEL
PCH_SPI_IO2 PCH_SPI_IO3
H2X6[10]M-2PITCH_BLACK-RH-3
N31-2061451-H06

PCH_SPI_CS0# R846 0R/4
D19 ESD-AOZ8131DI
C727 0.1u/16X/4

For TL624-1.1 : Stuff D7
Old : Only RSVD (Because 12V level)

P.S Close to JSPI1

HW MODE

A BIOS
B BIOS
MEC1 MEC2
BIOS_SW1 SW-DIP_BLACK-RH
SPI_SEL_R SPI2_SW
C755 0.1u/16X/4
R891 1K/4 SPI_SEL
R902 4.7K/4
SPI_VCC3
Skylake use SPI_VCC3
Skylake use SPI_VCC3
C753 0.1u/16X/4

SIO NCT6793 GP71
32,36 SPI_SEL
GPI default low
Active push pull high switch to SPI2
For auto testing in factory.
R896 100K1%4
U84 NC7SB3157P6X_SOT323-6
PCH_SPI_CS# SPI_SEL SPI_CS1# SPI_CS2#

IN=0 , D connected to S2 (SPI1- A Bios)
IN=1 , D connected to S1 (SPI2- B Bios)

ATX_5VSB R881 10K/4 SPI_SW_SEL SPI_SW_SEL 52,79
16,32 PCH_DPWROK D21 S-LRB520S-40T1G-HF
16,32 RSMRST# D22 S-LRB520S-40T1G-HF
16,22,32 CHIP_PWGD D23 X_S-LRB520S-40T1G-HF
32,36,73 SIO_SLPSUS D20 S-LRB520S-40T1G-HF

VCC5
R847 4.7K/4
A_BIOS1 LED04-R-20mA2.4V
R835 1K/4
B_BIOS1 LED04-W-20mA3.9V
ATX_5VSB
R898 47K/4
Q135 2N7002D
SPI_SEL SPI1_SW
Q137 2N7002

SPI_VCC3
R844 X_1K/4 PCH_SPI_MOSI
R845 X_1K/4 PCH_SPI_MISO

SPI FLASH ROM
Place close to SB.

MXIC:M31-2512832-M24
WinB:M31-2512853-W03

32M ROM For X299

A BIOS
R818 2.2K/4
A_SPI1
SPI_CS1# PCH_SPI_MISO PCH_SPI_IO2
R821 33R/4 SPI1_MISO
R825 33R/4 SPI1_IO2
C688 0.1u/16X/4
C692 10u6.3X6
SPI1_IO3 SPI1_CLK SPI1_MOSI
R819 R826 R828 33R/4
PCH_SPI_IO3 PCH_SPI_CLK PCH_SPI_MOSI
W25Q128FVSIQ-HF
M31-2512893-W03

B BIOS
R813 2.2K/4
B_SPI1
SPI_CS2# PCH_SPI_MISO PCH_SPI_IO2
R822 R833 33R/4
SPI2_MISO SPI2_IO2
C685 0.1u/16X/4
C687 10u6.3X6
SPI2_IO3 SPI2_CLK SPI2_MOSI
R817 R823 R834 33R/4
PCH_SPI_IO3 PCH_SPI_CLK PCH_SPI_MOSI
W25Q128FVSIQ-HF
M31-2512893-W03

*SPI_CLK & SPI_MOSI must be length matched to within 500mils. < 6 inch
*SPI_CLK & SPI_CS0# must be length matched to within 500mils.

ATX_5VSB
U81 X_GS7116S5-SOT23-5
VDD VOUT EN GND ADJ
C751 X_1u6.3X4
R880 X_47K/4
C750 X_680p50X4
R886 X_10K1%4
SPI_FB
R882 X_3.09K1%4
C728 X_22u6.3X8
SIO_SLPSUS
Q133 X_2N7002

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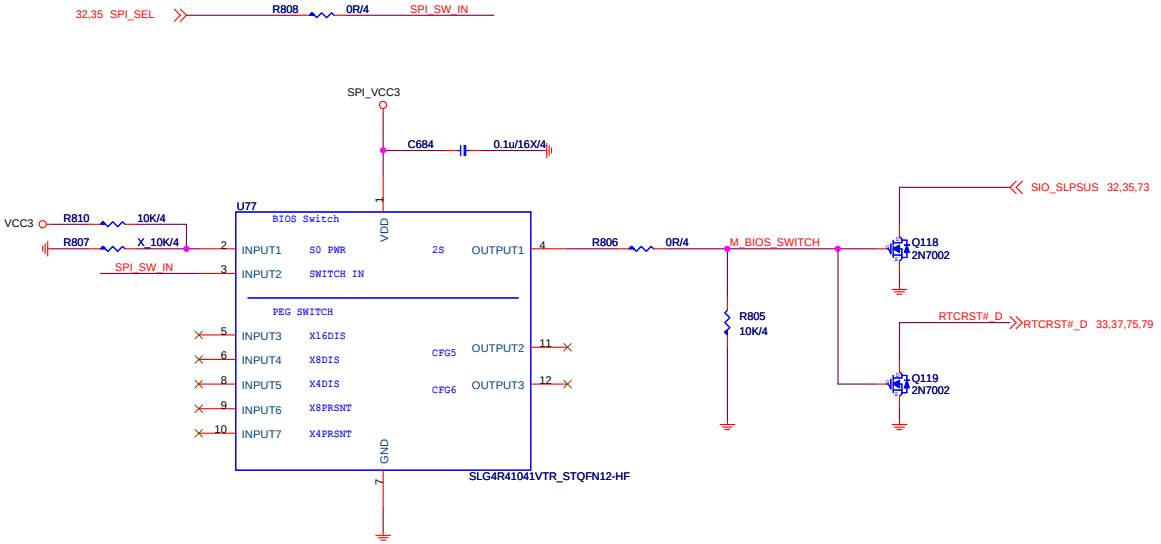
Skylake/Kabylake Path Circuit For Dual Bios



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RTCRST# R463 X_0R/4 RTCRST#_D

CUT VBAT

20160629

CLR_CMOS
R476 X_100K/4
CUT_VBAT
R483 X_100K/4

JBAT1 H1X2M_BLACK-RH
VBAT
R467 20K1%4
C456 1u6.3X6
D16 ESD-AOZ8131DI
32 CLR_CMOS
32 CUT_VBAT
SIO_3VA
R481 X_4.7K/4
R482 X_4.7K/4
CLR_CMOS
RTCRST#_D
CUT_VBAT
DIS_CHARGE
D15 X_100K/4

U58 SLG4B41231V_STQFN14-HF
VDD
C462 0.1u/16X/4
CLR_CMOS function 1
INPUT1 CLR_CMOS#
INPUT2 RTCRST#_D
RTCRST#_PCH
OUTPUT1 RTCRST#
RTCRST# 16,33
CUT_VBAT function 2
INPUT3 CUTVBAT
INPUT4 DIS_CHARGE
POWER_OFF
RTCRST#_SIO
OUTPUT2 POWER_OFF
OUTPUT3 RTCRST#_D
RTCRST#_D 33,36,75,79
LOW SWITCH
VIN VBAT
VBAT_PCH(POWER)
VOUT VBAT_PCH
NC-1 NC-2 GND-1 GND-2

if has cut other power,please use output 2.

if has discharge function R407 NC.

ATX_5VSB
R746 4.7K/4
R747 9.1KR1%0402
POWER_OFF
Q106 2N7002 3VDSW
Q105 2N7002 3VSB
Q102 2N7002 PCH_1VSB
3VA_OFF# 73
3VSB_EN# 73
PCH_1VSB_EN# 71

Add DCRTC dischage circuit

DCPRTC
R734 5.6K1%4
POWER_OFF R733 2.2K/4
Q99 2N7002
C589 0.1u/16X/4

VBAT

VBAT R464 VBAT_PCH
X_0R/4

VBAT C460 10u6.3X6
have timming issue keep 0805 size don't removed

VBAT
3VDSW
R1193 3K1%4
C459 1u6.3X6 Close to PCH
CRB
D33 S-BAT54C_SOT23
VBAT2
R1194 45.3K1%4
R1189 1K1%4
BAT1 BAT-2P-RH-1

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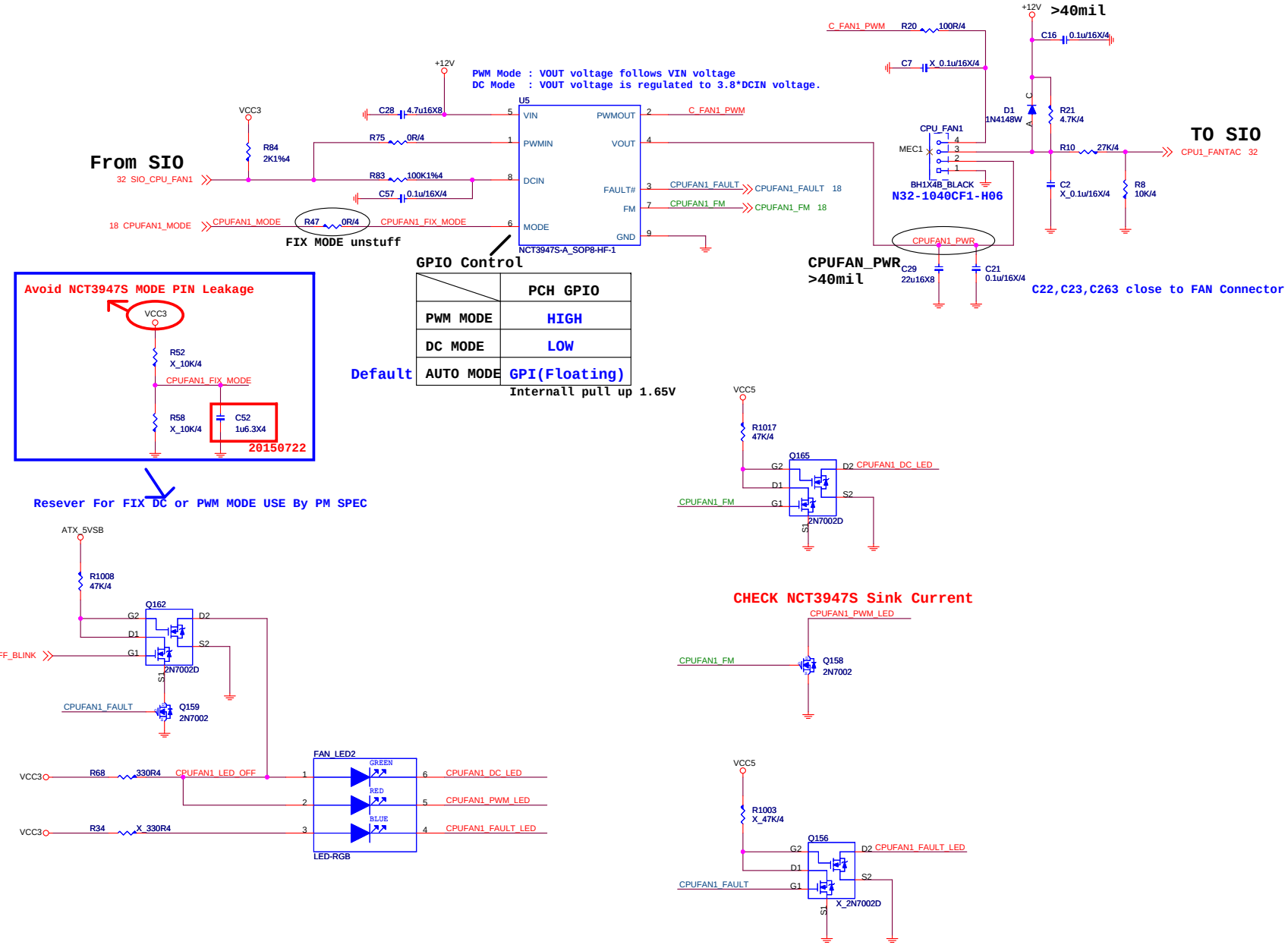
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



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Size: Custom	Document Description: CPU FAN1 — Rev: 11
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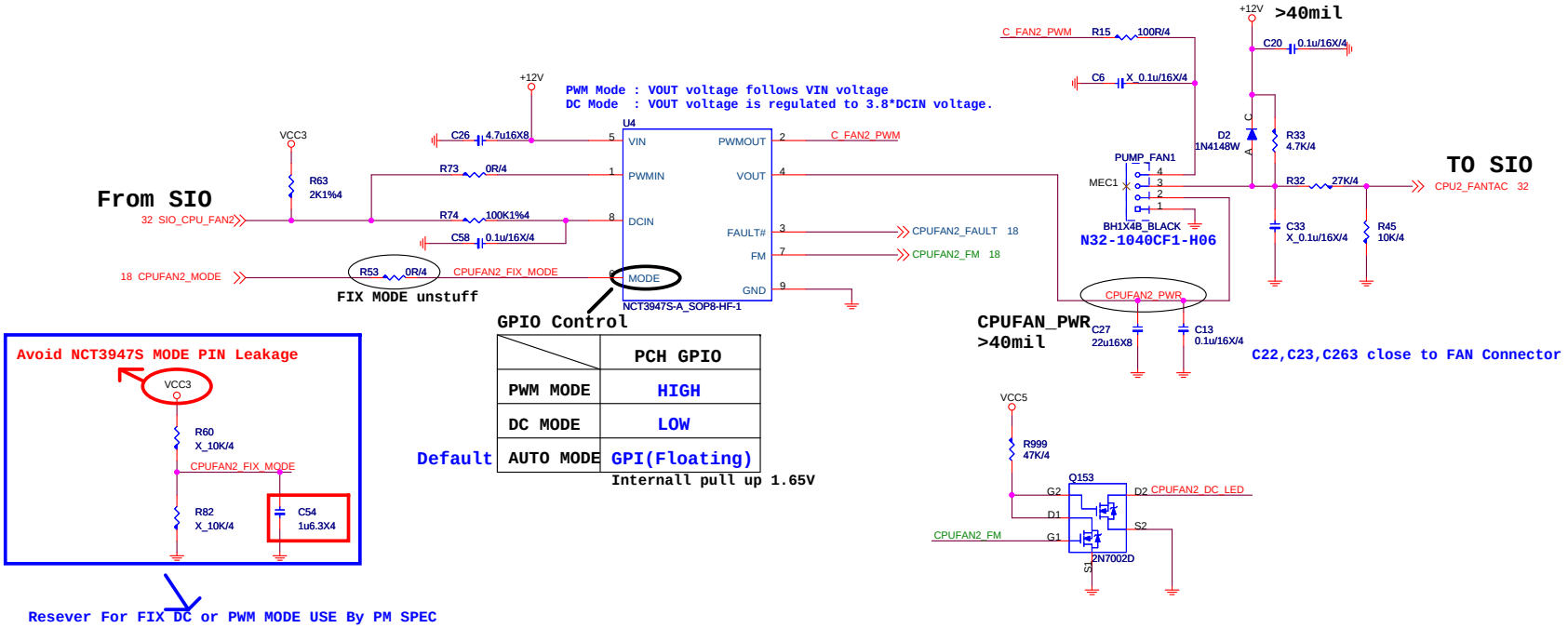
TYPE J : 4 PIN PUMP FAN USE NCT3947S USE PCH GPIO



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MS-7B05		
Size: Custom	Document Description: CPU FAN2	Rev: 11
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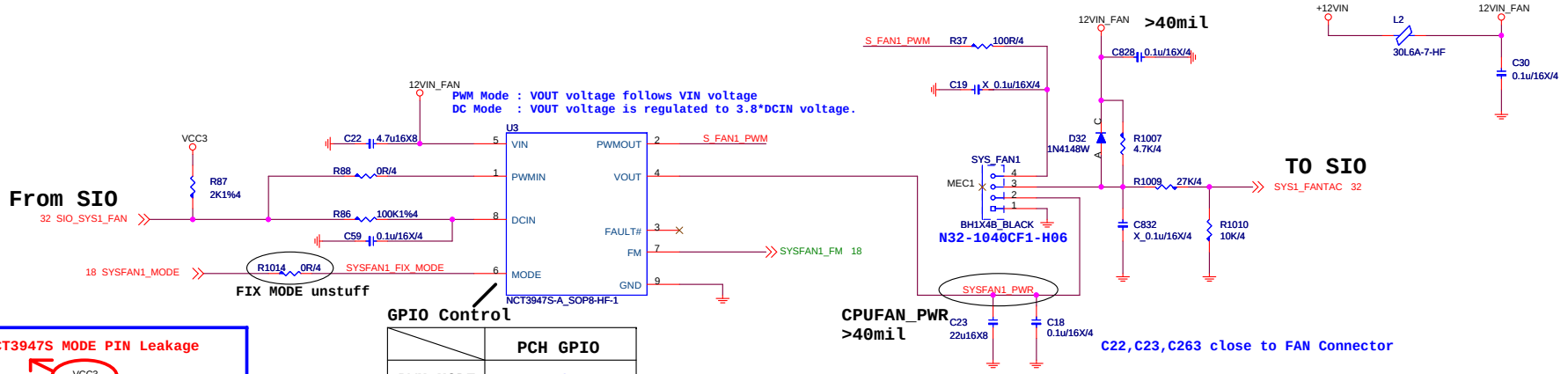
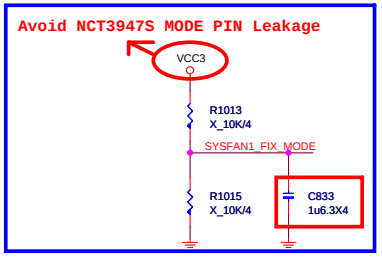
TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

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MS-7B05	
Size: Custom	Document Description: SYSTEM FAN1 www.teknisi-indonesia.com
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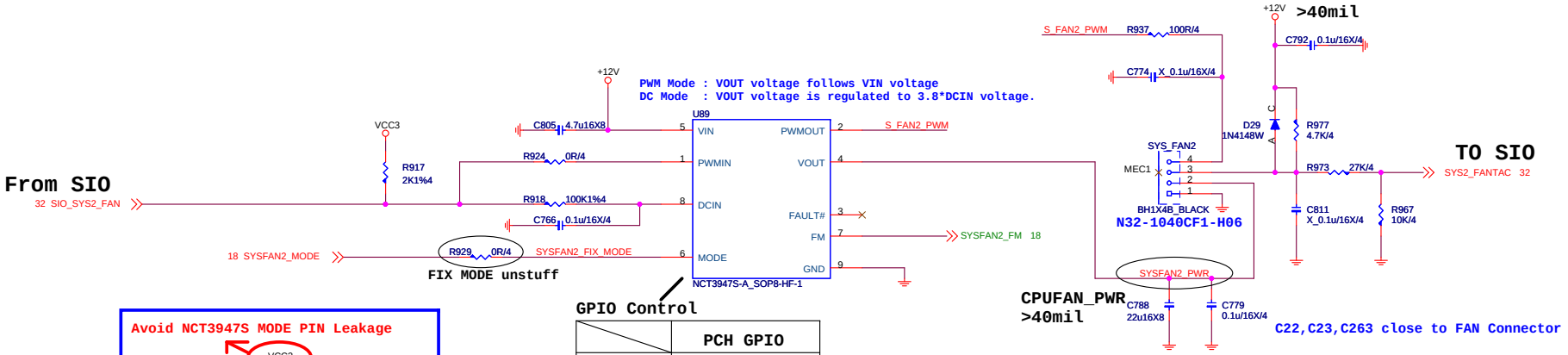
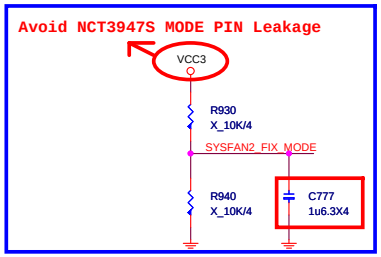
TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO





Resever For FIX DC or PWM MODE USE By PM SPEC

GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

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MS-7B05	
Size: Custom	Document Description: SYSTEM FAN2
Rev: 11	
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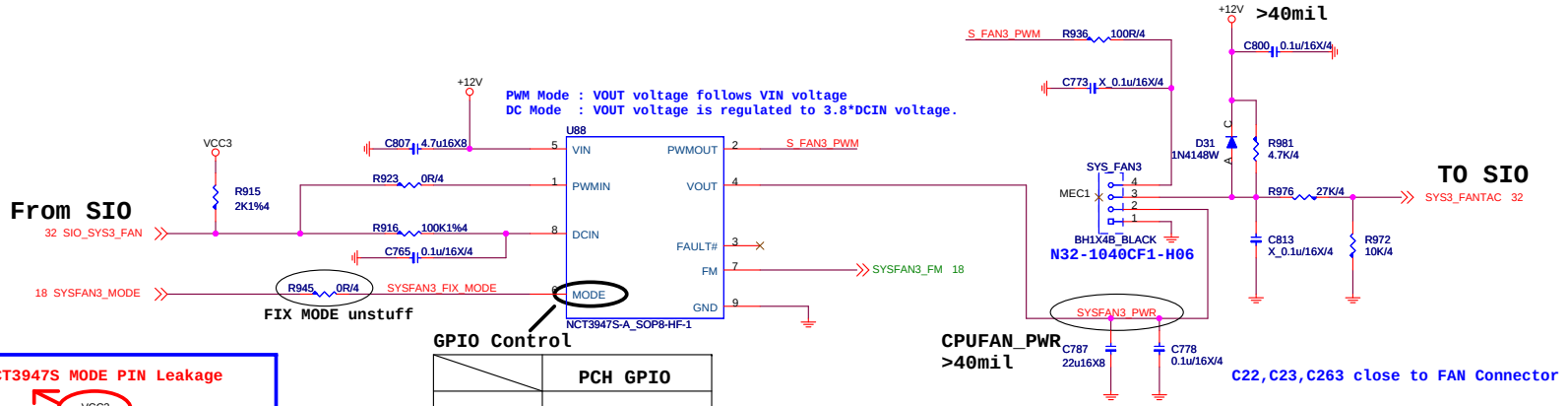
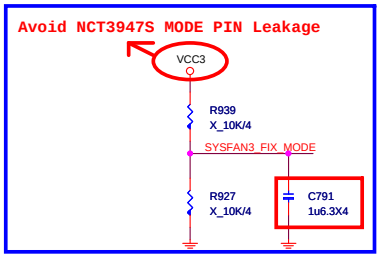
TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

MICRO-STAR INT'L CO.,LTD	
MS-7B05	
Size: Custom	Document Description: SYSTEM FAN3
Rev: 11	
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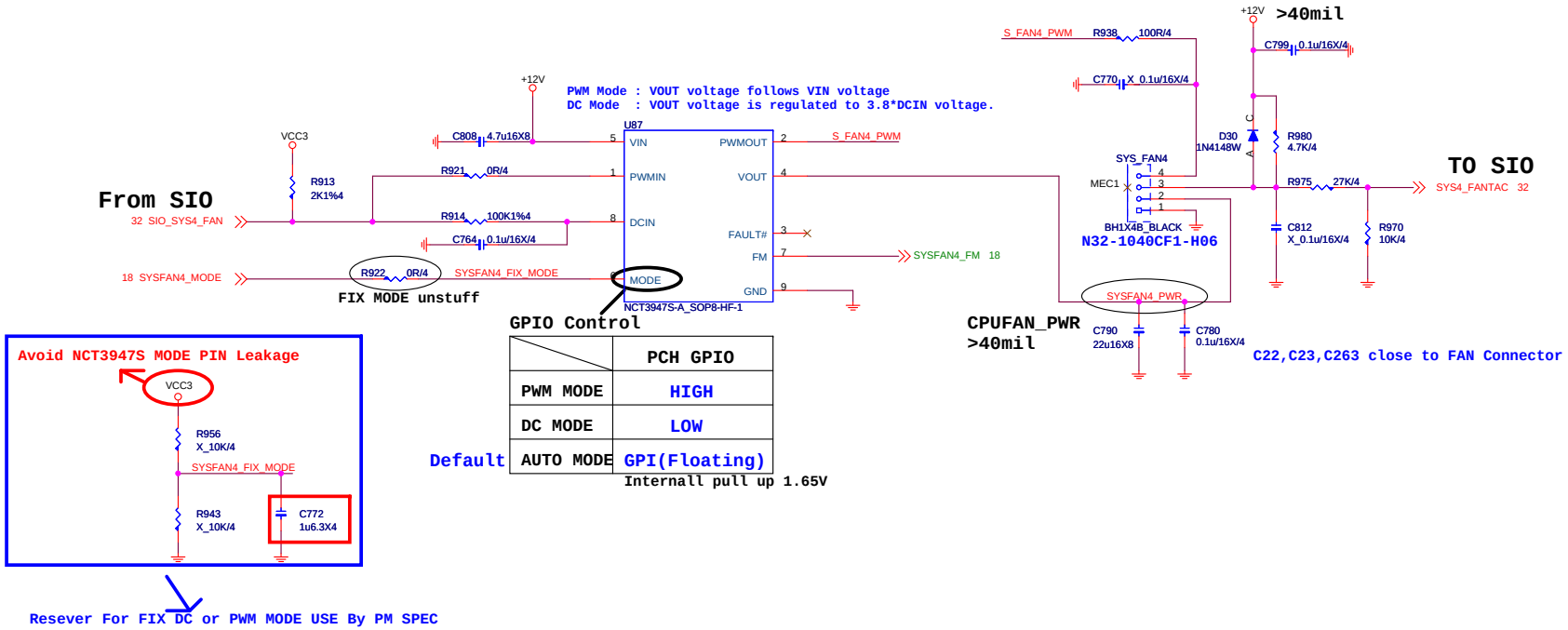
TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

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MS-7B05

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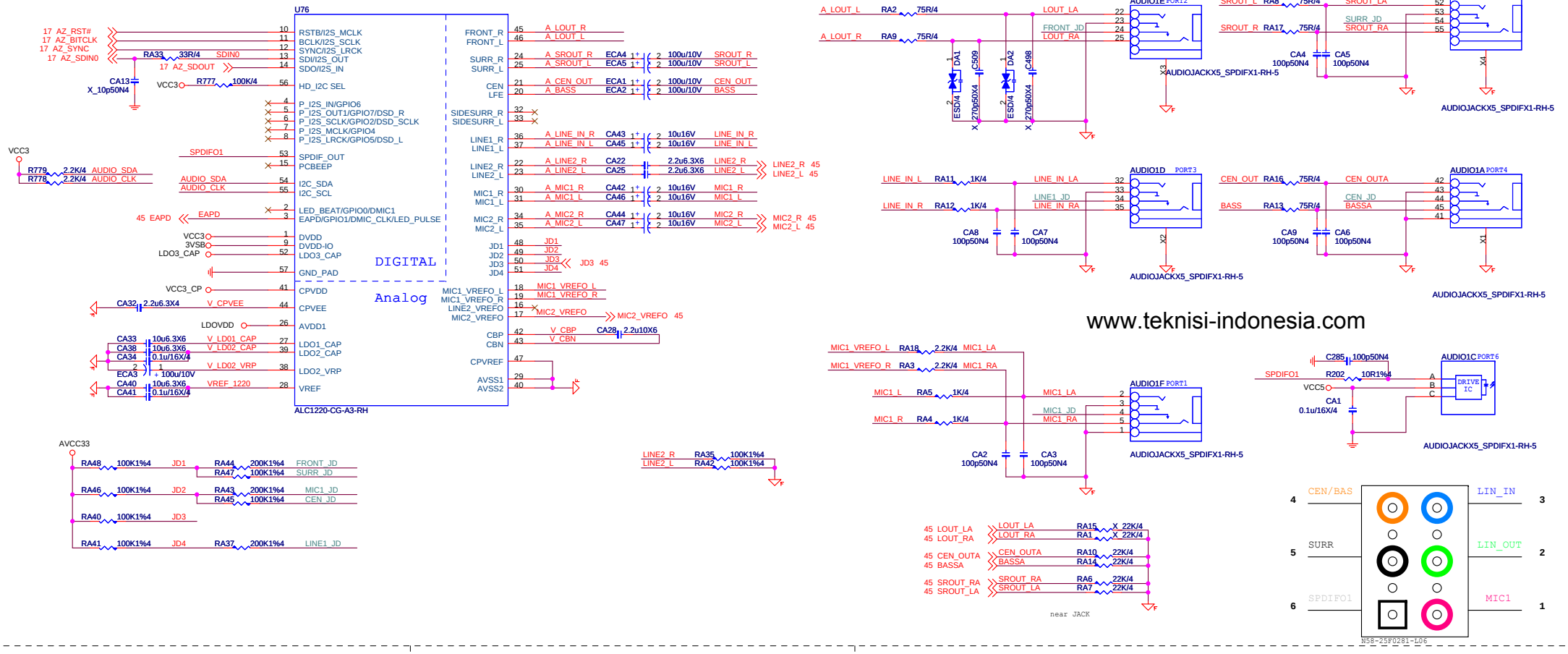
ALC1220



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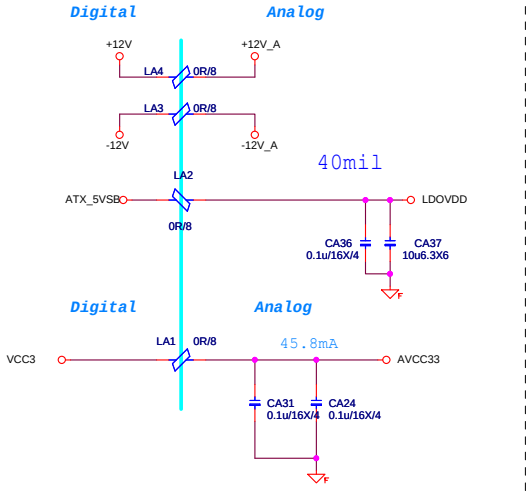
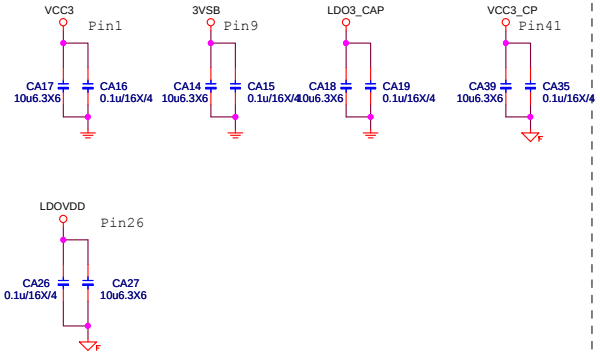
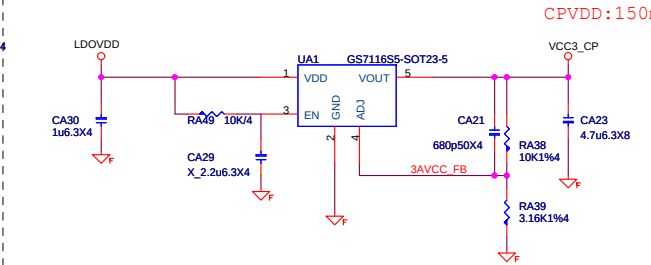


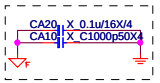
Closed Codec



CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V



EMI



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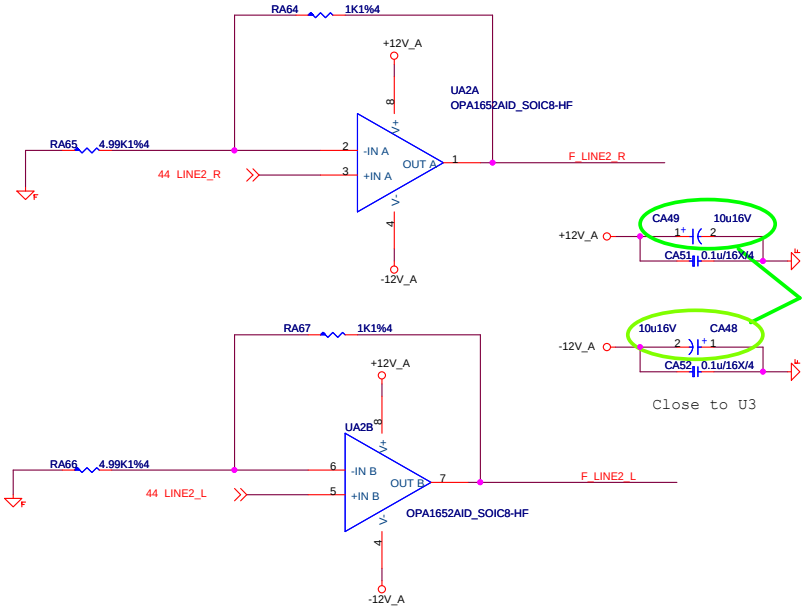
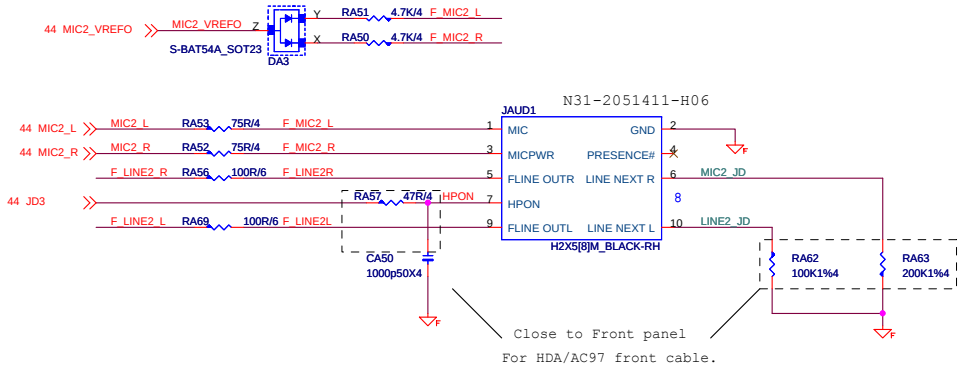


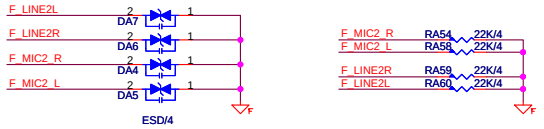


Close to Jack

ESD protect

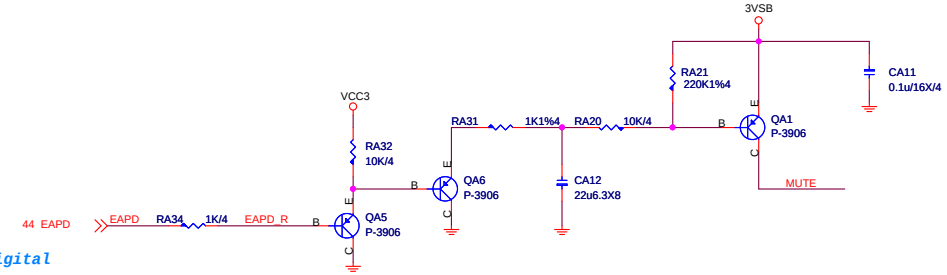
D0G-2950500-SI0

D0G-3010510-I05



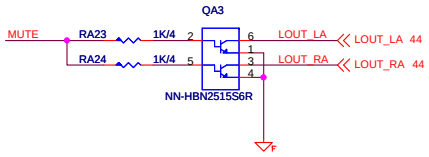
Rear Line OUT De-POP circuit

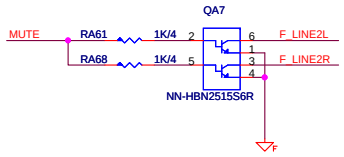
(De-pop circuit for Rear Line out & Front Headphone out)



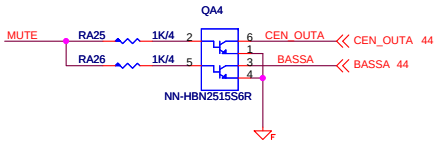
Digital

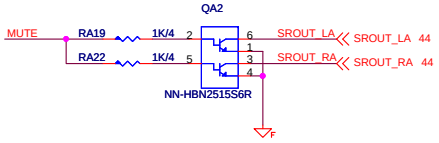
Analog





(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA13, CA23, CA24 to TVS)





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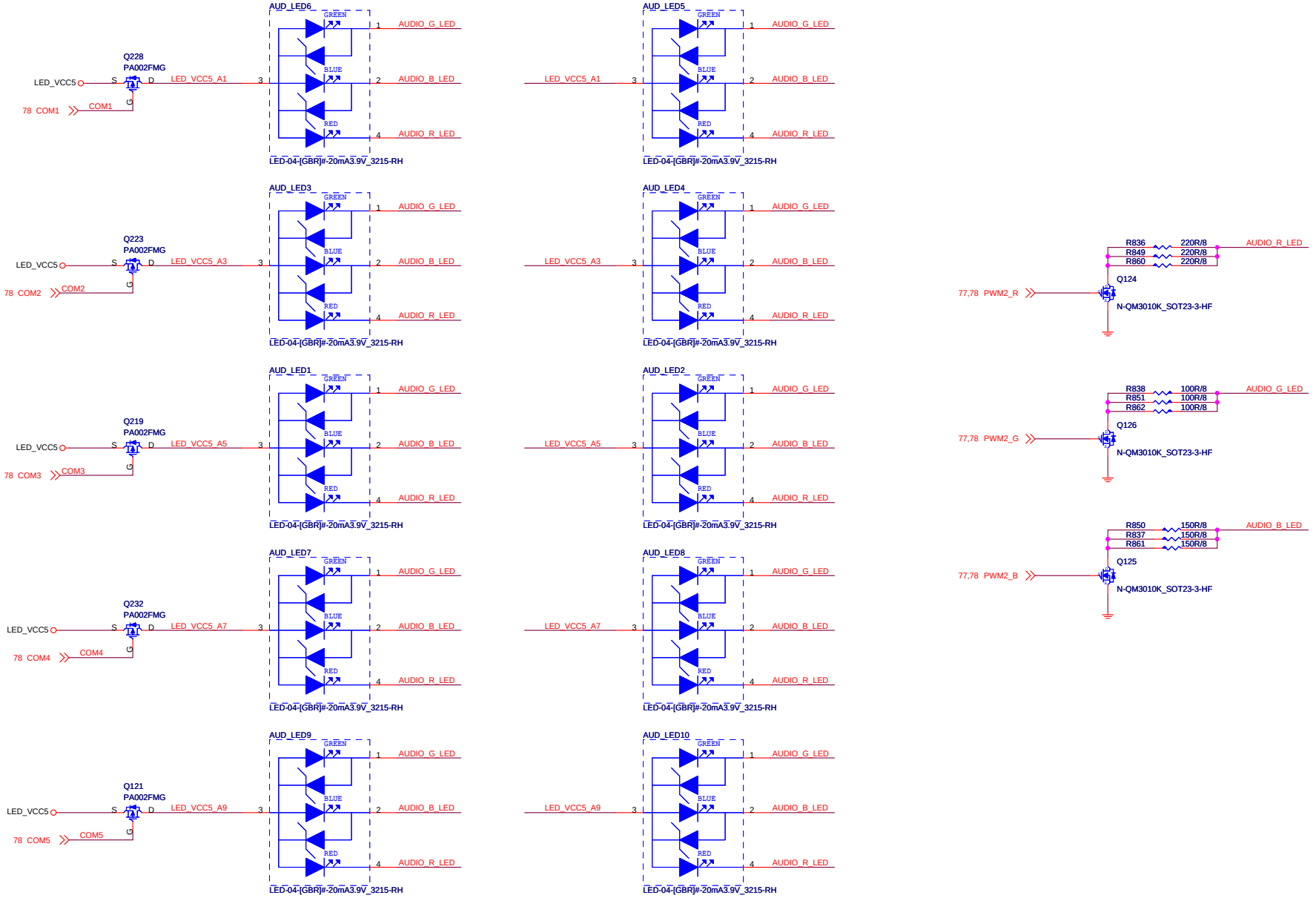
AUDIO_LED



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Intel I219V / I218V PHY

Reserve RL9.RL13 for Schematic Checklists

LAN_DISABLE# must be connected to PCH's LAN_PHY_PWR_CTRL

PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN

The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

RBIAS_LAN <500mil

500mA

L04-47A7870-C08
L04-47A7690-M26

For EMI

UL2&UL3 close to connector

D0G-06A050C-A68
D0G-05A0300-I14

support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.

+3.3V_LAN
I218:132mA
I219:542mW

Note:These caps closed to PHY

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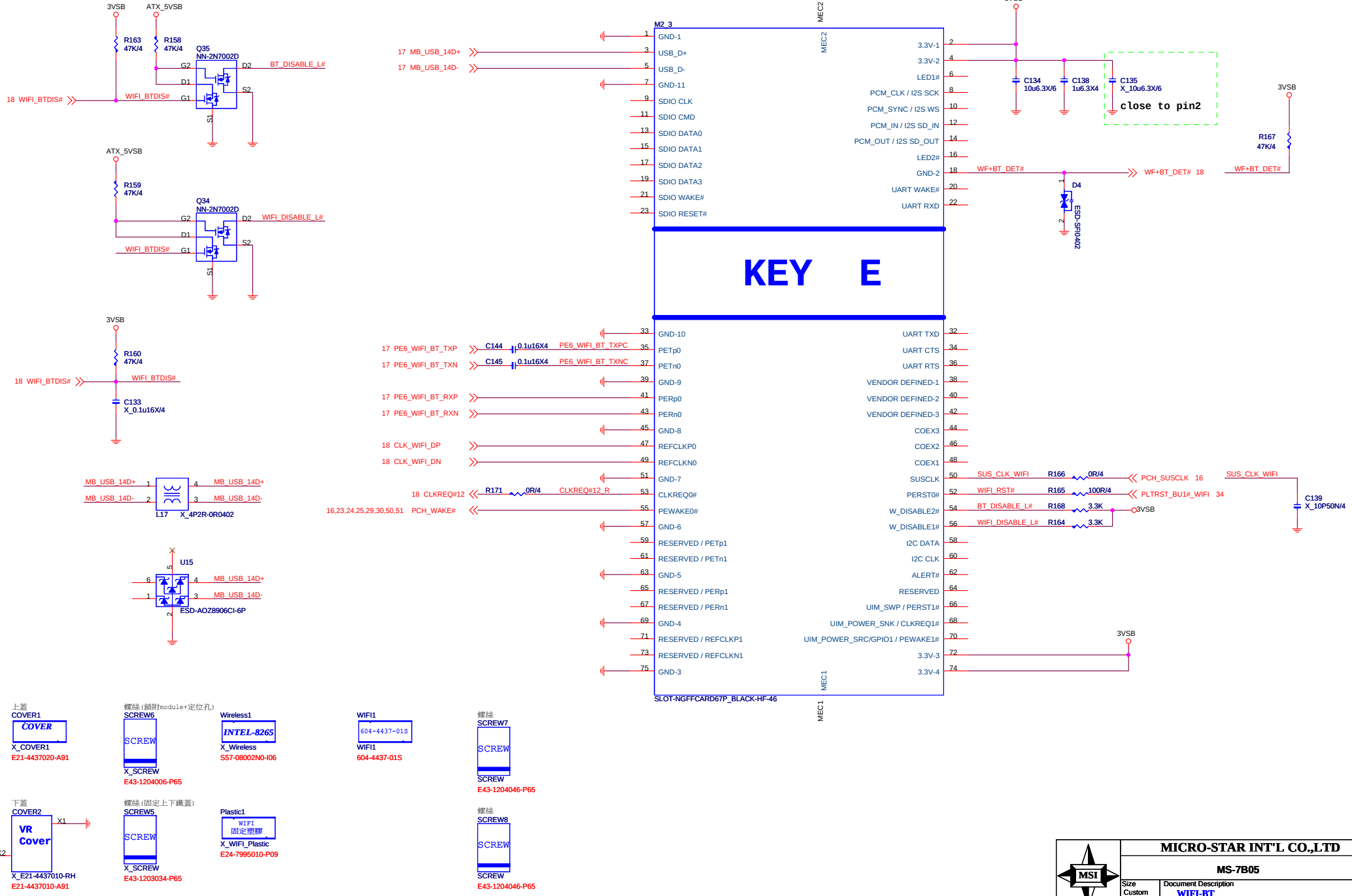
WiFi-BT



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Size: Custom	Document Description: WIFI-BT
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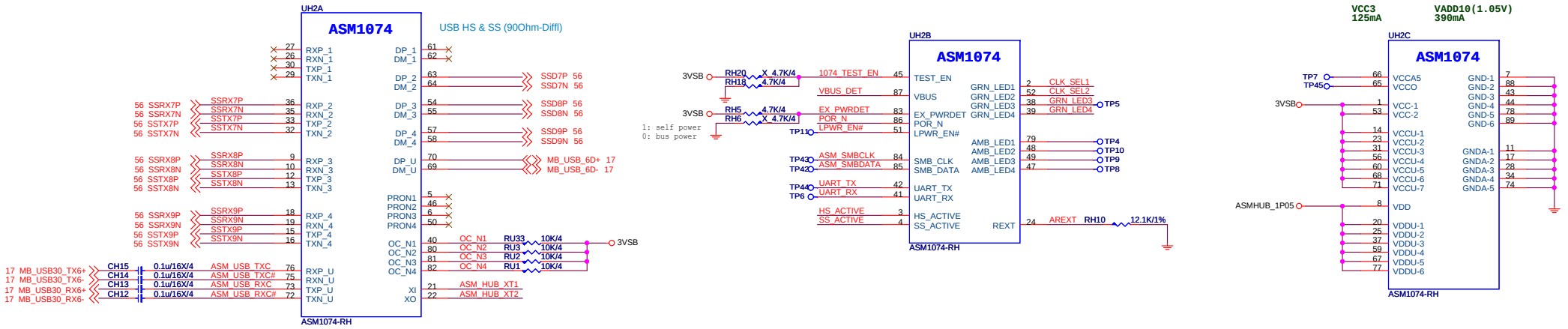

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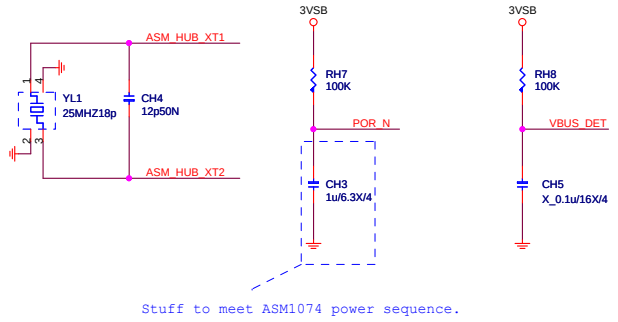
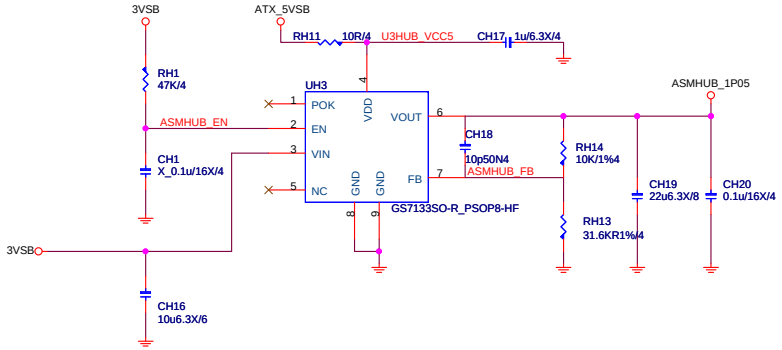
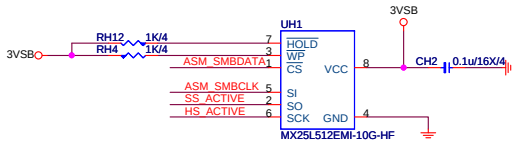
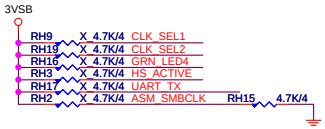


ASM1074 USB3.0 HUB core Power



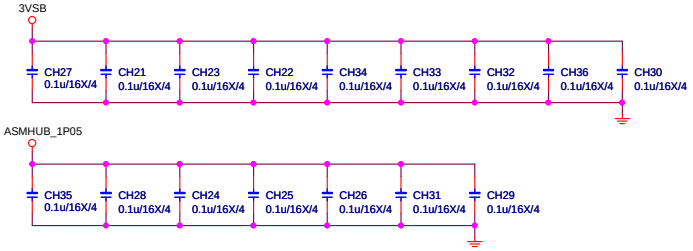


H/W Strapping



Strapping Table

GRN_LED2 (CLK_SEL1)	GRN_LED1 (CLK_SEL0)		
0	0	25MHz	Default
1	0	30MHz	
1	1	20MHz	



MICRO-STAR INT'L CO.,LTD

MS-7B05

Size	Document Description	Rev
Custom	ASM1074 USB3.0 HUB	11

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Layout Guide:

1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

Power Consumption

	3.3V	1.2V(1.05V)	3.3VSUS	1.05VSUS(1.2VSUS)	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP

UU1A ASM2142 — ASM3142-A1-RH

USB SS (80Ohm-Diff)
USB HS (90Ohm-Diff)

18 CLK_ASM1142_2_DP
18 CLK_ASM1142_2_DN
PECLKP
PECLKN
U2DP_A
U2DM_A
SS31_2_DP1 54
SS31_2_DN1 54

17 PE3_ASM1142_2_RXP
17 PE3_ASM1142_2_RXN
CU12 0.22u6.3X4
CU13 0.22u6.3X4
PE3_ASM1142_2_RXP_C
PE3_ASM1142_2_RXN_C
PTX0P
PTX0N
U3TXP_A
U3TXN_A
U3RXP_A
U3RXN_A
SS31_2_TXP1 54
SS31_2_TXN1 54
SS31_2_RXP1 54
SS31_2_RXN1 54

17 PE3_ASM1142_2_TXP
17 PE3_ASM1142_2_TXN
CU10 0.22u6.3X4
CU11 0.22u6.3X4
PE3_ASM1142_2_TXP_C
PE3_ASM1142_2_TXN_C
PRX0P
PRX0N

17 PE4_ASM1142_2_RXP
17 PE4_ASM1142_2_RXN
CU14 0.22u6.3X4
CU15 0.22u6.3X4
PE4_ASM1142_2_RXP_C
PE4_ASM1142_2_RXN_C
PTX1P
PTX1N
U2DP_B
U2DM_B
SS31_2_DP2 54
SS31_2_DN2 54

17 PE4_ASM1142_2_TXP
17 PE4_ASM1142_2_TXN
CU8 0.22u6.3X4
CU9 0.22u6.3X4
PE4_ASM1142_2_TXP_C
PE4_ASM1142_2_TXN_C
PRX1P
PRX1N
U3TXP_B
U3TXN_B
U3RXP_B
U3RXN_B
SS31_2_TXP2 54
SS31_2_TXN2 54
SS31_2_RXP2 54
SS31_2_RXN2 54

34 PLTRST_BU1#_ASM1142_1
PLTRST_BU1# ASM1142_1
ASM1142_WAKE# 2
PE_RST#
PE_WAKE#
PE_CLKREQ#

18 CLKREQ#10
RU6 0R/4

ASM1142_SMI1# 2
SMI#

VCC3
RU38 80.6K1%4
PONRST# 2
PORST#

CU55 1u6.3X6

USB_SPISCK_2
USB_SPICSB_2
USB_SPISI_2
USB_SPISO_2
SPI_CLK
SPI_CS#
SPI_DI
SPI_DO

PRON_A
PRON_B
PPONA_2
PPONB_2
TPU3
TPU5
PPON_X Internal Pull-up to VCC3

OCI_A#
OCI_B#
OCIA_2
OCIB_2
TPU2
TPU1
OCI_X Internal Pull-up to SUS

XI
XO
XI_2
XO_2

UART_RX
UART_TX
TPU11
TPU10
RX/TX Internal Pull-up

USB_SPISCK_2 RU10 4.7K/4 VCC3
RU9 X_4.7K/4

RU4 4.7K/4
TEST_EN
REXT
ASM1142_REXT_2 RU5 12.1K1%4

16,23,24,25,29,30,48,51 PCH_WAKE#
ASM1142_WAKE# 2
U41 ESD-0402-L
QU1 2N7002D
ASM1142_SMI1# 2

3VSB RU14 4.7K/4
18 USB3_SMI2
RU13 4.7K/4 VCC3

ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

UU1B ASM2142 — ASM3142-A1-RH

TPU9 VREGIN
TPU8 LXI
TPU6 VCCHSUS_IN
TPU4 VDDSUS_O
VCCLU-1
VCCHSUS
VDDSUS-1
VDDSUS-2
GND
TPU7 PGND

VCCH-1 VCCH-2 VCC3
VCCLP-1 VCCLP-2 USB3_3VCC_2P5_2
VCCLU-2 VCCLU-3
VDD-1 VDD-2 VDD-3 USB3_1P2_2
VDDP-1 VDDP-2
VDDU-1 VDDU-2 VDDU-3

USB3_3VCC_2P5_2
3VSB
RU37 0R
RU34 X_0R/4 VCCLU_2
USB3_1P2_VSB_2

VCC3
USB3_2P5_2
RU39 X_0R/4
RU40 0R
USB3_3VCC_2P5_2

ASM1142 RU36 stuff RU37 unstuff
ASM2142 RU36 unstuff RU37 stuff

USB3_1P2_2
Close to UU1.58
CU61 10u6.3X6

USB3_1P2_VSB_2
Close to UU1.21/34
CU49 0.1u/16X/4
CU4 0.1u/16X/4

USB3_1P2_2
Close to UU1.41
CU56 10u6.3X6

USB3_1P2_2
Close to UU1.1/12/33
CU53 0.1u/16X/4
CU60 0.1u/16X/4
CU52 0.1u/16X/4

VCC3
Close to UU1.4/32
CU57 0.1u/16X/4
CU51 0.1u/16X/4

USB3_1P2_2
Close to UU1.35/47/52
CU54 2.2u6.3X4
CU59 2.2u6.3X4
CU62 2.2u6.3X4

XO_2
CU7 C12p50N
YU1 20MHZ18p_S-HF
XI_2

3VSB
Close to UU1.20/24
CU3 0.1u/16X/4
CU50 0.1u/16X/4
VCCLU_2

USB3_3VCC_2P5_2
Close to UU1.38/44/55/62
CU58 2.2u6.3X4
CU63 2.2u6.3X4
CU5 2.2u6.3X4
CU6 2.2u6.3X4

UREXT,PEUREXT(W/S) : 10/7
OCIA,OCIB,PPONA,PPONB(W/S) : 5/8
X0/XI (95hm-Diff,Spacing 30mil)

ASM1142 1.2 VCC Power

VCC5
CU71 22u6.3X8
RU45 47K/4
VCC3
UU9 MP2143DJ
VIN SW EN FB PG PGND AGND OUT
U98 1.0u6.3A_1210-HF
USB3_1P2_PH_2
USB3_1P2_2
CU68 22u6.3X8
CU67 22u6.3X8
CU70 0.1u/16X/4
RU43 200KR1%0402
CU69 X_0.1u/16X/4
USB3_1P2_FB_2
RU44 240KR1%0402-HE

ASM1142 RU8/RU9 200K/187K_1.24V
ASM2142/ASM1042AE RU43/RU44 200K/240K_1.1V

ASM1142 1.2 VSB Power

VCC3
CU65 1u6.3X4
UU8 GS7116S_SOT23-5-RH
VDD VOUT EN GND ADJ
USB3_2P5_2
CU66 C47p50N0402-RH-1
RU41 430K1%4
RU42 200KR1%4
CU64 1u6.3X4

ASM1142 unstuff
ASM2142 stuff

3VSB
CU46 1u6.3X4
UU7 GS7116S5-SOT23-5
USB3_1P2_VSB_2
CU48 C47p50N0402-RH-1
RU35 75KR1%4
RU36 200KR1%4
CU47 1u6.3X4

ASM1142 RU33 18K_1.24V
ASM2142/ASM1042AE RU36/RU35 180K/68.1K_1.102V

EEPROM

VCC3
RU12 10K/4
RU11 10K/4
USB_SPICSB_2
USB_SPISO_2
RU8 X_4.7K/4
USB_SPISI_2
USB_SPISCK_2
UU2 MX25L1006EMI-10G
HOLD WP CS SI SO SCK VCC GND
CU16 0.1u/16X/4
RU7 X_4.7K
USB_SPISO_2

ASM1142 UU3 M31-2551222-M24(512K bit)
ASM2142 UU3 M31-2511022-M24(1M bit)

MICRO-STAR INT'L CO.,LTD

MS-7B05

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Custom	USB3.1-ASM2142AE-2	11

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Layout Guide:

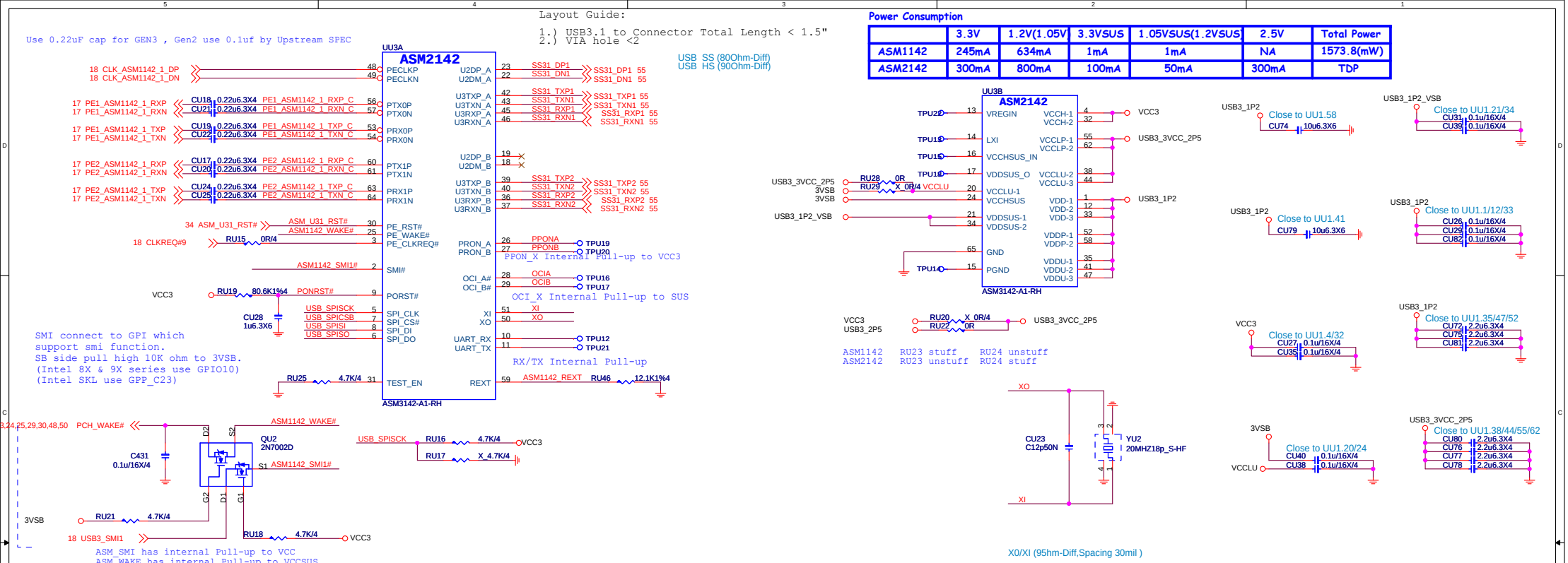
1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

Use 0.22uF cap for GEN3 , Gen2 use 0.1uf by Upstream SPEC

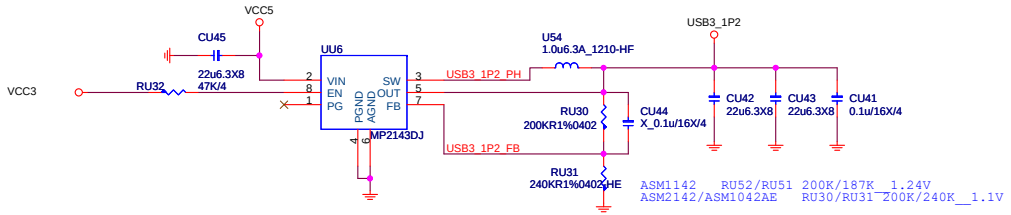
USB SS (80Ohm-Diff)
USB HS (90Ohm-Diff)

Power Consumption

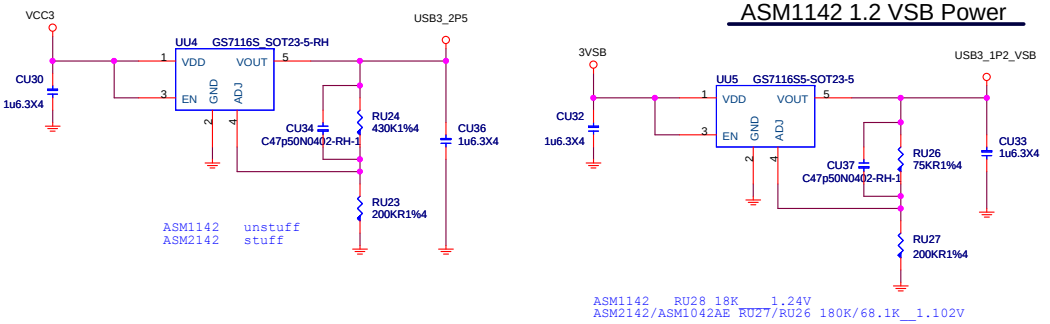
	3.3V	1.2V(1.05V)	3.3VSUS	1.05VSUS(1.2VSUS)	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP



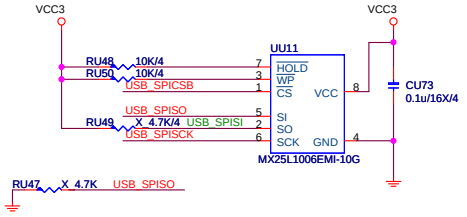
ASM1142 1.2 VCC Power



ASM1142 1.2 VSB Power



EEPROM



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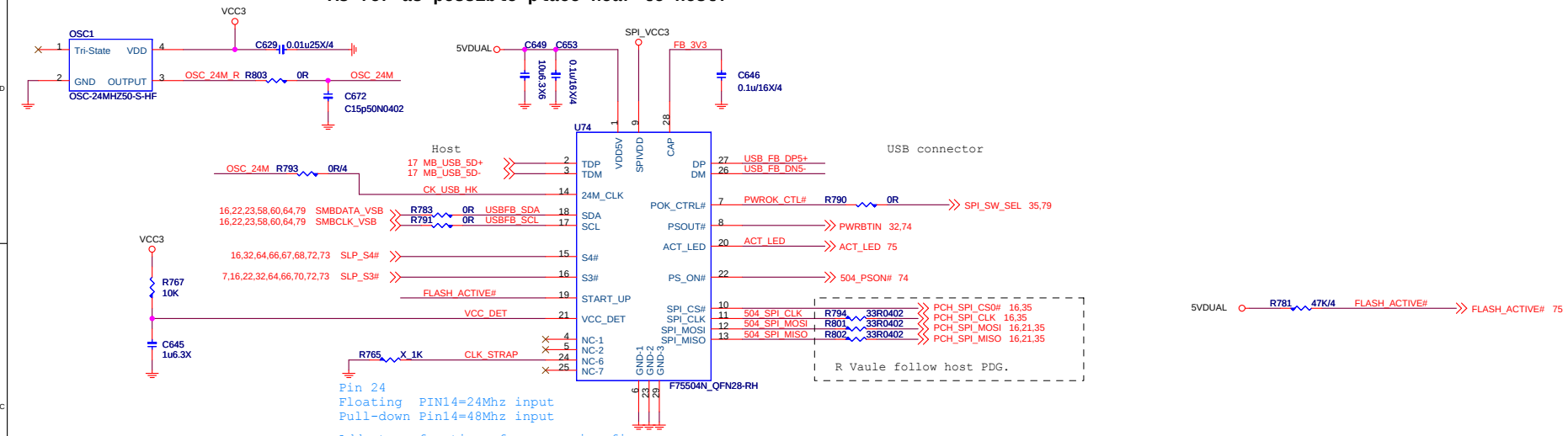
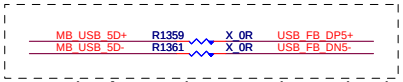
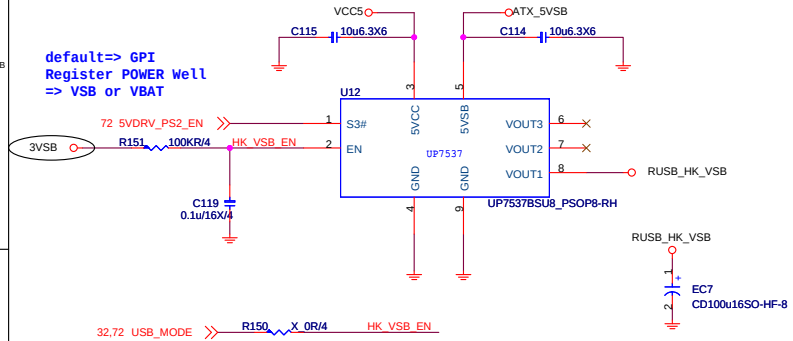
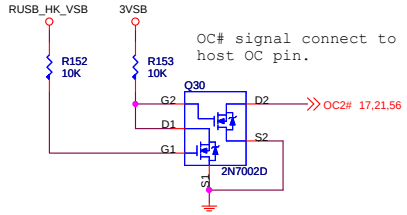
F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.

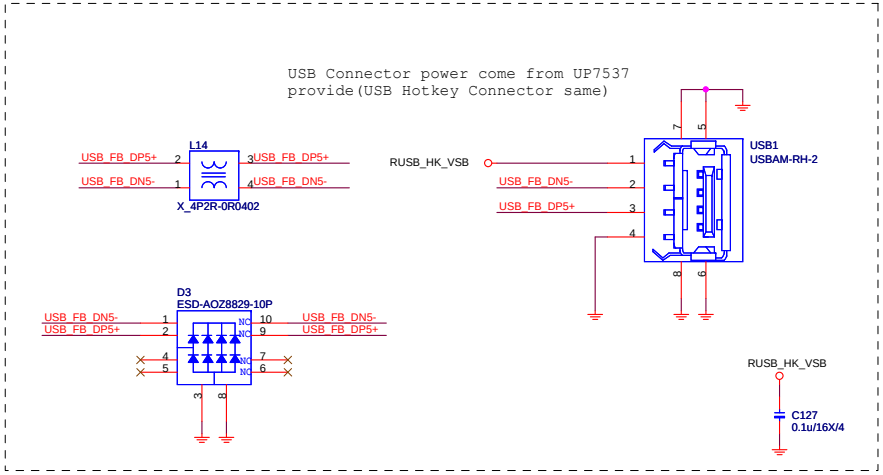




Reserved--place to bottom,stub must be shortest.







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	MS-7B05	
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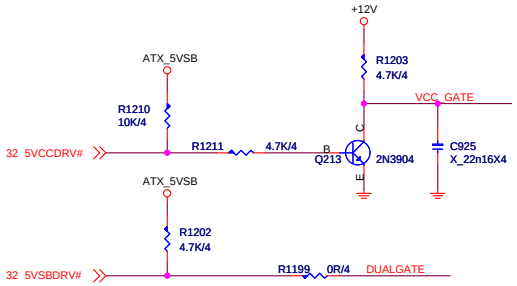
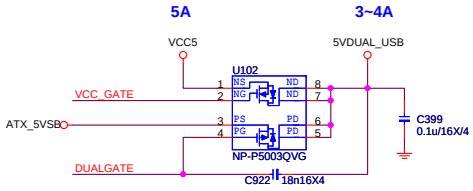
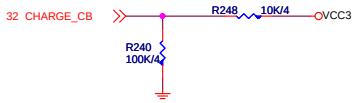
5VDUAL_USB

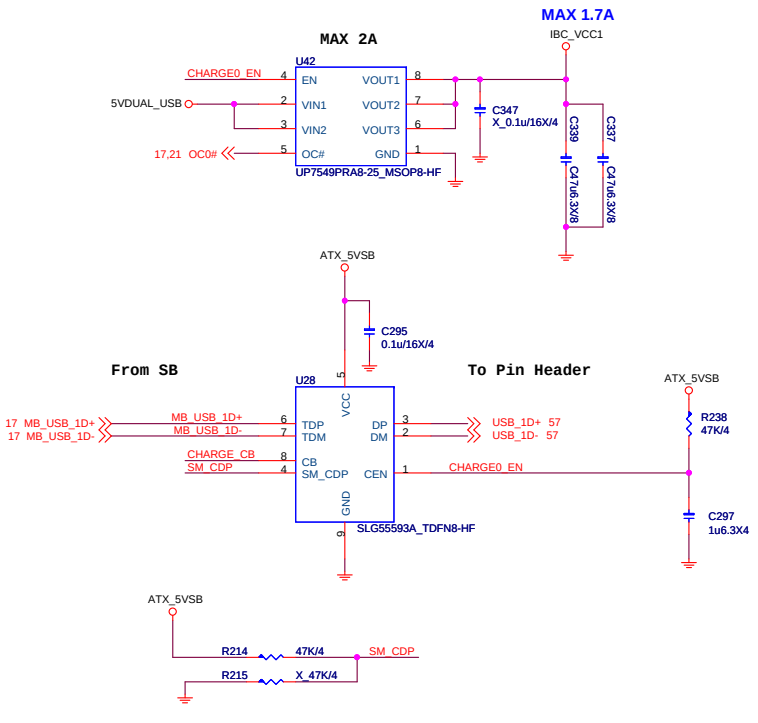




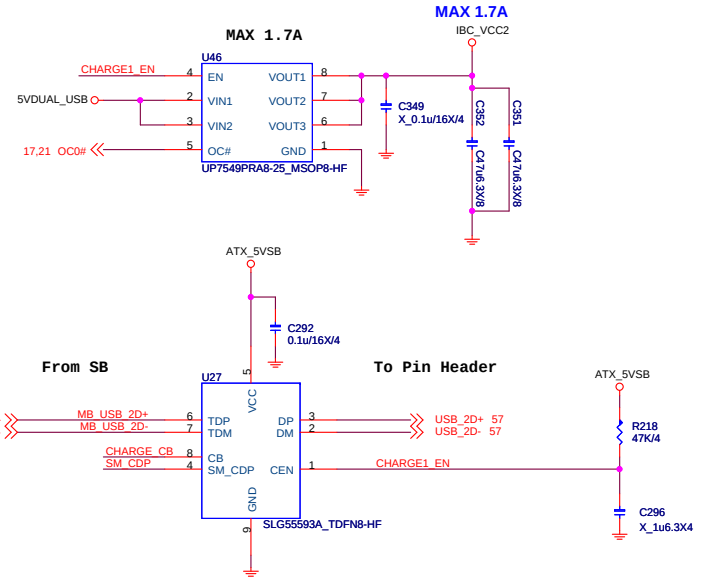
Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB



USB POWER PORT 0 For USB Charging



USB POWER PORT 1 For USB Charging



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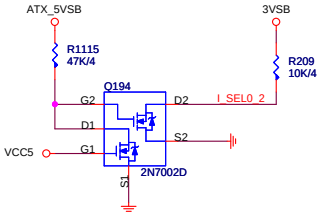
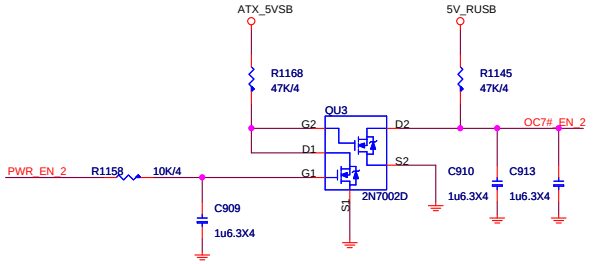
Current Mode

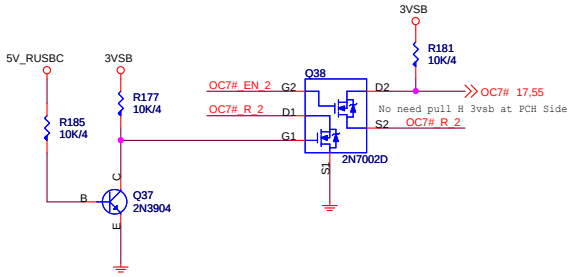


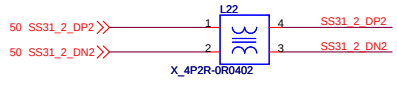
0	X	Default for 900mA
1	0	1.5A @5V
1	1	3A @5V

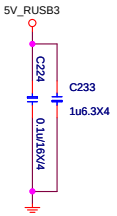
1.5A under S3 mode
3A under S0 mode

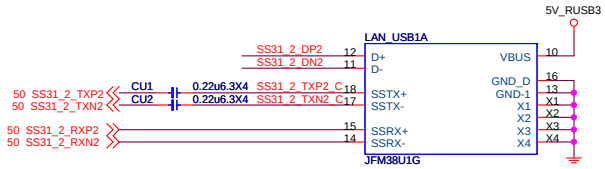
VBUS OC#

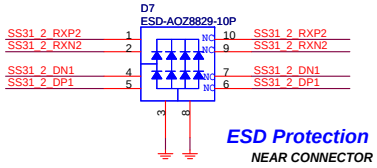






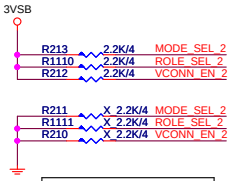






ESD Protection
NEAR CONNECTOR

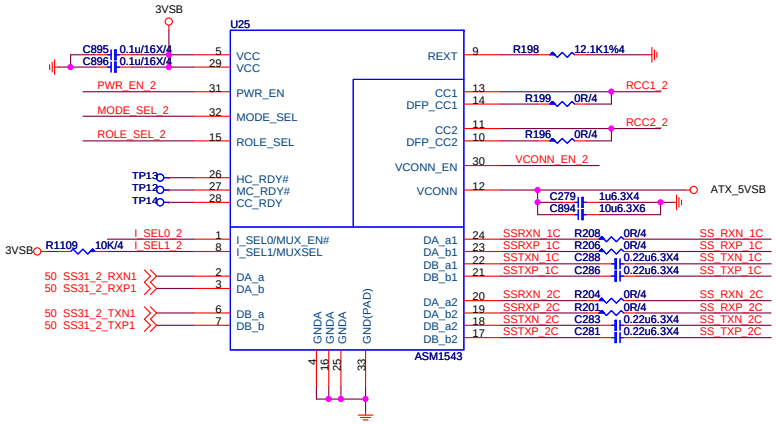
USB Type-C MUX with Configuration Channel (CC)

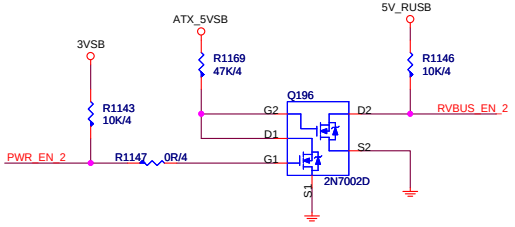


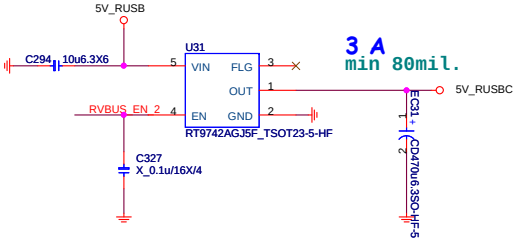
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

VCONN_EN	
1	enable
0	disable

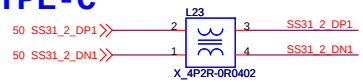


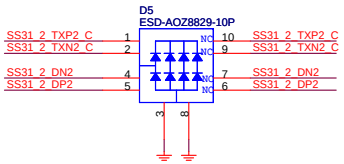




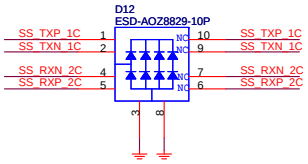
3 A
min 80mil.

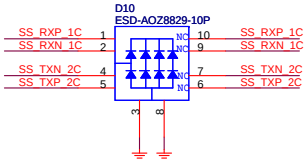
TYPE-C

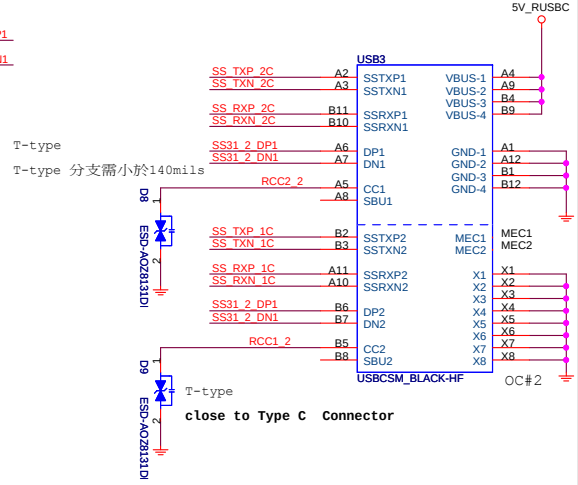


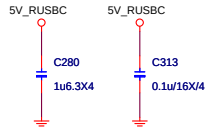


ESD Protection
NEAR CONNECTOR









USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-005 AVL

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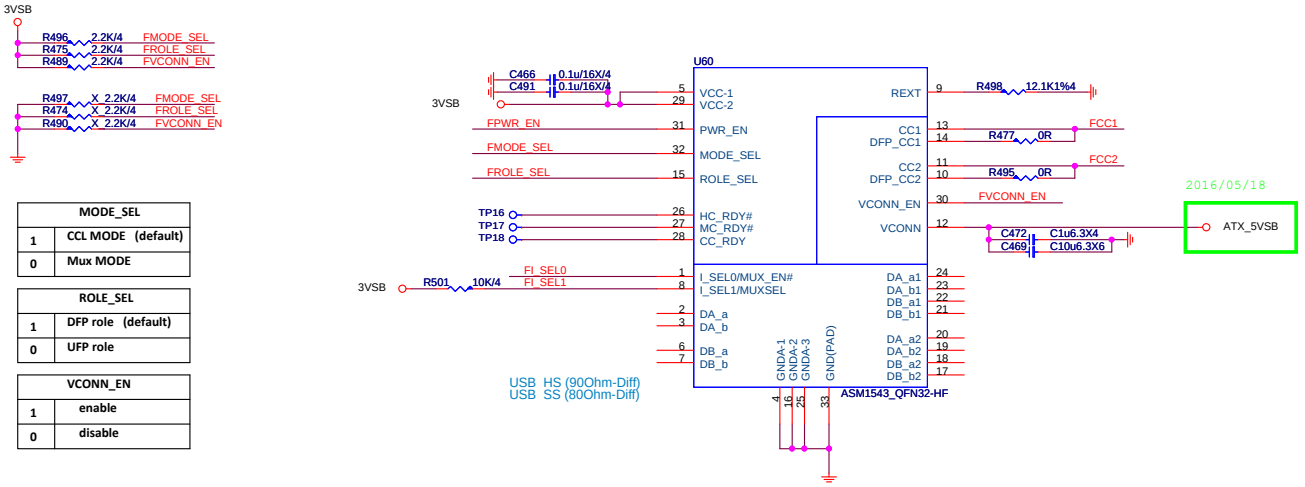
USB 3.1-Type-C

USB Type-C MUX with Configuration Channel (CC)

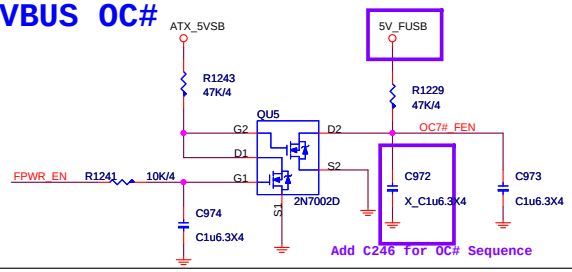


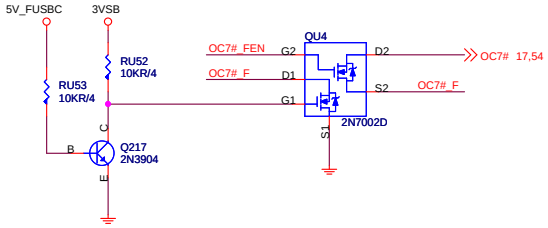
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

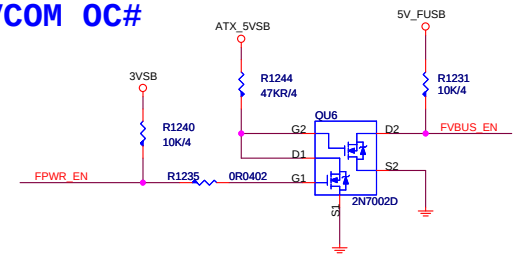
VCONN_EN	
1	enable
0	disable

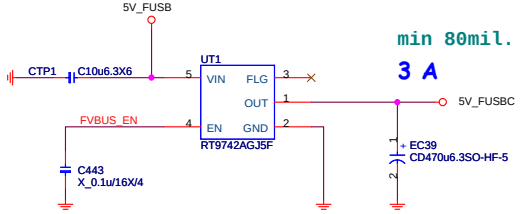
VBUS OC#





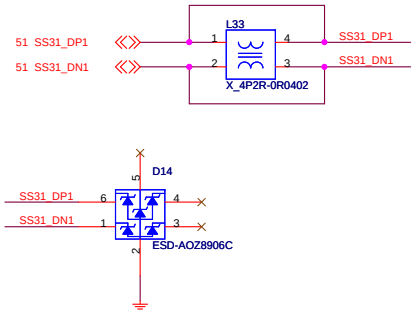
VCOM OC#

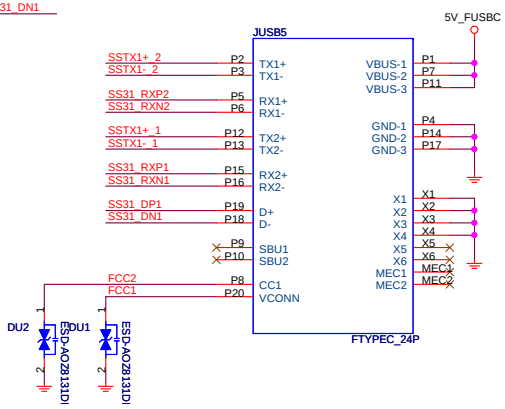




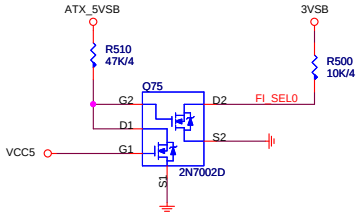
min 80mil.

3 A





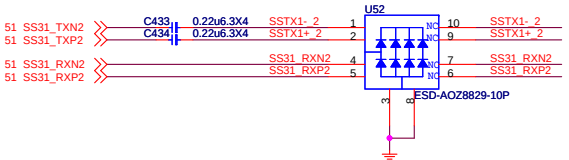
Current Mode

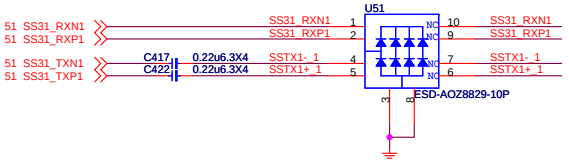


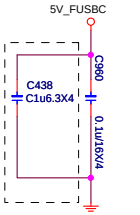
I_SEL0 : I_SEL1

X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

1.5A under S3 mode
3A under S0 mode







MICRO-STAR INT'L CO.,LTD

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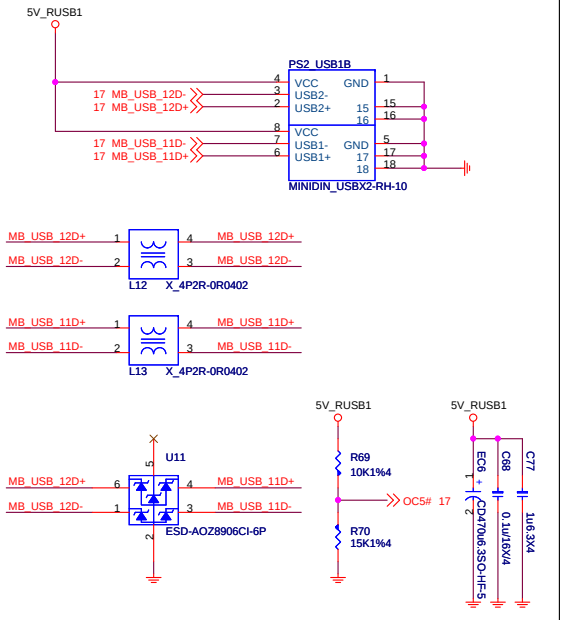
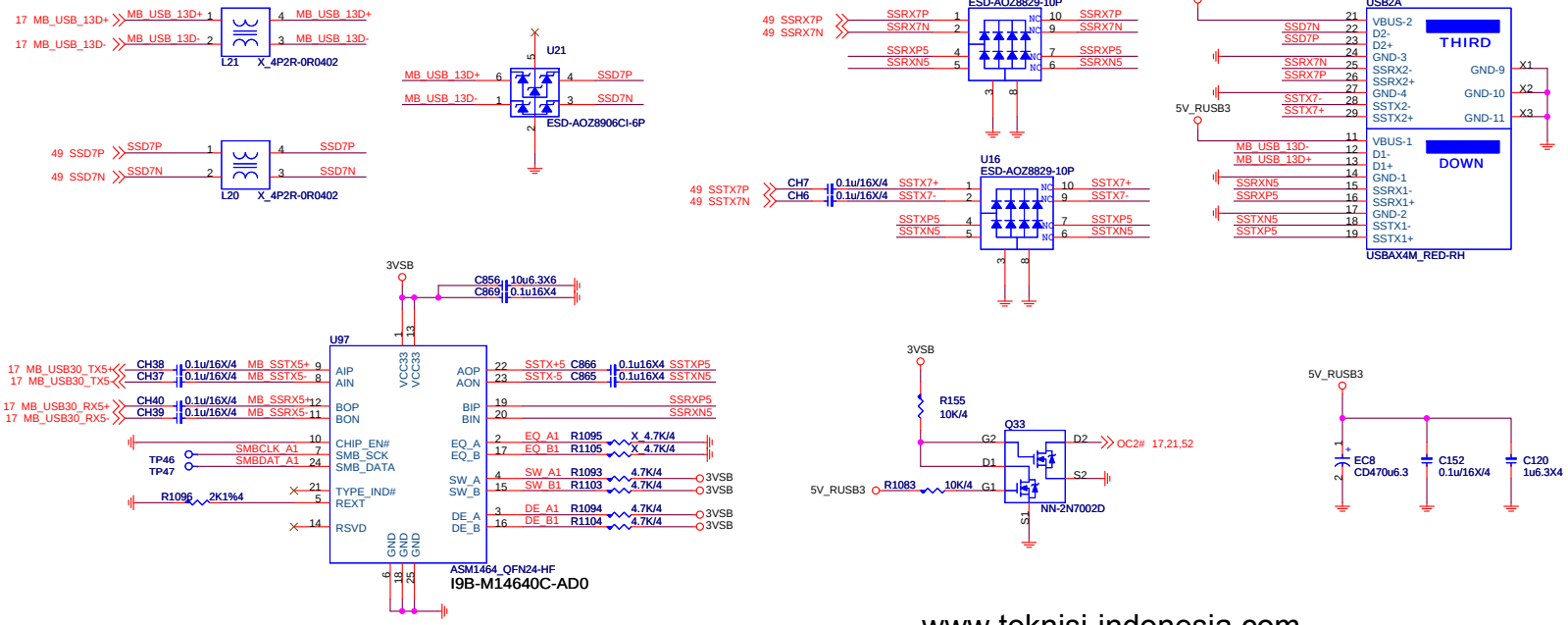
PS2_USB1



USB3_1 (ASM1074)



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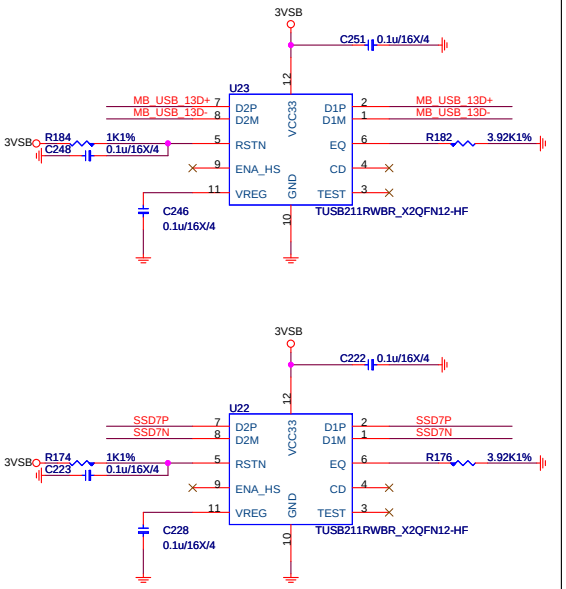

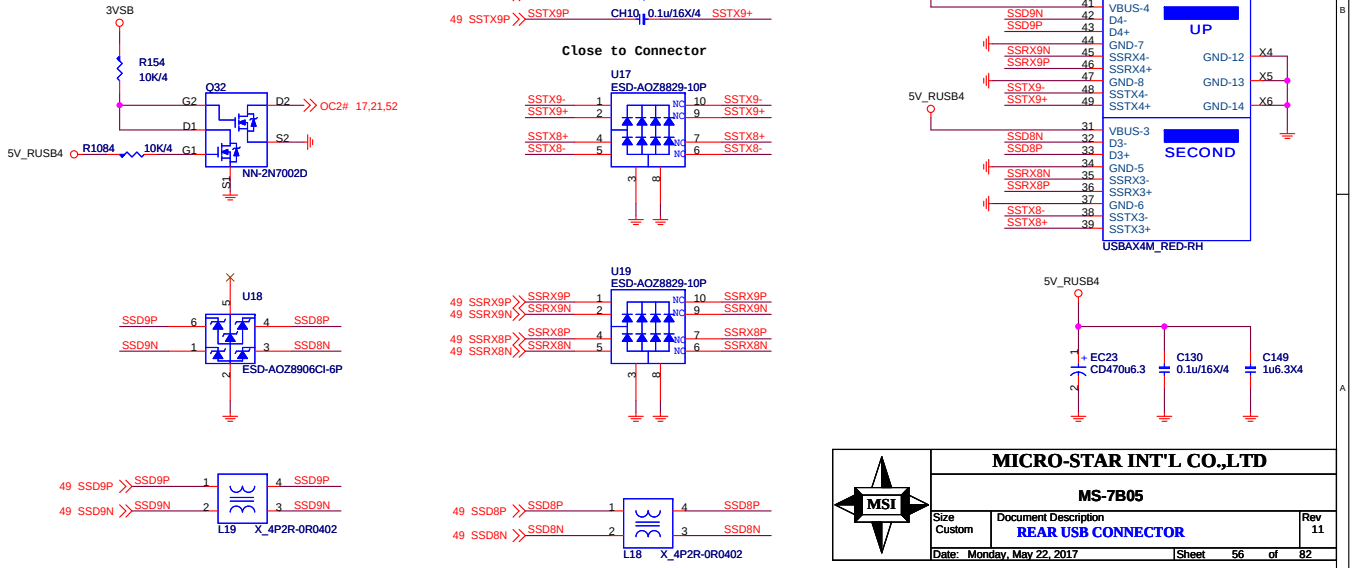

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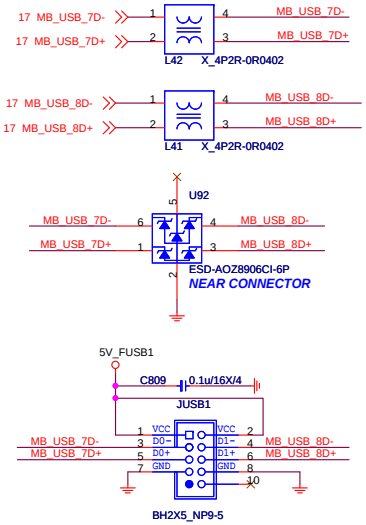
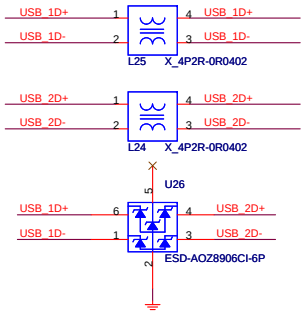
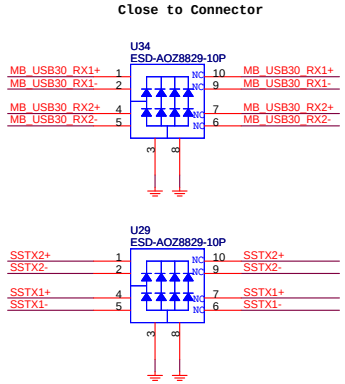
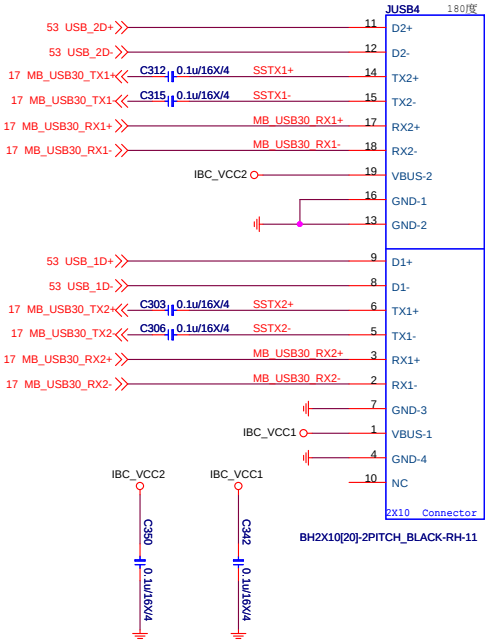
FRONT USB PORT 7,8

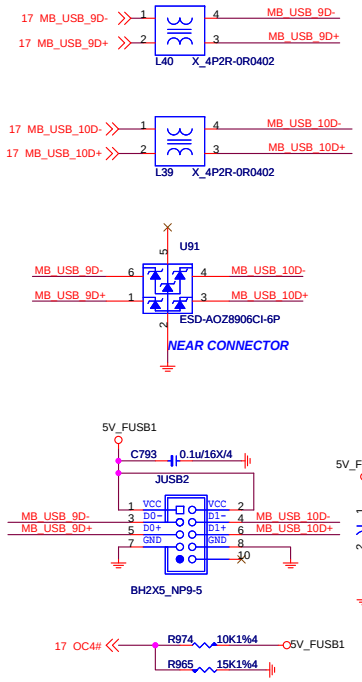


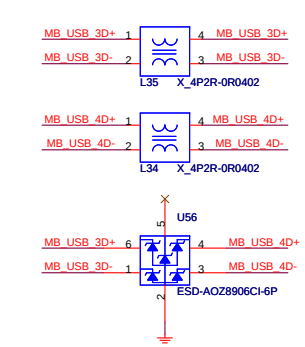


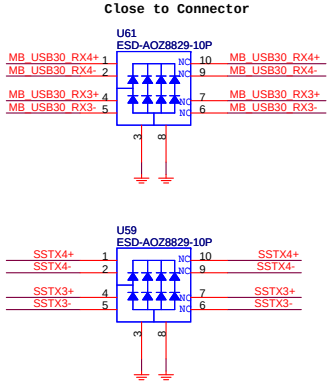


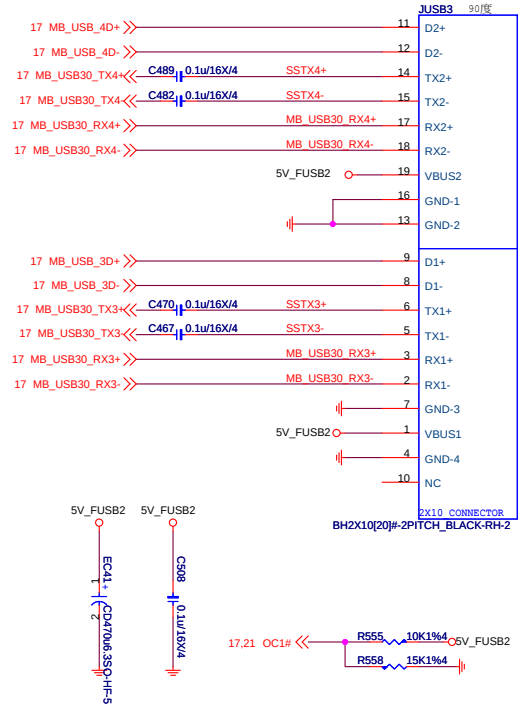


FRONT USB PORT 9.10









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	MS-7B05	
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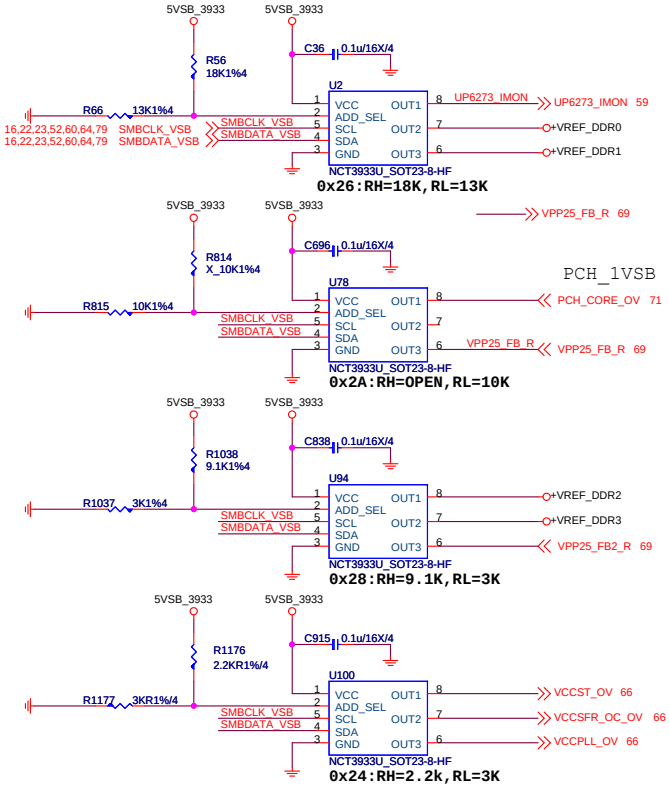
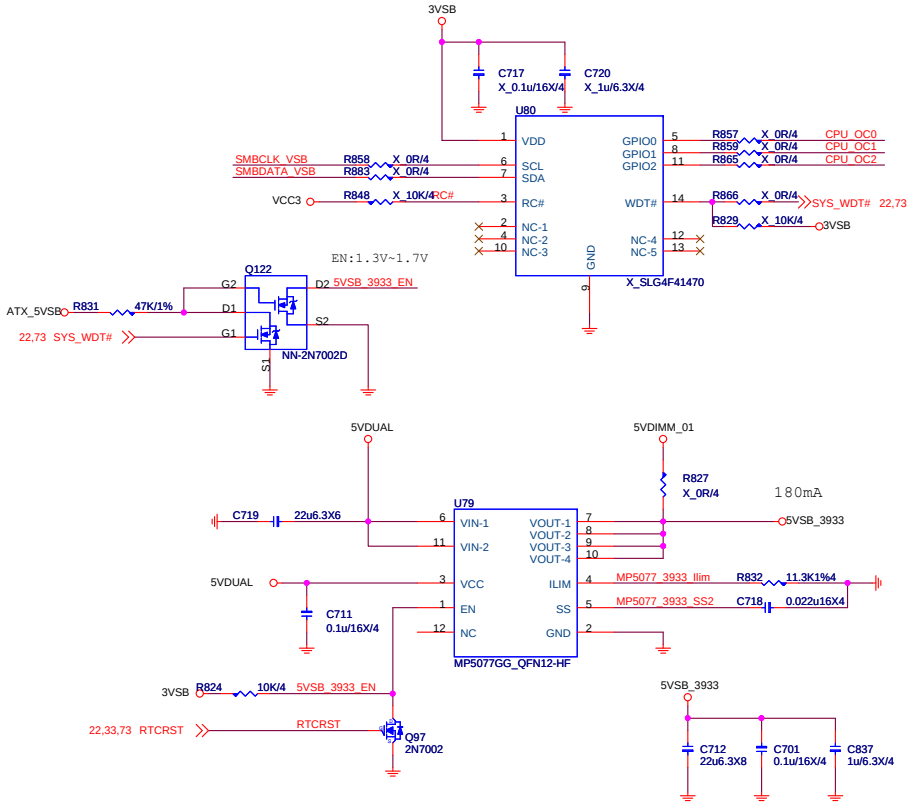
UPI VOLTAGE CONSOLE

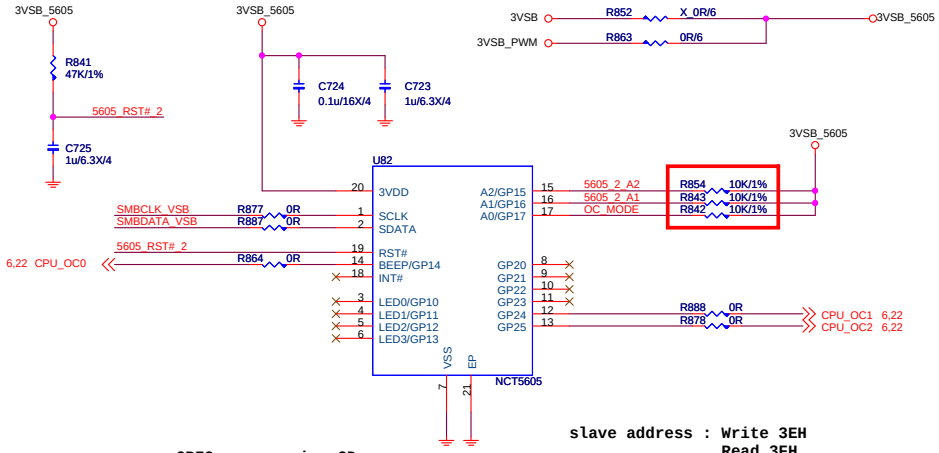


VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.2	3	3.9	OPEN
BUS_SEL	0%	25%	42%	58%	75%	100%



RSVD FOR OC



GPIO programming OD

slave address : Write 3EH
Read 3FH

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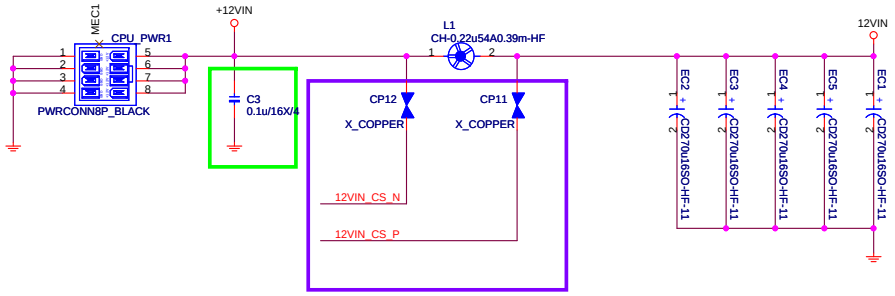
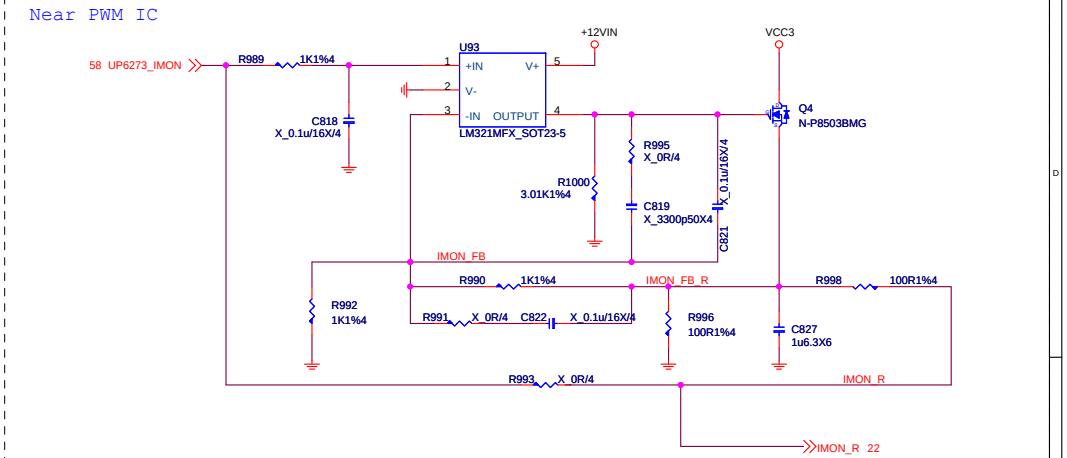
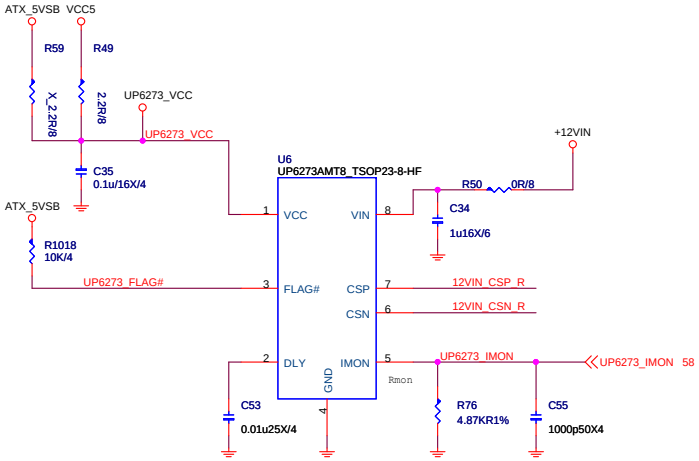


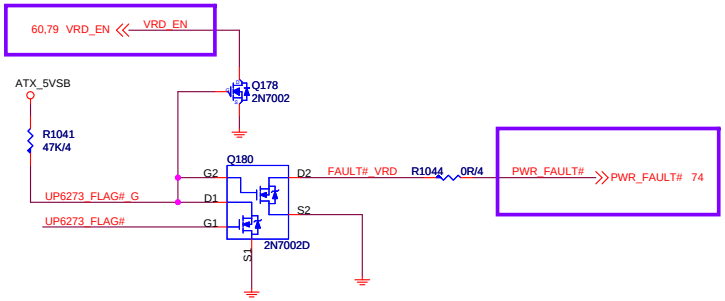


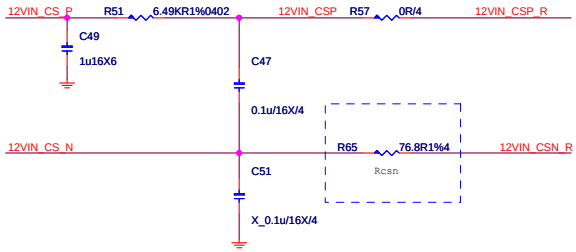


一階2A
Rimon5.23Kohm
Rcsn0.082Kohm
DCR0.39mohm
Vimon1.2V
Iocp48.2423885A

Iin=(Vmon*Rcsn)/(Rmon*Rdc)
Vmon=1.2
can change OCP trigger level by Rcsn and Rmon
Iin=(Vmon*Rcsn)/(Rmon*Rdc)
Vmon=1.2
=(1.2*82)/(5.23*0.39)
=98.4/2.0397
=48.24

OCP 50A
DCR*Iocp/Rcsn=1.2/5.1K
0.39m*50A/Rcsn=1.2/5.1K
Rcsn=82.8R





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VRMPWRGD LEVEL SHIFT

Vcore: ICC Max 100A
LL: 1.0 mohm
OCP: 400A

VSA: ICC Max 15A
OCP: 25A

PROC_ID1	Sequence	CPU TYPE
1	VCCIO->VCCIN->VCCSA	SKX-X (VR13)
0	VCCIO->VCCSA->VCCIN	KBL-X(IMVP8)

Close IC

Close IC

RT6 close to Choke

Close to MOSFET

Close to PWM

Diff pair

7B05 Add PWM6,7,8

0x26:RH=18K,RL=13K

		VR53	VR54	VC20	VR58	VR57	VR59	VR60
Default	Temp	6.49k	10k	100p	X	0R	X	0R
	VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

IR35201_R4
SMB Address: 0X70

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Size: Custom | Document Description: CPU PWR-IR35201 | Rev: 11

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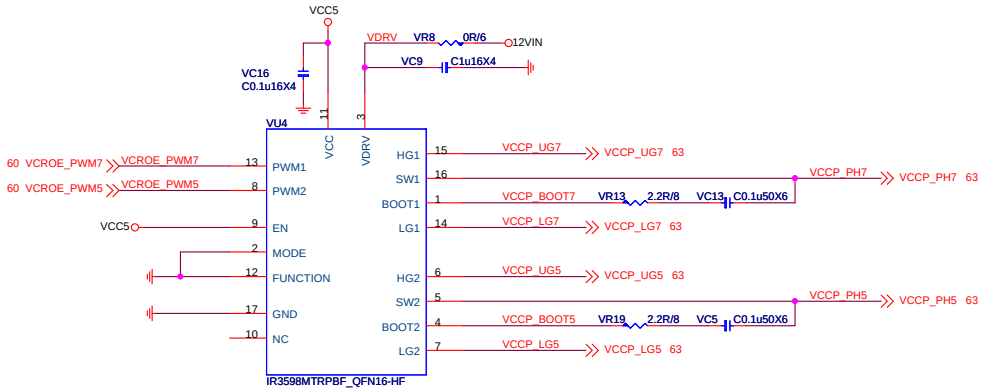

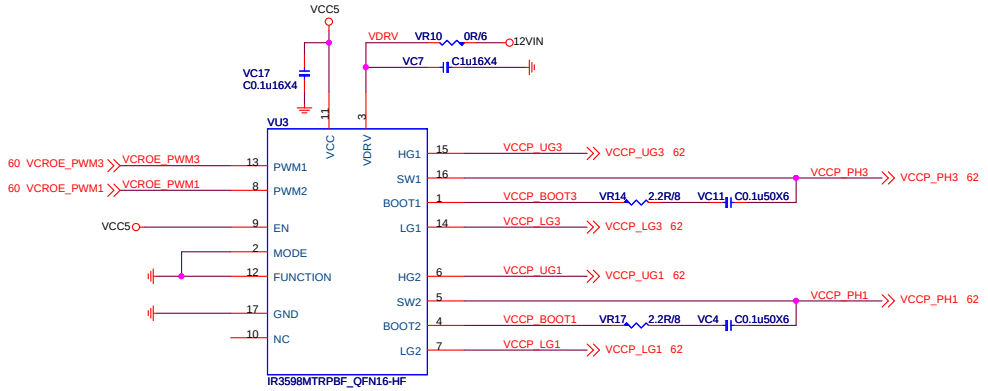

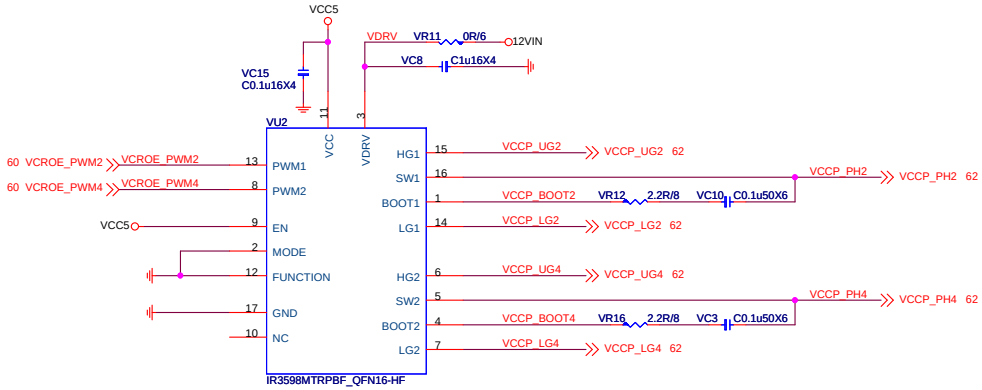

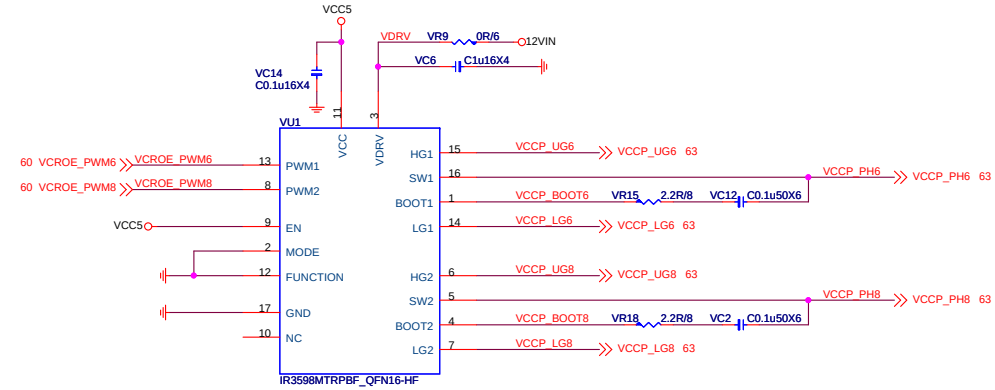

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU PWR-IR3598	11

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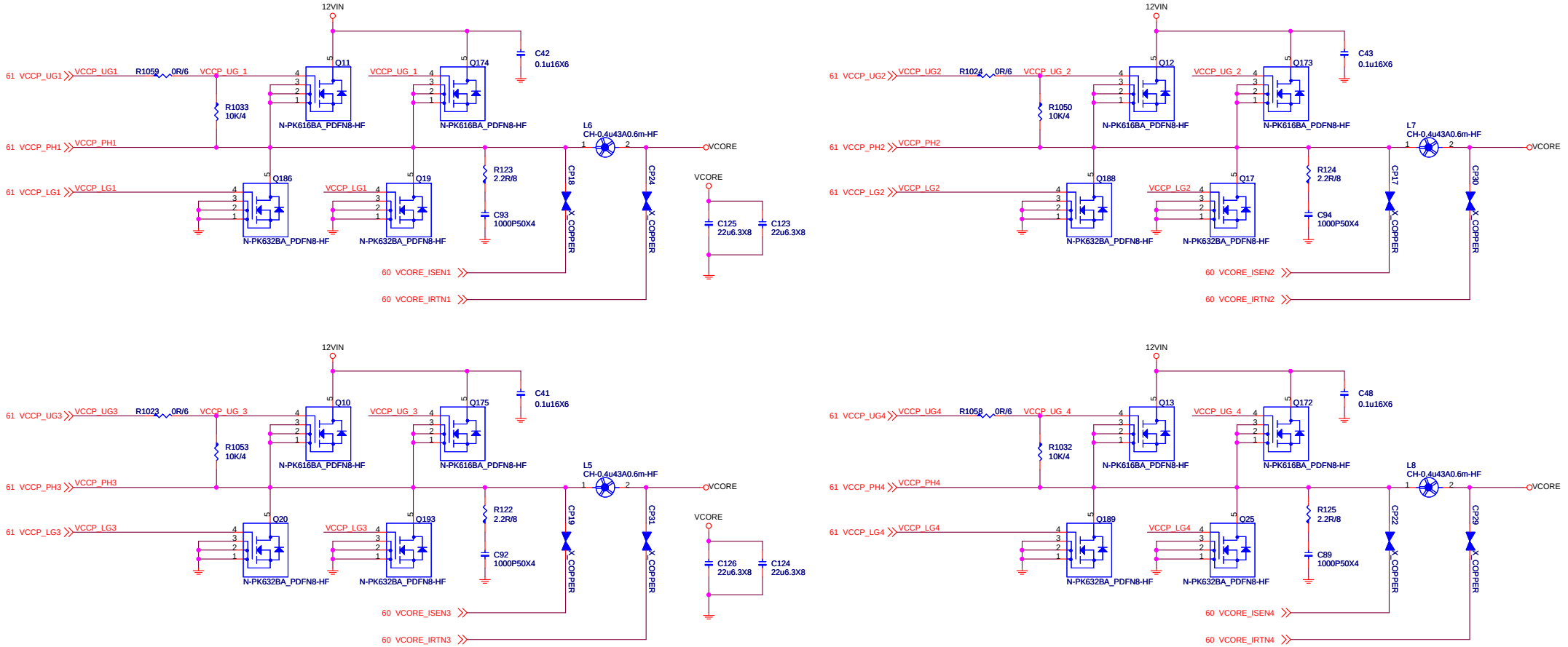

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU PWR-CORE-PH1~4	11

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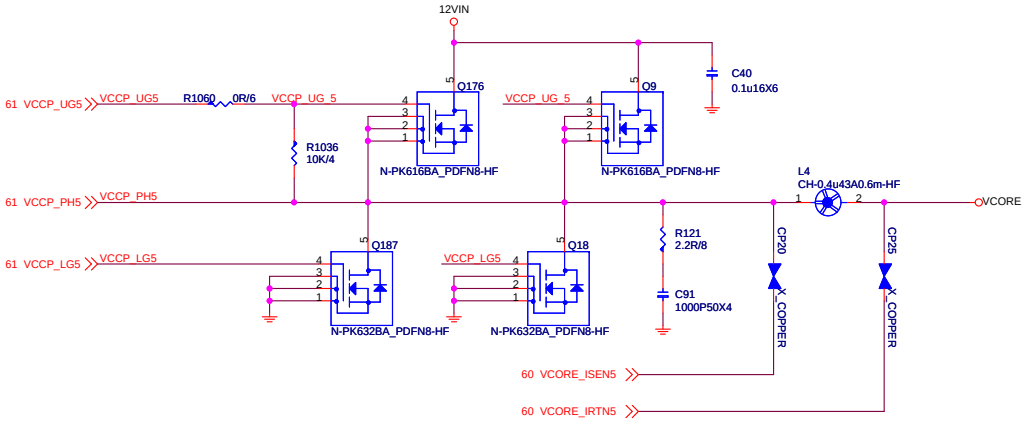

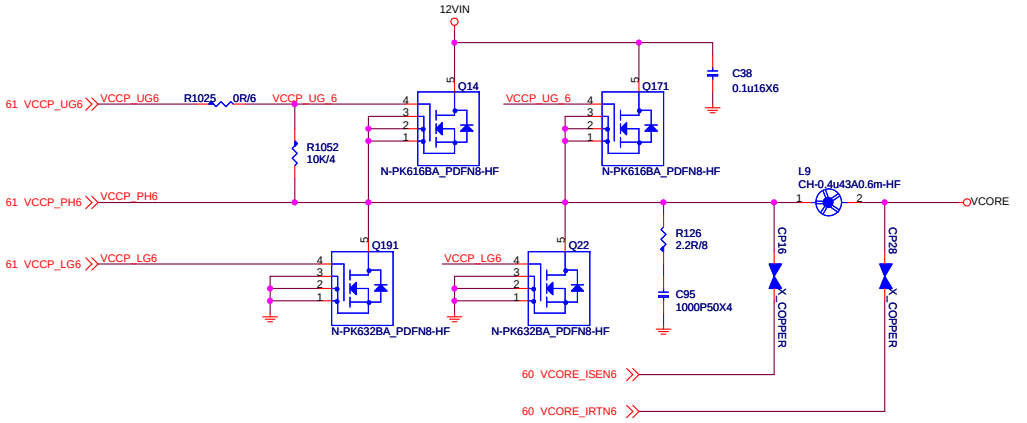

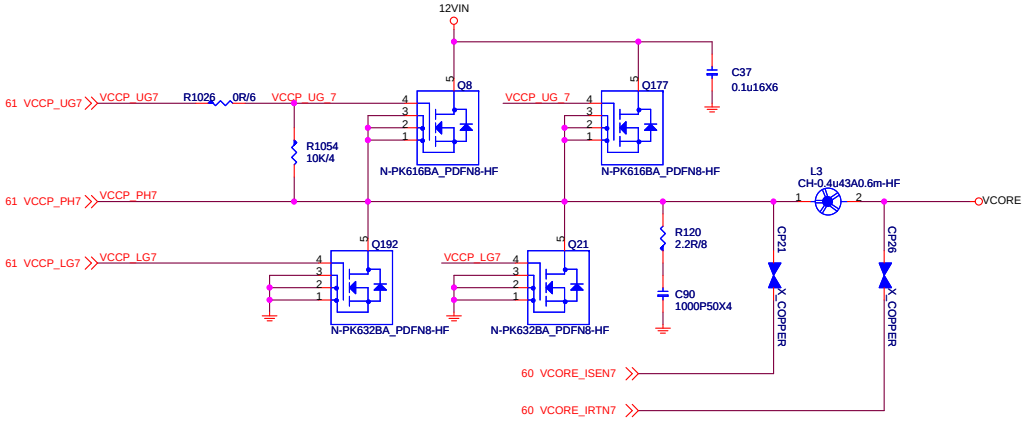

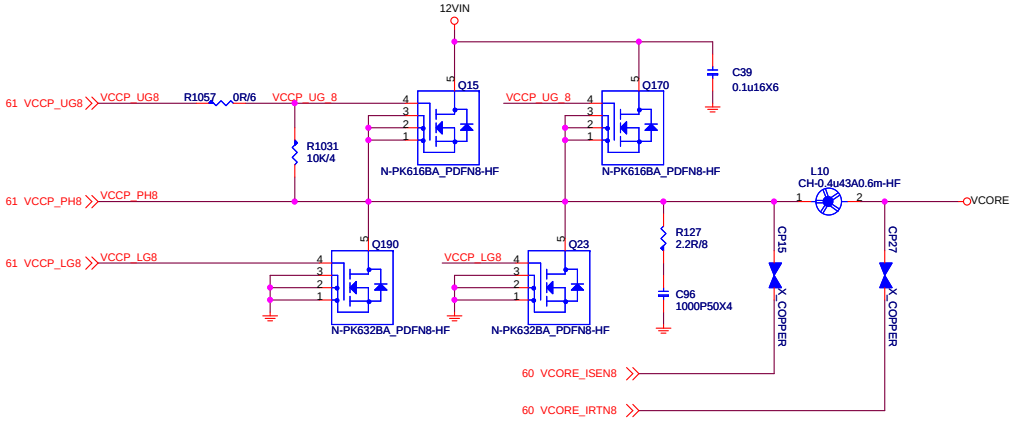

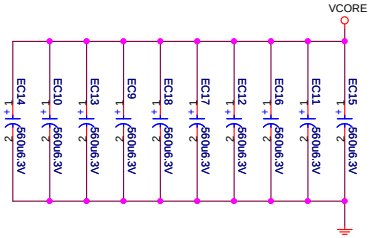

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7B05	
Size: Custom	Document Description: CPU PWR-CORE-PH5~8	Rev: 11
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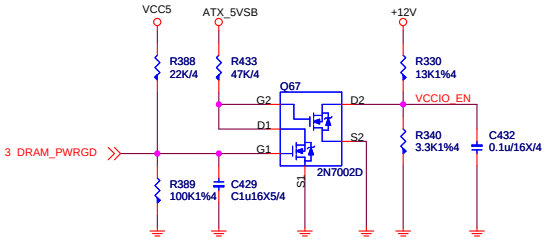
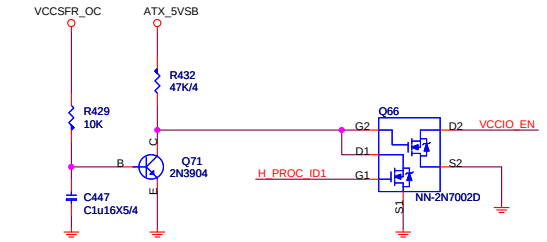
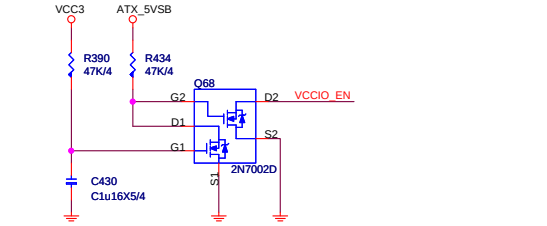
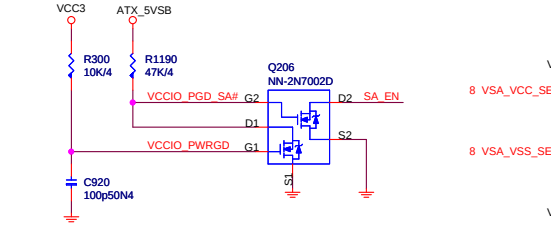
VCCIOPWRGD LEVEL SHIFT

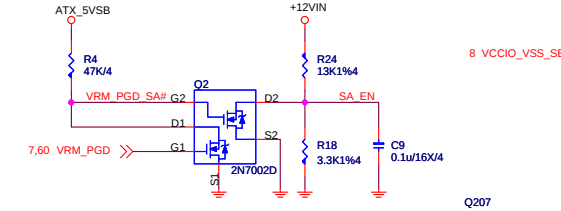


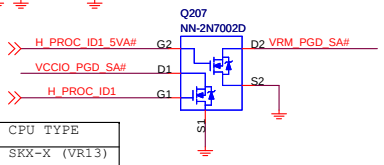
RSVD For KBL-X VCCIO Sequence



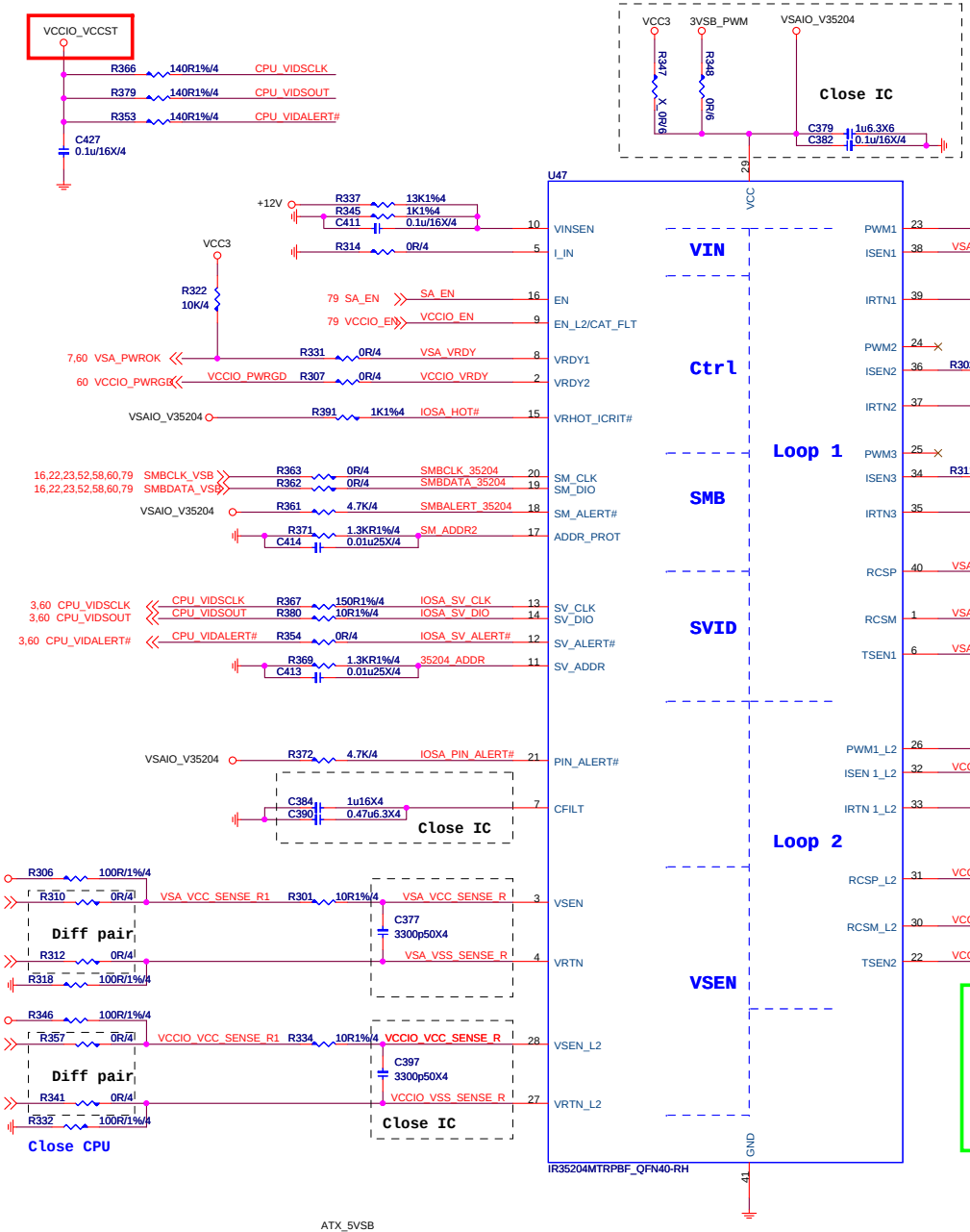








PROC_ID1	Sequence	CPU TYPE
1	VCCIO->VCCIN->VCCSA	SKX-X (VR13)
0	VCCIO->VCCSA->VCCIN	KBL-X(IMVP8)



CPU ID CFG

PROC_ID1	PROC_ID0	CPU TYPE
0	0	future CPU(IMVP9)
0	1	KBL-X(IMVP8)
1	0	future CPU
1	1	SKX-X (VR13)

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Custom	VR13_VSA/VCCIO IR35204	11

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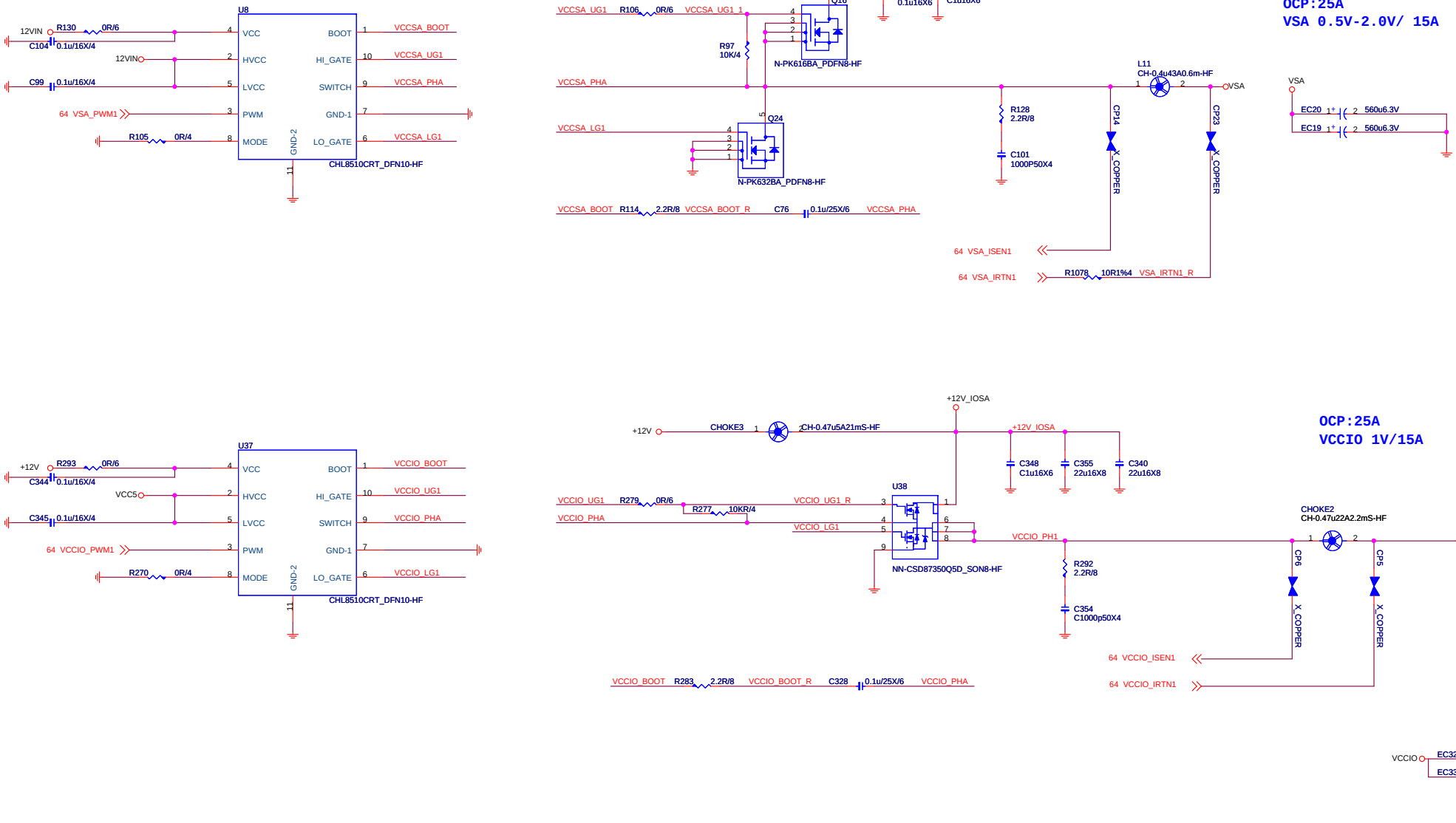

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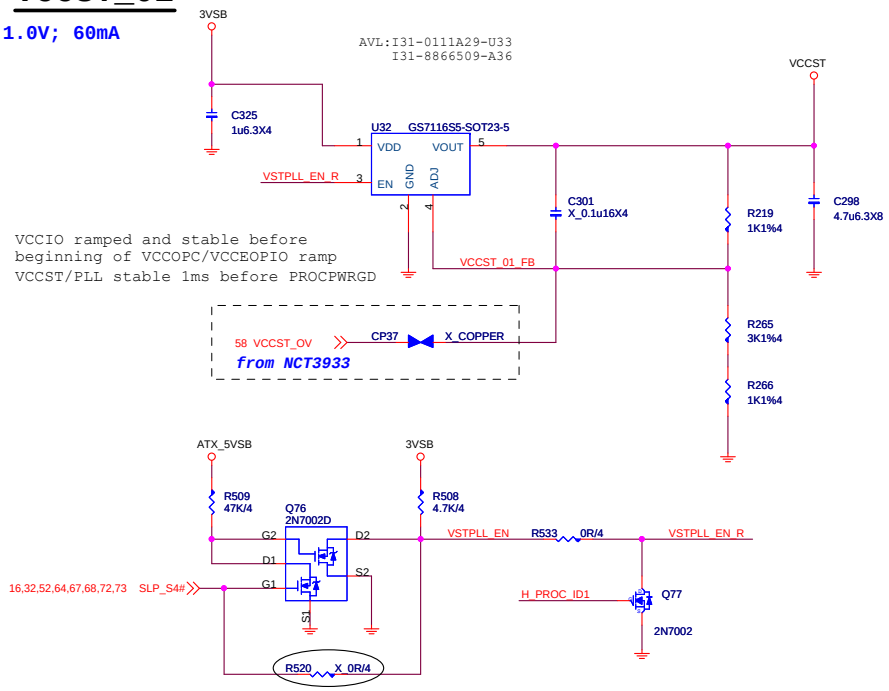
VCCST_01

1.0V; 60mA



VCCST_23

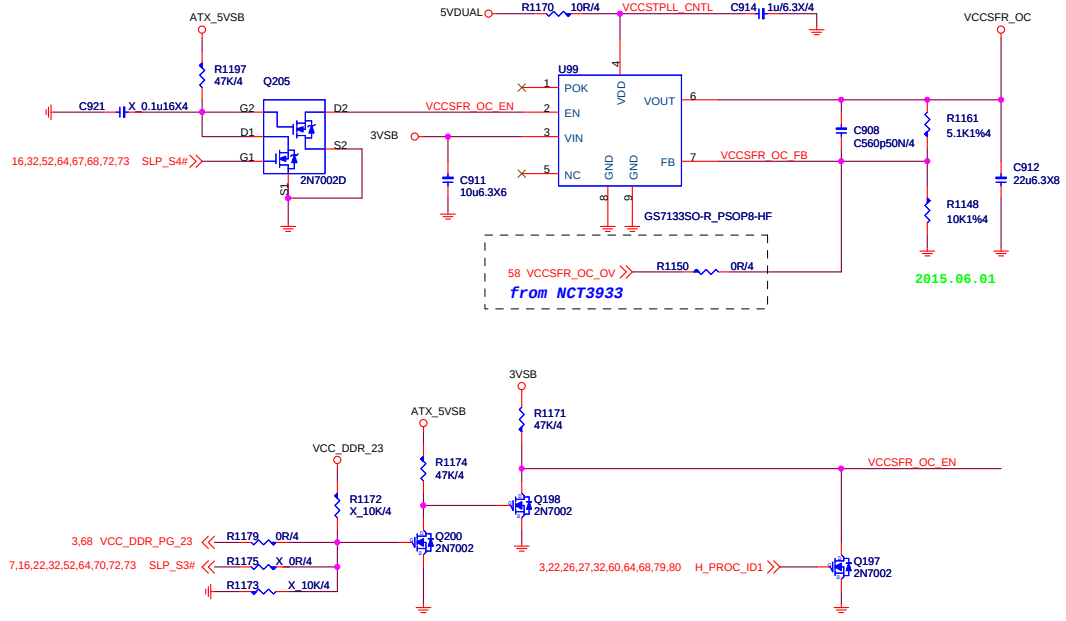
1.0V; 60mA

For non-OC system, configures +VCCSFR_OC as 1.2V

VCCSFR_OC

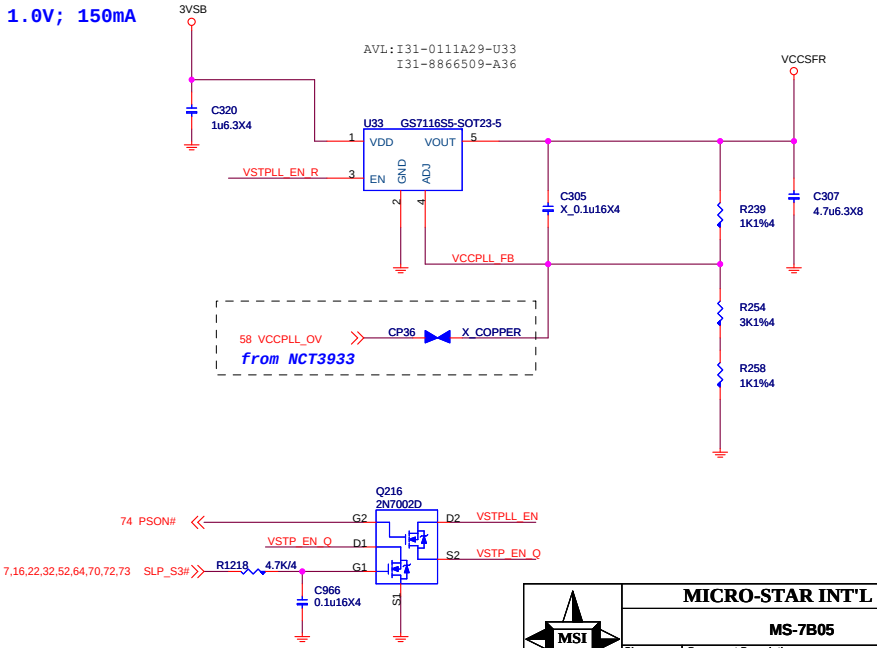
1.1V~1.5A; 500mA

EN:VIH1.2V
EN pin Maximum:VIN+0.3V



VCCSFR

1.0V; 150mA



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Size: Custom	Document Description: CPU VCCST/VCCSFR/VCCSFR_OC	Rev: 11
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DDR Power1-PV4210-2-Phase

DDR4 1.2V nominal,

0.8V-2.5V Max ,44.14A / OCP 50A

Iin ripple =5.2A

VCCIO_VCCST

R335 140R1%/4 DDR_VIDSCLK 3,68

R343 140R1%/4 DDR_VIDSOUT 3,68

R355 140R1%/4 DDR_VIDALERT# 3,68

C416 0.1u/16X/4

5VDIMM_01 — CHOKE4 — CH-0.47u22A2.2mS-HF — 5VDIMM_IN1 — 5VDIMM_IN1

C373 0.1u/16X/4

EC37 560u6.3V

EC35 560u6.3V

C365 0.1u/16X/4

VDD33D C394 0.1u/16X/4

VDD33A C396 0.1u/16X/4

V3201 C392 0.22u6.3X4

C393 0.22u6.3X4

C391 0.01u25X/4

3VSB_PWM

R315 0R/6 VDD33D

R316 1R/6 VDD33A

V3201

C395 0.1u/16X/4

U49

VDD33D
VDD33A
1V8
VDD5V
VR_ENABLE
VR_CLK
VR_DATA
VR_ALRT#
VR_HOT#
VR_READY
PIN_ALRT#
SCL
SDA
CONFIG
VBOOT
TSENP
TSENN
SYNC
IIN
DGND
AGND
VINSEN
DMD1
DMD2
PWM1
ISEN1P
ISEN1N
PWM2
ISEN2P
ISEN2N
VSENP
VSENN
VCOMP

PV4210

R317 10K/4 5VDIMM_IN1

R321 1K/4

C398 0.1u/16X/4

TP59 TP60

VR_DDR_EN1_R

DDR1_PWM1

DDR1_PWM2

3,68 DDR_VIDSCLK — R336 150R1%/4 — DDR01_SV_CLK

3,68 DDR_VIDSOUT — R344 10R1%/4 — DDR01_SV_DIO

3,68 DDR_VIDALERT# — R356 0R/4 — DDR01_SV_ALERT#

3VSB_PWM — R382 10K/4 — DDRVR1_HOT#

3 VCC_DDR_PG_01

3VSB_PWM — R325 1K/4 — DDR1_PINALERT#

16,31,34,68,78,79 SMBCLK_VCC — R402 0R/4 — DDR1_CLK

16,31,34,68,78,79 SMBDATA_VCC — R411 0R/4 — DDR1_DATA

R412 147KR1%4 DDR1_CFG

R1204 X_10K/4

TSENP1

TSENN1

TP58

ISEN1P_DDR1 R342 1K/4 ISEN1P_DDR1_R

ISEN1N_DDR1 R349 1K/4 ISEN1N_DDR1_R

ISEN2P_DDR1 R360 1K/4 ISEN2P_DDR1_R

ISEN2N_DDR1 R370 1K/4 ISEN2N_DDR1_R

C383 0.01u25X/4

DDR1_VSENP R326 0R/4 CP35

DDR1_VSENN CP34

DDR1_VCOMP

C400 100p50N4

close to DIMM side

X_COPPER X_COPPER VCC_DDR_01

3VSB_PWM

Q44 2N3904

TSENP1

C428 100p50N4

TSENN1

R394 1K/4

VCC_DDR_PG_01

Q49 NN-2N7002D

3VSB R364 47K/4 — G2 D1 G1 S1 D2 S2 — MEM_HOT_C01_N — MEM_HOT_C01_N 3,10,11

DDRVR1_HOT#

Q48 NN-2N7002D

3VSB R333 47K/4 — MEM_HOT_C01_N

DDR1_PINALERT#

ATX_5VSB

R385 47K/4

+VPP25_C01

R393 X_47K/4

Q56 X_NN-2N7002D

C421 X_0.01u25X/4

16,32,52,64,66,68,72,73 SLP_S4#

VR_DDR_EN1_R

D34 S-LRB520S-40T1G-HF

H_PROC_ID1_5VA

32,68 SIO_VDDQ_EN — R381 47K/4 — VR_DDR_EN1_R

3,69,79 H_PROC_ID1_5VA — H_PROC_ID1_5VA

5VDIMM_IN1

DDR1_UG1 R303 0R/6 DDR1_UG1_R

DDR1_PH1A R305 10KR/4 DDR1_LG1

U44

NN-CSD87350Q5D_SON8-HF

C358 C1u16X6

C364 C10u16X8

L28 CH-0.22u40A2.4mS-RH

DDR1_PH1

VCC_DDR_01

R338 2.2R/8

C402 C1000p50X4

CP10 X_COPPER

CP9 X_COPPER

DDR1_BOOT1 R274 2.2R/8 DDR1_BOOT1_R C332 0.1u/25X/6 DDR1_PH1A

ISEN1P_DDR1_R

R1180 412R1%4

C410 0.22u6.3X4

ISEN1N_DDR1_R

R1181 0R/4

5VDIMM_IN1

DDR1_UG2 R288 0R/6 DDR1_UG2_R

DDR1_PH2A R287 10KR/4 DDR1_LG2

U40

NN-CSD87350Q5D_SON8-HF

C378 C1u16X6

C403 C10u16X8

L26 CH-0.22u40A2.4mS-RH

DDR1_PH2

VCC_DDR_01

R299 2.2R/8

C363 C1000p50X4

CP8 X_COPPER

CP7 X_COPPER

DDR1_BOOT2 R273 2.2R/8 DDR1_BOOT2_R C338 0.1u/25X/6 DDR1_PH2A

ISEN2P_DDR1_R

R1168 412R1%4

C415 0.22u6.3X4

ISEN2N_DDR1_R

R1165 0R/4

R403 X_10K/4 DDR1_CFG

U35

DDR1_BOOT2 — BOOT — UGATE — DDR1_UG2

DDR1_PWM2 — PWM — PHASE — DDR1_PH2A

OD# — GND — DDR1_LG2

5VDIMM_01 R252 0R/6 UP1959_VCC2_R — VCC — LGATE

C311 0.1u/16X/4

C308 10u6.3X6

GND

UP1959

U36

DDR1_BOOT1 — BOOT — UGATE — DDR1_UG1

DDR1_PWM1 — PWM — PHASE — DDR1_PH1A

OD# — GND — DDR1_LG1

5VDIMM_01 R253 0R/6 UP1959_VCC1_R — VCC — LGATE

C309 0.1u/16X/4

C310 10u6.3X6

GND

UP1959

VCC_DDR_01

EC29 560u6.3V

EC36 560u6.3V

EC26 560u6.3V

EC38 560u6.3V

EC34 560u6.3V

MICRO-STAR INT'L CO.,LTD

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Custom	VR13_VCCDDR01 PV4201-2 phase	11

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DDR Power1-PV4210-2-Phase

DDR4 1.2V nominal,
0.8V-2.5V Max ,44.14A / OCP 50A

Iin ripple =5.2A

5VDIMM_23 → CHOKE1 → CH-0.47u22A2.2mS-HF → 5VDIMM_IN2 → 5VDIMM_IN2

C116 0.1u/16X/4
EC21 560u6.3V
EC22 560u6.3V
C131 0.1u/16X/4

VDD33D_2 C80 0.1u/16X/4
VDD33A_2 C85 0.1u/16X/4
V4201_2 C70 0.22u6.3X4
C79 0.22u6.3X4
C69 0.01u25X/4

C84 0.1u/16X/4

3VSB_PWM

R113 0R/6 VDD33D_2
R117 1R/6 VDD33A_2
V4201_2

VR_DDR_EN2_R

3,67 DDR_VIDSCLK R104 150R1%/4 DDR23_SV_CLK
3,67 DDR_VIDSOUT R103 10R1%/4 DDR23_SV_DIO
3,67 DDR_VIDALERT# R102 0R/4 DDR23_SV_ALERT#

3VSB_PWM R101 10K/4 DDRVR2_HOT#

3,66 VCC_DDR_PG_23

3VSB_PWM R1065 1K/4 DDR2_PINALERT#

16,31,34,67,78,79 SMBCLK_VCC R119 0R/4 DDR2_CLK
16,31,34,67,78,79 SMBDATA_VCC R134 0R/4 DDR2_DATA

DDR2_CFG
R115 X_10K/4 TSENP2 TSENN2

TP1

U9 PV4210

30	VDD33D	VINSEN	27
28	VDD33A	DMD1	12
31	1V8	DMD2	10
5	VR_ENABLE	PWM1	11 DDR2_PWM1
2	VR_CLK	ISEN1P	23 ISEN1P_DDR2 R138 1K/4 ISEN1P_DDR2_R
3	VR_DATA	ISEN1N	22 ISEN1N_DDR2 R137 1K/4 ISEN1N_DDR2_R
4	VR_ALRT#	PWM2	9 DDR2_PWM2
6	VR_HOT#	ISEN2P	21 ISEN2P_DDR2 R136 1K/4 ISEN2P_DDR2_R
7	VR_READY	ISEN2N	20 ISEN2N_DDR2 R135 1K/4 ISEN2N_DDR2_R
1	PIN_ALRT#	VSENP	26 DDR2_VSENP
16	SCL	VSENN	24 DDR2_VSENN
17	SDA	VCOMP	25 DDR2_VCOMP
18	CONFIG		
14	VBOOT		
15	TSENP		
19	TSENN		
8	SYNC		
29	VDD5V		
13	IIN		
32	DGND		
33	AGND		

R129 10K/4 5VDIMM_IN2
R131 1K/4
C97 0.1u/16X/4
TP3
TP2

C102 0.01u25X/4
R139 0R/4 CP32
CP33
X_COPPER
X_COPPER
VCC_DDR_23
C107 100p50N4
close to DIMM side

VCCIO_VCCST

R95 140R1%/4 DDR_VIDSCLK 3,67
R94 140R1%/4 DDR_VIDSOUT 3,67
R93 140R1%/4 DDR_VIDALERT# 3,67

C61 0.1u/16X/4

3VSB_PWM
R100 1K/4
VCC_DDR_PG_23

Q36 2N3904
TSENP2
TSENN2
C847 100p50N4

Q185 NN-2N7002D
3VSB R1067 47K/4 G2 D2 MEM_HOT_C23_N
DDRVR2_HOT# G1 S2 S1

Q184 NN-2N7002D
3VSB R1066 47K/4 G2 D2 MEM_HOT_C23_N MEM_HOT_C23_N 3,12,13
DDR2_PINALERT# G1 S2 S1

Q169 NN-2N7002D
3,22,26,27,32,60,64,66,79,80 H_PROC_ID1 G2 D2 R1034 133KR1%4 DDR2_CFG
DDR2_CFG R1035 110K1%4 D1
3,60,64,69,79 H_PROC_ID1_5VA# G1 S2 S1

PROC_ID1	Config	CPU TYPE
1	133K	SKX-X (VR13) (SVID)
0	110K	KBL-X(IMVP8) (non SVID)

ATX_5VSB
R142 47K/4
C105 X_0.01u25X/4
Q28 X_NN-2N7002D
16,32,52,64,66,67,72,73 SLP_S4# G2 D2 S2 S1 G1

+VPP25_C23
R145 X_47K/4
VR_DDR_EN2_R

32,67 SIO_VDDQ_EN R146 47K/4 VR_DDR_EN2_R

5VDIMM_IN2
C137 C1u16X6
C132 C10u16X8

DDR2_UG1 R157 0R/6 DDR2_UG1_R
R162 10KR/4
DDR2_PH1A
DDR2_LG1

U14 NN-CSD87350Q5D_SON8-HF

DDR2_PH1
L16 CH-0.22u40A2.4mS-RH
VCC_DDR_23
R170 2.2R/8
C141 C1000p50X4
CP2 X_COPPER
CP4 X_COPPER

DDR2_BOOT1 R1086 2.2R/8 DDR2_BOOT1_R C848 0.1u/25X/6 DDR2_PH1A
ISEN1P_DDR2_R R1089 412R1%4
C110 0.22u6.3X4
ISEN1N_DDR2_R R1090 0R/4

5VDIMM_IN2
C136 C1u16X6
C128 C10u16X8

DDR2_UG2 R156 0R/6 DDR2_UG2_R
R161 10KR/4
DDR2_PH2A
DDR2_LG2

U13 NN-CSD87350Q5D_SON8-HF

DDR2_PH2
L15 CH-0.22u40A2.4mS-RH
VCC_DDR_23
R169 2.2R/8
C140 C1000p50X4
CP1 X_COPPER
CP3 X_COPPER

DDR2_BOOT2 R1085 2.2R/8 DDR2_BOOT2_R C849 0.1u/25X/6 DDR2_PH2A
ISEN2P_DDR2_R R1091 412R1%4
C109 0.22u6.3X4
ISEN2N_DDR2_R R1092 0R/4

U96 UP1959

1	B00T	UGATE	8 DDR2_UG1
2	PWM	PHASE	7 DDR2_PH1A
3	OD#	GND	6
4	VCC	LGATE	5 DDR2_LG1
9	GND		

DDR2_BOOT1
DDR2_PWM1
5VDIMM_23 R1088 0R/6 UP1959_VCC3_R
C851 0.1u/16X/4
C852 10u6.3X6

U95 UP1959

1	B00T	UGATE	8 DDR2_UG2
2	PWM	PHASE	7 DDR2_PH2A
3	OD#	GND	6
4	VCC	LGATE	5 DDR2_LG2
9	GND		

DDR2_BOOT2
DDR2_PWM2
5VDIMM_23 R1087 0R/6 UP1959_VCC4_R
C850 0.1u/16X/4
C853 10u6.3X6

VCC_DDR_23
EC27 560u6.3V
EC24 560u6.3V
EC28 560u6.3V
EC25 560u6.3V
EC30 560u6.3V

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Size: Custom	Document Description: VR13_VCCDDR23 PV4201-2 phase	Rev: 11
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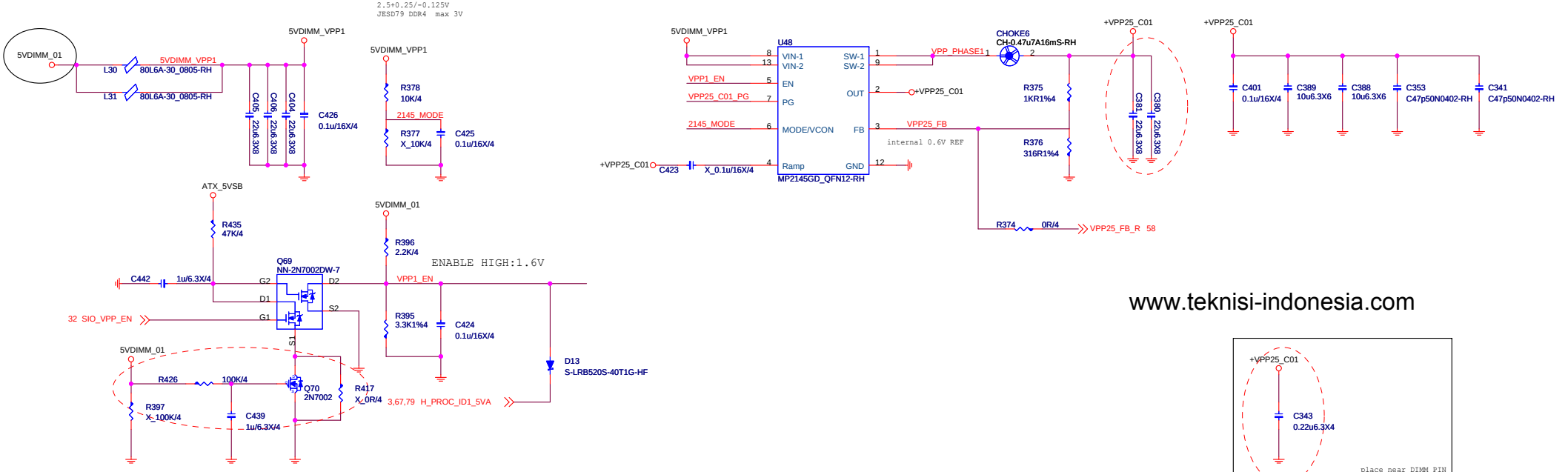
4DIMM :6A FOR DDR VPP



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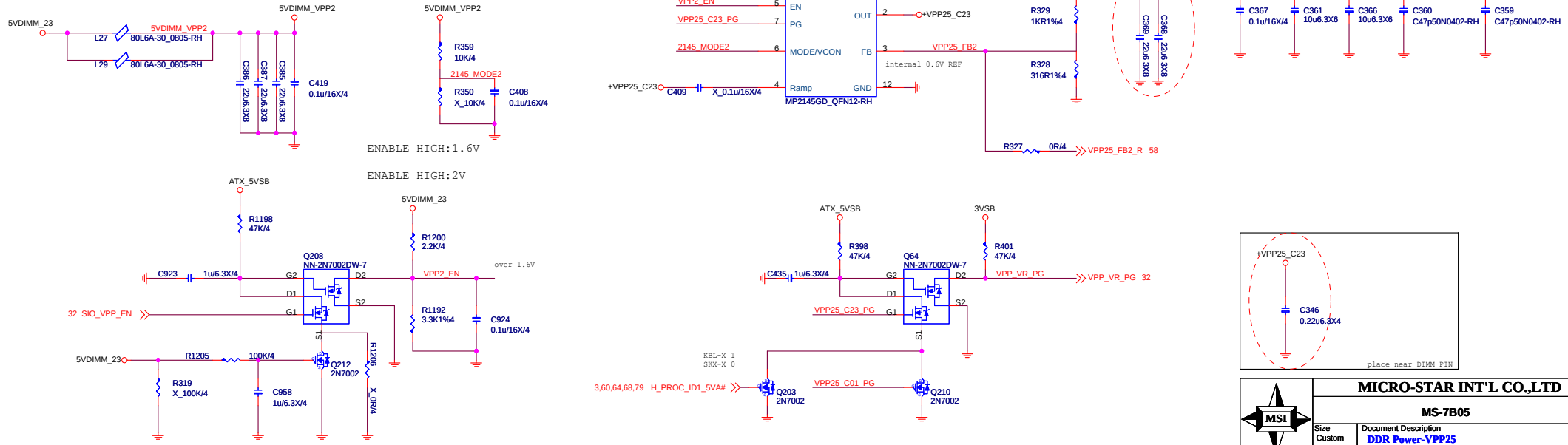

MICRO-STAR INT'L CO.,LTD		
MS-7B05		
Size: Custom	Document Description: DDR Power-VPP25	Rev: 11
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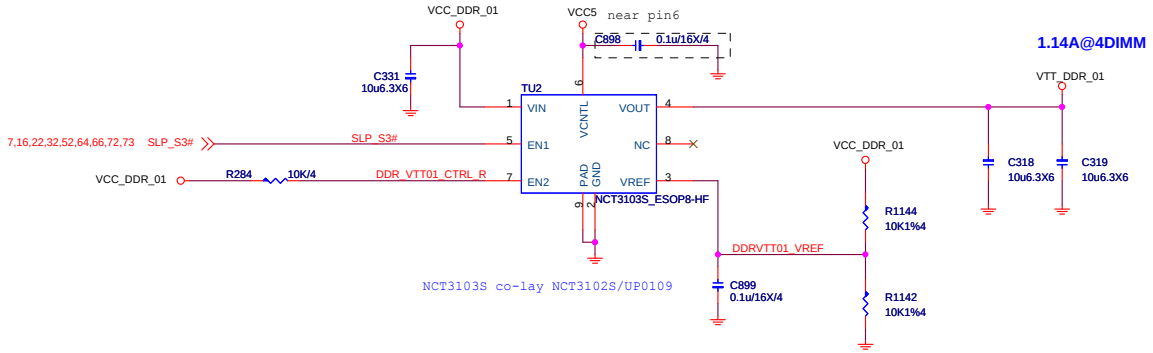
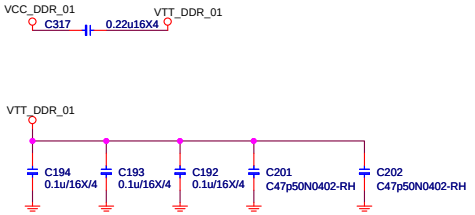
DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

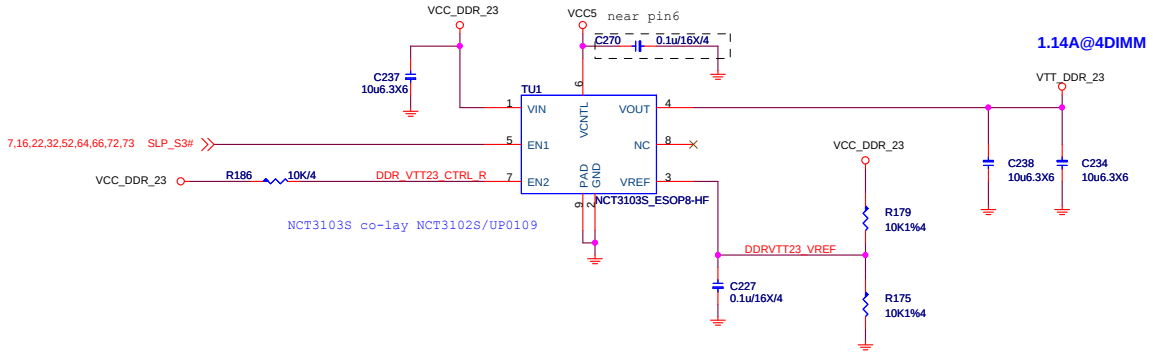


1.14A@4DIMM

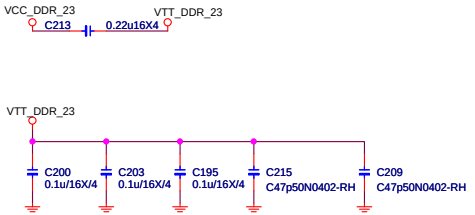


DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



1.14A@4DIMM



MICRO-STAR INT'L CO.,LTD		
MS-7B05		
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PCH_1VSB Power:1.0V,10A

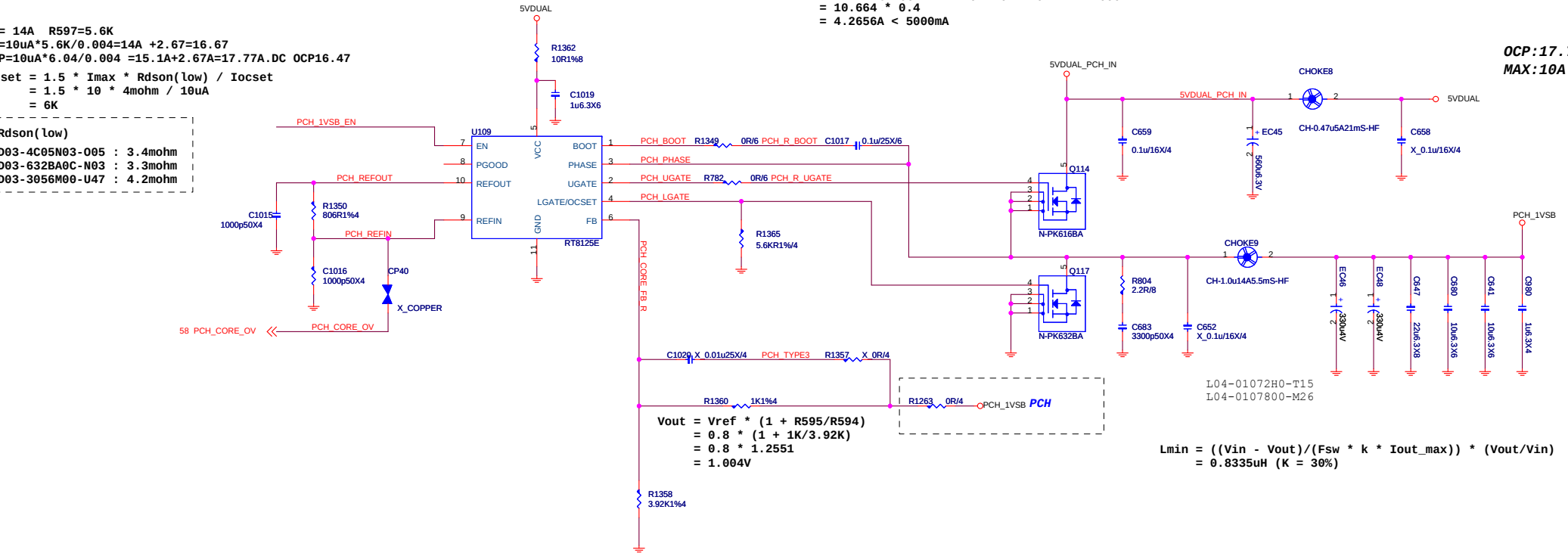
OCP = 14A R597=5.6K
IOCP=10uA*5.6K/0.004=14A +2.67=16.67
*IOOP=10uA*6.04/0.004 =15.1A+2.67A=17.77A.DC OCP16.47

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 1.5 * 10 * 4mohm / 10uA
= 6K

Rdson(low)
D03-4C05N03-005 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA

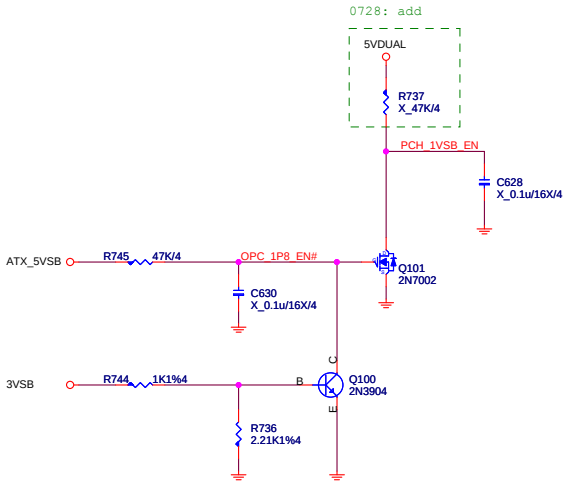
OCP:17.77
MAX:10A



L04-01072H0-T15
L04-0107800-M26

Vout = Vref * (1 + R595/R594)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)



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MS-7B05		
Size: Custom	Document Description: PCH POWER-RT8125E	Rev: 11
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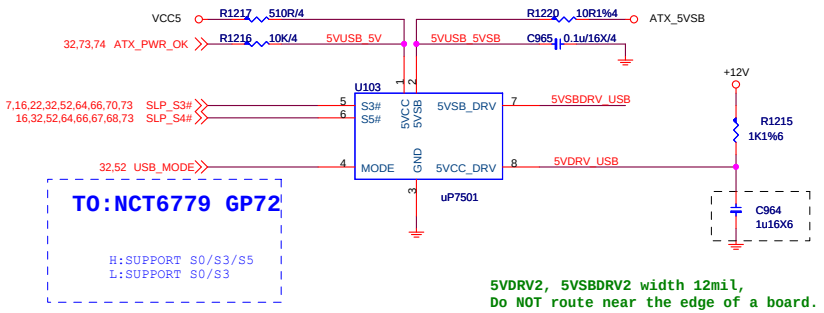
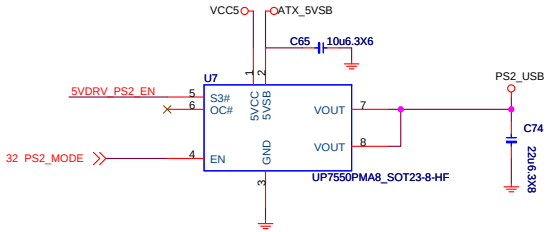
USB POWER

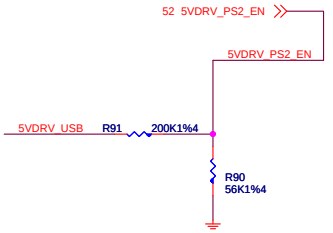


5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

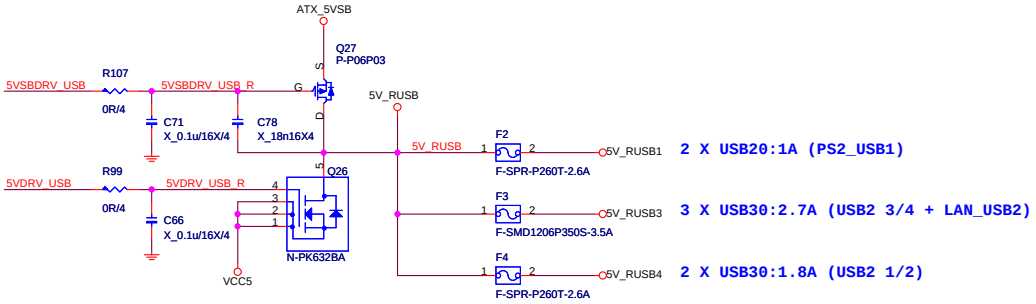
PS2 POWER



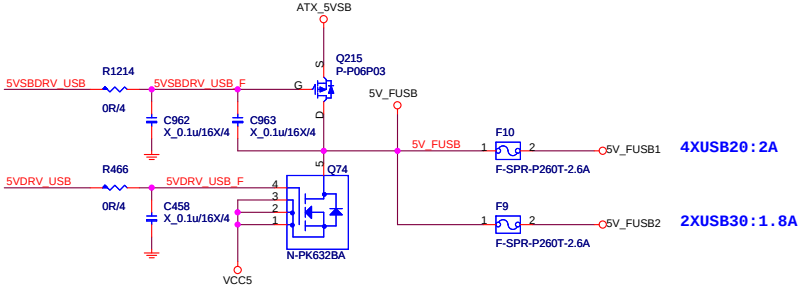
USB MODE



REAR USB PORT POWER



FRONT USB PORT POWER



MICRO-STAR INT'L CO.,LTD		
MS-7B05		
Size: Custom	Document Description: USB Power	Rev: 11
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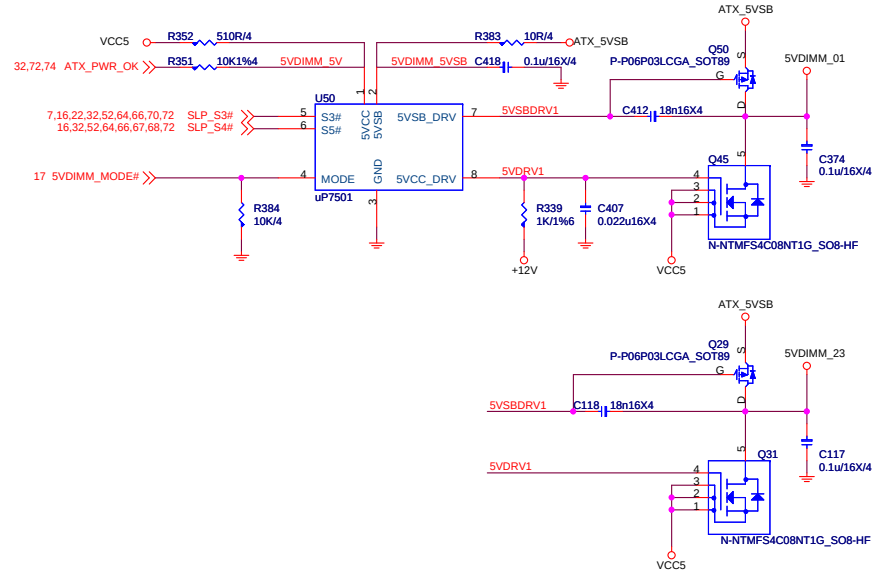
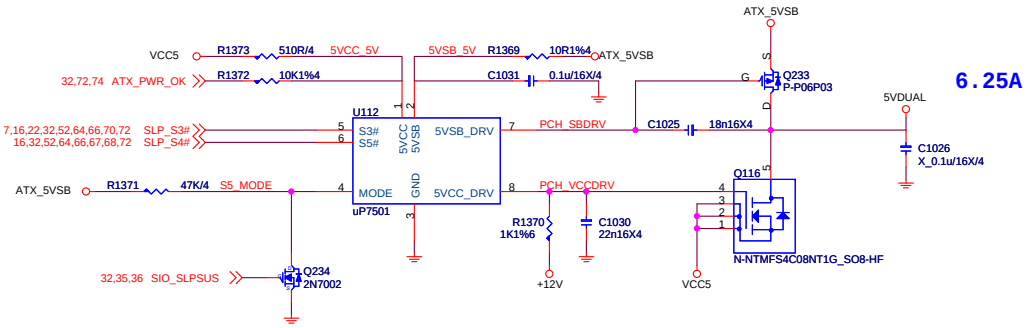
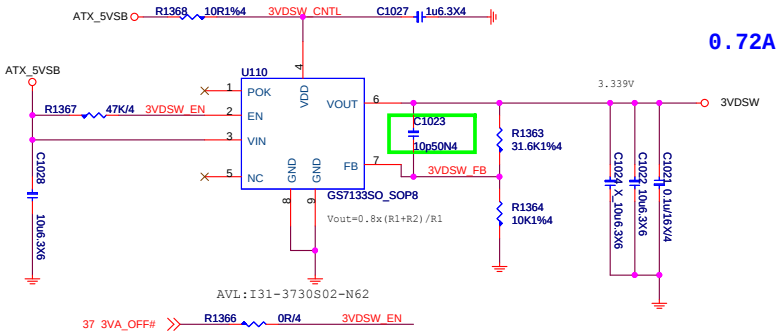
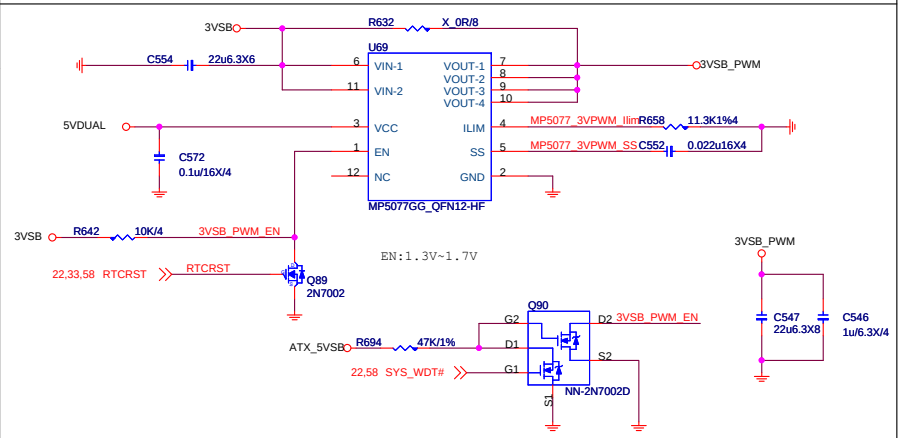
5VDIMM FOR DDR



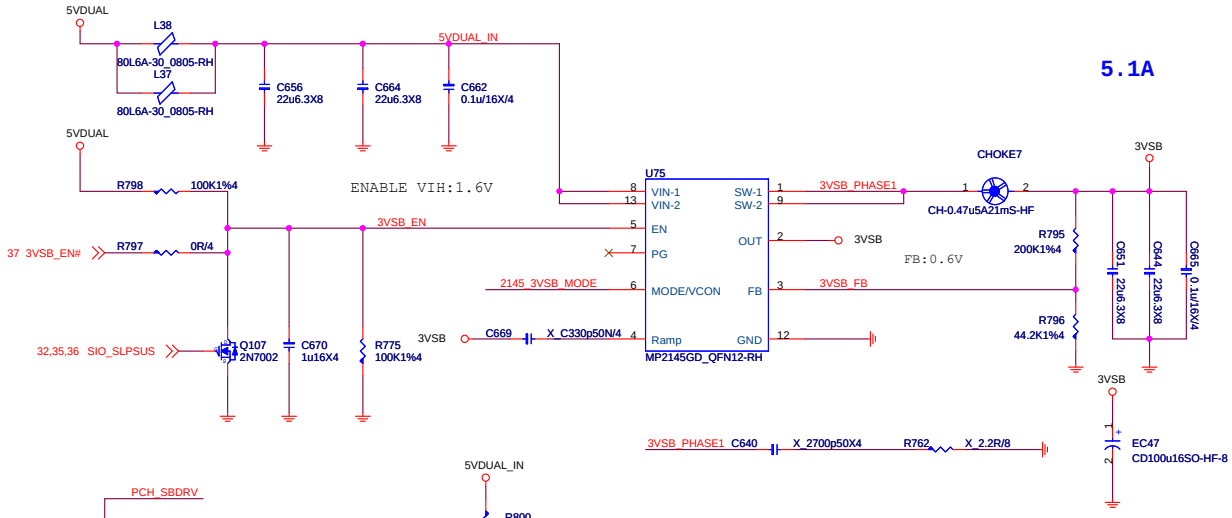


3VDSW





3VSB for OC & Gaming



防G3-->S5底下5VSBDRV2瞬間有電變沒電,使得下一級電壓爬升有drop

MICRO-STAR INT'L CO.,LTD		
MS-7B05		
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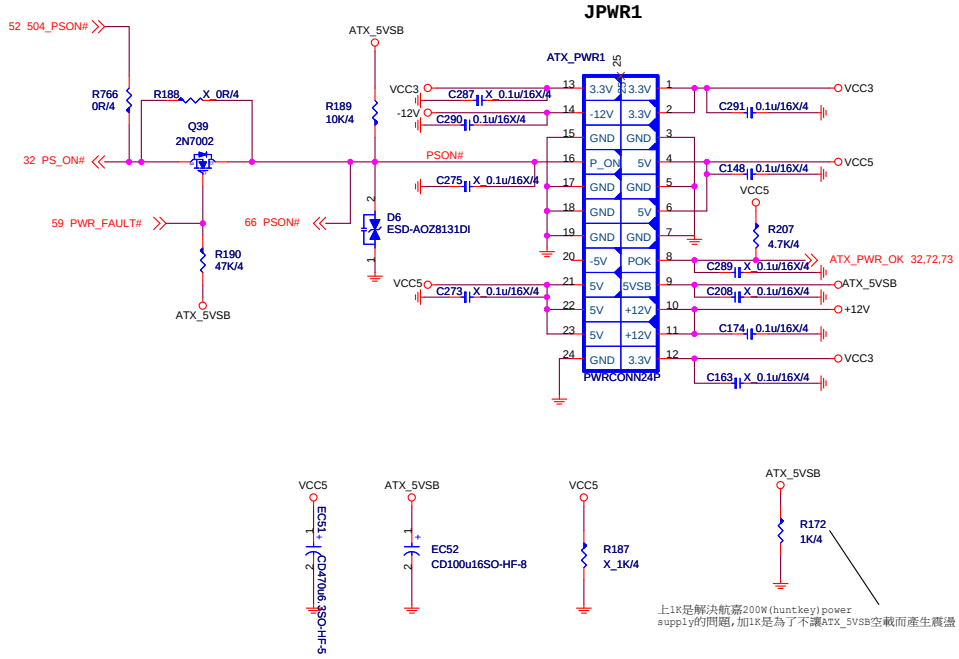
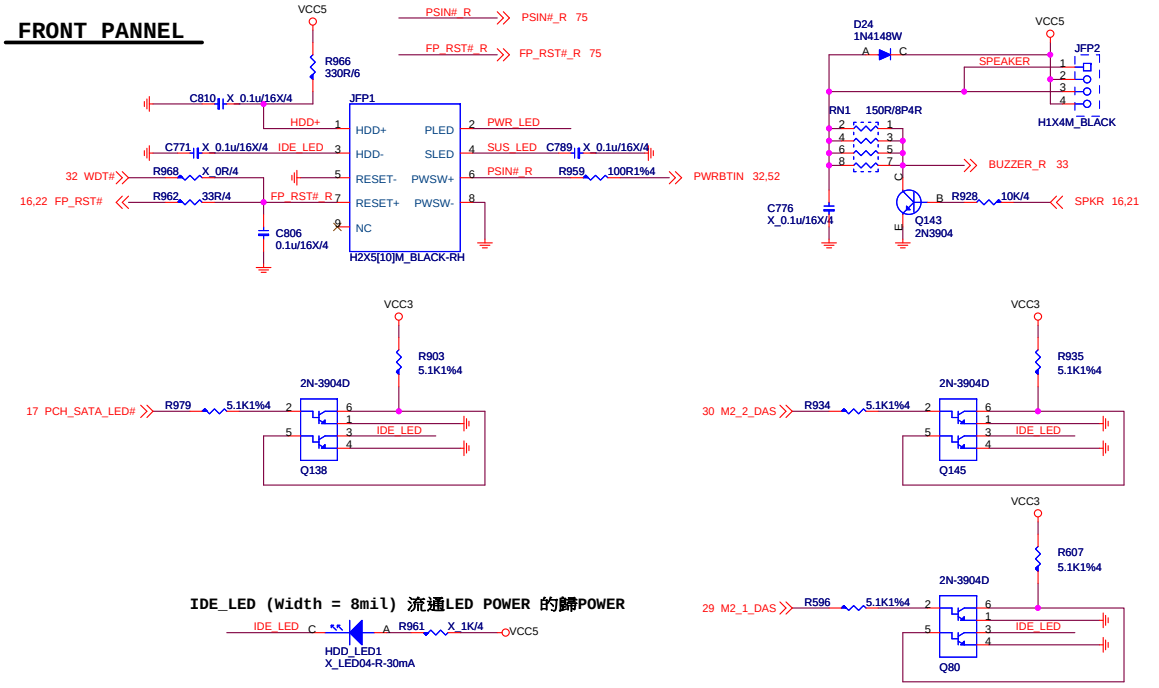
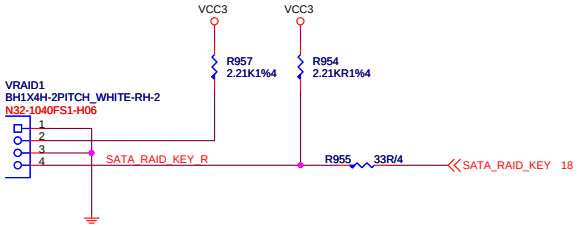
ATX POWER CONNECTOR



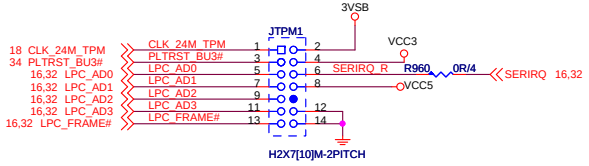
FRONT PANNEL



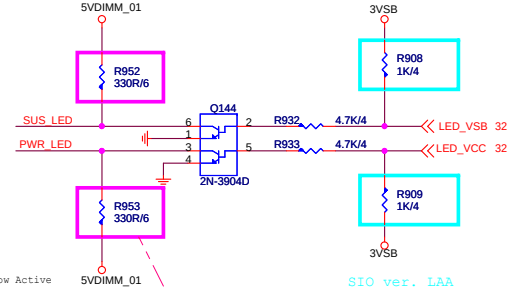
VROC Connentor



TPM Pin Header

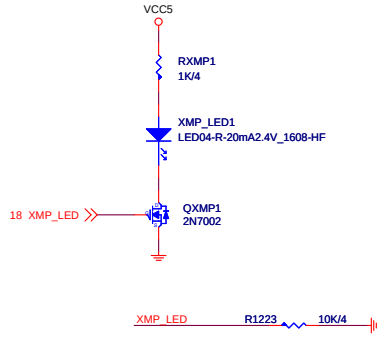


Front Panel LED



XMP LED

DIMM LED >> (default) :D0C-040P100-H91



MICRO-STAR INT'L CO.,LTD		
MS-7B05		
Size: Custom	Document Description: ATX Connector/F_Panel	Rev: 11
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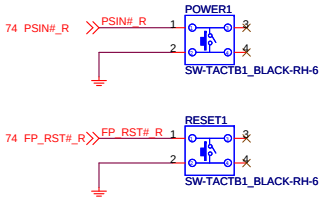
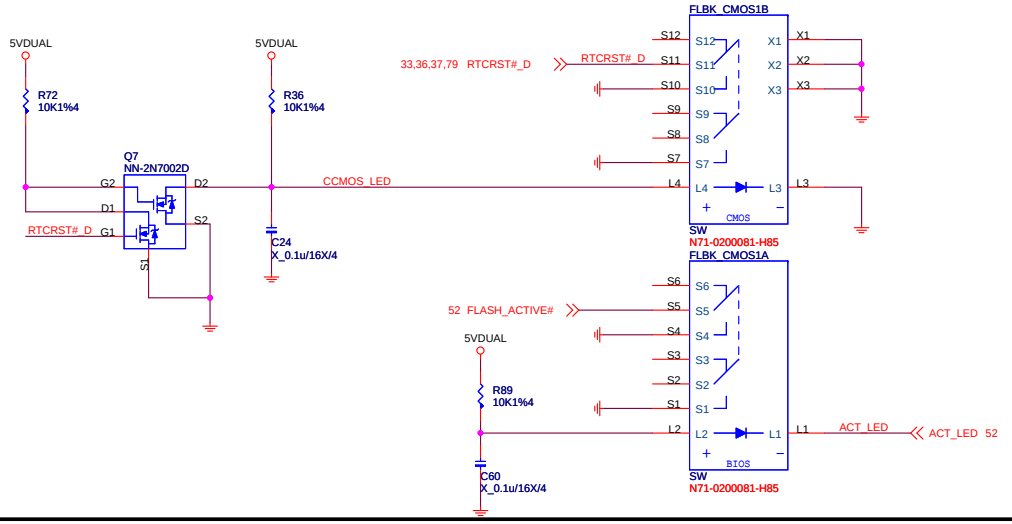
PWR/RST Botton



Clear CMOS button

LED LIGHTING RULE
S0/S3/S4 : LED OFF
S5 : LED ON



MICRO-STAR INT'L CO.,LTD		
MS-7B05		
Size: Custom	Document Description: Botton and OC GENIE	Rev: 11
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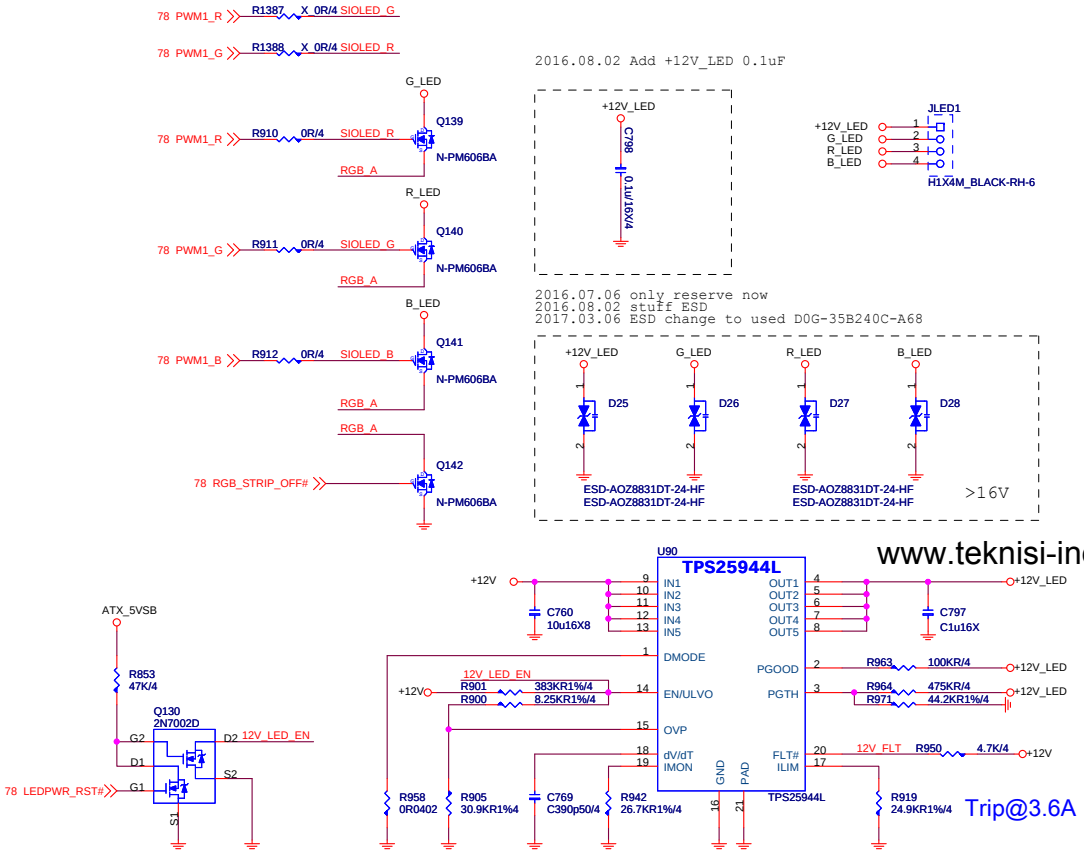
LED STRIPLINE



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	MS-7B05	
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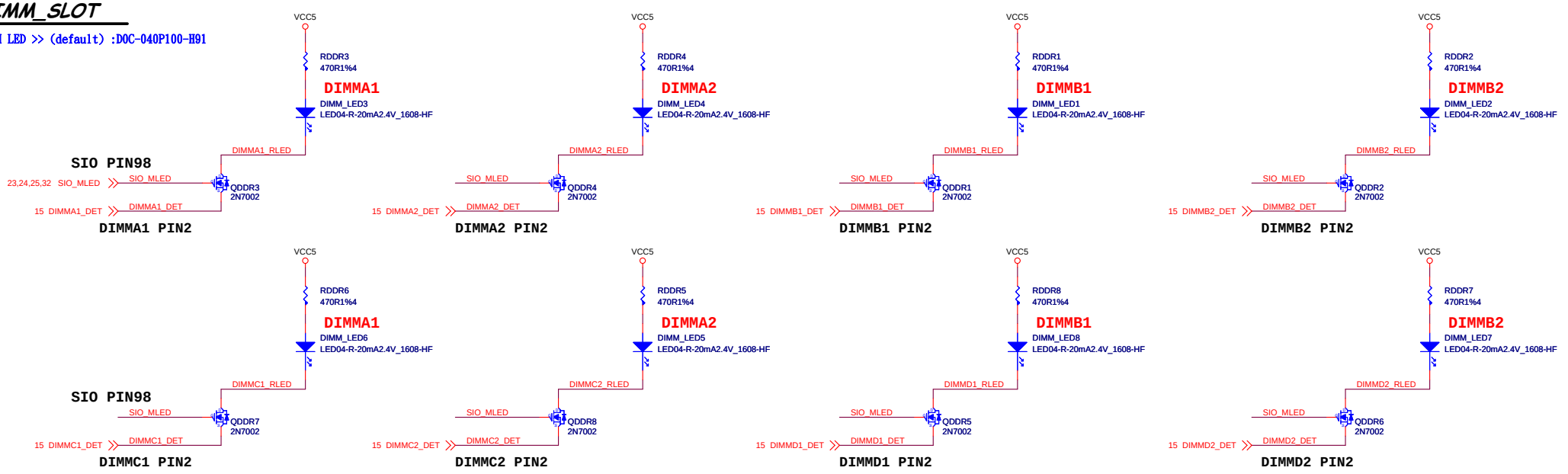
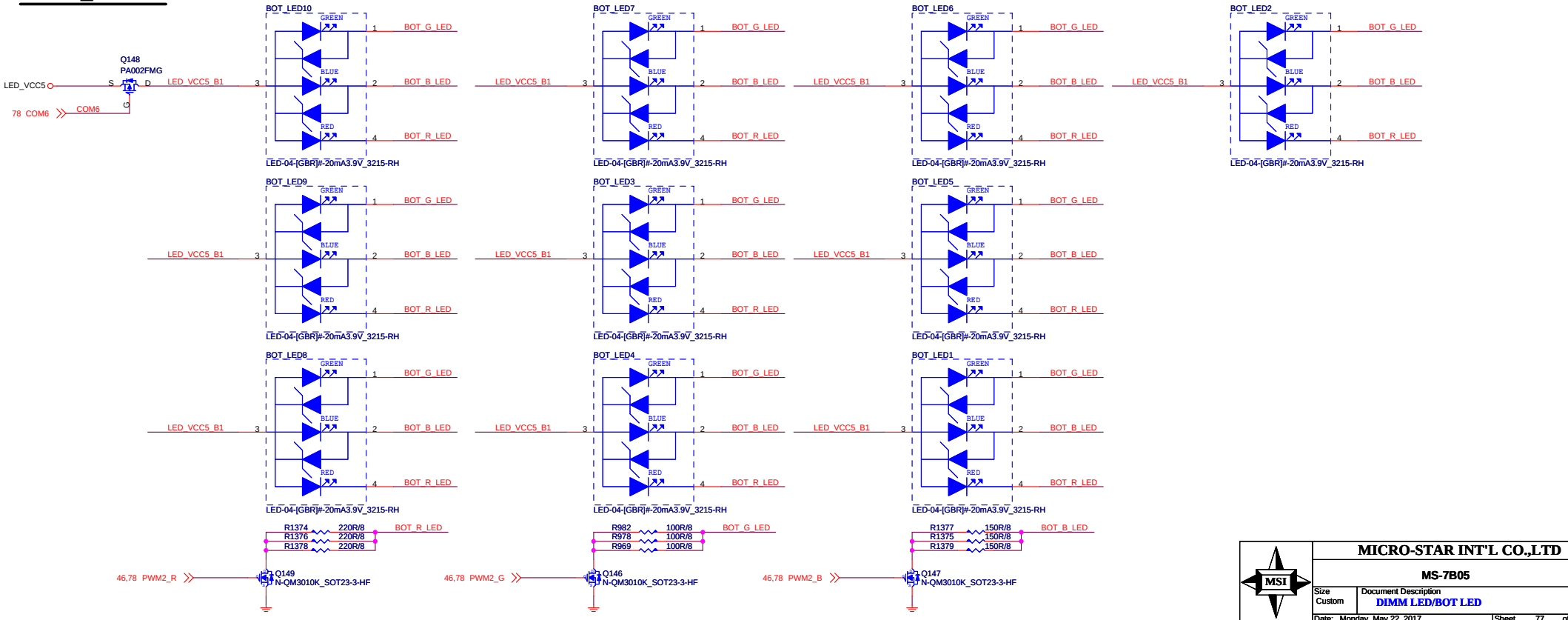
DIMM_SLOT

DIMM LED >> (default) :DOC-040P100-H91



Bottom_LED



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7B05	
Size: Custom	Document Description: DIMM LED/BOT LED	Rev: 11
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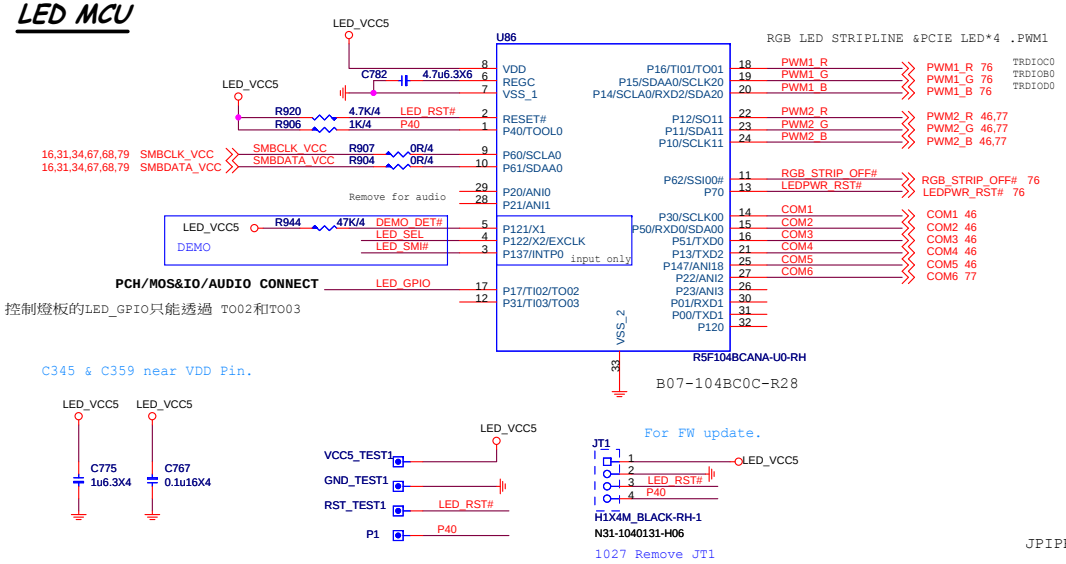
LED MCU



RGB LED STRIPLINE &PCIE LED*4 .PWM1

PWM1_R 18 → PWM1_R 76
PWM1_G 19 → PWM1_G 76
PWM1_B 20 → PWM1_B 76
PWM2_R 22 → PWM2_R 46,77
PWM2_G 23 → PWM2_G 46,77
PWM2_B 24 → PWM2_B 46,77
RGB_STRIP_OFF# 11 → RGB_STRIP_OFF# 76
LEDPWR_RST# 13 → LEDPWR_RST# 76
COM1 14 → COM1 46
COM2 15 → COM2 46
COM3 16 → COM3 46
COM4 21 → COM4 46
COM5 25 → COM5 46
COM6 27 → COM6 77

TRDIOC0
TRDIOB0
TRDIOD0

2016.10.21 100K下拉,避免floating

PWM1_G R894 100K/4
PWM1_R R895 100K/4
PWM1_B R893 100K/4
LEDPWR_RST# R897 47K/4 → LED_VCC5
RGB_STRIP_OFF# R899 47K/4 → LED_VCC5
LED_SEL R941 47K/4 C783 0.1u16X4 → LED_VCC5
LED_SMI# R931 47K/4 C781 0.1u16X4 → LED_VCC5

Control	Net Name	PWM USE	Connector
AUDIO Cover	LED_GPIO	No Use	JPIPE_LED1
PCH	LED_GPIO_01	No Use	JPIPE_LED2
MOS/IO cover	LED_GPIO_02	No Use	JPIPE_LED3
LED STRIPLINE	RGB_STRIP_OFF#	PWM1	JLED1
Board Side LED	COM1~8	PWM2	RGB LED
PCIE Side LED	COM1~4	PWM1	RGB LED

C345 & C359 near VDD Pin.

LED_VCC5 C775 1u6.3X4
LED_VCC5 C767 0.1u16X4

LED_VCC5
VCC5_TEST1
GND_TEST1
RST_TEST1 LED_RST#
P1 P40

For FW update.

JT1 1 2 3 4 LED_VCC5 LED_RST# P40
H1X4M_BLACK-RH-1
N31-1040131-H06
1027 Remove JT1

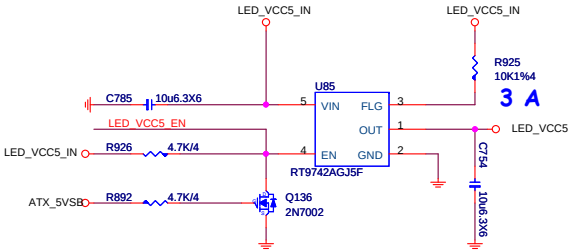
1 PCH HEATSINK LED

PCS LED*0.16W=W

JPIPE:PIN1:output ,PIN2:input
PIN 2:MCU IN
PIN 1:HEATSINK OUT

LED_VCC5 F7 F-SPR-P110-HF
LED_GPIO_01
LED_GPIO
PIPE1_PCH_VCC5
JPIPE_LED1
X_BH1X4S-1PITCH-0.74MM_BLACK-HF
N32-1040FH0-H06
LEDPWR_RST# Q46 N-QM3010K_SOT23-3-HF

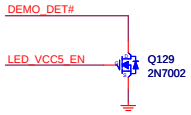
EXTERNAL POWER INPUT



min 80mil.

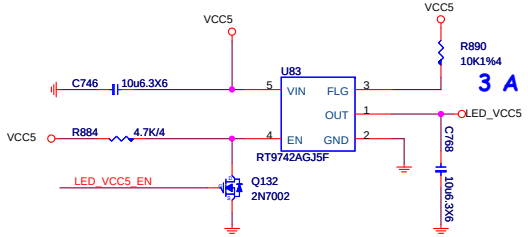
I36-9742A09-R11

LED Demo Button



2A Connector

JPWRLED1
BH1X2H-2PITCH_BLACK-HF
N32-1020CB1-H06
LED_VCC5_IN
C784 0.1u16X4
LED_VCC5_IN R951 100K1%4



2 MOS HEATSINK LED

PCS LED*0.16W=W

LED_VCC5 F1 F-SPR-P110-HF
LED_GPIO_02
PIPE3_MOS_VCC5
JPIPE_LED2
X_BH1X4S-1PITCH-0.74MM_BLACK-HF
N32-1040FH0-H06
LEDPWR_RST# Q5 N-QM3010K_SOT23-3-HF

3 AUDIO/IO Cover LED

PCS LED*0.16W=W

LED_VCC5 F8 F-SPR-P110-HF
LED_GPIO_02
LED_GPIO_01
PIPE2_AUDIO_VCC5
JPIPE_LED3
X_BH1X4S-1PITCH-0.74MM_BLACK-HF
N32-1040FH0-H06
LEDPWR_RST# Q47 N-QM3010K_SOT23-3-HF

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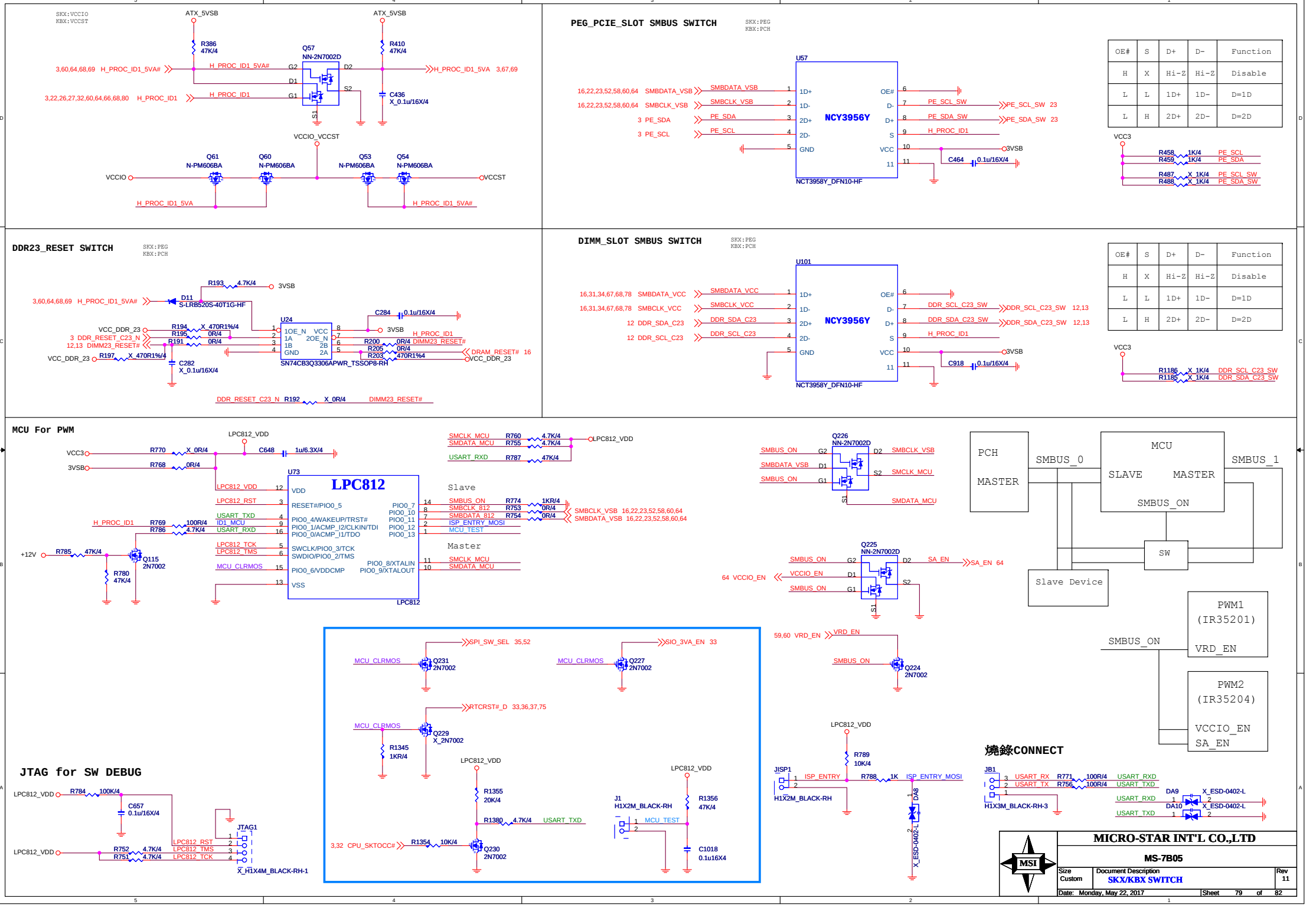
SKX:VCCIO
KBX:VCCST
ATX_5VSB
R386 47K/4
Q57 NN-2N7002D
R410 47K/4
C436 X_0.1u/16X/4
H_PROC_ID1_5VA#
H_PROC_ID1
VCCIO_VCCST
Q61 N-PM606BA
Q60 N-PM606BA
Q53 N-PM606BA
Q54 N-PM606BA
VCCIO
VCCST
PEG_PCIE_SLOT SMBUS SWITCH
SKX:PEG
KBX:PCH
U57
NCY3956Y
NCT3958Y_DFN10-HF
SMBDATA_VSB
SMBCLK_VSB
PE_SDA
PE_SCL
PE_SCL_SW
PE_SDA_SW
H_PROC_ID1
3VSB
C464 0.1u/16X/4
OE# S D+ D- Function
H X Hi-Z Hi-Z Disable
L L 1D+ 1D- D=1D
L H 2D+ 2D- D=2D
R458 1K/4 PE_SCL
R459 1K/4 PE_SDA
R487 X_1K/4 PE_SCL_SW
R488 X_1K/4 PE_SDA_SW
DDR23_RESET SWITCH
SKX:PEG
KBX:PCH
R193 4.7K/4
D11 S-LRB520S-40T1G-HF
U24
SN74CB3Q3306APWR_TSSOP8-RH
C284 0.1u/16X/4
R194 X_470R1%/4
R195 0R/4
R191 0R/4
R197 X_470R1%/4
C282 X_0.1u/16X/4
R200 0R/4 DIMM23_RESET#
R205 0R/4
R203 470R1%4
DRAM_RESET# 16
VCC_DDR_23
DDR_RESET_C23_N R192 X_0R/4 DIMM23_RESET#
DIMM_SLOT SMBUS SWITCH
SKX:PEG
KBX:PCH
U101
NCY3956Y
NCT3958Y_DFN10-HF
SMBDATA_VCC
SMBCLK_VCC
DDR_SDA_C23
DDR_SCL_C23
DDR_SCL_C23_SW
DDR_SDA_C23_SW
H_PROC_ID1
3VSB
C918 0.1u/16X/4
OE# S D+ D- Function
H X Hi-Z Hi-Z Disable
L L 1D+ 1D- D=1D
L H 2D+ 2D- D=2D
R1186 X_1K/4 DDR_SCL_C23_SW
R1185 X_1K/4 DDR_SDA_C23_SW
MCU For PWM
LPC812_VDD
R770 X_0R/4
C648 1u/6.3X/4
R768 0R/4
U73
LPC812
VDD
RESET#/PIO0_5
PIO0_4/WAKEUP/TRST#
PIO0_1/ACMP_I2/CLKIN/TDI
PIO0_0/ACMP_I1/TDO
SWCLK/PIO0_3/TCK
SWDIO/PIO0_2/TMS
PIO0_6/VDDCMP
VSS
PIO0_7
PIO0_10
PIO0_11
PIO0_12
PIO0_13
PIO0_8/XTALIN
PIO0_9/XTALOUT
LPC812_RST
USART_TXD
ID1_MCU
USART_RXD
LPC812_TCK
LPC812_TMS
MCU_CLRMOS
SMBUS_ON
SMBCLK_812
SMBDATA_812
ISP_ENTRY_MOSI
MCU_TEST
SMCLK_MCU
SMDATA_MCU
Slave
Master
SMCLK_MCU R760 4.7K/4
SMDATA_MCU R755 4.7K/4
USART_RXD R787 47K/4
R774 1KR/4
R753 0R/4
R754 0R/4
SMBCLK_VSB 16,22,23,52,58,60,64
SMBDATA_VSB 16,22,23,52,58,60,64
H_PROC_ID1
R769 100R/4
R786 4.7K/4
+12V
R785 47K/4
Q115 2N7002
R780 47K/4
Q226 NN-2N7002D
SMBUS_ON
SMBDATA_VSB
SMBCLK_VSB
SMBCLK_MCU
SMDATA_MCU
Q225 NN-2N7002D
VCCIO_EN
SA_EN
64 VCCIO_EN
SA_EN 64
PCH
MASTER
SMBUS_0
MCU
SLAVE
MASTER
SMBUS_1
SMBUS_ON
SW
Slave Device
PWM1 (IR35201)
VRD_EN
SMBUS_ON
PWM2 (IR35204)
VCCIO_EN
SA_EN
59,60 VRD_EN
Q224 2N7002
SPI_SW_SEL 35,52
SIO_3VA_EN 33
Q231 2N7002
Q227 2N7002
RTCRST#_D 33,36,37,75
Q229 X_2N7002
R1345 1KR/4
R1355 20K/4
R1380 4.7K/4 USART_TXD
R1354 10K/4
3,32 CPU_SKTOCC#
Q230 2N7002
J1 H1X2M_BLACK-RH
MCU_TEST
R1356 47K/4
C1018 0.1u16X4
JISP1 H1X2M_BLACK-RH
ISP_ENTRY
ISP_ENTRY_MOSI
R789 10K/4
R788 1K
DA8 X_ESD-0402-L
JTAG for SW DEBUG
R784 100K/4
C657 0.1u/16X/4
R752 4.7K/4
R751 4.7K/4
LPC812_RST
LPC812_TMS
LPC812_TCK
JTAG1
X_H1X4M_BLACK-RH-1
燒錄CONNECT
JB1
USART_RX
USART_TX
R771 100R/4
R756 100R/4
H1X3M_BLACK-RH-3
DA9 X_ESD-0402-L
DA10 X_ESD-0402-L
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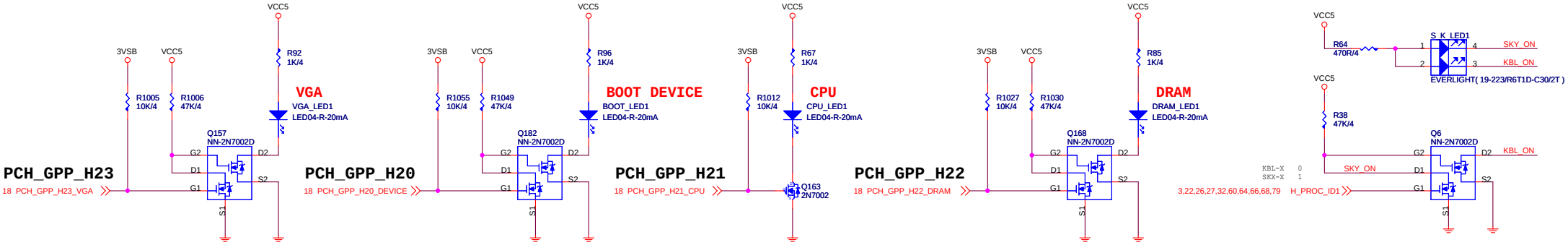
LED
紅 : D0C-040P100-H91
AVL: D0C-040S500-E07

LED
白 : D0C-040T200-H91
AVL: D0C-040S200-E07



GPIO / LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

關機斷電狀態下，4個LED先維持default全暗，開機通電後：

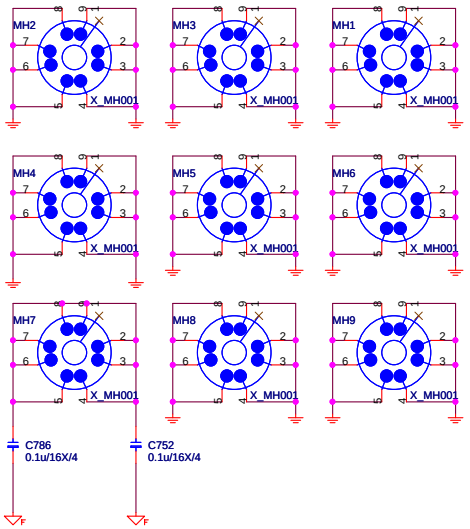
1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. BOOT DEVICE的check/BOOT LED亮，check PASS後則BOOT LED滅掉。
5. 因此最後正常順利開機後，四個LED燈都是滅掉的。
   （系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

HEATSINK

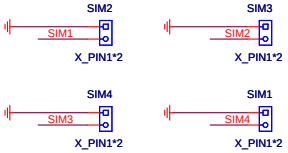
PCH_SINK1 — PCH_HEATSINK — E31-0409100-K08
CPU_SINK1 — CPU_HEATSINK — E31-0504930-K08
DDR_SLOT_LA1 — DDR_Slot — DDRIV-288P_WHITE-RH-12
PSINK_LA1 — PCH Heatsink — E31-0409150-K08
PCIE_SLOT_LA1 — PCIE_Slot — SLOT-PCI164P_WHITE-2PITCH-RH-4
CSINK_LA1 — CPU_MOS Heatsink — E31-0504970-K08
PCIE_SLOT_LA2 — PCIE_Slot — SLOT-PCI100P_WHITE-2PITCH-RH-3
VR_COVER1 — VR Cover — E21-7A63020-RH
M2_COVER1 — M2 Cover — X_M2_COVER1
CHOKE_COVER1 — choke Cover — X_CHOKE_COVER1
PCB_LA1 — PCB — PS0-07B0521-G37
CPU_H1 — CPU 鐵座 — X_CPU_ILM1 — E21-7881010-L06
CPU_H2 — CPU 鐵座 — X_CPU_BP1 — E93-0000131-L06
CPU_H3 — CPU 鐵座 — CPU_H1 — E21-7862010-L06
AMI_LA1 — AMI Label — G51-M1SPXXA-A09
MKT_LA1 — BIOS LABLE — X_G51-M1SPL09-Q13
MKT_LA2 — BIOS LABLE — G51-M1SPL54-Q13
MKT_LA3 — BIOS LABLE — G51-M1SPL70-Q13
CFOS_LA1 — CFOS Label — Y02-MU00170-CFO
XSPLIT_LA1 — XSPLIT Label — Y02-MA00401-XSP
NAH_LA1 — NAHIMIC Label — Y02-MU00100-NAH
SSE_LA1 — SSE Label — Y02-MA00101-SSE
SLI_LA1 — SLI Label — Y01-RNVIDIL-000
DLED_LA1 — LED Label — X_D0C-040T200-H91
VIRTUAL1 — Label — VIRTUAL
PCB1 — PD0-07B0511-G37
BAT1_X1 — BAT-BCR2032P-RH

PD0-07B0510-G37,精成-深圳,98,寶安恩斯邁廠(MSIS)8,black
PD0-07B0510-E48,競華,23,寶安恩斯邁廠(MSIS)8,black

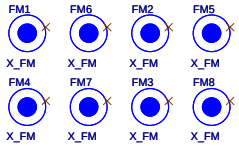
Mounting Holes



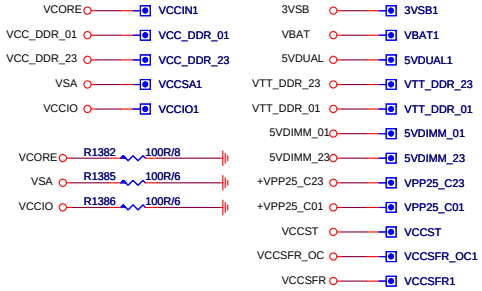
Simulation



Optical Fiducial Marks-120



Test point



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