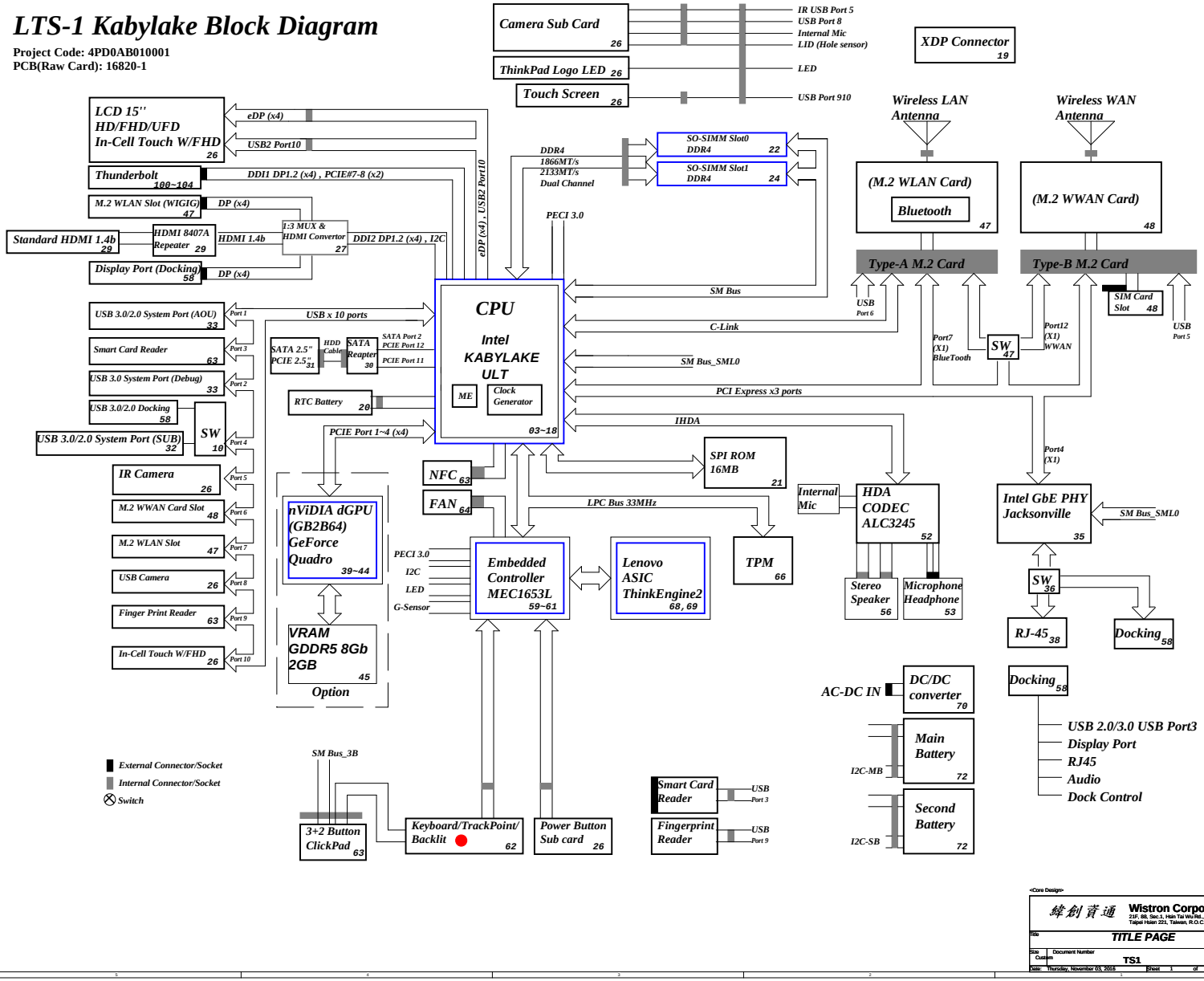
LTS-1 Kabylake Block Diagram

Project Code: 4PD0AB010001
PCB(Raw Card): 16820-1



<Core Design>

蟑創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: TITLE PAGE

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 1 of 103

RESISTOR

CAPACITOR

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EC HISTORY

Size	Document Number	Rev
C	TS1	1

Date: Thursday, November 03, 2016 Sheet 2 of 103

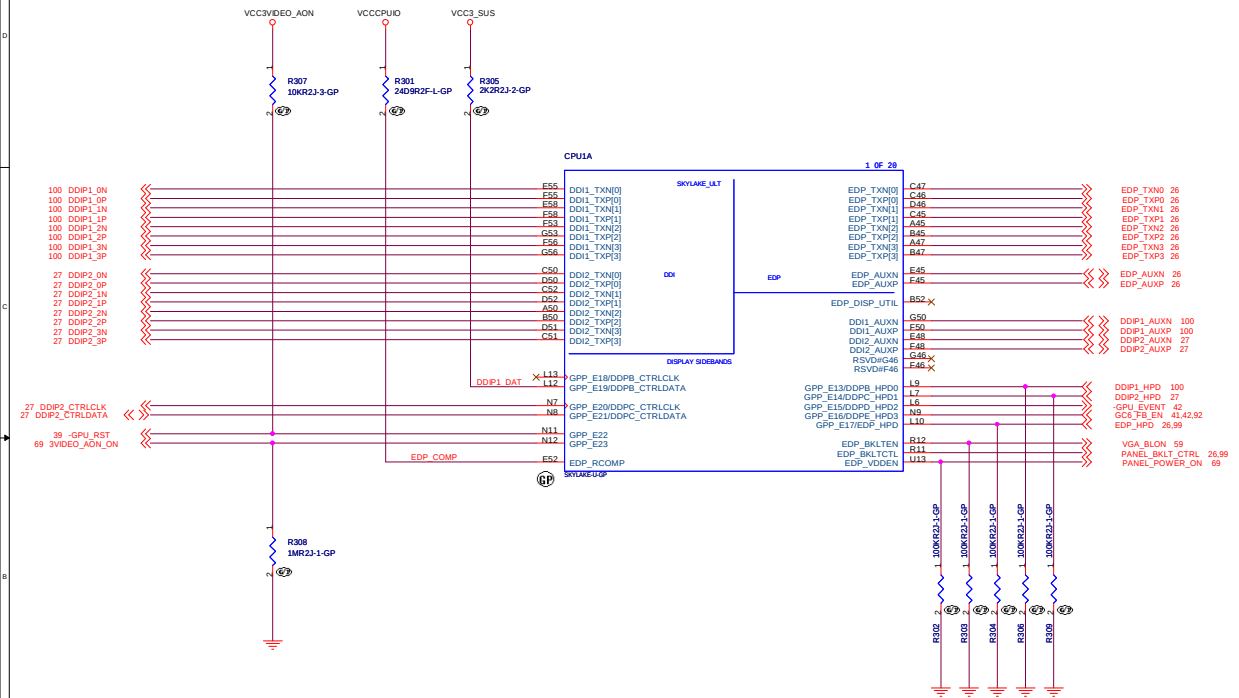
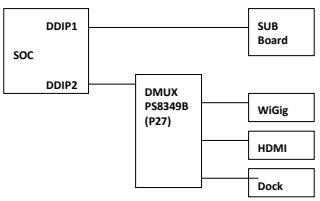


TABLE: Functional Strap

DDPB_CTRLDATA	
HIGH	Port B is detected.
LOW	Port B is not detected.
DDPC_CTRLDATA	
HIGH	Port C is detected.
LOW	Port C is not detected.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

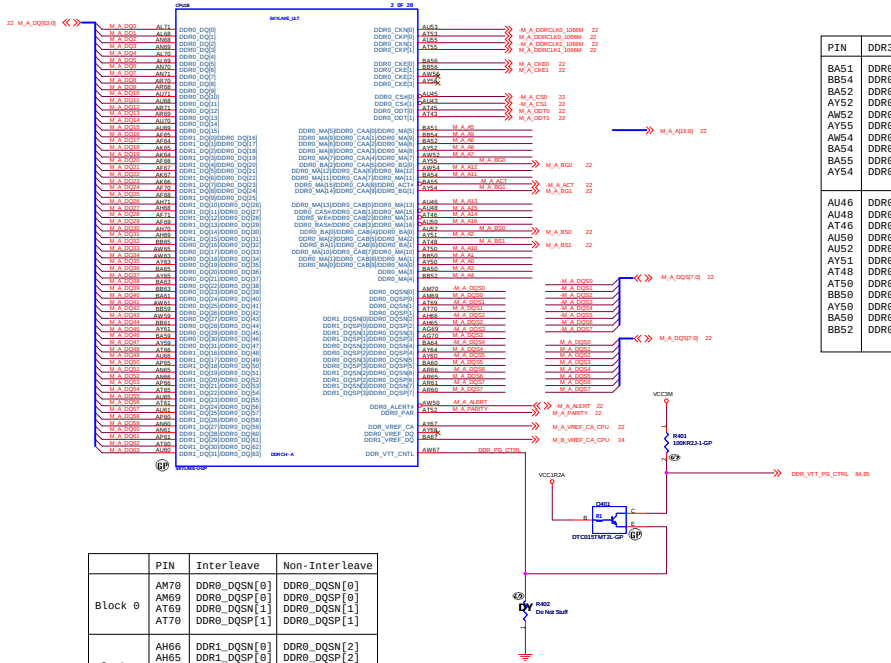
Title: CPU(1/16) : DDI/EDP

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 3 of 103

	PIN	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
	AU69	DDR0_DQ[15]	DDR0_DQ[15]
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF66	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 2	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA65	DDR0_DQ[20]	DDR0_DQ[36]
	AY65	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
	BB59	DDR0_DQ[26]	DDR0_DQ[42]
	AW59	DDR0_DQ[27]	DDR0_DQ[43]
	BB61	DDR0_DQ[28]	DDR0_DQ[44]
	AY61	DDR0_DQ[29]	DDR0_DQ[45]
	BA59	DDR0_DQ[30]	DDR0_DQ[46]
	AY59	DDR0_DQ[31]	DDR0_DQ[47]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN66	DDR1_DQ[20]	DDR0_DQ[52]
	AP66	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
	AT60	DDR1_DQ[30]	DDR0_DQ[62]
	AU60	DDR1_DQ[31]	DDR0_DQ[63]

LOGIC



	PIN	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]

LOGIC

PIN	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

LOGIC

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

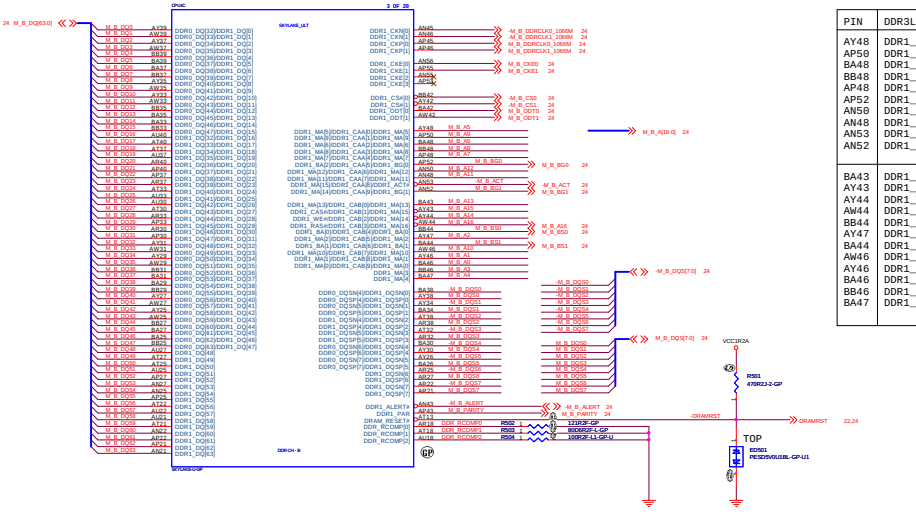
Title: CPU(2/16) : DDR CHANNEL-A

Size	Document Number	Rev
A2	TS1	1

Date: Thursday, November 03, 2016 Sheet 4 of 100

	PIN	Interleave	Non-Interleave
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
	BB33	DDR0_DQ[47]	DDR1_DQ[15]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU30	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
	AR30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	AW25	DDR0_DQ[59]	DDR1_DQ[43]
	BB27	DDR0_DQ[60]	DDR1_DQ[44]
	BA27	DDR0_DQ[61]	DDR1_DQ[45]
	BA25	DDR0_DQ[62]	DDR1_DQ[46]
	BB25	DDR0_DQ[63]	DDR1_DQ[47]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

LOGIC



	PIN	Interleave	Non-Interleave
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

LOGIC

PIN	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

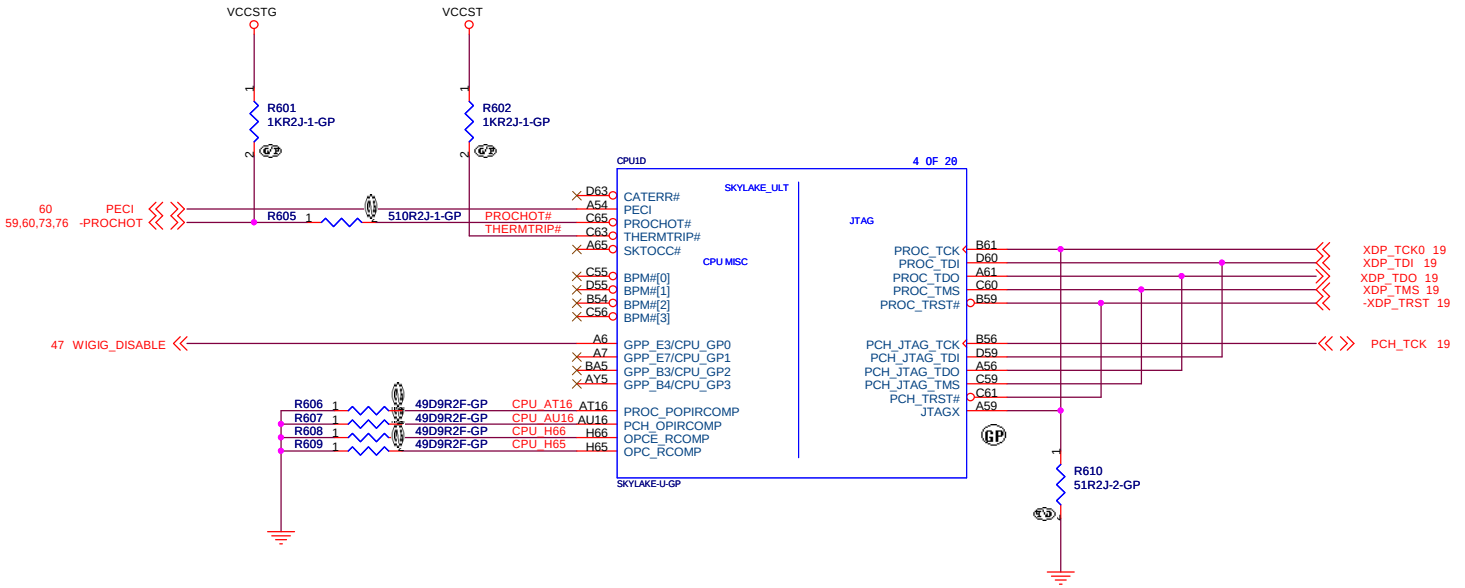
LOGIC

<Core Design>
偉創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(3/16) : DDR CHANNEL-B

Size	Document Number	Rev
A2	TS1	1

Date: Thursday, November 03, 2016 Sheet 5 of 100



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(4/16) : MISC/JTAG**

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 6 of 103

TABLE: Functional Strap

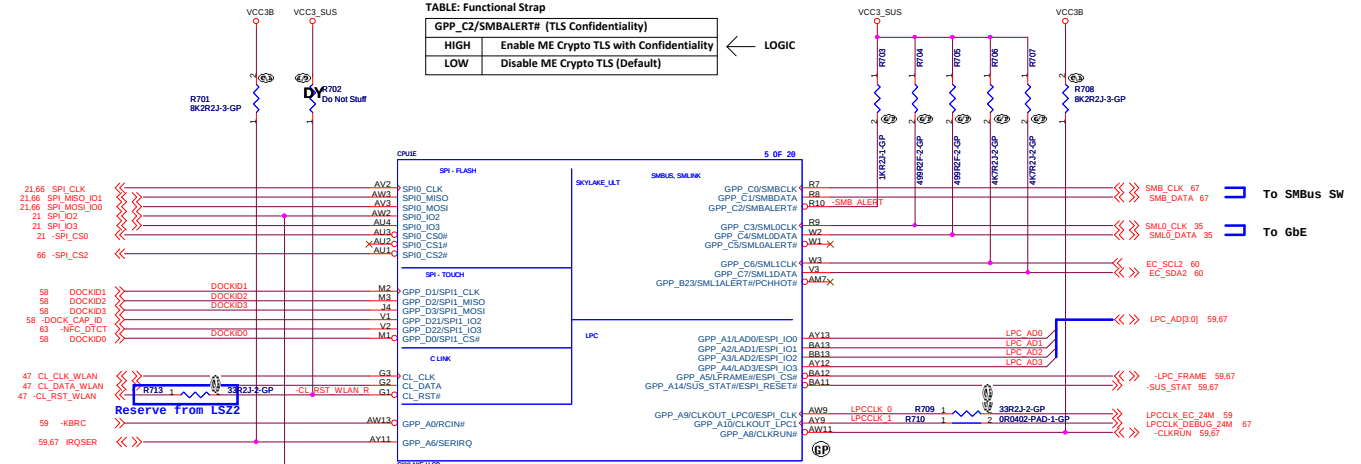
GPP_C5/SML0ALERT# (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

LOGIC

TABLE: Functional Strap

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

LOGIC



DY R712 Do Not Stuff

SPI_MISO_IO1

TABLE: Functional Strap

SPI0_IO2 (Consent Strap)	
HIGH	Enable (Default)
LOW	Disable

TABLE: Functional Strap

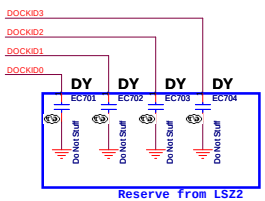
SPI0_MOSI (Boot Halt)	
HIGH	Disable(Default)
LOW	Enable

TABLE: Functional Strap

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disable(Default)
LOW	Enable

TABLE: Functional Strap

SPI0_MISO (JTAG ODT Disable)	
HIGH	Enable (Default)
LOW	Disable



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(5/16) : LPC/SPI/SMBUS/C-LINK

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 7 of 103

TABLE: Functional Strap

GPP_B22/GSPI1_MOSI (Boot BIOS Destination)	
HIGH	Boot BIOS from LPC
LOW	Boot BIOS from SPI (Default)

LOGIC

TABLE: Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)

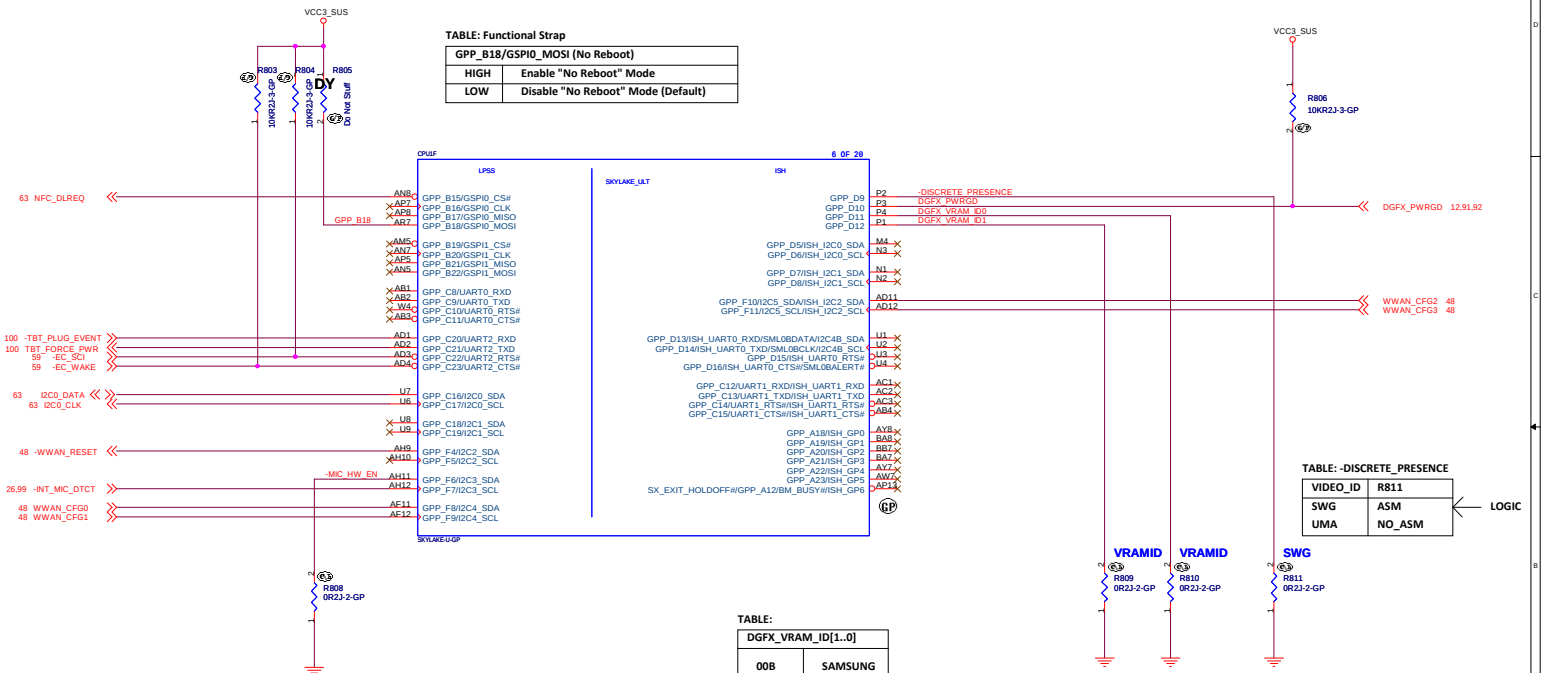


TABLE: -DISCRETE_PRESENCE

VIDEO_ID	R811
SWG	ASM
UMA	NO_ASM

LOGIC

TABLE:

DGFX_VRAM_ID[1..0]	
00B	SAMSUNG
01B	MICRON
10B	RESERVE
11B	RESERVE

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(6/16) : LPSS/ISH**

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 8 of 103

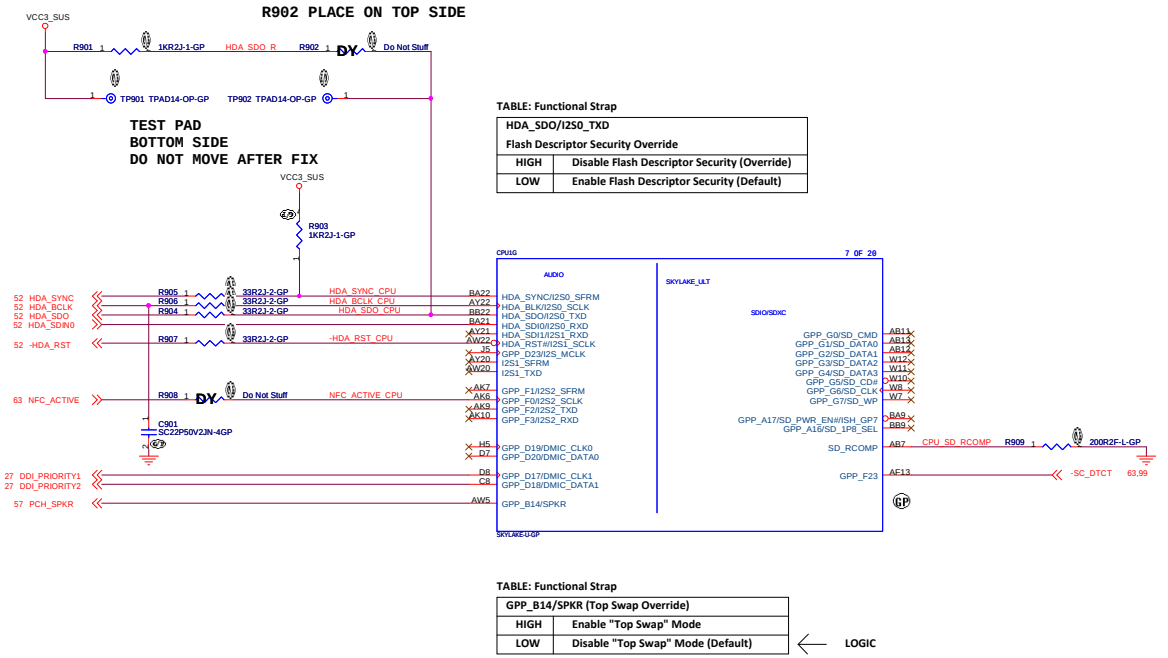


TABLE: Functional Strap

HDA_SDO/I2S0_TXD Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

TABLE: Functional Strap

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" Mode
LOW	Disable "Top Swap" Mode (Default)

← LOGIC

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(7/16) : AUDIO/SDXC

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 9 of 103

Flexible I/O Configuration			
I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3 1	USB3 1	USB3P0
Port 2	USB3 2/SSIC	USB3 2	USB3P1
Port 3	USB3 3	USB3 3	USB3P2
Port 4	USB3 4	USB3 4	USB3P3
Port 5	USB3 5/PCIE 1	PCIE 1 (x4)	PCIE0_L0
Port 6	USB3 6/PCIE 2	PCIE 2 (x4)	PCIE0_L1
Port 7	PCIE 3 (GbE)	PCIE 3 (x4)	PCIE0_L2
Port 8	PCIE 4 (GbE)	PCIE 4 (x4)	PCIE0_L3
Port 9	PCIE 5 (GbE)	PCIE 5 (GbE)	PCIE4
Port 10	PCIE 6	PCIE 6	PCIE5
Port 11	PCIE 7/SATA 0	PCIE 7 (x2)	PCIE6_L1
Port 12	PCIE 8/SATA 1A	GPIO STRAP	PCIE6_L0_SATA1
Port 13	PCIE 9 (GbE)	PCIE 9 (x2)	PCIE8_L1
Port 14	PCIE 10 (GbE)	PCIE 10 (x2)	PCIE8_L0
Port 15	PCIE 11/SATA 1B	PCIE 11 (x2)	PCIE10_L0
Port 16	PCIE 12/SATA 2	GPIO STRAP	PCIE10_L1_SATA2

PCIe Port Assignment	
0 (x4)	dGPU
4	Gbe PHY
5	M.2 WLAN Slot Port0
6(x2)	Optane x2 or M.2 WLAN slot Port1 x1
8(x2)	Alpine Ridge-LP
10 (x2)	Main Storage x2

SATA Port Assignment	
0	(PCIE 7)
1A	SATA SSD on WWAN slot
1B	(PCIE11)
2	SATA SSD Main Storage

USB Port Assignment	
0	USB 3.0 System Port (AOU)
1	USB 3.0 System Port (Debug)
2	Smart Card Reader
3	USB 3.0 System Port(SUB) /DOCK
4	IR camera
5	WWAN Card
6	M.2 WLAN Slot for BT
7	USB Camera
8	Fingerprint Reader
9	Touch Panel

USB 3.0 Port Assignment	
0	USB 3.0 System Port (AOU)
1	USB 3.0 System Port
2	Media Card controller
3	USB 3.0 System Port(SUB) /DOCK
4	(PCIE 1)
5	(PCIE 2)

close to CPU

Reserve for LSZ2

Pericom PI3PCIE3212ZBE 071.33212.0003
NXP CBTL02043ABQ 071.02043.0003
TOSHIBA TC7PCI3212MT 071.73212.0003

Pericom PI3USB102ZME 73.3US10.D03
NXP NX3DV42GU 073.00342.003

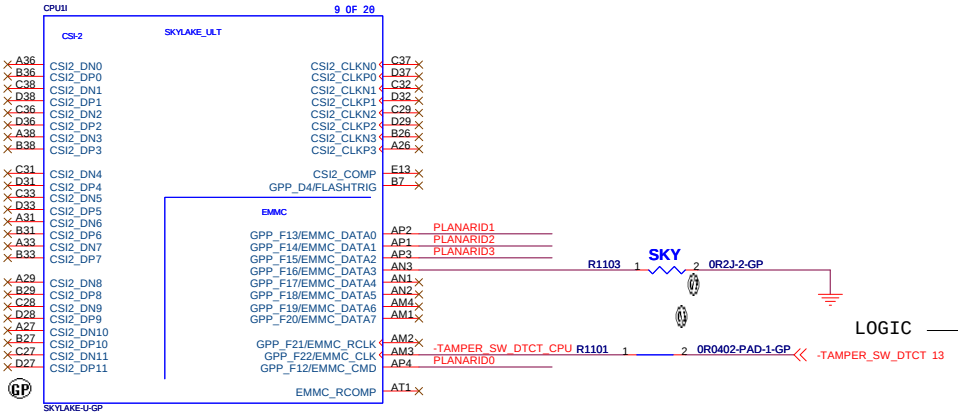
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(8/16) : PCIE/USB/SATA

Size	Document Number	Rev
A2	TS1	1

Date: Thursday, November 03, 2016 Sheet 30 of 100



TABLE

LEVEL	PLANAR ID			
	3	2	1	0
	R1106	R1107	R1108	R1109
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

TABLE

LEVEL	PLANARID[3..0]		
	UMA	GeForce (N16S-GTR)	Quadro(N17M-Q1)
SDV	0000B	0001B	0010B
FVT1/FVT2	0011B	0100B	0101B
SIT/SIT2	0110B	0111B	1000B
SVT	1001B	1010B	1011B
MP	1100B	1101B	1110B

TABLE

	R1103
Kabylake	DY
Skylake	ASM

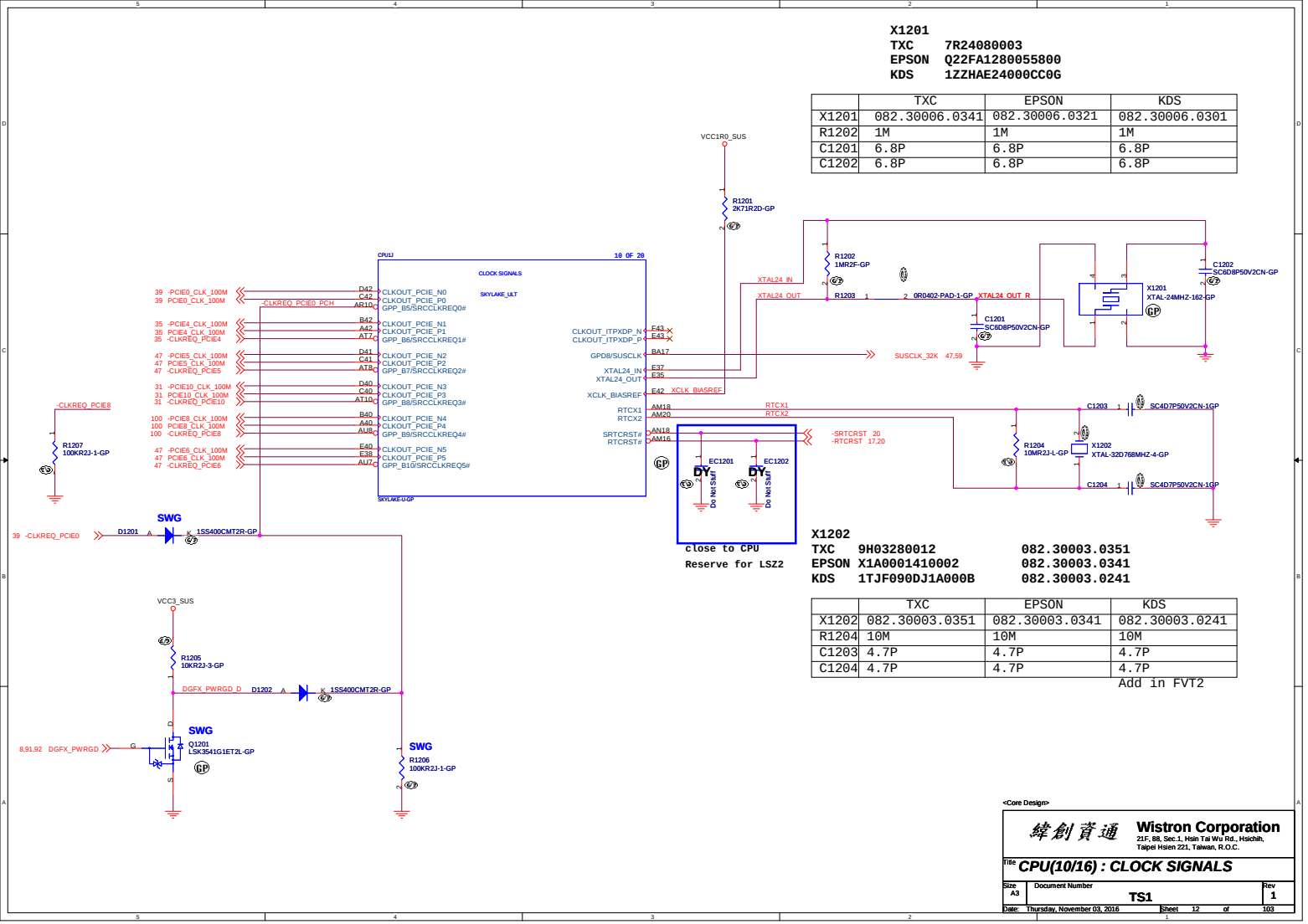
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU(9/16) : CSI-2/EMMC***

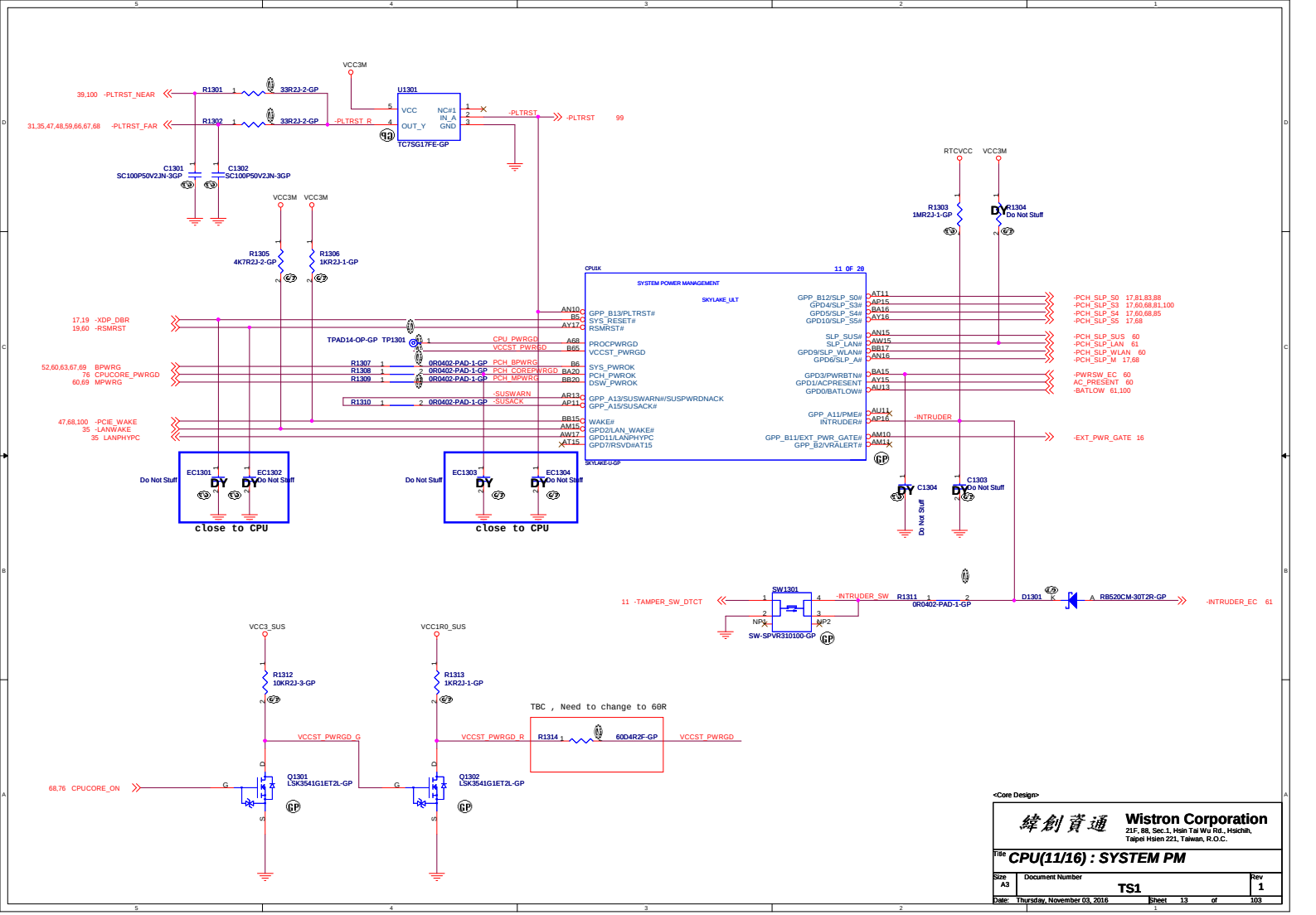
Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 11 of 103



	TXC	EPSON	KDS
X1201	082.30006.0341	082.30006.0321	082.30006.0301
R1202	1M	1M	1M
C1201	6.8P	6.8P	6.8P
C1202	6.8P	6.8P	6.8P

	TXC	EPSON	KDS
X1202	082.30003.0351	082.30003.0341	082.30003.0241
R1204	10M	10M	10M
C1203	4.7P	4.7P	4.7P
C1204	4.7P	4.7P	4.7P



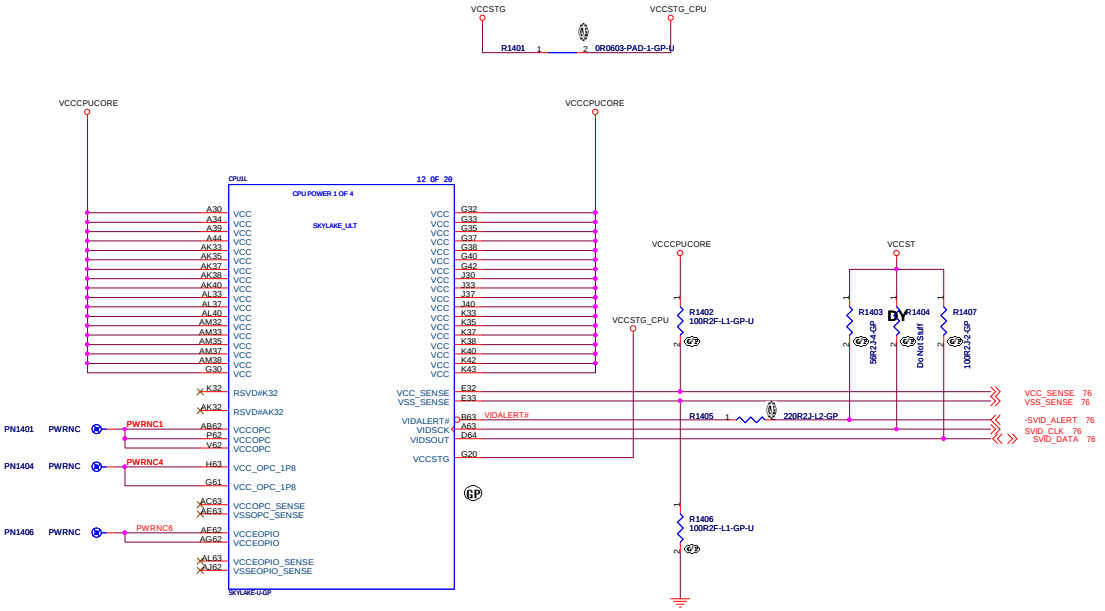
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(11/16) : SYSTEM PM

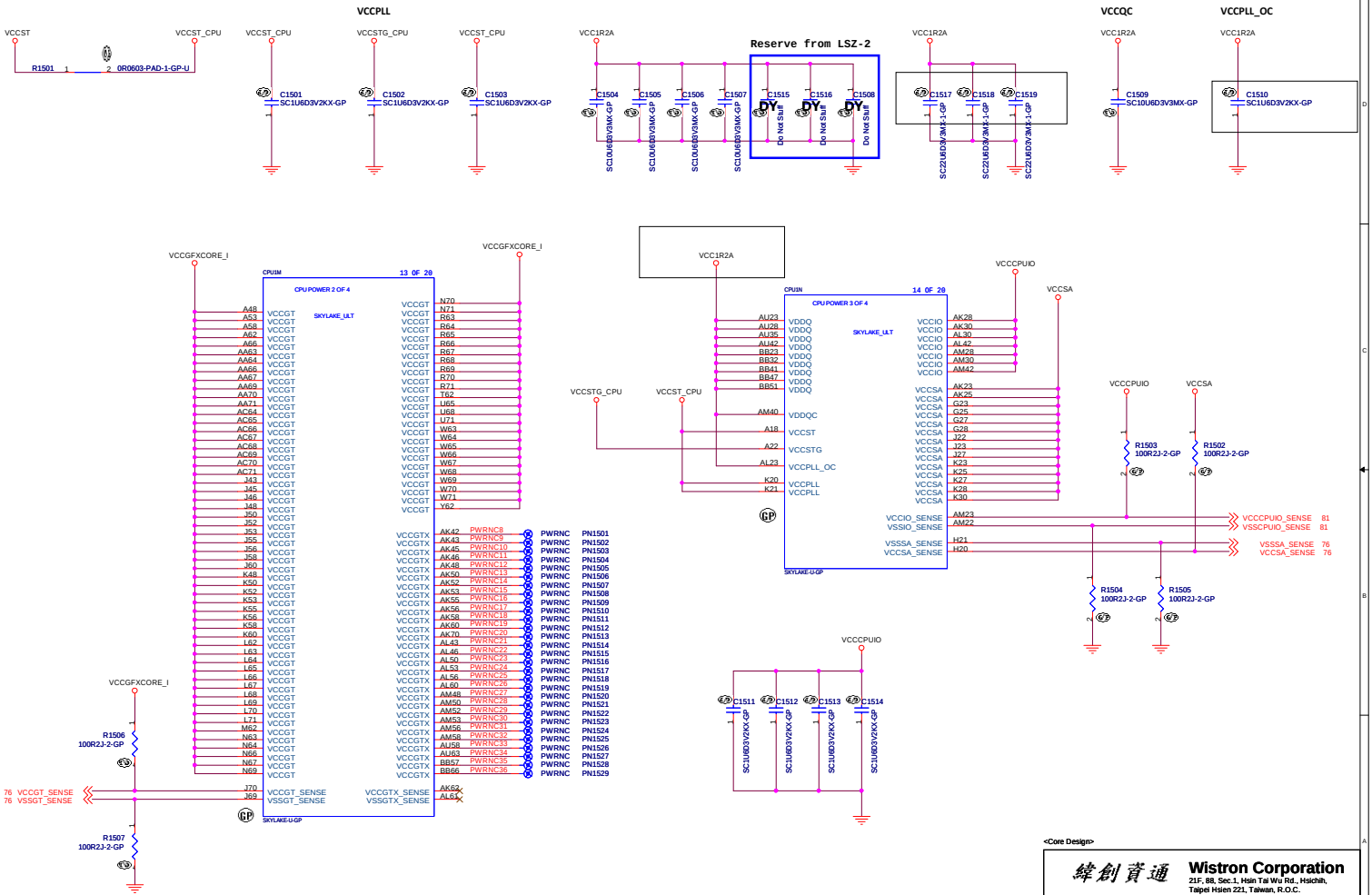
Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 13 of 103



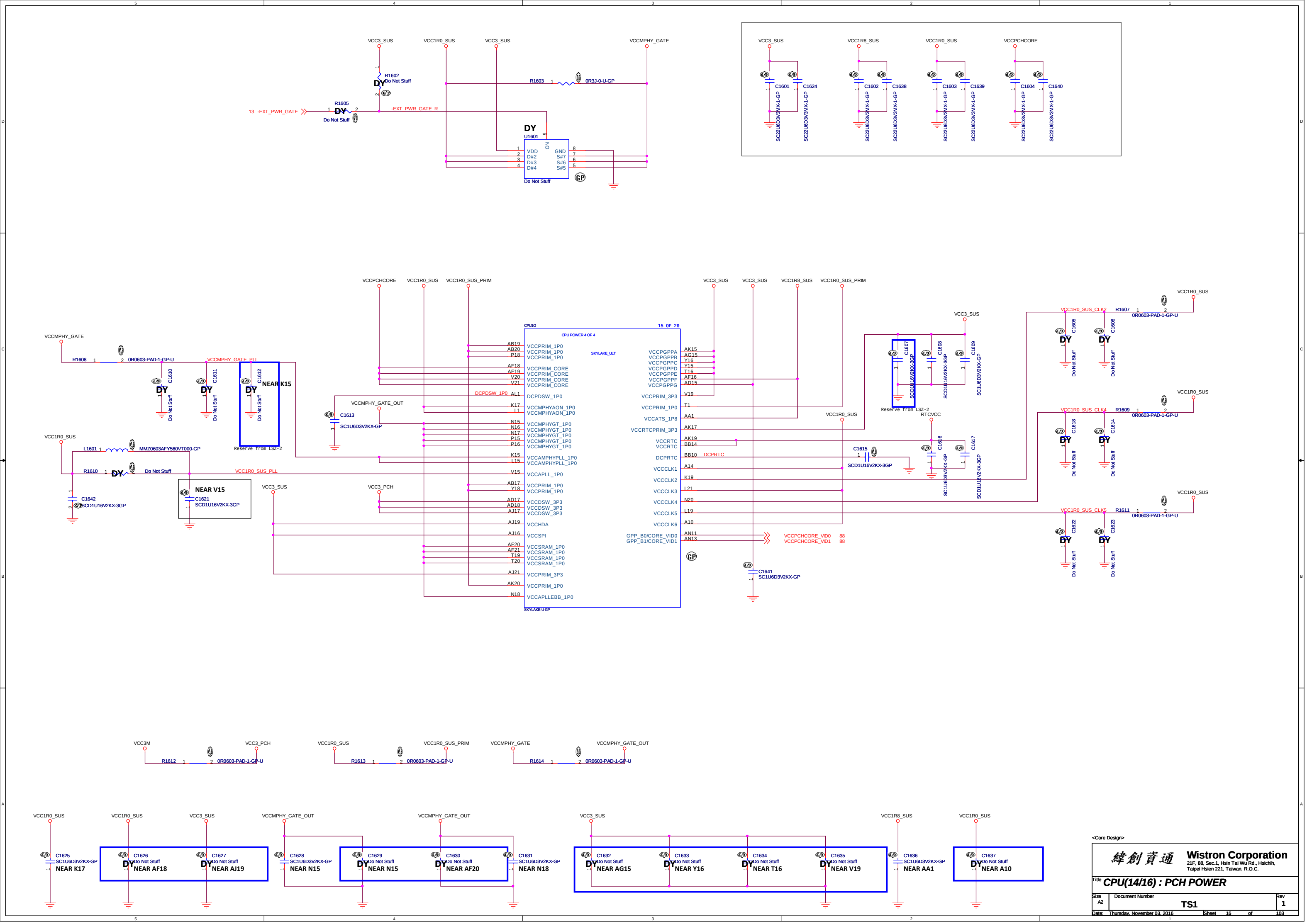
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CPU(12/16) : CPU POWER(1/2)***
Size: A3	Document Number: **TS1**
Rev: 1	
Date: Thursday, November 03, 2016	Sheet 14 of 103

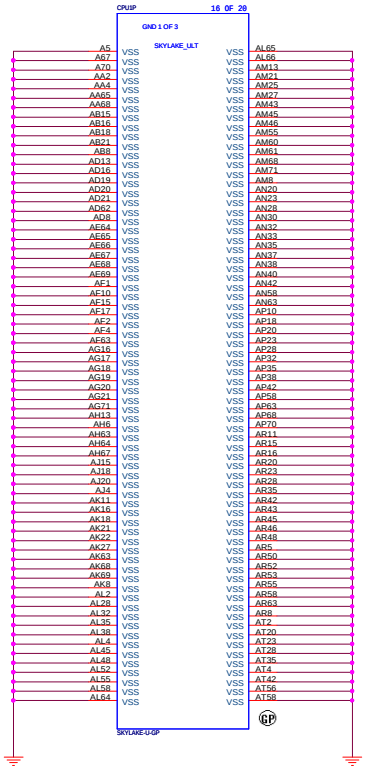


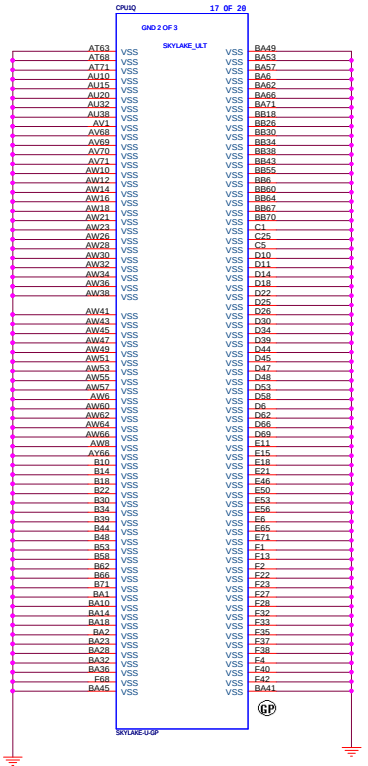
<Core Design>

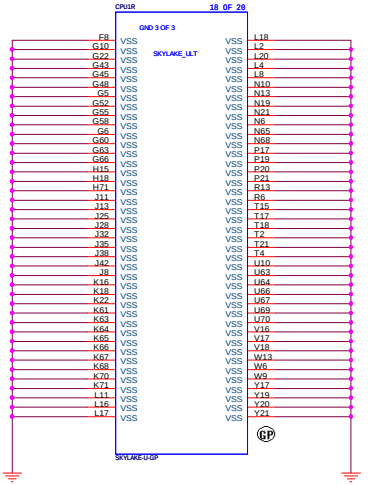
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CPU(13/16) : CPU POWER(2/2)***
Size: A3	Document Number: TS1
Rev: 1	
Date: Thursday, November 03, 2016	Sheet 15 of 103



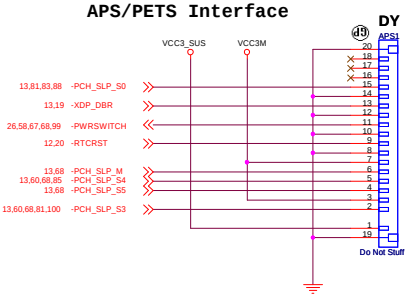
VCC3_SUS
VCC1R0_SUS
VCCMPHY_GATE
R1602
Do Not Stuff
DY
R1603
0R3J-0-U-GP
R1605
13 -EXT_PWR_GATE
-EXT_PWR_GATE_R
U1601
VDD
D#2
D#3
D#4
GND
S#7
S#6
S#5
ON
VCC1R8_SUS
VCCPCHCORE
C1601
C1624
C1602
C1638
C1603
C1639
C1604
C1640
SC22U6D3V3MX-1-GP
VCC1R0_SUS_PRIM
CPU1D
CPU POWER 4 OF 4
SKYLAKE_ULT
15 OF 20
VCCPRIM_1P0
VCCPRIM_CORE
DCPDSW_1P0
VCCMPHYAON_1P0
VCCMPHYGT_1P0
VCCAMPHYPLL_1P0
VCCAPLL_1P0
VCCDSW_3P3
VCCHDA
VCCSPI
VCCSRAM_1P0
VCCPRIM_3P3
VCCAPLLEBB_1P0
VCCPGPPA
VCCPGPPB
VCCPGPPC
VCCPGPPD
VCCPGPPE
VCCPGPPF
VCCPGPPG
VCCATS_1P8
VCCRTCPRIM_3P3
VCCRTC
DCPRTC
VCCCLK1
VCCCLK2
VCCCLK3
VCCCLK4
VCCCLK5
VCCCLK6
GPP_B0/CORE_VID0
GPP_B1/CORE_VID1
VCCPCHCORE_VID0 88
VCCPCHCORE_VID1 88
SKYLAKE-U-GP
R1608
0R0603-PAD-1-GP-U
VCCMPHY_GATE_PLL
C1610
C1611
C1612
NEAR K15
Reserve from LSZ-2
L1601
MMZ0603AFY560VT000-GP
R1610
VCC1R0_SUS_PLL
C1642
SCD1U16V2KX-3GP
NEAR V15
C1621
VCCMPHY_GATE_OUT
C1613
SC1U6D3V2KX-GP
VCC3_PCH
RTCVCC
C1607
C1608
C1609
C1615
C1616
C1617
C1641
SC1U6D3V2KX-GP
VCC1R0_SUS_CLK2
VCC1R0_SUS_CLK4
VCC1R0_SUS_CLK5
R1607
R1609
R1611
C1605
C1606
C1618
C1614
C1622
C1623
VCC3M
R1612
R1613
R1614
C1625
NEAR K17
C1626
NEAR AF18
C1627
NEAR AJ19
C1628
NEAR N15
C1629
C1630
NEAR AF20
C1631
SC1U6D3V2KX-GP
NEAR N18
C1632
NEAR AG15
C1633
NEAR Y16
C1634
NEAR T16
C1635
NEAR V19
C1636
NEAR AA1
C1637
NEAR A10
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title CPU(14/16) : PCH POWER
Size A2
Document Number TS1
Rev 1
Date: Thursday, November 03, 2016
Sheet 16 of 103







APS/PETS Interface



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

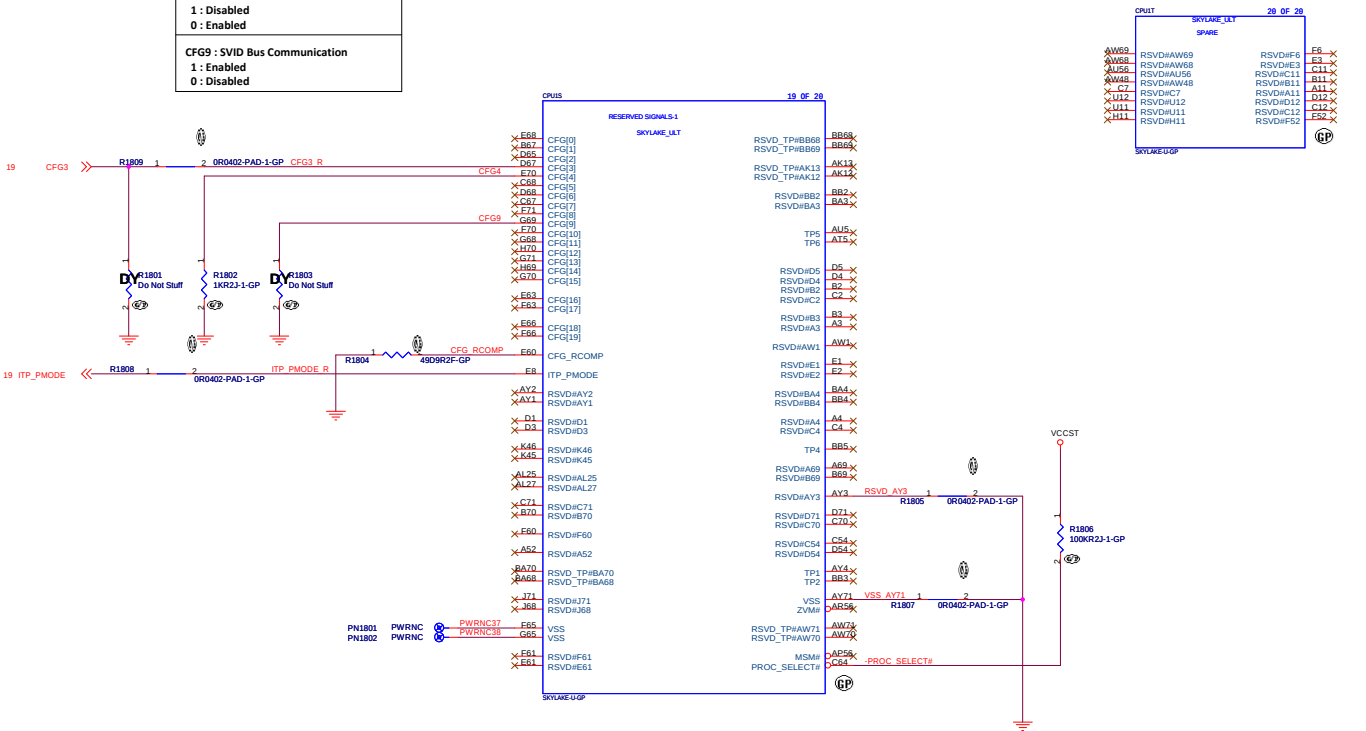
Title: **CPU(15/16) : GND**

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 17 of 103

TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted **1 : No Stall** **0 : Stall**
CFG3 : MSR Privacy Bit Feature **1 : MSR (C80h) bit[0] setting** **0 : MSR (C80h) bit[0] overridden**
CFG4 : eDP Enable **1 : Disabled** **0 : Enabled**
CFG9 : SVID Bus Communication **1 : Enabled** **0 : Disabled**



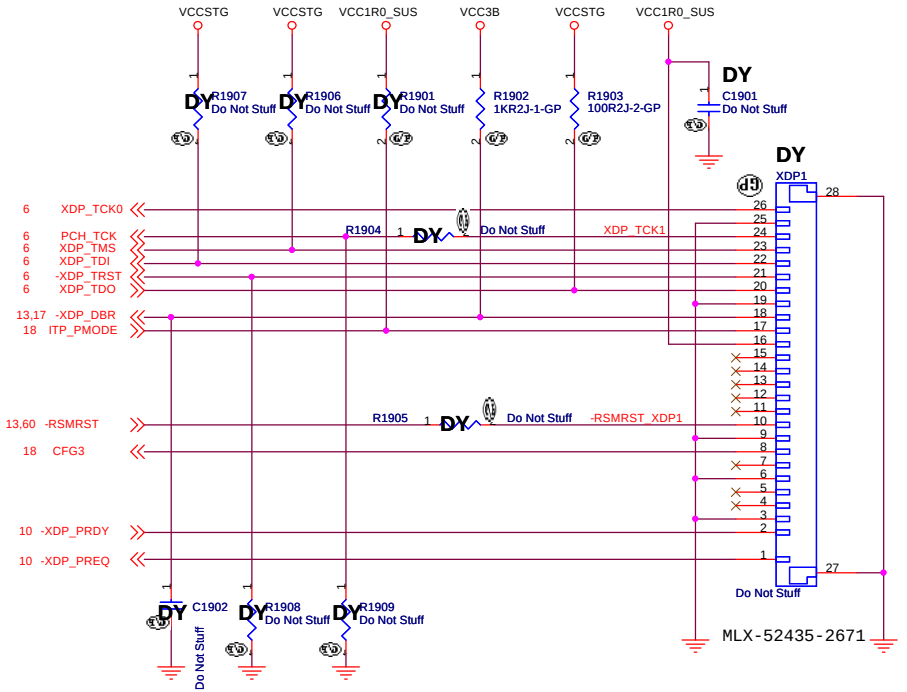
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(16/16) : CFG/RESERVED**

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 18 of 103



TABLE

Logic	Ref Des	Merged	DCI 2.0
Page 7	R712	ASM	NO_ASM
Page 18	R1801	ASM	NO_ASM
Page 19	XDP1	ASM	NO_ASM
	C1901	ASM	NO_ASM
	R1901	ASM	NO_ASM
	R1902	ASM	ASM
	R1903	ASM	ASM
	R1904	ASM	NO_ASM
	R1905	ASM	NO_ASM

LOGIC

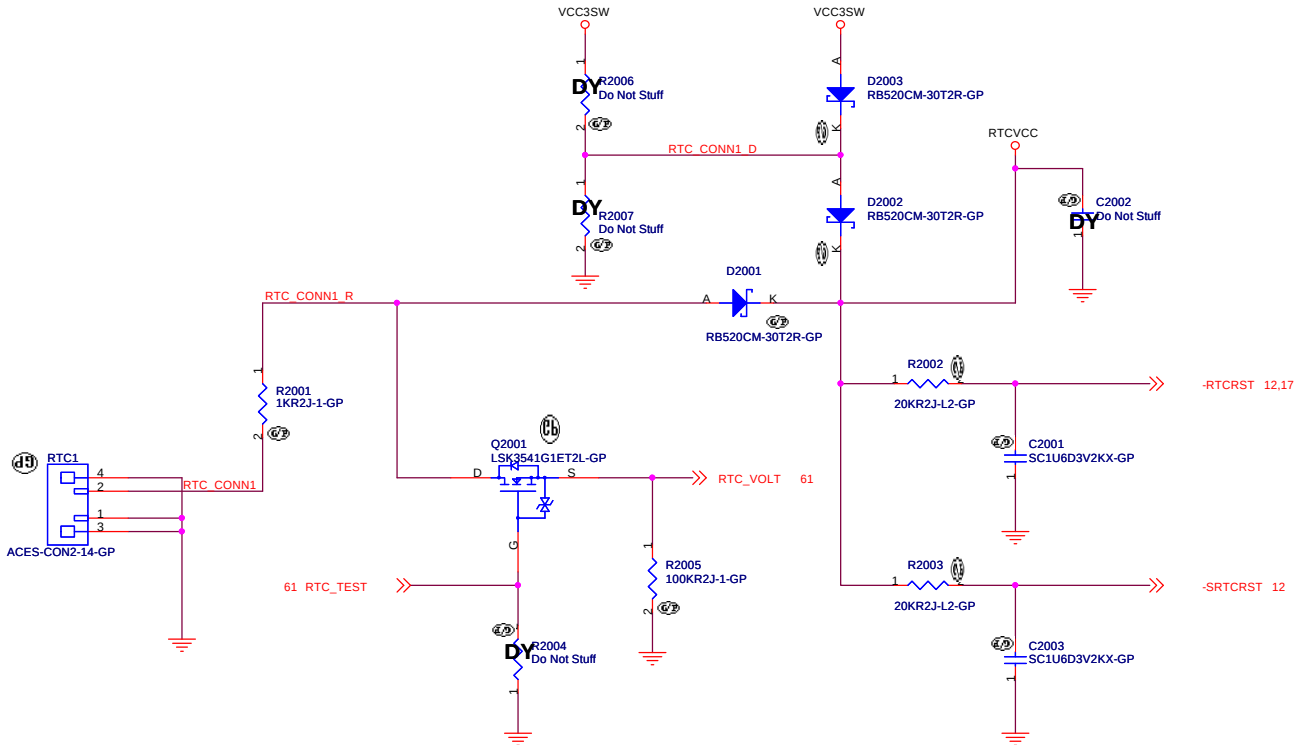
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **XDP CONNECTOR**

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 19 of 103



for test point, page 91

RTC_CONN1 RTC_CONN1 99

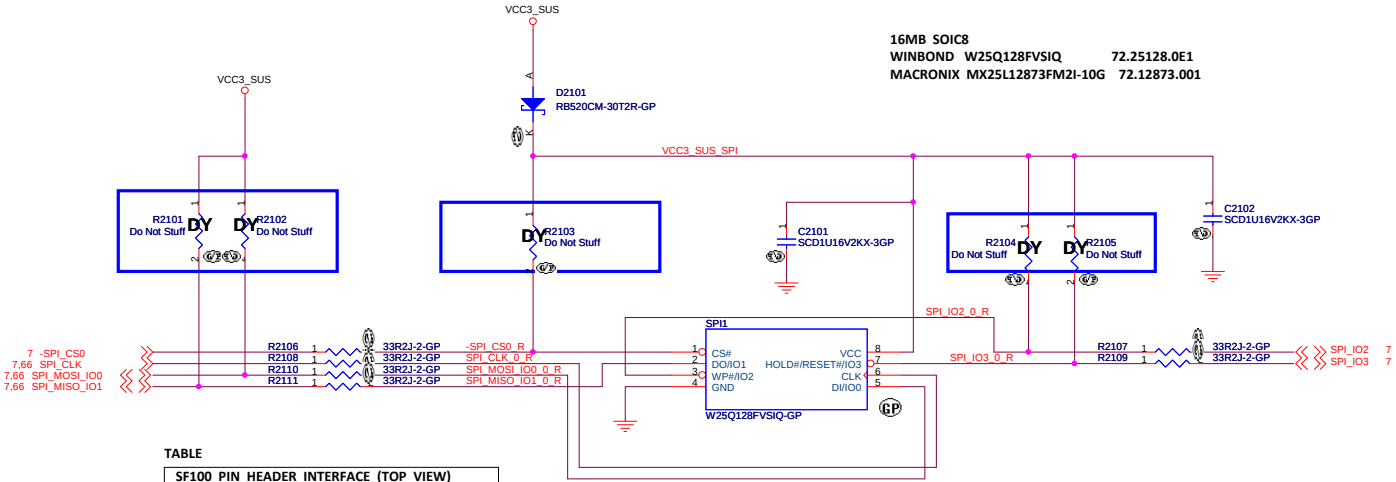
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **RTC BATTERY**

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 20 of 103



16MB SOIC8
WINBOND W25Q128FVSIQ 72.25128.0E1
MACRONIX MX25L12873FM2I-10G 72.12873.001

TABLE

SF100 PIN HEADER INTERFACE (TOP VIEW)					
1	VCC	D2101.K	GND	GND	2
3	CS#	R2104.2	R2106.2	CLK	4
5	MISO	R2109.2	R2108.2	MOSI	6
7	(KEY)	N/A	N/A	(RESET)	8

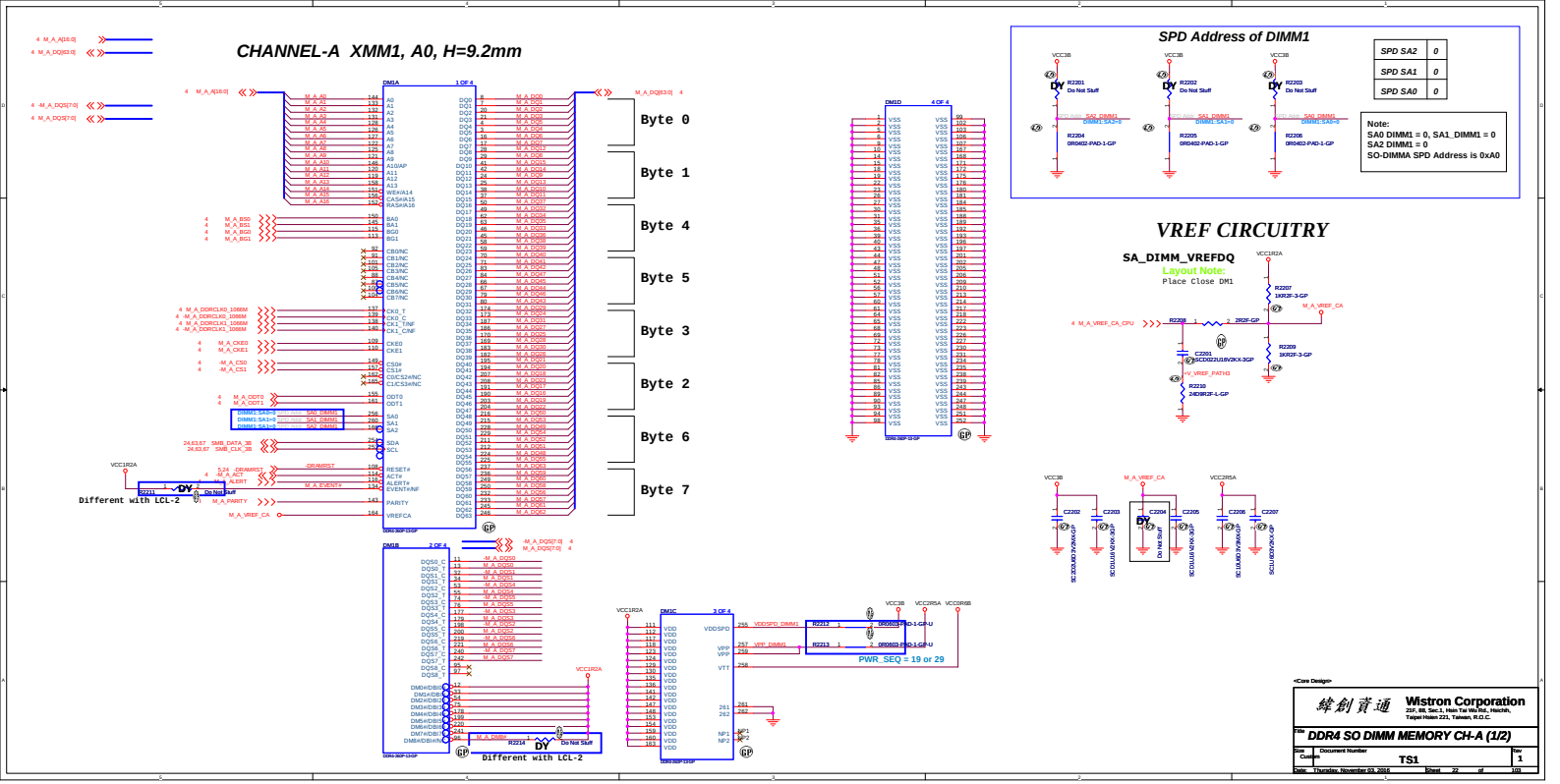
<Core Design>

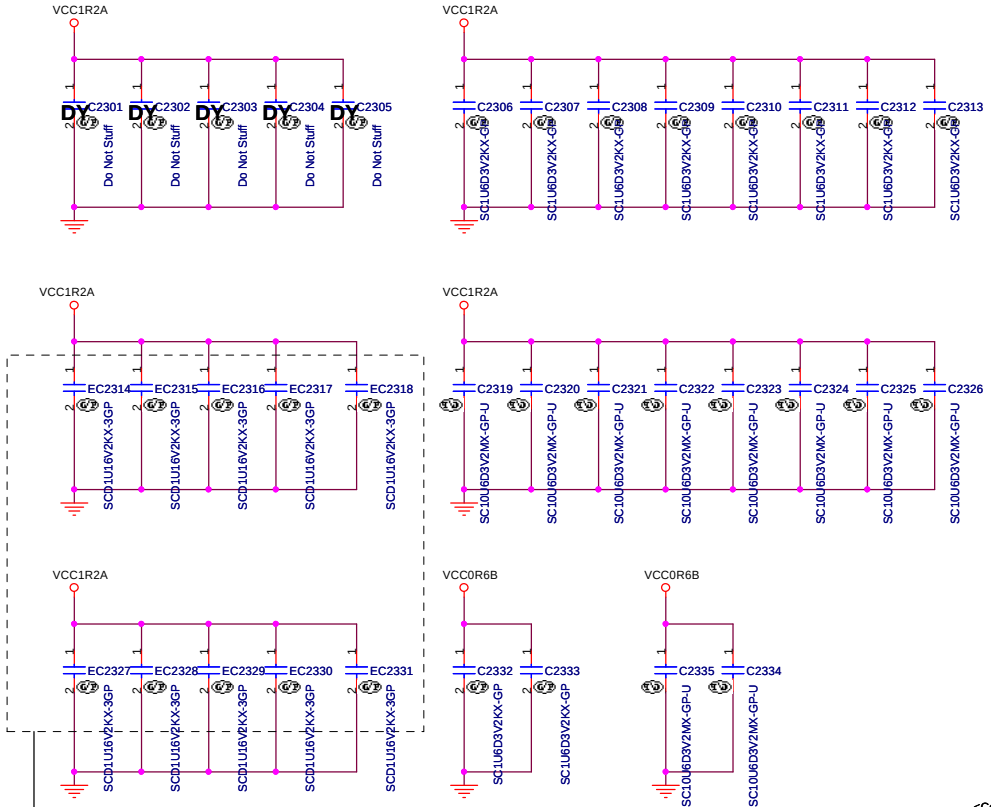
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SPI FLASH***

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 21 of 103


CHANNEL-A XMM1, A0, H=9.2mm
SPD Address of DIMM1
SPD SA2 0
SPD SA1 0
SPD SA0 0
Note:
SA0 DIMM1 = 0, SA1_DIMM1 = 0
SA2 DIMM1 = 0
SO-DIMMA SPD Address is 0xA0
VREF CIRCUITRY
SA_DIMM_VREFDQ
Layout Note:
Place Close DM1
Byte 0
Byte 1
Byte 4
Byte 5
Byte 3
Byte 2
Byte 6
Byte 7
Different with LCL-2
PWR_SEQ = 19 or 29
Wistron Corporation
DDR4 SO DIMM MEMORY CH-A (1/2)
TS1



ASM from EMI request.

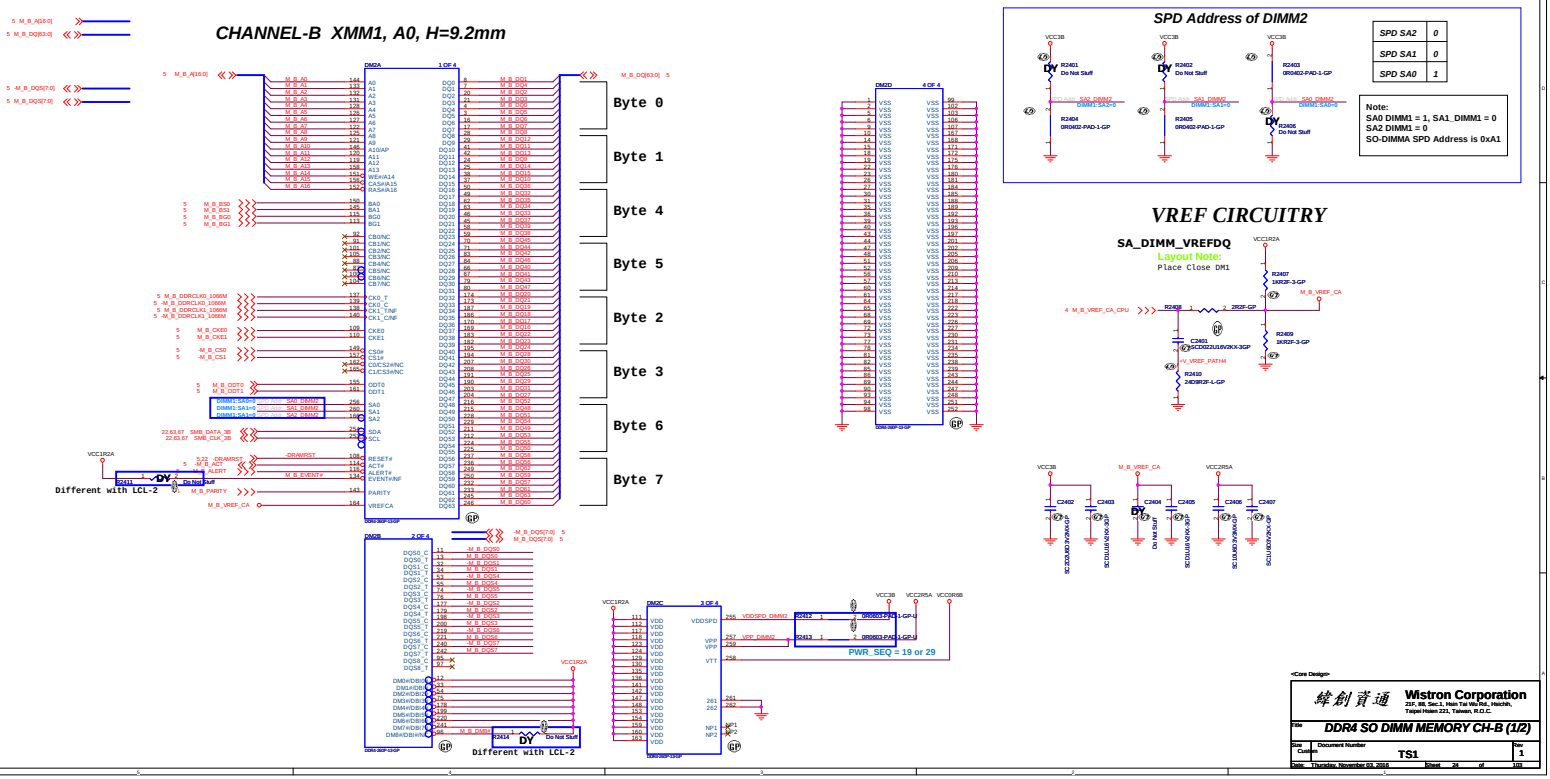
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR4 SO DIMM MEMORY CH-A (2/2)

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 23 of 103

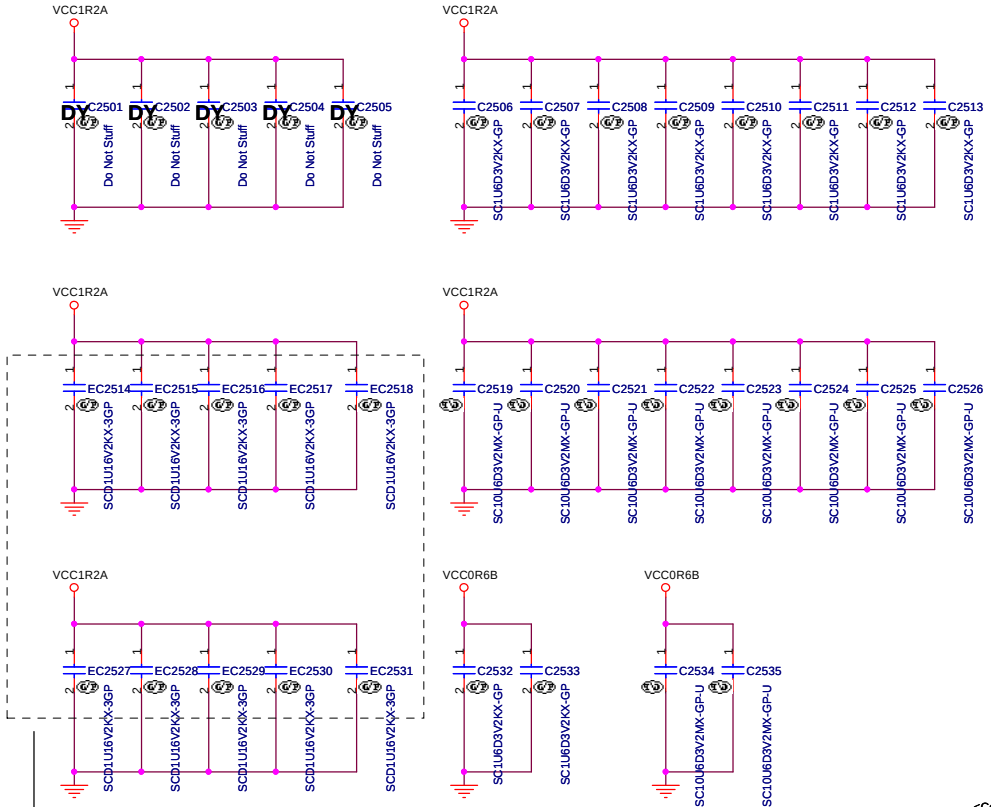


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR4 SO DIMM MEMORY CH-B (1/2)

Size: Custom | Document Number: TS1 | Rev: 1

Date: Thursday, November 03, 2016 | Sheet 24 of 103



ASM from EMI request.

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR4 SO DIMM MEMORY CH-B (2/2)***

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 25 of 103

LCD CONN

Q2601		
Vendor	Venor PN	Wistron PN
Rohm	RF4E070GN (1st source)	084.4E070.0037
Fairchild	FDMA7672 (2nd source)	084.07672.M001

0.9A

1.2A

LCD CONNECTOR

LCD1

ME-CON40-7-GP

020.K0144.0040

TABLE:

TP_EN	
HIGH	Enable Touch Panel
LOW	Disable Touch Panel

PLACE NEAR U2601

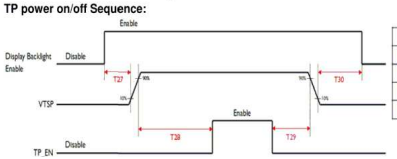
for test point, page 91

Change for HL DY

Change for HL

Near LCD CONN: LCD1 (P.91)

TP power on/off Sequence:



	Min	Max
T27	10ms	-
T28	20ms	-
T29	2ms	-
T30	100ms	-

Power BTN

<Core Design>

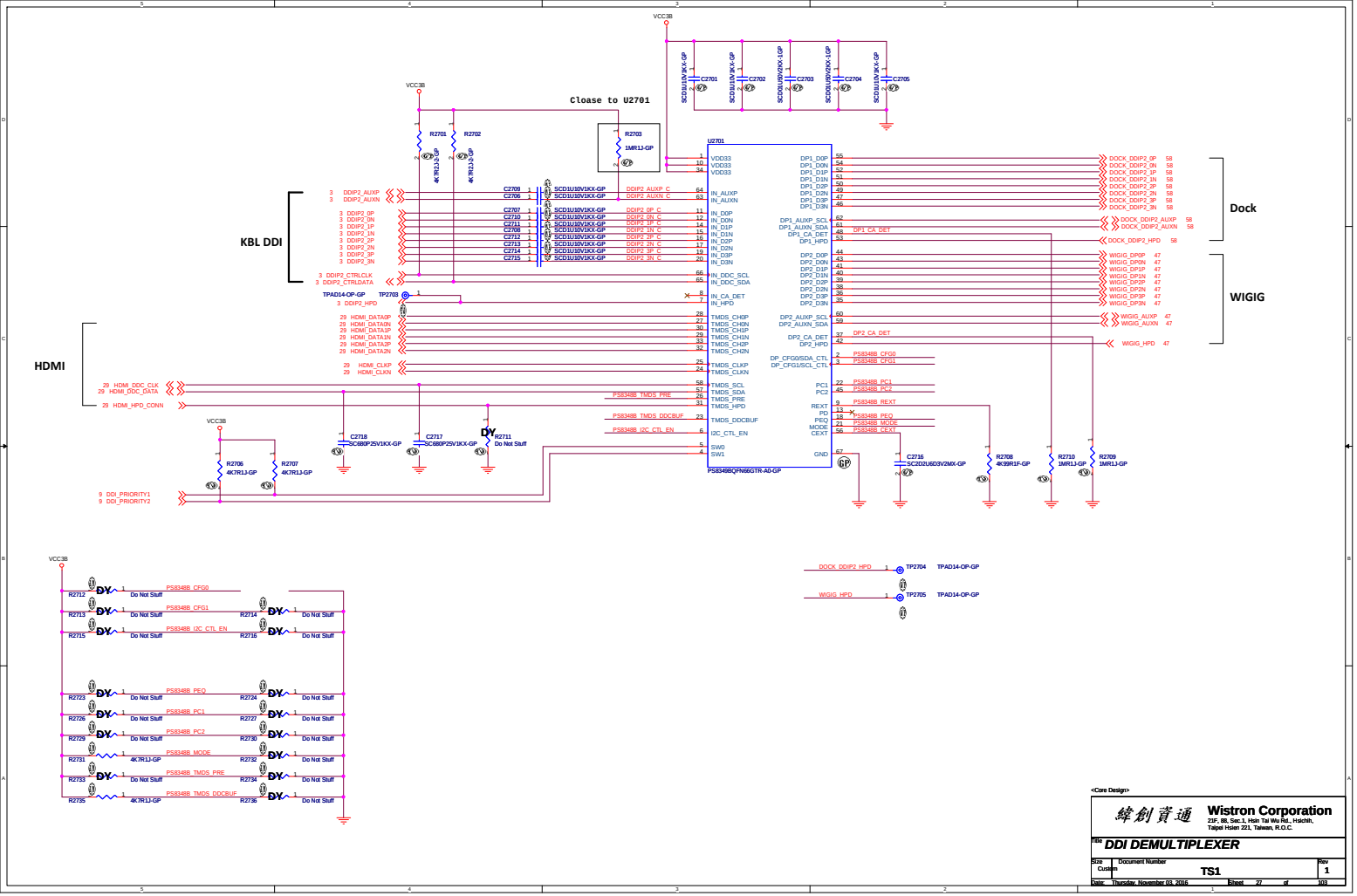
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/LID/MIC/CAMERA/PWR SW

Size	Document Number	Rev
A2	TS1	1

Date: Thursday, November 03, 2016 Sheet 26 of 100



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDI DEMULTIPLEXER

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 27 of 103

BLANK

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BLANK***	
Size: A	Document Number: **TS1**	Rev: **1**
Date: Thursday, November 03, 2016	Sheet 28 of 103	

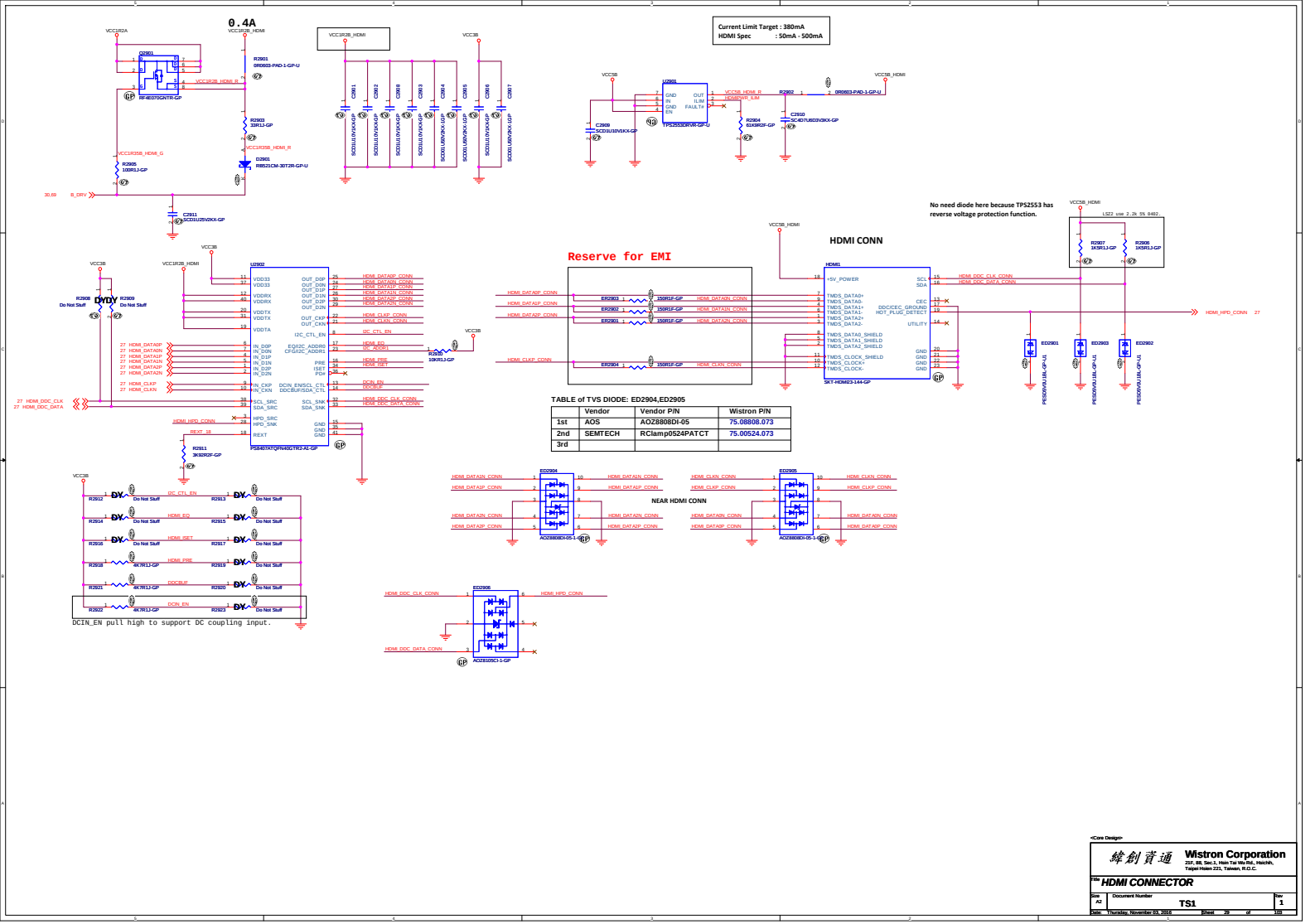


TABLE of TVS DIODE: ED2904,ED2905

	Vendor	Vendor P/N	Wistron P/N
1st	AOS	AOZ8808DI-05	75.08808.073
2nd	SEMTECH	RClamp0524PATCT	75.00524.073
3rd			

<Core Design>

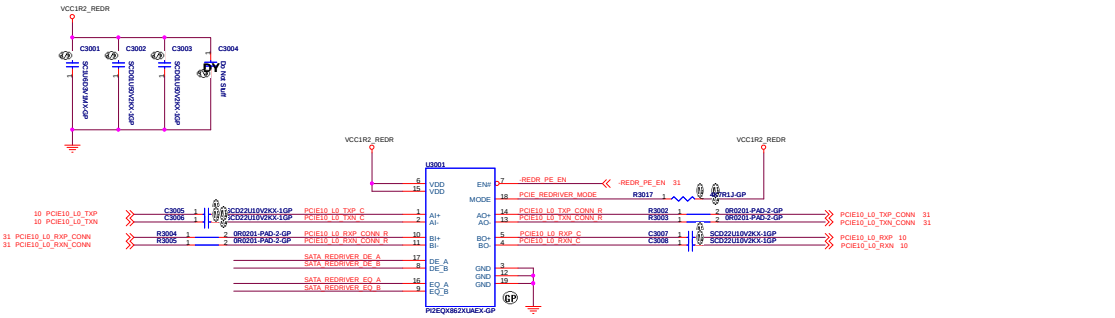
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI CONNECTOR

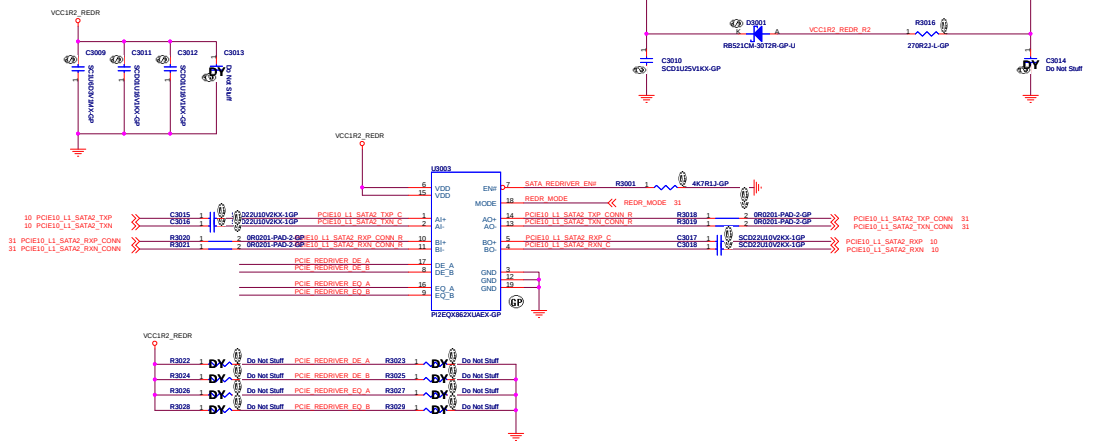
Size	Document Number	Rev
A2	TS1	1

Date: Thursday, November 03, 2016 Sheet 29 of 100

FOR PCIE ONLY



FOR SATA/PCIE



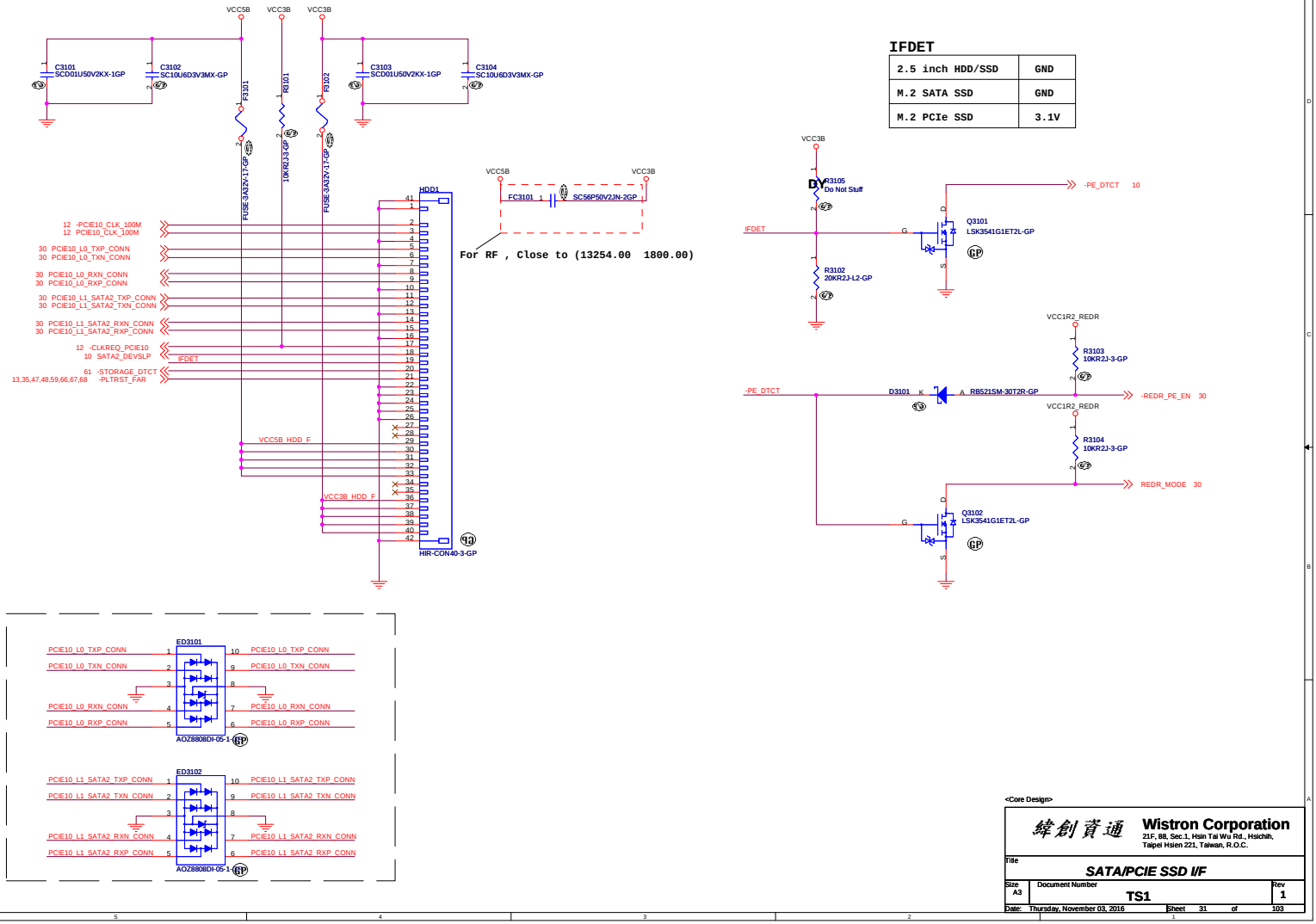
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: STORAGE I/F REDRIVER

Size	Document Number	Rev
C	TS1	1

Date: Thursday, November 03, 2016 Sheet 30 of 103



IFDET

2.5 inch HDD/SSD	GND
M.2 SATA SSD	GND
M.2 PCIe SSD	3.1V

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SATA/PCIE SSD I/F**

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 31 of 103

BLANK

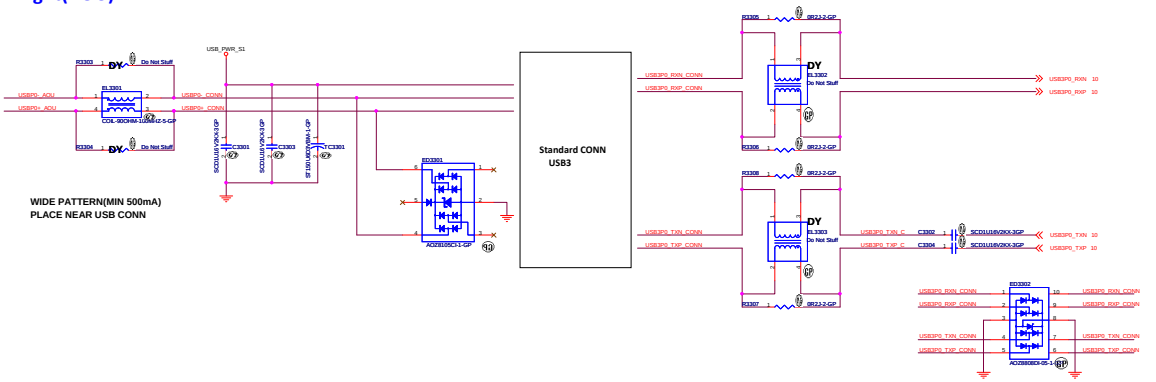
<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BLANK***	
Size: A	Document Number: **TS1**	Rev: **1**
Date: Thursday, November 03, 2016	Sheet 32 of 103	

Port1: Right(AOU)



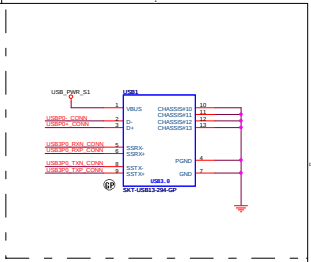
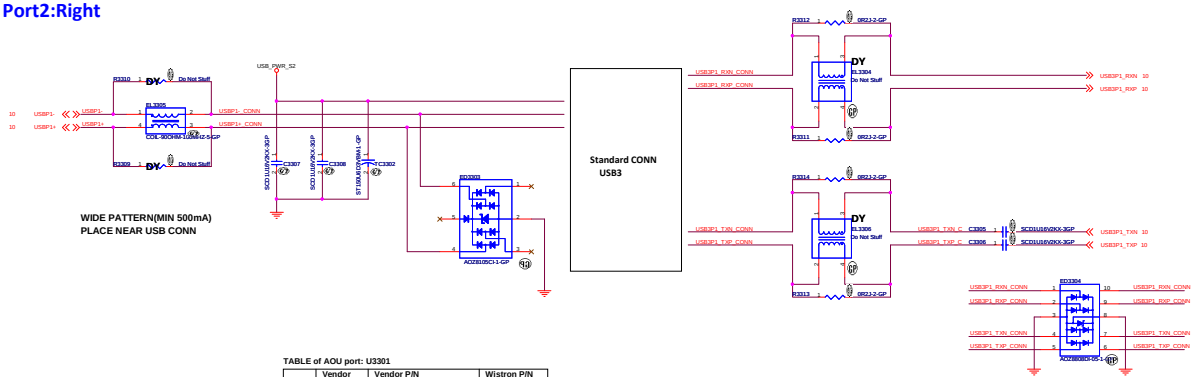


TABLE of TVS DIODE: ED3302

	Vendor	Vendor P/N	Wistron P/N
1st	AOS	AOZ8808DI-05	75.08808.073
2nd	SEMTECH	RClamp0524PATCT	75.00524.073
3rd			

Port2:Right



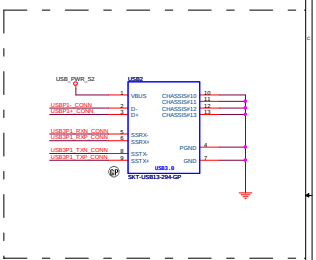
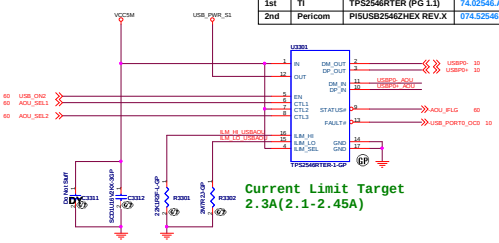


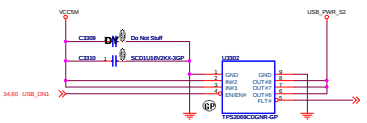
TABLE of TVS DIODE: ED3304

	Vendor	Vendor P/N	Wistron P/N
1st	AOS	AOZ8808DI-05	75.08808.073
2nd	SEMTECH	RClamp0524PATCT	75.00524.073
3rd			

TABLE of AOU port: U3301

	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2546RTER (PG 1.1)	74.02546.A73
2nd	Pericom	PI5USB2546ZHEX REV.X	074.52546.0A73





FOR ON BOARD SINGLE USB 3.0 CONNECTOR

Continous Current Limit 1.5A

TABLE of USB 3.0 port: U3302

	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2069CDGNR	74.02069.A79
2nd	ROHM	BD82032FVJ-GE2	74.82032.07G

<Core Design>

緯創資通 Wistron Corporation

21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB POWER/CONN		
Size: Custom	Document Number: TS1		Rev: 1
Date: Thursday, November 03, 2016		Sheet 33 of 103	

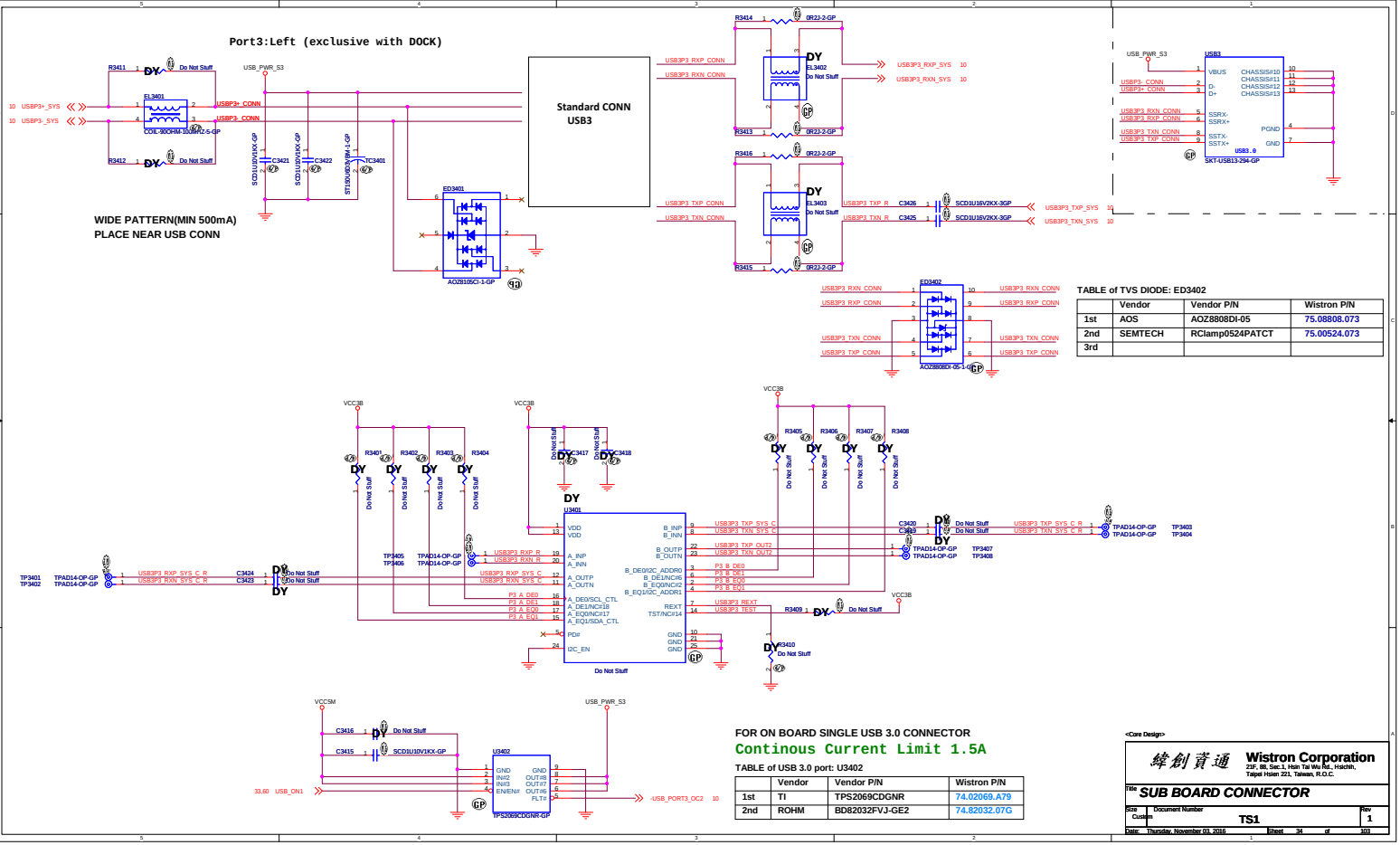


TABLE of TVS DIODE: ED3402

	Vendor	Vendor P/N	Wistron P/N
1st	AOS	AOZ8808DI-05	75.08808.073
2nd	SEMTECH	RClamp0524PATCT	75.00524.073
3rd			

FOR ON BOARD SINGLE USB 3.0 CONNECTOR

Continous Current Limit 1.5A

TABLE of USB 3.0 port: U3402

	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2069CDGNR	74.02069.A79
2nd	ROHM	BD82032FVJ-GE2	74.82032.07G

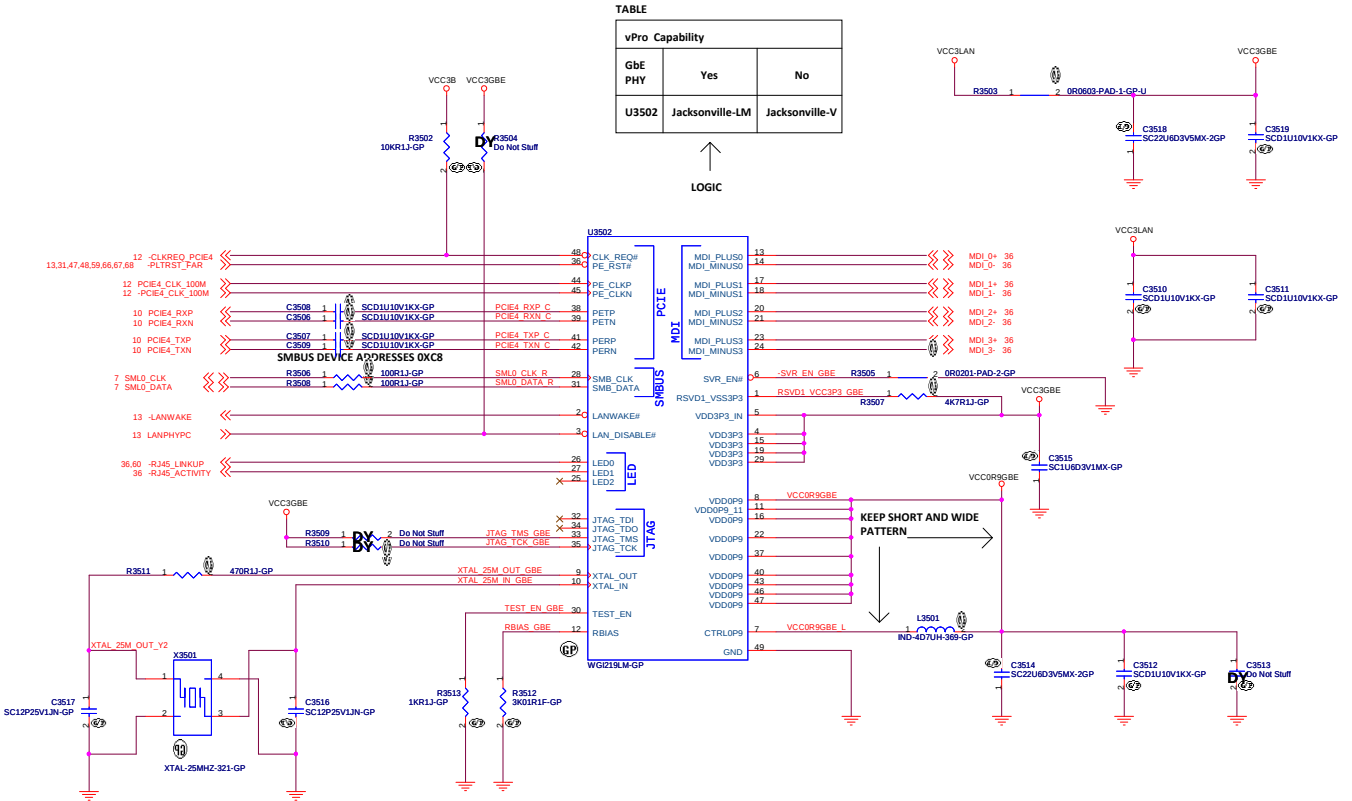
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SUB BOARD CONNECTOR

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 34 of 103



X3501

TXC 7R25080002

EPSON Q22FA1280055900

KDS 1ZZNAE25000CC0B

	TXC	EPSON	KDS
X3501	082.30005.0791	082.30006.0331	082.30005.0771
R3511	470 ohm	470 ohm	470 ohm
C3516	12P	12P	12P
C3517	12P	12P	12P

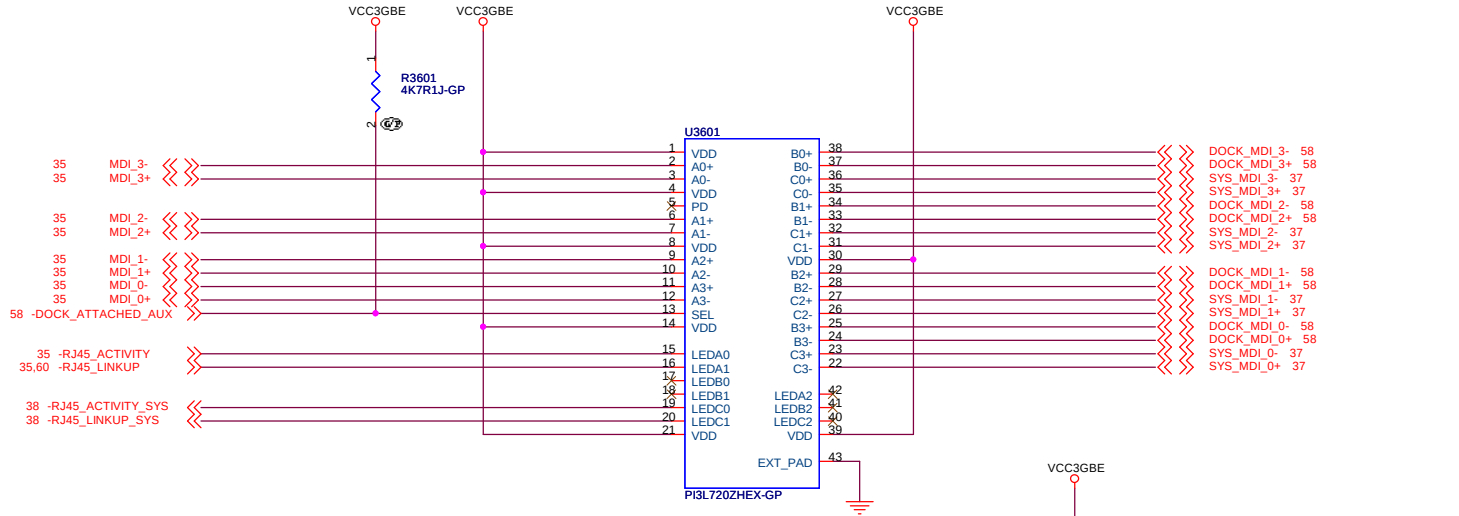
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GBE JACKSONVILLE

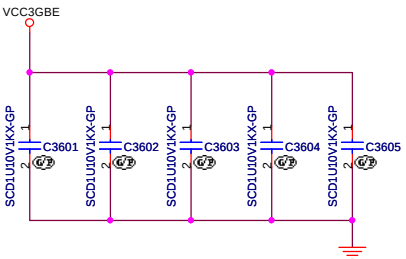
Size: A3 | Document Number: TS1 | Rev: 1

Date: Thursday, November 03, 2016 | Sheet 35 of 103



U3601

Vendor	P/N
Pericom	PI3L720ZHE
TI	TS3L501ERUAR



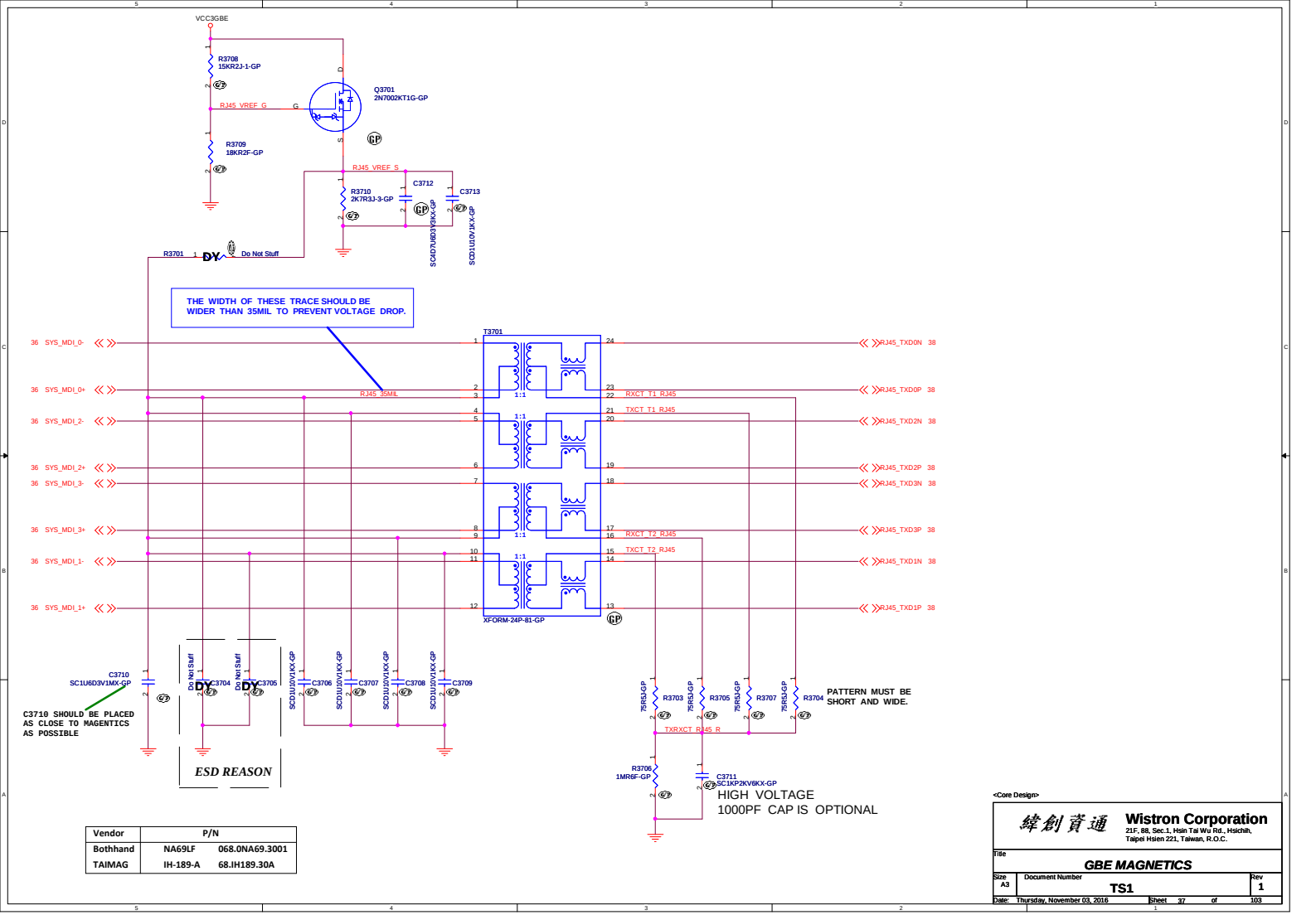
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GBE LAN Switch***

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 36 of 103



Vendor	P/N	
Bothhand	NA69LF	068.0NA69.3001
TAIMAG	IH-189-A	68.IH189.30A

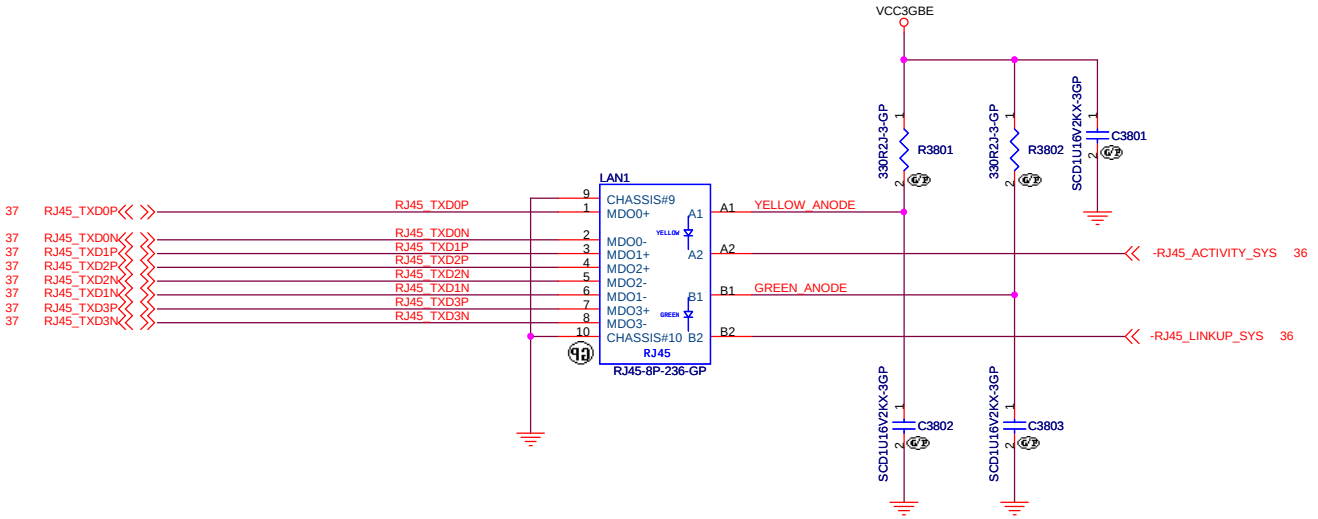
<Core Design>

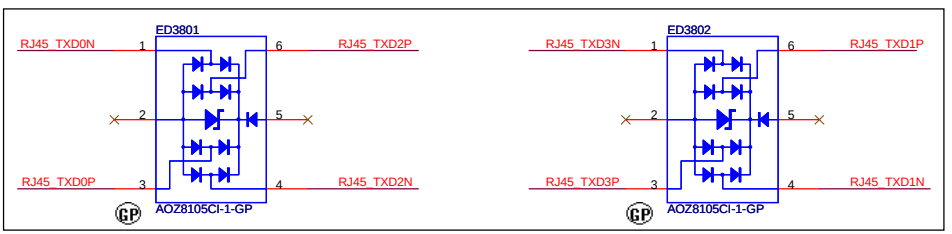
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GBE MAGNETICS**

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 37 of 103





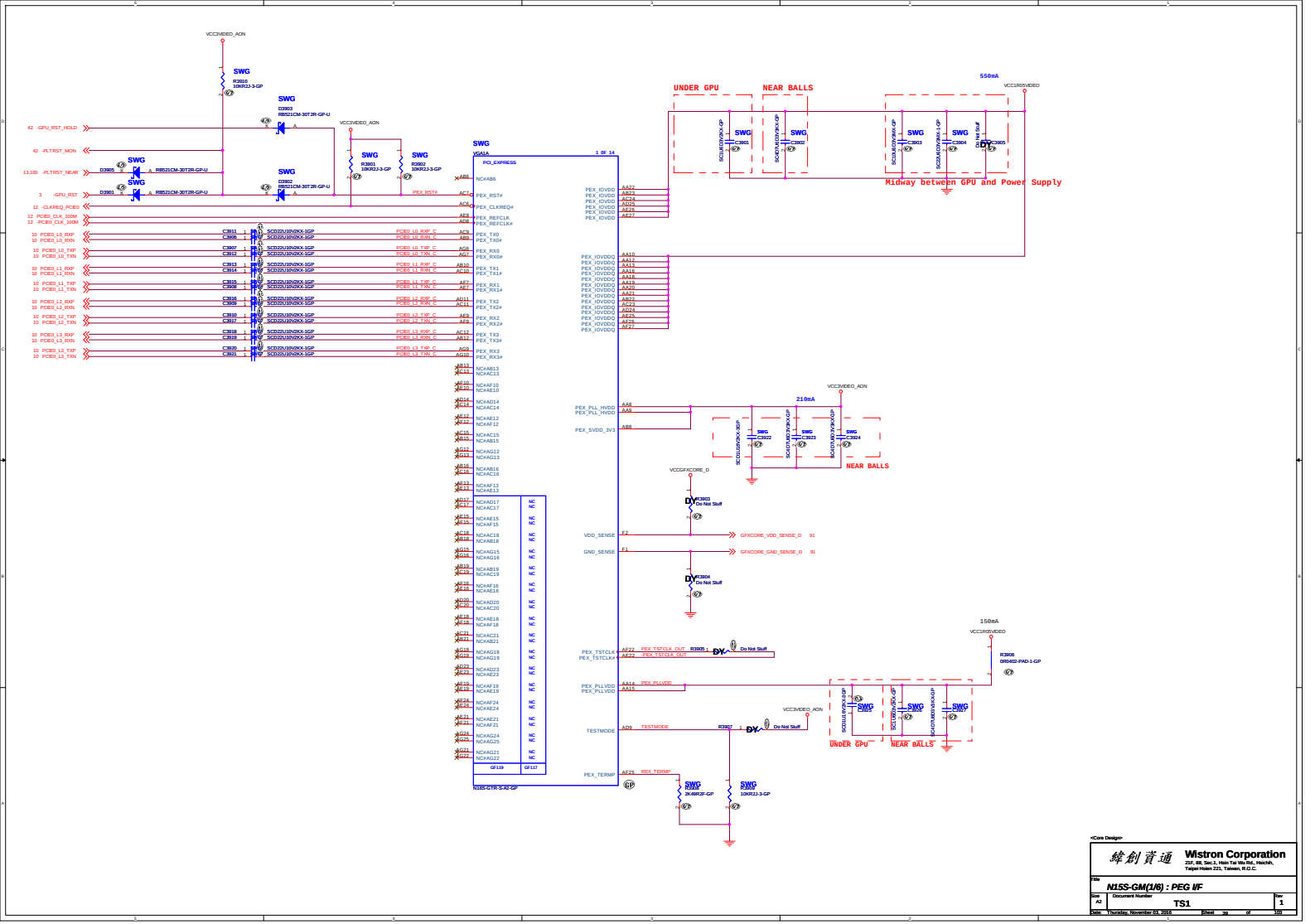
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RJ45 CONNECTOR***

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 38 of 103



<Core Design>

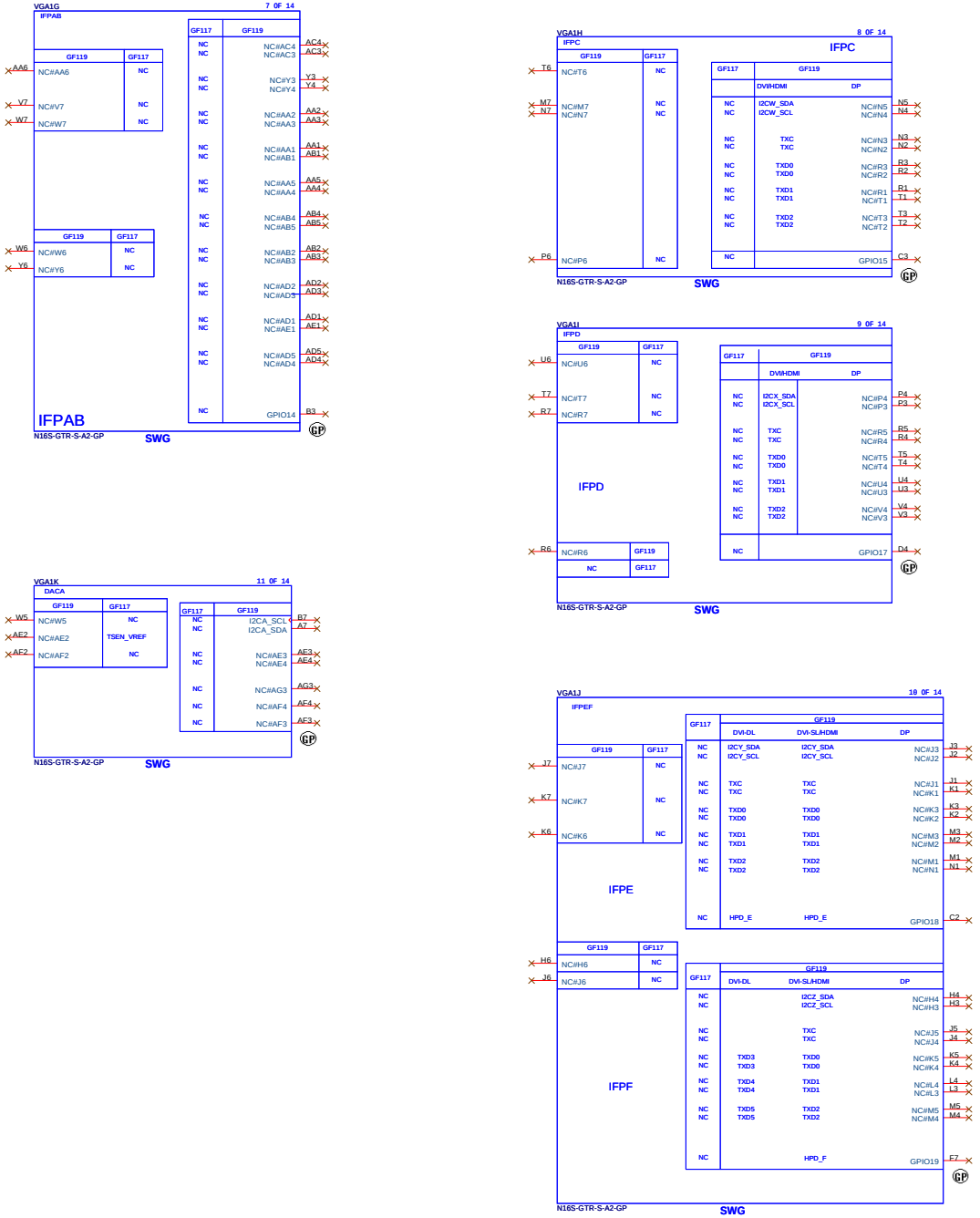
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: N15S-GM(1/6) : PEG I/F

Size	Document Number	Rev
A2	TS1	1

Date: Thursday, November 03, 2016 Sheet 39 of 100



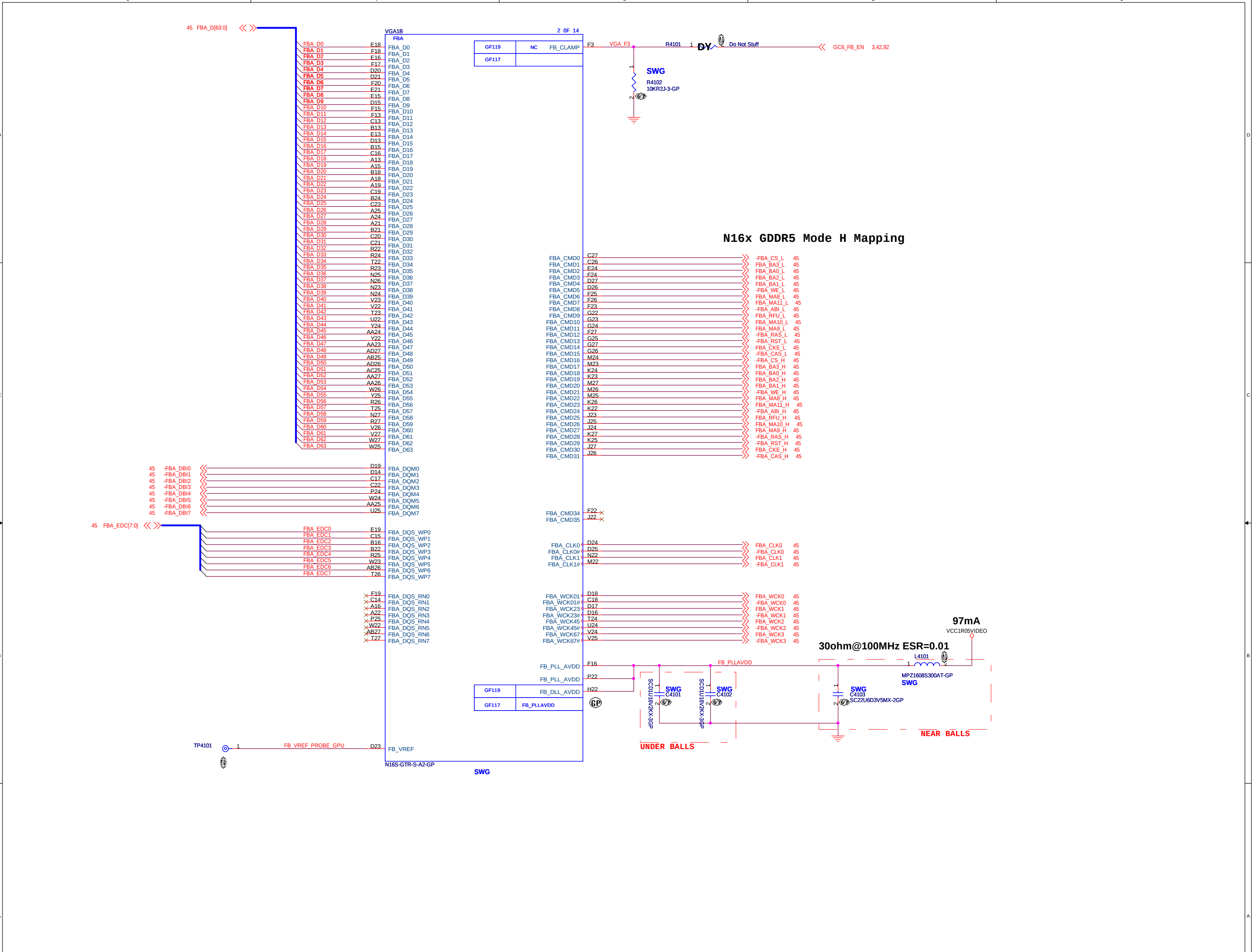
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N15S-GM(2/6) :DIGITAL OUT I/F

Size: Custom | Document Number: TS1 | Rev: 1

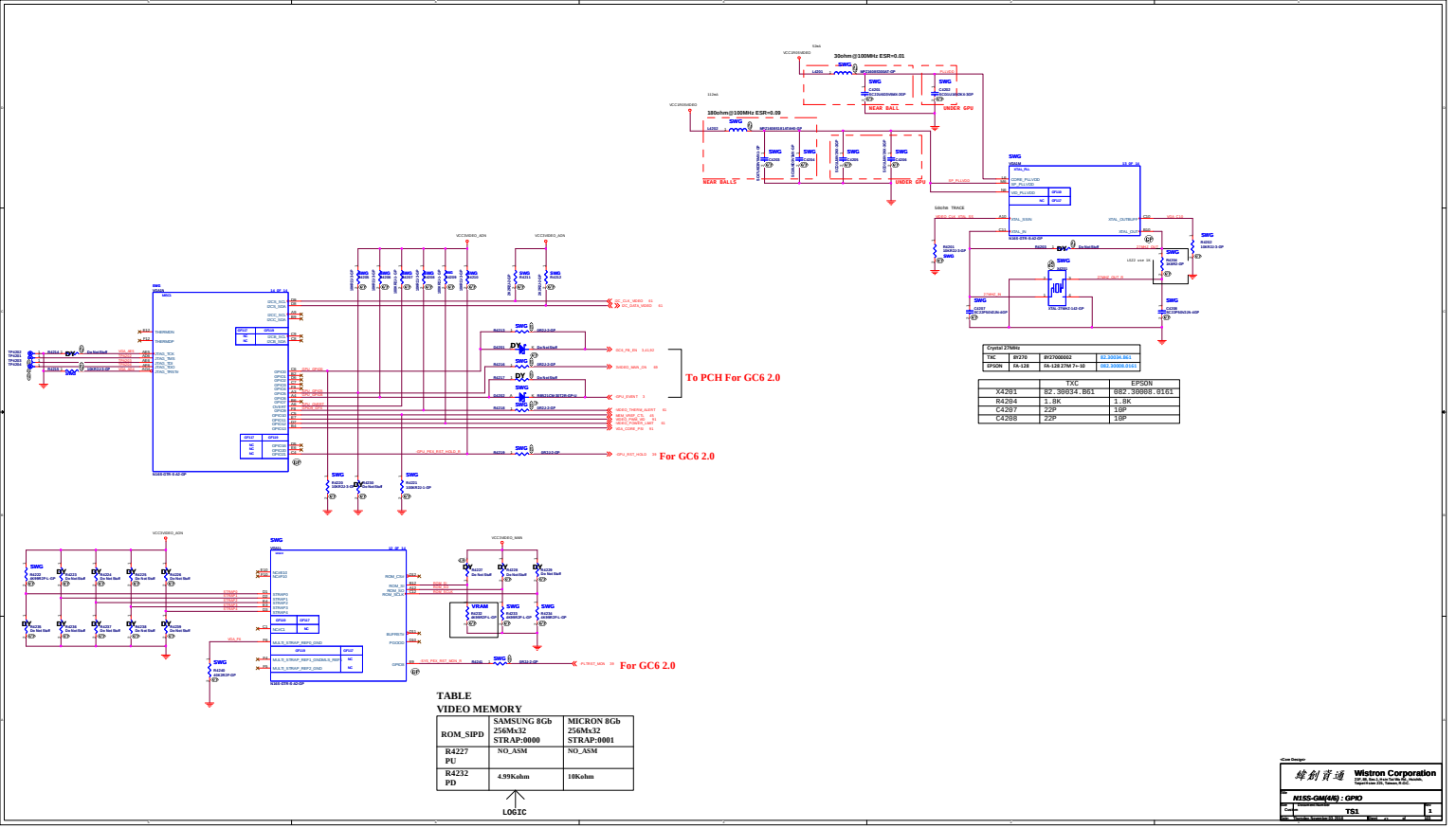
Date: Thursday, November 03, 2016 | Sheet 40 of 103



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
N15S-GM(3/6) : VRAM I/F		
Size: Custom	Document Number: **TS1**	Rev: **1**
Date: Thursday, November 03, 2016	Sheet 41 of 103	



	TXC	EPSON
X4201	82.30034.B01	082.30008.0101
R4204	1.8K	1.8K
C4207	22P	18P
C4208	22P	18P

TABLE
VIDEO MEMORY

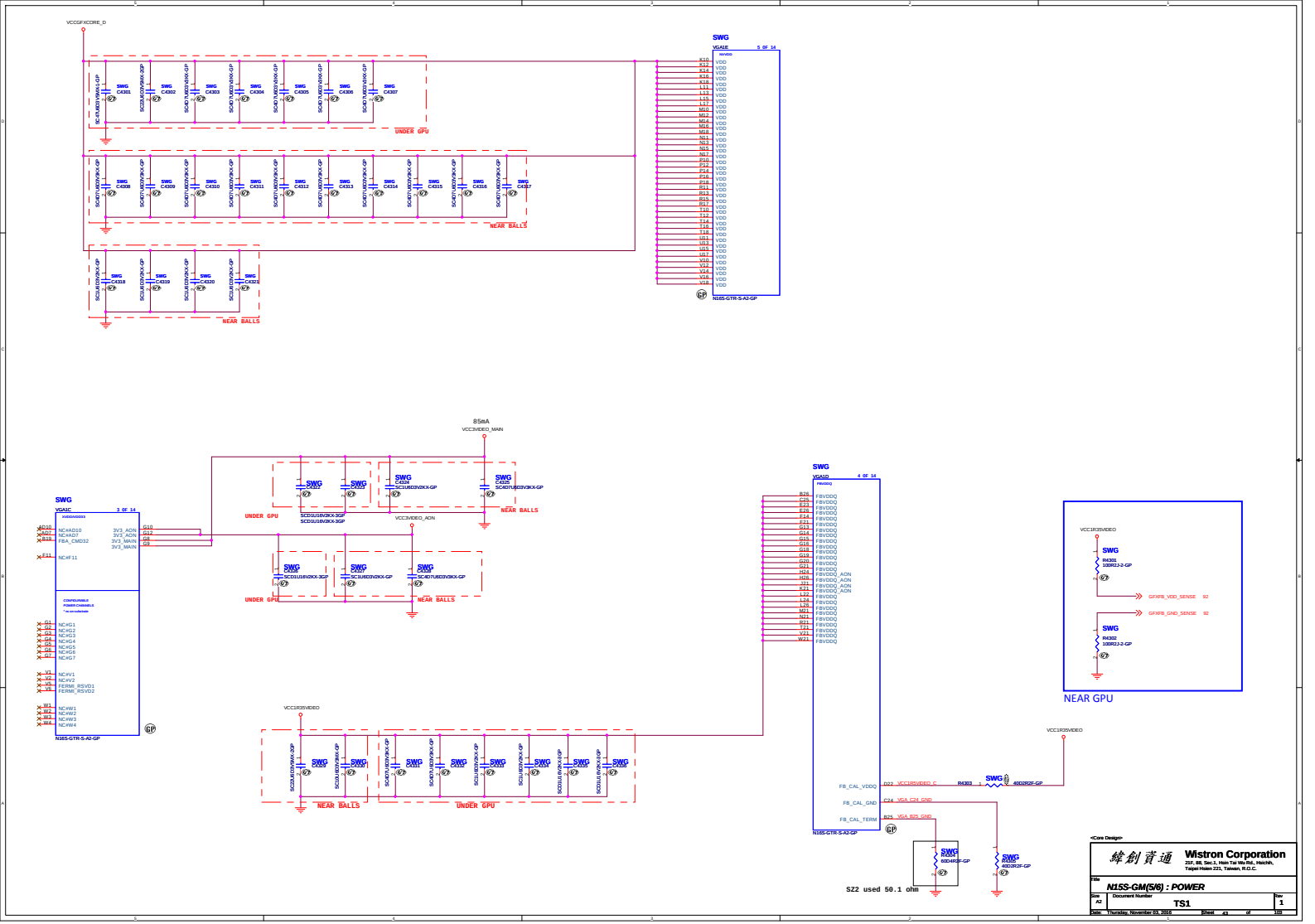
	SAMSUNG 8Gb 256Mx32 STRAP:0000	MICRON 8Gb 256Mx32 STRAP:0001
ROM_SIPD		
R4227 PU	NO_ASM	NO_ASM
R4232 PD	4.99Kohm	10Kohm

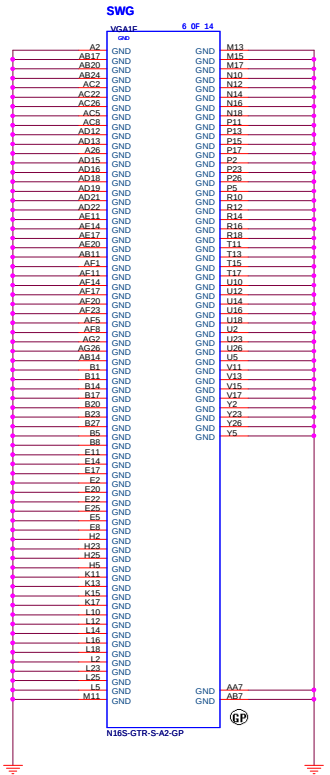
LOGIC

Wistron Corporation

N15S-GM(4/8) : GPIO

TS1


VCCGFXCORE_D
SWG
VGA1E
5 OF 14
UNDER GPU
NEAR BALLS
N16S-GTR-S-A2-GP
85mA
VCC3VIDEO_MAIN
VCC3VIDEO_AON
SWG
VGA1C
3 OF 14
N16S-GTR-S-A2-GP
SWG
VGA1D
4 OF 14
N16S-GTR-S-A2-GP
VCC1R35VIDEO
NEAR GPU
FB_CAL_VDDQ
FB_CAL_GND
FB_CAL_TERM
S22 used 50.1 ohm
<Core Design>
Wistron Corporation
N15S-GM(5/6) : POWER
TS1
Thursday, November 03, 2016



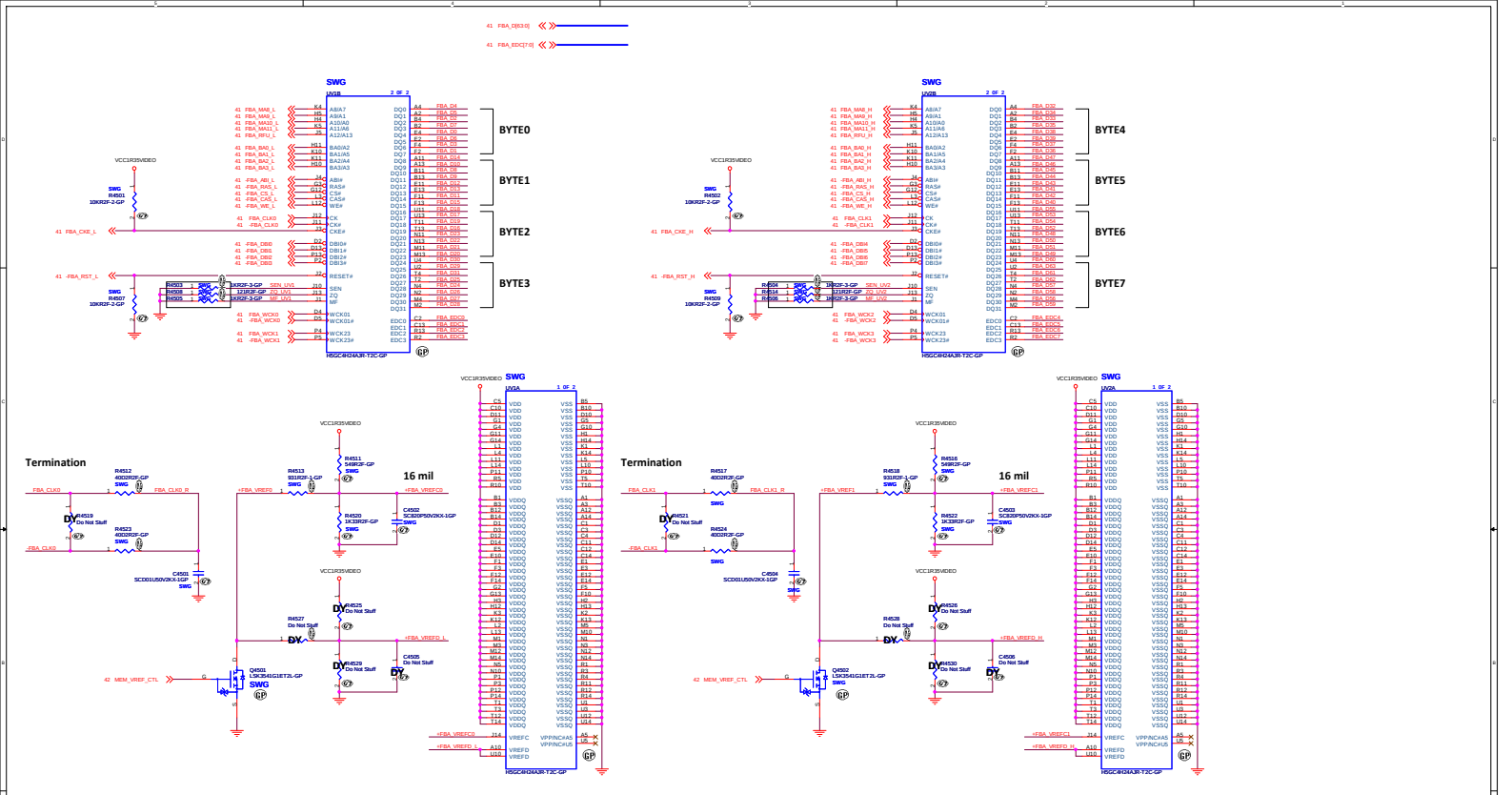
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *N15S-GM(6/6) : GND*

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 44 of 103



TS-1	For N16S-GTR (Geforce) For N15M-Q3 (Quadro)	
VRAM	SAMSUNG, GDDR5, 256M x 32, 8Gb	MICRON, GDDR5, 256M x 32, 8Gb
UV1 UV2	K4G80325FB-HC03 (B-die)	MT51J256M32HF-60:A (A-die)
BOM Structure	VS@	VM@

<Core Design>

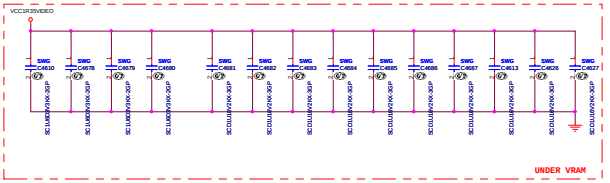
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM

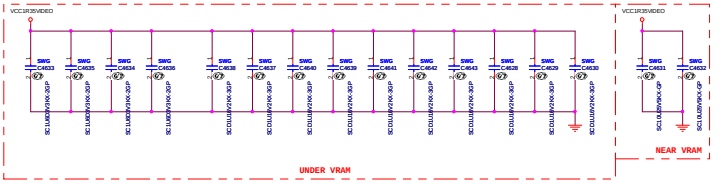
Size	Document Number	Rev
A2	TS1	1

Date: Thursday, November 03, 2016 Sheet 45 of 100

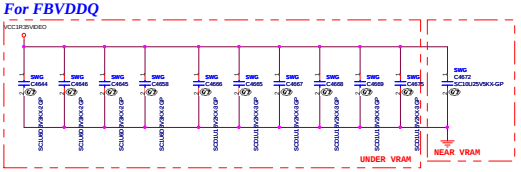
For UV1



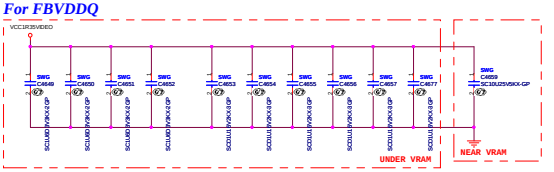
For UV2



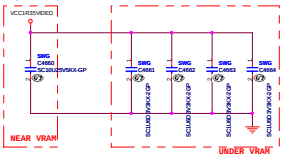
For FBVDDQ



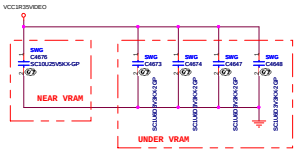
For FBVDDQ



For FBVDD



For FBVDD



Capacitor Type		Footprint		Population[1] FBVDDQ	Population[1] FBVDD	Location[2]
FBVDD/Q Combined						
0.1 µF	X7R	0402	10	10		Under DRAM
1.0 µF	X7R	0603	4	4		Under DRAM
10 µF	X5R	0805	2	2		Close to DRAM
FBVDD/Q Separate						
0.1 µF	X7R	0402	6	6	0	Under DRAM
1.0 µF	X7R	0603	8	4	4	Under DRAM
10 µF	X5R	0805	2	1	1	Close to DRAM

Note:
1. Per sub-partition, for example, per two pieces of ×16 DRAM or one piece of ×32 DRAM.
2. Location is close to DRAM for all decoupling with ×16 DRAM.

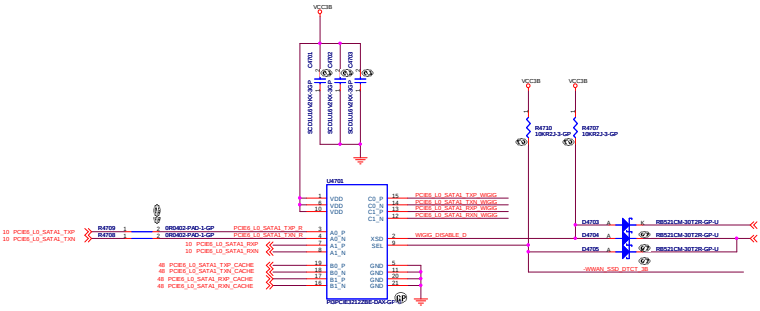
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

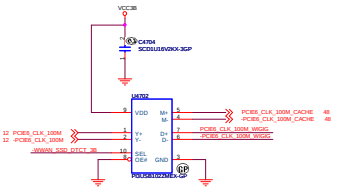
Title: VRAM MEMORY DECOUPLING

Size: A2 | Document Number: TS1 | Rev: 1

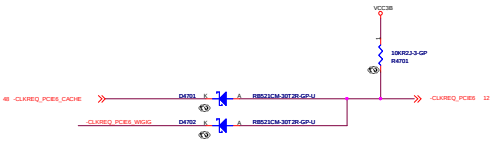
Date: Thursday, November 03, 2005 | Sheet 46 of 100



Pericom PI3PCIE3212ZBE 071.33212.0003
NXP CBTL02043ABQ 071.02043.0003
TOSHIBA TC7PCI3212MT 071.73212.0003



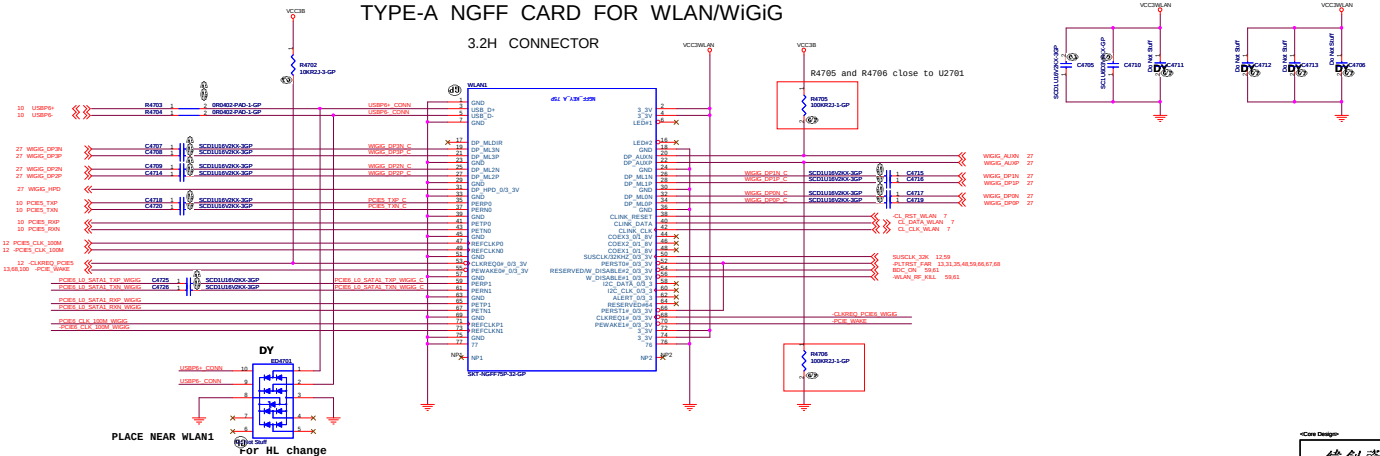
Pericom PI3USB102ZME 73.3US10.D03
NXP NX3DV42GU 73.00342.003



	WWAN Slot							
	Optance		SATA Cache		WWAN Card		None	
WiGig_DISABLE	L	H	L	H	L	H	L	H
-WWAN_SSD_DTCT	L	L	L	L	H	H	H	H
SEL(U4701)	L	L	L	L	H	H	H	H
XSD(U4701)	L	L	L	L	L	H	L	H
PCIE6_L0_SATA1	To M.2 Socket2	To M.2 Socket2	To M.2 Socket2	To M.2 Socket2	To M.2 Socket2	Disconnect	To M.2 Socket2	Disconnect
-WWAN_SATA_DTCT	High	High	Low	Low	High	High	High	High
PCIE6_L0_SATA1	PCIe	PCIe	SATA	SATA	PCIe	PCIe	PCIe	PCIe

TYPE-A NGFF CARD FOR WLAN/WiGiG

3.2H CONNECTOR

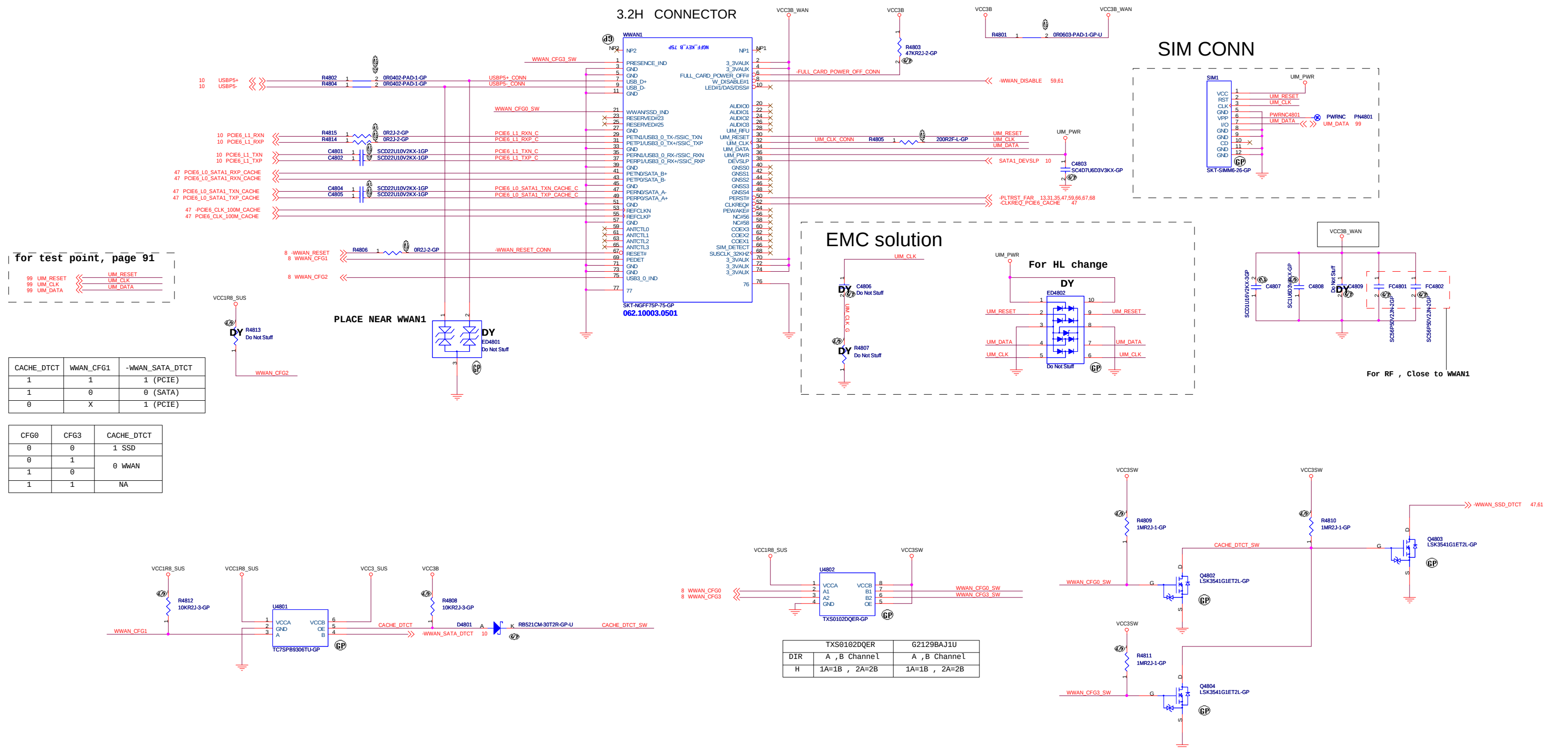


<Core Design>
鋒創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M.2 SOCKET 1 MODULE I/F
Size: A2
Document Number: TS1
Rev: 1
Date: Thursday, November 03, 2005
Sheet 47 of 100

TABLE:

State #	Module Configuration Decodes: CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)	Module Type and Main Host Interface	Port Configuration
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	GND	GND	NC	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	GND	NC	NC	WWAN - PCIe	1
4	GND	NC	GND	GND	WWAN - USB 3.0	0
5	GND	NC	GND	NC	WWAN - USB 3.0	1
6	GND	NC	NC	GND	WWAN - USB 3.0	2
7	GND	NC	NC	NC	WWAN - USB 3.0	3
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	GND	GND	NC	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	GND	NC	NC	WWAN - SSIC	3
12	NC	NC	GND	GND	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	NC	NC	GND	RFU	N/A
15	NC	NC	NC	NC	No Module Present	N/A



CACHE_DTCT	WWAN_CFG1	-WWAN_SATA_DTCT
1	1	1 (PCIE)
1	0	0 (SATA)
0	X	1 (PCIE)

CFG0	CFG3	CACHE_DTCT
0	0	1 SSD
0	1	0 WWAN
1	0	
1	1	NA

	TXS0102DQER	G2129BAJ1U
DIR	A ,B Channel	A ,B Channel
H	1A=1B , 2A=2B	1A=1B , 2A=2B

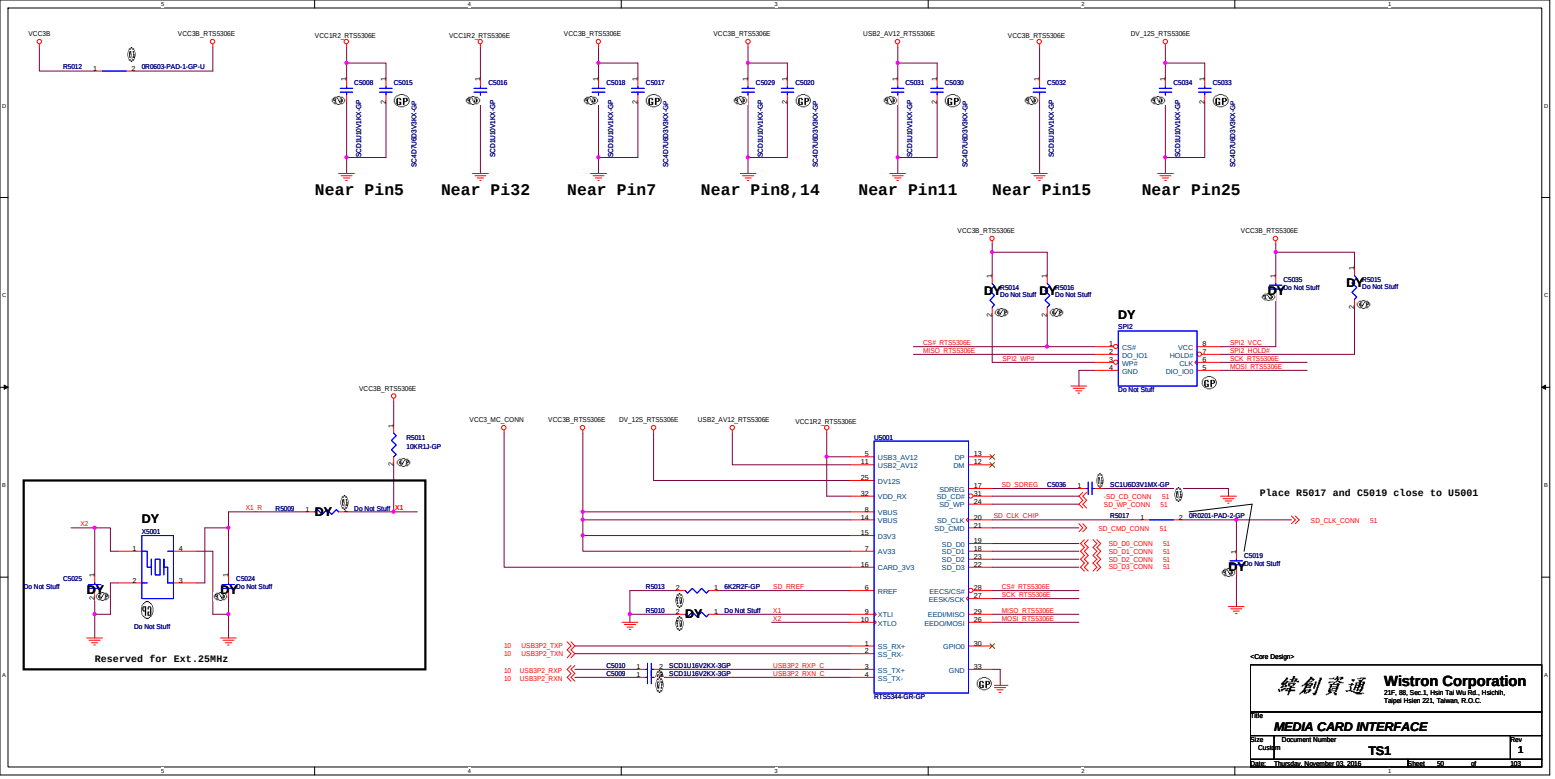
BLANK

<Core Design>

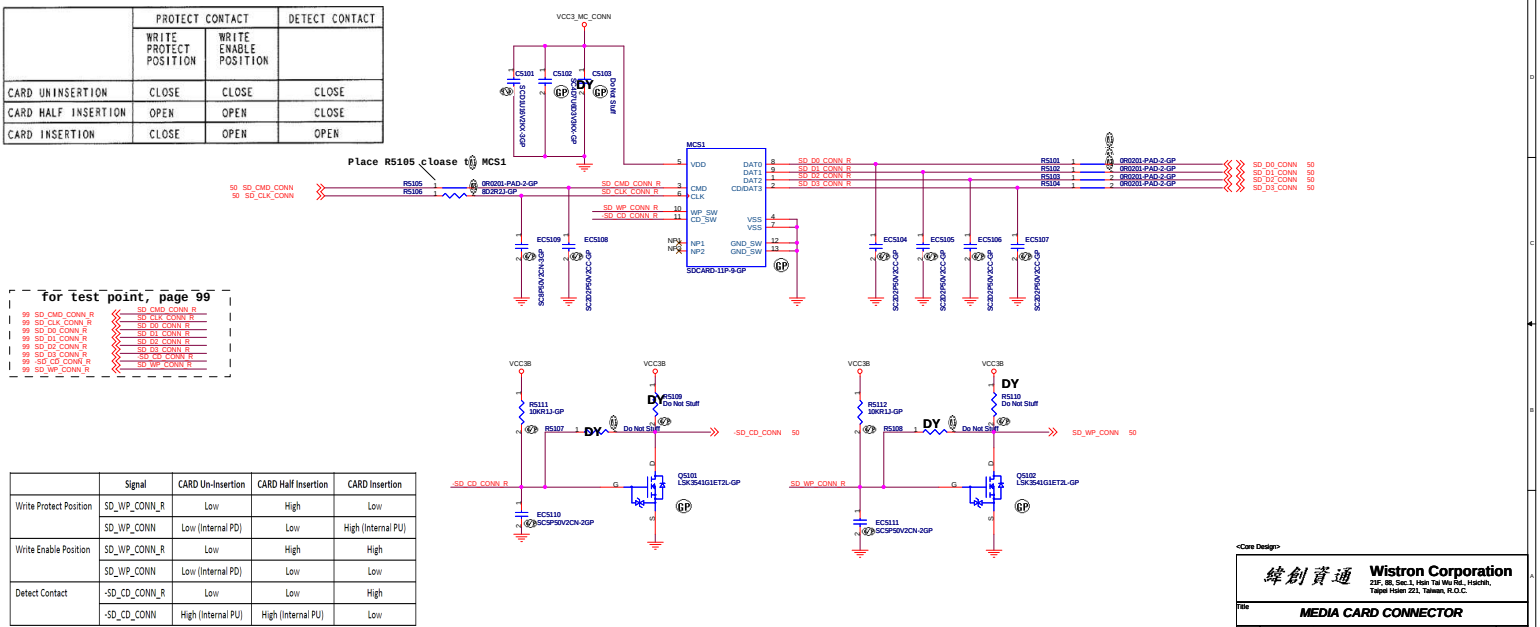
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BLANK***	
Size: A	Document Number: **TS1**	Rev: **1**
Date: Thursday, November 03, 2016	Sheet 49 of 103	


VCC3B
VCC3B_RTS5306E
R5012
0R0603-PAD-1-GP-U
VCC1R2_RTS5306E
C5008
C5015
Near Pin5
C5016
Near Pi32
VCC3B_RTS5306E
C5018
C5017
Near Pin7
C5029
C5020
Near Pin8,14
USB2_AV12_RTS5306E
C5031
C5030
Near Pin11
C5032
Near Pin15
DV_12S_RTS5306E
C5034
C5033
Near Pin25
R5014
R5016
SPI2
CS# RTS5306E
MISO RTS5306E
SPI2_WP#
Do Not Stuff
C5035
R5015
SPI2_VCC
SPI2_HOLD#
SCK RTS5306E
MOSI RTS5306E
R5011
10KR1J-GP
VCC3_MC_CONN
X5001
X1_R
R5009
X1
X2
C5025
C5024
Reserved for Ext.25MHz
USB3_AV12
USB2_AV12
DV12S
VDD_RX
VBUS
D3V3
AV33
CARD_3V3
RREF
XTLI
XTLO
SS_RX+
SS_RX-
SS_TX+
SS_TX-
DP
DM
SDREG
SD_CDI#
SD_WP
SD_CLK
SD_CMD
SD_D0
SD_D1
SD_D2
SD_D3
EECS/CS#
EESK/SCK
EEDI/MISO
EEDO/MOSI
GPIO0
GND
RTS5344-GR-GP
SD_SDREG
SC1U6D3V1MX-GP
SD_CD_CONN
SD_WP_CONN
SD_CLK_CHIP
SD_CMD_CONN
SD_D0_CONN
SD_D1_CONN
SD_D2_CONN
SD_D3_CONN
R5017
0R0201-PAD-2-GP
SD_CLK_CONN
C5019
Place R5017 and C5019 close to U5001
R5013
6K2R2F-GP
SD_RREF
R5010
USB3P2_TXP
USB3P2_TXN
USB3P2_RXP
USB3P2_RXN
C5010
C5009
SCD1U16V2KX-3GP
USB3P2_RXP_C
USB3P2_RXN_C
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MEDIA CARD INTERFACE
Size
Custom
Document Number
TS1
Rev
1
Date: Thursday, November 03, 2016
Sheet 50 of 103

	PROTECT CONTACT		DETECT CONTACT
	WRITE PROTECT POSITION	WRITE ENABLE POSITION	
CARD UNINSERTION	CLOSE	CLOSE	CLOSE
CARD HALF INSERTION	OPEN	OPEN	CLOSE
CARD INSERTION	CLOSE	OPEN	OPEN



	Signal	CARD Un-Insertion	CARD Half Insertion	CARD Insertion
Write Protect Position	SD_WP_CONN_R	Low	High	Low
	SD_WP_CONN	Low (Internal PD)	Low	High (Internal PU)
Write Enable Position	SD_WP_CONN_R	Low	High	High
	SD_WP_CONN	Low (Internal PD)	Low	Low
Detect Contact	-SD_CD_CONN_R	Low	Low	High
	-SD_CD_CONN	High (Internal PU)	High (Internal PU)	Low

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MEDIA CARD CONNECTOR

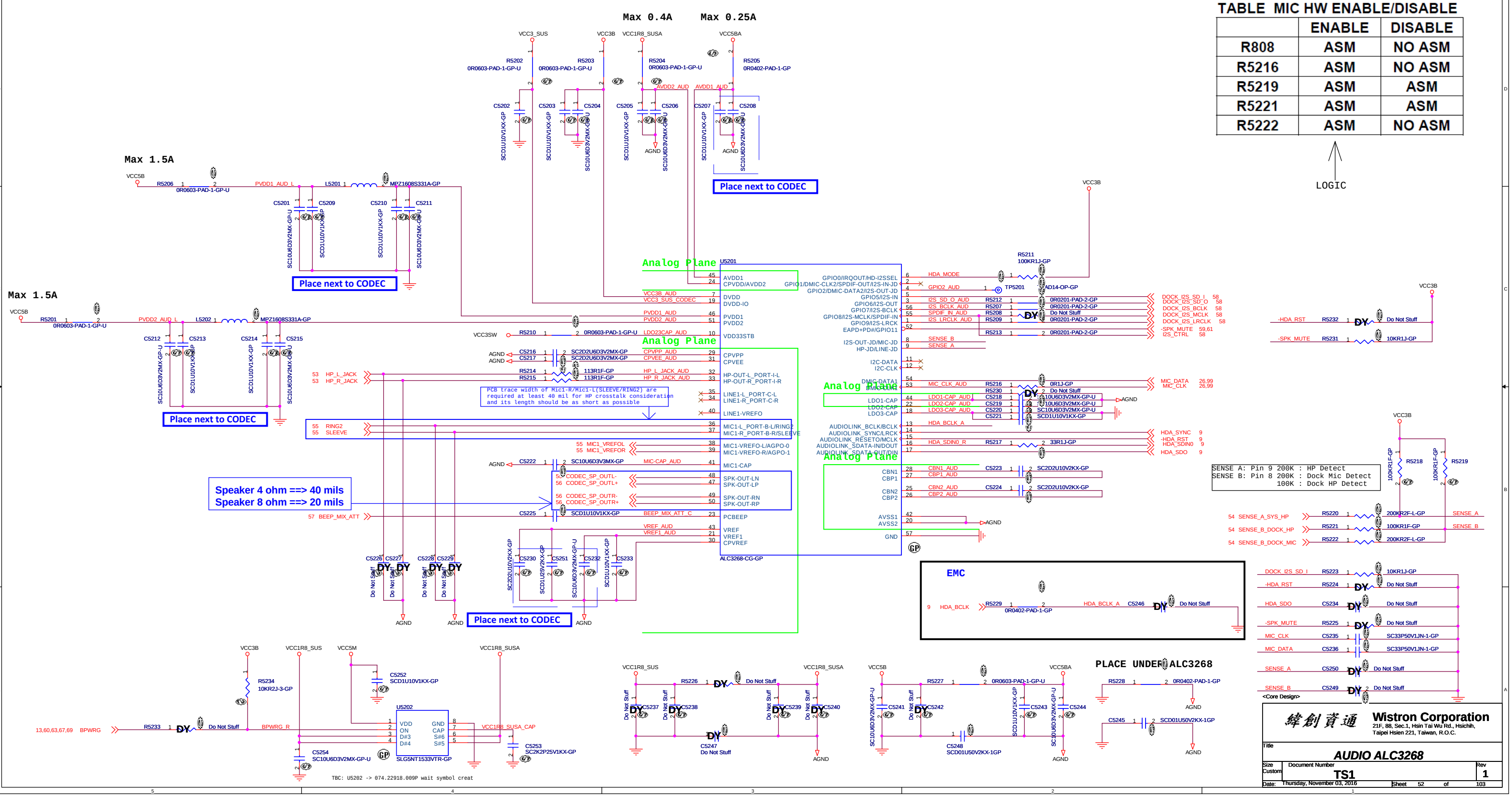
Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 51 of 103

TABLE MIC HW ENABLE/DISABLE

	ENABLE	DISABLE
R808	ASM	NO ASM
R5216	ASM	NO ASM
R5219	ASM	ASM
R5221	ASM	ASM
R5222	ASM	NO ASM

LOGIC



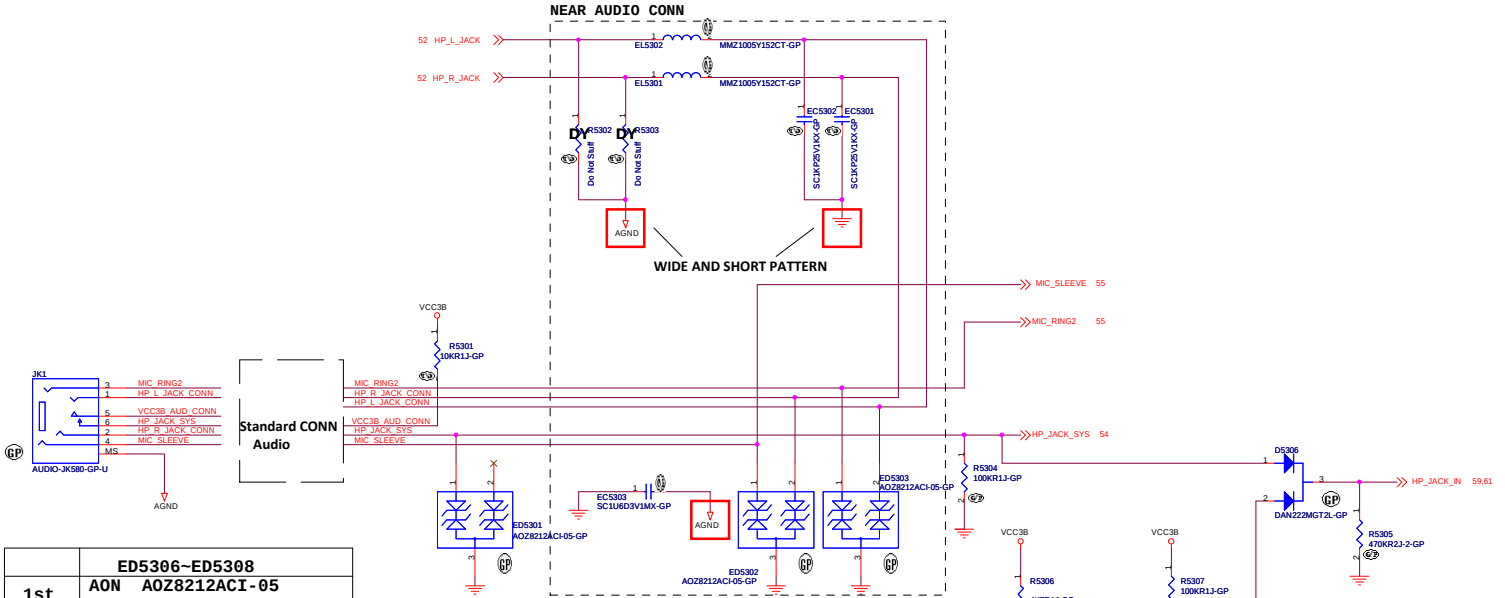
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO ALC3268

Size: Custom | Document Number: TS1 | Rev: 1

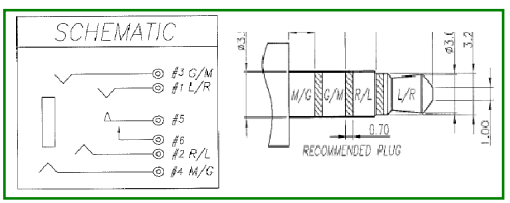
Date: Thursday, November 03, 2016 | Sheet 52 of 103

<Core Design>



	ED5306~ED5308
1st	AON AOZ8212ACI-05 075.08212.007D
2nd	LITTELFUSE SM24CANA-02HTG 075.00024.007D
3rd	NXP PESD5V0S2BT 75.005V0.A7D

Audio Jack



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CONNECTOR

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 53 of 103

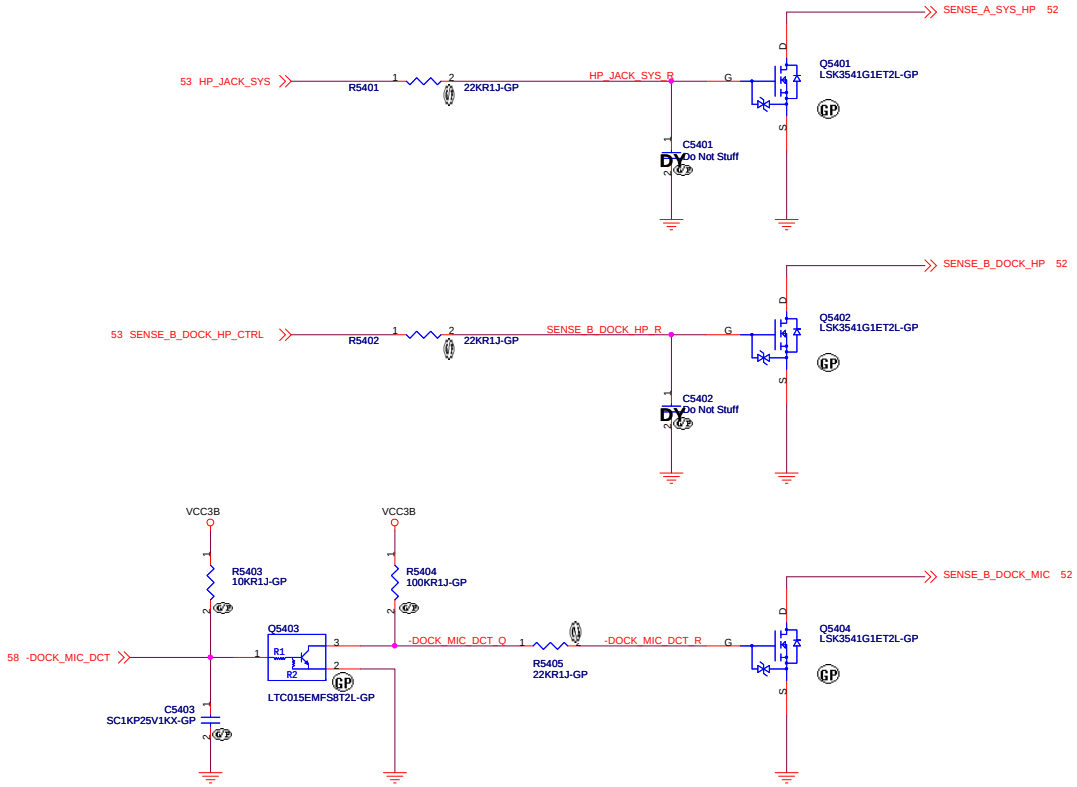


TABLE MIC HW ENABLE/DISABLE

	ENABLE	DISABLE
R5403	ASM	NO ASM
R5404	ASM	NO ASM
R5405	ASM	NO ASM
Q5403	ASM	NO ASM
Q5404	ASM	NO ASM

LOGIC

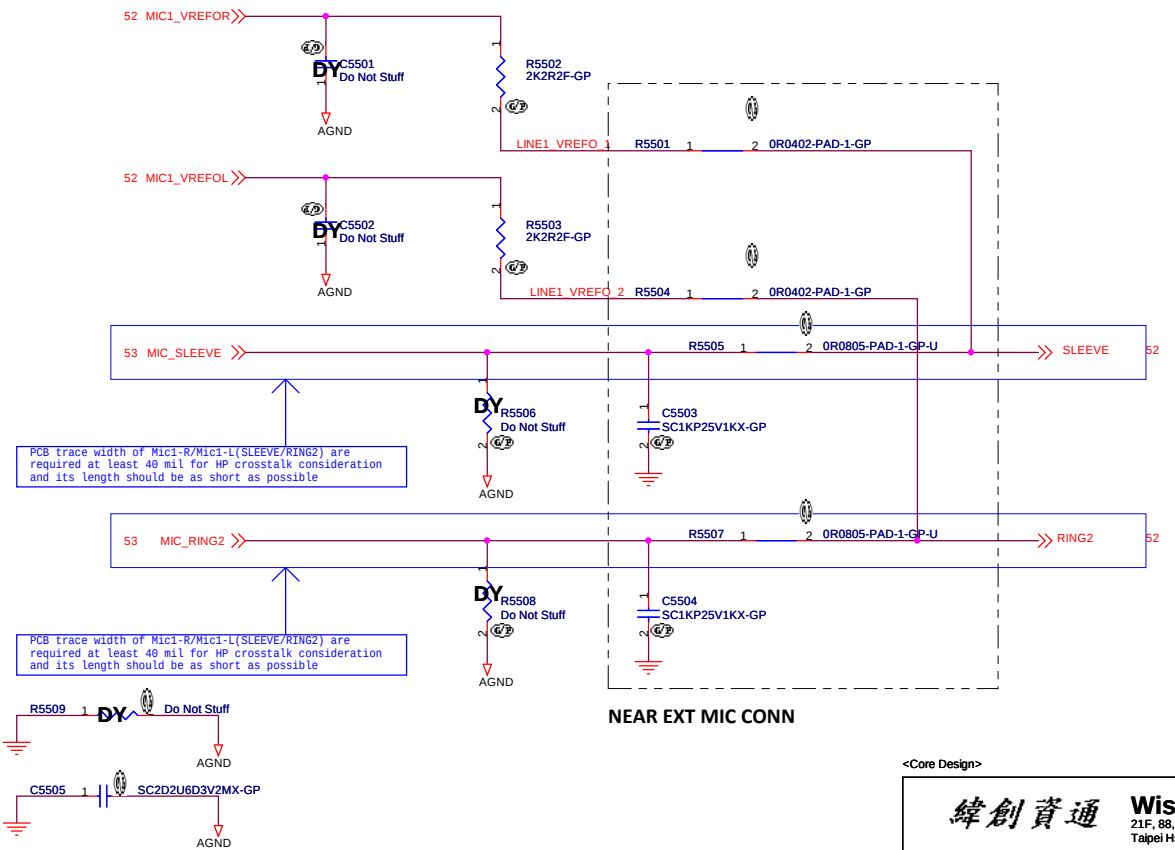
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO JACK SENSE**

Size: Custom | Document Number: TS1 | Rev: 1

Date: Thursday, November 03, 2016 | Sheet 54 of 103



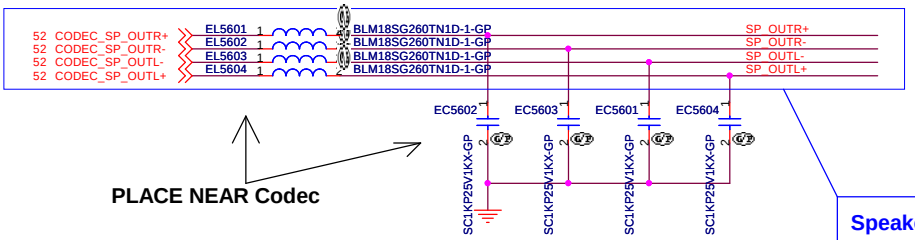
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO EXT MIC I/F***

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 55 of 103



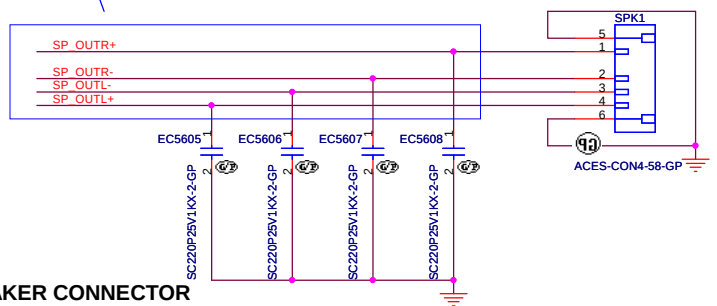
PLACE NEAR Codec

Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils

ALC3268 speaker output part

for test point, page 99

99 SP_OUTR+
99 SP_OUTR-
99 SP_OUTL-
99 SP_OUTL+



PLACE, NEAR SPEAKER CONNECTOR

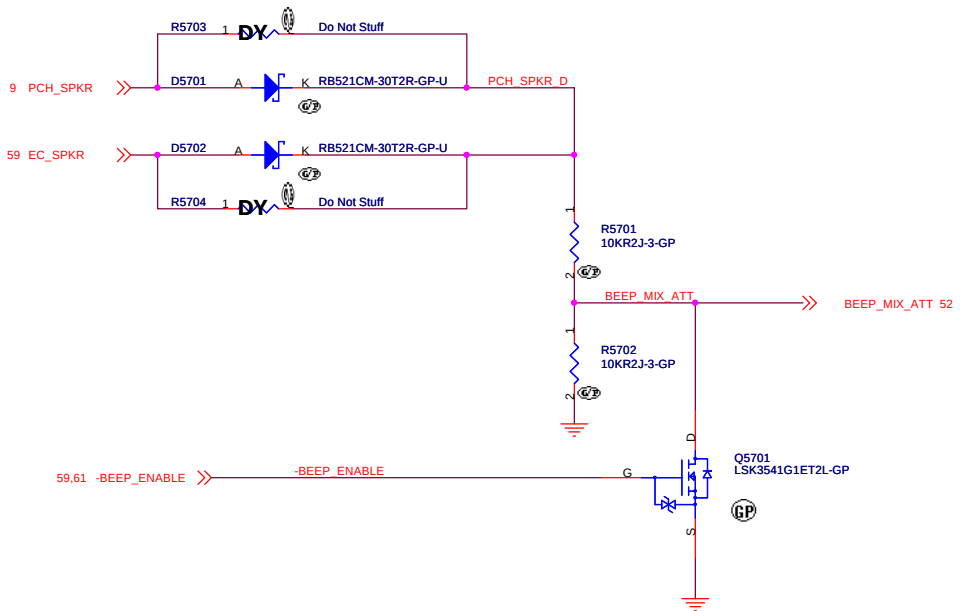
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO SPEAKER

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 56 of 103



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO BEEP***

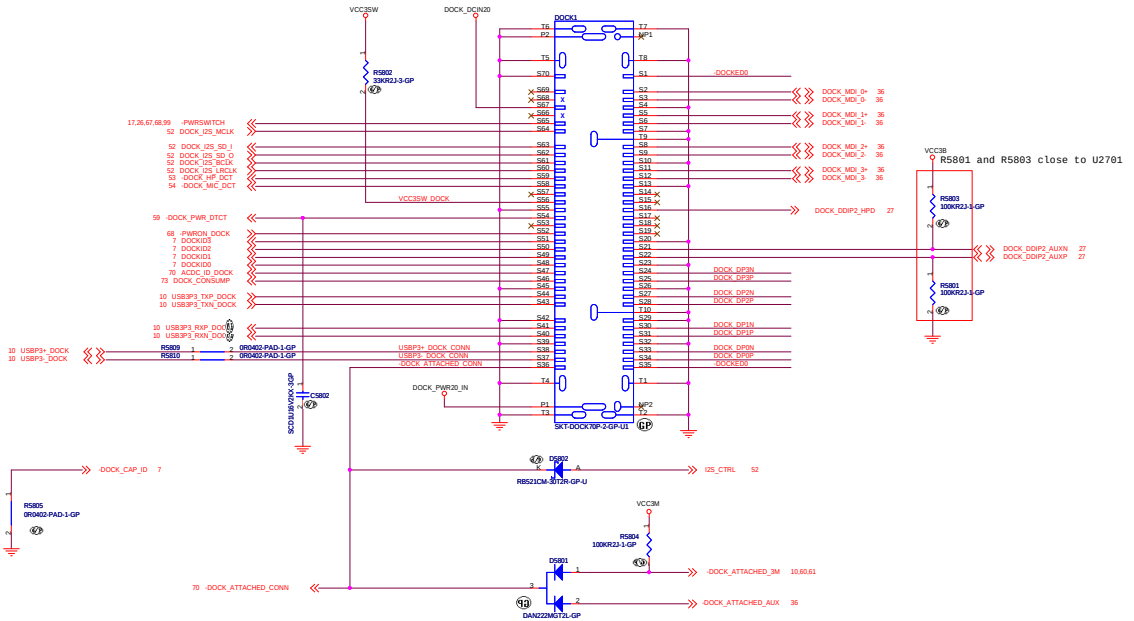
Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 57 of 103

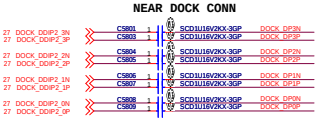
LOGIC

TABLE

ID	DOCKING SUPPORT	NON-SUPPORT
DOCK1	ASM	NO ASM
R5802	ASM	NO ASM
D5801	ASM	NO ASM
D5802	ASM	NO ASM
R5804	ASM	NO ASM
C5802	ASM	ASM
R5809	ASM	NO ASM
R5810	ASM	NO ASM
C5801	ASM	NO ASM
C5803	ASM	NO ASM
C5804	ASM	NO ASM
C5805	ASM	NO ASM
C5806	ASM	NO ASM
C5807	ASM	NO ASM
C5808	ASM	NO ASM
C5809	ASM	NO ASM
R5803	ASM	NO ASM
R5801	ASM	NO ASM
R5805	ASM	NO ASM



NEAR DOCK CONN



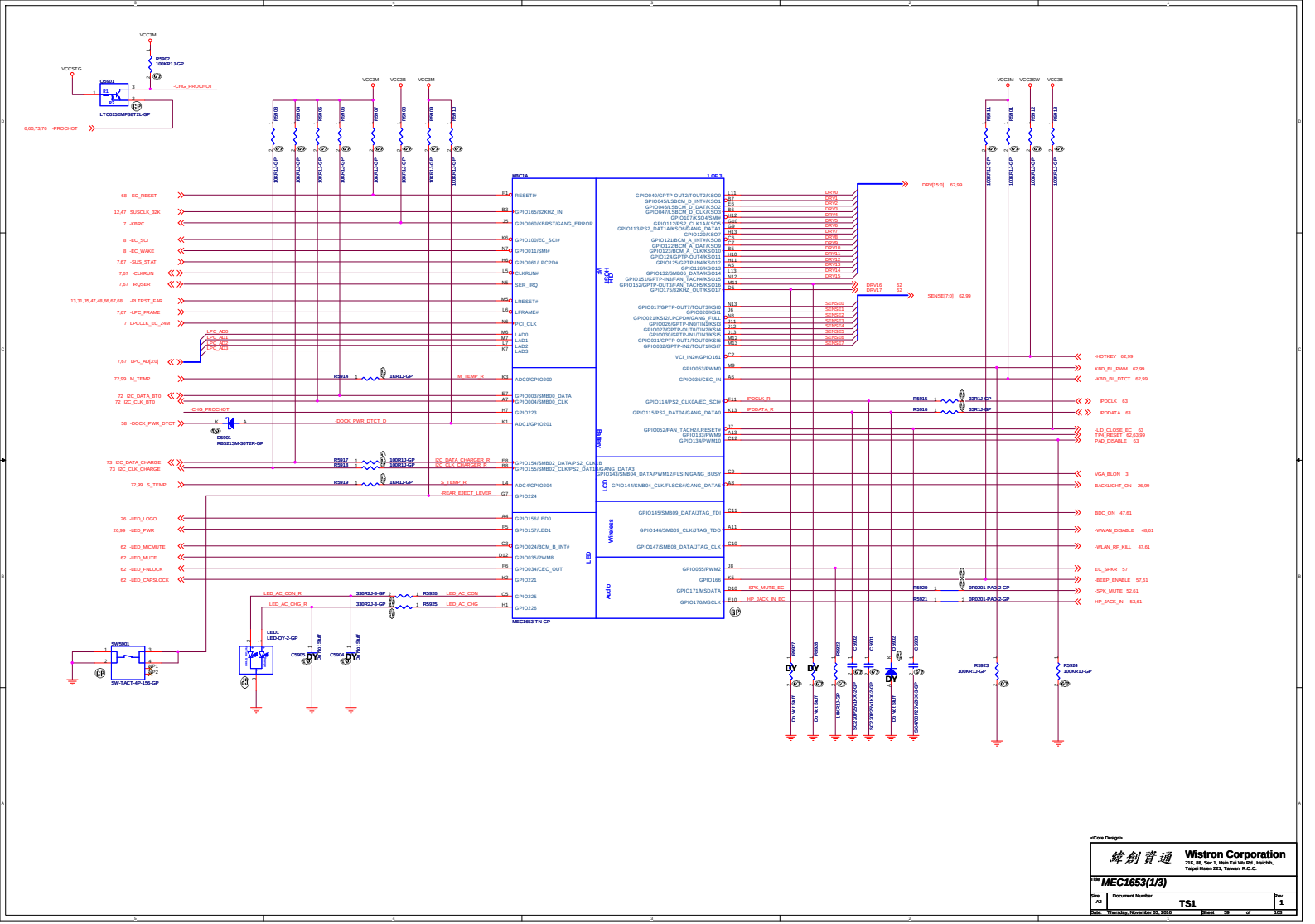
<Core Design>

Wistron Corporation
21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DOCKING CONNECTOR

Size: Custom | Document Number: TS1 | Rev: 1

Date: Thursday, November 03, 2016 | Sheet 58 of 103

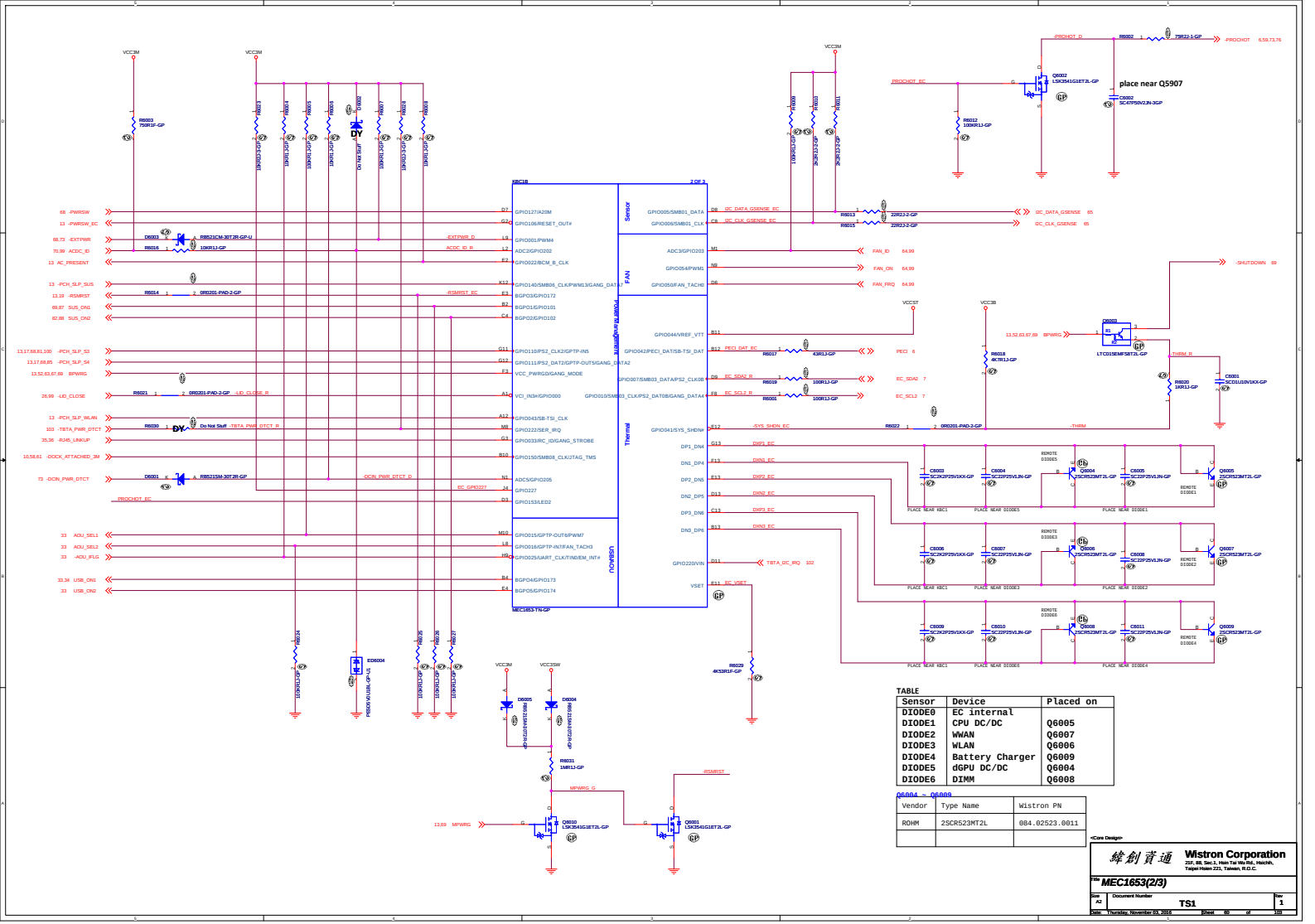


<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MEC1653(1/3)

Size	Document Number	Rev
A2	TS1	1

Date: Thursday, November 03, 2016 Sheet 58 of 100



TABLE

Sensor	Device	Placed on
DIODE0	EC internal	
DIODE1	CPU DC/DC	Q6005
DIODE2	WWAN	Q6007
DIODE3	WLAN	Q6006
DIODE4	Battery Charger	Q6009
DIODE5	dGPU DC/DC	Q6004
DIODE6	DIMM	Q6008

Q6004 ~ Q6009

Vendor	Type Name	Wistron PN
ROHM	2SCR523MT2L	084.02523.0011

<Core Design>

Wistron Corporation
2SF, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MEC1653(2/3)

Size	Document Number	Rev
A2	TS1	1

Date: Thursday, November 03, 2016 Sheet 80 of 100

Trace FIFO Debug Port

	Enable	Disable
R5920	22_5%	0_5%
R5921	22_5%	0_5%
R420(?)	NO_ASM	ASM

TABLE

VIDEO_ID	R6141	R6116
SWG	NO_ASM	ASM
UMA	ASM	NO_ASM

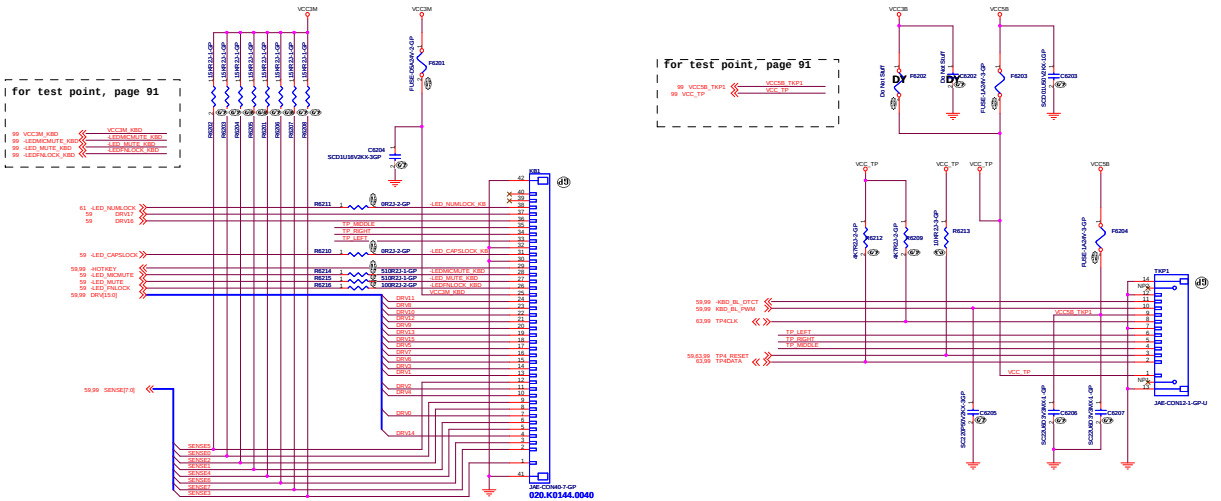
LOGIC

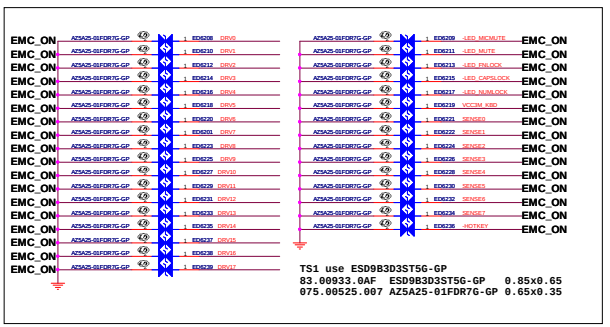
Improve rising time to change from 10K to 4.7K

JTAG Debug Port

	Enable	Disable
R6117	ASM	NO_ASM
R6140	NO_ASM	ASM
R6144	ASM	NO_ASM
R6145	ASM	NO_ASM
R6146	ASM	NO_ASM
R6147	ASM	NO_ASM
R5225	ASM	NO_ASM
R5231	NO_ASM	ASM

Wistron Corporation	22F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: MEC1653(3/3)	
Size: Custom	Document Number: TS1	Rev: 1
Date: Thursday, November 03, 2016	Sheet 61 of 103



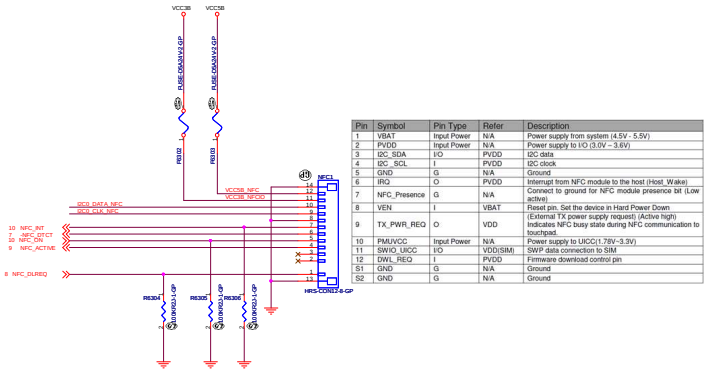


TS1 use ESD9B3D3ST5G-GP
83.00933.0AF ESD9B3D3ST5G-GP 0.85x0.65
075.00525.007 AZ5A25-01FDR7G-GP 0.65x0.35

<Core Design>

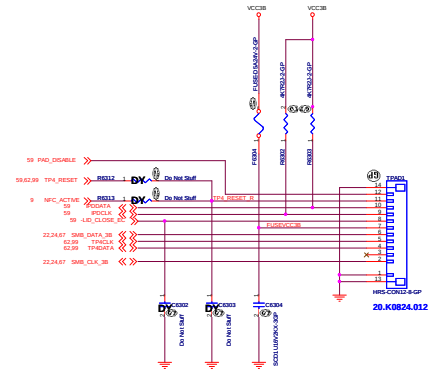
緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	KEYBOARD/TRACK POINT	
Size: A2	Document Number: TS1	Rev: 1
Date: Thursday, November 03, 2016	Sheet 62 of 100	

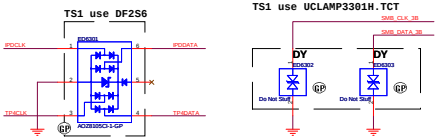
NFC



Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V – 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C_SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host_Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down
9	TX_PWR_REQ	O	VDD	(External TX power supply request) (Active high) Indicates NFC busy state during NFC communication to touchpad.
10	PMUVCC	Input Power	N/A	Power supply to UICC(1.78V~3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to SIM
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground

TOUCH PAD

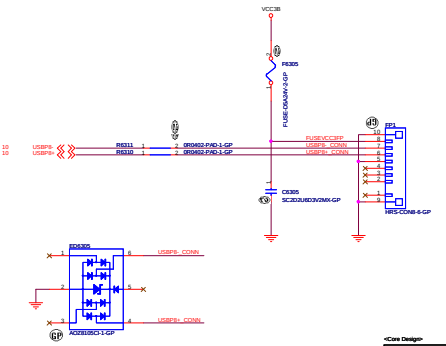




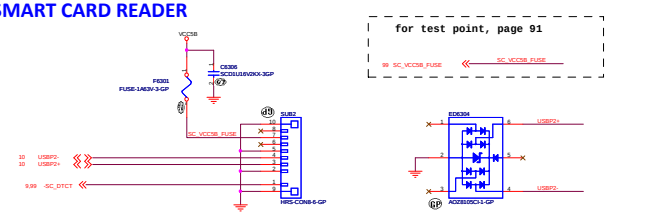
TS1 use DF2S6

TS1 use UCLAMP3301H.TCT

FINGER PRINT READER



SMART CARD READER



for test point, page 91

<Core Design>

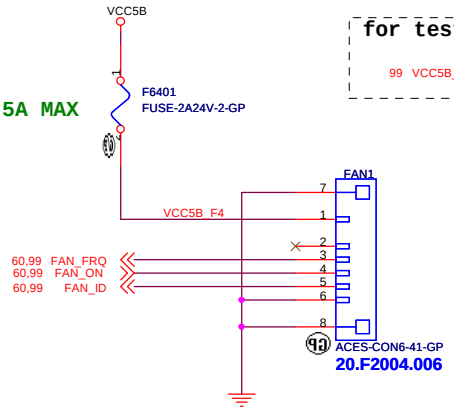
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	TOUCH PAD/NFC/FPR	
Size: A2	Document Number: TS1	Rev: 1
Date: Thursday, November 03, 2016	Sheet 63 of 100	

FAN

FAN CURRENT IS 0.5A MAX
FUSE 2.0A



for test point, page 91

99 VCC5B_F4 <<< VCC5B_F4

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FAN CONNECTOR

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 64 of 103

TABLE

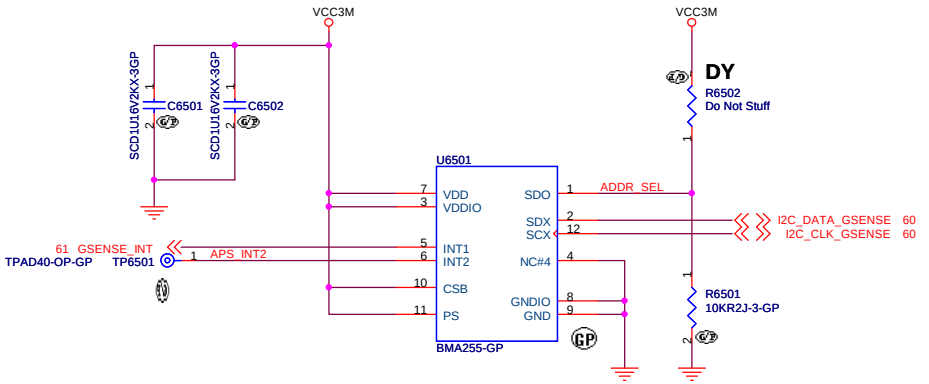
CSB	Mode Selection
H	I2C Mode
L	SPI Mode

Logic

TABLE

P/N	ADDR_SEL	Address
BMA255	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

LOGIC



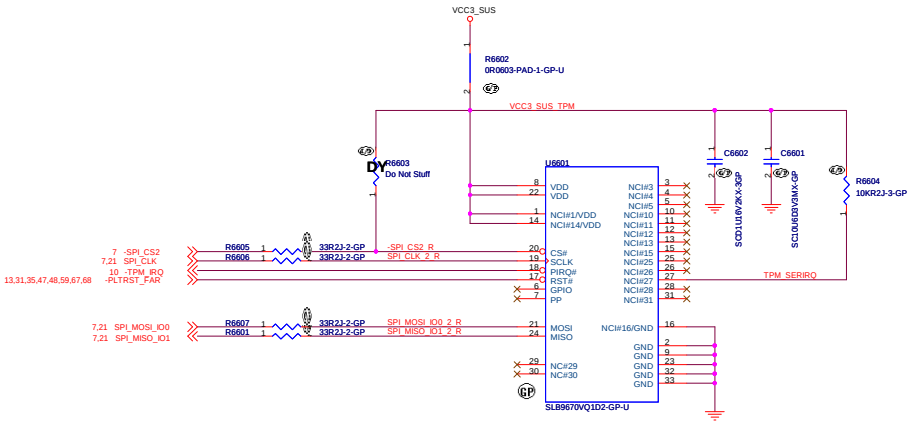
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***APS G-SENSOR***

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 65 of 103



TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ2.0 FW7.60	ST Micro ST33HTPH2E32AHA6	Nuvoton NPCT650LB0YX
1	VDD	VDD	NC	VSB
2	GND	GND	GND	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_IRQ#	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND

<Core Design>

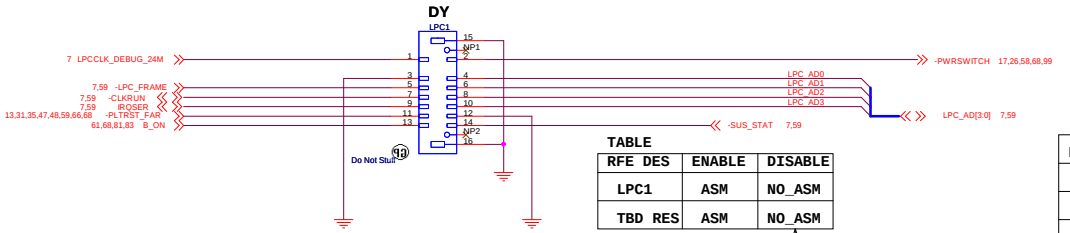
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE TPM 1.2

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 66 of 103

Lenovo Debug Tool I/F



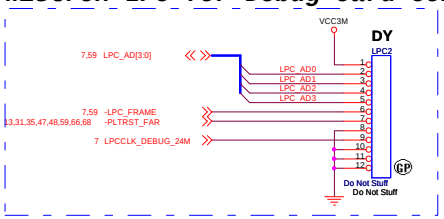
TABLE

RFE DES	ENABLE	DISABLE
LPC1	ASM	NO_ASM
TBD RES	ASM	NO_ASM

LOGIC

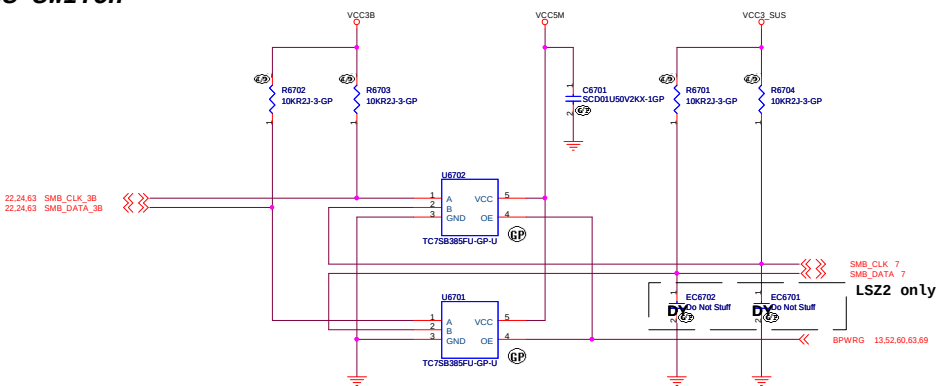
LEVEL	LPC1
SDV	ASM
FVT	No ASM
SIT	TBD
SVT	TBD

Wistron LPC for Debug Card Connector



LEVEL	LPC2
SDV	ASM
FVT	No ASM
SIT	TBD
SVT	TBD

SMBUS SWITCH



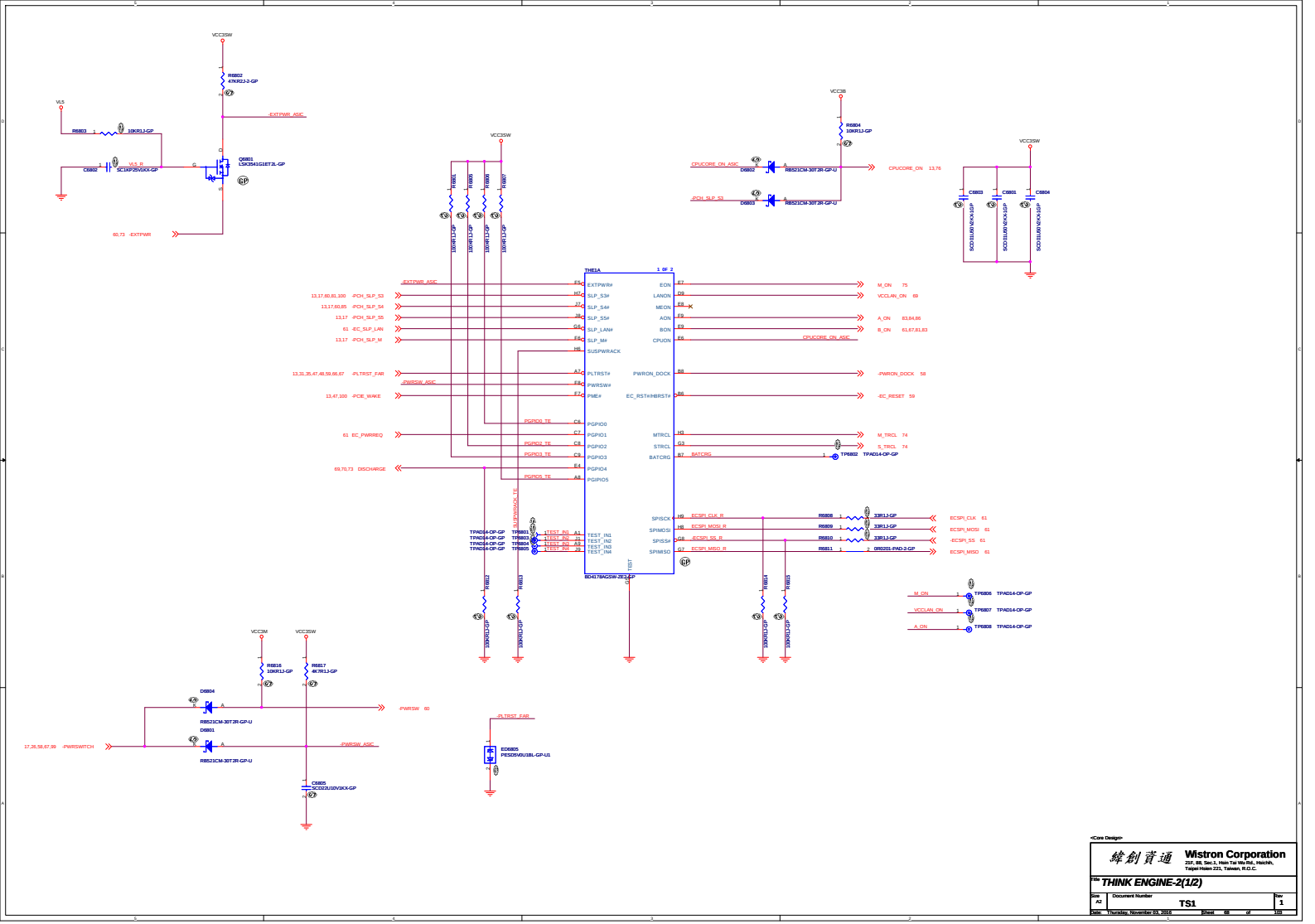
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS SWITCH/LPC DEBUG PORT

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 67 of 103



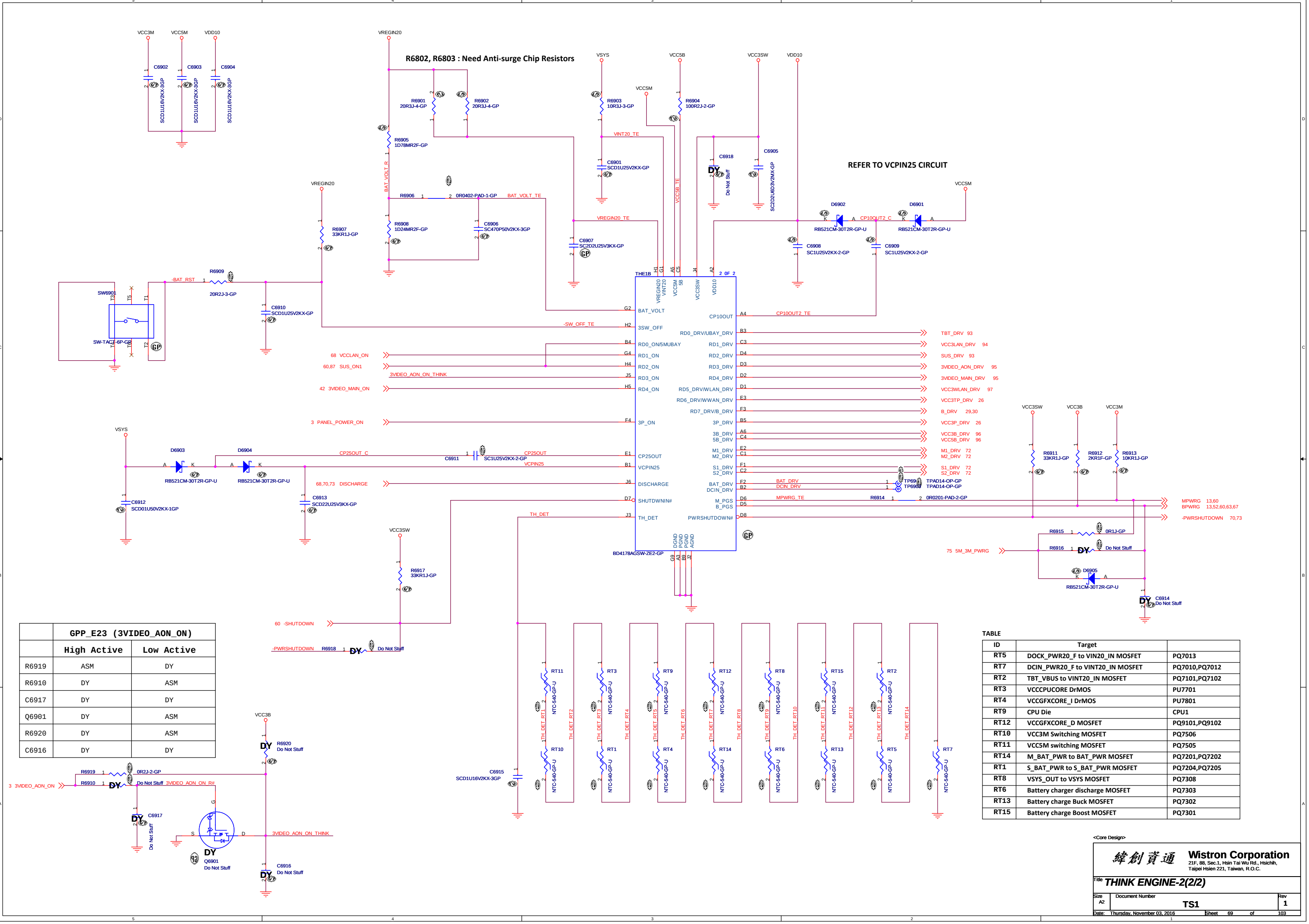
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THINK ENGINE-2(1/2)

Size	Document Number	Rev
A2	TS1	1

Date: Thursday, November 03, 2016 Sheet 68 of 100



	GPP_E23 (3VIDEO_AON_ON)	
	High Active	Low Active
R6919	ASM	DY
R6910	DY	ASM
C6917	DY	DY
Q6901	DY	ASM
R6920	DY	ASM
C6916	DY	DY

TABLE

ID	Target	
RT5	DOCK_PWR20_F to VIN20_IN MOSFET	PQ7013
RT7	DCIN_PWR20_F to VINT20_IN MOSFET	PQ7010,PQ7012
RT2	TBT_VBUS to VINT20_IN MOSFET	PQ7101,PQ7102
RT3	VCCCPUCORE DrMOS	PU7701
RT4	VCCGFXCORE_I DrMOS	PU7801
RT9	CPU Die	CPU1
RT12	VCCGFXCORE_D MOSFET	PQ9101,PQ9102
RT10	VCC3M Switching MOSFET	PQ7506
RT11	VCC5M switching MOSFET	PQ7505
RT14	M_BAT_PWR to BAT_PWR MOSFET	PQ7201,PQ7202
RT1	S_BAT_PWR to S_BAT_PWR MOSFET	PQ7204,PQ7205
RT8	VSYS_OUT to VSYS MOSFET	PQ7308
RT6	Battery charger discharge MOSFET	PQ7303
RT13	Battery charge Buck MOSFET	PQ7302
RT15	Battery charge Boost MOSFET	PQ7301

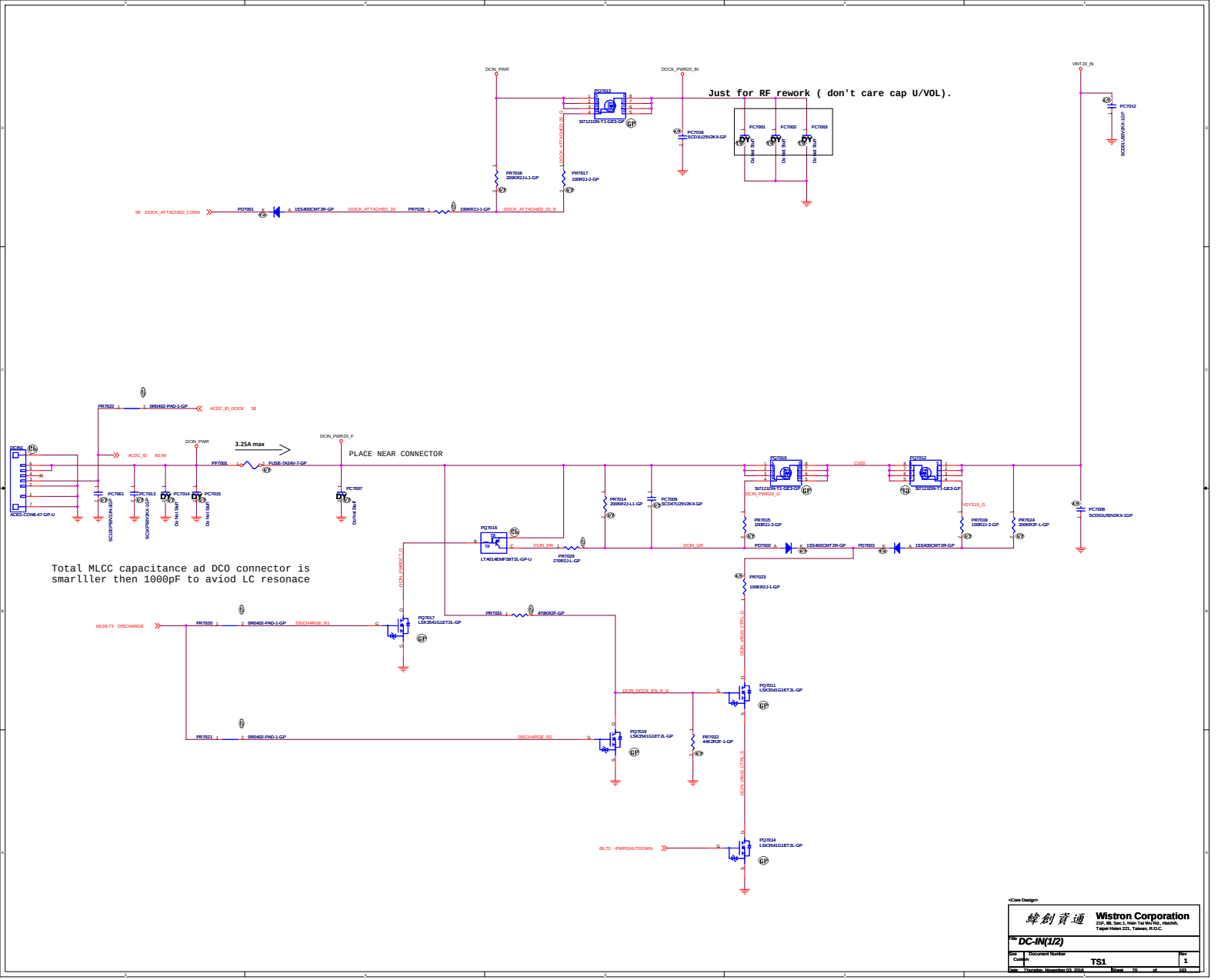
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: THINK ENGINE-2(2/2)

Size: A2 | Document Number: TS1 | Rev: 1

Date: Thursday, November 03, 2016 | Sheet 69 of 103



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

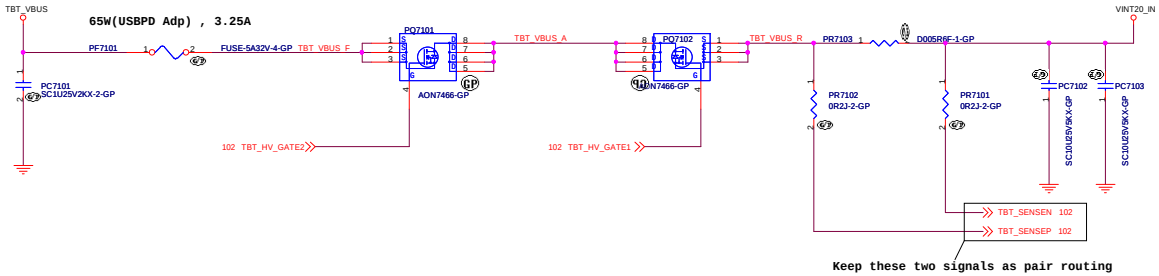
Title: **DC-IN(1/2)**

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 20 of 103

PQ7101 and PQ7102

	Vendor	Vendor PN	Wistron PN
1st	AOS	AON7466	084.07466.0037
2nd	Rohm	RQ3E150GNA10	084.03150.0037



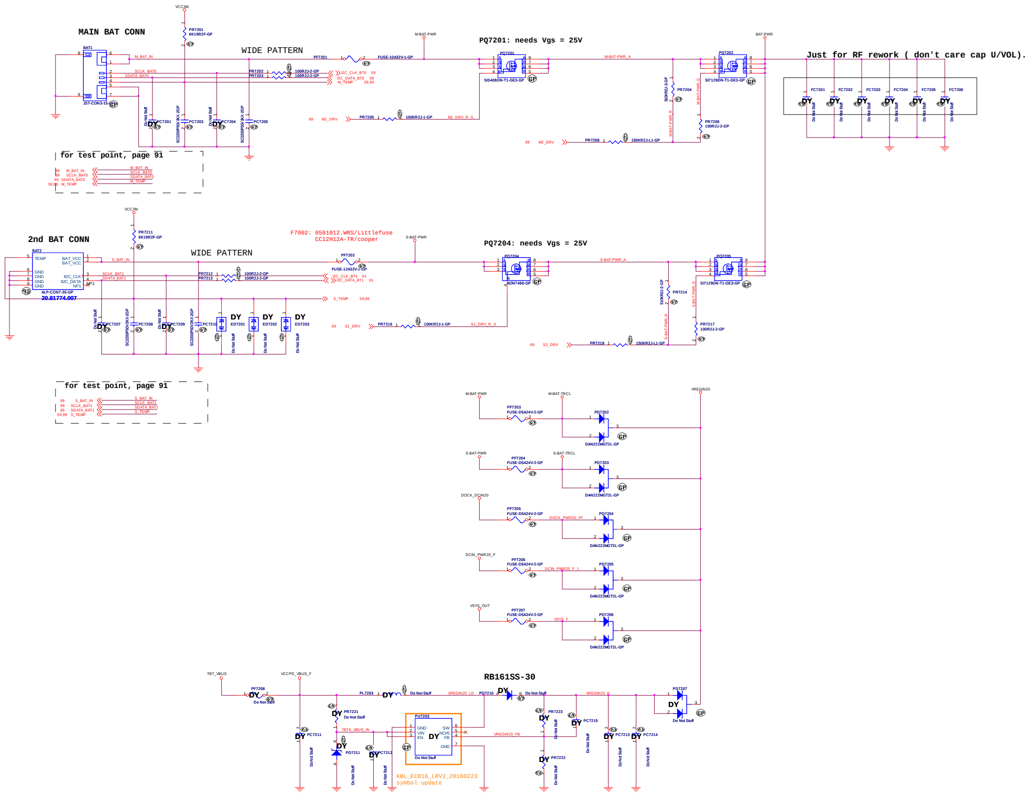
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC-IN(2/2)

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 71 of 103



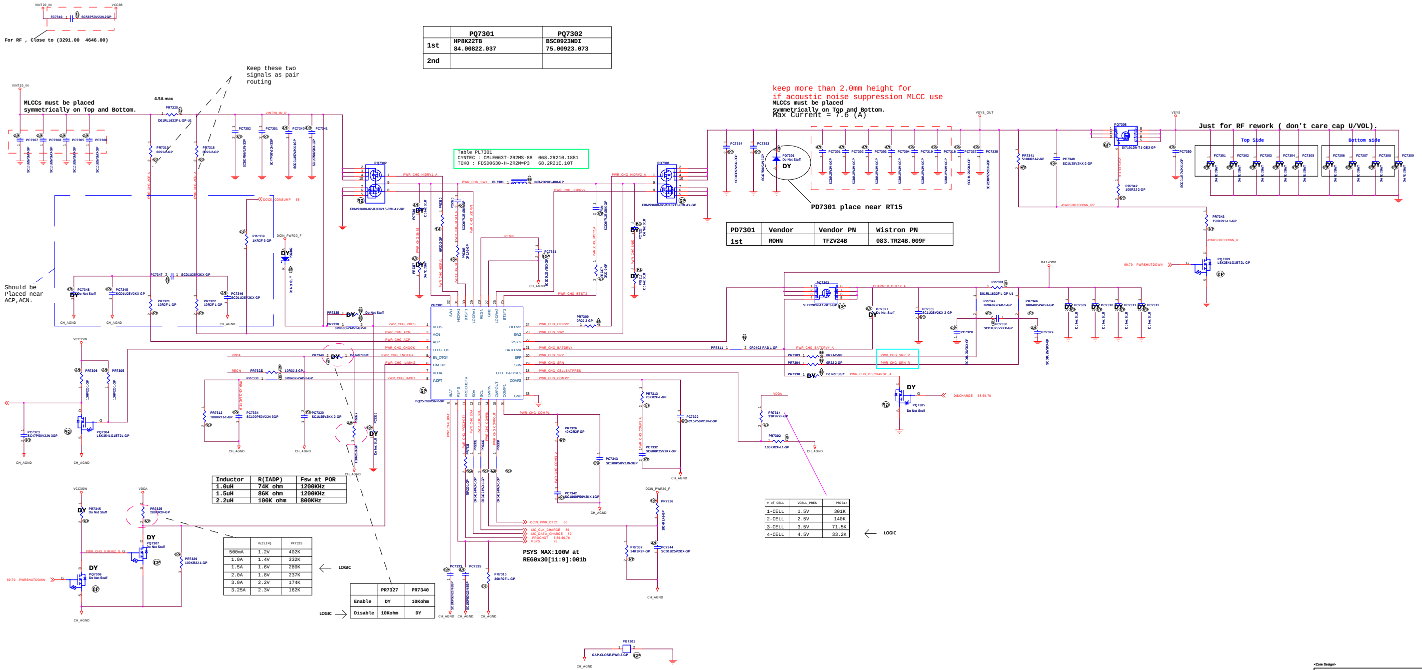
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATTERY INPUT**

Size: A1 | Document Number | Rev

Date: Thursday, November 03, 2016 | Sheet 72 of 103



	PQ7301	PQ7302
1st	HP8K22TB 84.00822.037	BSC0923NDI 75.00923.073
2nd		

PD7301	Vendor	Vendor PN	Wistron PN
1st	ROHN	TFZV24B	083.TR24B.009F

Inductor	R(IADP)	Fsw at POR
1.0uH	74K ohm	1200KHz
1.5uH	86K ohm	1200KHz
2.2uH	100K ohm	800KHz

	V(ILIM)	PR7325
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

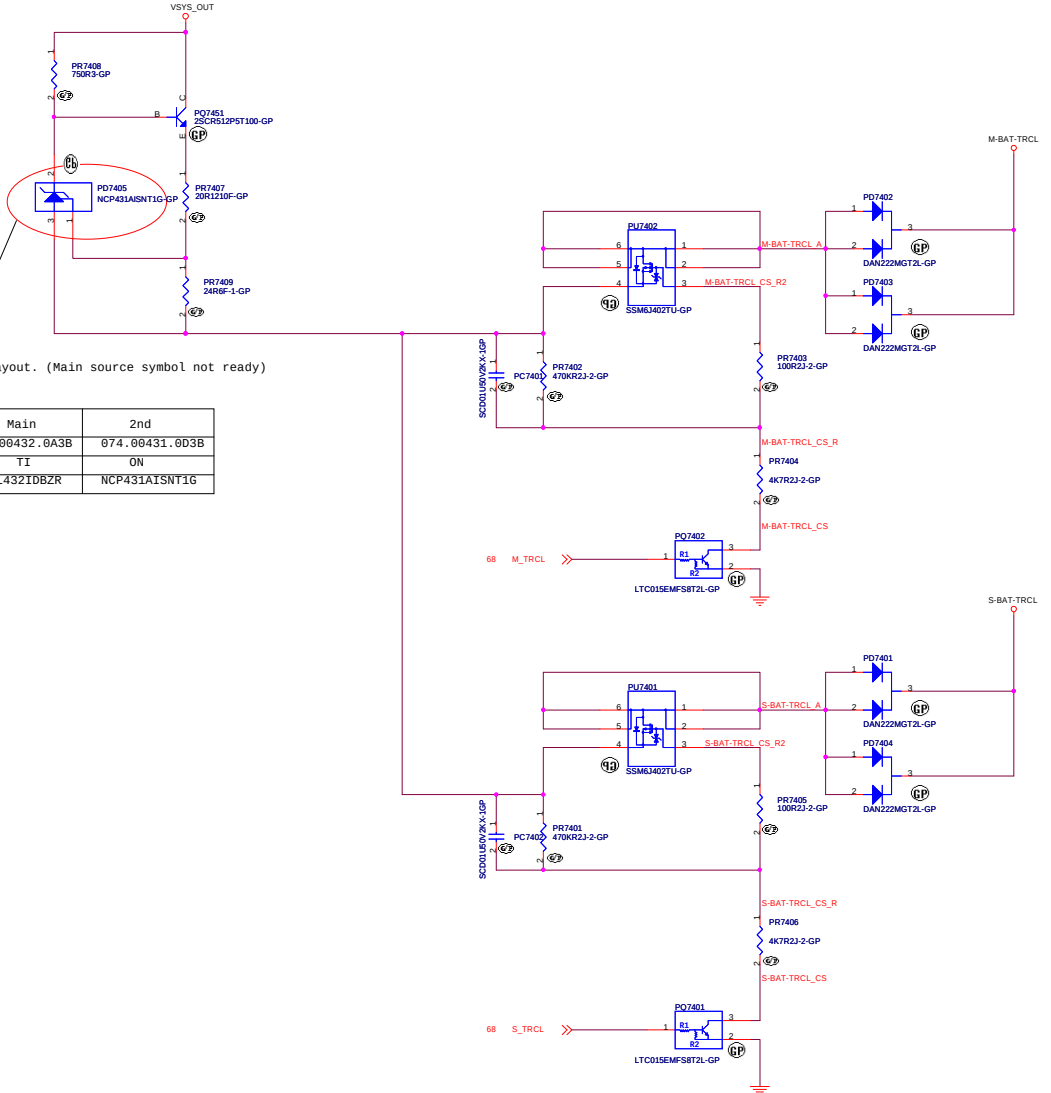
	PR7327	PR7340
Enable	DY	10Kohm
Disable	10Kohm	DY

# of CELL	VCELL_PRES	PR7314
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	BATTERY CHARGER(BQ25700)	
Size: Custom	Document Number: TS1	Rev: 1
Date: Thursday, November 03, 2016	Sheet 73	of 103



Use 2nd source for layout. (Main source symbol not ready)

PD7405

	Main	2nd
Wistron PN	074.00432.0A3B	074.00431.0D3B
Vendor	TI	ON
Vendor PN	TL432IDBZR	NCP431AISNT1G

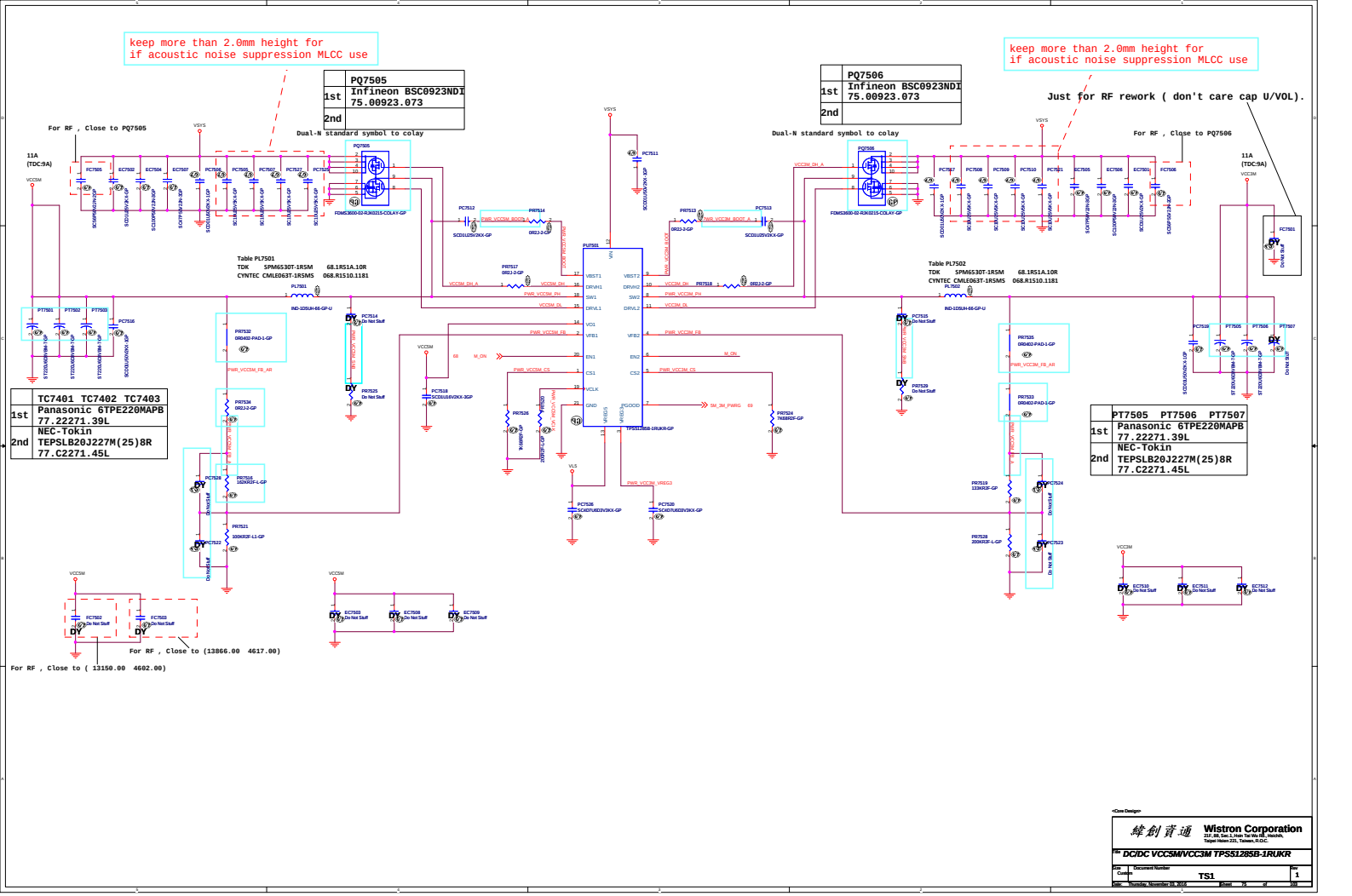
<Core Design>

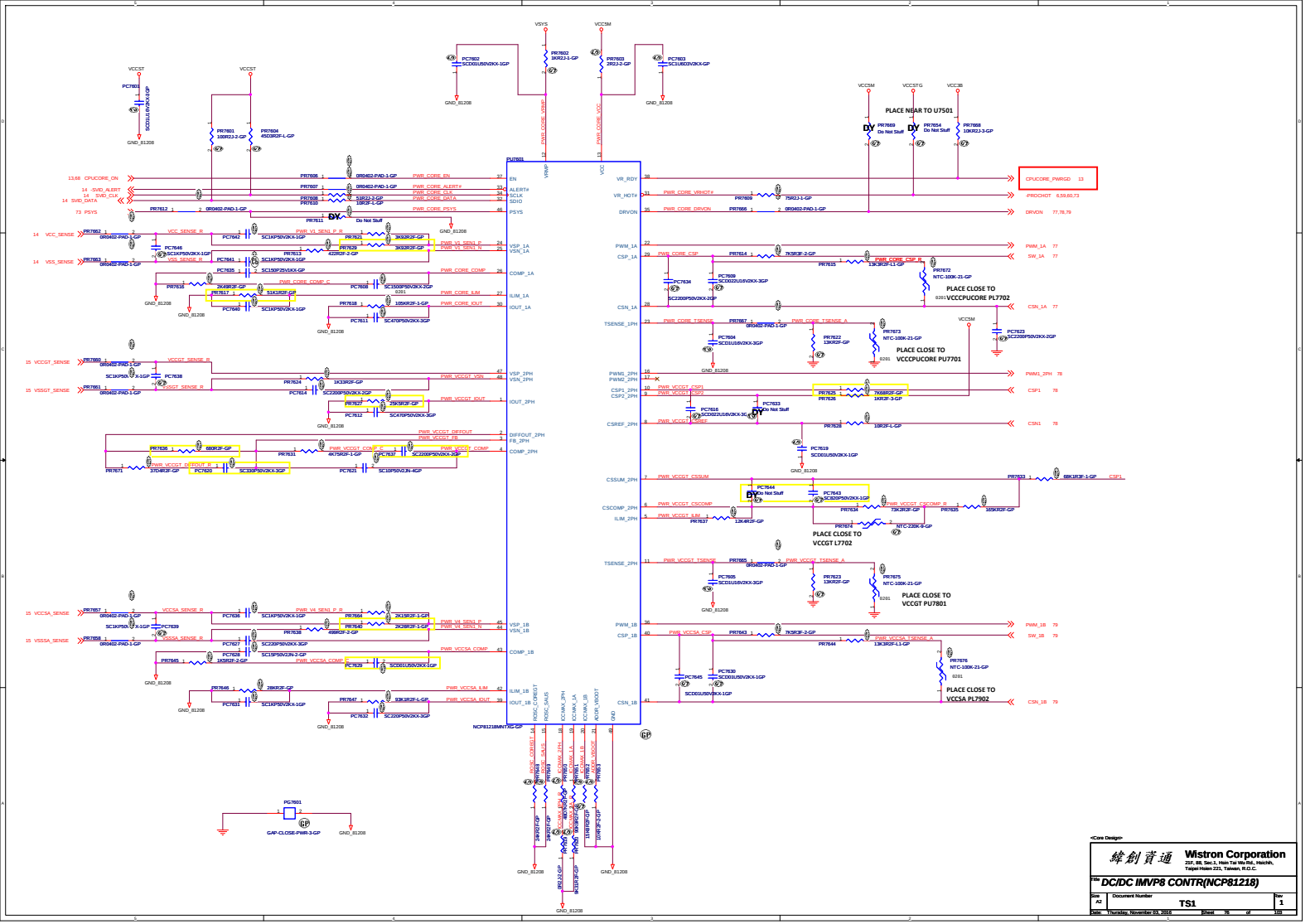
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER MONITOR**

Size	Document Number	Rev
Custom		

Date: Thursday, November 03, 2016 Sheet 74 of 103


keep more than 2.0mm height for
if acoustic noise suppression MLCC use
PQ7505
1st Infineon BSC0923NDI 75.00923.073
2nd
Dual-N standard symbol to colay
For RF , Close to PQ7505
11A (TDC:9A)
VCCIM
VSYS
PQ7506
1st Infineon BSC0923NDI 75.00923.073
2nd
keep more than 2.0mm height for
if acoustic noise suppression MLCC use
Just for RF rework (don't care cap U/VOL).
For RF , Close to PQ7506
Table PL7501
TDK SPM6530T-1R5M 68.1R1A.10R
CYNTEC CMLE063T-1R5MS 068.R1S10.1181
Table PL7502
TDK SPM6530T-1R5M 68.1R1A.10R
CYNTEC CMLE063T-1R5MS 068.R1S10.1181
TC7401 TC7402 TC7403
1st Panasonic 6TPE220MAPB 77.22271.39L
2nd NEC-Tokin TEPSLB20J227M(25)8R 77.C2271.45L
PT7505 PT7506 PT7507
1st Panasonic 6TPE220MAPB 77.22271.39L
2nd NEC-Tokin TEPSLB20J227M(25)8R 77.C2271.45L
PU7501
TPS51285B-1RUKR-GP
For RF , Close to (13866.00 4617.00)
For RF , Close to (13150.00 4602.00)
Wistron Corporation
DC/DC VCC5M/VCC3M TPS51285B-1RUKR
TS1



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC IMVP8 CONTR(NCP81218)

Size	Document Number	Rev
A2	TS1	1

Date: Thursday, November 03, 2016 Sheet 76 of 100

MLCCs must be placed
symmetrically on Top and Bottom.

keep more than 2.0mm height for
if acoustic noise suppression MLCC use

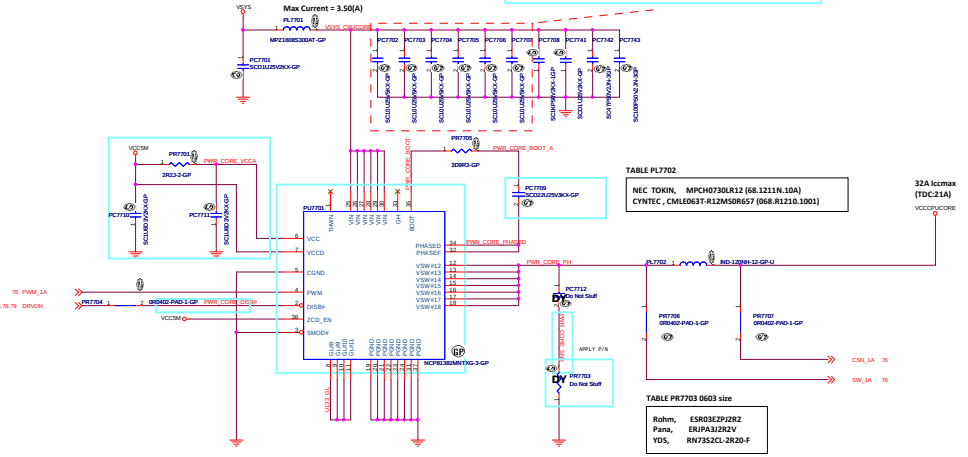


TABLE PL7702

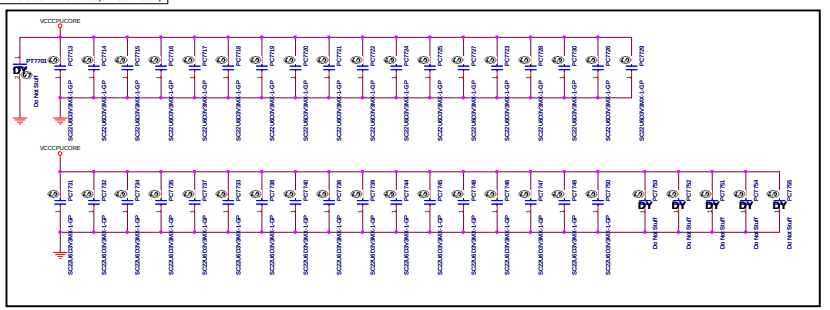
NEC TOKIN,	MPCH0730LR12 (68.1211N.10A)
CYNTEC ,	CMLE063T-R12MS0R657 (068.R1210.1001)

TABLE PR7703 0603 size

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
YDS,	RN73S2CL-2R20-F

TABLE for PT7701

NEC TOKIN	PSGB20E337M9 (80.3371V.A2L)
Panasonic	ETPE330MA9L (No Wistron P/N)
KEMET	T520B337M2R5ATE009 (077.C3371.0051)



22uF (0603) x 35 pcs
22uF (0603) x 5 pcs (DY)
330uF x 1 pcs (DY)

<Core Design>

緯創資通	Wistron Corporation
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

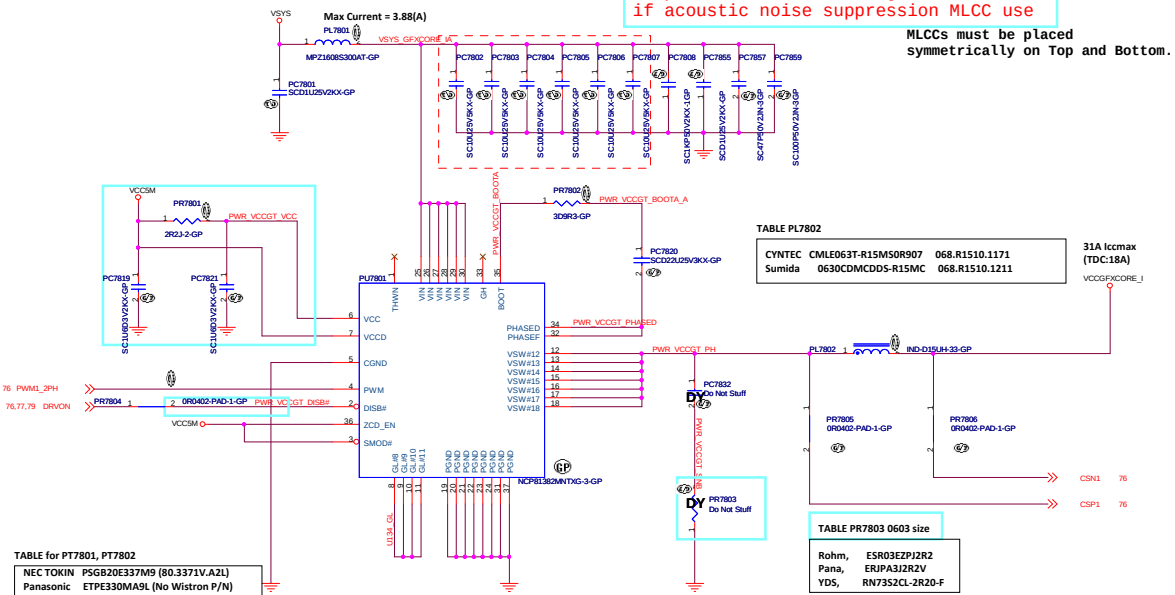
Title: DC/DC VCCCPUCORE(NCP81382)

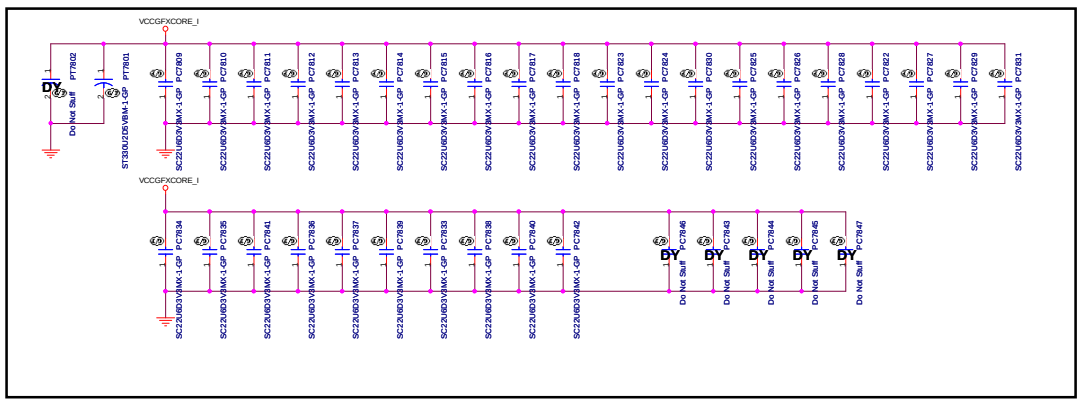
Size	Document Number	Rev
A2	TS1	1

Date: Friday, November 04, 2016 Sheet 77 of 103

keep more than 2.0mm height for
if acoustic noise suppression MLCC use

MLCCs must be placed
symmetrically on Top and Bottom.





22uF (0603) x 30 pcs
330uF x 1pcs
22uF (0603) x 5 pcs (DY)
330uF x 1 pcs (DY)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

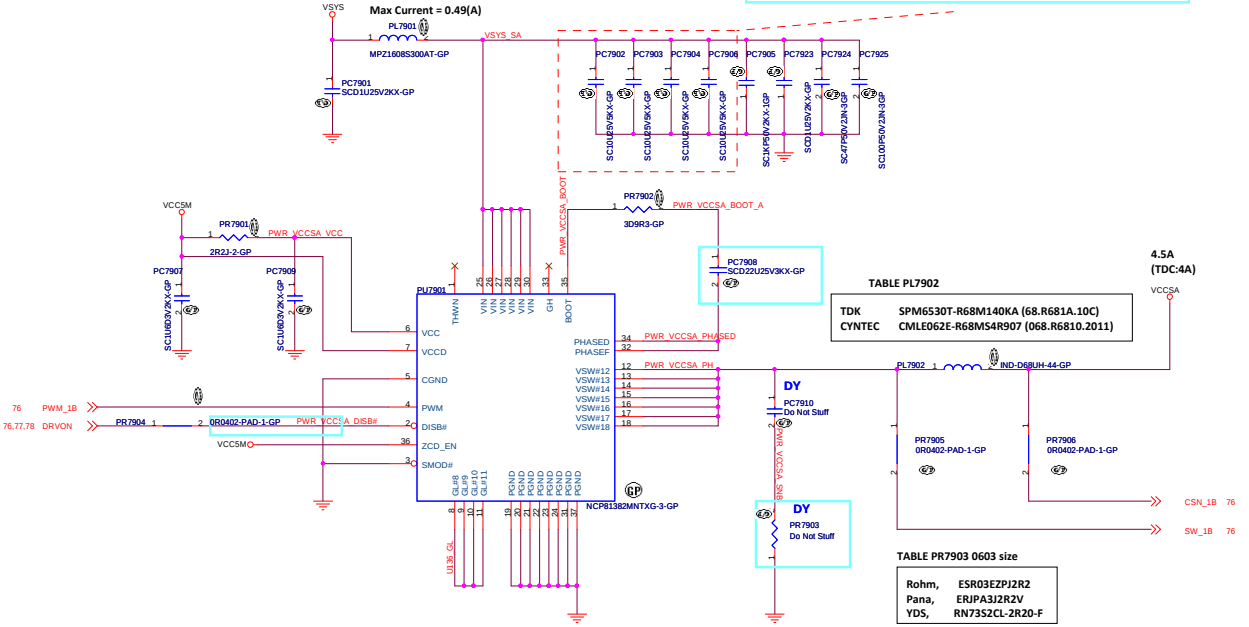
Title: DC/DC VCCGFXCORE_I(NCP81382

Size	Document Number	Rev
Custom	TS1	1

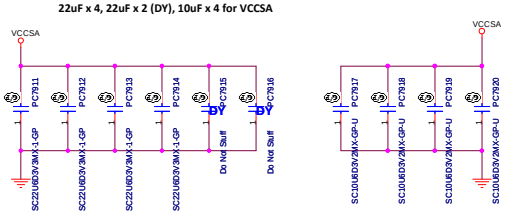
Date: Thursday, November 03, 2016 Sheet 78 of 103

MLCCs must be placed
symmetrically on Top and Bottom.

keep more than 2.0mm height for
if acoustic noise suppression MLCC use



22uF x 4, 22uF x 2 (DY), 10uF x 4 for VCCSA



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC VCCSA(NCP81380)

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 79 of 103

BLANK

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *N/A*		
Size: A4	Document Number: TS1	Rev: 1
Date: Thursday, November 03, 2016	Sheet 80 of 103	

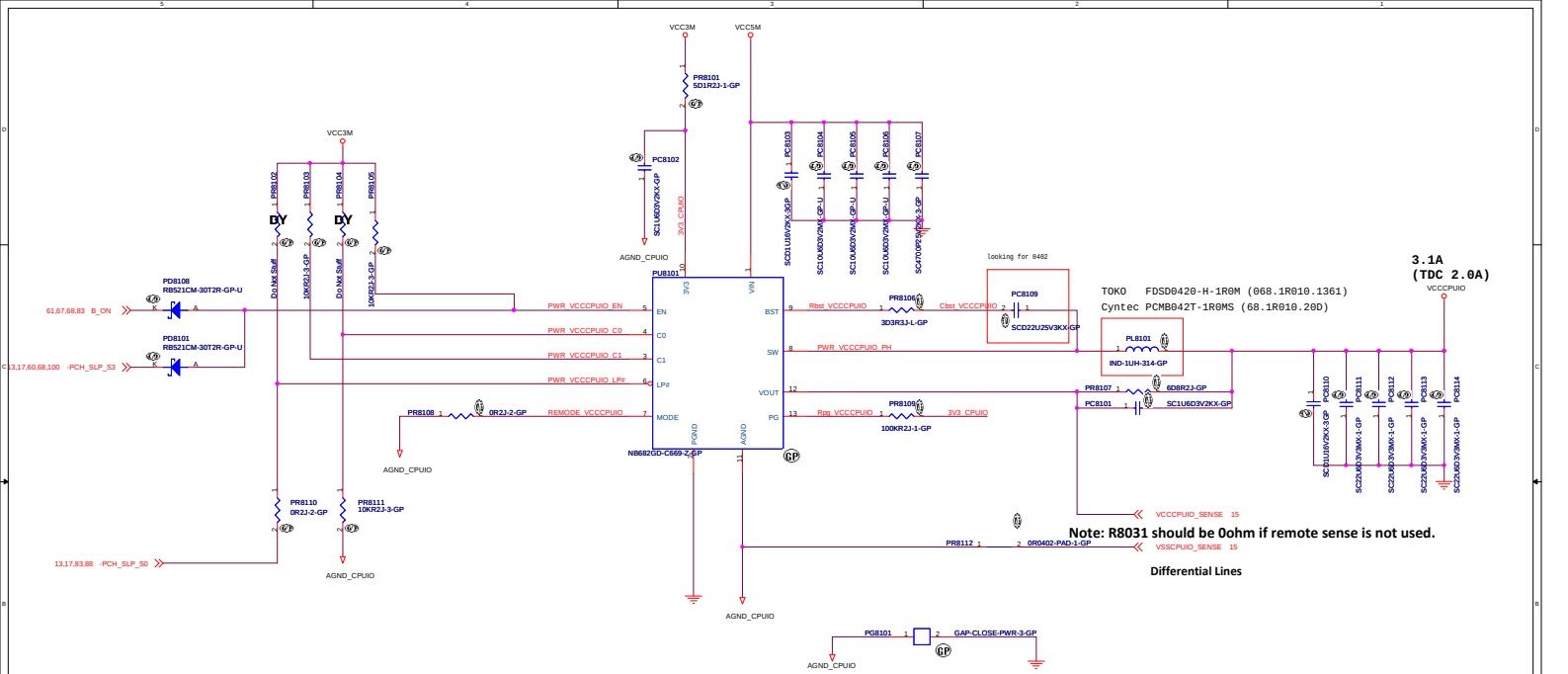


TABLE : NB682 MODE M1 (0 to GND)

LP#	C1	C0	VOUT	
0	X	X	0.000V	← SLP_S0#
1	0	0	0.850V	
1	0	1	0.875V	
1	1	0	0.950V	← LOGIC
1	1	1	0.975V	

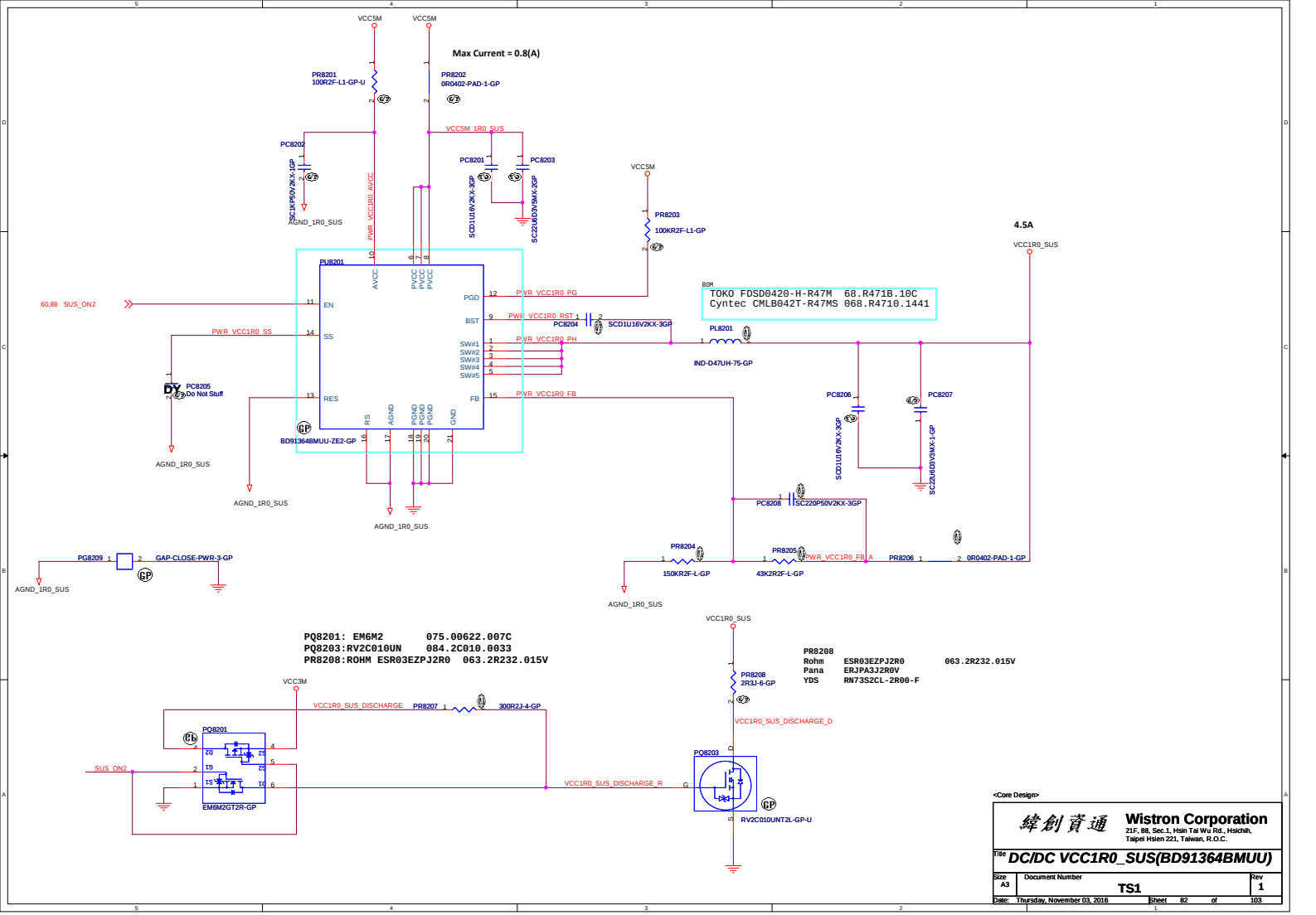
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC/DC VCCCPUIO(NB682)**

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 81 of 103



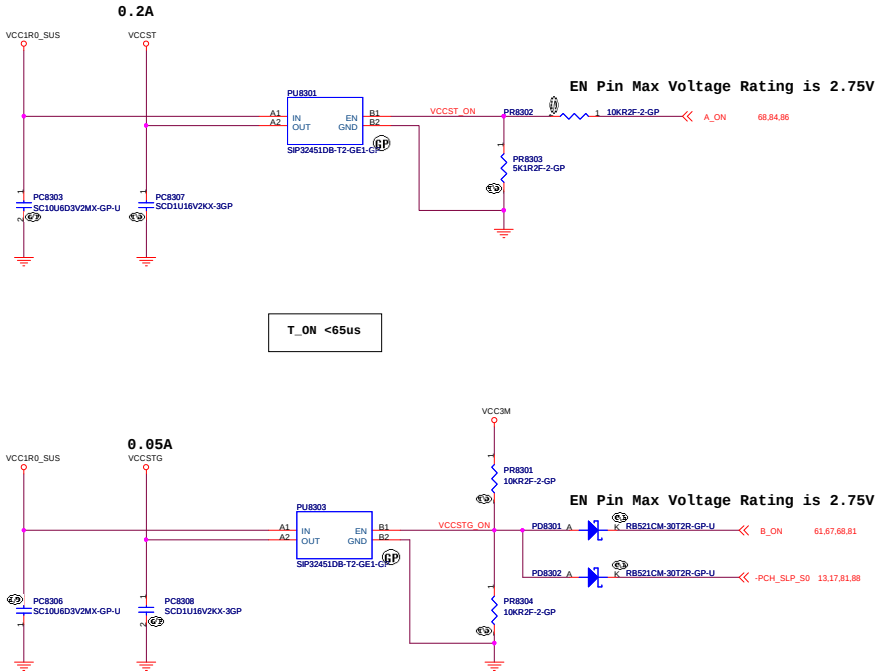
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DC/DC VCC1R0_SUS(BD91364BMUU)*

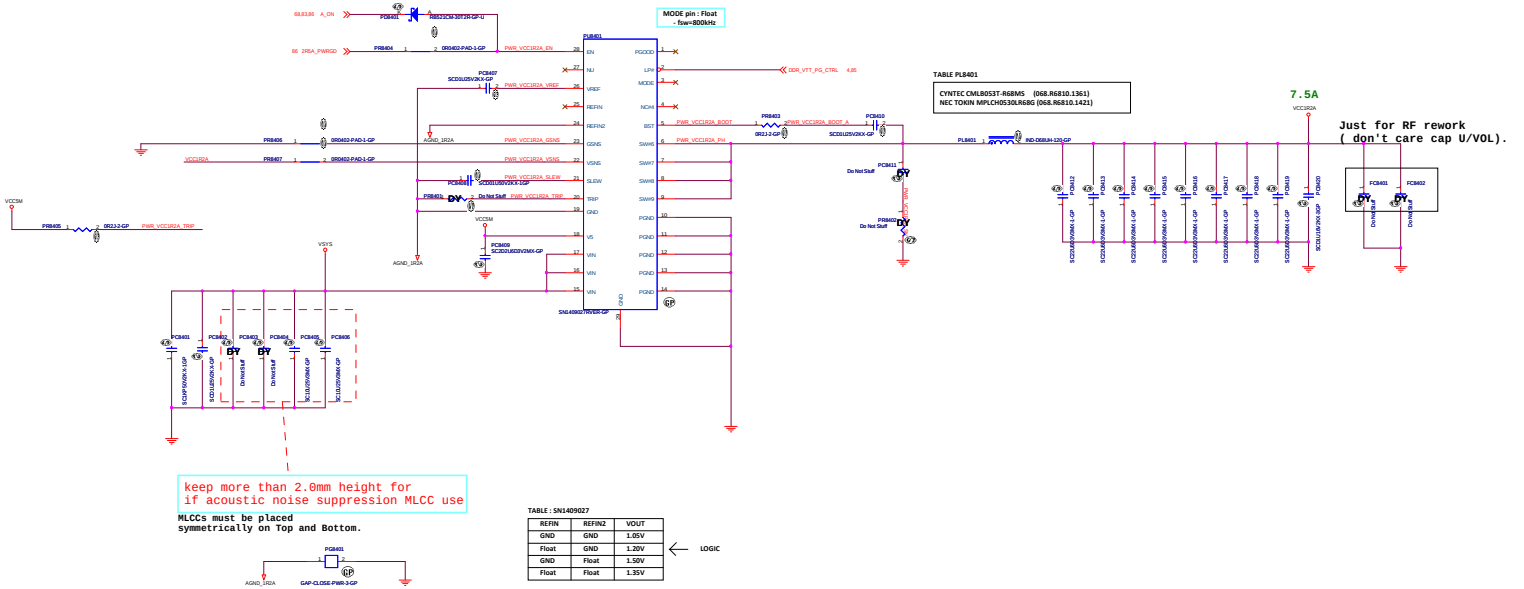
Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 82 of 103



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: LOAD SW VCCST & VCCSTG		
Size: A3	Document Number: TS1	Rev: 1
Date: Thursday, November 03, 2016	Sheet 83 of 103	



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

DC/DC VCC1R2A

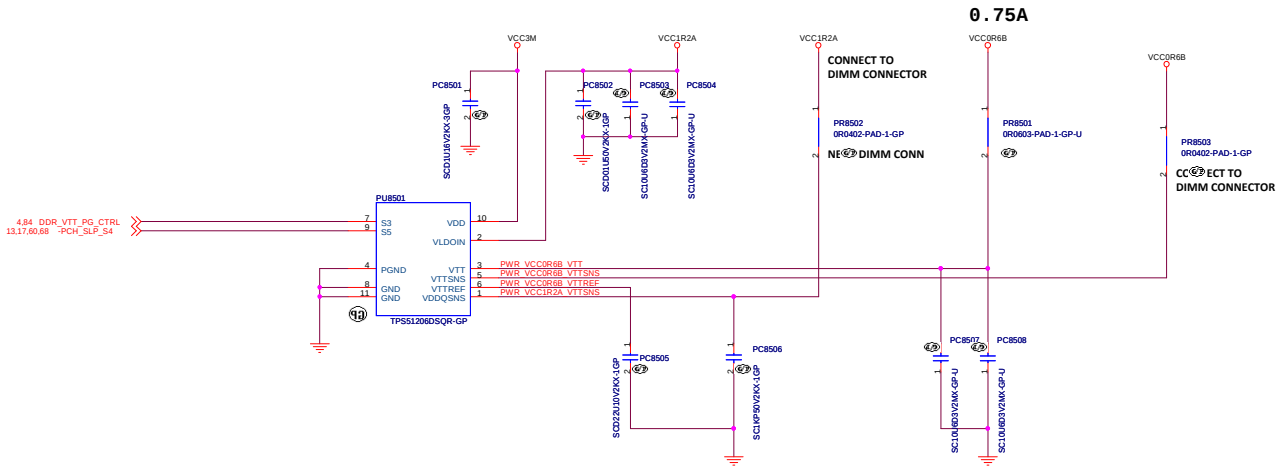


TABLE: TPS51206

S3	S5	VTT	VTTREF
High	High	ON	ON
Low	High	OFF(High-Z)	ON
Low	Low	OFF(Discharge)	OFF(Discharge)

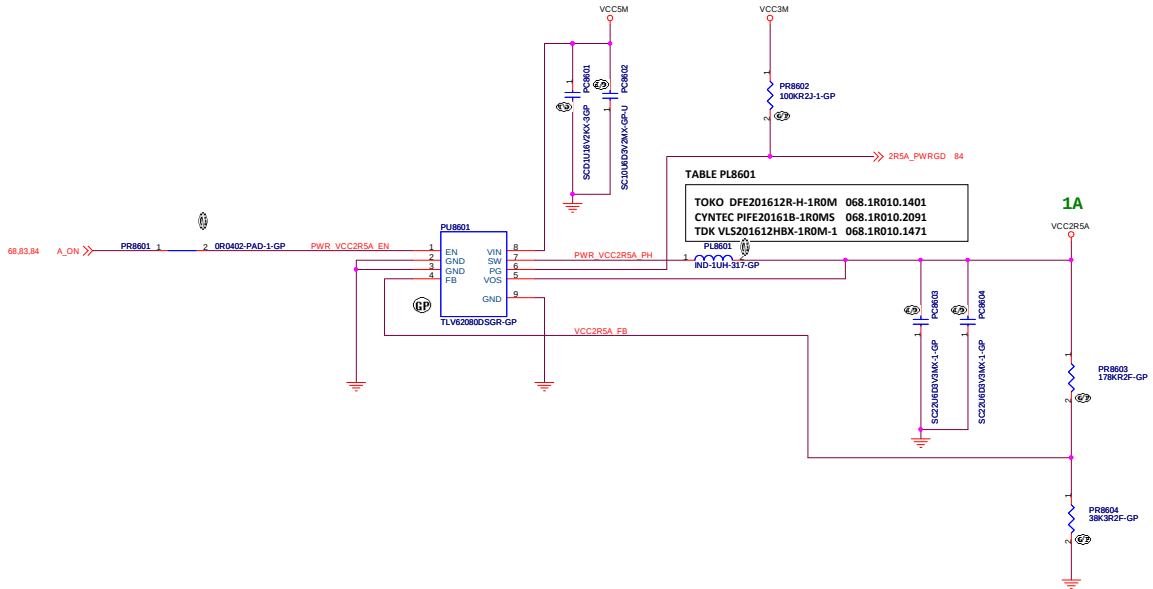
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DC/DC VCC0R6B***

Size	Document Number	Rev
A3		

Date: Thursday, November 03, 2016 Sheet 85 of 103



<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DC/DC VCC2R5A
Size A3	Document Number
Rev	
Date: Thursday, November 03, 2016	Sheet 86 of 103

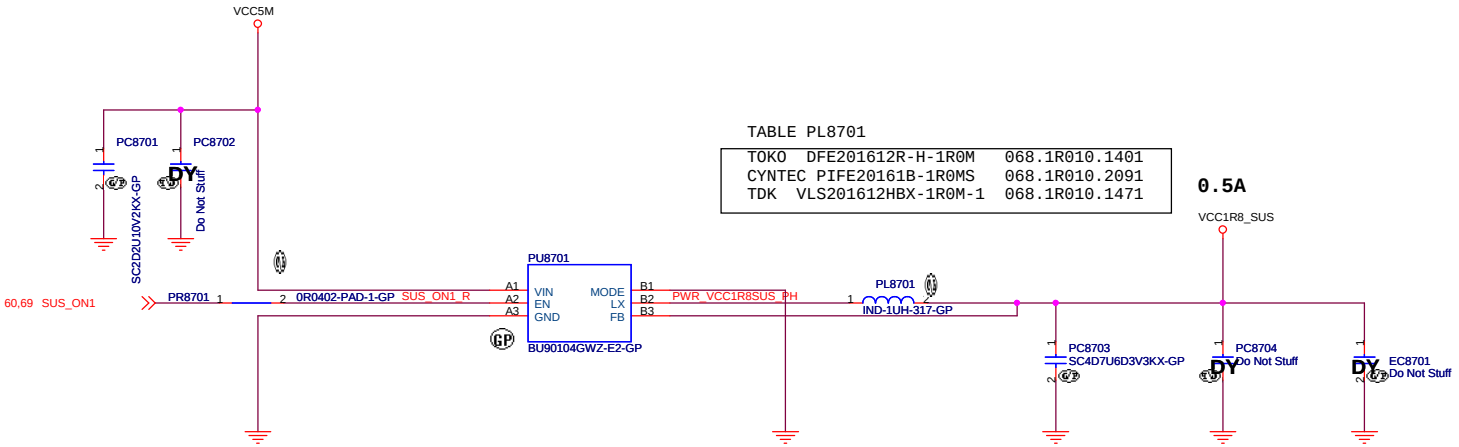


TABLE PL8701

TOKO	DFE201612R-H-1R0M	068.1R010.1401
CYNTEC	PIFE20161B-1R0MS	068.1R010.2091
TDK	VLS201612HBX-1R0M-1	068.1R010.1471

0.5A

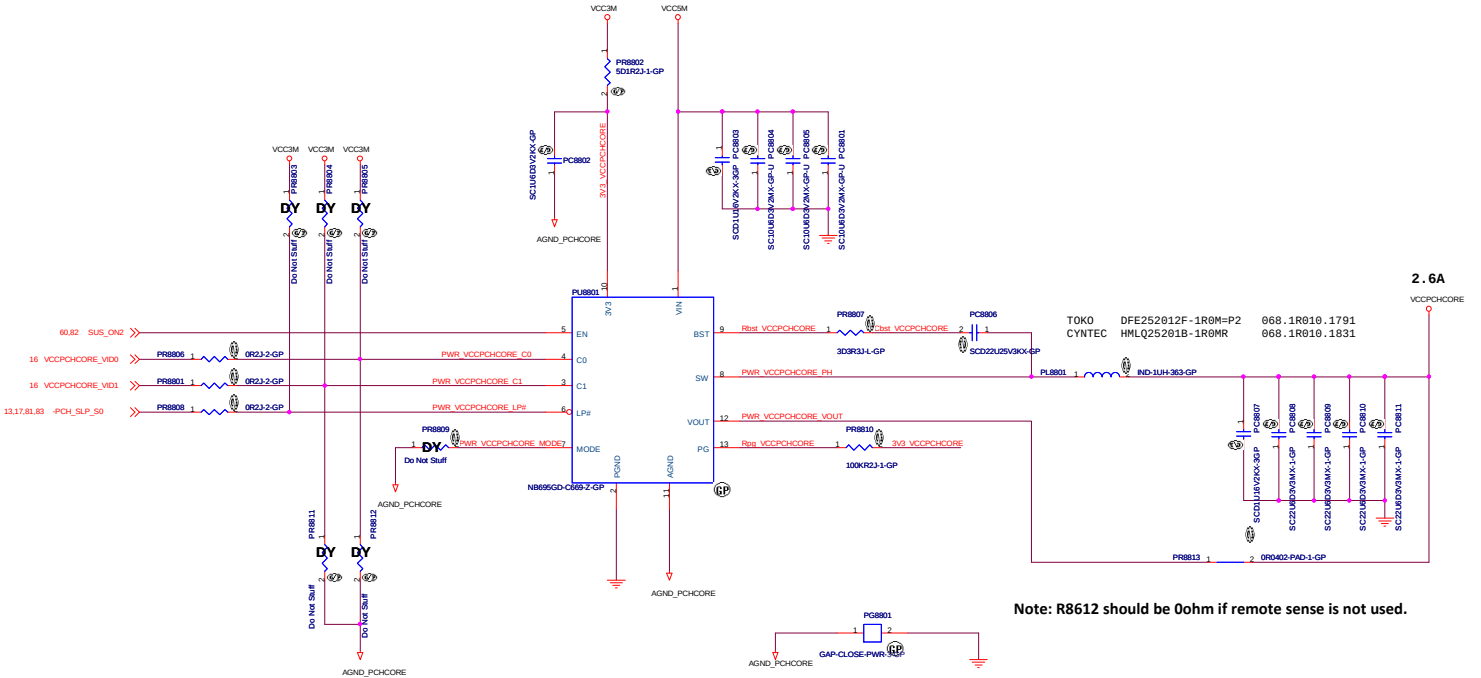
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DC/DC VCC1R8_SUS***

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 87 of 103



Note: R8612 should be 0ohm if remote sense is not used.

TABLE : NB682 MODE M2 (Float) - ES

LP#	C1	C0	VOUT	
0	X	X	0.700V	← SLP_S0#
1	0	0	0.850V	
1	0	1	0.900V	
1	1	0	0.950V	
1	1	1	1.000V	← DEFAULT

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *086_DC/DC VCCPCHCORE(NB682)*

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 88 of 103

BLANK

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BLANK***	
Size: A	Document Number: **TS1**	Rev: **1**
Date: Thursday, November 03, 2016	Sheet 89 of 103	

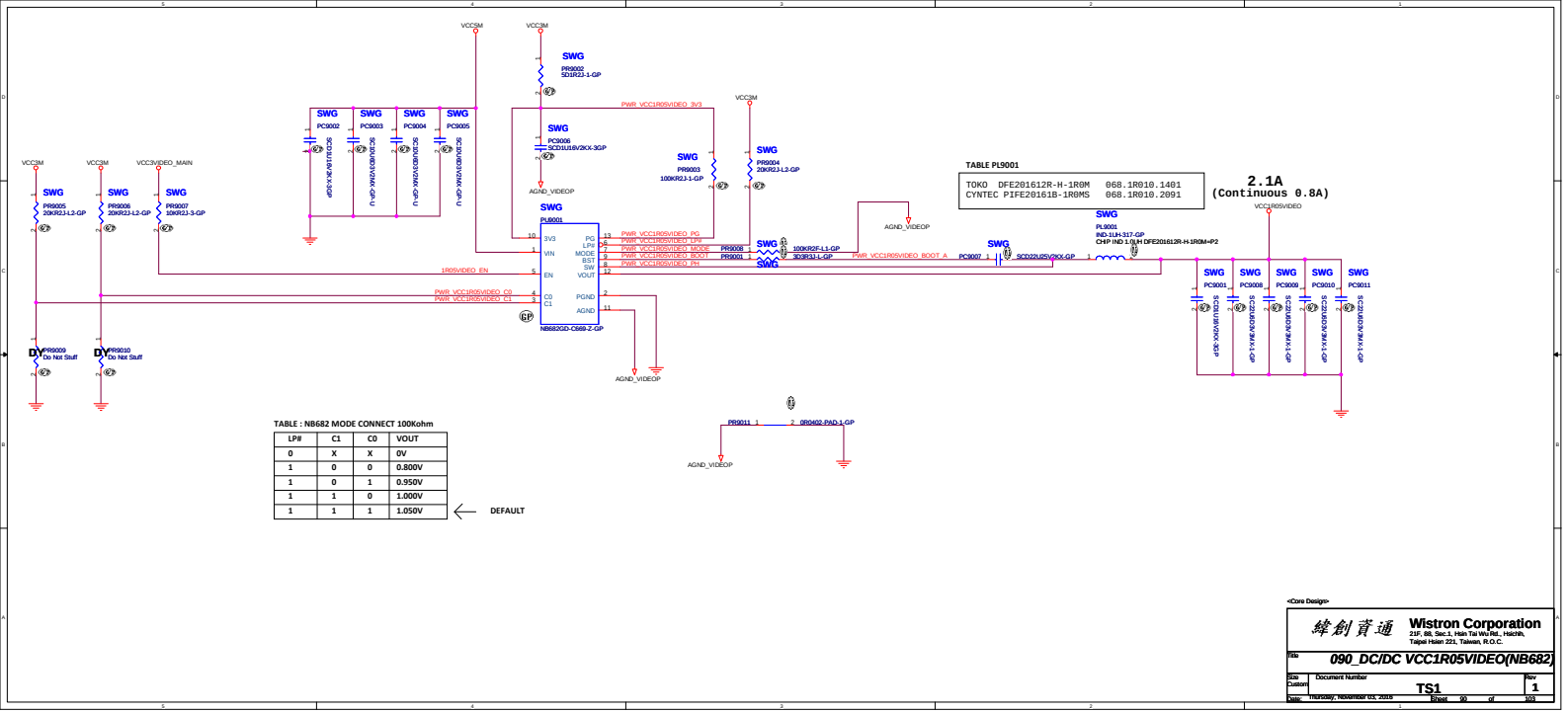


TABLE PL9001

TOKO DFE201612R-H-1R0M	068.1R010.1401
CYNTEC PIFE20161B-1R0MS	068.1R010.2091

TABLE : NB682 MODE CONNECT 100Kohm

LP#	C1	C0	VOUT	
0	X	X	0V	
1	0	0	0.800V	
1	0	1	0.950V	
1	1	0	1.000V	
1	1	1	1.050V	← DEFAULT

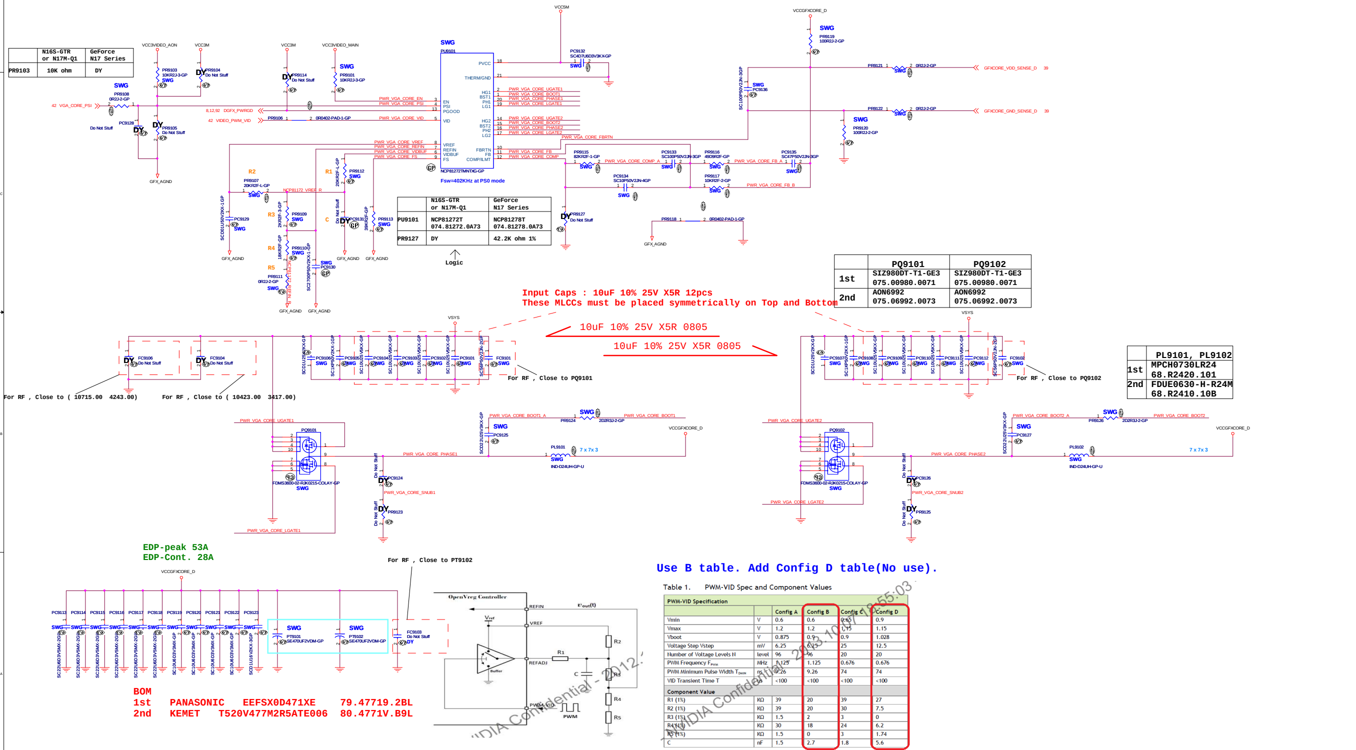
<Core Design>

蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: 090_DC/DC VCC1R05VIDEO(NB682)

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 04, 2010 Sheet 90 of 103



	N16S-GTR or N17M-Q1	GeForce N17 Series
PR9103	10K ohm	DY

	N16S-GTR or N17M-Q1	GeForce N17 Series
PU9101	NCP81272T 074.81272.0A73	NCP81278T 074.81278.0A73
PR9127	DY	42.2K ohm 1%

	PQ9101	PQ9102
1st	SIZ980DT-T1-GE3 075.00980.0071	SIZ980DT-T1-GE3 075.00980.0071
2nd	AON6992 075.06992.0073	AON6992 075.06992.0073

	PL9101, PL9102
1st	MPCH0730LR24 68.R2420.101
2nd	FDUE0630-H-R24M 68.R2410.10B

BOM

1st	PANASONIC	EEFSX0D471XE	79.47719.2BL
2nd	KEMET	T520V477M2R5ATE006	80.4771V.B9L

Use B table. Add Config D table(No use).

Table 1. PWM-VID Spec and Component Values

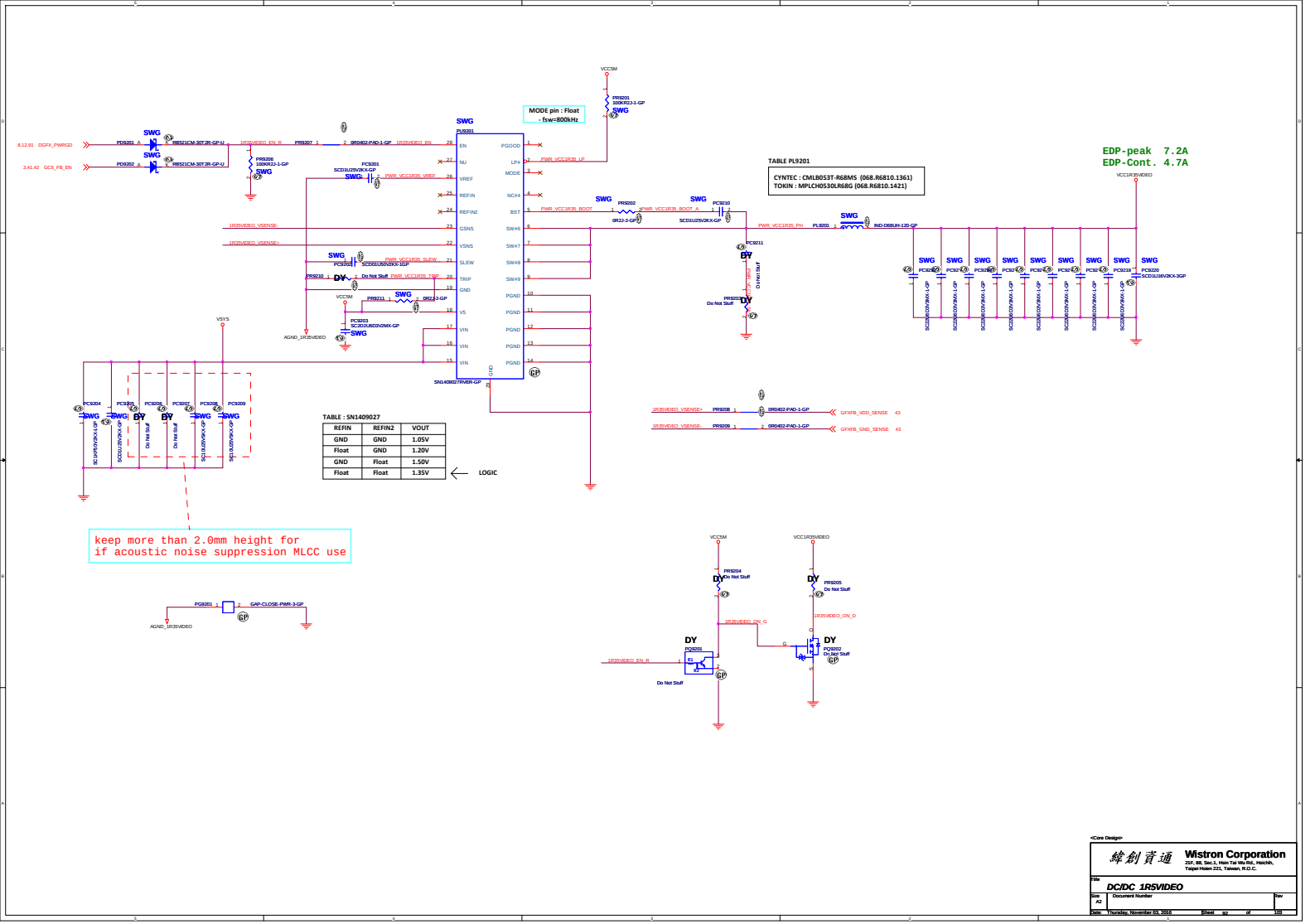
PWM-VID Specification		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.15	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26	74	74
VID Transient Time T	us	<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	20	39	27
R2 (1%)	KΩ	39	20	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	18	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

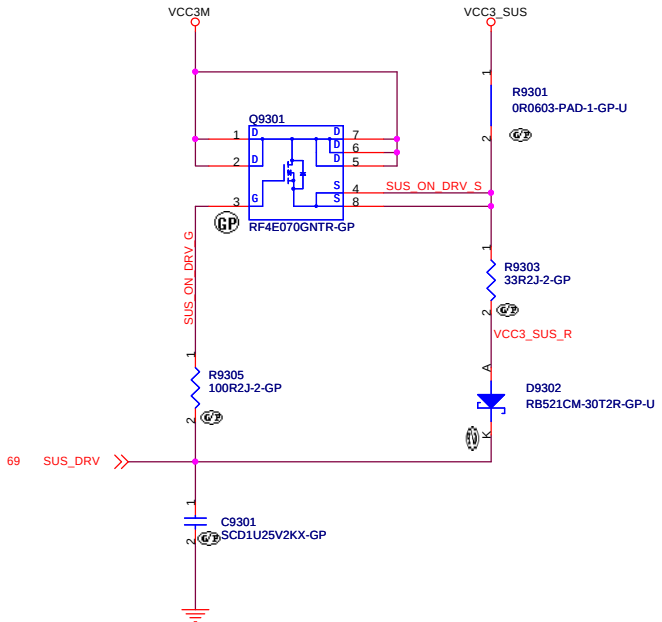
Title: **DC/DC VCCGFXCORE_D(NCP81172)**

Size: D | Document Number | Rev

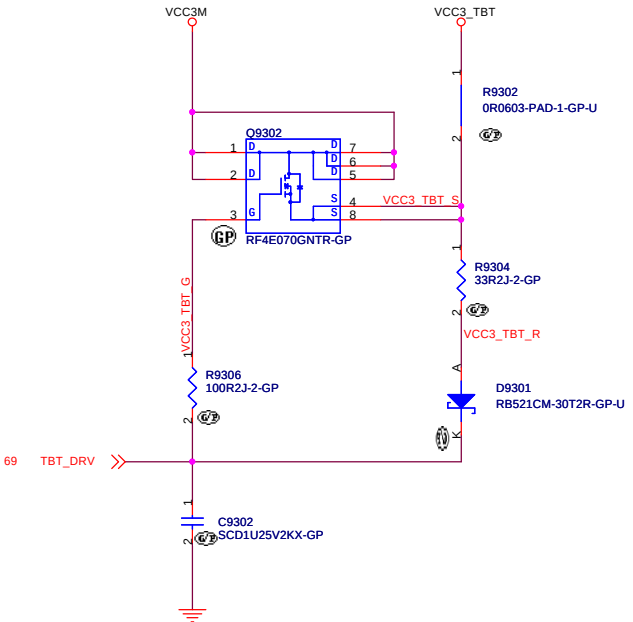

MODE pin : Float
- fsw=800kHz
EDP-peak 7.2A
EDP-Cont. 4.7A
TABLE PL9201
CYNTEC : CMLB053T-R68MS (068.R6810.1361)
TOKIN : MPLCH0530LR68G (068.R6810.1421)
TABLE : SN1409027
REFIN | REFIN2 | VOUT
GND | GND | 1.05V
Float | GND | 1.20V
GND | Float | 1.50V
Float | Float | 1.35V
LOGIC
keep more than 2.0mm height for
if acoustic noise suppression MLCC use
SN1409027RVER-GP
PL9201
PD9201
PD9202
PR9201
PR9202
PR9203
PR9204
PR9205
PR9206
PR9207
PR9208
PR9209
PR9210
PR9211
PC9201
PC9202
PC9203
PC9204
PC9205
PC9206
PC9207
PC9208
PC9209
PC9210
PC9211
PC9212
PC9213
PC9214
PC9215
PC9216
PC9217
PC9218
PC9219
PC9220
PQ9201
PQ9202
PG9201
VCC5M
VCC1R35VIDEO
VSYS
AGND_1R35VIDEO
1R35VIDEO_VSENSE-
1R35VIDEO_VSENSE+
PWR_VCC1R35_LP
PWR_VCC1R35_BOOT
PWR_VCC1R35_BOOT_A
PWR_VCC1R35_PH
PWR_VCC1R35_VREF
PWR_VCC1R35_SLEW
PWR_VCC1R35_TRIP
1R35VIDEO_EN_R
1R35VIDEO_ON_G
1R35VIDEO_ON_D
GFXFB_VDD_SENSE
GFXFB_GND_SENSE
Do Not Stuff
CAP-CLOSE-PWR-3-GP
IND-D8BUH-120-GP
Wistron Corporation
DC/DC 1R5VIDEO

Q9301 Q9302		
Vendor	Venor PN	Wistron PN
Rohm	RF4E070GN (1st source)	084.4E070.0037
Fairchild	FDMA7672 (2nd source)	084.07672.M001

0.8A



1A



<Core Design>

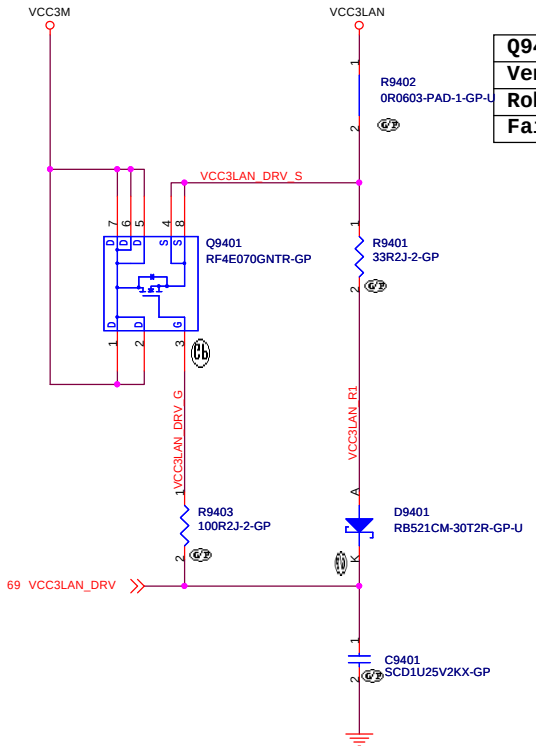
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LOAD SW PCH SUS/TRACK POINT***

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 93 of 103

0.5A



Q9401		
Vendor	Venor PN	Wistron PN
Rohm	RF4E070GN (1st source)	084.4E070.0037
Fairchild	FDMA7672 (2nd source)	084.07672.M001

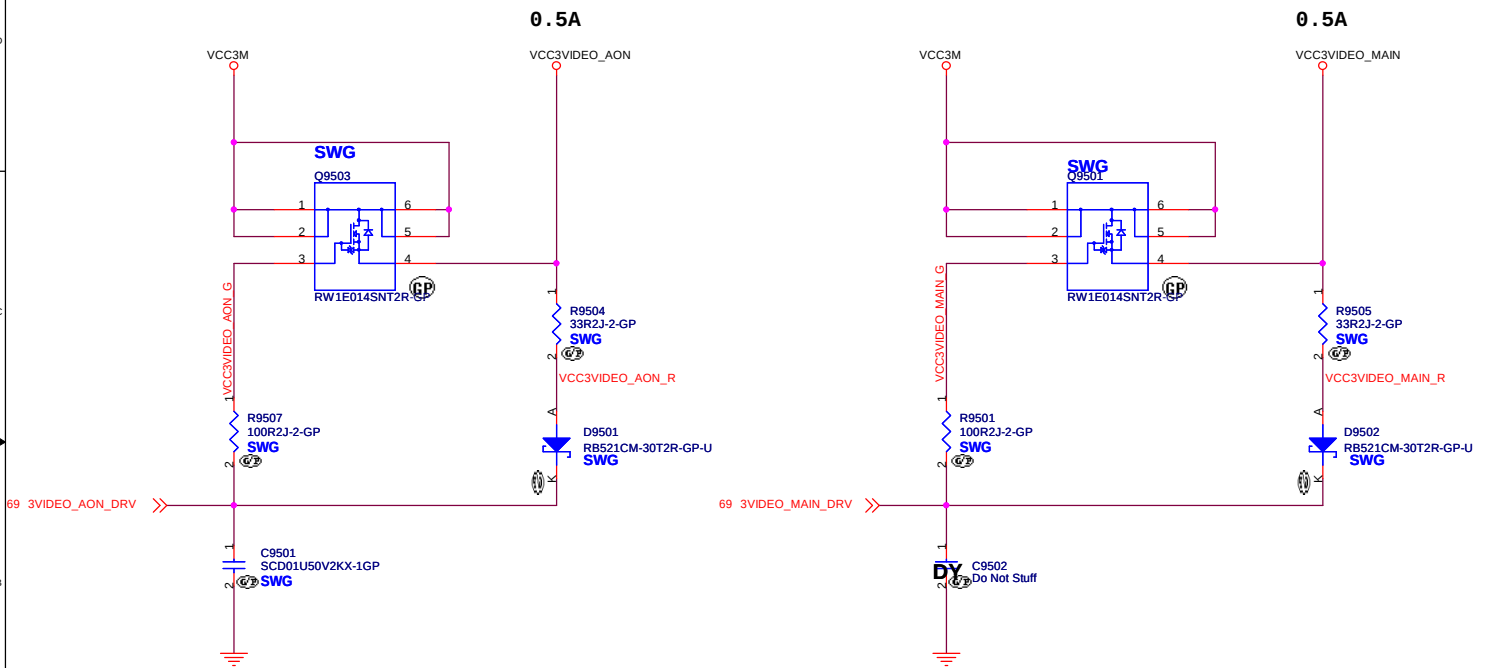
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LOAD SW LAN

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 94 of 103



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LOAD SW VIDEO***

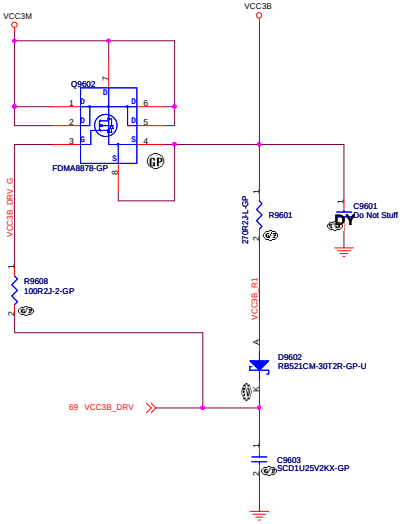
Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 95 of 103

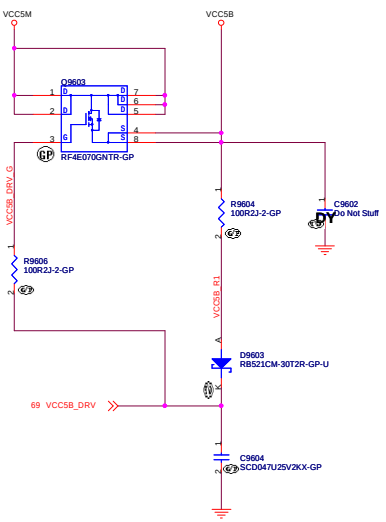
Q9602
FDMA8878 Fairchild 84.08878.030
SiA462DJ Vishay 084.00462.003D

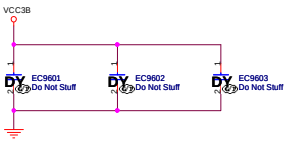
Q9603		
Vendor	Venor PN	Wistron PN
Rohm	RF4E070GN (1st source)	084.4E070.0037
Fairchild	FDMA7672 (2nd source)	084.07672.M001

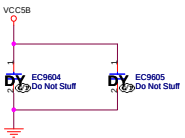
8.5A Peak
6.0A Cont.



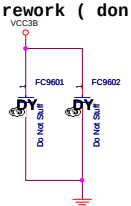
3.5A







Just for RF rework (don't care cap U/VOL).



<Core Design>

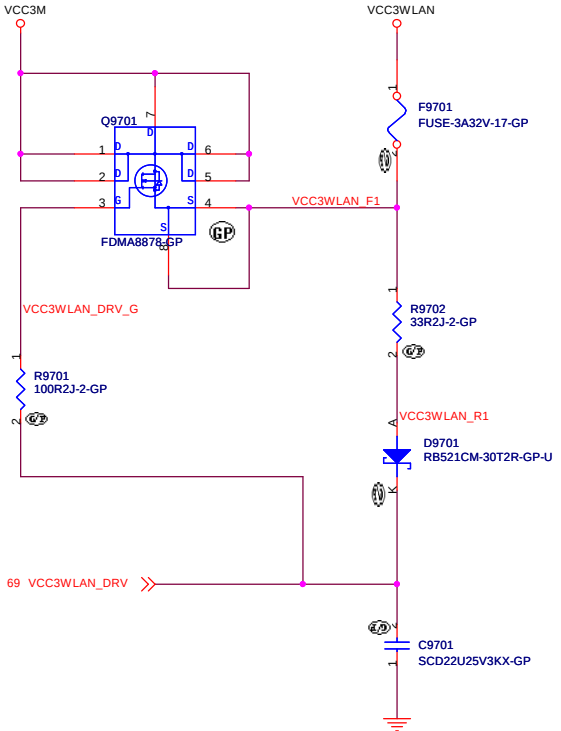
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LOAD SW B

Size: A3 | Document Number: TS1 | Rev: 1

Date: Thursday, November 03, 2016 | Sheet 96 of 103

2.5A peak
1.1A Cont

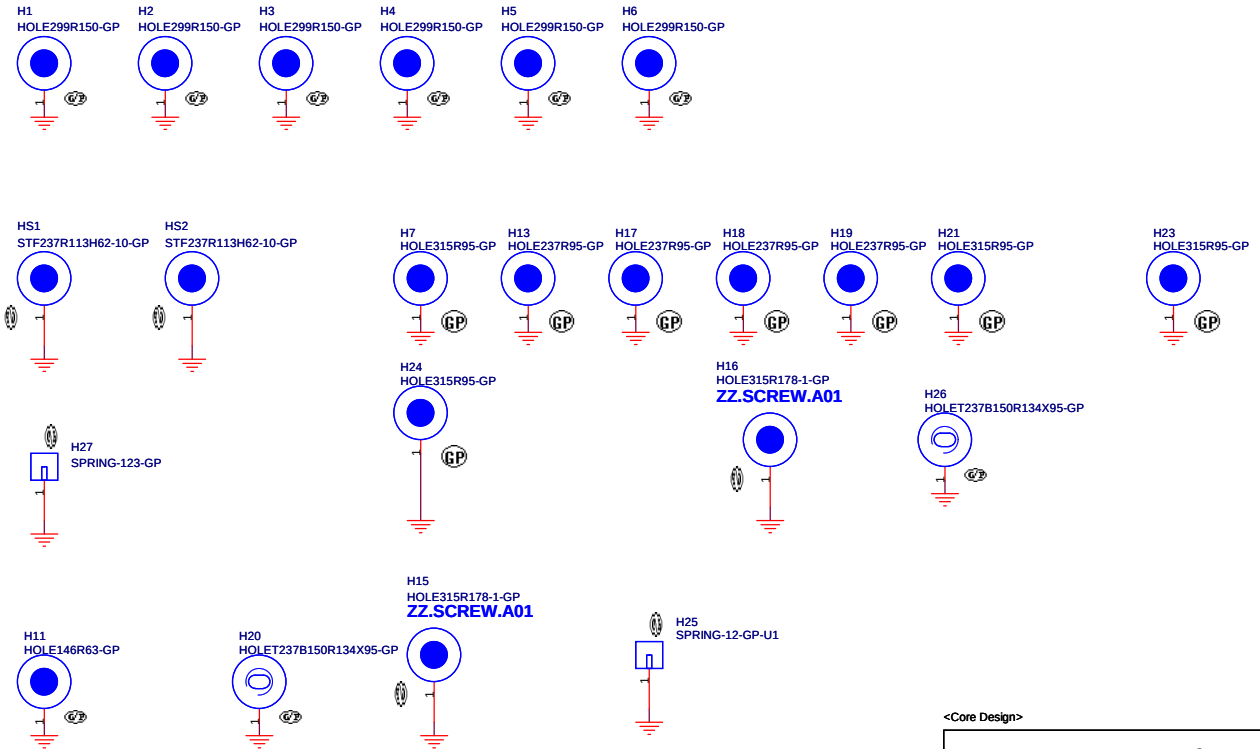


Q9701
1st : Fairchild FDMA8878 84.08878.030
2nd : Vishay SiA462DJ 084.00462.003D

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***LOAD SW WLAN***	
Size A4	Document Number **TS1**	Rev **1**
Date: Thursday, November 03, 2016	Sheet 97 of 103	



<Core Design>

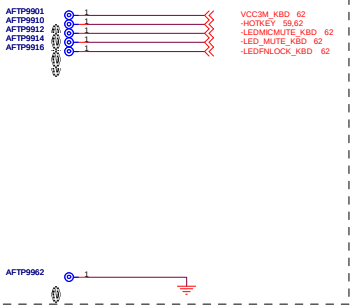
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PTH FOR SCREW HOLES***

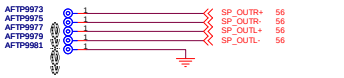
Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 98 of 103

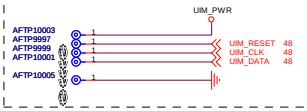
Near KB1(Keyboard connector)



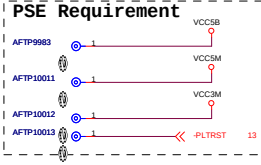
Near SPK1(Speaker)



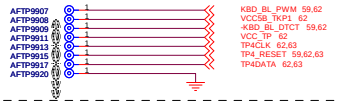
Near SIM1(SIM Card)



PSE Requirement



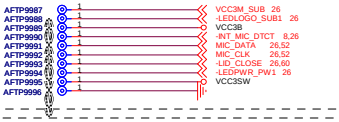
Near TKP1(Track point connector)



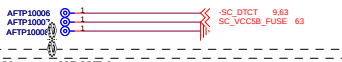
Near FAN1(FAN Connector)

Near RTC1(RTC Battery)

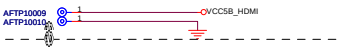
Near SUB1(Mic/CCD/Lid/Touch Screen)



Near SUB2(SMART CARD)



Near HDMI1

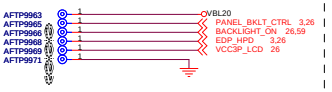


Near DC1(Adapter in)

Near BAT1(Battery in)

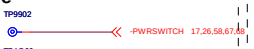
Near BAT2(Battery in)

Near LCD1(eDP connector)



For Power Switch

Top side



Bottom side

Near USB3(USB 3.0 conn)

Near USB2(USB 3.0 conn)

Near USB1(USB 3.0 conn)

Near MCS1 (MediaCard Slot)

Near PW1(Power Button)

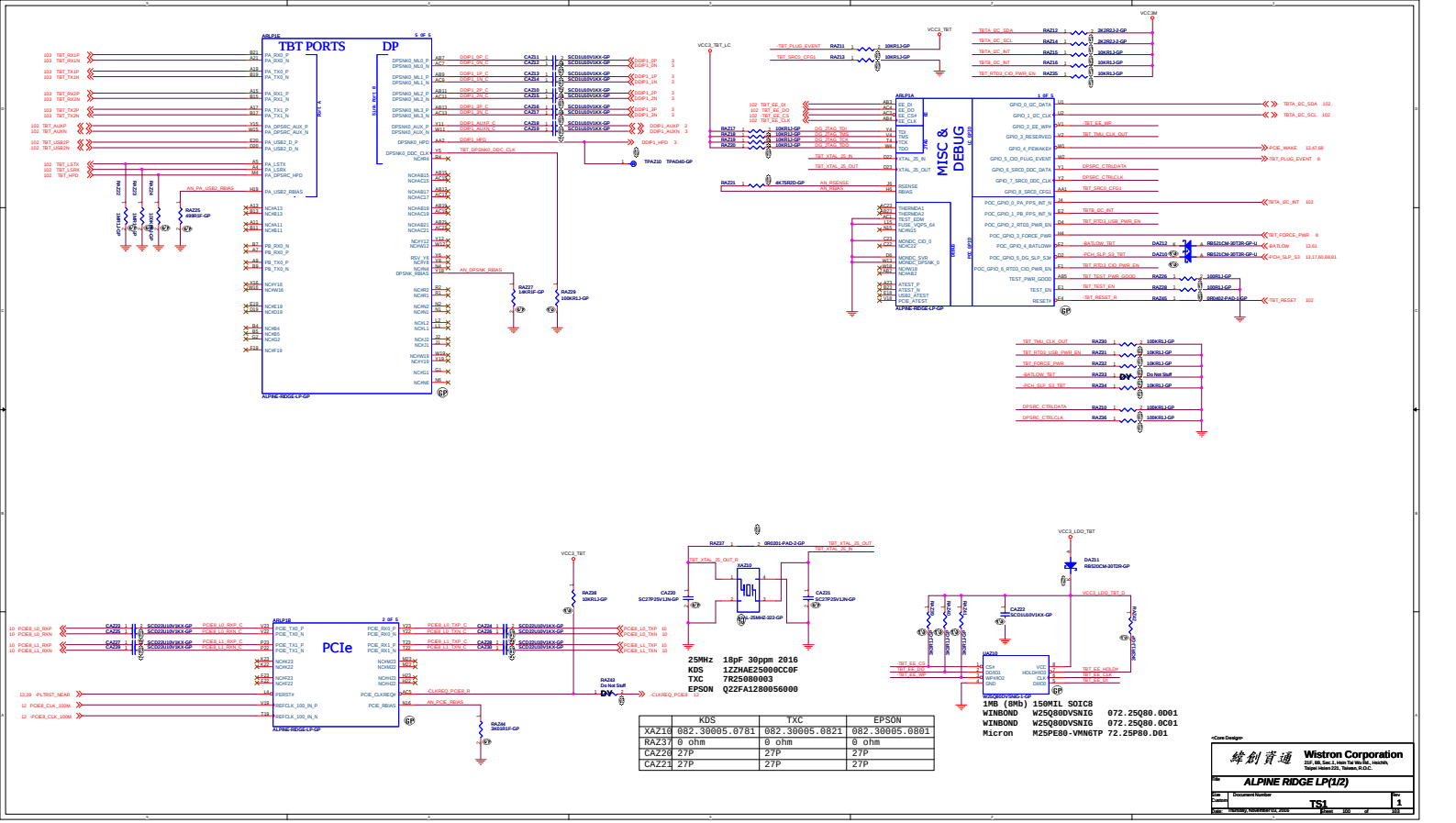
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Test Pad(AFTP)

Size: Custom | Document Number: TS1 | Rev: 1

Date: Thursday, November 03, 2016 | Sheet 99 of 103



	KDS	TXC	EPSON
XAZ10	082.30005.0781	082.30005.0821	082.30005.0801
RAZ37	0 ohm	0 ohm	0 ohm
CAZ20	27P	27P	27P
CAZ21	27P	27P	27P

25MHz 18pF 30ppm 2016
KDS 1ZZHAE25000CC0F
TXC 7R25000003
EPSON Q22FA1280056000

1MB (8Mb) 150MIL SOIC8
WINBOND W25Q80DVSNIG 072.25Q80.0D01
WINBOND W25Q80DVSNIG 072.25Q80.0C01
Micron M25PE80-VMN6TP 72.25P80.D01

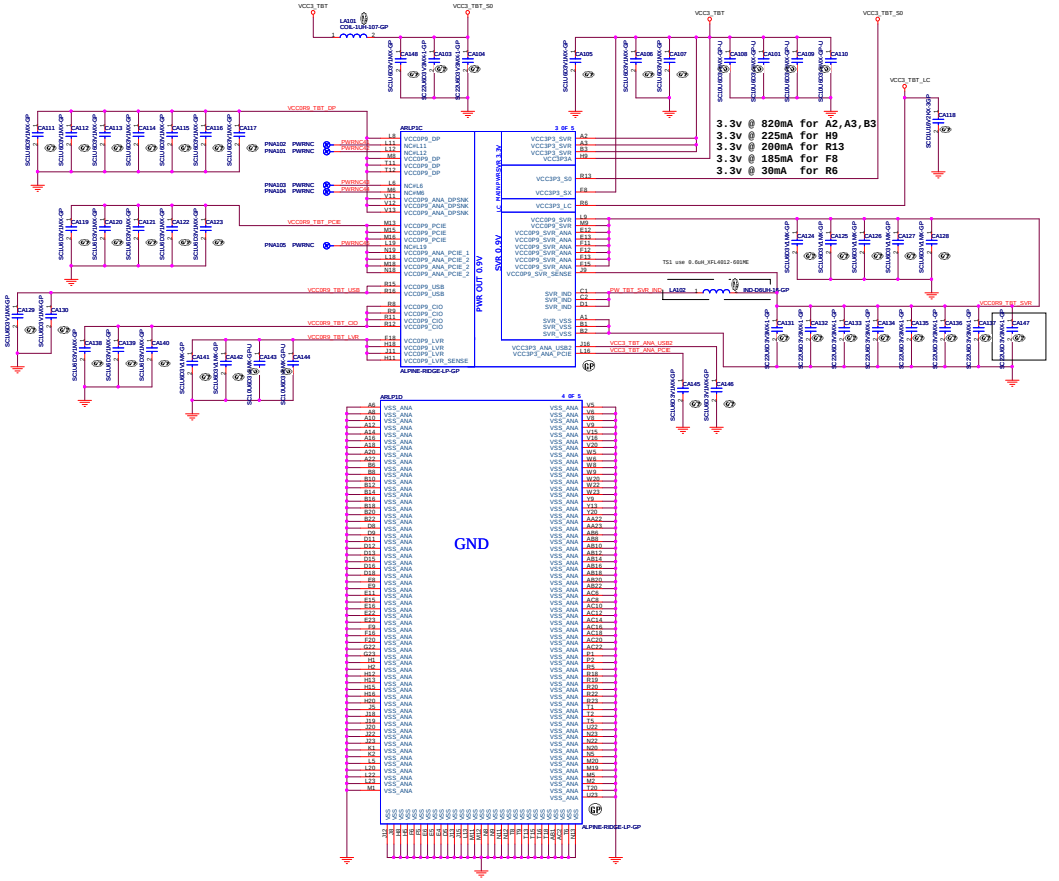


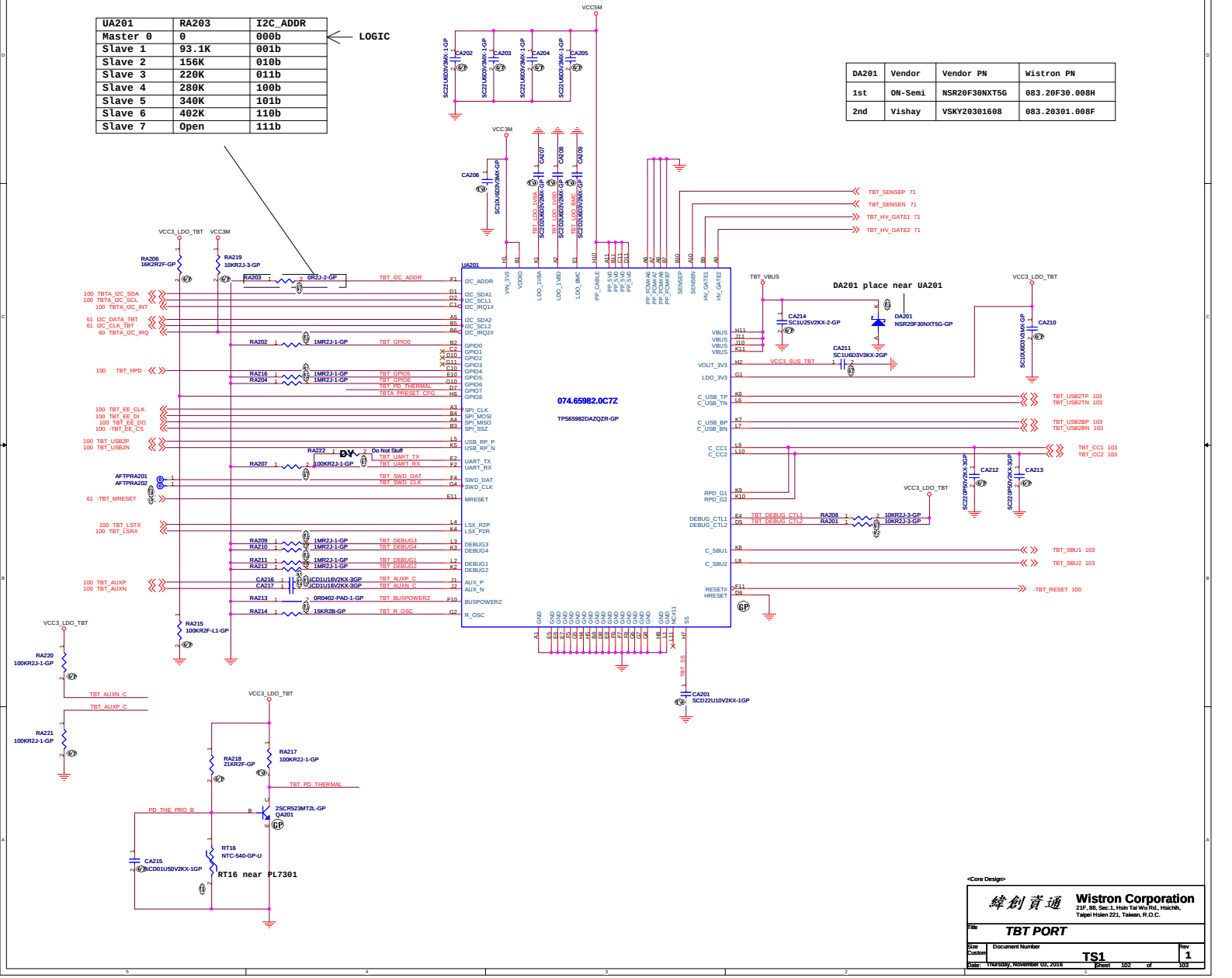
TABLE: TPS65982 I2C Address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	DEBUG_CTL2	DEBUG_CTL1	I2C_ADDR			R/W

UA201	RA203	I2C_ADDR
Master 0	0	000b
Slave 1	93.1K	001b
Slave 2	156K	010b
Slave 3	220K	011b
Slave 4	280K	100b
Slave 5	340K	101b
Slave 6	402K	110b
Slave 7	Open	111b

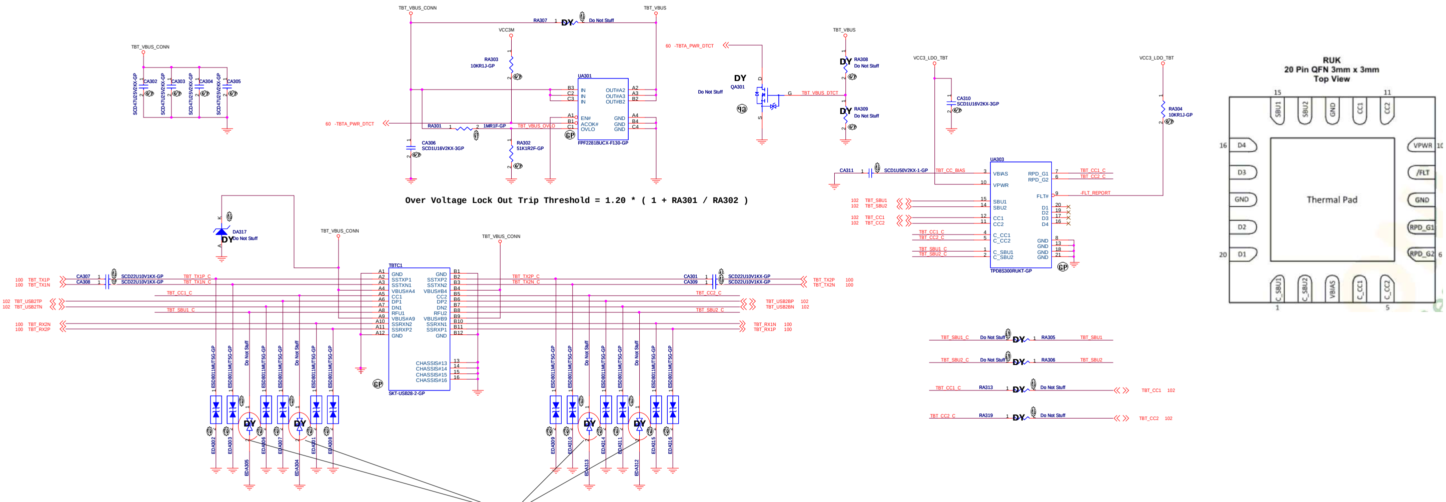
LOGIC

DA201	Vendor	Vendor PN	Wistron PN
1st	ON-Semi	NSR20F30NXT5G	083.20F30.008H
2nd	Vishay	VSKY20301608	083.20301.008F



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TBT PORT
Size: Custom | Document Number: TS1 | Rev: 1
Date: Thursday, November 03, 2016 | Sheet 102 of 103



Use NXP / ESD8011MUT5G Symbol

	EDA301~EDA303 ,EDA306~EDA311 EDA314~EDA316
1st	NXP PESD5V0H1BSF 083.5V0H1.00AF
2nd	N/A
3rd	N/A

	EDA304,EDA305,EDA312,EDA313
1st	RClamp2451ZA 083.02451.00A0
2nd	N/A
3rd	N/A

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **THUNDERBOLT CONNECTOR**

Size: Custom | Document Number: TS1 | Rev: 1

Date: Thursday, November 03, 2016 | Sheet 103 of 103