NSWAA/NTWAA

Liverpool 10

Sunderland 10

LA-5321P REV 1.0 Schematic

Intel Arrandale /IBEX PEAK

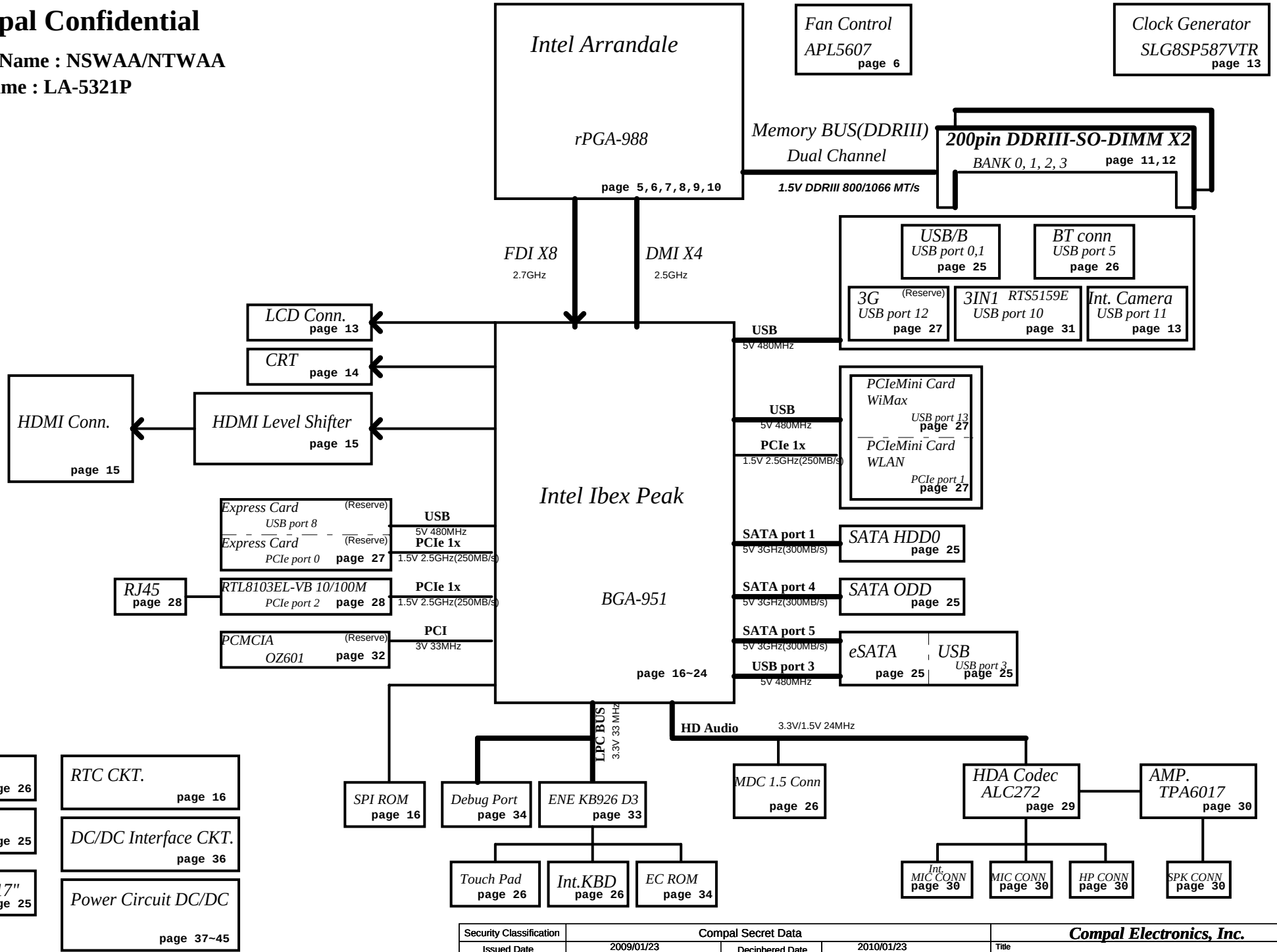
2009-11-12 Rev 1.0

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.		
Title: Schematic,LA5321P M/B		
Size: B	Document Number: 401782	Rev: D
Date: Monday, January 25, 2010	Sheet 1 of 48	

Compal Confidential

Model Name : NSWAA/NTWAA
File Name : LA-5321P



Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

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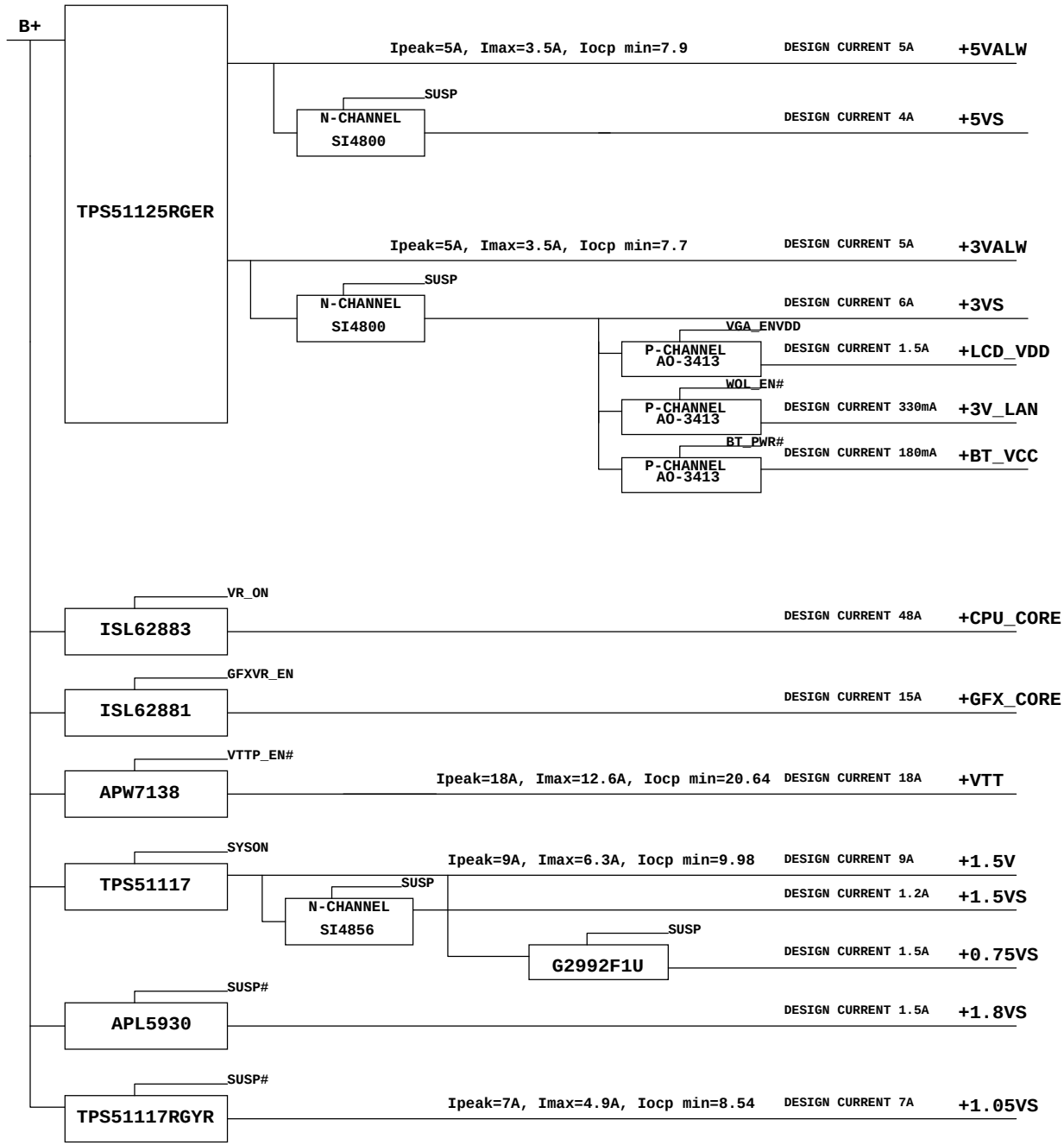
NSWAA Liverpool Intel Arrandale
NTWAA Sunderland Intel Arrandale



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Compal Electronics, Inc.

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	+B	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	0	0	0	0	0
S1	0	0	0	0	0
S3	0	0	0	0	X
S5 S4/AC	0	0	0	X	X
S5 S4/ Battery only	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X

BTO Option Table

Function	Bluetooth	RJ11	MIC	HDMI	Panel		3G	Express Card		Mini Card
description	(B)			(Y)			(G)	(E)	(A)	
explain	Bluetooth	MDC	MIC	HDMI	16"	17"	3G	New Card	PCMCIA	WIRELESS
BTO	BT@	MDC@	MIC@	IHDMI@	16@	17@	3G@	NEW@	PCM@	WLAN@

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

EC SM Bus1 address

Power	Device	Address
+3VALW	EC KB926 D3	
+3VALW	Smart Battery	0001 011x b

EC SM Bus2 address

Power	Device	Address
+3VS	EC KB926 D3	
+3VS	VGA THM Sensor ADM1032ARMZ	1001 110x b
+3VS	PCH	0100 110x b

PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMM0	1001 000x b
+3VS	DDR DIMM1	1001 010x b
+3VS	Express	
+3VS	WLAN/Wimax/3G	

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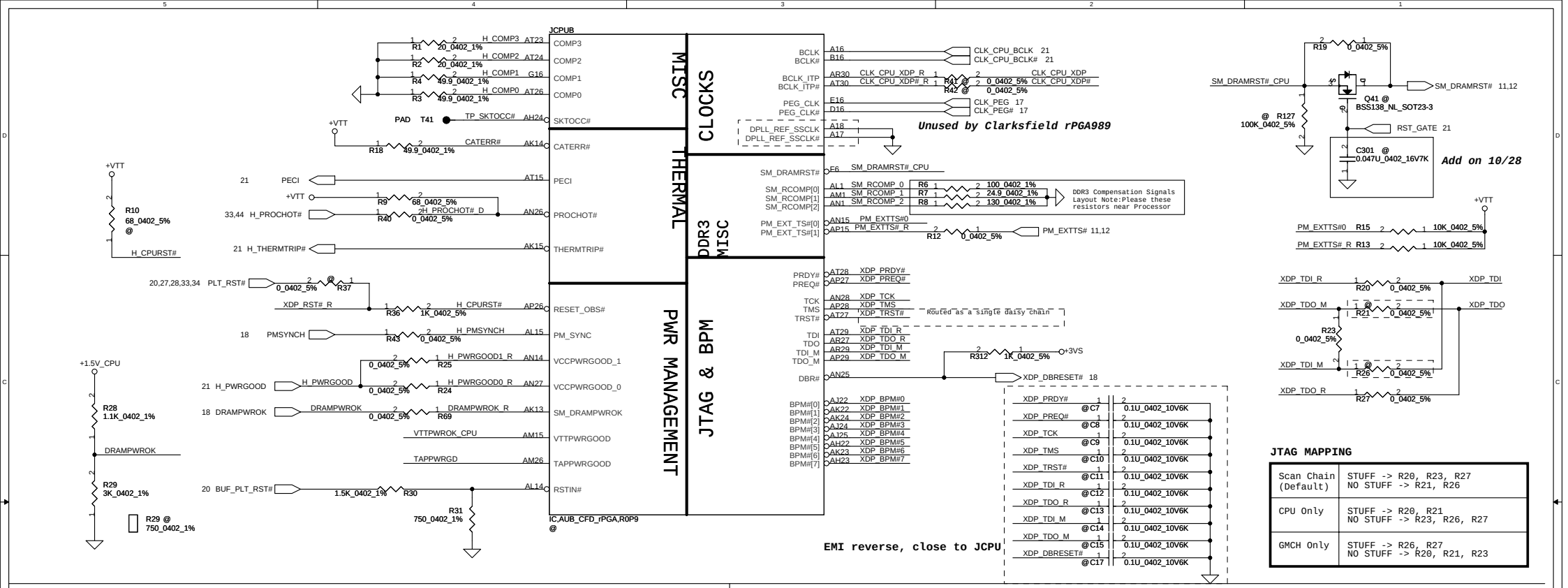

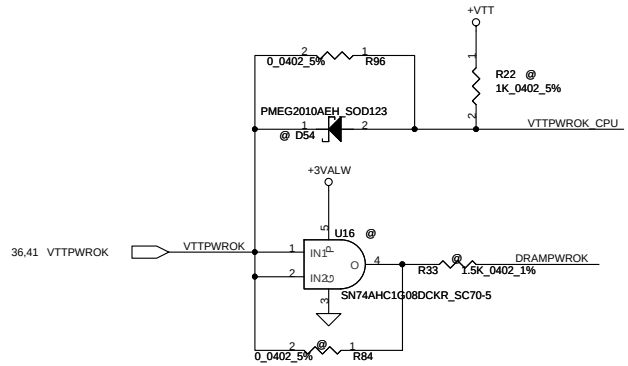

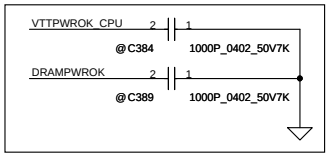

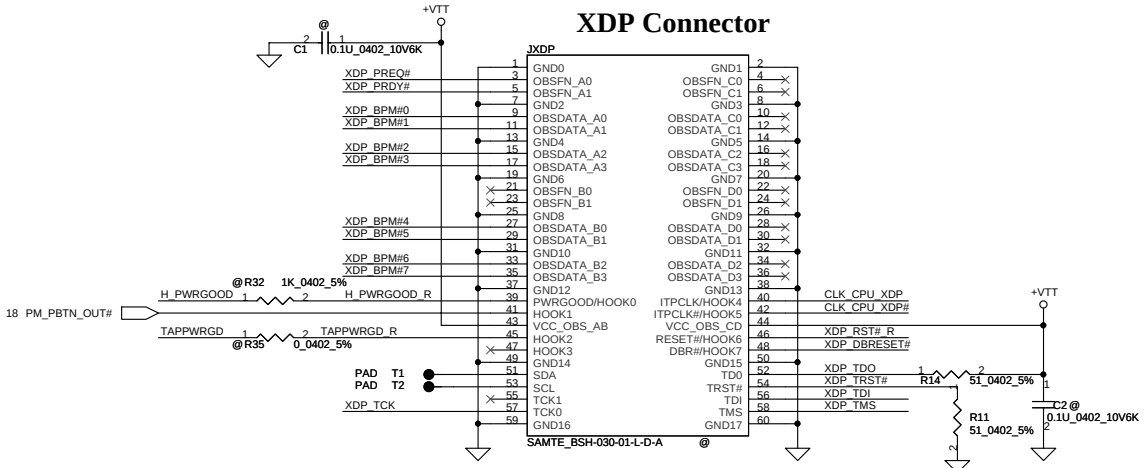

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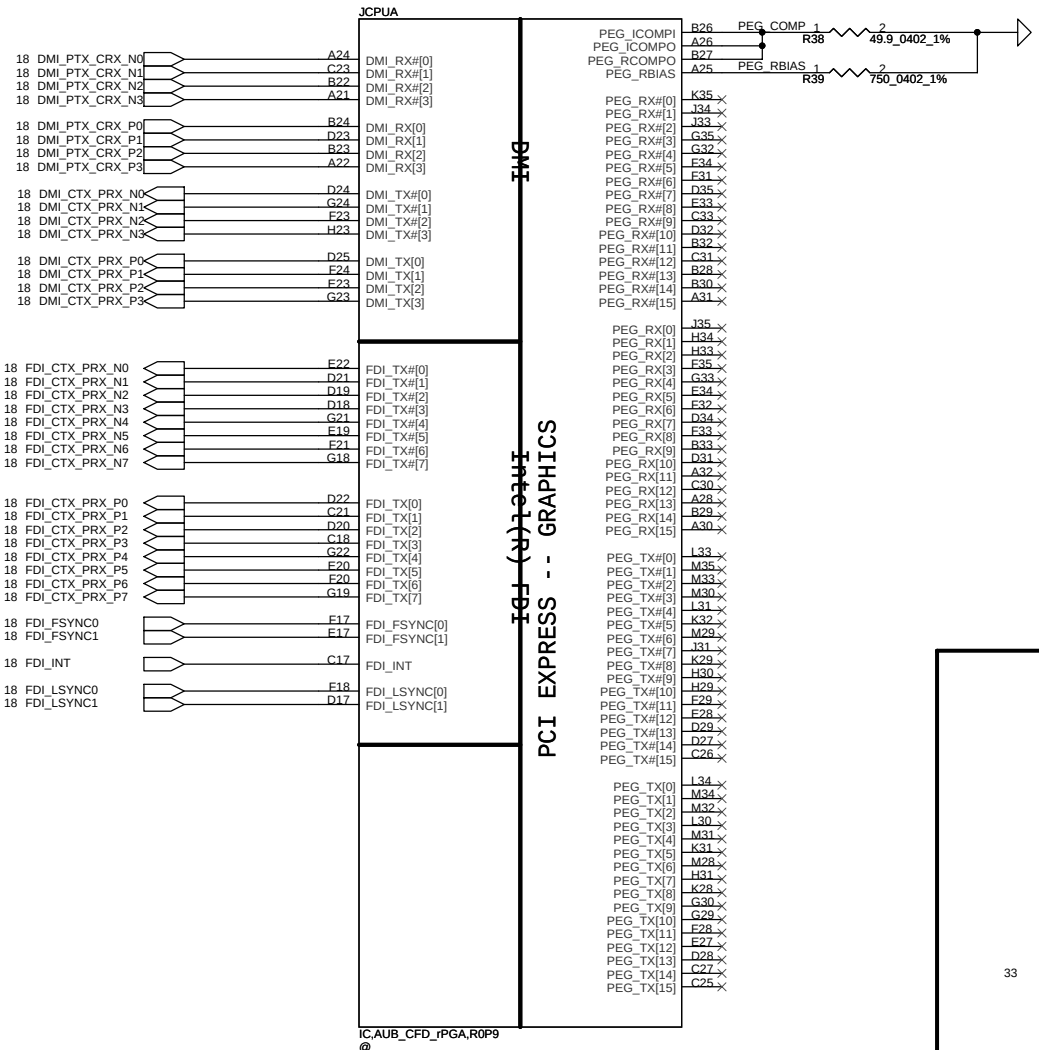

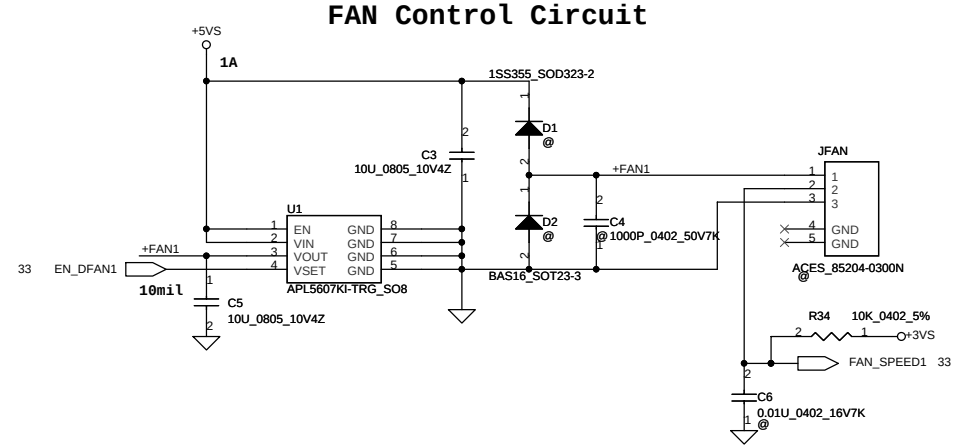

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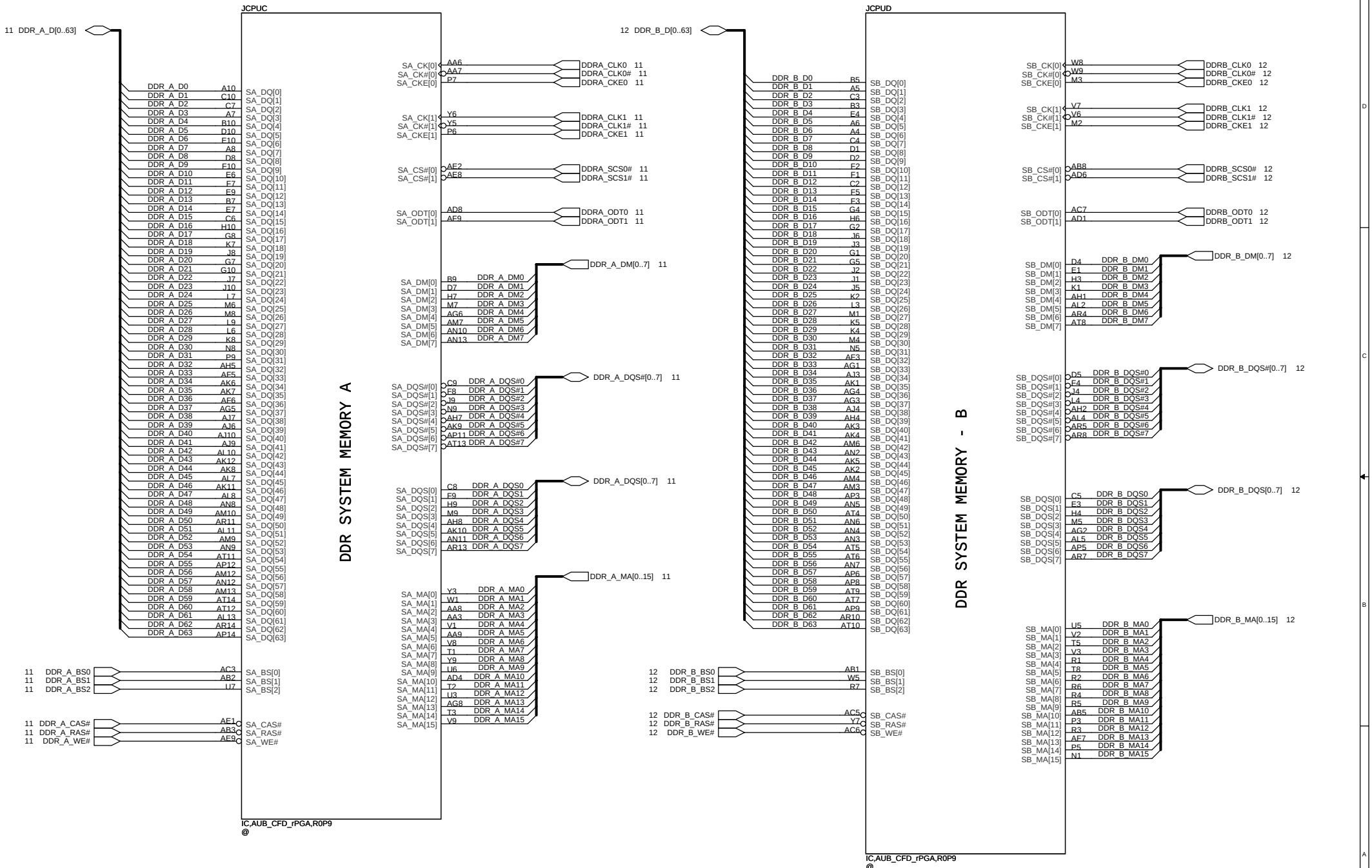

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Material Note (+VTT):
330uF/ 6mohm, number are 3,
power x1, HW x2

JCPUF

+CPU_CORE

Clarksfield: 65A
Auburndale:48A

Clarksfield: 21A
Auburndale:18A

1.1V RAIL POWER

CPU CORE SUPPLY

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44

+VTT

@ C80 330U_D2E_2.5VM_R6M
@ C82 330U_D2E_2.5VM_R6M
@ C84 330U_D2E_2.5VM_R6M
C89 22U_0805_6.3V6M
C91 22U_0805_6.3V6M

C81 C83 C85 C87 C88 C90 C92 10U_0805_10V4K
C94 10U_0805_10V4K@

(Place these capacitors under CPU socket Edge, top layer)

Co-layout with C80, C82

+VTT
C159 390U_2.5V_M_R10
C160 390U_2.5V_M_R10

Add on 5/25 for power team request

+CPU_CORE
22U_0805_6.3V6M
C158 @ C150 @ C148 C144 C131 C130 C132 C129 C149

POWER

CPU VIDS

PSI# AN33 H_PSI# 44

VID[0] AK35 CPU_VID0 44
VID[1] AK33 CPU_VID1 44
VID[2] AK34 CPU_VID2 44
VID[3] AL35 CPU_VID3 44
VID[4] AL33 CPU_VID4 44
VID[5] AM33 CPU_VID5 44
VID[6] AM35 CPU_VID6 44

PROC_DPRSLPVR AM34 H_DPRSLPVR_R R62 0_0402_5% H_DPRSLPVR 44

VTT_SELECT G15 H_VTTSELECT 41

CRB default setting:
VID[6:0]=[0100111]

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

H_VTTSELECT = low, 1.1V
H_VTTSELECT = high, 1.05V

SENSE LINES

ISENSE AN35 IMVP_IMON 44

VCC_SENSE AJ34 VCCSENSE_R R65 0_0402_5%
VSS_SENSE AJ35 VSSSENSE_R R66 0_0402_5%

R64 100_0402_1% +CPU_CORE
VCCSENSE
VSSSENSE
VCCSENSE 44
VSSSENSE 44
R67 100_0402_1%

VTT_SENSE B15 VTT_SENSE 41
VSS_SENSE_VTT A15 VSS_SENSE_VTT 41

near CPU

IC,AUB_CFD_rPGA,R0P9
@

(Place these capacitors between inductor and socket on Bottom)

+CPU_CORE
10U_0805_10V4K
C71 C72 C73 C74 C75 C76 C77 C78 C79

(Place these capacitors under CPU socket, top layer)

+CPU_CORE
10U_0805_10V4K
C98 C99 C100 C101 C102 C103 C104

(Place these capacitors on CPU cavity, Bottom Layer)

+CPU_CORE
22U_0805_6.3V6M
C105 C106 C107 C108 C109 C110
C111 C112 C113 C114 C115 C116

TOP side (under inductor)

+CPU_CORE
330U_D2_2.5VY_R9M
C121 C124 C122 C123

Co-layout with C124, C122

+CPU_CORE
C271 560U_2.5V_M @ C180 560U_2.5V_M @ C179 560U_2.5V_M @

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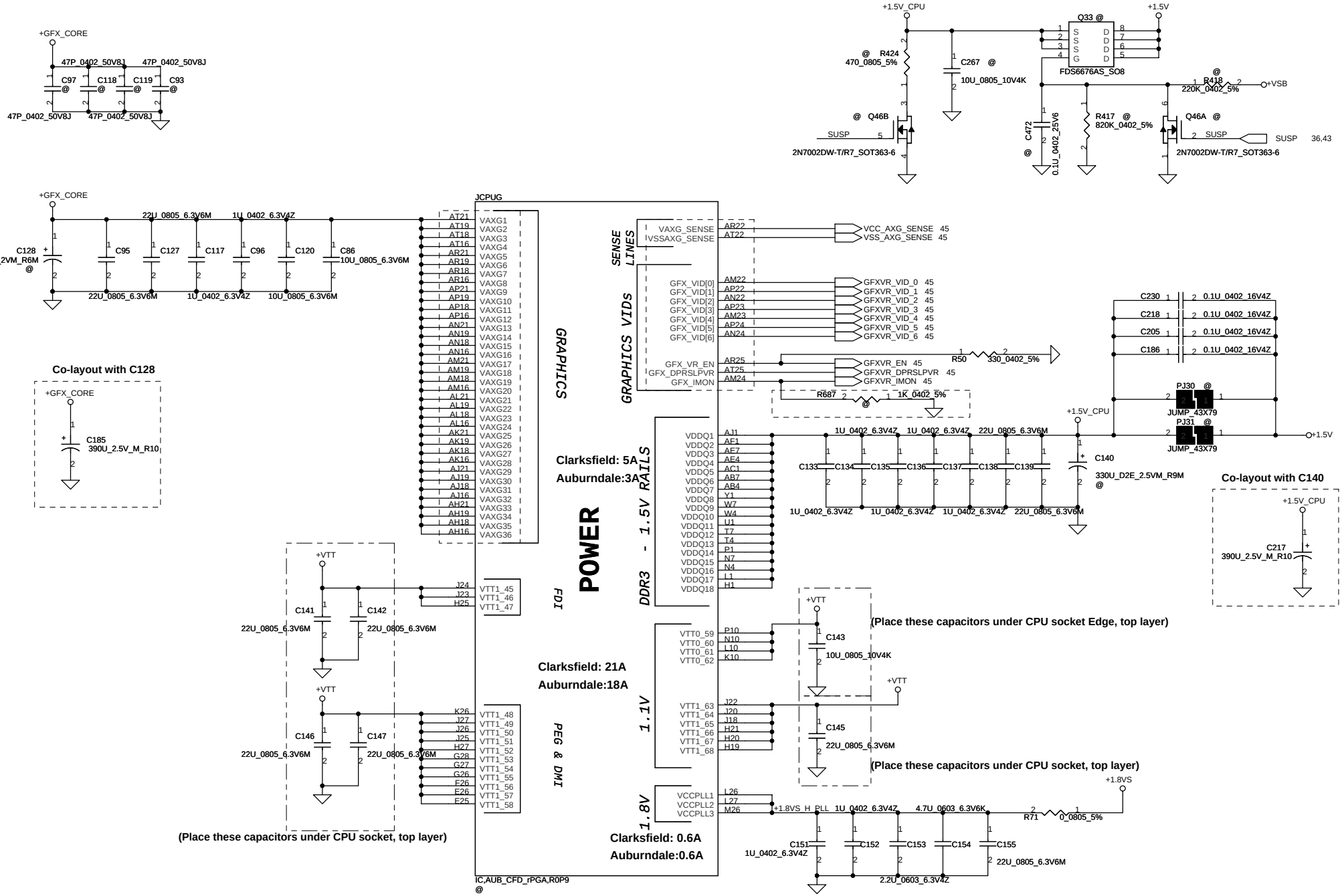

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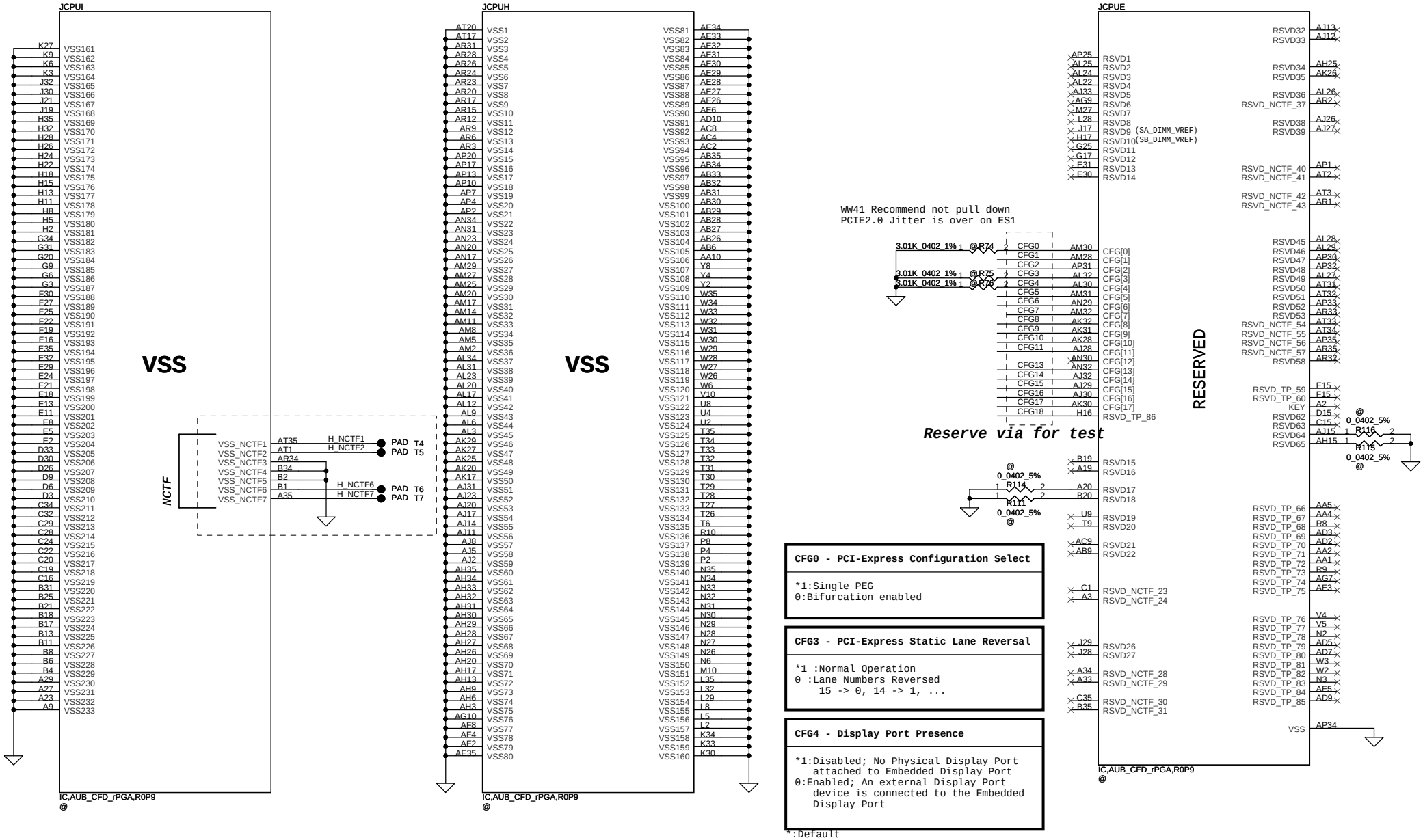

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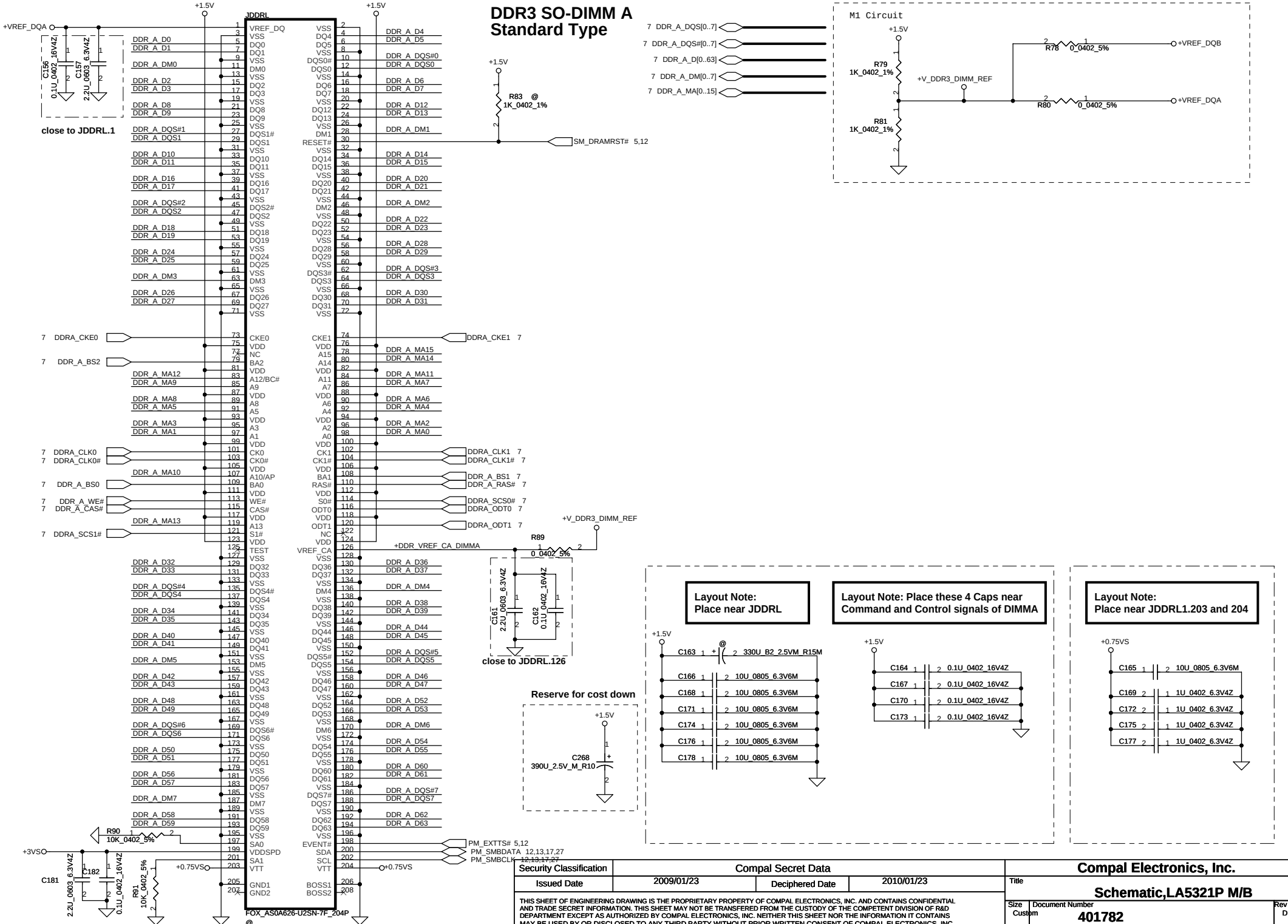
DDR3 SO-DIMM A
Standard Type



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Standard Type
DDR3 SO-DIMM B

7 DDR_B_DQS#[0..7]
7 DDR_B_DQS[0..7]
7 DDR_B_D[0..63]
7 DDR_B_DM[0..7]
7 DDR_B_MA[0..15]

JDDRH

+VREF_DQB	1	VREF_DQ	VSS	2	
DDR_B_D0	3	VSS	DQ4	4	DDR_B_D4
DDR_B_D1	5	DQ0	DQ5	6	DDR_B_D5
	7	DQ1	VSS	8	
DDR_B_DM0	9	VSS	DQS0#	10	DDR_B_DQS#0
	11	DM0	DQS0	12	DDR_B_DQS0
DDR_B_D2	13	VSS	VSS	14	
DDR_B_D3	15	DQ2	DQ6	16	DDR_B_D6
	17	DQ3	DQ7	18	DDR_B_D7
DDR_B_D8	19	VSS	VSS	20	
DDR_B_D9	21	DQ8	DQ12	22	DDR_B_D12
	23	DQ9	DQ13	24	DDR_B_D13
DDR_B_DQS#1	25	VSS	VSS	26	
DDR_B_DQS1	27	DQS1#	DM1	28	DDR_B_DM1
	29	DQS1	RESET#	30	SM_DRAMRST# 5,11
DDR_B_D10	31	VSS	VSS	32	
DDR_B_D11	33	DQ10	DQ14	34	DDR_B_D14
	35	DQ11	DQ15	36	DDR_B_D15
DDR_B_D16	37	VSS	VSS	38	
DDR_B_D17	39	DQ16	DQ20	40	DDR_B_D20
	41	DQ17	DQ21	42	DDR_B_D21
DDR_B_DQS#2	43	VSS	VSS	44	
DDR_B_DQS2	45	DQS2#	DM2	46	DDR_B_DM2
	47	DQS2	VSS	48	
DDR_B_D18	49	VSS	DQ22	50	DDR_B_D22
DDR_B_D19	51	DQ18	DQ23	52	DDR_B_D23
	53	DQ19	VSS	54	
DDR_B_D24	55	VSS	DQ28	56	DDR_B_D28
DDR_B_D25	57	DQ24	DQ29	58	DDR_B_D29
	59	DQ25	VSS	60	
DDR_B_DM3	61	VSS	DQS3#	62	DDR_B_DQS#3
	63	DM3	DQS3	64	DDR_B_DQS3
DDR_B_D26	65	VSS	VSS	66	
DDR_B_D27	67	DQ26	DQ30	68	DDR_B_D30
	69	DQ27	DQ31	70	DDR_B_D31
	71	VSS	VSS	72	
7 DDRB_CKE0	73	CKE0	CKE1	74	DDRB_CKE1 7
	75	VDD	VDD	76	
	77	NC	A15	78	DDR_B_MA15
7 DDR_B_BS2	79	BA2	A14	80	DDR_B_MA14
	81	VDD	VDD	82	
DDR_B_MA12	83	A12/BC#	A11	84	DDR_B_MA11
DDR_B_MA9	85	A9	A7	86	DDR_B_MA7
	87	VDD	VDD	88	
DDR_B_MA8	89	A8	A6	90	DDR_B_MA6
DDR_B_MA5	91	A5	A4	92	DDR_B_MA4
	93	VDD	VDD	94	
DDR_B_MA3	95	A3	A2	96	DDR_B_MA2
DDR_B_MA1	97	A1	A0	98	DDR_B_MA0
	99	VDD	VDD	100	
7 DDRB_CLK0	101	CK0	CK1	102	DDRB_CLK1 7
7 DDRB_CLK0#	103	CK0#	CK1#	104	DDRB_CLK1# 7
	105	VDD	VDD	106	
DDR_B_MA10	107	A10/AP	BA1	108	DDR_B_BS1 7
7 DDR_B_BS0	109	BA0	RAS#	110	DDR_B_RAS# 7
	111	VDD	VDD	112	
7 DDR_B_WE#	113	WE#	S0#	114	DDRB_SCS0# 7
7 DDR_B_CAS#	115	CAS#	ODT0	116	DDRB_ODT0 7
	117	VDD	VDD	118	
DDR_B_MA13	119	A13	ODT1	120	DDRB_ODT1 7
7 DDRB_SCS1#	121	S1#	NC	122	
	123	VDD	VDD	124	
	125	TEST	VREF_CA	126	+DDR_VREF_CA_DIMMB
	127	VSS	VSS	128	
DDR_B_D32	129	DQ32	DQ36	130	DDR_B_D36
DDR_B_D33	131	DQ33	DQ37	132	DDR_B_D37
	133	VSS	VSS	134	
DDR_B_DQS#4	135	DQS4#	DM4	136	DDR_B_DM4
DDR_B_DQS4	137	DQS4	VSS	138	
	139	VSS	DQ38	140	DDR_B_D38
DDR_B_D34	141	DQ34	DQ39	142	DDR_B_D39
DDR_B_D35	143	DQ35	VSS	144	
	145	VSS	DQ44	146	DDR_B_D44
DDR_B_D40	147	DQ40	DQ45	148	DDR_B_D45
DDR_B_D41	149	DQ41	VSS	150	
	151	VSS	DQS5#	152	DDR_B_DQS#5
DDR_B_DM5	153	DM5	DQS5	154	DDR_B_DQS5
	155	VSS	VSS	156	
DDR_B_D42	157	DQ42	DQ46	158	DDR_B_D46
DDR_B_D43	159	DQ43	DQ47	160	DDR_B_D47
	161	VSS	VSS	162	
DDR_B_D48	163	DQ48	DQ52	164	DDR_B_D52
DDR_B_D49	165	DQ49	DQ53	166	DDR_B_D53
	167	VSS	VSS	168	
DDR_B_DQS#6	169	DQS6#	DM6	170	DDR_B_DM6
DDR_B_DQS6	171	DQS6	VSS	172	
	173	VSS	DQ54	174	DDR_B_D54
DDR_B_D50	175	DQ50	DQ55	176	DDR_B_D55
DDR_B_D51	177	DQ51	VSS	178	
	179	VSS	DQ60	180	DDR_B_D60
DDR_B_D56	181	DQ56	DQ61	182	DDR_B_D61
DDR_B_D57	183	DQ57	VSS	184	
	185	VSS	DQS7#	186	DDR_B_DQS#7
DDR_B_DM7	187	DM7	DQS7	188	DDR_B_DQS7
	189	VSS	VSS	190	
DDR_B_D58	191	DQ58	DQ62	192	DDR_B_D62
DDR_B_D59	193	DQ59	DQ63	194	DDR_B_D63
	195	VSS	VSS	196	
	197	SA0	EVENT#	198	PM_EXTTS# 5,11
	199	VDDSPD	SDA	200	PM_SMBDATA 11,13,17,27
	201	SA1	SCL	202	PM_SMBCLK 11,13,17,27
	203	VTT	VTT	204	+0.75VS
	205	GND1	BOSS1	206	
	207	GND2	BOSS2	208	

FOX_AS0A626-UASN-7F_204P
@

+1.5V
+1.5V
+3VS
+0.75VS
+V_DDR3_DIMM_REF

C183 2.2U_0603_6.3V4Z
C184 0.1U_0402_16V4Z
close to JDDRH.1

C187 2.2U_0603_6.3V4Z
C188 0.1U_0402_16V4Z
close to JDDRH.126

R97 1 2 0_0402_5%
R98 1 2 10K_0402_5%
R99 1 2 10K_0402_5%

2.2U_0603_6.3V4Z C207
0.1U_0402_16V4Z C208

Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

C189 330U_B2_2.5VM_R15M
C192 10U_0805_6.3V6M
C194 10U_0805_6.3V6M
C197 10U_0805_6.3V6M
C200 10U_0805_6.3V6M
C202 10U_0805_6.3V6M
C204 10U_0805_6.3V6M

C190 0.1U_0402_16V4Z
C193 0.1U_0402_16V4Z
C196 0.1U_0402_16V4Z
C199 0.1U_0402_16V4Z

Layout Note:
Place near JDDRH.203 and 204

C191 10U_0805_6.3V6M
C195 1U_0402_6.3V4Z
C198 1U_0402_6.3V4Z
C201 1U_0402_6.3V4Z
C203 1U_0402_6.3V4Z

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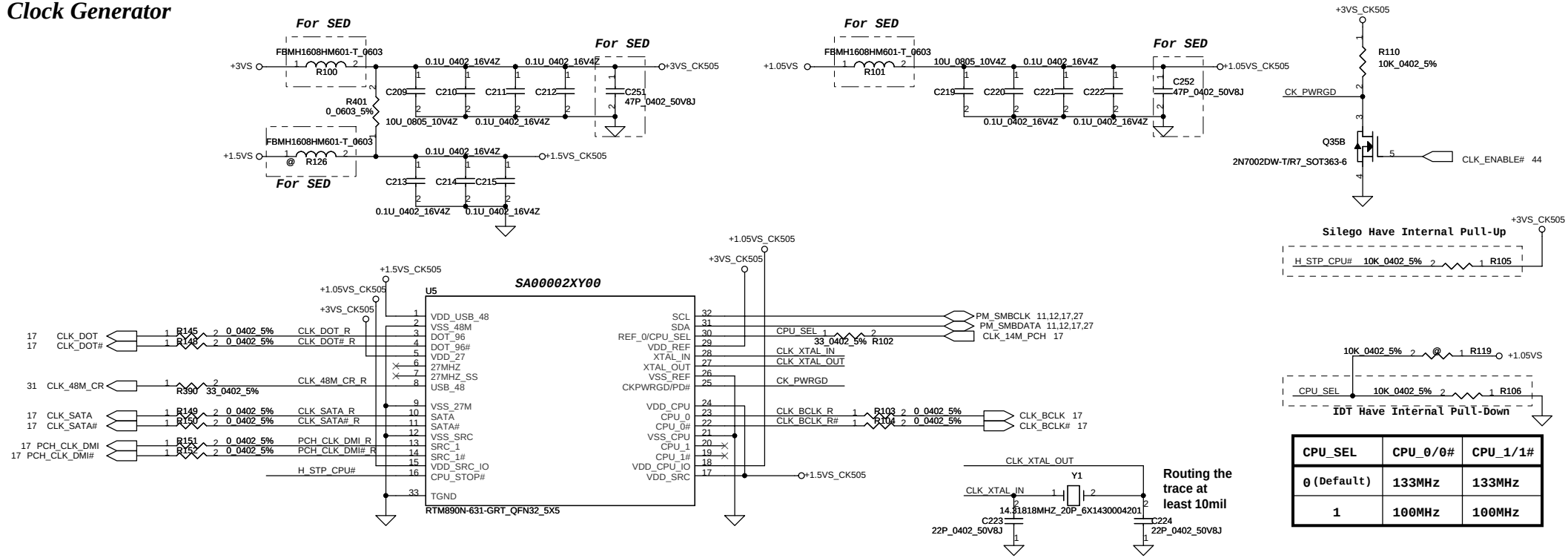
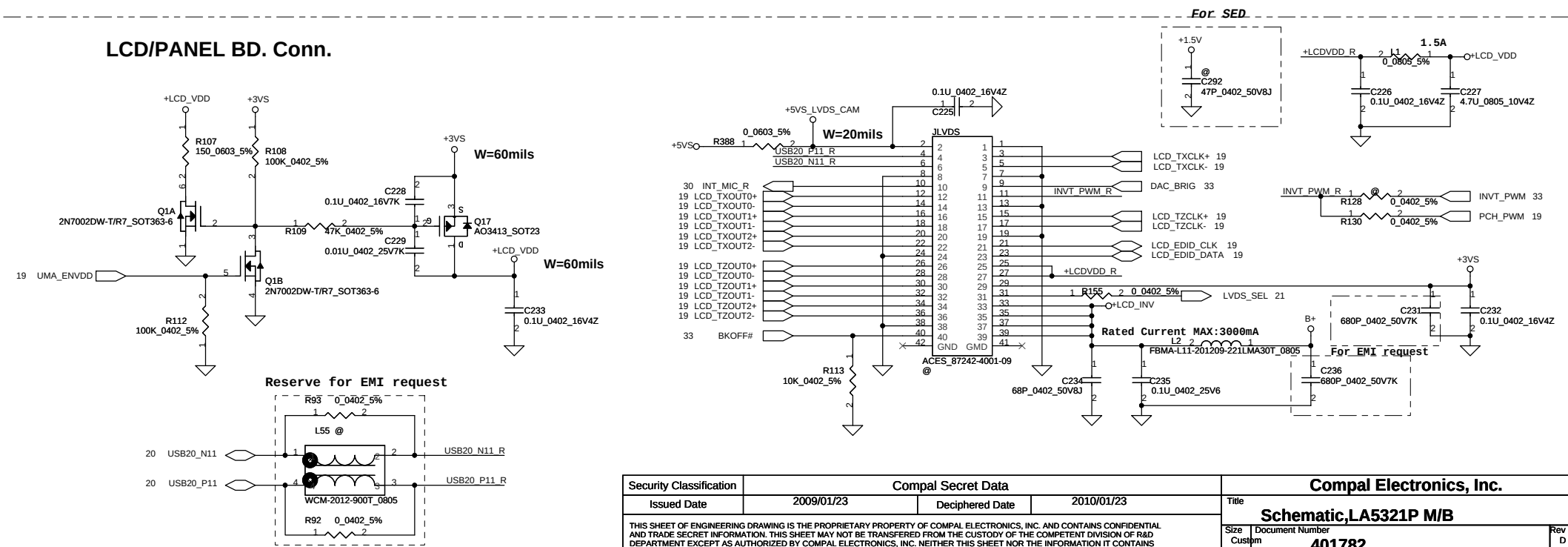
Clock Generator



CPU_SEL	CPU_0/0#	CPU_1/1#
0(Default)	133MHz	133MHz
1	100MHz	100MHz

LCD/PANEL BD. Conn.



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Compal Electronics, Inc.

Title: **Schematic,LA5321P M/B**

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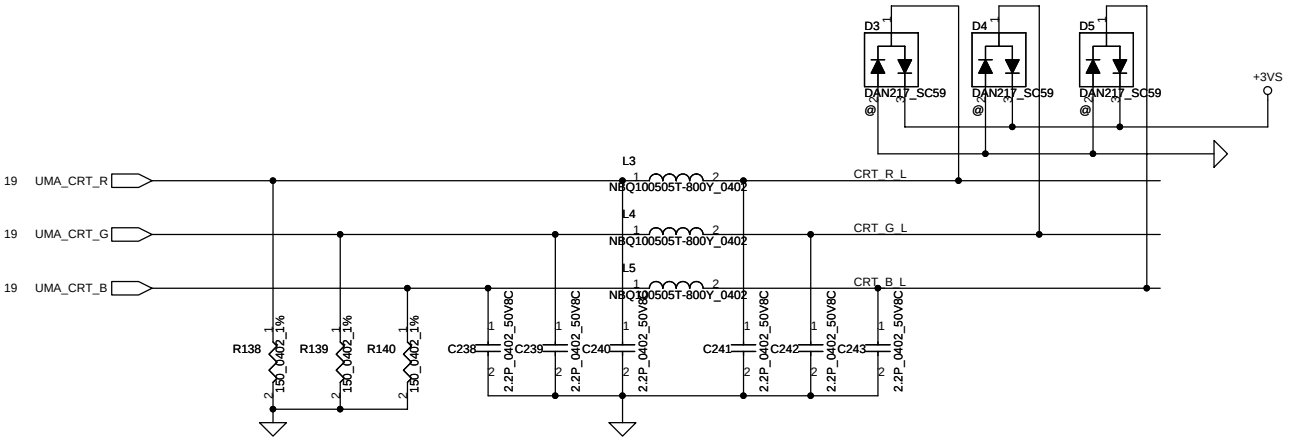
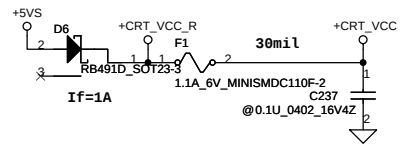
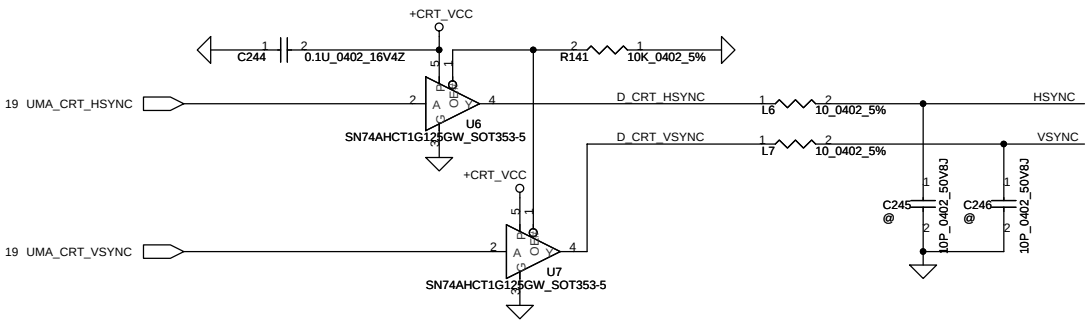
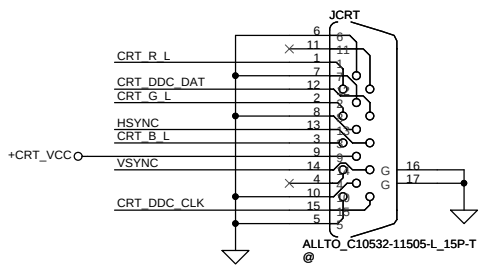
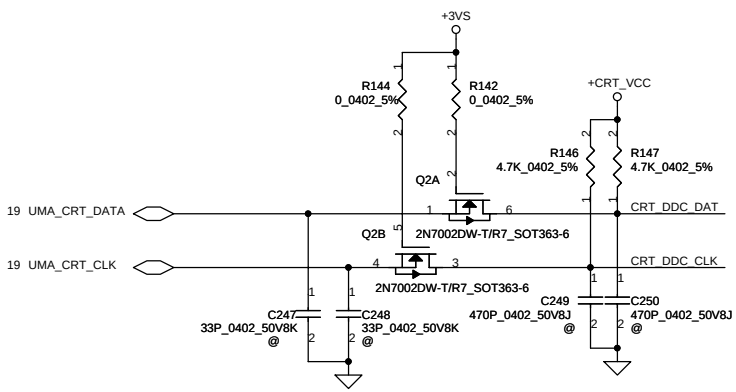
CRT CONNECTOR











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Compal Electronics, Inc.

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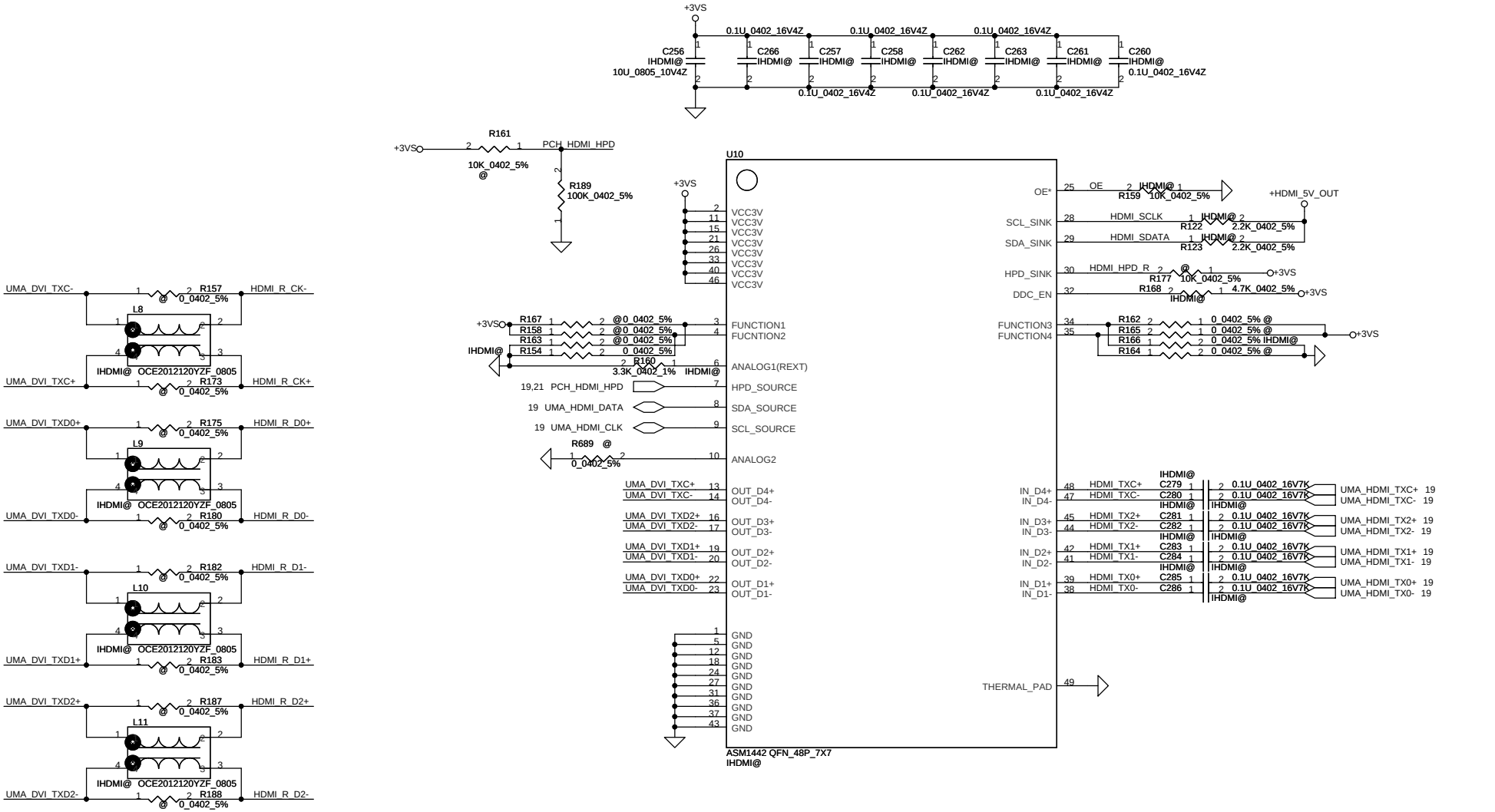
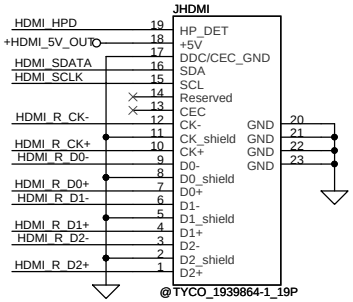
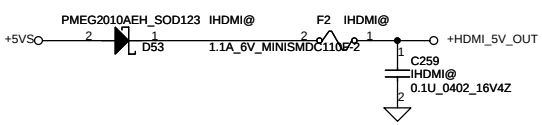
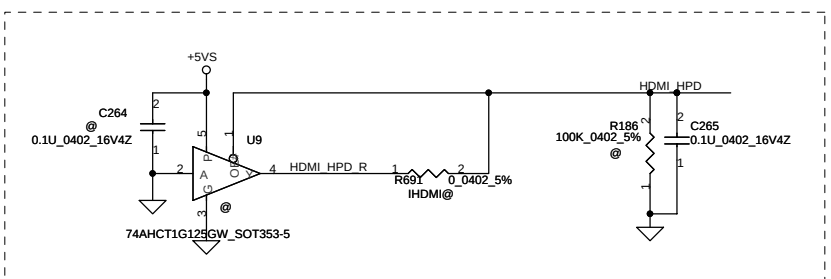


HDMI Connector







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CMOS Setting, near DDR Door

+RTCVCC — R282 20K_0402_1% — PCH_RTCRST# — JCMOS — C288 1U_0402_6.3V4Z

iME Setting.

R284 20K_0402_1% — PCH_SRTCRST# — J2 — C289 1U_0402_6.3V4Z

C287 15P_0402_50V8J — Y3 (NC, OSC, NC, OSC) — 32.768KHZ_12.5PF_Q13MC14610002 — R283 10M_0402_5% — C290 15P_0402_50V8J

Integrated SUS 1.05V VRM Enable	
PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)

HDA_SYNC
This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
*L=>On Die PLL is supplied by 1.8V

HDA_SDO
This signal has a weak internal pull down.
This signal can't PU

Flash Descriptor Security Overide	
HDA_DOCK_EN#	Low = Enabled High = Disabled *

ITPM Enabled	Internal: Pull down 20k
SPI_MOSI	High = Enabled Low = Disabled (Default)

U11A

RTC: PCH_RTCX1 B13 RTCX1; PCH_RTCX2 D13 RTCX2; PCH_RTCRST# C14 RTCRST#; PCH_SRTCRST# D17 SRTCRST#; SM_INTRUDER# A16 INTRUDER#; PCH_INTVRMEN A14 INTVRMEN

LPC: FWH0 / LAD0 D33 — LPC_AD0 33,34; FWH1 / LAD1 B33 — LPC_AD1 33,34; FWH2 / LAD2 C32 — LPC_AD2 33,34; FWH3 / LAD3 A32 — LPC_AD3 33,34; FWH4 / LFRAME# C34 — LPC_FRAME# 33,34; LDRQ0# A34; LDRQ1# / GPIO23 F34; SERIRQ AB9 — SERIRQ 32,33,34

IHDA: AZ_BITCLK A30 HDA_BCLK; AZ_SYNC D29 HDA_SYNC; 19,29 PCH_SPKR P1 SPKR; AZ_RST# C30 HDA_RST#; 29 AZ_SDIN0_HD G30 HDA_SDIN0; 26 AZ_SDIN1_MD F30 HDA_SDIN1; F32 HDA_SDIN2; F32 HDA_SDIN3; AZ_SDOUT B29 HDA_SDO

SATA: 33 PWRME_CTRL H32 HDA_DOCK_EN# / GPIO33; J30 HDA_DOCK_RST# / GPIO13

SATA0RXN AK7; SATA0RXP AK6; SATA0TXN AK11; SATA0TXP AK9

SATA1RXN AH6 — SATA_PRX_C_DTX_N1 25; SATA1RXP AH5 — SATA_PRX_C_DTX_P1 25; SATA1TXN AH9 — SATA_PTX_DRX_N1 25; SATA1TXP AH8 — SATA_PTX_DRX_P1 25 — **1ST HDD**

Desktop Only

SATA2RXN AE11; SATA2RXP AE9; SATA2TXN AE7; SATA2TXP AE6

SATA3RXN AH3; SATA3RXP AH1; SATA3TXN AF3; SATA3TXP AF1

SATA4RXN AD9; SATA4RXP AD8; SATA4TXN AD6; SATA4TXP AD5 — SATA_PRX_C_DTX_N4 25; SATA_PRX_C_DTX_P4 25; SATA_PTX_DRX_N4 25; SATA_PTX_DRX_P4 25 — **SATA ODD**

SATA5RXN AD3; SATA5RXP AD1; SATA5TXN AB3; SATA5TXP AB1 — SATA_PRX_C_DTX_N5 25; SATA_PRX_C_DTX_P5 25; SATA_PTX_DRX_N5 25; SATA_PTX_DRX_P5 25 — **eSATA**

SATAICOMPO AF16; SATAICOMPI AF15 — SATAICOMP R295 37.4_0402_1% +1.05VS

JTAG: PCH_JTAG_TCK M3 JTAG_TCK; PCH_JTAG_TMS K3 JTAG_TMS; PCH_JTAG_TDI K1 JTAG_TDI; PCH_JTAG_TDO J2 JTAG_TDO; PCH_JTAG_RST# J4 TRST#

SPI: PCH_SPI_CLK BA2 SPI_CLK; PCH_SPI_CS0# AV3 SPI_CS0#; AY3 SPI_CS1#; PCH_SPI_MOSI AY1 SPI_MOSI; PCH_SPI_MISO AV1 SPI_MISO

SATALED# T3 — SATA_LED# — SATA_LED# 35

SATA0GP / GPIO21 Y9 — SPK_SEL — SPK_SEL 29

SATA1GP / GPIO19 V1 — PCH_GPIO19

IBEXPEAK-M QV20 A0_FCBGA1071
HM55R3@

+3VS — R273 1K_0402_5% — PCH_SPI_MOSI

+RTCVCC — R285 1M_0402_5% — SM_INTRUDER#; R275 330K_0402_5% — PCH_INTVRMEN

R286 10K_0402_5% — +3VS — SERIRQ

R118 1K_0402_5% @ — PWRME_CTRL

26 AZ_BITCLK_MD / 29 AZ_BITCLK_HD — R287 MDC@ 33_0402_5%, R288 33_0402_5% — AZ_BITCLK

26 AZ_SYNC_MD / 29 AZ_SYNC_HD — R289 MDC@ 33_0402_5%, R290 33_0402_5% — AZ_SYNC

26 AZ_RST_MD# / 29 AZ_RST_HD# — R291 MDC@ 33_0402_5%, R292 33_0402_5% — AZ_RST#

26 AZ_SDOUT_MD / 29 AZ_SDOUT_HD — R293 MDC@ 33_0402_5%, R294 33_0402_5% — AZ_SDOUT

+3VS — PCH_GPIO19 R306 10K_0402_5%; SATA_LED# R301 10K_0402_5%; SPK_SEL R303 10K_0402_5%

+3VALW — @ R386 200_0402_5% — PCH_JTAG_TMS — @ R355 100_0402_5%

+3VALW — @ R363 200_0402_5% — PCH_JTAG_TDO — @ R535 100_0402_5%

+3VALW — @ R536 200_0402_5% — PCH_JTAG_TDI — @ R537 100_0402_5%

+3VALW — @ R643 20K_0402_5% — PCH_JTAG_RST# — @ R364 10K_0402_5%

R156 51_0402_5% — PCH_JTAG_TCK

06/01 change R125 from 4.7K to 51 ohm

PCH Pin	RefDes	PCH JTAG Enable ES1	PCH JTAG Enable ES2	PCH JTAG Disable (Default) ES1	PCH JTAG Disable (Default) ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
	R535	No Install	100ohm	No Install	No Install
PCH_JTAG_TMS	R355	200ohm	200ohm	No Install	No Install
	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R536	200ohm	200ohm	20Kohm	No Install
	R537	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
	R353	10Kohm	10Kohm	No Install	No Install

4MB

+3VS — C293 0.1U_0402_16V4Z — U13 MX25L3205DM2I-12G SO8

PCH_SPI_CS0# — PCH_SPI_CLK — PCH_SPI_MOSI — PCH_SPI_MISO

for EMI request

PCH_SPI_CLK — R385 10_0402_5% — C16 33P_0402_50V8J

+RTCBATT — D13 BAS40-04_SOT23-3 — +CHGRTC — +RTCVCC — C291 0.1U_0402_16V4Z

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Compal Electronics, Inc.

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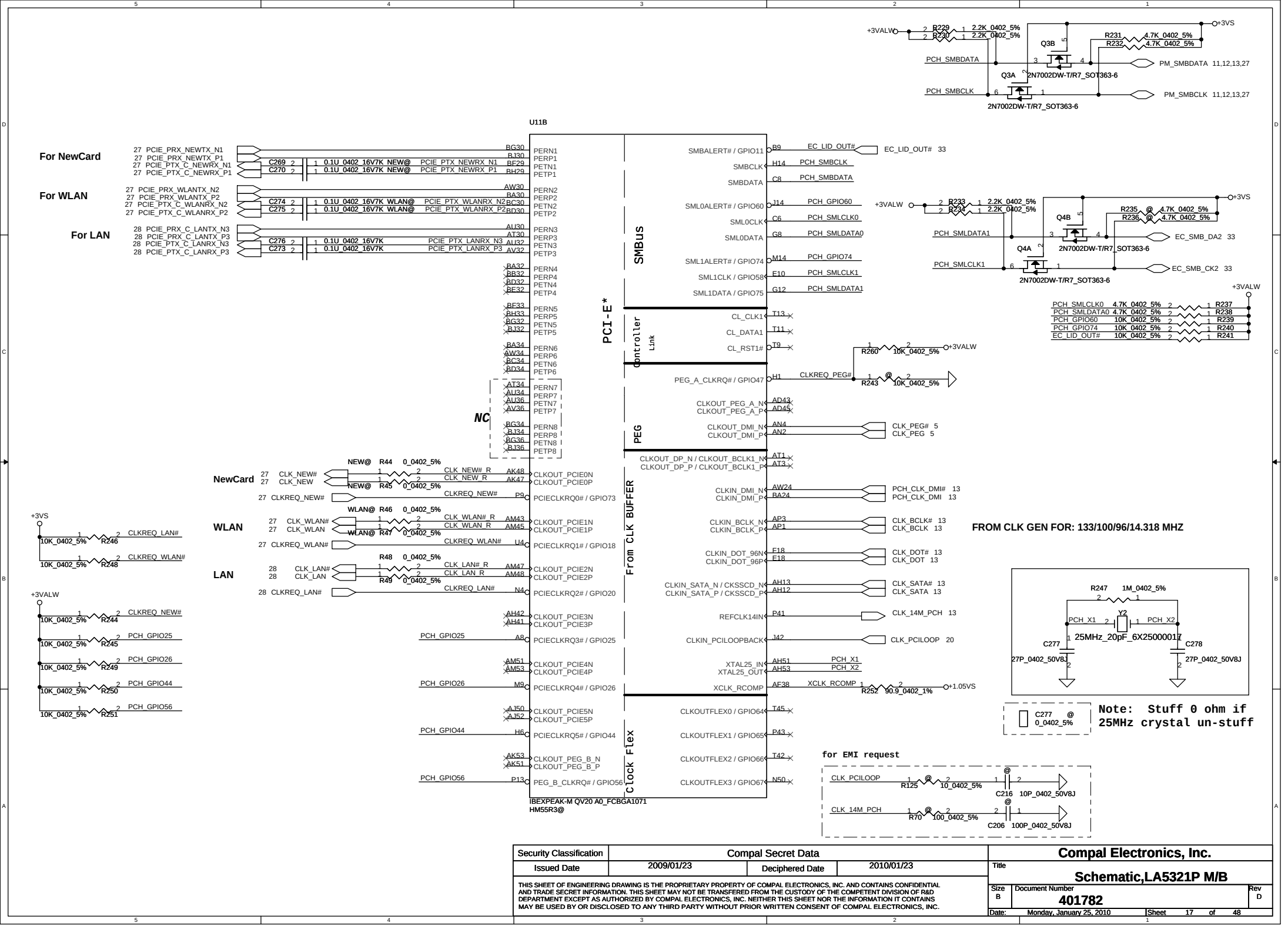

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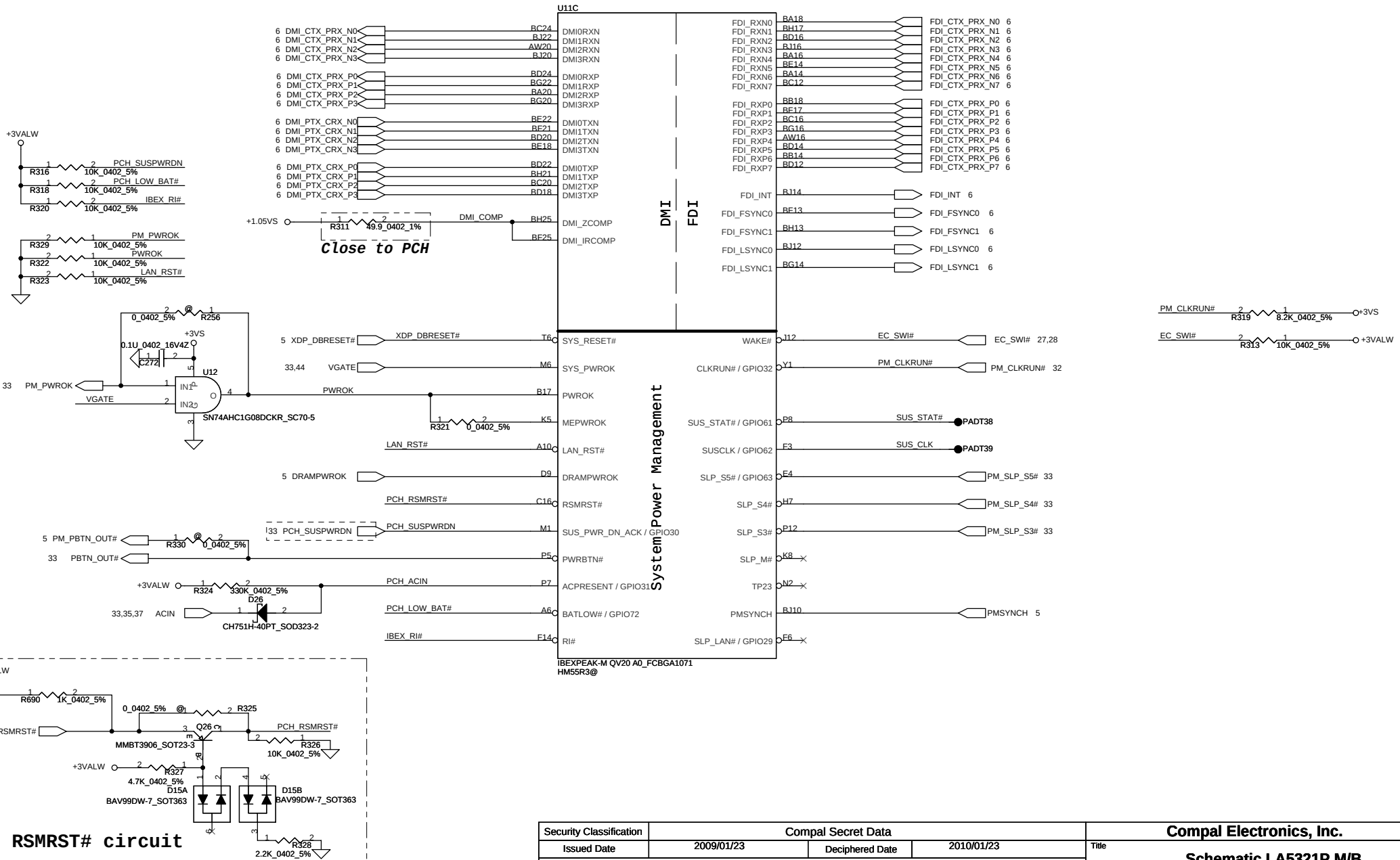

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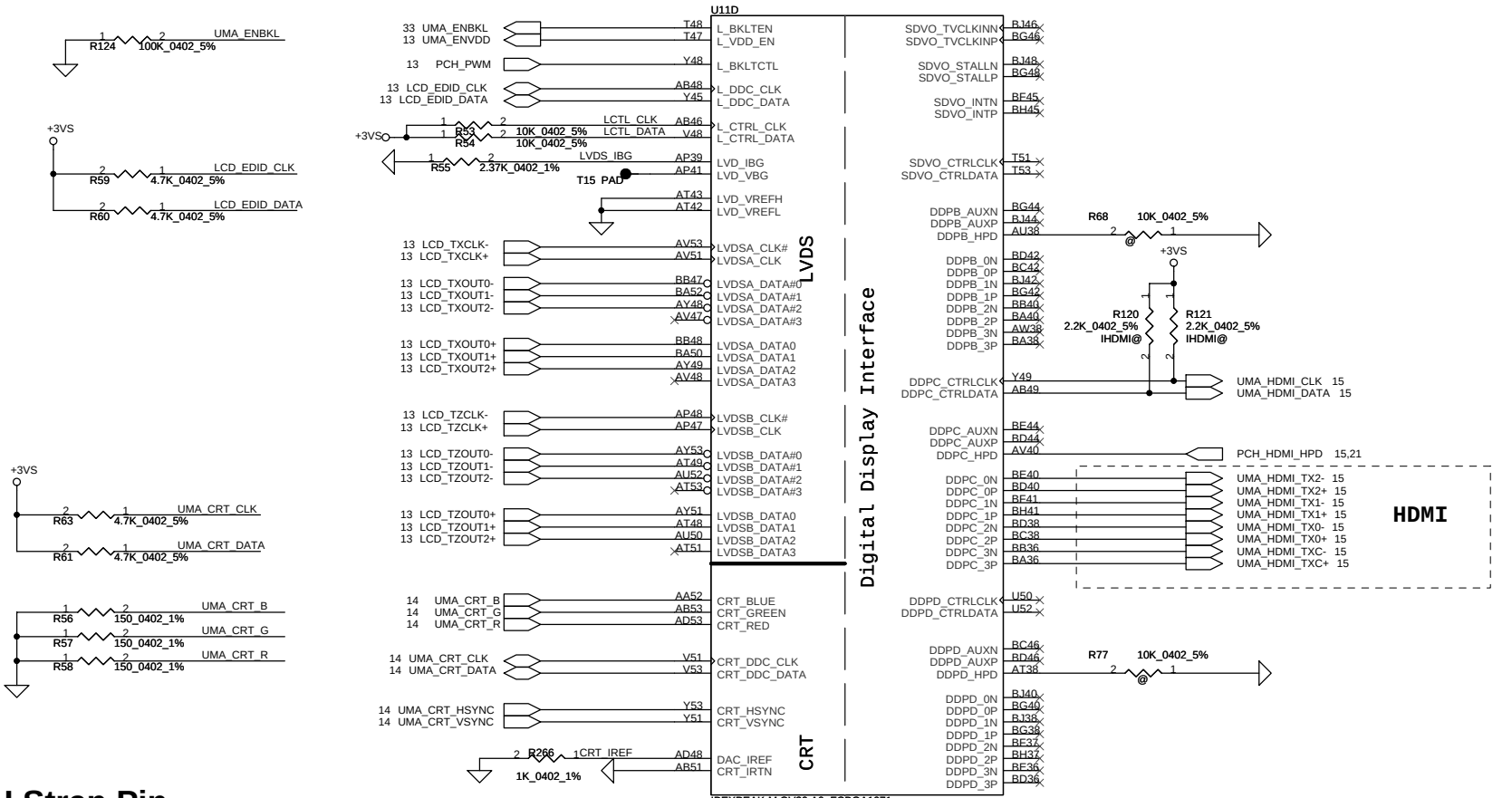
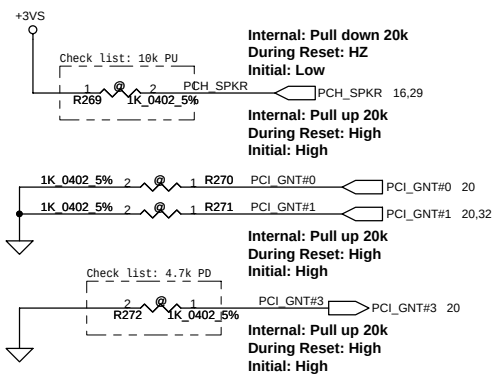


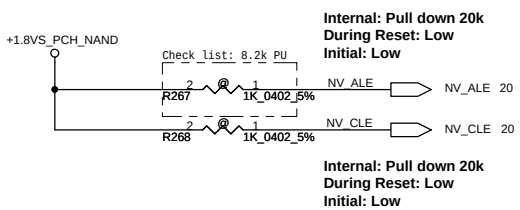
PCH Strap Pin



NO REBOOT Strap	
PCH_SPKR	Low= Disable High= Enable

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Loaction
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable



Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

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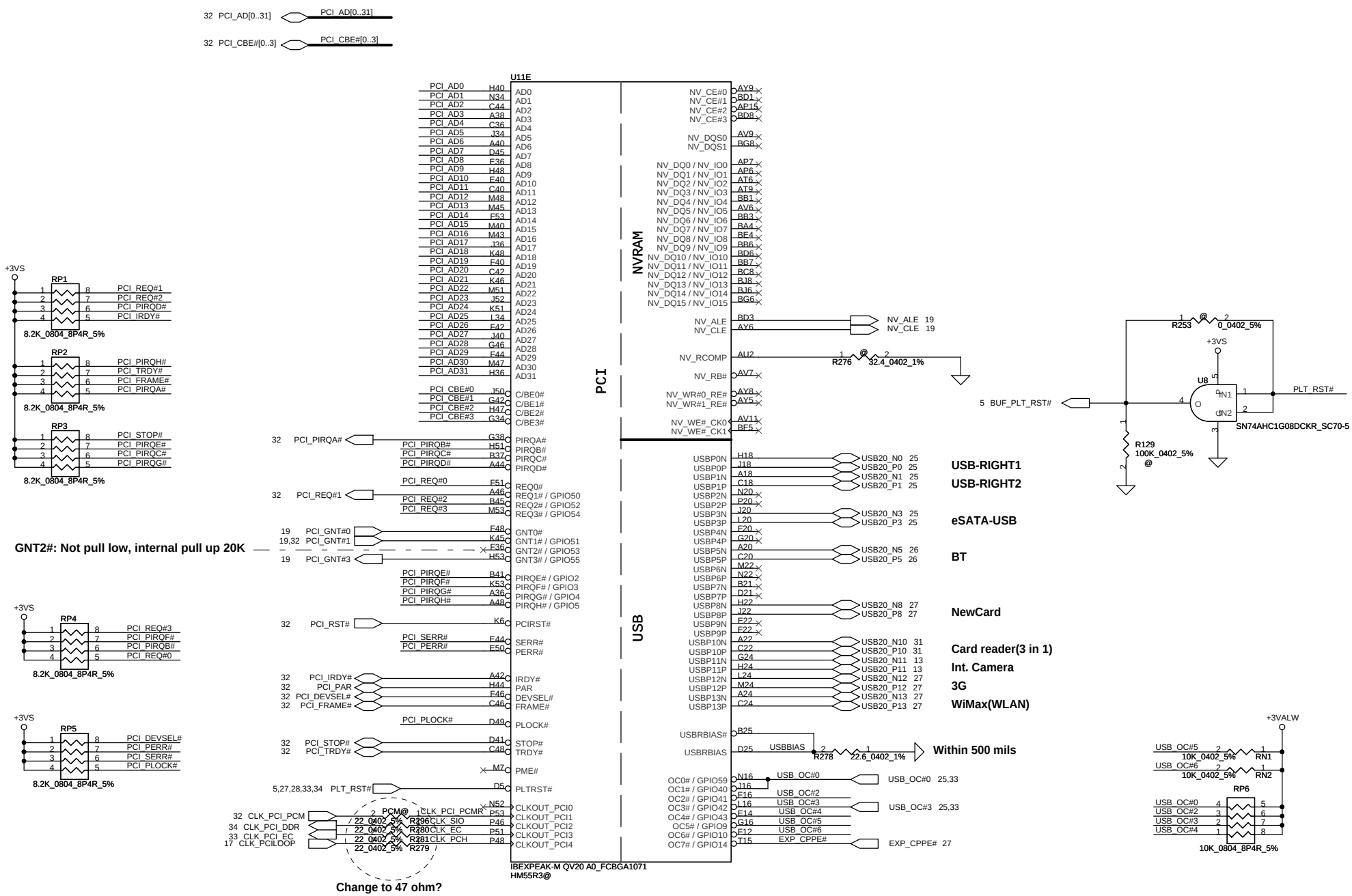

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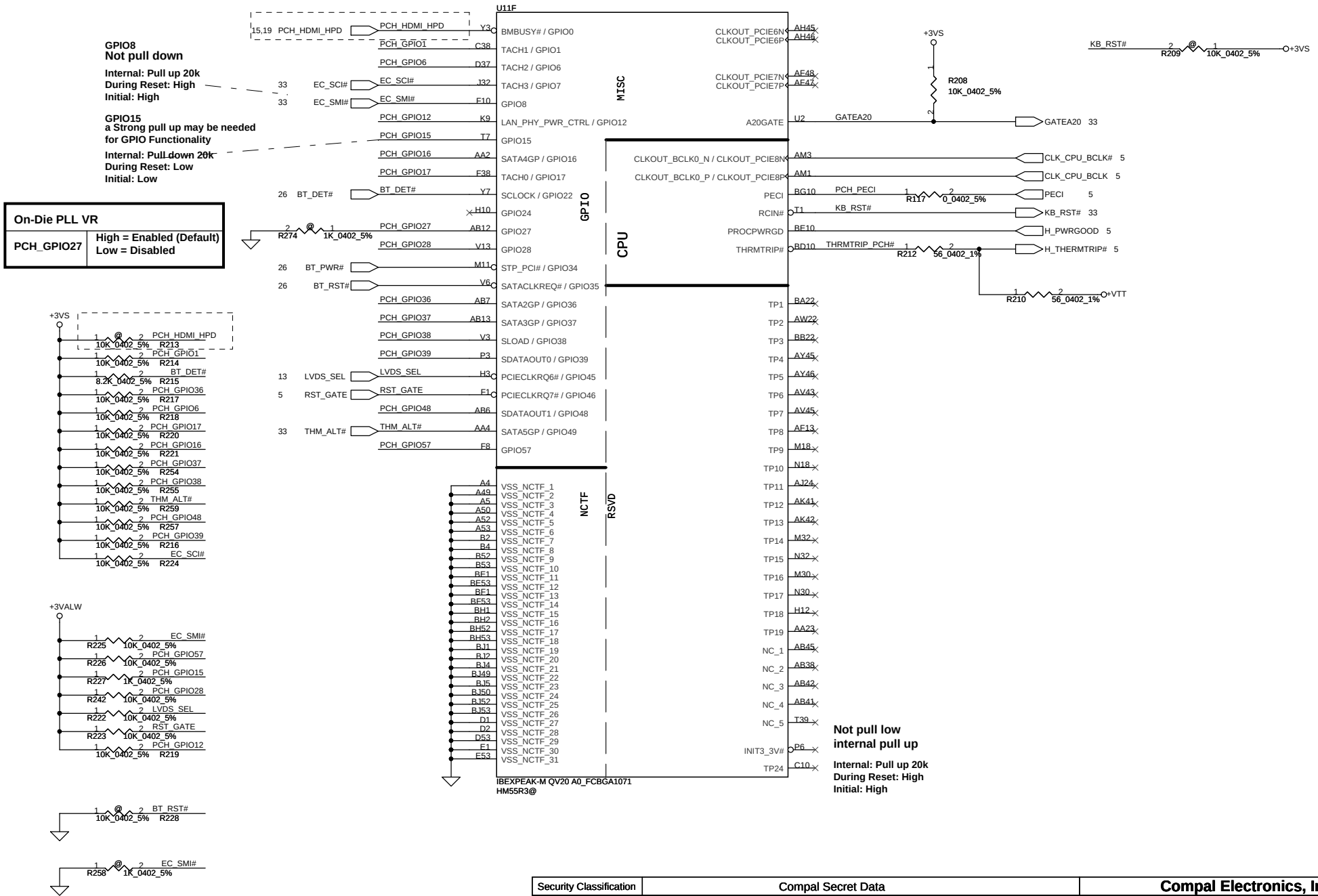

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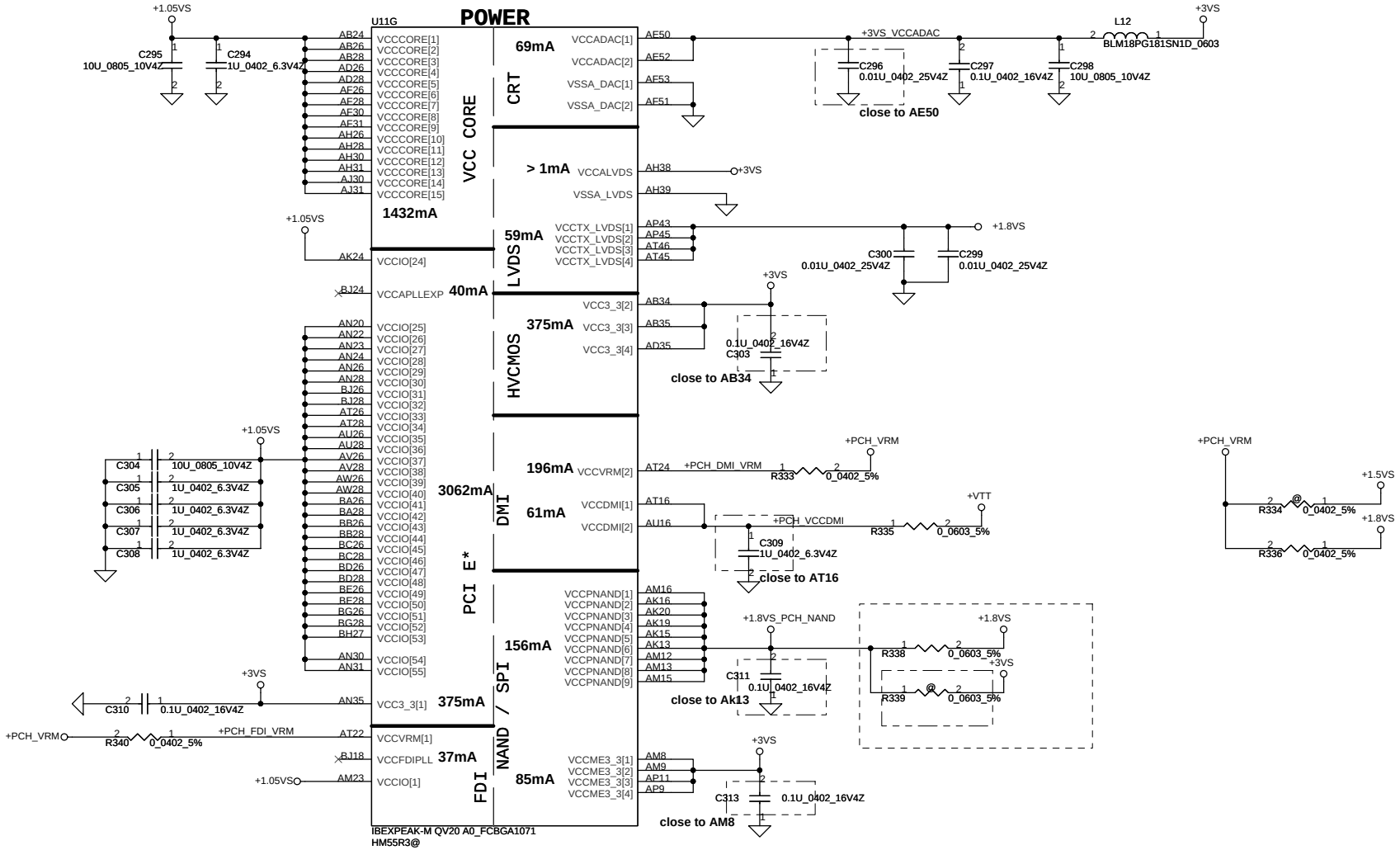

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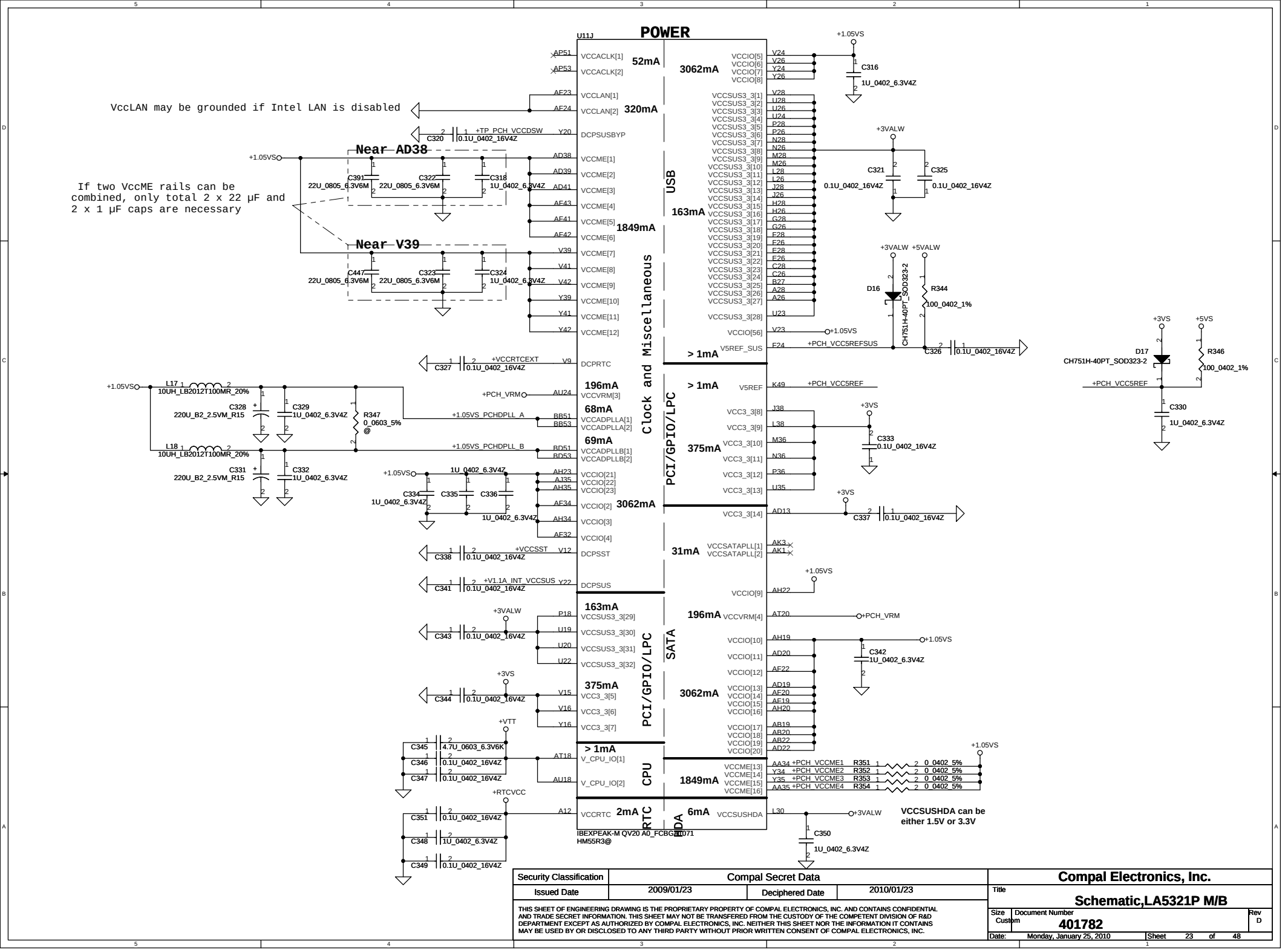

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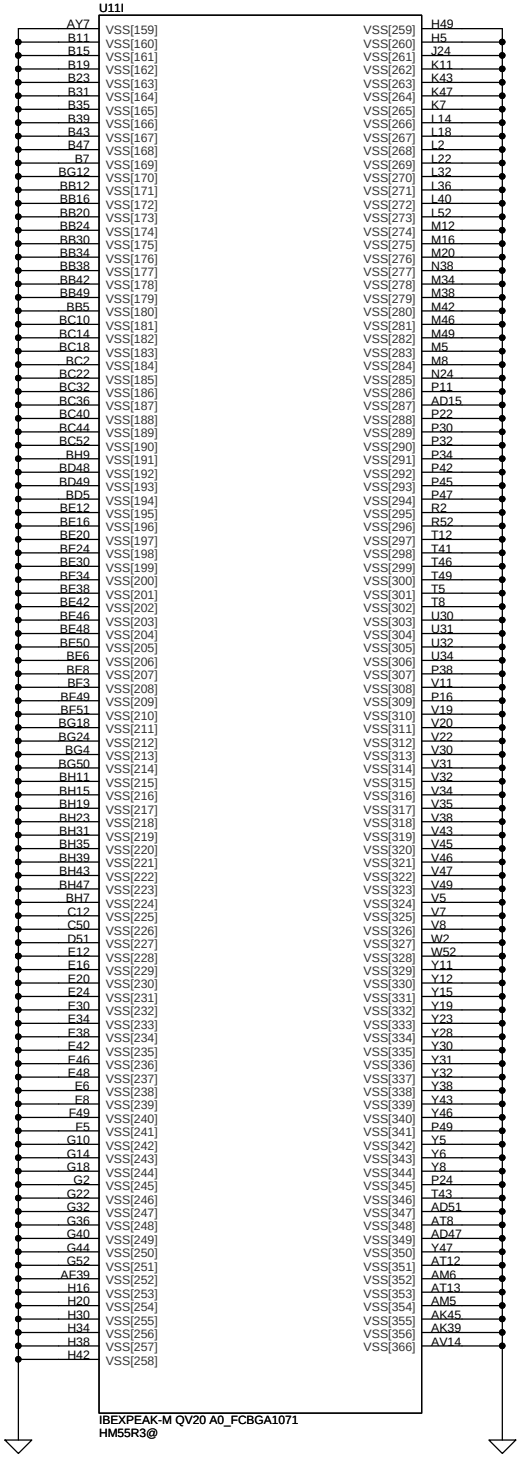

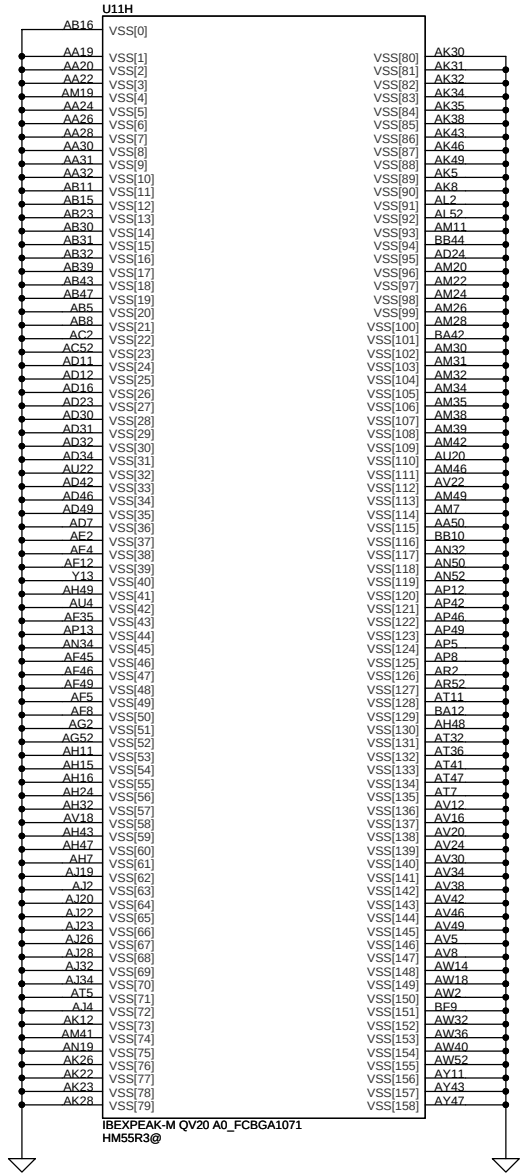

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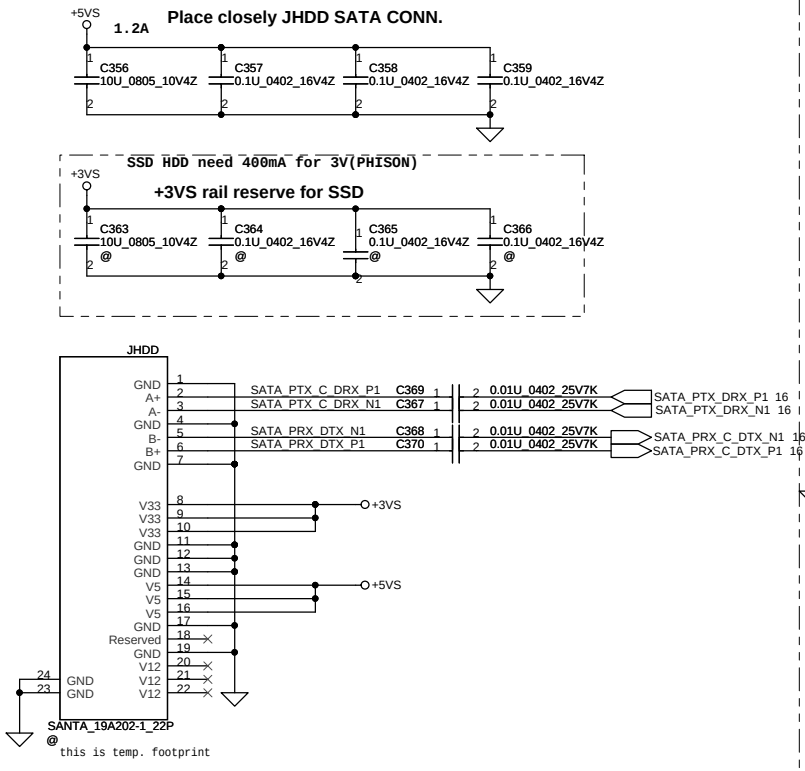
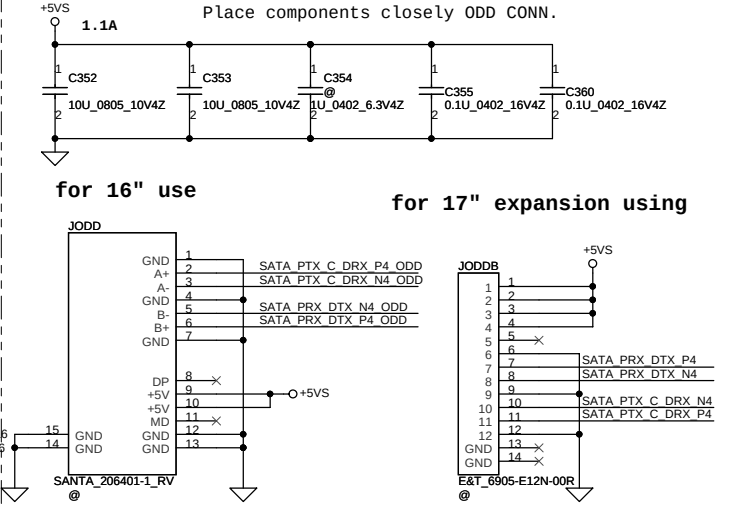
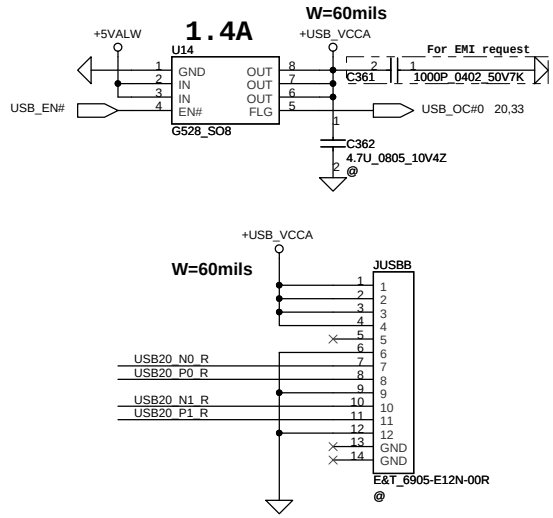
SATA HDD Conn.



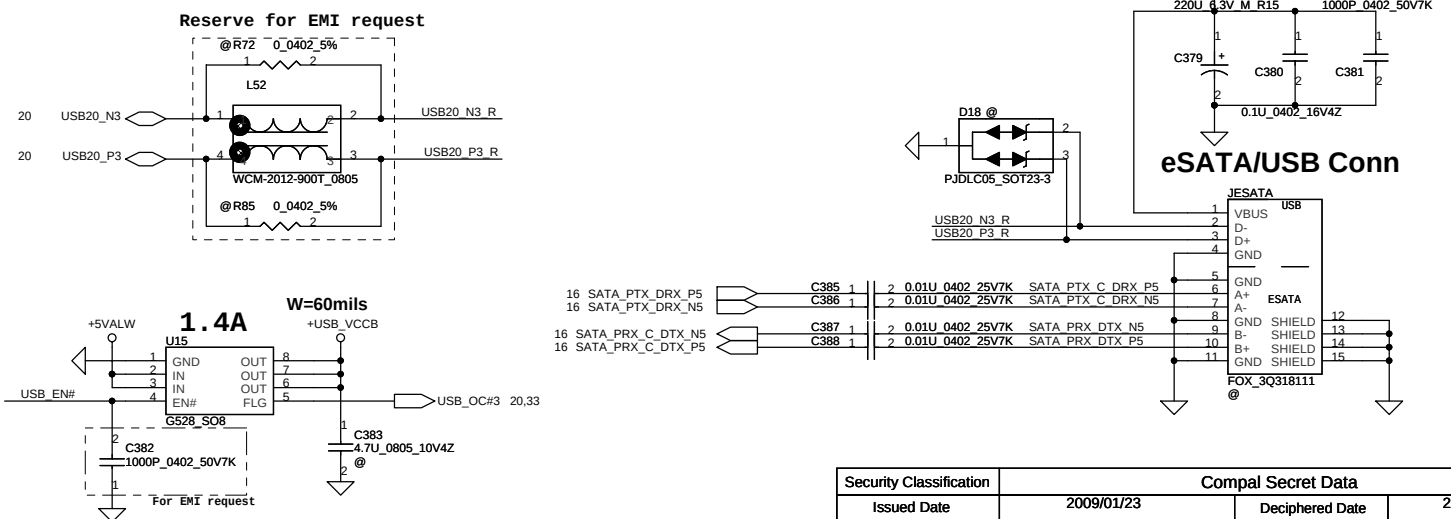
SATA ODD Conn



USB Board



eSATA/USB



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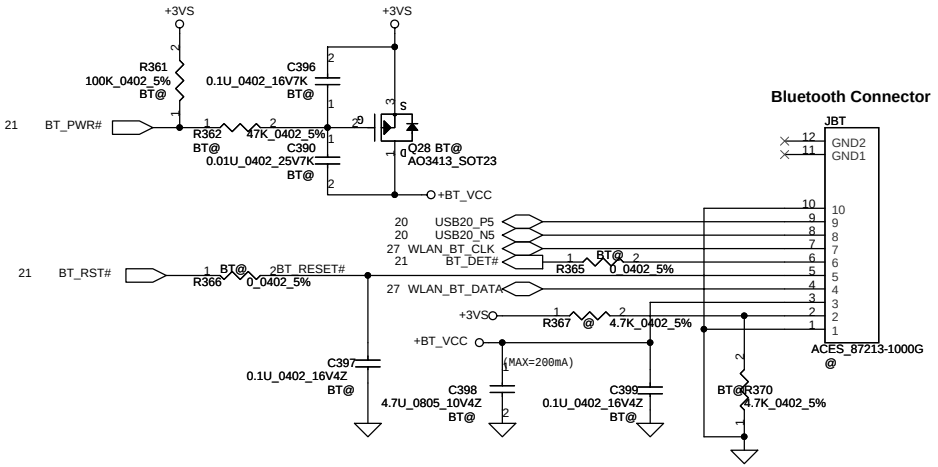
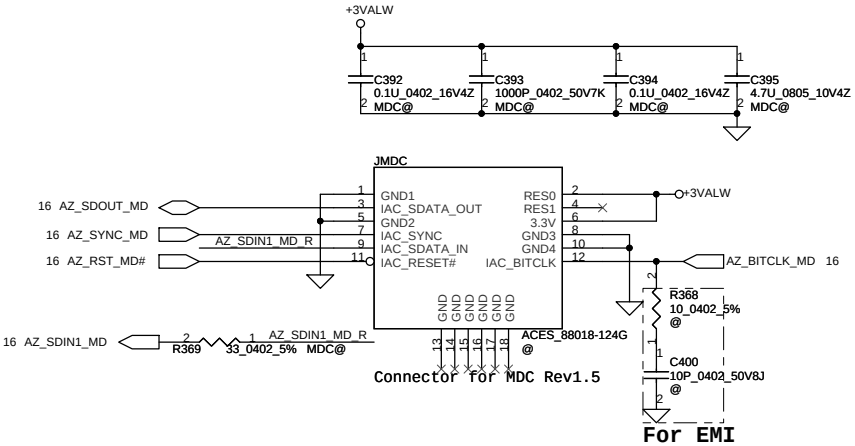
BlueTooth Interface

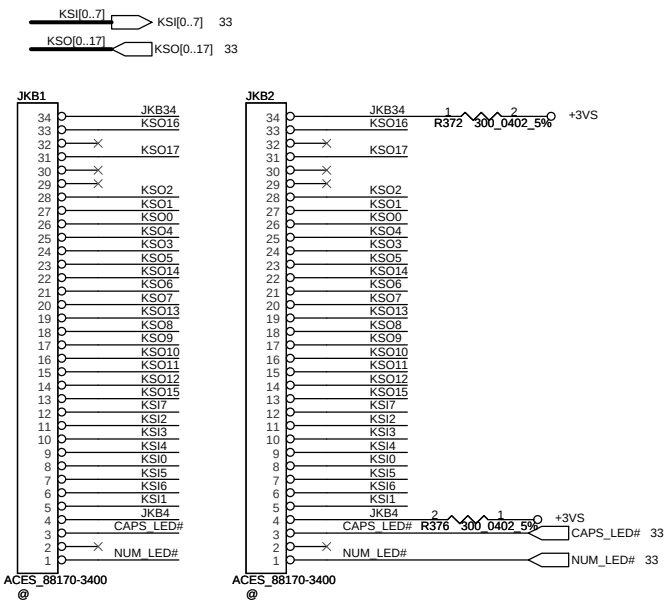


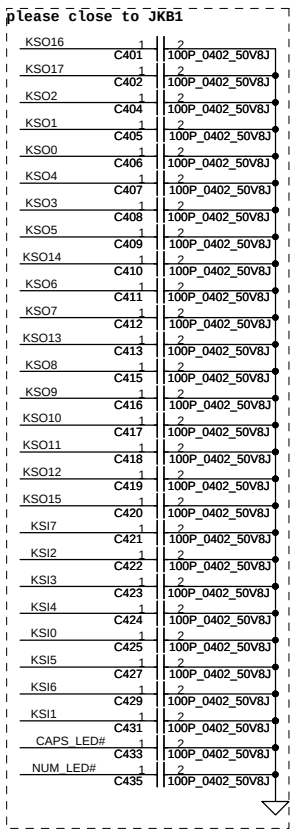
MDC 1.5 Conn.



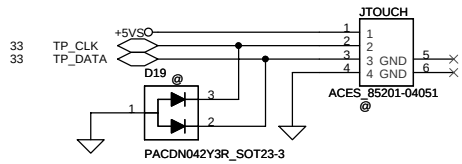
KEYBOARD CONN. for 16"

KEYBOARD CONN. for 17"

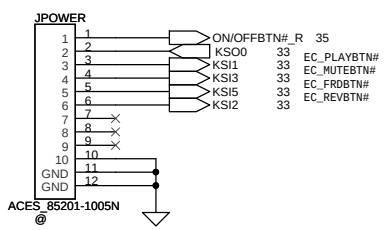


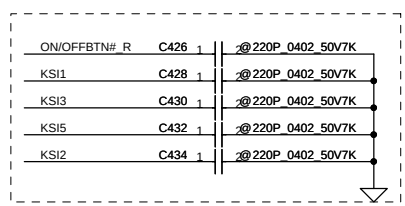


Touch/B Connector



SW/B Connector





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PCIe Mini Card-WLAN/WiMax

PJ27 JUMP_43X79 @ — +3VALW → +3V_WLAN
PJ26 JUMP_43X79 @ — +3VS

Short PJ27 for Wimax
Short PJ26 for WLAN

+3V_WLAN: 0.1U_0402_16V4Z — CM1 WLAN@, CM2 WLAN@, CM3 WLAN@ — 0.01U_0402_25V4Z; 4.7U_0805_10V4Z; C253 47P_0402_50V8J WLAN@ — *For SED*

+1.5VS: 0.1U_0402_16V4Z — CM7 WLAN@, CM8 WLAN@, CM9 WLAN@ — 0.01U_0402_25V4Z; 4.7U_0805_10V4Z; C254 47P_0402_50V8J WLAN@ — *For SED*

JWLAN — FOX_AS0B226-S40N-7F @

- 26 WLAN_BT_DATA
- 26 WLAN_BT_CLK
- 17 CLKREQ_WLAN#
- 17 CLK_WLAN#
- 17 CLK_WLAN
- XMIT_OFF# → XMIT_OFF# 33
- PLT_RST# → PLT_RST# 5,20,28,33,34
- 17 PCIE_PRX_WLANTX_N2
- 17 PCIE_PRX_WLANTX_P2
- PM_SMBCLK → PM_SMBCLK 11,12,13,17
- PM_SMBDATA → PM_SMBDATA 11,12,13,17
- 17 PCIE_PTX_C_WLANRX_N2
- 17 PCIE_PTX_C_WLANRX_P2
- USB20_N13 → USB20_N13 20
- USB20_P13 → USB20_P13 20

WLAN/ WiFi — **WiMax**

+3V_WLAN

83 E51_TXD — R16 0_0402_5%
83 E51_RXD — R17 0_0402_5%

Debug card using

RN5 1 — 2 PLT_RST# 100K_0402_5%

PCIe Mini Card-3G

+3VS

J3G — FOX_AS0B226-S40N-7F @

- UIM_DATA
- UIM_CLK
- UIM_RESET
- UIM_VPP
- +UIM_PWR
- PLT_RST# → 3G_OFF# 33
- PM_SMBCLK
- PM_SMBDATA
- USB20_N12 20
- USB20_P12 20

3G

+3VS: 0.1U_0402_16V4Z — CM4 3G@, CM5 3G@, CM6 3G@ — 0.01U_0402_25V4Z; 4.7U_0805_10V4Z; C255 47P_0402_50V8J 3G@ — ***90 MIL*** — *For SED*

+UIM_PWR

CM13 0.1U_0402_16V4Z 3G@ — DM1 RLZ20A_LL34 3G@

J3GSIM — MOLEX_47273-0001~D @

- VCC
- RST
- CLK
- NC
- GND
- VPP
- I/O
- NC
- UIM_RESET
- UIM_CLK
- UIM_VPP
- UIM_DATA

CM15 10P_0402_50V8J 3G@ — CM16 10P_0402_50V8J 3G@

DM2 DAN217_SC59 @ — DM3 DAN217_SC59 @ — DM4 DAN217_SC59 @

RM2 4.7K_0402_5% @ — CM14 22P_0402_50V8J @

+3VALW

RN4 1 — NEW@ 2 CP_USB# 100K_0402_5%

RN3 1 — 2 EXP_CPPE# 10K_0402_5%

share with USB OC PIN need always pull high

+3VALW_CARD: Imax = 0.275A — CN1 10U_0805_10V4Z NEW@, CN2 0.1U_0402_16V4Z NEW@

+3VS_CARD: Imax = 1.35A — CN3 10U_0805_10V4Z NEW@, CN4 0.1U_0402_16V4Z NEW@

+1.5VS_CARD: Imax = 0.75A — CN5 10U_0805_10V4Z NEW@, CN6 0.1U_0402_16V4Z NEW@

UN1 NEW@ — TPS2231MRGPR-2 QFN

- +1.5VS → 1.5Vin, 1.5Vout → +1.5VS_CARD — **60mils**
- +3VS → 3.3Vin, 3.3Vout → +3VS_CARD — **40mils**
- +3VALW → AUX_IN, AUX_OUT → +3VALW_CARD — **40mils**
- PLT_RST# → SYSRST#
- 33,42,43 SYSON → SHDN#
- 29,33,36,39,42,43 SUSP# → STBY#
- EXP_CPPE# → CPPE#
- CP_USB# → CPUSB#
- RCLKEN → RCLKEN
- OC# → PERST# (PERST#)
- NC, GND, Thermal_Pad

+3VS: RN6 10K_0402_5% @; RN7 10K_0402_5% @; CN7 0.1U_0402_16V4Z @

UN2 @ — NC7SZ32P5X_NL_SC70-5

- CLKREQ# → CLKREQ_NEW# → CLKREQ_NEW# 17

Q5A 2N7002DW-T/R7_SOT363-6 — **another at page36**

RCLKEN

CLKREQ# 1 — NEW@ 2 CLKREQ_NEW# RN8 0_0402_5%

Reserve for EMI request

R95 0_0402_5% NEW@ — L56 @ — R94 0_0402_5% NEW@

- 20 USB20_P8 → USB20_P8_R
- 20 USB20_N8 → USB20_N8_R

WCM-2012-900T_0805

JEXP — SANTA_132862-2_26P @ — this is temp. footprint

- USB20_N8_R
- USB20_P8_R
- CP_USB#
- PM_SMBCLK
- PM_SMBDATA
- +1.5VS_CARD
- 18,28 EC_SWI#
- +3VALW_CARD
- PERST#
- +3VS_CARD
- CLKREQ#
- EXP_CPPE#
- 17 CLK_NEW#
- 17 CLK_NEW
- 17 PCIE_PRX_NEWTX_N1
- 17 PCIE_PRX_NEWTX_P1
- 17 PCIE_PTX_C_NEWRX_N1
- 17 PCIE_PTX_C_NEWRX_P1

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Compal Electronics, Inc.

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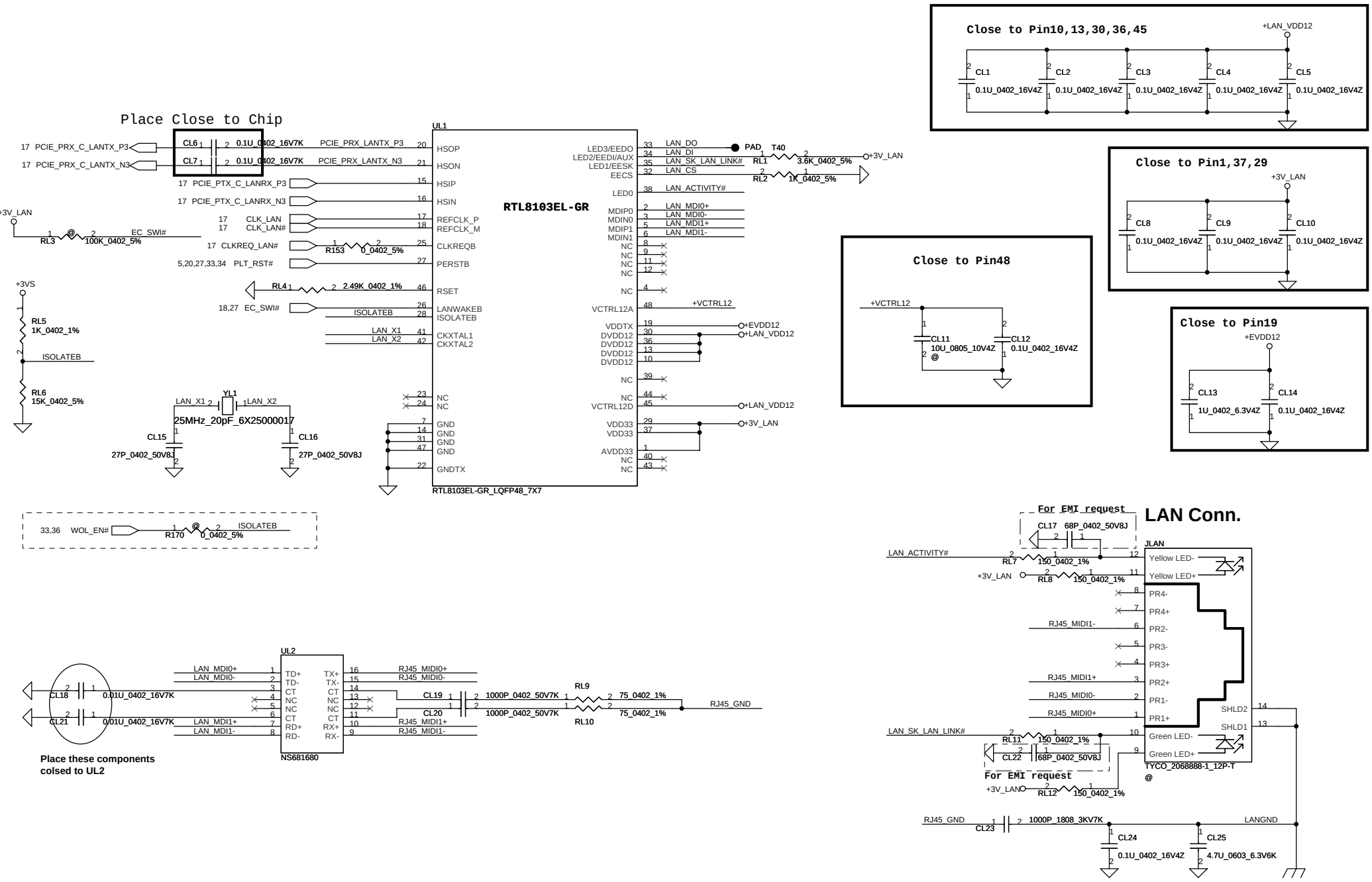

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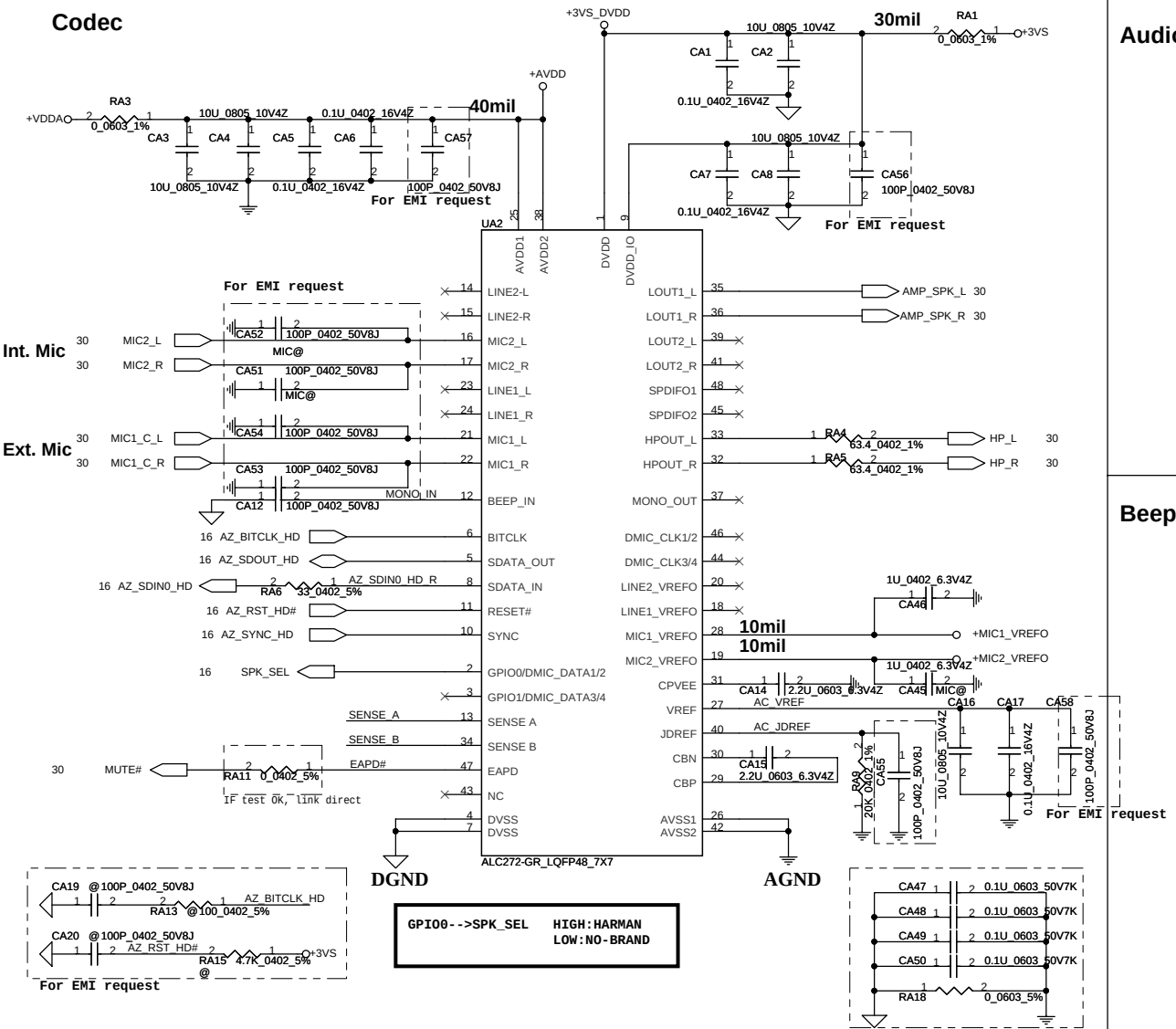
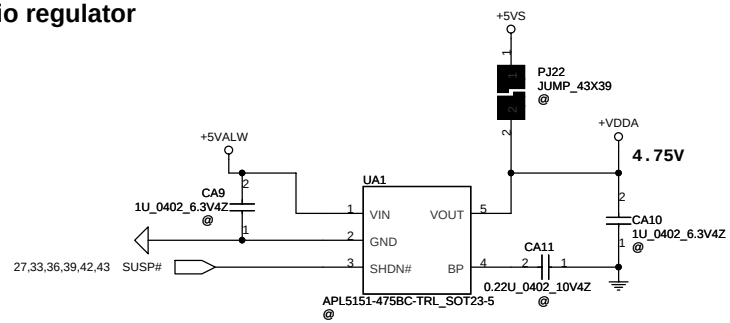
Codec

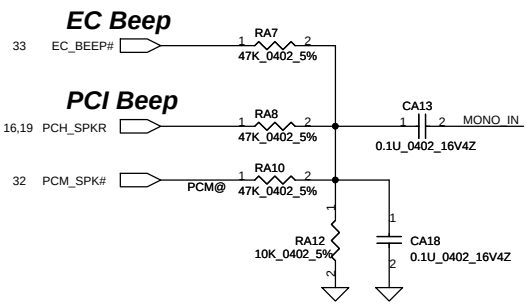


GPIO0-->SPK_SEL HIGH:HARMAN
LOW:NO-BRAND

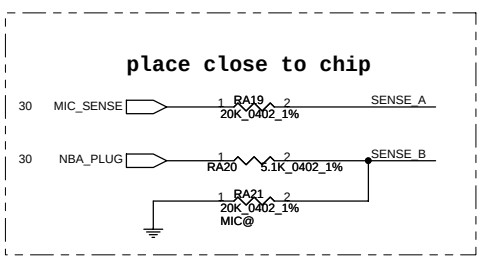
Audio regulator



Beep sound



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



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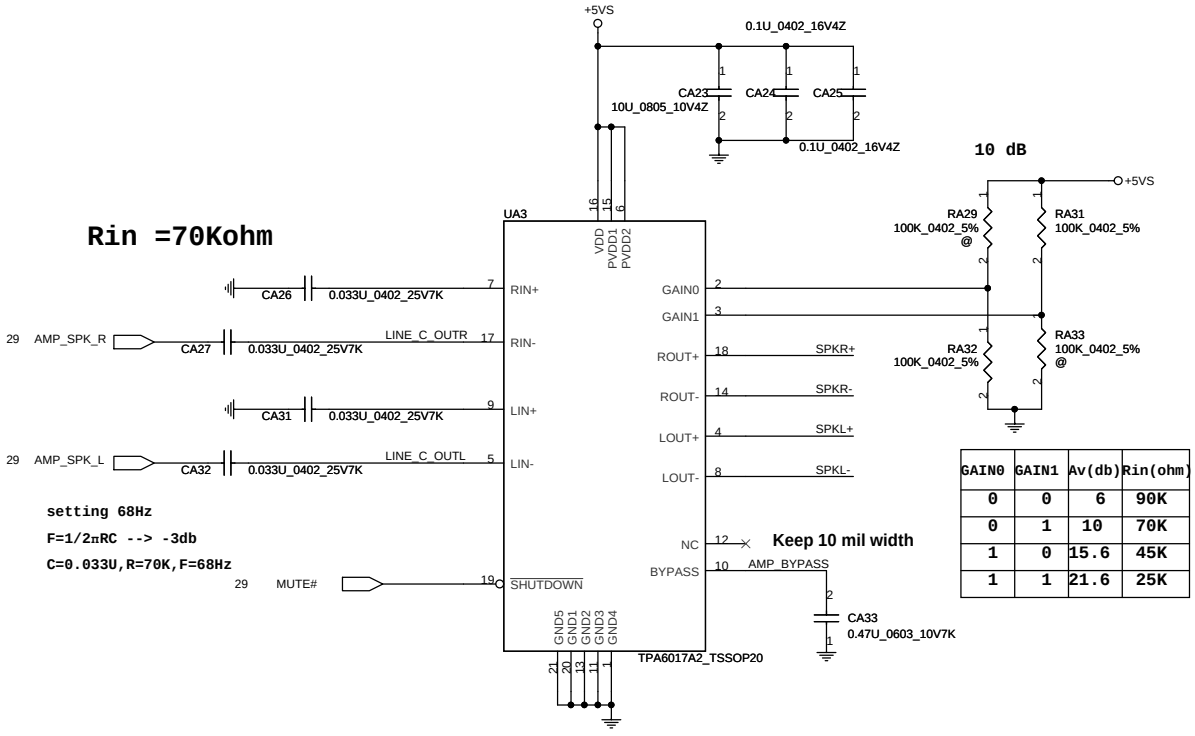
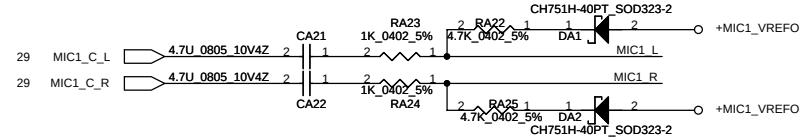
TPA6017 Medium Range Amplifier

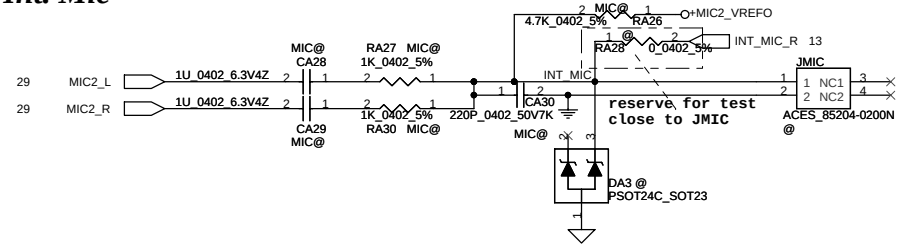


GAIN0	GAIN1	Av(db)	Rin(ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

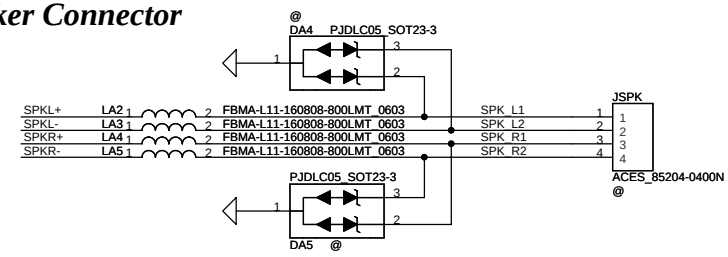
Ext. Mic



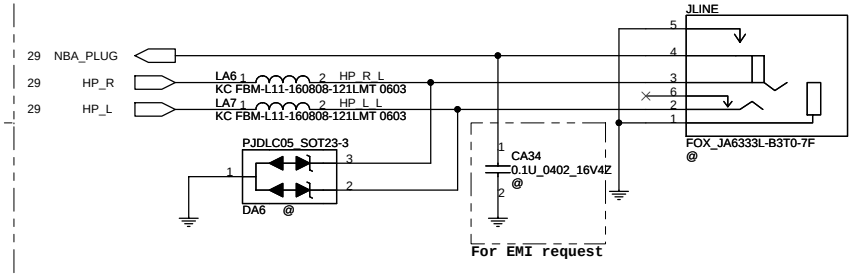
Int. Mic



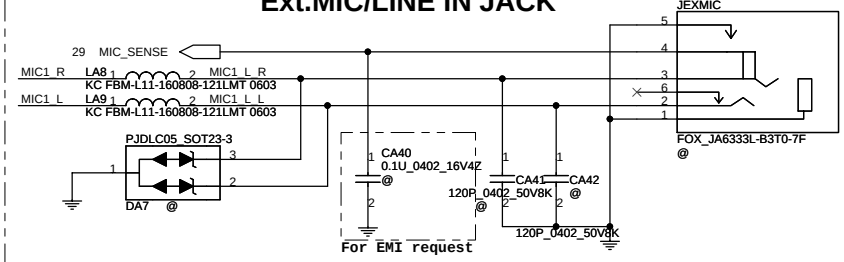
Speaker Connector



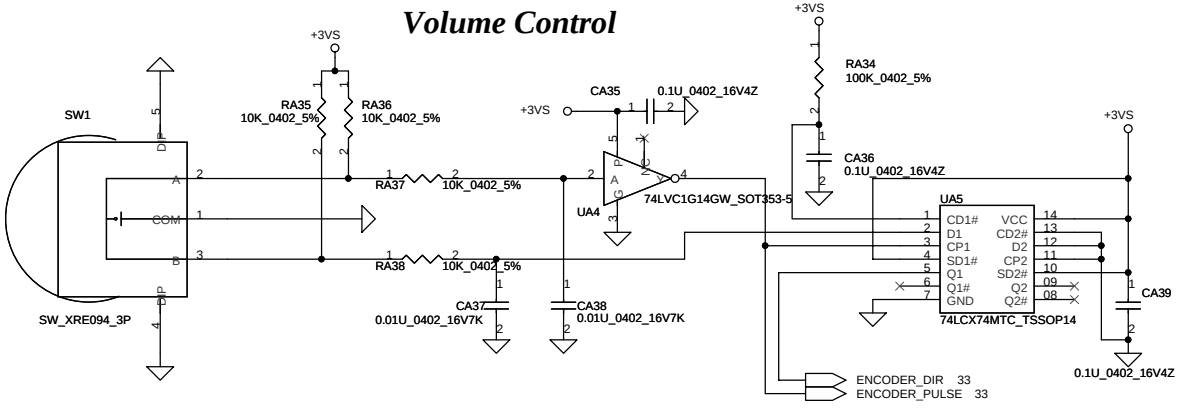
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK



Volume Control



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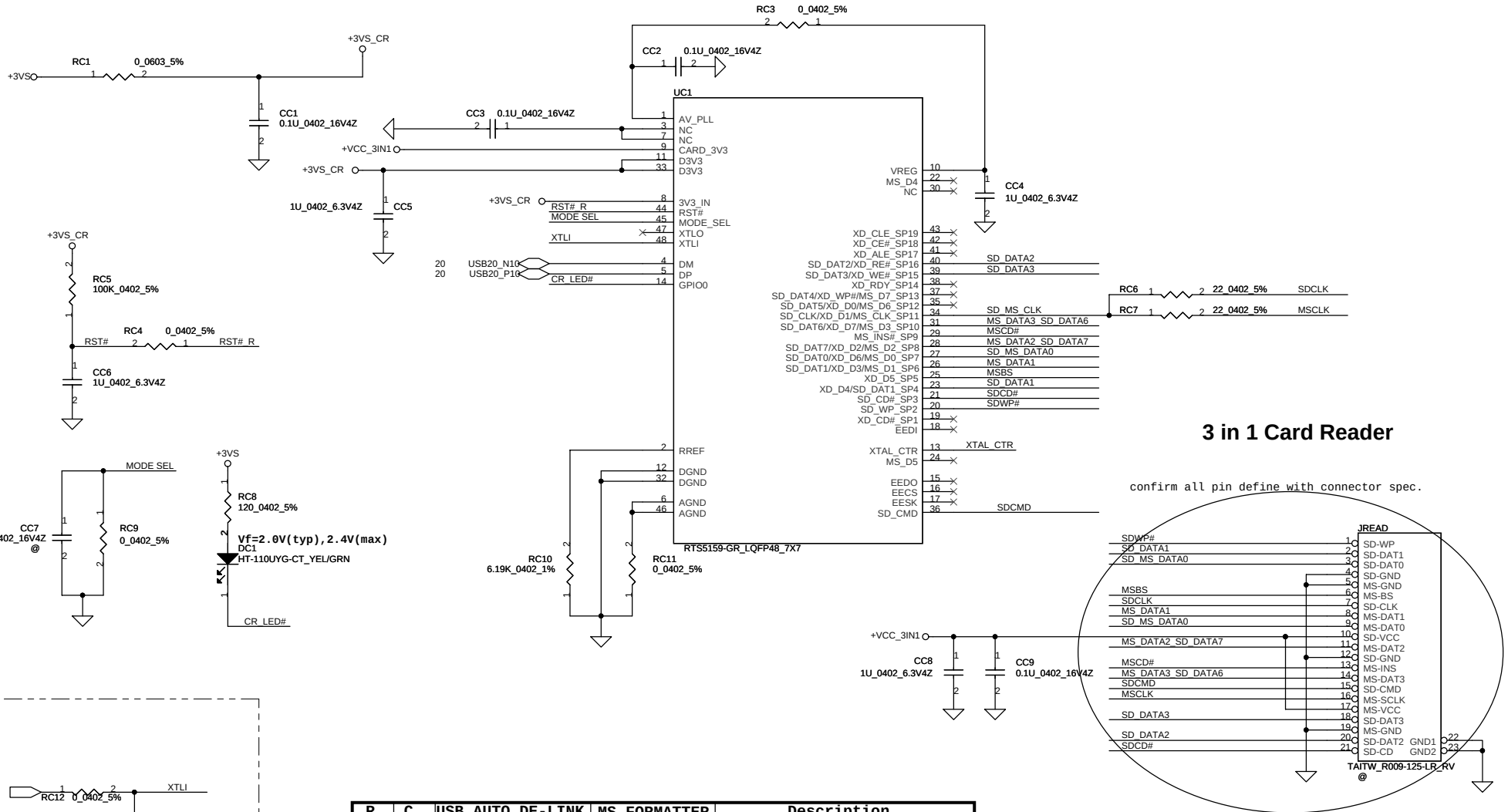

R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

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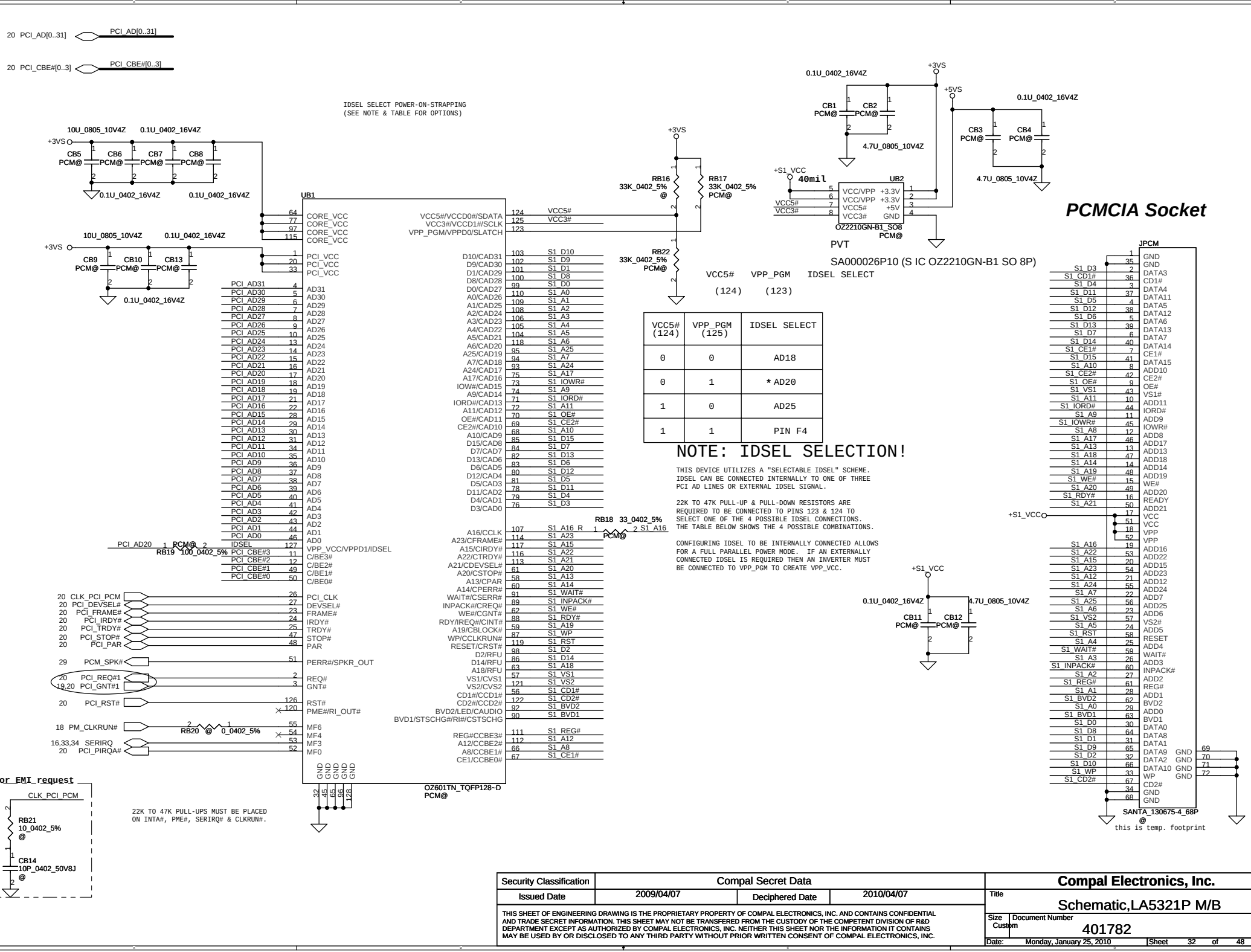

VCC5# (124)	VPP_PGM (125)	IDSEL SELECT
0	0	AD18
0	1	*AD20
1	0	AD25
1	1	PIN F4

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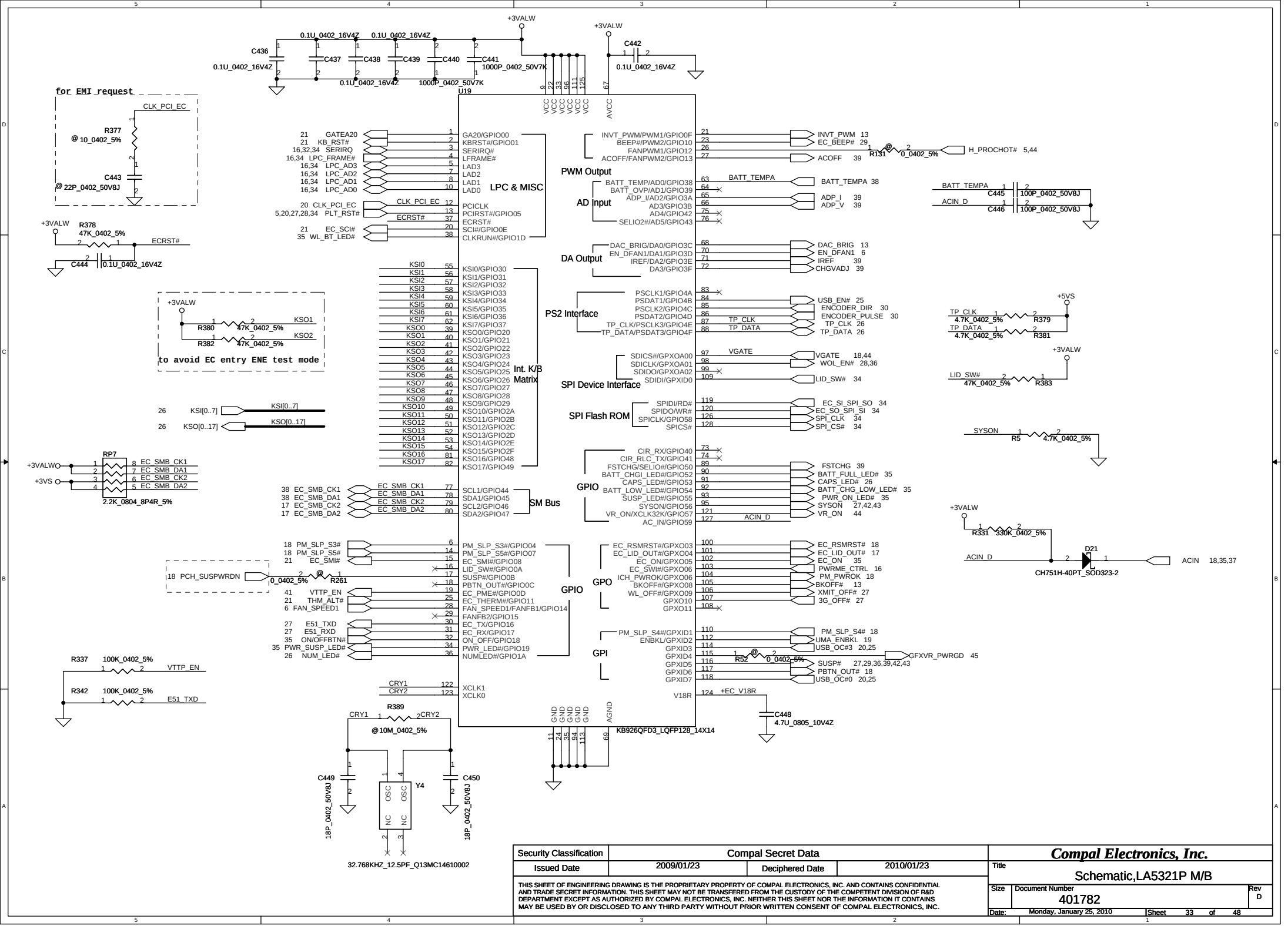

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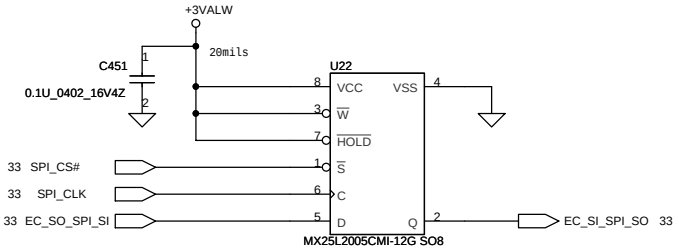
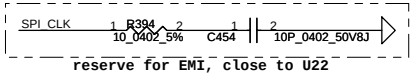
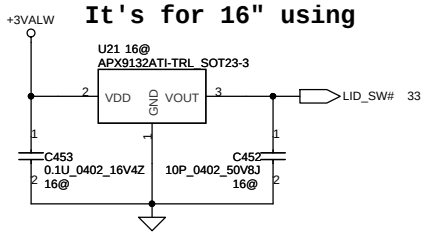
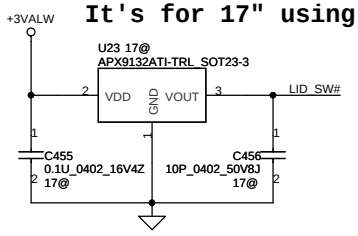
SPI Flash (256KB)





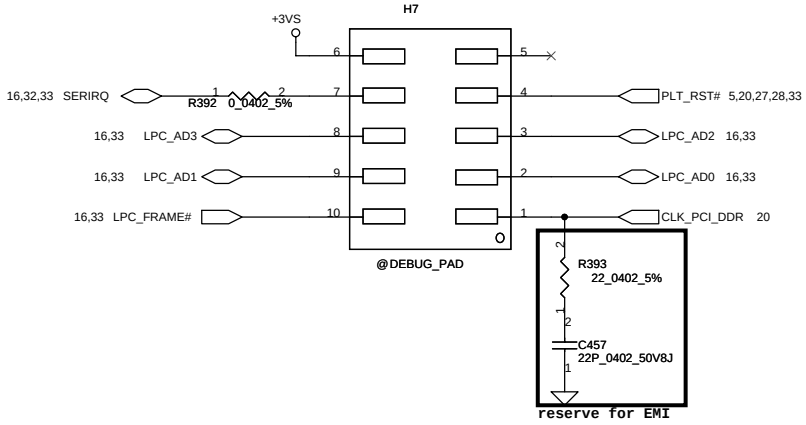
Lid SW





LPC Debug Port

Please place the PAD under DDR DIMM.



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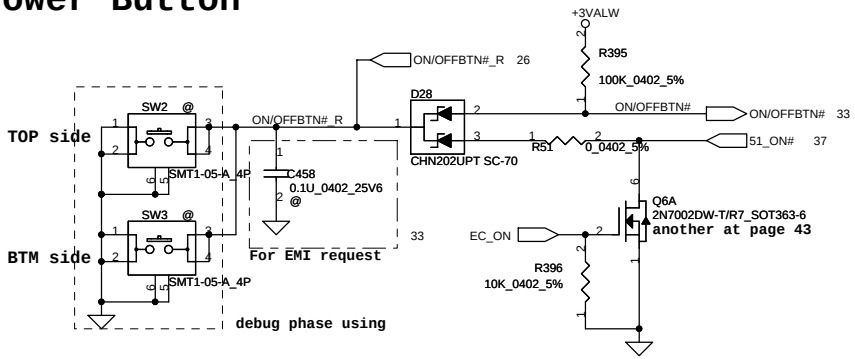
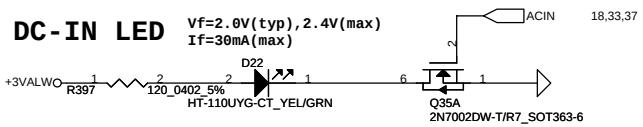
Power Button

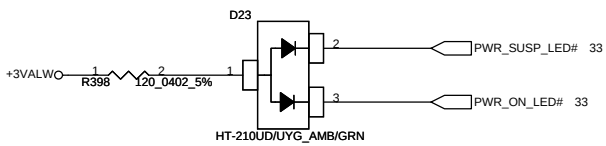


DC-IN LED

Vf=2.0V(typ),2.4V(max)
If=30mA(max)

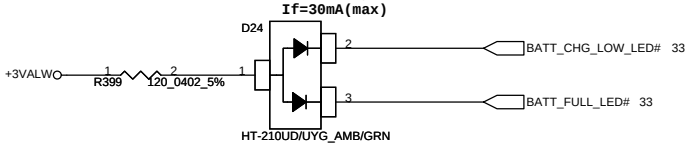


POWER/SUSPEND LED

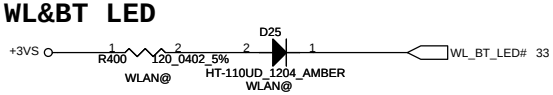


BATT CHARGE/FULL LED

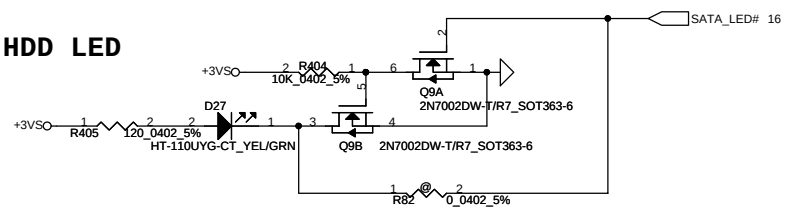
Vf=1.9V(typ),2.4V(max) for amber
Vf=2.0V(typ),2.4V(max) for green
If=30mA(max)



WL&BT LED



HDD LED



ISPD

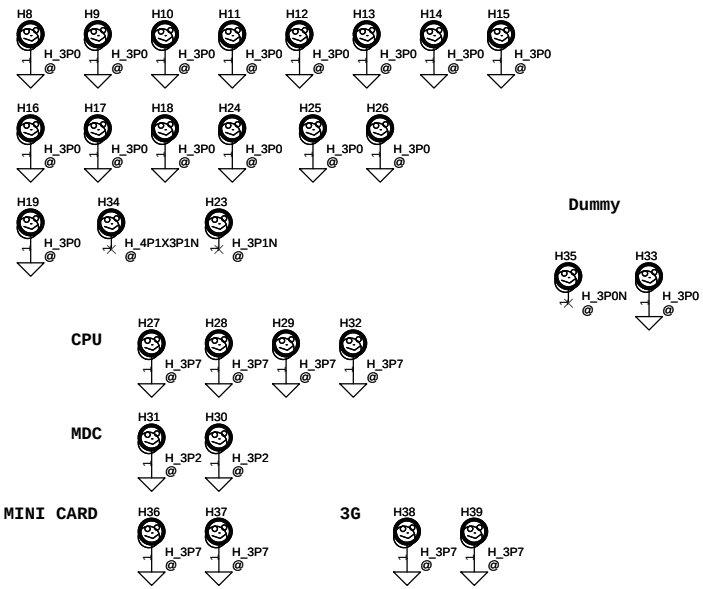
PCB — ZZZ — PCB LA-5321P REV10

PCH — U11 — PCH HM55R1@

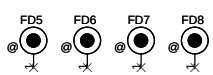
DC-IN 16 — PJP1 — PJP1 NSWAA45@

DC-IN 17 — PJP1 — PJP1 NTWAA45@

Screw Hole



PCB Fedical Mark PAD



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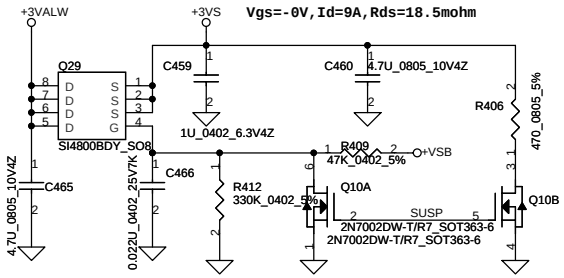
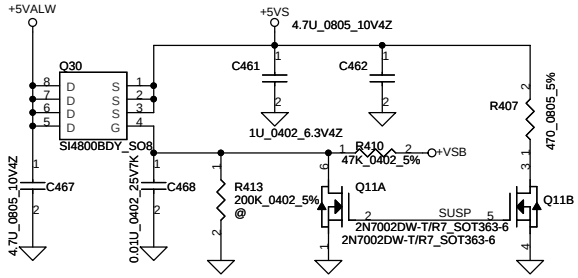
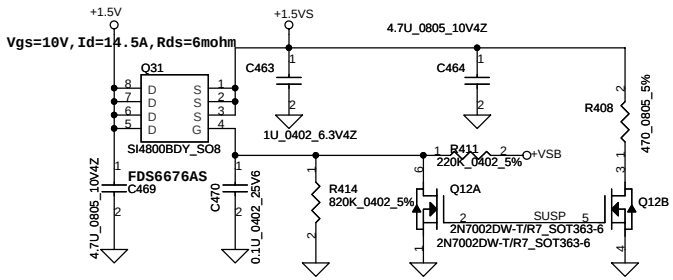
+3VALW TO +3VS



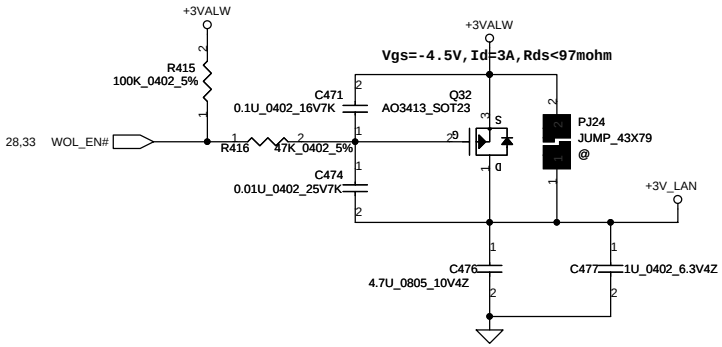
+5VALW TO +5VS

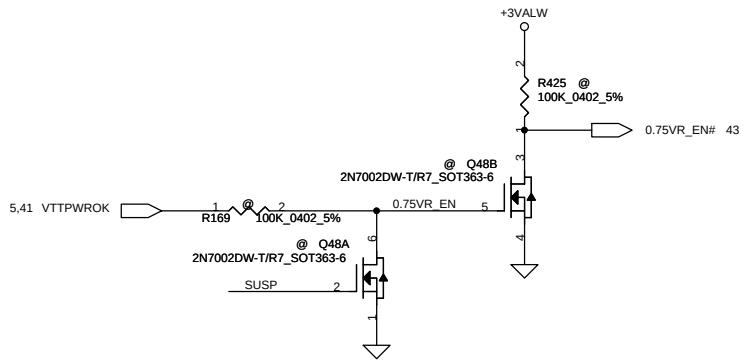


+1.5V to +1.5VS

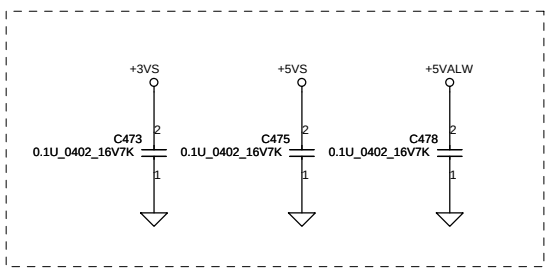


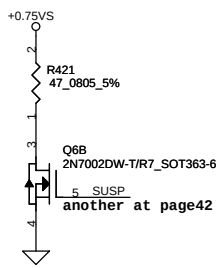
+3VALW TO +3V_LAN

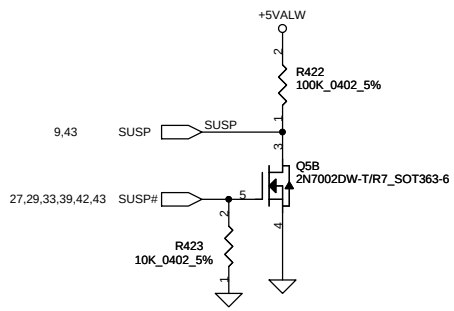




Reserve for EMI test







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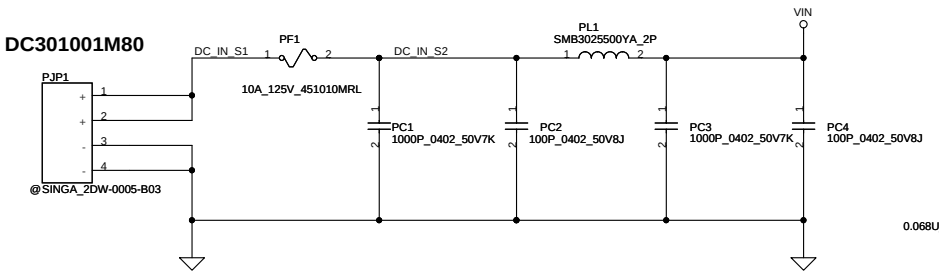
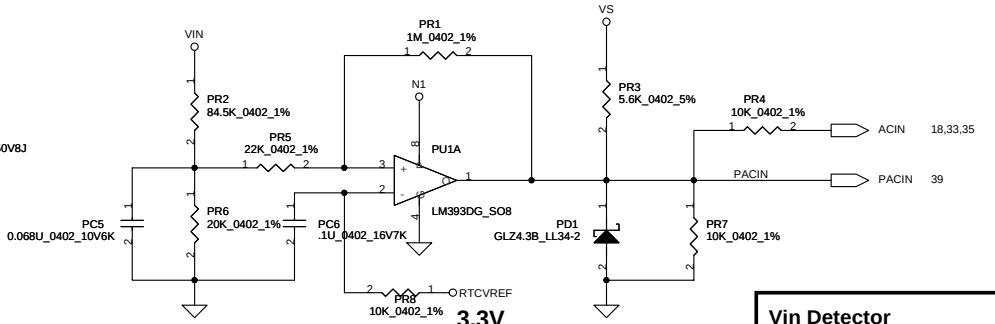
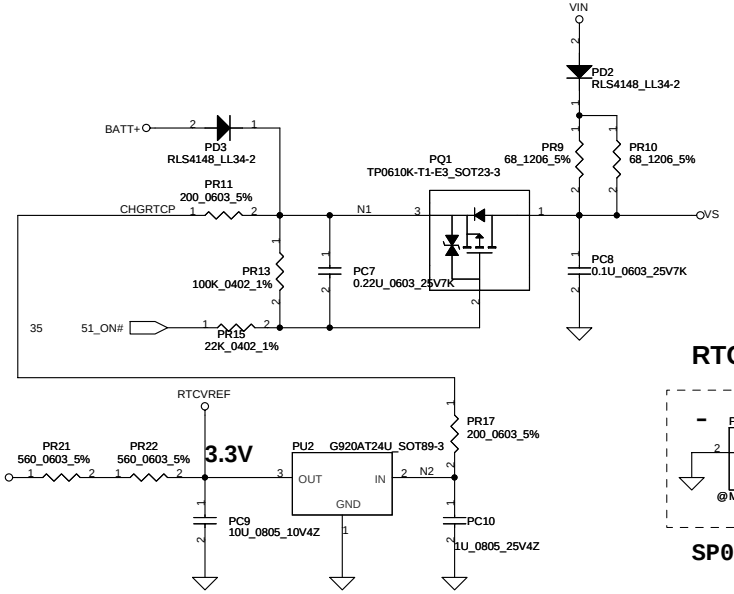


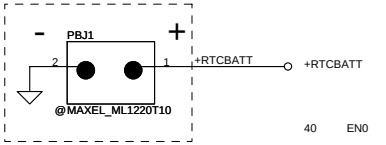


Vin Detector

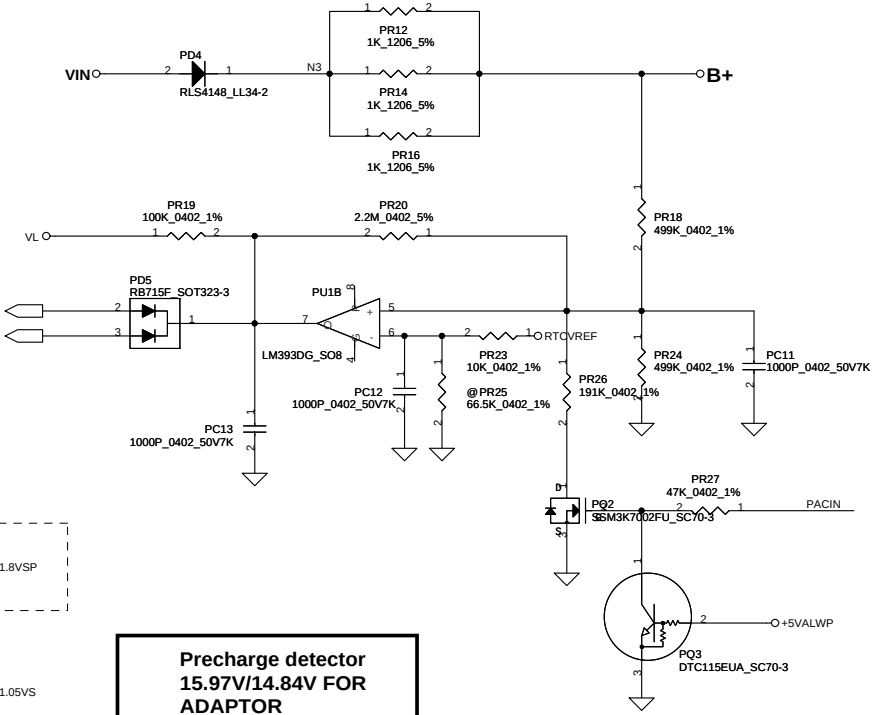
High	**18.384**	**17.901**	**17.430**
Low	**17.728**	**17.257**	**16.976**



RTC Battery



SP093MX0000

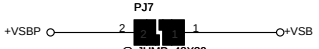


(5A,200mils ,Via NO.= 10)

OCP(min)=7.7A

(5A,200mils ,Via NO.= 10)

OCP(min)=7.9A



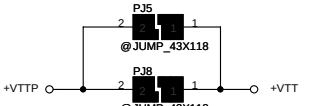
(120mA,40mils ,Via NO.= 1)

(1.5A,80mils ,Via NO.= 4)

(1.5A,60mils ,Via NO.= 4)

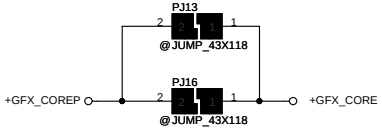
(9A,360mils ,Via NO.= 18)

OCP(min)=9.8A



(18A,720mils ,Via NO.=36)

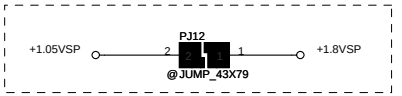
OCP(min)=20.64A

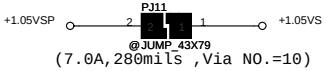


15A,600mils ,Via NO.=30)

OCP(min)=28.71A

Add on 10/29





(7.0A,280mils ,Via NO.=10)

OCP(min)=8.4A

Precharge detector
15.97V/14.84V FOR
ADAPTOR

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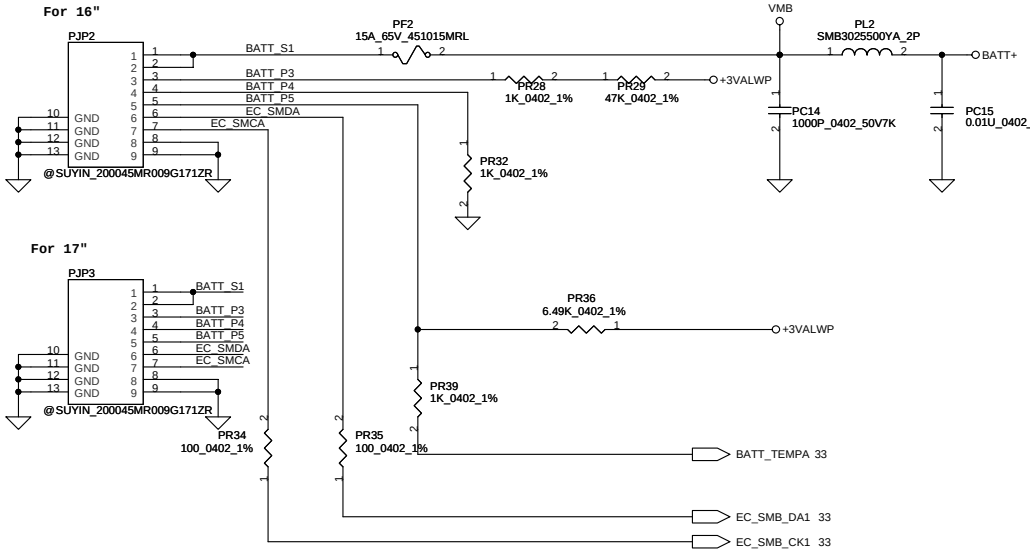
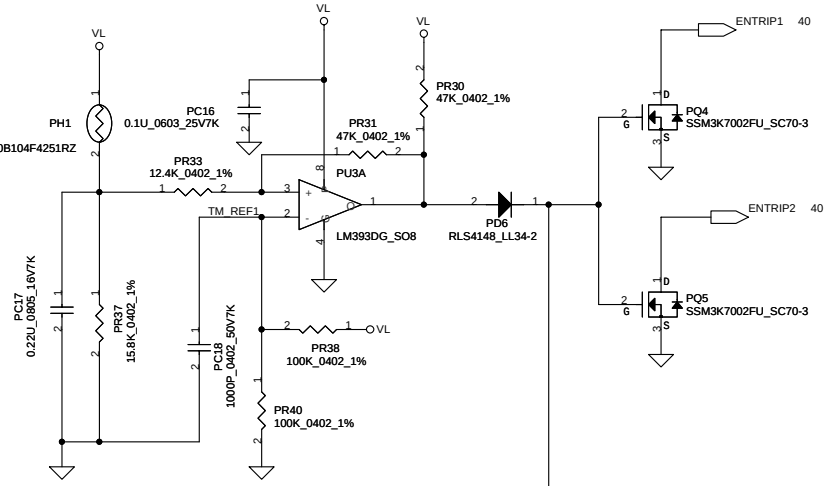
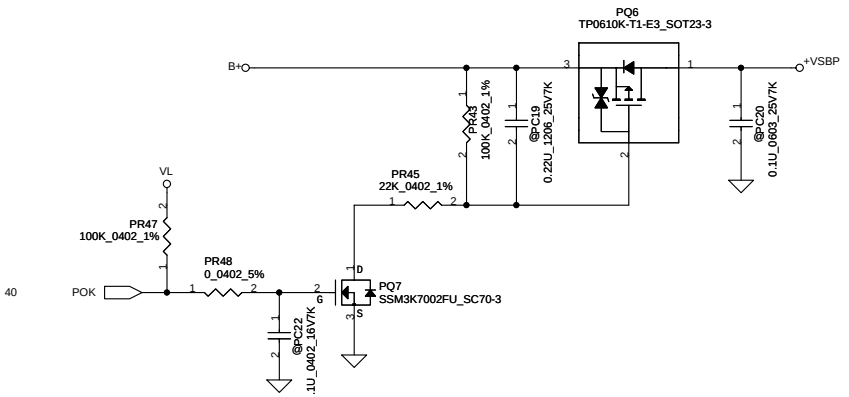
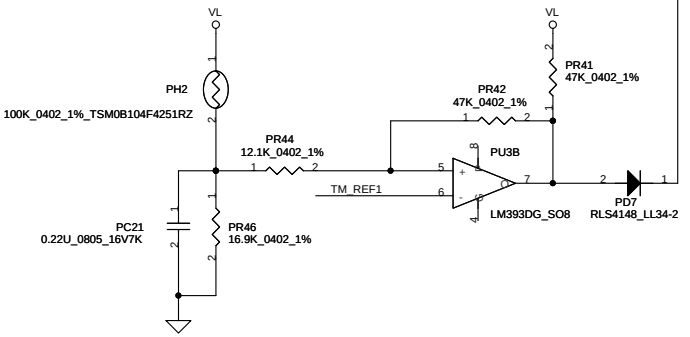
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





PH2 near main Battery CONN :
BAT. thermal protection at 90 degree C
Recovery at 55 degree C





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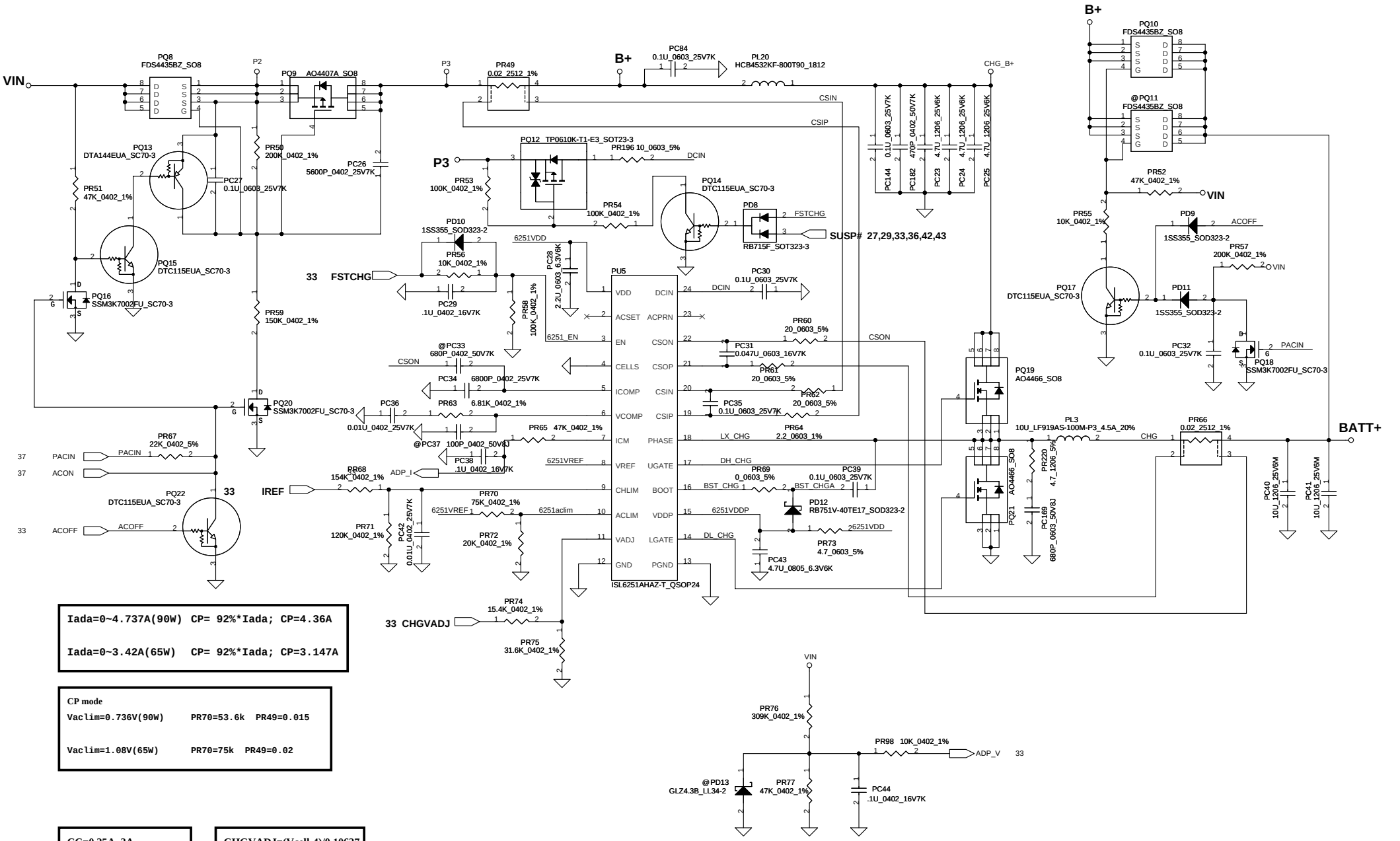

Iada=0~4.737A(90W)	CP= 92%*Iada; CP=4.36A
Iada=0~3.42A(65W)	CP= 92%*Iada; CP=3.147A

CP mode

Vaclim=0.736V(90W)	PR70=53.6k PR49=0.015
Vaclim=1.08V(65W)	PR70=75k PR49=0.02

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CELLS	VDD	GND	Float
CELL number	4	3	2

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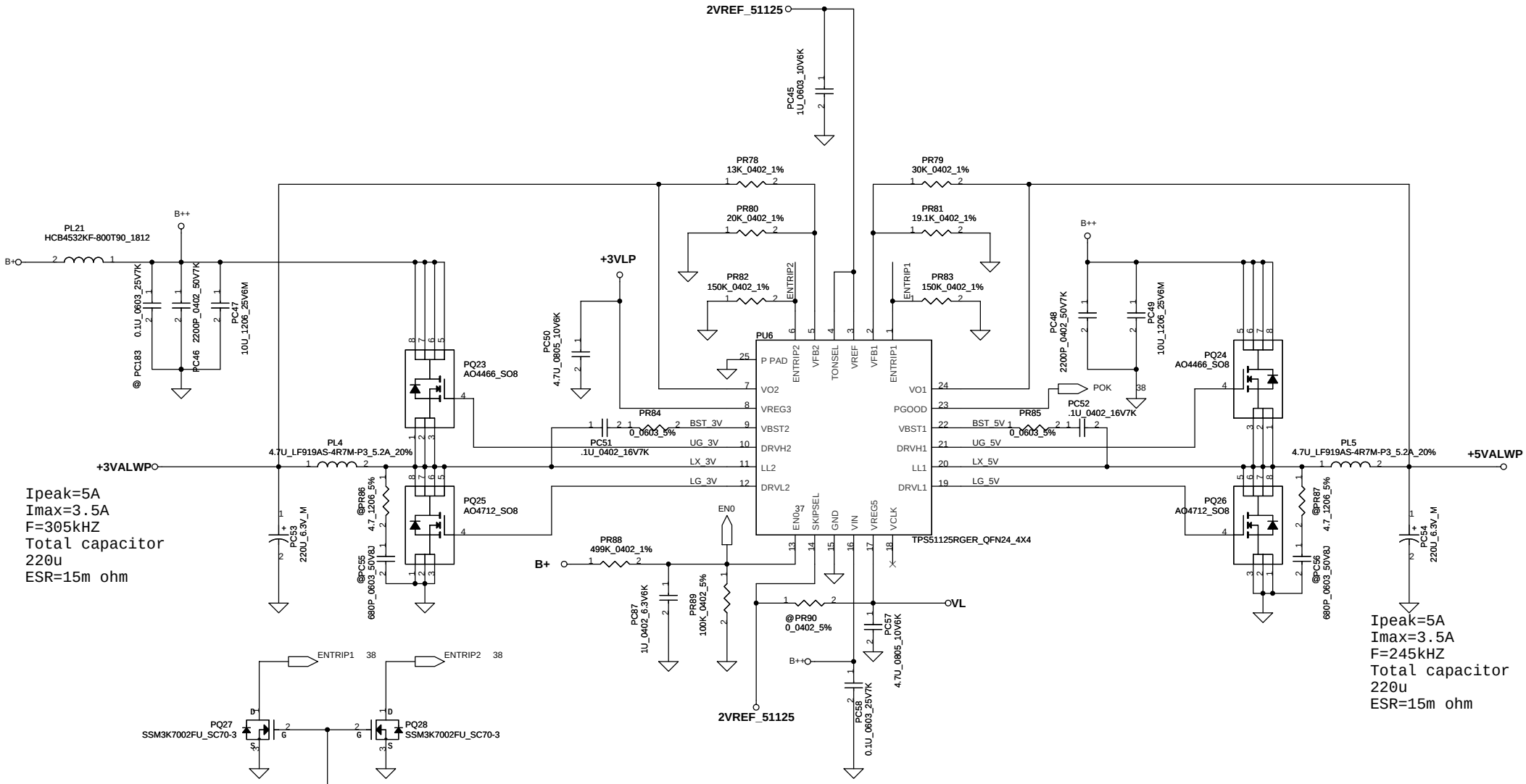

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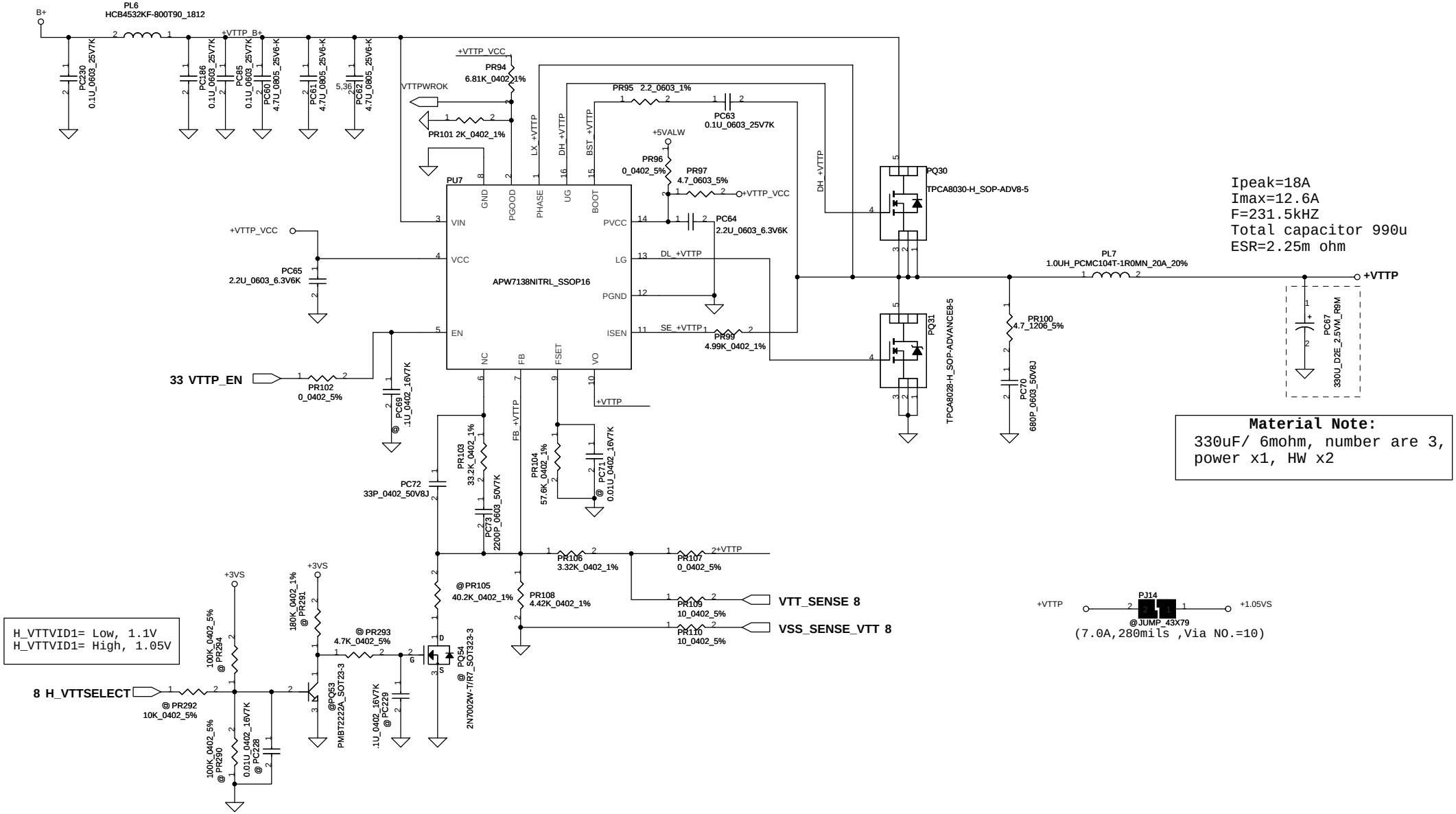

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

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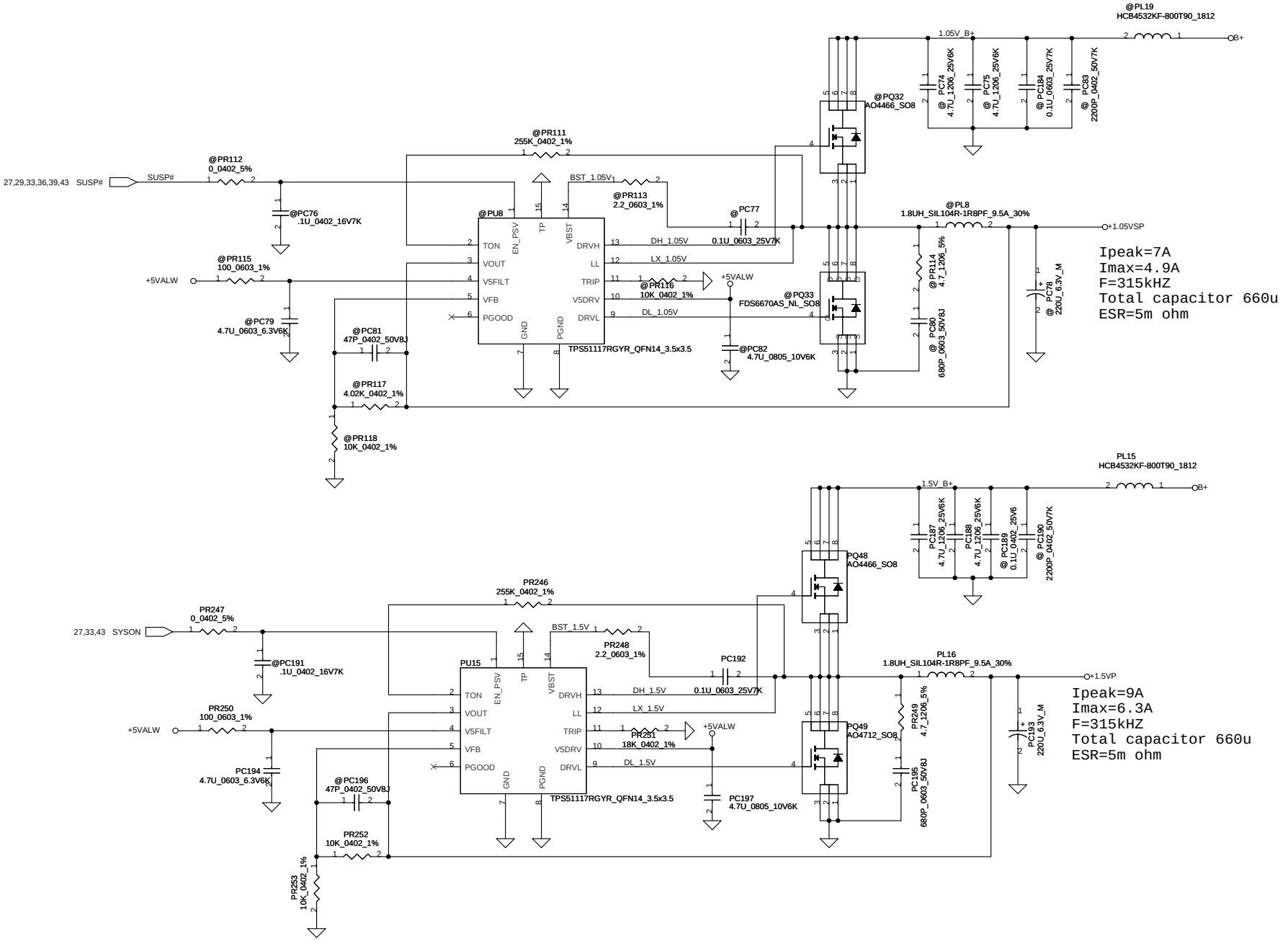

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

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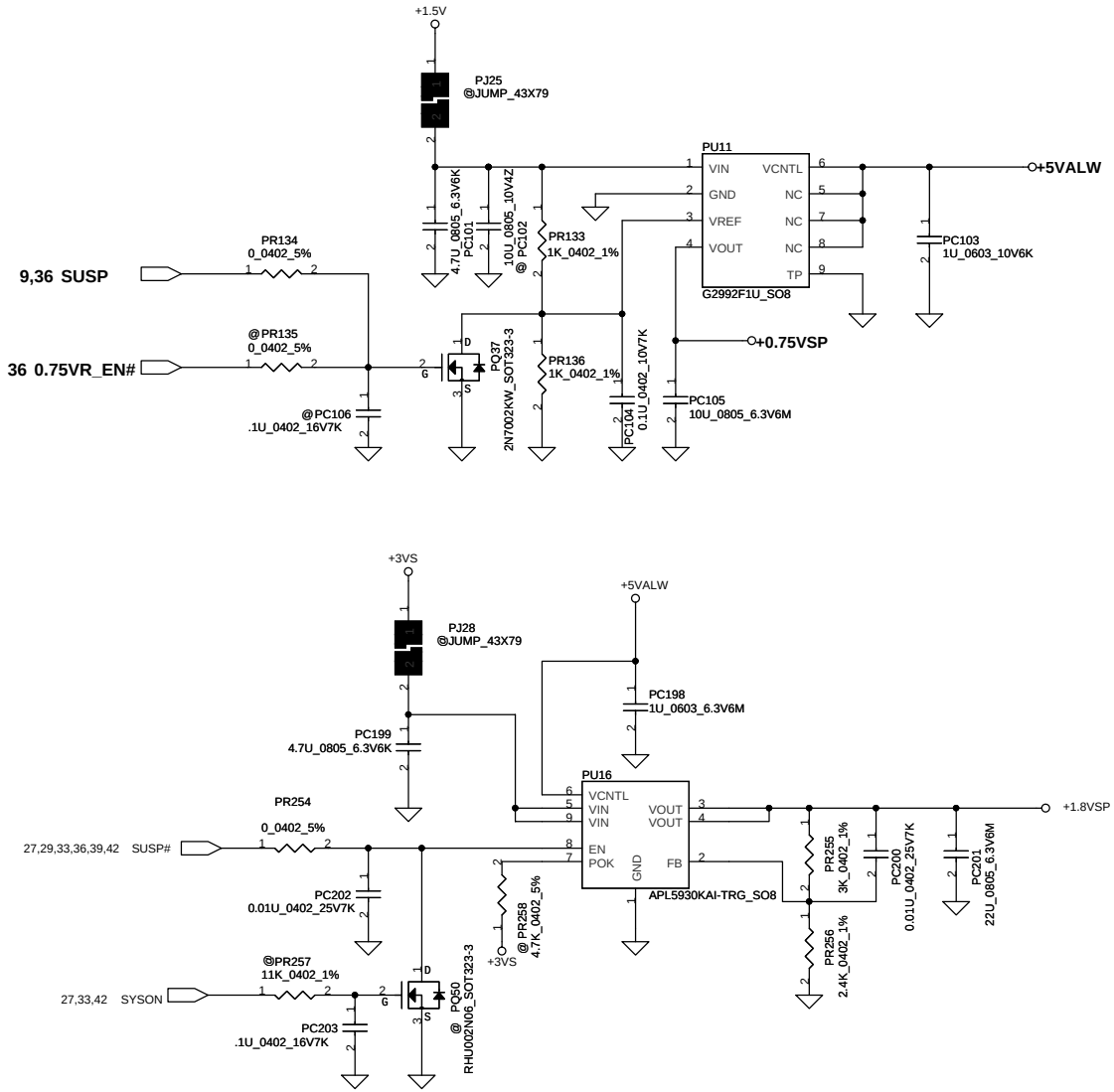

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

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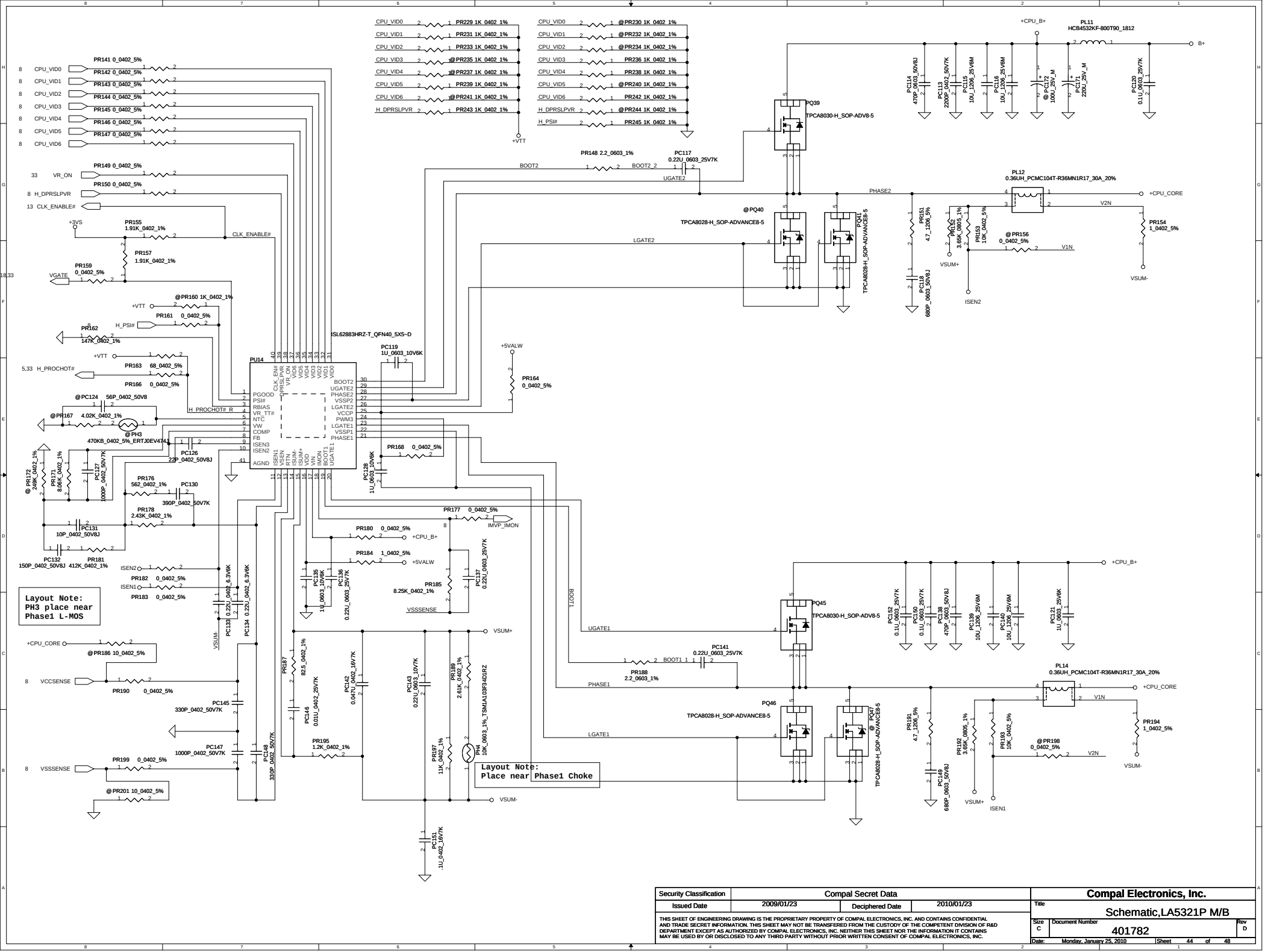

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

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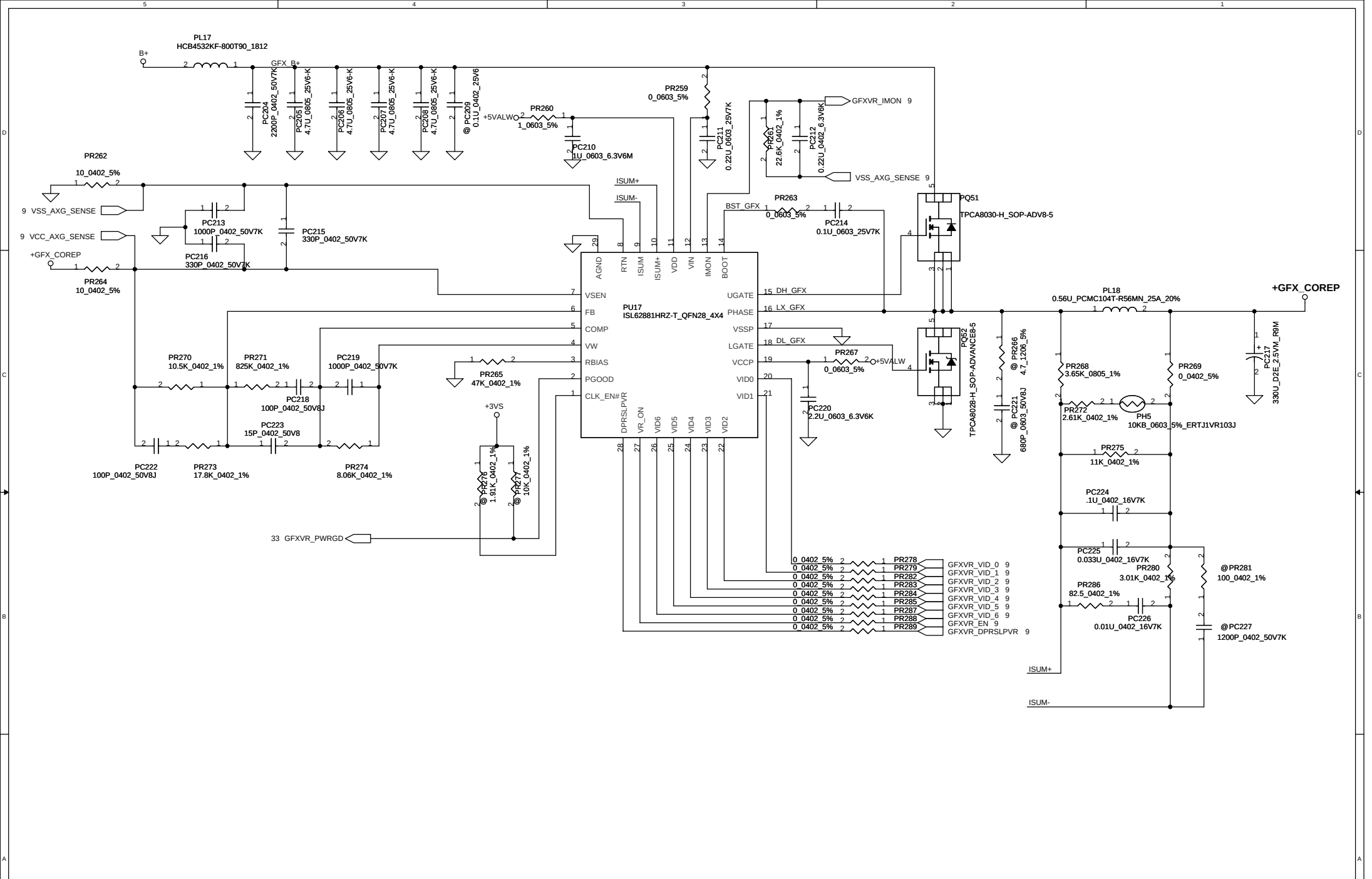

Security Classification	Compal Secret Data		
Issued Date	2009/02/02	Deciphered Date	2009/02/02

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PIR (Product Improve Record)

NSWAA LA-5321P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	6/29	18	Change R324 from 10K to 330K	To solve ACIN LED issue
	7/02	21	Change BT_PWR# from GPIO0 to GPIO34, add VGA_HDMI_HPD on GPIO0.	For common design with NSKAA
	7/02	26	DEL JCAM (R431,R432,C403,R371,R373,R374,R375,L20)	CAM cable combine with LVDS
	7/02	13	DEL R387	Remove +5VALW power to camera
	7/02	31	DEL YC1,CC10,CC12	Remove 12MHz crystal to cardreader
	7/02	31	DEL RC2	Remove +3VALW to cardreader
	7/03	13	Add R126,R401	Reserve +1.5VS to clk gen for low power clk gen test
	7/03	13,21	Add R155	Reserve LVDS_SEL on PCH GPIO45
	7/03	16,33	Connect PCH GPIO33 to EC pin 103 as PWRME_CTRL Change 3G_OFF# from EC pin 103 to pin 107	To reflash ME BIOS
	7/17	35	Add R82 on SATA_LED#	Reserve for cost down plan
	7/17	20	DEL R277,D12, Connect USB_OC#3_D to USB_OC#3	
	7/17	18,33,35	DEL R384, D14. Add R331	Modify ACIN circuit
	7/17	13,35	Change Q7,Q34 to Dual Q35	For cost down
	7/17	15	DEL R169~R172, C267,C268,C271,C272	No need for ASMedia level shifter
	7/20	5,9,11,21	Add Q41,R19,R127,R22,D54,U16,R33,R84,Q33,R424,R418, C267,Q46,C472,R417,C230,C218,C205,C186,PJ30,PJ31,R83 Q48,R425,R169 Add RST_GATE on PCH GPIO46	Reserve S3 power reduction circuit
	7/27	33	Add R5	To solve SYSON glitch issue
	7/27	21,33	Connect PCH GPIO49 to EC pin25 as THM_ALT#	Reserve for test
	7/27	8,9,11	Add C159,C160,C271,C180,C179,C185,C217,C268	For cost down
	7/30	36	Add C473,C475,C478	For EMI request
	7/30	16,34	Change U13 to 8MB, U22 to 1MB	For SW and EC request
	7/30	20	DEL Braidwood circuit	Calpella don't support Braidwood

NSWAA LA-5321P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	8/4	5	Change VTTPWROK to VTTPWROK_CPU on CPU side	Modify S3 power saving circuit
	8/4	15	Add R189 on PCH_HDMI_HPD	Add for no IHDMI sku
	8/4	36	Change Q31 from SI4856 to SI4800	Cost down
	8/19	15	Change HDMI level shifter from ST to ASMedia	For better HDMI signal quality
	8/19	13,19	Add R128,R130 for PCH BKL control	Reserve for deep green test

NSWAA LA-5321P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	9/28	32	Change UB1 pin53 connection from PCI_SERR# to SERIRQ	Modify PCMCIA circuit
	9/28	16	Change C287,C290 from 18p to 15p	To fine tune RTC timing
	10/15	15,21	Connect PCH_HDMI_HPD to PCH GPIO0	For TVAP HDMI control
	10/28	5	Reserve C301,C384,C389	Reserve for S3 power saving circuit

Security Classification	Compal Secret Data		Compal Electronics, Inc.
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT		P47-PWR_CHARGER	Change PR65 4.7 to 47k	For CPU throtting setting (2009/06/05)
EVT		P47-PWR_CHARGER	Change PR70 8.25k to 24k	Set 75W CP (2009/06/05)
			Change PR72 26.7k to 20k	
			Change PR49 0.015 Ohmto 0.02 Ohm	
EVT		P47-PWR_CHARGER	Change PQ8,PQ9,PQ10 AO4407 to FDS4435	Change PMOS for UMA SKU (2009/06/05)
EVT		P43-PWR_1.05VSP/1.5VP	Change PR115,PR250 422 Ohm to 100 Ohm	Avoid 2nd source RT8209B can no power on (2009/06/05)
			Change PC79,PC194 1U to 4.7U	
EVT		P43-PWR_1.05VSP/1.5VP	Change PR116 14.7k to 10k	Set 1.05V OCP to 8.54A(2009/06/05)
			Change PR251 13.7k to 18k	Set 1.5V OCP to 9.98A(2009/06/05)
EVT		P42-PWR_+VTTP	Change PR99 5.9k to 2.43k	Set VTT OCP to 19.7A(2009/06/05)
DVT		P46-PWR_GM VGA_CORE	Change PC218 15P to 100P	Correct link error (2009/07/07)
DVT		P46-PWR_GM VGA_CORE	Change PC211 SE080224K80 to SE000005Z80	Change voltage rating 10V to 25V (2009/07/07)
DVT		P45-PWR_CPU_CORE	PC133, PC134 SE083224Z80 to SE124224K80	PC133, PC134 tolerance Y5V to X5R(2009/0/07)
DVT		P49-PWR_+VTTP	Change PR99 2.43k to 4.99k	Set OCP(2009/07/07)
DVT		P43-PWR_1.05VSP/1.5VP	Change PC79, PC194 SE00000MAN0 to SE107475K80	Change part number(2009/07/07)
DVT		P41-PWR_3VALWP/5VALWP	Add PC87 1U_0402_6.3V6K	Avoid pre-charge can not finish(2009/07/07)
DVT		P41-PWR_3VALWP/5VALWP	Add PC45 0.22U to 1U	Prevent +3VALW/+5VALW can't boot up (2009/07/07)
DVT		P45-PWR_CPU_CORE	Change PR229~PR245 and PR160 10k to 1k	Change VID, PSI# and DPRSLPVR select resistor from 10k to 1k (2009/07/17)
DVT		P45-PWR_CPU_CORE	Change PR157 10k to 1.91k	Change PGOOD pull high resistor 10k to 1.91k(2009/07/17)
DVT		P45-PWR_CPU_CORE	Remove PH3, PC124, PR167	Modify circuit for CPU_CORE(2009/07/17)
			Change PC133, PC134 pin 2 from GND to VSUM-	
			Change PR152, PR192 0402 size to 0805 size	
DVT		P46-PWR_GM VGA_CORE	Remove PR281, PC227	Modify circuit for GFX (2009/07/17)
DVT		P39-PWR_BATTERY CONN / OTP	Change +3VLP to +3VALWP	Remove +3VLP power rail (2009/07/17)
DVT		P42-PWR_+VTTP	Remove PR290, PR291, PR292, PR293, PR293,PR105, PC228, PC229, PQ53, PQ54	Remove VTT voltage switch circuit (2009/07/17)
DVT		P47-PWR_CHARGER	Change PC84 0.1U	For EMI solution(2009/07/23)
DVT		P47-PWR_CHARGER	Add PC144 0.1U,Add PC182 470P	For EMI solution(2009/07/23)
DVT		P47-PWR_CHARGER	Add PC144 0.1U,Add PC182 470P	For EMI solution(2009/07/23)
DVT		P42-PWR_+VTTP	Add PC230 0.1U	For EMI solution(2009/07/23)
DVT		P42-PWR_+VTTP	Add PR100 4.7U, PC70 680P	Add snubber(2009/07/23)
DVT		P42-PWR_+VTTP	Change PR95 0 ohm to 2.2 ohm	Add boot strap resistor (2009/07/23)
DVT		P42-PWR_+VTTP	Change PR94 3.4k to 1.5k, PR101 1k to 3k	For HW solution(S3 power reduction)(2009/07/23)
DVT		P42-PWR_+VTTP	Add PJ14	For power test(2009/07/23)
DVT		P52-PWR_0.75VSP/1.1VSP	Add 0.75VR_EN# control signal	For HW solution(S3 power reduction) (2009/07/23)
DVT		P45-PWR_CPU_CORE	Change PR148, PR188 0 to 2.2 ohm	Add boot strap resistor(2009/07/23)
DVT		P45-PWR_CPU_CORE	Add PR151, PR191 4.7 ohm, PC118, PC149 680P	Add snubber(2009/07/23)
DVT		P45-PWR_CPU_CORE	Add PC114, PC138 470P	For EMI solution(2009/07/23)
DVT		P45-PWR_CPU_CORE	Add PC120 0.1U	For EMI solution(2009/07/23)
DVT		P45-PWR_CPU_CORE	Add PC121 1U	For EMI solution(2009/07/23)
DVT		P46-PWR_GM VGA_CORE	Change PL18 SH00000AC00 to SH05056BM00	Change current rating to 25A(2009/07/27)
DVT		P47-PWR_CHARGER	Change PQ9 FDS4435 to AO4407A	For design change(2009/07/27)
DVT		P45-PWR_CPU_CORE	Remove PQ40, PQ47	For design change(2009/07/28)
DVT		P52-PWR_0.75VSP/1.1VSP	Change PC101 10U to 4.7U	For design change(2009/07/28)
DVT		P52-PWR_0.75VSP/1.1VSP	Change PC106 SE076104KM8 to SE076104K80	Change to COMPAL PN(2009/08/03)
DVT		P45-PWR_CPU_CORE	Change PC151 SE076104KM8 to SE076104K80	Change to COMPAL PN(2009/08/03)
DVT			Change PC53, PC54, PC78, PC193 SF22001M200 to SF000001H00	SF22001M200 is forbids to use (2009/08/03)
DVT		P45-PWR_CPU_CORE	Change PR178 2.43k to 2.26k	Change Rdroop for load line (2009/08/03)
DVT		P42-PWR_+VTTP	Change PU7 ISL6268 to APW7138	For cost down (2009/08/03)
			Remove PC71 0.01U	For APW7138 solution (2009/08/03)
DVT		P39-PWR_BATTERY CONN / OTP	Change PR33 13.7k to 12.4k	Set OTP (2009/08/03)
			Change PR37 15.4k to 15.8k	
DVT		P46-PWR_GM VGA_CORE	Change PC223 SE071150J1M to SE071150J80	Change PC223 to COMPAL PN (2009/08/03)
DVT		P47-PWR_CHARGER	Add PR220 4.7 ohm, PC169 680P	Add charger snubber(RF solution) (2009/08/03)
DVT		P45-PWR_CPU_CORE	Add PC113 2200P	RF solution (2009/08/03)
PVT		P47-PWR_CHARGER	Change PR70 24k to 75k	Set 65W CP (2009/09/04)
PVT		P42-PWR_+VTTP	Change PL7 0.47U to 1U	Design change (2009/09/04)
PVT		P45-PWR_CPU_CORE	Change PR178 2.26k to 2.37k	Change Rdrrop for load line (2009/09/04)
PVT		P45-PWR_CPU_CORE	Add PC150, PC152 0.1U (SE042104K80)	For EMI soltion (2009/09/14)
PVT		P45-PWR_CPU_CORE	Add PC121 1U	For EMI soltion (2009/09/14)
PVT		P42-PWR_+VTTP	Add PC85, PC186 0.1U	For EMI soltion (2009/09/14)
PVT		P42-PWR_+VTTP	Remove PC66, PC68 10U	Design change (2009/09/14)
PVT		P47-PWR_CHARGER	Change PR64 PN SD013220B80 to SD014220B80	Use same PN (2009/09/14)
PVT		P42-PWR_+VTTP	Change PR95 PN SD013220B80 to SD014220B80	Use same PN (2009/09/14)
PVT		P43-PWR_1.05VSP/1.5VP	Change PR113, PR248 0 ohm to 2.2 ohm	Add boot trap resistor(2009/09/14)
			Add PR114, PR249 4.7 ohm, PC80, PC195 680P	Add snubberr(2009/09/14)
PVT		P45-PWR_CPU_CORE	Change PR148, PR188 PN to SD014220B80	Use same PN(2009/09/14)

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
PVT		P42-PWR_1.05VSP/1.5VP	Change PR117 8.25k to 4.02k	Avoid FB trace noise (2009/09/18)
			Change PR118, PR252, PR253 20.5k to 10k	
PREMP		P45-PWR_DCIN/DECTOR	Change PC7 SE041224K80 to SE000005Z80	Change CAP size from 1206 to 0603 (2009/10/09)
PREMP		P46-PWR_BATTERY CONN / OTP	Change PR44 13.7k to 12.1k	Modify OTP setting (2009/10/09)
PREMP		P44-PWR_CPU_CORE	Change PR178 2.37k to 2.43k	Change CPU_CORE OCP 52A to 57A and modify load line (2009/10/09)
			Change PR195 1.1k to 1.2k	
PREMP		P44-PWR_CPU_CORE	Change PC121 SE000009R80 to SE000006900	Change HW part to power part PN (2009/10/09)
PREMP		P44-PWR_CPU_CORE	Change PL12, PL14 SH000005680 to SH12036BM00	Use 5% tolerance DCR choke (2009/10/09)
PREMP		P41-PWR_+VTTP	Change PR94 1.5k to 39.2k	Adjust VTTPWROK voltage 3.3V to 1.05V (2009/10/27)
			Change PR101 3k to 10.5k	
PREMP		P42-PWR_1.05VSP/1.5VP	Remove 1.05V components	Cost down (2009/11/03)
MP		P41-PWR_+VTTP	Change PR94 39.2k to 6.81k	Modify resistor for VTTPWROK voltage (2009/11/26)
			Change PR101 10.5k to 2k	

Security Classification	Compal Secret Data		
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