RS780Q-LM2 VER:1.01

SCHEMATICS TABLE:

Job	Signature	Date
Schematics Designer	Dennis	01/09/'09
Layout	Joyce	01/09/'09
Approval		

PCB STACK:
L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

Elitegroup Computer Systems

Title: Cover Page

Size: Custom | Document Number: RS780Q-LM2 | Rev: 1.01

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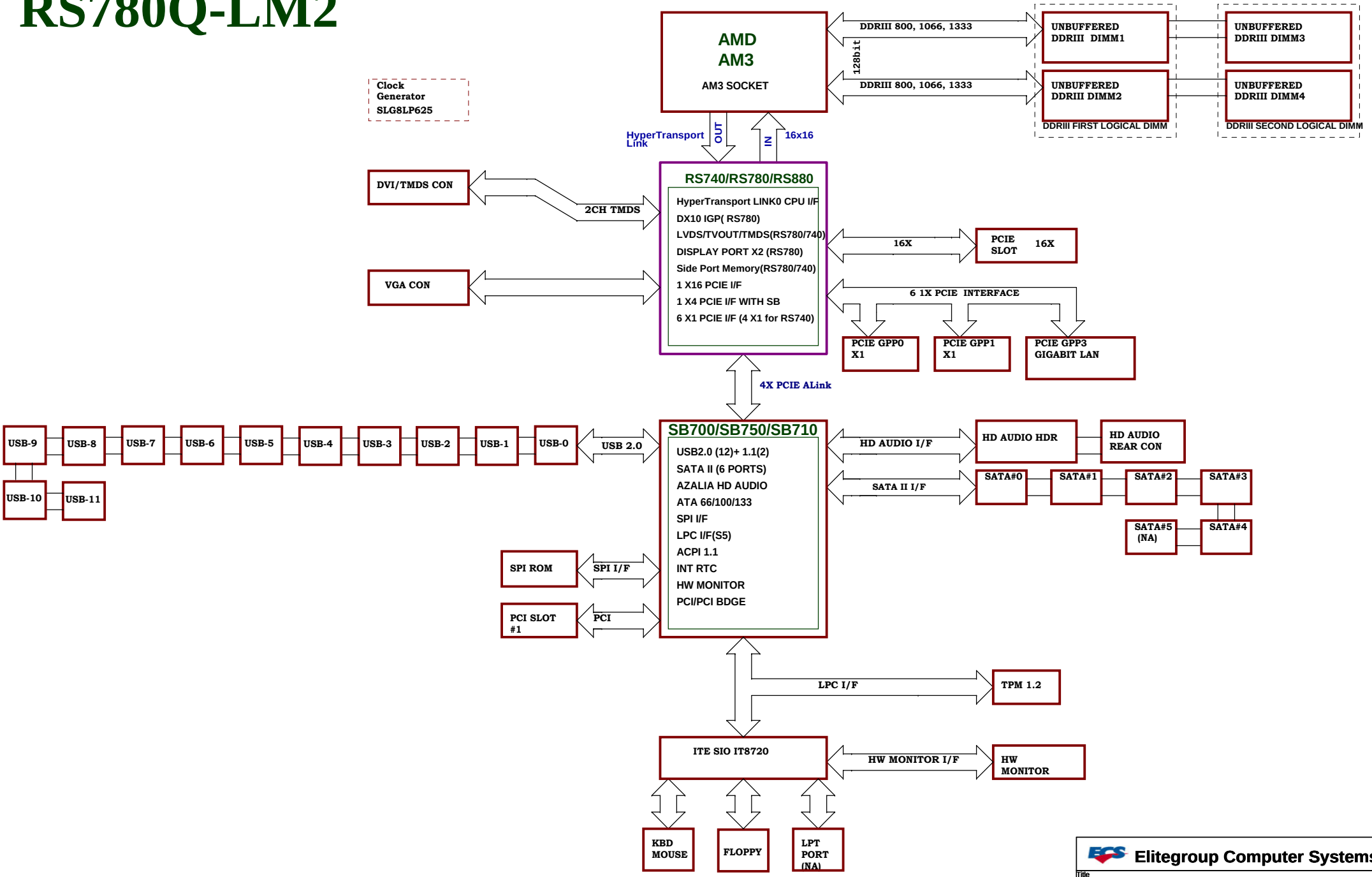
RS780Q-LM2



Elitegroup Computer Systems

Title	BLOCK DIAGRAM	
Size: Custom	Document Number: RS780Q-LM2	Rev: 1.01
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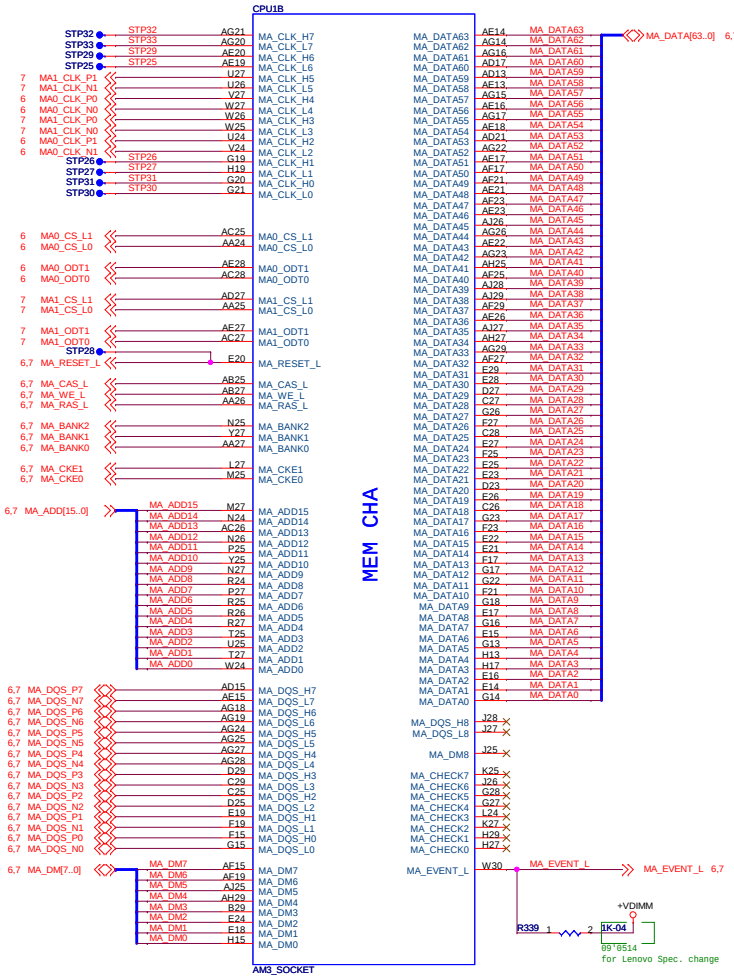
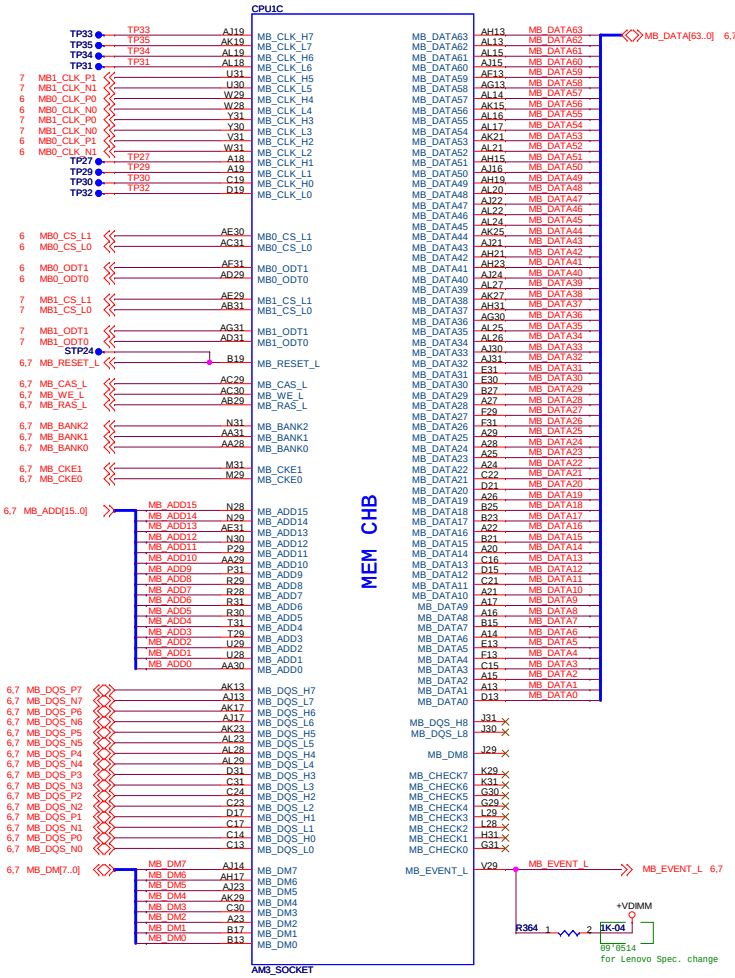
CPU Memory

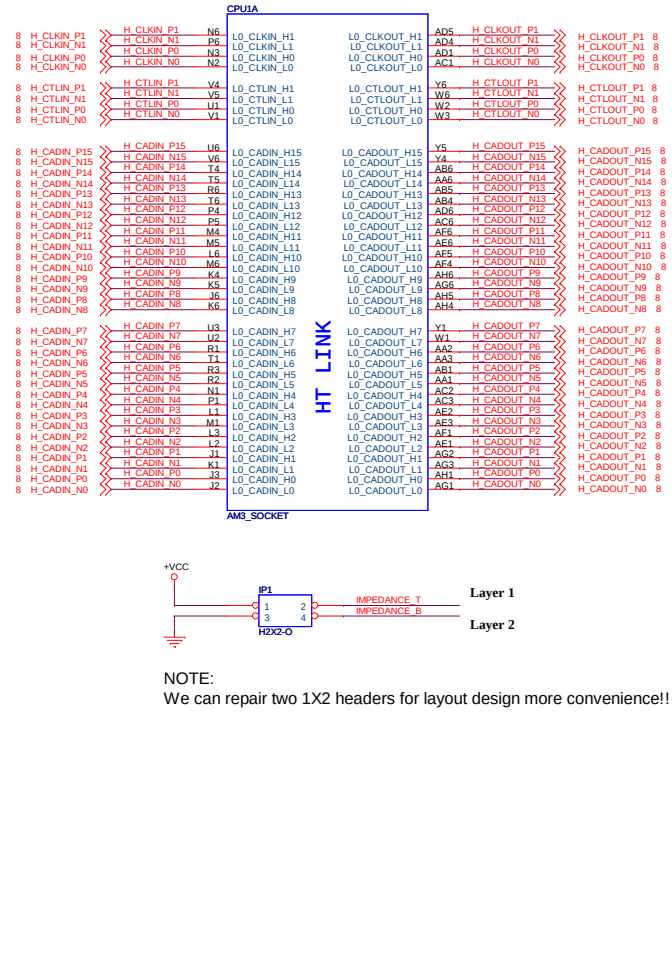
DDR3 Memory Interface A



DDR3 Memory Interface B



HT LINK



NOTE:
We can repair two 1X2 headers for layout design more convenience!!

Elitegroup Computer Systems			
Title: HT,CPU MEMORY			
Size: Custom	Document Number: RS780Q-LM2		Rev: 1.01
Date: Monday, July 20, 2009	Sheet 3 of 37		

CPU Control and Miscellaneous

VDDA_2P5V for CPU PLL

VDDA_2P5V@250mA

Note: Update with new clock termination scheme, if necessary.

FDV301N-S
03-050-530106

080814 AMD recommend.

080825 lenovo thermal SPEC.

Place within 500 mils of the CPU socket.

Use buffered reset

HDT Header

AM3 Top View

Elitegroup Computer Systems	
Title	CPU CONTROL & MISC
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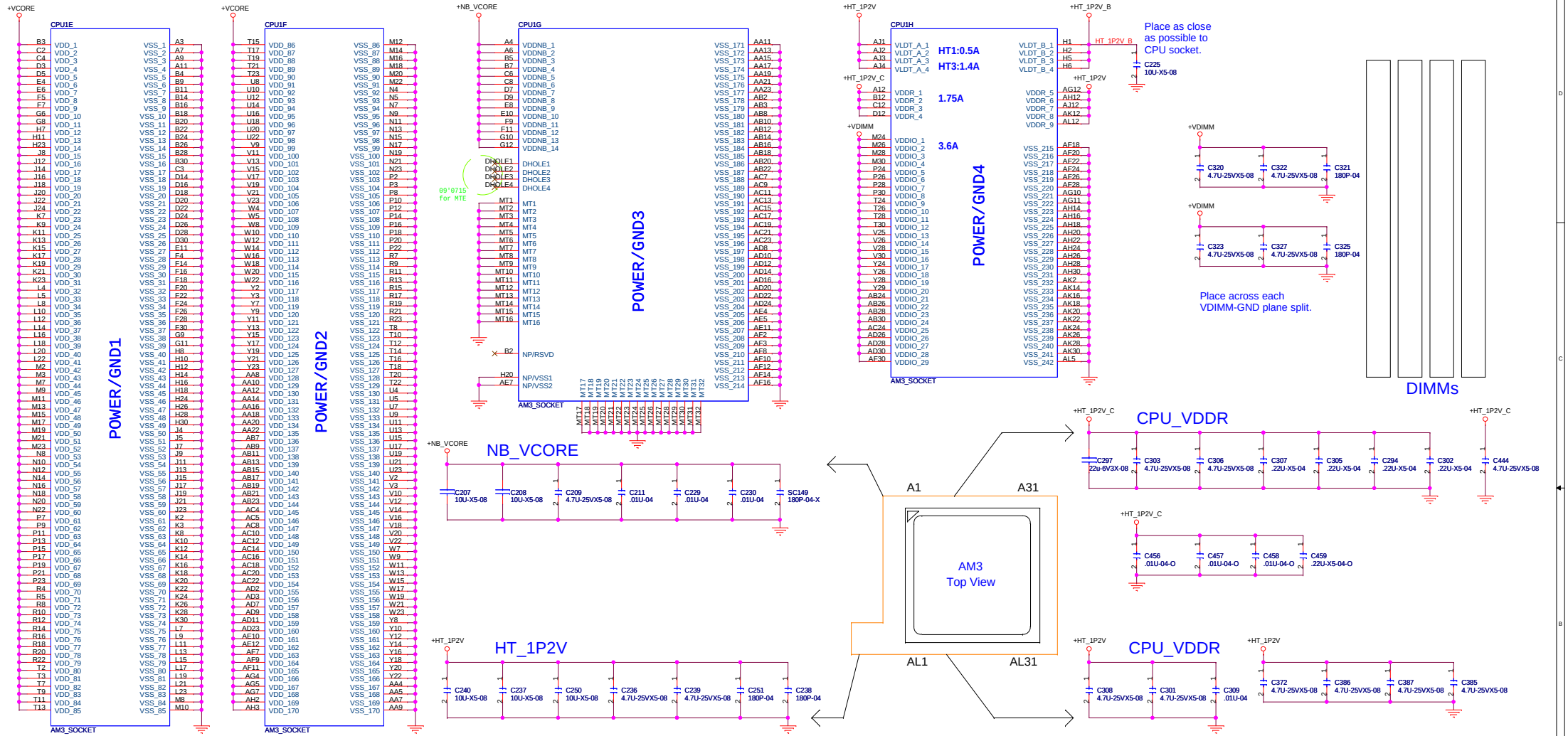
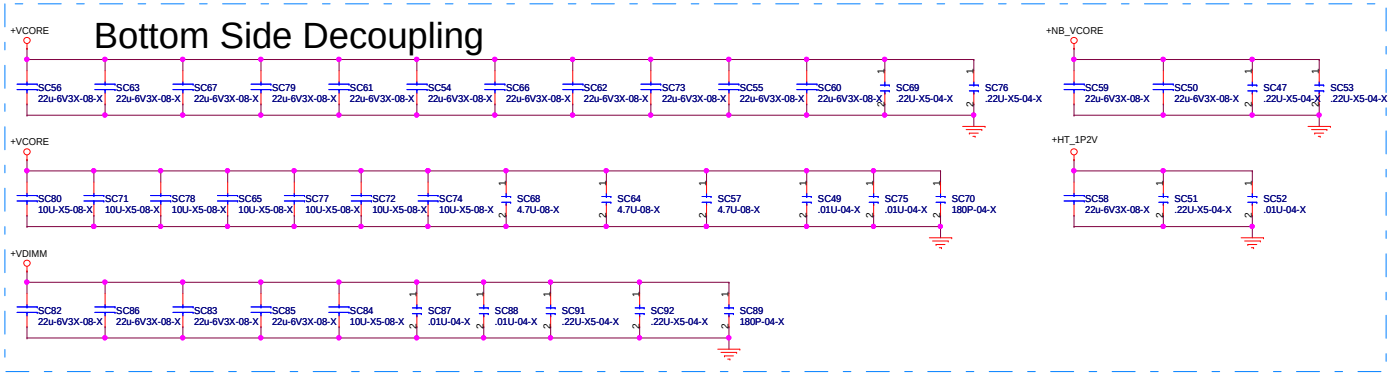
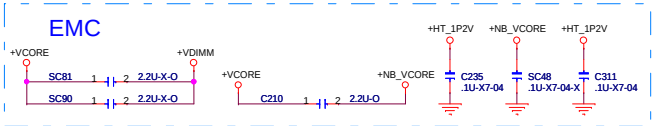
Processor Power and Ground



Bottom Side Decoupling



EMC



Elitegroup Computer Systems	
Title	CPU PWR & GND
Size: Custom	Document Number: RS780Q-LM2
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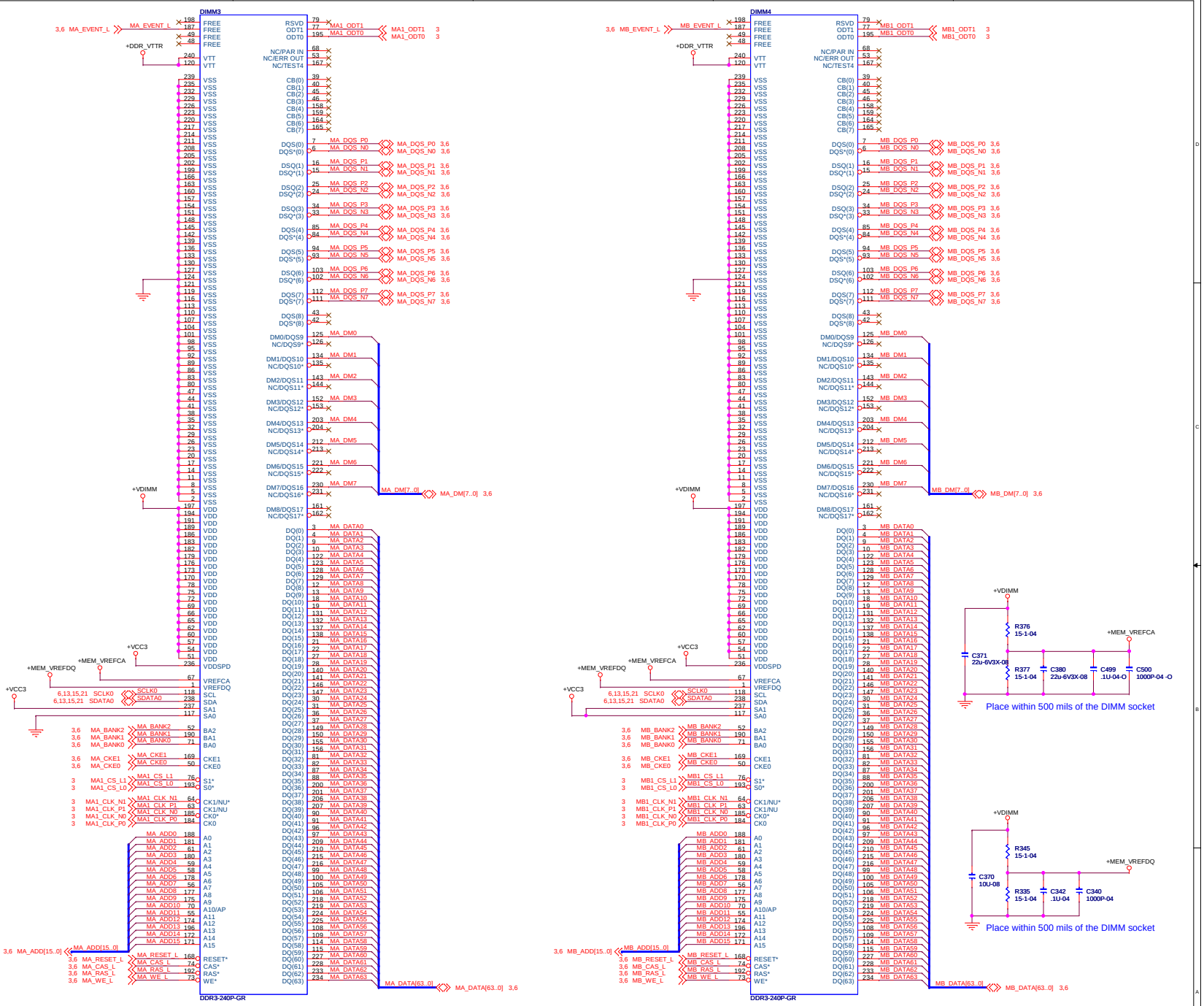
Date: Monday, July 20, 2009	Sheet 5 of 37

Elitegroup Computer Systems

Title: First Logic DDR3 DIMM

Size	Document Number	Rev
Custom	RS780Q-LM2	1.01

Date: Monday, July 20, 2009 Sheet 6 of 37

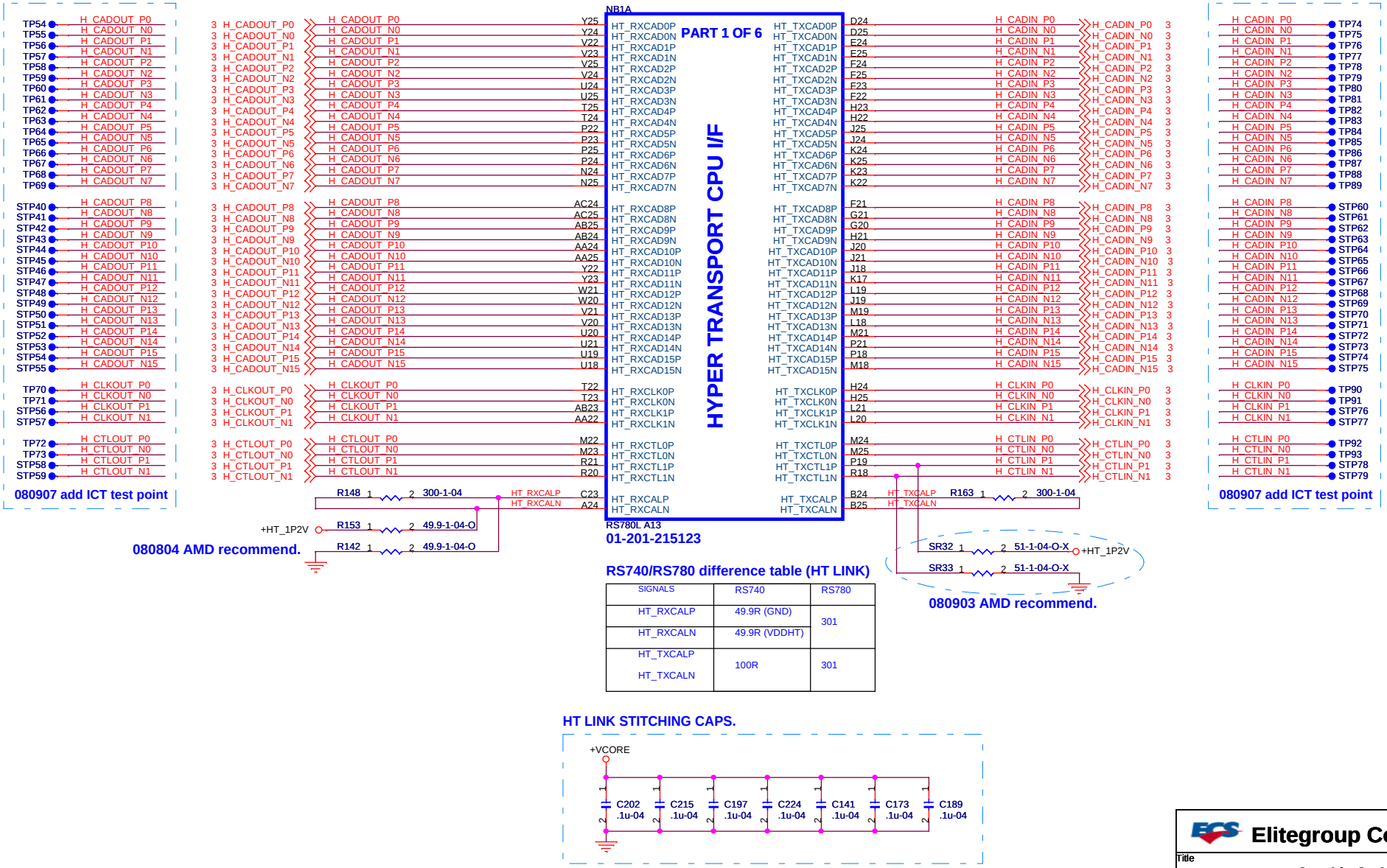


Elitegroup Computer Systems

Title: Second Logic DDR3 DIMM

Size	Document Number	Rev
Custom	RS780Q-LM2	1.01

Date: Monday, July 20, 2009 Sheet 7 of 37



RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RS780
HT_RXCALP	49.9R (GND)	301
HT_RXCALN	49.9R (VDDHT)	
HT_TXCALP HT_TXCALN	100R	301

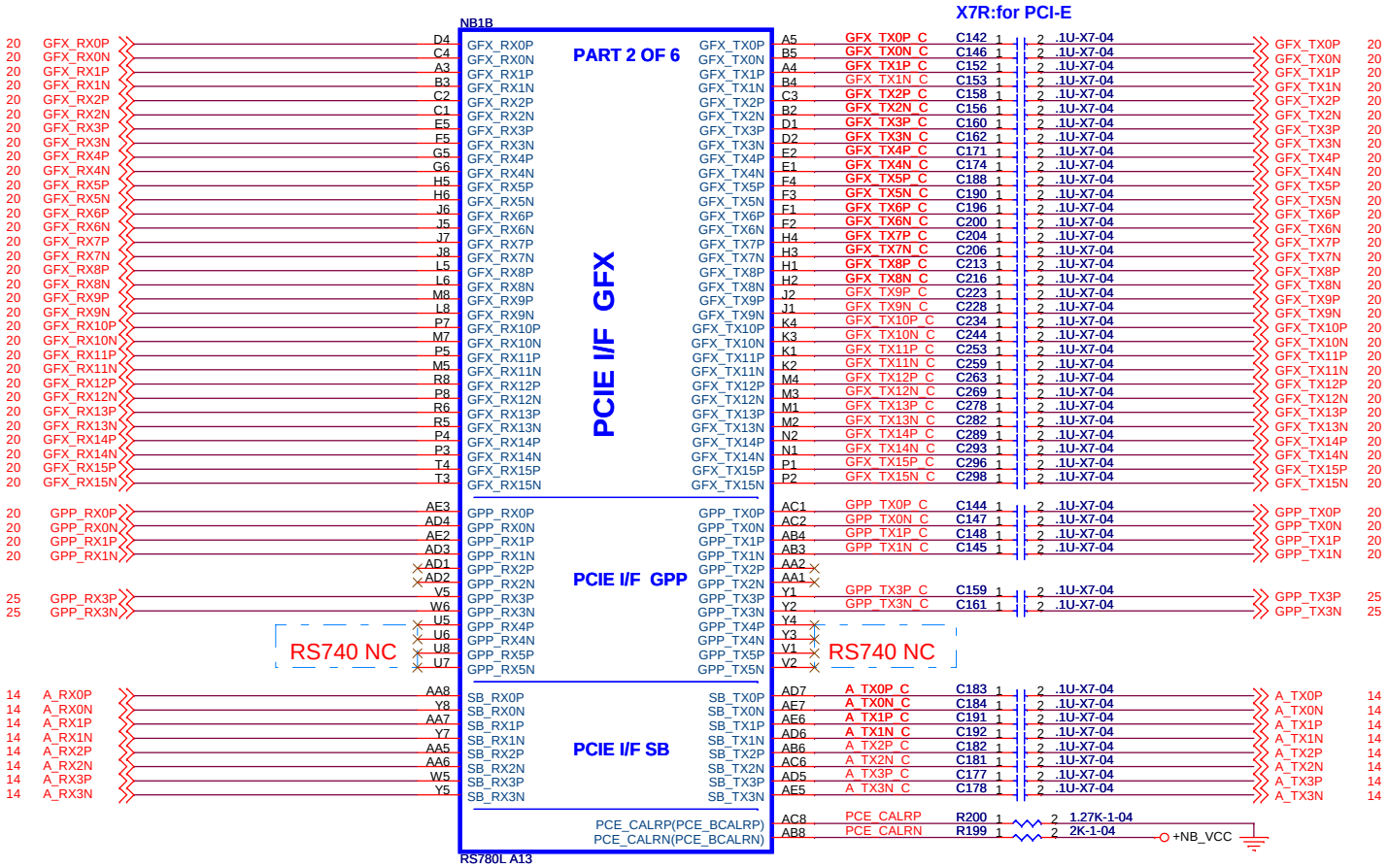
HT LINK STITCHING CAPS.

Elitegroup Computer Systems

Title: RS740/RS780-HT LINK I/F

Size: Custom | Document Number: RS780Q-LM2 | Rev: 1.01

Date: Monday, July 20, 2009 | Sheet 8 of 37



Elitegroup Computer Systems	
Title	RS740/RS780-PCIE I/F
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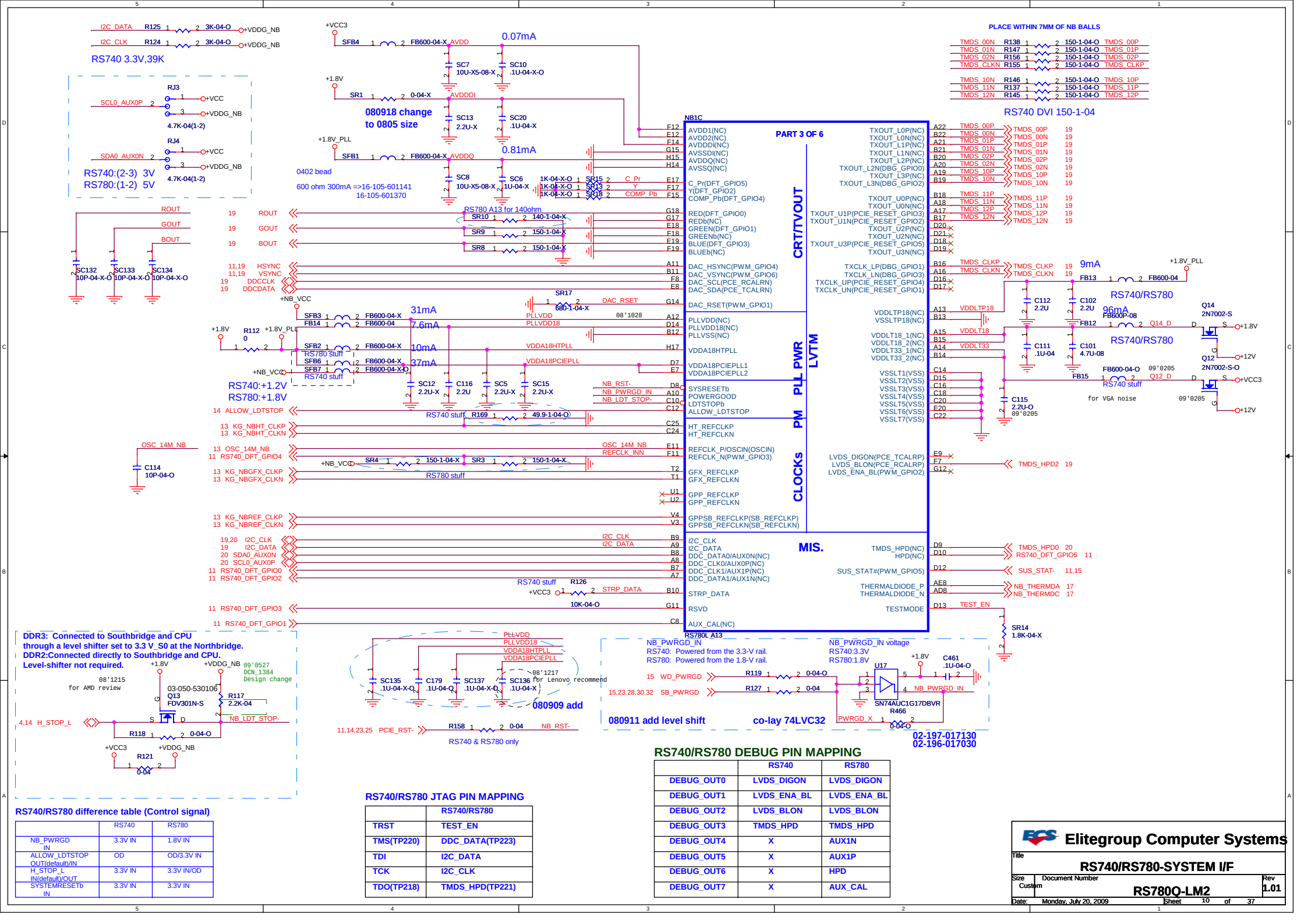
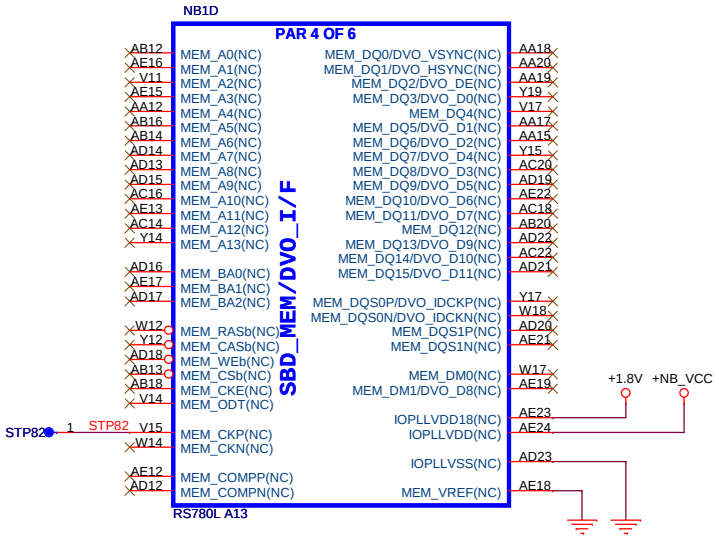


	RS740	RS780
NB_PWRGD	3.3V IN	1.8V IN
ALLOW_LDTSTOP	OD	OD/3.3V IN
H_STOP_L	3.3V IN	3.3V IN/OD
SYSTEMRESETb	3.3V IN	3.3V IN

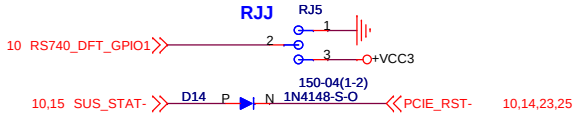
	RS740/RS780
TRST	TEST_EN
TMS(TP220)	DDC_DATA(TP223)
TDI	I2C_DATA
TCK	I2C_CLK
TDO(TP218)	TMDS_HPD(TP221)

	RS740	RS780
DEBUG_OUT0	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	X	AUX1N
DEBUG_OUT5	X	AUX1P
DEBUG_OUT6	X	HPD
DEBUG_OUT7	X	AUX_CAL



RS740/RS780 STRAPS

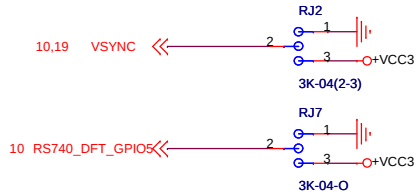
Note: for RS780, change RJJ to 150R as AUX_CAL,place close to pin C8



Note:RS740_DFT_GPIO1:Made provision for external pull-down which is not installed by default. Northbridge has an internal pull-up for bypassing EEPROM strapping and using default values for RS740

RS740/RS780: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740: pin DFT_GPIO1
RS780: pin SUS_STAT#



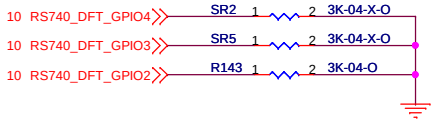
RS740/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable (RS740/RS780); Disable(RX780)
RS740: pin DFT_GPIO5
RS780: pin VSYNC

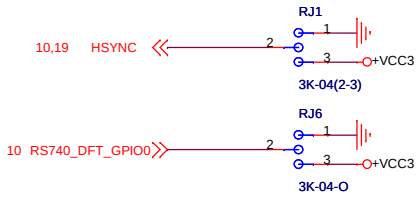
RS780: STRAP_PCIE_GPP_CFG[2:0] (configure thru register setting)

1-1-1-1-1-1 Mode L default
1-1-1-1-1-1 Mode L
2-0-2-0-2-0 Mode C2
2-0-2-0-1-1 Mode K
2-0-1-1-1-1 Mode E
1-1-1-1-1-1 Mode L
4-0-0-0-1-1 Mode C
4-0-0-0-2-0 Mode B

RS740: STRAP_PCIE_SB/GPP_CFG[2:0] (Pins: RS740_DFT_GPIO[4:2])



These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E) default
110: 4-0-0-0-0 Config A
101: 4-4-0-0-0 Config B
100: 4-2-2-0-0 Config C
011: 4-2-1-1-0 Config D
010: 4-1-1-1-1 Config E
others: register defined (default to Config E)



RS740/RS780: SIDE-PORT MEMORY ENABLE

Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740: pin DFT_GPIO0
RS780: pin HSYNC

RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

Enables Test debug bus using PCIE bus
1. Disable (can be enabled thru nbcfg register)
0 : Enable
RS780: configurable thru register setting only
RS740: Not supported

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Title: RS740/RS780-SPMEM/STRAPS

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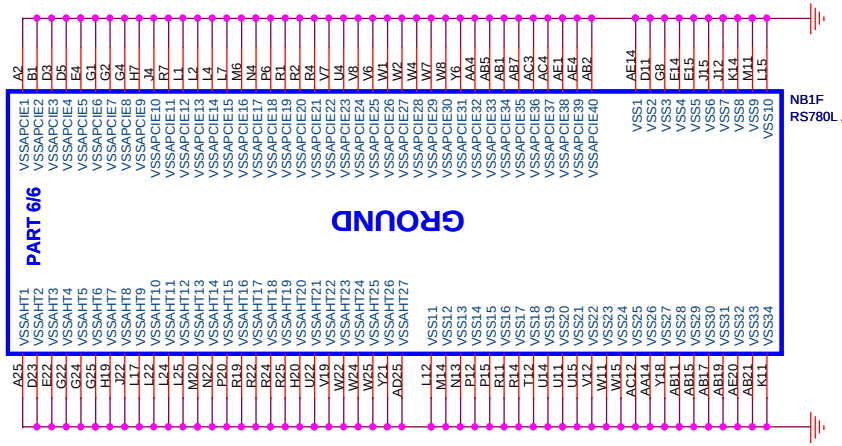
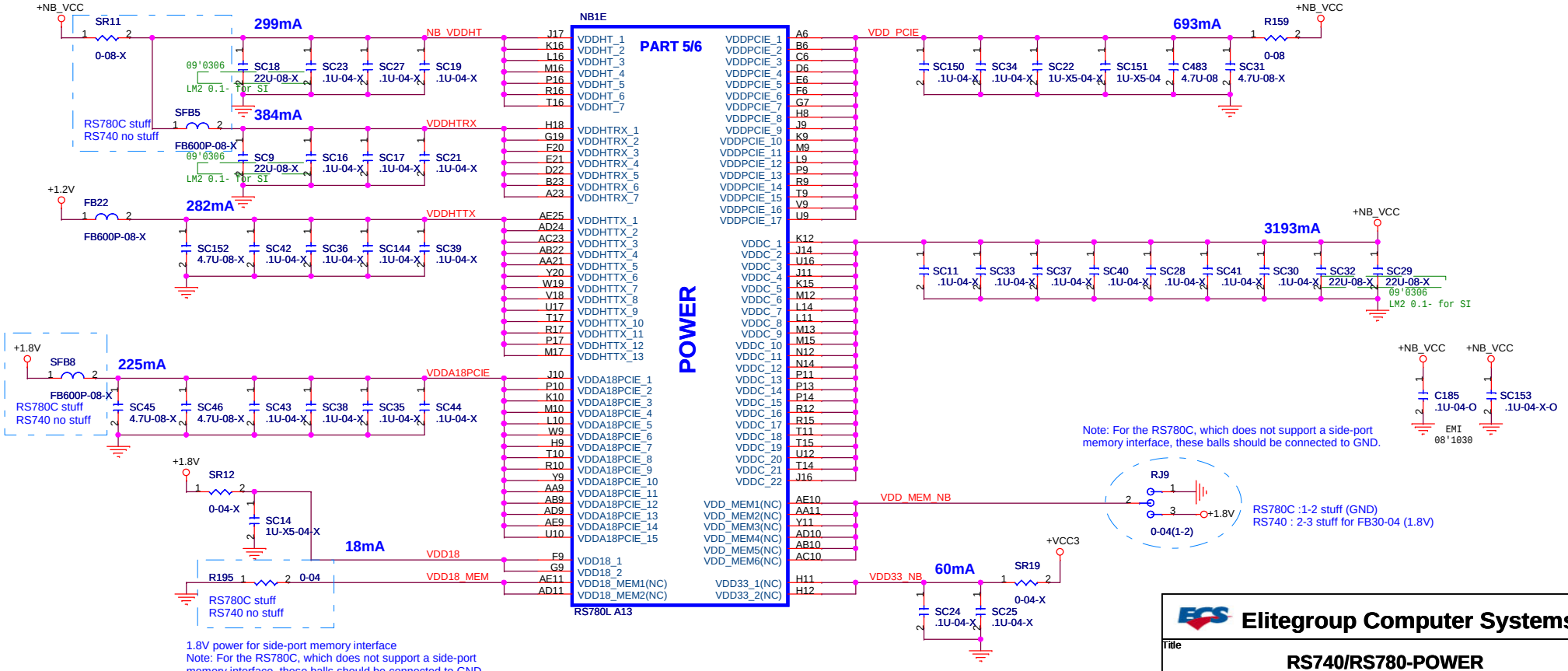
RS740/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RS780	PIN NAME	RS740	RS780
VDDHT	NC	+1.1V	IOPLLVDD	+1.2V	+1.1V
VDDHTRX	NC	+1.1V	AVDD	+3.3V	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	+1.8V	+1.8V
VDDA18PCIE	NC	+1.8V	AVDDQ	+1.8V	+1.8V
VDD18	+1.8V	+1.8V	PLLVDD	+1.2V	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	+1.8V	+1.8V
VDDPCIE	+1.2V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V
VDDC	+1.2V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	+1.8V	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	+1.8V
VDD33	+3.3V	+3.3V	VDDLT18	+1.8V	+1.8V
IOPLLVDD18	+1.8V	+1.8V	VDDLT33	+3.3V	NC





Elitegroup Computer Systems			
Title: RS740/RS780-POWER			
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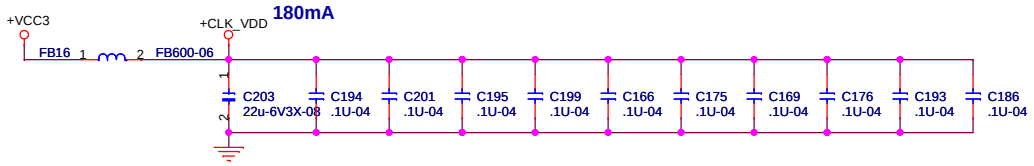
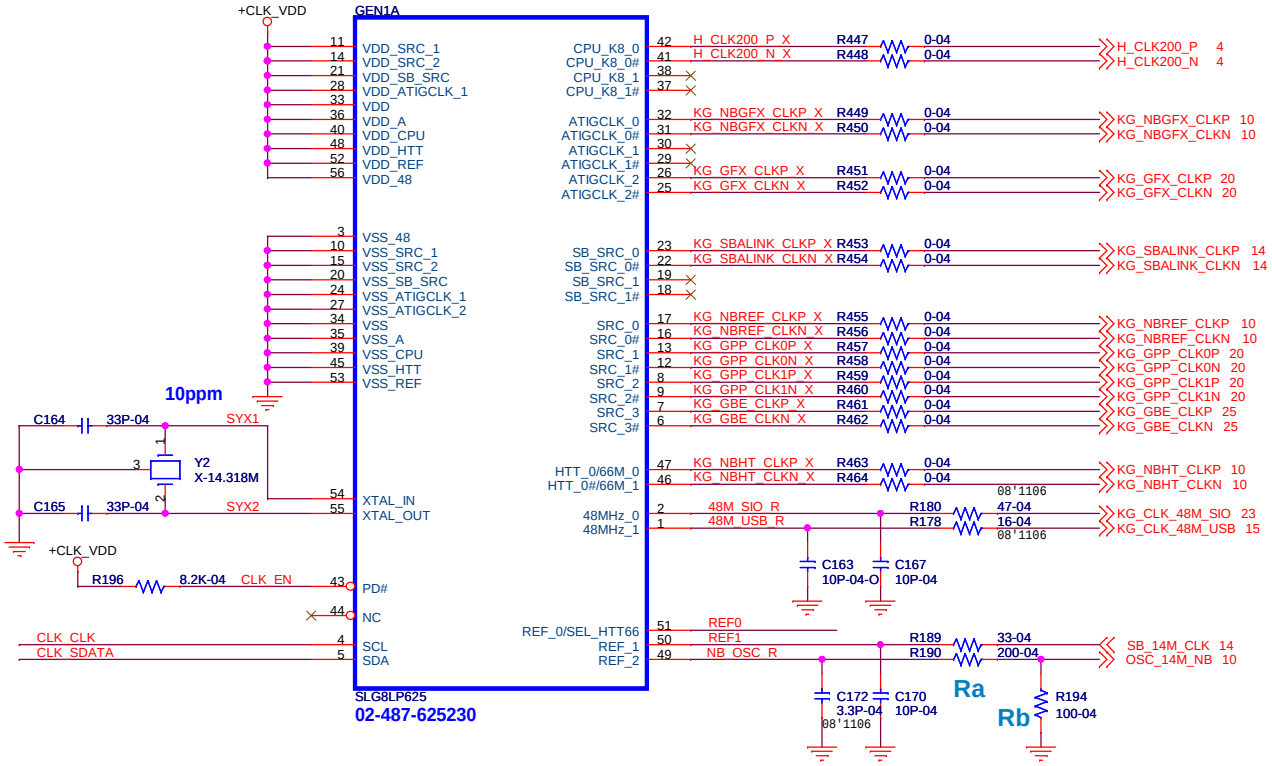




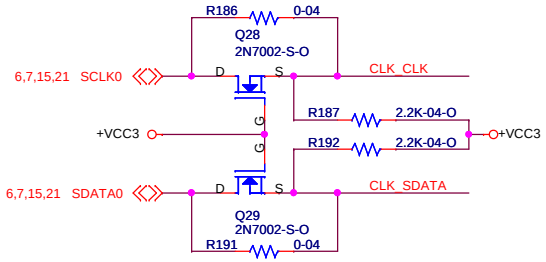
Clock chip has internal serial terminations for differencial pairs.

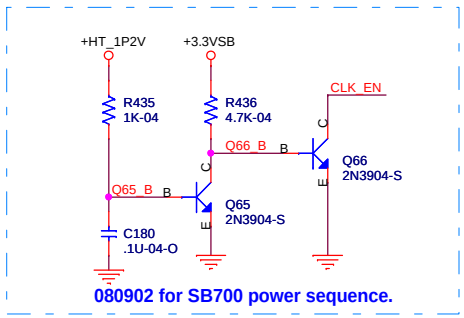
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

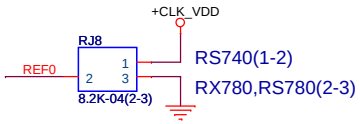
* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

	OSC_14M_NB	Ra	Rb
RS740	3.3V	33 ohm	X
RX780	1.8V	33 ohm	43 ohm
RS780	1.1V	200 ohm	100 ohm





080902 for SB700 power sequence.



REF0 / SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock

* default

Elitegroup Computer Systems

Title: CLOCK GENERATOR SLG8LP625

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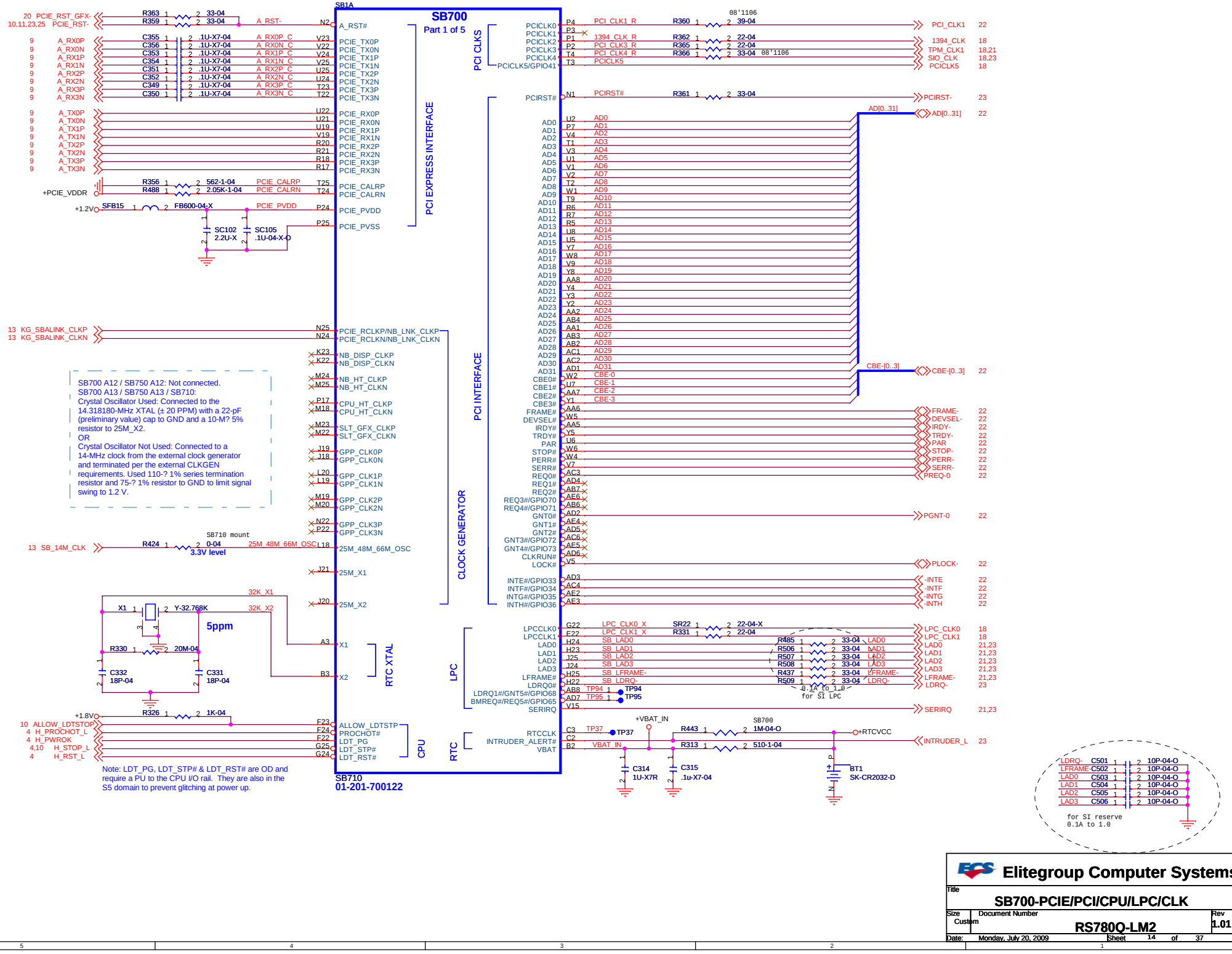
SB1A
SB700
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
SB710
01-201-700122
SB710 A12 / SB750 A12: Not connected.
SB700 A13 / SB750 A13 / SB710:
Crystal Oscillator Used: Connected to the 14.318180-MHz XTAL (± 20 PPM) with a 22-pF (preliminary value) cap to GND and a 10-M? 5% resistor to 25M_X2.
OR
Crystal Oscillator Not Used: Connected to a 14-MHz clock from the external clock generator and terminated per the external CLKGEN requirements. Used 110-? 1% series termination resistor and 75-? 1% resistor to GND to limit signal swing to 1.2 V.
Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.
5ppm
for SI LPC
for SI reserve
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SB700-PCIE/PCI/CPU/LPC/CLK
RS780Q-LM2
1.01
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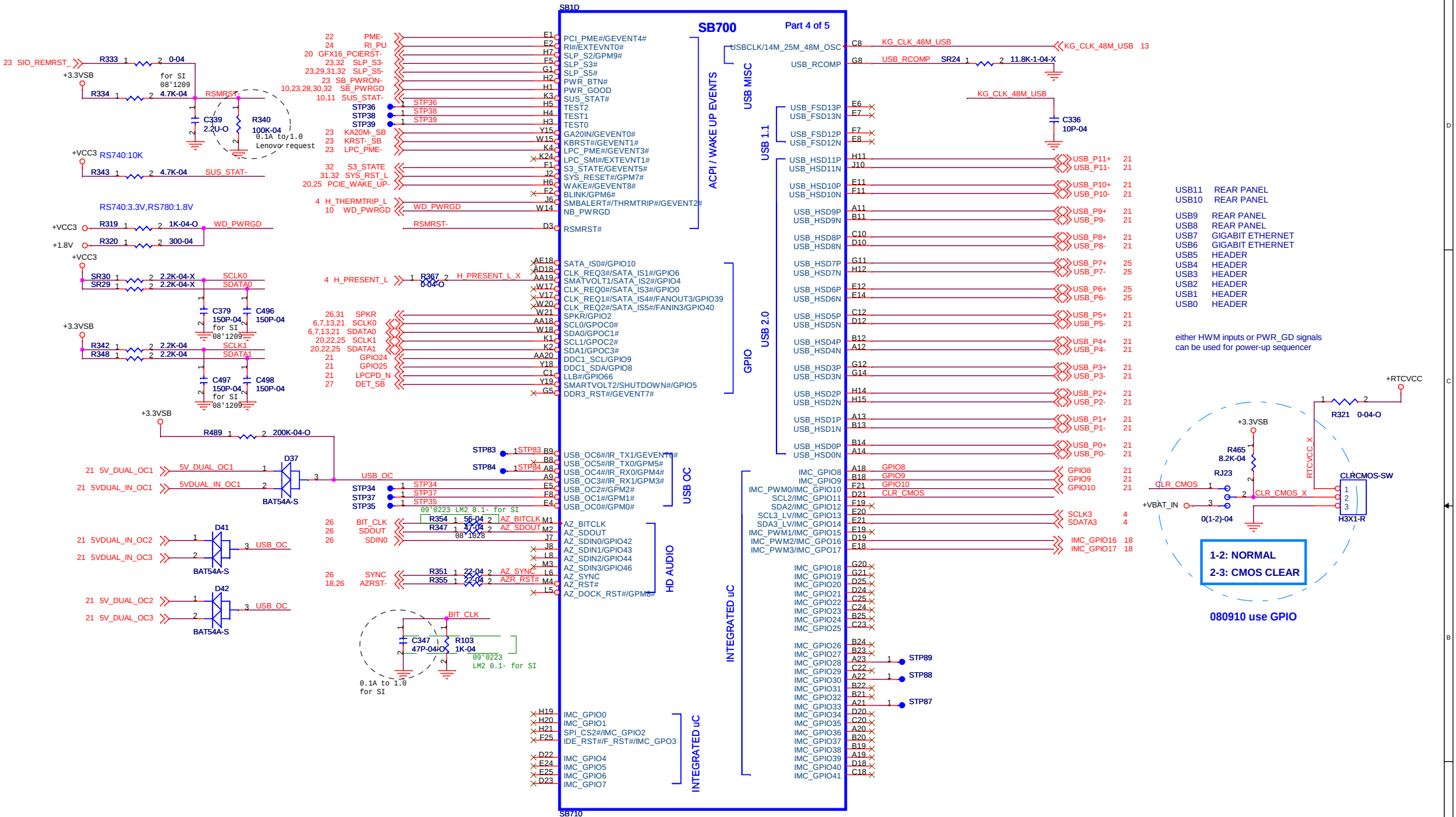

Elitegroup Computer Systems	
Title	SB700-ACPI/GPIO/USB/AUDIO
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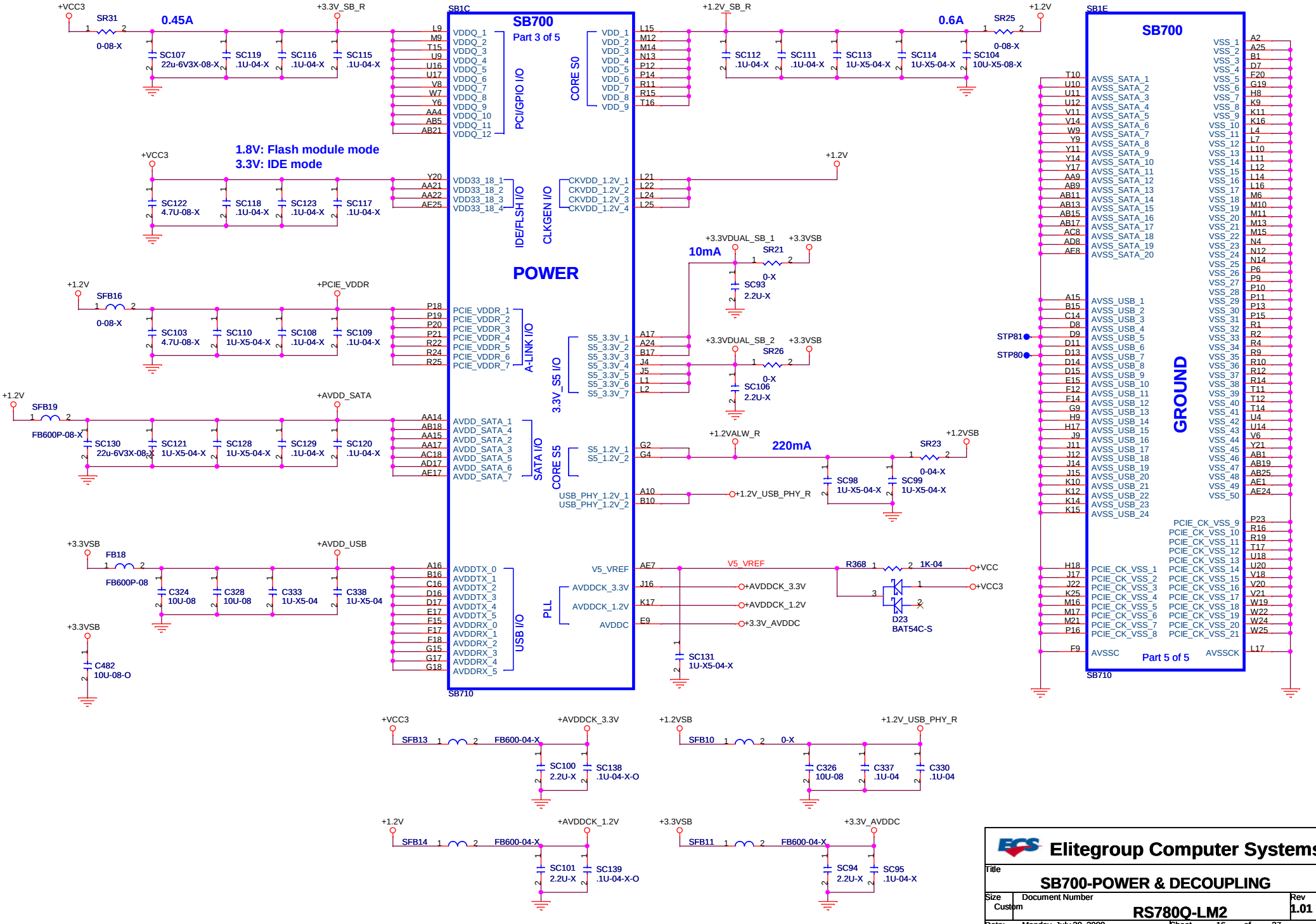
SB1C
SB700
Part 3 of 5
POWER
SB710
SB1E
SB700
GROUND
Part 5 of 5
SB710
0.45A
0.6A
1.8V: Flash module mode
3.3V: IDE mode
10mA
220mA
+VCC3
+3.3V_SB_R
+1.2V_SB_R
+1.2V
+3.3VDUAL_SB_1
+3.3VDUAL_SB_2
+3.3VSB
+1.2VALW_R
+1.2VSB
+PCIE_VDDR
+AVDD_SATA
+AVDD_USB
+3.3VSB
+VCC3
+AVDDCK_3.3V
+1.2VSB
+1.2V_USB_PHY_R
+1.2V
+AVDDCK_1.2V
+3.3VSB
+3.3V_AVDDC
PCI/GPIO I/O
CORE S0
IDE/FLSH I/O
CLKGEN I/O
A-LINK I/O
3.3V_S5 I/O
SATA I/O
CORE S5
USB I/O
PLL
V5_VREF
+1.2V_USB_PHY_R
+AVDDCK_3.3V
+AVDDCK_1.2V
+3.3V_AVDDC
+VCC
+VCC3
SR31
SR25
SR21
SR26
SR23
SFB16
SFB19
FB18
SFB13
SFB10
SFB14
SFB11
R368
D23
BAT54C-S
STP81
STP80
Elitegroup Computer Systems
SB700-POWER & DECOUPLING
RS780Q-LM2
Custom
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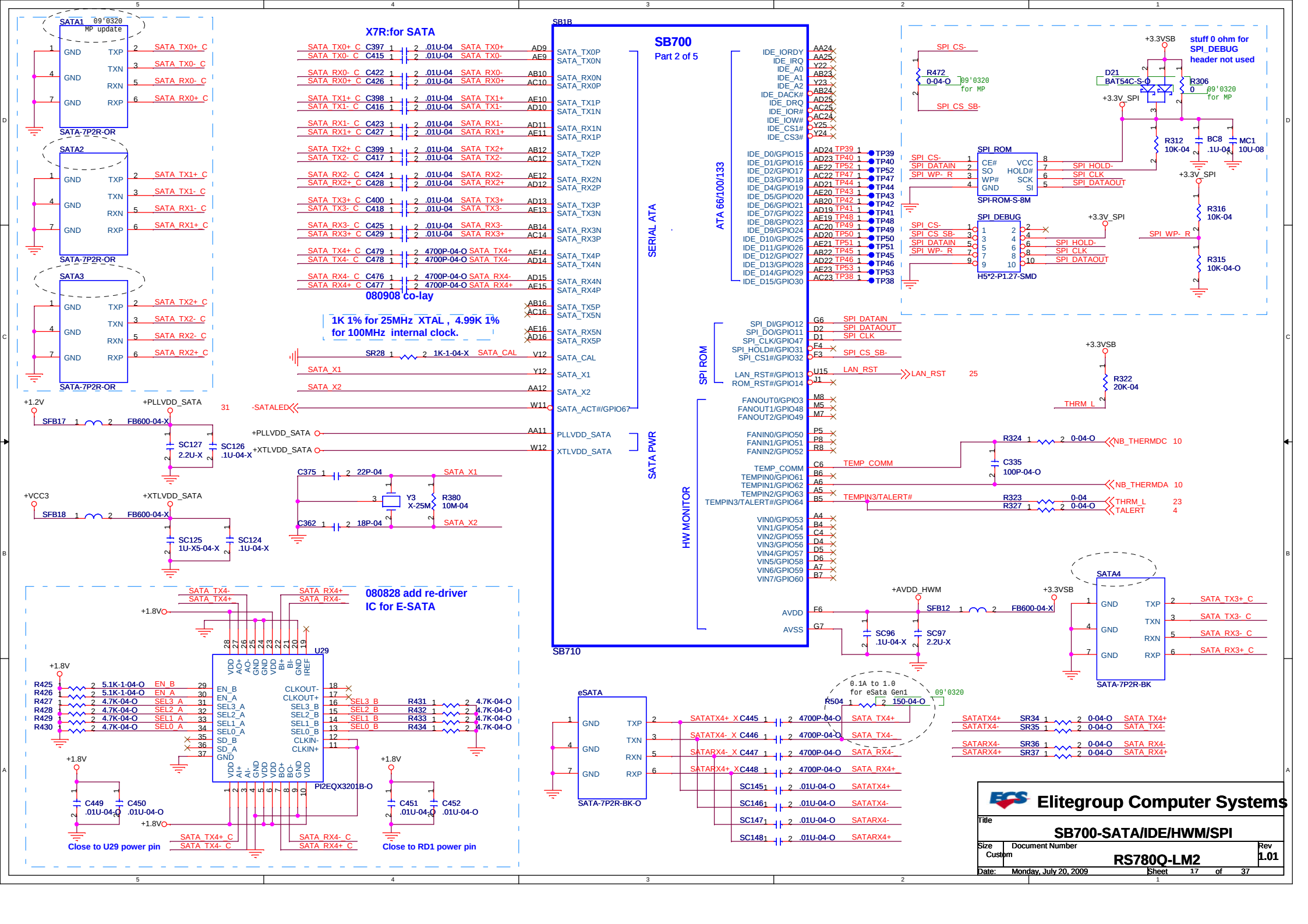
SATA1 09'0320 MP update
SATA-7P2R-OR
SATA2
SATA-7P2R-OR
SATA3
SATA-7P2R-OR
X7R:for SATA
080908 co-lay
1K 1% for 25MHz XTAL , 4.99K 1% for 100MHz internal clock.
SB1B
SB700
Part 2 of 5
SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR
SB710
stuff 0 ohm for SPI_DEBUG header not used
SPI_ROM
SPI-ROM-S-8M
SPI_DEBUG
H5*2-P1.27-SMD
080828 add re-driver IC for E-SATA
U29
PI2EQX3201B-O
Close to U29 power pin
Close to RD1 power pin
eSATA
SATA-7P2R-BK-O
SATA4
SATA-7P2R-BK
0.1A to 1.0 for eSata Gen1
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SB700-SATA/IDE/HWM/SPI
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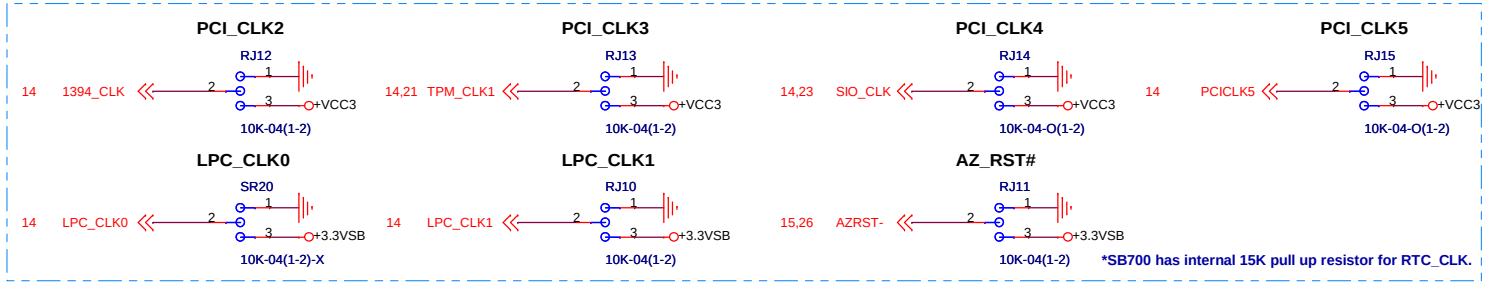

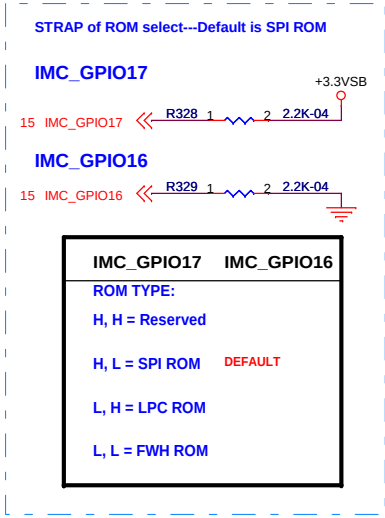

REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT

Elitegroup Computer Systems

Title: SB700-STRAPS

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RS780 A13 *:
- GREEN/BLUE: Connected to GND through two separate 150-? 1% resistors.
- RED: Connected to GND through two separate 140-? 1% resistors.

+12V
R52 10K-04
Q4 NDS351AN-S
Q4_G
09'0514 for Lenovo Spec. change
Q4_D
+VCC
R51 0-08-O
+VCC_DDC_VGA_DVI
FB9 FB600P-08
VCC_VGA
F2 FUSE-1.1A-18
C31 .1U-04
VGA1 CONN-15P3R-VGA

10 ROUT — L4 FB80-06-B — ROUT_X — L2 IND-68n — RED
10 GOUT — L5 FB80-06-B — GOUT_X — L3 IND-68n — GREEN
10 BOUT — L6 FB80-06-B — BOUT_X — L1 IND-68n — BLUE

RS780 A13
ER1 140-1-04
ER2 150-1-04
ER3 150-1-04
C36 22p-04
C37 22p-04
C38 22p-04
C18 18P-04
C28 18P-04
C27 18P-04

DDC1DATA — R12 33-04 SDAT
HSYNC1 — R11 27-04 H1SYNC
VSYNC1 — R25 27-04 V1SYNC
DDC1CLK — R24 33-04 SCLK

C17 100P-04
C16 1PVP-04
C23 1PVP-04
C25 100P-04

080915 reserve for VGA noise

U3 AZC099-04S
RED — BLUE
GREEN
BC6 .1U-04-O
Close to Connector

U2 AZC099-04S
HSYNC1 — DDC1DATA
VSYNC1 — DDC1CLK
BC7 .1U-04-O
Close to Connector

+VCC3
C471 10U-08-O
+VCC
C472 10U-08-O

+VCC3 +VCC_DDC_VGA_DVI
RS740:15K
RS780:5V,4.7K
R64 4.7K-04
10,20 I2C_CLK — I2C_CLK_DVI
Q7 2N7002-S-O
R71 0-04

+VCC3 +VCC_DDC_VGA_DVI
RS780:5V,4.7K
R63 4.7K-04
10 I2C_DATA — I2C_DATA_DVI
Q6 2N7002-S-O
R70 0-04

+VCC
U4 74HCT32-5-S
H1SYNC — HSYNC 10,11
C53 .1U-04-O
R18 0-04-O
09'0306 LM2 0.1- for SI

+VCC
U7 74HCT32-5-S
V1SYNC — VSYNC 10,11
C52 .1U-04-O
R58 0-04-O
09'0306 LM2 0.1- for SI

+VCC3 +VCC
RS740 stuff
R55 4.7K-04-O
Q2 2N7002-S-O
RS740 stuff
R22 4.7K-04
RS740:6.8k
RS780:4.7K
10 DDCDATA — SDAT
R46 0-04
RS780 stuff
080903 change to VCC

+VCC3 +VCC
RS740 stuff
R59 4.7K-04-O
Q3 2N7002-S-O
RS740 stuff
R23 4.7K-04
RS740:6.8k
RS780:4.7K
10 DDCCLK — SCLK
R47 0-04
RS780 stuff

CHOKE17 CMK90-4P2R-O
10 TMDS_10N — TMDS_10N — TMDS_10N_DVI
10 TMDS_10P — TMDS_10P — TMDS_10P_DVI

CHOKE18 CMK90-4P2R-O
10 TMDS_11N — TMDS_11N — TMDS_11N_DVI
10 TMDS_11P — TMDS_11P — TMDS_11P_DVI

CHOKE23 CMK90-4P2R-O
10 TMDS_12N — TMDS_12N — TMDS_12N_DVI
10 TMDS_12P — TMDS_12P — TMDS_12P_DVI

CHOKE21 CMK90-4P2R
10 TMDS_00N — TMDS_00N — TMDS_00N_DVI
10 TMDS_00P — TMDS_00P — TMDS_00P_DVI

CHOKE22 CMK90-4P2R
10 TMDS_01N — TMDS_01N — TMDS_01N_DVI
10 TMDS_01P — TMDS_01P — TMDS_01P_DVI

CHOKE19 CMK90-4P2R
10 TMDS_02P — TMDS_02P — TMDS_02P_DVI
10 TMDS_02N — TMDS_02N — TMDS_02N_DVI

CHOKE20 CMK90-4P2R
10 TMDS_CLKN — TMDS_CLKN — TMDS_CLKN_DVI
10 TMDS_CLKP — TMDS_CLKP — TMDS_CLKP_DVI

+VCC_DDC_VGA_DVI
U5 AZ1045-04QU-S-O
TMDS_11N — TMDS_11N
TMDS_11P — TMDS_11P
TMDS_10N — TMDS_10N
TMDS_10P — TMDS_10P
SC140 .1U-04-O
Close to Connector

+VCC_DDC_VGA_DVI
U9 AZ1045-04QU-S-O
I2C_DATA_DVI — I2C_DATA_DVI
I2C_CLK_DVI — I2C_CLK_DVI
SC141 .1U-04-O
TMDS_12P — TMDS_12P
TMDS_12N — TMDS_12N

+VCC_DDC_VGA_DVI
U8 AZ1045-04QU-S-O
TMDS_01N — TMDS_01N
TMDS_01P — TMDS_01P
TMDS_00N — TMDS_00N
TMDS_00P — TMDS_00P
SC142 .1U-04-O
080903 change to VCC_DDC_VGA_DVI

+VCC_DDC_VGA_DVI
U6 AZ1045-04QU-S-O
TMDS_CLKN — TMDS_CLKN
TMDS_CLKP — TMDS_CLKP
TMDS_02P — TMDS_02P
TMDS_02N — TMDS_02N
SC143 .1U-04-O
Close to Connector

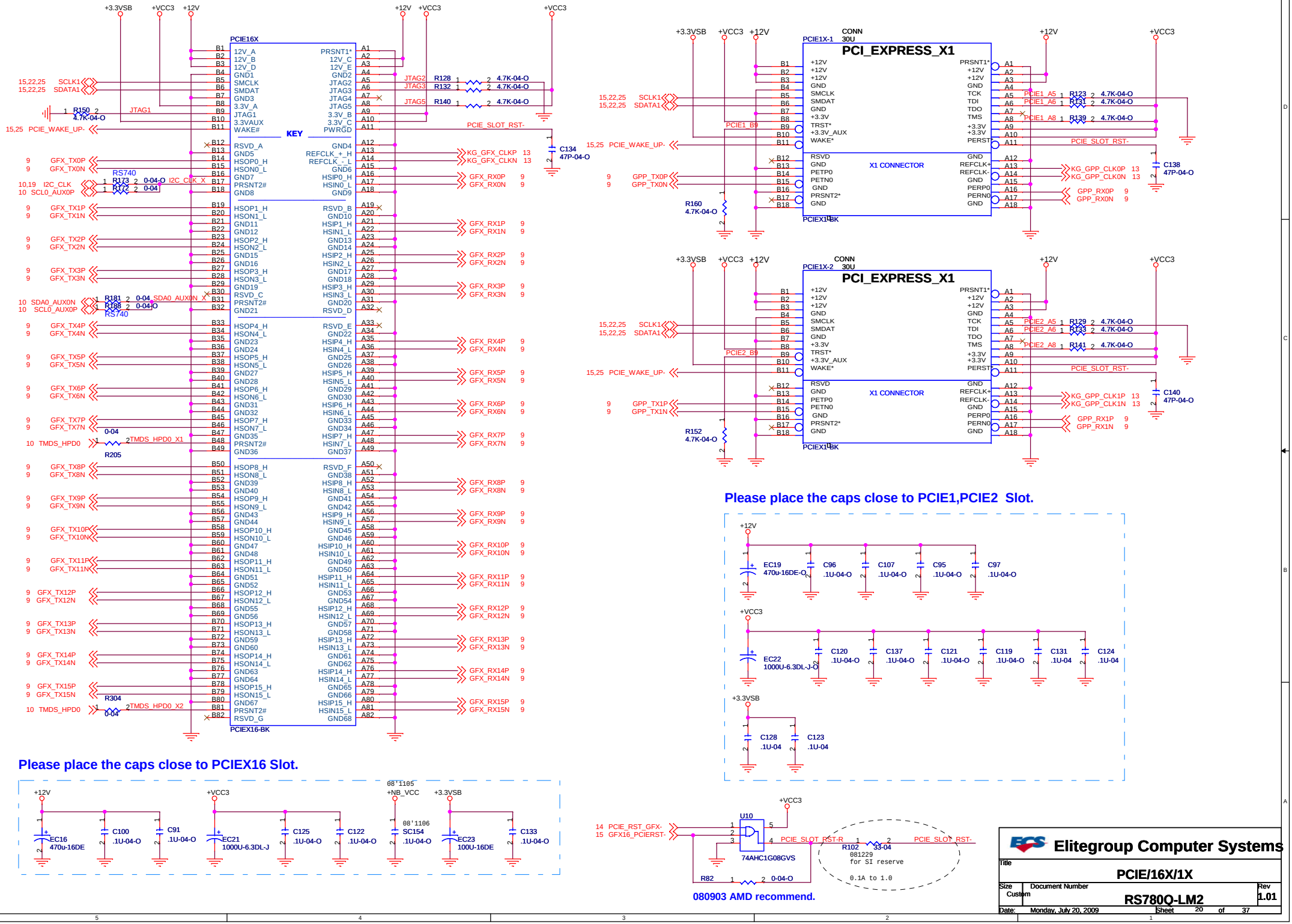
DVI1 CONN-24P3R-DVI
TMDS_02P_DVI — TMDS DATA 2+
TMDS_02N_DVI — TMDS DATA 2-
TMDS_11P_DVI — TMDS DATA 4+
TMDS_11N_DVI — TMDS DATA 4-
TMDS_01P_DVI — TMDS DATA 1+
TMDS_01N_DVI — TMDS DATA 1-
TMDS_10P_DVI — TMDS DATA 3+
TMDS_10N_DVI — TMDS DATA 3-
TMDS_00P_DVI — TMDS DATA 0+
TMDS_00N_DVI — TMDS DATA 0-
TMDS_12P_DVI — TMDS DATA 5+
TMDS_12N_DVI — TMDS DATA 5-
TMDS_CLKP_DVI — TMDS CLK +
TMDS_CLKN_DVI — TMDS CLK -
DDC CLK — I2C_CLK_DVI
DDC DATA — I2C_DATA_DVI
HOT PLUG DETECT — TMDS_HPD_DVI
RED — C1
GREEN — C2
BLUE — C3
H SYNC — C4
V SYNC — C8
A GND — C6
A GND — C5
GND (ANALOG) — 15
+5V POWER — 14
TMDS CLK SHIELD — 22
TMDS 2/4 SHIELD — 3
TMDS DATA 1/3 SHIELD — 11
TMDS DATA 0/5 SHIELD — 19
CASEGND — M2
CASEGND — M1

R62 200K-04
TMDS_HPD_DVI — TMDS_HPD_CON
10 TMDS_HPD2 — R68 33-04 — TMDS_HPD2_X
Q5 2N3904-S
TMDS_HPD_CON
R69 200K-04
R61 10K-04
+VCC3
+VCC_DDC_VGA_DVI

I2C_CLK_DVI — C129 10P-04-O
I2C_DATA_DVI — C54 10P-04-O

Elitegroup Computer Systems

Title	VGA / HDMI / DVI	
Size: Custom	Document Number: RS780Q-LM2	Rev: 1.01
Date: Monday, July 20, 2009	Sheet 19 of 37	


PCIE16X
PCIEX16-BK
KEY
Please place the caps close to PCIEX16 Slot.
PCIE1X-1
PCIE1X-2
CONN
30U
PCI_EXPRESS_X1
X1 CONNECTOR
PCIEX1-BK
Please place the caps close to PCIE1,PCIE2 Slot.
080903 AMD recommend.
Elitegroup Computer Systems
PCIE/16X/1X
RS780Q-LM2
1.01
Monday, July 20, 2009
20 of 37

5V_DUAL FOR USB,PS2,DIMM

TPM & Asset ID Function

0.1A to 1.0
reserve TPM/Assert ID

ST19NP18-O
02-440-918261

ST ST19NP18 & Winbond
WPCT200 co-lay

Winbond:
R338,R353,R358(H/W),
R352,R337,R349,R487

ST:
R346,R350,R349,R487

PCA24S08D-O
01-530-008210

	Ra	Rb	Rc	Rd	Re	Rf	Rg
ST	X	V	V	X	X	X	X
Winbond	V	X	X	V	V	V	V

to USB Header

to DIMM PWM

080905 change

to USB conn/PS2

FRONT SIDE 4 PORTS

USB 0,1

H6X2-P11E-Y
CMK90-4P2R
16-400-900142
AZC099-04S-O
Close to F_USB1 header

USB 2,3

H6X2-P11E-Y
CMK90-4P2R
AZC099-04S-O
Close to F_USB2 header

USB 4,5

H6X2-P11E-Y-O
CMK90-4P2R-O
AZC099-04S-O
Close to F_USB3 header

REAR SIDE 6 PORTS

080909 change to CMM21 type

16-400-900142

CMK90-4P2R-O

USB 8,9,10,11

USB-2
10-084-008241
10-084-008693
10-084-008453

080916 for ESD

Close to USB1 connector

USB STITCHING CAPS.

Elitegroup Computer Systems	
Title	TPM, USB,5VDUAL SWITCH
Size: Custom	Document Number: RS780Q-LM2
Rev	1.01
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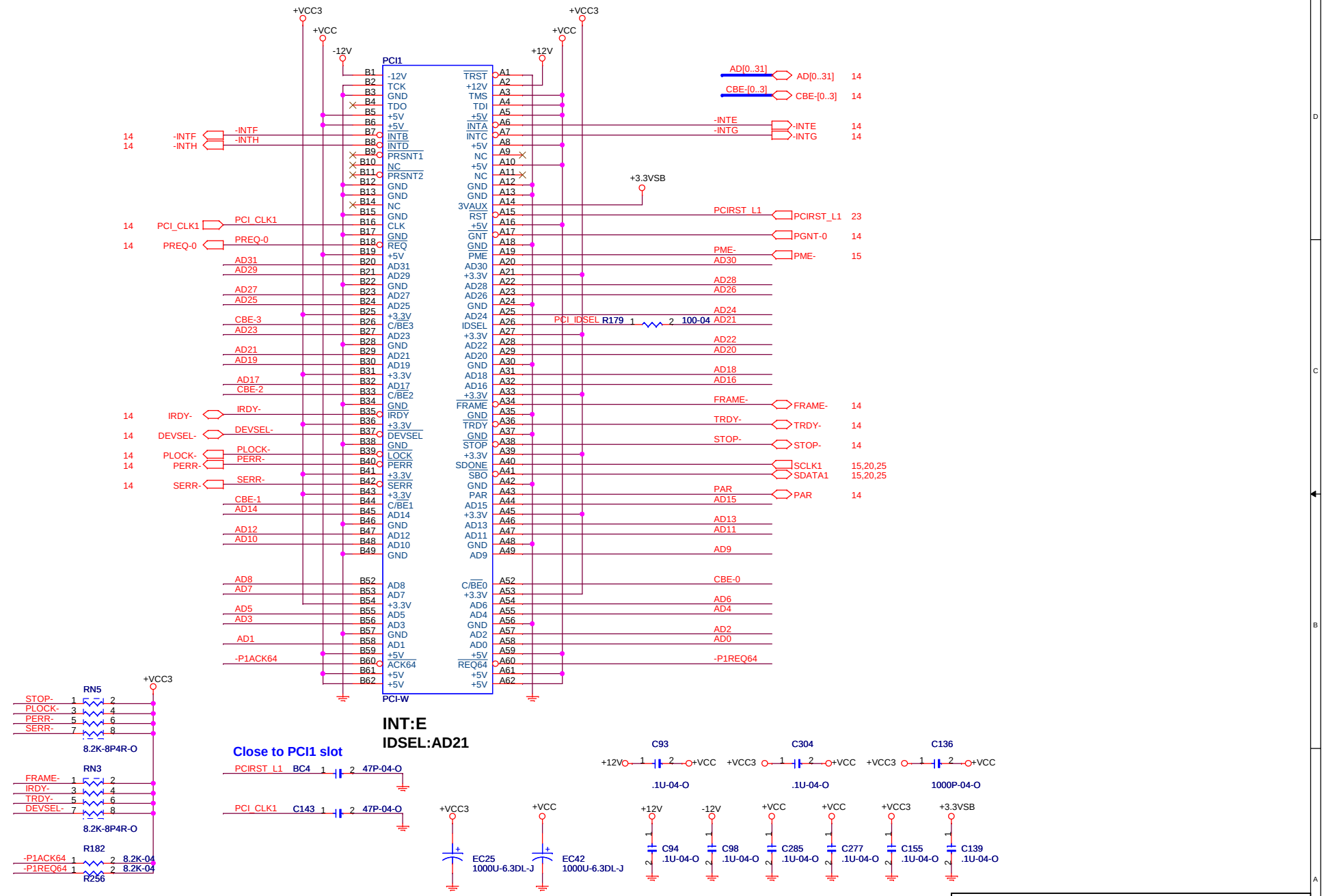
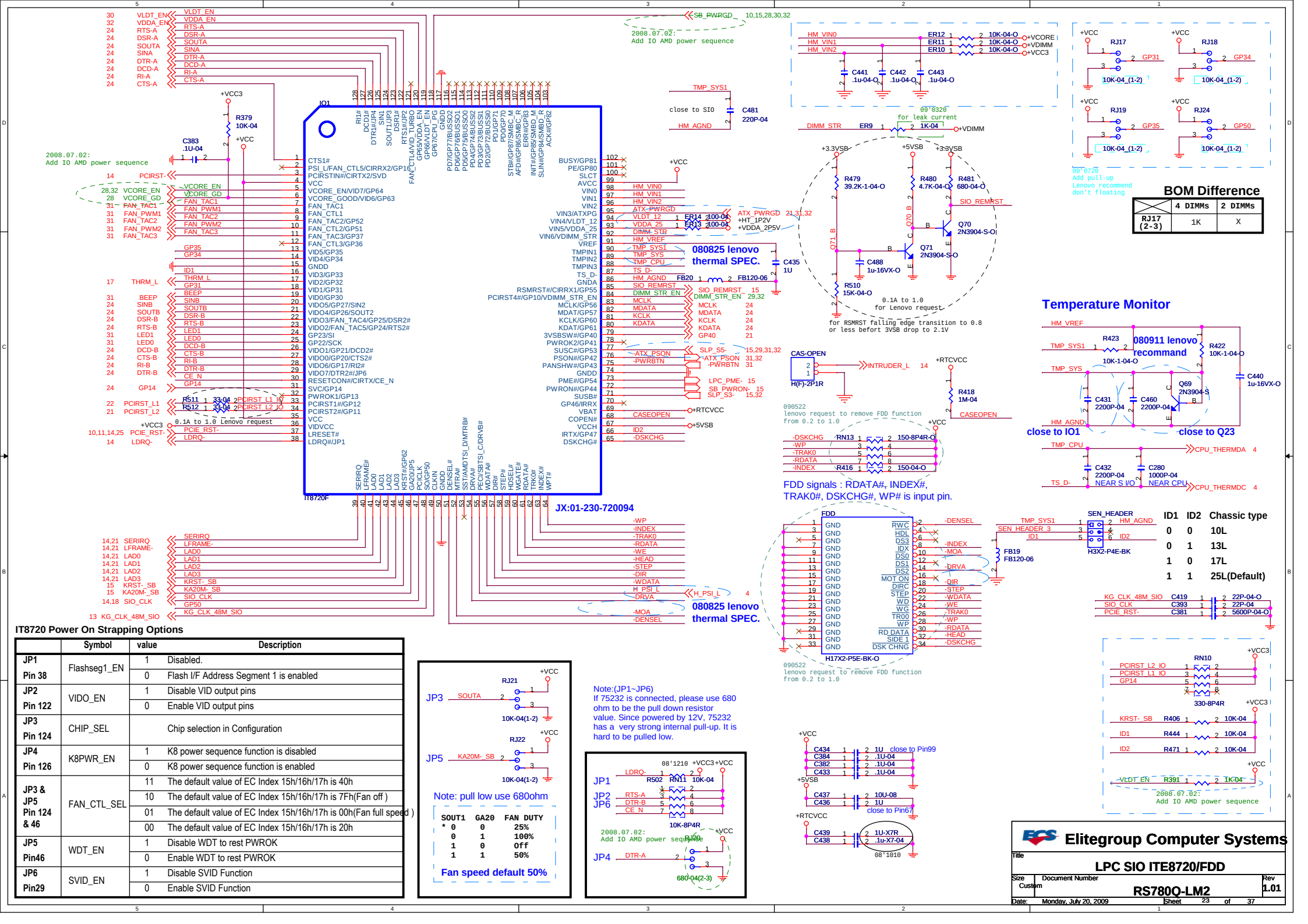


Elitegroup Computer Systems

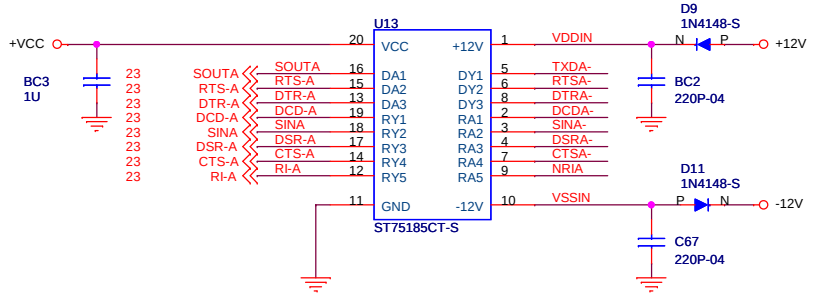
Title	PCI SLOT	
Size: Custom	Document Number: RS780Q-LM2	Rev: 1.01
Date: Monday, July 20, 2009	Sheet 22 of 37	

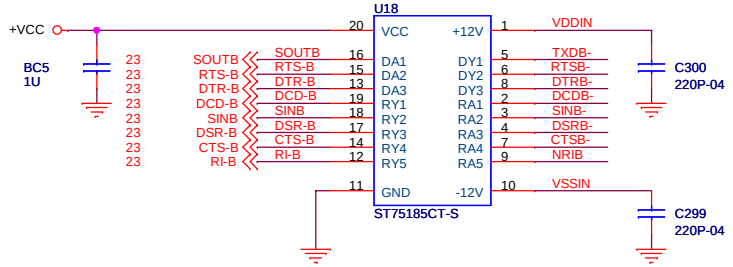


IT8720 Power On Strapping Options

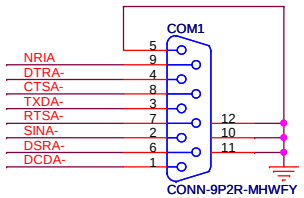
	Symbol	value	Description
JP1 Pin 38	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP2 Pin 122	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 124	CHIP_SEL		Chip selection in Configuration
JP4 Pin 126	K8PWR_EN	1	K8 power sequence function is disabled
		0	K8 power sequence function is enabled
JP3 & JP5 Pin 124 & 46	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 40h
		10	The default value of EC Index 15h/16h/17h is 7Fh(Fan off)
		01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
		00	The default value of EC Index 15h/16h/17h is 20h
JP5 Pin46	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP6 Pin29	SVID_EN	1	Disable SVID Function
		0	Enable SVID Function

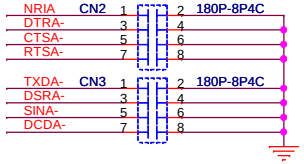
COM

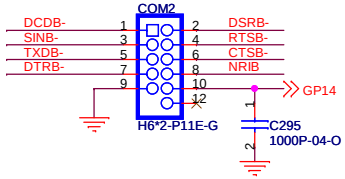


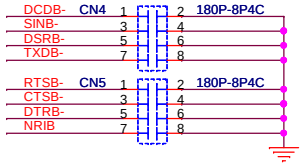


10-002-009021

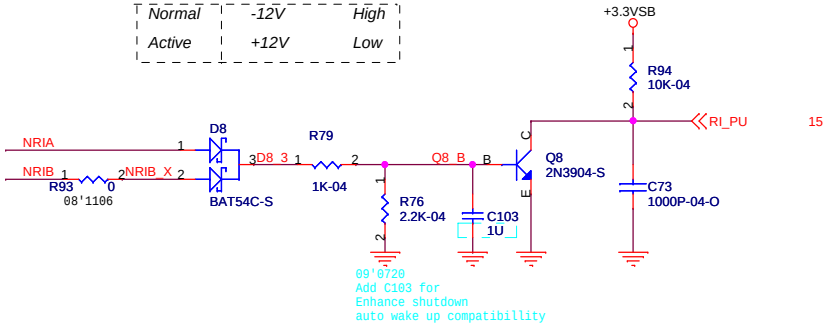




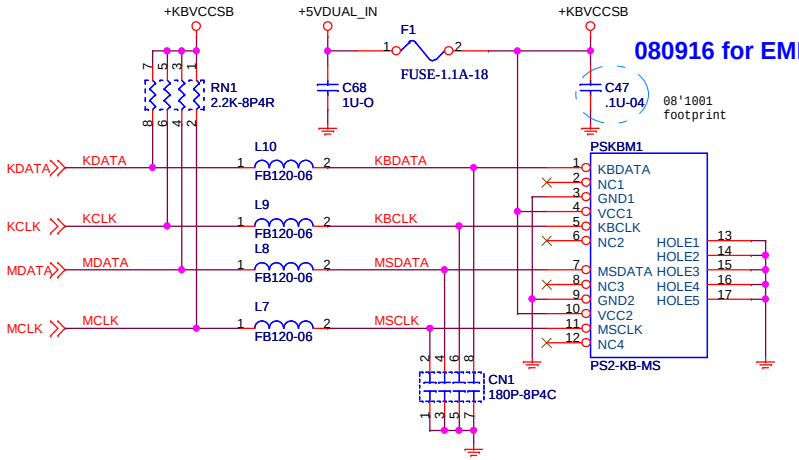




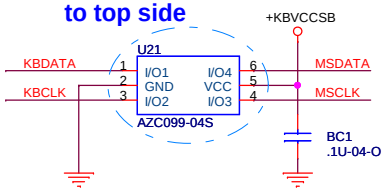
NRIA	RI#
Normal	-12V	High
Active	+12V	Low



PS2



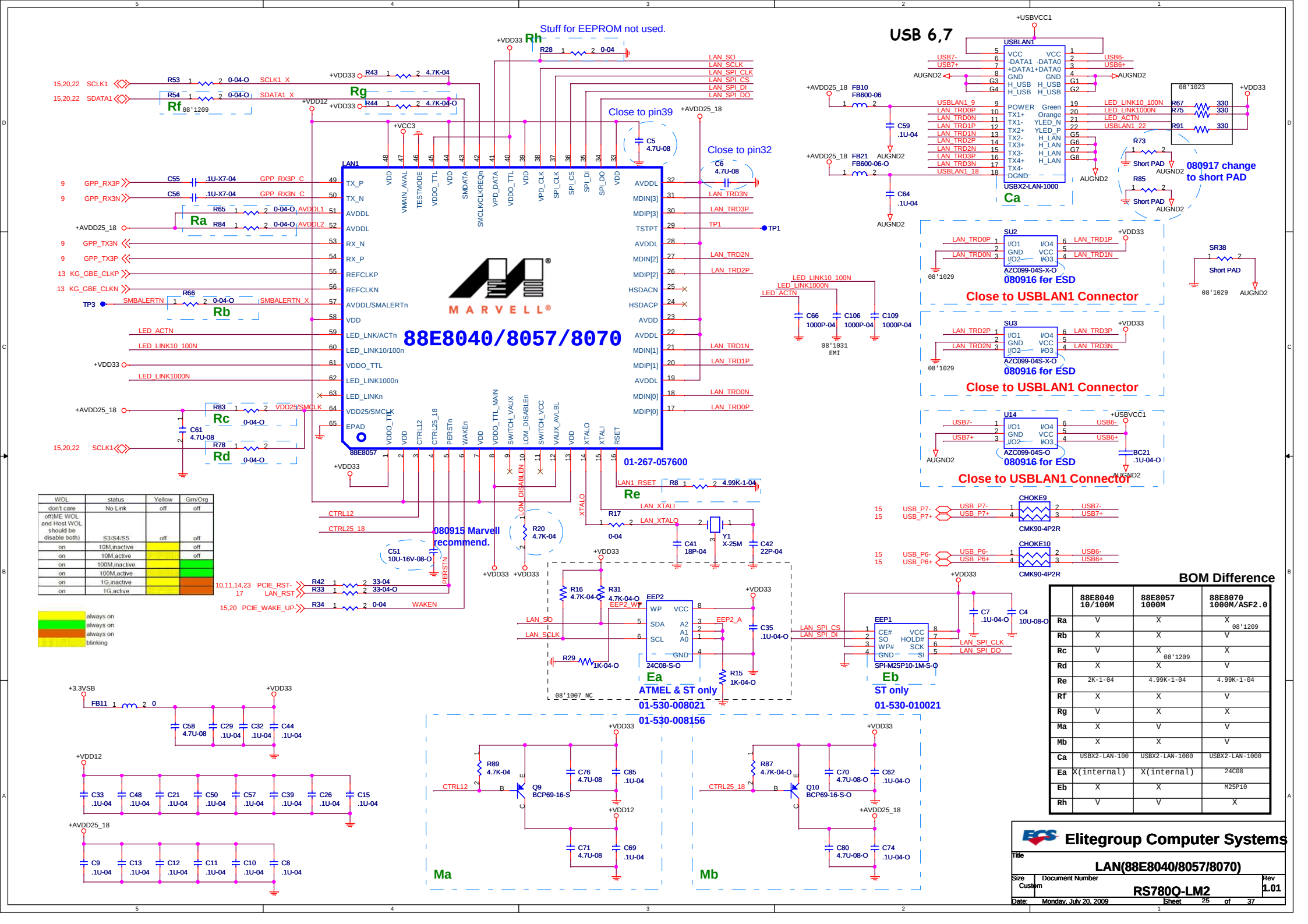
080919 change
to top side



Close to PSKBM1 connector

Elitegroup Computer Systems

Title	PS2 / COM PORT	
Size: Custom	Document Number: RS780Q-LM2	Rev: 1.01
Date: Monday, July 20, 2009	Sheet 24 of 37	

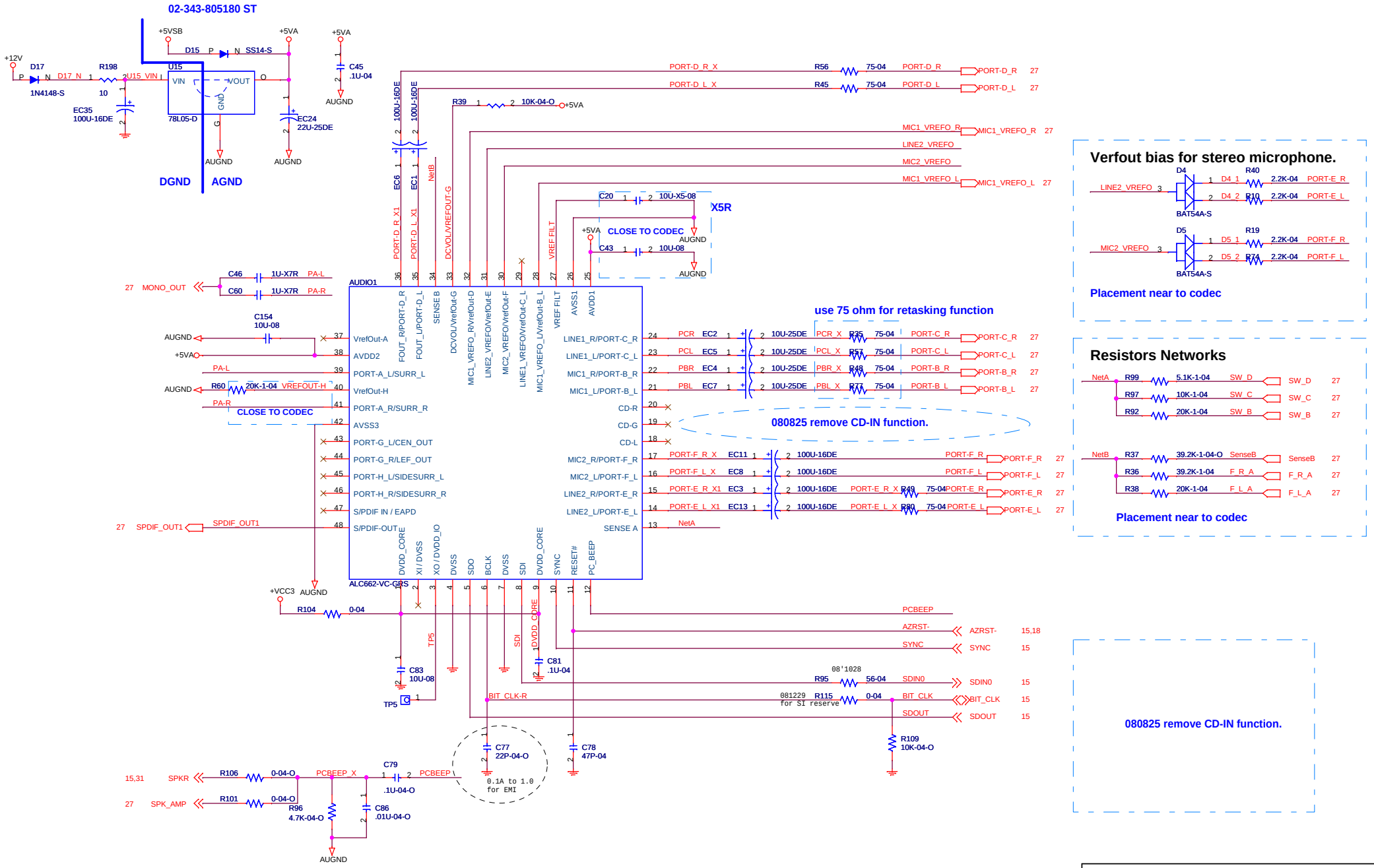


WOL	status	Yellow	Grn/Org
don't care	No Link	off	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off	off
on	10M,inactive		off
on	10M,active		off
on	100M,inactive		
on	100M,active		
on	1G,inactive		
on	1G,active		

always on
always on
always on
blinking

	88E8040 10/100M	88E8057 1000M	88E8070 1000M/ASF2.0
Ra	V	X	X 08'1209
Rb	X	X	V
Rc	V	X 08'1209	X
Rd	X	X	V
Re	2K-1-04	4.99K-1-04	4.99K-1-04
Rf	X	X	V
Rg	V	X	X
Ma	X	V	V
Mb	X	X	V
Ca	USBX2-LAN-100	USBX2-LAN-1000	USBX2-LAN-1000
Ea	X(internal)	X(internal)	24C08
Eb	X	X	M25P10
Rh	V	V	X

Title	LAN(88E8040/8057/8070)		
Size: Custom	Document Number: RS780Q-LM2		Rev: 1.01
Date: Monday, July 20, 2009	Sheet 25 of 37		


02-343-805180 ST
+12V
D17
1N4148-S
R198
10
U15
78L05-D
VIN
VOUT
GND
+5VSB
D15
SS14-S
+5VA
EC35
100U-16DE
EC24
22U-25DE
C45
.1U-04
AUGND
DGND
AGND
R39
10K-04-O
100U-16DE
EC6
EC1
NetB
DCVOL/VREFOUT-G
PORT-D_R_X1
PORT-D_L_X1
PORT-D_R_X
PORT-D_L_X
R56
R45
75-04
PORT-D_R
PORT-D_L
MIC1_VREFO_R
LINE2_VREFO
MIC2_VREFO
MIC1_VREFO_L
C20
10U-X5-08
X5R
C43
10U-08
CLOSE TO CODEC
VREF FILT
AVSS1
AVDD1
C46
C60
1U-X7R
PA-L
PA-R
MONO_OUT
AUDIO1
C154
10U-08
VrefOut-A
AVDD2
PORT-A_L/SURR_L
VrefOut-H
PORT-A_R/SURR_R
AVSS3
PORT-G_L/CEN_OUT
PORT-G_R/LEF_OUT
PORT-H_L/SIDESURR_L
PORT-H_R/SIDESURR_R
S/PDIF IN / EAPD
S/PDIF-OUT
SPDIF_OUT1
R60
20K-1-04
VREFOUT-H
FOUT_R/PORT-D_R
FOUT_L/PORT-D_L
SENSE B
DCVOL/VrefOut-G
MIC1_VREFO_R/VrefOut-D
LINE2_VREFO/VrefOut-E
MIC2_VREFO/VrefOut-F
LINE1_VREFO/VrefOut-C_L
MIC1_VREFO_L/VrefOut-B_L
use 75 ohm for retasking function
LINE1_R/PORT-C_R
LINE1_L/PORT-C_L
MIC1_R/PORT-B_R
MIC1_L/PORT-B_L
CD-R
CD-G
CD-L
MIC2_R/PORT-F_R
MIC2_L/PORT-F_L
LINE2_R/PORT-E_R
LINE2_L/PORT-E_L
SENSE A
PCR
PCL
PBR
PBL
EC2
EC5
EC4
EC7
10U-25DE
PCR_X
PCL_X
PBR_X
PBL_X
R35
R57
R48
R77
PORT-C_R
PORT-C_L
PORT-B_R
PORT-B_L
080825 remove CD-IN function.
PORT-F_R_X
PORT-F_L_X
PORT-E_R_X1
PORT-E_L_X1
EC11
EC8
EC3
EC13
100U-16DE
R49
R80
PORT-F_R
PORT-F_L
PORT-E_R
PORT-E_L
NetA
ALC662-VC-GRS
DVDD_CORE
XI / DVSS
XO / DVDD_IO
DVSS
SDO
BCLK
DVSS
SDI
DVDD_CORE
SYNC
RESET#
PC_BEEP
+VCC3
R104
0-04
TP5
C83
10U-08
C81
.1U-04
C77
22P-04-O
C78
47P-04
0.1A to 1.0
for EMI
PCBEEP
AZRST-
SYNC
08'1028
R95
56-04
SDIN0
BIT_CLK-R
081229
for SI reserve
R115
0-04
BIT_CLK
SDOUT
R109
10K-04-O
SPKR
SPK_AMP
R106
R101
0-04-O
PCBEEP_X
C79
.1U-04-O
R96
4.7K-04-O
C86
.01U-04-O
Verfout bias for stereo microphone.
D4
D5
BAT54A-S
R40
R19
2.2K-04
PORT-E_R
PORT-E_L
PORT-F_R
PORT-F_L
Placement near to codec
Resistors Networks
R99
R97
R92
5.1K-1-04
10K-1-04
20K-1-04
SW_D
SW_C
SW_B
R37
R36
R38
39.2K-1-04-O
39.2K-1-04
20K-1-04
SenseB
F_R_A
F_L_A
Placement near to codec
080825 remove CD-IN function.
Elitegroup Computer Systems
Title
AUDIO ALC662/ALC888
Size
Custom
Document Number
RS780Q-LM2
Rev
1.01
Date:
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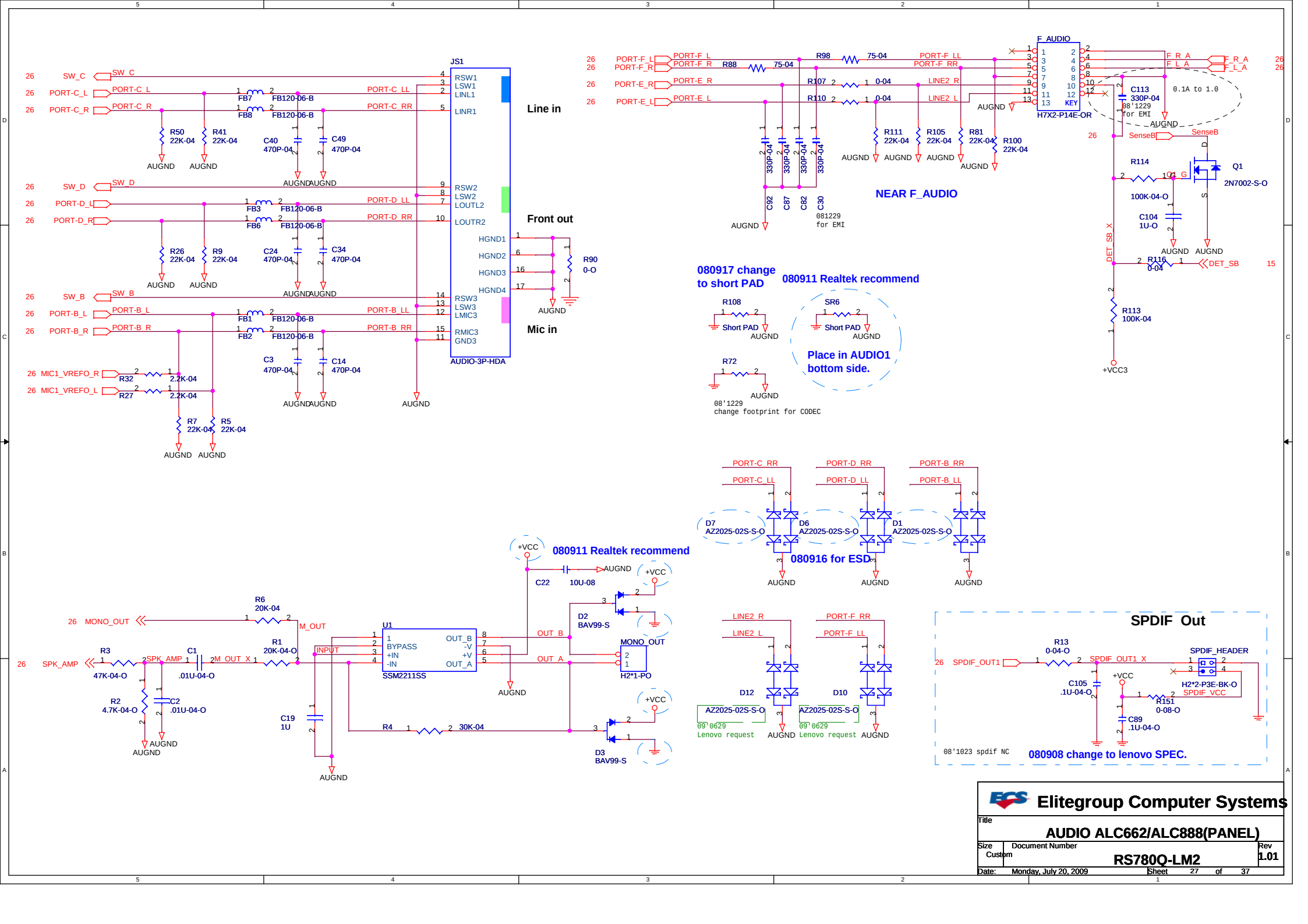
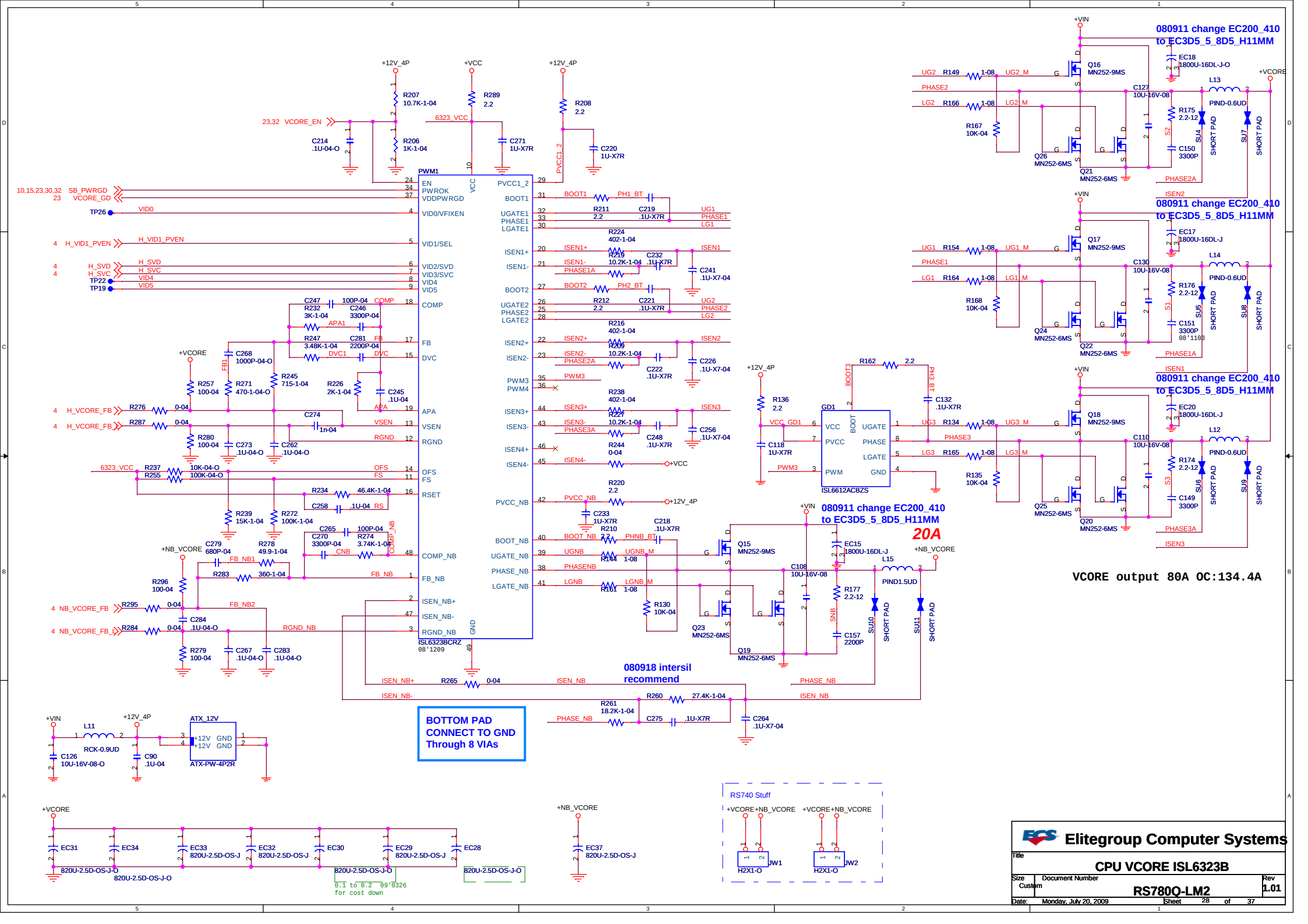
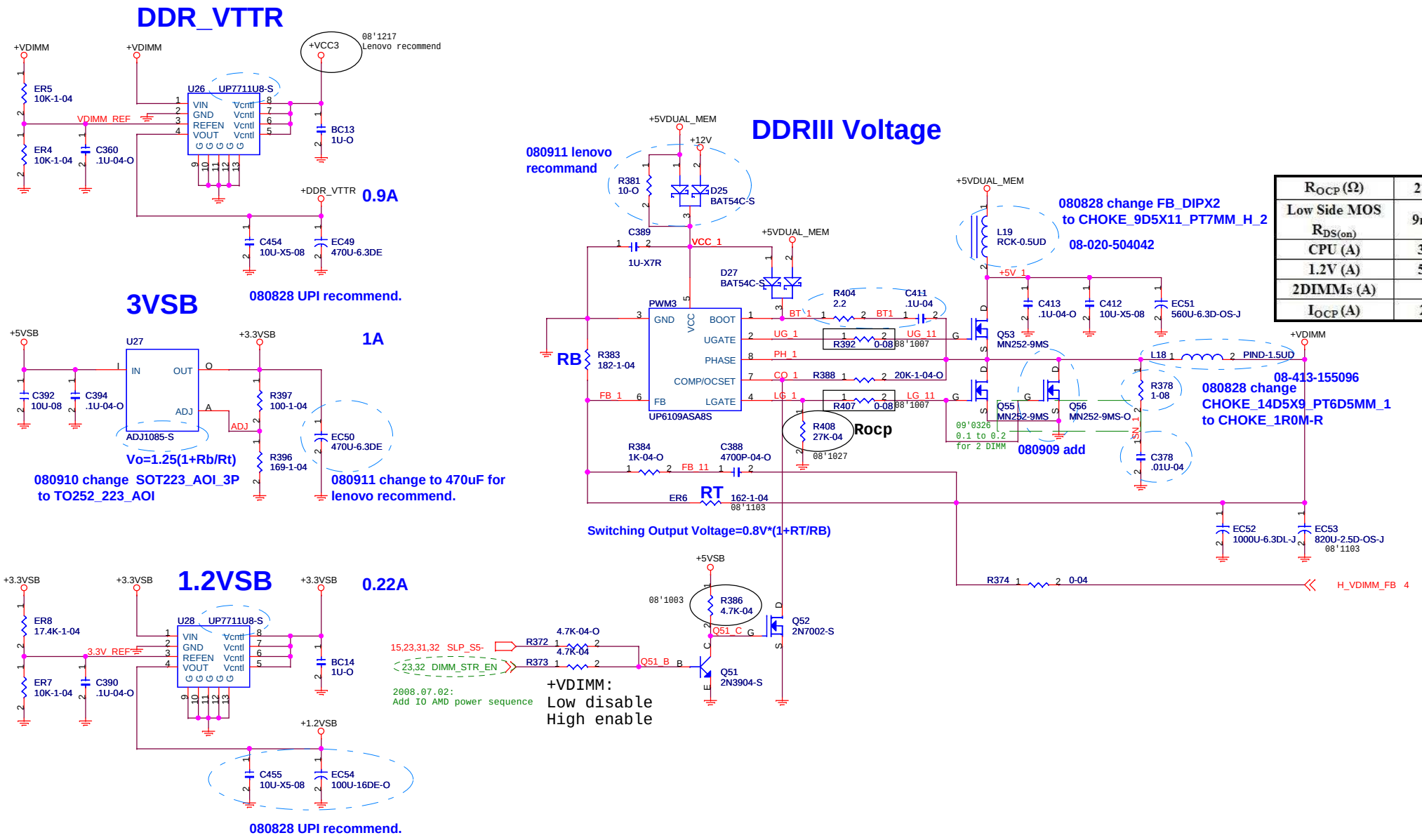
37


JS1
AUDIO-3P-HDA
Line in
Front out
Mic in
F_AUDIO
H7X2-P14E-OR
NEAR F_AUDIO
080917 change to short PAD
080911 Realtek recommend
Place in AUDIO1 bottom side.
080916 for ESD
SPDIF Out
080908 change to lenovo SPEC.
SSM2211SS
Elitegroup Computer Systems
AUDIO ALC662/ALC888(PANEL)
RS780Q-LM2
Monday, July 20, 2009


080911 change EC200_410 to EC3D5_5_8D5_H11MM
080911 change EC200_410 to EC3D5_5_8D5_H11MM
080911 change EC200_410 to EC3D5_5_8D5_H11MM
080911 change EC200_410 to EC3D5_5_8D5_H11MM
20A
VCORE output 80A OC:134.4A
080918 intersil recommend
BOTTOM PAD CONNECT TO GND Through 8 VIAs
RS740 Stuff
PWM1
ISL6323BCRZ
ISL6612ACBZS
Elitegroup Computer Systems
CPU VCORE ISL6323B
RS780Q-LM2
Monday, July 20, 2009



R_{OCP} (Ω)	27K
Low Side MOS $R_{DS(on)}$	9mΩ
CPU (A)	3.6
1.2V (A)	5.3
2DIMMs (A)	6
I_{OCP} (A)	25

Elitegroup Computer Systems

Title: DC POWER, DDRIII POWER

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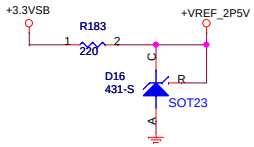
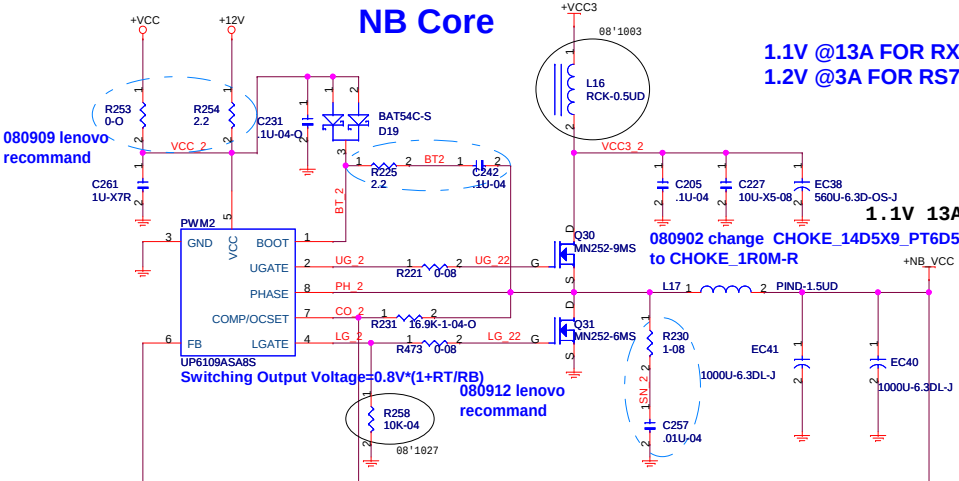
VREF 2.5V



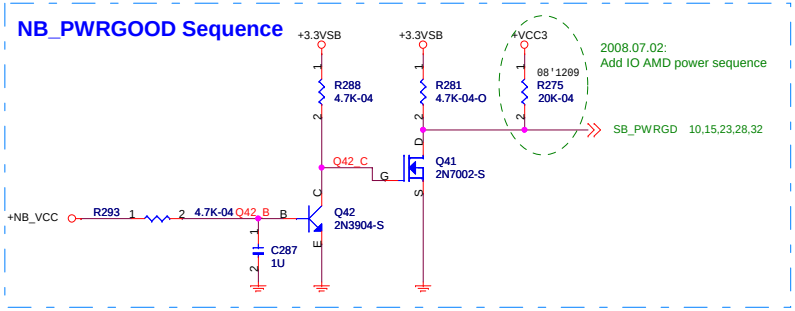
NB Core

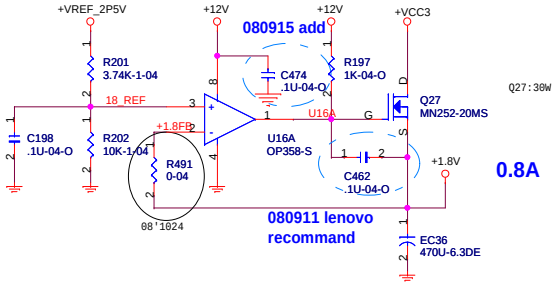
1.1V @13A FOR RX780/RS780
1.2V @3A FOR RS740



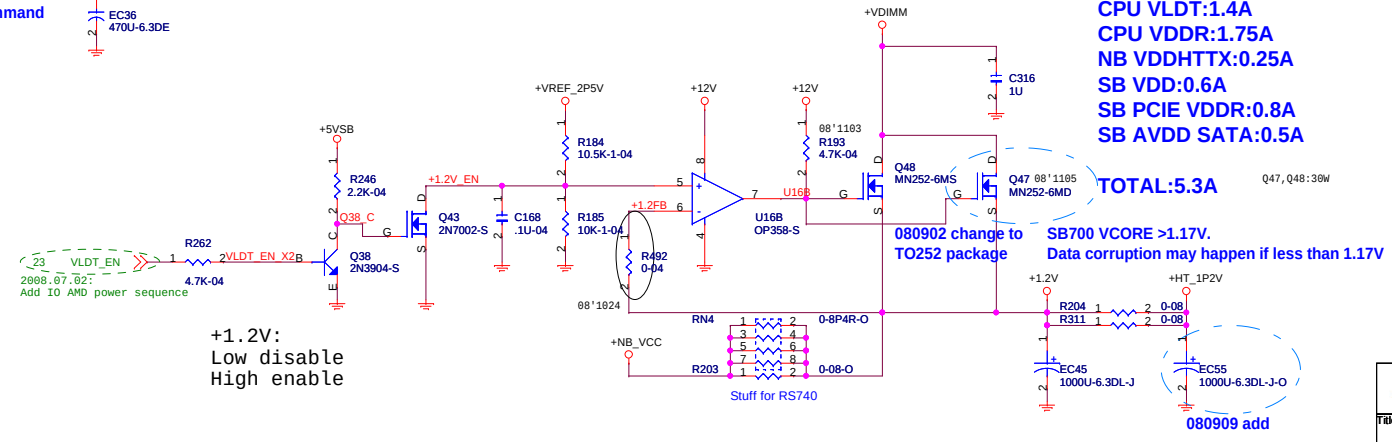
+NB_VCC:
Low disable
High enable

NB_PWRGOOD Sequence





RS780 USE



+1.2V:
Low disable
High enable

Elitegroup Computer Systems

Title	NB CORE POWER	
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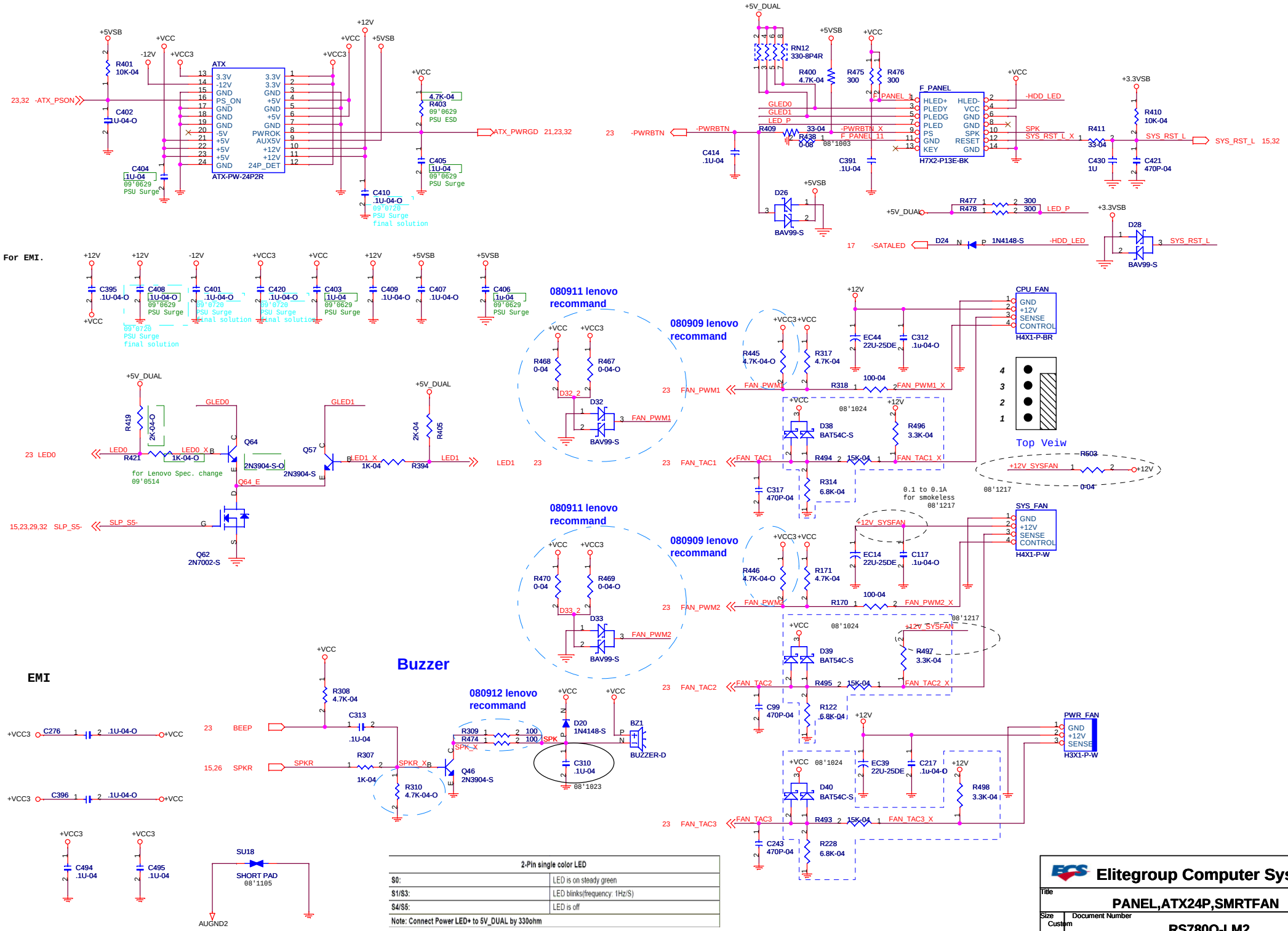
ATX
ATX-PW-24P2R
F_PANEL
H7X2-P13E-BK
CPU_FAN
H4X1-P-BR
SYS_FAN
H4X1-P-W
PWR_FAN
H3X1-P-W
BAV99-S
BUZZER-D
Top Veiw
080911 lenovo recommand
080909 lenovo recommand
080912 lenovo recommand
Buzzer
EMI
For EMI.
2-Pin single color LED
$0: LED is on steady green
$1/$3: LED blinks(frequency: 1Hz/S)
$4/$6: LED is off
Note: Connect Power LED+ to 5V_DUAL by 330ohm
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PANEL,ATX24P,SMRTFAN
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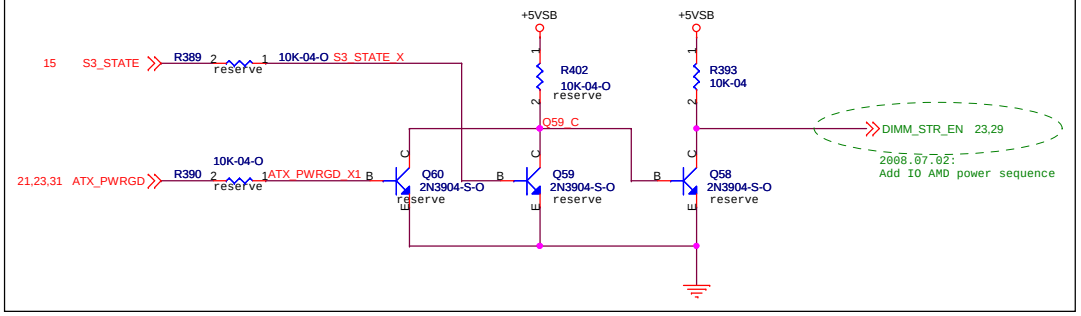
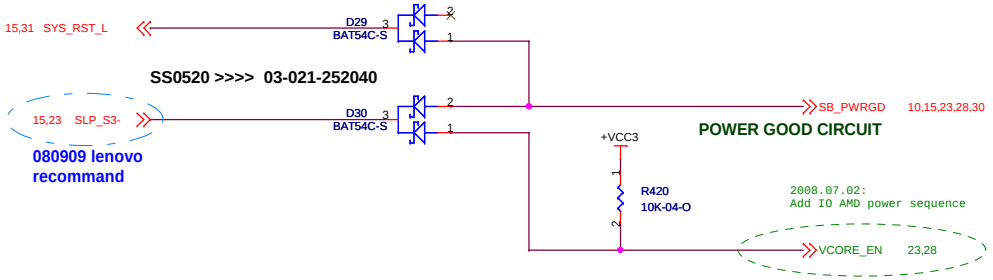
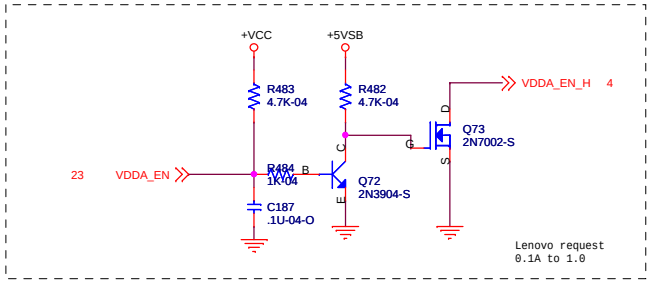
POWER GOOD & ENABLES

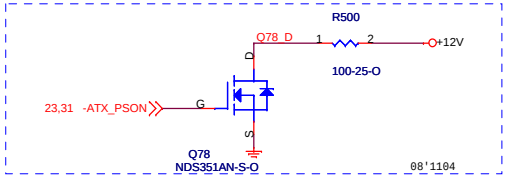
ATHLON64 POWER GOOD & ENABLES CIRCUIT

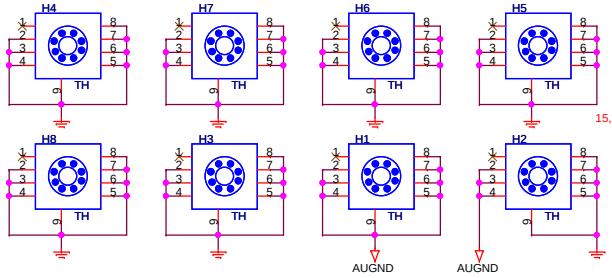


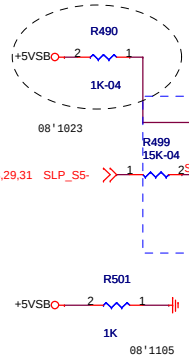
POWER GOOD CIRCUIT

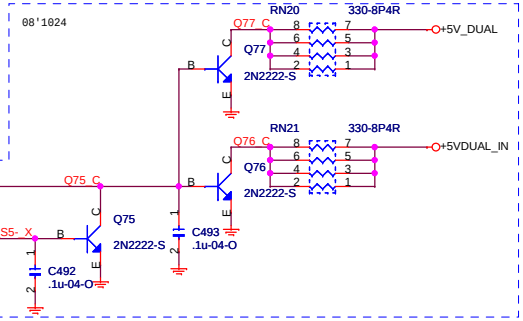












Elitegroup Computer Systems		
Title: POWER ENABLE		
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SB710

Name	Type	Voltage	Default	Functional Description	Function
GPIO4	I/O	3.3V	Input	Smartvolt Select 1/Serial ATA Interlock 2/GPIO 4	H_PRESENT_L
IMC_GPIO8	I/O	3.3V_S5	Input	IMC_GPIO8	F_USB1 detect
IMC_GPIO9	I/O	3.3V_S5	Input	IMC_GPIO9	F_USB2 detect
IMC_GPIO10	I/O	3.3V_S5	Input	IMC_GPIO10	F_USB3 detect
IMC_GPIO11	I/O	3.3V_S5	Input	IMC_GPIO11	LC CLR_CMOS
IMC_GPIO13	I/O	3.3V_S5	Input	Low Voltage SMBus Clock 3/IMC_GPIO13	SMCLK3
IMC_GPIO14	I/O	3.3V_S5	Input	Low Voltage SMBus Data 3/IMC_GPIO14	SMDATA3
GPIO5	I/O	3.3V	Input	SMARTVOLT2/SHUTDOWN#/GPIO5	F_AUDIO detect
GPIO9	I/O	3.3V	Input	DDC1_SCL/GPIO9	TPM reserve
GPIO8	I/O	3.3V	Input	DDC1_SDA/GPIO8	TPM reserve
GPIO13	I/O	3.3V	Output	LAN Reset//GPIO13	LAN_RST
GPIO66	I/O	3.3V_S5	Input	Low-Low Battery/GPIO 66	LPCPD_N

ITE8720

Name	Type	Voltage	Functional Description	Function
GP14	I/O	5V	Serial VID clock/PECI request/GPIO14	COM2 detect
GP22	I/O	5V_S5	Serial flash clock/GPIO22	Power LED
GP23	I/O	5V_S5	Serial flash in data/GPIO23	SUS LED
GP30	I/O	5V	Voltage ID0/GPIO30	BEEP
GP31	I/O	5V	Voltage ID1/GPIO31	BIOS reserve
GP34	I/O	5V	Voltage ID4/GPIO34	BIOS reserve
GP35	I/O	5V	Voltage ID5/GPIO35	BIOS reserve
GP40	I/O	5V_S5	3VSBSW/GP40	Dual switch
GP33	I/O	5V	VID3/GP33	Sensor header ID1
GP47	I/O	5V	IR output/GP47	Sensor header ID2
GP50	I/O	5V	Serial flash data output/GPIO50	BIOS reserve

For 103

X1(WIRE)1

XTAL-JW

For 104

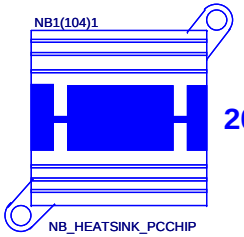
SPI_ROM_D(104)1

SPI-ROM-D-8M

BT1(104)1

BATTERY

NB1(104)1



20-120-014500

NB_HEATSINK_PCCHIP

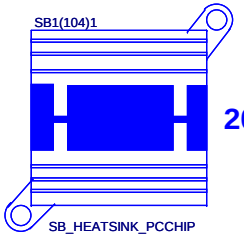
CLR_CMOS1(104)1

JP-R-H

SPI_DEBUG(104)1

JP-R-H

SB1(104)1



20-120-010773

SB_HEATSINK_PCCHIP

Elitegroup Computer Systems

Title: Attention

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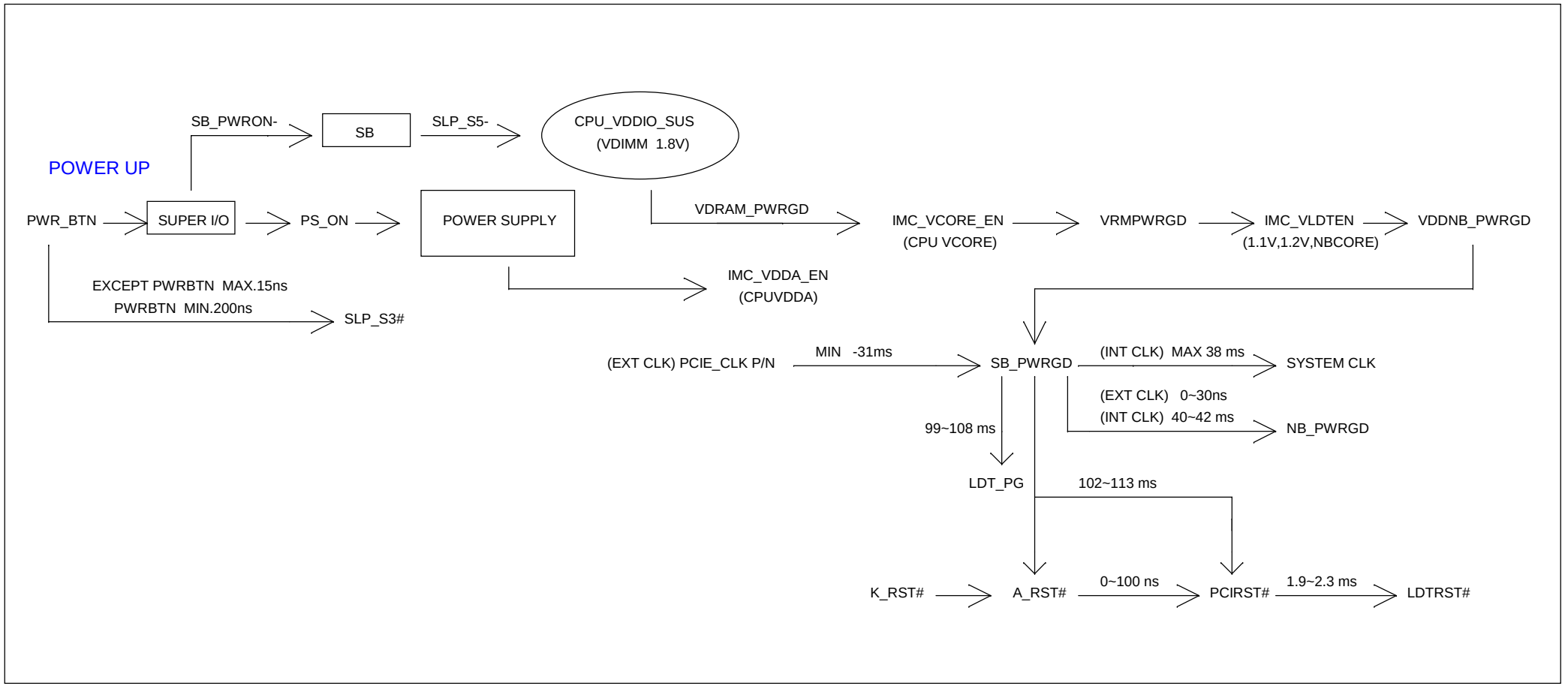

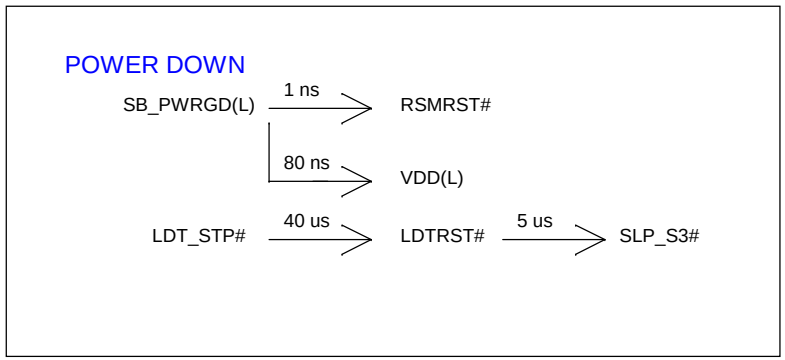

Elitegroup Computer Systems

Title: Power Sequence		
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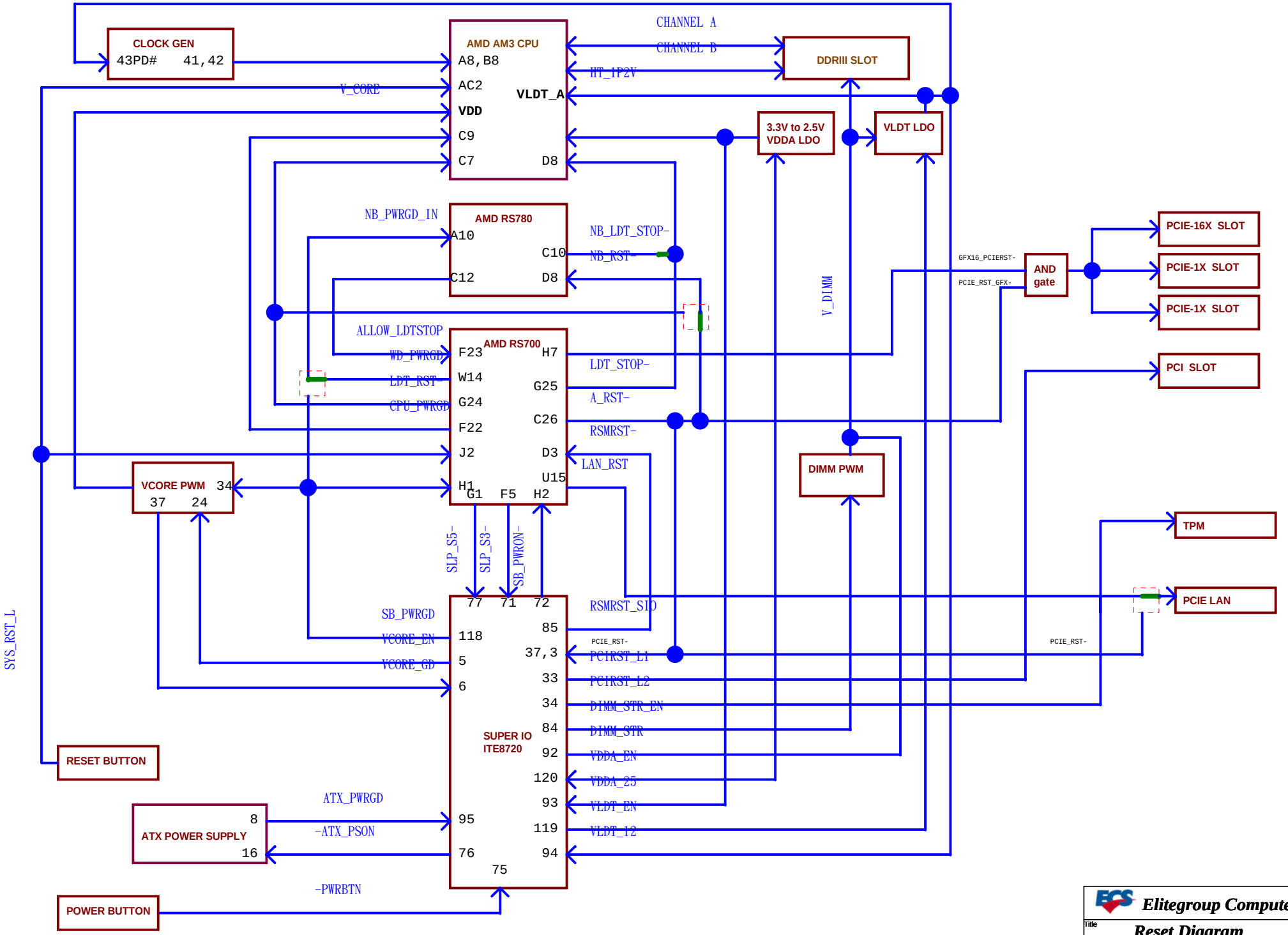

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Title: Reset Diagram

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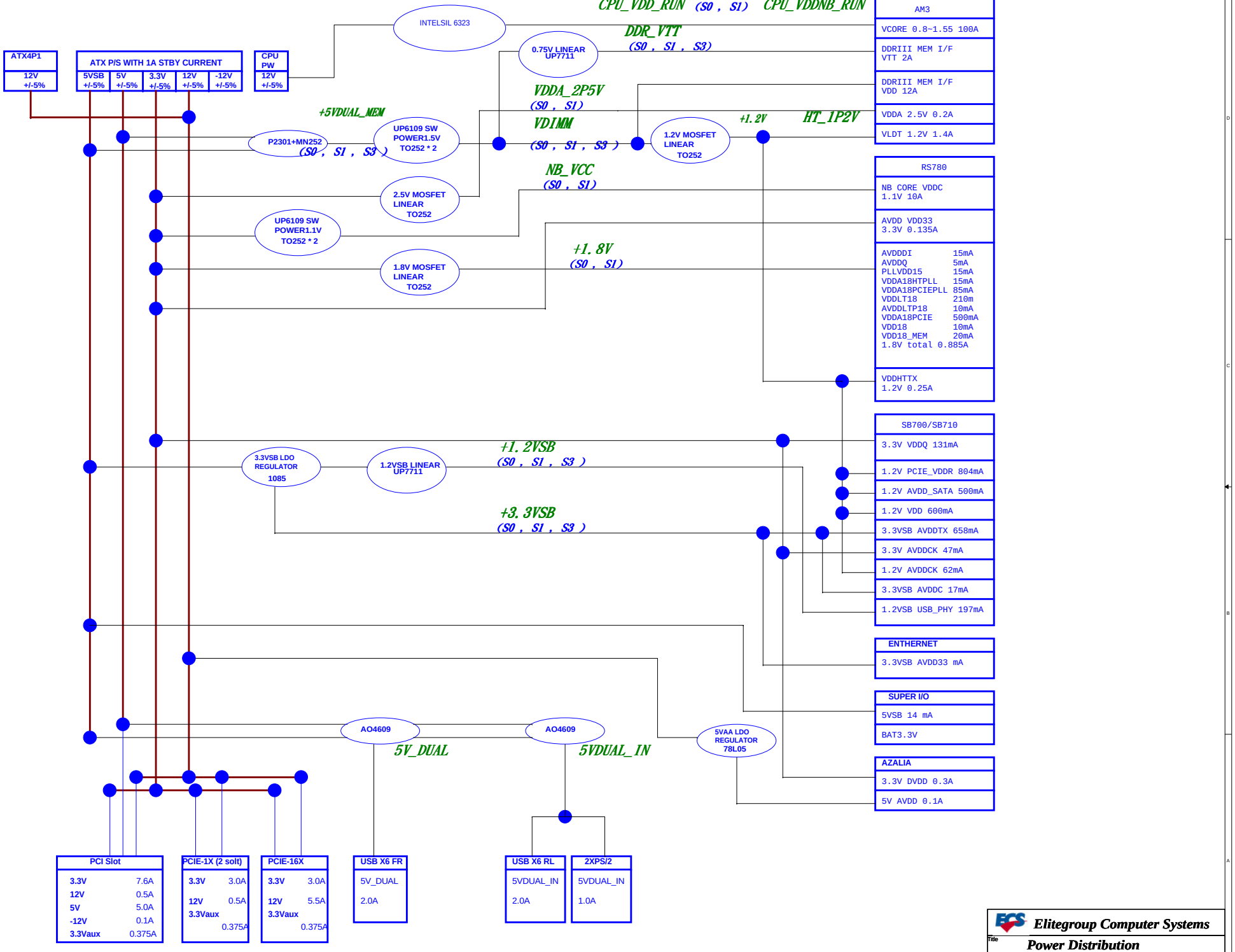

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Title: Power Distribution

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REVISION HISTORY:

Rev	Date	Notes
0.1(RS880)	09'0205	Change from RS780Q-LM V1.0 modify reserve function to meet RS880Q-LM V0.1 Spec. 1.Add DVI 2.change LAN to giga LAN 3.Add MONO_OUT 4.Add COM1 5.Add CAS-OPEN 6.Add Assert-ID 7.Add TPM 8.remove eSATA 9.Add FDD 10.change NB to RS880C 11.change 8M SPI ROM 12.del front USB(total 10 port) 13.add VGA noise soluction for RS880C
0.1(LM2)	09'0223	Change from RS880Q-LM V0.1 modify reserve function to meet Lenovo RS780Q-LM2 Spec. 1.Change NB to RS780L 2.Change DIMMs to 2 slots 3.Change LAN IC to without ASF IC(8057) 4.Change Rear USB to 4 ports 5.Change F_USB to 3 groups 6.Change SPDIF HEADER default value empty 7.Change TPM and Assert ID default value to empty
		P15 change R354 to 56 ohm,C347 remove,add R103 for SI
	09'0306	P19 mount U4,U7 unmount R18,R58 for SI P12 SC32,SC29,SC18,SC9 change to 22uF for SI P30 R233,R236 change value for SI
	09'0320	P17 update SATA text, R472,D21 unmount,mount R306 for MP P23 ER9 change to 1K for leak current
0.2(LM2)	09'0326	P21 unmount U20,U23,U25 for EMI cost down P28 unmount EC30,EC28 for cost down P29 Q55 change to 9m ohm for 2DIMM design
1.0(LM2)	09'0514	Add RS780Q-LM ECN_1373 modify Page3 R339,R364 change 1K for Lenovo Spec. change Page31 unmount R419,R421,Q64 for Lenovo Spec. change Page19 mount R52,Q4, unmount R51 for Lenovo Spec. change
1.0(LM2)	09'0522	Page23 Removed FDD, RN13, R416 for Lenovo Spec. change
	09'0629	Page27 Removed D10,D12 for Lenovo PM request Page31 Add R403,C405,C403,C408,C404,C406 for PSU Surge
1.01(LM2)	09'0715	change CPU footprint type for EMI
	09'0720	Page31 Del C420,C410,C401,C408 for PSU Surge final solution Page21 remove F_USB3 for Spec. update Page23 Add RJ17,RJ18,RJ19,RJ24 don't floating for Lenovo recommend Page24 Add C103 for enhance shutdown auto wake up compatibillity

Rev	Date	ECN no.	Notes
1.0(LM2)	09'0527	DCN_1384	Page10 R117 from 4.7K change to 2.2K for design change

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Title: Cover Page

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SD Ram (168 Pins, 3.3V) Pin Details

Supply:- 6,18,26,40,41 Ground:- 1,12,23,32 Data:- 2,3,4,4,7,8 Address:- 33,34,35,36,37

DDR-1 Ram (184 Pins, 2.5V) Pin Details

Supply:- 7,15,22,30,46 Ground:- 3,11,26,50 Data:- 2,4,6,12,13 Address:- 32,37,41,43,48

WE:- 63 CAS:- 65 RAS:- 154 SM DATA:- 91 SMCLOCK:- 92 BA:- 52,59

SPDVDD:- 184 Vref:- 1 CS:- 157,158 CKE:- 21,211 DCLK:- 16,17,137,138

DDR-2 Ram (240 pins, 1.8V) Pin Details

Supply:- 53,59,64 Ground:- 2,5,11,14 Data:- 3,4,9,10,12,13 Address:- 57,58,60,61

WE:- 73 CAS:- 74 RAS:- 192 SM DATA:- 119 SMCLOCK:- 120 BA:- 71,190

SPDVDD:- 238 Vref:- 1 CS:- 76,193 CKE:- 52,171 DCLK:- 221,220,138

DDR-3 Ram (240 Pins, 1.5V) Pin Details

Supply:- 51,54,57,60,62 Ground:- 2,5,8,11,14 Data:- 3,4,6,7,9,10 Address:- 55,56,58,59,61

WE:- 73 CAS:- 74 RAS:- 192 SM DATA:- 238 SMCLOCK:- 118 BA:- 82,190

SPDVDD:- 236 Vref:- 1 CS:- 193 CKE:- 50,93,94 DCLK:- 184,185

VTT:- 120,240

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