MS-7918 Ver: 1.0 ATX (243.84x304.8) mm

Intel Haswell Refresh Platform

CPU:Socket H3

2013 Haswell
2014 Boardwell

PCH:FCBGA708

Z97/H97/B85
SPI ROM: 64 MB
128 MB (H97/B85)

Main Memory:

*Dual Channel DDR3 * 4 (Max 32G)*

Power Solution:

Vcore : UP1649 6 Phase
DDR : UP1504

ACPI:

UPI

Onboard Chip:

LAN : Killer E2205
PCI Brige : ASM1083
HD Codec:ALC1150 + AMP (Gaming Type)
SIO:Nuvoton 6792D

Expansion Slots:

*PCI Express (X16) Slot * 1*
*PCI Express (X1) Slot * 2* >
*PCI Express (X4) Slot * 1* > *(Share Bandwidth)*
*PCI Slot * 3*
*M.2 Slot (Socket 3) * 1 (Share SATA)*

Internal Connectors

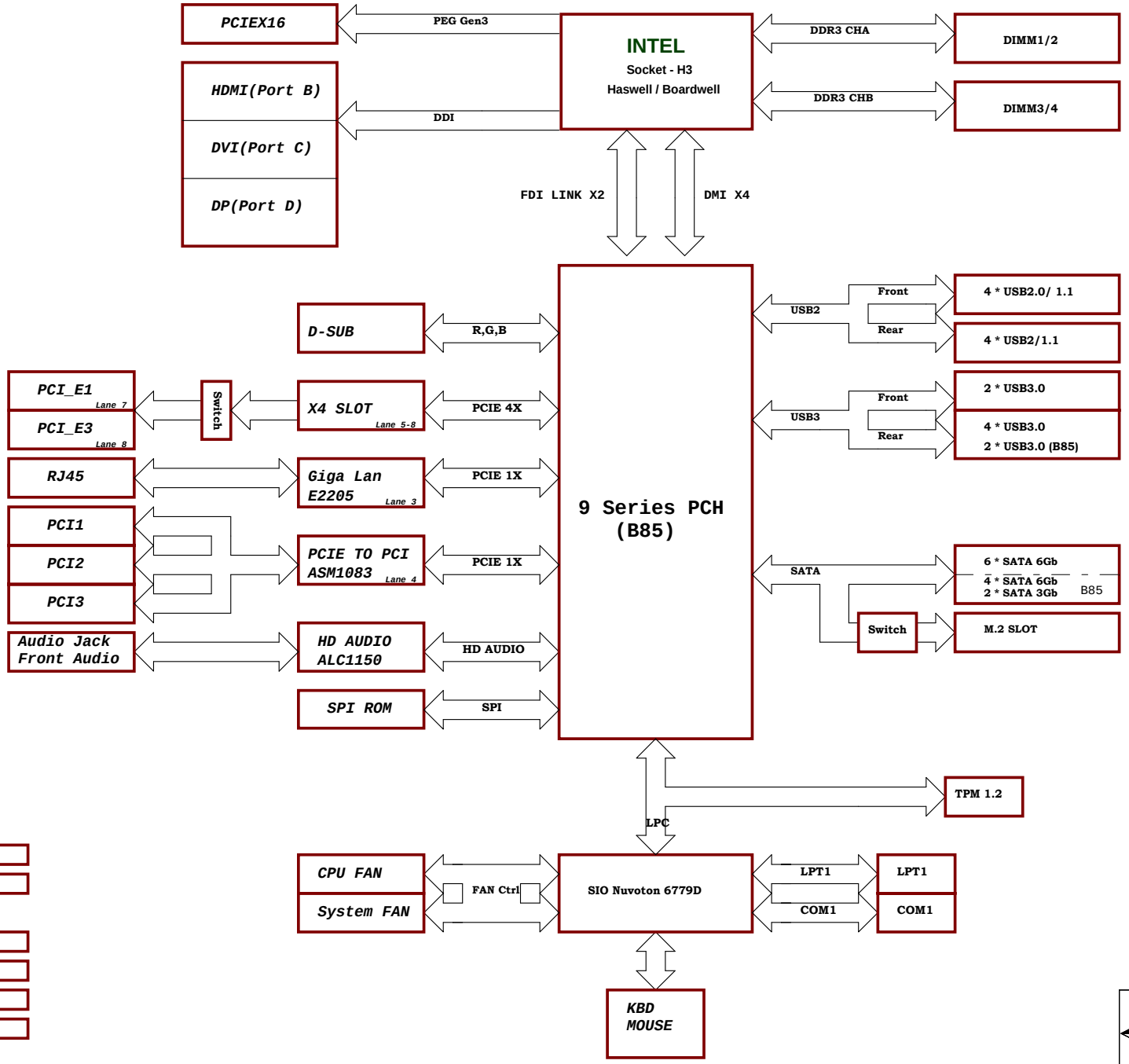
*SATA Gen3 * 6*
*FUSB2 Header * 2*
*FUSB3 Header * 1*
*Front Audio Header * 1*
*Serial Port Header * 1*
*Parallel Port Header * 1*
*Front Panel Header * 2*
*SPI Header * 1*
*TPM Header * 1*
*CPU Fan * 2*
*System Fan * 2*

Real I/O Connectors

PS2 + Dual USB2
Dual USB3 (B85 USB2)
DSUB + DVI
DP + HDMI + SPDIF
RJ45 + Dual USB3
Audio Jack 6 Port

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7918	
Size: Custom	Document Description: Cover Sheet	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 1 of 53	

MS-7918
Block Diagram



Slot Sequence:

- PCIE X1
- M.2 Slot
- PCIE X16
- PCIE X1
- PCI SLOT
- PCIE X16(X4)
- PCI SLOT
- PCI SLOT

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Size: Custom | Document Description: Block Diagram | Rev: 1.0

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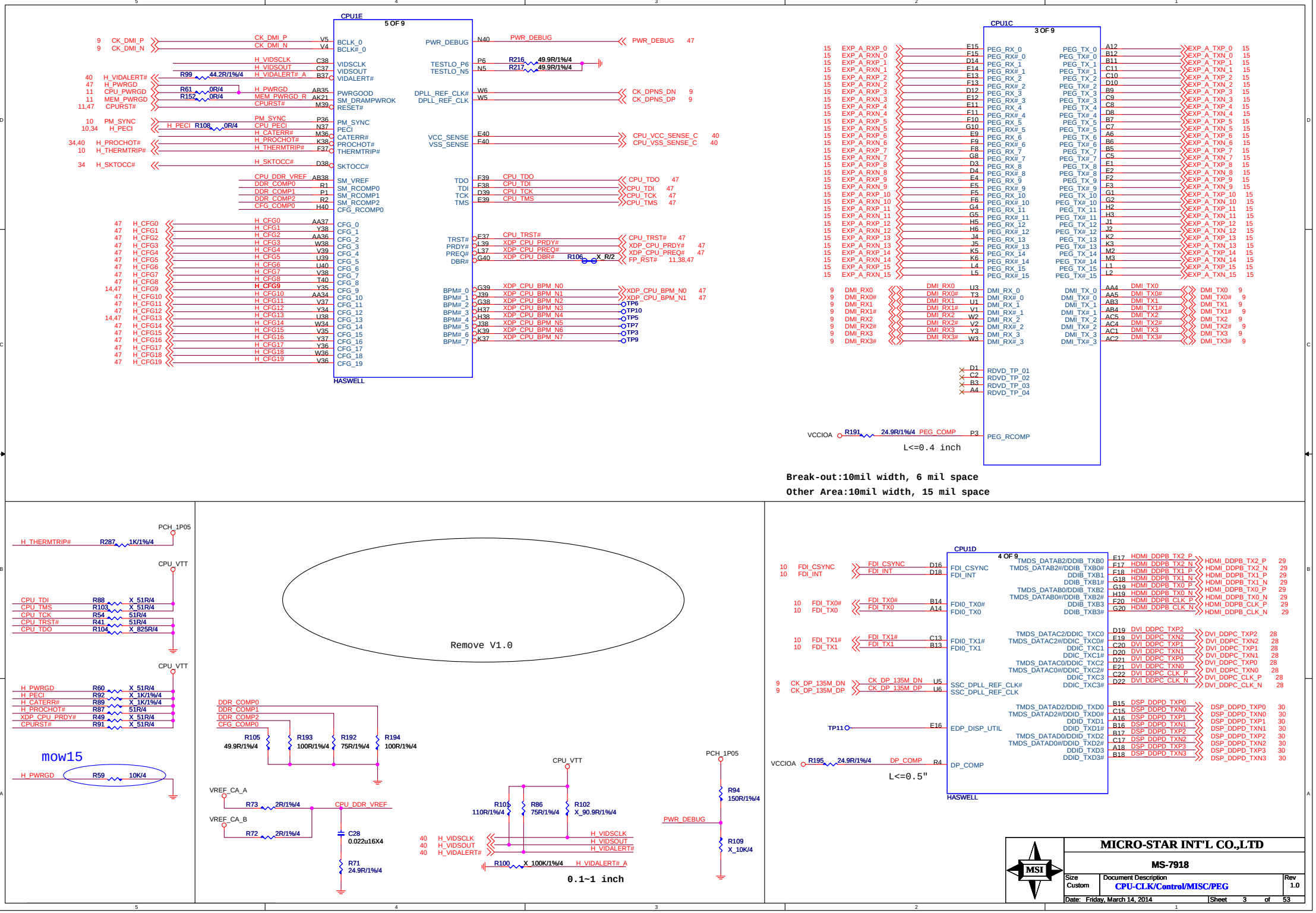
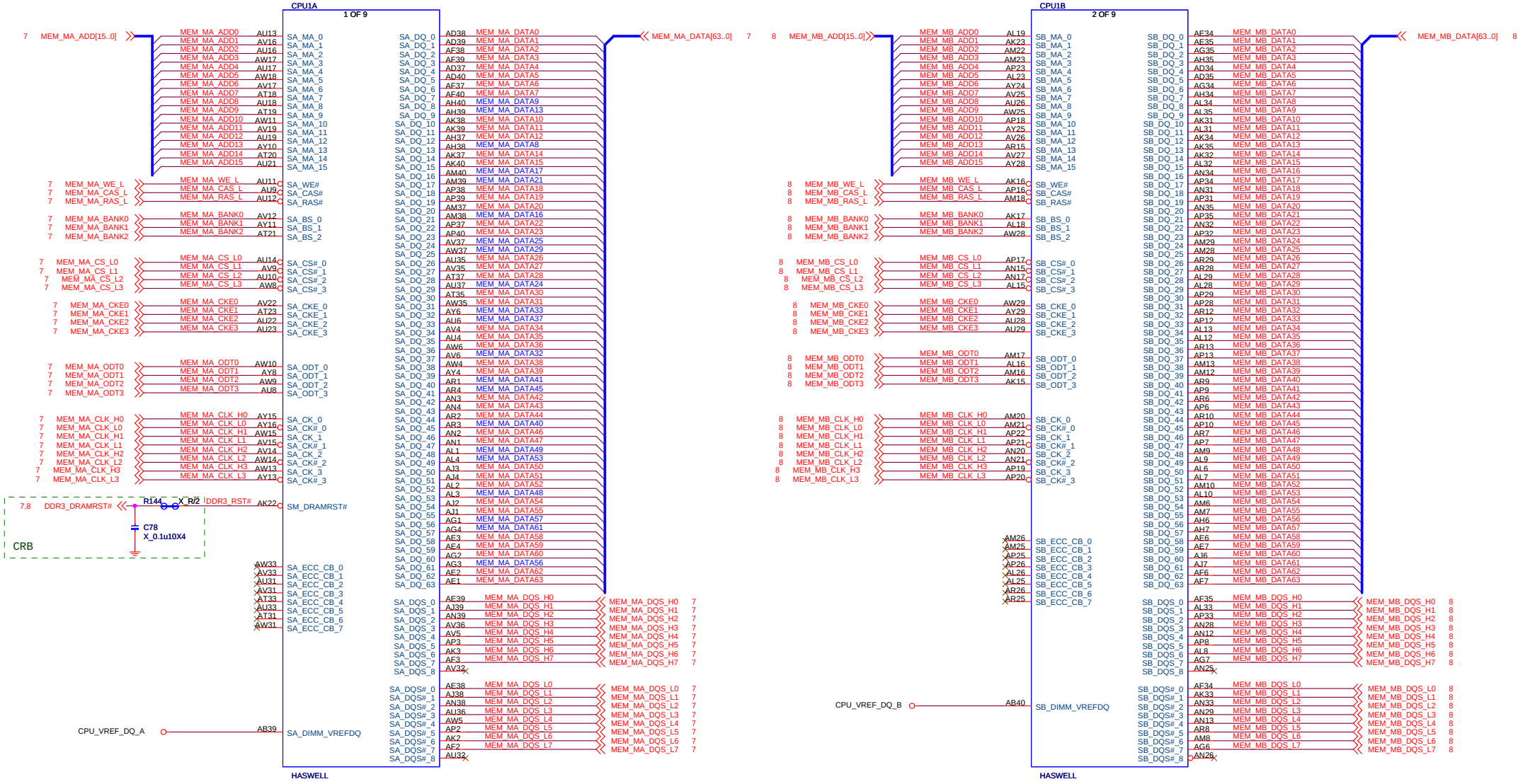

CPU1E
5 OF 9
HASWELL
CPU1C
3 OF 9
CPU1D
4 OF 9
Remove V1.0
mow15
0.1~1 inch
L<=0.4 inch
L<=0.5"
Break-out:10mil width, 6 mil space
Other Area:10mil width, 15 mil space
MICRO-STAR INT'L CO.,LTD
MS-7918
CPU-CLK/Control/MISC/PEG
Date: Friday, March 14, 2014
Sheet 3 of 53



MICRO-STAR INT'L CO.,LTD		
MS-7918		
Size: Custom	Document Description: CPU-Memory	Rev: 1.0
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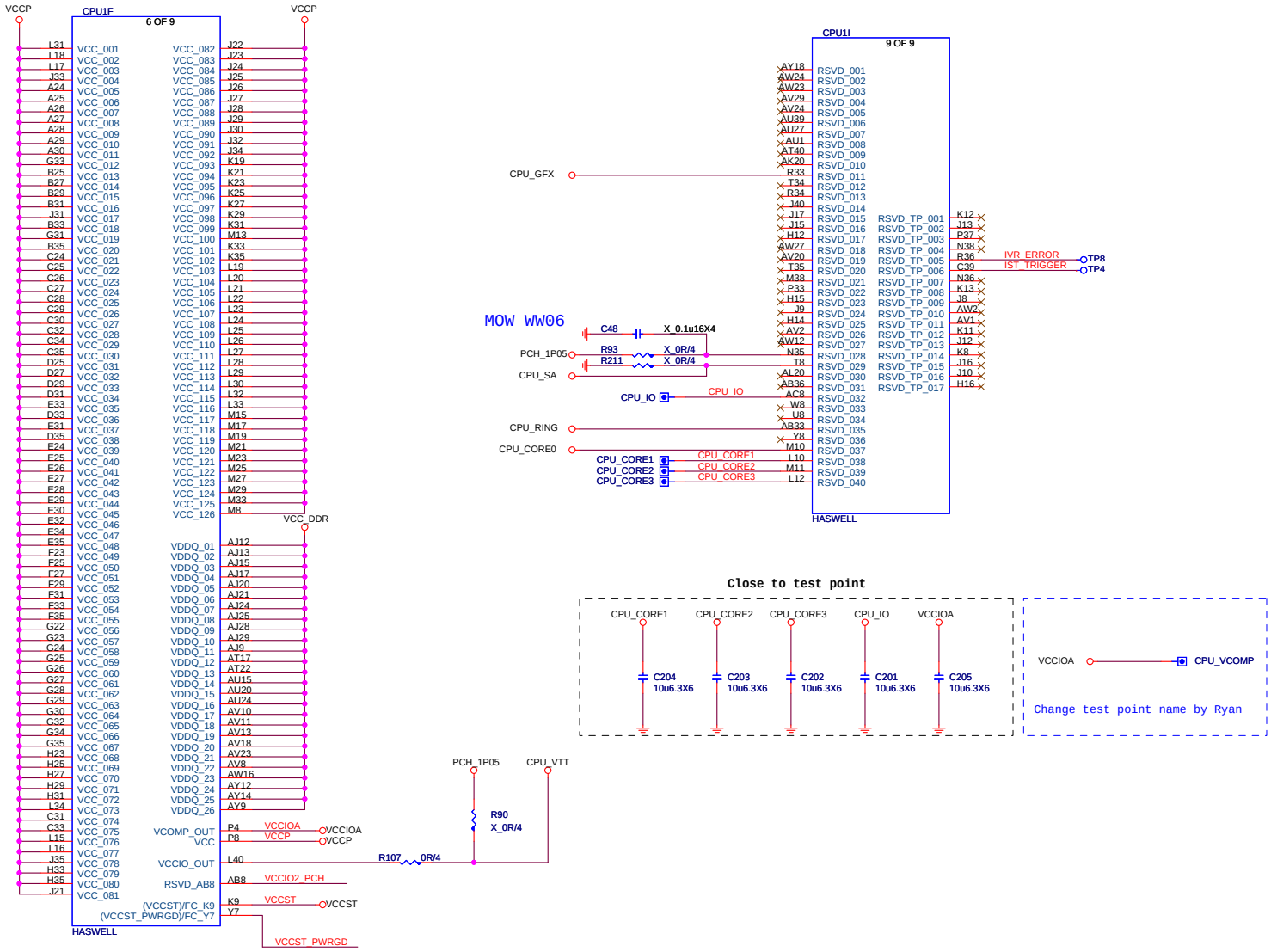
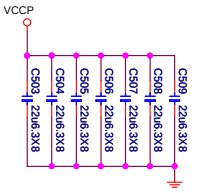
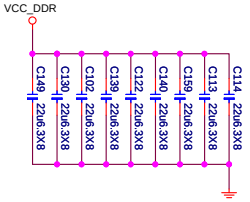


+CPU_VCCP-Decoupling



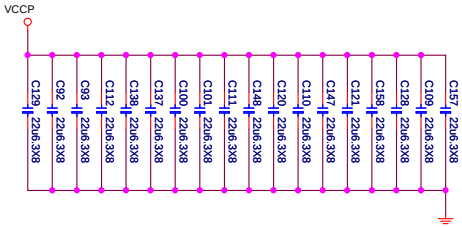
PLACE 0805 CAPS IN CPU SOCKET BOTTOM

+1.5V_DDR3-Decoupling



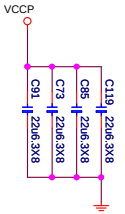
CPU SOCKET CAVITY 0805CAPS

+CPU_VCCP-Decoupling

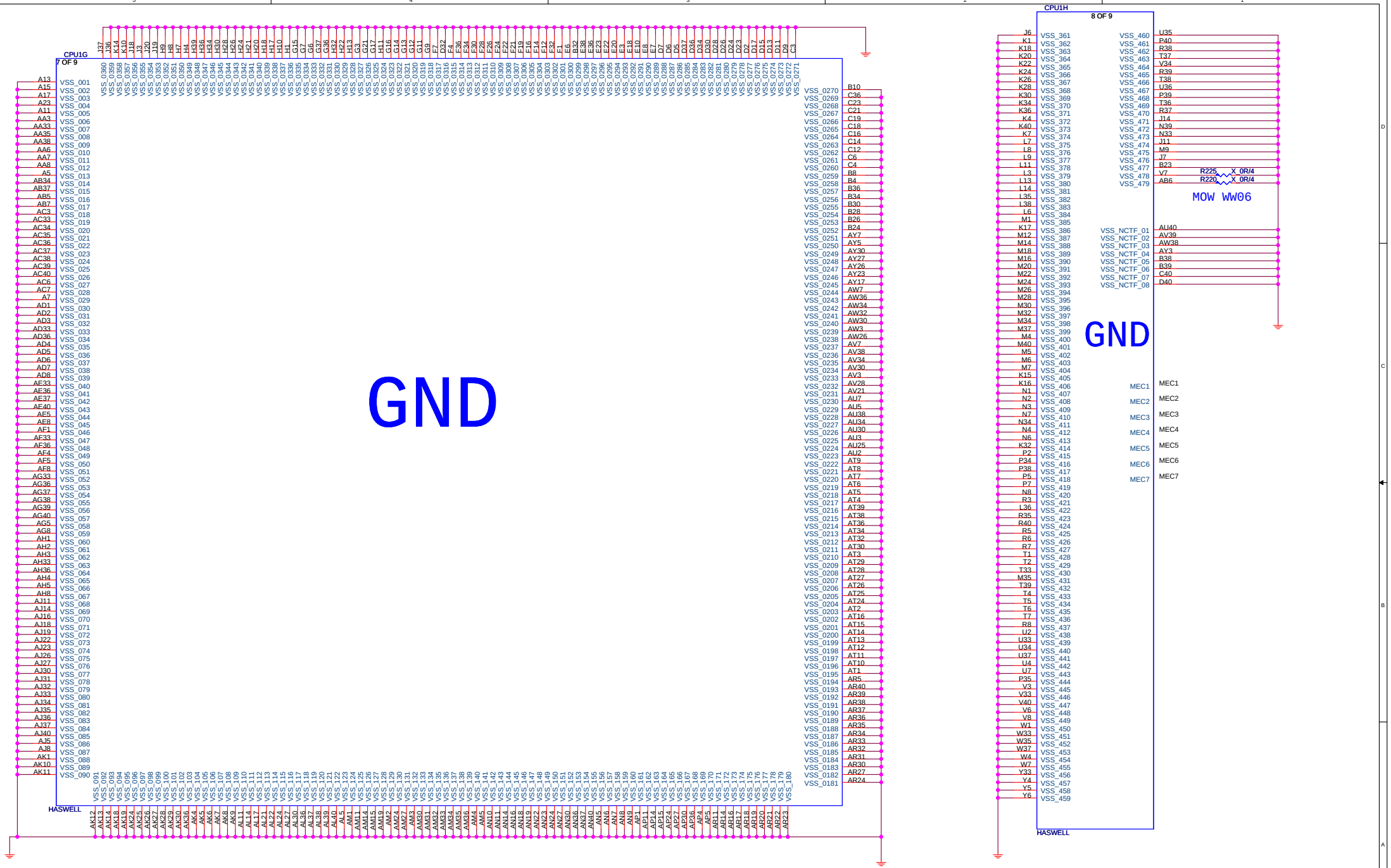


PLACE 0805CAPS INSIDE CPU SOCKET CAVITY

PLACE 0805CAPS Near CPU SOCKET edge



MICRO-STAR INT'L CO.,LTD		
MS-7918		
Size: Custom	Document Description: CPU-Power	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 5 of 53	



MICRO-STAR INT'L CO.,LTD	
MS-7918	
Size: Custom	Document Description: CPU-GND
Rev: 1.0	
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DDRIII DIMM_A0

DDRIII DIMM_A1

DDR3

DDR3

DIMM2(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

DIMM1(CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]

Place close to DIMM1

Place close to DIMM1 with DIMM2

Place close to DIMM2

UPI VOLTAGE CONSOLE

UPI VOLTAGE CONSOLE

MICRO-STAR INT'L CO.,LTD	
MS-7918	
Size: Custom	Document Description: DDR3-DIMM 1 / DIMM 2
Rev: 1.0	
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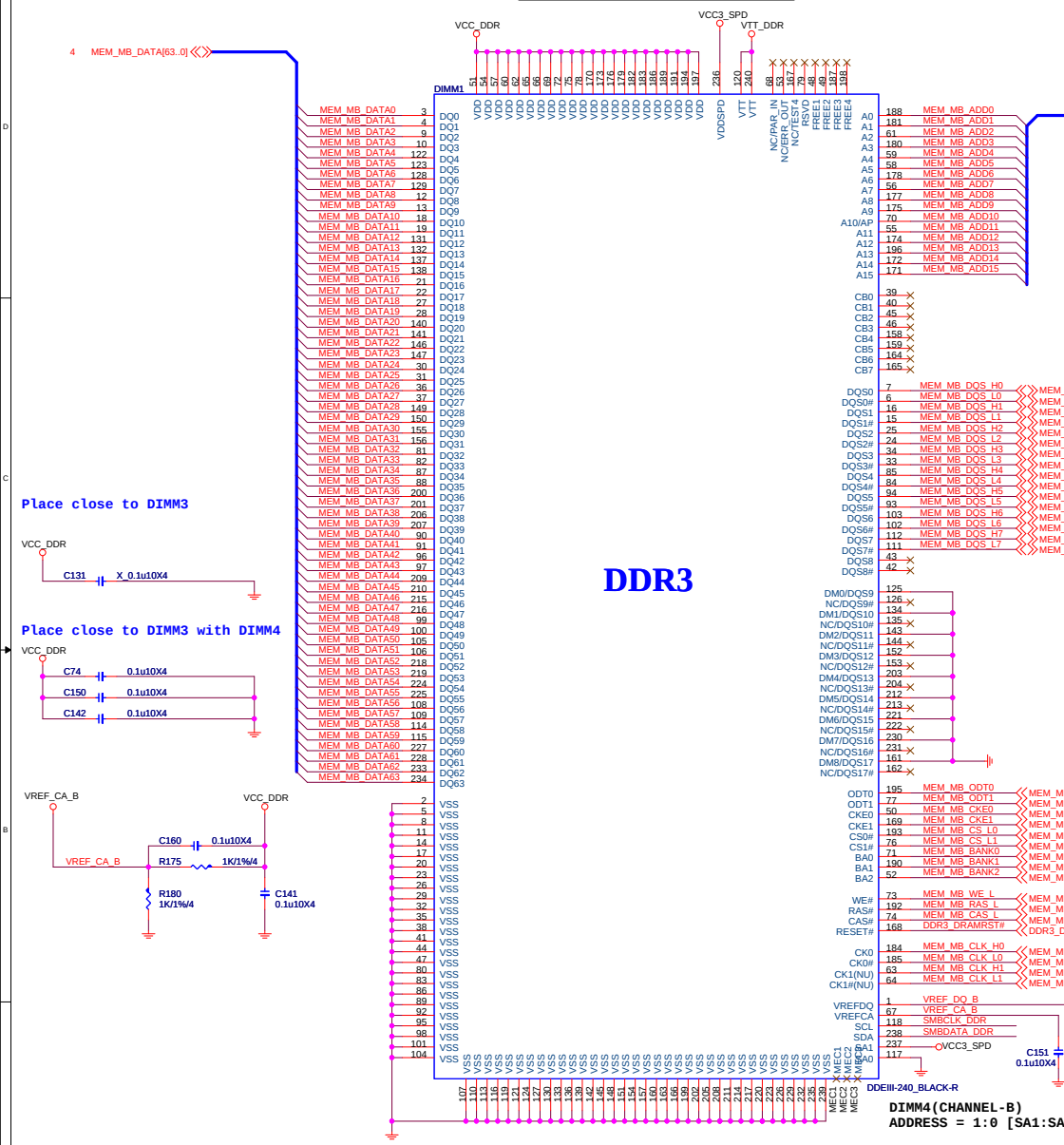
DDRIII DIMM_B0



DDRIII DIMM_B1

MICRO-STAR INT'L CO.,LTD			
MS-7918			
Size: Custom	Document Description: DDR3-DIMM 3 / DIMM 4		Rev: 1.0
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B85
USB2 Port 6,7 Disable
USB3 Port 2, 3 Only PCIE

Default
1X2 Port 5,6
2X1 Port 7,8

PCH1B
2 OF 8

PCI-E
USB(2.0)
USB(3.0)
DMI

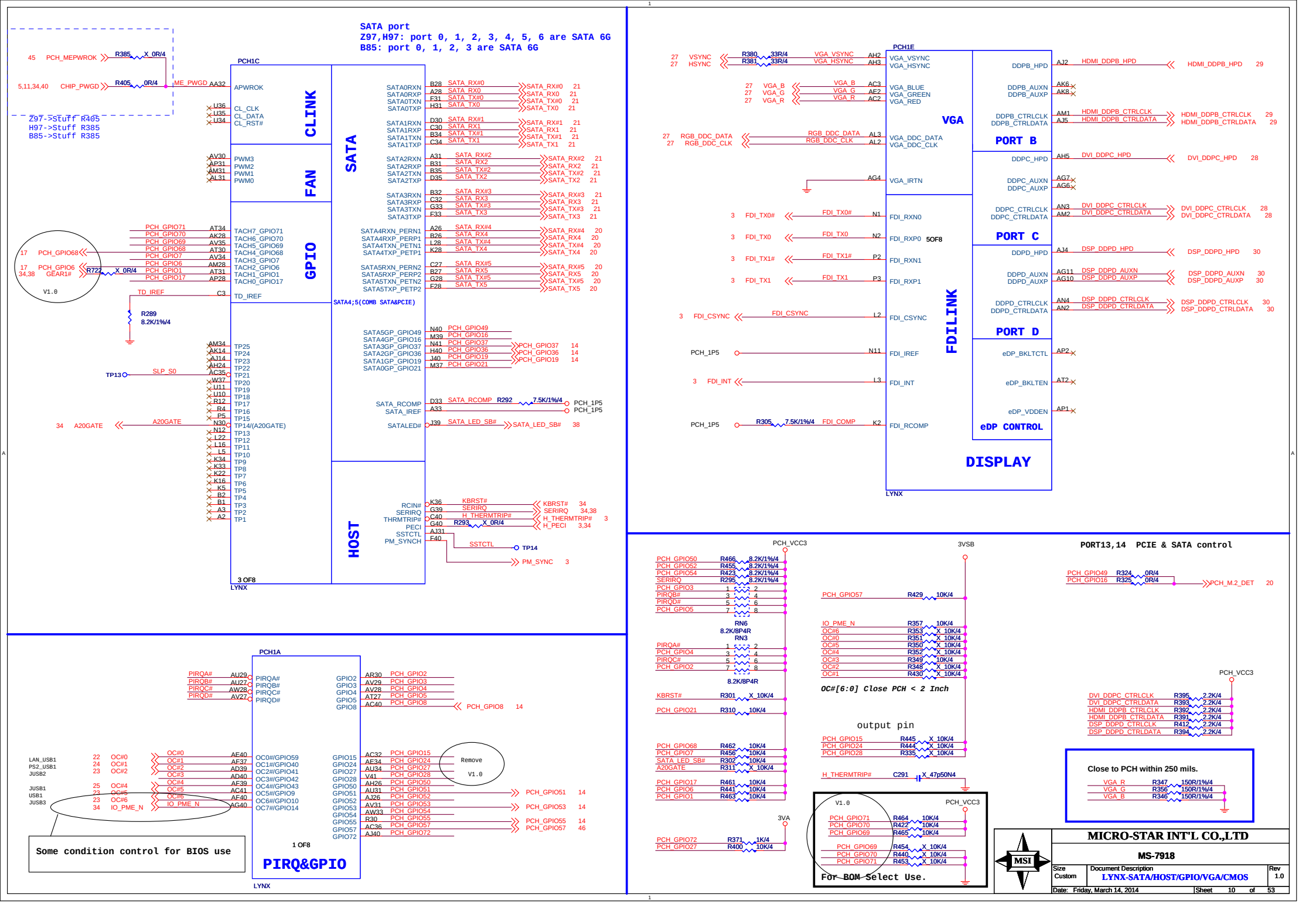
PCH1F
6 OF 8

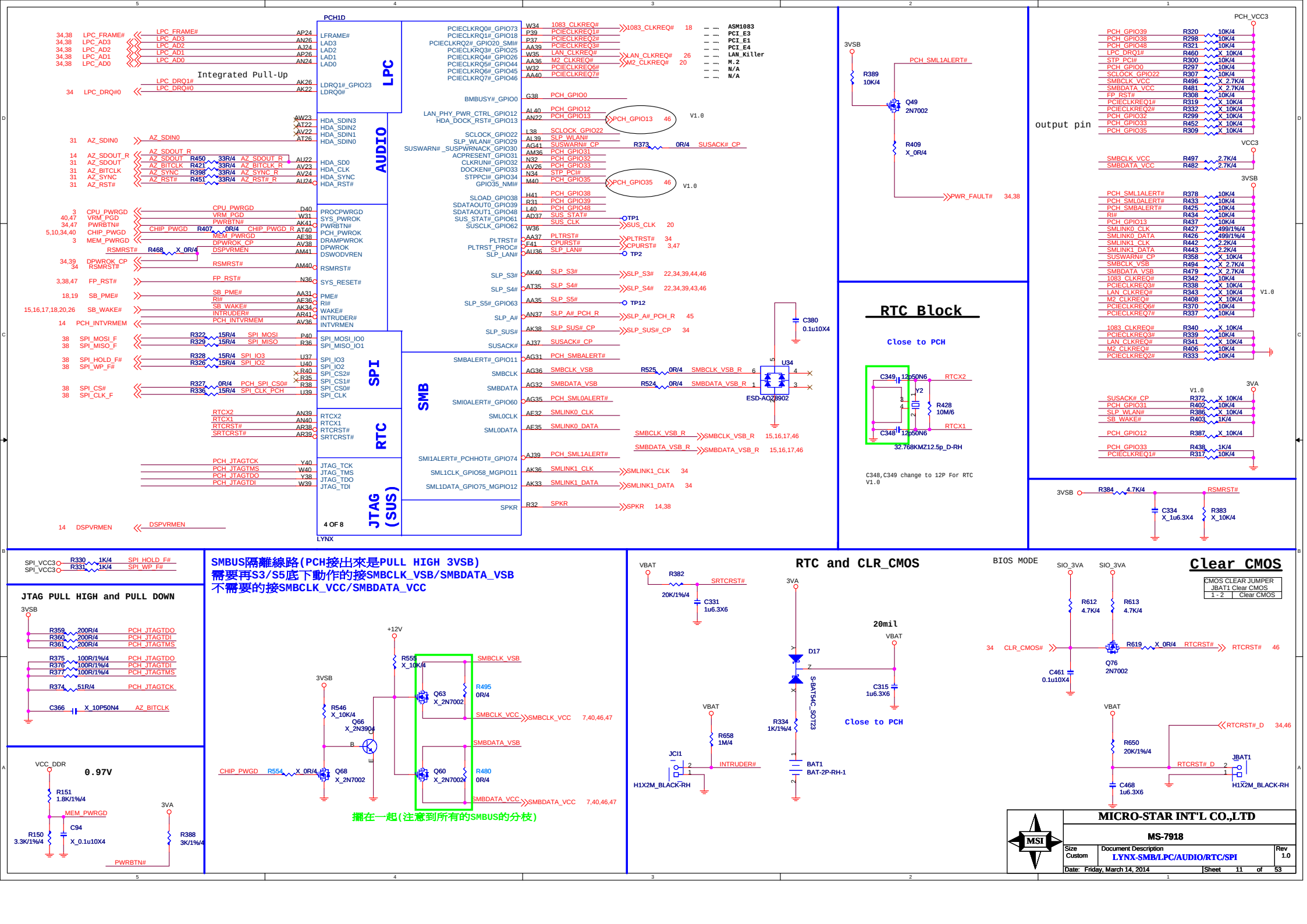
CLOCK
CLOCK_IN

LYNX

no clock gen pull down

EMI


SATA port
Z97,H97: port 0, 1, 2, 3, 4, 5, 6 are SATA 6G
B85: port 0, 1, 2, 3 are SATA 6G
PCH1C
CLINK
FAN
GPIO
SATA
HOST
APWROK
CL_CLK
CL_DATA
CL_RST#
PWM3
PWM2
PWM1
PWM0
TACH7_GPIO71
TACH6_GPIO70
TACH5_GPIO69
TACH4_GPIO68
TACH3_GPIO7
TACH2_GPIO6
TACH1_GPIO1
TACH0_GPIO17
TD_IREF
SATA4;5(COMB SATA&PCIE)
TP25
TP24
TP23
TP22
TP21
TP20
TP19
TP18
TP17
TP16
TP15
TP14/(A20GATE)
TP13
TP12
TP11
TP10
TP9
TP8
TP7
TP6
TP5
TP4
TP3
TP2
TP1
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN_PERN1
SATA4RXP_PERP1
SATA4TXN_PETN1
SATA4TXP_PETP1
SATA5RXN_PERN2
SATA5RXP_PERP2
SATA5TXN_PETN2
SATA5TXP_PETP2
SATA5GP_GPIO49
SATA4GP_GPIO16
SATA3GP_GPIO37
SATA2GP_GPIO36
SATA1GP_GPIO19
SATA0GP_GPIO21
SATA_RCOMP
SATA_IREF
SATALED#
RCIN#
SERIRQ
THRMTRIP#
PECI
SSTCTL
PM_SYNCH
3 OF8
LYNX
R385 X_0R/4
R405 0R/4
ME_PWGD
45 PCH_MEPWROK
5,11,34,40 CHIP_PWGD
Z97->Stuff R405
H97->Stuff R385
B85->Stuff R385
17 PCH_GPIO68
17 PCH_GPIO6
34,38 GEAR1#
R722 X_0R/4
V1.0
R289 8.2K/1%/4
TP13 SLP_S0
34 A20GATE
A20GATE
R292 7.5K/1%/4
PCH_1P5
SATA_LED_SB#
38
SSTCTL
TP14
PM_SYNC 3
KBRST#
SERIRQ 34,38
H_THERMTRIP# 3
H_PECI 3,4
R293 X_0R/4
PCH1E
VGA
PORT B
PORT C
PORT D
eDP CONTROL
FDILINK
DISPLAY
VGA_VSYNC
VGA_HSYNC
VGA_BLUE
VGA_GREEN
VGA_RED
VGA_DDC_DATA
VGA_DDC_CLK
VGA_IRTN
FDI_RXN0
FDI_RXP0
FDI_RXN1
FDI_RXP1
FDI_CSYNC
FDI_IREF
FDI_INT
FDI_RCOMP
5OF8
R380 33R/4
R381 33R/4
27 VSYNC
27 HSYNC
27 VGA_B
27 VGA_G
27 VGA_R
27 RGB_DDC_DATA
27 RGB_DDC_CLK
3 FDI_TX0#
3 FDI_TX0
3 FDI_TX1#
3 FDI_TX1
3 FDI_CSYNC
PCH_1P5
3 FDI_INT
R305 7.5K/1%/4 FDI_COMP
DDPB_HPD
DDPB_AUXN
DDPB_AUXP
DDPB_CTRLCLK
DDPB_CTRLDATA
DDPC_HPD
DDPC_AUXN
DDPC_AUXP
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPD_HPD
DDPD_AUXN
DDPD_AUXP
DDPD_CTRLCLK
DDPD_CTRLDATA
eDP_BKLTCTL
eDP_BKLTEN
eDP_VDDEN
HDMI_DDPB_HPD
DVI_DDPC_HPD
DSP_DDPD_HPD
DSP_DDPD_AUXN
DSP_DDPD_AUXP
DSP_DDPD_CTRLCLK
DSP_DDPD_CTRLDATA
LYNX
PCH_VCC3
3VSB
3VA
PCH_GPIO50 R466 8.2K/1%/4
PCH_GPIO52 R455 8.2K/1%/4
PCH_GPIO54 R423 8.2K/1%/4
SERIRQ R295 8.2K/1%/4
PCH_GPIO3
PIRQB#
PIRQD#
PCH_GPIO5
RN6
8.2K/8P4R
RN3
PIRQA#
PCH_GPIO4
PIRQC#
PCH_GPIO2
8.2K/8P4R
KBRST# R301 X_10K/4
PCH_GPIO21 R310 10K/4
PCH_GPIO68 R462 10K/4
PCH_GPIO7 R456 10K/4
SATA_LED_SB# R302 10K/4
A20GATE R311 X_10K/4
PCH_GPIO17 R461 10K/4
PCH_GPIO6 R441 10K/4
PCH_GPIO1 R463 10K/4
PCH_GPIO72 R371 1K/4
PCH_GPIO27 R400 10K/4
PCH_GPIO57 R429 10K/4
IO_PME_N R357 10K/4
OC#6 R353 X_10K/4
OC#0 R351 X_10K/4
OC#5 R350 X_10K/4
OC#4 R352 X_10K/4
OC#3 R349 10K/4
OC#2 R348 X_10K/4
OC#1 R430 X_10K/4
OC#[6:0] Close PCH < 2 Inch
output pin
PCH_GPIO15 R445 X_10K/4
PCH_GPIO24 R444 X_10K/4
PCH_GPIO28 R335 X_10K/4
H_THERMTRIP# C291 X_47p50N4
V1.0
PCH_GPIO71 R464 10K/4
PCH_GPIO70 R422 10K/4
PCH_GPIO69 R465 10K/4
PCH_GPIO69 R454 X_10K/4
PCH_GPIO70 R440 X_10K/4
PCH_GPIO71 R453 X_10K/4
For BOM Select Use.
PORT13,14 PCIE & SATA control
PCH_GPIO49 R324 0R/4
PCH_GPIO16 R325 0R/4
PCH_M.2_DET 20
DVI_DDPC_CTRLCLK R395 2.2K/4
DVI_DDPC_CTRLDATA R393 2.2K/4
HDMI_DDPB_CTRLCLK R392 2.2K/4
HDMI_DDPB_CTRLDATA R391 2.2K/4
DSP_DDPD_CTRLCLK R412 2.2K/4
DSP_DDPD_CTRLDATA R394 2.2K/4
Close to PCH within 250 mils.
VGA_R R347 150R/1%/4
VGA_G R356 150R/1%/4
VGA_B R346 150R/1%/4
PCH1A
PIRQ&GPIO
1 OF8
LYNX
PIRQA# AU29
PIRQB# AU27
PIRQC# AW28
PIRQD# AV27
GPIO2 AR30 PCH_GPIO2
GPIO3 AV29 PCH_GPIO3
GPIO4 AV28 PCH_GPIO4
GPIO5 AT27 PCH_GPIO5
GPIO8 AC40 PCH_GPIO8 14
LAN_USB1 22 OC#0
PS2_USB1 24 OC#1
JUSB2 23 OC#2
JUSB1 25 OC#4
USB1 23 OC#5
JUSB3 23 OC#6
34 IO_PME_N
OC0#/GPIO59 AE40
OC1#/GPIO40 AE37
OC2#/GPIO41 AD39
OC3#/GPIO42 AD40
OC4#/GPIO43 AE39
OC5#/GPIO9 AC41
OC6#/GPIO10 AE40
OC7#/GPIO14 AG40
GPIO15 AC32 PCH_GPIO15
GPIO24 AE34 PCH_GPIO24
GPIO27 AU34 PCH_GPIO27
GPIO28 V41 PCH_GPIO28
GPIO50 AH26 PCH_GPIO50
GPIO51 AU31 PCH_GPIO51 PCH_GPIO51 14
GPIO52 AJ26 PCH_GPIO52
GPIO53 AV31 PCH_GPIO53 PCH_GPIO53 14
GPIO54 AW33 PCH_GPIO54
GPIO55 R30 PCH_GPIO55 PCH_GPIO55 14
GPIO57 AC36 PCH_GPIO57 PCH_GPIO57 46
GPIO72 AJ40 PCH_GPIO72
Remove
V1.0
Some condition control for BIOS use
MICRO-STAR INT'L CO.,LTD
MS-7918
Size Custom
Document Description
LYNX-SATA/HOST/GPIO/VGA/CMOS
Rev 1.0
Date: Friday, March 14, 2014
Sheet 10 of 53


PCH1D
LPC
AUDIO
SPI
RTC
JTAG (SUS)
SMB
LYNX
4 OF 8
Integrated Pull-Up
LPC_FRAME#
LPC_AD3
LPC_AD2
LPC_AD1
LPC_AD0
LPC_DRQ1#
LPC_DRQ#0
AZ_SDIN0
AZ_SDOUT_R
AZ_SDOUT
AZ_BITCLK
AZ_SYNC
AZ_RST#
CPU_PWRGD
VRM_PGD
PWRBTN#
CHIP_PWGD
MEM_PWRGD
DPWROK_CP
RSMRST#
SB_PME#
RI#
SB_WAKE#
INTRUDER#
PCH_INTVRMEM
SPI_MOSI_F
SPI_MISO_F
SPI_HOLD_F#
SPI_WP_F#
SPI_CS#
SPI_CLK_F
FP_RST#
SYS_RESET#
DSPVRMEN
RTCX2
RTCX1
RTCRST#
SRTCRST#
PCH_JTAGTCK
PCH_JTAGTMS
PCH_JTAGTDO
PCH_JTAGTDI
1083_CLKREQ#
LAN_CLKREQ#
M2_CLKREQ#
SLP_WLAN#
SUSWARN#_CP
SLP_S3#
SLP_S4#
SLP_S5#
SLP_A#
SLP_SUS#
SUSACK#
SMBCLK_VSB
SMBDATA_VSB
SMLINK0_CLK
SMLINK0_DATA
SMLINK1_CLK
SMLINK1_DATA
SPKR
PCH_SML1ALERT#
PCH_SMBALERT#
PCH_SML0ALERT#
TP1
TP2
ESD-AQ28902
C380
0.1u10X4
RTC Block
Close to PCH
C349
C348
Y2
R428
10M/6
32.768KMZ12.5p_D-RH
C348,C349 change to 12P For RTC
V1.0
output pin
PCH_VCC3
VCC3
3VSB
3VA
V1.0
R384
4.7K/4
C334
X_1u6.3X4
R383
X_10K/4
RSMRST#
JTAG PULL HIGH and PULL DOWN
SMBUS隔離線路(PCH接出來是PULL HIGH 3VSB)
需要再S3/S5底下動作的接SMBCLK_VSB/SMBDATA_VSB
不需要的接SMBCLK_VCC/SMBDATA_VCC
+12V
Q63
X_2N7002
Q66
X_2N3904
Q68
Q60
R495
0R/4
R480
R546
X_10K/4
R555
CHIP_PWGD
R554
摺在一起(注意到所有的SMBUS的分枝)
RTC and CLR_CMOS
VBAT
R382
20K/1%/4
C331
1u6.3X6
D17
S-BAT54C_SOT23
20mil
C315
1u6.3X6
R658
1M/4
JCI1
INTRUDER#
H1X2M_BLACK-RH
R334
1K/1%/4
BAT1
BAT-2P-RH-1
BIOS MODE
Clear CMOS
CMOS CLEAR JUMPER
JBAT1 Clear CMOS
1 - 2 Clear CMOS
R612
4.7K/4
R613
4.7K/4
CLR_CMOS#
R619
X_0R/4
RTCRST#
Q76
2N7002
C461
0.1u10X4
R650
20K/1%/4
C468
1u6.3X6
RTCRST#_D
JBAT1
VCC_DDR
0.97V
R151
1.8K/1%/4
C94
X_0.1u10X4
R150
3.3K/1%/4
R388
3K/1%/4
PWRBTN#
MICRO-STAR INT'L CO.,LTD
MS-7918
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Document Description
LYNX-SMB/LPC/AUDIO/RTC/SPI
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Change to 10UH if
VCCA_DPLLA/VCCA_DPLLB
has noise issue.

AF25 ;AD25 DT CRB0.7 ASW POWER

(Internal) 1.29A+(External)1.12A=2.41A

POWER

VCC3	0.21A
3VA	0.015A
VBAT	6uA
3VSB	0.261A
VCC1_5	0.249A
PCH_1P05	6A

PCH_VCC3 HAVE SEQENCING

AG1 DT CRB0.7 VCC3 POWER

(Internal) 0.261A+(External)0.261A=0.532A

Z97->Stuff
H97,B85->un-Stuff

Backside for V14,U12,T16,V16

unstuff

PCH decoupling cap

MICRO-STAR INT'L CO.,LTD	
MS-7918	
Size: Custom	Document Description: LYNX-POWER
Rev: 1.0	
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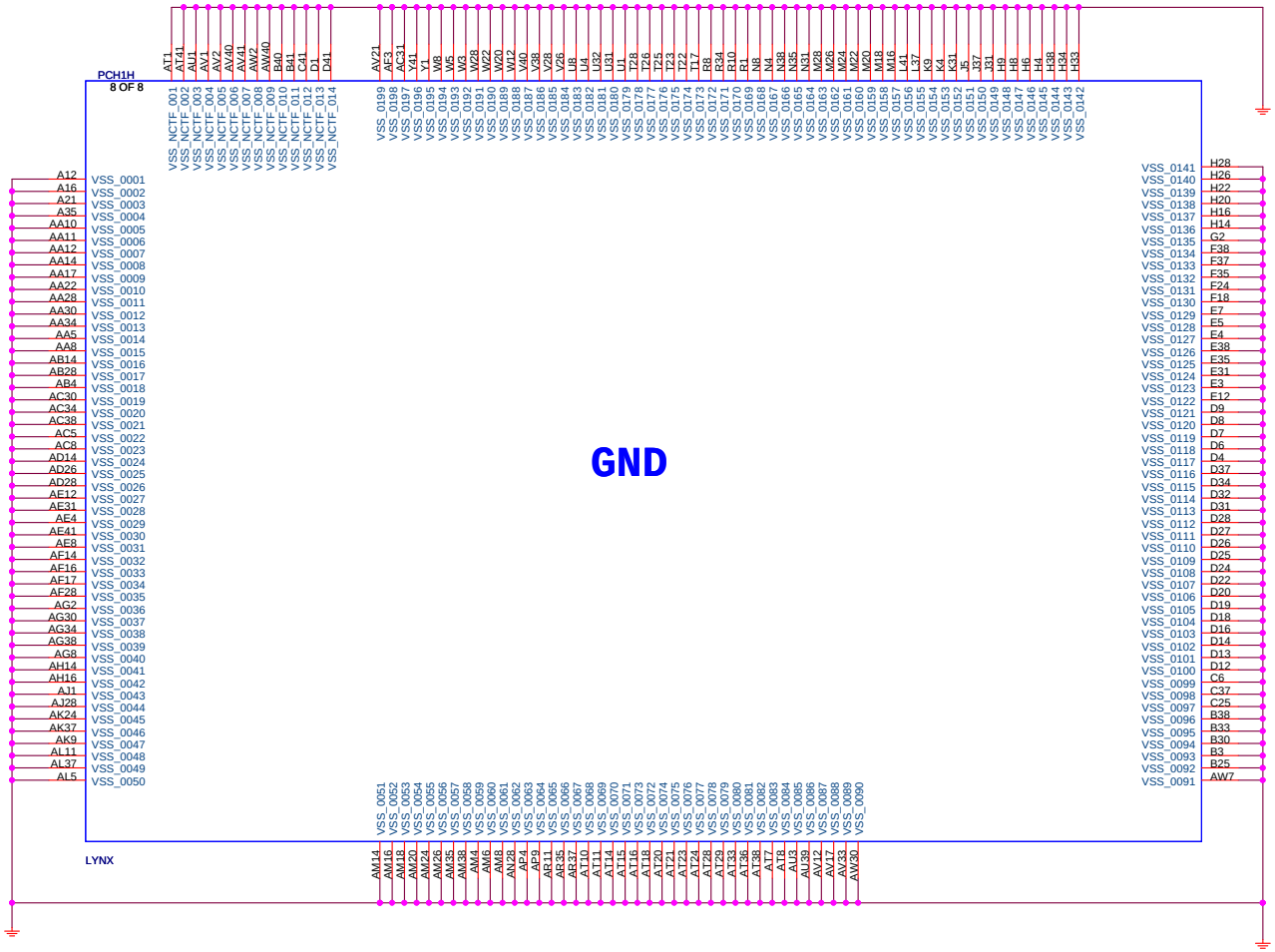
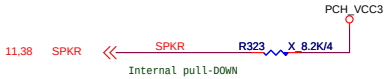
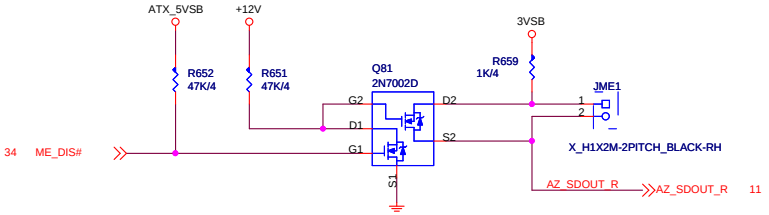


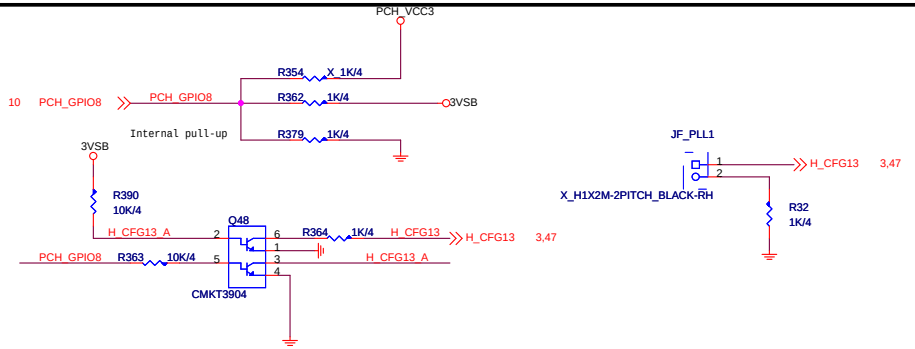
MICRO-STAR INT'L CO.,LTD		
MS-7918		
Size: Custom	Document Description: LYNX-GND	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 13 of 53	

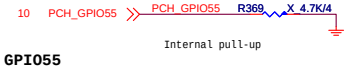


SPKR
Default Mode:
Internal weak Pull-down.

No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.

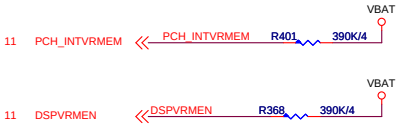


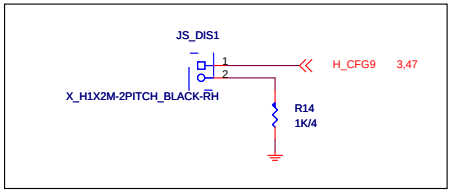




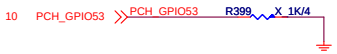
GPIO55
Default Mode:
Internal pull-up.

Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.

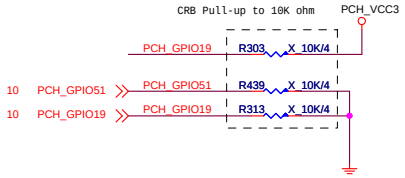




For Sx power Cycling May Fail Due to SVID Logic Race Condition Within the Processor



GPIO53
Connect to ground with 1k Ohm pull-down resistor.



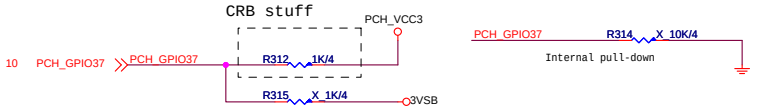
Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

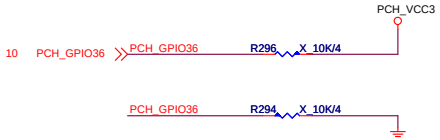
BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

Default



Enable TLS:
Pull up with 1k Ohm to VccSus3.3.

Default (Disable TLS):
Leave NC. Internal pull down.



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Size	Document Description	Rev
Custom	LYNX-Strap	1.0

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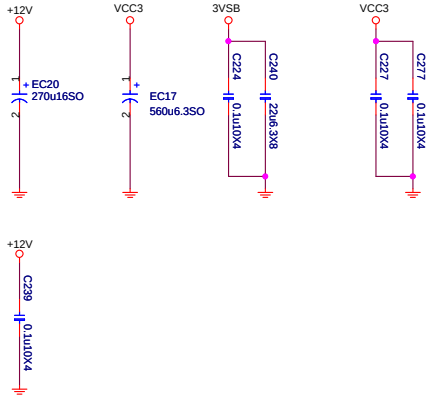
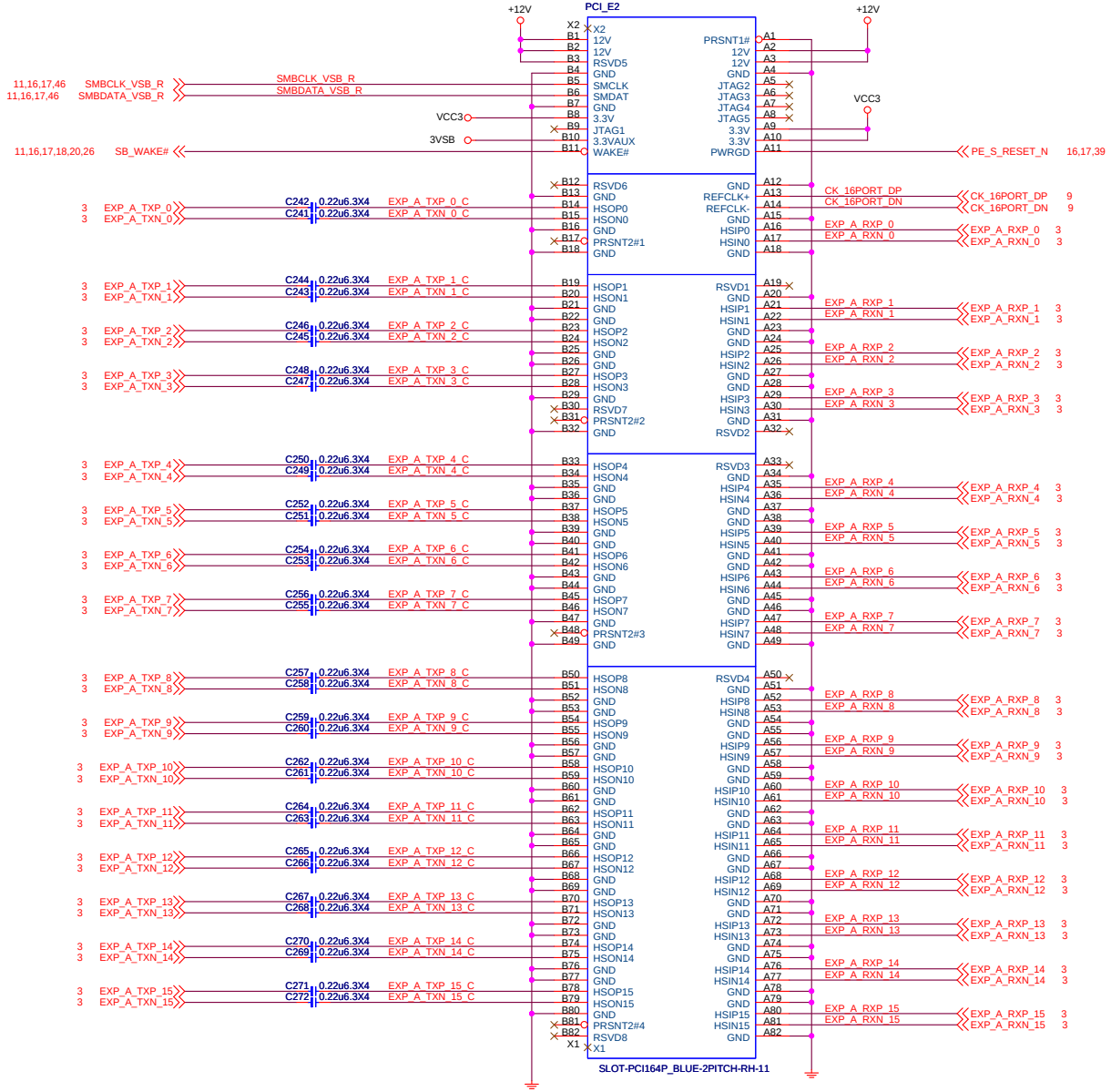
12V - 5.5A

VCC3 - 3A

3VSBV - 375mA





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MS-7918	
Size: Custom	Document Description: PCIE SLOT (X16)
Rev: 1.0	
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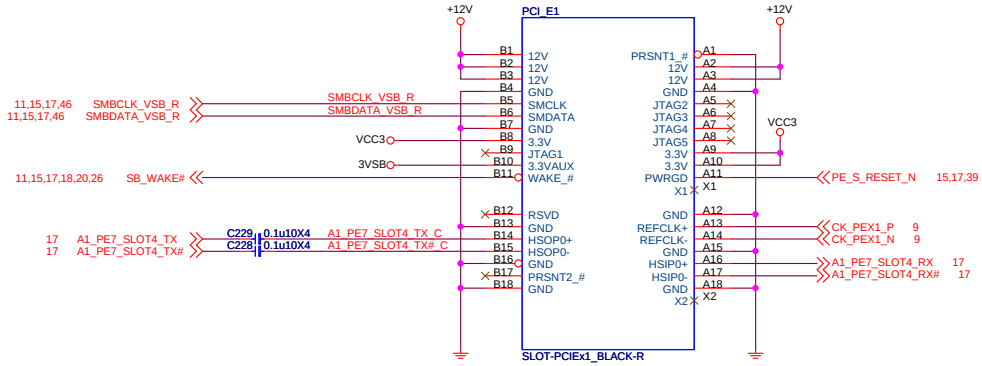
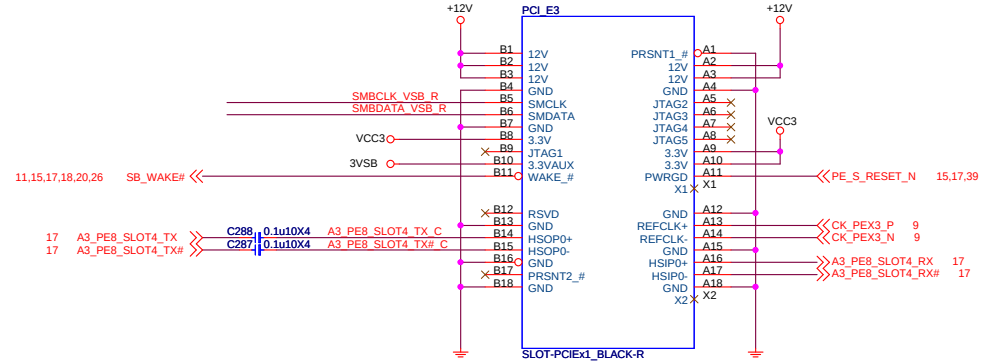


12V - 0.5A

VCC3 - 3A

3VSBV - 375mA



12V - 0.5A

VCC3 - 3A

3VSBV - 375mA

MICRO-STAR INT'L CO.,LTD

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Size: Custom | Document Description: PCIE SLOT (X1) | Rev: 1.0

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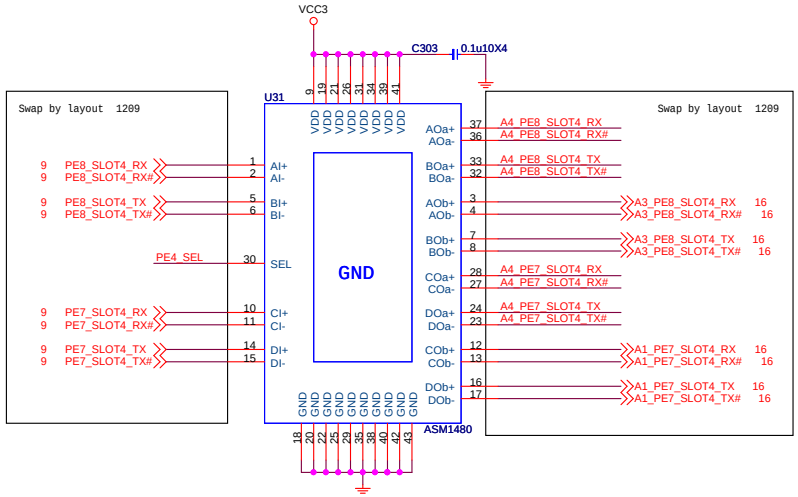
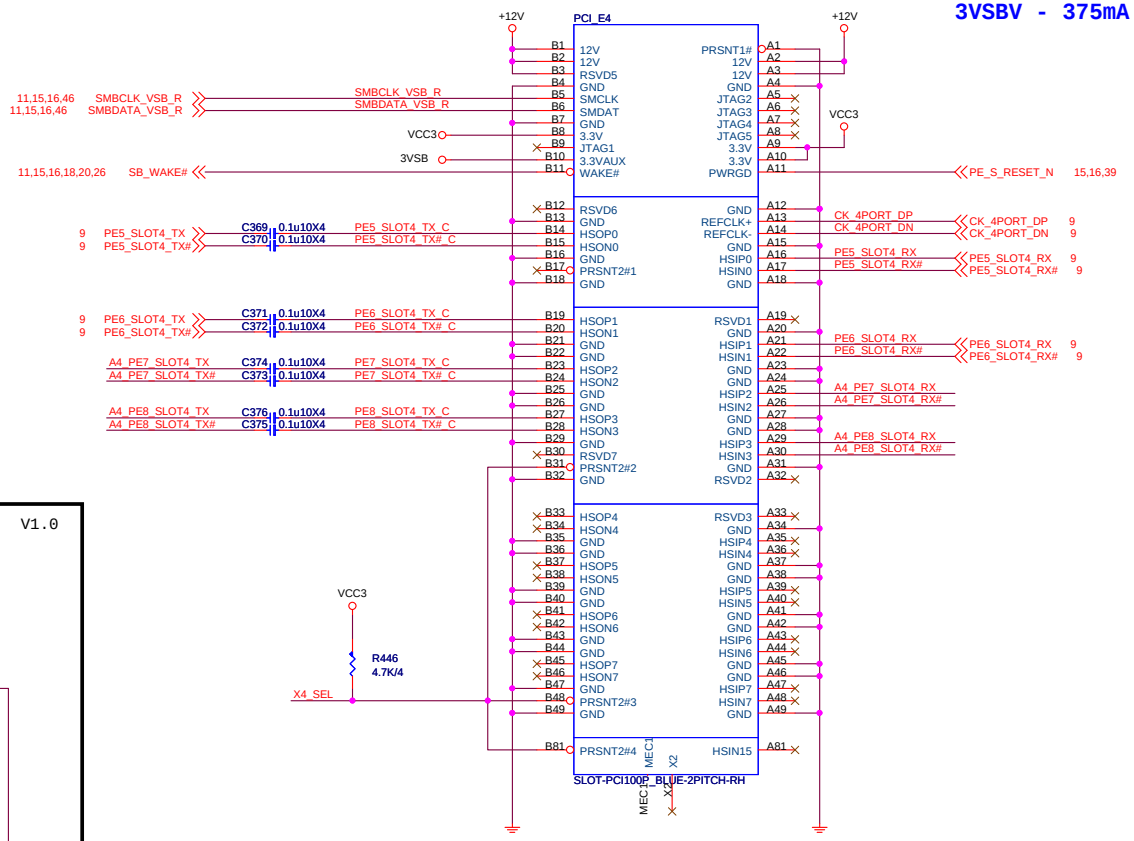
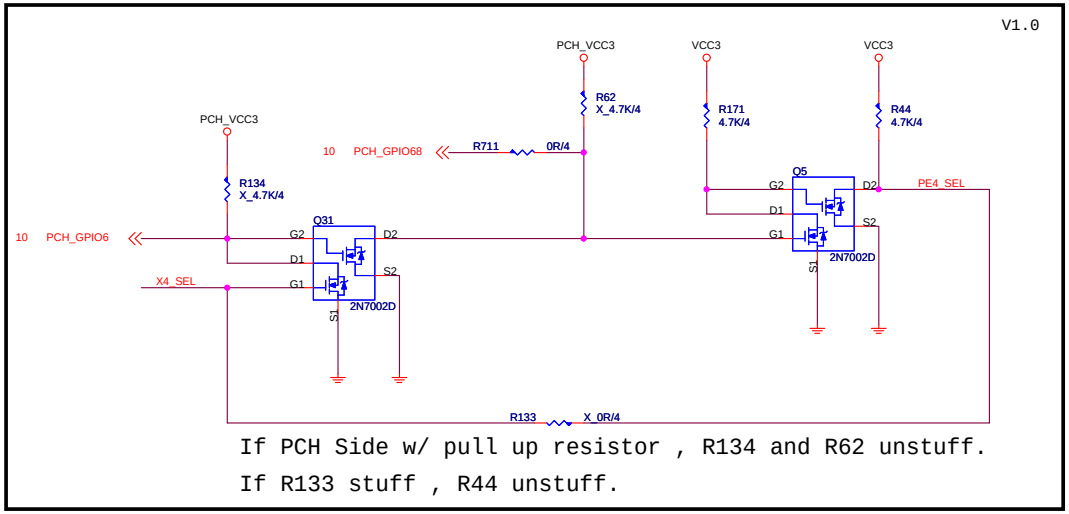
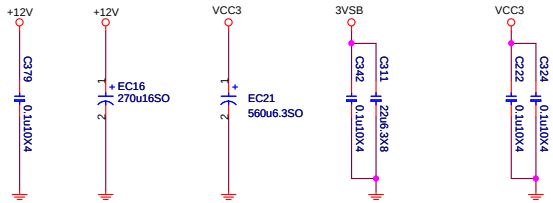
PCI_Express X4 Slot

12V - 2.1A
VCC3 - 3A
3VSBV - 375mA









Default PCI_E1,PCI_E3,PCI_E4 Working

	HW		SW	
	X2+1+1	X4	2+1+1	X4
X4_SEL	High	Low	X	X
PCH_GPIO6	Low	High	Low	Low
PCH_GPIO68	High (GPI)	Low (GPI)	High (GPO)	Low (GPO)

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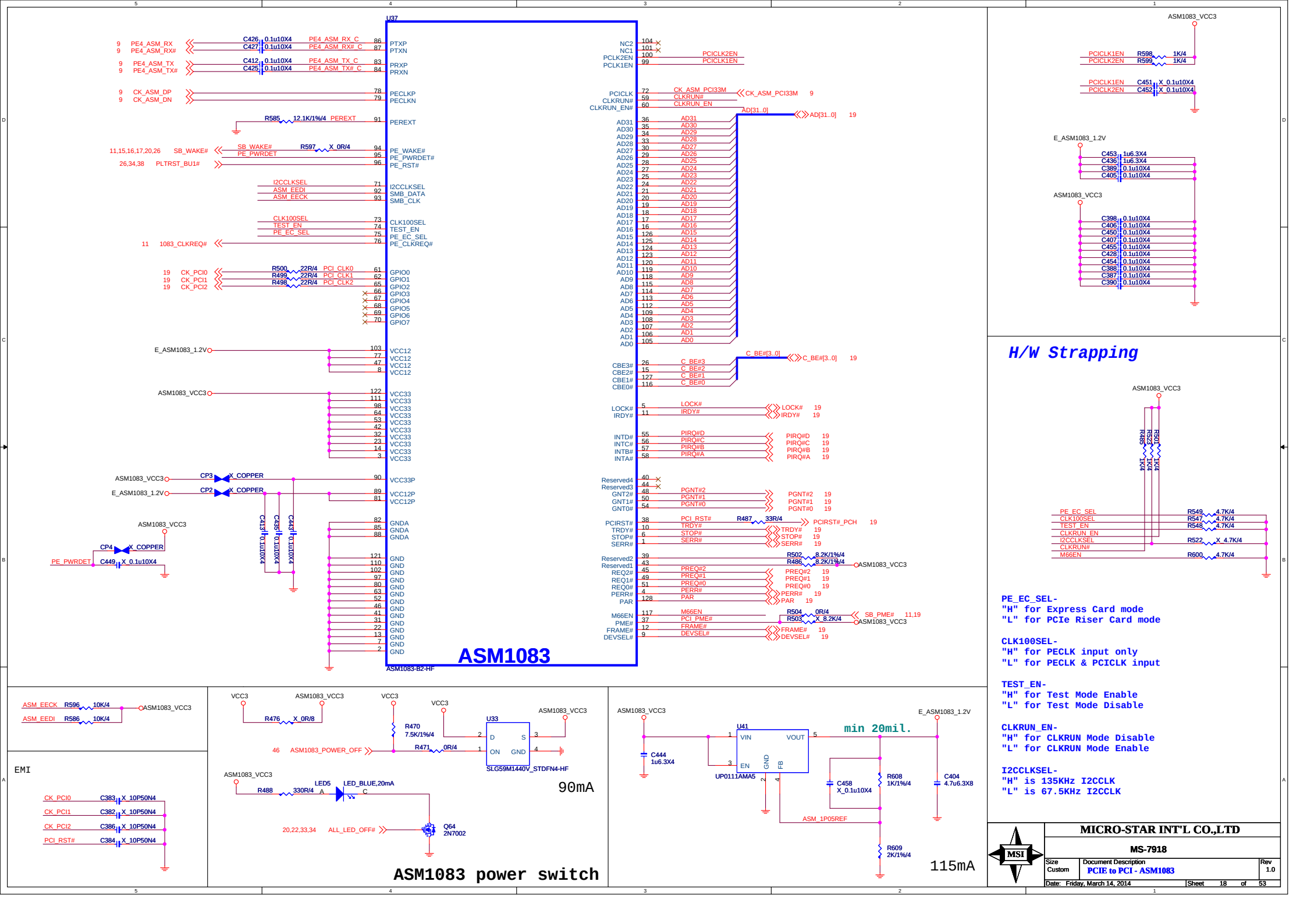
ASM1083
ASM1083-B2-HF
U37
PTXP
PTXN
PRXP
PRXN
PECLKP
PECLKN
PEREXT
PE_WAKE#
PE_PWRDET#
PE_RST#
I2CCLKSEL
SMB_DATA
SMB_CLK
CLK100SEL
TEST_EN
PE_EC_SEL
PE_CLKREQ#
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
VCC12
VCC33
VCC33P
VCC12P
GND
AD[31..0]
C_BE#[3..0]
LOCK#
IRDY#
PIRQ#D
PIRQ#C
PIRQ#B
PIRQ#A
PGNT#2
PGNT#1
PGNT#0
PCI_RST#
PCIRST#_PCH
TRDY#
STOP#
SERR#
PREQ#2
PREQ#1
PREQ#0
PERR#
PAR
M66EN
PCI_PME#
FRAME#
DEVSEL#
CK_ASM_PCI33M
PCICLK2EN
PCICLK1EN
H/W Strapping
PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode
CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input
TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable
CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable
I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK
EMI
ASM1083 power switch
90mA
115mA
min 20mil.
U33
SLG59M1440V_STDFN4-HF
U41
UP0111AMA5
LED_BLUE,20mA
Q64
2N7002
MICRO-STAR INT'L CO.,LTD
MS-7918
PCIE to PCI - ASM1083
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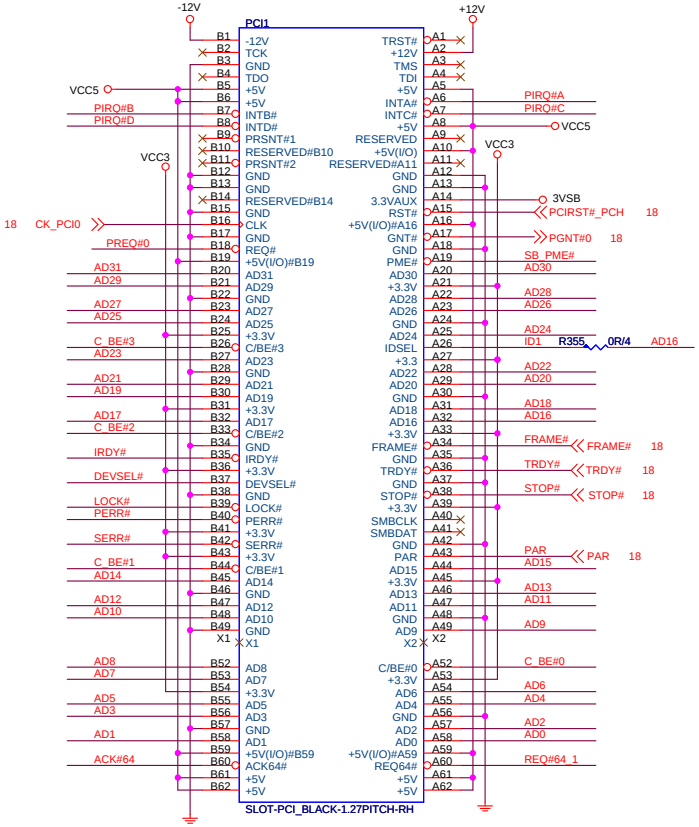
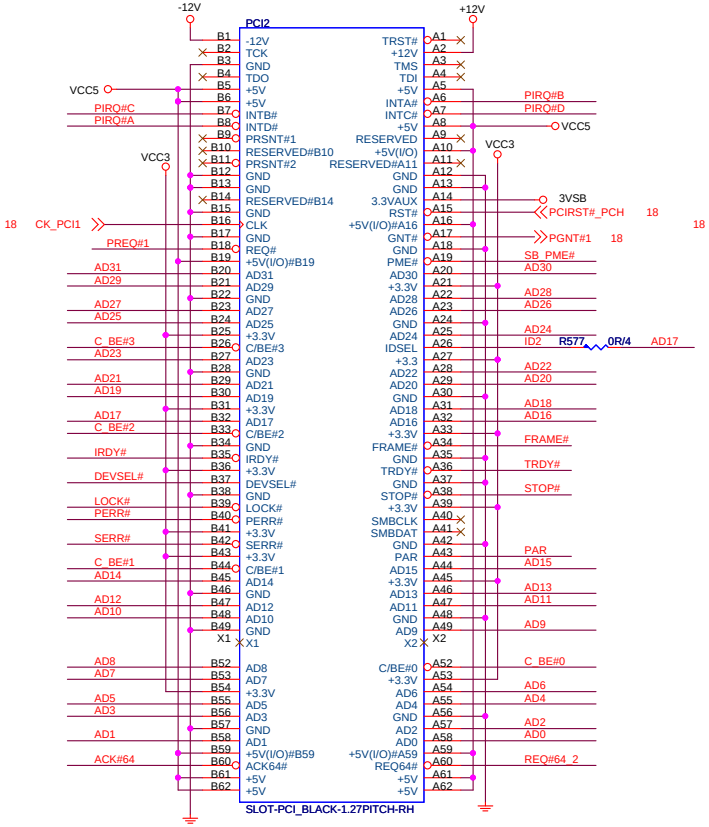
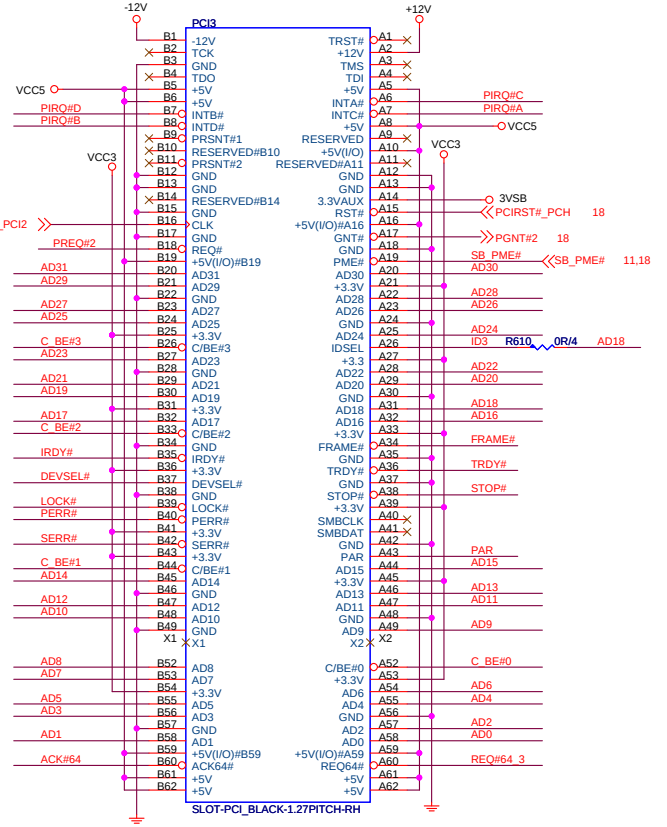


IDSEL = AD16
MASTER = PREQ#0
PIRQ#A



IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

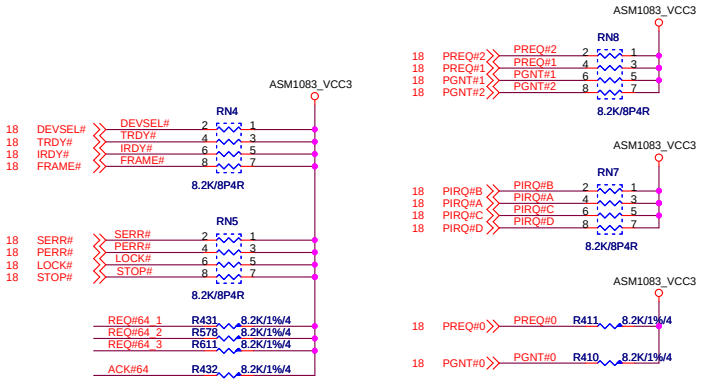


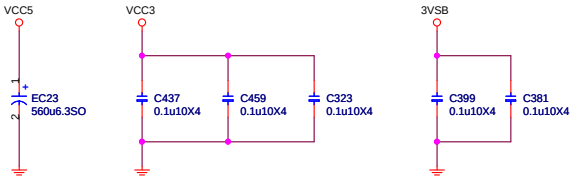
IDSEL = AD18
MASTER = PREQ#2
PIRQ#C

AD[31..0] — AD[31..0] 18

C_BE#[3..0] — C_BE#[3..0] 18

PCI PULL-UP / DOWN RESISTORS





PCI slot (X3)	
+3.3Vaux (wake)	- 1125mA
+3.3Vaux (no wake)	- 60mA
+3.3V	- 7.6A
+5V	- 15A
+12V	- 1.5A

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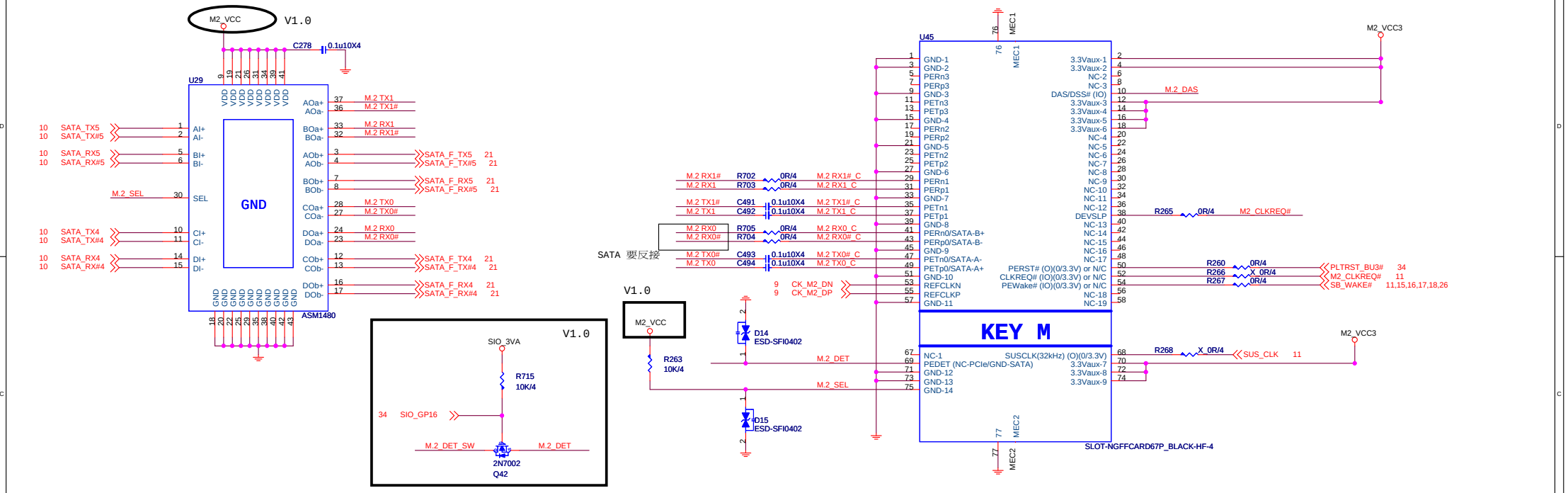
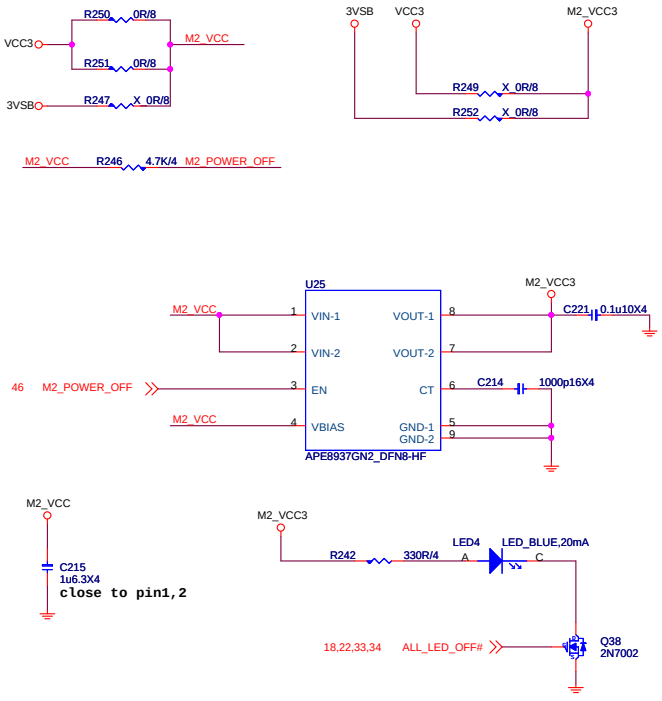


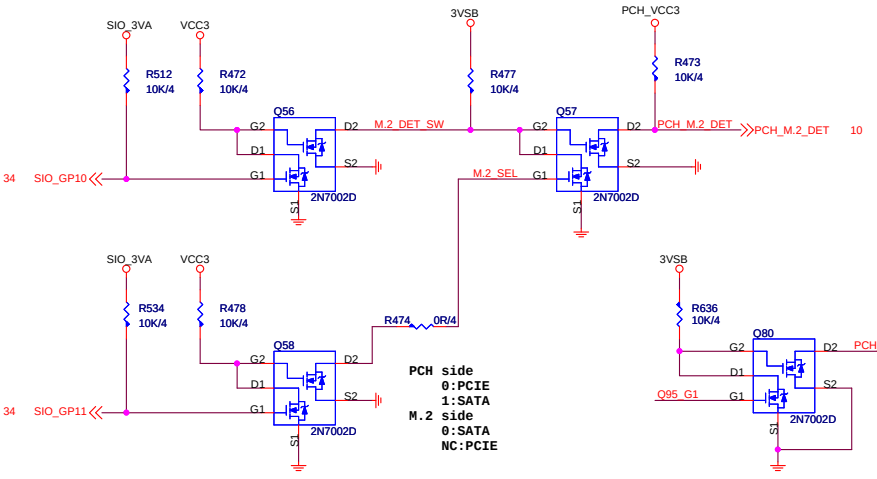
M2 cut power



BIOS_MODE

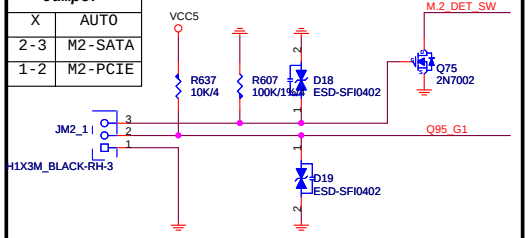
GP10	GP11	PCH_SEL	Mode
0	0	1	M2-SATA
0	1	1	Int-SATA
1	0	0	M2-PCIE
1	1	1	AUTO

SATA & PCIE SWITCH

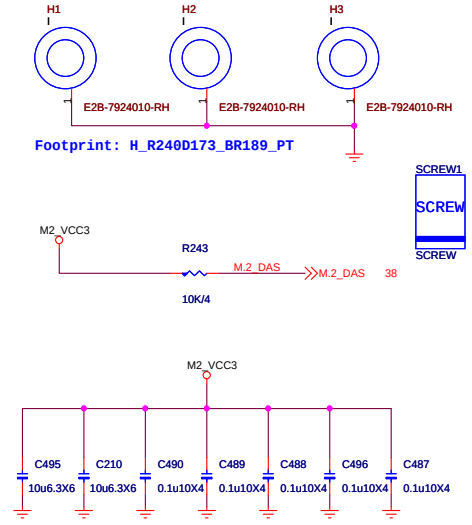


Jumper

X	AUTO
2-3	M2-SATA
1-2	M2-PCIE



For module card detect mode fail



Company	MICRO-STAR INT'L CO.,LTD
Model	MS-7918
Size	Custom
Document Description	Switch - SATA CONN/M2_SLOT
Rev	1.0
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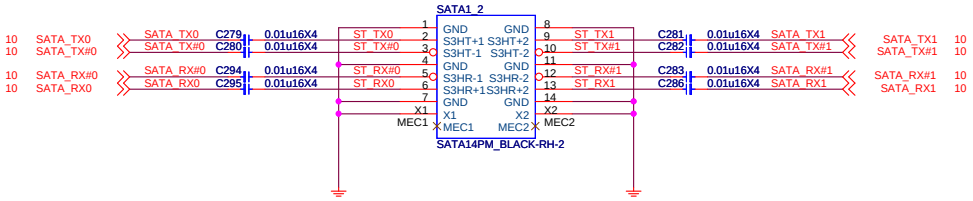
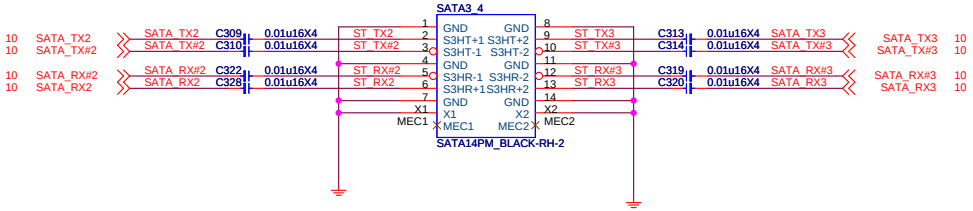
SATA 6G PORT 0,1

Gaming Black



SATA 6G PORT 2,3

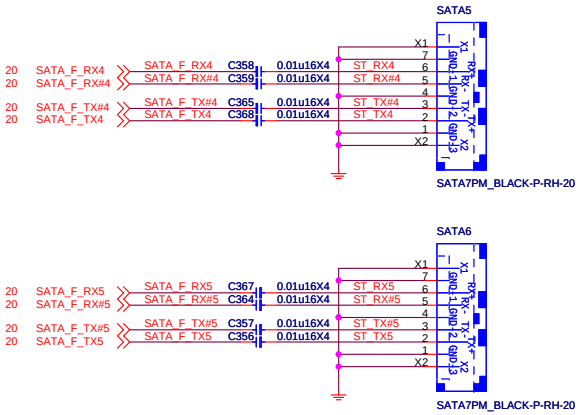
Gaming Black



SATA 6G PORT 0,1

Gaming Black

Z97/H97 SATA Gen3
B85 SATA Gen2



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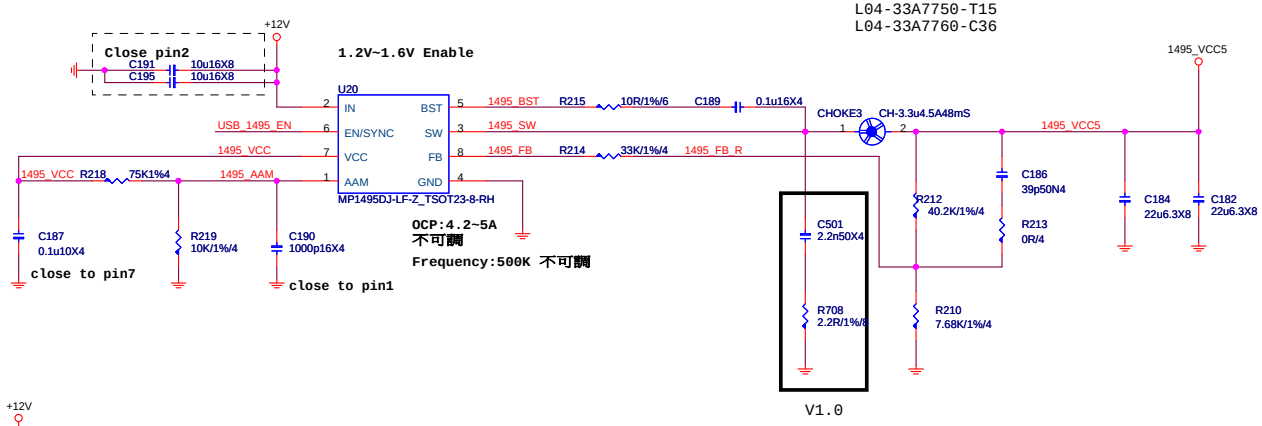
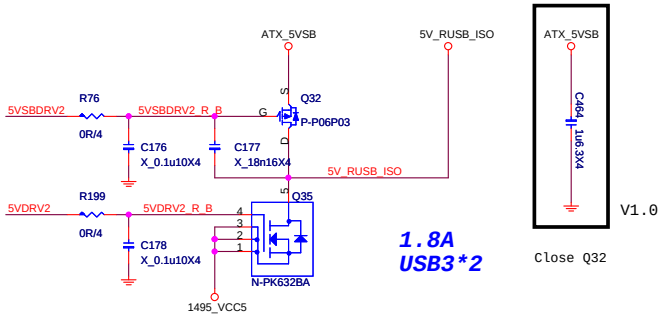
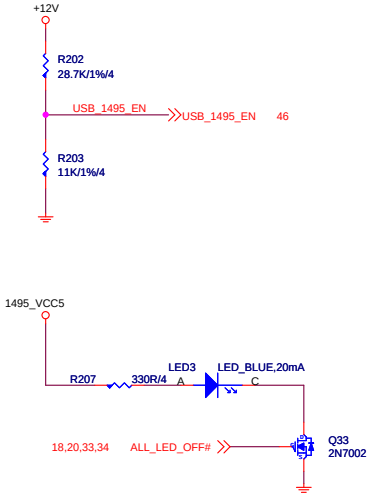
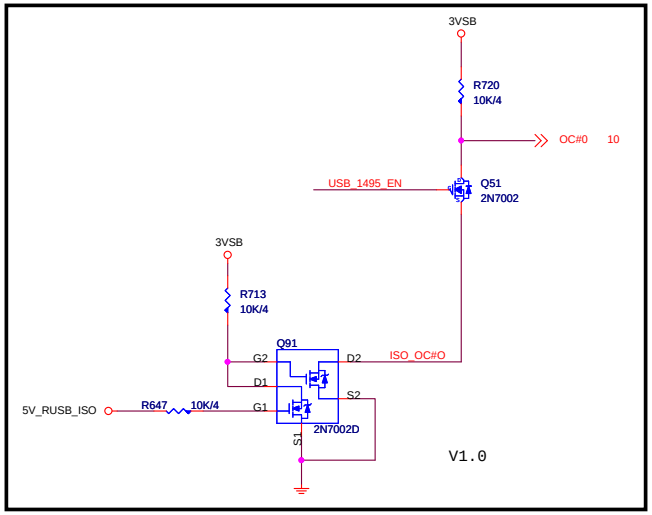
CHOKE
L04-33A7750-T15
L04-33A7760-C36



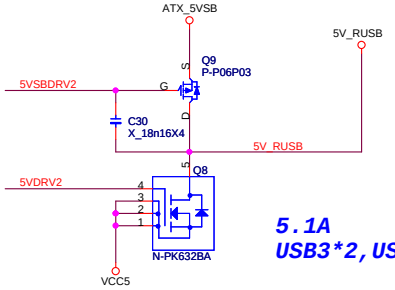
LAN_USB PORT POWER

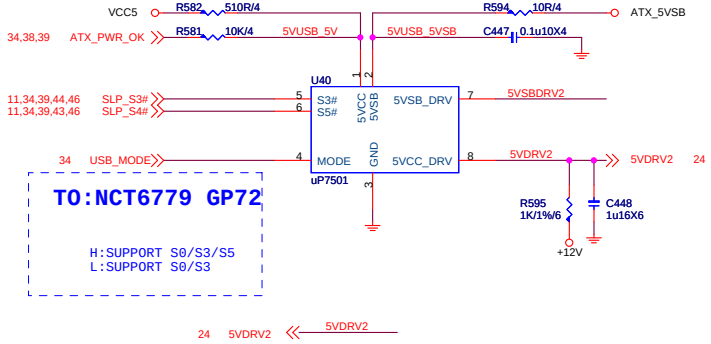




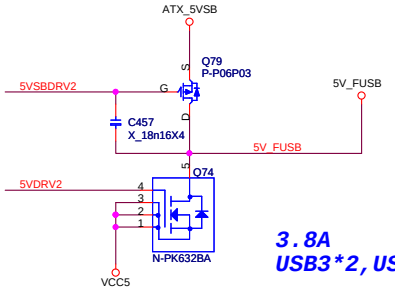


Real USB PORT POWER





Front USB PORT POWER



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7918	
Size: Custom	Document Description: USB POWER - MP1495/UP7501	Rev: 1.0
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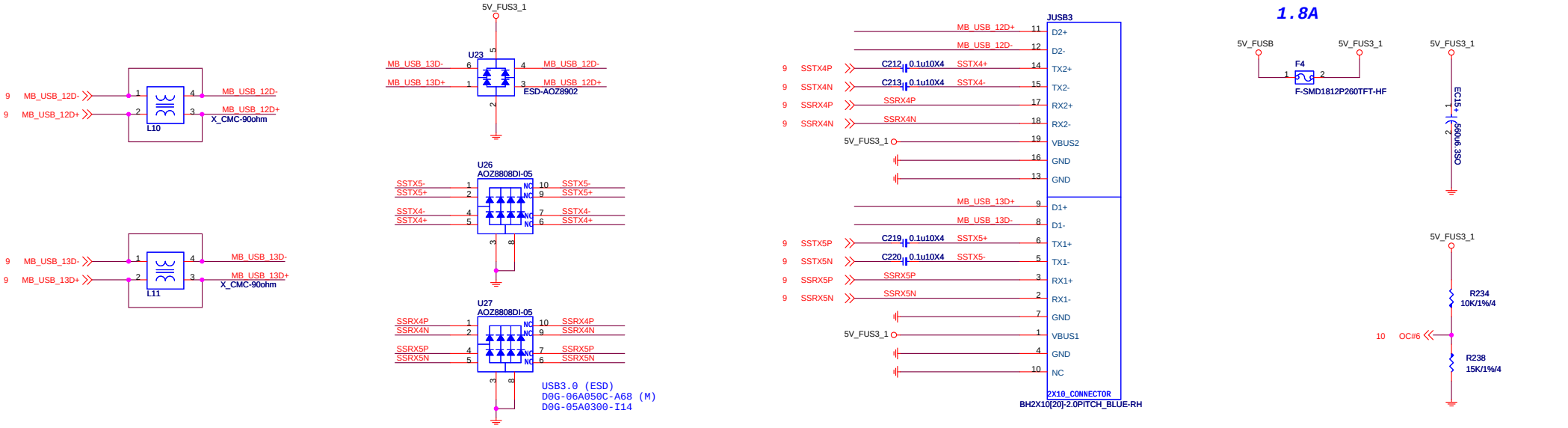
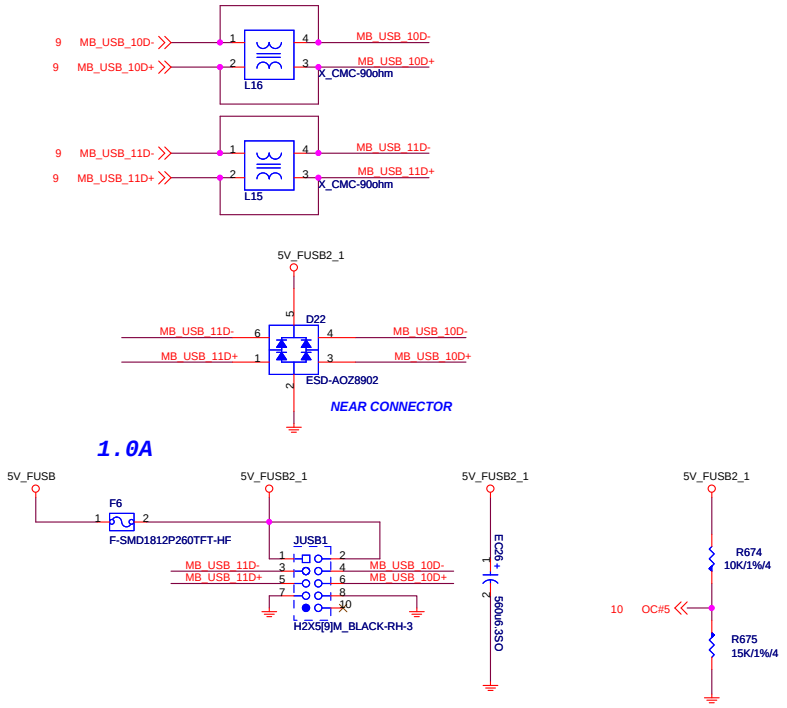
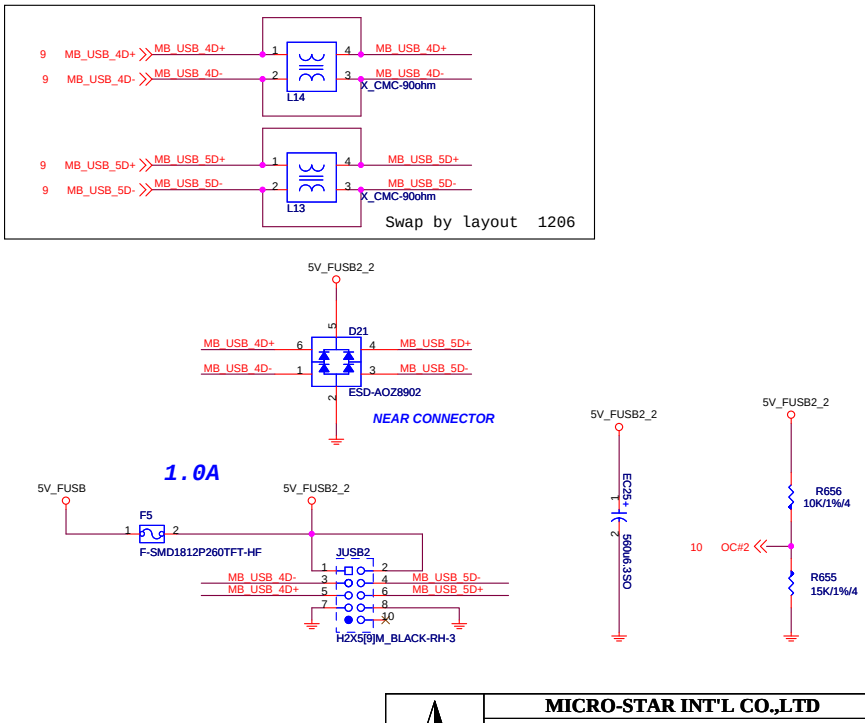


FRONT USB PORT 8,9



FRONT USB PORT 12,13



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MS-7918		
Size: Custom	Document Description: Front USB3/USB2	Rev: 1.0
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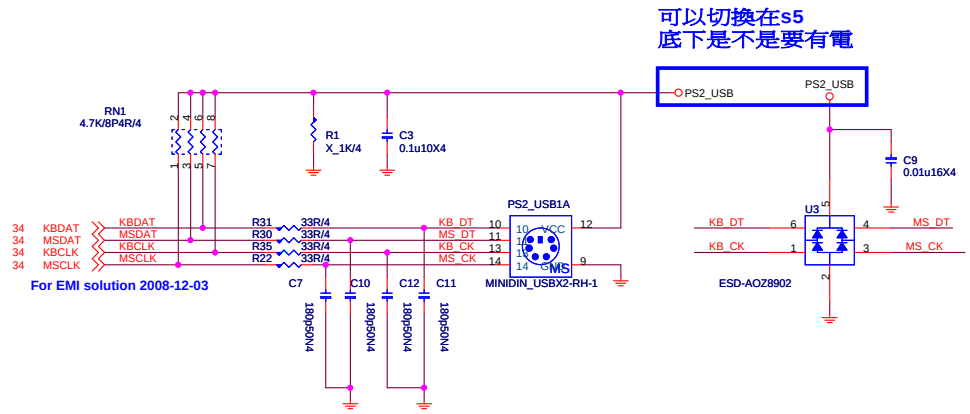
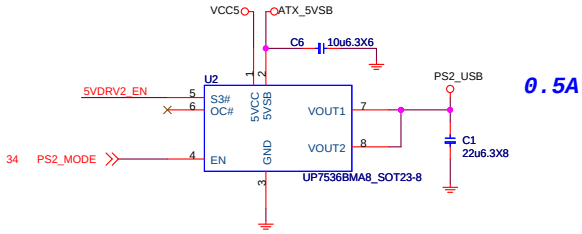
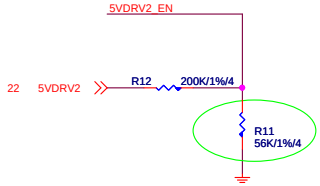
PS2 KEYBOARD & MOUSE CONNECTOR



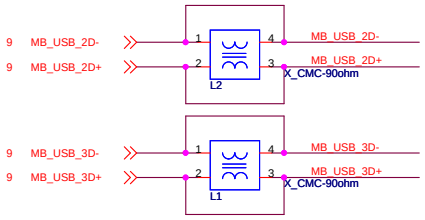
PS2 Power

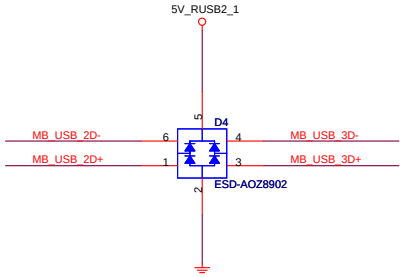


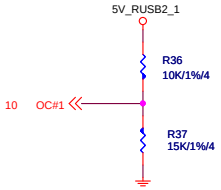
USB MODE

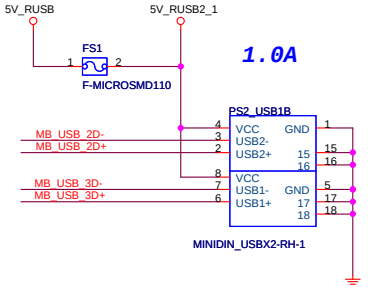


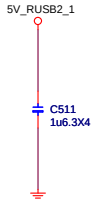
REAR USB PORT 2,3 (W/ PS2)











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MS-7918		
Size: Custom	Document Description: Rear I/O PS2/USB2	Rev: 1.0
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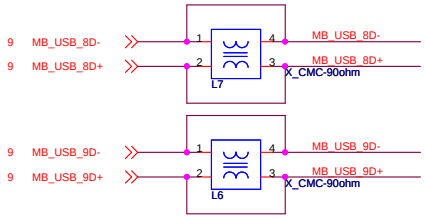
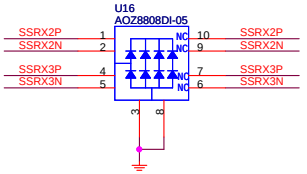
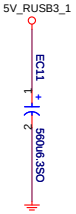
Dual USB3 Connector







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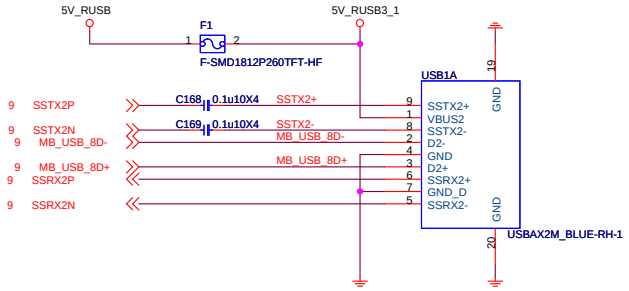

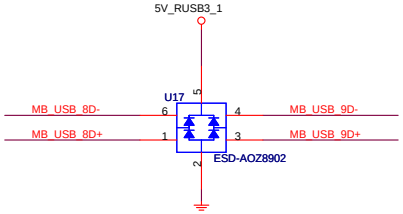

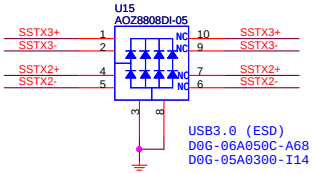

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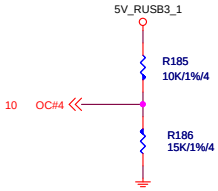
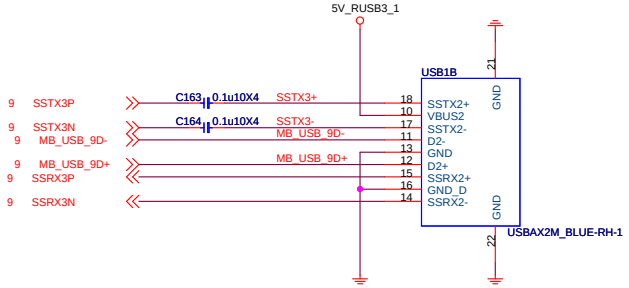
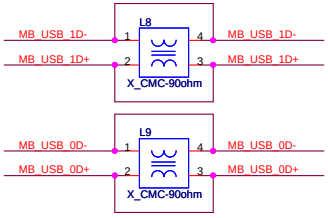
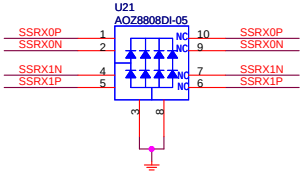




Dual USB3 Connector (W/ LAN)





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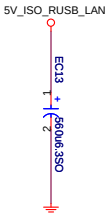

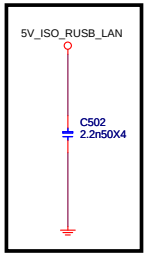

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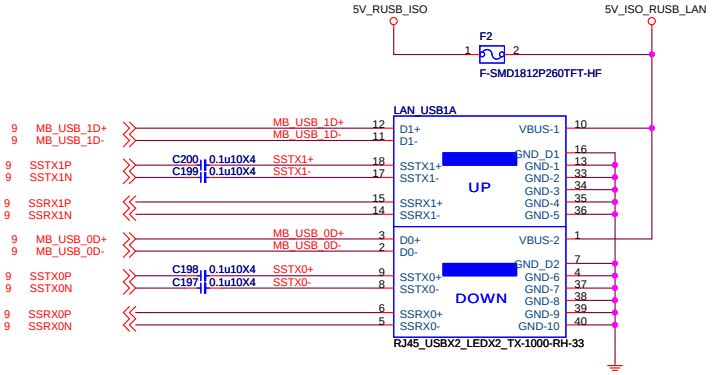

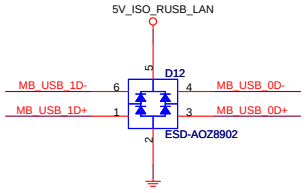

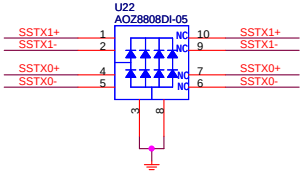

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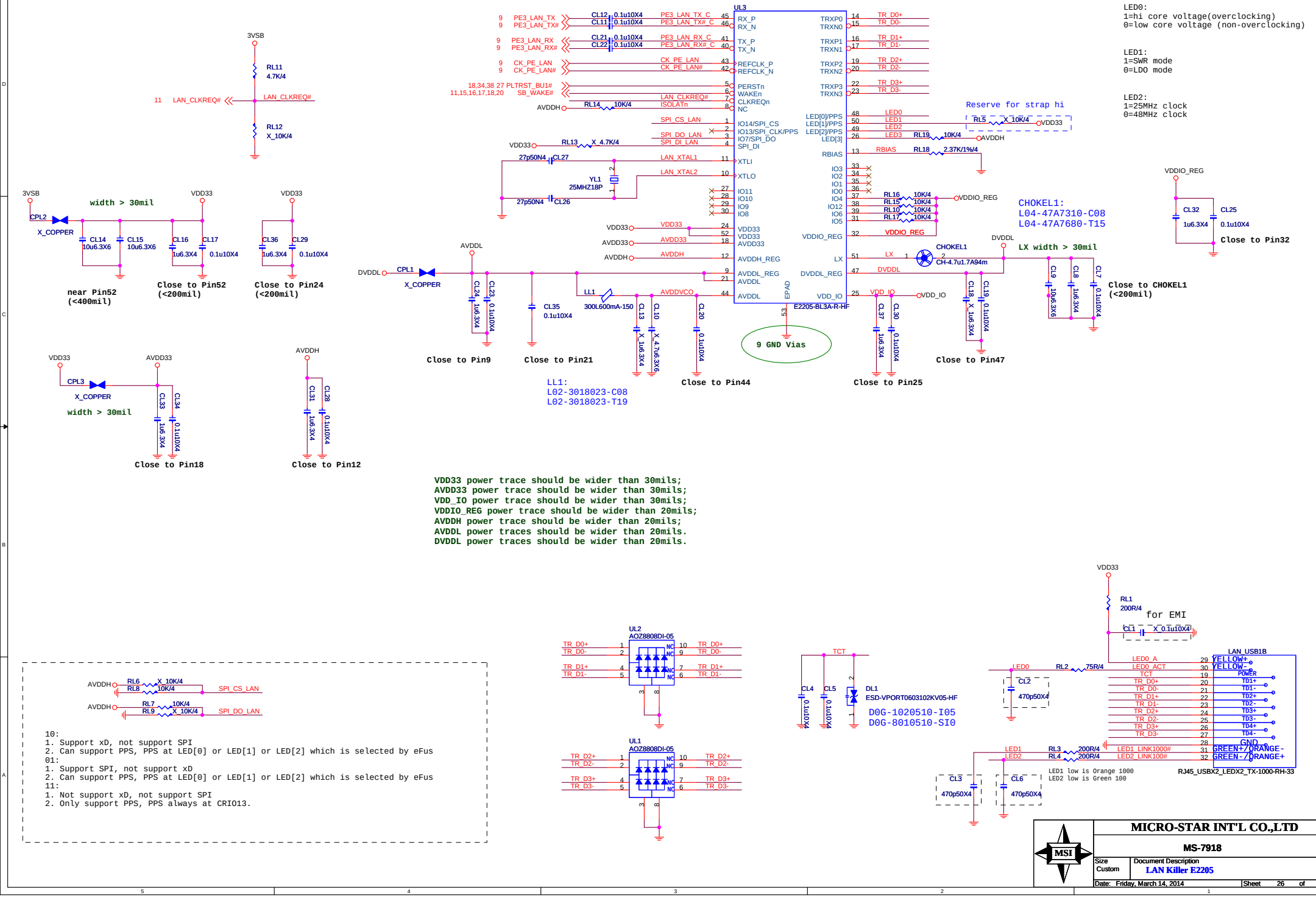
E2205-B Giga LAN



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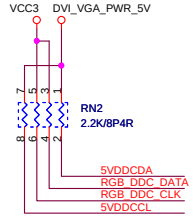
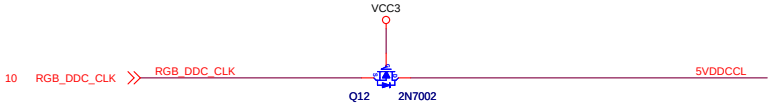
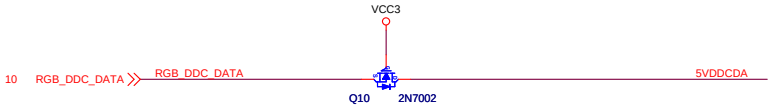
D-Sub

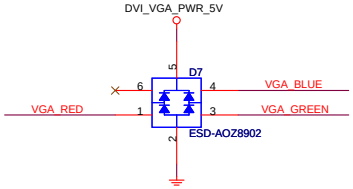
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

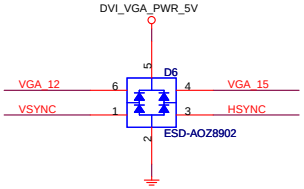
Level shift

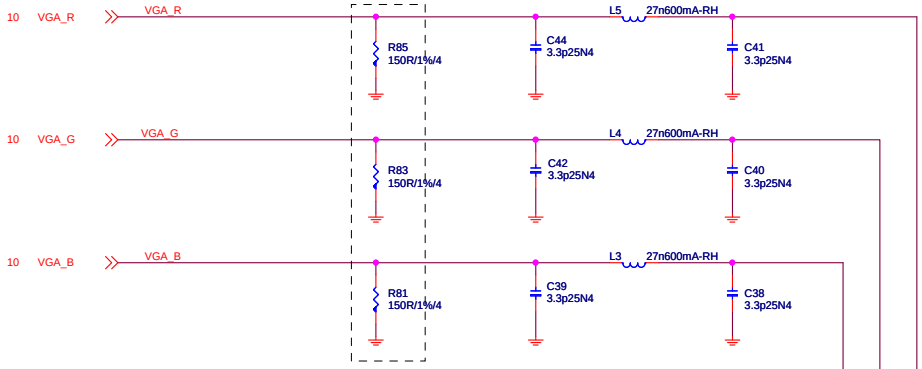




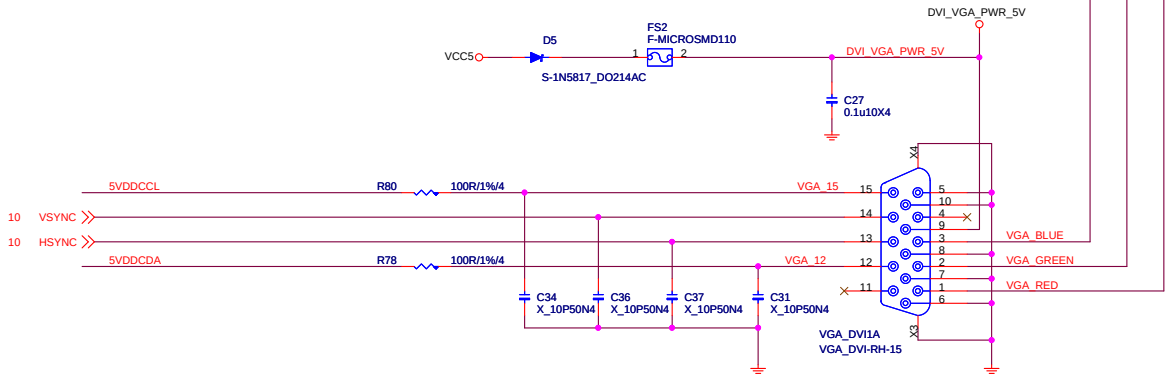








PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN



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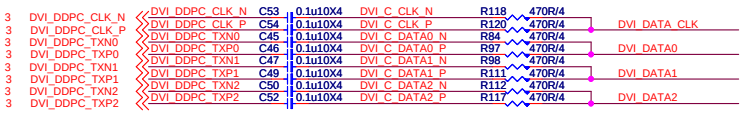
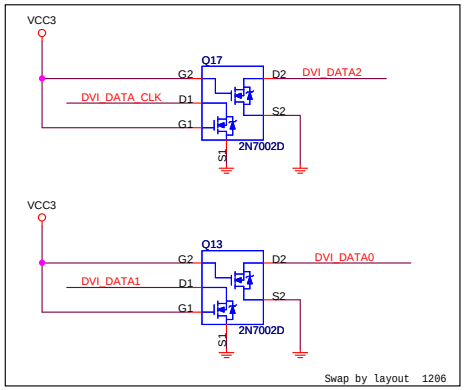
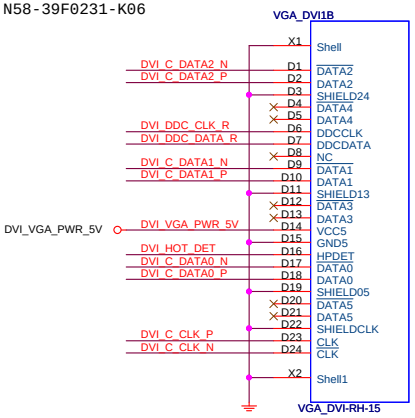
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)





Check MSI PN
N58-39F0231-K06



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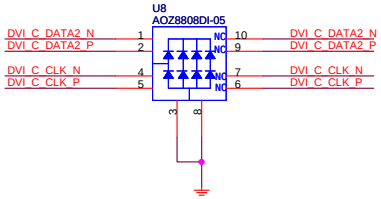

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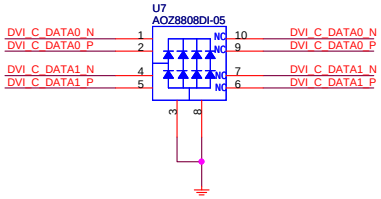
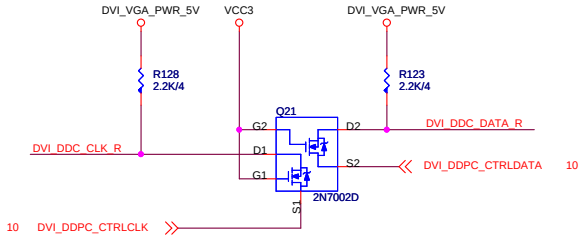
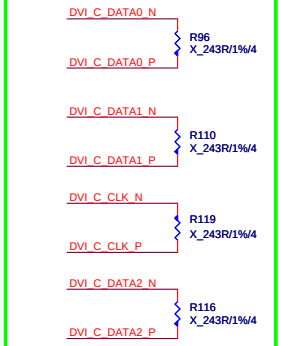
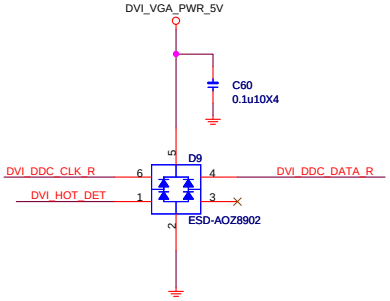
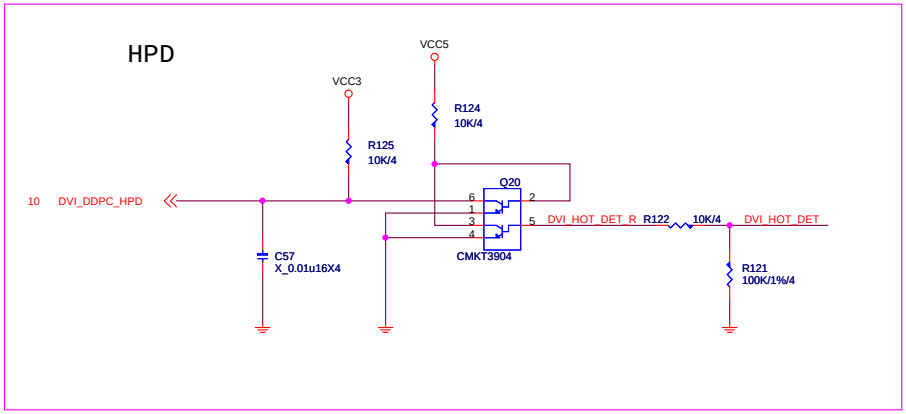


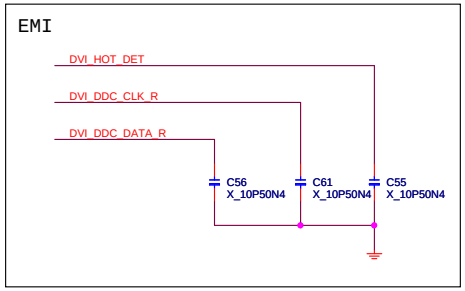


For EMI









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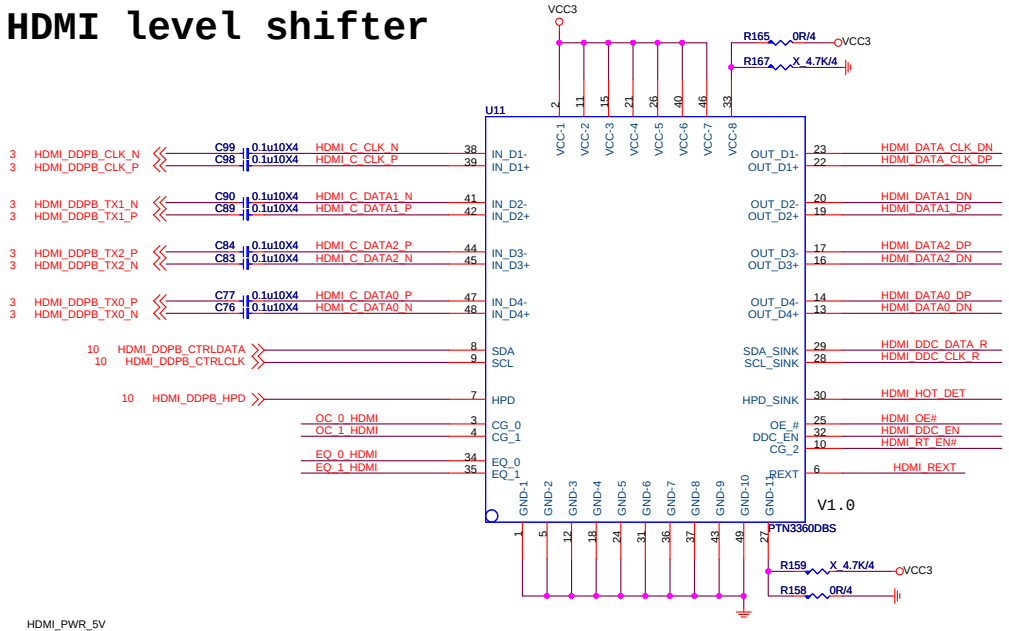
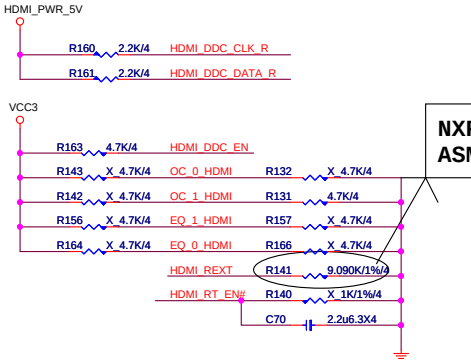
HDMI level shifter



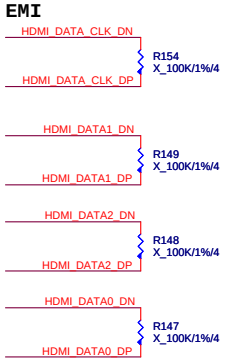


	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

EMI



EMI cap.

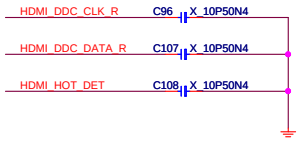
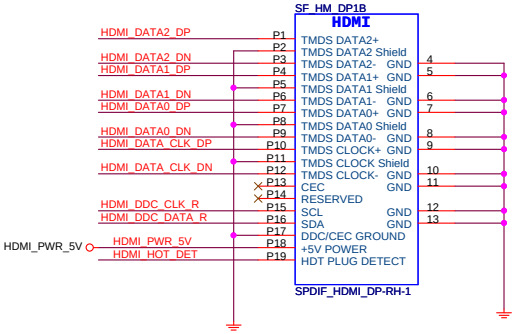
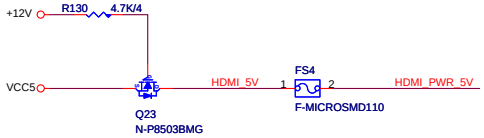
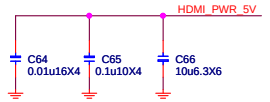


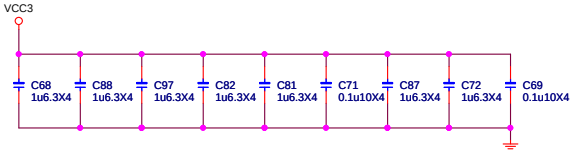
Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	









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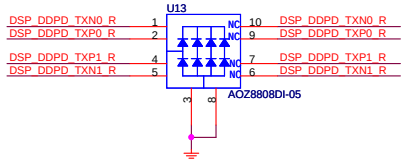
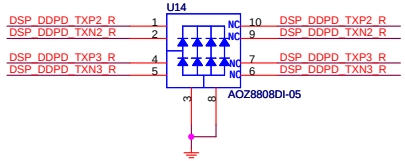
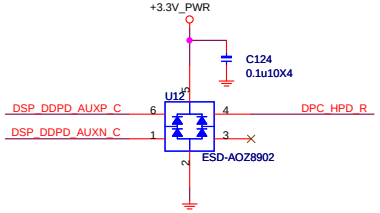
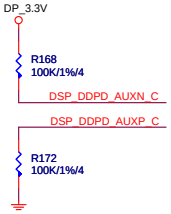
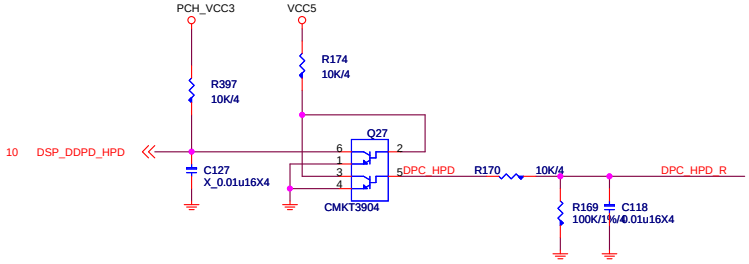
DP

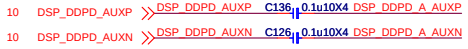


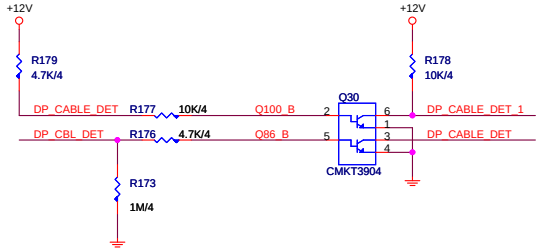


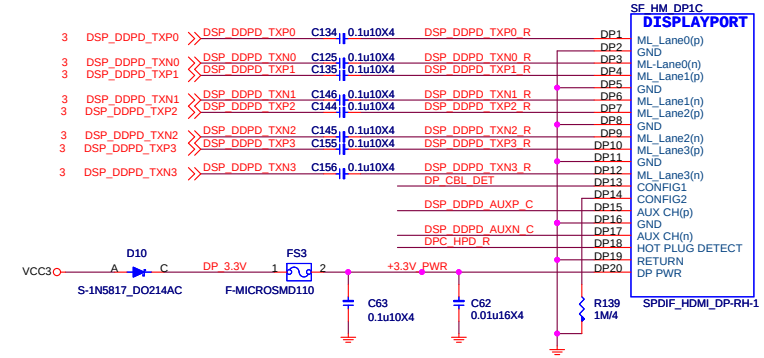




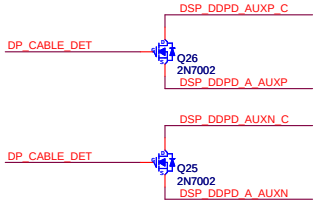






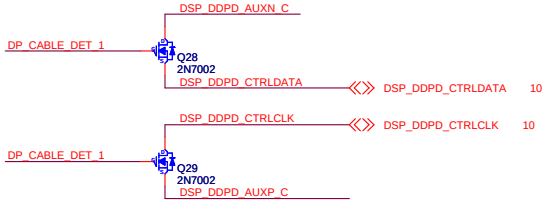


DisplayPort*Interoperability Implementation



PS:DSP_DDPD_CTRLCLK

PULL HIGH 3.3V 2.2K ohm on chip side



PS:DSP_DDPD_CTRLDATA

PULL HIGH 3.3V 2.2K ohm on chip side

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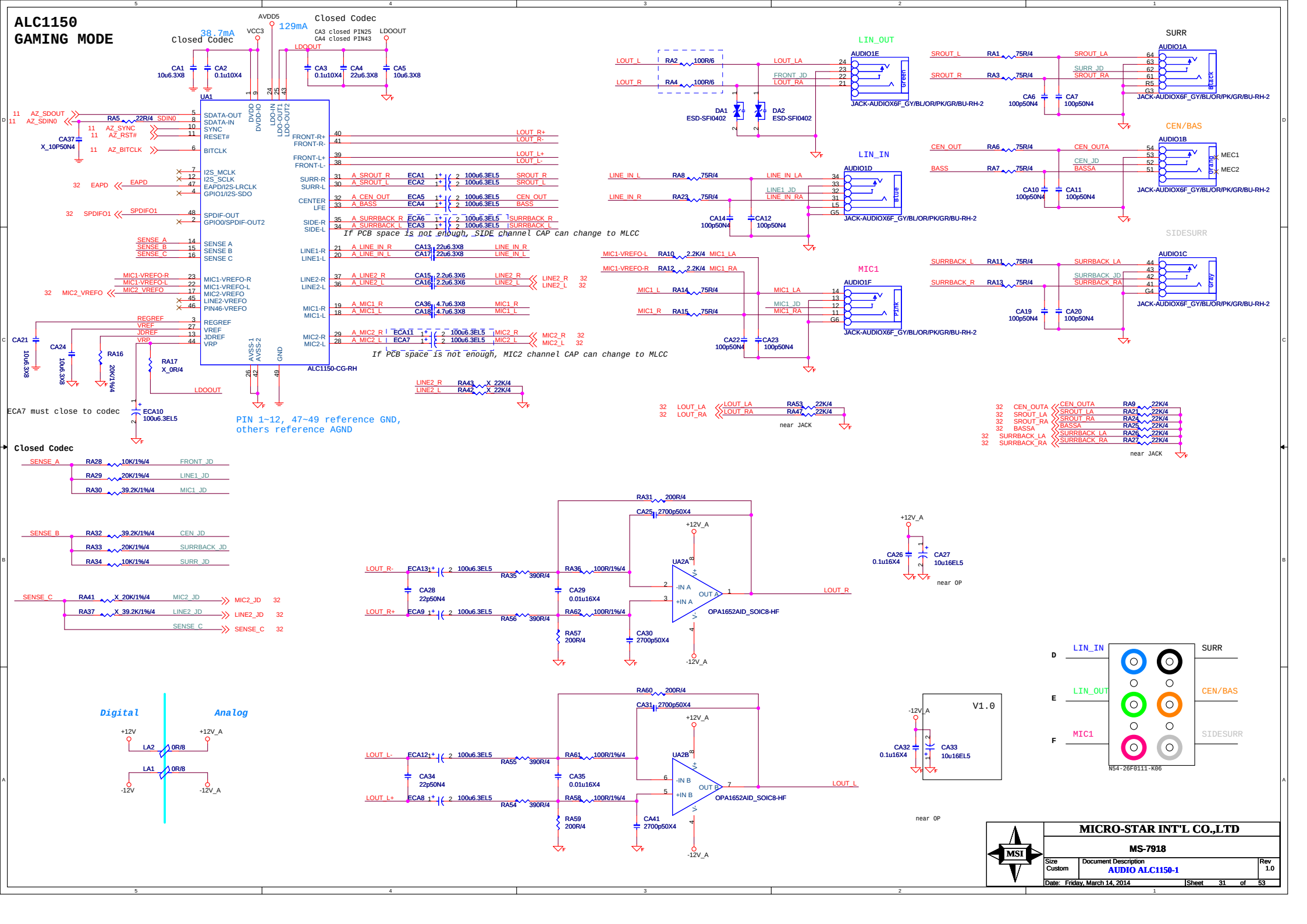
ALC1150 GAMING MODE



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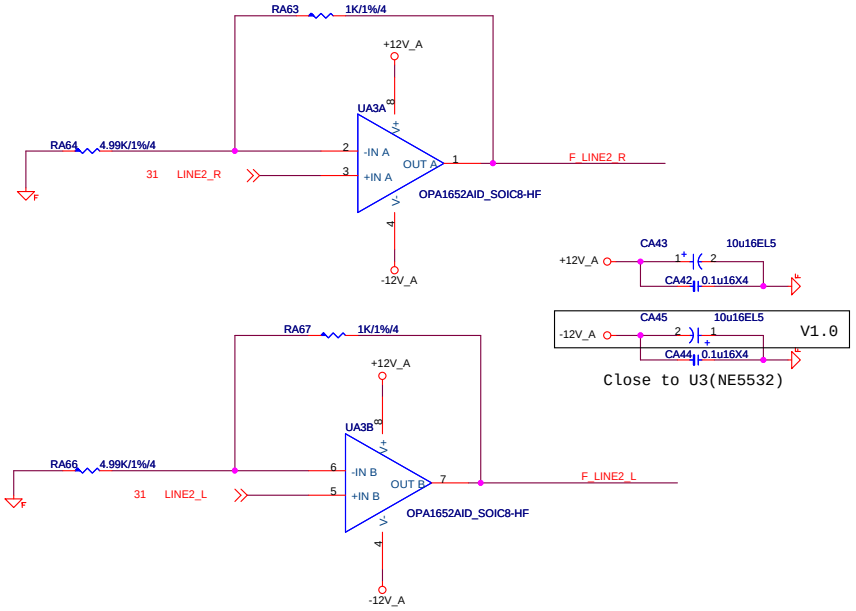
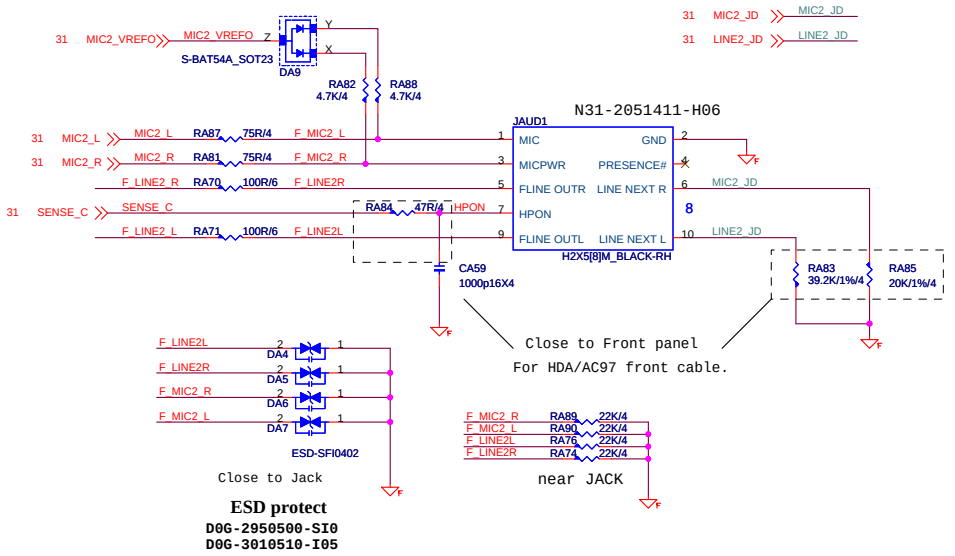
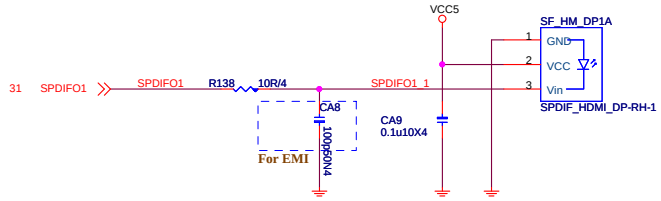




SPDIF OUT

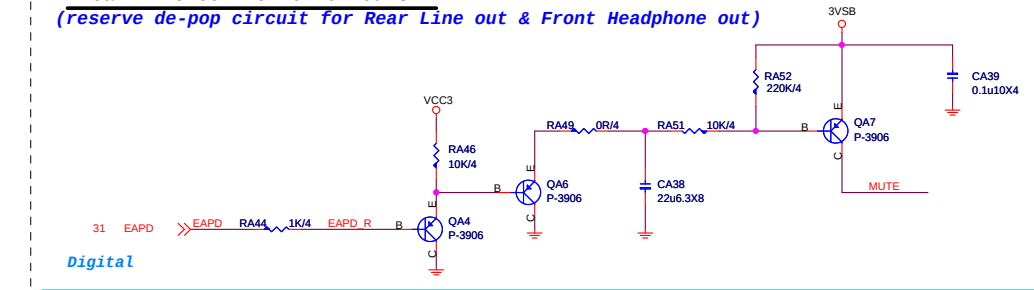
N58-42M0021-F02(HDMI+DP+SPDIF)
N58-06F0201-K06



Rear Line OUT De-POP circuit

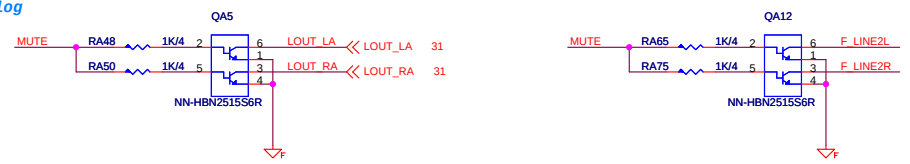
V1.0

(reserve de-pop circuit for Rear Line out & Front Headphone out)

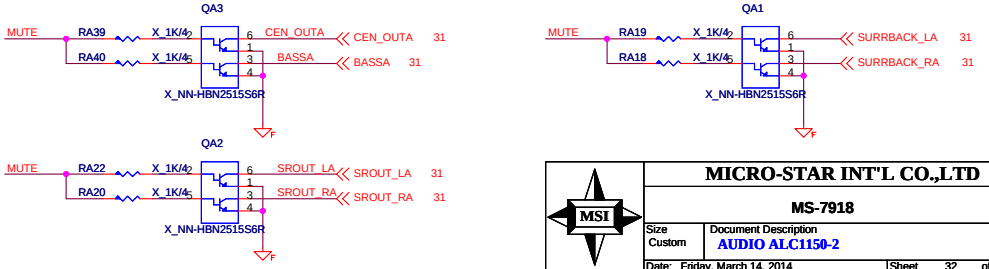


Analog

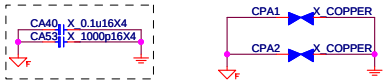
V1.0



(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA13, CA23, CA24 to TVS)



EMI



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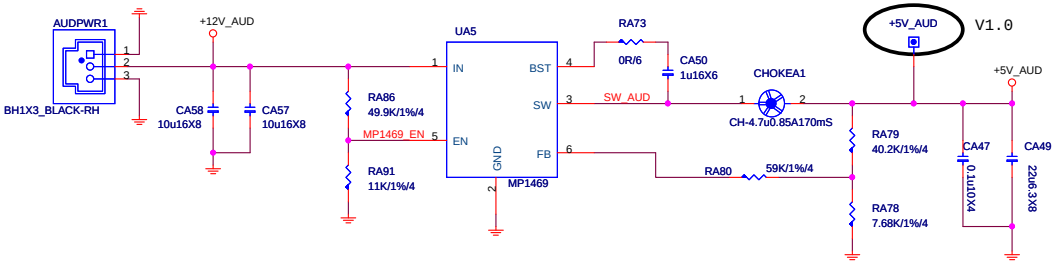
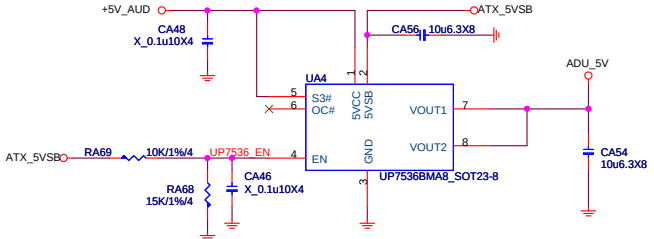
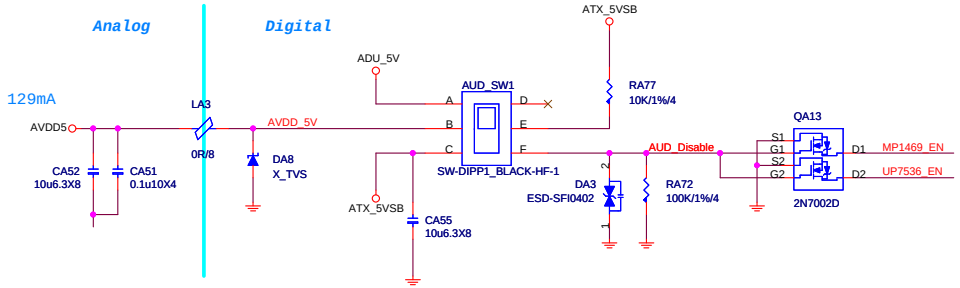






A-B: 5V power from AUDPWR1
B-C: 5V power from M/B ATX_5VSB (Default)

History:

2013/09/25: ALC1150 for Gaming module circuit initial release.

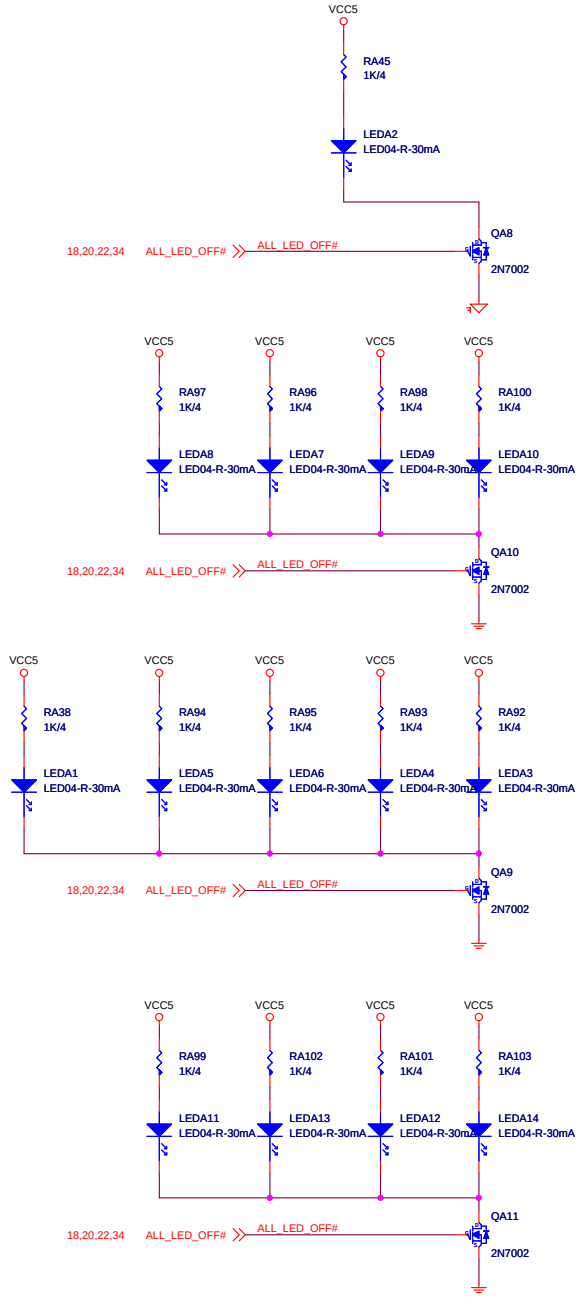
2013/10/14: Add audio 5V power switch. Swap MIC1-VREFO-L & MIC1-VREFO-R

2013/10/23: Change AUD_SW1 and to disable external 5V power if switched to M/B ATX_5VSB.

2013/10/29: update AUD_SW1 P/N.

2013/11/01: Change AUDPWR1 to 3PIN

Audio moat is transparent and width 40mil



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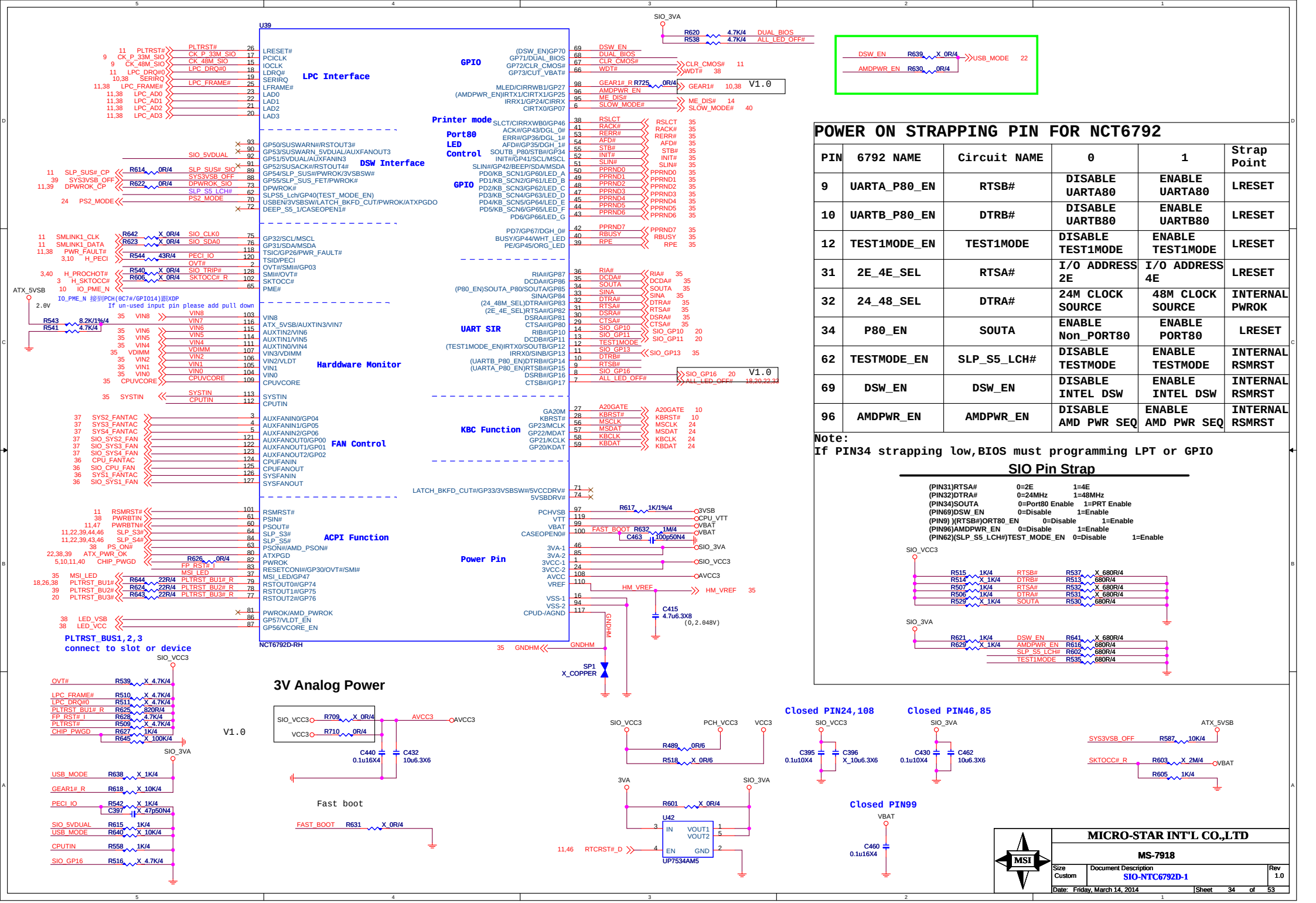

POWER ON STRAPPING PIN FOR NCT6792

PIN	6792 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	24_48_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
62	TESTMODE_EN	SLP_S5_LCH#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

SIO Pin Strap

(PIN31)RTSA# 0=2E 1=4E
(PIN32)DTRA# 0=24MHz 1=48MHz
(PIN34)SOUTA 0=Port80 Enable 1=PRT Enable
(PIN69)DSW_EN 0=Disable 1=Enable
(PIN9))(RTSB#)ORT80_EN 0=Disable 1=Enable
(PIN96)AMDPWR_EN 0=Disable 1=Enable
(PIN62)(SLP_S5_LCH#)TEST_MODE_EN 0=Disable 1=Enable

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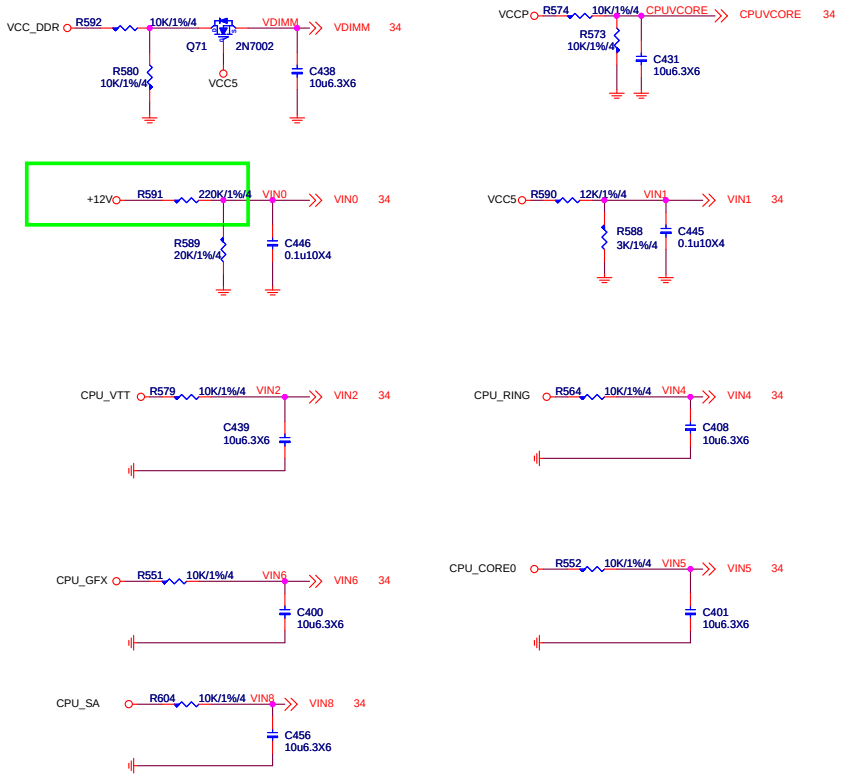
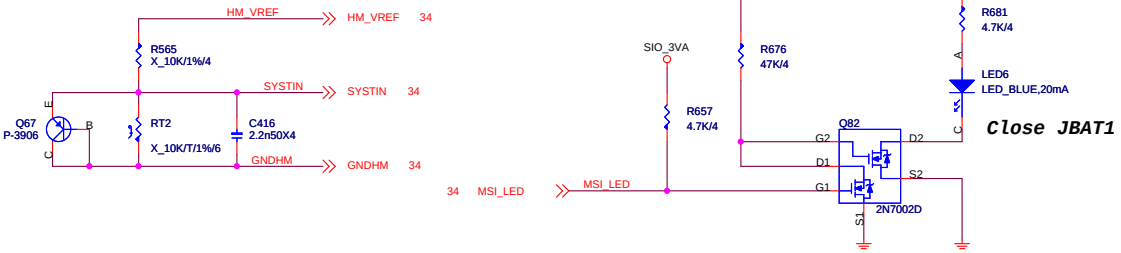
HW Monitor - Voltage

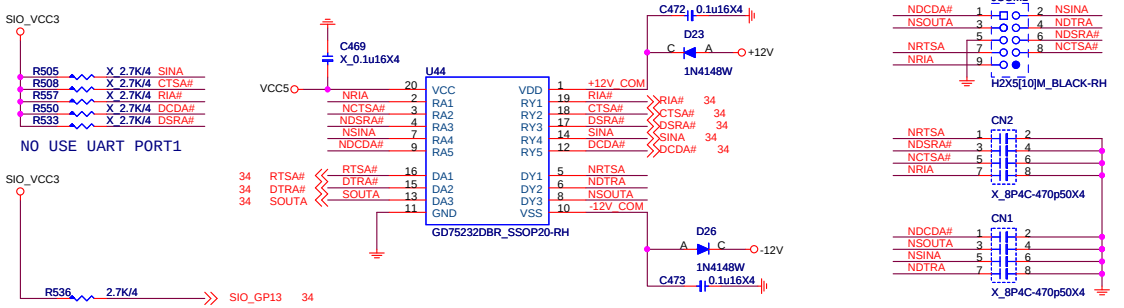
SIO HM Voltage voer 2V will not detect



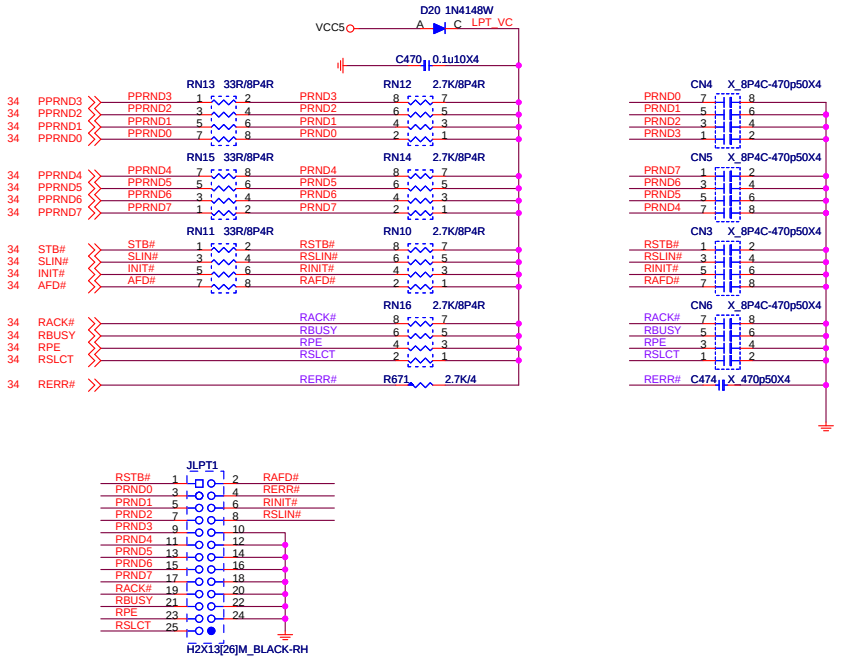
Thermal Monitor



SERIAL PORT 1



PARALLAL PORT



N31-2131151-H06 : 2.0mm

N31-2131131-H06 : 2.54mm

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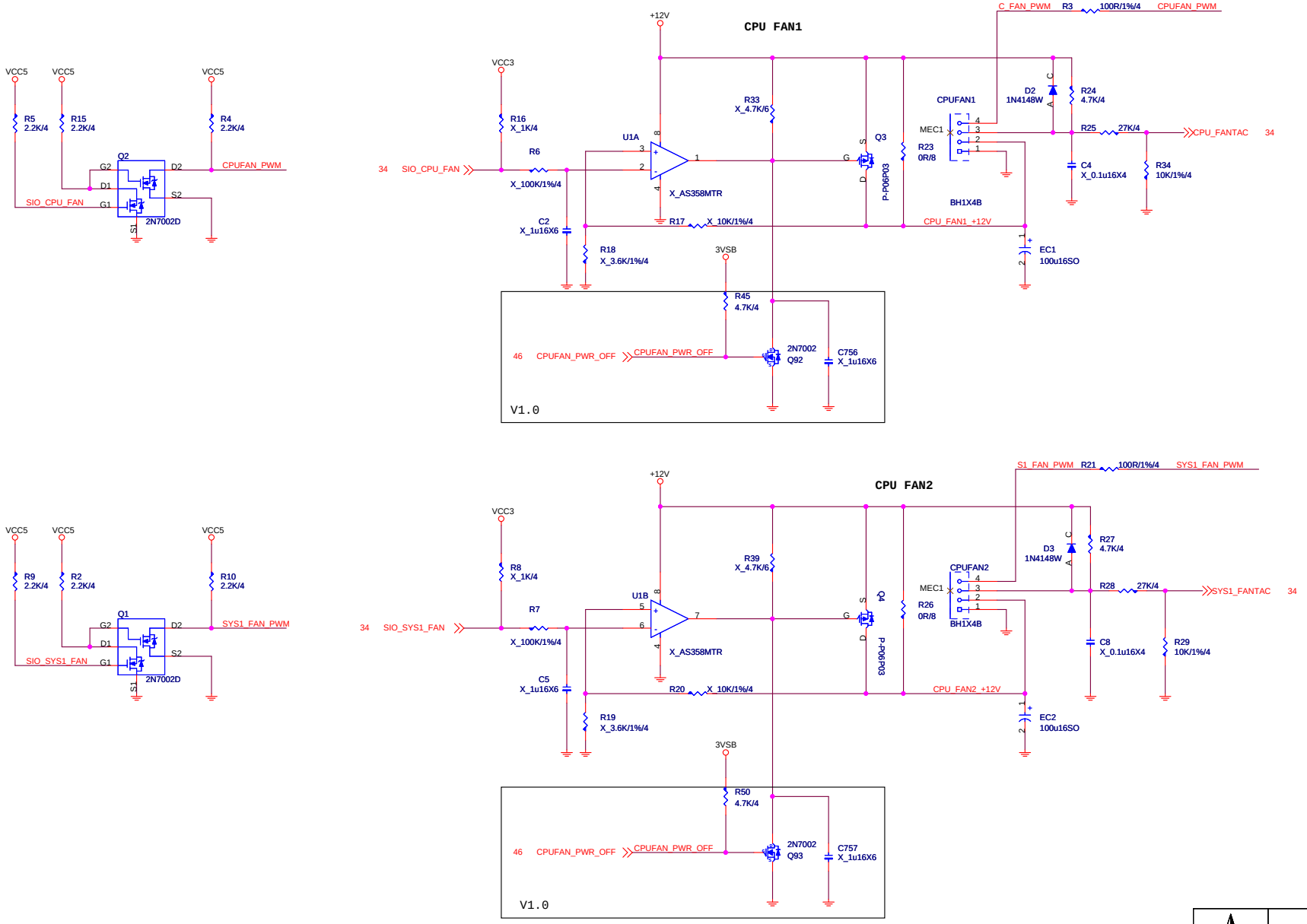
Type E : 4 PIN CPU FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6776/5533)

FAN-COUNTROL CIRCUIT



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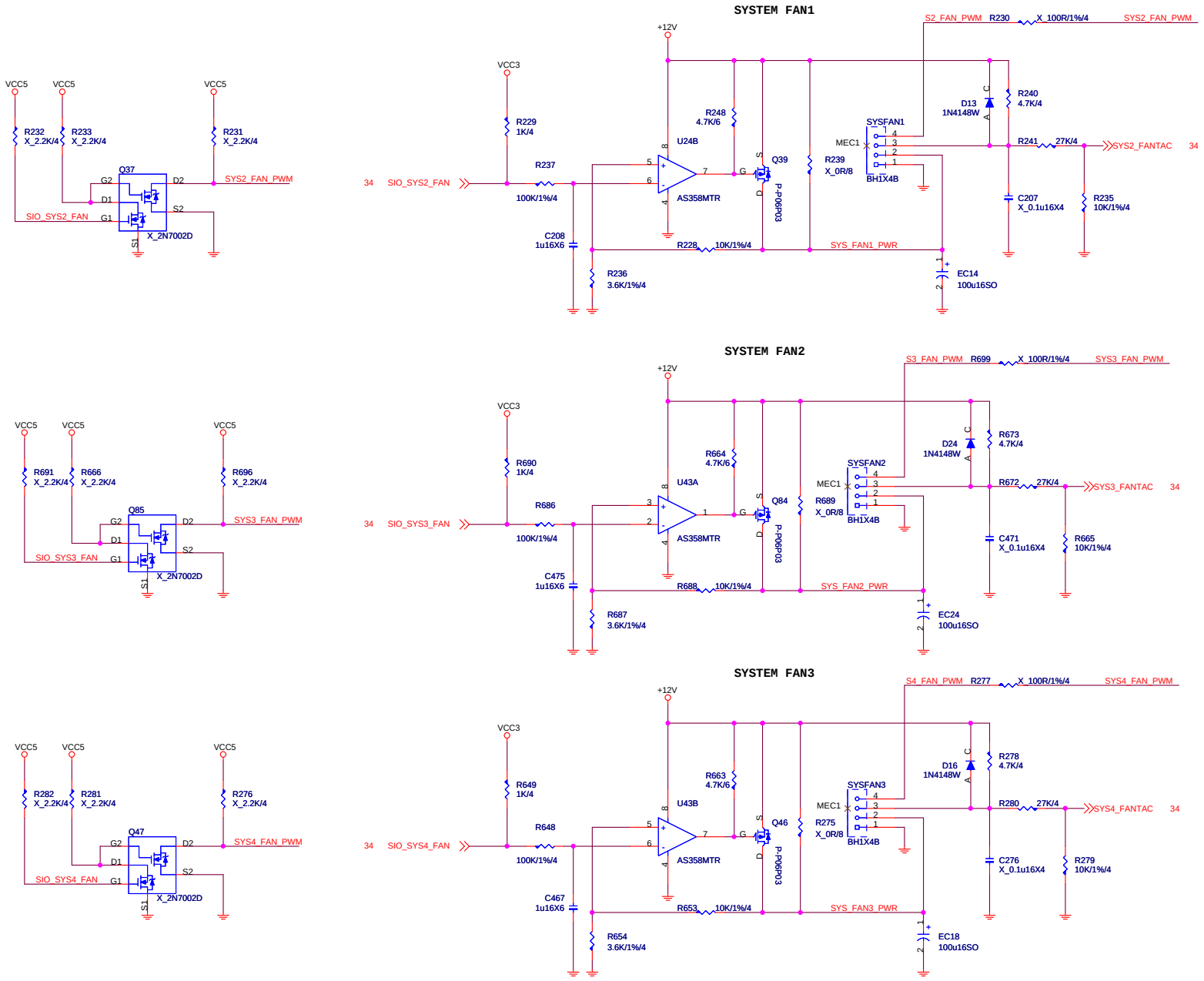
Type F : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6776/5533)



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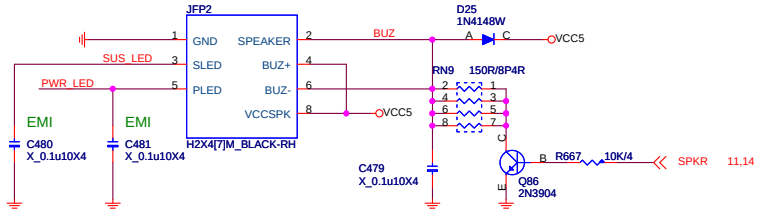
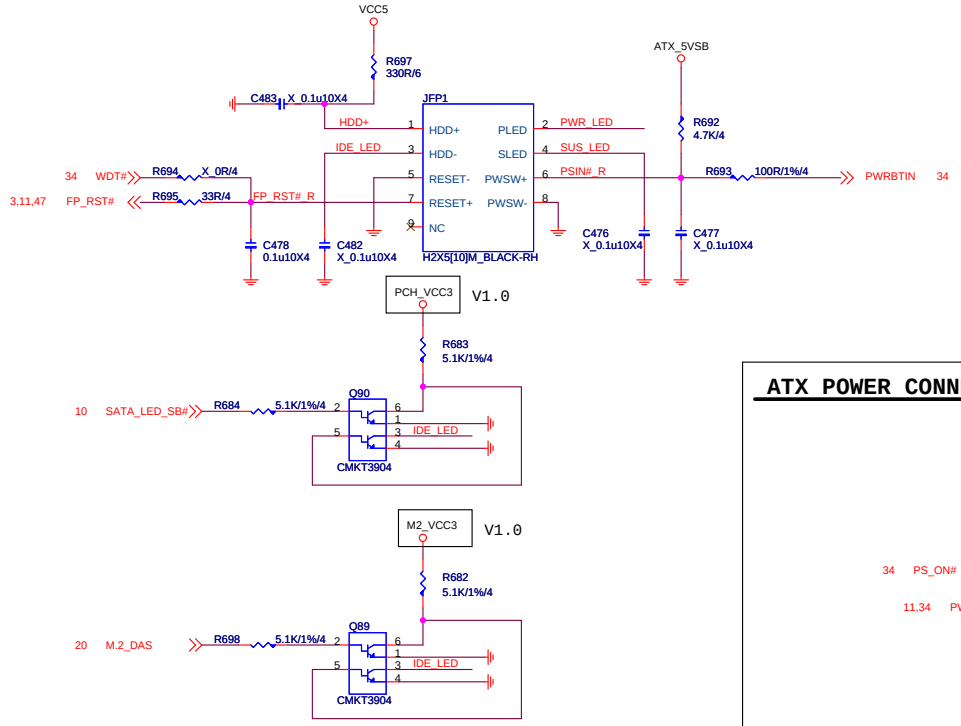
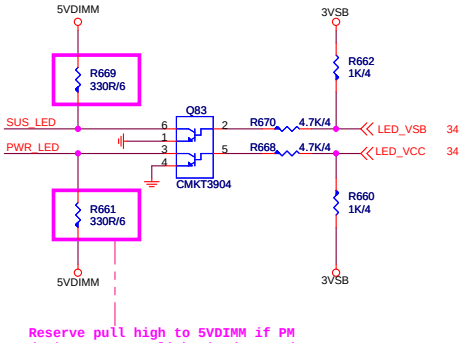
FRONT PANNEL





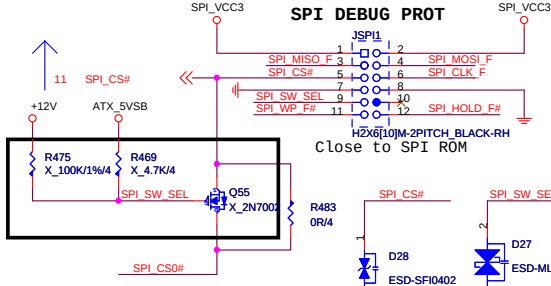
LED (for Fintek 71869)



Reserve pull high to 5VDIMM if PM
don't want PLED light in deep mode.

Z97:stuff R614->+12V
H97:stuff R611->ATX_5VSB
Q55:Z97->2N7002, H97->D03-0341409-A68 / D03-0230019-A30

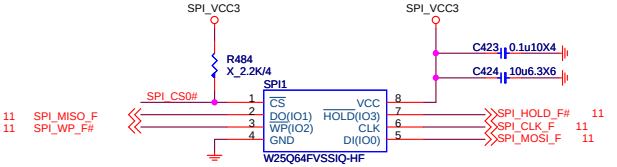
SPI DEBUG PROT



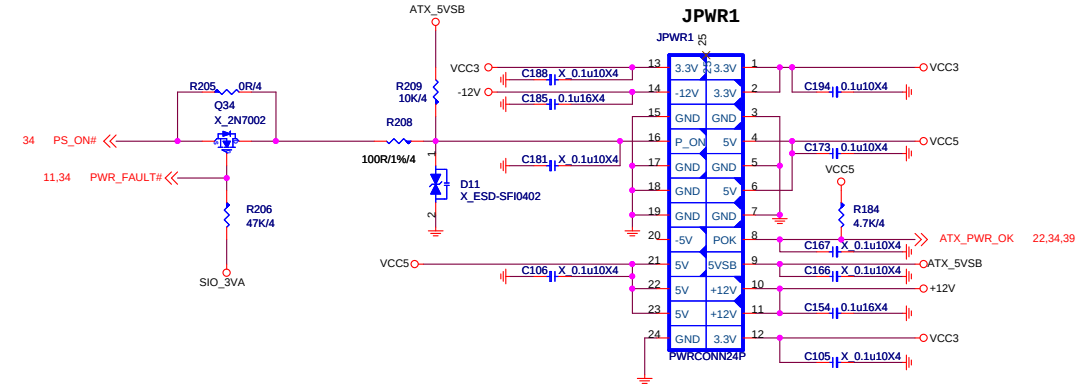
SPI FLASH ROM

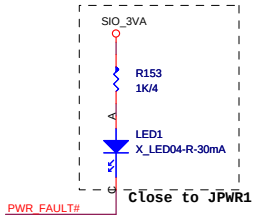
Place close to SB.

*SPI_CLK & SPI_CS0# must be length matched to within 500mils.
*SPI_CLK & SPI_MOSI must be length matched to within 500mils.

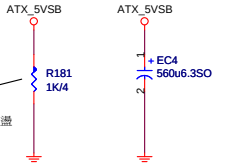


ATX POWER CONNECTOR

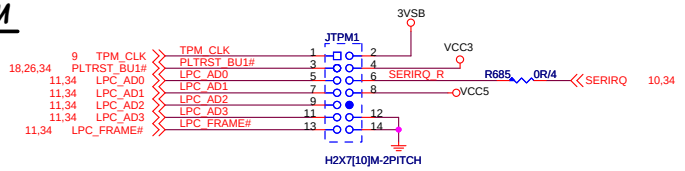




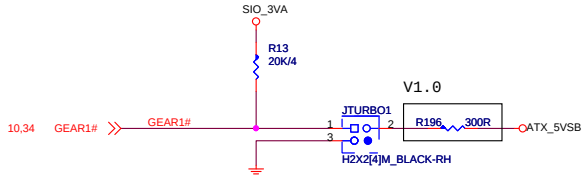
上1K是解決航嘉200W(huntkey)power supply的問題,加1K是爲了不讓ATX_5VSB空載而產生震盪



TPM



JTurbo



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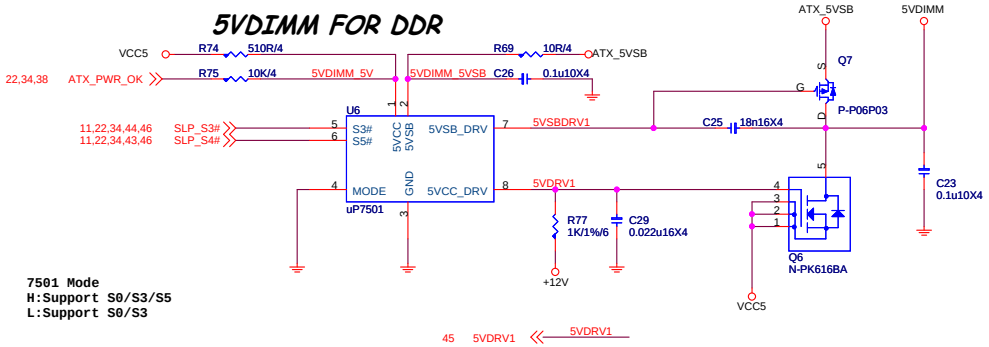
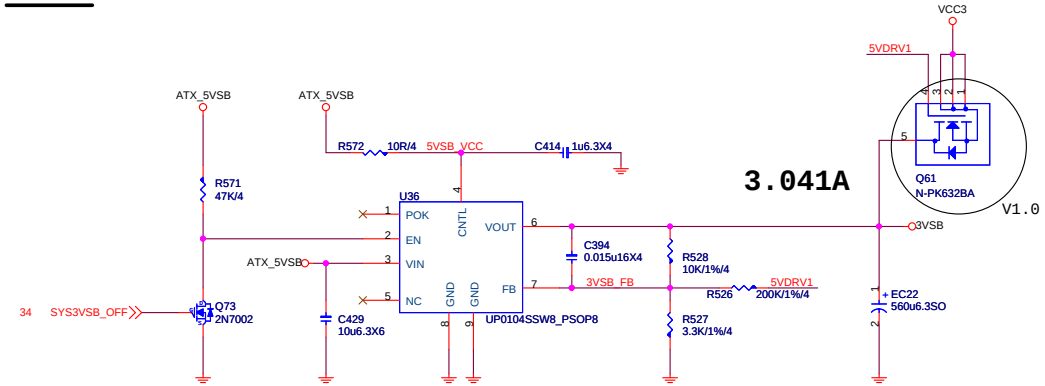
5VDIMM FOR DDR



7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

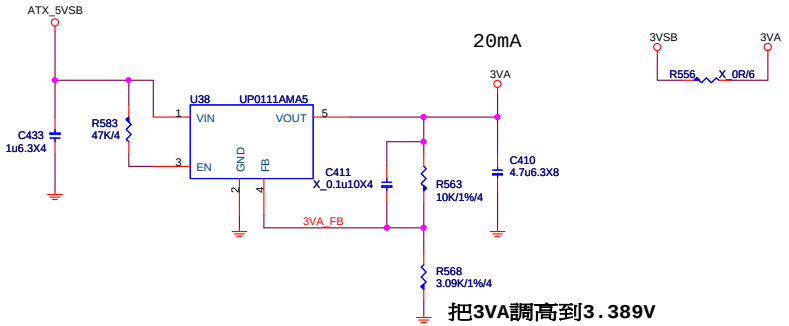
3VSB



3.041A

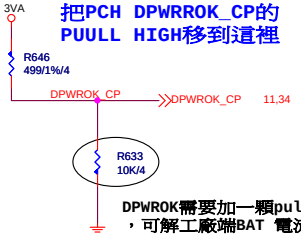
V1.0

3VA



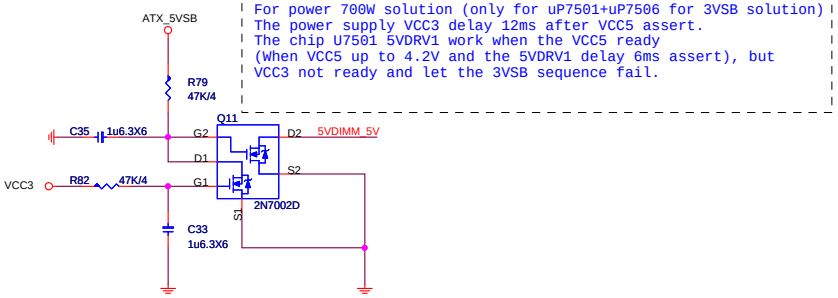
把3VA調高到3.389V

Ver:1.0
Remove 3VA Power Down circuit



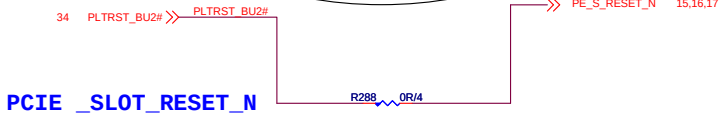
把PCH DPWRROK_CP的
PUULL HIGH移到這裡

DPWROK需要加一顆pull down 10k電阻
，可解工廠端BAT 電流過大問題



For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

Remove Buffer Ver:1.0



PCIE _SLOT_RESET_N
from SIO RESET_BUS2

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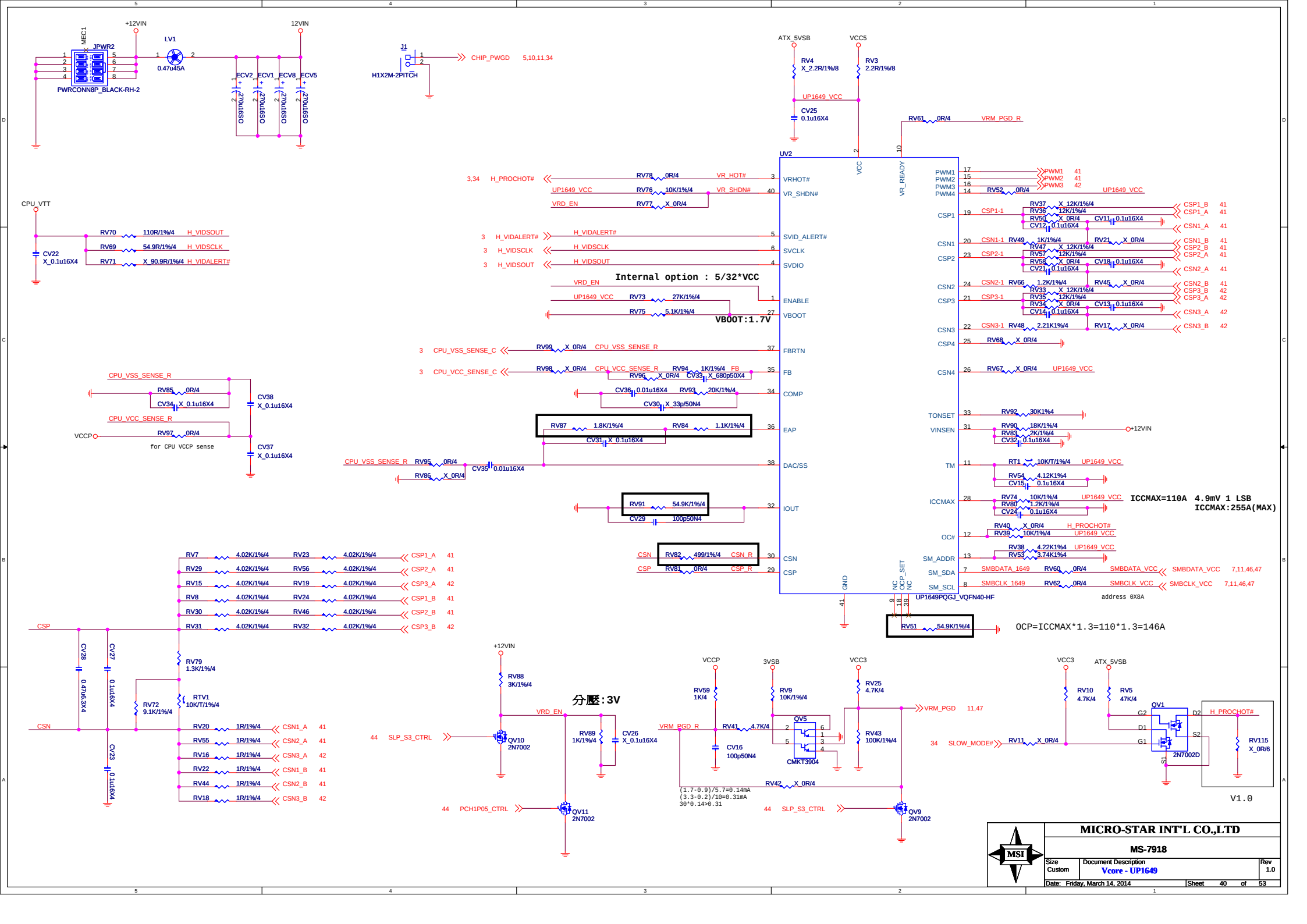

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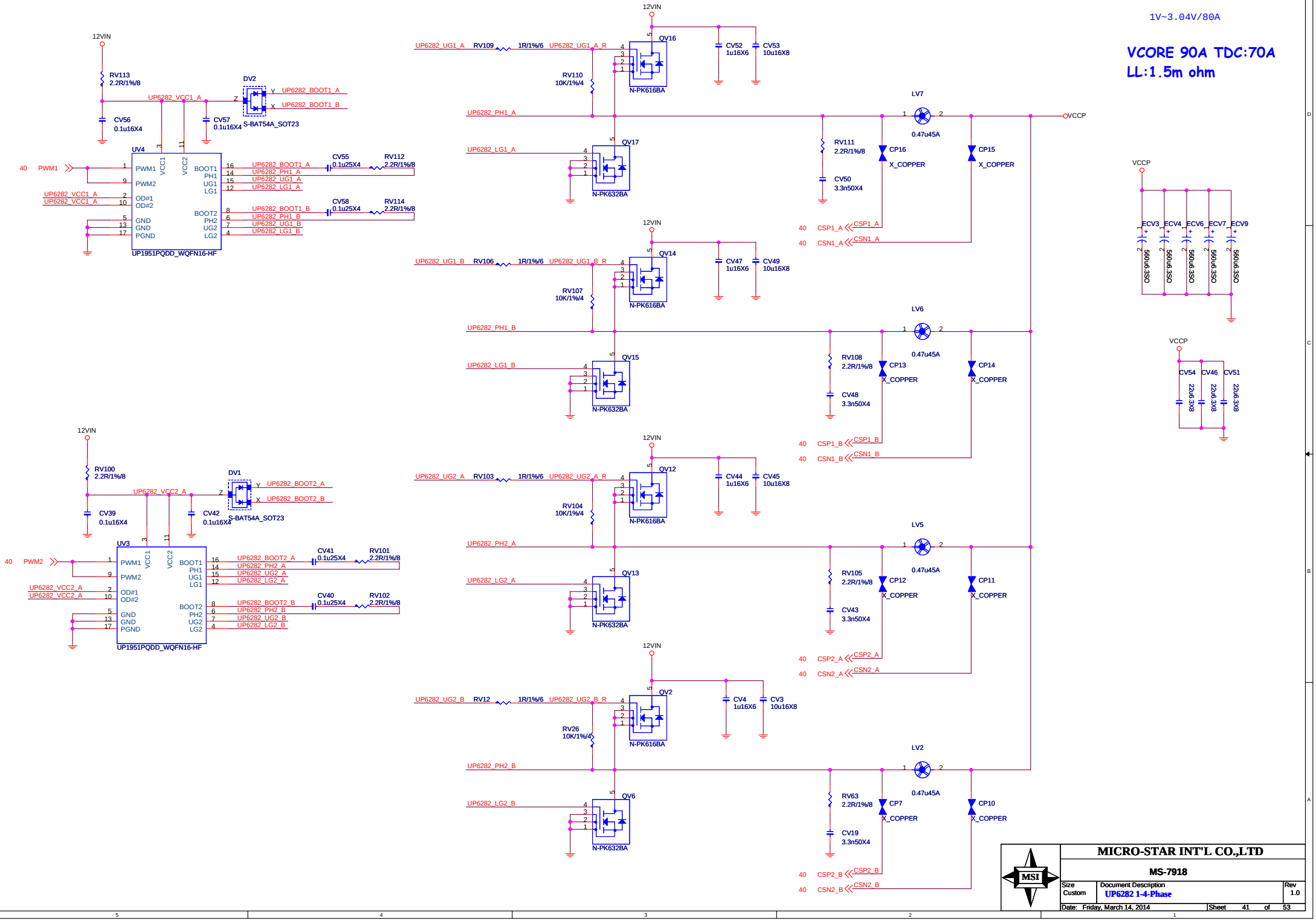
1V~3.04V/80A

VCORE 90A TDC:70A
LL:1.5m ohm



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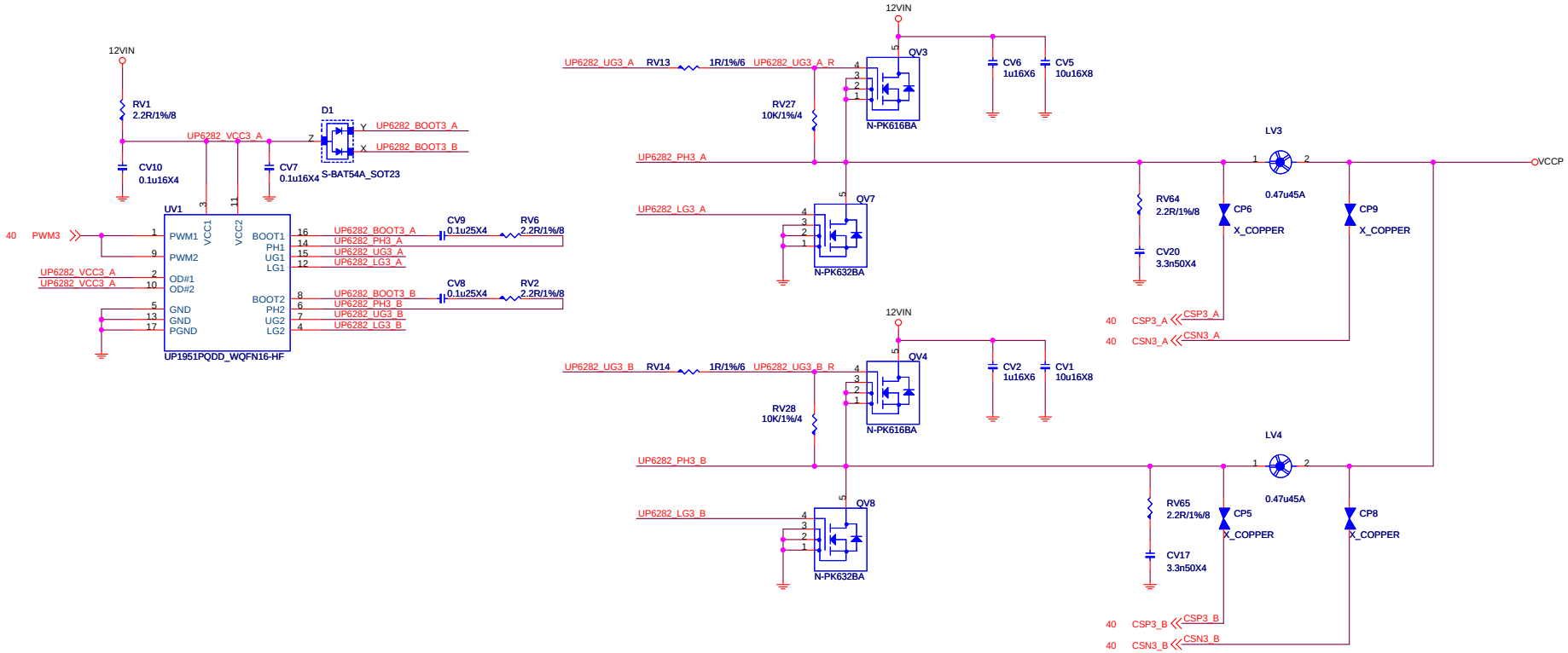

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DDR Power:1.5V

DDR3_1.5V 4.2A+12A+1.115A+6A=23.315A

4.2A FOR CPU
12A FOR 4DIMM
1.115A FOR VTT_DDR
PCH Core 6A
OCP 23.315A*1.5=34.9725A
OCP=[20uA*Rocs(R320)]/4*Rdson(Low side NXP)2mohm
R320=14K ohm

Iripple=7.934729A

23.315A

DDR3_1.5V

(OS-CON CAP)

5VDIMM_IN — C43 10u6.3X6 — C32 0.1u10X4 — EC5 560u6.3SO — EC6 560u6.3SO — CHOKE1 CH-1.2u15A1.7m-RH — 5VDIMM — C22 0.1u10X4

+12V — D8 S-BAT54C_SOT23 — 5VDIMM — R135 2.2R/1%/8 — DDR_1504_VCC — C67 1u16X6

Internal 0.6

VCC_DDR — R146 1K/1%/4 — DDR3_FB — R145 0R/4 — C75 0.01u16X4 — V1.0

((R569/R317)+1)*0.6=1.5V

分壓

U9 UP1504SSU8_PSOP8-HF: DDR_0_6_REF_R, REFIN, VCC, BOOT, PHASE, UGATE, LGATE, FB, GND, OCS

1504_DDR_BOOT1 — R127 2.2R/1%/8C59 — 0.1u16X4

1504_DDR_PH1 — 1504_DDR_UG1 — 1504_DDR_LG1

R136 665R/1%/4 — R129 14K/1%/4 — **OCP=35A**

R126 2.2R/1%/8 — C58 3.3n50X4

CHOKE2 CH-1.1u32A1.4m-RH

VCC_DDR — EC12 560u6.3SO — EC9 560u6.3SO — EC10 560u6.3SO — C133 1u6.3X4 — C170 22u6.3X8 — C86 10u6.3X6 — C95 10u6.3X6

R137 0R/4 — DDR3_FB_R — DDR3_FB_R 46

5VDIMM_IN

1504_DDR_UG1 — R114 1R/1%/6 — 1504_DDR_UG1_R — Q15 N-PK616BA — R113 10K/1%/4

1504_DDR_UG1_R — Q14 N-PK616BA

1504_DDR_PH1

1504_DDR_LG1 — Q22 N-PK632BA

1504_DDR_LG1 — Q19 N-PK632BA

VCC_DDR — C486 X_22u6.3X8 — C484 X_22u6.3X8 — C485 X_22u6.3X8 — C116 22u6.3X8 — C117 22u6.3X8 — C171 22u6.3X8 — C143 22u6.3X8 — C80 22u6.3X8

DDR_0_6_REF_R

ATX_5VSB — R115 10K/4 — DDR3_ENB — Q18 2N7002 — C51 X_0.1u10X4

11,22,34,39,46 — SLP_S4# — R95 4.7K/4 — Q16 2N3904

5VDIMM — R635 10K/4 — Q50 2N7002 — R634 X_0R/4 — R680 100K/1%/4 — C304 1u16X6

V1.0

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

VCC5 — CP1 X_COPPER — close to pin6

U18 UP0109PSW8_PSOP8-HF 1.25V/2.9A: NC3, NC2, VCNTL, NC1, VIN, GND, REFIN, VOUT, GND

VCC_DDR — VCC_DDR — R198 10K/1%/4 — DDRVTT_VREF — per DIMM

1.115A VTT_DDR

C180 0.1u10X4 — C465 0.1u10X4 — R204 10K/1%/4 — C211 0.1u10X4 — C217 0.1u10X4 — C216 0.1u10X4 — C218 0.1u10X4 — C179 22u6.3X8 — C183 22u6.3X8

P.S. Only for meet Intel power down sequence.

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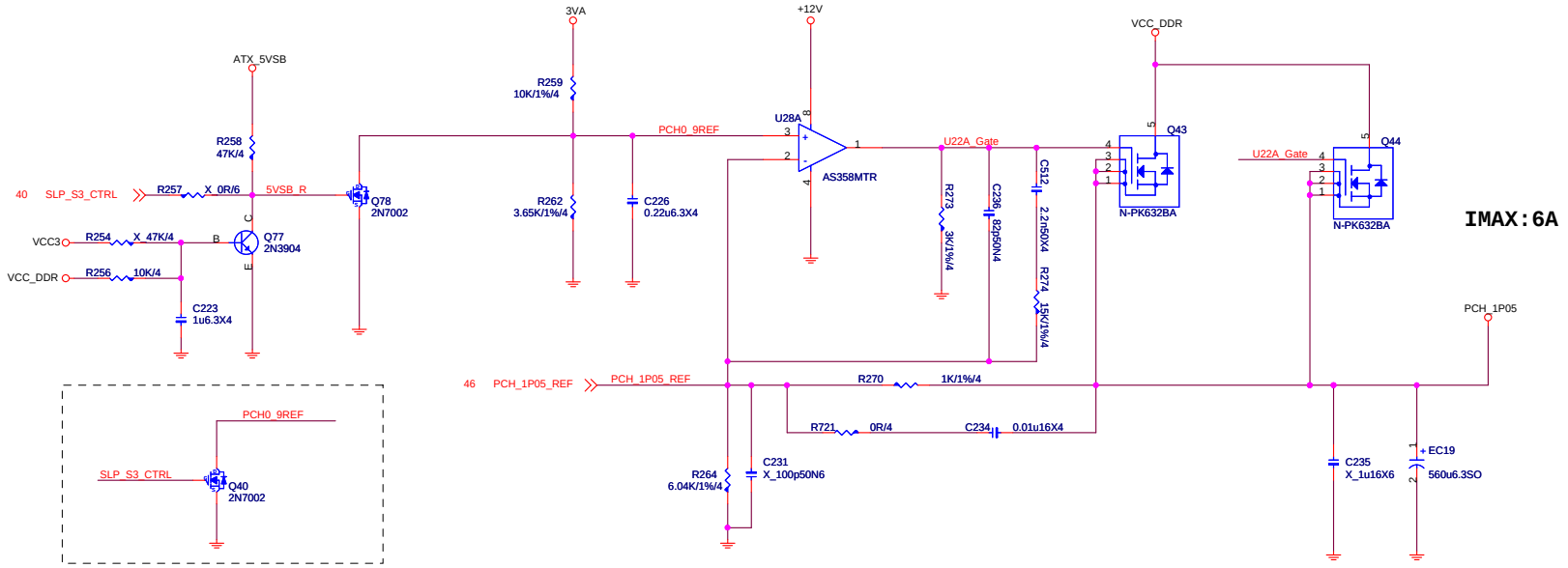
PCH Power:1.05V

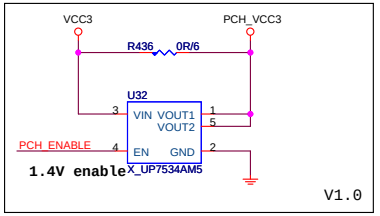
PCH Core 6A



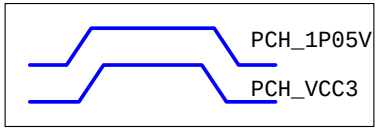
IMAX:6A

PCH Power:3.3V

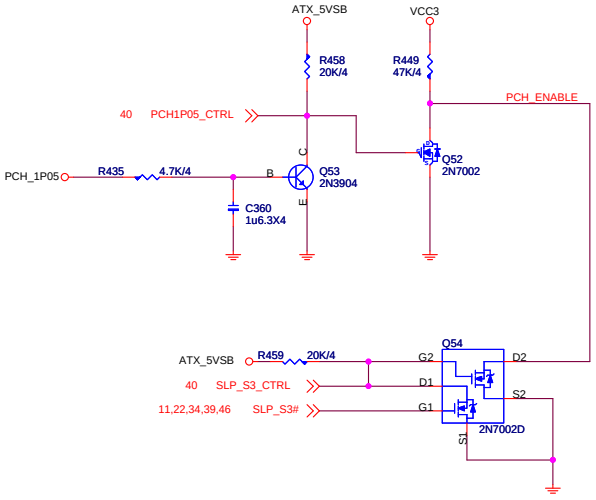
0.133A



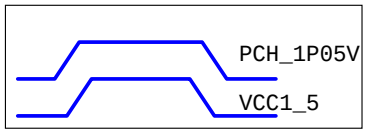
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



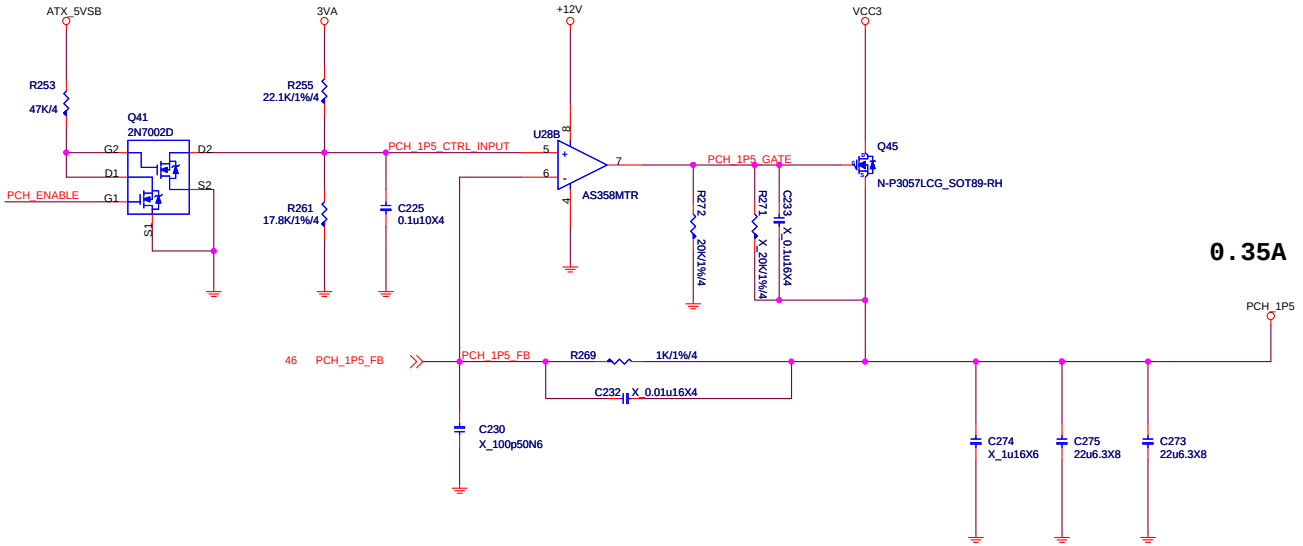
Waitting PCH_1P05 Ready



VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



PCH Power:1.5V



0.35A

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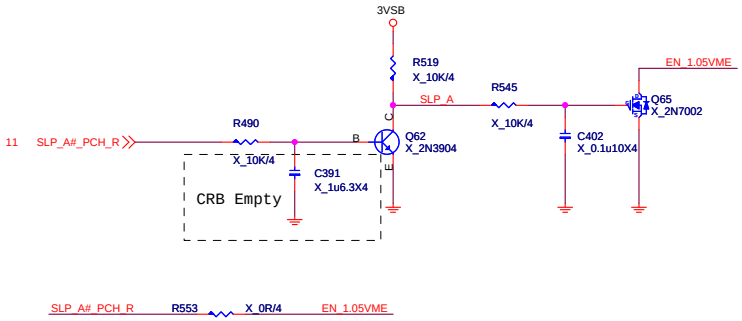
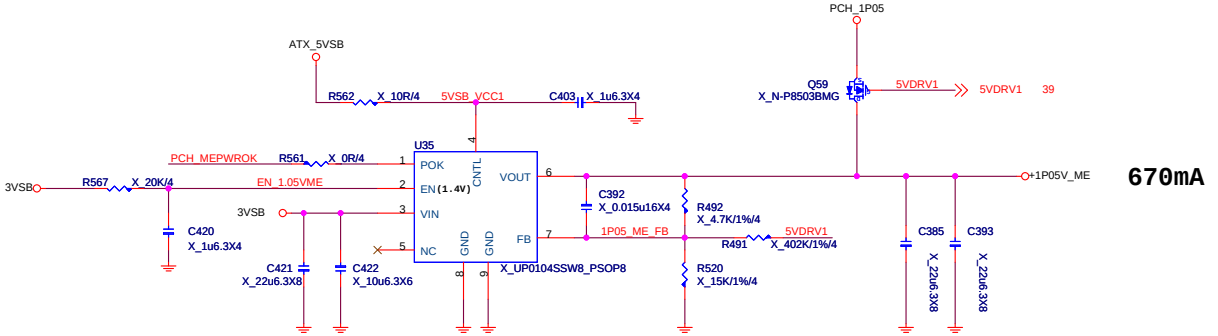
SLP_A

ME Power Control

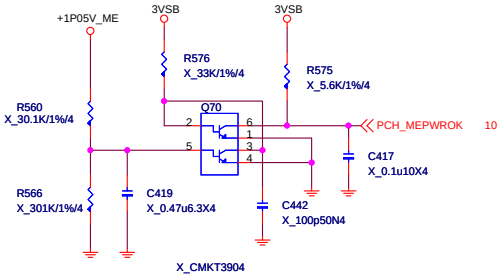


+1.05V_ME(VCCIO_ME)

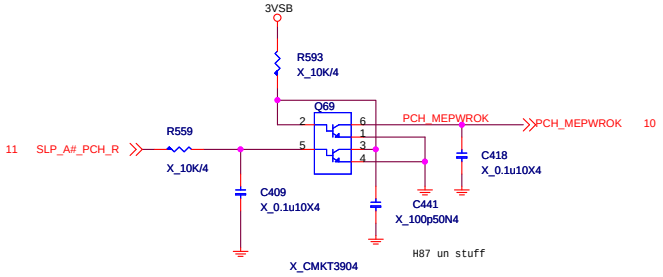


670mA

PCH_MEPWROK

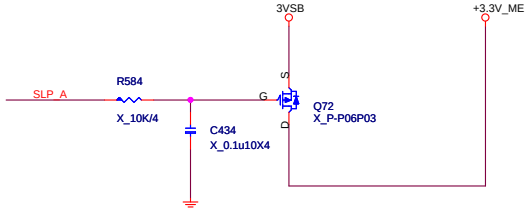


VccASW active to APWROK high 1ms



APWROK falling to VccASW falling 40ns

+3.3V_ME



For INTEL ME BUG

Z97->Stuff R569
H97->Stuff R570

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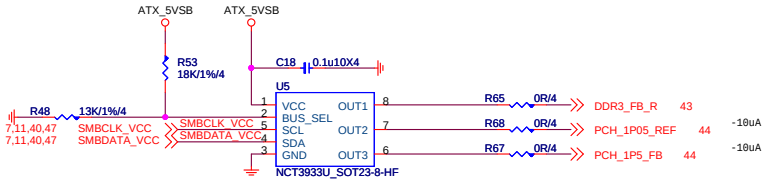
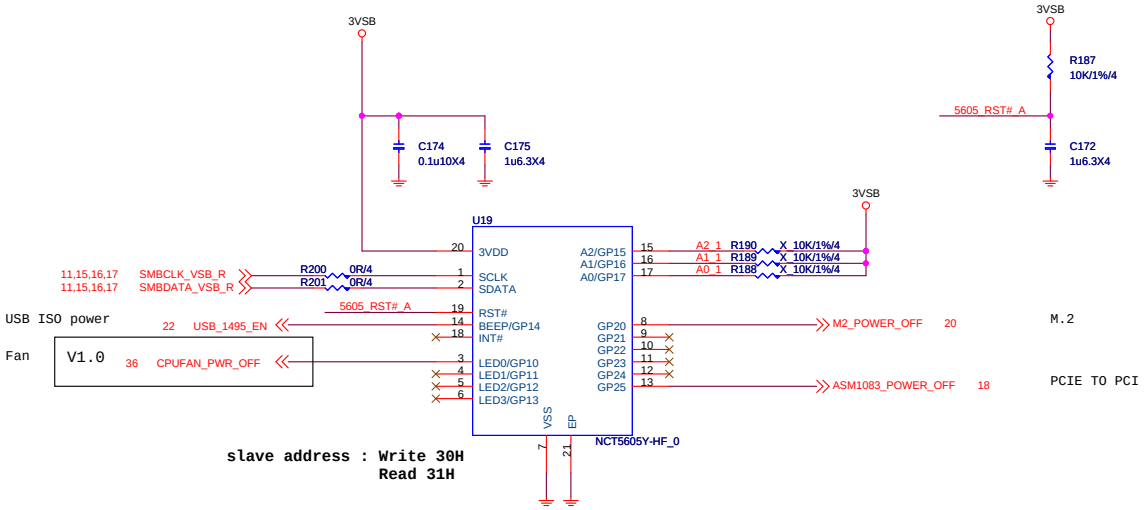
0x26:RH=18K,RL=13K

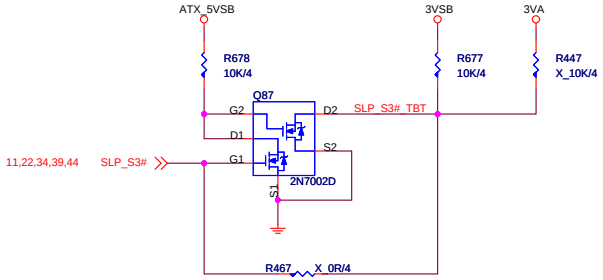


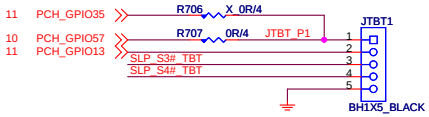
Close TO VCC_DDR Plan



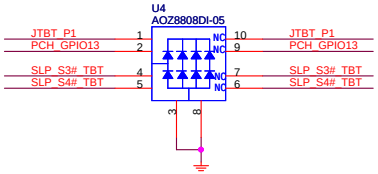
slave address : Write 30H
Read 31H

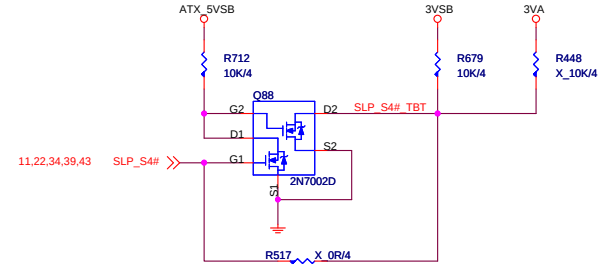
JTBT





N32-1050271-H06

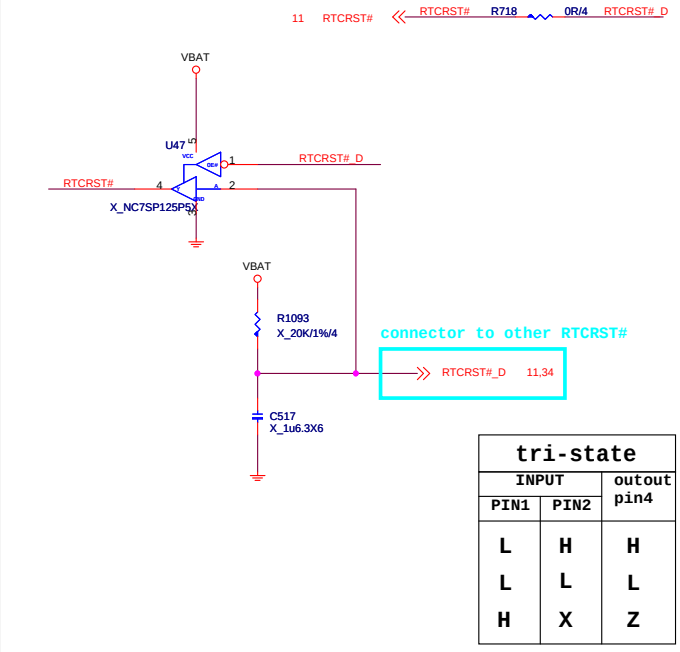




V1.0

V1.0

co-lay



tri-state		
INPUT		outout pin4
PIN1	PIN2	
L	H	H
L	L	L
H	X	Z

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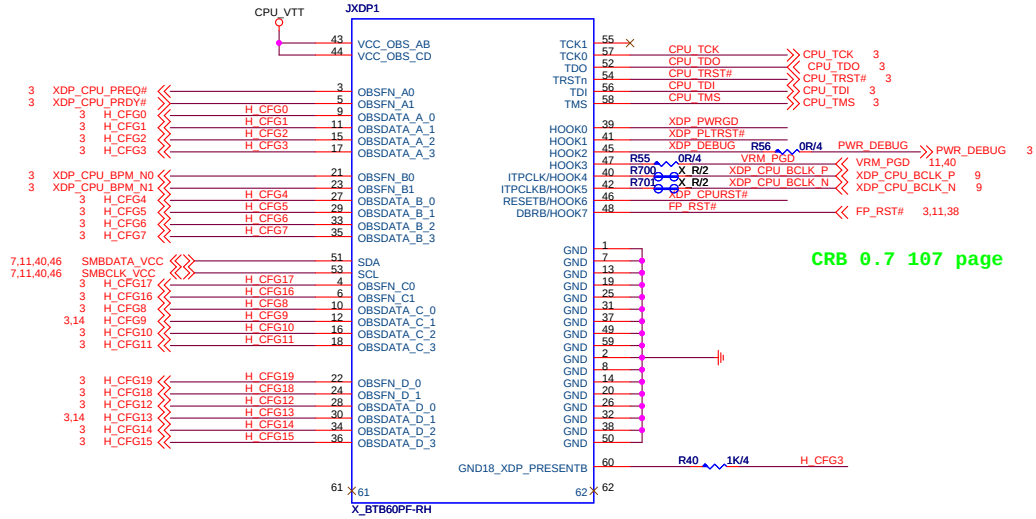
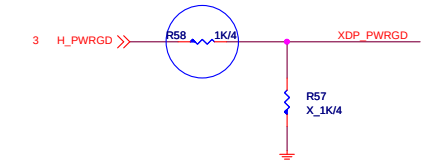
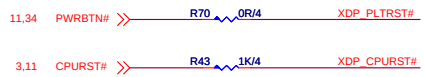
Reserve debug port 5020



CRB 0.7 107 page

mow15





PLACE NEAR XDP CONNECTOR

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PCB

7918_10

PD0-0791810-G37,精成,23,寶安恩斯邁廠(MSIS)
PD0-0791810-G37,精成,77,寶安恩斯邁廠(MSIS)
PD0-0791810-E48,競華,23,寶安恩斯邁廠(MSIS)
PD0-0791810-E48,競華,77,寶安恩斯邁廠(MSIS)

SBC_LA1
Label
SBC
SBC LABEL

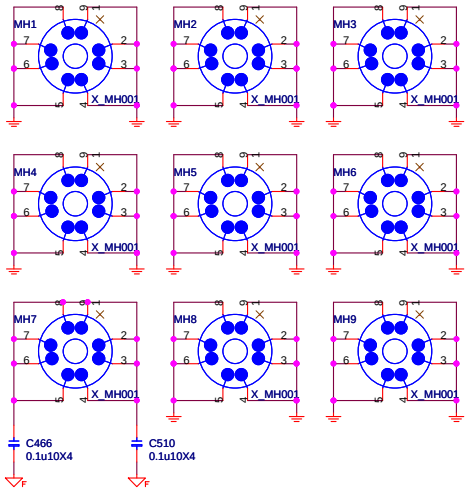
CPU_H1
CPU
鐵座
CPU_H1

BAT1_X1
BAT-BCR2032P-RH

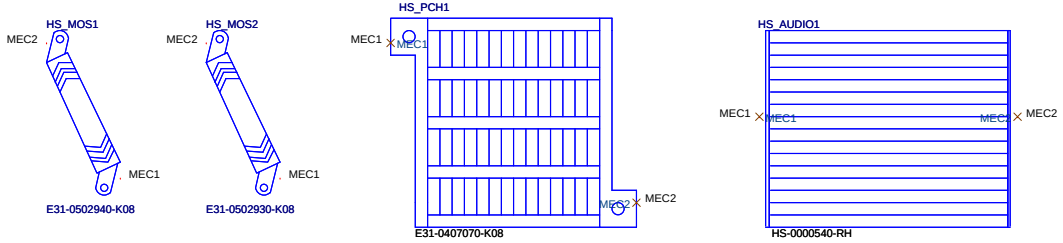
HDMI_LA1
Label
HDMI
HDMI LABEL

AMI_LA1
AMI_BIOS LABLE
BIOS_LABLE

Mounting Holes



HEATSINK



SPI OPT.

SPI_128
SPI
8M
X_W25Q128FVSIQ-HF

H97 OPT.

U0H97
LPT
H97
X_H97

LAH97
Label
H97-Gaming3
X_MKT-LABEL

Z97 OPT.

LAZ97
Label
Z97-Gaming3
MKT-LABEL

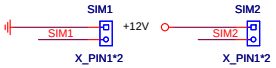
B85 OPT.

U0B85
LPT
B85
X_B85

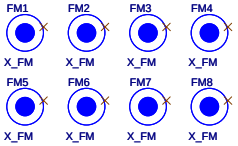
LAB85
Label
B85-Gaming3
X_MKT-LABEL

CNTUSB1
USB3
Co-lay
USB2
X_USB2
N53-08M0611-F02

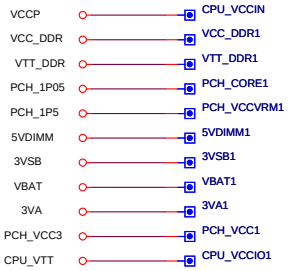
Simulation



Optical Fiducial Marks-120



Test point



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Size	Document Description	Rev
Custom	EMI CAP	1.0

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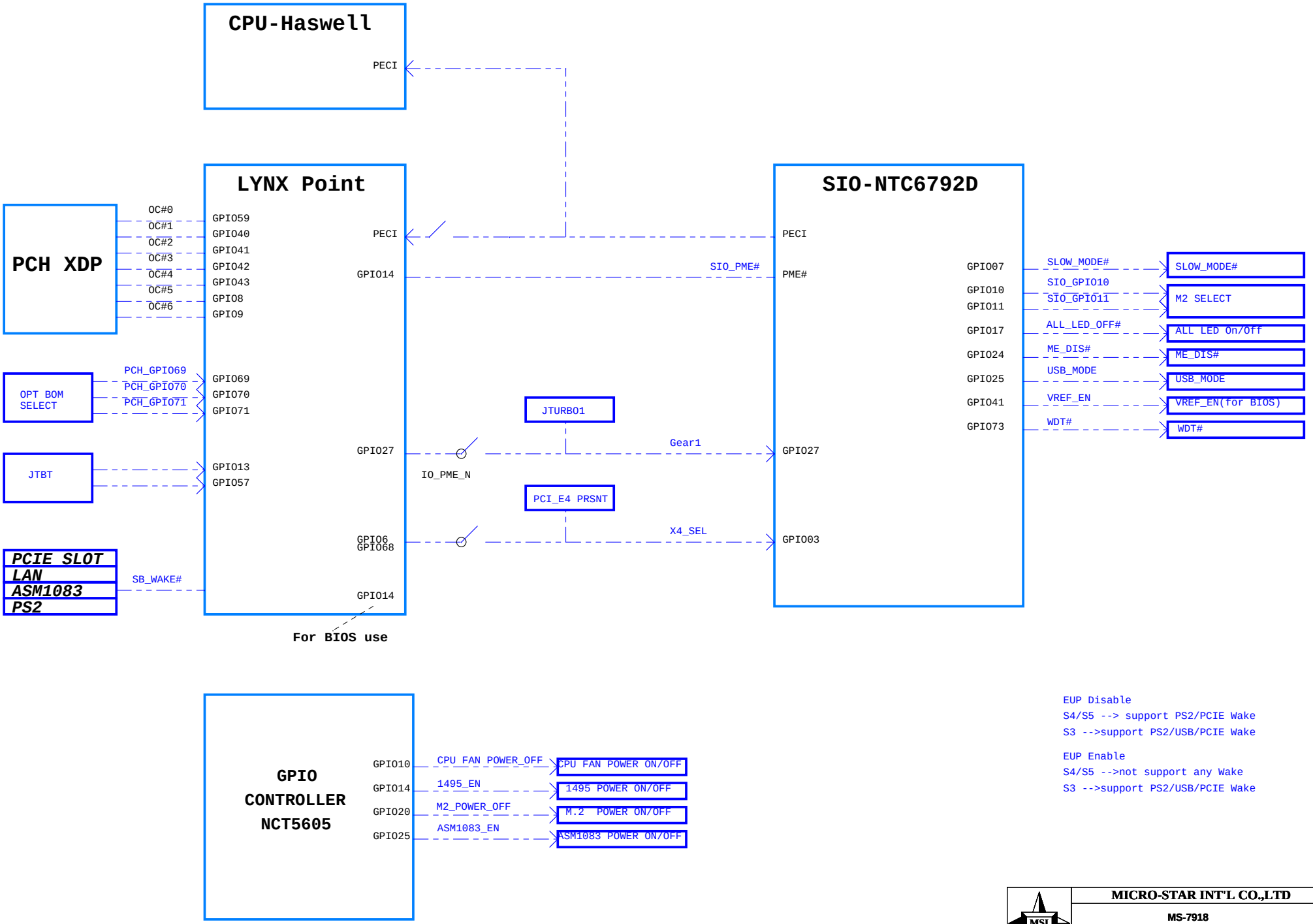

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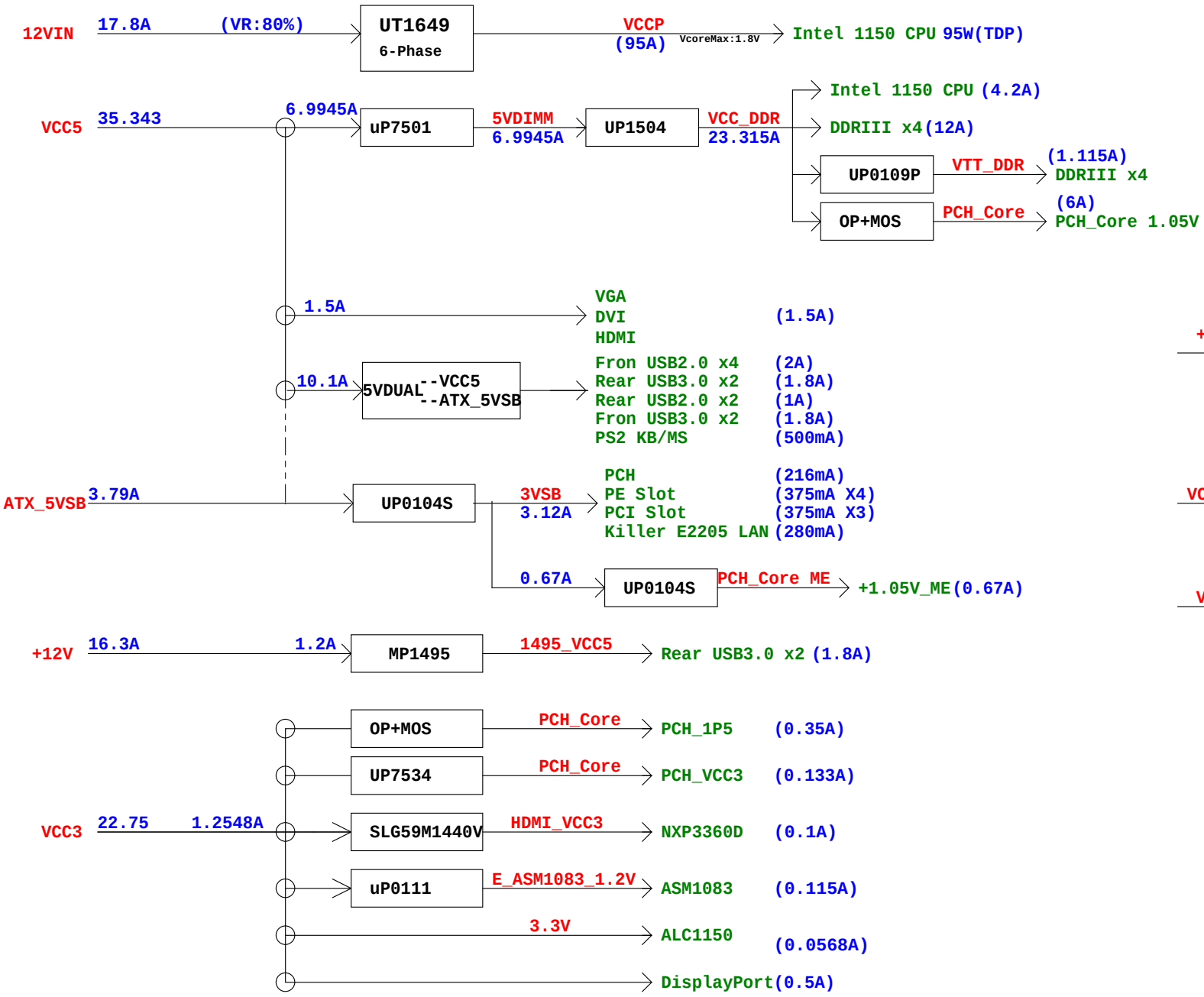
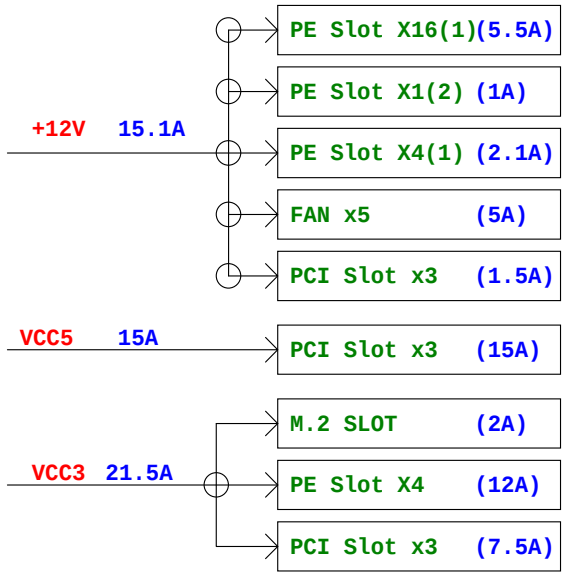
Power Delivery



Slot

PCI slot (X3)	
+3.3Vaux (wake)	- 1125mA
+3.3Vaux (no wake)	- 60mA
+3.3V	- 7.6A
+5V	- 15A
+12V	- 1.5A



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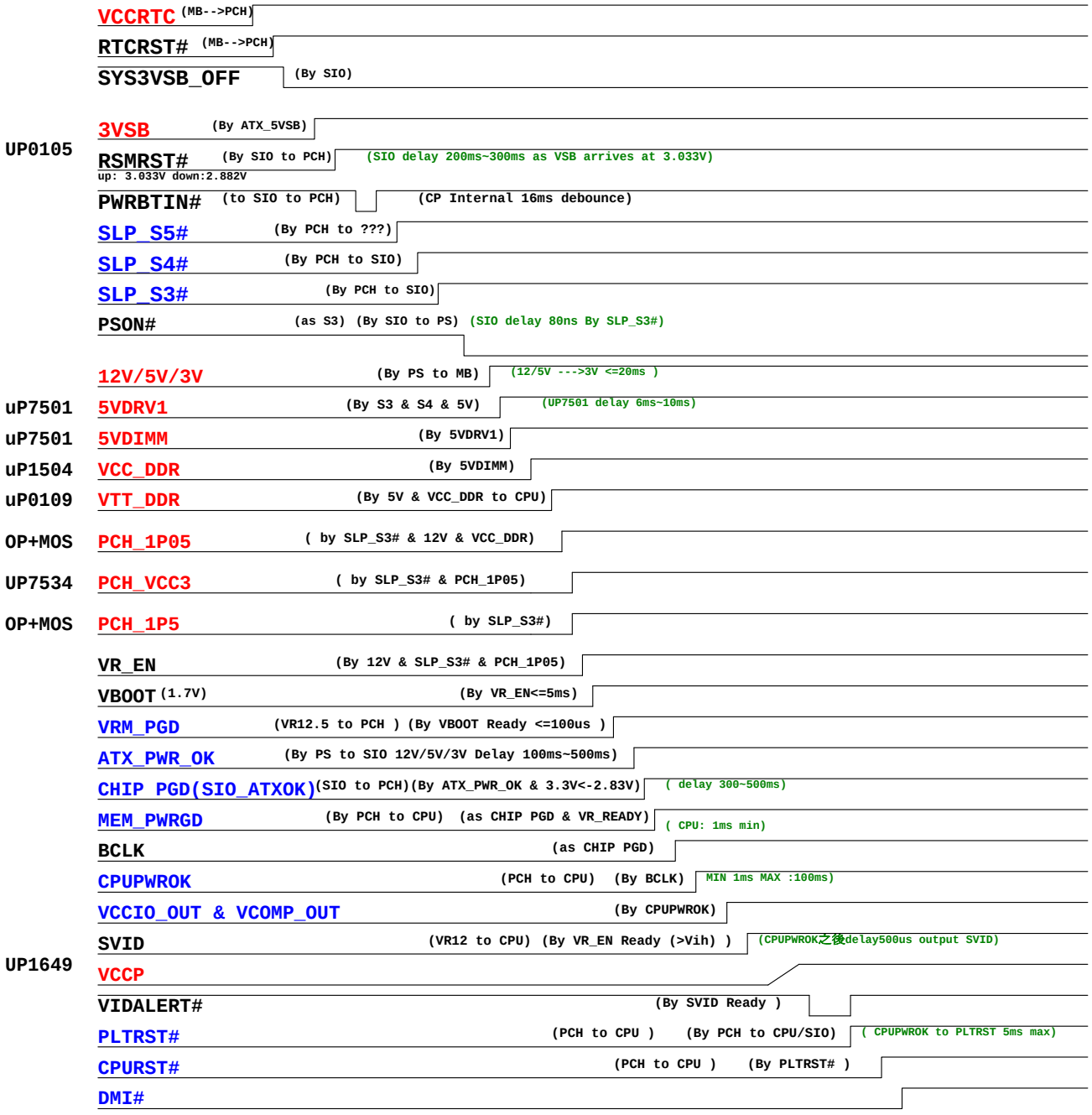
(G3)DS5 ---> S0



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0A To 1.0

Page 3 Remove PLTRST# Co-lay CPU_RESET#

Page 5 Add 22u*7 ON CPU SOCKET BOTTOM Side

page 10 Remove R424 Add R717,R718,R719
        Add R722 For Gear1

Page 11 C348,C349 change to 12P
        R343 un-stuff

Page 17 Remove R447 R448 R467 R517 Q50 Q51
        add R134 R62 R711 R171 R44 R133 Q31 Q5
        For PCI_E4 X4 SEL Function

Page 20 Add R715,Q42

Page 22 Add C501,R708 For MP1495
        Add Q51,Q91,R713,R647,R720 For OC#0 Level Shift

Page 24 Add C511 For USB Drop

Page 25 Add C502 For MP1495
        Remove R196,R197 For OC#0

Page 29 U11 change to NXP,R141 9.09K,C70,Remove HDMI cut power

Page 31~33 Change CA33,CA45 to -12V_A

Page 34 CP17,L12 change to 0R/0402
        Change R618 Pull high to SIO_3VA
        C462 Stuff
        R516 un-stuff
        Add SIO_GP16 For M.2
        Change GP27 NetName to Gear1

Page 36 Add Fan Cut Power circuit
        R45,R50,Q92,Q93,C756,C757

PAge 38 R683 Pull-up to PCH_VCC3
        R682 Pull-up to M2_VCC3
        R475,R469,Q55 un-stuff
        R483 stuff
        Add D27,D28

Page 39 Q61 Reverse NET 3VSB,VCC3
        Remove 3VA Power Down circuit.
        Remove PEG Co-lay circuit

Page 40 RV87 1.8K
        RV84 1.1K
        RV91,RV51 54.9K
        RV82 499R
        RV49 1K
        RV66 48K
        RV11 Change to 0402
        Add RV115 for Slow Mode

Page 43 R145,C75 Stuff
        Add Q50,R635,R680,C304 for sequence
        Add C465

Page 44 Add C512,R721 For Type 2&3
            U32 Un-stuff
            R436 stuff

Page 46 Add R447,R488 Pull-up to 3VA
        Add R706,R707 for Co-lay GPIO
        Change R677,R679 Pull-up to 3VSB
        Change ESD
        Change U19.3/GPIO10 For Fan cut power

Model	Sample BOM	chipset	Market Name	BIOS Define
MS-7918 10	601-7918-XXX	Z97 chipset	Z97 GAMING 3	E7918ims.2XX
MS-7918 10	601-7918-XXX	H97 chipset	H97 GAMING 3	E7918ims.1XX
MS-7918 10	601-7918-XXX	B85 chipset	B85 GAMING 3	E7918ims.3XX

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