Plano Intel 11.6" Schematics Document

Braswell

2015-04-24
REV : A00

DY : None Installed
XDP: For CPU XDP Debug Port installed
PCH_XDP: For PCH XDP Debug Port installed

A00

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Title: *Cover Page*

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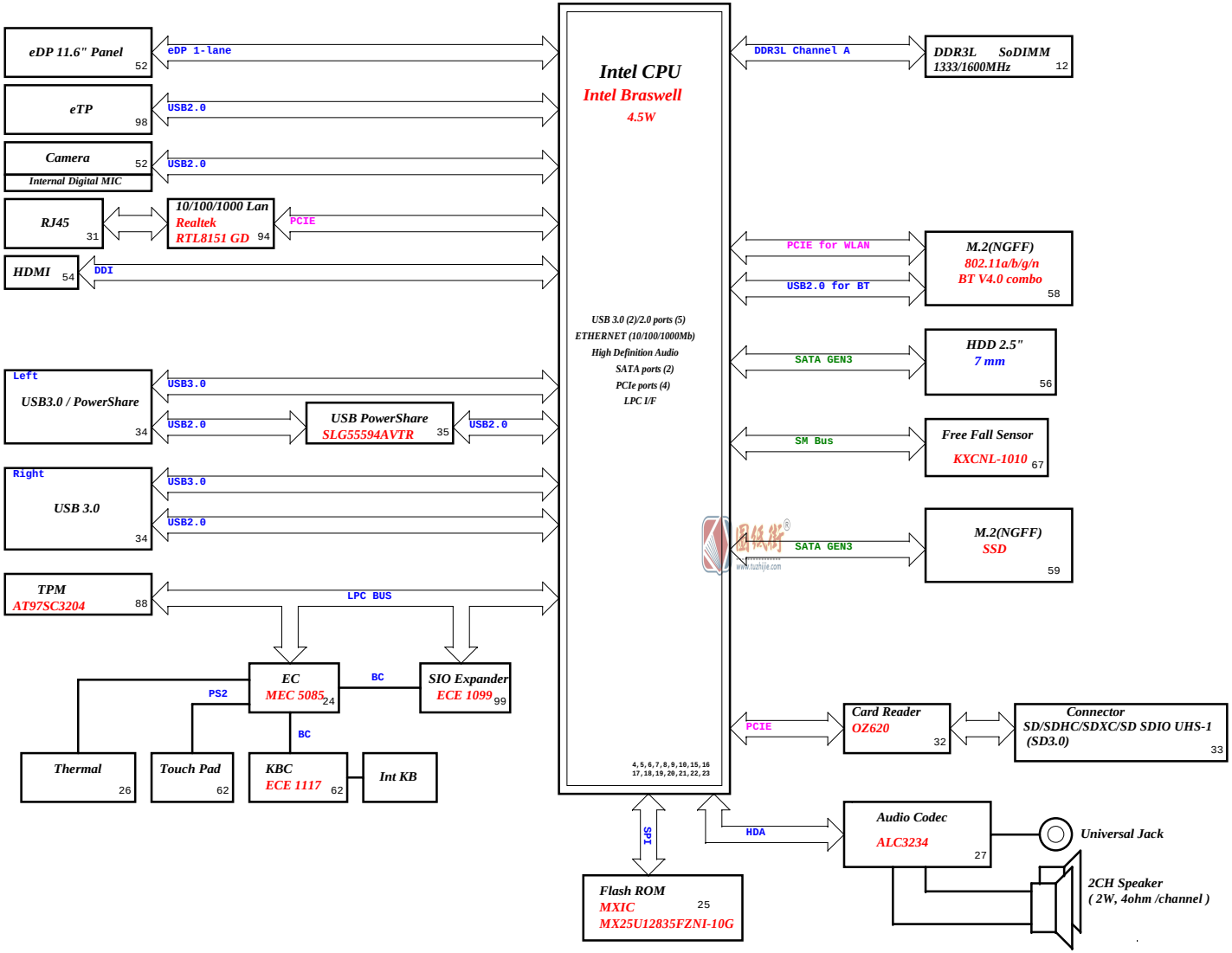
Plano 11.6" Block Diagram

Project code : 4PD03Y010001
PCB P/N : 13329
Revision : 2



CHARGER
BQ24715 — 44

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC
TPS51225 — 45

INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 3D3V_S5 5V_S5

CPU DC/DC
RT8199BGQW*2 — 46~48

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE0 GFX_CORE

SYSTEM DC/DC
SY8206DQNC & RT8068 — 50

INPUTS	OUTPUTS
DCBATOUT 3D3V_S5	1D05V_S5 1D15V_S5

SYSTEM DC/DC
SY8206DQNC & APL5338 — 49

INPUTS	OUTPUTS
DCBATOUT 1D35V_S3	1D35V_S3 0D675V_S0 DDR_VREF_S3

SYSTEM DC/DC
S-1339D15-M5001
RT9043GB & SYW232 — 51

INPUTS	OUTPUTS
3D3V_S5	1D5V_S0 1D24V_S5 1D8V_S5

Load Switches — 36

INPUTS	OUTPUTS
5V_S5 3D3V_S5 1D8V_S5	5V_S0 3D3V_S0 3D3V_LAN 3D3V_S5_PRIME 1D8V_S0

PCB LAYER(FR4-6 Layer)
L1:Top
L2:PWR/GND
L3:Signal
L4:Signal
L5:PWR/GND
L6:Bottom

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Title: Block Diagram

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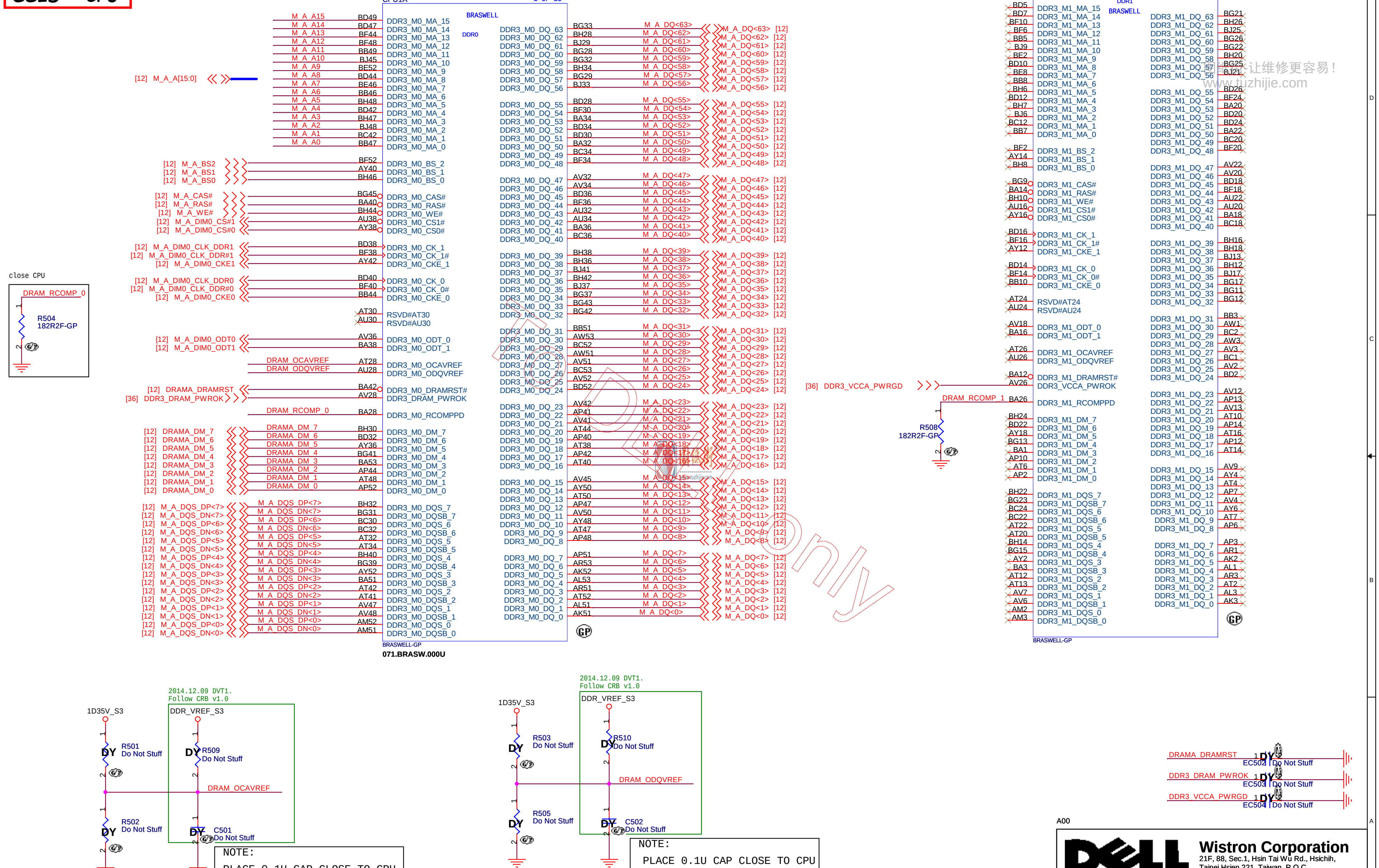
SSID = CPU



NOTE:
PLACE 0.1U CAP CLOSE TO CPU

PLACE TWO 4.7K RESISTORS CLOSE TO CPU TO CPU PINS ON M_VREF ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

NOTE:
PLACE 0.1U CAP CLOSE TO CPU

PLACE TWO 4.7K RESISTORS CLOSE TO CPU TO CPU PINS ON M_VREF ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

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Title: CPU (DDR)

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SSID = CPU

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Title

CPU (CFG)

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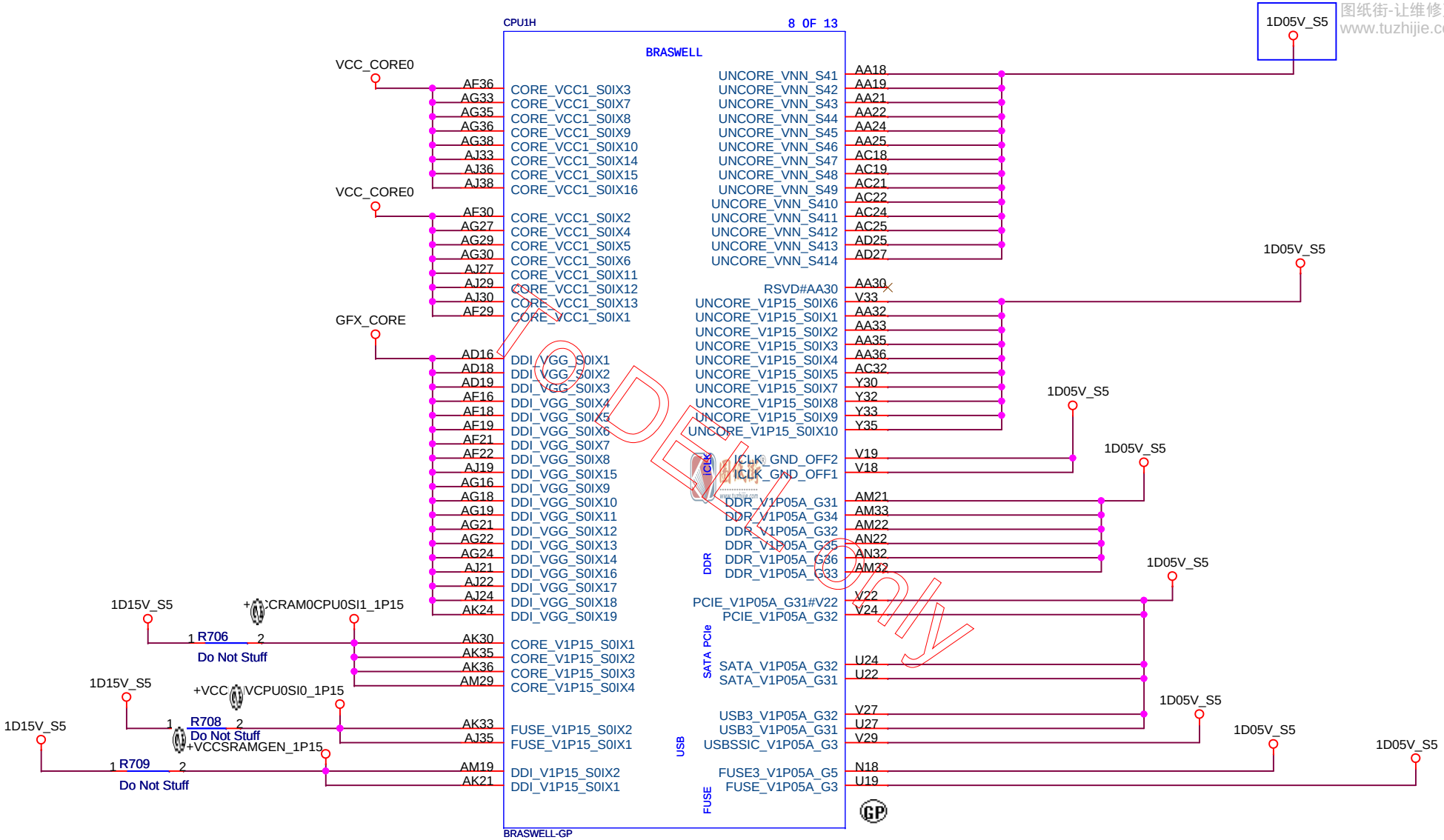
SSID = CPU

2014.09.25 EVT.
VNN change to 1D05V_S5



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Title: CPU (VCC_CORE)

Size	Document Number	Rev
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SSID = CPU

CPU1C — 3 OF 13 — BRASWELL

Rev 0.92

10.8 Unused Interface Termination

Table 10-4. MIPI*-CSI-2 Pins

Signal Name	Action
MCSI_[3:1]_CLKN MCSI_[3:1]_CLKP	No connect
MCSI_1_DN[0:3] MCSI_1_DP[0:3] MCSI_2_DN[0:1] MCSI_2_DP[0:1]	No connect
MCSI_RCOMP	Connect to ground with 150 Ohms ±1% resistor

NOTE: If a x1 or x2 or x3 Camera is used on MCSI_X4 port, causing some lines to be unconnected, these unused signals can be no connect.

HDMI

1D8V_S5 — RN801 SRN2K2J-1-GP CRB 2.2k

[54] HDMI_DATA2 / [54] HDMI_DATA2# — D50 / C51 — DDI0_TXP_0 / DDI0_TXN_0
[54] HDMI_DATA1 / [54] HDMI_DATA1# — H49 / H50 — DDI0_TXP_1 / DDI0_TXN_1
[54] HDMI_DATA0 / [54] HDMI_DATA0# — F53 / F52 — DDI0_TXP_2 / DDI0_TXN_2
[54] HDMI_CLK / [54] HDMI_CLK# — G53 / G52 — DDI0_TXP_3 / DDI0_TXN_3
DDI0_AUXP — H47
DDI0_AUXN — H46
[54] HDMI_PCH_DET# — W51 — HV_DDI0_HPD
[54] PCH_HDMI_CLK — Y51 — HV_DDI0_DDC_SCL
[54] PCH_HDMI_DATA — Y52 — HV_DDI0_DDC_SDA
V52 — PANEL0_BKLTEN
V51 — PANEL0_BKLTCTL
W53 — PANEL0_VDDEN
R802 402R2F-GP — DDI0_PLLOBS_P — F38
DDI0_PLLOBS_N — G38
DDI0_PLLOBS_P
DDI0_PLLOBS_N

1.35V / 1.8A — DDI0

Braswell-M/D Platform Display Configuration

	Default	1	2	3	4	5	6	7
DDI-0	DP	DP	DP	DP	HDMI	HDMI	HDMI	HDMI
DDI-1	eDP	eDP	DP	HDMI (Intrp)	eDP	eDP	DP	HDMI (Intrp)
DDI-2	HDMI	DP	HDMI	HDMI	HDMI	DP	HDMI	HDMI
PCU UART	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No

R813 1MR2J-1-GP — L_BKLT_EN_CPU

EDP

[52] eDP_TXP0_CPU / [52] eDP_TXN0_CPU — J51 / H51 — DDI1_TXP_0 / DDI1_TXN_0
K51 / K52 — DDI1_TXP_1 / DDI1_TXN_1
L53 / L51 — DDI1_TXP_2 / DDI1_TXN_2
M52 / M51 — DDI1_TXP_3 / DDI1_TXN_3
[52] eDP_AUXP_CPU — M42 — DDI1_AUXP
[52] eDP_AUXN_CPU — K42 — DDI1_AUXN
[52] EDP_HPD# — R51 — HV_DDI1_HPD
L_BKLT_EN_CPU — P51
L_BKLT_CTRL_CPU — P52
LVDS_VDD_EN_CPU — R53
R801 402R2F-GP — DDI1_PLLOBS_P — F47
DDI1_PLLOBS_N — F49
DDI1_PLLOBS_P
DDI1_PLLOBS_N

1.35V / 1.8A — DDI1

DDI2_TXP_0 — F40 / DDI2_TXN_0 — G40
DDI2_TXP_1 — J40 / DDI2_TXN_1 — K40
DDI2_TXP_2 — F42 / DDI2_TXN_2 — G42
DDI2_TXP_3 — D44 / DDI2_TXN_3 — F44
DDI2_AUXP — D48 / DDI2_AUXN — C49
HV_DDI2_HPD — U51 — HV_DDI2_HPD
[16] UART1_TX — T51 — HV_DDI2_DDC_SCL
[16] UART1_RX — T52 — HV_DDI2_DDC_SDA
CRB:UART TO USB PORT

1.8A — DDI2

PDG 0.92 Modify

Table 25-16. DDI Disable Guidelines

Signal	Recommendation
DDIx_TXP[3:0] DDIx_TXN[3:0]	NC
DDIx_AUXP DDIx_AUXN	NC
HV_DDIx_HPD HV_DDIx_DDC_SCL HV_DDIx_DDC_SDA	NC
PANELx_VDDEN PANELx_BKLTEN PANELx_BKLTCTL	NC
DDIx_PLLOBS_P and N	Connect P and N signal with one 402 ohms ± 1% resistor

DDI2 do not support eDP

RSVD#B53 / RSVD#A52 / RSVD#E52 / RSVD#D52 / RSVD#B50 / RSVD#B49 / RSVD#E53 / RSVD#C53 / RSVD#A51 / RSVD#A49 / RSVD#G44 — NC's

1D8V_S5 — R816 DY Do Not Stuff — HV_DDI2_HPD — EVT DY — R819 DY Do Not Stuff

MCSI and Camera interface

RSVD#M44 / RSVD#K44 — M44 / K44
RSVD#K48 / RSVD#K47 — K48 / K47
MCSI_1_CLKP — T44
MCSI_1_CLKN — T45
MCSI_1_DP_0 — Y47
MCSI_1_DN_0 — Y48
MCSI_1_DP_1 — V45
MCSI_1_DN_1 — V47
MCSI_1_DP_2 — V50
MCSI_1_DN_2 — V48
MCSI_1_DP_3 — T41
MCSI_1_DN_3 — T42
MCSI_2_CLKP — P50
MCSI_2_CLKN — P48
MCSI_2_DP_0 — P47
MCSI_2_DN_0 — P45
MCSI_2_DP_1 — M48
MCSI_2_DN_1 — M47
RSVD#T50 / RSVD#T48 — T50 / T48
MCSI_COMP — P44 — MCSI_COMP — R817 150R2F-1-GP

1.8A
GP_CAMERASB00 — AB41 — GP_CAMERASB00 [96]
GP_CAMERASB01 — AB45 — GP_CAMERASB01 [96]
GP_CAMERASB02 — AB44 — GP_CAMERASB02 [96]
GP_CAMERASB03 — AC53 — GP_CAMERASB03 [96]
GP_CAMERASB04 — AB51 — GP_CAMERASB04 [96]
GP_CAMERASB05 — AB52 — GP_CAMERASB05 [96]
GP_CAMERASB06 — AA51 — GP_CAMERASB06 [96]
GP_CAMERASB07 — AB40 — GP_CAMERASB07 [96]
GP_CAMERASB08 — Y44 — GP_CAMERASB08 [15,96]
GP_CAMERASB09 — Y42 — GP_CAMERASB09 [15]
GP_CAMERASB10 — Y41
GP_CAMERASB11 — V40 — GP_CAMERASB11 [15]

To XDP

Table 21-3. e-MMC* Component Characteristics

Component	Description	Specifications
R_{COMP}	Compensation resistor	100 Ω ±1%
R_S	Series Resistor	0~10 Ω
Note:	Rs need to be placed close to the device.	

21.2.2 SDMMC1_RCOMP Compensation Guidelines

SDMMC1_RCOMP signal requires a 100 Ω ±1% pull-down resistor, placed as close as possible to SoC.

1.8A — SDMMC1
SDMMC1_CLK — M7
SDMMC1_CMD — P6
SDMMC1_D0 — M6
SDMMC1_D1 — M4
SDMMC1_D2 — P9
SDMMC1_D3_CD# — P7
MMC1_D4_SD_WE — T6
MMC1_D5 — T7
MMC1_D6 — T10
MMC1_D7 — T12
MMC1_RCLK — T13
SDMMC1_RCOMP — P13 — SDMMC1_RCOMP — 2014.12.10 DVT1. Follow CRB v1.0 — R814 100R2F-L1-GP-U

1.8A — SDMMC2
SDMMC2_CLK — K10
SDMMC2_CMD — K9
SDMMC2_D0 — M12 — LCD_CBL_DET# [52]
SDMMC2_D1 — M10 — HDD_DET# [56]
SDMMC2_D2 — K7 — CAMERA_DET# [52]
SDMMC2_D3_CD# — K6 — KB_DET# [62]

3.3 — SDMMC3
SDMMC3_CLK — F2 — ONE_DIMM
SDMMC3_CMD — D2 — 3.3V_CAM_EN# [52]
1.8A — SDMMC3_CD# — K3
SDMMC3_D0 — J1 — 3.3V_TP_EN [62]
SDMMC3_D1 — J3 — 3.3V_mSATA_EN [59]
SDMMC3_D2 — H3 — 3.3V_HDD_EN [56]
SDMMC3_D3 — G2 — FFS_INT2 [67]
SDMMC3_1P8_EN — K2
SDMMC3_PWR_EN# — L3
SDMMC3_RCOMP — P12 — SDMMC3_RCOMP — R815 80D6R2F-L-GP

Set as GPIO. Use during factory verification process.
reserve pull high 3D3V_S0 in FFS side

2014.10.3 EVT. Install R823 for SW request.

1D8V_S5
2014.10.29 eVT stuff
LCD_CBL_DET# — R830 100KR2J-1-GP
HDD_DET# — R812 100KR2J-1-GP
CAMERA_DET# — R823 100KR2J-1-GP
KB_DET# — R820 100KR2J-1-GP
2014.10.29 EVT stuff

3D3V_S5_PRIME
2014.11.28 DVT1 add
3.3V_CAM_EN# — R826 10KR2F-2-GP
3.3V_TP_EN — R831 10KR2F-2-GP
3.3V_mSATA_EN — R818 10KR2F-2-GP
3.3V_HDD_EN — R824 10KR2F-2-GP

3D3V_S5_PRIME
R827 100KR2J-1-GP — ONE_DIMM
2015.02.25 DVT2 change from 10 to 100k.
DY R828 Do Not Stuff

Level shift

3D3V_S0 / 1D8V_S0 / 1D8V_S5
R803 2K2R2J-2-GP — R804 2K2R2J-2-GP — R805 DY Do Not Stuff
LVDS_VDD_EN_B — Q801 LMBT3904LT1G-GP
[24,36] LVDS_VDD_EN_CPU
84.T3904.H11
2nd = 84.T3904.K11
3rd = 84.03904.E11

3D3V_S0 / 1D8V_S0 / 1D8V_S5
R806 2K2R2J-2-GP — R807 2K2R2J-2-GP — R808 DY Do Not Stuff
L_BKLT_CTRL_B — Q802 LMBT3904LT1G-GP
[52] L_BKLT_CTRL — L_BKLT_CTRL_CPU
84.T3904.H11
2nd = 84.T3904.K11
3rd = 84.03904.E11

3D3V_S0 / 1D8V_S0 / 1D8V_S5
R810 10KR2J-3-GP — R809 2K2R2J-2-GP — R811 DY Do Not Stuff
L_BKLT_EN_B — Q803 LMBT3904LT1G-GP
[52] L_BKLT_EN — L_BKLT_EN_CPU
84.T3904.H11
2nd = 84.T3904.K11
3rd = 84.03904.E11

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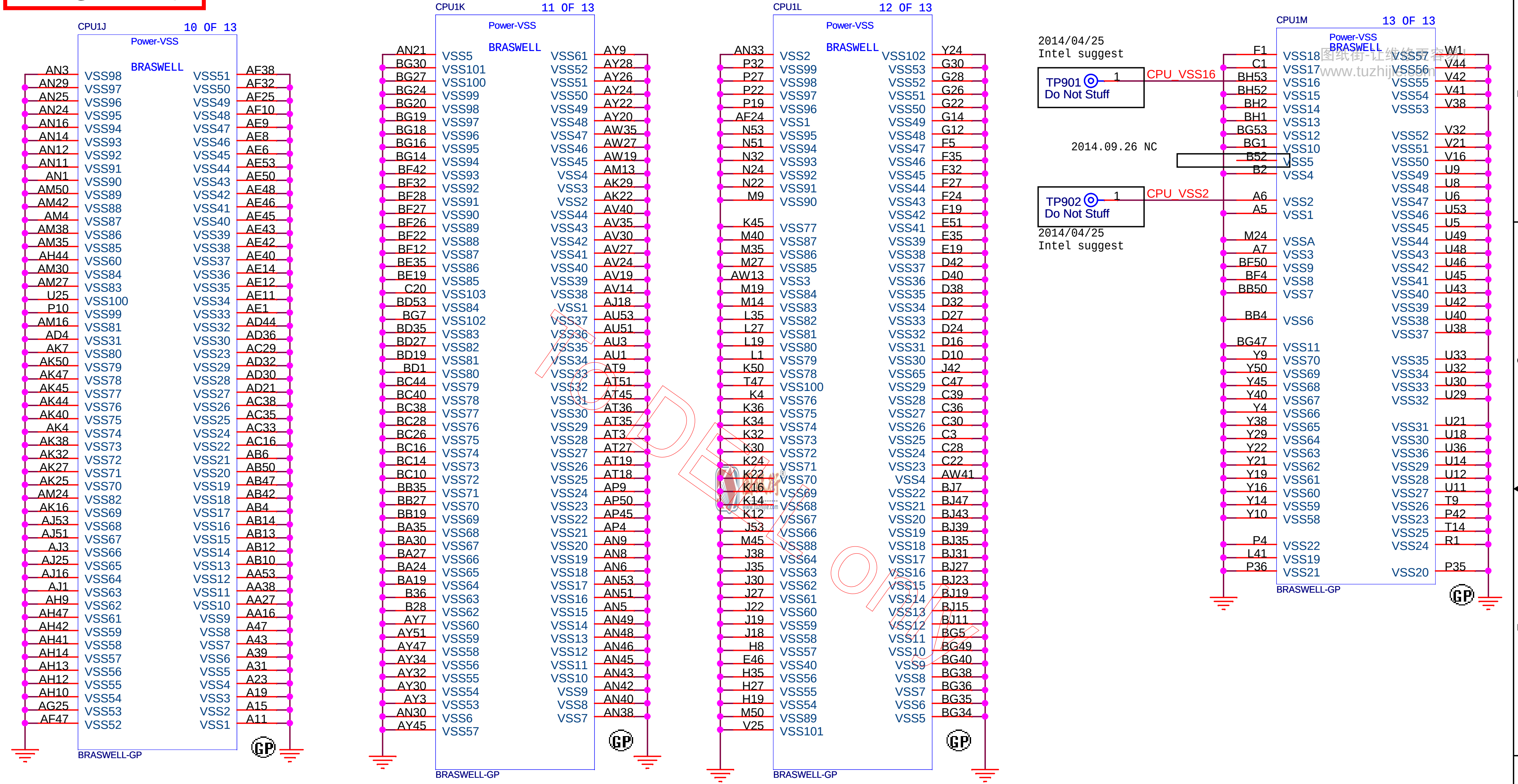
SSID = CPU



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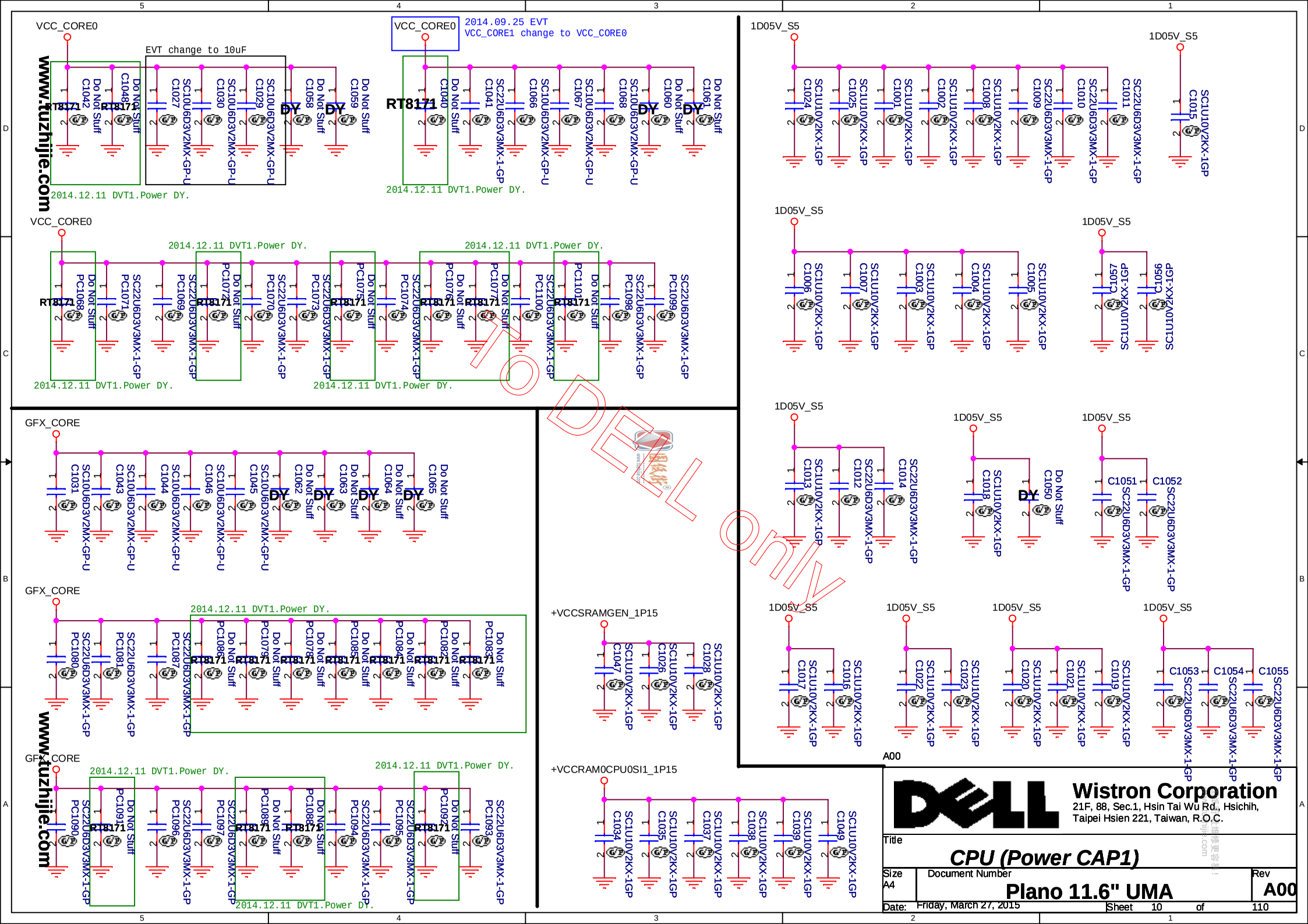
VCC_CORE0
EVT change to 10uF
2014.12.11 DVT1.Power DY.
2014.09.25 EVT
VCC_CORE1 change to VCC_CORE0
1D05V_S5
GFX_CORE
+VCCSRAMGEN_1P15
+VCCRAM0CPU0SI1_1P15
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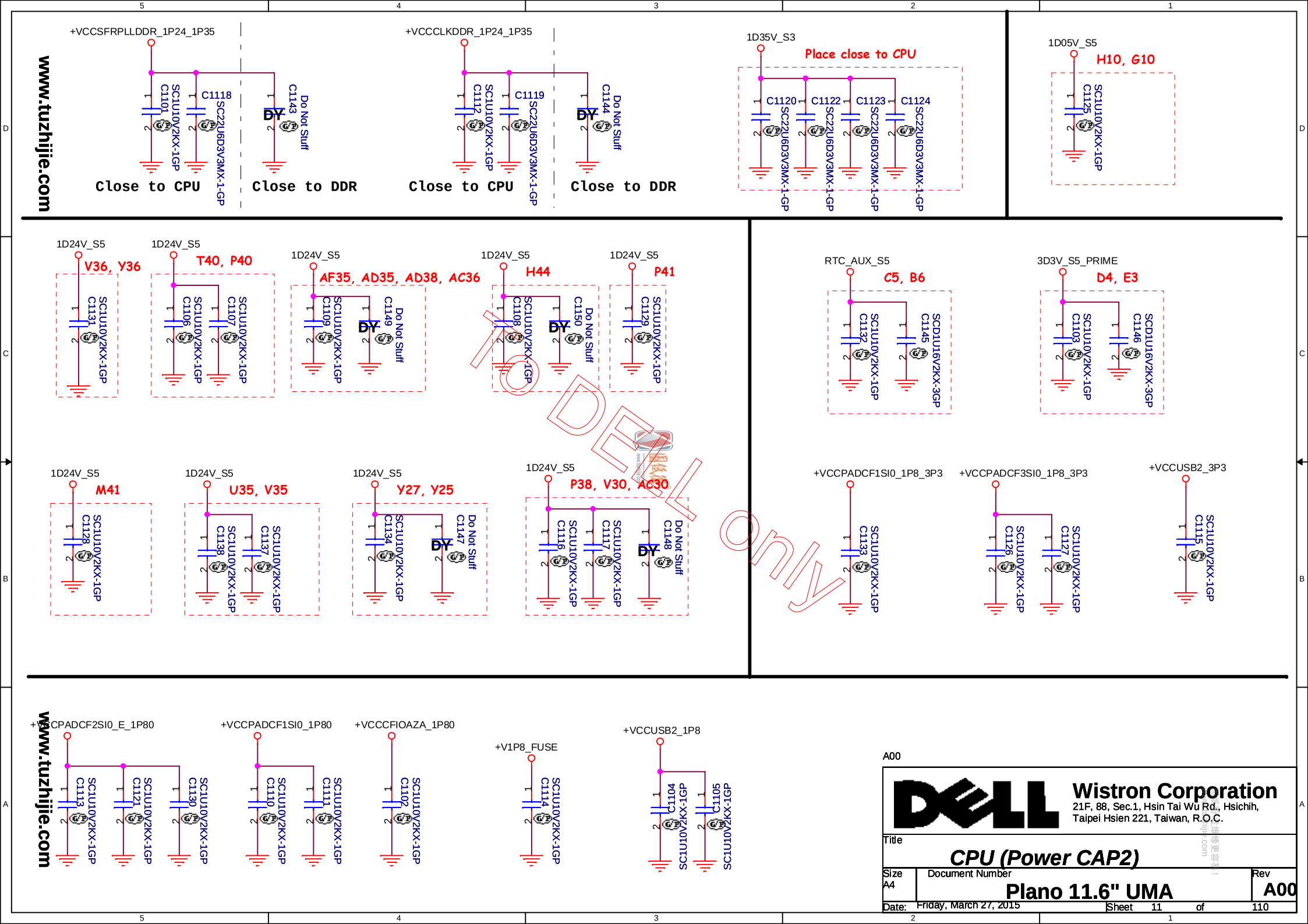
+VCCSFRPLLDDR_1P24_1P35
C1101 SC1U10V2KX-1GP
C1118 SC22U6D3V3MX-1-GP
C1143 Do Not Stuff
DY
Close to CPU
Close to DDR
+VCCCLKDDR_1P24_1P35
C1112 SC1U10V2KX-1GP
C1119 SC22U6D3V3MX-1-GP
C1144 Do Not Stuff
DY
Close to CPU
Close to DDR
1D35V_S3
Place close to CPU
C1120 SC22U6D3V3MX-1-GP
C1122 SC22U6D3V3MX-1-GP
C1123 SC22U6D3V3MX-1-GP
C1124 SC22U6D3V3MX-1-GP
1D05V_S5
H10, G10
C1125 SC1U10V2KX-1GP
1D24V_S5
V36, Y36
C1131 SC1U10V2KX-1GP
1D24V_S5
T40, P40
C1106 SC1U10V2KX-1GP
C1107 SC1U10V2KX-1GP
1D24V_S5
AF35, AD35, AD38, AC36
C1109 SC1U10V2KX-1GP
C1149 Do Not Stuff
DY
1D24V_S5
H44
C1108 SC1U10V2KX-1GP
C1150 Do Not Stuff
DY
1D24V_S5
P41
C1129 SC1U10V2KX-1GP
RTC_AUX_S5
C5, B6
C1132 SC1U10V2KX-1GP
C1145 SCD1U16V2KX-3GP
3D3V_S5_PRIME
D4, E3
C1103 SC1U10V2KX-1GP
C1146 SCD1U16V2KX-3GP
1D24V_S5
M41
C1128 SC1U10V2KX-1GP
1D24V_S5
U35, V35
C1138 SC1U10V2KX-1GP
C1137 SC1U10V2KX-1GP
1D24V_S5
Y27, Y25
C1134 SC1U10V2KX-1GP
C1147 Do Not Stuff
DY
1D24V_S5
P38, V30, AC30
C1116 SC1U10V2KX-1GP
C1117 SC1U10V2KX-1GP
C1148 Do Not Stuff
DY
+VCCPADCF1SI0_1P8_3P3
C1133 SC1U10V2KX-1GP
+VCCPADCF3SI0_1P8_3P3
C1126 SC1U10V2KX-1GP
C1127 SC1U10V2KX-1GP
+VCCUSB2_3P3
C1115 SC1U10V2KX-1GP
+VCCPADCF2SI0_E_1P80
C1113 SC1U10V2KX-1GP
C1121 SC1U10V2KX-1GP
C1130 SC1U10V2KX-1GP
+VCCPADCF1SI0_1P80
C1110 SC1U10V2KX-1GP
C1111 SC1U10V2KX-1GP
+VCCCFIOAZA_1P80
C1102 SC1U10V2KX-1GP
+V1P8_FUSE
C1114 SC1U10V2KX-1GP
+VCCUSB2_1P8
C1104 SC1U10V2KX-1GP
C1105 SC1U10V2KX-1GP
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SSID = MEMORY

P30

DDR3-204P-108-GP-U
62.10017.X41
2nd = 62.10024.M31
3rd = 62.10017.131

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

TS# DIMM0_1 — DY R1201 Do Not Stuff — 3D3V_S0

For Intel Recommend Close to DIMM(Braswell)

DDR_VREF_S3 — R1212 Do Not Stuff — VREF_DQ — C1213 SCD1U16V2KX-GP
1D35V_S3 — R1202 Do Not Stuff — R1204 Do Not Stuff
reserve for verification

For Intel Recommend Close to DIMM(Braswell)

DDR_VREF_S3 — R1213 Do Not Stuff — VREF_CA — C1201 SCD1U16V2KX-GP
1D35V_S3 — R1205 Do Not Stuff — R1206 Do Not Stuff
reserve for verification

Layout Note:
Place these Caps near SO-DIMMA.

SODIMM A DECOUPLING

1D35V_S3 — C1203 C1204 C1205 C1206 C1207 C1221 C1222 C1223 TC1201 (Do Not Stuff) — SCD1U16V2KX-GP
2015.01.26 DVT2 RF add 0.1uF

C1209 C1210 C1211 C1212 — SCD1U10V2KX-GP

0D675V_S0 — Place these caps close to VTT1 and VTT2.
C1214 C1215 C1216 C1217 C1219 C1220 — SCD1U10V2KX-GP

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SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

All the straps are sampled on the rising edge of the PMC_RSMRST_N signal (check list)

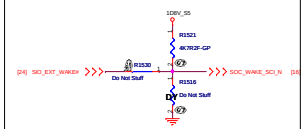
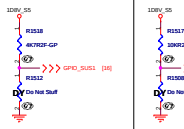
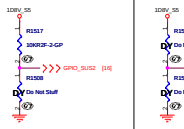
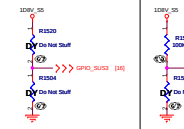
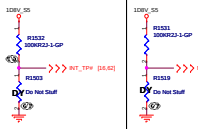
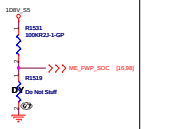
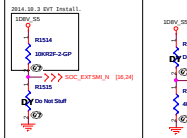
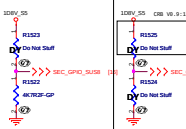
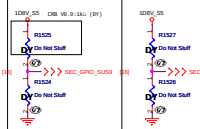
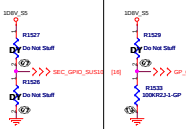
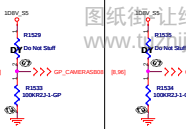
Description	DDI0_Detected	DDI1_Detected	A16 Swap Override	DSI Display Detected	Boot BIOS Strap BBS	Flash Descriptor Security Override	DFX Boot Halt Strap & VISA Early POSM Debug Enable	DFX Sus Debug Strap	ICLK, USB2, DDI SFR Supply Select	ICLK SFR Bypass	POSM Select	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC bypass
GPIO	GPIO_SUS0	GPIO_SUS1	GPIO_SUS2	GPIO_SUS3	GPIO_SUS4	GPIO_SUS5	GPIO_SUS6	GPIO_SUS7	SEC_GPIO_SUS8	SEC_GPIO_SUS9	SEC_GPIO_SUS10	GP_CAMERASB08	GP_CAMERASB09	GP_CAMERASB11
Schematic														
High	DDI0 Detect	DDI1 Detect	Normal Operation	DSI Detect	Boot from SPI	Weak internal pull-up Normal Operation	Normal	Weak internal pull-up Normal	1.35V	Weak internal pull-up Bypass with 1.05V	PMC	Bypass	Bypass	Bypass
Low	Disable	Disable	Change Boot Loader address (A16 Override)	Disable Weak internal pull-down	Boot from LPC	Override	Halt boot enable	Sus Debug enable	1.25V	No bypass	Fuse controller Weak internal pull-down	No bypass	No bypass	No bypass

Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap overdrive	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

Table 29. Straps (Sheet 2 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, iCLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass

CHV Straps [CRB] -- strap detect @ RSMRST# assertion

Purpose	CHV Pin Name (refer CHV symbol PIN)	PU/PD (internal - Week)	Options	Default State on board?
DDI0 Detected	GPIO_SUS0	PD	1 - DDI0 Detect, 0 - Disable	High
DDI1 Detected	GPIO_SUS1	PD	1 - DDI1 Detect, 0 - Disable	High
A16 swap override	GPIO_SUS2	PU	1- Default, 0- A16 override	High
DSI Display Detected	GPIO_SUS3	PD	1 - DSI detect, 0 - Disable	Low
Boot BIOS Strap BBS	GPIO_SUS4	PU	1 - Boot from SPI, 0 - Boot from LPC	High
Flash Descriptor Security Override	GPIO_SUS5	PU	1- Security enabled, 0 - Security disabled	High
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	PU	1 - normal, 0 - Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	1- Normal, 0 - Sus Debug enable	High
ICLK, USB2, DDI SFR Supply Select-	SEC_GPIO_SUS8	PU	1 - 1.35V, 0 - 1.25V	Low
ICLK SFR Bypass	SEC_GPIO_SUS9	PD	1 - Bypass with 1.05V, 0 - No Bypass	Low
POSM Select	SEC_GPIO_SUS10	PD	1 - PMC, 0 - Fuse controller	Don't care, if GPIO_SUS6 is pulled high.
ICLK Xtal OSC Bypass	GP_CAMERASB08	PD	1 - Bypass, 0 - No bypass	Low
CCU SUS RO Bypass	GP_CAMERASB09	PD	1 - Bypass, 0 - No bypass	Low
RTC OSC Bypass	GP_CAMERASB11	PD	1 - Bypass, 0 - No bypass	Low

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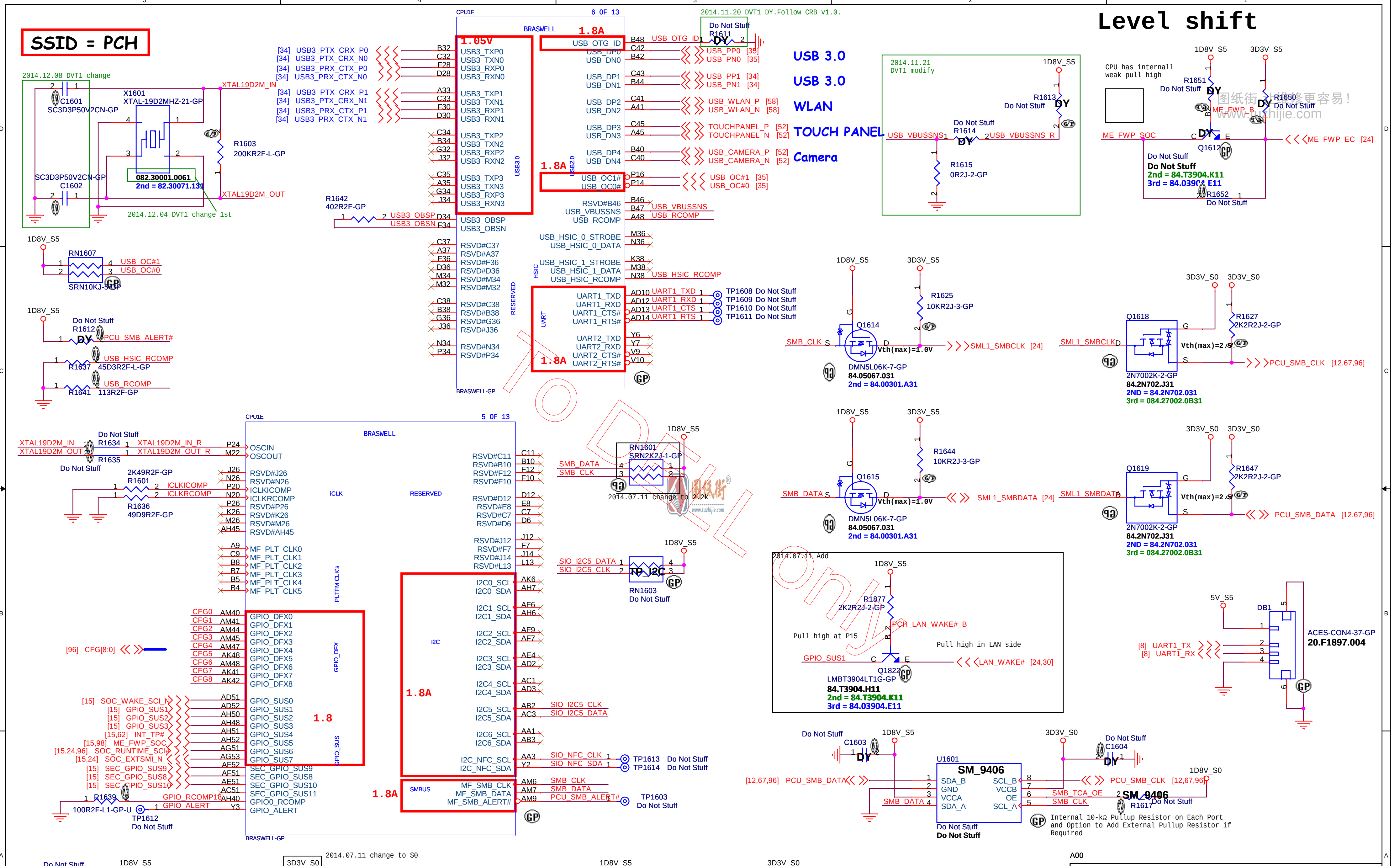
CPU(STRAP)

Size: A1 | Document Number: Plano 11.6" UMA | Rev: A00

Date: Wednesday, November 11, 2015 | Sheet 15 of 110



SSID = PCH
Level shift
CPU1F
6 OF 13
BRASWELL
1.05V
1.8A
USB3_TXP0
USB3_TXN0
USB3_RXP0
USB3_RXN0
USB3_TXP1
USB3_TXN1
USB3_RXP1
USB3_RXN1
USB3_TXP2
USB3_TXN2
USB3_RXP2
USB3_RXN2
USB3_TXP3
USB3_TXN3
USB3_RXP3
USB3_RXN3
USB3_OBSP
USB3_OBSN
USB_OTG_ID
USB_DP0
USB_DN0
USB_DP1
USB_DN1
USB_DP2
USB_DN2
USB_DP3
USB_DN3
USB_DP4
USB_DN4
USB_OC1#
USB_OC0#
USB_VBUSSNS
USB_RCOMP
USB_HSIC_0_STROBE
USB_HSIC_0_DATA
USB_HSIC_1_STROBE
USB_HSIC_1_DATA
USB_HSIC_RCOMP
UART1_TXD
UART1_RXD
UART1_CTS#
UART1_RTS#
UART2_TXD
UART2_RXD
UART2_CTS#
UART2_RTS#
BRASWELL-GP
USB 3.0
USB 3.0
WLAN
TOUCH PANEL
Camera
2014.11.20 DVT1 DY.Follow CRB v1.0.
2014.11.21 DVT1 modify
2014.12.08 DVT1 change
2014.12.04 DVT1 change 1st
X1601
XTAL-19D2MHZ-21-GP
082.30001.0061
2nd = 82.30071.131
R1603
200KR2F-L-GP
XTAL19D2M_IN
XTAL19D2M_OUT
SC3D3P50V2CN-GP
C1601
C1602
R1642
402R2F-GP
RN1607
SRN10KJ-5-GP
R1612
R1637
45D3R2F-L-GP
R1641
113R2F-GP
TP1608 Do Not Stuff
TP1609 Do Not Stuff
TP1610 Do Not Stuff
TP1611 Do Not Stuff
CPU has internall weak pull high
R1651
R1650
R1613
R1614
R1615
0R2J-2-GP
Q1612
2nd = 84.T3904.K11
3rd = 84.03904.E11
R1652
ME_FWP_SOC
ME_FWP_EC
Q1614
R1625
10KR2J-3-GP
DMN5L06K-7-GP
84.05067.031
2nd = 84.00301.A31
Vth(max)=1.0V
SMB_CLK
SML1_SMBCLK
PCU_SMB_CLK
Q1618
R1627
2K2R2J-2-GP
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 084.27002.0B31
Q1615
R1644
SMB_DATA
SML1_SMBDATA
PCU_SMB_DATA
Q1619
R1647
CPU1E
5 OF 13
OSCIN
OSCOUT
R1634
R1635
R1601
2K49R2F-GP
R1636
49D9R2F-GP
ICLKICOMP
ICLKRCOMP
MF_PLT_CLK0
MF_PLT_CLK1
MF_PLT_CLK2
MF_PLT_CLK3
MF_PLT_CLK4
MF_PLT_CLK5
GPIO_DFX0
GPIO_DFX1
GPIO_DFX2
GPIO_DFX3
GPIO_DFX4
GPIO_DFX5
GPIO_DFX6
GPIO_DFX7
GPIO_DFX8
CFG[8:0]
GPIO_SUS0
GPIO_SUS1
GPIO_SUS2
GPIO_SUS3
GPIO_SUS4
GPIO_SUS5
GPIO_SUS6
GPIO_SUS7
SEC_GPIO_SUS8
SEC_GPIO_SUS9
SEC_GPIO_SUS10
SEC_GPIO_SUS11
GPIO0_RCOMP
GPIO_ALERT
R1639
100R2F-L1-GP-U
TP1612
I2C0_SCL
I2C0_SDA
I2C1_SCL
I2C1_SDA
I2C2_SCL
I2C2_SDA
I2C3_SCL
I2C3_SDA
I2C4_SCL
I2C4_SDA
I2C5_SCL
I2C5_SDA
I2C6_SCL
I2C6_SDA
I2C_NFC_SCL
I2C_NFC_SDA
MF_SMB_CLK
MF_SMB_DATA
MF_SMB_ALERT#
SIO_I2C5_CLK
SIO_I2C5_DATA
SIO_NFC_CLK
SIO_NFC_SDA
TP1613 Do Not Stuff
TP1614 Do Not Stuff
TP1603 Do Not Stuff
RN1601
SRN2K2J-1-GP
2014.07.11 change to 2.2k
RN1603
TP_I2C
2014.07.11 Add
R1877
2K2R2J-2-GP
PCH_LAN_WAKE#_B
Pull high at P15
Pull high in LAN side
GPIO_SUS1
LAN_WAKE#
Q1822
LMBT3904LT1G-GP
84.T3904.H11
2nd = 84.T3904.K11
3rd = 84.03904.E11
DB1
ACES-CON4-37-GP
20.F1897.004
UART1_TX
UART1_RX
U1601
SM_9406
C1603
C1604
R1617
Internal 10-kΩ Pullup Resistor on Each Port and Option to Add External Pullup Resistor if Required
U1605
SM_9406
C1606
C1608
R1622
2014.07.11 change to S0
U1602
TP_I2C
C1605
C1607
R1619
TP_I2C
TP_I2C_DATA
TP_I2C_CLK
Do Not Stuff

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Title: CPU (USB/LPC/GPIO)

Size: A3 | Document Number: Plano 11.6" UMA | Rev: A00

Date: Friday, April 24, 2015 | Sheet 16 of 110

Blanking

A00

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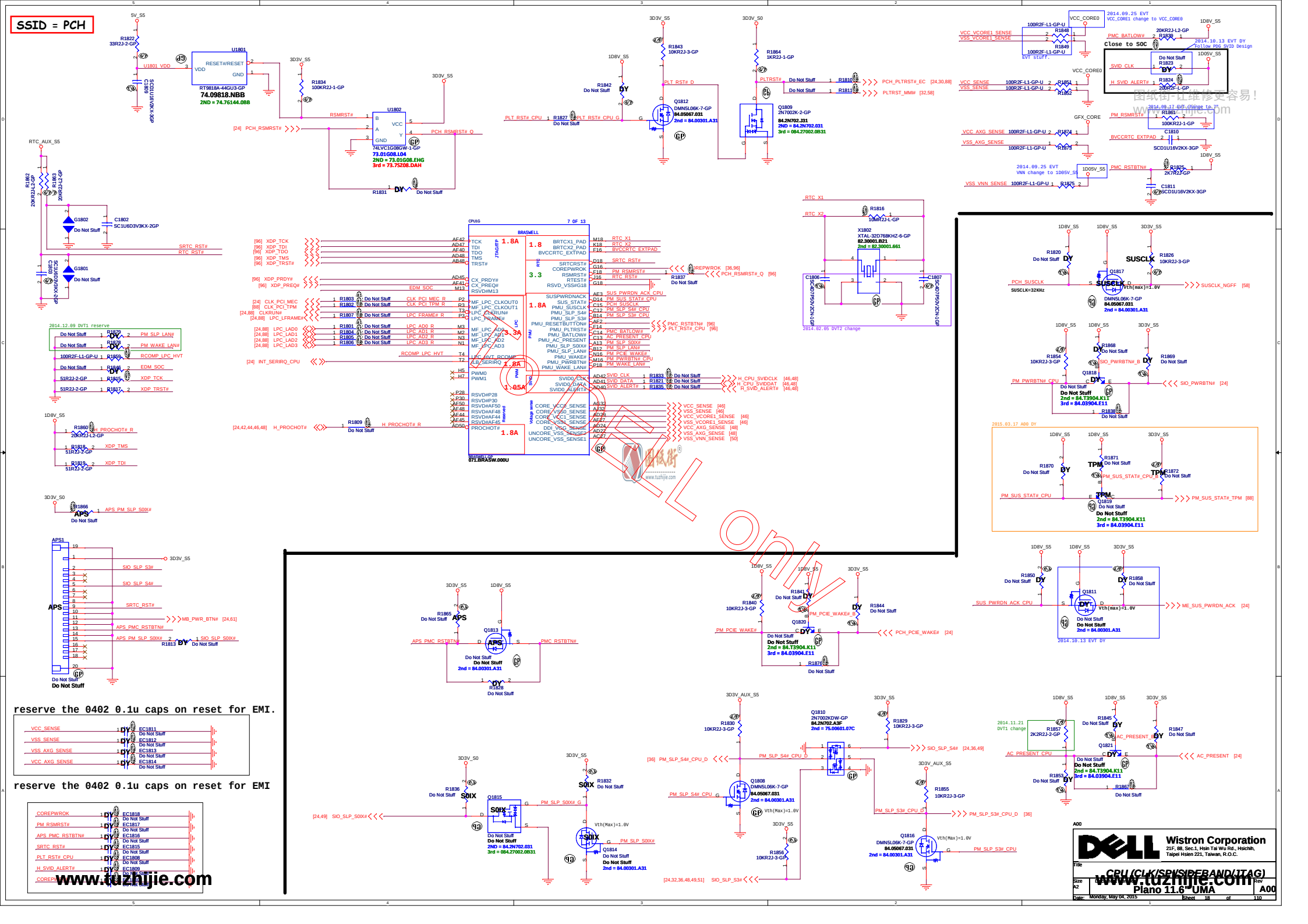
Title
CPU (Reserved)

Size	Document Number	Rev
A4	Plano 11.6" UMA	A00

Date: Friday, March 27, 2015 Sheet 17 of 110

SSID = PCH


U1801
RT9818A-44GU3-GP
74.09818.NBB
2ND = 74.76144.0BB
U1802
74LVC1G08GW-1-GP
73.01G08.L04
2ND = 73.01G08.EHG
3rd = 73.7SZ08.DAH
Q1812
DMN5L06K-7-GP
84.05067.031
2nd = 84.00301.A31
Q1809
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 084.27002.0B31
CPU8G
BRASWELL
7 OF 13
071.BRASW.000U
1.8A
1.8
3.3
1.8A
3.3A
1.8A
1.05A
1.8A
Do Not Stuff
DY
GP
2014.09.25 EVT
VCC_CORE1 change to VCC_CORE0
Close to SOC
2014.10.13 EVT DY
follow PDG SVID Design
2014.09.17 EVT change to
2014.09.25 EVT
VNN change to 1D05V_S5
2014.12.09 DVT1 reserve
2014.02.05 DVT2 change
2015.03.17 A00 DY
2014.10.13 EVT DY
2014.11.21
DVT1 change
reserve the 0402 0.1u caps on reset for EMI.
reserve the 0402 0.1u caps on reset for EMI
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2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU (CLK/SPI/SIDEBAND/JTAG)
Plano 11.6"UMA
A00
Monday, May 04, 2015
Sheet 18 of 110

SSID = PCH

CPU1D

4 OF 13

BRASWELL

1.05V

CARD

[32] PCIE_PTX_CARDRX_P1_C
[32] PCIE_PTX_CARDRX_N1_C
[32] PCIE_PRX_CARDTX_P1
[32] PCIE_PRX_CARDTX_N1

C1913 2 1 SCD1U16V2KX-3GP PCIE_PTX_CARDRX_P1
C1914 2 1 SCD1U16V2KX-3GP PCIE_PTX_CARDRX_N1

WLAN

[58] PCIE_PTX_WLANRX_P2_R
[58] PCIE_PTX_WLANRX_N2_R
[58] PCIE_PRX_WLANTX_P2
[58] PCIE_PRX_WLANTX_N2

C1915 2 1 SCD1U16V2KX-3GP PCIE_PTX_WLANRX_P2
C1916 2 1 SCD1U16V2KX-3GP PCIE_PTX_WLANRX_N2

LOM

[30] PCIE_PTX_LANRX_P3_C
[30] PCIE_PTX_LANRX_N3_C
[30] PCIE_PRX_LANTX_P3
[30] PCIE_PRX_LANTX_N3

C1911 2 1 SCD1U16V2KX-3GP PCIE_PTX_LANRX_P3
C1912 2 1 SCD1U16V2KX-3GP PCIE_PTX_LANRX_N3

C24 PCIE_TXP0
B24 PCIE_TXN0
G20 PCIE_RXP0
J20 PCIE_RXN0
A25 PCIE_TXP1
C25 PCIE_TXN1
D20 PCIE_RXP1
F20 PCIE_RXN1
B26 PCIE_TXP2
C26 PCIE_TXN2
D22 PCIE_RXP2
F22 PCIE_RXN2
A27 PCIE_TXP3
C27 PCIE_TXN3
G24 PCIE_RXP3
J24 PCIE_RXN3

PCIe

SATA_TXP0 C31 SATA_PTX_HDDRX_P0 [56]
SATA_TXN0 B30 SATA_PTX_HDDRX_N0 [56]
SATA_RXP0 N28 SATA_PRX_HDDTX_P0 [56]
SATA_RXN0 M28 SATA_PRX_HDDTX_N0 [56]
SATA_TXP1 C29 SATA_PTX_SSDRX_P1 [59]
SATA_TXN1 A29 SATA_PTX_SSDRX_N1 [59]
SATA_RXP1 J28 SATA_PRX_SSDTX_P1 [59]
SATA_RXN1 K28 SATA_PRX_SSDTX_N1 [59]

HDD

SSD

1.8S

SATA

SATA_LED# AH3 SATA_LED# [61]
SATA_GP0 AH2 HDD_FALL_INT_C
SATA_GP1 AG3 TOUCH_SCREEN_PD [52]
SATA_GP2 AG1 HDD_DEVSLP [56]
SATA_GP3 AF3 NGFF_DEVSLP1 [59]

SATA_OBSP N30 SATA_OBSP 2 R1931 1 402R2F-GP
SATA_OBSN M30 SATA_OBSN

1.8A

FST_SPI_CLK W3 PCH_SPI_CLK [25]
FST_SPI_CS0# V4 PCH_SPI_CS0# [25]
FST_SPI_CS1# V6
FST_SPI_CS2# V7 3.3V_TS_EN [52]

FAST SPI

FST_SPI_D0 V2 PCH_SPI_SI [25]
FST_SPI_D1 V3 PCH_SPI_SO [25]
FST_SPI_D2 U1 PCH_SPI_DQ2 [25]
FST_SPI_D3 U3 PCH_SPI_DQ3 [25]

1.5S

MF_HDA_RST# AE13 HDA_RST#
MF_HDA_SDI1 AD6 HDA_SDIN1
MF_HDA_CLK AD9 HDA_BITCLK
MF_HDA_SDI0 AD7 HDA_SDIN0 [27]
MF_HDA_SYNC AE12 HDA_SYNC
MF_HDA_SDO AE14 HDA_SDO
MF_HDA_DOCKEN# AB9
MF_HDA_DOCKRST# AB7

AUDIO

SPKR H4 HDA_SPKR [27]

GP_SSP_2_CLK AK9
GP_SSP_2_FS AK10
GP_SSP_2_TXD AK12
GP_SSP_2_RXD AK13

1.8

SPI

SPI1_CLK V14
SPI1_CS0# Y13
SPI1_CS1# Y12
SPI1_MISO V13
SPI1_MOSI V12

BRASWELL-GP

1.8A

PCIE_CLKREQ0# AM10
PCIE_CLKREQ1# AM12
PCIE_CLKREQ2# AK14
PCIE_CLKREQ3# AM14

For FFS INT2 SMI pin

[67] FFS_PCH_INT2
Devise side is OD [32] CLK_PCIE_CARD_REQ1#
[58] CLK_PCIE_WLAN_REQ2#
Devise side is OD [30] CLK_PCIE_LOM_REQ3#

2015.03.18 DVT2 add.

[32] CLK_PCIE_CARD_P1_C
[32] CLK_PCIE_CARD_N1_C
[58] CLK_PCIE_WLAN_P2_C
[58] CLK_PCIE_WLAN_N2_C
[30] CLK_PCIE_LOM_P3_C
[30] CLK_PCIE_LOM_N3_C

R1933 1 0R2J-2-GP CLK_PCIE_CARD_P1
R1934 1 0R2J-2-GP CLK_PCIE_CARD_N1
R1935 1 0R2J-2-GP CLK_PCIE_WLAN_P2
R1936 1 0R2J-2-GP CLK_PCIE_WLAN_N2
R1937 1 0R2J-2-GP CLK_PCIE_LOM_P3
R1938 1 0R2J-2-GP CLK_PCIE_LOM_N3

CLK_DIFF_P_0 A21
CLK_DIFF_N_0 C21
CLK_DIFF_P_1 C19
CLK_DIFF_N_1 B20
CLK_DIFF_P_2 C18
CLK_DIFF_N_2 B18
CLK_DIFF_P_3 C17
CLK_DIFF_N_3 A17
CLK_DIFF_P_4 C16
CLK_DIFF_N_4 B16

402R2F-GP
R1930 1 2 PCIE_OBSP D26
PCIE_OBSN F26

PCIE_OBSP
PCIE_OBSN

1D8V_S0

RN1902
SRN10KJ-5-GP
1 2 4 3
CLK_PCIE_LOM_REQ3#
CLK_PCIE_CARD_REQ1#

1D8V_S5

DY
R1940 Do Not Stuff
R1939 10KR2J-3-GP
CLK_PCIE_WLAN_REQ2#

1D8V_S0 1D8V_S0

R1907 10KR2J-3-GP
R1908 2K2R2J-2-GP
FFS_PCH_INT_B

reserve pull high in device side.
device is push pull

HDD_FALL_INT_C
Q1901 C B E
LMBT3904LT1G-GP
84.T3904.H11
2nd = 84.T3904.K11
3rd = 84.03904.E11

FFS_PCH_INT1 [67]
FFS INT1

For FFS INT1 IRQ pin

HDA_RST# R1928 1 Do Not Stuff HDA_CODEC_RST# [27]
HDA_BITCLK R1927 1 Do Not Stuff HDA_CODEC_BITCLK [27]
HDA_SYNC R1926 1 Do Not Stuff HDA_CODEC_SYNC [27]
HDA_SDO R1929 1 Do Not Stuff HDA_CODEC_SDOUT [27]
HDA_SDIN1 R1932 1 Do Not Stuff

DY

2014.12.05 DVT1 reserve

HDA_RST#
DY C1910 Do Not Stuff

A00

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SATA/PCIE/IHDA)

Size: A4 | Document Number: Plano 11.6" UMA | Rev: A00

Date: Wednesday, April 22, 2015 | Sheet 19 of 110

SSID = PCH

Blanking

A00

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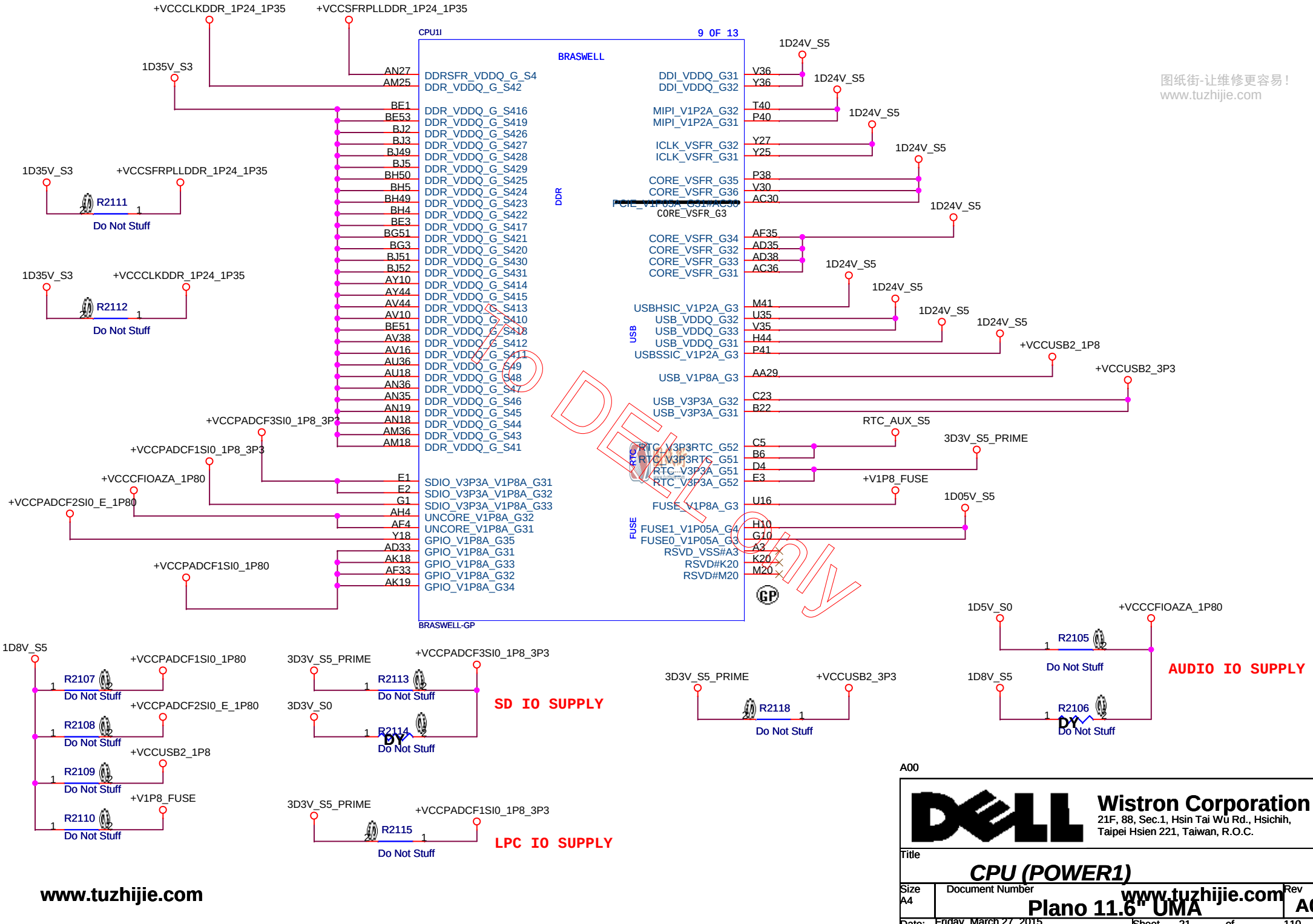
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	Plano 11.6" UMA	A00

Date: Friday, March 27, 2015 Sheet 20 of 110



A00

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (POWER1)***

Size	Document Number	Rev
A4	Plano 11.6" UMA	A00

Date: Friday, March 27, 2015 Sheet 21 of 110

Blanking

A00

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Plano 11.6" UMA

Size	Document Number	Rev
A4		A00

Date: Thursday, April 09, 2015 Sheet 22 of 110

SSID = PCH

Blanking

A00

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size	Document Number	Rev
A4	Plano 11.6" UMA	A00

Date: Friday, March 27, 2015 Sheet 23 of 110

SSID = KBC

0 = Reset JTAG I/F
1 = Disable

Need to runing change to 071.05085.0A03(5085 with X01 code)

To CPU

Place close to Pin58

Level shift

JTAG

R2463 pull DN, Enable JTAG debug mode

VCCA < VCCB

Plano 11.6" UMA
BOARD_ID

Res. Value	Cap. Value	REV
4700pF	1k ohm	EV BD
	2k ohm	EVT
	4.3k ohm	DVT1
	8.2k ohm	DVT2
	33k ohm	A00

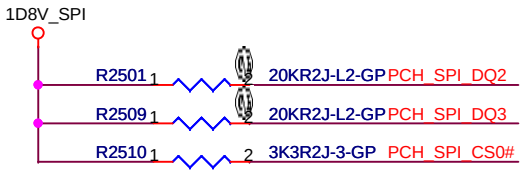
LIMITS				External Circuit Components	
MIN count	MAX count	Range	Band Gap	C (pF)	R (K)
Avg-20%	Avg+10%	max-min	between RC values	10%	5%
80	112	32		4700	1
160	222	62	48	4700	2
344	474	130	122	4700	4.3
659	907	248	185	4700	8.2
2617	3600	983	1710	4700	33
4862	6686	1824	1262	4700	62
8866	12687	3721	3180	4700	130
17384	23904	6520	3817	4700	240

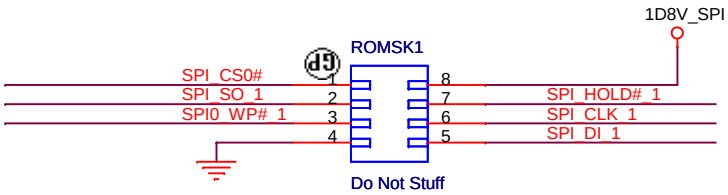
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: EC_MEC5085
Size: A2 | Document Number: Plano 11.6" UMA | Rev: A00
Date: Wednesday, April 22, 2015 | Sheet 24 of 110

SSID = Flash.ROM

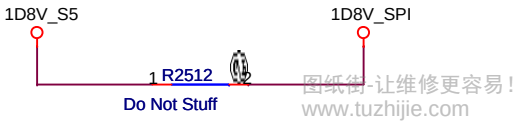
SPI ROM Equal length need to less than 500mil

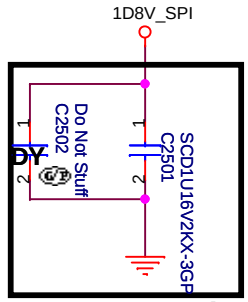




Do Not Stuff

Debug config need to stuff socket and SOIC(072.25128.0E01)

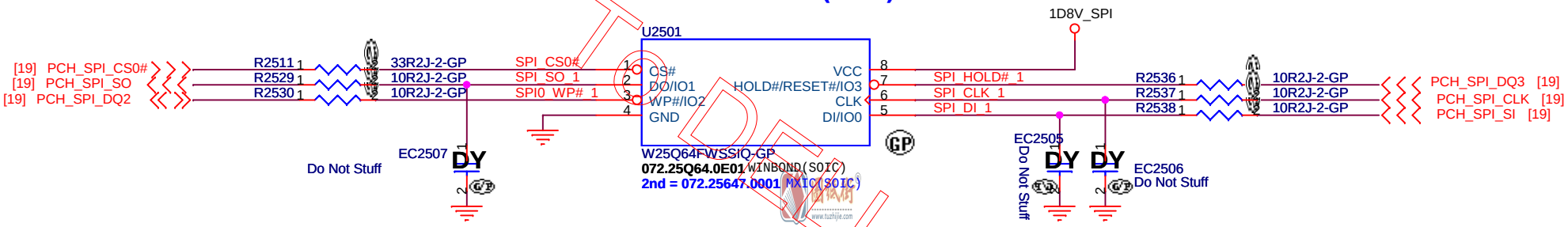




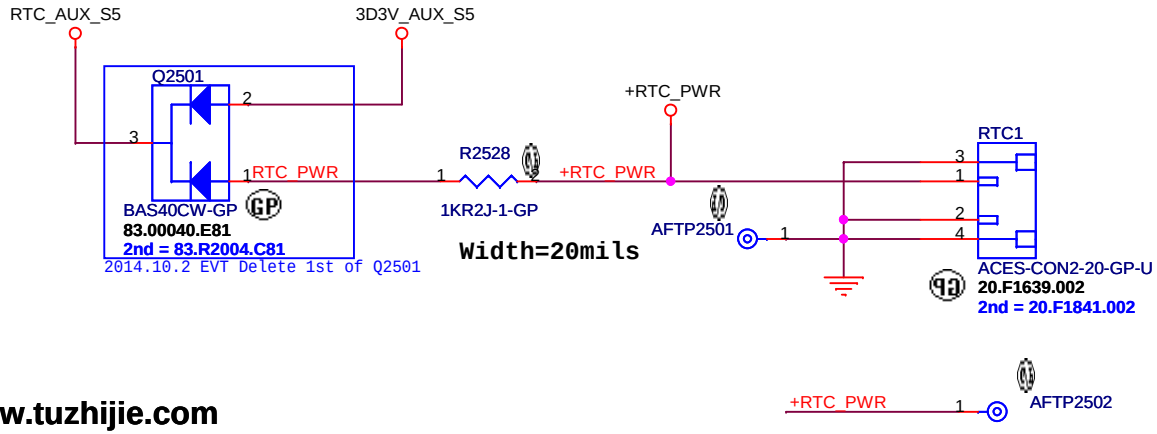
Layout Note: Close to U2501 Pin 8

SYSTEM SPI ROM

SPI Flash ROM(16M) for PCH



SSID = RTC



A00

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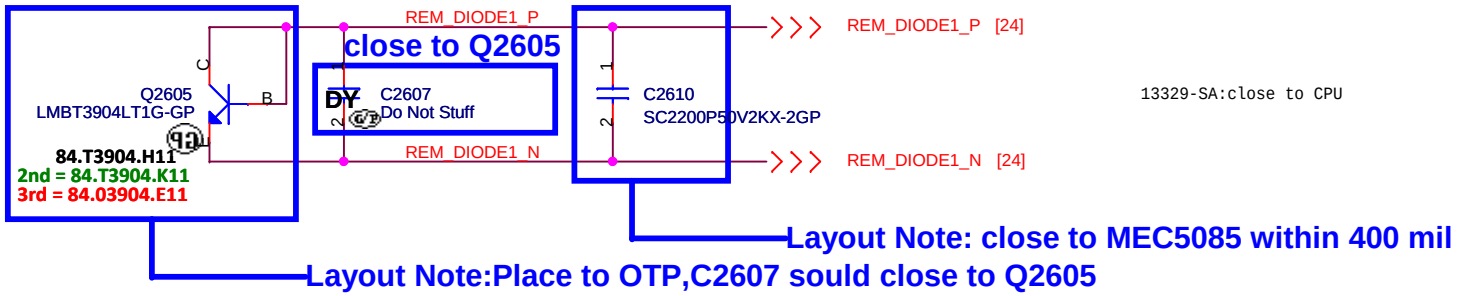
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Flash/RTC**

Size	Document Number	Rev
A4	Plano 11.6" UMA	A00

Date: Wednesday, April 22, 2015 Sheet 25 of 110

SSID = Thermal

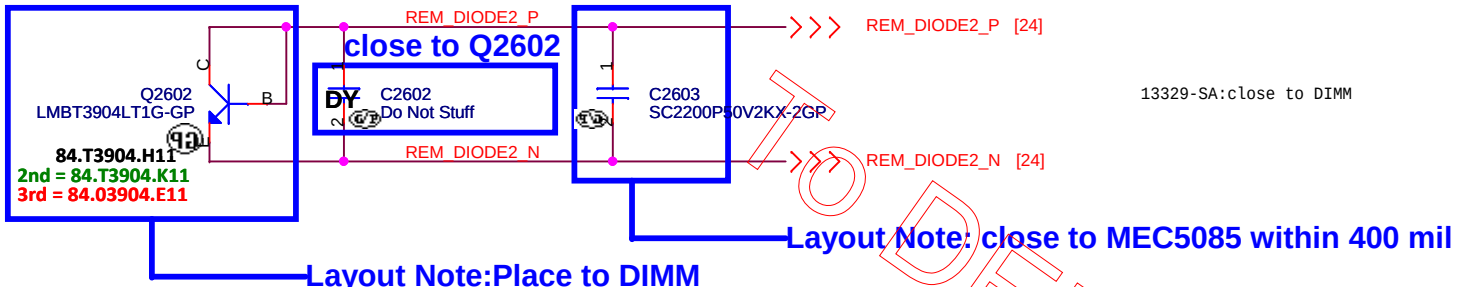


13329-SA:close to CPU

Layout Note: close to MEC5085 within 400 mil

Layout Note:Place to OTP,C2607 sould close to Q2605

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

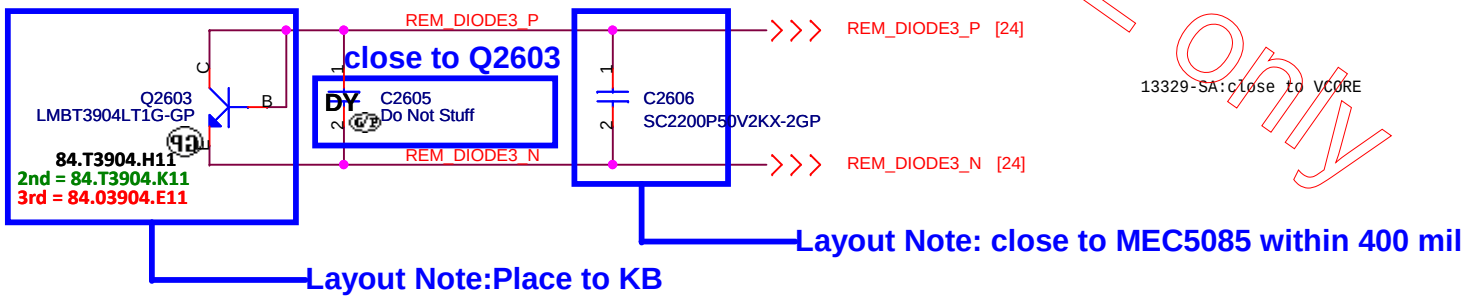


13329-SA:close to DIMM

Layout Note: close to MEC5085 within 400 mil

Layout Note:Place to DIMM

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

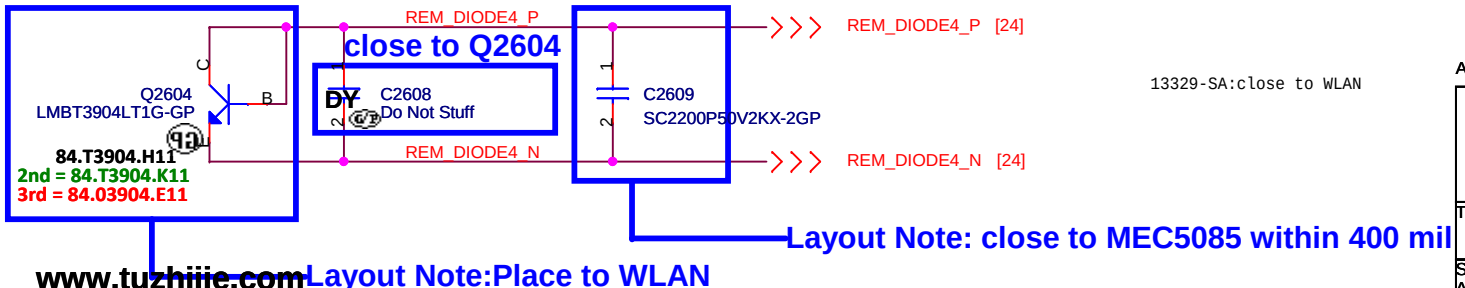


13329-SA:close to VCORE

Layout Note: close to MEC5085 within 400 mil

Layout Note:Place to KB

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.



13329-SA:close to WLAN

Layout Note: close to MEC5085 within 400 mil

Layout Note:Place to WLAN

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Channel 1 is for CPU
Channel 2 is for DIMM
Channel 3 is for KB Skin
Channel 4 is for WLAN

A00

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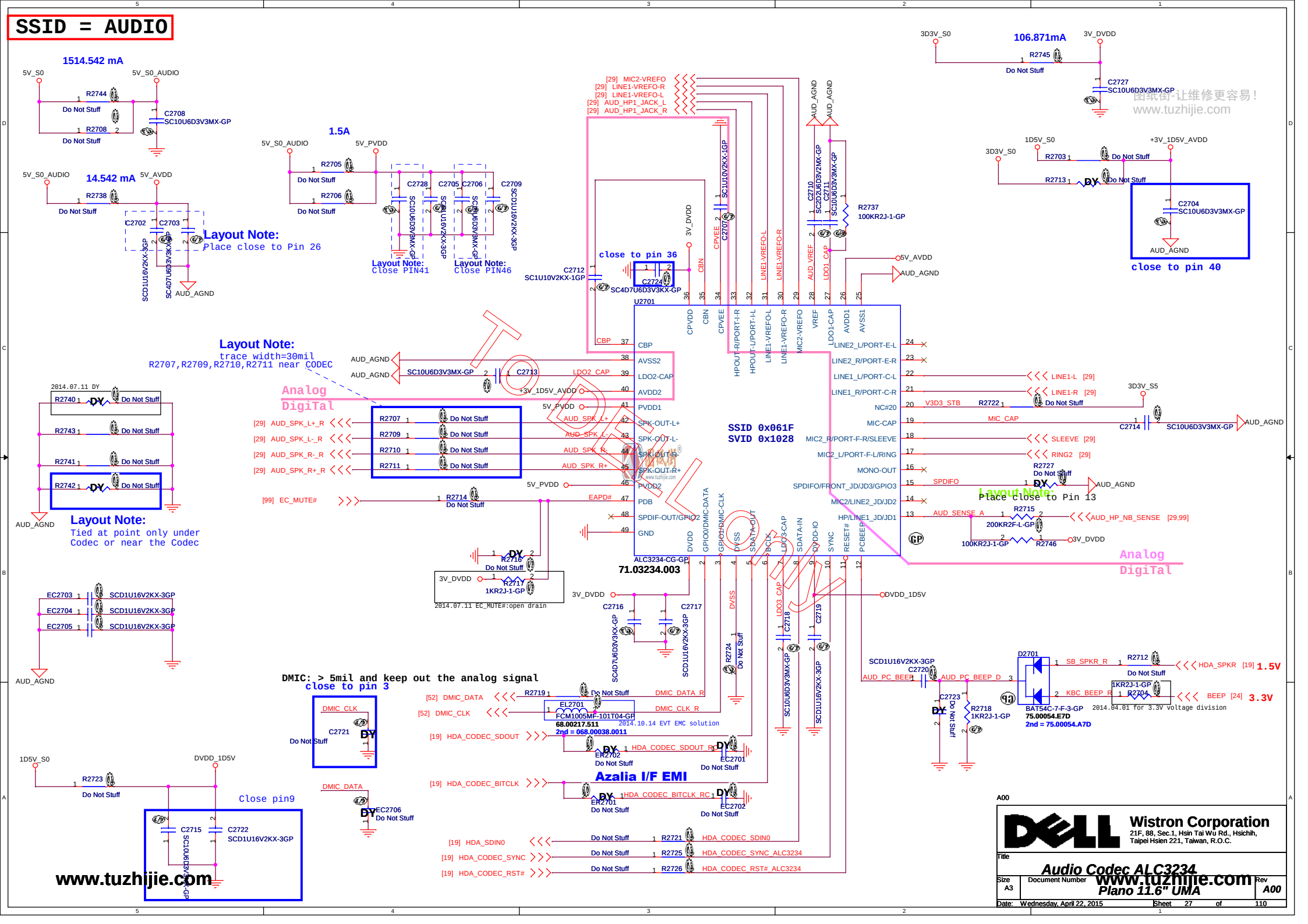
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal

Size	Document Number	Rev
A4	Plano 11.6" UMA	A00

Date: Wednesday, April 22, 2015 Sheet 26 of 110

SSID = AUDIO



(Blanking)

A00

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Title: ***Reserved***

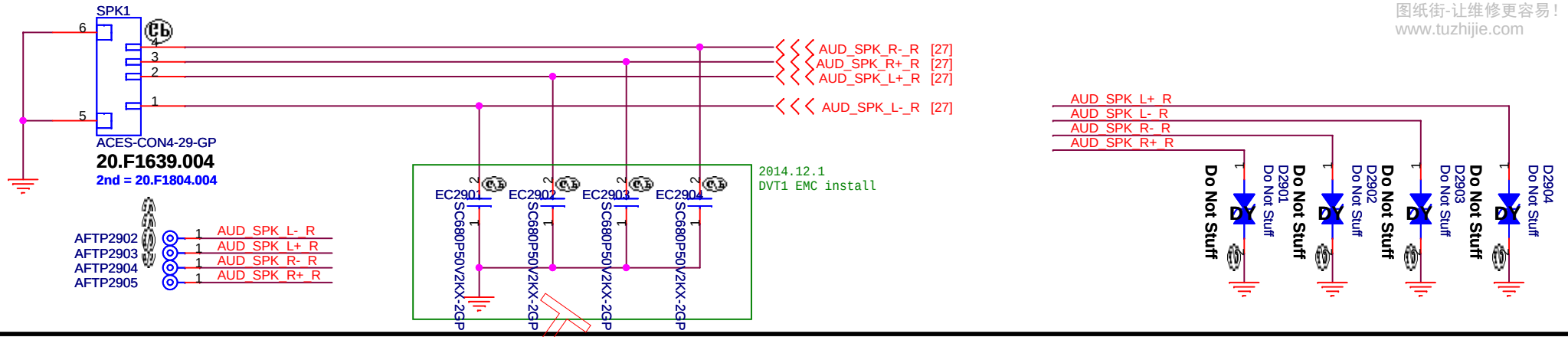
Size	Document Number	Rev
A	***Plano 11.6" UMA***	A00

Date: Friday, March 27, 2015 Sheet 28 of 110

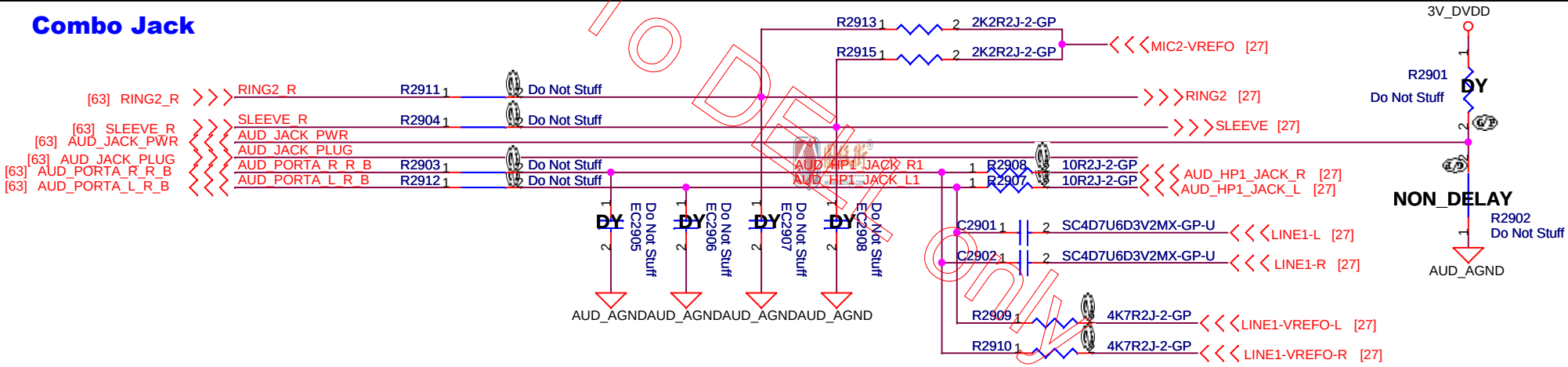
SSID = AUDIO

Speaker

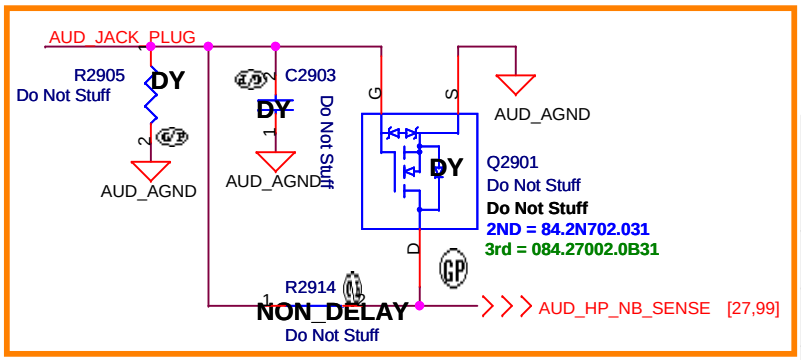
2W/ch

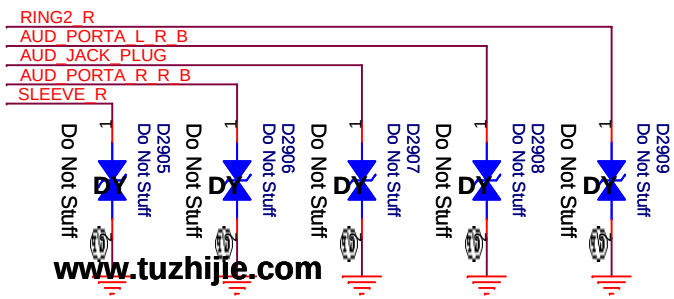


Combo Jack



Delay circuit





A00

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/HPMIC CONN

Size	Document Number	Rev
A4	Plano 11.6" UMA	A00

Date: Wednesday, April 22, 2015 Sheet 29 of 110

For RTL8151GD

* Place C3001 and C3002 close to each AVDD33 pin-- 11, 32

* For surge improvement, place C3003 and C3004 close to each AVDD33 pin-- 11, 32. (optional)

For RTL8151GD

* Place C3008 ~ C3011 close to each VDD10 pin-- 3, 8, 22, 30

2014.07.11 avoid leakage

For RTL8151GD

* Place C3012 and C3013 close to each VDD10 pin-- 22

Active low

O/D

2014.06.25 change to 15pF,follow Cedar

+/- 20 ppm

Loading 12pF

RTL8151GD-CG-GP-U 71.08151.M06

74LVC1G08GW-1-GP

73.01G08.L04

2ND = 73.01G08.EHG

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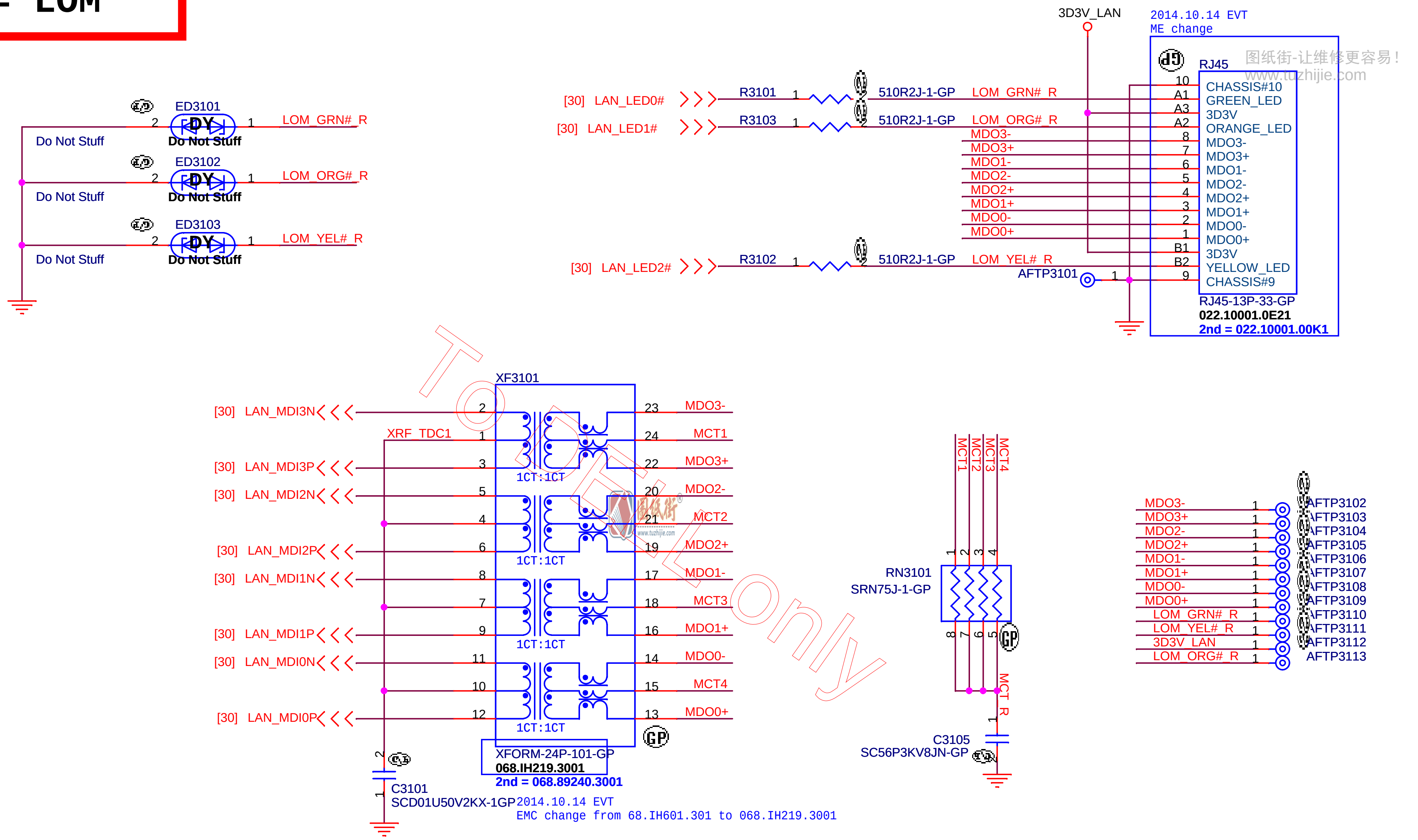
Title: LOM RTK8151G			
Size: A4	Document Number: Plano 11.6" UMA		Rev: A00
Date: Wednesday, April 22, 2015		Sheet 30 of 110	

SSID = LOM

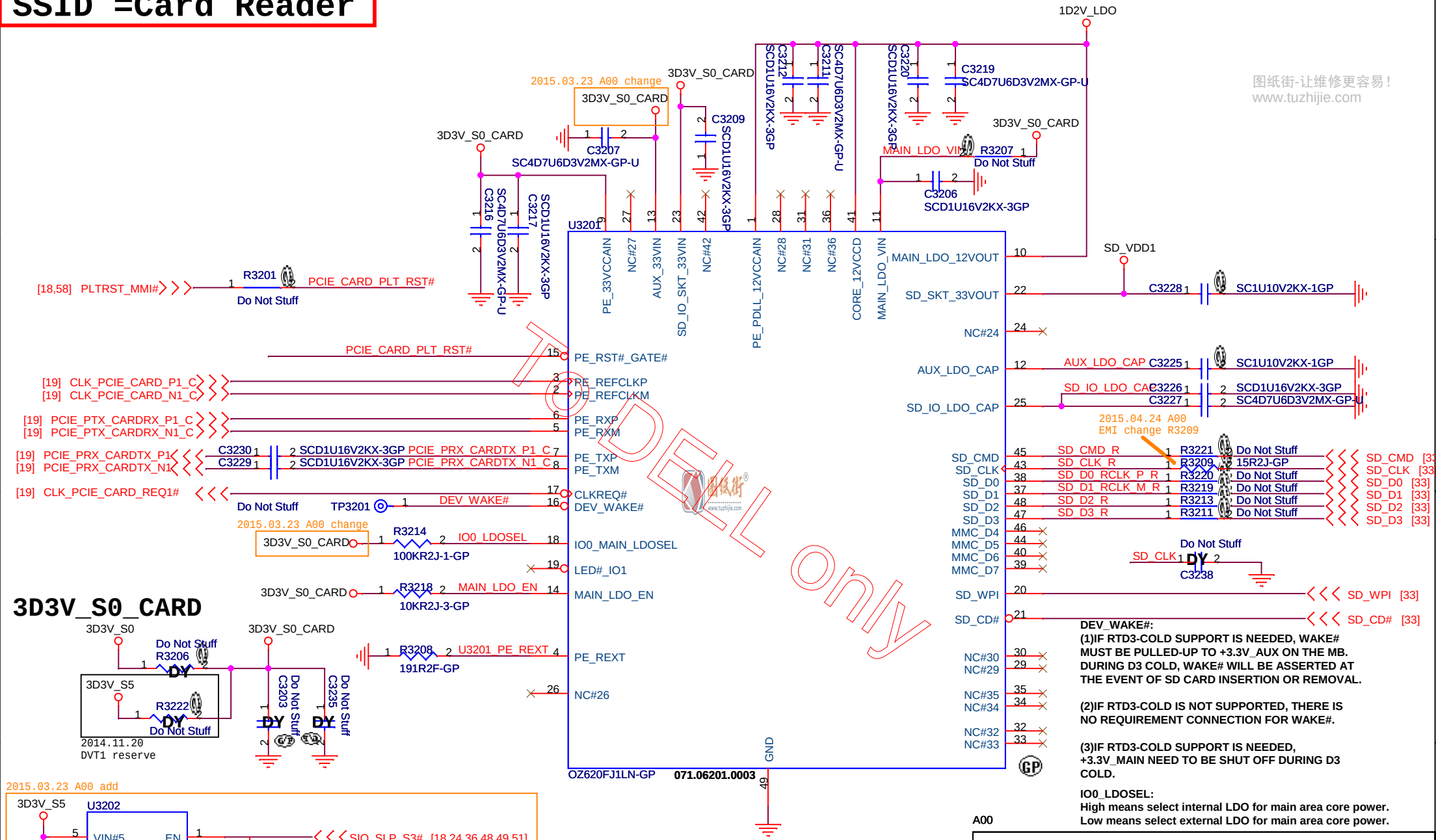


A00

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RJ45/Transformer	
Size A4	Document Number: Plano 11.6" UMA	Rev A00
Date: Wednesday, April 22, 2015	Sheet 31 of 110	

SSID =Card Reader



DEV_WAKE#:
(1)IF RTD3-COLD SUPPORT IS NEEDED, WAKE# MUST BE PULLED-UP TO +3.3V_AUX ON THE MB. DURING D3 COLD, WAKE# WILL BE ASSERTED AT THE EVENT OF SD CARD INSERTION OR REMOVAL.

(2)IF RTD3-COLD IS NOT SUPPORTED, THERE IS NO REQUIREMENT CONNECTION FOR WAKE#.

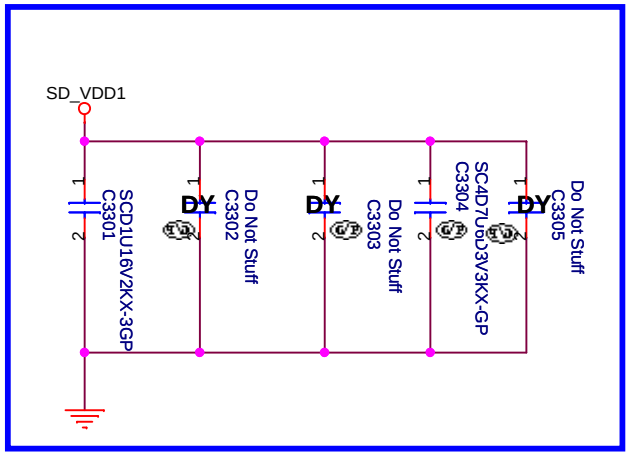
(3)IF RTD3-COLD SUPPORT IS NEEDED, +3.3V_MAIN NEED TO BE SHUT OFF DURING D3 COLD.

IO0_LDOSEL:
High means select internal LDO for main area core power.
Low means select external LDO for main area core power.

A00

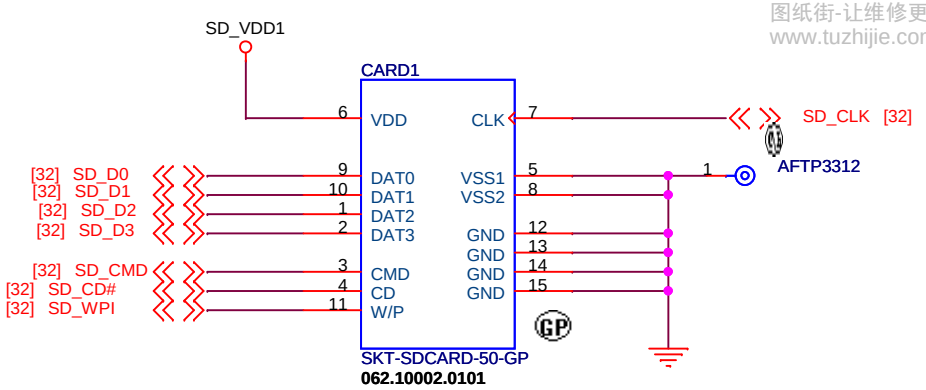
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Card Reader		
Size: A4	Document Number: Plano 11.6" UMA	Rev: A00
Date: Friday, April 24, 2015	Sheet 32 of 110	

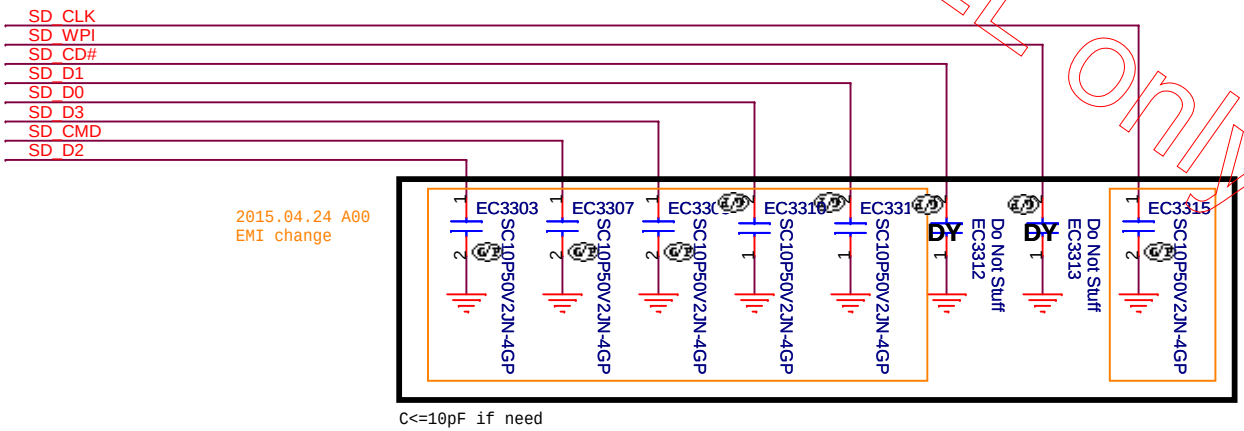
SSID =Card Reader

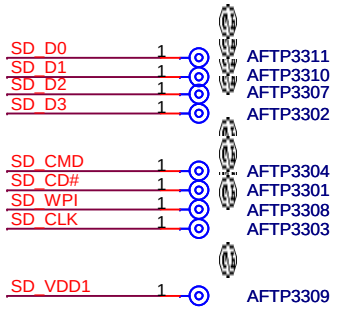


Layout Note:Close to Card Reader CONN

SD 3.0 Card Connector







A00

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Card Reader CONN**

Size	Document Number	Rev
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Date: Friday, May 29, 2015 Sheet 33 of 110

SSID = USB

[16] USB3_PTX_CRX_P0 → C3403 SCD1U16V2KX-3GP → USB3_PTX_CRX_P0_R → R3405 Do Not Stuff → USB3_PTX_CRX_P0_C

[16] USB3_PTX_CRX_N0 → C3404 SCD1U16V2KX-3GP → USB3_PTX_CRX_N0_R → R3406 Do Not Stuff → USB3_PTX_CRX_N0_C

[16] USB3_PRX_CTX_P0 → R3407 Do Not Stuff → USB3_PRX_CTX_P0_C

[16] USB3_PRX_CTX_N0 → R3408 Do Not Stuff → USB3_PRX_CTX_N0_C

EU3403 AZ1045-04F-R7G-GP

USB3_PRX_CTX_N0_C	1	LINE_1	NC#10	10	USB3_PRX_CTX_N0_C
USB3_PRX_CTX_P0_C	2	LINE_2	NC#9	9	USB3_PRX_CTX_P0_C
	3	GND	GND	8	
USB3_PTX_CRX_N0_C	4	LINE_3	NC#7	7	USB3_PTX_CRX_N0_C
USB3_PTX_CRX_P0_C	5	LINE_4	NC#6	6	USB3_PTX_CRX_P0_C

2014.12.08 DVT1 change

75.01045.073

USB30_VCCB
USB20_DN0_C
USB20_DP0_C
USB3_PRX_CTX_N0_C
USB3_PRX_CTX_P0_C
USB3_PTX_CRX_N0_C
USB3_PTX_CRX_P0_C

AFTP3410
AFTP3411
AFTP3412
AFTP3413
AFTP3414
AFTP3415
AFTP3416

EU3404 AZC099-04S-1-GP

USB_PN0_R	1	I/O1	I/O4	6	USB_PP0_R
	2	GND	VDD	5	
	3	I/O2	I/O3	4	

75.09904.07C
2nd = 75.04285.07C

USB30_VCCB

EXT Port1 Left Side, Support Power Share

USB1

1	VBUS	D-	2	USB20_DN0_C
		D+	3	USB20_DP0_C
USB3_PRX_CTX_N0_C	5	STDA_SSRX-	GND_DRAIN	7	
USB3_PRX_CTX_P0_C	6	STDA_SSRX+		
USB3_PTX_CRX_N0_C	8	STDA_SSTX-	GND	10	AFTP3409
USB3_PTX_CRX_P0_C	9	STDA_SSTX+	GND	11	
12	CHASSIS#12	GND	4	
13	CHASSIS#13		

SKT-USB13-18-GP-U
22.10339.331
2nd = 22.10339.S31

[35] USB_PP0_R
[35] USB_PN0_R

2nd = 068.CMF11.2011
68.01012.20B

FILTER-4P-137-GP-U
TR3405

---

[16] USB3_PTX_CRX_P1 → C3401 SCD1U16V2KX-3GP → USB3_PTX_CRX_P1_R → R3401 Do Not Stuff → USB3_PTX_CRX_P1_C

[16] USB3_PTX_CRX_N1 → C3402 SCD1U16V2KX-3GP → USB3_PTX_CRX_N1_R → R3402 Do Not Stuff → USB3_PTX_CRX_N1_C

[16] USB3_PRX_CTX_P1 → R3403 Do Not Stuff → USB3_PRX_CTX_P1_C

[16] USB3_PRX_CTX_N1 → R3404 Do Not Stuff → USB3_PRX_CTX_N1_C

EU3401 AZ1045-04F-R7G-GP

USB3_PRX_CTX_N1_C	1	LINE_1	NC#10	10	USB3_PRX_CTX_N1_C
USB3_PRX_CTX_P1_C	2	LINE_2	NC#9	9	USB3_PRX_CTX_P1_C
	3	GND	GND	8	
USB3_PTX_CRX_N1_C	4	LINE_3	NC#7	7	USB3_PTX_CRX_N1_C
USB3_PTX_CRX_P1_C	5	LINE_4	NC#6	6	USB3_PTX_CRX_P1_C

2014.12.08 DVT1 change

75.01045.073

USB30_VCCA
USB3_PRX_CTX_N1_C
USB3_PRX_CTX_P1_C
USB20_DN1_C
USB20_DP1_C
USB3_PTX_CRX_P1_C
USB3_PTX_CRX_N1_C

AFTP3401
AFTP3403
AFTP3404
AFTP3405
AFTP3406
AFTP3407
AFTP3408

EU3402

USB30_VCCA

USB_PN1	1	I/O1	I/O4	6	USB_PP1
	2	GND	VDD	5	
	3	I/O2	I/O3	4	

AZC099-04S-1-GP
75.09904.07C
2nd = 75.04285.07C

2014.12.01 DVT
EMC install

EXT Port2 Right Side

USB30_VCCA

USB2 SKT-USB13-197-GP

1	VBUS	CHASSIS#10	10	
		CHASSIS#11	11	
USB20_DN1_C	2	D-	CHASSIS#12	12	
USB20_DP1_C	3	D+	CHASSIS#13	13	
USB3_PRX_CTX_N1_C	5	SSRX-			AFTP3402
USB3_PRX_CTX_P1_C	6	SSRX+		
			PGND	4	
USB3_PTX_CRX_N1_C	8	SSTX-	GND	7	
USB3_PTX_CRX_P1_C	9	SSTX+		
		USB3.0		

022.10005.00H1

A00

[16] USB_PP1
[16] USB_PN1

2nd = 068.CMF11.2011
68.01012.20B

FILTER-4P-137-GP-U
TR3403

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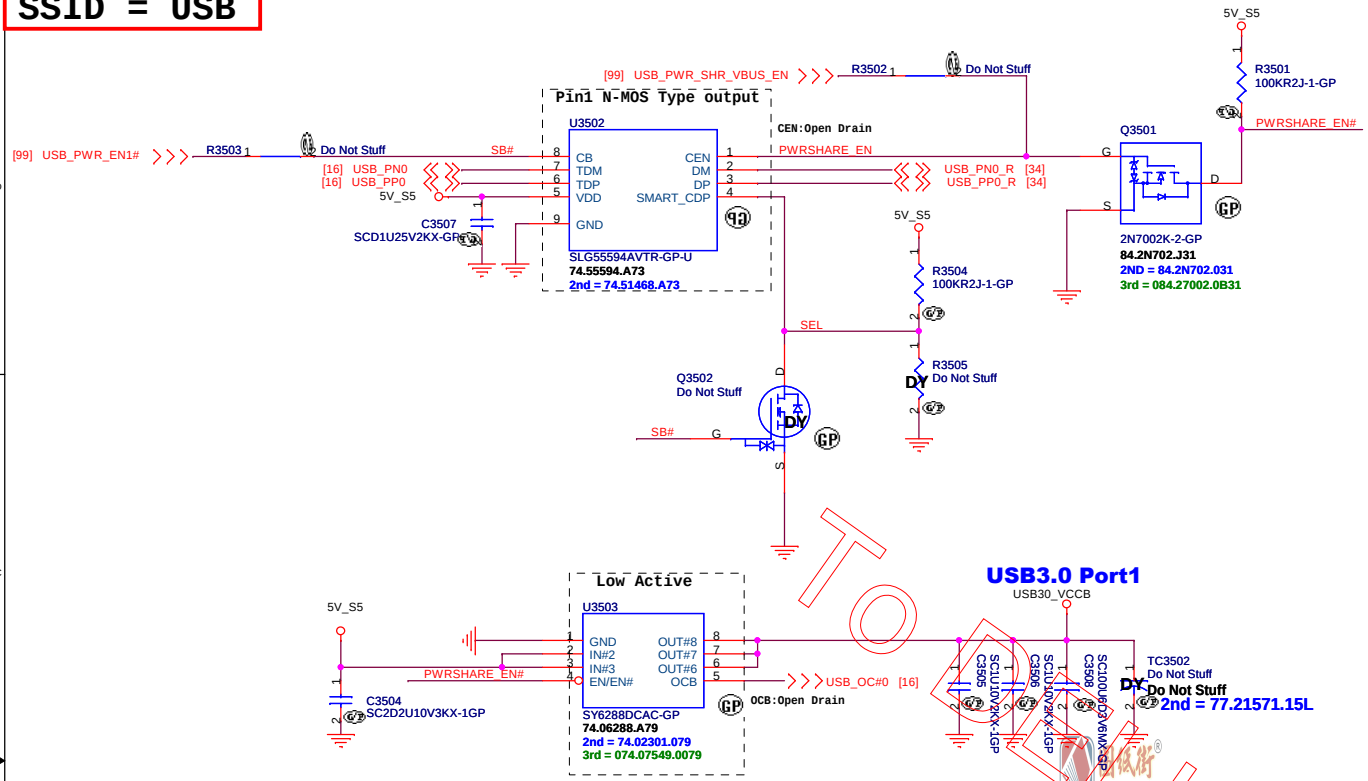
Wistron Corporation	Title: USB 3.0 Port	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	Size: A4	Document Number: Plano 11.6" UMA
	Rev: A00	
	Date: Wednesday, November 11, 2015	Sheet 34 of 110

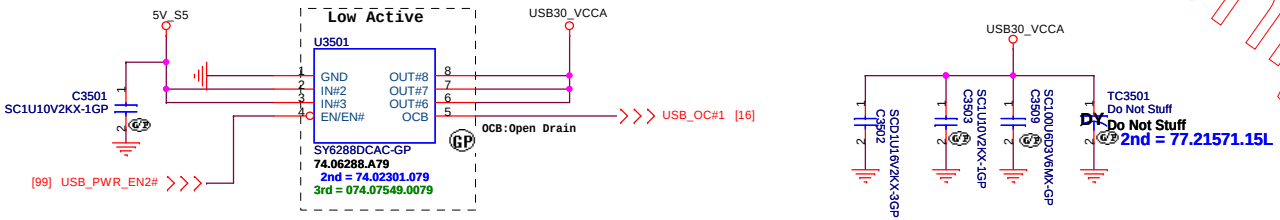
SSID = USB



AC mode				
feature enabled/Wake on USB enabled				
	S0	S3	S4	S5
USBPowerShare_EN# PP	1	1	1	1
USBPwrShr_Vbus_EN OD	1	1	1	1
feature enabled/Wake on USB disabled				
	S0	S3	S4	S5
USBPowerShare_EN# PP	1	0	0	0
USBPwrShr_Vbus_EN OD	1	1	1	1
feature disabled/Wake on USB enabled				
	S0	S3	S4	S5
USBPowerShare_EN# PP	1	1	1	1
USBPwrShr_Vbus_EN OD	1	1	1	1
featured disabled/Wake on USB disabled				
	S0	S3	S4	S5
USBPowerShare_EN# PP	1	0	0	0
USBPwrShr_Vbus_EN OD	1	0	0	0

Battery mode				
feature enabled/Wake on USB enabled				
	S0	S3	S4	S5
USBPowerShare_EN# PP	1	1	x	x
USBPwrShr_Vbus_EN OD	1	1	x	x
feature enabled/Wake on USB disabled				
	S0	S3	S4	S5
USBPowerShare_EN# PP	1	0	x	x
USBPwrShr_Vbus_EN OD	1	1	x	x
featured disabled/Wake on USB enabled				
	S0	S3	S4	S5
USBPowerShare_EN# PP	1	1	x	x
USBPwrShr_Vbus_EN OD	1	1	x	x
featured disabled/Wake on USB disabled				
	S0	S3	S4	S5
USBPowerShare_EN# PP	1	0	x	x
USBPwrShr_Vbus_EN OD	1	0	x	x

CB	SMART-CDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device) And, when Non-CDP phone is plugged in, the CDP mode will be changed automatically to SDP mode during handshaking protocol for supporting data communication.



USB Power SW (U3501 & U3503)

Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DII (Diodes)	AP2301MPG-13	74.02301.079	2ND

A00

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.0 Power SW

Size | Document Number: Plano 11.6" UMA | Rev: A00

Date: Wednesday, April 22, 2015 | Sheet 35 of 110

SSID = Reset.Suspend

Power Sequence

From 3V 5V VR

From EC

5V_S0/3D3V_S0

3D3V_LAN/LCDCDD POWER

1D8V_S0

3D3V_S5_PRIME

Discharge circuit

3D3V_S5_PRIME power good

Power Sequence

DDR3_VCCA_PWRGD

DDR3_DRAM_PWROK

Reserve for HW fine tune power sequence

2014.03.21 for power off sequence to meet EDS

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable
Size: Custom | Document Number: Plano 11.6 UMA | Rev: 0.2
Date: Wednesday, May 13, 2015 | Sheet 36 of 110

SSID = Reset.Suspend

(Blanking)

A00

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER

Size	Document Number	Rev
A4	Plano 11.6" UMA	A00

Date: Friday, March 27, 2015 Sheet 37 of 110

(Blanking)

A00

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Title: Reserved

Size	Document Number	Rev
A4	Plano 11.6" UMA	A00

Date: Friday, March 27, 2015 Sheet 38 of 110

(Blanking)

A00

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A	*Plano 11.6" UMA*	A00

Date: Friday, March 27, 2015 Sheet 39 of 110

SSID = 0BFF

(Blanking)

A00

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A4	Plano 11.6" UMA	A00

Date: Friday, March 27, 2015 Sheet 40 of 110

(Blanking)

A00

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Title

Reserved

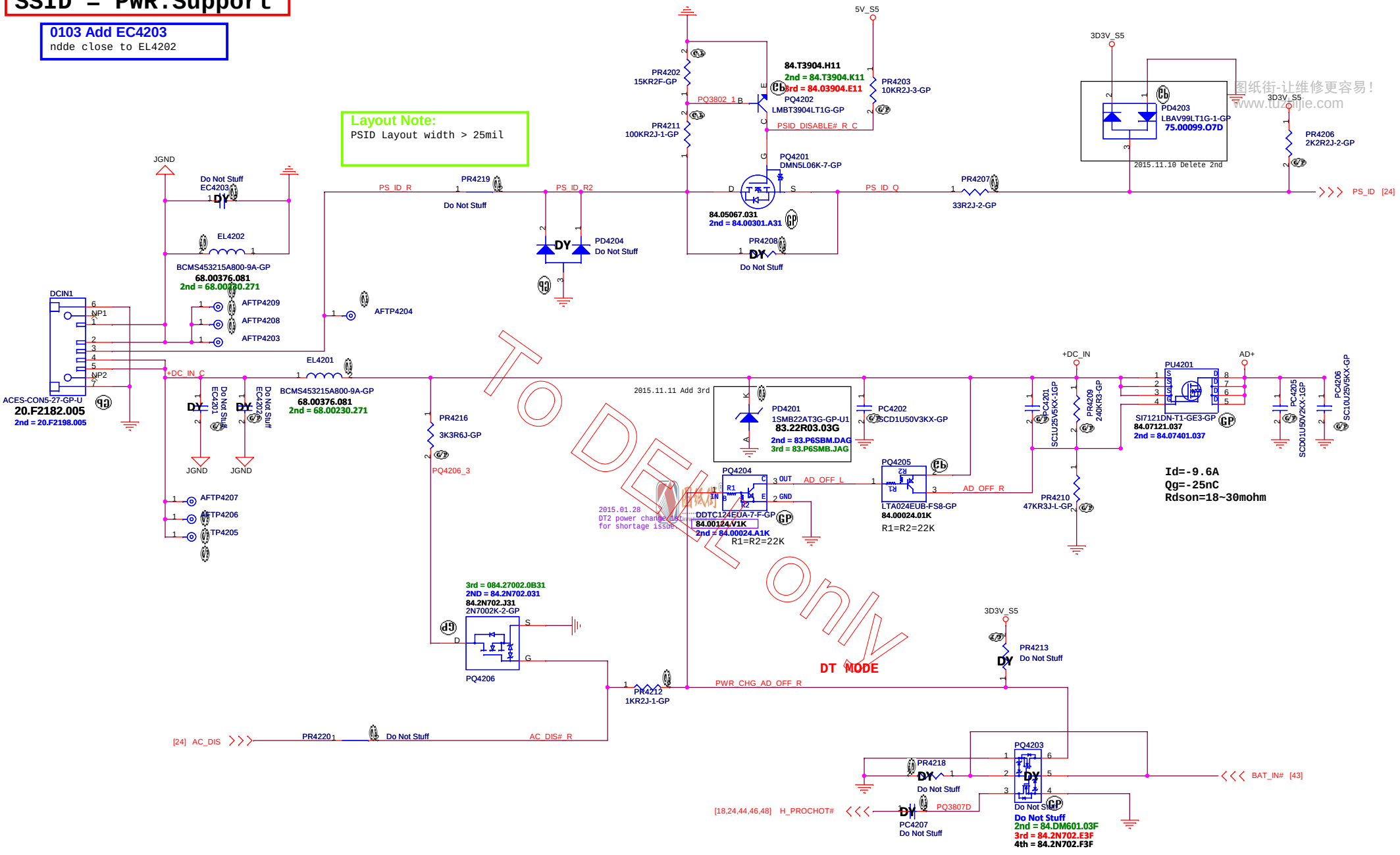
Size	Document Number	Rev
A	*Plano 11.6" UMA*	A00

Date: Friday, March 27, 2015 Sheet 41 of 110

SSID = PWR.Support

0103 Add EC4203
ndde close to EL4202

Layout Note:
PSID Layout width > 25mil



A00

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

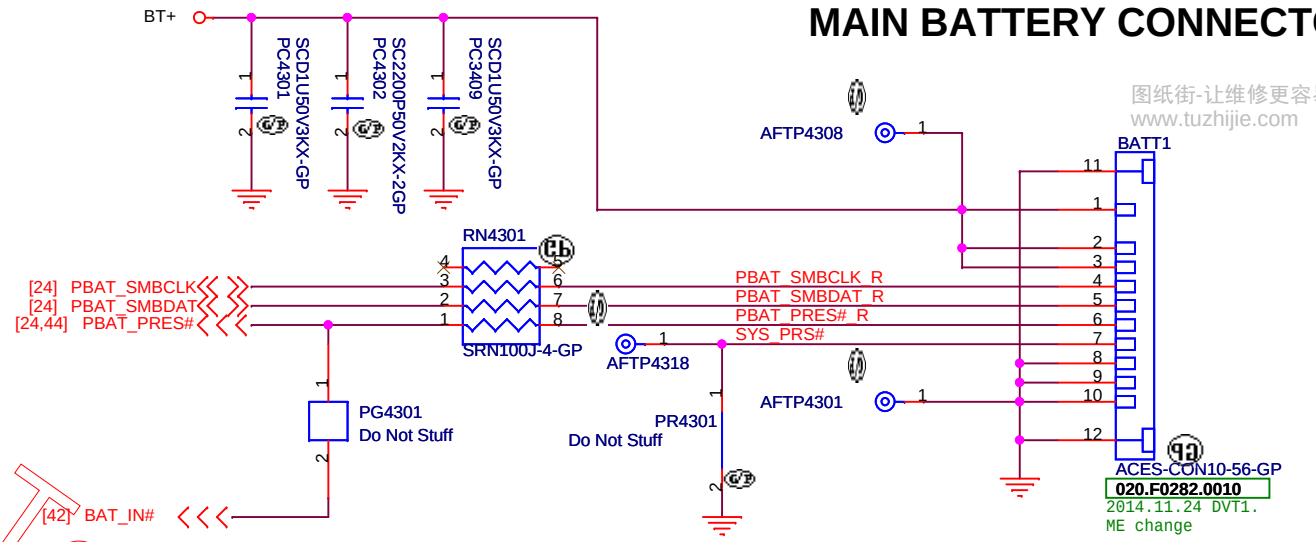
Title: **DCIN JACK**

Size	Document Number	Rev
A3	Plano 11.6" UMA	A00

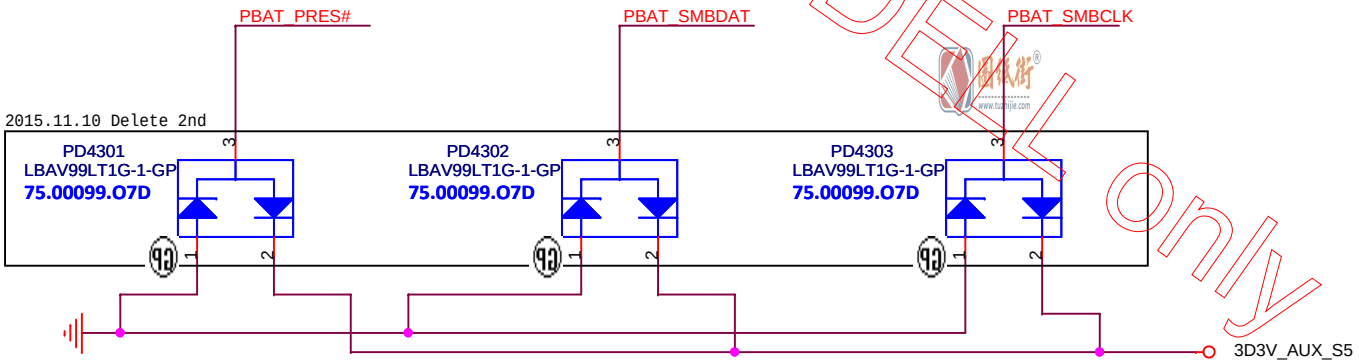
Date: Wednesday, November 18, 2015 Sheet 42 of 110

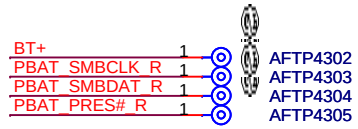
SSID = PWR.Support

MAIN BATTERY CONNECTOR



Layout Note: Place near Battery CONN





A00

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATTERY CONN

Size	Document Number	Rev
A4	Plano 11.6" UMA	A00

Date: Wednesday, November 11, 2015 Sheet 43 of 110

SSID = Charger

KBC FOR DT MODE
CHECK EE PULL HIGH

VacDET=2.4V
Acok setting=2.4*((PR4444+PR4411)/PR4411)
2.4*((369+49.9)k/49.9k)=17.26172V
Setting=17.26v

ACAV_IN
H=ACIN
L=UNAC

PT_0802

value check EE follow fanseca

VREGN_REG	REGN Regulator Voltage	VVCC > 6.5V, VACDET>0.6V (0-50mA load)	5.5	6	6.5	V

REGN REGULATOR

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGE(BQ24715)
Size: A2 | Document Number: MAIN 21.0 UMA | Rev: A00
Date: Wednesday, April 22, 2015 | Sheet 44 of 110

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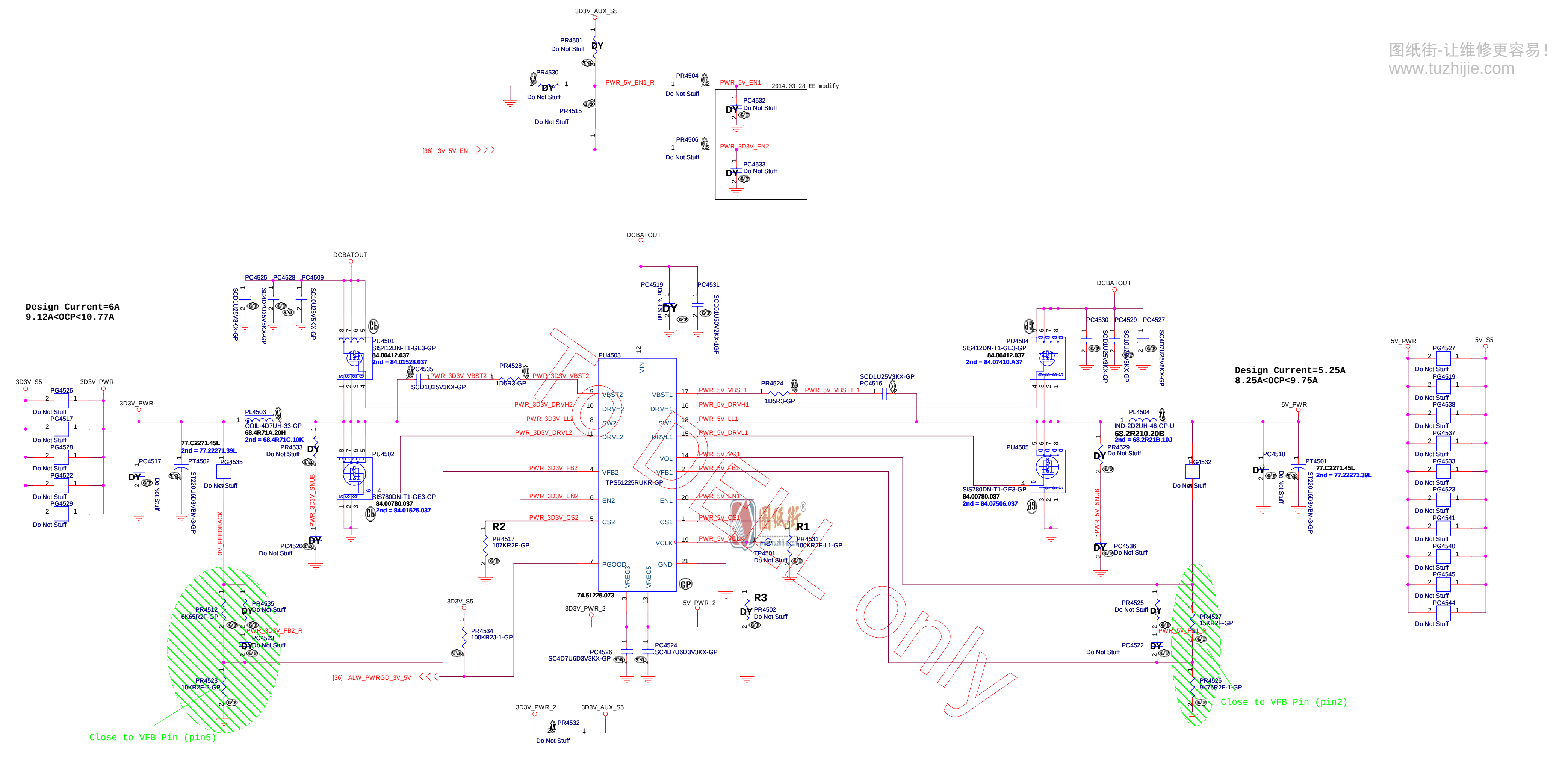
SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 4.7UH PCMB063T-4R7MS Cyntec 28mohm/33mohm Isat =6.5Arms 68.4R71A.20H
O/P capCHIP CAP T 220U 6.3V M3528 PSL /NEC/ 25mOhm / 77.C2271.45L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

TPS51225 & TPS51285 Co-lay

	TPS51225	TPS51285
R1	100K	20K
R2	107K	21.5K
R3	DY	200

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P capCHIP CAP T 220U 6.3V M3528 PSL /NEC/ 25mOhm / 77.C2271.45L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

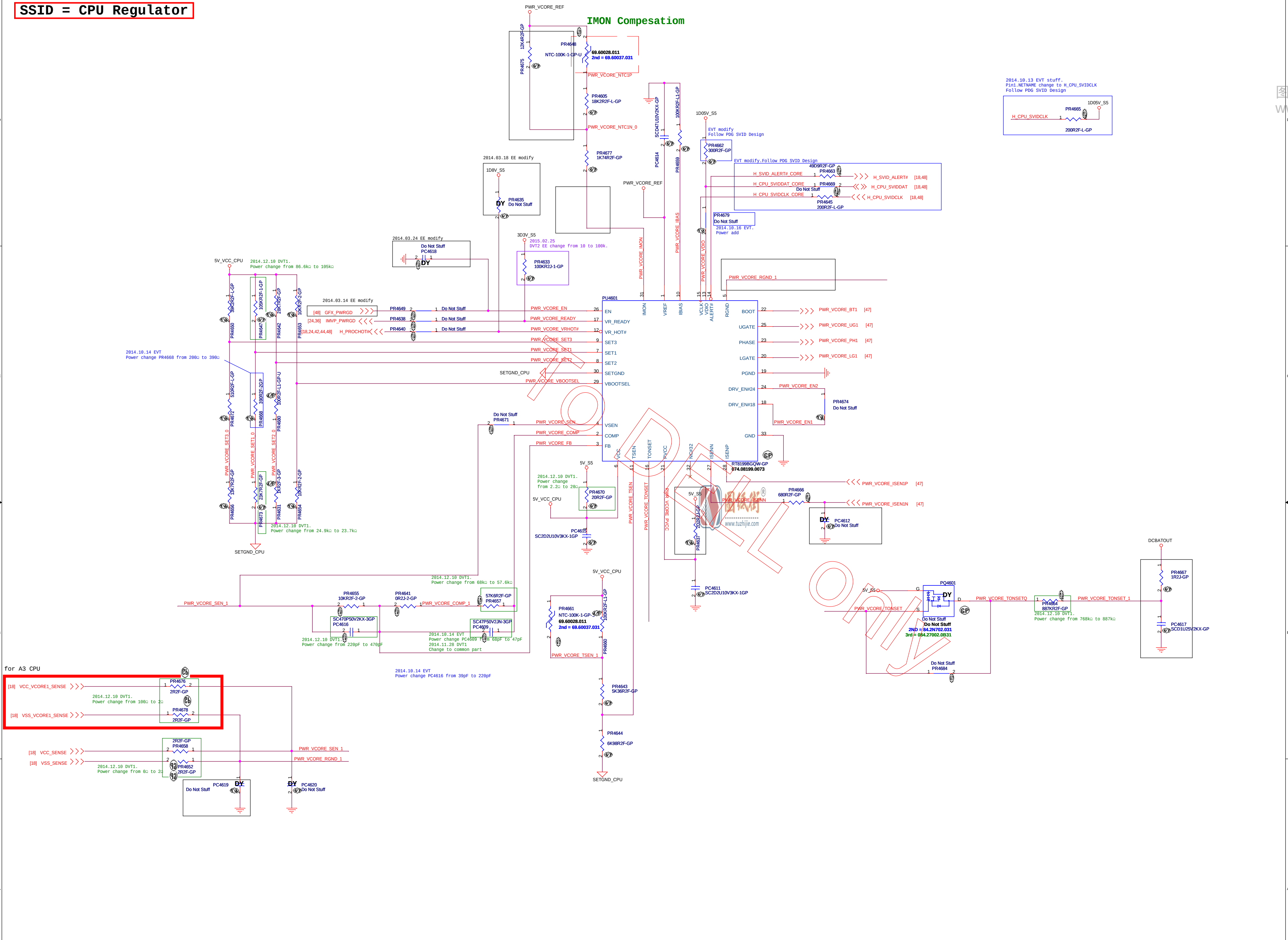
A00

DELL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51225_5V/3D3V
Size A2 Plano 11.6" UMA Rev A00

SSID = CPU Regulator

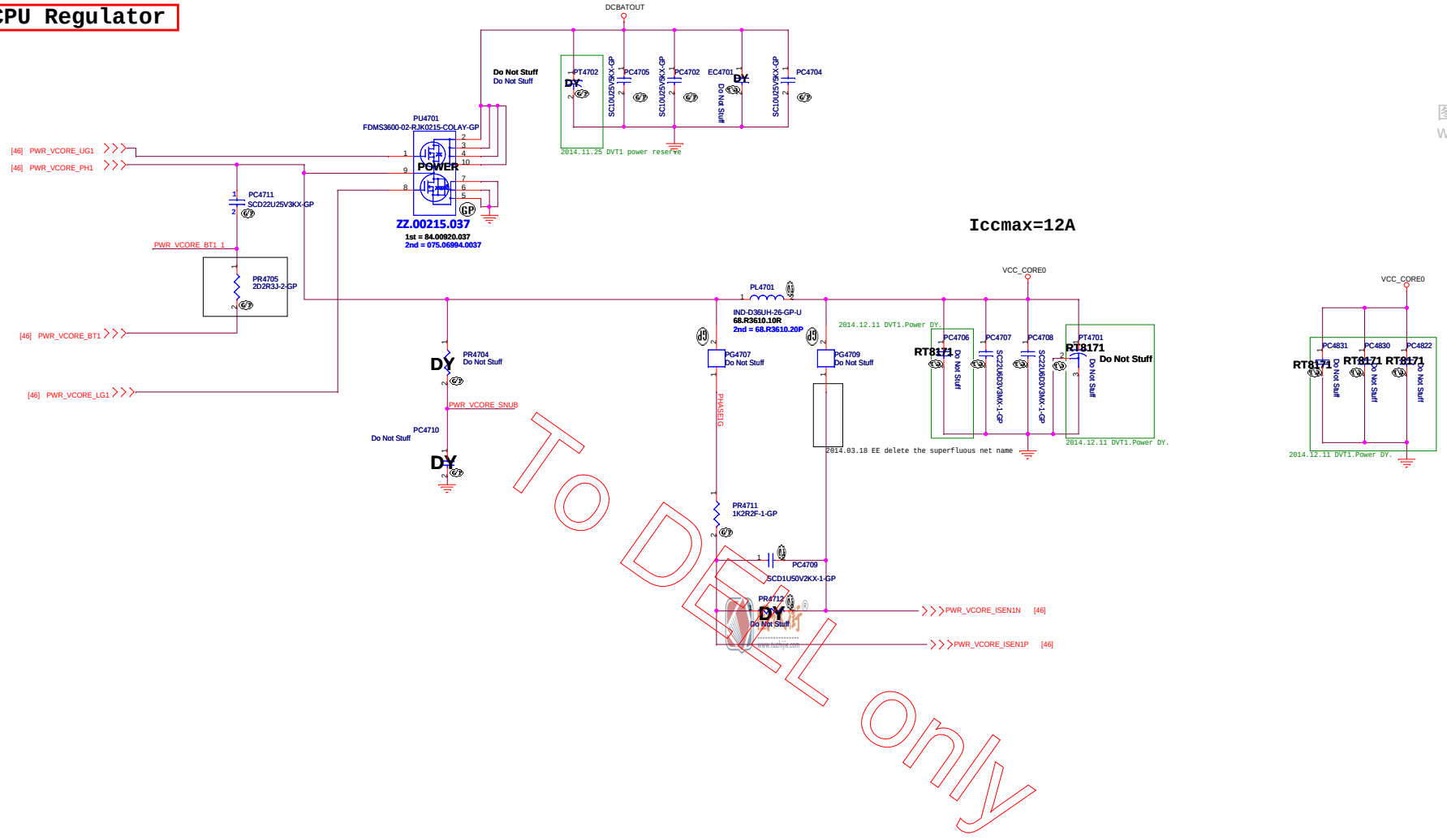


A00

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8171B_CPUCORE(1/3)	
Size: Custom	Document Number: Plano 11.6" UMA	Rev: A00
Date: Thursday, April 23, 2015	Sheet 46 of 110	

SSID = CPU Regulator



A00

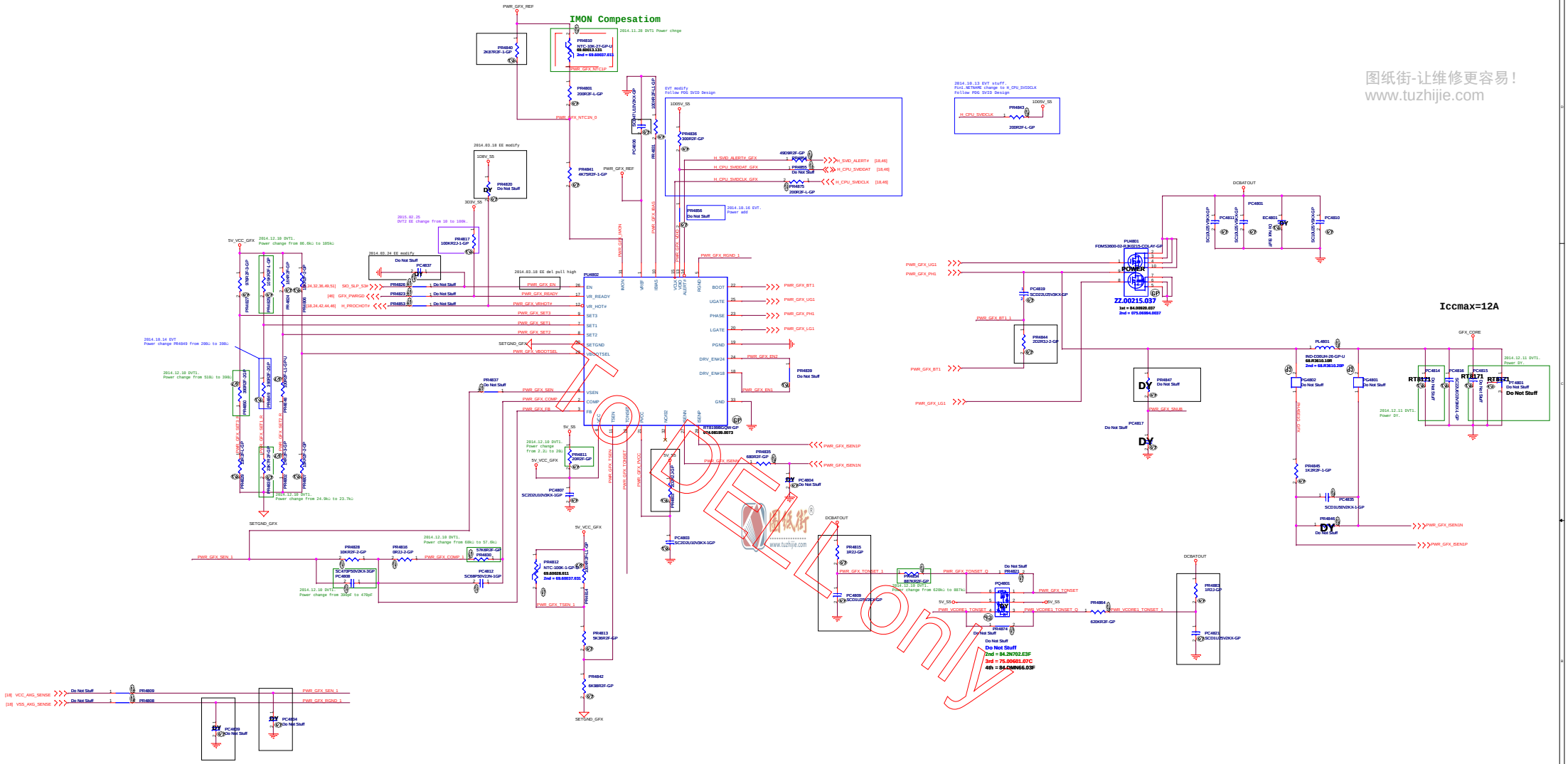
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8171B_CPU Regulator

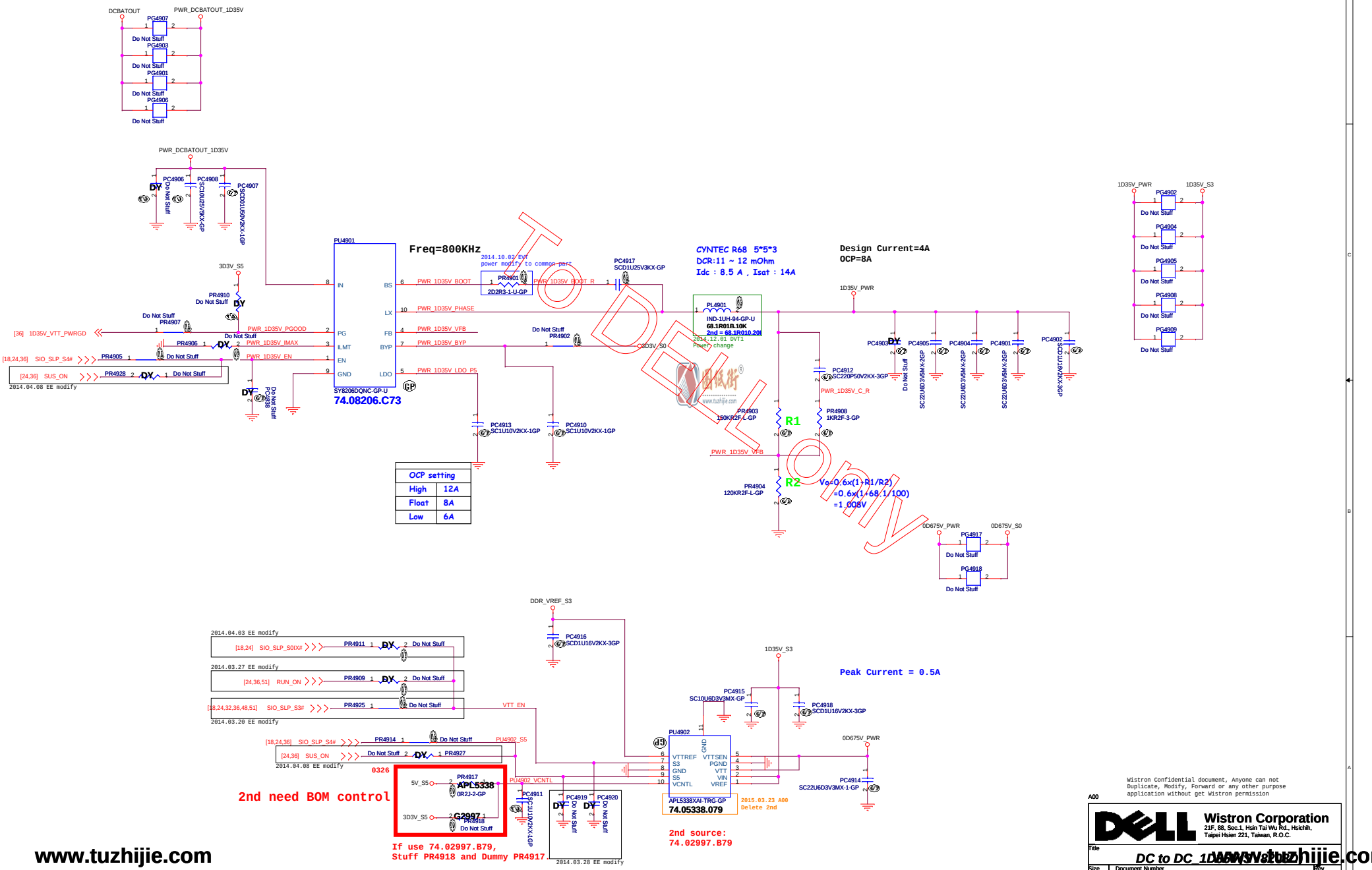
Size: C | Document Number: Plano 11.6" UMA | Rev: A00

Date: Wednesday, April 22, 2015 | Sheet 47 of 110

SSID = GFX Regulator



SY8206D for 1D35V



A00

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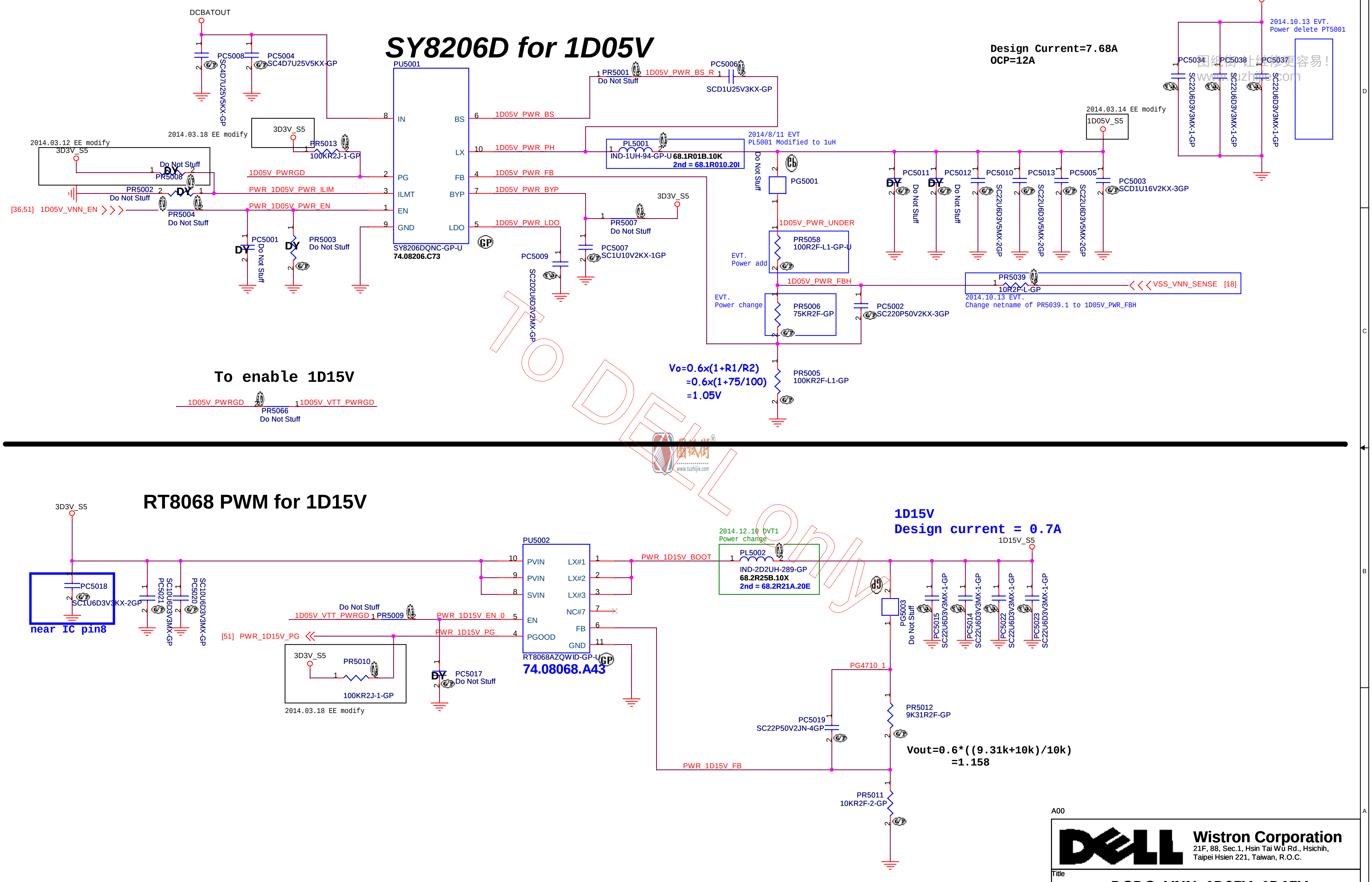
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC_1D35V(SY8206D)

Size: C | Document Number: Plano 11.6" UMA | Rev: A00

Date: Wednesday, April 22, 2015 | Sheet 49 of 110

SSID = PWR.Plane.Regulator_1p05v



SY8206D for 1D05V
Design Current=7.68A
OCP=12A
DCBATOUT
PC5008
SC4D7U25V5KX-GP
PC5004
SC4D7U25V5KX-GP
PU5001
IN
BS
LX
PG
FB
ILMT
BYP
EN
GND
LDO
SY8206DQNC-GP-U
74.08206.C73
1D05V_PWR_BS
1D05V_PWR_PH
1D05V_PWR_FB
1D05V_PWR_BYP
1D05V_PWR_LDO
1D05V_PWRGD
PWR_1D05V_PWR_ILMT
PWR_1D05V_PWR_EN
PR5001
Do Not Stuff
1D05V_PWR_BS_R
PC5006
SCD1U25V3KX-GP
2014.03.18 EE modify
3D3V_S5
PR5013
100KR2J-1-GP
2014.03.12 EE modify
Do Not Stuff
PR5008
PR5002
PR5004
[36,51] 1D05V_VNN_EN
PC5001
PR5003
PR5007
PC5007
SC1U10V2KX-1GP
PC5009
SC2D2U6D3V2MX-GP
2014/8/11 EVT
PL5001 Modified to 1uH
PL5001
IND-1UH-94-GP-U
68.1R01B.10K
2nd = 68.1R010.20I
PG5001
1D05V_PWR_UNDER
PR5058
100R2F-L1-GP-U
EVT.
Power add
1D05V_PWR_FBH
EVT.
Power change
PR5006
75KR2F-GP
PC5002
SC220P50V2KX-3GP
PR5039
10R2F-L-GP
VSS_VNN_SENSE [18]
2014.10.13 EVT.
Change netname of PR5039.1 to 1D05V_PWR_FBH
PR5005
100KR2F-L1-GP
Vo=0.6x(1+R1/R2)
=0.6x(1+75/100)
=1.05V
PC5011
PC5012
PC5010
PC5013
PC5005
PC5003
SC22U6D3V5MX-2GP
SCD1U16V2KX-3GP
2014.03.14 EE modify
1D05V_S5
2014.10.13 EVT.
Power delete PT5001
PC5034
PC5038
PC5037
SC22U6D3V3MX-1-GP
To enable 1D15V
1D05V_PWRGD
PR5066
Do Not Stuff
1D05V_VTT_PWRGD
RT8068 PWM for 1D15V
3D3V_S5
PC5018
SC1U6D3V3KX-2GP
near IC pin8
PC5021
PC5020
SC10U6D3V3MX-GP
PU5002
PVIN
SVIN
EN
PGOOD
LX#1
LX#2
LX#3
NC#7
FB
GND
RT8068AZQWID-GP-U
74.08068.A43
1D05V_VTT_PWRGD
PR5009
PWR_1D15V_EN_0
[51] PWR_1D15V_PG
PR5010
100KR2J-1-GP
2014.03.18 EE modify
PC5017
Do Not Stuff
PWR_1D15V_BOOT
2014.12.10 DVT1
Power change
PL5002
IND-2D2UH-289-GP
68.2R25B.10X
2nd = 68.2R21A.20E
1D15V
Design current = 0.7A
1D15V_S5
PG5003
PC5015
PC5014
PC5022
PC5023
SC22U6D3V3MX-1-GP
PG4710_1
PR5012
9K31R2F-GP
PC5019
SC22P50V2JN-4GP
Vout=0.6*((9.31k+10k)/10k)
=1.158
PWR_1D15V_FB
PR5011
10KR2F-2-GP

A00

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

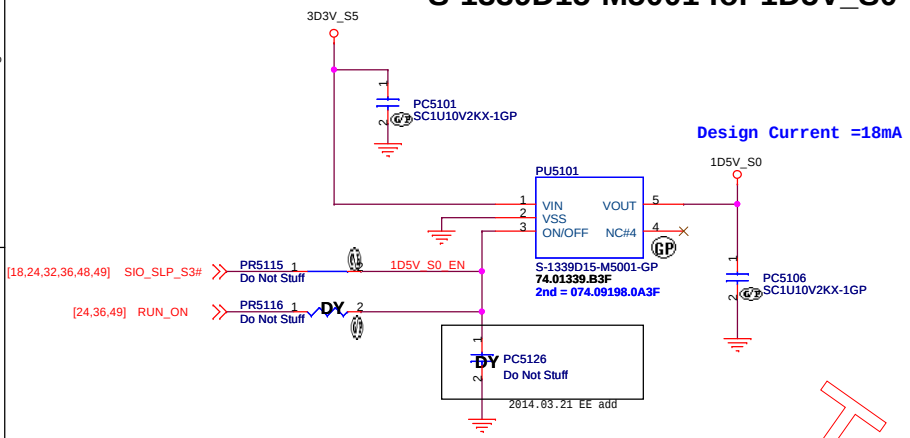
Title: **DCDC_VNN_1D05V..1D15V**

Size: A3 | Document Number: **Plano 11.6" UMA** | Rev: **A00**

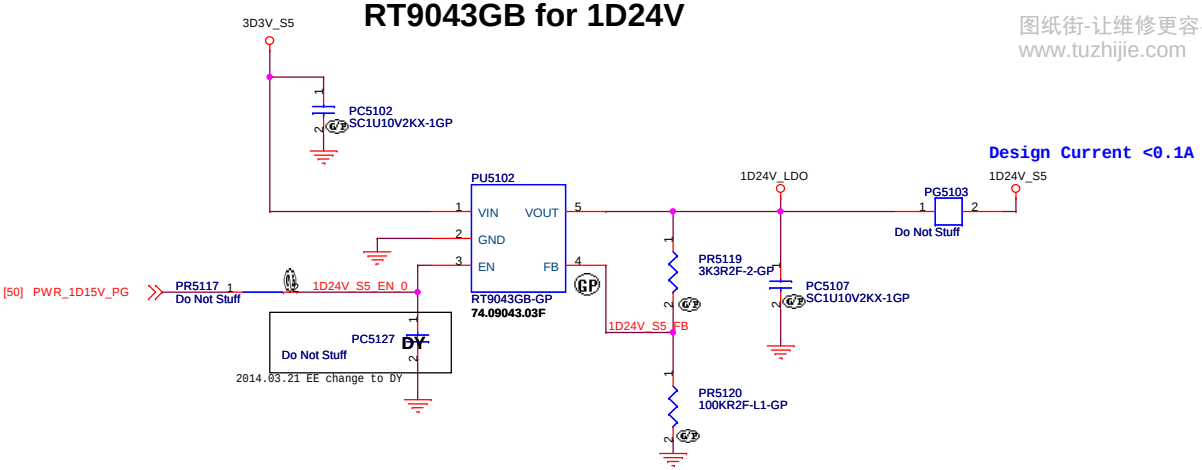
Date: Wednesday, April 22, 2015 | Sheet 50 of 110

SSID = PWR.Plane.Regulator_1p5v

S-1339D15-M5001 for 1D5V_S0

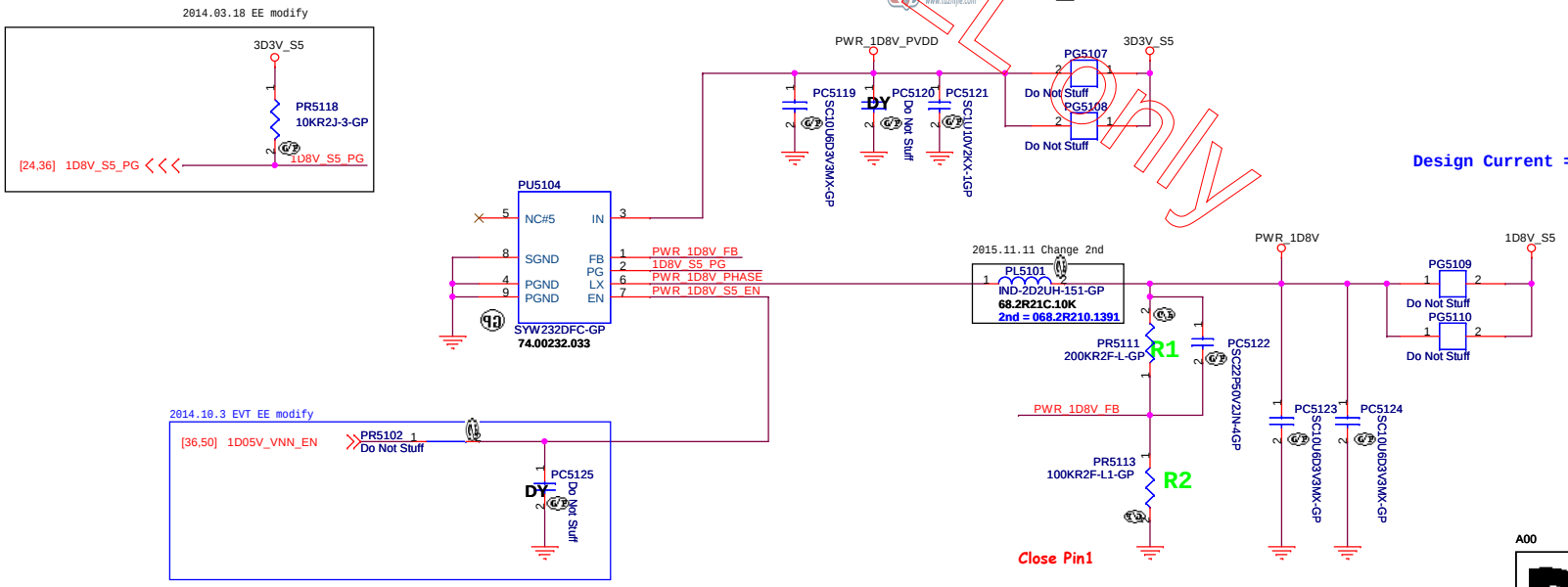


RT9043GB for 1D24V



SSID = PWR.Plane.Regulator_1p8v

SYW232 for 1D8V_S5



A00

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D8V_1D5V_1D24V...

Size: A3 | Document Number: Plano 11.6" UMA | Rev: A00

Date: Wednesday, November 11, 2015 | Sheet 51 of 110

SSID = VIDEO

eDP CONNECTOR

LCD1 IPEX-CONN40-2R-2-GP

Panel(INNOLUX/N116BGE) HPD High level :2.25~2.75V
Panel(AUO/B116XTN02) HPD High level :2~3.6V

20.F2379.040
2nd = 20.F2091.040
2014.10.21 EVT. ME change

Camera Power

DMP2130 continuous 2.4A
Rds(on) = 99~125 mOhm
|VGS|max=12V

Q5201 DMP2130L-7-GP
84.02130.031
2ND = 84.00102.031
3rd = 84.03413.B31

TOUCH PANEL POWER

DMP2130 continuous 2.4A
Rds(on) = 99~125 mOhm
|VGS|max=12V

Q5206 DMP2130L-7-GP
84.02130.031
2ND = 84.00102.031
3rd = 84.03413.B31

Q5207 DMN5L06K-7-GP
2nd = 84.00301.A31
84.05067.031

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SI3457 continuous 2.5A

Rds(on) = 0.113~0.092 Ohm
|VGS|max=20V

U5201 SI3457CDV-T1-GE3-GP
84.03457.A3D
2ND = 84.00658.83D
3rd = 84.00658.C3D

INVERTER POWER

Q5202 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 084.27002.0B31

TR5201 FILTER-4P-137-GP-U
68.01012.20B
2nd = 068.CMF11.2011

Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: eDP Connector			
Size: A3	Document Number: Hand 11.0 JUMA		Rev: A00
Date: Wednesday, November 11, 2015	Sheet 52 of 110		

(Blanking)

A00

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

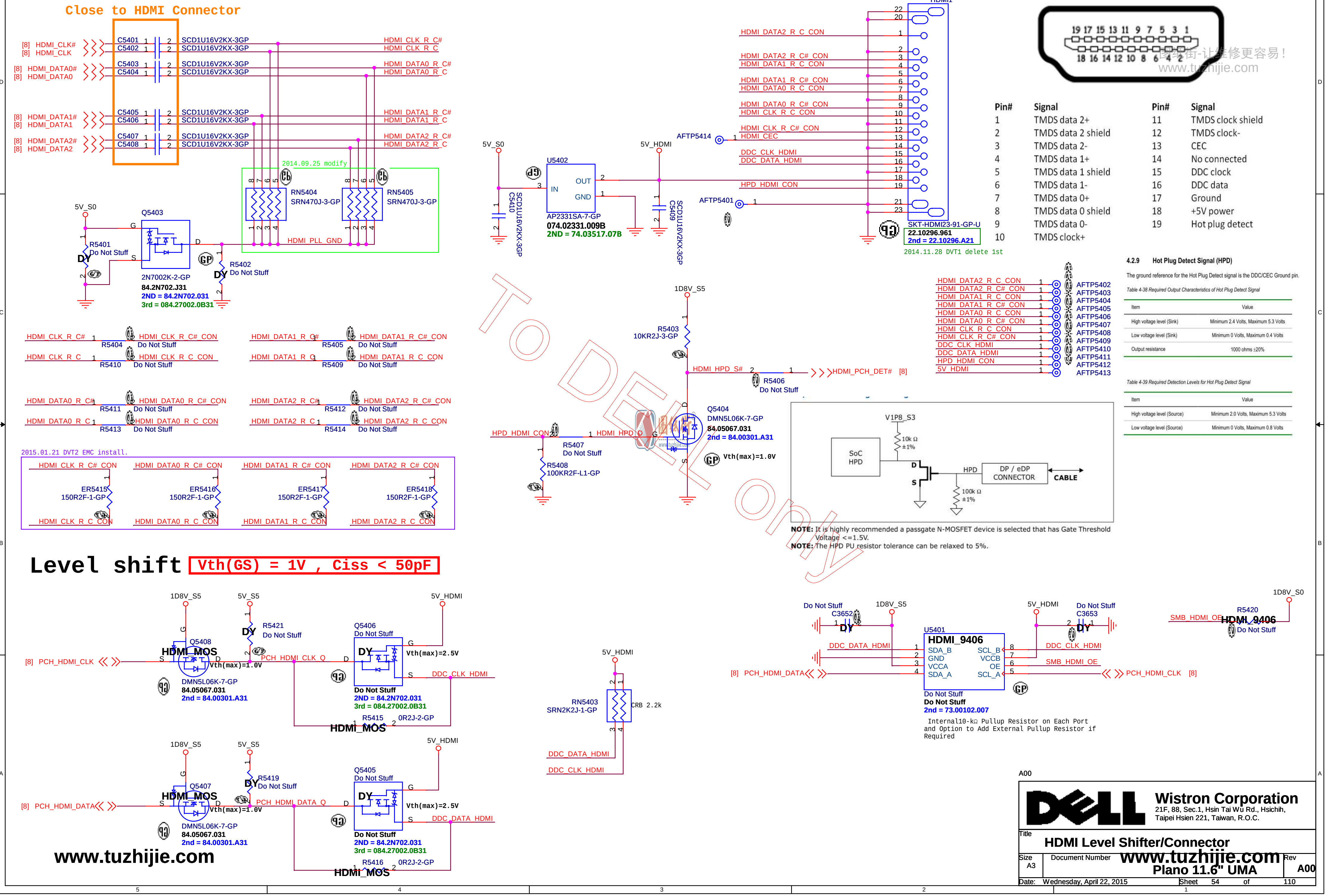
Title: (Reserved)

Size: A3 | Document Number: Plano 11.6" UMA | Rev: A00

Date: Friday, March 27, 2015 | Sheet 53 of 110

SSID = VIDEO

HDMI CONNECTOR



Close to HDMI Connector
[8] HDMI_CLK#
[8] HDMI_CLK
[8] HDMI_DATA0#
[8] HDMI_DATA0
[8] HDMI_DATA1#
[8] HDMI_DATA1
[8] HDMI_DATA2#
[8] HDMI_DATA2
C5401 SCD1U16V2KX-3GP
C5402 SCD1U16V2KX-3GP
C5403 SCD1U16V2KX-3GP
C5404 SCD1U16V2KX-3GP
C5405 SCD1U16V2KX-3GP
C5406 SCD1U16V2KX-3GP
C5407 SCD1U16V2KX-3GP
C5408 SCD1U16V2KX-3GP
HDMI_CLK_R_C#
HDMI_CLK_R_C
HDMI_DATA0_R_C#
HDMI_DATA0_R_C
HDMI_DATA1_R_C#
HDMI_DATA1_R_C
HDMI_DATA2_R_C#
HDMI_DATA2_R_C
2014.09.25 modify
RN5404 SRN470J-3-GP
RN5405 SRN470J-3-GP
HDMI_PLL_GND
5V_S0
Q5403
R5401 Do Not Stuff
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 084.27002.0B31
R5402 Do Not Stuff
5V_S0
U5402
IN OUT GND
AP2331SA-7-GP
074.02331.009B
2ND = 74.03517.07B
C5410 SCD1U16V2KX-3GP
5V_HDMI
C5409 SCD1U16V2KX-3GP
AFTP5414
AFTP5401
HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C#_CON
HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C#_CON
HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C#_CON
HDMI_CLK_R_C_CON
HDMI_CLK_R_C#_CON
HDMI_CEC
DDC_CLK_HDMI
DDC_DATA_HDMI
HPD_HDMI_CON
HDMI1
SKT-HDMI23-91-GP-U
22.10296.961
2nd = 22.10296.A21
2014.11.28 DVT1 delete 1st
HDMI_CLK_R_C# R5404 Do Not Stuff HDMI_CLK_R_C#_CON
HDMI_CLK_R_C R5410 Do Not Stuff HDMI_CLK_R_C_CON
HDMI_DATA1_R_C# R5405 Do Not Stuff HDMI_DATA1_R_C#_CON
HDMI_DATA1_R_C R5409 Do Not Stuff HDMI_DATA1_R_C_CON
HDMI_DATA0_R_C# R5411 Do Not Stuff HDMI_DATA0_R_C#_CON
HDMI_DATA0_R_C R5413 Do Not Stuff HDMI_DATA0_R_C_CON
HDMI_DATA2_R_C# R5412 Do Not Stuff HDMI_DATA2_R_C#_CON
HDMI_DATA2_R_C R5414 Do Not Stuff HDMI_DATA2_R_C_CON
2015.01.21 DVT2 EMC install.
ER5415 150R2F-1-GP
ER5416 150R2F-1-GP
ER5417 150R2F-1-GP
ER5418 150R2F-1-GP
1D8V_S5
R5403 10KR2J-3-GP
HDMI_HPD_S#
R5406 Do Not Stuff
HDMI_PCH_DET# [8]
Q5404 DMN5L06K-7-GP
84.05067.031
2nd = 84.00301.A31
Vth(max)=1.0V
HPD_HDMI_CON
HDMI_HPD_D
R5407 Do Not Stuff
R5408 100KR2F-L1-GP
AFTP5402 AFTP5403 AFTP5404 AFTP5405 AFTP5406 AFTP5407 AFTP5408 AFTP5409 AFTP5410 AFTP5411 AFTP5412 AFTP5413
5V_HDMI
V1P8_S3
SoC HPD
10k Ω ±1%
100k Ω ±1%
HPD
DP / eDP CONNECTOR
CABLE
Level shift
Vth(GS) = 1V , Ciss < 50pF
1D8V_S5
5V_S5
5V_HDMI
Q5408 HDMI_MOS
[8] PCH_HDMI_CLK
DMN5L06K-7-GP
84.05067.031
2nd = 84.00301.A31
R5421 Do Not Stuff
PCH_HDMI_CLK_Q
Q5406 Do Not Stuff
Vth(max)=2.5V
DDC_CLK_HDMI
2ND = 84.2N702.031
3rd = 084.27002.0B31
R5415 0R2J-2-GP
HDMI_MOS
Q5407
[8] PCH_HDMI_DATA
R5419 Do Not Stuff
PCH_HDMI_DATA_Q
Q5405 Do Not Stuff
DDC_DATA_HDMI
R5416 0R2J-2-GP
5V_HDMI
RN5403 SRN2K2J-1-GP
CRB 2.2k
DDC_DATA_HDMI
DDC_CLK_HDMI
Do Not Stuff C3652
1D8V_S5
U5401 HDMI_9406
SDA_B GND VCCA SDA_A SCL_B VCCB OE SCL_A
[8] PCH_HDMI_DATA
PCH_HDMI_CLK [8]
SMB_HDMI_OE
Do Not Stuff
2nd = 73.00102.007
Internal10-kΩ Pullup Resistor on Each Port and Option to Add External Pullup Resistor if Required
Do Not Stuff C3653
1D8V_S0
R5420 Do Not Stuff

NOTE: It is highly recommended a passgate N-MOSFET device is selected that has Gate Threshold Voltage <=1.5V.
NOTE: The HPD PU resistor tolerance can be relaxed to 5%.

Pin#	Signal	Pin#	Signal
1	TMDS data 2+	11	TMDS clock shield
2	TMDS data 2 shield	12	TMDS clock-
3	TMDS data 2-	13	CEC
4	TMDS data 1+	14	No connected
5	TMDS data 1 shield	15	DDC clock
6	TMDS data 1-	16	DDC data
7	TMDS data 0+	17	Ground
8	TMDS data 0 shield	18	+5V power
9	TMDS data 0-	19	Hot plug detect
10	TMDS clock+		

4.2.9 Hot Plug Detect Signal (HPD)

The ground reference for the Hot Plug Detect signal is the DDC/CEC Ground pin.

Table 4-38 Required Output Characteristics of Hot Plug Detect Signal

Item	Value
High voltage level (Sink)	Minimum 2.4 Volts, Maximum 5.3 Volts
Low voltage level (Sink)	Minimum 0 Volts, Maximum 0.4 Volts
Output resistance	1000 ohms ±20%

Table 4-39 Required Detection Levels for Hot Plug Detect Signal

Item	Value
High voltage level (Source)	Minimum 2.0 Volts, Maximum 5.3 Volts
Low voltage level (Source)	Minimum 0 Volts, Maximum 0.8 Volts

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Title: **HDMI Level Shifter/Connector**

Size: A3 | Document Number: Plano 11.6" UMA | Rev: A00

Date: Wednesday, April 22, 2015 | Sheet 54 of 110

(Blanking)

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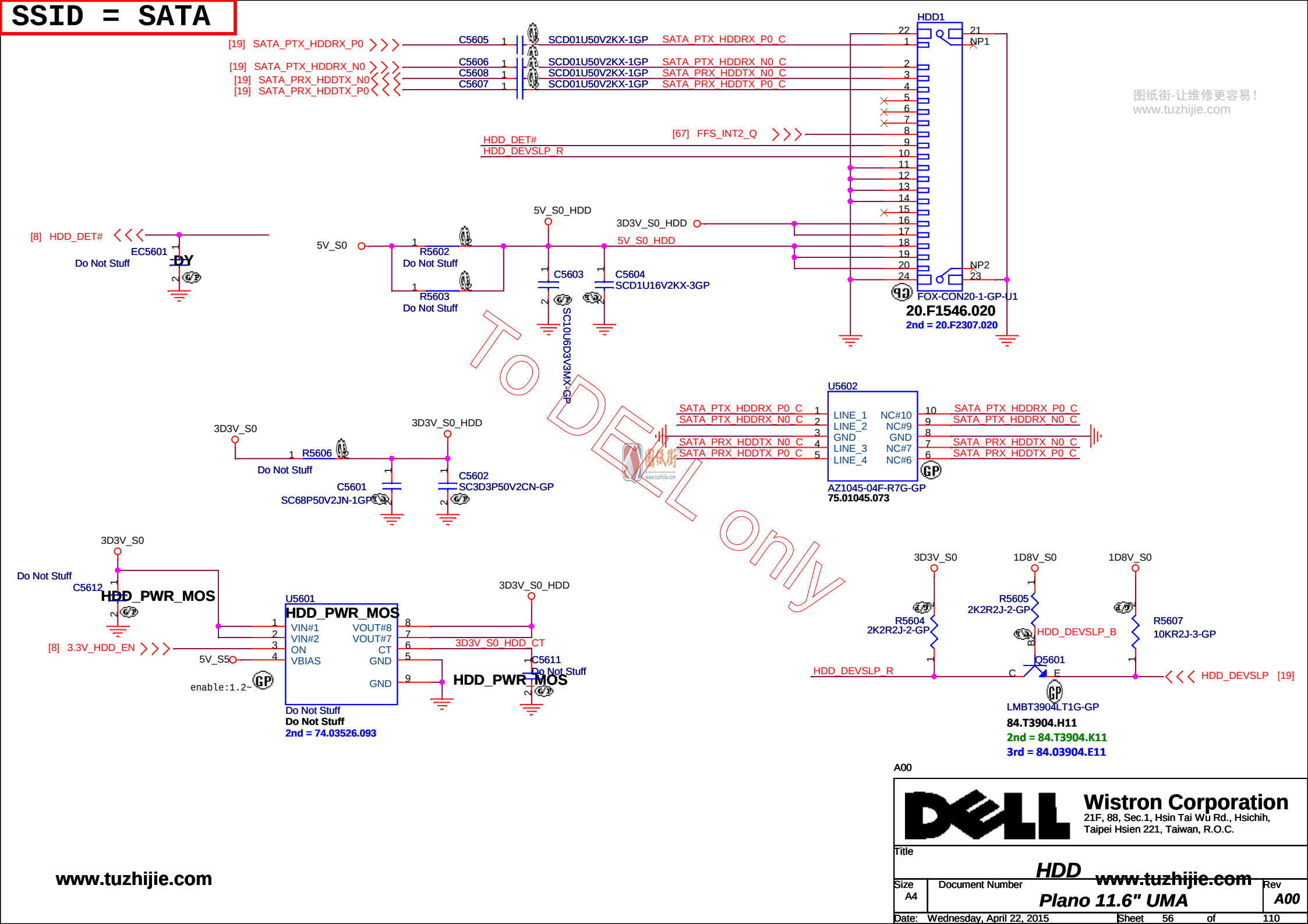
Title: **HDMI Level Shifter/Connector**

Size	Document Number	Rev
A	Plano 11.6" UMA	A00

Date: Friday, March 27, 2015 Sheet 55 of 110

SSID = SATA



A00

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Title	HDD	
Size A4	Document Number Plano 11.6" UMA	Rev A00
Date: Wednesday, April 22, 2015	Sheet 56 of 110	

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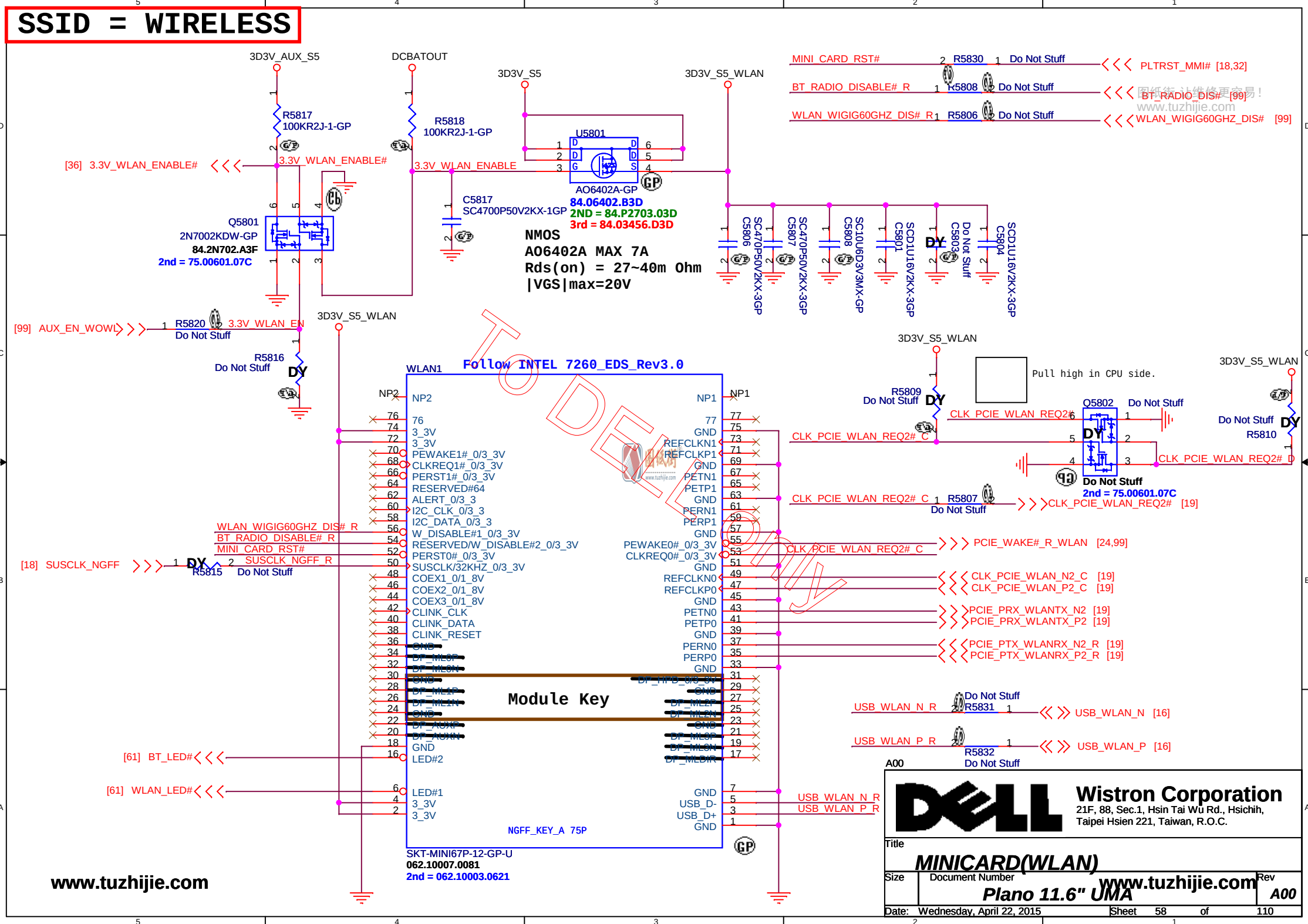
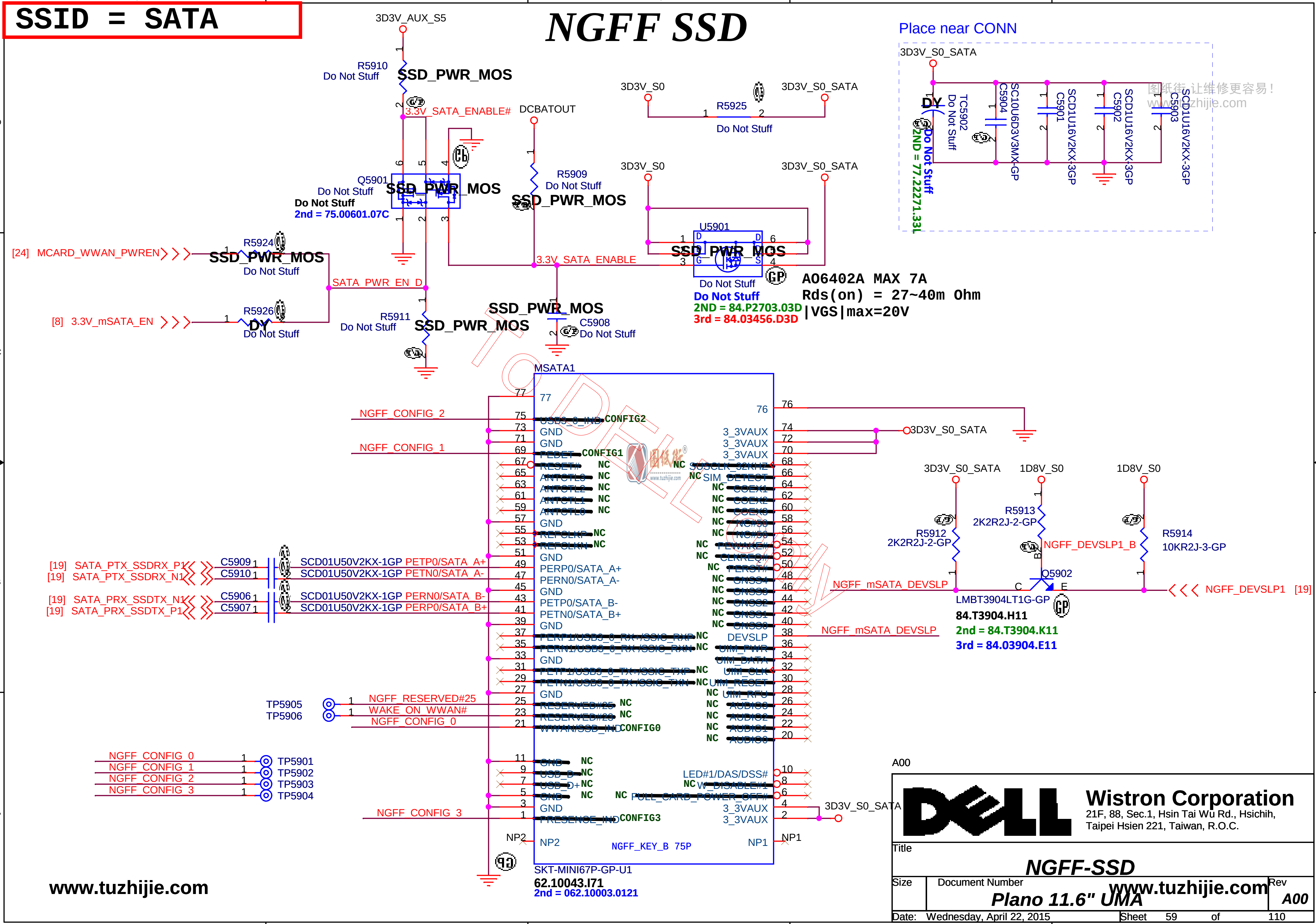
Title: *Reserved*

Size	Document Number	Rev
A4	*Plano 11.6" UMA*	*A00*

Date: Friday, March 27, 2015 Sheet 57 of 110

SSID = WIRELESS





SSID = SATA
NGFF SSD
Place near CONN
3D3V_AUX_S5
R5910
Do Not Stuff
SSD_PWR_MOS
3.3V_SATA_ENABLE#
DCBATOUT
3D3V_S0
3D3V_S0_SATA
R5925
Do Not Stuff
Q5901
Do Not Stuff
2nd = 75.00601.07C
R5909
Do Not Stuff
U5901
AO6402A MAX 7A
Rds(on) = 27~40m Ohm
|VGS|max=20V
Do Not Stuff
2ND = 84.P2703.03D
3rd = 84.03456.D3D
TC5902
Do Not Stuff
2ND = 77.22271.33L
C5904
SC10U6D3V3MX-GP
C5901
SCD1U16V2KX-3GP
C5902
SCD1U16V2KX-3GP
C5903
SCD1U16V2KX-3GP
[24] MCARD_WWAN_PWREN
R5924
SATA_PWR_EN_D
3.3V_SATA_ENABLE
[8] 3.3V_mSATA_EN
R5926
DY
R5911
C5908
Do Not Stuff
MSATA1
NGFF_CONFIG_2
NGFF_CONFIG_1
USB3_0_IND CONFIG2
PEDET CONFIG1
RESET#
ANTCTL3
ANTCTL2
ANTCTL1
ANTCTL0
GND
REFCLKP
REFCLKN
PERP0/SATA_A+
PERN0/SATA_A-
PETP0/SATA_B-
PETN0/SATA_B+
DEVSLP
3_3VAUX
SUSCLK_32KHZ
SIM_DETECT
COEX1
COEX2
COEX3
PEWAKE#
CLKREQ#
PERST#
GNSS4
GNSS3
GNSS2
GNSS1
GNSS0
UIM_PWR
UIM_DATA
UIM_CLK
UIM_RESET
UIM_RFU
AUDIO3
AUDIO2
AUDIO1
AUDIO0
[19] SATA_PTX_SSDRX_P1
[19] SATA_PTX_SSDRX_N1
[19] SATA_PRX_SSDTX_N1
[19] SATA_PRX_SSDTX_P1
C5909
C5910
C5906
C5907
SCD01U50V2KX-1GP PETP0/SATA_A+
SCD01U50V2KX-1GP PETN0/SATA_A-
SCD01U50V2KX-1GP PERN0/SATA_B-
SCD01U50V2KX-1GP PERP0/SATA_B+
PERP1/USB3_0_RX+/SSIC_RXP
PERN1/USB3_0_RX-/SSIC_RXN
PETP1/USB3_0_TX+/SSIC_TXP
PETN1/USB3_0_TX-/SSIC_TXN
RESERVED#25
RESERVED#23
WWAN/SSD_IND CONFIG0
TP5905
TP5906
NGFF_RESERVED#25
WAKE_ON_WWAN#
NGFF_CONFIG_0
NGFF_CONFIG_0
NGFF_CONFIG_1
NGFF_CONFIG_2
NGFF_CONFIG_3
TP5901
TP5902
TP5903
TP5904
USB_D-
USB_D+
LED#1/DAS/DSS#
W_DISABLE#1
FULL_CARD_POWER_OFF#
PRESENCE_IND CONFIG3
NGFF_CONFIG_3
NP1
NP2
NGFF_KEY_B 75P
SKT-MINI67P-GP-U1
62.10043.I71
2nd = 062.10003.0121
1D8V_S0
R5913
2K2R2J-2-GP
R5912
2K2R2J-2-GP
R5914
10KR2J-3-GP
NGFF_DEVSLP1_B
Q5902
NGFF_mSATA_DEVSLP
NGFF_DEVSLP1 [19]
LMBT3904LT1G-GP
84.T3904.H11
2nd = 84.T3904.K11
3rd = 84.03904.E11
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Size
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SSID =WIRELESS

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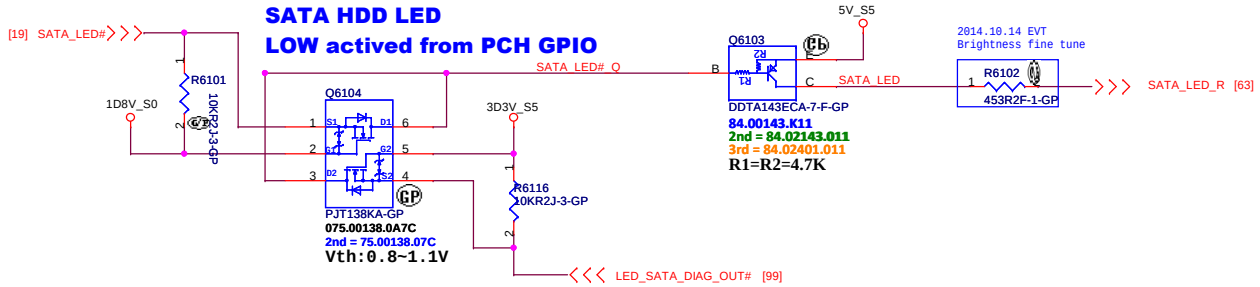
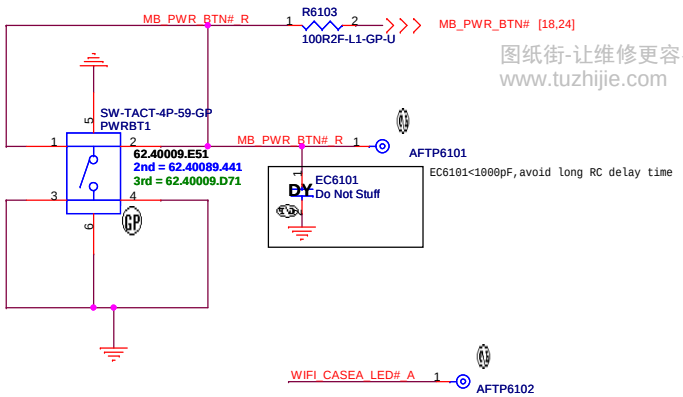
SSID = User.Interface

SATA HDD LED
LOW actived from PCH GPIO

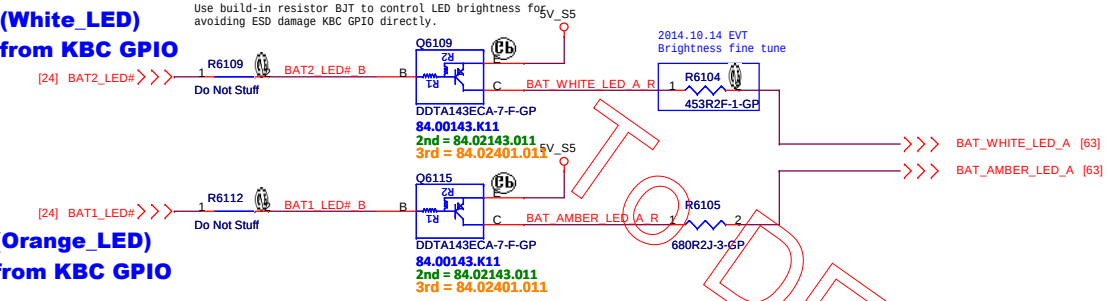


POWER BUTTON

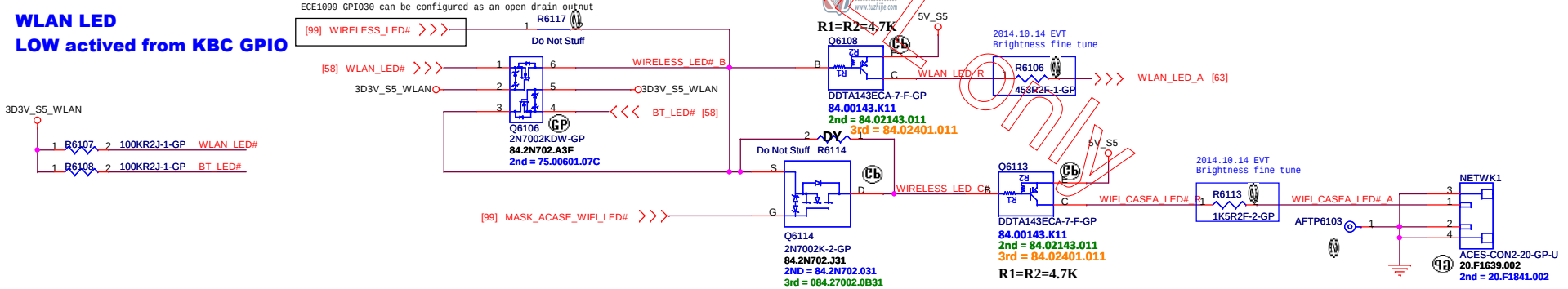


Battery LED2(White_LED)
LOW actived from KBC GPIO

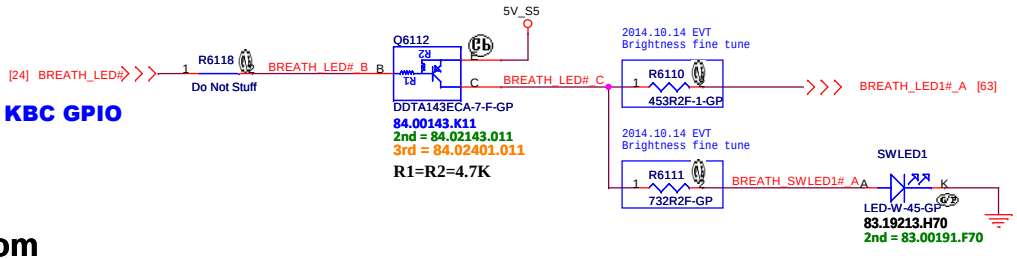
Battery LED1(Orange_LED)
LOW actived from KBC GPIO



WLAN LED
LOW actived from KBC GPIO



Power LED
LOW actived from KBC GPIO



POWER BUTTON LED

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Title: LED

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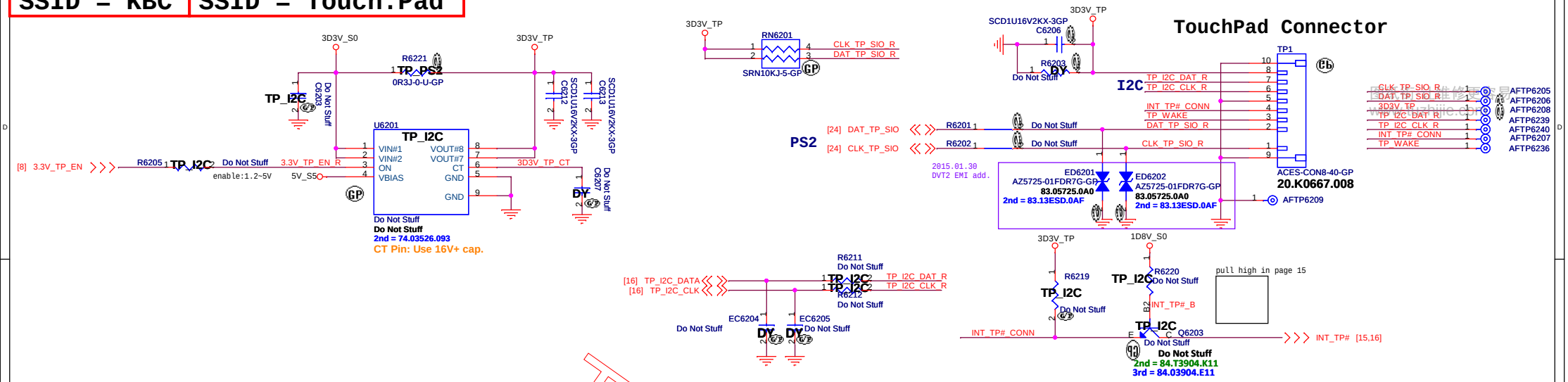
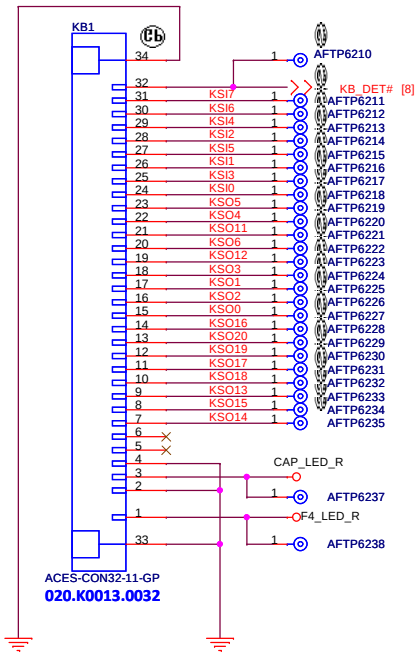
SSID = KBC | **SSID = Touch.Pad**

TouchPad Connector

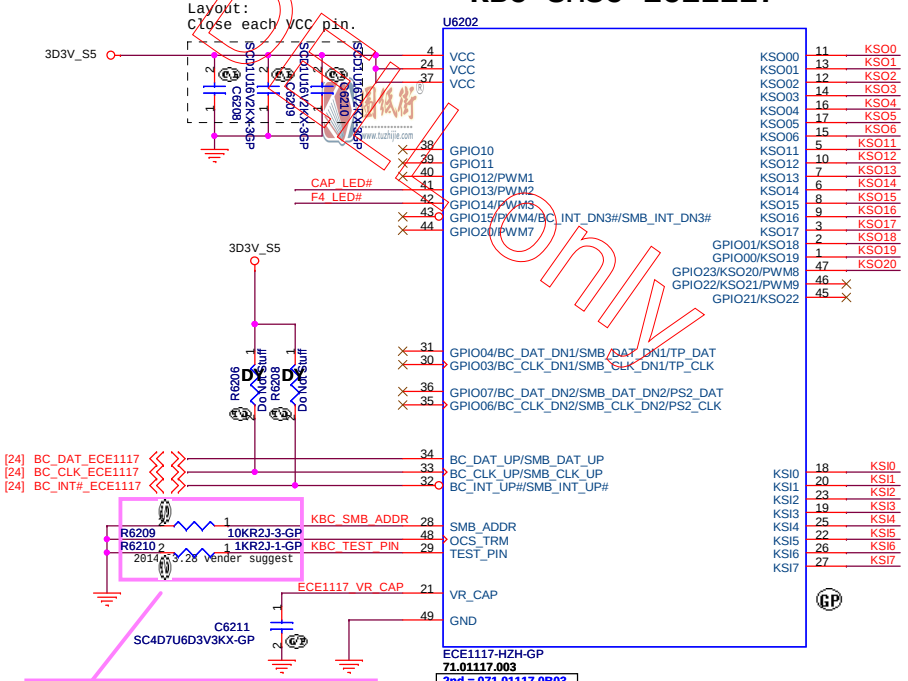


Internal KeyBoard Connector



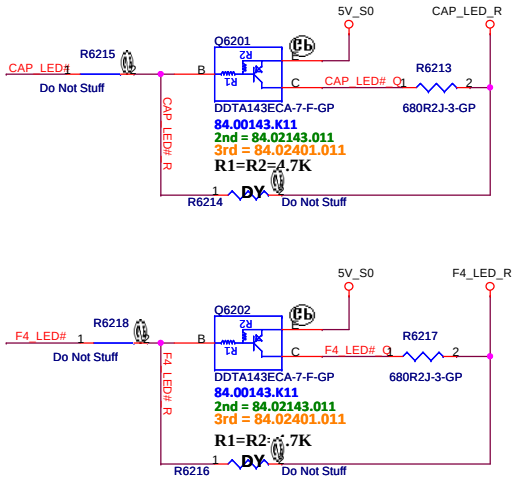
PIN#	SIGNAL
1	Diagnostic(LOOP to Pin 31)
2	KSI[7] = KBD S8
3	KSI[6] = KBD S7
4	KSI[4] = KBD S5
5	KSI[2] = KBD S3
6	KSI[5] = KBD S6
7	KSI[1] = KBD S2
8	KSI[3] = KBD S4
9	KSI[0] = KBD S1
10	KSO[5] = KBD D6
11	KSO[4] = KBD D5
12	KSO[11] = KBD D8
13	KSO[6] = KBD D7
14	KSO[12] = KBD D9
15	KSO[3] = KBD D4
16	KSO[1] = KBD D2
17	KSO[2] = KBD D3
18	KSO[0] = KBD D1
19	KSO[16] = KBD D13
20	KSO[20] = KBD D17
21	KSO[19] = KBD D16
22	KSO[17] = KBD D14
23	KSO[18] = KBD D15
24	KSO[13] = KBD D10
25	KSO[15] = KBD D12
26	KSO[14] = KBD D11
27	NC
28	NC
29	GND
30	CapsLK_LED
31	GND
32	F4_LED

KBC SMSC ECE1117



Pin28 SMBus Address select strap pin.
10K pull ground=0111 000b
10K pull VCC=0111 001b

Pin29 has a weak internal pull-down



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Title: Key Board/Touch Pad

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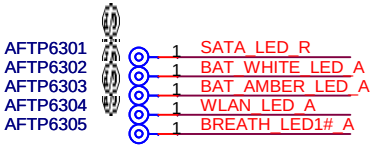

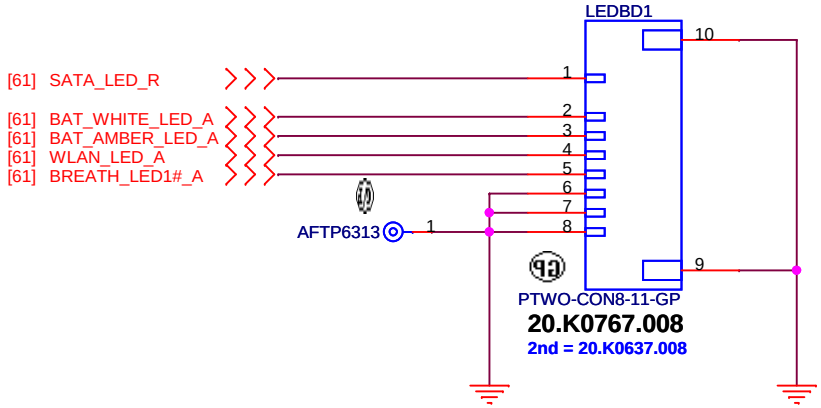

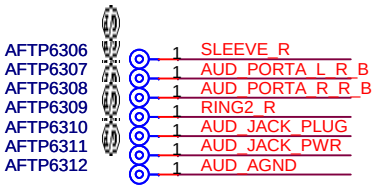

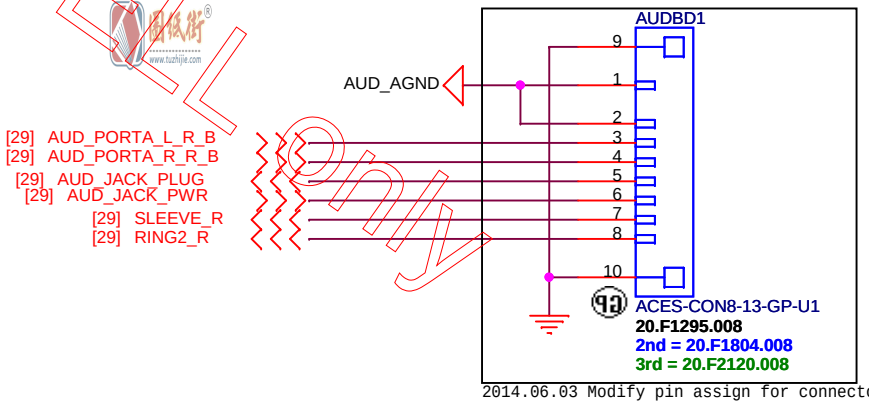

2014.06.03 Modify pin assign for connector change

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Title: **IO CONN**

Size	Document Number	Rev
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Title

Hall Sensor

Size	Document Number	Rev
	Plano 11.6" UMA	***A00***

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SSID = DEBUG PORT

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Title: Debug connector

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Title: SENSOR

Size: A3 | Document Number: Plano 11.6" UMA | Rev: A00

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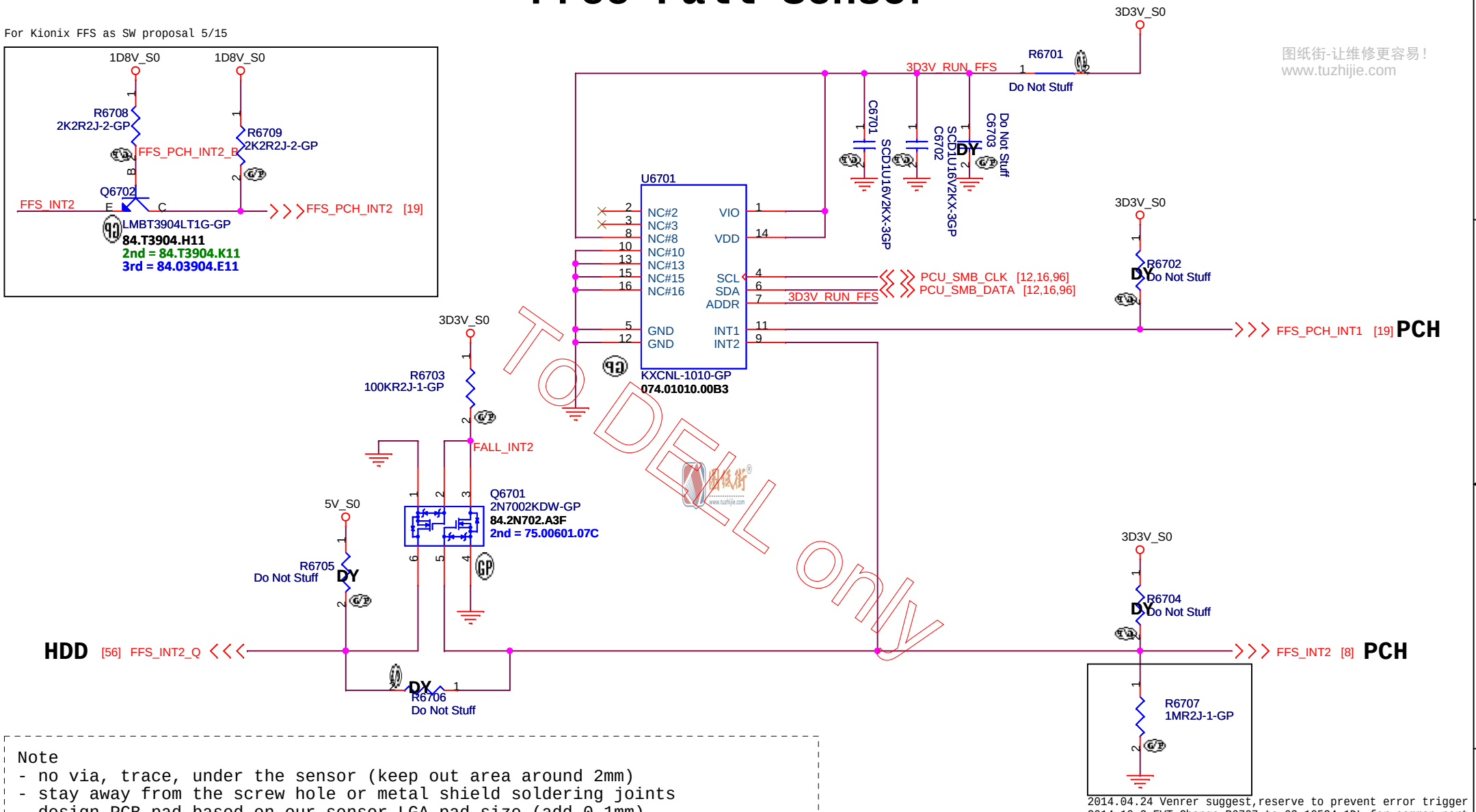
SSID = User.interface

Free Fall Sensor

For Kionix FFS as SW proposal 5/15



Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

2014.04.24 Venrer suggest,reserve to prevent error trigger
2014.10.2 EVT Change R6707 to 63.10534.1DL for common part

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Title: Free Fall Sensor

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A4	Plano 11.6" UMA	A00

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Title: *Thunderbolt (1/5)*

Size: A3 | Document Number: *Plano 11.6" UMA* | Rev: *A00*

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Title

Thunderbolt (2/5)

Size	Document Number	Rev
A	*Plano 11.6" UMA*	A00

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Title: ***Thunderbolt (3/5)***

Size	Document Number	Rev
A	***Plano 11.6" UMA***	A00

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Title: *Thunderbolt (4/5)*

Size	Document Number	Rev
A	*Plano 11.6" UMA*	A00

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Title: ***Thunderbolt (5/5)***

Size	Document Number	Rev
A	***Plano 11.6" UMA***	A00

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Title

GPU (1/5) PEG

Size	Document Number	Rev
A	Plano 11.6" UMA	A00

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Title: ***GPU (2/5) DIGITAL***

Size	Document Number	Rev
A	***Plano 11.6" UMA***	A00

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Title

GPU (3/5) VRAM

Size	Document Number	Rev
A	*Plano 11.6" UMA*	A00

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Title

GPU (4/5) GPIO

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A	*Plano 11.6" UMA*	A00

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Title: ***GPU (5/5) PWR/GND***

Size	Document Number	Rev
A	***Plano 11.6" UMA***	A00

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Title: ***VRAM1,2 (1/4)***

Size	Document Number	Rev
A	***Plano 11.6" UMA***	A00

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Title: ***VRAM3,4 (2/4)***

Size	Document Number	Rev
A	***Plano 11.6" UMA***	A00

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Title: ***VRAM5,6 (3/4)***

Size	Document Number	Rev
A	***Plano 11.6" UMA***	A00

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Title: ***VRAM7,8 (4/4)***

Size	Document Number	Rev
A	***Plano 11.6" UMA***	A00

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Title: *VGA CORE*

Size	Document Number	Rev
A	*Plano 11.6" UMA*	A00

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Title: *DISCRETE VGAPOWER*

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A	*Plano 11.6" UMA*	A00

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Title

Switchable GFXLCD

Size	Document Number	Rev
A	Plano 11.6" UMA	A00

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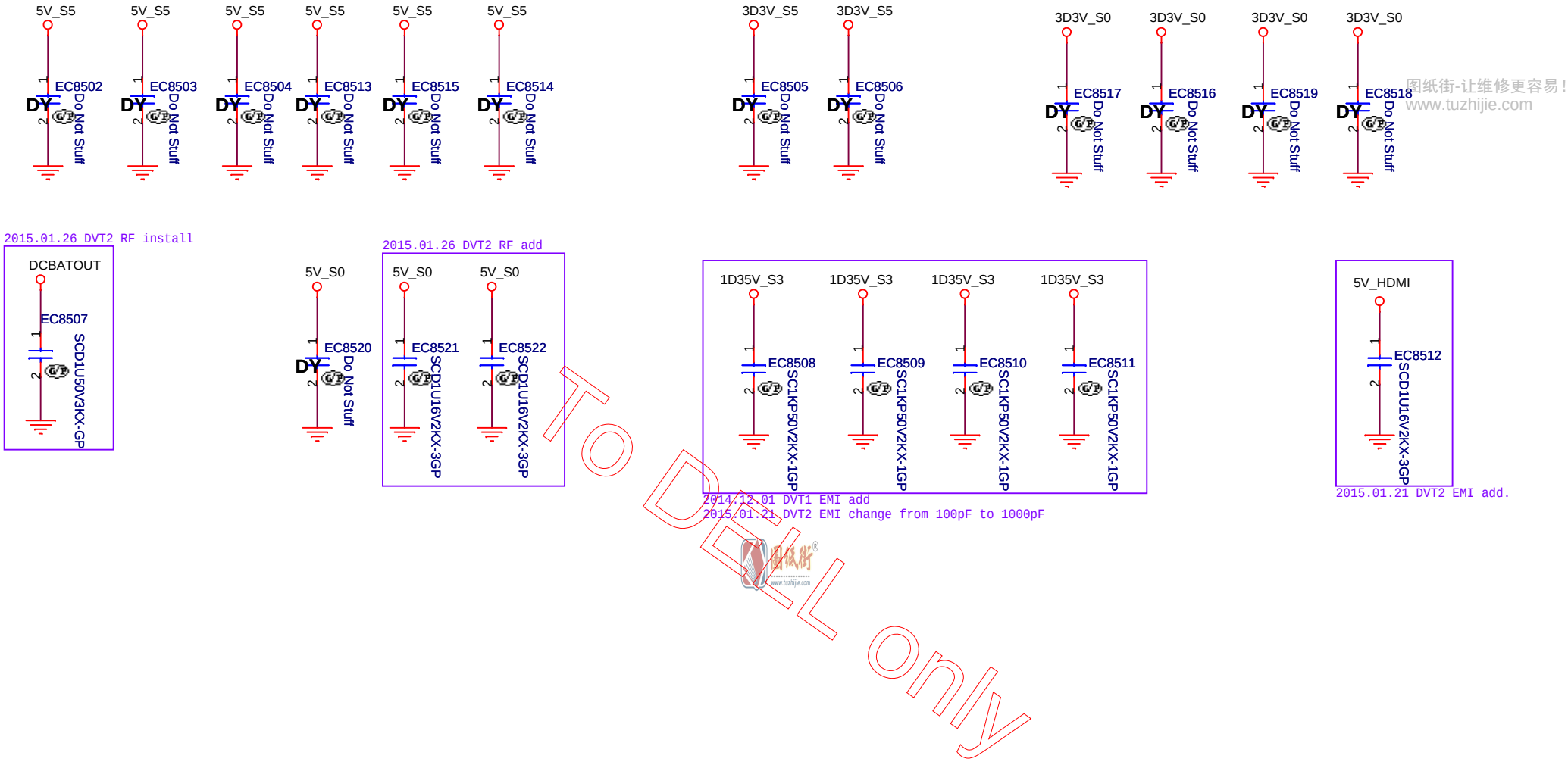

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Title: ***UNUSED PARTS/EMI Capacitors***

Size	Document Number	Rev
A4	***Plano 11.6" UMA*** www.tuzhijie.com	***A00***

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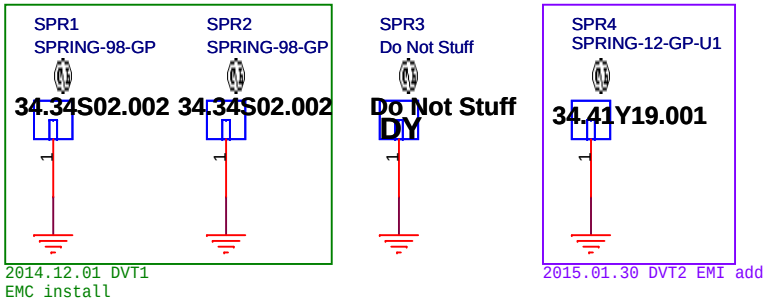

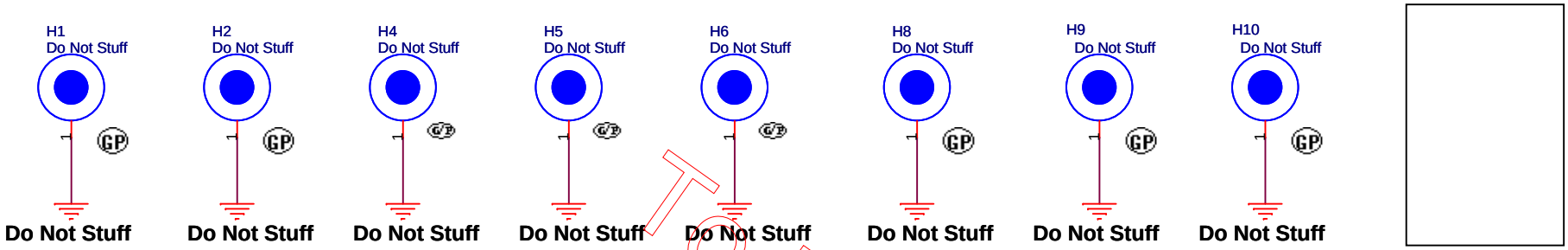

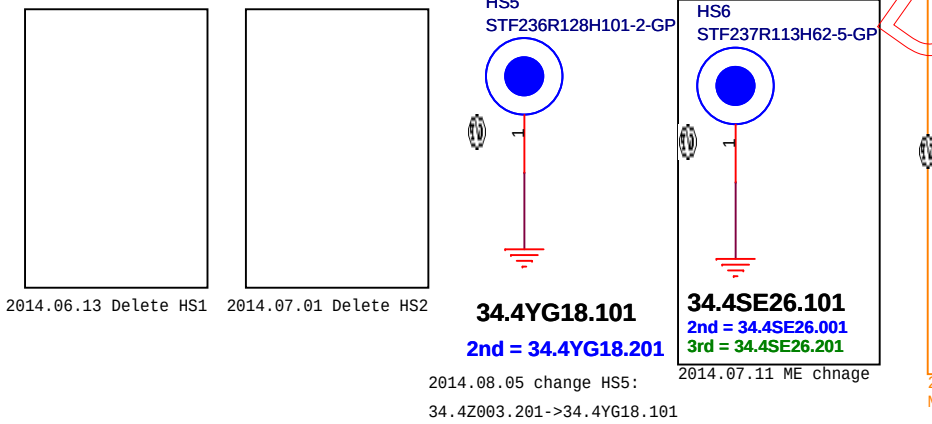

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Title
UNUSED PARTS/EMI Capacitors

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SSID = USH

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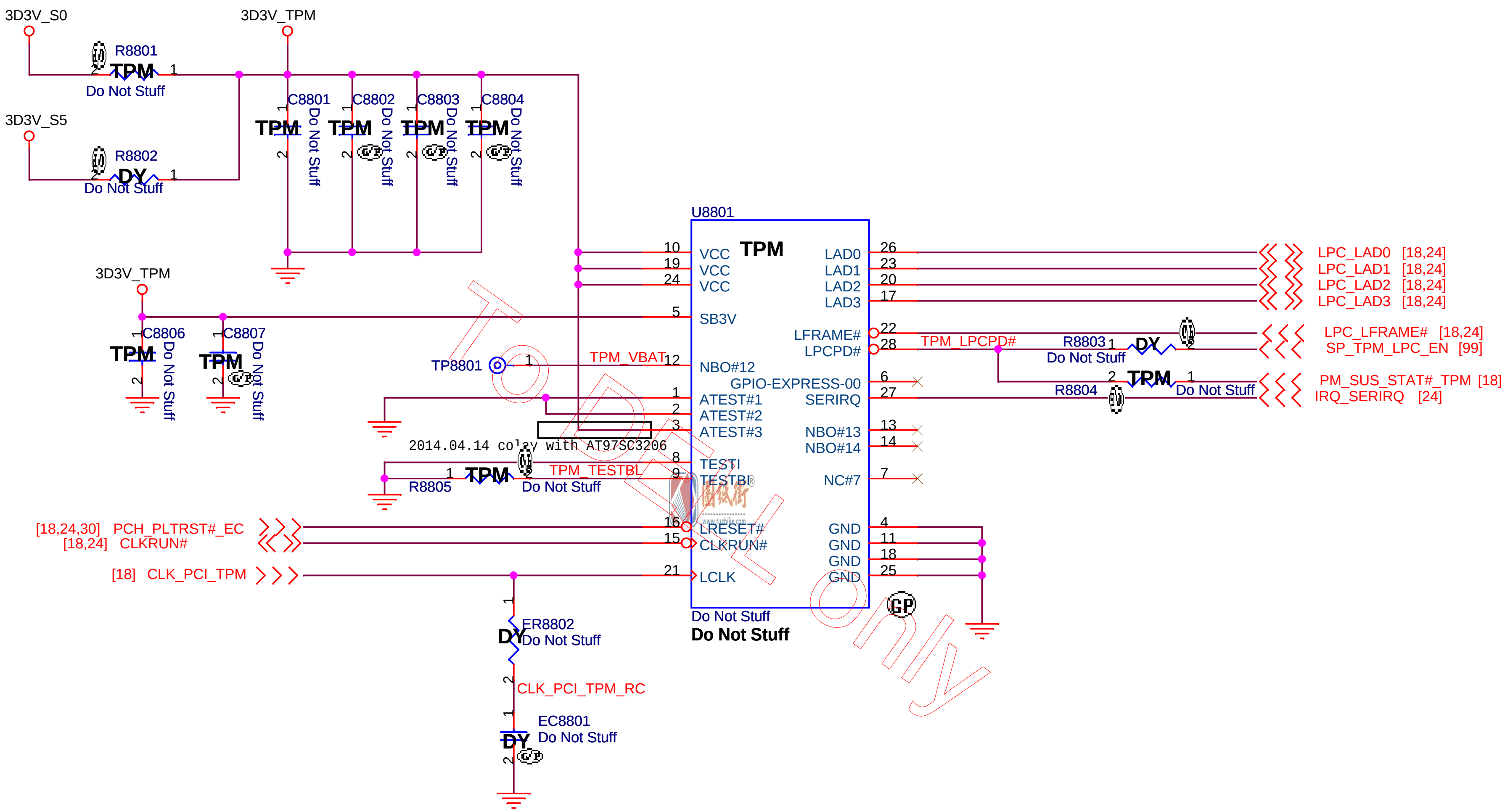
Title: *USH Board Connector*

Size	Document Number	Rev
A4	Plano 11.6" UMA	A00

Date: Friday, March 27, 2015 Sheet 87 of 110

SSID = TPM



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Title: **TPM**

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Title: ***Finger Print***

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A	***Plano 11.6" UMA***	A00

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Title: ***NFC Connector***

Size	Document Number	Rev
A4	***Plano 11.6" UMA***	***A00***

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Title: ***Smart Card***

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Title: *Reserved*

Size	Document Number	Rev
A	*Plano 11.6" UMA*	A00

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SSID = Docking

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Title: DOCKING

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Title

Reserved

Plano 11.6" UMA

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Title: LAN SW

Size	Document Number	Rev
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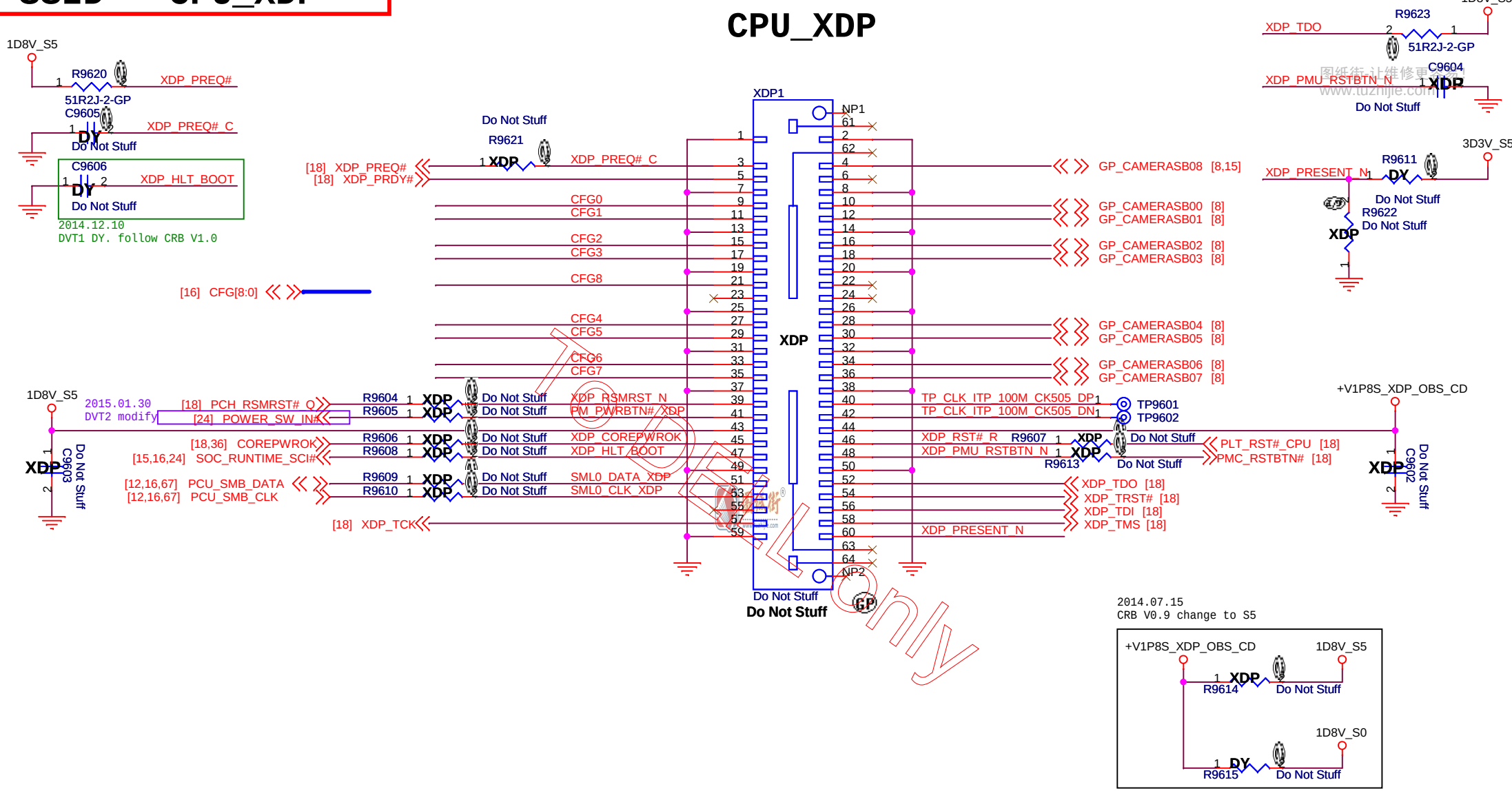
SSID = CPU_XDP

CPU_XDP



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Title: CPU_XDP		
Size: A4	Document Number: Plano 11.6" UMA	Rev: A00
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Title: USB2.0 HUB

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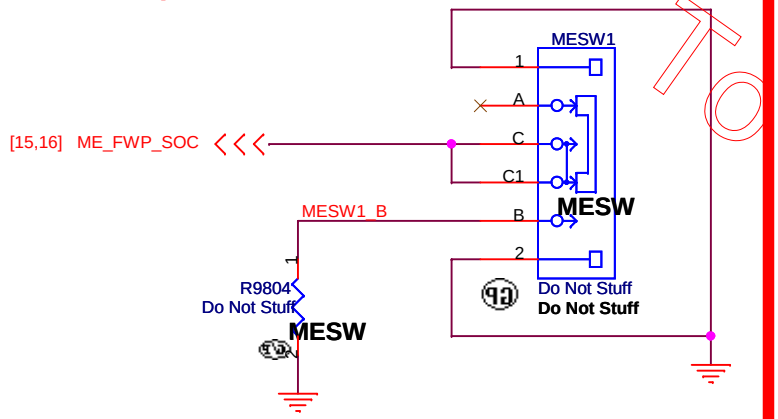
SSID = User.Interface

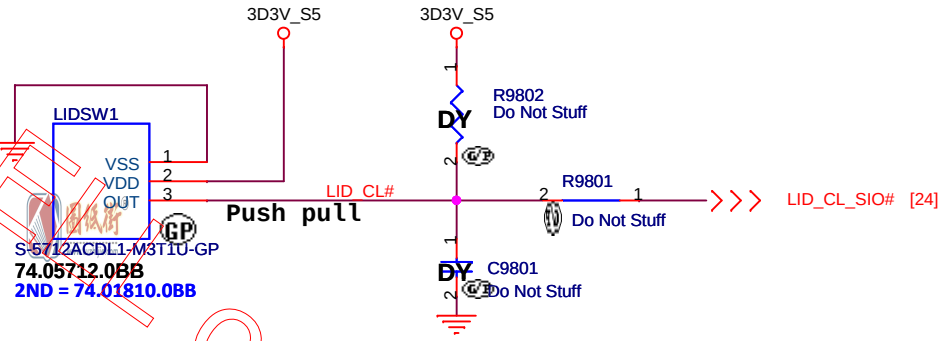
Firmware SW

Default setting:pull high
DY for production



	A	B
ME_FWP_SOC	High	Low
	Normal Operation (Default)	Override

Lid Close:Active Low



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Title: ***Lid Close***

Size	Document Number	Rev
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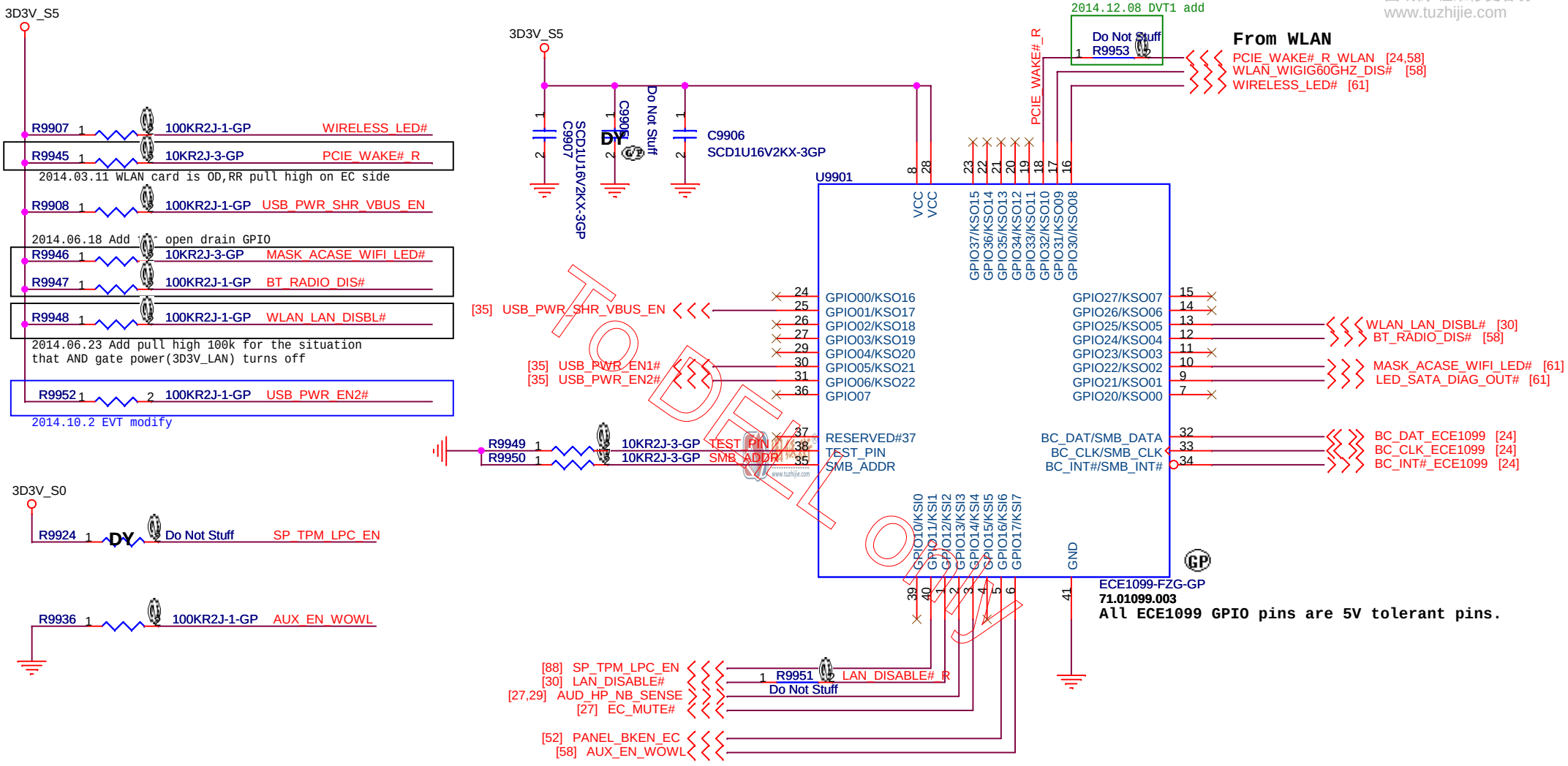
SSID = SIO



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Title: SIO - ECE1099

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Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap overdrive	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, iCLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass

CHV Straps [CRB] -- strap detect @ RSMRST# assertion

Purpose	CHV Pin Name (refer CHV symbol PIN)	PU/PD (internal - Week)	Options	Default State on board?
DSI Display Detected	GPIO_SUS3	PD	1 - DSI detect, 0 - Disable	Low
DFX Boot Halt Strap & VISA Early POSM	GPIO_SUS6	PU	1 - normal, 0 - Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	1- Normal, 0 - Sus Debug enable	High

USB2.0 MCP Side

Pair	Device
0	USB port 1 (usb charger)
1	USB port 2
2	WLAN (BT)
3	Touch Panel
4	CAMERA

USH Side

Pair	Device
0	NA
1	NA

USB HUB Side

Pair	Device
1	NA
2	NA
3	NA
4	NA

USB3.0 MCP Side

Pair	Device
1	USB port 1
2	USB port 2
3	N/A
4	N/A

PCIE Table

PCIE	
Lane	Device
1	NA
2	Card Reader
3	WLAN
4	LOM

SATA Table

SATA	
Pair	Device
0	HDD
1	NGFF SSD

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Title: Table of Content

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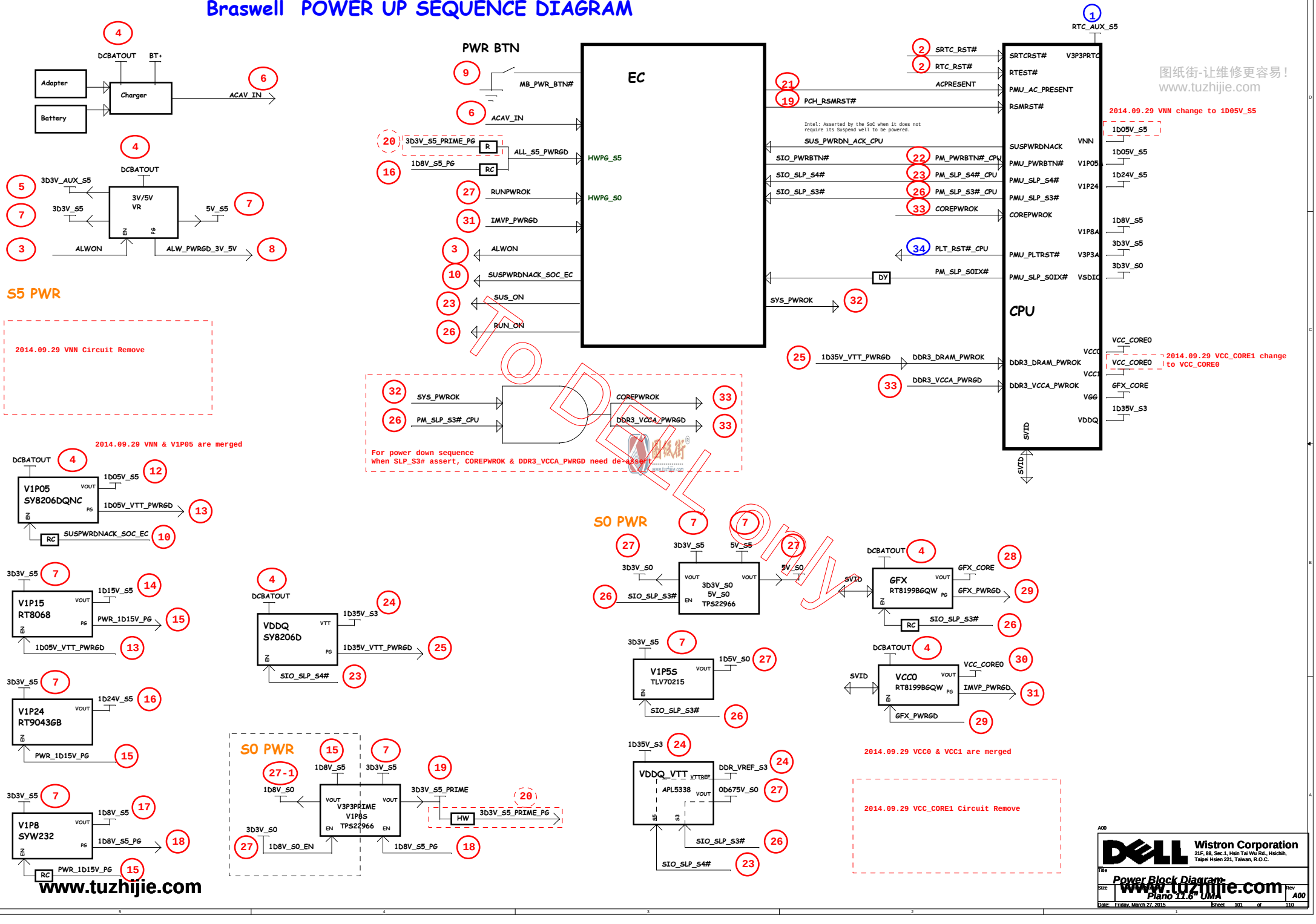
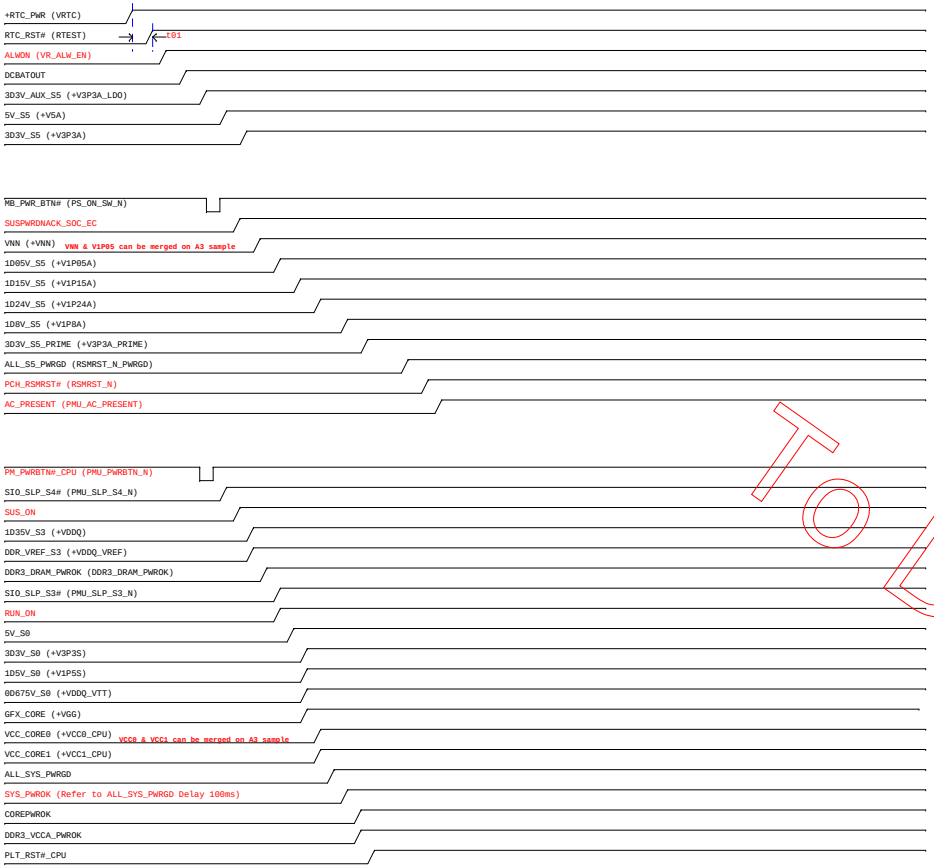
Braswell POWER UP SEQUENCE DIAGRAM



Intel-Power Up Sequence

(AC mode)

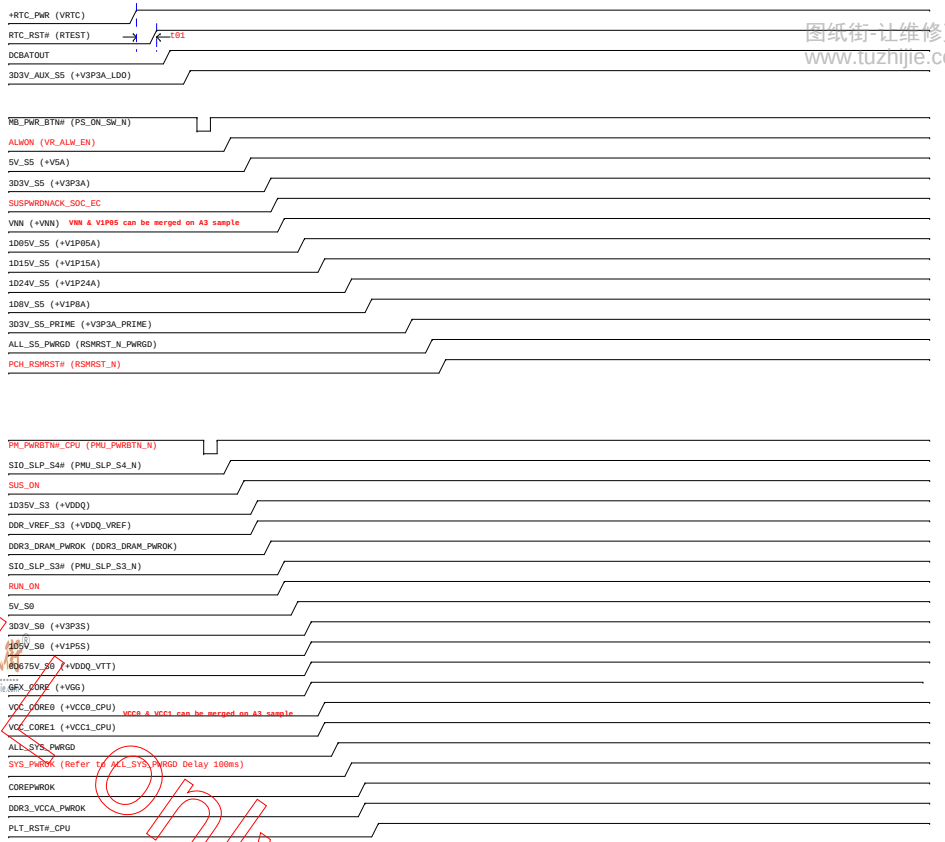
Red word : KBC GPIO



Intel-Power Up Sequence

(DC mode)

Red word : KBC GPIO



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Power Up Sequence		
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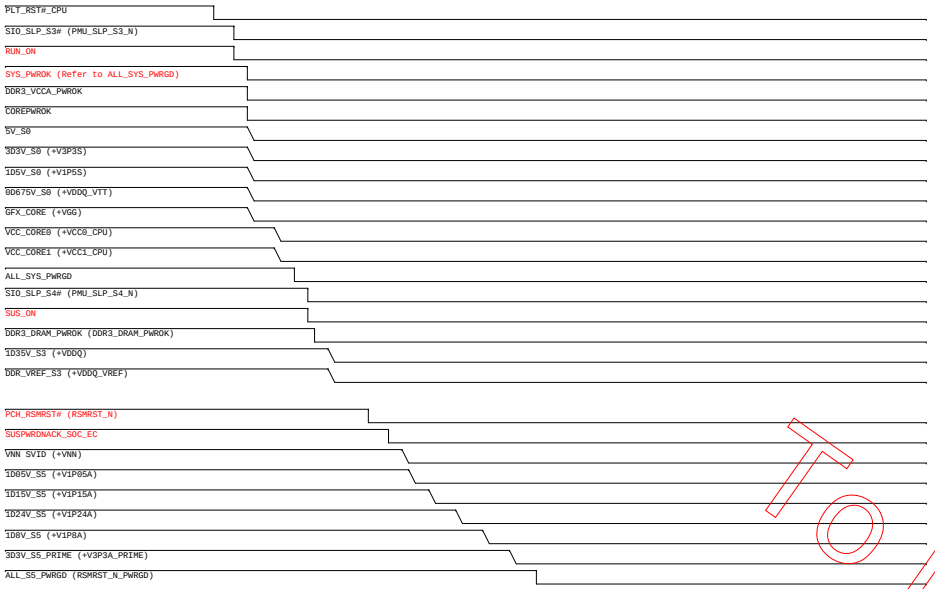
Intel-Power Down Sequence

(AC mode)

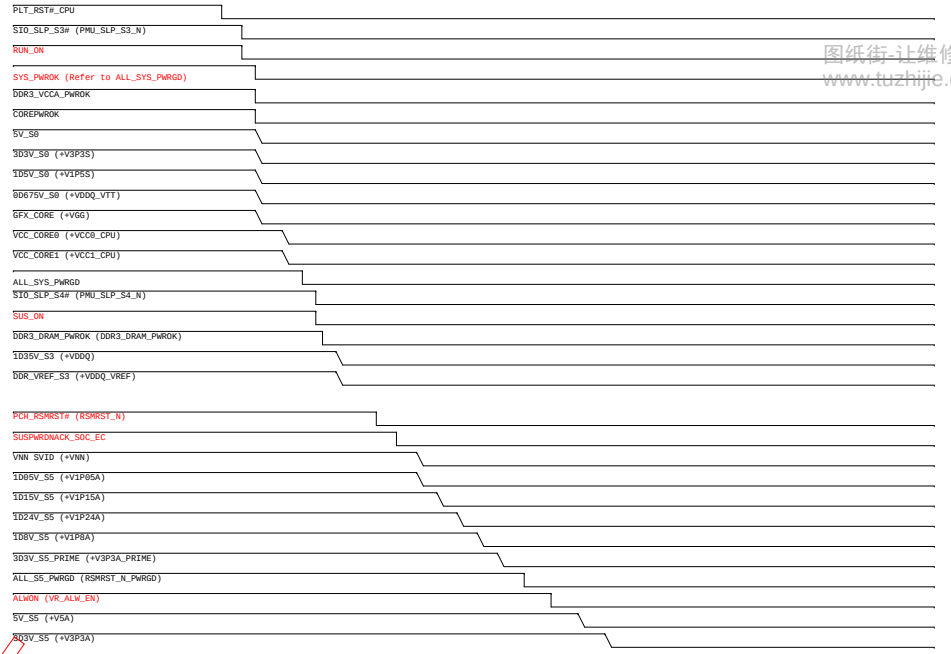
Red word : KBC GPIO



Intel-Power Down Sequence

(DC mode)

Red word : KBC GPIO



A00		
Wistron Corporation		
Title: Power Down Sequence		
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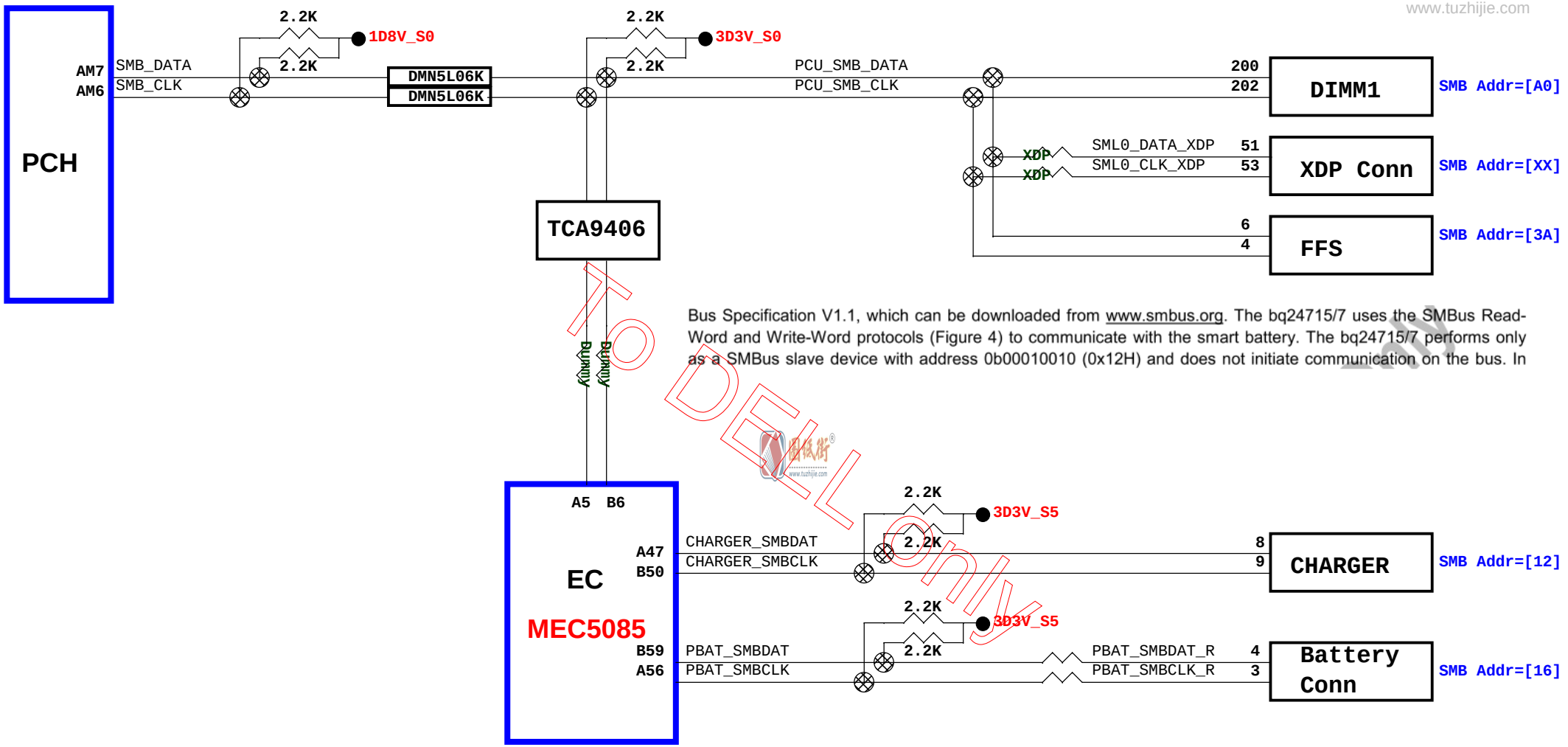

Bus Specification V1.1, which can be downloaded from www.smbus.org. The bq24715/7 uses the SMBus Read-Word and Write-Word protocols (Figure 4) to communicate with the smart battery. The bq24715/7 performs only as a SMBus slave device with address 0b00010010 (0x12H) and does not initiate communication on the bus. In

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Title: SMBUS Block Diagram

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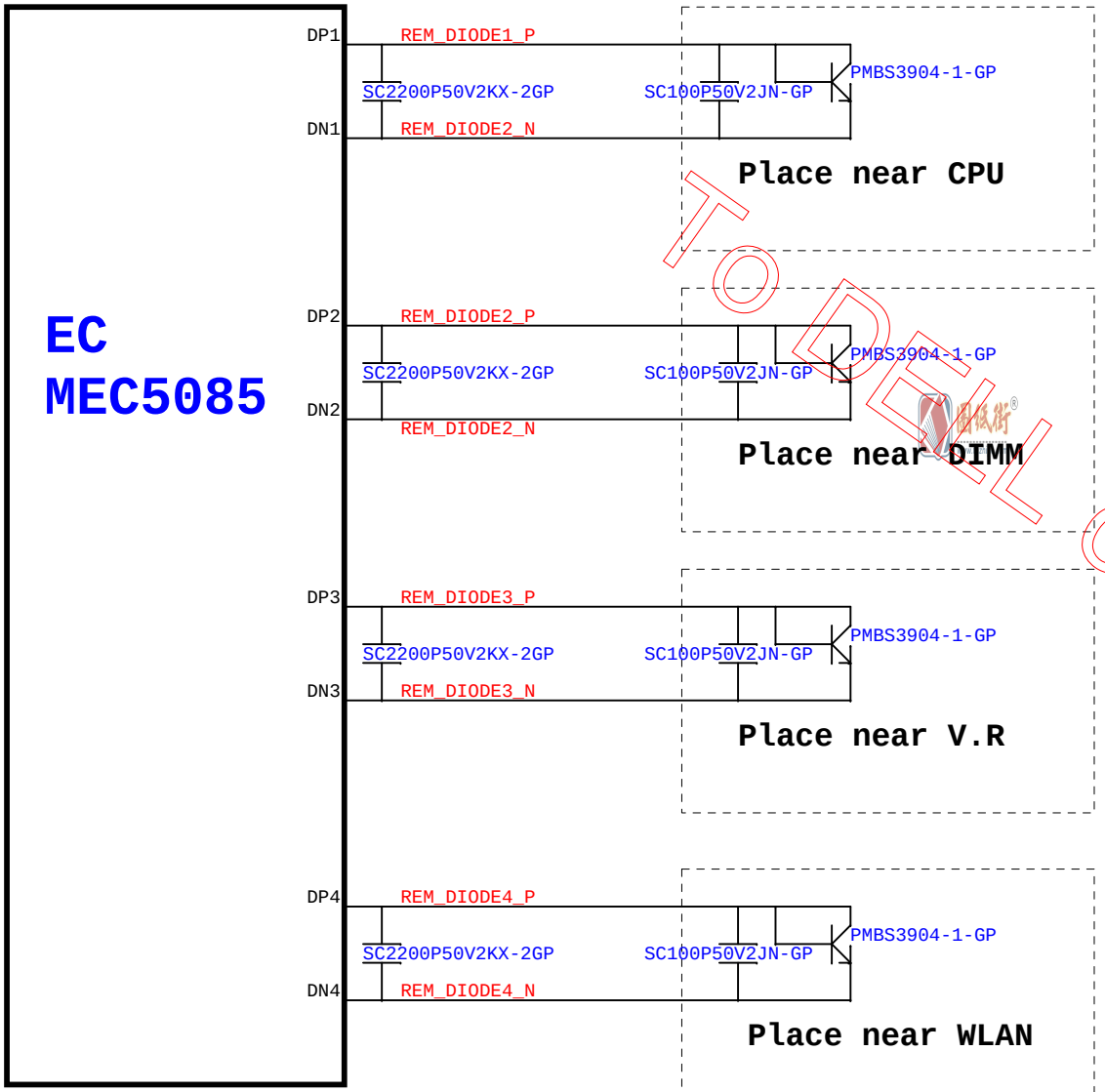
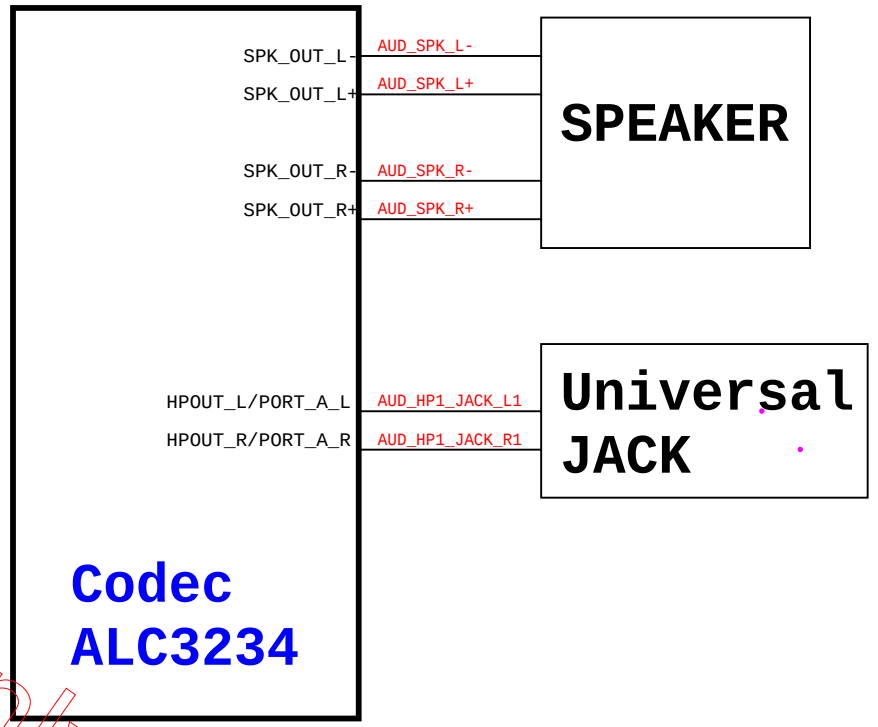
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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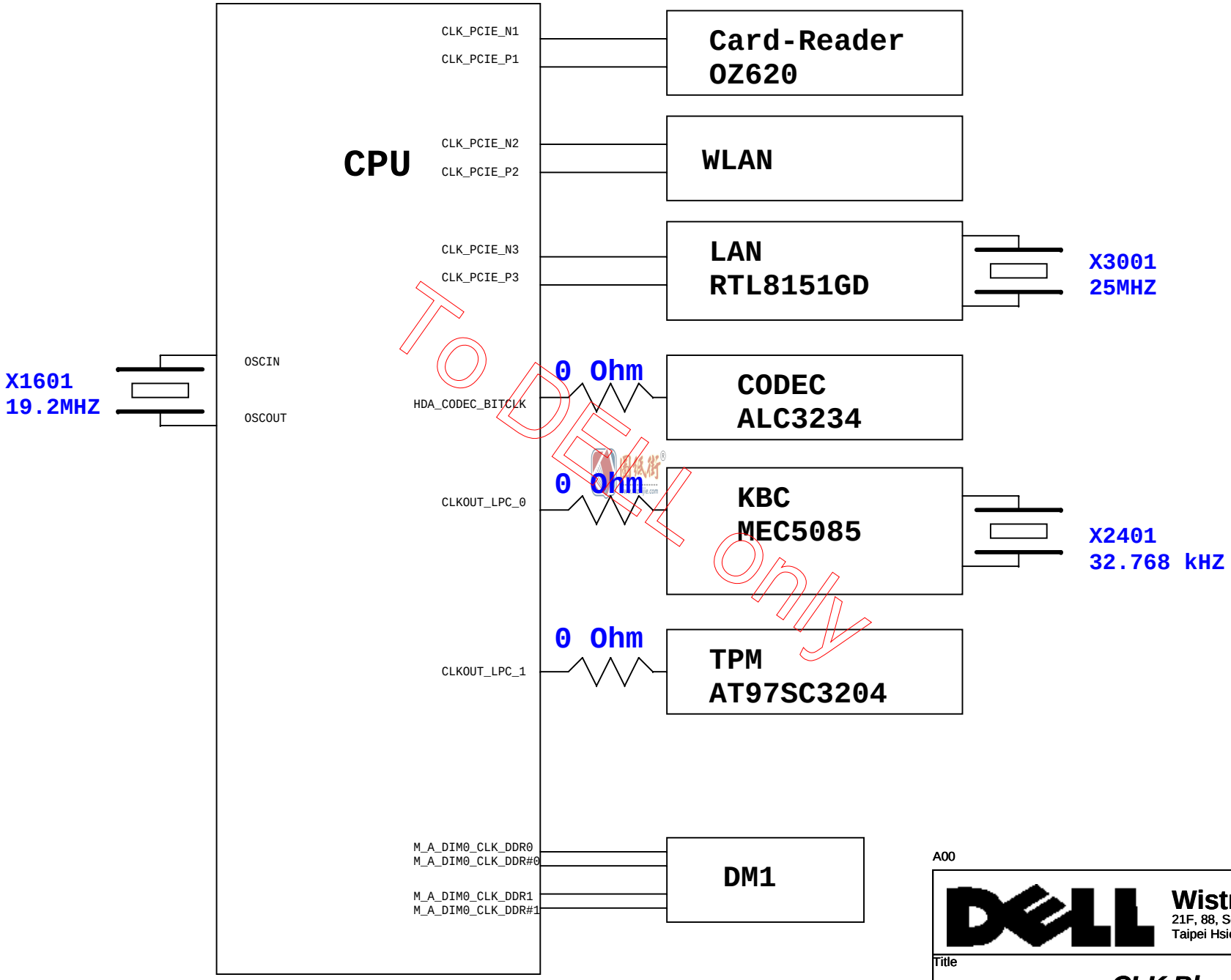
SSID = User.Interface



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Title: CLK Block

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	101	2014.08.12		Modify power sequence	ALWON->(3), DCBATOUT->(4), 3D3V_AUX_S5->(5),ACAV_IN->(6)	
2	102	2014.08.12		Modify AC mode power sequence	ALWON->(3), DCBATOUT->(4), 3D3V_AUX_S5->(5)	
3	102,103	2014.08.12		Modify Signal name	IMVP_PWRGD modifies to ALL_SYS_PWRGD	
4	102	2014.08.12		Modify Signal name and change to red color	SYS_PWROK(EC_DELAY_ALL_SYS_PWRGD) modifies to SYS_PWROK(Refer to ALL_SYS_PWRGD Delay 100ms)	
5	103	2014.08.12		Modify Signal name and change to red color	SYS_PWROK(EC_DELAY_ALL_SYS_PWRGD) modifies to SYS_PWROK(Refer to ALL_SYS_PWRGD)	
6	103	2014.08.12		Remove Signal	Remove SUS_PWRDN_ACK_CPU	
7	18,46,48	2014.08.13		PDG Rev0.9: Change the value of Resistance	Modify R1823,PR4645,PR4662,PR4669,PR4836,PR4855,PR4875,R819	
8	54	2014.09.25		PDG Rev0.92: Rpd required 470ohm	Modify RN5404, RN5405 from 620ohm to 470ohm	
9 10	7,10,18, 46,47,48, 50,51	2014.09.25		1D05V_S5 merges with VNN, VCC_CORE0 merges with VCC_CORE1	Delete VNN and VCC_CORE1 circuit	
11	9	2014.09.25		CPU1M_B52 connects to GND	CPU1M_B52 connects to GND	
12	9	2014.09.29		CPU1M_B52 can't connect to GND	Modify CPU1M_B52 to NC	
13	54	2014.09.29		RN5404 and RN5405's footprint is too big	Modify RN5404 and RN5405's part number	
14	9	2014.10.02		Save the layout space	Modify R704's footprint from 1206 to 0805	
15	52	2014.10.02	EE	3D3V_CAMERA soft-star fine tune	Change C5228 to 0.1uF and R5227 to 10k	
16	61	2014.10.02	EE & ME	LED brightness fine tune	Change R6113 to 1.5kΩ Change R6102,R6104,R6106,R6110 to 453Ω Change R6113 to 732Ω	
17	99	2014.10.02	EE	USB20_VCCA USB power sequence fine tune	Add pull high R9952	
18	29	2014.10.02	EE	EMC speaker fail	Add EMC solution 680pF for speaker signal, DY first	
19	8	2014.10.03	SW	Avoid camera detect floating	Install R823 for SW request	
20	15	2014.10.03	EE	Internal pull up is too weak	Install R1514 for SMI signal	
21	51	2014.10.03	EE	Modify 1D8V_S5 Power Sequence	Change PR5102 to 0 ohm, Dummy PC5125, Change PR5102.1 netname to 1D05V_VNN_EN	
22	51	2014.10.06	Power,EC	For IPCC fail reserve	Assign A12 to be I_ADP. Connect I_BATT to I_ADP by R2461.R2461:DY	
23	50	2014.10.07	Power	Remove VNN.Modify VSS_VNN_SENSE.	Change netname of PR5039.1 to 1D05V_PWR_FBH	
24	50	2014.10.07	EE	EC code removw ME_SUS_PWRDN_ACK function	DY Q1811,R1858	
25	50	2014.10.07	Power	Follow PDG SVID Design	R1823 DY.	

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Title: Change History-01

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
26	46	2014.10.13	Power	Follow PDG SVID Design	PR4665 stuff. Pin1.NETNAME change to H_CPU_SVIDCLK	EVT
27	48	2014.10.13	Power	Follow PDG SVID Design	PR4843 stuff. Pin1.NETNAME change to H_CPU_SVIDCLK	EVT
28	50	2014.10.13	Power	No VNN power	Delete PT5001	EVT
29	86	2014.10.14	ME	ME change HS7	1st--->34.4WZ01.001 2nd--->34.4WZ01.201	EVT
30	31	2014.10.14	EMC	EMC solution	XF3101 change from 68.IH601.301 to 068.IH219.3001	EVT
31	58	2014.10.14	ME	ME change	Delete 1st (62.10043.K51) of WLAN1	EVT
32	27	2014.10.14	EMC	EMC solution for DMIC	Add EL2701 68.00217.511	EVT
33	31	2014.10.14	ME	ME change	Change RJ45 to 022.10001.0E21	EVT
34	46	2014.10.14	Power	Use VCC0_SENSE and VSS0_SENSE to VR	Change PR4658 and PR4652 from 100Ω to 0Ω	EVT
35	46	2014.10.14	Power	Fine tune for VCC_CORE	Change PR4668 from 200Ω to 390Ω Change PC4616 from 39pF to 220pF Change PC4609 from 68pF to 47pF Change PR4664 from 620kΩ to 768kΩ	EVT
36	48	2014.10.14	Power	Fine tune for GFX_CORE	Change PR4849 from 200Ω to 390Ω Change PC4808 from 39pF to 390pF	EVT
37	48	2014.10.16	Power	For VCORE SVIDDAT fine tune For VGFX SVIDDAT fine tune	Reserve PR4679 & PR4856	EVT
38	52	2014.10.21	ME	ME change LCD1	1st--->20.F2379.040 2nd--->20.F2091.040	EVT
39	24	2014.10.22	Power,EC	IPCC fail	R2461--->stuff, R2434--->DY	EVT
40	32	2014.11.20	EE	leakage	Reserve R3222 to 3D3V_S5 for Card Reader	DVT1
41	16	2014.11.21	EE	Follow CRB v1.0.	DY R1611,R1614 and R1613 and add R1615	DVT1
42	18	2014.11.21	EE	Fine tune signal level	Change R1857 from 10k to 2.2k	DVT1
43	24	2014.11.21	EE	Change for board ID	Change R2457	DVT1
44	43	2014.11.21	MW	ME change	Change BATT1 from 20.F2504.010 to 020.F0282.0010	DVT1
45	47	2014.11.25	Power	Reserve for acoustic noise	Reserve PT4702	DVT1
46	52	2014.11.28	EE	Change for panel sequence	Change C5226	DVT1
47	46	2014.11.28	Power,EE	Change to PC4609 for common part	Change to PC4609	DVT1
48	34	2014.12.01	EMI	For EMI solution	Install EU3402	DVT1
49	29	2014.12.01	EMI	For EMI solution	Install SPR1 and SPR2	DVT1
50	51	2014.12.01	Power	Power change	Change PL5101	DVT1
51	51	2014.12.01	Power	Power change	Change PL5002	DVT1
52	49	2014.12.01	Power	Power change	Change PL4901	DVT1
53	8	2014.11.28	EE	Pull high	Install R826, R831, R818 and R824 for pull high	DVT1
54	24	2014.12.04	EC	Reserve for EC	Reserve R2468 and R2467	DVT1
55	16	2014.12.04	EE	Vender suggest	Change X1601	DVT1
56	19	2014.12.05	EE	Reserve R1932	Reserve R1932	
57	24	2014.12.08	EE	Reserve R1932 for power consumption measure	Add R2403	
58	24,99	2014.12.08	EE,EC	Reserve for PCIE wake	Add R9953(install), R2431(DY) and R2407	
59	34	2014.12.08	EE,EMC	Change for SI fail	Change EU3401 and EU3403	

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Title: Change History-02

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
60	16	2014.12.08	EE	Crystal vender suggest	Change C1601 and C1602 from 8p to 3.3p	DVT1
61	18	2014.12.08	EE	Crystal vender suggest	Change C1806 and C1807 from 5p to 3.9p	DVT1
62	18	2014.12.09	EE	Reserve	Reserve R1879(DY) and R1878(DY)	DVT1
63	8	2014.12.10	EE	Follow CRB v1.0	Change R814 from 80Ω to 100Ω	DVT1
64	46,48	2014.12.10	Power	Power change solution for Vcore and Vgfx	Change PU4601 and PU4802 from RT8171BGQW to RT8199BGQW Change PR4647 from 86.6kΩ to 105kΩ Change PR4673 from 24.9kΩ to 23.7kΩ Change PR4670 from 2.2Ω to 20Ω Change PR4657 forom 68kΩ to 57.6kΩ Change PR4676 and PR4678from 100Ω to 2.2Ω Change PR4658 and PR4652 from 0Ω to 2.2Ω Change PC4616 from 220pF to 470pF Change PR4664 from 768kΩ to 887kΩ Change PR4825 from 86.6kΩ to 105kΩ Change PR4850 from 510Ω to 390Ω Change PR4838 from 24.9kΩ to 23.7kΩ Change PR4811 from 2.2Ω to 20Ω Change PR4834 from 620kΩ to 887kΩ Change PR4830 from 68kΩ to 57.6kΩ Change PC4808 from 390pF to 470pF DY part:PT4701,PC1077,C1048,PC4706,C1042,PC4830,PC1101,PC1075, PC1068,PC4822,PC4831,C1040,PC1076,PC1072,PT4801,PC1084,PC1088, PC1085,PC1091,PC4815,PC1086,PC4814,PC1083,PC1082,PC1079, PC1089,PC1092,PC1078	DVT1
65	44	2014.12.10	Power	Power change	PD4402 DY	DVT1
66	45	2014.12.10	Power	Power change	Change PU5001 from SY8208DQNC to SY8206DQNC	DVT1
67	24	2015.01.19	vender	EE change	X2401 change 2nd from 82.30001.B11 to 082.30003.0441	DVT2
68	54	2015.01.21	EMI	EMI issue	change R5415,R5416,R5417,R5418 to 150Ω and install	DVT2
69	85	2015.01.21	EMI	EMI issue	Add EC8512	DVT2
70	85	2015.01.21	EMI	EMI issue	Change EC8508.EC8509,EC8510,EC8511 from 100pF to 10000pF	DVT2
71	25	2015.01.21	EE & SW	EE and SW change	Change SPI ROM from 16M WSON to 8M SOIC	DVT2
72	85	2015.01.26	RF	RF install	Install EC8507	DVT2
73	12	2015.01.26	RF	EMI issue	Add C1221 and C1222	DVT2
74	42	2015.01.28	Power	shortage issue.	Change PQ4204 1st	DVT2
75	86	2015.01.30	EMI	EMI issue	Add SPR4	DVT2
76	96	2015.01.30	EE	MB_PWR_BTN# level modify when use XDP	Modify POWER_SW_IN# and change R9605 from 1k to 1M	DVT2
77	62	2015.01.30	EMI	TouchPad ESD issue	Add ED6201 and ED6202	DVT2
78	15	2015.01.30	EE	Follow CRB v1.2 and check list v1.2	Change R1506 from 10k to 4.7k	DVT2
79	44	2015.02.02	Power	Power delete	Delete 1st 69.60040.001 of PD4401 and PD4405	DVT2
80	52	2015.02.02	EE	OBS issue	Change 1st from 69.60040.001 to 69.50007.G71	DVT2
81	18	2015.02.05	EE	Vender suggest	Change C1806 and C1807 from 3.3pF to 4.7pF	DVT2
82	54	2015.02.05	EE	EE add	Add 2nd 73.00102.007 for U5401	DVT2
83	36	2015.02.24	EE	For S5 power saving	R3617:DY, R3616:install	DVT2
84	8,46,48	2015.02.24	EE	For S3 power saving	Change R827,PR4633,PR4817 from 10k to 100k	DVT2

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
85	19	2015.03.18	EE	Reserve for PCIE_CLK leakage issue	Reserve 0Ω for PCIE CLK	A00
86	32	2015.03.23	EE	Add for leakage issue	Add U3202	A00
87	24	2015.03.23	EE	Change for board ID	Change R2457 to from 8.2k to 33k	A00
88	54	2015.03.23	EE	Change for HDMI compatibility	Install Q5408 and Q5407 Add R5415 and R5416 for HDMI compatibility	A00
89	86	2015.03.16	ME	Add 2nd	Add 2nd 34.4WZ01.101 for HS7	A00
90	18	2015.03.27	EE	TPM schematic DY	DY Q1819,R1870,R1871,R1872	A00
91	27	2015.03.27	EE	Change 0Ω to short pad	Add R2743	A00
92	27	2015.03.23	EE	Add for leakage issue	Change power rail for pin 18 and pin 13 from 3D3V_S0 to 3D3V_S0_CARD	A00
92	36	2015.03.27	EE	Reserve for power dischange	Reserve dischange schematic for 3D3V_LAN and 3D3V_S5_WLAN	A00
93	19	2015.03.17	EE	Reserve	Reserve CLK_PCIE_WLAN_REQ2# S0 power rail	A00
94	all	2015.03.27	EE	Change 0Ω to short pad	Change 0Ω to short pad	A00
95	18	2015.04.22	EE	RTC rail power consumption	CPU pin G18 short to ground	A00
96	32,33	2015.04.24	EE	Card reader SI and EMI	Change EC3303 EC3307 EC3308 EC3310 EC3311 EC3315 to 10pF Change R3209 to 15Ω	A00
97	42	2015.05.20	Power	Add 2nd	Add 2nd 83.P6SBM.DAG for PD4201	PD
98	42,43	2015.04.20	Power	Delete unqualified part 75.00099.K7D(YEASHIN).	Delete 2nd 75.00099.K7D for 75.00099.O7D	PD
99	51	2015.09.21	Power	1st and 2nd(068.2R210.1381) have the different packaging	Change PL5101 068.2R210.1381(2nd) to 068.2R210.1391	
100	62	2015.11.06	EE	cost down version	Add 2nd source 071.01117.0B03 for U6202(71.01117.003)	
101	52	2015.11.03	EE	Sourcer request	Add 3rd source 84.00658.C3D for U5201	
102	42	2015.11.03	EE	Sourcer request	Add 3rd 83.P6SMB.JAG for PD4201	

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