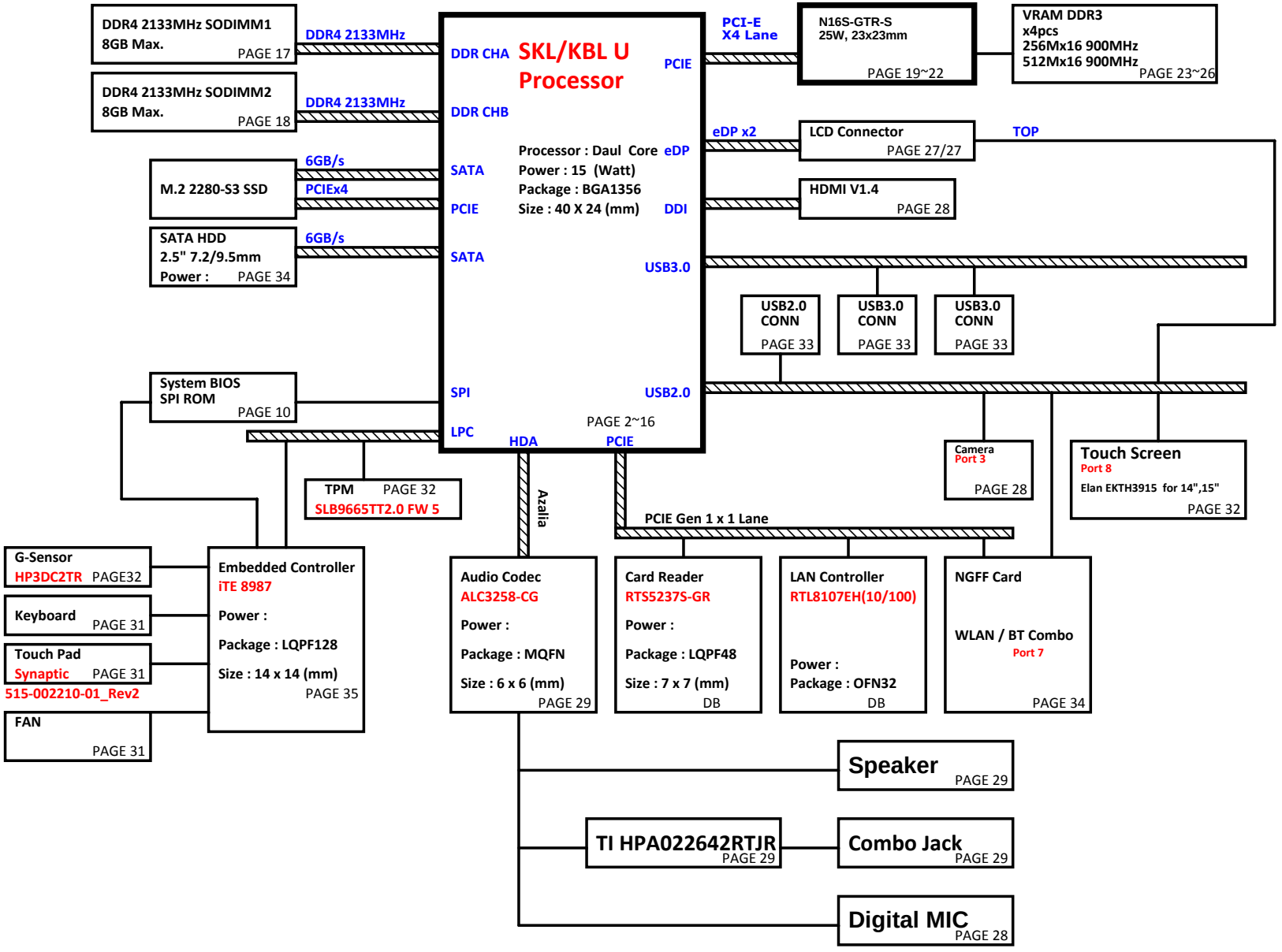
DIS (14") Dessert(G31)

Intel SKL/KBL ULT Platform Block Diagram

01

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



PROJECT :Y11X-6L

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Tuesday, December 01, 2015 Sheet 1 of 49

+3V 4,10,11,12,13,14,15,16,17,18,20,21,25,26,27,28,29,30,32,33,34,40,44,45
+1.0V 4,6,34,39
+VCCSTPLL 4,5,6,9,13,39,40

HDMI

26 IN_D2# → IN_D2# E55
26 IN_D2 → IN_D2 F55
26 IN_D1# → IN_D1# E58
26 IN_D1 → IN_D1 F58
26 IN_D0# → IN_D0# F53
26 IN_D0 → IN_D0 G53
26 IN_CLK# → IN_CLK# F56
26 IN_CLK → IN_CLK G56

U1A SKL_ULT ? **Need apply PN**

DDI1_TXN[0] DDI1_TXP[0] DDI1_TXN[1] DDI1_TXP[1] DDI1_TXN[2] DDI1_TXP[2] DDI1_TXN[3] DDI1_TXP[3]
DDI2_TXN[0] DDI2_TXP[0] DDI2_TXN[1] DDI2_TXP[1] DDI2_TXN[2] DDI2_TXP[2] DDI2_TXN[3] DDI2_TXP[3]
DDI
DISPLAY SIDEBANDS

EDP_TXN[0] C47 → INT_EDP_TXN0 → INT_EDP_TXN0 25
EDP_TXP[0] C46 → INT_EDP_TXP0 → INT_EDP_TXP0 25
EDP_TXN[1] D46 → INT_EDP_TXN1 → INT_EDP_TXN1 25
EDP_TXP[1] C45 → INT_EDP_TXP1 → INT_EDP_TXP1 25
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47
EDP

need surport to FHD 2 Lane

EDP_AUXN E45 → INT_EDP_AUXN → INT_EDP_AUXN 25
EDP_AUXP F45 → INT_EDP_AUXP → INT_EDP_AUXP 25
EDP_DISP_UTIL B52 → TP1

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN F48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP F46

GPP_E13/DDPB_HPD0 L9 → HDMI_HPD_CON → HDMI_HPD_CON 26
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 L5
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD L10 → ULT_EDP_HPD → ULT_EDP_HPD 25

EDP_BKLTEN R12 → PCH_EDP_BLON → PCH_EDP_BLON 25
EDP_BKLTCTL R11 → PCH_DPST_PWM → PCH_DPST_PWM 25
EDP_VDDEN U13 → PCH_DISP_ON → PCH_DISP_ON 25

26 SDVO_CLK → GPP_E18/DDPB_CTRLCLK L13
26 SDVO_DATA → GPP_E19/DDPB_CTRLDATA L12
GPP_E20/DDPC_CTRLCLK N7
GPP_E21/DDPC_CTRLDATA N8
GPP_E22/DDPD_CTRLCLK N11
GPP_E23/DDPD_CTRLDATA N12

+1.0V R3 24.9/F_4 EDP_RCOMP → EDP_RCOMP E52

*SKL_ULT
REV = 1
1 OF 20
?

1026 modify

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!

+3V
R1 *10K/F_4
ULT_EDP_HPD
R2 100K_4

U1D SKL_ULT ? **Need apply PN**

34,40 H_PROCHOT# → R4 499/F_4 → 34 EC_PECI
34 PM_THRMTRIP#

CATERR# D63
EC_PECI A54
PROCHOT# C65
PM_THRMTRIP# C63
SKTOCC# A65
CATERR#
PECI
PROCHOT#
THERMTRIP#
SKTOCC#
CPU MISC

XDP_BPM0 TP8504 C55
XDP_BPM1 TP8505 D55
BPM#[0] B54
BPM#[1] C56
BPM#[2]
BPM#[3]

0924 del

TP200 3D_FW_GPIO_R A6
TP4 CPU_GP1 A7
TP5 CPU_GP2 BA5
TP6 CPU_GP3 AY5
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3

R8 49.9/F_4 PROC_POPIRCOMP AT16
R11 49.9/F_4 PCH_OPI_RCOMP AU16
R12 49.9/F_4 EDRAM_OPIO_RCOMP H66
R14 49.9/F_4 EOPIO_RCOMP H65
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

Rcomp < 600mil

*SKL_ULT
REV = 1
4 OF 20

JTAG

PROC_TCK B61 XDP_TCK0 → XDP_TCK0
PROC_TDI D60 XDP_TDI_CPU → XDP_TDI_CPU
PROC_TDO A61 XDP_TDO_CPU → XDP_TDO_CPU
PROC_TMS C60 XDP_TMS_CPU → XDP_TMS_CPU
PROC_TRST# B59 XDP_TRST#_CPU → XDP_TRST#_CPU 2

PCH_JTAG_TCK B56 JTAG_TCK_PCH → JTAG_TCK_PCH
PCH_JTAG_TDI D59 JTAG_TDI_PCH → JTAG_TDI_PCH
PCH_JTAG_TDO A56 JTAG_TDO_PCH → JTAG_TDO_PCH
PCH_JTAG_TMS C59 JTAG_TMS_PCH → JTAG_TMS_PCH
PCH_TRST# C61 XDP_TRST#_CPU → XDP_TRST#_CPU 2
JTAGX A59 JTAGX_PCH → JTAGX_PCH

+VCCSTPLL
R6 *49.9/F_4 CATERR#

+1.0V
R10 *51_4 JTAGX_PCH
R13 51_4 JTAG_TMS_PCH
R15 51_4 JTAG_TDI_PCH
R16 51_4 JTAG_TDO_PCH
R18 51_4 JTAG_TCK_PCH
Close to Chipset

1013 short

Close to EC

+VCCSTPLL
PM_THRMTRIP# R5 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

PLACE NEAR CPU

+1.0V
XDP_TMS_CPU R17 *51_4
XDP_TDI_CPU R19 *51_4
XDP_TDO_CPU R20 *51_4

+1.0V
H_PROCHOT# R21 1K_4
XDP_TCK0 R22 51_4
XDP_TRST#_CPU R23 51_4

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	02 -- SKYPAKE 1/20(eDP/DDI)	1A
Date: Tuesday, December 01, 2015	Sheet 2 of 49	

17 M_A_DQSN[7:0]
17 M_A_DQSP[7:0]
18 M_B_DQSN[7:0]
18 M_B_DQSP[7:0]
17 M_A_DQ[63:0]
18 M_B_DQ[63:0]

+1.2VSUS 6,17,18,37,39,47

SkyLake ULT Processor (DDR4)

Non Interleave SIDE BY SIDE

Need apply PN

U1B — SKL_ULT — 2 OF 20

U1C — SKL_ULT — 3 OF 20

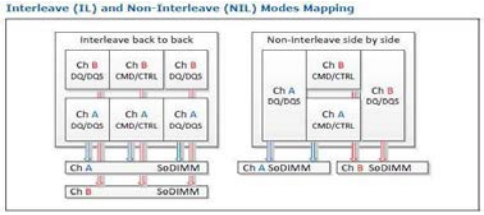
*SKL_ULT
REV = 1

20mils width

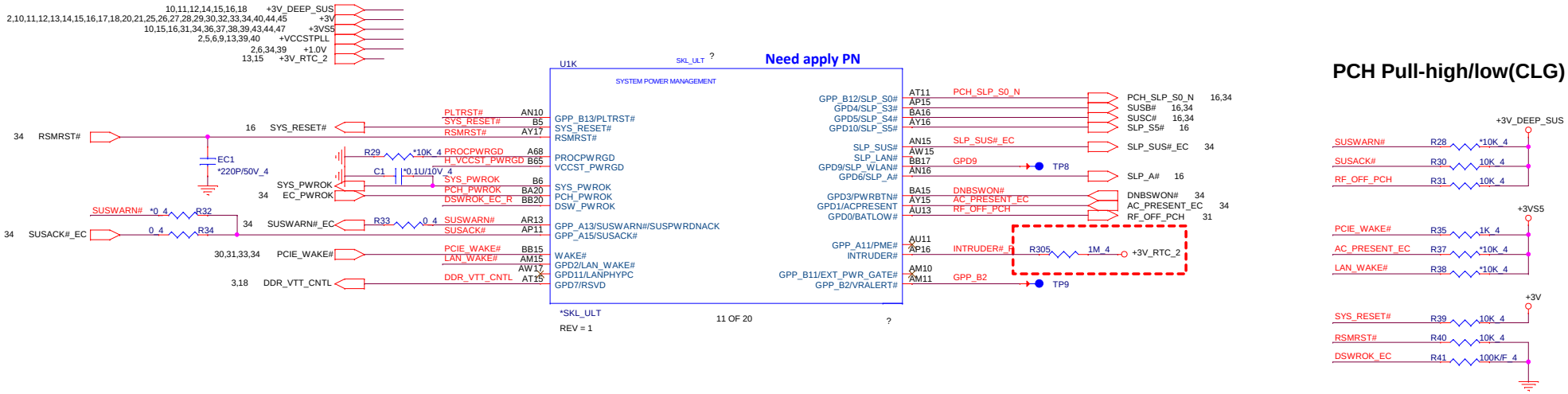
NIL-DDR CH - A

NIL-DDR CH - B

Interleave (IL) and Non-Interleave (NIL) Modes Mapping

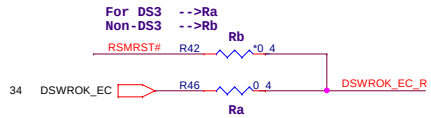


PROJECT :Y11X-6L Quanta Computer Inc.			
Size: Custom	Document Number: 03 -- SKYPAKE 3/20(DDR3-A I/F)		Rev: 1A
Date: Tuesday, December 01, 2015	Sheet: 3 of 49		



PCH Pull-high/low(CLG)

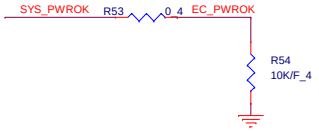
For DS3 Sequence

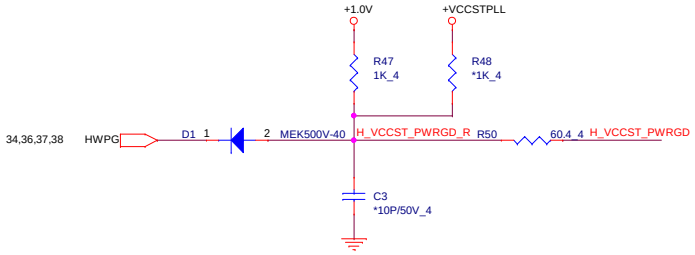


PLTRST#(CLG)

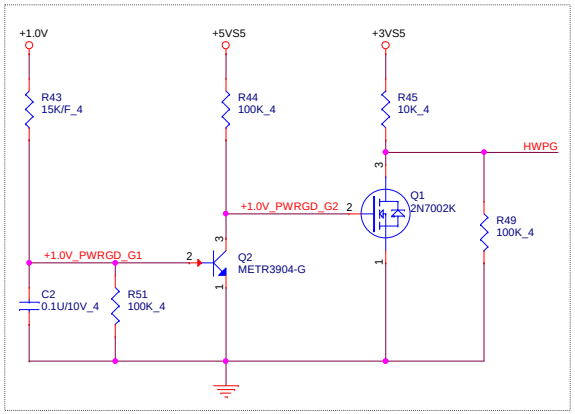
Rise/Fall time less than 100ns

System PWR_OK(CLG)





H_VCCST_PWRGD trace 0.3" - 1.5"



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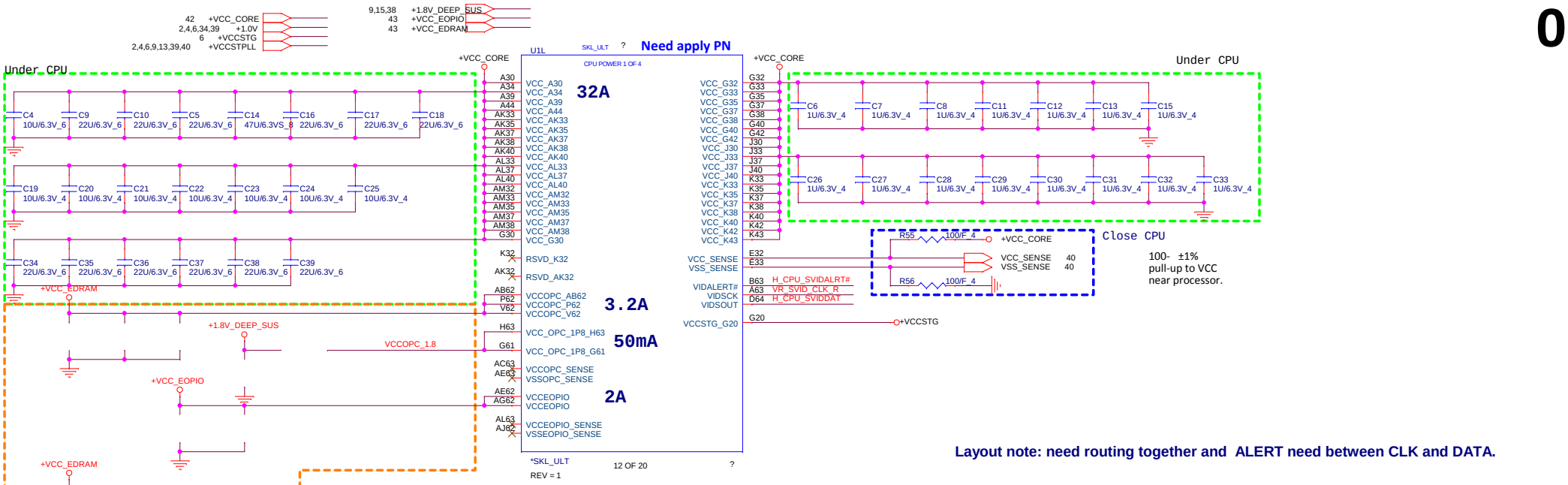
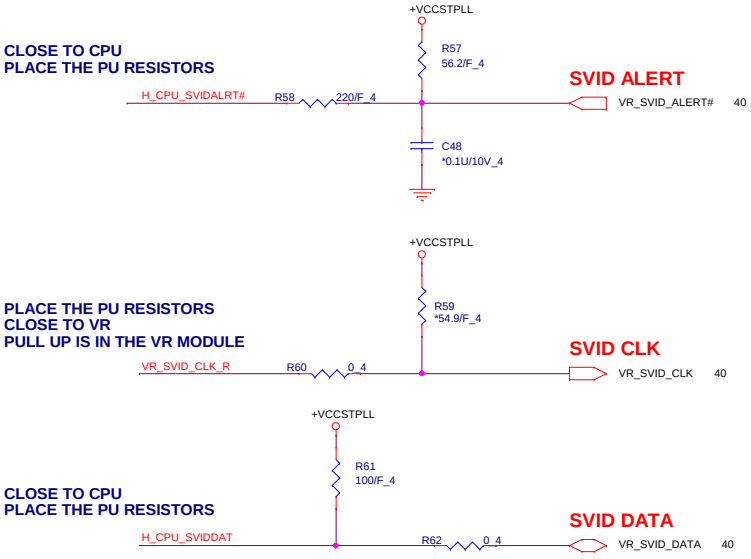
Quanta Computer Inc.

Size	Document Number	Rev
Custom	04 -- SKYPAKE 5/20(Power Manger)	1A
Date: Tuesday, December 01, 2015	Sheet 4 of 49	



Layout note: need routing together and ALERT need between CLK and DATA.



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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Size	Document Number	Rev
Custom	05 -- SKYPAKE 6/20 (POWER-1)	1A

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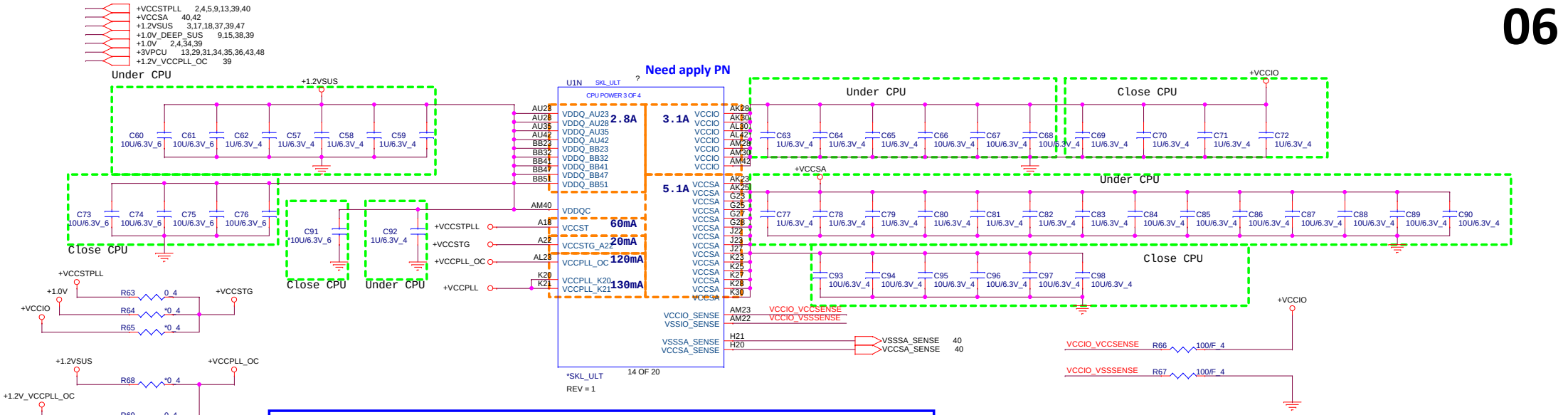
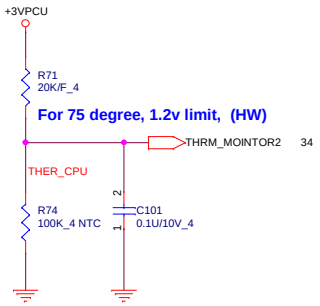
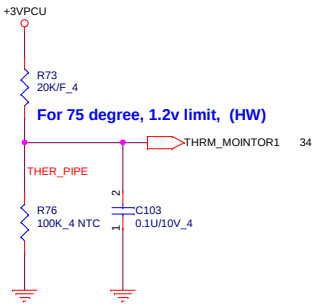


IO Thrm Protect

For CPU USE



For PIPE USE



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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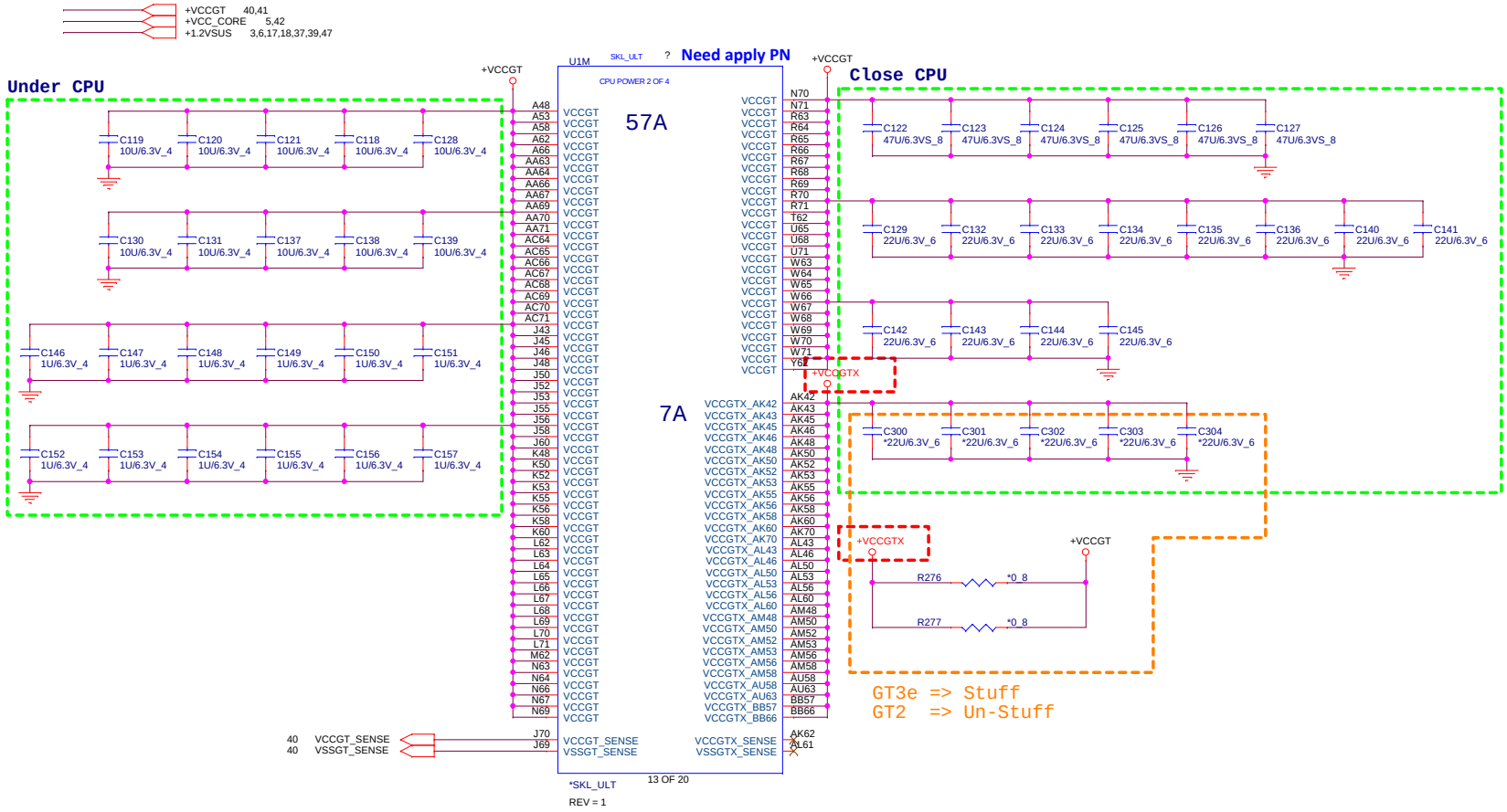
Quanta Computer Inc.

Size	Document Number	Rev
Custom	06 -- SKYPAKE 7/20 (POWER-2)	1A
Date: Tuesday, December 01, 2015	Sheet 6 of 49	



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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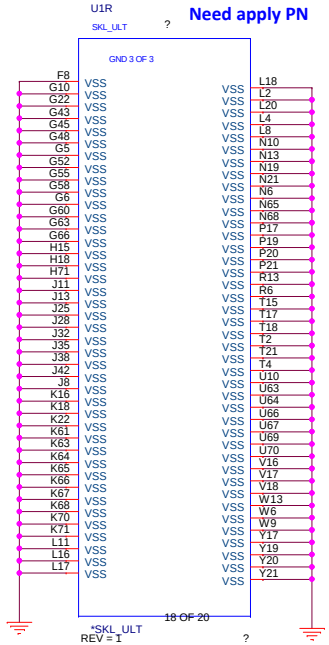
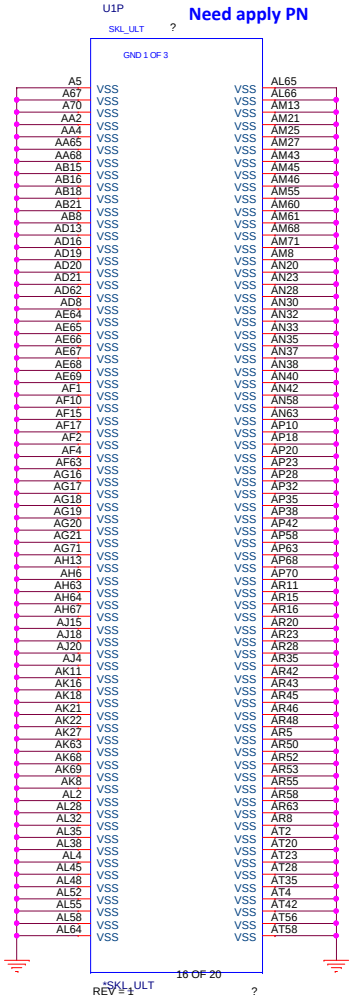
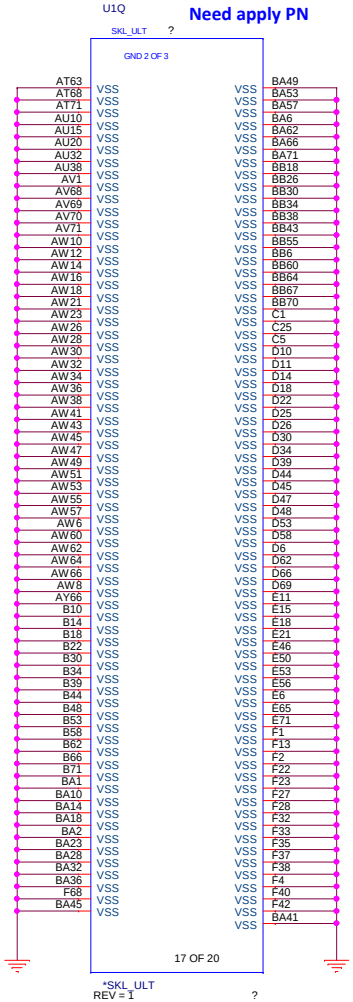
Quanta Computer Inc.

Size	Document Number	Rev
Custom	07 -- SKYPAKE 8/20 (POWER-3)	1A
Date: Tuesday, December 01, 2015	Sheet 7 of 49	







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Quanta Computer Inc.

Size	Document Number	Rev
Custom	8 -- SKYPAKE 9/20 (GND-1)	1A
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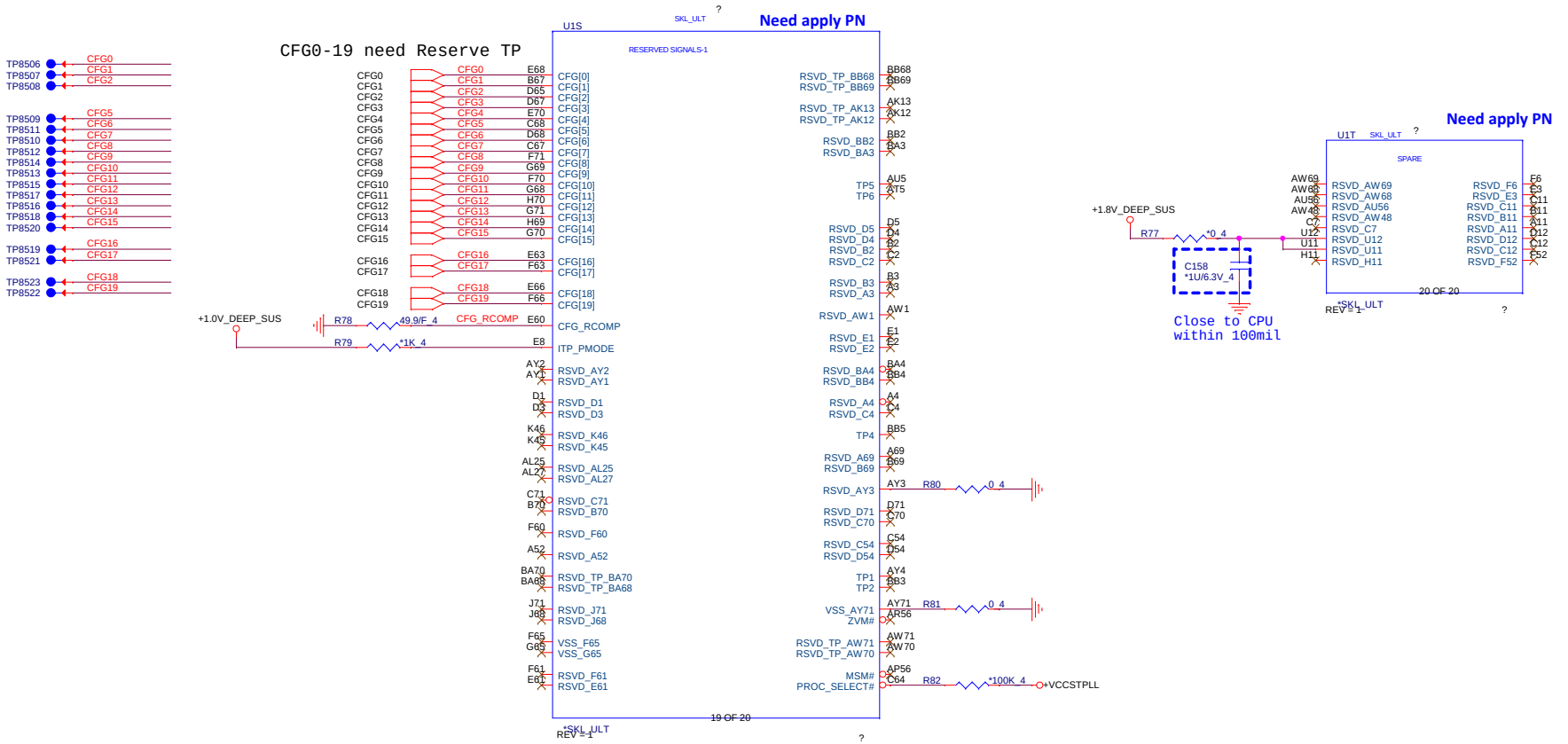

Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R83 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R84 1K_4

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Size	Document Number	Rev
Custom	9 -- SKYPAKE 12/20 (RSV-1)	1A

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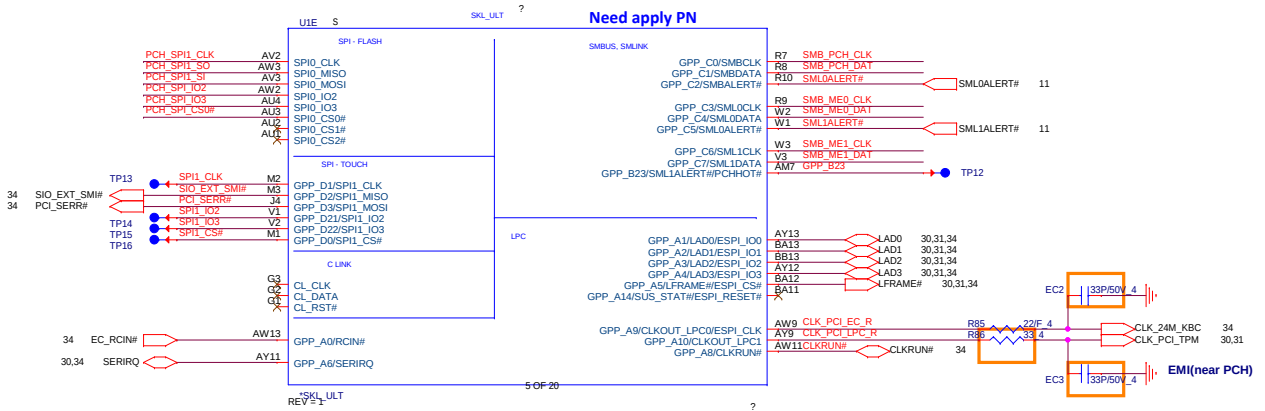
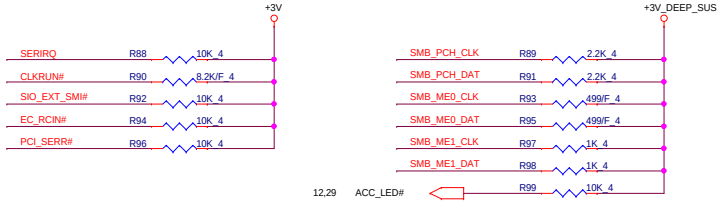
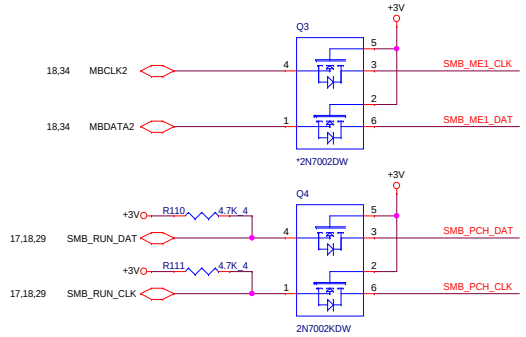
+3V_DEEP_SUS 4,11,12,14,15,16,18
+3V 2,4,11,12,13,14,15,16,17,18,20,21,25,26,27,28,29,30,32,33,34,40,44,45
+5V 25,26,27,28,29,44
+1.0V 2,4,6,34,39
+3VS5 4,15,16,31,34,36,37,38,39,43,44,47



GPIO Pull UP



SMBus/Pull-up(CLG)



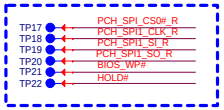
CPU heat pipe local thermal sensor
DDR thermal sensor
RTD2136
EC

Touch Pad
XDP
DDR4

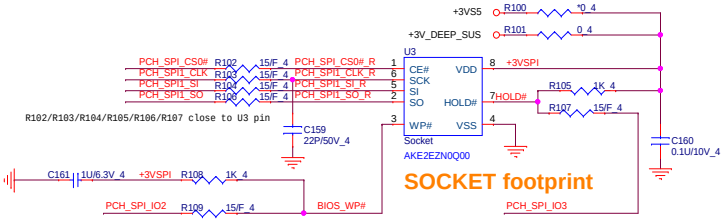
PCH SPI ROM(CLG)

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

need place to TOP



PCH SPI ROM(CLG)



1123 modify P/N to AKE2EZN0Q00

PROJECT :Y11X-6L
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Size	Document Number	Rev
Custom	10 -- SKYPAKE 14/20(SPI/LPC/SMBUS)	1A
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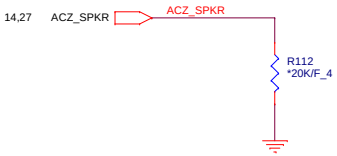
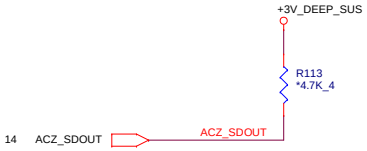
Functional Strap Definitions

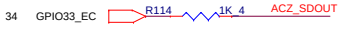
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET

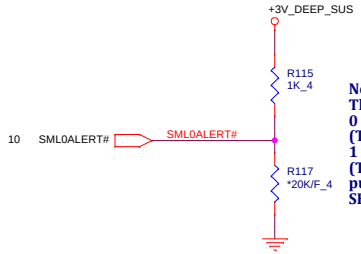


TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

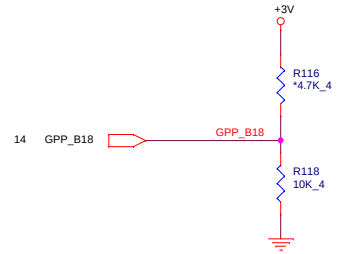


No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.

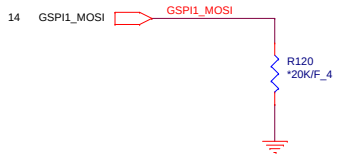




No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

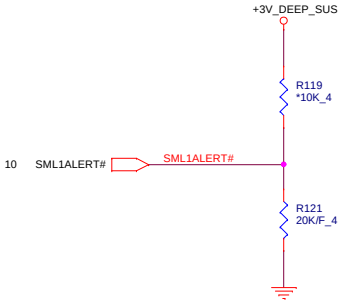


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO
Timer system reboot feature).
This function is useful when running ITP/XDP.

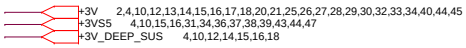


No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.



PROJECT :Y11X-6L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	11 -- SKYPAKE 15/20(HDA)	1A
Date: Tuesday, December 01, 2015	Sheet 11of 49	

+3V 2,4,10,11,13,14,15,16,17,18,20,21,25,26,27,28,29,30,32,33,34,40,44,45
+3VS5 4,10,15,16,31,34,36,37,38,39,43,44,47
+3V_DEEP_SUS 4,10,11,14,15,16,18

DIS only

dGPU

Cardreader

LAN

HDD

WLAN

SSD PCIE x2

SSD SATA*1

U1H SKL_ULT ?

PCIE/USB3/SATA

SSIC / USB3

USB2

Need apply PN

USB3.0 (M/B-1)

USB3.0 (M/B-2)

1005 Add USB3.0 TXP TP

NO (3D CAMERA)

Combo USB3.0 MB-1

Combo USB3.0 MB-2

Camera

IR Camera

USB2.0 MB

WLAN

Touch Screen

DIS ONLY

1002 Pull high

PLACE 'Ra' WITHIN 500 MILS
FROM USB2_COMP PIN WITH
TRACE IMPEDANCE LESS THAN 0.5 OHMS

Ra

Modify 0922

If OTG is not implemented on the platform, then USB2_ID and USB2_VBUSSENSE should both be connected to ground.

DB modify swap

DB modify

GPIO35:
SSD SATA IF => High
SSD PCIE IF => Low

*SKL_ULT REV = 1

? 8 OF 20

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	VGA
Port2	dGPU	Port1	SSD
Port3	dGPU	Port2	WLAN
Port4	dGPU	Port3	LAN
Port5	CardReader	Port4	CardReader
Port6	LAN	Port5	Un-used
Port7	HDD		
Port8			
Port9	WLAN		
Port10			
Port11	PCIE x2		
Port12	PCIE x2 / SATA2		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	NC
PORT-4	NC

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB-1
PORT-2	Cobime USB3.0 MB-2
PORT-3	Camera
PORT-4	NC
PORT-5	IR Camera
PORT-6	USB2.0 MB
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

PROJECT :Y11X-6L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	12 -- SKYPAKE 16/20 (PCIE/USB)	1A
Date: Tuesday, December 01, 2015	Sheet 12of 49	

+1.0V_DEEP_SUS 9,15,38,39
+BAT_RTC 31,35,48
+1.8V_DEEP_SUS 5,9,15,38
+3V 2,4,10,11,12,14,15,16,17,18,20,21,25,26,27,28,29,30,32,33,34,40,44,45
+3VPCU 6,29,31,34,35,36,43,48

1005 SWAP CLK RQ Port

VGA	19	CLK_VGA_N	CLK_VGA_N
	19	CLK_VGA_P	CLK_VGA_P
	19	PCIE_CLKREQ_VGA#	PCIE_CLKREQ_VGA#
SSD	32	CLK_PCIE_SSDN	CLK_PCIE_SSDN
	32	CLK_PCIE_SSDP	CLK_PCIE_SSDP
	32	PCIE_CLKREQ_SSD#	PCIE_CLKREQ_SSD#
WLAN	31	CLK_PCIE_WLANN	CLK_PCIE_WLANN
	31	CLK_PCIE_WLANP	CLK_PCIE_WLANP
	31	PCIE_CLKREQ_WLAN#	PCIE_CLKREQ_WLAN#
LAN	33	CLK_PCIE_LANN	CLK_PCIE_LANN
	33	CLK_PCIE_LANP	CLK_PCIE_LANP
	33	PCIE_CLKREQ_LAN#	PCIE_CLKREQ_LAN#
Cardreader	30	CLK_PCIE_CRN	CLK_PCIE_CRN
	30	CLK_PCIE_CRP	CLK_PCIE_CRP
	30	PCIE_CLKREQ_CR#	PCIE_CLKREQ_CR#

U1J SKL_ULT ? Need apply PN

CLOCK SIGNALS

D42 CLKOUT_PCIE_N0 / C42 CLKOUT_PCIE_P0 / AR10 GPP_B5/SRCCLKREQ0#
B42 CLKOUT_PCIE_N1 / A42 CLKOUT_PCIE_P1 / AT7 GPP_B6/SRCCLKREQ1#
D41 CLKOUT_PCIE_N2 / C41 CLKOUT_PCIE_P2 / AT8 GPP_B7/SRCCLKREQ2#
D40 CLKOUT_PCIE_N3 / C40 CLKOUT_PCIE_P3 / AT10 GPP_B8/SRCCLKREQ3#
B40 CLKOUT_PCIE_N4 / A40 CLKOUT_PCIE_P4 / AU8 GPP_B9/SRCCLKREQ4#
E40 CLKOUT_PCIE_N5 / E39 CLKOUT_PCIE_P5 / AU7 GPP_B10/SRCCLKREQ5#

PCIE_CLKREQ5#

CLKOUT_ITPXDP_N F43 CK_XDP_N_R → TP400
CLKOUT_ITPXDP_P E43 CK_XDP_P_R → TP401
GPD8/SUSCLK BA17 → TP203
XTAL24_IN E37 XTAL24_IN
XTAL24_OUT E35 XTAL24_OUT
XCLK_BIASREF E42 XCLK_BIASREF
RTCX1 AM18 RTC_X1
RTCX2 AM20 RTC_X2 → TP38
SRTCRST# AN18 SRTC_RST#
RTCRST# AM16 RTC_RST# → RTC_RST# 16

TBT

10 OF 20

*SKL_ULT REV = 1 ?

1013 CHANGE TO TP

1027 modify for eazy layout

+VCCSTPLL
R135 2.7K/F_4
XCLK_BIASREF
R137 *60.4/F_4

CLK_REQ/Strap Pin(CLG)

+3V
PCIE_CLKREQ_VGA# R136 10K_4
PCIE_CLKREQ_WLAN# R138 10K_4
PCIE_CLKREQ_LAN# R139 10K_4
PCIE_CLKREQ_CR# R140 10K_4
PCIE_CLKREQ_SSD# R141 10K_4
PCIE_CLKREQ5# R142 10K_4

U1I SKL_ULT ? Need apply PN

CSI-2

A36 CSI2_DN0 / B36 CSI2_DP0 / C36 CSI2_DN1 / D36 CSI2_DP1 / C35 CSI2_DN2 / D35 CSI2_DP2 / A35 CSI2_DN3 / B35 CSI2_DP3
C31 CSI2_DN4 / D31 CSI2_DP4 / C33 CSI2_DN5 / D33 CSI2_DP5 / A33 CSI2_DN6 / B33 CSI2_DP6 / A32 CSI2_DN7 / B32 CSI2_DP7
A29 CSI2_DN8 / B29 CSI2_DP8 / C29 CSI2_DN9 / D29 CSI2_DP9 / A27 CSI2_DN10 / B27 CSI2_DP10 / C27 CSI2_DN11 / D27 CSI2_DP11

CSI2_CLKN0 C37 / CSI2_CLKP0 D37 / CSI2_CLKN1 C32 / CSI2_CLKP1 D32 / CSI2_CLKN2 C29 / CSI2_CLKP2 D29 / CSI2_CLKN3 C26 / CSI2_CLKP3 D26
CSI2_COMP E13 / GPP_D4/FLASHTRIG B7 GPP_D4 → R143 100/F_4 → TP39

EMMC

GPP_F13/EMMC_DATA0 AP2 / GPP_F14/EMMC_DATA1 AP1 / GPP_F15/EMMC_DATA2 AP3 / GPP_F16/EMMC_DATA3 AN3 / GPP_F17/EMMC_DATA4 AN1 / GPP_F18/EMMC_DATA5 AN2 / GPP_F19/EMMC_DATA6 AM4 / GPP_F20/EMMC_DATA7 AM1
GPP_F21/EMMC_RCLK AM2 / GPP_F22/EMMC_CLK AM3 / GPP_F12/EMMC_CMD AP4
EMMC_RCOMP AT1 EMMC_RCOMP R144 200/F_4

1001 Del TP

9 OF 20

*SKL_ULT REV = 1 ?

RTC Clock 32.768KHz

C177 12P/50V_4 — Y1 32.768KHZ — C179 12P/50V_4
RTC_X1 / RTC_X2
R147 10M_4

RTC Circuitry(RTC)

4,15 +3V_RTC_2

30mils

+3V_RTC_2 / +BAT_RTC
Coin BAT -->Rb
Rb / Ra
R307 *0_4

Modify 0922

RTC Power trace width 20mils.

R145 *0_6 → RTC_RST#
R146 20K/F_4
C178 1U/6.3V_4
R149 20K/F_4
SRTC_RST#
C182 1U/6.3V_4

+3V_RTC_0
R150 1K_4
+3VPCU
+3V_RTC_1
D2 BAT54CW-7-F
C181 1U/6.3V_4

CN11 RTC_CONN_2P DFHD02MS119

1005 modify

Q5 2N7002K
RTC_RST# / EC_RTC_RST 34
R151 10K_4

External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

TP51 → C176 27P/50V_4
XTAL24_IN / XTAL24_OUT
R148 1M_4
24MHZ +-30PPM Y2
C180 27P/50V_4 → TP52

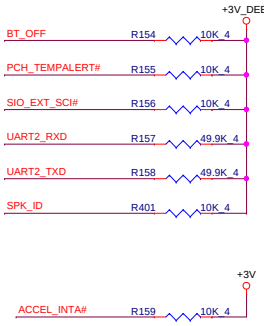
1123 modify P/N to BG624000112

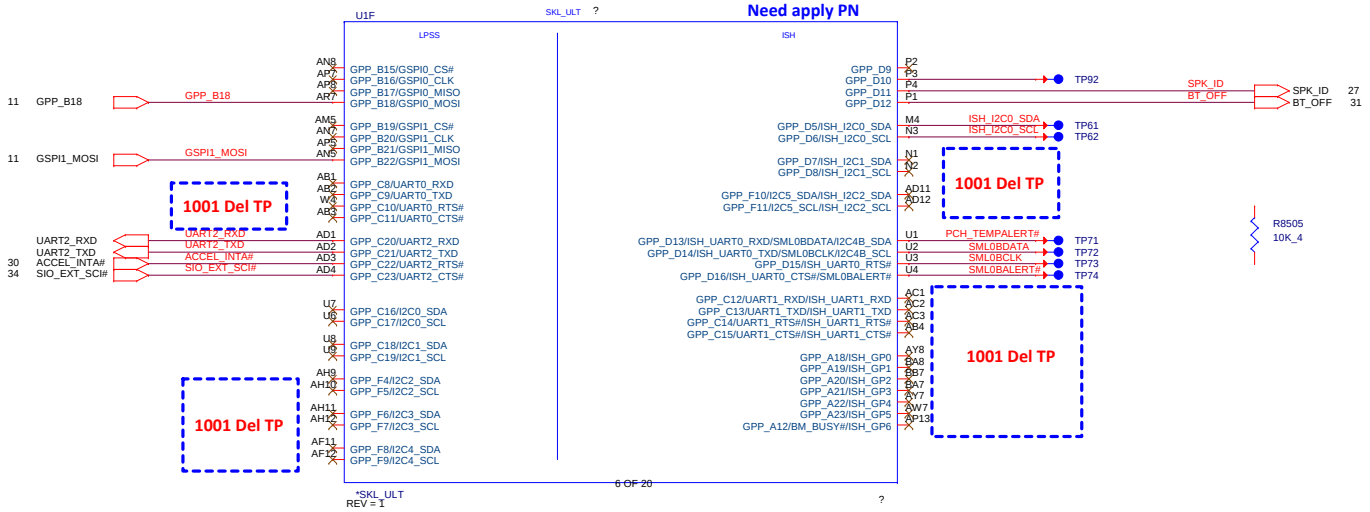
PROJECT :Y11X-6L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	13 -- SKYPAKE 17/20 (CLK)	1A
Date: Tuesday, December 01, 2015	Sheet 13of 49	

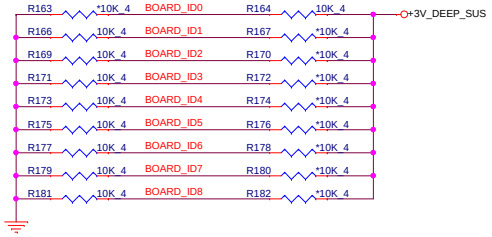
Skylake (GPIO)

+3V 2,4,10,11,12,13,15,16,17,18,20,21,25,26,27,28,29,30,32,33,34,40,44,45
+3V_DEEP_SUS 4,10,11,12,15,16,18



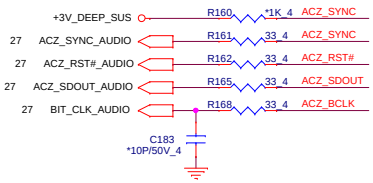


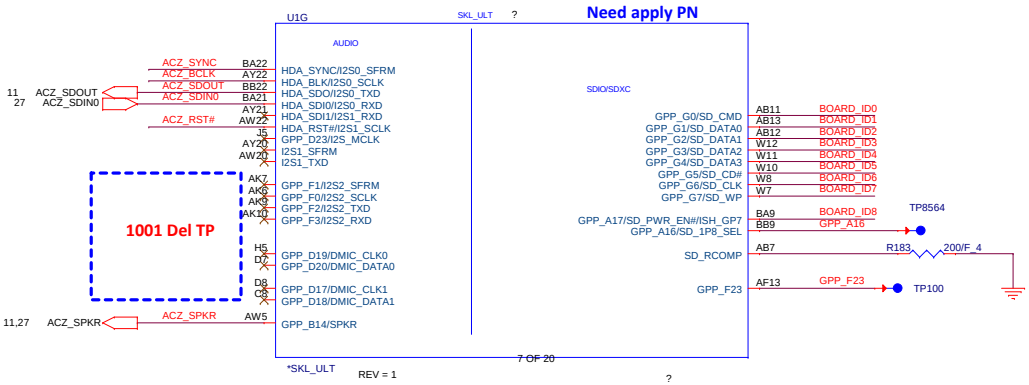
HDA Bus(CLG)



Skylake U	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6 ID5	ID4 ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	Reserve (Default = 00)	00 Single Rank (X1B) 01 Dual Rank (X1B) 10 Meso-AMD (X1A) 11 Reserve	00 14" 01 15" 10 17" 11 Reserve	0 : UMA 1 : DIS

HDA Bus(CLG)





PROJECT :Y11X-6L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	14 -- SKYPAKE 19/20 (GPIO)	1A
Date: Tuesday, December 01, 2015	Sheet 14of 49	

4,10,11,12,14,16,18 +3V_DEEP_SUS
9,38,39 +1.0V_DEEP_SUS
5,9,38 +1.8V_DEEP_SUS

4,10,16,31,34,36,37,38,39,43,44,47 +3VS5
4,13 +3V_RTC_2

U1O SKL_ULT

CPU POWER 4 OF 4

Need apply PN

PCH Internal VRM

Ca and Cb close to CPU less then 100 mils

+VCCPRIM
C184 1U/6.3V_4
AB19 AB20 P18
VCCPRIM_1P0 VCCPRIM_1P0 VCCPRIM_1P0
2.899A

+1.0V_DEEP_SUS
C185 1U/6.3V_4
AF18 AF19 V20 V21
VCCPRIM_CORE VCCPRIM_CORE VCCPRIM_CORE VCCPRIM_CORE
2.57A

+VCCDSW_1.0V
Ca
C187 1U/6.3V_4
AL1
DCPDSW_1P0

+1.0V_DEEP_SUS
R188 0_4 22mA +VCCMPHYAON_1P0
C188 1U/6.3V_4
K17 L1
VCCMPHYAON_1P0 VCCMPHYAON_1P0

+1.0V_DEEP_SUS
C189 1U/6.3V_4
C190 47U/6.3VS_8
N15 N16 N17 P15 P16
VCCMPHYGT_1P0_N15 VCCMPHYGT_1P0_N16 VCCMPHYGT_1P0_N17 VCCMPHYGT_1P0_P15 VCCMPHYGT_1P0_P16
1.714A

+1.0V_DEEP_SUS
R194 0_6 +VCCAMPHYPLL_1P0
C192 1U/6.3V_4
K15 L15
VCCAMPHYPLL_1P0 VCCAMPHYPLL_1P0

+1.0V_DEEP_SUS
R196 0_4 26mA +VCCAPLL_1.0V
V15
VCCAPLL_1P0
0.03A

+1.0V_DEEP_SUS
R199 0_6 +VCCPRIM
AB17 Y18
VCCPRIM_1P0_AB17 VCCPRIM_1P0_Y18

+3VS5
R201 0_4 +3VS5_AD17
C193 1U/6.3V_4
AD17 AD18 AJ17
VCCDSW_3P3_AD17 VCCDSW_3P3_AD18 VCCDSW_3P3_AJ17
0.09A

+V3.3DX_1.5DX_ADO
C194 1U/6.3V_4
AJ19
VCCHDA

+3V_DEEP_SUS
R205 0_4 11mA +VCCSPI
AJ16
VCCSPI

+1.0V_DEEP_SUS
R206 0_6 700mA +VCCSRAM_1.0V
C196 1U/6.3V_4
AF20 AF21 T19 T20
VCCSRAM_1P0 VCCSRAM_1P0 VCCSRAM_1P0 VCCSRAM_1P0

+3V_DEEP_SUS
R207 0_4 75mA +VCCPRIM_3.3V
AJ21
VCCPRIM_3P3_AJ21

+1.0V_DEEP_SUS
R208 0_6 700mA +VCCPRIM_1.0V
AK20
VCCPRIM_1P0_AK20

+1.0V_DEEP_SUS
R209 0_4 33mA +VCCAPLLEBB
C197 1U/6.3V_4
N18
VCCAPLLEBB

15 OF 20

*SKL_ULT
REV = 1

VCCPGPPA AK15 +VCCPGPPA
VCCPGPPB AG15 +VCCPGPPB
VCCPGPPC Y16 +VCCPGPPC
VCCPGPPD Y15 +VCCPGPPD
VCCPGPPE T16 +VCCPGPPE
VCCPGPPF AF16 +VCCPGPPF
VCCPGPPG AD15 +VCCPGPPG

VCCPRIM_3P3_V19 V19
C186 1U/6.3V_4 +3V_DEEP_SUS

VCCPRIM_1P0_T1 T1 +VCCPRIM_1.0V_T1
R187 0_6 +1.0V_DEEP_SUS

VCCATS_1P8 AA1 +VCCATS_1.8V
6mA R190 0_4 +1.8V_DEEP_SUS

VCCRTCPRIM_3P3 AK17 +VCCRTCPRIM_3.3V
1mA R192 0_4 +3V_DEEP_SUS

VCCRTC_AK19 AK19
VCCRTC_BB14 BB14
+3V_RTC_2
20mils

DCPRTC BB10 DCPRTC
Cb
C191 0.1U/10V_4 +1.0V_DEEP_SUS

VCCCLK1 A14 +VCCCLK1
R195 0_4 35mA

VCCCLK2 K19 +VCCCLK2
R198 0_4 29mA

VCCCLK3 L21 +VCCCLK3
R200 0_4 24mA

VCCCLK4 N20 +VCCCLK4
R202 0_4 33mA

VCCCLK5 L19 +VCCCLK5
R203 0_4 4mA

VCCCLK6 A10 +VCCCLK6
R204 0_4 10mA
C195 1U/6.3V_4

GPP_B0/CORE_VID0 AN11 CORE_VID0
GPP_B1/CORE_VID1 AN13 CORE_VID1
TP102
TP103

+3V_DEEP_SUS
20mA +VCCPGPPA R184 0_4
4mA +VCCPGPPB R185 0_4
6mA +VCCPGPPC R186 0_4
8mA +VCCPGPPD R189 0_4
6mA +VCCPGPPE R191 0_4
41mA +VCCPGPPG R193 0_4

+1.8V_DEEP_SUS
160mA +VCCPGPPF R197 0_4

+V3.3DX_1.5DX_ADO
R210 0_4 +3V

+1.0V_DEEP_SUS
C203 *1U/6.3V_4
C204 *22U/6.3V_6

for DS3

+3VS5
R211 100K_4
C205 1U/6.3V_4
U4
5 IN
4 IN
3 ON/OFF
OUT 1
GND 2
IC(5P) G5243AT11U-Lay
34,38,39 SLP_SUS_ON
C210 *10P/50V_4
+3V_DEEP_SUS
C209 0.1U/10V_4

+VCCATS_1.8V
C198 1U/6.3V_4

+3V_RTC_2
C199 0.1U/10V_4
C200 1U/6.3V_4

+VCCRTCPRIM_3.3V
C201 1U/6.3V_4
C202 0.1U/10V_4

+VCCPGPPB
C206 1U/6.3V_4

+VCCPGPPC
C207 1U/6.3V_4

+VCCPGPPE
C208 1U/6.3V_4

modify to AL002821000

PROJECT :Y11X-6L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	15 -- SKYPAKE 20/20(PCH POWER)	1A

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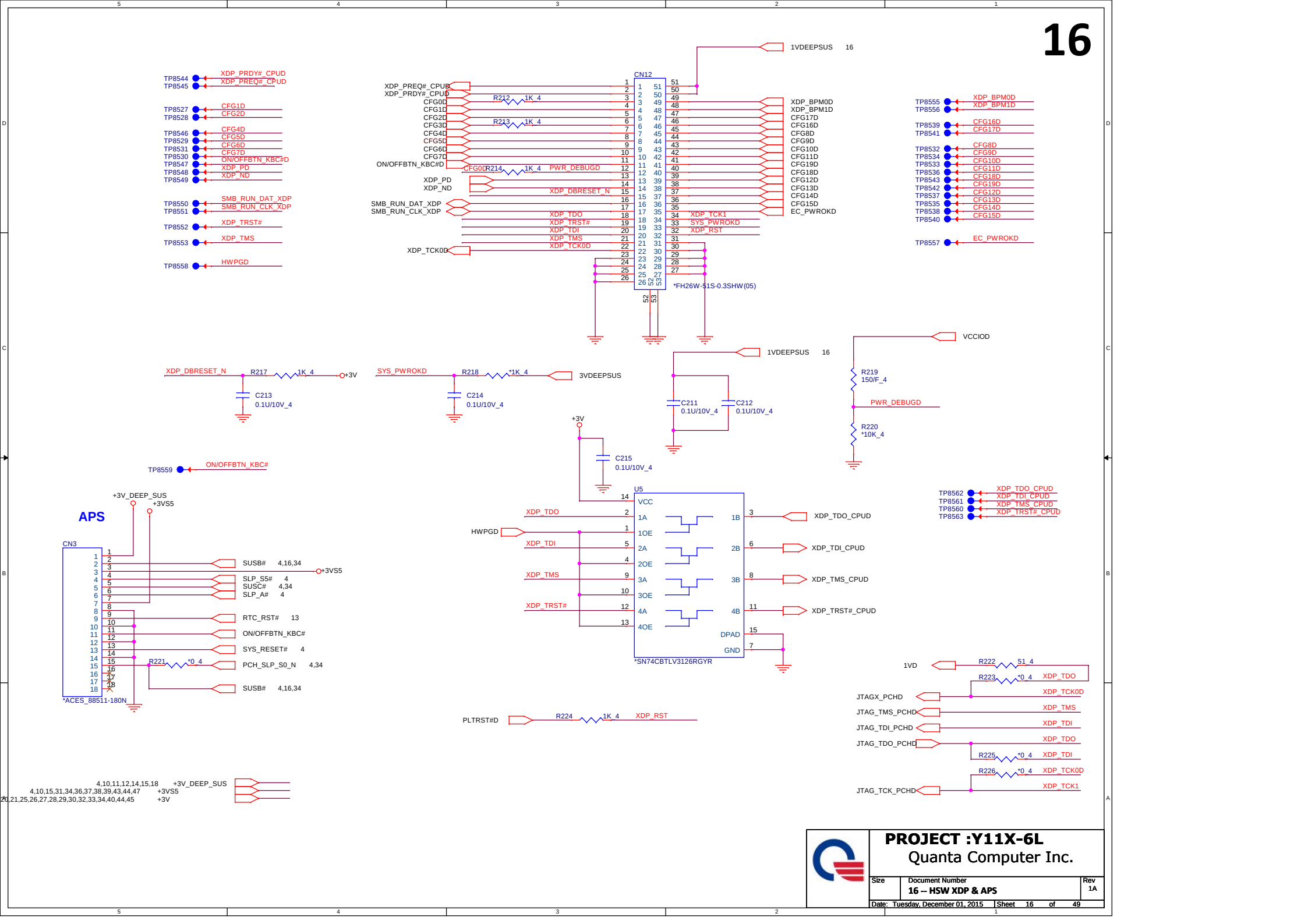
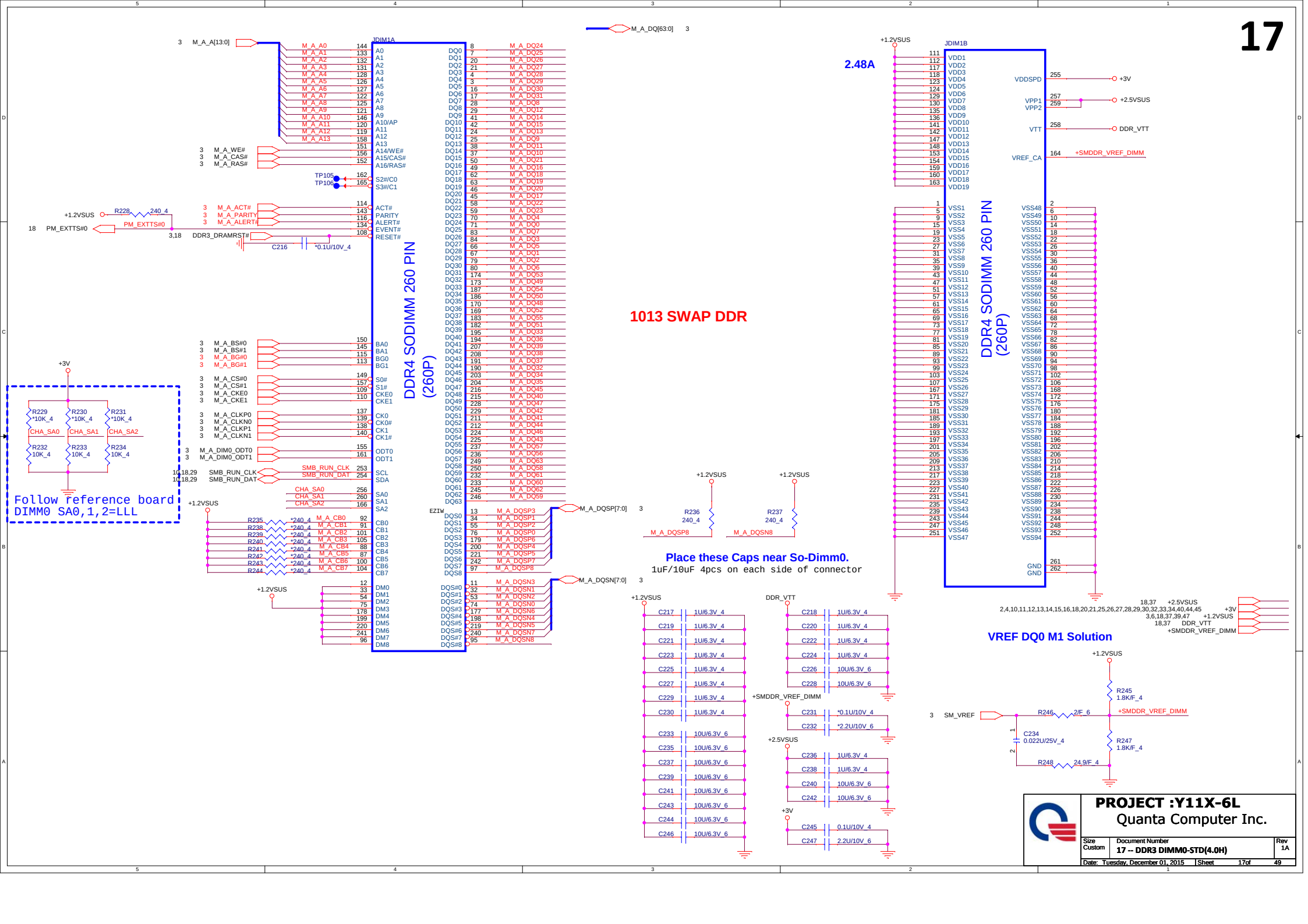


PROJECT :Y11X-6L

Quanta Computer Inc.

Size	Document Number	Rev
	16 -- HSW XDP & APS	1A

Date: Tuesday, December 01, 2015 Sheet 16 of 49


JDIM1A
DDR4 SODIMM 260 PIN (260P)
JDIM1B
DDR4 SODIMM 260 PIN (260P)
1013 SWAP DDR
2.48A
Follow reference board
DIMM0 SA0,1,2=LLL
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
VREF DQ0 M1 Solution
PROJECT :Y11X-6L
Quanta Computer Inc.
Size Custom
Document Number
17 -- DDR3 DIMM0-STD(4.0H)
Rev 1A
Date: Tuesday, December 01, 2015
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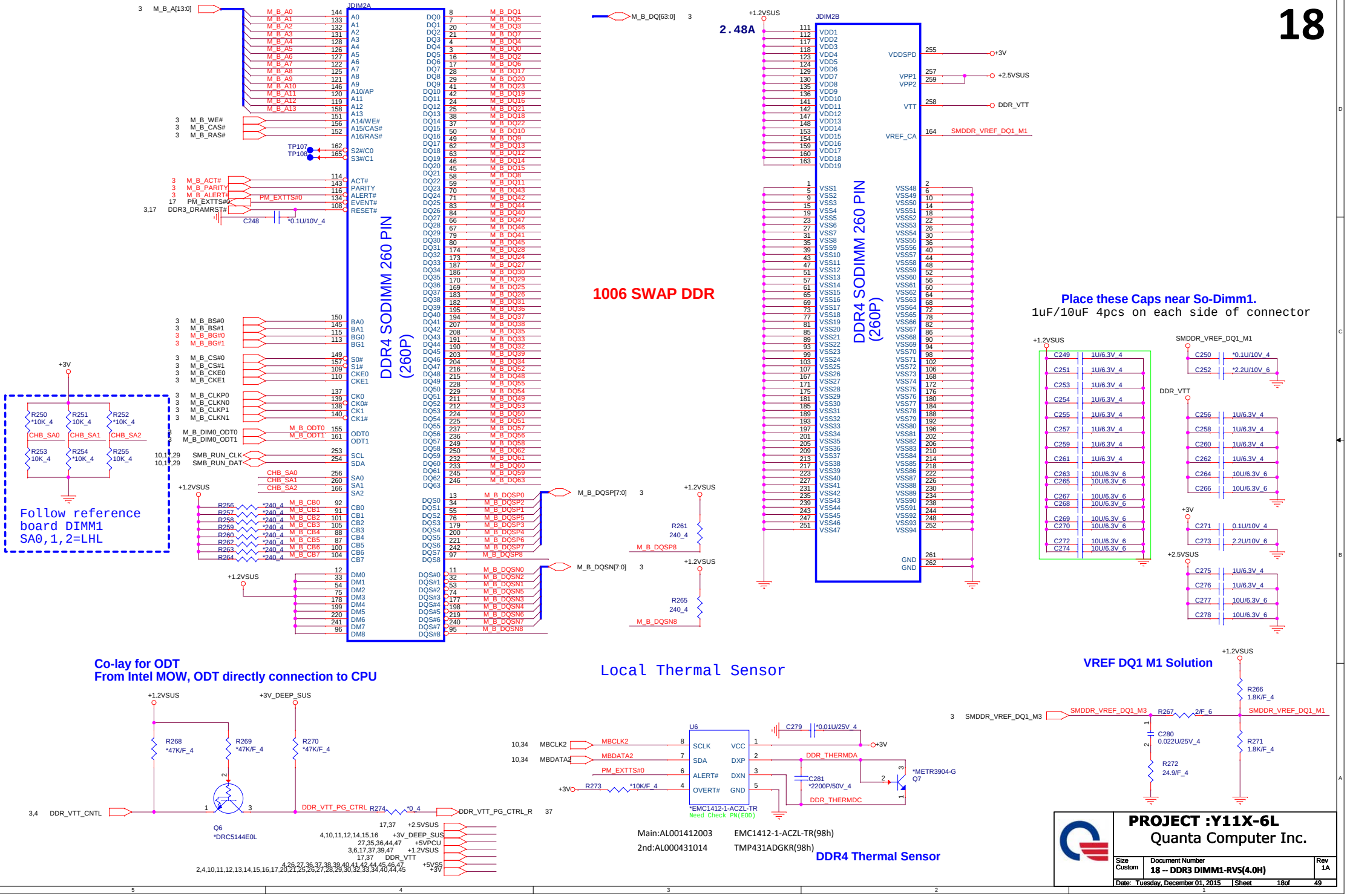
JDIM2A
DDR4 SODIMM 260 PIN (260P)
M_B_A[13:0]
M_B_WE#
M_B_CAS#
M_B_RAS#
TP107
TP108
M_B_ACT#
M_B_PARITY
M_B_ALERT#
PM_EXTTS#0
DDR3_DRAMRST#
C248
*0.1U/10V_4
M_B_BS#0
M_B_BS#1
M_B_BG#0
M_B_BG#1
M_B_CS#0
M_B_CS#1
M_B_CKE0
M_B_CKE1
M_B_CLKP0
M_B_CLKN0
M_B_CLKP1
M_B_CLKN1
M_B_DIM0_ODT0
M_B_DIM0_ODT1
SMB_RUN_CLK
SMB_RUN_DAT
CHB_SA0
CHB_SA1
CHB_SA2
M_B_CB0
M_B_CB1
M_B_CB2
M_B_CB3
M_B_CB4
M_B_CB5
M_B_CB6
M_B_CB7
M_B_DQ[63:0]
M_B_DQSP[7:0]
M_B_DQSN[7:0]
M_B_DQSP8
M_B_DQSN8
R261
R265
240_4
+1.2VSUS
+3V
R250 *10K_4
R251 10K_4
R252 *10K_4
R253 10K_4
R254 *10K_4
R255 10K_4
Follow reference board DIMM1 SA0,1,2=LHL
R256 *240_4
R257 *240_4
R258 *240_4
R259 *240_4
R260 *240_4
R262 *240_4
R263 *240_4
R264 *240_4
1006 SWAP DDR
JDIM2B
2.48A
DDR4 SODIMM 260 PIN (260P)
VDDSPD
VPP1
VPP2
VTT
VREF_CA
SMDDR_VREF_DQ1_M1
DDR_VTT
+2.5VSUS
Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector
C249 1U/6.3V_4
C251 1U/6.3V_4
C253 1U/6.3V_4
C254 1U/6.3V_4
C255 1U/6.3V_4
C257 1U/6.3V_4
C259 1U/6.3V_4
C261 1U/6.3V_4
C263 10U/6.3V_6
C265 10U/6.3V_6
C267 10U/6.3V_6
C268 10U/6.3V_6
C269 10U/6.3V_6
C270 10U/6.3V_6
C272 10U/6.3V_6
C274 10U/6.3V_6
C250 *0.1U/10V_4
C252 *2.2U/10V_6
C256 1U/6.3V_4
C258 1U/6.3V_4
C260 1U/6.3V_4
C262 1U/6.3V_4
C264 10U/6.3V_6
C266 10U/6.3V_6
C271 0.1U/10V_4
C273 2.2U/10V_6
C275 1U/6.3V_4
C276 1U/6.3V_4
C277 10U/6.3V_6
C278 10U/6.3V_6
Co-lay for ODT
From Intel MOW, ODT directly connection to CPU
+3V_DEEP_SUS
R268 *47K/F_4
R269 *47K/F_4
R270 *47K/F_4
DDR_VTT_CNTL
DDR_VTT_PG_CTRL
R274 *0_4
DDR_VTT_PG_CTRL_R
Q6
*DRC5144E0L
Local Thermal Sensor
U6
SCLK
SDA
ALERT#
OVERT#
VCC
DXP
DXN
GND
MBCLK2
MBDATA2
PM_EXTTS#0
R273 *10K/F_4
C279 *0.01U/25V_4
DDR_THERMDA
DDR_THERMDC
C281 *2200P/50V_4
*METR3904-G
Q7
*EMC1412-1-ACZL-TR
Need Check PN(EOD)
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)
DDR4 Thermal Sensor
VREF DQ1 M1 Solution
SMDDR_VREF_DQ1_M3
R266 1.8K/F_4
R267 2/F_6
C280 0.022U/25V_4
R271 1.8K/F_4
R272 24.9/F_4
PROJECT :Y11X-6L
Quanta Computer Inc.
Size Custom
Document Number 18 -- DDR3 DIMM1-RVS(4.0H)
Rev 1A
Date: Tuesday, December 01, 2015
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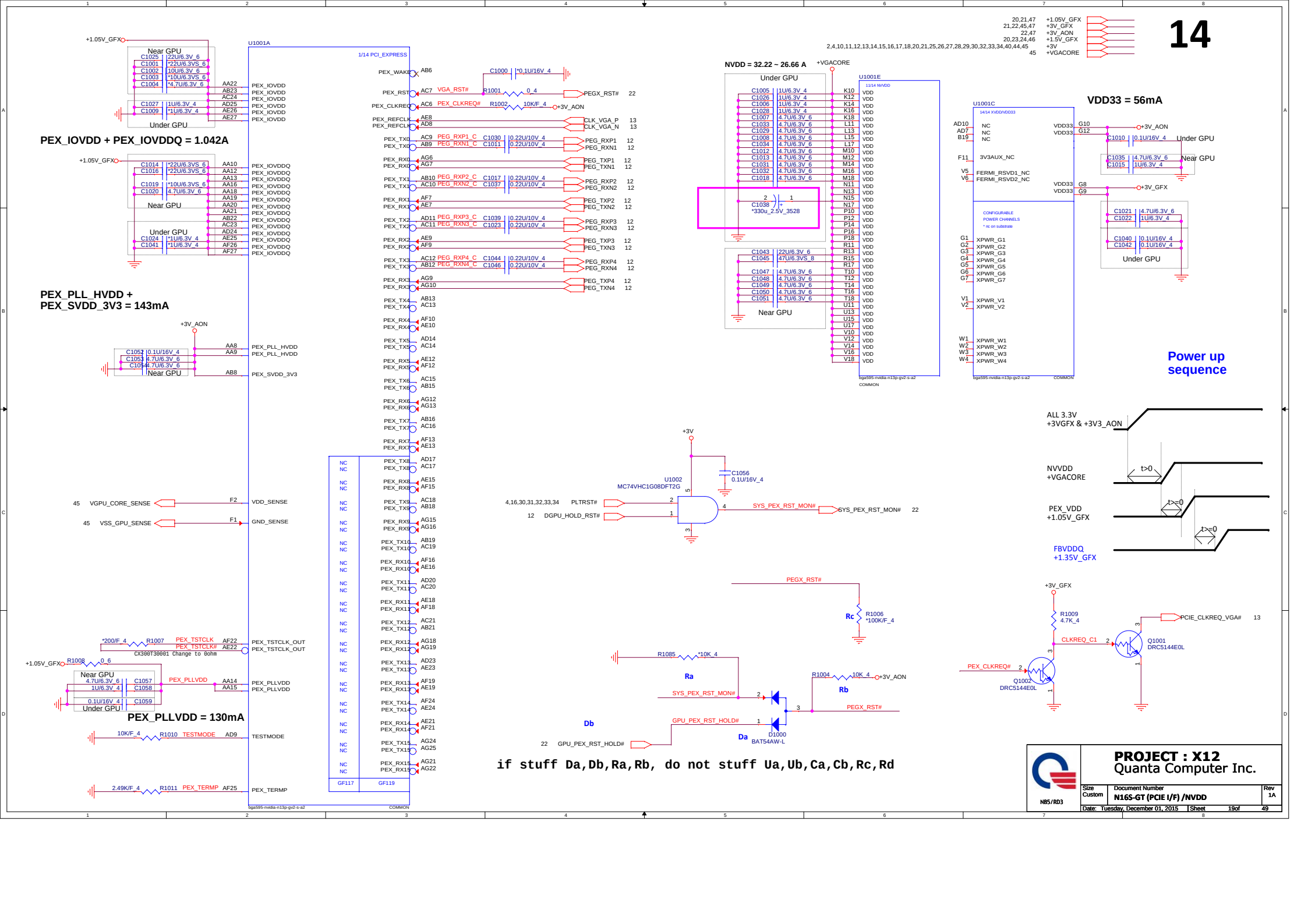
14
PEX_IOVDD + PEX_IOVDDQ = 1.042A
PEX_PLL_HVDD +
PEX_SVDD_3V3 = 143mA
PEX_PLLVDD = 130mA
NVDD = 32.22 ~ 26.66 A
VDD33 = 56mA
Power up
sequence
ALL 3.3V
+3VGFX & +3V3_AON
NVVDD
+VGACORE
PEX_VDD
+1.05V_GFX
FBVDDQ
+1.35V_GFX
if stuff Da,Db,Ra,Rb, do not stuff Ua,Ub,Ca,Cb,Rc,Rd
PROJECT : X12
Quanta Computer Inc.
N16S-GT (PCIE I/F) /NVDD
Tuesday, December 01, 2015

U1001E

R1012 10K/F_4 PS_FB_CLAMP F3

NC	GF119
FB_CLAMP	GF117

FBA_ODT_L FBA_CMD2 R1014 10K/F_4
FBA_ODT_H FBA_CMD18 R1016 10K/F_4
FBA_RST# FBA_CMD5 R1013 10K/F_4
FBA_CKE_L FBA_CMD3 R1017 10K/F_4
FBA_CKE_H FBA_CMD19 R1015 10K/F_4

2/14 FBA

FBA_D0	E18	VMA_DQ0
FBA_D1	F18	VMA_DQ1
FBA_D2	E16	VMA_DQ2
FBA_D3	F17	VMA_DQ3
FBA_D4	D20	VMA_DQ4
FBA_D5	D21	VMA_DQ5
FBA_D6	F20	VMA_DQ6
FBA_D7	E21	VMA_DQ7
FBA_D8	E15	VMA_DQ8
FBA_D9	D15	VMA_DQ9
FBA_D10	F15	VMA_DQ10
FBA_D11	F13	VMA_DQ11
FBA_D12	C13	VMA_DQ12
FBA_D13	B13	VMA_DQ13
FBA_D14	E13	VMA_DQ14
FBA_D15	D13	VMA_DQ15
FBA_D16	B15	VMA_DQ16
FBA_D17	C16	VMA_DQ17
FBA_D18	A13	VMA_DQ18
FBA_D19	A15	VMA_DQ19
FBA_D20	B18	VMA_DQ20
FBA_D21	A18	VMA_DQ21
FBA_D22	A19	VMA_DQ22
FBA_D23	C19	VMA_DQ23
FBA_D24	B24	VMA_DQ24
FBA_D25	C23	VMA_DQ25
FBA_D26	A25	VMA_DQ26
FBA_D27	A24	VMA_DQ27
FBA_D28	A21	VMA_DQ28
FBA_D29	B21	VMA_DQ29
FBA_D30	C20	VMA_DQ30
FBA_D31	C21	VMA_DQ31
FBA_D32	R22	VMA_DQ32
FBA_D33	R24	VMA_DQ33
FBA_D34	T22	VMA_DQ34
FBA_D35	R23	VMA_DQ35
FBA_D36	N25	VMA_DQ36
FBA_D37	N26	VMA_DQ37
FBA_D38	N23	VMA_DQ38
FBA_D39	N24	VMA_DQ39
FBA_D40	V23	VMA_DQ40
FBA_D41	V22	VMA_DQ41
FBA_D42	T23	VMA_DQ42
FBA_D43	U22	VMA_DQ43
FBA_D44	Y24	VMA_DQ44
FBA_D45	AA24	VMA_DQ45
FBA_D46	Y22	VMA_DQ46
FBA_D47	AA23	VMA_DQ47
FBA_D48	AD27	VMA_DQ48
FBA_D49	AB25	VMA_DQ49
FBA_D50	AD26	VMA_DQ50
FBA_D51	AC25	VMA_DQ51
FBA_D52	AA27	VMA_DQ52
FBA_D53	AA26	VMA_DQ53
FBA_D54	W26	VMA_DQ54
FBA_D55	Y25	VMA_DQ55
FBA_D56	R26	VMA_DQ56
FBA_D57	T25	VMA_DQ57
FBA_D58	N27	VMA_DQ58
FBA_D59	R27	VMA_DQ59
FBA_D60	V26	VMA_DQ60
FBA_D61	V27	VMA_DQ61
FBA_D62	W27	VMA_DQ62
FBA_D63	W25	VMA_DQ63

FBA_DQM0	D19	VMA_DM0
FBA_DQM1	D14	VMA_DM1
FBA_DQM2	C17	VMA_DM2
FBA_DQM3	C22	VMA_DM3
FBA_DQM4	P24	VMA_DM4
FBA_DQM5	W24	VMA_DM5
FBA_DQM6	AA25	VMA_DM6
FBA_DQM7	U25	VMA_DM7

FBA_DQS_WP0	E19	VMA_WDQS0
FBA_DQS_WP1	C15	VMA_WDQS1
FBA_DQS_WP2	B16	VMA_WDQS2
FBA_DQS_WP3	B22	VMA_WDQS3
FBA_DQS_WP4	R25	VMA_WDQS4
FBA_DQS_WP5	W23	VMA_WDQS5
FBA_DQS_WP6	AB26	VMA_WDQS6
FBA_DQS_WP7	T26	VMA_WDQS7

FBA_DQS_RN0	F19	VMA_RDQS0
FBA_DQS_RN1	C14	VMA_RDQS1
FBA_DQS_RN2	A16	VMA_RDQS2
FBA_DQS_RN3	A22	VMA_RDQS3
FBA_DQS_RN4	P25	VMA_RDQS4
FBA_DQS_RN5	W22	VMA_RDQS5
FBA_DQS_RN6	AB27	VMA_RDQS6
FBA_DQS_RN7	T27	VMA_RDQS7

FB_VREF_PROBE D23

23	FBA_CMD0	C27 FBA_CMD0
23	FBA_CMD1	C26 FBA_CMD1
23	FBA_CMD2	E24 FBA_CMD2
23	FBA_CMD3	F24 FBA_CMD3
23,24	FBA_CMD4	D27 FBA_CMD4
23,24	FBA_CMD5	D26 FBA_CMD5
23,24	FBA_CMD6	F25 FBA_CMD6
23,24	FBA_CMD7	F26 FBA_CMD7
23,24	FBA_CMD8	F23 FBA_CMD8
23,24	FBA_CMD9	G22 FBA_CMD9
23,24	FBA_CMD10	G23 FBA_CMD10
23,24	FBA_CMD11	G24 FBA_CMD11
23,24	FBA_CMD12	F27 FBA_CMD12
23,24	FBA_CMD13	G25 FBA_CMD13
23,24	FBA_CMD14	G27 FBA_CMD14
23,24	FBA_CMD15	G26 FBA_CMD15
24	FBA_CMD16	M24 FBA_CMD16
24	FBA_CMD17	M23 FBA_CMD17
24	FBA_CMD18	K24 FBA_CMD18
24	FBA_CMD19	K23 FBA_CMD19
23,24	FBA_CMD20	M27 FBA_CMD20
23,24	FBA_CMD21	M26 FBA_CMD21
23,24	FBA_CMD22	M25 FBA_CMD22
23,24	FBA_CMD23	K26 FBA_CMD23
23,24	FBA_CMD24	K22 FBA_CMD24
23,24	FBA_CMD25	J23 FBA_CMD25
23,24	FBA_CMD26	J25 FBA_CMD26
23,24	FBA_CMD27	J24 FBA_CMD27
23,24	FBA_CMD28	K27 FBA_CMD28
23,24	FBA_CMD29	K25 FBA_CMD29
23,24	FBA_CMD30	J27 FBA_CMD30
		J26 FBA_CMD31

+1.5V_GFX
R1021 *60.4_4 F22 FBA_DEBUG0
R1022 *60.4_4 J22 FBA_DEBUG1

23	VMA_CLK0	D24 FBA_CLK0
23	VMA_CLK0#	D25 FBA_CLK0
24	VMA_CLK1	N22 FBA_CLK1
24	VMA_CLK1#	M22 FBA_CLK1

	D18 FBA_WCK01
	C18 FBA_WCK01
	D17 FBA_WCK23
	D16 FBA_WCK23
	T24 FBA_WCK45
	U24 FBA_WCK45
	V24 FBA_WCK67
	V25 FBA_WCK67

FB_PLLAVDD = 55mA

Add La (0402) for co-lay

+1.05V_GFX L1001 *PBY160808T-300Y-N L1002 HCB1005KF-330T30/S +FB_PLLAVDD
La
C1069 22U/6.3VS_6
C1070 0.1U/16V_4
C1071 0.1U/16V_4
C1072 0.1U/16V_4
F16 FB_PLLAVDD
P22 FB_PLLAVDD
H22 FB_DLLAVDD

FB_DLLAVDD	GF119
FB_PLLAVDD	GF117

FB_DLLAVDD = 15mA

bga595-nvidia-n13p-gv2-s-a2 COMMON

VMA_DQ[63:0] VMA_DQ[63:0] 23,24

FBVDDQ + FBVDD = 3.116A

+1.5V_GFX

U1001D 12/14 FBVDDQ

C1060 0.1U/16V_4
C1061 0.1U/16V_4
C1062 1U/6.3V_4
C1065 1U/6.3V_4
C1066 4.7U/6.3V_6
C1063 4.7U/6.3V_6
C1067 10U/6.3V_6
C1064 22U/6.3V_6

B26	FBVDDQ
C25	FBVDDQ
E23	FBVDDQ
E26	FBVDDQ
F14	FBVDDQ
F21	FBVDDQ
G13	FBVDDQ
G14	FBVDDQ
G15	FBVDDQ
G16	FBVDDQ
G18	FBVDDQ
G19	FBVDDQ
G20	FBVDDQ
G21	FBVDDQ
H24	FBVDDQ
H26	FBVDDQ
J21	FBVDDQ
K21	FBVDDQ
L22	FBVDDQ
L24	FBVDDQ
L26	FBVDDQ
M21	FBVDDQ
N21	FBVDDQ
R21	FBVDDQ
T21	FBVDDQ
V21	FBVDDQ
W21	FBVDDQ

bga595-nvidia-n13p-gv2-s-a2 COMMON

VMA_DM[7:0] 23,24
VMA_WDQS[7:0] 23,24
VMA_RDQS[7:0] 23,24

FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R1018 40.2/F_4 +1.5V_GFX
FB_CAL_PU_GND C24 FB_CAL_PU_GND R1019 42.2/F_4
FB_CALTERM_GND B25 FB_CAL_TERM_GND R1020 51.1/F_4

U1001F 13/14 GND

A2	GND	GND	M13
AB17	GND	GND	M15
AB20	GND	GND	M17
AB24	GND	GND	N10
AC2	GND	GND	N12
AC22	GND	GND	N14
AC26	GND	GND	N16
AC5	GND	GND	N18
AC8	GND	GND	P11
AD12	GND	GND	P13
AD13	GND	GND	P15
AD26	GND	GND	P17
AD15	GND	GND	P2
AD16	GND	GND	P23
AD18	GND	GND	P26
AD19	GND	GND	P5
AD21	GND	GND	R10
AD22	GND	GND	R12
AE11	GND	GND	R14
AE14	GND	GND	R16
AE17	GND	GND	R18
AE20	GND	GND	T11
AB11	GND	GND	T13
AF1	GND	GND	T15
AF11	GND	GND	T17
AF14	GND	GND	U10
AF17	GND	GND	U12
AF20	GND	GND	U14
AF23	GND	GND	U16
AF5	GND	GND	U18
AF8	GND	GND	U2
AG2	GND	GND	U23
AG26	GND	GND	U26
AB14	GND	GND	U5
B1	GND	GND	V11
B11	GND	GND	V13
B14	GND	GND	V15
B17	GND	GND	V17
B20	GND	GND	Y2
B23	GND	GND	Y23
B27	GND	GND	Y26
B5	GND	GND	Y5
B8	GND		
E11	GND		
E14	GND		
E17	GND		
E2	GND		
E20	GND		
E22	GND		
E25	GND		
E5	GND		
E8	GND		
H2	GND		
H23	GND		
H25	GND		
H5	GND		
K11	GND		
K13	GND		
K15	GND		
K17	GND		
L10	GND		
L12	GND		
L14	GND		
L16	GND		
L18	GND		
L2	GND		
L23	GND		
L25	GND		
L5	GND	GND	AA7
M11	GND	GND	AB7

bga595-nvidia-n13p-gv2-s-a2 COMMON

if stuff Da,Ra, do not stuff Ua,Ca,Rb,Rc

GC6_FB_EN
DGPU_VC_EN
D1004 *BAT54CW-7-F
Da
DGPU_FB_EN
R1123 Ra *100K/F_4

For support GC6 2.0

SI 1127 CHANGE TO OR GATE

+3V
Ua
U1003 NL17SZ32DFT2G
Ca C1068 0.1U/16V_4
12,47 DGPU_PWR_EN R1023 *0_4
45,47 DGPU_VC_EN R1024 0_4
Rc
12,22 GC6_FB_EN
DGPU_FB_EN 46
Rb R1025 100K/F_4

2,4,10,11,12,13,14,15,16,17,18,21,25,26,27,28,29,30,32,33,34,40,44,45

19,21,47	+1.05V_GFX
19,21,22,45,47	+3V_GFX
19,22,47	+3V_AON
23,24,46	+1.5V_GFX
	+3V

NB5/RD3

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Quanta Computer Inc.

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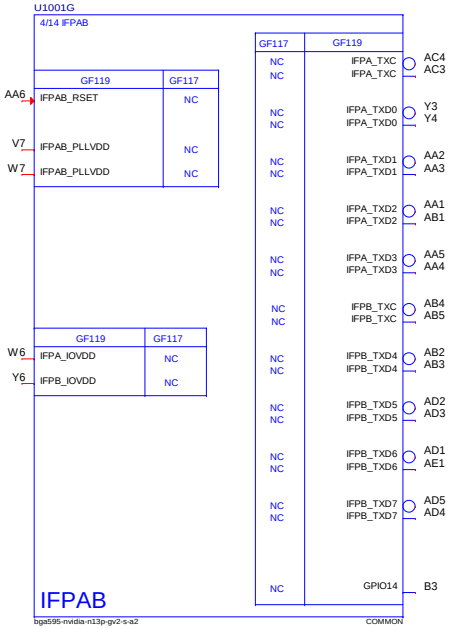
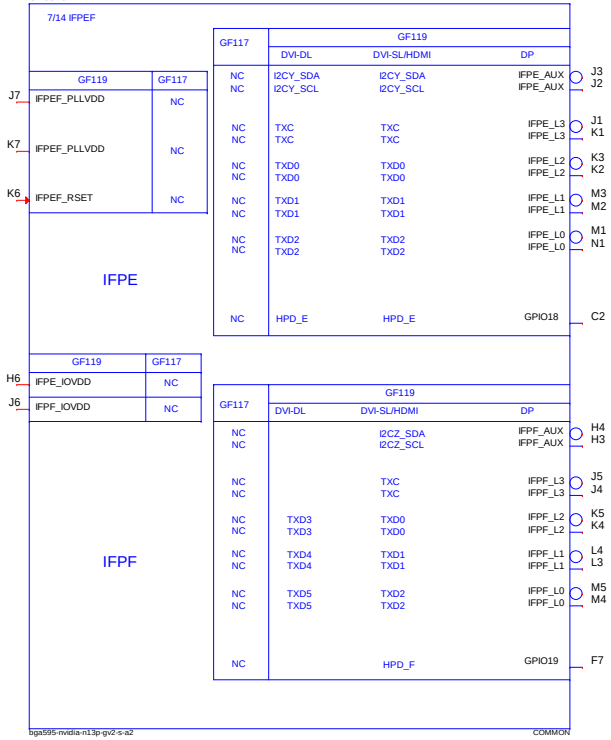
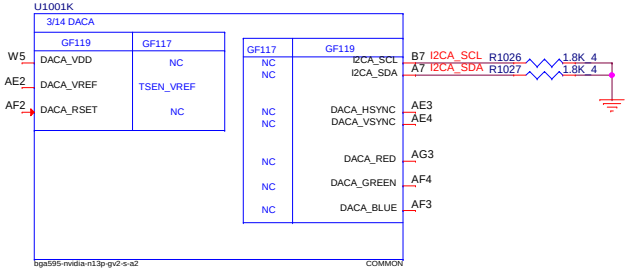
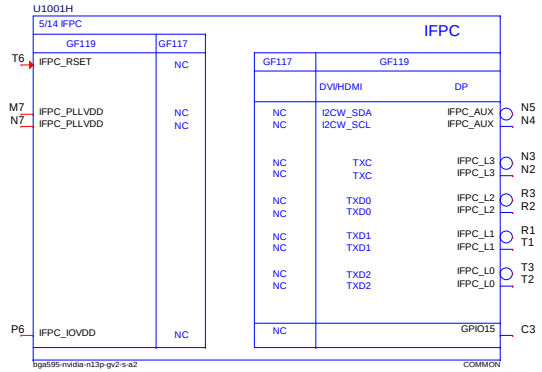
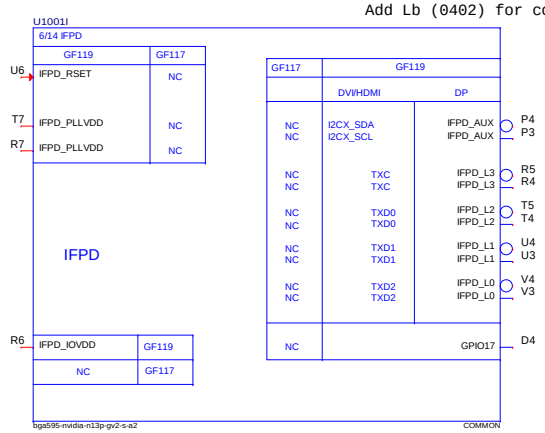


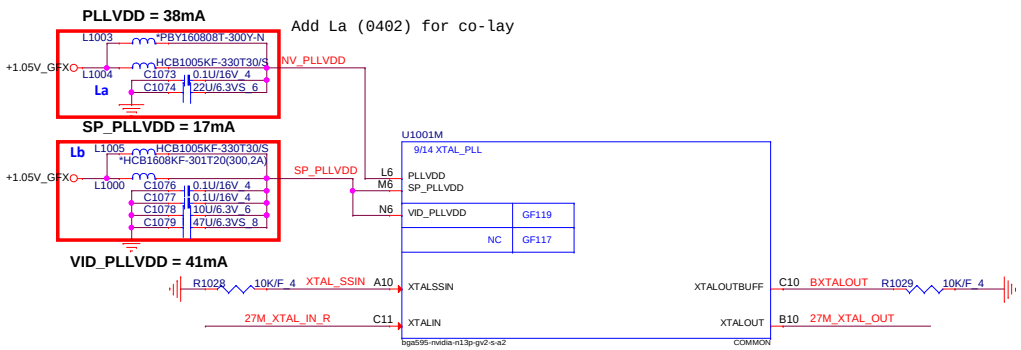


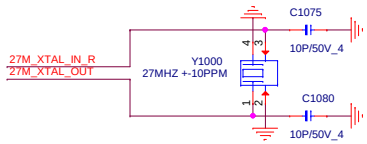


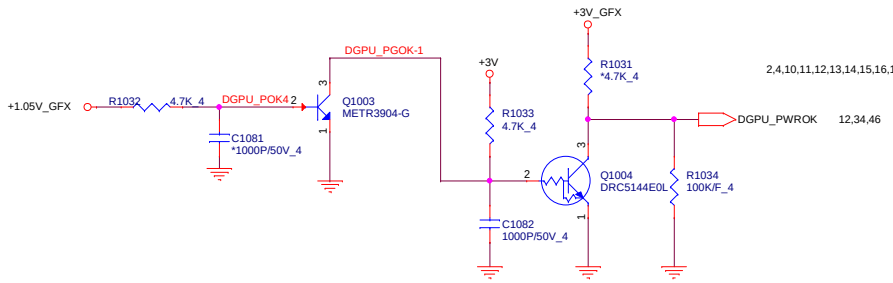


Add Lb (0402) for co-lay









19,20,47 +1.05V_GFX
19,22,45,47 +3V_GFX
19,22,47 +3V_AON
20,23,24,46 +1.5V_GFX
2,4,10,11,12,13,14,15,16,17,18,20,25,26,27,28,29,30,32,33,34,40,44,45 +3V

N85/RD3	**PROJECT : X12** Quanta Computer Inc.	
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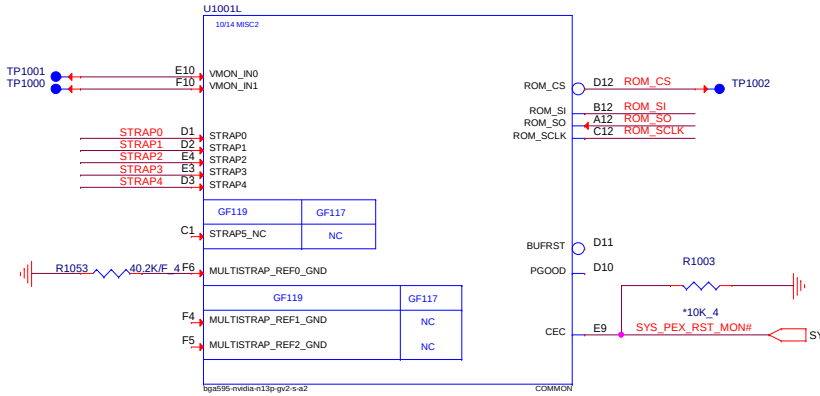

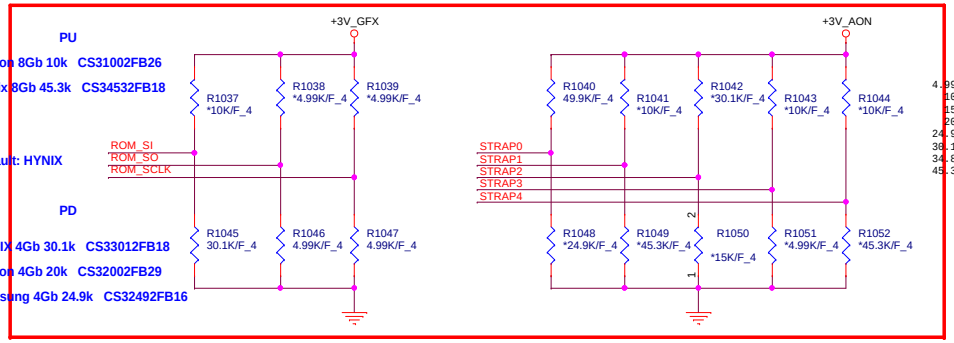

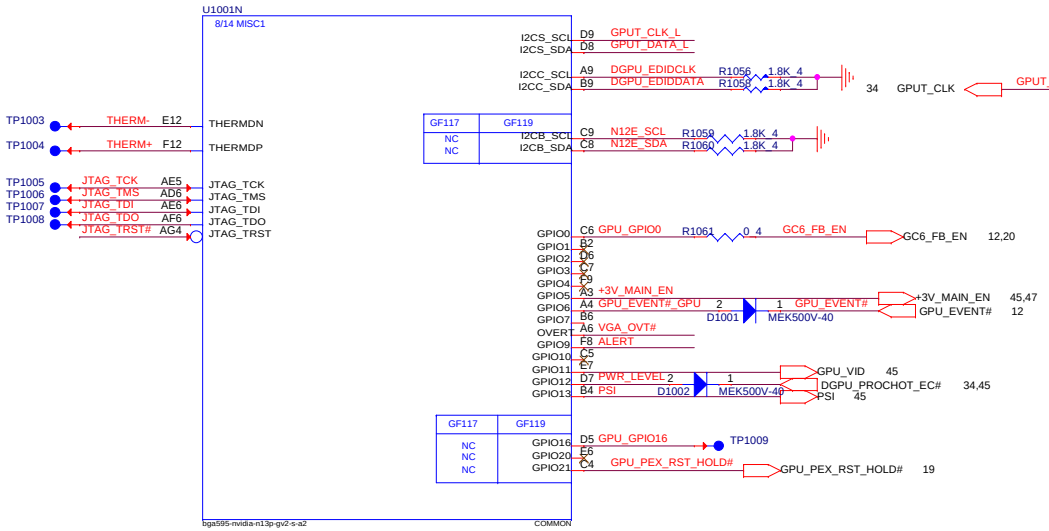

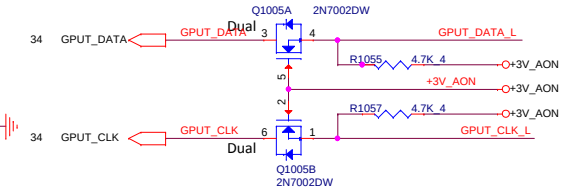

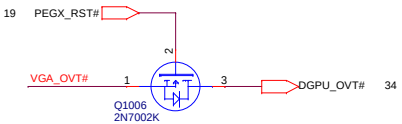

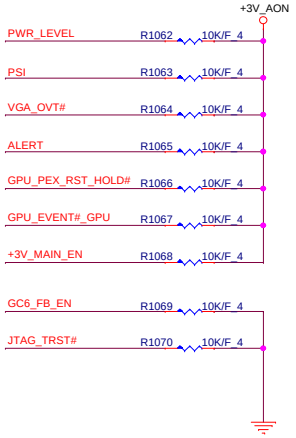

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

VRAM Configuration Table **ROM_SI S F**

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	Straping	TOP B/S	QBC
0000	...	...	...	...	...	...
0101	DDR3 256Mx16, 64bit, 4Gb,900MHz	HYNIX	H5TC4G63CFR-N0C	0x5	AKD5PZDTW01	AKD5PZDTW02
0011	DDR3 256Mx16, 64bit, 4Gb,900MHz	Micron	MT41J256M16LY-091G:N	0x3	AKD59GSTL01	AKD59GSTL00
0100	DDR3 256Mx16, 64bit, 4Gb,900MHz	SAMSUNG	K4W4G1646E-BC1A	0x4	AKD5PGDT500	AKD5PGDT501
1001	DDR3 512Mx16, 64bit, 4Gb,900MHz	Micron	MT41K512M16HA-107G:A	0x9	AKD50GSTL05	AKD50GSTL09
1111	DDR3 512Mx16, 64bit, 4Gb,900MHz	HYNIX	H5TC8G63CMR-11C	0xF	AKD5QFDTW00	AKD5QFDTW01

19,21,45,47 +3V_GFX
19,47 +3V_AON
20,23,24,46 +1.5V_GFX

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

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Rank0

U1004 — VRAM_DDR3_HYNIX_256MX16

U1005 — VRAM_DDR3_HYNIX_256MX16

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

stuff R1124 for
Hynix 8Gb DDP VRAM

stuff R1125 for
Hynix 8Gb DDP VRAM

reserve for Hynix 8Gb DDP VRAM

SDDR3_BGA100

	0..31	32..63
CMD0	CS0*	
CMD1	CS1*	
CMD2	ODT	
CMD3	CKE	
CMD16		CS0*
CMD17		CS1*
CMD18		ODT
CMD19		CKE

SNN_FBA0_ODT1	J1	NC/ODT1
SNN_FBA0_CKE1	J9	NC/CKE1
SNN_FBA0_CS1	L1	NC/CS1
SNN_FBA0_ZQ1	L9	NC/ZQ1

MicronVRAM-256Mx16 DDR3AKD59GSTL00IC SDRAM(96P)MT41J256M16LY-091G:N QBCON
MicronVRAM-256Mx16 DDR3AKD59GSTL01IC SDRAM(96P)MT41J256M16LY-091G:N TOPBSQ
HynixVRAM-256Mx16 DDR3AKD5PZDTW01IC SDRAM(96P)H5TC4G63CFR-N0C(FBGA)TOPBSQ
HynixVRAM-256Mx16 DDR3AKD5PZDTW02IC SDRAM(96P)H5TC4G63CFR-N0C(FBGA)QBCON

MicronVRAM-512Mx16 DDR3AKD5QGSTL09ICSDRAM(96P)MT41K512M16HA-107G:A QBCON
MicronVRAM-512Mx16 DDR3AKD5QGSTL05ICSDRAM(96)MT41K512M16HA-107G:ATOPDTBSQ
HynixVRAM-512Mx16 DDR3AKD5QFDTW00IC SDRAM(96P)H5TC8G63CMR-11C(FBGA)TOPBSQ
HynixVRAM-512Mx16 DDR3AKD5QFDTW01IC SDRAM(96P)H5TC8G63CMR-11C(FBGA)QBCON

20,24,46 +1.5V_GFX

NB5/RD3

PROJECT : X12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3L - RANK0	1A

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Rank0

1114SWAP

1114SWAP

1114SWAP

1114SWAP

U1006

U1007

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

stuff R1124 for
Hynix 8Gb DDP VRAM

stuff R1124 for
Hynix 8Gb DDP VRAM

MicronVRAM-256Mx16 DDR3AKD59GSTL00IC SDRAM(96P)MT41J256M16LY-091G:N QBCON
MicronVRAM-256Mx16 DDR3AKD59GSTL01IC SDRAM(96P)MT41J256M16LY-091G:N TOPBSQ
HynixVRAM-256Mx16 DDR3AKD5PZDTW01IC SDRAM(96P)H5TC4G63CFR-N0C(FBGA)TOPBSQ
HynixVRAM-256Mx16 DDR3AKD5PZDTW02IC SDRAM(96P)H5TC4G63CFR-N0C(FBGA)QBCON

MicronVRAM-512Mx16 DDR3AKD5QGSTL09ICSDRAM(96P)MT41K512M16HA-107G:A QBCON
MicronVRAM-512Mx16 DDR3AKD5QGSTL05ICSDRAM(96)MT41K512M16HA-107G:ATOPDTBSQ
HynixVRAM-512Mx16 DDR3AKD5QFDTW00IC SDRAM(96P)H5TC8G63CMR-11C(FBGA)TOPBSQ
HynixVRAM-512Mx16 DDR3AKD5QFDTW01IC SDRAM(96P)H5TC8G63CMR-11C(FBGA)QBCON

NB5/RD3

PROJECT : X12
Quanta Computer Inc.

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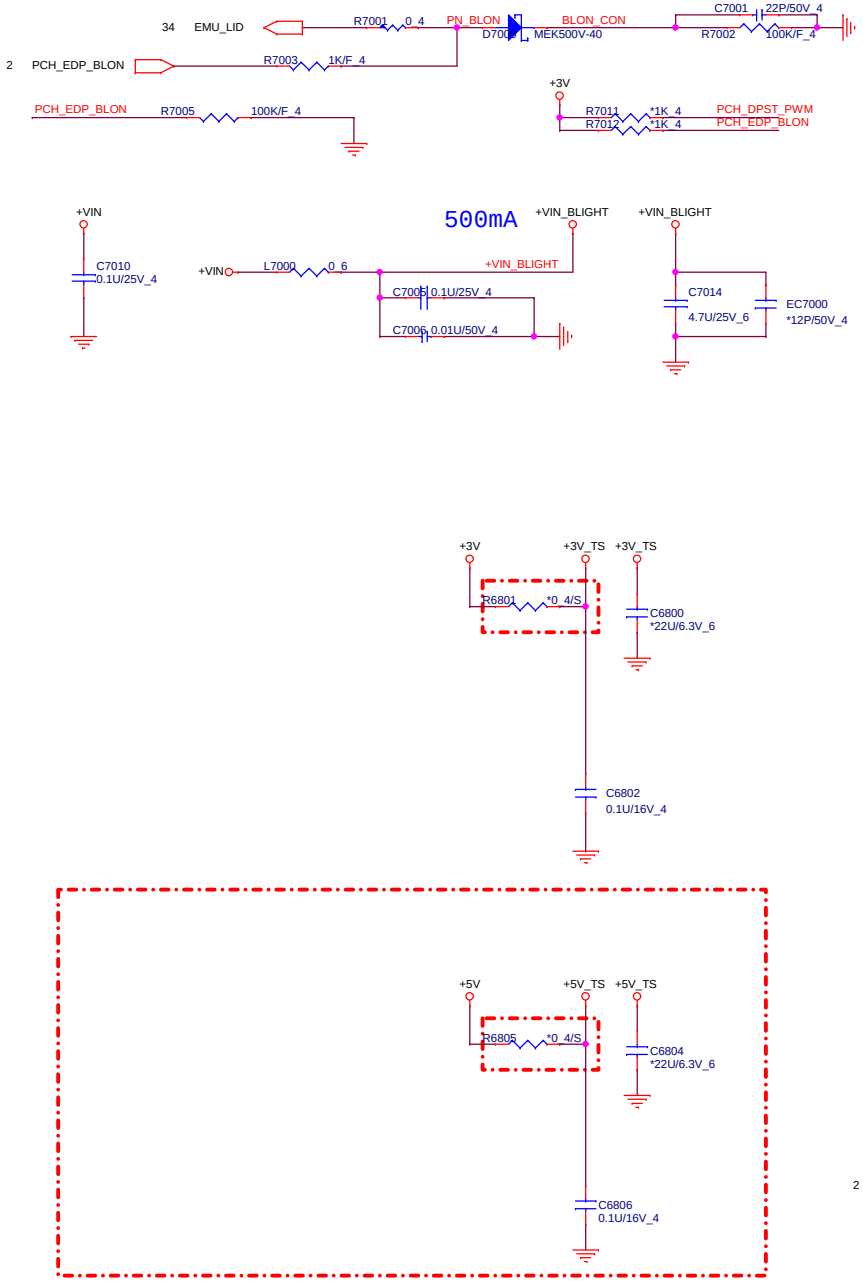
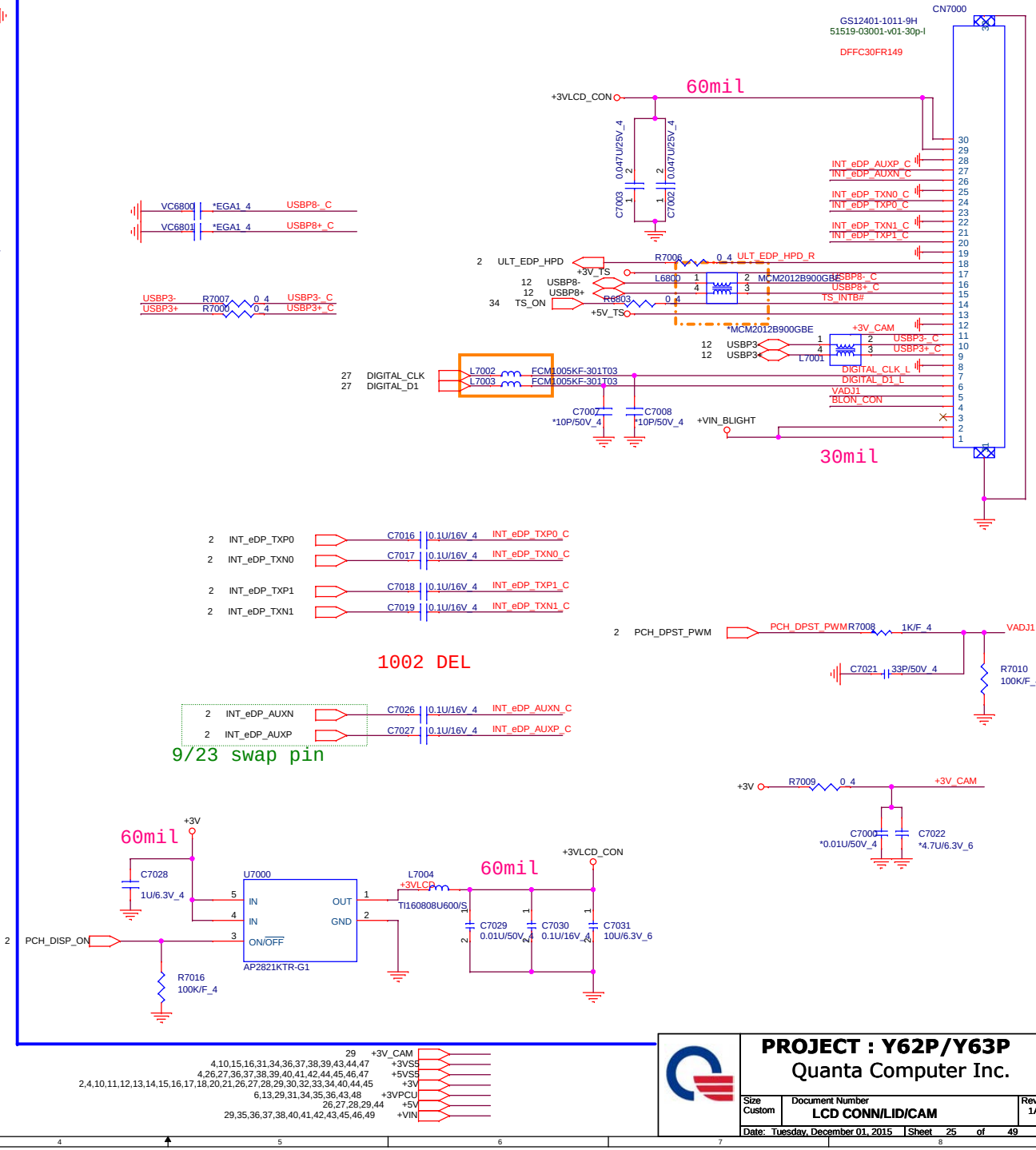
LID Switch



eDP Conn.



PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
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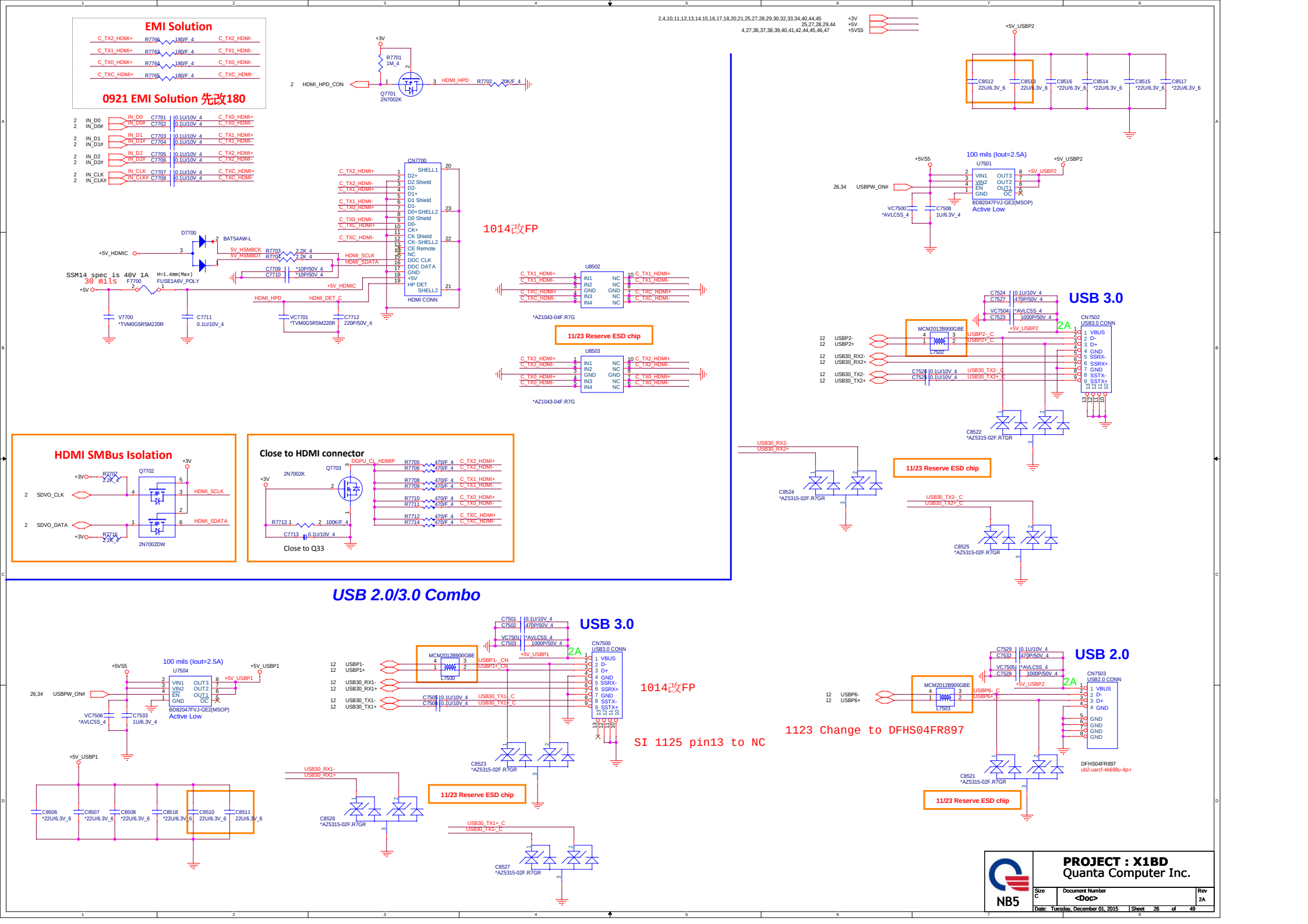
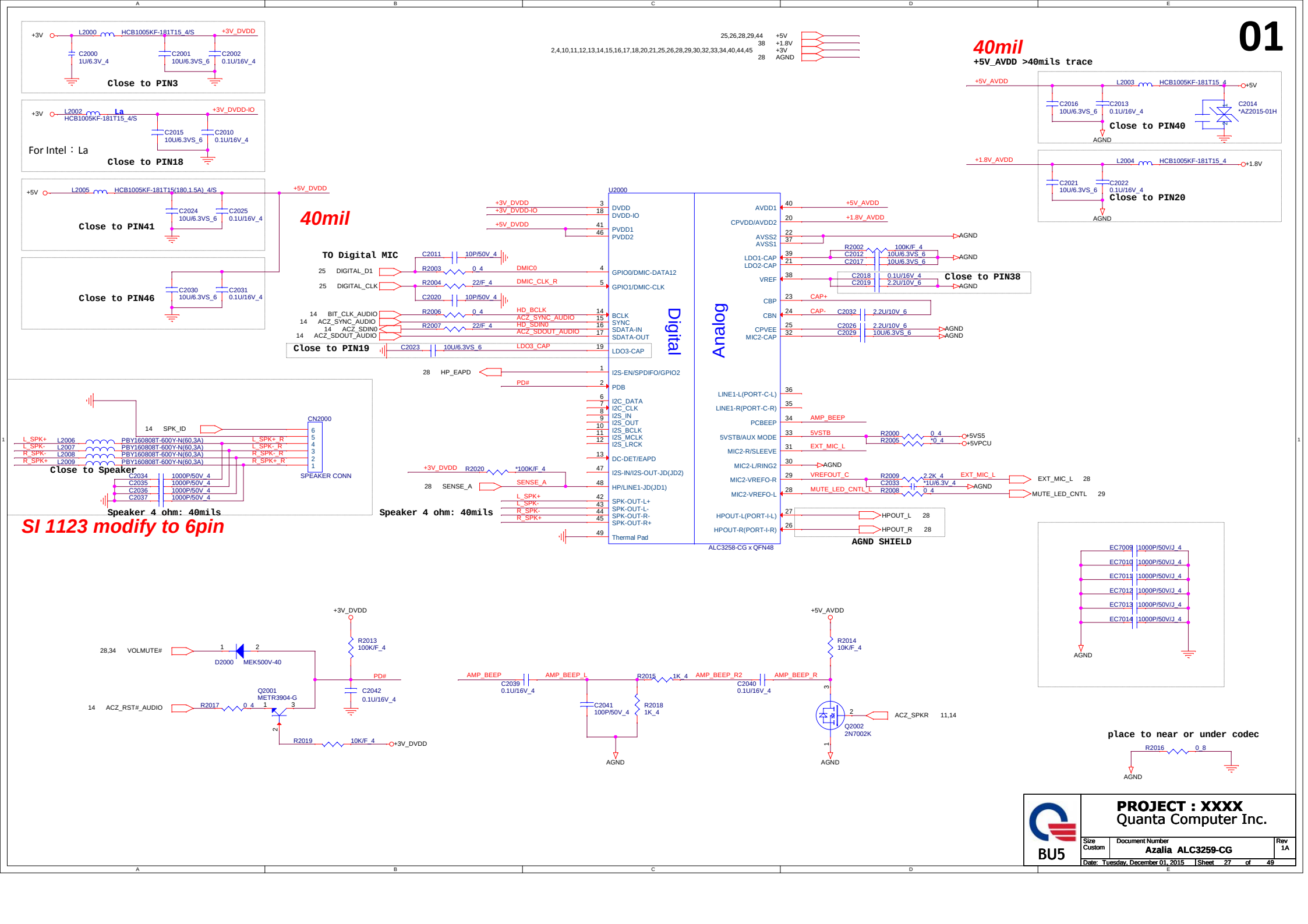

EMI Solution
0921 EMI Solution 先改180
1014改FP
11/23 Reserve ESD chip
HDMI SMBus Isolation
Close to HDMI connector
Close to Q33
USB 3.0
USB 2.0
USB 2.0/3.0 Combo
100 mils (Iout=2.5A)
Active Low
1123 Change to DFHS04FR897
SI 1125 pin13 to NC
PROJECT : X1BD
Quanta Computer Inc.
NB5


01
+3V L2000 HCB1005KF-181T15_4/S +3V_DVDD
C2000 1U/6.3V_4
C2001 10U/6.3VS_6
C2002 0.1U/16V_4
Close to PIN3
+3V L2002 La HCB1005KF-181T15_4/S +3V_DVDD-IO
C2015 10U/6.3VS_6
C2010 0.1U/16V_4
For Intel：La
Close to PIN18
+5V L2005 HCB1005KF-181T15(180,1.5A) 4/S +5V_DVDD
C2024 10U/6.3VS_6
C2025 0.1U/16V_4
Close to PIN41
C2030 10U/6.3VS_6
C2031 0.1U/16V_4
Close to PIN46
25,26,28,29,44 +5V
38 +1.8V
2,4,10,11,12,13,14,15,16,17,18,20,21,25,26,28,29,30,32,33,34,40,44,45 +3V
28 AGND
40mil
+5V_AVDD >40mils trace
+5V_AVDD L2003 HCB1005KF-181T15_4 +5V
C2016 10U/6.3VS_6
C2013 0.1U/16V_4
C2014 *AZ2015-01H
Close to PIN40
AGND
+1.8V_AVDD L2004 HCB1005KF-181T15_4 +1.8V
C2021 10U/6.3VS_6
C2022 0.1U/16V_4
Close to PIN20
AGND
40mil
TO Digital MIC
25 DIGITAL_D1 C2011 10P/50V_4 R2003 0_4 DMIC0
25 DIGITAL_CLK R2004 22/F_4 DMIC_CLK_R C2020 10P/50V_4
14 BIT_CLK_AUDIO R2006 0_4 HD_BCLK
14 ACZ_SYNC_AUDIO ACZ_SYNC_AUDIO
14 ACZ_SDIN0 R2007 22/F_4 HD_SDIN0
14 ACZ_SDOUT_AUDIO ACZ_SDOUT_AUDIO
Close to PIN19 C2023 10U/6.3VS_6 LDO3_CAP
U2000
+3V_DVDD +3V_DVDD-IO +5V_DVDD
3 DVDD
18 DVDD-IO
41 PVDD1
46 PVDD2
4 GPIO0/DMIC-DATA12
5 GPIO1/DMIC-CLK
14 BCLK
15 SYNC
16 SDATA-IN
17 SDATA-OUT
19 LDO3-CAP
Digital
28 HP_EAPD
1 I2S-EN/SPDIFO/GPIO2
PD#
2 PDB
6 I2C_DATA
7 I2C_CLK
8 I2S_IN
9 I2S_OUT
10 I2S_BCLK
11 I2S_MCLK
12 I2S_LRCK
13 DC-DET/EAPD
+3V_DVDD R2020 *100K/F_4
47 I2S-IN/I2S-OUT-JD(JD2)
28 SENSE_A SENSE_A
48 HP/LINE1-JD(JD1)
L_SPK+ L_SPK- R_SPK- R_SPK+
42 SPK-OUT-L+
43 SPK-OUT-L-
44 SPK-OUT-R-
45 SPK-OUT-R+
49 Thermal Pad
Analog
40 AVDD1 +5V_AVDD
20 CPVDD/AVDD2 +1.8V_AVDD
22 AVSS2
37 AVSS1 AGND
39 LDO1-CAP R2002 100K/F_4 C2012 10U/6.3VS_6
21 LDO2-CAP C2017 10U/6.3VS_6 AGND
38 VREF C2018 0.1U/16V_4 C2019 2.2U/10V_6 AGND
Close to PIN38
23 CBP CAP+
24 CBN CAP- C2032 2.2U/10V_6
25 CPVEE C2026 2.2U/10V_6 AGND
32 MIC2-CAP C2029 10U/6.3VS_6 AGND
36 LINE1-L(PORT-C-L)
35 LINE1-R(PORT-C-R)
34 PCBEEP AMP_BEEP
33 5VSTB/AUX MODE 5VSTB R2000 0_4 +5VS5 R2005 *0_4 +5VPCU
31 MIC2-R/SLEEVE EXT_MIC_L
30 MIC2-L/RING2 AGND
29 MIC2-VREFO-R VREFOUT_C R2009 2.2K_4 EXT_MIC_L C2033 *1U/6.3V_4 AGND EXT_MIC_L 28
28 MIC2-VREFO-L MUTE_LED_CNTL_L R2008 0_4 MUTE_LED_CNTL 29
27 HPOUT-L(PORT-I-L) HPOUT_L 28
26 HPOUT-R(PORT-I-R) HPOUT_R 28
AGND SHIELD
ALC3258-CG x QFN48
14 SPK_ID
L_SPK+ L2006 PBY160808T-600Y-N(60,3A) L_SPK+_R
L_SPK- L2007 PBY160808T-600Y-N(60,3A) L_SPK-_R
R_SPK- L2008 PBY160808T-600Y-N(60,3A) R_SPK-_R
R_SPK+ L2009 PBY160808T-600Y-N(60,3A) R_SPK+_R
CN2000
6 5 4 3 2 1
SPEAKER CONN
Close to Speaker
C2034 1000P/50V_4
C2035 1000P/50V_4
C2036 1000P/50V_4
C2037 1000P/50V_4
Speaker 4 ohm: 40mils
Speaker 4 ohm: 40mils
SI 1123 modify to 6pin
EC7009 1000P/50V/J_4
EC7010 1000P/50V/J_4
EC7011 1000P/50V/J_4
EC7012 1000P/50V/J_4
EC7013 1000P/50V/J_4
EC7014 1000P/50V/J_4
AGND
+3V_DVDD
28,34 VOLMUTE# D2000 MEK500V-40
R2013 100K/F_4
PD#
C2042 0.1U/16V_4
14 ACZ_RST#_AUDIO R2017 0_4 Q2001 METR3904-G
R2019 10K/F_4 +3V_DVDD
+5V_AVDD
R2014 10K/F_4
AMP_BEEP C2039 0.1U/16V_4 AMP_BEEP_L R2015 1K_4 AMP_BEEP_R2 C2040 0.1U/16V_4 AMP_BEEP_R
C2041 100P/50V_4
R2018 1K_4
Q2002 2N7002K
ACZ_SPKR 11,14
AGND
place to near or under codec
R2016 0_8
AGND
PROJECT : XXXX
Quanta Computer Inc.
BU5
Size Custom
Document Number Azalia ALC3259-CG
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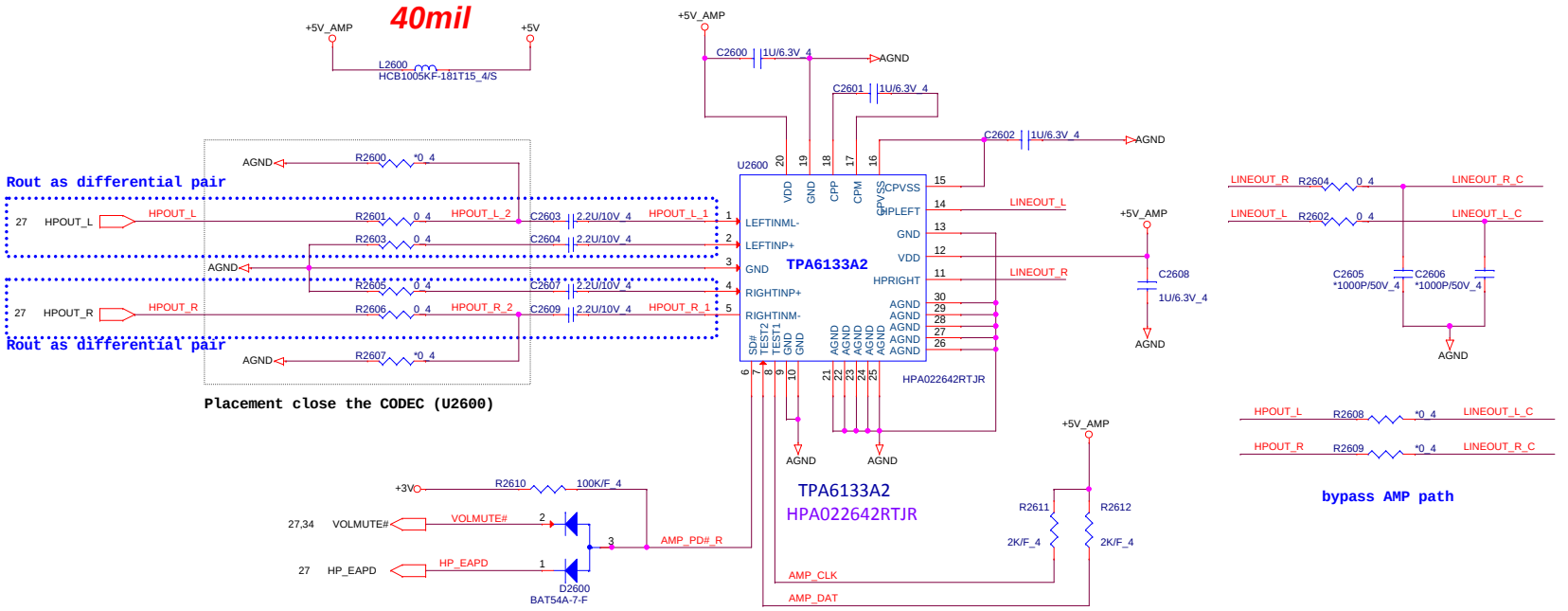
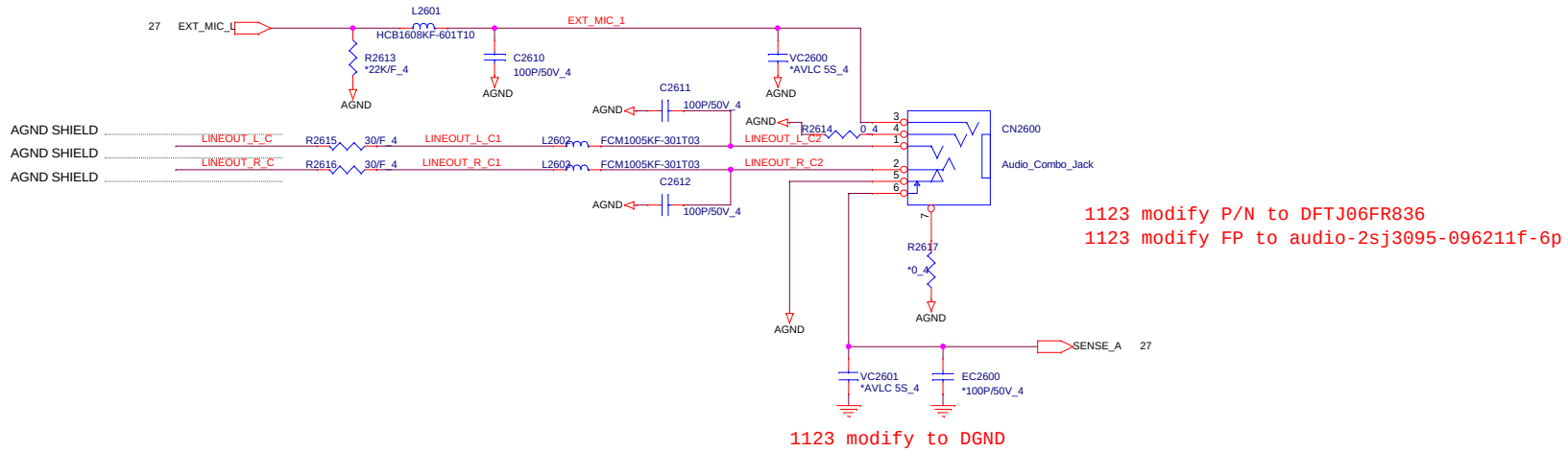
Head Phone out

25,26,27,29,44 +5V
27 AGND



Audio Combo



1123 modify P/N to DFTJ06FR836
1123 modify FP to audio-2sj3095-096211f-6p

1123 modify to DGND

BU5

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Quanta Computer Inc.

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Custom	HP AMP HPA022642RTJR	1A

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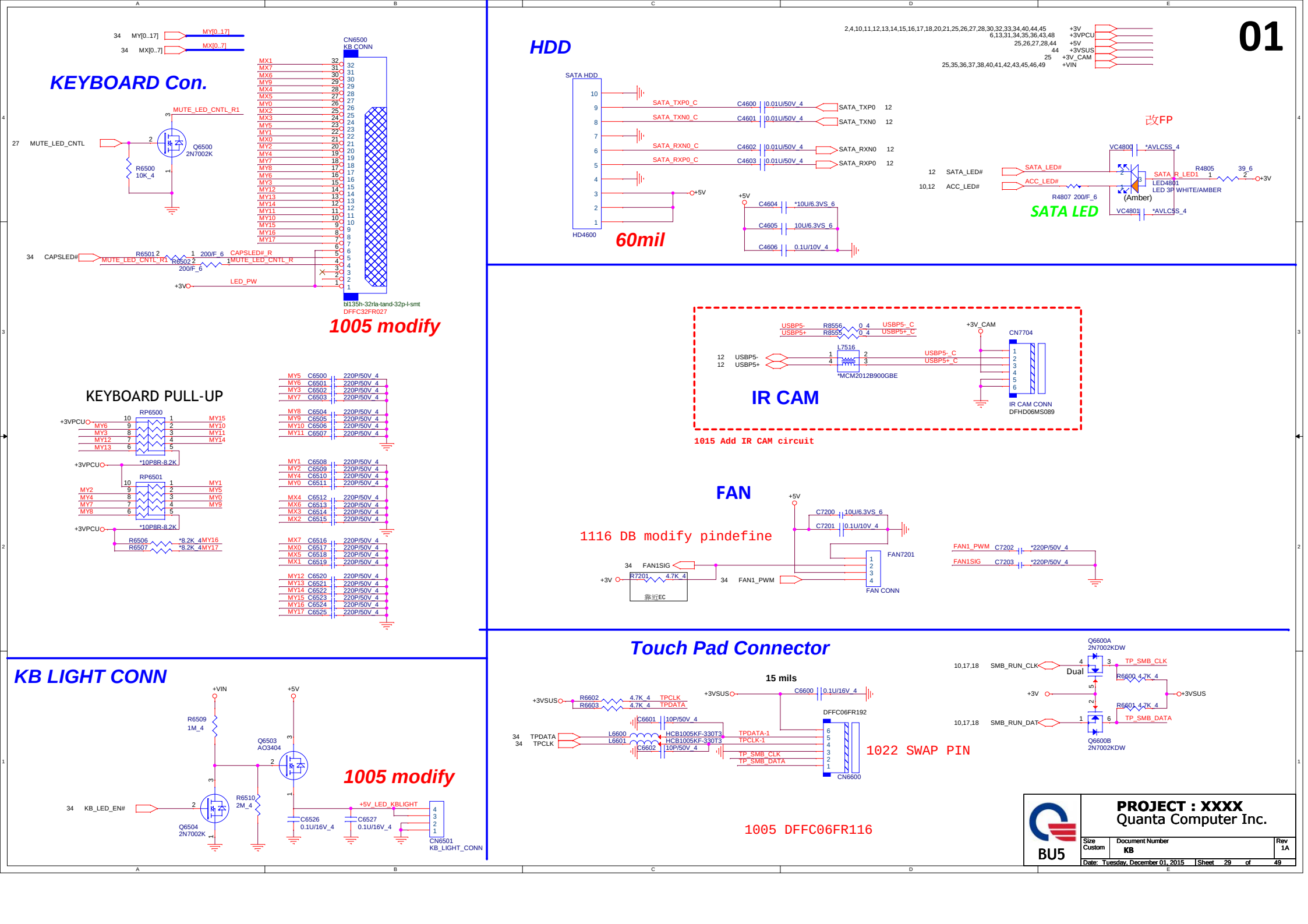
KEYBOARD Con.
CN6500
KB CONN
MUTE_LED_CNTL_R1
MUTE_LED_CNTL
Q6500
2N7002K
R6500
10K_4
CAPSLED#
CAPSLED#_R
LED_PW
+3V
bl135h-32rla-tand-32p-l-smt
DFFC32FR027
1005 modify
KEYBOARD PULL-UP
RP6500
RP6501
*10P8R-8.2K
R6506
R6507
*8.2K_4
KB LIGHT CONN
+VIN
+5V
R6509
1M_4
Q6503
AO3404
R6510
2M_4
Q6504
2N7002K
KB_LED_EN#
+5V_LED_KBLIGHT
C6526
0.1U/16V_4
C6527
0.1U/16V_4
CN6501
KB_LIGHT_CONN
1005 modify
HDD
SATA HDD
HD4600
SATA_TXP0_C
SATA_TXN0_C
SATA_RXN0_C
SATA_RXP0_C
C4600
C4601
C4602
C4603
0.01U/50V_4
SATA_TXP0
SATA_TXN0
SATA_RXN0
SATA_RXP0
C4604
C4605
C4606
*10U/6.3VS_6
10U/6.3VS_6
0.1U/10V_4
60mil
+3V
+3VPCU
+5V
+3VSUS
+3V_CAM
+VIN
改FP
VC4800
*AVLC5S_4
SATA_LED#
ACC_LED#
SATA_R_LED1
R4805
39_6
LED4801
LED 3P WHITE/AMBER
(Amber)
R4807 200/F_6
VC4801
SATA LED
IR CAM
USBP5-
USBP5+
R8556
R8557
USBP5-_C
USBP5+_C
L7516
*MCM2012B900GBE
CN7704
IR CAM CONN
DFHD06MS089
1015 Add IR CAM circuit
FAN
1116 DB modify pindefine
C7200
C7201
FAN7201
FAN CONN
FAN1SIG
FAN1_PWM
R7201
4.7K_4
靠近EC
C7202
C7203
*220P/50V_4
Touch Pad Connector
15 mils
R6602
R6603
TPCLK
TPDATA
C6600
0.1U/16V_4
C6601
10P/50V_4
L6600
L6601
HCB1005KF-330T3
C6602
TPDATA-1
TPCLK-1
TP_SMB_CLK
TP_SMB_DATA
DFFC06FR192
CN6600
1022 SWAP PIN
1005 DFFC06FR116
Q6600A
2N7002KDW
Dual
Q6600B
2N7002KDW
SMB_RUN_CLK
SMB_RUN_DAT
R6600 4.7K_4
R6601 4.7K_4
01
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Quanta Computer Inc.
BU5
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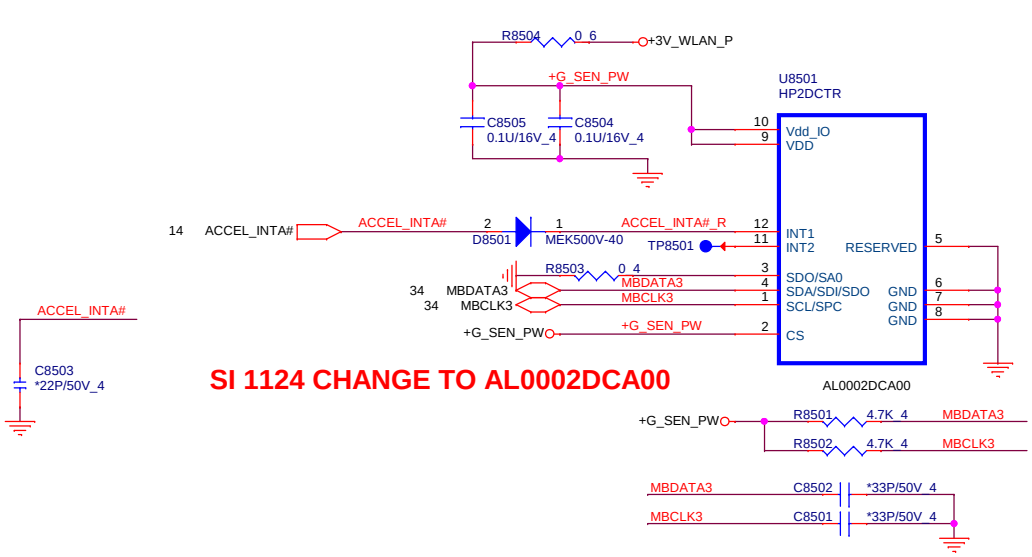
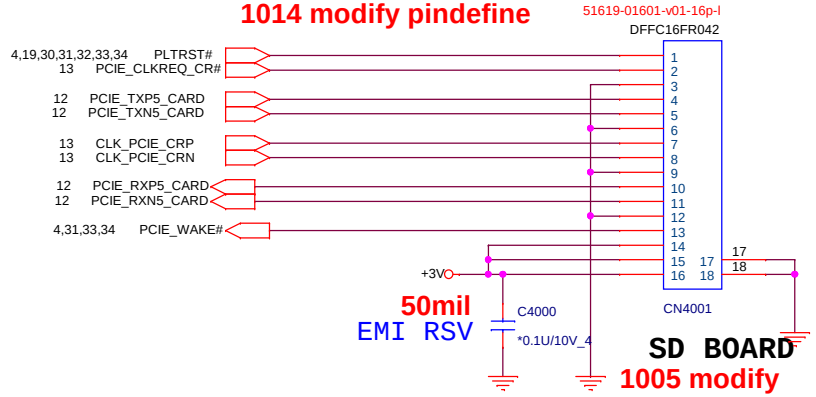
Accelerometer Sensor



1014 modify pindefine



31 +3V_WLAN_P
2,4,10,11,12,13,14,15,16,17,18,20,21,25,26,27,28,29,32,33,34,40,44,45 +3V

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Size B	Document Number <Doc>	Rev <RevCode>
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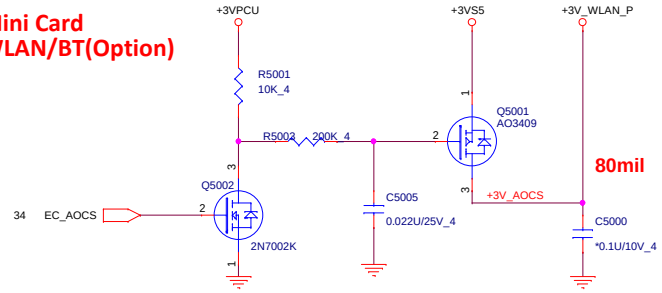
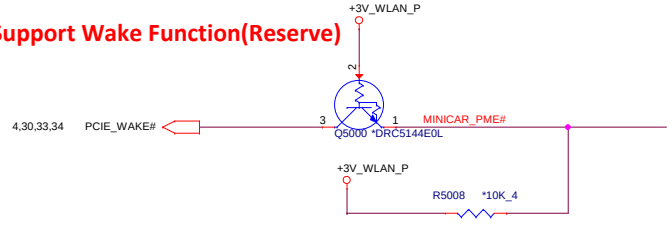
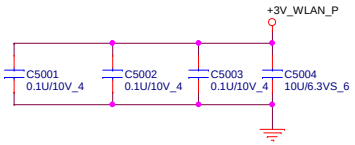
Mini Card WLAN/BT(Option)



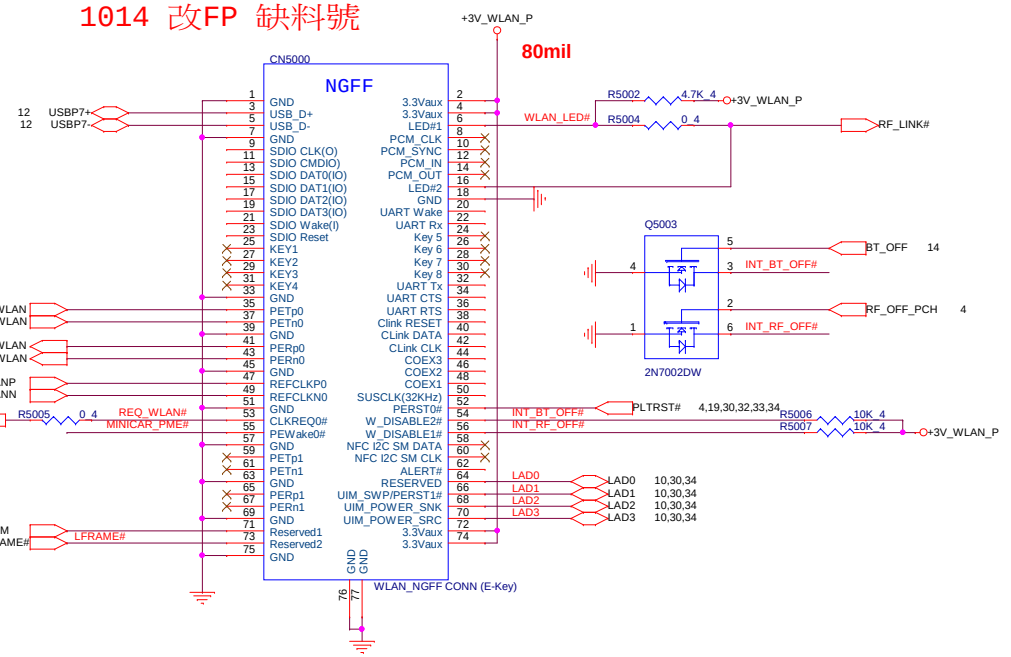
Support Wake Function(Reserve)



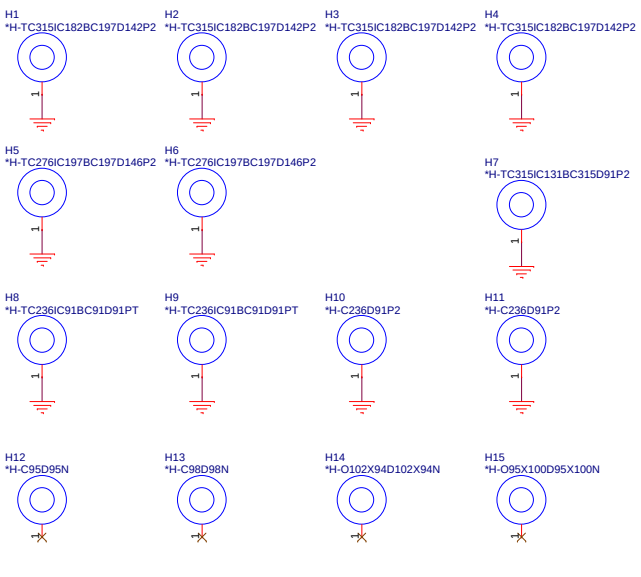
need check module spec

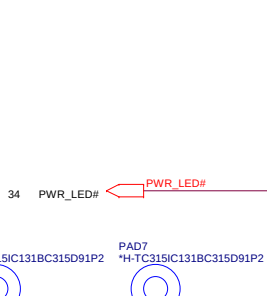


1014 改FP 缺料號

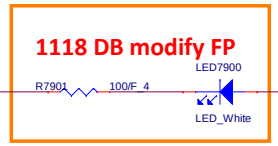


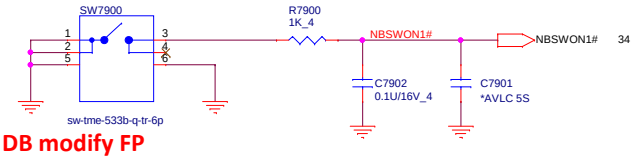
PAD/HOLE

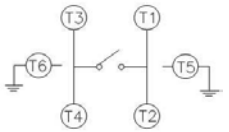


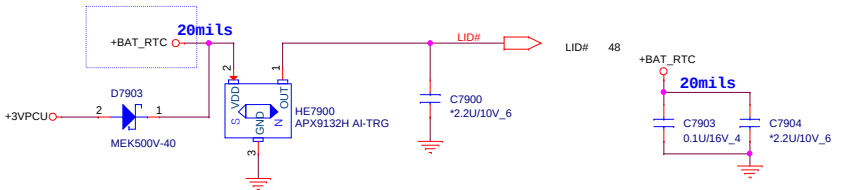


1118 DB modify FP

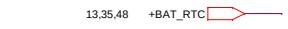








1118 change to M2 MBZRQ001010



NB5	**PROJECT : X1BD** Quanta Computer Inc.	
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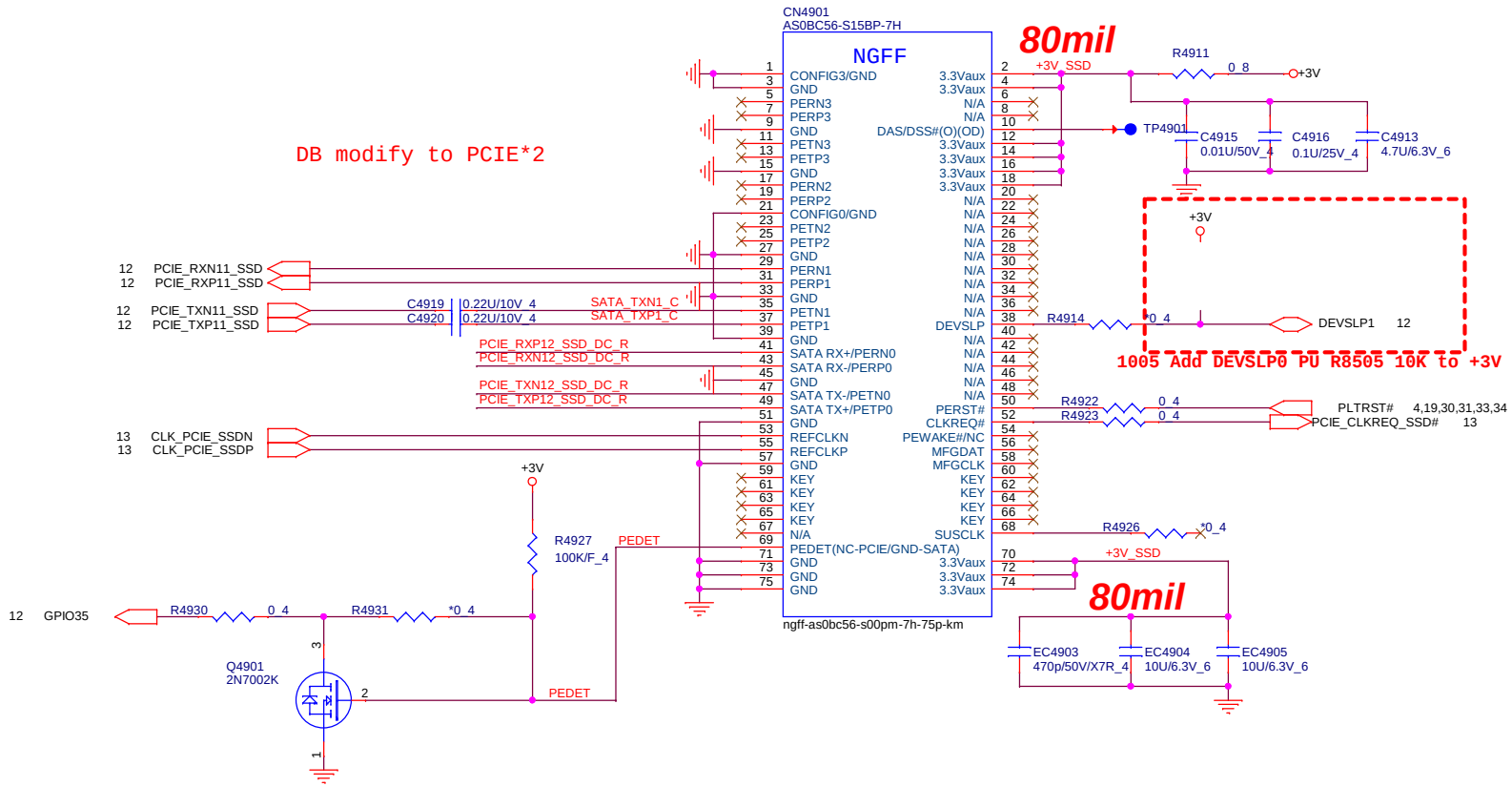

Quanta Computer Inc.		
PROJECT : PS8527A		
Size	Document Number	Rev
	SATA3.0 redriver	
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LAN & RJ45

01

For SWR mode support RTL8111HSH/RTL8107ESH

Stuff La, Ca ,Cb

* Place Cc,Cd,Ce,Cf for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 3, 22, 8 , 30

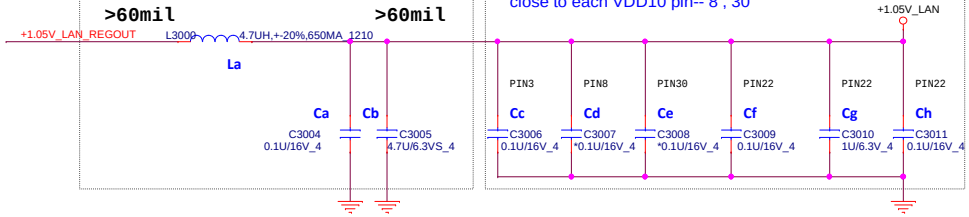
* Place Cg,Ch for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 22(reserved)

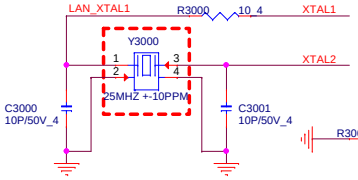
* Place Cq,Cr for RTL8166EH close to each VDD10 pin-- 30(reserved)

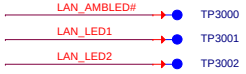
* Place Ce,Cd for RTL8166EH close to each VDD10 pin-- 8 , 30

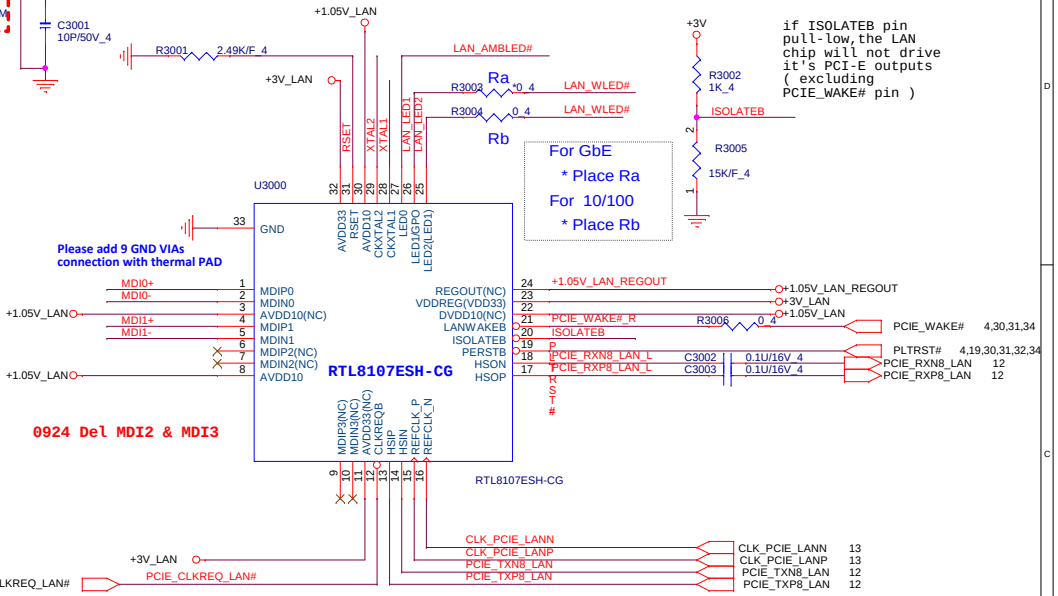
Power trace Layout 寬度> 60mil

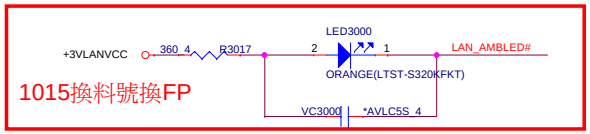
>60mil >60mil





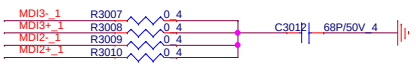






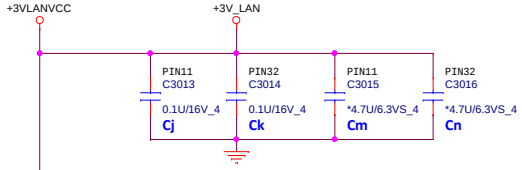
For 10/100 stuff only

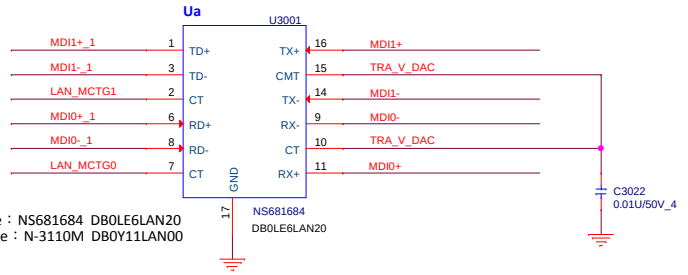
Close RJ45



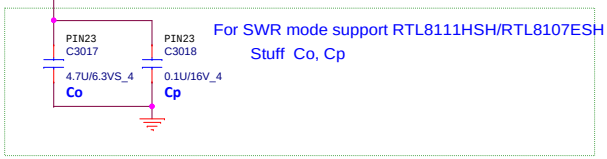
* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8111H(S) & RTL8107E(S)

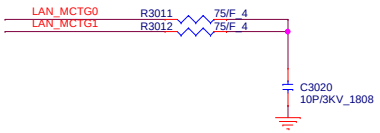
* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)



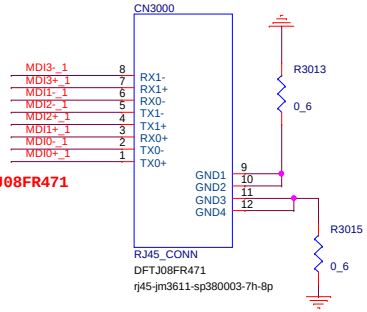


1st source：NS681684 DB0LE6LAN20
2nd source：N-3110M DB0Y11LAN00





RJ45



1127 Change P/N to DFTJ08FR471

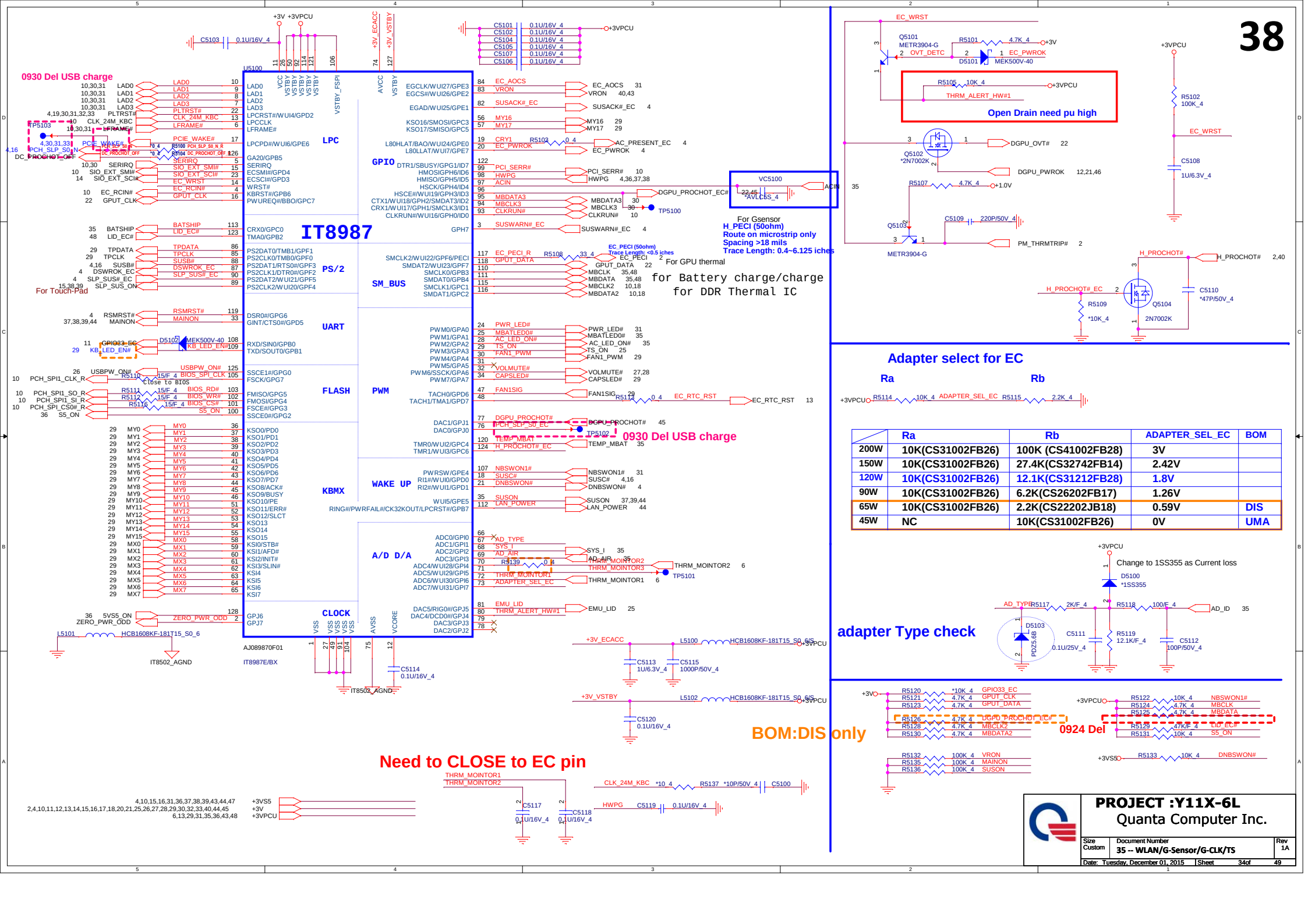
2,4,10,11,12,13,14,15,16,17,18,20,21,25,26,27,28,29,30,32,34,40,44,45

44 +3V +3VLANVCC

BU5

PROJECT : XXXX
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN RTL8107ESH-CG/RJ45	1A
Date: Tuesday, December 01, 2015	Sheet 33 of 49	



	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002FB26)	100K (CS41002FB28)	3V	
150W	10K(CS31002FB26)	27.4K(CS32742FB14)	2.42V	
120W	10K(CS31002FB26)	12.1K(CS31212FB28)	1.8V	
90W	10K(CS31002FB26)	6.2K(CS26202FB17)	1.26V	
65W	10K(CS31002FB26)	2.2K(CS22202JB18)	0.59V	DIS
45W	NC	10K(CS31002FB26)	0V	UMA

PROJECT :Y11X-6L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	35 -- WLAN/G-Sensor/G-CLK/TS	1A
Date: Tuesday, December 01, 2015	Sheet 34of 49	

+3VPCU 6,13,29,31,34,35,36,43,48
+5VPCU 27,36,44,47
+BAT_RTC 4,13,15,31,48
+VIN 25,29,36,37,38,40,41,42,43,45,46,47,49
+3VPCU 6,13,29,31,34,35,36,43,48

DC_JACK/65W

Do Not add test pad on BATDIS_G signal

Place this ZVS close to Diode away +VIN

+BAT_RTC
1S---10-ohm
>2S---100ohm

14"

2015/10/23 updated

2015/10/5 updated

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this R&C close to EC

Place this cap close to EC

VIN>22.5V (AC OVP)
VIN>17.2V (Enable Charging)
VIN>15.2V (AC present)

Vacdet=2.4V

Notes:
For 4S pack
Stuff Block A + Ra
Ra = 69.8K (P/N:CS36982FB11)

MIN. BATV=7.2V

Size Custom	Document Number Charger(BQ24738H)		Rev 1A
Date Tuesday, December 01, 2015	Sheet 35 of 49		

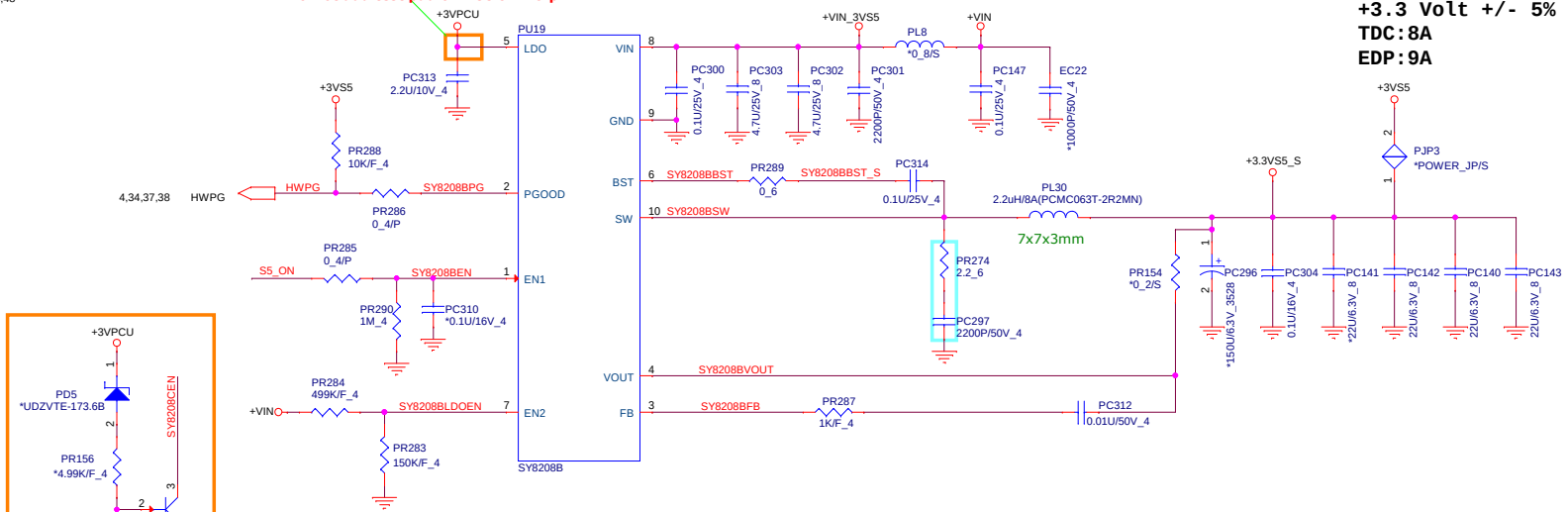
NB5

PROJECT : X1Q
Quanta Computer Inc.

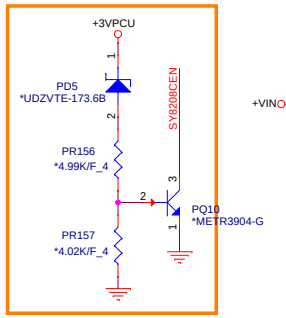
DC/DC +3VS5/+5VS5

+VIN 25,29,35,37,38,40,41,42,43,45,46,47,49
+3VS5 4,10,15,16,25,31,34,37,38,39,43,44,47
+5VS5 4,25,26,27,37,38,39,40,41,42,44,45,46,47
+3VPCU 6,13,29,31,34,35,43,48
+5VPCU 27,35,44,47

Do Not add test pad on VCC & LDO pin

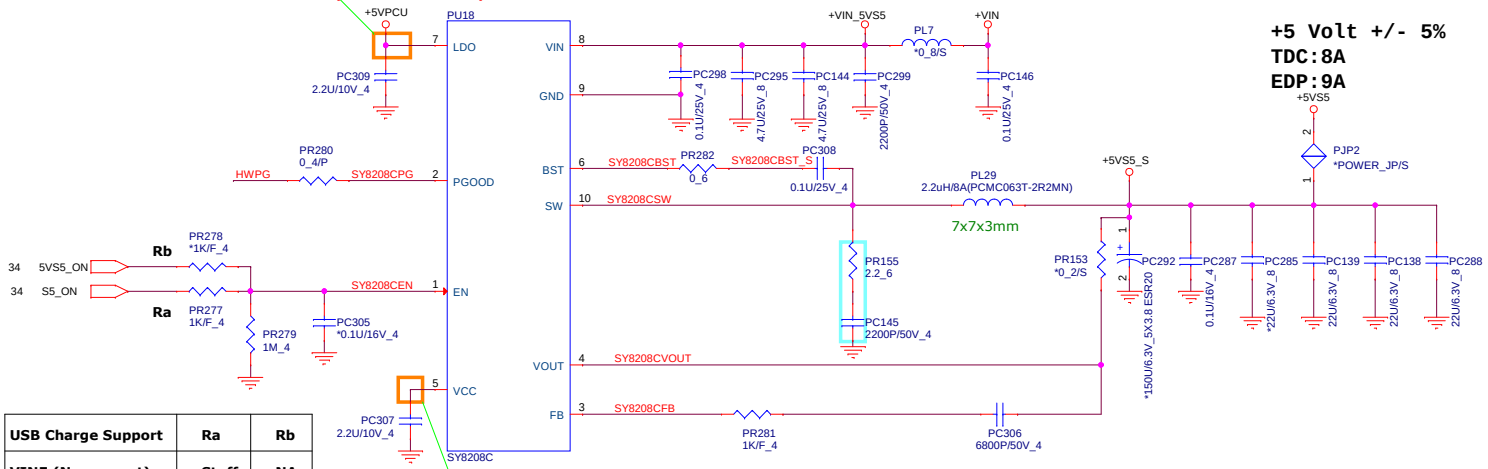


+3.3 Volt +/- 5%
TDC:8A
EDP:9A



2014/12/12 updated

Do Not add test pad on VCC & LDO pin



+5 Volt +/- 5%
TDC:8A
EDP:9A

USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

Do Not add test pad on VCC & LDO pin

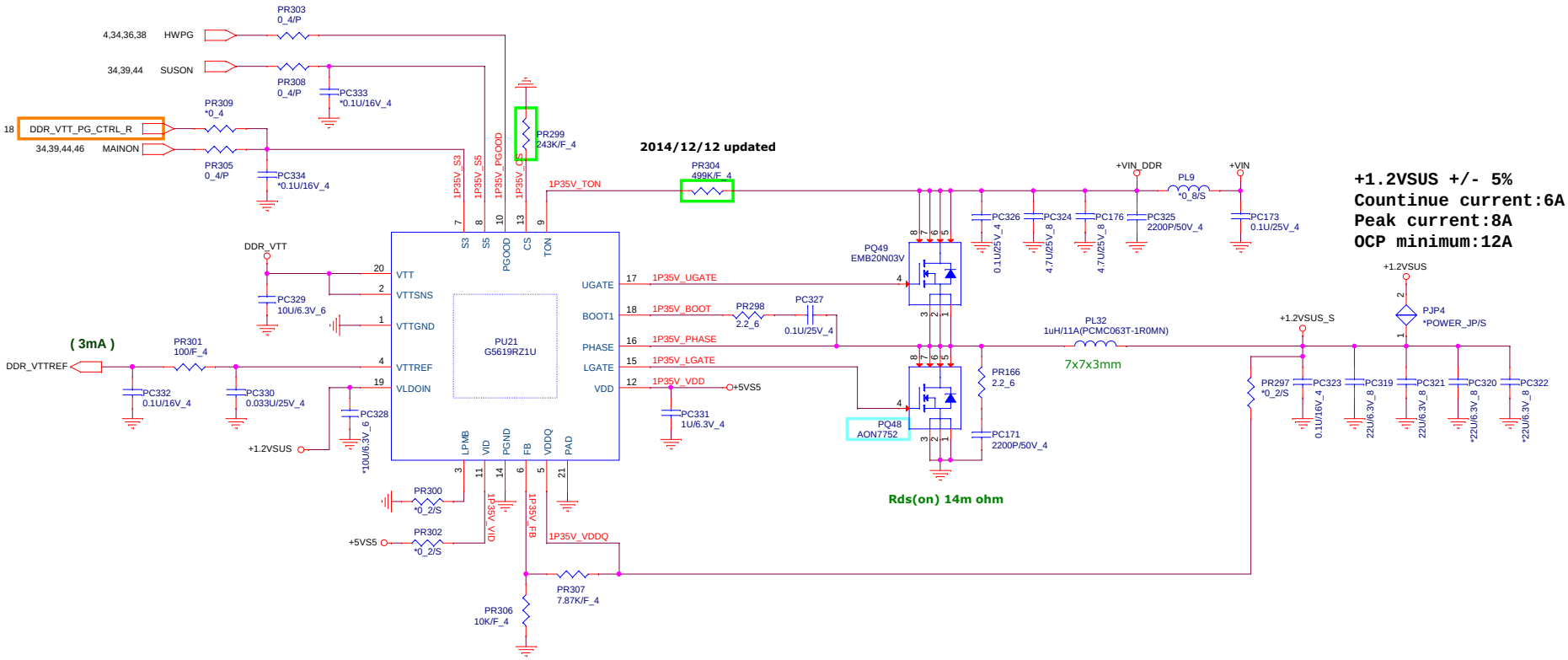
NB5

PROJECT : X1Q
Quanta Computer Inc.

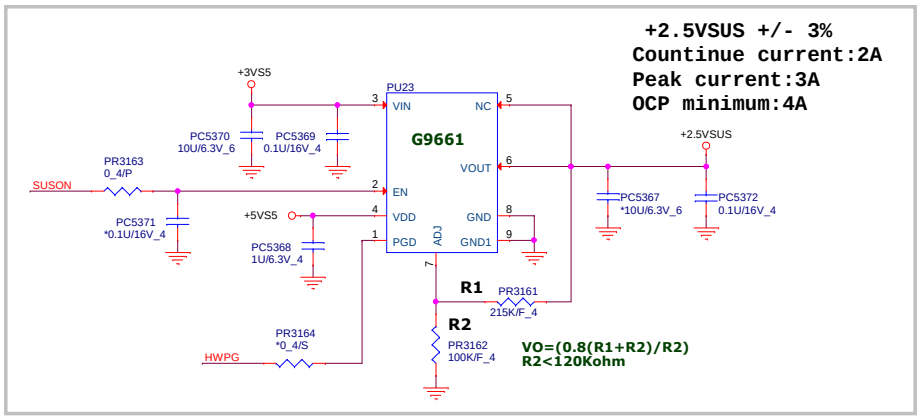
Size	Document Number	Rev
Custom	3/5VPCU(RT8243A)	1A

Date: Tuesday, December 01, 2015 Sheet 36 of 49

+VIN 25,29,35,36,38,40,41,42,43,45,46,47,49
+5VS5 4,25,26,27,36,38,39,40,41,42,44,45,46,47
+1.2VSUS 3,6,17,18,39,47
DDR_VTT 17,18



20151015 updated

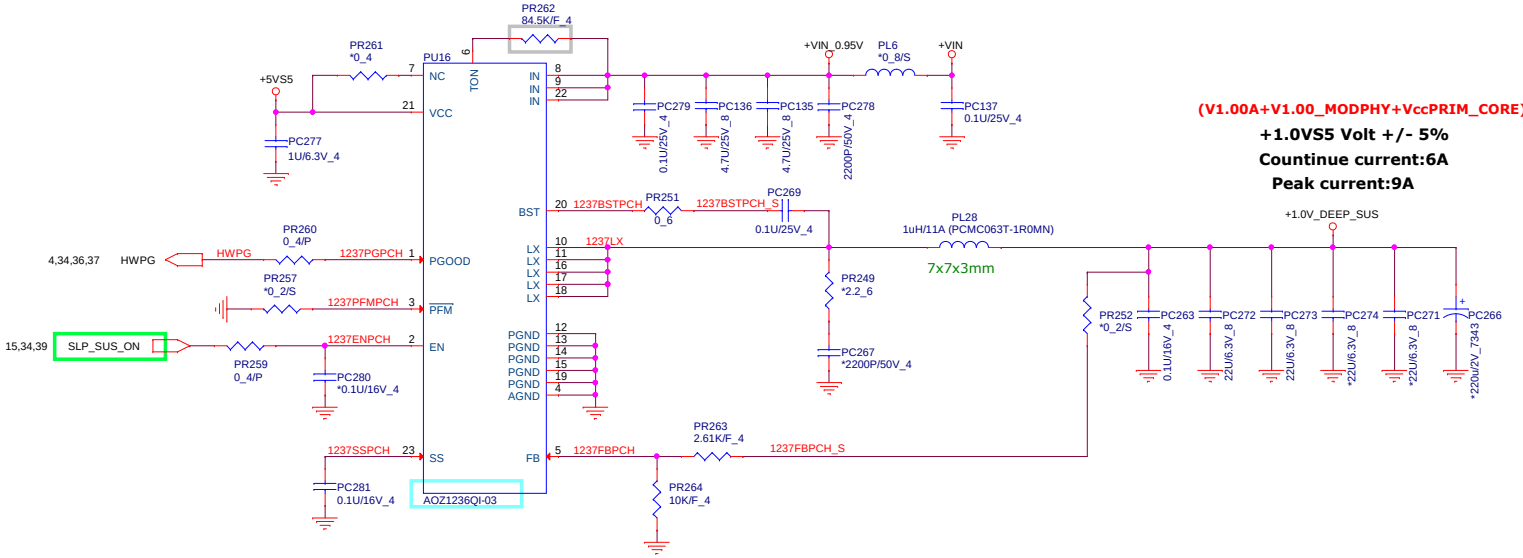


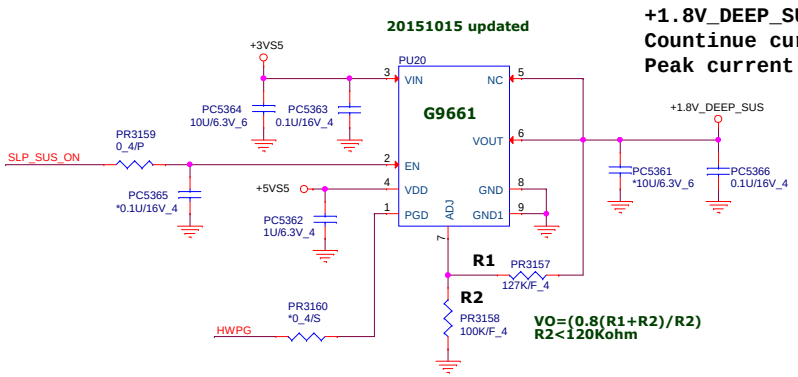
PROJECT : X1Q
Quanta Computer Inc.

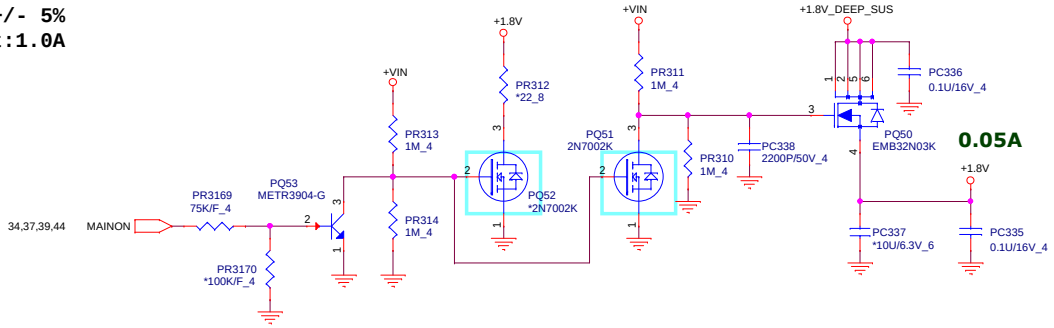
Size	Document Number	Rev
	DDR3 (RT8231B)/1.8VS5	1A

NB5
Tuesday, December 01, 2015
Sheet 37 of 49

+VIN 25,29,35,36,37,40,41,42,43,45,46,47,49
+3VS5 4,10,15,16,25,31,34,36,37,39,43,44,47
+5VS5 4,25,26,27,36,37,39,40,41,42,44,45,46,47
+1.0V_DEEP_SUS 9,13,15,39
+1.8V_DEEP_SUS 5,9,15,46
MAINON 34,37,39,44,46
+1.5V







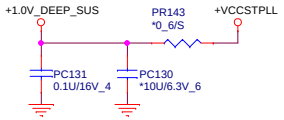
NB5	**PROJECT : X1Q** Quanta Computer Inc.	
Size Custom	Document Number +1.1VS5 (RT8228)/2.5V	Rev 1A
Date: Tuesday, December 01, 2015	Sheet 38 of 49	

+1.0V 2,4,6,34
+3VS5 4,10,15,16,25,31,34,36,37,38,43,44,47
+5VS5 4,25,26,27,36,37,38,40,41,42,44,45,46,47
+VCCIO 2,6
+1.2VSUS 3,6,17,18,37,47
+VCCSTPLL 2,4,5,6,9,40
+1.0V_DEEP_SUS 9,13,15,38
+1.2V_VCCPLL_OC 6
MAINON 34,37,44,46

Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

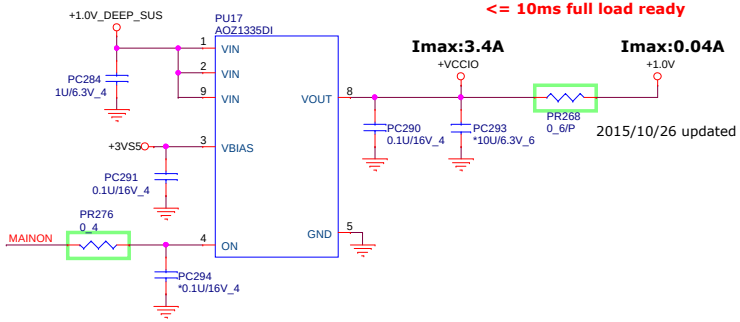
Imax:0.24A



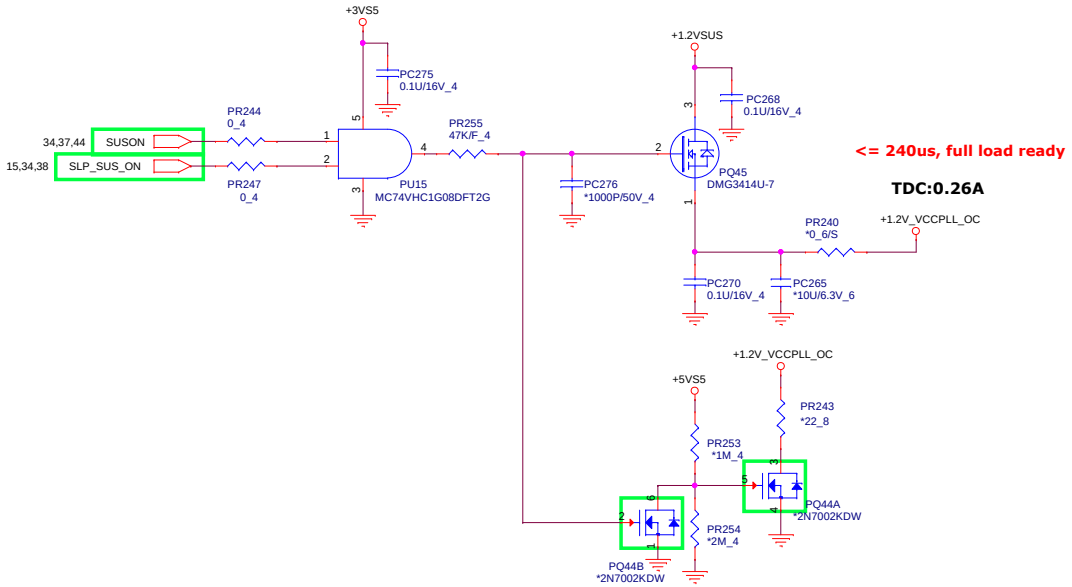
Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 3.4A

<= 10ms full load ready

Imax:3.4A **Imax:0.04A**



2015/10/26 updated

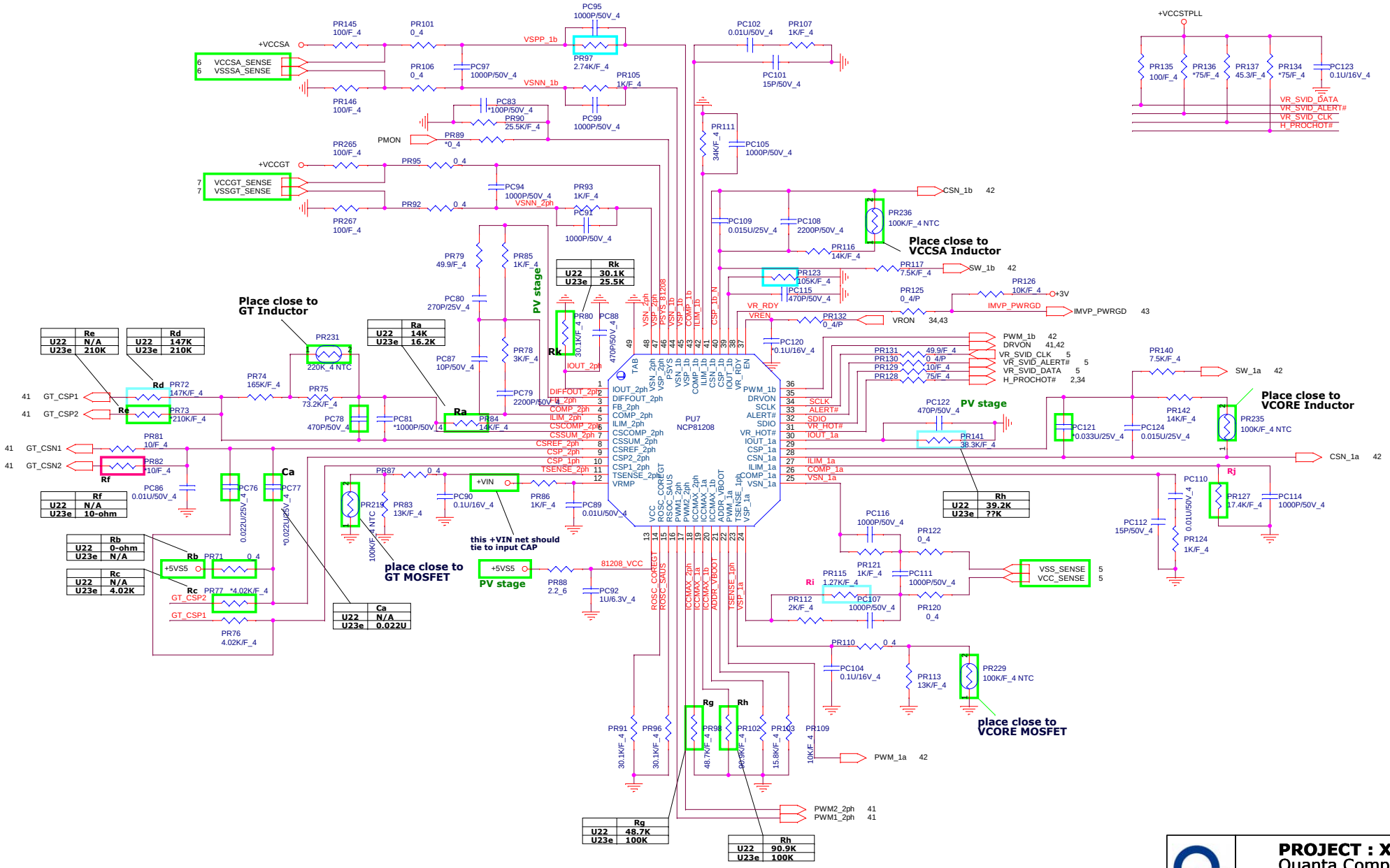


<= 240us, full load ready

TDC:0.26A

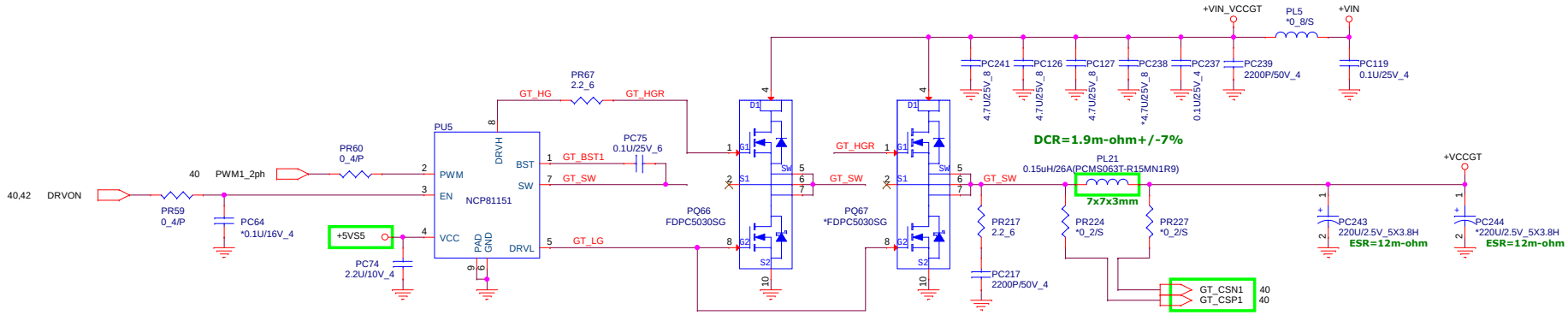
NB5	**PROJECT : X1Q** Quanta Computer Inc.	
Size: Custom	Document Number: +1.0V/+VCCSTPLL	Rev: 1A
Date: Tuesday, December 01, 2015	Sheet 39 of 49	

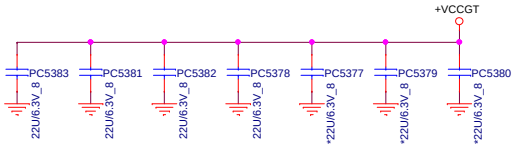
+3V 2,4,10,11,12,13,14,15,17,18,19,20,21,25,26,27,28,29,30,32,33,34,44,45
+5V 25,26,27,28,29,44
+VIN 25,29,35,36,37,38,41,42,43,45,46,47,49
+5VPCU 27,35,36,44,47
+VCCSA 6,42
+VCCGT 7,41
+VCCSTPLL 2,4,5,6,9,39



PROJECT : X1Q	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: CPU VR IC (NCP81206)
Rev: 2A	
Date: Tuesday, December 01, 2015	Sheet 40 of 49

+5V 25,26,27,28,29,44
+VIN 25,29,35,36,37,38,40,42,43,45,46,47,49
+5VPCU 27,35,36,44,47
+VCCGT 7,40





H/W side output CAP list

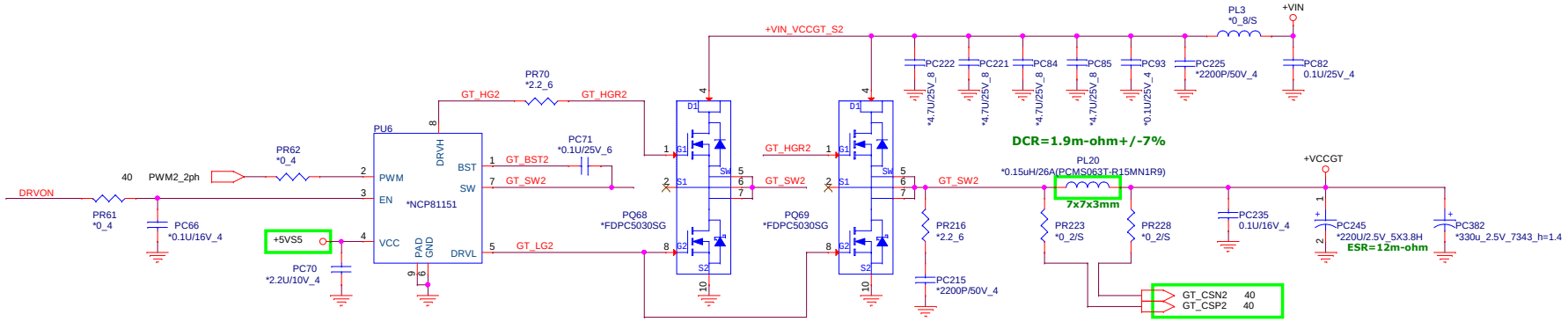
47U/6.3V_0805 X 6
22U/6.3V_0603 X 12 (GTX+5)
10U/6.3V_0402 X 10
1U/6.3V_0402 X 12

+VCC_GT

U-line 22 (15W)
TDC:18A(22)
Icc max:31A(22)
L/L=3.1mV/A

U-line 23e(28W)
TDC:35A(23e)
Icc max =64A(GT+GTx)
L/L=2mV/A

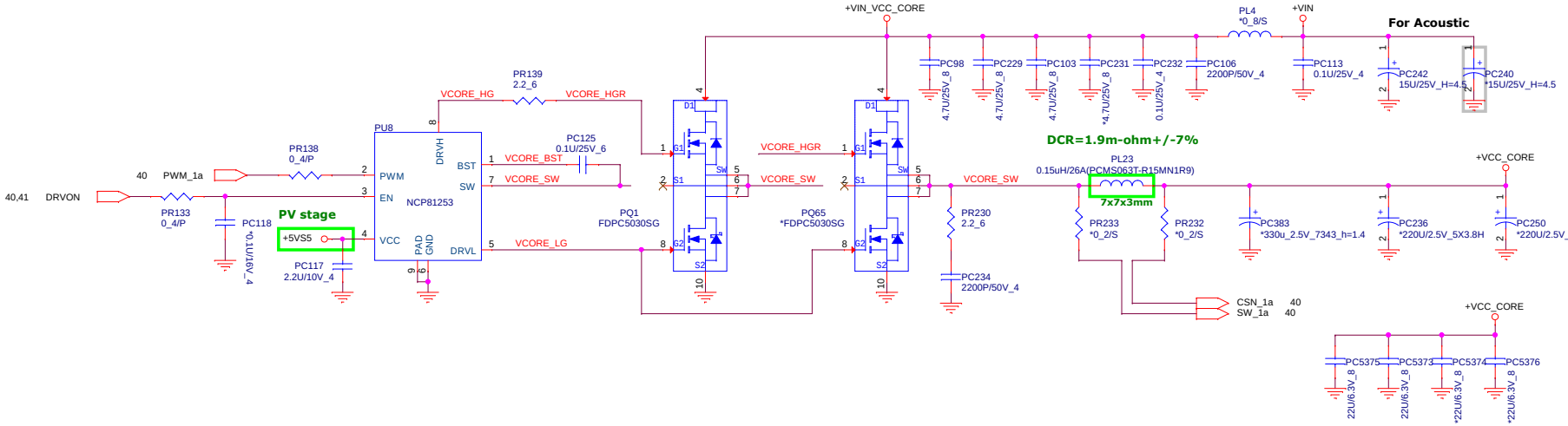
For U23e --> Add These Components



NB5	**PROJECT : X1Q** Quanta Computer Inc.	
Size Custom	Document Number +VCCSA (NCP81253)	Rev 2A
Date: Tuesday, December 01, 2015	Sheet 41 of 49	

CPU CORE

+VIN 25,29,35,36,37,38,40,41,43,45,46,47,49
+5VPCU 27,35,36,44,47
+VCCSA 6,40
+VCC_CORE 5



+VCC_CORE

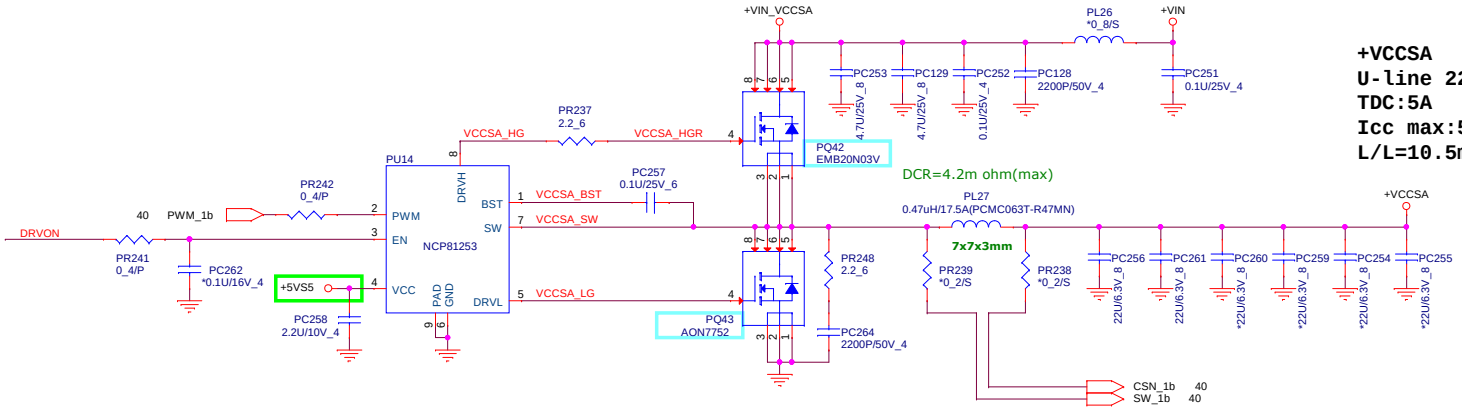
U-line 22(15W)
TDC:21A
Icc max:29A
L/L=2.4mV/A

U-line 23e(28W)
TDC:23A
Icc max:32A
L/L=2.4mV/A

H/W side output CAP list

47U/6.3V_0805 X 9
22U/6.3V_0805 X 1
22U/6.3V_0603 X 13
10U/6.3V_0603 X 1
10U/6.3V_0402 X 15
1U/6.3V_0402 X 15

VCCSA



+VCCSA
U-line 22&23e
TDC:5A
Icc max:5A
L/L=10.5mV/A

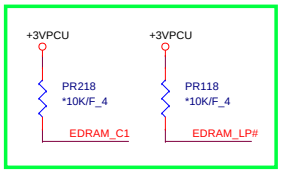
PROJECT : X1Q
Quanta Computer Inc.

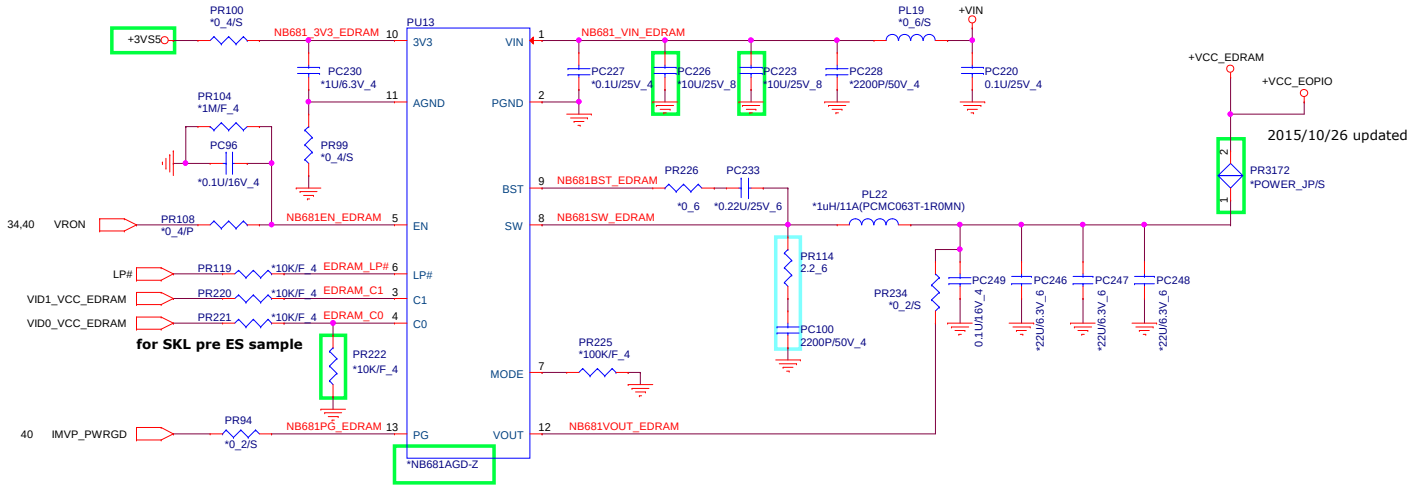
NB5

Size	Document Number	Rev
Custom	+VCORE/VCCSA (NCP81253)	
Date: Tuesday, December 01, 2015	Sheet 42 of 49	

+VIN 25,29,35,36,37,38,40,41,42,45,46,47,49
+3VPCU 6,13,29,31,34,35,36,48
+VCC_EOPIO 5
+VCC_EDRAM 5
+3VS5 4,10,15,16,25,31,34,36,37,38,39,44,47

+VCC_EDRAM +/- 5%
Countinue current:4.5A
Peak current:6A





2015/10/26 updated

VCC_EDRAM

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

MODE

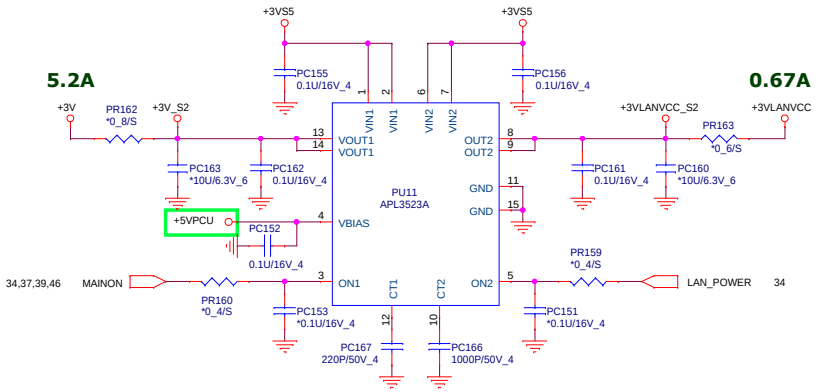
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

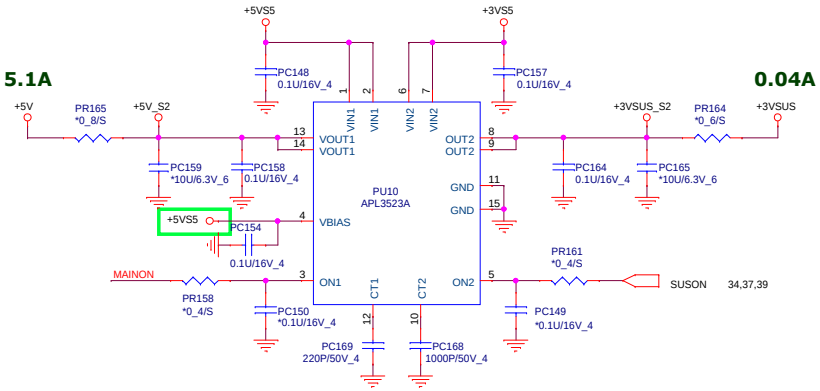
PROJECT : X1Q
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	+VCC_EDRAM (NB681)_23E	
Date: Tuesday, December 01, 2015	Sheet 43 of 49	

+3V 2,4,10,11,12,13,14,15,17,18,19,20,21,25,26,27,28,29,30,32,33,34,40,45
+5V 25,26,27,28,29
+VIN 25,29,35,36,37,38,40,41,42,43,45,46,47,49
+3VS5 4,10,15,16,25,31,34,36,37,38,39,43,47
+5VS5 4,25,26,27,36,37,38,39,40,41,42,45,46,47
+3VSUS 29
+5VPCU 27,35,36,47
+3VLANVCC 33



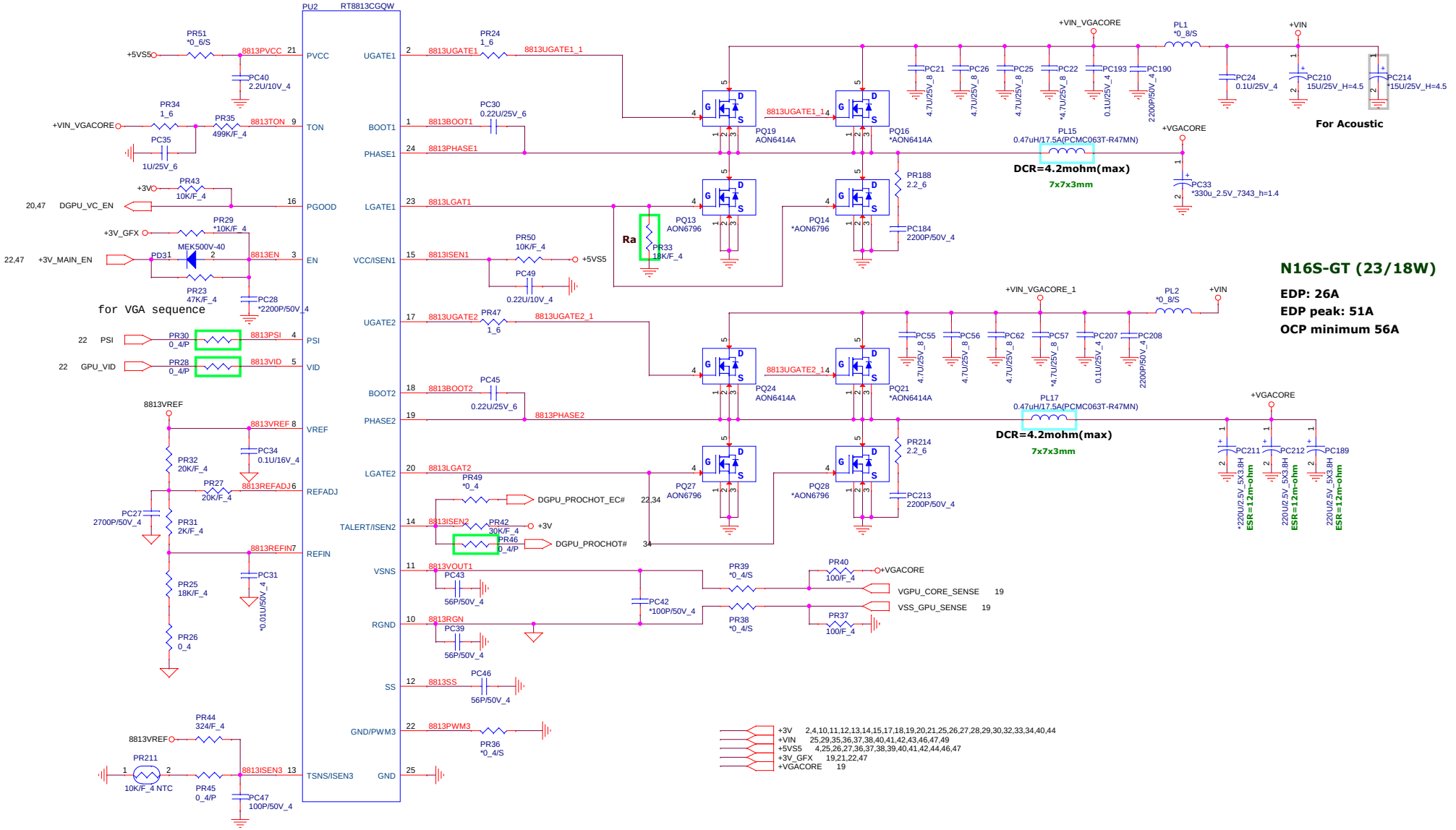


NB5

PROJECT : X1Q
Quanta Computer Inc.

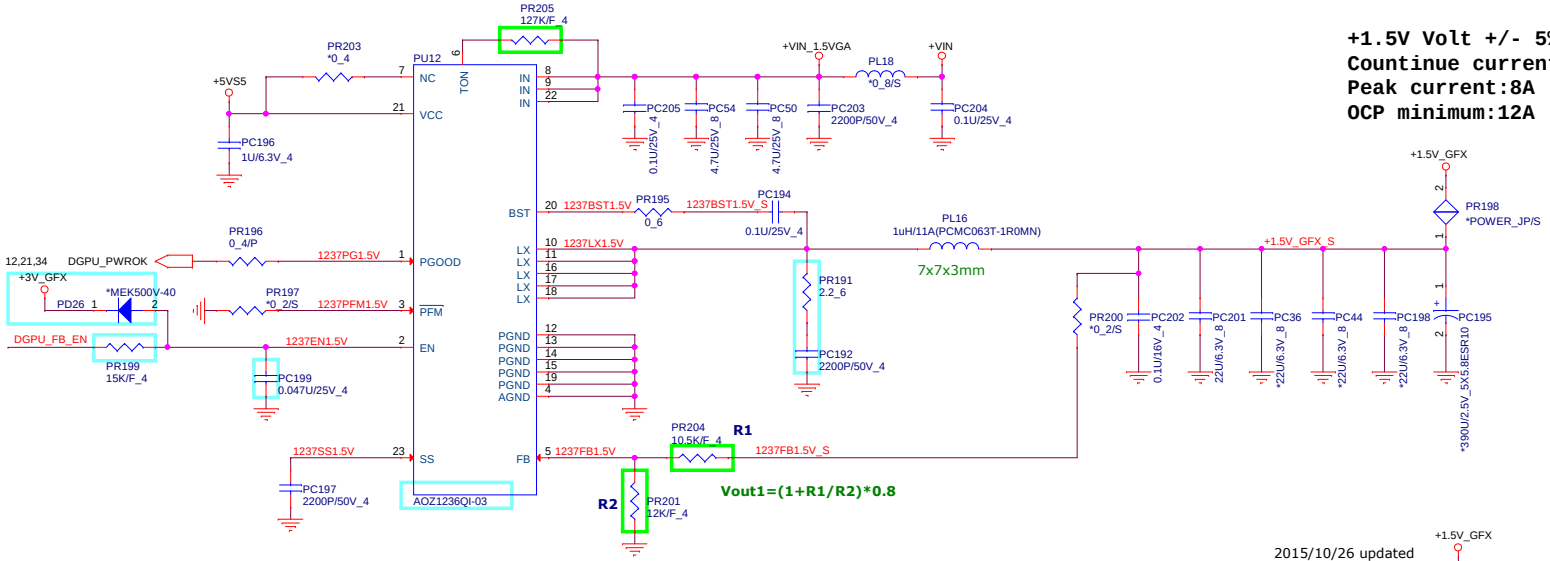
Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448)	1A
Date: Tuesday, December 01, 2015	Sheet 44 of 49	

VGA Core

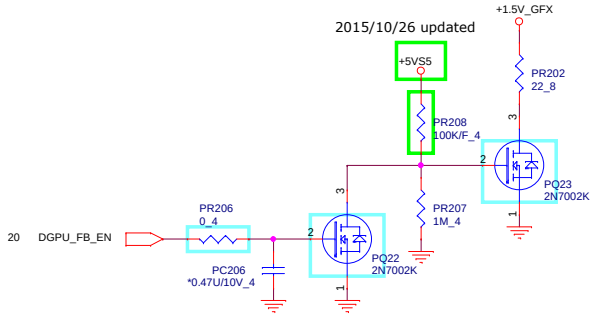


NB5	**PROJECT : X1Q** Quanta Computer Inc.		
	Size: Custom	Document Number: +VGACORE (RT8813A)	Rev: 2A
	Date: Tuesday, December 01, 2015	Sheet 45 of 49	

+VIN 25,29,35,36,37,38,40,41,42,43,45,47,49
+5VS5 4,25,26,27,36,37,38,39,40,41,42,44,45,47
+1.5V_GFX 20,21,23,24

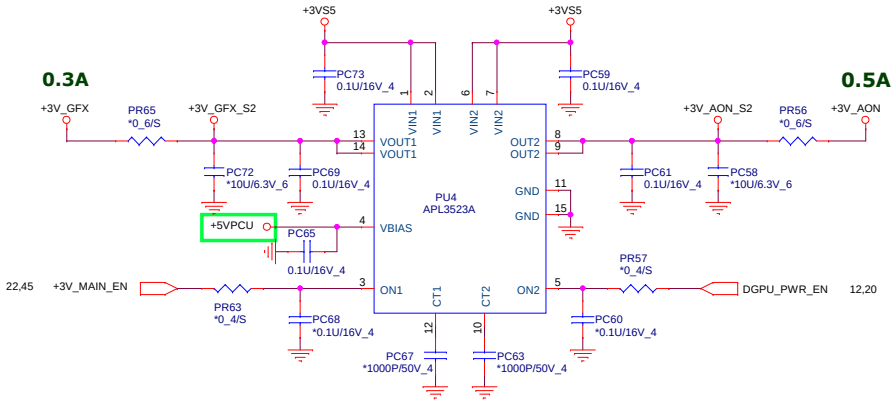


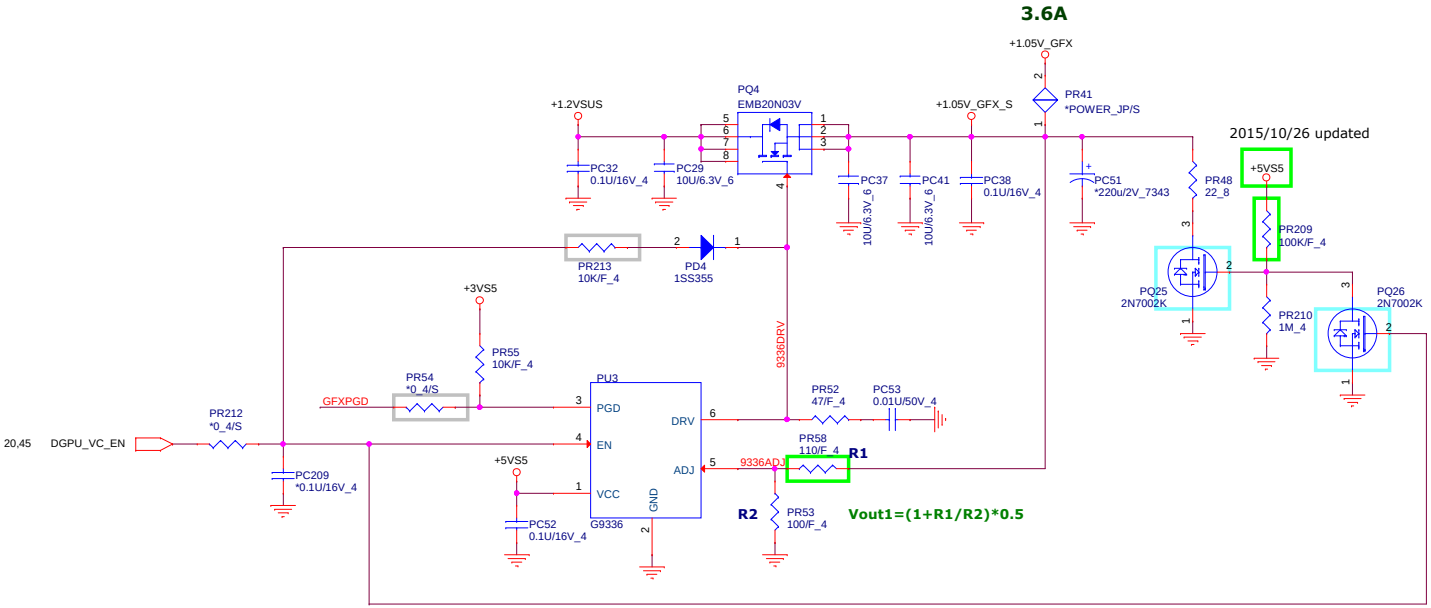
+1.5V Volt +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A



NB5	**PROJECT : X1Q** Quanta Computer Inc.	
Size: Custom	Document Number: +1.35V_VGA(AOZ1237)	Rev: 1A
Date: Tuesday, December 01, 2015	Sheet 46 of 49	

+VIN 25,29,35,36,37,38,40,41,42,43,45,46,49
+3VS5 4,10,15,16,25,31,34,36,37,38,39,43,44
+5VS5 4,25,26,27,36,37,38,39,40,41,42,44,45,46
+3V_GFX 19,21,22,45
+3V_AON 19,22
+1.2VSUS 3,6,17,18,37,39
+1.05V_GFX 19,20,21





NB5	**PROJECT : X1Q** Quanta Computer Inc.	
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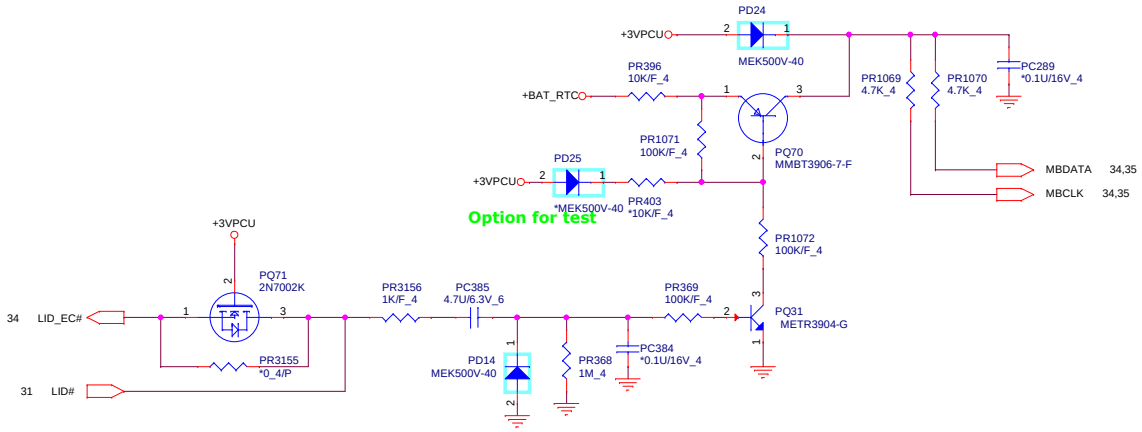
+3VPCU 6,13,29,31,34,35,36,43
+BAT_RTC 4,13,15,31,35



NB5	**PROJECT : X1Q** Quanta Computer Inc.	
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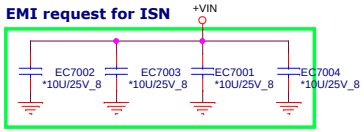
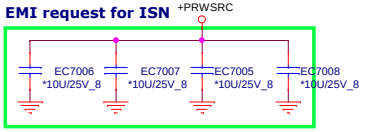
EMI request for ISN



EMI request for ISN



NB5

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Quanta Computer Inc.

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Custom	EMI solution	1A
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