MS-7673

ATX(Full Size)
Ver: 10

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH

OnBoard Chipset:

Clock Gen:IDT 4105
HD Audio Codec:RTL892
LAN:RTL 8111E 10/100/1000 NIC X 2
SIO:FIN71889ED(LAA)
ESATA Controller: JM363
USB3.0: UPD720200F1
Flash ROM: 64 Mb SPI (PCH)
1394 Controller: VT6308P

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 2

PCI Express (X1) Slot * 4

PCI Slot * 1(From IDT TSI383)

PWM:

CPU:UPI6234(5PHASE)
CPU_VTT:UP6103A(1PHASE)
CPU_SA:UP6103A (1PHASE)
DDR/PCH PWR:UP6103A

Other:

SATA3.0 x2+SATA2.0 x4 (PCH)

ESATA2.0 x2 (JMB363)
USB2.0 *4 (Rear*8 Front*4)
COM Header *1

ACPI:

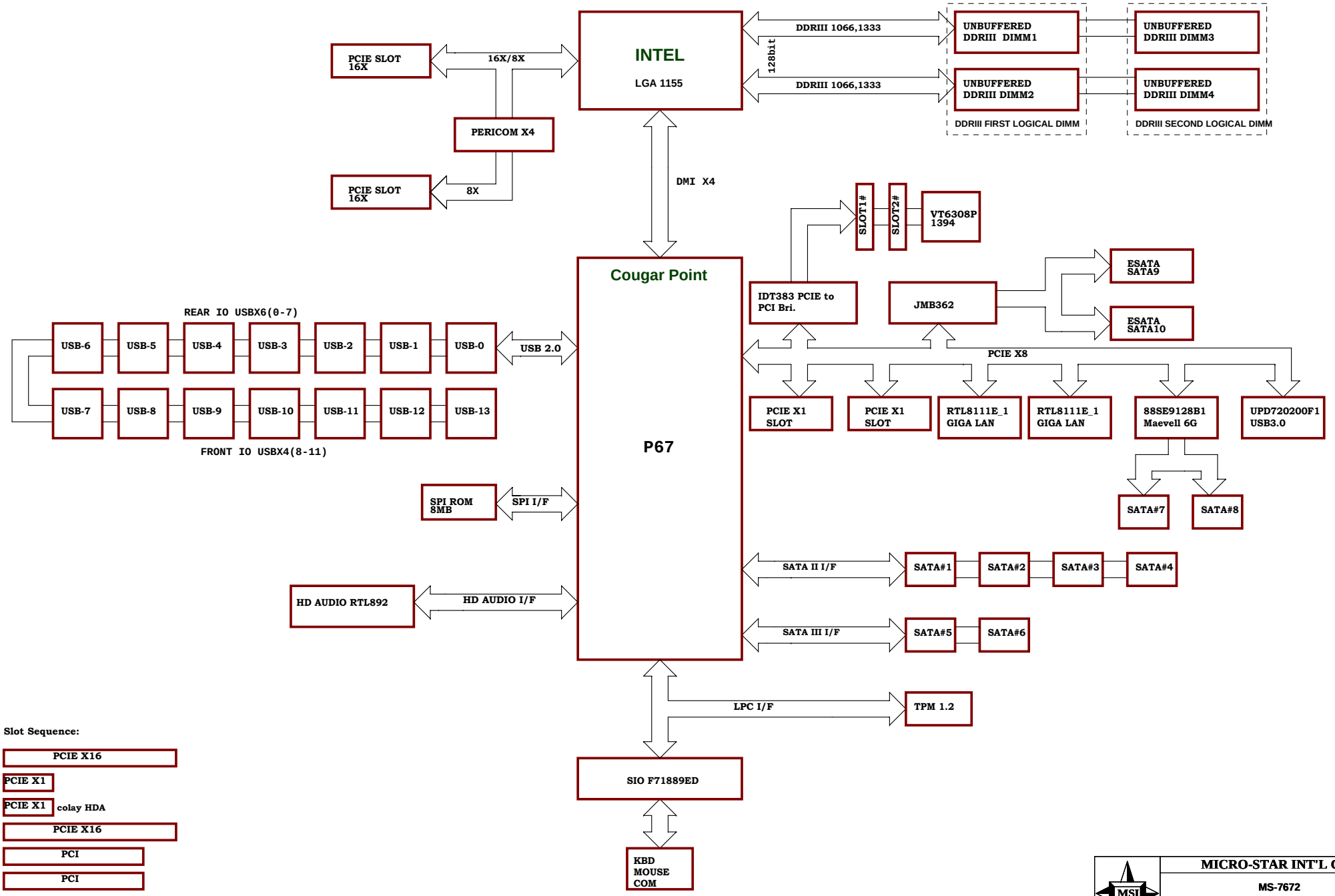
UPI

MICRO-STAR INT'L CO.,LTD

MS-7673

Size	Document Description	Rev
Custom	Cover Sheet	10

Date: Wednesday, October 13, 2010 Sheet 1 of 45



Slot Sequence:

- PCIE X16
- PCIE X1
- PCIE X1 colay HDA
- PCIE X16
- PCI
- PCI

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Size: Custom	Document Description: Block Diagram	Rev: 0A
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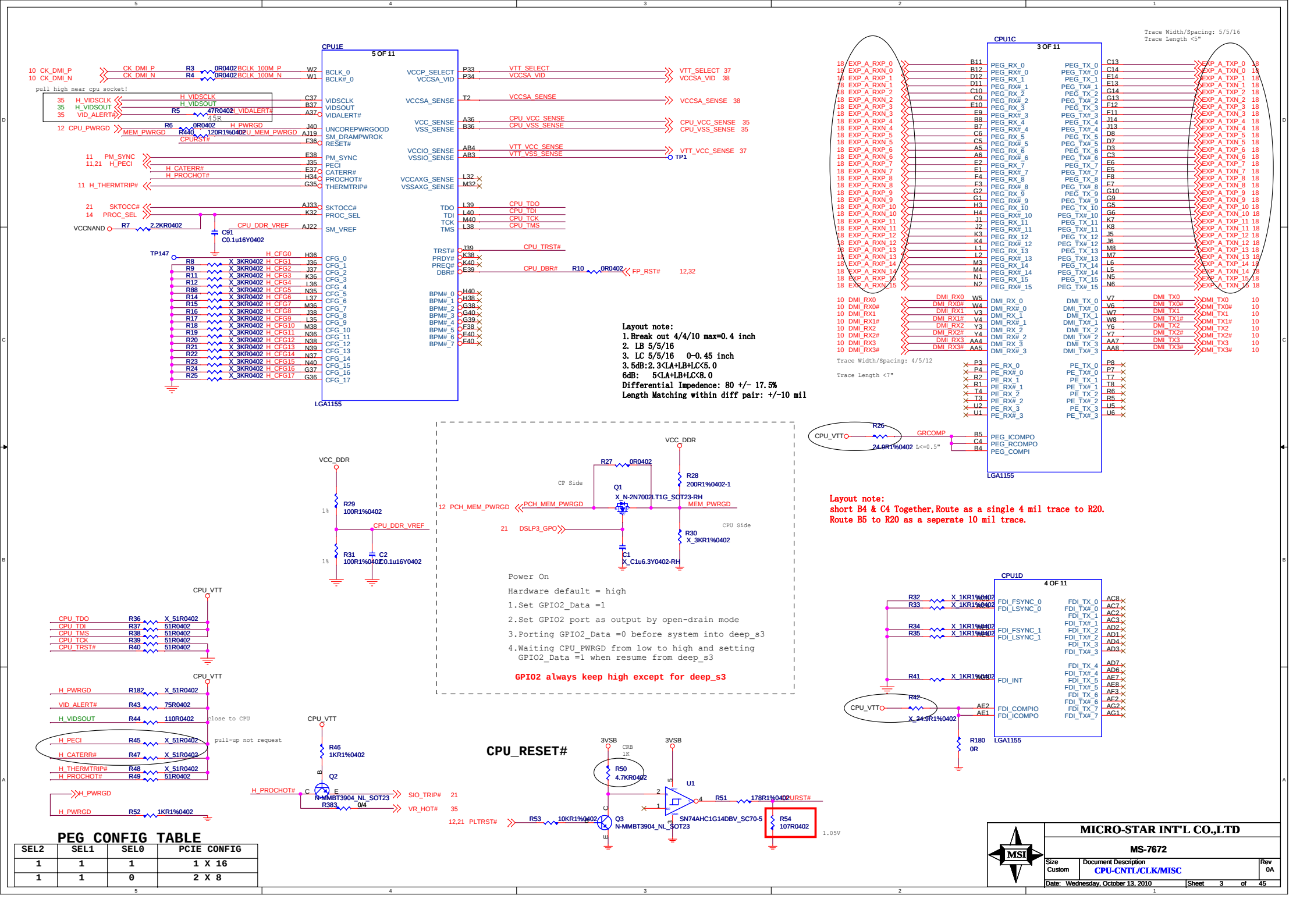
CPU1E
5 OF 11
LGA1155
CPU1C
3 OF 11
LGA1155
CPU1D
4 OF 11
LGA1155
Trace Width/Spacing: 5/5/16
Trace Length <5"
Trace Width/Spacing: 4/5/12
Trace Length <7"
pull high near cpu socket!
close to CPU
pull-up not request
Layout note:
1.Break out 4/4/10 max=0.4 inch
2. LB 5/5/16
3. LC 5/5/16 0~0.45 inch
3.5dB:2.3<LA+LB+LC<5.0
6dB: 5<LA+LB+LC<8.0
Differential Impedence: 80 +/- 17.5%
Length Matching within diff pair: +/-10 mil
Layout note:
short B4 & C4 Together,Route as a single 4 mil trace to R20.
Route B5 to R20 as a seperate 10 mil trace.
CP Side
CPU Side
Power On
Hardware default = high
1.Set GPIO2_Data =1
2.Set GPIO2 port as output by open-drain mode
3.Porting GPIO2_Data =0 before system into deep_s3
4.Waiting CPU_PWRGD from low to high and setting GPIO2_Data =1 when resume from deep_s3
GPIO2 always keep high except for deep_s3
CPU_RESET#
PEG CONFIG TABLE
SEL2 SEL1 SEL0 PCIE CONFIG
1 1 1 1 X 16
1 1 0 2 X 8
MICRO-STAR INT'L CO.,LTD
MS-7672
Size Custom
Document Description CPU-CNTL/CLK/MISC
Rev 0A
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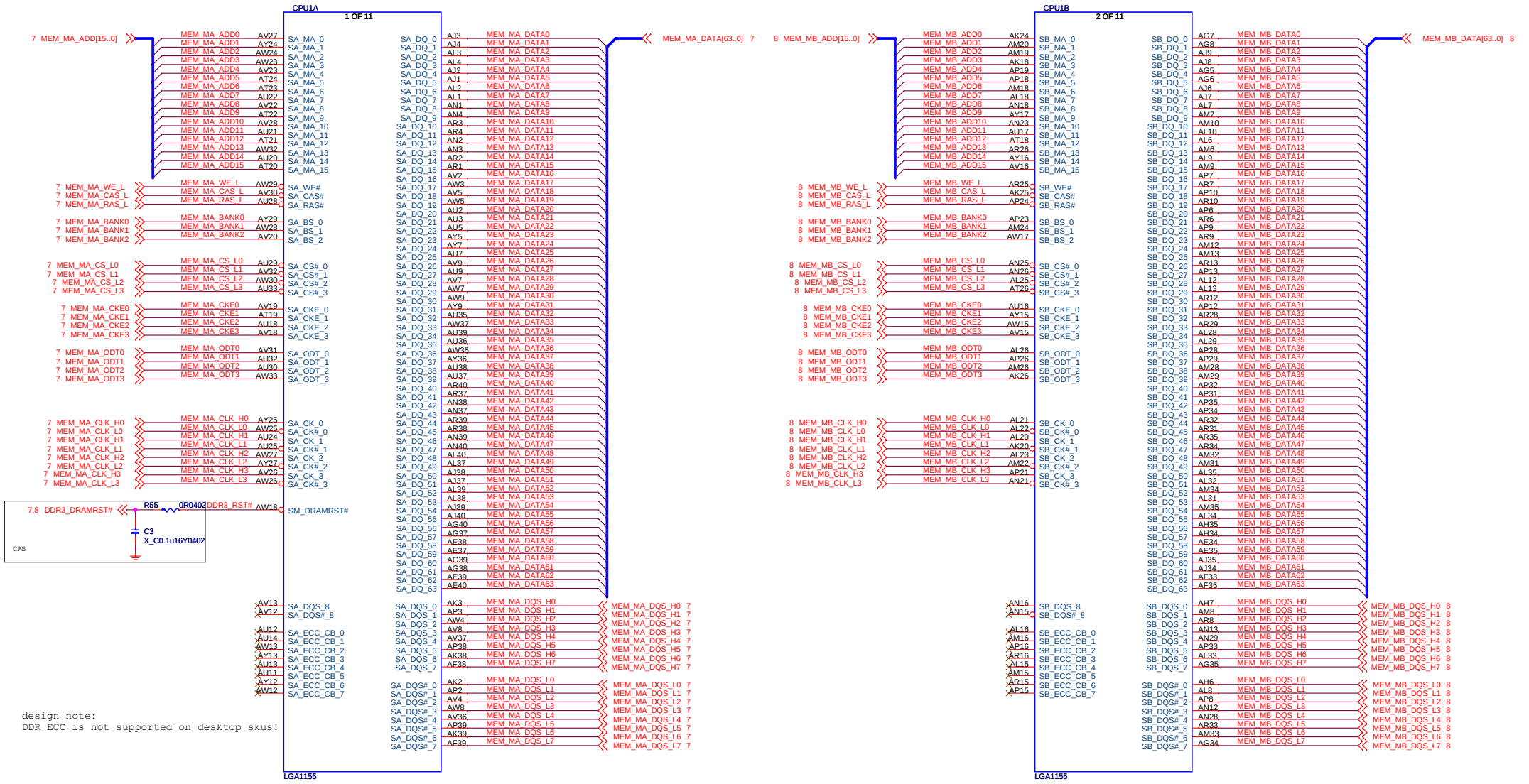

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(1.05V / 1.00V)

VCCP

CPU1F
6 OF 11
LGA1155

CPU_VTT

CPU1H
8 OF 11
LGA1155

VCC_DDR

CPU_SA

VCC1_8

CPU1G
7 OF 11
LGA1155

VCCP: 112A
CPU_VTT: 8.2A
CPU_SA: 8.8A
VCC_DDR: 25A
VCC1_8: 1.6A

+1.5V_DDR3-Decoupling

VCC_DDR

C4 C5 C6 — C22u6.3X50805-RH

CPU SOCKET CAVITY CAPS

+CPU_VTT Decoupling

CPU_VTT

C7 C8 C9 C10 C11 C12 C13 C14 C15 — X_C22u6.3X50805-RH / C22u6.3X50805-RH

CPU SOCKET CAVITY CAPS

CPU_VTT

C16 C17 C18 C19 — C22u6.3X50805-RH / X_C22u6.3X50805-RH

Backside

CPU_SA

C20 C21 — C22u6.3X50805-RH

CPU SOCKET

+CPU_VCCP-Decoupling

VCCP

PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY

C23 C24 C25 C26 C27 — C22u6.3X50805-RH

C28 C29 C30 C31 C32 — C22u6.3X50805-RH

C33 C34 C35 C36 C37 C38 C39 C40 — C22u6.3X50805-RH / X_C22u6.3X50805-RH

C41 C42 C43 C44 — C22u6.3X50805-RH

Backside

VCC1_8

C22 C22u6.3X50805-RH

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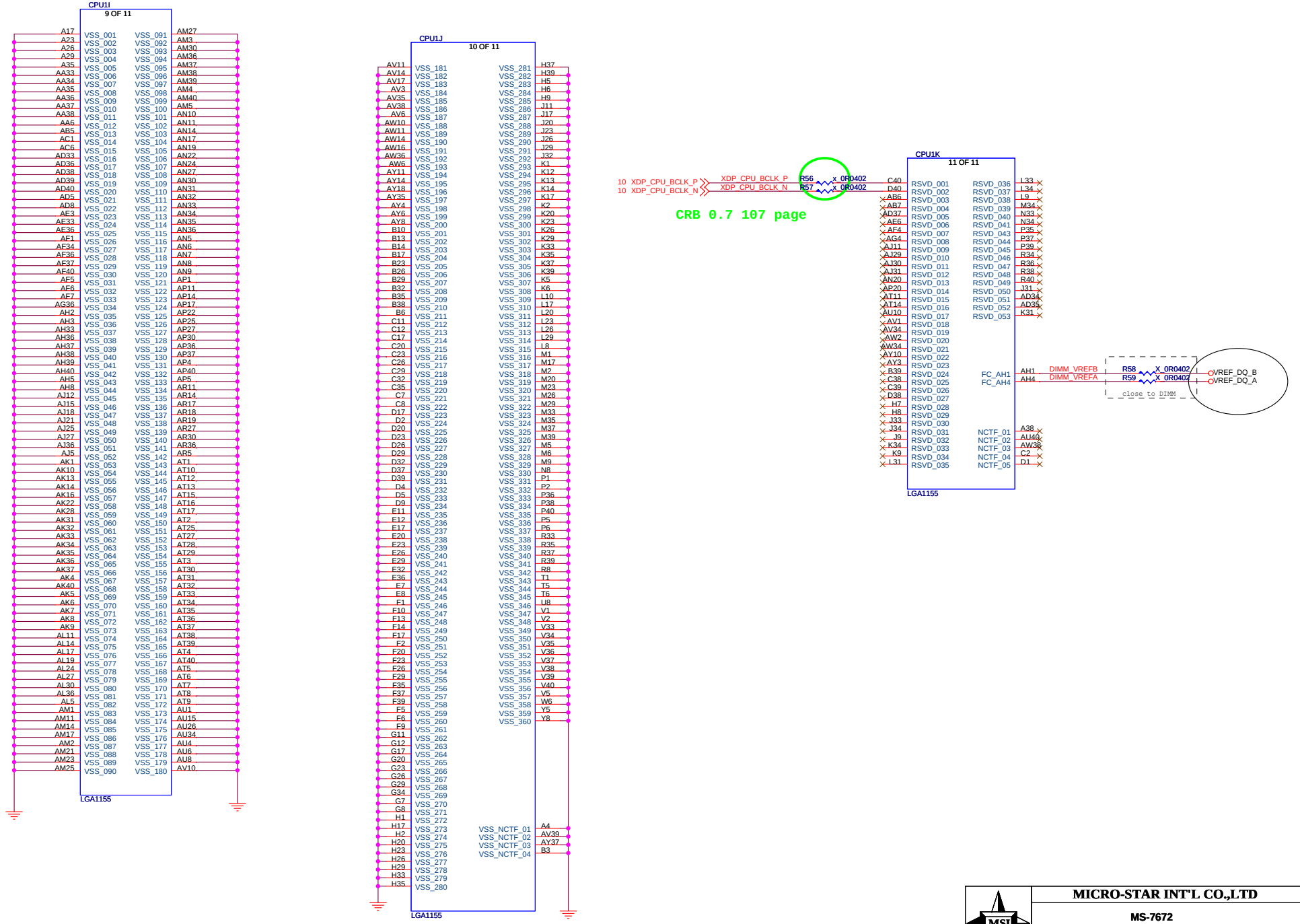

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Size	Document Description	Rev
Custom	CPU-GND	0A

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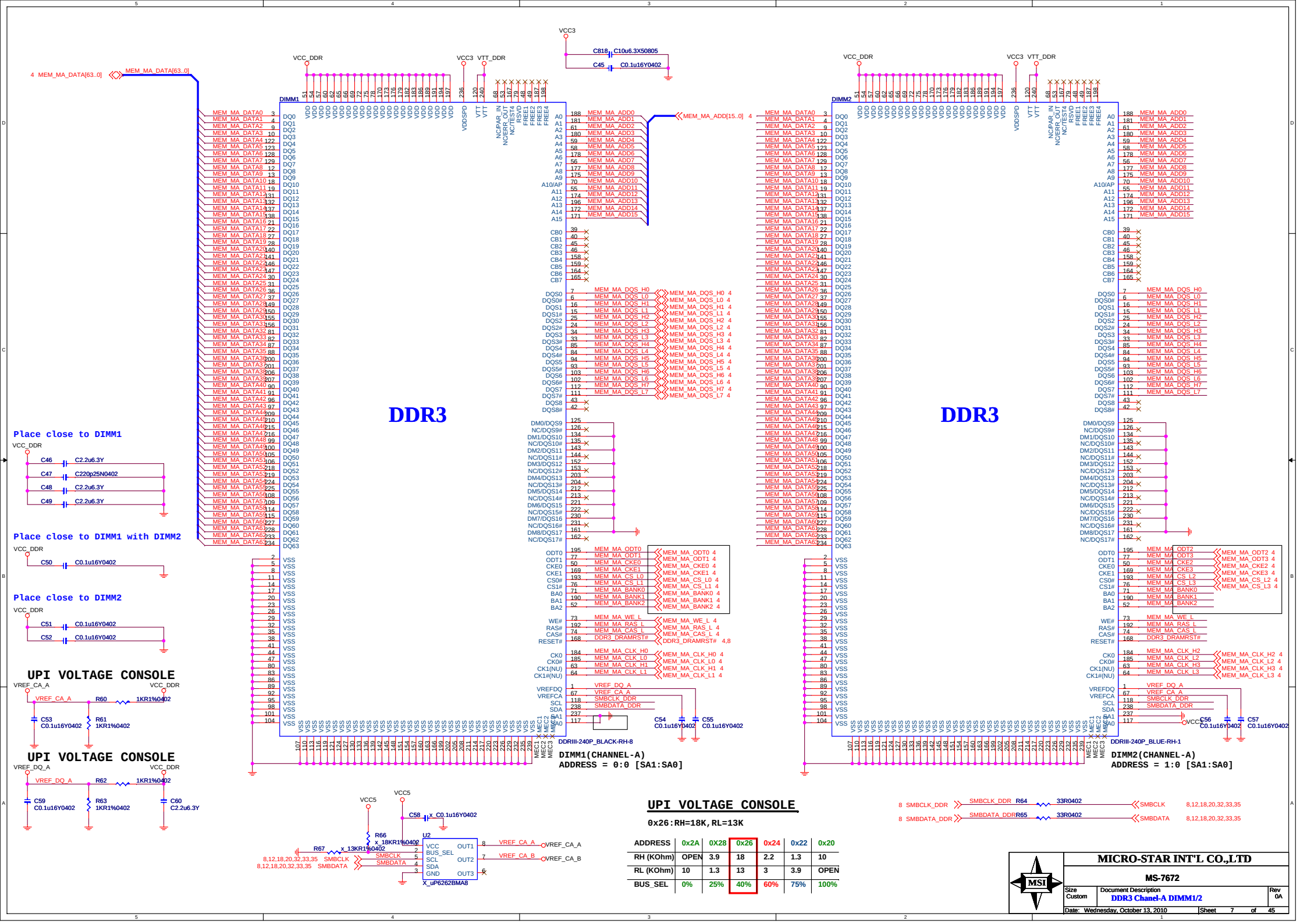

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	18	2.2	1.3	10
RL (KOhm)	10	1.3	13	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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Size: Custom	Document Description: DDR3 Chanel-A DIMM1/2
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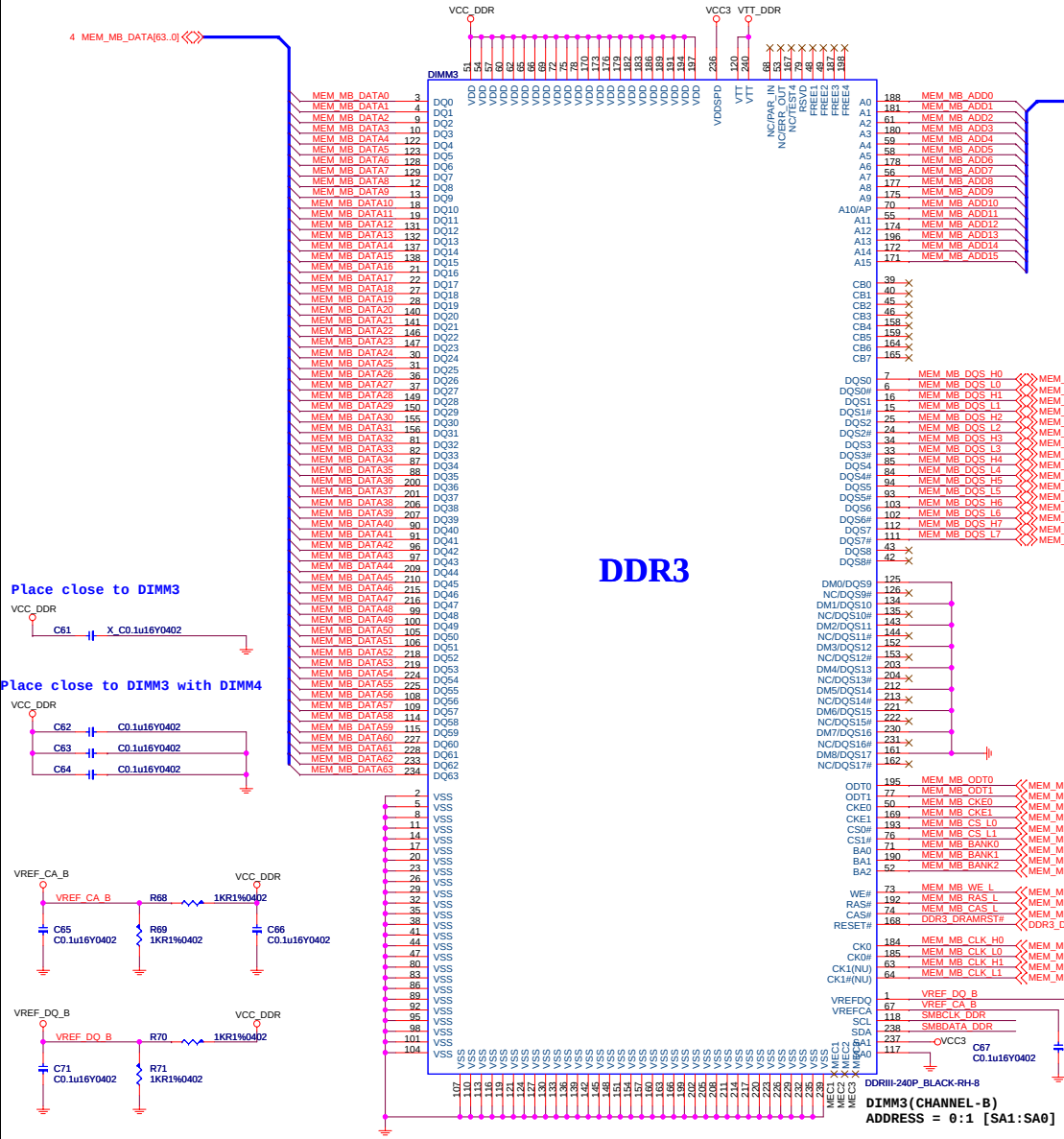
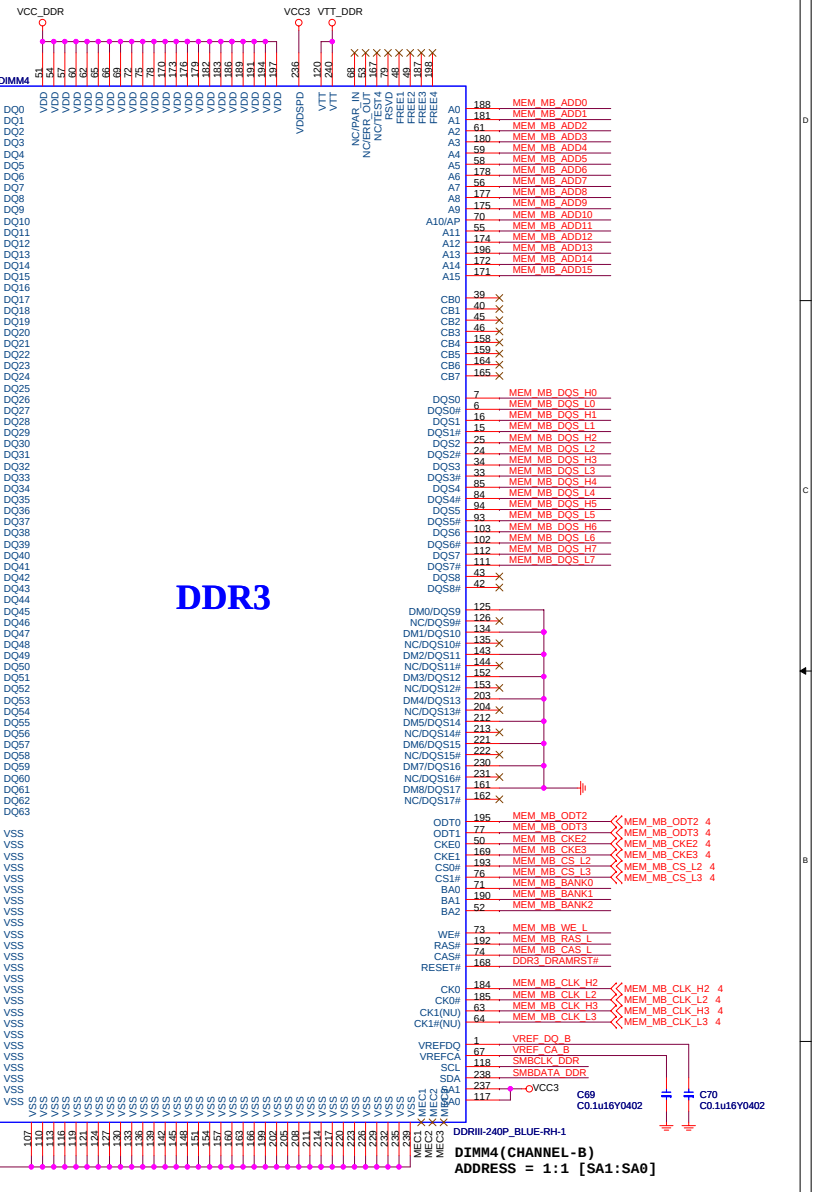
DDRIII DIMM_B0

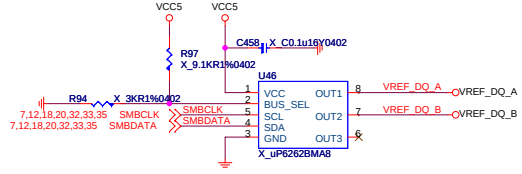


DDRIII DIMM_B1



UPI VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K



ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	9.1	3	2.2	1.3	10
RL (KOhm)	10	3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

SMBCLK_DDR 7
SMBDATA_DDR 7

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MS-7672	
Size: Custom	Document Description: DDR3 Chanel-B DIMM3/4
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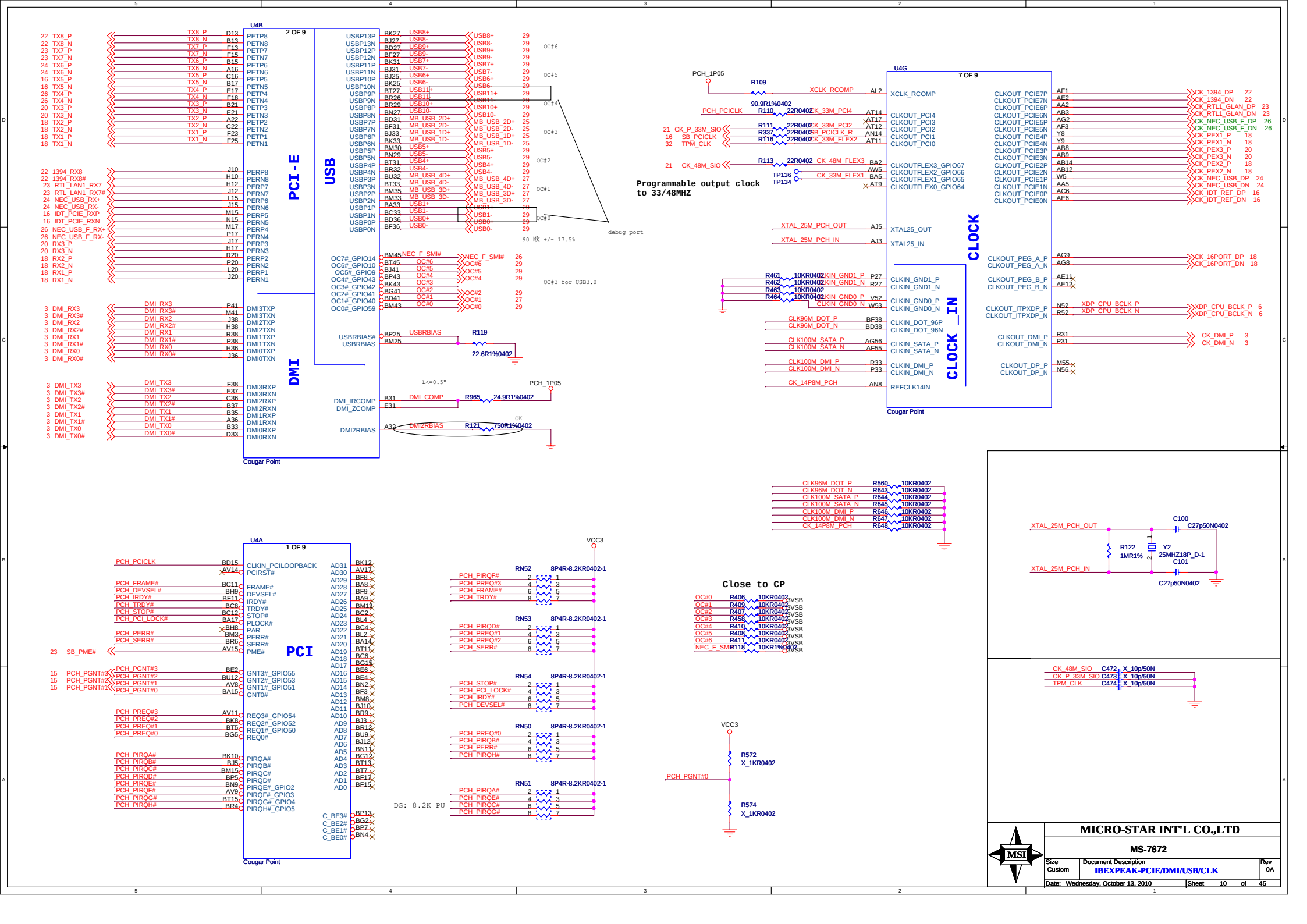
U4B
2 OF 9
PCI-E
USB
DMI
Cougar Point
U4G
7 OF 9
CLOCK
CLOCK_IN
Cougar Point
Programmable output clock to 33/48MHZ
debug port
U4A
1 OF 9
PCI
Cougar Point
Close to CP
DG: 8.2K PU
MICRO-STAR INT'L CO.,LTD
MS-7672
IBEXPEAK-PCIE/DMI/USB/CLK
Date: Wednesday, October 13, 2010
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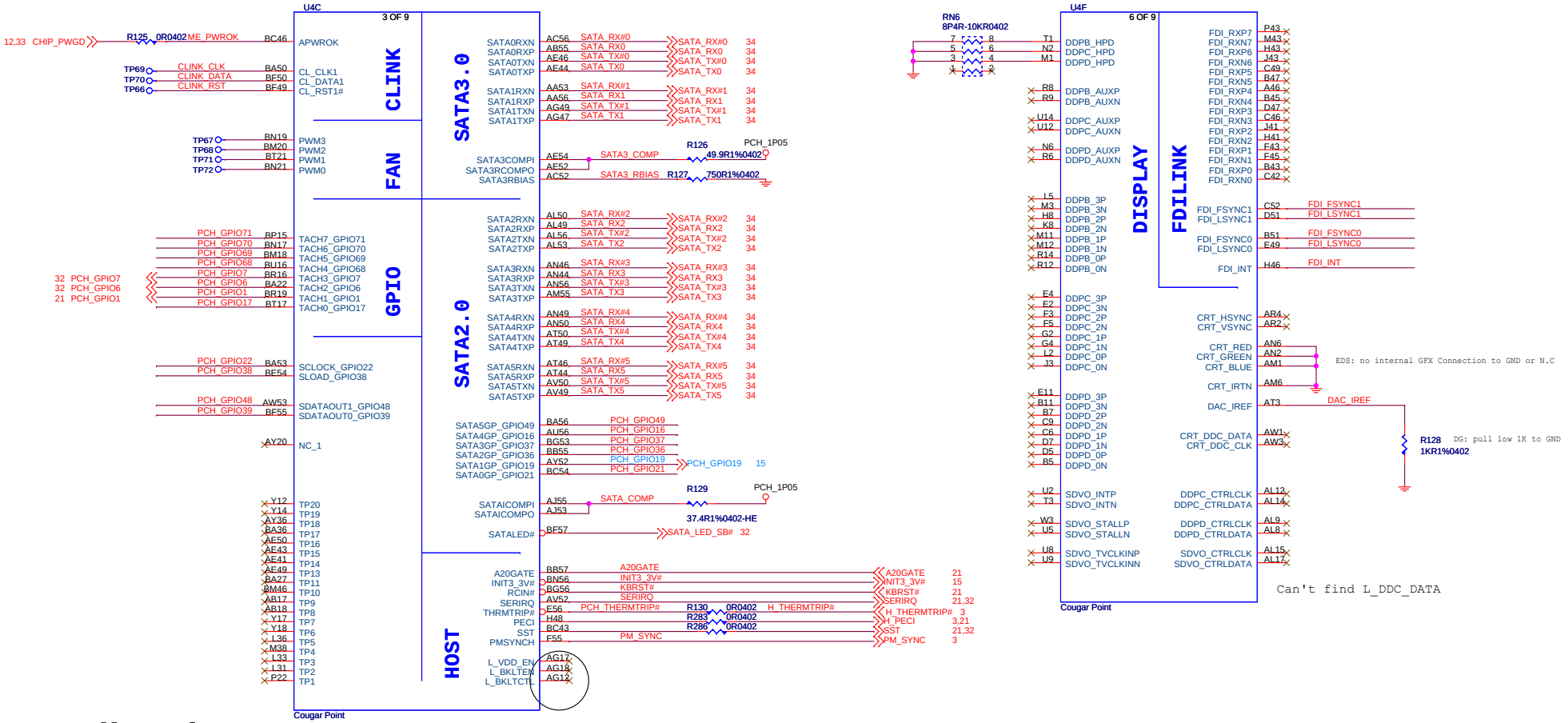
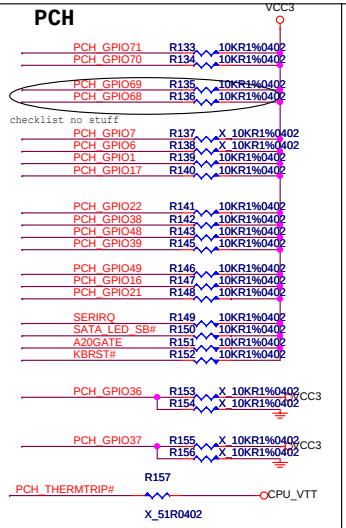
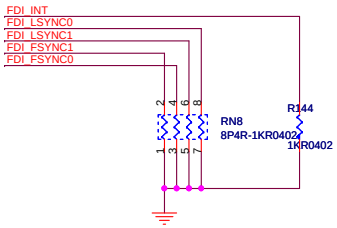


Pull HIGH for PCH



No VGA(FDI 1Kohm pull down)



DG: no VGA these signal Connect to Vcc_fdi or GND via a 1 K resistor

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Size: Custom	Document Description: Cougar Point-SATA/HOST/FAN/GPIO
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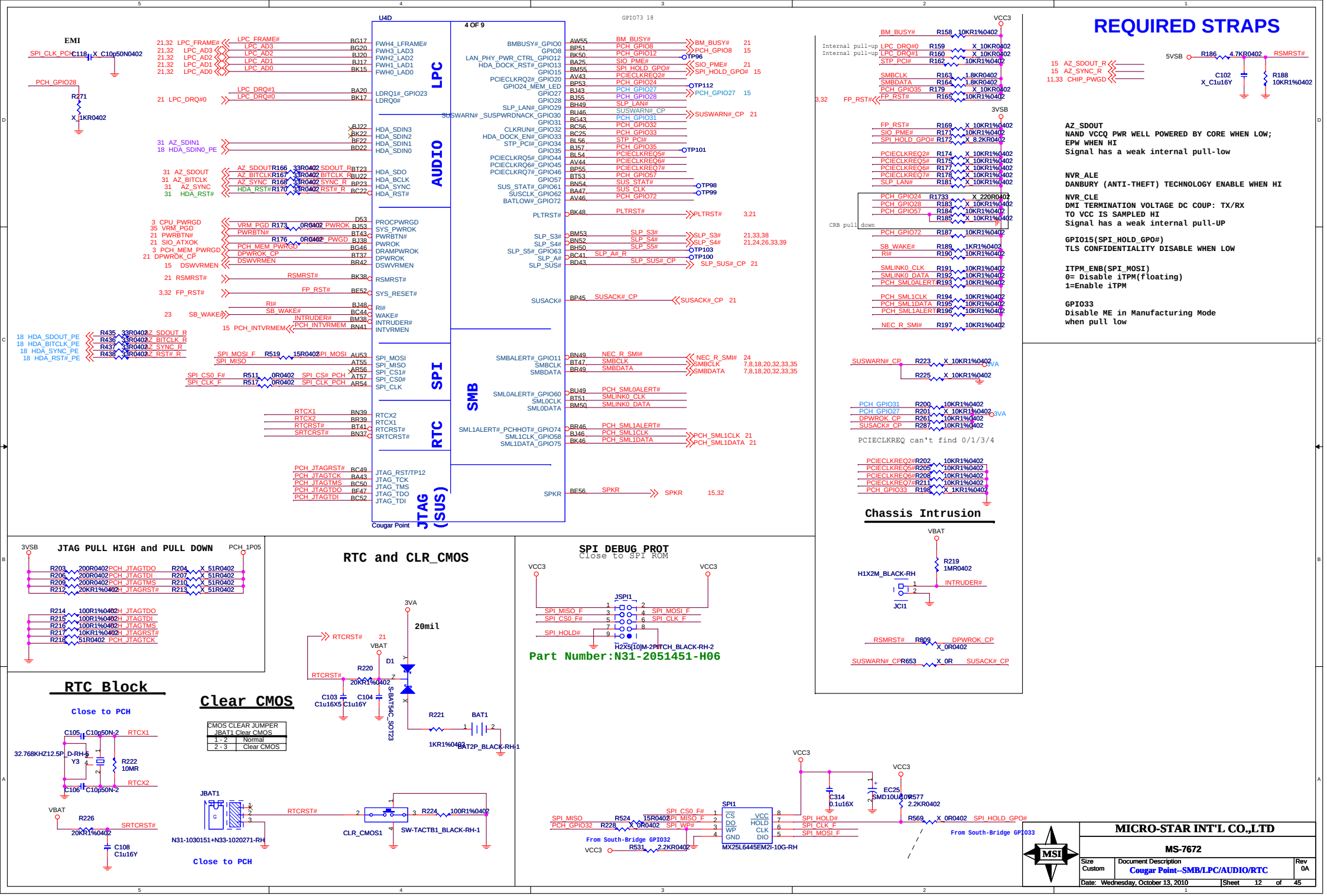
U4D
4 OF 9
Cougar Point
LPC
AUDIO
SPI
SMB
RTC
JTAG (SUS)
EMI
REQUIRED STRAPS
AZ_SDOUT
NAND VCCQ PWR WELL POWERED BY CORE WHEN LOW;
EPW WHEN HI
Signal has a weak internal pull-low
NVR_ALE
DANBURY (ANTI-THEFT) TECHNOLOGY ENABLE WHEN HI
NVR_CLE
DMI TERMINATION VOLTAGE DC COUP: TX/RX
TO VCC IS SAMPLED HI
Signal has a weak internal pull-UP
GPIO15(SPI_HOLD_GPO#)
TLS CONFIDENTIALITY DISABLE WHEN LOW
ITPM_ENB(SPI_MOSI)
0= Disable iTPM(floating)
1=Enable iTPM
GPIO33
Disable ME in Manufacturing Mode
when pull low
JTAG PULL HIGH and PULL DOWN
RTC and CLR_CMOS
SPI DEBUG PROT
Close to SPI ROM
Part Number:N31-2051451-H06
Chassis Intrusion
RTC Block
Close to PCH
Clear CMOS
CMOS CLEAR JUMPER
JBAT1 Clear CMOS
1 - 2 Normal
2 - 3 Clear CMOS
Close to PCH
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Cougar Point--SMB/LPC/AUDIO/RTC
Size Custom
Rev 0A
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Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.

PCH_1P05

L1 X_1u50mA_0805-RH VCCAFDIPLL

R232 X_0R0402 VCCACLK NO THIS PIN

R233 X_0R0805 VCCAPLLDMI2
C110 X_C10u6.3X50805
C111 C1u6.3X50402-HF

R234 0R0805 VCCCLKDMI
C113 C10u6.3X50805
C114 C1u6.3X50402-HF

R236 0R0805 VCCA_DPLLA

R237 0R0805 VCCA_DPLLB

PCH_1P05

DMI PLL FILTER

L2 X_1u500mA_0805-RH-1 VCCAPLLEXP
C121 X_C10u6.3X50805
C122 C1u6.3X50402-HF

SATA PLL FILTER

L3 X_10u100mA_0805-RH VCCAPLLSATA
C123 X_C10u6.3X50805
C124 C1u6.3X50402-HF

PCH_1P05: 7.66A
CPU_VTT: 0.058A
VCC1_8: 0.159A
VCC3: 0.697A
3VSB: 0.11A
5VREF: 0.001A
5VREF_SUS: 0.001A

POWER

U4H 8 OF 9 — Cougar Point

4.07A

PCH_1P05

CPU_VTT 0.001A → V_PROC_IO, V_PROC_IO_NCTF

CPU_VTT 0.057A → VCCDMI_02, VCCDMI_01

C112 C1u6.3X50402-HF 0.02A → VCCAPLLDMI2, VCCCLKDMI

0.001A 5VREF → V5REF
0.001A 5VREF_SUS → V5REF_SUS

+3.3V_DAC 0.068A → VCCADAC
VCCACLK → VCCACLK

0.1A VCCA_DPLLA → VCCADPLLA
0.1A VCCA_DPLLB → VCCADPLLB

VCCAPLLSATA → VCCAPLLSATA

VCCAPLLEXP → VCCAPLLEXP

VCCAFDIPLL → VCCAFDIPLL

PCH_1P05 R262 X_0R0805 → 3VSB 0.01A → VCCSUSHDA

VCC3 0.02A → VCCSPI

VCC1_8 R235 0R0805 → 0.159A → VCCVRM_04, VCCVRM_03, VCCVRM_02, VCCVRM_01

C116 C1u6.3X50402-HF DCPSUS → TP102 → DCPSUS_03, DCPSUS_02, DCPSUS_01

C117 C0.1u10X0402 DCPRTC → DCPRTC, DCPRTC_NCTF

TP104 → DCPSUSBYP

C119 C0.1u10X0402 DCPSST → DCPSST

VBAT → VCCRTC, VCCDSW3_3

3VA 0.003A → C120 x_C0.1u10X0402, C266 C0.1u10X0402

PCH_1P05 0.055A → VCCDIFFCLKN_03, VCCDIFFCLKN_02, VCCDIFFCLKN_01

PCH_1P05 CP1 X_COPPER → VCCSSC 0.105A

VCCDFTERM → 0.2A

VCC3_3_10 … VCC3_3_01 → 0.409A → VCC3

VCCSUS3_3_011 … VCCSUS3_3_001 → 0.097A → 3VSB

VCCNAND

VCC1_8 R238 0R X_0R → VCCNAND
VCC3 R239 X_0R → C125 X_C0.1u16Y0402

PCH_1P05

VCCCORE_022 … VCCCORE_001 → 1.6A

VCCASW_023 … VCCASW_001 → 1.61A

5VREF & 5VREF_SUS Sequencing Circuit

VCC3 → Q9 N-MMBT3904_NL_SOT23 (B) → C139 C1u6.3X50402-HF → 5VREF
VCC5 R240 10R0402 → 5VREF

3VSB → Q10 N-MMBT3904_NL_SOT23 (B) → C154 C0.1u16X0402-2 → 5VREF_SUS
5VSB R241 100R1%0402 → 5VREF_SUS

VCC3 → CP2 X_COPPER → +3.3V_DAC

Near ball AF1

C138 C0.1u10X0402

PCH decoupling cap

VBAT → C126 C0.1u16Y0402, C127 C1u10Y

VCC3 → C128 C0.1u16Y0402, C129 X_C0.1u16Y0402, C130 X_C0.1u16Y0402, C131 C0.1u16Y0402, C132 X_C0.1u16Y0402, C133 C4.7u10X50805-HF, C134 C1u10Y

CPU_VTT → C135 C4.7u10X50805-HF, C136 C0.1u16Y0402, C137 C0.1u16Y0402

3VSB → C140 C0.1u16Y0402, C141 C0.1u16Y0402

PCH_1P05 → C142 C1u10Y, C143 C10u6.3X50805, C144 C1u10Y, C145 C10u6.3X50805, C146 C4.7u10X50805-HF, C147 C10u6.3X50805, C148 C1u10Y, C149 C10u6.3X50805, C150 X_C0.1u16Y0402, C151 X_C0.1u16Y0402, C152 X_C0.1u16Y0402, C153 C0.1u16Y0402

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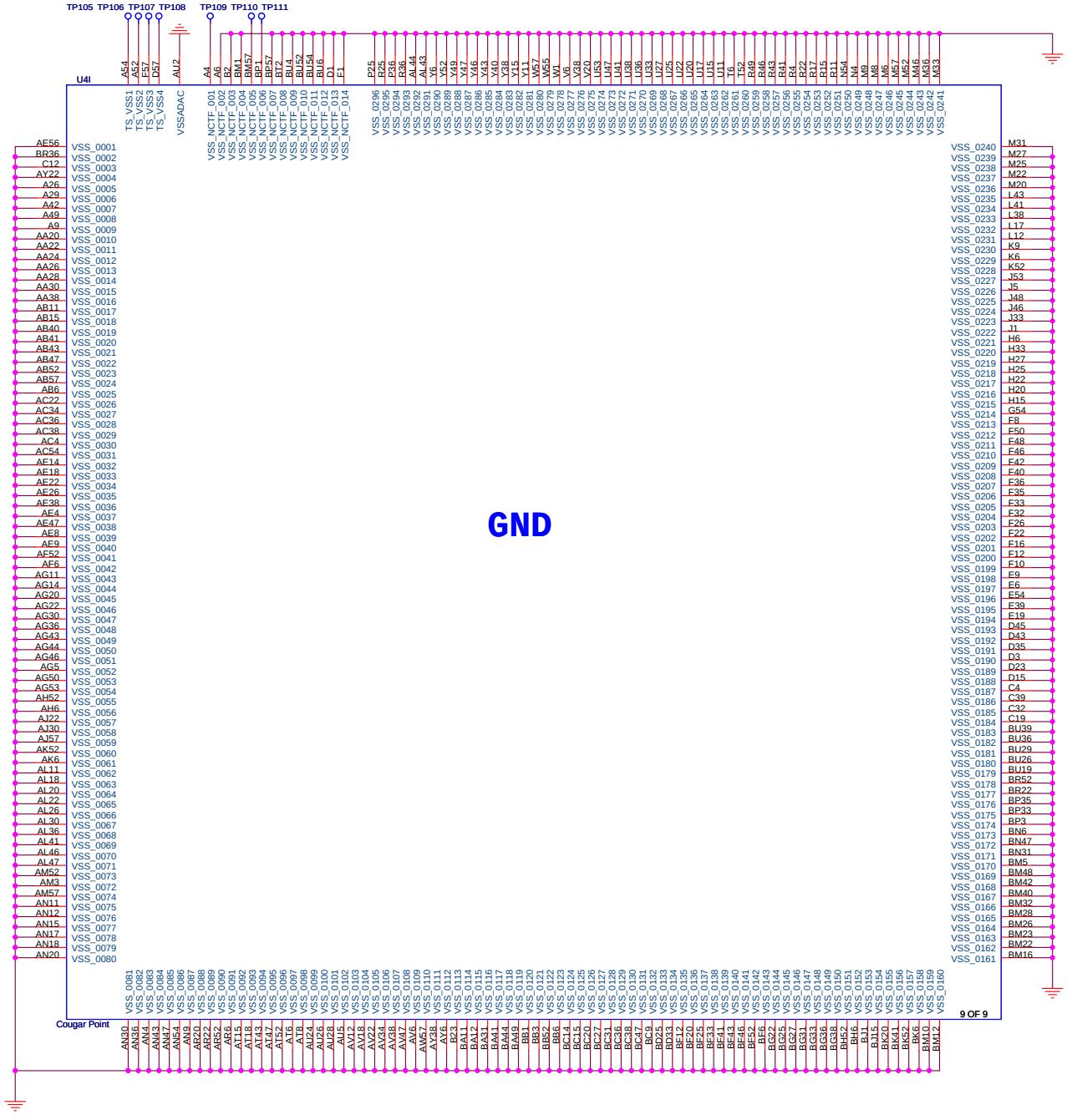

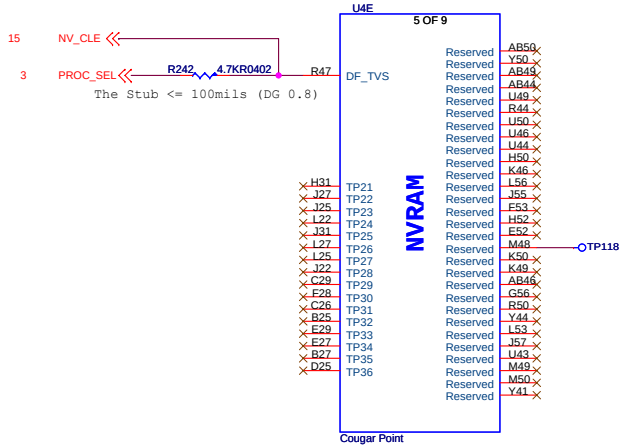

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MS-7672		
Size: Custom	Document Description: Cougar Point--GND/NVRAM	Rev: 0A
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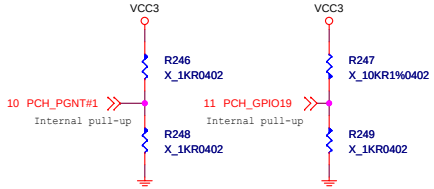
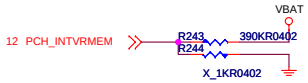
PCH Straps

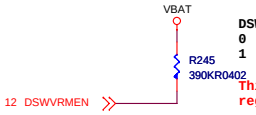
BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1





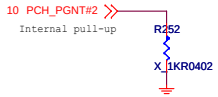
INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltageregulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

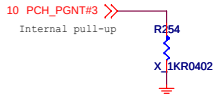


DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

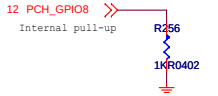
This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.



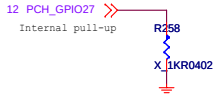
DMI AC/DC MODE
0 : AC
1 : DC *



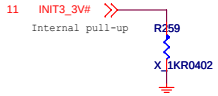
Topblock swap override when pull-low
Signal has a weak internal pull-up



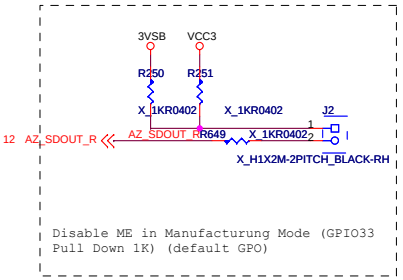
GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)



GPIO27
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up

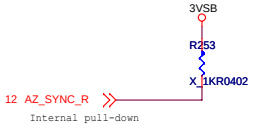


INT3_3V#
0 : INIT3_3V to asserted for 16 PCI clock to reset theprocessor by some evens occur
1 : Can not to reset the processor



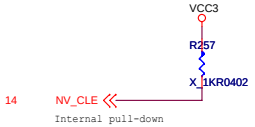
HDA_SDO
Disable ME in Manufacturing Mode when pull LOW ????

Internal pull-down

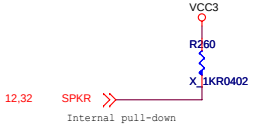


HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7672	
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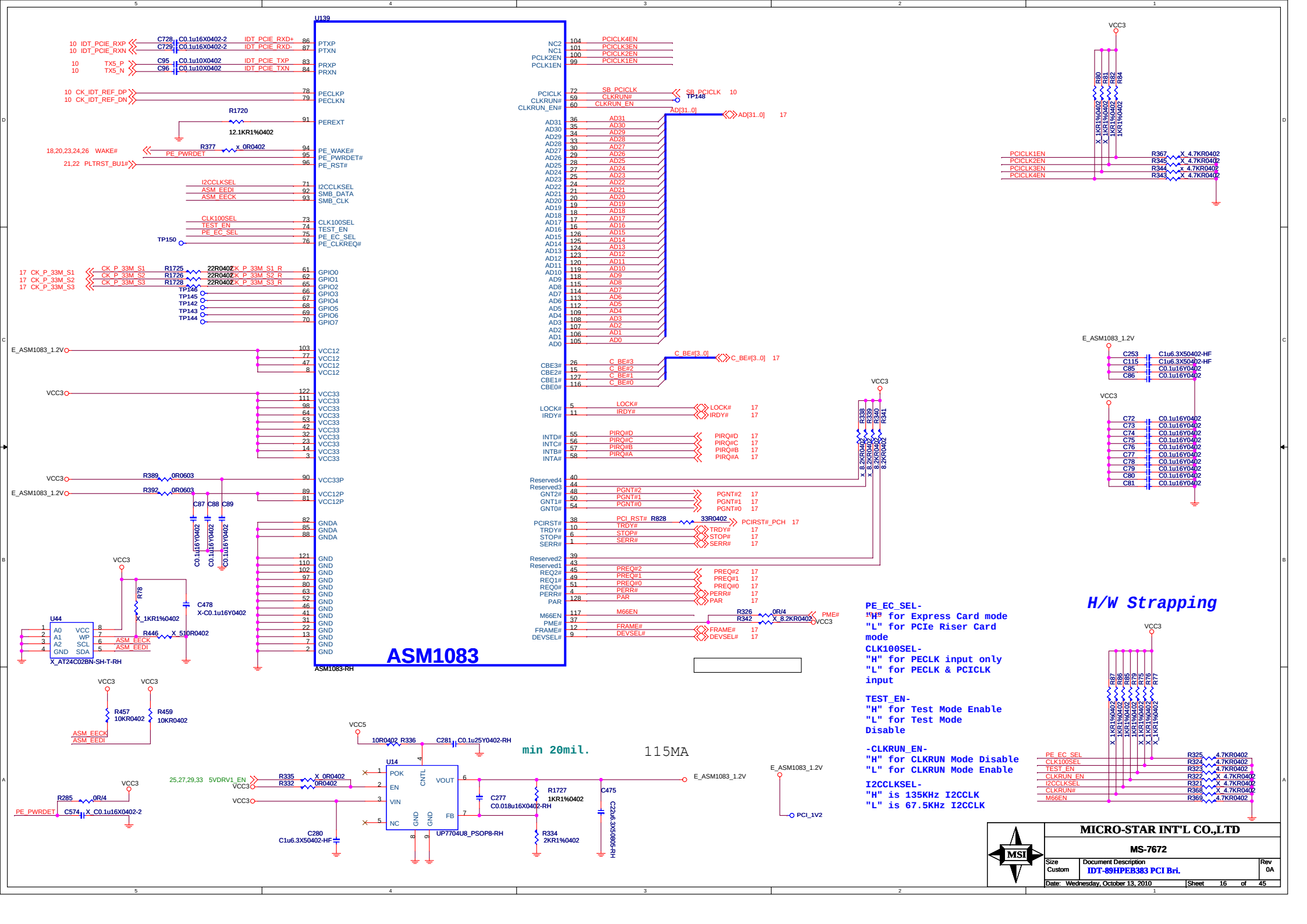
U139
ASM1083
ASM1083-RH
PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode
CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input
TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable
-CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable
I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK
H/W Strapping
min 20mil.
115MA
MICRO-STAR INT'L CO.,LTD
MS-7672
IDT-89HPEB383 PCI Bri.
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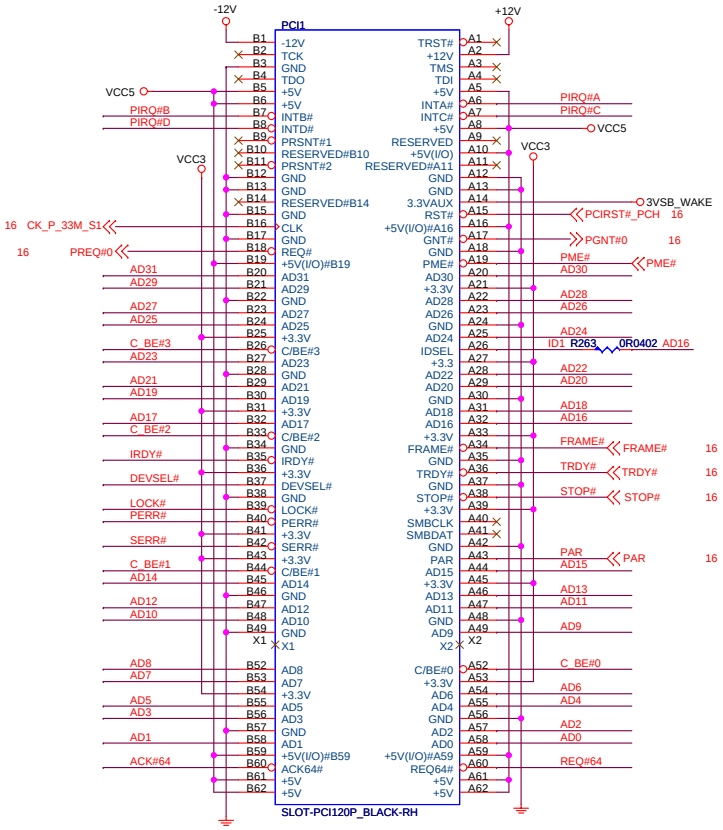
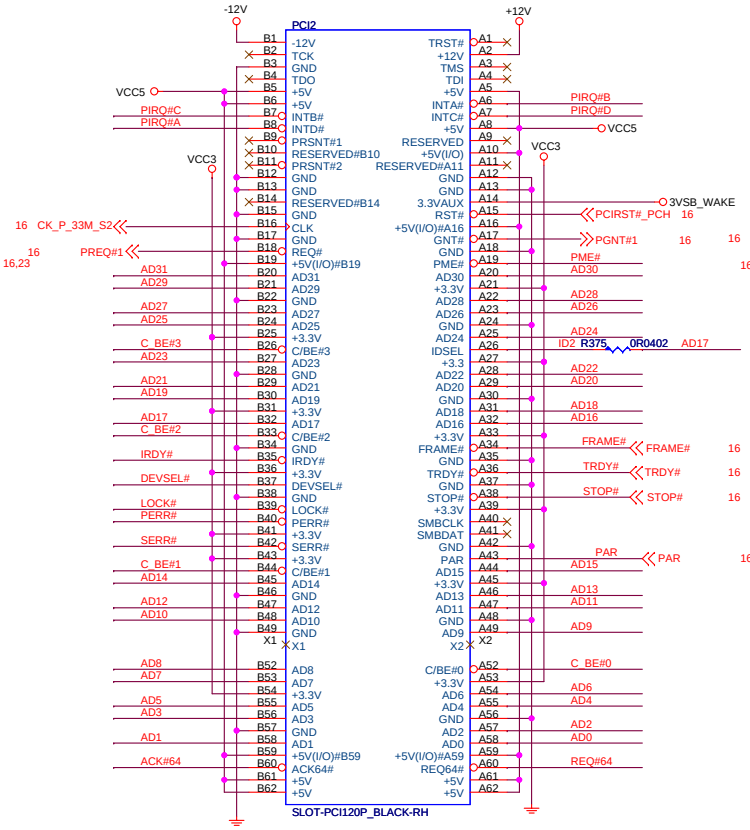
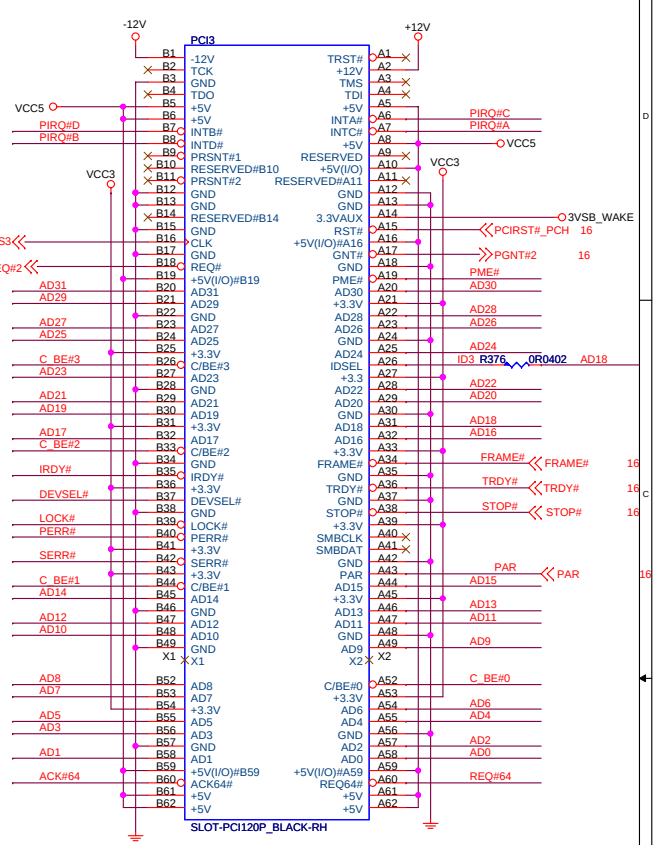
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

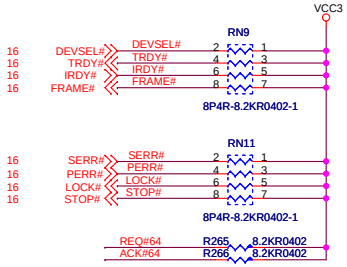


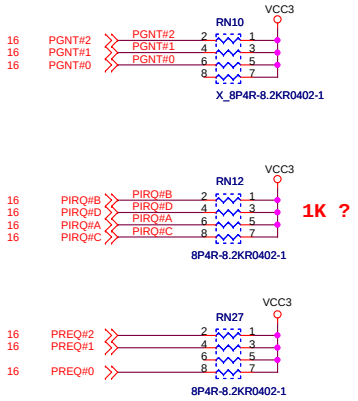
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B



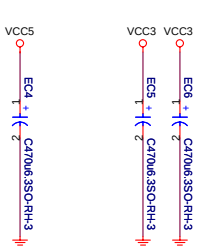
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

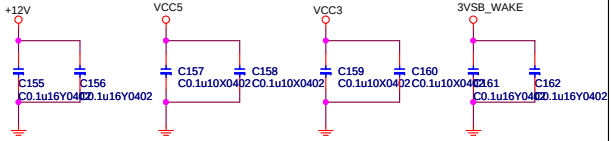
PCI PULL-UP / DOWN RESISTORS





PCI SLOT DECOUPLING CAPACITORS





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MS-7672		
Size: Custom	Document Description: PCI Slot 1 & 2 & 3	Rev: 0A
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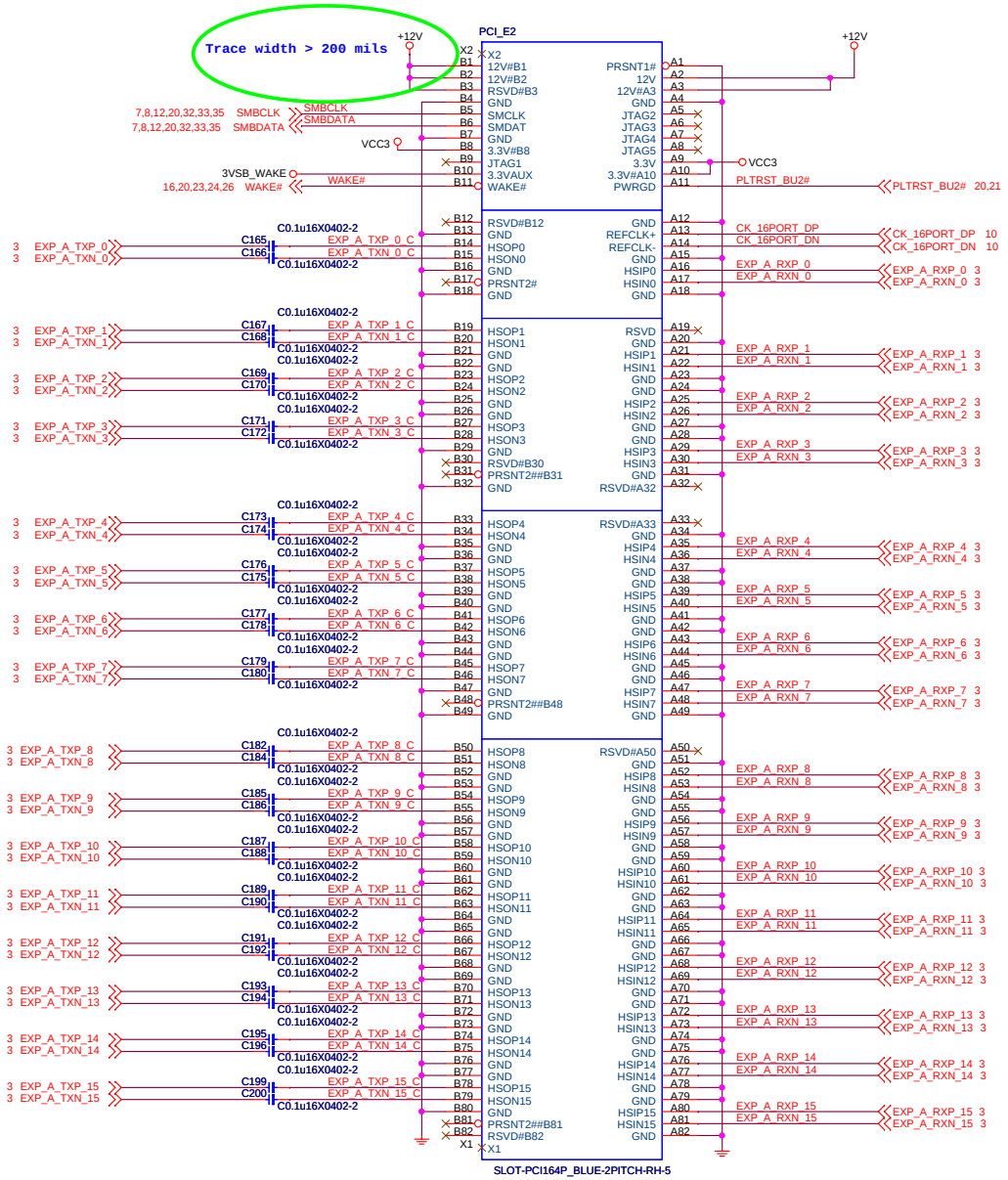
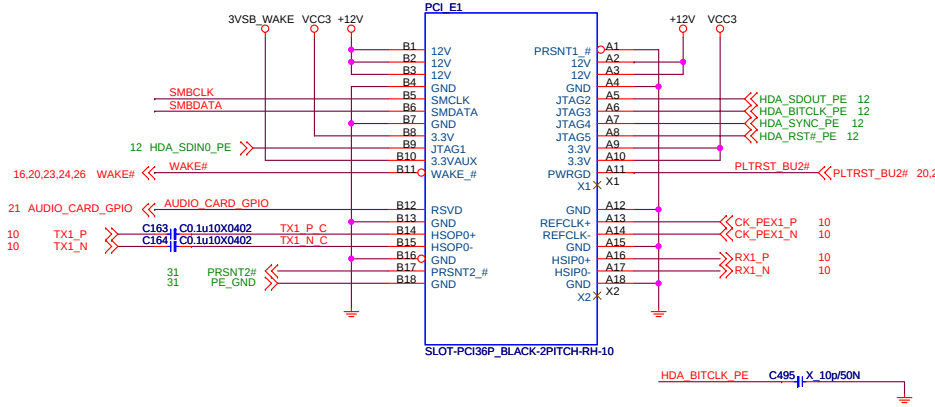
PCI_Express X16 Slot

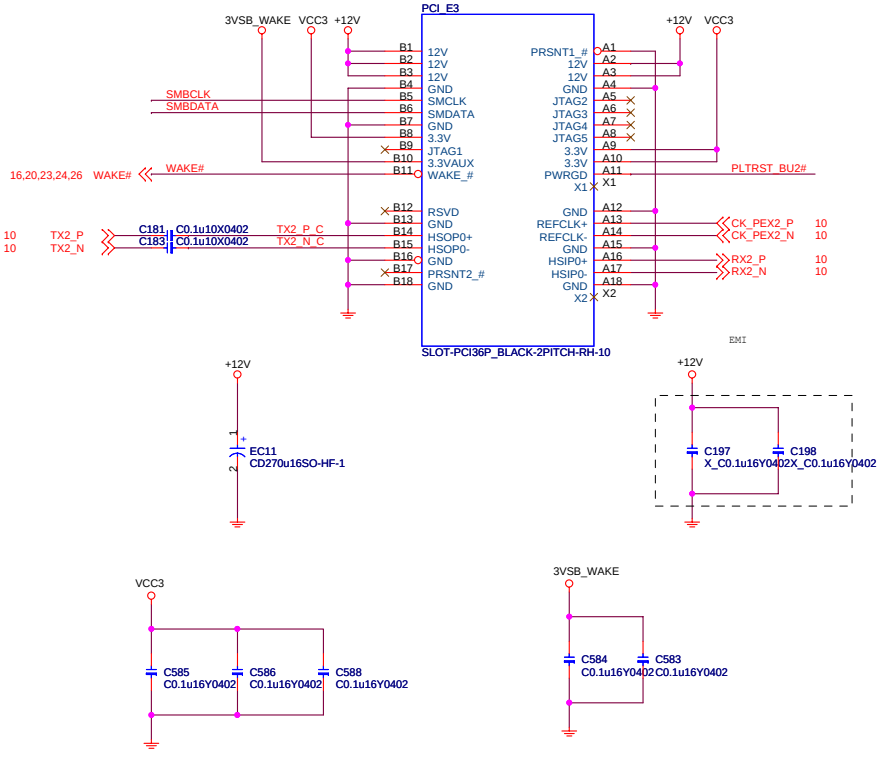


HDA co-lay PCIEx1

PCI EXPRESS x1-PORT



PCI EXPRESS x1-PORT



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MS-7672		
Size: Custom	Document Description: PCIE x16, x1	Rev: 0A
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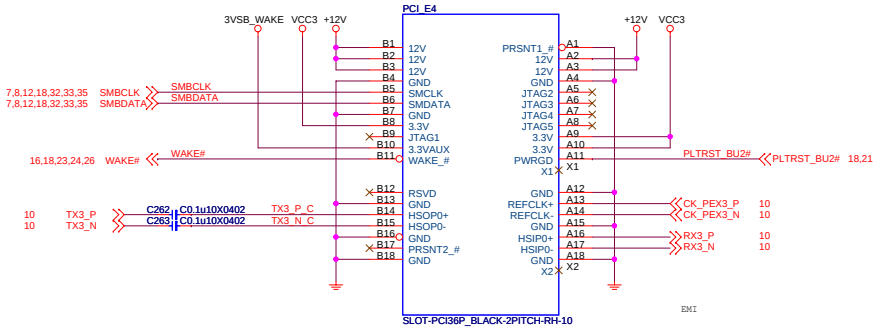
PCI EXPRESS x1-PORT



PCI EXPRESS x1-PORT

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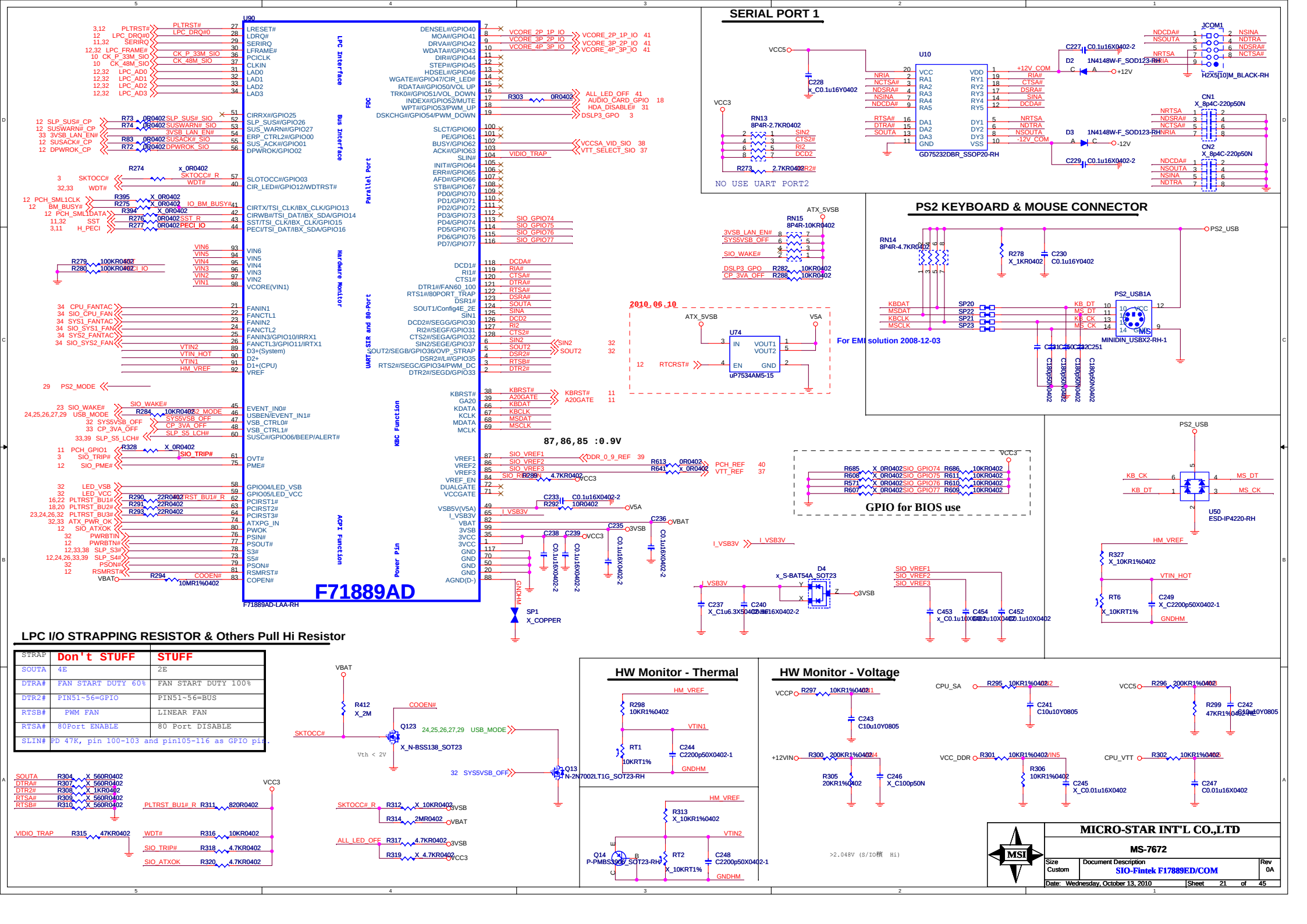

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
DTR2#	PIN51~56=GPIO	PIN51~56=BUS
RTSB#	PWM FAN	LINEAR FAN
RTSA#	80Port ENABLE	80 Port DISABLE
SLIN#	PD 47K, pin 100-103 and pin105-116 as GPIO pin.	

Size	Custom
Document Description	SIO-Fintek F71889ED/COM
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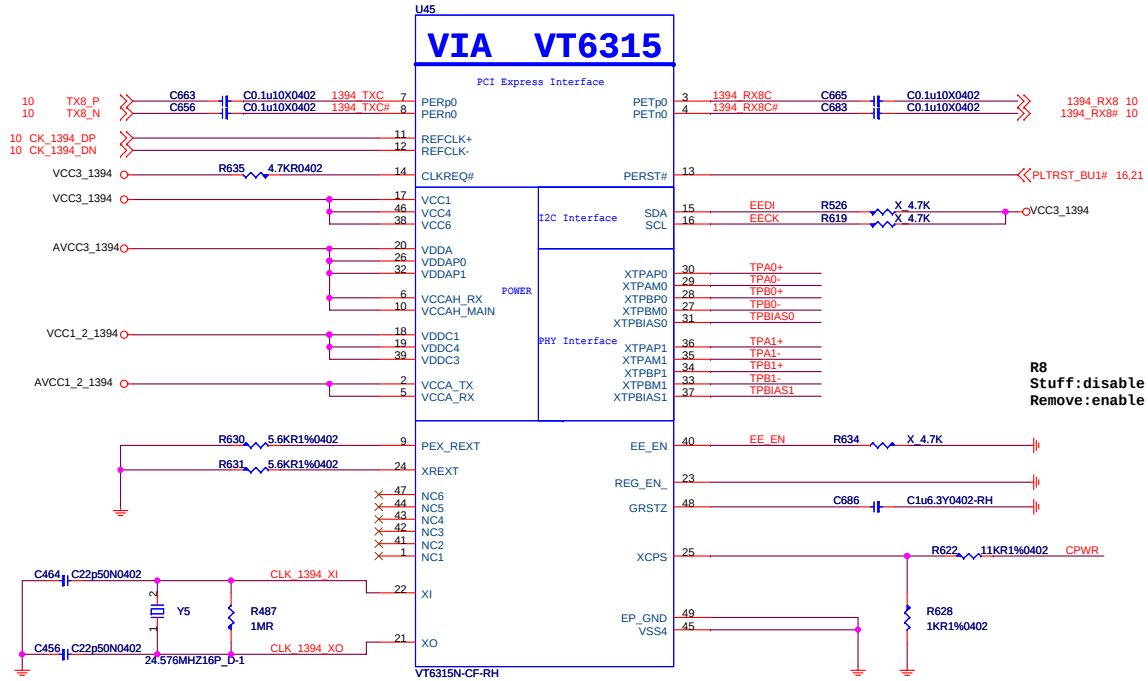
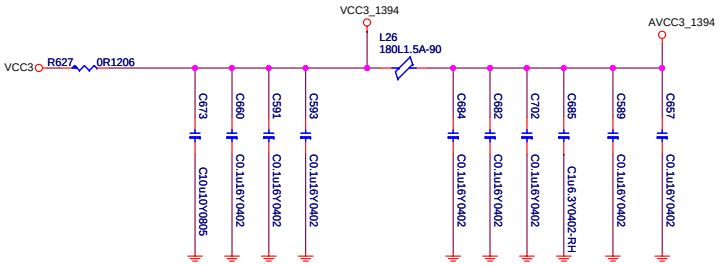
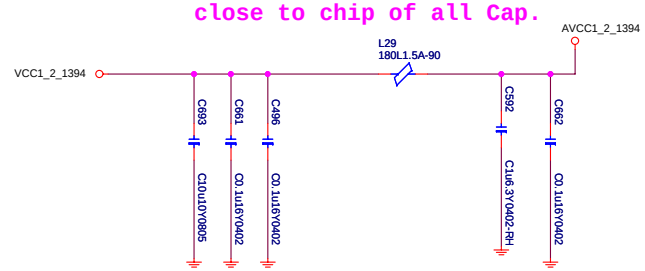
1394 CONTROLLER



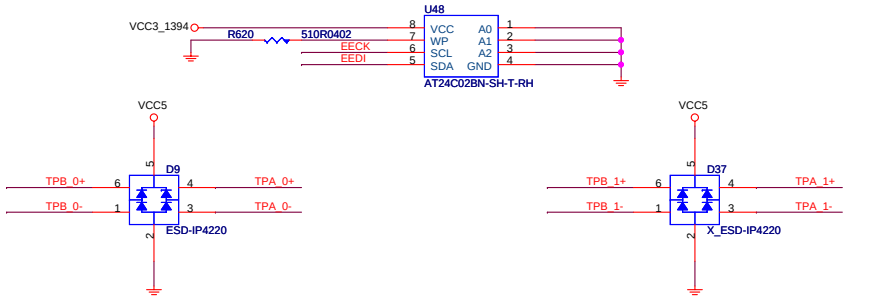
R8
Stuff:disable EE PROM
Remove:enable EE PROM



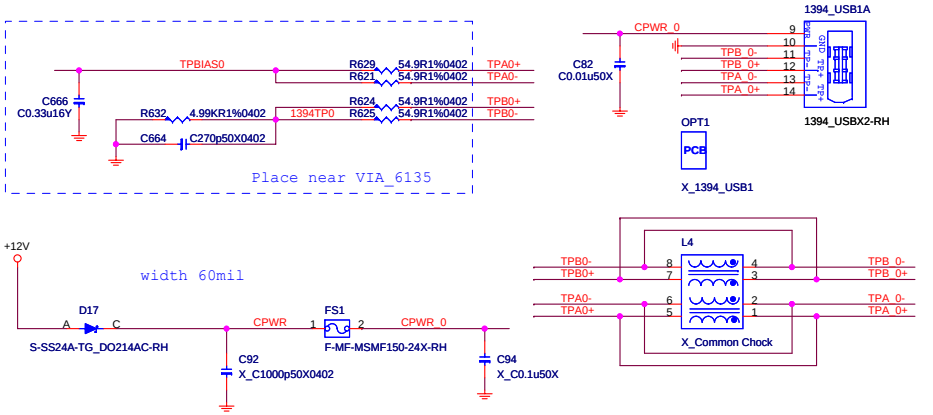
close to chip of all Cap.



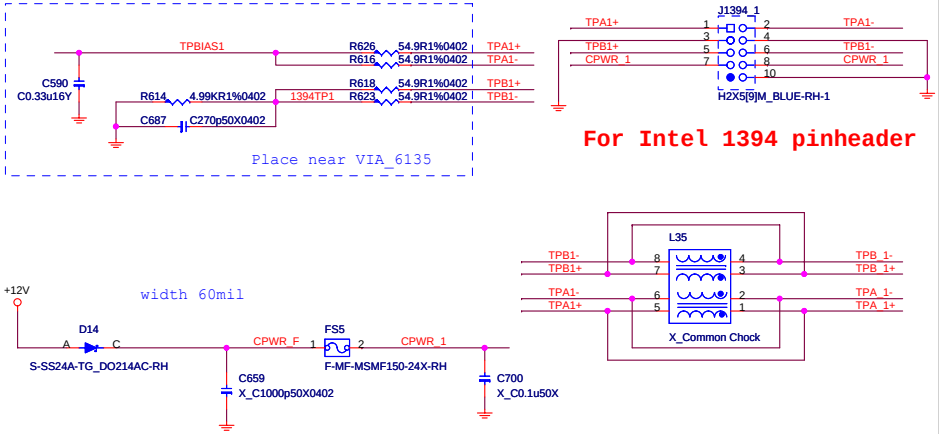
EE PROM



Rear 1394 port



Front 1394 pin header



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MS-7678		
Size: Custom	Document Description: 1394 Controller - VT6315N-CE	Rev: 08
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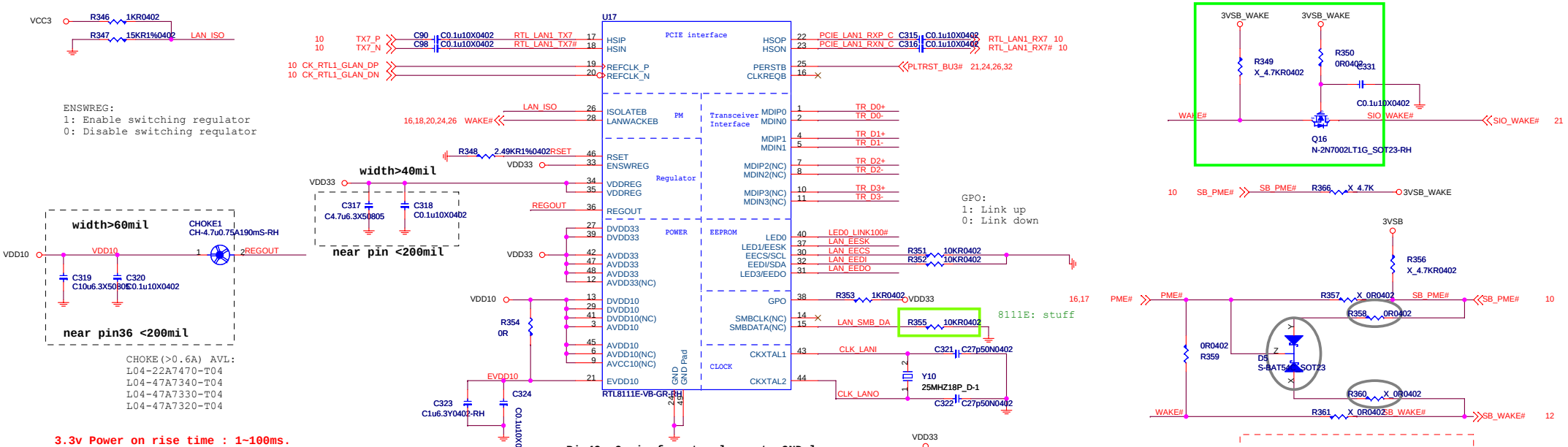
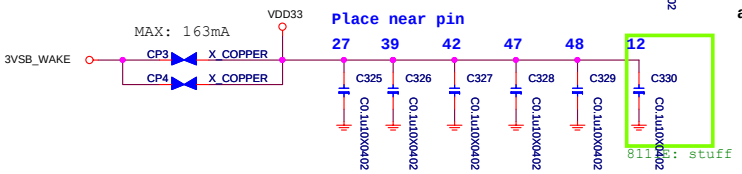
RTL8111E Giga LAN

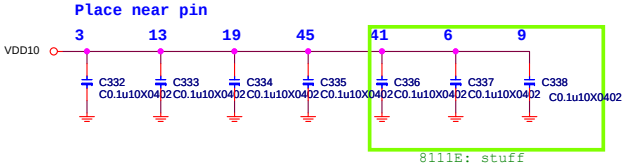
LAN/PCIE/PCI Wake Up CTRL Circuit

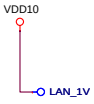


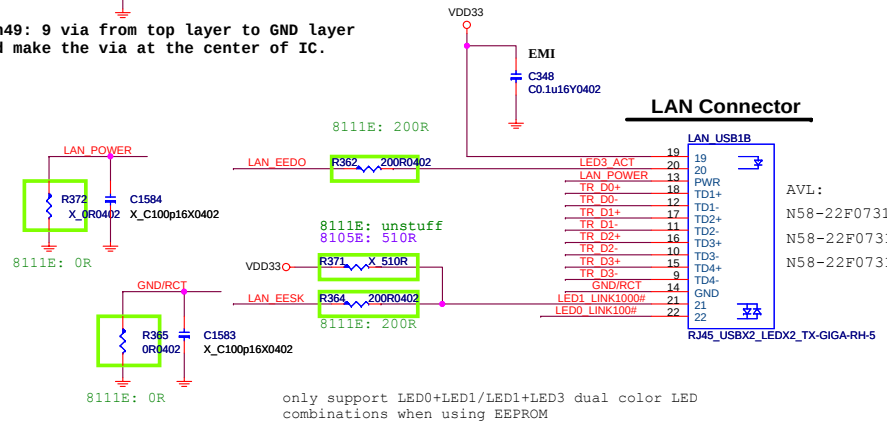
3.3v Power on rise time : 1~100ms.



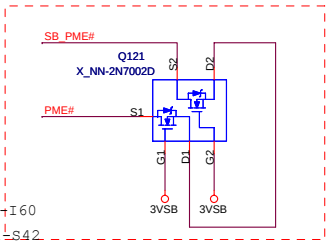
Pin49: 9 via from top layer to GND layer and make the via at the center of IC.





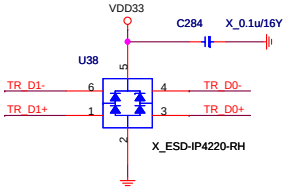


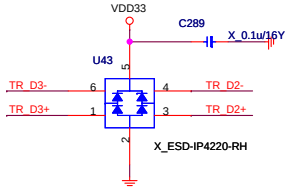
LAN Connector

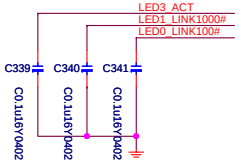


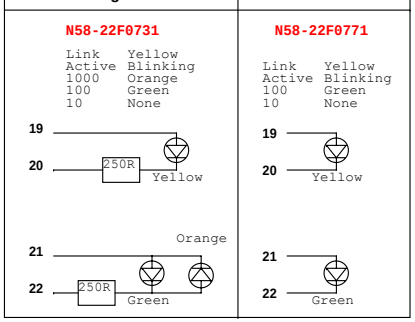
AVL:
N58-22F0731-I60
N58-22F0731-S42
N58-22F0731-U30

only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM









8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

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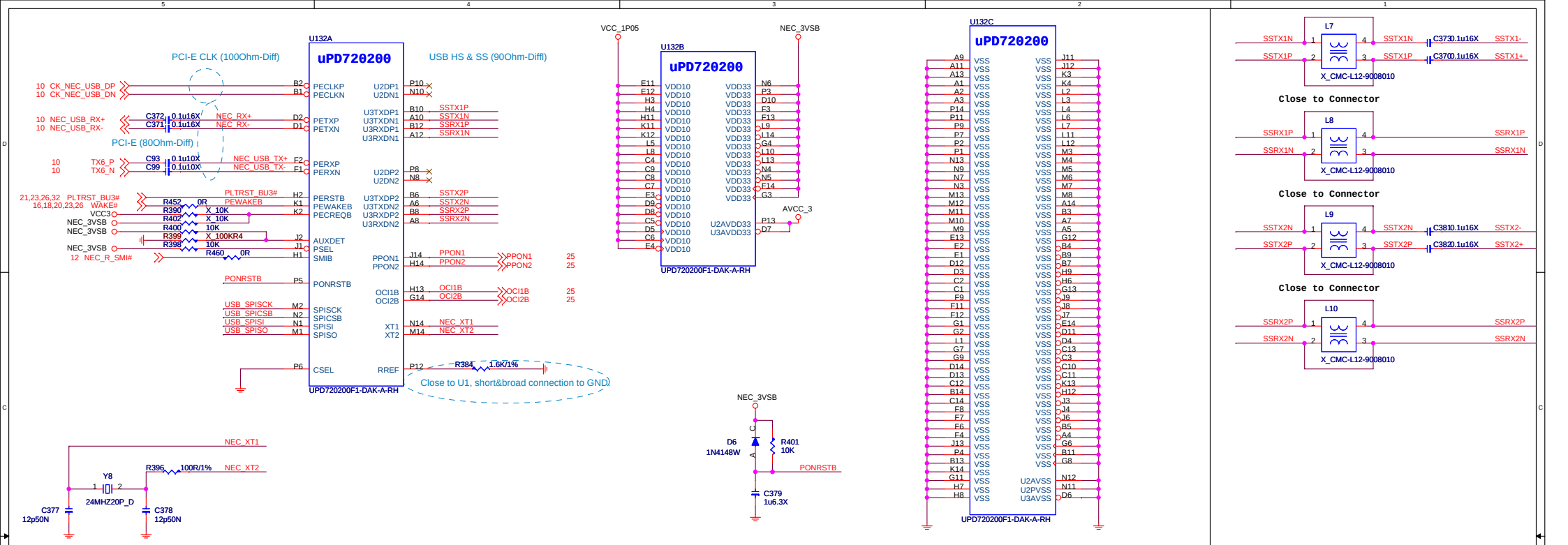

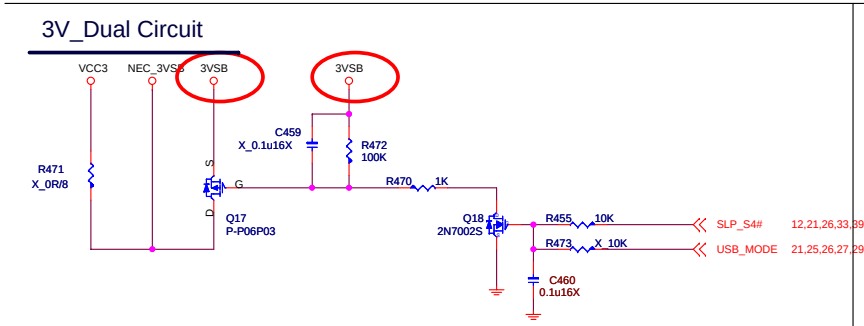

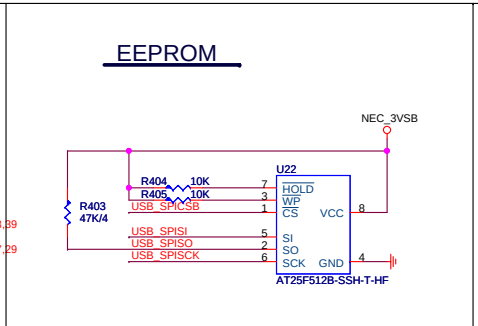

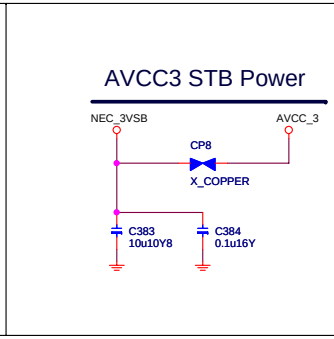

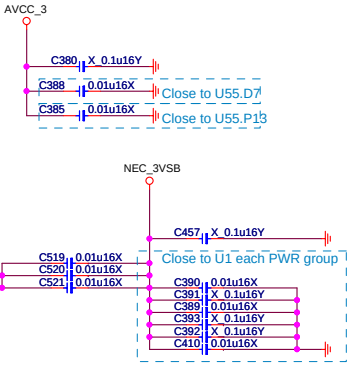

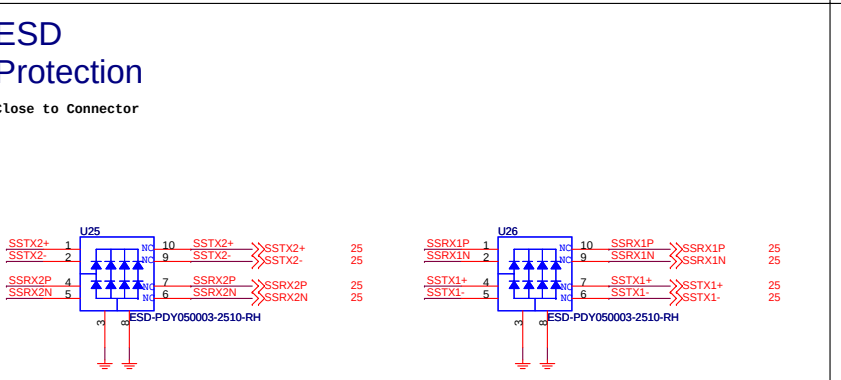

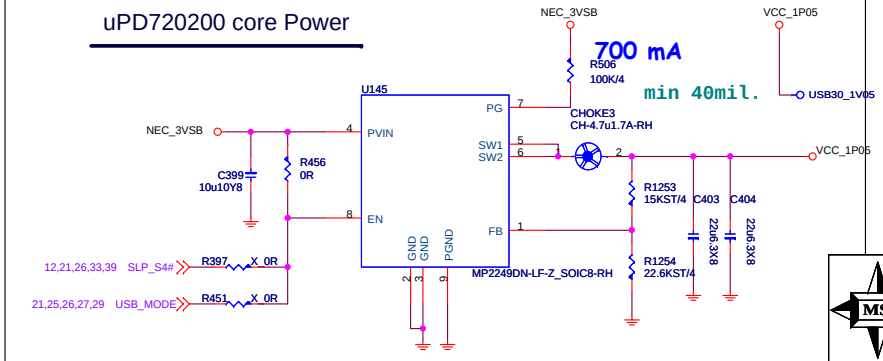

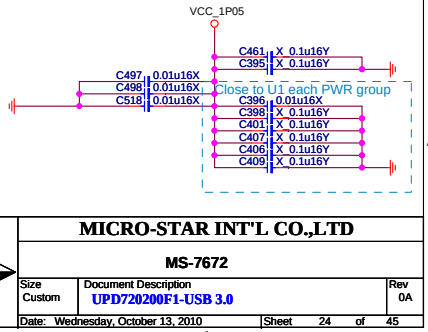

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MS-7672		
Size: Custom	Document Description: UPD720200F1-USB 3.0	Rev: 0A
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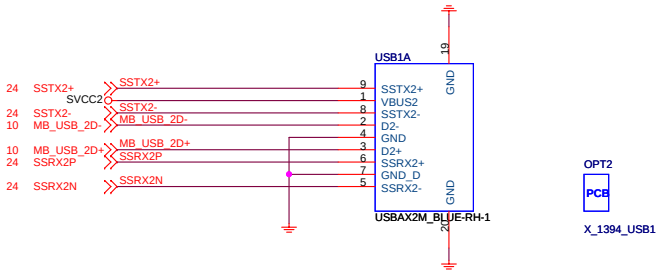
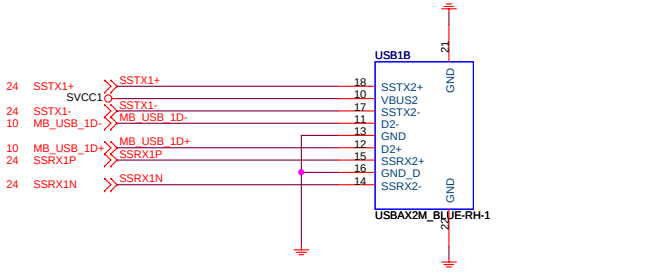
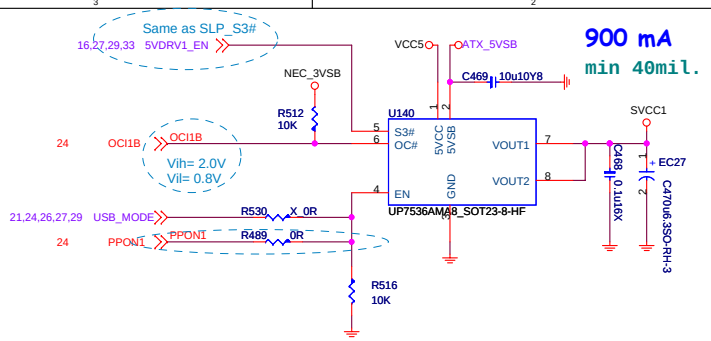
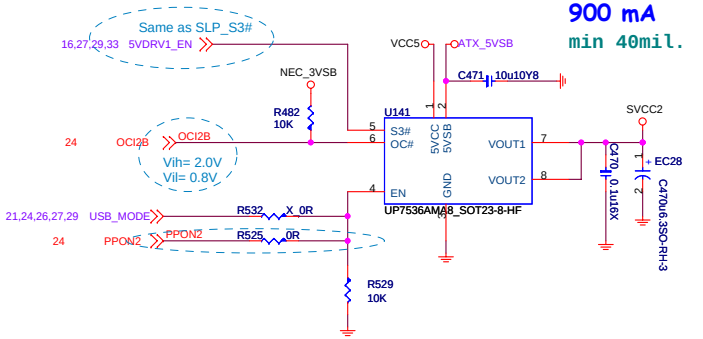


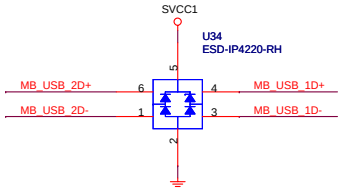


OPT2
PCB
X_1394_USB1



All power sources of uPD720200 are supplied, PPONx is enable.
PPONx is low when OCIx going to low.





Close to Connector
RN20
X_CMC-L12-9008044
MB_USB_1D-
MB_USB_1D+

Close to Connector
RN21
X_CMC-L12-9008044
MB_USB_2D-
MB_USB_2D+

MICRO-STAR INT'L CO.,LTD

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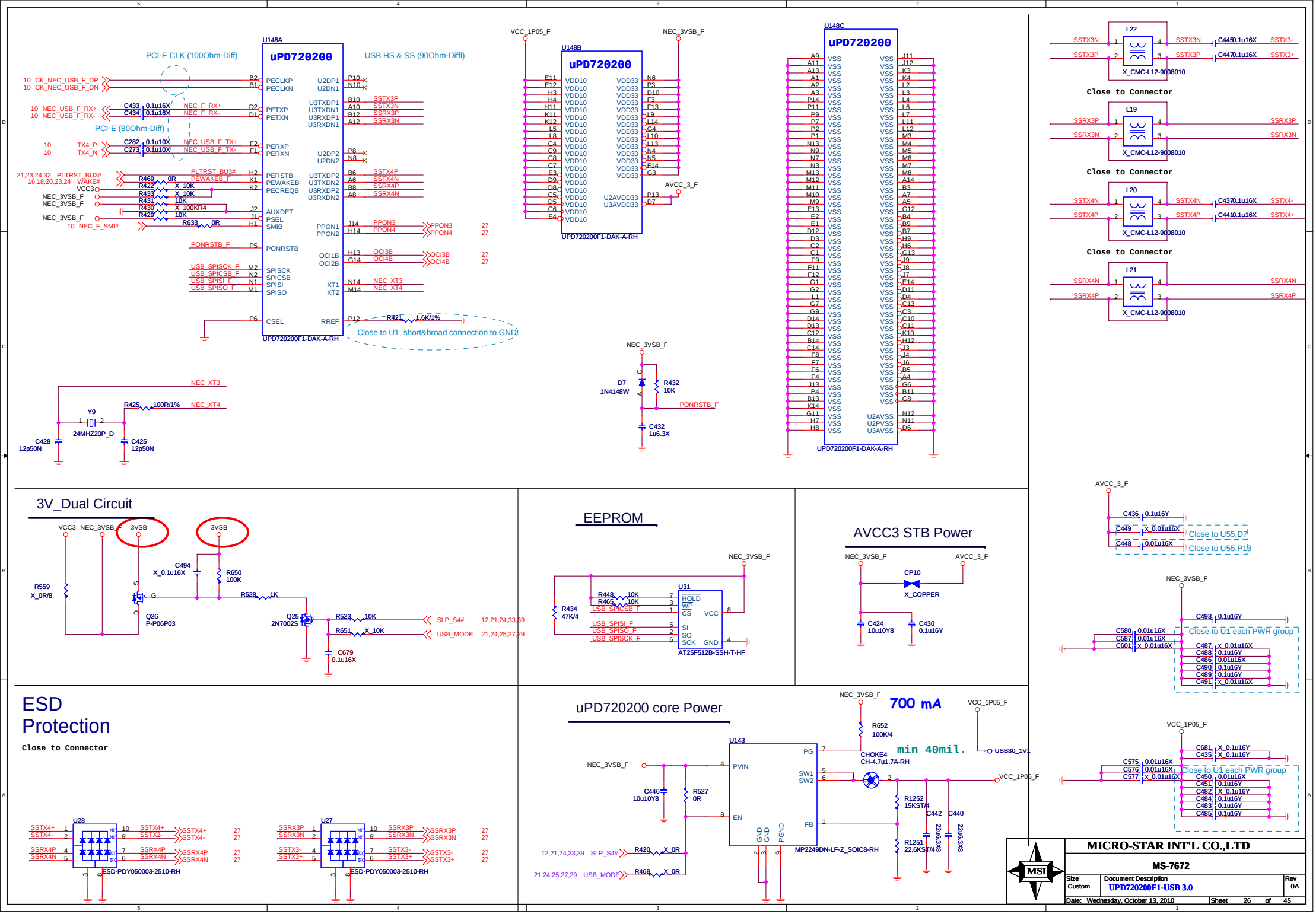
U148A
uPD720200
PCI-E CLK (100Ohm-Diff)
USB HS & SS (90Ohm-Diffl)
PCI-E (80Ohm-Diff)
PERSTB
PEWAKEB
PECREQB
AUXDET
PSEL
SMIB
PONRSTB
SPISCK
SPICSB
SPISI
SPISO
CSEL
RREF
Close to U1, short&broad connection to GND
UPD720200F1-DAK-A-RH
U148B
U148C
VCC_1P05_F
NEC_3VSB_F
AVCC_3_F
Y9
24MHZ20P_D
C428
12p50N
C425
12p50N
D7
1N4148W
R432
10K
PONRSTB_F
C432
1u6.3X
L22
L19
L20
L21
X_CMC-L12-9008010
Close to Connector
3V_Dual Circuit
Q26
P-P06P03
Q25
2N7002S
EEPROM
U31
AT25F512B-SSH-T-HF
AVCC3 STB Power
CP10
X_COPPER
C424
10u10Y8
C430
0.1u16Y
Close to U55.D7
Close to U55.P13
Close to U1 each PWR group
ESD
Protection
Close to Connector
U28
U27
ESD-PDY050003-2510-RH
uPD720200 core Power
700 mA
min 40mil.
U143
MP2249DN-LF-Z_SOIC8-RH
CHOKE4
CH-4.7u1.7A-RH
MICRO-STAR INT'L CO.,LTD
MS-7672
Size
Custom
Document Description
UPD720200F1-USB 3.0
Rev
0A
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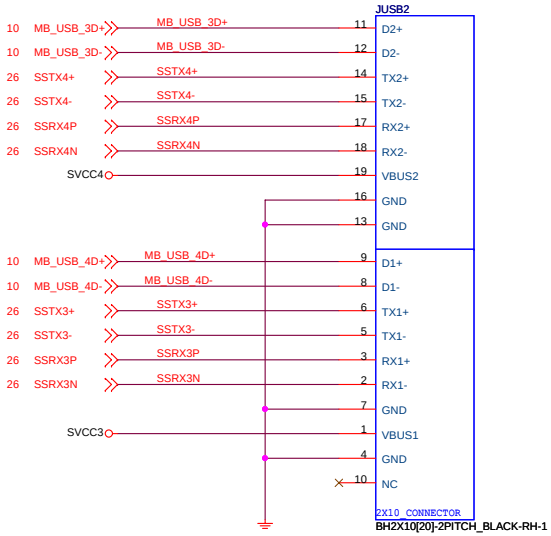
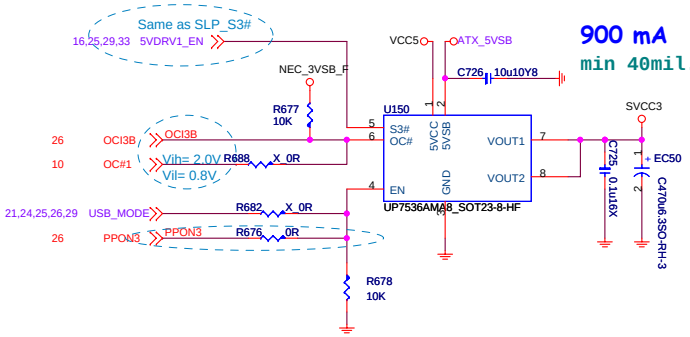
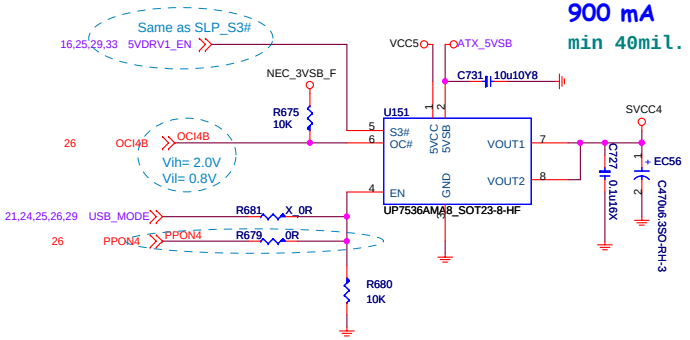
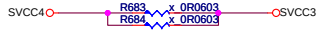
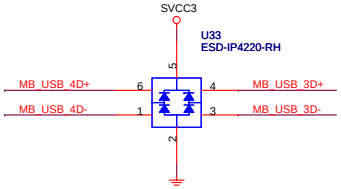


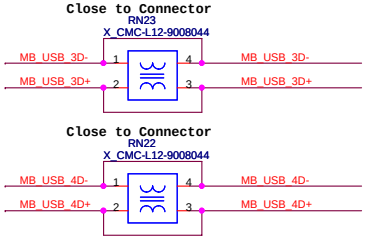


All power sources of uPD720200 are supplied, PPONx is enable.
PPONx is low when OCIx going to low.









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MS-7672		
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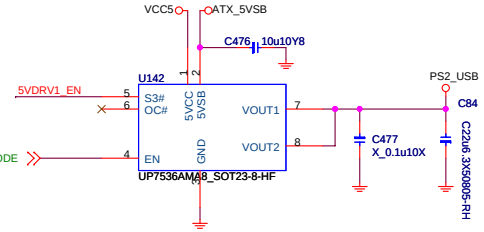
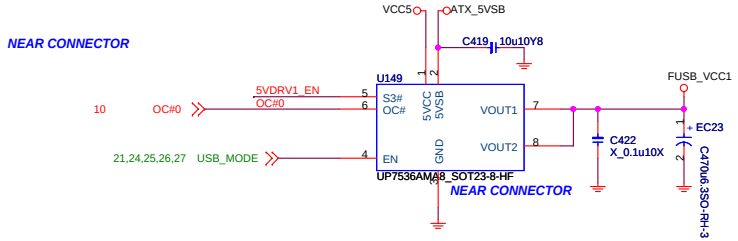
Front USB Connector

USB POWER FOR PORT 11,12

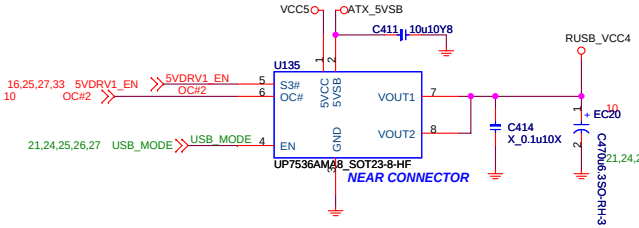


USB POWER FOR PORT 11,12

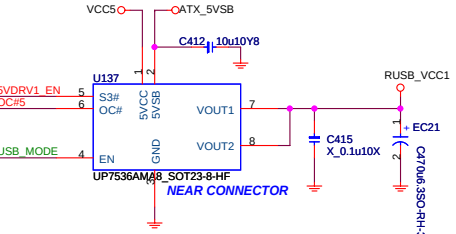


Rear USB Connector

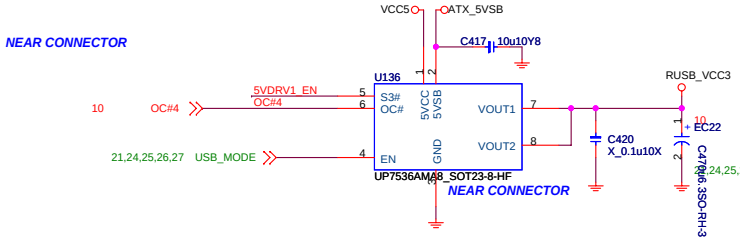
USB POWER FOR PORT 4,5



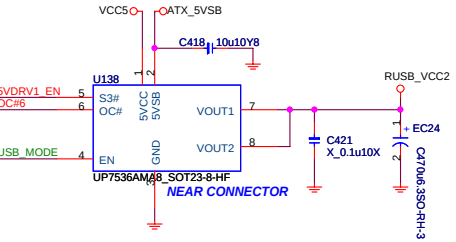
USB POWER FOR PORT 6,7



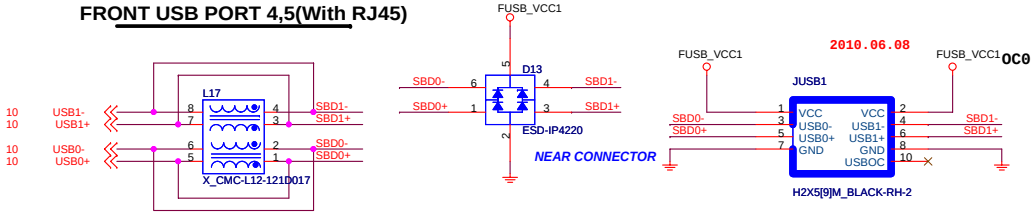
USB POWER FOR PORT 11,12



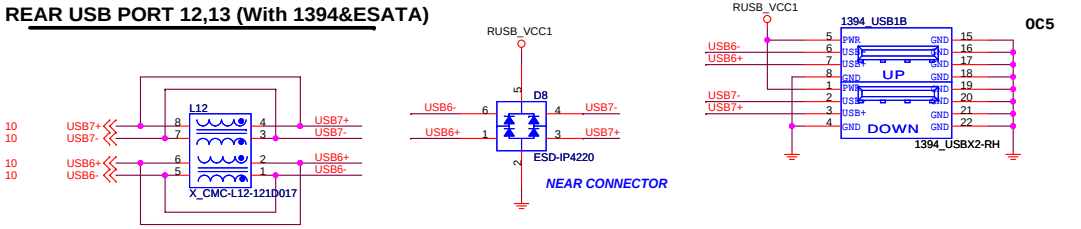
USB POWER FOR PORT 8,9



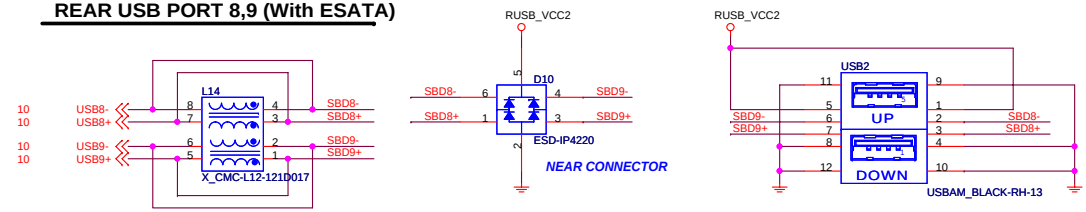
FRONT USB PORT 4,5(With RJ45)



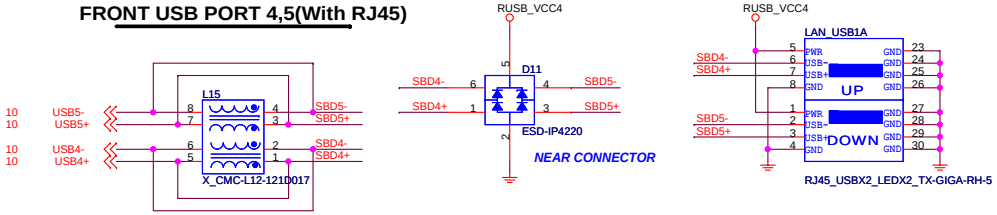
REAR USB PORT 12,13 (With 1394&ESATA)



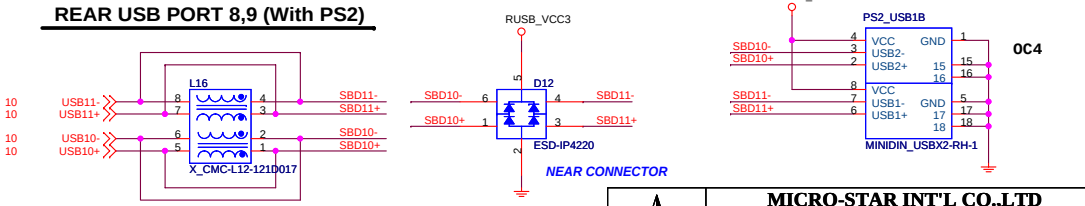
REAR USB PORT 8,9 (With ESATA)



FRONT USB PORT 4,5(With RJ45)



REAR USB PORT 8,9 (With PS2)



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MS-7672		
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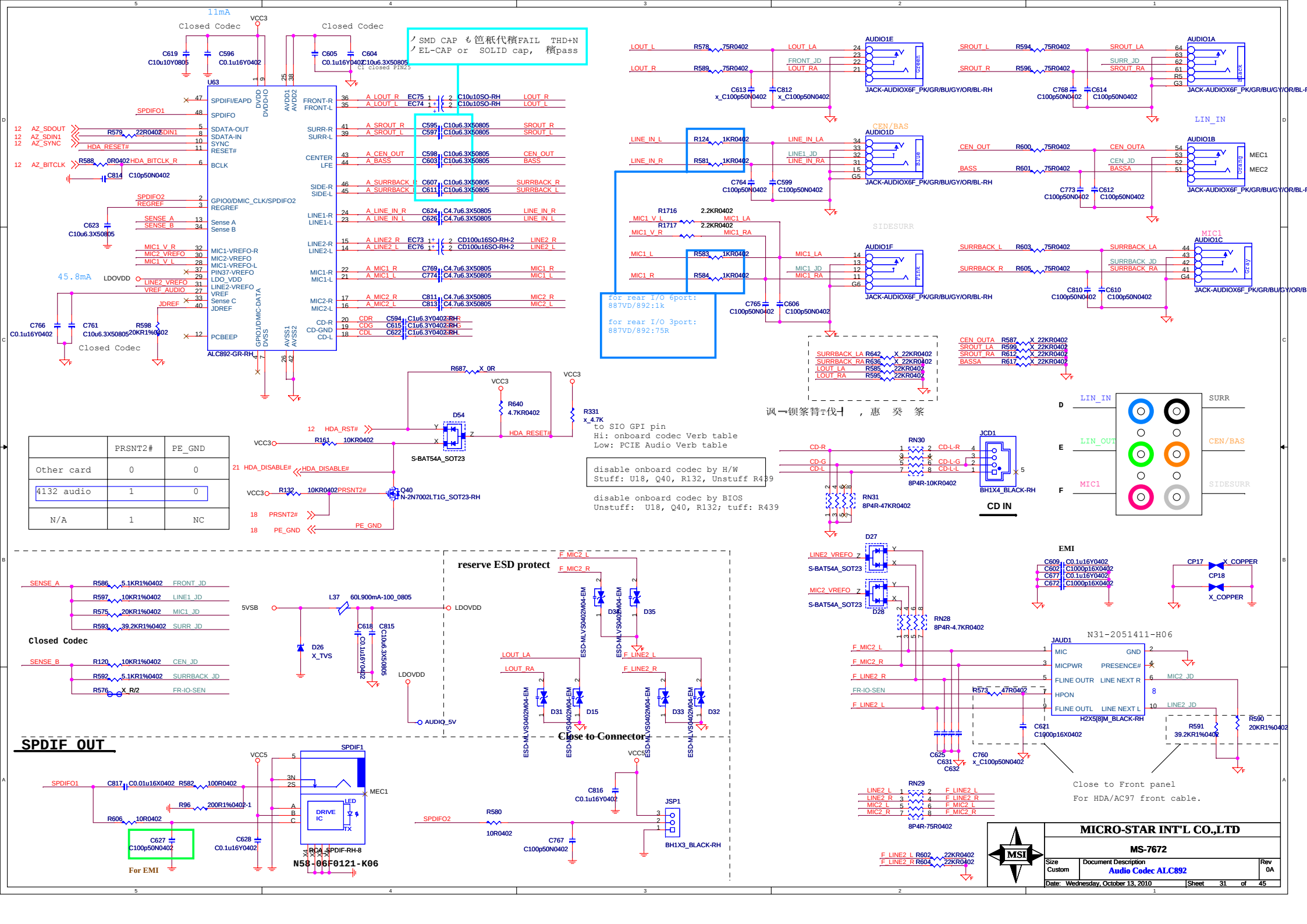
11mA
Closed Codec
VCC3
C619 C10u10Y0805
C596 C0.1u16Y0402
C605 C0.1u16Y0402
C604 C10u6.3X50805
C1 closed PIN25
SMD CAP 也爸代稹FAIL THD+N
EL-CAP or SOLID cap, 稹pass
U63
ALC892-GR-RH
SPDIFO1
SPDIFO2
REGREF
AZ_SDOUT
AZ_SDIN1
AZ_SYNC
HDA_RESET#
AZ_BITCLK
R579 22R0402
R588 0R0402
HDA_BITCLK_R
C814 C10p50N0402
C623 C10u6.3X50805
MIC1_V_R
MIC2_VREFO
MIC1_V_L
LINE2_VREFO
VREF_AUDIO
JDREF
C766 C0.1u16Y0402
C761 C10u6.3X50805
R598 20KR1%0402
45.8mA
LDOVDD
Closed Codec
FRONT-R
FRONT-L
SURR-R
SURR-L
CENTER
LFE
SIDE-R
SIDE-L
LINE1-R
LINE1-L
LINE2-R
LINE2-L
MIC1-R
MIC1-L
MIC2-R
MIC2-L
CD-R
CD-GND
CD-L
R687 X_0R
R640 4.7KR0402
R331 x_4.7K
to SIO GPI pin
Hi: onboard codec Verb table
Low: PCIE Audio Verb table
D54
S-BAT54A_SOT23
R161 10KR0402
R132 10KR0402
Q40 N-2N7002LT1G_SOT23-RH
HDA_RST#
HDA_DISABLE#
PRSNT2#
PE_GND
disable onboard codec by H/W
Stuff: U18, Q40, R132, Unstuff R439
disable onboard codec by BIOS
Unstuff: U18, Q40, R132; tuff: R439
LOUT_L
LOUT_R
R578 75R0402
R589 75R0402
AUDIO1E
JACK-AUDIOX6F_PK/GR/BU/GY/OR/BL-RH
SROUT_L
SROUT_R
R594 75R0402
R596 75R0402
AUDIO1A
LIN_IN
LINE_IN_L
LINE_IN_R
R124 1KR0402
R581 1KR0402
AUDIO1D
CEN/BAS
CEN_OUT
BASS
R600 75R0402
R601 75R0402
AUDIO1B
MEC1
MEC2
R1716 2.2KR0402
R1717 2.2KR0402
MIC1_V_L
MIC1_V_R
MIC1_L
MIC1_R
R583 1KR0402
R584 1KR0402
AUDIO1F
SIDESURR
for rear I/O 6port:
887VD/892:1k
for rear I/O 3port:
887VD/892:75R
SURRBACK_L
SURRBACK_R
R603 75R0402
R605 75R0402
AUDIO1C
MIC1
SURRBACK_LA R642 X_22KR0402
SURRBACK_RA R636 X_22KR0402
LOUT_LA R585 22KR0402
LOUT_RA R595 22KR0402
CEN_OUTA R587 X_22KR0402
SROUT_LA R599 X_22KR0402
SROUT_RA R612 X_22KR0402
BASSA R617 X_22KR0402
讽一钡笨臂T伐┫ ，惠 癸 笨
RN30 8P4R-10KR0402
RN31 8P4R-47KR0402
JCD1 BH1X4_BLACK-RH
CD IN
CD-R
CD-G
CD-L
LIN_IN
LIN_OUT
MIC1
SURR
CEN/BAS
SIDESURR
SENSE_A
SENSE_B
R586 5.1KR1%0402 FRONT_JD
R597 10KR1%0402 LINE1_JD
R575 20KR1%0402 MIC1_JD
R593 39.2KR1%0402 SURR_JD
R120 10KR1%0402 CEN_JD
R592 5.1KR1%0402 SURRBACK_JD
R576 X_R/2 FR-IO-SEN
Closed Codec
reserve ESD protect
5VSB
L37 60L900mA-100_0805
D26 X_TVS
C618 C0.1u16Y0402
C815 C10u6.3X50805
LDOVDD
AUDIO_5V
F_MIC2_L
F_MIC2_R
F_LINE2_L
F_LINE2_R
D34 D35 D31 D15 D33 D32
ESD-MLVS0402M04-EM
LOUT_LA
LOUT_RA
Close to Connector
D27 D28
S-BAT54A_SOT23
LINE2_VREFO
MIC2_VREFO
RN28 8P4R-4.7KR0402
EMI
C609 C0.1u16Y0402
C602 C1000p16X0402
C677 C0.1u16Y0402
C672 C1000p16X0402
CP17 X_COPPER
CP18 X_COPPER
N31-2051411-H06
JAUD1
H2X5[8]M_BLACK-RH
MIC
GND
MICPWR
PRESENCE#
FLINE OUTR
LINE NEXT R
HPON
FLINE OUTL
LINE NEXT L
FR-IO-SEN
R573 47R0402
MIC2_JD
LINE2_JD
C621 C1000p16X0402
C625
C631
C632
C760 x_C100p50N0402
R590 20KR1%0402
R591 39.2KR1%0402
RN29 8P4R-75R0402
Close to Front panel
For HDA/AC97 front cable.
SPDIF OUT
SPDIFO1
C817 C0.01u16X0402
R582 100R0402
R96 200R1%0402-1
R606 10R0402
C627 C100p50N0402
For EMI
C628 C0.1u16Y0402
SPDIF1
MEC1
DRIVE IC
RCA_SPDIF-RH-8
N58-06F0121-K06
SPDIFO2
R580 10R0402
C767 C100p50N0402
C816 C0.1u16Y0402
JSP1
BH1X3_BLACK-RH
PRSNT2# PE_GND
Other card 0 0
4132 audio 1 0
N/A 1 NC
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MS-7672
Size Custom
Document Description
Audio Codec ALC892
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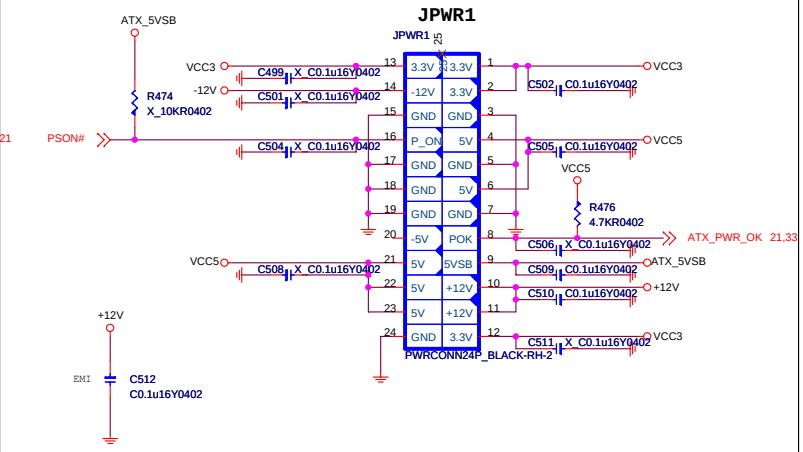
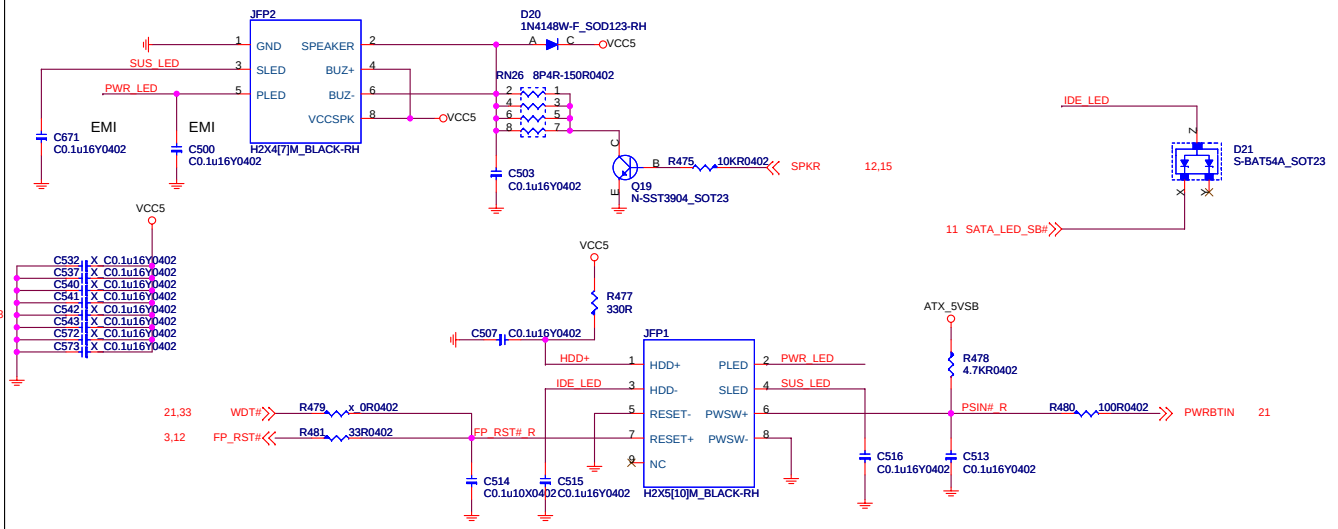
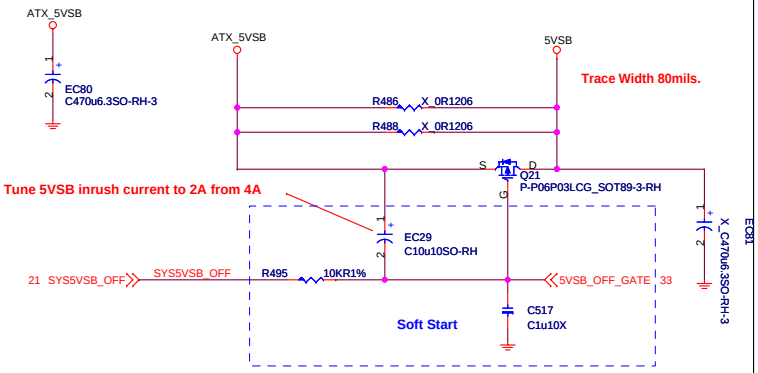
ATX POWER CONNECTOR



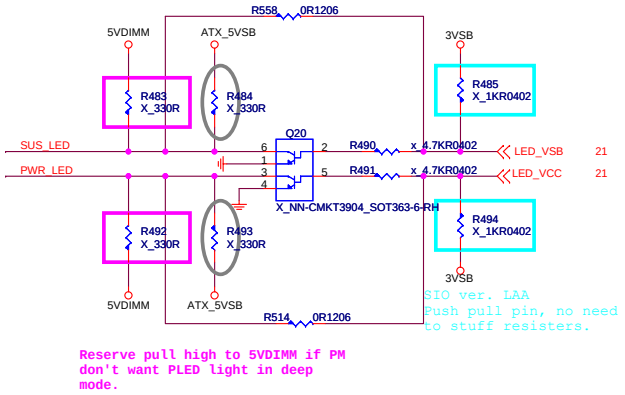
FRONT PANNEL



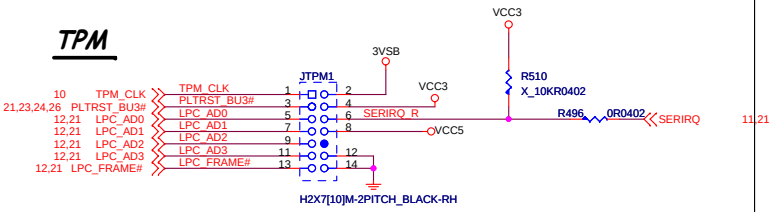
5VSB Power Switch

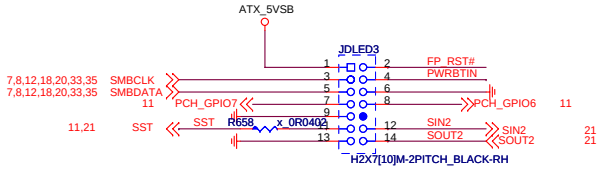


LED (for Fintek 71889)



TPM





MICRO-STAR INT'L CO.,LTD

MS-7672

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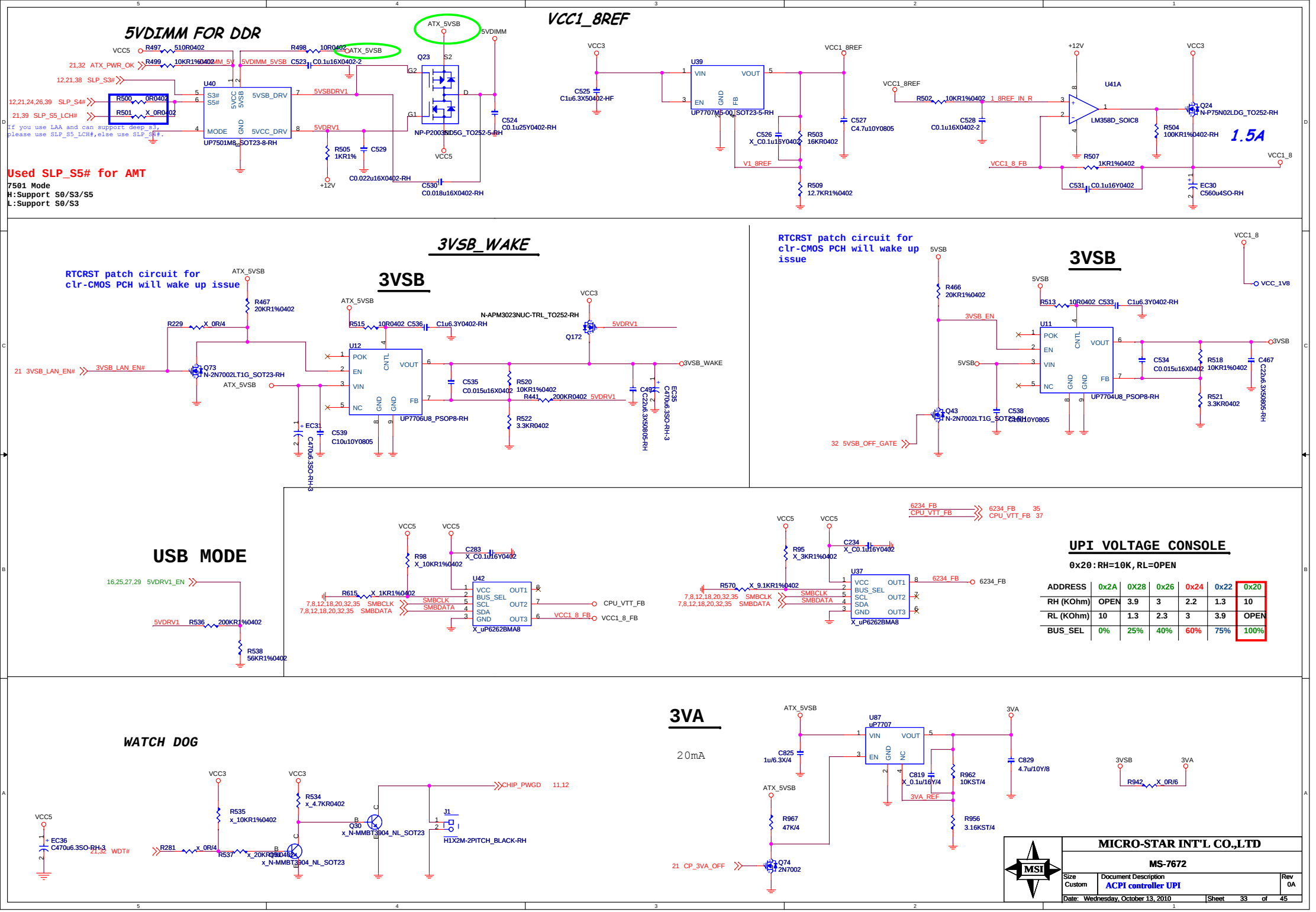
5VDIMM FOR DDR
VCC1_8REF
3VSB_WAKE
3VSB
RTCRST patch circuit for clr-CMOS PCH will wake up issue
Used SLP_S5# for AMT
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3
USB MODE
UPI VOLTAGE CONSOLE
0x20:RH=10K,RL=OPEN
ADDRESS 0x2A 0X28 0x26 0x24 0x22 0x20
RH (KOhm) OPEN 3.9 3 2.2 1.3 10
RL (KOhm) 10 1.3 2.3 3 3.9 OPEN
BUS_SEL 0% 25% 40% 60% 75% 100%
WATCH DOG
3VA
20mA
MICRO-STAR INT'L CO.,LTD
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ACPI controller UPI
Date: Wednesday, October 13, 2010
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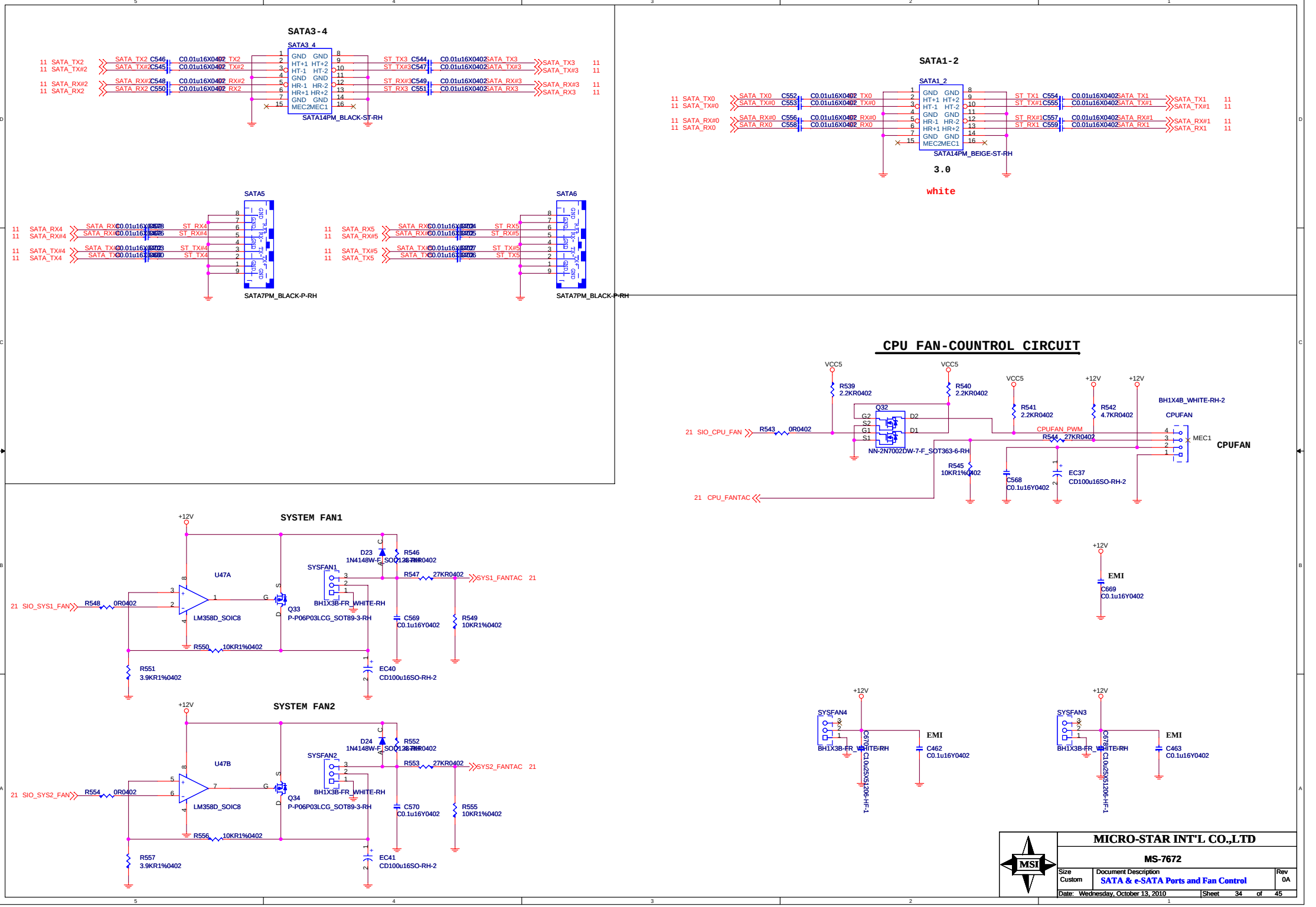
SATA3-4
SATA3_4
SATA14PM_BLACK-ST-RH
SATA1-2
SATA1_2
SATA14PM_BEIGE-ST-RH
3.0
white
SATA5
SATA7PM_BLACK-P-RH
SATA6
SATA7PM_BLACK-P-RH
CPU_FAN-COUNTROL_CIRCUIT
NN-2N7002DW-7-F_SOT363-6-RH
BH1X4B_WHITE-RH-2
CPUFAN
SYSTEM FAN1
SYSTEM FAN2
LM358D_SOIC8
P-P06P03LCG_SOT89-3-RH
BH1X3B-FR_WHITE-RH
CD100u16SO-RH-2
EMI
MICRO-STAR INT'L CO.,LTD
MS-7672
SATA & e-SATA Ports and Fan Control
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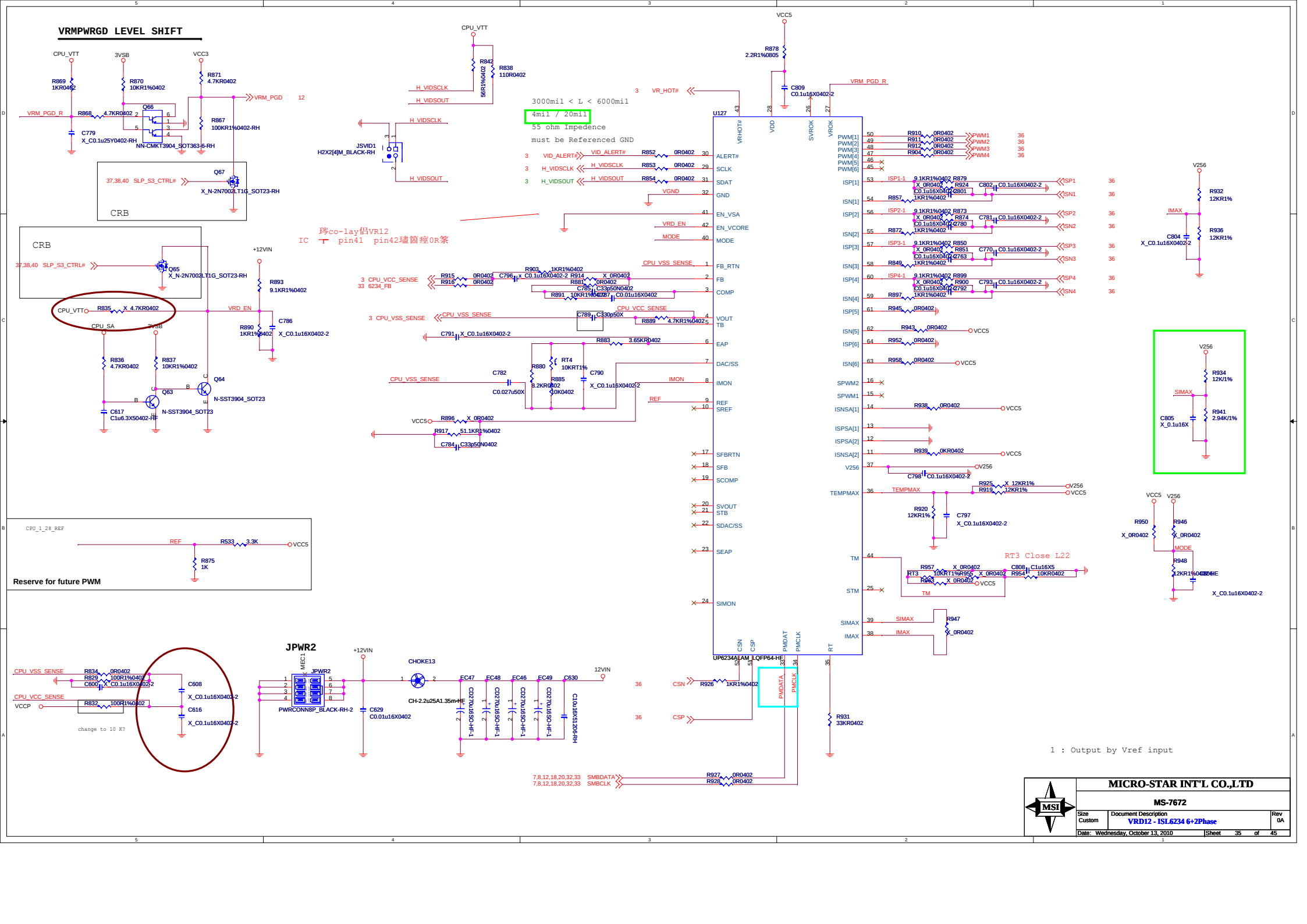
VRMPWRGD LEVEL SHIFT
CRB
CRB
Reserve for future PWM
JPWR2
珍co-lay侶VR12
IC ┬ pin41 pin42瑾箇痤0R笨
3000mil < L < 6000mil
4mil / 20mil
55 ohm Impedence
must be Referenced GND
RT3 Close L22
1 : Output by Vref input
UP6234ALAM_LQFP64-HF
MICRO-STAR INT'L CO.,LTD
MS-7672
VRD12 - ISL6234 6+2Phase
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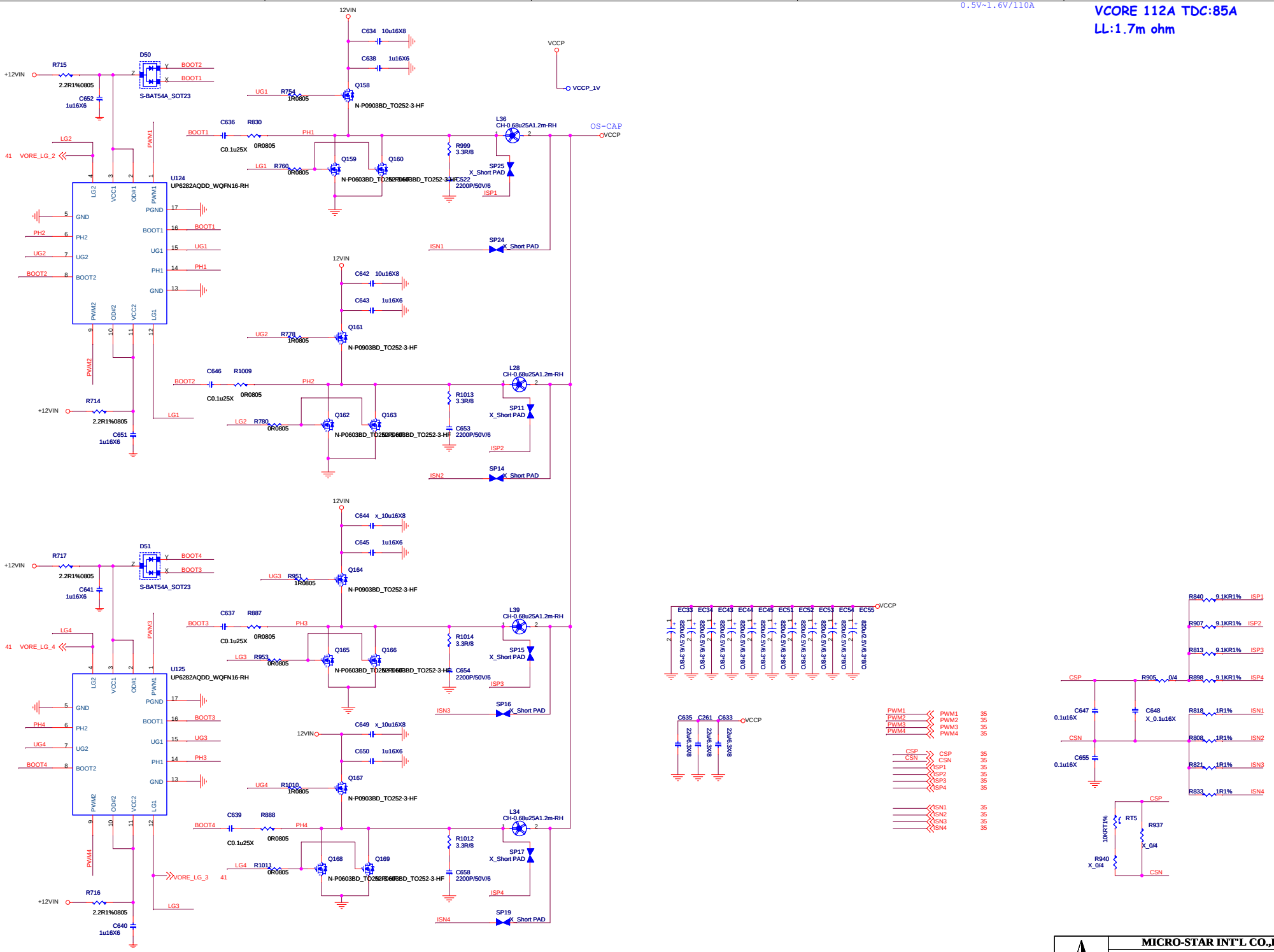
0.5V~1.6V/110A

VCORE 112A TDC:85A
LL:1.7m ohm



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7672	
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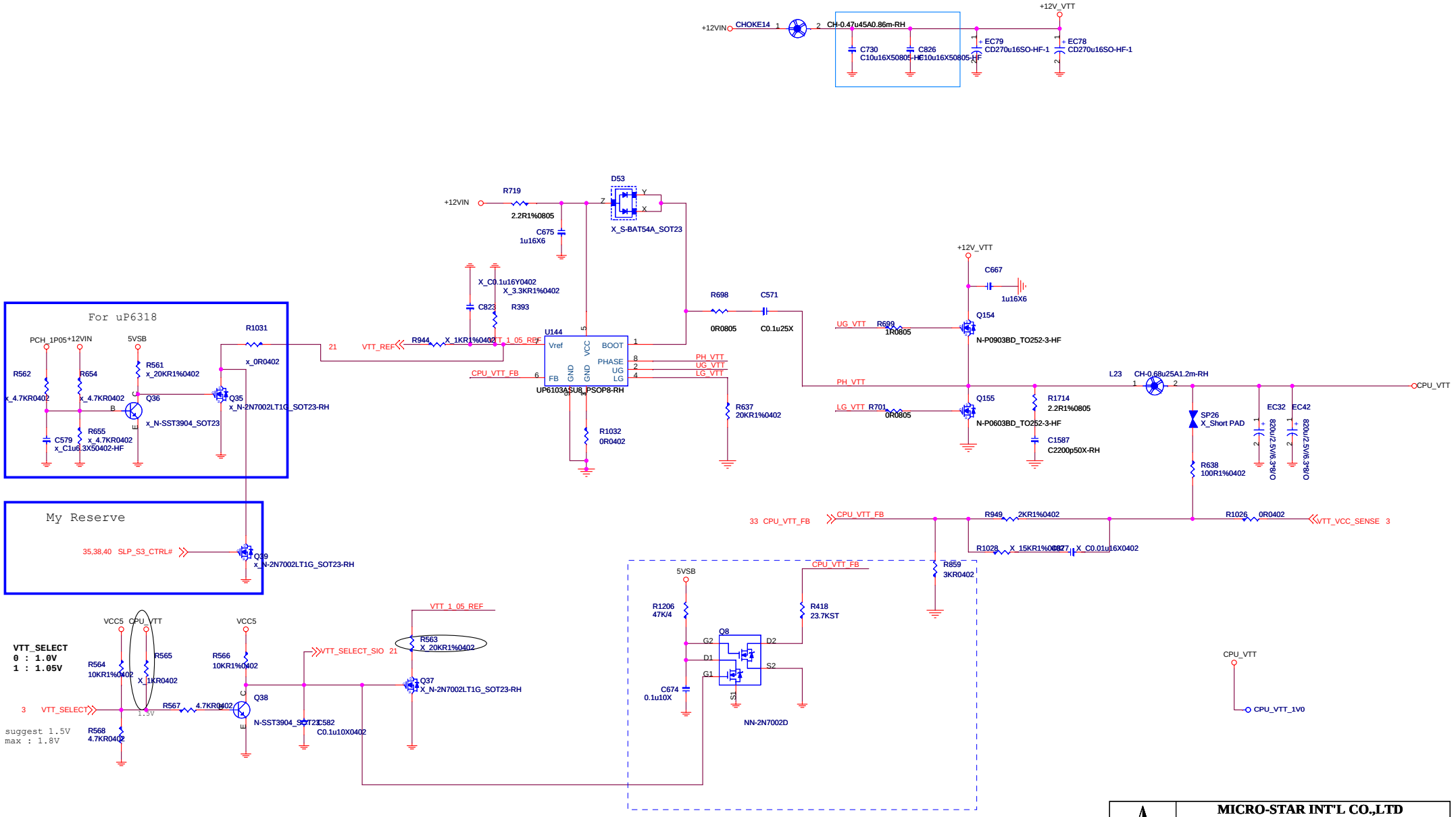
CPU_VTT:1.05/1.00

CPU VTT 8.2A

Iripple=1.9(vtt)+1.8(sa)
5*2=10A>3.8A



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7672	
Size: Custom	Document Description: CPU_VTT- uP6138 1-Phase	Rev: 0A
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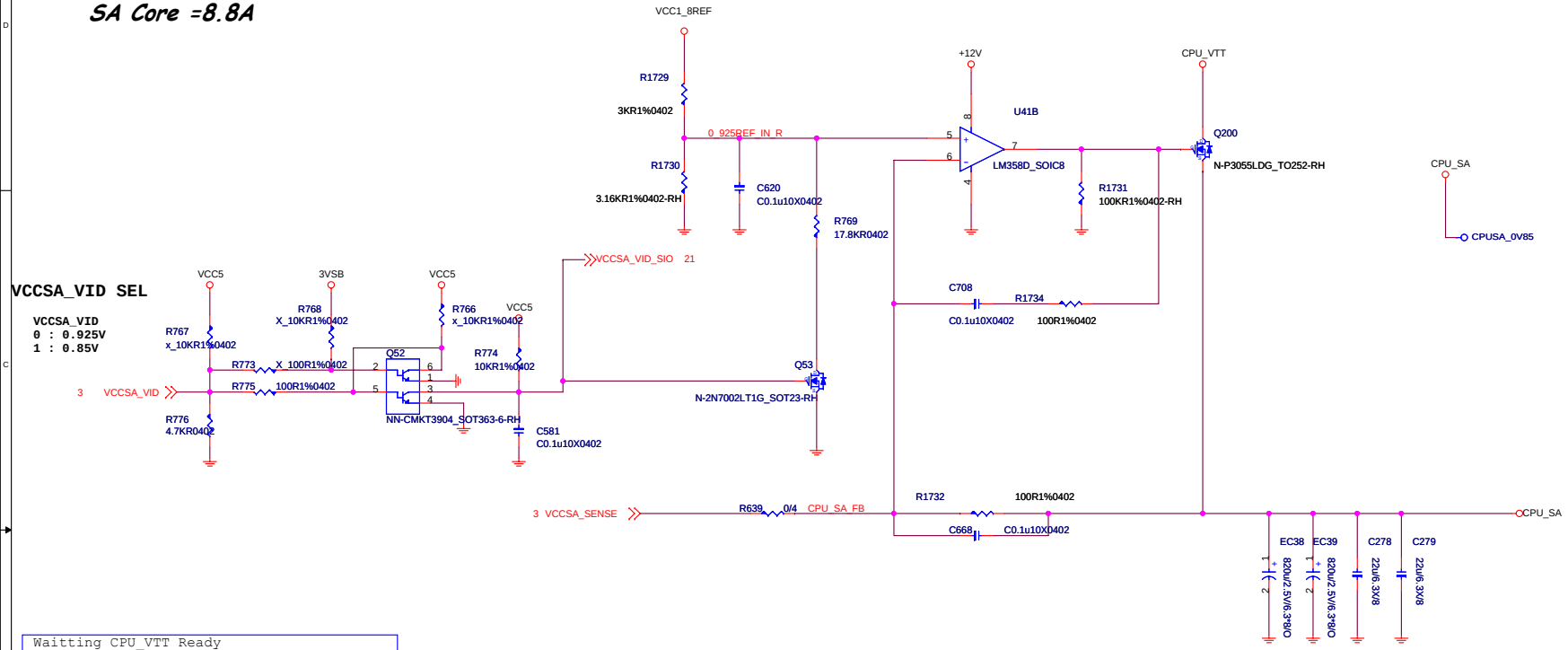
CPU_SA:0.925/0.85

SA Core =8.8A



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7672	
Size: Custom	Document Description: CPU_SA-uP6113-1Dr.MOS	Rev: 0A
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DDR3_1.5V 4.5A+15A+1A=20.5A

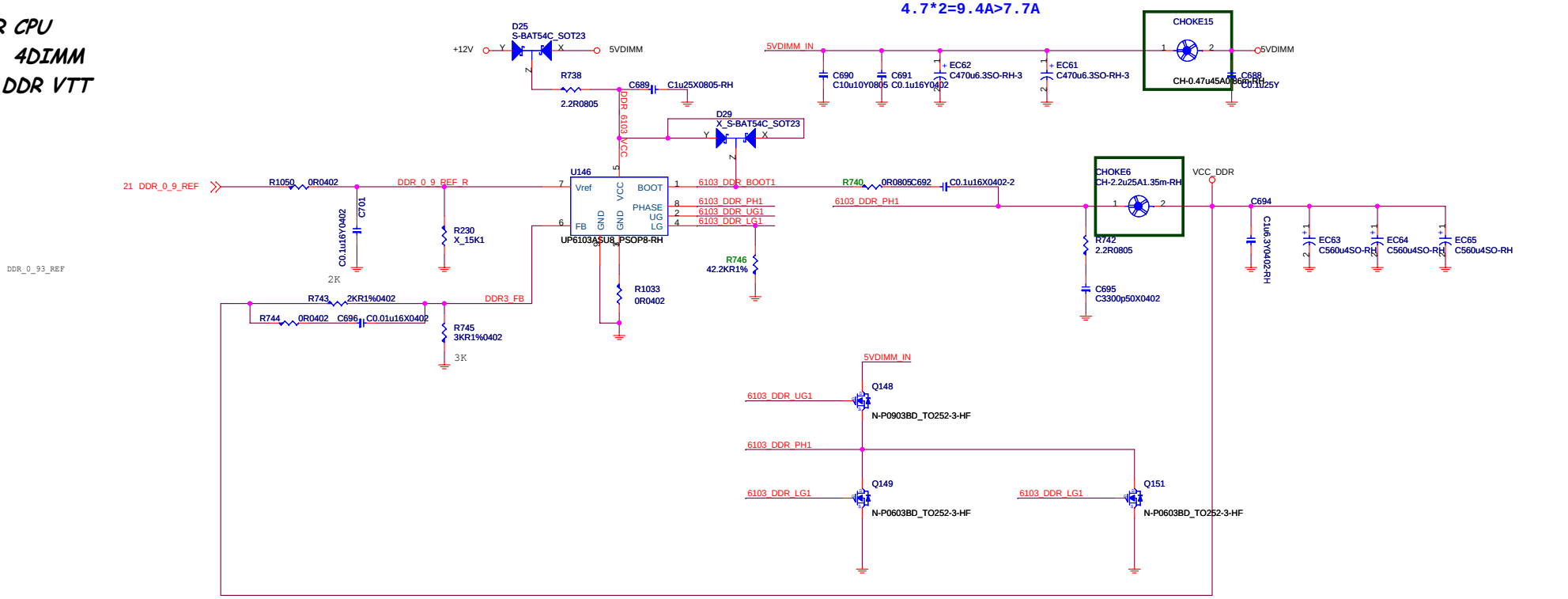
4.5A FOR CPU

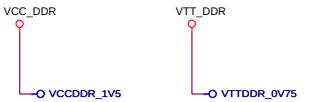
15A FOR 4DIMM

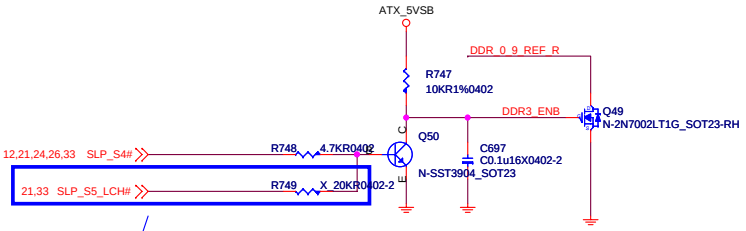
1A FOR DDR VTT

Iripple=7.7A

4.7*2=9.4A>7.7A







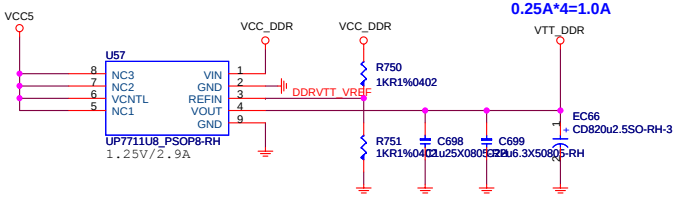
Meet Intel Power Down Sequence

If you use LAA and can support deep_s3,
please use SLP_S5_LCH#,else use SLP_S4#.

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

0.25A*4=1.0A



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MS-7672		
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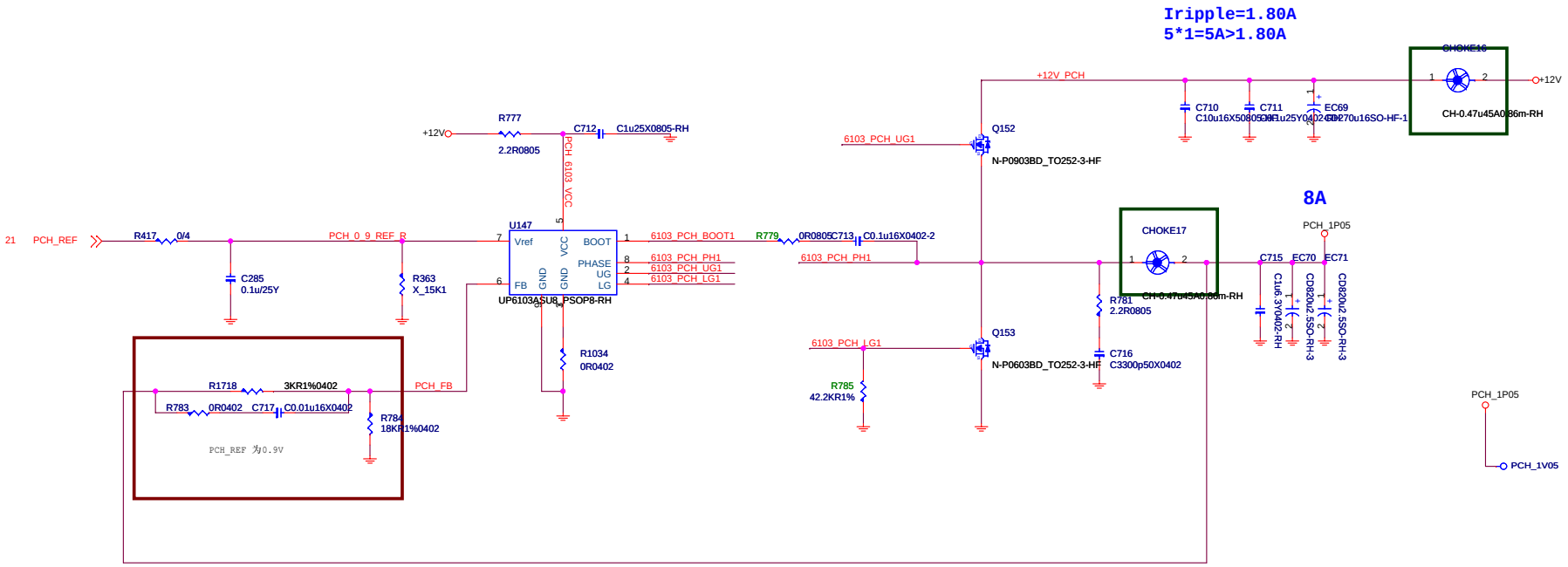
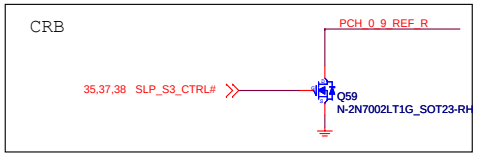
PCH Core 6.2A+1.8A=8A





	uP6103A	uP6138
PIN1	BOOT	BOOT
PIN2	UG	UG
PIN3	GND	VREFIN
PIN4	LG	LG
PIN5	VCC	VCC
PIN6	FB	FB
PIN7	Vref	OCP/EN
PIN8	PHASE	PHASE
PIN9	GND	GND

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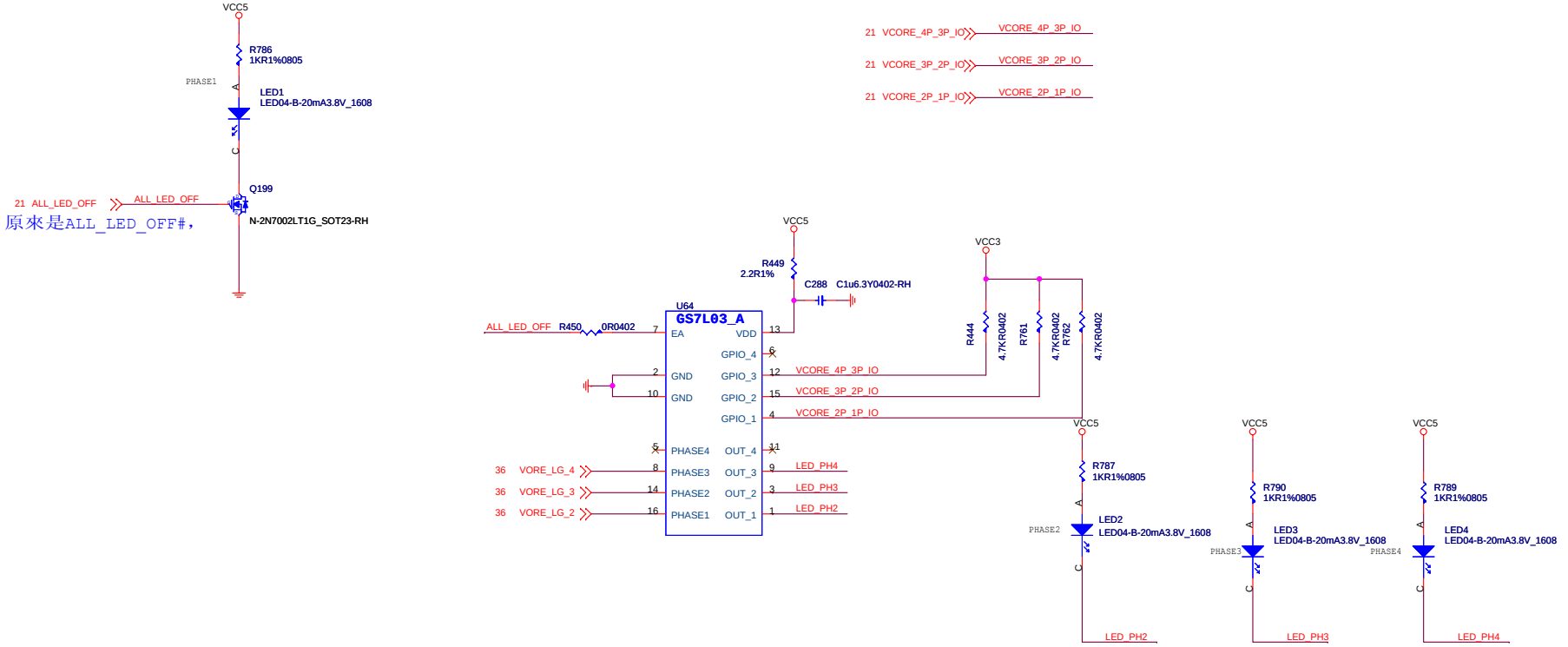
all on board LED switch



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	MS-7672	
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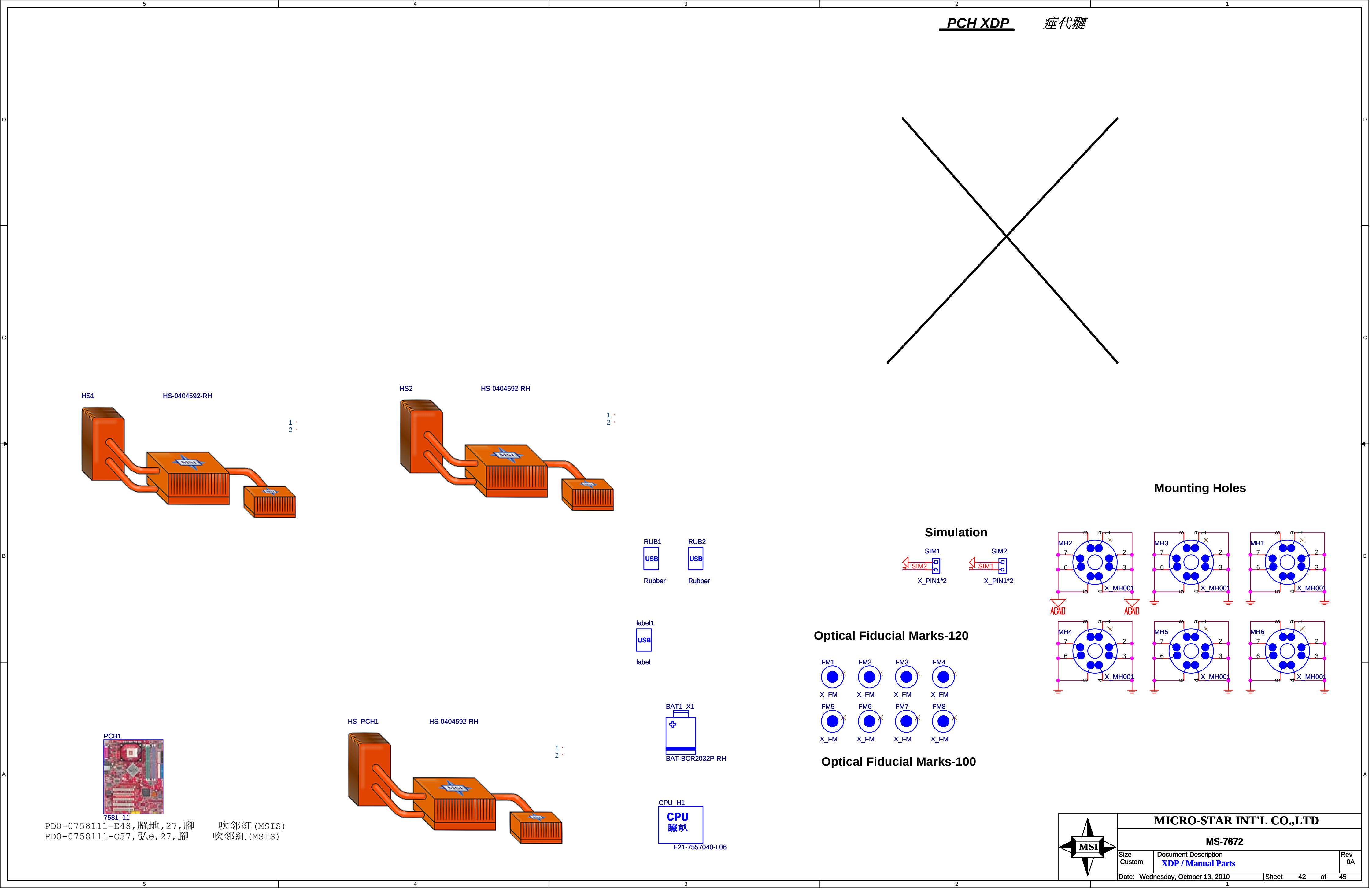

PCH XDP
瘞代虀
HS1
HS-0404592-RH
HS2
HS-0404592-RH
HS_PCH1
HS-0404592-RH
PCB1
7581_11
PD0-0758111-E48,朧地,27,腳 吹邻紅(MSIS)
PD0-0758111-G37,弘⊝,27,腳 吹邻紅(MSIS)
RUB1
RUB2
USB
Rubber
label1
label
BAT1_X1
BAT-BCR2032P-RH
CPU_H1
CPU
E21-7557040-L06
Simulation
SIM1
SIM2
X_PIN1*2
Optical Fiducial Marks-120
FM1
FM2
FM3
FM4
FM5
FM6
FM7
FM8
X_FM
Optical Fiducial Marks-100
Mounting Holes
MH1
MH2
MH3
MH4
MH5
MH6
X_MH001
AGND
MSI
MICRO-STAR INT'L CO.,LTD
MS-7672
Size Custom
Document Description
XDP / Manual Parts
Rev 0A
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