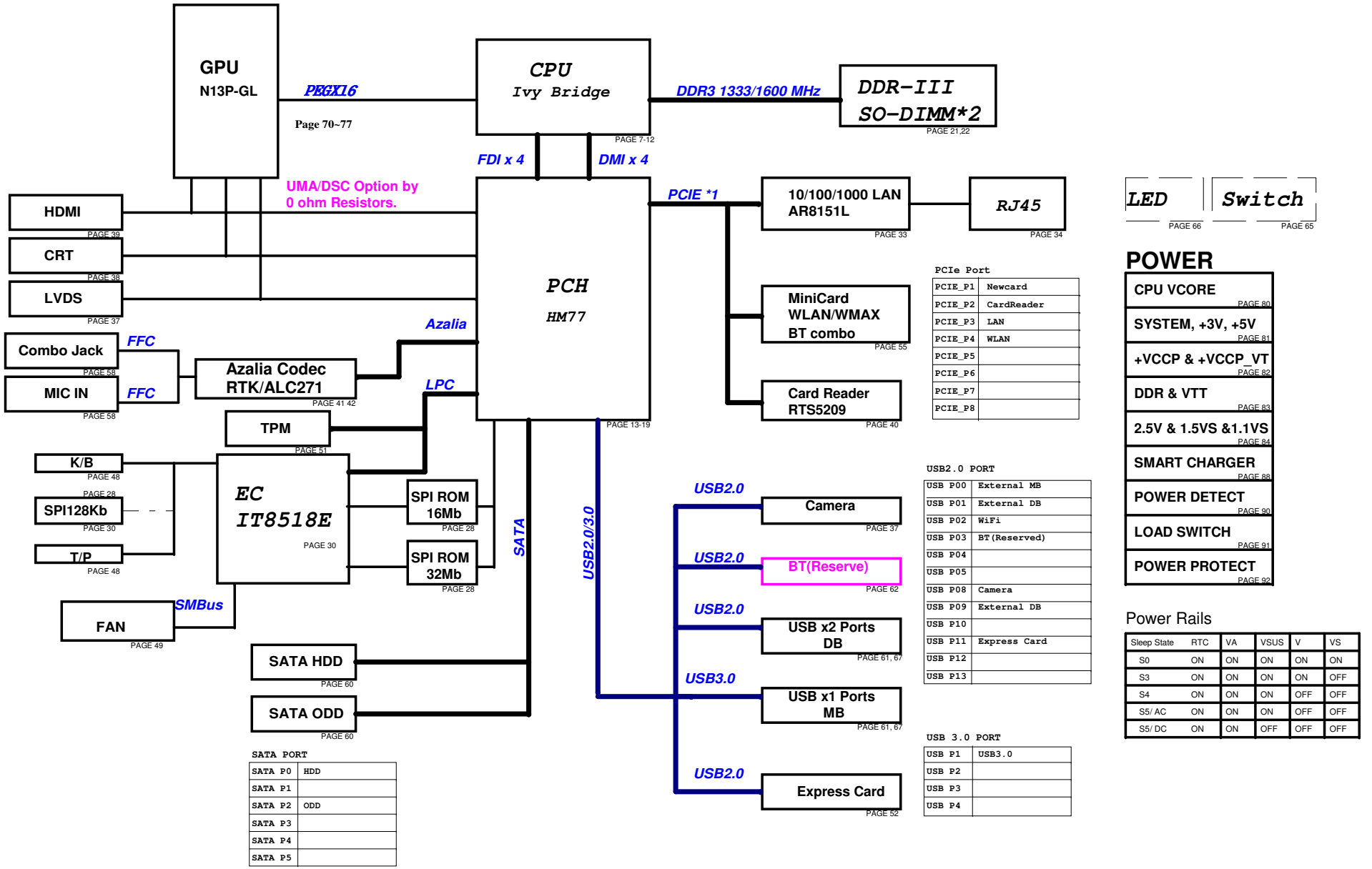
BA50 BLOCK DIAGRAM



PCIe Port

PCIE_P1	Newcard
PCIE_P2	CardReader
PCIE_P3	LAN
PCIE_P4	WLAN
PCIE_P5	
PCIE_P6	
PCIE_P7	
PCIE_P8	

USB2.0 PORT

USB P00	External MB
USB P01	External DB
USB P02	WiFi
USB P03	BT(Reserved)
USB P04	
USB P05	
USB P08	Camera
USB P09	External DB
USB P10	
USB P11	Express Card
USB P12	
USB P13	

USB 3.0 PORT

USB P1	USB3.0
USB P2	
USB P3	
USB P4	

SATA PORT

SATA P0	HDD
SATA P1	
SATA P2	ODD
SATA P3	
SATA P4	
SATA P5	

POWER

- CPU VCORE — PAGE 80
- SYSTEM, +3V, +5V — PAGE 81
- +VCCP & +VCCP_VT — PAGE 82
- DDR & VTT — PAGE 83
- 2.5V & 1.5VS &1.1VS — PAGE 84
- SMART CHARGER — PAGE 88
- POWER DETECT — PAGE 90
- LOAD SWITCH — PAGE 91
- POWER PROTECT — PAGE 92

Power Rails

Sleep State	RTC	VA	VSUS	V	VS
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4	ON	ON	ON	OFF	OFF
S5/ AC	ON	ON	ON	OFF	OFF
S5/ DC	ON	ON	OFF	OFF	OFF

PEGATRON Title : BLOCK DIAGRAM

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

Date: Friday, May 18, 2012 Sheet 1 of 77

BOM optional	Remark
N/A	For 上件
/ABCT	For ABCT，上件
/niAMT	For no iAMT，上件
/HOME	For 上件(EMI)
/HR	For Huron River，上件
share_rom	上件
non_share	不上件
/usb30	不上件
/USB20	上件
Gsensor	不上件
/HDMI	For HDMI用,上件
/TP1_BT	For power control，不上件
/TP1_CR	For power control，不上件
/TP1_CAMERA	For power control，不上件
/TP1_WLAN	For power control，不上件
/TP1_AUD	For power control，不上件
/Zero_ODD	ODD ZERO POWER，上件
/non_Zero_ODD	ODD ZERO POWER，不上件
@	For 不上件
/BT270	不上件
Express	不上件
/SATA+	For Sata Repeater, SR先上件
PCH_SATA	For NO Sata Repeater, SR不上件
/USBSLP	不上件
/non_USBSLP	上件
/THERM	For Palm Rest溫度，不上件
/UMA	依key part list而決定
/DGPU	依key part list而決定

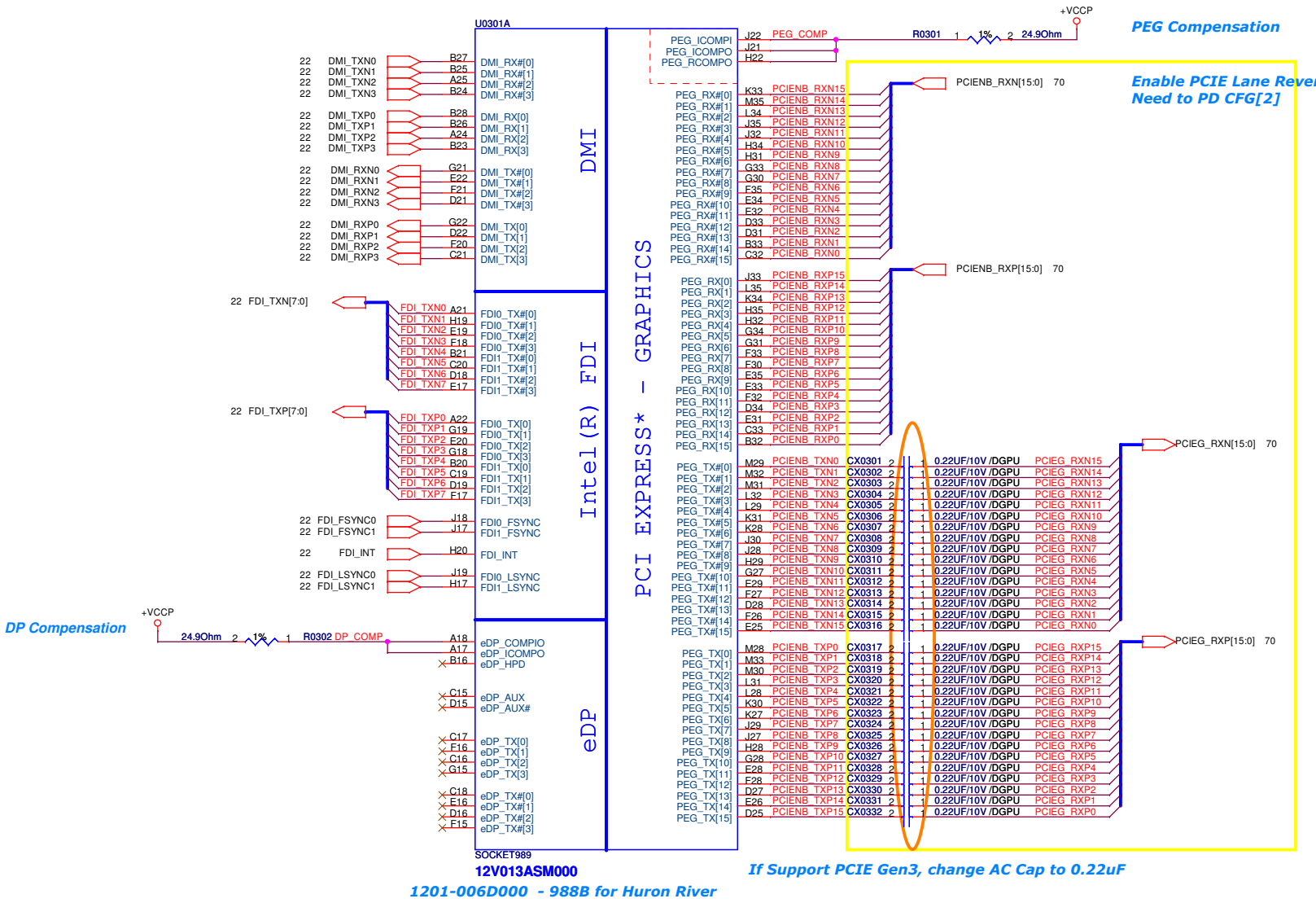
PEGATRON Title : System Setting

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
A	BA52HR/CR	1.0

Date: Friday, May 18, 2012 Sheet 2 of 94

+VCCP +VCCP 4,6,7,25,26,27,47,63,82



Title :	CPU(1)_DMI,PEG,FDI,CLK,MISC
Engineer:	Wing_Cheng
PEGATRON COMPUTER INC	
Size	Custom
Project Name	BA52HR/CR
Rev	1.0
Date:	Friday, May 18, 2012
Sheet	3 of 94

Select the termination voltage of DMI and FDI Tx/Rx (PCH Strap)
H_SNB_IVB# connected to DF_TVS via 1Kohm
DF_TVS needs PU via 2.2Kohm to +1.8VS

U0301B

MISC
SNB_IVB#
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#

CLOCKS
BCLK
BCLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#

THERMAL
DDR3 MISC
SM_DRAMRST#
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]

PWR MANAGEMENT
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#

JTAG & BPM
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]

SOCKET989

12V013ASM000

DDR3 DRAM Reset.

System Memory Impedance Compensation
Huron River platform Design Guide 436735 P.88 Table 37.
Eric Fang to Alan Chien 11/15/2010

Huron River platform Design Guide Update 440484
SM_RCOMP_1 use 26ohm 1%

+1.5V_VCCDDQ 7
+3VS 16,17,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,51,52,55,60,62,63,65,66,69,91,92
+3VSUS 22,24,27,28,30,33,37,41,55,62,81,92
+VCCP 3,6,7,25,26,27,47,63,82
+3V 24,37,51,52,62,63,65,91

PM_SYS_PWRGD is the power good for +1.5V_VCCDDQ

Reserve S3 power reduction schematic

Power good for +1.5V_VCCDDQ (delay > 100ns)

If don't support S3 power reduction
1. Unmount R0450, R0452, U0404, R0453, Q0403, C0404, R0455, R0454, C0405
2. Change R0449 to 200ohm from 1kohm, change R0409 to 130ohm from 0ohm - Design Guide 1.0 page 106

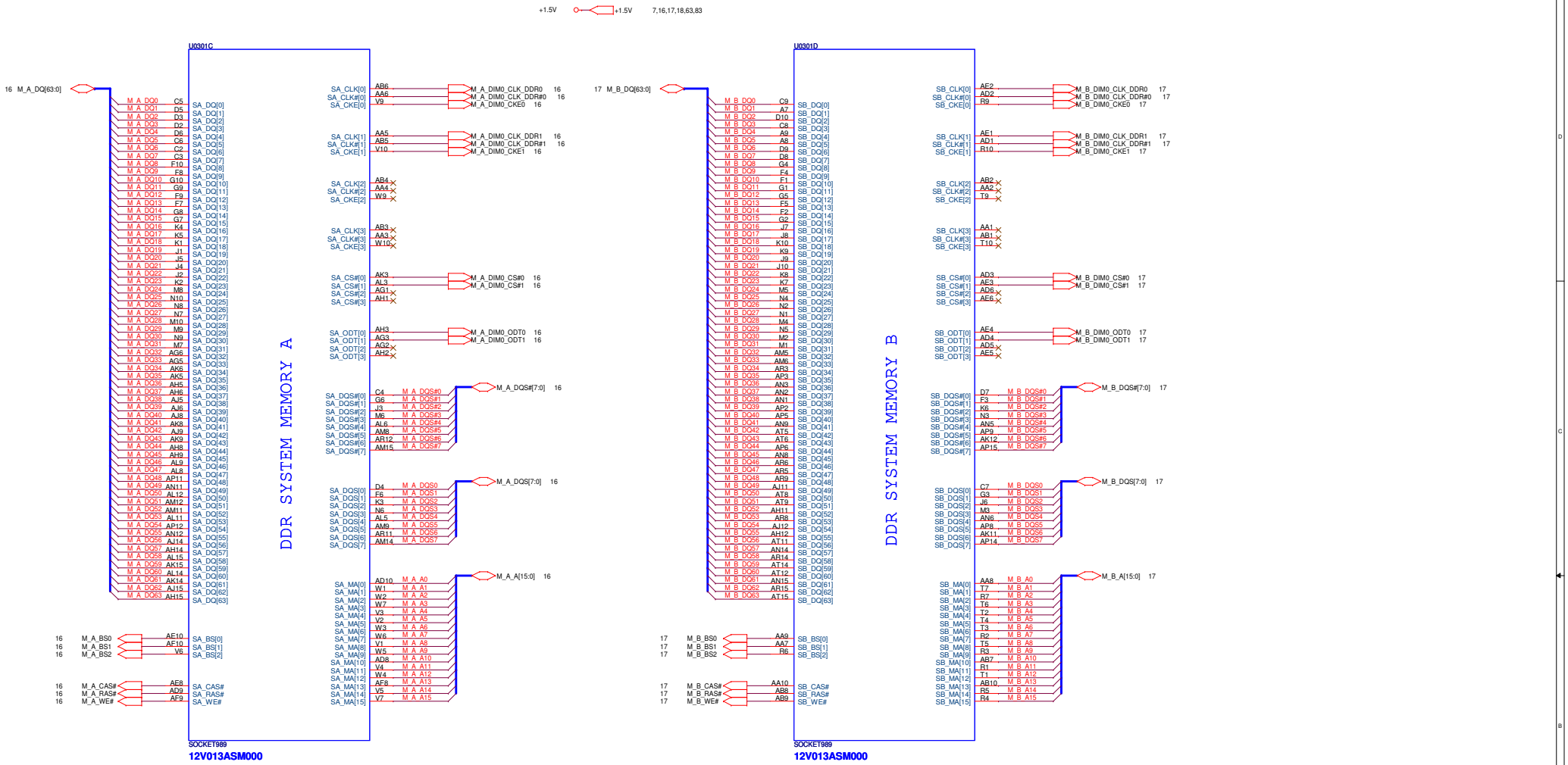
3. Unmount Q0501, C0501, R0506, R0504, R0507
4. Mount R0501, change r0508 to 0ohm from 1kohm

5 Unmount Q0701, R0703, R0705, Q0702
6. Mount R0702 and short JP0701

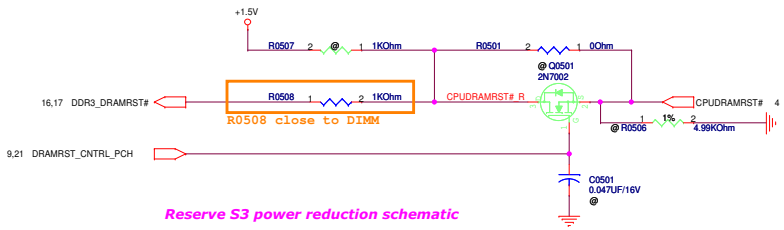
7. Unmount R2232, R2231, Q2203

R1.0 0119
Sandy Bridge:R0417 = 750 ohm (10V220000093)
Ivy Bridge:R0417 = 680 ohm (10V240000041)

PEGATRON Title : CPU(1)_DMI,PEG,FDI,CLK,MISC
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Friday, May 18, 2012 | Sheet 4 of 94



R1.0 S3 circuit:- DRAM_RST# to memory should be high during S3



Reserve S3 power reduction schematic

If don't support S3 power reduction
1. Unmount R0450, R0452, U0404, R0453, Q0403, C0404, R0455, R0454, C0405
2. Change R0449 to 200ohm from 1kohm, change R0409 to 130ohm from 0ohm - Design Guide 1.0 page 106

3. Unmount Q0501, C0501, R0506, R0504, R0507
4. Mount R0501, change r0508 to 0ohm from 1kohm

5 Unmount Q0701, R0703, R0705, Q0702
6. Mount R0702 and short JP0701

7. Unmount R2232, R2231, Q2203

PEGATRON Title : CPU(2)_DDR3
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Friday, May 18, 2012 | Sheet 5 of 94

POWER

Vcc for processor core
Voltage range: 0.3 - 1.52V

Voltage for the memory controller and shared cache defined at the motherboard VCCIO_SENSE and VSS_SENSE_VCCIO

SV-QC ICCMAX 94A
SV-DC ICCMAX 53A

ICCMAX_VCCIO 8.5A

U0301F

CORE SUPPLY
PEG AND DDR
SVID
SENSE LINES

+VCC_CORE
+VCCP

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

VIDALERT# VIDSCLK VIDSOUT

VCC_SENSE VSS_SENSE

VCCIO_SENSE VSSIO_SENSE

SOCKET989
12V013ASM000

+VCCP
+VCC_CORE

C0634 C0635 C0636 C0637 C0638 C0639 C0640 22UF/6.3V
C0645 C0646 C0647 C0648 C0649 C0650 C0651 C0652 22UF/6.3V
C0656 C0657 C0658 C0659 22UF/6.3V
C0601 C0602 C0604 C0605 C0622 C0607 C0627 C0609 C0610 C0611 10UF/25V
C0612 C0613 C0615 C0616 C0617 C0618 C0619 C0620 C0621 C0606 22UF/6.3V
C0614 C0626 C0608 C0628 C0629 C0630 22UF/6.3V

R0603 75Ohm 1%
R0605 54.9Ohm 1%
R0607 130Ohm 1%
R0608 130Ohm 1%
R0602 43Ohm
SP0604 SP0605
R0402 R0402

Close to CPU
Close to VR
Close to CPU
Close to VR

H_CPU_SVIDALRT#
VR_SVID_ALERT# 80
VR_SVID_CLK 80
VR_SVID_DATA 80
VCC_SENSE_R
VSS_SENSE_R
VCCSENSE 80
VSSSENSE 80
VCCP_SENSE 82
VSSP_SENSE 82

+VCCP +VCCP 3,4,7,25,26,27,47,63,82
+VCC_CORE +VCC_CORE 63,80

HR_Decoupling guide from Intel (POWER + EE)
+VCCP 22uF * 19pcs (7 nostuff)
330uF * 3pcs

EIH31/30 (EE)
+VCCP 10uF * 19pcs (2pcs no stuff)
22uF* 10 pcs (total no stuff)
330 uF *1pcs Power support

CR_Decoupling guide from Intel (POWER + EE)
+VCCP 22uF * 19pcs (7 nostuff)
330uF * 3pcs

Decoupling guide for Everest (EE)
+VCCP 22uF * 19pcs (7 no stuff)
330uF * 1pcs (1 no stuff)=>JE31HR/CR power support

HR_Decoupling guide from Intel (POWER + EE)
+VCC_CORE 22uF * 16pcs
10uF * 10pcs
470uF * 4pcs

EIH31/30
+VCC_CORE 22uF * 14pcs(6pcs unmount)
10uF * 16pcs (4pcs unmount)
470uF * 2pcs (Power support)

CR_Decoupling guide from Intel (POWER + EE)
+VCC_CORE 22uF * 16pcs
10uF * 10pcs
470uF * 4pcs

Decoupling guide for Everest (EE)
+VCC_CORE 22uF * 16pcs (8 nostuff)
10uF * 10pcs (3 nostuff)
470uF * 1pcs=>JE31HR/CR power support

Frank
20110602 check pull up/pull down reserve power schematic or not.

Frank
20110516 Change VCCP_SENSE to VCCIO_SENSE
and change VSSP_SENSE to VSSIO_SENSE
for meet power schematic.

Frank
20110516 Remove R0601 and R0604, because Power is already reserved

PEGATRON
PEGATRON COMPUTER INC
Title : CPU(4)_PWR
Engineer: Wing_Cheng
Size: C
Project Name: BA52HR/CR
Rev: 1.0
Date: Friday, May 18, 2012
Sheet 6 of 94

SV-QC ICCMAX_VAXG 33A
SV-DC ICCMAX_VAXG 33A

POWER

+VGFX_CORE

Graphics core voltage
Voltage range: 0 - 1.52V

C0703 22UF/6.3V /UMA
C0704 22UF/6.3V /UMA
C0705 22UF/6.3V /UMA
C0706 22UF/6.3V /UMA
C0707 22UF/6.3V /UMA
C0708 22UF/6.3V /UMA
C0711 22UF/6.3V /UMA
C0712 22UF/6.3V /UMA
C0713 22UF/6.3V /UMA
C0714 22UF/6.3V /UMA
C0715 22UF/6.3V @
C0716 22UF/6.3V @
R0710 0Ohm /DGPU

U0301G

GRAPHICS: VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

SENSE LINES: VAXG_SENSE, VSSAXG_SENSE — AK35 VCCGT_SENSE_R, AK34 VSSGT_SENSE_R — SP0701, SP0702 — R0402, R0402 — VCCGT_SENSE 80, VSSGT_SENSE 80

Close to CPU

VREF: SM_VREF — AL1 +V_SM_VREF_CNT — +V_SM_REF 10mil

R0702 0Ohm
Q0701 2N7002 @
R0703 100KOhm @
+V_SM_VREF

DDR3 Reference Voltage

Reserve S3 power reduction schematic

DDR3 -1.5V RAILS: VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15

+1.5V_VCCDDQ

C0725 10UF/25V
C0724 10UF/25V
C0723 10UF/25V @
C0722 10UF/25V
C0721 10UF/25V @
C0720 10UF/25V @
CE0702 220UF/2V

PS_S3CNTRL_1.5V_R — R0705 0Ohm @ — PS_S3CNTRL_1.5V 22
C0730 470PF/50V @
SIR472DP-T1-GE3 @ Q0702
+1.5V
3MM_OPEN_5MIL JP0701

ICCMAX_VDDQ 5A

Processor I/O supply voltage for DDR3 (DC + AC specification)

HR_Decoupling guide from Intel (POWER + EE)
+VGFX_CORE 22uF * 12pcs
470uF * 2pcs

EIH31/30
+VCCP 22uF* 16 pcs (6 unmount)
330uF * 1pcs (power support)
470uF *1pcs (EIH31 Del 470uF For Layout)

CR_Decoupling guide from Intel (POWER + EE)
+VGFX_CORE 22uF * 12pcs
470uF * 2pcs

Decoupling guide for Everest (EE)
+VGFX_CORE 22uF * 12pcs (2 nostuff)
470uF * 1pcs (JE31HR/CR power support)

PLL supply voltage (DC + AC specification)

ICCMAX_VCCPLL 1.2A

+1.8VS
CE0701 100UF/6.3V
C0717 10UF/25V
C0718 1UF/6.3V
C0719 1UF/6.3V

1.8V RAIL: B6 VCCPLL1, A6 VCCPLL2, A2 VCCPLL3

SOCKET989
12V013ASM000

HR_Decoupling guide from Intel (POWER + EE)
+1.8VS 1uF * 2pcs
10uF * 1pcs
330uF * 1pcs

EIH31/30
+1.8VS 1uF * 2pcs
10uF * 1pcs
2.2uF*1pcs
4.7uF*1pcs
22uF * 1pcs (un-mount)

CR_Decoupling guide from Intel (POWER + EE)
+1.8VS 1uF * 2pcs
10uF * 1pcs
330uF * 1pcs

Decoupling guide from Everest (EE)
+1.8VS 1uF * 2pcs
10uF * 1pcs
100uF * 1pcs

ICCMAX_VCCSA 6A

Voltage for the System Agent and VCCSA_SENSE

SA RAIL: VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8

+VCCSA
C0729 10UF/25V
C0727 10UF/25V
C0726 10UF/25V @
CE0703 100UF/6.3V

MISC: VCCSA_SENSE — H23 — R0704 0Ohm @ Close to CPU — VCCSA_SENSE 85
FC_C22 VCCSA_VID1 — C22, C24 — VCCSA_SEL0 85, VCCSA_SEL1 85

+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

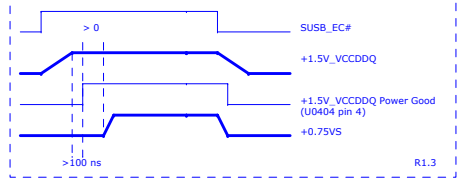
+VCCP
R0708 1KOhm @
R0709 1KOhm @
VCCSA_SEL0
VCCSA_SEL1
R0706 1KOhm
R0707 1KOhm

HR_Decoupling guide from Intel (POWER + EE)
+VCCSA 10uF * 3pcs
330uF * 1pcs

EIH31/30
+VCCSA 10uF * 4pcs (2 nostuff)
100uF * 1pcs

CR_Decoupling guide from Intel (POWER + EE)
+VCCSA 10uF * 3pcs
330uF * 1pcs

Decoupling guide for Everest (EE)
+VCCSA 10uF * 3pcs (1 nostuff)
100uF * 1pcs



HR_Decoupling guide from Intel (POWER + EE)
+VDDQ 10uF * 6pcs
330uF * 1pcs

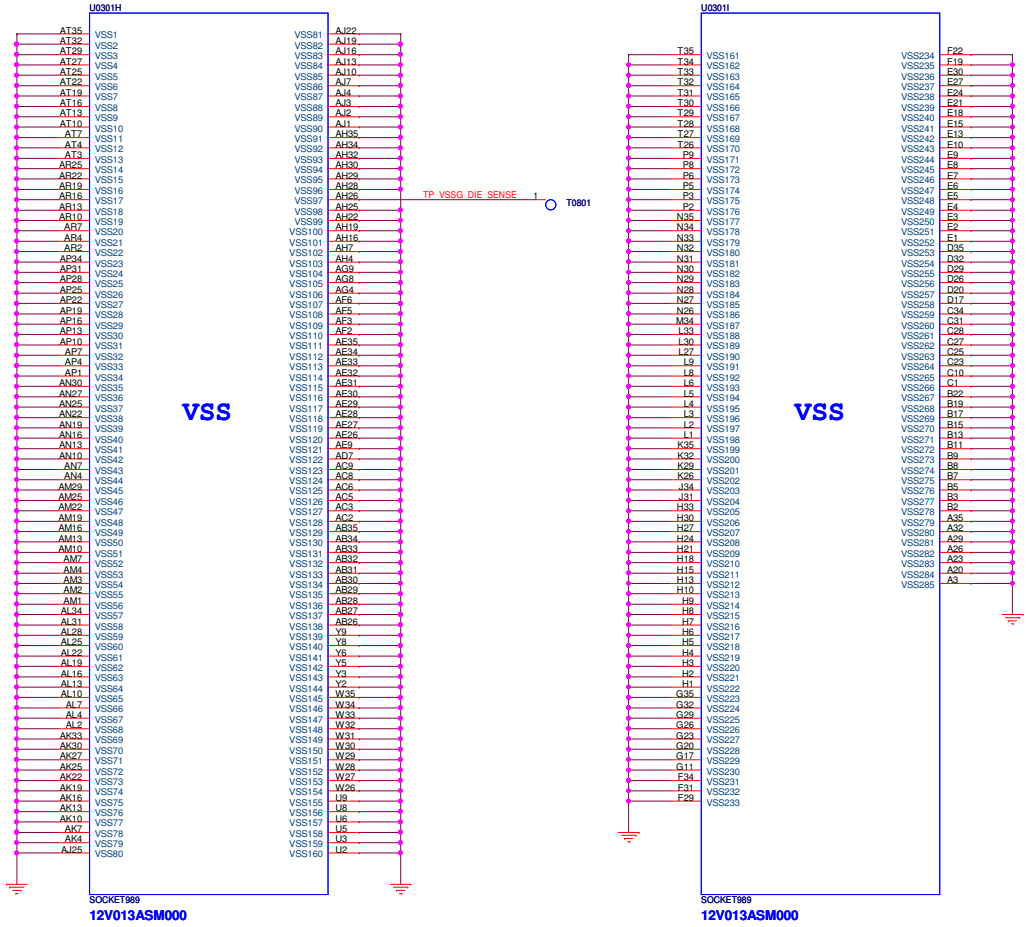
EIH31
+VDDQ 10uF * 6pcs (3 nostuff)
220uF * 1pcs

CR_Decoupling guide from Intel (POWER + EE)
+VDDQ 10uF * 6pcs
330uF * 1pcs

Decoupling guide for Everest (EE)
+VDDQ 10uF * 6pcs (3 nostuff)
220uF * 1pcs

+VCCP +VCCP 3,4,6,25,26,27,47,63,82
+1.5V +1.5V 5,16,17,18,63,83
+VCCSA +VCCSA 85
+1.8VS +1.8VS 25,26,63,84
+VGFX_CORE +VGFX_CORE 63,80
+1.5V_VCCDDQ +1.5V_VCCDDQ 4
+V_SM_VREF +V_SM_VREF 18

PEGATRON Title : CPU(4)_PWR
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Friday, May 18, 2012 | Sheet 7 of 94



PEGATRON	Title : CPU(3)_CFG,RSVD,GND		
PEGATRON COMPUTER INC	Engineer: Wing_Cheng		
Size: C	Project Name: BA52HR/CR		Rev: 1.0
Date: Friday, May 18, 2012	Sheet 8 of 94		

CFG strapping information:

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches sockect pin map definition
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection

- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

CFG[6:5]: PCI Express Port Bifurcation Straps

- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

CFG[7]: PEG DEFER TRAINING

- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training

CFG2 R0902 1% 1KOhm N/A
CFG4 R0903 1% @ 1KOhm
CFG5 R0904 1% @ 1KOhm
CFG6 R0905 1% @ 1KOhm
CFG7 R0906 1% @ 1KOhm

BA50H GPCIE Lane Number Reverse

Power schematic reserve 1.0V or not??

+VCCIO_SEL	
1	1.05V
0	1.00V

IVB VCCIO for Mobile and Desktop is changed from 1.0v to 1.05v, same as PPT VCCIO. (461017 WW23'11)

TPC26T T0918 CFG0 AK28
TPC26T T0917 CFG1 AK29
TPC26T T0916 CFG2 AL26
TPC26T T0915 CFG3 AL27
TPC26T T0914 CFG4 AK26
TPC26T T0913 CFG5 AL29
TPC26T T0912 CFG6 AL30
TPC26T T0911 CFG7 AM31
TPC26T T0910 CFG8 AM32
TPC26T T0909 CFG9 AM30
TPC26T T0908 CFG10 AM28
TPC26T T0907 CFG11 AM26
TPC26T T0906 CFG12 AN28
TPC26T T0905 CFG13 AN31
TPC26T T0904 CFG14 AN26
TPC26T T0903 CFG15 AM27
TPC26T T0902 CFG16 AK31
TPC26T T0901 CFG17 AN29

TPC26T T0953 VAXG_VAL_SENSE AJ31
TPC26T T0952 VSSAXG_VAL_SENSE AH31
TPC26T T0951 VCC_VAL_SENSE AJ33
TPC26T T0950 VSS_VAL_SENSE AH33

DDR_WR_VREF01 B4
DDR_WR_VREF02 D1

DIMM0_VREF_DQ_R Pull Down 1k ohm
DIMM1_VREF_DQ_R Pull Down 1k ohm
Design Guide 1.0 P.89 Figure 44 (436735)

R0909 1KOhm 1% @
R0910 1KOhm 1% @

TPC26T T0955 VCCIO_SEL_R

Frank
20110516 Change VCCP_SEL to VCCIO_SEL for meeting Power schematic defined

U0301E

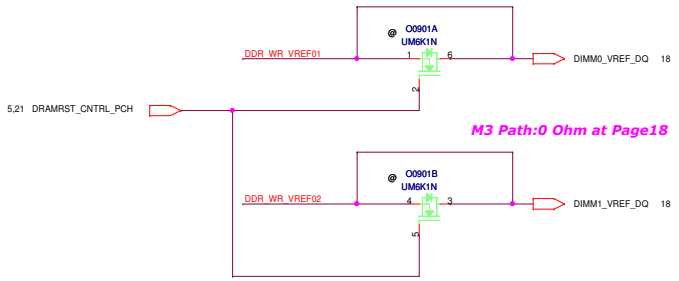
RSVD1 AJ31
RSVD2 AH31
RSVD3 AJ33
RSVD4 AH33
RSVD5 AJ26
RSVD6 B4
RSVD7 D1
RSVD8 F25
RSVD9 F24
RSVD10 F23
RSVD11 D24
RSVD12 G25
RSVD13 G24
RSVD14 F23
RSVD15 D23
RSVD16 C30
RSVD17 A31
RSVD18 B30
RSVD19 B29
RSVD20 D30
RSVD21 B31
RSVD22 A30
RSVD23 C29
RSVD24 J20
RSVD25 B18
RSVD26 A19
RSVD27 J15

RESERVED

RSVD28 L7
RSVD29 AG7
RSVD30 AE7
RSVD31 AK2
RSVD32 W8
RSVD33 AT26
RSVD34 AM33
RSVD35 AJ27
RSVD37 T8
RSVD38 J16
RSVD39 H16
RSVD40 G16
RSVD41 AR35
RSVD42 AT34
RSVD43 AT33
RSVD44 AP35
RSVD45 AR34
RSVD46 B34
RSVD47 A33
RSVD48 A34
RSVD49 B35
RSVD50 C35
RSVD51 AJ32
RSVD52 AK32
RSVD53 AH27 TP_VCCG_DIE_SENSE T0954 TPC26T
RSVD54 AN35
RSVD55 AM35
RSVD56 AT2
RSVD57 AT1
RSVD58 AR1
KEY B1

SOCKET989
12V013ASM000

PROCESSOR DRIVEN Vref PATH WAS STUFFED BY DEFAULT:



M3 Path:0 Ohm at Page18

Reserve S3 power reduction schematic

M3: Processor Generated SO-DIMM VREFDQ
– New Requirement

Sandy Bridge CPU Only: M1 Implementation
Sandy Bridge/Ivy Bridge CPU: M1 and M3 Implementation

PEGATRON Title : CPU(3)_CFG,RSVD,GND
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Friday, May 18, 2012 | Sheet 9 of 94

+VTT_PCH_ORG +VTT_PCH_ORG 22,26,27

+3VSUS +3VSUS 4,22,24,27,28,30,33,37,41,55,62,81,92

+VCCP +VCCP 3,4,6,7,25,26,27,47,63,82

+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,51,52,55,60,62,63,65,66,69,91,92

CPU XDP connector

PCH XDP connector

PEGATRON Title : NB(3)_****

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Friday, May 18, 2012 Sheet 10 of 99

+1.5V +1.5V 5,7,17,18,63,83
+1.5V_DDR3 +1.5V_DDR3 5,7,17,18,63,83
+0.75VS +0.75VS 17,63,83
+3VS +3VS 4,17,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,51,52,55,60,62,63,65,66,69,91,92
+V_VREF_CA_DIMM0 +V_VREF_CA_DIMM0 18
+V_VREF_DQ_DIMM0 +V_VREF_DQ_DIMM0 18

+1.5V
+1.5V_DDR3
+1.5V_DDR3
CE1603 22UF/6.3V @

+1.5V_DDR3
Layout Note: Place these caps near SO DIMM 0
C1609 10UF/25V @
C1610 10UF/25V @
C1611 10UF/25V @
C1612 10UF/25V @
C1613 10UF/25V
C1618 10UF/25V

+0.75VS
C1616 1UF/6.3V
C1617 1UF/6.3V
C1619 1UF/6.3V @
C1620 1UF/6.3V @

5 M_A_A[15:0]
M_A_DQ[63:0] 5

J1601A
M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12/BC#
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15

DQ0 5 M_A_DQ5
DQ1 7 M_A_DQ0
DQ2 15 M_A_DQ7
DQ3 17 M_A_DQ2
DQ4 4 M_A_DQ4
DQ5 6 M_A_DQ1
DQ6 16 M_A_DQ6
DQ7 18 M_A_DQ3
DQ8 21 M_A_DQ13
DQ9 23 M_A_DQ10
DQ10 33 M_A_DQ12
DQ11 35 M_A_DQ15
DQ12 22 M_A_DQ9
DQ13 24 M_A_DQ8
DQ14 34 M_A_DQ14
DQ15 36 M_A_DQ11
DQ16 39 M_A_DQ21
DQ17 41 M_A_DQ20
DQ18 51 M_A_DQ16
DQ19 53 M_A_DQ17
DQ20 40 M_A_DQ22
DQ21 42 M_A_DQ18
DQ22 50 M_A_DQ23
DQ23 52 M_A_DQ19
DQ24 57 M_A_DQ27
DQ25 59 M_A_DQ28
DQ26 67 M_A_DQ29
DQ27 69 M_A_DQ26
DQ28 56 M_A_DQ24
DQ29 58 M_A_DQ31
DQ30 68 M_A_DQ30
DQ31 70 M_A_DQ25
DQ32 129 M_A_DQ36
DQ33 131 M_A_DQ33
DQ34 141 M_A_DQ34
DQ35 143 M_A_DQ37
DQ36 130 M_A_DQ32
DQ37 132 M_A_DQ38
DQ38 140 M_A_DQ35
DQ39 142 M_A_DQ39
DQ40 147 M_A_DQ43
DQ41 149 M_A_DQ40
DQ42 157 M_A_DQ46
DQ43 159 M_A_DQ41
DQ44 146 M_A_DQ47
DQ45 148 M_A_DQ44
DQ46 158 M_A_DQ42
DQ47 160 M_A_DQ45
DQ48 163 M_A_DQ50
DQ49 165 M_A_DQ53
DQ50 175 M_A_DQ52
DQ51 177 M_A_DQ55
DQ52 164 M_A_DQ48
DQ53 166 M_A_DQ49
DQ54 174 M_A_DQ51
DQ55 176 M_A_DQ54
DQ56 181 M_A_DQ56
DQ57 183 M_A_DQ60
DQ58 191 M_A_DQ63
DQ59 193 M_A_DQ59
DQ60 180 M_A_DQ58
DQ61 182 M_A_DQ61
DQ62 192 M_A_DQ57
DQ63 194 M_A_DQ62

0~7
8~15
16~23
24~31
32~39
40~47
48~55
56~63

5 M_A_DIM0_CLK_DDR1 102 CK1
5 M_A_DIM0_CLK_DDR#1 104 CK1#
5 M_A_DIM0_CLK_DDR0 101 CK0
5 M_A_DIM0_CLK_DDR#0 103 CK0#
5 M_A_DIM0_CS#1 121 S1#
5 M_A_DIM0_CS#0 114 S0#
5 M_A_DIM0_ODT1 120 ODT1
5 M_A_DIM0_ODT0 116 ODT0
5 M_A_WE# 113 WE#
5 M_A_RAS# 110 RAS#
5 M_A_CAS# 115 CAS#
5 M_A_BS2 79 BA2
5 M_A_BS1 108 BA1
5 M_A_BS0 109 BA0
5 M_A_DIM0_CKE1 74 CKE1
5 M_A_DIM0_CKE0 73 CKE0
SA1 201
SA0 197

M_A_DIM0_CLK_DDR0
M_A_DIM0_CLK_DDR#0
M_A_DIM0_CLK_DDR1
C1626 10PF/50V @
R1604 150Ohm 1%
M_A_DIM0_CLK_DDR#1
PLACE CLOSE TO SODIMM

SMBus Slave Address: A0H
Follow B3:take care if can't boot or S3 issue

5 M_A_DQS[7:0]
5 M_A_DQS#[7:0]
M_A_DQS7 188 DQS7
M_A_DQS#7 186 DQS#7
M_A_DQS6 171 DQS6
M_A_DQS#6 169 DQS#6
M_A_DQS5 154 DQS5
M_A_DQS#5 152 DQS#5
M_A_DQS4 137 DQS4
M_A_DQS#4 135 DQS#4
M_A_DQS3 64 DQS3
M_A_DQS#3 62 DQS#3
M_A_DQS2 47 DQS2
M_A_DQS#2 45 DQS#2
M_A_DQS1 29 DQS1
M_A_DQS#1 27 DQS#1
M_A_DQS0 12 DQS0
M_A_DQS#0 10 DQS#0

DM should connect to GND directly
Design Guide 1.0 P.88 (436735)
187 DM7
170 DM6
153 DM5
136 DM4
63 DM3
46 DM2
28 DM1
11 DM0

17,28,52,55 SMB_CLK_S 202 SCL
17,28,52,55 SMB_DAT_S 200 SDA
RESET# 30 DDR3_DRAMRST# 5,17

DDR3_DIMM_204P
12V02GBSM000

H:9.2mm

+1.5V_DDR3
Layout Note: Place these caps near SO DIMM 0
C1605 0.1UF/16V
C1606 0.1UF/16V
C1607 0.1UF/16V
C1608 0.1UF/16V

J1601B
VDD1 75 VDD2 76
VDD3 81 VDD4 82
VDD5 87 VDD6 88
VDD7 93 VDD8 94
VDD9 99 VDD10 100
VDD11 105 VDD12 106
VDD13 111 VDD14 112
VDD15 117 VDD16 118
VDD17 123 VDD18 124

VSS1 2 VSS2 3
VSS3 8 VSS4 9
VSS5 13 VSS6 14
VSS7 19 VSS8 20
VSS9 25 VSS10 26
VSS11 31 VSS12 32
VSS13 37 VSS14 38
VSS15 43 VSS16 44
VSS17 48 VSS18 49
VSS19 54 VSS20 55
VSS21 60 VSS22 61
VSS23 65 VSS24 66
VSS25 71 VSS26 72
VSS27 127 VSS28 128
VSS29 133 VSS30 134
VSS31 138 VSS32 139
VSS33 144 VSS34 145
VSS35 150 VSS36 151
VSS37 155 VSS38 156
VSS39 161 VSS40 162
VSS41 167 VSS42 168
VSS43 172 VSS44 173
VSS45 178 VSS46 179
VSS47 184 VSS48 185
VSS49 189 VSS50 190
VSS51 195 VSS52 196

GND1 207
GND2 208
NP_NC1 205
NP_NC2 206
VTT1 203
VTT2 204
VREFCA 126
VREFDQ 1
VDDSPD 199

T1601 1 PM_EXTTS#0_DIM_A
EVENT# 198
TEST 125
NC1 77
NC2 122

+0.75VS
+3VS
C1615 0.1UF/16V
C1614 2.2UF/10V @

+V_VREF_CA_DIMM0
C1624 2.2UF/10V @
C1623 0.1UF/16V

+V_VREF_DQ_DIMM0
C1622 2.2UF/10V @
C1625 0.1UF/16V

DDR3_DIMM_204P
12V02GBSM000

PEGATRON Title : DDR3(1)_SO-DIMM0
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Friday, May 18, 2012 Sheet 16 of 94

+1.5V +1.5V 5,7,16,18,63,83
+1.5V_DDR3 +1.5V_DDR3 5,7,16,18,63,83
+0.75VS +0.75VS 16,63,83
+3VS +3VS 4,16,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,51,52,55,60,62,63,65,66,69,91,92
+V_VREF_CA_DIMM1 +V_VREF_CA_DIMM1 18
+V_VREF_DQ_DIMM1 +V_VREF_DQ_DIMM1 18

+1.5V_DDR3
CE1703 22UF/6.3V @

+1.5V_DDR3
Layout Note: Place these caps near SO DIMM 1
C1709 10UF/25V @
C1710 10UF/25V
C1711 10UF/25V @
C1712 10UF/25V
C1713 10UF/25V @
C1718 10UF/25V @

+0.75VS
C1716 1UF/6.3V
C1717 1UF/6.3V
C1719 1UF/6.3V @
C1730 1UF/6.3V @

5 M_B_A[15:0]
M_B_DQ[63:0] 5

J1701A
M_B_A0 98 A0
M_B_A1 97 A1
M_B_A2 96 A2
M_B_A3 95 A3
M_B_A4 92 A4
M_B_A5 91 A5
M_B_A6 90 A6
M_B_A7 86 A7
M_B_A8 89 A8
M_B_A9 85 A9
M_B_A10 107 A10/AP
M_B_A11 84 A11
M_B_A12 83 A12/BC#
M_B_A13 119 A13
M_B_A14 80 A14
M_B_A15 78 A15

DQ0 5 M_B_DQ0
DQ1 7 M_B_DQ5
DQ2 15 M_B_DQ3
DQ3 17 M_B_DQ1
DQ4 4 M_B_DQ6
DQ5 6 M_B_DQ4
DQ6 16 M_B_DQ2
DQ7 18 M_B_DQ7
DQ8 21 M_B_DQ12
DQ9 23 M_B_DQ13
DQ10 33 M_B_DQ15
DQ11 35 M_B_DQ14
DQ12 22 M_B_DQ9
DQ13 24 M_B_DQ8
DQ14 34 M_B_DQ11
DQ15 36 M_B_DQ10
DQ16 39 M_B_DQ21
DQ17 41 M_B_DQ20
DQ18 51 M_B_DQ23
DQ19 53 M_B_DQ18
DQ20 40 M_B_DQ16
DQ21 42 M_B_DQ17
DQ22 50 M_B_DQ19
DQ23 52 M_B_DQ22
DQ24 57 M_B_DQ26
DQ25 59 M_B_DQ30
DQ26 67 M_B_DQ31
DQ27 69 M_B_DQ27
DQ28 56 M_B_DQ28
DQ29 58 M_B_DQ24
DQ30 68 M_B_DQ25
DQ31 70 M_B_DQ29
DQ32 129 M_B_DQ37
DQ33 131 M_B_DQ33
DQ34 141 M_B_DQ35
DQ35 143 M_B_DQ34
DQ36 130 M_B_DQ38
DQ37 132 M_B_DQ39
DQ38 140 M_B_DQ36
DQ39 142 M_B_DQ32
DQ40 147 M_B_DQ44
DQ41 149 M_B_DQ41
DQ42 157 M_B_DQ46
DQ43 159 M_B_DQ47
DQ44 146 M_B_DQ40
DQ45 148 M_B_DQ45
DQ46 158 M_B_DQ42
DQ47 160 M_B_DQ43
DQ48 163 M_B_DQ50
DQ49 165 M_B_DQ52
DQ50 175 M_B_DQ51
DQ51 177 M_B_DQ49
DQ52 164 M_B_DQ53
DQ53 166 M_B_DQ48
DQ54 174 M_B_DQ55
DQ55 176 M_B_DQ54
DQ56 181 M_B_DQ57
DQ57 183 M_B_DQ56
DQ58 191 M_B_DQ59
DQ59 193 M_B_DQ62
DQ60 180 M_B_DQ60
DQ61 182 M_B_DQ58
DQ62 192 M_B_DQ63
DQ63 194 M_B_DQ61

0~7
8~15
16~23
24~31
32~39
40~47
48~55
56~63

5 M_B_DIM0_CLK_DDR1 102 CK1
5 M_B_DIM0_CLK_DDR#1 104 CK1#
5 M_B_DIM0_CLK_DDR0 101 CK0
5 M_B_DIM0_CLK_DDR#0 103 CK0#
5 M_B_DIM0_CS#1 121 S1#
5 M_B_DIM0_CS#0 114 S0#
5 M_B_DIM0_ODT1 120 ODT1
5 M_B_DIM0_ODT0 116 ODT0
5 M_B_WE# 113 WE#
5 M_B_RAS# 115 RAS#
5 M_B_CAS#
5 M_B_BS2 79 BA2
5 M_B_BS1 108 BA1
5 M_B_BS0 109 BA0
5 M_B_DIM0_CKE1 74 CKE1
5 M_B_DIM0_CKE0 73 CKE0
201 SA1
197 SA0

5 M_B_DQS[7:0]
5 M_B_DQS#[7:0]
M_B_DQS7 188 DQS7
M_B_DQS#7 186 DQS#7
M_B_DQS6 171 DQS6
M_B_DQS#6 169 DQS#6
M_B_DQS5 154 DQS5
M_B_DQS#5 152 DQS#5
M_B_DQS4 137 DQS4
M_B_DQS#4 135 DQS#4
M_B_DQS3 64 DQS3
M_B_DQS#3 62 DQS#3
M_B_DQS2 47 DQS2
M_B_DQS#2 45 DQS#2
M_B_DQS1 29 DQS1
M_B_DQS#1 27 DQS#1
M_B_DQS0 12 DQS0
M_B_DQS#0 10 DQS#0

187 DM7
170 DM6
153 DM5
136 DM4
63 DM3
46 DM2
28 DM1
11 DM0

16,28,52,55 SMB_CLK_S 202 SCL
16,28,52,55 SMB_DAT_S 200 SDA
RESET# 30 DDR3_DRAMRST# 5,16

DDR3_DIM_204P
12V02GWSM000

M_B_DIM0_CLK_DDR0 C1720 10PF/50V @ 150Ohm R1707
M_B_DIM0_CLK_DDR#0
M_B_DIM0_CLK_DDR1 C1721 10PF/50V @ 150Ohm R1708
M_B_DIM0_CLK_DDR#1
PLACE CLOSE TO SODIMM

SMBus Slave Address: A4H
+3VS R1709 SP1703 2 1 2.0KOhm 1
take care if can't boot or S3 issue

DM should connect to GND directly
Design Guide 1.0 P.88 (436735)

H:5.2mm

+1.5V_DDR3 C1705 0.1UF/16V C1706 0.1UF/16V
+1.5V_DDR3 C1707 0.1UF/16V C1708 0.1UF/16V
Layout Note: Place these caps near SO DIMM 1

J1701B
VDD1 75 VDD2 76
VDD3 81 VDD4 82
VDD5 87 VDD6 88
VDD7 93 VDD8 94
VDD9 99 VDD10 100
VDD11 105 VDD12 106
VDD13 111 VDD14 112
VDD15 117 VDD16 118
VDD17 123 VDD18 124

VSS1 2 VSS2 3
VSS3 8 VSS4 9
VSS5 13 VSS6 14
VSS7 19 VSS8 20
VSS9 25 VSS10 26
VSS11 31 VSS12 32
VSS13 37 VSS14 38
VSS15 43 VSS16 44
VSS17 48 VSS18 49
VSS19 54 VSS20 55
VSS21 60 VSS22 61
VSS23 65 VSS24 66
VSS25 71 VSS26 72
VSS27 127 VSS28 128
VSS29 133 VSS30 134
VSS31 138 VSS32 139
VSS33 144 VSS34 145
VSS35 150 VSS36 151
VSS37 155 VSS38 156
VSS39 161 VSS40 162
VSS41 167 VSS42 168
VSS43 172 VSS44 173
VSS45 178 VSS46 179
VSS47 184 VSS48 185
VSS49 189 VSS50 190
VSS51 195 VSS52 196

GND1 207
GND2 208
NP_NC1 205
NP_NC2 206
VTT1 203 +0.75VS
VTT2 204

T1701 1 PM_EXTTS#0_DIM_B
EVENT# 198
TEST 125
NC1 77
NC2 122
VREFCA 126
VREFDQ 1
VDDSPD 199 +3VS

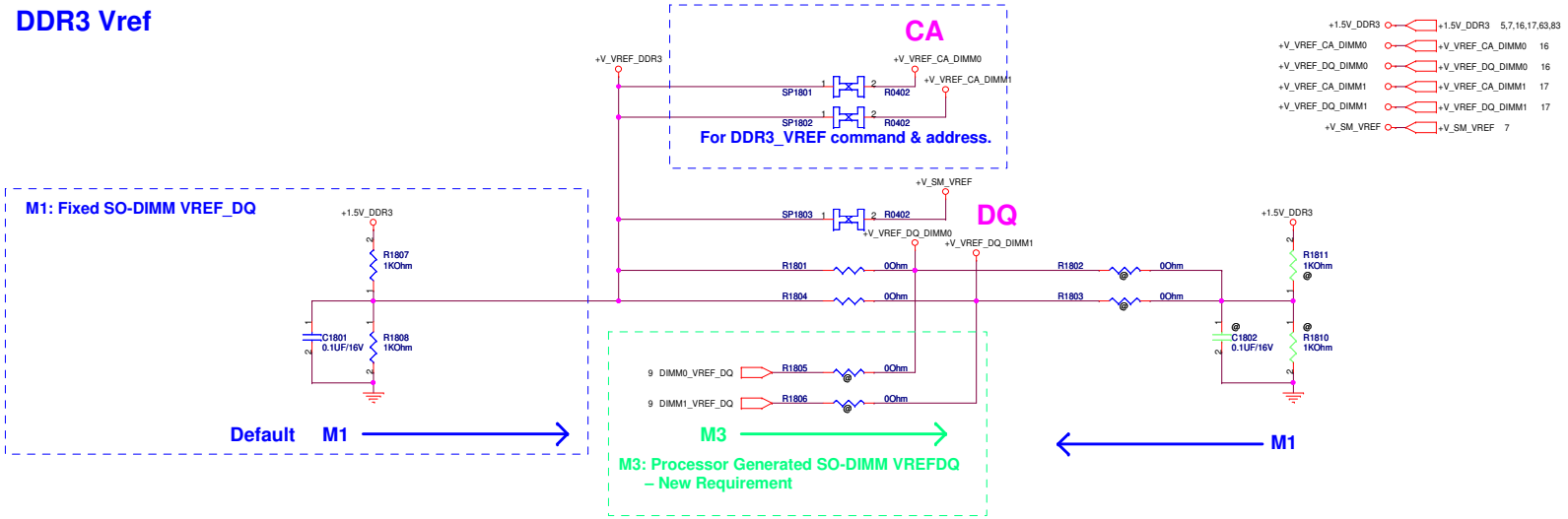
+V_VREF_CA_DIMM1
C1724 2.2UF/10V @ C1723 0.1UF/16V
+V_VREF_DQ_DIMM1
C1722 2.2UF/10V @ C1725 0.1UF/16V

C1715 0.1UF/16V C1714 2.2UF/10V @

DDR3_DIM_204P
12V02GWSM000

PEGATRON Title : DDR3(2)_SO-DIMM1
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Friday, May 18, 2012 Sheet 17 of 94

DDR3 Vref



If support M1 :(Sandy Bridge CPU Only)
1. Un mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
2. Mount R1801,R1804
==>CA and DQ are the same path

If support M1 and M3 :(Sandy Bridge/Ivy Bridge CPU)
1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
2. Un mount R1801,R1804
==> CA and DQ are separate path

Sandy Bridge CPU Only: M1 Implementation
Sandy Bridge/Ivy Bridge CPU: M1 and M3 Implementation

PEGATRON Title : DDR3(3)_CA/DQ Voltage
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Friday, May 18, 2012 | Sheet 18 of 94

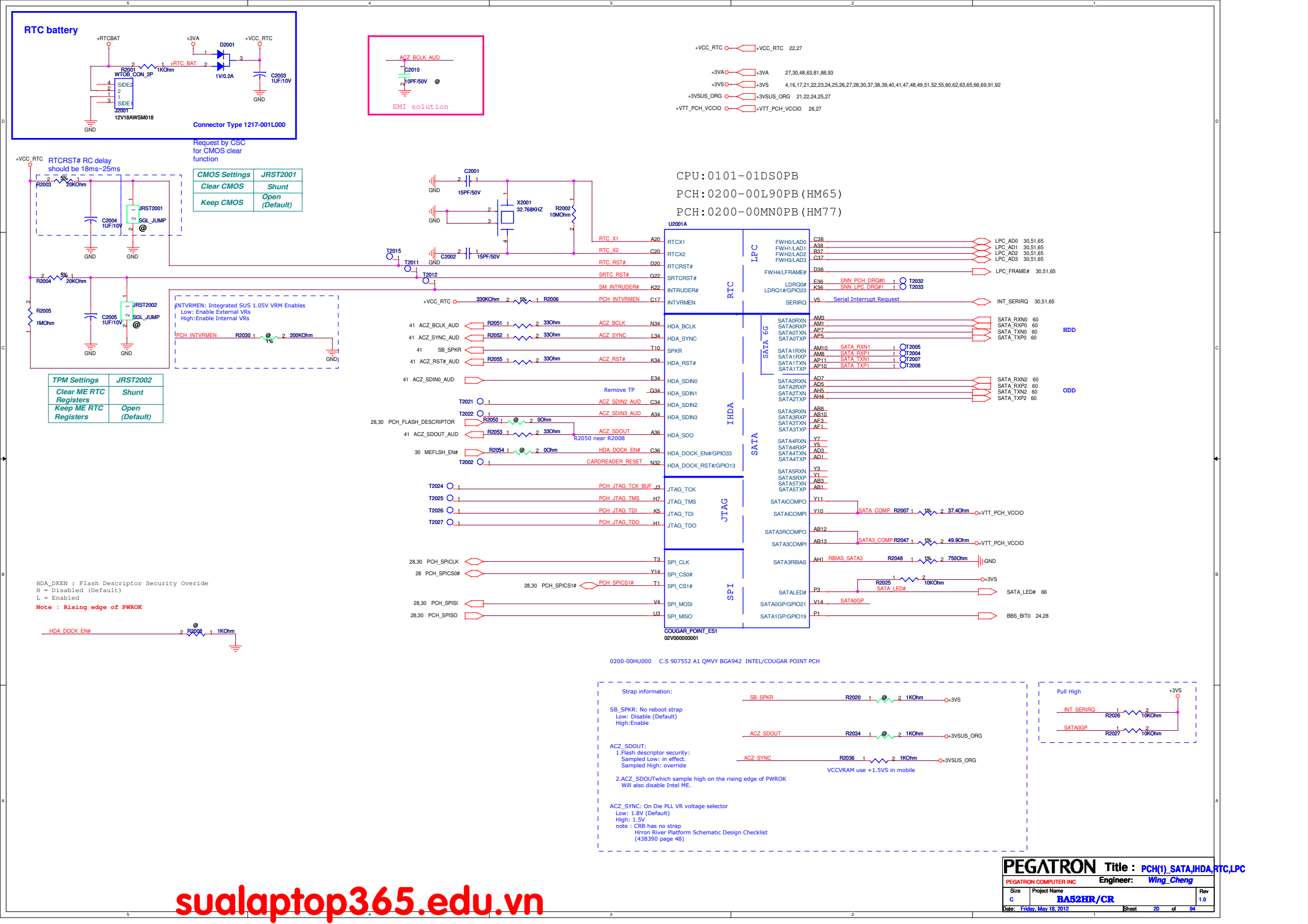
R1.4--2

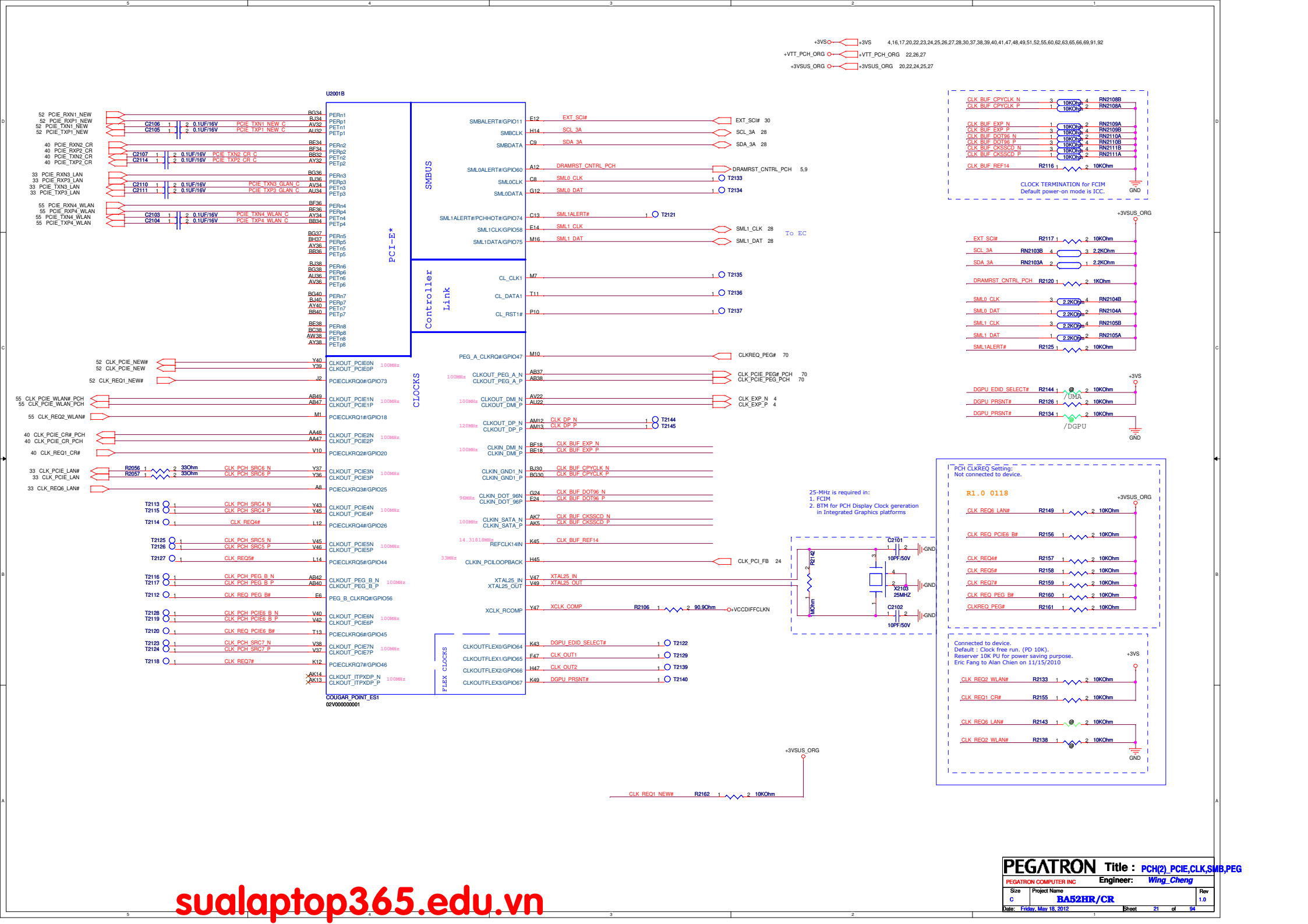
PEGATRON Title : VID Controller

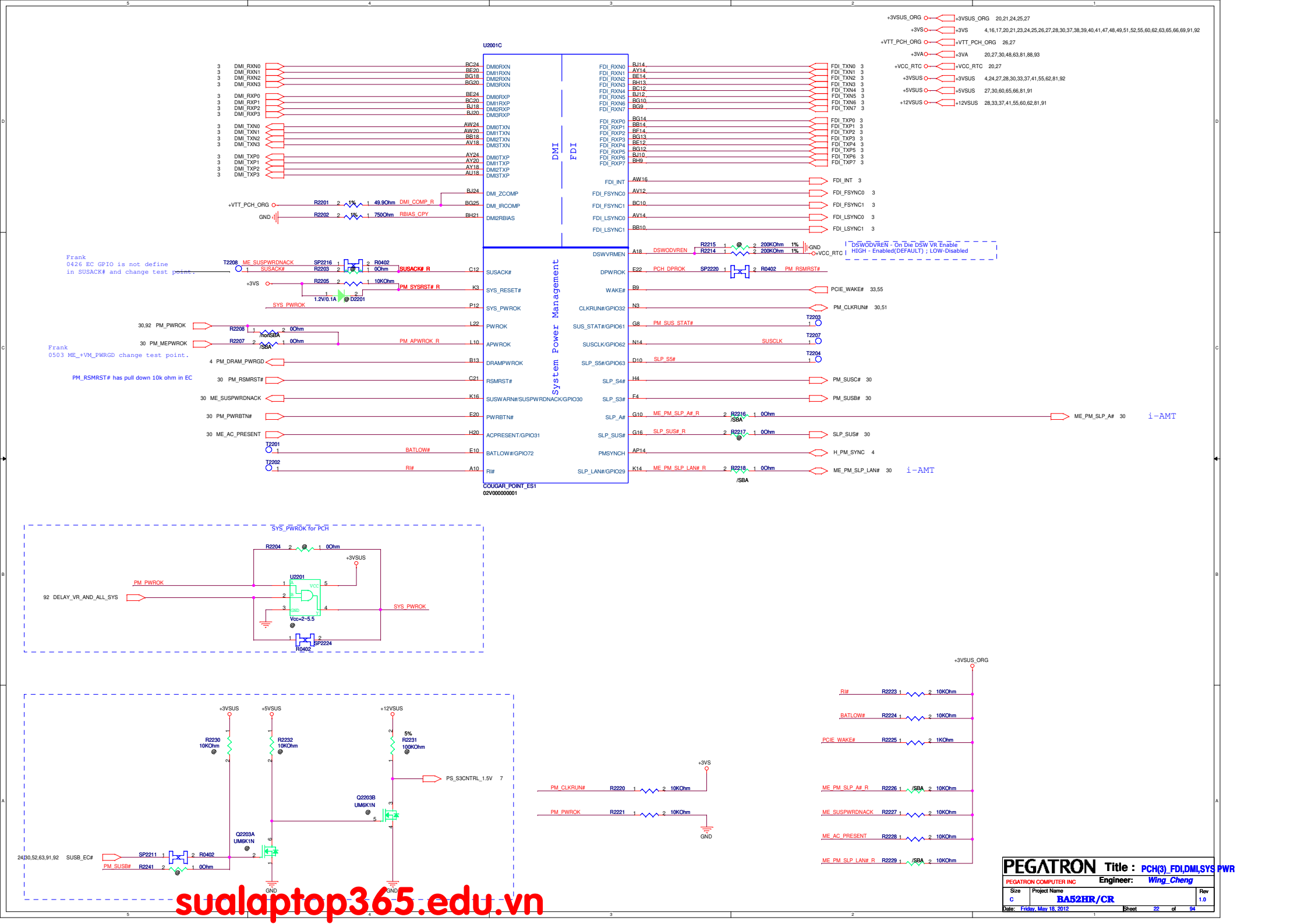
PEGATRON COMPUTER INC Engineer: Wing_Cheng

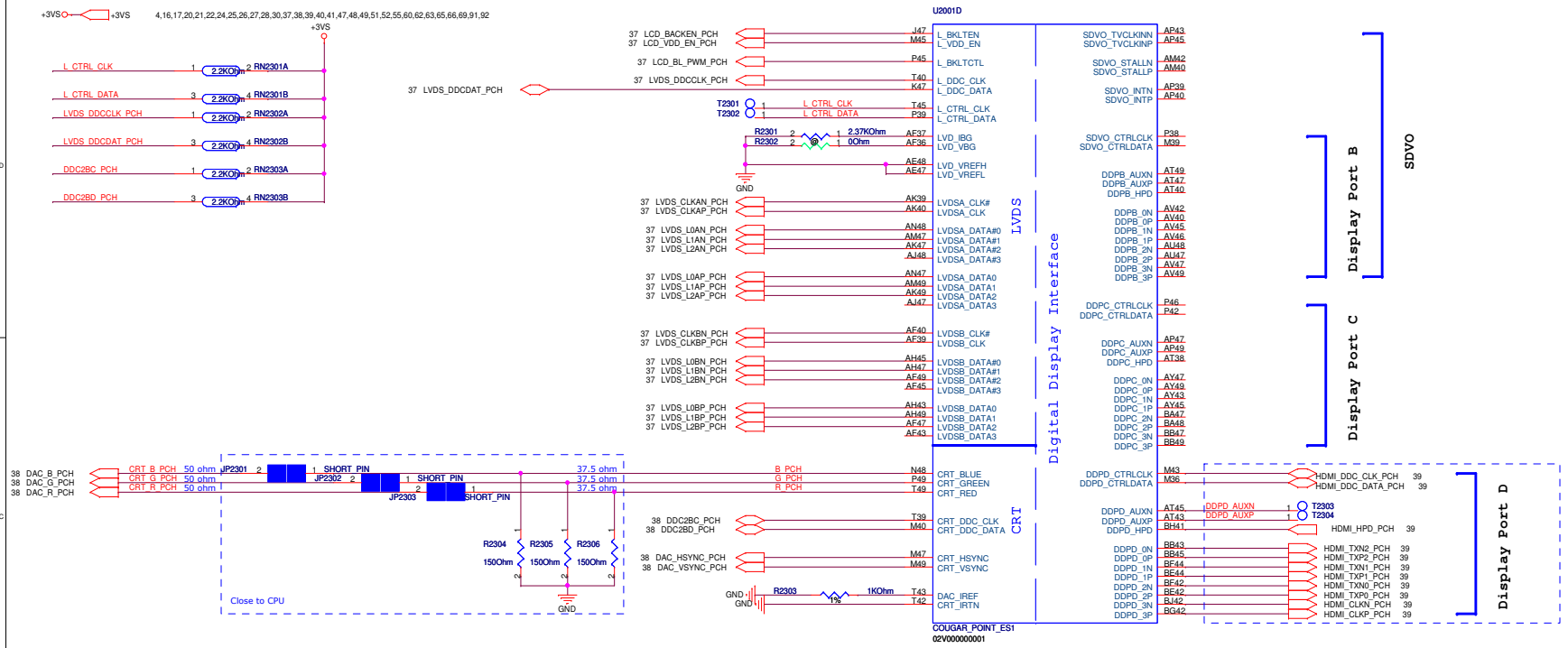
Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Friday, May 18, 2012 Sheet 19 of 94






U2001C
DMI
FDI
System Power Management
COUGAR_POINT_ES1
02V000000001
Frank
0426 EC GPIO is not define
in SUSACK# and change test point.
Frank
0503 ME_+VM_PWRGD change test point.
PM_RSMRST# has pull down 10k ohm in EC
DSWODVREN - On Die DSW VR Enable
HIGH - Enabled(DEFAULT) ; LOW-Disabled
SYS_PWROK for PCH
U2201
Vcc=2~5.5
i-AMT
i-AMT
PEGATRON
Title : PCH(3)_FDI,DMI,SYS PWR
PEGATRON COMPUTER INC
Engineer: Wing_Cheng
BA52HR/CR
Date: Friday, May 18, 2012
Sheet 22 of 94
sualaptop365.edu.vn



CRT Disable: (For discrete graphic)

1. NC:

CRT_RED,CRT_GREEN,CRT_BLUE

CRT_HSYCN,CRT_VSYNC

2. 1-kΩ ±0.5% pull-down to GND:

DAC_IREF

3. Connected to GND:

CRT_ITRN

4. Connect to +V3.3:

VCCADAC

DisPlay Port Disable: (For discrete graphic)

1. NC:

ALL

LVDS Disable: (For discrete graphic)

1. NC:

LVDSA_DATA [3:0], LVDSA_DATA# [3:0],

LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],

LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#

L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH

LVD_VREFL, LVD_IBG, LVD_VBG

2. Connected to GND:

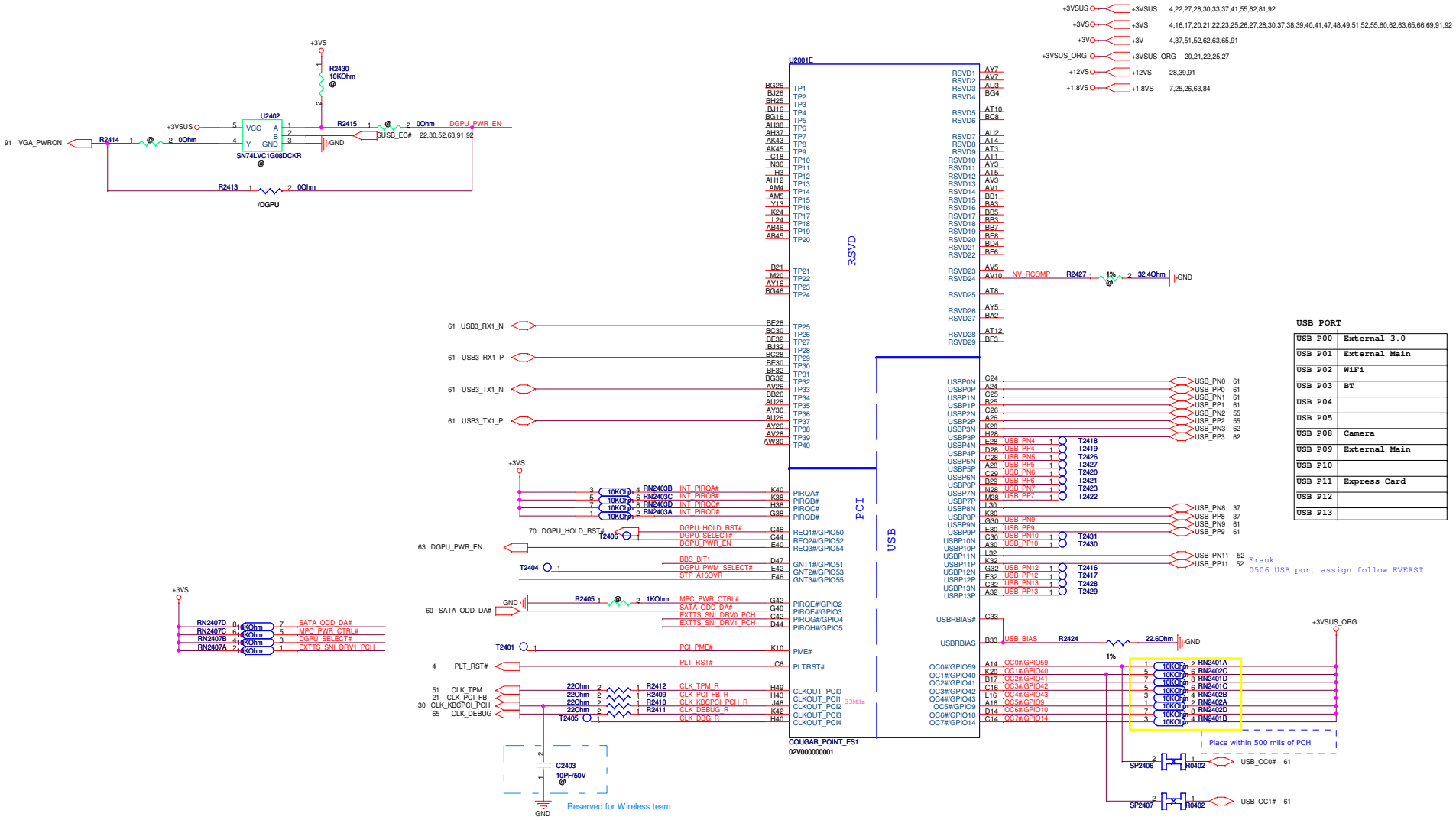
VccALVDS,VccTX_LVDS

PEGATRON Title : PCH(4)_DP,LVDS,CRT

PEGATRON COMPUTER INC Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Friday, May 18, 2012 Sheet 23 of 94



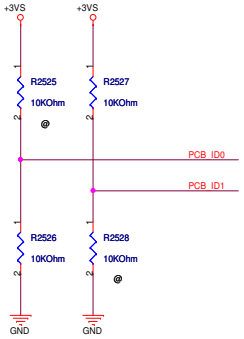
PEGATRON Title : PCH(5)_PCI,NVRAM,USB

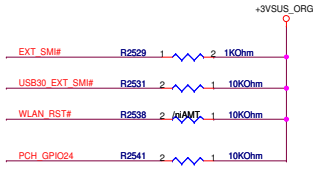
PEGATRON COMPUTER INC Engineer: Wing_Cheng

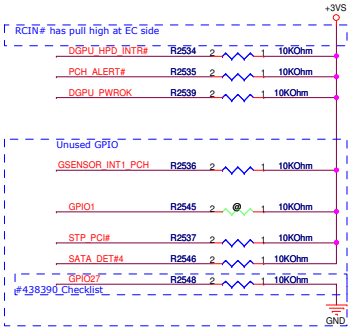
Size	Project Name	Rev
C	BA52HR/CR	1.0

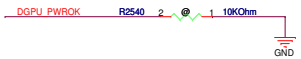
Date: Friday, May 18, 2012 Sheet 24 of 94

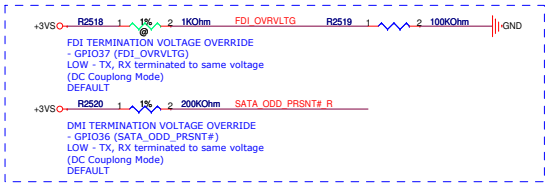
	PCB_ID1	PCB_ID0
SR	L	L
ER	L	H
PR	H	L
MP		

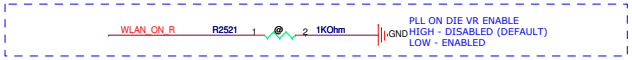










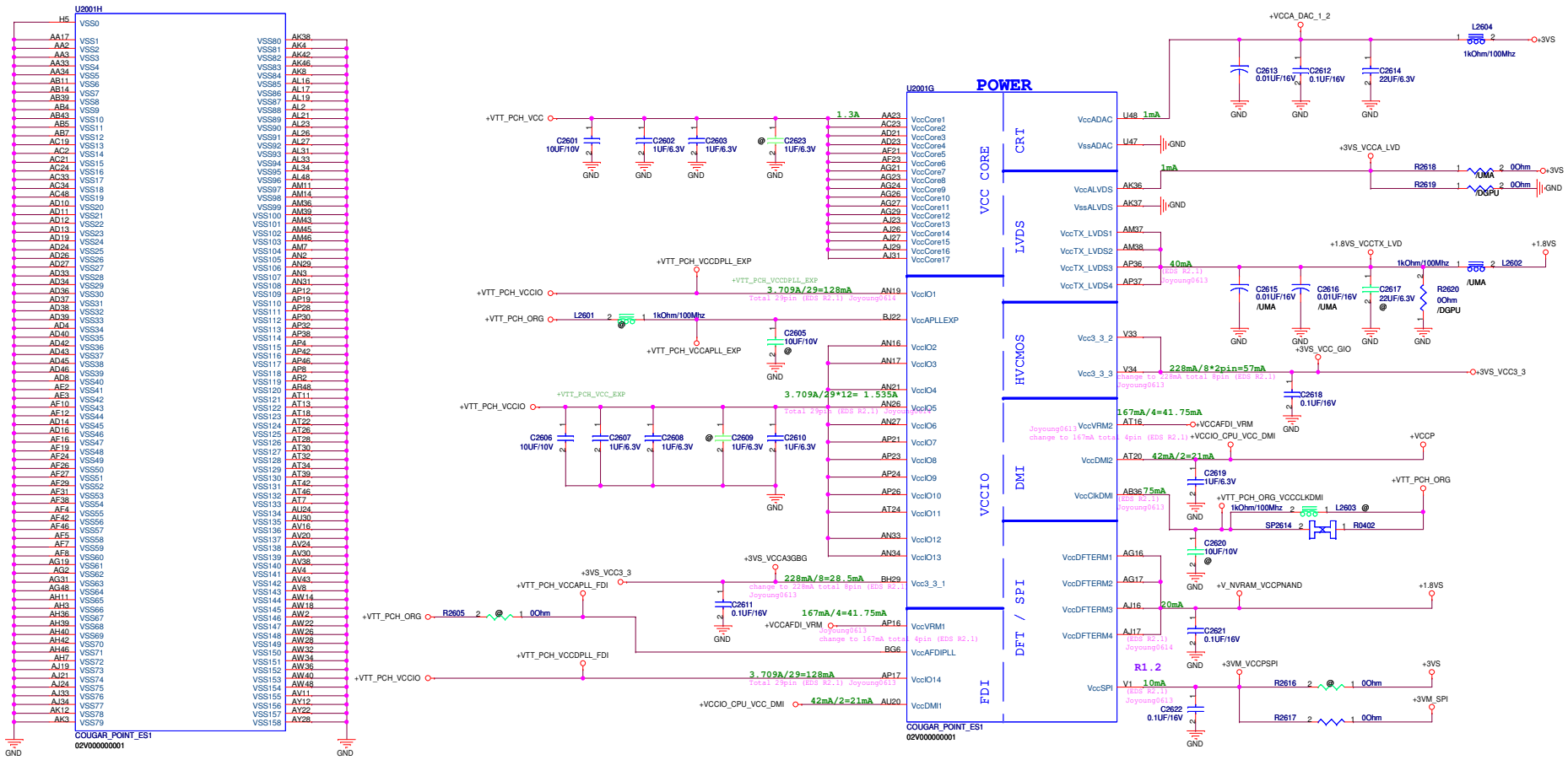


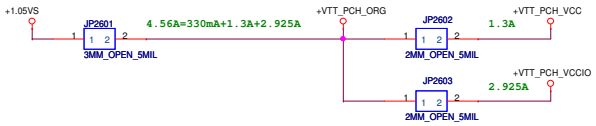
PEGATRON Title : PCH(6)_CPU,GPIO,MISC

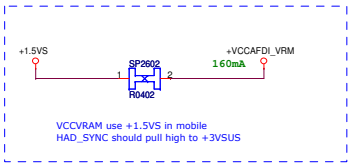
PEGATRON COMPUTER INC Engineer: Wing_Cheng

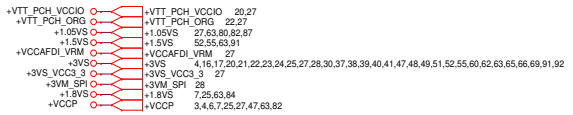
Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Friday, May 18, 2012 Sheet 25 of 94



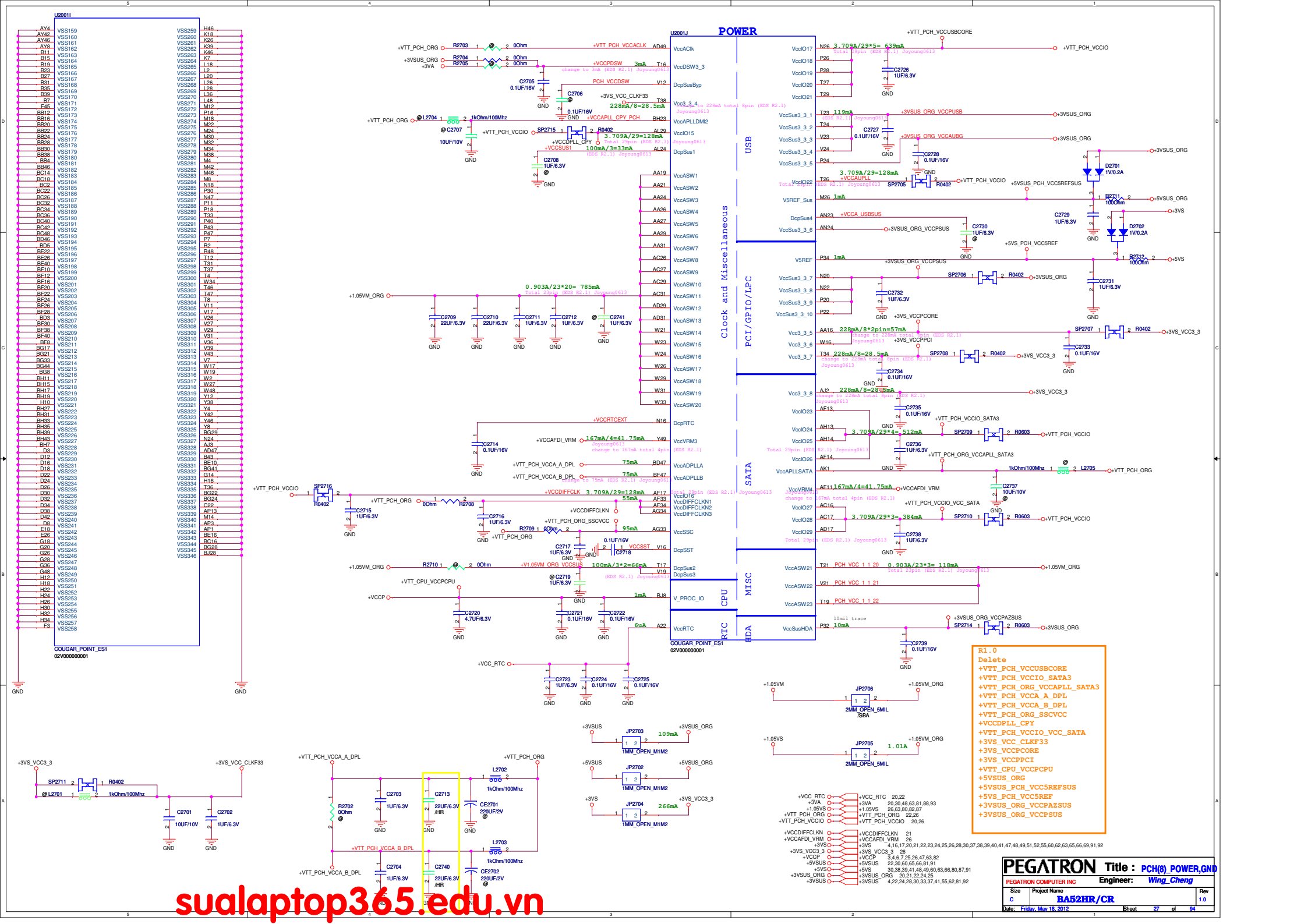






R1.0
Delete
+VTT_PCH_VCC
+VTT_PCH_VCCDPLL_EXP
+VTT_PCH_VCCAPLL_EXP
+VTT_PCH_VCCDPLL_FDI
+VTT_PCH_VCCAPLL_FDI
+3VS_VCCA3GBG
+3VS_VCC_GIO
+VCCA_DAC_1_2
+3VS_VCCA_LVDS
+3VM_VCCPSPI
+V_NVRAM_VCCPNAND
+1.8VS_VCCTX_LVD
+VCCIO_CPU_VCC_DMI
+VTT_PCH_ORG_VCCCLKDMI

PEGATRON Title : PCH(7)_POWER,GND
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Friday, May 18, 2012 | Sheet 26 of 94


POWER
U2001I
COUGAR_POINT_ES1
02V000000001
U2001J
COUGAR_POINT_ES1
02V000000001
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
MISC
RTC
HDA
R1.0
Delete
+VTT_PCH_VCCUSBCORE
+VTT_PCH_VCCIO_SATA3
+VTT_PCH_ORG_VCCAPLL_SATA3
+VTT_PCH_VCCA_A_DPL
+VTT_PCH_VCCA_B_DPL
+VTT_PCH_ORG_SSCVCC
+VCCDPLL_CPY
+VTT_PCH_VCCIO_VCC_SATA
+3VS_VCC_CLKF33
+3VS_VCCPCORE
+3VS_VCCPPCI
+VTT_CPU_VCCPCPU
+5VSUS_ORG
+5VSUS_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
+3VSUS_ORG_VCCPAZSUS
+3VSUS_ORG_VCCPSUS
PEGATRON
Title : PCH(8)_POWER,GND
PEGATRON COMPUTER INC
Engineer: Wing_Cheng
Size C
Project Name BA52HR/CR
Rev 1.0
Date: Friday, May 18, 2012
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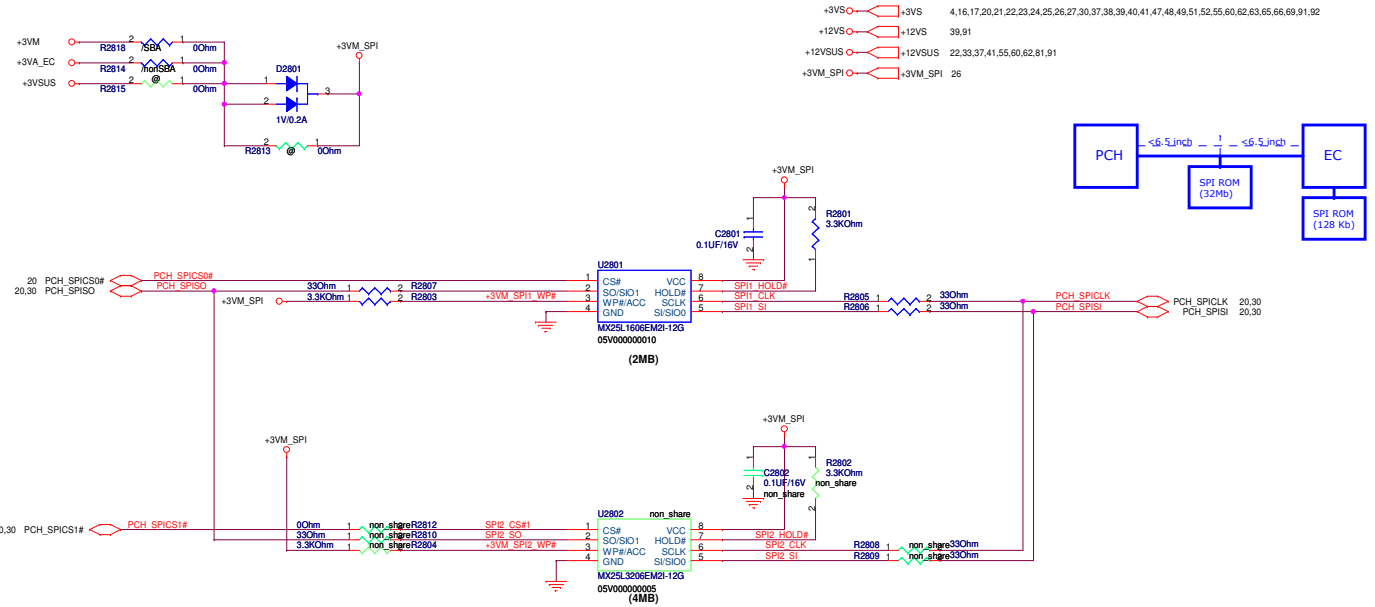
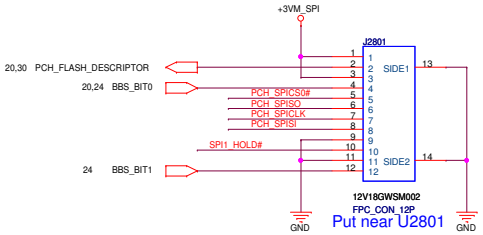
PCH SPI ROM

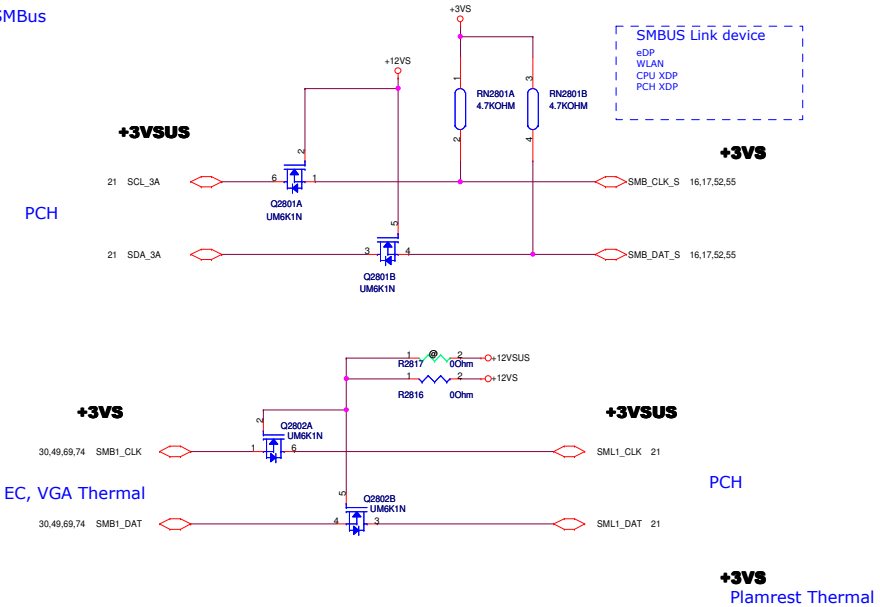
	WIN7/WIN8	SBA
U2801(2M)	○	○ (8M)
U2802(4M)		
U3003(128K)		○
U3004(4M)	○	



SPI Debug Connector



PCH SMBus



PEGATRON Title : PCH(9)_SPI,SMB
PEGATRON COMPUTER INC Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
Date: Friday, May 18, 2012 | Sheet 28 of 94

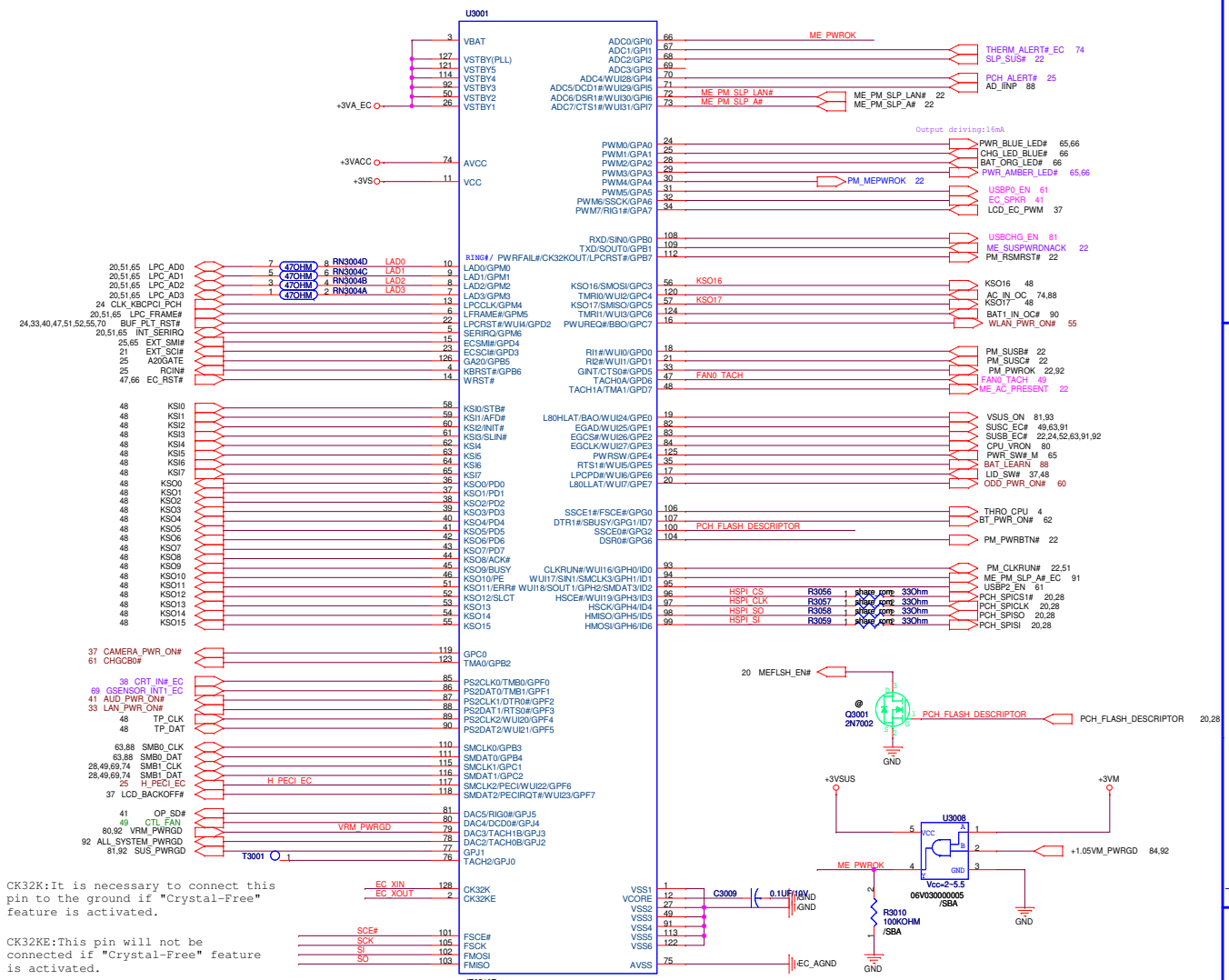
PEGATRON Title : CLK_ICS9LRS3197

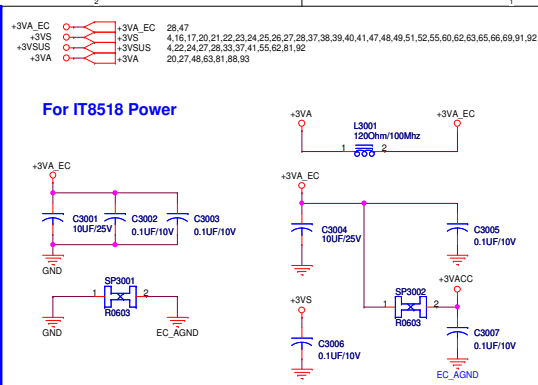
PEGATRON COMPUTER INC Engineer: Wing_Cheng

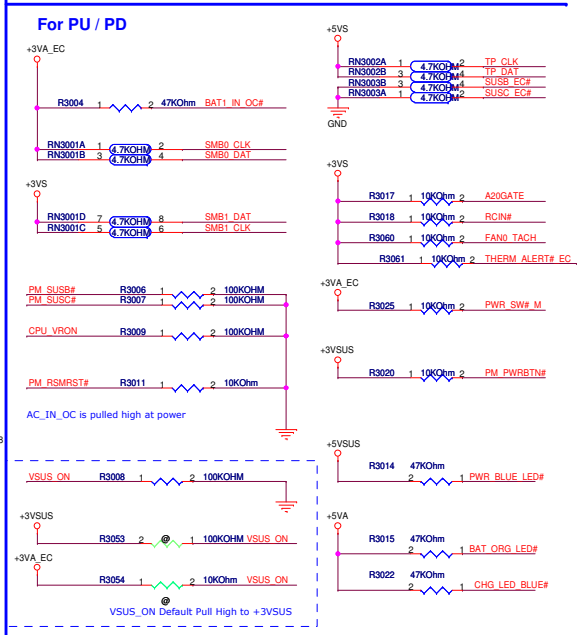
Size	Project Name	Rev
Custom	BA52HR/CR	1.0

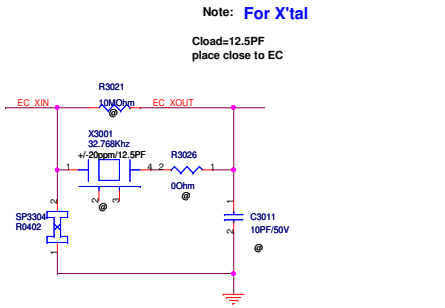
Date: Friday, May 18, 2012 Sheet 29 of 94

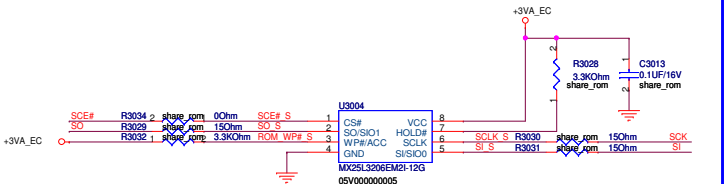
EC PN:0638-0022000

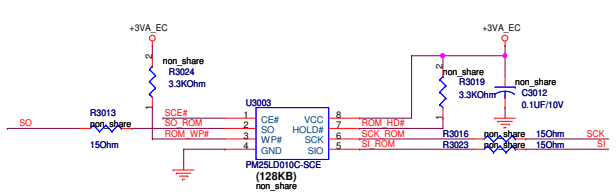












PEGATRON Title : ITE8518E

BU2/RD3 Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

Date: Friday, May 18, 2012 Sheet 30 of 99

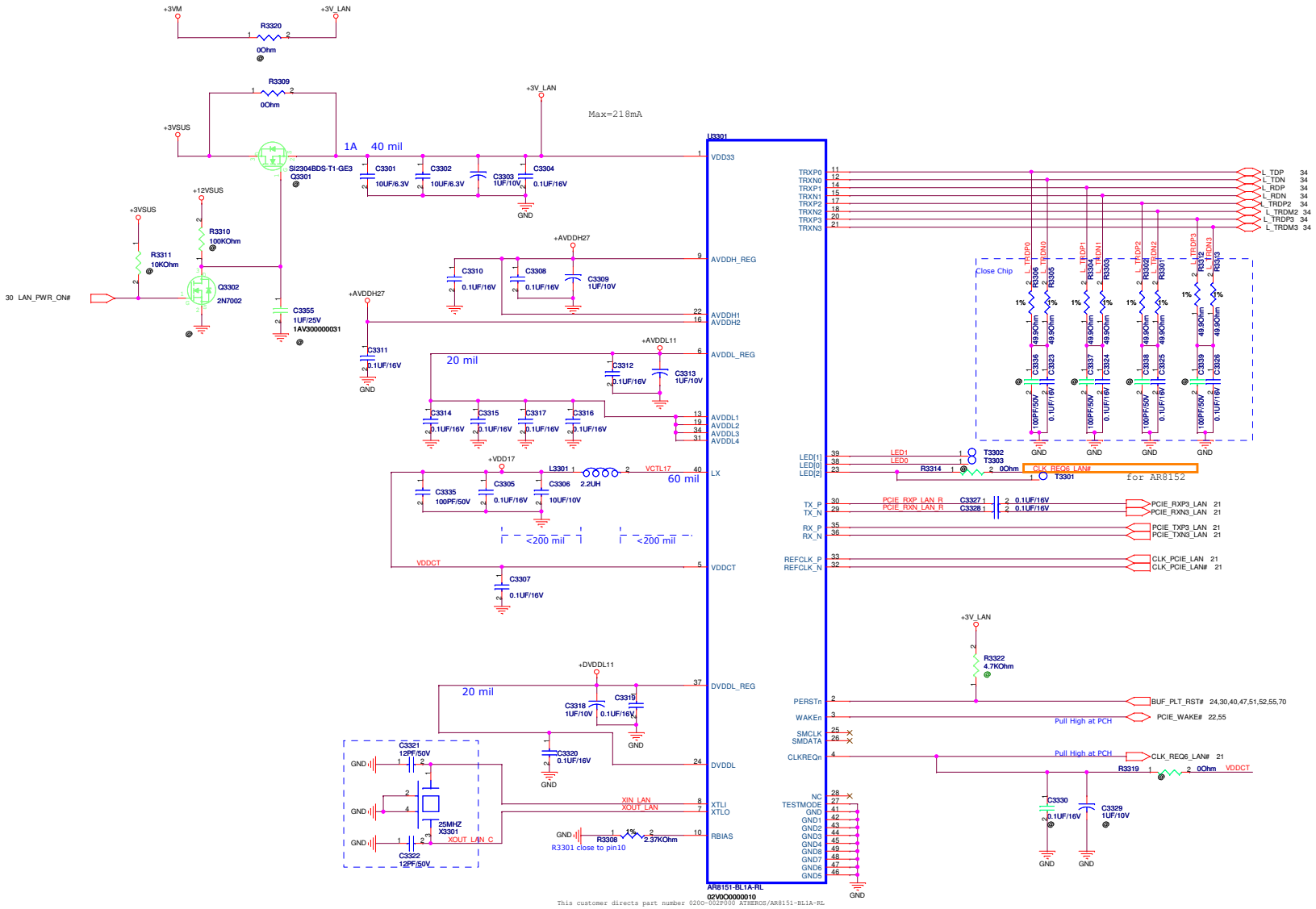
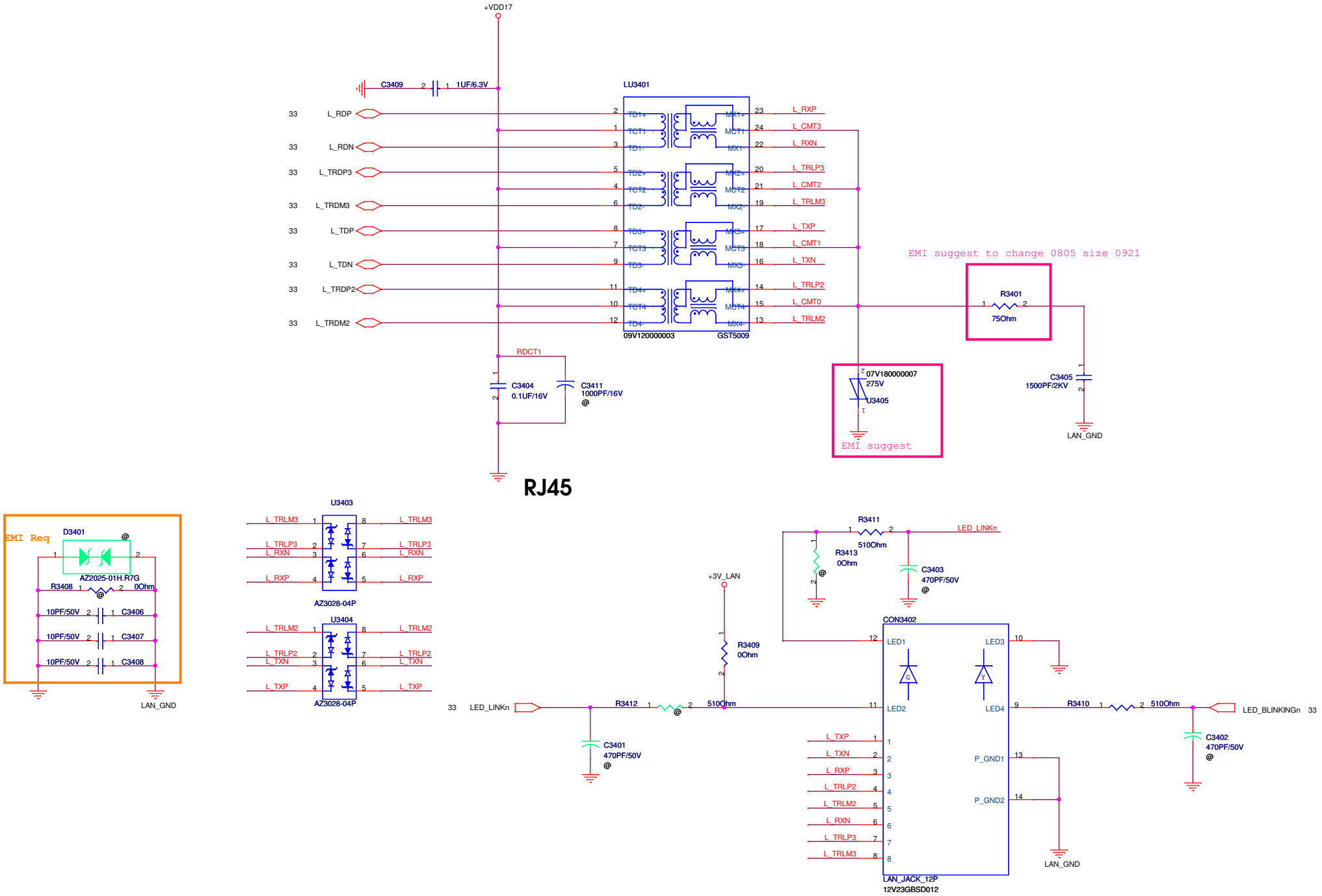


Table 2-6. **LED Link Table**

LED[0] LED_ACT	LED[1] LED_LINK	LED[2] LED_LINK_1000	Selected Speed	Link Status
High	High	High	Any Speed	Link Down
Blink	High	High	10 Mbps; Half-Duplex	Link Up
Blink	Low	High	10 Mbps; Full-Duplex	Link Up
Blink	Low	High	100 Mbps; Half-Duplex	Link Up
Blink	Low	High	100 Mbps; Full-Duplex	Link Up
Blink	Low	Low	Auto, 1000 Mbps, Full-Duplex	Link Up

AR8152-BL1A(SWR mode)	Stuff L3301,C3306,C3305,C3330; Remove C3335,C3330,R3318,R3319
AR8152-BL1A(LDO mode)	Stuff C3329,C3330,R3319; Remove L3301,C3306,C3305,C3335;R3318
AR8151-BL1A	Stuff L3301,C3306,C3305,C3335;R3318; Remove C3330,C3329,R3319

PEGATRON Title : LAN_AR8151L
BG1\HW3 Engineer: Nike_Liu
Size: Custom | Project Name: BA50HR/CR | Rev: 1.0
Date: Friday, May 18, 2012 | Sheet 33 of 99



PEGATRON Title : RJ45/ RJ11

BG1\HW3 Engineer: Nike_Liu

Size	Project Name	Rev
Custom	BA50HR/CR	1.0

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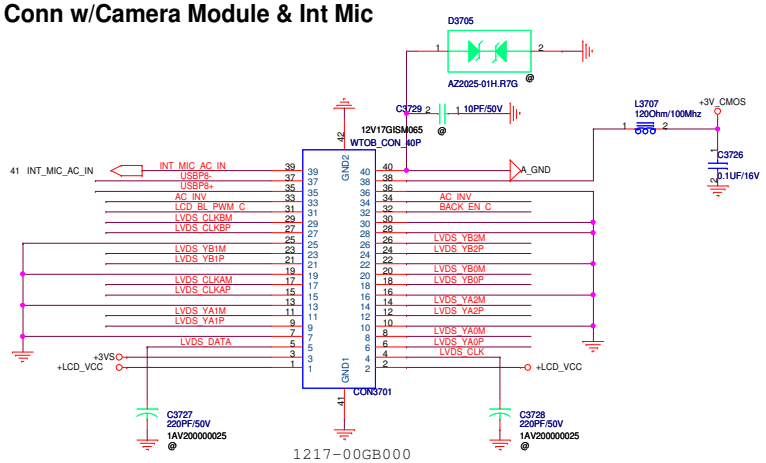
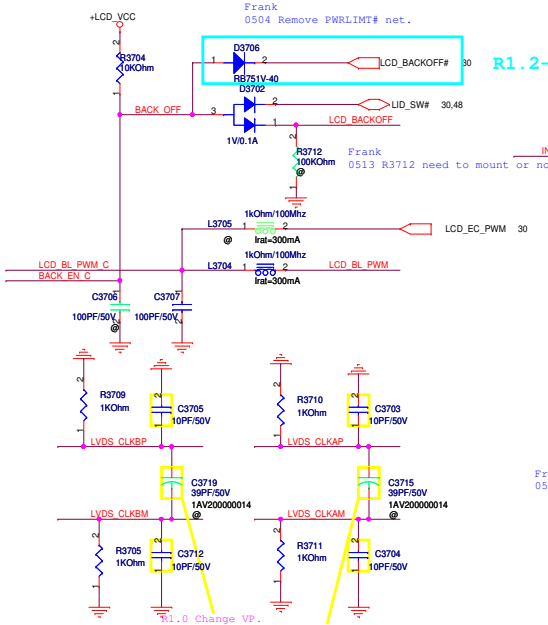
LVDS Conn w/Camera Module & Int Mic

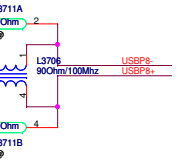


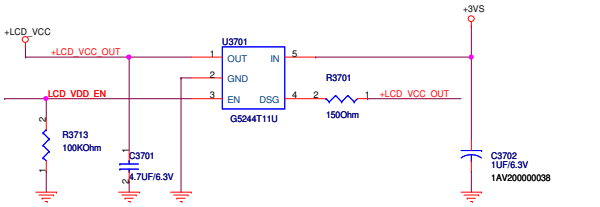
1217-00GB000

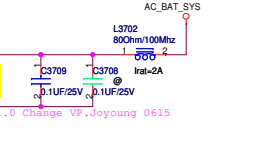
Modify LVDS Pin definition

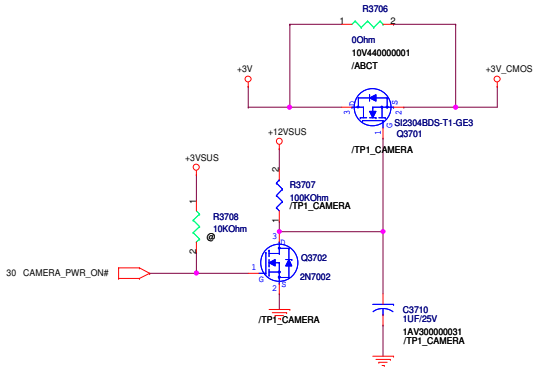
0125-11 SR-43

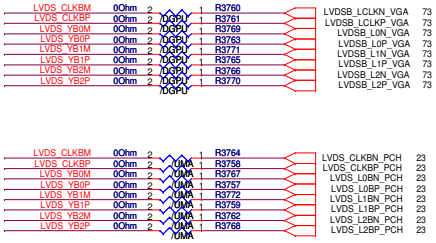


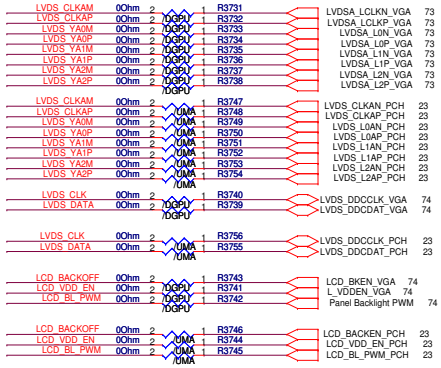












PEGATRON Title : LVDS CONN

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

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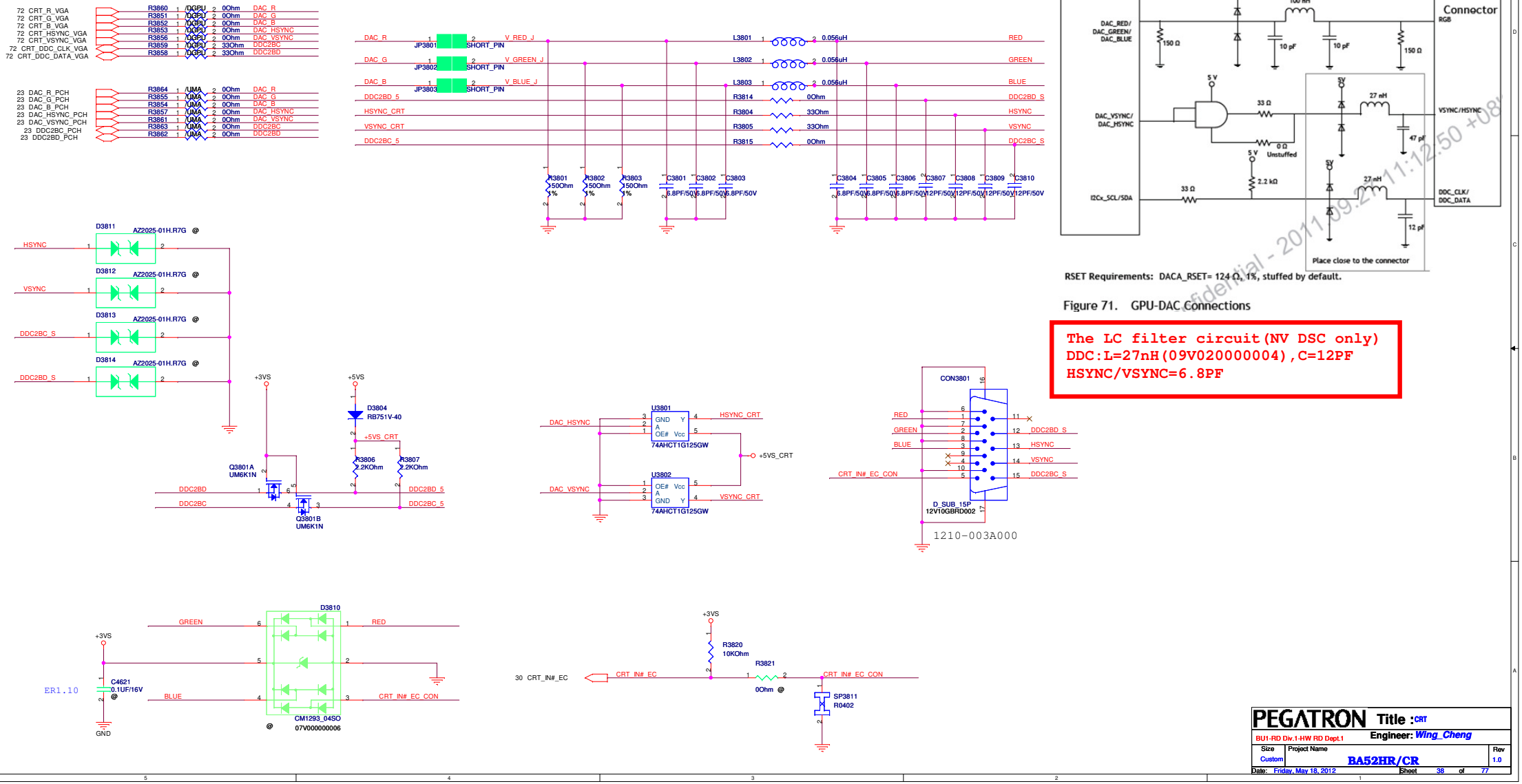
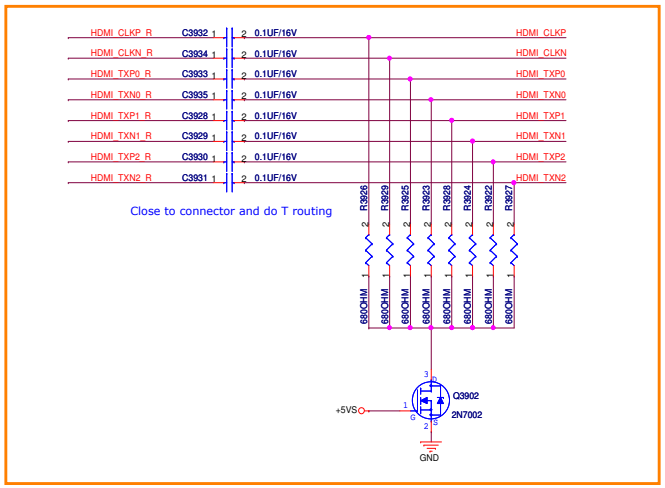
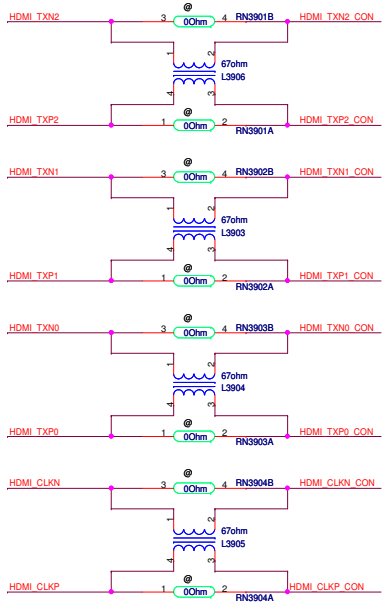
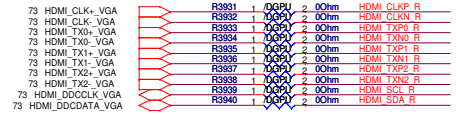


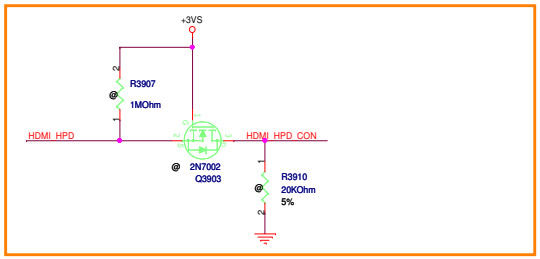
R1.0
HDMI Data and Clock Cost Reduced Level Shifter for Max Data Rate of 1.65 Gb/s



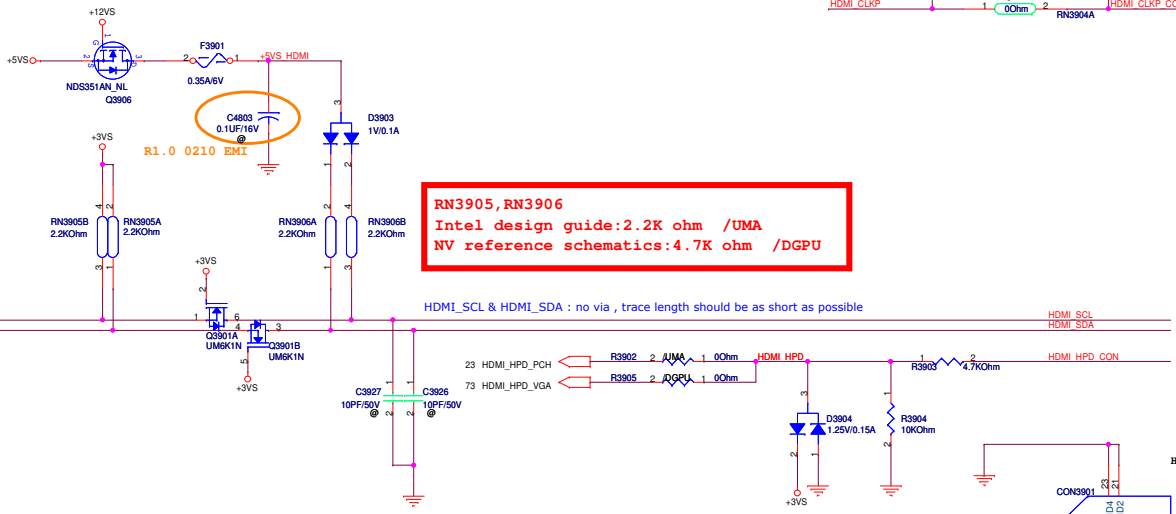




R1.0 0106
HDMI HPD Cost Reduced Level Shifter Design Recommendation



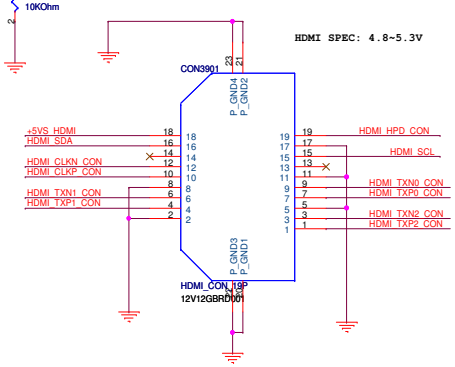
R3926,R3929,R3925,R3923,R3928,R3924,R3922,R3927
Intel design guide : 680ohm /UMA
NV reference schematics : 499ohm /DGPU



RN3905,RN3906
Intel design guide:2.2K ohm /UMA
NV reference schematics:4.7K ohm /DGPU

R3903,R3904
R3903/R3904:4.7Kohm/10Kohm -UMA
R3903/R3904:1Kohm/100Kohm -DGPU

HDMI SPEC: 4.8~5.3V



PEGATRON Title : HDMI
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Wing_Cheng
Size C | Project Name BA52HR/CR | Rev 1.0
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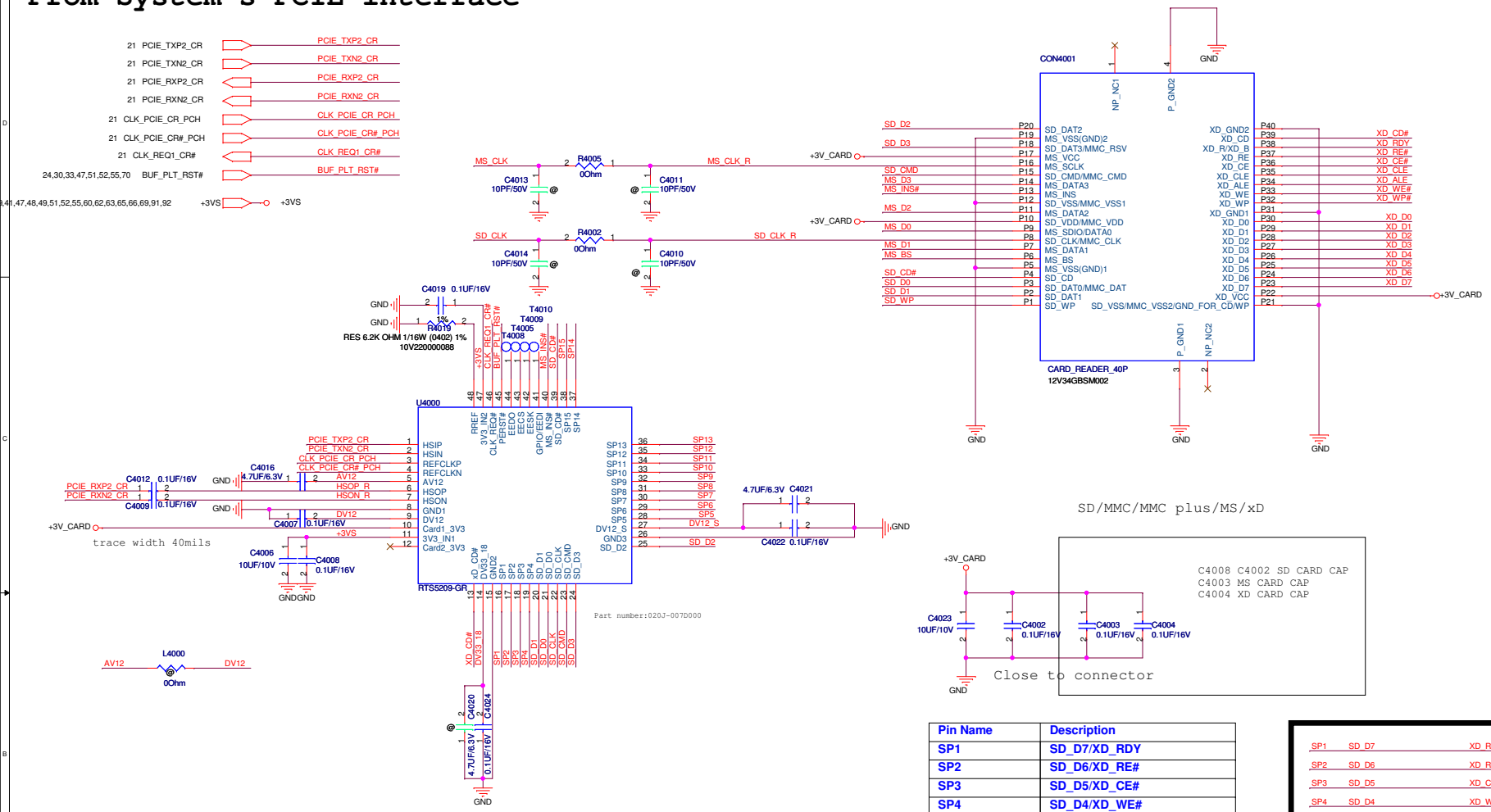
From System's PCIE interface



Remove Serial Flash

Reserve for BIOS boot function

When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

SP1	SD_D7	XD_RDY
SP2	SD_D6	XD_RE#
SP3	SD_D5	XD_CE#
SP4	SD_D4	XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15	SD_WP	XD_D7

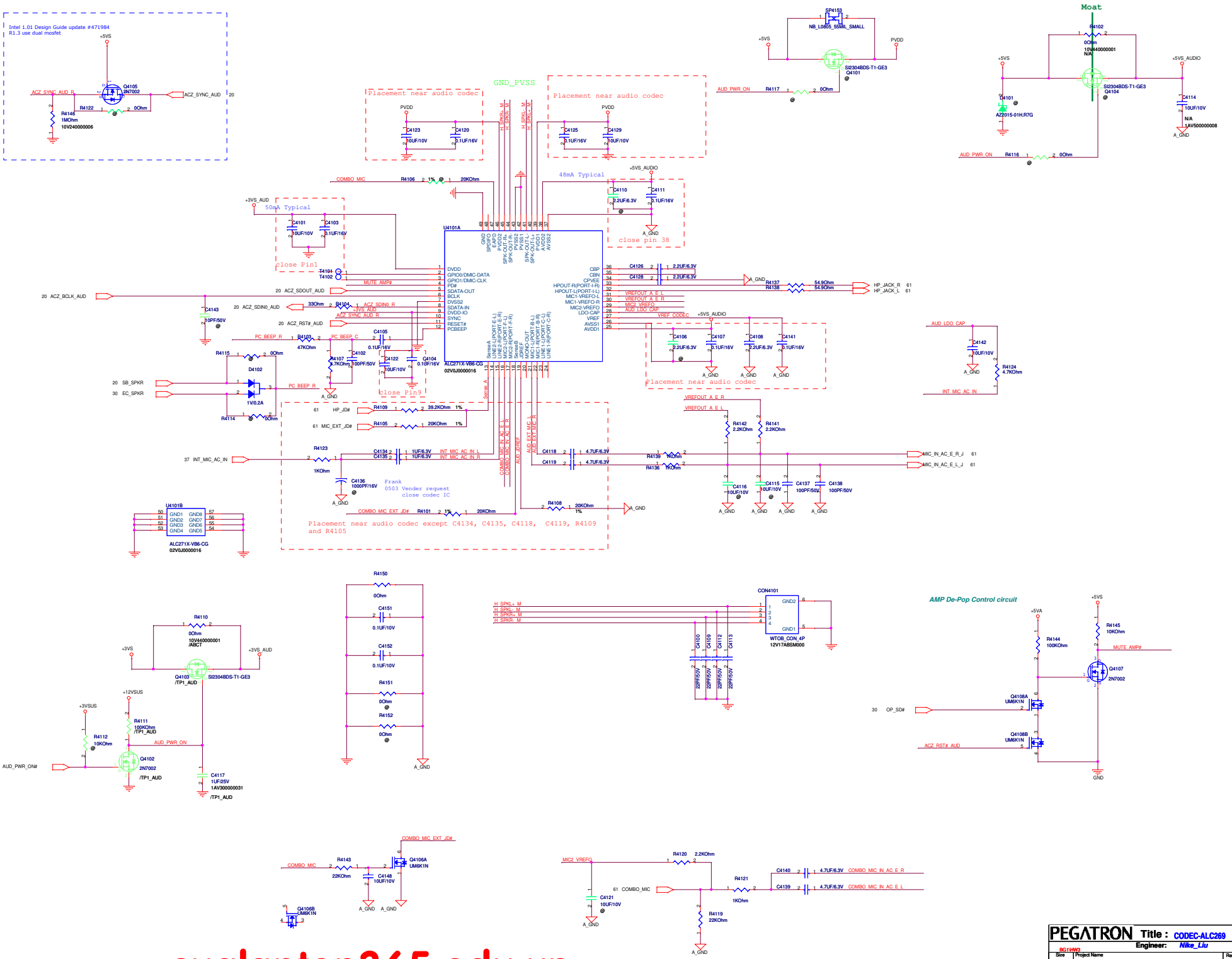
Share Pin

PEGATRON Title : RTS5209

BG1/CSC/HW5 Engineer: Peter5 Huang

Size: Custom | Project Name: Comal | Rev: 1.0

Date: Friday, May 18, 2012 | Sheet 40 of 99


Intel 1.01 Design Guide update #471984
R1.3 use dual mosfet
Placement near audio codec
GND_PVSS
48mA Typical
50mA Typical
close pin 38
close Pin1
close Pin9
Placement near audio codec except C4134, C4135, C4118, C4119, R4109 and R4105
Frank
0503 Vender request close codec IC
AMP De-Pop Control circuit
Moat
ALC271X-VB6-CG
02V0J0000016
WTOB_CON_4P
12V17ABSM000
PEGATRON
Title : CODEC-ALC269
Engineer: Nike_Liu
BA50HR/CR
Friday, May 18, 2012
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PEGATRON Title : AUDIO ALC269

BG1\HW3 Engineer: Nike_Liu

Size	Project Name	Rev
B	BA50HR/CR	1.0

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PEGATRON Title : MDC CONN

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

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Del Entry audio circuit

SR-8
0121-11

PEGATRON	Title : CODEC-ALC269	
ASUSTeK COMPUTER INC. NB1	Engineer: Wing_Cheng	
Size: Custom	Project Name: BA52HR/CR	Rev: 1.0
Date: Friday, May 18, 2012	Sheet 44 of 77	

Del Entry audio circuit

SR-8
0121-11

PEGATRON

Title : AUDIO ALC269

BU1-RD Div.1-HW RD Dept.1

Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

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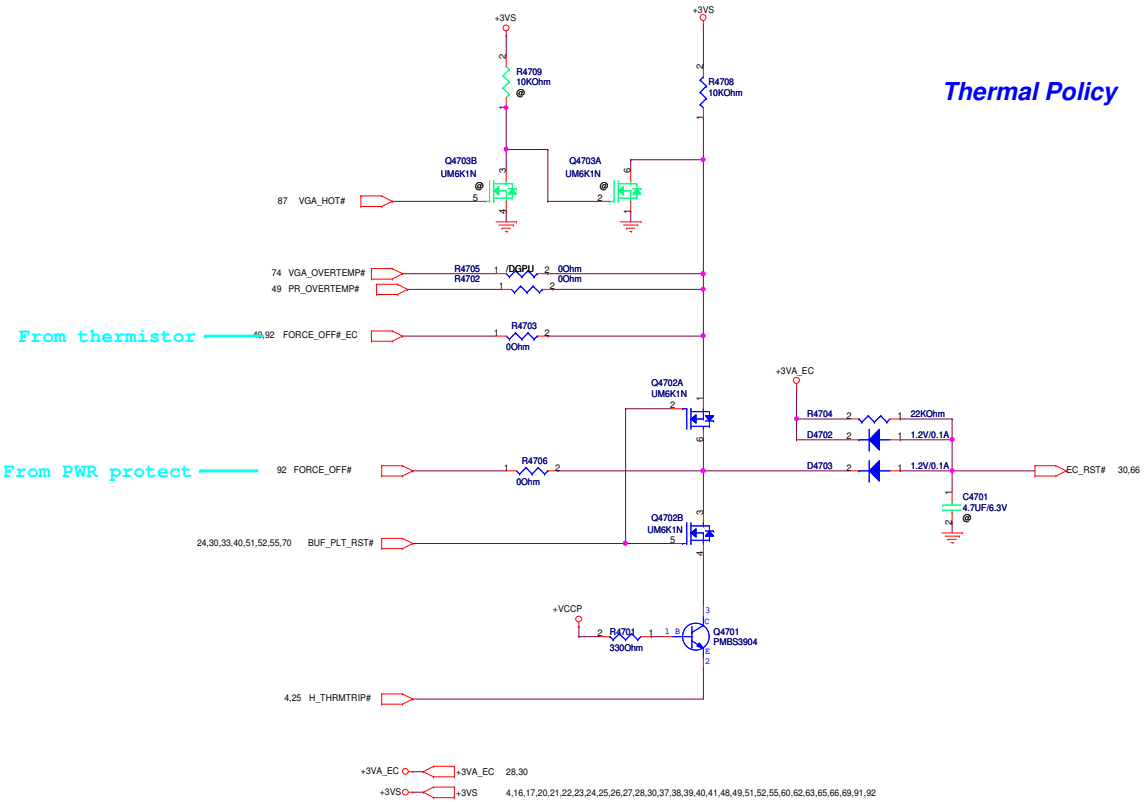


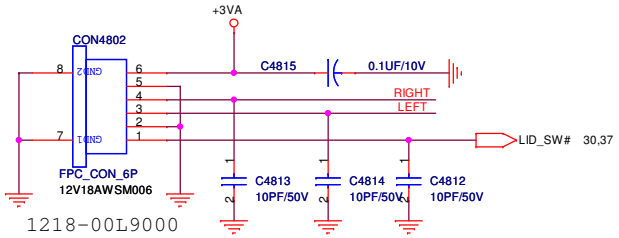
PEGATRON Title : RST_Reset Circuit

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

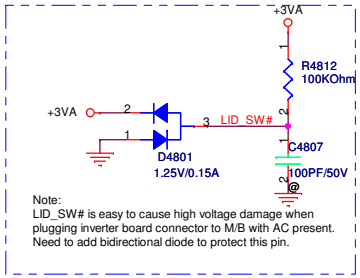
Date: Friday, May 18, 2012 Sheet 47 of 77

Touch Pad Button/ Hall Sensor

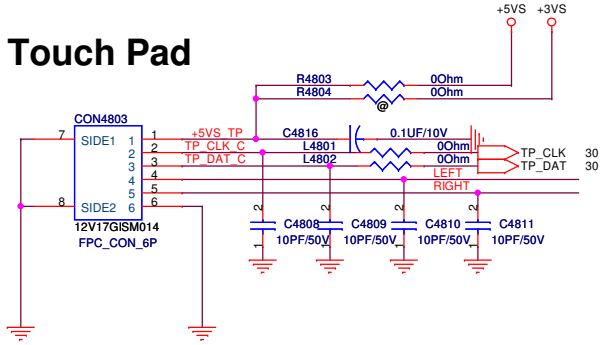


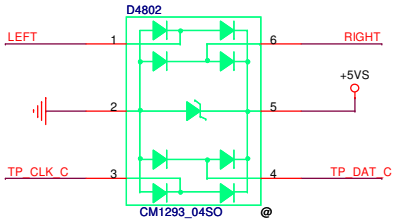
1218-00L9000

close to CON4802

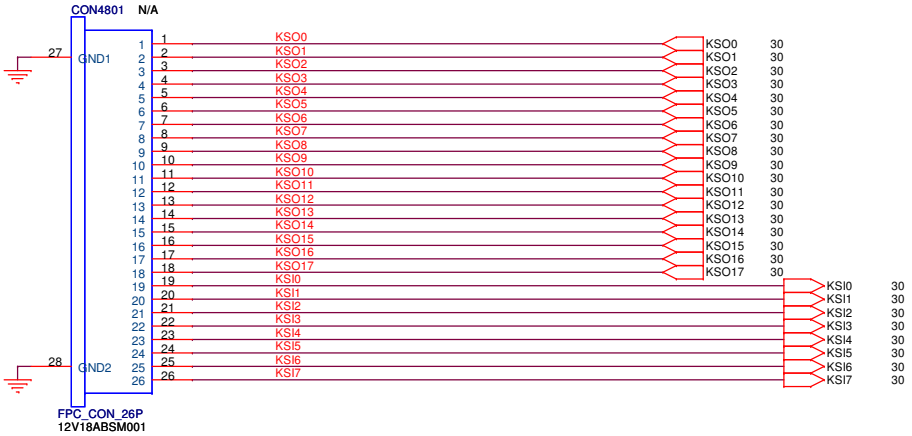


Touch Pad



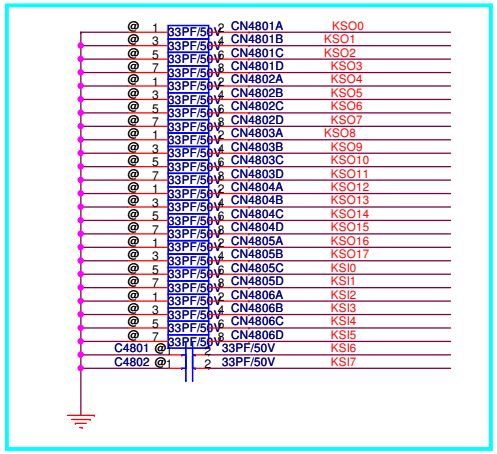


Keyboard



1218-00MW000

EMI



PEGATRON Title : KB/ TP/ FLASH

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

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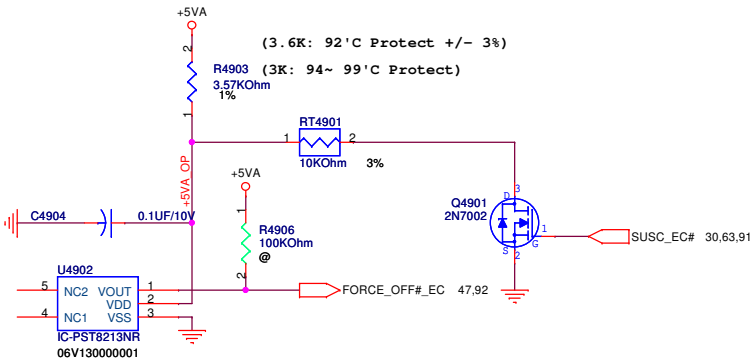
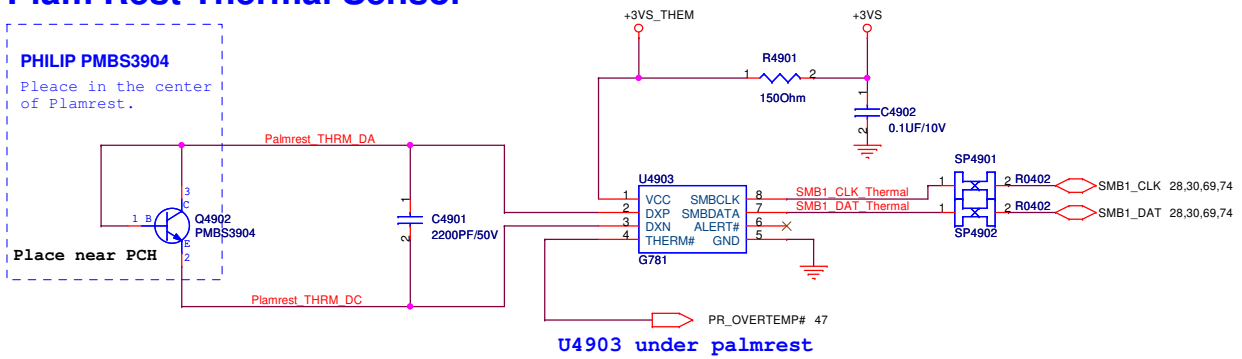
Thermister



Plam Rest Thermal Sensor

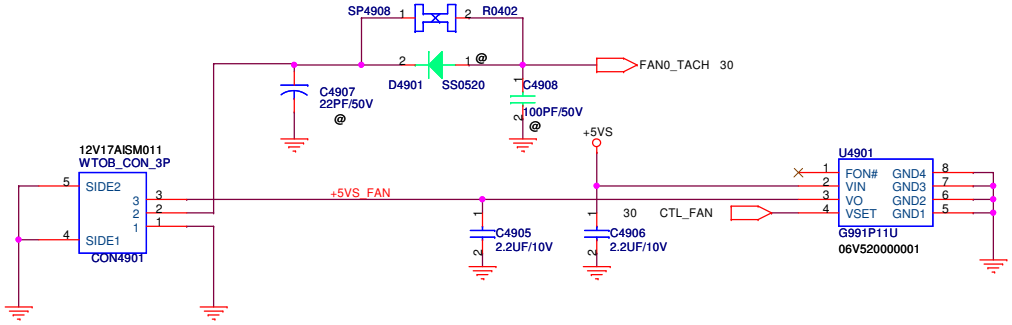


U4903 under palmrest

SMBUS addr=1001100x (98)

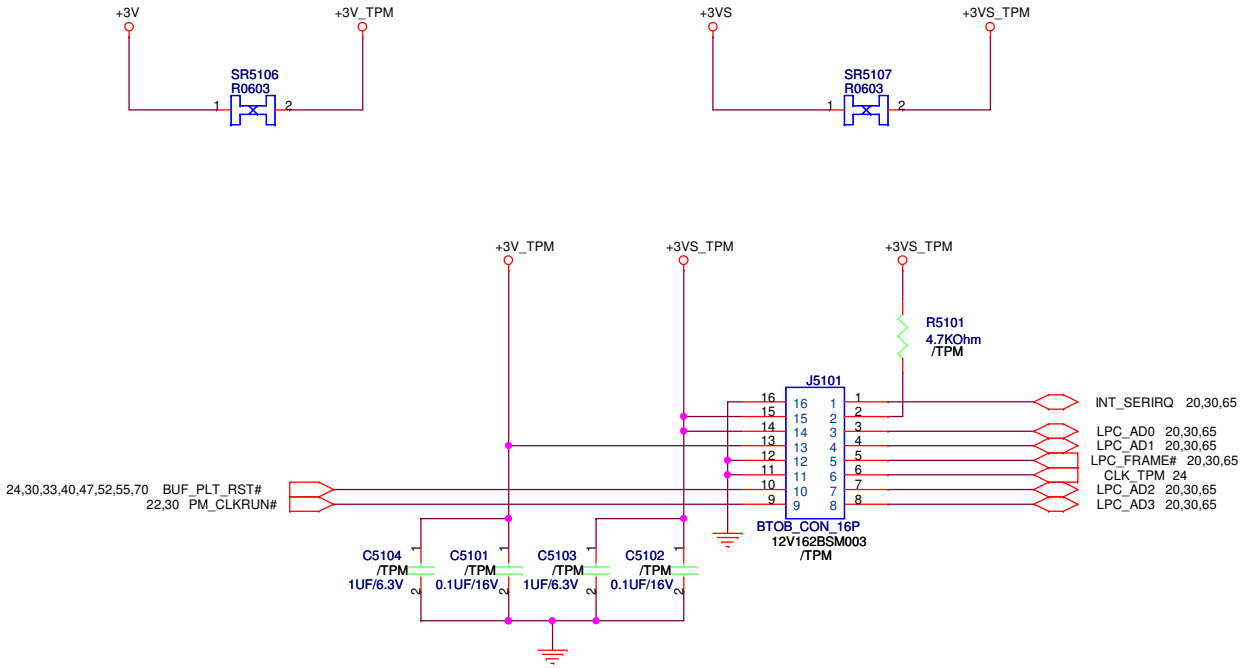
U4903: Remote(Local) thermal sensor,use remote mode.

FAN



1217-00LH000

PEGATRON	Title : THERMAL/FAN	
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng	
Size: Custom	Project Name: BA52HR/CR	Rev: 1.0
Date: Friday, May 18, 2012	Sheet 49 of 77	

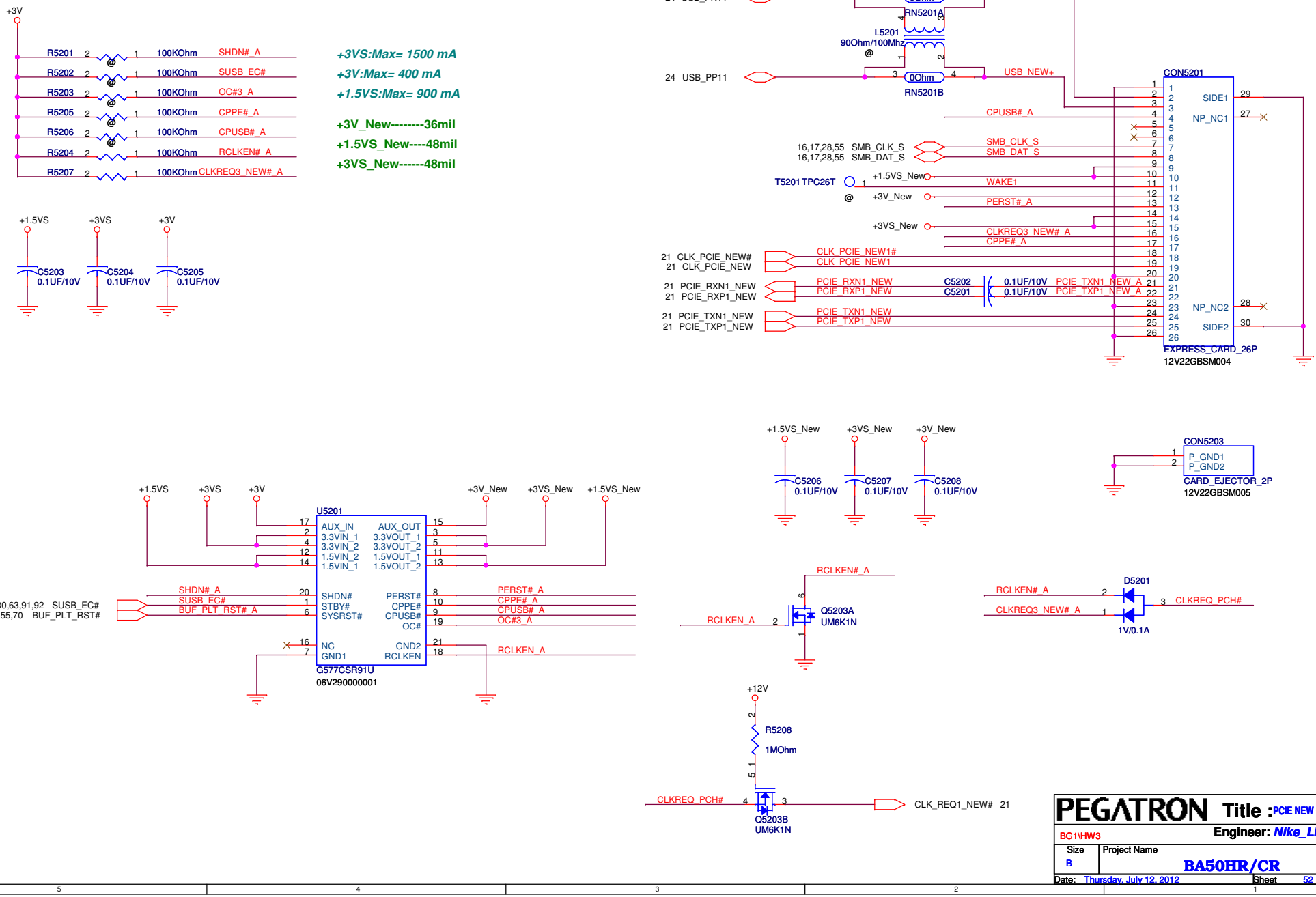


PEGATRON Title : USB3.0 uPD720200

BG1\HW1 Engineer: Wing_Cheng

Size	Project Name	Rev
B	BA52HR/CR	1.0

Date: Friday, May 18, 2012 Sheet 51 of 77



PEGATRON Title : MINICARD (WWAN)

BU1-RD Div.1-HW RD Dept.1 Engineer:

Size	Project Name	Rev
Custom		1.0

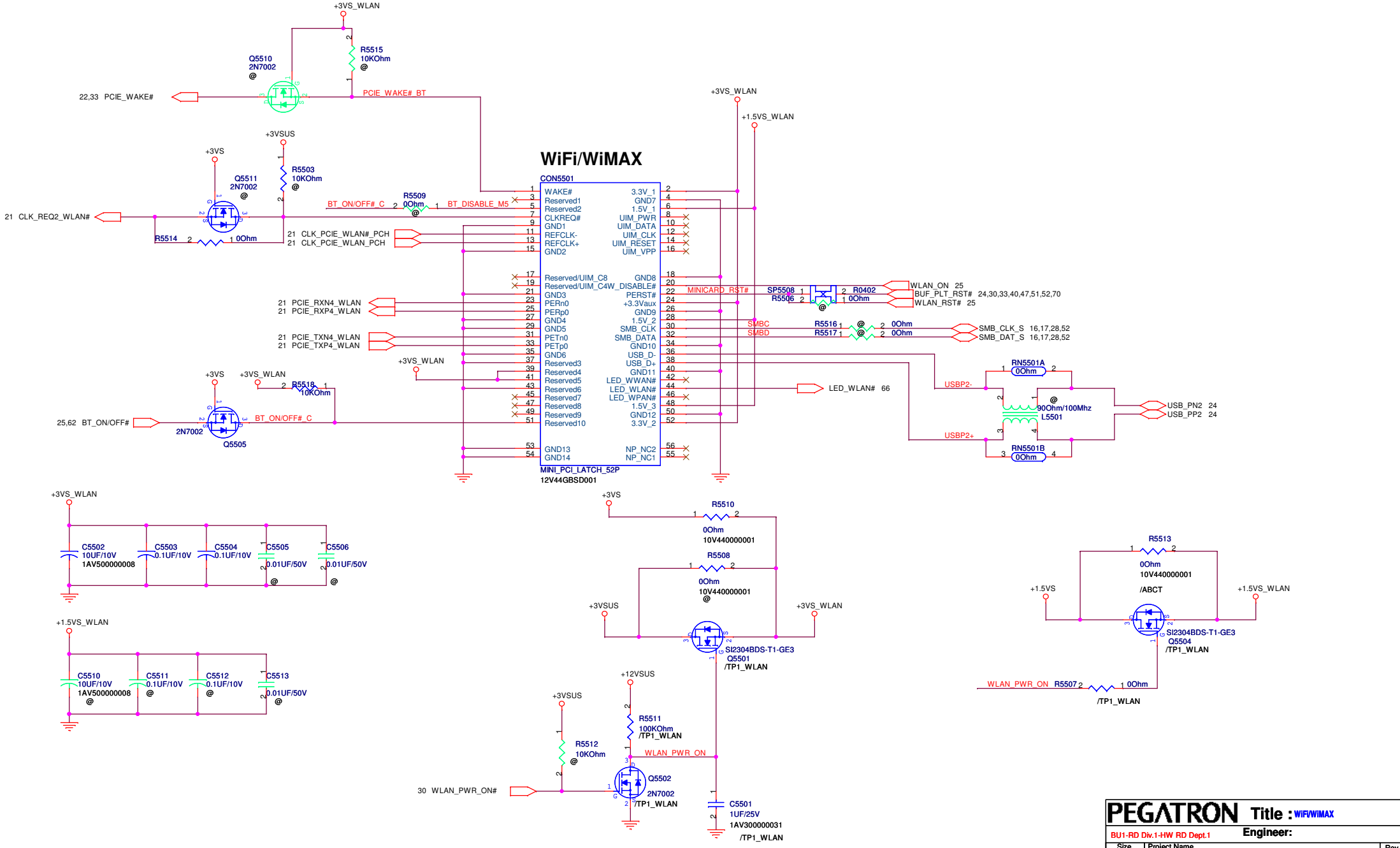
Date: Friday, May 18, 2012 Sheet 53 of 77

PEGATRON Title : MINICARD (WUSB /UPCONVERT)

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

Date: Friday, May 18, 2012 Sheet 54 of 77

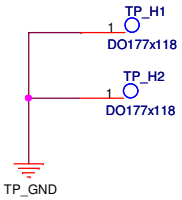


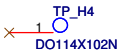
PEGATRON Title : WiFi/WiMAX

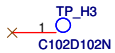
BU1-RD Div.1-HW RD Dept.1 Engineer:

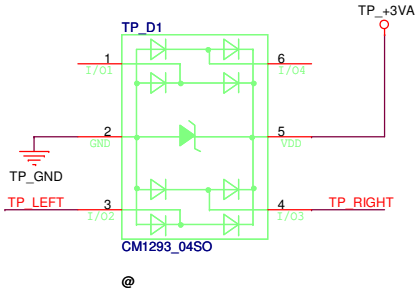
Size	Project Name	Rev
Custom	BA52HR/CR	1.0

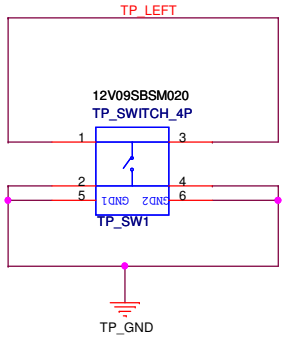
Date: Friday, May 18, 2012 Sheet 55 of 77



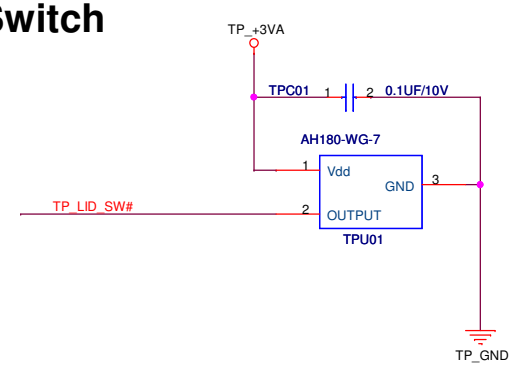


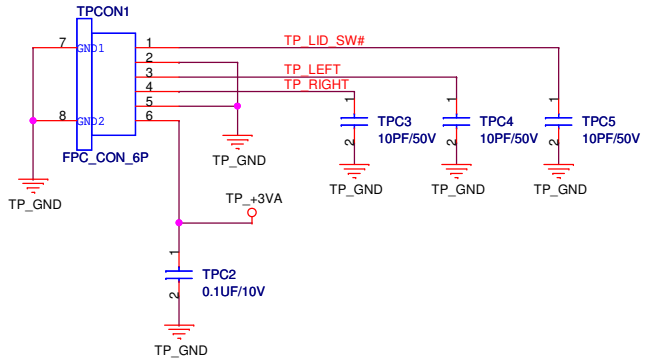


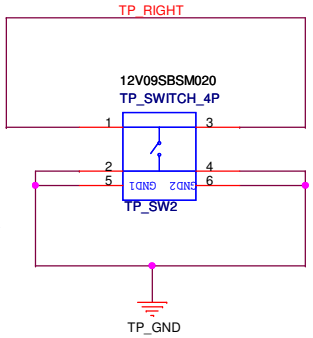




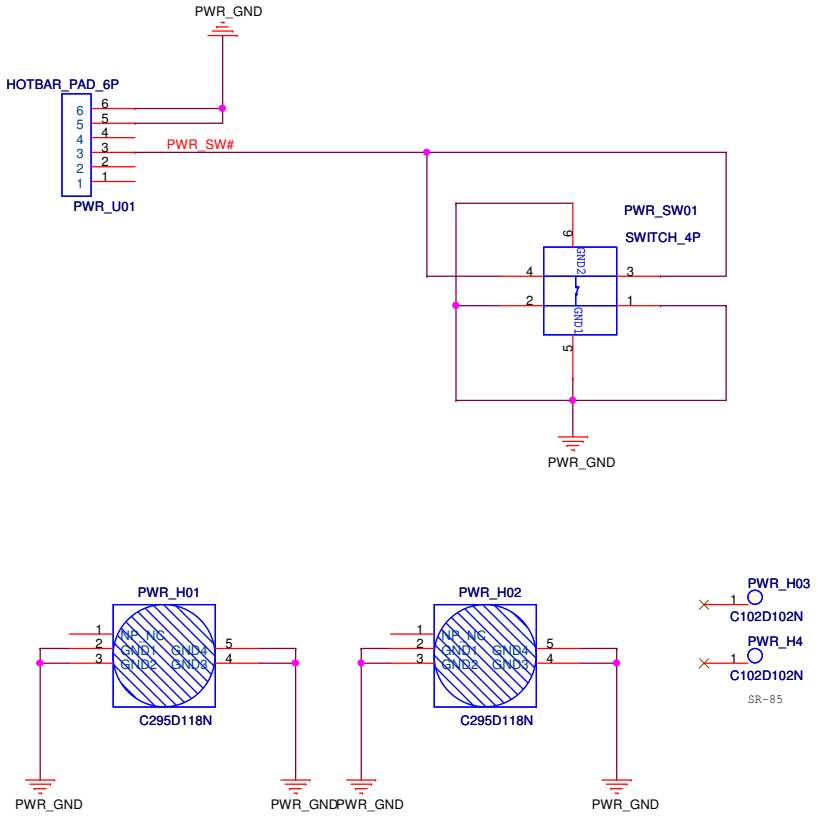
LID Switch



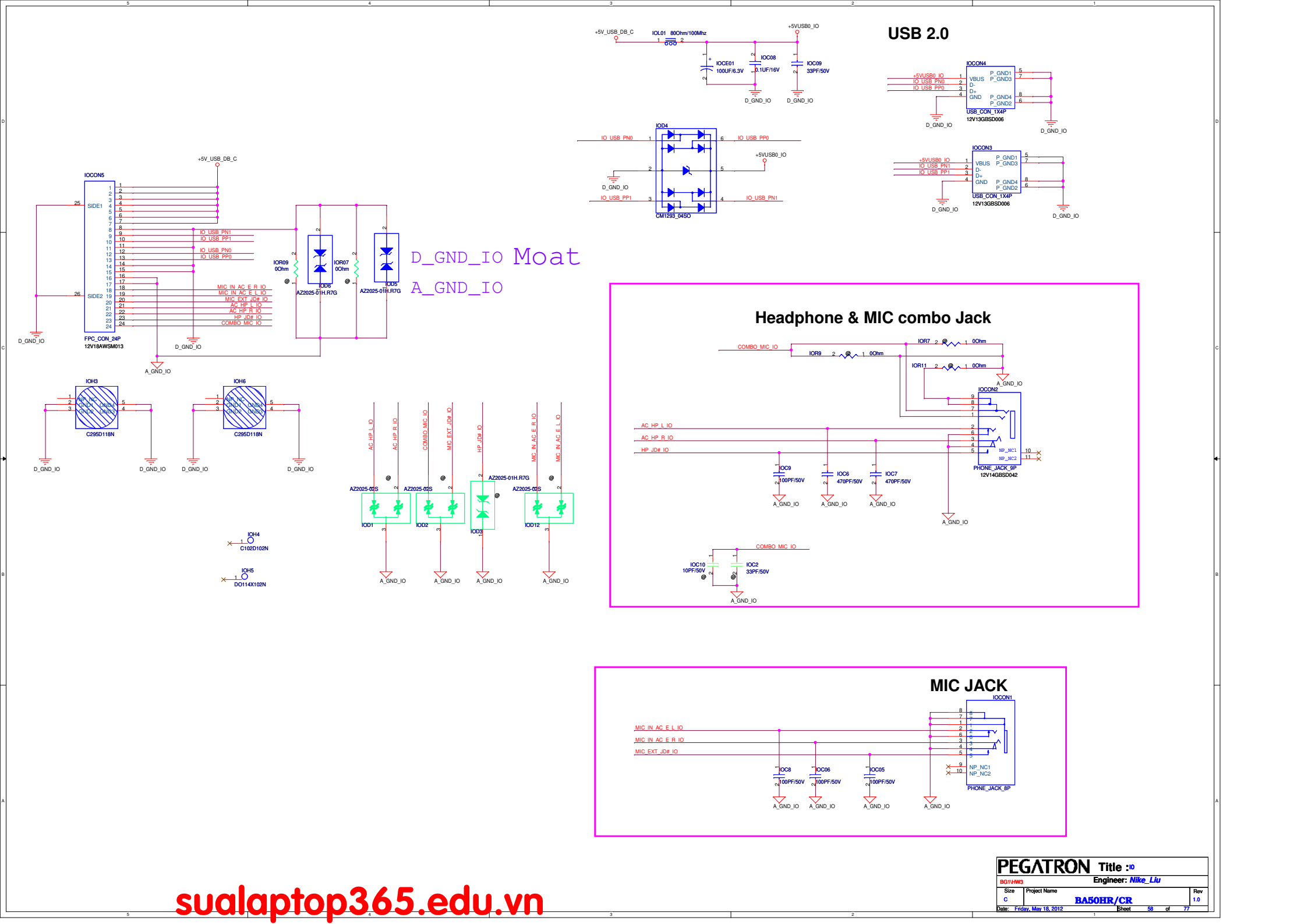




PEGATRON	Title : TP_M	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Wing_Cheng	
Size: B	Project Name: BA52HR/CR	Rev: 1.0
Date: Friday, May 18, 2012	Sheet 56 of 77	



PEGATRON	Title : PWR BTN		
BU1-RD Div.1-HW RD Dept.1	Engineer: Wing_Cheng		
Size: B	Project Name: BA52HR/CR		Rev: 1.0
Date: Friday, May 18, 2012	Sheet 57 of 77		



PEGATRON Title : IO

BG1\HW3 Engineer: Nike_Liu

Size	Project Name	Rev
C	BA50HR/CR	1.0

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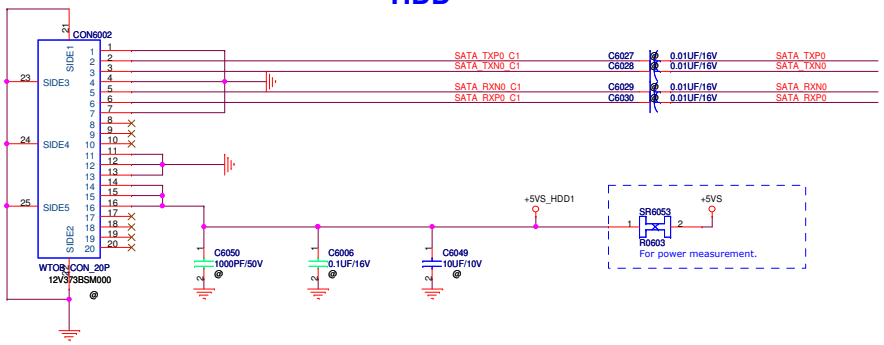
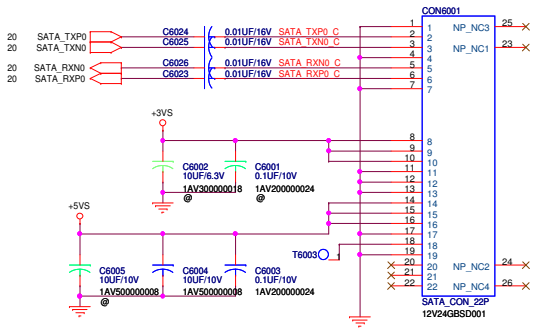
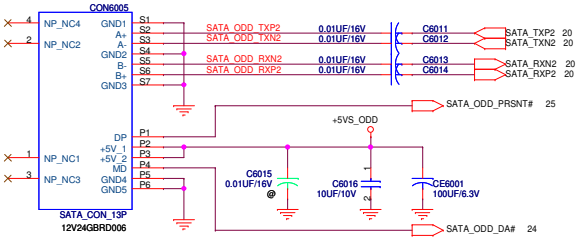
HDD



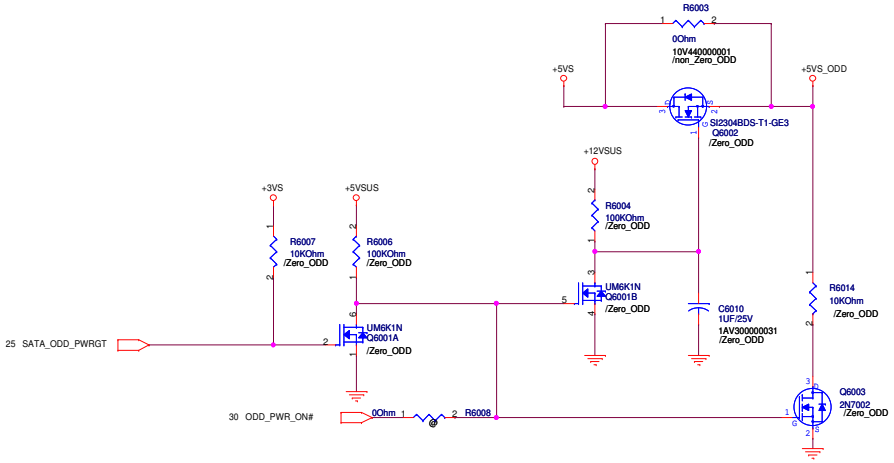
HDD



ODD



ZERO POWER ODD SUPPORT



PEGATRON Title : SATA HDD/ODD

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

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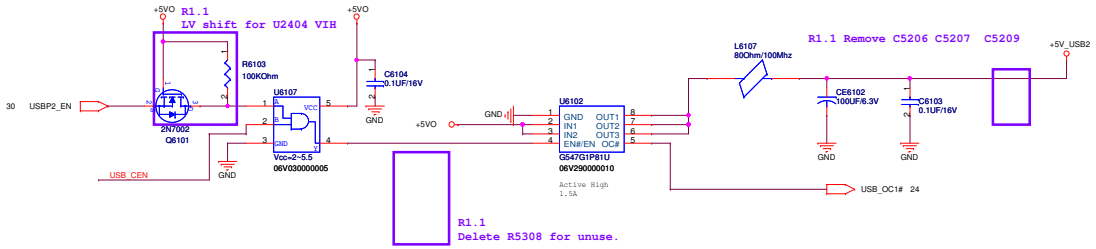
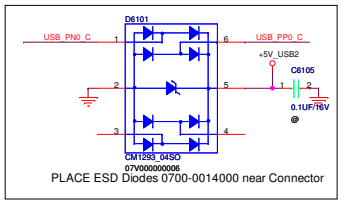
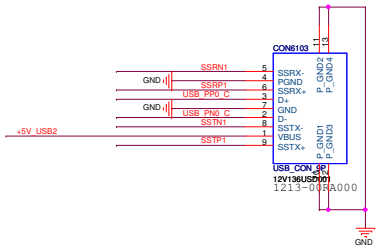
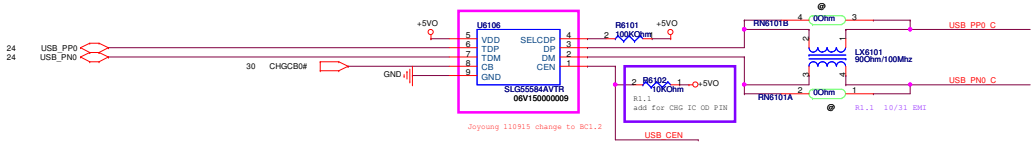
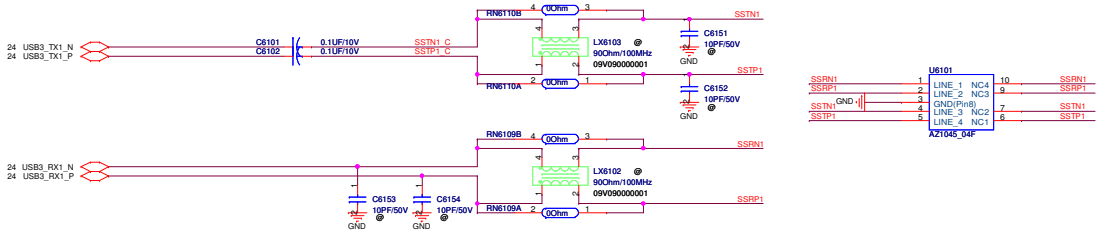


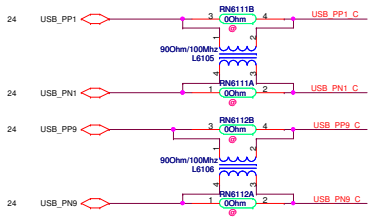


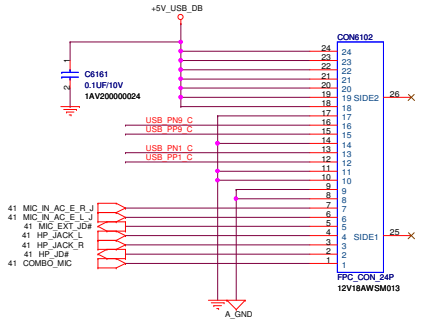




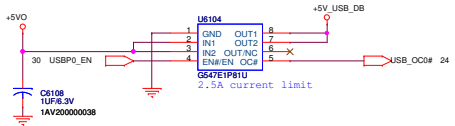


AUDIO BOARD/w USB2.0 x2

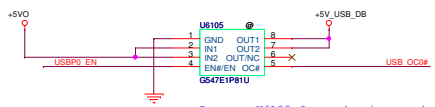




USB Power Switch for USB DB Main



change USB power switch circuit

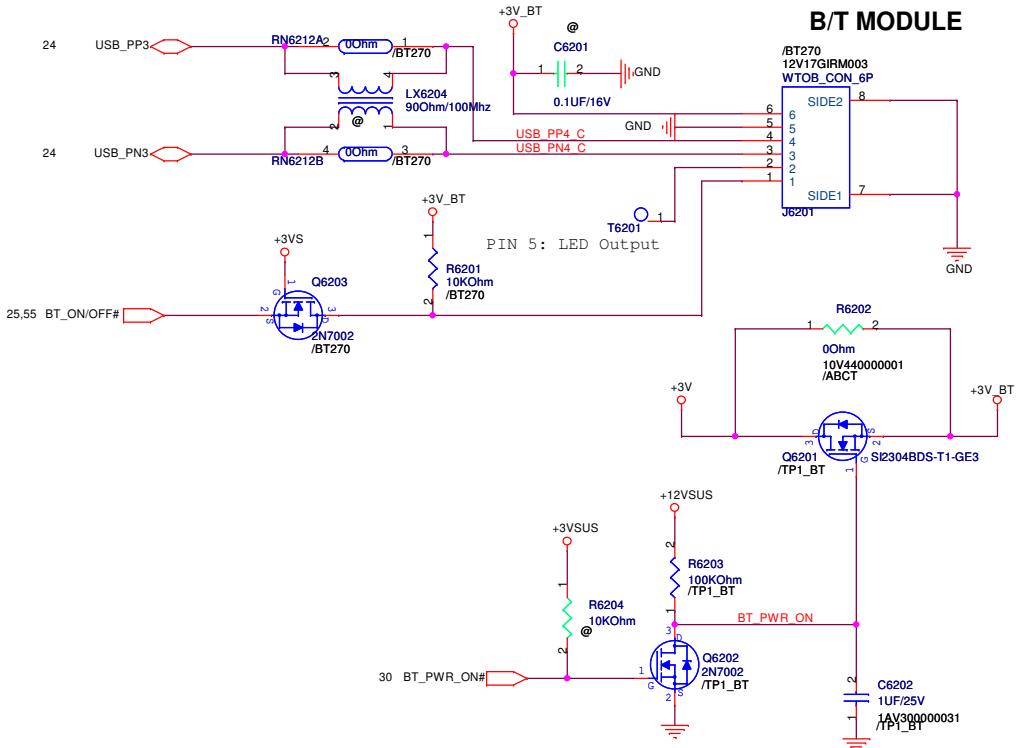


PEGATRON Title : USB PORTS/ eSATA
BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng
Size: Custom | Project Name: BA52HR/CR | Rev: 1.0
Date: Friday, May 18, 2012 | Sheet 61 of 77

TouchPanel CON

Camera Module CON

B/T MODULE



FELICA MODULE

PEGATRON Title : Camera/ BT/ FL CONN

BU1-RD Div.1-HW RD Dept.1 Engineer: Nike_Liu

Size	Project Name	Rev
Custom	BA50HR/CR	1.0

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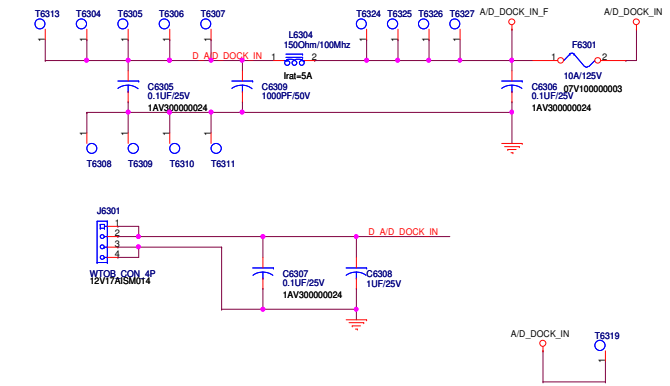
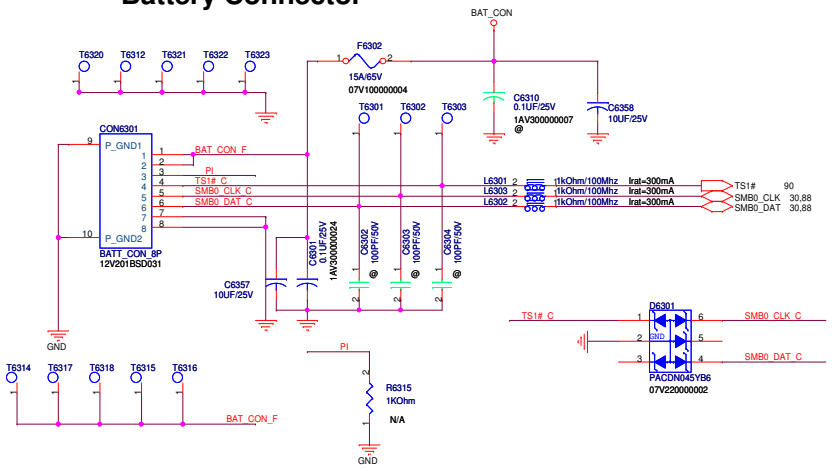
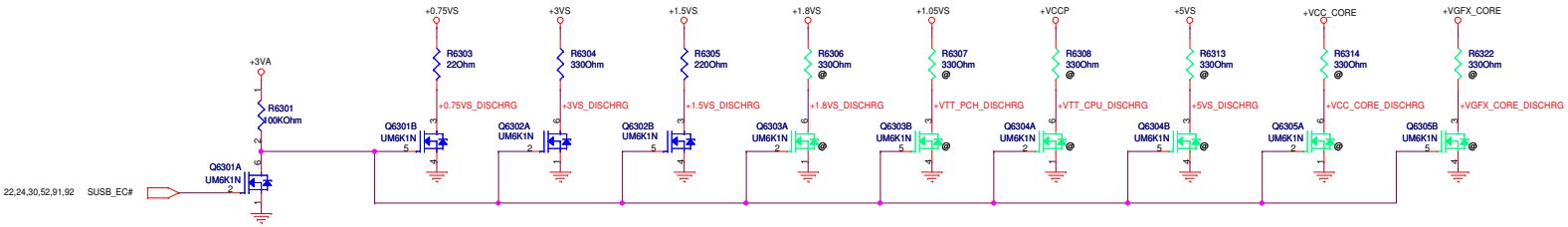
DC IN



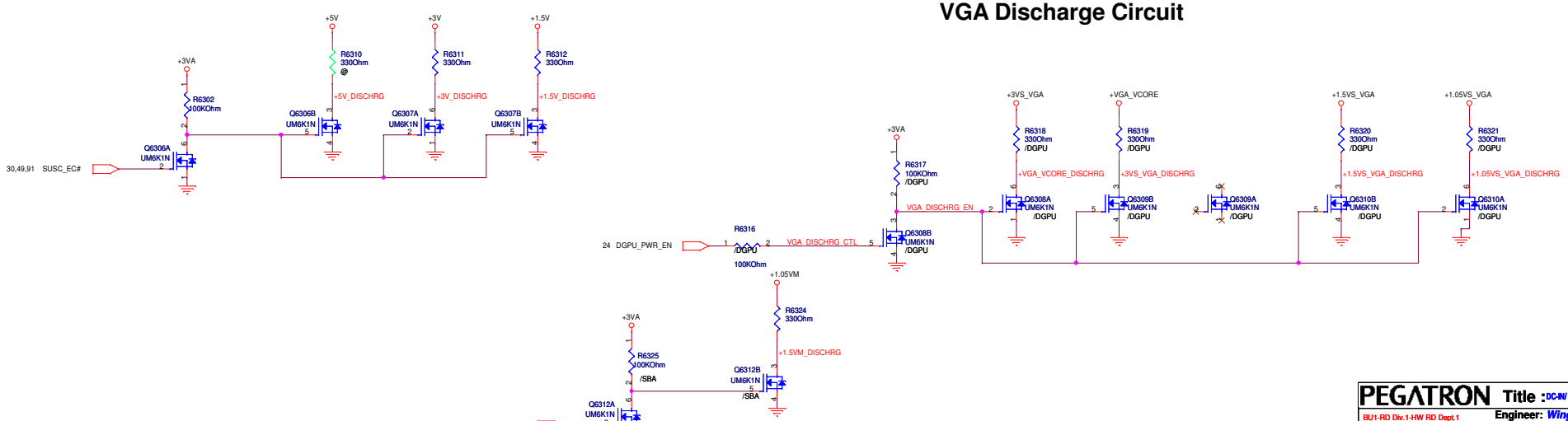
Battery Connector



Discharge Circuit



VGA Discharge Circuit



PEGATRON Title : DC-IN/ DISCHARGE

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
C	BA52HR/CR	1.0

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Notes:
BRAIDWOOD right angled Connector (1.8V keyed)
Compatible BRAIDWOOD Modules
1.8V Mobile NVM 4GB 31.60mm x21.5mm
1.8V Mobile NVM 8GB 31.60mm x 21.5mm
1.8V Mobile NVM 16GB 31.60mm x 32.5mm

PEGATRON Title : NVM

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

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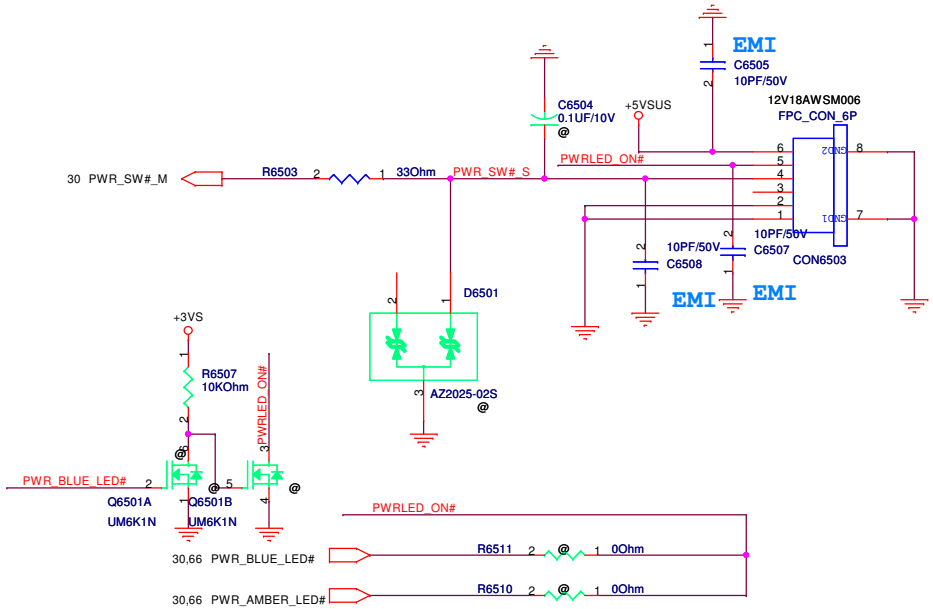
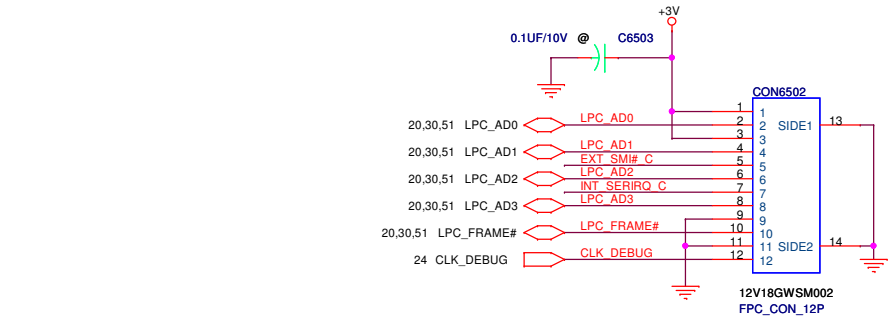
PWR BRD/ AMBIENT/ HALL CONN.



MODEM MODULE

KILL SWITCH.

DEBUG CARD CONN.



20,30,51 INT_SERIRQ R6501 2 @ 1 0Ohm INT_SERIRQ_C

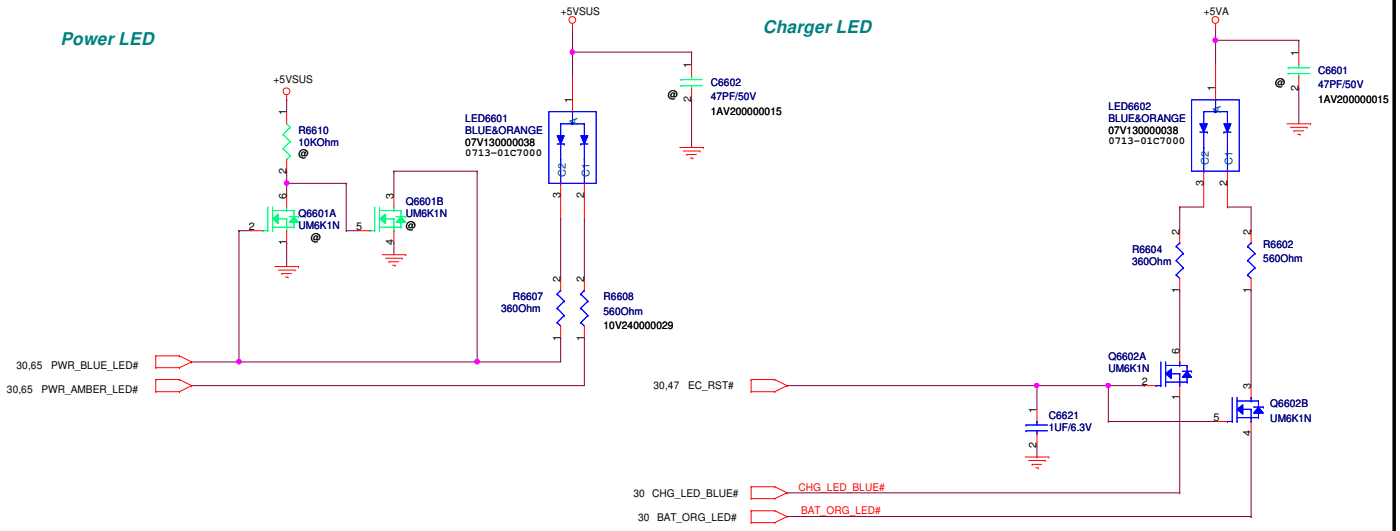
25,30 EXT_SMI# R6502 2 @ 1 0Ohm EXT_SMI#_C

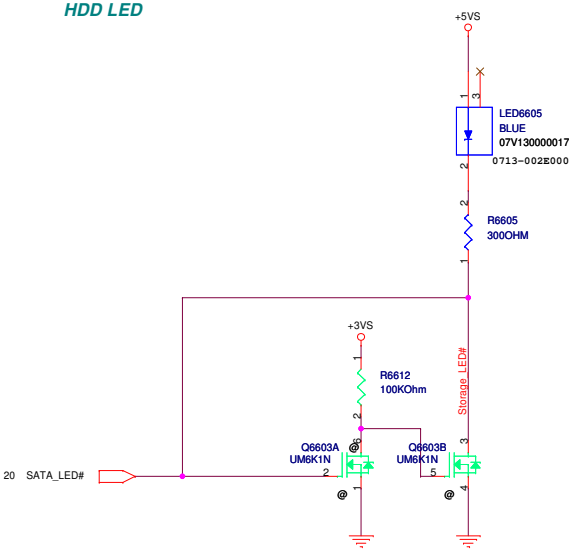
PEGATRON Title : MDC/ PWR SW/ Debug

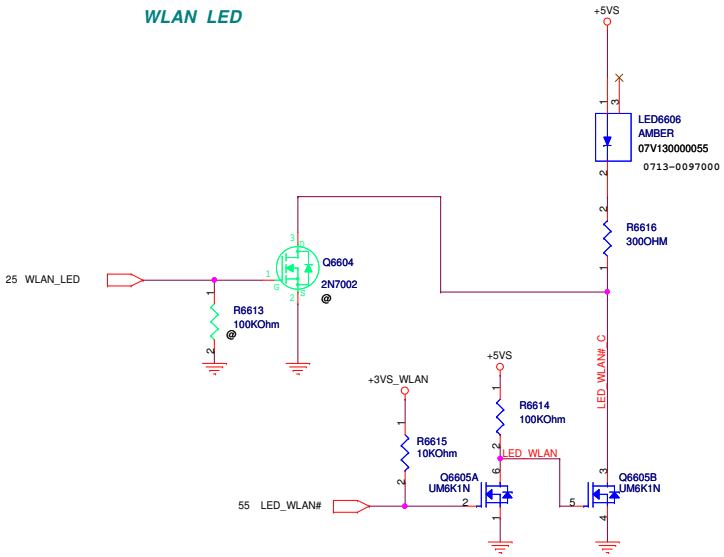
BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

Date: Friday, May 18, 2012 Sheet 65 of 77







PCH Local Side Symbol

WLAN NUT

H6628
CT217B176D146

Fix hole

H6649
C102D102N

Detail C

H6650
DO114X102N

R1.2-16 EMI

H6646
C354D118N

R2.0-2 EMI

S6601
EMI_SPRING_PAD
靠近D_SUB
1302-0097000

S6602
EMI_SPRING_PAD
1302-0098000
靠近CPU
@

Screw Ax15

H6637
C354D118
H6639
C354D118
H6640
C354D118
H6642
C354D118
H6651
C354D118
H6648
C354D118

FCH

H6611
CT236B67ID47
H6612
CT236B67ID47

H6614
CRT293CB276D142
H6615
CRT293CB276D142
H6616
CRT293CB276D142
H6617
CRT293CB276D142

Screw Px4
CPU

GPU Screw B x 2

H6605
CRT370X382CBD138
H6606
CRT370X382CBD138

R2.0-1

H6641
H6653
H6638
H6647
H6652
H6644
C354D118N

H6643
CT236CB276D118

PEGATRON Title : LED/ CIR/ FN SCREW
BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng
Size: Custom | Project Name: BA52HR/CR | Rev: 1.0
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PEGATRON Title : Fenaco USB 3.0

Pegatron Corp. Engineer: Wing_Cheng

Size	Project Name	Rev
A1	RA52HR/CR	1.0

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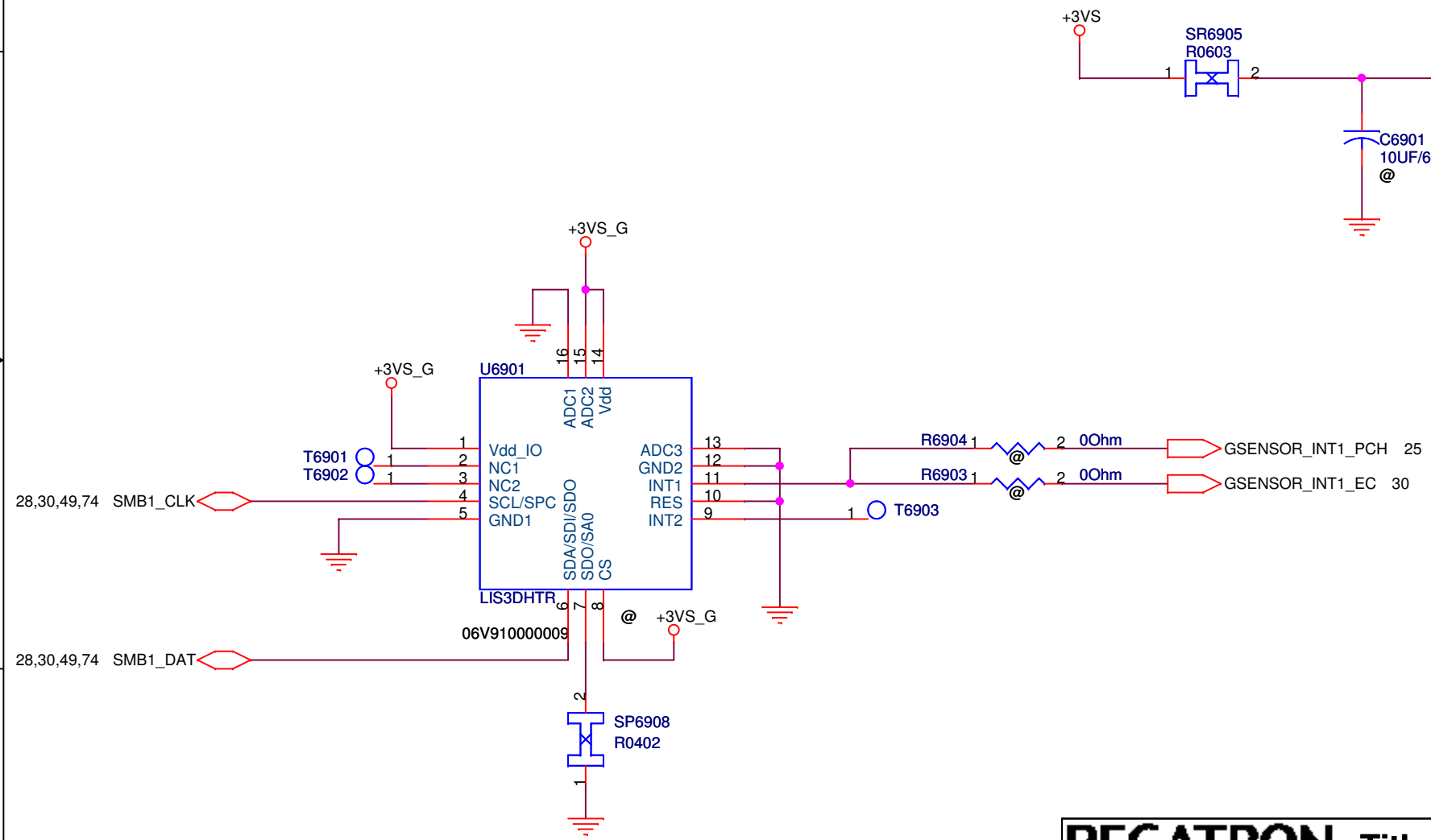
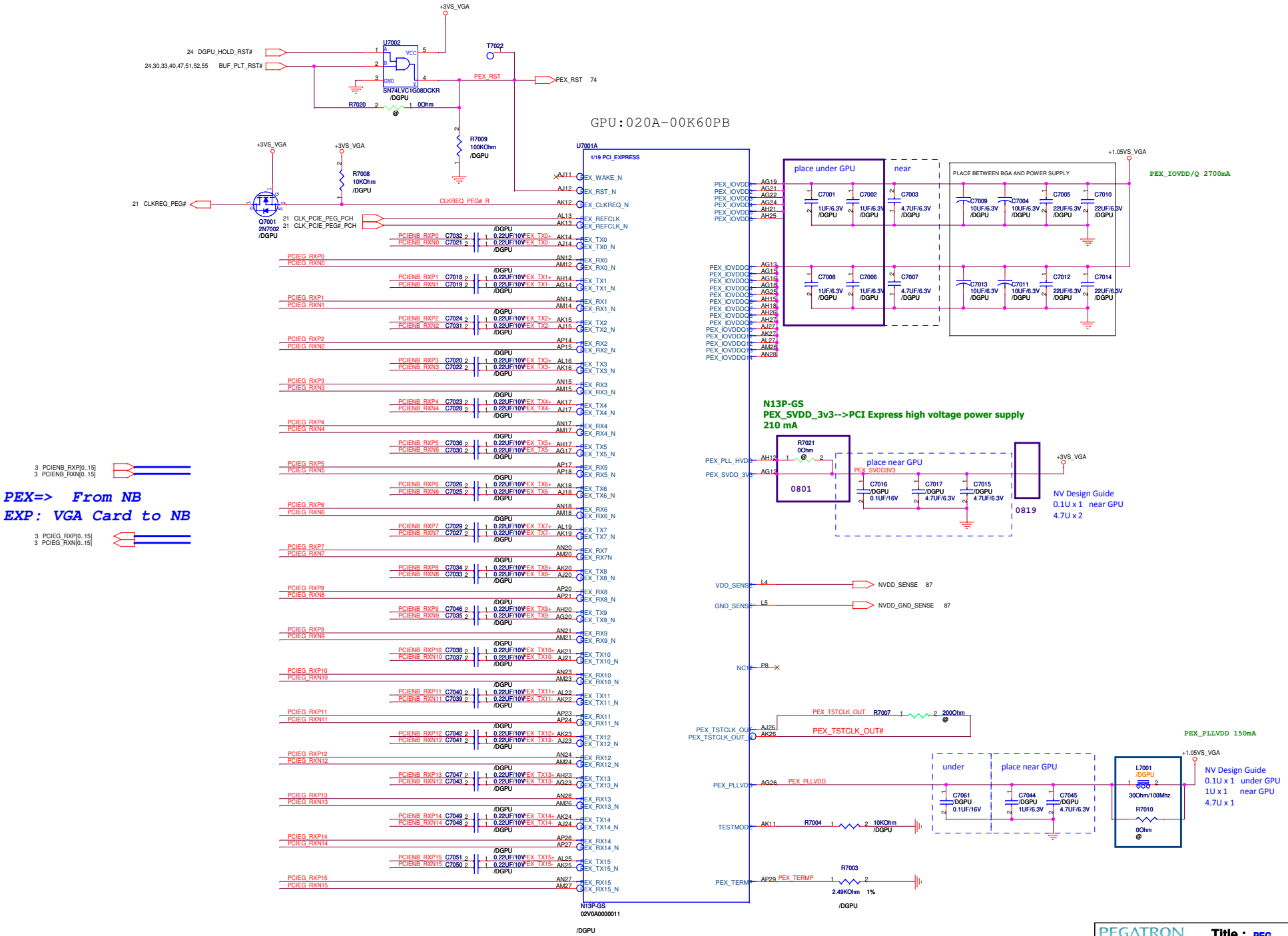


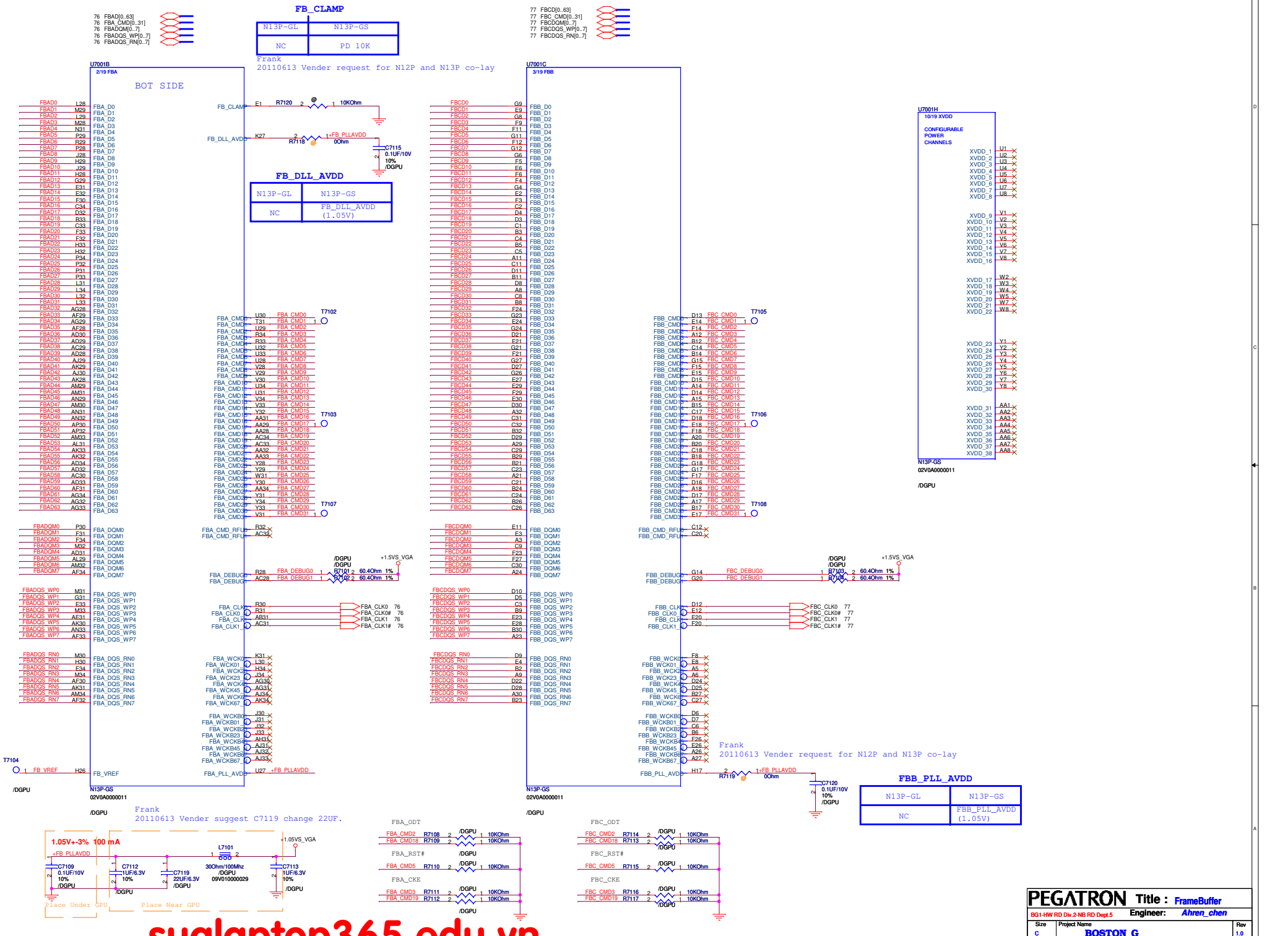
PEGATRON	Title : G-Sensor LIS3DHTR	
BU1-RD Div.1-HW RD Dept.1	Engineer: Nike_Liu	
Size: A	Project Name: BA50HR/CR	Rev: 1.0
Date: Friday, May 18, 2012	Sheet 69 of 77	

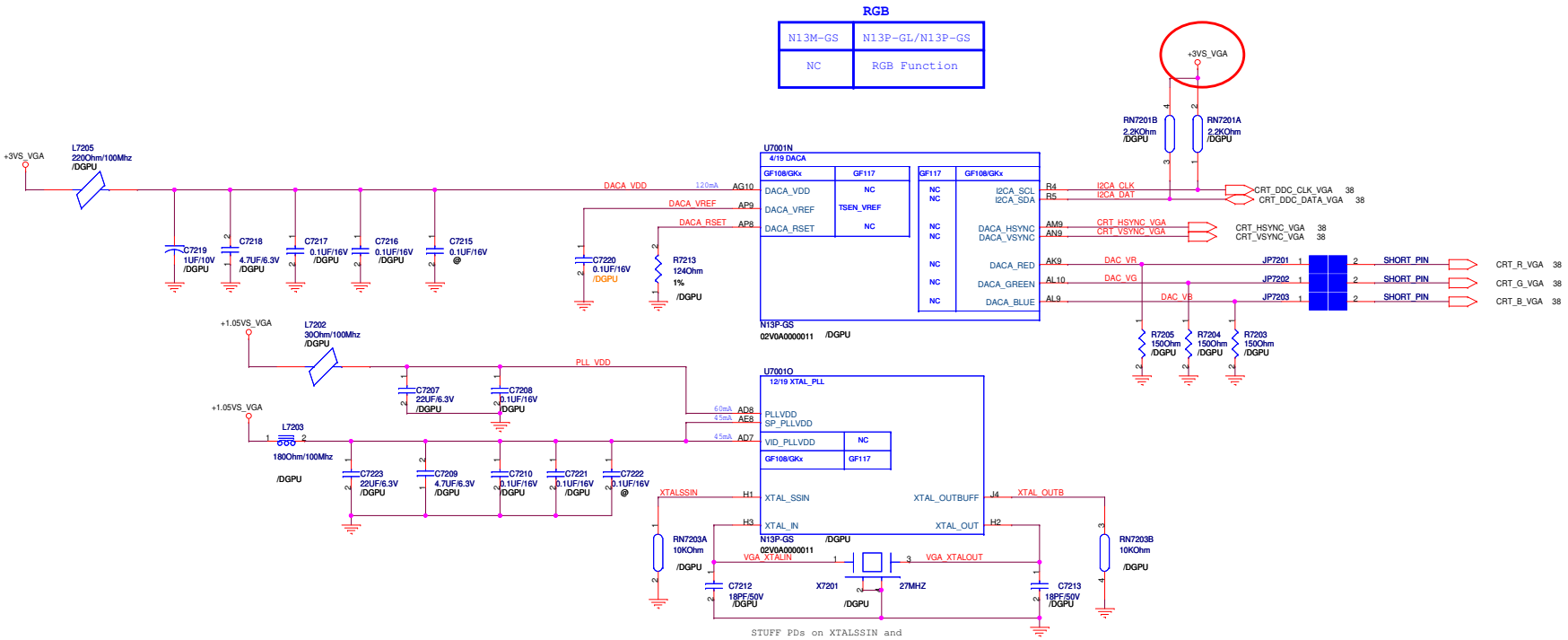
Frank
20110513 Change N13P GPU.

GPU:020A-00K60PB



PEGATRON	Title : PEG		
PEGATRON COMPUTER INC	Engineer: Ahren_Chen		
Size C	Project Name N13P-GDDR5		Rev 1.3
	P/N <OrgAddr2>		
Date: Friday, May 18, 2012	Sheet 70 of 99		





PEGATRON
PEGATRON COMPUTER INC

Title : FRAME BUFFER C
Engineer: Ahren_Chen

Size	Project Name	Rev
C	N13P-GDDR5	1.0
	P/N: <OrgAddr2>	

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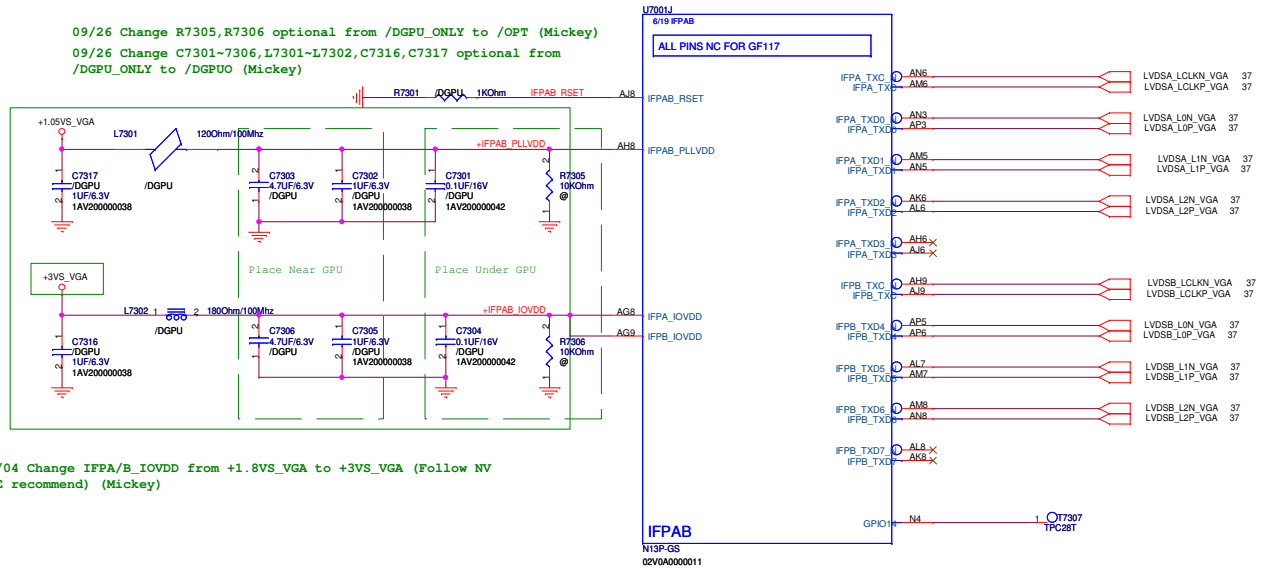
LVDS

09/26 Change R7305,R7306 optional from /DGPU_ONLY to /OPT (Mickey)

09/26 Change C7301~7306,L7301~L7302,C7316,C7317 optional from /DGPU_ONLY to /DGPUO (Mickey)



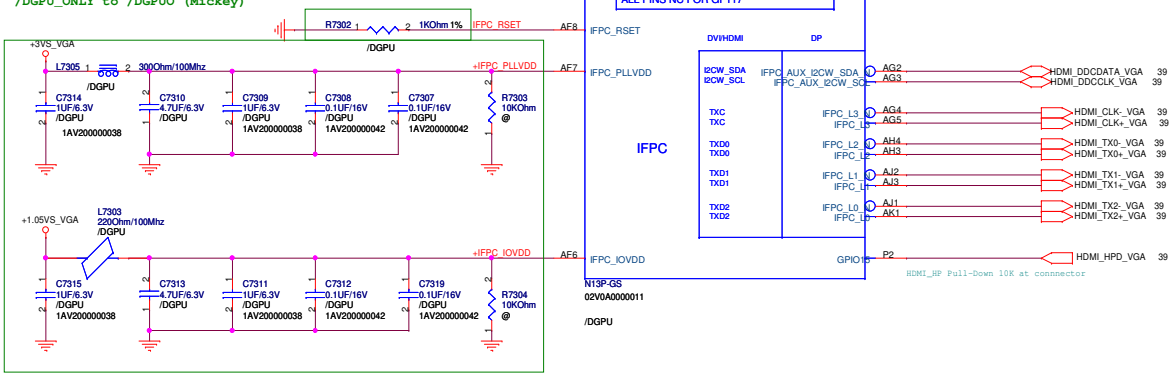
10/04 Change IFPA/B_IOVDD from +1.8VS_VGA to +3VS_VGA (Follow NV FAE recommend) (Mickey)

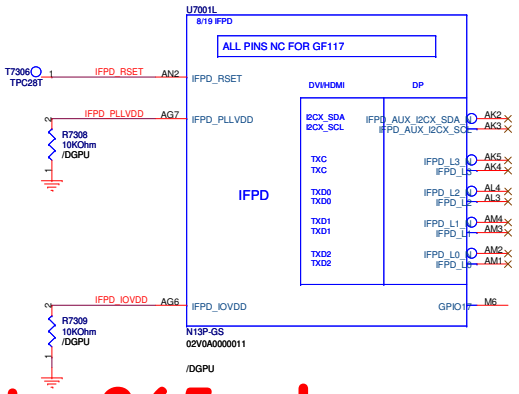
HDMI

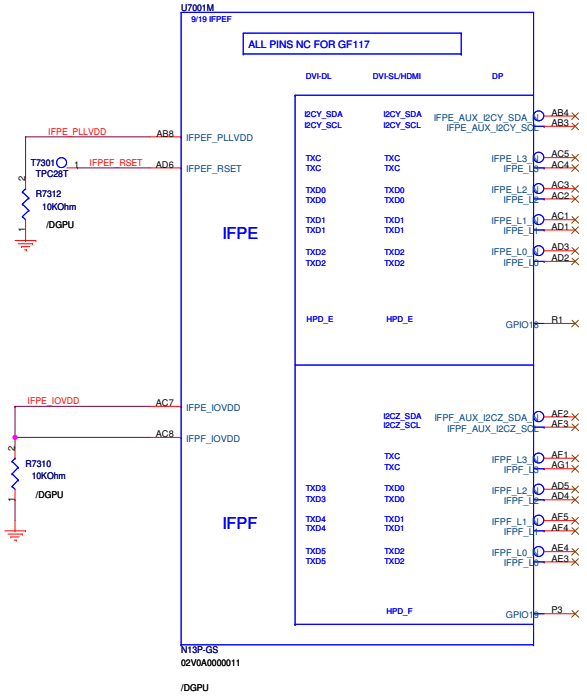
09/27 Change R7302 optional from /DGPU to /N13P-GS_N13P-GL (Mickey)

09/26 Change R7303,R7304 optional from /DGPU_ONLY to /OPT (Mickey)

09/26 Change C7307~7315,L7303,L7305 optional from /DGPU_ONLY to /DGPUO (Mickey)



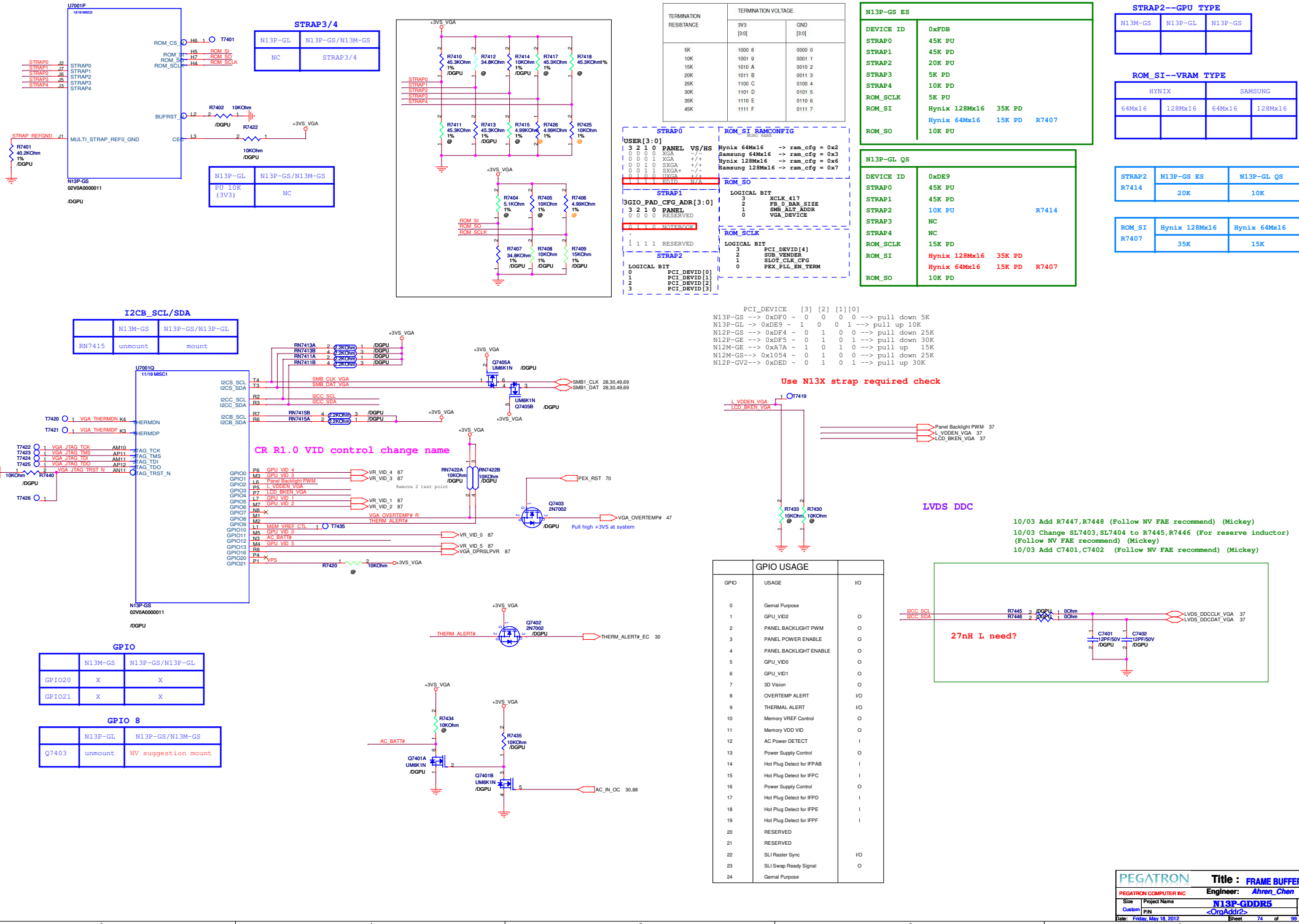


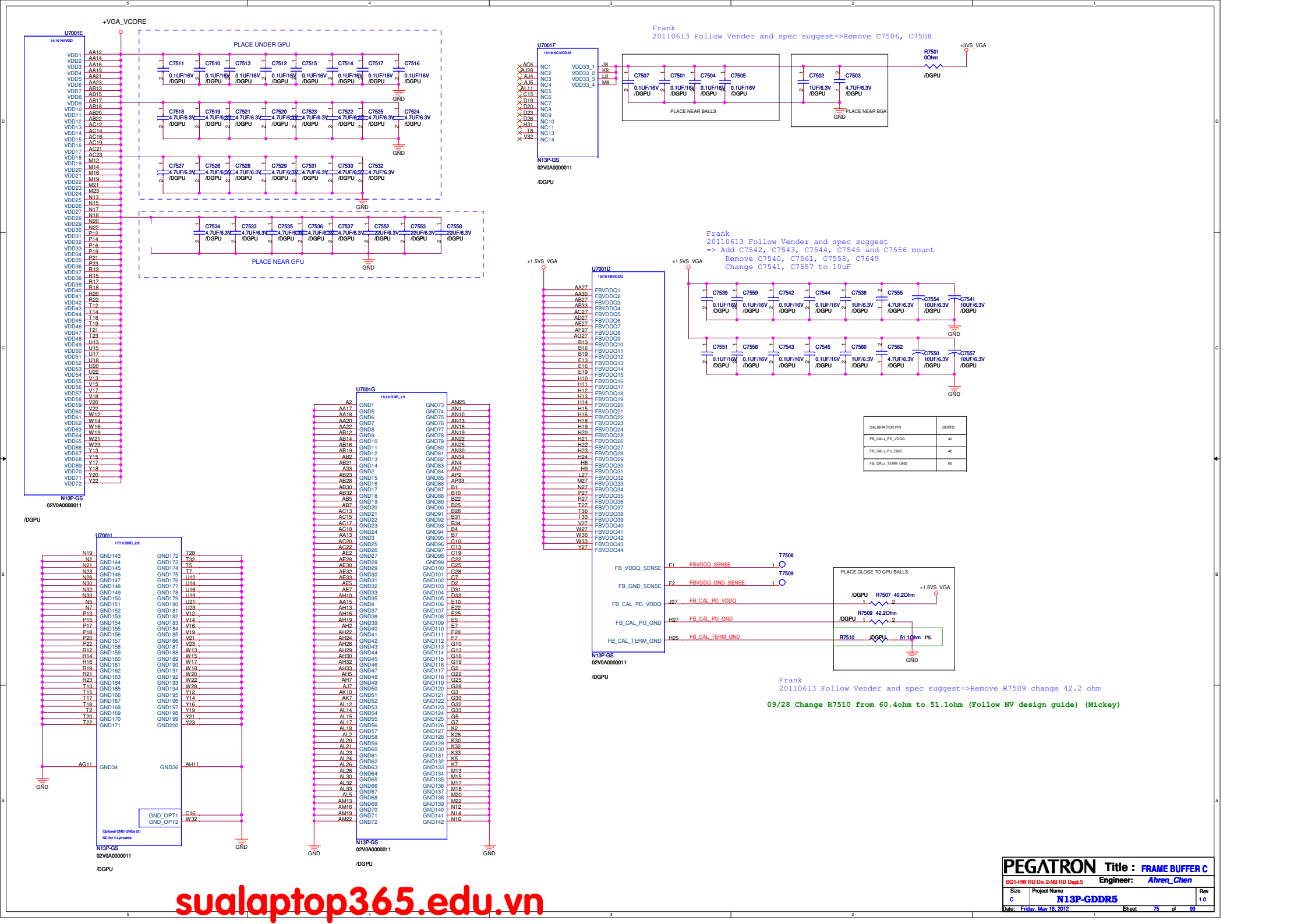


IFPX channel

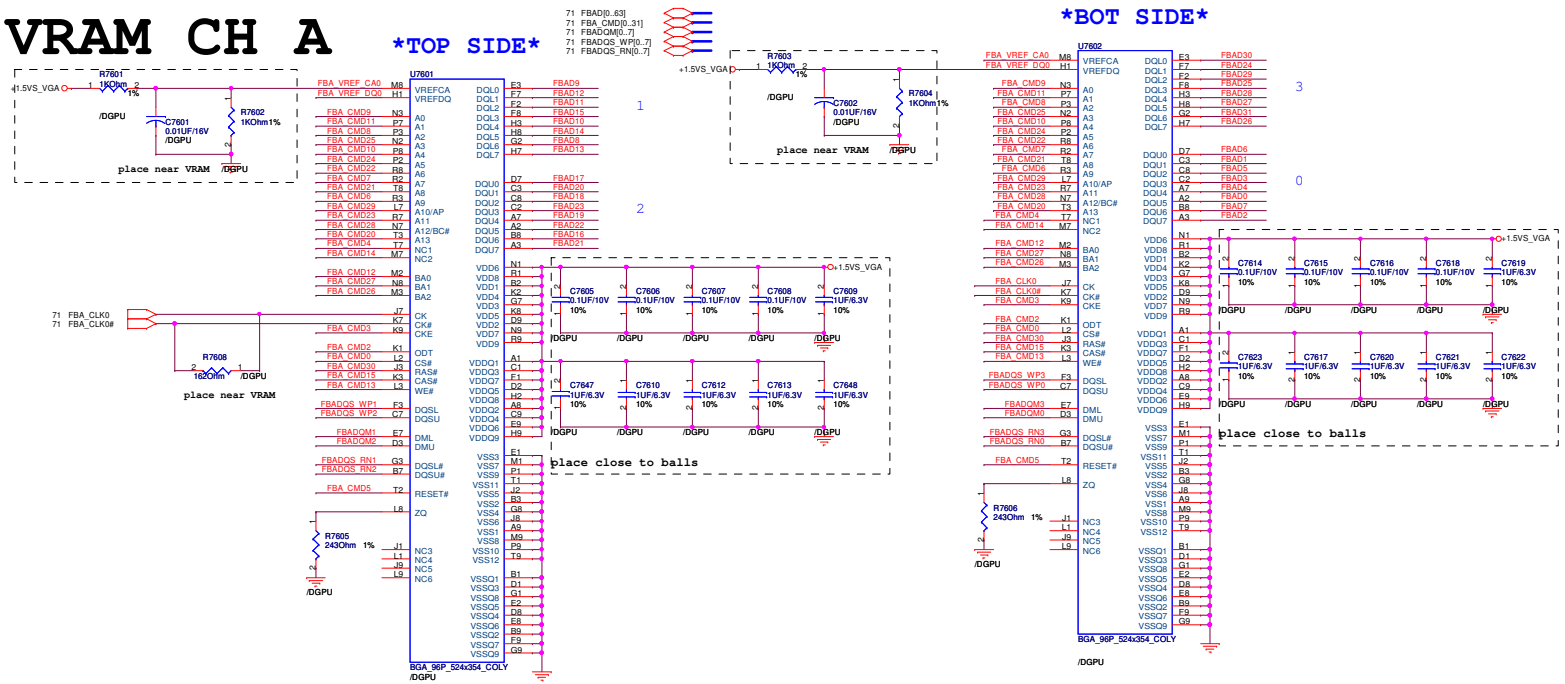
	N13M-GS	N13P-GS/N13P-GL	
IFPA/B	X	V	LVDS
IFPC	X	V	HDMI
IFPD	X	V	EDP
IFPE/F	X	V	

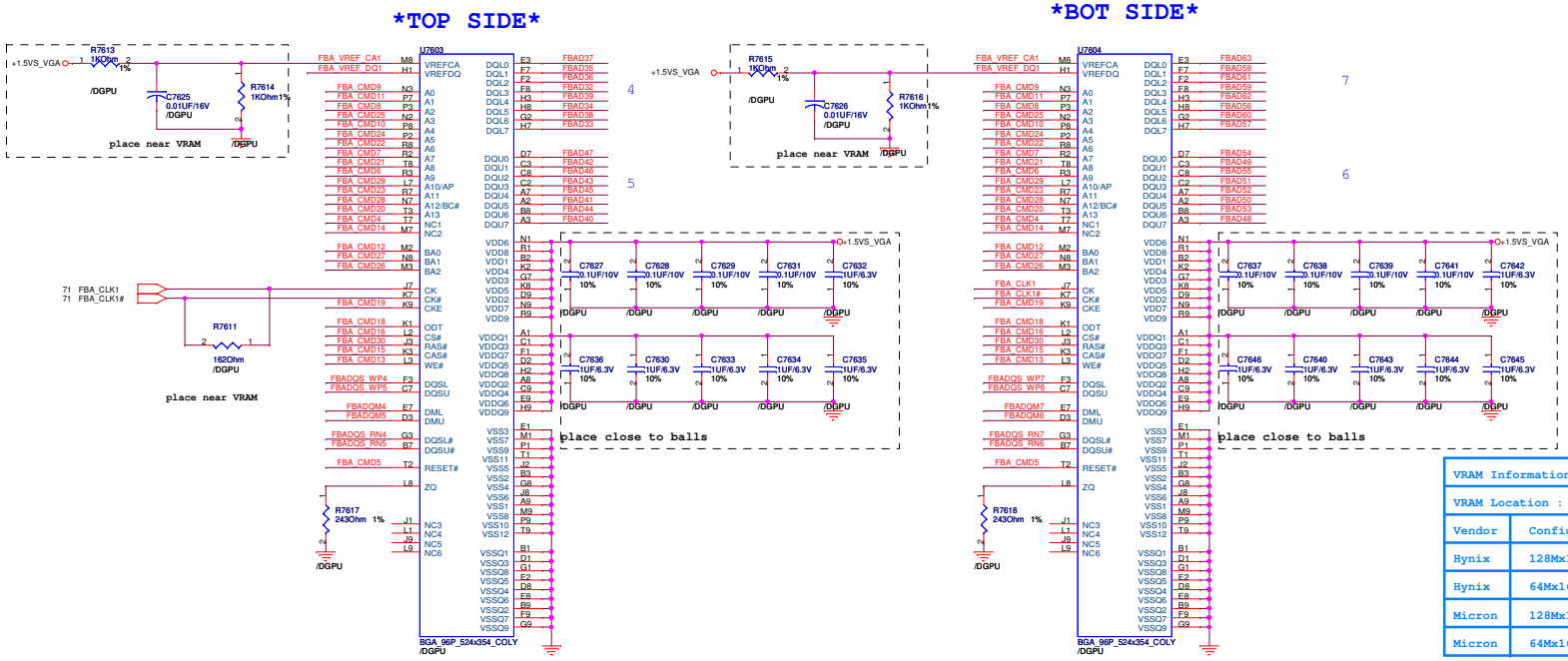
PEGATRON
PEGATRON COMPUTER INC
Title : FRAME BUFFER C
Engineer: Ahren_Chen
Size C | Project Name N13P-GDDR5 | Rev 1.0
P/N <OrgAddr2>
Date: Friday, May 18, 2012 | Sheet 73 of 99





VRAM CH A



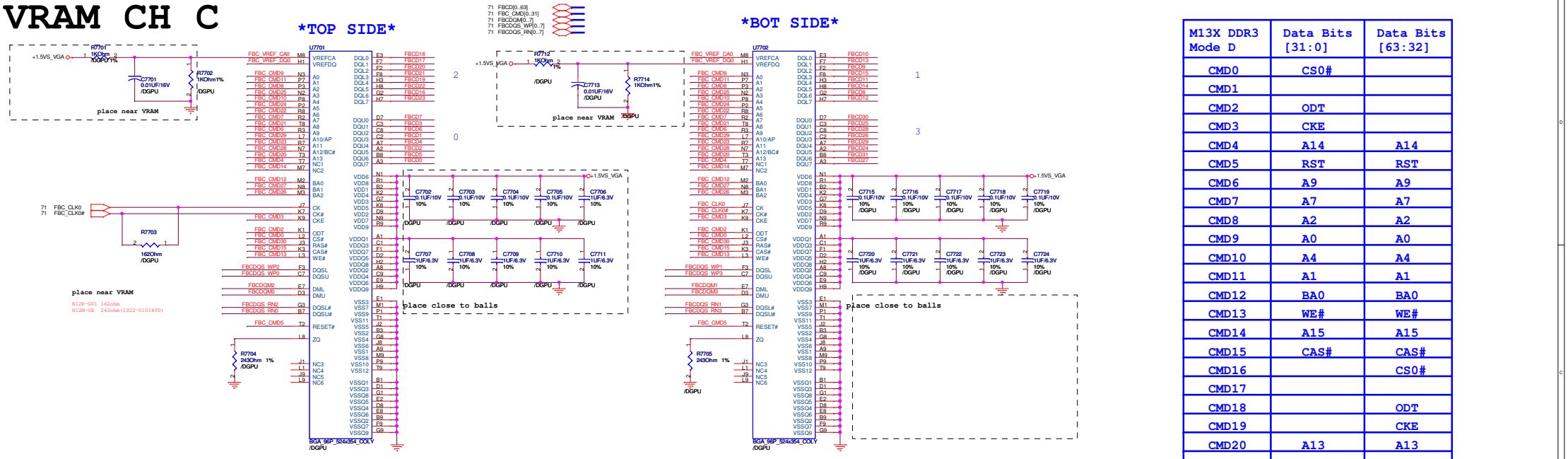


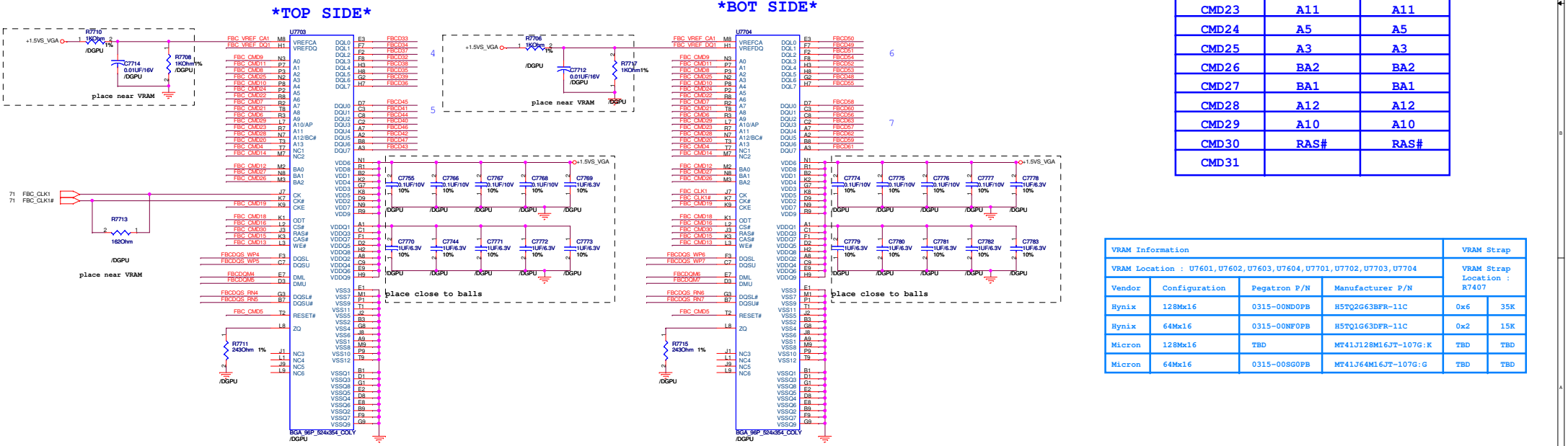
M13X DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
CMD0	CS0#	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE#	WE#
CMD14	A15	A15
CMD15	CAS#	CAS#
CMD16		CS0#
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS#	RAS#
CMD31		

VRAM Information				VRAM Strap	
VRAM Location : U7601,U7602,U7603,U7604,U7701,U7702,U7703,U7704				VRAM Strap Location : R7407	
Vendor	Configuration	Pegatron P/N	Manufacturer P/N		
Hynix	128Mx16	0315-00ND0PB	H5TQ2G63BFR-11C	0x6	35K
Hynix	64Mx16	0315-00NF0PB	H5TQ1G63DFR-11C	0x2	15K
Micron	128Mx16	TBD	MT41J128M16JT-107G:K	TBD	TBD
Micron	64Mx16	0315-00SG0PB	MT41J64M16JT-107G:G	TBD	TBD

PEGATRON Title : FRAME BUFFER A
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Ahren_chen
Size: A2 | Project Name: BOSTON G & RG | Rev: 1.0
Date: Friday, May 18, 2012 | Sheet 76 of 99

VRAM CH C





M13X DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
CMD0	CS0#	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE#	WE#
CMD14	A15	A15
CMD15	CAS#	CAS#
CMD16		CS0#
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS#	RAS#
CMD31		

VRAM Information				VRAM Strap	
VRAM Location : U7601,U7602,U7603,U7604,U7701,U7702,U7703,U7704				VRAM Strap Location : R7407	
Vendor	Configuration	Pegatron P/N	Manufacturer P/N		
Hynix	128Mx16	0315-00ND0PB	H5TQ2G63BFR-11C	0x6	35K
Hynix	64Mx16	0315-00NF0PB	H5TQ1G63DFR-11C	0x2	15K
Micron	128Mx16	TBD	MT41J128M16JT-107G:K	TBD	TBD
Micron	64Mx16	0315-00SG0PB	MT41J64M16JT-107G:G	TBD	TBD

PEGATRON Title : FRAME BUFFER B
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Ahren_chen
Size: Custom Project Name: BOSTON G & RG Rev: 1.0
Date: Friday, May 18, 2012 Sheet 77 of 99

PEGATRON

Title : Connector, LED

PEGATRON COMPUTER INC

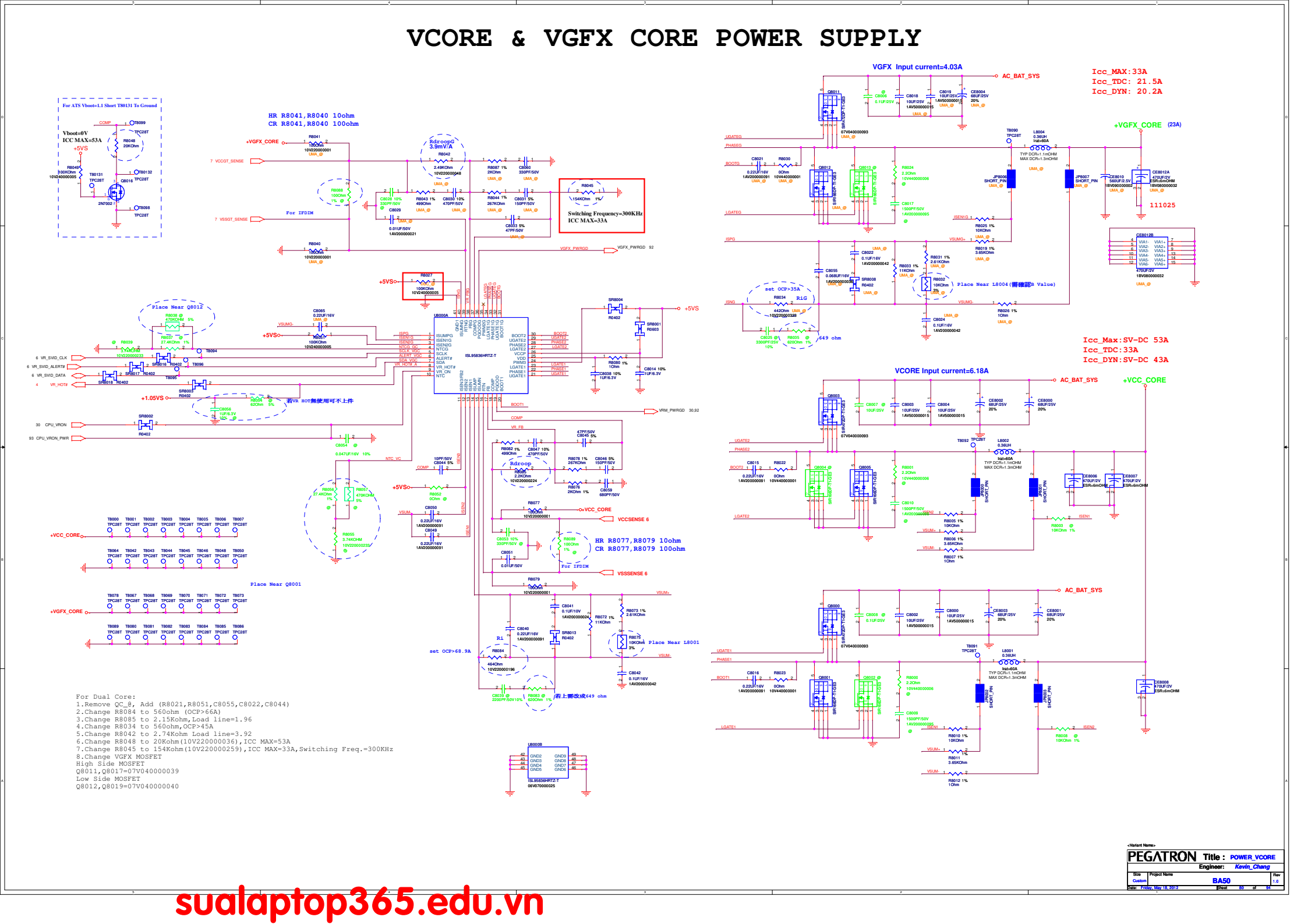
Engineer: Ahren_Chen

Size	Project Name	Rev
C	N13P-GDDR5	1.0
	P/N <OrgAddr2>	

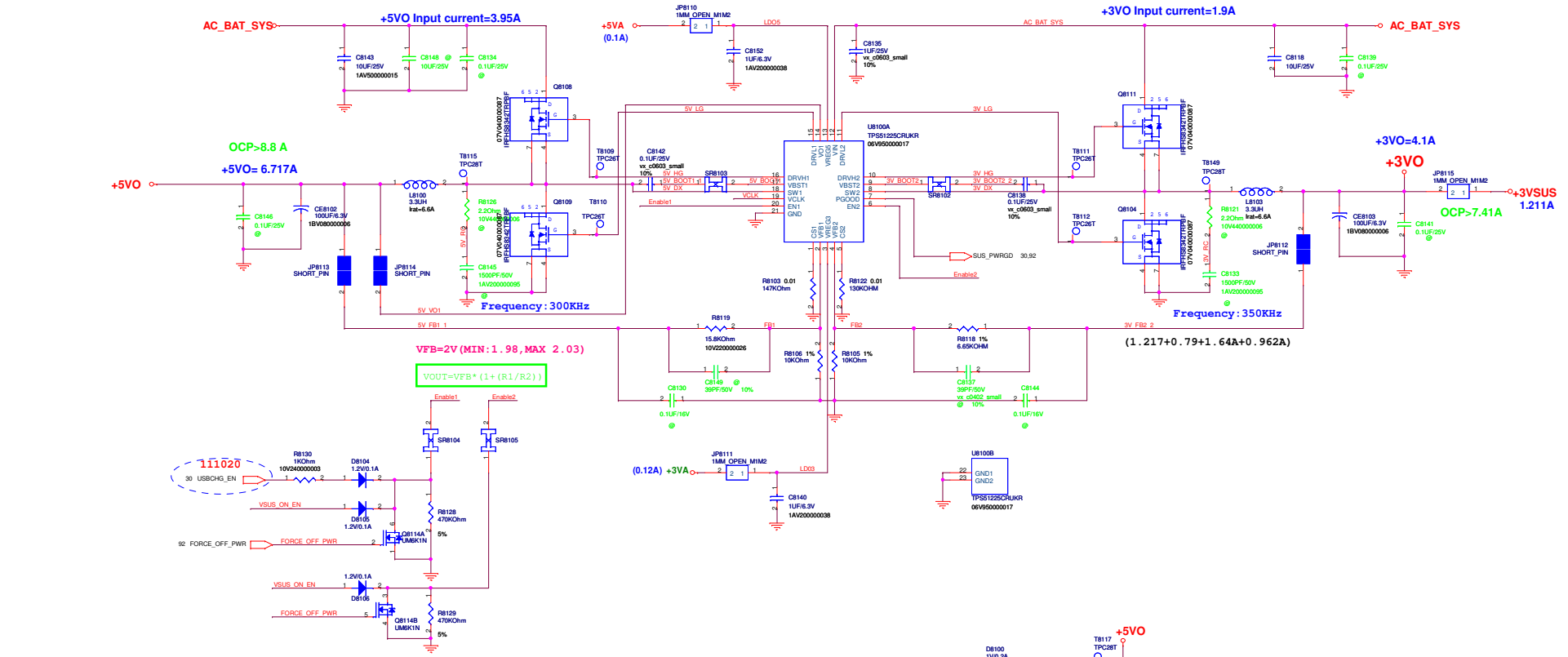
Date: Friday, May 18, 2012 Sheet 78 of 99

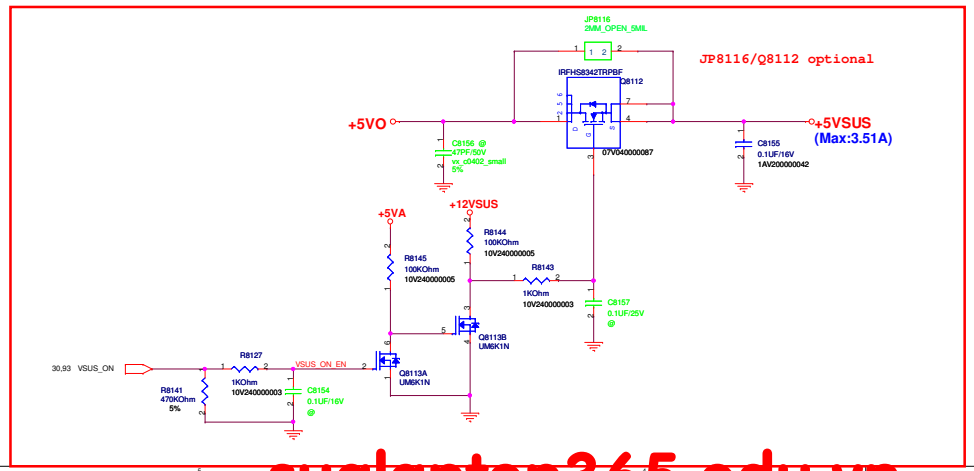
PEGATRON	Title : GPU PWR/GND		
PEGATRON COMPUTER INC	Engineer: Ahren_Chen		
Size: C	Project Name: N13P-GDDR5		Rev: 1.0
	P/N: <OrgAddr2>		
Date: Friday, May 18, 2012	Sheet 79 of 99		

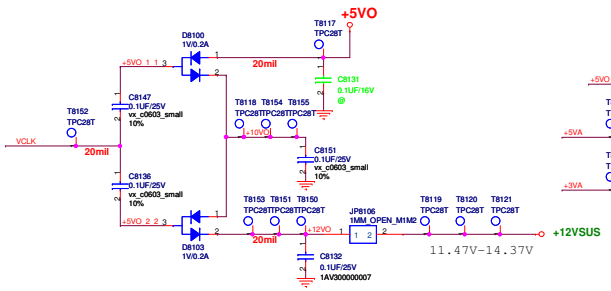
VCORE & VGFX CORE POWER SUPPLY



+5VO & +3VO POWER SUPPLY



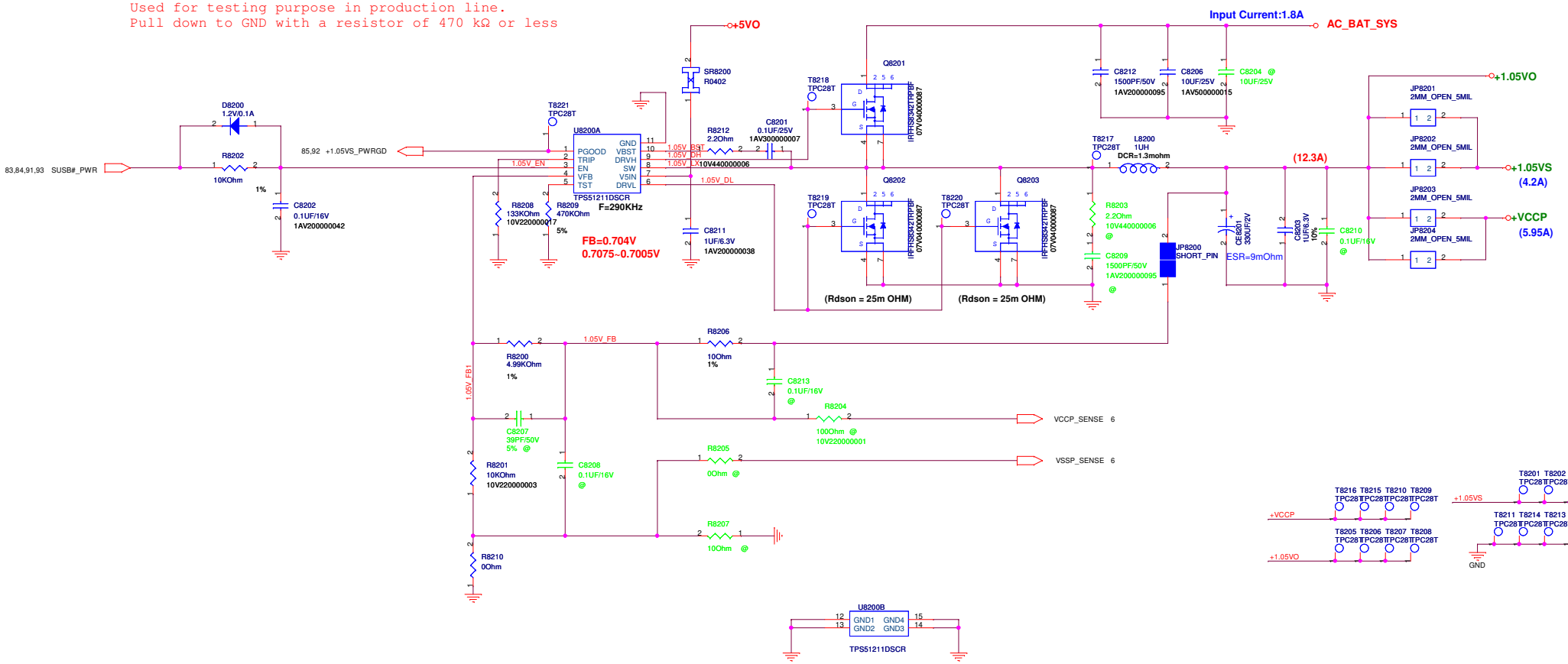




VCCP&+1.05VS POWER SUPPLY

TRIP V (mV) = TRIP R (k) * TRIP I (mA)
TRIPI current, which is 10uA
VOCP = TRIP V / (8 / Rdson) + (I ripple / 2)

Used for testing purpose in production line.
Pull down to GND with a resistor of 470 kΩ or less



<Variant Name>

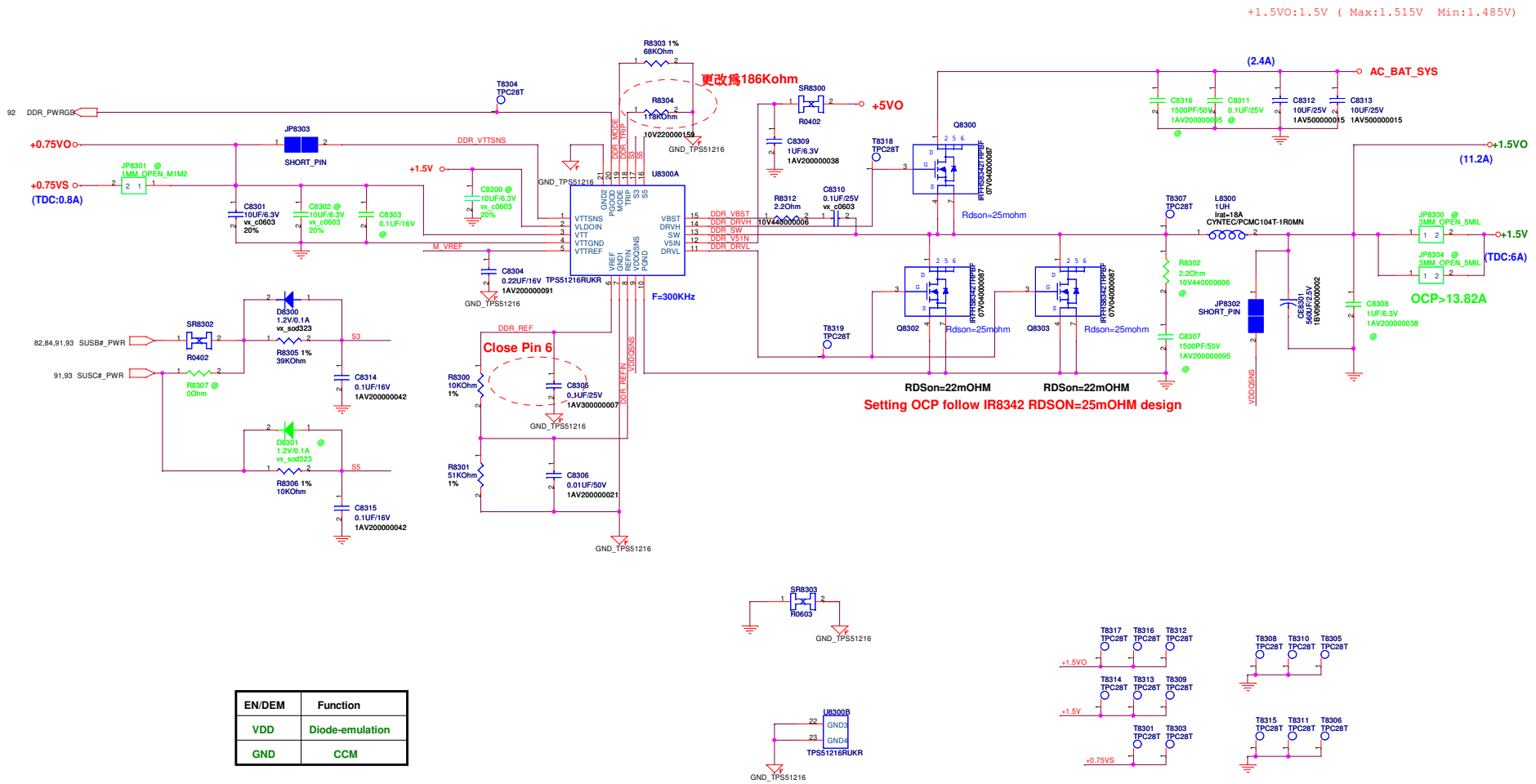
PEGATRON Title : POWER_VCCP

Engineer:

Size	Project Name	Rev
Custom	BA50	1.1

Date: Friday, May 18, 2012 Sheet 82 of 94

DDR & VTT POWER SUPPLY



EN/DEM	Function
VDD	Diode-emulation
GND	CCM

<Variant Name>

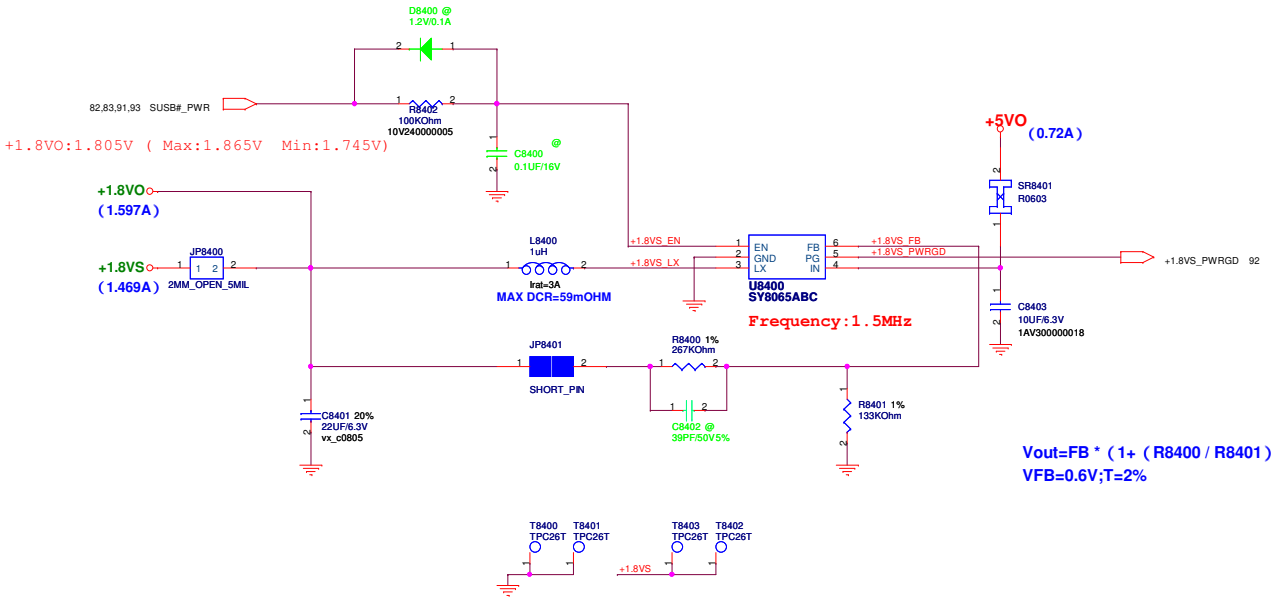
PEGATRON Title : POWER_DDR & VTT

Engineer: Kevin_Chang

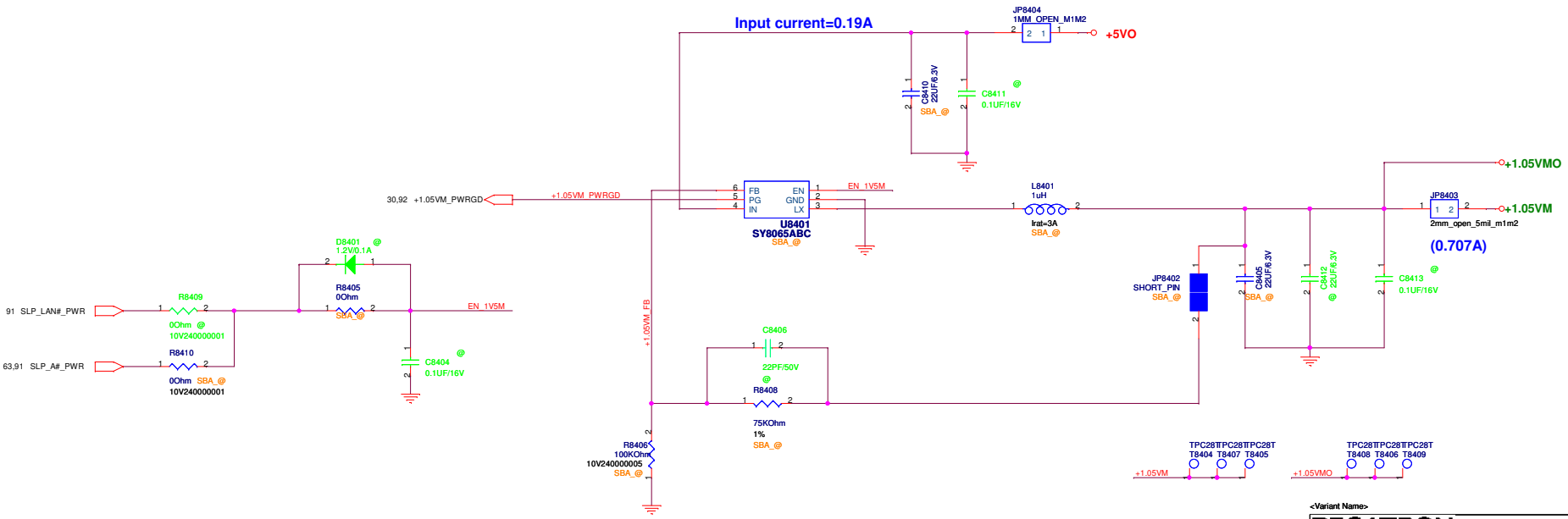
Size	Project Name	Rev
Custom	BA50	1.0

Date: Friday, May 18, 2012 Sheet 83 of 94

1.8VS POWER SUPPLY



+1.05VM POWER SUPPLY



<Variant Name>

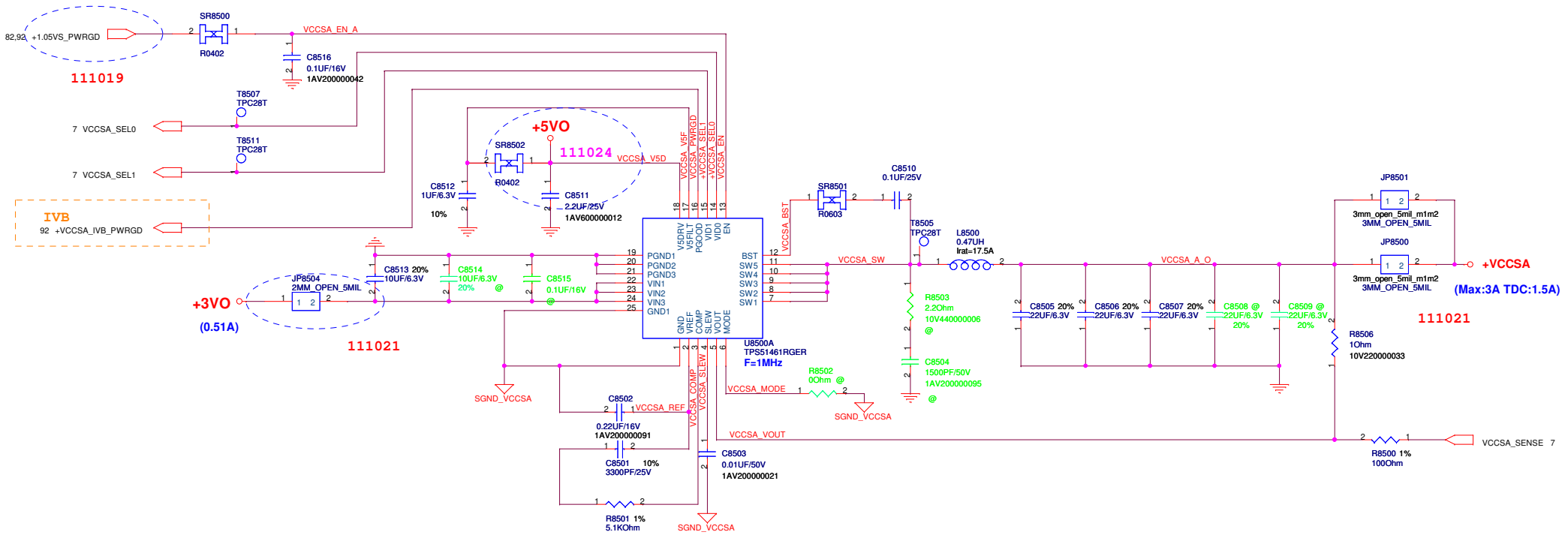
PEGATRON Title : POWER_1.8VS

Engineer: Kevin_Chang

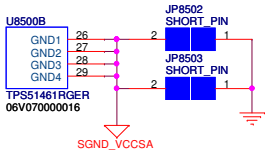
Size	Project Name	Rev
Custom	BA50	1.0

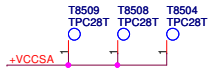
Date: Friday, May 18, 2012 Sheet 84 of 94

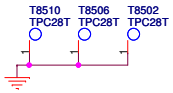
IVB VCCSA POWER SUPPLY



+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V







<Variant Name>

PEGATRON Title : POWER_VCCSA

Engineer: Kevin_Chang

Size	Project Name	Rev
Custom	BA50	1.0

Date: Friday, May 18, 2012 Sheet 85 of 94

VGA_CORE POWER SUPPLY

VID Set 0.9V,For N13M-GS & N13P-GS. 2011/09/30

For N13P-GL,VID Set 0.975V, Mount R8764 R8770 R8771, Unmount R8781 R8763 R8786 2011/10/25

R8703=(Period(us)-0.29)*2.65
Period(us)=1/300KHz

R8706 Setting OCP

VGA Input current=5.6A

+VGA_VCORE
TDC=40A

VGA_DPRSLPVR	VGA_PSI#	VO_action
L	L	1 Phase CCM
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE

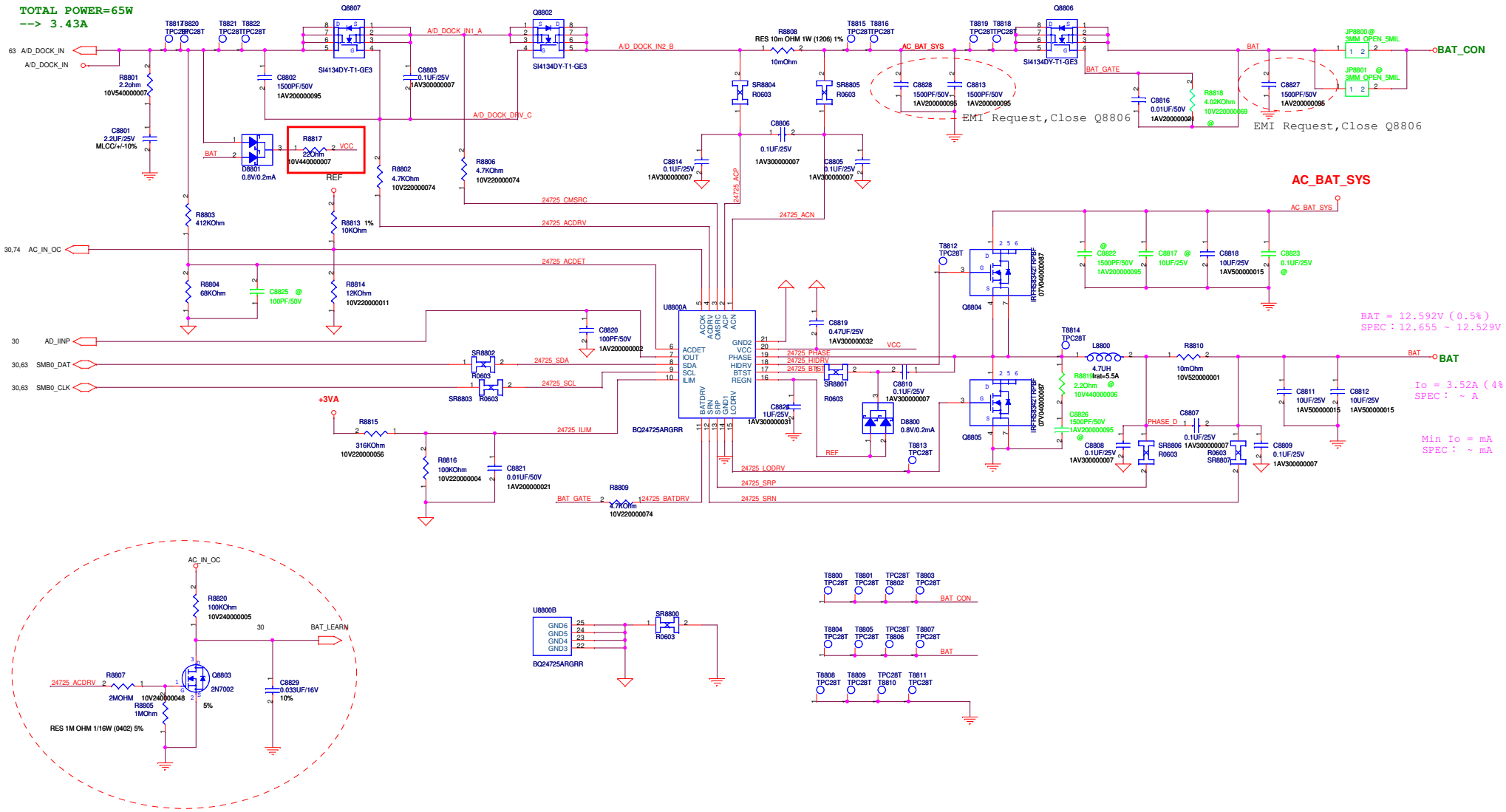
<Variant Name>

PEGATRON Title : POWER_VGACORE
Engineer: Kevin_Chang

Size	Project Name	Rev
Custom	BA50	1.0

Date: Friday, May 18, 2012 Sheet 87 of 99

BATTERY CHARGER



<Variant Name>

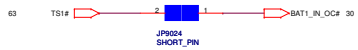
PEGATRON Title : POWER_CHARGER

Engineer: Kevin_Chnag

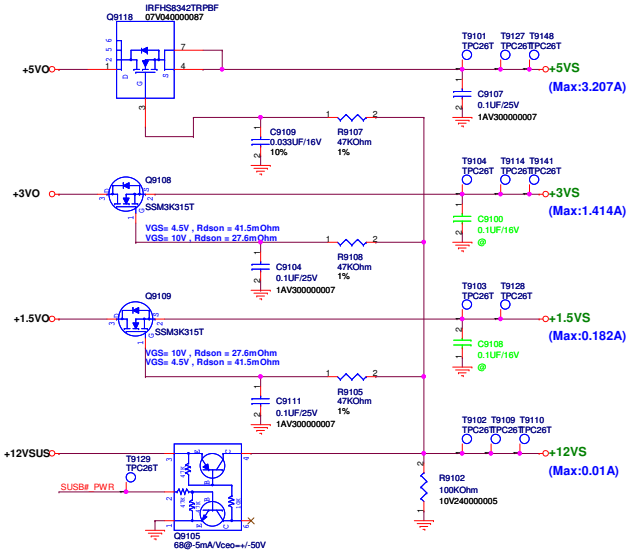
Size	Project Name	Rev
Custom	BA50	1.0

Date: Friday, May 18, 2012 Sheet 88 of 15

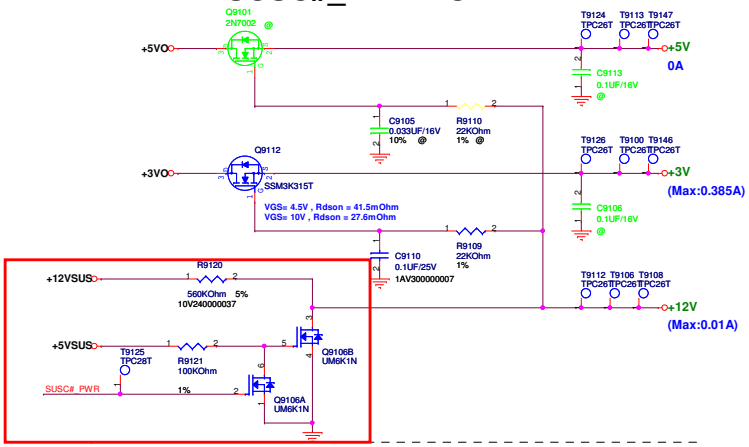
BATTERY IN DETECT



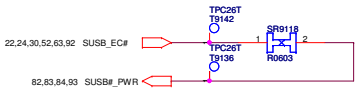
SUSB#_PWR POWER

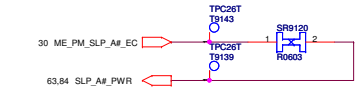


SUSC#_PWR POWER

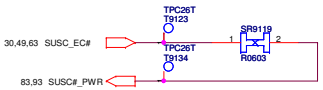


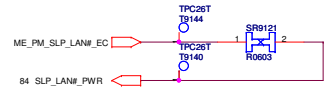
SUSB#_PWR POWER Control



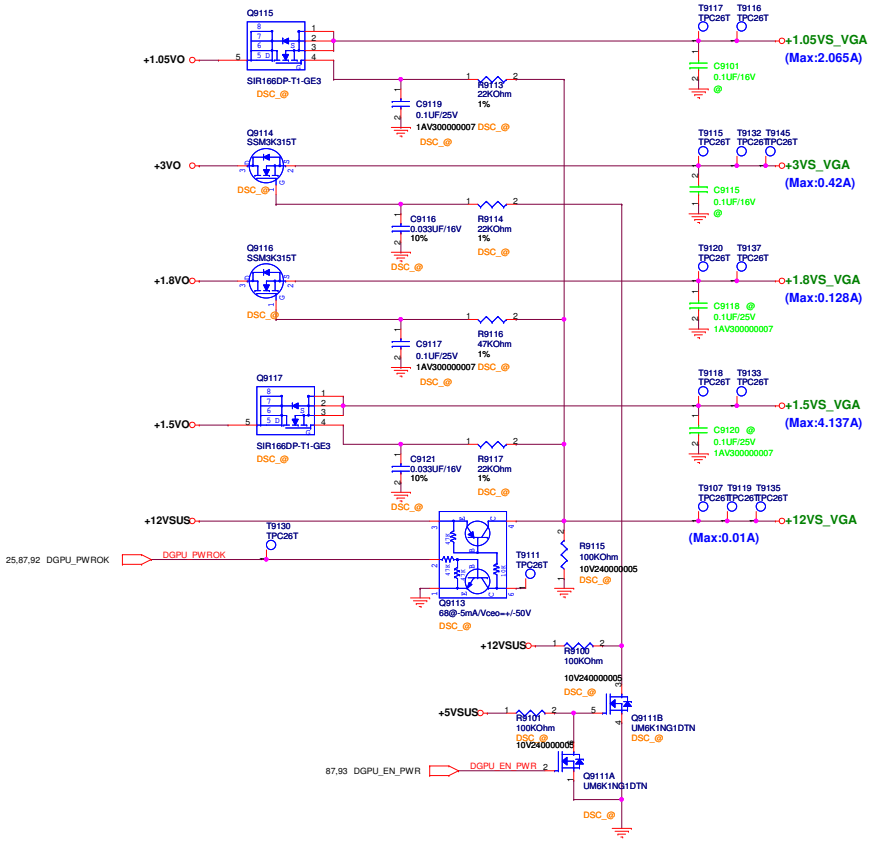


SUSB#_PWR POWER Control

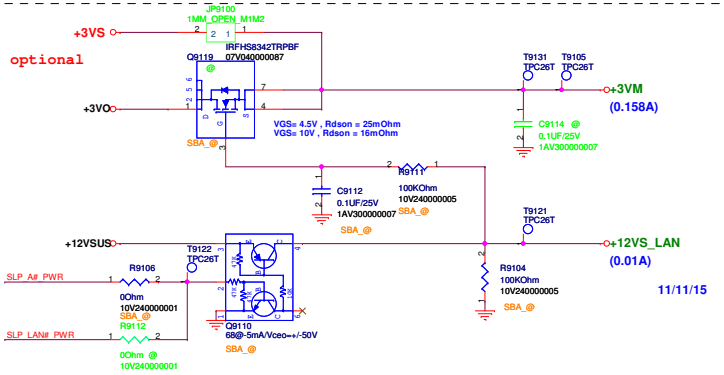




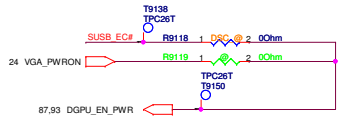
DSC#_PWR POWER(dGPU)



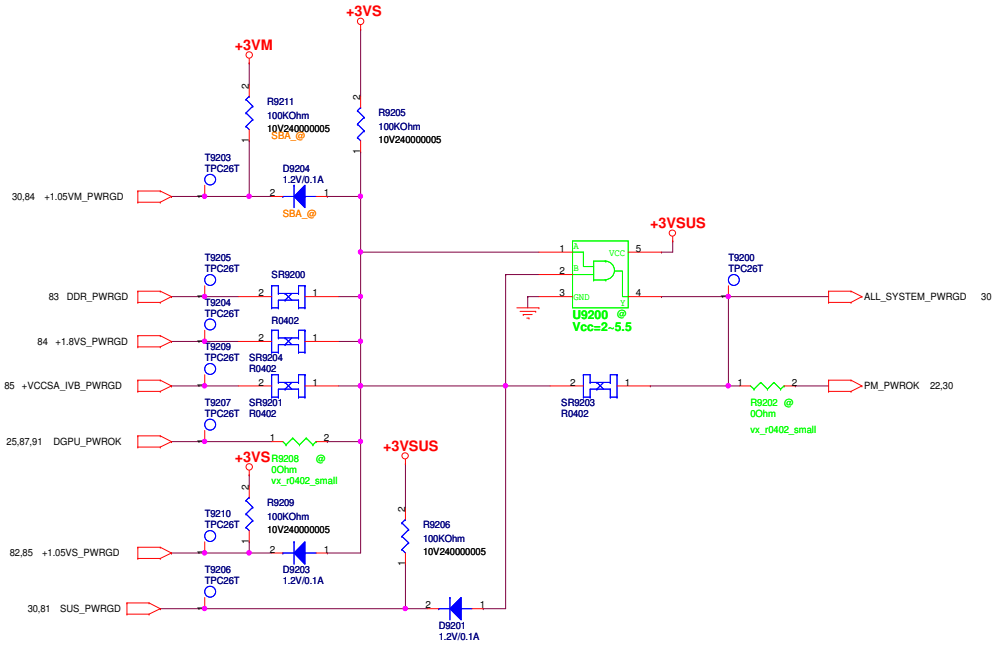
JP9100/Q9119 optional

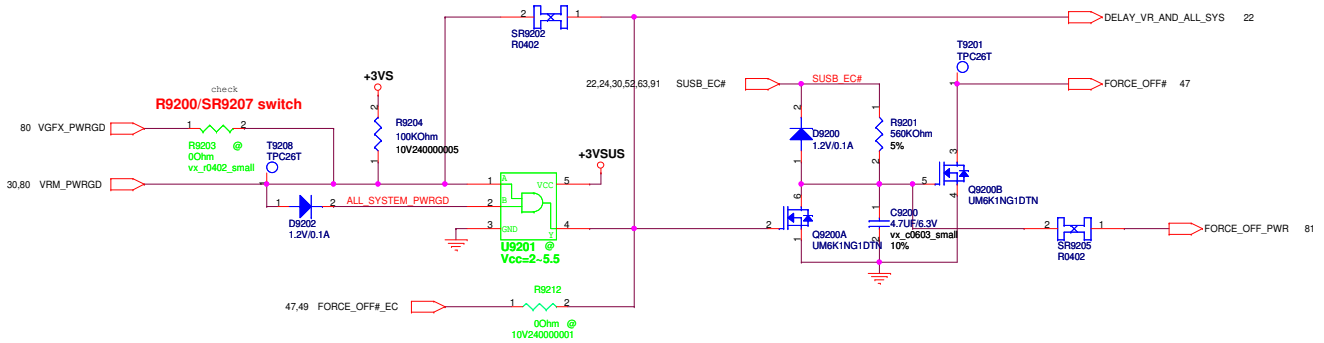


DSC_VGA_PWR POWER Control



POWER GOOD DETECTER





<Variant Name>

PEGATRON Title : POWER_PROTECT

Engineer: Kevin_Chang

Size	Project Name	Rev
Custom	BA50	1.0

Date: Friday, May 18, 2012 Sheet 92 of 94

AC_BAT_SYS → AC_BAT_SYS 37,80,81,82,83,87,88

BAT_CON → BAT_CON 63,88

+5VA → +5VA 30,41,49,66,81

+3VA → +3VA 20,27,30,48,63,81,88

+5VAO → +5VAO

+5VO → +5VO 61,81,82,83,84,85,91

+3VO → +3VO 81,85,91

+1.8VO → +1.8VO 84,91

+1.5VO → +1.5VO 83,91

+1.05VO → +1.05VO 82,91

+12VSUS → +12VSUS 22,28,33,37,41,55,60,62,81,91

+5VSUS → +5VSUS 22,27,30,60,65,66,81,91

+3VSUS → +3VSUS 4,22,24,27,28,30,33,37,41,55,62,81,92

+12V → +12V 52,91

+5V → +5V 63,91

+3V → +3V 4,24,37,51,52,62,63,65,91

+1.5V → +1.5V 5,7,16,17,18,63,83

+12VS → +12VS 28,39,91

+5VS → +5VS 27,30,38,39,41,48,49,60,63,66,80,87,91

+3VS → +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,51,52,55,60,62,63,65,66,69,91,92

+1.8VS → +1.8VS 7,25,26,63,84

+1.5VS → +1.5VS 26,52,55,63,91

+1.05VS → +1.05VS 26,27,63,80,82,87

+0.75VS → +0.75VS 16,17,63,83

+VCCSA → +VCCSA 7,85

+VCCIO → +VCCIO

+VCCP → +VCCP 3,4,6,7,25,26,27,47,63,82

+12VS_VGA → +12VS_VGA 91

+3VS_VGA → +3VS_VGA 63,70,72,73,74,75,87,91

+1.5VS_VGA → +1.5VS_VGA 63,71,75,76,77,91

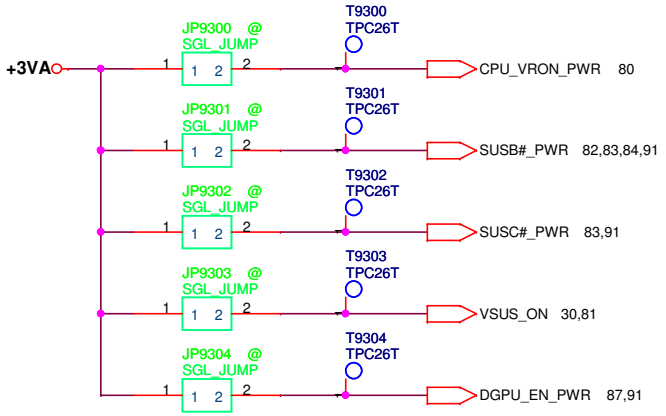
+1.05VS_VGA → +1.05VS_VGA 63,70,71,72,73,91

+VGA_VCORE → +VGA_VCORE 63,75,87

+VGFX_CORE → +VGFX_CORE 7,63,80

+VCC_CORE → +VCC_CORE 6,63,80

FOR POWER TEST



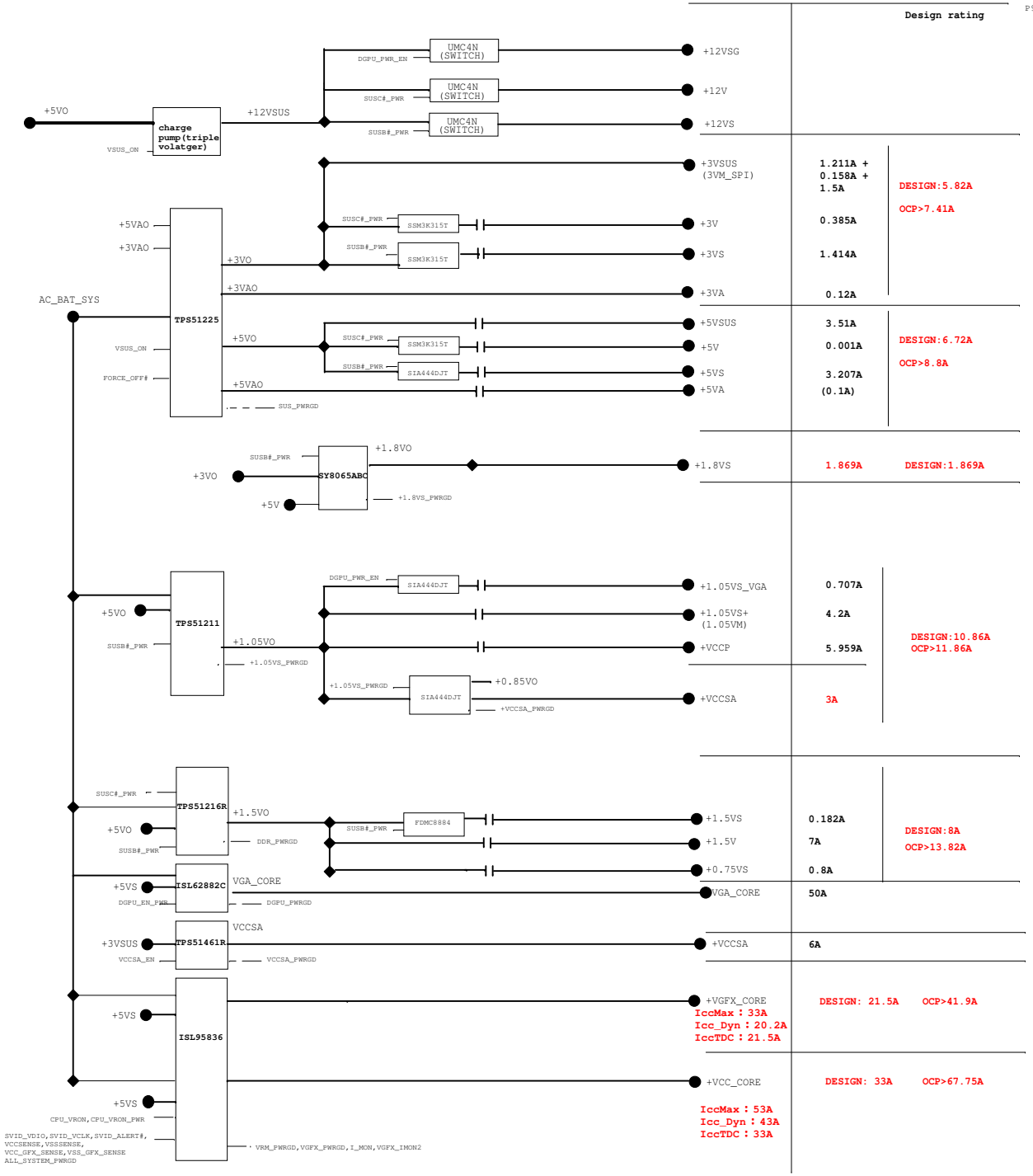
<Variant Name>

PEGATRON Title : POWER_SIGNAL

Engineer: Kevin_Chang

Size	Project Name	Rev
Custom	BA50	1.0

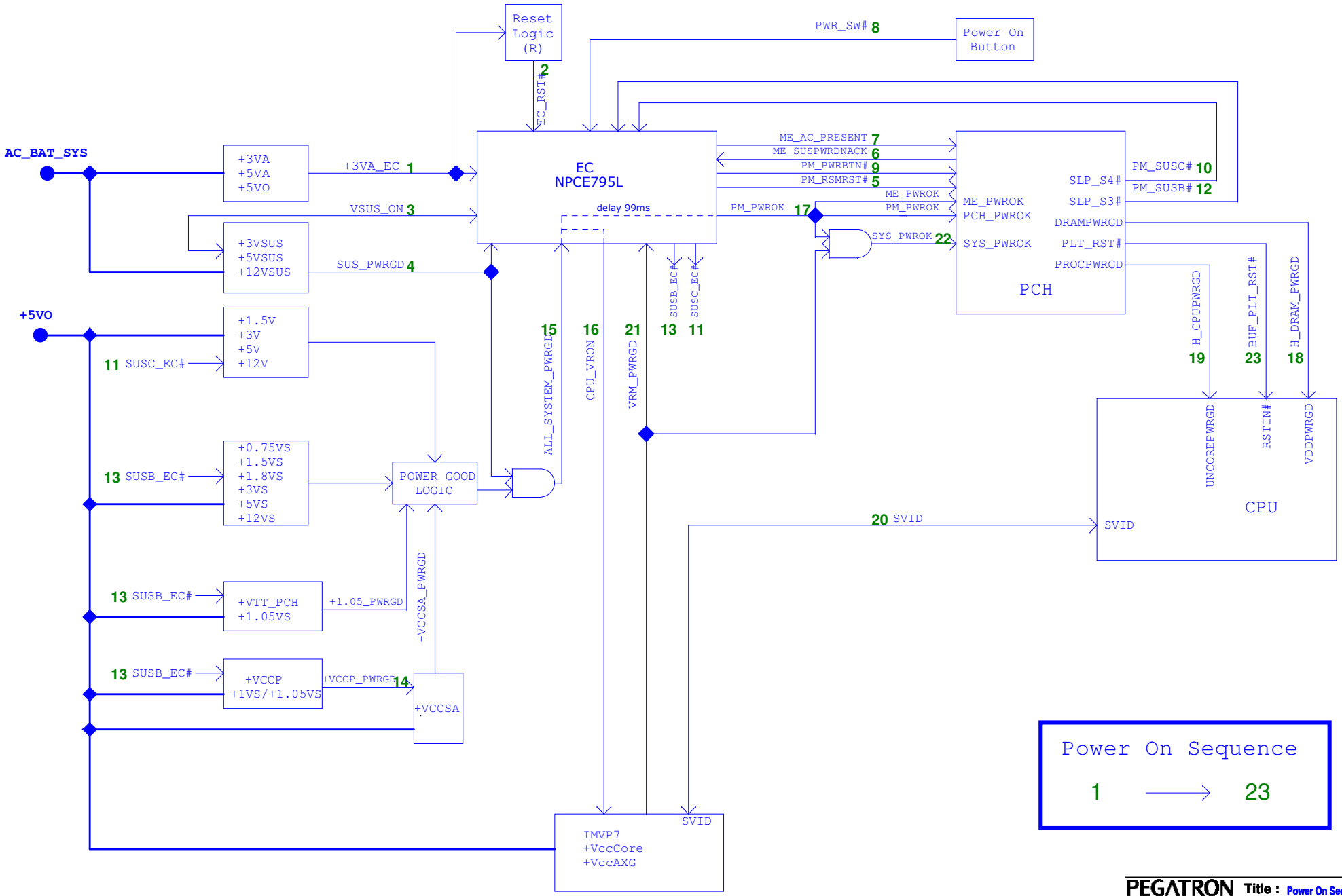
Date: Friday, May 18, 2012 Sheet 93 of 94



PEGATRON	Title : ****	
BG1\HW1	Engineer: *Ivan Liu*	
Size: A	Project Name: **H36HC**	Rev: 1.0
Date: Friday, May 18, 2012	Sheet 96 of 99	

PEGATRON	Title : ****	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.0
Date: Friday, May 18, 2012	Sheet 97 of 99	

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



PEGATRON Title : Power On Sequence
<OrgName> Engineer: JAY TSAI
Size C | Project Name EIH31 | Rev 1.0
Date: Friday, May 18, 2012 | Sheet 98 of 99

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)

PEGATRON	Title : Power On Timing	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.0
Date: Friday, May 18, 2012	Sheet 99 of 99	