ZZZ PCB@

PCB 1G7 LA-D822P REV0 M/B UMA
DA80017E000

Compal Confidential

Dali & Astro
BKA40/BKA50/BKD40/BKD50
MB Schematic Document

LA-D822P
Rev: 1.0 (A00)
2016.06.06

UC1 KBL_15W_I3@
SA0000A382L
KBL_U_SR2VN
S IC FJ8067702739738 SR2VN H0 2.4G A31!

UC1 KBL_15W_I5@
SA0000A372L
KBL_U_SR2VL
S IC FJ8067702739739 SR2VL H0 2.5G A31!

UC1 KBL_15W_I7@
SA0000A342L
KBL_U_SR2VM
S IC FJ8067702739740 SR2VM H0 2.7G A31!

UC1 KBL_15W_2+1@
SA00009QM0L
KBL_U_QKKQ
S IC A31 FJ8067702739920 QKKQ G0 1.7G

UC1 KBL_15W_2+2@
SA00009PJ0L
KBL_U_QKKS
S IC A31 FJ8067702739720 QKKS G0 2.4G

UC1 SKL_15W@
SA000092N4L
SKL_U_I3-6100U
S IC FJ8066201931104 SR2EU D1 2.3G A31!

Compal Electronics, Inc.

Title	Cover Page	
Size	Document Number: LA-D822P	Rev: 1.0
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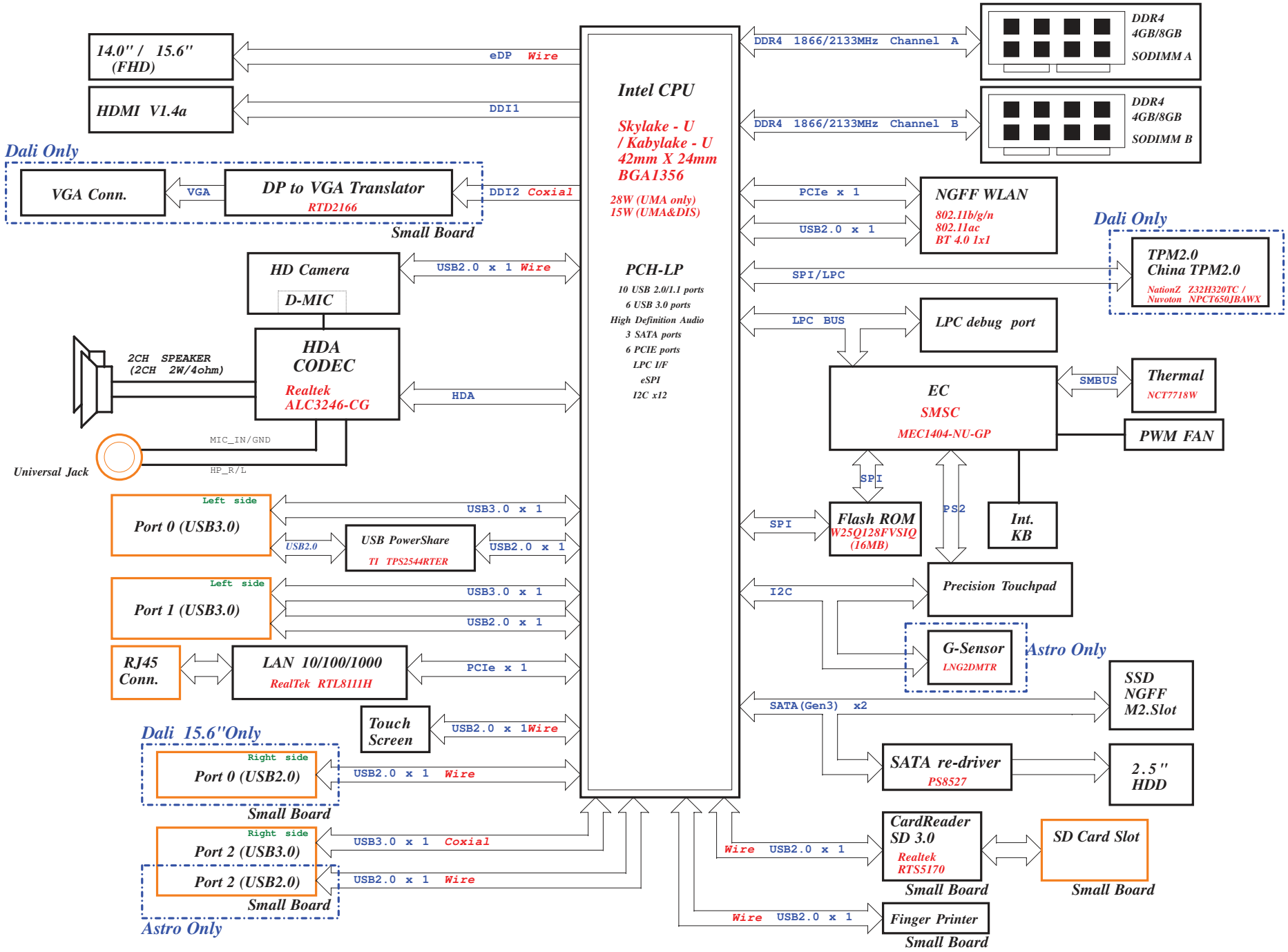

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: Block Diagram			
Size: Custom	Document Number: LA-D822P		Rev: 1.0
Date: Monday, June 06, 2016	Sheet 2 of 46		

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+RTC_CELL +RTC_VCC +3VLP +19VB	+1.0V_PRIM +1.0V_MPHYPLL +5VALW +3VALW +3.3V_ALW_DSW +1.8V_PRIM	+1.0V_VCCST +1.2V_DDR +2.5V_MEM +3VALW_PCH	+1.0VS_VCCIO +1.0V_VCCSTG +VCC_GT +VCC_SA +VCC_CORE +GPU_CORE +5VS +3VS +1.8VS +0.6V_DDR_VTT
S0	ON	ON	ON	ON
S3	ON	ON	ON	OFF
S4&S5 / AC	ON	ON	OFF	OFF
S4&S5 / DC	ON	OFF	OFF	OFF

Board ID & Model ID table

Item	Pull-down(K ohm)	Pull-up (K ohm)	Voltage	Board ID/Model ID
1	100	10.0	3.000	EVT(X00)
2	100	13.7	2.902	DVT1(X01)
3	100	17.8	2.801	DVT2(X02)
4	100	22.1	2.703	Pilot(A00)
5	100	27.0	2.598	
6	100	32.4	2.492	
7	100	37.4	2.402	
8	100	49.9	2.201	
9	100	57.6	2.094	
10	100	64.9	2.001	
11	100	73.2	1.905	
12	100	82.5	1.808	
13	100	93.1	1.709	
14	100	107.0	1.594	

USB PORT#	DESTINATION
1	USB3.0 Port0
2	USB3.0 Port1
3	USB3.0 Port2 (IO Board)
4	USB2.0 Port0
5	HD CAM
6	Card Reader
7	Touch Screen
8	BT
9	Finger Printer
10	N/A

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				USB3.0 Port0
USB3.0-2	SSIC-1			USB3.0 Port1
USB3.0-3	SSIC-2			USB3.0 Port2 (IO Board)
USB3.0-4				N/A
USB3.0-5		PCIE-1		N/A
USB3.0-6		PCIE-2		N/A
		PCIE-3		N/A
		PCIE-4		N/A
		PCIE-5		WLAN
		PCIE-6		GLAN
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	N/A
		PCIE-9		N/A
		PCIE-10		N/A
		PCIE-11	SATA-1*	N/A
		PCIE-12	SATA-2	SATA SSD

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Title: Notes List

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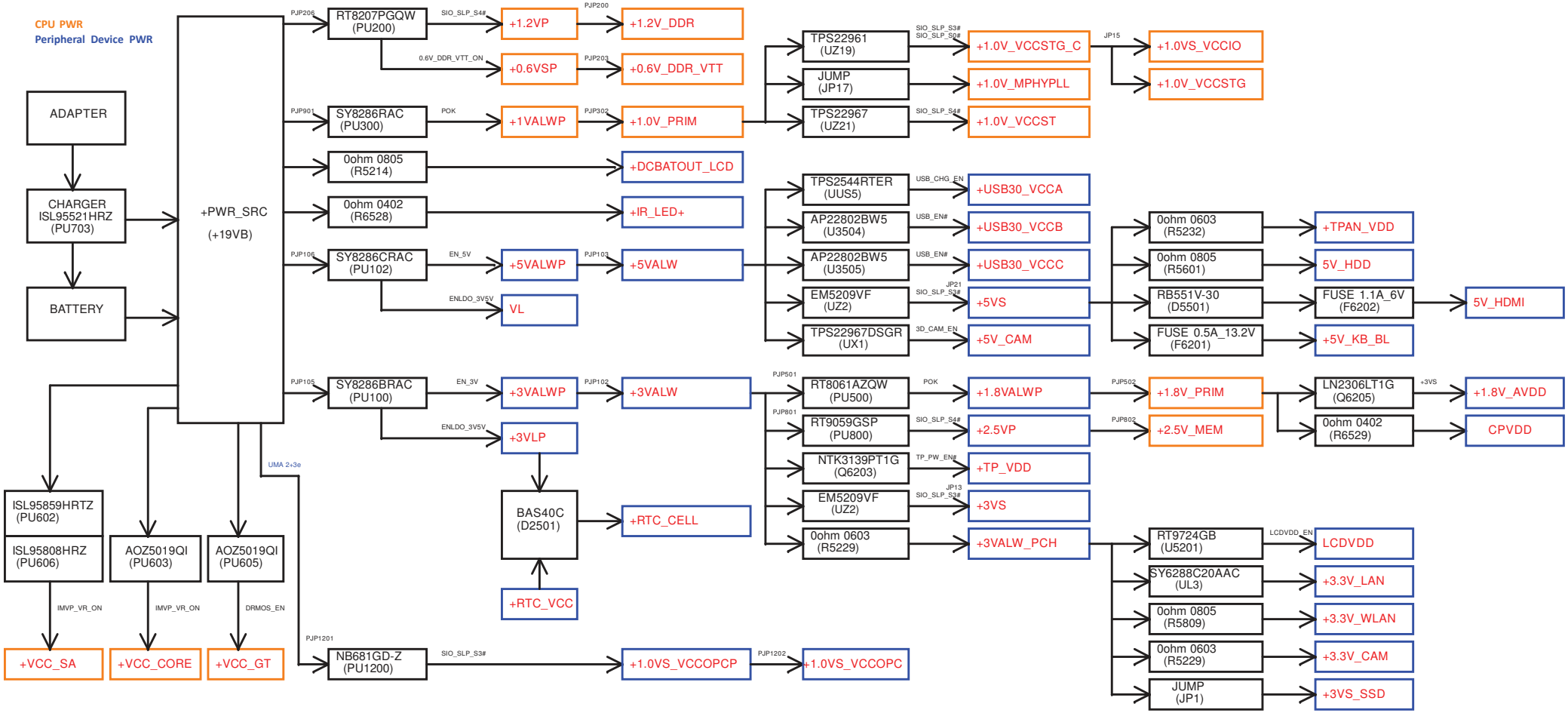

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Title: Power Rail

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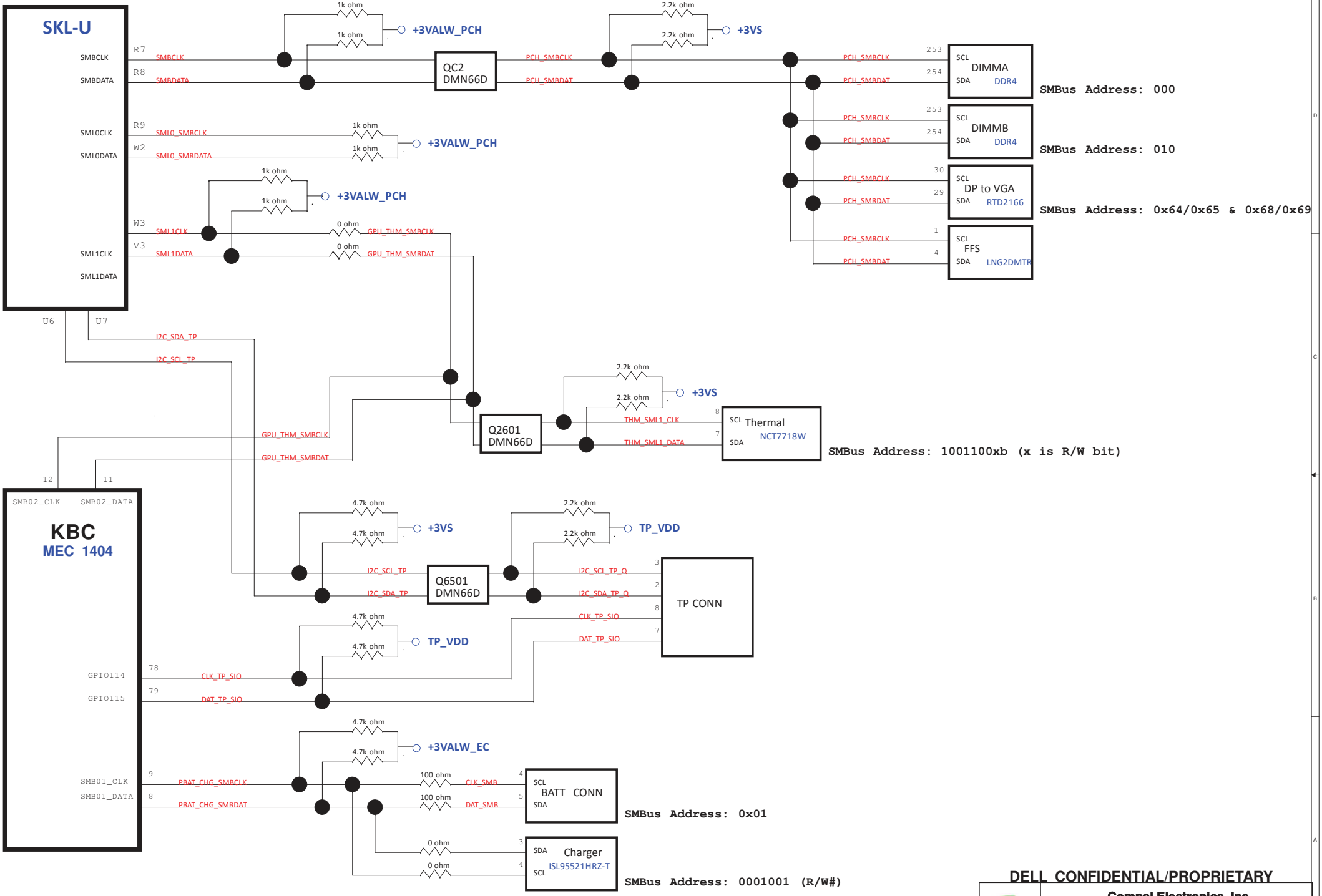

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Title: SMBus Block Diagram

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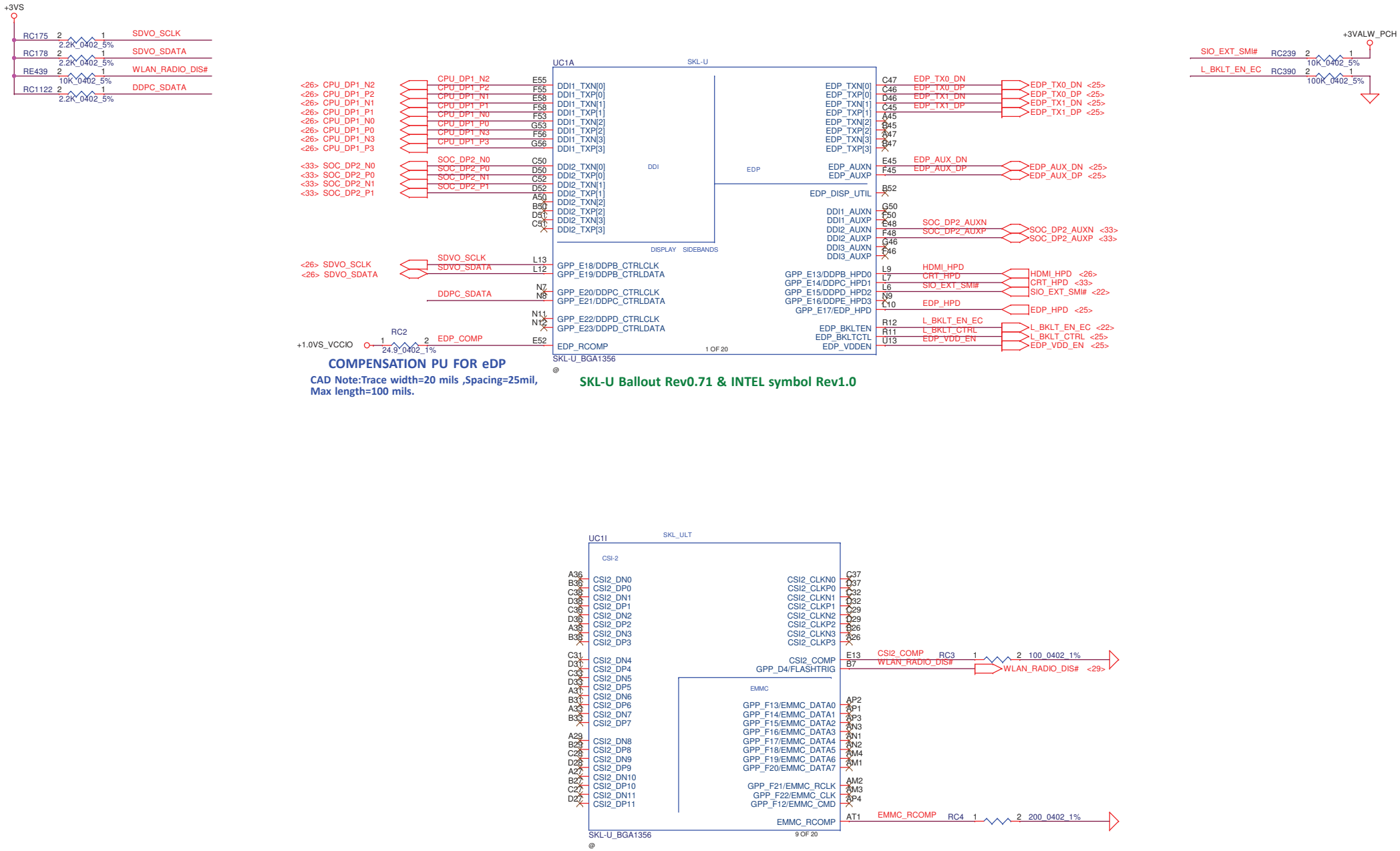

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Title: MCP(1/14)DDI,EDP,CSI2,EMMC

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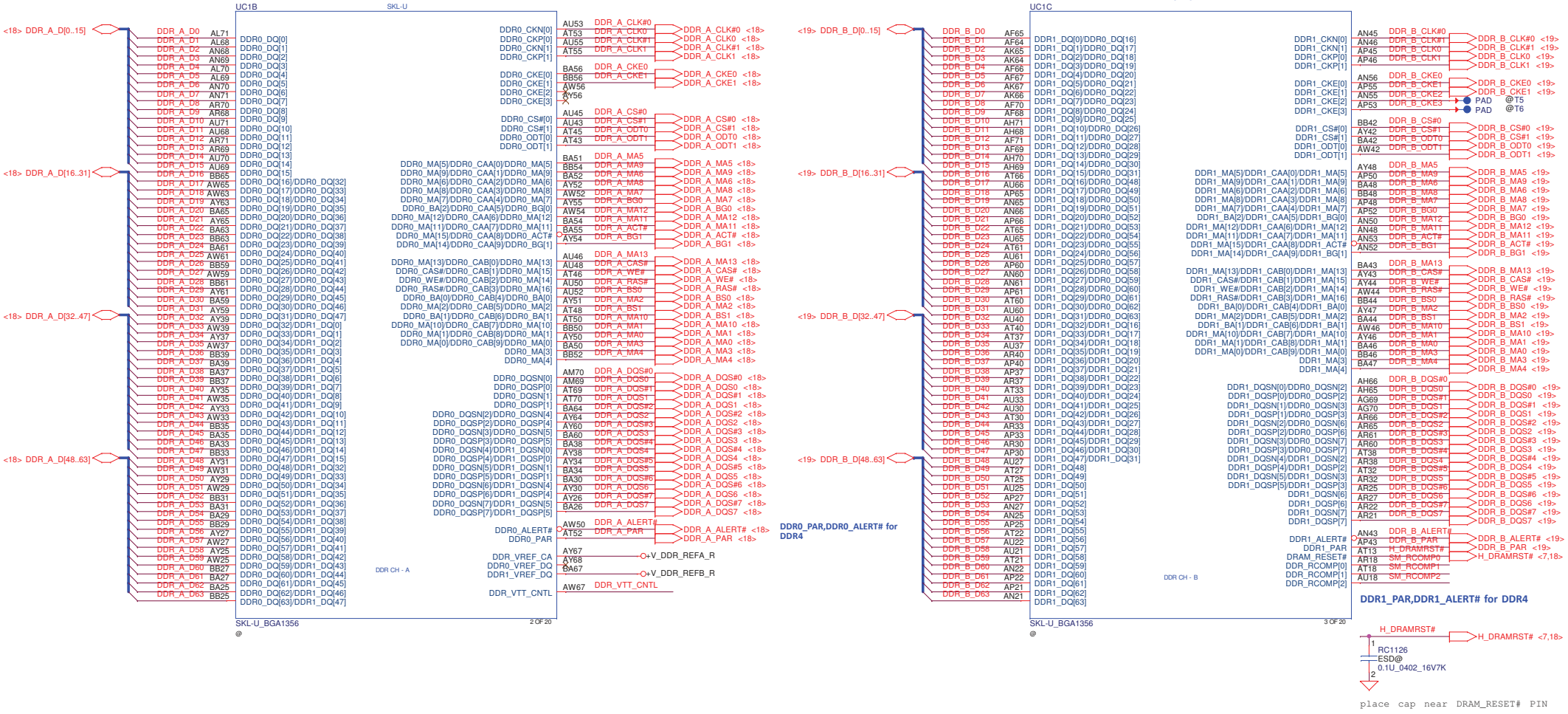
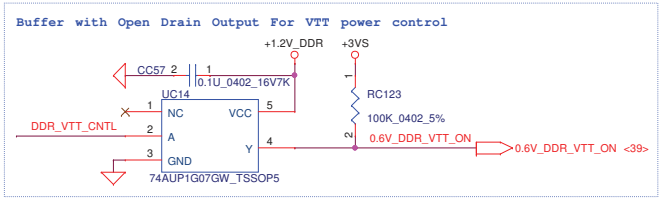
DDR4, Ballot for B2B(Interleave)

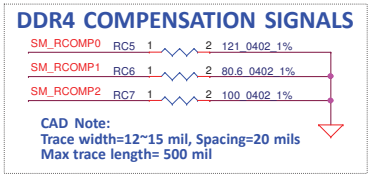


H_DRAMRST# → H_DRAMRST# <7,18>

RC1126 ESD@ 0.1U_0402_16V7K

place cap near DRAM_RESET# PIN





Compal Electronics, Inc.

Title: MCP(2/14)DDR4

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SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

SML1 -> EC,DGPU,THM

SMB -> DDR,CRT,FFS

Single SPI ROM_CS0#

16M SPI ROM (Confirmed by BIOS RD)

Layout need meet L1 = L2 = L3

Int. PD.

TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Int. PD.

EC interface	
HIGH	ESPI
LOW(DEFAULT)	LPC

Modify Value to 150k for WW52 MOW
2015/03/03 Jason

EXI BOOT STALL BYPASS	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Compal Electronics, Inc.

Title: MCP(3/14)SPI,SMB,LPC

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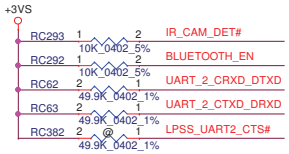
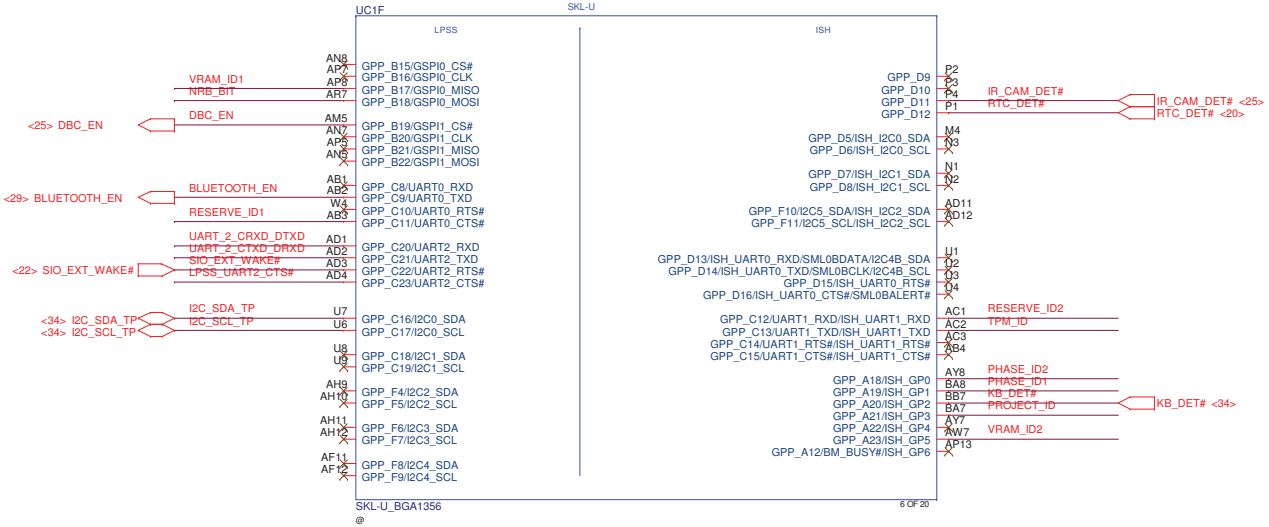
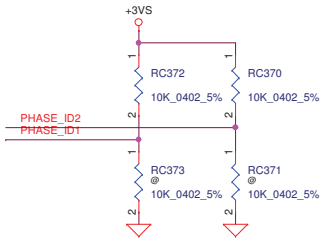
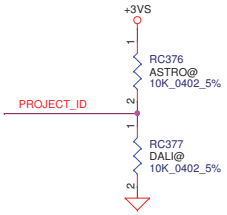


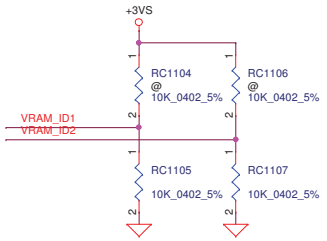




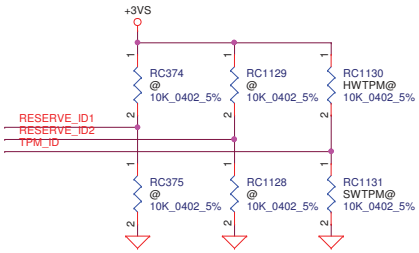
PHASE ID	PHASE_ID1 (GPP_A19)	PHASE_ID2 (GPP_A18)
EVT	0	0
DVT1	0	1
DVT2	1	0
Pilot	1	1



PROJECT ID	PROJECT_ID (GPP_A21)
Dali	0
Astro	1

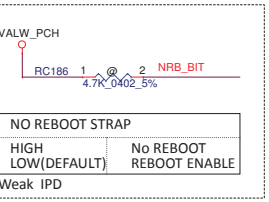


VRAM ID (PCBA VRAM Size Config.)	VRAM_ID2 (GPP_A23)	VRAM_ID1 (GPP_B17)
UMA	0	0
2G	0	1
4G	1	0
Reserved	1	1



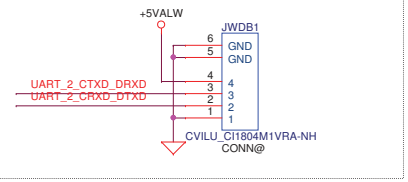
PROJECT ID	TPM_ID (GPP_C13)
SW_TPM	0
HW_TPM	1

RESERVE ID	RESERVE_ID1 (GPP_C11)	RESERVE_ID2 (GPP_C12)



Win7 Debug solution

Option 2 : For Open Chassis Platforms



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Title: MCP(4/14)GSPI,I2C,UART,ISH

Size | Document Number: LA-D822P | Rev: 1.0

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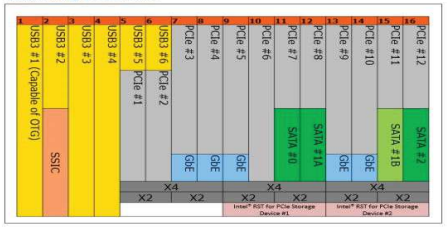
3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSIO Muxing on SKL PCH U



There are 16 HSIO lanes on SKL PCH-LP U Series, supporting the following port configurations:

1. Up to 12 PCIe* lanes (multiplexed with USB 3.0 ports, SATA Ports)
   - Only a maximum of 6 PCIe* ports (or devices) can be enabled at any time.
   - Ports 1-4, Ports 5-8, and Ports 9-12, can each be individually configured as 4x1, 2x2, 1x2 + 2x1, or 1x4.
2. Up to 3 SATA ports (multiplexed with PCIe*)
   - SATA Port 1 has the flexibility to be mapped to either PCIe* Port 8 or Port 11.
3. Up to 6 USB 3.0 ports (multiplexed with PCIe*)
   - USB Dual Role (OTG) capability is available on USB 3.0 Port 1
   - One SSIC x1 port is multiplexed with USB 3.0 Port 2
4. One GbE lane
   - GbE can be mapped into one of the PCIe* Ports 3-5 and Ports 9-10
   - When GbE is enabled, there can be at most up to 5 PCIe* ports enabled.
5. Up to 2 Intel RST for PCIe* storage devices supported
   - Devices can be x2 or x4
   - Devices can be implemented on PCIe Ports 5-8 and Ports 9-12

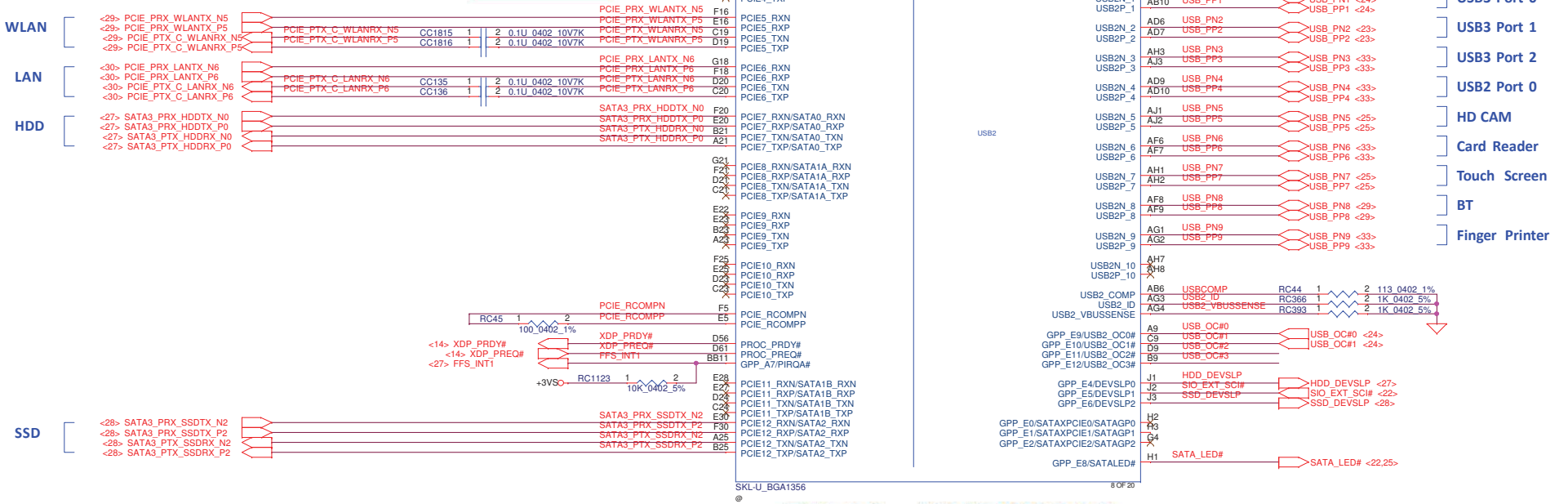


Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe / LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe / LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe / LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

Compal Electronics, Inc.

Title: MCP(5/14)PCIE,USB,SATA

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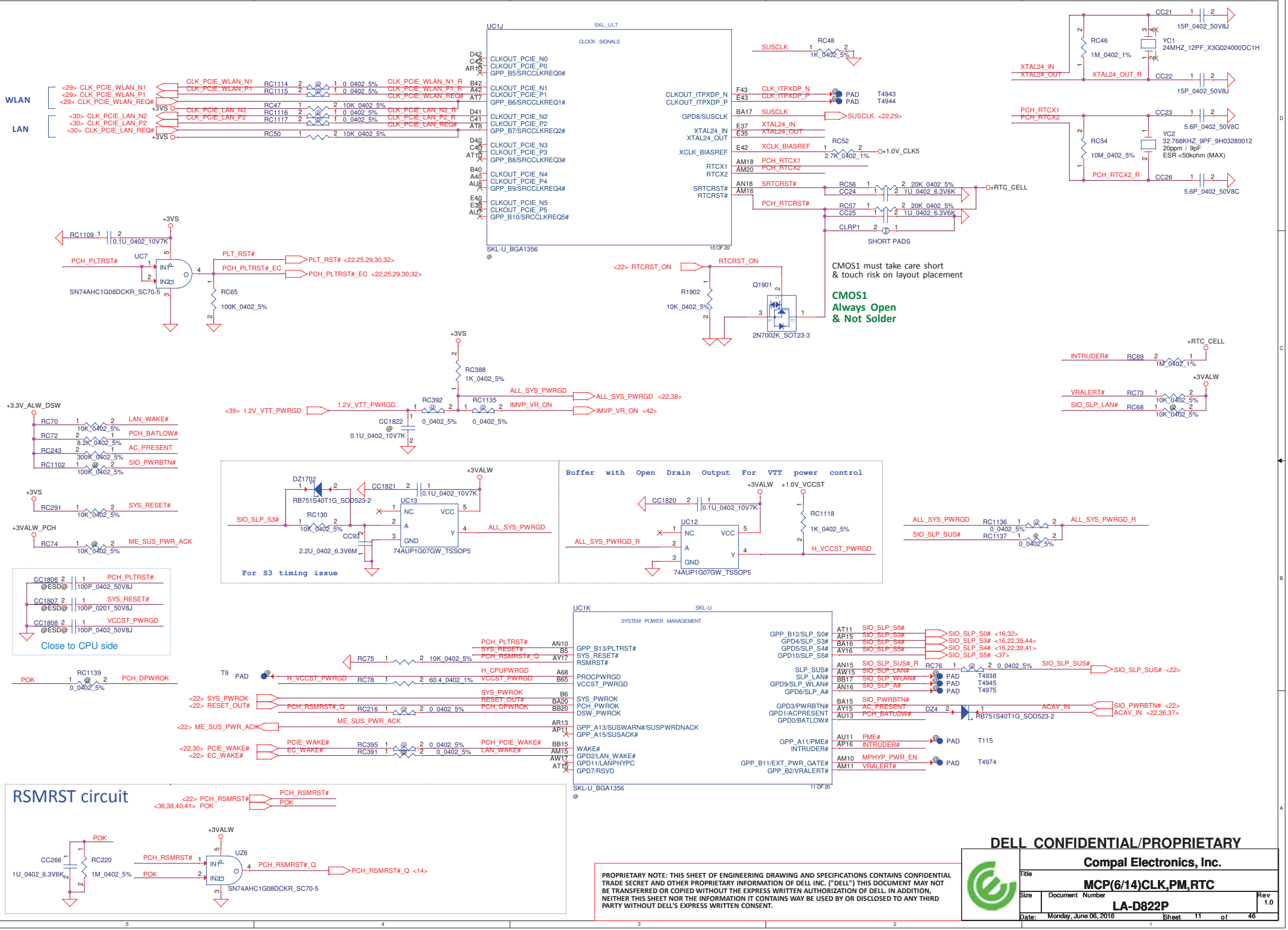
WLAN
LAN
CLK_PCIE_WLAN_N1
CLK_PCIE_WLAN_P1
CLK_PCIE_WLAN_REQ#
CLK_PCIE_LAN_N2
CLK_PCIE_LAN_P2
CLK_PCIE_LAN_REQ#
UC1J
SKL_ULT
CLOCK SIGNALS
SKL-U_BGA1356
10 OF 20
SUSCLK
XTAL24_IN
XTAL24_OUT
XCLK_BIASREF
PCH_RTCX1
PCH_RTCX2
SRTCRST#
RTCRST#
PCH_RTCRST#
+RTC_CELL
SHORT PADS
CMOS1 must take care short
& touch risk on layout placement
CMOS1
Always Open
& Not Solder
2N7002K_SOT23-3
SN74AHC1G08DCKR_SC70-5
PLT_RST#
PCH_PLTRST#
PCH_PLTRST#_EC
RTCRST_ON
+3VS
+3VALW
+3.3V_ALW_DSW
+3VALW_PCH
+1.0V_VCCST
ALL_SYS_PWRGD
1.2V_VTT_PWRGD
IMVP_VR_ON
LAN_WAKE#
PCH_BATLOW#
AC_PRESENT
SIO_PWRBTN#
SYS_RESET#
ME_SUS_PWR_ACK
INTRUDER#
VRALERT#
SIO_SLP_LAN#
RB751S40T1G_SOD523-2
74AUP1G07GW_TSSOP5
For S3 timing issue
Buffer with Open Drain Output For VTT power control
H_VCCST_PWRGD
ALL_SYS_PWRGD_R
SIO_SLP_SUS#
SIO_SLP_S3#
PCH_PLTRST#
SYS_RESET#
VCCST_PWRGD
Close to CPU side
POK
PCH_DPWROK
T9
PAD
H_VCCST_PWRGD
SYS_PWROK
RESET_OUT#
PCH_RSMRST#_Q
ME_SUS_PWR_ACK
PCIE_WAKE#
EC_WAKE#
PCH_PCIE_WAKE#
LAN_WAKE#
UC1K
SKL-U
SYSTEM POWER MANAGEMENT
SKL-U_BGA1356
11 OF 20
SIO_SLP_S0#
SIO_SLP_S3#
SIO_SLP_S4#
SIO_SLP_S5#
SIO_SLP_SUS#
SIO_SLP_LAN#
SIO_SLP_WLAN#
SIO_SLP_A#
SIO_PWRBTN#
AC_PRESENT
PCH_BATLOW#
ACAV_IN
PME#
INTRUDER#
MPHYP_PWR_EN
VRALERT#
RB751S40T1G_SOD523-2
RSMRST circuit
PCH_RSMRST#
POK
SN74AHC1G08DCKR_SC70-5
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MCP(6/14)CLK,PM,RTC
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1.0
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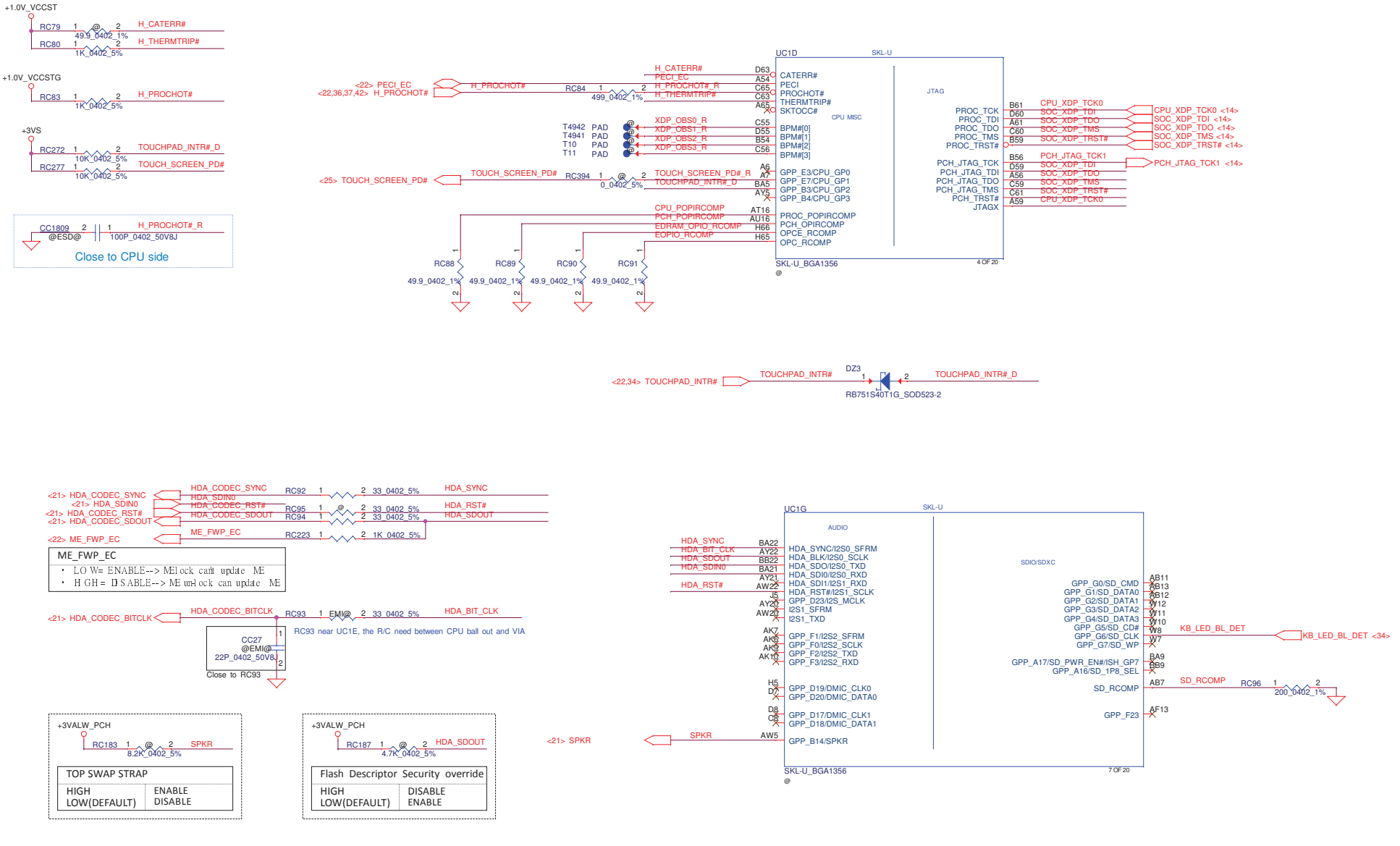

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Compal Electronics, Inc.

Title: MCP(7/14)MISC,JTAG,HDA,SDIO

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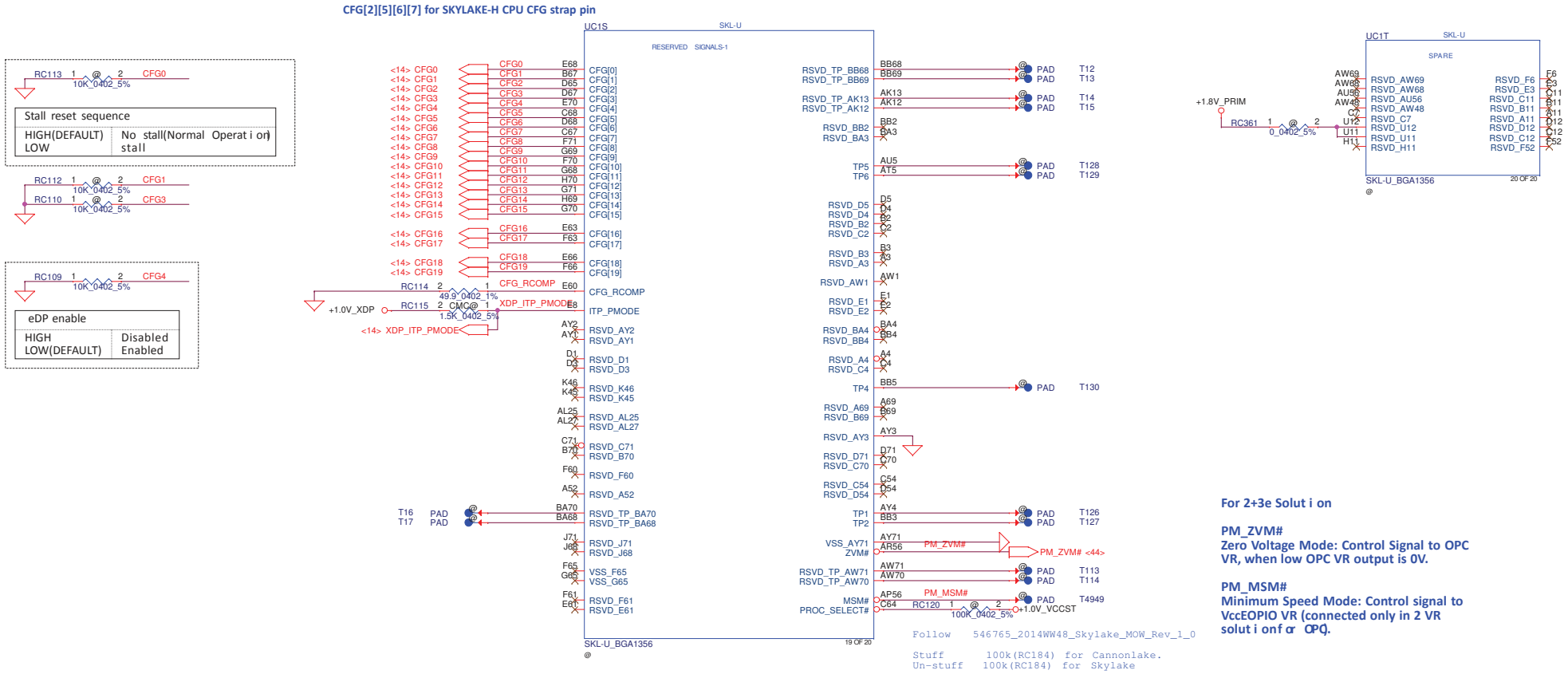

Compal Electronics, Inc.

Title: MCP(8/14)CFG,RSVD

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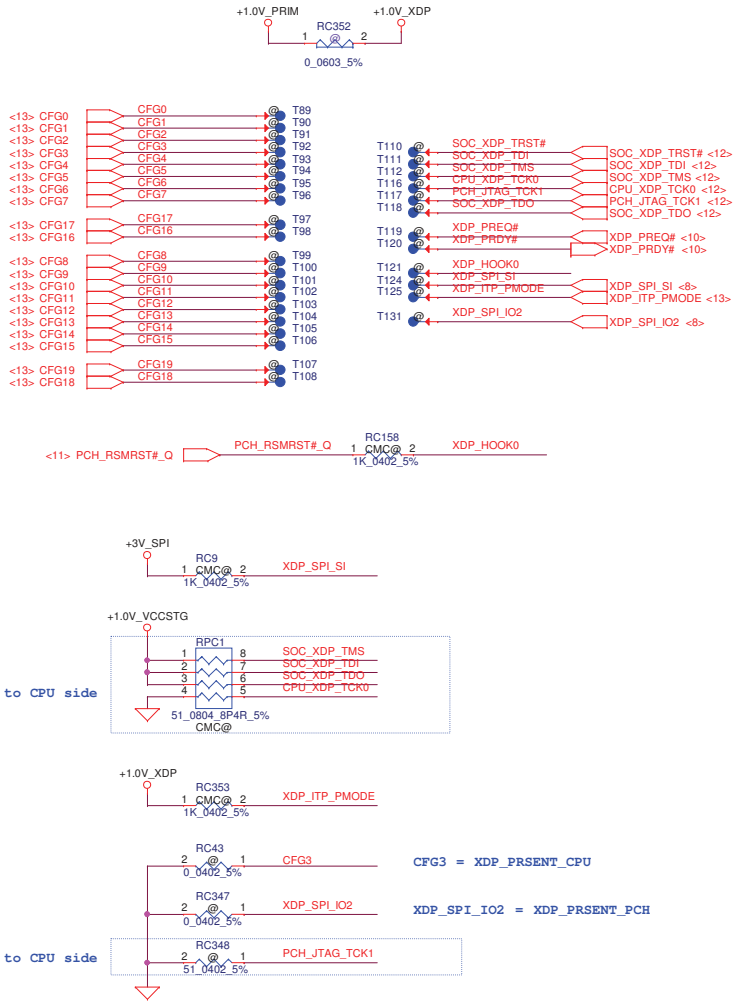
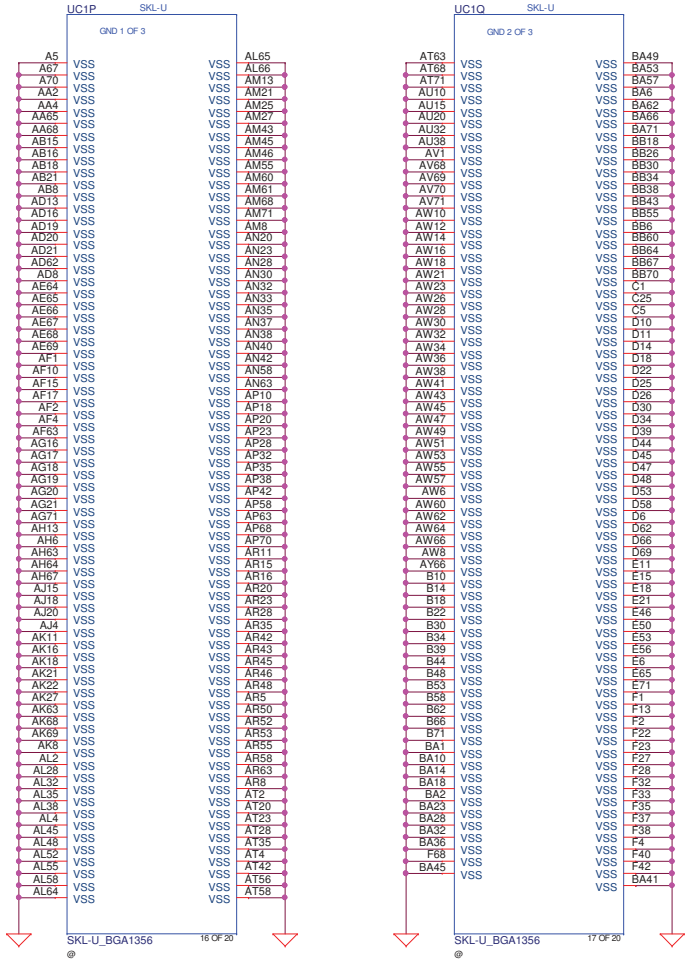
PRIMARY CMC CONN





For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

Compal Electronics, Inc.

Title: MCP(9,14/14)XDP/VSS

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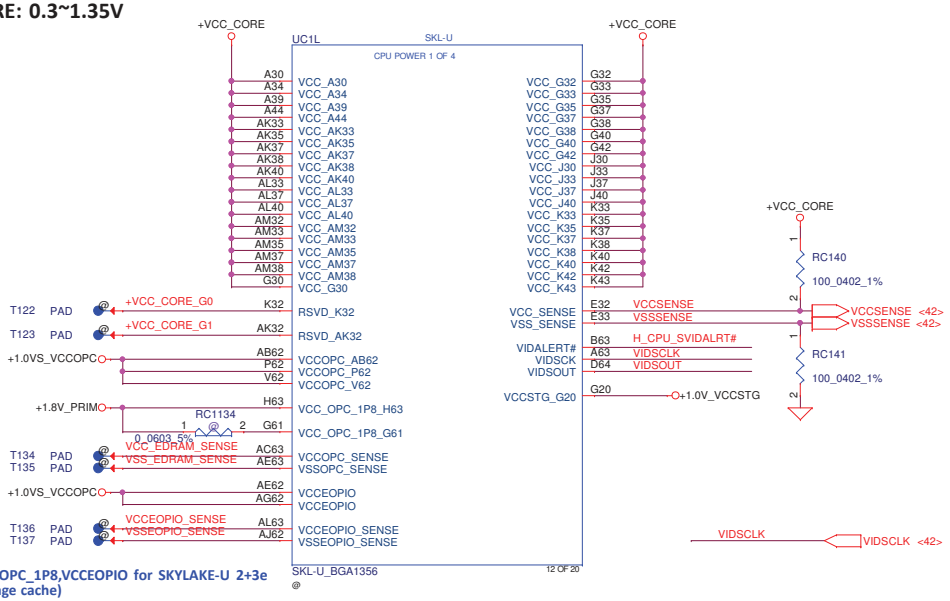
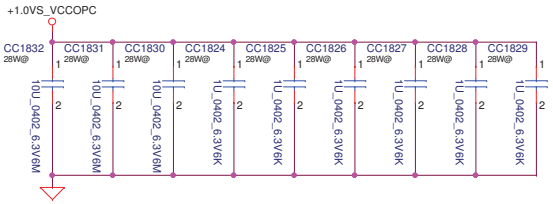
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

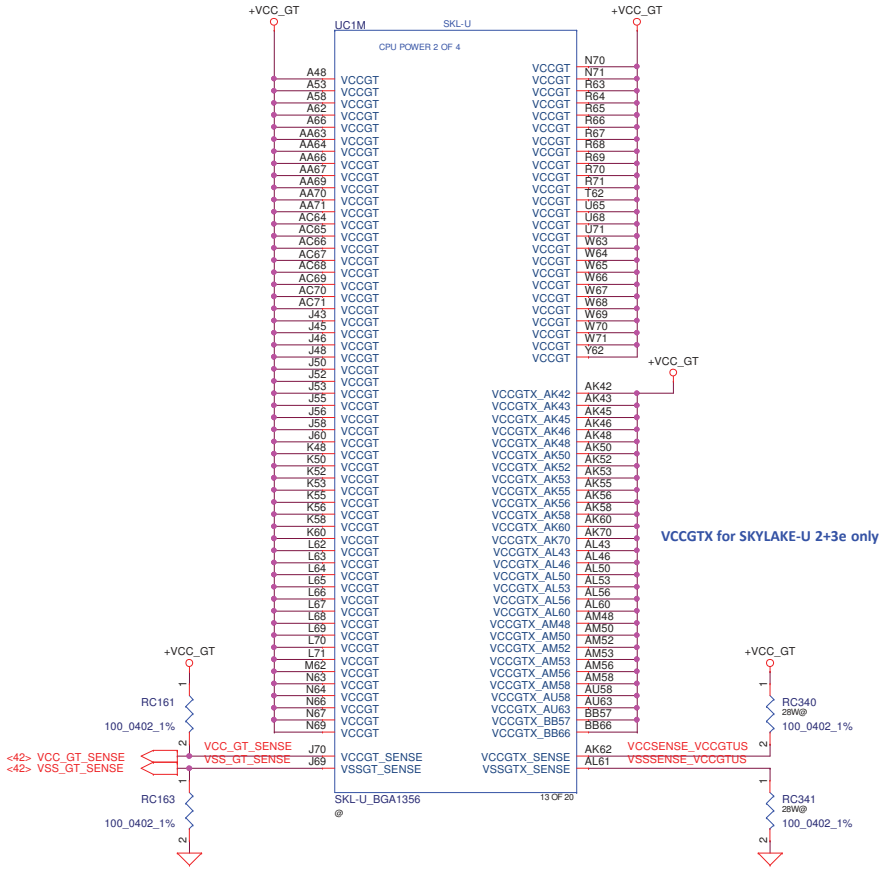
+VCC_CORE: 0.3~1.35V



VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)

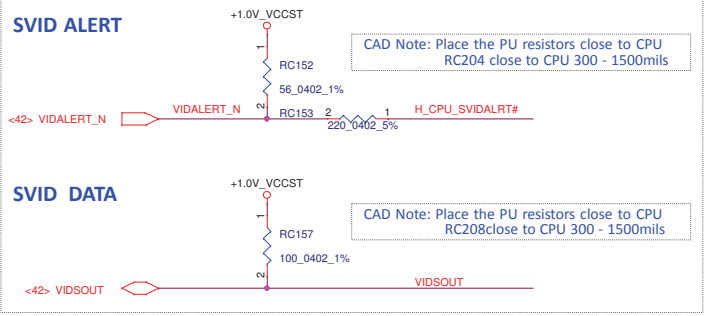


+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



VCCGTX for SKYLAKE-U 2+3e only

SVID ALERT



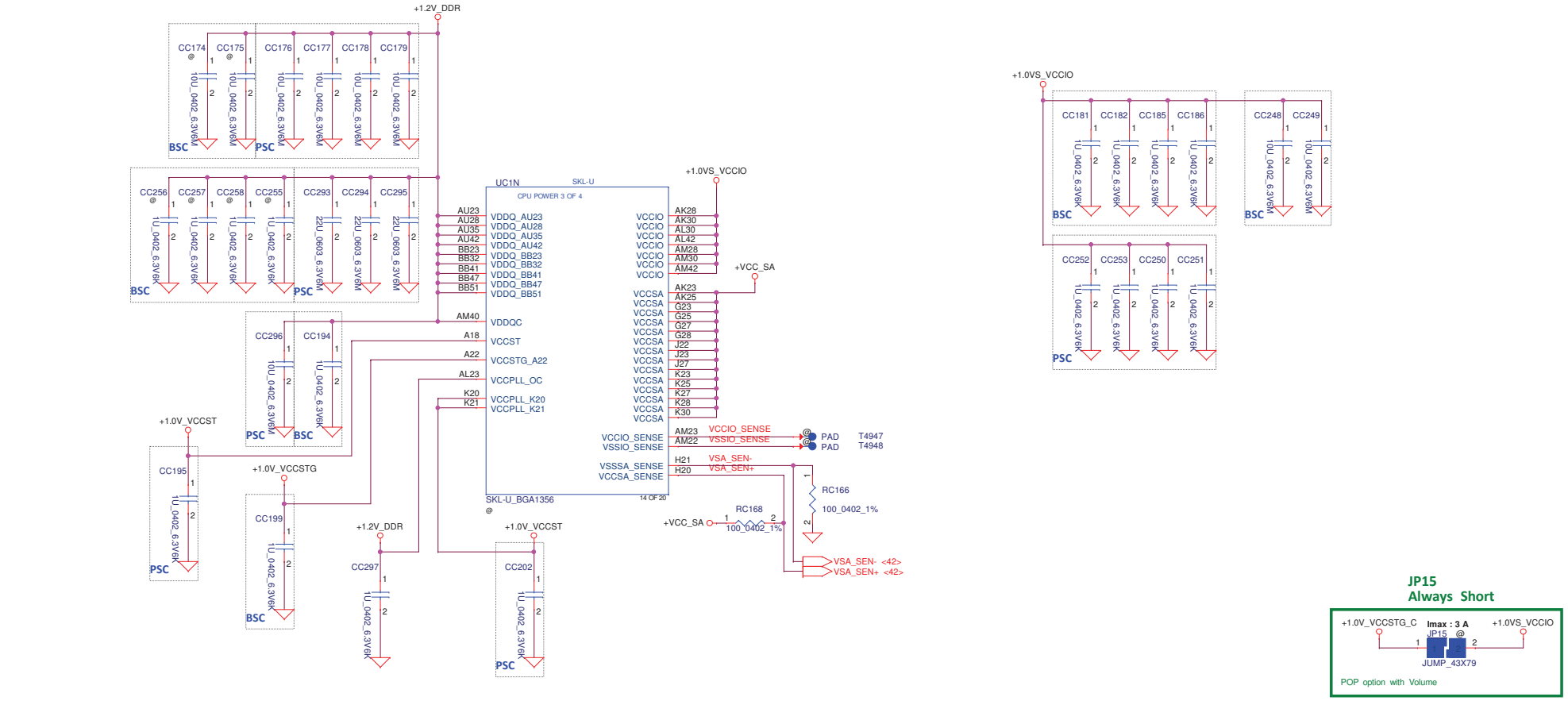
SVID DATA

Compal Electronics, Inc.

Title: MCP(10,11/14)PWR-VCCCORE,GT

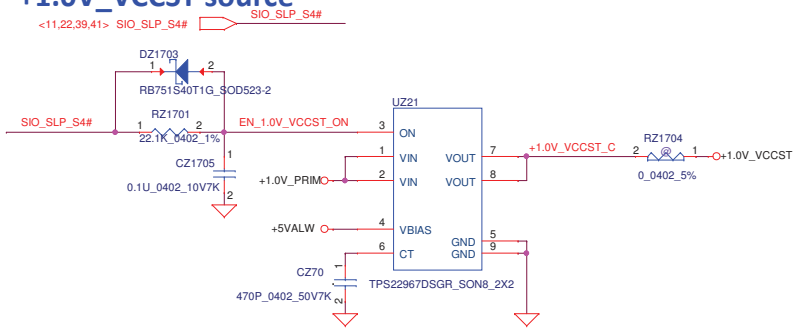
Size | Document Number: LA-D822P | Rev: 1.0

Date: Monday, June 06, 2016 | Sheet 15 of 46

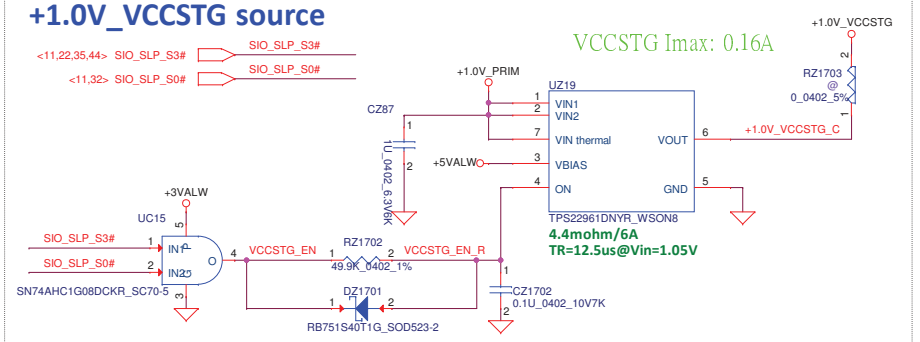


JP15
Always Short

+1.0V_VCCST source



+1.0V_VCCSTG source

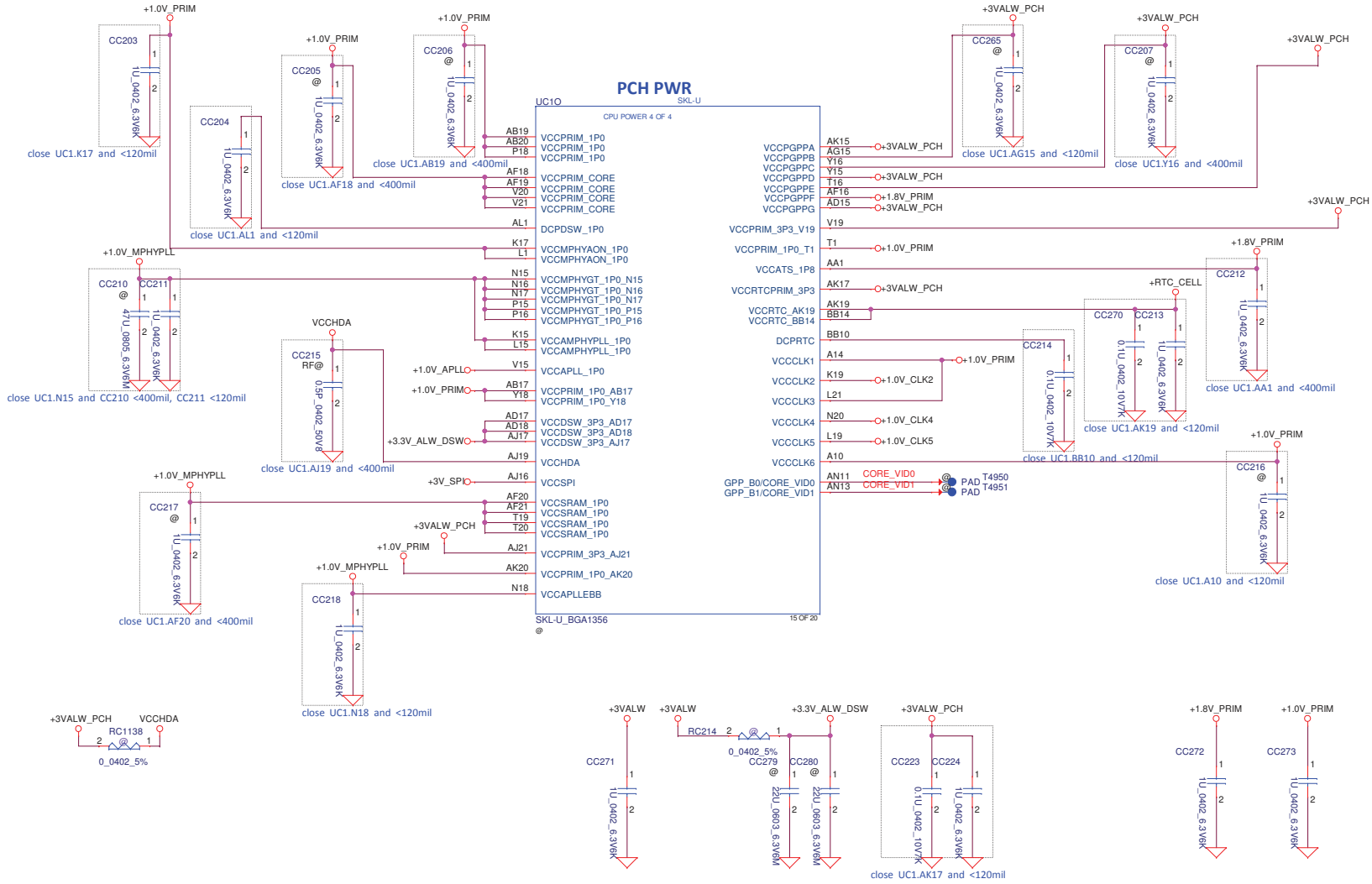


Compal Electronics, Inc.

Title: MCP(12/14)PWR-VCCIO,MEM

Size | Document Number: LA-D822P | Rev: 1.0

Date: Monday, June 06, 2016 | Sheet 16 of 46

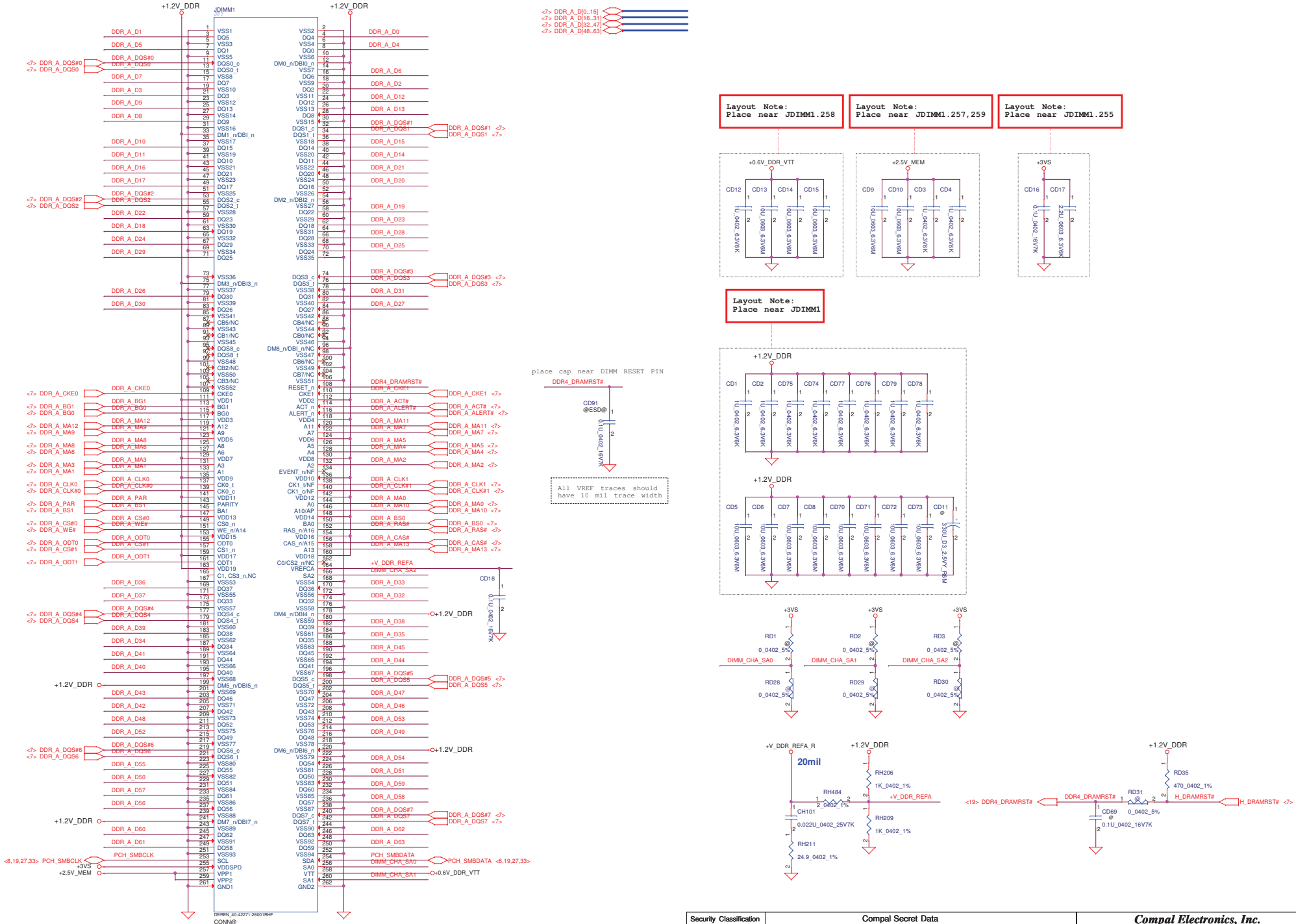


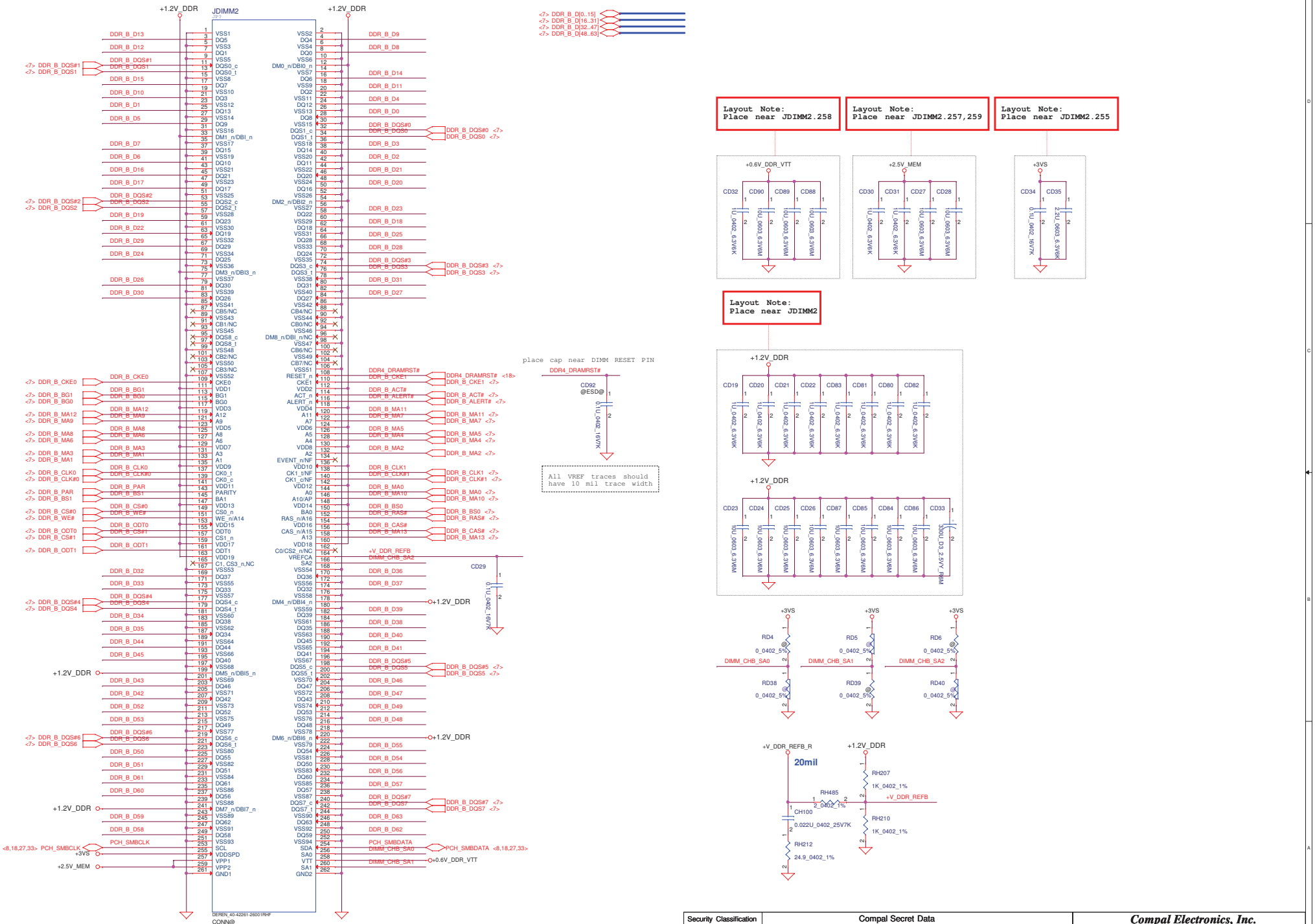
Compal Electronics, Inc.

Title: MCP(13/14)PCH PWR

Size | Document Number: LA-D822P | Rev: 1.0

Date: Monday, June 06, 2016 | Sheet 17 of 46


JDIMM1
CONN@
DEREN_40-42271-26001RHF
+1.2V_DDR
+3VS
+2.5V_MEM
+0.6V_DDR_VTT
Layout Note: Place near JDIMM1.258
Layout Note: Place near JDIMM1.257,259
Layout Note: Place near JDIMM1.255
Layout Note: Place near JDIMM1
place cap near DIMM RESET PIN
All VREF traces should have 10 mil trace width
20mil
Security Classification
Compal Secret Data
Issued Date
2015/01/30
Deciphered Date
2016/12/31
Compal Electronics, Inc.
DDRIV DIMMA
LA-D822P
Rev 1.0
Monday, June 06, 2016
Sheet 18 of 46



Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.	
Title	DDRIV DIMMB
Size	Document Number: LA-D822P
Rev	1.0
Date:	Monday, June 06, 2016
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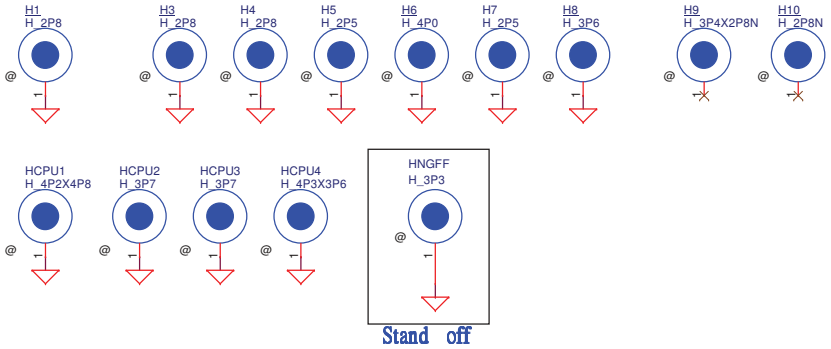
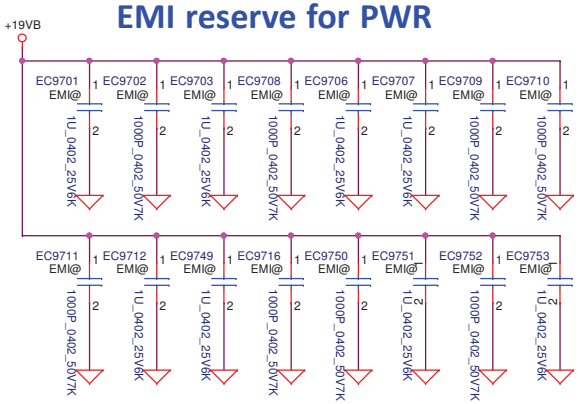
Main Func = Other

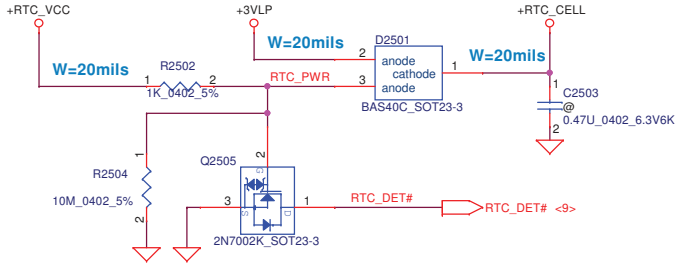
Screw hole/FD/EMI stop



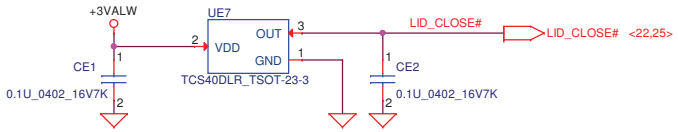
EMI reserve for PWR



Main Func = RTC



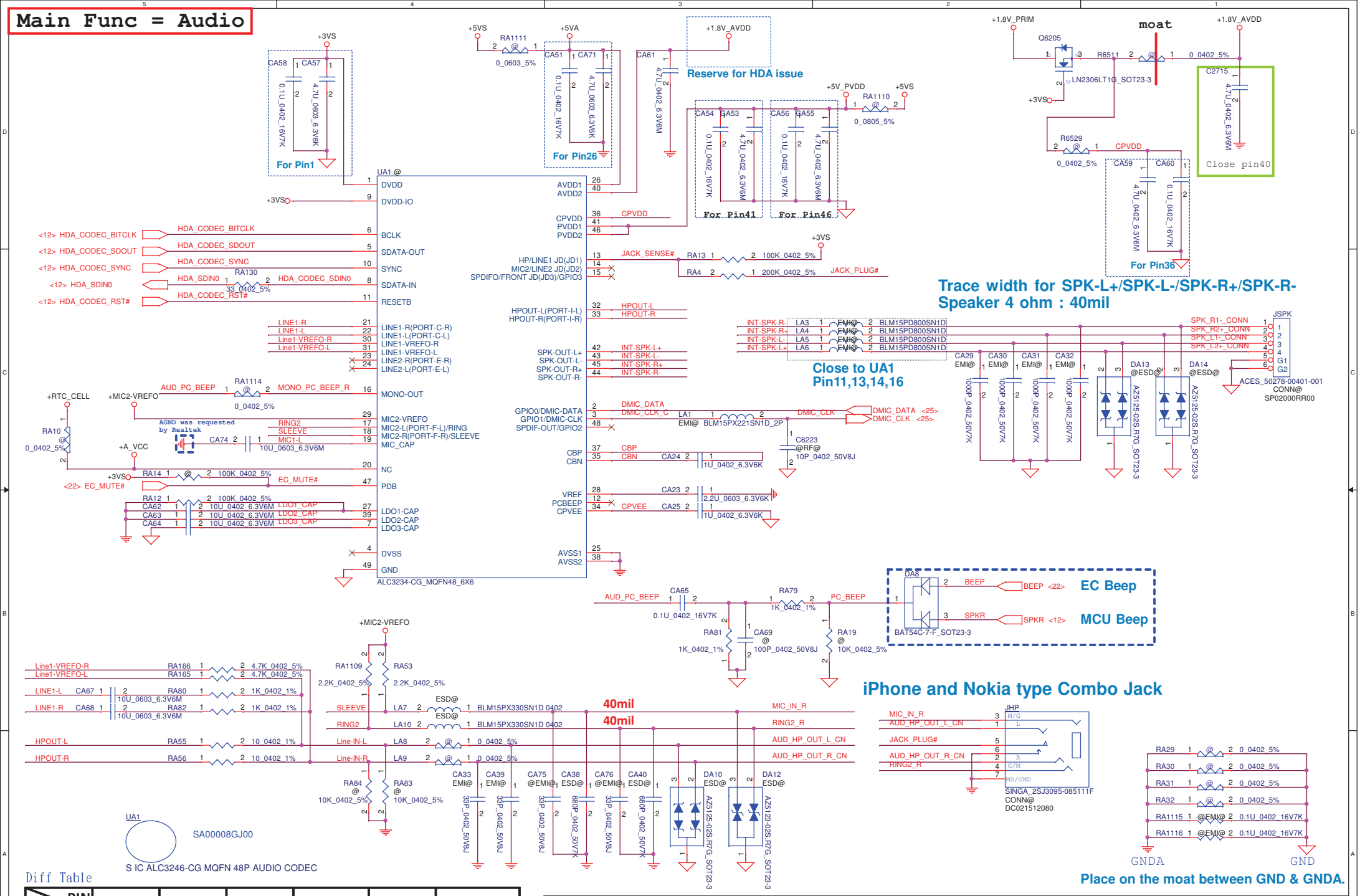
Main Func = LID Switch



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title: RTC/LID SW/Screw hole/EMI			
Size	Document Number: LA-D822P		Rev: 1.0
Date: Monday, June 06, 2016	Sheet 20 of 46		

Main Func = Audio

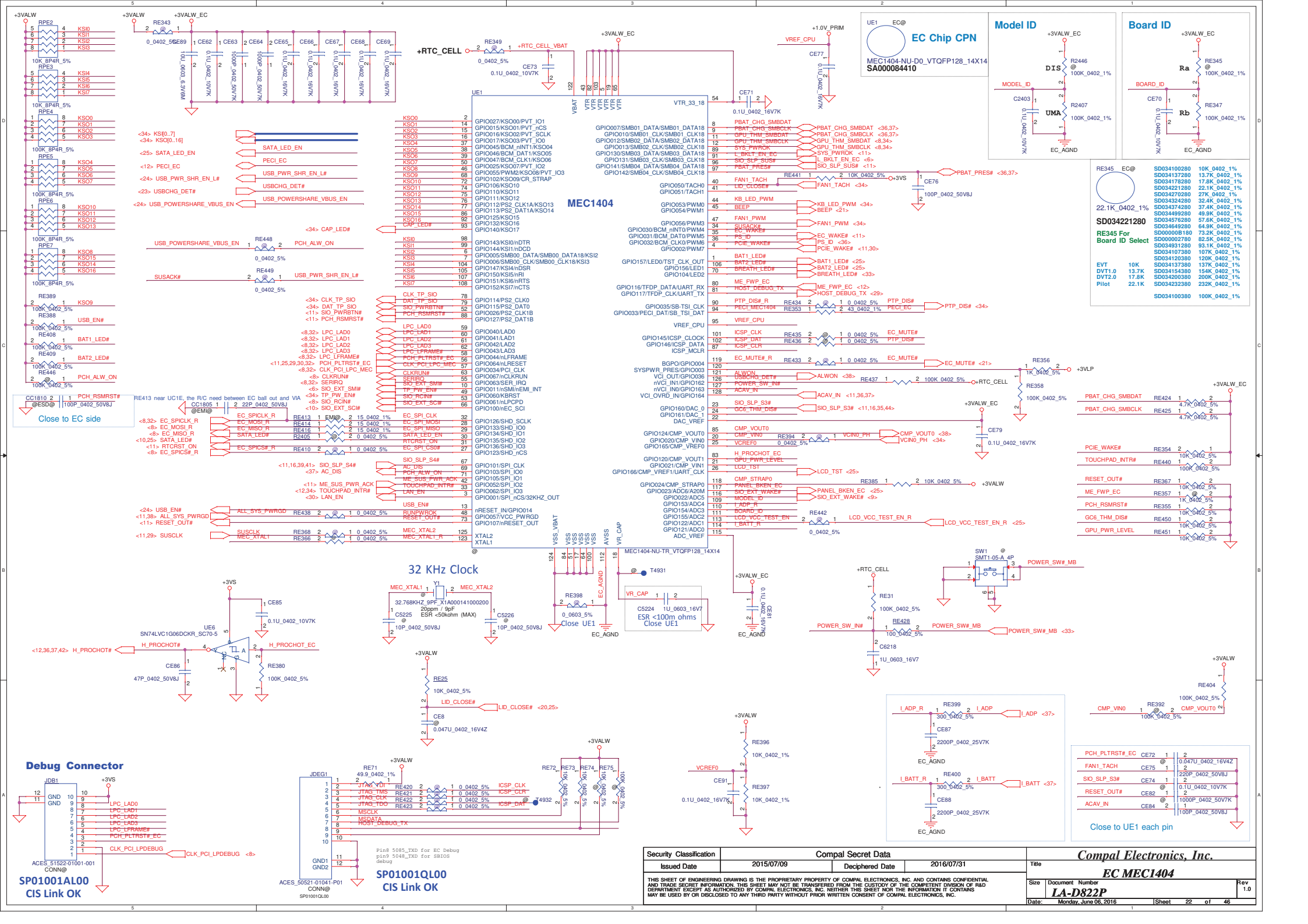


Diff Table

IC \ PIN	PIN4	PIN11	PIN12	PIN16	PIN20	PIN36
ALC3234	DVSS	RESETB	PCBEEP	MONO-OUT	NC	CPVDD(3.3V)
ALC3246	DC_DET	I2C_SDA	I2C_SCL	PCBEEP	5VSTB	CPVDD(1.8V)

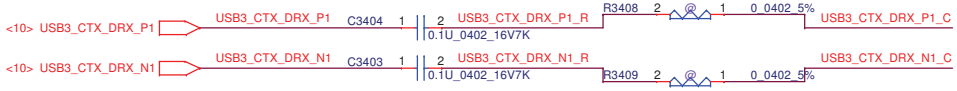
Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.	
Title	Audio Codec ALC3246
Size	Document Number: LA-D822P — Rev: 1.0
Date: Monday, June 06, 2016	Sheet 21 of 46

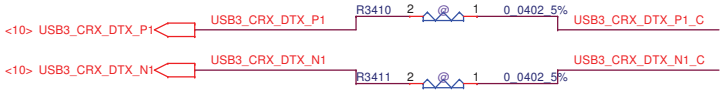

MEC1404
EC Chip CPN
MEC1404-NU-D0_VTQFP128_14X14
SA000084410
Model ID
Board ID
RE345 EC@
22.1K_0402_1%
SD034221280
RE345 For Board ID Select
EVT 10K
DVT1.0 13.7K
DVT2.0 17.8K
Pilot 22.1K
Close to EC side
32 KHz Clock
Close UE1
Debug Connector
SP01001AL00
CIS Link OK
SP01001QL00
CIS Link OK
Close to UE1 each pin
Compal Electronics, Inc.
EC MEC1404
LA-D822P
Monday, June 06, 2016

Main Func = USB3.0 Port1/Port2

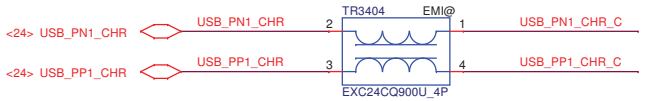
USB3.0 90ohm
Main SM070003V00(S COM FI_ INPAQ HCM1012GH900BP)
2nd SM070004000(S COM FI_ TAIYO MCF12102G900-T)
3rd SM070004300(S COM FI_ PANASONIC EXC24CH900U)



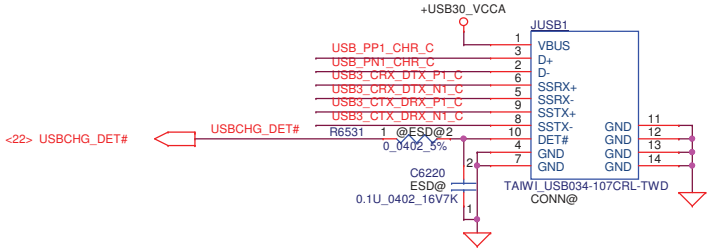
USB3.0 90ohm
Main SM070003V00(S COM FI_ INPAQ HCM1012GH900BP)
2nd SM070004000(S COM FI_ TAIYO MCF12102G900-T)
3rd SM070004300(S COM FI_ PANASONIC EXC24CH900U)

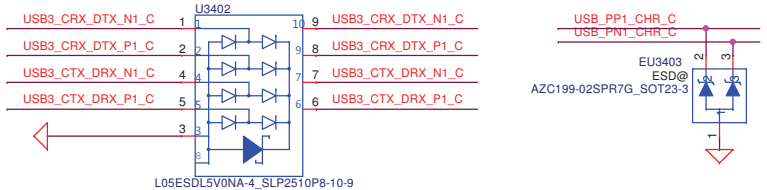


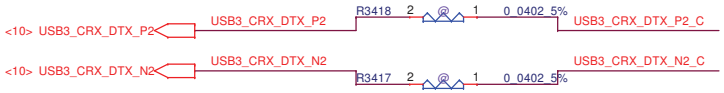
USB2.0 90ohm
Main SM070003Z00(S COM FI_ INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FI_ MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FI_ PANASONIC EXC24CQ900U)

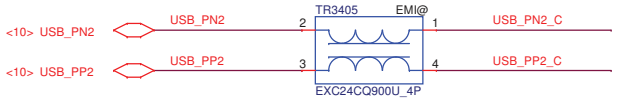


USB3.0 Port1

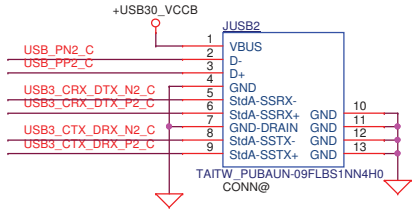


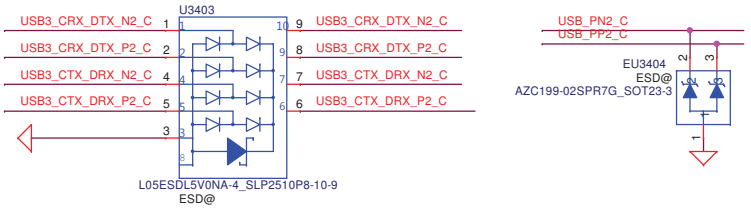






USB3.0 Port2





Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: **USB3.0 CONN**

Size	Document Number	Rev
	LA-D822P	1.0

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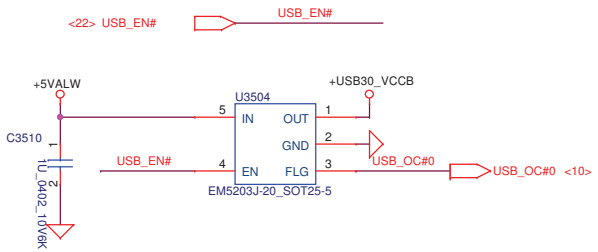
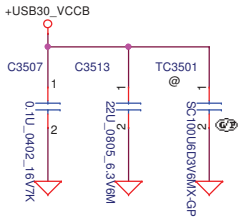
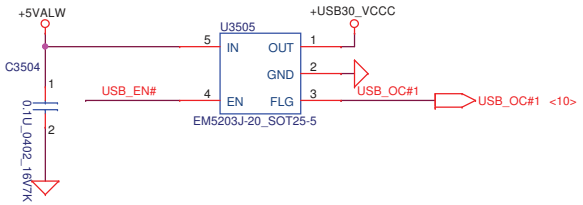
Main Func = USB3.0 Port2

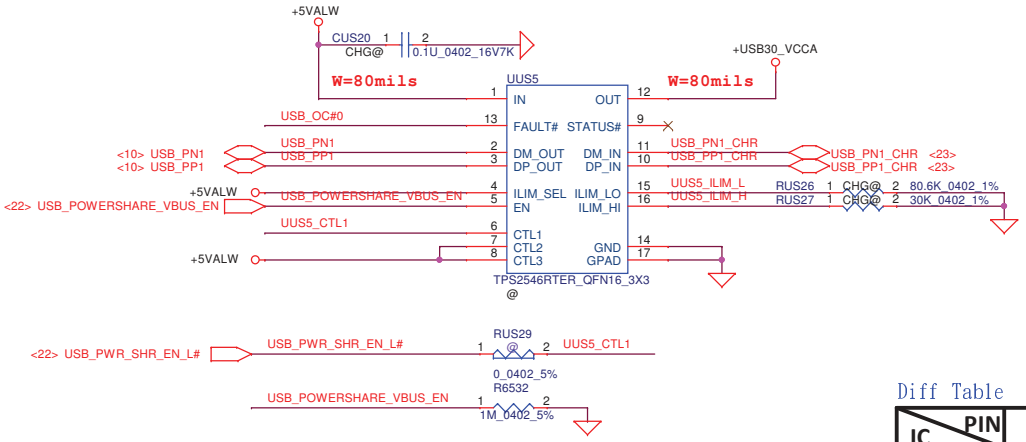


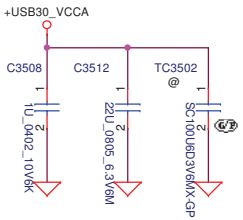


Main Func = USB3.0 Port3 / USB2.0 Port



Main Func = USB Chager





Charger CT	CTL1	CTL2	CTL3	ILIM_SEL
EC GPIO	GPXIOA07(pin104)	GPIO22(pin41)	GPXIOA11(pin108)	GPIO21(pin40)
S0/S3(CDP)	1	1	1	1
S4/S5(DCP)	0	1	1	1

Diff Table

IC \ PIN	PIN9
TPS2546	STATUS#
TPS2544	NC

UUS5

SA000070N00

CHG@

S IC TPS2544RTER WQFN 16P PWR SW

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: USB Power SW

Size | Document Number: LA-D822P | Rev: 1.0

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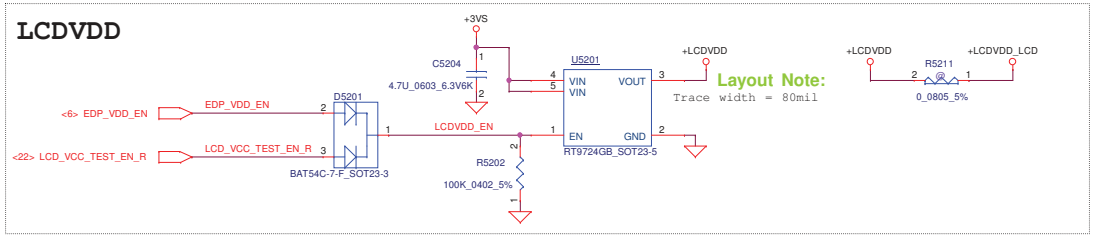
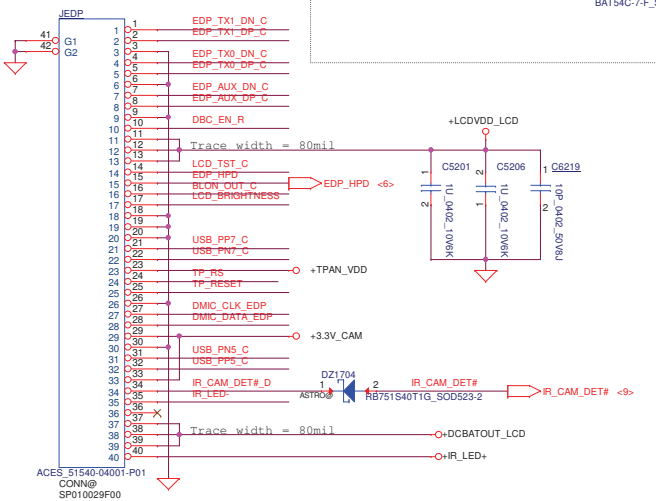
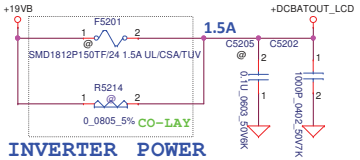
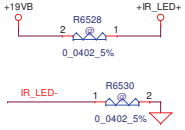
Main Func = LCD

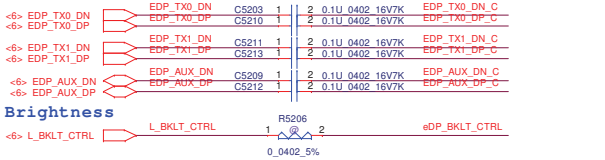
LCDVDD

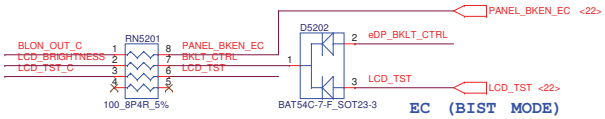


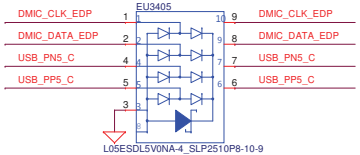


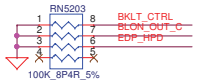


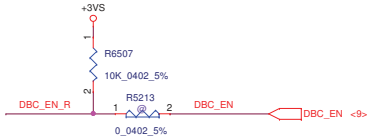




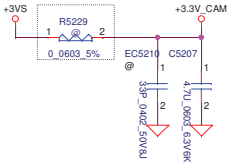


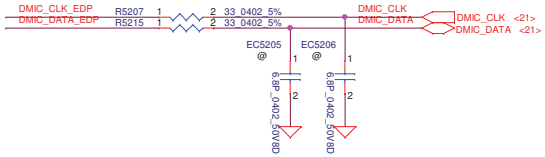






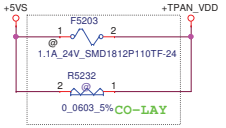
Main Func = CAM

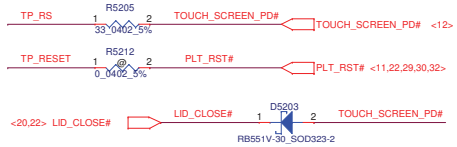




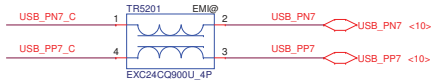
Main Func = TS

Touch Panel

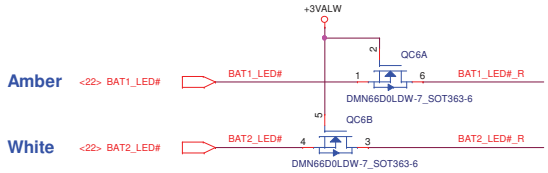


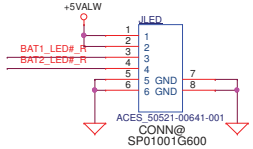


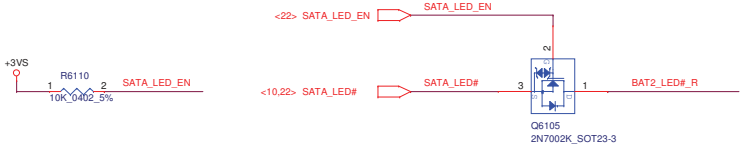
USB2.0 90ohm
Main SM070003Z00(S COM FI_ INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FI_ MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FI_ PANASONIC EXC24CQ900U)



Main Func = LED







Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title	LCD/Cam/MIC/T.Panel/LED		
Size	Document Number		Rev
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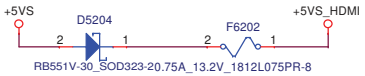
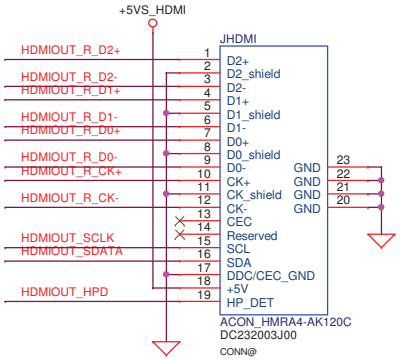
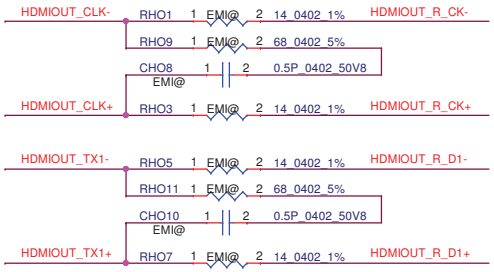
Main Func = HDMI

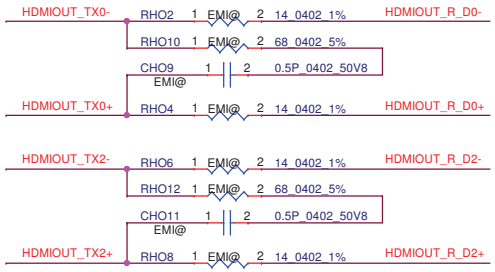
2014.12.25
1. LHO1 ,LHO2 ,LHO3 , LH O4 chan ge ro ot p in (SI ZE : 050 4) a nd unpp
2. RHO1,RHO3,RHO5,RHO7,RHO2,RHO4,RHO6,RHO8,RHO13,RHO14,RHO15,RHO16, change to pop.

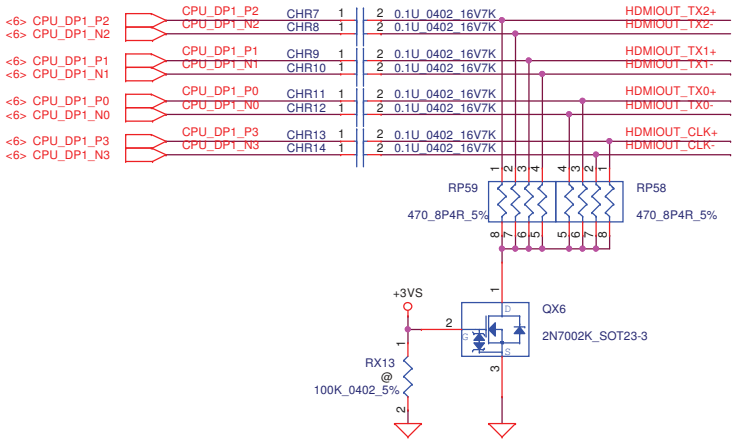


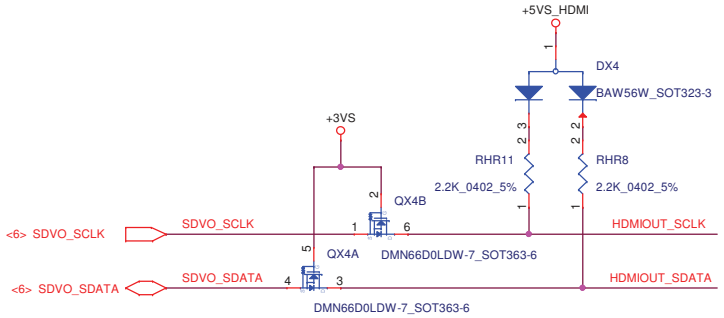
HDMI-OUT Connector

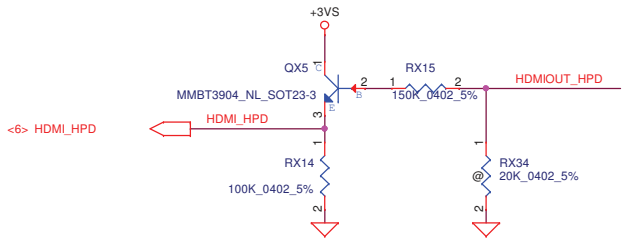












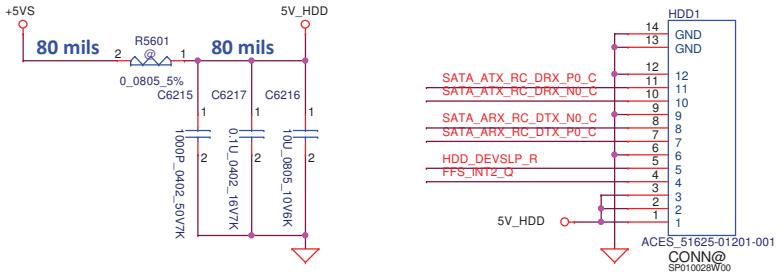
Security Classification	Compal Secret Data		
Issued Date	2014/04/02	Deciphered Date	2015/10/02

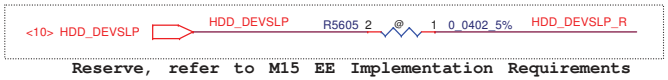
Compal Electronics, Inc.			
Title: HDMI			
Size	Document Number: LA-D822P		Rev: 1.0
Date: Monday, June 06, 2016	Sheet 26 of 46		

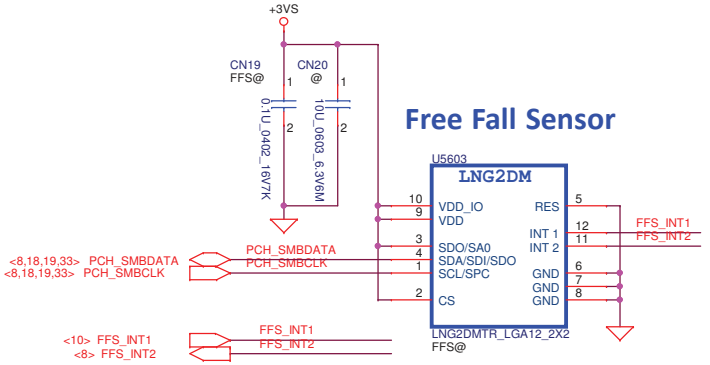
Main Func = HDD

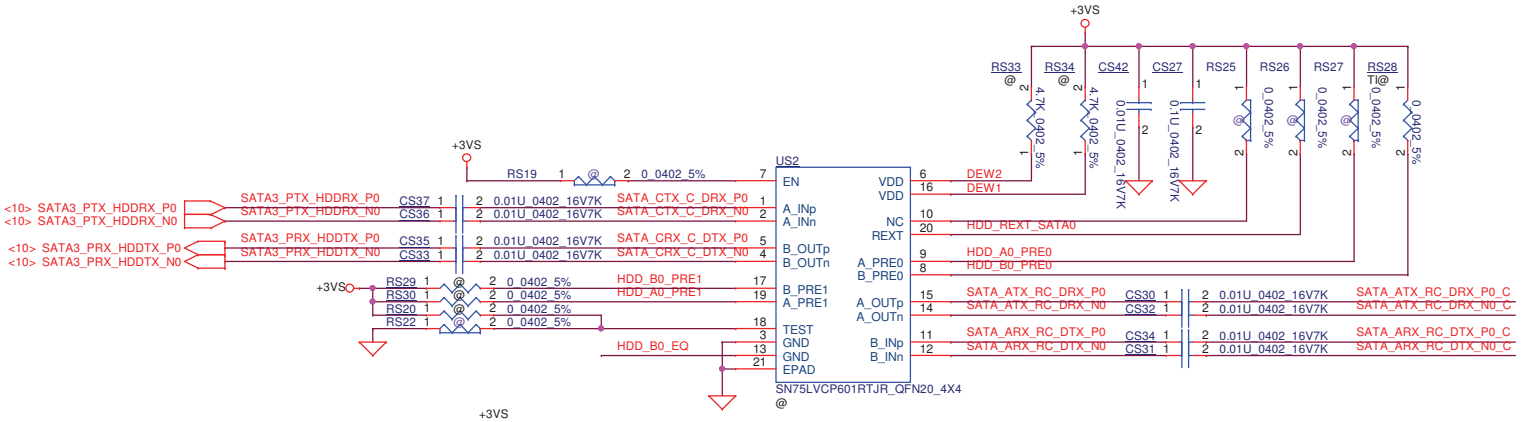
SATA HDD Connector

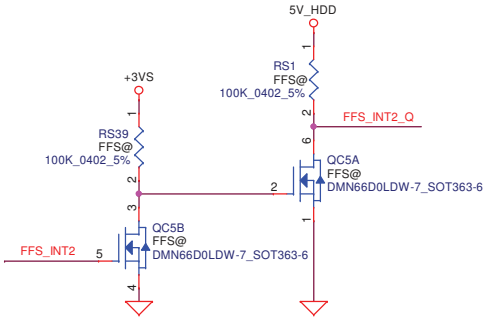
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

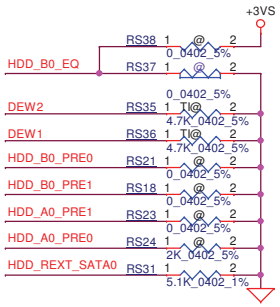












	US2	RS35	RS36	RS18	RS22	RS23	RS24	RS28
TI	SA00003ZX00	4.7K	4.7K	NC	NC	NC	2K	V
PARADE	SA00007JU00	7.5K	NC	V	V	V	NC	NC

US2 TI@

SN75LVCP601RTJR

SA00003ZX00

US2 PARADE@

PS8527CTQFN20GTR2-A2

SA00007JU10

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

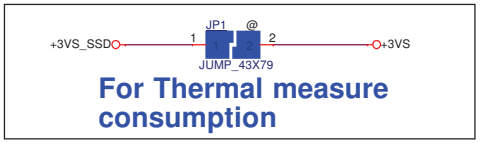
Compal Electronics, Inc.

Title: HDD+Sensor

Size	Document Number	Rev
	LA-D822P	1.0

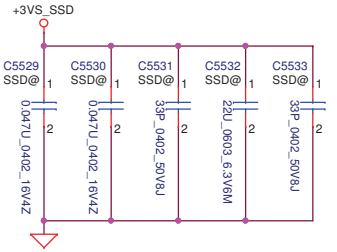
Date: Monday, June 06, 2016 Sheet 27 of 46

Main Func = SSD

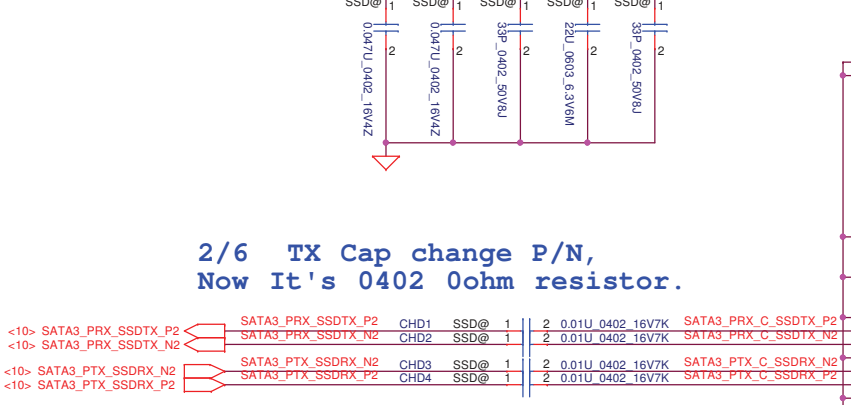


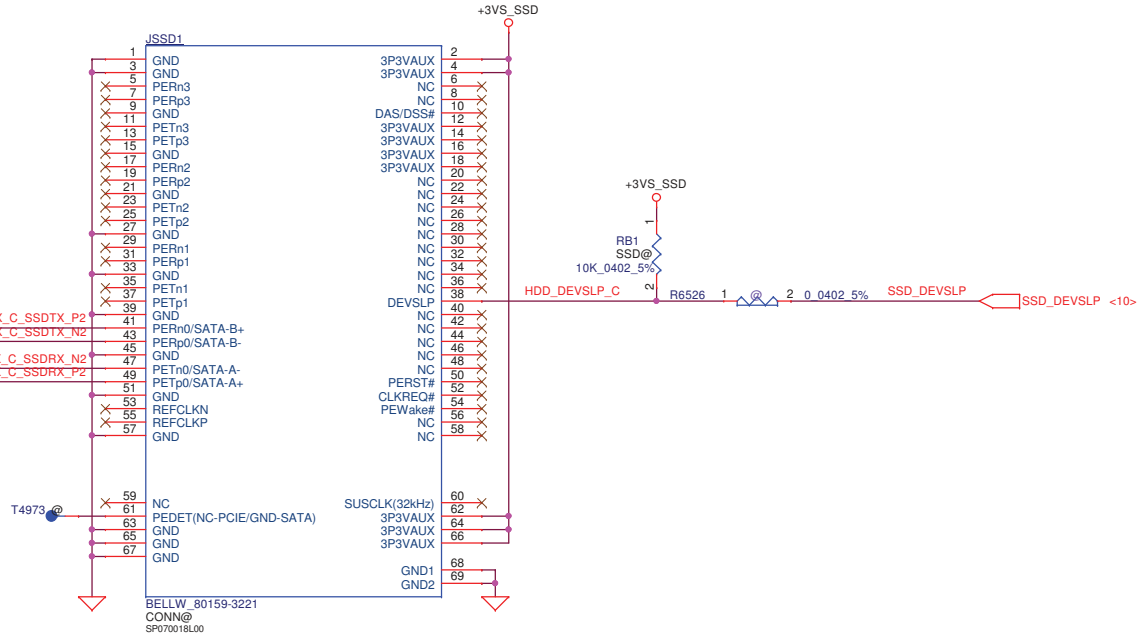
SSD

NGFF Slot_2 Key M



2/6 TX Cap change P/N,
Now It's 0402 0ohm resistor.

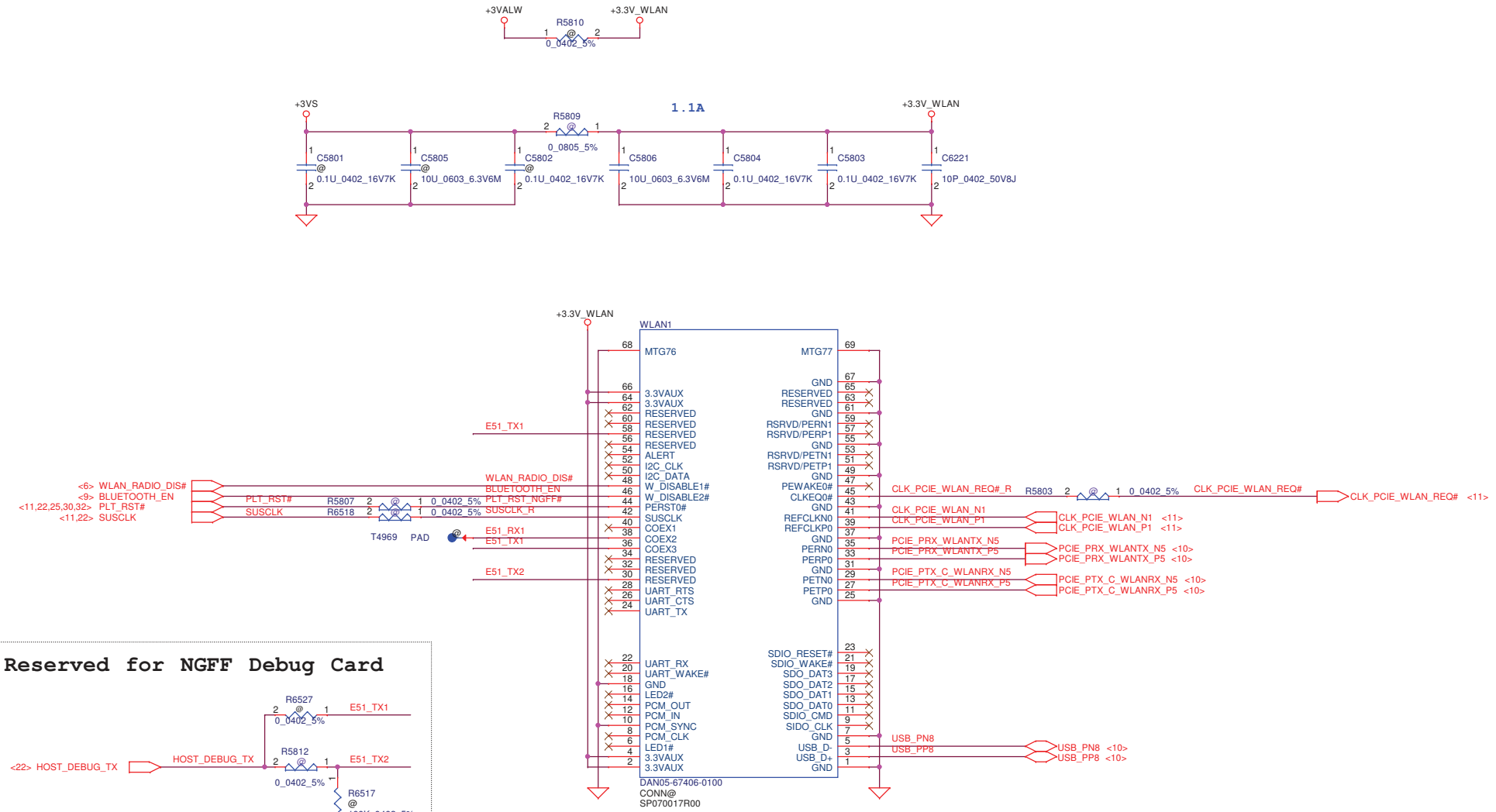




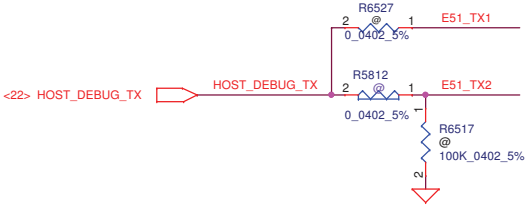
Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title: SSD			
Size	Document Number: LA-D822P		Rev: 1.0
Date: Monday, June 06, 2016	Sheet 28 of 46		

Main Func = WLAN



Reserved for NGFF Debug Card



Support: Intel Dual Band Wireless-AC 3160

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

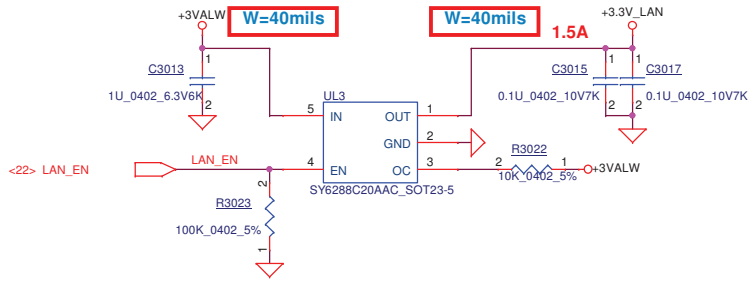
Title: **WLAN**

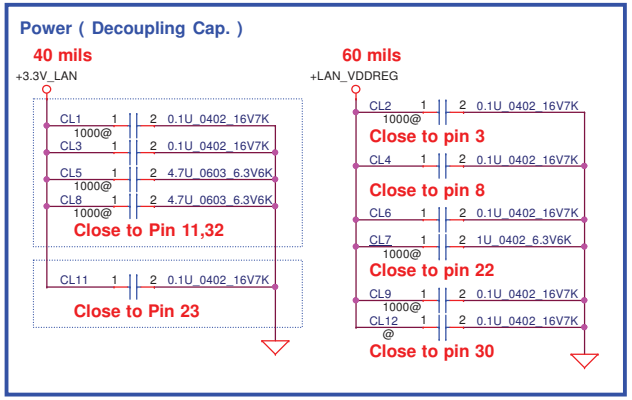
Size | Document Number: **LA-D822P** | Rev: 1.0

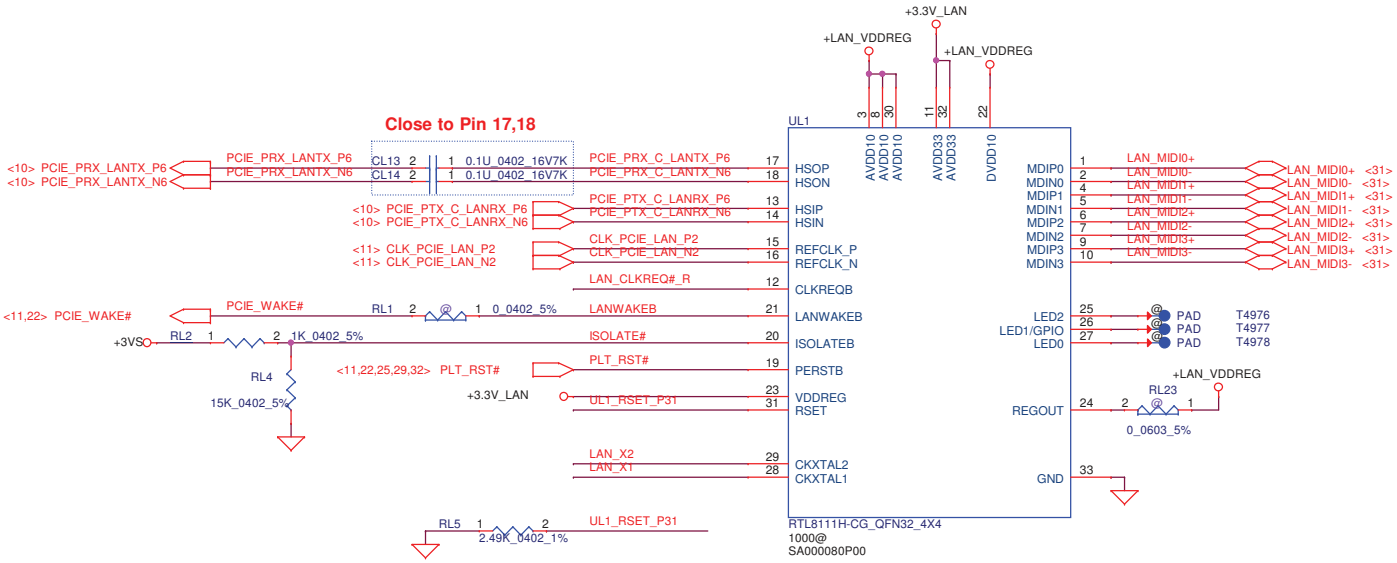
Date: Monday, June 06, 2016 | Sheet 29 of 46

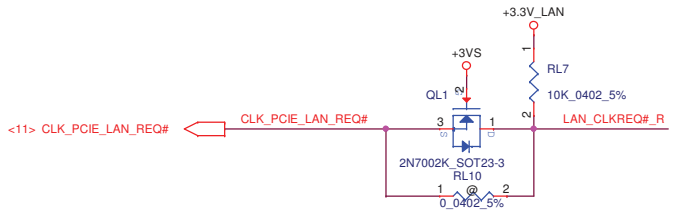
Main Func = LAN

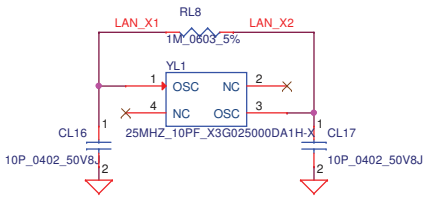
+3.3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.











Security Classification	Compal Secret Data		
Issued Date	2014/12/15	Deciphered Date	2016/12/15

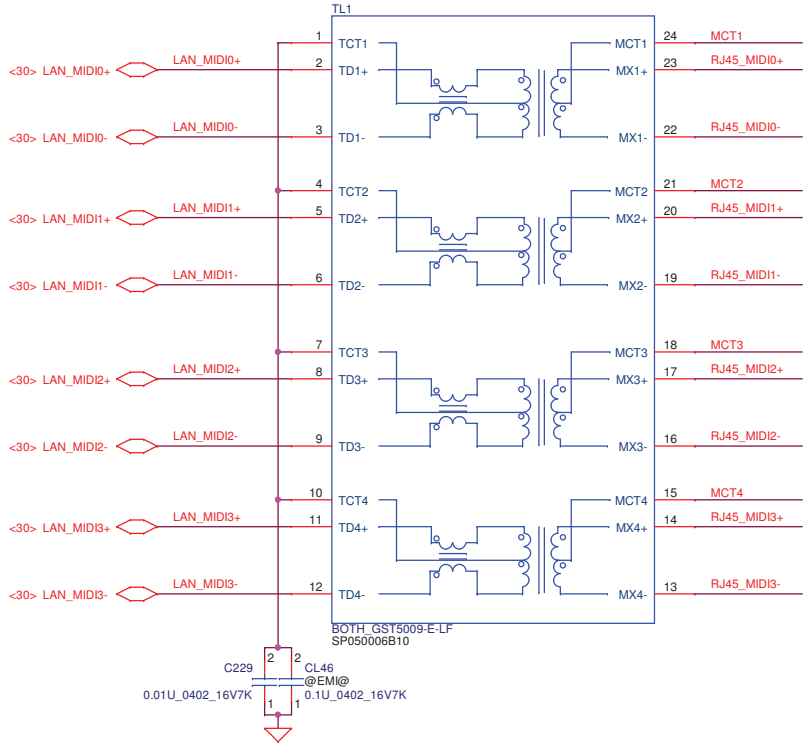
Compal Electronics, Inc.

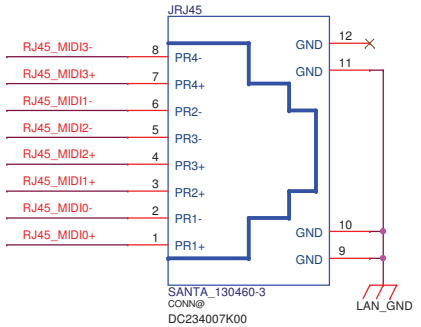
Title: LAN RTL8111H

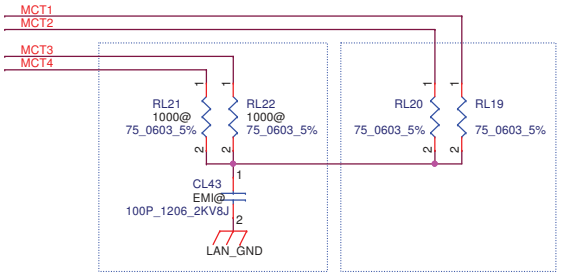
Size: Custom | Document Number: LA-D822P | Rev: 1.0

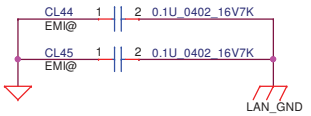
Date: Monday, June 06, 2016 | Sheet 30 of 46

Main Func = LAN









Security Classification	Compal Secret Data		
Issued Date	2012/04/27	Deciphered Date	2013/04/27

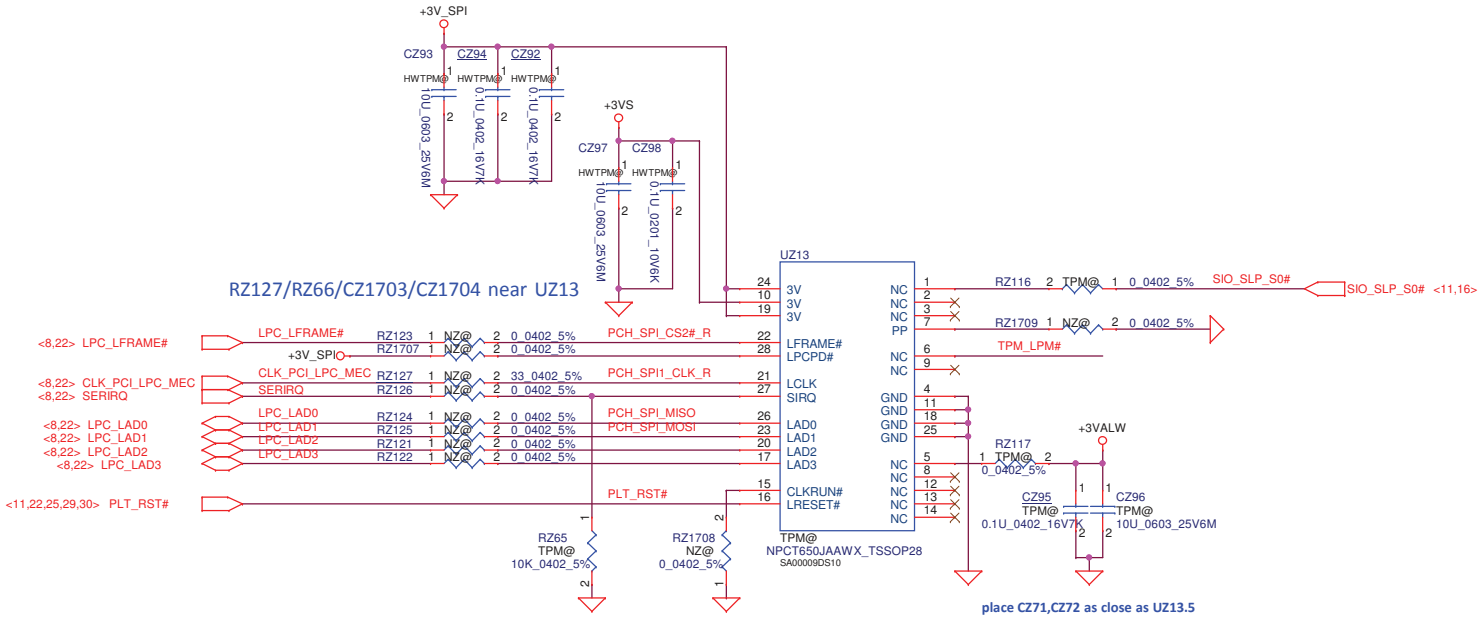
Compal Electronics, Inc.

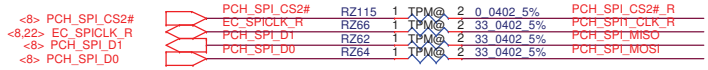
Title: RJ45

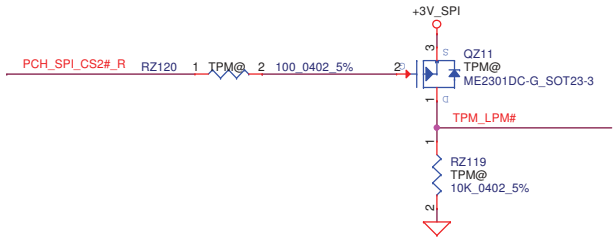
Size	Document Number	Rev
Custom	LA-D822P	1.0

Date: Monday, June 06, 2016 Sheet 31 of 46

Main Func = TPM2.0



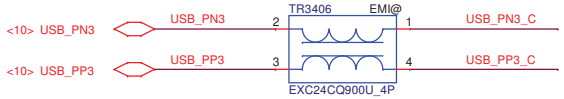


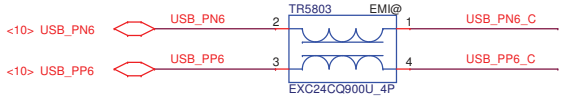


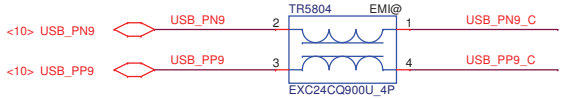
Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	2015/07/21

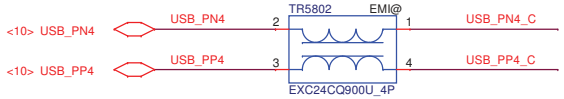
Compal Electronics, Inc.			
Title: TPM2.0			
Size: Custom	Document Number: LA-D822P		Rev: 1.0
Date:	Sheet 32 of 46		

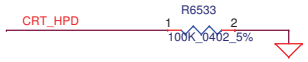
Main Func = IO Connector



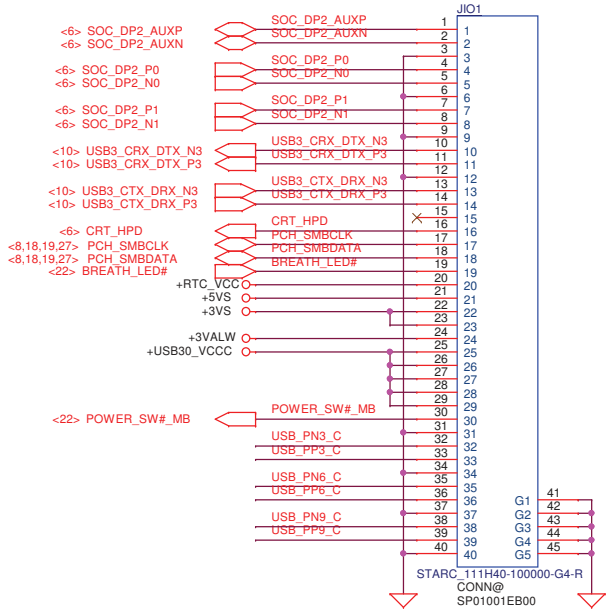


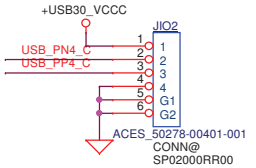






I/O Board Connector





Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: IO Board Conn.

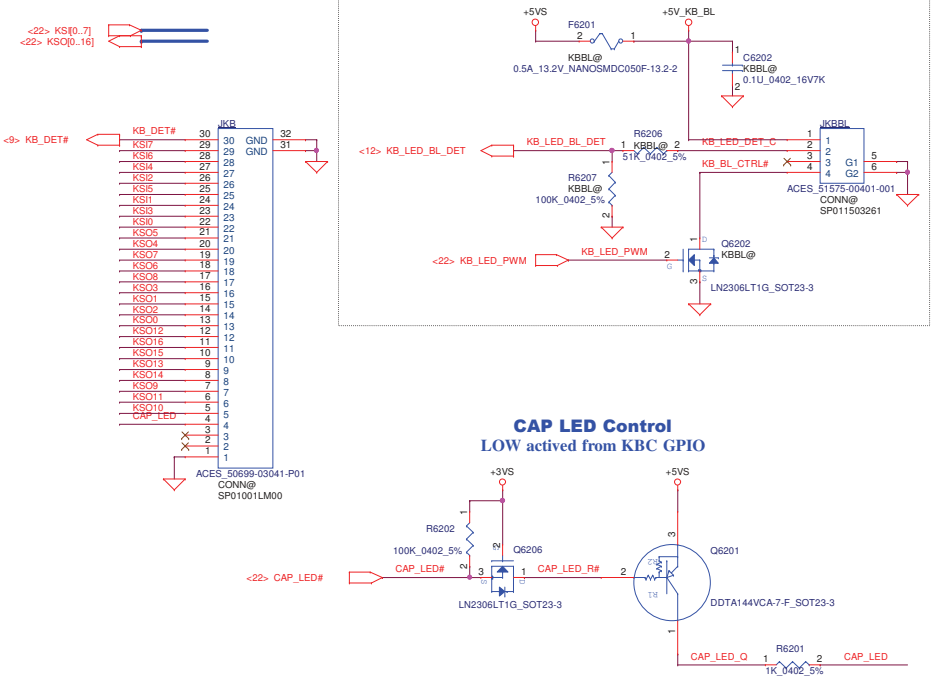
Size	Document Number	Rev
	LA-D822P	1.0

Date: Monday, June 06, 2016 Sheet 33 of 46

Main Func = KB

Keyboard Backlight (Reserved)

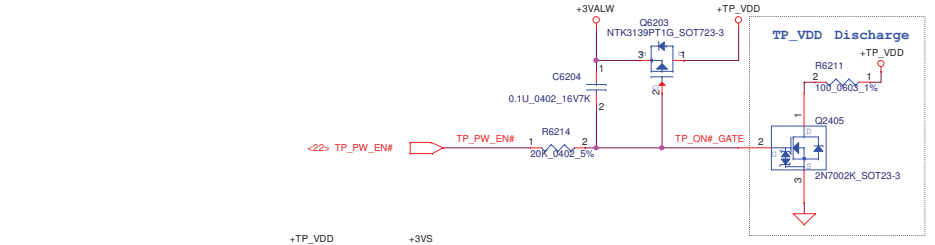
KB Backlight Power Consumption: 285mA max.



CAP LED Control

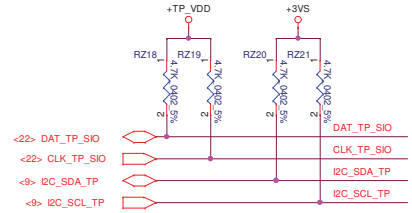
LOW actived from KBC GPIO

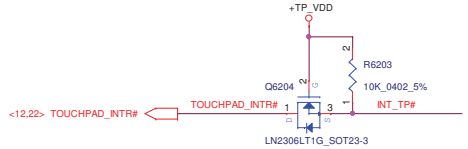
Main Func = TPAD

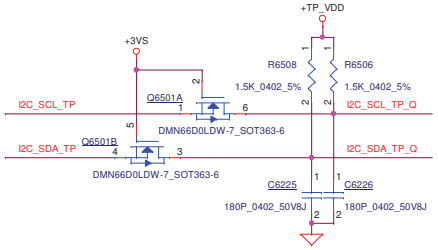


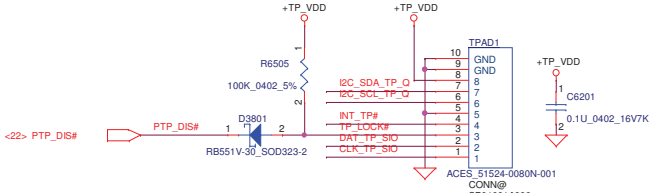
EC/PS2

PCH/I2C

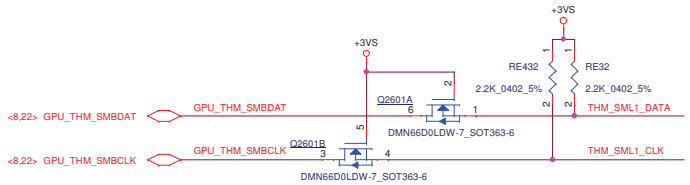


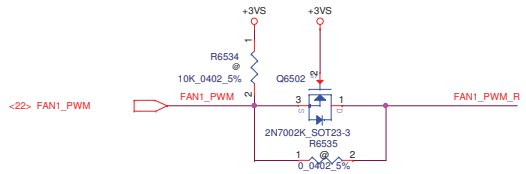


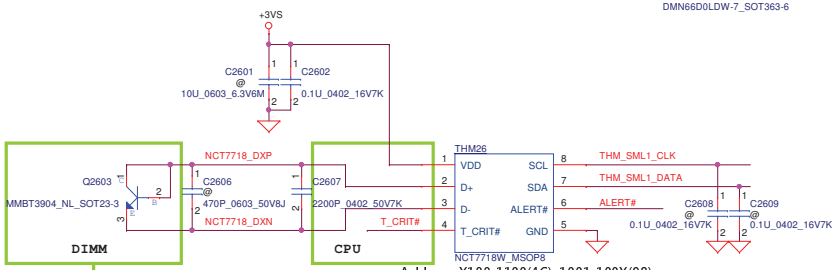




Main Func = Thermal







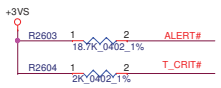
Address: X100_1100(4C), 1001_100X(98)

Layout Note:

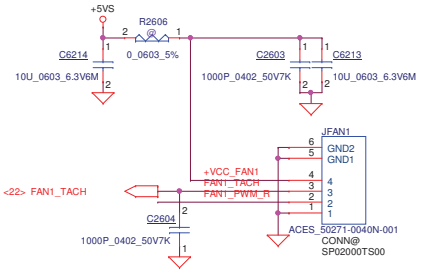
DXN and DXP routing width and spacing is 10 mil / 10 mil.

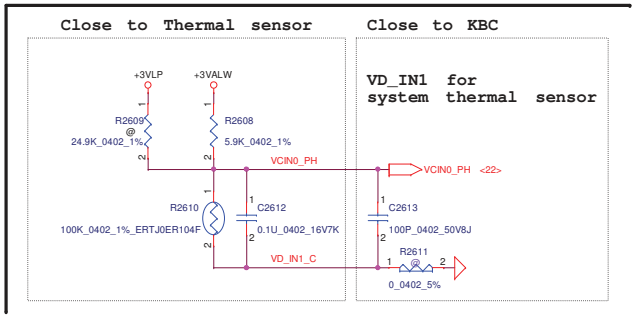
Layout Note:

C2607 close THM26



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

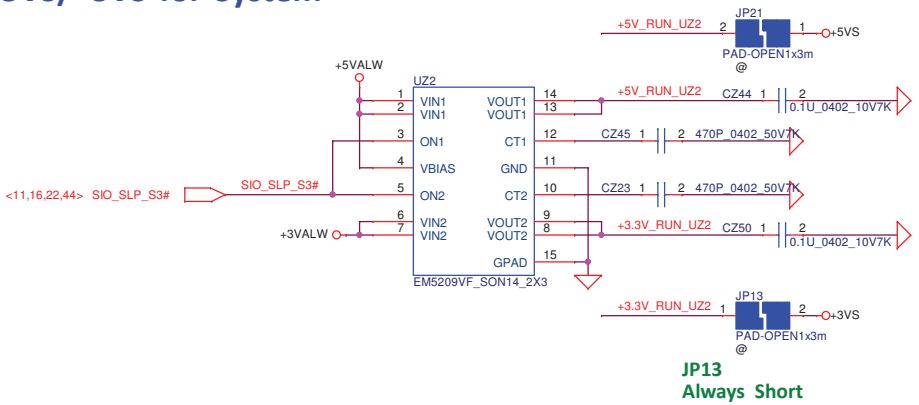




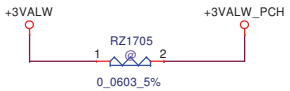
Security Classification	Compal Secret Data	
Issued Date	2015/07/09	Deciphered Date 2016/07/31

Compal Electronics, Inc.		
Title: KB/TP/Thermal/FAN		
Size	Document Number: LA-D822P	Rev: 1.0
Date: Monday, June 06, 2016	Sheet 34 of 46	

+5VS/+3VS for System



+3VALW_PCH for System

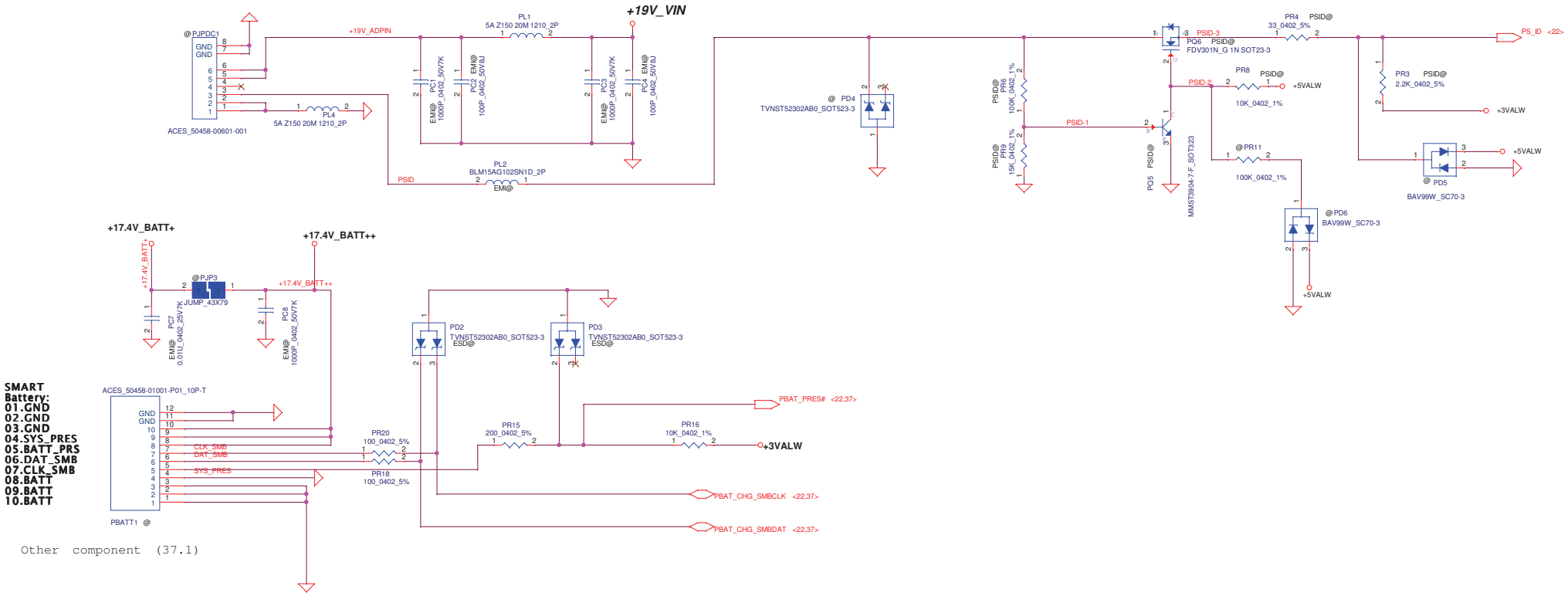


Compal Electronics, Inc.

Title: DC to DC

Size | Document Number: LA-D822P | Rev: 1.0

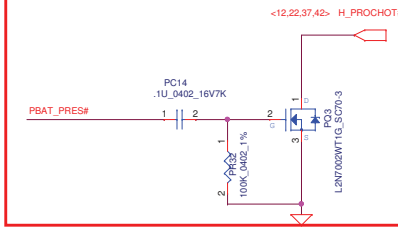
Date: Monday, June 06, 2016 | Sheet 35 of 46



Other component (37.1)

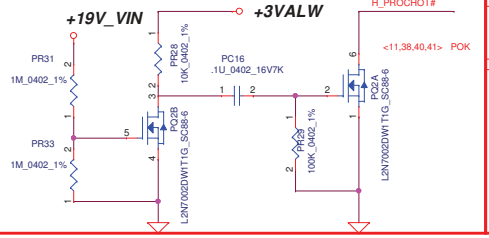
Adapter protection

if battery removed, adaptor only, then trigger the H_PROCHOT#, keep @ in BOM since battery can not be removed by end user

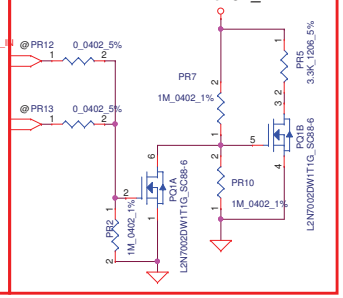


Battery protection

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC



Erp lot6 Circuit



15W_U22(SKL)
X63:PSID@/U22_SKL@/15W@_U22
X4P:EMI@/ESD@/RF@

15W_U22(KBL)
X63:PSID@/U22_KBL@/15W@_U22
X4P:EMI@/ESD@/RF@

28W_U23e
X63:PSID@/U23@/28W@
X4P:EMI@/ESD@/RF@

15W_U23e(Unused)
X63:PSID@/U23@/15W@_U22/15W@_U23
X4P:EMI@/ESD@/RF@

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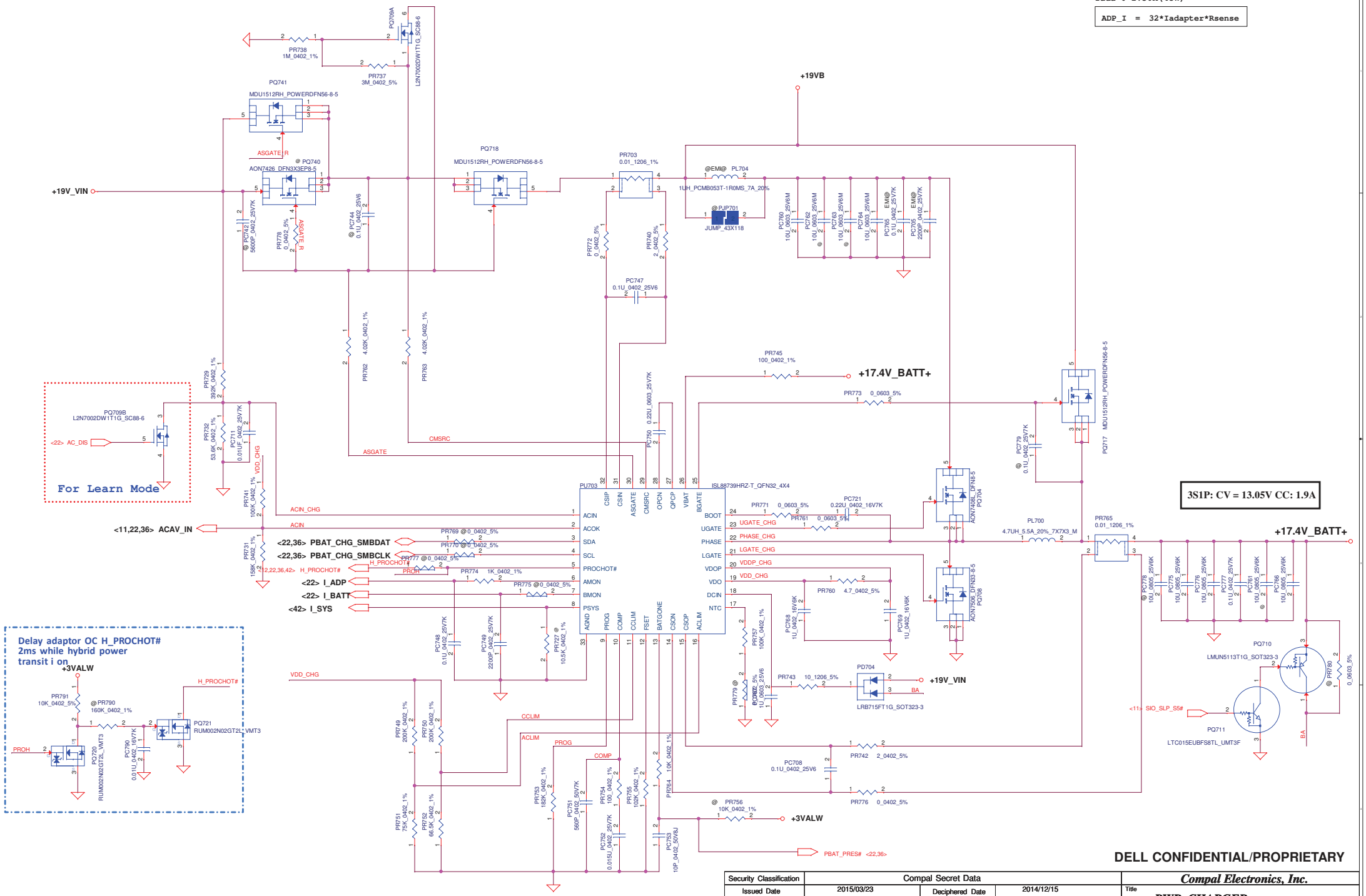
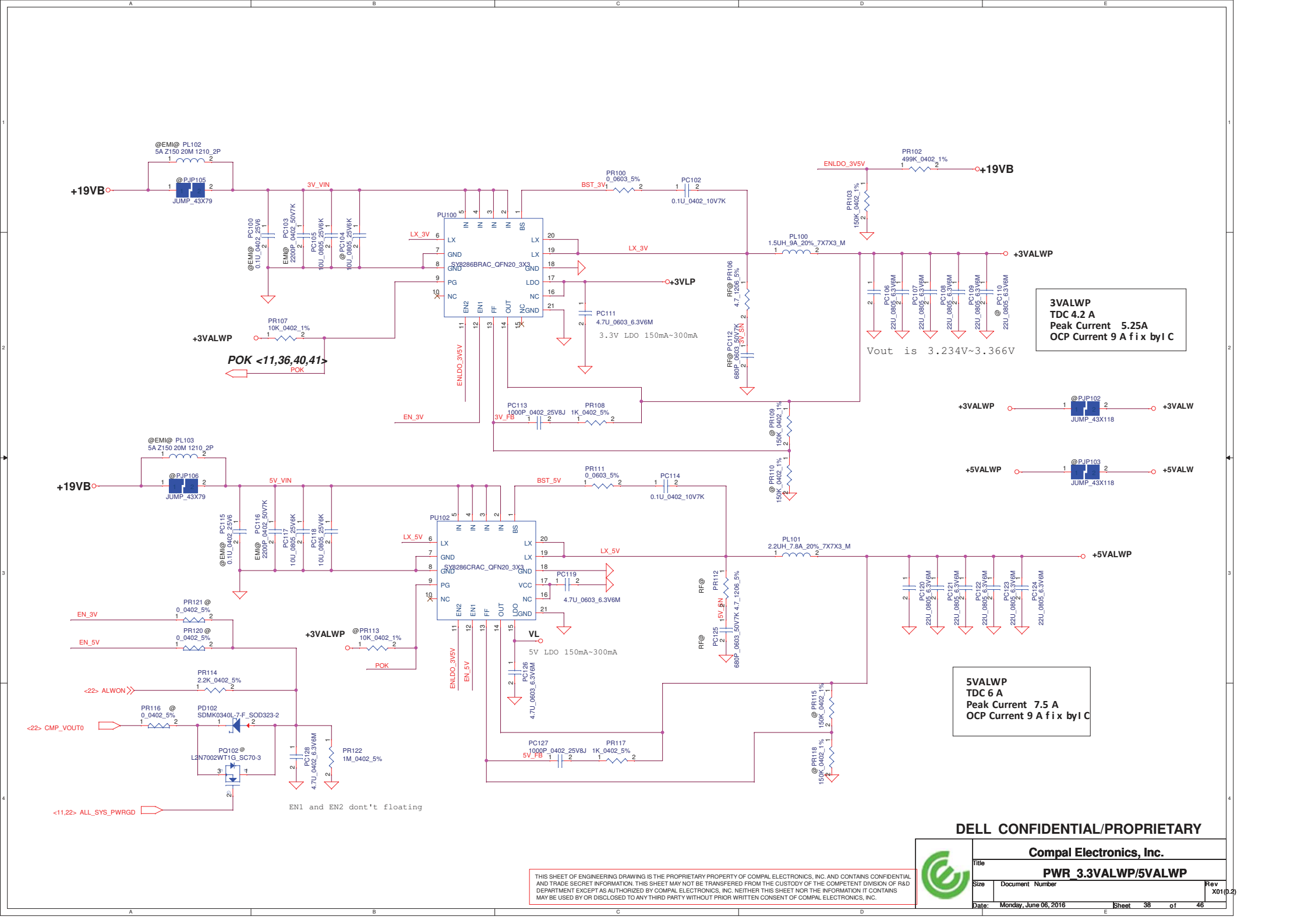
Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.			
Title	PWR_DCIN/BATT CONN/OTP		
Size	Document Number		Rev X01(0.2)
Date: Monday, June 06, 2016		Sheet 36 of 46	





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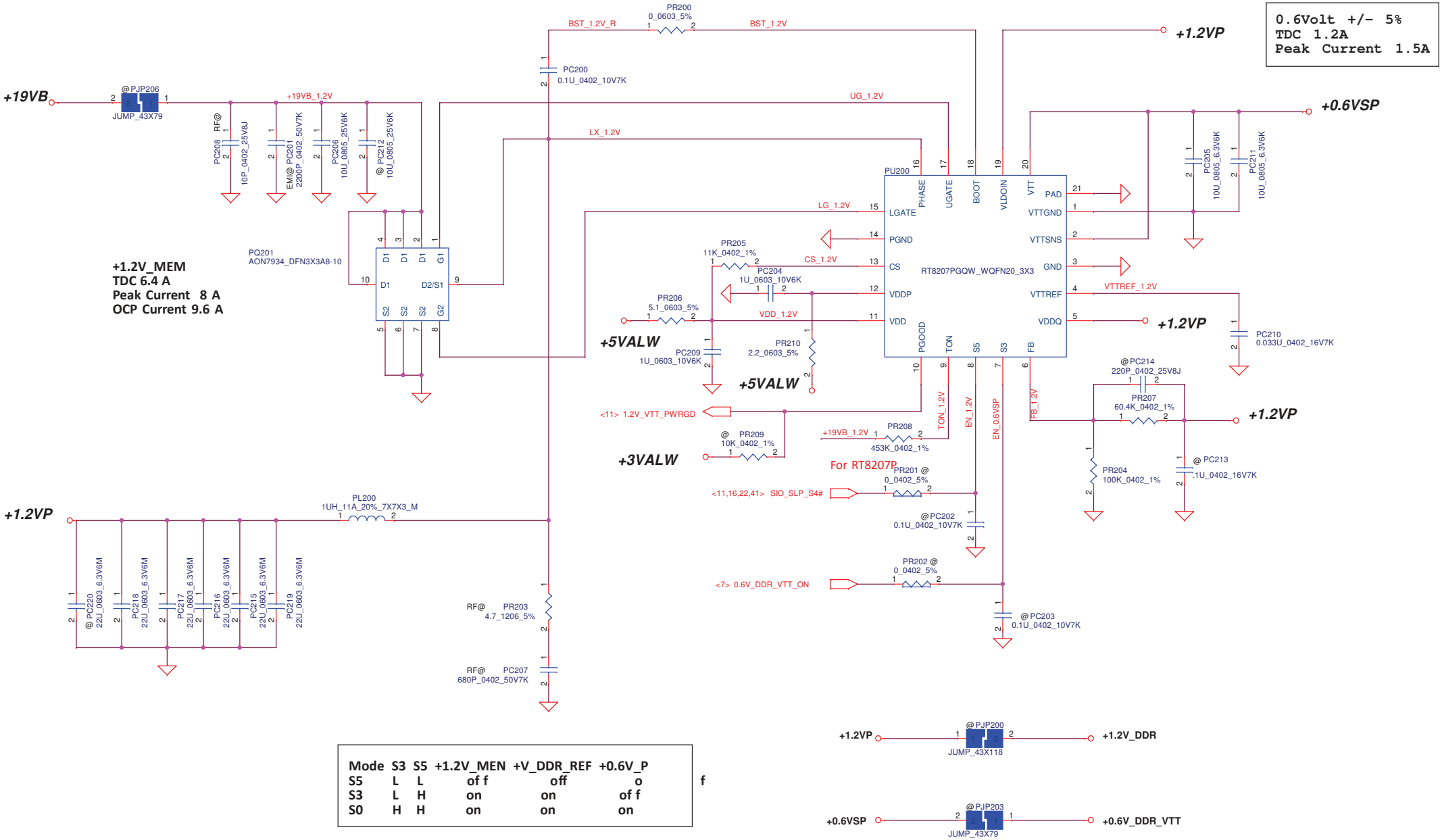
Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

Size | Document Number | Rev X01(0.2)

Date: Monday, June 06, 2016 | Sheet 38 of 46



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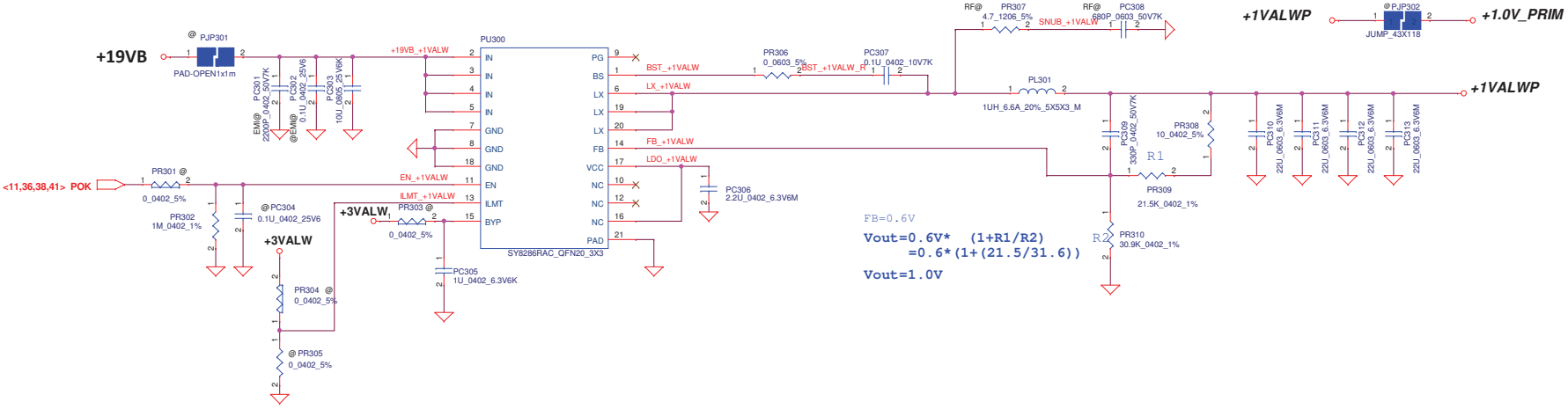
Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Title: PWR_+1.2V_MEN/+0.6V_DDR_VTT

Size	Document Number	Rev
Custom		X01(0.2)

Date: Monday, June 06, 2016 Sheet 39 of 46



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

OCP setting	ILMT(pin3)
6A	Pull low
9A	Floating
12A	Pull high

+1.0V_PRIM
TDC 6 A
Peak Current 8.6 A
OCP Current 12 A Fix by IC

	TYP	MAX
Choke DCR	11.0mohm ,	12.0mohm

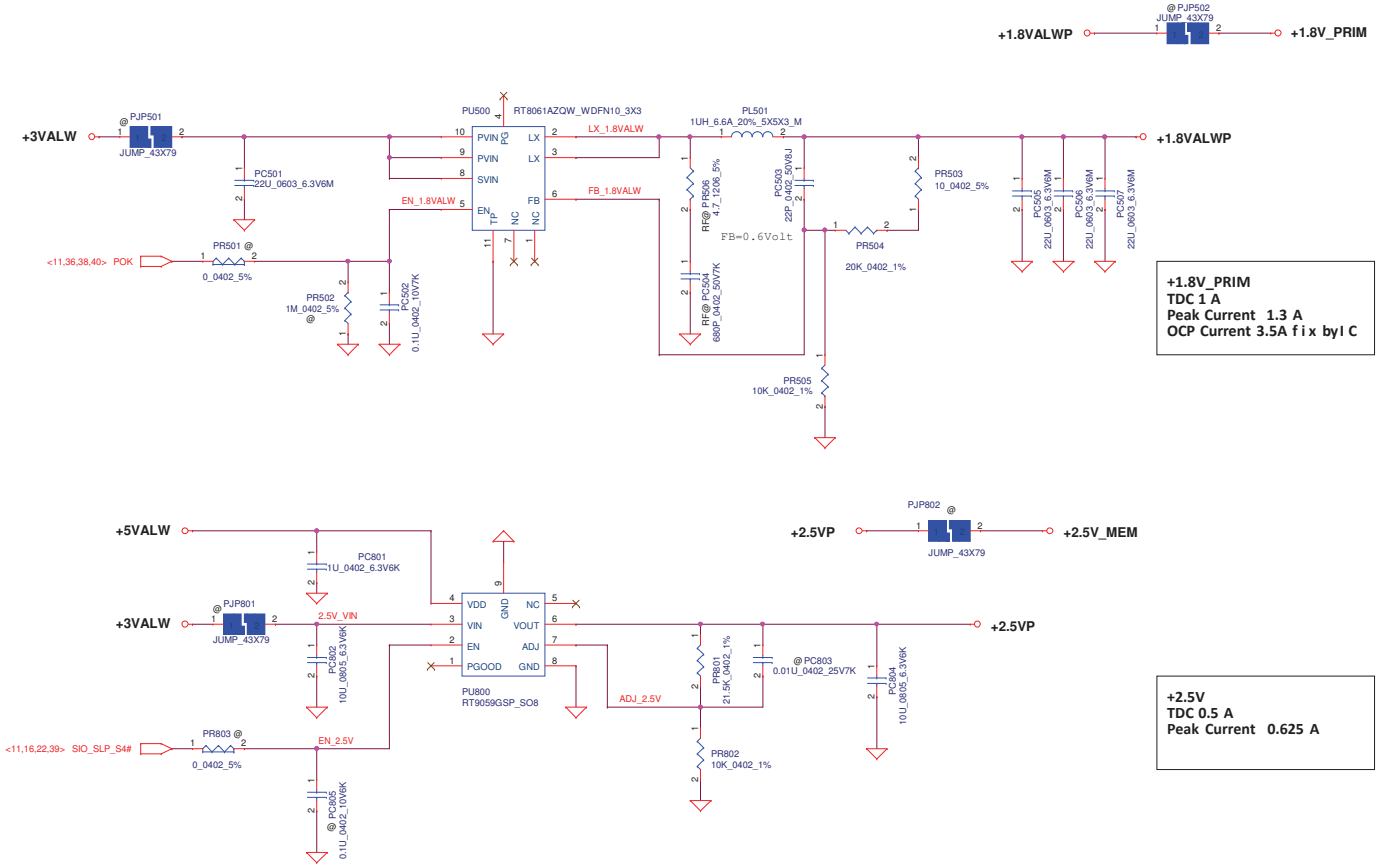
Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: PWR_+1VALWP

Size	Document Number	Rev
C		X01(0.2)

Date: Monday, June 06, 2016 Sheet 40 of 46



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Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: PWR_+1.8V_PRIM and +2.5V

Size	Document Number	Rev
C		XD1(0.2)

Date: Monday, June 06, 2016 | Sheet 41 of 46

VCC_SA
Loadline : 10.3m-ohm

TDC 5A
Peak Current 5A
OCP current 7A
Choke DCR 12 +-5%m ohm

VCCSA_B+ — @ PJP603 — PAD-OPEN1x1m — CPU_B+

Local sense put on HW site

+1.0V_VCCST

PU602 ISL95859HRTZ-T_TQFN40_5X5

PU606 ISL95808HRZ-TS2378_DFN8_2X2

AON7934_DFN3X3A-8-10 PQ601

PL601 0.68UH +-20% 7.9A

+VCC_SA

+5VALW

+3VS

VCCSA_B+

	U22@	U23@
PR622	1.96k	2.55K
PR648	1.37K	1.69k
PR629	84.5K	97.6K
PR651	140K	80.6K
PR608	78.7K	100K
PR638	274	357
PR640	255	301
PC626	0.047U	0.1U
PC621	680P	470P
PR621	1K	316
PC617	220P	390P
PC614	2200P	6800P

Local sense put on HW site

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Security Classification	Compal Secret Data		
Issued Date	2015/12/07	Deciphered Date	2017/01/31

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Compal Electronics, Inc.

Title: PWR_+VCC_SA

Size | Document Number | Rev X00

Date: Monday, June 06, 2016 | Sheet 42 of 46

VCC_core
U22 - 15W
Loadline : 2.4m-ohm
U23e - 15W/28W
Loadline : 2.4m-ohm

15W-U22/U23e
TDC 21A
Peak Current 29A
OCP current 34A
Choke DCR 0.66 +-7%m ohm

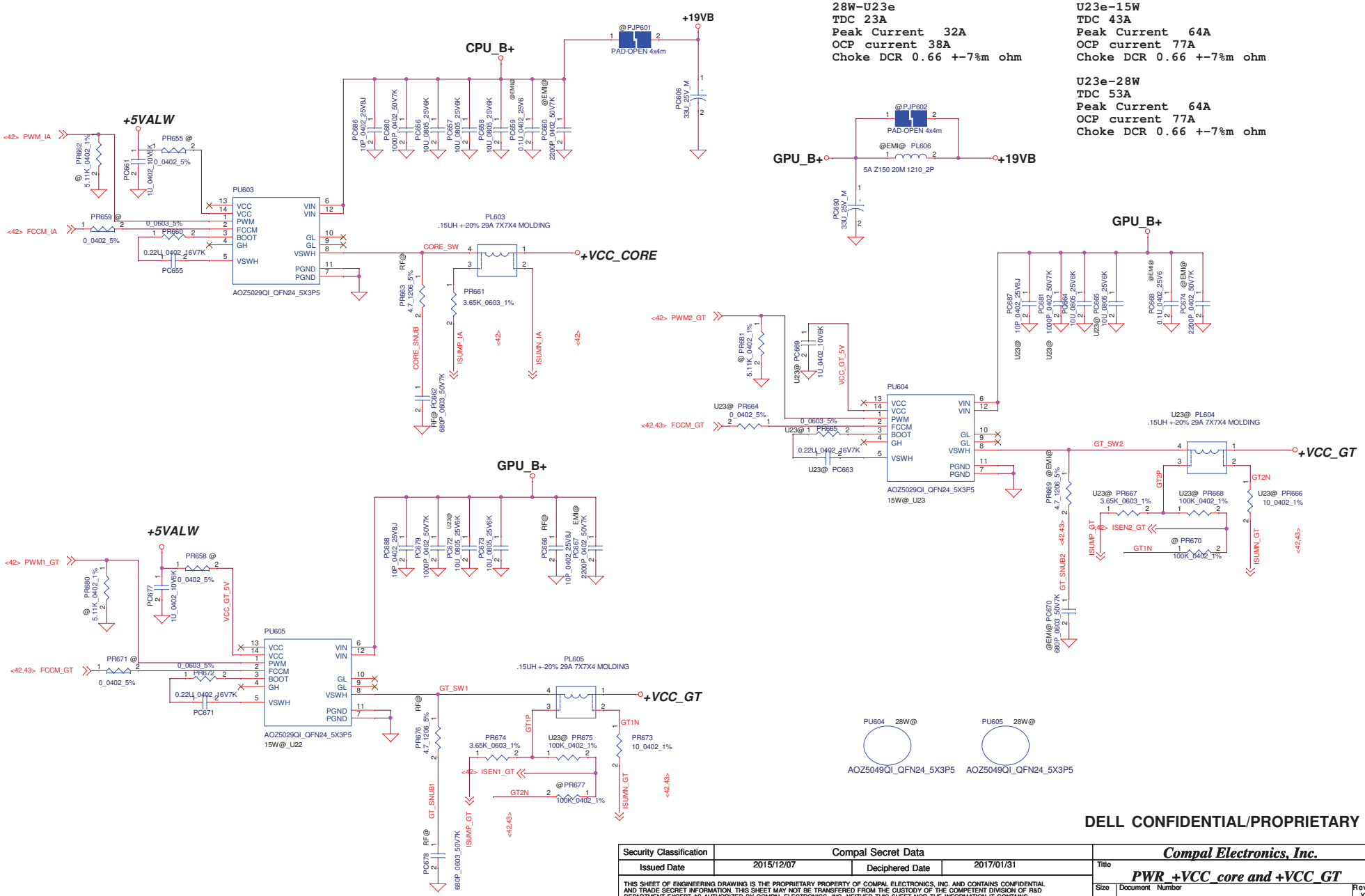
28W-U23e
TDC 23A
Peak Current 32A
OCP current 38A
Choke DCR 0.66 +-7%m ohm

VCC_GT
U22 - 15W
Loadline : 3.1m-ohm
U23e - 15W/28W
Loadline : 2m-ohm

U22-15W
TDC 18A
Peak Current 31A
OCP current 37A
Choke DCR 0.66 +-7%m ohm

U23e-15W
TDC 43A
Peak Current 64A
OCP current 77A
Choke DCR 0.66 +-7%m ohm

U23e-28W
TDC 53A
Peak Current 64A
OCP current 77A
Choke DCR 0.66 +-7%m ohm



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Security Classification	Compal Secret Data		
Issued Date	2015/12/07	Deciphered Date	2017/01/31

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Compal Electronics, Inc.

Title: PWR_+VCC_core and +VCC_GT

Size | Document Number | Rev X00

Date: Monday, June 06, 2016 | Sheet 43 of 46

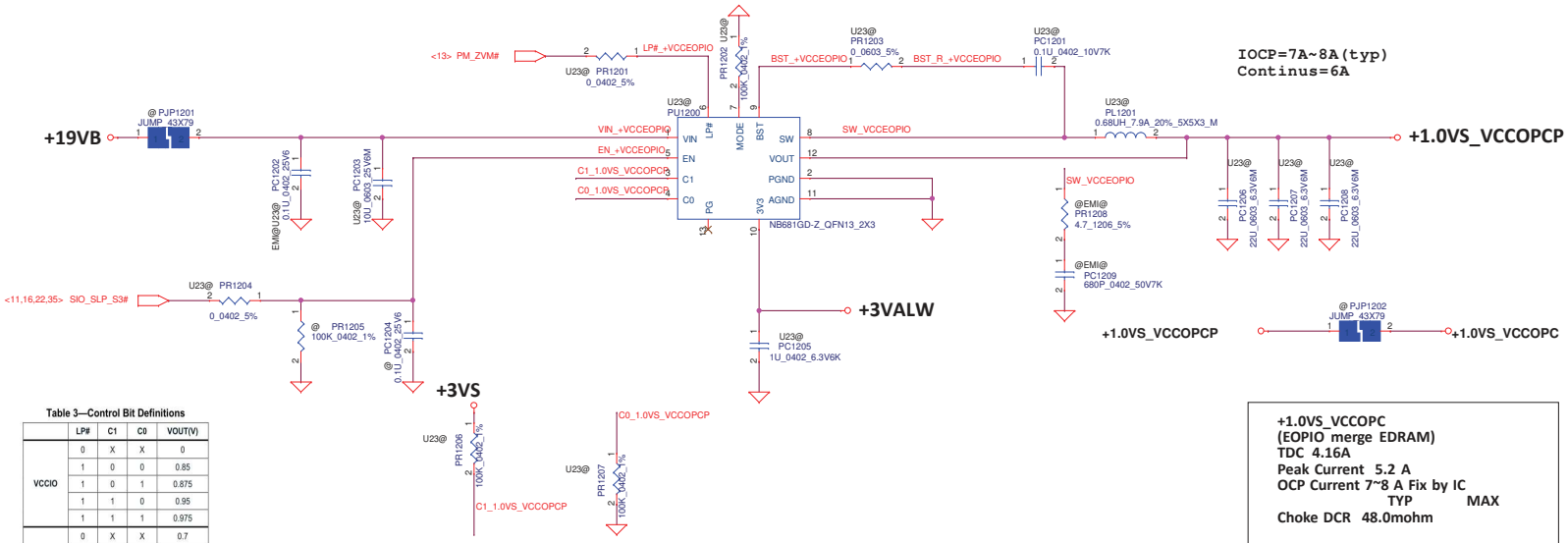


Table 3—Control Bit Definitions

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPCH	0	X	X	0.7
	1	0	0	0.8
	1	0	1	0.85
	1	1	0	0.9
	1	1	1	0.95
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2

+1.0VS_VCCOPC
(EOPIO merge EDRAM)
TDC 4.16A
Peak Current 5.2 A
OCP Current 7~8 A Fix by IC
TYP MAX
Choke DCR 48.0mohm

Security Classification	Compal Secret Data		
Issued Date	2015/12/07	Deciphered Date	2017/01/31

Compal Electronics, Inc.

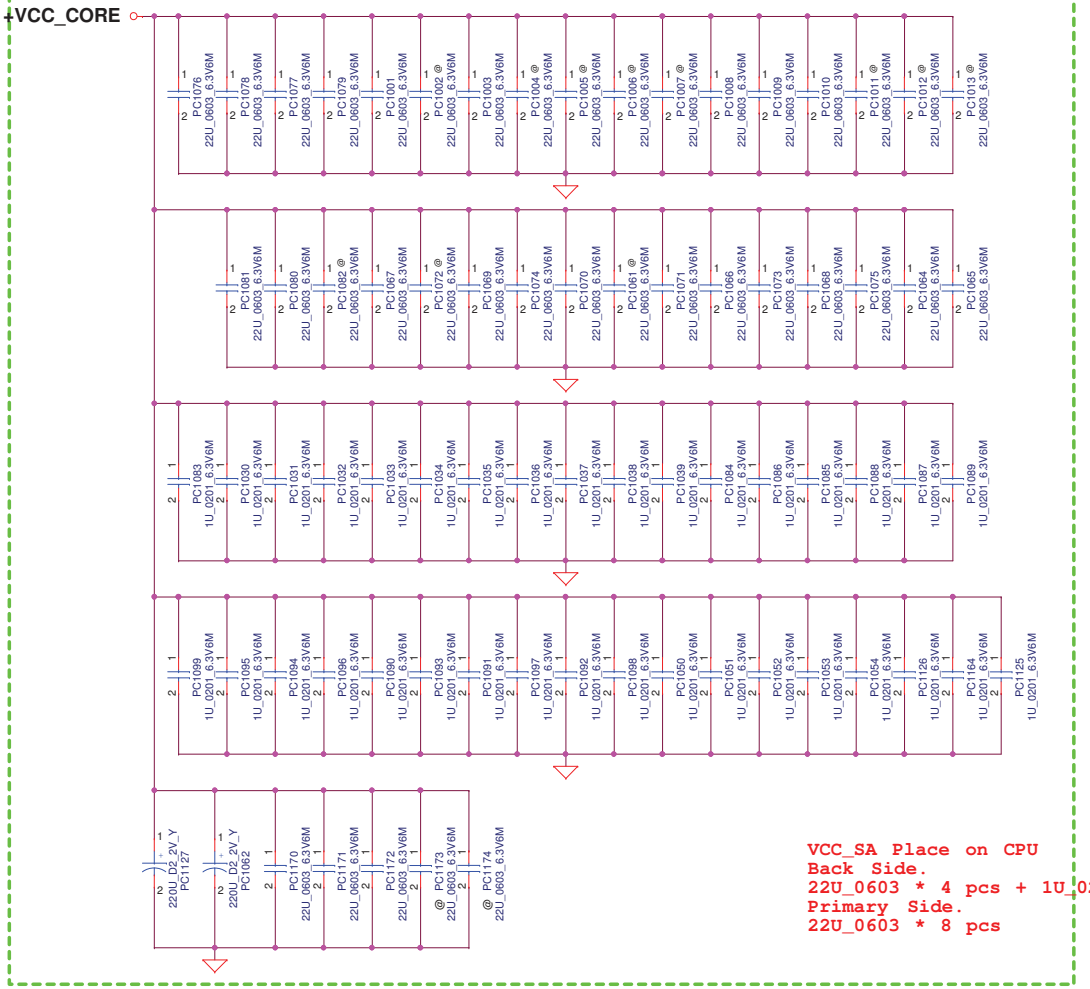
Title: ***PWR_+VCCEDRAM / +VCCEPOIO***

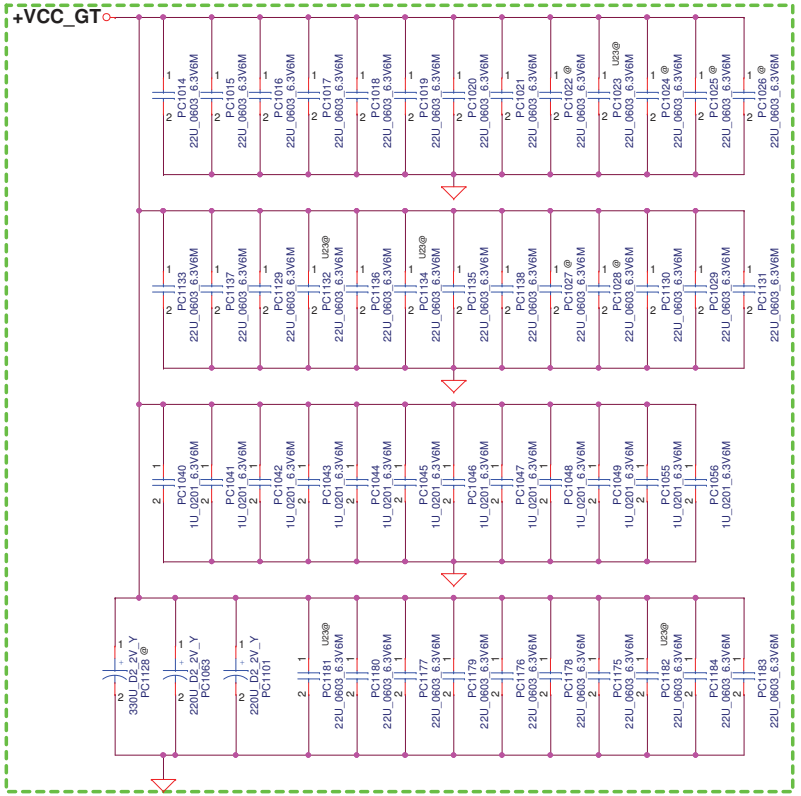
Size	Document Number	Rev
		X00

Date: Monday, June 06, 2016 Sheet 44 of 46

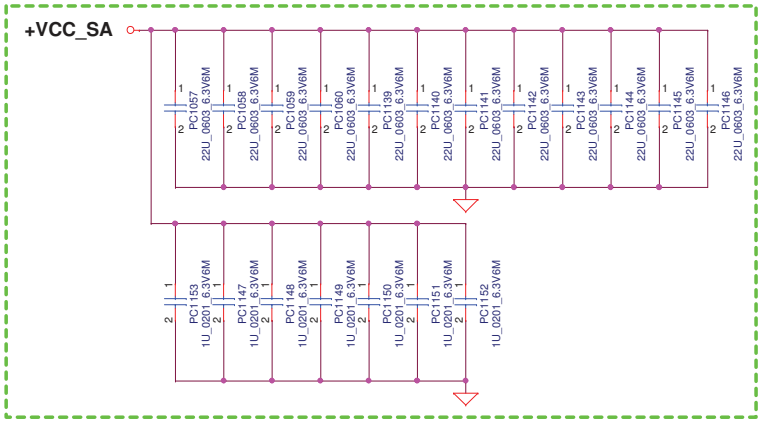
VCC_CORE Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*35 pcs
Primary Side.
22U_0603 * 20 pcs+220u_D2*2 pcs

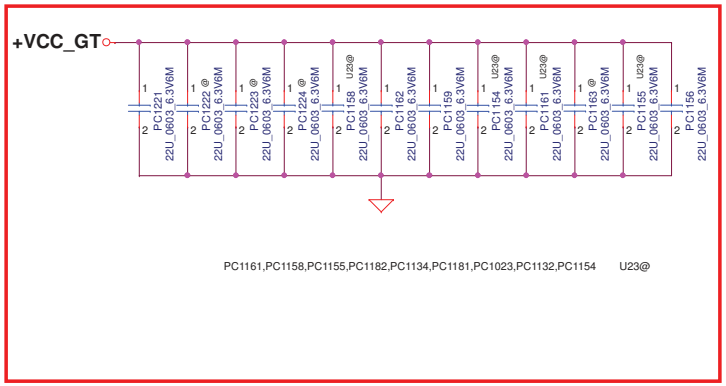
VCC_GT Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*12 pcs
Primary Side.
22U_0603 * 13 pcs +220u_D2*2 pcs





VCC_SA Place on CPU
Back Side.
22U_0603 * 4 pcs + 1U_0201*7 pcs
Primary Side.
22U_0603 * 8 pcs





Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: PWR_CPU&VGA bulk and MLCC

Size	Document Number	Rev
		X00(0.1)

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P37	PWR	20160303	COMPAL	to change charger IC	change charger IC(PU703) to ISL88739	0.2(X01)

2	P39
	P43
	P45
	P46
		PWR	20160303	COMPAL	to prevent RF issue	add PC208
						add PC666,PR676,PC678
						add PC1116,PR1122,PC1109,
						add PC1402,PR1408,PC1408	

3	P42	PWR	20160303	COMPAL	to adjust +VCC_CORE and +VCC_GT load line	change PR622 to 1.91K,PR638 to 287 ohm,PC626 to 0.1uF,PC642 to 0.1uF	
4	P36,P42	PWR	20160303	COMPAL	to save layout space	delete PL3,PL602(reserve location)	
5	P36	PWR	20160303	COMPAL	to fix battery connector ME issue	to change battery connector	
6	P37	PWR	20160304	COMPAL	to fix Temp/Voltage 19.5V DC-IN issue	change PR732 to 53.6K	
7	P44	PWR	20160304	COMPAL	to fix DFB solder open problem	change PC1127,PC1062,PC1128 footprint	
8	P38	PWR	20160308	COMPAL	to prevent OTP functions abnormal issue	to reserve PQ102 and connect to ALL_SYS_PWRGD	
9	P37	PWR	20160316	COMPAL	to save layout space by EMI request	change PC760,PC762,PC763,PC764 to 0603 size and delete PR766,PC767	
10	P43	PWR	20160328	COMPAL	according to test result to adjust VCC_CORE and GT_CORE's load line	to unmount PC624 and PC646	
11	P45	PWR	20160328	COMPAL	according to test result to adjust VCC_CORE and GT_CORE's output MLCC's location(only change BOM) and bulk cap	unmount:PC1021,PC1135,PC1133,PC1131,PC1022,PC1025,PC1027, PC1028,PC1063, PC1008,PC1003,PC1011,PC1072,PC1076,PC1071,PC1081,PC1082,PC1004, PC1007,PC1012 to mount:PC1176,PC1175,PC1177,PC1179,PC1178,PC1180,PC1183,PC1184, PC1170,PC1173,PC1174 to change PC1127,PC1062 to 220uF/9m ohm	
12	P36	PWR	20160429	COMPAL	To improve EMI and reduce inrush current to mount π filter' s bead and change cap	unmount:PL1,PL4 change:PC2,PC4 to 100pF	
13	P37	PWR	20160429	COMPAL	ISL88739 doesn't support PSYS function	unmount:PR727 change PR774 to 1K ohm change PC748 0.1uF	
14	P39	PWR	20160429	COMPAL	to adjust 1.2V OCP to 10.2A	change PR205 to 11K	
15	P37	PWR	20160429	COMPAL	to aviod inrush to damage MOS	to reserve PQ741	0.3(X02)

Security Classification	Compal Secret Data		
Issued Date	2015/07/15	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: PWR_Change list

Size | Document Number | Rev 1.0(A00)

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