COMPAL
CONFIDENTIAL

MODEL NAME : CAP00

PCB NO : LA-E311P

BOM P/N : 431A4X31L01

GPIO MAP: Gen7 GPIO Master_XXXX

CRANE15

Kaby Lake H-type (2 chip)

REV : 1.0(A00)

2016.11.21

@ : Nopop Component

EMC@ : EMI/ESD/RF part

CONN@ : Connector Component

XDP@ : Total debug Component (pop them until ST)

Layout Dell logo

REV: X00
PWB: XXXXX
DATE: 1403-06

PCB 1TS LA-E311P REV0 MB 1

Part Number	Description
DAA000CS010	PCB 1TS LA-E311P REV1 MB 1

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Title: Cover Sheet

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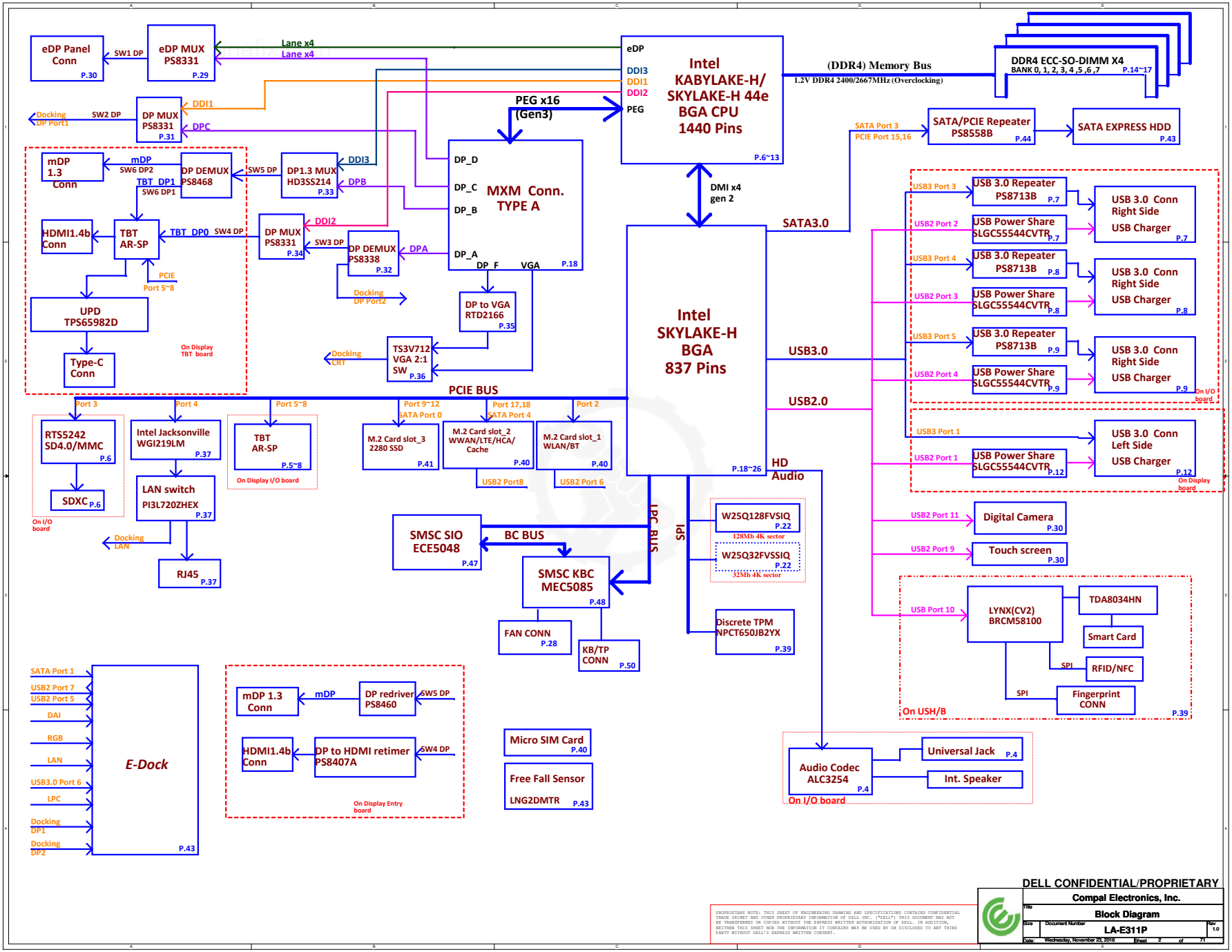

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE			RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane / State	+PWR_SRC +5V_ALW +3.3V_ALW +3.3V_ALW2 +3.3V_ALW_DSW +3.3V_ALW_PCH +3.3V_RTC_LDO +1.8V_ALW +1.0V_PRIM	+3.3V_SUS +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +3.3V_MXM +5V_MXM +MXM_PWR_SRC		(M-OFF) +VCC_CORE +VCC_EDRAM +VCC_EOPIO +VCC_GTU +VCC_GT +1.0V_VCCSTG +VCC_SA
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

Stack up

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil
			SolderMask	IT-158
			Add Plating	
1	Top		Copper foil	0.5oz
		3.7	Prepreg	1080
2	GND/PWR		Copper foil	1oz
		3.7	Core	4mil
3	Sig 1		Copper foil	1oz
		4.1	Prepreg	2116Mx2
4	GND/PWR		Copper foil	1oz
		3.7	Core	4mil
5	Sig 2		Copper foil	1oz
		3.8	Prepreg	1080Hx2
6	Sig 3		Copper foil	1oz
		3.7	Core	4mil
7	GND/PWR		Copper foil	1oz
		4.1	Prepreg	2116Mx2
8	Sig 4		Copper foil	1oz
		3.7	Core	4mil
9	GND/PWR		Copper foil	1oz
		3.7	Prepreg	1080
10	Bottom		Copper foil	0.5oz
			Add Plating	
			SolderMask	
Overall Thickness (1.45mm ± 10%)			57.09	

SATA	DESTINATION
SATA 0	2280 SSD
SATA 1	Dock ESATA
SATA 2	NA
SATA 3	SATAe HDD
SATA 4	M.2 Slot-2 (cache)
SATA 5	NA

USB3.0	DESTINATION
Port 1	Left Side JUSB1
Port 2	M.2 Slot-2 (WWAN/LTE/HCA)
Port 3	Right Side JUSB1
Port 4	Right Side JUSB2
Port 5	Right Side JUSB3
Port 6	Docking

	USB PORT#	DESTINATION
PCH	1	Left Side JUSB1
	2	Right Side JUSB1
	3	Right Side JUSB2
	4	Right Side JUSB3
	5	Docking USB3.0
	6	M.2 Slot-1 (BT)
	7	Docking USB 2.0
	8	M.2 Slot-2 (WWAN/LTE/HCA)
	9	Touch Screen
	10	USH
	11	Camera
	12	NA
	13	NA
	14	NA

USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	M.2 Slot-1 (WLAN)
Lane 3	MMI(Card reader)
Lane 4	10/100/1G LOM
Lane 5~8	TBT-Alpine Ridge
Lane 9~12	M.2 Slot-3(SSD 2280)
Lane 13~14	(Dock ESATA),NA(LANE reservsal)
Lane 15~16	SATA-Express HDD(LANE reservsal)
Lane 17~18	M.2 Slot-2(WWAN/LTE/Optane)

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Title: Index and Config.

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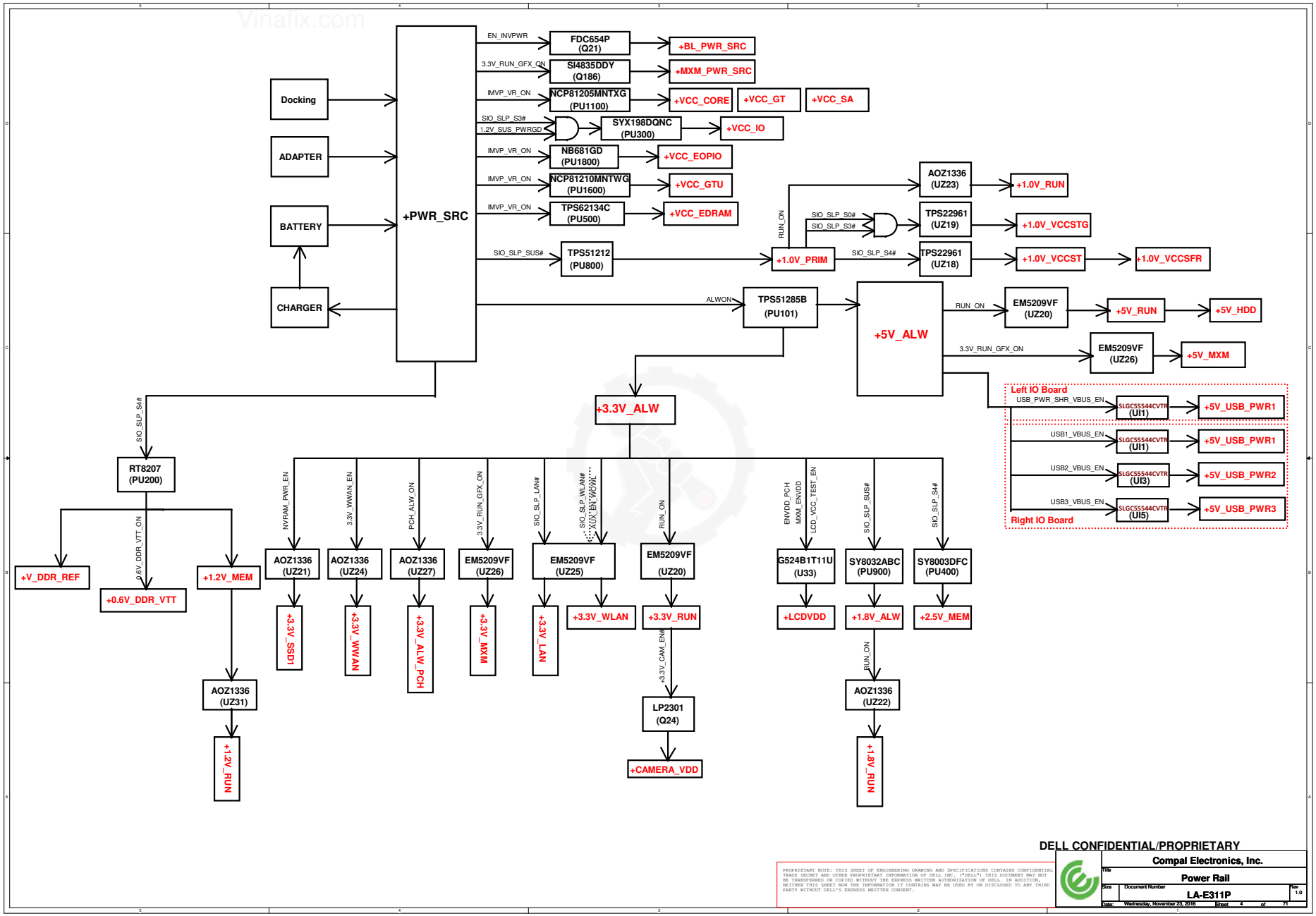

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Title: Power Rail

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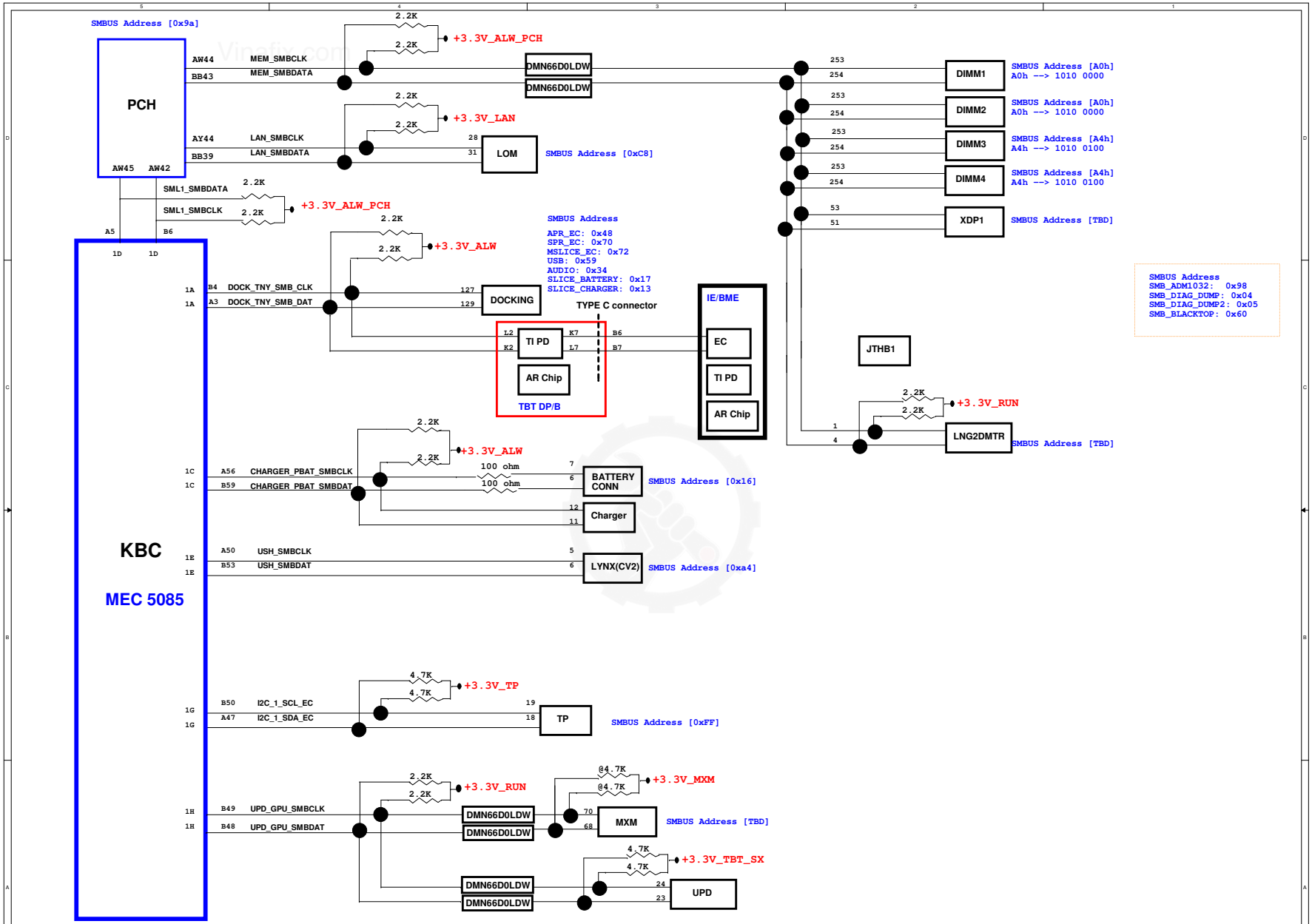

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Title	SMBUS Bolck Diagram
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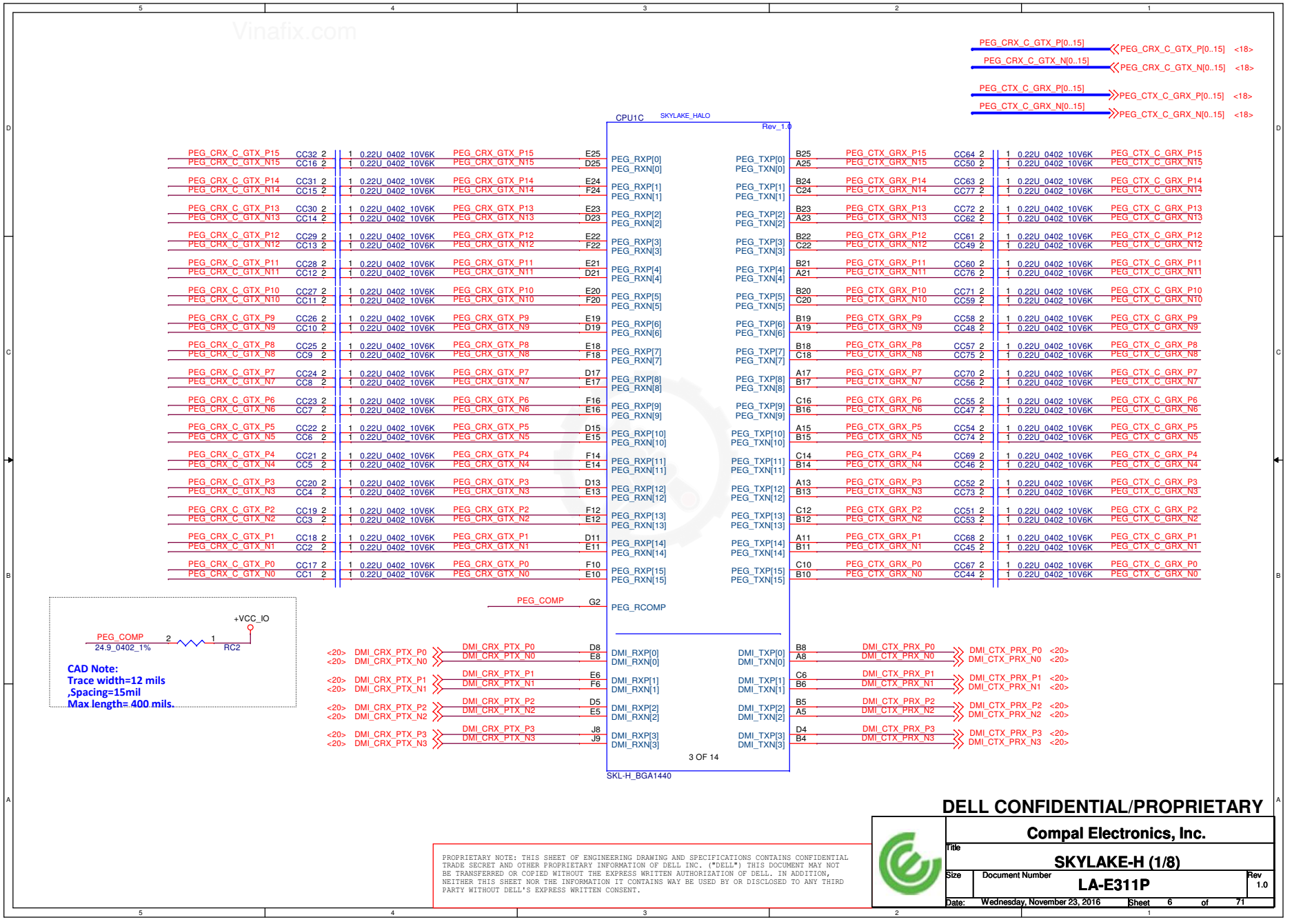

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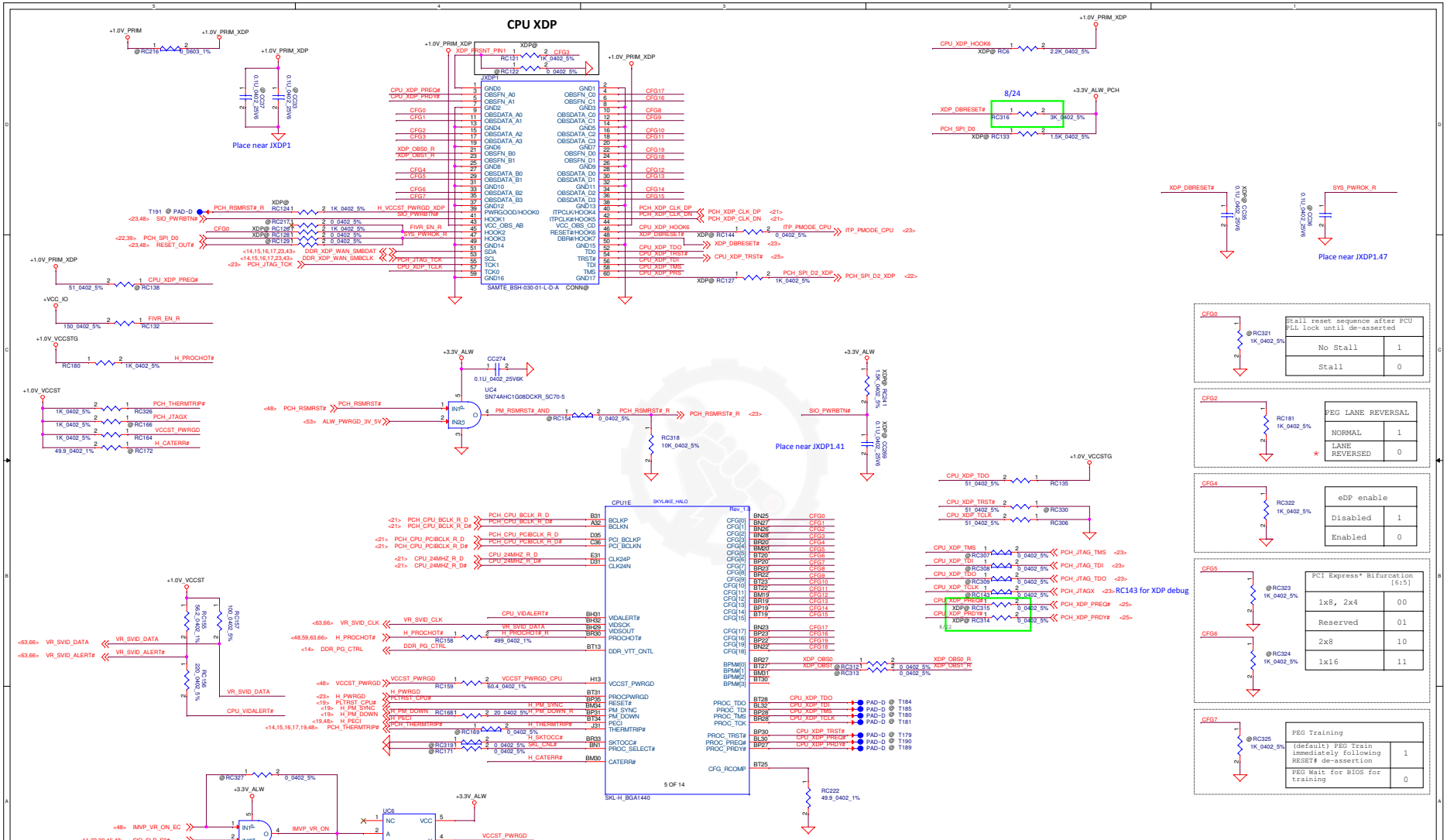
CPU XDP



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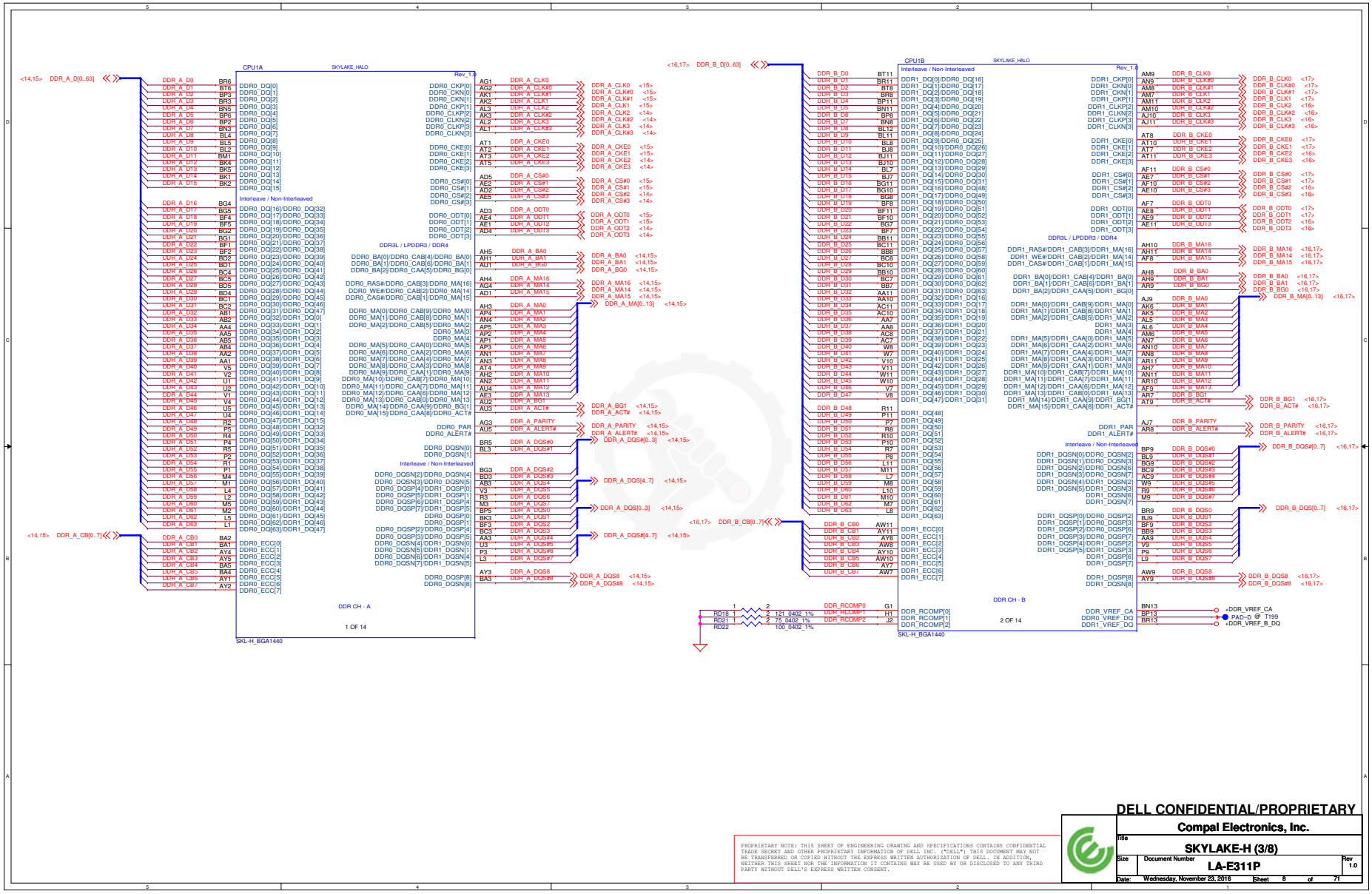

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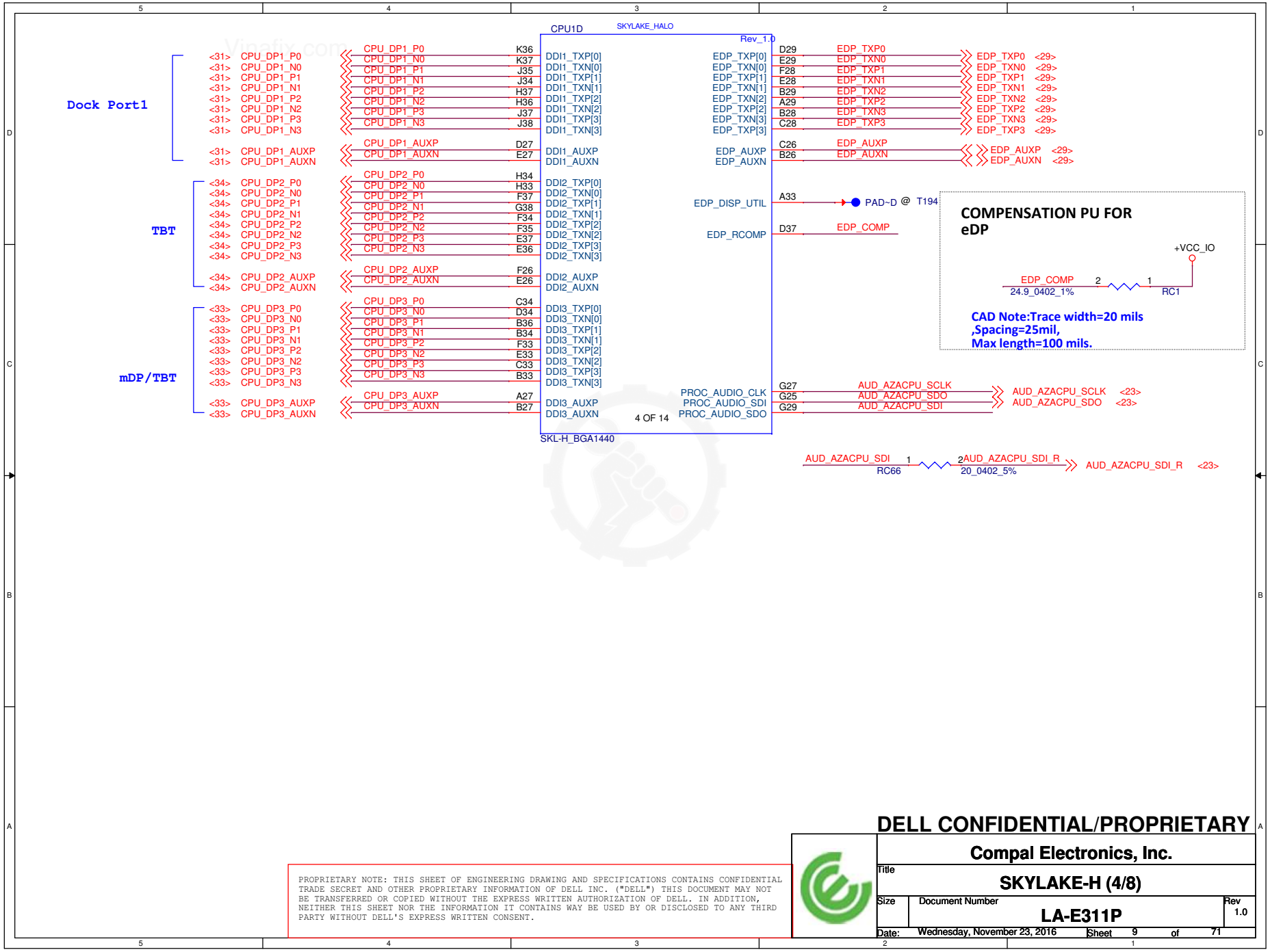

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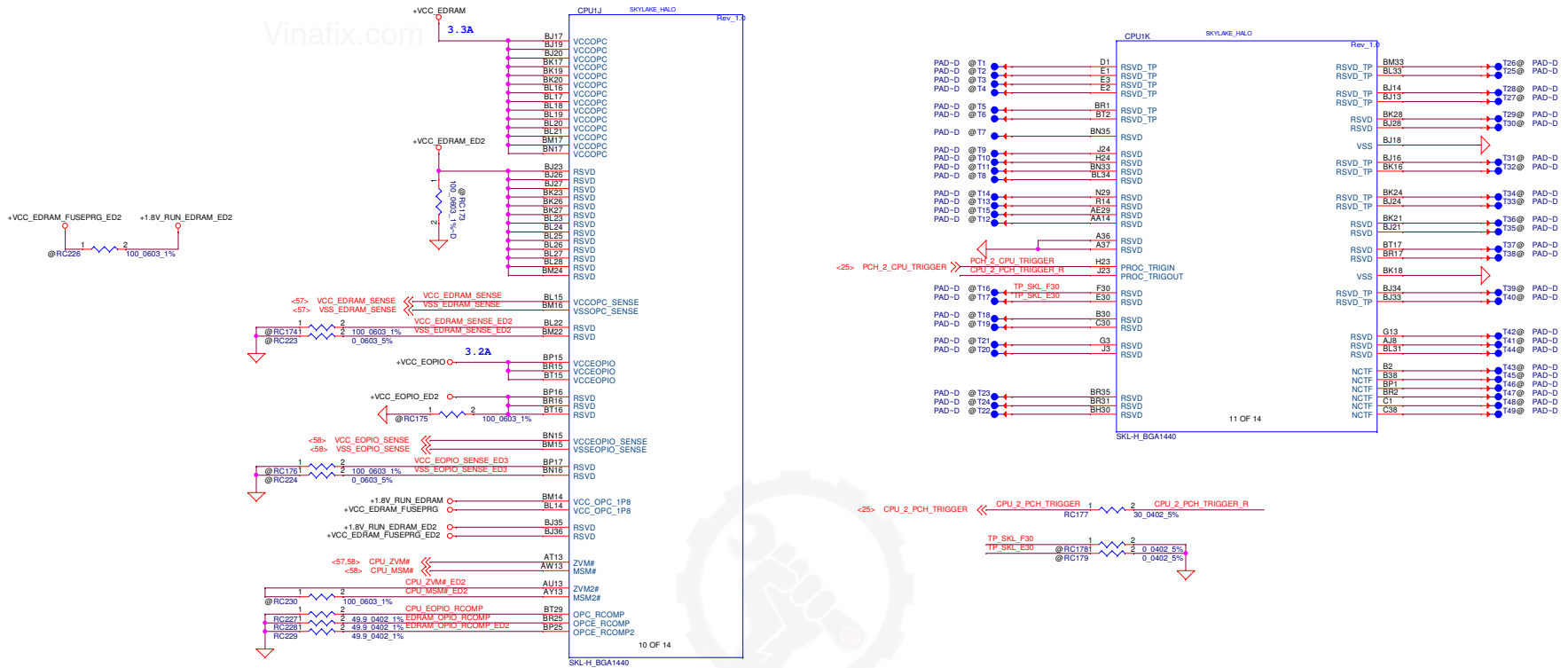

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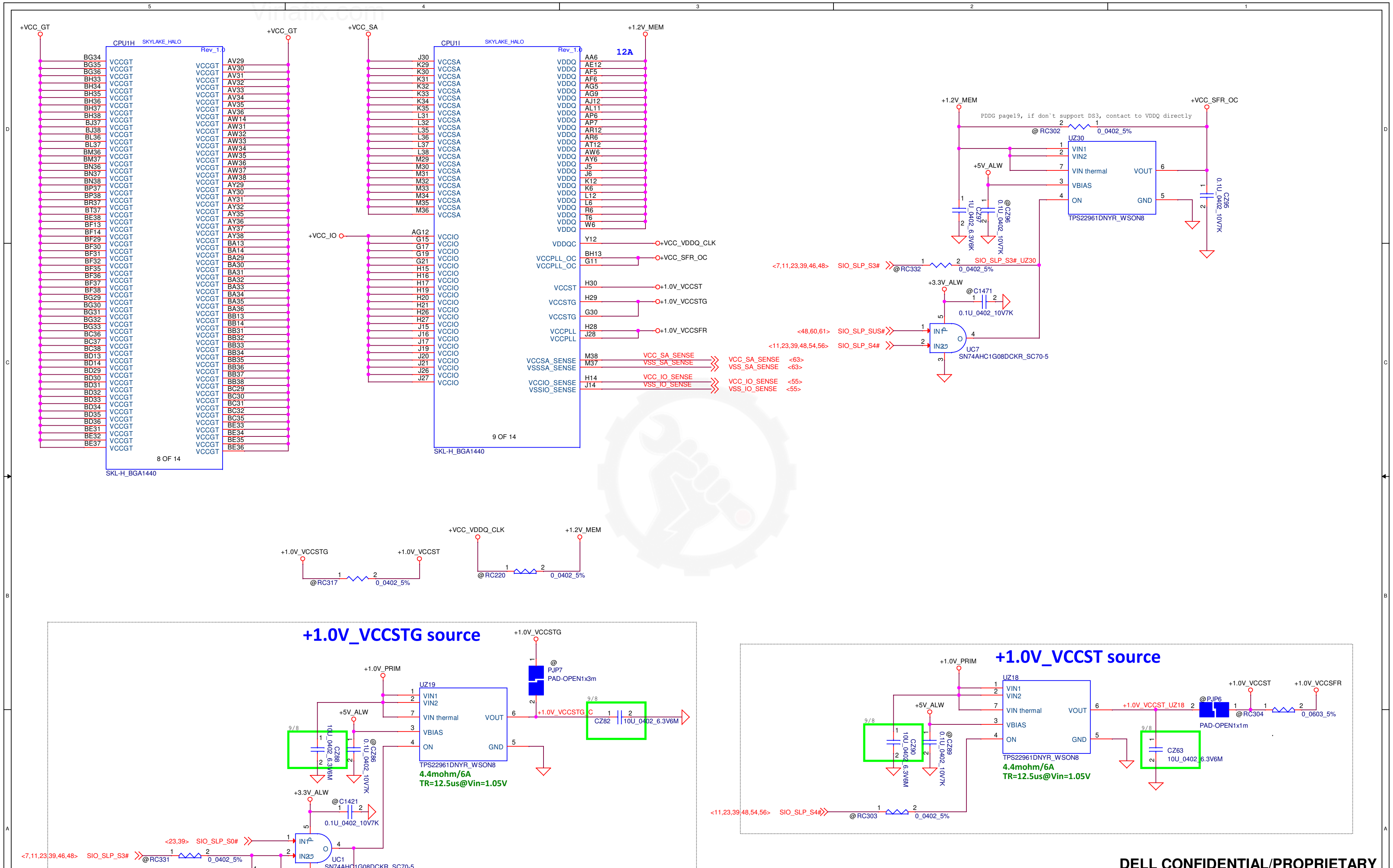

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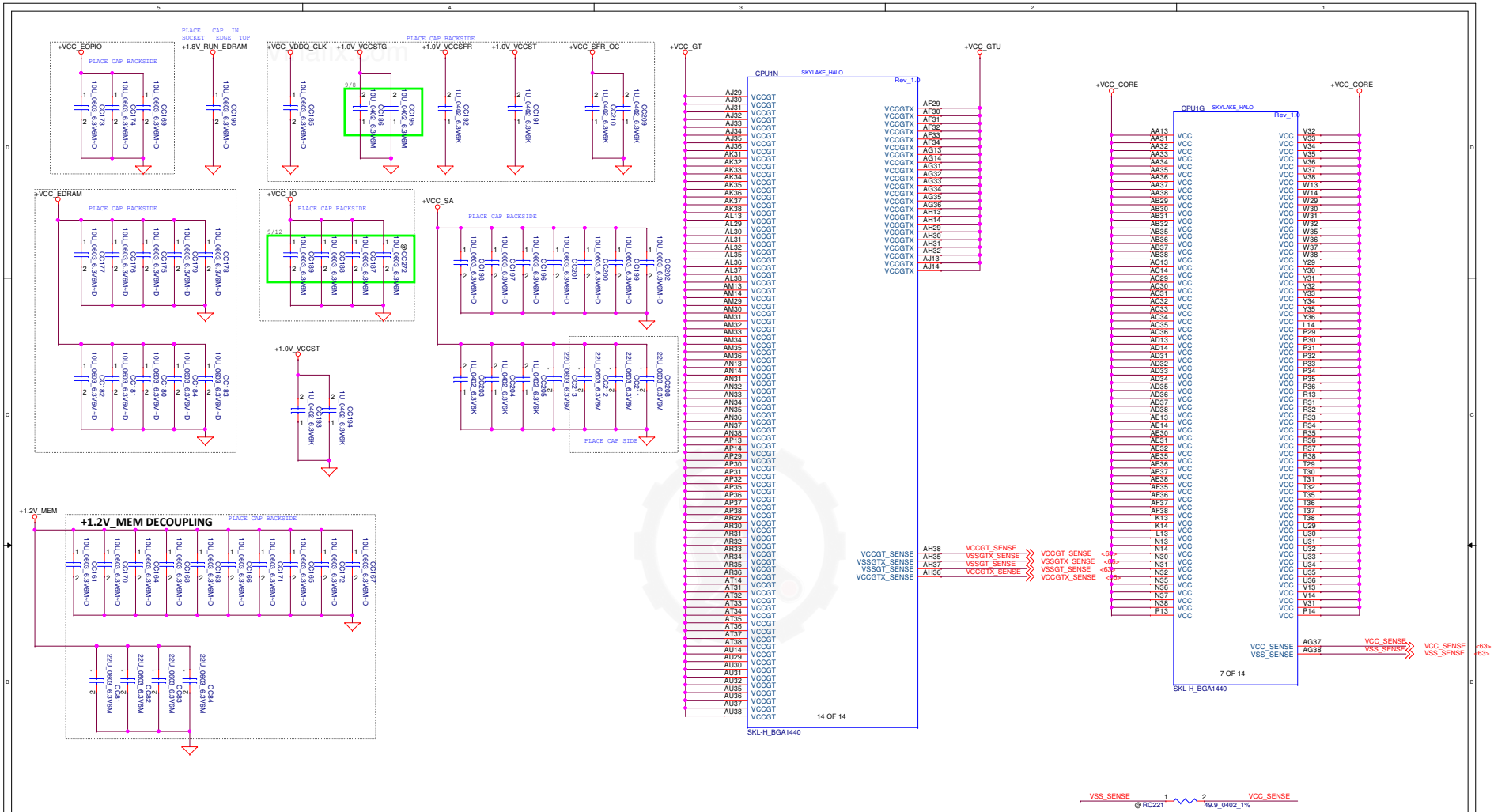

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All VREF traces should have 10 mil trace width

JDIMM1 STD Type H=9.2

Layout Note: Place near JDIMM1.258

DIMM Select

	SA0	SA1	SA2
DIMM2	0	0	0
DIMM4	0	1	0
* DIMM1	1	0	0
DIMM3	1	1	0

CPU

STD JDIMM1 D — Top Side

STD JDIMM3 C — Bottom Side

A JDIMM2 STD

B JDIMM4 REV

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Title: DDRIII-SODIMM SLOT1

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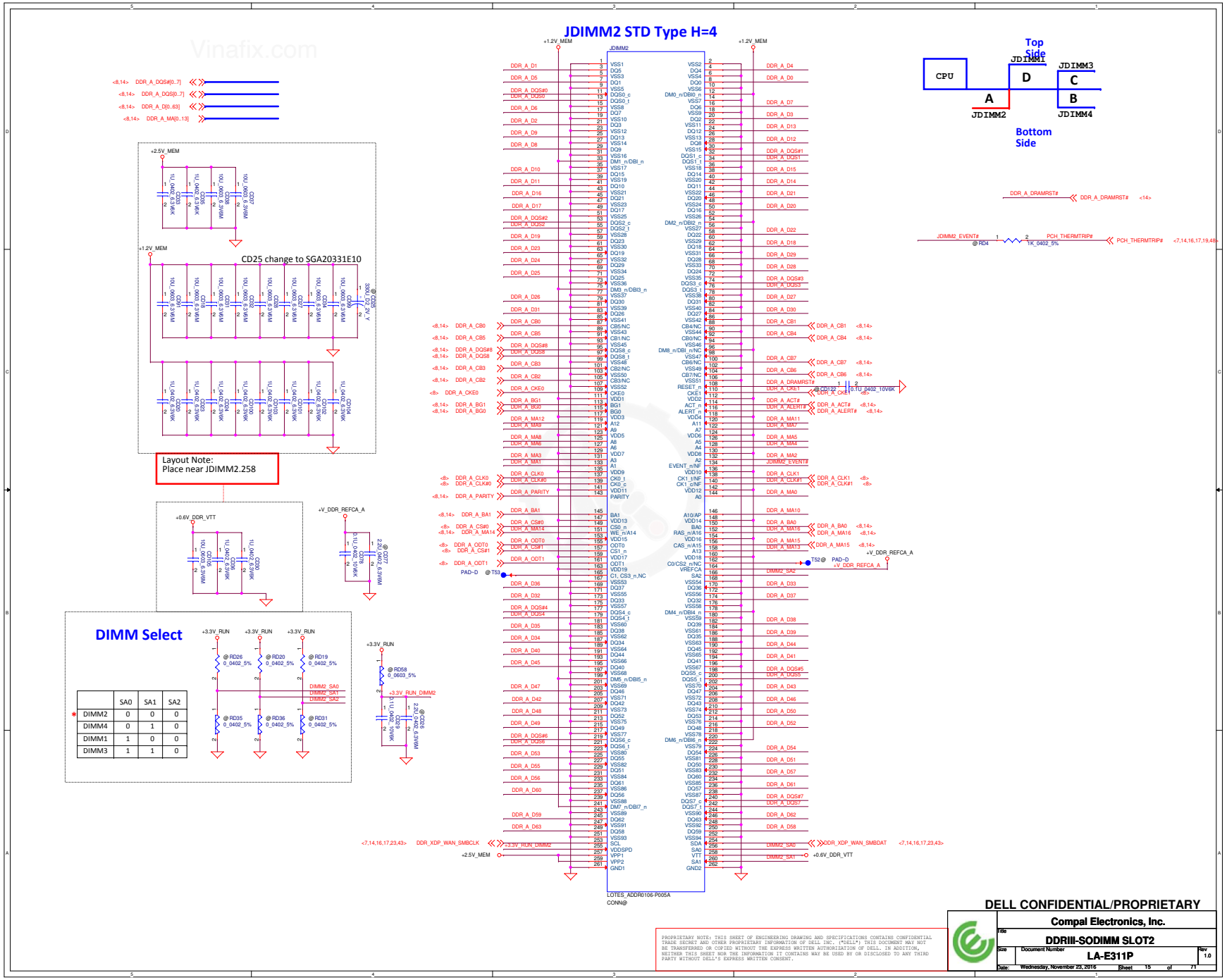
JDIMM2 STD Type H=4
CD25 change to SGA20331E10
Layout Note:
Place near JDIMM2.258
DIMM Select
SA0 SA1 SA2
DIMM2 0 0 0
DIMM4 0 1 0
DIMM1 1 0 0
DIMM3 1 1 0
Top Side
Bottom Side
CPU
JDIMM1
JDIMM3
JDIMM2
JDIMM4
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DDRIII-SODIMM SLOT2
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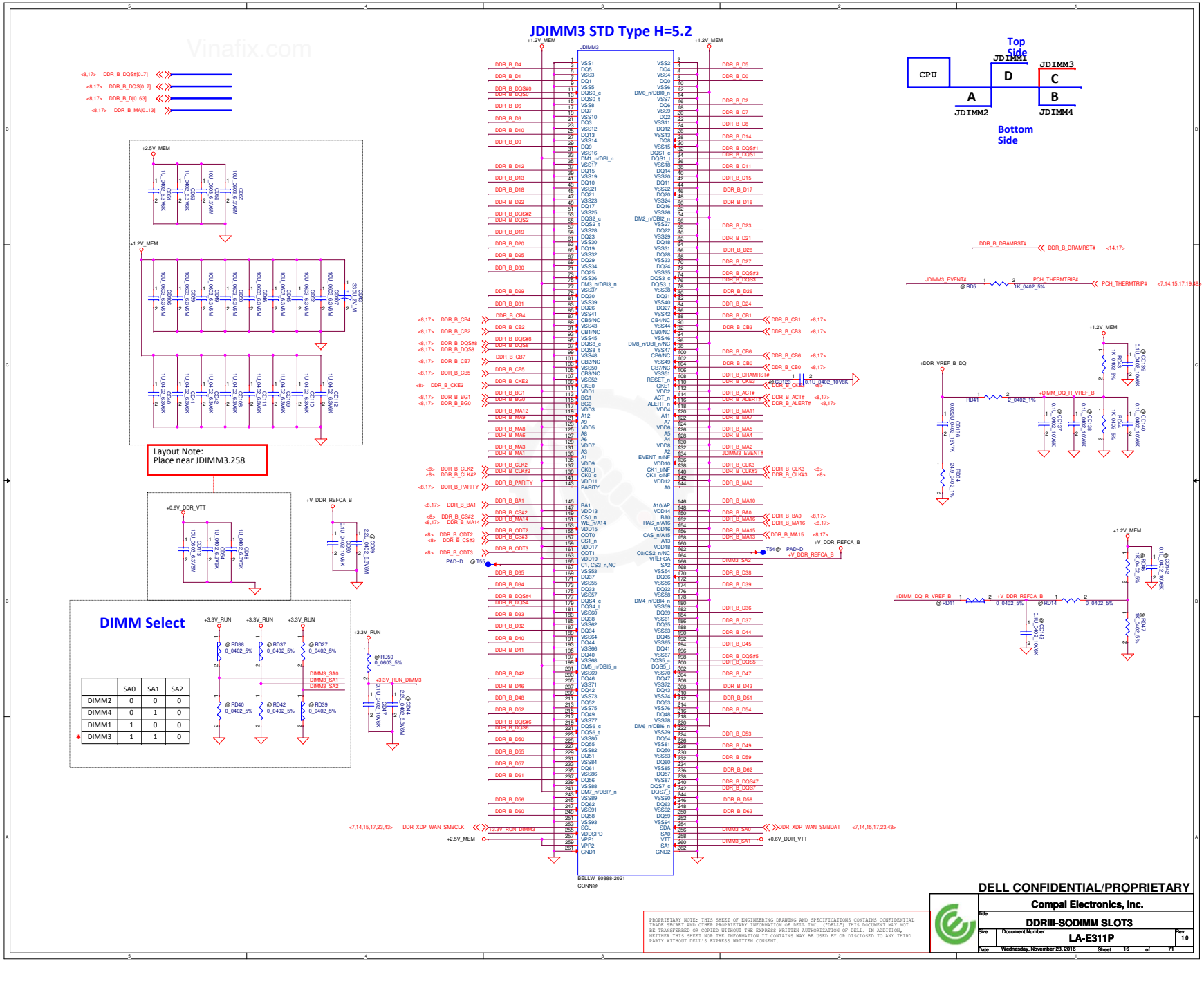
JDIMM3 STD Type H=5.2
Top Side
Bottom Side
CPU
JDIMM1
JDIMM3
JDIMM2
JDIMM4
Layout Note:
Place near JDIMM3.258
DIMM Select
SA0 SA1 SA2
DIMM2 0 0 0
DIMM4 0 1 0
DIMM1 1 0 0
DIMM3 1 1 0
JDIMM3
BELLW_80888-2021
CONN@
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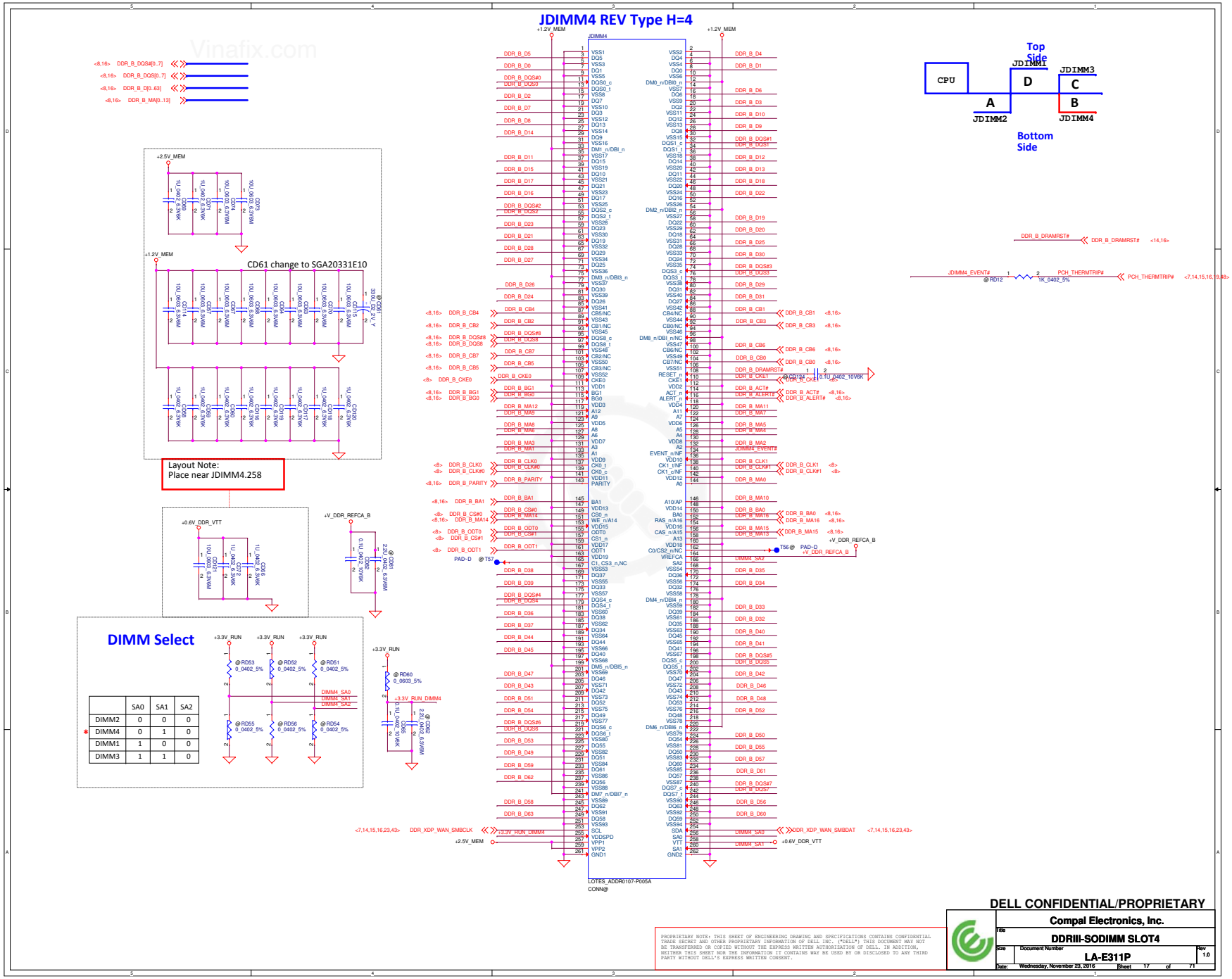
JDIMM4 REV Type H=4
Top Side
Bottom Side
CPU
JDIMM1
JDIMM3
JDIMM2
JDIMM4
CD61 change to SGA20331E10
Layout Note:
Place near JDIMM4.258
DIMM Select
SA0 SA1 SA2
DIMM2 0 0 0
DIMM4 0 1 0
DIMM1 1 0 0
DIMM3 1 1 0
JDIMM4
LOTES_ADDR0107-P005A
CONN@
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DDRIII-SODIMM SLOT4
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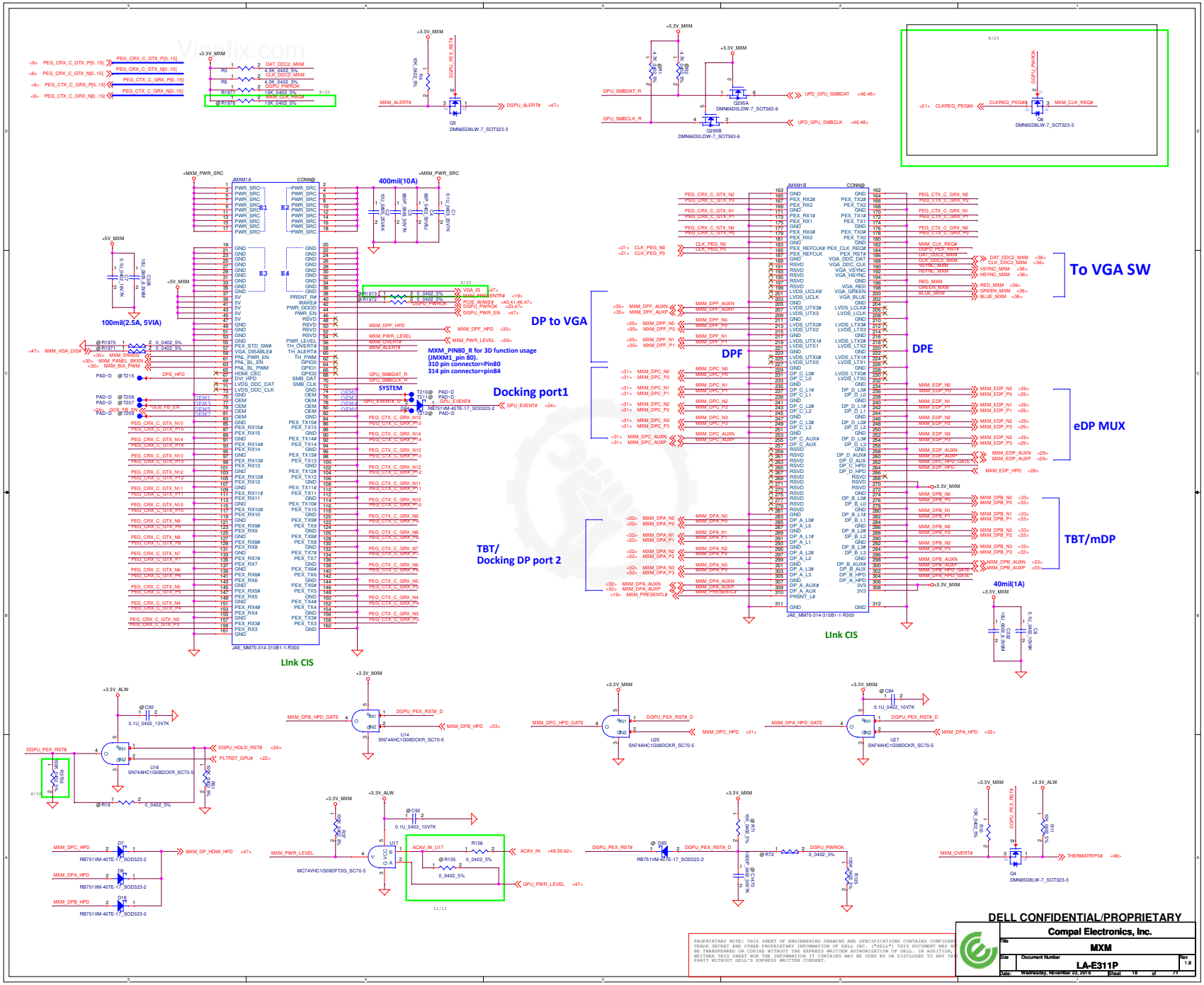
To VGA SW
DP to VGA
DPF
DPE
eDP MUX
TBT/mDP
TBT/
Docking DP port 2
Docking port1
Lnk CIS
Lnk CIS
400mil(10A)
100mil(2.5A, 5VIA)
40mil(1A)
MXM_PIN80_R for 3D function usage
(JMXM1_pin 80).
310 pin connector=Pin80
314 pin connector=pin84
SYSTEM
JAE_MM70-314-310B1-1-R300
JAE_MM70-314-310B1-1-R300
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MXM
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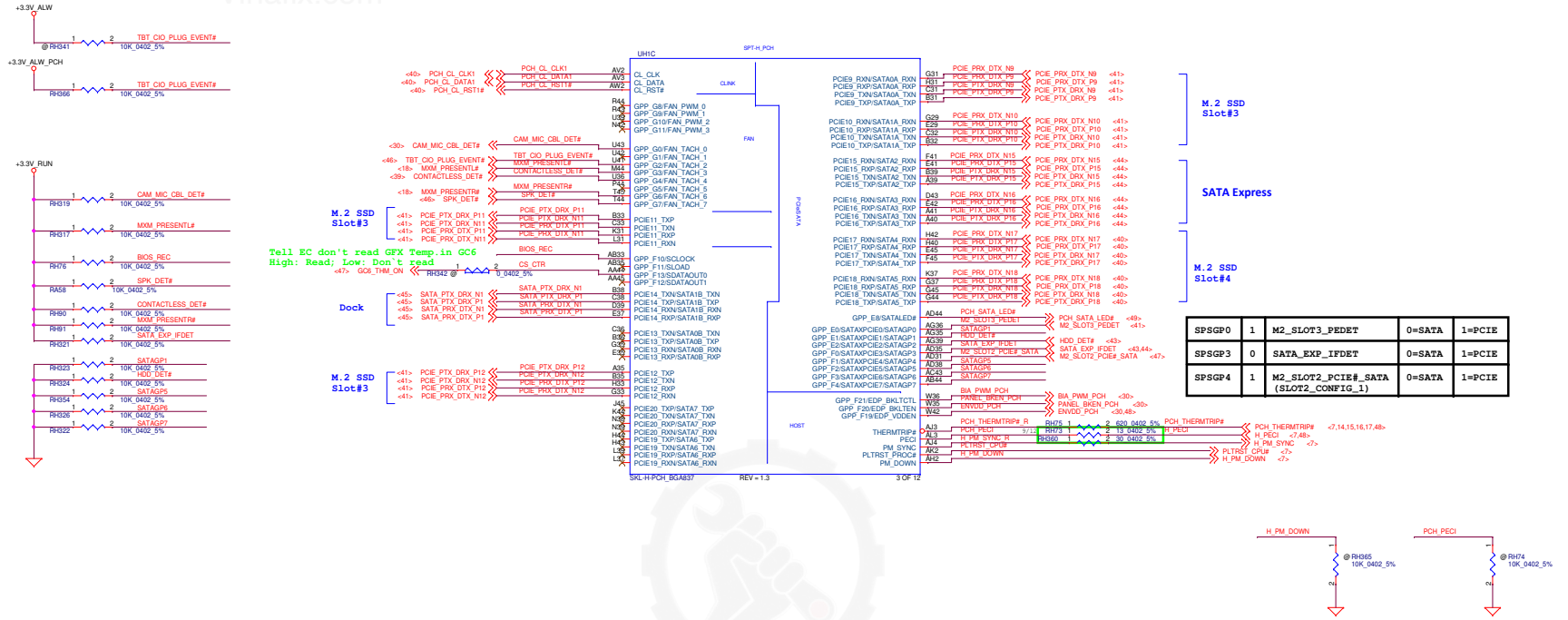

SPSGP0	1	M2_SLOT3_PEDET	0=SATA	1=PCIE
SPSGP3	0	SATA_EXP_IFDET	0=SATA	1=PCIE
SPSGP4	1	M2_SLOT2_PCIE#_SATA (SLOT2_CONFIG_1)	0=SATA	1=PCIE

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Title: SKYLAKE PCH-H (1/9)

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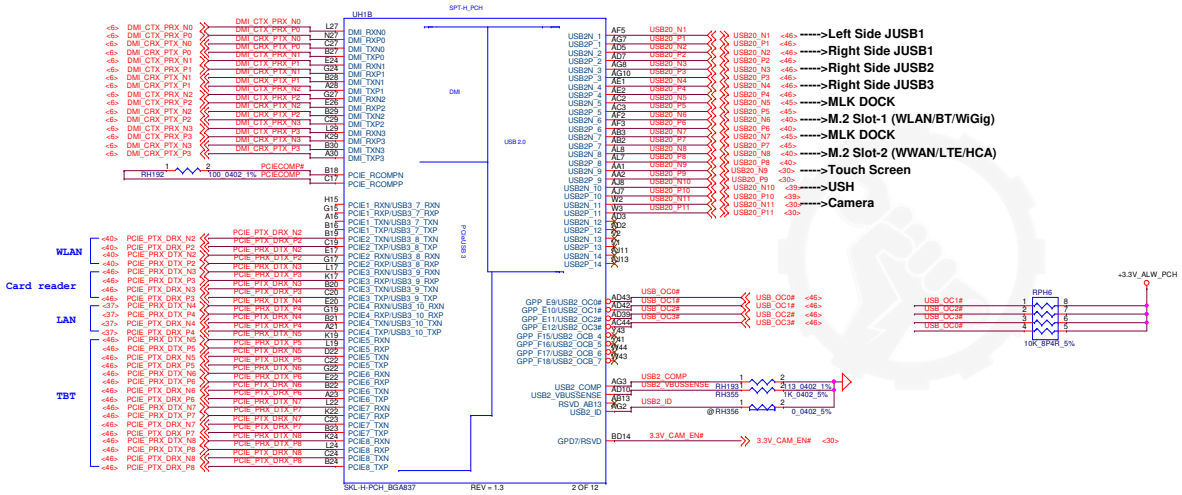

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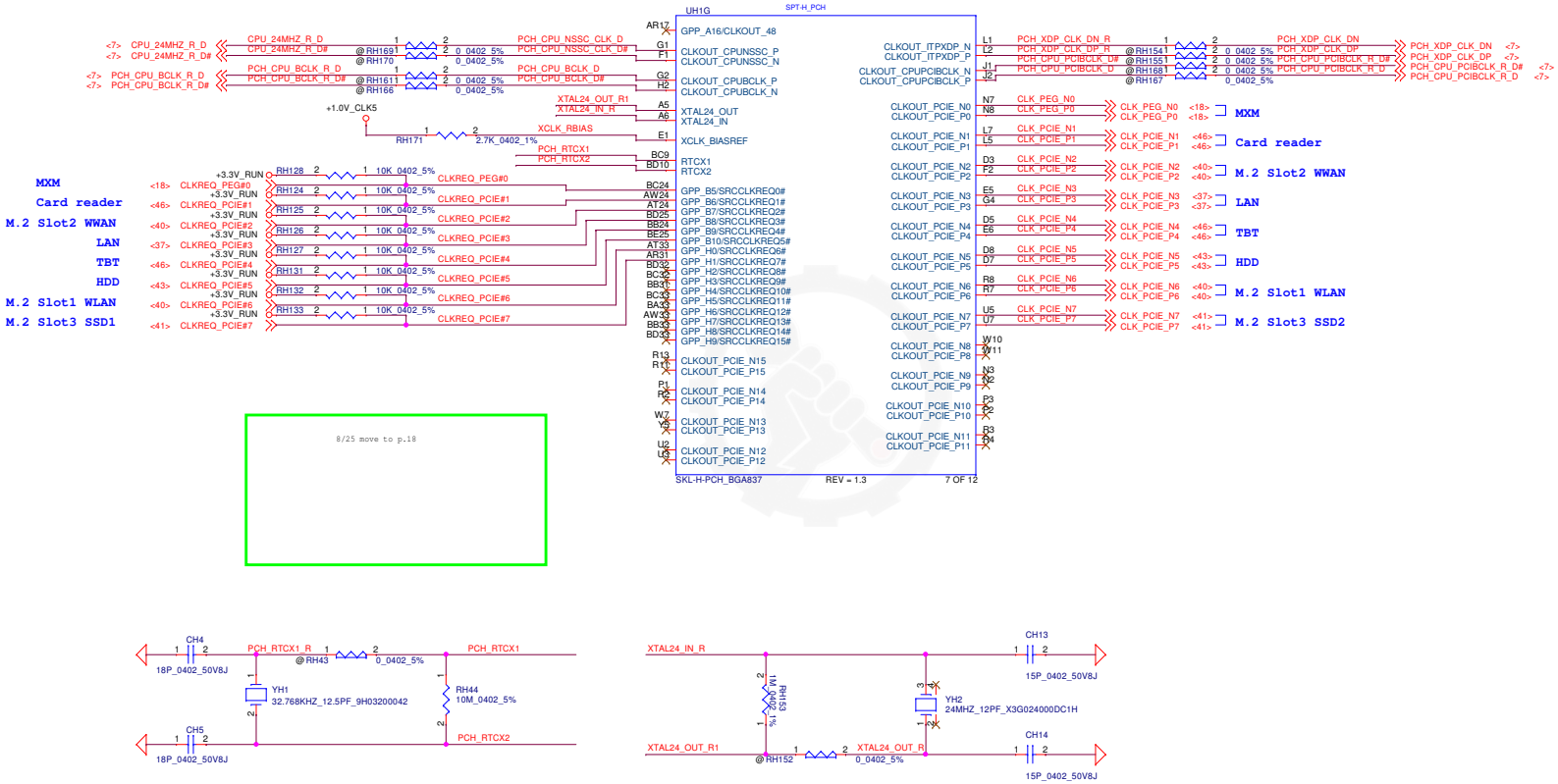

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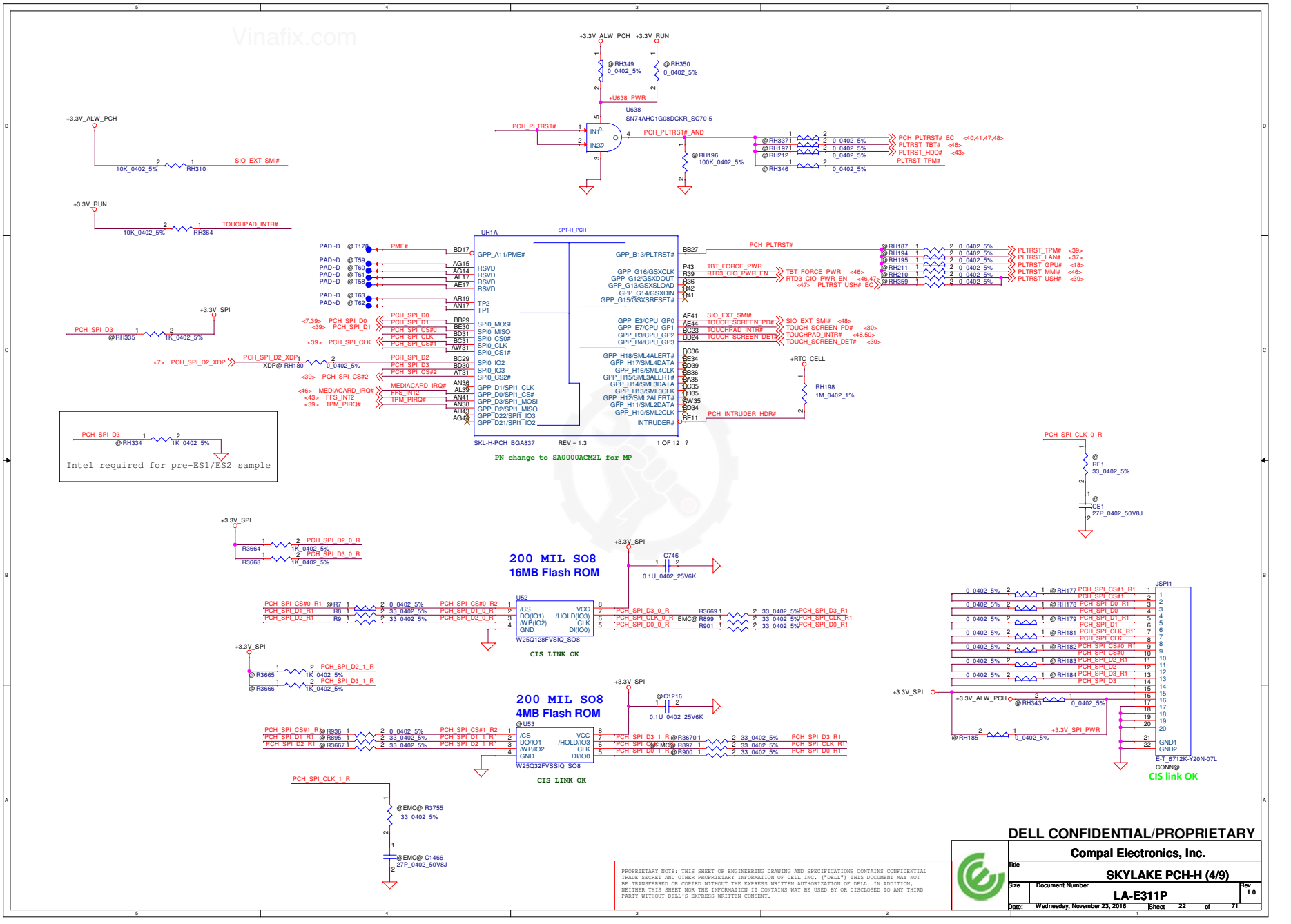
+3.3V_ALW_PCH
+3.3V_RUN
SIO_EXT_SMI#
TOUCHPAD_INTR#
PCH_PLTRST#
PCH_PLTRST# AND
PCH_PLTRST#_EC
PLTRST_TBT#
PLTRST_HDD#
PLTRST_TPM#
U638
SN74AHC1G08DCKR_SC70-5
UH1A
SPT-H_PCH
SKL-H-PCH_BGA837
REV = 1.3
1 OF 12
PN change to SA0000ACM2L for MP
Intel required for pre-ES1/ES2 sample
200 MIL SO8
16MB Flash ROM
W25Q128FVSIQ_SO8
CIS LINK OK
200 MIL SO8
4MB Flash ROM
W25Q32FVSSIQ_SO8
CIS LINK OK
JSPI1
E-T_6712K-Y20N-07L
CONN@
CIS link OK
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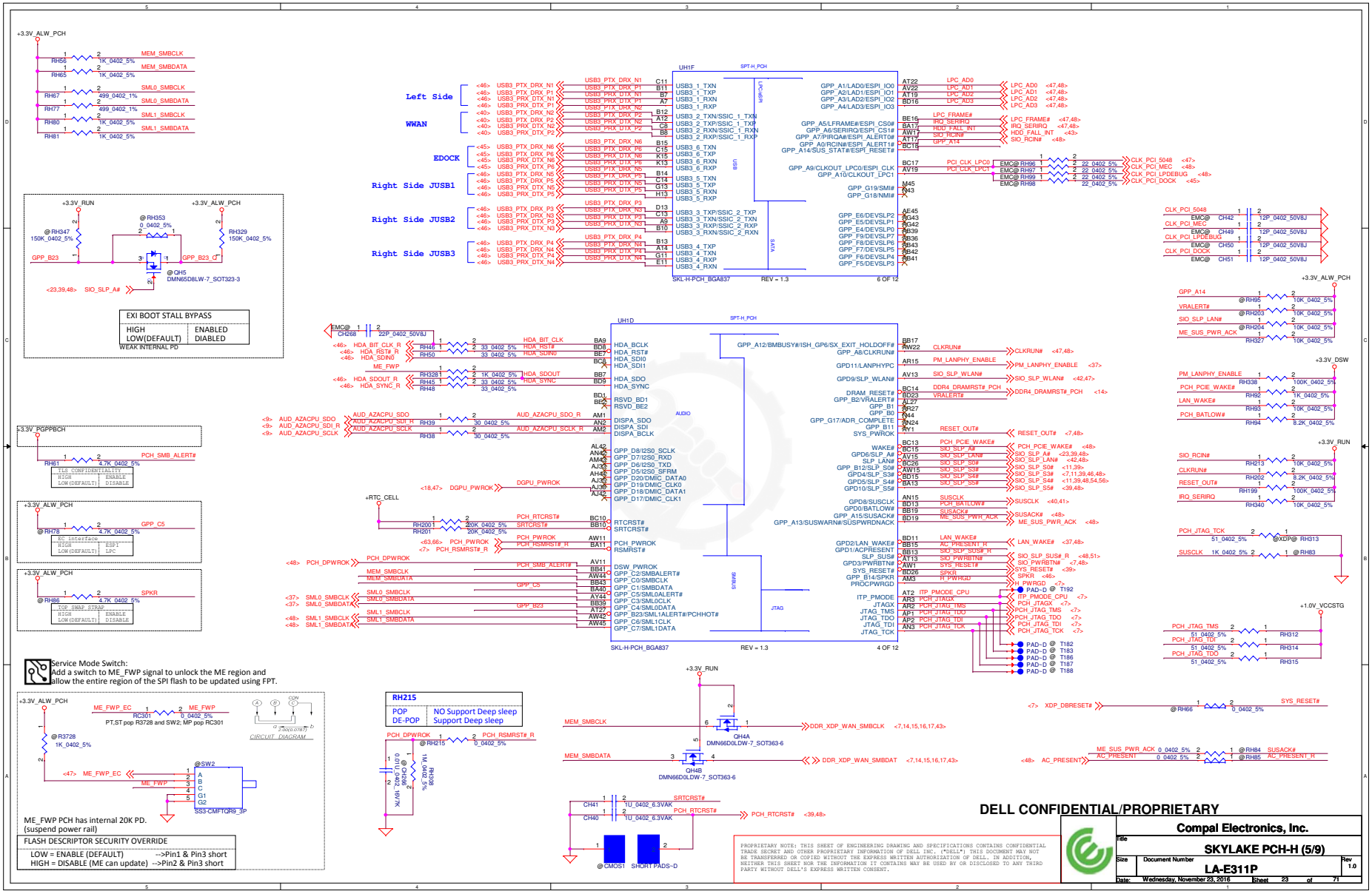
Left Side
WWAN
EDOCK
Right Side JUSB1
Right Side JUSB2
Right Side JUSB3
UH1F
SPT-H_PCH
SKL-H-PCH_BGA837
REV = 1.3
6 OF 12
UH1D
4 OF 12
EXI BOOT STALL BYPASS
HIGH ENABLED
LOW(DEFAULT) DIABLED
WEAK INTERNAL PD
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.
ME_FWP PCH has internal 20K PD. (suspend power rail)
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = ENABLE (DEFAULT) -->Pin1 & Pin3 short
HIGH = DISABLE (ME can update) -->Pin2 & Pin3 short
RH215
POP NO Support Deep sleep
DE-POP Support Deep sleep
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SKYLAKE PCH-H (5/9)
LA-E311P
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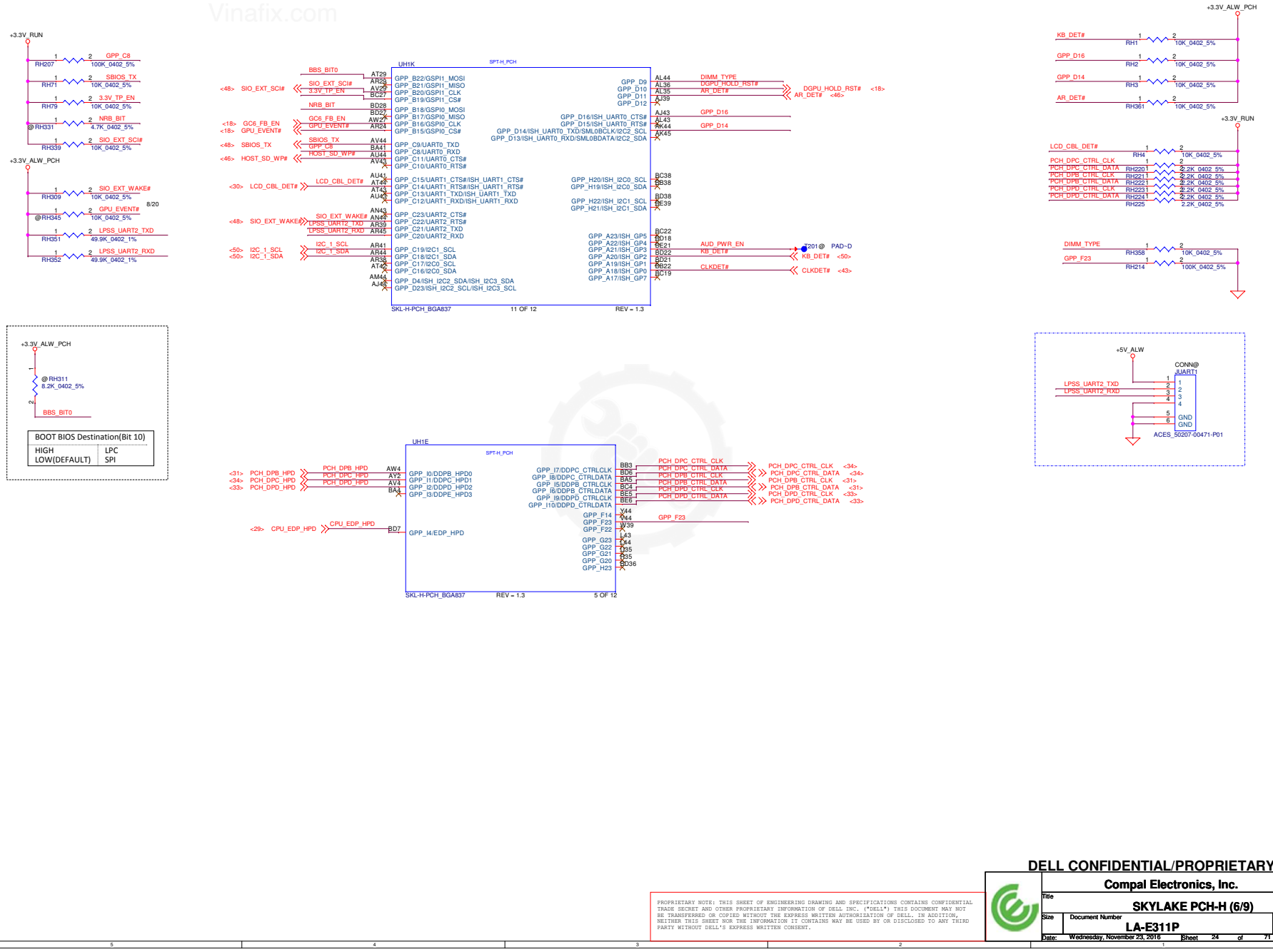

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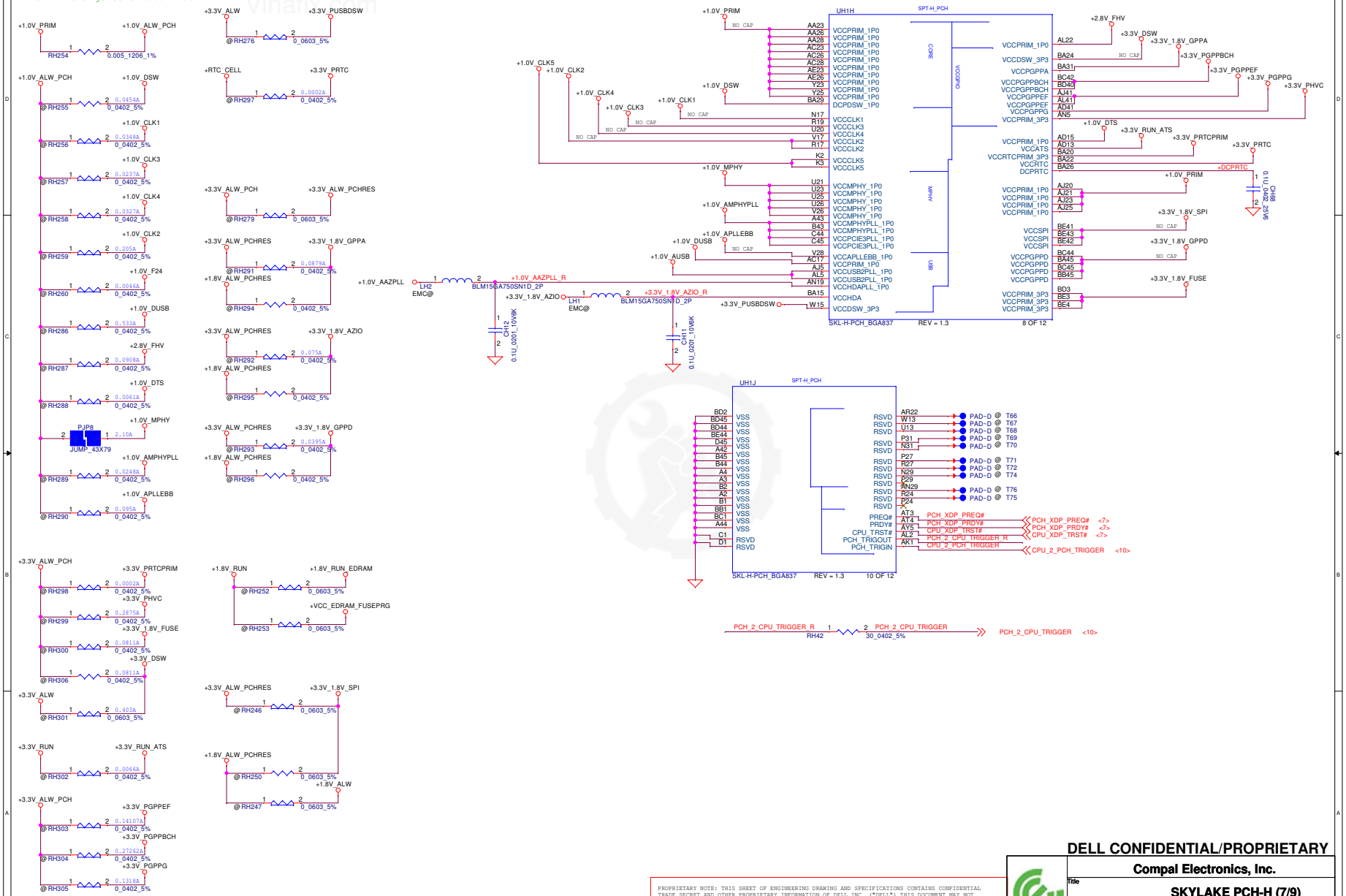
RH254 PN change to SD000017R00



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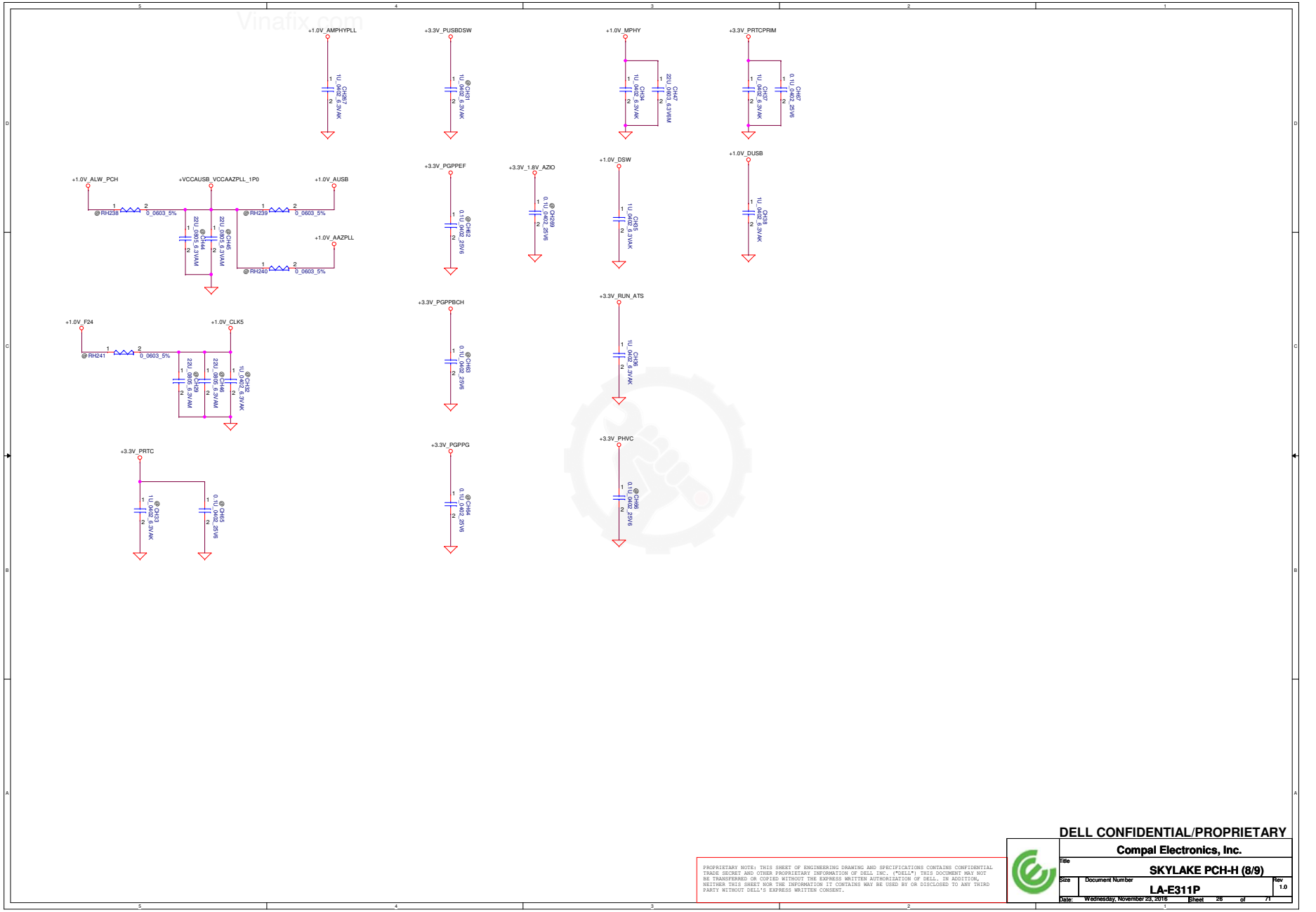

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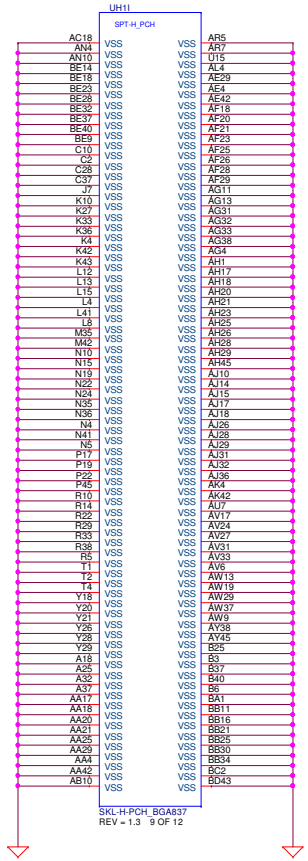

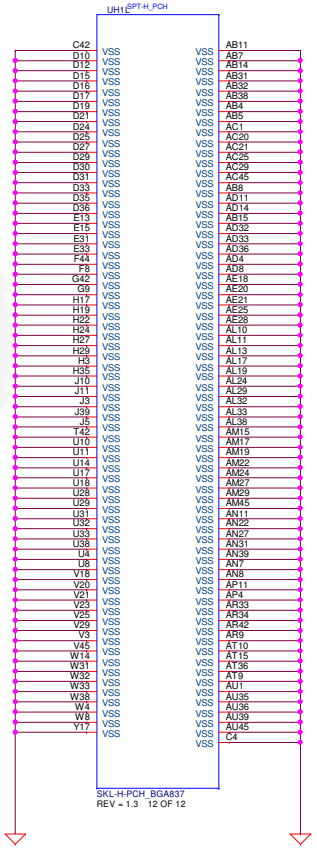

Compal Electronics, Inc.

Title: SKYLAKE PCH-H (9/9)

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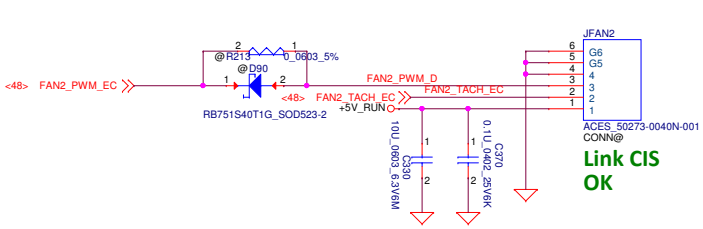
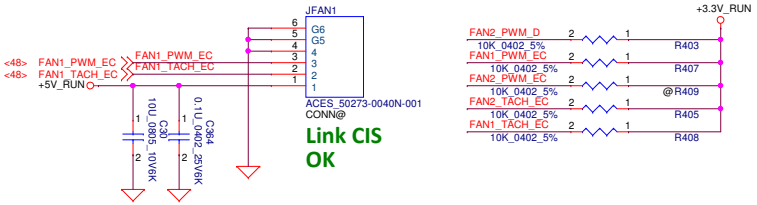
Date: Wednesday, November 23, 2016 | Sheet 27 of 71

MXM FAN



Link CIS
OK

CPU FAN



Link CIS
OK

Compal Electronics, Inc.

Title: FAN control

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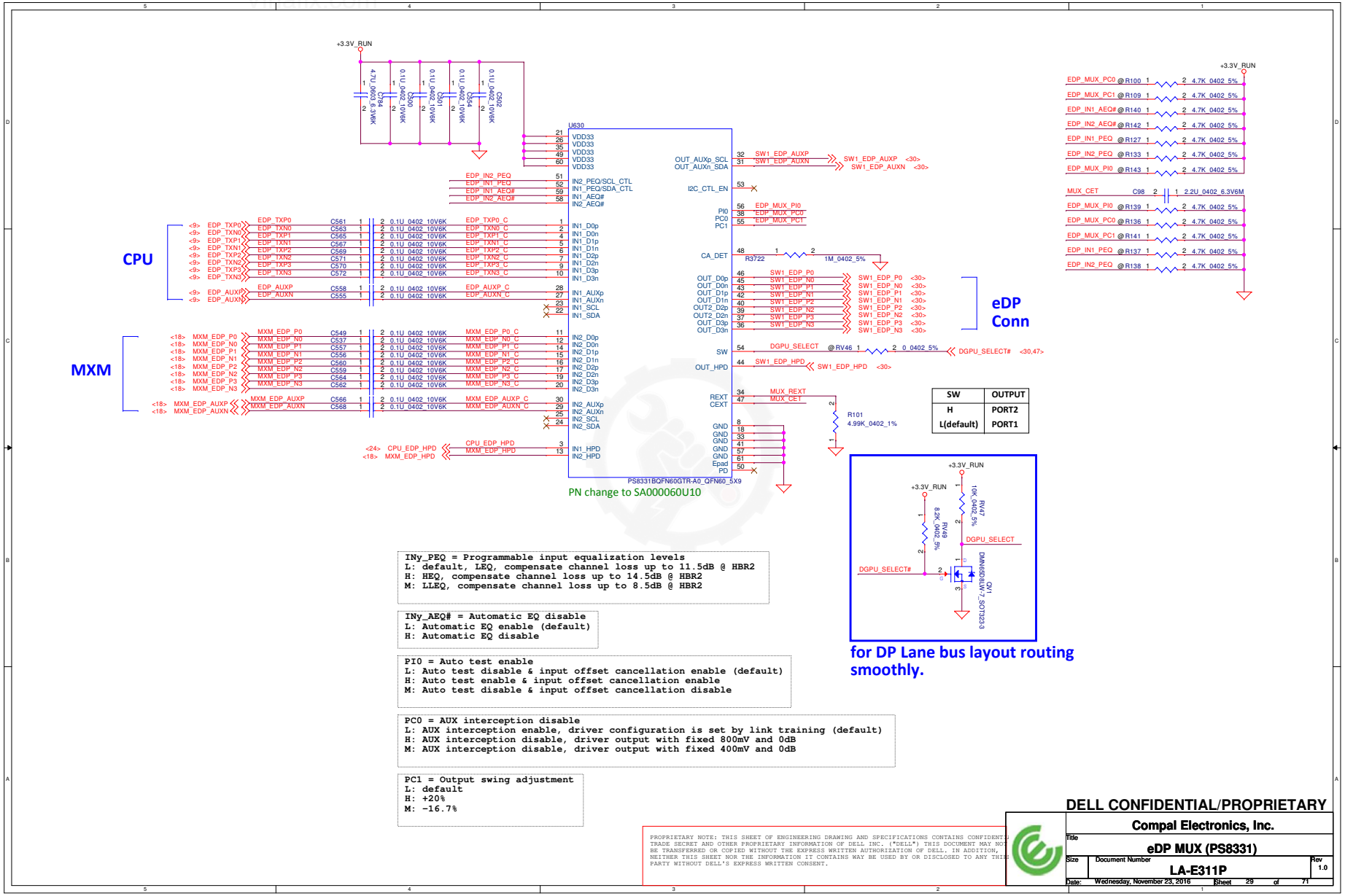
Date: Wednesday, November 23, 2016 | Sheet 28 of 71

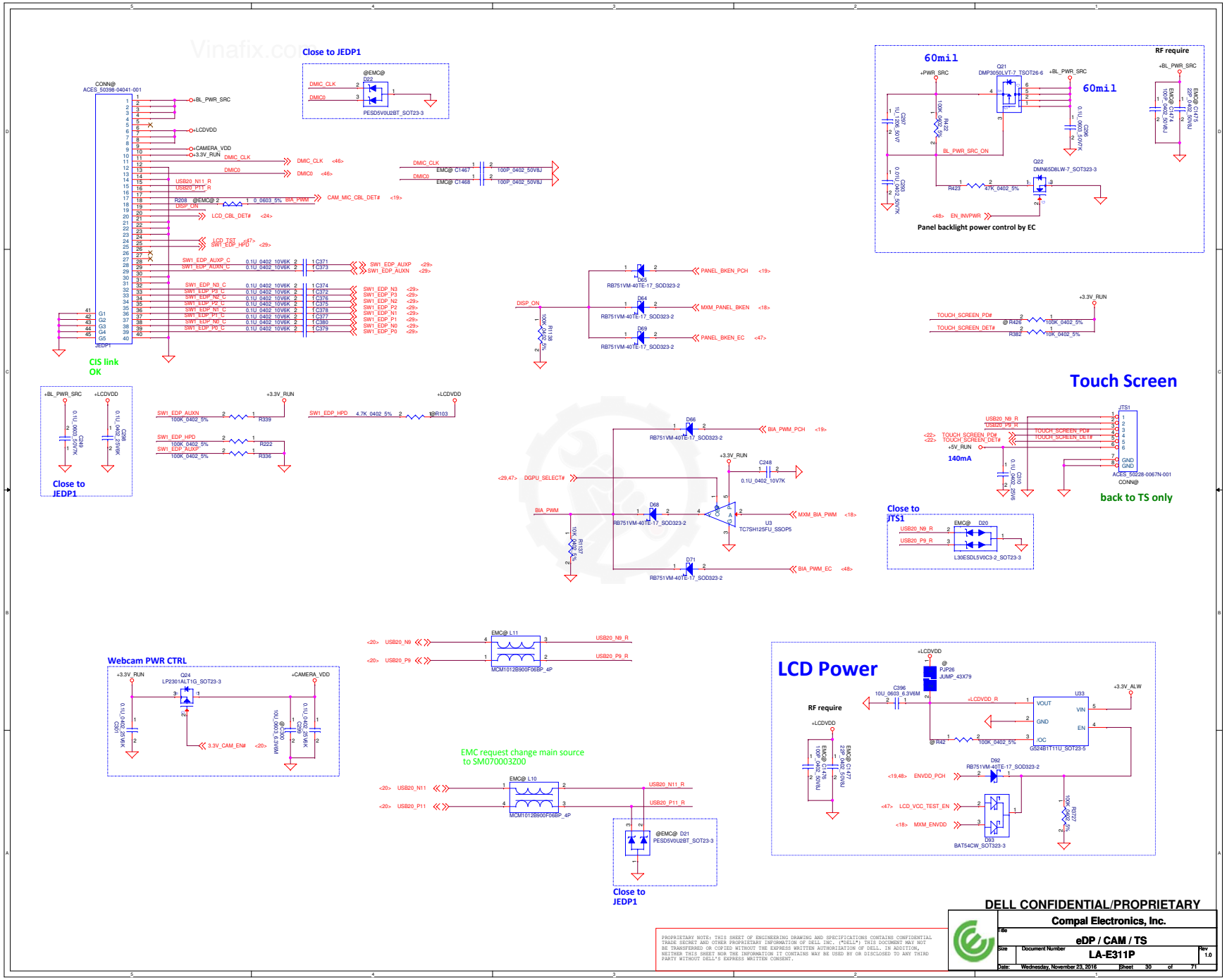


Compal Electronics, Inc.

Title: eDP MUX (PS8331)

Size | Document Number: LA-E311P | Rev: 1.0

Date: Wednesday, November 23, 2016 | Sheet 29 of 71


Close to JEDP1
CONN@
ACES_50398-04041-001
JEDP1
CIS link OK
60mil
RF require
Q21
DMP3050LVT-7_TSOT26-6
Q22
DMN65D8LW-7_SOT323-3
Panel backlight power control by EC
Touch Screen
JTS1
ACES_50228-0067N-001
back to TS only
140mA
Close to JTS1
Webcam PWR CTRL
Q24
LP2301ALT1G_SOT23-3
EMC request change main source to SM070003Z00
LCD Power
Close to JEDP1
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
eDP / CAM / TS
LA-E311P
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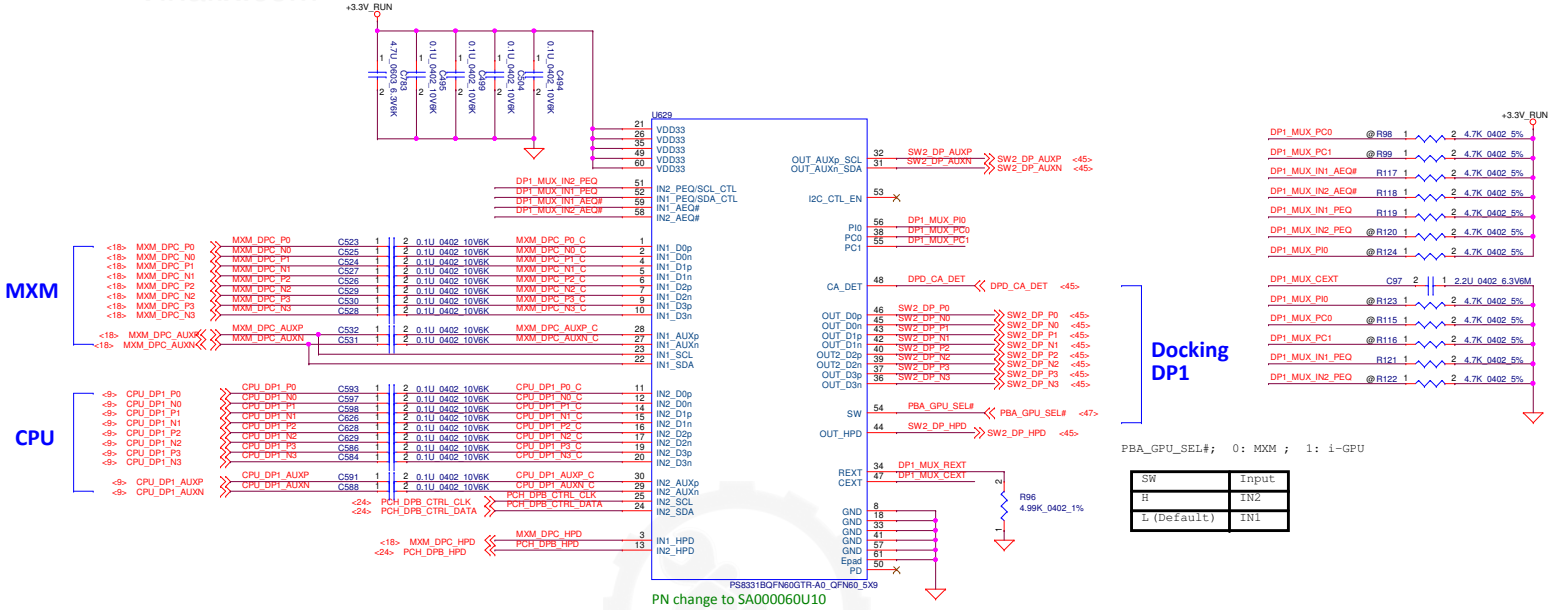

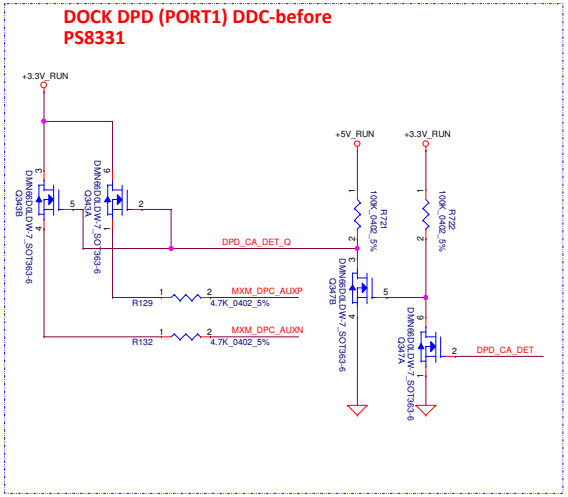

INy_PEQ = Programmable input equalization levels
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
L: Automatic EQ enable (default)
H: Automatic EQ disable

PI0 = Auto test enable
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment
L: default
H: +20%
M: -16.7%

Compal Electronics, Inc.

Title: MXM/CPU MUX(PS8331)

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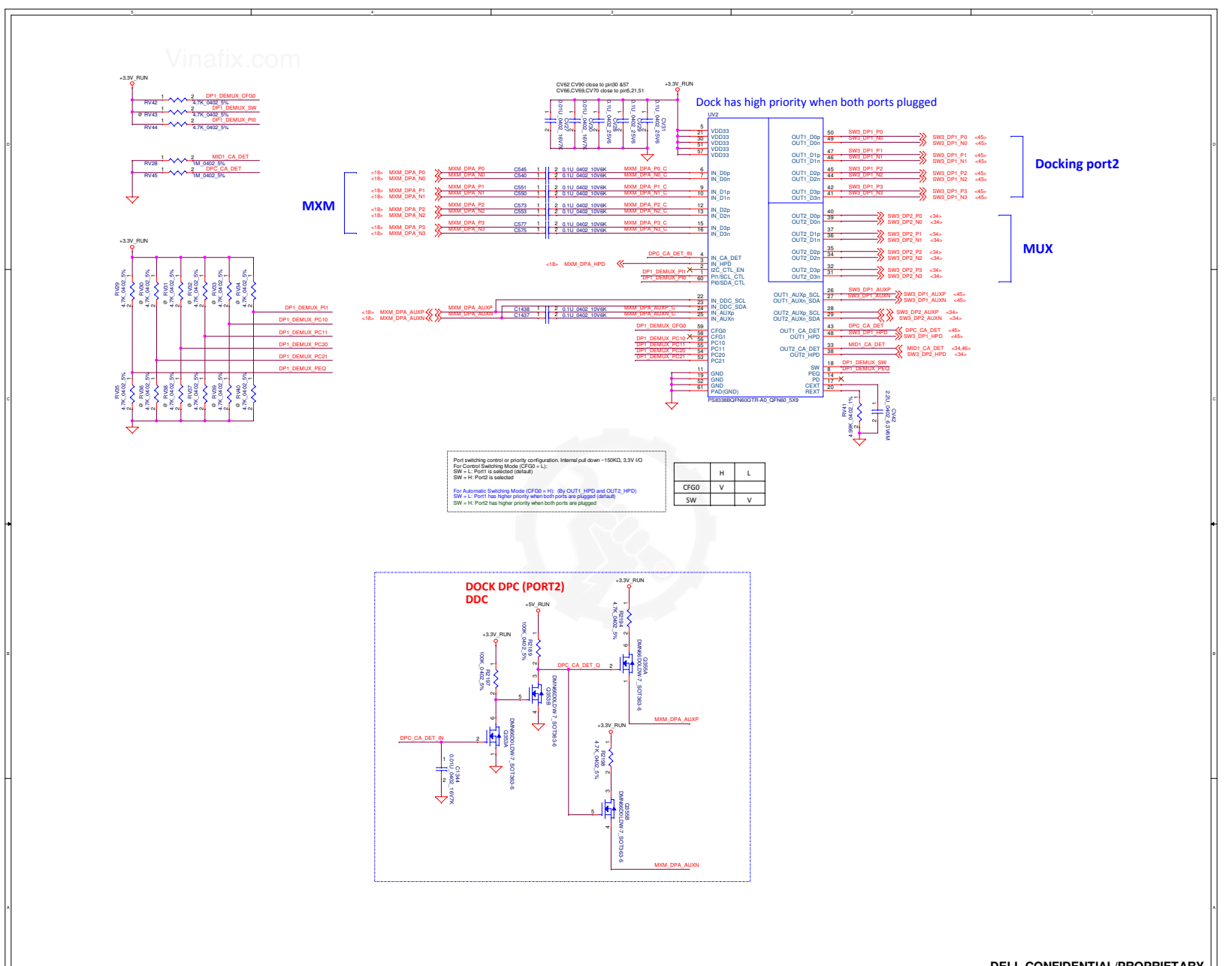
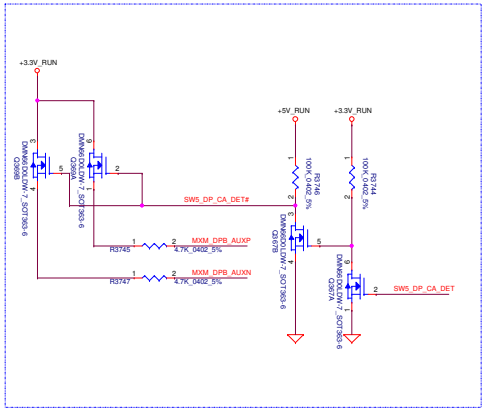


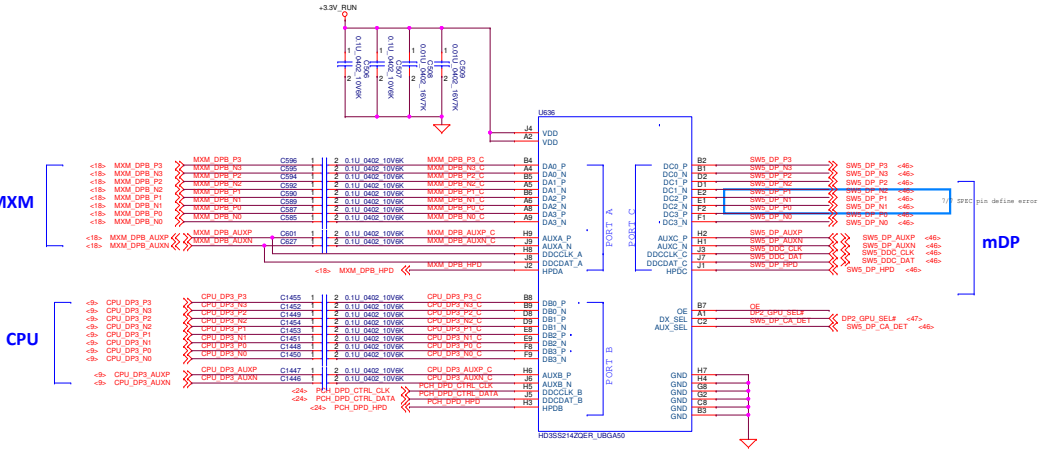
Compal Electronics, Inc.

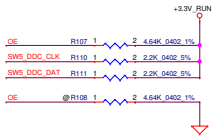
Title: DP DeMUX (PS8338)

Size: | Document Number: LA-E311P | Rev: 1.0

Date: Wednesday, November 23, 2016 | Sheet 32 of 71







OE	Output enable
H	Normal Operation
L (Default)	Standby Mode

DP2_GPU_SEL#;
0: MXM ; 1: i-GPU

DX_SEL	Input
H	Port B
L (Default)	Port A

SW5_DP_CA_DET;
0: DP; 1: HDMI

AUX_SEL	To/From
H	DDC
L (Default)	AUX

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Compal Electronics, Inc.

Title: P33-mDP MB DP1.3 MUX (HD3SS214)

Size: | Document Number: LA-E311P | Rev: 1.0

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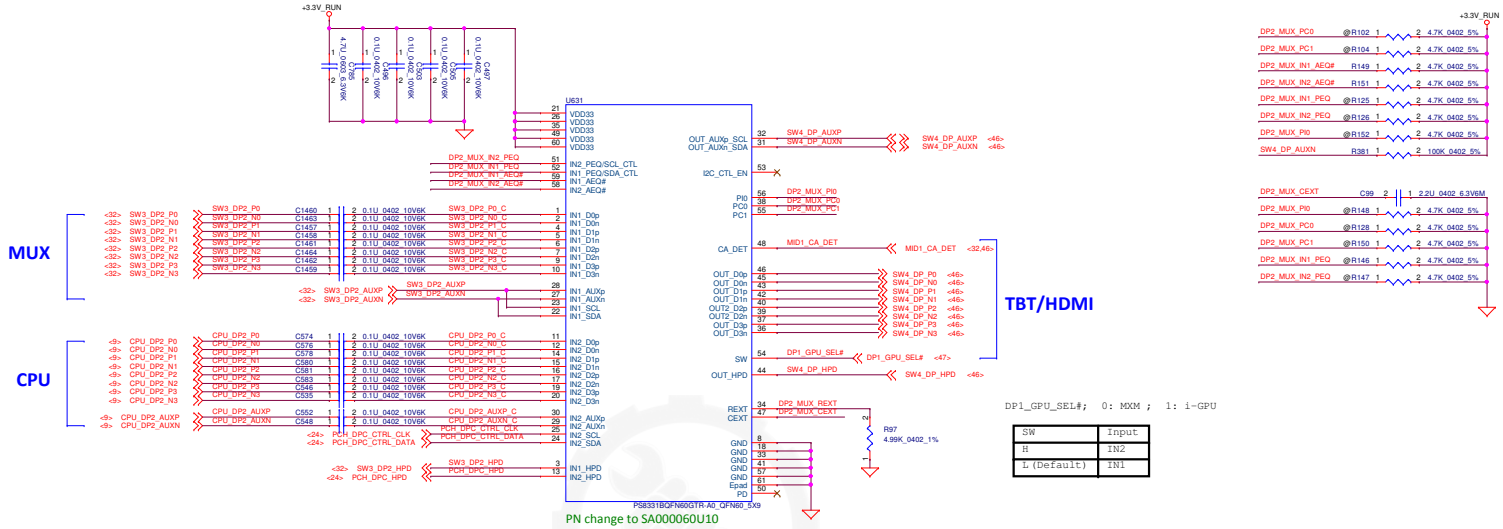

PN change to SA000060U10

DP1_GPU_SEL#; 0: MXM ; 1: i-GPU

SW	Input
H	IN2
L (Default)	IN1

INy_PEQ = Programmable input equalization levels
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
L: Automatic EQ enable (default)
H: Automatic EQ disable

PI0 = Auto test enable
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment
L: default
H: +20%
M: -16.7%

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Compal Electronics, Inc.

Title: VGA CONN

Size | Document Number: LA-E311P | Rev: 1.0

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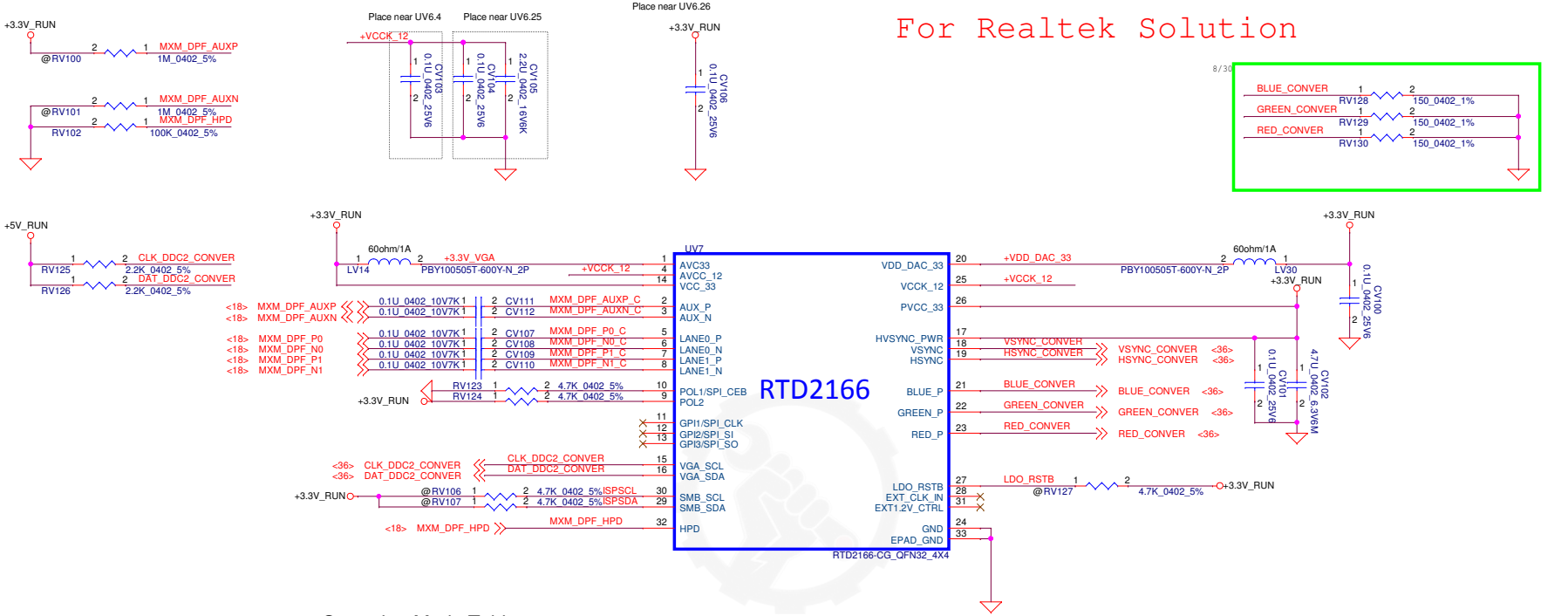
For Realtek Solution



Operation Mode Table

		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	Flash

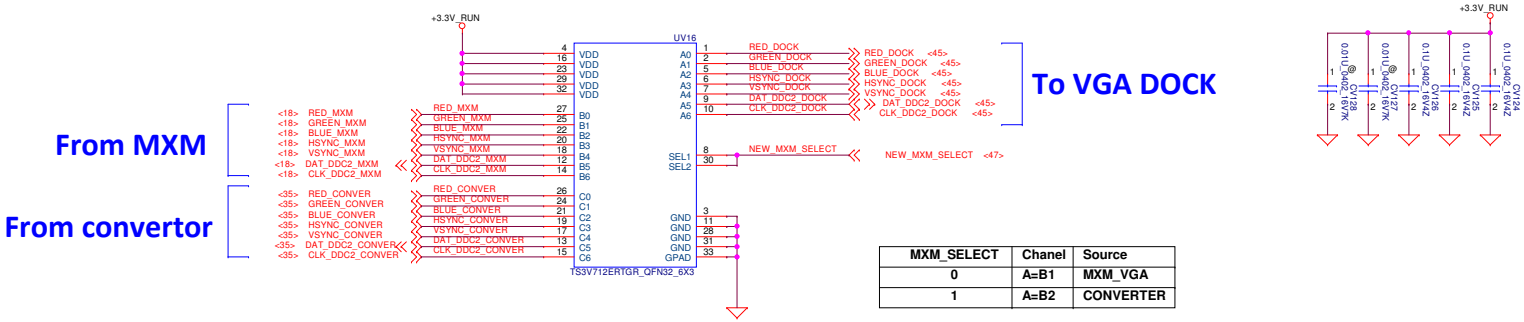
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: DP to VGA

Size: B | Document Number: LA-E311P | Rev: 1.0

Date: Wednesday, November 23, 2016 | Sheet 35 of 71



MXM_SELECT	Chanel	Source
0	A=B1	MXM_VGA
1	A=B2	CONVERTER

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: VGA SW(TS3V712)

Size: Custom | Document Number: LA-E311P | Rev: 1.0

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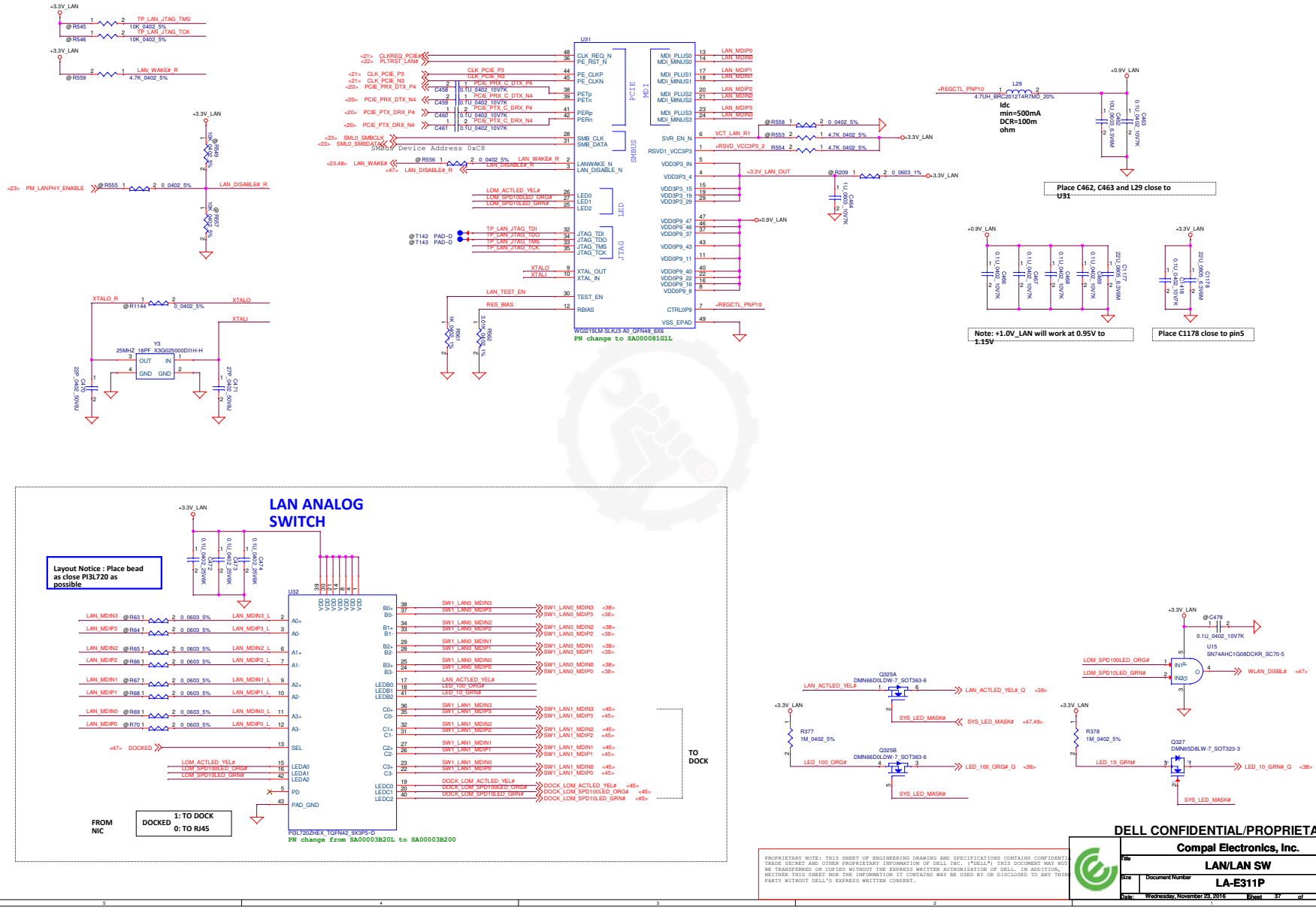
U31
WG8219LM-SLKJ3-A0_QFN48_6X6
PN change to SA000081G1L
Device Address 0xC8
Place C462, C463 and L29 close to U31
Note: +1.0V_LAN will work at 0.95V to 1.15V
Place C1178 close to pin5
LAN ANALOG SWITCH
Layout Notice : Place bead as close PI3L720 as possible
U32
PI3L720ZHEX_TQFN42_9X3P5-D
PN change from SA00003B20L to SA00003B200
DOCKED 1: TO DOCK 0: TO RJ45
FROM NIC
TO DOCK
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
LAN/LAN SW
LA-E311P
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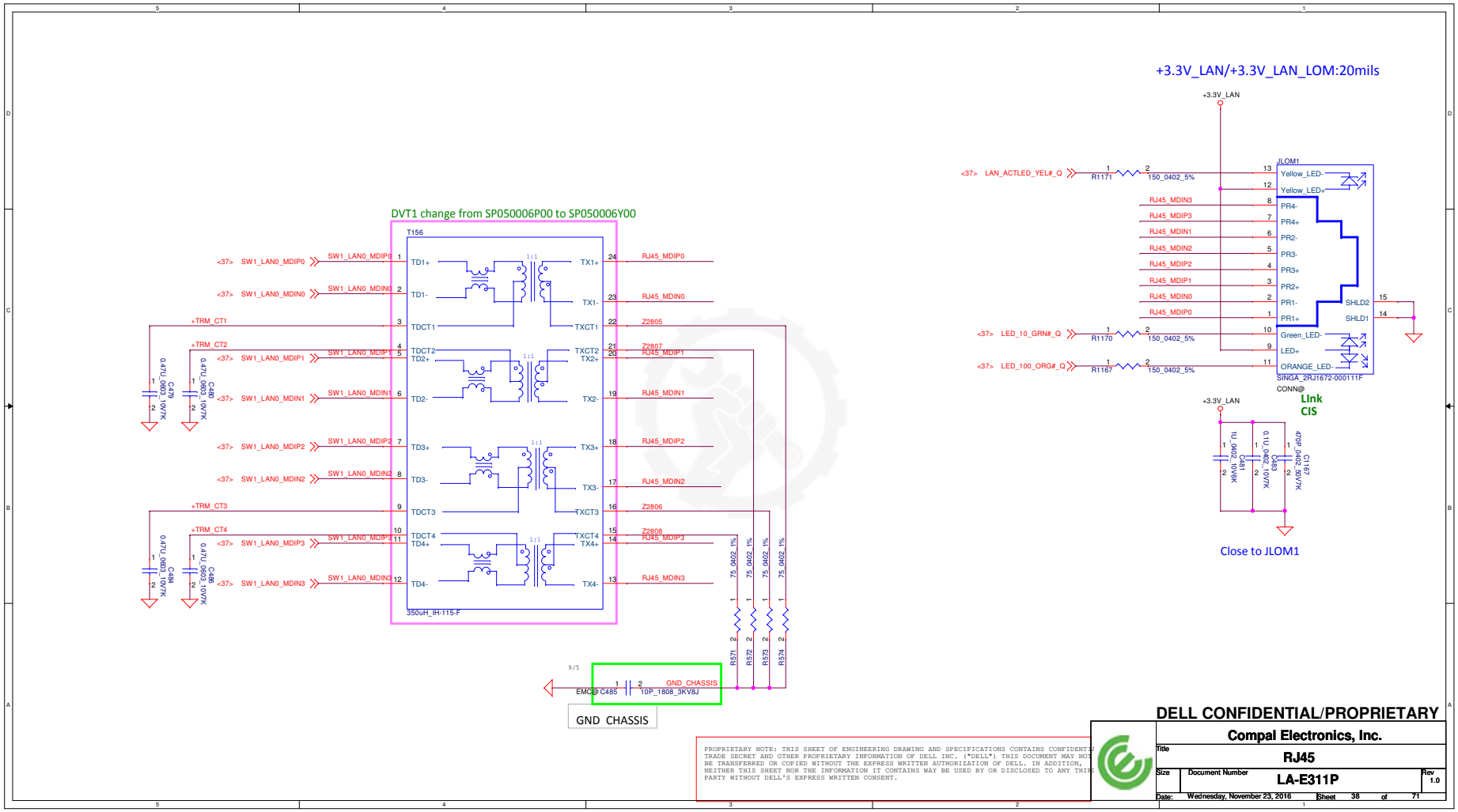

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Compal Electronics, Inc.

Title	RJ45	
Size	Document Number: LA-E311P	Rev: 1.0
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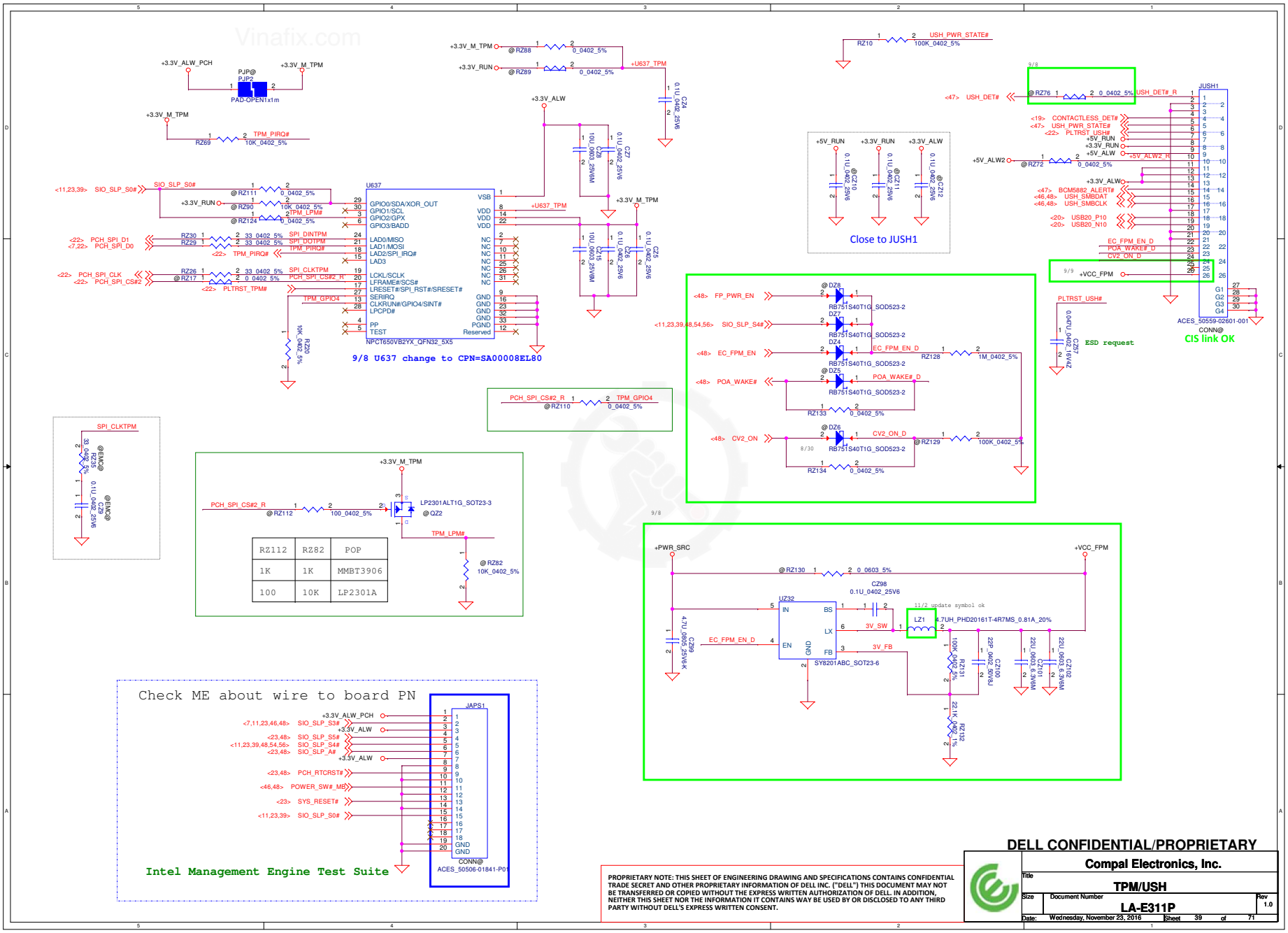
Vinafix.com
+3.3V_ALW_PCH
+3.3V_M_TPM
PJP@
PJP2
PAD-OPEN1x1m
TPM_PIRQ#
RZ69
10K_0402_5%
U637
SIO_SLP_S0#
+3.3V_RUN
SPI_DINTPM
SPI_DOTPM
SPI_CLKTPM
PCH_SPI_CS#2_R
PLTRST_TPM#
TPM_GPIO4
GPIO0/SDA/XOR_OUT
GPIO1/SCL
GPIO2/GPX
GPIO3/BADD
LAD0/MISO
LAD1/MOSI
LAD2/SPI_IRQ#
LAD3
LCLK/SCLK
LFRAME#/SCS#
LRESET#/SPI_RST#/SRESET#
SERIRQ
CLKRUN#/GPIO4/SINT#
LPCPD#
PP
TEST
VSB
VDD
PGND
Reserved
NPCT650VB2YX_QFN32_5X5
+U637_TPM
9/8 U637 change to CPN=SA00008EL80
PCH_SPI_CS#2_R
TPM_GPIO4
SPI_CLKTPM
LP2301ALT1G_SOT23-3
@QZ2
TPM_LPM#
RZ112
RZ82
POP
1K
1K
MMBT3906
100
10K
LP2301A
Check ME about wire to board PN
JAPS1
Intel Management Engine Test Suite
USH_PWR_STATE#
100K_0402_5%
USH_DET#
USH_DET#_R
JUSH1
CONTACTLESS_DET#
USH_PWR_STATE#
PLTRST_USH#
BCM5882_ALERT#
USH_SMBDAT
USH_SMBCLK
USB20_P10
USB20_N10
EC_FPM_EN_D
POA_WAKE#_D
CV2_ON_D
+VCC_FPM
ACES_50559-02601-001
CONN@
CIS link OK
Close to JUSH1
PLTRST_USH#
ESD request
FP_PWR_EN
EC_FPM_EN
POA_WAKE#
CV2_ON
RB751S40T1G_SOD523-2
RZ128
1M_0402_5%
RZ133
RZ134
RZ129
100K_0402_5%
+PWR_SRC
UZ32
SY8201ABC_SOT23-6
LZ1
4.7UH_PHD20161T-4R7MS_0.81A_20%
3V_SW
3V_FB
EC_FPM_EN_D
RZ131
RZ132
CZ100
CZ101
CZ102
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Compal Electronics, Inc.
TPM/USH
LA-E311P
Wednesday, November 23, 2016
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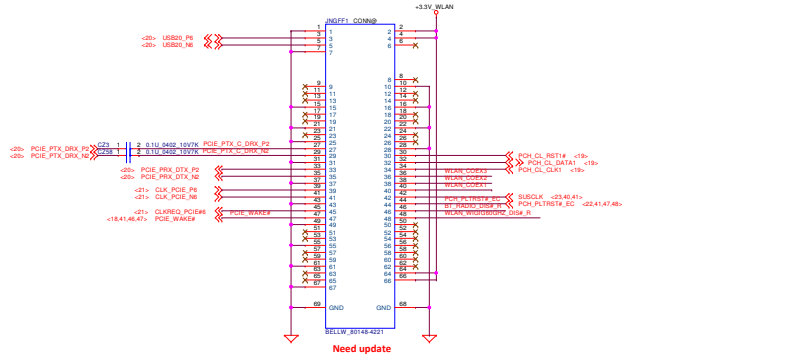
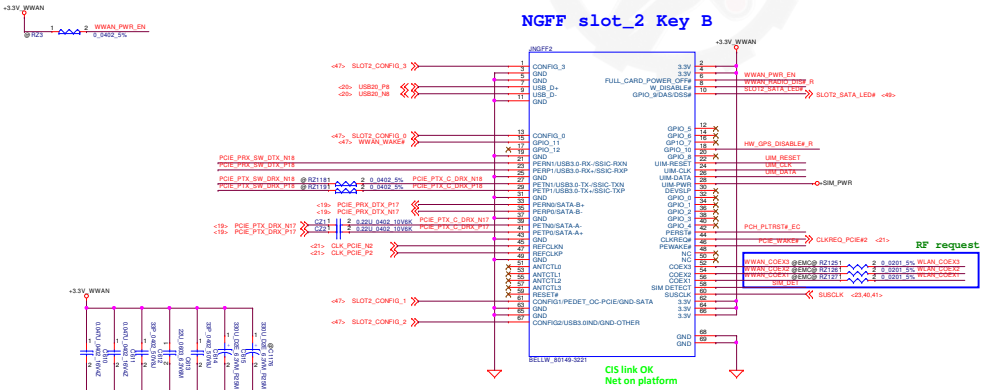
WLAN/BT

NGFF slot_1 Key A

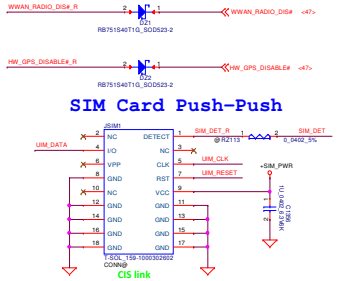


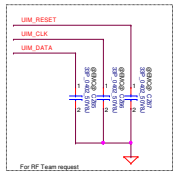
WWAN/LTE/Cache(Optane)

NGFF slot_2 Key B



Function	SEL	PD
B to A	L	L
C to A	H	L
All ports Hi-Z, IC power down	X	H





STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	0	0	0	0	SSD-SATA
8	1	0	0	0	WWAN
14	1	0	1	1	HCA-PCIE
15	1	1	1	1	Cache

Compal Electronics, Inc.

Title: M.2 Card-1/2

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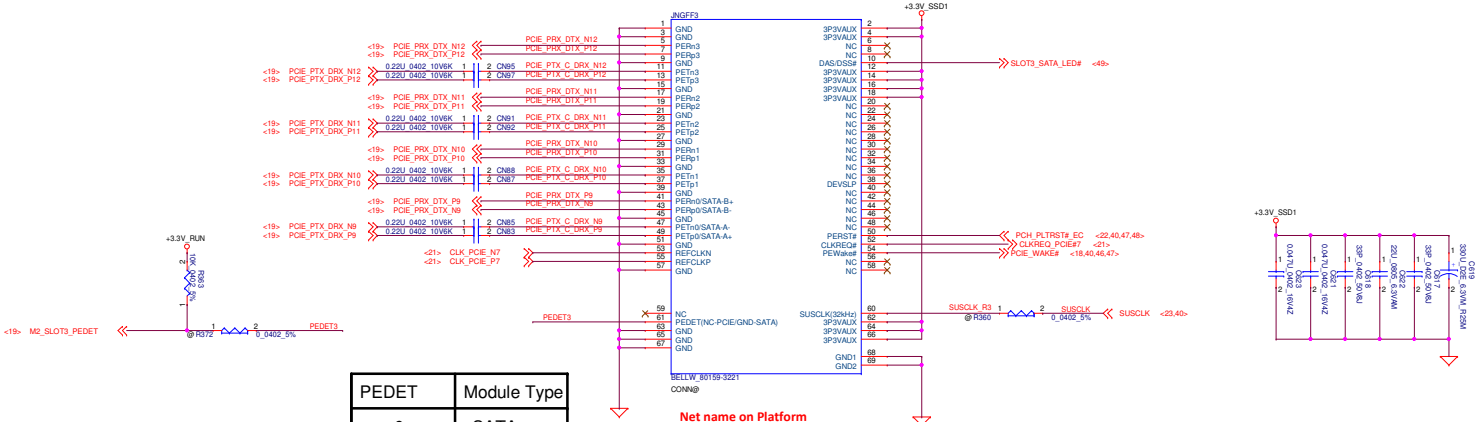
SSD
NGFF slot_3 Key M



PEDET	Module Type
0	SATA
1	PCIE

Compal Electronics, Inc.

Title	M.2 Card-2/2	
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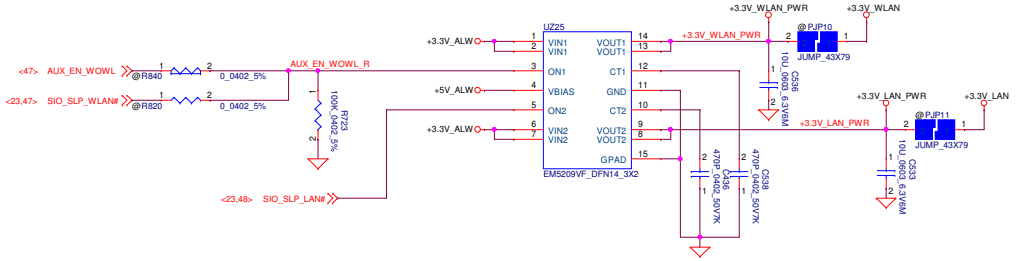
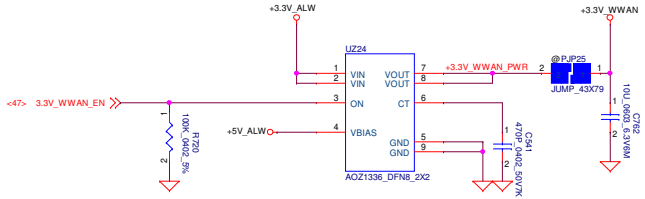
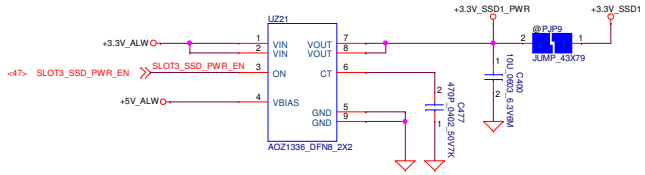
Power Control for M.2 slot 1. & +3.3V_RUN Source



Power Control for M.2 slot 2.



Power Control for M.2 slot 3. Source



Compal Electronics, Inc.

Title	M.2 Card PWR	
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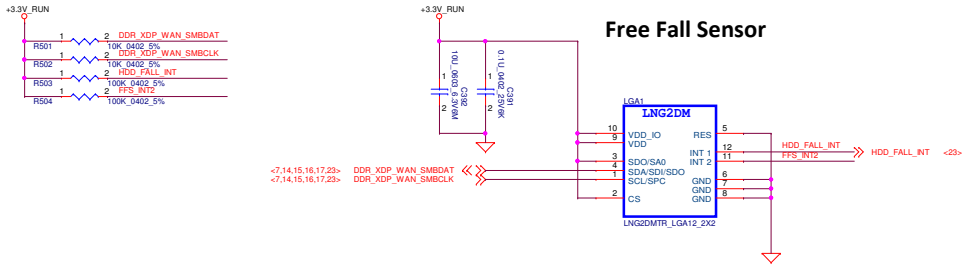
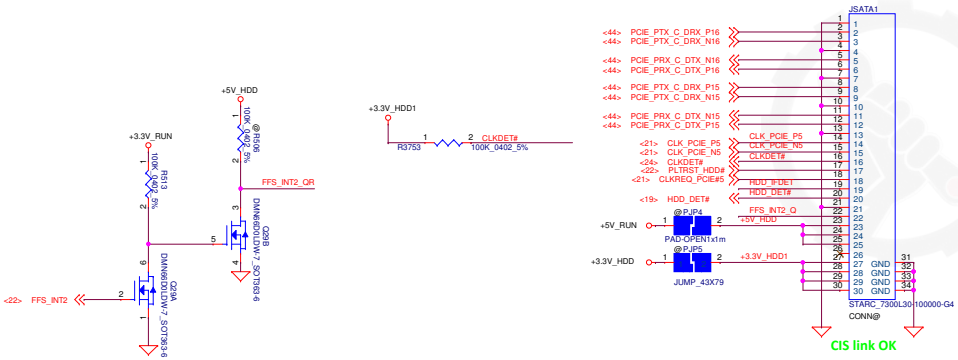
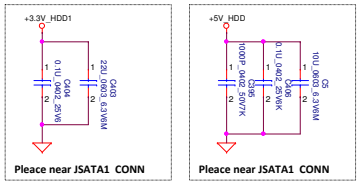
Free Fall Sensor



HDD1 CONN

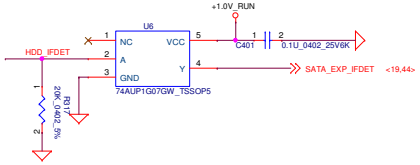


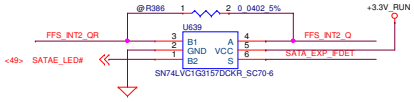


HDD_IFDET	DEVICE interface
0	SATA
1 (1.44V)	PCIE

SATA_EXP_IFDET	DEVICE interface
0	SATA
1 (3.3V)	PCIE

SATA_EXP_IFDET	channel on
0	A-->B1
1	A-->B2





Compal Electronics, Inc.

Title: HDD CONN

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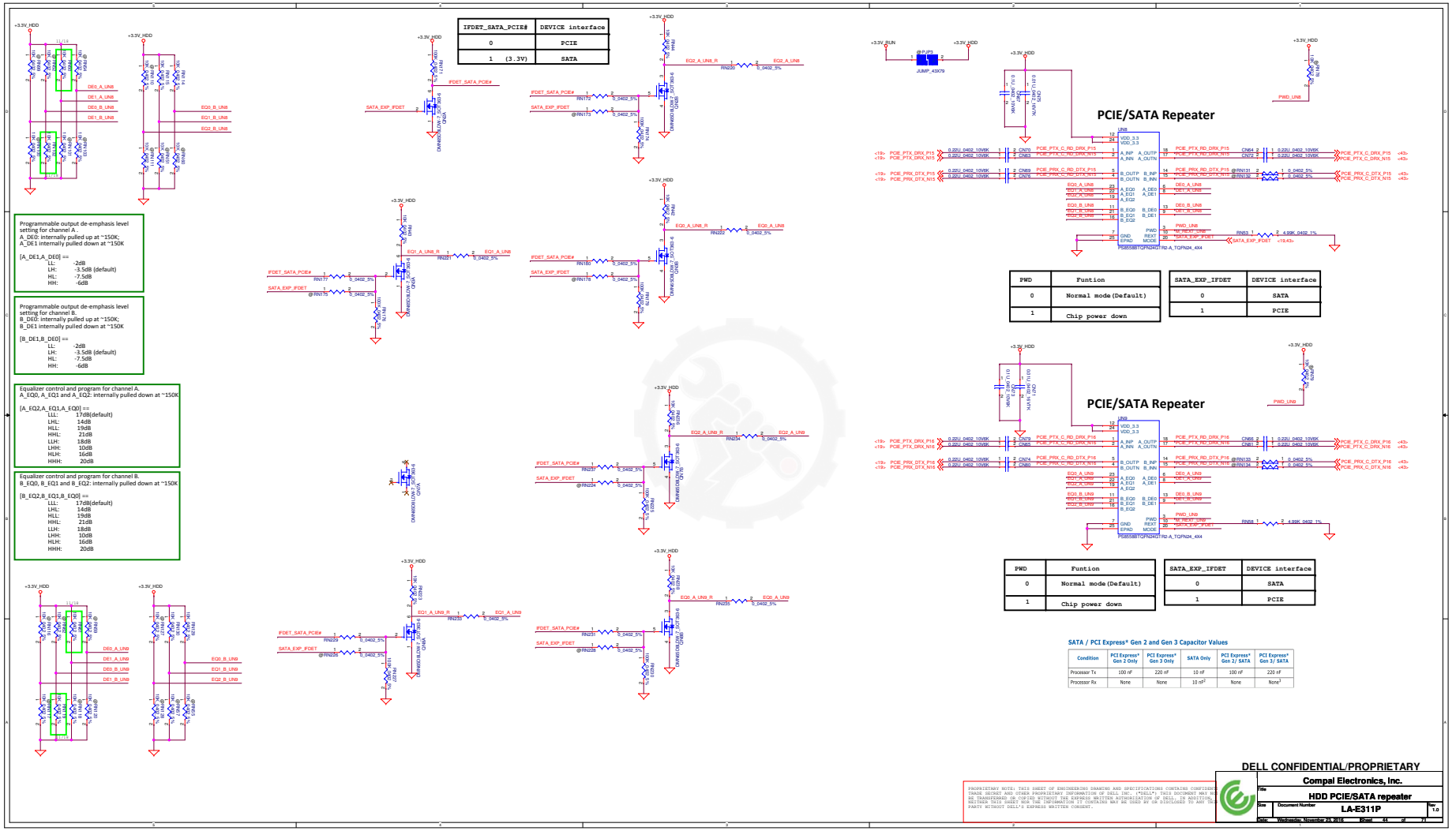
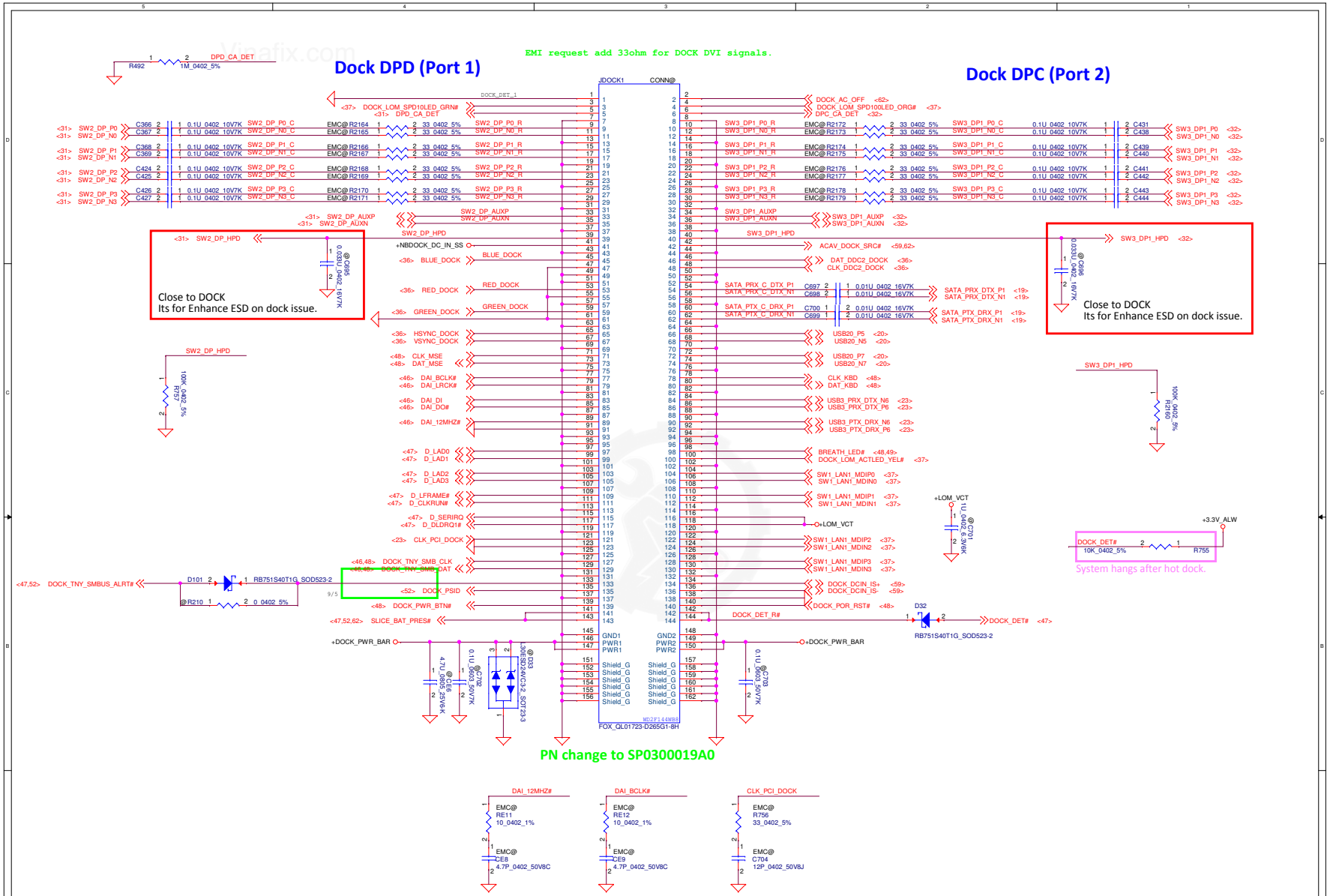

IFDET_SATA_PCIE#
DEVICE interface
0
PCIE
1 (3.3V)
SATA
Programmable output de-emphasis level setting for channel A .
A_DE0: internally pulled up at ~150K;
A_DE1 internally pulled down at ~150K
[A_DE1,A_DE0] ==
LL: -2dB
LH: -3.5dB (default)
HL: -7.5dB
HH: -6dB
Programmable output de-emphasis level setting for channel B.
B_DE0: internally pulled up at ~150K;
B_DE1 internally pulled down at ~150K
[B_DE1,B_DE0] ==
LL: -2dB
LH: -3.5dB (default)
HL: -7.5dB
HH: -6dB
Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K
[A_EQ2,A_EQ1,A_EQ0] ==
LLL: 17dB(default)
LHL: 14dB
HLL: 19dB
HHL: 21dB
LLH: 18dB
LHH: 10dB
HLH: 16dB
HHH: 20dB
Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K
[B_EQ2,B_EQ1,B_EQ0] ==
LLL: 17dB(default)
LHL: 14dB
HLL: 19dB
HHL: 21dB
LLH: 18dB
LHH: 10dB
HLH: 16dB
HHH: 20dB
PCIE/SATA Repeater
PWD
Funtion
0
Normal mode(Default)
1
Chip power down
SATA_EXP_IFDET
DEVICE interface
0
SATA
1
PCIE
SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values
Condition
PCI Express* Gen 2 Only
PCI Express* Gen 3 Only
SATA Only
PCI Express* Gen 2/ SATA
PCI Express* Gen 3/ SATA
Processor Tx
100 nF
220 nF
10 nF
100 nF
220 nF
Processor Rx
None
None
10 nF2
None
None2
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
HDD PCIE/SATA repeater
LA-E311P
Wednesday, November 25, 2015



Compal Electronics, Inc.

Title: Docking

Size: | Document Number: LA-E311P | Rev: 1.0

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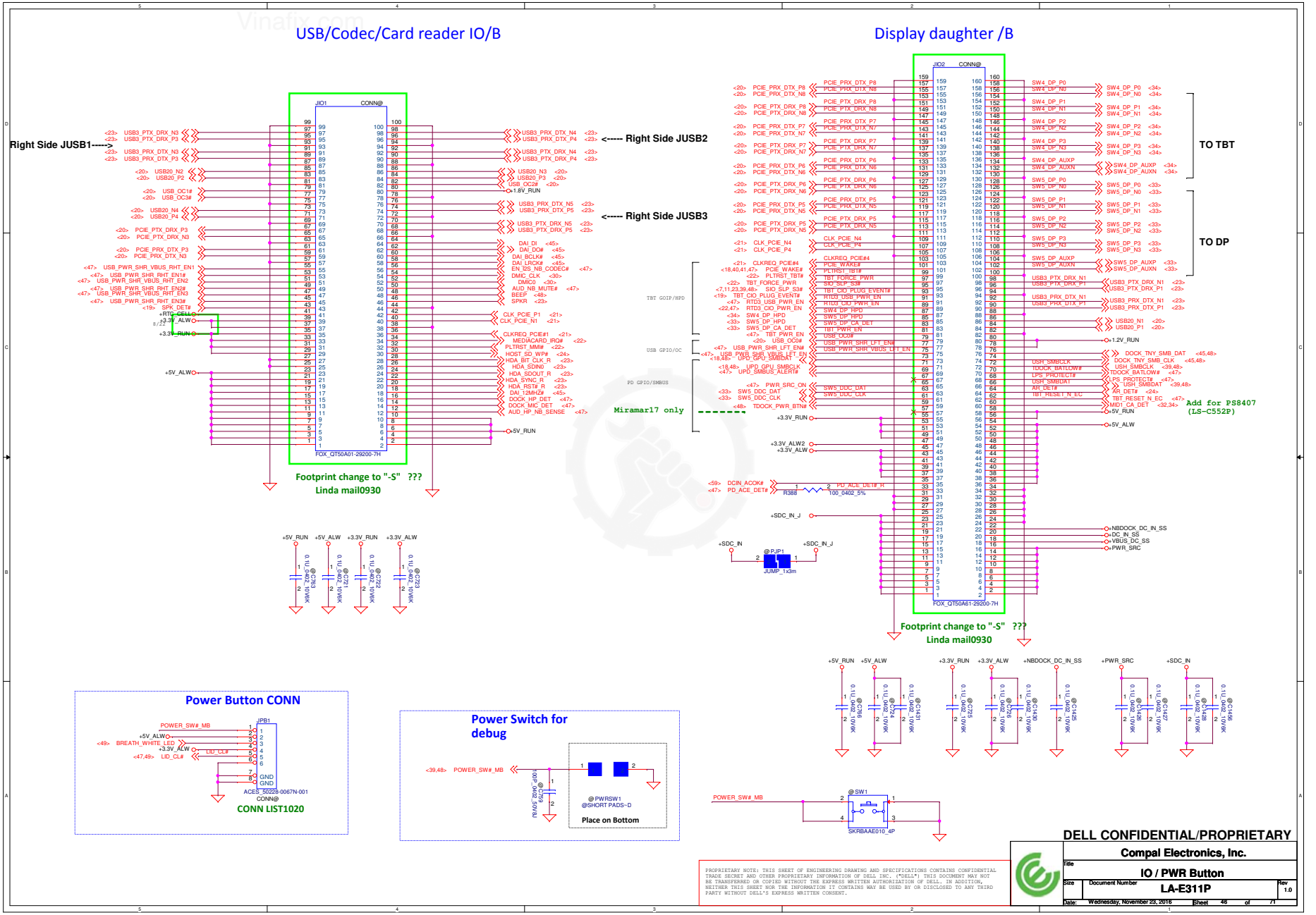
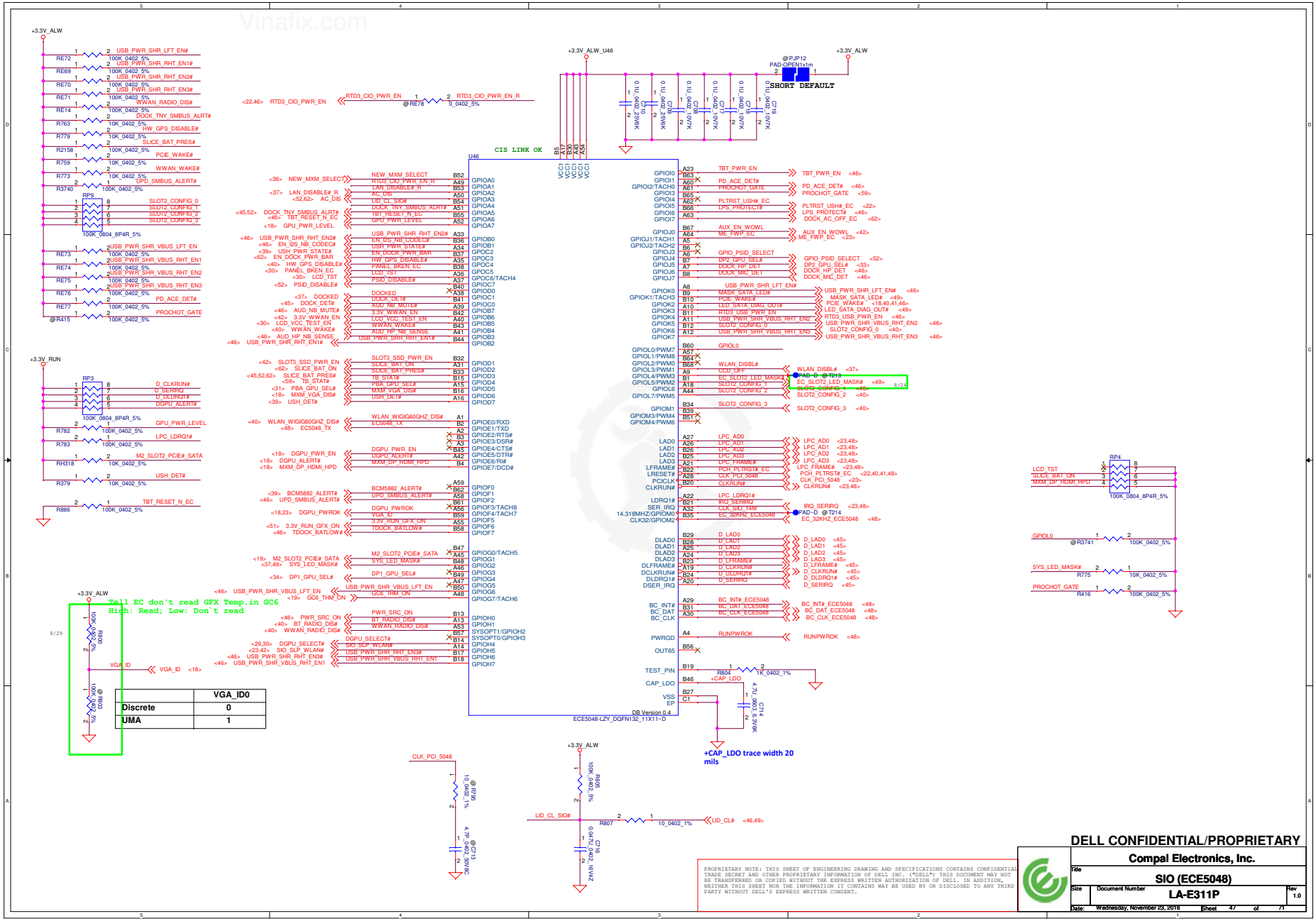

USB/Codec/Card reader IO/B
Display daughter /B
Right Side JUSB1----->
<----- Right Side JUSB2
<----- Right Side JUSB3
JIO1
CONN@
FOX_QT50A01-29200-7H
JIO2
CONN@
FOX_QT50A61-29200-7H
TO TBT
TO DP
Footprint change to "-S" ???
Linda mail0930
Miramar17 only
Add for PS8407
(LS-C552P)
Power Button CONN
CONN LIST1020
Power Switch for debug
@PWRSW1
@SHORT PADS-D
Place on Bottom
SKRBAAE010_4P
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
IO / PWR Button
LA-E311P
Wednesday, November 23, 2016


+3.3V_ALW
+3.3V_RUN
+3.3V_ALW_U46
U46
CIS LINK OK
SHORT DEFAULT
@PJP12
PAD-OPEN1x1m
@RE78
RTD3_CIO_PWR_EN
RTD3_CIO_PWR_EN_R
0_0402_5%
USB_PWR_SHR_LFT_EN#
USB_PWR_SHR_RHT_EN1#
USB_PWR_SHR_RHT_EN2#
USB_PWR_SHR_RHT_EN3#
WWAN_RADIO_DIS#
DOCK_TNY_SMBUS_ALRT#
HW_GPS_DISABLE#
SLICE_BAT_PRES#
PCIE_WAKE#
WWAN_WAKE#
UPD_SMBUS_ALRT#
USB_PWR_SHR_VBUS_LFT_EN
USB_PWR_SHR_VBUS_RHT_EN1
USB_PWR_SHR_VBUS_RHT_EN2
USB_PWR_SHR_VBUS_RHT_EN3
PD_ACE_DET#
PROCHOT_GATE
SLOT2_CONFIG_0
SLOT2_CONFIG_1
SLOT2_CONFIG_2
SLOT2_CONFIG_3
RP9
RP3
RP4
100K_0804_8P4R_5%
D_CLKRUN#
D_SERIRQ
D_DLDRQ1#
DGPU_ALERT#
GPU_PWR_LEVEL
LPC_LDRQ1#
M2_SLOT2_PCIE#_SATA
USH_DET#
TBT_RESET_N_EC
Tell EC don't read GFX Temp.in GC6
High: Read; Low: Don`t read
VGA_ID
VGA_ID0
Discrete
0
UMA
1
CLK_PCI_5048
LID_CL_SIO#
LID_CL#
+CAP_LDO
+CAP_LDO trace width 20 mils
ECE5048-LZY_DQFN132_11X11~D
DB Version 0.4
GPIO0
SYS_LED_MASK#
PROCHOT_GATE
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
SIO (ECE5048)
LA-E311P
Wednesday, November 23, 2016
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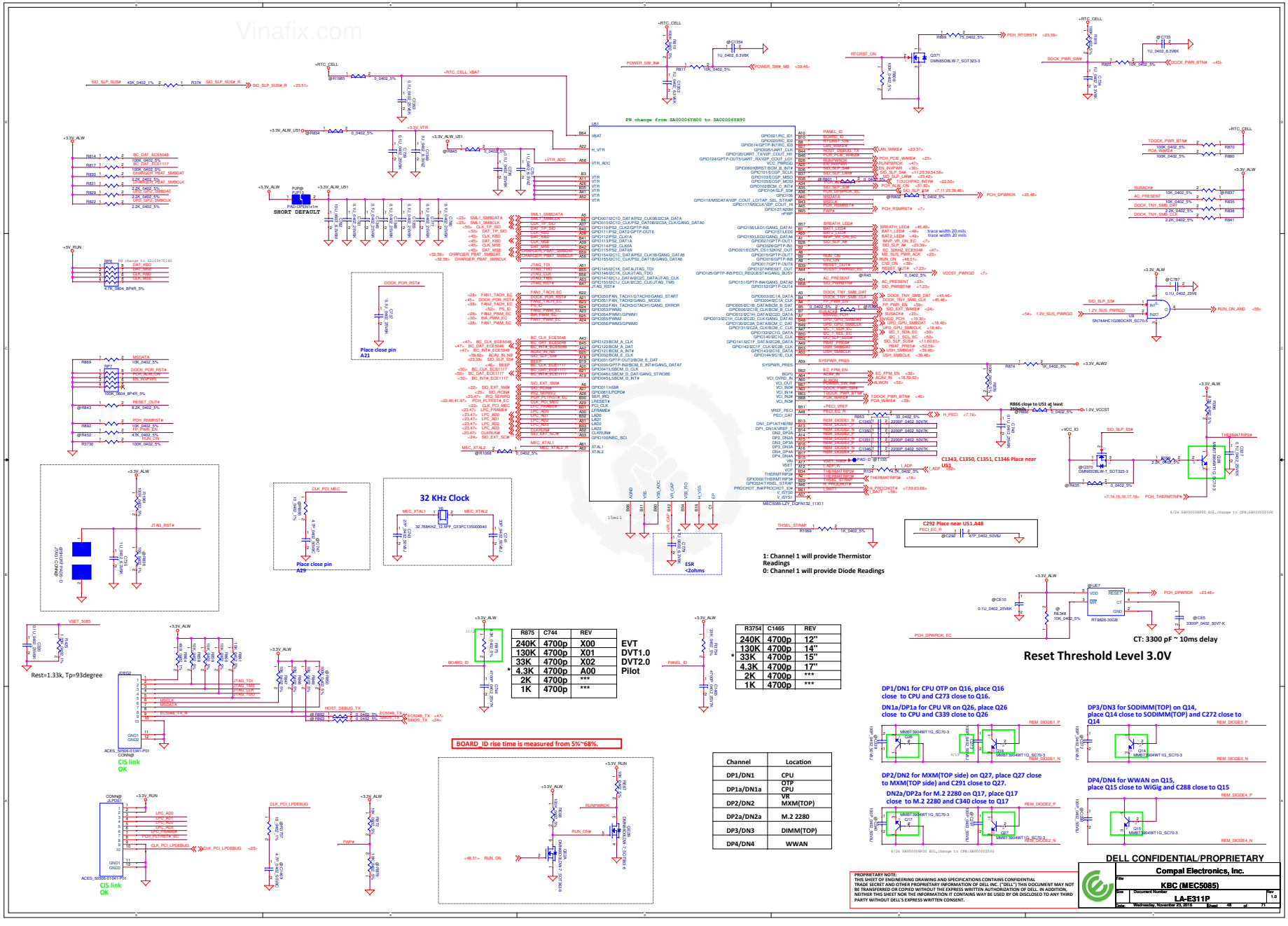
71

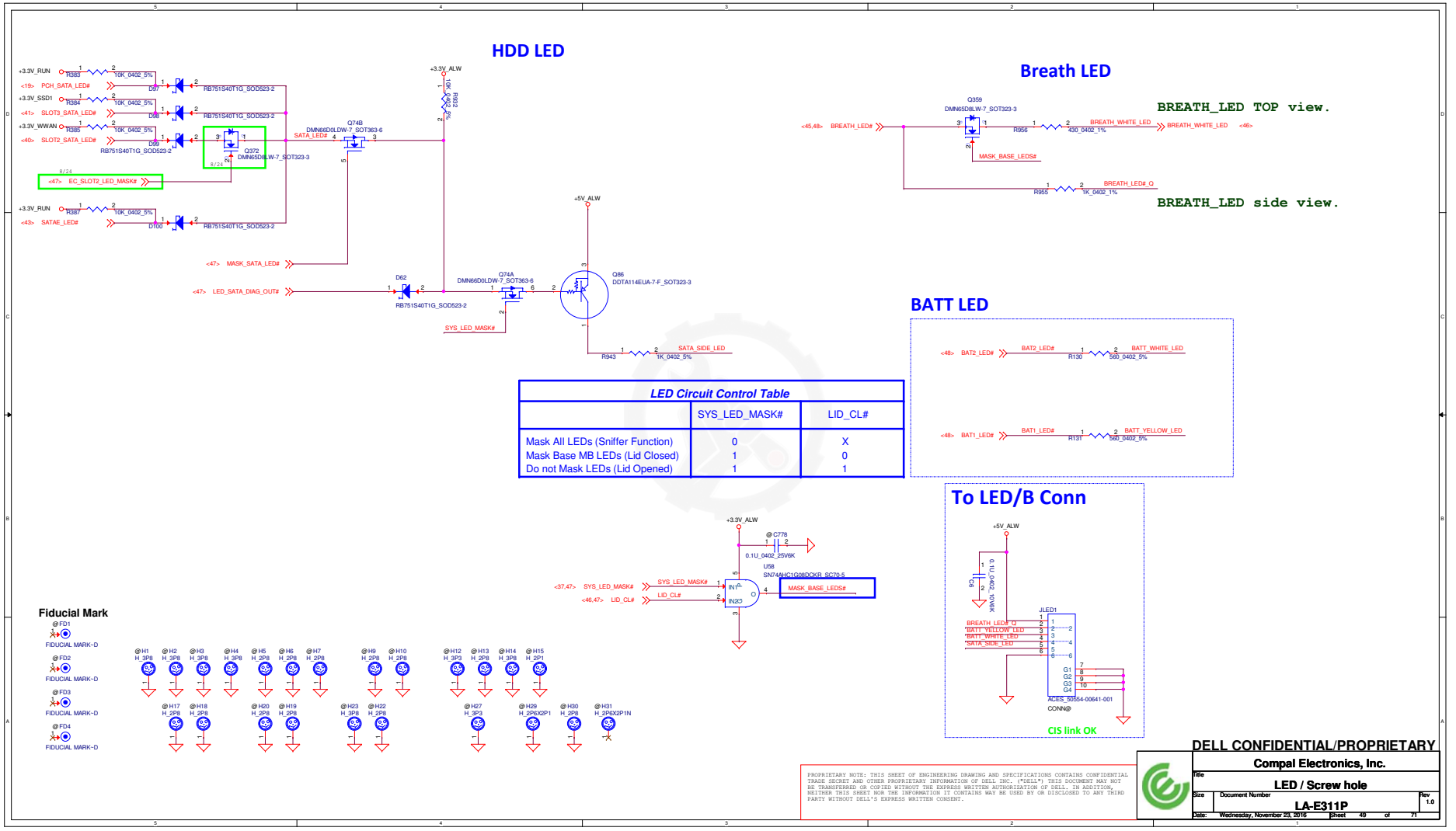


R875	C744	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
4.3K	4700p	A00
2K	4700p	***
1K	4700p	***

EVT
DVT1.0
DVT2.0
Pilot

R3754	C1465	REV
240K	4700p	12"
130K	4700p	14"
33K	4700p	15"
4.3K	4700p	17"
2K	4700p	***
1K	4700p	***

Channel	Location
DP1/DN1	CPU
DP1a/DN1a	OTP CPU
DP2/DN2	VR MXM(TOP)
DP2a/DN2a	M.2 2280
DP3/DN3	DIMM(TOP)
DP4/DN4	WWAN



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

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Compal Electronics, Inc.	
Title	LED / Screw hole
Size	Document Number: LA-E311P
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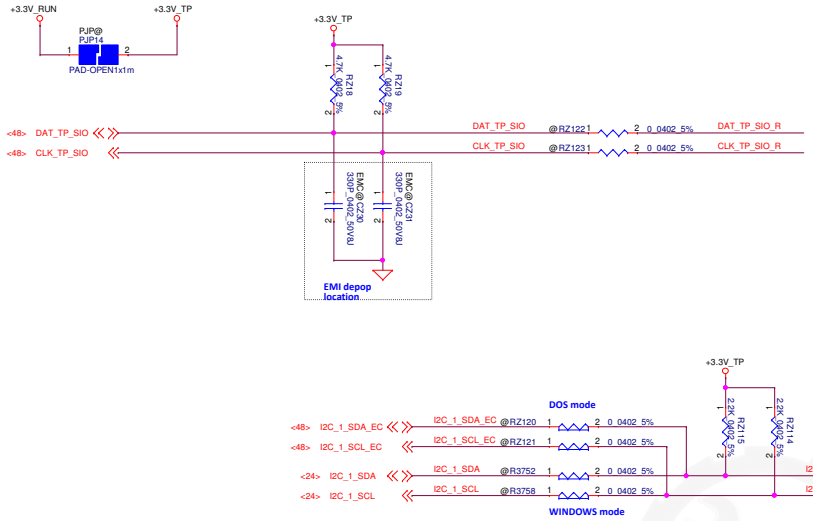
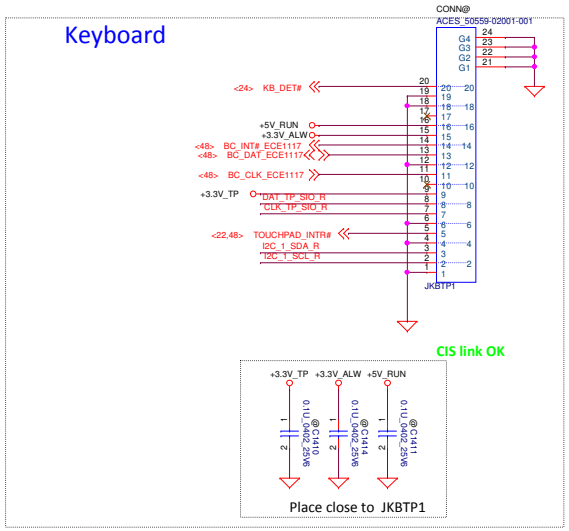
Date: Wednesday, November 23, 2016	Sheet 49 of 71

Touch Pad



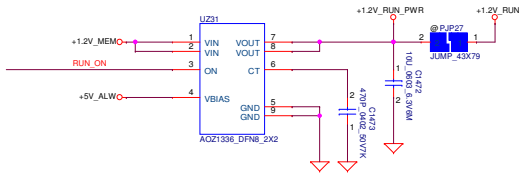
Keyboard



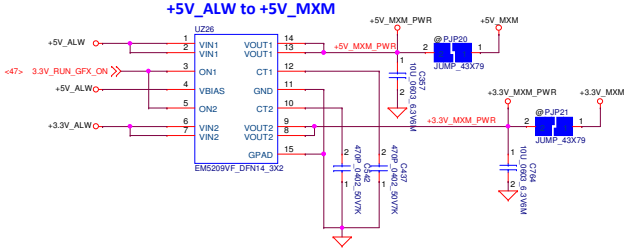
Compal Electronics, Inc.

Title	KB / TP / RSMRST#	
Size	Document Number: LA-E311P	Rev: 1.0
Date: Wednesday, November 23, 2016	Sheet 50 of 71	

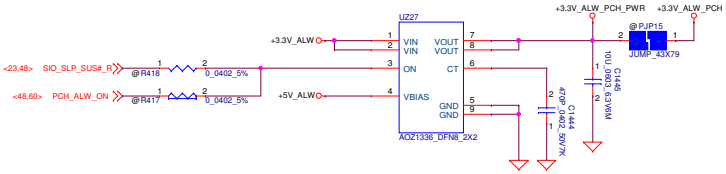
+1.2V_RUN Source



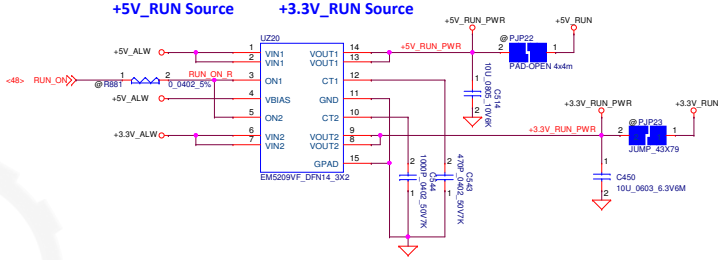
+3.3V_ALW to +3.3V_MXM
+5V_ALW to +5V_MXM



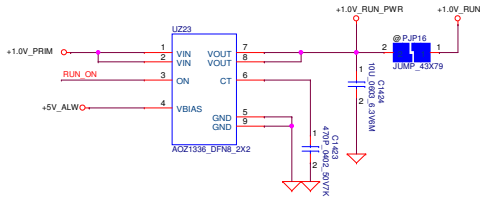
+3.3V_ALW_PCH Source



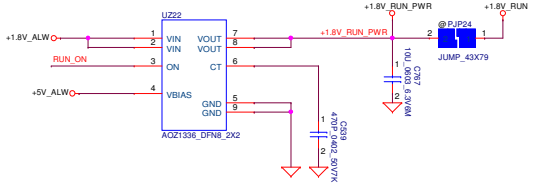
+5V_RUN Source
+3.3V_RUN Source



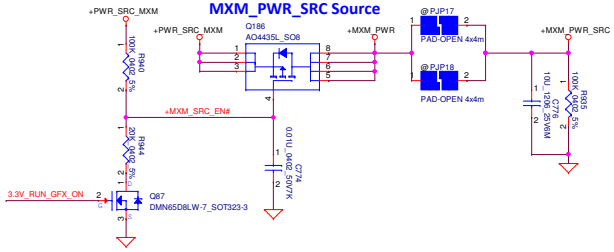
+1.0V_PRIM to +1.0V_RUN



+1.8V_RUN Source



MXM_PWR_SRC Source



Compal Electronics, Inc.	
Title	Power Control
Size	Document Number: LA-E311P
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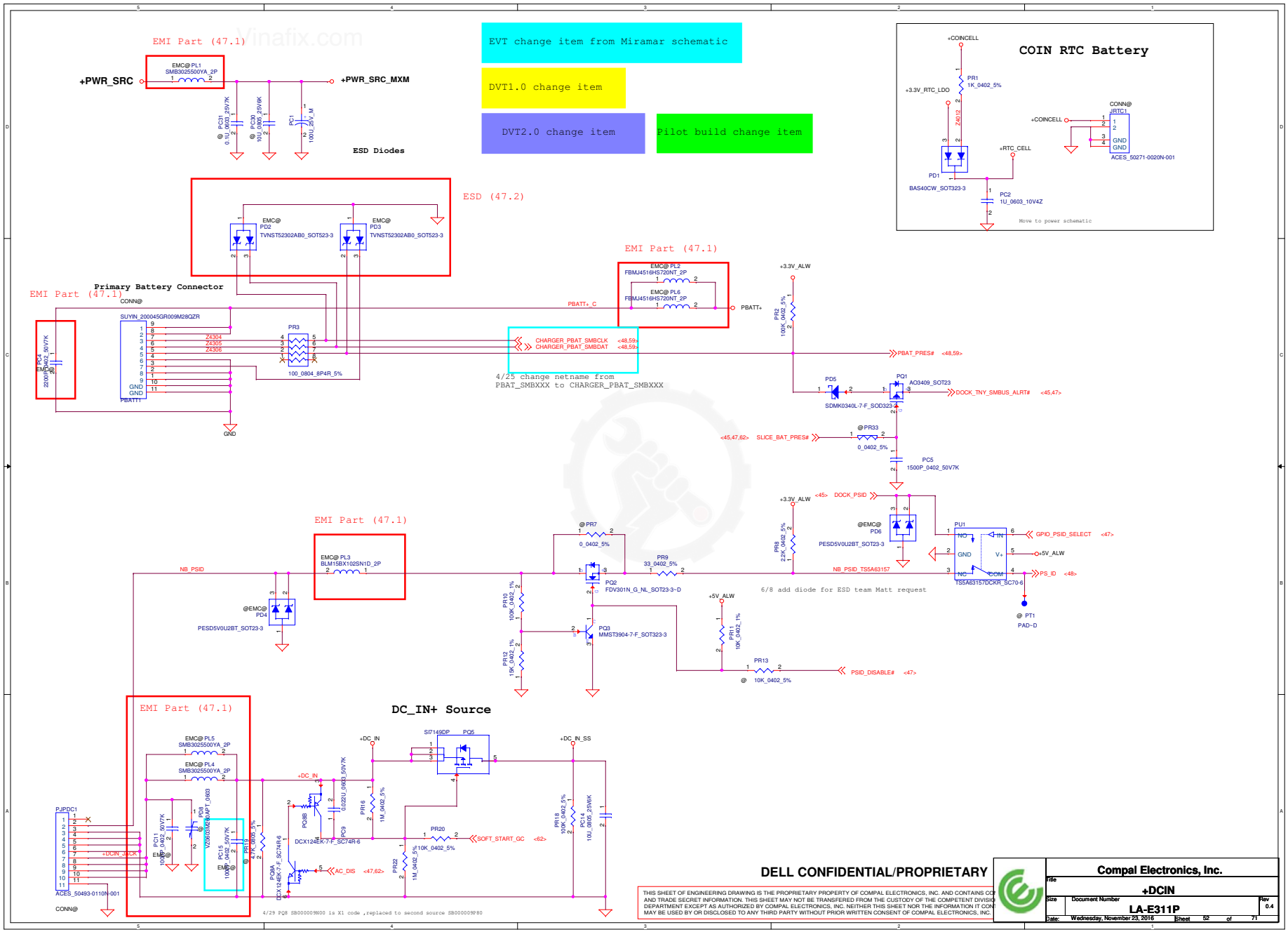
EVT change item from Miramar schematic
DVT1.0 change item
DVT2.0 change item
Pilot build change item
COIN RTC Battery
+COINCELL
+3.3V_RTC_LDO
+RTC_CELL
BAS40CW_SOT323-3
ACES_50271-0020N-001
Move to power schematic
EMI Part (47.1)
+PWR_SRC
+PWR_SRC_MXM
ESD Diodes
ESD (47.2)
TVNST52302AB0_SOT523-3
Primary Battery Connector
SUYIN_200045GR009M28QZR
100_0804_8P4R_5%
4/25 change netname from
PBAT_SMBXXX to CHARGER_PBAT_SMBXXX
CHARGER_PBAT_SMBCLK
CHARGER_PBAT_SMBDAT
PBATT+_C
PBATT+
PBAT_PRES#
DOCK_TNY_SMBUS_ALRT#
SLICE_BAT_PRES#
DOCK_PSID
GPID_PSID_SELECT
PS_ID
NB_PSID
PESD5V0U2BT_SOT23-3
SDMK0340L-7-F_SOD323-2
AO3409_SOT23
PESD5V0U2BT_SOT23-3
TS5A63157DCKR_SC70-6
FDV301N_G_NL_SOT23-3-D
MMST3904-7-F_SOT323-3
6/8 add diode for ESD team Matt request
PSID_DISABLE#
DC_IN+ Source
SI7149DP_PQ5
DCX124EK-7-F_SC74R-6
SOFT_START_GC
AC_DIS
4/29 PQ8 SB000009N00 is X1 code ,replaced to second source SB000009P80
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+DCIN
LA-E311P
0.4
Wednesday, November 23, 2016
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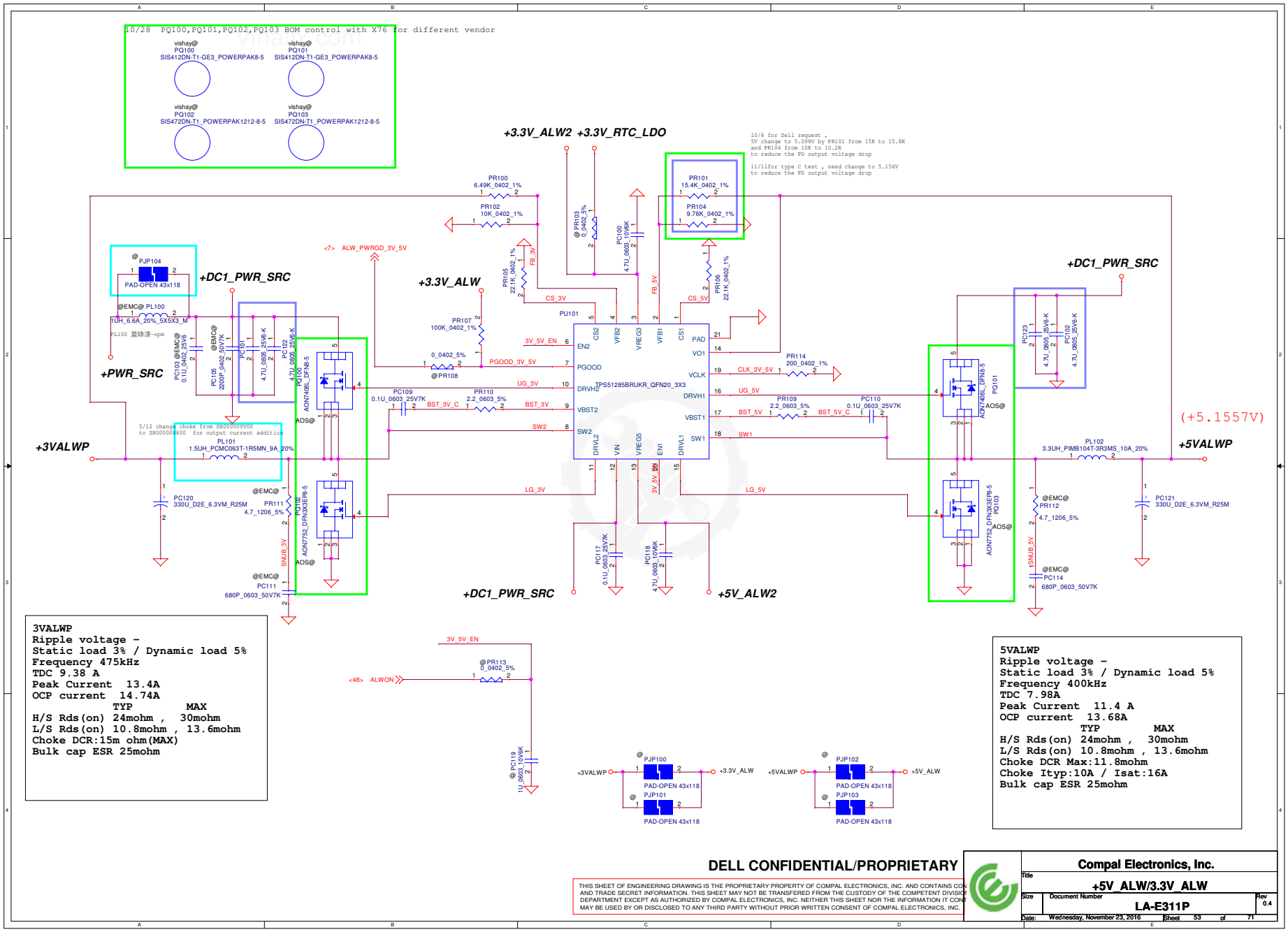
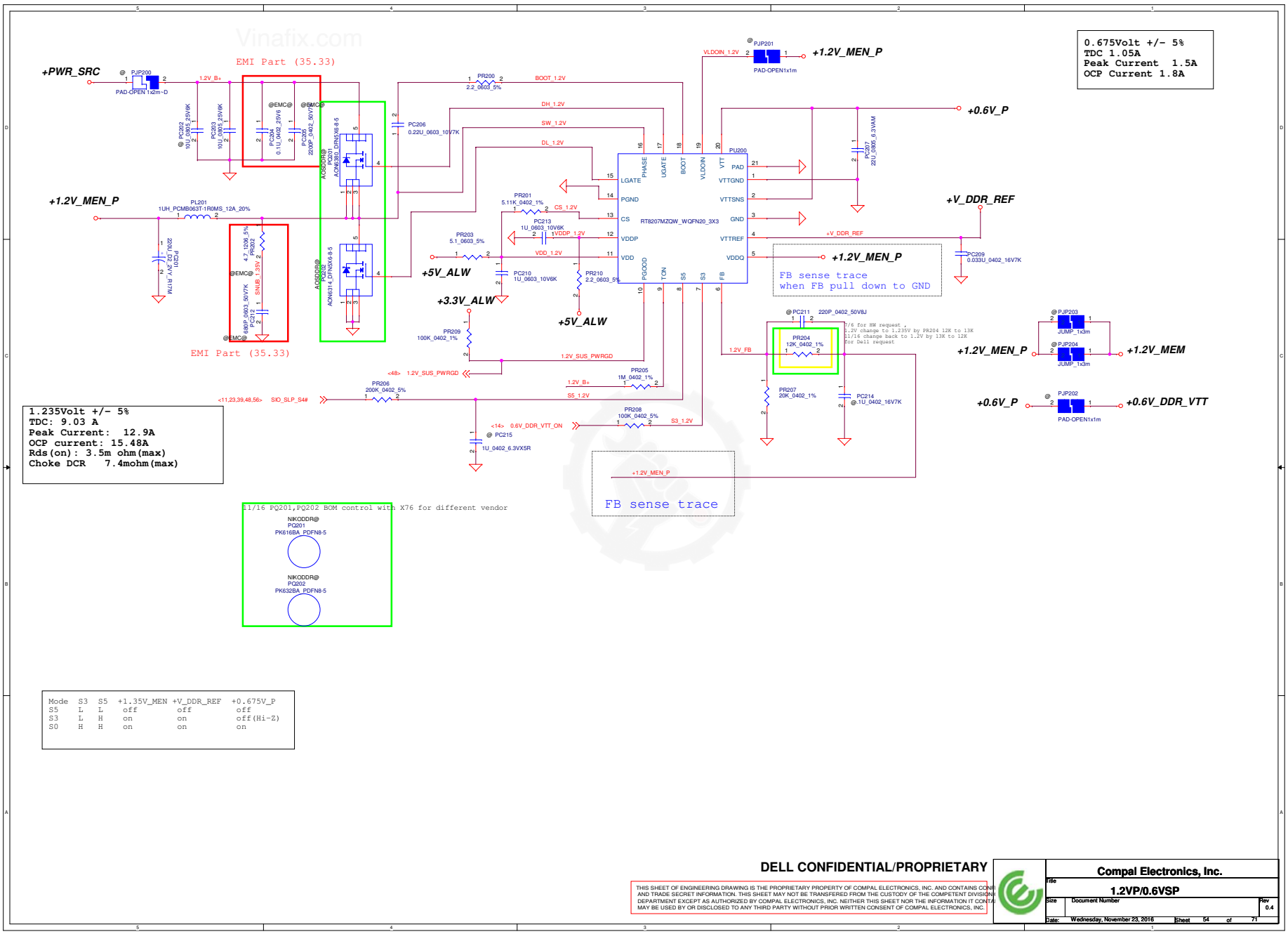
71




0.675Volt +/- 5%
TDC 1.05A
Peak Current 1.5A
OCP Current 1.8A
+PWR_SRC
PJP200
PAD-OPEN 1x2m~D
EMI Part (35.33)
PJP201
PAD-OPEN1x1m
+1.2V_MEN_P
+0.6V_P
+V_DDR_REF
PL201
1UH_PCMB063T-1R0MS_12A_20%
PU200
RT8207MZQW_WQFN20_3X3
PHASE
LGATE
PGND
UGATE
BOOT
VLDOIN
VTT
PAD
VTTGND
VTTSNS
GND
VTTREF
VDDQ
CS
VDDP
VDD
PGOOD
TON
S5
S3
FB
+5V_ALW
+3.3V_ALW
FB sense trace
when FB pull down to GND
FB sense trace
1.235Volt +/- 5%
TDC: 9.03 A
Peak Current: 12.9A
OCP current: 15.48A
Rds(on): 3.5m ohm(max)
Choke DCR 7.4mohm(max)
11/16 PQ201,PQ202 BOM control with X76 for different vendor
NIKODDR@
PQ201
PK616BA_PDFN8-5
NIKODDR@
PQ202
PK632BA_PDFN8-5
PJP203
JUMP_1x3m
PJP204
JUMP_1x3m
+1.2V_MEM
PJP202
PAD-OPEN1x1m
+0.6V_DDR_VTT
Mode S3 S5 +1.35V_MEN +V_DDR_REF +0.675V_P
S5 L L off off off
S3 L H on on off(Hi-Z)
S0 H H on on on
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MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
1.2VP/0.6VSP
Wednesday, November 23, 2016
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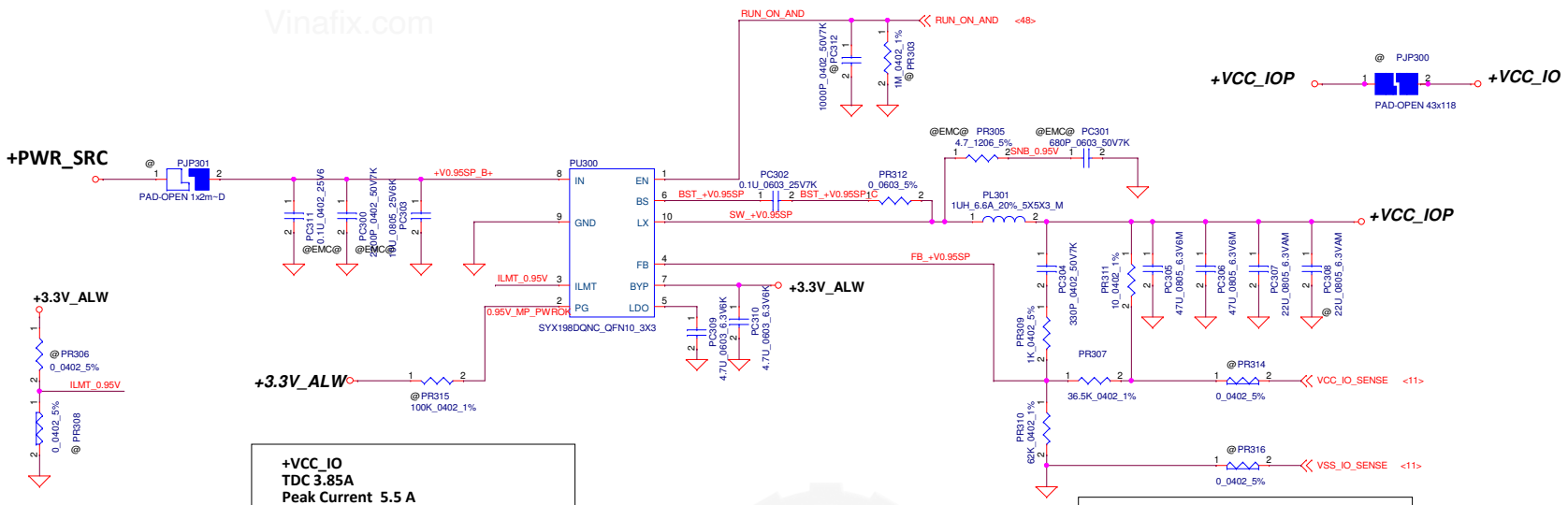

+VCC_IO
TDC 3.85A
Peak Current 5.5 A
OCP Current 8 A

	TYP	MAX
Choke DCR	13.0mohm ,	14.0mohm

proximal
PR311 0 ohm PR314 10 ohm PR316 10 ohm

remote
PR311 10 ohm PR314 0 ohm PR316 0 ohm

Compal Electronics, Inc.		
Title: +VCC_IO 0.95V		
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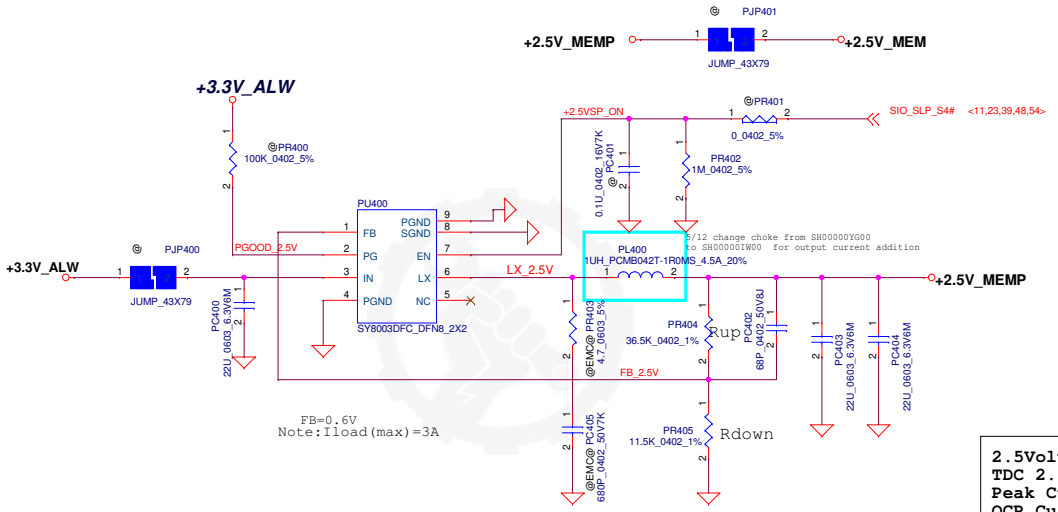
Date: Wednesday, November 23, 2016	Sheet 55 of 71	



2.5Volt
TDC 2.8A
Peak Current 4A
OCP Current 4.8A

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

Compal Electronics, Inc.		
Title: +2.5V_MEM		
Size	Document Number: LA-E311P	Rev: 0.4
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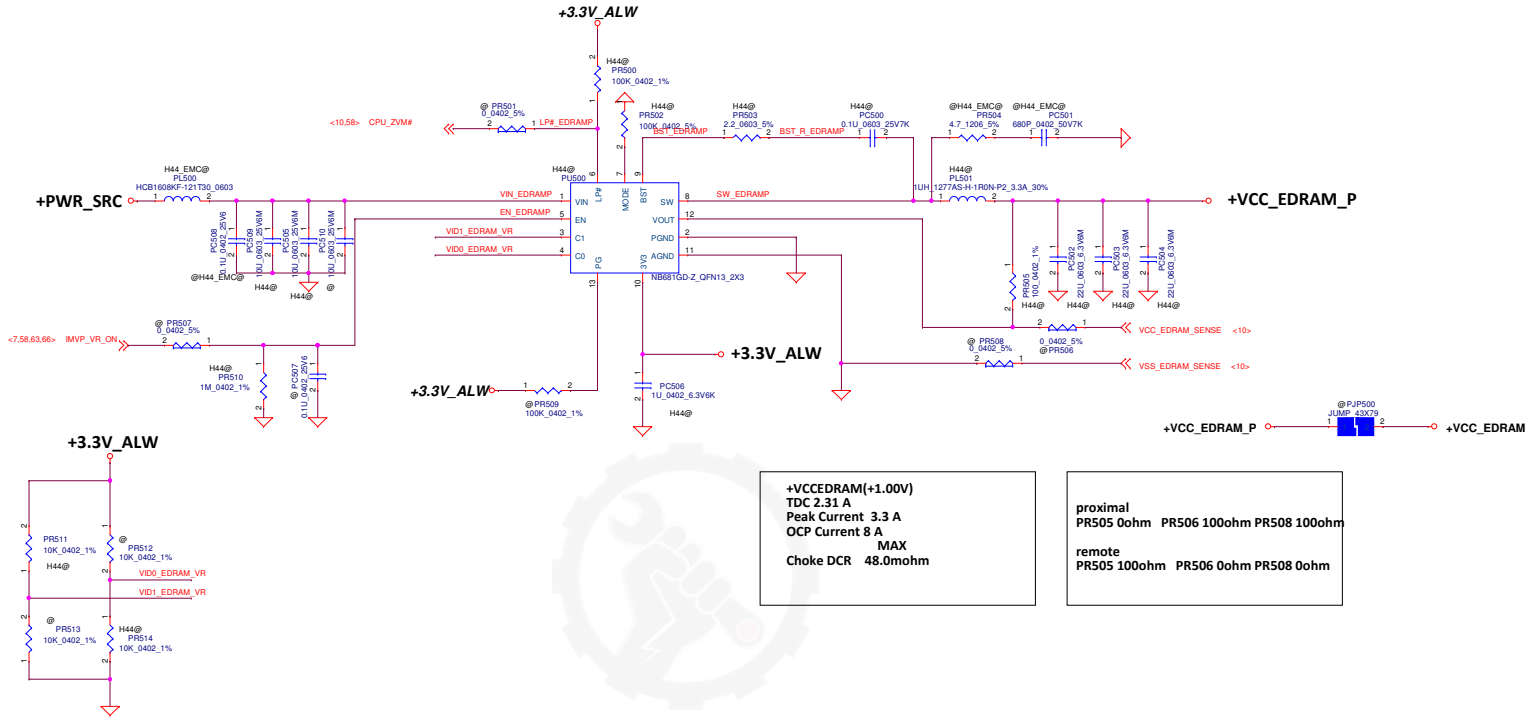
Note:Use VCCSA_SEL to switch High & Low Level for VID[1]

Only H44e



+VCCEDRAM(+1.00V)
TDC 2.31 A
Peak Current 3.3 A
OCP Current 8 A
MAX
Choke DCR 48.0mohm

proximal
PR505 0ohm PR506 100ohm PR508 100ohm

remote
PR505 100ohm PR506 0ohm PR508 0ohm

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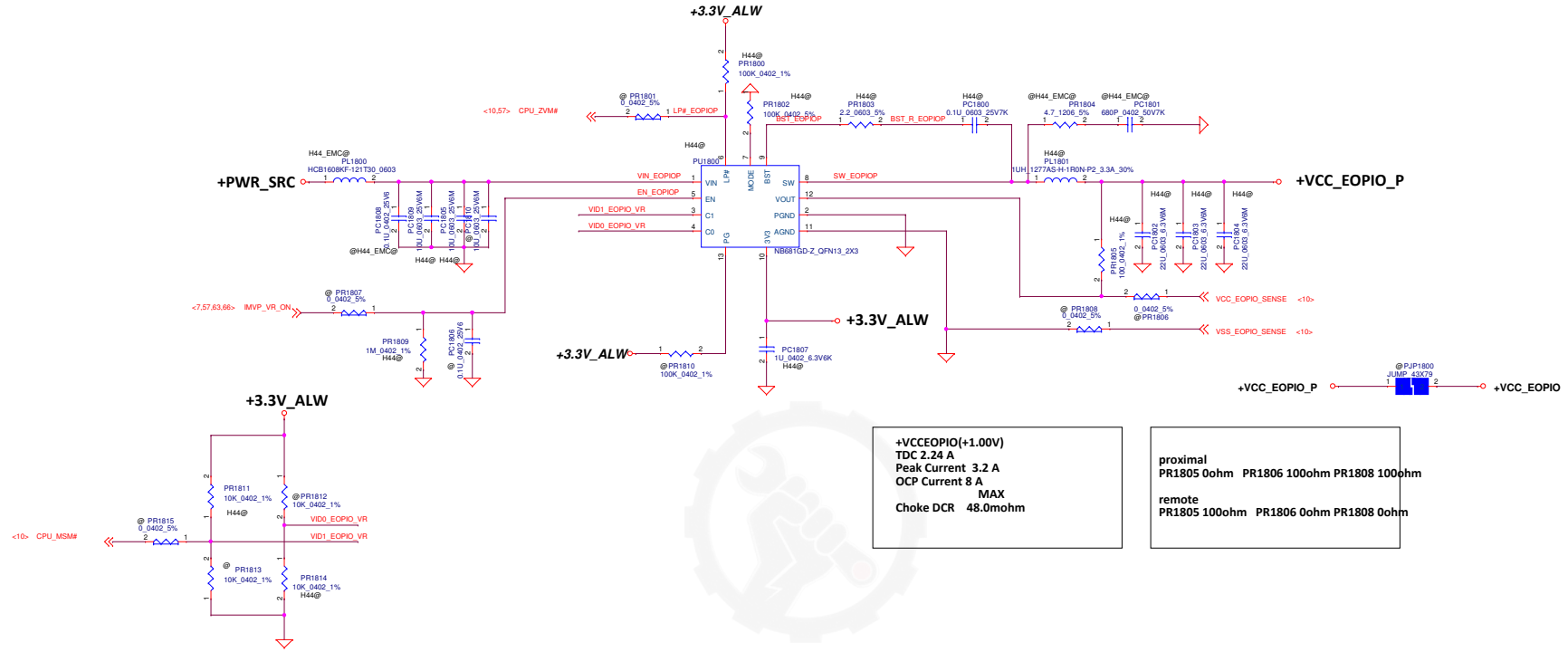
Compal Electronics, Inc.

Title: +VCCEDRAM, 1V

Size: | Document Number: LA-E311P | Rev: 0.4

Date: Wednesday, November 23, 2016 | Sheet 57 of 71

Only H44e



+VCCEOPIO(+1.00V)
TDC 2.24 A
Peak Current 3.2 A
OCP Current 8 A
MAX
Choke DCR 48.0mohm

proximal
PR1805 0ohm PR1806 100ohm PR1808 100ohm

remote
PR1805 100ohm PR1806 0ohm PR1808 0ohm

Compal Electronics, Inc.
Title: +VCCEOPIO, 1V
Size: Document Number: LA-E311P
Rev: 0.4
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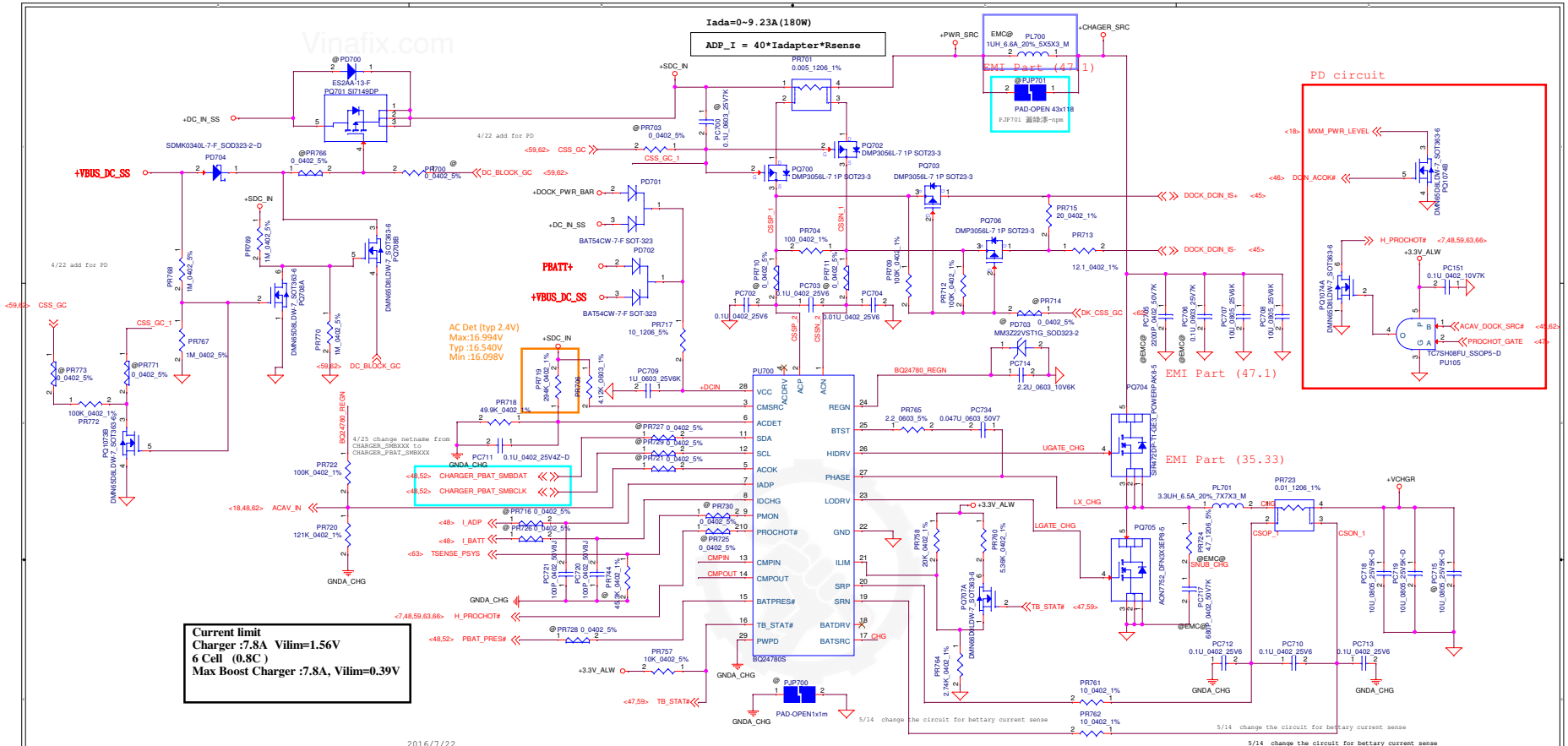
Iada=0~9.23A(180W)
ADP_I = 40*Iadapter*Rsense
PD circuit
EMI Part (47.1)
EMI Part (35.33)
AC.Det (typ 2.4V)
Max:16.994V
Typ :16.540V
Min :16.098V
Current limit
Charger :7.8A Vilim=1.56V
6 Cell (0.8C)
Max Boost Charger :7.8A, Vilim=0.39V
2016/7/22
For Temp voltage test ,
+DC_IN setting for ACAVIN_NB need less than 17.55V ,
so change PR737 from SD034665380
(S RES 1/16W 665K +-1% 0402) to
SD034634380(S RES 1/16W 634K +-1% 0402)
+DC_IN
CMP_REF=2.3V
+DC_IN>17V then ACAV_IN_NB high
for 3cell battery 13.05V
(CMP_REF=2.3V
+DC_IN>17.6V then ACAV_IN_NB high
for 4cell battery 17.4V[Miramar setting])
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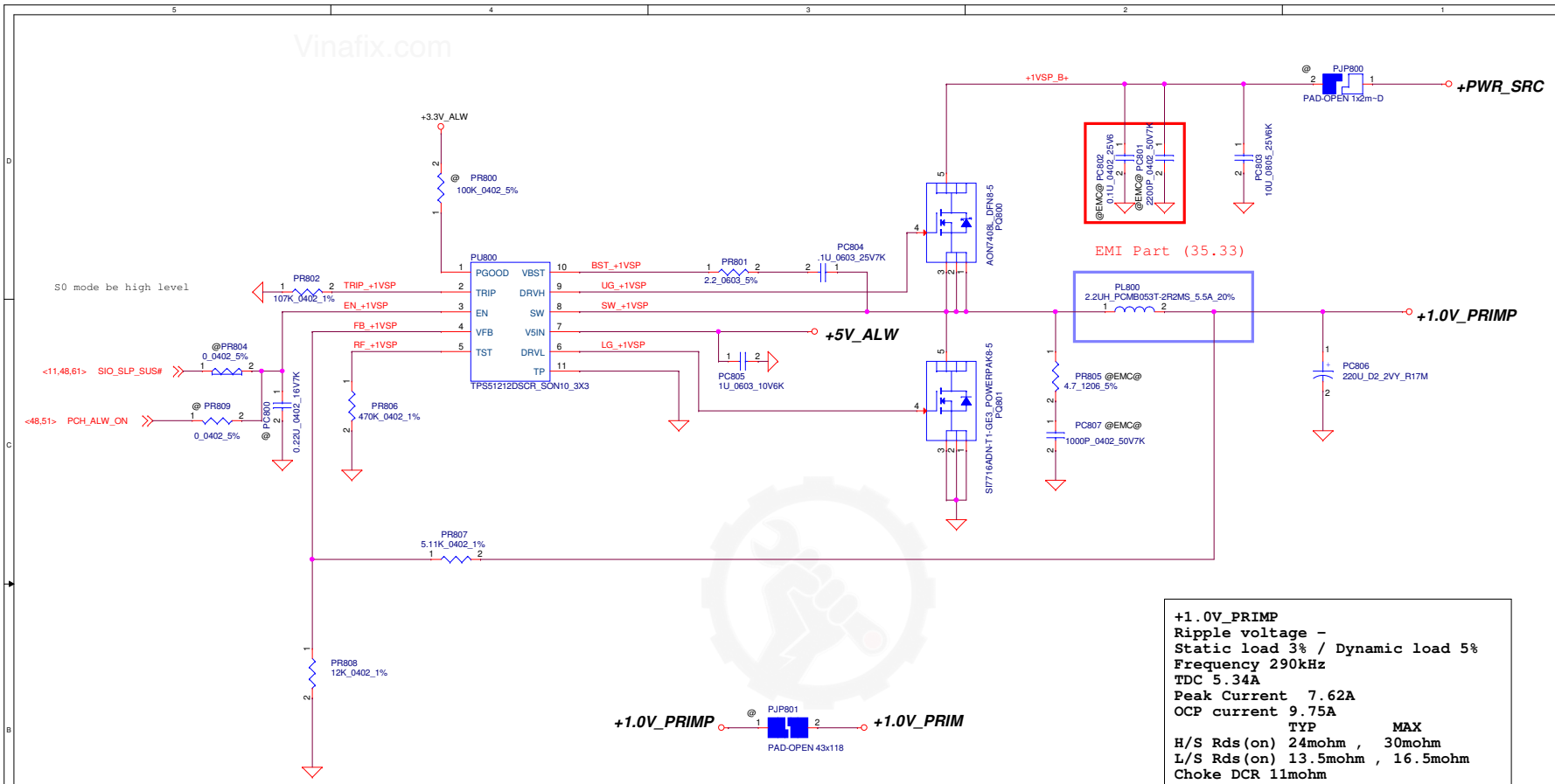
Compal Electronics, Inc.
PWR_Charger
LA-E311P




```
+1.0V_PRIMP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 290kHz
TDC 5.34A
Peak Current  7.62A
OCP current 9.75A
              TYP          MAX
H/S Rds(on) 24mohm ,   30mohm
L/S Rds(on) 13.5mohm , 16.5mohm
Choke DCR 11mohm
Bulk cap ESR 17mohm
```


Compal Electronics, Inc.	
Title	+1.0V_PRIM
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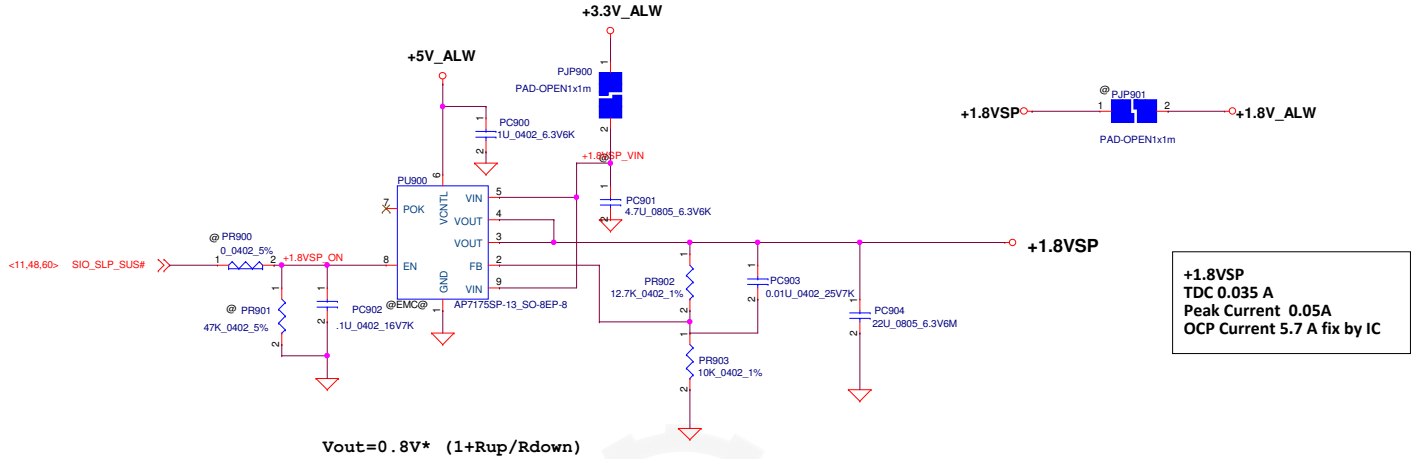


Vout=0.8V* (1+Rup/Rdown)

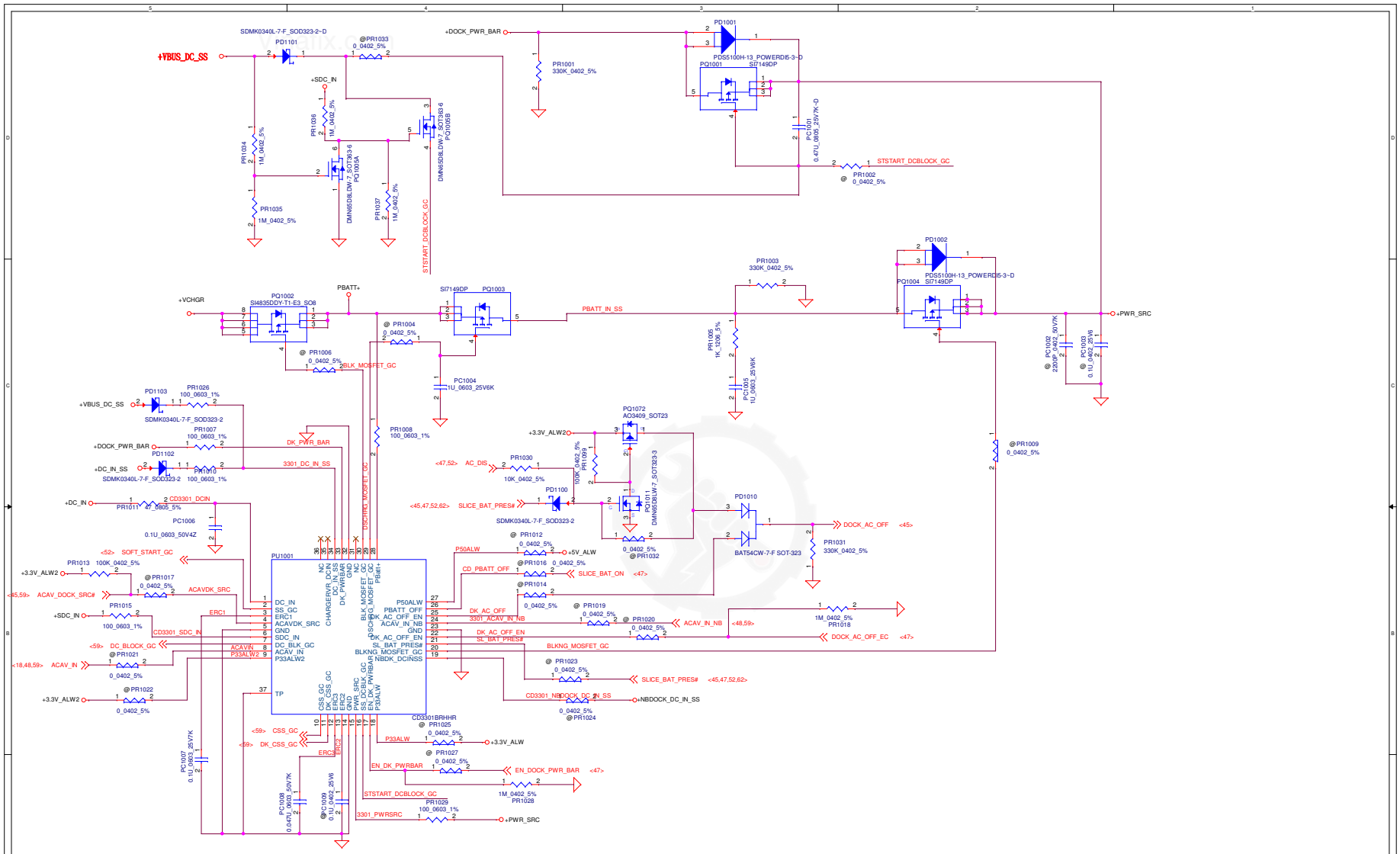
+1.8VSP
TDC 0.035 A
Peak Current 0.05A
OCP Current 5.7 A fix by IC

Compal Electronics, Inc.

Title: +1.8V_ALW

Size | Document Number: LA-E311P | Rev: 0.4

Date: Wednesday, November 23, 2016 | Sheet 61 of 71



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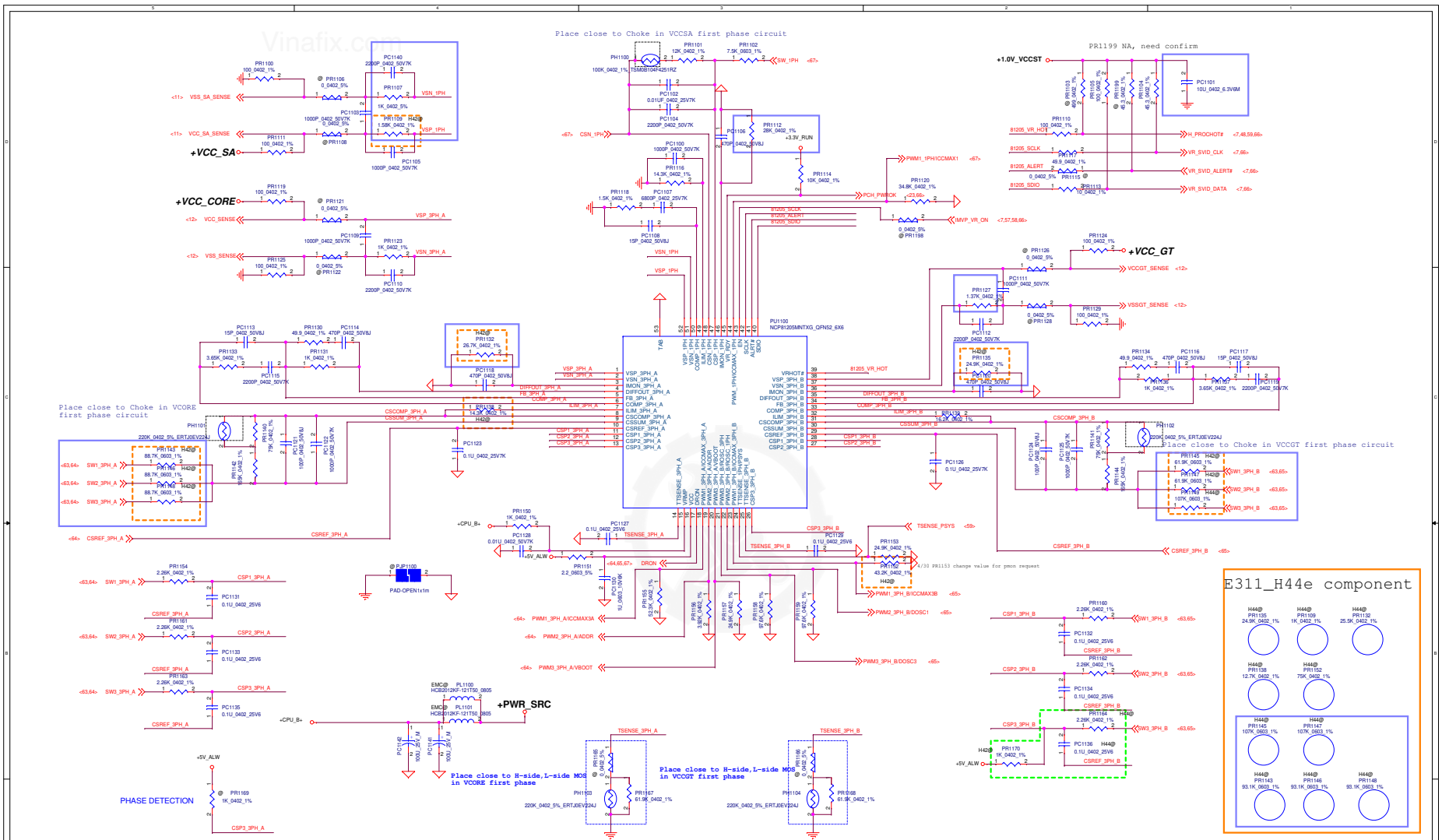
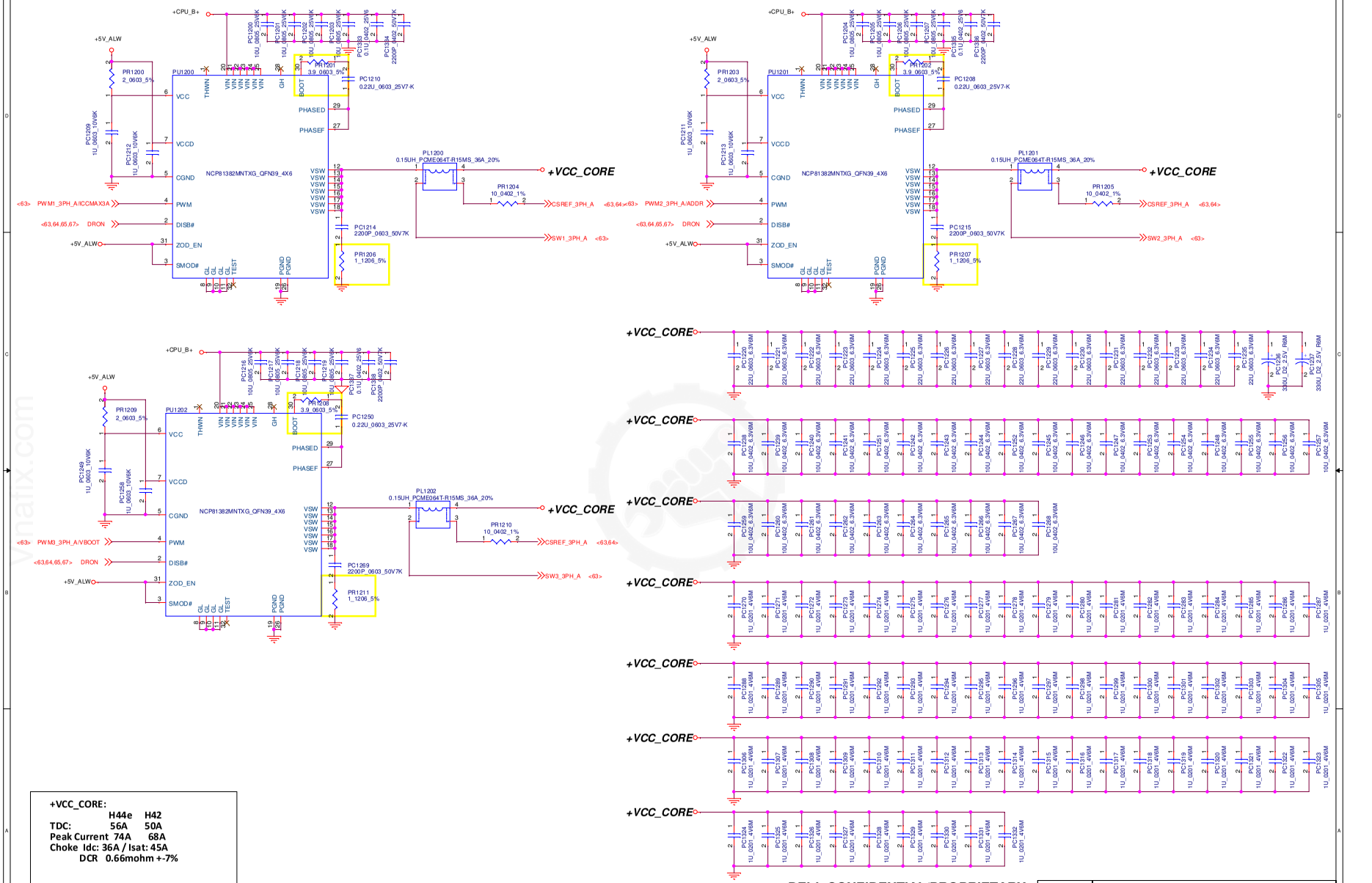
Compal Electronics, Inc.		
Title: Selector		
Size	Document Number: LA-E311P	Rev: 0.4
Date: Wednesday, November 23, 2016	Sheet 62 of 71	


Place close to Choke in VCCSA first phase circuit
PR1199 NA, need confirm
+1.0V_VCCST
+VCC_SA
+VCC_CORE
+VCC_GT
PU1100
NCP81205MNTXG_QFN52_6X6
Place close to Choke in VCORE first phase circuit
Place close to Choke in VCCGT first phase circuit
PHASE DETECTION
+PWR_SRC
Place close to H-side,L-side MOS in VCORE first phase
Place close to H-side,L-side MOS in VCCGT first phase
E311_H44e component
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
+VCORE
LA-E311P


+CPU_B+
+5V_ALW
PU1200
PU1201
PU1202
NCP81382MNTXG_QFN39_4X6
PL1200
PL1201
PL1202
0.15UH_PCME064T-R15MS_36A_20%
+VCC_CORE
PWM1_3PH_A/ICCMAX3A
PWM2_3PH_A/ADDR
PWM3_3PH_A/VBOOT
DRON
CSREF_3PH_A
SW1_3PH_A
SW2_3PH_A
SW3_3PH_A
PR1204
PR1205
PR1210
PR1211
PC1214
PC1215
PC1269
PC1250
PR1206
PR1207
PR1209
PR1200
PR1201
PR1202
PR1203
PR1208
PC1210
PC1208
PC1212
PC1213
PC1211
PC1209
PC1345
PC1350
PC1216
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PC1321
PC1322
PC1323
PC1324
PC1325
PC1326
PC1327
PC1328
PC1329
PC1330
PC1331
PC1332
+VCC_CORE:
H44e H42
TDC: 56A 50A
Peak Current 74A 68A
Choke Idc: 36A / Isat: 45A
DCR 0.66mohm +-7%
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+VCC_CORE
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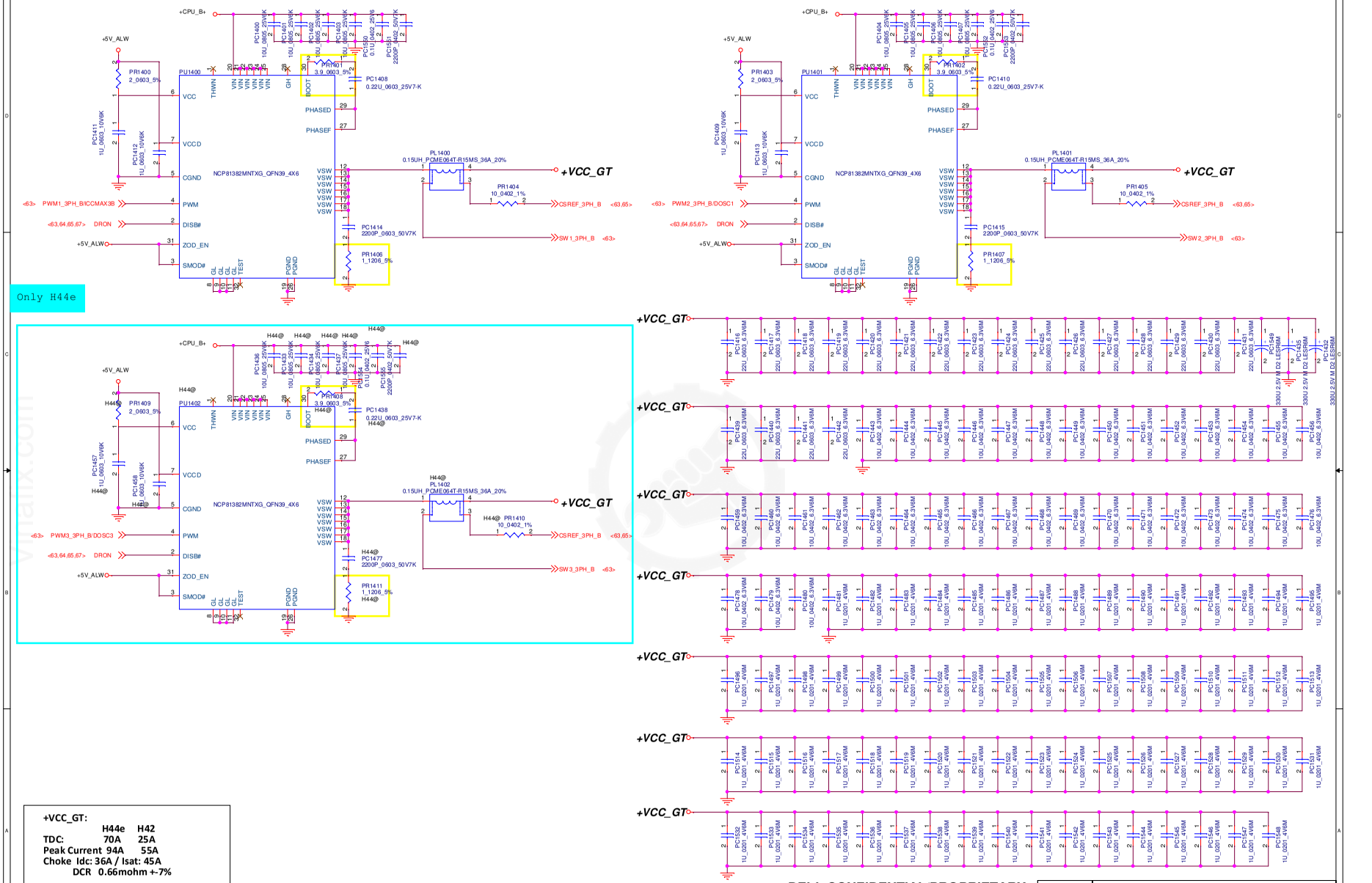
Only H44e
+CPU_B+
+5V_ALW
PU1400
PU1401
PU1402
NCP81382MNTXG_QFN39_4X6
PL1400
PL1401
PL1402
0.15UH_PCME064T-R15MS_36A_20%
+VCC_GT
CSREF_3PH_B
SW1_3PH_B
SW2_3PH_B
SW3_3PH_B
PWM1_3PH_B/ICCMAX3B
PWM2_3PH_B/DOSC1
PWM3_3PH_B/DOSC3
DRON
PR1406
PR1407
PR1411
1_1206_5%
PR1404
PR1405
PR1410
10_0402_1%
PC1414
PC1415
PC1477
2200P_0603_50V7K
0.22U_0603_25V7-K
3.9_0603_5%
2_0603_5%
1U_0603_10V6K
10U_0805_25V6K
10U_0402_6.3V6M
1U_0201_4V6M
330U_2.5V_M_D2_LESR6M
+VCC_GT:
H44e H42
TDC: 70A 25A
Peak Current 94A 55A
Choke Idc: 36A / Isat: 45A
DCR 0.66mohm +-7%
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Compal Electronics, Inc.
+VCC_GT
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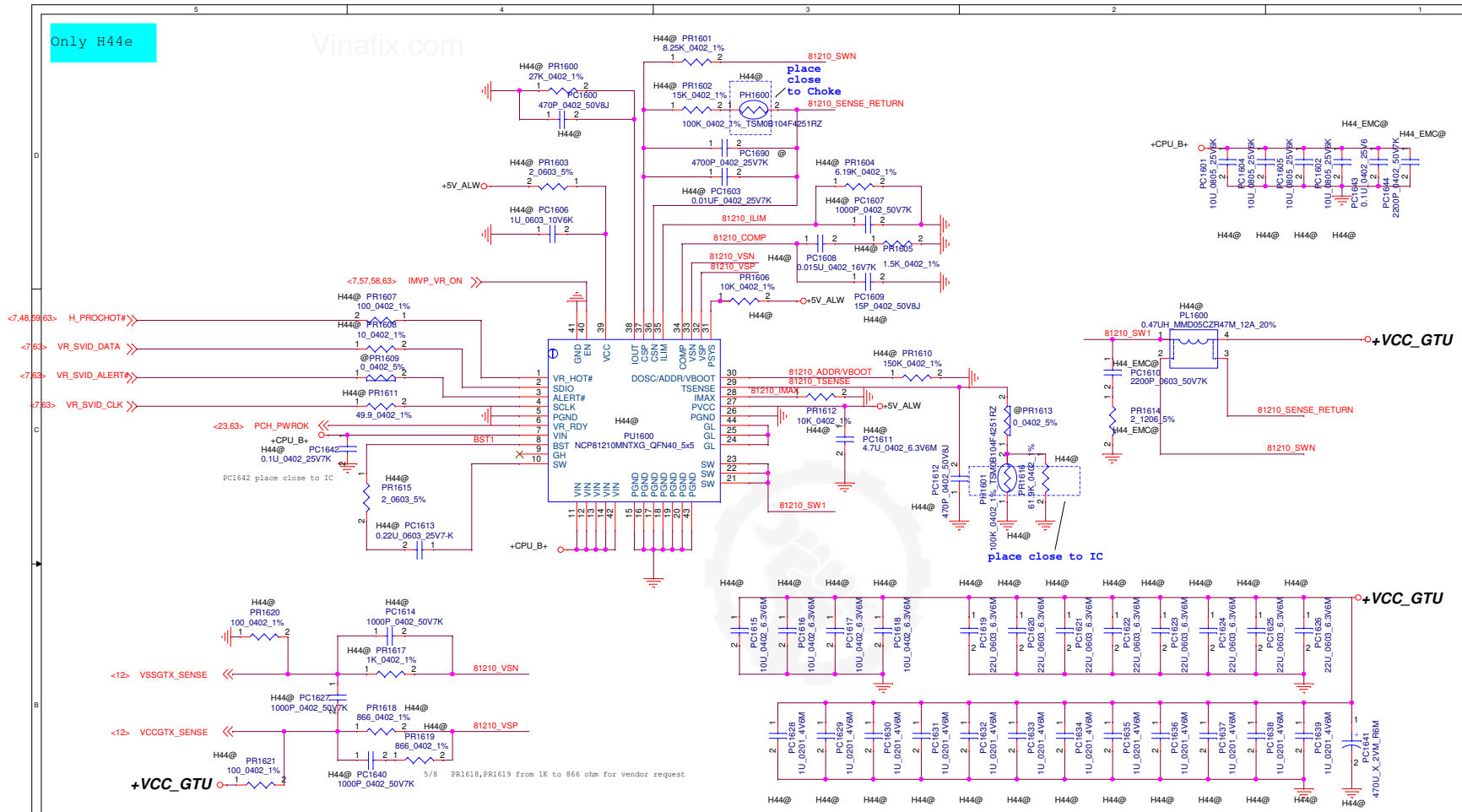

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Title: +VCC_GTX

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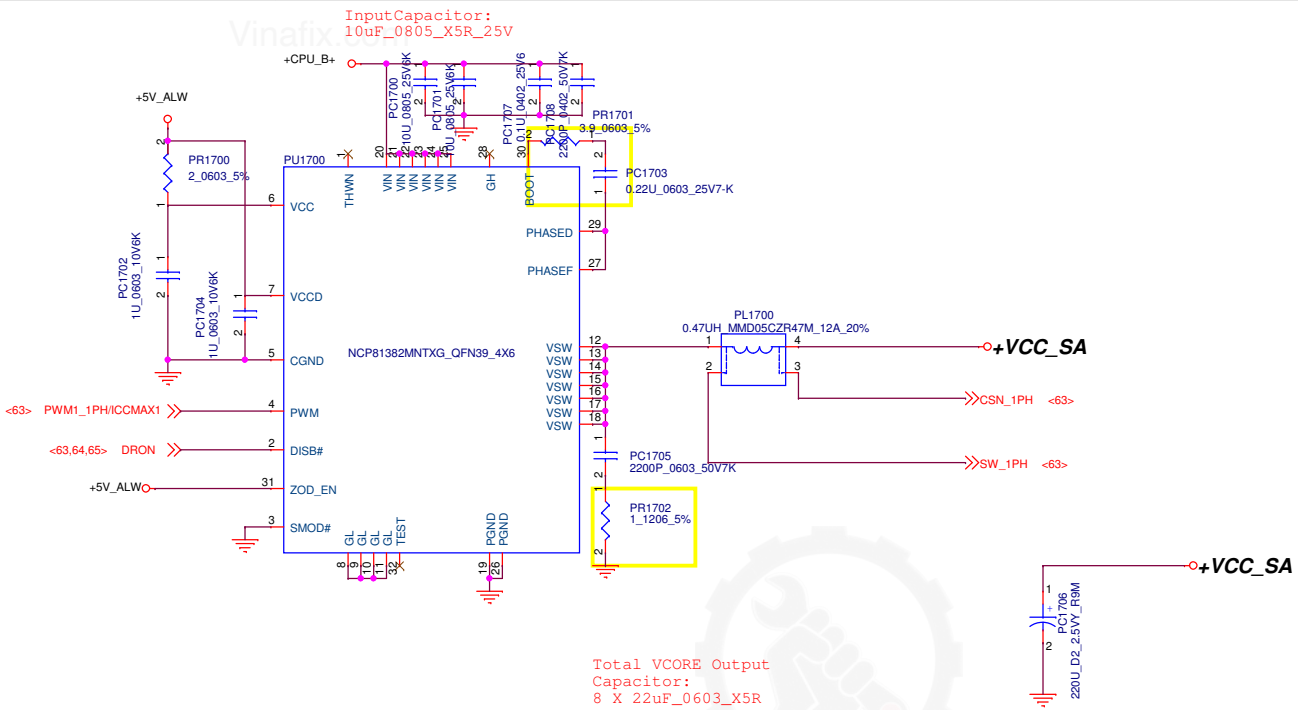

+VCC_SA
TDC 7.77A
Peak Current 11.1 A
OCP Current 13.32 A
Choke Idc: 12.2A / Isat: 16A
DCR 6.2mohm +-5%

Compal Electronics, Inc.		
Title: +VCC_SA		
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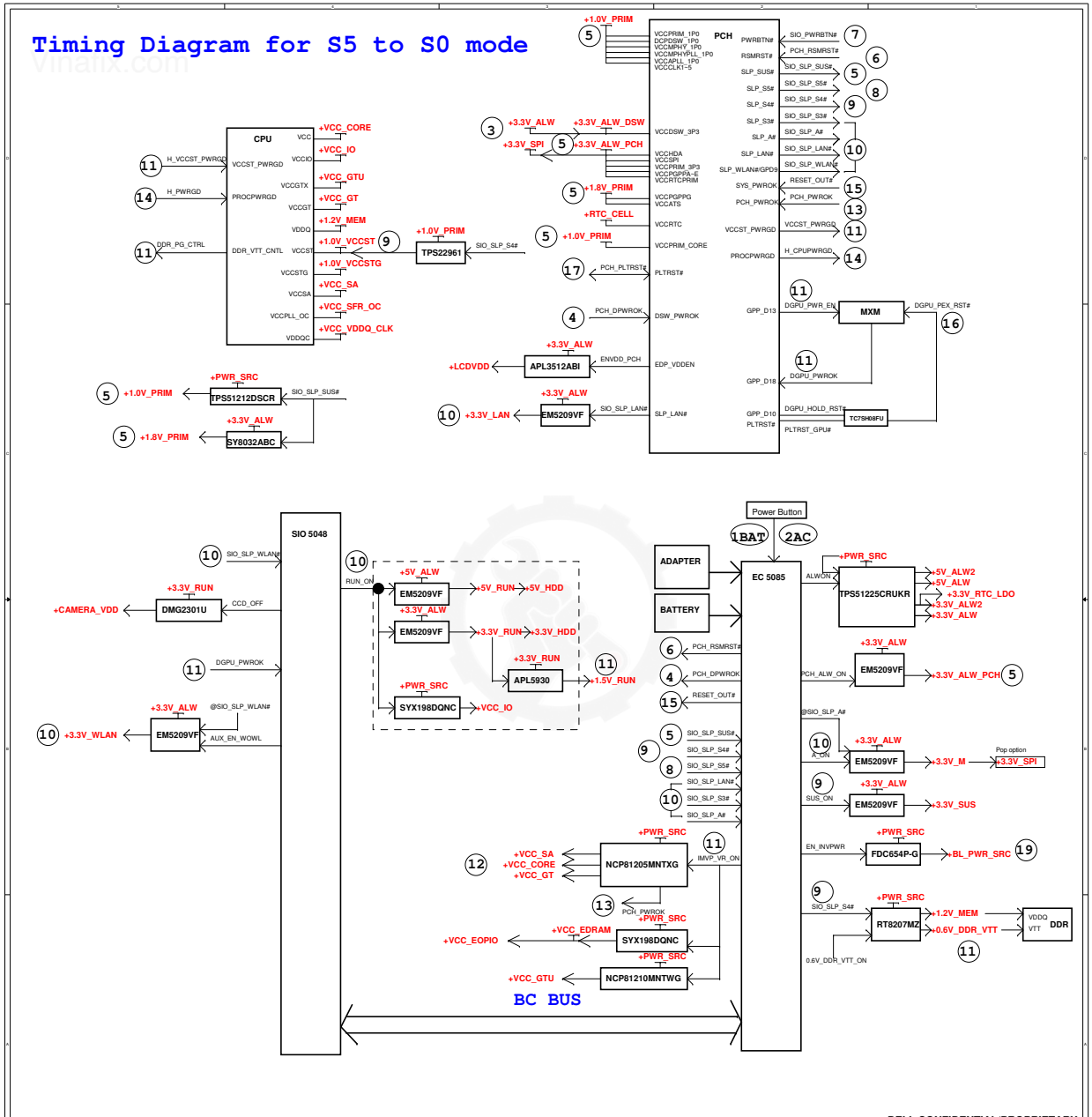
Timing Diagram for S5 to S0 mode



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Compal Electronics, Inc.	
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29	HW	2016/06/01	compal	system can't disply on eDP panel	change CPU_EDP_HPD to U630.3 and MXM_EDP_HPD to U630.13	0.2(X00)
2	39	HW	2016/06/07	compal	system can't detect USH/B	change RZ72 to 0ohm short for load sw power to turn on +3.3V_CV2,+3.3V_FPM(EVT pop)	0.3(X01)
3	33	HW	2016/06/07	compal	mDP can't display	change HD3SS214 operate mode change from stand by mode to normal mode,pop R107,depop R108(EVT pop)	0.3(X01)
4	39	HW	2016/06/07	compal	Reserve for version B TPM IC design	add @RZ124	0.3(X01)
5	14,17	HW	2016/06/07	compal	change 330uF cap placement for 1pcs/1channel	pop CD25,depop CD43	0.3(X01)
6	48	HW	2016/06/07	compal	For press power button over 20 sec,EC can sent RTCRST_ON to reset RTC	add R808,R809,Q371,and connect R808.1,Q371.2 to U51.B8	0.3(X01)
7	38	HW	2016/06/23	compal	change C481 package size from 0603 to 0402	change C481 from SE080105K80 to SE00000QL10	0.3(X01)
8	46	HW	2016/06/28	compal	prevent damage with Miramar I/O board	JIO1 rotate 180 degree.	0.3(X01)
9	19	HW	2016/06/28	compal	TBT_CIO_PLUG_EVENT# pull up change from +3.3V_ALW to +3.3V_ALW_PCH for power leakage	TBT_CIO_PLUG_EVENT# add RH366 pull to +3.3V_ALW_PCH, de-pop RH341	0.3(X01)
10	48	HW	2016/07/01	compal	reserve for DPWROK sequence	add @UE7,@CE5,@CE10,@RE348,change R802 from 0ohm-short to 0ohm and pop it.	0.3(X01)
11	48	HW	2016/07/01	compal	Board ID change to X01	change R875 from 240Kohm to 130Kohm	0.3(X01)
12	39	HW	2016/07/01	compal	TPM leverage X8	change RZ111 from 0ohm-short to 0ohm,depop RZ111,RZ112,RZ82,QZ2,pop RZ124	0.3(X01)
13	39	HW	2016/07/01	compal	USH	change RZ10 from 1M to 100Kohm,depop DZ3,pop RZ76	0.3(X01)
14	40	RF	2016/07/01	compal	leverage X8-reserved 0 ohm on COEX1~3 betweem WWAN and WLAN	add RZ125,RZ126,RZ127	0.3(X01)
15	47	HW	2016/07/04	compal	leverage X8-TBT_RESET_N_EC add R886 PD 100Kohm	add R886	0.3(X01)
16	25	RF	2016/07/05	compal	5.76G noise mitigation	change RH362,RH363 from 0ohm to bead(BLM15GA750SN1) and location change to LH1,LH2	0.3(X01)
17	33	HW	2016/07/07	TI	HD3SS214ZQER SPEC pin define error	change SW5_DP_N1 from U636.E2 to U636.E1, SW5_DP_P1 from U636.E1 to U636.E2	0.3(X01)
18	46	HW	2016/08/22	compal	support RIO USB3.0 wake on WWAN in S3	change JIO1.37 from +3.3V_RUN to +3.3V_ALW	0.4(X02)
19	48	HW	2016/08/22	compal	Board ID change to X02	change R875 from 130Kohm to 33Kohm	0.4(X02)
20	7	HW	2016/08/22	compal	DCI enable on KBL-H	change RC314,RC315 BS from @XDP@ to XDP@	0.4(X02)
21	7	HW	2016/08/24	compal	leverage X8-aviod system always re-boot	change RC316 to 3Kohm and BS from XDP@ to always pop	0.4(X02)
22	47,49	HW	2016/08/24	compal	BITS293066: HDD LED keeps lighting when WWAN Card installed	add Q372 and Q372.2 connect to U46.B1(EC_SLOT2_LED_MASK#),remove T165	0.4(X02)
23	18,21	HW	2016/08/25	compal	add CLK_REQ# isolation for N17P/N17E MXM card	change QH3 to Q6 and connect Q6.1 to CLKREQ_PEG#0,Q6.2 to DGPU_PWROK,Q6.3 to MXM_CLK_REQ#,depop R1978	0.4(X02)
24	48	HW	2016/08/26	compal	SB000008P00 EOL	change Q14,Q15,Q16,Q17,Q26,Q27,Q28 to SB00000Z500	0.4(X02)
25	18,47	HW	2016/08/29	compal	support UMA detect for VGA ID	add @R1973 between UH1.T45 and U46.B59,depop R803,pop R800	0.4(X02)
26	39	HW	2016/08/29	compal	add USH protect circuit for EC	add DZ4,@DZ5,@DZ6,DZ7,@DZ8,RZ128,@RZ129,UZ32,@RZ130,RZ131-RZ134,CZ98-CZ102,LZ1,remove @RZ70,@RZ73,change JUSH1.25 to NC,JUSH1.26 to +VCC_FPM,depop R432	0.4(X02)
27	18	HW	2016/08/30	Nvidia	vender suggest	pop R3750 as default for DGPU_PEX_RST# to avoid EC/PCH electrical timming error	0.4(X02)
28	35	HW	2016/08/30	compal	CRT impendance match to 75ohm on R,G,B	add PD 150ohm (RV128,RV129,RV130) on RED_CONVER, GREEN_CONVER, BLUE_CONVER	0.4(X02)
29	39	HW	2016/08/30	compal	Fix 5085 BGP0 behavior abnormal when surprise power shut down with POA disable	add DZ7 between natname RUN_ON and EC_FPM_EN_D	0.4(X02)
30	45	HW	2016/09/01	compal	add Docking protect circuit for EC	add D101,@R210	0.4(X02)
31	**38**	**HW**	**2016/09/05**	**compal**	**EMI EA**	**change C485 from 150pF to 10pF**	**0.4(X02)**
32	**11,12**	**HW**	**2016/09/08**	**compal**	**reduce ripple of +1.0V_VCCST,+1.0V_VCCSTG, +1.0V_PRIMP**	**change CZ82, CZ88, CC195,CC186,CZ63,CZ90 to 10uf_0402**	**0.4(X02)**
33	**39**	**HW**	**2016/09/08**	**compal**	**leverage X8-change TPM MPN to NPCT650VB2YX**	**change U637 from SA00008EL70 to SA00008EL80**	**0.4(X02)**
34	**39**	**HW**	**2016/09/08**	**compal**	**remove reserve component on USH**	**remove DZ3,change RZ76 to 0ohm_short**	**0.4(X02)**
35	**50**	**HW**	**2016/09/12**	**compal**	**leverage X8-change TP I2C PU R**	**change RZ114,RZ115 from 4.7Kohm to 2.2Kohm**	**0.4(X02)**
36	**12,19**	**HW**	**2016/09/12**	**INTEL**	**PDG1.0**	**change RH73 from 43ohm to 13ohm,CC187,CC188,C189,CC272 from 22uF to 10uF,depop CC272**	**0.4(X02)**
37	**48**	**HW**	**2016/09/19**	**compal**	**BITS297377 <Crane 15" DVT1> OTP (Q15)can not meet spec 93+/-3C**	**pop C273**	**0.4(X02)**
38	**37**	**HW**	**2016/09/19**	**compal**	**LAN chip change to production PN**	**change U31 from SA000081G1L to SA000081G3L**	**0.4(X02)**
39	**33**	**HW**	**2016/11/09**	**compal**	**AMD MXM CARD,display icon SHOW 3 Display when plug 1 monitor**	**Add R153,R154 PD on MXM_DPB_HPD,PCH_DPD_HPD**	**1.0(A00)**
40	**48**	**HW**	**2016/11/23**	**compal**	**Board ID change to A00**	**change R875 from 33Kohm to 4.3Kohm**	**1.0(A00)**
41	**46**	**HW**	**2016/11/10**	**compal**	**advance BTB connector connection**	**change JIO1 from QT50A01-29100-7H to QT50A01-29200-7H,JIO2 from QT50A61-29100-7H to QT50A61-29200-7H**	**1.0(A00)**
42	**18**	**HW**	**2016/11/11**	**compal**	**reserve for NV request**	**Add @R155 between U17.1 and U17.2,add R156 between U17.1 and ACAV_IN**	**1.0(A00)**
43	**44**	**HW**	**2016/11/18**	**compal**	**PCIE IEMT EA-channel A/B de-emphasis level= -6dB/-2dB**	**pop RN50,RN102,RN61,RN119**	**1.0(A00)**
44	**37,20**	**HW**	**2016/11/21**	**compal**	**change UH1,U31 to MP part number**	**change UH1 to SA0000ACM2L,U31 to SA000081G1L**	**1.0(A00)**

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	52 57	POWER	4/29	COMPAL	change PBAT_SMBCLK,CHARGER_SMBCLK PBAT_SMBDAT,CHARGER_SMBDAT net name for HW request	PBAT_SMBCLK,CHARGER_SMBCLK change to CHARGER_PBAT_SMBCLK; PBAT_SMBDAT,CHARGER_SMBDAT change to CHARGER_PBAT_SMBDAT	Rev.01
2	52	POWER	5/4	COMPAL	for EMC request , pop and change PC15 from 0.1U to 1000P	change PC15 from 0.1U(SE042104K80) to 1000P(SE074102K80)	Rev.01
3	53 57	POWER	5/4	COMPAL	for EMI request, nreed to depop PL100 and PL700	co-layout a jump on PL100 and PL700	Rev.01
4	53 56	POWER	5/12	COMPAL	for DDR4 2400 current request, change output choke to support	1.PL101 change from SH00000YV00 (S COIL 2.2UH +-20% 7.8A 7X7X3 MOLDING) to SH000016700(S COIL 1.5UH +-20% 9A 7X7X3 MOLDING) 2.PL400 change from SH00000YG00(S COIL 1UH +-30% 2.8A 4X4X2 FERRITE) to SH00000IW00 (S COIL 1UH +-20% PCMB042T-1R0MS 4.5A)	Rev.01
5	54	POWER	7/1	COMPAL	for RAM issue , HW request to change from 1.2V to 1.235V	change PR204 from 12K(SD034120280) to 13K(SD034130280)	Rev.03
6	64 65 67	POWER	7/1	COMPAL	For FAE check,pop Dr.MOS EMC part and change bootstrap resister to reduce the ringing of SW node	change PR1201 PR1202 PR1208 PR1401 PR1402 PR1701 from SD013200B80 (S RES 1/10W 2 +-5% 0603) to SD00000YH00 (S RES 1/10W 3.9 +-5% 0603)	Rev.03
7	64 65 67	POWER	7/11	COMPAL	For FAE check, change snubber resister to reduce the ringing of SW node	change PR1206 PR1207 PR12011 PR1406 PR1407 PR1702 from SD001200B80 (S RES 1/4W 2 +-5% 1206) to SD011100B80 (S RES 1/4W 1 +-5% 1206)	Rev.03
8	59	POWER	7/22	COMPAL	For Temp voltage test , +DC_IN setting for ACAVIN_NB need less than 17.55V , so change PR737 to achieve	change PR737 from SD034665380(S RES 1/16W 665K +-1% 0402) to SD034634380(S RES 1/16W 634K +-1% 0402)	Rev.03
9	53	POWER	9/2	COMPAL	With compal rule , need to use even part to back to back for acoustic noise improvement so add 3.3V/5V input MLCC to achieve	change PC101,PC102 from SE00000QK00(S CER CAP 10U 25V K X5R 0805 H1.25) to SE000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25) and add PC121,PC122 SE000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25)	Rev.04

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
10	63	POWER	9/2	COMPAL	Change SW to controller resisters size from 0402 to 0603 to improve initial voltage for FAE suggest	change PR1143,PR1146,PR1148 from 82.5K 0402(SD000002780) to 82.5K 0603(SD014825280) and PR1145,PR1147 from 56.2K 0402(SD000001580) to 56.2K 0603(SD014562280)	Rev.04
11	60 63	POWER	9/2	COMPAL	To improve HW side +1.0V_VCCST ,+1.0V_VCCSTG and +1.0V_VCCSFR output ripple , change 1.0V_PRIM choke and VCCST MLCC	Change PL800 from SH00000Z200 (S COIL 1UH +-20% 6.6A 5X5X3 MOLDING) to SH00000R810 (S COIL 2.2UH +-20% PCMB053T-2R2MS 5.5A) and PC1101 from SE00000G880 (S CER CAP 0.1U 25V K X5R 0402) to SE00000UD00 (S CER CAP 10U 6.3V M X5R 0402)	Rev.04
12	63	POWER	9/12	COMPAL	For SA Loadline and Iout improvement , modify parameter of VR ciruit from FAE suggestion	Pop PC1140 and change from 1000P(SE074102K80) to 2200P(SE074222K80); change PR1107 from short pad to 1K(SD028100180); change PR1109 from 1.43K(SD034143180) to 1.58K(SD00000SJ80); change PR1112 from 30K(SD034300280) to 28K(SD034280280)	Rev.04
13	63	POWER	9/14	COMPAL	For IA,GT Loadline and Iout improvement , modify parameter of VR ciruit from FAE suggestion	IA part Change PR1143,PR1146,PR1148 from 82.5K(SD014825280) to 88.7K(SD014887280); change PR1132 from 24.3K to 26.7K(SD034267280); GT part Change PR1145,PR1147 from 56.2K(SD014562280) to 61.9K(SD014619280); change PR1135 from 22.6K to 24.9K(SD034249280)	Rev.04
14	53 59 60	POWER	9/20	COMPAL	For Dell request , 3.3V/5V HS and LS MOS should be used with the same vendor	High side MOS Change PQ100,PQ101,PQ800 from SB000001A00 S TR SIS412DN-T1-GE3 1N POWERPAK1212-8 to SB00000H800 S TR AON7408L 1N DFN; Low side MOS Change PQ102,PQ103,PQ705 from SB00000N800 S TR FDMC7692S 1N MLP to SB000010U00 S TR AON7752 1N DFN3X3EP	Rev.04
15	53	POWER	9/26	COMPAL	For HW request , need to increase 5V output voltage from 5V to 5.08V to reduce PD output voltage drop	Change PR101 from SD034150280 (S RES 1/16W 15K +-1% 0402) to SD034154280 (S RES 1/16W 15.4K +-1% 0402)	Rev.04
16	63	POWER	9/26	COMPAL	To meet intel SPEC for GT voltage , need to modify parameter of VR circuit	Change PR1127 from SD034100180 (S RES 1/16W 1K +-1% 0402) to SD034137180 (S RES 1/16W 1.37K +-1% 0402)	Rev.04
17	53	POWER	11/11	COMPAL	For type C test , change FB resisters to rise output voltage from 5V to 5.156V	Change PR101 from SD034158280(S RES 1/16W 15.8K +-1% 0402) to SD034154280(S RES 1/16W 15.4K +-1% 0402) change PR104 from SD028102280(S RES 1/16W 10.2K +-1% 0402) to SD034976180(S RES 1/16W 9.76K +-1% 0402)	Rev.10
18	54	POWER	11/11	COMPAL	For 1.2V damage issue , upgrade high side MOS to improve	Change PQ201 from SB00000K300(S TR SIR472DP-T1-GE3 1N POWERPAK SO8) to SB00000WY00(S TR SIRA14DP-T1-GE3 1N POWERPAK SO8)	Rev.10
19	54	POWER	11/16	COMPAL	For 1.2V damage issue , change HS/LS MOS from Vishay to Magnachop and 1.235V change back to 1.2V	Change PQ201 from SB00000WY00(S TR SIRA14DP-T1-GE3 1N POWERPAK SO8)to SB00001GP00(S TR AON6380 1N DFN5X6-8): change PQ202 from SB00000WX00(S TR SIRA06DP-T1-GE3 1N POWERPAKSO-8) to SB00001GK00(S TR AON6314 1N DFN5X6-8) change PR204 from SD034130280(S RES 1/16W 13K +-1% 0402) to SD034120280S RES 1/16W 12K +-1% 0402)	Rev.10