PCB Number: 14058-2
ECO# number : 776481

BOM Configuration
(R):Unmount
(G):GPU
(U):UMA
(X):Debug used
(T):Touch

PAGE	TITLE	Quantity
01	Cover Page	
02	Block Diagram	
03	CPU_DDRA_DDRB	
04	CPU_CFG/CLOCK	
05	CPU_PCIE	
06	CPU_ (VSS)	
07	CPU_(VCC_CORE/TP)	
08	CPU_(DDI/EDP)	
09	CPU_(POWER CAP1)	
10	CPU_(POWER CAP2)	
11	Reserved	
12	DDR3_SODIMM1	
13	DDR3_SODIMM2	
14	Reserved	
15	PCH(SPI/SMBUS/Audio/JTAG)	
16	PCH_(Clock)	
17	PCH (PCIE/SATA/USB)	
18	PCH (USB3.0/GPIO/HPD)	
19	PCH (GPIO)	
20	PCH_(Stap Pin)	
21	PCH_(Power)	
22	PCH_(Vss/TP)	
23	PCH_(Reserved)	
24	SIO_ITE8739	
25	Flash ROM/RTC	
26	FAN CIRCUITS/HOLE	
27	AUDIO ALC3661	
28	AMP TPA3131	
29	MIC/SPEAKER/AUDIO JACK	
30	Reserved	
31	LAN_RTL8111HSD	
32	RJ45+TRANSFORMER	
33	READER CONN	
34	USB2.0 CONN	
35	USB3.0 CONN	
36	Reserved	
37	Reserved	
38	WEBCAM	
39	Reserved	
40	Power enable & sequence	
41	DCIN	
42	Run PWR/USB/ DSWPWR	
43	CHARGER	
44	VCORE & V_GT(NCP81203)	
45	VCORE OUTPUT (NCP81151)	
46	V_GT OUTPUT(NCP81151)	
47	VCCSA(RT8237)	
48	VCCIO(RT8237)	
49	5V & 3.3V(RT8243A)	
50	DDR_PWR (RT8207M)	
51	PCH_1D0V(RT8237)	
52	1D8V(RT9025)	
53	12V(RT8289)	
54	Reserved	
55	Scalar	
56	HDMI OUT	
57	HDMI IN	
58	PANEL CONTROL	

PAGE	TITLE	Quantity
59	OZ554A LED Converter	
60	HDD/ODD	
61	NGFF CONN	
62	TOUCH	
63	Reserved	
64	LED BOARD/POWER BUTTON	
65	Reserved	
66	Reserved	
67	FFS	
68	DEBUG CONNECTOR	
69	Reserved	
70	Reserved	
71	Reserved	
72	Reserved	
73	Reserved	
74	Reserved	
75	Reserved	
76	GPU(1/5) PEG	
77	GPU(2/5)DIGITALOUT	
78	GPU(3/5):VRAM I/F	
79	GPU(4/5):GPIO/STRAP	
80	080_GPU(5/5):PWR/GND	
81	VRAM 1,2(1/2)	
82	VRAM 3,4(2/2)	
83	VRAM5,6(3/4)	
84	VRAM7,8(4/4)	
85	Reserved	
86	PWR_GPU_LDO	
87	Reserved	
88	PWR_GPU_CORE	
89	Reserved	
90	Reserved	
91	Reserved	
92	Reserved	
93	Reserved	
94	Reserved	
95	Reserved	
96	Reserved	
97	Reserved	
98	Reserved	
99	CPU_XDP	
100	Reserved	
101	Reserved	
102	POWER Sequence	
103	POWER BLOCK DIAGRAM	
104	POWER GOOD & RESET DIAGRAM	
105	CLOCK DIAGRAM	

<Variant Name>

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Title: 001_Cover Page

Size | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 1 of 107

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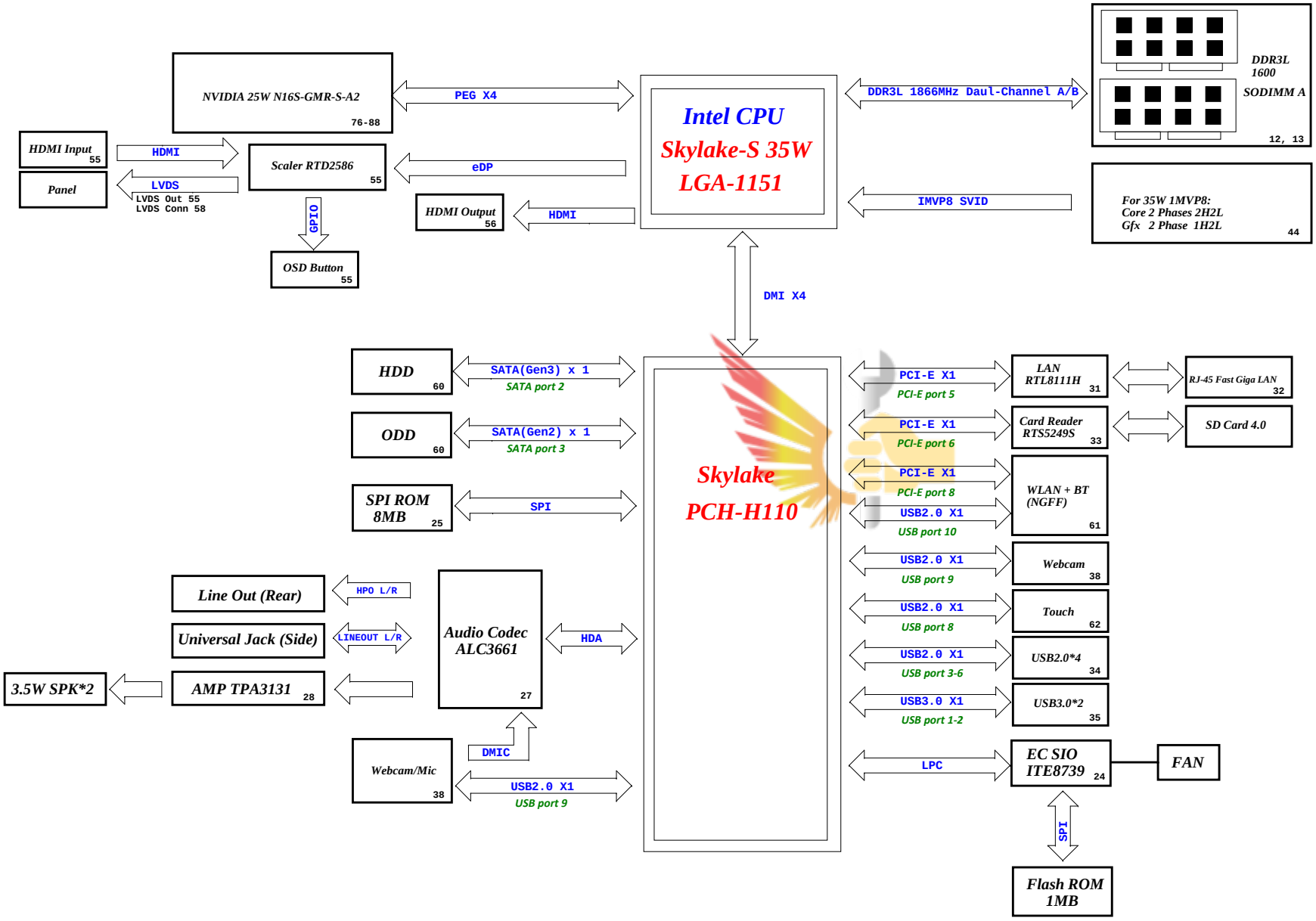
Project code:3PD025010001
ECO# Number: 776481
PCB Number: 14058
Revision:A01

COLORADO MLK Skylake-S Block Diagram



CHARGER	
BQ24727RGRR-1-GP	43
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC	
RT8243AZQW-GP	49
INPUTS	OUTPUTS
DCBATOUT	V_3P3_A V_5P0_A

CPU Core Power	
NCP81203MNTXG-SI2-GP	44,45
INPUTS	OUTPUTS
DCBATOUT	V_CPU_CORE

GFX Core Power	
NCP81172MNTXG-GP-U	88
INPUTS	OUTPUTS
DCBATOUT	+V_GPU_CORE

DDR3L SUS	
TPS51716RUKR-GP	50
INPUTS	OUTPUTS
DCBATOUT	V_SM V_SM_VTT

CPU GT POWER	
NCP81203MNTXG-SI2-GP	44,46
INPUTS	OUTPUTS
DCBATOUT	V_CPU_GT

CPU 1.05V	
NCP5230MNTWG	47
INPUTS	OUTPUTS
DCBATOUT	V_CPU_SA

CPU 0.95V	
RT8237CZQW-2-GP	48
INPUTS	OUTPUTS
DCBATOUT	V_CPU_IO

PCH 1.0V	
S-1339D15-M5001-GP	51
INPUTS	OUTPUTS
DCBATOUT	V1P0_PCH_S5

FAN 12V	
RT8289GSP-GP	53
INPUTS	OUTPUTS
DCBATOUT	12V_S0

GPU 1.35V	
APW8713QBI-GP	86
INPUTS	OUTPUTS
DCBATOUT	+V_1P35_VGA

System switchs	
INPUTS	OUTPUTS
V_5P0_A	SB5V
V_3P3_A	SB3V
V_5P0_A	VCC
V_3P3_A	VCC3
V_SM	+V_1P05_VGA

PCB LAYER

L1:Top
L2:GND
L3:Signal
L4:Signal
L5:GND
L6:Bottom

<Variant Name>

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Title: 002_Block Diagram

Size	Document Number	Rev
Custom	COLORADO MLK SKYLAKE-S	-2
Date:	Sheet 2 of 107	

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DDR DATA

12 M_DATA_A[0..63]
13 M_DATA_B[0..63]

12 M_DQS_A_DP[0..7]
12 M_DQS_A_DN[0..7]

13 M_DQS_B_DP[0..7]
13 M_DQS_B_DN[0..7]

DDR CMD/ADD

12 M_MAA_A[0..15]
13 M_MAA_B[0..15]

12 M_WE_A_N
12 M_CAS_A_N
12 M_RAS_A_N
12 M_SBS_A0
12 M_SBS_A1
12 M_SBS_A2

13 M_WE_B_N
13 M_CAS_B_N
13 M_RAS_B_N
13 M_SBS_B0
13 M_SBS_B1
13 M_SBS_B2

DDR CTRL

12 M_SCS_A_N0
12 M_SCS_A_N1

12 M_SCKE_A0
12 M_SCKE_A1

12 M_ODT_A0
12 M_ODT_A1

13 M_SCS_B_N0
13 M_SCS_B_N1

13 M_SCKE_B0
13 M_SCKE_B1

13 M_ODT_B0
13 M_ODT_B1

DDR CLOCK

12 CK_M_DDR0_A_DP
12 CK_M_DDR0_A_DN
12 CK_M_DDR1_A_DP
12 CK_M_DDR1_A_DN

13 CK_M_DDR0_B_DP
13 CK_M_DDR0_B_DN
13 CK_M_DDR1_B_DP
13 CK_M_DDR1_B_DN

DDR OTHERS

12 DIMM_DQ_CPU_VREF_A
13 DIMM_DQ_CPU_VREF_B
12 DIMM_CA_VREF_A
13 DIMM_CA_VREF_B

06/24 Allen modify

CPU1A — 1 OF 12 — SKYLAKE — LGA1151

M_DATA_A5 AE38 … M_DATA_A63 AG37
DDR0_DQ0 … DDR0_DQ63
M_DATA_B0 AD34 … M_DATA_B63 AF33
DDR1_DQ0 … DDR1_DQ63

DDR0_CKP0 AW18 CK_M_DDR0_A_DP
DDR0_CKN0 AV18 CK_M_DDR0_A_DN
DDR0_CKP1 AW17 CK_M_DDR1_A_DP
DDR0_CKN1 AV17
DDR0_CKP2 AW16
DDR0_CKN2 AV16
DDR0_CKP3 AT16
DDR0_CKN3 AU16

DDR1_CKP0 AM26 CK_M_DDR0_B_DP
DDR1_CKN0 AM25 CK_M_DDR0_B_DN
DDR1_CKP1 AP27 CK_M_DDR1_B_DP
DDR1_CKN1 AP26 CK_M_DDR1_B_DN
DDR1_CKP2 AN26
DDR1_CKN2 AN25
DDR1_CKP3 AP25
DDR1_CKN3 AP24

DDR0_CKE0 AY24 M_SCKE_A0
DDR0_CKE1 AW24 M_SCKE_A1
DDR0_CKE2 AV24
DDR0_CKE3 AV25

DDR1_CKE0 AY29 M_SCKE_B0
DDR1_CKE1 AV29 M_SCKE_B1
DDR1_CKE2 AW28
DDR1_CKE3 AU28

DDR0_CS#0 AW12 M_SCS_A_N0
DDR0_CS#1 AU11 M_SCS_A_N1
DDR0_CS#2 AV12
DDR0_CS#3 AV10

DDR1_CS#0 AP17 M_SCS_B_N0
DDR1_CS#1 AN17 M_SCS_B_N1
DDR1_CS#2 AN15
DDR1_CS#3 AM15

DDR0_ODT0 AU14 M_ODT_A0
DDR0_ODT1 AU13 M_ODT_A1
DDR0_ODT2 AU10
DDR0_ODT3 AT10

DDR1_ODT0 AM16 M_ODT_B0
DDR1_ODT1 AL15 M_ODT_B1
DDR1_ODT2 AP15
DDR1_ODT3 AL16

DDR0_BA0/DDR0_CAB4/DDR0_BA0 AV13 M_SBS_A0
DDR0_BA1/DDR0_CAB5/DDR0_BA1 AV15 M_SBS_A1
DDR0_BA2/DDR0_CAA5/DDR0_BG0 AW13 M_SBS_A2

DDR1_BA0/DDR1_CAB4/DDR1_BA0 AN19 M_SBS_B0
DDR1_BA1/DDR1_CAB5/DDR1_BA1 AM18 M_SBS_B1
DDR1_BA2/DDR1_CAA5/DDR1_BG0 AW28 M_SBS_B2

DDR0_RAS#/DDR0_CAB3/DDR0_MA16 AV14 M_WE_A_N
DDR0_WE#/DDR0_CAB2/DDR0_MA14 AV11 M_CAS_A_N
DDR0_CAS#/DDR0_CAB1/DDR0_MA15 AW15 M_RAS_A_N

DDR1_RAS#/DDR1_CAB3/DDR1_MA16 AL17 M_WE_B_N
DDR1_WE#/DDR1_CAB2/DDR1_MA14 AP18 M_CAS_B_N
DDR1_CAS#/DDR1_CAB1/DDR1_MA15 AL18 M_RAS_B_N

DDR0_MA0/DDR0_CAB9/DDR0_MA0 AU18 M_MAA_A0
DDR0_MA1/DDR0_CAB8/DDR0_MA1 AU17 M_MAA_A1
DDR0_MA2/DDR0_CAB7/DDR0_MA2 AV16 M_MAA_A2
DDR0_MA3 AT19 M_MAA_A3
DDR0_MA4 AU20 M_MAA_A4
DDR0_MA5/DDR0_CAA9/DDR0_MA5 AV20 M_MAA_A5
DDR0_MA6/DDR0_CAA2/DDR0_MA6 AU21 M_MAA_A6
DDR0_MA7/DDR0_CAA4/DDR0_MA7 AT20 M_MAA_A7
DDR0_MA8/DDR0_CAA3/DDR0_MA8 AT22 M_MAA_A8
DDR0_MA9/DDR0_CAA1/DDR0_MA9 AV19 M_MAA_A9
DDR0_MA10/DDR0_CAB7/DDR0_MA10 AU22 M_MAA_A10
DDR0_MA11/DDR0_CAA7/DDR0_MA11 AV22 M_MAA_A11
DDR0_MA12/DDR0_CAA6/DDR0_MA12 AV17 M_MAA_A12
DDR0_MA13/DDR0_CAB6/DDR0_MA13 AV23 M_MAA_A13
DDR0_MA14/DDR0_CAA8/DDR0_BG1 AU24 M_MAA_A14
DDR0_MA15/DDR0_CAA9/DDR0_ACT# AP22 M_MAA_A15

DDR1_MA0/DDR1_CAB9/DDR1_MA0 AL20 M_MAA_B0
DDR1_MA1/DDR1_CAB8/DDR1_MA1 AL22 M_MAA_B1
DDR1_MA2/DDR1_CAB7/DDR1_MA2 AM23 M_MAA_B2
DDR1_MA3 AP23 M_MAA_B3
DDR1_MA4 AL24 M_MAA_B4
DDR1_MA5/DDR1_CAA9/DDR1_MA5 AW24 M_MAA_B5
DDR1_MA6/DDR1_CAA2/DDR1_MA6 AY26 M_MAA_B6
DDR1_MA7/DDR1_CAA4/DDR1_MA7 AU26 M_MAA_B7
DDR1_MA8/DDR1_CAA3/DDR1_MA8 AW27 M_MAA_B8
DDR1_MA9/DDR1_CAA1/DDR1_MA9 AP19 M_MAA_B9
DDR1_MA10/DDR1_CAB7/DDR1_MA10 AU27 M_MAA_B10
DDR1_MA11/DDR1_CAA7/DDR1_MA11 AV27 M_MAA_B11
DDR1_MA12/DDR1_CAA6/DDR1_MA12 AR15 M_MAA_B12
DDR1_MA13/DDR1_CAB6/DDR1_MA13 AY28 M_MAA_B13
DDR1_MA14/DDR1_CAA8/DDR1_BG1 AU28 M_MAA_B14
DDR1_MA15/DDR1_CAA9/DDR1_ACT# AL20 M_MAA_B15

DDR0_PAR AY15 TP_DDR0_PAR
DDR0_ALERT# AT23 DDR0_ALERT#
R1 49D402-PAD
TP1 TPAD28

DDR1_PAR AY20 TP_DDR1_PAR
DDR1_ALERT# AY21 DDR1_ALERT#
R2 49D402-PAD
TP2 TPAD28

NOTE CMD SIGNALS FOR DIFFERENT MEMORY TECHINOLOGIES:
LEFT TO RIGHT: DDR3L/LPDDR3/DDR4

THIS IS FOR RVP10 ONLY
Short PAD ,if Layout placement inpact

06/24 Allen modify

Can be left as no connects if no support ECC.

DDR0_DQSN0/DDR0_DQSN0 AK39 M_DQS_A_DN0
DDR0_DQSN1/DDR0_DQSN1 AP39 M_DQS_A_DN1
DDR0_DQSN2/DDR0_DQSN4 AU36 M_DQS_A_DN2
DDR0_DQSN3/DDR0_DQSN5 AW7 M_DQS_A_DN3
DDR0_DQSN4/DDR1_DQSN0 AU3 M_DQS_A_DN4
DDR0_DQSN5/DDR1_DQSN1 AN3 M_DQS_A_DN5
DDR0_DQSN6/DDR1_DQSN4 AJ3 M_DQS_A_DN6
DDR0_DQSN7/DDR1_DQSN5 M_DQS_A_DN7

DDR0_DQSP0/DDR0_DQSP2 AK38 M_DQS_A_DP0
DDR0_DQSP1/DDR0_DQSP3 AP38 M_DQS_A_DP1
DDR0_DQSP2/DDR0_DQSP4 AV36 M_DQS_A_DP2
DDR0_DQSP3/DDR0_DQSP5 AV7 M_DQS_A_DP3
DDR0_DQSP4/DDR1_DQSP0 AU2 M_DQS_A_DP4
DDR0_DQSP5/DDR1_DQSP1 AN2 M_DQS_A_DP5
DDR0_DQSP6/DDR1_DQSP4 AJ2 M_DQS_A_DP6
DDR0_DQSP7/DDR1_DQSP5 M_DQS_A_DP7

DDR0_DQSP8 AV32 TP_DDR0_DQSP8
DDR0_DQSN8 AU32 TP_DDR0_DQSN8
TP3 TPAD28
TP4 TPAD28

DDR0_ECC0 AT33
DDR0_ECC1 AW33
DDR0_ECC2 AU31
DDR0_ECC3 AU33
DDR0_ECC4 AY31
DDR0_ECC5 AW31
DDR0_ECC6 AY33
DDR0_ECC7 A

DDR CHANNEL A

SKYLAKE-1

All types of DIMMs are DDR3L

CPU1B — 2 OF 12 — SKYLAKE — LGA1151

DDR1_DQ0/DDR0_DQ16 … DDR1_DQ63/DDR0_DQ63

DDR1_CKP0 AM26 CK_M_DDR0_B_DP
DDR1_CKN0 AM25 CK_M_DDR0_B_DN
DDR1_CKP1 AP27 CK_M_DDR1_B_DP
DDR1_CKN1 AP26 CK_M_DDR1_B_DN
DDR1_CKP2 AN26
DDR1_CKN2 AN25
DDR1_CKP3 AP25
DDR1_CKN3 AP24

DDR1_CKE0 AY29 M_SCKE_B0
DDR1_CKE1 AV29 M_SCKE_B1
DDR1_CKE2 AW28
DDR1_CKE3 AU28

DDR1_CS#0 AP17 M_SCS_B_N0
DDR1_CS#1 AN17 M_SCS_B_N1
DDR1_CS#2 AN15
DDR1_CS#3 AM15

DDR1_ODT0 AM16 M_ODT_B0
DDR1_ODT1 AL15 M_ODT_B1
DDR1_ODT2 AP15
DDR1_ODT3 AL16

DDR1_RAS#/DDR1_CAB3/DDR1_MA16 AL17 M_WE_B_N
DDR1_WE#/DDR1_CAB2/DDR1_MA14 AP18 M_CAS_B_N
DDR1_CAS#/DDR1_CAB1/DDR1_MA15 AL18 M_RAS_B_N

DDR1_BA0/DDR1_CAB4/DDR1_BA0 AN19 M_SBS_B0
DDR1_BA1/DDR1_CAB5/DDR1_BA1 AM18 M_SBS_B1
DDR1_BA2/DDR1_CAA5/DDR1_BG0 AW28 M_SBS_B2

DDR1_MA0/DDR1_CAB9/DDR1_MA0 AL20 M_MAA_B0
DDR1_MA1/DDR1_CAB8/DDR1_MA1 AL22 M_MAA_B1
DDR1_MA2/DDR1_CAB7/DDR1_MA2 AM23 M_MAA_B2
DDR1_MA3 AP23 M_MAA_B3
DDR1_MA4 AL24 M_MAA_B4
DDR1_MA5/DDR1_CAA9/DDR1_MA5 AW24 M_MAA_B5
DDR1_MA6/DDR1_CAA2/DDR1_MA6 AY26 M_MAA_B6
DDR1_MA7/DDR1_CAA4/DDR1_MA7 AU26 M_MAA_B7
DDR1_MA8/DDR1_CAA3/DDR1_MA8 AW27 M_MAA_B8
DDR1_MA9/DDR1_CAA1/DDR1_MA9 AP19 M_MAA_B9
DDR1_MA10/DDR1_CAB7/DDR1_MA10 AU27 M_MAA_B10
DDR1_MA11/DDR1_CAA7/DDR1_MA11 AV27 M_MAA_B11
DDR1_MA12/DDR1_CAA6/DDR1_MA12 AR15 M_MAA_B12
DDR1_MA13/DDR1_CAB6/DDR1_MA13 AY28 M_MAA_B13
DDR1_MA14/DDR1_CAA8/DDR1_BG1 AU28 M_MAA_B14
DDR1_MA15/DDR1_CAA9/DDR1_ACT# AL20 M_MAA_B15

DDR1_PAR AY20 TP_DDR1_PAR
DDR1_ALERT# AY21 DDR1_ALERT#
R2 49D402-PAD
TP2 TPAD28

NOTE CMD SIGNALS FOR DIFFERENT MEMORY TECHINOLOGIES:
LEFT TO RIGHT: DDR3L/LPDDR3/DDR4

THIS IS FOR RVP10 ONLY
Short PAD ,if Layout placement inpact

06/24 Allen modify

Can be left as no connects if no support ECC.

DDR1_DQSN0/DDR0_DQSN2 AF34 M_DQS_B_DN0
DDR1_DQSN1/DDR0_DQSN3 AN33 M_DQS_B_DN1
DDR1_DQSN2/DDR1_DQSN6 AN29 M_DQS_B_DN2
DDR1_DQSN3/DDR0_DQSN7 AN31 M_DQS_B_DN3
DDR1_DQSN4/DDR1_DQSN2 AR31 M_DQS_B_DN4
DDR1_DQSN5/DDR1_DQSN3 AM31 M_DQS_B_DN5
DDR1_DQSN6/DDR1_DQSN6 AD31 M_DQS_B_DN6
DDR1_DQSN7 AD29 M_DQS_B_DN7

DDR1_DQSP0/DDR0_DQSP2 AF35 M_DQS_B_DP0
DDR1_DQSP1/DDR0_DQSP3 AL33 M_DQS_B_DP1
DDR1_DQSP2/DDR0_DQSP4 AP33 M_DQS_B_DP2
DDR1_DQSP3/DDR0_DQSP5 AN28 M_DQS_B_DP3
DDR1_DQSP4/DDR1_DQSP2 AN27 M_DQS_B_DP4
DDR1_DQSP5/DDR1_DQSP3 AP31 M_DQS_B_DP5
DDR1_DQSP6 AL31 M_DQS_B_DP6
DDR1_DQSP7 AG31 M_DQS_B_DP7

DDR1_DQSP8 AN25 TP_DDR1_DQSP8
DDR1_DQSN8 AN24 TP_DDR1_DQSN8
TP5 TPAD28
TP6 TPAD28

DDR1_ECC0 AP29
DDR1_ECC1 AM29
DDR1_ECC2 AP30
DDR1_ECC3 AN30
DDR1_ECC4 AP28
DDR1_ECC5 AL29
DDR1_ECC6 AL30
DDR1_ECC7

DDR CHANNEL B

SKYLAKE-1

DDR_VREF_CA AB40 DIMM_CA_CPU_VREF_A
DDR0_VREF_DQ AC40 DIMM_DQ_CPU_VREF_A
DDR1_VREF_DQ AC39 DIMM_DQ_CPU_VREF_B

C2 SCD1U16V2KX-3DLGP
C1 SCD1U16V2KX-3DLGP

DIMM_CA_CPU_VREF_A
C3 SCD022U16V2KX-3DLGP
DIMM_CA_CPU_VREF_RC
R5 240/8R2F-L-GP
R3 2R2F-GP
R4 2R2F-GP
DIMM_CA_VREF_A
DIMM_CA_VREF_B

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 003_CPU_DDRA_DDR8

Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

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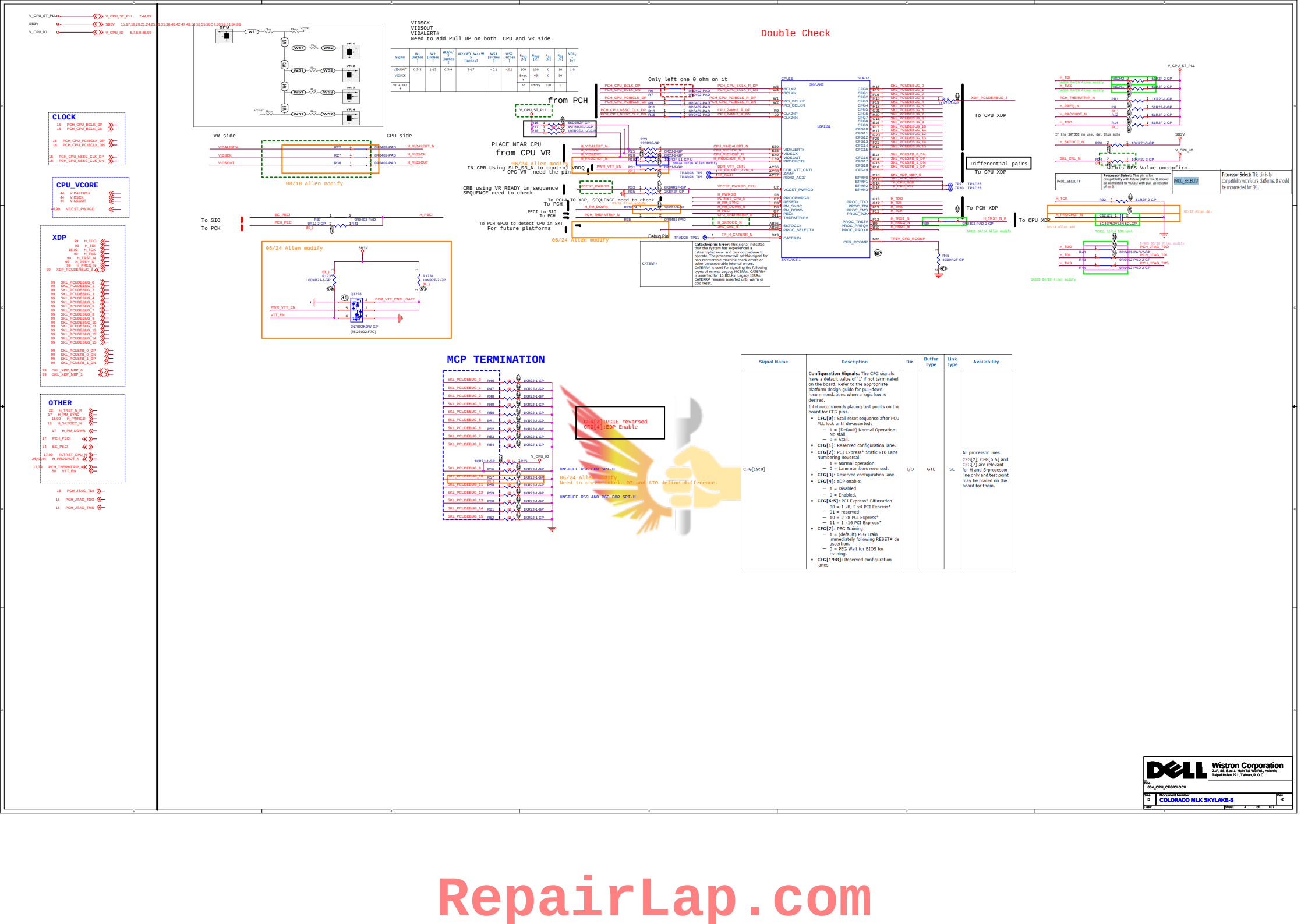

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	WS1 [inches]	WS2 [inches]	R_{SU} [Ω]	R_{SD} [Ω]	R_{SI} [Ω]	R_{SO} [Ω]	VCC_S [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: – 1 = (Default) Normal Operation; No stall. – 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: – 1 = Disabled. – 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

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V_CPU_IO — V_CPU_IO 4,7,8,9,40,99

DMI

17 DMI_IT_MR_DP[0..3]
17 DMI_IT_MR_DN[0..3]
17 DMI_MT_IR_DP[0..3]
17 DMI_MT_IR_DN[0..3]

Already SWAP

CHECK PCIEX8 swap ?????

76 PEG_RXN[7..0]
PEG_RXN7 PEG_RXN6 PEG_RXN5 PEG_RXN4 PEG_RXN3 PEG_RXN2 PEG_RXN1 PEG_RXN0

76 PEG_RXP[7..0]
PEG_RXP7 PEG_RXP6 PEG_RXP5 PEG_RXP4 PEG_RXP3 PEG_RXP2 PEG_RXP1 PEG_RXP0

CPU1C 3 OF 12
SKYLAKE
LGA1151

B8 PEG_RXP0	B7 PEG_RXN0	PEG_TXP0 A5	PEG_TXN0 A6
C7 PEG_RXP1	C6 PEG_RXN1	PEG_TXP1 B4	PEG_TXN1 B5
D6 PEG_RXP2	D5 PEG_RXN2	PEG_TXP2 C3	PEG_TXN2 C4
E5 PEG_RXP3	E4 PEG_RXN3	PEG_TXP3 D2	PEG_TXN3 D3
F6 PEG_RXP4	F5 PEG_RXN4	PEG_TXP4 E1	PEG_TXN4 E2
G5 PEG_RXP5	G4 PEG_RXN5	PEG_TXP5 F2	PEG_TXN5 F3
H6 PEG_RXP6	H5 PEG_RXN6	PEG_TXP6 G1	PEG_TXN6 G2
J5 PEG_RXP7	J4 PEG_RXN7	PEG_TXP7 H2	PEG_TXN7 H3
K6 PEG_RXP8	K5 PEG_RXN8	PEG_TXP8 J1	PEG_TXN8 J2
L5 PEG_RXP9	L4 PEG_RXN9	PEG_TXP9 K2	PEG_TXN9 K3
M6 PEG_RXP10	M5 PEG_RXN10	PEG_TXP10 L1	PEG_TXN10 L2
N5 PEG_RXP11	N4 PEG_RXN11	PEG_TXP11 M2	PEG_TXN11 M3
P6 PEG_RXP12	P5 PEG_RXN12	PEG_TXP12 N1	PEG_TXN12 N2
R5 PEG_RXP13	R4 PEG_RXN13	PEG_TXP13 P2	PEG_TXN13 P3
T6 PEG_RXP14	T5 PEG_RXN14	PEG_TXP14 R2	PEG_TXN14 R1
U5 PEG_RXP15	U4 PEG_RXN15	PEG_TXP15 T2	PEG_TXN15 T3

PEG_RXP7 PEG_RXN7 — PEG_C_TXP7 PEG_C_TXN7
PEG_RXP6 PEG_RXN6 — PEG_C_TXP6 PEG_C_TXN6
PEG_RXP5 PEG_RXN5 — PEG_C_TXP5 PEG_C_TXN5
PEG_RXP4 PEG_RXN4 — PEG_C_TXP4 PEG_C_TXN4
PEG_RXP3 PEG_RXN3 — PEG_C_TXP3 PEG_C_TXN3
PEG_RXP2 PEG_RXN2 — PEG_C_TXP2 PEG_C_TXN2
PEG_RXP1 PEG_RXN1 — PEG_C_TXP1 PEG_C_TXN1
PEG_RXP0 PEG_RXN0 — PEG_C_TXP0 PEG_C_TXN0

V_CPU_IO
R63 24D9R2F-L-GP
PEG_COMP L7 PEG_RCOMP

DMI_IT_MR_DP0 Y3	DMI_IT_MR_DN0 Y4	DMI_RXP0 DMI_RXN0	DMI_TXP0 AC2 DMI_TXN0 AC1	DMI_MT_IR_DP0 DMI_MT_IR_DN0
DMI_IT_MR_DP1 AA4	DMI_IT_MR_DN1 AA5	DMI_RXP1 DMI_RXN1	DMI_TXP1 AD3 DMI_TXN1 AD2	DMI_MT_IR_DP1 DMI_MT_IR_DN1
DMI_IT_MR_DP2 AB4	DMI_IT_MR_DN2 AB3	DMI_RXP2 DMI_RXN2	DMI_TXP2 AE2 DMI_TXN2 AE1	DMI_MT_IR_DP2 DMI_MT_IR_DN2
DMI_IT_MR_DP3 AC4	DMI_IT_MR_DN3 AC5	DMI_RXP3 DMI_RXN3	DMI_TXP3 AF2 DMI_TXN3 AF3	DMI_MT_IR_DP3 DMI_MT_IR_DN3

SKYLAKE-1

06/24 Allen add

PEG_C_TXN7 (G_) C11898 1 — 1 SCD22U10V2KX-2-GP — PEG_TXN7
PEG_C_TXN6 (G_) C11899 1 — 1 SCD22U10V2KX-2-GP — PEG_TXN6
PEG_C_TXN5 (G_) C11900 1 — 1 SCD22U10V2KX-2-GP — PEG_TXN5
PEG_C_TXN4 (G_) C11902 1 — 1 SCD22U10V2KX-2-GP — PEG_TXN4
PEG_C_TXN3 (G_) C11904 1 — 1 SCD22U10V2KX-2-GP — PEG_TXN3
PEG_C_TXN2 (G_) C11905 1 — 1 SCD22U10V2KX-2-GP — PEG_TXN2
PEG_C_TXN1 (G_) C11907 1 — 1 SCD22U10V2KX-2-GP — PEG_TXN1
PEG_C_TXN0 (G_) C11908 1 — 1 SCD22U10V2KX-2-GP — PEG_TXN0
PEG_TXN[7..0] 76

PEG_C_TXP7 (G_) C12138 1 — 1 SCD22U10V2KX-2-GP — PEG_TXP7
PEG_C_TXP6 (G_) C12139 1 — 1 SCD22U10V2KX-2-GP — PEG_TXP6
PEG_C_TXP5 (G_) C12140 1 — 1 SCD22U10V2KX-2-GP — PEG_TXP5
PEG_C_TXP4 (G_) C12141 1 — 1 SCD22U10V2KX-2-GP — PEG_TXP4
PEG_C_TXP3 (G_) C12142 1 — 1 SCD22U10V2KX-2-GP — PEG_TXP3
PEG_C_TXP2 (G_) C12143 1 — 1 SCD22U10V2KX-2-GP — PEG_TXP2
PEG_C_TXP1 (G_) C12144 1 — 1 SCD22U10V2KX-2-GP — PEG_TXP1
PEG_C_TXP0 (G_) C12145 1 — 1 SCD22U10V2KX-2-GP — PEG_TXP0
PEG_TXP[7..0] 76

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

Sandy Bridge Socket

SKT1 Load Plate (22.78003.021)
SKT2 Back Plate (22.78006.031)
SKT3 CPU Cover (42.3EQ28.011)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 005_CPU_PCIE
Size: C | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2
Date: | Sheet 5 of 107

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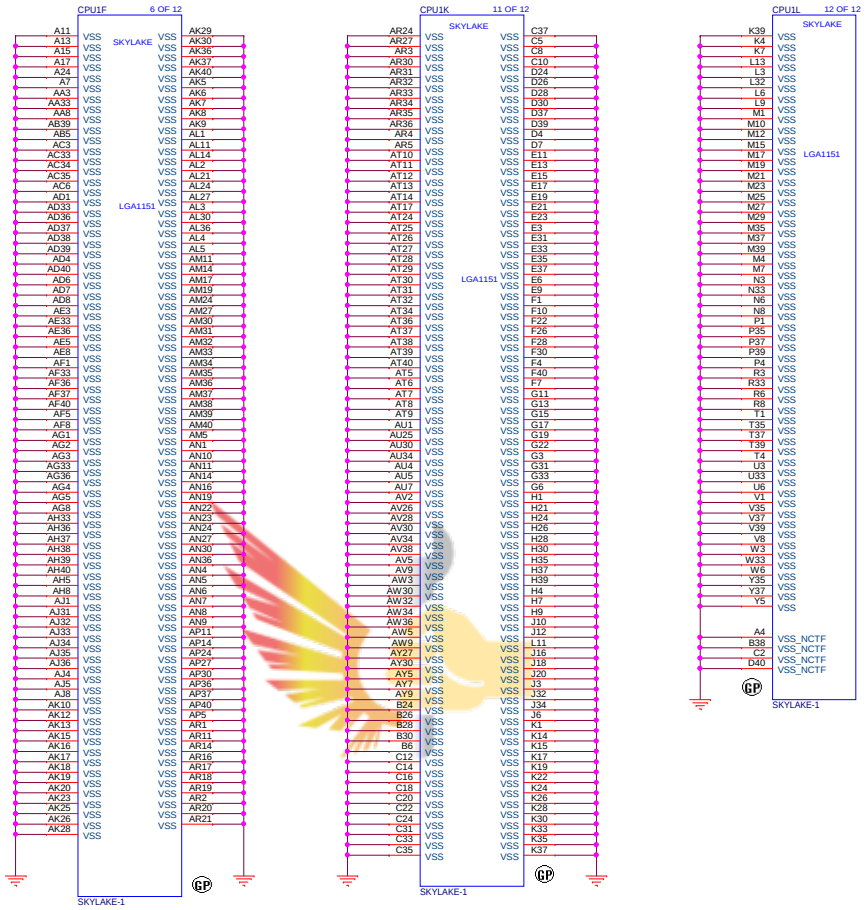

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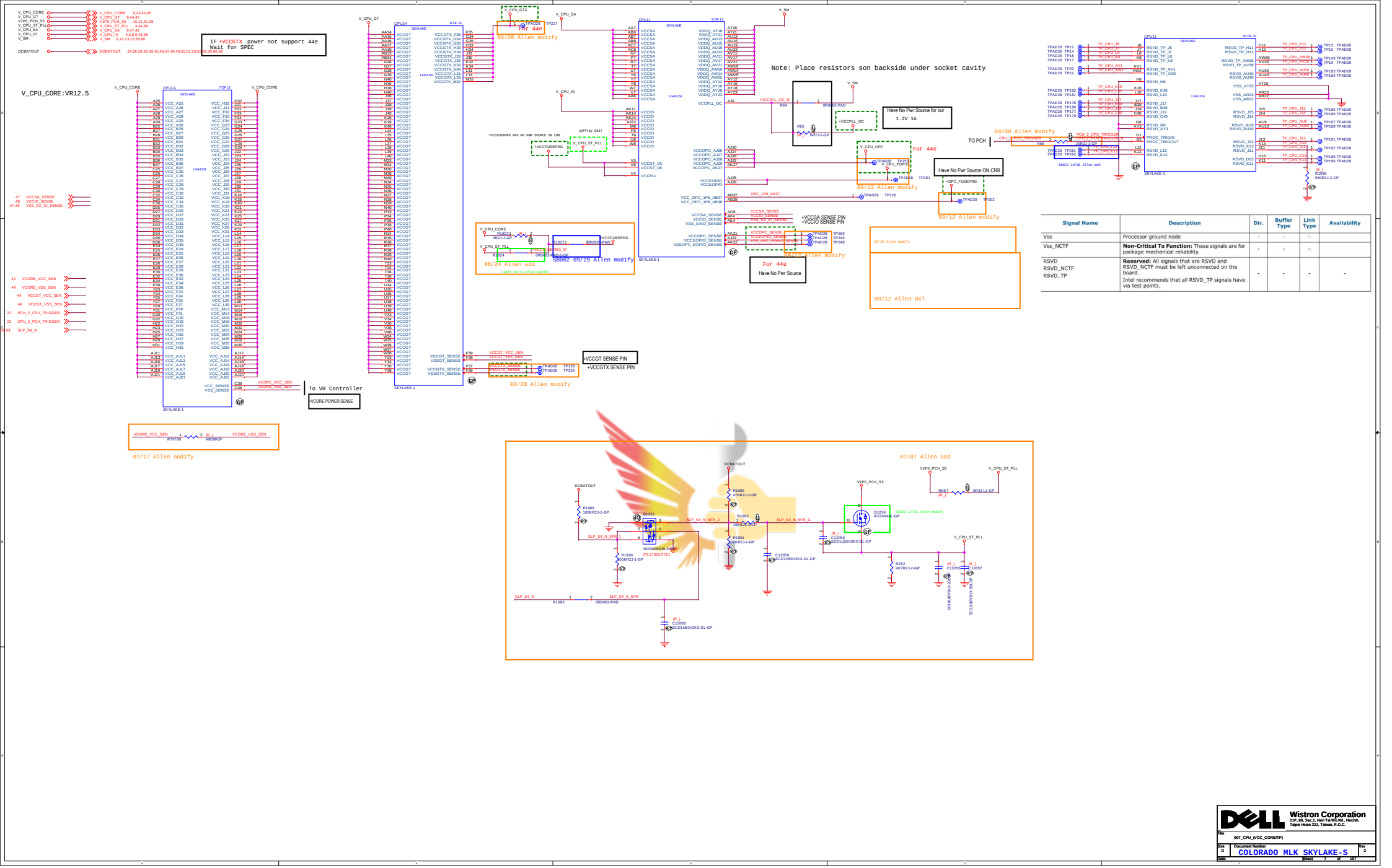
Title: 006_CPU_(VSS)

Size: C | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 6 of 107



Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
Vss	Processor ground node	-	-	-	
Vss_NCTF	**Non-Critical To Function:** These signals are for package mechanical reliability.	-	-	-	
RSVD RSVD_NCTF RSVD_TP	**Reserved:** All signals that are RSVD and RSVD_NCTF must be left unconnected on the board. Intel recommends that all RSVD_TP signals have via test points.	-	-	-	-

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Title: 007_CPU_(VCC_CORE/TP)

Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

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V_CPU_IO → V_CPU_IO 4,5,7,9,48,99

HDMI PORT B

56 DDSP_B_TX_DN_0
56 DDSP_B_TX_DP_0
56 DDSP_B_TX_DN_1
56 DDSP_B_TX_DP_1
56 DDSP_B_TX_DN_2
56 DDSP_B_TX_DP_2
56 DDSP_B_TX_DN_3
56 DDSP_B_TX_DP_3

eDISPLAY PORT E

55 DPD_LANE0P
55 DPD_LANE0N
55 DPD_LANE1P
55 DPD_LANE1N
55 DPD_LANE2P
55 DPD_LANE2N
55 DPD_LANE3P
55 DPD_LANE3N
55 DPD_AUXN
55 DPD_AUXP

AUDIO

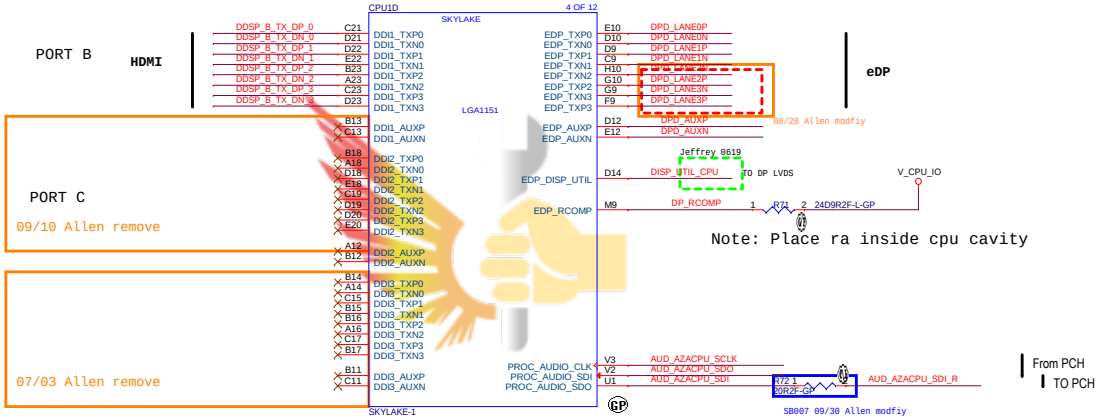
15 AUD_AZACPU_SCLK
15 AUD_AZACPU_SDO
15 AUD_AZACPU_SDI_R
55 DISP_UTIL_CPU

- H/S-processor line processors supports eDP and up to 3 DDI supporting DP/HDMI.

In CRB,
DDI1 for DP
DDI2 dor HDMI
DDI3 for DP HDMI combo
DDI4 for eDP

x4 eDP
Or
x2 eDP + x2 DP

DDI B
(X4 DP/HDMI)
DDI C
(X4 DP/HDMI)
DDI D
(X4 DP/HDMI)



<Variant Name>

Wistron Corporation
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Title: 008_CPU_(DDI/EDP)

Size: C | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

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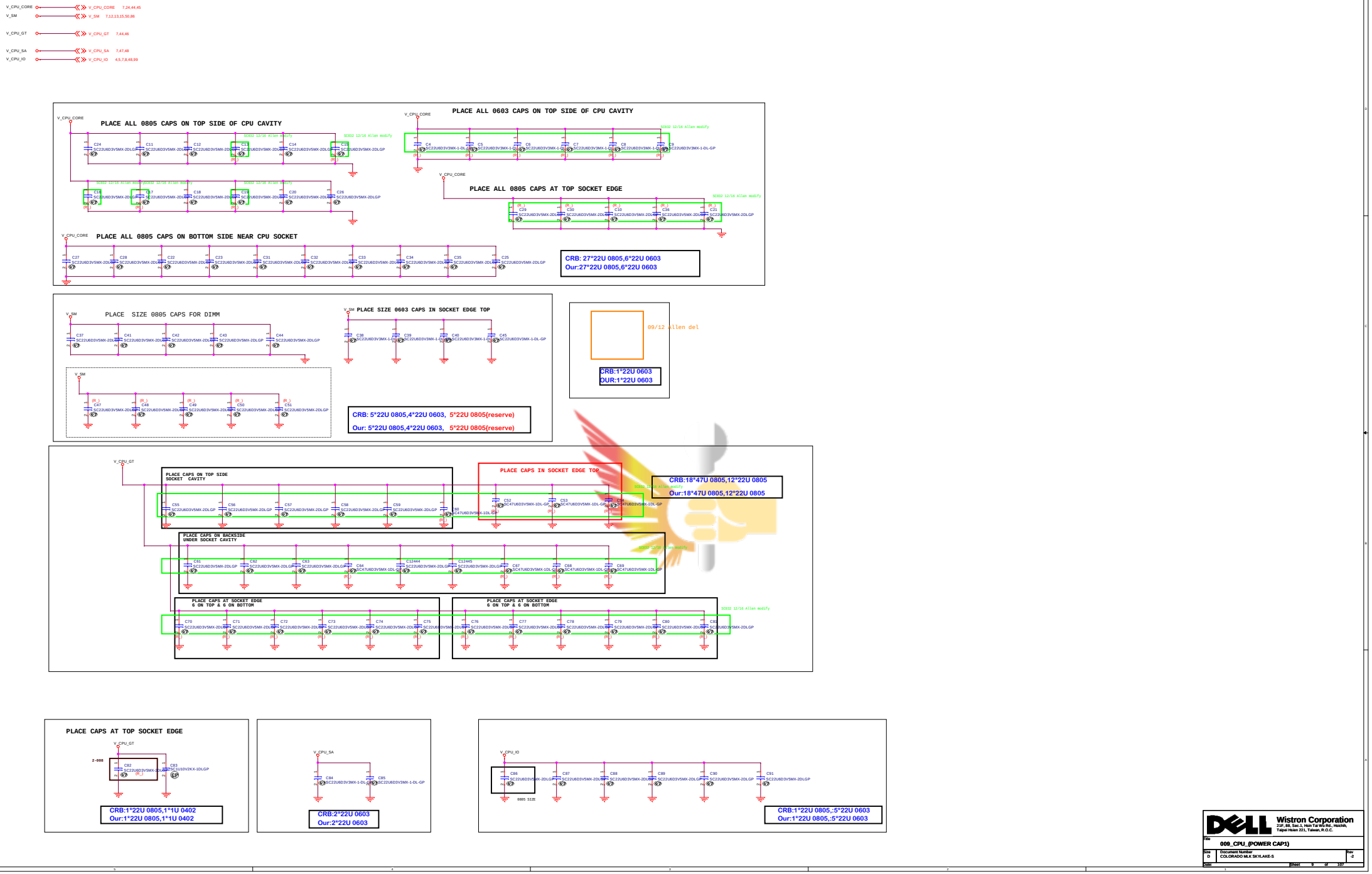

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Taipei Hsien 221, Taiwan, R.O.C.

Title: 009_CPU_(POWER CAP1)

Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

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For 44e

GTTX
CRB:4*22U 0603,10*47U 0805

For 44e

V_CPU_OPC
CRB:6*22U 0603

For 44e

V_CPU_EOPIO
CRB:7*22U 0603

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 010_CPU_(POWER CAP2)

Size: A | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

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<Variant Name>

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Title

Size	Document Number	Rev
D	COLORADO MLK SKYLAKE-S	-2

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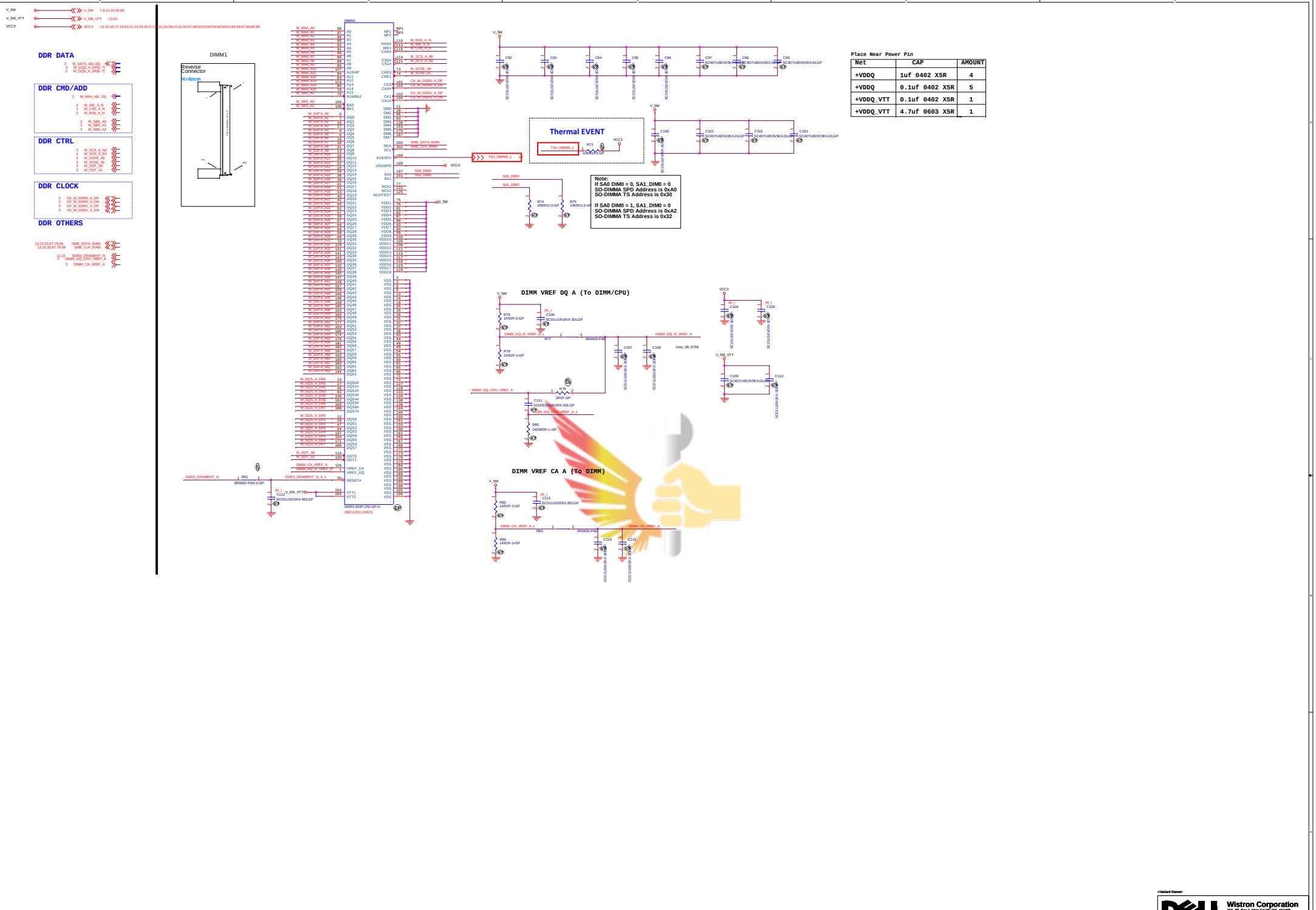

Place Near Power Pin

Net	CAP	AMOUNT
+VDDQ	1uf 0402 X5R	4
+VDDQ	0.1uf 0402 X5R	5
+VDDQ_VTT	0.1uf 0402 X5R	1
+VDDQ_VTT	4.7uf 0603 X5R	1

<Variant Name>

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File: 012_DDR3_SODIMM1

Size: A1 | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 12 of 100

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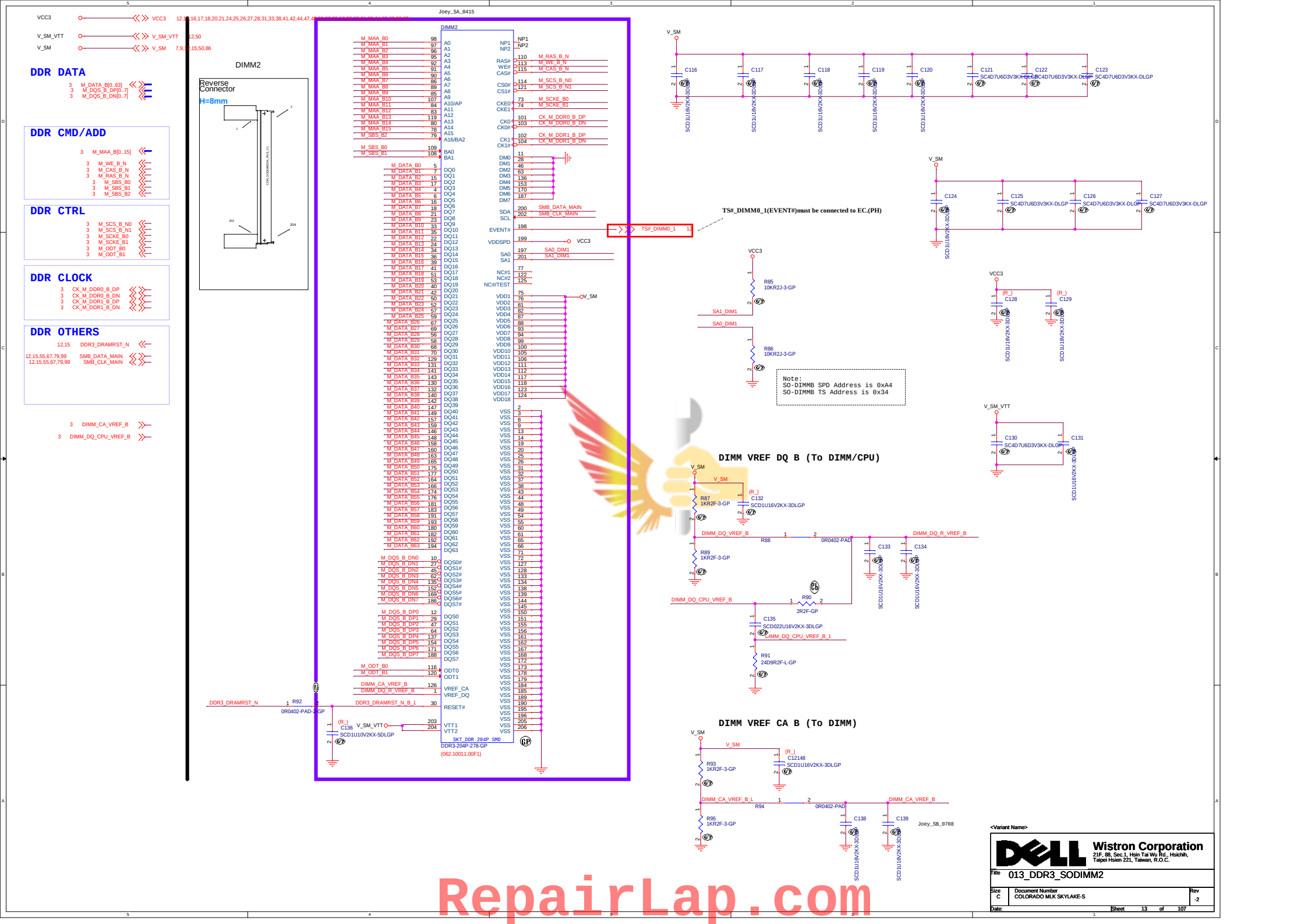

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Blanking

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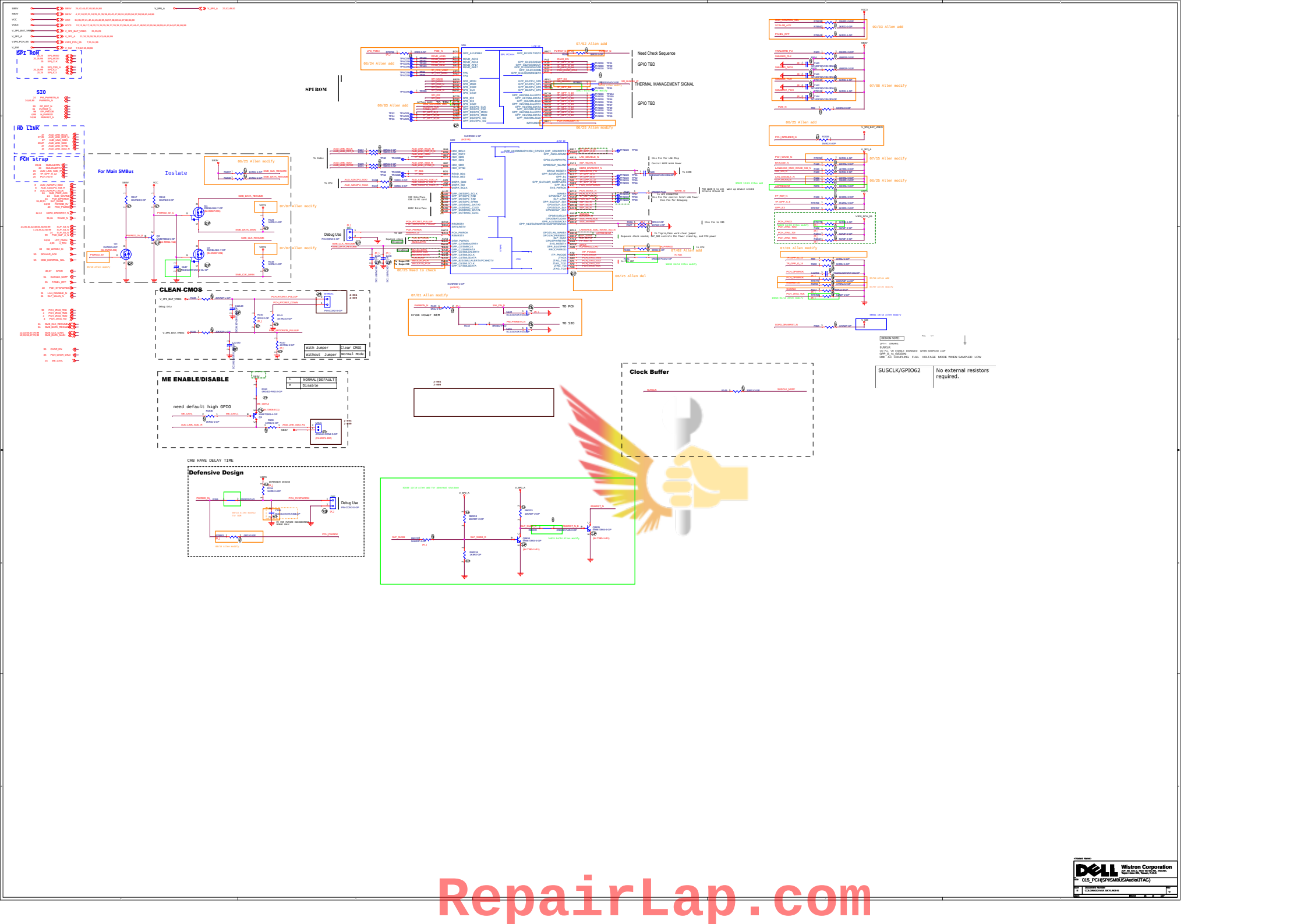
Title		
Size: A4	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
Date:	Sheet 14 of 107	



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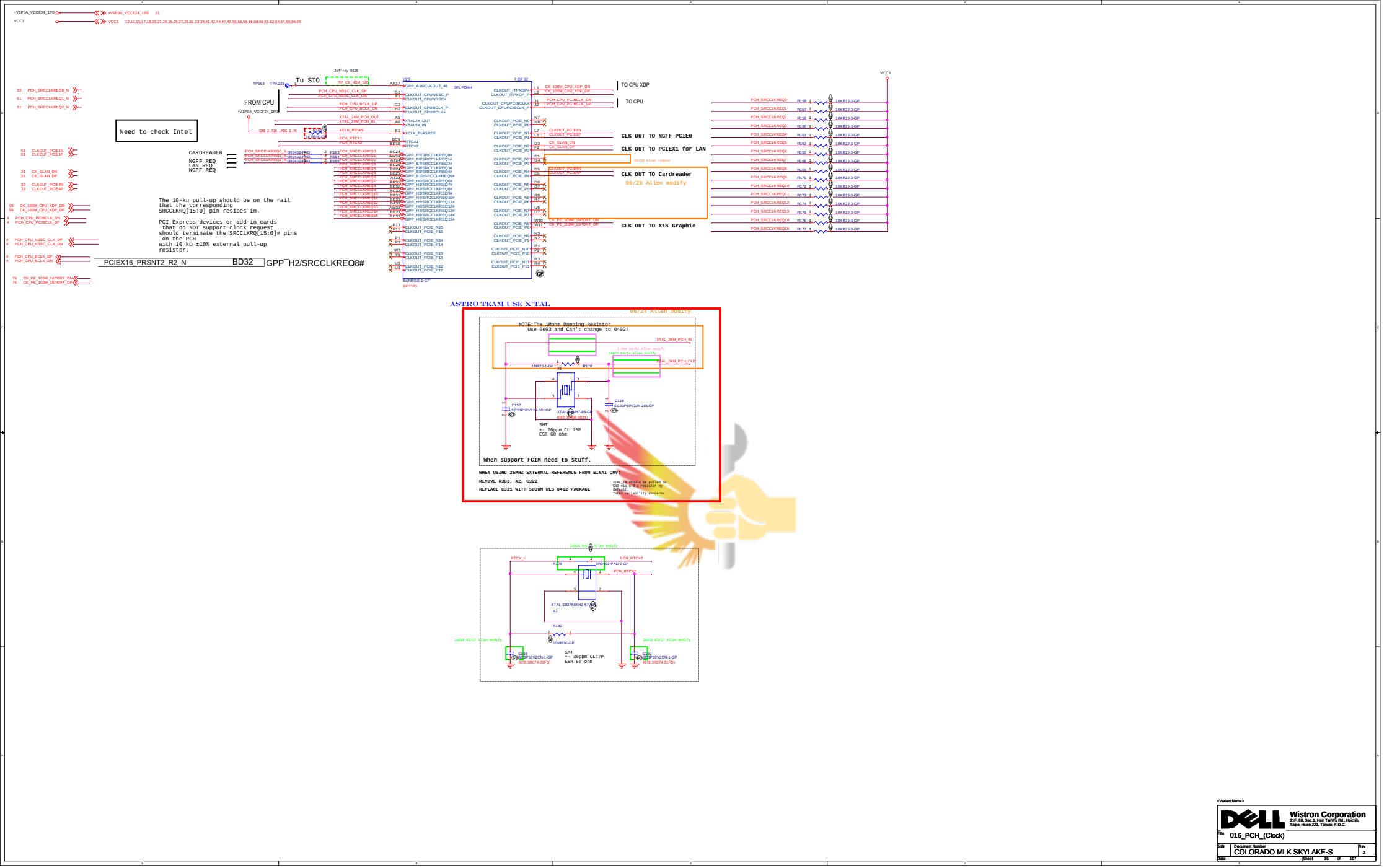

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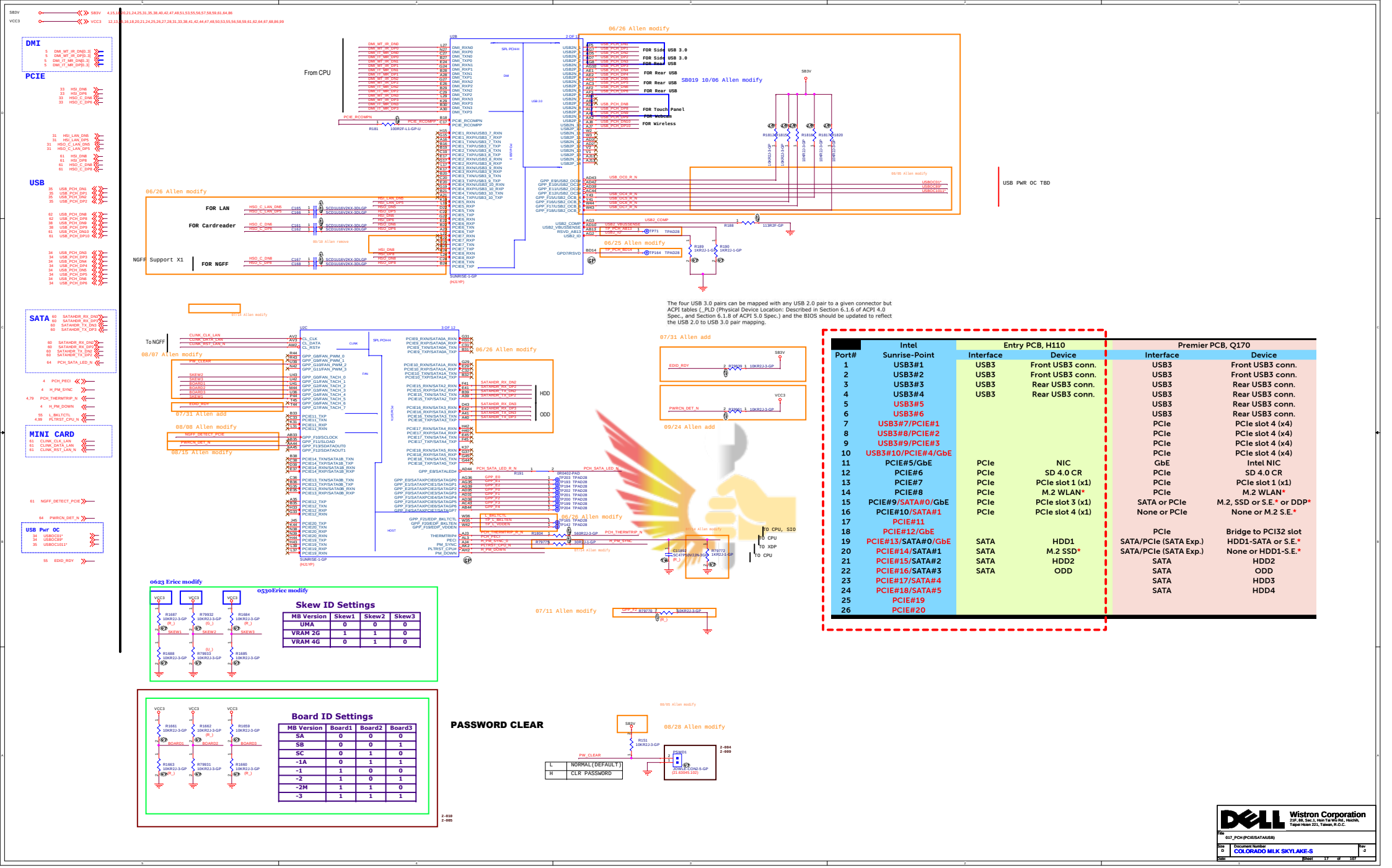

MB Version	Skew1	Skew2	Skew3
UMA	0	0	0
VRAM 2G	1	1	0
VRAM 4G	0	1	0

MB Version	Board1	Board2	Board3
SA	0	0	0
SB	0	0	1
SC	0	1	0
-1A	0	1	1
-1	1	0	0
-2	1	0	1
-2M	1	1	0
-3	1	1	1

L	NORMAL(DEFAULT)
H	CLR PASSWORD

	Intel	Entry PCB, H110		Premier PCB, Q170	
Port#	Sunrise-Point	Interface	Device	Interface	Device
1	USB3#1	USB3	Front USB3 conn.	USB3	Front USB3 conn.
2	USB3#2	USB3	Front USB3 conn.	USB3	Front USB3 conn.
3	USB3#3	USB3	Rear USB3 conn.	USB3	Rear USB3 conn.
4	USB3#4	USB3	Rear USB3 conn.	USB3	Rear USB3 conn.
5	USB3#5			USB3	Rear USB3 conn.
6	USB3#6			USB3	Rear USB3 conn.
7	USB3#7/PCIE#1			PCIe	PCIe slot 4 (x4)
8	USB3#8/PCIE#2			PCIe	PCIe slot 4 (x4)
9	USB3#9/PCIE#3			PCIe	PCIe slot 4 (x4)
10	USB3#10/PCIE#4/GbE			PCIe	PCIe slot 4 (x4)
11	PCIE#5/GbE	PCIe	NIC	GbE	Intel NIC
12	PCIE#6	PCIe	SD 4.0 CR	PCIe	SD 4.0 CR
13	PCIE#7	PCIe	PCIe slot 1 (x1)	PCIe	PCIe slot 1 (x1)
14	PCIE#8	PCIe	M.2 WLAN*	PCIe	M.2 WLAN*
15	PCIE#9/SATA#0/GbE	PCIe	PCIe slot 3 (x1)	SATA or PCIe	M.2, SSD or S.E.* or DDP*
16	PCIE#10/SATA#1	PCIe	PCIe slot 4 (x1)	None or PCIe	None or M.2 S.E.*
17	PCIE#11				
18	PCIE#12/GbE			PCIe	Bridge to PCI32 slot
19	PCIE#13/SATA#0/GbE	SATA	HDD1	SATA/PCIe (SATA Exp.)	HDD1-SATA or S.E.*
20	PCIE#14/SATA#1	SATA	M.2 SSD*	SATA/PCIe (SATA Exp.)	None or HDD1-S.E.*
21	PCIE#15/SATA#2	SATA	HDD2	SATA	HDD2
22	PCIE#16/SATA#3	SATA	ODD	SATA	ODD
23	PCIE#17/SATA#4			SATA	HDD3
24	PCIE#18/SATA#5			SATA	HDD4
25	PCIE#19				
26	PCIE#20				

Wistron Corporation
2F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: 017_PCH(PCIE/SATA/USB)

Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

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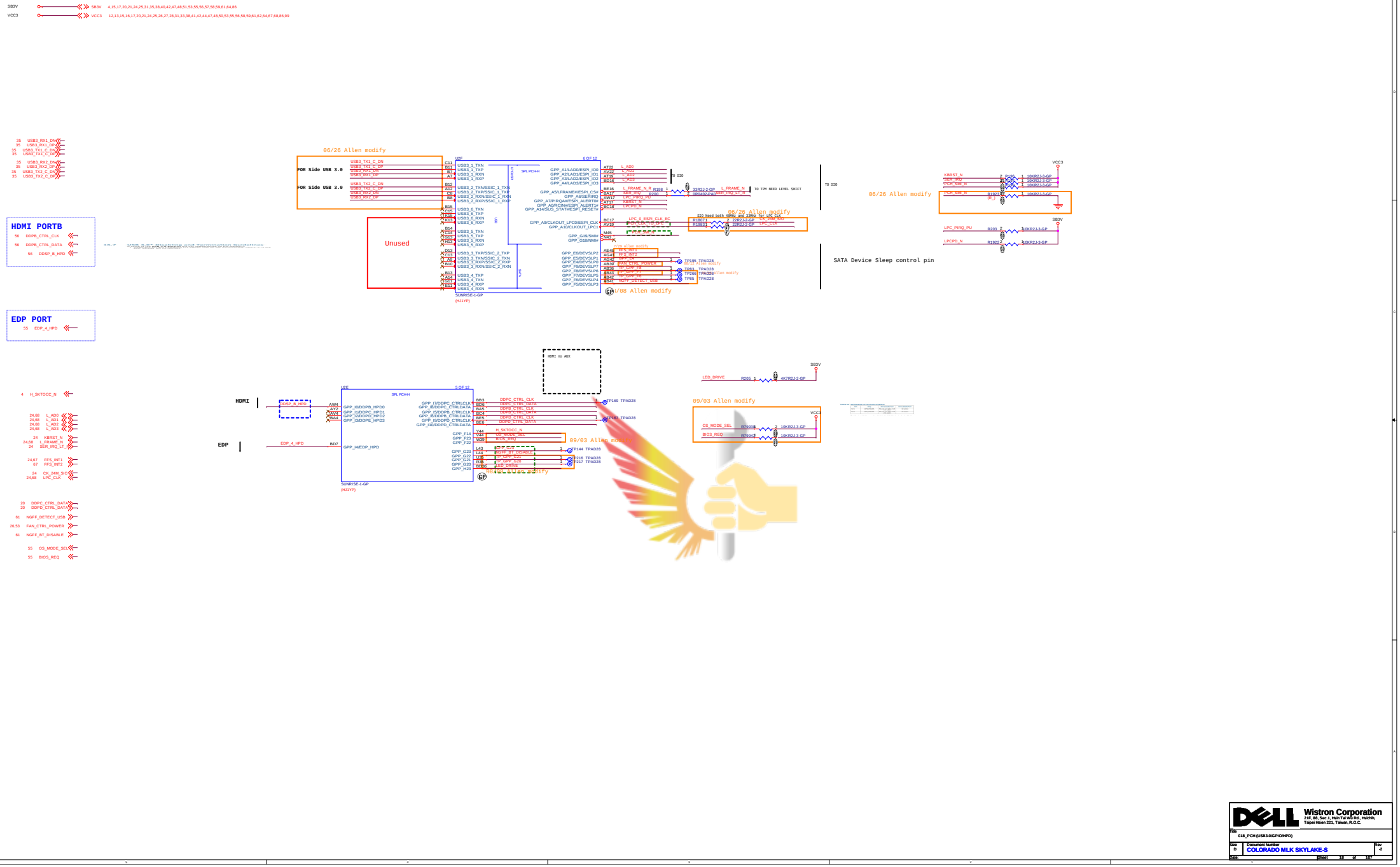
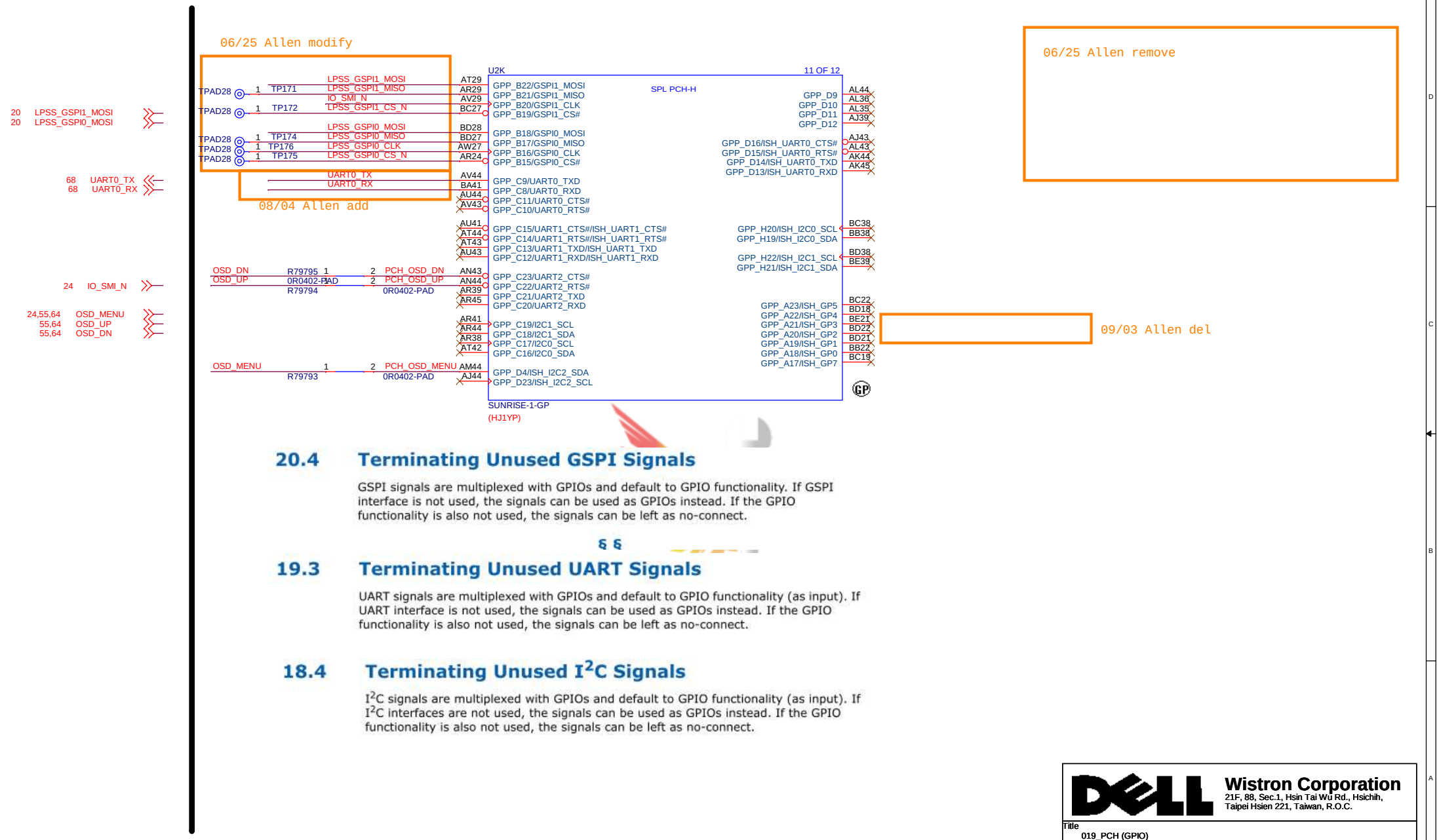

SB3V
VCC3
HDMI PORTB
EDP PORT
06/26 Allen modify
FOR Side USB 3.0
Unused
SATA Device Sleep control pin
HDMI
EDP
09/03 Allen modify
09/08 Allen modify
Wistron Corporation
2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
018_PCH (USB3.0/GPIO/HPD)
COLORADO MLK SKYLAKE-S
RepairLap.com



20.4 Terminating Unused GSPI Signals

GSPI signals are multiplexed with GPIOs and default to GPIO functionality. If GSPI interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

§ §

19.3 Terminating Unused UART Signals

UART signals are multiplexed with GPIOs and default to GPIO functionality (as input). If UART interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

18.4 Terminating Unused I²C Signals

I²C signals are multiplexed with GPIOs and default to GPIO functionality (as input). If I²C interfaces are not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

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Title: 019_PCH (GPIO)		
Size: B	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
Date:	Sheet 19 of 107	

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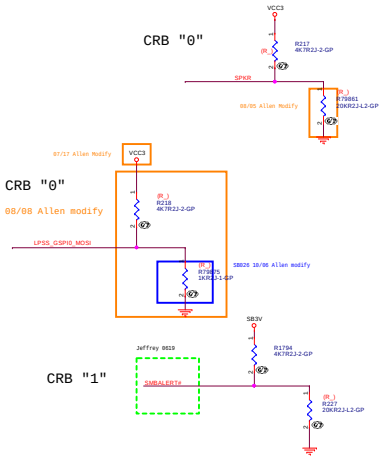
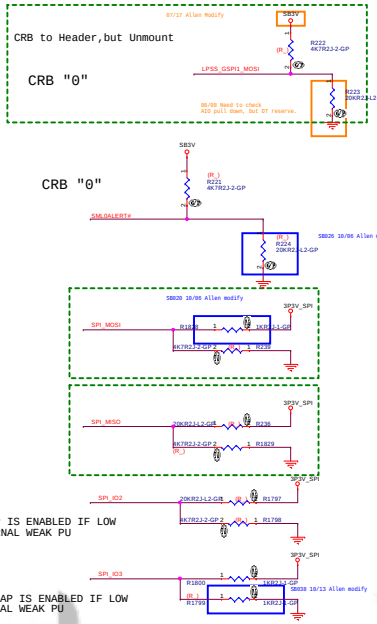
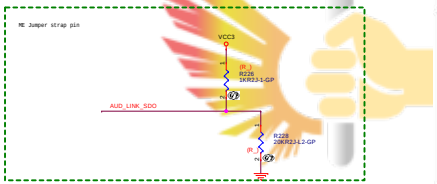
Check GPIO require to Pull Up or Pull down



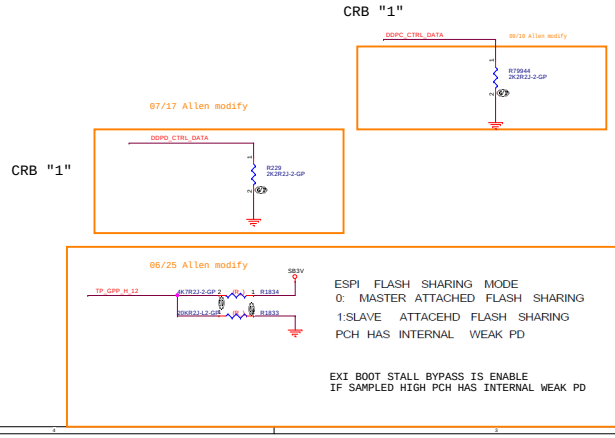
Signal	Usage	When Sampled	Comment
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FITC). ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.



Signal	Usage	When Sampled	Comment
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). Bit 6: 0 = SPI (Default); 1 = LPC ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** Is selected for EC. (Default) 1 = **eSPI** Is selected for EC. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SPI0_MOSI	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SML1ALERT# / PCHHOT# / GPP_B23	Reserved	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



Signal	Usage	When Sampled	Comment
HDA_SDO	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Asserting HDA_SDO high on the rising edge of PCH_PWROK will also halt Intel Management Engine after Chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. 3. This signal is in the primary well.
DDPB_CTRLDATA / GPP_I6	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_I8	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPD_CTRLDATA / GPP_I10	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
GPP_H12	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Note:*** The pull-down resistor is disabled after RSMRST# de-asserts



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Title: 020_PCH_(Stap Pin)
Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2
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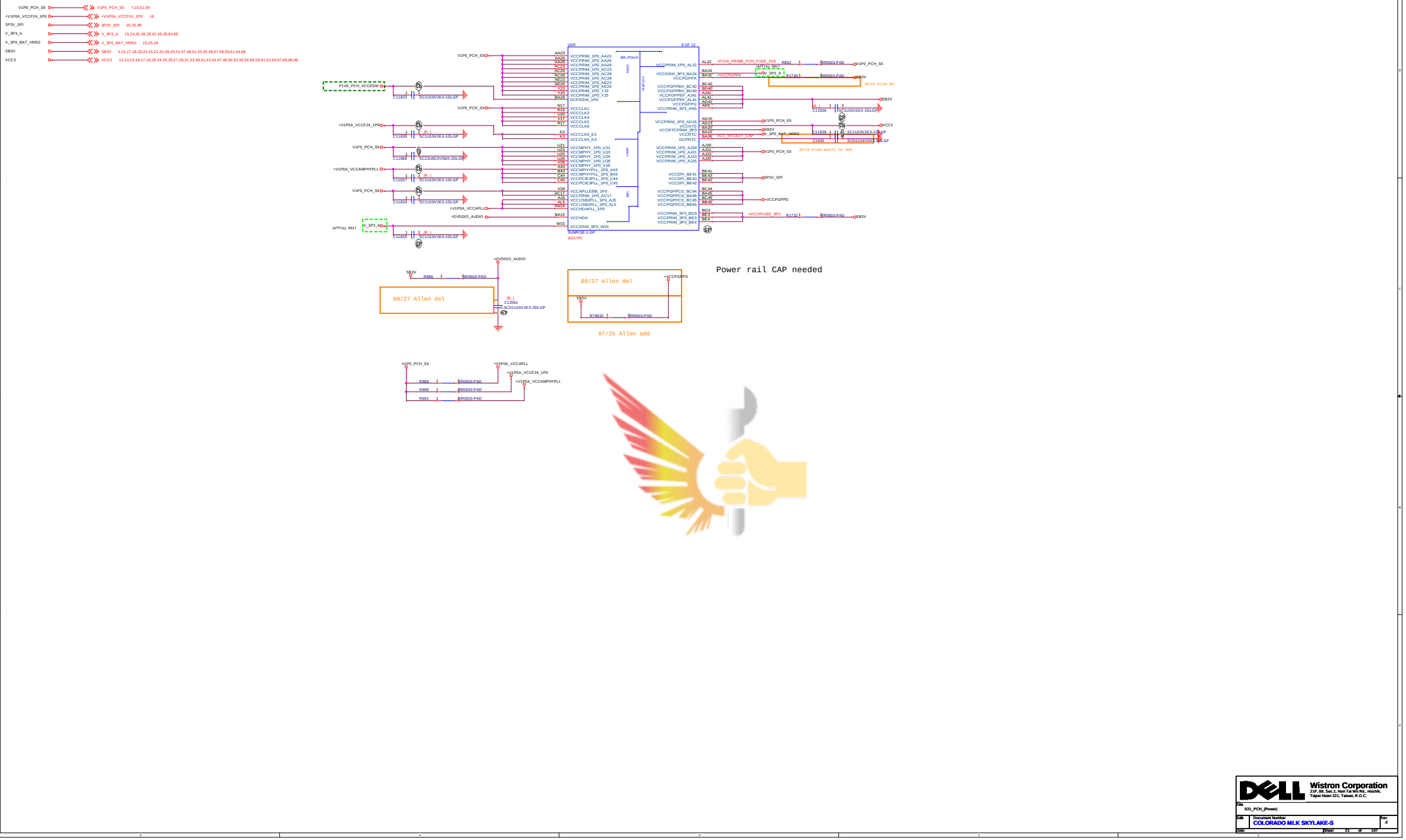

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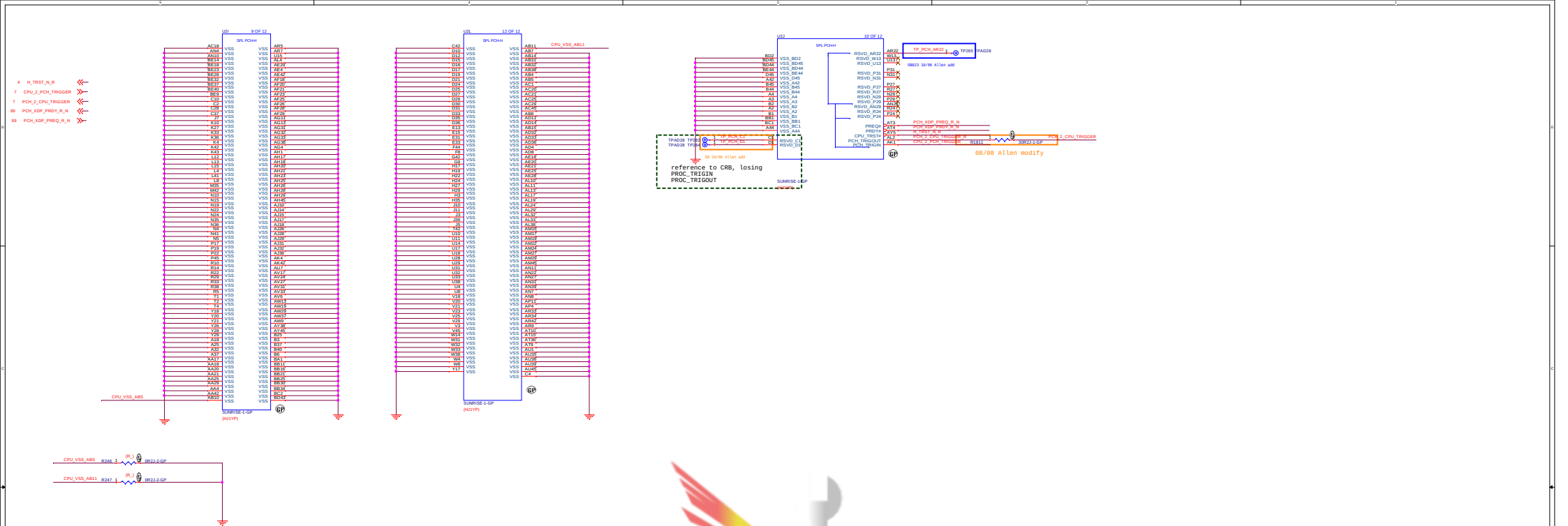

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Wistron Corporation	Title: 022_PCH_(Vss/TP)	
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Blanking

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Title: 023_PCH_(Reserved)		
Size: A4	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
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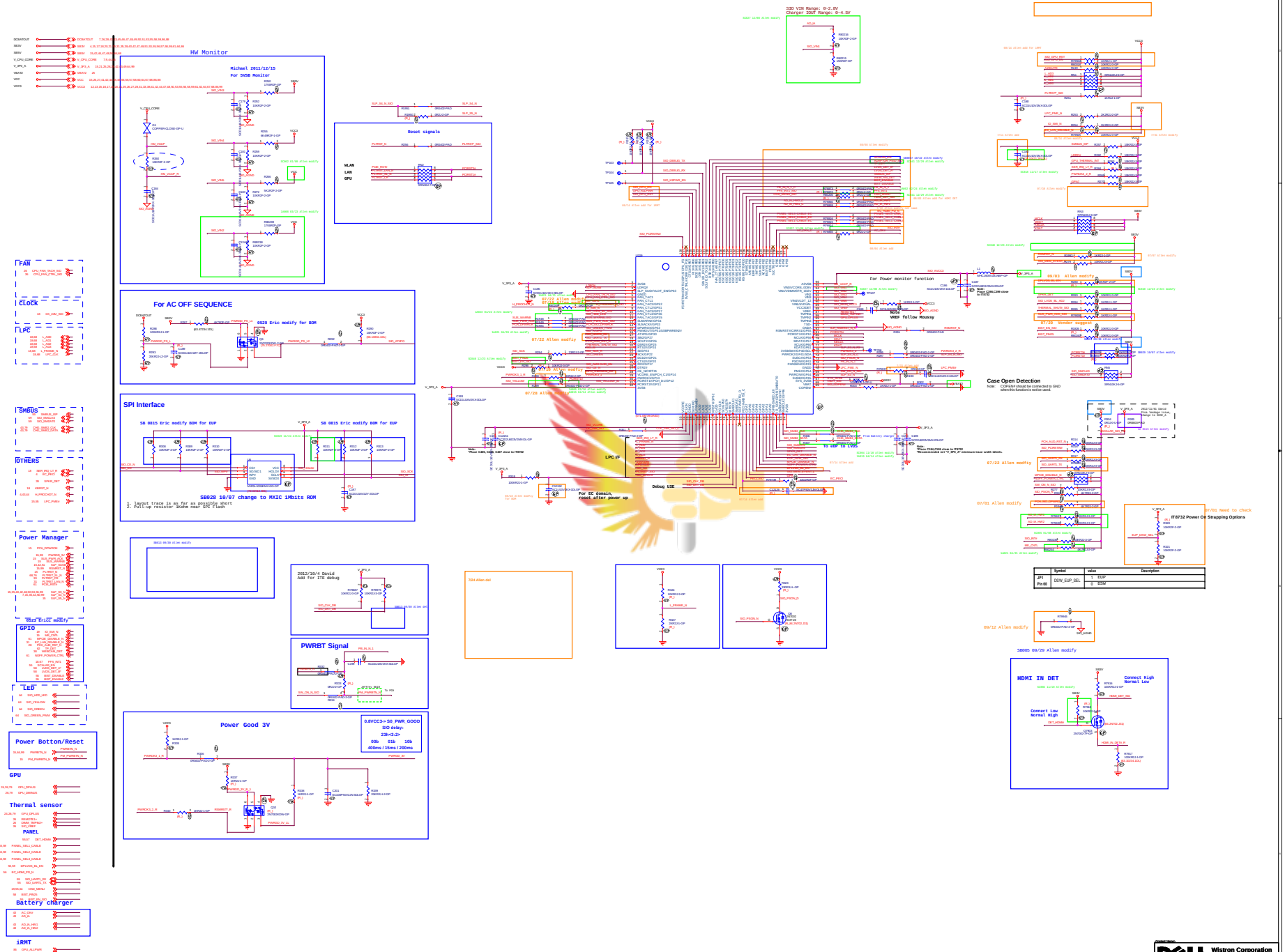

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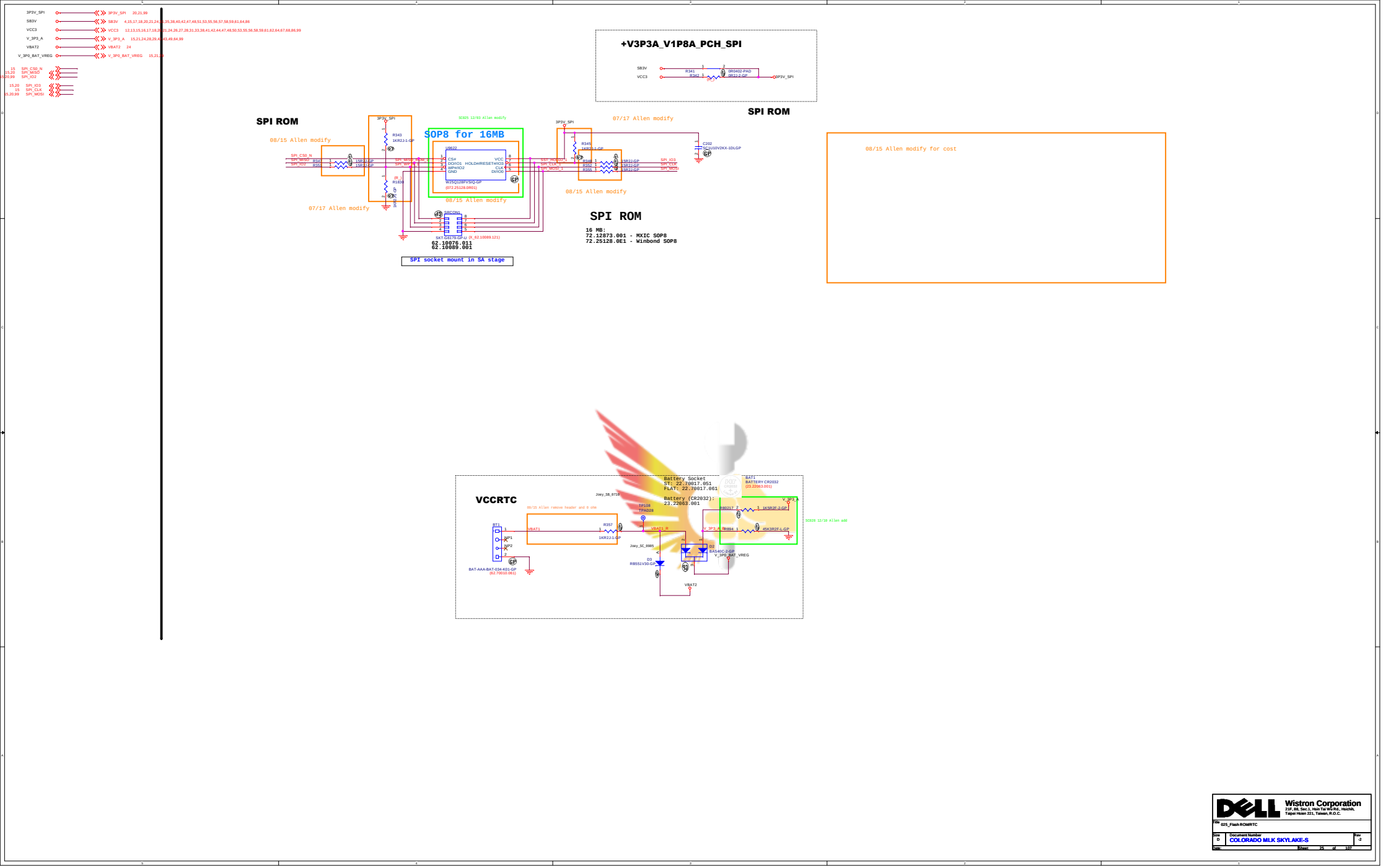

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DCBATOUT
VCC
VCC3
12V_S0

SIO FAN CONTROL

24 CPU_FAN_CTRL_SIO
24 CPU_FAN_TACH_SIO

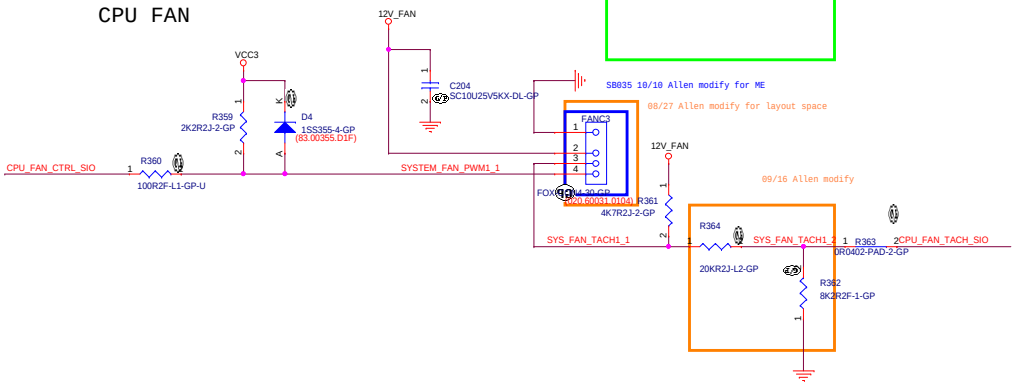
From SIO

18,53 FAN_CTRL_POWER

24 SIO_VREF
24 REMOTE1+
24 DIMM_TMPIN2+
24,79 GPU_DPLUS
79 GPU_DMINUS

4 PINS FAN CONTROL

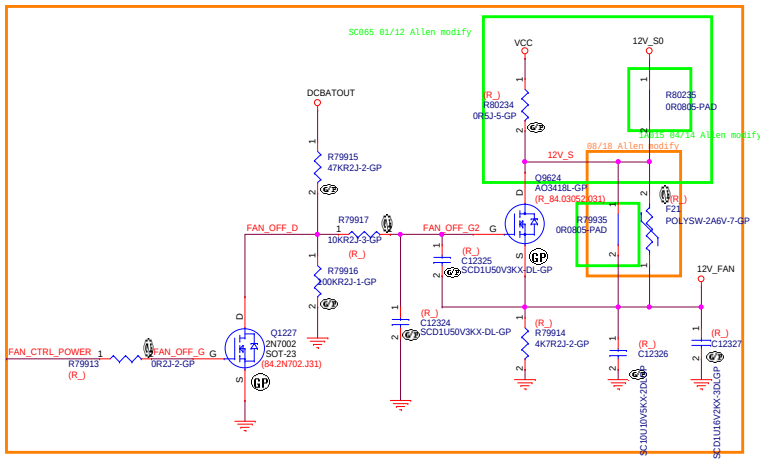
CPU FAN



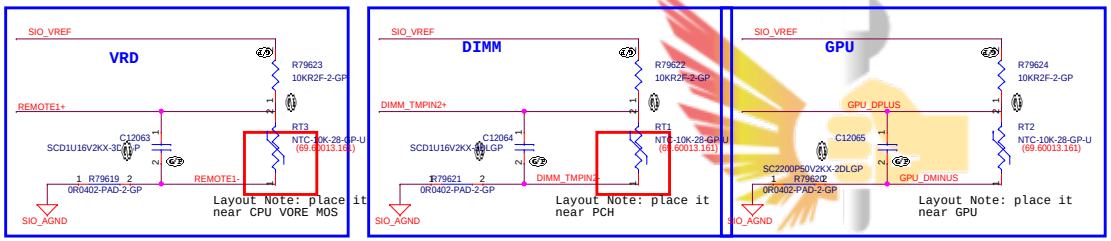
07/29 Allen modify for down size

SC065 01/12 Allen del

08/12 Allen add



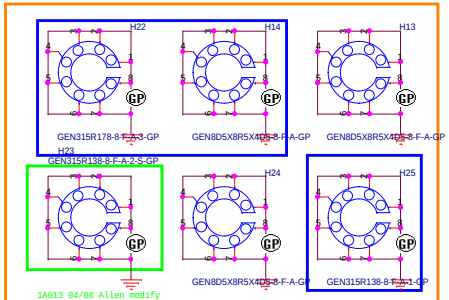
THERMAL DIODES

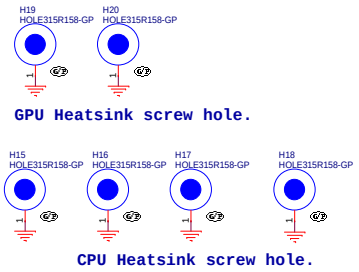


09/02 Allen modify for ME

SB021 10/06 Allen modify

A





SB006 09/30 Allen modify

<Variant Name>

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Title 026_FAN CIRCUITS/HOLE

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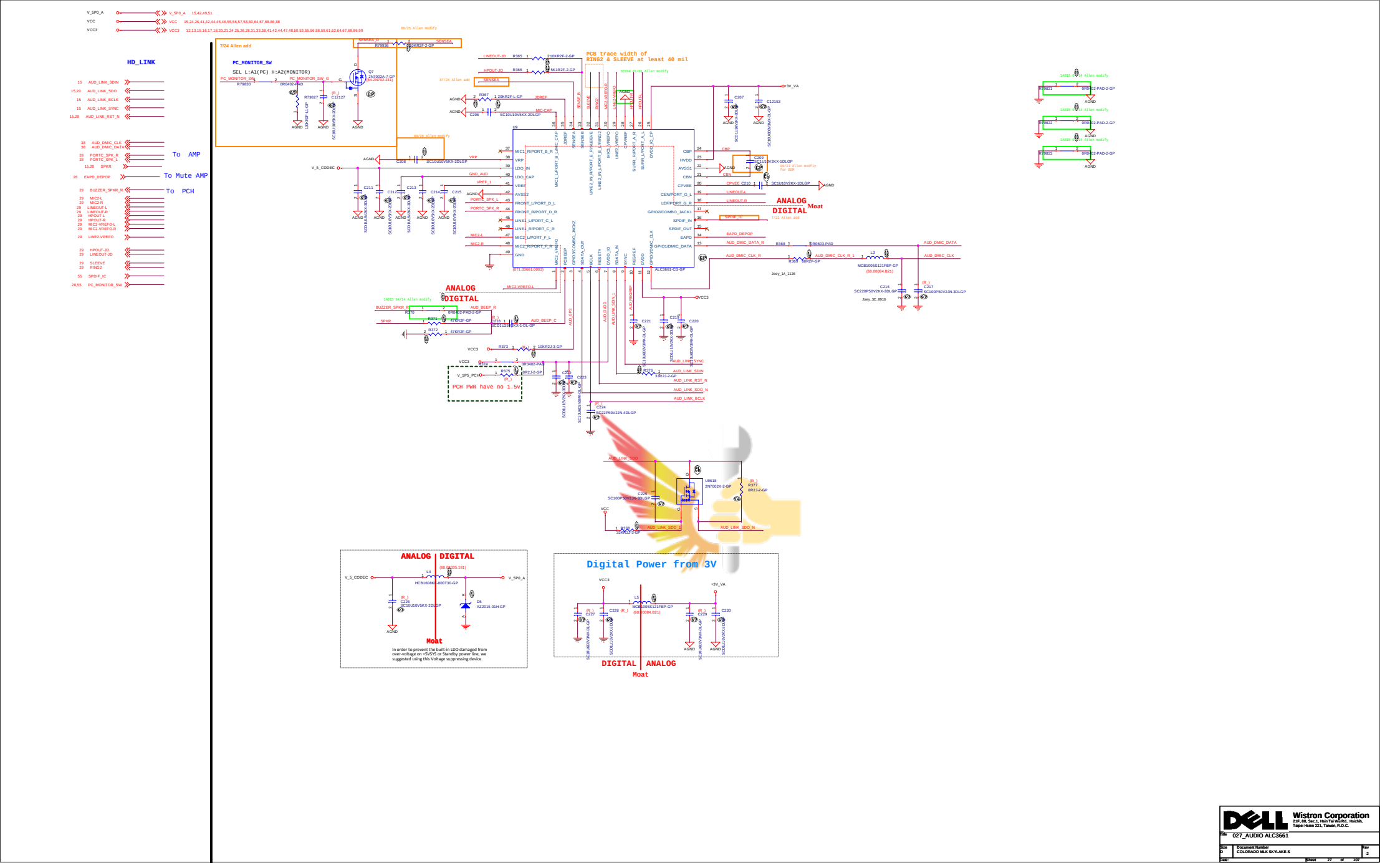

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Title: 027_AUDIO ALC3661

Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

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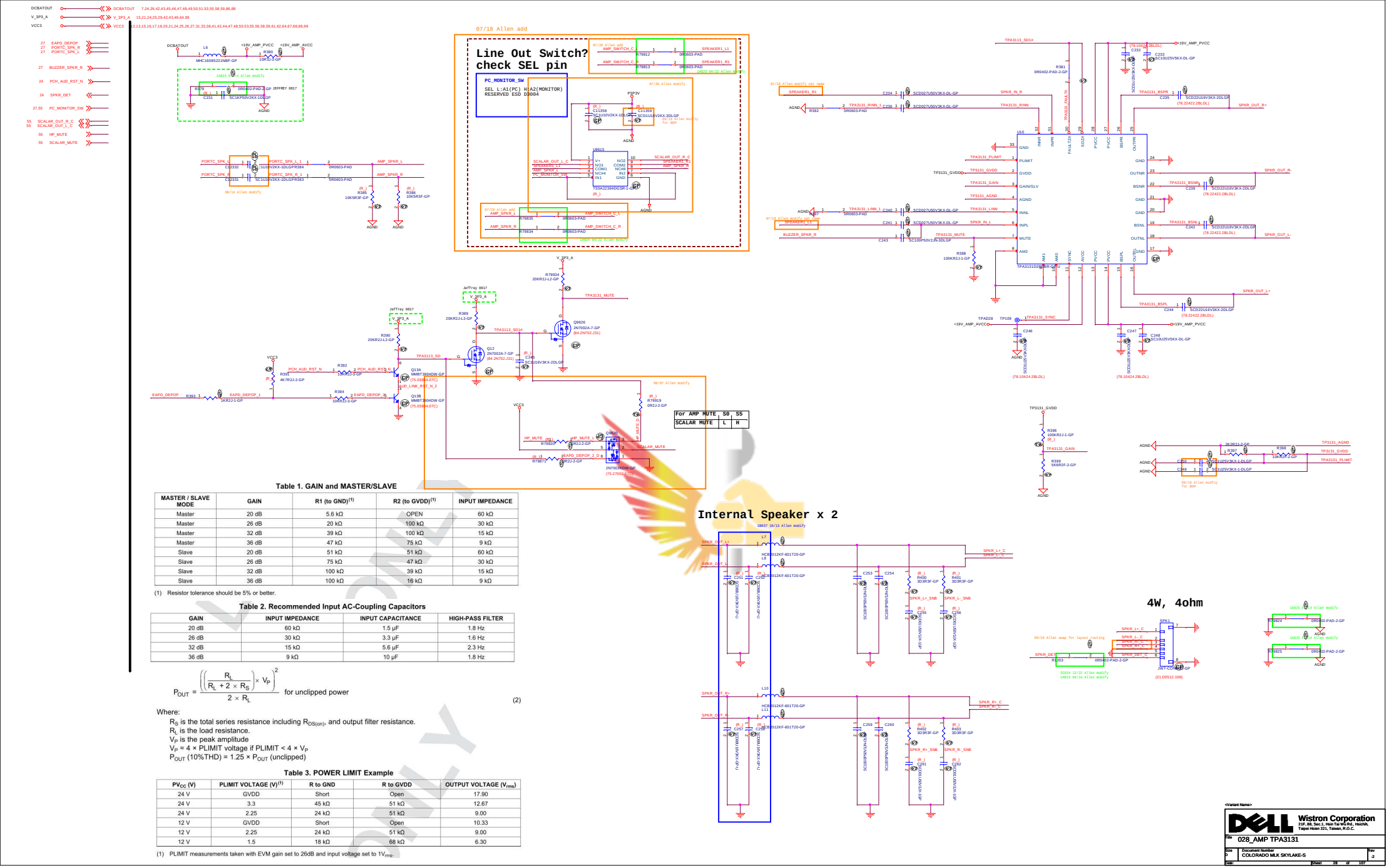

Table 1. GAIN and MASTER/SLAVE

MASTER / SLAVE MODE	GAIN	R1 (to GND)(1)	R2 (to GVDD)(1)	INPUT IMPEDANCE
Master	20 dB	5.6 kΩ	OPEN	60 kΩ
Master	26 dB	20 kΩ	100 kΩ	30 kΩ
Master	32 dB	39 kΩ	100 kΩ	15 kΩ
Master	36 dB	47 kΩ	75 kΩ	9 kΩ
Slave	20 dB	51 kΩ	51 kΩ	60 kΩ
Slave	26 dB	75 kΩ	47 kΩ	30 kΩ
Slave	32 dB	100 kΩ	39 kΩ	15 kΩ
Slave	36 dB	100 kΩ	16 kΩ	9 kΩ

(1) Resistor tolerance should be 5% or better.

Table 2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	60 kΩ	1.5 µF	1.8 Hz
26 dB	30 kΩ	3.3 µF	1.6 Hz
32 dB	15 kΩ	5.6 µF	2.3 Hz
36 dB	9 kΩ	10 µF	1.8 Hz

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power} \qquad (2)$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
R_L is the load resistance.
V_P is the peak amplitude
$V_P = 4 \times$ PLIMIT voltage if PLIMIT $< 4 \times V_P$
P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)

Table 3. POWER LIMIT Example

PV_{CC} (V)	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	OUTPUT VOLTAGE (V_{rms})
24 V	GVDD	Short	Open	17.90
24 V	3.3	45 kΩ	51 kΩ	12.67
24 V	2.25	24 kΩ	51 kΩ	9.00
12 V	GVDD	Short	Open	10.33
12 V	2.25	24 kΩ	51 kΩ	9.00
12 V	1.5	18 kΩ	68 kΩ	6.30

(1) PLIMIT measurements taken with EVM gain set to 26dB and input voltage set to 1V_{rms}.

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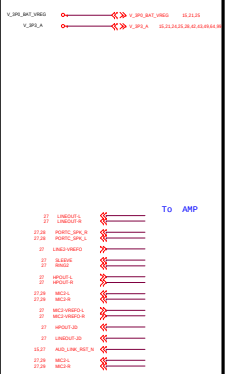

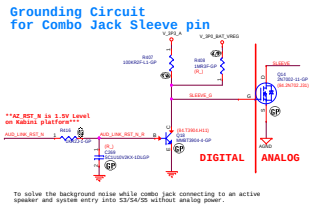

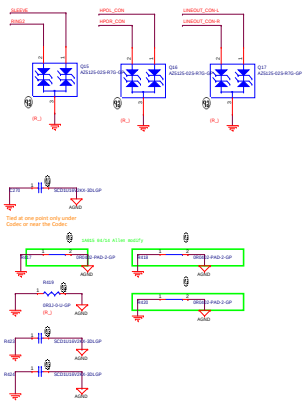

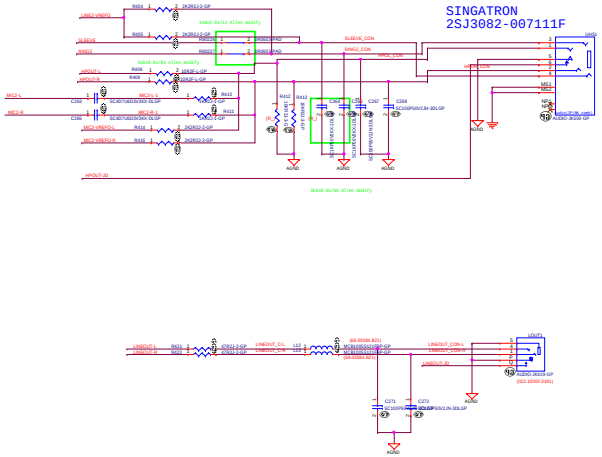

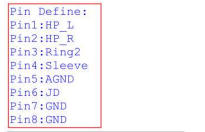

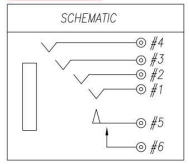

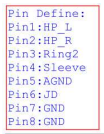

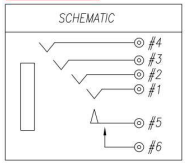

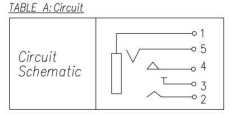

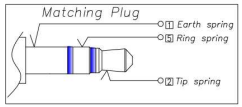

4-pin 3.5mm Headset Connector Pinout

Nokia, Lenovo mobile		
Pin Number	Pin Name	Description
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	**Microphone**
4	Sleeve	**Ground / Common**

iPhone, Samsung, Blackberry, HTC		
Pin Number	Pin Name	Description
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	**Ground / Common**
4	Sleeve	**Microphone**

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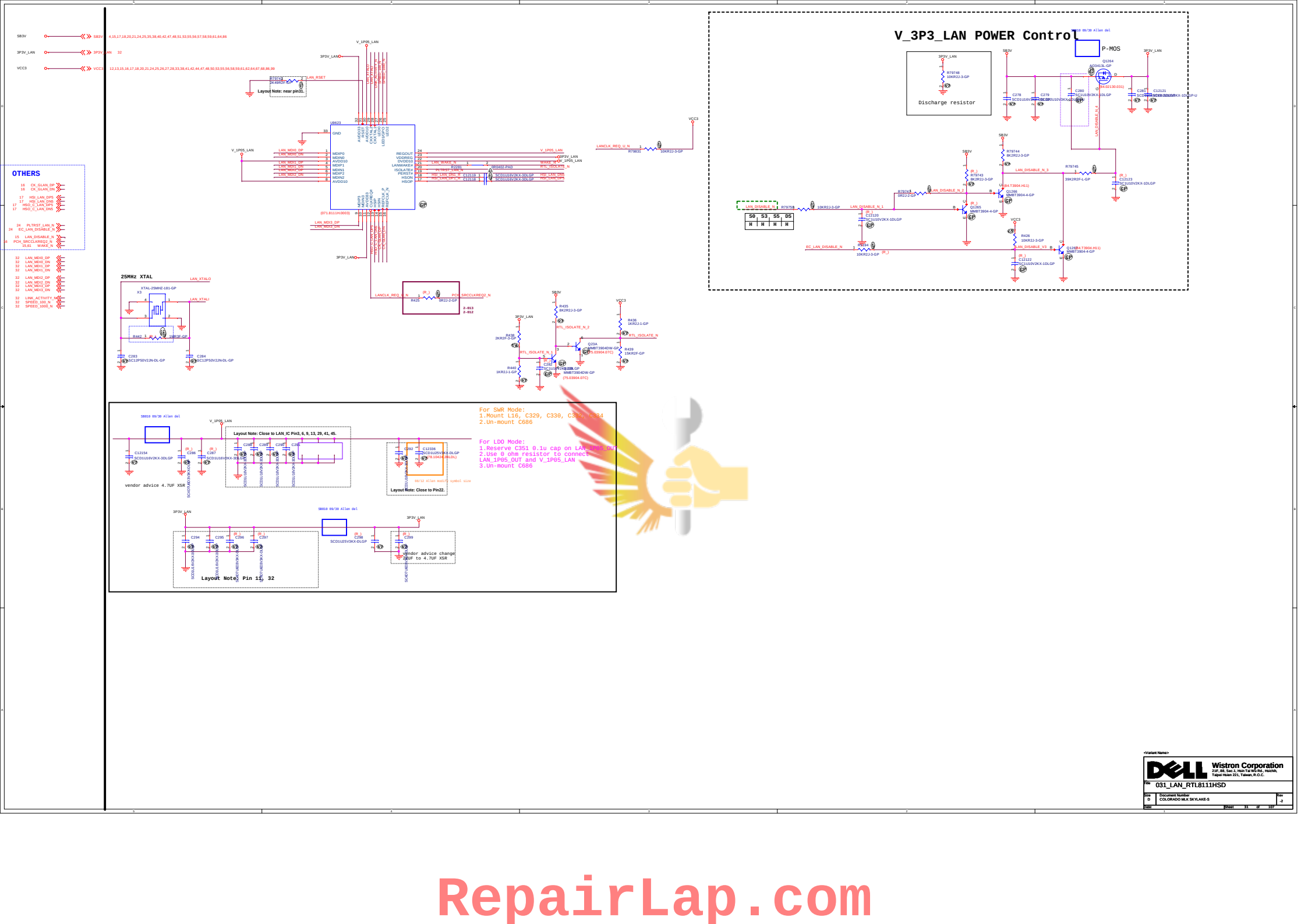

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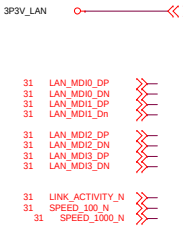
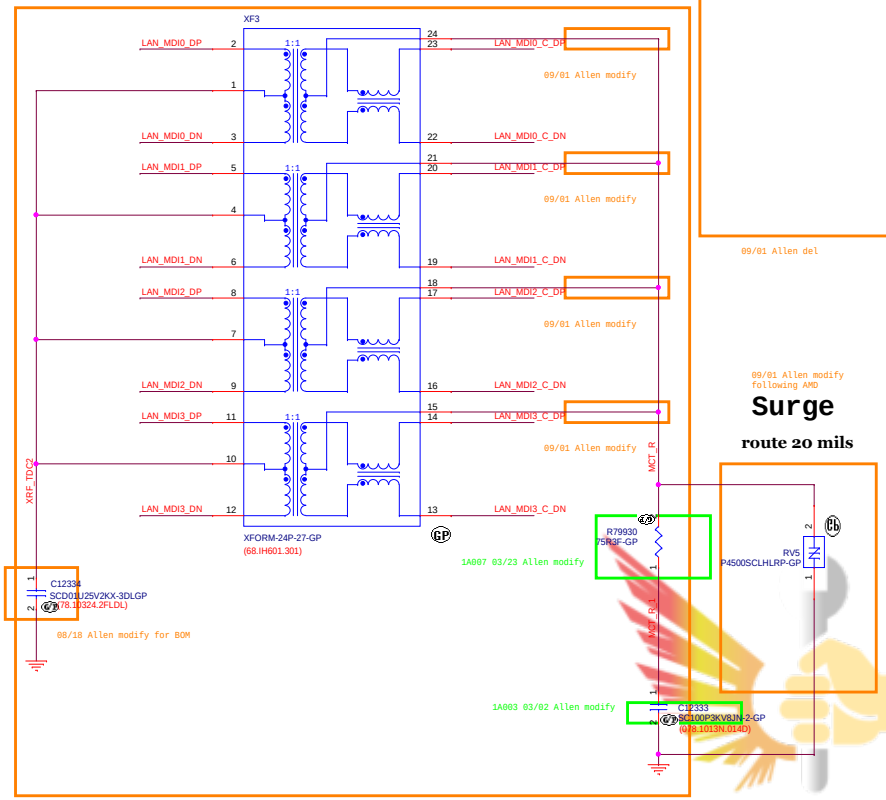
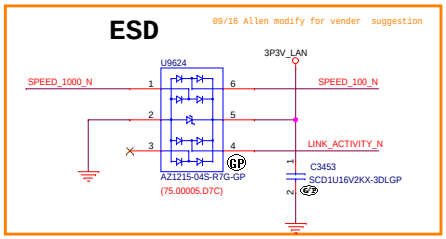
0702 Eric modify from Dogfish

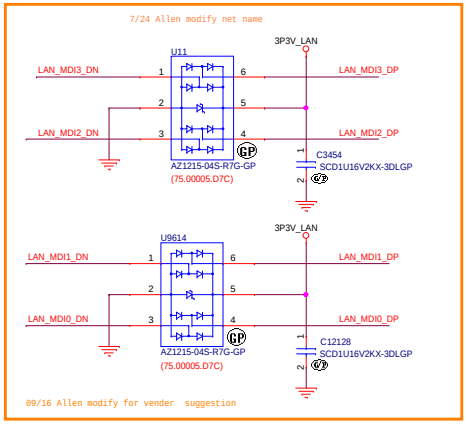


Transformer



ESD





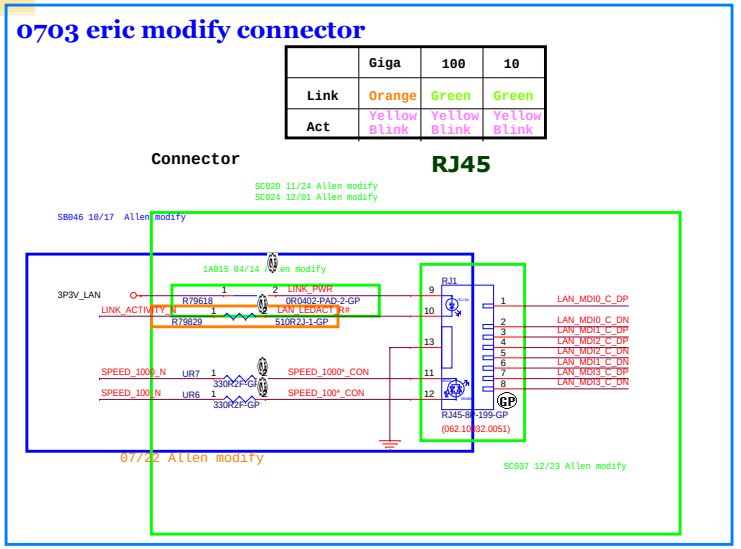
Transformer

0703 eric modify connector

	Giga	100	10
Link	Orange	Green	Green
Act	Yellow Blink	Yellow Blink	Yellow Blink

Connector

RJ45



<Variant Name>

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Title: 032_RJ45+TRANSFORMER

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VCC3 → VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,38,41,42,44,47,48,50,53,55,56,58,59,61,62,64,67,68,86,99

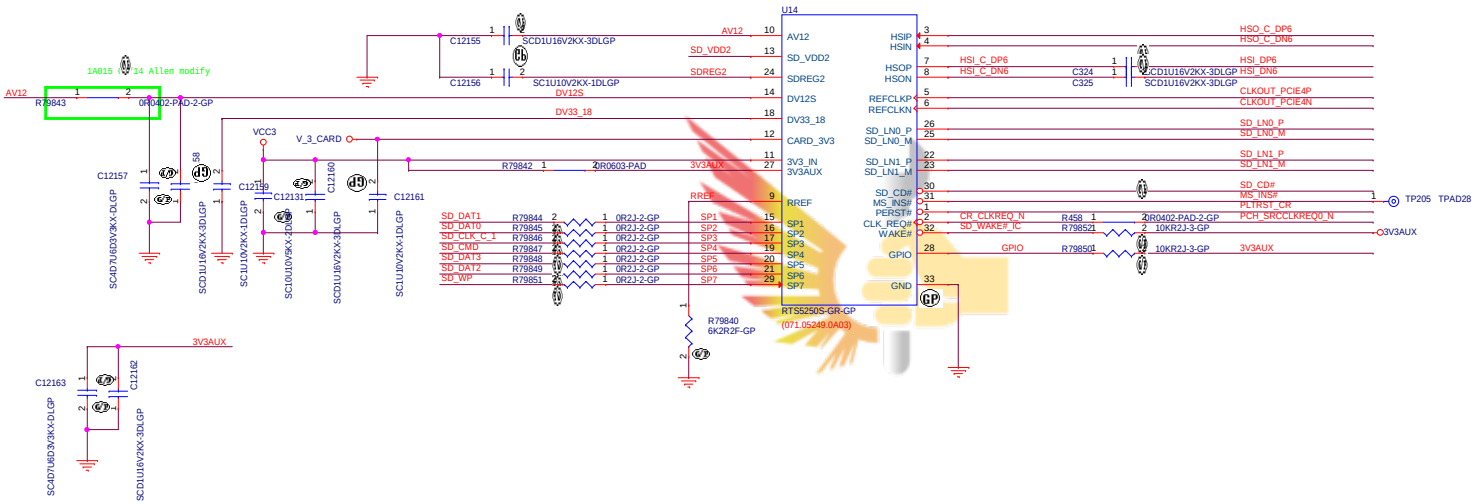
Card Reader

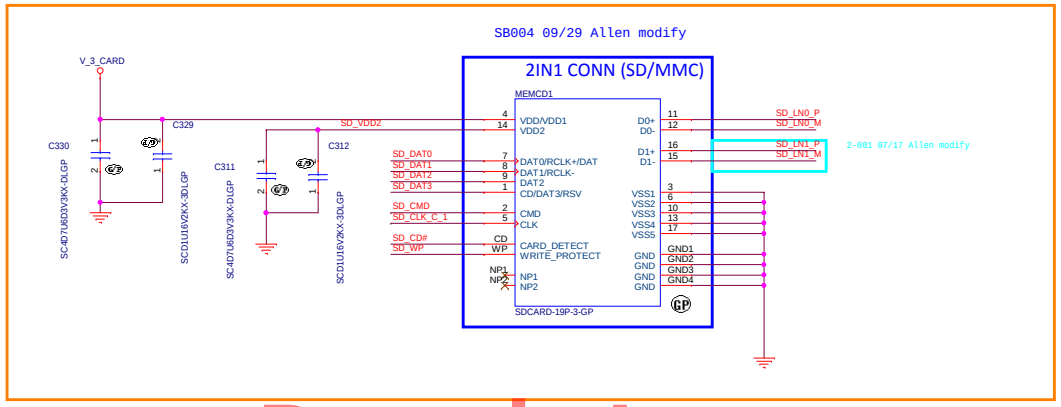
17 HSI_DN6
17 HSI_DP6
17 HSO_C_DN6
17 HSO_C_DP6

16 PCH_SRCCLKREQ0_N
24 PLTRST_CR

16 CLKOUT_PCIE4N
16 CLKOUT_PCIE4P

15 SD_WAKE#_IC





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Title: 033_READER CONN

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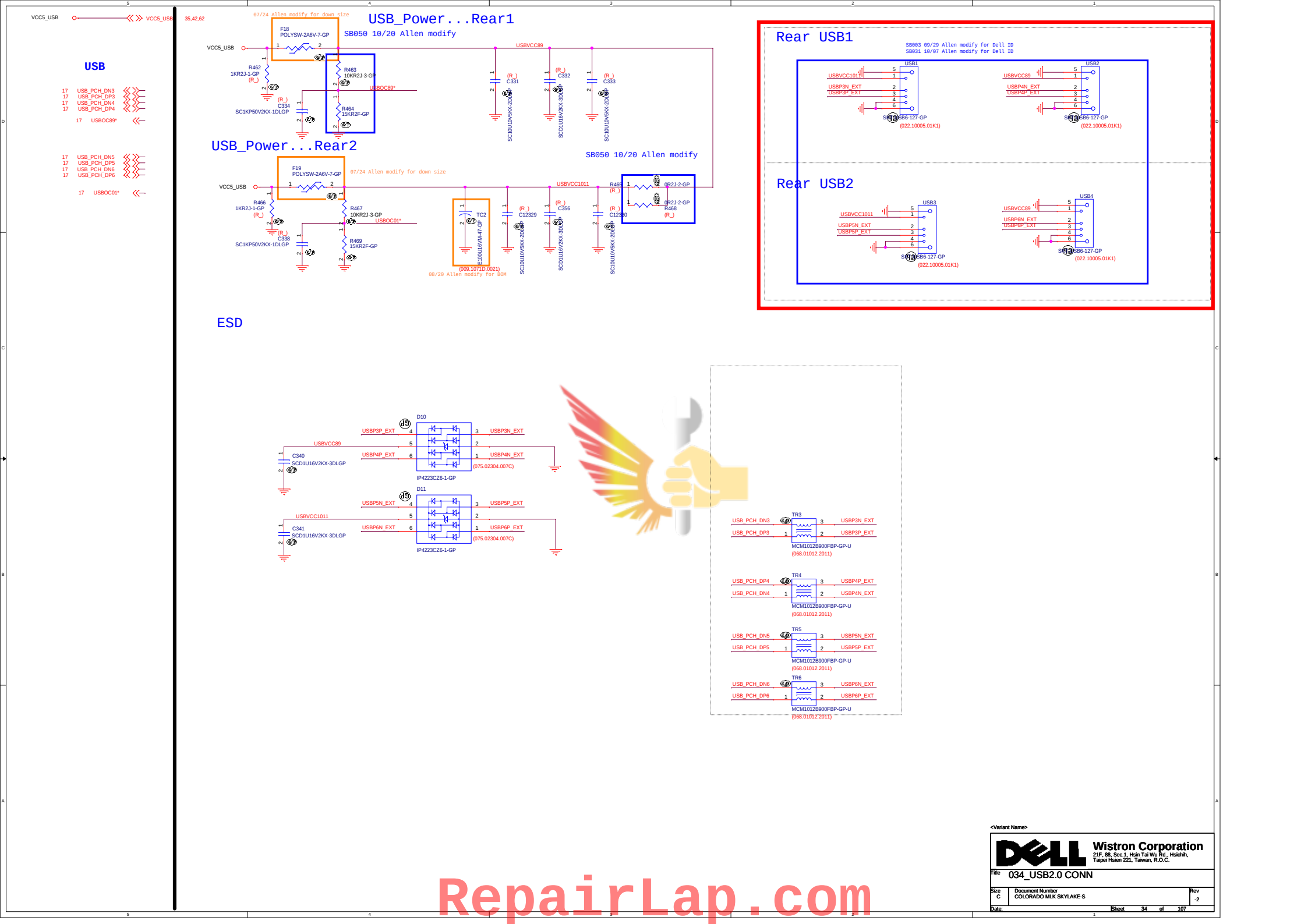

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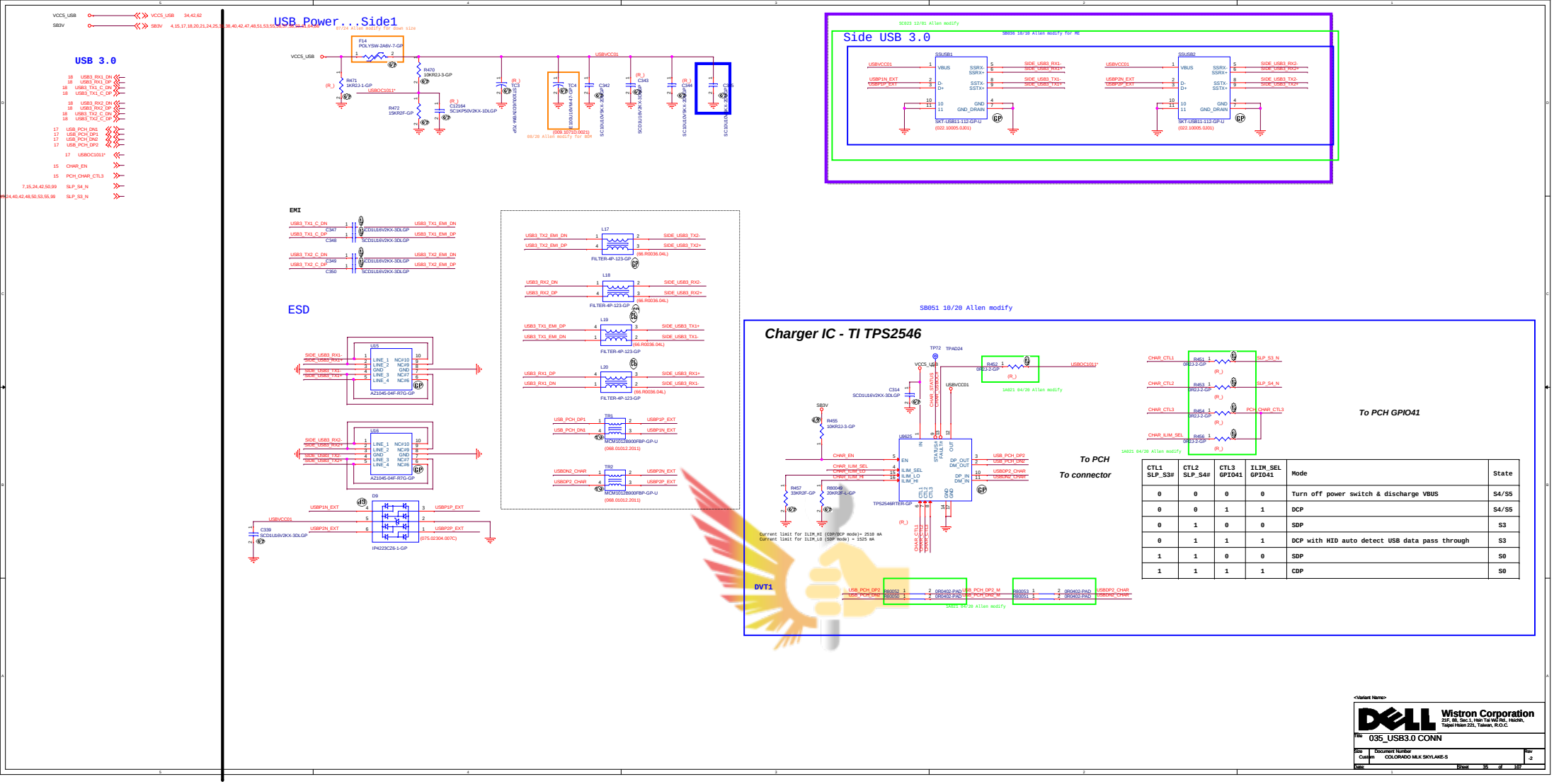

CTL1 SLP_S3#	CTL2 SLP_S4#	CTL3 GPIO41	ILIM_SEL GPIO41	Mode	State
0	0	0	0	Turn off power switch & discharge VBUS	S4/S5
0	0	1	1	DCP	S4/S5
0	1	0	0	SDP	S3
0	1	1	1	DCP with HID auto detect USB data pass through	S3
1	1	0	0	SDP	S0
1	1	1	1	CDP	S0

<Variant Name>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 035_USB3.0 CONN

Size: Custom | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

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RepairLap.com

<Variant Name>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Size A4	Document Number COLORADO MLK SKYLAKE-S	Rev -2
Date:	Sheet 36 of 107	

RepairLap.com

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
Custom	COLORADO MLK SKYLAKE-S	-2

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SB3V — SB3V — 4,15,17,18,20,21,24,25,31,35,40,42,47,48,51,53,55,56,57,58,59,61,64,86

VCC3 — VCC3 — 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,41,42,44,47,48,50,53,55,56,58,59,61,62,64,67,68,86,99

WEBCAM

17 USB_PCH_DN9
17 USB_PCH_DP9

27 AUD_DMIC_CLK
27 AUD_DMIC_DATA

24 WEBCAM_DET

WEBCAM

07/24 Allen modify for down size

TR7
USB_PCH_DP9 — 1 — 2 — USB_PCH_DP9_PP
USB_PCH_DN9 — 4 — 3 — USB_PCH_DN9_NN
MCM1012B900FBP-GP-U
(068.01012.2011)

VCC3 — F20 POLYSW-1D5A6V-12-GP — VCC3_CAM
R473 0R3J-0-U-GP (R_)
SB3V
R474 0R3J-0-U-GP (R_)
F6 POLYSW-1D5A6V-12-GP (R_)
C351 SC10U10V5KX-2DL
C352 SC10U10V5KX-2DL
C353 SCD1U16V2KX-3DLGP

FOR EMI

WEBCAM_DET
(R_) PC2 SC22P50V2JN-4DLGP

07/29 Allen modify for down size

VCC3
R475 10KR2J-3-GP
VCC3_CAM
WEBCAM_DET

WEBCM1
USB_PCH_DP9_PP
USB_PCH_DN9_NN
AUD_DMIC_CLK
AUD_DMIC_DATA
JWT-CON8-4-GP
(020.F0100.0008)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 038_WEBCAM

Size: C | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 38 of 107

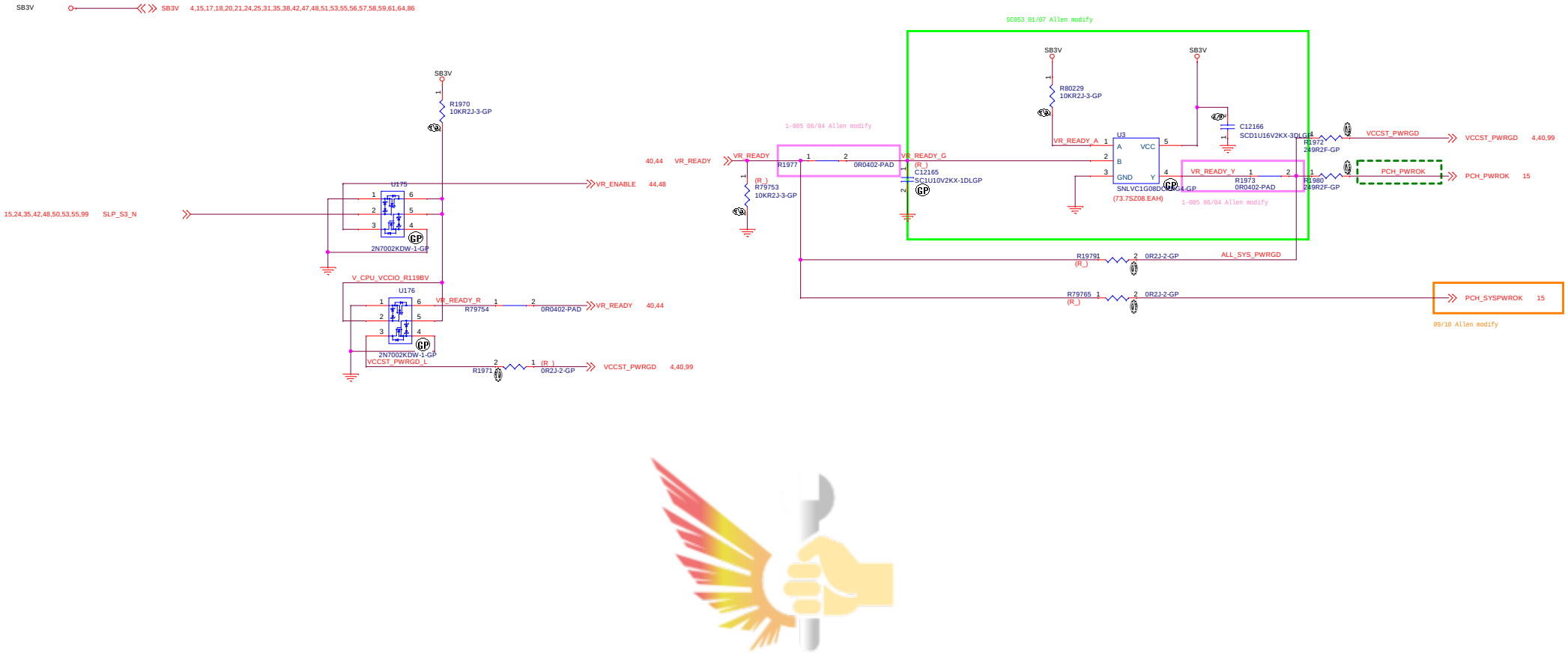
RepairLap.com

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Size: A	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
Date:	Sheet 39 of 107	

RepairLap.com



RepairLap.com

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 040_Power enable & sequence

Size: Custom | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

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VCC
VCC3

VCC 15,24,26,27,42,44,45,46,55,56,57,58,60,64,67,68,86,88

VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,42,44,47,48,50,53,55,56,58,59,61,62,64,67,68,86,99

For layout top and bottom the same

U33 R981 R982 R983

R1718

SC020 11/24 Allen modify

Adaptor in to generate DCBATOUT

DC in

DCIN1

DC-JACK345-GP

(022.10015.0361)

AD_JK

C355 SCD1U50V3KX-DL-GP

D12 PESMB27A-1-GP (83.PESMB.HAG)

SCD01U50V2ZY-1GP

C12328

U17 U18 AO4407AL-GP

DC_19V

R484 10KR5J-L-GP

C356

R486 56KR2F-GP

R485 10KR3J-L1-GP

C357 SCD1U50V3KX-DL-GP

11A,11mohm <14mohm
Vgs=-20 , 14mohm <18
mohm Vgs=-10

Jeffrey 0617

JACK_PSID

L21 BLM15BD102SN1D-GP

PSID_D

PSID_G

Q24 2N7002A-7-GP (84.05067.031)

ADAPTOR_PSID_R

R495 33R2J-2-GP

D13 BAV99GP-GP (75.00099.07D)

VCC3

R492 1K5R2J-3-GP

ADAPTOR_PSID_SIO

BIOS GPIO

VCC

R499 10KR2J-3-GP

R501 100KR2J-1-GP

PSID_D_1

Q26 MMBT3904-4-GP (84.T3904.H11)

R503 15KR2F-GP

<Variant Name>

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 041_DCIN

Size	Document Number	Rev
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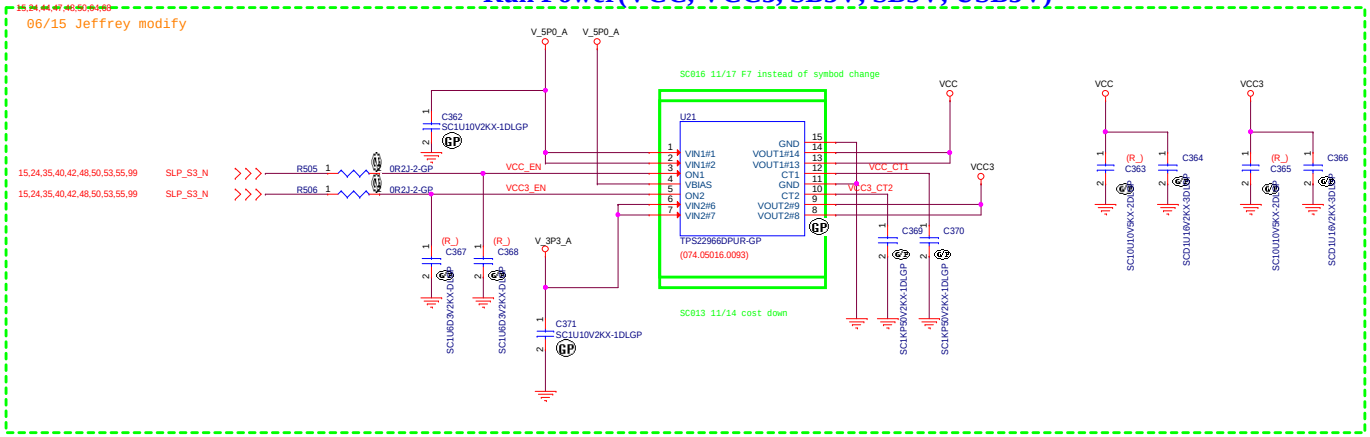
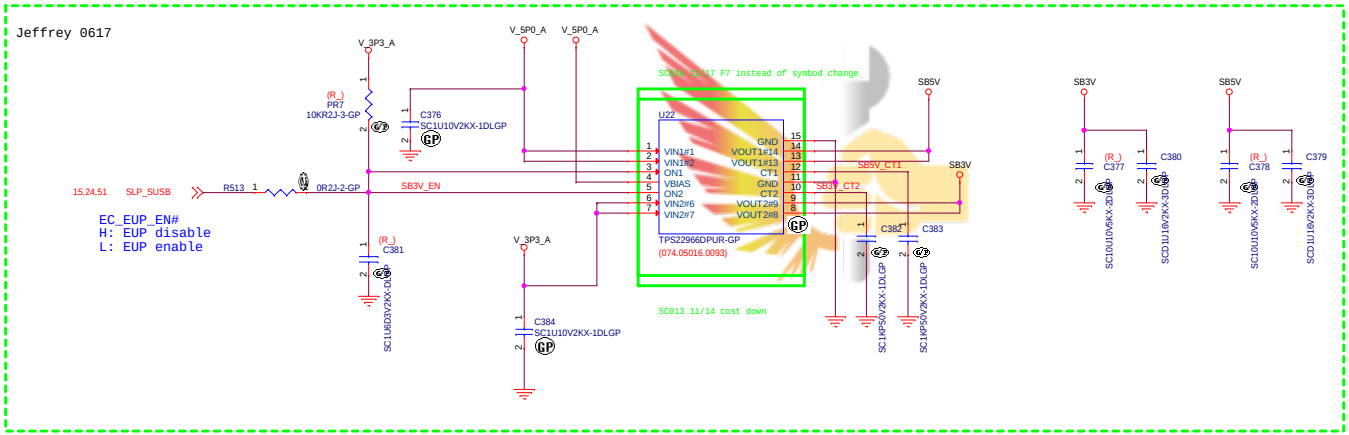
RepairLap.com

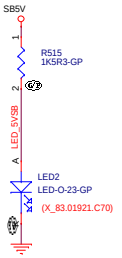
DCBATOUT — DCBATOUT 7,24,26,28,43,45,46,47,48,49,50,51,53,55,58,59,86,88
V_3P3_A — V_3P3_A 15,21,24,25,28,29,43,49,64,99
V_5P0_A — V_5P0_A 15,27,49,51
VCC — VCC 15,24,26,27,41,44,45,46,55,56,57,58,60,64,67,68,86,88
VCC3 — VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,41,44,47,48,50,53,55,56,58,59,61,62,64,67,68,86,99
VCC5_USB — VCC5_USB 34,35,62
SB3V — SB3V 4,15,17,18,20,21,24,25,31,35,38,40,47,48,51,53,55,56,57,58,59,61,64,86
SB5V — SB5V 15,24,44,47,48,50,51,65

Run Power(VCC, VCC3, SB3V, SB5V, USB5V)

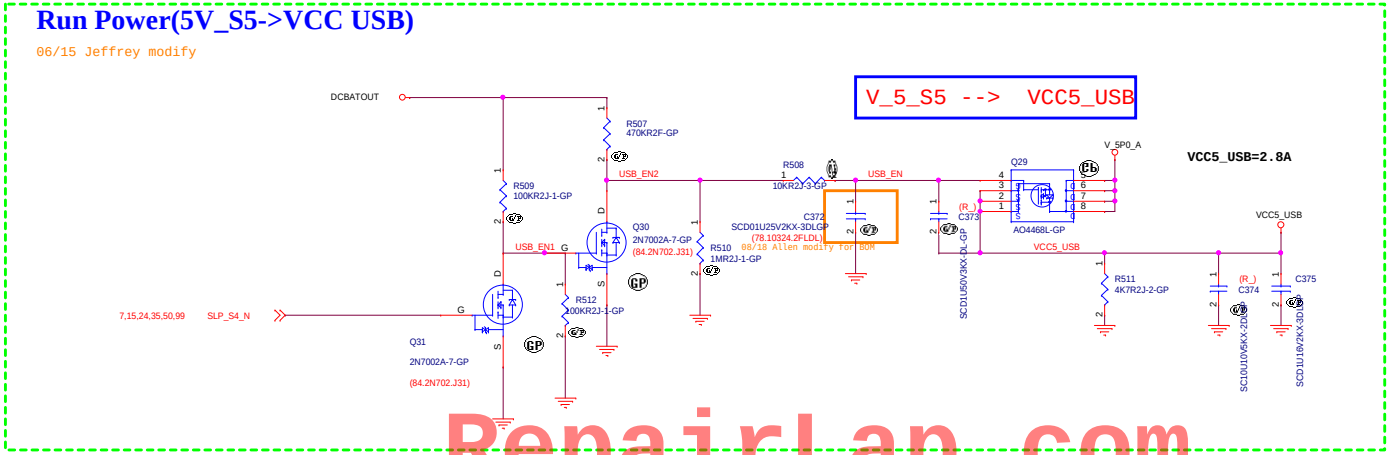




VCC5SB LED



Run Power(5V_S5->VCC USB)



RepairLap.com

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 042_Run PWR/USB/DSWPWR

Size: C | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

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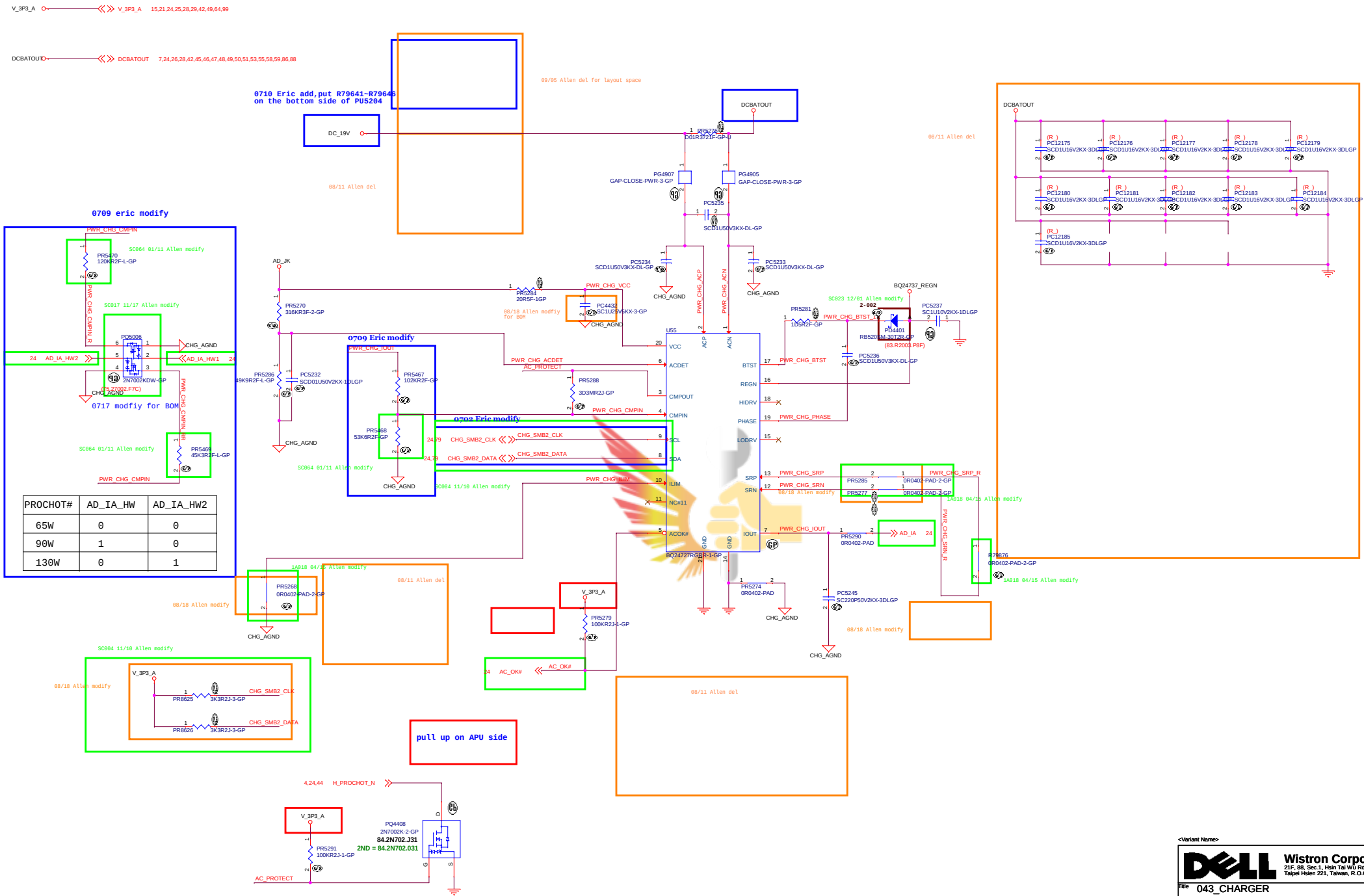
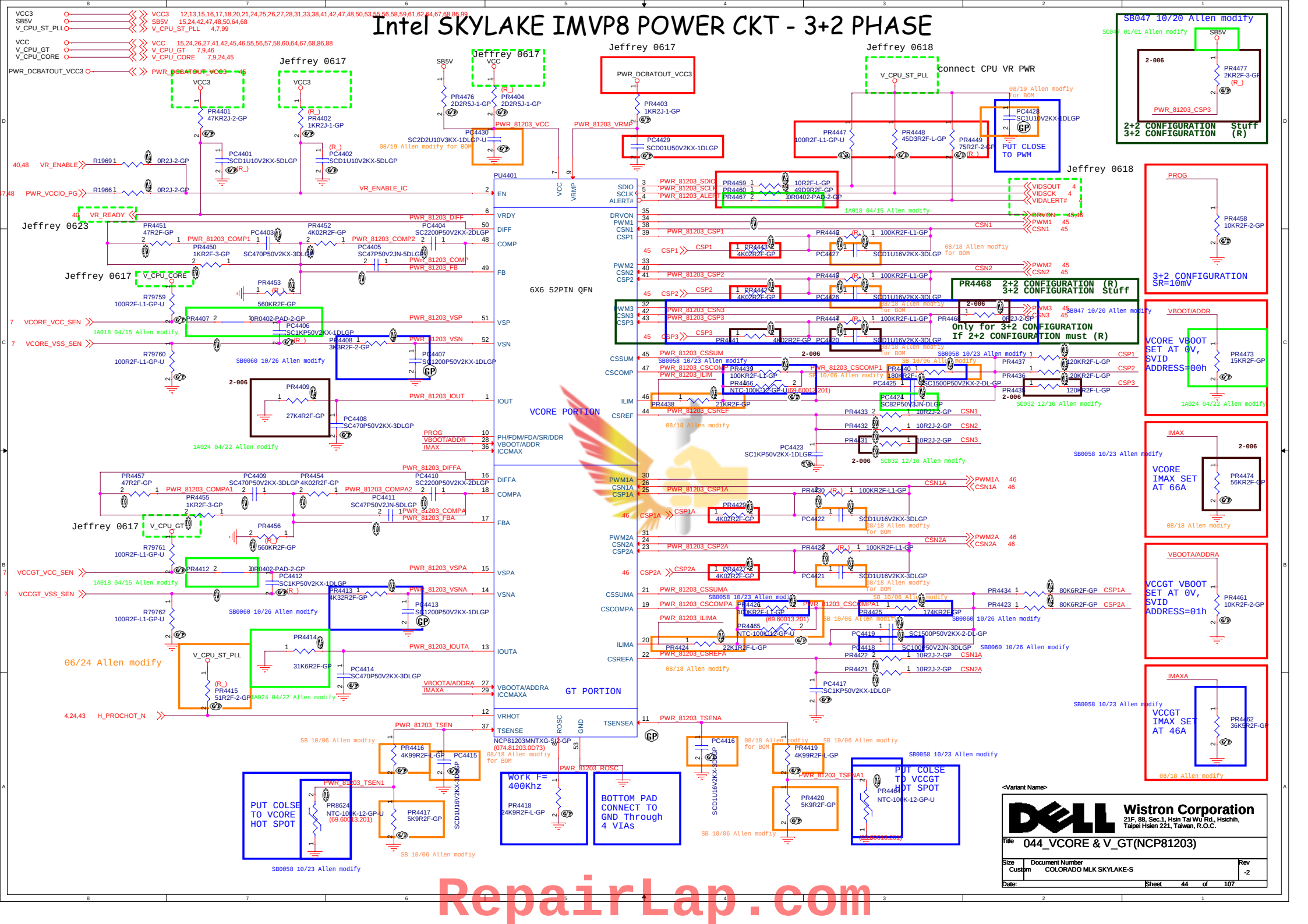


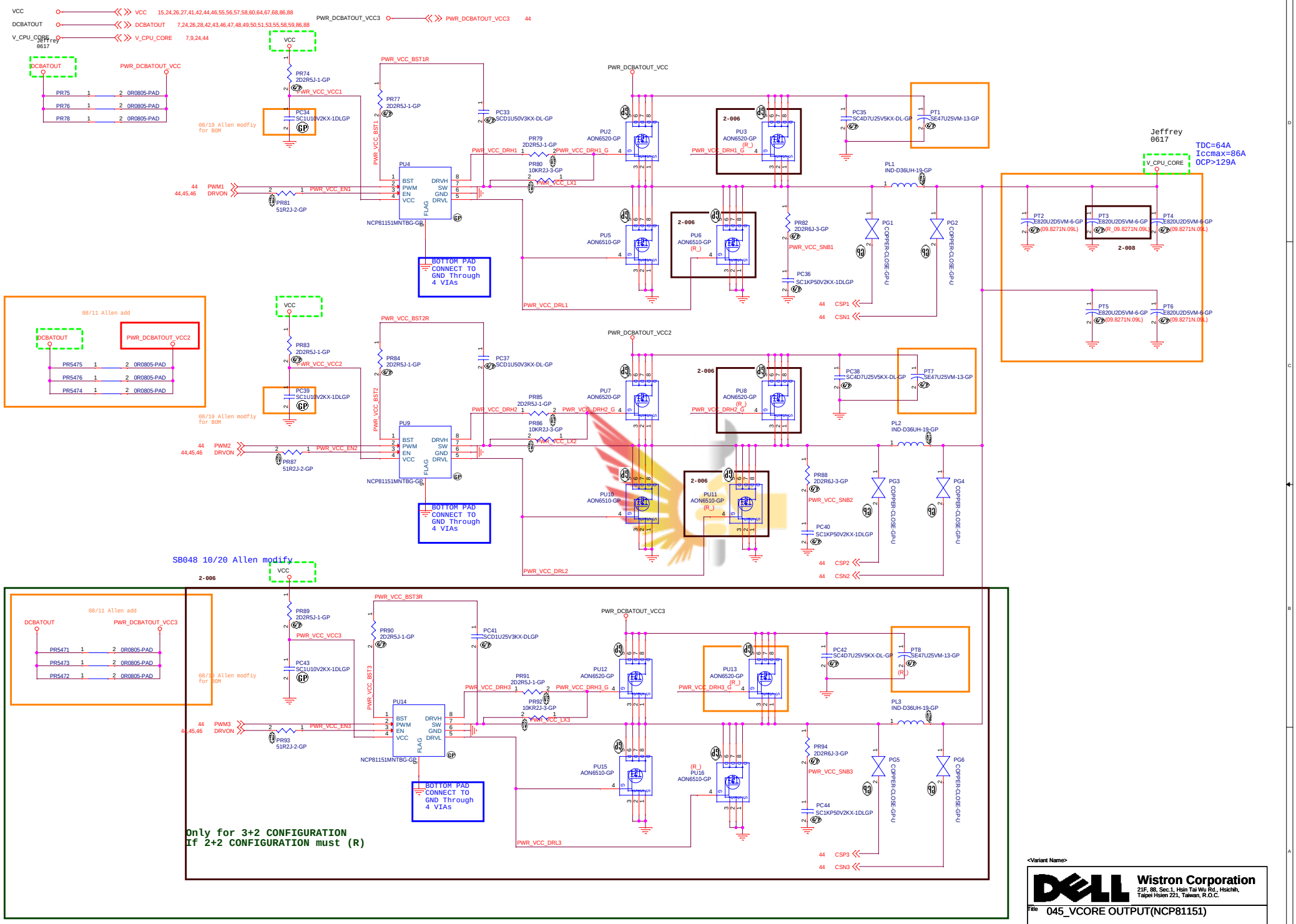
RepairLap.com

<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title 043_CHARGER
Size Custom
Document Number COLORADO MLK SKYLAKE-S
Rev -2
Date:
Sheet 43 of 107

Intel SKYLAKE IMVP8 POWER CKT - 3+2 PHASE



RepairLap.com



RepairLap.com

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 045_VCORE OUTPUT(NCP81151)

Size	Document Number	Rev
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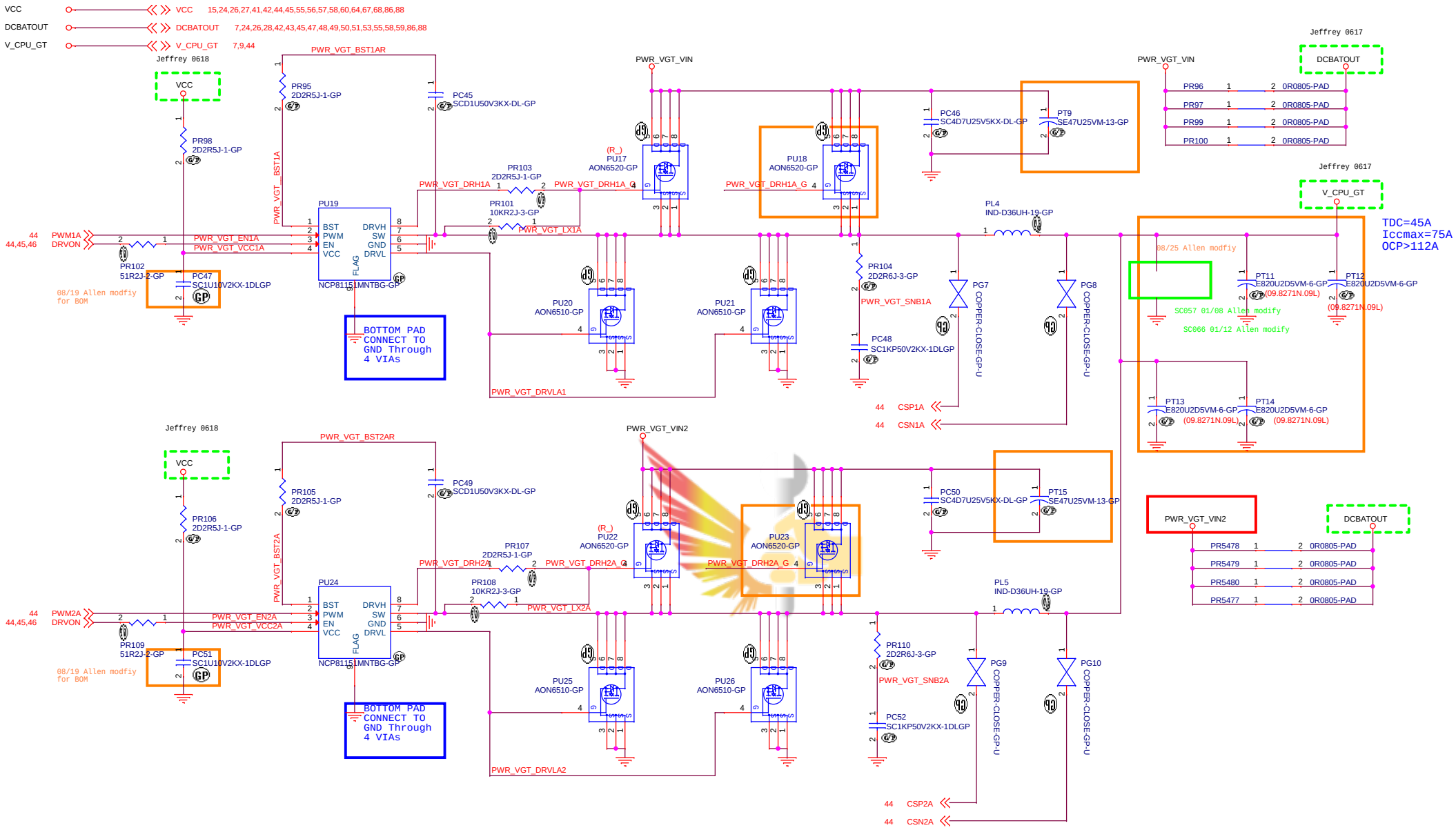


<Variant Name>

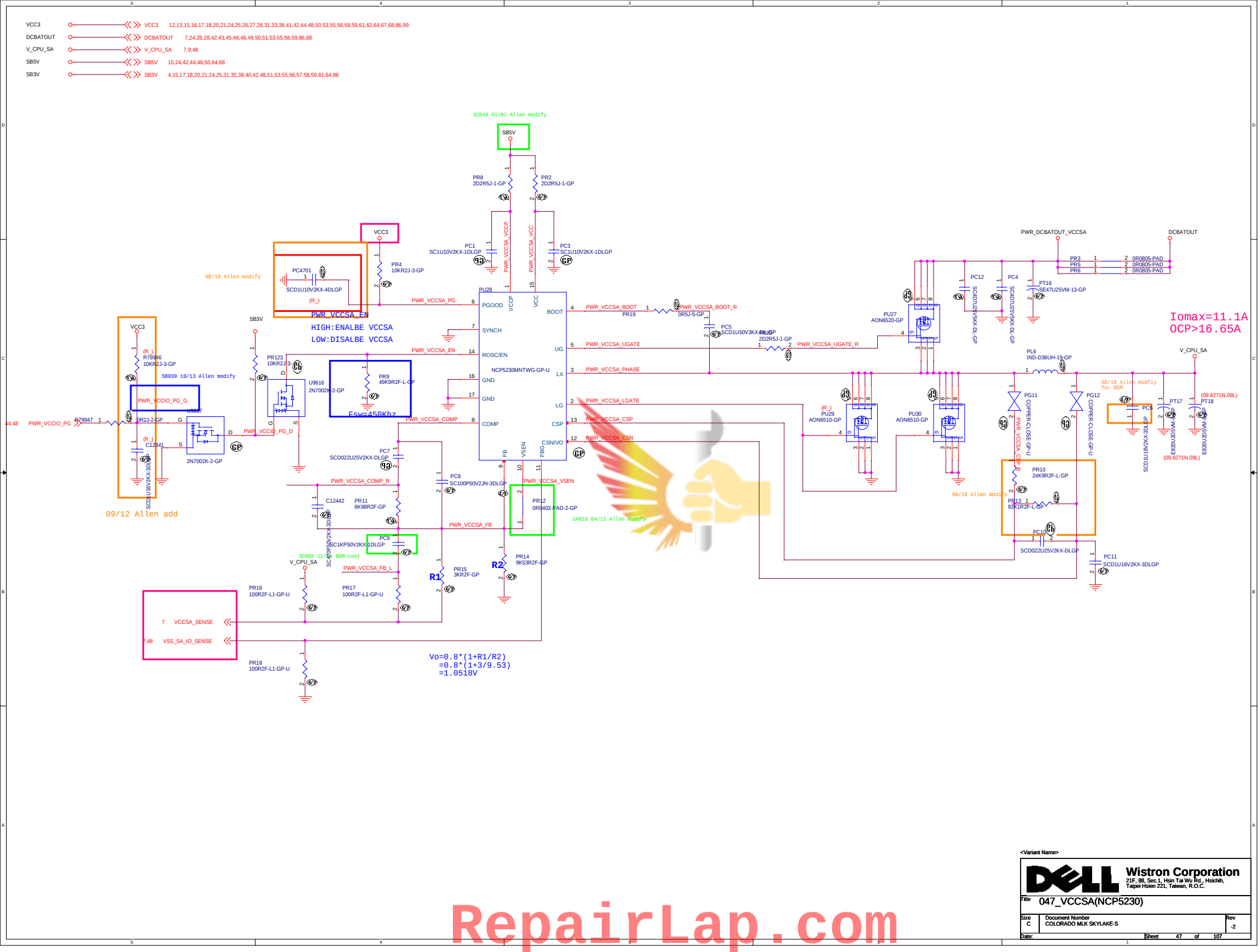
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: 046_V_GT OUTPUT(NCP81151)

Size: Custom | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 46 of 107

RepairLap.com



RepairLap.com

VCC3 VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,41,42,44,47,50,53,55,56,58,59,61,62,64,67,68,86,99

DCBATOUT DCBATOUT 7,24,26,28,42,43,45,46,47,49,50,51,53,55,58,59,86,88

V_CPU_IO V_CPU_IO 4,5,7,8,9,99

SB5V SB5V 15,24,42,44,47,50,64,68

SB3V SB3V 4,15,17,18,20,21,24,25,31,35,38,40,42,47,51,53,55,56,57,58,59,61,64,86

V_CPU_SA V_CPU_SA 7,9,47

Jeffrey 0617

VCC3

PR135 10KR2J-3-GP

44,47 PWR_VCCIO_PG

PWR_VCCIO_PG

PC4431 SC1KP50V2KX-1DLGP

PR136 75KR2F-GP

PWR_VCCIO_CS

PWR_VCCIO_EN

PWR_VCCIO_FB

PWR_VCCIO_RF

PC64 SC1KP50V2KX-1DLGP

PR143 470KR2F-GP

PU32

PGOOD CS EN FB RF GND BOOT UGATE PHASE VCC LGATE

RT8237CZQW-2-GP

PWR_VCCIO_BOOT

PWR_VCCIO_UGATE

PWR_VCCIO_PHASE

PWR_VCCIO_LGATE

PR139 2D2R3-1-U-GP

PWR_VCCIO_BOOT_R

PC62 SCD1U50V2KX-DL-GP

SB5V

PC63 SC1U10V2KX-1DLGP

SC043 01/01 Allen modify

Jeffrey 0617

PU31 AON7410-GP

PU33 AON7506-GP

PR145 2D2R5J-1-GP

PWR_VCCIO_SW

08/11 Allen modify

PC65 SC1KP50V2KX-1DLGP

PWR_DCBATOUT_VCCIO

PR133 0R0805-PAD

PR134 0R0805-PAD

PC61 SC4D7U25V5KX-DL-GP

PC117 SC4D7U25V5KX-DL-GP

PL7 IND-1D5UH-53-GP

Iomaax=5.4A
OCP>8.1A

PWR_VCCIO

PR4801 100R2F-L1-GP-U

PC66 SCD1U16V2KX-3DLGP

PT20 EB20U2D5VM-GP

(09.8271N.09L)

08/18 Allen modify for BOM

Jeffrey 0617

DCBATOUT

Jeffrey 0617

V_CPU_IO

PWR_VCCIO

PR137 0R0805-PAD

PR138 0R0805-PAD

PR140 0R0805-PAD

PR141 0R0805-PAD

PR142 0R0805-PAD

PR144 0R0805-PAD

PWR_VCCIO

V_CPU_SA

R1985 0R6J-L-GP

R1986 0R6J-L-GP

07/07 Allen Add

SC052 1/7 Allen modify

VCC3 VCC3 SB3V

R1961 10KR2J-3-GP

R1964 10KR2J-3-GP

R1963 100KR2J-1-GP

PWR_VCCIO_EN_R

R1968 0R2J-2-GP PWR_VCCIO_EN

R1967 0R2J-2-GP VR_ENABLE

VR_ENABLE 40,44

U173

PWR_VCCIO_EN_G1

PWR_VCCIO_EN_G2

2N7002KDW-1-GP

C12055 SCD1U16V2KX-3DLGP

08/18 Allen modfiy for BOM

SC052 1/7 Allen modify

15,24,35,40,42,50,53,55,99 SLP_S3_N

R80228 2KR2F-3-GP PWR_VCCIO_EN_G1

1A006 03/20 Allen modify

Vout = 0.704*(1+R1/R2)
= 0.704*(1+11.8/33)
= 0.9557V

PWR_VCCIO_FB_R

PR4802 0R0402-PAD-2-GP VCCIO_SENSE

VCCIO_SENSE 7

1A018 04/15 Allen modify

07/08 Power modify

PR146 11K8R2F-GP R1

PC67 SC18P50V2JN-1DLGP

PWR_VCCIO_FB

PR147 33KR2F-GP R2

08/11 Allen modify

PR4803 0R0402-PAD-2-GP VSS_SA_IO_SENSE

VSS_SA_IO_SENSE 7,47

1A018 04/15 Allen modify

07/08 Power modify

R79948 100R2F-L1-GP-U

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title 048_VCCIO(RT8237)

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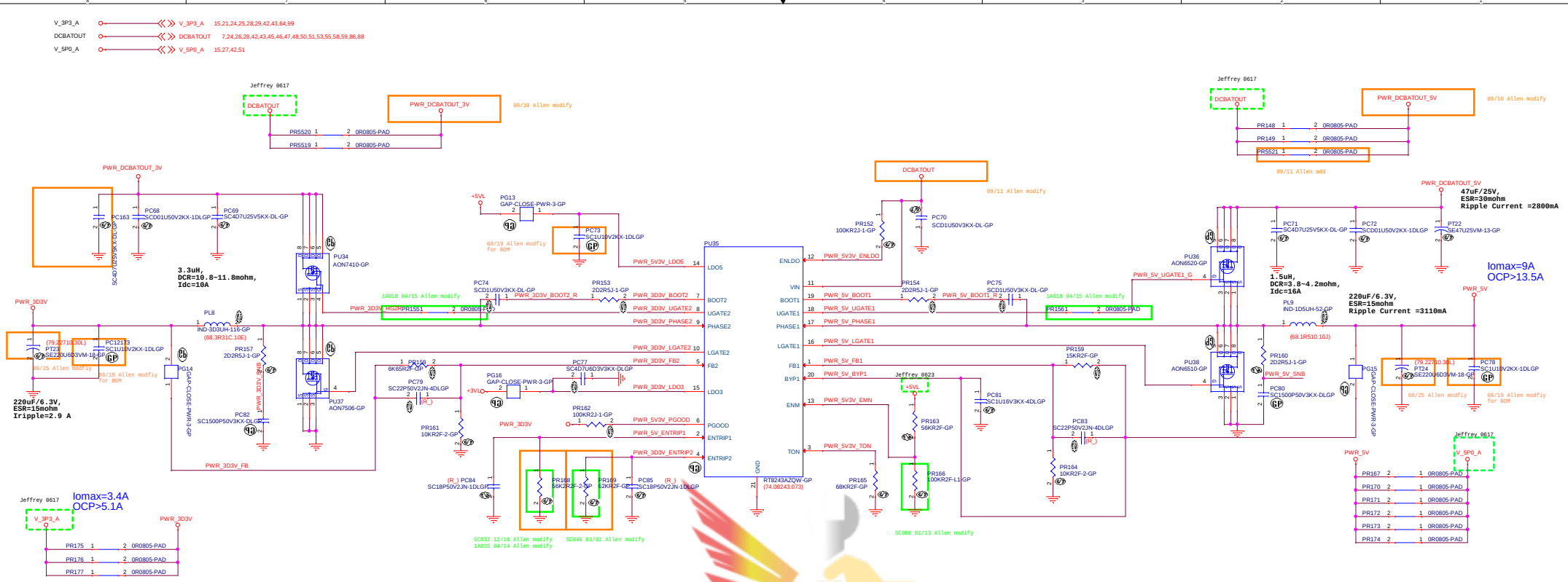
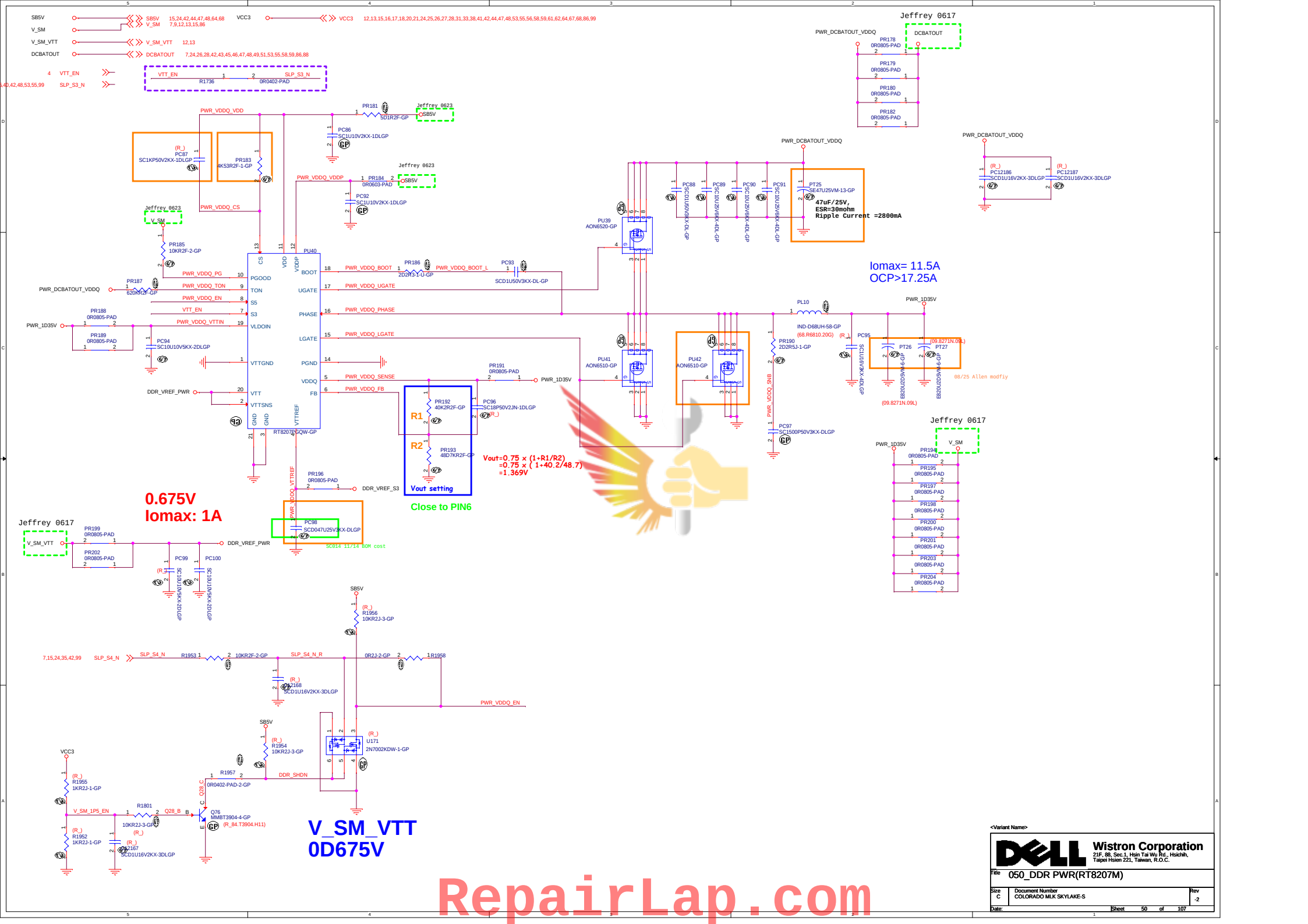


Table 2. Power Up Sequencing(RT8243A)

ENLDO(V)	SECFB	ENTRIP1	ENTRIP2	LDO5(V)	LDO3(V)	SMPS1	SMPS2
LOW	LOW	X	X	Off	Off	Off	Off
>1.6V =>High	LOW	X	X	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	Off	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	On	On	On	Off	On
>1.6V =>High	>2.3V =>High	On=>PD	On=>PD	On	On	On	On
>1.6V =>High	>2.3V =>High	On	Off	On	On	On	On

RepairLap.com



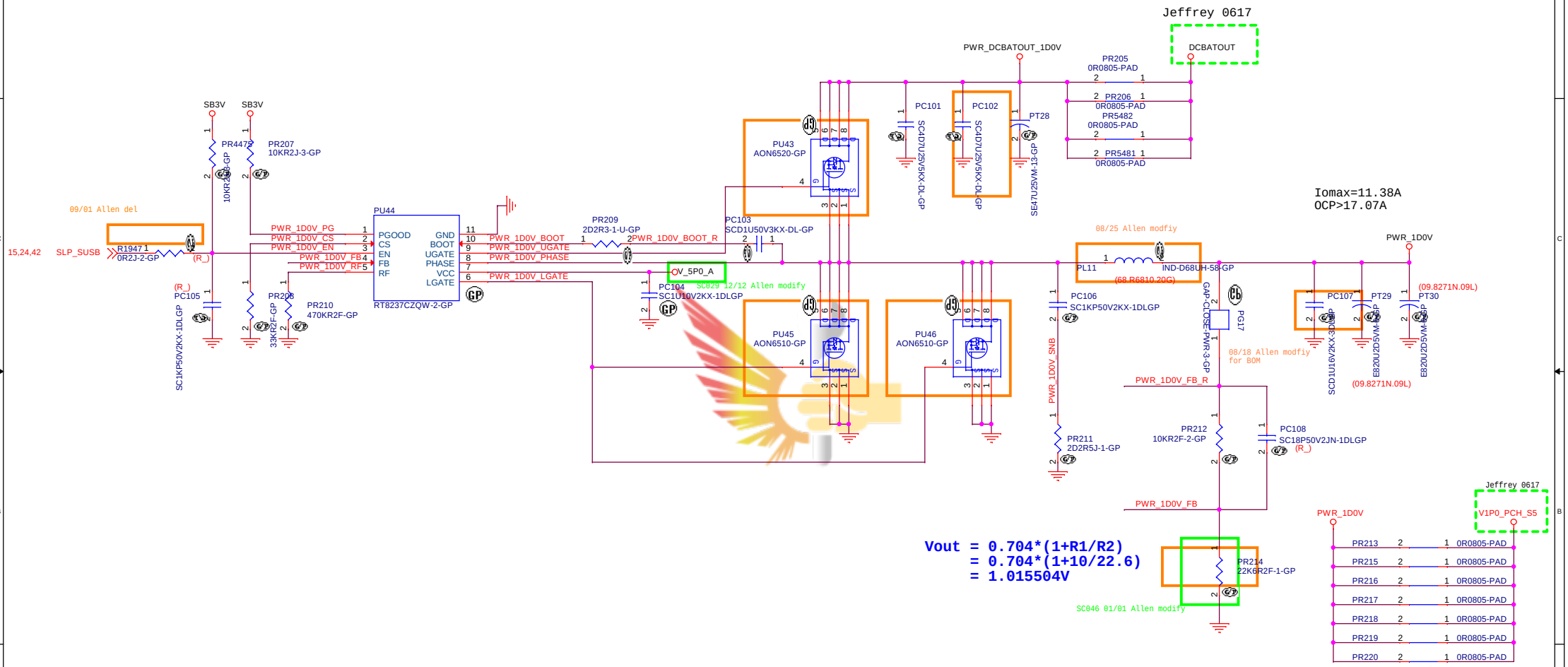
RepairLap.com

SB3V SB3V 4,15,17,18,20,21,24,25,31,35,38,40,42,47,48,53,55,56,57,58,59,61,64,86

DCBATOUT DCBATOUT 7,24,26,28,42,43,45,46,47,48,49,50,53,55,58,59,86,88

V1P0_PCH_S5 V1P0_PCH_S5 7,15,21,99

V_5P0_A V_5P0_A 15,27,42,49



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 051_PCH 1D0V(RT8237)

Size: A3 | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

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RepairLap.com

08/27 Allen del

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A3	COLORADO MLK SKYLAKE-S	-2

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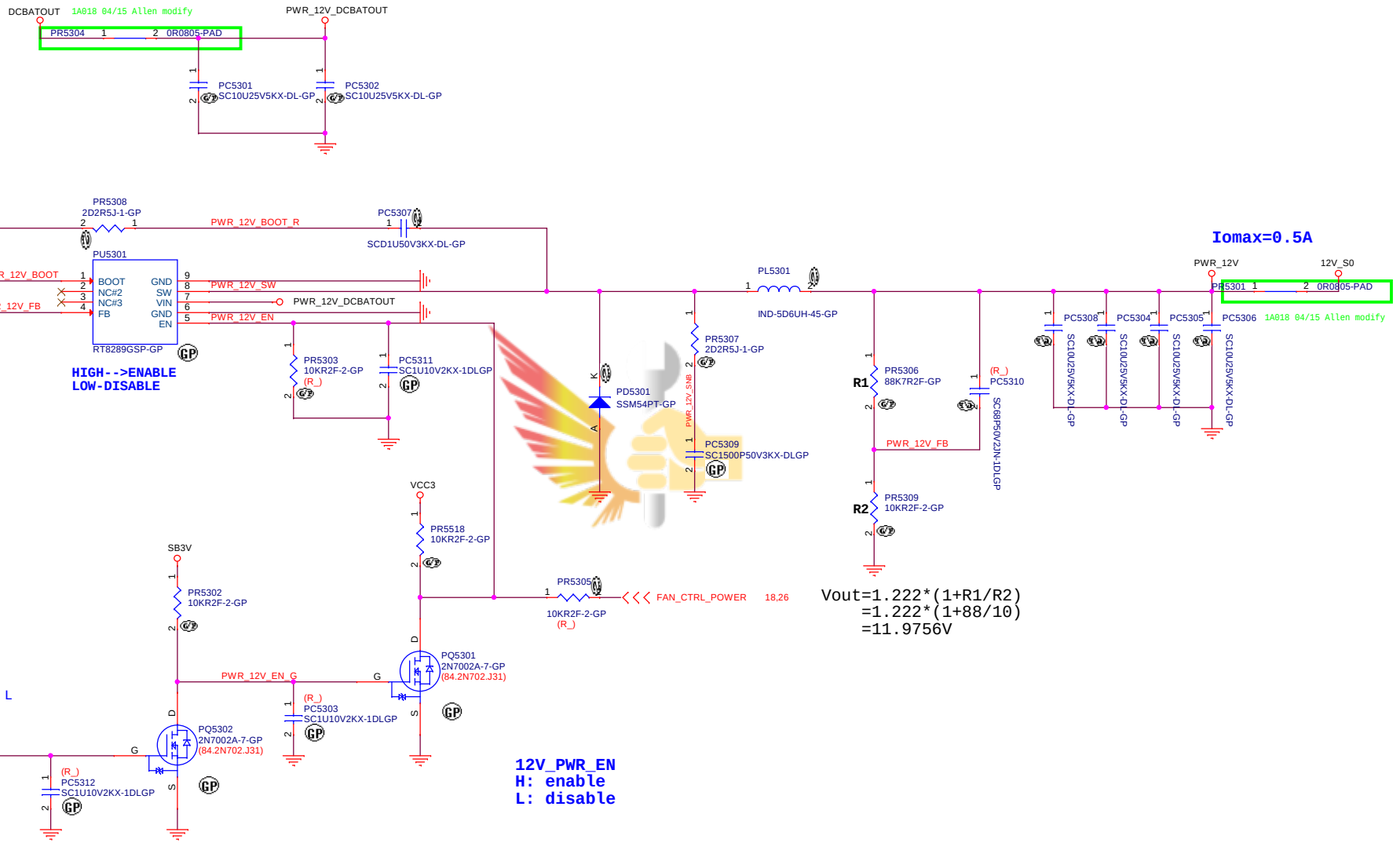
RepairLap.com

DCBATOUT
12V_S0

DCBATOUT 7,24,26,28,42,43,45,46,47,48,49,50,51,55,58,59,86,88
12V_S0 26

VCC3
SB3V

VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,41,42,44,47,48,50,55,56,58,59,61,62,64,67,68,86,99
SB3V 4,15,17,18,20,21,24,25,31,35,38,40,42,47,48,51,55,56,57,58,59,61,64,86



En Threshold	Logic Low Voltage	V_{IL}		--	--	0.4	V
	Logic High Voltage	V_{IH}		1.4	--	5.5	V

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title 053_12V(RT8289)

Size A3 | Document Number COLORADO MLK SKYLAKE-S | Rev -2

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RepairLap.com

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
Custom	COLORADO MLK SKYLAKE-S	-2

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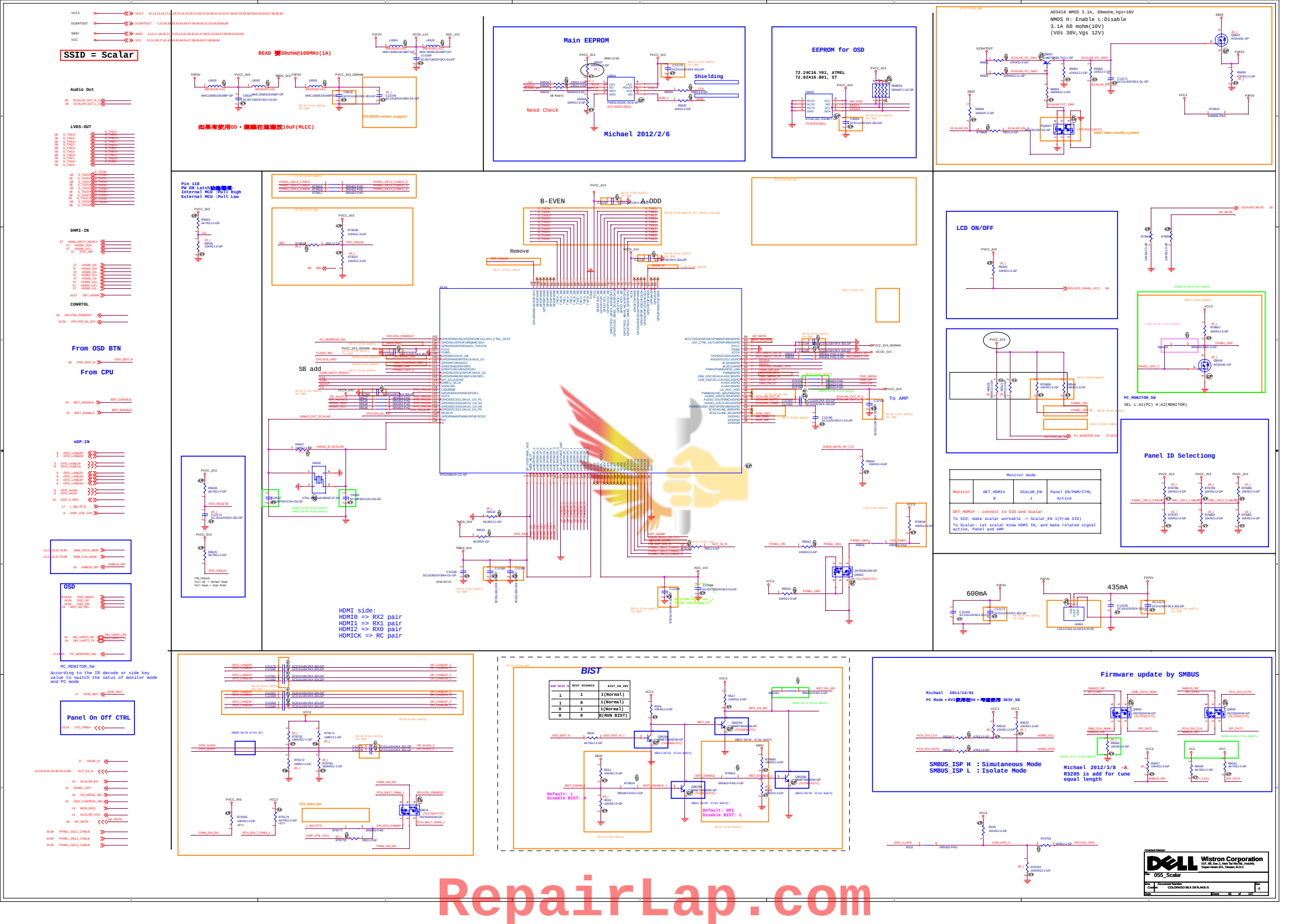
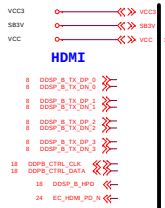
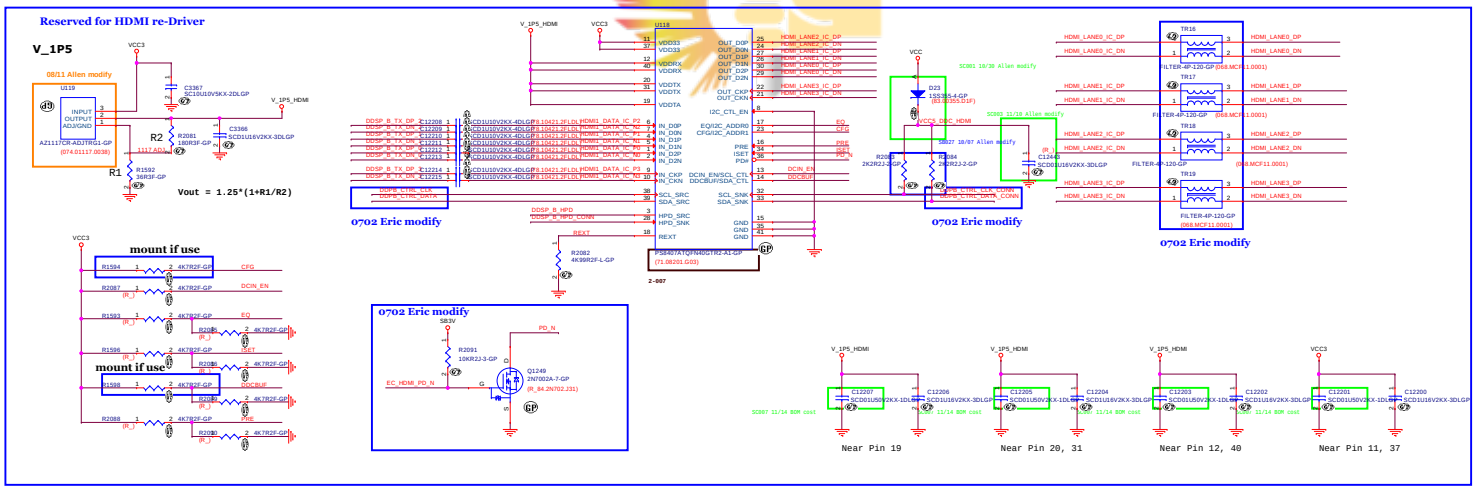
RepairLap.com

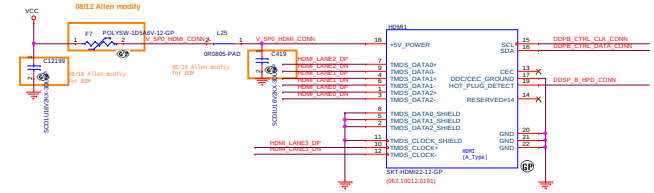


RepairLap.com

HDMI

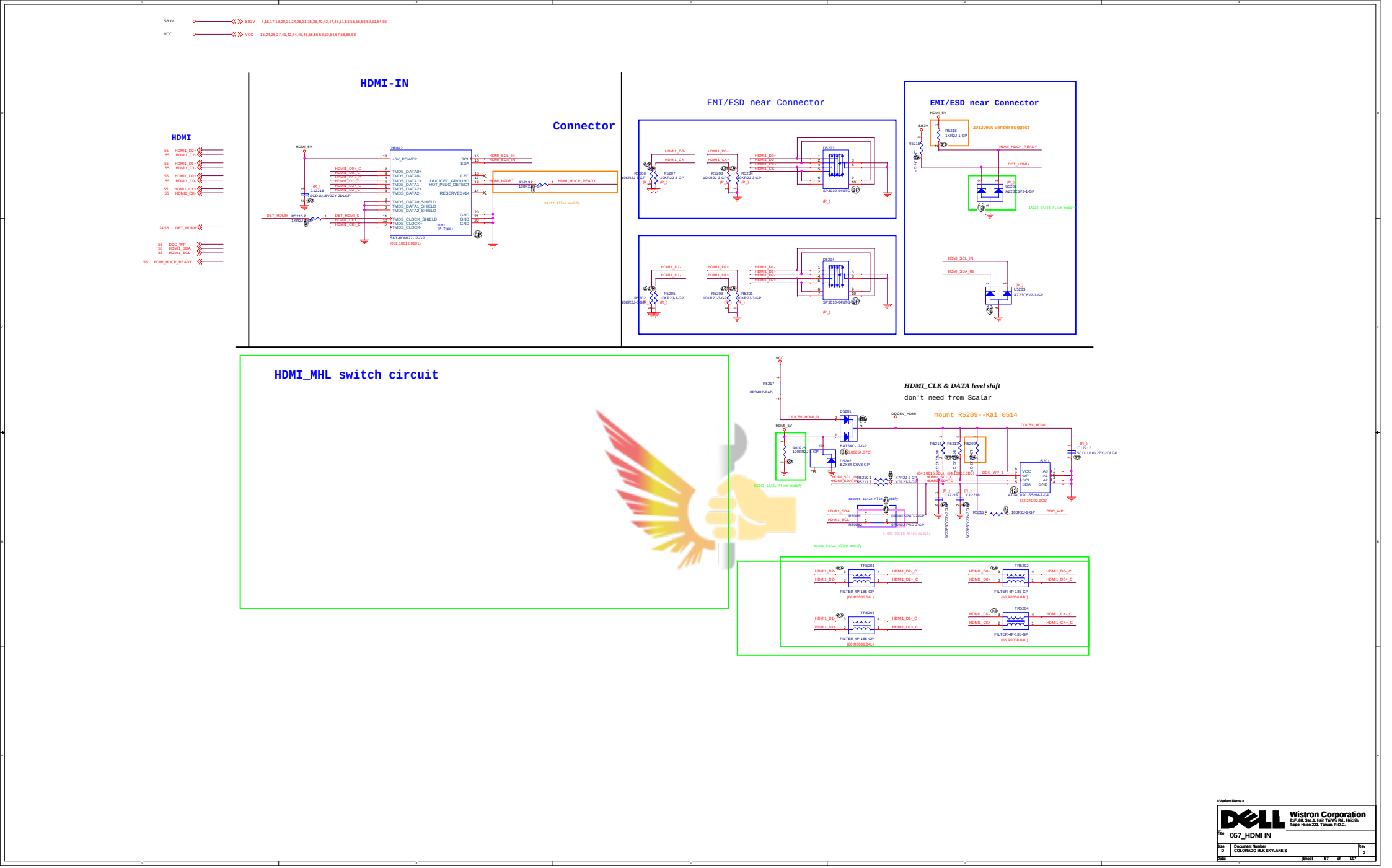






ESD

RepairLap.com



RepairLap.com

SB3V — SB3V 4,15,17,18,20,21,24,25,31,35,38,40,42,47,48,51,53,55,56,57,59,61,64,86

VCC — VCC 15,24,26,27,41,42,43,45,46,55,56,57,60,64,67,68,86,88

VCC3 — VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,41,42,44,47,48,50,53,55,56,59,61,62,64,67,68,86,99

DCBATOUT — DCBATOUT 7,24,26,28,43,45,46,47,48,49,50,51,53,55,59,86,88

From RTD2136S to LVDS

55 S_TXE3+ — S_TXE3+
55 S_TXE3- — S_TXE3-
55 S_TXEC+ — S_TXEC+
55 S_TXEC- — S_TXEC-
55 S_TXE2+ — S_TXE2+
55 S_TXE2- — S_TXE2-
55 S_TXE1+ — S_TXE1+
55 S_TXE1- — S_TXE1-
55 S_TXE0+ — S_TXE0+
55 S_TXE0- — S_TXE0-

55 S_TXO0- — S_TXO0-
55 S_TXO0+ — S_TXO0+
55 S_TXO1- — S_TXO1-
55 S_TXO1+ — S_TXO1+
55 S_TXO2- — S_TXO2-
55 S_TXO2+ — S_TXO2+
55 S_TXOC- — S_TXOC-
55 S_TXOC+ — S_TXOC+
55 S_TXO3- — S_TXO3-
55 S_TXO3+ — S_TXO3+

GPIO

24 LVDS_DET_A*
24 LVDS_DET_B*
55 DPLVDS_PANEL_VCC — DPLVDS_PANEL_VCC
55 IMS

From RTD2136R

0624 Eric modify

S_TXO0+ / S_TXO0-
S_TXO1+ / S_TXO1-
S_TXO2+ / S_TXO2-
S_TXO3+ / S_TXO3-
S_TXOC+ / S_TXOC-
S_TXE0+ / S_TXE0-
S_TXE1+ / S_TXE1-
S_TXE2+ / S_TXE2-
S_TXE3+ / S_TXE3-
S_TXEC+ / S_TXEC-

09/11 Allen modify

LVDS1

ACES-CON60J-GP

SC040 12/23 Allen modify
SC051 01/06 Allen modify

R79729 10KR2F-3-GP — VCC5_PANEL
R79730 10KR2F-3-GP — SB3V
LVDS_DET_A*
Q664B AO3413L-GP (84.02130.031) — VCC5_PANEL
R78718 100R2F-L1-GP-U
R11852 1KR2F-3-GP — VCC5_PANEL
2Q1 Allen add
IMS for LG Interlace Mode Selection function
VCC5_PANEL
LVDS_DET_B_C*
C12222 C12223 C12222
SCD1U16V2KX-GP
R79811 0R2J-2-GP
Q103 2N7002A-7-GP (84.2N702.231) — SB3V
R79732 10KR2J-3-GP
LVDS_DET_B*
C12223
SCD1U16V2KX-GP

SC058 01/08 Allen modify

VCC5_PANEL
R80230 10KR2J-3-GP
BIST_PIN25_G
Q9650 2N7002A-7-GP (84.2N702.231)
BIST_PIN25

DCBATOUT
R79738 100KR2J-1-GP
Q1261 2N7002A-7-GP (84.2N702.231)
R79727 470KR2F-GP
VCC
C12113 SC4D7U10V3KX-0GP
U65 AOZ8052AQI-GP
MAIN: 84.80482.B3D
Alt: 84.80655.B3D
L62 HCB2012KF-600T30-GP (68.00335.121)
V_5_LCD1
V_5_LCD2
R79735 330R3J-L-GP
PANEL_ON_5
Q1262 2N7002A-7-GP (84.2N702.231)
High: Enable
Low: Disable
C12156 SE000102V2KX-3D-GP
R19 1MR2J-1-GP
PANEL_ON_4
Low: Enable
High: Disable
07/24 Allen modify for down size
F17 POLYSW-2A6V-7-GP
SB000 09/30 Allen del

VCC3
R79737 10KR2J-3-GP (R_)
R79376 10KR2J-3-GP
DPLVDS_PANEL_VCC
R79738 22R2J-2-GP
PANEL_ON_3
R42 10KR2J-3-GP
PANEL_ON_2
Q1283 MMBT3904-4-GP-R (84.T3904.H11)
09/30 Allen modify for EOM
High: Enable
Low: Disable

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 058_PANEL CONTROL

Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

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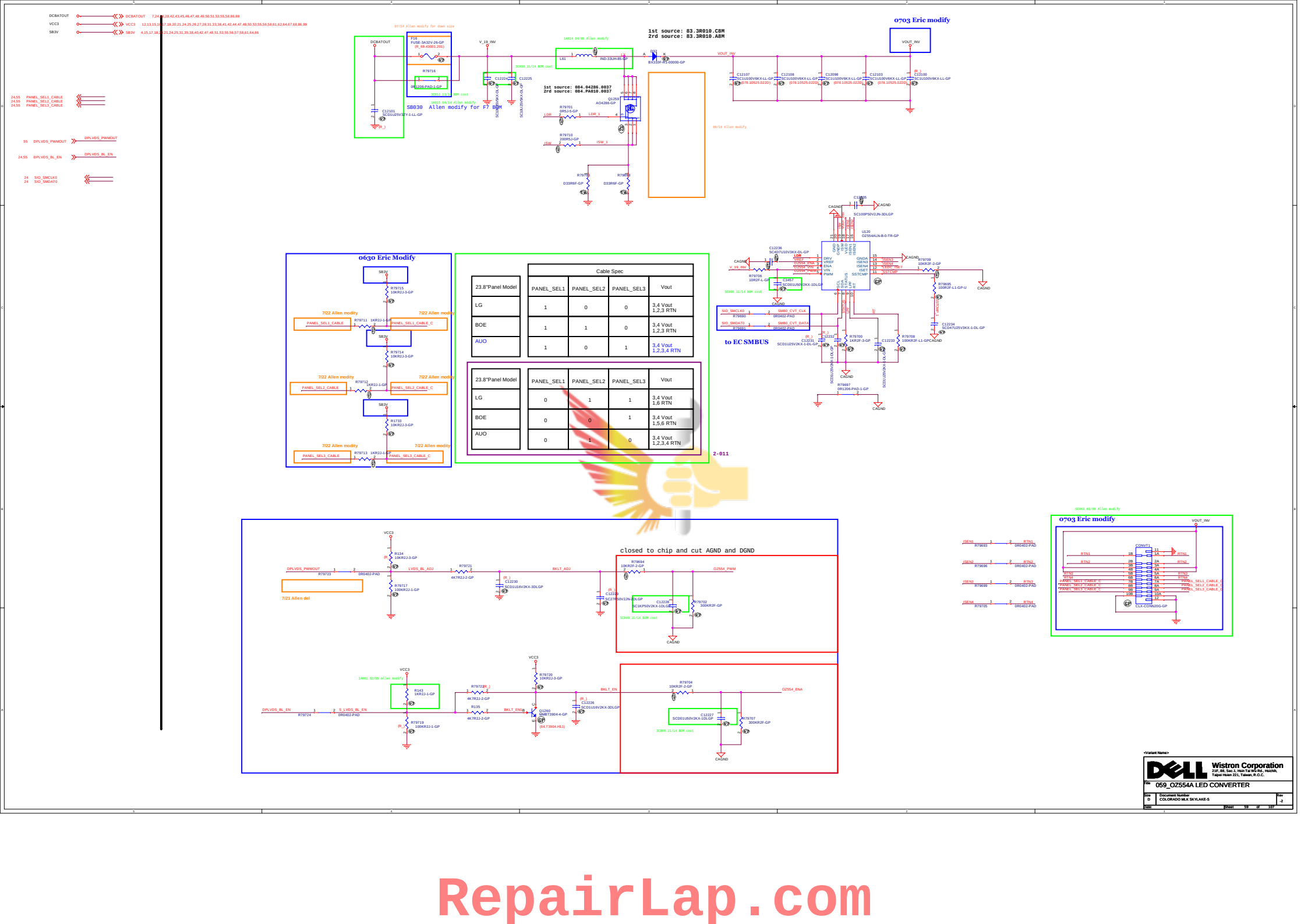


RepairLap.com

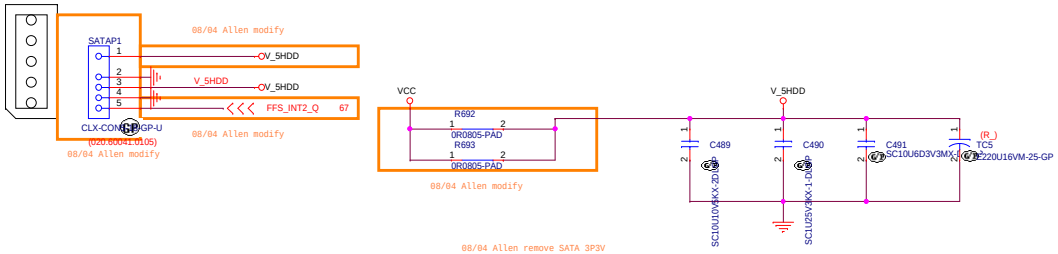
VCC — VCC 15,24,26,27,41,42,44,45,46,55,56,57,58,64,67,68,86,88

SATA

17 SATAHDR_RX_DP2
17 SATAHDR_RX_DN2
17 SATAHDR_TX_DN2
17 SATAHDR_TX_DP2
17 SATAHDR_RX_DP3
17 SATAHDR_RX_DN3
17 SATAHDR_TX_DN3
17 SATAHDR_TX_DP3

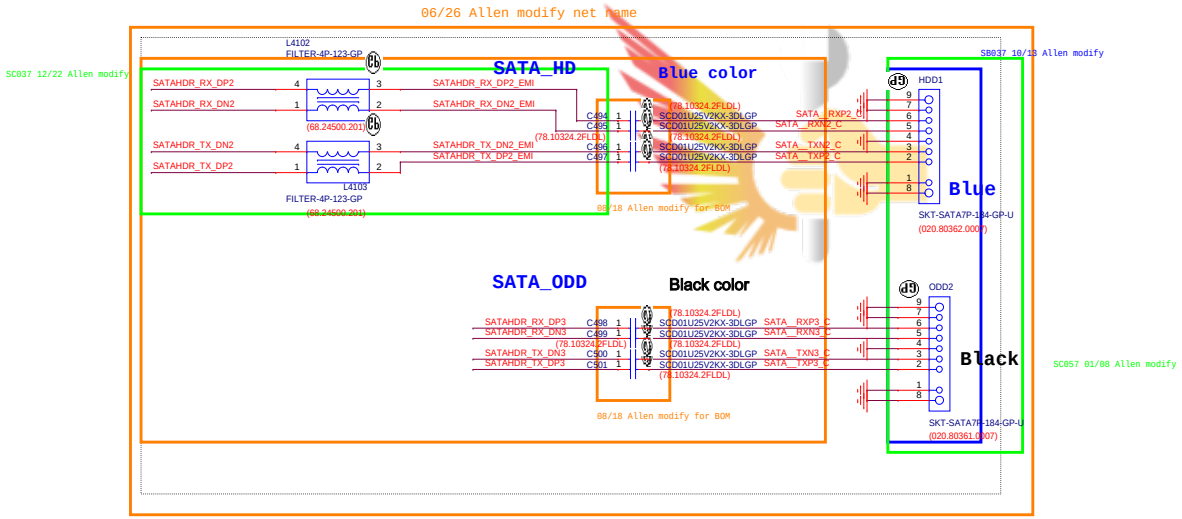
SATA

Layout: Please put them together



08/11 Allen modfiy SATA connector

06/26 Allen modify net name



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 060_HDD/ODD

Size: C | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 60 of 107

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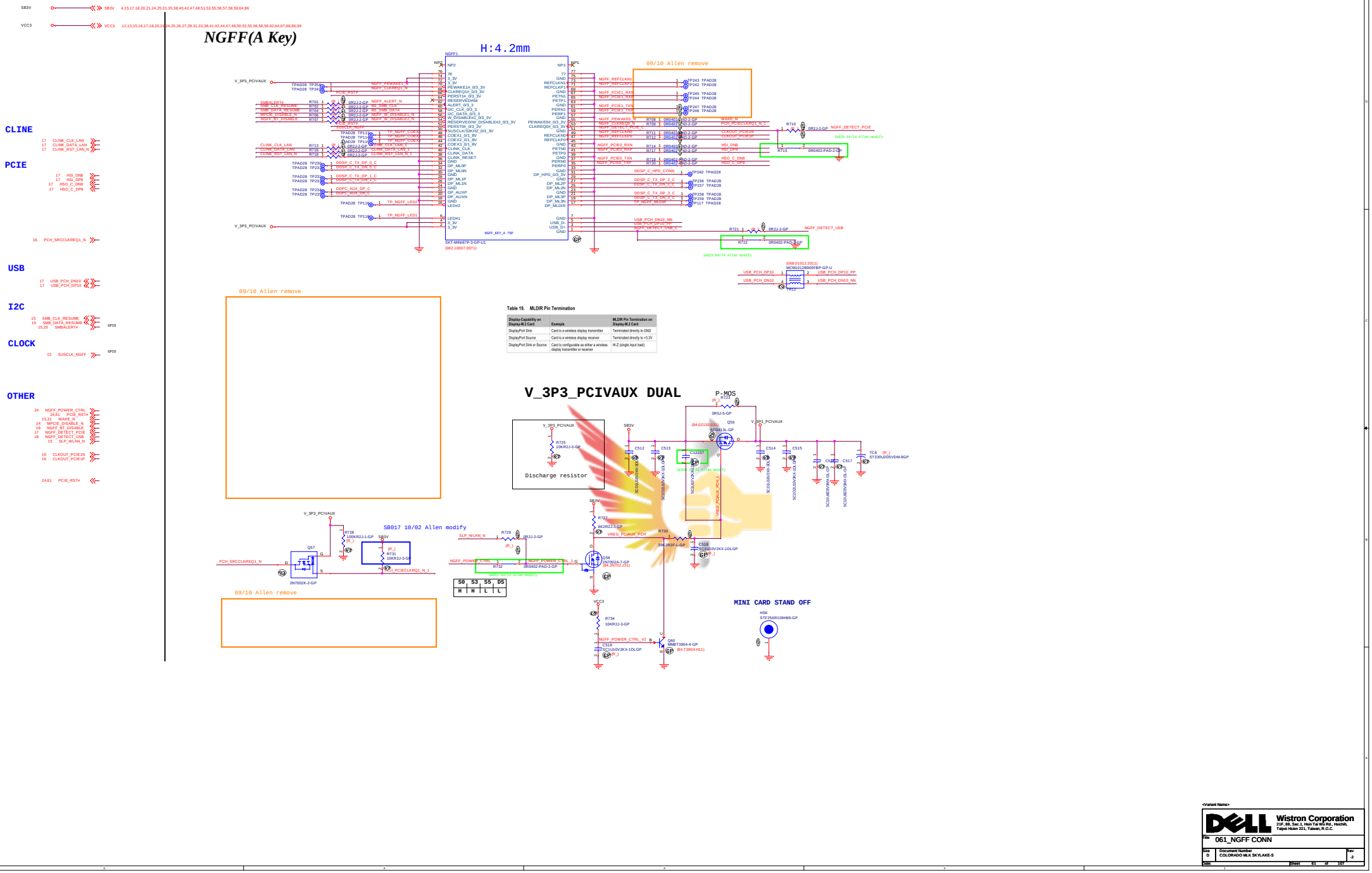

Table 19. MLDIR Pin Termination

Display-Capability on Display-M.2 Card	Example	MLDIR Pin Termination on Display-M.2 Card
DisplayPort Sink	Card is a wireless display transmitter	Terminated directly to GND
DisplayPort Source	Card is a wireless display receiver	Terminated directly to +3.3V
DisplayPort Sink or Source	Card is configurable as either a wireless display transmitter or receiver	Hi-Z (single input load)

S0	S3	S5	DS
H	H	L	L

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VCC3 → VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,41,42,44,47,48,50,53,55,56,58,59,61,64,67,68,86,99

VCC5_USB → VCC5_USB 34,35,42

USB TOUCH PANEL

17 USB_PCH_DN8
17 USB_PCH_DP8
24 TP_DET → GPIO

TOUCH PANEL

SB 09/30 Allen modify

VCC5_USB → F12 POLYSW-1D5A6V-12-GP (T_) → USBVCCTP

C520 SC10U10V5KX-2DLGP

TR13
USB_PCH_DP8 → USB_PCH_DP8_PP
USB_PCH_DN8 → USB_PCH_DN8_NN
MCM1012B900FBP-GP-U
(T_068.01012.2011)

FOR EMI

USB_PCH_DP8_PP
USB_PCH_DN8_NN
(R_) C522 SC10P50V2JN-4GS
(R_) C523 SC10P50V2JN-4GS

VCC3 → R738 10KR2J-3-GP → TP_DET

USBVCCTP

SB031 10/07 Allen modfiy symbol

SB014 09/30 Allen modify SMD for layout space

TOUCH2
USB_PCH_DP8_PP
USB_PCH_DN8_NN
ENT-CON5-GP

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<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: 062_TOUCH

Size: C | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 62 of 107

<Variant Name>

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Title

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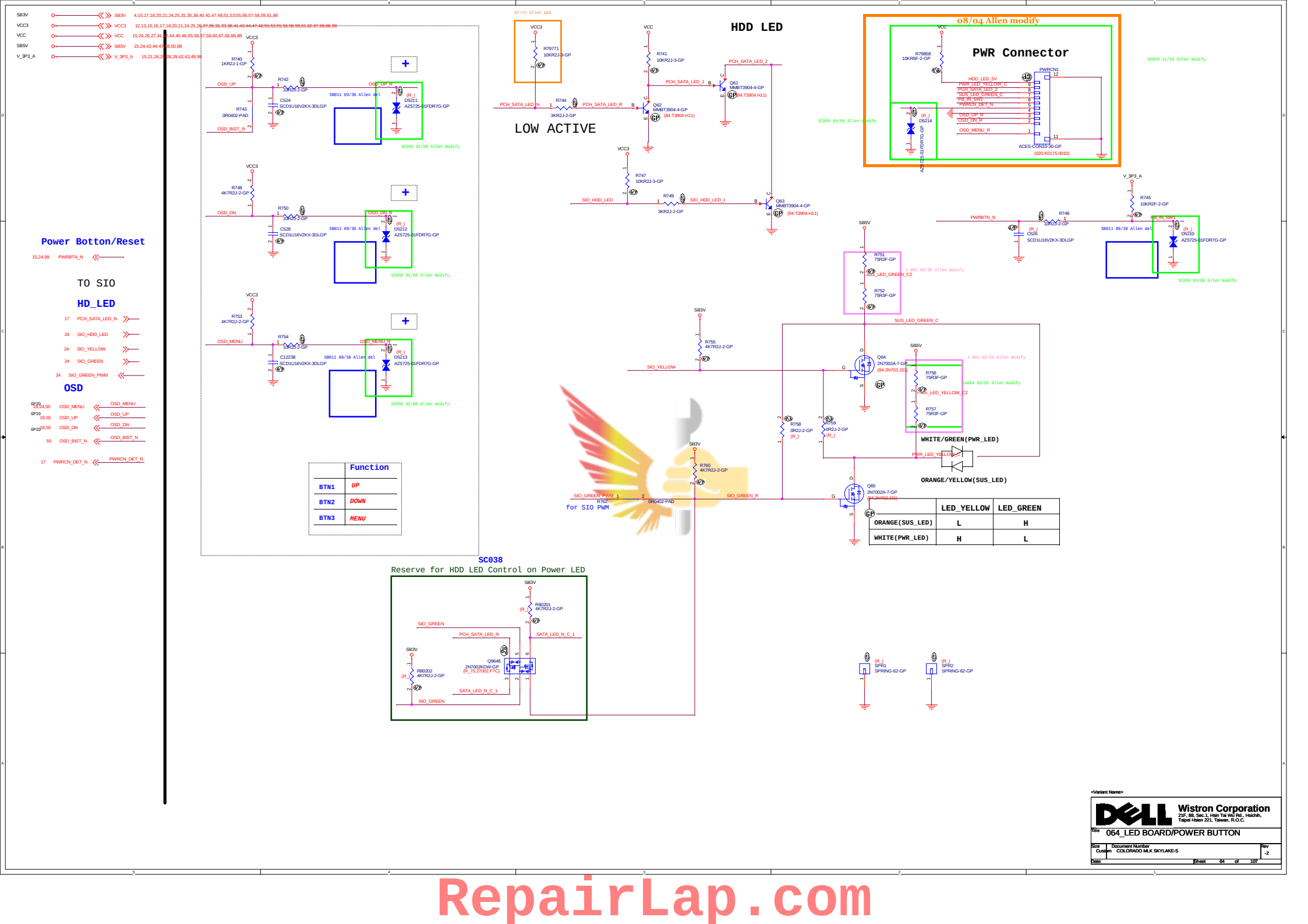

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Title		
Size: A4	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
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<Variant Name>

Wistron Corporation
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Title

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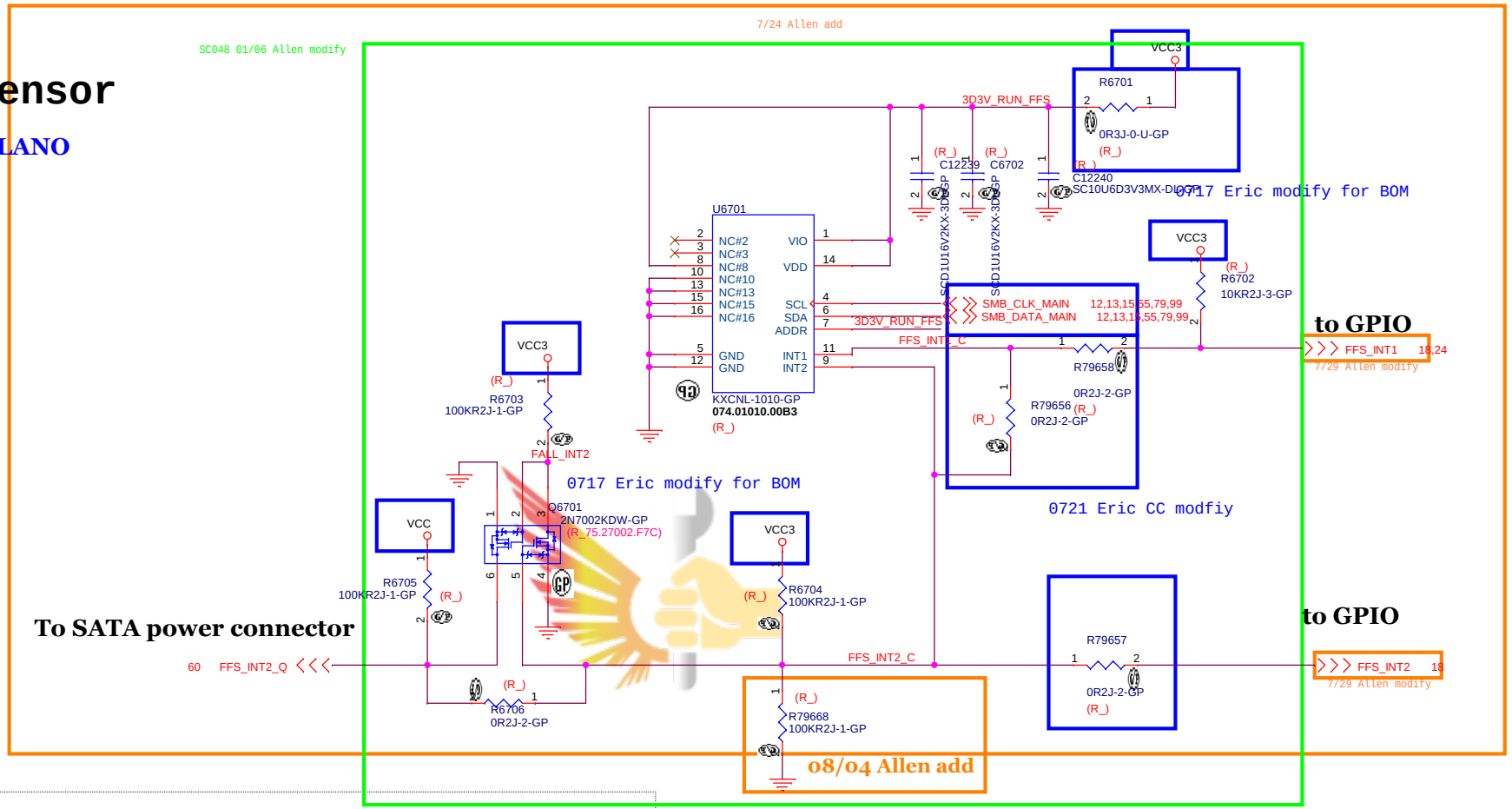
VCC VCC 15,24,26,27,41,42,44,45,46,55,56,57,58,60,64,68,86,88

VCC3 VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,41,42,44,47,48,50,53,55,56,58,59,61,62,64,68,86,99

Free Fall Sensor

0716 modfiy from PLANO



Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: 067_FFS		
Size: B	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
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SSID = DEBUG PORT

VCC — VCC — 15,24,26,27,41,42,44,45,48,55,56,57,58,60,64,67,86,88

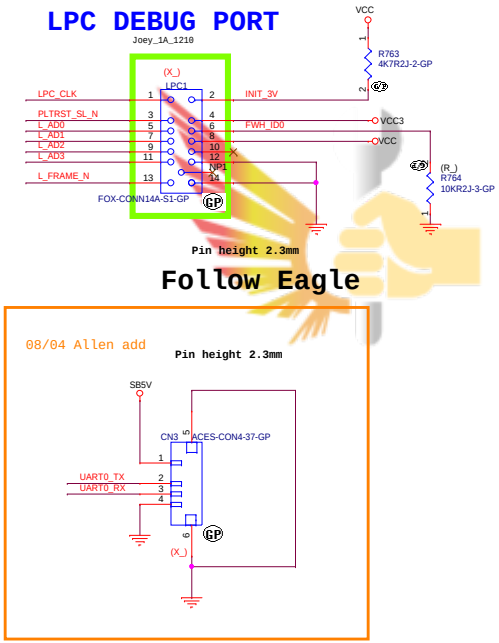
VCC3 — VCC3 — 12,13,15,16,17,18,20,21,23,25,26,27,28,31,33,38,41,42,44,47,48,50,53,55,56,58,59,61,62,64,67,86,99

SB5V — SB5V — 15,24,42,44,47,48,50,64

LPC DEBUG PORT

18,24 L_AD0
18,24 L_AD1
18,24 L_AD2
18,24 L_AD3
18,24 L_FRAME_N
18,24 LPC_CLK
24,76 PLTRST_SL_N

19 UART0_TX
19 UART0_RX



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 068_DEBUG CONNECTOR

Size: C | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

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<Variant Name>

Reserved

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

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A	COLORADO MLK SKYLAKE-S	-2

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<Variant Name>

Reserved

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	SA

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<Variant Name>

DELL	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		
Size: A4	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
Date:	Sheet 71 of 107	

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<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A3	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 72 of 107

<Variant Name>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Reserved		
Size: A4	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
Date:	Sheet 73 of 107	

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<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A	COLORADO MLK SKYLAKE-S	-2

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<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title Reserved

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+V_1P05_VGA +V_1P05_VGA 78,79,86

+V_3P3_VGA +V_3P3_VGA 79,80,86,88

PCIEX4

5 PEG_TXP[7..0]
5 PEG_TXN[7..0]

5 PEG_RXP[7..0]
5 PEG_RXN[7..0]

16,76 CK_PE_100M_16PORT_DP
16,76 CK_PE_100M_16PORT_DN

24,68,76 PLTRST_SL_N

79 PEX_RST_GPU

+V_3P3_VGA

R591 10KR2J-3-GP (G_)

PEX_CLKREQ

AMD_RST#_L — R1212 0R0402-PAD-2-GP — PEX_RST_GPU

100MHz

16,76 CK_PE_100M_16PORT_DP
16,76 CK_PE_100M_16PORT_DN

GPU1A 1 OF 14
1/14 PCI_EXPRESS

PEG_RXP0 / PEG_RXN0	SCD22U10V2KX-2-GP	PEG_C_RXP0 / PEG_C_RXN0
PEG_RXP1 / PEG_RXN1	SCD22U10V2KX-2-GP	PEG_C_RXP1 / PEG_C_RXN1
PEG_RXP2 / PEG_RXN2	SCD22U10V2KX-2-GP	PEG_C_RXP2 / PEG_C_RXN2
PEG_RXP3 / PEG_RXN3	SCD22U10V2KX-2-GP	PEG_C_RXP3 / PEG_C_RXN3
PEG_RXP4 / PEG_RXN4	SCD22U10V2KX-2-GP	PEG_C_RXP4 / PEG_C_RXN4
PEG_RXP5 / PEG_RXN5	SCD22U10V2KX-2-GP	PEG_C_RXP5 / PEG_C_RXN5
PEG_RXP6 / PEG_RXN6	SCD22U10V2KX-2-GP	PEG_C_RXP6 / PEG_C_RXN6
PEG_RXP7 / PEG_RXN7	SCD22U10V2KX-2-GP	PEG_C_RXP7 / PEG_C_RXN7

PEG_TXP0 / PEG_TXN0	AG6 / AG7	PEX_RX0 / PEX_RX0#
PEG_TXP1 / PEG_TXN1	AF7 / AE7	PEX_RX1 / PEX_RX1#
PEG_TXP2 / PEG_TXN2	AE9 / AF9	PEX_RX2 / PEX_RX2#
PEG_TXP3 / PEG_TXN3	AG9 / AG10	PEX_RX3 / PEX_RX3#
PEG_TXP4 / PEG_TXN4	AF10 / AE10	PEX_RX4 / PEX_RX4#
PEG_TXP5 / PEG_TXN5	AE12 / AF12	PEX_RX5 / PEX_RX5#
PEG_TXP6 / PEG_TXN6	AG12 / AG13	PEX_RX6 / PEX_RX6#
PEG_TXP7 / PEG_TXN7	AF13 / AE13	PEX_RX7 / PEX_RX7#

PEX_WAKE#	AB6
PEX_RST#	AC7
PEX_CLKREQ#	AC6
PEX_REFCLK	AE8
PEX_REFCLK#	AD8
PEX_TX0 / PEX_TX0#	AC9 / AB9
PEX_TX1 / PEX_TX1#	AB10 / AC10
PEX_TX2 / PEX_TX2#	AD11 / AC11
PEX_TX3 / PEX_TX3#	AC12 / AB12
PEX_TX4 / PEX_TX4#	AB13 / AC13
PEX_TX5 / PEX_TX5#	AD14 / AC14
PEX_TX6 / PEX_TX6#	AC15 / AB15
PEX_TX7 / PEX_TX7#	AB16 / AC16
PEX_TX8 / PEX_TX8#	AD17 / AC17
PEX_RX8 / PEX_RX8#	AE15 / AF15
PEX_TX9 / PEX_TX9#	AC18 / AB18
PEX_RX9 / PEX_RX9#	AG15 / AG16
PEX_TX10 / PEX_TX10#	AB19 / AC19
PEX_RX10 / PEX_RX10#	AF16 / AE16
PEX_TX11 / PEX_TX11#	AD20 / AC20
PEX_RX11 / PEX_RX11#	AE18 / AF18
PEX_TX12 / PEX_TX12#	AC21 / AB21
PEX_RX12 / PEX_RX12#	AG18 / AG19
PEX_TX13 / PEX_TX13#	AD23 / AE23
PEX_RX13 / PEX_RX13#	AF19 / AE19
PEX_TX14 / PEX_TX14#	AF24 / AE24
PEX_RX14 / PEX_RX14#	AE21 / AF21
PEX_TX15 / PEX_TX15#	AG24 / AG25
PEX_RX15 / PEX_RX15#	AG21 / AG22

NC FOR GM108

NC FOR GF117/GK208/GM108

PEX_IOVDD_1 … PEX_IOVDD_6	AA22, AB23, AC24, AD25, AE26, AE27
PEX_IOVDDQ_1 … PEX_IOVDDQ_14	AA10, AA12, AA13, AA16, AA18, AA19, AA20, AA21, AB22, AC23, AD24, AE25, AF26, AF27
NC FOR GF119	
PEX_PLL_HVDD_1 / PEX_PLL_HVDD_2	AA8 / AA9
PEX_SVDD_3V3	AB8
VDD_SENSE	F2 — PWR_VGA_CORE_SENCE+ — PWR_VGA_CORE_SENCE+ 88
GND_SENSE	F1 — PWR_VGA_CORE_SENCE- — PWR_VGA_CORE_SENCE- 88
PEX_TSTCLK_OUT / PEX_TSTCLK_OUT#	AF22 / AE22 — PEX_TSTCLK_OUT / PEX_TSTCLK_OUT# — R193 200R2F-L-GP
PEX_PLLVDD_1 / PEX_PLLVDD_2	AA14 / AA15 — PEX_PLLVDD_GPU
TESTMODE	AD9 — GPU_TESTMODE — R192 10KR2J-3-GP
PEX_TERMP	AF25 — PEX_TERMP — R79978 2K49R2F-GP

N16S-GM-S-A2-GP
(G_071.0N16S.0G0U)

+V_1P05_VGA

C445 C434 C437 SCD1U6D3V3MX-DL-GP SCD1U6D3V3KX-1DLGP
C412 C413 C417 C420 SCD1U6D3V3MX-DL-GP SCD1U6D3V3KX-2DLGP

+V_1P05_VGA

C442 C441 C433 SCD1U6D3V3KX-1DLGP SCD1U6D3V3MX-DLGP
C12376 C421 C429 C426 SCD1U6D3V3MX-DLGP SCD1U6D3V3KX-2DLGP

+V_3P3_VGA

C440 C443 C438 SCD1U16V2KX-3DLGP SC4D7U6D3V3KX-DLGP SC4D7U6D3V3KX-DLGP

+V_1P05_VGA

L9524 (G_68.00217.161) MCB1608S121IBP-GP

C444 C435 C427 C430 C428 SC10U16V2KX-3DLGP SC10U6D3V5KX-1DLGP SC47U2V5KX-1DLGP SC47U2V5KX-1DLGP SC10U6D3V5KX-1DLGP

100MHZ 120mohm

1U Under GPU

4.7U NEAR TO GPU

10U mid TO GPU

Michael 2011/12/12

Add two 1uF Caps according to the NV Comment

SB042 10/17 Allen modify

08/14 Allen add for iRMT

SC005 11/11 Allen modify

R80059 10KR2J-2-GP (G_) +V_3P3_VGA

24 SIO_GPU_RST
24,68,76 PLTRST_SL_N

U9521 NL17SZ08DFT2G-GP (R_)

AMD_RST#_L

(R_) R80060 100KR2F-L1-GP

SB0055 10/22 Allen modify

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 076_GPU(1/5) PEG

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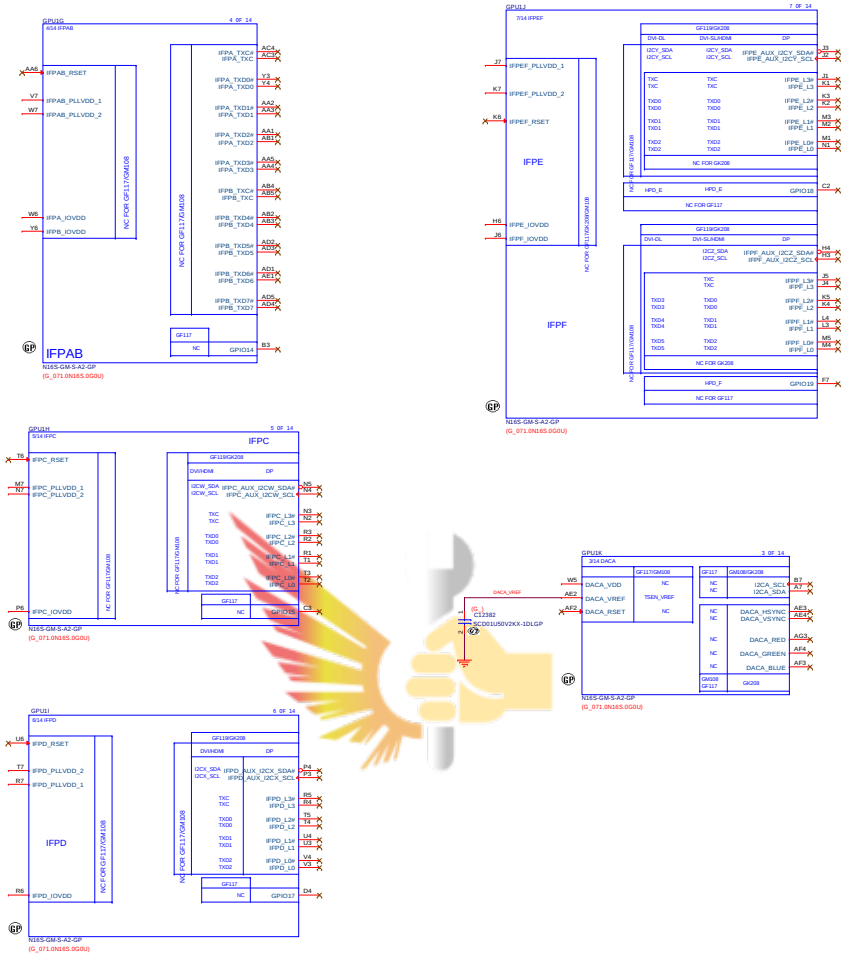

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<Variant Name>

Wistron Corporation
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Title: 077_GPU(2/5)DIGITALOUT

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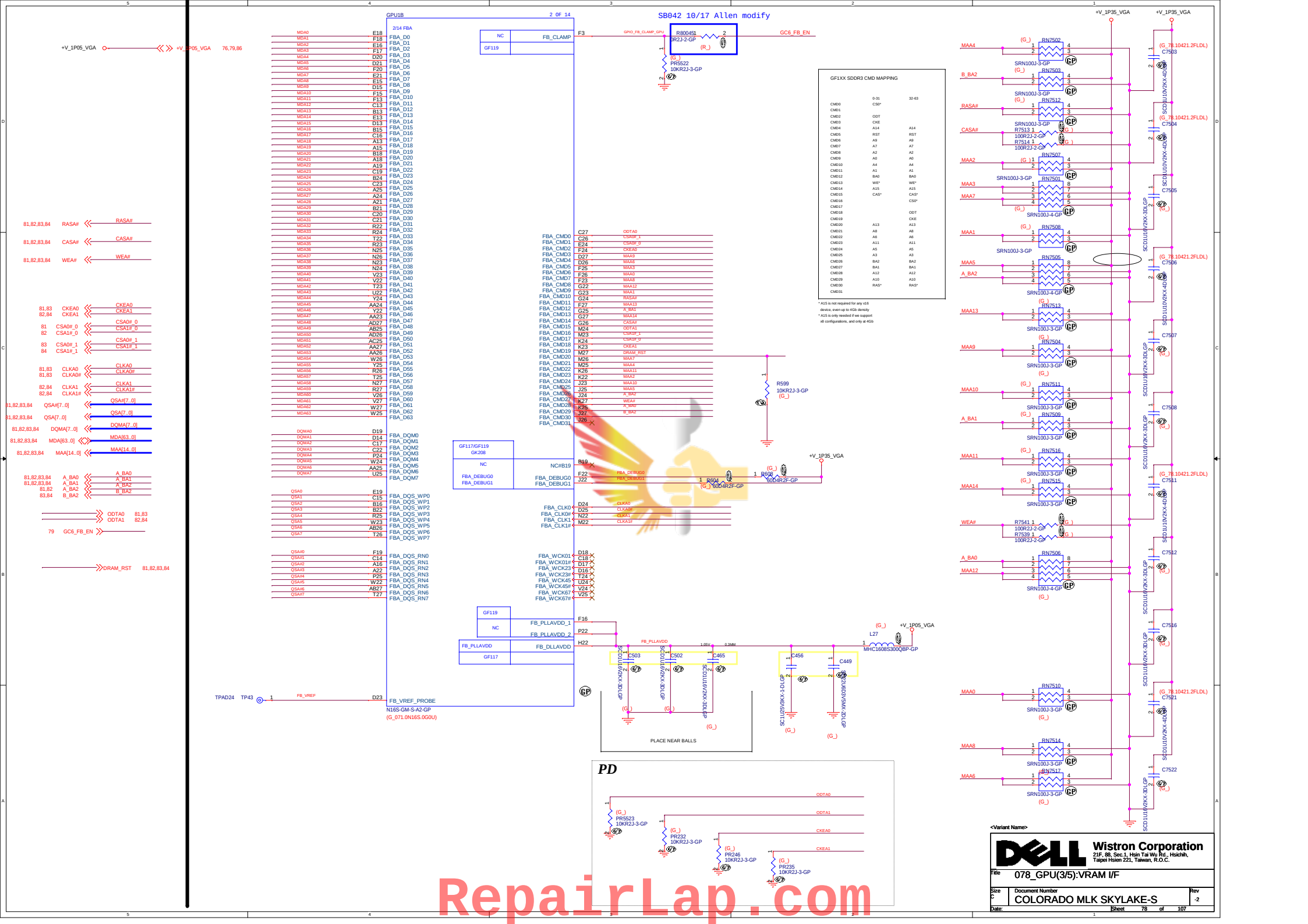
GPU1B
2 OF 14
SB042 10/17 Allen modify
2/14 FBA
GF1XX SDDR3 CMD MAPPING
PLACE NEAR BALLS
PD
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
078_GPU(3/5):VRAM I/F
Size
C
Document Number
COLORADO MLK SKYLAKE-S
Rev
-2
Date:
Sheet 78 of 107
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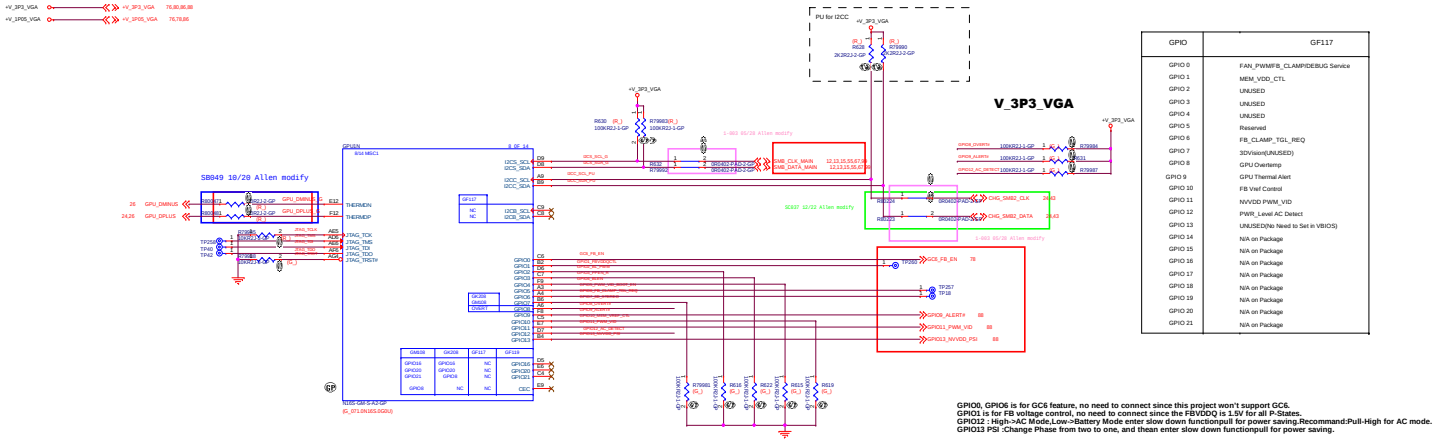


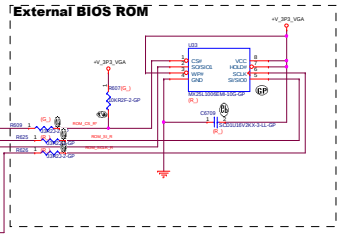
GPIO	GF117
GPIO 0	FAN_PWMFB_CLAMPDEBUG Service
GPIO 1	MEM_VDD_CTL
GPIO 2	UNUSED
GPIO 3	UNUSED
GPIO 4	UNUSED
GPIO 5	Reserved
GPIO 6	FB_CLAMP_TGL_REQ
GPIO 7	3DVision(UNUSED)
GPIO 8	GPU Overtemp
GPIO 9	GPU Thermal Alert
GPIO 10	FB Vsnf Control
GPIO 11	NVVDD PWM_VID
GPIO 12	PWR_Level AC Detect
GPIO 13	UNUSED(No Need to Set in VBIOS)
GPIO 14	N/A on Package
GPIO 15	N/A on Package
GPIO 16	N/A on Package
GPIO 17	N/A on Package
GPIO 18	N/A on Package
GPIO 19	N/A on Package
GPIO 20	N/A on Package
GPIO 21	N/A on Package

GPIO0, GPIO6 is for GC6 feature, no need to connect since this project won't support GC6.
GPIO1 is for FB voltage control, no need to connect since the FBVDDQ is 1.5V for all P-States.
GPIO12 : High->AC Mode,Low->Battery Mode enter slow down functionpull for power saving.Recommand:Pull-High for AC mode.
GPIO13 PSI :Change Phase from two to one, and thean enter slow down functionpull for power saving.

Table 12-1. GB2-64 GPIO Description

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	Reserved			
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	Pull-up/pull-down to set the FBVDD/Q boot voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 kΩ pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	100 kΩ pull-down
GPIO4	LCD_BLEH	O	Panel Backlight Enable	100 kΩ pull-down
GPIO5	Reserved			
GPIO6	Reserved			
GPIO7	3DVision	O	3D Vision L/R signal	100 kΩ pull-down
GPIO8	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up
GPIO9	THERM_ALERT	I/O	Thermal Alert, Open Drain	10 kΩ pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL		AC power detect or power supply overdraw input	100 kΩ pull-up
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	Reserved			
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IPFB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	Reserved			

STRAP



STRAP PIN MODE TABLE	
PIN NAME	BINARY BRINGUP
STRAP0	3GIO_PADCFG_LUT_ADR0
STRAP1	3GIO_PADCFG_LUT_ADR1
STRAP2	3GIO_PADCFG_LUT_ADR2
STRAP3	3GIO_PADCFG_LUT_ADR3
STRAP4	PCI_MAX_SPEED
ROM_SCLK	SMB_ALT_ADDR
ROM_SI	SUB_VENDOR
ROM_SO	VGA_DEVICE

NOTE 2: See table 1 for the correct value/location of the strap resistor for the desired modes

NOTE 3: Bring-up SKU(s) have jumper configurable subvendor and DEVID_A settings see the ROM_SCLK STRAP

Table 4. H16S-GM/-GT/-LP DDR3L Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
DDR3L	1.35V/ 1.35V	128Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC2G63FFR-11C	F-die	0x9	900	H/A	Production ready
				Micron	MT41J128M16JT-093:K	K-die	0xA	900	1322	Production ready
				Samsung	K4W2G1646Q-BC1A	Q-die	0xB	900	H/A	Production ready
		256Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0x3	900	H/A	Production ready
				Micron	MT41J256M16HA-093:E	E-die	0x4	900	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	H/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0x1	900	H/A	Post production ready
				Hynix	H5TC4G63CFR-H0C	C-die	0x2	900	H/A	Post production ready
			Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0x3	900	H/A	Production ready
				Micron	MT41J256M16HA-093:G/E	E-die	0x4	900	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	H/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0x7	900	H/A	Post production ready
				Hynix	H5TC4G63CFR-H0C	C-die	0xE	900	H/A	Post production ready

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

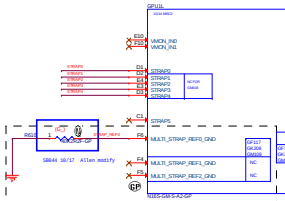


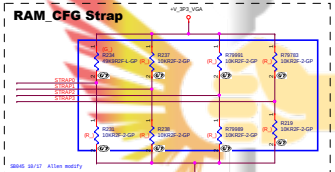
Table 119. Device Specific Strap Mode Selection

	N14M-GE/-GL	Other N14x GPUs
Multi_Strap_Ref2_GND (Only on GB2-64 package)	No Connect	H/A
Multi_Strap_Ref1_GND (Only on GB2-64 package)	No Connect	H/A
Multi_Strap_Ref0_GND	No Connect	40.2k 1% to GND
Strap Mode Selected	Bit4/0	Multi-Level

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

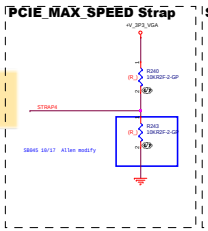
Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			
STRAP2				
STRAP3				
STRAP4				

RAM_CFG Strap

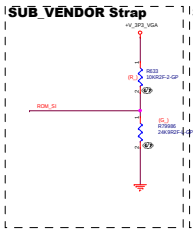


RMA_CFG [3:0]
Samsung - K4W2G1646E-BC11 (1000MHz) [0101]
Micron - MT41J128M16JT-093G:K (1000MHz) [0001]

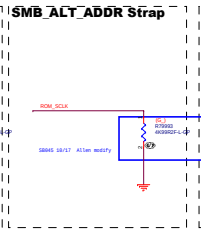
PCIE_MAX_SPEED Strap



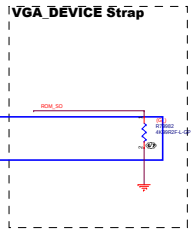
SUB_VENDOR Strap



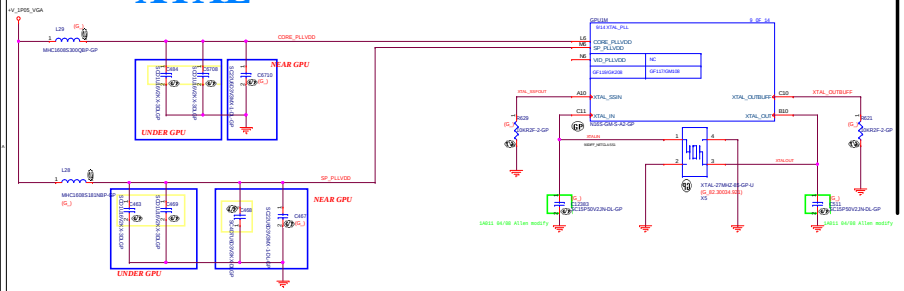
SMB_ALT_ADDR Strap



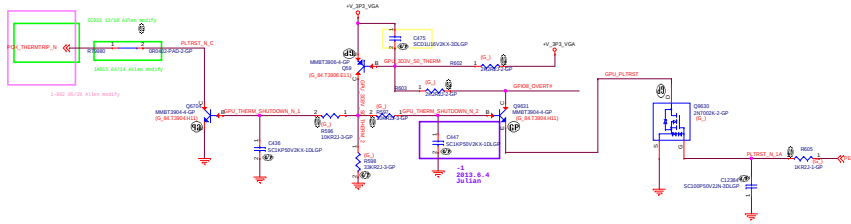
VGA_DEVICE Strap



XTAL



THERMAL PROTECTION



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079_GPU(4/5):GPIO/STRAP
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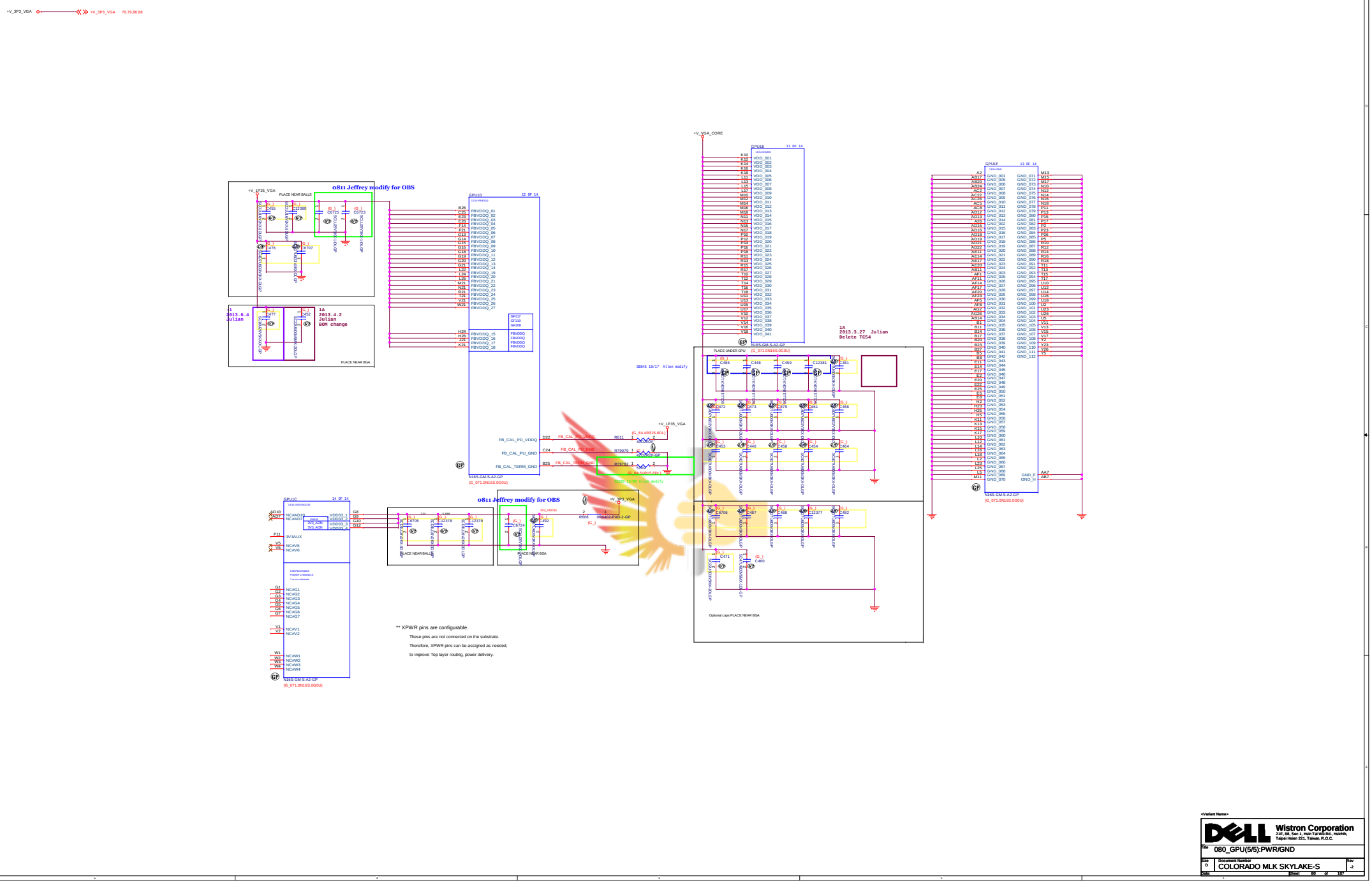

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Title: 080_GPU(5/5):PWR/GND
Size: D
Document Number: COLORADO MLK SKYLAKE-S
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Date:
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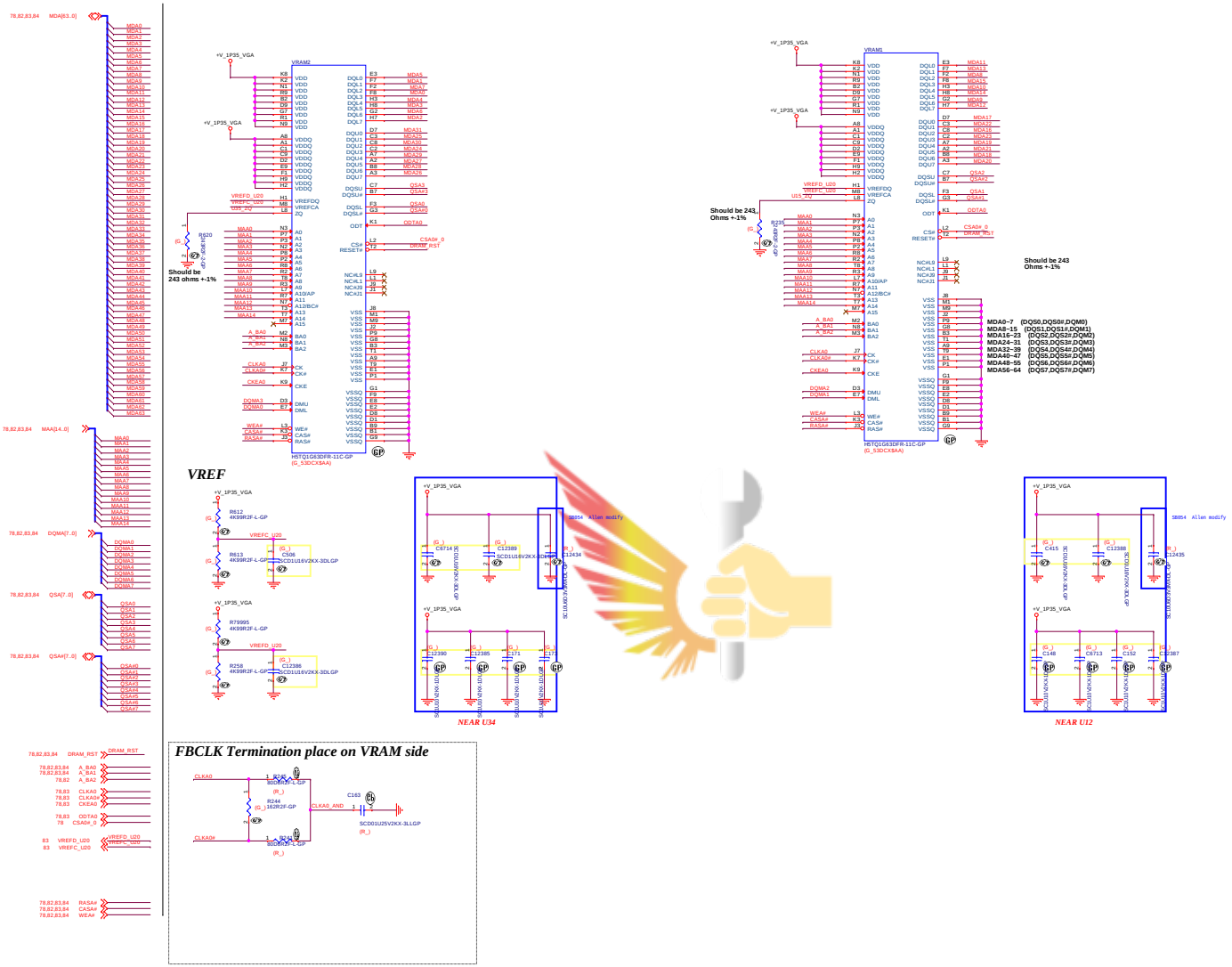
CHANNEL A:1GB DDR3

72.42164.G0U	2Gb DDR3 128M*16 900MHz SDRAM FBGA96P	Samsung- K4W2G1646E-BC11
0B41791AA	2Gb DDR3 128M*16 900MHz SDRAM FBGA96P	Hynix- H5TQ2G63DFR-11C



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Title: 081_VRAM 1,2 (1/4)
Size: D
Document Number: COLORADO MLK SKYLAKE-S
Rev: -2
Date:
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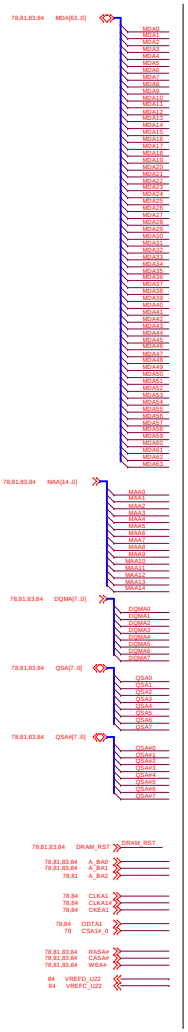
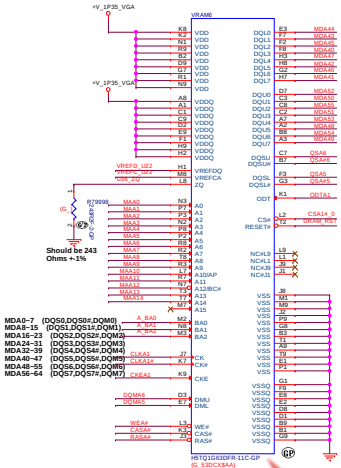
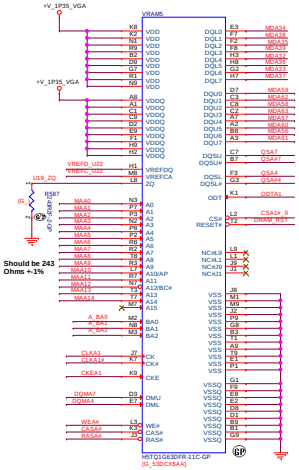
CHANNEL A:1GB DDR3

72.42164.G0U	2Gb DDR3 128M*16 900MHz SDRAM FBGA96P	Samsung- K4W2G1646E-BC11
0B41791AA	2Gb DDR3 128M*16 900MHz SDRAM FBGA96P	Hynix- H5TQ2G63DFR-11C







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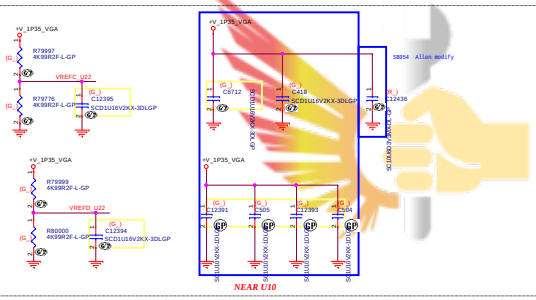
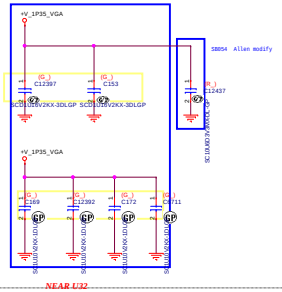
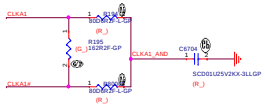




FBCLK Termination place on VRAM side



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CHANNEL A:1GB DDR3

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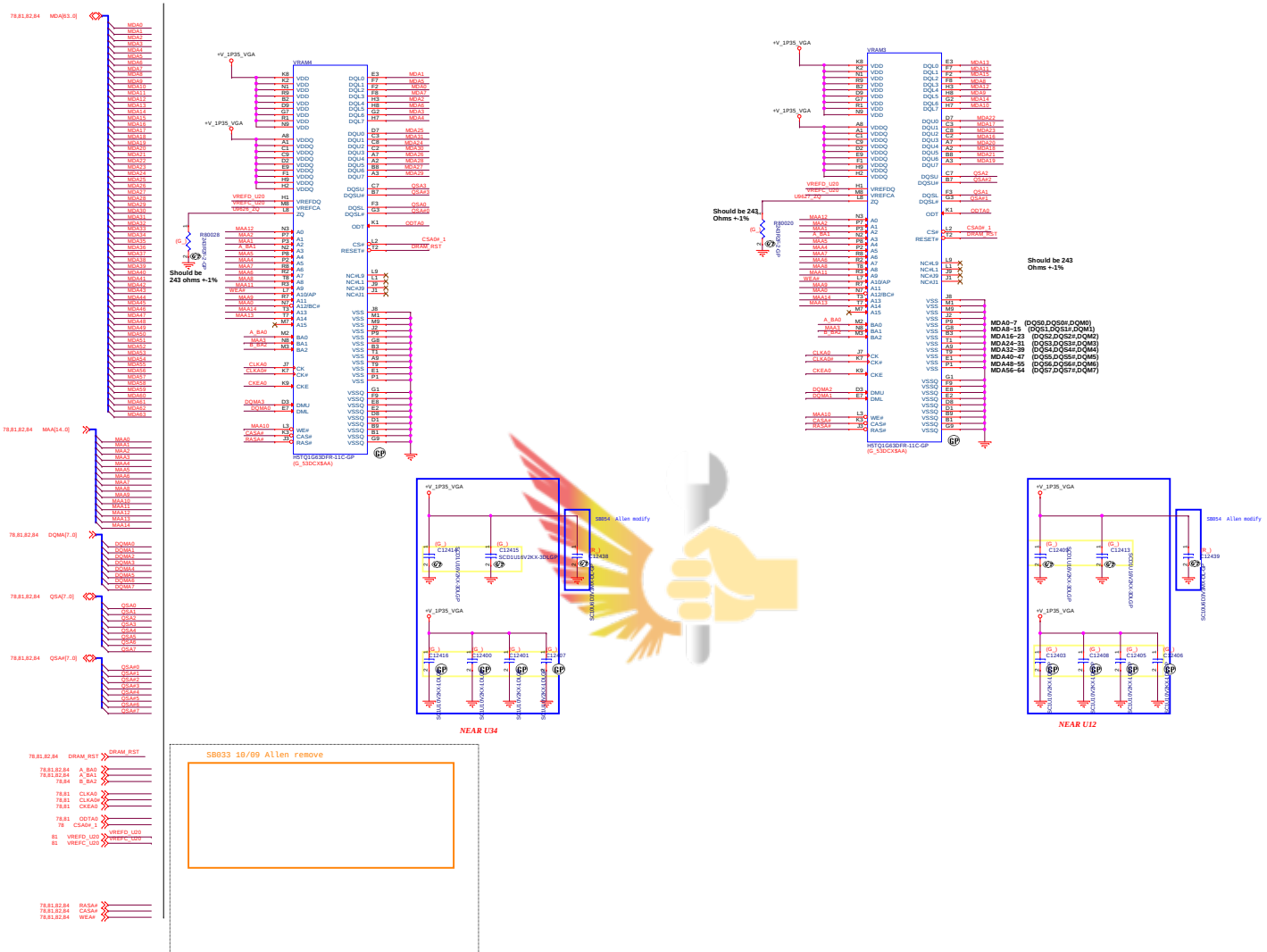
0B41791AA	2Gb	DDR3 128M*16 900MHz SDRAM FBGA96P	Hynix-	H5TQ2G63DFR-11C



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Title: 083_VRAM 5,6 (2/4)

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CHANNEL A:1GB DDR3

72.42164.G0U	2Gb DDR3 128M*16 900MHz SDRAM FBGA96P	Samsung- K4W2G1646E-BC11
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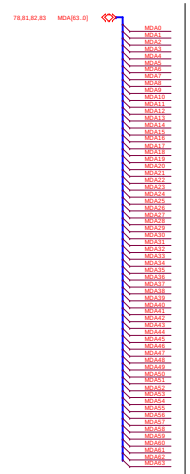

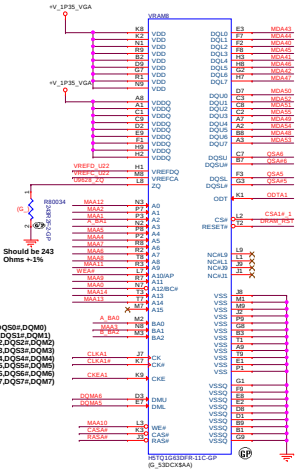

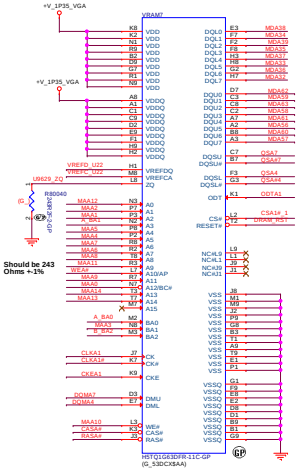

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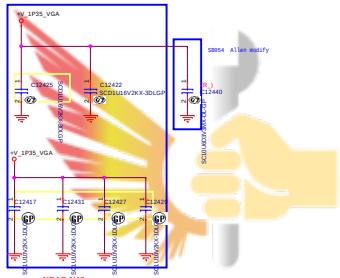

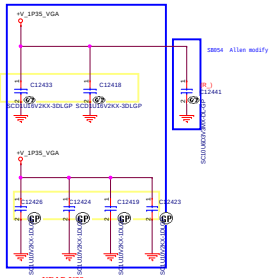

FBCLK Termination place on VRAM side

SB033 10/09 Allen remove

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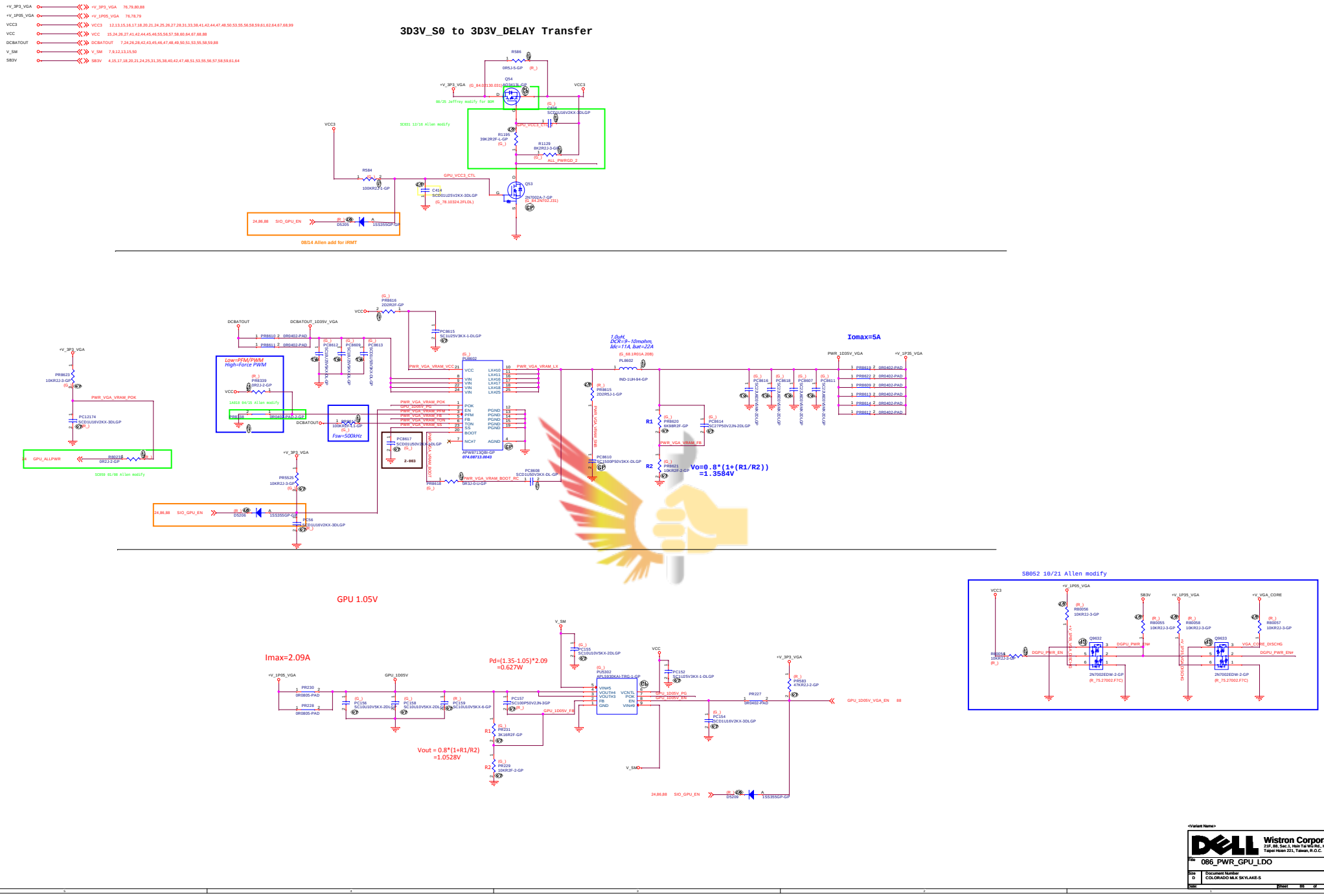

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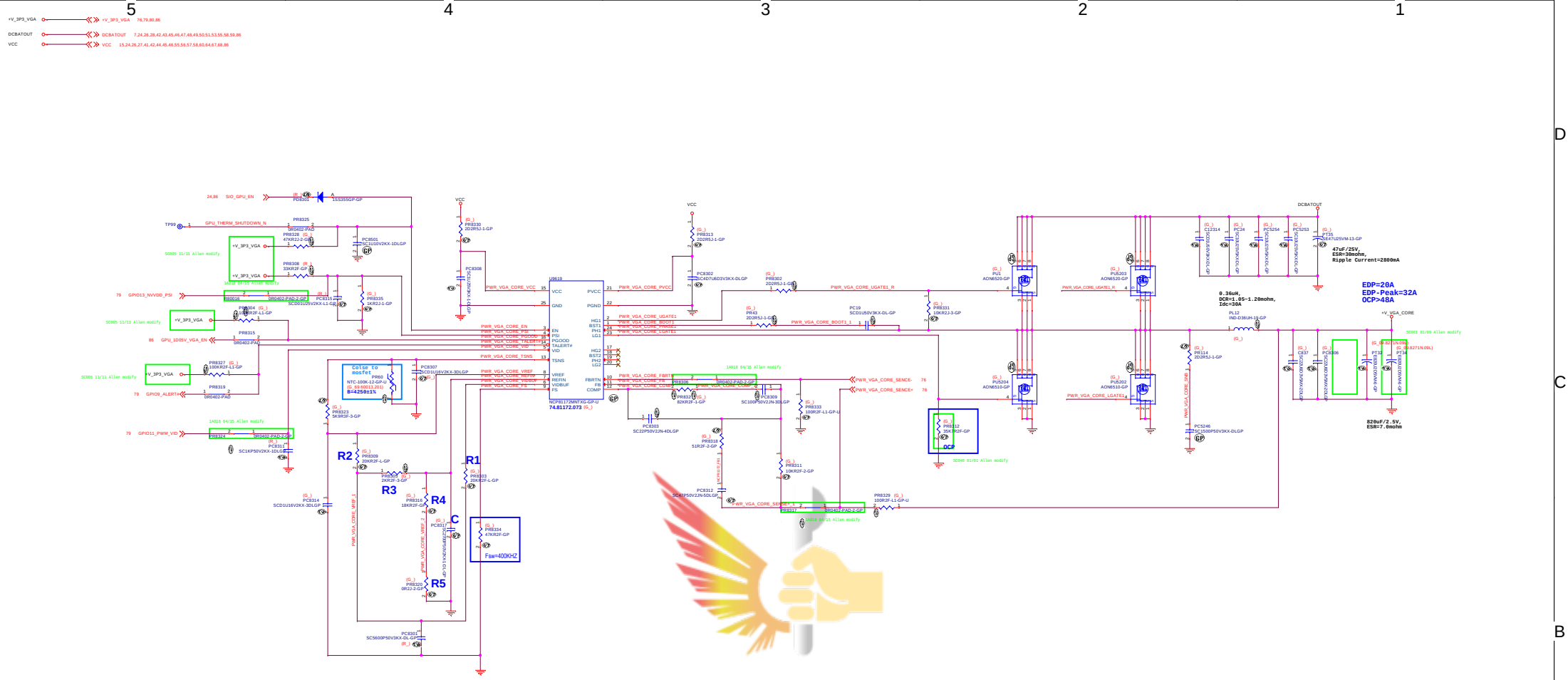

		Config A	Config B
R1 (1%)	KΩ	39	20
R2 (1%)	KΩ	39	20
R3 (1%)	KΩ	1.5	2
R4 (1%)	KΩ	30	18
R5 (1%)	KΩ	1.5	0
C	nF	1.5	2.7

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DELL

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Title

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Size: A4	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
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Title

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V1P0_PCH_S5 — V1P0_PCH_S5 7,15,21,51
V_3P3_A — V_3P3_A 15,21,24,25,28,29,42,43,49,64
V_CPU_IO — V_CPU_IO 4,5,7,8,9,48

VCC3 — VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,41,42,44,47,48,50,53,55,56,58,59,61,62,64,67,68,86
V_CPU_ST_PLL — V_CPU_ST_PLL 4,7,44
3P3V_SPI — 3P3V_SPI 20,21,25

XDP for CPU

4 H_TDO
4 H_TDI
4 H_TMS
4,15 H_TCK
4 H_TRST_N
4 H_PREQ_N
4 H_PRDY_N

4,15 H_PWRGD
4,40 VCCST_PWRGD
15,20,25 SPI_MOSI
4 SKL_PCUDEBUG_0
4 SKL_PCUDEBUG_1
4 SKL_PCUDEBUG_2
4 SKL_PCUDEBUG_3
4 SKL_PCUDEBUG_4
4 SKL_PCUDEBUG_5
4 SKL_PCUDEBUG_6
4 SKL_PCUDEBUG_7
4 SKL_PCUDEBUG_8
4 SKL_PCUDEBUG_9
4 SKL_PCUDEBUG_10
4 SKL_PCUDEBUG_11
4 SKL_PCUDEBUG_12
4 SKL_PCUDEBUG_13
4 SKL_PCUDEBUG_14
4 SKL_PCUDEBUG_15
4 XDP_PCUDERBUG_3
4 SKL_XDP_MBP_0
4 SKL_XDP_MBP_1

4 SKL_PCUSTB_0_DN
4 SKL_PCUSTB_0_DP
4 SKL_PCUSTB_1_DN
4 SKL_PCUSTB_1_DP
12,13,15,55,67,79 SMB_DATA_MAIN
12,13,15,55,67,79 SMB_CLK_MAIN
16 CK_100M_CPU_XDP_DN
16 CK_100M_CPU_XDP_DP
4,17 PLTRST_CPU_N
15,20,25 SPI_IO2

APS CONNECTOR

15,24,35,40,42,48,50,53,55 SLP_S3_N
7,15,24,35,42,55 SLP_S4_N
15 PCH_SLP_A_N
15,24,64,99 PWRBTN_N

XDP for PCH

15 PCH_JTAG_TCK
15,24,64,99 PWRBTN_N
15,24 RSMRST_N
15,24 PWRGD_3V
15 FP_RST_N
15 ITP_PMODE
22 PCH_XDP_PRDY_R_N
22 PCH_XDP_PREQ_R_N

XDP for CPU

1A015 04/14 Allen modify
PCH_XDP_PREQ_R_N — R1773 — H_PREQ_N
PCH_XDP_PRDY_R_N — R1774 — H_PRDY_N
3P3V_SPI — R79874 2K2R2J-2-GP — SPI_MOSI
PWRGD_3V — R1779 1KR2F-3-GP — XDP_VR_READY
R1781 — C12241 SCD1U16V2KX-3DLGP
06/25 Need to check sequence
RSMRST_N — R1778 — PCH_RSMRST_N
H_PWRGD — R1775 — XDP_PWRGD
VCCST_PWRGD — R1777
V_CPU_ST_PLL — R79769 51R2F-2-GP
H_TDO — R79768
V1P0_PCH_S5 — R17761 150R2J-2-GP — PLTRST_CPU_N
R17711 1KR2J-1-GP — ITP_PMODE
R1770 — H_RSTOUT_XDP_N
VCC3 — R17623 — FP_RST_N
V_3P3_A — R17931 1KR2F-3-GP — PWRBTN_N
R1792 — XDP_PLTRST_N
C12242 SCD1U16V2KX-3DLGP (X_)
C12243 SCD1U16V2KX-3DLGP (R_)
V_CPU_IO — R17692 150R2F-1-GP — SKL_PCUDEBUG_0
R17663 1KR2F-3-GP — XDP_PWR_DEBUG
PCH_JTAG_TCK — R1764 — PRM_XDP_JTAG_TCK_R
SPI_IO2 — R1812 — XDP_PREQ
06/25 Allen modify

SB025 10/06 Allen modify
XDPC1 — MK1 — MK2
V1P0_CPU_XDP_S5 — R1748 0R0603-PAD — V1P0_PCH_S5
R1749 0R0603-PAD
TP135 TPAD28 — R1782 0R2J-2-GP — XDP_PCUDERBUG_3
H_PREQ_N — TP136 TPAD28
H_PRDY_N — TP137 TPAD28 — SKL_PCUDEBUG_3
SKL_PCUDEBUG_0 … SKL_PCUDEBUG_15
SKL_XDP_MBP_0 … SKL_XDP_MBP_1
SKL_PCUSTB_0_DP … SKL_PCUSTB_1_DN
XDP_PWRGD
XDP_PLTRST_N
XDP_PWR_DEBUG
XDP_VR_READY
SMB_DATA_MAIN
SMB_CLK_MAIN
PRM_XDP_JTAG_TCK_R
H_TCK
CK_100M_CPU_XDP_DP
CK_100M_CPU_XDP_DN
H_RSTOUT_XDP_N
FP_RST_N
H_TDO
H_TRST_N
H_TDI
H_TMS
XDP_PRDY
SM_DMC_CONN_GP (X_)
R1780 0R2J-2-GP (X_)
06/25 Allen modify
06/24 Allen modify
H_TRST_N — R1789 — S1R2J-2-GP (R_)
1A016 04/14 Allen modify

APS CONNECTOR

08/27 Allen modify for layout space
SLP_S4_N — R1784 — SLP_S4_N_CN — TP221 TPAD28
PCH_SLP_A_N — R1786 — SLP_A#_CN — TP222 TPAD28
SLP_S3_N — R1785 — SLP_S3_N_CN — TP223 TPAD28
PWRBTN_N — R1787 — PWRBTN_N_CN — TP224 TPAD28
FP_RST_N — R1783 — FP_RST_PCH_N_CN — TP225 TPAD28
0R402-PAD-2-GP

All parts can be placed at back side

XDP for PCH

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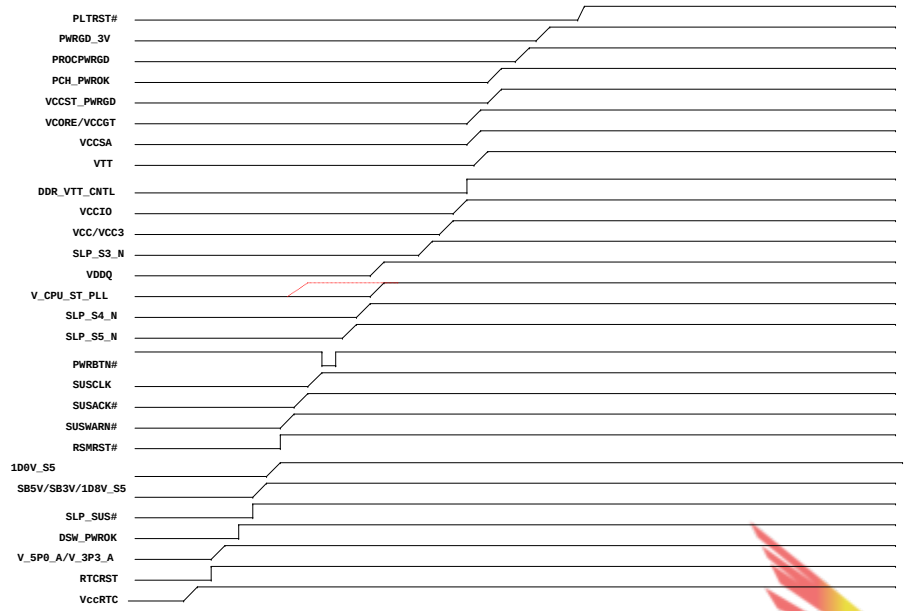
POWER ON SEQUENCE



3.3V-->NVVDD&PEX_VDD(+V_VGA_CORE&+V_1P05_VGA)-->FBVDD/Q(+V_1P5_VGA)

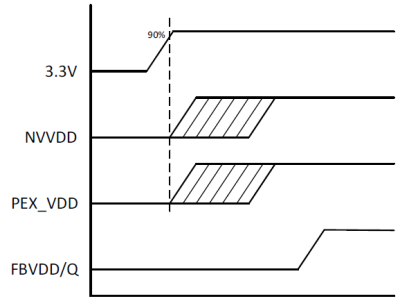


Figure 3-7. Example of Power-Up Sequencing Order

CRB	+V3_BAT (0) → RTCRST# (1) → AC_IN (2) → +V5DSW (3) → +V3p3DSW BACKFEED_CUT_N (4) → DPWROK SMC_RST# (5) →
	BAT (0) → RTCRST# (1) → AC_IN (2) → 19V (3) → V_5P0_A V_3P3_A (4) → DPWROK (5) →
CRB	SLP_SUS# (6) → +V5DUAL +V1P8A +V5A +V3p3A BACKFEED_CUT_N LATCHED_BACKFEED_CUT (7) → +VCCST_VCCSFR +V1P0A (8) → RSMRST#_PWRGD (9) → RSMRST# (10)
	SLP_SUS# (6) → SB5V SB3V V_1P8_A (7) → V_CPU_ST_PLL +V1P0A (8) → RSMRST# (9) → SUSWARN# (10) → SUSACK# (11)
CRB	→ SUSWARN# (11) → SUSACK# (12) → PWRBTN (13) → SLP_S5 SLP_S4 SLP_S3 (15) → +VCCST_VCCSFR +VCCST_VCCPLL +VPP(DDR4) (16) →
	→ PWRBTN (12) → SLP_S5 SLP_S4 SLP_S3 (13) → V_SM +VCCST_VCCSFR (14) → VCC VCC3 (15) → VCCIO_EN (16) →
CRB	FPGA_VDDQ_EN (17) → PS_ON_N +VDDQ +VDDQ_VTT (18) → +V12S +V5S +V3p3S +V12S_CPU (19) → VCCIO_EN PWRGD_VCCPLL_OC VDDQ_PWRGD_ISOLATE (20) → +VCCIO (21)
	V_CPU_IO (17) → DDR_VTT_CNTL (18) → +VDDQ_VTT (19) → VCCIO_PWRGD (20) → V_CPU_GT/V_CPU_CORE V_CPU_SA (21)
CRB	→ VCCIO_PWRGD (22) → +VCCSA (23) → VR_READY (24) → ALL_SYS_PWRGD (25) →
	→ VR_READY (22) → ALL_SYS_PWRGD (23) → PWRGD_3V (24) →
CRB	SYSPWROK (26) → PLTRST# PLTRST_CPU# (27)
	PLTRST# PLTRST_CPU# (25)

Noter:
If +VCCST_VCCSFR is only in S0, power can be controlled by slp _s4.

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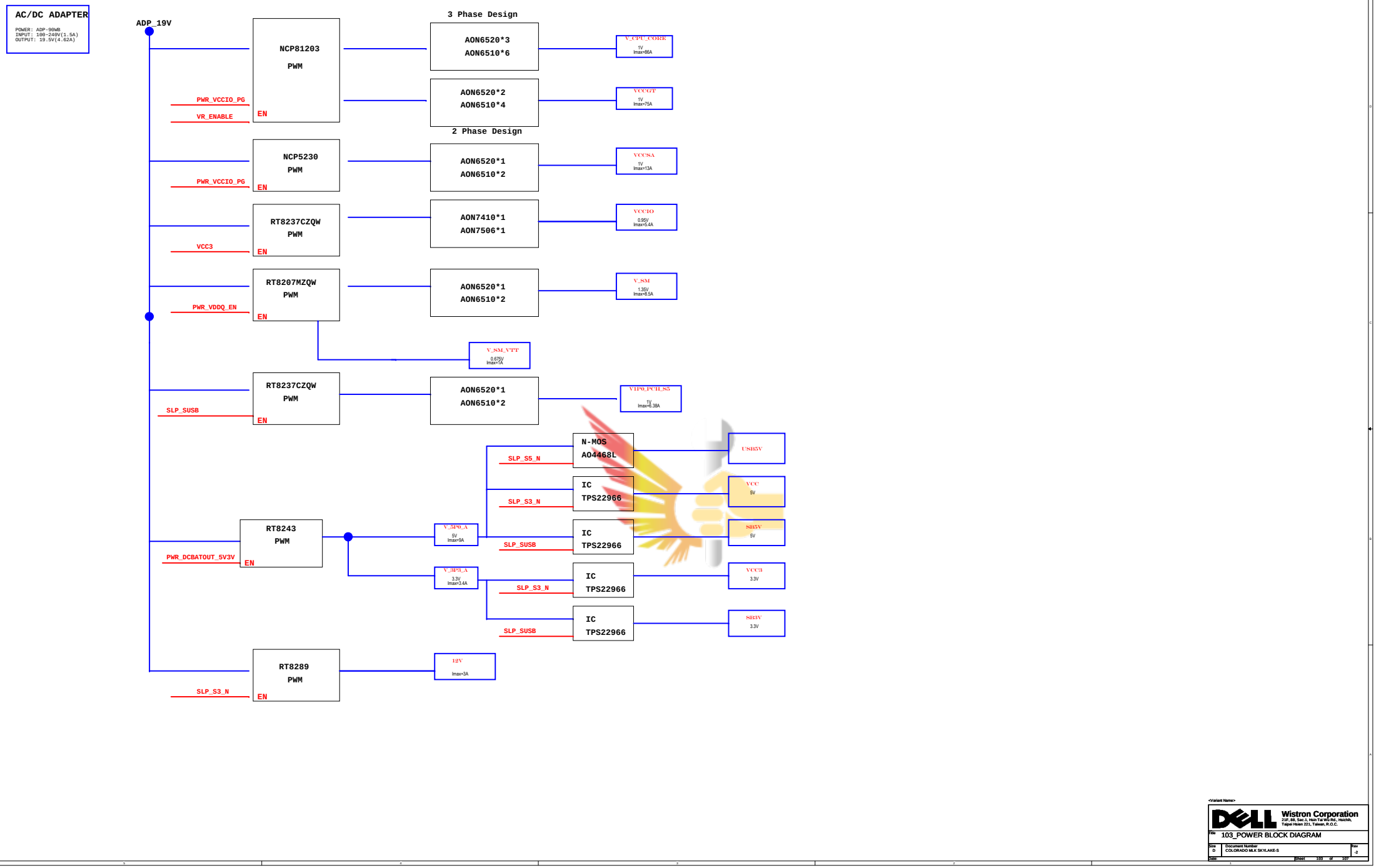

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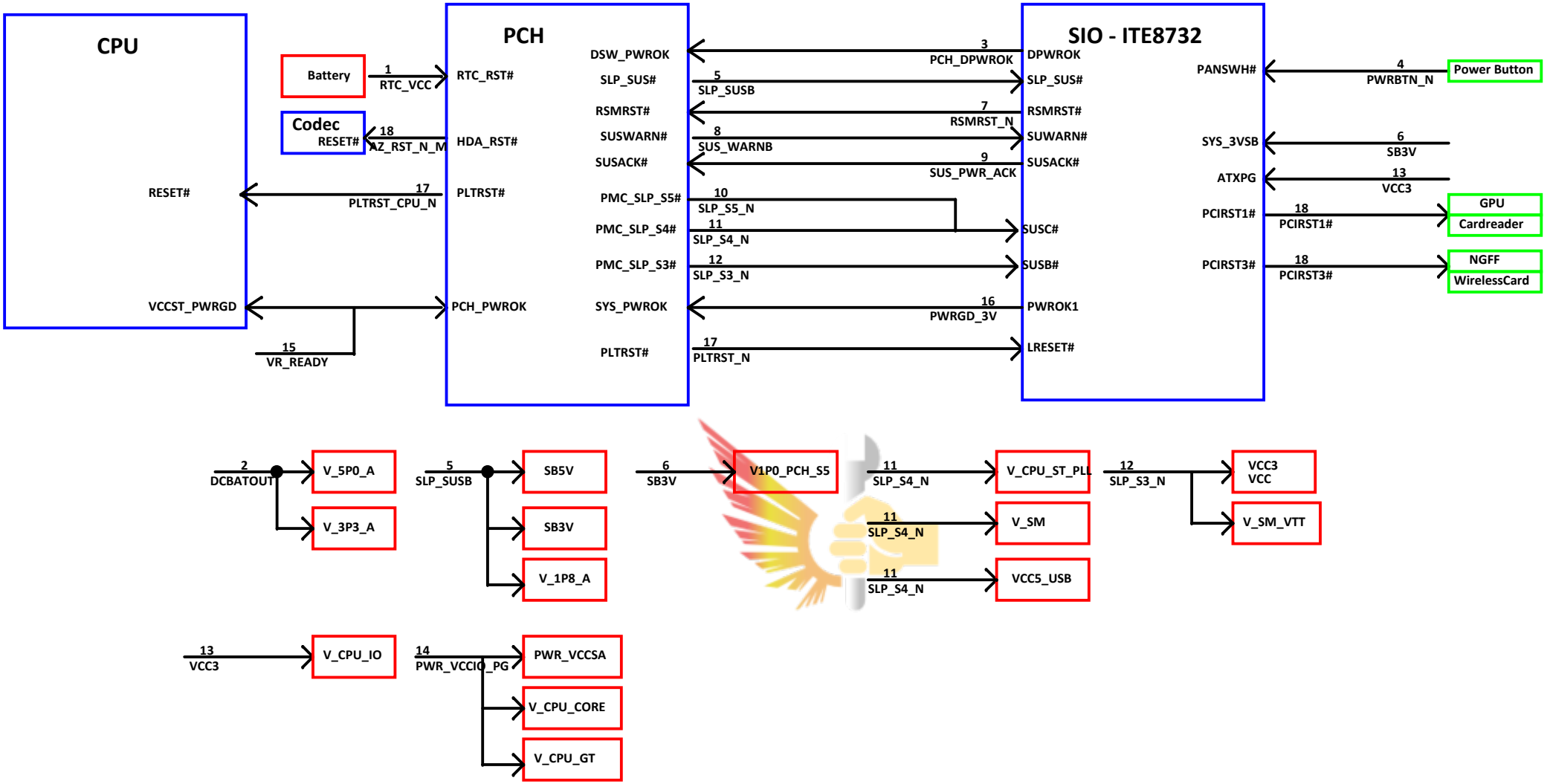

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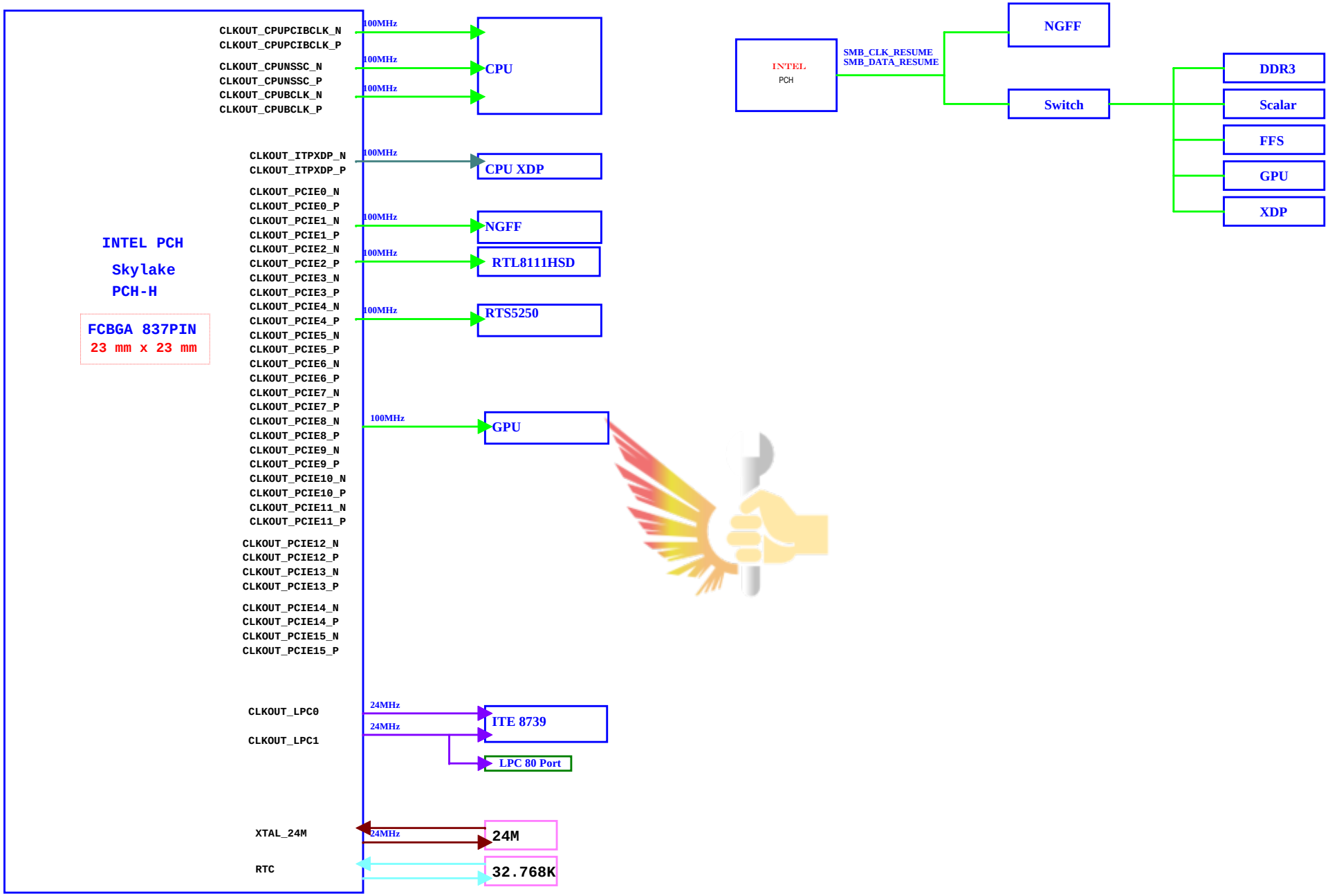

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