1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J17 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0002056619	PRODUCTION RELEASED	2013-05-30

LAST_MODIFIED=Fri May 31 13:43:58 2013

DRAWING
TITLE=J17
ABBREV=DRAWING
LAST_MODIFIED=Fri May 31 13:43:58 2013

DRAWING TITLE: SCHEM,MLB,J17

Apple Inc.

DRAWING NUMBER: 051-9884 | SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 1 OF 127
SHEET: 1 OF 106

BOM VARIANTS

BOM NUMBER	BOM NAME	BOM OPTIONS
639-4206	PCBA,MLB,GOOD,HYNIX,J17	J17_COMMON,J17,CPU:GOOD,GPU:GK107EGX,FB:2G_HYNIX,FBA,FBB,SSD:Y,EEEE:F8YL
639-4418	PCBA,MLB,GOOD,ELPIDA,J17	J17_COMMON,J17,CPU:GOOD,GPU:GK107EGX,FB:2G_ELPIDA,FBA,FBB,SSD:Y,EEEE:FCTC
985-0047	PCBA,MLB,DEV,J17	DEVELOPMENT,J17_DEVEL

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4532	1	HSW,SR14E,PRQ,C0,3.2G,84W,4+2,1.15,6M,LGA	CPU	CRITICAL	CPU:GOOD
337S4505	1	HSW,QE70,Q8,C0,3.2G,84W,4+2,1.15,6M,LGA	CPU	CRITICAL	CPU:GOOD_TDP

CPU SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0080	1	SOCKET,MOLEX,LGA1150,CPU-HF	U0500	CRITICAL	

BOM Groups

BOM GROUP	BOM OPTIONS
J17_COMMON	COMMON,ALTERNATE,J17_COMMON1,J17_PROGPARTS
J17_COMMON1	XDP,SPEAKERID,TBTHV:P12V,CPUVCC:4PHASE,EXT_GPU:YES,VDDQ:P1V5
J17_PROGPARTS	SMC:PROG,BOOTROM:PROG,TBTROM:PROG,CIVROM:PROG,CAMROM:PROG,BLCMCU:PROG
J17_DEVEL	XDP_CONN,LPCPLUS,DDRVREF_DAC
DEVEL_SENSORS	TEMPSNSDEV,AP_ISNS:Y
J17_PRODUCTION	AP_ISNS:N

ASICs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4541	1	IC,SR198,Z87,LPT-D,C2,PRQ,23X22MM,FCBGA708	U1100	CRITICAL	
337S4562	1	IC,QEWL,LPT-D,C2,8Q8,23X22MM,FCBGA708	U1100	CRITICAL	PCH_TDP
338S1113	1	IC,TBT,CR-4C,B1,PRQ,288 FCBGA,12X12MM	U2800	CRITICAL	
343S0616	1	IC,BCM57766A1,ENET&SD,8X8	U3900	CRITICAL	

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S3880	1	IC,PROGRMD,EFI ROM,V0095,J17	U5210	CRITICAL	BOOTROM:PROG
335S0807	1	IC,64 MBIT SPI SERIAL FLASH	U5210	CRITICAL	BOOTROM:BLANK
341S3874	1	IC,PROG,SMC-A3,V2.14F9,PVT,J17	U5000	CRITICAL	SMC:PROG
338S1159	1	IC,SMC,LM4FS1BH5BBCIGR,SCPL	U5000	CRITICAL	SMC:BLANK
341S3860	1	IC,EEPROM,CR,V23.10,J17	U2890	CRITICAL	TBTROM:PROG
335S0865	1	IC,EEPROM,SERIAL,8KB,MLP8	U2890	CRITICAL	TBTROM:BLANK
341S3735	1	IC,ENET 1MBIT, SPI,ROM, V1.13 J17	U3990	CRITICAL	CIVROM:PROG
335S0862	1	IC,SERIAL FLASH,2MBIT, 2.7V, REF F	U3990	CRITICAL	CIVROM:BLANK
341S3778	1	IC,CAMERA FLASH,V7230,J16/17	U4202	CRITICAL	CAMROM:PROG
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK
341S3674	1	IC,BLC,MCU, PRPOGRAMMED, V0204, D8	U8100	CRITICAL	BLCMCU:PROG
337S3978	1	IC,BLC MCU LPC2132FBD64/01, LQFP64	U8100	CRITICAL	BLCMCU:BLANK

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7896	1	LABEL,MLB,2D	EEEE_F8YL	CRITICAL	EEEE:F8YL
825-7896	1	LABEL,MLB,2D	EEEE_FCTC	CRITICAL	EEEE:FCTC

J17 SCHEMATIC / PCB #'S

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9884	1	SCH,MLB,J17	SCH1	CRITICAL	J17
820-3478	1	PCBF,MLB,J17	PCB1	CRITICAL	J17

J17 ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0147	377S0126		ALL	USB Diodes Array
377S0155	377S0104		ALL	USB Diode
157S0084	157S0058		ALL	Enet Magnetics
376S0975	376S1081		ALL	P/NCH DUAL FET
128S0365	128S0368		ALL	150UF CAPS BLK
138S0803	138S0804		ALL	2.2UF CAPS SOFT
126-0161	126-0160		ALL	56UF CAPS 10X12 THD
197S0481	197S0480		Y1950	25MHz PCH Xtal
197S0479	197S0478		ALL	12MHz Cam Xtal
372S0186	372S0185		ALL	Alt temp diode
107S0251	107S0249		R5520	Alt 2mOhm sense
107S0254	107S0241		R5450,R5480	Alt 5mOhm sense
107S0255	107S0240		R5450,R5480	Alt 1mOhm sense
341S3747	341S3735		U3990	ENET ROM,ATMEL,V1.13
138S0681	138S0638		ALL	10uF Caps
376S1106	376S0969		ALL	N-Ch FET
138S0860	138S0775		ALL	Single-source 1uF
138S0859	138S0788		ALL	Single-source 10uF

Y4200 and Y8105

GPU and VRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4430	1	IC,GPU,NV,GK107-BGX,PS-A2	U8700	CRITICAL	GPU:GK107EGX
333S0630	4	IC,GDDR5,2GBIT,64MX32,GEMMA-DIE,170B FBGA	U9200,U9250,U9300,U9350	CRITICAL	FB:2G_HYNIX
333S0695	4	IC,GDDR5,2GBIT,64MX32,H-DIE,170B FBGA	U9200,U9250,U9300,U9350	CRITICAL	FB:2G_ELPIDA

SYNC MASTER=J17 DINI SYNC DATE=02/06/2013

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BOM Configuration

Apple Inc.

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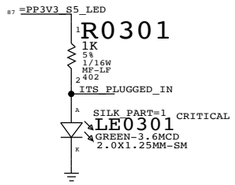
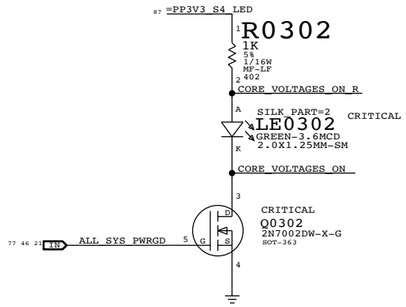
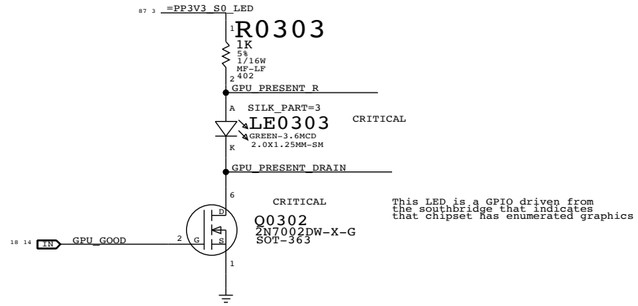
S5 Led



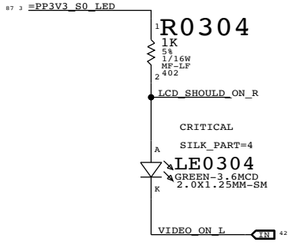
ALL_SYS_PWRGD Led



GPU GOOD Led



VIDEO ON Led



SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE

DEBUG LEDS

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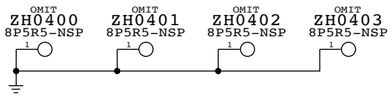
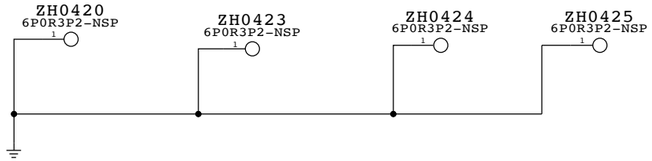
CPU Heatsink

4MM PLATED HOLES (998-4158)



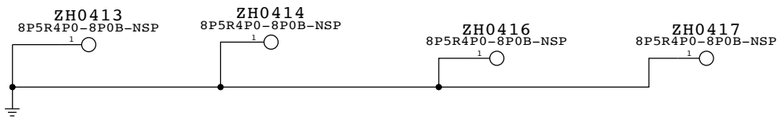
GPU HEATSINK MOUNTING FEATURES

(998-5013. PLATED HOLE, 3.2MM DIA, 6MM PAD TOP/BOT)



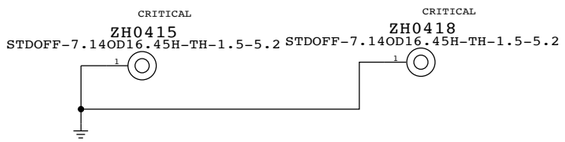
Rear Cover

998-5014 (PLATED HOLES, 4MM DRILL, 8.5MM TOP, 8MM BOT)



Rear Cover

860-1487 (PCB STANDOFF)

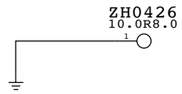


WIRELESS CARD MTG HOLES

998-4938 (PLATED HOLES, 1.9MM INNER DIAMETER, 4.3MM PAD)

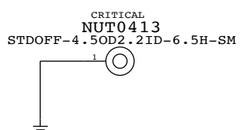
HEATPIPE MTG HOLES

998-4640 (PLATED HOLES, 10MM DIA, 12MM PAD)



SSD STANDOFF

APN: 860-1624



SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE: Holes/PD parts

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DRAWING NUMBER: 051-9884 SIZE: D

REVISION: A.0.0

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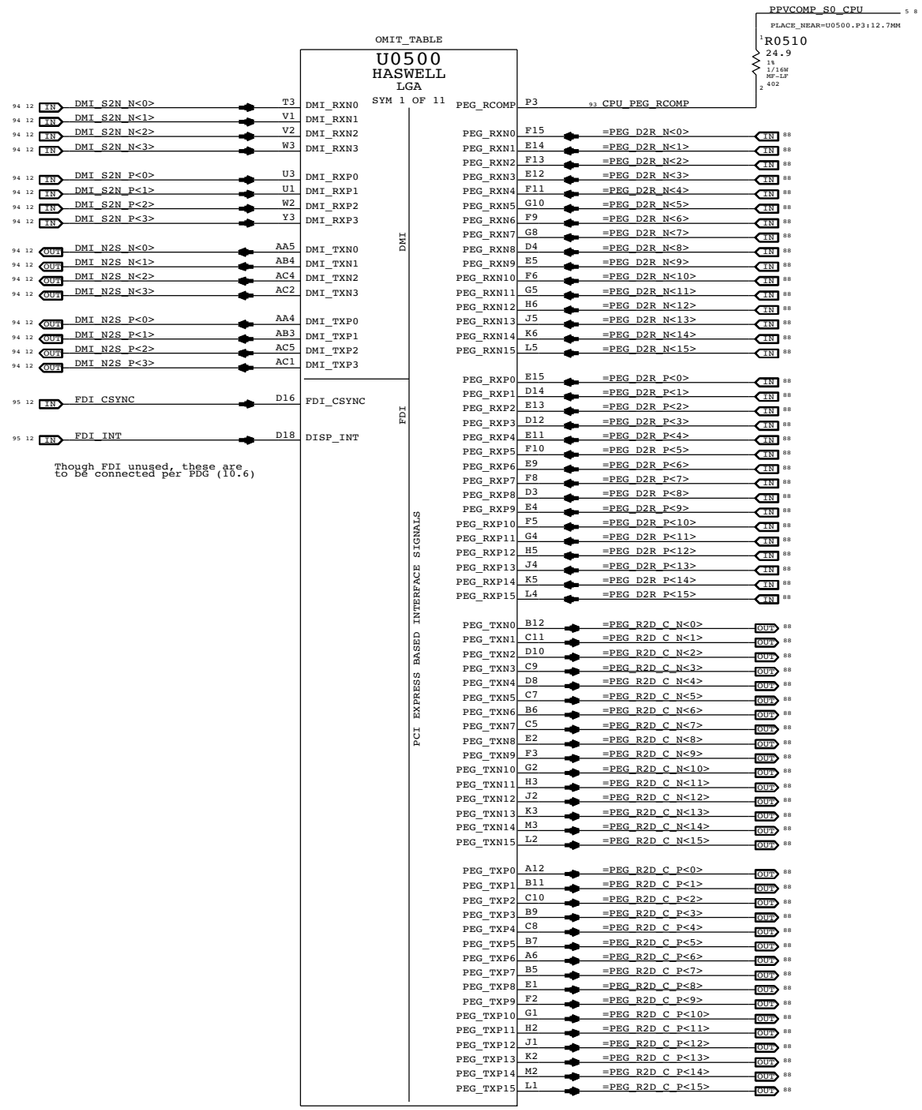

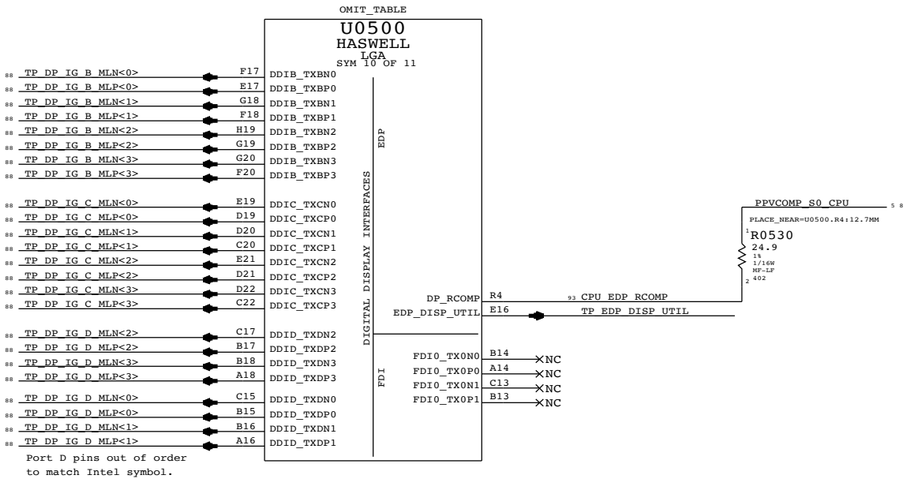

SYNC MASTER=J17 ULTIMATE | SYNC DATE=05/16/2013

PAGE TITLE

CPU DMI/PEG/FDI/RSVD

Apple Inc.

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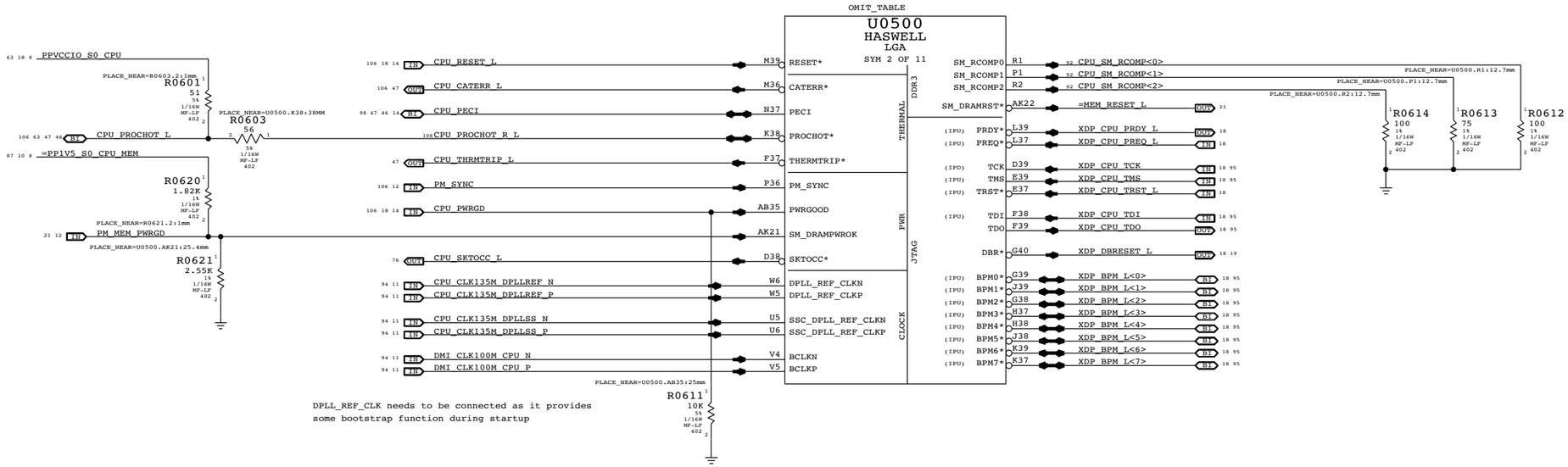
SHEET 5 OF 106



SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE

CPU Clock/Misc/JTAG/CFG

Apple Inc.

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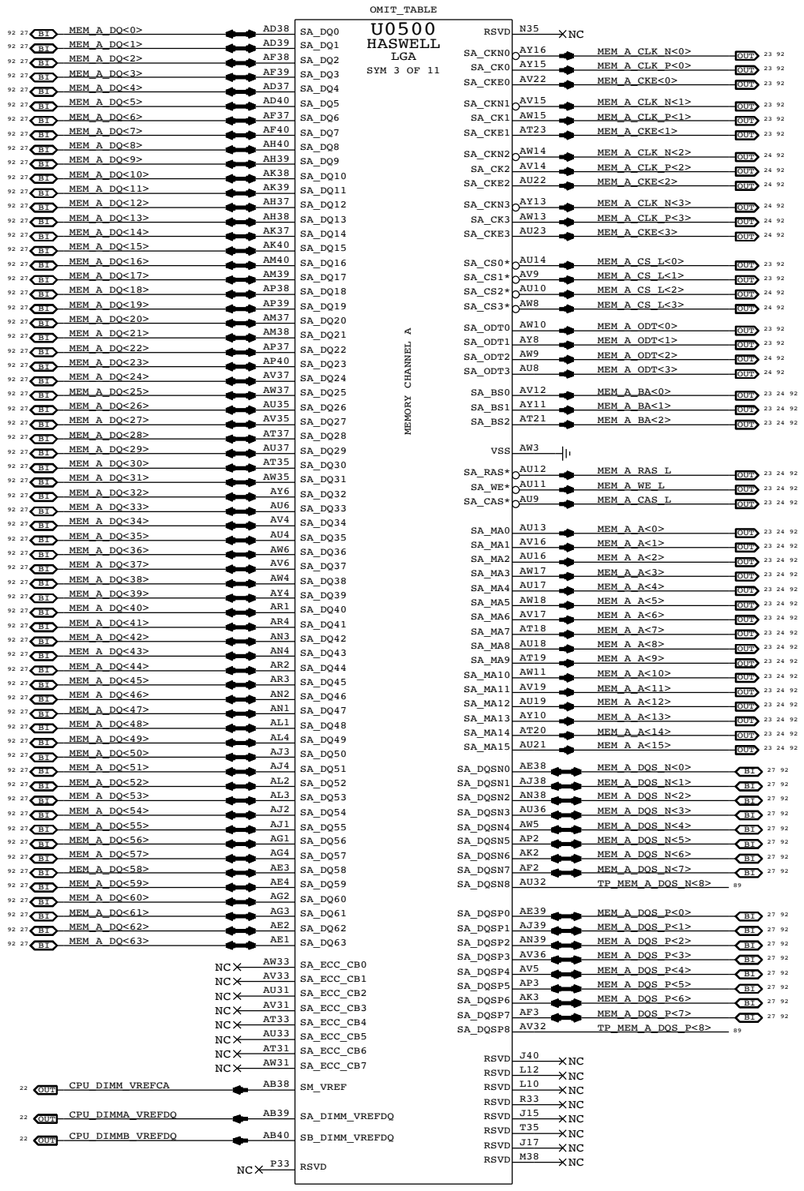

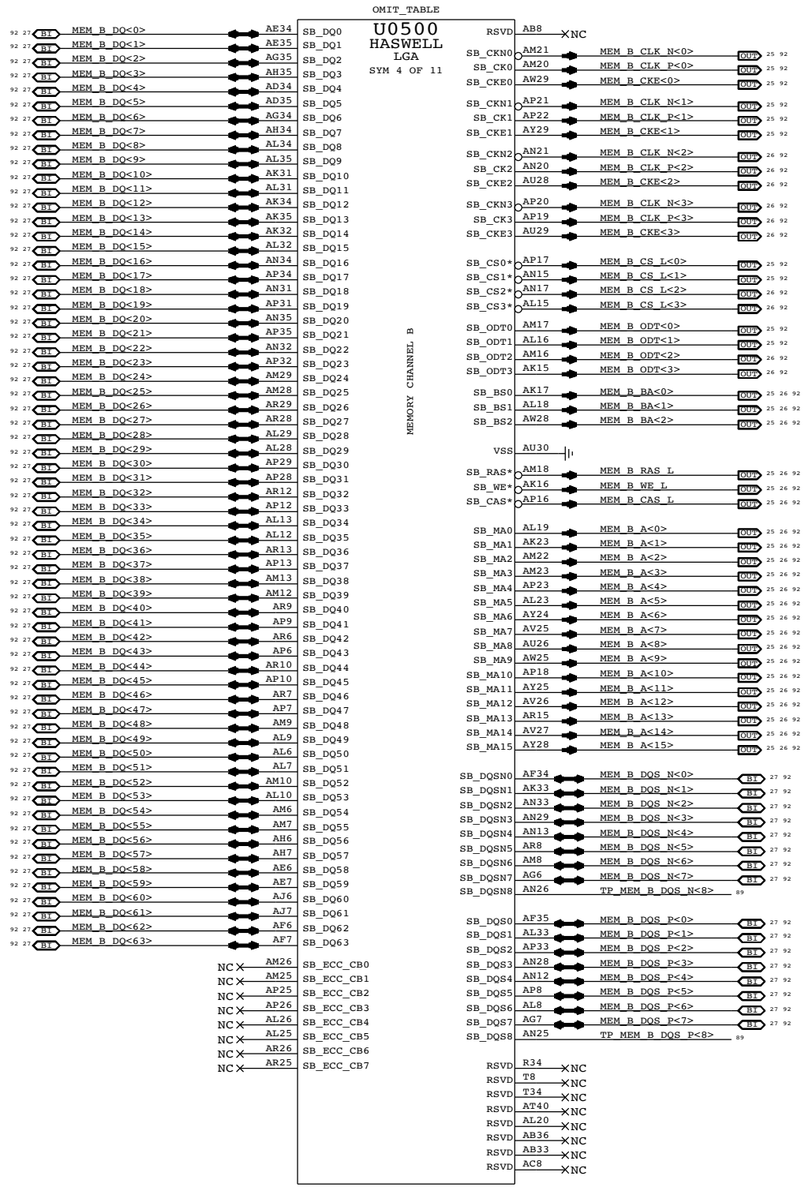

INTEL'S HASWELL DT EDS SAYS THAT ALL RSVD AND RSVD_NCTF SHOULD BE NC'D

SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

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NOTE: Aliases not used on CPU supply outputs
to avoid any extraneous connections.

63 18 6 PPVCCIO_S0_CPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
Max load: 300mA

R0801 75 1% 1/16W MF-LF 402
R0804 110 1% 1/16W MF-LF 402
Max load: 300mA

R0802 43 5% 1/16W MF-LF 402
R0803 0 5% 1/16W MF-LF 402
R0805 0 5% 1/16W MF-LF 402

100 63 IN CPU_VIDALERT_L
100 63 OUT CPU_VIDSCLK
100 63 BI CPU_VIDSOUT

R0804.2: PLACE_NEAR=U0500.C37:12.7mm
R0802.2: PLACE_NEAR=U0500.B37:12.7mm
R0801.2: PLACE_NEAR=R0802.1:25.4mm

87 10 6 =PP1V5_S0_CPU_MEM

87 63 50 10 8 6 =PPCPUVCC_S0_CPU

R0800 100 5% 1/16W MF-LF 402
PLACE_NEAR=U0500.E40:50.8mm
PLACE_SIDE=BOTTOM

100 62 OUT CPU_VCCSENSE_P

5 PPVCOMP_S0_CPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

100 CPU_VIDALERT_R_L
100 CPU_VIDSCLK_R
100 CPU_VIDSOUT_R

18 IN CPU_PWR_DEBUG

OMIT_TABLE
U0500
HASWELL
LGA
SYM 5 OF 11

NC	AW12	RSVD
NC	AW23	RSVD
NC	AW24	RSVD
NC	AW27	RSVD
	AJ12	VDDQ
	AJ13	
	AJ15	
	AJ17	
	AJ20	
	AJ21	
	AJ24	
	AJ25	
	AJ28	
	AJ29	
	AJ9	
	AT17	
	AT22	
	AU15	
	AU20	
	AU24	
	AV10	
	AV11	
	AV13	
	AV18	
	AV23	
	AV8	
	AW16	
	AY12	
	AY14	
	AY9	
NC	AU39	RSVD
	L22	VCC
	L23	VCC
NC	AU27	RSVD
NC	AU1	RSVD
	E40	VCC_SENSE
NC	AK20	RSVD
	L40	VCCIO_OUT
NC	AV24	RSVD
	P4	VCOMP_OUT
NC	AV2	RSVD
NC	AY18	RSVD
NC	AV29	RSVD
NC	AV20	RSVD
	B37	VIDALERT*
	C38	VIDSCLK
	C37	VIDSOUT
	AY5	VSS
	N40	PWR_DEBUG
	AY7	VSS
NC	AW2	RSVD
NC	AV1	RSVD
NC	A4	RSVD
NC	B3	RSVD
	B4	VSS
	AY26	VSS
	AW34	VSS
	AW32	VSS
	AY17	VSS
	AW36	VSS
	AY27	VSS
	AW26	VSS
	AY30	VSS
	AW30	VSS
	AY23	VSS
	A29	VCC
	A30	
	B25	
	B27	
	B29	
	B31	
	B33	
	B35	
	C26	
	C27	
	C24	
	C25	

=PPCPUVCC_S0_CPU 6 8 10 50 63 87

	C28	VCC
	C29	
	C30	
	C31	
	C32	
	C33	
	C34	
	C35	
	D25	
	D27	
	D29	
	D31	
	D33	
	D35	
	E24	
	E25	
	E26	
	E27	
	E28	
	E29	
	E30	
	E31	
	E32	
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	F23	
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	F35	
	G22	
	G23	
	G24	
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	G30	
	G31	
	G32	
	G33	
	G34	
	G35	
	H23	
	H25	
	H27	
	H29	
	H31	
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	H35	
	J21	
	J22	
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	J26	
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	J28	
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	J35	
	K19	
	K21	
	K23	
	K25	
	K27	
	K29	
	K31	
	K33	
	K35	
	L15	
	L16	
	L17	
	L18	
	L19	
	L20	
	L21	
FC_Y7	Y7	TP_CPU_VCCST_PWRGD
FC_K9	K9	TP_CPU_VCCST

Y7,K9 FOR FUTURE CPU COMPATIBILITY
NC FOR NOW BUT NEEDED FOR 2014 CPUS

87 63 50 10 8 6 =PPCPUVCC_S0_CPU

OMIT_TABLE
U0500
HASWELL
LGA
SYM 6 OF 11
POWER

M33	VCC
M29	
M27	
M25	
M23	
M21	
M19	
M17	
M15	
M13	
M8	
L34	
L33	
L32	
L31	
L30	
L29	
L28	
L27	
L26	
L25	
L24	
A28	
A27	
A26	
A25	
A24	

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SYNC DATE=05/16/2013
PAGE TITLE
CPU Power
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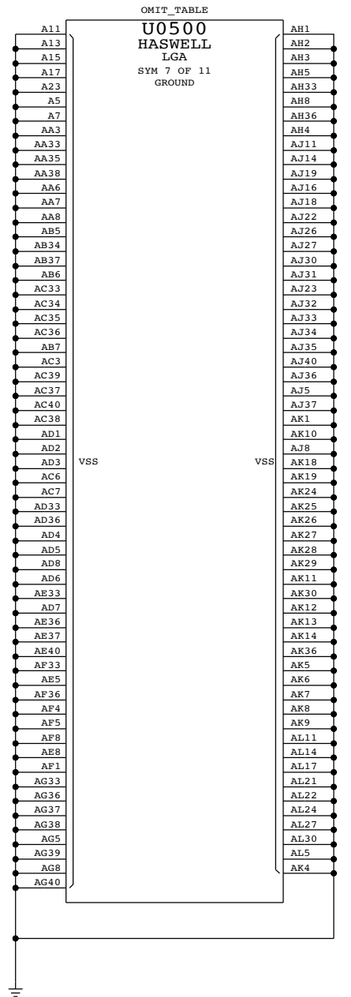

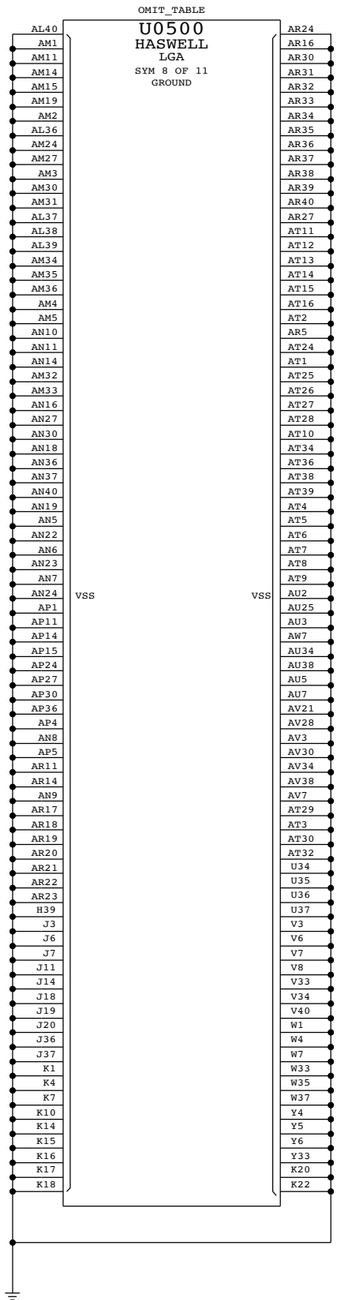

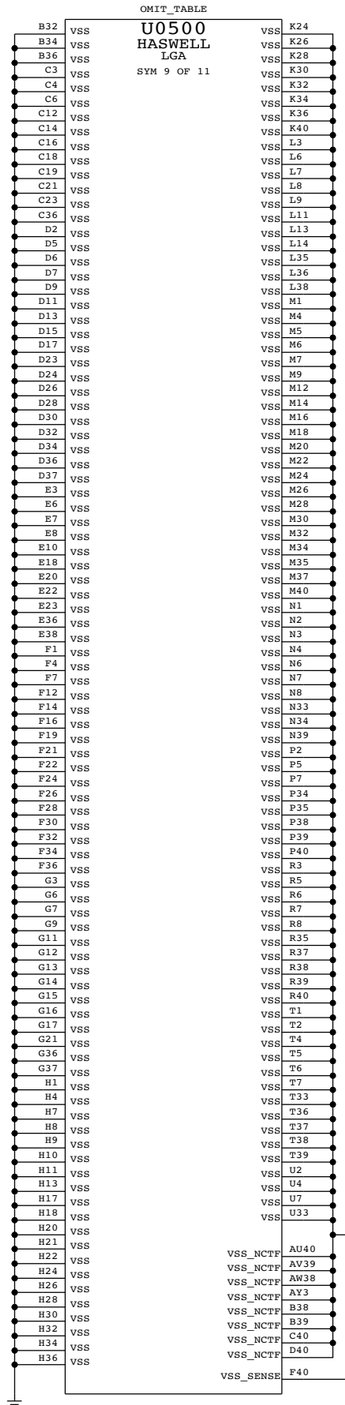

SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

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CPU Ground

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DRAWING NUMBER 051-9884 SIZE D

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CPU VCORE DECOUPLING

Intel Recommendation:22x 22UF 0805,topside (18 inside cavity, 4 north of processor),8x 470uF bulk caps(5 stuffed,3 no-stuffed)
Apple Implementation:28x 22UF 0603 per Harold
18x 10UF 0603 placed inside socket cavity

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.
BULK CAPS ON CPU VREG PAGE 71

87 63 50 8 6 =PPCPUVCC_S0_CPU

CRITICAL C1000 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1001 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1002 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1003 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1004 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1005 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1006 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1007 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1008 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1009 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1010 22UF 20% 6.3V X5R-CERM2 0603

CRITICAL C1011 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1012 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1013 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1014 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1015 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1016 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1017 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1018 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1019 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1020 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1021 22UF 20% 6.3V X5R-CERM2 0603

CRITICAL C1022 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1023 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1024 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1025 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1026 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1027 22UF 20% 6.3V X5R-CERM2 0603

ADDED CRITICAL PROPERTY TO CPU CORE DECOUPLING
DUE TO ACOUSTICS CONCERNS

CRITICAL C1030 10UF 20% 6.3V X5R 603
CRITICAL C1031 10UF 20% 6.3V X5R 603
CRITICAL C1032 10UF 20% 6.3V X5R 603
CRITICAL C1033 10UF 20% 6.3V X5R 603
CRITICAL C1034 10UF 20% 6.3V X5R 603
CRITICAL C1035 10UF 20% 6.3V X5R 603
CRITICAL C1036 10UF 20% 6.3V X5R 603
CRITICAL C1037 10UF 20% 6.3V X5R 603
CRITICAL C1038 10UF 20% 6.3V X5R 603

CRITICAL C1039 10UF 20% 6.3V X5R 603
CRITICAL C1040 10UF 20% 6.3V X5R 603
CRITICAL C1041 10UF 20% 6.3V X5R 603
CRITICAL C1042 10UF 20% 6.3V X5R 603
CRITICAL C1043 10UF 20% 6.3V X5R 603
CRITICAL C1044 10UF 20% 6.3V X5R 603
CRITICAL C1045 10UF 20% 6.3V X5R 603
CRITICAL C1046 10UF 20% 6.3V X5R 603
CRITICAL C1047 10UF 20% 6.3V X5R 603

Memory (CPU VCCDDR) DECOUPLING

Intel Recommendation:9x 22UF 0805 near CPU power pins
Apple Implementation:9x 22UF 0603 per Harold

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.

87 8 6 =PP1V5_S0_CPU_MEM

C1050 22UF 20% 6.3V X5R-CERM2 0603
C1051 22UF 20% 6.3V X5R-CERM2 0603
C1052 22UF 20% 6.3V X5R-CERM2 0603
C1053 22UF 20% 6.3V X5R-CERM2 0603
C1054 22UF 20% 6.3V X5R-CERM2 0603
C1055 22UF 20% 6.3V X5R-CERM2 0603
C1056 22UF 20% 6.3V X5R-CERM2 0603
C1057 22UF 20% 6.3V X5R-CERM2 0603
C1058 22UF 20% 6.3V X5R-CERM2 0603

NOSTUFF C1060 22UF 20% 6.3V X5R-CERM2 0603
NOSTUFF C1061 22UF 20% 6.3V X5R-CERM2 0603
NOSTUFF C1062 22UF 20% 6.3V X5R-CERM2 0603

NOSTUFF CRITICAL C1059 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

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CPU DECOUPLING

Apple Inc.

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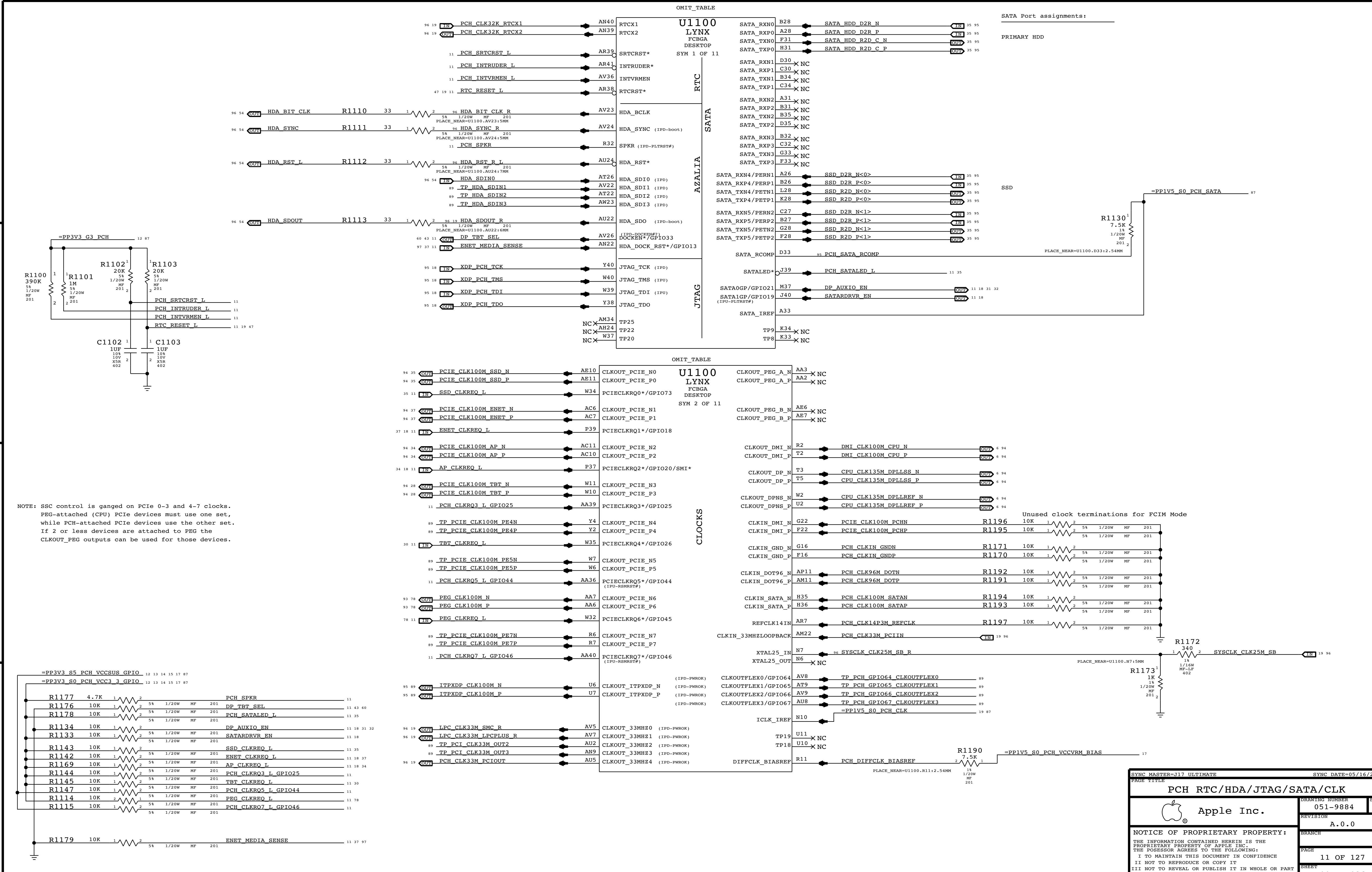
OMIT_TABLE
U1100
LYNX
FCBGA
DESKTOP
SYM 1 OF 11
RTC
SATA
AZALIA
JTAG
PCH_CLK32K_RTCX1
PCH_CLK32K_RTCX2
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L
HDA_BIT_CLK
R1110
HDA_SYNC
R1111
HDA_RST_L
R1112
HDA_SDOUT
R1113
HDA_BIT_CLK_R
HDA_SYNC_R
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
DP_TBT_SEL
ENET_MEDIA_SENSE
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
RTCX1
RTCX2
SRTCRST*
INTRUDER*
INTVRMEN
RTCRST*
HDA_BCLK
HDA_SYNC (IPD-boot)
SPKR (IPD-PLTRST#)
HDA_RST*
HDA_SDI0 (IPD)
HDA_SDI1 (IPD)
HDA_SDI2 (IPD)
HDA_SDI3 (IPD)
HDA_SDO (IPD-boot)
DOCKEN*/GPIO33
HDA_DOCK_RST*/GPIO13
JTAG_TCK (IPD)
JTAG_TMS (IPU)
JTAG_TDI (IPU)
JTAG_TDO
TP25
TP22
TP20
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
SATA_RXN2
SATA_RXP2
SATA_TXN2
SATA_TXP2
SATA_RXN3
SATA_RXP3
SATA_TXN3
SATA_TXP3
SATA_RXN4/PERN1
SATA_RXP4/PERP1
SATA_TXN4/PETN1
SATA_TXP4/PETP1
SATA_RXN5/PERN2
SATA_RXP5/PERP2
SATA_TXN5/PETN2
SATA_TXP5/PETP2
SATA_RCOMP
SATALED*
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA_IREF
TP9
TP8
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SSD_D2R_N<0>
SSD_D2R_P<0>
SSD_R2D_N<0>
SSD_R2D_P<0>
SSD_D2R_N<1>
SSD_D2R_P<1>
SSD_R2D_N<1>
SSD_R2D_P<1>
PCH_SATA_RCOMP
PCH_SATALED_L
DP_AUXIO_EN
SATARDRVR_EN
SATA Port assignments:
PRIMARY HDD
SSD
=PP1V5_S0_PCH_SATA
R1130
7.5K
PLACE_NEAR=U1100.D33:2.54MM
=PP3V3_G3_PCH
R1100
390K
R1101
1M
R1102
20K
R1103
20K
C1102
1UF
C1103
1UF
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L
OMIT_TABLE
U1100
LYNX
FCBGA
DESKTOP
SYM 2 OF 11
CLOCKS
PCIE_CLK100M_SSD_N
PCIE_CLK100M_SSD_P
SSD_CLKREQ_L
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
ENET_CLKREQ_L
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
AP_CLKREQ_L
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
PCH_CLKRQ3_L_GPIO25
TP_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P
TBT_CLKREQ_L
TP_PCIE_CLK100M_PE5N
TP_PCIE_CLK100M_PE5P
PCH_CLKRQ5_L_GPIO44
PEG_CLK100M_N
PEG_CLK100M_P
PEG_CLKREQ_L
TP_PCIE_CLK100M_PE7N
TP_PCIE_CLK100M_PE7P
PCH_CLKRQ7_L_GPIO46
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
LPC_CLK33M_SMC_R
LPC_CLK33M_LPCPLUS_R
TP_PCI_CLK33M_OUT2
TP_PCI_CLK33M_OUT3
PCH_CLK33M_PCIOUT
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
PCIECLKRQ0*/GPIO73
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
PCIECLKRQ1*/GPIO18
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
PCIECLKRQ2*/GPIO20/SMI*
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
PCIECLKRQ3*/GPIO25
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
PCIECLKRQ4*/GPIO26
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
PCIECLKRQ5*/GPIO44
CLKOUT_PCIE_N6
CLKOUT_PCIE_P6
PCIECLKRQ6*/GPIO45
CLKOUT_PCIE_N7
CLKOUT_PCIE_P7
PCIECLKRQ7*/GPIO46
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_33MHZ0
CLKOUT_33MHZ1
CLKOUT_33MHZ2
CLKOUT_33MHZ3
CLKOUT_33MHZ4
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKOUT_DPNS_N
CLKOUT_DPNS_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND_N
CLKIN_GND_P
CLKIN_DOT96_N
CLKIN_DOT96_P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_33MHZLOOPBACK
XTAL25_IN
XTAL25_OUT
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
ICLK_IREF
TP19
TP18
DIFFCLK_BIASREF
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
CPU_CLK135M_DPLLSS_N
CPU_CLK135M_DPLLSS_P
CPU_CLK135M_DPLLREF_N
CPU_CLK135M_DPLLREF_P
Unused clock terminations for FCIM Mode
PCIE_CLK100M_PCHN
PCIE_CLK100M_PCHP
PCH_CLKIN_GNDN
PCH_CLKIN_GNDP
PCH_CLK96M_DOTN
PCH_CLK96M_DOTP
PCH_CLK100M_SATAN
PCH_CLK100M_SATAP
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
SYSCLK_CLK25M_SB_R
SYSCLK_CLK25M_SB
R1196
R1195
R1171
R1170
R1192
R1191
R1194
R1193
R1197
R1172
340
R1173
1K
TP_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3
=PP1V5_S0_PCH_CLK
R1190
7.5K
=PP1V5_S0_PCH_VCCVRM_BIAS
PLACE_NEAR=U1100.R11:2.54MM
=PP3V3_S5_PCH_VCCSUS_GPIO
=PP3V3_S0_PCH_VCC3_3_GPIO
R1177
4.7K
R1176
R1178
R1134
R1133
R1143
R1142
R1169
R1144
R1145
R1147
R1114
R1115
R1179
PCH_SPKR
DP_TBT_SEL
PCH_SATALED_L
DP_AUXIO_EN
SATARDRVR_EN
SSD_CLKREQ_L
ENET_CLKREQ_L
AP_CLKREQ_L
PCH_CLKRQ3_L_GPIO25
TBT_CLKREQ_L
PCH_CLKRQ5_L_GPIO44
PEG_CLKREQ_L
PCH_CLKRQ7_L_GPIO46
ENET_MEDIA_SENSE

NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.

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PAGE TITLE

PCH RTC/HDA/JTAG/SATA/CLK

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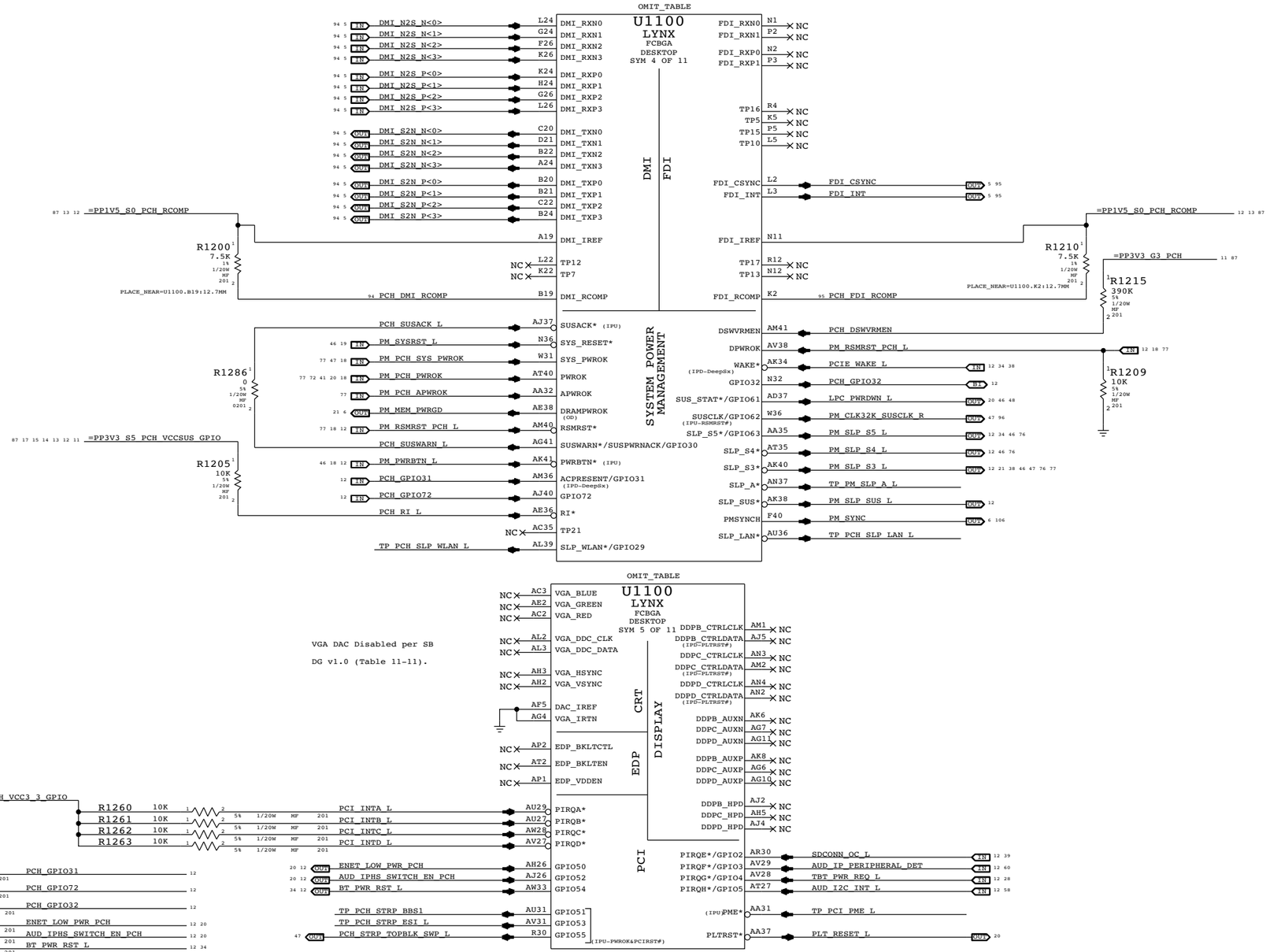

SYNC MASTER=J17 ULTIMATE
SYNC DATE=05/16/2013

PAGE TITLE

PCH DMI/FDI/PM/GFX/PCI

Apple Inc.

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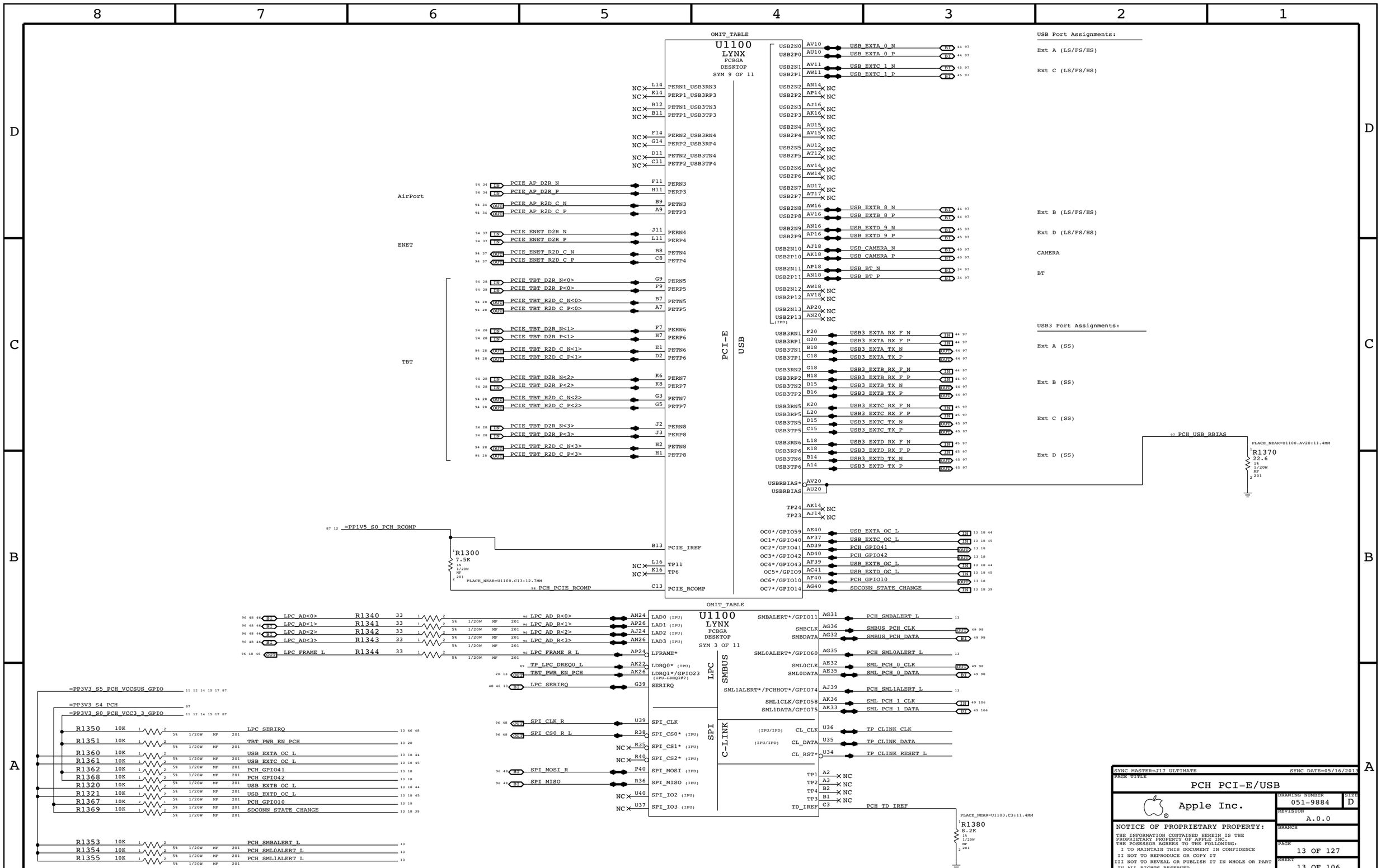
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U1100
LYNX
FCBGA
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PCI-E
USB
PERN1_USB3RN3
PERP1_USB3RP3
PETN1_USB3TN3
PETP1_USB3TP3
PERN2_USB3RN4
PERP2_USB3RP4
PETN2_USB3TN4
PETP2_USB3TP4
AirPort
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
ENET
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
TBT
PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_D2R_N<3>
PCIE_TBT_D2R_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_C_P<3>
=PP1V5_S0_PCH_RCOMP
R1300
7.5K
PLACE_NEAR=U1100.C13:12.7MM
PCH_PCIE_RCOMP
PCIE_IREF
PCIE_RCOMP
TP11
TP6
USB Port Assignments:
Ext A (LS/FS/HS)
Ext C (LS/FS/HS)
Ext B (LS/FS/HS)
Ext D (LS/FS/HS)
CAMERA
BT
USB3 Port Assignments:
Ext A (SS)
Ext B (SS)
Ext C (SS)
Ext D (SS)
USB_EXTA_0_N
USB_EXTA_0_P
USB_EXTC_1_N
USB_EXTC_1_P
USB_EXTB_8_N
USB_EXTB_8_P
USB_EXTD_9_N
USB_EXTD_9_P
USB_CAMERA_N
USB_CAMERA_P
USB_BT_N
USB_BT_P
USB3_EXTA_RX_F_N
USB3_EXTA_RX_F_P
USB3_EXTA_TX_N
USB3_EXTA_TX_P
USB3_EXTB_RX_F_N
USB3_EXTB_RX_F_P
USB3_EXTB_TX_N
USB3_EXTB_TX_P
USB3_EXTC_RX_F_N
USB3_EXTC_RX_F_P
USB3_EXTC_TX_N
USB3_EXTC_TX_P
USB3_EXTD_RX_F_N
USB3_EXTD_RX_F_P
USB3_EXTD_TX_N
USB3_EXTD_TX_P
PCH_USB_RBIAS
R1370
22.6
PLACE_NEAR=U1100.AV20:11.4MM
USBRBIAS
USBRBIAS*
TP24
TP23
USB_EXTA_OC_L
USB_EXTC_OC_L
PCH_GPIO41
PCH_GPIO42
USB_EXTB_OC_L
USB_EXTD_OC_L
PCH_GPIO10
SDCONN_STATE_CHANGE
OMIT_TABLE
U1100
LYNX
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DESKTOP
SYM 3 OF 11
LPC
SMBUS
SPI
C-LINK
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
LPC_FRAME_L
R1340
R1341
R1342
R1343
R1344
33
LPC_AD_R<0>
LPC_AD_R<1>
LPC_AD_R<2>
LPC_AD_R<3>
LPC_FRAME_R_L
TP_LPC_DREQ0_L
TBT_PWR_EN_PCH
LPC_SERIRQ
SPI_CLK_R
SPI_CS0_R_L
SPI_MOSI_R
SPI_MISO
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
CL_CLK
CL_DATA
CL_RST*
PCH_SMBALERT_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
PCH_SML0ALERT_L
SML_PCH_0_CLK
SML_PCH_0_DATA
PCH_SML1ALERT_L
SML_PCH_1_CLK
SML_PCH_1_DATA
TP_CLINK_CLK
TP_CLINK_DATA
TP_CLINK_RESET_L
TD_IREF
PCH_TD_IREF
R1380
8.2K
PLACE_NEAR=U1100.C3:11.4MM
=PP3V3_S5_PCH_VCCSUS_GPIO
=PP3V3_S4_PCH
=PP3V3_S0_PCH_VCC3_3_GPIO
R1350
R1351
R1360
R1361
R1362
R1368
R1320
R1321
R1367
R1369
R1353
R1354
R1355
10K
TBT_PWR_EN_PCH
PCH_SML0ALERT_L
PCH_SML1ALERT_L
SYNC MASTER=J17 ULTIMATE
SYNC DATE=05/16/2013
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PCH PCI-E/USB
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OMIT_TABLE

U1100
LYNX
PCBGA
DESKTOP
SYM 6 OF 11

20	IN	TBT_CIO_PLUG_EVENT_ISOL	G38 BMBUSY*/GPIO0
14		FW_PME_L	AT31 TACH1/GPIO1
14		DPMUX_UC_IRQ	AM28 TACH2/GPIO6
98 46 14	IN	SMC_RUNTIME_SCI_L	AV34 TACH3/GPIO7
36 18	OUT	HDD_PWR_EN	AC40 GPIO8 (IPU-RSMRST#)
38 14	OUT	WOL_EN	AL40 LAN_PHY_PWR_CTRL/GPIO12
14		MEM_VDD_SEL_1V5_L	AC32 GPIO15
18 14	IN	PCH_GPIO16	M39 SATA4GP/GPIO16 (IPU-Boot/SATA4GP7)
48 14	BI	LPCPLUS_GPIO	AP28 TACH0/GPIO17
20 14	OUT	JTAG_TBT_TMS_PCH	L38 SCLOCK/GPIO22
28 14	BI	TBT_GO2SX_BIDIR	AE34 GPIO24
98 46 14	IN	SMC_WAKE_SCI_L	AU34 GPIO27 (IPU-DeepSx)
27	OUT	ISOLATE_CPU_MEM_L	V41 GPIO28
30	OUT	TBT_SW_RESET_L	N34 GPIO34
18 7	OUT	GPU_GOOD	M40 GPIO35/NMI*
18 14	OUT	PCH_GPIO36	H40 SATA2GP/GPIO36 (IPD-PLTRST#)
20 18 14	OUT	JTAG_ISP_TCK	N41 SATA3GP/GPIO37 (IPD-PLTRST#)
20 14	IN	JTAG_ISP_TDO	H41 SLOAD/GPIO38
20 14	OUT	JTAG_ISP_TDI	R31 SDATAOUT0/GPIO39
14		FW_PWR_EN_PCH	L40 SDATAOUT1/GPIO48
18 14	IN	PCH_GPIO49	N40 SATA5GP/GPIO49 (IPU-Boot/SATA5GP7)
96 48	BI	SPIROM_USE_MLB	AC36 GPIO57
41	OUPT	PCH_CAM_EXT_BOOT_R_L	33.2 R1461 AT30 TACH4/GPIO68 14 PCH_CAM_EXT_BOOT_L
41	OUPT	PCH_CAM_RESET_R	33.2 R1462 AV35 TACH5/GPIO69 14 PCH_CAM_RESET
			PLACE_NEAR=U1100.AT30:10MM
			PLACE_NEAR=U1100.AV35:10MM
72 14		PCH_BLC_MCU_RESET_R	AK28 TACH6/GPIO70 (IPU-Boot?)
72 14		PCH_BLC_EXT_BOOT_R	AT34 TACH7/GPIO71 (IPU-Boot?)

CPU/MISC

GPIO

PWM0	AL31	NC
PWM1	AM31	NC
PWM2	AP31	NC
PWM3	AV30	NC
SST	AJ31	NC
TP14	N30	PCH_A20GATE 14
(IPD) PECI	G40	PCH_PECI
RCIN*	K36	PCH_RCIN_L 14
PROCPWRGD	D40	106 PCH_PROCPWRGD
THRMTRIP*	C40	PM_THRMTRIP_L_R
PLTRST_PROC*	F41	CPU_RESET_L OUT 6 18 106
VSS	AV33	
VSS	AT20	
VSS	AT21	
VSS	AT23	
VSS	AT24	
VSS	AT28	
VSS	AT29	
VSS	AT33	
VSS	AT36	
VSS	AT38	
VSS	AT41	
VSS	AT7	
VSS	AT8	
VSS	AU1	
VSS	AU3	
VSS	AU39	
VSS	AV1	
VSS	AV12	
VSS	AV17	
VSS	AV2	
VSS	AV21	
VSS	AT14	
VSS	AT15	
VSS	AT16	
VSS	AT18	

=PP1V05_S0_PCH_V_PROC_IO 15 17 87

NOSTUFF
R1457 1K 5% 1/16W MF-LF 402

NOSTUFF
R1470 43 5% 1/20W MF 201 CPU_PECI BI 6 46 47 98

R1440 0 5% 1/20W MF 0201 CPU_PWRGD OUT 6 18 106

R1456 390 5% 1/20W MF 201 PM_THRMTRIP_L IN 47 106

=PP3V3_S5_PCH_VCC5US_GPIO 11 12 13 15 17 87
=PP3V3_S0_PCH_VCC3_3_GPIO 11 12 13 15 17 87

R1485	10K	5% 1/20W MF 201	FW_PME_L 14
R1411	20K	5% 1/20W MF 201	DPMUX_UC_IRQ 14
R1496	10K	5% 1/20W MF 201	SMC_RUNTIME_SCI_L 14 46 98
R1494	10K	5% 1/20W MF 201	WOL_EN 14 38
R1489	10K	5% 1/20W MF 201	MEM_VDD_SEL_1V5_L 14
R1495	10K	5% 1/20W MF 201	PCH_GPIO16 14 18
R1490	100K	5% 1/20W MF 201	LPCPLUS_GPIO 14 48
R1412	10K	5% 1/20W MF 201	JTAG_TBT_TMS_PCH 14 20
R1492	10K	5% 1/20W MF 201	TBT_GO2SX_BIDIR 14 28
R1491	10K	5% 1/20W MF 201	SMC_WAKE_SCI_L 14 46 98
R1498	10K	5% 1/20W MF 201	PCH_GPIO36 14 18
R1413	10K	5% 1/20W MF 201	JTAG_ISP_TCK 14 18 20
R1486	10K	5% 1/20W MF 201	JTAG_ISP_TDO 14 20
R1499	10K	5% 1/20W MF 201	JTAG_ISP_TDI 14 20
R1484	10K	5% 1/20W MF 201	FW_PWR_EN_PCH 14
R1497	10K	5% 1/20W MF 201	PCH_GPIO49 14 18
R1450	10K	5% 1/20W MF 201	PCH_A20GATE 14
R1455	10K	5% 1/20W MF 201	PCH_RCIN_L 14

72 14 PCH_BLC_EXT_BOOT_R
72 14 PCH_BLC_MCU_RESET_R

R1426 1K 5% 1/20W MF 201
R1427 1K 5% 1/20W MF 201

14 PCH_CAM_EXT_BOOT_L
14 PCH_CAM_RESET

R1422 1K 5% 1/20W MF 201
R1423 1K 5% 1/20W MF 201

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SYNC DATE=05/16/2013
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PCH GPIO/MISC/NCTF

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87 17 =PP1V05_S0_PCH_VCC
VCC: 1312mA Max, 130mA Idle

V20 VCC
V22 VCC
V23 VCC
V25 VCC
W17 VCC
W19 VCC
W23 VCC
W25 VCC
AA19 VCC
AA20 VCC
AB1 VCC
AB16 VCC
AB17 VCC
AB19 VCC
AB20 VCC
AD16 VCC

17 =PP1V05_S0_PCH_VCC_CLK_F

PLACE_NEAR=R1550.1:2.54mm
PPVOUT_S5_PCH_DCPSUSBYP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

C1550
1UF
10%
6.3V
CERM
402

R1550
5.11
1%
1/20W
MF-LF
201

PLACE_NEAR=U1100.AU40:2.54MM
PPVOUT_S5_PCH_DCPSUSBYP_R
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

Powered in DeepSx

AU40 DCPSUSBYP
AU41 DCPSUSBYP

C1 VCCVRM
C2 VCCVRM
K1 VCCVRM
T14 VCCVRM

17 15 =PP1V5_S0_PCH_VCCVRM_CLK
VCCVRM: 158mA Max, 43mA Idle

87 17 15 =PP1V05_S0_PCH_VCCASW
VCCASW: 670mA Max, 34mA Idle

AF25 VCCASW
AA25 VCCASW
AA26 VCCASW
AB22 VCCASW
AB23 VCCASW
AB25 VCCASW
AB26 VCCASW
AD17 VCCASW
AD19 VCCASW
AD20 VCCASW
AD22 VCCASW
AD23 VCCASW
AD25 VCCASW

CORE
CRT
FDI
HVCMOS
USB3
PCIE/DMI
SATA
VCCMPHY

VCCADAC1_5 AF2 CKPLUS_WAIVE=PWRTERM2GND
VSS AV40 VGA DAC Disabled per LPT DG v1.0 (Table 12-18).
VCCADACBG3_3 AE1 CKPLUS_WAIVE=PWRTERM2GND

VCCVRM B39 =PP1V5_S0_PCH_VCCVRM_FDI 17
VCCVRM: 158mA Max, 43mA Idle
VCCIO AC12 =PP1V05_S0_PCH_VCCIO 15 17 87
VCCIO: 3491mA Max, 199mA Idle
VCCIO AF19 =PP1V05_S0_PCH_VCCIO_USB2 15 17 87

VCC3_3 AG1 =PP3V3_S0_PCH_VCC3_3_HVCMOS 17 87
VCC3_3: 133mA Max, 3mA Idle

DCPSUS1 AE30 NC
VCCSUS3_3 AN33 =PP3V3_S5_PCH_VCCSUS_GPIO 11 12 13 14 15 17 87
VCCSUS3_3: 261mA Max, 6mA Idle
VCCSUS3_3 P20 =PP3V3_S5_PCH_VCCSUS_USB3 87
DCPSUS3 P19 NC

VCCIO P25 =PP1V05_S0_PCH_VCCIO 15 17 87
VCCIO: 3491mA Max, 199mA Idle
VCCVRM A39 =PP1V5_S0_PCH_VCCVRM_USB3 17
VCCVRM: 158mA Max, 43mA Idle
VCCVRM A4

VCCVRM B4 =PP1V5_S0_PCH_VCCVRM_PCIE 17
VCCVRM: 158mA Max, 43mA Idle
VCCIO P23

VCCVRM A40 =PP1V5_S0_PCH_VCCVRM_SATA 17
VCCVRM: 158mA Max, 43mA Idle
VCCIO P26

VCCIO P28
VCCIO T19
VCCIO T20
VCCIO AF20 =PP1V05_S0_PCH_VCCIO_USB2 15 17 87
VCCIO AF22
VCCIO AF23

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87 17 15 =PP3V3_S5_PCH_VCCSUS_USB
VCCSUS3_3: 261mA Max, 6mA Idle

AH22 VCCSUS3_3
AJ20 VCCSUS3_3
AK20 VCCSUS3_3

87 17 15 14 13 12 11 =PP3V3_S5_PCH_VCCSUS_GPIO
AM33 VCCSUS3_3

AV41 VSS

87 17 =PP1V05_S0_PCH_VCCUSBPLL
AP22 VCCUSBPLL

87 17 =PP1V05_S0_PCH_VCCIO_FDI
M14 VCCIO

87 17 15 =PP1V05_S0_PCH_VCCIO
VCCIO: 3491mA Max, 199mA Idle
P16 VCCIO
P17 VCCIO
P22 VCCIO

NC AJ22 DCPSUS2

17 16 =PP1V5_S0_PCH_VCCVRM_CLK
VCCVRM: 158mA Max, 43mA Idle
A38 VCCVRM

87 17 =PP1V05_S0_PCH_VCCCLK_SSC
VCCCLK: 306mA Max, 89mA Idle
T16 VCCCLK

87 17 =PP3V3_S0_PCH_VCCCLK3_3
VCCCLK3_3: 55mA Max, 11mA Idle
AM9 VCCCLK3_3
AK11 VCCCLK3_3
AG12 VCCCLK3_3
AM7 VCCCLK3_3
AP5 VCCCLK3_3
AP7 VCCCLK3_3
AW3 VCCCLK3_3
AW4 VCCCLK3_3
AW9 VCCCLK3_3
AR4 VCCCLK3_3
AT5 VCCCLK3_3
AV3 VCCCLK3_3
AV4 VCCCLK3_3

V16 VCCCLK
U12 VCCCLK
V14 VCCCLK
W14 VCCCLK
W16 VCCCLK
AA16 VCCCLK
AB2 VCCCLK

87 17 =PP1V05_S0_PCH_VCCCLK_CLK100
VCCCLK: 306mA Max, 89mA Idle
87 17 =PP1V05_S0_PCH_VCCCLK_CLK135
VCCCLK: 306mA Max, 89mA Idle
87 17 =PP1V05_S0_PCH_VCCCLK_SSC100
VCCCLK: 306mA Max, 89mA Idle

USB
GPIO/LPC
HDA
RTC
CPU
SPI
CLK/MISC
THERMAL

VCCSUS3_3 AH18 =PP3V3_S5_PCH_VCCSUS_USB 15 17 87
VCCSUS3_3: 261mA Max, 6mA Idle
VCCSUS3_3 AH20
VCCDSW3_3 AV39 =PP3V3_S5_PCH_VCCDSW 17 87
VCCDSW3_3: 15mA Max, 1mA Idle
VCCDSW3_3 AW38
VCCDSW3_3 AW39

DCPSST AH28 PPVOUT_S0_PCH_DCPSST BYPASS=U1100.AH28:6.35MM
MIN_LINE_WIDTH=0.2 mm VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 mm
C1580 0.1UF 20% 10V CERM 402

VCC3_3 AF26 =PP3V3_S0_PCH_VCC_FUSE 17 87
VCC3_3 U30 =PP3V3_S0_PCH_VCC3_3_GPIO 11 12 13 14 15 17 87
VCC3_3 AW21 =PP3V3_S0_PCH_VCC3_3_USB 17 87
VCC3_3 W30 =PP3V3_S0_PCH_VCC3_3_GPIO 11 12 13 14 15 17 87
VCCIO P14 =PP1V05_S0_PCH_VCCIO 15 17 87
VCCIO: 3491mA Max, 199mA Idle

VCCSUSHDA AW26 =PP3V3_S5_PCH_VCCSUS_HDA 17 87
VCCSUSHDA: 10mA Max, 1mA Idle

VCCSUS3_3 AP35 =PP3V3_S5_PCH_VCCSUS_RTC 17 87
VCCRTC AP33
6uA Max (3.0V, room temperature)
DCPRTC AW35 PPVOUT_S0_PCH_DCPRTC BYPASS=U1100.AW35:6.35MM
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
C1590 0.1UF 20% 10V CERM 402

=PP3V3_G3_PCH_RTC 87
C1533 0.1UF 20% 10V CERM 402
C1532 0.1UF 20% 10V CERM 402
C1531 1UF 10% 6.3V CERM 402
BYPASS=U1100.AP33:6.35MM
BYPASS=U1100.AP33:6.35MM
BYPASS=U1100.AP33:6.35MM

V_PROC_IO C39 =PP1V05_S0_PCH_V_PROC_IO 14 17 87
V_PROC_IO: 4mA Max, 2mA Idle

VCCSPI R41 =PP3V3_S5_PCH_VCC_SPI 17 87
VCCSPI: 22mA Max, 1mA Idle

VCC V17 =PP1V05_S0_PCH_VCCIO 15 17 87
VCC V19

VCCASW W26 =PP1V05_S0_PCH_VCCASW 15 17 87
VCCASW: 670mA Max, 34mA Idle
VCCASW AA23 =PP1V05_S0_PCH_VCCASW 15 17 87
VCCASW: 670mA Max, 34mA Idle

VCCVRM B37 =PP1V5_S0_PCH_VCCVRM_THRM 17
VCCVRM: 158mA Max, 43mA Idle
VCC3_3 B6 =PP3V3_S0_PCH_VCC3_3_THRM 17 87
VCC3_3: 133mA Max, 3mA Idle

Current data from LPT EDS (doc #486708, Rev 1.0).

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A12	VSS	VSS	F18
A16	VSS	VSS	F24
A21	VSS	VSS	F35
A35	VSS	VSS	F37
B25	VSS	VSS	F38
B3	VSS	VSS	G2
B30	VSS	VSS	H14
B33	VSS	VSS	H16
B38	VSS	VSS	H20
B40	VSS	VSS	H22
B41	VSS	VSS	H26
C25	VSS	VSS	H28
C37	VSS	VSS	H33
C41	VSS	VSS	H34
C6	VSS	VSS	H38
D1	VSS	VSS	H4
D12	VSS	VSS	H6
D13	VSS	VSS	H8
D14	VSS	VSS	H9
D16	VSS	VSS	J31
D18	VSS	VSS	J37
D19	VSS	VSS	J5
D20	VSS	VSS	K31
D22	VSS	VSS	K4
D24	VSS	VSS	K9
D25	VSS	VSS	L37
D26	VSS	VSS	L41
D27	VSS	VSS	M16
D28	VSS	VSS	M18
D31	VSS	VSS	M20
D32	VSS	VSS	M22
D34	VSS	VSS	M24
D37	VSS	VSS	M26
D4	VSS	VSS	M28
D41	VSS	VSS	N31
D6	VSS	VSS	N35
D7	VSS	VSS	N38
D8	VSS	VSS	N4
D9	VSS	VSS	N8
E12	VSS	VSS	R1
E3	VSS	VSS	R10
E31	VSS	VSS	R34
E35	VSS	VSS	R8
E38	VSS	VSS	T17
E4	VSS	VSS	T22
E5	VSS	VSS	AW2
E7	VSS	VSS	AW30
		VSS	AW40
		VSS	AW7

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T23	VSS	VSS	AE12
T25	VSS	VSS	AE31
T26	VSS	VSS	AE4
T28	VSS	VSS	AE41
U1	VSS	VSS	AE8
U31	VSS	VSS	AF14
U32	VSS	VSS	AF16
U4	VSS	VSS	AF17
U8	VSS	VSS	AF28
V26	VSS	VSS	AF3
V28	VSS	VSS	AG2
V38	VSS	VSS	AG30
V40	VSS	VSS	AG34
W12	VSS	VSS	AG38
W20	VSS	VSS	AG8
W22	VSS	VSS	AH14
W28	VSS	VSS	AH16
W3	VSS	VSS	AJ1
W5	VSS	VSS	AJ28
W8	VSS	VSS	AK24
Y1	VSS	VSS	AK37
Y41	VSS	VSS	AK9
AA10	VSS	VSS	AL11
AA11	VSS	VSS	AL37
AA12	VSS	VSS	AL5
AA14	VSS	VSS	AM14
AA17	VSS	VSS	AM16
AA22	VSS	VSS	AM18
AA28	VSS	VSS	AM20
AA30	VSS	VSS	AM24
AA34	VSS	VSS	AM26
AA5	VSS	VSS	AM35
AA8	VSS	VSS	AM38
AB14	VSS	VSS	AM4
AB28	VSS	VSS	AM6
AB4	VSS	VSS	AM8
AC30	VSS	VSS	AN28
AC31	VSS	VSS	AP4
AC34	VSS	VSS	AP9
AC38	VSS	VSS	AR11
AC5	VSS	VSS	AR35
AC8	VSS	VSS	AR37
AD14	VSS	VSS	AT1
AD26	VSS	VSS	AT10
AD28	VSS	VSS	AT11

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR) INTEL:1X 0.1UF(402)
87 15 =PP3V3_S5_PCH_VCCDSW
15mA Max, 1mA Idle
C1700 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.AW39:6.35MM

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR) INTEL:1X 1UF(402)
87 15 =PP3V3_S5_PCH_VCC_SPI
22mA Max, 1mA Idle
C1702 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.R41:6.35MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR) INTEL:1X 0.1UF(402)
87 15 14 13 12 11 =PP3V3_S5_PCH_VCCSUS_GPIO
261mA Max, 6mA Idle
C1704 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.AN33:6.35MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR) INTEL:1X 0.1UF(402)
87 15 =PP3V3_S5_PCH_VCCSUS_USB
261mA Max, 6mA Idle
C1706 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.AK20:6.35MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V DSW RTC PWR) INTEL:1X 1UF(402)
87 15 =PP3V3_S5_PCH_VCCSUS_RTC
C1708 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AP35:6.35MM

PCH VCCCLK3_3 BYPASS 55mA Max, 11mA Idle
(PCH 3.3V CLK PWR) INTEL:4X 1UF(402)
87 15 =PP3V3_S0_PCH_VCCCLK3_3
C1720 1 1UF 10% 6.3V CERM 402 2
C1721 1 1UF 10% 6.3V CERM 402 2
C1722 1 1UF 10% 6.3V CERM 402 2
C1723 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AP5:6.35MM
BYPASS=U1100.AV4:6.35MM
BYPASS=U1100.AR4:6.35MM
BYPASS=U1100.AT5:6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR) INTEL:1X 0.1UF(402)
87 15 =PP3V3_S0_PCH_VCC3_3_HVCMOS
133mA Max, 3mA Idle
C1726 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.AG1:6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR) INTEL:1X 0.1UF(402)
87 15 14 13 12 11 =PP3V3_S0_PCH_VCC3_3_GPIO
133mA Max, 3mA Idle
C1728 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.W30:6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR) INTEL:1X 1UF(402)
87 15 =PP3V3_S0_PCH_VCC3_3_USB
133mA Max, 3mA Idle
C1730 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AW21:6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR) INTEL:1X 0.1UF(402)
87 15 =PP3V3_S0_PCH_VCC3_3_THRM
133mA Max, 3mA Idle
C1732 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.B6:6.35MM

PCH VCC BYPASS
(PCH 3.3V FUSE PWR) INTEL:1X 1UF(402)
87 15 =PP3V3_S0_PCH_VCC_FUSE
133mA Max, 3mA Idle
C1734 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AP26:6.35MM

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR) INTEL:1X10UF(805), 1X1UF(402)
87 15 =PP1V05_S0_PCH_VCCASW
670mA Max, 34mA Idle
C1750 1 10UF 20% 6.3V X5R 603 2
C1751 1 1UF 10% 6.3V CERM 402 2
C1752 1 1UF 10% 6.3V CERM 402 2
place_near=U1100.AD17:2.54MM
place_near=U1100.AD17:2.54MM
place_near=U1100.AD19:2.54MM

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
87 15 =PP1V05_S0_PCH_VCC
1312mA Max, 130mA Idle
THESE 4X1UF ARE EXTRA BYPASS
C1761 1 1UF 10% 6.3V CERM 402 2
C1756 1 1UF 10% 6.3V CERM 402 2
C1757 1 1UF 10% 6.3V CERM 402 2
C1758 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.P14:6.35MM
BYPASS=U1100.V22:6.35MM
BYPASS=U1100.V25:6.35MM
BYPASS=U1100.AA19:6.35MM

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR) INTEL:2X10UF(805), 3X1UF(402)
87 15 =PP1V05_S0_PCH_VCCIO
3491mA Max, 114mA Idle
C1760 1 10UF 20% 6.3V X5R 603 2
C1755 1 10UF 20% 6.3V X5R 603 2
C1762 1 1UF 10% 6.3V CERM 402 2
C1763 1 1UF 10% 6.3V CERM 402 2
C1764 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.P14:12.7MM
BYPASS=U1100.P28:12.7MM
BYPASS=U1100.P16:6.35MM
BYPASS=U1100.P17:6.35MM
BYPASS=U1100.P26:6.35MM

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR) INTEL:1X 1UF(402)
87 15 =PP1V05_S0_PCH_VCCUSBPLL
C1770 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AP22:6.35MM

PCH VCCIO BYPASS
(PCH 1.05V FDI PWR) INTEL:1X 1UF(402)
87 15 =PP1V05_S0_PCH_VCCIO_FDI
3491mA Max, 114mA Idle
C1772 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.M14:6.35MM

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR) INTEL:1X 1UF(402)
87 15 =PP1V05_S0_PCH_VCCIO_USB2
3491mA Max, 114mA Idle
C1774 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AF19:6.35MM

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR) INTEL:1X1UF(603), 2X0.1UF(402)
87 15 14 =PP1V05_S0_PCH_V_PROC_IO
4mA Max, 2mA Idle
C1785 1 1UF 10% 6.3V CERM 402 2
C1786 1 0.1UF 20% 10V CERM 402 2
C1787 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.C39:12.7MM
BYPASS=U1100.C39:6.35MM
BYPASS=U1100.C39:6.35MM

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR) INTEL:2X 1UF(402)
87 15 =PP1V05_S0_PCH_VCCCLK_SSC100
306mA Max, 89mA Idle
C1776 1 1UF 10% 6.3V CERM 402 2
C1777 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AA16:6.35MM
BYPASS=U1100.W16:6.35MM

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK PWR) INTEL:2X 1UF(402)
87 15 =PP1V05_S0_PCH_VCCCLK_CLK100
306mA Max, 89mA Idle
C1778 1 1UF 10% 6.3V CERM 402 2
C1783 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.U12:6.35MM
BYPASS=U1100.AB2:6.35MM

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK135 PWR) INTEL:1X 1UF(402)
87 15 =PP1V05_S0_PCH_VCCCLK_CLK135
306mA Max, 89mA Idle
C1780 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.W14:6.35MM

PCH VCCCLK BYPASS
(PCH 1.05V SSC PWR) INTEL:1X 1UF(402)
87 15 =PP1V05_S0_PCH_VCCCLK_SSC
306mA Max, 89mA Idle
C1782 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.V16:6.35MM

PCH VCCSUSHDA BYPASS
(PCH 3.3V HDA PWR) INTEL:1X 0.1UF(402)
87 15 =PP3V3_S5_PCH_VCCSUS_HDA
10mA Max, 1mA Idle
C1710 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.AW26:6.35MM

PCH VCCVRM BYPASS
(PCH 1.5V VCCVRM PWR) INTEL:1X 0.1UF(402)
87 =PP1V5_S0_PCH_VCCVRM
158mA Max, 43mA Idle
11 =PP1V5_S0_PCH_VCCVRM_BIAS
15 =PP1V5_S0_PCH_VCCVRM_FDI
15 =PP1V5_S0_PCH_VCCVRM_USB3
15 =PP1V5_S0_PCH_VCCVRM_PCIE
15 =PP1V5_S0_PCH_VCCVRM_SATA
15 =PP1V5_S0_PCH_VCCVRM_CLK
15 =PP1V5_S0_PCH_VCCVRM_THRM
C1740 1 0.1UF 20% 16V CERM 603 2
BYPASS=U1100.T14:12.7MM

PCH_CLK VCC BYPASS INTEL:1X10UF(603), 1X1UF(402)
(PCH 1.05V CLK PLL PWR. NOSTUFF 10UF IF IDG NO USED)
87 =PP1V05_S0_PCH_VCC_CLK
306mA Max, 89mA Idle
L1790 0 5% 1/10W MF-LF 603 1 2
15 PP1V05_S0_PCH_VCC_CLK_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
C1790 1 NOSTUFF 10UF 20% 6.3V X5R 603 2
C1791 1 1UF 10% 10V X5R 402
BYPASS=U1100.AB1:12.7MM
BYPASS=U1100.AB1:6.35MM

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013
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PCH DECOUPLING

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Extra BPM Testpoints

XDP_BPM_L<2>	TP1802	TP-P6
XDP_BPM_L<3>	TP1803	TP-P6
XDP_BPM_L<4>	TP1804	TP-P6
XDP_BPM_L<5>	TP1805	TP-P6
XDP_BPM_L<6>	TP1806	TP-P6
XDP_BPM_L<7>	TP1807	TP-P6

CPU Micro2-XDP

PPVCCIO_S0_CPU

=PP1V05_S0_XDP

R1830 150 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_CPU_PREQ_L	OBSFN_A0	OBSFN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSFN_A1	OBSFN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSFN_B0	OBSFN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSFN_B1	OBSFN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_VR_READY	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_CPU_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	XDP_CPU_TRST_L
	TCK1	TDI	XDP_CPU_TDI
XDP_CPU_TCK	TCK0	TMS	XDP_CPU_TMS
	NC	XDP_PRESENT#	

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XDP_CPU_PRESENT_L

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

NC per Intel DPDG.

XDP R1831 1K 5% 1/16W MF-LF 402

XDP C1804 0.1UF 20% 10V CERM 402

XDP C1800 0.1UF 20% 10V CERM 402

XDP C1801 0.1UF 20% 10V CERM 402

XDP C1806 0.1UF 20% 10V CERM 402

XDP R1805 1K 5% 1/20W MF 201 — CPU_RESET_L

XDP R1800 1K 5% 1/20W MF 201 — CPU_PWRGD (PLACE_NEAR=U0500.AB35:16.5mm)

XDP R1802 0 5% 1/20W MF 0201 — PM_PWRBTN_L

WF: SB DPDG says HOOK1 is BP_PWRGD_RST#

XDP R1804 220 5% 1/20W MF 201 — PM_PCH_SYS_PWROK

CPU-PCH JTAG Chain Support

To link CPU and PCH JTAG pull ICT_JTAG_EN to 5V (must be in S0)

TP1845 TP-P6 — ICT_JTAG_EN

TP1840 TP-P6 — XDP_CPU_PCH_TMS (PLACE_NEAR=J1800.57:5.08mm)

TP1841 TP-P6 — XDP_CPU_PCH_TCK (PLACE_NEAR=J1800.58:5.08mm)

XDP_CPU_TDO_PCH_TDI (PLACE_NEAR=J1800.51:5.08mm)

Q1840 DMN5L06VK-7 SOT-563

Q1842 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3

Q1846 DMN5L06VK-7 SOT-563

Q1848 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3

XDP_PCH_TMS (PLACE_NEAR=J1850.57:6mm)

XDP_PCH_TCK (PLACE_NEAR=J1850.58:5.08mm)

XDP_PCH_TDI (PLACE_NEAR=J1850.55:5.08mm)

R1842 1M 5% 1/20W MF 201

R1841 1M 5% 1/20W MF 201

R1840 1M 5% 1/20W MF 201

R1845 1K 5% 1/20W MF 201

XDP SIGNALS

PCH SIGNALS

		OMIT (All 18 R's)		
USB_EXTA_OC_L	R1890	SHORT	XDP_DA0_USB_EXTA_OC_L	
USB_EXTC_OC_L	R1893	SHORT	XDP_DA1_USB_EXTC_OC_L	
PCH_GPIO41	R1894	SHORT	XDP_DA2_PCH_GPIO41	
PCH_GPIO42	R1895	SHORT	XDP_DA3_PCH_GPIO42	
USB_EXTB_OC_L	R1880	SHORT	XDP_DB0_USB_EXTB_OC_L	
USB_EXTD_OC_L	R1881	SHORT	XDP_DB1_USB_EXTD_OC_L	
PCH_GPIO10	R1896	SHORT	XDP_DB2_PCH_GPIO10	
SDCONN_STATE_CHANGE	R1897	SHORT	XDP_DB3_SDCONN_STATE_CHANGE_L	
DP_AUXIO_EN	R1872	SHORT	XDP_DC0_DP_AUXCH_ISOL_L	
SATARDRVR_EN	R1873	SHORT	XDP_DC1_SATARDRVR_EN	
PCH_GPIO36	R1874	SHORT	XDP_DC2_PCH_GPIO36	
JTAG_ISP_TCK	R1875	SHORT	XDP_DC3_JTAG_ISP_TCK	
PCH_GPIO16	R1878	SHORT	XDP_DD0_PCH_GPIO16	
PCH_GPIO49	R1879	SHORT	XDP_DD1_PCH_GPIO49	
ENET_CLKREQ_L	R1882	SHORT	XDP_DD2_ENET_CLKREQ_L	
AP_CLKREQ_L	R1883	SHORT	XDP_DD3_AP_CLKREQ_L	
HDD_PWR_EN	R1886	SHORT	XDP_FC0_HDD_PWR_EN	
GPU_GOOD	R1887	SHORT	XDP_FC1_GPU_GOOD	

PCH Micro2-XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J1850
DF40RC-60DP-0.4V
M-ST-SM

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

	OBSFN_A0	OBSFN_C0	XDP_FC0_HDD_PWR_EN
	OBSFN_A1	OBSFN_C1	XDP_FC1_GPU_GOOD
XDP_DA0_USB_EXTA_OC_L	OBSDATA_A0	OBSDATA_C0	XDP_DC0_DP_AUXCH_ISOL_L
XDP_DA1_USB_EXTC_OC_L	OBSDATA_A1	OBSDATA_C1	XDP_DC1_SATARDRVR_EN
XDP_DA2_PCH_GPIO41	OBSDATA_A2	OBSDATA_C2	XDP_DC2_PCH_GPIO36
XDP_DA3_PCH_GPIO42	OBSDATA_A3	OBSDATA_C3	XDP_DC3_JTAG_ISP_TCK
	OBSFN_B0	OBSFN_D0	
	OBSFN_B1	OBSFN_D1	
XDP_DB0_USB_EXTB_OC_L	OBSDATA_B0	OBSDATA_D0	XDP_DD0_PCH_GPIO16
XDP_DB1_USB_EXTD_OC_L	OBSDATA_B1	OBSDATA_D1	XDP_DD1_PCH_GPIO49
XDP_DB2_PCH_GPIO10	OBSDATA_B2	OBSDATA_D2	XDP_DD2_ENET_CLKREQ_L
XDP_DB3_SDCONN_STATE_CHANGE_L	OBSDATA_B3	OBSDATA_D3	XDP_DD3_AP_CLKREQ_L
XDP_PCH_S5_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	
XDP_PCH_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	
	VCC_OBS_AB	VCC_OBS_CD	
	HOOK2	RESET#/HOOK6	XDP_PM_PCH_PWROK
	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_PCH_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	TP_XDP_PCH_TRST_L
	TCK1	TDI	XDP_PCH_TDI
XDP_PCH_TCK	TCK0	TMS	XDP_PCH_TMS
	NC	XDP_PRESENT#	

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NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP C1880 0.1UF 20% 10V CERM 402

XDP C1881 0.1UF 20% 10V CERM 402

XDP R1870 1K 5% 1/20W MF 201 — PM_PCH_PWROK

XDP R1892 0 5% 1/16W MF-LF 402 NOSTUFF — =PP3V3_S5_XDP → PP3V3_S5_XDP_R (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.15MM, MAX_NECK_LENGTH=3MM)

XDP R1860 210 1% 1/20W MF 201 — XDP_PCH_TDO (J1850.51:2.54mm)

XDP R1861 210 1% 1/20W MF 201 — XDP_PCH_TDI (U1100.W39:4mm)

XDP R1862 210 1% 1/20W MF 201 — XDP_PCH_TMS (U1100.W40:3.5mm)

XDP_PCH_TCK

XDP R1867 100 5% 1/20W MF 201 — J1850.51:5mm

XDP R1868 100 5% 1/20W MF 201 — U1100.W39:21MM

XDP R1869 100 5% 1/20W MF 201 — U1100.W40:20MM

XDP R1866 51 5% 1/20W MF 201

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

XDP R1884 1K 5% 1/20W MF 201 — PM_RSMRST_PCH_L (PLACE_NEAR=J1850.40:2.54mm)

XDP R1885 0 5% 1/20W MF 0201 — PM_PWRBTN_L (PLACE_NEAR=U5000.J3:2.54mm)

XDP R1820 51 5% 1/20W MF 201 — XDP_CPU_TDO (PLACE_NEAR=J1800.51:5MM)

XDP R1823 51 5% 1/20W MF 201 — XDP_CPU_TCK

XDP R1824 51 5% 1/20W MF 201 — XDP_CPU_TRST_L

TDI and TMS are terminated in CPU.

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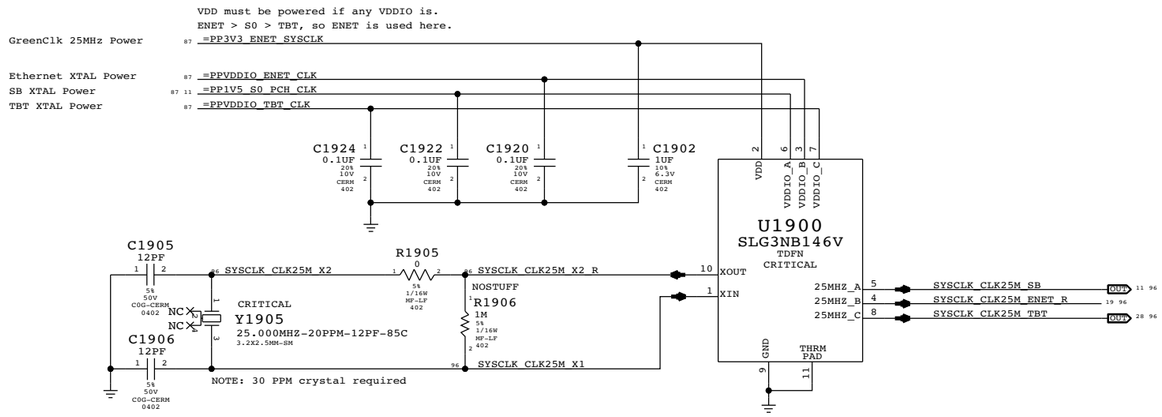
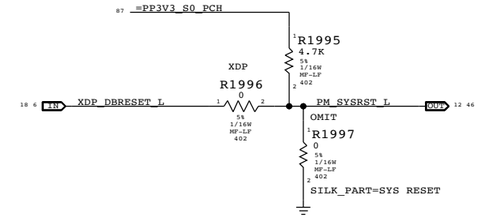
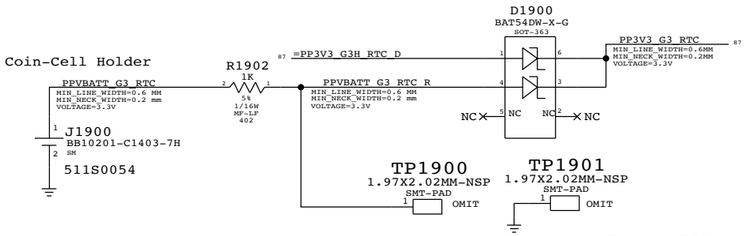
System 25MHz Clock Generator



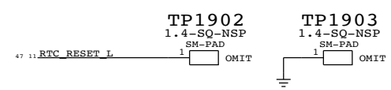
PCH Reset Button



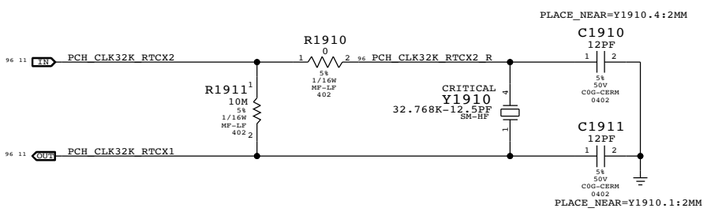
RTC Power Sources



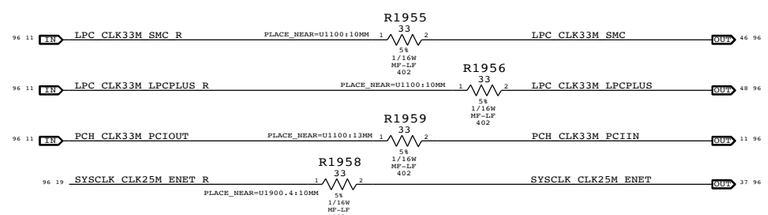
Place TP1901-TP1903 on bottom side



PCH RTC Crystal

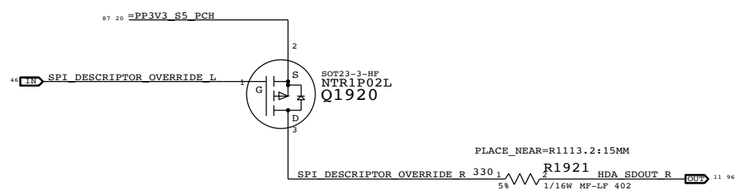


Clock series termination



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.



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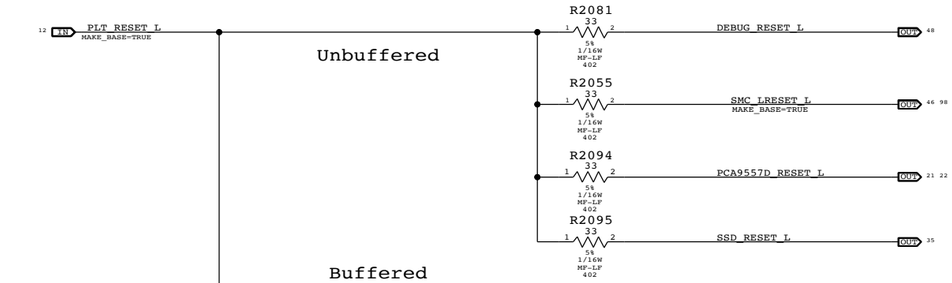
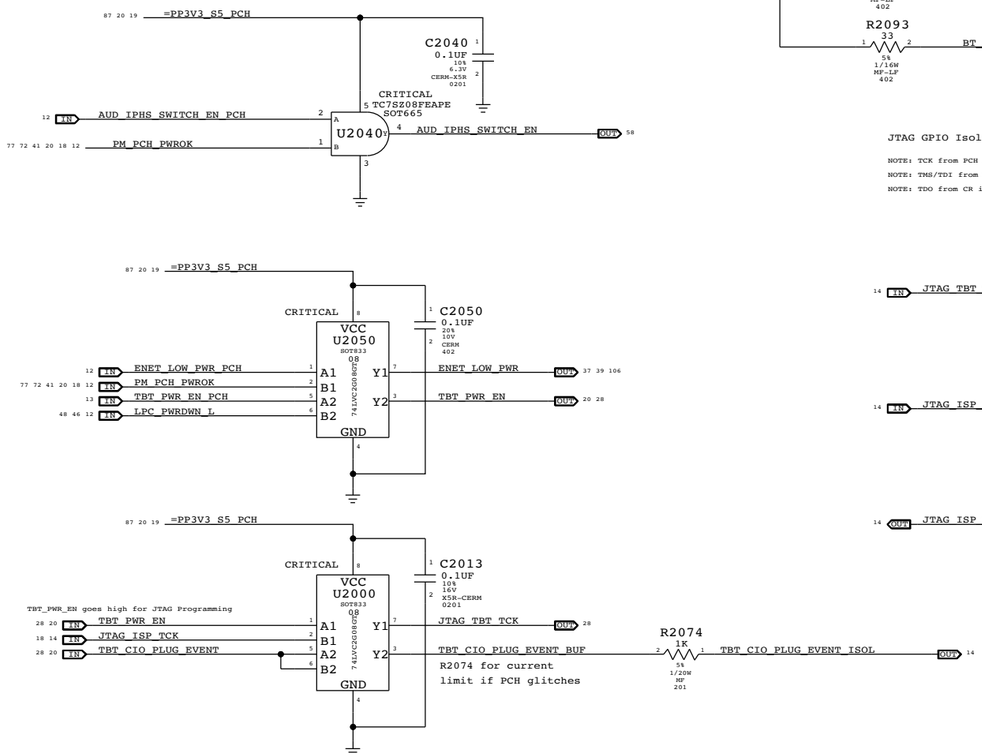
Platform Reset Connections

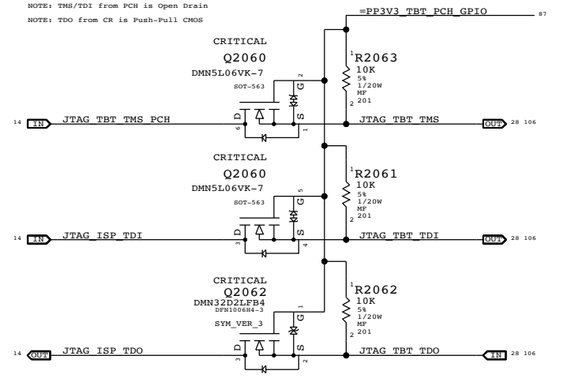


GPIO Glitch Prevention



JTAG GPIO Isolation due to glitch in and out of sleep

NOTE: TCK from PCH is Push-Pull CMOS
NOTE: TMS/TDI from PCH is Open Drain
NOTE: TDO from CR is Push-Pull CMOS



R2060 10K 5% 1/20W MF 201 TBT_CIO_PLUG_EVENT 20 28

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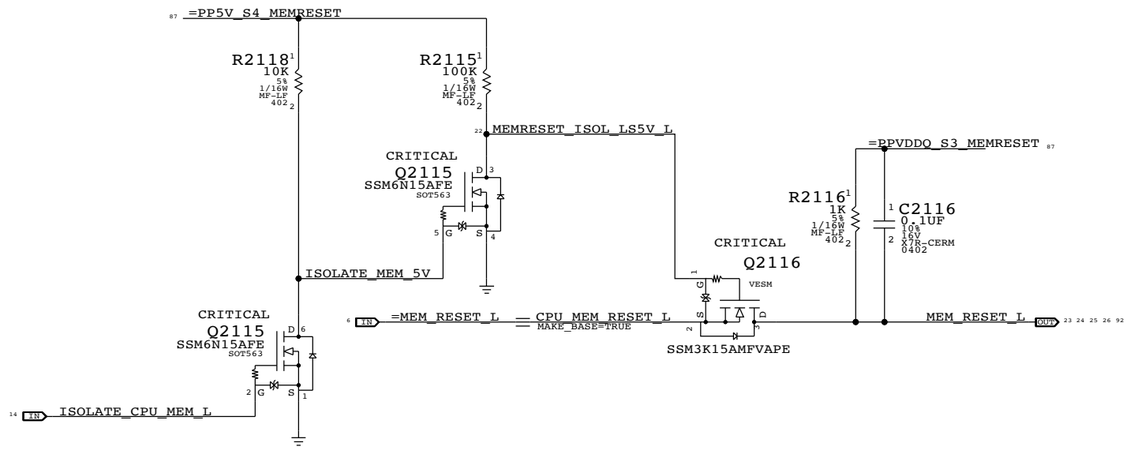
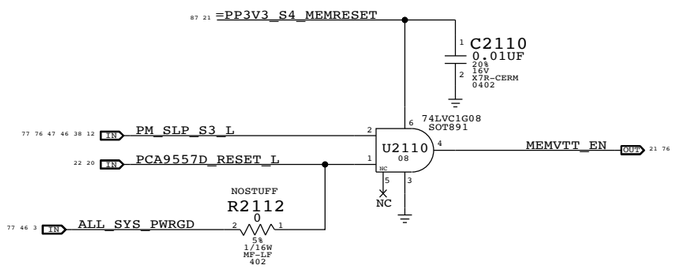
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

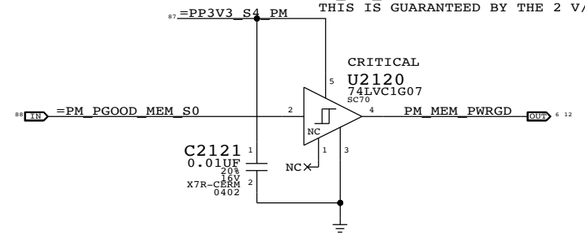
MEMVTT_EN = PLT_RESET_L * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L





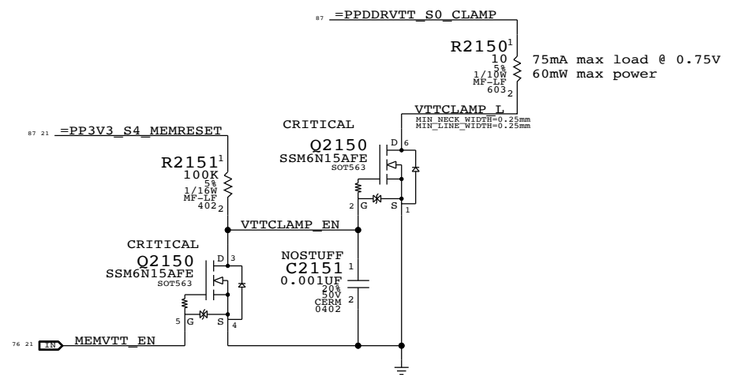
MEM S0 "PGOOD" FOR CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page
PM_MEM_PWRGD MUST ASSERT MIN 100 NS AFTER MEM_VDDQ RAMPS 80%
THIS IS GUARANTEED BY THE 2 V/MS RAMP RATE OF THE FET



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1
to	1	0	1	1	1	1	1
S3	2	0	0	1	1	1	0
	3	0	0	0	X	1	0
S3	4	0	0	1	X	1	0
to	5	0	1	1	0 (*)	1	1
S0	6	0	1	1	1	1	1
	7	1	1	1	1	CPU_MEM_RESET_L	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must de-assert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013
PAGE TITLE
CPU Memory S3 Support

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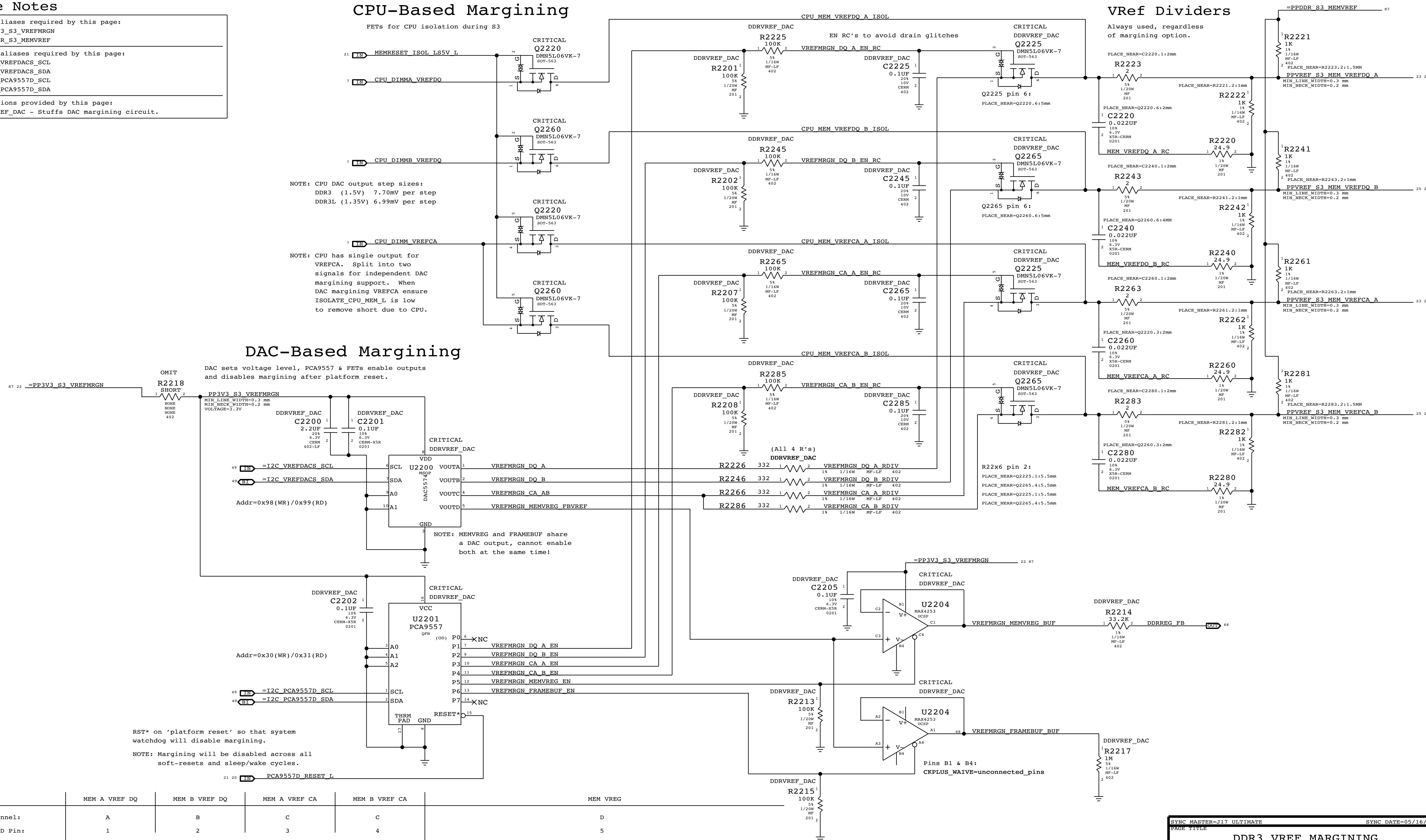
Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.



CPU-Based Margining
FETs for CPU isolation during S3
MEMRESET_ISOL_LS5V_L
CPU_DIMMA_VREFDQ
CPU_DIMMB_VREFDQ
CPU_DIMM_VREFCA
CRITICAL
Q2220
Q2260
DMN5L06VK-7
SOT-563
NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure ISOLATE_CPU_MEM_L is low to remove short due to CPU.
CPU_MEM_VREFDQ_A_ISOL
CPU_MEM_VREFDQ_B_ISOL
CPU_MEM_VREFCA_A_ISOL
CPU_MEM_VREFCA_B_ISOL
EN RC's to avoid drain glitches
DDRVREF_DAC
R2225
R2245
R2265
R2285
100K
R2201
R2202
R2207
R2208
C2225
C2245
C2265
C2285
0.1UF
VREFMRGN_DQ_A_EN_RC
VREFMRGN_DQ_B_EN_RC
VREFMRGN_CA_A_EN_RC
VREFMRGN_CA_B_EN_RC
Q2225
Q2265
Q2225 pin 6:
PLACE_NEAR=Q2220.6:5mm
Q2265 pin 6:
PLACE_NEAR=Q2260.6:5mm
VRef Dividers
Always used, regardless of margining option.
=PPDDR_S3_MEMVREF
R2221
R2222
R2241
R2242
R2261
R2262
R2281
R2282
1K
R2223
R2243
R2263
R2283
R2220
R2240
R2260
R2280
24.9
C2220
C2240
C2260
C2280
0.022UF
MEM_VREFDQ_A_RC
MEM_VREFDQ_B_RC
MEM_VREFCA_A_RC
MEM_VREFCA_B_RC
PPVREF_S3_MEM_VREFDQ_A
PPVREF_S3_MEM_VREFDQ_B
PPVREF_S3_MEM_VREFCA_A
PPVREF_S3_MEM_VREFCA_B
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
DAC-Based Margining
DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.
=PP3V3_S3_VREFMRGN
OMIT
R2218
SHORT
PP3V3_S3_VREFMRGN
C2200
2.2UF
C2201
0.1UF
U2200
DAC5574
VDD
SCL
SDA
A0
A1
GND
VOUTA
VOUTB
VOUTC
VOUTD
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA
Addr=0x98(WR)/0x99(RD)
VREFMRGN_DQ_A
VREFMRGN_DQ_B
VREFMRGN_CA_AB
VREFMRGN_MEMVREG_FBVREF
(All 4 R's)
R2226
R2246
R2266
R2286
332
VREFMRGN_DQ_A_RDIV
VREFMRGN_DQ_B_RDIV
VREFMRGN_CA_A_RDIV
VREFMRGN_CA_B_RDIV
R22x6 pin 2:
PLACE_NEAR=Q2225.1:5.5mm
PLACE_NEAR=Q2265.4:5.5mm
NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!
C2202
U2201
PCA9557
VCC
P0
P1
P2
P3
P4
P5
P6
P7
NC
RESET*
THRM PAD
Addr=0x30(WR)/0x31(RD)
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA
VREFMRGN_DQ_A_EN
VREFMRGN_DQ_B_EN
VREFMRGN_CA_A_EN
VREFMRGN_CA_B_EN
VREFMRGN_MEMVREG_EN
VREFMRGN_FRAMEBUF_EN
PCA9557D_RESET_L
RST* on 'platform reset' so that system watchdog will disable margining.
NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.
C2205
U2204
MAX4253
R2214
33.2K
VREFMRGN_MEMVREG_BUF
DDRREG_FB
R2213
R2215
R2217
1M
VREFMRGN_FRAMEBUF_BUF
Pins B1 & B4:
CKPLUS_WAIVE=unconnected_pins

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5

	DDR3 (1.5V)	DDR3L (1.35V)	DDR3 (1.5V)	DDR3L (1.35V)
Nominal value	0.750V (DAC: 0x3A = 0.747mV)	0.675V (DAC: 0x34 = 0.670mV)	1.500V (DAC: 0x74 = 1.495V)	1.343V (DAC: 0x68 = 1.341V)
Margined target:	0.300V - 1.200V (+/- 450mV)	0.275V - 1.075V (+/- 400mV)	1.200V - 1.800V (+/- 300mV)	0.950V - 1.750V (+/- 400mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)	0.000V - 1.354V (0x00 - 0x69)	0.000V - 3.004V (0x00 - 0xE9)	0.000V - 2.707V (0x00 - 0xD2)
Margined range:	0.299V - 1.206V (+/- 453mV)	0.269V - 1.083V (+/- 406mV)	1.199V - 1.801V (+/- 301mV)	0.932V - 1.760V (+/- 414mV)
VRef current:	+901uA - -911uA (- = sourced)	+811uA - -816uA (- = sourced)	+36uA - -36uA (- = sourced)	+28uA - -29uA (- = sourced)
DAC step size:	7.68mV / step @ output	7.67mV / step @ output	2.575mV / step @ output	3.923mV / step @ output

NOTE: DDR3 assumes TPS51916 supply with 10.0k/49.9k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE: DDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER: 051-9884 SIZE: D

REVISION: A.0.0

BRANCH

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

24 22 PPVREF_S3_MEM_VREFDQ_A
VOLTAGE=0.75V

C2330 2.2UF 20% 6.3V CERM 402-LF
C2331 0.1UF 20% 10V CERM 402

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

87 24 23 =PPVDDQ_S3_MEM_A

C2310 0.1UF 20% 10V CERM 402
C2311 0.1UF 20% 10V CERM 402
C2312 0.1UF 20% 10V CERM 402
C2313 0.1UF 20% 10V CERM 402
C2314 0.1UF 20% 10V CERM 402
C2315 0.1UF 20% 10V CERM 402
C2316 0.1UF 20% 10V CERM 402
C2317 0.1UF 20% 10V CERM 402

C2300 10UF 20% 6.3V X5R 603
C2301 10UF 20% 6.3V X5R 603
C2318 0.1UF 20% 10V CERM 402
C2319 0.1UF 20% 10V CERM 402
C2320 0.1UF 20% 10V CERM 402
C2321 0.1UF 20% 10V CERM 402
C2322 0.1UF 20% 10V CERM 402
C2323 0.1UF 20% 10V CERM 402

23 MEM_DIMM0_SA<1>
23 MEM_DIMM0_SA<0>
87 24 23 =PP3V3_S0_MEM_A_SPD

C2340 2.2UF 20% 6.3V CERM 402-LF
R2340 10K 5% 1/16W MF-LF 402
R2341 10K 5% 1/16W MF-LF 402

87 24 23 =PPDDRVTT_S0_MEM_A

J2300 SODIMM-P0.60-D8 F-ANG-SM-1 SYM 1 OF 2

1	VREFDQ		
3	VSS_1	CRITICAL	
5	DQ0		=MEM_A_DQ<0>
7	DQ1		=MEM_A_DQ<1>
9	VSS_3		
11	DM0		
13	VSS_4		
15	DQ2		=MEM_A_DQ<2>
17	DQ3		=MEM_A_DQ<3>
19	VSS_6		
21	DQ8		=MEM_A_DQ<8>
23	DQ9		=MEM_A_DQ<9>
25	VSS_8		
27	DQS1*		=MEM_A_DQS_N<1>
29	DQS1		=MEM_A_DQS_P<1>
31	VSS_10		
33	DQ10		=MEM_A_DQ<10>
35	DQ11		=MEM_A_DQ<11>
37	VSS_12		
39	DQ16		=MEM_A_DQ<16>
41	DQ17		=MEM_A_DQ<17>
43	VSS_14		
45	DQS2*		=MEM_A_DQS_N<2>
47	DQS2		=MEM_A_DQS_P<2>
49	VSS_17		
51	DQ18		=MEM_A_DQ<18>
53	DQ19		=MEM_A_DQ<19>
55	VSS_19		
57	DQ24		=MEM_A_DQ<24>
59	DQ25		=MEM_A_DQ<25>
61	VSS_21		
63	DM3		
65	VSS_22		
67	DQ26		=MEM_A_DQ<26>
69	DQ27		=MEM_A_DQ<27>
71	VSS_24		
		KEY	
73	CKE0		MEM_A_CKE<0>
75	VDD_0		
77	NC_0	NCX	
79	BA2		MEM_A_BA<2>
81	VDD_2		
83	A12/BC*		MEM_A_A<12>
85	A9		MEM_A_A<9>
87	VDD_4		
89	A8		MEM_A_A<8>
91	A5		MEM_A_A<5>
93	VDD_6		
95	A3		MEM_A_A<3>
97	A1		MEM_A_A<1>
99	VDD_8		
101	CK0		MEM_A_CLK_P<0>
103	CK0*		MEM_A_CLK_N<0>
105	VDD_10		
107	A10_AP		MEM_A_A<10>
109	BA0		MEM_A_BA<0>
111	VDD_12		
113	WE*		MEM_A_WE_L
115	CAS*		MEM_A_CAS_L
117	VDD_14		
119	A13		MEM_A_A<13>
121	S1*		MEM_A_CS_L<1>
123	VDD_16		
125	TEST	NCX	
127	VSS_26		
129	DQ32		=MEM_A_DQ<32>
131	DQ33		=MEM_A_DQ<33>
133	VSS_28		
135	DQS4*		=MEM_A_DQS_N<4>
137	DQS4		=MEM_A_DQS_P<4>
139	VSS_31		
141	DQ34		=MEM_A_DQ<34>
143	DQ35		=MEM_A_DQ<35>
145	VSS_33		
147	DQ40		=MEM_A_DQ<40>
149	DQ41		=MEM_A_DQ<41>
151	VSS_35		
153	DM5		
155	VSS_36		
157	DQ42		=MEM_A_DQ<42>
159	DQ43		=MEM_A_DQ<43>
161	VSS_38		
163	DQ48		=MEM_A_DQ<48>
165	DQ49		=MEM_A_DQ<49>
167	VSS_40		
169	DQS6*		=MEM_A_DQS_N<6>
171	DQS6		=MEM_A_DQS_P<6>
173	VSS_43		
175	DQ50		=MEM_A_DQ<50>
177	DQ51		=MEM_A_DQ<51>
179	VSS_45		
181	DQ56		=MEM_A_DQ<56>
183	DQ57		=MEM_A_DQ<57>
185	VSS_47		
187	DM7		
189	VSS_48		
191	DQ58		=MEM_A_DQ<58>
193	DQ59		=MEM_A_DQ<59>
195	VSS_50		
197	SA0		MEM_DIMM0_SA<0>
199	VDDSPD		=PP3V3_S0_MEM_A_SPD
201	SA1		MEM_DIMM0_SA<1>
203	VTT_0		

J2300 SODIMM-P0.60-D8 F-ANG-SM-1 SYM 2 OF 2

2	VSS_0		
4	DQ4		=MEM_A_DQ<4>
6	DQ5		=MEM_A_DQ<5>
8	VSS_2		
10	DQS0*		=MEM_A_DQS_N<0>
12	DQS0		=MEM_A_DQS_P<0>
14	VSS_5		
16	DQ6		=MEM_A_DQ<6>
18	DQ7		=MEM_A_DQ<7>
20	VSS_7		
22	DQ12		=MEM_A_DQ<12>
24	DQ13		=MEM_A_DQ<13>
26	VSS_9		
28	DM1		
30	RESET*		MEM_RESET_L
32	VSS_11		
34	DQ14		=MEM_A_DQ<14>
36	DQ15		=MEM_A_DQ<15>
38	VSS_13		
40	DQ20		=MEM_A_DQ<20>
42	DQ21		=MEM_A_DQ<21>
44	VSS_15		
46	DM2		
48	VSS_16		
50	DQ22		=MEM_A_DQ<22>
52	DQ23		=MEM_A_DQ<23>
54	VSS_18		
56	DQ28		=MEM_A_DQ<28>
58	DQ29		=MEM_A_DQ<29>
60	VSS_20		
62	DQS3*		=MEM_A_DQS_N<3>
64	DQS3		=MEM_A_DQS_P<3>
66	VSS_23		
68	DQ30		=MEM_A_DQ<30>
70	DQ31		=MEM_A_DQ<31>
72	VSS_25		
74	CKE1		MEM_A_CKE<1>
76	VDD_1		
78	A15		MEM_A_A<15>
80	A14		MEM_A_A<14>
82	VDD_3		
84	A11		MEM_A_A<11>
86	A7		MEM_A_A<7>
88	VDD_5		
90	A6		MEM_A_A<6>
92	A4		MEM_A_A<4>
94	VDD_7		
96	A2		MEM_A_A<2>
98	A0		MEM_A_A<0>
100	VDD_9		
102	CK1		MEM_A_CLK_P<1>
104	CK1*		MEM_A_CLK_N<1>
106	VDD_11		
108	BA1		MEM_A_BA<1>
110	RAS*		MEM_A_RAS_L
112	VDD_13		
114	S0*		MEM_A_CS_L<0>
116	ODT0		MEM_A_ODT<0>
118	VDD_15		
120	ODT1		MEM_A_ODT<1>
122	NC_1	NCX	
124	VDD_17		
126	VREFCA		
128	VSS_27		
130	DQ36		=MEM_A_DQ<36>
132	DQ37		=MEM_A_DQ<37>
134	VSS_29		
136	DM4		
138	VSS_30		
140	DQ38		=MEM_A_DQ<38>
142	DQ39		=MEM_A_DQ<39>
144	VSS_32		
146	DQ44		=MEM_A_DQ<44>
148	DQ45		=MEM_A_DQ<45>
150	VSS_34		
152	DQS5*		=MEM_A_DQS_N<5>
154	DQS5		=MEM_A_DQS_P<5>
156	VSS_37		
158	DQ46		=MEM_A_DQ<46>
160	DQ47		=MEM_A_DQ<47>
162	VSS_39		
164	DQ52		=MEM_A_DQ<52>
166	DQ53		=MEM_A_DQ<53>
168	VSS_41		
170	DM6		
172	VSS_42		
174	DQ54		=MEM_A_DQ<54>
176	DQ55		=MEM_A_DQ<55>
178	VSS_44		
180	DQ60		=MEM_A_DQ<60>
182	DQ61		=MEM_A_DQ<61>
184	VSS_46		
186	DQS7*		=MEM_A_DQS_N<7>
188	DQS7		=MEM_A_DQS_P<7>
190	VSS_49		
192	DQ62		=MEM_A_DQ<62>
194	DQ63		=MEM_A_DQ<63>
196	VSS_51		
198	EVENT*		MEM_EVENT_L
200	SDA		=I2C_SODIMMA_SDA
202	SCL		=I2C_SODIMMA_SCL
204	VTT_1		

P/N: 516S1019

J2300 SODIMM-P0.60-D8 F-ANG-SM-1 SYM 2 OF 2

205 206 207 208 209 MTG HOLE

=PPVDDQ_S3_MEM_A 23 24 87

PPVREF_S3_MEM_VREFCA_A 22 24
VOLTAGE=0.75V

C2335 2.2UF 20% 6.3V CERM 402-LF
C2336 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_A 23 24 87

C2350 1UF 10% 10V X5R 402
C2351 1UF 10% 10V X5R 402
C2352 1UF 10% 10V X5R 402
C2353 1UF 10% 10V X5R 402

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
DDR3 SO-DIMM Connector A Slot0

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
BRANCH
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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1019

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

J2400
SODIMM-P0.60-D8
F-ANG-SM-1
SYM 1 OF 2
CRITICAL

J2400
SODIMM-P0.60-D8
F-ANG-SM-1
SYM 2 OF 2
MTG HOLE

1	VREFDQ		2	VSS_0			
3	VSS_1		4	DQ4	=MEM_A_DQ<4>	BI	23 27
5	DQ0	=MEM_A_DQ<0>	6	DQ5	=MEM_A_DQ<5>	BI	23 27
7	DQ1	=MEM_A_DQ<1>	8	VSS_2			
9	VSS_3		10	DQS0*	=MEM_A_DQS_N<0>	BI	23 27
11	DM0		12	DQS0	=MEM_A_DQS_P<0>	BI	23 27
13	VSS_4		14	VSS_5			
15	DQ2	=MEM_A_DQ<2>	16	DQ6	=MEM_A_DQ<6>	BI	23 27
17	DQ3	=MEM_A_DQ<3>	18	DQ7	=MEM_A_DQ<7>	BI	23 27
19	VSS_6		20	VSS_7			
21	DQ8	=MEM_A_DQ<8>	22	DQ12	=MEM_A_DQ<12>	BI	23 27
23	DQ9	=MEM_A_DQ<9>	24	DQ13	=MEM_A_DQ<13>	BI	23 27
25	VSS_8		26	VSS_9			
27	DQS1*	=MEM_A_DQS_N<1>	28	DM1			
29	DQS1	=MEM_A_DQS_P<1>	30	RESET*	MEM_RESET_L	IN	21 23 25 26 92
31	VSS_10		32	VSS_11			
33	DQ10	=MEM_A_DQ<10>	34	DQ14	=MEM_A_DQ<14>	BI	23 27
35	DQ11	=MEM_A_DQ<11>	36	DQ15	=MEM_A_DQ<15>	BI	23 27
37	VSS_12		38	VSS_13			
39	DQ16	=MEM_A_DQ<16>	40	DQ20	=MEM_A_DQ<20>	BI	23 27
41	DQ17	=MEM_A_DQ<17>	42	DQ21	=MEM_A_DQ<21>	BI	23 27
43	VSS_14		44	VSS_15			
45	DQS2*	=MEM_A_DQS_N<2>	46	DM2			
47	DQS2	=MEM_A_DQS_P<2>	48	VSS_16			
49	VSS_17		50	DQ22	=MEM_A_DQ<22>	BI	23 27
51	DQ18	=MEM_A_DQ<18>	52	DQ23	=MEM_A_DQ<23>	BI	23 27
53	DQ19	=MEM_A_DQ<19>	54	VSS_18			
55	VSS_19		56	DQ28	=MEM_A_DQ<28>	BI	23 27
57	DQ24	=MEM_A_DQ<24>	58	DQ29	=MEM_A_DQ<29>	BI	23 27
59	DQ25	=MEM_A_DQ<25>	60	VSS_20			
61	VSS_21		62	DQS3*	=MEM_A_DQS_N<3>	BI	23 27
63	DM3		64	DQS3	=MEM_A_DQS_P<3>	BI	23 27
65	VSS_22		66	VSS_23			
67	DQ26	=MEM_A_DQ<26>	68	DQ30	=MEM_A_DQ<30>	BI	23 27
69	DQ27	=MEM_A_DQ<27>	70	DQ31	=MEM_A_DQ<31>	BI	23 27
71	VSS_24		72	VSS_25			
	KEY						
73	CKE0	MEM_A_CKE<2>	74	CKE1	MEM_A_CKE<3>	IN	7 92
75	VDD_0		76	VDD_1			
77	NC_0	NCX	78	A15	MEM_A_A<15>	IN	7 23 92
79	BA2	MEM_A_BA<2>	80	A14	MEM_A_A<14>	IN	7 23 92
81	VDD_2		82	VDD_3			
83	A12/BC*	MEM_A_A<12>	84	A11	MEM_A_A<11>	IN	7 23 92
85	A9	MEM_A_A<9>	86	A7	MEM_A_A<7>	IN	7 23 92
87	VDD_4		88	VDD_5			
89	A8	MEM_A_A<8>	90	A6	MEM_A_A<6>	IN	7 23 92
91	A5	MEM_A_A<5>	92	A4	MEM_A_A<4>	IN	7 23 92
93	VDD_6		94	VDD_7			
95	A3	MEM_A_A<3>	96	A2	MEM_A_A<2>	IN	7 23 92
97	A1	MEM_A_A<1>	98	A0	MEM_A_A<0>	IN	7 23 92
99	VDD_8		100	VDD_9			
101	CK0	MEM_A_CLK_P<2>	102	CK1	MEM_A_CLK_P<3>	IN	7 92
103	CK0*	MEM_A_CLK_N<2>	104	CK1*	MEM_A_CLK_N<3>	IN	7 92
105	VDD_10		106	VDD_11			
107	A10_AP	MEM_A_A<10>	108	BA1	MEM_A_BA<1>	IN	7 23 92
109	BA0	MEM_A_BA<0>	110	RAS*	MEM_A_RAS_L	IN	7 23 92
111	VDD_12		112	VDD_13			
113	WE*	MEM_A_WE_L	114	S0*	MEM_A_CS_L<2>	IN	7 92
115	CAS*	MEM_A_CAS_L	116	ODT0	MEM_A_ODT<2>	IN	7 92
117	VDD_14		118	VDD_15			
119	A13	MEM_A_A<13>	120	ODT1	MEM_A_ODT<3>	IN	7 92
121	S1*	MEM_A_CS_L<3>	122	NC_1	NCX		
123	VDD_16		124	VDD_17			
125	TEST	NCX	126	VREFCA	PPVREF_S3_MEM_VREFCA_A		22 23
127	VSS_26		128	VSS_27			
129	DQ32	=MEM_A_DQ<32>	130	DQ36	=MEM_A_DQ<36>	BI	23 27
131	DQ33	=MEM_A_DQ<33>	132	DQ37	=MEM_A_DQ<37>	BI	23 27
133	VSS_28		134	VSS_29			
135	DQS4*	=MEM_A_DQS_N<4>	136	DM4			
137	DQS4	=MEM_A_DQS_P<4>	138	VSS_30			
139	VSS_31		140	DQ38	=MEM_A_DQ<38>	BI	23 27
141	DQ34	=MEM_A_DQ<34>	142	DQ39	=MEM_A_DQ<39>	BI	23 27
143	DQ35	=MEM_A_DQ<35>	144	VSS_32			
145	VSS_33		146	DQ44	=MEM_A_DQ<44>	BI	23 27
147	DQ40	=MEM_A_DQ<40>	148	DQ45	=MEM_A_DQ<45>	BI	23 27
149	DQ41	=MEM_A_DQ<41>	150	VSS_34			
151	VSS_35		152	DQS5*	=MEM_A_DQS_N<5>	BI	23 27
153	DM5		154	DQS5	=MEM_A_DQS_P<5>	BI	23 27
155	VSS_36		156	VSS_37			
157	DQ42	=MEM_A_DQ<42>	158	DQ46	=MEM_A_DQ<46>	BI	23 27
159	DQ43	=MEM_A_DQ<43>	160	DQ47	=MEM_A_DQ<47>	BI	23 27
161	VSS_38		162	VSS_39			
163	DQ48	=MEM_A_DQ<48>	164	DQ52	=MEM_A_DQ<52>	BI	23 27
165	DQ49	=MEM_A_DQ<49>	166	DQ53	=MEM_A_DQ<53>	BI	23 27
167	VSS_40		168	VSS_41			
169	DQS6*	=MEM_A_DQS_N<6>	170	DM6			
171	DQS6	=MEM_A_DQS_P<6>	172	VSS_42			
173	VSS_43		174	DQ54	=MEM_A_DQ<54>	BI	23 27
175	DQ50	=MEM_A_DQ<50>	176	DQ55	=MEM_A_DQ<55>	BI	23 27
177	DQ51	=MEM_A_DQ<51>	178	VSS_44			
179	VSS_45		180	DQ60	=MEM_A_DQ<60>	BI	23 27
181	DQ56	=MEM_A_DQ<56>	182	DQ61	=MEM_A_DQ<61>	BI	23 27
183	DQ57	=MEM_A_DQ<57>	184	VSS_46			
185	VSS_47		186	DQS7*	=MEM_A_DQS_N<7>	BI	23 27
187	DM7		188	DQS7	=MEM_A_DQS_P<7>	BI	23 27
189	VSS_48		190	VSS_49			
191	DQ58	=MEM_A_DQ<58>	192	DQ62	=MEM_A_DQ<62>	BI	23 27
193	DQ59	=MEM_A_DQ<59>	194	DQ63	=MEM_A_DQ<63>	BI	23 27
195	VSS_50		196	VSS_51			
197	SA0	MEM_DIMM1_SA<0>	198	EVENT*	MEM_EVENT_L	OUTPD	23 25 26 46 47
199	VDDSPD	=PP3V3_S0_MEM_A_SPD	200	SDA	=I2C_SODIMMA_SDA	BI	23 49
201	SA1	MEM_DIMM1_SA<1>	202	SCL	=I2C_SODIMMA_SCL	IN	23 49
203	VTT_0		204	VTT_1			

=PPVDDQ_S3_MEM_A 87 24 23 — C2410 C2411 C2412 C2413 C2414 C2415 C2416 C2417 0.1UF 20% 10V CERM 402

=PPVDDQ_S3_MEM_A 87 24 23 — C2400 10UF 20% 6.3V X5R 603; C2401 10UF 20% 6.3V X5R 603; C2418 C2419 C2420 C2421 C2422 C2423 0.1UF 20% 10V CERM 402

PPVREF_S3_MEM_VREFDQ_A 23 22 (VOLTAGE=0.75V) — C2430 2.2UF 20% 6.3V CERM 402-LF; C2431 0.1UF 20% 10V CERM 402

PPVREF_S3_MEM_VREFCA_A 22 23 (VOLTAGE=0.75V) — C2435 2.2UF 20% 6.3V CERM 402-LF; C2436 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_A 23 24 87 — C2450 C2451 C2452 C2453 1UF 10% 10V X5R 402

=PP3V3_S0_MEM_A_SPD 87 24 23 — R2440 10K 5% 1/16W MF-LF 402 — MEM_DIMM1_SA<0> 24

MEM_DIMM1_SA<1> 24 — =PP3V3_S0_MEM_A_SPD 87 24 23 — C2440 2.2UF 20% 6.3V CERM 402-LF; R2441 10K 5% 1/16W MF-LF 402

=PPDDRVTT_S0_MEM_A 87 24 23

SYNC_MASTER=J17_ULTIMATE	SYNC_DATE=05/16/2011
PAGE TITLE	DDR3 SO-DIMM Connector A Slot1
Apple Inc.	DRAWING NUMBER 051-9884 SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 24 OF 127
	SHEET 24 OF 106

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IV ALL RIGHTS RESERVED

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1019

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

J2500 SODIMM-P0.60-D8 F-ANG-SM-1 SYM 1 OF 2 (CRITICAL)

J2500 SODIMM-P0.60-D8 F-ANG-SM-1 SYM 2 OF 2 (MTG HOLE SYM)

SYNC MASTER=J17 ULTIMATE	SYNC DATE=05/16/2013
PAGE TITLE: DDR3 SO-DIMM CONNECTOR B SLOT0	
Apple Inc.	DRAWING NUMBER: 051-9884 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 25 OF 127
	SHEET: 25 OF 106

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1019

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

J2600
SODIMM-P0.60-D8
F-ANG-SM-1
SYM 1 OF 2

J2600
SODIMM-P0.60-D8
F-ANG-SM-1
SYM 2 OF 2

SYNC MASTER=J17 ULTIMATE		SYNC DATE=05/16/2013	
PAGE TITLE: DDR3 SO-DIMM CONNECTOR B SLOT1			
Apple Inc.	DRAWING NUMBER: 051-9884	SIZE: D	
	REVISION: A.0.0		
	BRANCH:		
	PAGE: 26 OF 127		
	SHEET: 26 OF 106		

THERE ARE NO PIN SWAPS

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SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE

DDR3 ALIASES AND BITSWAPS

Apple Inc.

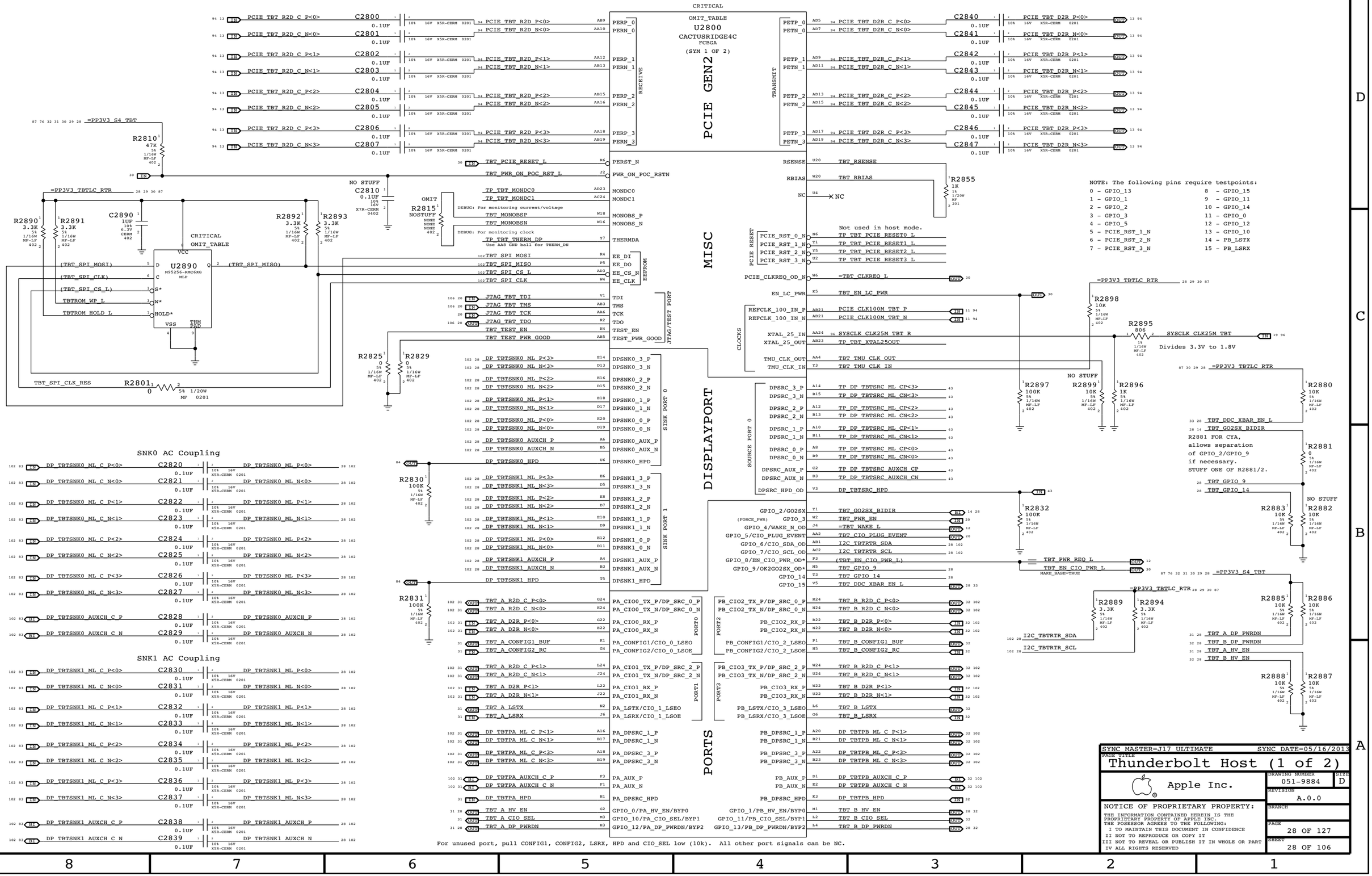
DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

BRANCH

PAGE 27 OF 127

SHEET 27 OF 106



SYNC_MASTER=J17 ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE

Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

BRANCH

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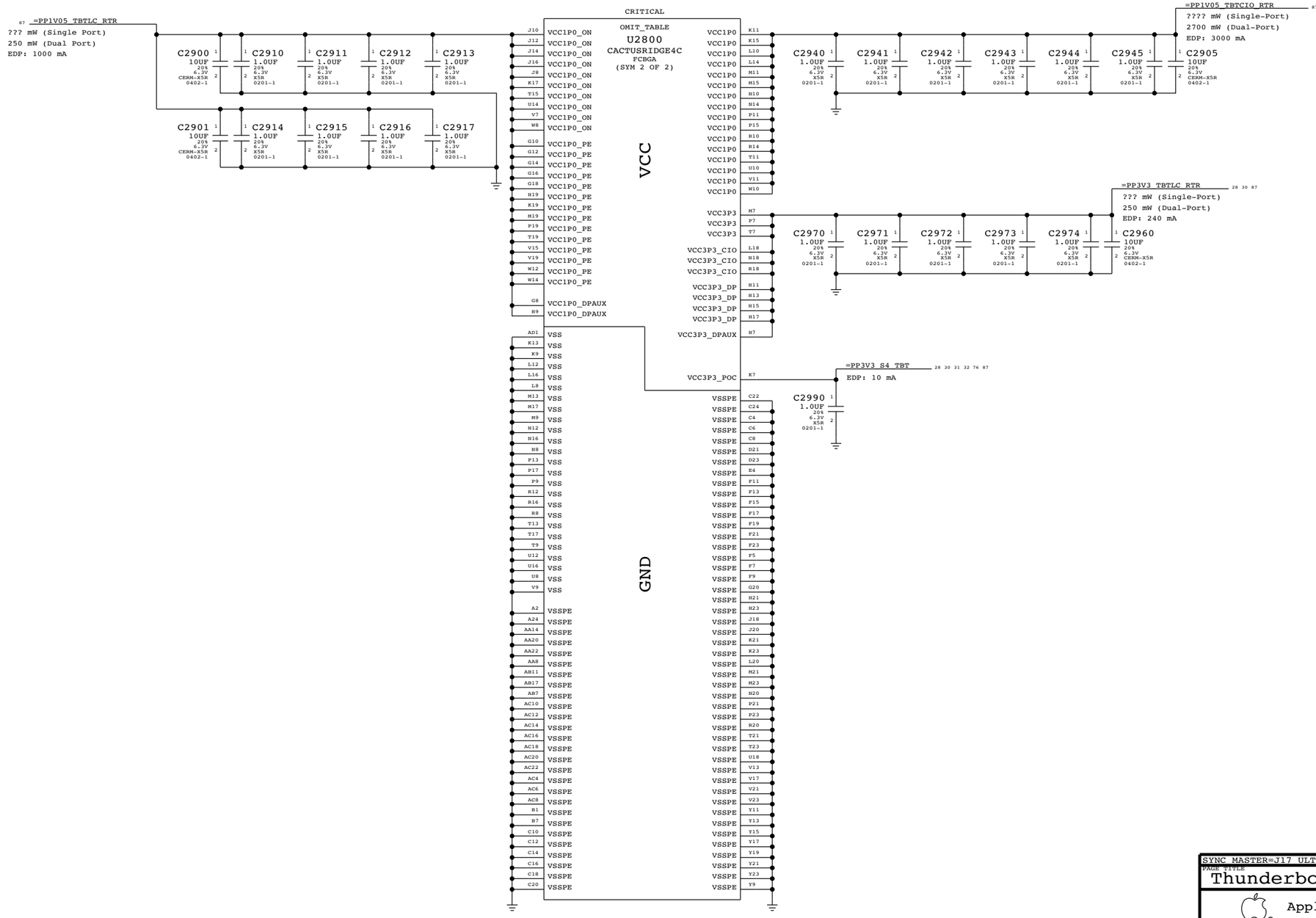
SHEET 28 OF 106



EDP current / power consumption figures from CR DG v0.57, IBL doc #472455.

PAGE TITLE
Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

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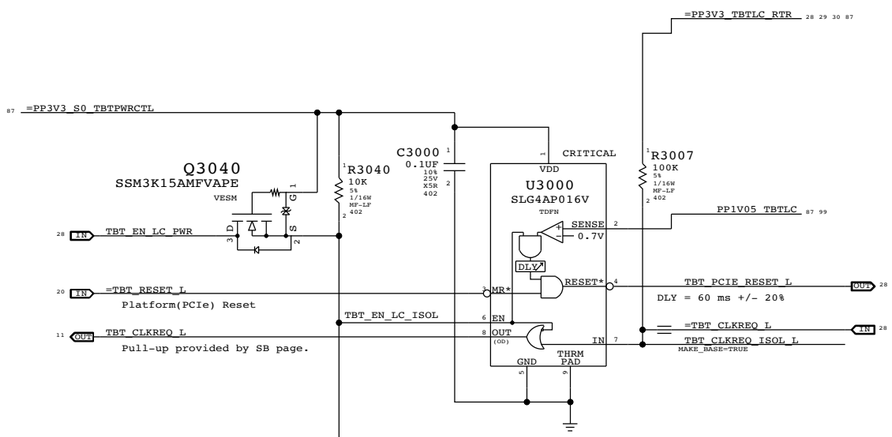
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

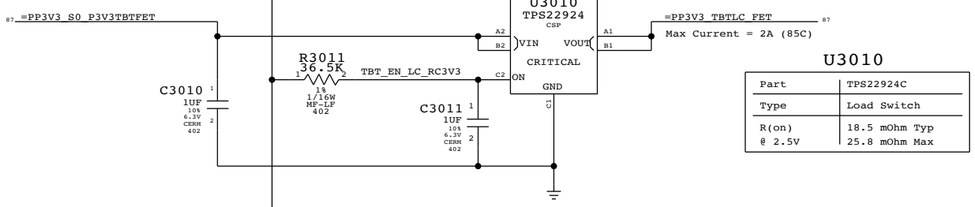
Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

Supervisor & CLKREQ# Isolation



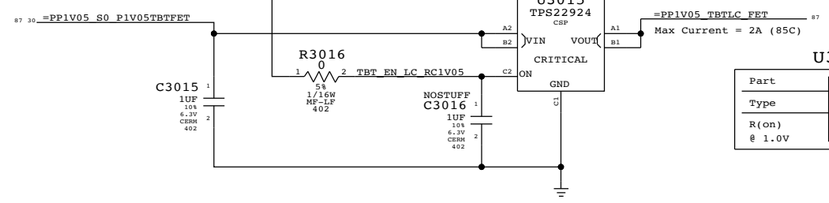
3.3V TBT "LC" Switch



U3010

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

1.05V TBT "LC" Switch

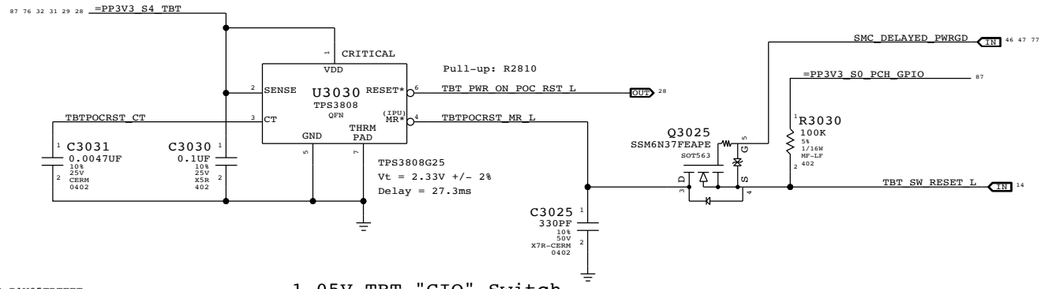


U3015

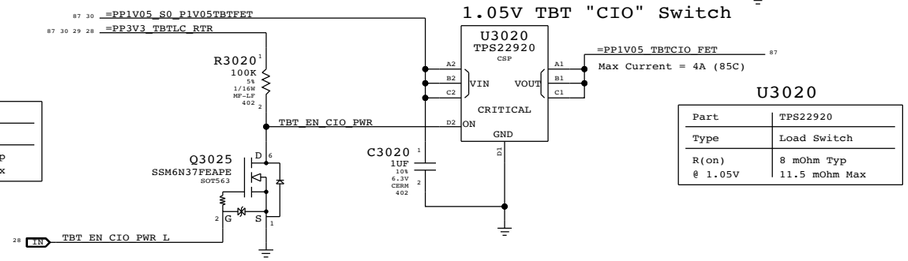
Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.



1.05V TBT "CIO" Switch



U3020

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
Thunderbolt Power Support

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTAPWRSW
CRITICAL C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C3280 22UF 20% 6.3V X5R-CERM-1 603
C3281 0.1UF 20% 10V CERM 402
=PPHV_SW_TBTAPWRSW
18.9V Max
C3215 4.7UF 10% 25V X5R-CERM 0603
C3210 0.1UF 10% 50V X7R 603-1
CRITICAL U3210 CD3210A0RGP QFN
V3P3OUT NC
OUT PPHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
C3211 0.1UF 10% 50V X7R 603-1
V3P3 VHV RSVD RSVD
=TBTAPWRSW_EN EN ISET_V3P3 TBTAPWRSW_ISET_V3P3
TBT_A_HV_EN HV_EN ISET_S0 TBTAPWRSW_ISET_S0
=TBT_S0_EN S0 ISET_S3 TBTAPWRSW_ISET_S3
GND THRM PAD
12V: See below
TBTHV:P15V
R3210 22.6K 1% 1/16W MF-LF 402
R3211 22.6K 1% 1/16W MF-LF 402
R3212 36.5K 1% 1/16W MF-LF 402
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R3213 22.6K 1% 1/16W MF-LF 402
R3214 22.6K 1% 1/16W MF-LF 402
Two Rs in series required by CD3210 for single-fault protection(S0,S3 only)

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R3210,R3213		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0596	311S0593		ALL	TI Alternate
128S0398	128S0220		ALL	3.3V INPUT CAP

Thunderbolt Connector A

=PP3V3_S4_TBT
C3220 0.1UF 10% 6.3V CERM-X5R 0201
C3221 0.1UF 10% 6.3V CERM-X5R 0201
R3227 10K 5% 1/20W MF 201
R3229 100K 5% 1/20W MF 201
VDD
CRITICAL U3220 CBTL05023 HVQFN
TBT_A_BIAS VOLTAGE=3.3V
C3225 0.1UF 10% 6.3V CERM-X5R 0201
TBT_A_CIO_SEL
DP_AUXIO_EN
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
C3230 0.1UF 10% 6.3V CERM-X5R 0201
C3231 0.1UF 10% 6.3V CERM-X5R 0201
DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
C3232 0.22UF 20% 6.3V X5R 0201
C3233 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_P<1>
DP_TBTPA_ML_N<1>
TBT_A_LSTX
TBT_A_LSRX_UNBUF
TBT_A_DP_PWRDN
DP_TBTPA_HPD
BIASIN BIASOUT AUXIO_EN AUX- AUX+ DDC_DAT DDC_CLK CA_DETOUT DP+ DP- LSTX LSRX DP_PD HPDOUT
AUXIO- AUXIO+ CA_DET DPMLO+ DPMLO- HPD
DP_A_AUXCH_DDC_N
DP_A_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_HPD
GND_THMPAD
R3226 1M 5% 1/20W MF 201
R3228 100K 5% 1/20W MF 201
=PP3V3_S4_TBT
CRITICAL U3260 74AUP1T97GM SOT886
TBT_A_LSRX
C3260 0.1UF 10% 16V X5R-CERM 0201

L3200 FERR-120-OHM-3A 0603
PP3V3R3V_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
C3200 0.01UF 10% 50V X7R-CERM 0402
C3201 0.01UF 10% 50V X7R-CERM 0402
TBTACONN_20_RC
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
R3201 J2 5% 1/20W MF 201
TBT Dir DP Dir

C3205 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_1_C
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
(0-18.9V)
DP Dir TBT Dir
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT: TX_0
C3270 0.22UF 20% 6.3V X5R 0201
C3271 0.22UF 20% 6.3V X5R 0201
GND_VOID=TRUE (Both C's)
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201
GND_VOID=TRUE

CRITICAL J3200 DUAL-MDP-D8 F-ANG-TH
SHLD
HPD CONFIG1 CONFIG2 GND2 ML_LANE3P ML_LANE3N GND4 AUX_CHP AUX_CHN DP_PWR
ML_LANE0P ML_LANE0N GND1 ML_LANE1P ML_LANE1N GND3 ML_LANE2P ML_LANE2N RETURN
PORT A
SHLD

C3206 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_7_C
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
(0-18.9V)
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
TBT: TX_1
C3272 0.22UF 20% 6.3V X5R 0201
C3273 0.22UF 20% 6.3V X5R 0201
GND_VOID=TRUE (Both C's)
TBT_A_R2D_C_N<1>
TBT_A_R2D_C_P<1>
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201
GND_VOID=TRUE
470k R's for ESD protection on AC-coupled signals.

J16:514-0824 / J17:514-0831

GND_VOID=TRUE (Both C's)
C3274 0.47UF 20% 4V CERM-X5R-1 201
C3275 0.47UF 20% 4V CERM-X5R-1 201
TBT_A_D2R_N<0>
TBT_A_D2R_P<0>
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
NOTE: Polarity Swapped for layout!
R3294 1K 5% 1/20W MF 201
R3295 1K 5% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
C3278 0.22UF 20% 6.3V X5R 0201
C3279 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
DP_TBTPA_ML_P<3>
DP_TBTPA_ML_N<3>
TBT: Terminated
R3278 470K 5% 1/20W MF 201
R3279 470K 5% 1/20W MF 201
TBT_A_BIAS
R3298 2.2K 5% 1/20W MF 201
R3299 2.2K 5% 1/20W MF 201
GND_VOID=TRUE (Both C's)
C3276 0.47UF 20% 4V CERM-X5R-1 201
C3277 0.47UF 20% 4V CERM-X5R-1 201
TBT_A_D2R_N<1>
TBT_A_D2R_P<1>
TBT_A_D2R_C_P<1>
TBT_A_D2R_C_N<1>
NOTE: Polarity Swapped for layout!
CRITICAL
GND_VOID=TRUE (Both D's)
D3298 BAR90-02LRH TSLP-2-7
D3299 BAR90-02LRH TSLP-2-7
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
CRITICAL L3298 650NH-5%-0.430MA-0.52OHM 0603
CRITICAL L3299 650NH-5%-0.430MA-0.52OHM 0603
NO_XNET_CONNECTION=TRUE
DP_A_AUXCH_DDC_P
DP_A_AUXCH_DDC_N
C3298 30PF 5% 50V C0G-NP0 0402
C3299 30PF 5% 50V C0G-NP0 0402
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R-CERM 0201
C3295 330PF 10% 16V X7R-CERM 0201
R3241 100K 5% 1/20W MF 201
C3202 0.01UF 10% 25V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTBPWRSW
CRITICAL C3387 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C3380 22UF 20% 6.3V X5R-CERM-1 603
C3381 0.1UF 20% 10V CERM 402
=PPHV_SW_TBTBPWRSW
18.9V Max
C3315 4.7UF 10% 25V X5R-CERM 0603
C3310 0.1UF 10% 50V X7R 603-1
CRITICAL U3310 CD3210A0RGP QFN
V3P3
VHV
RSVD
EN
HV_EN
S0
V3P3OUT
OUT
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
NC
PPHV_SW_TBTBPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C3311 0.1UF 10% 50V X7R 603-1
=TBTBPWRSW_EN
TBT_B_HV_EN
=TBT_S0_EN
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
TBTHV:P15V
12V: See below
R3310 22.6K 1% 1/16W MF-LF 402
R3311 22.6K 1% 1/16W MF-LF 402
R3312 36.5K 1% 1/16W MF-LF 402
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
R3313 22.6K 1% 1/16W MF-LF 402
R3314 22.6K 1% 1/16W MF-LF 402
Two Rs in series required by CD3210 for single-fault protection(S0,S3 only)

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R3310,R3313		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Thunderbolt Connector B

=PP3V3_S4_TBT
C3320 0.1UF 10% 6.3V CERM-X5R 0201
C3321 0.1UF 10% 6.3V CERM-X5R 0201
R3327 10K 5% 1/20W MF 201
R3329 100K 5% 1/20W MF 201
VDD
CRITICAL U3320 CBTL05023 HVQFN
TBT_B_BIAS VOLTAGE=3.3V
C3325 0.1UF 10% 6.3V CERM-X5R 0201
TBT_B_CIO_SEL
DP_AUXIO_EN
DP_TBTPB_AUXCH_C_N
DP_TBTPB_AUXCH_C_P
C3330 0.1UF 10% 6.3V CERM-X5R 0201
C3331 0.1UF 10% 6.3V CERM-X5R 0201
DP_TBTPB_AUXCH_N
DP_TBTPB_AUXCH_P
DP_TBTPB_DDC_DATA
DP_TBTPB_DDC_CLK
TBT_B_CONFIG1_BUF
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
C3332 0.22UF 20% 6.3V X5R 0201
C3333 0.22UF 20% 6.3V X5R 0201
DP_TBTPB_ML_P<1>
DP_TBTPB_ML_N<1>
TBT_B_LSTX
TBT_B_LSRX_UNBUF
TBT_B_DP_PWRDN
DP_TBTPB_HPD
TBT_B_LSRX
CRITICAL U3360 74AUP1T97GM SOT886
C3360 0.1UF 10% 16V X5R-CERM 0201
R3326 1M 5% 1/20W MF 201
R3328 100K 5% 1/20W MF 201
BIASIN
AUXIO_EN
AUX-
AUX+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
LSTX
LSRX
DP_PD
HPDOUT
BIASOUT
AUXIO-
AUXIO+
CA_DET
DPMLO+
DPMLO-
HPD
GND_THMPAD
DP_B_AUXCH_DDC_N
DP_B_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_B_CONFIG1_RC
DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>
TBT: LSX_B_R2P/P2R (P/N)
TBT_B_HPD

L3300 FERR-120-OHM-3A 0603
PP3V3R3HV_SW_TBTBPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C3300 0.01UF 10% 50V X7R-CERM 0402
C3301 0.01UF 10% 50V X7R-CERM 0402
TBTBCONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
R3301 12 5% 1/20W MF 201
TBT Dir
DP Dir
J3200 DUAL-MDP-D8 F-ANG-TH
SHLD
HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN
PORT B SHLD
J16:514-0824 / J17:514-0831
C3305 0.01UF 10% 25V X5R-CERM 0201
TBTBCONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
TBT_B_R2D_P<0>
TBT_B_R2D_N<0>
TBT: TX_0
C3306 0.01UF 10% 25V X5R-CERM 0201
TBTBCONN_7_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
TBT: LSX_R2P/P2R (P/N)
TBT_B_R2D_P<1>
TBT_B_R2D_N<1>
TBT: TX_1
GND_VOID=TRUE (Both C's)
C3370 0.22UF 20% 6.3V X5R 0201
C3371 0.22UF 20% 6.3V X5R 0201
R3370 470K 5% 1/20W MF 201
R3371 470K 5% 1/20W MF 201
C3372 0.22UF 20% 6.3V X5R 0201
C3373 0.22UF 20% 6.3V X5R 0201
R3372 470K 5% 1/20W MF 201
R3373 470K 5% 1/20W MF 201
470k R's for ESD protection on AC-coupled signals.

GND_VOID=TRUE (Both C's)
C3374 0.47UF 20% 4V CERM-X5R-1 201
C3375 0.47UF 20% 4V CERM-X5R-1 201
TBT_B_D2R_N<0>
TBT_B_D2R_P<0>
TBT_B_D2R_C_P<0>
TBT_B_D2R_C_N<0>
NOTE: Polarity Swapped for Layout!
R3394 1K 5% 1/20W MF 201
R3395 1K 5% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
C3378 0.22UF 20% 6.3V X5R 0201
C3379 0.22UF 20% 6.3V X5R 0201
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_C_N<3>
DP_TBTPB_ML_P<3>
DP_TBTPB_ML_N<3>
TBT: Terminated
R3378 470K 5% 1/20W MF 201
R3379 470K 5% 1/20W MF 201
TBT_B_BIAS
R3398 2.2K 5% 1/20W MF 201
R3399 2.2K 5% 1/20W MF 201
GND_VOID=TRUE (Both C's)
C3376 0.47UF 20% 4V CERM-X5R-1 201
C3377 0.47UF 20% 4V CERM-X5R-1 201
TBT_B_D2R_N<1>
TBT_B_D2R_P<1>
TBT_B_D2R_C_P<1>
TBT_B_D2R_C_N<1>
NOTE: Polarity Swapped for Layout!
CRITICAL
GND_VOID=TRUE (Both D's)
D3398 BAR90-02LRH TSLP-2-7
D3399 BAR90-02LRH TSLP-2-7
TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N
CRITICAL L3398 650NH-5%-0.430MA-0.52OHM 0603
CRITICAL L3399 650NH-5%-0.430MA-0.52OHM 0603
NO_XNET_CONNECTION=TRUE
DP_B_AUXCH_DDC_P
DP_B_AUXCH_DDC_N
C3398 30PF 5% 50V C0G-NP0 0402
C3399 30PF 5% 50V C0G-NP0 0402
TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC
R3352 1M 5% 1/20W MF 201
R3351 1M 5% 1/20W MF 201
C3394 330PF 10% 16V X7R-CERM 0201
C3395 330PF 10% 16V X7R-CERM 0201
R3341 100K 5% 1/20W MF 201
C3302 0.01UF 10% 25V X5R-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

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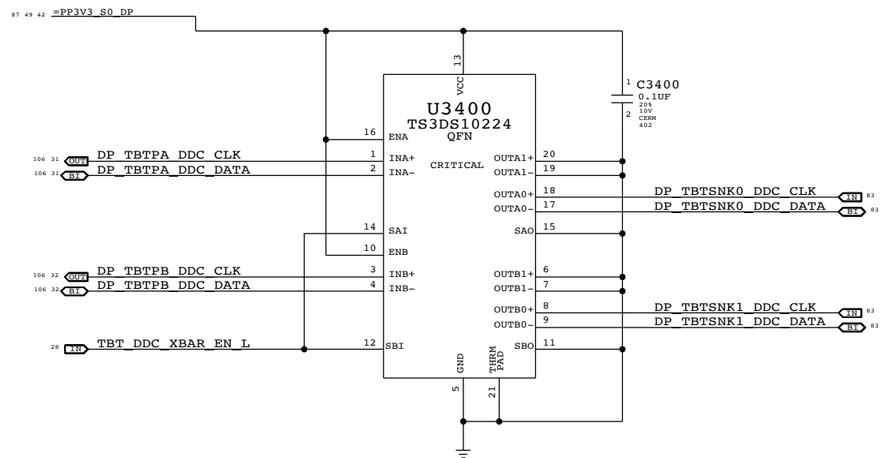
Dual-Port Host DDC Crossbar



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TBT DDC Crossbar

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AIRPORT BLUETOOTH

AP & BT Load Switch

SWITCH	TPS22924B
CHANNEL	N-TYPE
RDS(ON)	18.4 MOHM @3.3V
LOADING	2 A (EDP)

=PP3V3_S4_AP → U3510 TPS22924 CSP (A2, B2 VIN; A1, B1 VOUT; C2 ON; GND; CRITICAL; C1) ← AP_PWR_EN

PP3V3_S4_AP_FET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

CRITICAL L3502 FERR-220-OHM-2.5A 0603

PP3V3_S4_AP_FLT
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3502 0.1UF 10% 16V X7R-CERM 0402
C3503 0.1UF 10% 16V X7R-CERM 0402
C3504 10UF 20% 6.3V X5R 603

514S0335 CRITICAL
J3500 SSD-K99 F-RT-SM1

PCIE_AP_R2D_C_N → C3505 0.1UF 10% 16V X7R-CERM 0201 PLACE_NEAR=J3500.4:7mm
PCIE_AP_R2D_C_P → C3506 0.1UF 10% 16V X7R-CERM 0201 PLACE_NEAR=J3500.5:7mm

AP_EVENT_L
PCIE_AP_R2D_N
PCIE_AP_R2D_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_AP_D2R_P
PCIE_AP_D2R_N
AP_WAKE_L
AP_RESET_CONN_L
AP_CLKREQ_Q_L
USB_BT_MUX_N
USB_BT_MUX_P

=PP3V3_G3H_BT → U3540 TPS22924B CSP (A2, B2 VIN; A1, B1 VOUT; C2 ON; GND; CRITICAL; C1)

PP3V3_G3H_BT_FET
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

CRITICAL L3501 FERR-220-OHM-2.5A 0603

PP3V3_G3H_BT_FLT
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

C3507 0.1UF 10% 16V X7R-CERM 0402
C3508 10UF 20% 6.3V X5R 603

BT_RESET_MASK_L

BT_RESET_MASK_L GATES BT_PWR_RST_L
until after S0 GPIO is guranteed stable

CRITICAL Q3540 DMC2400UV SOT563 P-CHN

BT_PWR_RST_L

SMC_G3_WAKESRC_EN → R3542 10K 5% 1/16W MF-LF 402

BT_PWR_EN

Q3540 DMC2400UV SOT563 N-CHN

BT_PWR_RST → R3543 10K 5% 1/16W MF-LF 402 ; C3541 0.01UF 20% 16V CERM 402

Wake from BT in G3H circuit

SMC_PME_S4_WAKE_L

CRITICAL Q3501 SSM3K15AMFVAPE VESM

=PP3V3_G3H_BT → C3500 0.1UF 10% 10V X5R-CERM 0201

U3501 USB3740 DFN (VDD; CRITICAL)

USB_BT_N → DP_2
USB_BT_P → DM_2
USB_BT_WAKEN → DP_1
NC → DM_1
PM_SLP_S5_L → OE*
S
GND
DP → USB_BT_MUX_N
DM → USB_BT_MUX_P

SIGNAL_MODEL=SWI_USB3740_DFN_USB3740_MOJO

R3501 15K 5% 1/20W MF 201

Supervisor & CLKREQ# Isolation
Delay = 130 ms +/- 20%

PP3V3_S4_AP_FLT → R3530 100K 1% 1/16W MF-LF 402
=PP3V3_S4_AP → R3531 232K 1% 1/16W MF-LF 402

CRITICAL U3530 SLG4AP041V TDFN (VDD)

P3V3AP_VMON → SENSE, VREF
DLY
RESET* → AP_RESET_L
MR* ← AP_RESET_CONN_L
EN ← AP_PWR_EN
IN ← AP_CLKREQ_Q_L
OUT (OD) → AP_CLKREQ_L
THRM PAD, GND

C3530 0.1uF 10% 16V CERM 402

R3532 100K 1% 1/16W MF-LF 402

Q3570 SSM3K15AMFVAPE VESM CRITICAL

PP3V3_S4_AP_FLT → R3570 10K 5% 1/16W MF-LF 402

PCIE_WAKE_L → AP_WAKE_L

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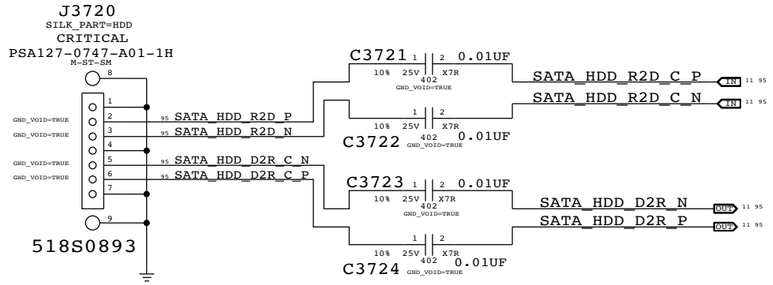
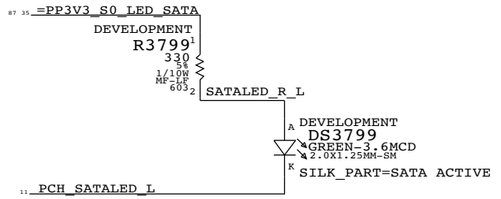
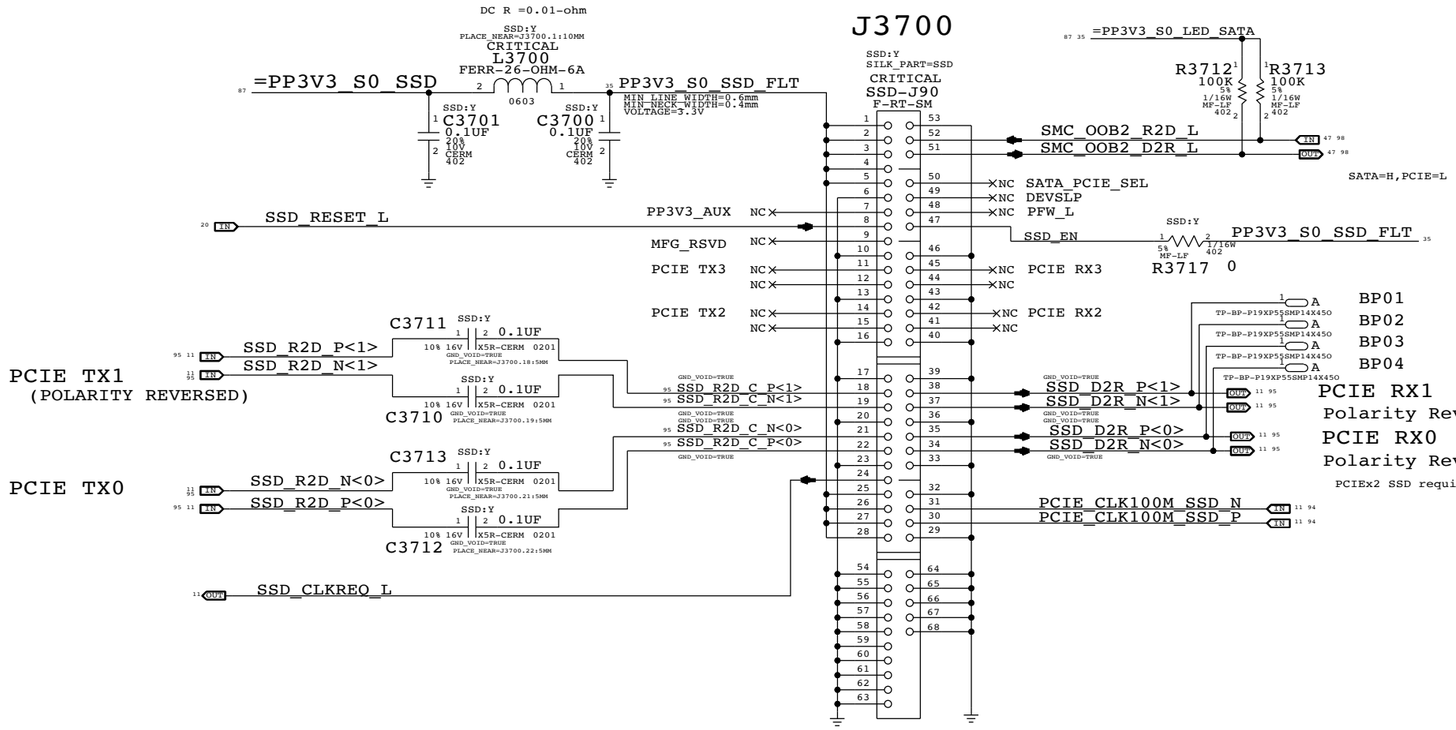
HDD SIGNAL CONNECTOR



SATA Activity LED



GS3 SSD



POR:514S0457 (tall)

SYNC_MASTER=J17_ULTIMATE	SYNC_DATE=05/16/2013
PAGE TITLE: SATA/SSD Connectors	
Apple Inc.	DRAWING NUMBER: 051-9884 SIZE: D
	REVISION: A.0.0
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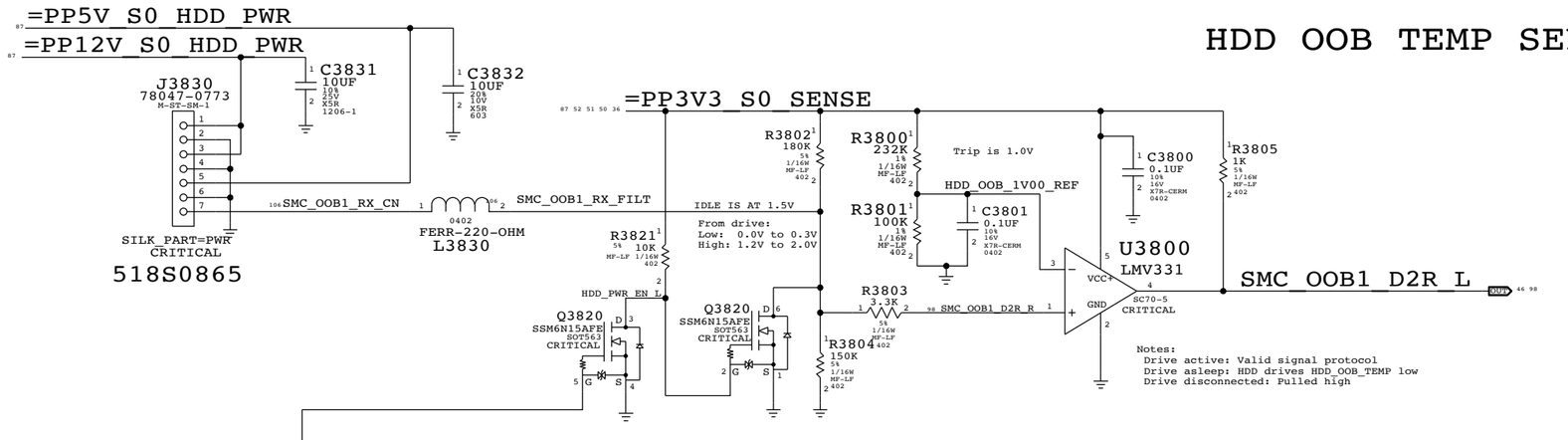
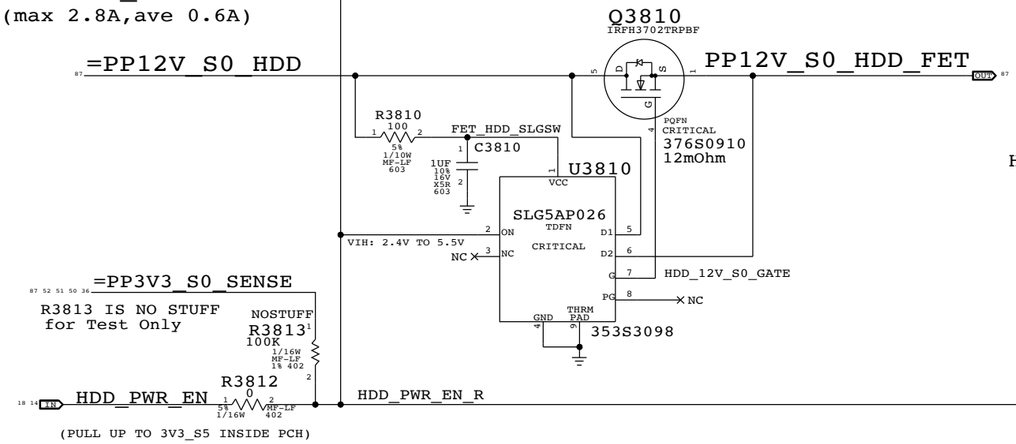
HDD POWER

HDD OOB TEMP SENSING

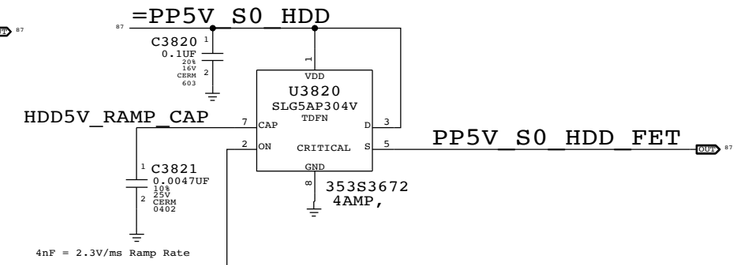


HDD 12V_S0 FET

(max 2.8A,ave 0.6A)



HDD 5V_S0 FET (max 0.7A,ave 0.3A)



REMOVE R3813 AND SHORT R3812 AFTER HDD_PWR_EN WORKS

SYNC MASTER=J17_ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE: HDD/SSD Temp Sense

Apple Inc.

DRAWING NUMBER: 051-9884 SIZE: D

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

87 38 37 =PP3V3_ENET_PHY

281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
38 =PP3V3R1V8_CR_VDDIO

ENET_SR_LX 38

=ENET_SR_VFB 38

Internal 1.2V Switching Regulator pins.

=PP1V2_ENET_PHY 38

396mA (1000base-T, Caesar II)

CRITICAL
L3900
FERR-600-OHM-300MA-0.85OHM
0402
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C3900 0.1UF 10% 16V X5R-CERM 0201
ENET_XTALVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

CRITICAL
L3905
FERR-600-OHM-300MA-0.85OHM
0402
PP3V3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL
L3910
FERR-600-OHM-300MA-0.85OHM
0402
PP3V3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201

CRITICAL
L3920
FERR-600-OHM-300MA-0.85OHM
0402
PP1V2_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL
L3925
FERR-600-OHM-0.5A
SM
PP1V2_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL
L3930
FERR-600-OHM-300MA-0.85OHM
0402
PP1V2_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.15 mm
VOLTAGE=1.2V
C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 20% 6.3V X5R-CERM1 402
C3916 0.1UF 10% 16V X5R-CERM 0201
C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

87 =PP3V3_S0_ENET
R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

C3950 0.1UF 10% 16V X5R-CERM 0201
C3951 0.1UF 10% 16V X5R-CERM 0201
C3955 0.1UF 10% 16V X5R-CERM 0201
C3956 0.1UF 10% 16V X5R-CERM 0201

94 13 OUT PCIE_ENET_D2R_N
94 13 OUT PCIE_ENET_D2R_P
94 13 IN PCIE_ENET_R2D_C_P
94 13 IN PCIE_ENET_R2D_C_N
38 OUT =ENET_WAKE_L
(See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
94 11 IN PCIE_CLK100M_ENET_P
94 11 IN PCIE_CLK100M_ENET_N
39 IN ENET_RESET_L
18 11 OUT ENET_CLKREQ_L
ENET_LOW_PWR
SMB_ENET_SCL
SMB_ENET_SDA
97 37 IN ENET_SCLK
97 37 IN ENET_MISO
97 37 IN ENET_MOSI
97 37 IN ENET_CS_L
38 OUT ENET_TRAFFICLED_L
96 19 IN SYSCLK_CLK25M_ENET
97 ENET_RDAC

R3965 1.24K 1% 1/16W MF-LF 402

U3900
BCM57766C0KMLG
QFN-8X8
OMIT_TABLE

42	AVDDH		
48			
37	BIASVDDH		
17	XTALVDDH		
7			
20	VDDO		
56			
62			
14	SR_VDD		
15	SR_VDDP		
16	SR_LX		
13	SR_VFB		
39			
45	AVDDL		
51			
29			
32	PCIE_PLLVDDL		
36	GPHY_PLLVDDL		
35	VDDC		
61			
58	VMAIN_PRSNT	(IPD-ENET)	
27	PCIE_TXD_N		
28	PCIE_TXD_P		
33	PCIE_RXD_P		
34	PCIE_RXD_N		
31	PCIE_REFCLK_P		
30	PCIE_REFCLK_N		
11	PERST*	(IPD)	
12	CLKREQ*	(OD)	
3	WAKE*	(OD)	
4	LOW_PWR	(IPD)	
6	SMB_CLK		
10	SMB_DATA	(IPD-ENETM)	
66	SCLK_SPD1000LED*		
64	SI/EEDATA		
65	SO_LINKLED*		
63	CS*/EECLK		
2	SPD100LED*/SERIAL_DO	(OD)	
67	TRAFFICLED*/SERIAL_DI	(OD)	
18	XTALI		
19	XTALO		
38	RDAC		
69	THRM_PAD		

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

TRD0_P	40	ENETCONN_MDI_P<0>	B1 38 97
TRD0_N	41	ENETCONN_MDI_N<0>	B1 38 97
TRD1_P	44	ENETCONN_MDI_P<1>	B1 38 97
TRD1_N	43	ENETCONN_MDI_N<1>	B1 38 97
TRD2_P	46	ENETCONN_MDI_P<2>	B1 38 97
TRD2_N	47	ENETCONN_MDI_N<2>	B1 38 97
TRD3_P	50	ENETCONN_MDI_P<3>	B1 38 97
TRD3_N	49	ENETCONN_MDI_N<3>	B1 38 97

PP3V3R1V8_ENET_LR_OUT 38
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.15 mm
VOLTAGE=3.3V

(IPD)	GPIO_0/CR_ACT_LED*	5	NC
	GPIO_1/LR_OUT	8	
	GPIO_2/MEDIA_SENSE	9	ENET_MEDIA_SENSE → OUT 11 97
(IPx-ENET)	SD_DETECT	1	ENET_SD_DETECT_L → IN 39 97
(IPU-ENET)	CR_CMD	26	97 ENET_SD_CMD — R3961 33 1/20W MF 201 — SDCONN_CMD IN 39 97
	CR_CLK	21	97 ENET_SD_CLK — R3979 33 1/20W MF 201 — SDCONN_CLK OUT 39 97
(IPU-ENET)	CR_DATA0	25	97 ENET_CR_DATA<0> — R3971 33 1/20W MF 201 — SDCONN_DATA<0> B1 39 97
	CR_DATA1	24	97 ENET_CR_DATA<1> — R3972 33 1/20W MF 201 — SDCONN_DATA<1> B1 39 97
	CR_DATA2	23	97 ENET_CR_DATA<2> — R3973 33 1/20W MF 201 — SDCONN_DATA<2> B1 39 97
	CR_DATA3	22	97 ENET_CR_DATA<3> — R3974 33 1/20W MF 201 — SDCONN_DATA<3> B1 39 97
	CR_DATA4	52	97 ENET_CR_DATA<4> — R3975 33 1/20W MF 201 — SDCONN_DATA<4> B1 39 97
	CR_DATA5	53	97 ENET_CR_DATA<5> — R3976 33 1/20W MF 201 — SDCONN_DATA<5> B1 39 97
	CR_DATA6	54	97 ENET_CR_DATA<6> — R3977 33 1/20W MF 201 — SDCONN_DATA<6> B1 39 97
	CR_DATA7	55	97 ENET_CR_DATA<7> — R3978 33 1/20W MF 201 — SDCONN_DATA<7> B1 39 97
(IPU-ENET)	MS_INS*	59	NC
(IPU-ENET)	CR_LED*/CR_BUS_PWR	60	ENET_CR_PWREN → OUT 39
(IPU-ENET)	CR_WP*	57	SDCONN_WP → IN 39
	SR_DISABLE	68	ENET_SR_DISABLE — R3981 1K 1/16W MF-LF 402

(See note)

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

ENET 1.2V SR IS ENABLED IF FLOATING.

ENET supports both active-levels for WP.

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT can only be used active low due to errata.

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE

If ENET switching regulator is used, this pin should have a 1K pull-down to GND

PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

87 38 37 =PP3V3_ENET_PHY
C3990 0.1UF 10% 16V X5R-CERM 0201
U3990
AT45DB011D
SOIC-8S1
OMIT_TABLE
VCC
SCK
CS*
WP*
RESET*
SI
SO
GND
97 37 IN ENET_SCLK
97 37 IN ENET_CS_L
ENET_MOSI IN 37 97
ENET_MISO OUT 37 97
NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
ETHERNET PHY (CAESAR IV)

Apple Inc.

DRAWING NUMBER 051-9884
SIZE D
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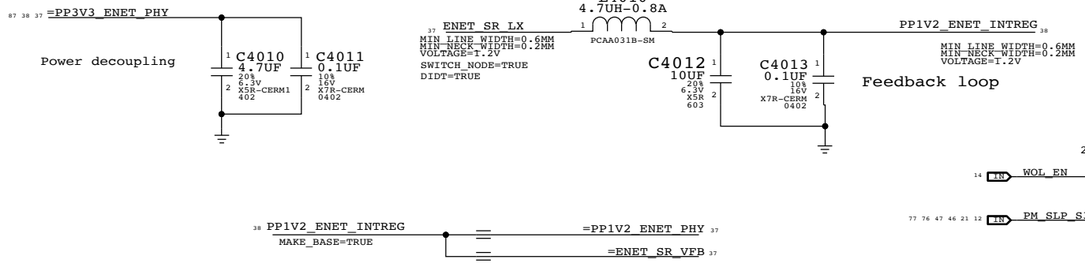
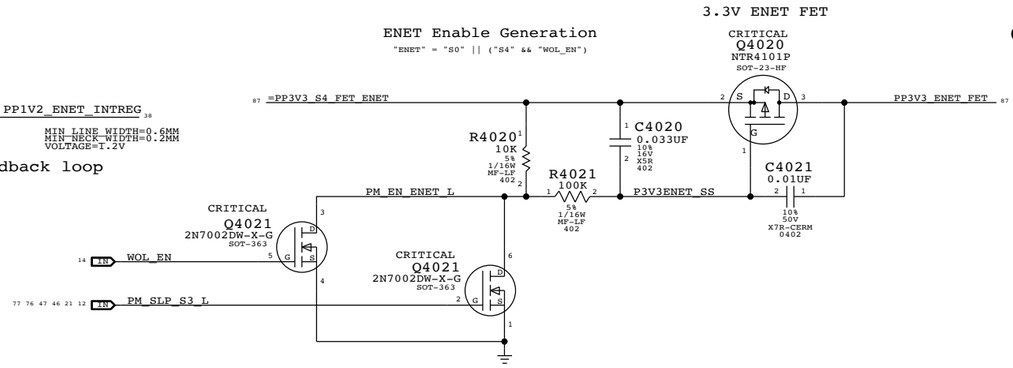
CAESAR IV 1.2V INT.VR CMPTS



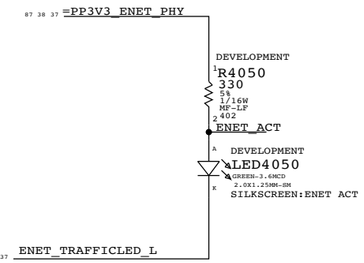
ENET Enable Generation

"ENET" = "S0" || ("S4" && "WOL_EN")

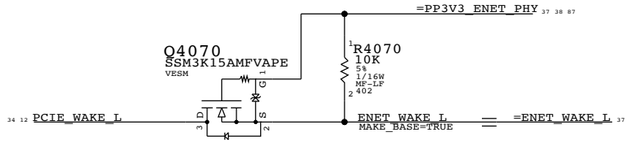
3.3V ENET FET

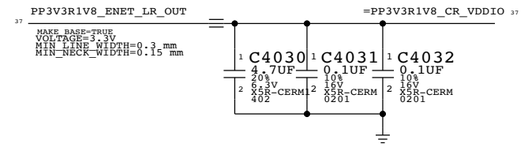


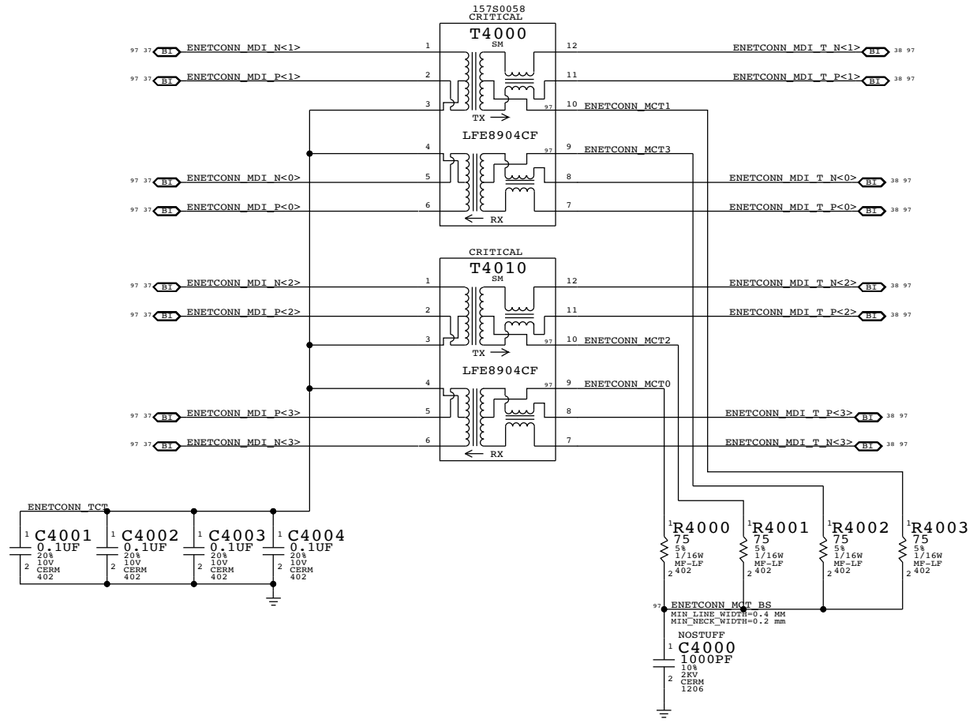
CAESAR IV ACTIVITY LED

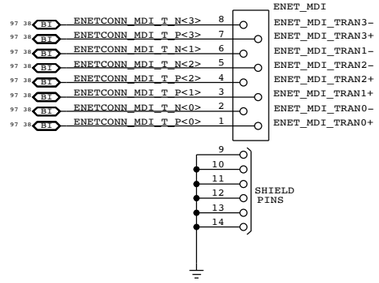


CAESAR IV WAKE# ISOLATION









SYNC MASTER=J17_ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE

Ethernet Support & Connector

Apple Inc.

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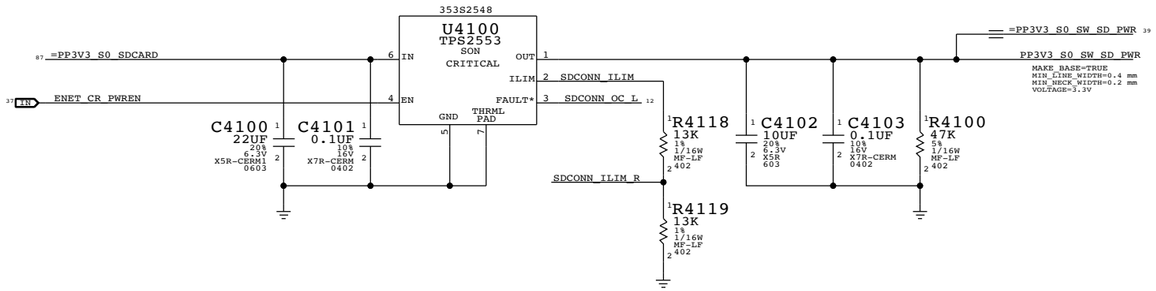
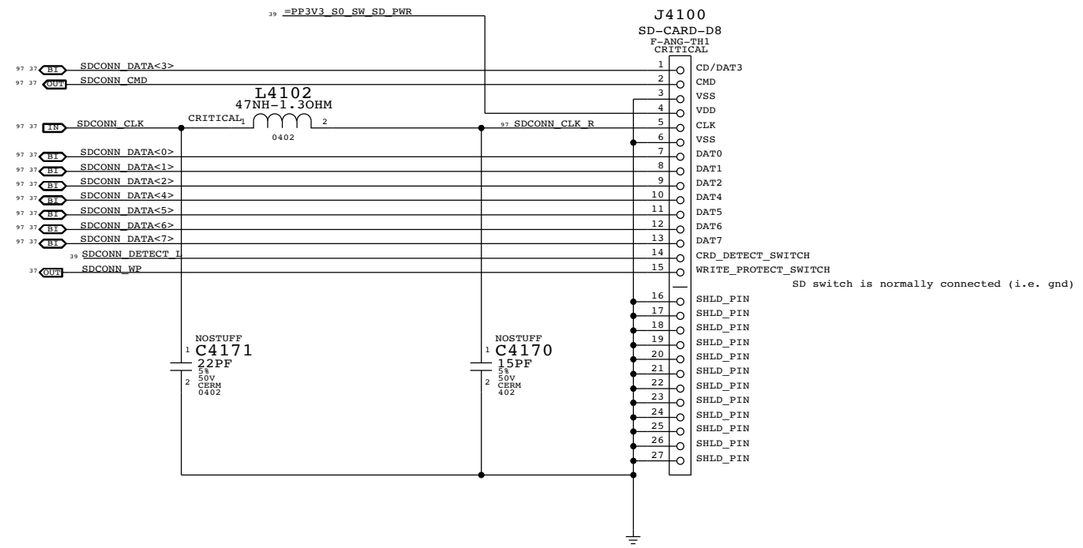
SD CARD 3.3V OVERCURRENT PROTECTION CHIP

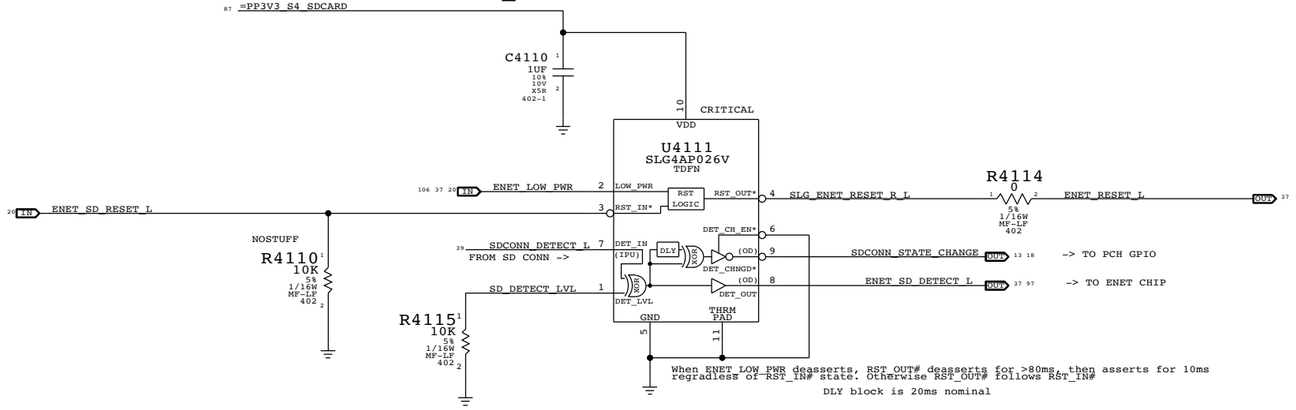


J16:516-0249 / J17:512-0038

SD CARD CONNECTOR



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE

SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

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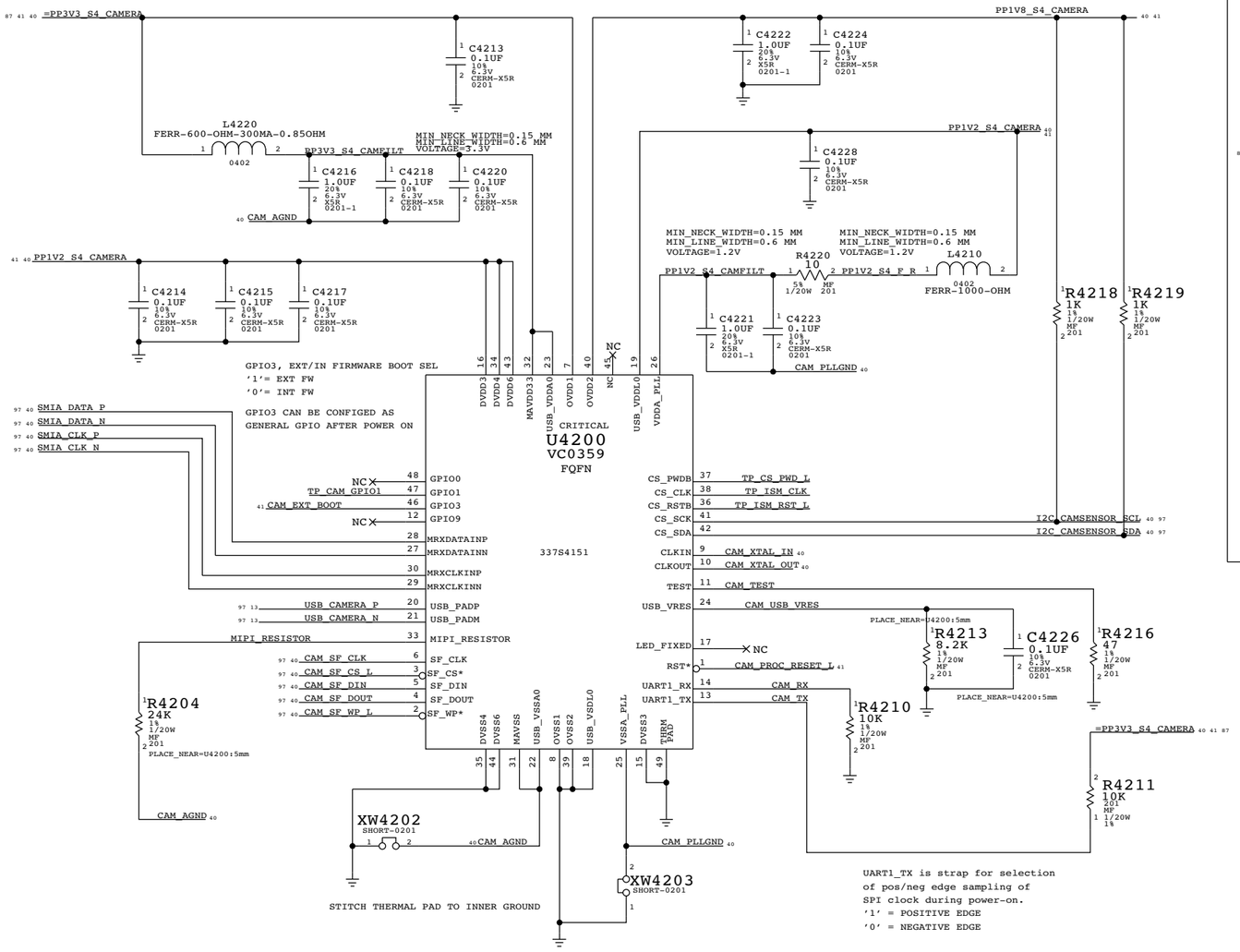
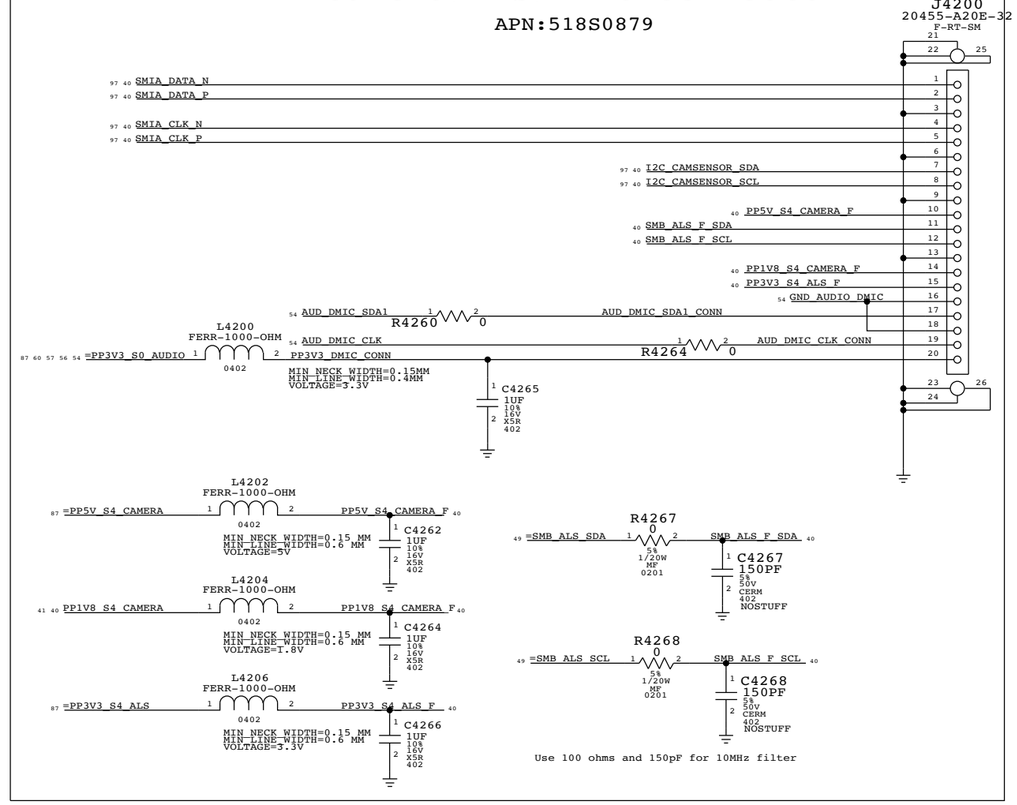
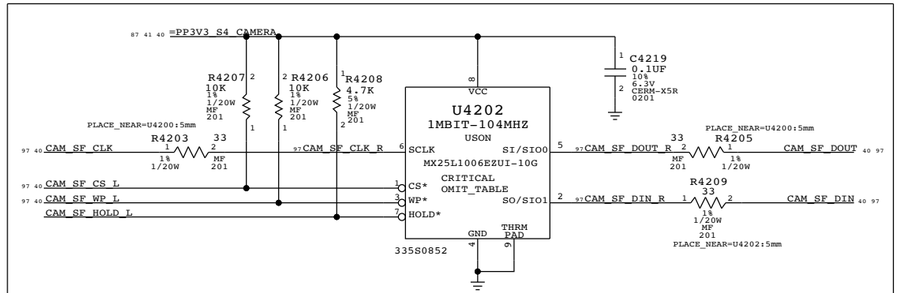
USB CAMERA CONTROLLER



Camera/ALS/DMIC connector

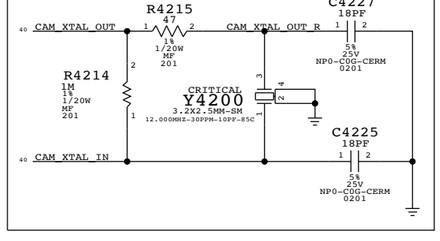
APN:518S0879





SERIAL FLASH

CRYSTAL



SYNC_MASTER=J17_ULTIMATE	SYNC_DATE=05/16/2013
PAGE TITLE	Camera Controller
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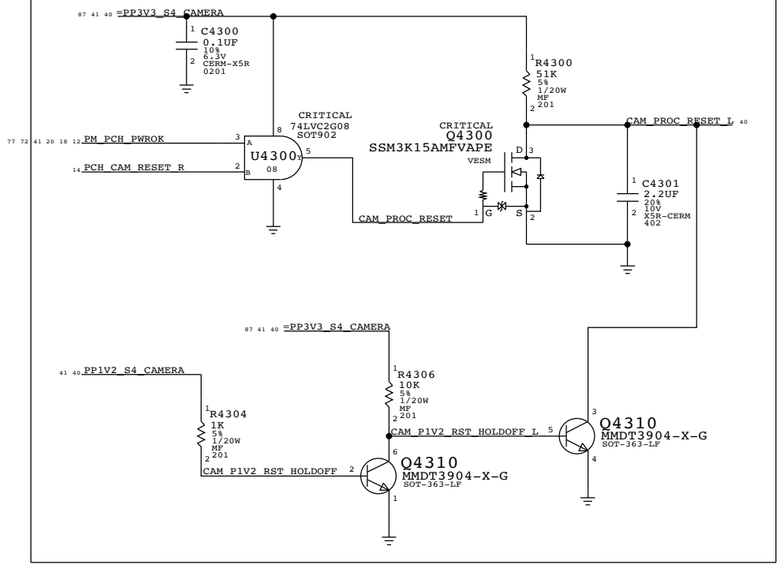
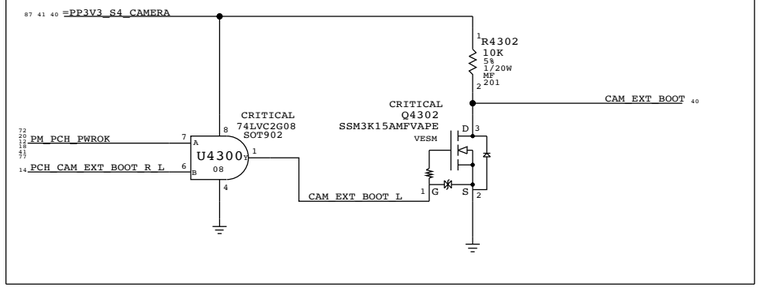
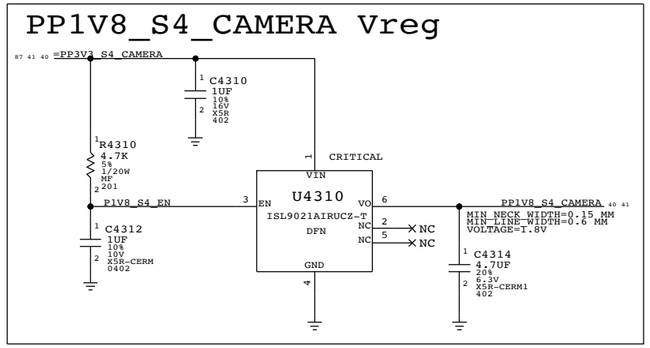
Camera Processor Reset



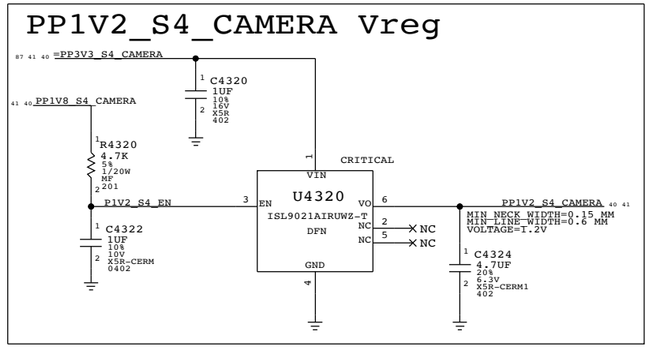
Camera Processor ExtBoot Cntl



PP1V8_S4_CAMERA Vreg



PP1V2_S4_CAMERA Vreg



SYNC MASTER=J17_ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE
Camera Controller Support

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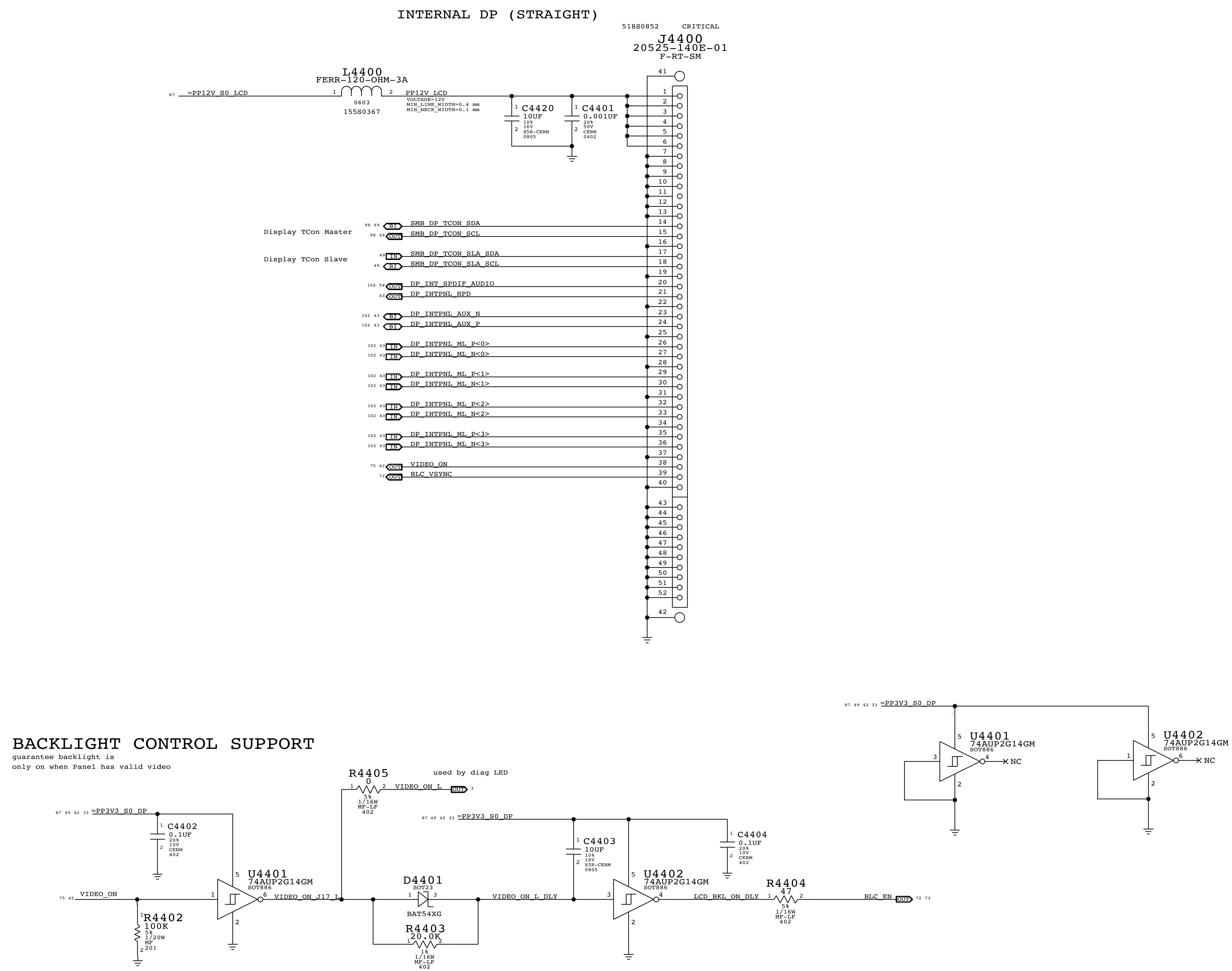
INTERNAL DP (STRAIGHT)
518S0852 CRITICAL
J4400
20525-140E-01
F-RT-SM
L4400
FERR-120-OHM-3A
0603
155S0367
=PP12V_S0_LCD
PP12V_LCD
VOLTAGE=12V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
C4420
10UF
10%
16V
X5R-CERM
0805
C4401
0.001UF
20%
50V
CERM
0402
Display TCon Master
SMB_DP_TCON_SDA
SMB_DP_TCON_SCL
Display TCon Slave
SMB_DP_TCON_SLA_SDA
SMB_DP_TCON_SLA_SCL
DP_INT_SPDIF_AUDIO
DP_INTPNL_HPD
DP_INTPNL_AUX_N
DP_INTPNL_AUX_P
DP_INTPNL_ML_P<0>
DP_INTPNL_ML_N<0>
DP_INTPNL_ML_P<1>
DP_INTPNL_ML_N<1>
DP_INTPNL_ML_P<2>
DP_INTPNL_ML_N<2>
DP_INTPNL_ML_P<3>
DP_INTPNL_ML_N<3>
VIDEO_ON
BLC_VSYNC
BACKLIGHT CONTROL SUPPORT
guarantee backlight is
only on when Panel has valid video
=PP3V3_S0_DP
C4402
0.1UF
20%
10V
CERM
402
VIDEO_ON
R4402
100K
5%
1/20W
MF
201
U4401
74AUP2G14GM
SOT886
VIDEO_ON_J17_L
R4405
0
5%
1/16W
MF-LF
402
VIDEO_ON_L
used by diag LED
D4401
SOT23
BAT54XG
R4403
20.0K
1%
1/16W
MF-LF
402
VIDEO_ON_L_DLY
C4403
10UF
10%
16V
X5R-CERM
0805
U4402
74AUP2G14GM
SOT886
C4404
0.1UF
20%
10V
CERM
402
LCD_BKL_ON_DLY
R4404
47
5%
1/16W
MF-LF
402
BLC_EN
NC
NC

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE

Internal DP Support

Apple Inc.

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TP to DP aliases

TP_DP_TBTSRC_ML_CP<0>	=	DP_TBTSRC_ML_P<0>
TP_DP_TBTSRC_ML_CN<0>	=	DP_TBTSRC_ML_N<0>
TP_DP_TBTSRC_ML_CP<1>	=	DP_TBTSRC_ML_P<1>
TP_DP_TBTSRC_ML_CN<1>	=	DP_TBTSRC_ML_N<1>
TP_DP_TBTSRC_ML_CP<2>	=	DP_TBTSRC_ML_P<2>
TP_DP_TBTSRC_ML_CN<2>	=	DP_TBTSRC_ML_N<2>
TP_DP_TBTSRC_ML_CP<3>	=	DP_TBTSRC_ML_P<3>
TP_DP_TBTSRC_ML_CN<3>	=	DP_TBTSRC_ML_N<3>
TP_DP_TBTSRC_AUXCH_CP	=	DP_TBTSRC_AUXCH_P
TP_DP_TBTSRC_AUXCH_CN	=	DP_TBTSRC_AUXCH_N

MAKE_BASE=TRUE

=PP1V5_S0_DP

R4510 470K 5% 1/20W MF 201

R4511 470K 5% 1/20W MF 201

C4508 0.1UF 10% 10V X5R 0201

C4509 0.1UF 10% 10V X5R 0201

DP_INT_EG_AUX_P

DP_INT_EG_AUX_N

DP_INT_EG_AUX_C_P

DP_INT_EG_AUX_C_N

=PP1V5_S0_DP

R4512 470K 5% 1/20W MF 201

R4513 470K 5% 1/20W MF 201

C4510 0.1UF 10% 10V X5R 0201

C4511 0.1UF 10% 10V X5R 0201

DP_TBTSRC_AUXCH_P

DP_TBTSRC_AUXCH_N

DP_TBTSRC_AUX_C_P

DP_TBTSRC_AUX_C_N

=PP3V3_S0_INTDPMUX

R4504 10K 5% 1/20W MF 201

DP_GPU_MUX_EN

DP_INT_EG_HPD

R4500 100K 5% 1/20W MF 201

DP_TBT_SEL

DP_TBTSRC_HPD

PD is on the LR page

U4500 CBTL06142EEE TFBGA CRITICAL

DP_INT_EG_ML_P<0>	B4	DIN1_0+	
DP_INT_EG_ML_N<0>	A4	DIN1_0-	
DP_INT_EG_ML_P<1>	B5	DIN1_1+	
DP_INT_EG_ML_N<1>	A5	DIN1_1-	
DP_INT_EG_ML_P<2>	B6	DIN1_2+	
DP_INT_EG_ML_N<2>	A6	DIN1_2-	
DP_INT_EG_ML_P<3>	A8	DIN1_3+	
DP_INT_EG_ML_N<3>	A9	DIN1_3-	
	H9	DAUX1+	
	J9	DAUX1-	
	H8	DDC_CLK1	NC
	J8	DDC_DAT1	NC
	J2	HPD_1	
DP_TBTSRC_ML_C_P<0>	B8	DIN2_0+	
DP_TBTSRC_ML_C_N<0>	B9	DIN2_0-	
DP_TBTSRC_ML_C_P<1>	D8	DIN2_1+	
DP_TBTSRC_ML_C_N<1>	D9	DIN2_1-	
DP_TBTSRC_ML_C_P<2>	E8	DIN2_2+	
DP_TBTSRC_ML_C_N<2>	E9	DIN2_2-	
DP_TBTSRC_ML_C_P<3>	F8	DIN2_3+	
DP_TBTSRC_ML_C_N<3>	F9	DIN2_3-	
	H6	DAUX2+	
	J6	DAUX2-	
	H5	DDC_CLK2	NC
	J5	DDC_DAT2	NC
	H3	HPD_2	
	A1	GPU_SEL	
	B7	XSD*	
	C2	DDC_AUX_SEL	
	B2	DOUT_0+	
	B1	DOUT_0-	
	D2	DOUT_1+	
	D1	DOUT_1-	
	E2	DOUT_2+	
	E1	DOUT_2-	
	F2	DOUT_3+	
	F1	DOUT_3-	
	H2	AUX+	
	H1	AUX-	
	J1	HPDIN	
	B3, C8, G8, H4, H7, G2	GND	
	A2, J4	VDD	

C4568 0.1UF 10% 10V X5R 0201

C4569 0.1UF 10% 10V X5R 0201

C4500 0.15UF 10% 6.3V X5R 0201

C4501 0.15UF 10% 6.3V X5R 0201

C4502 0.15UF 10% 6.3V X5R 0201

C4503 0.15UF 10% 6.3V X5R 0201

C4504 0.15UF 10% 6.3V X5R 0201

C4505 0.15UF 10% 6.3V X5R 0201

C4506 0.15UF 10% 6.3V X5R 0201

C4507 0.15UF 10% 6.3V X5R 0201

DP_INTPNL_ML_C_P<0> DP_INTPNL_ML_C_N<0> DP_INTPNL_ML_C_P<1> DP_INTPNL_ML_C_N<1> DP_INTPNL_ML_C_P<2> DP_INTPNL_ML_C_N<2> DP_INTPNL_ML_C_P<3> DP_INTPNL_ML_C_N<3>

DP_INTPNL_ML_P<0> DP_INTPNL_ML_N<0> DP_INTPNL_ML_P<1> DP_INTPNL_ML_N<1> DP_INTPNL_ML_P<2> DP_INTPNL_ML_N<2> DP_INTPNL_ML_P<3> DP_INTPNL_ML_N<3>

DP_INTPNL_AUX_P

DP_INTPNL_AUX_N

DP_INTPNL_HPD

R4502 100K 5% 1/20W MF 201

R4503 100K 5% 1/20W MF 201

=PP3V3_S0_INTDPMUX

NOSTUFF R4501 10K 5% 1/20W MF 201

U4500.A1:8MM

=PP1V5_S0_DP

R4590 0 5% 1/16W MF-LF 402

PP1V5_S0_DP_BIAS

MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=1.5V

C4590 1UF 10% 16V X5R 402

C4591 0.1UF 10% 16V X7R-CERM 0402

R4560 470K 5% 1/20W MF 201

R4561 470K 5% 1/20W MF 201

R4562 470K 5% 1/20W MF 201

R4563 470K 5% 1/20W MF 201

R4564 470K 5% 1/20W MF 201

R4565 470K 5% 1/20W MF 201

R4566 470K 5% 1/20W MF 201

R4567 470K 5% 1/20W MF 201

DP_TBTSRC_ML_P<0>	C4550 0.22UF	DP_TBTSRC_ML_C_P<0>
DP_TBTSRC_ML_N<0>	C4551 0.22UF	DP_TBTSRC_ML_C_N<0>
DP_TBTSRC_ML_P<1>	C4552 0.22UF	DP_TBTSRC_ML_C_P<1>
DP_TBTSRC_ML_N<1>	C4553 0.22UF	DP_TBTSRC_ML_C_N<1>
DP_TBTSRC_ML_P<2>	C4554 0.22UF	DP_TBTSRC_ML_C_P<2>
DP_TBTSRC_ML_N<2>	C4555 0.22UF	DP_TBTSRC_ML_C_N<2>
DP_TBTSRC_ML_P<3>	C4556 0.22UF	DP_TBTSRC_ML_C_P<3>
DP_TBTSRC_ML_N<3>	C4557 0.22UF	DP_TBTSRC_ML_C_N<3>

20% 6.3V X5R 0201

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE: Internal DP MUXing

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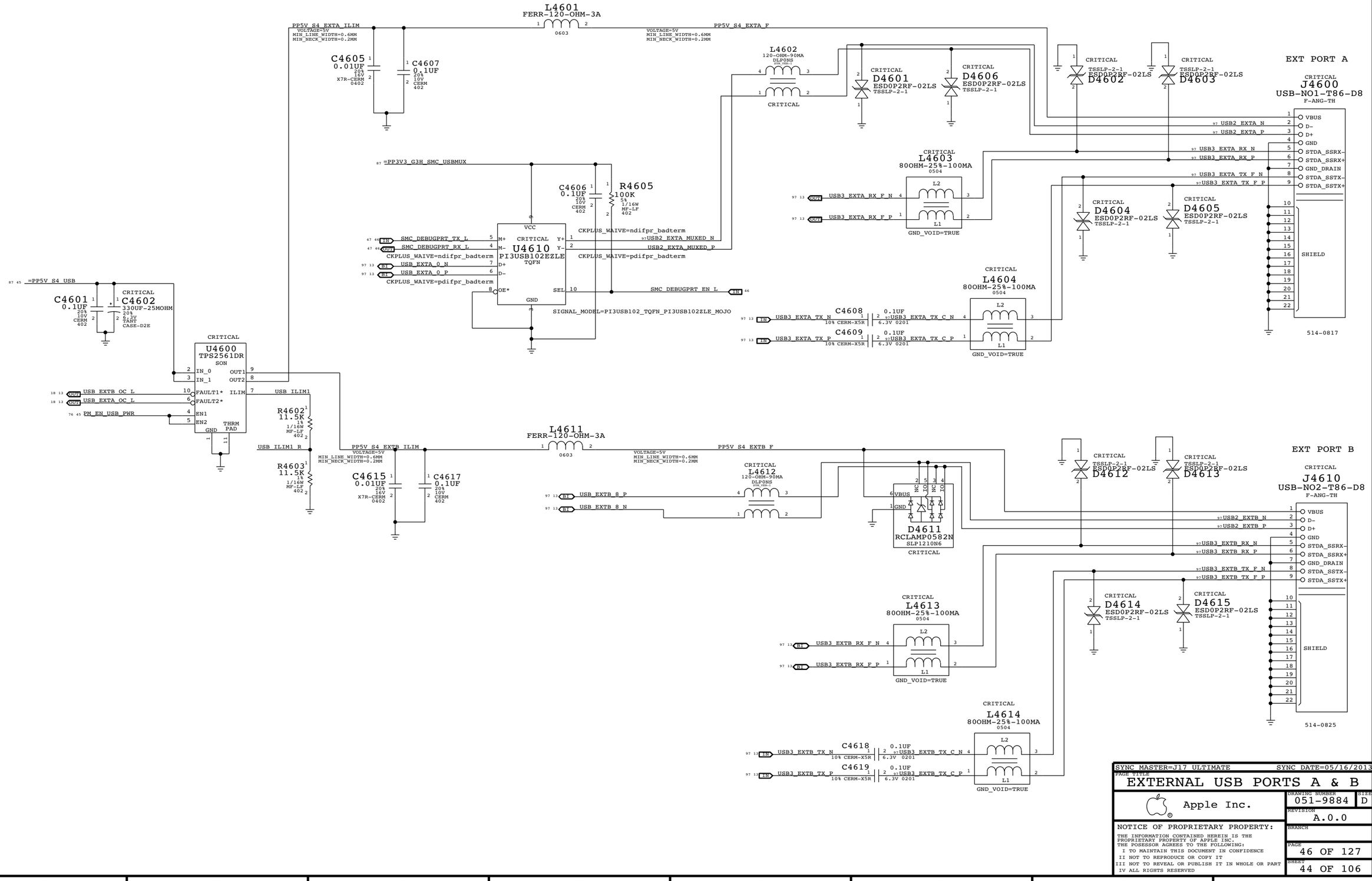

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

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EXTERNAL USB PORTS A & B

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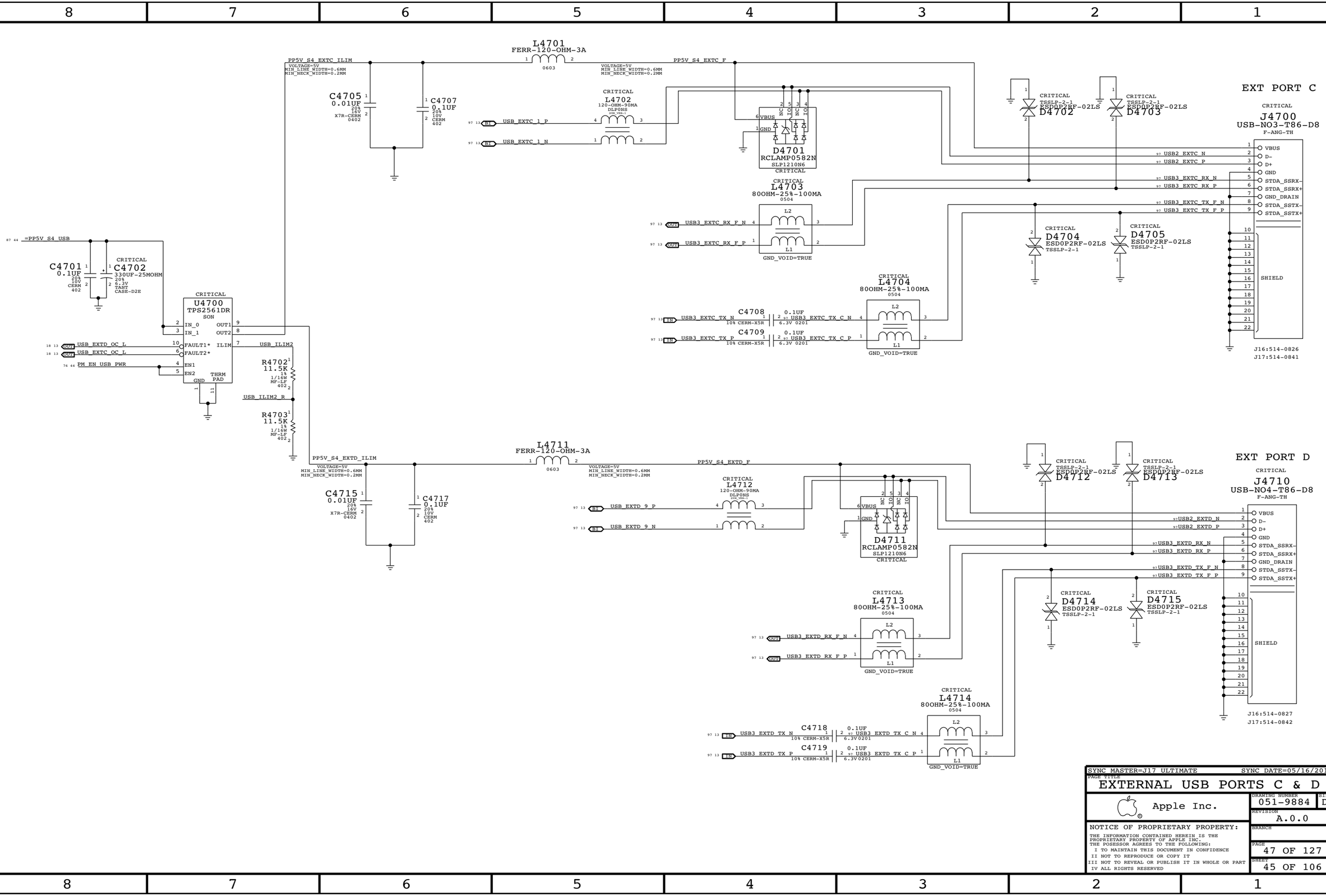

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

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EXTERNAL USB PORTS C & D

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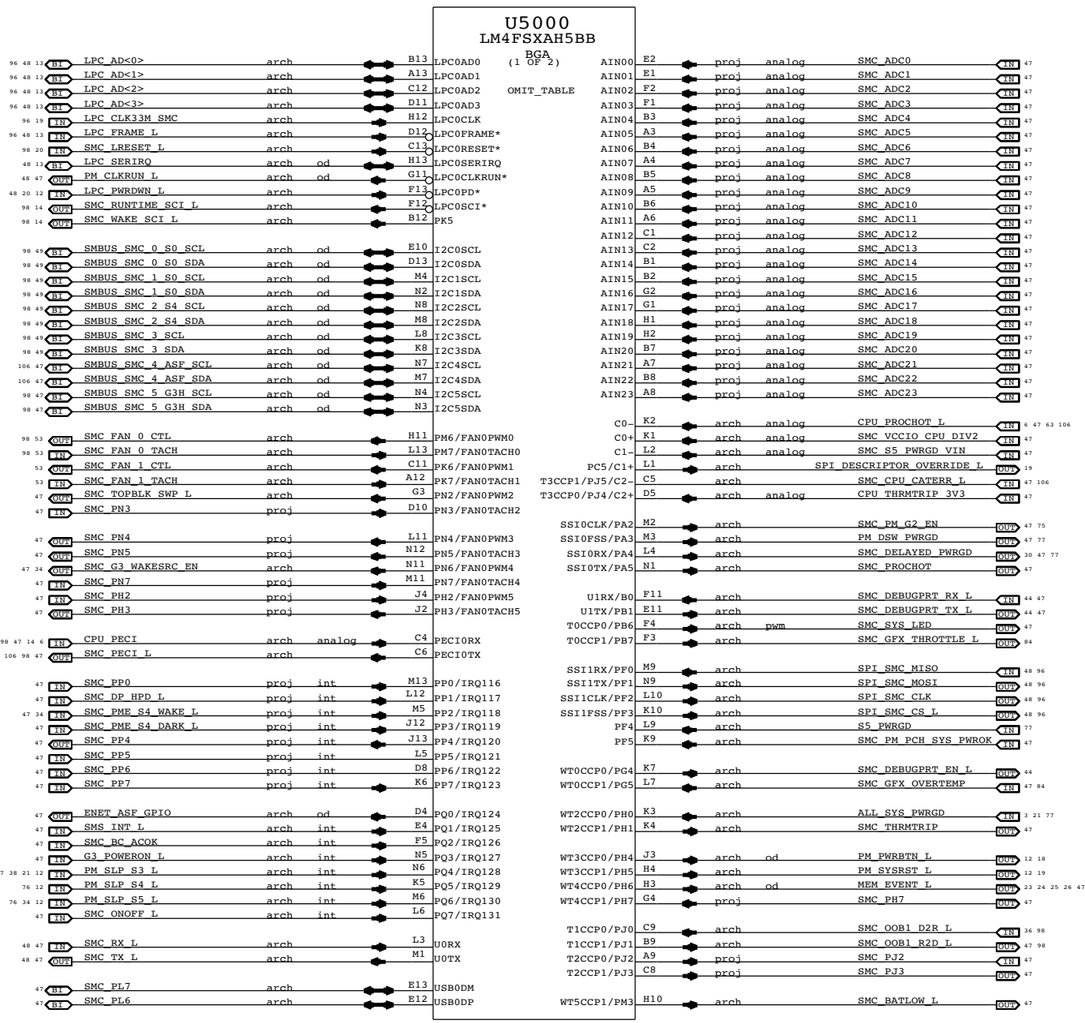
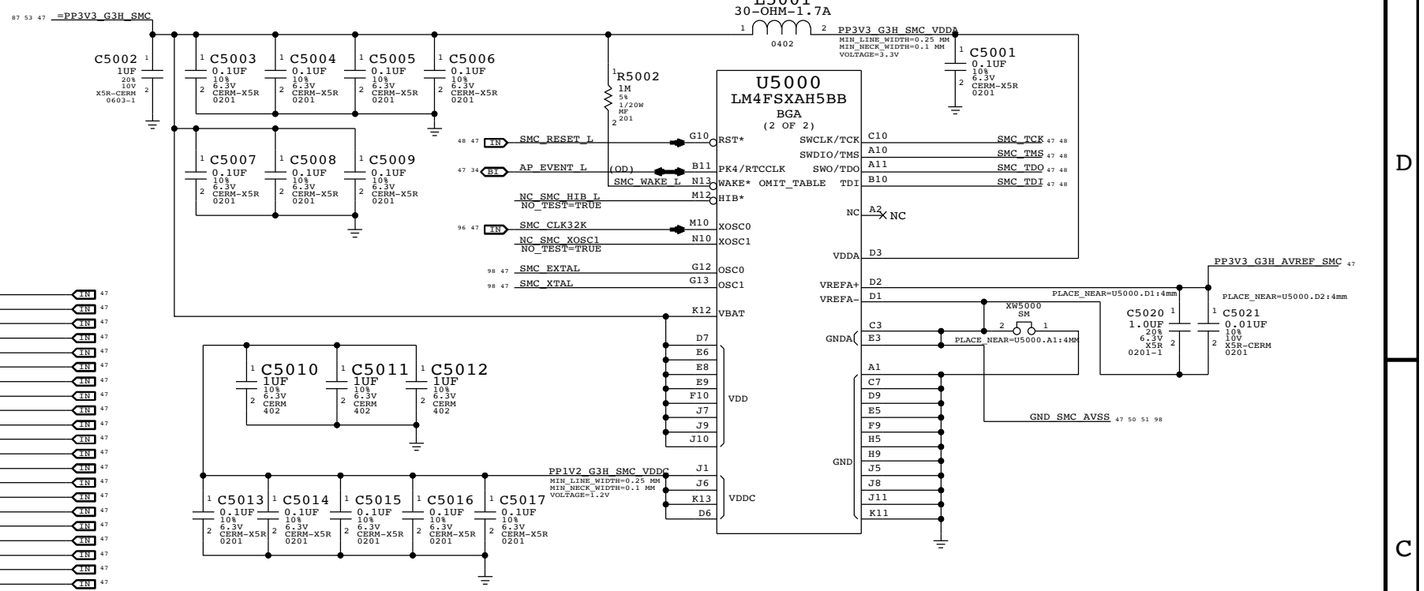
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





SYNC_MASTER=J17 ULTIMATE	SYNC_DATE=05/16/2013
PAGE TITLE: SMC	
Apple Inc.	DRAWING NUMBER: 051-9884 SIZE: D
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SMC Supervisor and AVREF Supply

=PP3V3_G3H_SMC → R5102 47 5% 1/16W MF-LF 402 → PP3V42_G3H_SMC_SPVSR (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.1MM, VOLTAGE=3.42V)

C5102 4.7UF 20% 6.3V X5R-CERM1 402

=PPVIN_G3H_SMCVREF

C5100 0.47UF 10% 6.3V CERM-X5R 402

U5100 VREF-3.3V-VDET-3.0V (DFN) — V+, VIN, NC, MR1*(ipu), MR2*(ipu), SN0903049, RESET*, DELAY, CRITICAL, REFOUT, THRM PAD, GND

R5105 100K 5% 1/16W MF-LF 402

R5103 0 5% 1/20W MF 0201 → SMC_RESET_L (OUT 46 48)

SMC_MANUAL_RST_L

C5101 0.01UF 10% 16V X7R-CERM 0402

C5105 1UF 20% 10V X5R-CERM 0603-1

C5106 0.01UF 10% 16V X7R-CERM 0402

NOSTUFF C5103 1000PF 5% 25V CERM 0402

PP3V3_G3H_AVREF_SMC (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.1MM, VOLTAGE=3.3V)

GND_SMC_AVSS (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.1MM, VOLTAGE=0V)

Note: IPU are pulled to VIN rail

ADC Channel Aliases

SMC_ADC0	VSNS_P12VG3H
SMC_ADC1	ISNS_P12VG3H
SMC_ADC2	VSNS_P12VS0_GPUCORE
SMC_ADC3	ISNS_P12VS0_GPUCORE
SMC_ADC4	VSNS_P1V5S0
SMC_ADC5	ISNS_P1V5S0
SMC_ADC6	VSNS_VDDQS3_DDR
SMC_ADC7	ISNS_VDDQS3_DDR
SMC_ADC9	ISNS_P12VS0_FBVDDQ
SMC_ADC10	VSNS_CPUVCC
SMC_ADC11	ISNS_CPUVCC
SMC_ADC12	VSNS_GPUCORE_ALT
SMC_ADC13	ISNS_GPUCORE_ALT
SMC_ADC14	VSNS_HDDS0
SMC_ADC15	ISNS_HDDS0
SMC_ADC17	VSNS_P1V05S0_PCH
SMC_ADC18	ISNS_P12VS0_HDD
SMC_ADC19	ISNS_P3V3S4_AP
SMC_ADC20	ISNS_SSDS0
SMC_ADC21	VSNS_P3V3S5
SMC_ADC8	VSNS_P12VS0_FBVDDQ

Unused ADC Channels

SMC_PH3	NC_SMC_PH3	
SMC_ADC16	NC_SMC_ADC16	NO_TEST=TRUE
SMC_ADC22	NC_SMC_ADC22	NO_TEST=TRUE
SMC_ADC23	NC_SMC_ADC23	NO_TEST=TRUE

Project-specific Aliases

SMC_PN5	ACDC_BURST_EN_L
SMC_PJ3	SMC_OOB2_R2D_L
SMC_PJ2	SMC_OOB2_D2R_L
SMC_PP0	SMC_ACDC_ID
SMC_PH2	SMC_ASSERT_RTCRST
SMC_PL6	SMC_WIFI_PWR_EN

Unused Project-specific

SMC_PL7	NC_SMC_PL7	NO_TEST=TRUE
SMC_PN3	NC_SMC_PN3	NO_TEST=TRUE
SMC_PN4	NC_SMC_PN4	NO_TEST=TRUE
SMC_PP4	NC_SMC_S4_WAKESRC_EN	NO_TEST=TRUE
SMC_PN7	NC_SMC_PN7	NO_TEST=TRUE
SMC_PP5	NC_SMC_PP5	NO_TEST=TRUE
SMC_PP6	NC_SMC_PP6	NO_TEST=TRUE
SMC_PP7	NC_SMC_PP7	NO_TEST=TRUE
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	NO_TEST=TRUE
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	NO_TEST=TRUE
SMC_PH7 (TP for access if ZPB re-intstated)	TP_SMC_PH7	NO_TEST=TRUE
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	NO_TEST=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	NO_TEST=TRUE
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	NO_TEST=TRUE
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	NO_TEST=TRUE
SMC_S5_PWRGD_VIN	NC_SMC_S5_PWRGD_VIN	NO_TEST=TRUE
SMC_OOB1_R2D_L	NC_SMC_OOB1_R2D_L	NO_TEST=TRUE
SMC_BATLOW_L	NC_SMC_SMC_BATLOW_L	NO_TEST=TRUE

SMC 32KHz Clock

PM_CLK32K_SUSCLK_R (IN) → R5160 22 5% 1/16W MF-LF 402 → SMC_CLK32K (OUT 46 96)

PLACE_NEAR=U1100.W36:12.7MM

SMC Crystal

NOTE: SMC team wants 12MHz for this Xtal

CRITICAL Y5165 12.000MHZ-50PPM-8PF-100OHM 5X3.2X1.2-SM

SMC_EXTAL (46 98) — NOSTUFF R5166 1M 5% 1/16W MF-LF 402 — SMC_XTAL_R — R5165 0 5% 1/16W MF-LF 402 — SMC_XTAL (46 98)

C5165 12PF 5% 50V C0G-CERM 0402

C5166 12PF 5% 50V C0G-CERM 0402

Power Button

=PP3V3_G3H_SMC (87 53 47 46) → R5120 10K 5% 1/20W MF 201

SILK_PART=PwrBtn

DEVELOPMENT J5120 NTC020AA1JB260T

SMC_ONOFF_L (MAKE_BASE=TRUE) (OUT 46)

PWR_BTN (OUT 62)

SMC Controlled RTC Reset

To absorb current from discharging RTC Reset CAP

CRITICAL Q5199 SSM3K15AMFVAPE VESM

RTC_RESET_L_R1 → R5194 330 5% 1/16W MF-LF 402 → RTC_RESET_L (OUT 11 19)

=PP3V3_S5_SMC (47) → R5199 10K 5% 1/16W MF-LF 402

NOSTUFF C5199 1.0UF 20% 6.3V X5R-CERM 0402

PROCHOT Support

Level-shifter that allows SMC to drive PROCHOT

CRITICAL Q5125 SSM3K15AMFVAPE VESM

CPU_PROCHOT_L (BI 6 46 63 106)

=PP1V05_S0_SMC (87 47) → R5123 51 1/20W MF 201

SMC_PROCHOT (IN 46)

PECI Support

Level-shifter that allows SMC to drive PECI

Place this circuit near the Tee point to minimize reflections

=PP1V05_S0_SMC (87 47)

CRITICAL Q5135 SSM3K15AMFVAPE VESM

SMC_PECI_L (IN 106 98 46) → R5135 0 5% 1/16W MF-LF 402

SMC_PECI_L_R → CPU_PECI_R → R5138 43 5% 1/16W MF-LF 402 → CPU_PECI (BI 6 14 46 98)

OMIT R5136 NOSTUFF NONE NONE NONE 402

R5137 330 5% 1/16W MF-LF 402

Comparator Reference

=PP1V05_S0_SMC (87 47)

R5130 10K 1% 1/16W MF-LF 402

PLACE_NEAR=U5000.K1:5MM

SMC_VCCIO_CPU_DIV2 (OUT 46)

PLACE_NEAR=U5000.K1:5MM — PLACE_NEAR=U5000.K1:3MM

R5131 10K 1% 1/16W MF-LF 402

C5131 0.1UF 10% 16V X7R-CERM 0402

Platform Thermal Control

PM_THRMTRIP_L (BI 14 106)

CRITICAL Q5123 SSM6N15AFE SOT563

SMC_GFX_OVERTEMP (IN 84 46) → R5124 10K 5% 1/20W MF 201

CRITICAL Q5123 SSM6N15AFE SOT563

=PP3V3_S0_SMC (87 84 47)

R5128 3.3K 5% 1/20W MF 201

3 CRITICAL Q5127 MMDT3904-X-G SOT-363-LF

SMC_ROMBOOT (IN 48) → R5125 1K 5% 1/20W MF 201 → R5126 10K 5% 1/20W MF 201

Note: For SMC recovery mode

SMC_THRMTRIP (IN 46)

CPU_THRMTRIP_3V3 (OUT 46)

CPU_THRMTRIP_L (IN 6) → R5127 3.3K 5% 1/20W MF 201 → CPU_TT_OC_L

6 CRITICAL Q5127 MMDT3904-X-G SOT-363-LF

See (RADAR://PROBLEM/11724870)
This circuit will not work.
Changing second stage to FET will not fix
S0 collapses before signal reaches 3.3
Solution will require latching of TT

Arch Pull Up/Down

=PP3V3_S0_SMC (87 84 47)

MEM_EVENT_L (46 26 25 24 23)	R5170	10K	1/20W MF 201
PM_CLKRUN_L (48 46)	R5171	10K	1/20W MF 201

=PP3V3_G3H_SMC (87 53 47 46)

ENET_ASF_GPIO (46)	R5175	10K	1/20W MF 201
G3_POWERON_L (46)	R5176	10K	1/20W MF 201
SMC_BC_ACOK (46)	R5178	100K	1/20W MF 201
SMC_SYS_LED (46)	R5179	100K	1/20W MF 201
SMS_INT_L (46)	R5180	10K	1/20W MF 201
SMC_PME_S4_WAKE_L (46 34)	R5181	10K	1/20W MF 201

PP3V3_S4_AP_FET (34)

AP_EVENT_L (46 34)	R5185	10K	1/20W MF 201
SMC_G3_WAKESRC_EN (46 34)	R5118	100K	1/20W MF 201
SMC_DELAYED_PWRGD (77 46 30)	R5186	100K	1/16W MF-LF 402
PM_DSW_PWRGD (77 46)	R5184	100K	1/16W MF-LF 402
SMC_PM_G2_EN (75 46)	R5187	100K	1/20W MF 201

Note:

Serial/JTAG Interface Pull-ups

=PP3V3_G3H_SMC (87 53 47 46)

SMC_TX_L (48 46)	R5190	10K	1/20W MF 201
SMC_RX_L (48 46)	R5191	100K	1/20W MF 201
SMC_TCK (48 46)	R5195	10K	1/20W MF 201
SMC_TDI (48 46)	R5196	10K	1/20W MF 201
SMC_TDO (48 46)	R5197	10K	1/20W MF 201
SMC_TMS (48 46)	R5198	10K	1/20W MF 201
SMC_DEBUGPRT_TX_L (47 46 44)	R5192	20K	1/20W MF 201
SMC_DEBUGPRT_RX_L (47 46 44)	R5193	20K	1/20W MF 201

AC/DC Burst Mode Enable

=PP3V3_S4_SMC (87) → R5141 10K 5% 1/20W MF 201 → BURSTMODE_EN_L (OUT 62 67)

=PP3V3_S5_SMC (87 47) → R5140 10K 5% 1/20W MF 201

CRITICAL Q5140 SSM6N15AFE SOT563

ACDC_BURST

CRITICAL Q5140 SSM6N15AFE SOT563

ACDC_BURST_EN_L (IN 47)

=PP3V3_S5_SMC (87 47) → C5140 0.1UF 10% 6.3V CERM-X5R 0201

U5140 TC7SZ08FEAPE SOT665

PM_SLP_S3_BUF_L

PM_SLP_S3_L (77 76 46 38 21 12)

Note:
Open-drain stage on S4 to account
case when SMC is initializing in S5,
and chip is not yet configured.
and ACDC_BURST_EN_L could be floating.

Connect BLC Serial through Mojo Mux

For a debug ability to communicate to BLC MCU through SMC

SMC_DEBUGPRT_TX_L (47 46 44) → NOSTUFF R5150 0 5% 1/16W MF-LF 402 → CRITICAL Q5150 SSM6N15AFE SOT563

SMC_DEBUGPRT_RX_L (47 46 44) → NOSTUFF R5151 0 5% 1/16W MF-LF 402 → CRITICAL Q5150 SSM6N15AFE SOT563

BLC_EXT_BOOT (IN 72 47)

SMC_TO_BLC_TX_L (10) → DP

SMC_TO_BLC_RX_L (9) → DM

=PP3V3_S0_SMC (47 84 87) → C5150 0.01UF 10% 16V X7R-CERM 0402

U5150 USB3740 (DFN)

VDD		
DP_2	6	SMC_BLC_MUX_TX_L (OUT 72)
DM_2	7	SMC_BLC_MUX_RX_L (IN 72)
DP_1	2	NC
DM_1	1	NC
OE*	3	
S	4	BLC_EXT_BOOT (IN 47 72)
GND	8	

SYNC_MASTER=J17_ULTIMATE	SYNC_DATE=05/16/2013
PAGE TITLE	SMC Support
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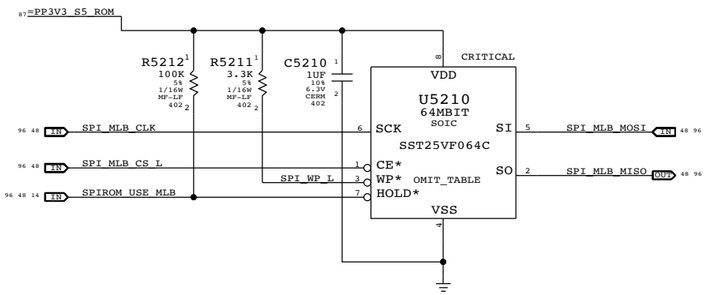
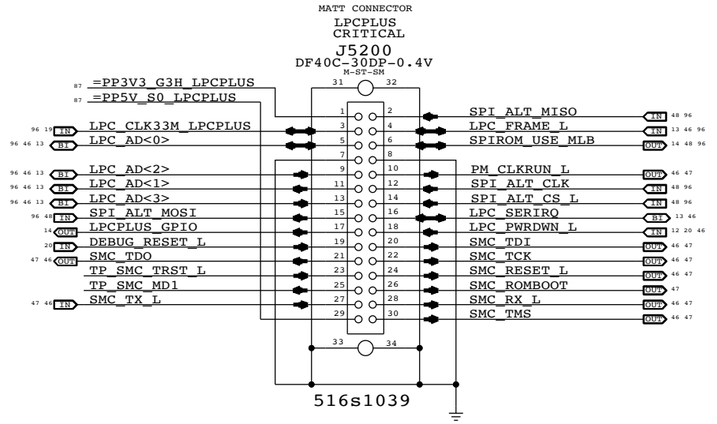
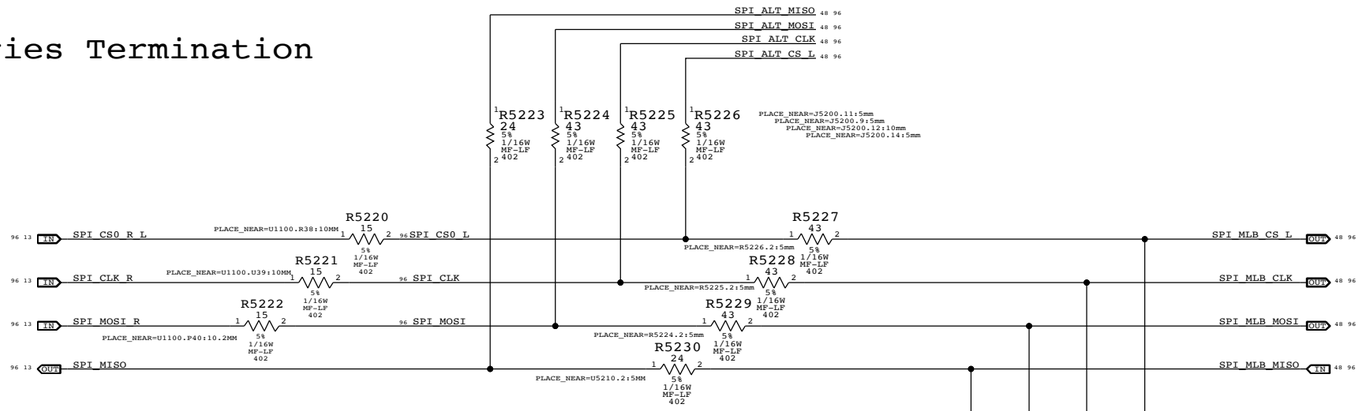
SPI BootROM



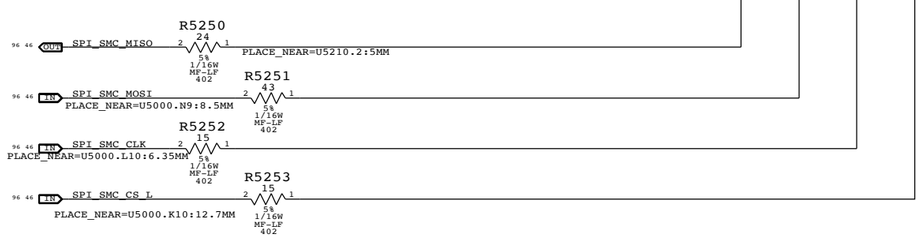
LPC+SPI Connector



SPI Series Termination



SMC SPI Support



SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE

SPI and Debug Connector

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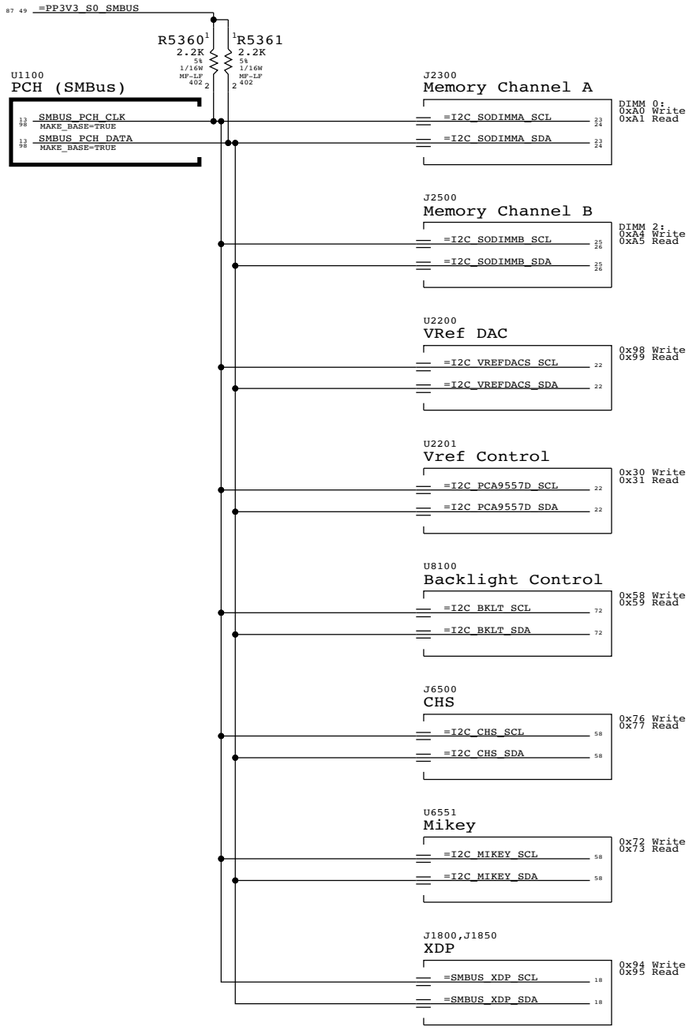
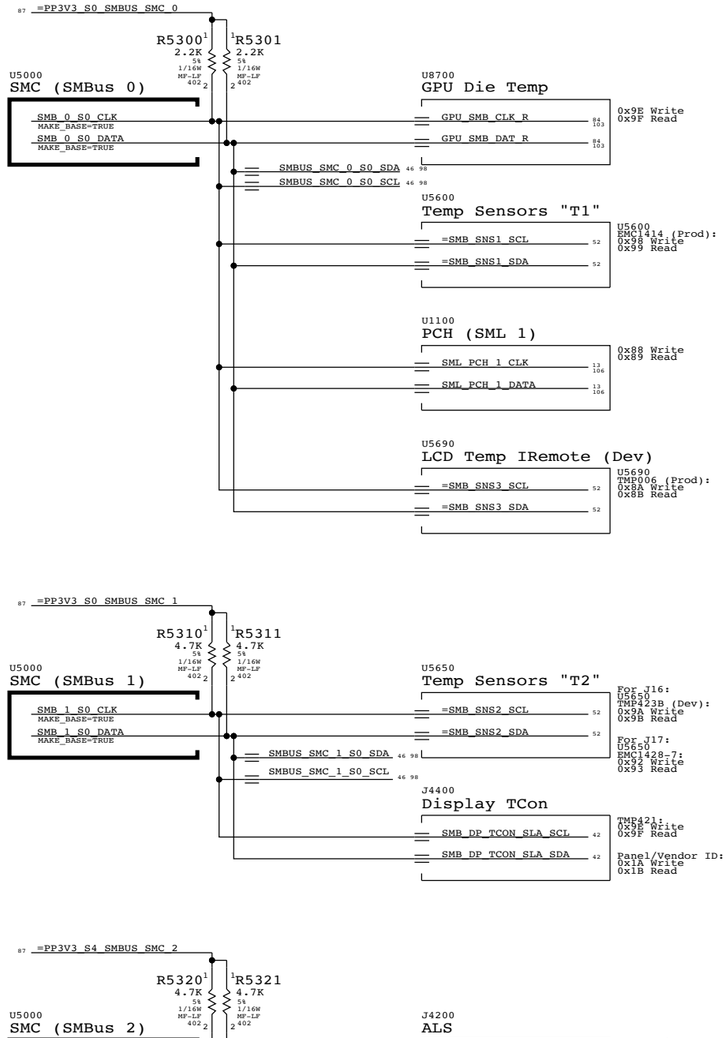
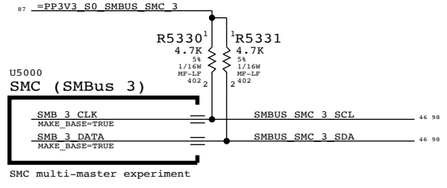
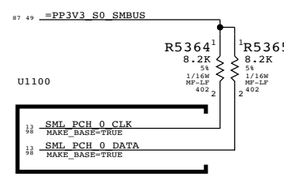


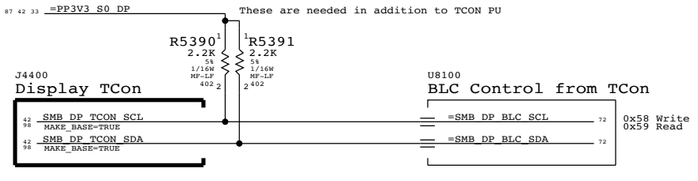


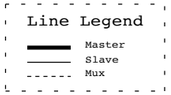


SMC multi-master experiment



Unused PCH SM Link





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SMBus Connections

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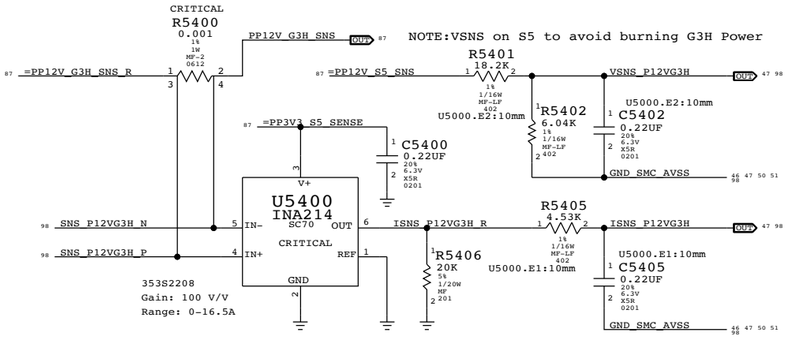
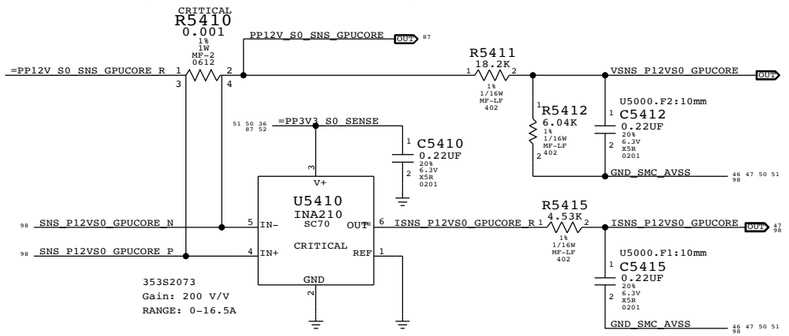
12V G3H (VD2R:ADC0/ID2R:ADC1) AC/DC lowside sense (System total)

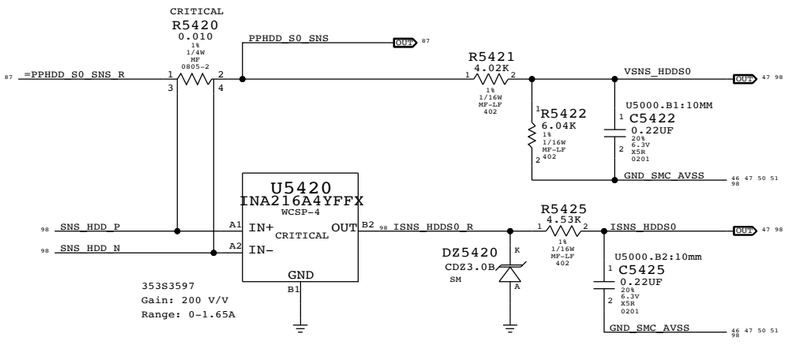


GPU Core (VG1C:ADC2/IG1C:ADC3) GPU highside sense for GPU Core Regulator

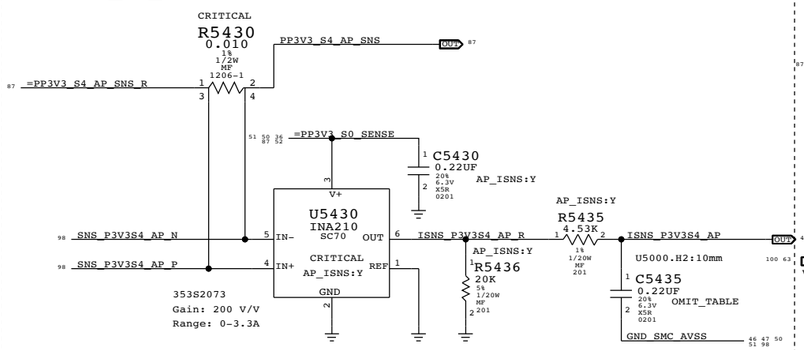


HDD S0 (VH05:ADC14/IH05:ADC15)

I/V-sense for HDD (Development, but need R5420)



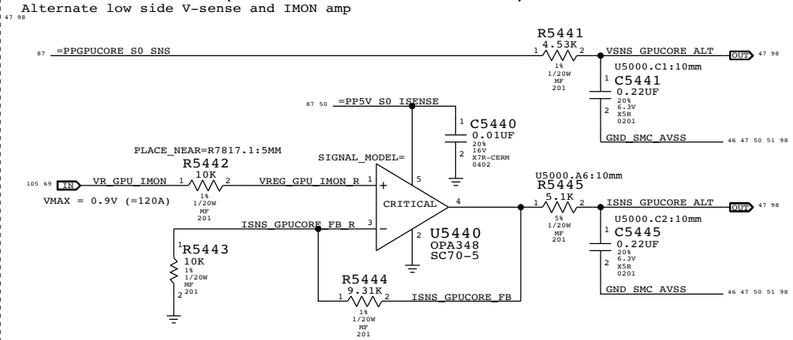
PP3V3_S4_AP (IW0R:ADC19) Airport supply current sense



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	1	CAP,0.22UF,201	C5435	AP_ISNS:Y
117S0201	1	RES,0 OHM,201	C5435	AP_ISNS:N

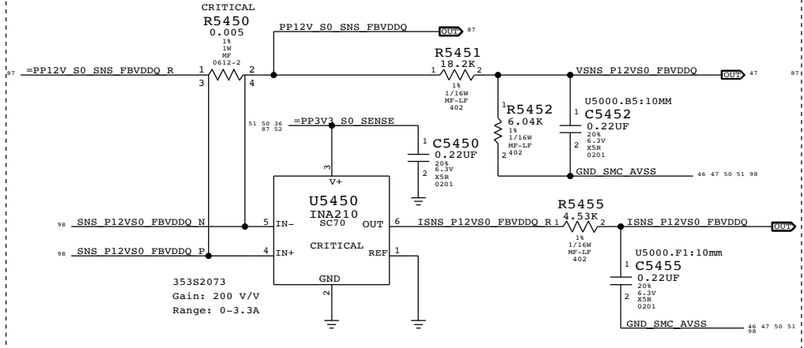
GPU Core - Alt (VG0C:ADC12/IG0C:ADC13)

Alternate low side V-sense and IMON amp



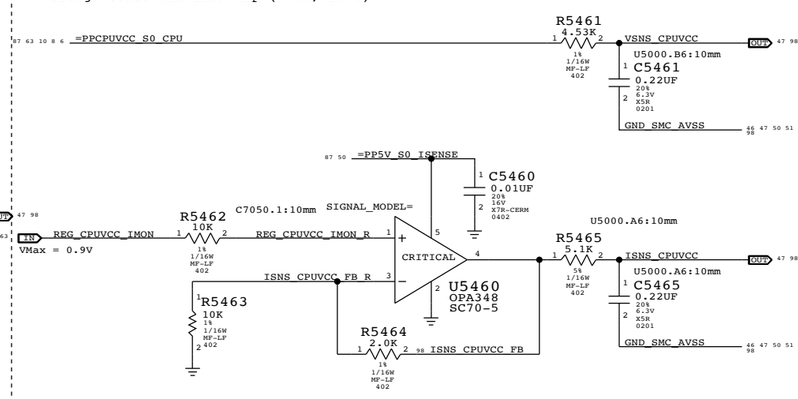
GPU FB (VG0F:ADC8/IG0F:ADC9)

GPU highside sense for GPU Frame Buffer 1.5V VDDQ Regulator



CPU Core (VC0C:ADC10/IC0C:ADC11)

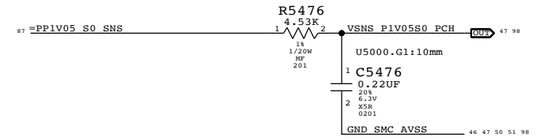
Voltage sense and IMON amp (VC0C, IC0C)



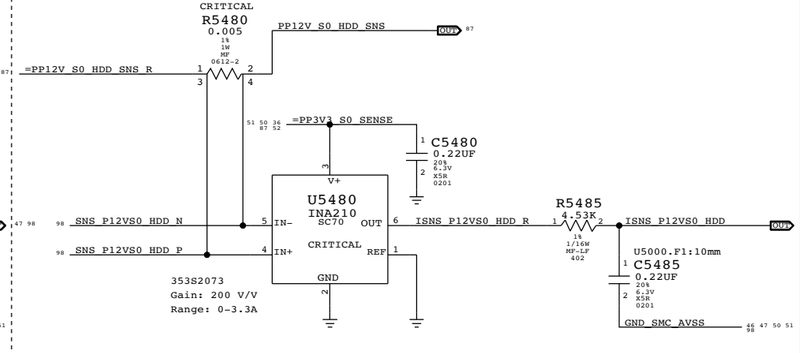
PP1V05_S0_PCH (VR1R:ADC17)

I/V-sense for PP1V05_S0_PCH

Since PP1V05 Vreg feedback is coming
from near GPU, place this sensor near PCH.



PP12V_S0_HDD (IH02:ADC18) HDD 12V CURRENT SENSE



SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

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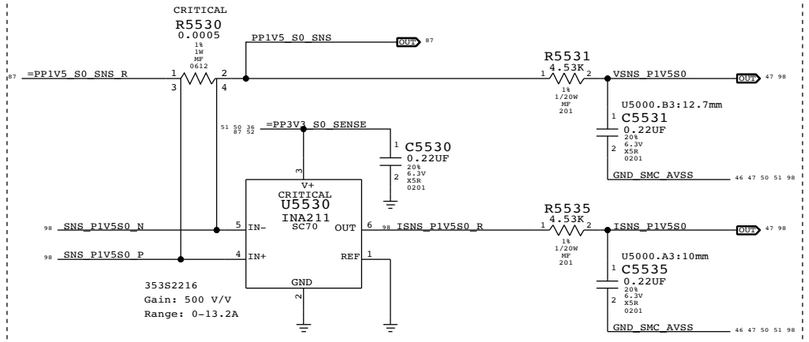
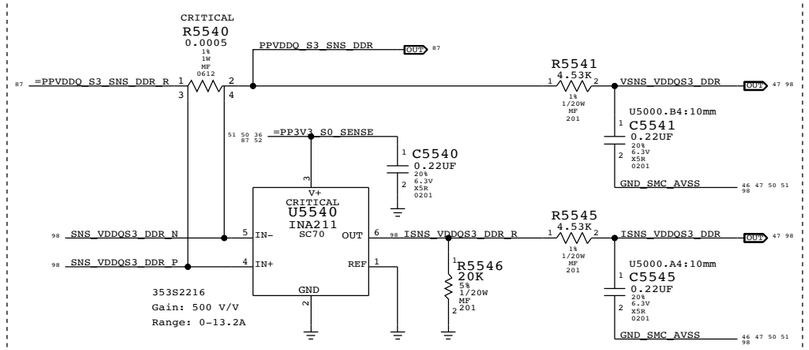
PP1V5_S0 (VC0M:ADC4/IC0M:ADC5)

lowside sense for VCCVRM,PCH,CPU mem, audio

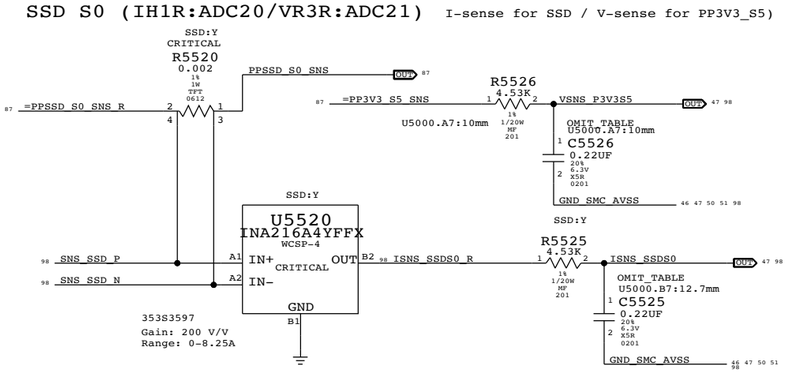


VDDQ S3 (VM0R:ADC6/IM0R:ADC7)

VDDQ lowside sense for SO-DIMM modules



SSD S0 (IH1R:ADC20/VR3R:ADC21) I-sense for SSD / V-sense for PP3V3_S5)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	2	CAP,0.22UF,201	C5525,C5526	SSD:Y
117S0201	2	RES,0 OHM,201	C5525,C5526	SSD:N

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE

I and V Sense(Continued)

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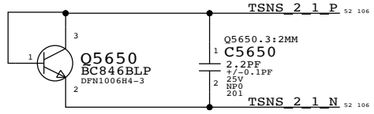
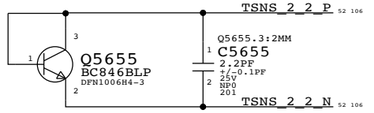
Temperature Sensor T2 EMC1428: Near GPU VR

GPU Proximity



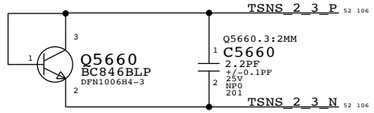
PLACEMENT_NOTE=Place Q5550 near GPU and GDDR5

Ambient



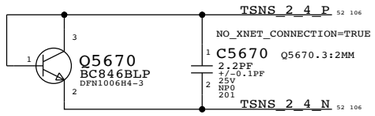
PLACEMENT_NOTE=Place Q5555 near bottom of board

BLC Proximity



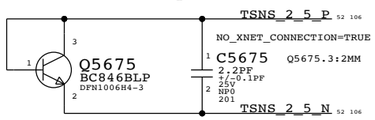
PLACEMENT_NOTE=Place Q5560 near BLC VR

SO-DIMM Proximity 1



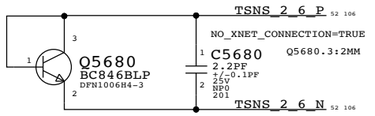
PLACEMENT_NOTE=Place Q5570 near SO-DIMM connectors (top left)

SO-DIMM Proximity 2



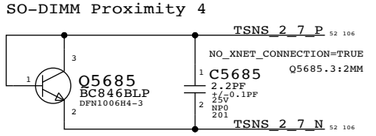
PLACEMENT_NOTE=Place Q5575 near SO-DIMM connectors (top right)

SO-DIMM Proximity 3



PLACEMENT_NOTE=Place Q5580 near SO-DIMM connectors (bottom left)

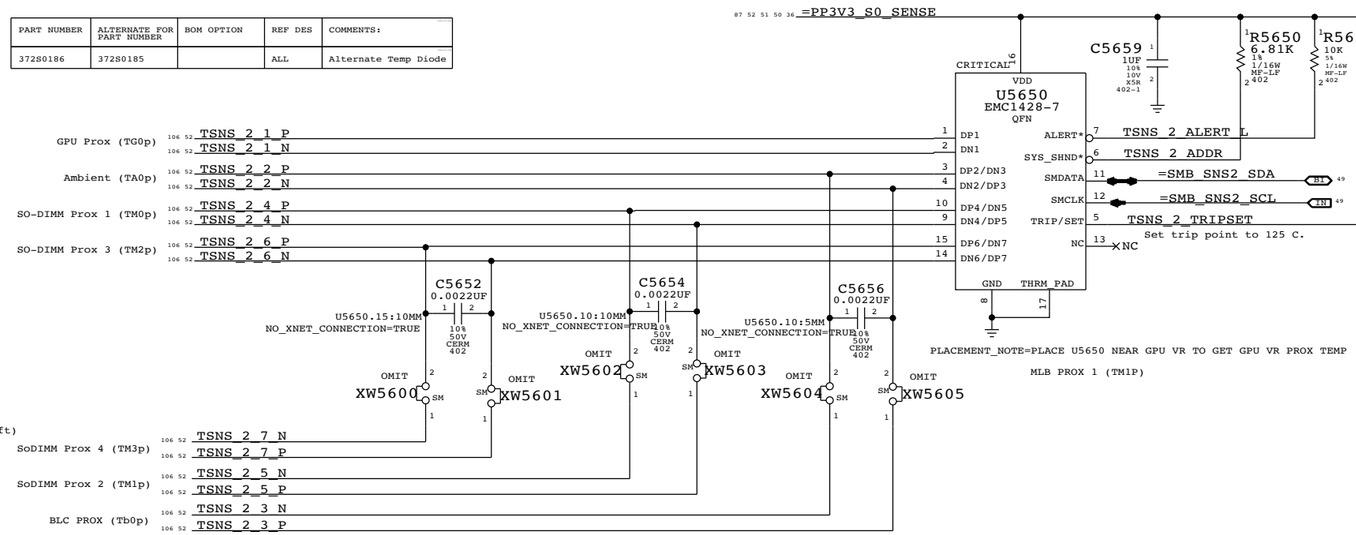
SO-DIMM Proximity 4



PLACEMENT_NOTE=Place Q5585 near SO-DIMM connectors (bottom right)

SNS T2: TEMP SENSOR IC

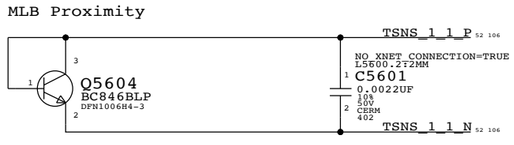
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode



EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

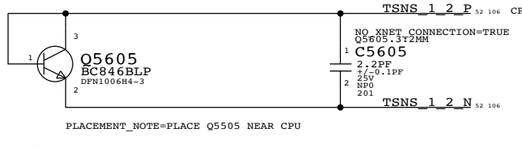
Temperature Sensor T1 EMC1414: Near PSU Conn

MLB Proximity



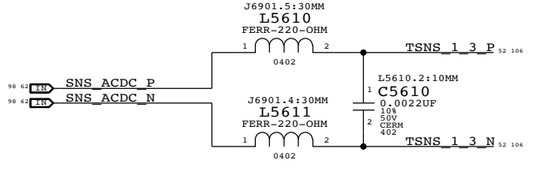
PLACEMENT_NOTE=PLACE Q5504 UNDER CPU

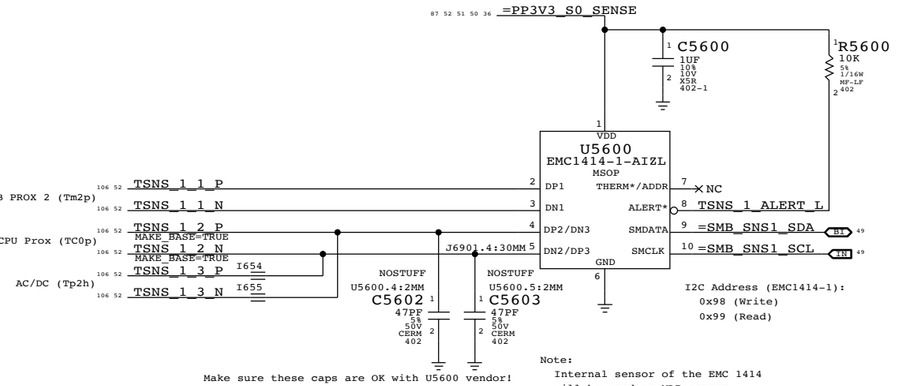
CPU Proximity



PLACEMENT_NOTE=PLACE Q5505 NEAR CPU

AC/DC Via connector to diode inside PSU



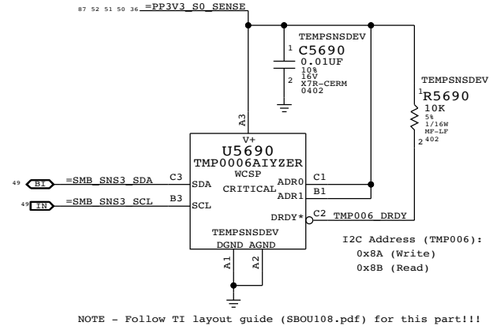


Make sure these caps are OK with U5600 vendor!

PLACEMENT_NOTE=PLACE U5600 NEAR PSU CONNECTOR

Note:
Internal sensor of the EMC 1414
will be used as MLB sensor.
MLB PROX 0 (Tm0p)

Temperature Sensor T3: LCD Remote Sensor(Dev Only)



NOTE - Follow TI layout guide (SBOU108.pdf) for this part!!!

SYNC MASTER=J17_ULTIMATE SYNC DATE=05/16/2013

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Temperature Sensors

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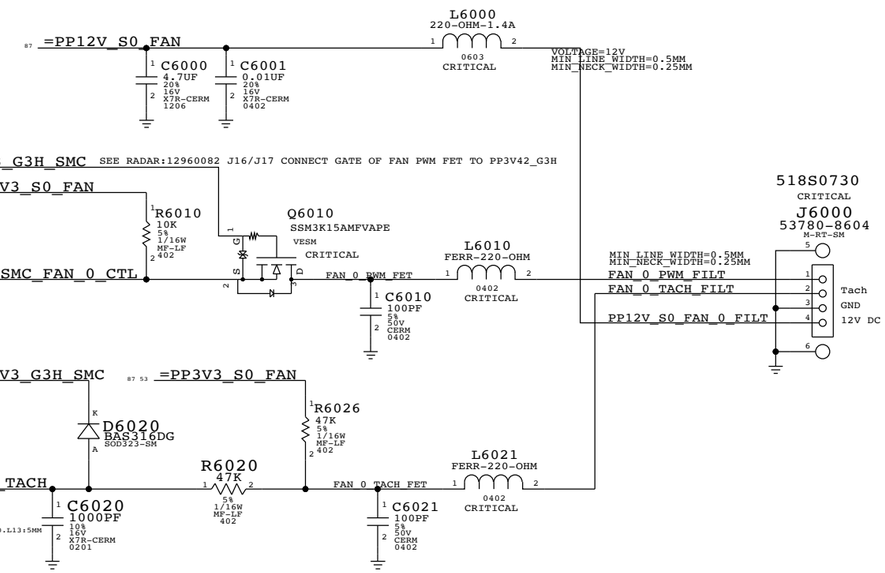
SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).



Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Proto1 Fan Tach instability.

SMC Fan 1 (Unused)

46 IN SMC_FAN_1_CTL — NC_SMC_FAN_1_CTL
MAKE_BASE=TRUE NO_TEST=TRUE

46 OUT SMC_FAN_1_TACH — NC_SMC_FAN_1_TACH
MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

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System Fan

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AUDIO CODEC

APPLE P/N 353S2592

PLACE C6100 AS CLOSE TO PIN 9 AS POSSIBLE

VD MUST BE LESS THAN OR EQUAL TO VL_HD

=PP1V5_S0_AUD_DIG

C6101 4.7UF 20% 4V X5R-1 402

C6100 0.47UF 10% 10V X5R 0402

GND_AUDIO_CODEC

PP4V5_AUDIO_ANALOG

R6100 2.67K 1% 1/16W MF-LF 402

C6109 2.2UF 20% 6.3V CERM 402-LF

C6110 2.2UF 20% 6.3V CERM 402-LF

C6108 10UF 20% 16V POLY-TANT CASE-B2-SM

VBIAS_DAC

CS4206_FP

CS4206_FN

U6101 CS4206B QFN

VD VA_REF VA_HP VA

DMICS 1 & 2 — AUD_DMIC_SDA1

NC — TP_AUD_GPIO_1

HP AMP CNTRL — AUD_GPIO_2

MAC SPKR AMP CNTRL — AUD_CODEC_MICBIAS

D6100 SOD-523 BAT54XV2T1

WIN SPKR AMP CNTRL — AUD_GPIO_3

AUD_SENSE_A

R6106 100K 1% 1/16W MF-LF 402

C6111 2.2UF 20% 6.3V CERM 402-LF

C6112 2.2UF 20% 6.3V CERM 402-LF

CS4206_FLYP

CS4206_FLYC

CS4206_FLYN

PLACE TP FOR ALL HDA SIGNALS NEAR CODEC

HDA_BIT_CLK

HDA_SYNC

HDA_SDIN0

R6101 22 5% 1/16W MF-LF 402

AUD_SDI_R

HDA_SDOUT

HDA_RST_L

DP_INT_SPDIF_AUDIO

AUD_SPDIF_CHIP

AUD_SPDIF_OUT

R6102 22 5% 1/16W MF-LF 402

R6103 100K 1% 1/16W MF-LF 402

DGND THRM_PAD AGND

DMICS SHOULD HAVE OWN GND ON CONNECTOR SHARED WITH CAMERA

GND_AUDIO_DMIC

MIN_LINE_WIDTH=0.20MM
MIN_NECK_WIDTH=0.15MM
VOLTAGE=0V

XW6100

GND_AUDIO_CODEC

C6102 0.47UF 10% 10V X5R 0402

C6103 10UF 20% 16V POLY-TANT CASE-B2-SM

C6105 1UF 10% 10V X5R 402-1

C6104 0.47UF 10% 10V X5R 0402

C6106 0.47UF 10% 10V X5R 0402

CRITICAL C6107 10UF 20% 16V X5R-CERM 0402-1

PP5V_AUDIO_HPAMP

=PP3V3_S0_AUDIO

PP4V5_AUDIO_ANALOG

GND_AUDIO_CODEC

R6105 0 5% 1/16W MF-LF 402

HPOUT_L — TP_AUD_HP_L NC

HPOUT_R — TP_AUD_HP_R NC

HPREF — CS4206_HPREF

LINEOUT_L1+ — AUD_LO1_L_P

LINEOUT_L1- — AUD_LO1_L_N

LINEOUT_R1+ — AUD_LO1_R_P

LINEOUT_R1- — AUD_LO1_R_N

HP AMP/LINE OUT TWEETERS

RESERVE SPACE FOR POSSIBLE LATCH CIRCUIT

LINEOUT_L2+ — AUD_LO2_L_P

LINEOUT_L2- — AUD_LO2_L_N

LINEOUT_R2+ — AUD_LO2_R_P

LINEOUT_R2- — AUD_LO2_R_N

WOOFERS

MICBIAS — AUD_CODEC_MICBIAS

VCOM — CS4206_VCOM

MIN_LINE_WIDTH=0.20MM
MIN_NECK_WIDTH=0.15MM

LINEIN_L+ — NO_TEST=TRUE — AUD_LI_P_L NC

LINEIN_C- — NO_TEST=TRUE — AUD_LI_COM NC

LINEIN_R+ — NO_TEST=TRUE — AUD_LI_P_R NC

MICIN_L+ — AUD_MIC_INL_P

MICIN_L- — AUD_MIC_INL_N

MICIN_R+ — NO_TEST=TRUE — AUD_MIC_INP_R NC

MICIN_R- — NO_TEST=TRUE — AUD_MIC_INN_R NC

VREF+_ADC — MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM — CS4206_VREF_ADC NC

DMIC_SCL — CS4206_DMIC_SCL

R6104 22 5% 1/16W MF-LF 402 — AUD_DMIC_CLK

CRITICAL C6113 1UF 10% 20V TANT CASE-P3-HF

CRITICAL C6114 10UF 20% 16V POLY-TANT CASE-B2-SM

C6115 0.47UF 10% 10V X5R 0402

R6107 100K 1% 1/16W MF-LF 402

R6108 100K 1% 1/16W MF-LF 402

R6109 100K 1% 1/16W MF-LF 402

R6110 100K 1% 1/16W MF-LF 402

R6111 100K 1% 1/16W MF-LF 402

Q6170_P_S

DEVEL_AUDIO CRITICAL Q6170 DMC2400UV SOT563

Q6170_P_G

R6170 0 5% 1/16W MF-LF 402

Q6170_N_G

Q6170_N_S

R6171 0 5% 1/16W MF-LF 402

Q6171_P_S

Q6171 DMC2400UV SOT563

Q6171_P_G

R6172 0 5% 1/16W MF-LF 402

Q6171_N_G

Q6171_N_S

R6173 0 5% 1/16W MF-LF 402

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

L6111 FERR-220-OHM 0402

MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=5V

PP5V_AUDIO_HPAMP

L6110 FERR-220-OHM 0402

=PP5V_S0_AUDIO

VR6101 TPS71745 SON CRITICAL

4V5_REG_IN

4V5_REG_EN

4V5_NR

PP4V5_AUDIO_ANALOG

MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.15MM
VOLTAGE=4.5V

R6120 0 5% 1/16W MF-LF 402

=PP3V3_S0_AUDIO

C6122 1UF 10% 10V X5R 402-1

XW6110

C6123 0.1UF 10% 16V X7R-CERM 0402

C6124 1UF 10% 10V X5R 402-1

MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM

GND_AUDIO_CODEC

MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

XW6111

GND_AUDIO_HPAMP

MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

PLACE XW6110 BENEATH U6101, BETWEEN PINS 2 & 5

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE

AUDIO: CODEC/REGULATORS

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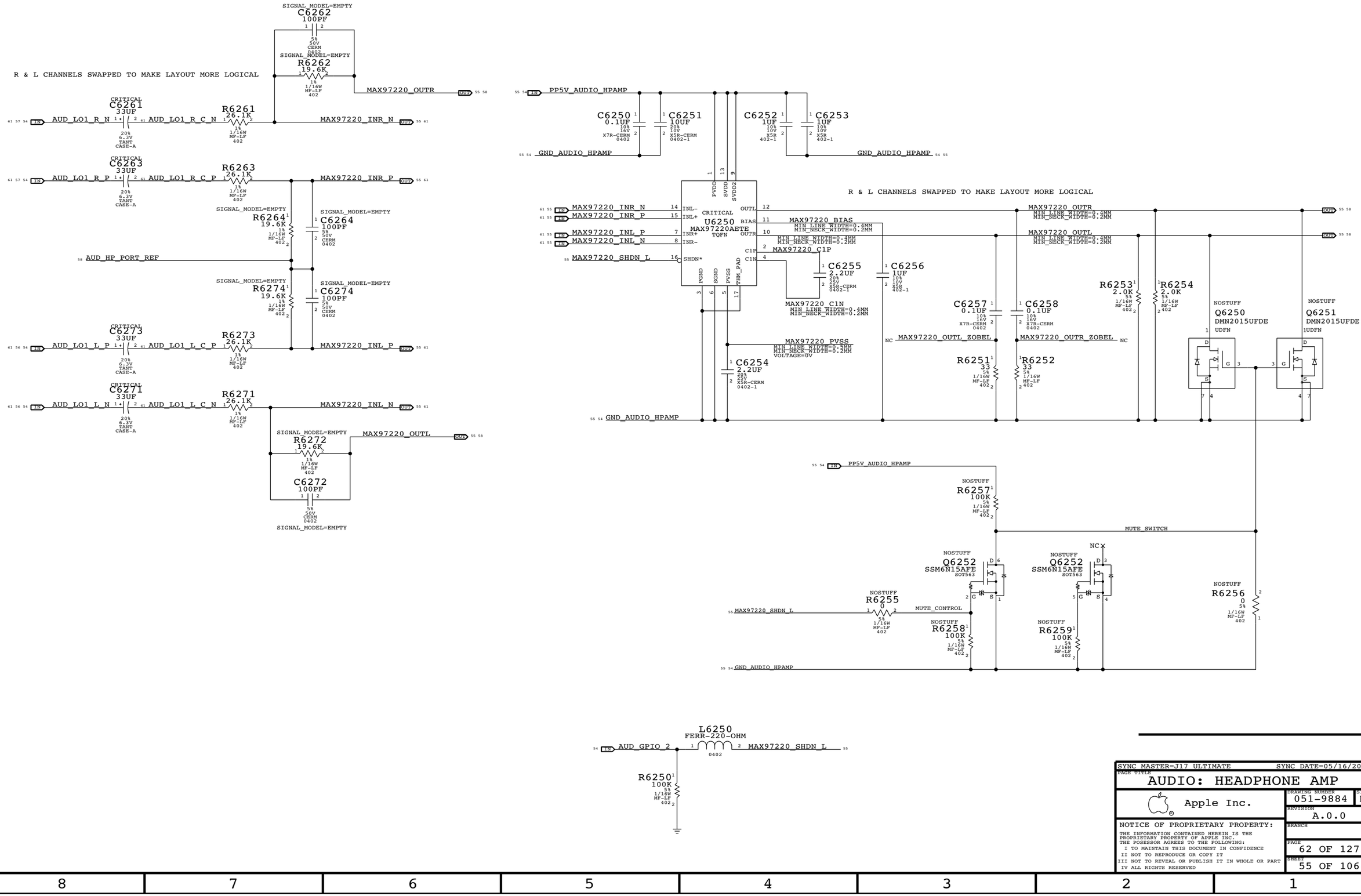
R & L CHANNELS SWAPPED TO MAKE LAYOUT MORE LOGICAL
C6262 100PF
R6262 19.6K
MAX97220_OUTR
C6261 33UF
R6261 26.1K
AUD_LO1_R_N
AUD_LO1_R_C_N
MAX97220_INR_N
C6263 33UF
R6263 26.1K
AUD_LO1_R_P
AUD_LO1_R_C_P
MAX97220_INR_P
R6264 19.6K
C6264 100PF
AUD_HP_PORT_REF
R6274 19.6K
C6274 100PF
C6273 33UF
R6273 26.1K
AUD_LO1_L_P
AUD_LO1_L_C_P
MAX97220_INL_P
C6271 33UF
R6271 26.1K
AUD_LO1_L_N
AUD_LO1_L_C_N
MAX97220_INL_N
R6272 19.6K
MAX97220_OUTL
C6272 100PF
SIGNAL_MODEL=EMPTY
CRITICAL
PP5V_AUDIO_HPAMP
GND_AUDIO_HPAMP
C6250 0.1UF
C6251 10UF
C6252 1UF
C6253 1UF
U6250 MAX97220AETE TQFN
PVDD
SVDD
SVDD2
INL-
INL+
INR+
INR-
SHDN*
OUTL
OUTR
BIAS
C1P
C1N
PGND
SGND
PVSS
THM_PAD
MAX97220_SHDN_L
MAX97220_BIAS
MAX97220_C1P
MAX97220_C1N
MAX97220_PVSS
C6255 2.2UF
C6256 1UF
C6254 2.2UF
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
C6257 0.1UF
C6258 0.1UF
MAX97220_OUTL_ZOBEL
MAX97220_OUTR_ZOBEL
R6251 33
R6252 33
R6253 2.0K
R6254 2.0K
NOSTUFF
Q6250 DMN2015UFDE
Q6251 DMN2015UFDE
UDFN
R6257 100K
MUTE_SWITCH
Q6252 SSM6N15AFE
SOT563
R6255 0
MUTE_CONTROL
R6258 100K
R6259 100K
R6256 0
L6250 FERR-220-OHM
AUD_GPIO_2
R6250 100K
SYNC_MASTER=J17_ULTIMATE
SYNC_DATE=05/16/2013
PAGE TITLE
AUDIO: HEADPHONE AMP
Apple Inc.
DRAWING NUMBER 051-9884
SIZE D
REVISION A.0.0
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LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +12 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

=PP12V_S0_AUDIO_SPKRAMP

C6300 10UF 10% 25V X5R 805
C6301 10UF 10% 25V X5R 805
C6302 0.1UF 10% 25V X5R 402
C6303 1UF 20% 25V X5R 603-1
C6304 0.1UF 10% 25V X5R 402
C6305 1UF 10% 25V X5R 603-1
CRITICAL C6306 220UF 20% 16V ELEC SM-CASE-C1-HF
CRITICAL C6307 220UF 20% 16V ELEC SM-CASE-C1-HF

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

L6300 FERR-1000-OHM 0402 — AUD_LO2_L_N → AUD_LAMP_RINC_P — C6308 1UF 10% 25V X5R 0402 → AUD_LAMP_RIN_P
L6301 FERR-1000-OHM 0402 — AUD_LO2_L_P → AUD_LAMP_RINC_N — C6309 1UF 10% 25V X5R 0402 → AUD_LAMP_RIN_N
L6302 FERR-1000-OHM 0402 — AUD_LO1_L_P → AUD_LAMP_LINC_P — C6310 4700PF 5% 50V NPO-C0G-CERM 0805 → AUD_LAMP_LIN_P
L6303 FERR-1000-OHM 0402 — AUD_LO1_L_N → AUD_LAMP_LINC_N — C6311 4700PF 5% 50V NPO-C0G-CERM 0805 → AUD_LAMP_LIN_N

=PP3V3_S0_AUDIO

CRITICAL U6300 SSM3302 LFCSP

20	INR+	
19	INR-	
22	SDNR*	ONLY WOOFERS ON UNDER WINDOWS: AUD_SPKRAMP_WIN_SHDN_L
16	MONO	AUD_LAMP_MONO
9	SDNL*	WOOFERS & TWEETERS ON UNDER MAC OS: AUD_SPKRAMP_MAC_SHDN_L
11	INL+	
12	INL-	
21	GAIN	AUD_LAMP_GAIN
8	VREG/AVDD	AUD_LAMP_AVDD (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V)
23	REGEN	
34,35,36,37	PVDD	
7,24,41	AGND	
31,32,33,38,39,40	PGND	
17	THERM	TP_AUD_LAMP_THERM NC
30	BOOTR+	C6313 0.22UF 20% 25V X5R 603
28,29	OUTR+	AUD_LAMP_OUTPR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
26,27	OUTR-	AUD_LAMP_OUTNR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
25	BOOTR-	C6314 0.22UF 20% 25V X5R 603
10	EDGE	AUD_LAMP_EDGE
1	BOOTL+	C6315 0.22UF 20% 25V X5R 603
2,3	OUTL+	AUD_LAMP_OUTPL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
4,5	OUTL-	AUD_LAMP_OUTNL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
6	BOOTL-	C6316 0.22UF 20% 25V X5R 603
18	NC	NC
13	NC	NC
14	TEST	
15		

C6317 2.2UF 20% 10V X5R-CERM 402

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

SIGNAL_MODEL=EMPTY CRITICAL L6305 110-OHM-3A DLY5ATN1111SQ2 (EMI_VSS-1)
AUD_LAMP_OUTPR → AUD_SPKR_LWFR_OUT_P — SIGNAL_MODEL=EMPTY CRITICAL C6323 1000PF 5% 25V CERM 0402
AUD_LAMP_OUTNR → AUD_SPKR_LWFR_OUT_N

SIGNAL_MODEL=EMPTY CRITICAL L6307 110-OHM-3A DLY5ATN1111SQ2 (EMI_VSS-1)
AUD_LAMP_OUTPL → AUD_SPKR_LTWT_OUT_P — SIGNAL_MODEL=EMPTY CRITICAL C6324 1000PF 5% 25V CERM 0402
AUD_LAMP_OUTNL → AUD_SPKR_LTWT_OUT_N

SIGNAL_MODEL=EMPTY — CRITICAL C6320 1000PF 5% 25V CERM 0402
SIGNAL_MODEL=EMPTY — CRITICAL C6322 1000PF 5% 25V CERM 0402 — SIGNAL_MODEL=EMPTY
SIGNAL_MODEL=EMPTY — CRITICAL C6319 1000PF 5% 25V CERM 0402
CRITICAL C6321 1000PF 5% 25V CERM 0402 — SIGNAL_MODEL=EMPTY

L6308 FERR-1000-OHM 0402 — AUD_CODEC_MICBIAS → AUD_SPKRAMP_MAC_SHDN_L
R6301 100K 5% 1/16W MF-LF 402 — NOSTUFF C6312 100PF 5% 50V CERM 402

R6308 0 5% 1/16W MF-LF 402 — AUD_GPIO_3 → AUD_SPKRAMP_WIN_SHDN_L
R6309 100K 5% 1/16W MF-LF 402 — NOSTUFF C6318 100PF 5% 50V CERM 402

EDGE RATE CONTROL

	R6304	R6305
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6306	R6307
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF

AUD_LAMP_AVDD
R6304 0 5% 1/16W MF-LF 402 — AUD_LAMP_EDGE
NOSTUFF R6305 0 5% 1/16W MF-LF 402
R6303 0 5% 1/16W MF-LF 402 — AUD_LAMP_MONO
NOSTUFF R6306 0 5% 1/16W MF-LF 402 — AUD_LAMP_GAIN
R6307 47K 5% 1/16W MF-LF 402

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013
PAGE TITLE: AUDIO: LEFT SPKR AMP

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RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +12 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

ONLY WOOFERS ON UNDER WINDOWS

WOOFERS & TWEETERS ON UNDER MAC OS

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

EDGE RATE CONTROL	R6404	R6405
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6406	R6407
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF

SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE
AUDIO: RIGHT SPKR AMP

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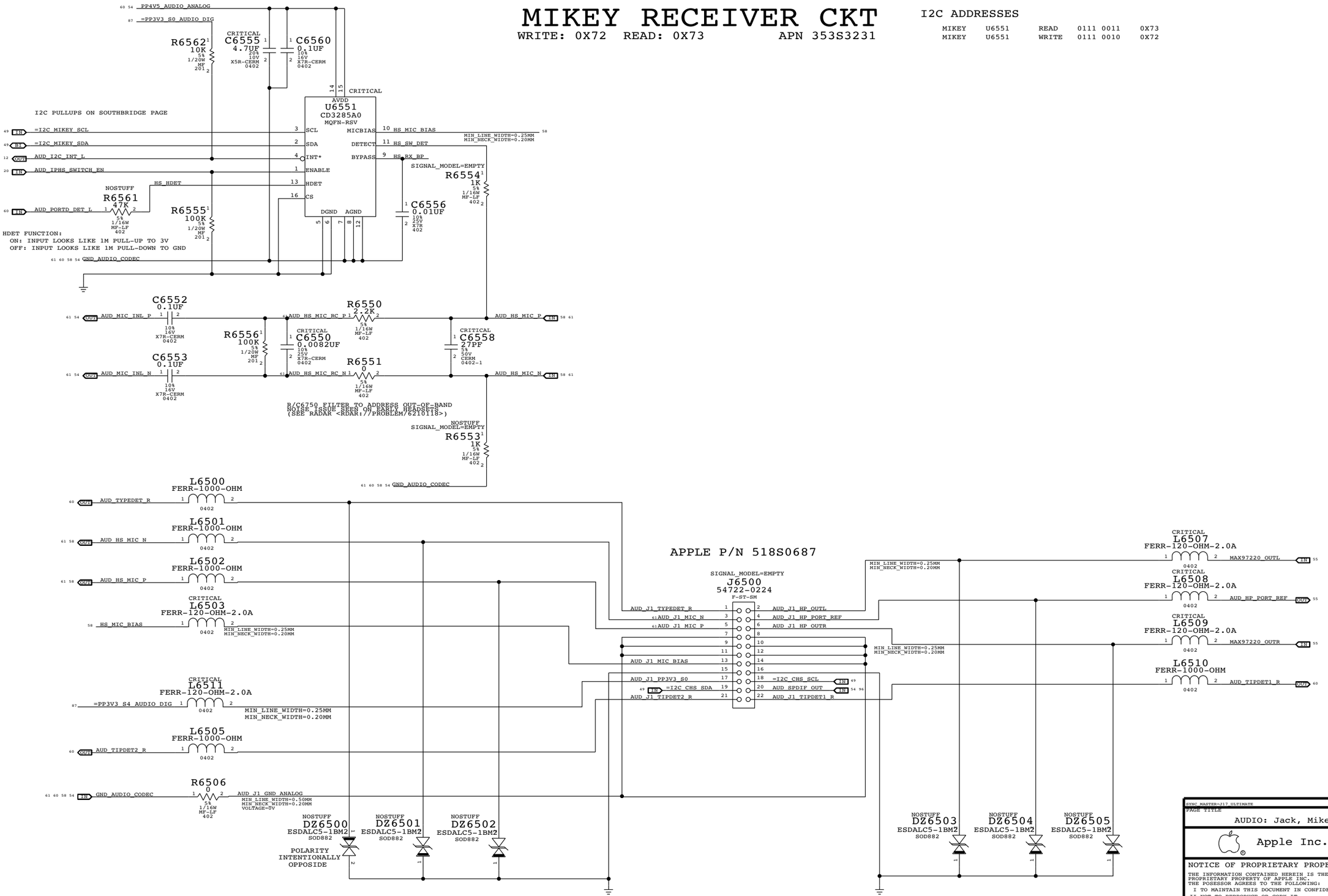
MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S3231

I2C ADDRESSES

MIKEY	U6551	READ	0111 0011	0X73
MIKEY	U6551	WRITE	0111 0010	0X72



SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2011

PAGE TITLE

AUDIO: Jack, Mikey, CHS Switch

Apple Inc.

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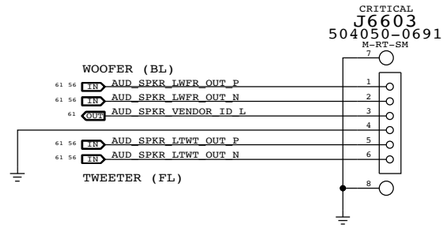
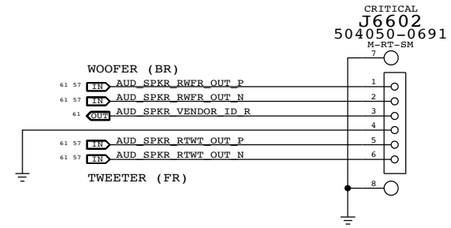
SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862





SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE

Audio: Spkr/Mic Conn.

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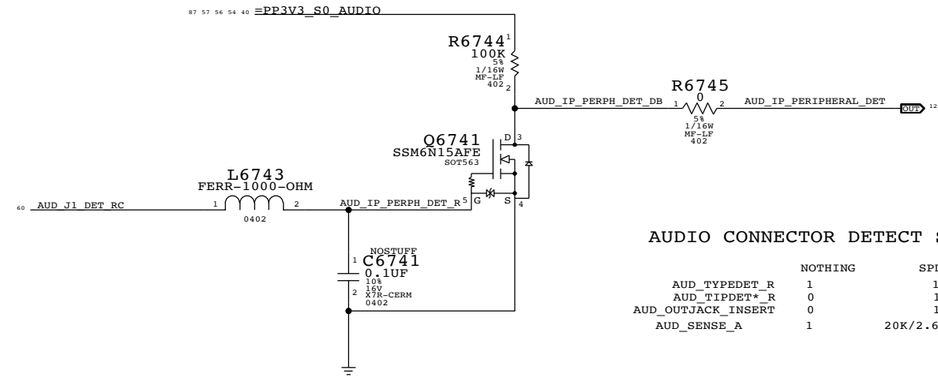
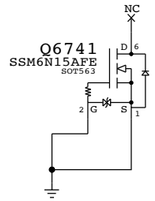
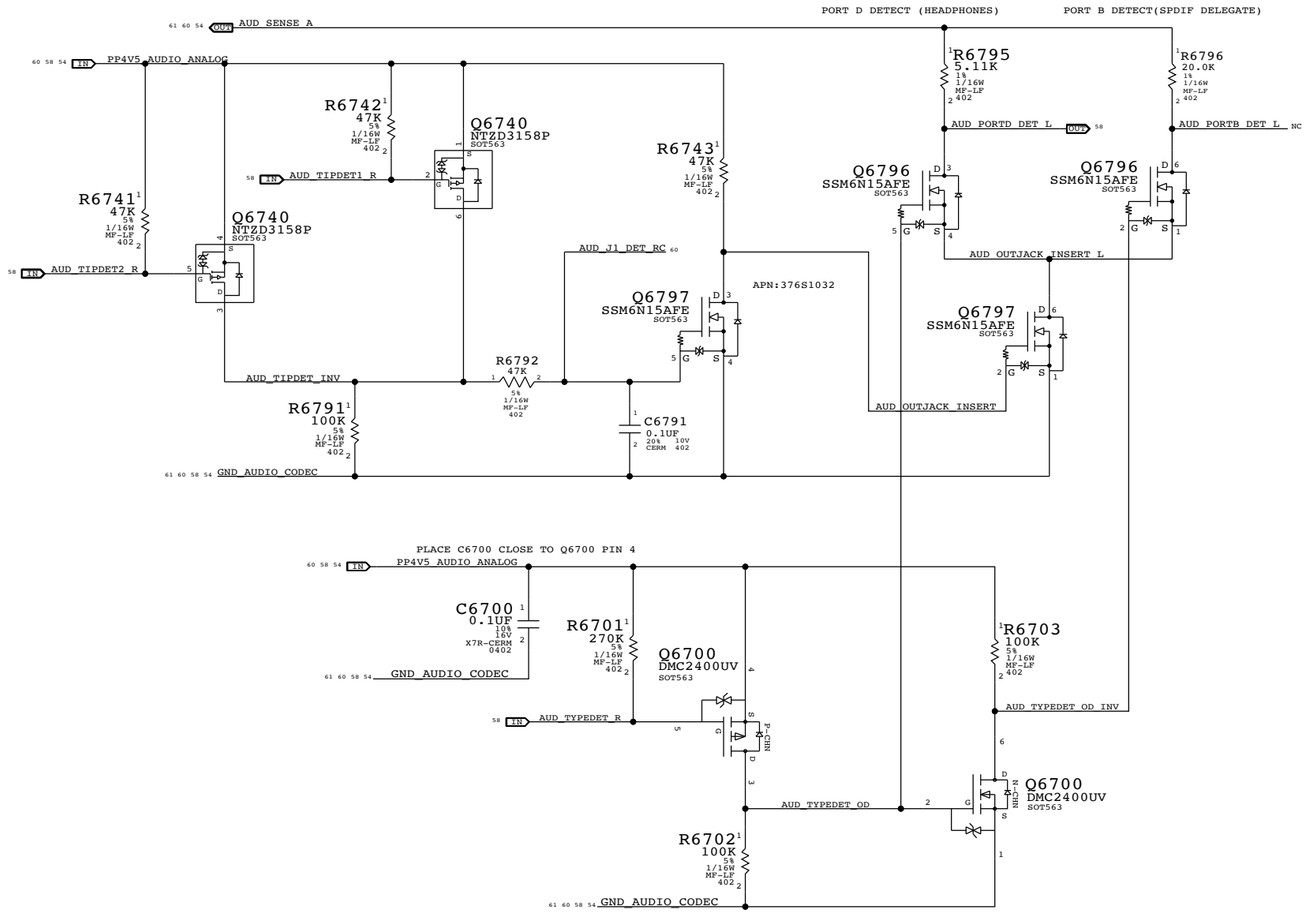
IPHS HS Detect Debounce CKT



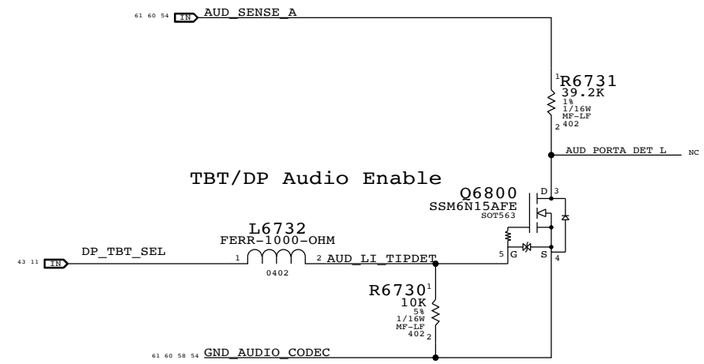
AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_TYPEDET_R	1	1	0
AUD_TIPDET*_R	0	1	1
AUD_OUTJACK_INSERT	0	1	1
AUD_SENSE_A	1	20K/2.67K RDIV	5.11K/2.67K RDIV





Target Display Mode Detect



SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE
AUDIO: Detects/Grounding

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	Lynx POINT GPIO 16	Lynx POINT GPIO 5 (RCVR INT) Lynx POINT GPIO 3 (PERIPH DET)

OTHER DETECT

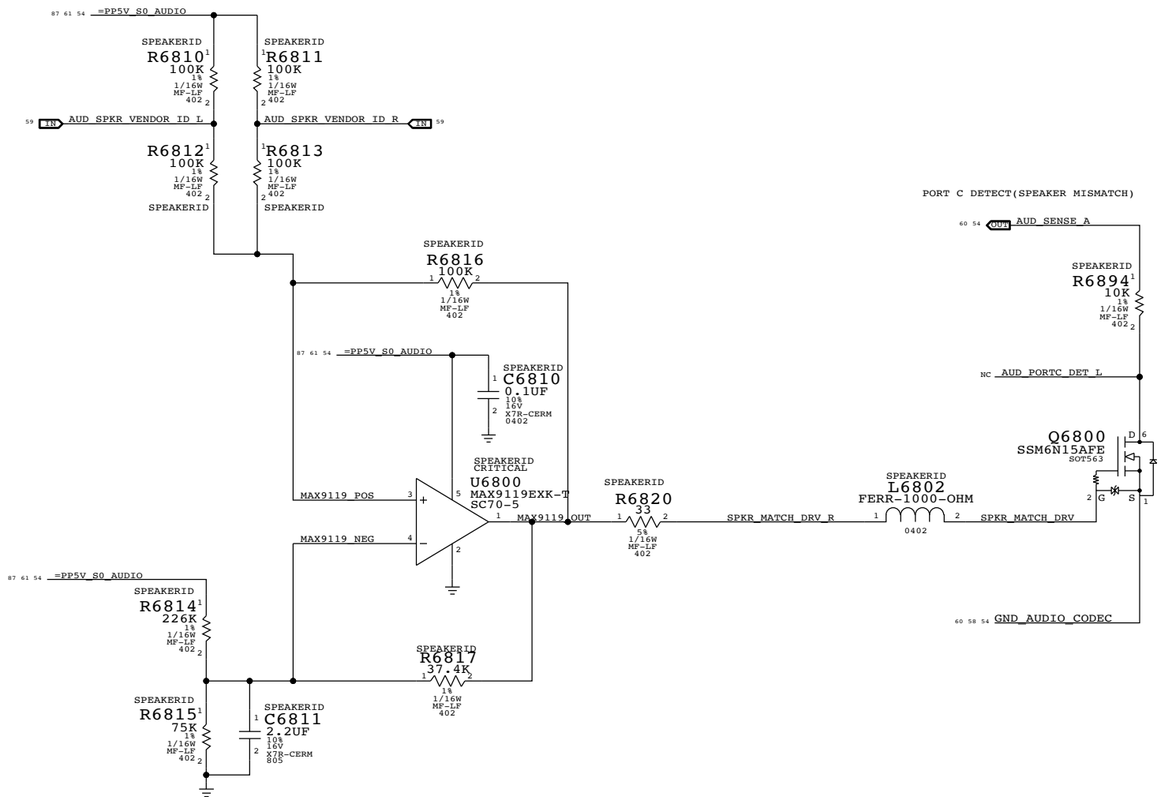
FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

CIRCUIT THEORY OF OPERATION AVAILABLE IN <RDAR://PROBLEM/9776522>



PORT C DETECT(SPEAKER MISMATCH)

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	54 55 56
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	54 55 56
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	55
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	55
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	54 55 57
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	54 55 57
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	55
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	55
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	54 56
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	54 56
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	54 57
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	54 57
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	57
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	57
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	57
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	57
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	57
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	57
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	57
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	57
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	56
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	56
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	56
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	56
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	56
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	56
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	56
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	56
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_P	55
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_N	55
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_P	55
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_N	55
I2S SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	57 59
I2S SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	57 59
I2S SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	57 59
I2S SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	57 59
I2S SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	56 59
I2S SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	56 59
I2S SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	56 59
I2S SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	56 59
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	54 58
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	54 58
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_P	58
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_N	58
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P	58
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N	58
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_P	58
I2S AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_N	58

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE: AUDIO: Speaker ID

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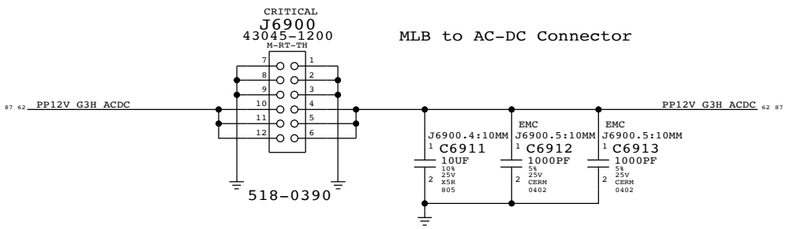
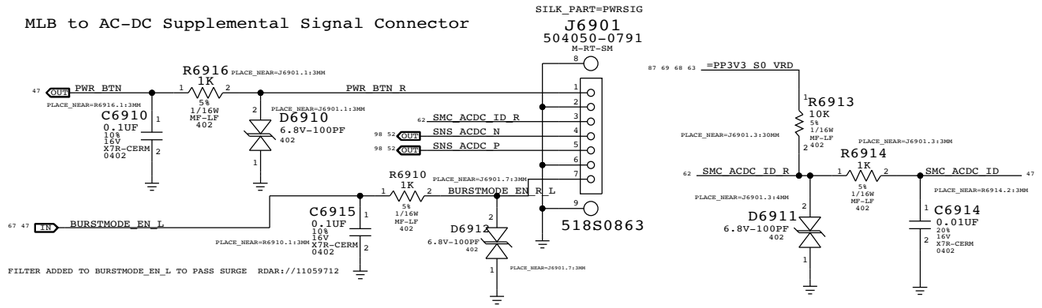
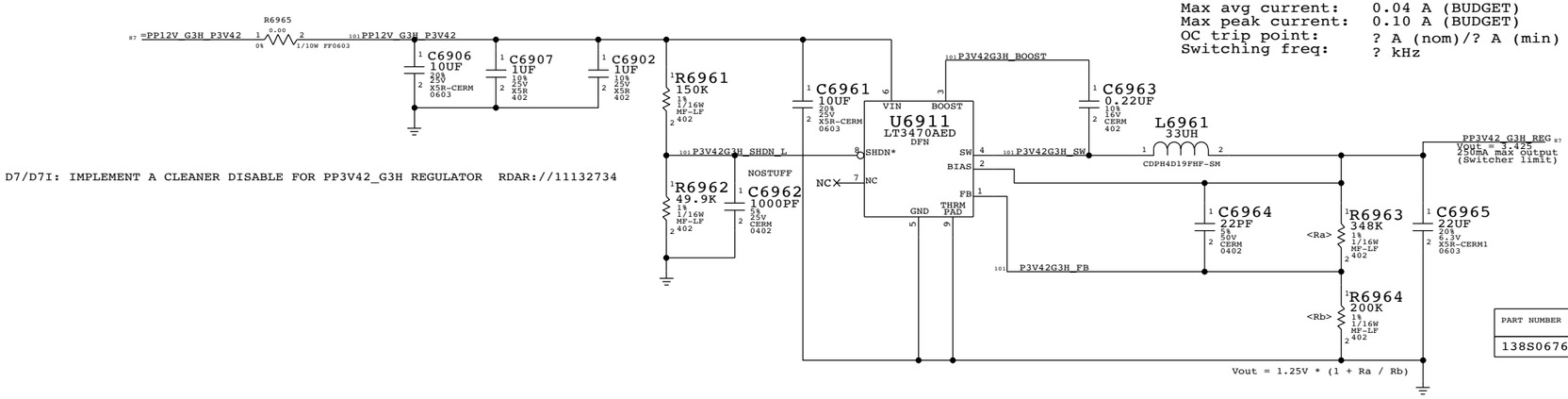




D8:CONTROLLER CHANGE FOR 3.42V SMC SUPPLY RDAR://11003901

3.425V "G3Hot" Regulator

Max avg current: 0.04 A (BUDGET)
Max peak current: 0.10 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz



D7/D7I: IMPLEMENT A CLEANER DISABLE FOR PP3V42_G3H REGULATOR RDAR://11132734

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0676	138S0691		C6965	

SYNC MASTER=J17_ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE
Power Connectors / VReg G3Hot

Apple Inc.

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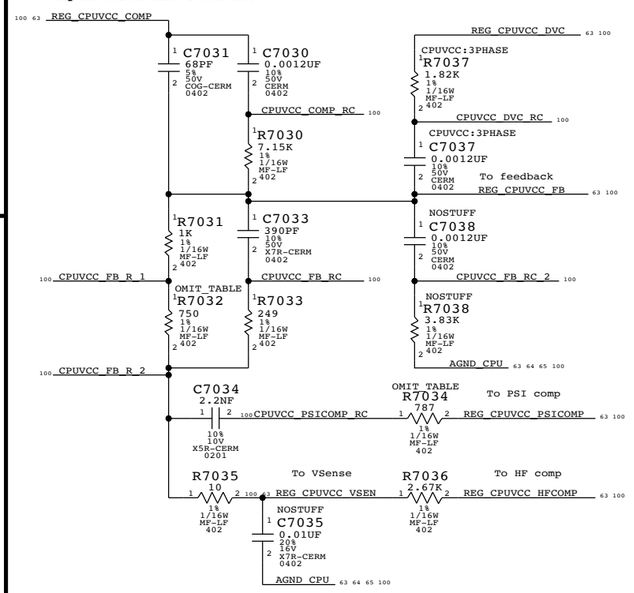
CPU VCC S0 Regulator

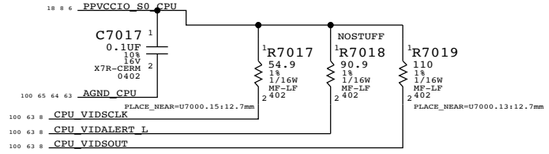
OC trip point: 114 A

Switching freq: 403 kHz = 5 E10 / R7003

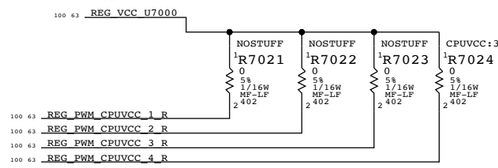
Compensation and feedback

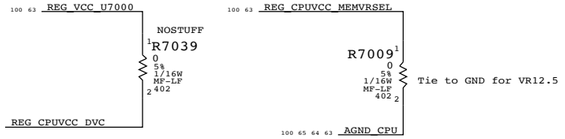


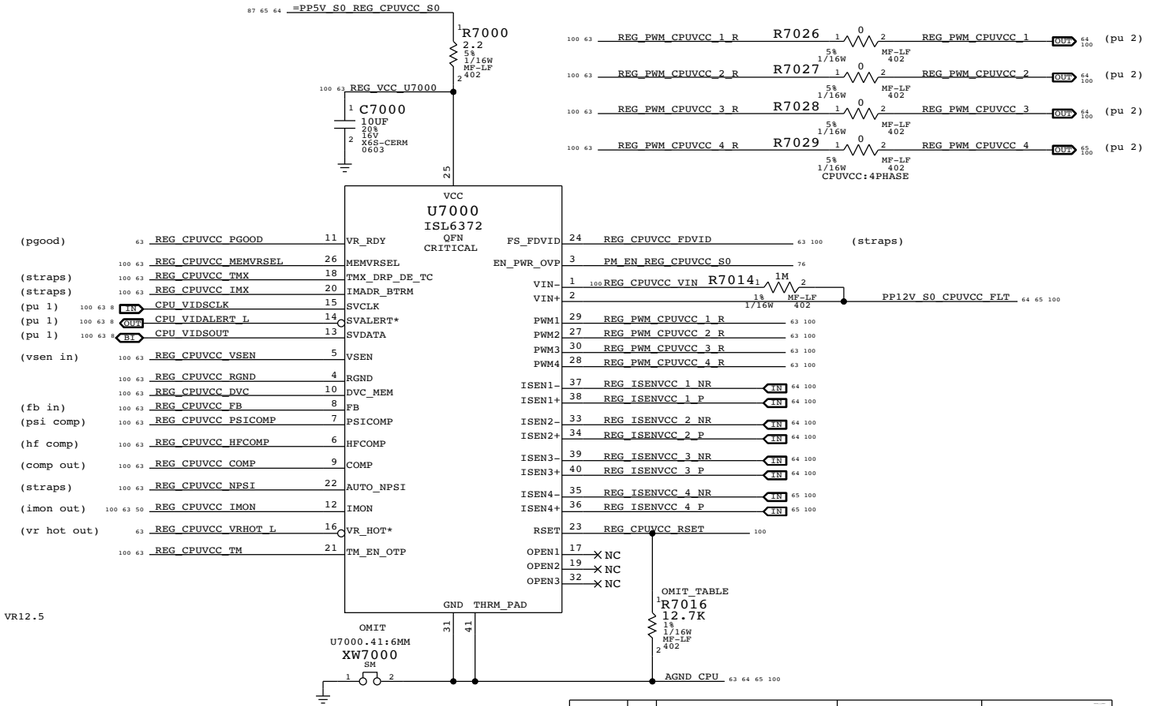
Pull-ups 1



Pull-ups 2

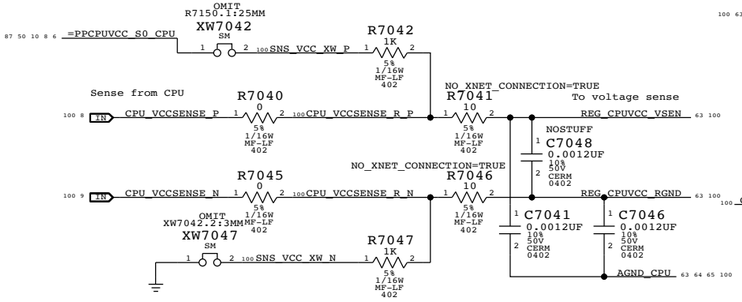




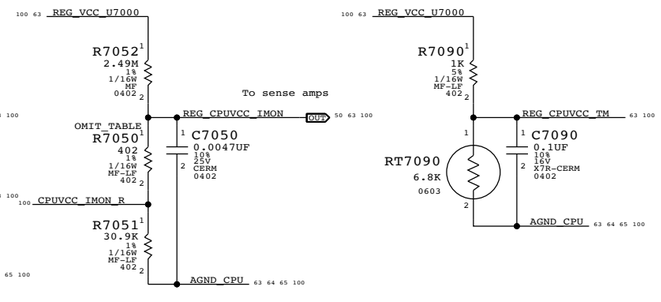


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0324	1	RES,12.7K,402	R7016	CPUVCC:3PHASE
114S0316	1	RES,10.2K,402	R7016	CPUVCC:4PHASE

Voltage sense input

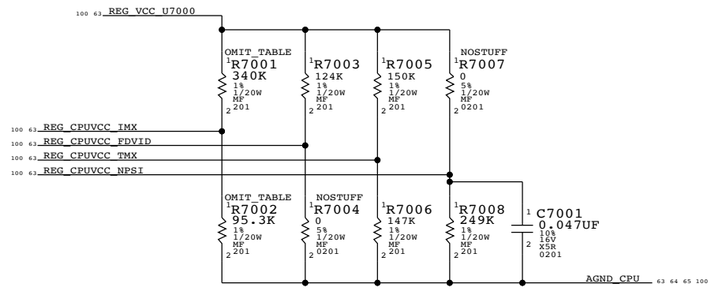


IMON output

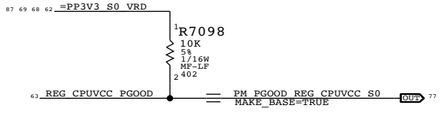


Temp measurement

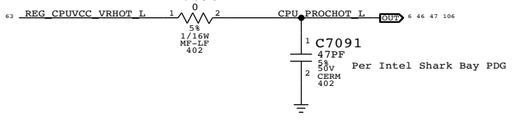
Straps



Power goods



VRHot to ProcHot



J16: 3PHASE
J17: 4PHASE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S0311	1	RES,340K,201	R7001	CPUVCC:3PHASE
118S0116	1	RES,158K,201	R7001	CPUVCC:4PHASE
118S0575	1	RES,95.3K,201	R7002	CPUVCC:3PHASE
118S0380	1	RES,44.2K,201	R7002	CPUVCC:4PHASE
114S0206	1	RES,750 OHM,402	R7032	CPUVCC:3PHASE
114S0210	1	RES,825 OHM,402	R7032	CPUVCC:4PHASE
114S0208	1	RES,787 OHM,402	R7034	CPUVCC:3PHASE
114S0189	1	RES,499 OHM,402	R7034	CPUVCC:4PHASE
114S0179	1	RES,402 OHM,402	R7050	CPUVCC:3PHASE
114S0184	1	RES,453 OHM,402	R7050	CPUVCC:4PHASE

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE: VReg CPU VCC Cntl

Apple Inc.

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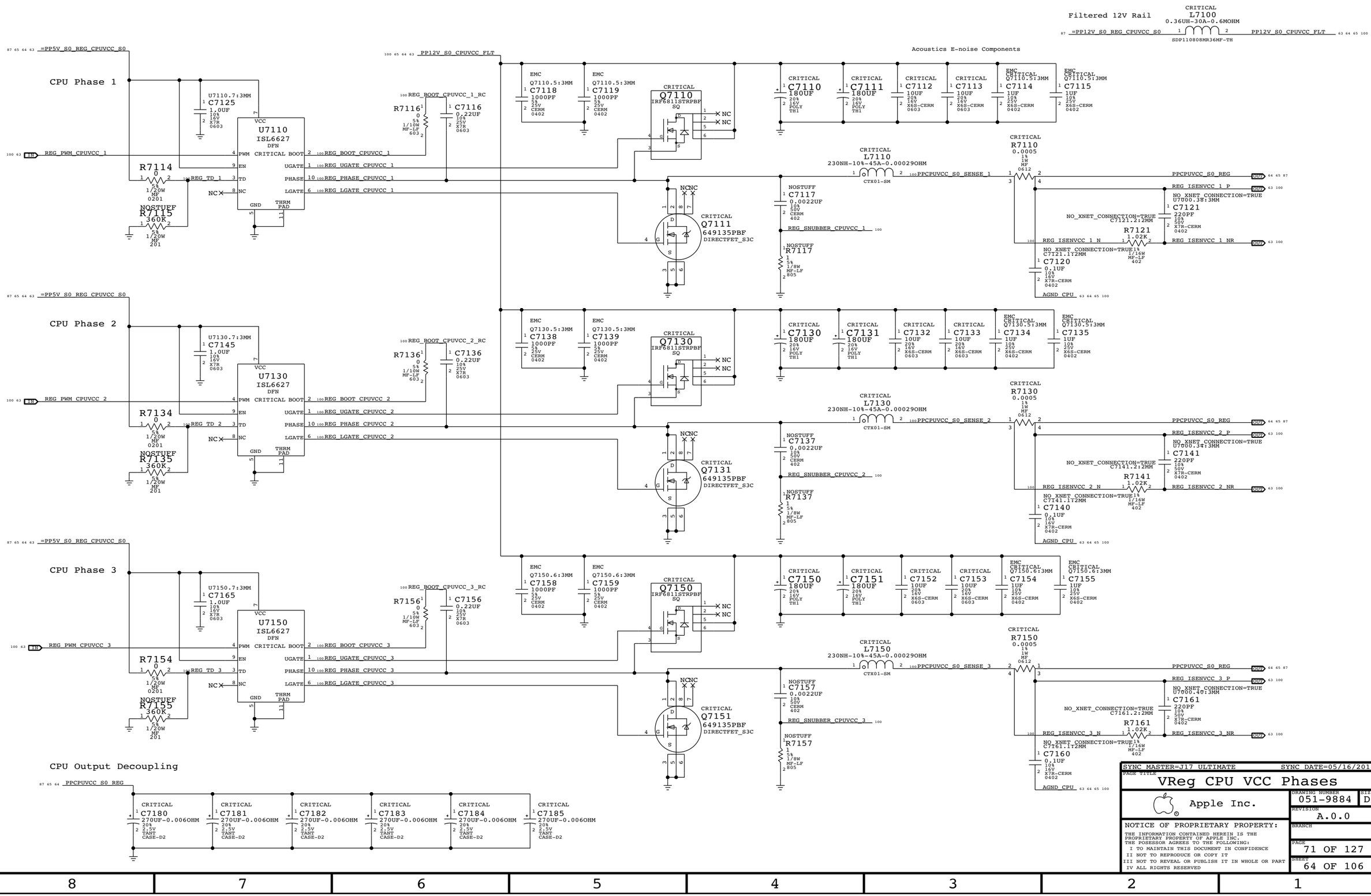
Filtered 12V Rail
CRITICAL L7100 0.36UH-30A-0.6MOHM
=PP12V_S0_REG_CPUVCC_S0
PP12V_S0_CPUVCC_FLT
SDP110808MR36MF-TH
Acoustics E-noise Components
CPU Phase 1
CPU Phase 2
CPU Phase 3
CPU Output Decoupling
U7110 ISL6627 DFN
U7130 ISL6627 DFN
U7150 ISL6627 DFN
REG_PWM_CPUVCC_1
REG_PWM_CPUVCC_2
REG_PWM_CPUVCC_3
REG_BOOT_CPUVCC_1_RC
REG_BOOT_CPUVCC_2_RC
REG_BOOT_CPUVCC_3_RC
REG_TD_1
REG_TD_2
REG_TD_3
REG_BOOT_CPUVCC_1
REG_UGATE_CPUVCC_1
REG_PHASE_CPUVCC_1
REG_LGATE_CPUVCC_1
REG_BOOT_CPUVCC_2
REG_UGATE_CPUVCC_2
REG_PHASE_CPUVCC_2
REG_LGATE_CPUVCC_2
REG_BOOT_CPUVCC_3
REG_UGATE_CPUVCC_3
REG_PHASE_CPUVCC_3
REG_LGATE_CPUVCC_3
Q7110 IRF6811STRPBF SQ
Q7111 649135PBF DIRECTFET_S3C
Q7130 IRF6811STRPBF SQ
Q7131 649135PBF DIRECTFET_S3C
Q7150 IRF6811STRPBF SQ
Q7151 649135PBF DIRECTFET_S3C
L7110 230NH-10%-45A-0.00029OHM CTX01-SM
L7130 230NH-10%-45A-0.00029OHM CTX01-SM
L7150 230NH-10%-45A-0.00029OHM CTX01-SM
PPCPUVCC_S0_SENSE_1
PPCPUVCC_S0_SENSE_2
PPCPUVCC_S0_SENSE_3
PPCPUVCC_S0_REG
REG_SNUBBER_CPUVCC_1
REG_SNUBBER_CPUVCC_2
REG_SNUBBER_CPUVCC_3
REG_ISENVCC_1_P
REG_ISENVCC_1_N
REG_ISENVCC_1_NR
REG_ISENVCC_2_P
REG_ISENVCC_2_N
REG_ISENVCC_2_NR
REG_ISENVCC_3_P
REG_ISENVCC_3_N
REG_ISENVCC_3_NR
NO_XNET_CONNECTION=TRUE
AGND_CPU
SYNC_MASTER=J17_ULTIMATE
SYNC_DATE=05/16/2013
PAGE TITLE
VReg CPU VCC Phases
Apple Inc.
DRAWING NUMBER 051-9884
SIZE D
REVISION A.0.0
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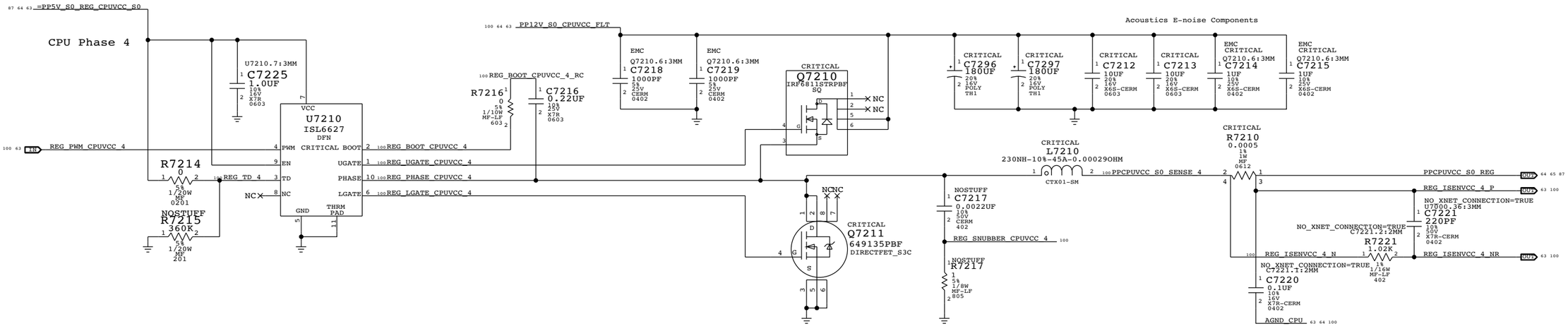

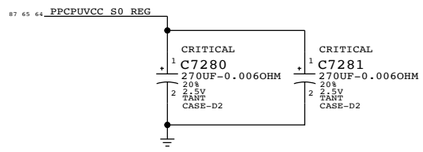

SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE
VReg CPU VCC Phase 4

Apple Inc.

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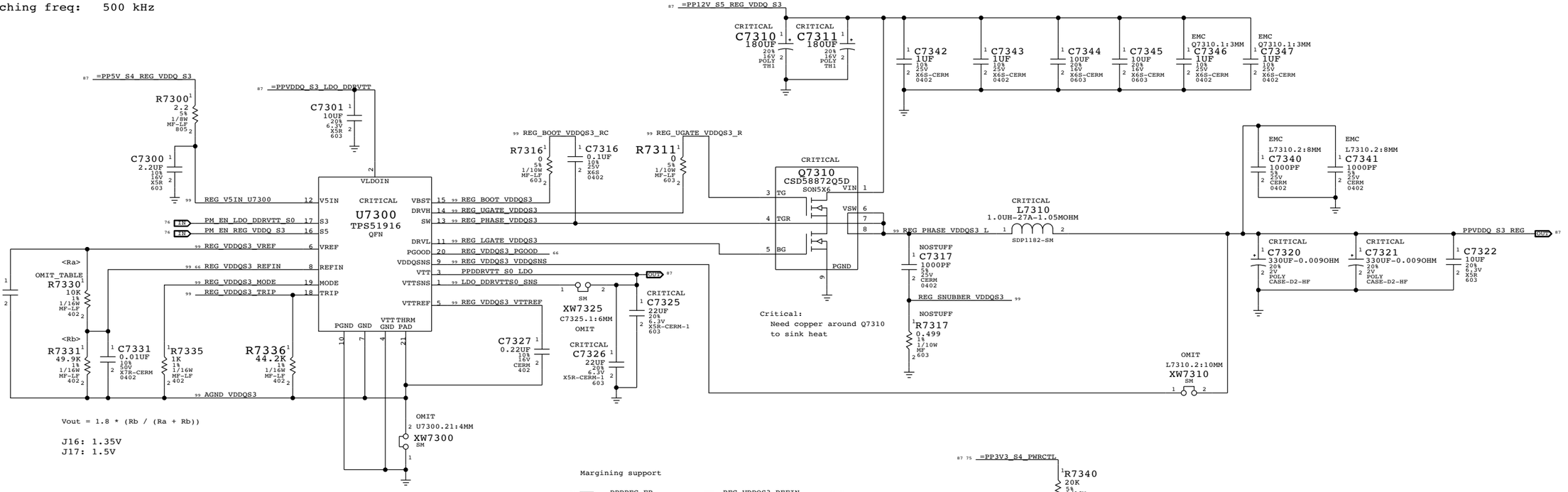
VDDQ (1.5V / 1.35V) S3 Regulator

OC trip point: 30.4 A VDDQ = $\frac{R7336}{8\ E5\ *\ Rds(Q7310)} + \frac{0.65625}{L7310\ *\ f(switch)}$

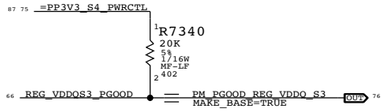
3 A VTT (FIXED)
10 mA VTTREF (FIXED)

Switching freq: 500 kHz



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0335	1	RES,16.5K,402	R7330	VDDQ:P1V35
114S0315	1	RES,10K,402	R7330	VDDQ:P1V5

Margining support



SYNC MASTER=J17_ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE: VReg VDDQ S3

Apple Inc.

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3.3V S5 Regulator

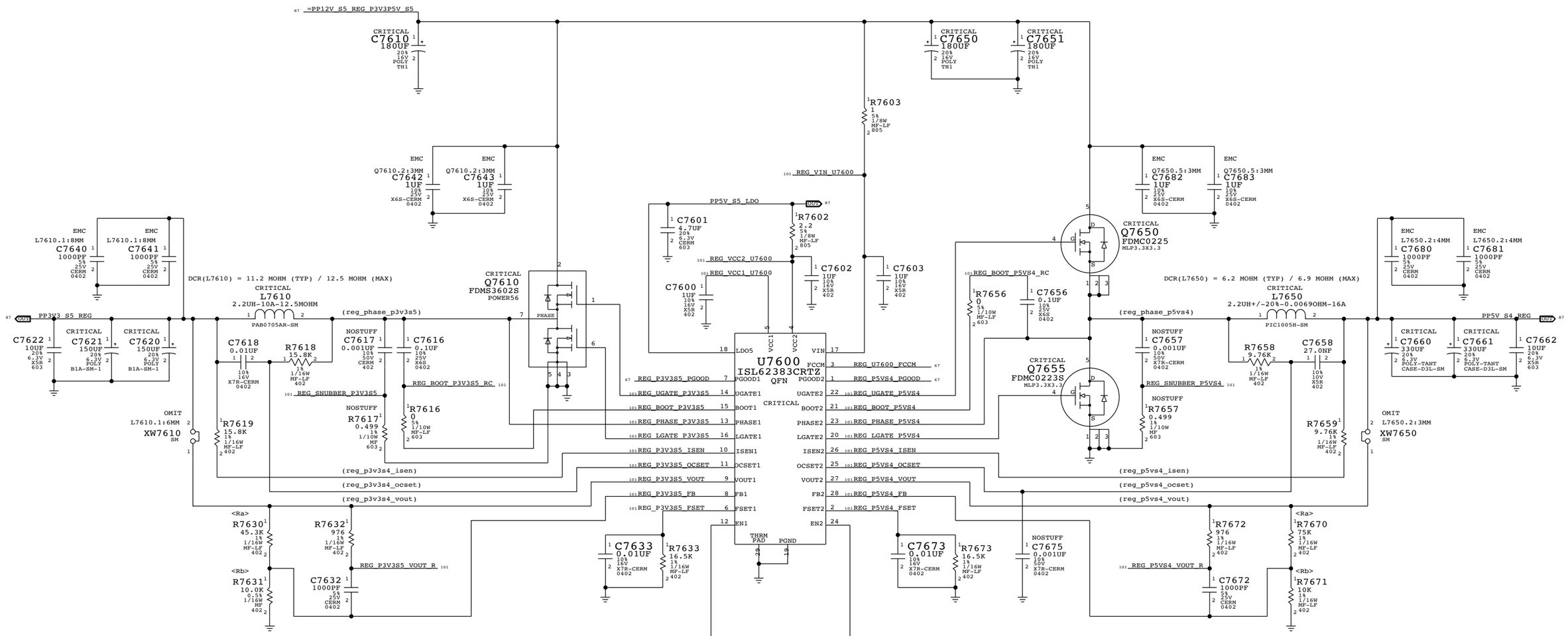
OC trip point: 12.5 A = $\frac{\text{R7618 * 10 E-6}}{\text{DCR(L7610)}}$

Switching freq: 356 kHz = $\frac{1}{\text{170 E-12 * R7633}}$

5V S4 Regulator

OC trip point: 14.1 A = $\frac{\text{R7658 * 10 E-6}}{\text{DCR(L7650)}}$

Switching freq: 356 kHz = $\frac{1}{\text{170 E-12 * R7673}}$



SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE: VReg 3.3V S5/5V S4

Apple Inc.

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GPU VDDQ SUPPLY

VOUT = 1.5V / 1.35V

F = 500 KHZ

GPIO_16 VID 1	VID 0	GPU VDDQ
0	0	1.5 V
1	0	1.35 V

Vout = 0.5 * (1 + Ra / Rb)

Note:
Regulator requires a minimum load to prevent noise in the audio frequencies

GPU/PCH/TBT 1V05 SUPPLY

VOUT = 1.05V

F = 500 KHZ

Vout = 0.5 * (1 + Ra / Rb)

SYNC MASTER=J17 ULTIMATE	SYNC DATE=05/16/2013
PAGE TITLE	GPU VDDQ AND 1V05 GPU/PCH/TBT VREGS
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GPU CORE REG 1.1V/???A O/P= PPGPUCORE_S0_REG

=PP5V_S0_VRD → R7818 2.2 5% 1/8W MF-LF 805 (MAX_NECK_LENGTH=3MM, MIN_NECK_WIDTH=0.2MM, MIN_LINE_WIDTH=0.6MM, VOLTAGE=5V) → PP5V_S0_GPU_VCORE_VCC

GPU VCORE
VOUT = VCORE
PEAK = ???A
AVG = ???A

VSNS / VR_GPU_VSEN

VSNS_GPU_VDD (IN) → SM XW7820 OMIT (VOLTAGE=1.1V, NET_PHYSICAL_TYPE=SNS_DIFF_PAIR, SIGNAL_MODEL=EMPTY) → VR_GPU_VSEN

VSNS_GPU_VSS (IN) → XW7830 SM OMIT (VOLTAGE=0V, NET_PHYSICAL_TYPE=SNS_DIFF_PAIR) → VR_GPU_RGND

1.25 mOhm loadline

NOSTUFF C7801 0.0022UF 10% 50V CERM 402 (VR_GPU_VSEN – VR_GPU_RGND)

C7802 0.0022UF 10% 50V CERM 402 (VR_GPU_RGND – AGND_GPU)

C7803 0.0022UF 10% 50V CERM 402 (VR_GPU_VSEN – AGND_GPU)

VR_GPU_FB_R / VR_GPU_COMP_R

C7804 47PF 5% 50V CERM 402 (VR_GPU_FB_R – VR_GPU_COMP_R)

R7801 8.06K 1% 1/16W MF-LF 402 (VR_GPU_COMP_R – VR_GPU_COMP_RC)

C7805 0.0047UF 10% 25V CERM 0402 (VR_GPU_COMP_RC – AGND_GPU)

R7879 0 5% 1/16W MF-LF 402 (VR_GPU_COMP_RC – VR_GPU_COMP)

R7802 1K 1% 1/16W MF-LF 402 (VR_GPU_COMP – VR_VDF_R1)

R7803 287 1% 1/16W MF-LF 402 (VR_VDF_R1 – AGND_GPU)

NOSTUFF R7846 1M 5% 1/16W MF-LF 402 (VR_GPU_COMP – AGND_GPU)

R7804 0 5% 1/16W MF-LF 402 (VR_GPU_COMP – VR_GPU_FB)

C7807 1UF 10% 10V X6S-CERM 0402 (LOCAL 5V – AGND_GPU)

C7806 0.001UF 10% 50V X7R-CERM 0402 (VR_VDF_R2 – AGND_GPU)

R7849 47.5 1% 1/16W MF-LF 402 (VR_VDF_R2 – VR_GPU_VDIFF)

PP5V_S0_GPU_VCORE_VCC

VR_HOT goes HIGH when VTM/VCC < 28% and LOW when VTM/VCC > 33%.

R7800 1.02K 1% 1/16W MF-LF 402 (PP5V_S0_GPU_VCORE_VCC – VR_GPU_VDIFF)

NOSTUFF R7805 20.0K 1% 1/16W MF-LF 402 (PP5V_S0_GPU_VCORE_VCC – VR_GPU_VDIFF)

NOSTUFF R7898 0 5% 1/16W MF-LF 402 (PP5V_S0_GPU_VCORE_VCC – VR_GPU_VDIFF)

R7877 100K 1% 1/16W MF-LF 402 (PP5V_S0_GPU_VCORE_VCC – VR_GPU_VDIFF)

LAYOUT: PLACE RT7801 NEAR HOT SPOT

RT7801 6.8K 0603

C7880 0.1UF 10% 10V CERM 402

NOSTUFF R7806 0 5% 1/16W MF-LF 402

NOSTUFF R7807 21K 1% 1/16W MF-LF 402

R7808 75K 1% 1/16W MF-LF 402

NOSTUFF R7809 100K 1% 1/16W MF-LF 402

C7810 0.0033UF 10% 50V X7R-CERM 0402

R7810 2.15K 1% 1/16W MF-LF 402

=PP5V_S0_VRD → R7811 10K 0.1% 1/16W MF-LF 0402

PP5V_S0_GPU_VCORE_VCC

=PP3V3_S0_VRD

=PP3V3_S0_GPU → R7812 2.0K 5% 1/16W MF-LF 402

R7899 10K 0.1% 1/16W MF-LF 0402

PM_PGOOD_REG_GPUCORE_S0 (OUT)

GPU_PSI_L (IN)

VR_GPU_IMON (OUT)

R7814 49.9K 1% 1/16W MF-LF 402

R7815 49.9K 1% 1/16W MF-LF 402

R7845 0 5% 1/16W MF-LF 402 (VR_GPU_IMON_R – VR_GPU_IMON)

R7817 10K 1% 1/16W MF-LF 402 (VR_GPU_IOUT_PD – VR_GPU_IMON_R)

C7812 0.022UF 10% 16V X5R-X7R-CERM 0402 (VR_GPU_IMON_R – AGND_GPU)

R7816 0 5% 1/16W MF-LF 402 (VR_GPU_IMON_R – AGND_GPU)

DEFAULT: 0.9000V STEP: 12.5MV

=PP3V3_S0_GPU

NOSTUFF R7878 1K 1% 1/16W MF-LF 402

NOSTUFF R7870 1K 1% 1/16W MF-LF 402

NOSTUFF R7871 1K 1% 1/16W MF-LF 402

NOSTUFF R7872 1K 1% 1/16W MF-LF 402

NOSTUFF R7873 1K 1% 1/16W MF-LF 402

NOSTUFF R7874 1K 1% 1/16W MF-LF 402

NOSTUFF R7875 1K 1% 1/16W MF-LF 402

NOSTUFF R7876 1K 1% 1/16W MF-LF 402

REG_GPUCORE_VID7
REG_GPUCORE_VID6
REG_GPUCORE_VID5
REG_GPUCORE_VID4
REG_GPUCORE_VID3
REG_GPUCORE_VID2
REG_GPUCORE_VID1
REG_GPUCORE_VID0

NOSTUFF R7895 1K 1% 1/16W MF-LF 402

NOSTUFF R7896 1K 1% 1/16W MF-LF 402

NOSTUFF R7897 1K 1% 1/16W MF-LF 402

NOSTUFF R7880 1K 1% 1/16W MF-LF 402

NOSTUFF R7881 1K 1% 1/16W MF-LF 402

NOSTUFF R7882 1K 1% 1/16W MF-LF 402

NOSTUFF R7885 1K 1% 1/16W MF-LF 402

NOSTUFF R7883 1K 1% 1/16W MF-LF 402

NEED TO FIGURE OUT SEQUENCING FOR ENABLE

U7800 ISL6334D QFN (VCC CRITICAL SYM_VER_2)

13	COMP	VR_GPU_COMP
14	FB	VR_GPU_FB
15	VDIFF	VR_GPU_VDIFF
17	VSEN	
16	RGND	
18	TCOMP	VR_GPU_TCOMP
9	OFS	VR_GPU_OFS
34	FS	VR_GPU_FS
35	SS	VR_GPU_SS
11	DAC	VR_GPU_DAC
12	REF	VR_GPU_REF
39	TM	VR_GPU_TM
33	EN_VTT	VR_GPU_EN_VTT
36	VR_RDY	
7	VID0	
6	VID1	
5	VID2	
4	VID3	
3	VID4	
2	VID5	
1	VID6	
40	VID7	
8	PSI*	
10	IMON	VR_GPU_IMON_R
37	VR_FAN	VR_GPU_FAN
38	VR_HOT	VR_GPU_VRDHOT
32	EN_PWR	PM_EN_REG_GPUCORE_S0_R
26	PWM1	VR_GPU_PWM1_R
28	ISEN1+	VR_GPU_ISNS1_R_P
27	ISEN1-	VR_GPU_ISNS1_R_N
20	PWM2	VR_GPU_PWM2_R
22	ISEN2+	VR_GPU_ISNS2_R_P
21	ISEN2-	VR_GPU_ISNS2_R_N
31	PWM3	VR_GPU_PWM3_R
29	ISEN3+	VR_GPU_ISNS3_R_P
30	ISEN3-	VR_GPU_ISNS3_R_N
25	PWM4	VR_GPU_PWM4_R
23	ISEN4+	VR_GPU_ISNS4_R_P
24	ISEN4-	VR_GPU_ISNS4_R_N
19	GND	AGND_GPU

THRM PAD 41

OMIT XW7801 SM (AGND_GPU – AGND_GPU) MAX_NECK_LENGTH=3MM, MIN_NECK_WIDTH=0.3MM, MIN_LINE_WIDTH=0.6MM, VOLTAGE=0V

R7884 0 5% 1/16W MF-LF 402 (PM_EN_REG_GPUCORE_S0 – PM_EN_REG_GPUCORE_S0_R)

NOSTUFF C7809 0.01UF 10% 16V X7R-CERM 0402

NOSTUFF R7847 0 5% 1/16W MF-LF 402

NOSTUFF R7848 0 5% 1/16W MF-LF 402

NOSTUFF R7844 0 5% 1/16W MF-LF 402

NOSTUFF R7855 0 5% 1/16W MF-LF 402

Phase 1

R7834 0 5% 1/16W MF-LF 402 → REG_PWM_GPUCORE_1 (OUT)

R7831 178 1% 1/16W MF-LF 402 (VR_GPU_ISNS1_RR_2)

R7832 0 5% 1/16W MF-LF 402

NOSTUFF C7830 15PF 1% 50V COG 402

C7831 150PF 5% 50V CERM 402

C7832 0.1UF 10% 16V X7R-CERM 0402

C7833 220PF 5% 25V COG-CERM 0402

R7833 1.02K 1% 1/16W MF-LF 402

DIFFERENTIAL_PAIR=REG_ISEN_GCORE_1
REG_ISEN_GCORE_1_P (IN)
REG_ISEN_GCORE_1_N (IN)
DIFFERENTIAL_PAIR=REG_ISEN_GCORE_1

Phase 2

R7840 0 5% 1/16W MF-LF 402 → REG_PWM_GPUCORE_2 (OUT)

R7841 178 1% 1/16W MF-LF 402 (VR_GPU_ISNS2_RR_2)

R7842 0 5% 1/16W MF-LF 402

NOSTUFF C7840 15PF 1% 50V COG 402

C7841 150PF 5% 50V CERM 402

C7842 0.1UF 10% 16V X7R-CERM 0402

C7843 220PF 5% 25V COG-CERM 0402

R7843 1.02K 1% 1/16W MF-LF 402

DIFFERENTIAL_PAIR=REG_ISEN_GCORE_2
REG_ISEN_GCORE_2_P (IN)
REG_ISEN_GCORE_2_N (IN)
DIFFERENTIAL_PAIR=REG_ISEN_GCORE_2

Phase 3

R7850 0 5% 1/16W MF-LF 402 → REG_PWM_GPUCORE_3 (OUT)

R7851 178 1% 1/16W MF-LF 402 (VR_GPU_ISNS3_RR_2)

R7852 0 5% 1/16W MF-LF 402

NOSTUFF C7850 15PF 1% 50V COG 402

C7851 150PF 5% 50V CERM 402

C7852 0.1UF 10% 16V X7R-CERM 0402

C7853 220PF 5% 25V COG-CERM 0402

R7853 1.02K 1% 1/16W MF-LF 402

DIFFERENTIAL_PAIR=REG_ISEN_GCORE_3
REG_ISEN_GCORE_3_P (IN)
REG_ISEN_GCORE_3_N (IN)
DIFFERENTIAL_PAIR=REG_ISEN_GCORE_3

Phase 4

R7838 0 5% 1/16W MF-LF 402 → REG_PWM_GPUCORE_4 (OUT)

R7839 178 1% 1/16W MF-LF 402 (VR_GPU_ISNS4_RR_2)

R7820 0 5% 1/16W MF-LF 402

NOSTUFF C7860 15PF 1% 50V COG 402

C7861 150PF 5% 50V CERM 402

C7862 0.1UF 10% 16V X7R-CERM 0402

C7863 220PF 5% 25V COG-CERM 0402

R7821 1.02K 1% 1/16W MF-LF 402

DIFFERENTIAL_PAIR=REG_ISEN_GCORE_4
REG_ISEN_GCORE_4_P (IN)
REG_ISEN_GCORE_4_N (IN)
DIFFERENTIAL_PAIR=REG_ISEN_GCORE_4

AGND_GPU

=PP12V_S0_REG_GPUCORE → PP12V_S0_GPUCORE_FLT

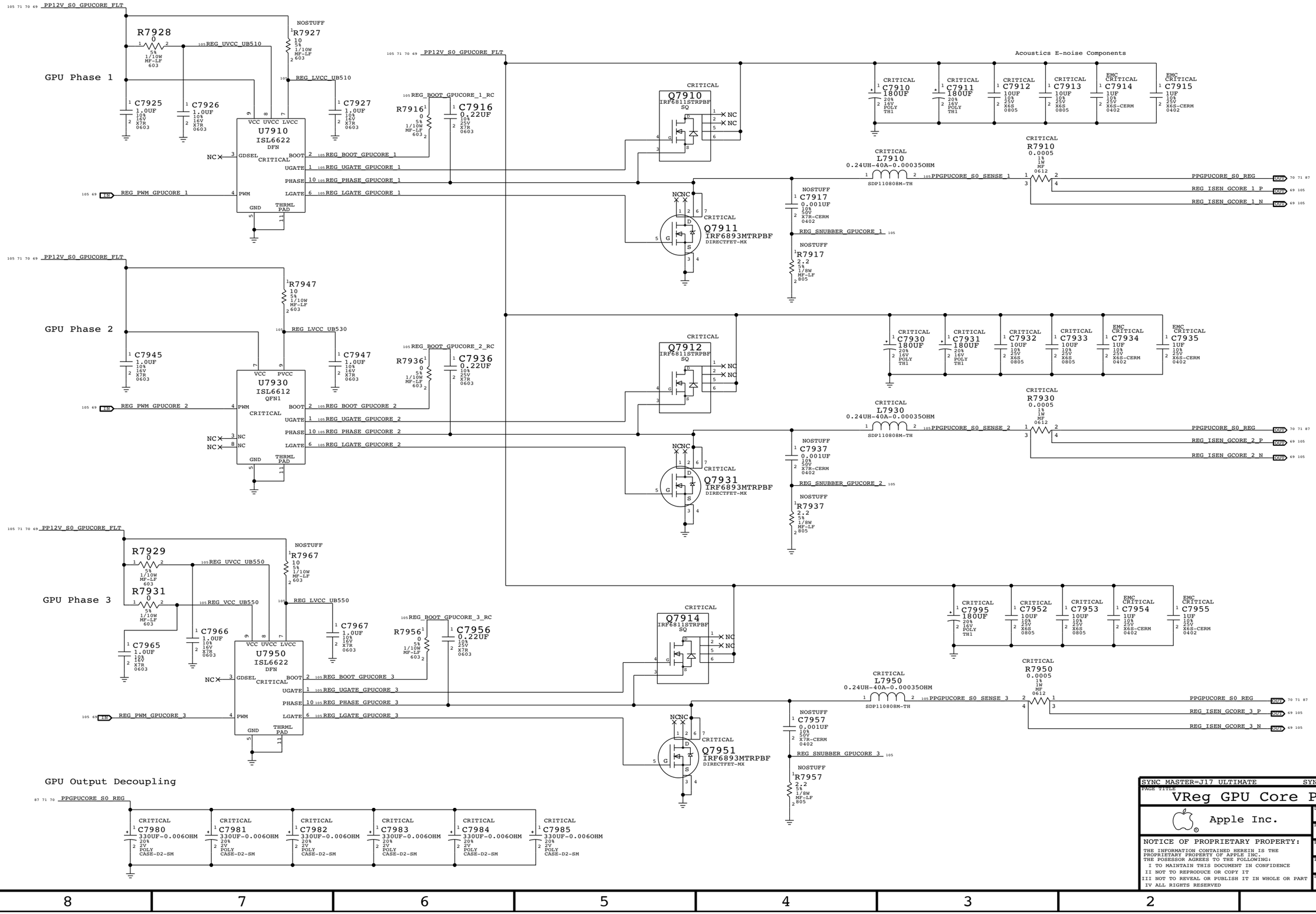
IMAX = 10.5A

CRITICAL L7800 0.36UH-30A-0.6MOHM SDP110808MR36MF-TH

152-0110

GPU CORE INPUT Filtering

SYNC MASTER=J17 ULTIMATE	SYNC DATE=05/16/2013
PAGE TITLE	VReg GPU Core Phases
Apple Inc.	DRAWING NUMBER 051-9884 · SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 78 OF 127
	SHEET 69 OF 106



SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE

VReg GPU Core Phases

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

BRANCH

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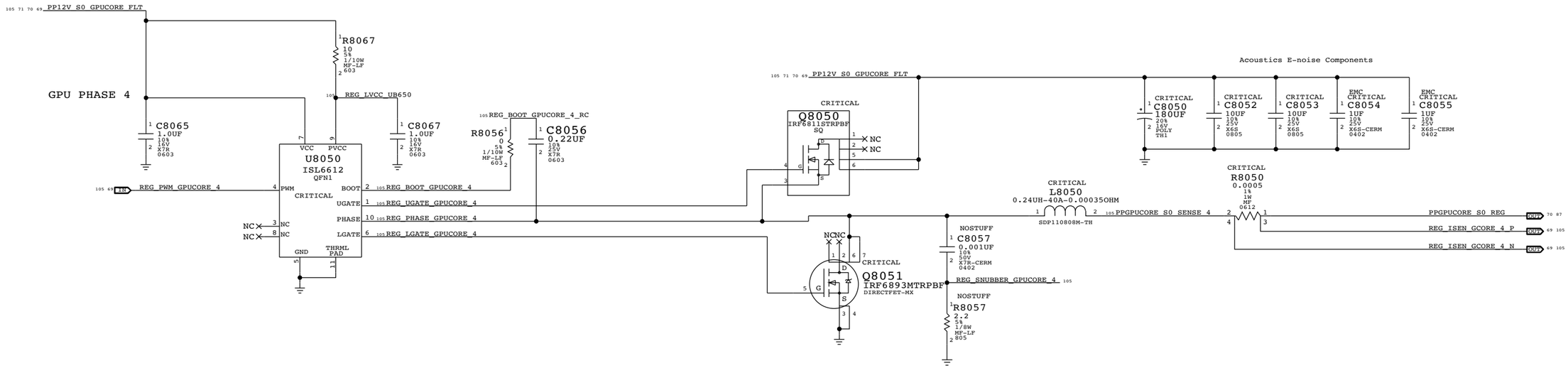
SHEET 70 OF 106



SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE

VREG GPU CORE PHASE 4

Apple Inc.

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14V BLC PRE-REGULATOR

BLC MCU

MCU ISP PROG AND TEST CONNECTOR

D8:SUOPERTEX GPIOS FOR BLC ISP RDAR://10987156

D8 PROTO 2 BLC ADDING 3.3V VOLTAGE REFERENCE RDAR://11280328

(WAS BLC_BLON)

(WAS BLC_GPIO)

BLC_EN IS DRIVEN BY TCON (CSA95)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0142	126S0128			C8149

PAGE TITLE: BACKLIGHT LED DRIVER

Apple Inc.

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BRANCH:
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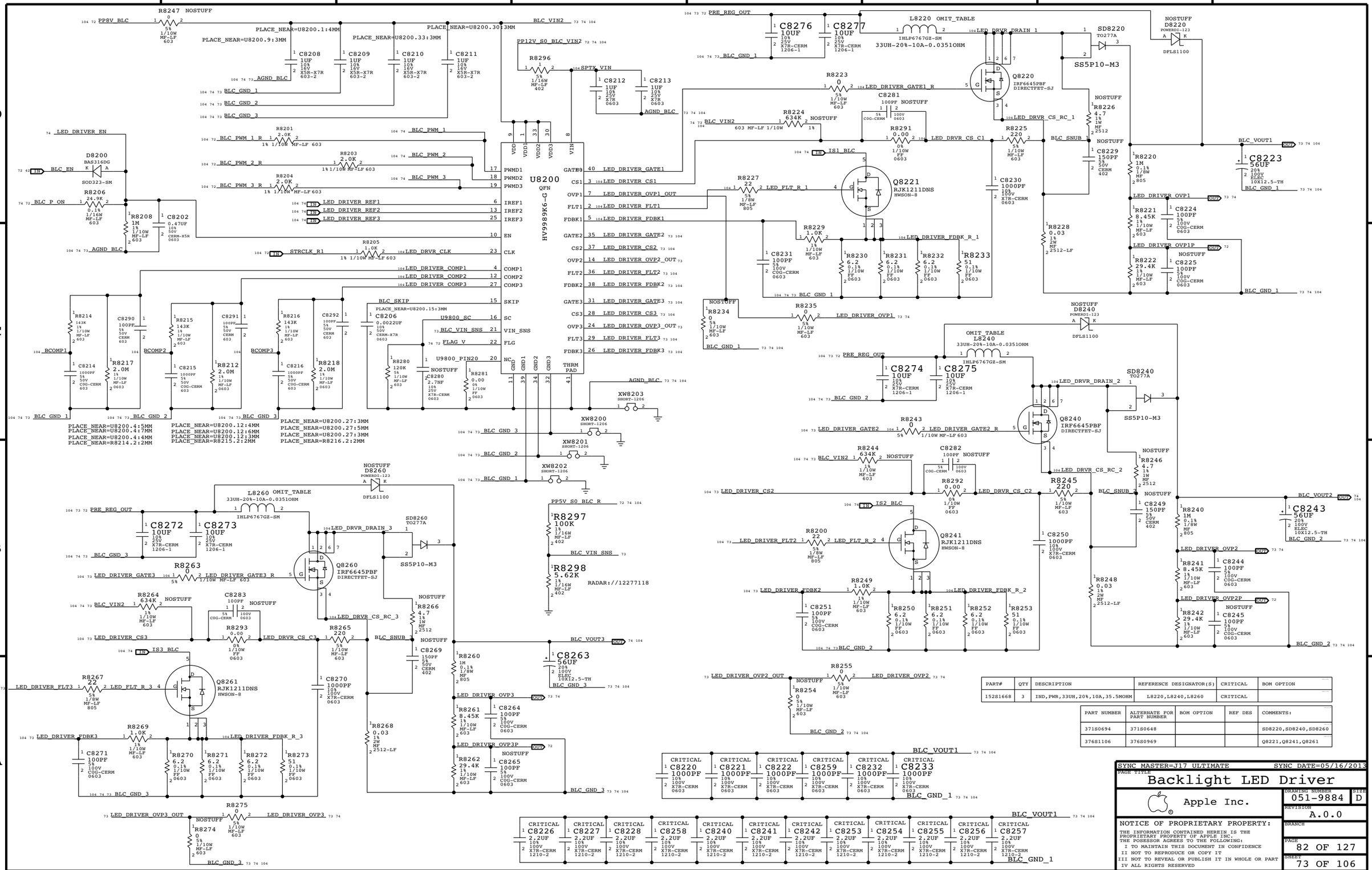
SHEET: 72 OF 106



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1668	3	IND,PWR,33UH,20%,10A,35.5MOHM	L8220,L8240,L8260	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S0694	371S0648			SD8220,SD8240,SD8260
376S1106	376S0969			Q8221,Q8241,Q8261

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE: Backlight LED Driver

Apple Inc.

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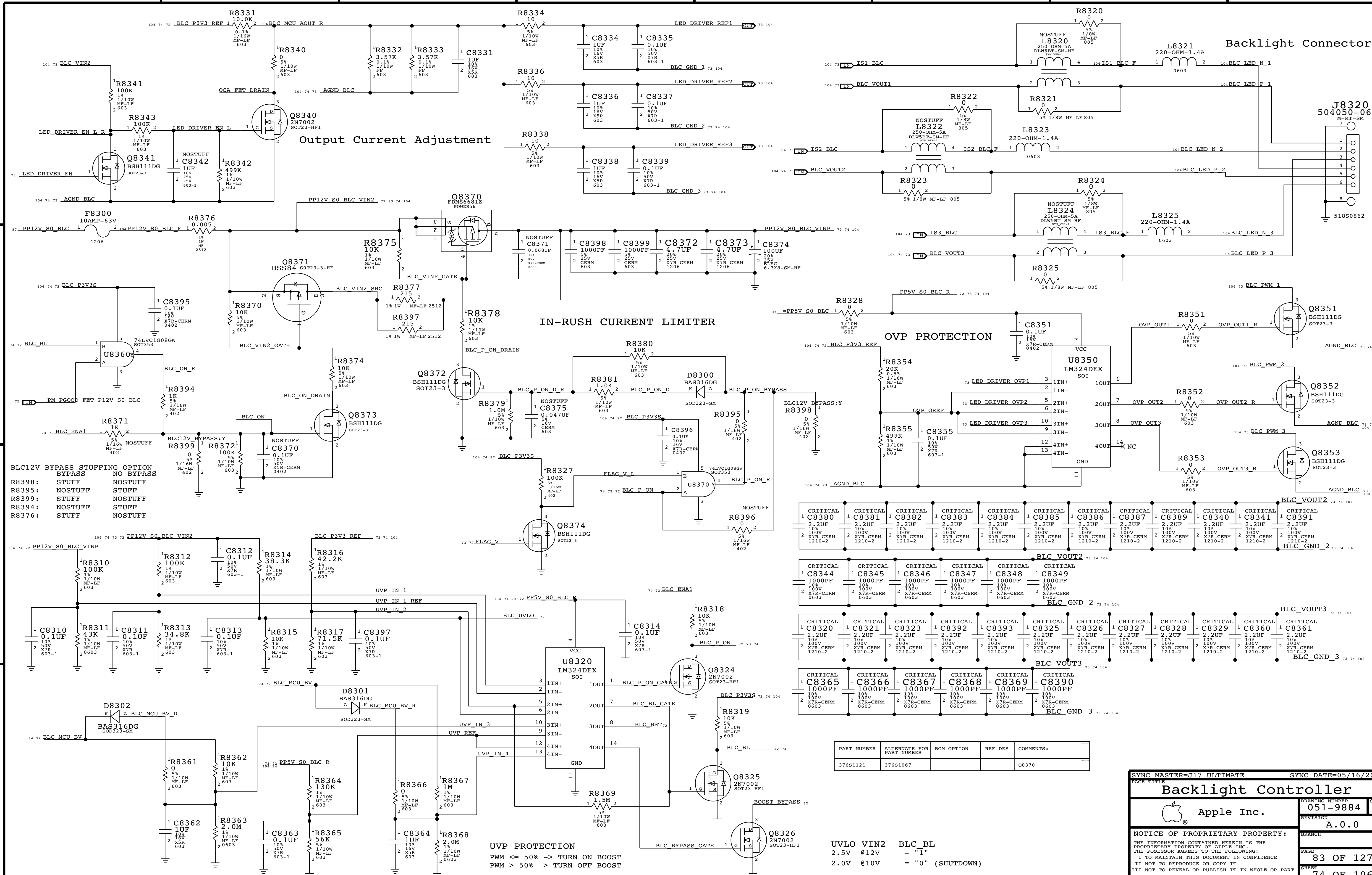

BLC12V BYPASS STUFFING OPTION

	BYPASS	NO BYPASS
R8398:	STUFF	NOSTUFF
R8395:	NOSTUFF	STUFF
R8399:	STUFF	NOSTUFF
R8394:	NOSTUFF	STUFF
R8376:	STUFF	NOSTUFF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1121	376S1067			Q8370

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE

Backlight Controller

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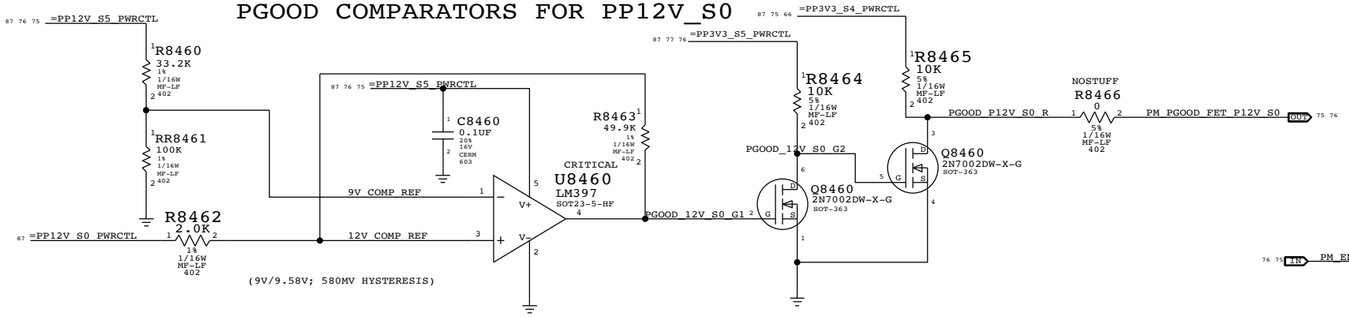
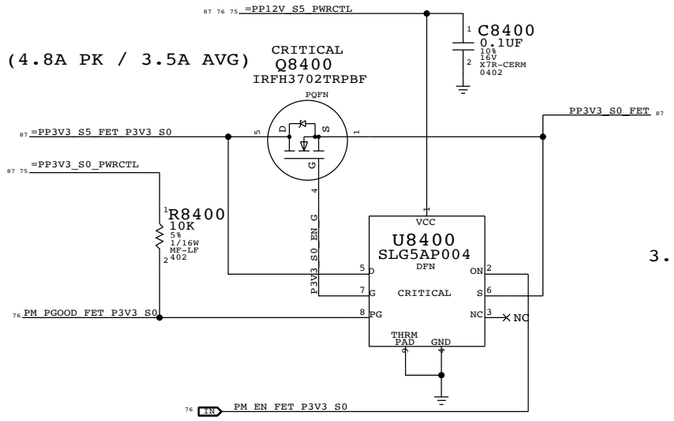
BRANCH

PGOOD COMPARATORS FOR PP12V_S0

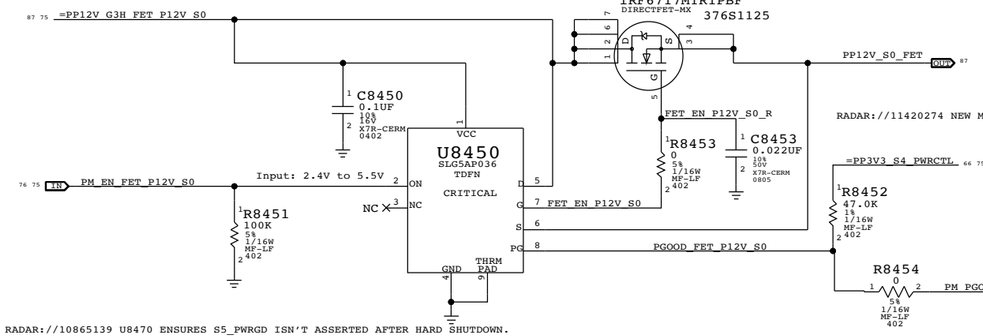


3.3V S0 FET (4.8A PK / 3.5A AVG)



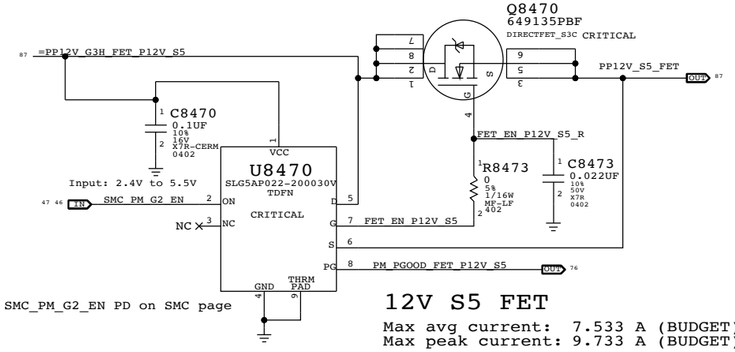
12V S0 FET

Max avg current: 20.4 A (BUDGET)
Max peak current: 24.1 A (BUDGET)



RADAR://11420274 NEW MOSFET Q8450 TO AVOID 50A 100US PULSE ON 12V S0.

RADAR://10865139 U8470 ENSURES S5_PWRGD ISN'T ASSERTED AFTER HARD SHUTDOWN.

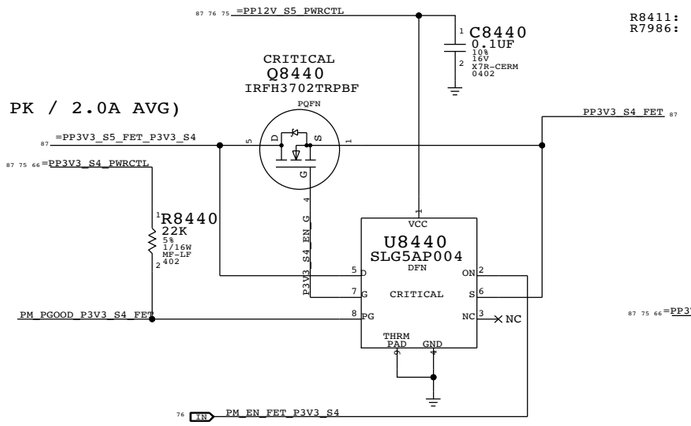


SMC_PM_G2_EN PD on SMC page

12V S5 FET

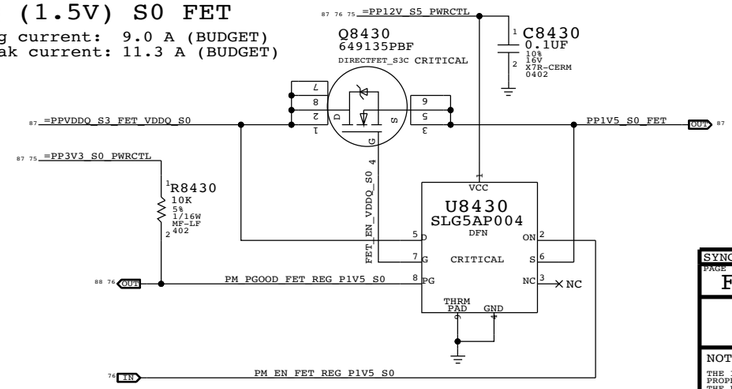
Max avg current: 7.533 A (BUDGET)
Max peak current: 9.733 A (BUDGET)

3.3V S4 FET (2.7A PK / 2.0A AVG)



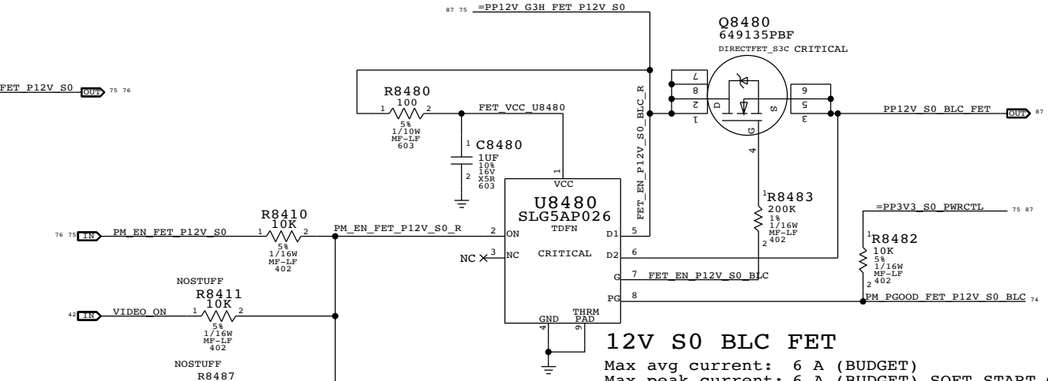
VDDQ (1.5V) S0 FET

Max avg current: 9.0 A (BUDGET)
Max peak current: 11.3 A (BUDGET)



12V S0 BLC FET

Max avg current: 6 A (BUDGET)
Max peak current: 6 A (BUDGET) SOFT START ON BLC



BLC12V BYPASS STUFFING OPTION

	BYPASS	NO BYPASS
R8411:	STUFF	NOSTUFF
R7986:	STUFF	NOSTUFF

5V S0 FET

Max avg current: 2.7 A (BUDGET)
Max peak current: 3.9 A (BUDGET)

SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE: FET-Controlled S0 and S4

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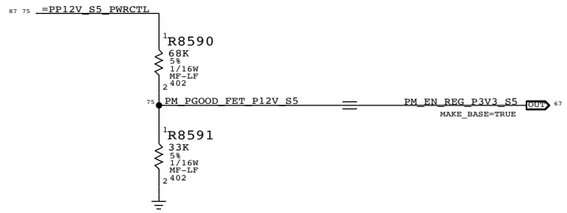
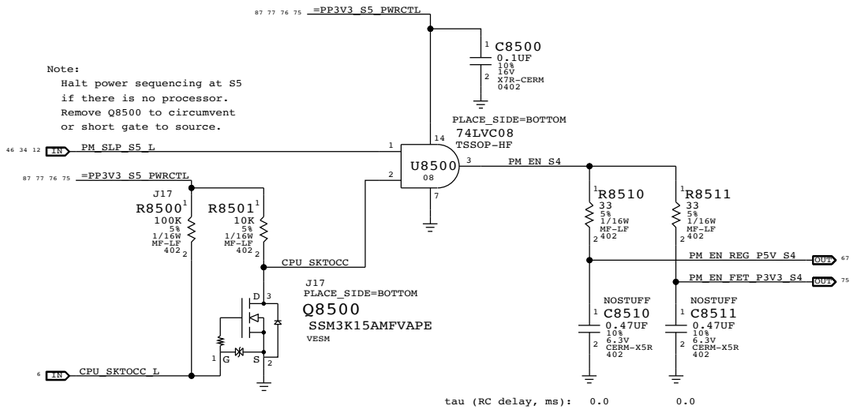
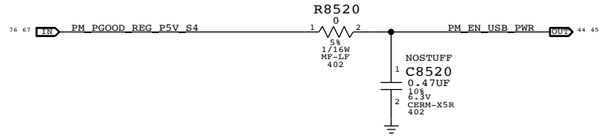
S5 Enable



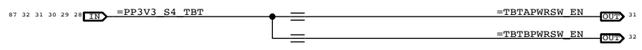
S4 Enables



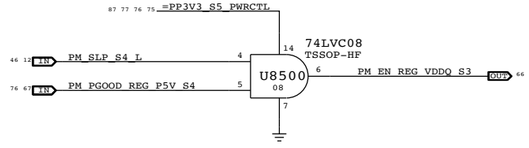
S4 USB Enable



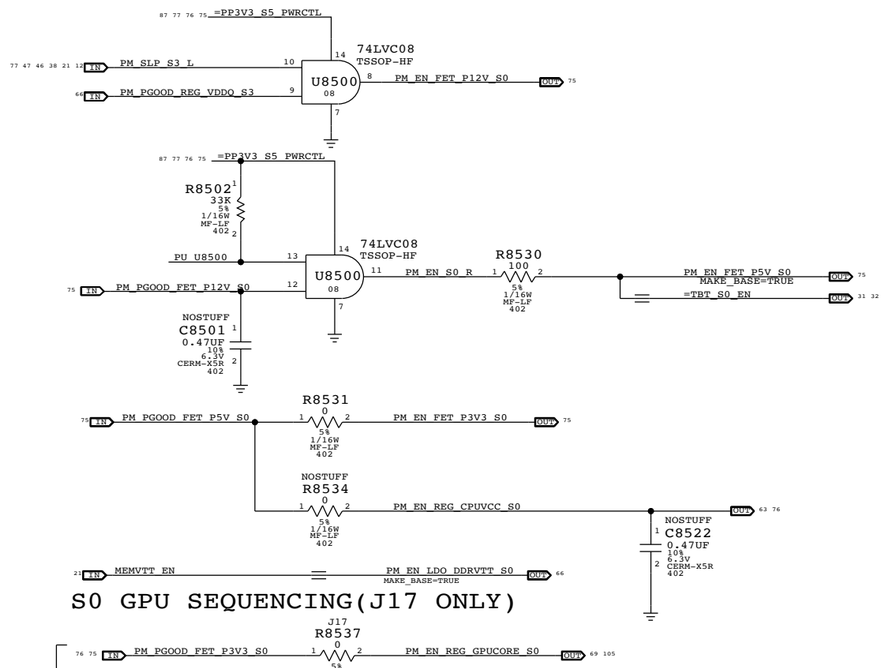
S4 TBT S4 Port Enable



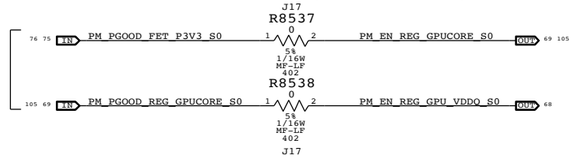
S3 VDDQ Enable



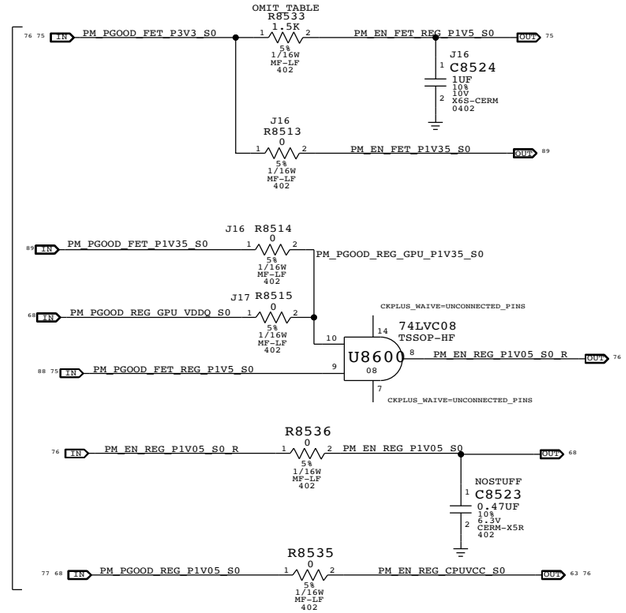
S0 Enables



S0 GPU SEQUENCING(J17 ONLY)



S0 PCH Sequencing



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0070	1	RES,1.5K,0402,5%	R8533	J16
116S0004	1	RES,0OHM,0402,5%	R8533	J17

Rail definitions

Platform: All processor non-Core and non-Graphics (5 V, 3.3 V, 1.5 V, 1.05V for PCH/TBT/GPU)
Uncore: VDDQ

Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. VCC3_3 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC3V3 ramping to 2.6V
4. VCC1_5 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC1V5 ramping to 1.35V
5. VCC may power down before VCC3_3, VCC3_3 must ramp down to 2.6V within 35ms
6. VCC may power down before VCC1_5, VCC1_5 must ramp down to 1.35V within 35ms

NVIDIA:
1. 3V3_S0 must ramp first
4. VDDQ MUST RAMP AFTER GPU_CORE
5. PEX_VDD with IFPC/D/E/F_IOVDD (1.05V) must ramp after VDDQ
6. All rails must reach their target voltages in more than 40 uS

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
PM Regulator Enables

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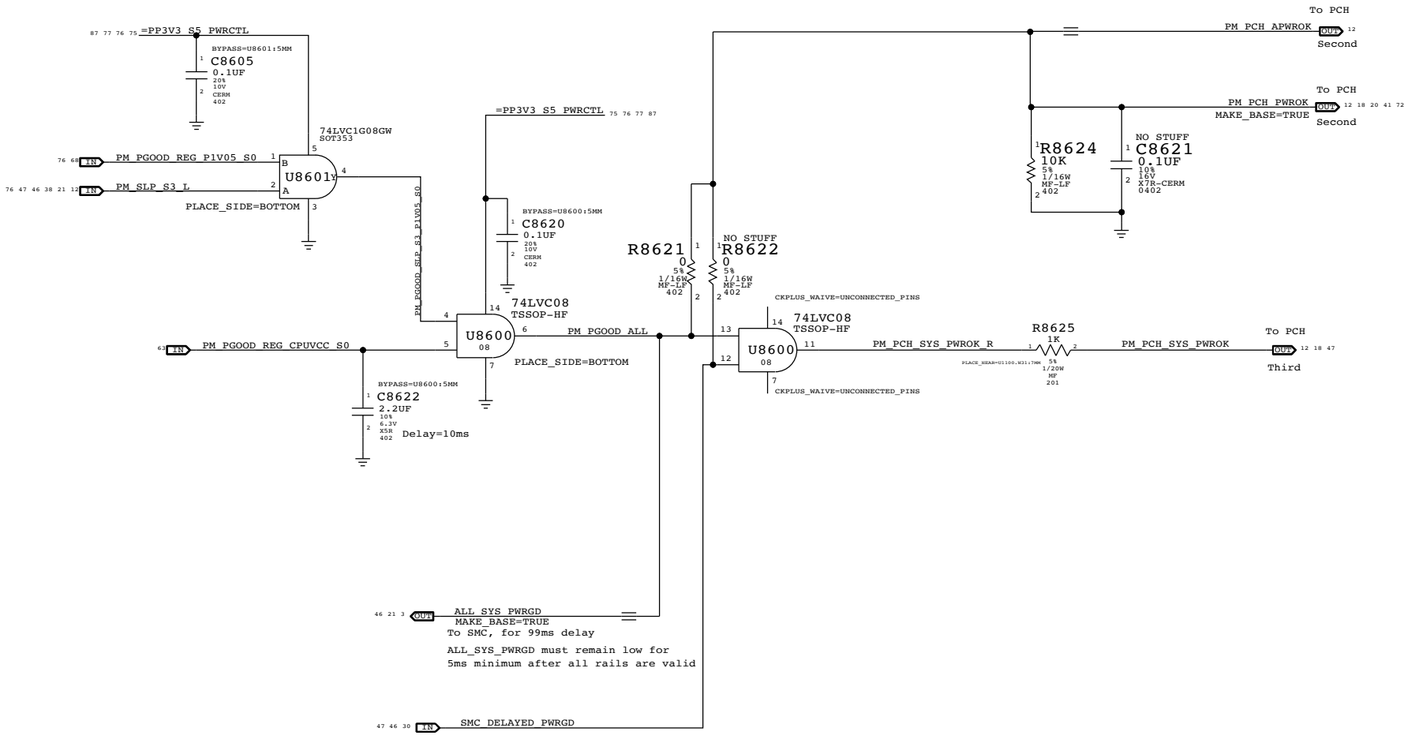
ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation

PCH Power Goods



Resume Reset

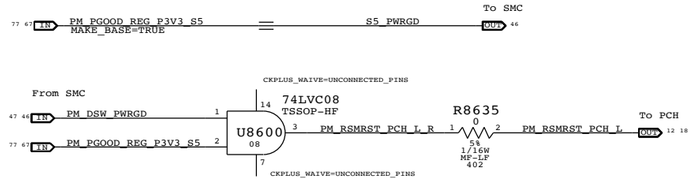
Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

Note:
The iMac J16/J17 designs does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE: PM Power Good

Apple Inc.

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Page Notes

Power aliases required by this page:

- +3VS_GPU_VDD33

Signal aliases required by this page:

(NONE)

ROM options provided by this page:

(NONE)

ALL LANES ARE REVERSED (SEE ALIASES ON CSA 102),SEE DIFF PAIRS FOR POLARITY SWAPPED

93 78	PEG_R2D_P<0>	C8720	0.22UF	1	2	PEG_R2D_C_P<0>	78 93
	POLARITY SWAPPED!		GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<0>	C8721	0.22UF	1	2	PEG_R2D_C_N<0>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_P<1>	C8722	0.22UF	1	2	PEG_R2D_C_P<1>	78 93
	POLARITY SWAPPED!		GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<1>	C8723	0.22UF	1	2	PEG_R2D_C_N<1>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_P<2>	C8724	0.22UF	1	2	PEG_R2D_C_P<2>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<2>	C8725	0.22UF	1	2	PEG_R2D_C_N<2>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_P<3>	C8726	0.22UF	1	2	PEG_R2D_C_P<3>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<3>	C8727	0.22UF	1	2	PEG_R2D_C_N<3>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_P<4>	C8728	0.22UF	1	2	PEG_R2D_C_P<4>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<4>	C8729	0.22UF	1	2	PEG_R2D_C_N<4>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<5>	C8730	0.22UF	1	2	PEG_R2D_C_P<5>	78 93
	POLARITY SWAPPED!		GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_P<5>	C8731	0.22UF	1	2	PEG_R2D_C_N<5>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_P<6>	C8732	0.22UF	1	2	PEG_R2D_C_P<6>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<6>	C8733	0.22UF	1	2	PEG_R2D_C_N<6>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_P<7>	C8734	0.22UF	1	2	PEG_R2D_C_P<7>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<7>	C8735	0.22UF	1	2	PEG_R2D_C_N<7>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<8>	C8736	0.22UF	1	2	PEG_R2D_C_P<8>	78 93
	POLARITY SWAPPED!		GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_P<8>	C8737	0.22UF	1	2	PEG_R2D_C_N<8>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<9>	C8738	0.22UF	1	2	PEG_R2D_C_P<9>	78 93
	POLARITY SWAPPED!		GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_P<9>	C8739	0.22UF	1	2	PEG_R2D_C_N<9>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<10>	C8740	0.22UF	1	2	PEG_R2D_C_P<10>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_P<10>	C8741	0.22UF	1	2	PEG_R2D_C_N<10>	78 93
	POLARITY SWAPPED!		GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_P<11>	C8742	0.22UF	1	2	PEG_R2D_C_P<11>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<11>	C8743	0.22UF	1	2	PEG_R2D_C_N<11>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<12>	C8744	0.22UF	1	2	PEG_R2D_C_P<12>	78 93
	POLARITY SWAPPED!		GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_P<12>	C8745	0.22UF	1	2	PEG_R2D_C_N<12>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<13>	C8746	0.22UF	1	2	PEG_R2D_C_P<13>	78 93
	POLARITY SWAPPED!		GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_P<13>	C8747	0.22UF	1	2	PEG_R2D_C_N<13>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<14>	C8748	0.22UF	1	2	PEG_R2D_C_P<14>	78 93
	POLARITY SWAPPED!		GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_P<14>	C8749	0.22UF	1	2	PEG_R2D_C_N<14>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_P<15>	C8750	0.22UF	1	2	PEG_R2D_C_P<15>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 78	PEG_R2D_N<15>	C8751	0.22UF	1	2	PEG_R2D_C_N<15>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		

ALL LANES ARE REVERSED (SEE ALIASES ON CSA 102),SEE DIFF PAIRS FOR POLARITY SWAPPED

93 88	PEG_D2R_P<0>	C8755	0.22UF	1	2	PEG_D2R_C_P<0>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<0>	C8756	0.22UF	1	2	PEG_D2R_C_N<0>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_P<1>	C8757	0.22UF	1	2	PEG_D2R_C_P<1>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<1>	C8758	0.22UF	1	2	PEG_D2R_C_N<1>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<2>	C8759	0.22UF	1	2	PEG_D2R_C_P<2>	78 93
	POLARITY SWAPPED!		GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_P<2>	C8760	0.22UF	1	2	PEG_D2R_C_N<2>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_P<3>	C8761	0.22UF	1	2	PEG_D2R_C_P<3>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<3>	C8762	0.22UF	1	2	PEG_D2R_C_N<3>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_P<4>	C8763	0.22UF	1	2	PEG_D2R_C_P<4>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<4>	C8764	0.22UF	1	2	PEG_D2R_C_N<4>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_P<5>	C8765	0.22UF	1	2	PEG_D2R_C_P<5>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<5>	C8766	0.22UF	1	2	PEG_D2R_C_N<5>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_P<6>	C8767	0.22UF	1	2	PEG_D2R_C_P<6>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<6>	C8768	0.22UF	1	2	PEG_D2R_C_N<6>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<7>	C8769	0.22UF	1	2	PEG_D2R_C_P<7>	78 93
	POLARITY SWAPPED!		GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_P<7>	C8770	0.22UF	1	2	PEG_D2R_C_N<7>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_P<8>	C8771	0.22UF	1	2	PEG_D2R_C_P<8>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<8>	C8772	0.22UF	1	2	PEG_D2R_C_N<8>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_P<9>	C8773	0.22UF	1	2	PEG_D2R_C_P<9>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<9>	C8774	0.22UF	1	2	PEG_D2R_C_N<9>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<10>	C8775	0.22UF	1	2	PEG_D2R_C_P<10>	78 93
	POLARITY SWAPPED!		GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_P<10>	C8776	0.22UF	1	2	PEG_D2R_C_N<10>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_P<11>	C8777	0.22UF	1	2	PEG_D2R_C_P<11>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<11>	C8778	0.22UF	1	2	PEG_D2R_C_N<11>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<12>	C8779	0.22UF	1	2	PEG_D2R_C_P<12>	78 93
	POLARITY SWAPPED!		GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_P<12>	C8780	0.22UF	1	2	PEG_D2R_C_N<12>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_P<13>	C8781	0.22UF	1	2	PEG_D2R_C_P<13>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<13>	C8782	0.22UF	1	2	PEG_D2R_C_N<13>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_P<14>	C8783	0.22UF	1	2	PEG_D2R_C_P<14>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<14>	C8784	0.22UF	1	2	PEG_D2R_C_N<14>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_N<15>	C8785	0.22UF	1	2	PEG_D2R_C_P<15>	78 93
	POLARITY SWAPPED!		GND_VOID=TRUE		20% 6.3V X5R 0201		
93 88	PEG_D2R_P<15>	C8786	0.22UF	1	2	PEG_D2R_C_N<15>	78 93
			GND_VOID=TRUE		20% 6.3V X5R 0201		

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93 78	PEG_R2D_P<0>	AN12	PEX_RX0	AK14	PEX_TX0
93 78	PEG_R2D_N<0>	AM12	PEX_RX0*	AJ14	PEX_TX0*
93 78	PEG_R2D_P<1>	AN14	PEX_RX1	AH14	PEX_TX1
93 78	PEG_R2D_N<1>	AM14	PEX_RX1*	AG14	PEX_TX1*
93 78	PEG_R2D_P<2>	AP14	PEX_RX2	AK15	PEX_TX2
93 78	PEG_R2D_N<2>	AP15	PEX_RX2*	AJ15	PEX_TX2*
93 78	PEG_R2D_P<3>	AN15	PEX_RX3	AL16	PEX_TX3
93 78	PEG_R2D_N<3>	AM15	PEX_RX3*	AK16	PEX_TX3*
93 78	PEG_R2D_P<4>	AN17	PEX_RX4	AK17	PEX_TX4
93 78	PEG_R2D_N<4>	AM17	PEX_RX4*	AJ17	PEX_TX4*
93 78	PEG_R2D_P<5>	AP17	PEX_RX5	AH17	PEX_TX5
93 78	PEG_R2D_N<5>	AP18	PEX_RX5*	AG17	PEX_TX5*
93 78	PEG_R2D_P<6>	AN18	PEX_RX6	AK18	PEX_TX6
93 78	PEG_R2D_N<6>	AM18	PEX_RX6*	AJ18	PEX_TX6*
93 78	PEG_R2D_P<7>	AN20	PEX_RX7	AL19	PEX_TX7
93 78	PEG_R2D_N<7>	AM20	PEX_RX7*	AK19	PEX_TX7*
93 78	PEG_R2D_P<8>	AP20	PEX_RX8	AK20	PEX_TX8
93 78	PEG_R2D_N<8>	AP21	PEX_RX8*	AJ20	PEX_TX8*
93 78	PEG_R2D_P<9>	AN21	PEX_RX9	AH20	PEX_TX9
93 78	PEG_R2D_N<9>	AM21	PEX_RX9*	AG20	PEX_TX9*
93 78	PEG_R2D_P<10>	AN23	PEX_RX10	AK21	PEX_TX10
93 78	PEG_R2D_N<10>	AM23	PEX_RX10*	AJ21	PEX_TX10*
93 78	PEG_R2D_P<11>	AP23	PEX_RX11	AL22	PEX_TX11
93 78	PEG_R2D_N<11>	AP24	PEX_RX11*	AK22	PEX_TX11*
93 78	PEG_R2D_P<12>	AN24	PEX_RX12	AK23	PEX_TX12
93 78	PEG_R2D_N<12>	AM24	PEX_RX12*	AJ23	PEX_TX12*
93 78	PEG_R2D_P<13>	AN26	PEX_RX13	AH23	PEX_TX13
93 78	PEG_R2D_N<13>	AM26	PEX_RX13*	AG23	PEX_TX13*
93 78	PEG_R2D_P<14>	AP26	PEX_RX14	AK24	PEX_TX14
93 78	PEG_R2D_N<14>	AP27	PEX_RX14*	AJ24	PEX_TX14*
93 78	PEG_R2D_P<15>	AN27	PEX_RX15	AL25	PEX_TX15
93 78	PEG_R2D_N<15>	AM27	PEX_RX15*	AK25	PEX_TX15*

93 11	IN PEG_CLK100M_P	AL13	PEX_REFCLK	AJ26	PEX_TSTCLK_OUT
93 11	IN PEG_CLK100M_N	AK13	PEX_REFCLK*	AK26	PEX_TSTCLK_OUT*
88 84	IN GPU_RESET_L — R8700 0 — GPU_RESET_R_L	AJ12	PEX_RST*	AP29	PEX_TERMP
11	OUT PEG_CLKREQ_L	AK12	PEX_CLKREQ*		
NC		AJ11	PEX_WAKE*		
				AG12	PEX_SVDD_3V3

R8702 200 — PLACE_NEAR=U8700.AJ26:8MM — 103:PEX_TSTCLK_O_PL — 2 MOSTUFF — 103:PEX_TSTCLK_O_NG

R8705 2.49K — PLACE_NEAR=U8700.AP29:8MM — 103:GPU_PEX_TERMP

PEX_SVDD_3V3 — =PP3V3_GPU_VDD33 83 84 85 86

SYNC_MASTER=J17 PETE SYNC_DATE=01/21/2013

PAGE TITLE

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Apple Inc.

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REVISION A.0.0

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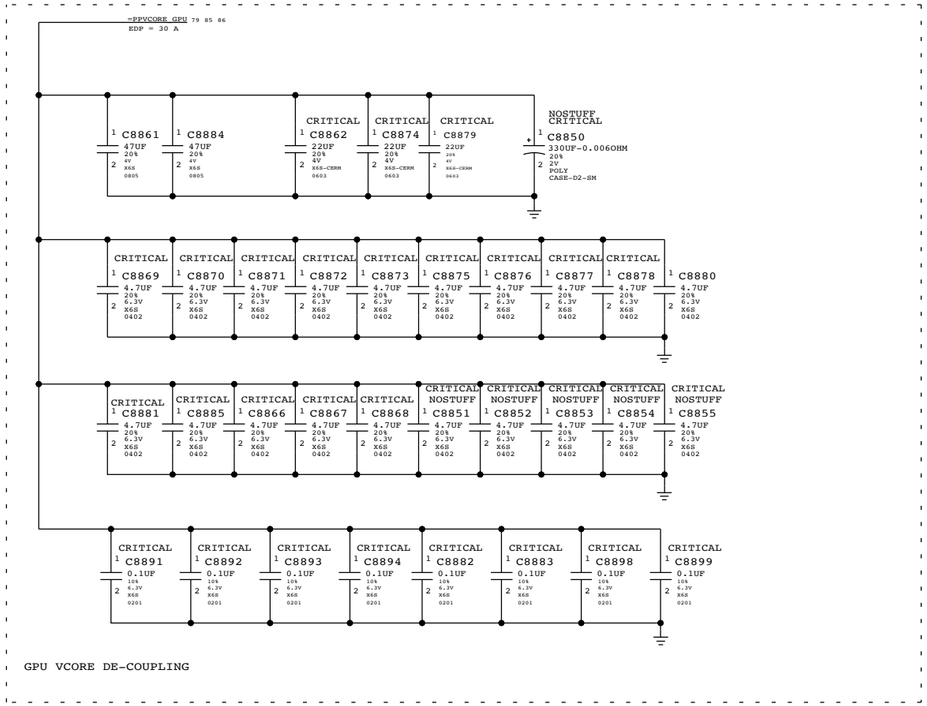
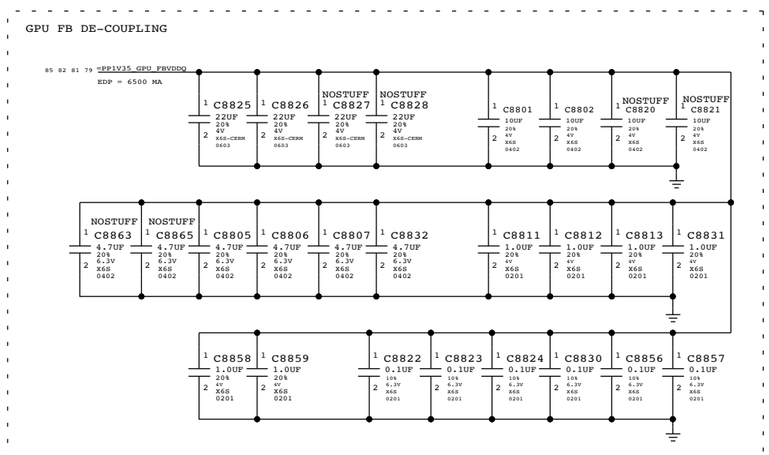
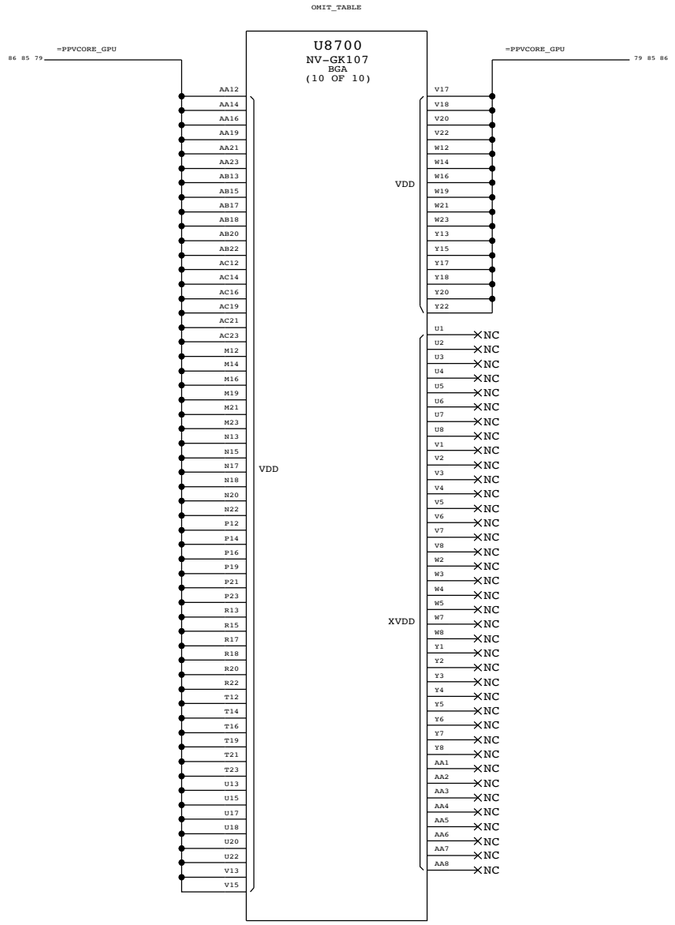
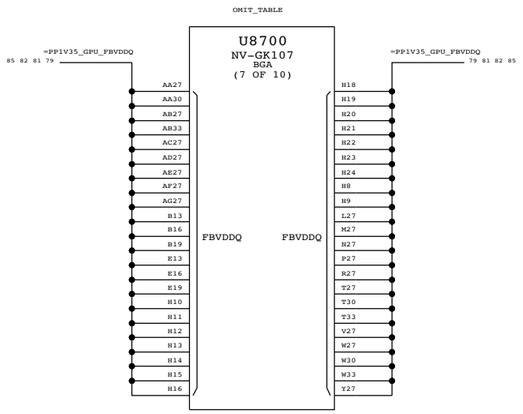
DE-COUPLING IS BASED ON NV DESIGN GUIDELINE DG-05587-001









Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PPV3V3_GPU_FWPROG

Signal aliases required by this page:

(NONE)

BOM options provided by this page.

(NONE)

SYNC MASTER=J17 PETE	SYNC DATE=01/21/2013
PAGE TITLE: KEPLER CORE/FB POWER	
Apple Inc.	DRAWING NUMBER: 051-9884 SIZE: D
	REVISION: A.0.0
	BRANCH:
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NOTE:GDDR5 MODE N MAPPING

OMIT_TABLE

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MEM INTERFACE A

103 81	B1	FB_A0_DQ<0>	L28	FBA_D0			
103 81	B1	FB_A0_DQ<1>	M29	FBA_D1			
103 81	B1	FB_A0_DQ<2>	L29	FBA_D2			
103 81	B1	FB_A0_DQ<3>	M28	FBA_D3			
103 81	B1	FB_A0_DQ<4>	N31	FBA_D4			
103 81	B1	FB_A0_DQ<5>	P29	FBA_D5			
103 81	B1	FB_A0_DQ<6>	R29	FBA_D6			
103 81	B1	FB_A0_DQ<7>	P28	FBA_D7			
103 81	B1	FB_A0_DQ<8>	J28	FBA_D8			
103 81	B1	FB_A0_DQ<9>	H29	FBA_D9			
103 81	B1	FB_A0_DQ<10>	J29	FBA_D10			
103 81	B1	FB_A0_DQ<11>	H28	FBA_D11			
103 81	B1	FB_A0_DQ<12>	G29	FBA_D12			
103 81	B1	FB_A0_DQ<13>	E31	FBA_D13			
103 81	B1	FB_A0_DQ<14>	E32	FBA_D14			
103 81	B1	FB_A0_DQ<15>	F30	FBA_D15			
103 81	B1	FB_A0_DQ<16>	C34	FBA_D16			
103 81	B1	FB_A0_DQ<17>	D32	FBA_D17			
103 81	B1	FB_A0_DQ<18>	B33	FBA_D18			
103 81	B1	FB_A0_DQ<19>	C33	FBA_D19			
103 81	B1	FB_A0_DQ<20>	F33	FBA_D20			
103 81	B1	FB_A0_DQ<21>	F32	FBA_D21			
103 81	B1	FB_A0_DQ<22>	H33	FBA_D22			
103 81	B1	FB_A0_DQ<23>	H32	FBA_D23			
103 81	B1	FB_A0_DQ<24>	P34	FBA_D24			
103 81	B1	FB_A0_DQ<25>	P32	FBA_D25			
103 81	B1	FB_A0_DQ<26>	P31	FBA_D26			
103 81	B1	FB_A0_DQ<27>	P33	FBA_D27			
103 81	B1	FB_A0_DQ<28>	L31	FBA_D28			
103 81	B1	FB_A0_DQ<29>	L34	FBA_D29			
103 81	B1	FB_A0_DQ<30>	L32	FBA_D30			
103 81	B1	FB_A0_DQ<31>	L33	FBA_D31			
103 81	B1	FB_A1_DQ<0>	AG28	FBA_D32			
103 81	B1	FB_A1_DQ<1>	AF29	FBA_D33			
103 81	B1	FB_A1_DQ<2>	AG29	FBA_D34			
103 81	B1	FB_A1_DQ<3>	AF28	FBA_D35			
103 81	B1	FB_A1_DQ<4>	AD30	FBA_D36			
103 81	B1	FB_A1_DQ<5>	AD29	FBA_D37			
103 81	B1	FB_A1_DQ<6>	AC29	FBA_D38			
103 81	B1	FB_A1_DQ<7>	AD28	FBA_D39			
103 81	B1	FB_A1_DQ<8>	AJ29	FBA_D40			
103 81	B1	FB_A1_DQ<9>	AK29	FBA_D41			
103 81	B1	FB_A1_DQ<10>	AJ30	FBA_D42			
103 81	B1	FB_A1_DQ<11>	AK28	FBA_D43			
103 81	B1	FB_A1_DQ<12>	AM29	FBA_D44			
103 81	B1	FB_A1_DQ<13>	AM31	FBA_D45			
103 81	B1	FB_A1_DQ<14>	AN29	FBA_D46			
103 81	B1	FB_A1_DQ<15>	AM30	FBA_D47			
103 81	B1	FB_A1_DQ<16>	AN31	FBA_D48			
103 81	B1	FB_A1_DQ<17>	AN32	FBA_D49			
103 81	B1	FB_A1_DQ<18>	AP30	FBA_D50			
103 81	B1	FB_A1_DQ<19>	AP32	FBA_D51			
103 81	B1	FB_A1_DQ<20>	AM33	FBA_D52			
103 81	B1	FB_A1_DQ<21>	AL31	FBA_D53			
103 81	B1	FB_A1_DQ<22>	AK33	FBA_D54			
103 81	B1	FB_A1_DQ<23>	AK32	FBA_D55			
103 81	B1	FB_A1_DQ<24>	AD34	FBA_D56			
103 81	B1	FB_A1_DQ<25>	AD32	FBA_D57			
103 81	B1	FB_A1_DQ<26>	AC30	FBA_D58			
103 81	B1	FB_A1_DQ<27>	AD33	FBA_D59			
103 81	B1	FB_A1_DQ<28>	AF31	FBA_D60			
103 81	B1	FB_A1_DQ<29>	AG34	FBA_D61			
103 81	B1	FB_A1_DQ<30>	AG32	FBA_D62			
103 81	B1	FB_A1_DQ<31>	AG33	FBA_D63			

103 81	OUT	FB_A0_WCLK_P<0>	K31	FBA_WCK01			
103 81	OUT	FB_A0_WCLK_N<0>	L30	FBA_WCK01*			
103 81	OUT	FB_A0_WCLK_P<1>	H34	FBA_WCK23			
103 81	OUT	FB_A0_WCLK_N<1>	J34	FBA_WCK23*			
103 81	OUT	FB_A1_WCLK_P<0>	AG30	FBA_WCK45			
103 81	OUT	FB_A1_WCLK_N<0>	AG31	FBA_WCK45*			
103 81	OUT	FB_A1_WCLK_P<1>	AJ34	FBA_WCK67			
103 81	OUT	FB_A1_WCLK_N<1>	AK34	FBA_WCK67*			

NC		J30	FBA_WCKB01	
NC		J31	FBA_WCKB01*	
NC		J32	FBA_WCKB23	
NC		J33	FBA_WCKB23*	
NC		AH31	FBA_WCKB45	
NC		AJ31	FBA_WCKB45*	
NC		AJ32	FBA_WCKB67	
NC		AJ33	FBA_WCKB67*	

			U30	FBA_CMD0	FB_A0_CS_L	OUT	81 103
			T31	FBA_CMD1	FB_A0_A<3>	OUT	81 103
			U29	FBA_CMD2	FB_A0_A<2>	OUT	81 103
			R34	FBA_CMD3	FB_A0_A<4>	OUT	81 103
			R33	FBA_CMD4	FB_A0_A<5>	OUT	81 103
			U32	FBA_CMD5	FB_A0_WE_L	OUT	81 103
			U33	FBA_CMD6	FB_A0_A<7>	OUT	81 103
			U28	FBA_CMD7	FB_A0_A<6>	OUT	81 103
			V28	FBA_CMD8	FB_A0_ABI_L	OUT	81 103
			V29	FBA_CMD9	FB_A0_A<8>	OUT	81 103
			V30	FBA_CMD10	FB_A0_A<0>	OUT	81 103
			U34	FBA_CMD11	FB_A0_A<1>	OUT	81 103
			V31	FBA_CMD12	FB_A0_RAS_L	OUT	81 103
			V34	FBA_CMD13	FB_A0_RESET_L	OUT	80 81 103
			V33	FBA_CMD14	FB_A0_CKE_L	OUT	80 81 103
			Y32	FBA_CMD15	FB_A0_CAS_L	OUT	81 103
			AA31	FBA_CMD16	FB_A1_CS_L	OUT	81 103
			AA29	FBA_CMD17	FB_A1_A<3>	OUT	81 103
			AA28	FBA_CMD18	FB_A1_A<2>	OUT	81 103
			AC34	FBA_CMD19	FB_A1_A<4>	OUT	81 103
			AC33	FBA_CMD20	FB_A1_A<5>	OUT	81 103
			AA32	FBA_CMD21	FB_A1_WE_L	OUT	81 103
			AA33	FBA_CMD22	FB_A1_A<7>	OUT	81 103
			Y28	FBA_CMD23	FB_A1_A<6>	OUT	81 103
			Y29	FBA_CMD24	FB_A1_ABI_L	OUT	81 103
			W31	FBA_CMD25	FB_A1_A<8>	OUT	81 103
			Y30	FBA_CMD26	FB_A1_A<0>	OUT	81 103
			AA34	FBA_CMD27	FB_A1_A<1>	OUT	81 103
			Y31	FBA_CMD28	FB_A1_RAS_L	OUT	81 103
			Y34	FBA_CMD29	FB_A1_RESET_L	OUT	80 81 103
			Y33	FBA_CMD30	FB_A1_CKE_L	OUT	80 81 103
			V31	FBA_CMD31	FB_A1_CAS_L	OUT	81 103
			R30	FBA_CLK0	FB_A0_CLK_P	OUT	81 103
			R31	FBA_CLK0*	FB_A0_CLK_N	OUT	81 103
			AB31	FBA_CLK1	FB_A1_CLK_P	OUT	81 103
			AC31	FBA_CLK1*	FB_A1_CLK_N	OUT	81 103
			P30	FBA_DQM0	FB_A0_DBI_L<0>	BI	81 103
			F31	FBA_DQM1	FB_A0_DBI_L<1>	BI	81 103
			F34	FBA_DQM2	FB_A0_DBI_L<2>	BI	81 103
			M32	FBA_DQM3	FB_A0_DBI_L<3>	BI	81 103
			AD31	FBA_DQM4	FB_A1_DBI_L<0>	BI	81 103
			AL29	FBA_DQM5	FB_A1_DBI_L<1>	BI	81 103
			AM32	FBA_DQM6	FB_A1_DBI_L<2>	BI	81 103
			AF34	FBA_DQM7	FB_A1_DBI_L<3>	BI	81 103

	M30	FBA_DQS_RN0	NC	
	H30	FBA_DQS_RN1	NC	
	E34	FBA_DQS_RN2	NC	
	M34	FBA_DQS_RN3	NC	
	AF30	FBA_DQS_RN4	NC	
	AH31	FBA_DQS_RN5	NC	
	AH34	FBA_DQS_RN6	NC	
	AF32	FBA_DQS_RN7	NC	
	M31	FBA_DQS_WP0	FB_A0_EDC<0>	IN 81 103
	G31	FBA_DQS_WP1	FB_A0_EDC<1>	IN 81 103
	E33	FBA_DQS_WP2	FB_A0_EDC<2>	IN 81 103
	M33	FBA_DQS_WP3	FB_A0_EDC<3>	IN 81 103
	AE31	FBA_DQS_WP4	FB_A1_EDC<0>	IN 81 103
	AK30	FBA_DQS_WP5	FB_A1_EDC<1>	IN 81 103
	AN33	FBA_DQS_WP6	FB_A1_EDC<2>	IN 81 103
	AF33	FBA_DQS_WP7	FB_A1_EDC<3>	IN 81 103
	K27	FB_DLL_AVDD	PP1V05_GPU_FB_DLL_AVDD	80
	U27	FBA_PLL_AVDD	PP1V05_GPU_FB_PLL_AVDD	80
	R28	FBA_DEBUG	GPU_FBA_DEBUG0	
	AC28	FBA_DEBUG	GPU_FBA_DEBUG1	
	J27	FB_CAL_PD_VDDQ	FB_CAL_PD_VDDQ	80 103
	H27	FB_CAL_PU_GND	FB_CAL_PU_GND	80 103
	H25	FB_CAL_TERM_GND	FB_CAL_TERM_GND	103
	E1	FB_CLAMP	FB_CLAMP	
	R32	FBA_CMD_RFU	NC	
	AC32	FBA_CMD_RFU	NC	
	F1	FB_VDDQ_SENSE	SNS_GPUVDDQ_P	OUT 85
	F2	FB_GND_SENSE	SNS_GPUVDDQ_N	OUT 85

103 81 80 FB_A0_RESET_L — R9050 10K 1% 1/20W MF 201 — 1 2 — VDD33

103 81 80 FB_A1_RESET_L — R9051 10K 1% 1/20W MF 201 — 1 2 — VDD33

=PP1V35_GPU_S0_FB 80 85 — R9052 10K 1% 1/20W MF 201 — R9053 10K 1% 1/20W MF 201

103 81 80 FB_A0_CKE_L

103 81 80 FB_A1_CKE_L

=PP1V35_GPU_S0_FB 80 85 — NOSTUFF R9058 1.33K 1% 1/20W MF 201 — FB_VREF 80 — NOSTUFF R9059 1.33K 1% 1/20W MF 201 — NOSTUFF C9060 0.1UF 10% 6.3V CERM-X5R 0201

FB VREF GEN (TEST ONLY)

=PP1V35_GPU_S0_FB 80 85 — NOSTUFF R9003 60.4 1% 1/20W MF 201 — NOSTUFF R9002 60.4 1% 1/20W MF 201

NOSTUFF R9070 100 5% 1/20W MF 201

R9001 60.4 1% 1/20W MF 201 — R9061 10K MF 1% 1/20W 201

NOSTUFF R9071 100 5% 1/20W MF 201

PLACE CLOSE TO BGA

103 80 FB_CAL_PU_GND — R9004 40.2 1% 1/20W MF 201

=PP1V35_GPU_S0_FB 80 85 — R9005 40.2 1% 1/20W MF 201

FB_CAL_PD_VDDQ 80 103

OMIT_TABLE

U8700
NV-GK107
BGA
(4 OF 10)
MEM INTRERFACE B

103 82	B1	FB_B0_DQ<0>	G9	FBB_D0			
103 82	B1	FB_B0_DQ<1>	E9	FBB_D1			
103 82	B1	FB_B0_DQ<2>	G8	FBB_D2			
103 82	B1	FB_B0_DQ<3>	F9	FBB_D3			
103 82	B1	FB_B0_DQ<4>	F11	FBB_D4			
103 82	B1	FB_B0_DQ<5>	G11	FBB_D5			
103 82	B1	FB_B0_DQ<6>	F12	FBB_D6			
103 82	B1	FB_B0_DQ<7>	G12	FBB_D7			
103 82	B1	FB_B0_DQ<8>	G6	FBB_D8			
103 82	B1	FB_B0_DQ<9>	F5	FBB_D9			
103 82	B1	FB_B0_DQ<10>	E6	FBB_D10			
103 82	B1	FB_B0_DQ<11>	F6	FBB_D11			
103 82	B1	FB_B0_DQ<12>	F4	FBB_D12			
103 82	B1	FB_B0_DQ<13>	G4	FBB_D13			
103 82	B1	FB_B0_DQ<14>	E2	FBB_D14			
103 82	B1	FB_B0_DQ<15>	F3	FBB_D15			
103 82	B1	FB_B0_DQ<16>	C2	FBB_D16			
103 82	B1	FB_B0_DQ<17>	D4	FBB_D17			
103 82	B1	FB_B0_DQ<18>	D3	FBB_D18			
103 82	B1	FB_B0_DQ<19>	C1	FBB_D19			
103 82	B1	FB_B0_DQ<20>	B3	FBB_D20			
103 82	B1	FB_B0_DQ<21>	C4	FBB_D21			
103 82	B1	FB_B0_DQ<22>	B5	FBB_D22			
103 82	B1	FB_B0_DQ<23>	C5	FBB_D23			
103 82	B1	FB_B0_DQ<24>	A11	FBB_D24			
103 82	B1	FB_B0_DQ<25>	C11	FBB_D25			
103 82	B1	FB_B0_DQ<26>	D11	FBB_D26			
103 82	B1	FB_B0_DQ<27>	B11	FBB_D27			
103 82	B1	FB_B0_DQ<28>	D8	FBB_D28			
103 82	B1	FB_B0_DQ<29>	A8	FBB_D29			
103 82	B1	FB_B0_DQ<30>	C8	FBB_D30			
103 82	B1	FB_B0_DQ<31>	B8	FBB_D31			
103 82	B1	FB_B1_DQ<0>	F24	FBB_D32			
103 82	B1	FB_B1_DQ<1>	G23	FBB_D33			
103 82	B1	FB_B1_DQ<2>	E24	FBB_D34			
103 82	B1	FB_B1_DQ<3>	G24	FBB_D35			
103 82	B1	FB_B1_DQ<4>	D21	FBB_D36			
103 82	B1	FB_B1_DQ<5>	E21	FBB_D37			
103 82	B1	FB_B1_DQ<6>	G21	FBB_D38			
103 82	B1	FB_B1_DQ<7>	F21	FBB_D39			
103 82	B1	FB_B1_DQ<8>	G27	FBB_D40			
103 82	B1	FB_B1_DQ<9>	D27	FBB_D41			
103 82	B1	FB_B1_DQ<10>	G26	FBB_D42			
103 82	B1	FB_B1_DQ<11>	E27	FBB_D43			
103 82	B1	FB_B1_DQ<12>	E29	FBB_D44			
103 82	B1	FB_B1_DQ<13>	F29	FBB_D45			
103 82	B1	FB_B1_DQ<14>	E30	FBB_D46			
103 82	B1	FB_B1_DQ<15>	D30	FBB_D47			
103 82	B1	FB_B1_DQ<16>	A32	FBB_D48			
103 82	B1	FB_B1_DQ<17>	C31	FBB_D49			
103 82	B1	FB_B1_DQ<18>	C32	FBB_D50			
103 82	B1	FB_B1_DQ<19>	B32	FBB_D51			
103 82	B1	FB_B1_DQ<20>	D29	FBB_D52			
103 82	B1	FB_B1_DQ<21>	A29	FBB_D53			
103 82	B1	FB_B1_DQ<22>	C29	FBB_D54			
103 82	B1	FB_B1_DQ<23>	B29	FBB_D55			
103 82	B1	FB_B1_DQ<24>	B21	FBB_D56			
103 82	B1	FB_B1_DQ<25>	C23	FBB_D57			
103 82	B1	FB_B1_DQ<26>	A21	FBB_D58			
103 82	B1	FB_B1_DQ<27>	C21	FBB_D59			
103 82	B1	FB_B1_DQ<28>	B24	FBB_D60			
103 82	B1	FB_B1_DQ<29>	C24	FBB_D61			
103 82	B1	FB_B1_DQ<30>	B26	FBB_D62			
103 82	B1	FB_B1_DQ<31>	C26	FBB_D63			

103 82	OUT	FB_B0_WCLK_P<0>	F8	FBB_WCK01			
103 82	OUT	FB_B0_WCLK_N<0>	E8	FBB_WCK01*			
103 82	OUT	FB_B0_WCLK_P<1>	A5	FBB_WCK23			
103 82	OUT	FB_B0_WCLK_N<1>	A6	FBB_WCK23*			
103 82	OUT	FB_B1_WCLK_P<0>	D24	FBB_WCK45			
103 82	OUT	FB_B1_WCLK_N<0>	D25	FBB_WCK45*			
103 82	OUT	FB_B1_WCLK_P<1>	B27	FBB_WCK67			
103 82	OUT	FB_B1_WCLK_N<1>	C27	FBB_WCK67*			

NC		D6	FBB_WCKB01	
NC		D7	FBB_WCKB01*	
NC		C6	FBB_WCKB23	
NC		B6	FBB_WCKB23*	
NC		F26	FBB_WCKB45	
NC		E26	FBB_WCKB45*	
NC		A26	FBB_WCKB67	
NC		A27	FBB_WCKB67*	

			D13	FBB_CMD0	FB_B0_CS_L	OUT	82 103
			E14	FBB_CMD1	FB_B0_A<3>	OUT	82 103
			F14	FBB_CMD2	FB_B0_A<2>	OUT	82 103
			A12	FBB_CMD3	FB_B0_A<4>	OUT	82 103
			B12	FBB_CMD4	FB_B0_A<5>	OUT	86 85 80 82 103
			C14	FBB_CMD5	FB_B0_WE_L	OUT	82 103
			B14	FBB_CMD6	FB_B0_A<7>	OUT	82 103
			G15	FBB_CMD7	FB_B0_A<6>	OUT	82 103
			F15	FBB_CMD8	FB_B0_ABI_L	OUT	82 103
			E15	FBB_CMD9	FB_B0_A<8>	OUT	82 103
			D15	FBB_CMD10	FB_B0_A<0>	OUT	82 103
			A14	FBB_CMD11	FB_B0_A<1>	OUT	82 103
			D14	FBB_CMD12	FB_B0_RAS_L	OUT	82 103
			A15	FBB_CMD13	FB_B0_RESET_L	OUT	80 82 103
			B15	FBB_CMD14	FB_B0_CKE_L	OUT	80 82 103
			C17	FBB_CMD15	FB_B0_CAS_L	OUT	82 103
			D18	FBB_CMD16	FB_B1_CS_L	OUT	82 103
			E18	FBB_CMD17	FB_B1_A<3>	OUT	82 86 85 80 103
			F18	FBB_CMD18	FB_B1_A<2>	OUT	82 103
			A20	FBB_CMD19	FB_B1_A<4>	OUT	82 103
			B20	FBB_CMD20	FB_B1_A<5>	OUT	82 103
			C18	FBB_CMD21	FB_B1_WE_L	OUT	82 103
			B18	FBB_CMD22	FB_B1_A<7>	OUT	82 103
			G18	FBB_CMD23	FB_B1_A<6>	OUT	82 103
			G17	FBB_CMD24	FB_B1_ABI_L	OUT	82 103
			F17	FBB_CMD25	FB_B1_A<8>	OUT	82 103
			D16	FBB_CMD26	FB_B1_A<0>	OUT	82 103
			A18	FBB_CMD27	FB_B1_A<1>	OUT	82 103
			D17	FBB_CMD28	FB_B1_RAS_L	OUT	82 103
			A17	FBB_CMD29	FB_B1_RESET_L	OUT	80 82 103
			B17	FBB_CMD30	FB_B1_CKE_L	OUT	80 82 103
			E17	FBB_CMD31	FB_B1_CAS_L	OUT	82 103
			D12	FBB_CLK0	FB_B0_CLK_P	OUT	82 103
			E12	FBB_CLK0*	FB_B0_CLK_N	OUT	82 103
			E20	FBB_CLK1	FB_B1_CLK_P	OUT	82 103
			F20	FBB_CLK1*	FB_B1_CLK_N	OUT	82 103
			E11	FBB_DQM0	FB_B0_DBI_L<0>	BI	82 103
			E3	FBB_DQM1	FB_B0_DBI_L<1>	BI	82 103
			A3	FBB_DQM2	FB_B0_DBI_L<2>	BI	82 103
			C9	FBB_DQM3	FB_B0_DBI_L<3>	BI	82 103
			F23	FBB_DQM4	FB_B1_DBI_L<0>	BI	82 103
			F27	FBB_DQM5	FB_B1_DBI_L<1>	BI	82 103
			C30	FBB_DQM6	FB_B1_DBI_L<2>	BI	82 103
			A24	FBB_DQM7	FB_B1_DBI_L<3>	BI	82 103
			D9	FBB_DQS_RN0	NC		
			E4	FBB_DQS_RN1	NC		
			B2	FBB_DQS_RN2	NC		
			A9	FBB_DQS_RN3	NC		
			D22	FBB_DQS_RN4	NC		
			D28	FBB_DQS_RN5	NC		
			A30	FBB_DQS_RN6	NC		
			B23	FBB_DQS_RN7	NC		
			D10	FBB_DQS_WP0	FB_B0_EDC<0>	IN	82 103
			D5	FBB_DQS_WP1	FB_B0_EDC<1>	IN	82 103
			C3	FBB_DQS_WP2	FB_B0_EDC<2>	IN	82 103
			B9	FBB_DQS_WP3	FB_B0_EDC<3>	IN	82 103
			E23	FBB_DQS_WP4	FB_B1_EDC<0>	IN	82 103
			E28	FBB_DQS_WP5	FB_B1_EDC<1>	IN	82 103
			B30	FBB_DQS_WP6	FB_B1_EDC<2>	IN	82 103
			A23	FBB_DQS_WP7	FB_B1_EDC<3>	IN	82 103
			H17	FBB_PLL_AVDD	PP1V05_GPU_FB_PLL_AVDD	80	
			G14	FBB_DEBUG0	GPU_FBB_DEBUG0	80	
			G20	FBB_DEBUG1	GPU_FBB_DEBUG1	80	
			H26	FB_VREF	FB_VREF	80	
			C12	FBB_CMD_RFU0	NC		
			C20	FBB_CMD_RFU1	NC		

C9006 1.0UF 20% 4V X6S 0201 — C9007 0.1UF 10% 6.3V X6S 0201

=PP1V35_GPU_S0_FB 80 85 — NOSTUFF R9006 60.4 1% 1/20W MF 201 — NOSTUFF R9007 60.4 1% 1/20W MF 201

80 GPU_FBB_DEBUG0

80 GPU_FBB_DEBUG1

Page Notes

Power aliases required by this page:
- =PP1V35_GPU_S0_FB
- =PP1V05_GPU_FB_PLL_AVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

L9001
30-OHM-25%-5A-0.01-OHM
=PP1V05_GPU_PEX_IOVDD 1 — 2 0603
CRITICAL
ESR = 0.050HM
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
PP1V05_GPU_FB_PLL_AVDD 80
C9001 200UF 20% 4V X5R-CERM 0402 — C9002 1.0UF 20% 4V X6S 0201 — C9003 0.1UF 10% 6.3V X6S 0201 — C9004 0.1UF 10% 6.3V X6S 0201

RDAR://11427653 D8: NV GUIDELINE USES 22UF. APPLE USES 20UF

L9002
30-OHM-25%-5A-0.01-OHM
=PP1V05_GPU_PEX_IOVDD 1 — 2 0603
CRITICAL
ESR = 0.050HM
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
PP1V05_GPU_FB_DLL_AVDD 80
C9008 200UF 20% 4V X5R-CERM 0402 — C9009 1.0UF 20% 4V X6S 0201 — C9005 0.1UF 10% 6.3V X6S 0201

FB PLL & DLL VDD

103 82 80 FB_B0_RESET_L — R9054 10K 1% 1/20W MF 201

103 82 80 FB_B1_RESET_L — R9055 10K 1% 1/20W MF 201

=PP1V35_GPU_S0_FB 80 85 — R9056 10K 1% 1/20W MF 201 — R9057 10K 1% 1/20W MF 201

103 82 80 FB_B0_CKE_L

103 82 80 FB_B1_CKE_L

MEM VREFC & VREFD SWITCH

82 81 OUT FB_SW_LEG

CRITICAL
Q9065
SSM3K15AMFVAPE
VESM

GPU_ALT_VREF — R9060 10K 5% 1/20W MF 201 — 84

SYNC_MASTER=J17 PETE — SYNC_DATE=11/02/2012

PAGE TITLE
KEPLER FRAME BUFFER I/F

Apple Inc.

DRAWING NUMBER 051-9884 — SIZE D
REVISION A.0.0
BRANCH
PAGE 90 OF 127
SHEET 80 OF 106

Page Notes

Power aliases required by this page:

- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

This memory device is in Mirrored Mode.

CK TERMINATION - A0

CK TERMINATION - A1

OMIT_TABLE

PLACE CLOSE TO U9200

PLACE CLOSE TO U9250

SYNC_MASTER=J17_PETE	SYNC_DATE=11/02/2012
PAGE TITLE: GDDR5 Frame Buffer A	
Apple Inc.	DRAWING NUMBER: 051-9884 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 92 OF 127
	SHEET: 81 OF 106

Page Notes

Power aliases required by this page:

- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

This memory device is in Mirrored Mode.

CK TERMINATION - B0

PLACE_NEAR=U9300.J11:8.4MM

FB_B0_CLK_P — R9301 40.2 1% 1/20W MF 201 — FB_B0_CK_MID — R9302 40.2 1% 1/20W MF 201 — FB_B0_CLK_N

FBB C9390 0.01UF 10% 10V X5R-CERM 0201

PLACE_NEAR=U9300.J12:8.4MM

PLACE_NEAR=U9300.J11:8.4MM

CK TERMINATION - B1

PLACE_NEAR=U9350.J11:8.4MM

FB_B1_CLK_P — R9351 40.2 1% 1/20W MF 201 — FB_B1_CK_MID — R9352 40.2 1% 1/20W MF 201 — FB_B1_CLK_N

FBB C9391 0.01UF 10% 10V X5R-CERM 0201

PLACE_NEAR=U9350.J11:8.4MM

R9300 120 1% 1/20W MF 201 FBB

R9304 1K 5% 1/20W MF 201 FBB

R9303 1K 5% 1/20W MF 201 FBB

U9300
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)

FB_B0_A<2>	H11	BA0/A2	
FB_B0_A<5>	K10	BA1/A5	
FB_B0_A<4>	K11	BA2/A4	
FB_B0_A<3>	H10	BA3/A3	
FB_B0_A<7>	K4	A8/A7	
FB_B0_A<1>	H5	A9/A1	
FB_B0_A<0>	H4	A10/A0	
FB_B0_A<6>	K5	A11/A6	
FB_B0_CKE_L	J3	CKE*	
FB_B0_CLK_P	J12	CK	
FB_B0_CLK_N	J11	CK*	
FB_B0_CS_L	G12	CS*	
FB_B0_WE_L	L12	WE*	
FB_B0_CAS_L	L3	CAS*	
FB_B0_RAS_L	G3	RAS*	
FB_B0_ZQ	J13	ZQ	
FB_B0_MF	J1	MF (MF=0)	
FB_B0_SEN	J10	SEN	
FB_B0_RESET_L	J2	RESET*	
FB_B0_ABI_L	J4	ABI*	
FB_B0_EDC<0>	C2	EDC0	
FB_B0_EDC<1>	C13	EDC1	
FB_B0_EDC<2>	R13	EDC2	
FB_B0_EDC<3>	R2	EDC3	
FB_B0_WCLK_P<0>	D4	WCK01	
FB_B0_WCLK_N<0>	D5	WCK01*	
FB_B0_WCLK_P<1>	P4	WCK23	
FB_B0_WCLK_N<1>	P5	WCK23*	

OMIT_TABLE

DBI0*	D2	FB_B0_DBI_L<0>	
DBI1*	D13	FB_B0_DBI_L<1>	
DBI2*	P13	FB_B0_DBI_L<2>	
DBI3*	P2	FB_B0_DBI_L<3>	
DQ0	A4	FB_B0_DQ<0>	
DQ1	A2	FB_B0_DQ<1>	
DQ2	B4	FB_B0_DQ<2>	
DQ3	B2	FB_B0_DQ<3>	
DQ4	E4	FB_B0_DQ<4>	
DQ5	E2	FB_B0_DQ<5>	
DQ6	F4	FB_B0_DQ<6>	
DQ7	F2	FB_B0_DQ<7>	
DQ8	A11	FB_B0_DQ<8>	
DQ9	A13	FB_B0_DQ<9>	
DQ10	B11	FB_B0_DQ<10>	
DQ11	B13	FB_B0_DQ<11>	
DQ12	E11	FB_B0_DQ<12>	
DQ13	E13	FB_B0_DQ<13>	
DQ14	F11	FB_B0_DQ<14>	
DQ15	F13	FB_B0_DQ<15>	
DQ16	U11	FB_B0_DQ<16>	
DQ17	U13	FB_B0_DQ<17>	
DQ18	T11	FB_B0_DQ<18>	
DQ19	T13	FB_B0_DQ<19>	
DQ20	N11	FB_B0_DQ<20>	
DQ21	N13	FB_B0_DQ<21>	
DQ22	M11	FB_B0_DQ<22>	
DQ23	M13	FB_B0_DQ<23>	
DQ24	U4	FB_B0_DQ<24>	
DQ25	U2	FB_B0_DQ<25>	
DQ26	T4	FB_B0_DQ<26>	
DQ27	T2	FB_B0_DQ<27>	
DQ28	N4	FB_B0_DQ<28>	
DQ29	N2	FB_B0_DQ<29>	
DQ30	M4	FB_B0_DQ<30>	
DQ31	M2	FB_B0_DQ<31>	
NC	A5	NC	
A12/RFU/NC	J5	FB_B0_A<8>	
NC	U5	NC	

U9300
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

=PP1V35_GPU_FBVDDQ

FBB C9300 4.7UF 20% 6.3V X5R 402
FBB C9301 4.7UF 20% 6.3V X5R 402
FBB C9302 4.7UF 20% 6.3V X5R 402
FBB C9303 4.7UF 20% 6.3V X5R 402
FBB C9304 4.7UF 20% 6.3V X5R 402
FBB C9305 4.7UF 20% 6.3V X5R 402

VDD

FBB C9306 1UF 20% 6.3V X5R 0201
FBB C9307 1UF 20% 6.3V X5R 0201
FBB C9308 1UF 20% 6.3V X5R 0201
FBB C9309 1UF 20% 6.3V X5R 0201
FBB C9310 1UF 20% 6.3V X5R 0201
FBB C9311 1UF 20% 6.3V X5R 0201
FBB C9312 1UF 20% 6.3V X5R 0201
FBB C9313 1UF 20% 6.3V X5R 0201
FBB C9314 1UF 20% 6.3V X5R 0201
FBB C9315 1UF 20% 6.3V X5R 0201
FBB C9316 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9317 0.1UF 10% 6.3V CERM-X5R 0201

VDDQ

FBB C9318 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9319 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9320 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9321 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9322 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9323 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9324 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9325 0.1UF 10% 6.3V CERM-X5R 0201

VSS

VSSQ

FB_B0_VREFC — J14 VREFC

FB_B0_VREFD — A10 VREFD — U10 VREFD

=PP1V35_GPU_FBVDDQ

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM

FBB R9330 549 1% 1/20W MF 201 — PLACE_NEAR=U9300.J14:8.4MM

FB_B0_VREFC

FBB C9331 820PF 10% 50V CERM 0402

FBB R9331 1.33K 1% 1/20W MF 201

FBB R9334 931 1% 1/20W MF 201 — FB_SW_LEG

PLACE CLOSE TO U9300

=PP1V35_GPU_FBVDDQ

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM

FBB R9332 549 1% 1/20W MF 201 — PLACE_NEAR=U9300.U10:8.4MM

FB_B0_VREFD

FBB C9332 820PF 10% 50V CERM 0402

FBB C9333 820PF 10% 50V CERM 0402

FBB R9333 1.33K 1% 1/20W MF 201

FBB R9335 931 1% 1/20W MF 201 — FB_SW_LEG

U9350
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

FB_B1_A<2>	K11	BA0/A2	
FB_B1_A<5>	H10	BA1/A5	
FB_B1_A<4>	H11	BA2/A4	
FB_B1_A<3>	K10	BA3/A3	
FB_B1_A<7>	H4	A8/A7	
FB_B1_A<1>	K5	A9/A1	
FB_B1_A<0>	K4	A10/A0	
FB_B1_A<6>	H5	A11/A6	
FB_B1_CKE_L	J3	CKE*	
FB_B1_CLK_P	J12	CK	
FB_B1_CLK_N	J11	CK*	
FB_B1_CS_L	L12	CS*	
FB_B1_WE_L	G12	WE*	
FB_B1_CAS_L	G3	CAS*	
FB_B1_RAS_L	L3	RAS*	
FB_B1_ZQ	J13	ZQ	
FB_B1_MF	J1	MF (MF=1)	
FB_B1_SEN	J10	SEN	
FB_B1_RESET_L	J2	RESET*	
FB_B1_ABI_L	J4	ABI*	
FB_B1_EDC<0>	R2	EDC0	
FB_B1_EDC<1>	R13	EDC1	
FB_B1_EDC<2>	C13	EDC2	
FB_B1_EDC<3>	C2	EDC3	
FB_B1_WCLK_P<0>	P4	WCK01	
FB_B1_WCLK_N<0>	P5	WCK01*	
FB_B1_WCLK_P<1>	D4	WCK23	
FB_B1_WCLK_N<1>	D5	WCK23*	

OMIT_TABLE

DBI1*	P13	FB_B1_DBI_L<1>	
DBI2*	D13	FB_B1_DBI_L<2>	
DBI0*	P2	FB_B1_DBI_L<0>	
DBI3*	D2	FB_B1_DBI_L<3>	
DQ0	U4	FB_B1_DQ<0>	
DQ1	U2	FB_B1_DQ<1>	
DQ2	T4	FB_B1_DQ<2>	
DQ3	T2	FB_B1_DQ<3>	
DQ4	N4	FB_B1_DQ<4>	
DQ5	N2	FB_B1_DQ<5>	
DQ6	M4	FB_B1_DQ<6>	
DQ7	M2	FB_B1_DQ<7>	
DQ8	U11	FB_B1_DQ<8>	
DQ9	U13	FB_B1_DQ<9>	
DQ10	T11	FB_B1_DQ<10>	
DQ11	T13	FB_B1_DQ<11>	
DQ12	N11	FB_B1_DQ<12>	
DQ13	N13	FB_B1_DQ<13>	
DQ14	M11	FB_B1_DQ<14>	
DQ15	M13	FB_B1_DQ<15>	
DQ16	A11	FB_B1_DQ<16>	
DQ17	A13	FB_B1_DQ<17>	
DQ18	B11	FB_B1_DQ<18>	
DQ19	B13	FB_B1_DQ<19>	
DQ20	E11	FB_B1_DQ<20>	
DQ21	E13	FB_B1_DQ<21>	
DQ22	F11	FB_B1_DQ<22>	
DQ23	F13	FB_B1_DQ<23>	
DQ24	A4	FB_B1_DQ<24>	
DQ25	A2	FB_B1_DQ<25>	
DQ26	B4	FB_B1_DQ<26>	
DQ27	B2	FB_B1_DQ<27>	
DQ28	E4	FB_B1_DQ<28>	
DQ29	E2	FB_B1_DQ<29>	
DQ30	F4	FB_B1_DQ<30>	
DQ31	F2	FB_B1_DQ<31>	
NC	A5	NC	
A12/RFU/NC	J5	FB_B1_A<8>	
NC	U5	NC	

U9350
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

=PP1V35_GPU_FBVDDQ

FBB C9350 4.7UF 20% 6.3V X5R 402
FBB C9351 4.7UF 20% 6.3V X5R 402
FBB C9352 4.7UF 20% 6.3V X5R 402
FBB C9353 4.7UF 20% 6.3V X5R 402
FBB C9354 4.7UF 20% 6.3V X5R 402
FBB C9355 4.7UF 20% 6.3V X5R 402

VDD

FBB C9356 1UF 20% 6.3V X5R 0201
FBB C9357 1UF 20% 6.3V X5R 0201
FBB C9358 1UF 20% 6.3V X5R 0201
FBB C9359 1UF 20% 6.3V X5R 0201
FBB C9360 1UF 20% 6.3V X5R 0201
FBB C9361 1UF 20% 6.3V X5R 0201
FBB C9362 1UF 20% 6.3V X5R 0201
FBB C9363 1UF 20% 6.3V X5R 0201
FBB C9364 1UF 20% 6.3V X5R 0201
FBB C9365 1UF 20% 6.3V X5R 0201
FBB C9366 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9367 0.1UF 10% 6.3V CERM-X5R 0201

VDDQ

FBB C9368 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9369 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9370 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9371 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9372 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9373 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9374 0.1UF 10% 6.3V CERM-X5R 0201
FBB C9375 0.1UF 10% 6.3V CERM-X5R 0201

VSS

VSSQ

FB_B1_VREFC — J14 VREFC

FB_B1_VREFD — A10 VREFD — U10 VREFD

=PP1V35_GPU_FBVDDQ

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM

FBB R9380 549 1% 1/20W MF 201 — PLACE_NEAR=U9350.J14:8.4MM

FB_B1_VREFC

FBB C9381 820PF 10% 50V CERM 0402

FBB R9381 1.33K 1% 1/20W MF 201

FBB R9384 931 1% 1/20W MF 201 — FB_SW_LEG

PLACE CLOSE TO U9350

=PP1V35_GPU_FBVDDQ

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM

FBB R9382 549 1% 1/20W MF 201 — PLACE_NEAR=U9350.U10:8.4MM

FB_B1_VREFD

FBB C9382 820PF 10% 50V CERM 0402

FBB C9383 820PF 10% 50V CERM 0402

FBB R9383 1.33K 1% 1/20W MF 201

FBB R9385 931 1% 1/20W MF 201 — FB_SW_LEG

R9354 1K 5% 1/20W MF 201 FBB — =PP1V35_GPU_FBVDDQ

R9350 120 1% 1/20W MF 201 FBB

R9353 1K 5% 1/20W MF 201 FBB

SYNC_MASTER=J17_PETE SYNC_DATE=11/02/2012

PAGE TITLE: GDDR5 Frame Buffer B

Apple Inc.

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BRANCH	
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PD FOR AUX CHANNELS (FOR NVIDIA)

DP_INT_EG_AUX_P
DP_INT_EG_AUX_N
DP_TBTSNK0_EG_AUXCH_P
DP_TBTSNK0_EG_AUXCH_N
DP_TBTSNK1_EG_AUXCH_P
DP_TBTSNK1_EG_AUXCH_N

R9614 100K 1% 1/20W MF 201
R9613 100K 1% 1/20W MF 201
R9615 100K 1% 1/20W MF 201
R9616 100K 1% 1/20W MF 201
R9617 100K 1% 1/20W MF 201
R9618 100K 1% 1/20W MF 201

DISABLE PHYS A, B & C FOR D8

GPU_IFPA_IOVDD
GPU_IFPB_IOVDD
GPU_IFPC_IOVDD
PP1V05_GPU_IFPD_IOVDD
PP1V05_GPU_IFPEF_IOVDD
PP1V05_GPU_IFPEF_IOVDD

GPU_IFPAB_PLLVDD
GPU_IFPX_PLLVDD
PP3V3_GPU_IFPX_PLLVDD
PP3V3_GPU_IFPX_PLLVDD
IFPD_RESET
IFPEF_RESET

OMIT_TABLE
CRITICAL

U8700
NV-GK107
BGA
(5 OF 10)

IFPA_IOVDD	AG8	IFPA_TXC	AM6 → NC
IFPB_IOVDD	AG9	IFPA_TXC*	AN6 → NC
IFPC_IOVDD	AF6	IFPA_TXD0	AP3 → NC
IFPD_IOVDD	AG6	IFPA_TXD0*	AN3 → NC
IFPE_IOVDD	AC7	IFPA_TXD1	AN5 → NC
IFPF_IOVDD	AC8	IFPA_TXD1*	AM5 → NC
IFPAB_PLLVDD	AH8	IFPA_TXD2	AL6 → NC
IFPAB_RSET	AJ8	IFPA_TXD2*	AK6 → NC
IFPC_PLLVDD	AF7	IFPA_TXD3	AJ6 → NC
IFPC_RSET	AF8	IFPA_TXD3*	AH6 → NC
IFPD_PLLVDD	AG7	IFPB_TXC	AJ9 → NC
IFPD_RSET	AH2	IFPB_TXC*	AH9 → NC
IFPEF_PLLVDD	AH8	IFPB_TXD4	AF6 → NC
IFPEF_RSET	AD6	IFPB_TXD4*	AF5 → NC
		IFPB_TXD5	AM7 → NC
		IFPB_TXD5*	AL7 → NC
		IFPB_TXD6	AH8 → NC
I2CA_SCL	R4	IFPB_TXD6*	AM8 → NC
I2CA_SDA	R5	IFPB_TXD7	AK8 → NC
		IFPB_TXD7*	AL8 → NC
		IFPC_AUX_I2CW_SCL	AG3 → NC
		IFPC_AUX_I2CW_SDA*	AG2 → NC
I2C_SCL	R2	IFPC_L0	AK1 → NC
I2CC_SDA	R3	IFPC_L0*	AJ1 → NC
		IFPC_L1	AJ3 → NC
		IFPC_L1*	AJ2 → NC
		IFPC_L2	AH3 → NC
I2CS_SCL	T4	IFPC_L2*	AH4 → NC
I2CS_SDA	T3	IFPC_L3	AG5 → NC
		IFPC_L3*	AG4 → NC
		IFPD_AUX_I2CX_SCL	AK3 → DP_INT_EG_AUX_P
		IFPD_AUX_I2CX_SDA*	AK2 → DP_INT_EG_AUX_N
		IFPD_L0	AM1 → DP_INT_EG_ML_P<0>
		IFPD_L0*	AM2 → DP_INT_EG_ML_N<0>
		IFPD_L1	AM3 → DP_INT_EG_ML_P<1>
		IFPD_L1*	AM4 → DP_INT_EG_ML_N<1>
		IFPD_L2	AL3 → DP_INT_EG_ML_P<2>
		IFPD_L2*	AL4 → DP_INT_EG_ML_N<2>
		IFPD_L3	AK4 → DP_INT_EG_ML_P<3>
		IFPD_L3*	AK5 → DP_INT_EG_ML_N<3>
I2C_SCL	R7	IFPE_AUX_I2CY_SCL	AB3 → DP_TBTSNK0_EG_AUXCH_P
I2C_SDA	R6	IFPE_AUX_I2CY_SDA*	AB4 → DP_TBTSNK0_EG_AUXCH_N
		IFPE_L0	AD2 → DP_TBTSNK0_ML_C_P<0>
		IFPE_L0*	AD3 → DP_TBTSNK0_ML_C_N<0>
		IFPE_L1	AD1 → DP_TBTSNK0_ML_C_P<1>
		IFPE_L1*	AC1 → DP_TBTSNK0_ML_C_N<1>
		IFPE_L2	AC2 → DP_TBTSNK0_ML_C_P<2>
		IFPE_L2*	AC3 → DP_TBTSNK0_ML_C_N<2>
		IFPE_L3	AC4 → DP_TBTSNK0_ML_C_P<3>
		IFPE_L3*	AC5 → DP_TBTSNK0_ML_C_N<3>
		IFPF_AUX_I2C2_SCL	AF3 → DP_TBTSNK1_EG_AUXCH_P
		IFPF_AUX_I2C2_SDA*	AF2 → DP_TBTSNK1_EG_AUXCH_N
		IFPF_L0	AE3 → DP_TBTSNK1_ML_C_P<0>
		IFPF_L0*	AE4 → DP_TBTSNK1_ML_C_N<0>
		IFPF_L1	AF4 → DP_TBTSNK1_ML_C_P<1>
		IFPF_L1*	AF5 → DP_TBTSNK1_ML_C_N<1>
		IFPF_L2	AD4 → DP_TBTSNK1_ML_C_P<2>
		IFPF_L2*	AD5 → DP_TBTSNK1_ML_C_N<2>
		IFPF_L3	AG1 → DP_TBTSNK1_ML_C_P<3>
		IFPF_L3*	AF1 → DP_TBTSNK1_ML_C_N<3>
		DACA_VDD	AG10 ← DAC_AVDD
		DACA_RED	AK9 → NC
		DACA_GREEN	AL10 → NC
		DACA_BLUE	AL9 → NC
		DACA_VREF	AP9 → NC
		DACA_RSET	AP8 → NC
		DACA_HSYNC	AM9 → NC
		DACA_VSYNC	AN9 → NC
		CEC	L3 → NC

DDC MAPPING
I2CA -> IFPE DDC
I2CB -> IFPF DDC
I2CC -> Not used (was ext SSC cntl)

GPU_IFPA_IOVDD → R9601 10K 1% 1/20W MF 201
GPU_IFPB_IOVDD → R9602 10K 1% 1/20W MF 201
GPU_IFPC_IOVDD → R9603 10K 1% 1/20W MF 201
GPU_TESTMODE → R9608 10K 1% 1/20W MF 201
GPU_IFPAB_PLLVDD → R9604 10K 1% 1/20W MF 201
GPU_IFPX_PLLVDD → R9619 10K 1% 1/20W MF 201

PD FOR RSET

IFPD_RSET → R9606 1K 1% 1/20W MF 201 (PLACE_NEAR=U8700.AK2:5MM)
IFPEF_RSET → R9607 1K 1% 1/20W MF 201 (PLACE_NEAR=U8700.AD6:5MM)

Page Notes

Power aliases required by this page:
- +PP3V3_GPU_IFPA_IOVDD
- +PP1V05_GPU_IFPCD_IOVDD
- +PP1V8_GPU_IFPA_IOVDD
- +PP1V05_GPU_IFPEF_IOVDD
- +PP1V8_GPU_SMBJ
- +PP3V3_GPU_VDD33
- +PP1V05_GPU_SMBJ
- +PP3V3_GPU_IFPX_PLLVDD

Signal aliases required by this page:
(NONE)

ROM options provided by this page:
- J31:VBB
- J5:VBB

PP1V05_GPU_SP_PLLVDD = PP1V05_GPU_VID_PLLVDD (MAKE_BASE=TRUE)
DP_TBTSNK0_EG_AUXCH_P = DP_TBTSNK0_AUXCH_C_P (MAKE_BASE=TRUE)
DP_TBTSNK0_EG_AUXCH_N = DP_TBTSNK0_AUXCH_C_N (MAKE_BASE=TRUE)
DP_TBTSNK1_EG_AUXCH_P = DP_TBTSNK1_AUXCH_C_P (MAKE_BASE=TRUE)
DP_TBTSNK1_EG_AUXCH_N = DP_TBTSNK1_AUXCH_C_N (MAKE_BASE=TRUE)

=PP3V3_GPU_VDD33

R9624 4.7K 1% 1/20W MF 201
R9623 4.7K 1% 1/20W MF 201
R9625 2.2K 5% 1/20W MF 201 NOSTUFF
R9626 2.2K 5% 1/20W MF 201 NOSTUFF
R9629 100K 1% 1/20W MF 201
R9630 100K 1% 1/20W MF 201

=PP3V3_GPU_VDD33

R9627 2.2K 5% 1/20W MF 201 NOSTUFF
R9628 2.2K 5% 1/20W MF 201 NOSTUFF
R9632 100K 1% 1/20W MF 201
R9631 100K 1% 1/20W MF 201
R9600 10K 1% 1/20W MF 201

CRITICAL
L9604 330-OHM-1.2A 0603
=PP3V3_GPU_IFPX_PLLVDD → PP3V3_GPU_IFPX_PLLVDD (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V)

IFPX PLLVDD
C9619 4.7UF 20% 6.3V X6S 0402
C9615 1UF 20% 6.3V X5R 0201
C9617 0.1UF 10% 6.3V X6S 0201
C9618 0.1UF 10% 6.3V X6S 0201
C9612 0.1UF 10% 6.3V X6S 0201

L9605
FERR-220-OHM-2A 0603
CRITICAL
ESR = 0.050OHM
=PP1V05_GPU_IFPCD_IOVDD → PP1V05_GPU_IFPD_IOVDD (MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=1.05V)

IFP CD IOVDD
C9625 4.7UF 20% 6.3V X6S 0402
C9656 1.0UF 20% 4V X6S 0201
C9657 0.1UF 10% 6.3V X6S 0201
C9658 0.1UF 10% 6.3V X6S 0201

L9606
FERR-220-OHM-2A 0603
CRITICAL
ESR = 0.050OHM
=PP1V05_GPU_IFPEF_IOVDD → PP1V05_GPU_IFPEF_IOVDD (MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=1.05V)

IFP EF IOVDD
C9633 4.7UF 20% 6.3V X6S 0402
C9634 4.7UF 20% 6.3V X6S 0402
C9635 1.0UF 20% 4V X6S 0201
C9636 1.0UF 20% 4V X6S 0201
C9637 0.1UF 10% 6.3V X6S 0201
C9638 0.1UF 10% 6.3V X6S 0201
C9631 0.1UF 10% 6.3V X6S 0201
C9632 0.1UF 10% 6.3V X6S 0201

OMIT_TABLE

U8700
NV-GK107
BGA
(6 OF 10)

=PP3V3_GPU_MISC	J8	
=PP3V3_GPU_VDD33	K8	
	L8	VDD33
	M8	
GPU_ROM_CS_L	H6	ROM_CS*
GPU_ROM_SCLK	H4	ROM_SCLK
GPU_ROM_SI	H5	ROM_SI
GPU_ROM_SO	H7	ROM_SO
MULTI_STRAP_REF	J1	MULTI_STRAP_REF0_GND
GPU_TESTMODE	AK11	TESTMODE
PP1V05_GPU_SP_PLLVDD	AE8	SP_PLLVDD
PP1V05_GPU_PLLVDD	AD8	PLLVDD
PP1V05_GPU_VID_PLLVDD	AD7	VID_PLLVDD
GPU_OSC_27M_XTALIN	H3	XTAL_IN
GPU_OSC_27M_XTALOUT	H2	XTAL_OUT
GPU_XTAL_OUTBUFF	J4	XTAL_OUTBUFF
GPU_XTAL_SSIN	H1	XTAL_SSIN
GPU_MLS_STRAP0	J2	STRAP0
GPU_MLS_STRAP1	J7	STRAP1
GPU_MLS_STRAP2	J6	STRAP2
GPU_MLS_STRAP3	J5	STRAP3
GPU_MLS_STRAP4	J3	STRAP4
GPIO0	P6	GPU_GPIO_0
GPIO1	M3	GPU_GPIO_1
GPIO2	L6	GPU_GPIO_2
GPIO3	P5	GPU_GPIO_3
GPIO4	P7	GPU_GPIO_4
GPIO5	L7	GPU_GPIO_5
GPIO6	M7	GPU_GPIO_6
GPIO7	N8	GPU_GPIO_7
GPIO8	M1	GPU_GPIO_8
GPIO9	M2	GPU_GPIO_9
GPIO10	L1	GPU_GPIO_10
GPIO11	M5	GPU_GPIO_11
GPIO12	N3	GPU_GPIO_12
GPIO13	M4	GPU_GPIO_13
GPIO14	N4	GPU_GPIO_14
GPIO15	P2	GPU_GPIO_15
GPIO16	R8	GPU_GPIO_16
GPIO17	M6	GPU_GPIO_17
GPIO18	R1	GPU_GPIO_18
GPIO19	P3	GPU_GPIO_19
GPIO20	P4	GPU_GPIO_20
GPIO21	P1	GPU_GPIO_21
JTAG_TCK	AM10	GPU_JTAG_TCK
JTAG_TDI	AM11	GPU_JTAG_TDI
JTAG_TDO	AP12	GPU_JTAG_TDO
JTAG_TMS	AP11	GPU_JTAG_TMS
JTAG_TRST*	AN11	GPU_JTAG_TRST_L
THERMDP	K3	GPU_TDIODE_P
THERMDN	K4	GPU_TDIODE_N

R9609 40.2K 1% 1/20W MF 0201 (PLACE_NEAR=U8700.J1:5MM)
R9620 10K 5% 1/20W MF 201
R9622 10K 5% 1/20W MF 201
R9610 10K 5% 1/20W MF 201

GPU PLL VDD

L9607
FERR-220-OHM-2A 0603
CRITICAL
ESR = 0.050OHM
=PP1V05_GPU_PEX_PLLVDD → PP1V05_GPU_PLLVDD (PLACE_NEAR=U8700.AD6:5MM, MIN_LINE_WIDTH=0.41MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=1.05V)

C9651 20UF 20% 4V X5R-CERM 0402
C9654 0.1UF 10% 6.3V X6S 0201

GPU 3V3 VDD

=PP3V3_GPU_VDD33
C9642 1UF 20% 6.3V X5R 0201
C9643 0.1UF 10% 6.3V X6S 0201
C9644 0.1UF 10% 6.3V X6S 0201

=PP3V3_GPU_MISC
C9646 4.7UF 20% 6.3V X6S 0402
C9649 0.1UF 10% 6.3V X6S 0201
C9650 0.1UF 10% 6.3V X6S 0201

SYNC_MASTER=J17_PETE	SYNC_DATE=11/02/2012
PAGE TITLE	KEPLER EDP/DP/GPIO
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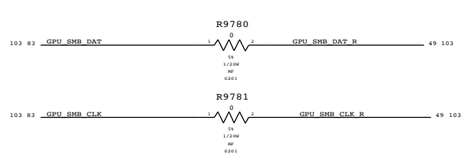
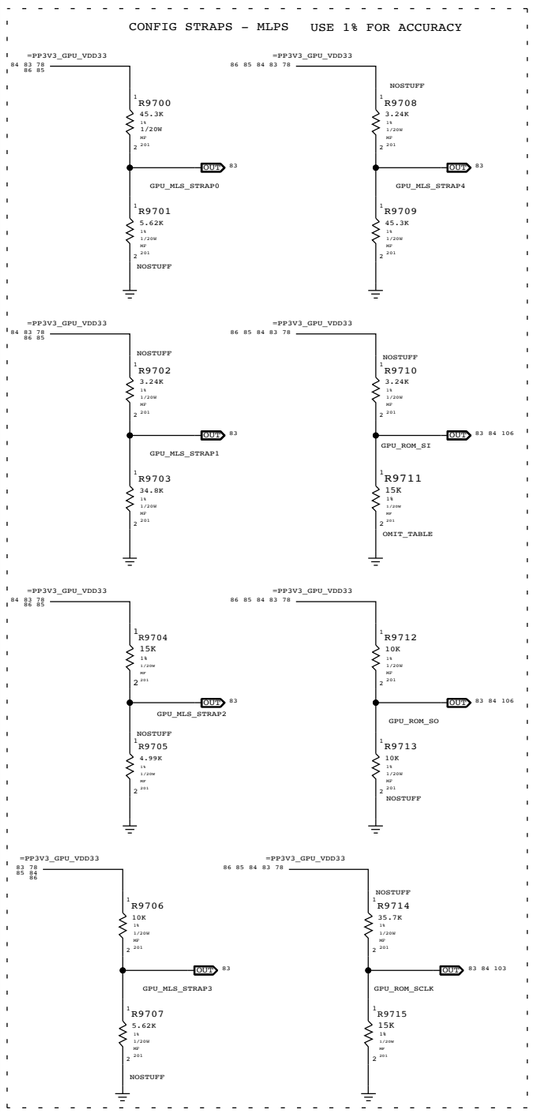
IV ALL RIGHTS RESERVED

ISOLATION R's for GPU Int Temp Sense

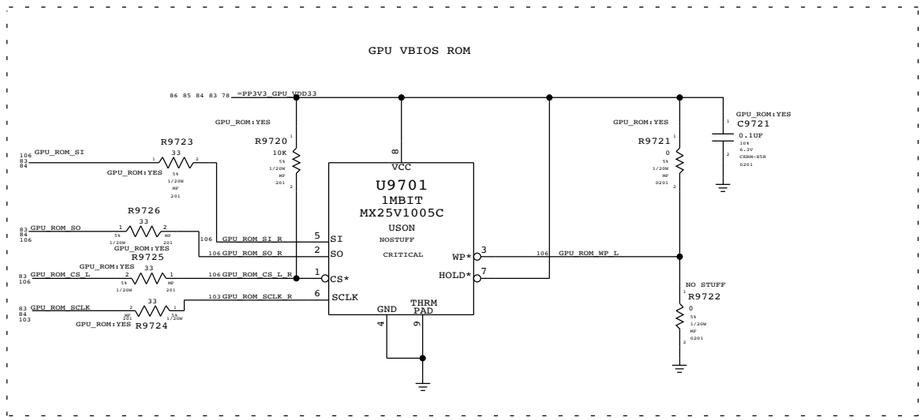


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0280	1	RES,MF,30.1K ,1,1/20W,0201	R9711		FB:2G_ELPIDA
118S0230	1	RES,MF,24.9K ,1,1/20W,0201	R9711		FB:2G_HYNIX

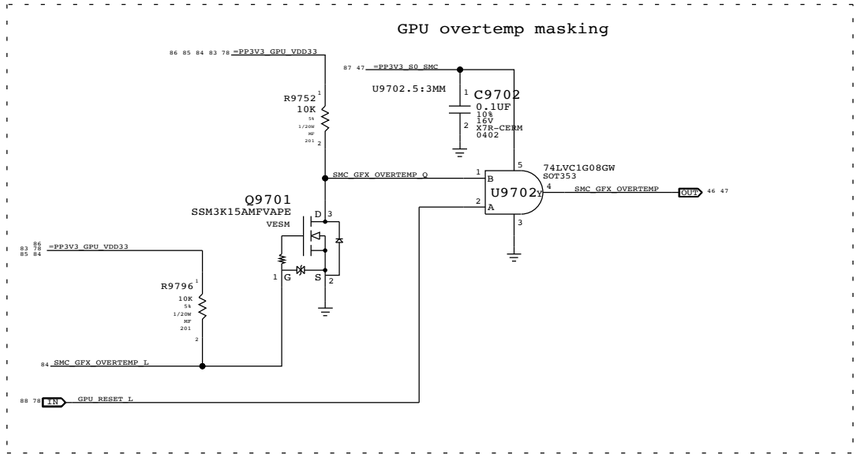
CONFIG STRAPS - MLPS USE 1% FOR ACCURACY



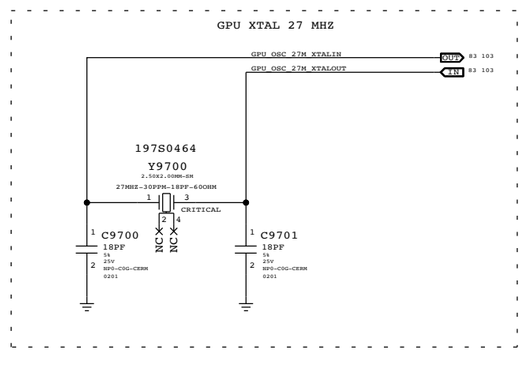
GPU VBIOS ROM

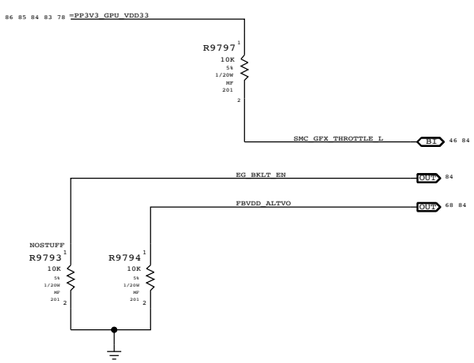


GPU overtemp masking

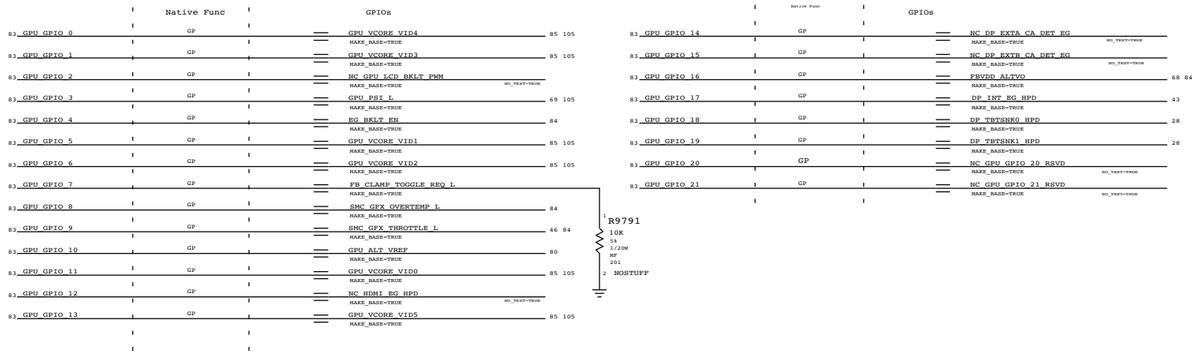


GPU XTAL 27 MHZ





Native Func GPIOs



GPIOs

SYNC_MASTER=J17_PETE SYNC_DATE=11/02/2012

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KEPLER GPIOS,CLK & STRAPS

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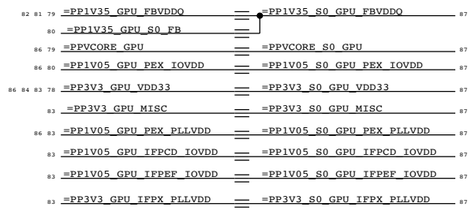
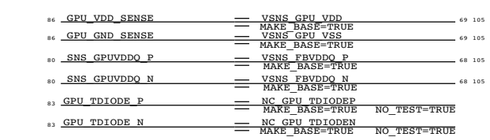
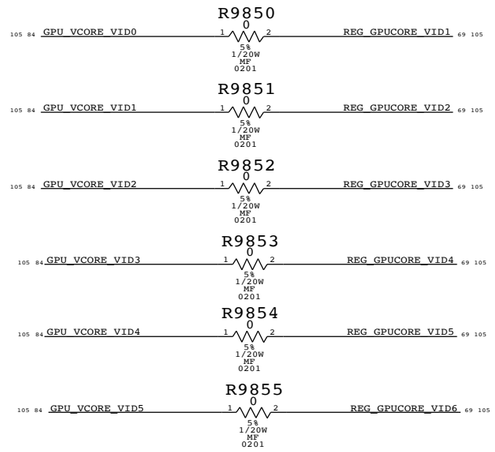
GPU POWER ALIAS



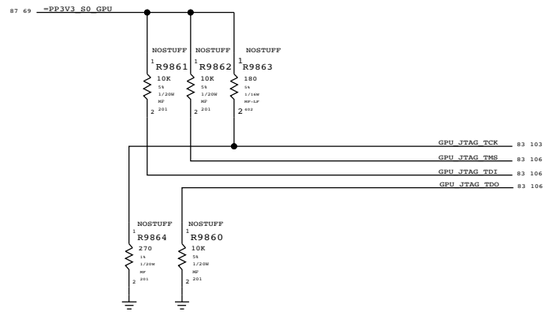
GPU SIGNAL & SENSE ALIAS



GPU VIDS ALIAS (VR VID0 IS TIED LOW)



PU/PD IS BASED ON RECOMMENDATION FROM NVDIA FOR THEIR GPU JTAG DEBUGGER



SYNC MASTER=J17 PETE SYNC DATE=01/21/2013

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GPU SIGNAL & POWER ALIASES

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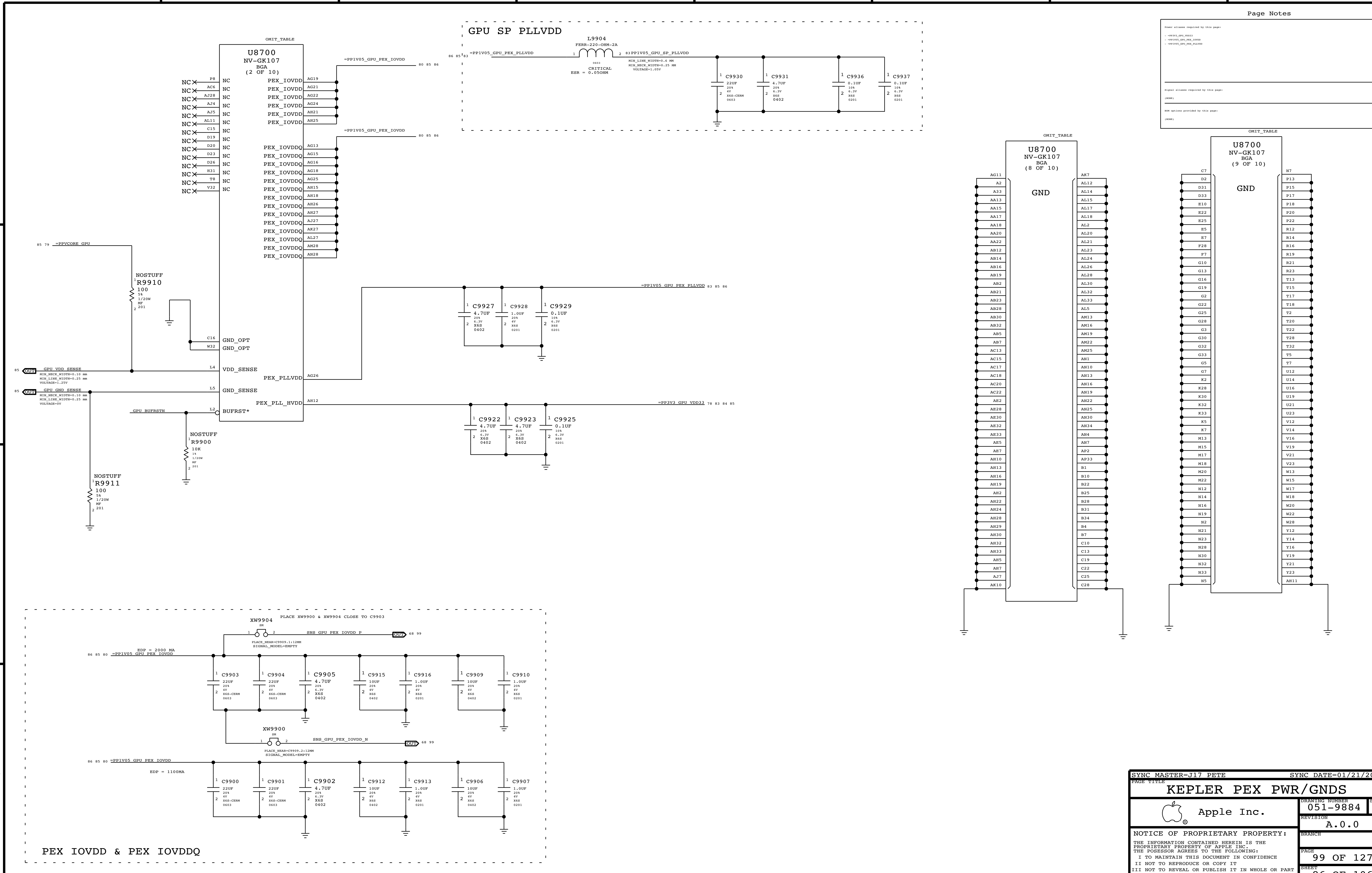

SYNC_MASTER=J17_PETE SYNC_DATE=01/21/2013

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KEPLER PEX PWR/GNDS

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G3 Rails

Always on: Keeps the PCH RTC alive

101	PP3V3_G3 (MAKE_BASE=TRUE)	PP3V3_G3_RTC	19
		=PP3V3_G3_PCH_RTC	15
		=PP3V3_G3_PCH	11 12

G3H Rails

On with AC/DC plugged in

101	PP12V_ACDC (MAKE_BASE=TRUE)	PP12V_G3H_ACDC	62
		=PP12V_G3H_SNS_R	50
101	PP12V_G3H (MAKE_BASE=TRUE)	PP12V_G3H_SNS	50
		=PP12V_G3H_P3V42	62
		=PP12V_G3H_FET_P12V_S0	75
		=PP12V_G3H_FET_P12V_S5	75
101	PP3V42_G3H (MAKE_BASE=TRUE)	PP3V42_G3H_REG	62
		=PP3V3_G3H_BT	34
		=PP3V3_G3H_RTC_D	19
		=PP3V3_G3H_SMC	46 47 53
		=PP3V3_G3H_SMC_USBMUX	44
		=PPVIN_G3H_SMCVREF	47
		=PP3V3_G3H_LPCPLUS	48

Ground/Common

GND (MAKE_BASE=TRUE)		

S5 Rails

On when in S5

101	PP12V_S5 (MAKE_BASE=TRUE)	PP12V_S5_FET	75
		=PP12V_S5_REG_P3V3P5V_S5	67
		=PP12V_S5_REG_VDDQ_S3	66
		=PP12V_S5_PWRCTL	75 76
		=PPHV_SW_TBTAPWRSW	31
		=PPHV_SW_TBTBPWRSW	32
		=PP12V_S5_SNS	50
101	PP5V_S5 (MAKE_BASE=TRUE)	PP5V_S5_LDO	67
		=PP5V_S5_PWRCTL	67
101	PP3V3_S5 (MAKE_BASE=TRUE)	PP3V3_S5_REG	67
		=PP3V3_S5_FET_P3V3_S0	75
		=PP3V3_S5_FET_P3V3_S4	75
		=PP3V3_S5_SMC	47
		=PP3V3_S5_LED	3
		=PP3V3_S5_PCH_VCCSUS_GPIO	11 12 13 14 15 17
		=PP3V3_S5_PCH_VCCDSW	15 17
		=PP3V3_S5_PCH_VCC_SPI	15 17
		=PP3V3_S5_PCH_VCCSUS_HDA	15 17
		=PP3V3_S5_PCH_VCCSUS_USB	15 17
		=PP3V3_S5_PCH_VCCSUS_RTC	15 17
		=PP3V3_S5_PCH_VCCSUS_USB3	15
		=PP3V3_S5_PCH	19 20
		=PP3V3_S5_PWRCTL	75 76 77
		=PP3V3_S5_ROM	48
		=PP3V3_S5_VRD	67
		=PP3V3_S5_XDP	18
		=PP3V3_S5_SENSE	50
		=PP3V3_S5_SNS	51

S4 Rails

Enabled when system has AC and is in run or sleep

	I2380		
101	PP5V_S4 (MAKE_BASE=TRUE)	PP5V_S4_REG	67
	I2381	=PP5V_S4_REG_VDDQ_S3	66
	I2382	=PP5V_S4_FET_P5V_S0	75
	I2384	=PP5V_S4_MEMRESET	21
	I2383	=PP5V_S4_USB	44 45
	I2385	=PP5V_S4_CAMERA	40
	I2387		
101	PP3V3_S4 (MAKE_BASE=TRUE)	PP3V3_S4_FET	75
	I2386	=PP3V3_S4_FET_ENET	38
	I2388	=PP3V3_S4_PWRCTL	66 75
	I2389	=PP3V3_S4_ALS	40
	I2390	=PP3V3_S4_LED	3
	I2392	=PP3V3_S4_MEMRESET	21
	I2391	=PP3V3_S4_PCH	13
	I2393	=PP3V3_S4_PM	21
	I2394	=PP3V3_S4_SDCARD	39
	I2396	=PP3V3_S4_SMC	47
	I2395	=PP3V3_S4_SMBUS_SMC_2	49
	I2397	=PP3V3_S4_TBT	28 29 30 31 32 76
	I2398	=PP3V3_S4_CAMERA	40 41
	I2399	=PP3V3_S4_AUDIO_DIG	58
	I2401	=PP3V3_S4_AP_SNS_R	50
	I2400	=PP3V3_S3_VREFMRGN	22
	I2402	=PP3V3_S4_TBTAPWRSW	31
	I2403	=PP3V3_S4_TBTBPWRSW	32
101	PP3V3_S4_AP (MAKE_BASE=TRUE)	PP3V3_S4_AP_SNS	50
		=PP3V3_S4_AP	34 47

S3 Rails

Enabled when system is in run or sleep

101	PP3V3_ENET (MAKE_BASE=TRUE)	PP3V3_ENET_FET	38
		=PP3V3_ENET_PHY	37 38
		=PP3V3_ENET_SYSCLK	19
		=PPVDDIO_ENET_CLK	19
99	PPVDDQ_S3 (MAKE_BASE=TRUE)	PPVDDQ_S3_REG	66
		=PPVDDQ_S3_SNS_DDR_R	51
	THIS IS 1.5V RAIL	=PPVDDQ_S3_FET_VDDQ_S0	75
99	PPVDDQ_S3_DDR (MAKE_BASE=TRUE)	PPVDDQ_S3_SNS_DDR	51
		=PPDDR_S3_MEMVREF	22
	THIS IS 1.5V RAIL	=PPVDDQ_S3_MEM_A	23 24
		=PPVDDQ_S3_MEM_B	25 26
		=PPVDDQ_S3_MEMRESET	21
		=PPVDDQ_S3_LDO_DDRVTT	66

S0 Rails

Enabled when system is in run

101	PP12V_S0 (MAKE_BASE=TRUE)	PP12V_S0_FET	75
		=PP12V_S0_AUDIO_SPKRAMP	56 57
		=PP12V_S0_FAN	53
		=PP12V_S0_SNS_GPUCORE_R	50
		=PP12V_S0_LCD	42
		=PP12V_S0_REG_CPUVCC_S0	64
		=PP12V_S0_REG_P1V05_S0	68
		=PP12V_S0_PWRCTL	75
		=PP12V_S0_SNS_FBVDDQ_R	50
		=PP12V_S0_HDD	36
101	PP12V_S0_GPUCORE (MAKE_BASE=TRUE)	PP12V_S0_SNS_GPUCORE	50
		=PP12V_S0_REG_GPUCORE	69
101	PPHDD12_S0 (MAKE_BASE=TRUE)	PP12V_S0_HDD_FET	36
		=PP12V_S0_HDD_SNS_R	50
101	PP12V_S0_HDD (MAKE_BASE=TRUE)	PP12V_S0_HDD_SNS	50
		=PP12V_S0_HDD_PWR	36
101	PP12V_S0_BLC (MAKE_BASE=TRUE)	PP12V_S0_BLC_FET	75
		=PP12V_S0_BLC	74
101	PP12V_S0_FBVDDQ (MAKE_BASE=TRUE)	PP12V_S0_SNS_FBVDDQ	50
		=PP12V_S0_REG_FBVDDQ	68
101	PP5V_S0 (MAKE_BASE=TRUE)	PP5V_S0_FET	75
		=PP5V_S0_AUDIO	54 61
		=PP5V_S0_BLC	74
		=PP5V_S0_ISENSE	50
		=PP5V_S0_LPCPLUS	48
		=PP5V_S0_REG_CPUVCC_S0	63 64 65
		=PP5V_S0_REG_FBVDDQ	68
		=PP5V_S0_REG_P1V05	68
		=PP5V_S0_HDD	36
		=PP5V_S0_VRD	69
101	PPHDD_S0 (MAKE_BASE=TRUE)	PP5V_S0_HDD_FET	36
		=PPHDD_S0_SNS_R	50
101	PP5V_S0_HDD (MAKE_BASE=TRUE)	PPHDD_S0_SNS	50
		=PP5V_S0_HDD_PWR	36
101	PP3V3_S0 (MAKE_BASE=TRUE)	PP3V3_S0_FET	75
		=PP3V3_S0_GPU_IFPX_PLLVDD	85
		=PP3V3_S0_GPU_MISC	85
		=PP3V3_S0_GPU_VDD33	85
		=PP3V3_S0_AUDIO	40 54 56 57 60
		=PP3V3_S0_AUDIO_DIG	58
		=PP3V3_S0_BLC	72
		=PP3V3_S0_DP	33 42 49
		=PP3V3_S0_ENET	37
		=PP3V3_S0_FAN	53
		=PP3V3_S0_GPU	69 85
		=PP3V3_S0_INTDPMUX	43
		=PP3V3_S0_LED	3
		=PP3V3_S0_LED_SATA	35
		=PP3V3_S0_MEM_A_SPD	23 24
		=PP3V3_S0_MEM_B_SPD	25 26
		=PP3V3_S0_P3V3TBTFET	30
		=PP3V3_S0_PCH	19
		=PP3V3_S0_PCH_VCC3_3_GPIO	11 12 13 14 15 17
		=PP3V3_S0_PCH_VCC3_3_THRM	15 17
		=PP3V3_S0_PCH_VCCCLK3_3	15 17
		=PP3V3_S0_PCH_VCC3_3_HVCMOS	15 17
		=PP3V3_S0_PCH_VCC_FUSE	15 17
		=PP3V3_S0_PWRCTL	75
		=PP3V3_S0_RSTBUF	20
		=PP3V3_S0_SDCARD	39
		=PP3V3_S0_SENSE	36 50 51 52
		=PP3V3_S0_SMBUS	49
		=PP3V3_S0_SMBUS_SMC_0	49
		=PP3V3_S0_SMBUS_SMC_1	49
		=PP3V3_S0_SMBUS_SMC_3	49
		=PP3V3_S0_SMC	47 84
		=PP3V3_S0_TBTPWRCTL	30
		=PP3V3_S0_VRD	62 63 68 69
		=PP3V3_S0_PCH_GPIO	30
		=PP3V3_S0_PCH_VCC3_3_USB	15 17
		=PPSSD_S0_SNS_R	51
101	PPSSD_S0 (MAKE_BASE=TRUE)	PPSSD_S0_SNS	51
		=PP3V3_S0_SSD	35
99	PP1V5_S0 (MAKE_BASE=TRUE)	PP1V5_S0_FET	75
		=PP1V5_S0_SNS_R	51
99	PP1V5_S0_PCH (MAKE_BASE=TRUE)	PP1V5_S0_SNS	51
		=PP1V5_S0_CPU_MEM	6 8 10
		=PP1V5_S0_AUD_DIG	54
		=PP1V5_S0_PCH_VCCVRM	17
		=PP1V5_S0_PCH_RCOMP	12 13
		=PP1V5_S0_PCH_SATA	11
		=PP1V5_S0_PCH_CLK	11 19
		=PP1V5_S0_DP	43
99	PPDDRVTT_S0 (MAKE_BASE=TRUE)	PPDDRVTT_S0_LDO	66
		=PPDDRVTT_S0_CLAMP	21
		=PPDDRVTT_S0_MEM_A	23 24
		=PPDDRVTT_S0_MEM_B	25 26
100	PPCPUVCC_S0_CPU (MAKE_BASE=TRUE)	PPCPUVCC_S0_REG	64 65
		=PPCPUVCC_S0_CPU	6 8 10 50 63

GPU Rails (S0)

Enabled when system is in run

105	PPVCORE_S0_GPU (MAKE_BASE=TRUE)	PPGPUCORE_S0_REG	70 71
		=PPVCORE_S0_GPU	85
		=PPGPUCORE_S0_SNS	50
105	PPFBVDDQ_S0_GPU (MAKE_BASE=TRUE)	PP1V5R1V35_S0_GPU_REG	68
		=PP1V35_S0_GPU_FBVDDQ	85
99	PP1V05_S0 (MAKE_BASE=TRUE)	PP1V05_S0_REG	68
		=PP1V05_S0_P1V05TBTFET	30
		=PP1V05_S0_PCH_VCC	15 17
		=PP1V05_S0_PCH_VCCCLK_CLK100	15 17
		=PP1V05_S0_PCH_VCCASW	15 17
		=PP1V05_S0_PCH_VCC_CLK	17
		=PP1V05_S0_PCH_VCCIO_FDI	15 17
		=PP1V05_S0_PCH_VCCCLK_SSC	15 17
		=PP1V05_S0_PCH_VCCUSBPLL	15 17
		=PP1V05_S0_PCH_VCCIO	15 17
		=PP1V05_S0_PCH_VCCCLK_SSC100	15 17
		=PP1V05_S0_PCH_VCCCLK_CLK135	15 17
		=PP1V05_S0_PCH_VCCIO_USB2	15 17
		=PP1V05_S0_PCH_V_PROC_IO	14 15 17
		=PP1V05_S0_SNS	50
		=PP1V05_S0_SMC	47
		=PP1V05_S0_XDP	18
		=PP1V05_S0_GPU_IFPCD_IOVDD	85
		=PP1V05_S0_GPU_IFPEF_IOVDD	85
		=PP1V05_S0_GPU_PEX_IOVDD	85
		=PP1V05_S0_GPU_PEX_PLLVDD	85

Thunderbolt Rails (S0)

Enabled when Thunderbolt cable is plugged in

101	PP3V3_TBTLC (MAKE_BASE=TRUE)	=PP3V3_TBTLC_FET	30
		=PP3V3_TBT_PCH_GPIO	20
		=PP3V3_TBTLC_RTR	28 29 30
		=PPVDDIO_TBT_CLK	19
99 30	PP1V05_TBTLC (MAKE_BASE=TRUE)	=PP1V05_TBTLC_FET	30
		=PP1V05_TBTLC_RTR	29
99	PP1V05_TBTCIO (MAKE_BASE=TRUE)	=PP1V05_TBTCIO_FET	30
		=PP1V05_TBTCIO_RTR	29

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

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Power Connectors/Aliases

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PEG aliases

93 78 PEG_D2R_N<0..15> ═══ =PEG_D2R_N<15..0> 5
MAKE_BASE=TRUE

93 78 PEG_D2R_P<0..15> ═══ =PEG_D2R_P<15..0> 5
MAKE_BASE=TRUE

93 78 PEG_R2D_C_N<0..15> ═══ =PEG_R2D_C_N<15..0> 5
MAKE_BASE=TRUE

93 78 PEG_R2D_C_P<0..15> ═══ =PEG_R2D_C_P<15..0> 5
MAKE_BASE=TRUE

DDI/FDI ALIASES

I64

5 TP_DP_IG_B_MLN<0..3> ═══ NC_DP_IG_B_MLN<0..3>
MAKE_BASE=TRUE

5 TP_DP_IG_B_MLP<0..3> ═══ NC_DP_IG_B_MLP<0..3>
MAKE_BASE=TRUE

5 TP_DP_IG_C_MLN<0..3> ═══ NC_DP_IG_C_MLN<0..3>
MAKE_BASE=TRUE

5 TP_DP_IG_C_MLP<0..3> ═══ NC_DP_IG_C_MLP<0..3>
MAKE_BASE=TRUE

5 TP_DP_IG_D_MLN<0..3> ═══ NC_DP_IG_D_MLN<0..3>
MAKE_BASE=TRUE

5 TP_DP_IG_D_MLP<0..3> ═══ NC_DP_IG_D_MLP<0..3>
MAKE_BASE=TRUE

GPU ALIASES

84 78 GPU_RESET_L ═══ TP_GPU_RESET_L 20
MAKE_BASE=TRUE

MEMORY PGOOD

21 =PM_PGOOD_MEM_S0 ═══ PM_PGOOD_FET_REG_P1V5_S0 75 76
MAKE_BASE=TRUE

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

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Signal Aliases

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CPU Reserved

95 18 6 CPU_CFG<15..12> — TP_CPU_CFG<15..12>
MAKE_BASE=TRUE

CPU Memory

7 TP_MEM_A_DQS_N<8> — NC_MEM_A_DQSNX<8>
MAKE_BASE=TRUE NO_TEST=TRUE

7 TP_MEM_A_DQS_P<8> — NC_MEM_A_DQSPX<8>
MAKE_BASE=TRUE NO_TEST=TRUE

7 TP_MEM_B_DQS_N<8> — NC_MEM_B_DQSNX<8>
MAKE_BASE=TRUE NO_TEST=TRUE

7 TP_MEM_B_DQS_P<8> — NC_MEM_B_DQSPX<8>
MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCIe

11 TP_PCIE_CLK100M_PE4N — NC_PCIE_CLK100M_PE4NX
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCIE_CLK100M_PE4P — NC_PCIE_CLK100M_PE4PX
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCIE_CLK100M_PE5N — NC_PCIE_CLK100M_PE5NX
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCIE_CLK100M_PE5P — NC_PCIE_CLK100M_PE5PX
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCIE_CLK100M_PE7N — NC_PCIE_CLK100M_PE7NX
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCIE_CLK100M_PE7P — NC_PCIE_CLK100M_PE7PX
MAKE_BASE=TRUE NO_TEST=TRUE

PCH Clocks

11 TP_PCH_GPIO64_CLKOUTFLEX0 — NC_PCH_GPIO64_CLKOUTFLEX0
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCH_GPIO65_CLKOUTFLEX1 — NC_PCH_GPIO65_CLKOUTFLEX1
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCH_GPIO66_CLKOUTFLEX2 — NC_PCH_GPIO66_CLKOUTFLEX2
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCH_GPIO67_CLKOUTFLEX3 — NC_PCH_GPIO67_CLKOUTFLEX3
MAKE_BASE=TRUE NO_TEST=TRUE

TP_ITPXDP_CLK100MP — ITPXDP_CLK100M_P 11 95
MAKE_BASE=TRUE NO_TEST=TRUE

TP_ITPXDP_CLK100MN — ITPXDP_CLK100M_N 11 95
MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCI

13 TP_LPC_DREQ0_L — NC_LPC_DREQ0_L
MAKE_BASE=TRUE NO_TEST=TRUE

PCH Miscellaneous

11 TP_HDA_SDIN1 — NC_HDA_SDIN1
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_HDA_SDIN2 — NC_HDA_SDIN2
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_HDA_SDIN3 — NC_HDA_SDIN3
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCI_CLK33M_OUT2 — NC_PCI_CLK33M_OUT2
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCI_CLK33M_OUT3 — NC_PCI_CLK33M_OUT3
MAKE_BASE=TRUE NO_TEST=TRUE

POWER SEQUENCING

76 PM_EN_FET_P1V35_S0 — NC_PM_EN_FET_P1V35_S0
MAKE_BASE=TRUE NO_TEST=TRUE

76 PM_PGOOD_FET_P1V35_S0 — NC_PGOOD_FET_P1V35_S0
MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

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Unused Signal Aliases

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J17 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA_TBT	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.185 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	ISL5,ISL8	Y	0.205 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.220 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.150 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	ISL5,ISL8	Y	0.165 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.130 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	ISL5,ISL8	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.155 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.115 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	ISL5,ISL8	Y	0.126 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.090 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	ISL5,ISL8	Y	0.100 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	ISL5,ISL8	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.171 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.085 MM	=STANDARD	0.150 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.136 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.141 MM	0.085 MM	=STANDARD	0.185 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.121 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.109 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.086 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.085 MM	=STANDARD	0.230 MM	0.1 MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1X_DIELECTRIC	ISL3,ISL10	0.101 MM	?
1X_DIELECTRIC	*	0.076 MM	?

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_ISO	*	=STANDARD	8000
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

GENERIC

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GENERIC_ISO	*	=1:1_SPACING	?

Board Stack-up

FINISHED BOARD THICKNESS: 1.94 MM

Top	Signal	0.5 oz (Cu plated)	
	Prepreg	0.071 MM	
2	Plane	1 oz	
	Core	0.101 MM	
3	Signal	0.5 oz	
	Prepreg	0.115 MM	
4	Plane	1 oz	
	Core	0.076 MM	
5	Signal	0.5 oz	
	Prepreg	0.380 MM	
6	Plane	1 oz	
	Core	0.076 MM	
7	Plane	1 oz	
	Prepreg	0.380 MM	
8	Signal	0.5 oz	
	Core	0.076 MM	
9	Plane	1 oz	
	Prepreg	0.115 MM	
10	Signal	0.5 oz	
	Core	0.101 MM	
11	Plane	1 oz	
	Prepreg	0.071 MM	
Btm	Signal	0.5 oz (Cu plated)	

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

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DDR3

DDR3-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
DDR_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
DDR_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
DDR_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM
DDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
DDR_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF
DDR_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

Minimum diff spacing is 4 mil
Table 4-5, Intel Doc# 486712

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
POWER_DDR_P4MM	*	Y	0.400 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_DDR	*	POWER_DDR_P4MM
DDR_CLK_PHY	*	DDR_68D
DDR_CTRL_PHY	*	DDR_39S
DDR_CMD_PHY	*	DDR_34S
DDR_DQ_PHY	*	DDR_42S
DDR_DQS_PHY	*	DDR_42S_D
DDR_COMP_PHY	*	DDR_COMP

DDR3 Power-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_DDR	*	=2:1_SPACING	?

DDR3-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DDR_CLK_ISO	*	=5:1_SPACING	?
DDR_CTRL_ISO	*	=3.5:1_SPACING	?
DDR_CTRL2CTRL	*	=2.5:1_SPACING	?
DDR_CMD_ISO	*	=3.5:1_SPACING	?
DDR_CMD2CMD	*	=2:1_SPACING	?
DDR_DATA_ISO	*	=3:1_SPACING	?
DDR_DQ2DQ	*	=2:1_SPACING	900
DDR_DQ2DQS	*	=3:1_SPACING	?
DDR_BL2BL	*	=3:1_SPACING	?
DDR_CH2CH	*	=6.5:1_SPACING	?
DDR_COMP_ISO	*	0.381 MM	?

Main Segment Min Spacing Rules (mils) (Shark Bay PDG, Intel Doc# 486712)

Table	Trace	Design	Iso	Design	Comments
4-2	4	(diff)	15	19.69	CLK trace spacing controlled by =68_OHM_DIFF
4-3	8	9.84	12	13.78	
4-4	6	7.87	12	13.78	
4-5	8.5	7.87	12	11.81	DQ or DQS to other signals not in the same bytelane (but not ch)
					DQ to DQ in the same bytelane of the same channel
			10	11.81	DQ to DQS in the same bytelane of the same channel
			12	11.81	DQ or DQS in different bytelanes of the same channel
			25	25.59	DQ or DQS in different channels
			-	25.59	DDR3 to any other signal not DDR3

Constraints

Clocks: CK[3:0], CK#[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CLK	*	*	DDR_CLK_ISO

Control: CS#[3:0], CKE[3:0], ODT[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CTRL	*	*	DDR_CTRL_ISO
DDR_CTRL	DDR_CTRL	*	DDR_CTRL2CTRL

Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CMD	*	*	DDR_CMD_ISO
DDR_CMD	DDR_CMD	*	DDR_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_COMP	*	*	DDR_COMP_ISO

Data: DQS[7:0], DQS#[7:0], DQ[63:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
DDR_A_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_A_DQS*	*	*	DDR_DATA_ISO	
DDR_B_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_B_DQS*	*	*	DDR_DATA_ISO	
DDR_*_DQ_BYTE*	=SAME	*	DDR_DQ2DQ	See Note (3)
DDR_A_DQ_BYTE*	DDR_A_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_A_DQ_BYTE*	DDR_A_DQ_BYTE*	*	DDR_BL2BL	See Note (3)
DDR_B_DQ_BYTE*	DDR_B_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_B_DQ_BYTE*	DDR_B_DQ_BYTE*	*	DDR_BL2BL	
DDR_A_*	DDR_B_*	*	DDR_CH2CH	See Note (2)

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME to win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

DDR3

Electrical Contraint Set	Physical	Spacing		
Channel A				
T17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<1..0>	? 23
T17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<1..0>	? 23
T25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<3..2>	? 24
T25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<3..2>	? 24
T18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<1..0>	? 23
T18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<1..0>	? 23
T18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<1..0>	? 23
T24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<3..2>	? 24
T24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<3..2>	? 24
T24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<3..2>	? 24
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_A<15..0>	? 23 24
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_BA<2..0>	? 23 24
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_RAS_L	? 23 24
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_CAS_L	? 23 24
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_WE_L	? 23 24
T18 DDR_A_DQ_BYTE0	DDR_DQ_PHY	DDR_A_DQ_BYTE0	MEM_A_DQ<7..0>	? 27
T18 DDR_A_DQ_BYTE1	DDR_DQ_PHY	DDR_A_DQ_BYTE1	MEM_A_DQ<15..8>	? 27
T19 DDR_A_DQ_BYTE2	DDR_DQ_PHY	DDR_A_DQ_BYTE2	MEM_A_DQ<23..16>	? 27
T19 DDR_A_DQ_BYTE3	DDR_DQ_PHY	DDR_A_DQ_BYTE3	MEM_A_DQ<31..24>	? 27
T19 DDR_A_DQ_BYTE4	DDR_DQ_PHY	DDR_A_DQ_BYTE4	MEM_A_DQ<39..32>	? 27
T19 DDR_A_DQ_BYTE5	DDR_DQ_PHY	DDR_A_DQ_BYTE5	MEM_A_DQ<47..40>	? 27
T19 DDR_A_DQ_BYTE6	DDR_DQ_PHY	DDR_A_DQ_BYTE6	MEM_A_DQ<55..48>	? 27
T19 DDR_A_DQ_BYTE7	DDR_DQ_PHY	DDR_A_DQ_BYTE7	MEM_A_DQ<63..56>	? 27
T19 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_P<0>	? 27
T19 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_N<0>	? 27
T19 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_P<1>	? 27
T19 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_N<1>	? 27
T20 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_P<2>	? 27
T20 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_N<2>	? 27
T20 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_P<3>	? 27
T20 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_N<3>	? 27
T20 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_P<4>	? 27
T20 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_N<4>	? 27
T20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_P<5>	? 27
T20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_N<5>	? 27
T20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_P<6>	? 27
T20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_N<6>	? 27
T21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_P<7>	? 27
T21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_N<7>	? 27
Channel B				
T21 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<1..0>	? 25
T21 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<1..0>	? 25
T25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<3..2>	? 26
T25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<3..2>	? 26
T21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<1..0>	? 25
T21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<1..0>	? 25
T21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<1..0>	? 25
T25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<3..2>	? 26
T25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<3..2>	? 26
T25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<3..2>	? 26
T21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_A<15..0>	? 25 26
T21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_BA<2..0>	? 25 26
T21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_RAS_L	? 25 26
T22 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_CAS_L	? 25 26
T22 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_WE_L	? 25 26
T22 DDR_B_DQ_BYTE0	DDR_DQ_PHY	DDR_B_DQ_BYTE0	MEM_B_DQ<7..0>	? 27
T22 DDR_B_DQ_BYTE1	DDR_DQ_PHY	DDR_B_DQ_BYTE1	MEM_B_DQ<15..8>	? 27
T22 DDR_B_DQ_BYTE2	DDR_DQ_PHY	DDR_B_DQ_BYTE2	MEM_B_DQ<23..16>	? 27
T22 DDR_B_DQ_BYTE3	DDR_DQ_PHY	DDR_B_DQ_BYTE3	MEM_B_DQ<31..24>	? 27
T22 DDR_B_DQ_BYTE4	DDR_DQ_PHY	DDR_B_DQ_BYTE4	MEM_B_DQ<39..32>	? 27
T22 DDR_B_DQ_BYTE5	DDR_DQ_PHY	DDR_B_DQ_BYTE5	MEM_B_DQ<47..40>	? 27
T22 DDR_B_DQ_BYTE6	DDR_DQ_PHY	DDR_B_DQ_BYTE6	MEM_B_DQ<55..48>	? 27
T22 DDR_B_DQ_BYTE7	DDR_DQ_PHY	DDR_B_DQ_BYTE7	MEM_B_DQ<63..56>	? 27
T23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_P<0>	? 27
T23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_N<0>	? 27
T23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_P<1>	? 27
T23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_N<1>	? 27
T23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_P<2>	? 27
T23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_N<2>	? 27
T23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_P<3>	? 27
T23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_N<3>	? 27
T23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_P<4>	? 27
T23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_N<4>	? 27
T24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_P<5>	? 27
T24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_N<5>	? 27
T24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_P<6>	? 27
T24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_N<6>	? 27
T24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_P<7>	? 27
T24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_N<7>	? 27
Reset				
T24	DDR_50S		MEM_RESET_L	21 23 24 25 26
SM COMP				
T25	DDR_COMP_PHY	DDR_COMP	CPU_SM_RCOMP<0..2>	6

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PCI Express/DMI

PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
PCIE_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE3_PHY	*	PCIE_80D
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	PCIE_COMP

PCIe and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIe. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=4:1_SPACING	?

Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO
PEG_R2D	PEG_R2D	*	PEG_SAME_DIR
PEG_D2R	PEG_D2R	*	PEG_SAME_DIR
PEG_D2R	PEG_R2D	*	PEG_ALT_DIR
PEG_D2R	*	*	PEG_ISO
PEG_R2D	*	*	PEG_ISO

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PEG_SAME_DIR	*	=3.5X_DIELECTRIC	?
PEG_ALT_DIR	*	=7X_DIELECTRIC	?
PEG_ISO	*	=4:1_SPACING	?

PEG Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	80	16	15.75	PCIe Gen3. Allow looser spacing for same direction on stripline per Anil

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
x16 Graphics				
R44P	PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<15> 78
R44N	PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<15> 78
R44P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<15> 78 88
R44N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<15> 78 88
R44P	PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<15> 78 88
R44N	PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<15> 78 88
R44P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<15> 78
R44N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<15> 78
R43P	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<14> 78
R43N	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<14> 78
R43P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<14> 78 88
R43N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<14> 78 88
R43P	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<14> 78 88
R43N	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<14> 78 88
R43P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<14> 78
R43N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<14> 78
R45P	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<13> 78
R45N	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<13> 78
R45P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<13> 78 88
R46N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<13> 78 88
R45P	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<13> 78 88
R46N	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<13> 78 88
R46P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<13> 78
R46N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<13> 78
R46P	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<12> 78
R46N	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<12> 78
R46P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<12> 78 88
R44N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<12> 78 88
R44P	PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<12> 78 88
R47N	PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<12> 78 88
R46P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<12> 78
R47N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<12> 78
R47P	PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<11> 78
R47N	PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<11> 78
R47P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<11> 78 88
R47N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<11> 78 88
R47P	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<11> 78 88
R47N	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<11> 78 88
R47P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<11> 78
R47N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<11> 78
R48P	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<10> 78
R48N	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<10> 78
R48P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<10> 78 88
R48N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<10> 78 88
R48P	PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<10> 78 88
R48N	PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<10> 78 88
R48P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<10> 78
R48N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<10> 78
R48P	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<9> 78
R48N	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<9> 78
R49P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<9> 78 88
R49N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<9> 78 88
R49P	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<9> 78 88
R49N	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<9> 78 88
R49P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<9> 78
R49N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<9> 78
R50P	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<8> 78
R50N	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<8> 78
R49P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<8> 78 88
R49N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<8> 78 88
R50P	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<8> 78 88
R50N	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<8> 78 88
R50P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<8> 78
R50N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<8> 78

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
x16 Graphics				
T45P	PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<7> 78
T45N	PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<7> 78
T45P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<7> 78 88
T45N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<7> 78 88
T46P	PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<7> 78 88
T46N	PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<7> 78 88
T45P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<7> 78
T45N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<7> 78
T43P	PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<6> 78
T43N	PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<6> 78
T43P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<6> 78 88
T43N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<6> 78 88
T44P	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<6> 78 88
T44N	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<6> 78 88
T43P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<6> 78
T43N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<6> 78
T52P	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<5> 78
T52N	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<5> 78
T52P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<5> 78 88
T52N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<5> 78 88
T52P	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<5> 78 88
T52N	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<5> 78 88
T52P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<5> 78
T52N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<5> 78
T53P	PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<4> 78
T53N	PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<4> 78
T53P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<4> 78 88
T53N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<4> 78 88
T54P	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<4> 78 88
T54N	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<4> 78 88
T53P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<4> 78
T53N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<4> 78
T55P	PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<3> 78
T55N	PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<3> 78
T55P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<3> 78 88
T55N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<3> 78 88
T56P	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<3> 78 88
T56N	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<3> 78 88
T55P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<3> 78
T55N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<3> 78
T58P	PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<2> 78
T58N	PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<2> 78
T57P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<2> 78 88
T57N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<2> 78 88
T59P	PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<2> 78 88
T59N	PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<2> 78 88
T58P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<2> 78
T58N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<2> 78
T60P	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<1> 78
T60N	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<1> 78
T60P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<1> 78 88
T60N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<1> 78 88
T59P	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<1> 78 88
T59N	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<1> 78 88
T59P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<1> 78
T59N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<1> 78
T56P	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<0> 78
T56N	PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<0> 78
T61P		PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<0> 78 88
T61N		PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<0> 78 88
T56P	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<0> 78 88
T56N	PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<0> 78 88
T61P		PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<0> 78
T61N		PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<0> 78
CPU PCIe Clocks				
T65P	PEG_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_P 11 78
T65N	PEG_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_N 11 78
CPU PCIe Compensation				
T67P		COMP_PCIE_PHY	COMP_PCIE	CPU_PEG_RCOMP 5
CPU eDP Compensation				
T67N		COMP_PCIE_PHY	COMP_PCIE	CPU_EDP_RCOMP 5

SYNC_MASTER=J17_NICK SYNC_DATE=12/14/2012

PAGE TITLE: CPU PCIe Constraints

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Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_85D
COMP_DMI_PHY	*	DMI_COMP

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_SAME_DIR	*	=3.5X_DIELECTRIC	?
PCIE_ALT_DIR	*	=7X_DIELECTRIC	?
PCIE_ISO	*	=4:1_SPACING	?

TBT x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_TBT_R2D	PCIE_TBT_R2D	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_D2R	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_R2D	*	PCIE_ALT_DIR
PCIE_TBT_D2R	*	*	PCIE_ISO
PCIE_TBT_R2D	*	*	PCIE_ISO

PCH x1 PCIE Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO

DMI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
DMI_SAME_DIR	*	=4X_DIELECTRIC	?
DMI_ALT_DIR	*	=5X_DIELECTRIC	?
DMI_ISO	*	=4X_DIELECTRIC	?

DMI x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_N2S	DMI_N2S	*	DMI_SAME_DIR
DMI_S2N	DMI_S2N	*	DMI_SAME_DIR
DMI_N2S	DMI_S2N	*	DMI_ALT_DIR
DMI_N2S	*	*	DMI_ISO
DMI_S2N	*	*	DMI_ISO

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DMI_COMP	*	Y	0.2032 MM	0.2032 MM	3 MM	=STANDARD	=STANDARD

PCIe (PCH)

Electrical Contraint Set	Physical	Spacing		
x4 Thunderbolt				
B132 PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_P<3..0>	28
B133 PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_N<3..0>	28
B134	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_P<3..0>	13 28
B135	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_N<3..0>	13 28
B136 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_P<3..0>	13 28
B137 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_N<3..0>	13 28
B138	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_P<3..0>	28
B139	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_N<3..0>	28
B140 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
B141 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
x1 AirPort				
B142 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_P	34
B143 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_N	34
B144	PCIE_PHY	PCIE	PCIE_AP_R2D_C_P	13 34
B145	PCIE_PHY	PCIE	PCIE_AP_R2D_C_N	13 34
B146 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_P	13 34
B147 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_N	13 34
B148 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_P	11 34
B149 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_N	11 34
x1 Caesar IV				
B150 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_P	37
B151 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_N	37
B152	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_P	13 37
B153	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_N	13 37
B154 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_P	13 37
B155 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_N	13 37
B156	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_P	37
B157	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_N	37
B158 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_P	11 37
B159 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_N	11 37
x2 SSD				
B160 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_P	11 35
B161 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_N	11 35
PCH PCIE Compensation				
B170	COMP_DMI_PHY	COMP_PCIE	PCH_PCIE_RCOMP	13

DMI

Electrical Contraint Set	Physical	Spacing		
DMI				
B162 DMI_N2S	PCIE_PHY	DMI_N2S	DMI_N2S_P<3..0>	5 12
B163 DMI_N2S	PCIE_PHY	DMI_N2S	DMI_N2S_N<3..0>	5 12
B164 DMI_S2N	PCIE_PHY	DMI_S2N	DMI_S2N_P<3..0>	5 12
B165 DMI_S2N	PCIE_PHY	DMI_S2N	DMI_S2N_N<3..0>	5 12
B166 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_P	6 11
B167 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_N	6 11
DMI Compensation				
B171	COMP_DMI_PHY	COMP_PCIE	PCH_DMI_RCOMP	12

CPU DP REF CLK

Electrical Contraint Set	Physical	Spacing		
CPU DP REF CLK				
B172 CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
B173 CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
B174 CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
B175 CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11

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SATA

SATA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SATA_PHY	*	SATA_85D
COMP_SATA_PHY	*	SATA_50S
SATA_PHY_90	*	SATA_90D

SATA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	*	=6:1_SPACING	?
COMP_SATA_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
COMP_SATA	*	*	COMP_SATA_ISO

SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
15.2.1	90	95	20	23.62	SATA Gen2, SATA Gen3

SATA Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
15-3	50	50	15	15.75	SATA Gen2, SATA Gen3

FDI

FDI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FDI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
COMP_FDI	*	Y	0.25 MM	0.25 MM	3 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FDI_SE_PHY	*	FDI_50S
COMP_FDI_PHY	*	COMP_FDI

FDI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FDI_ISO	*	=3:1_SPACING	?
COMP_FDI_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FDI	*	*	FDI_ISO
COMP_FDI	*	*	COMP_FDI_ISO

FDI Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Table	Imp	Design	Iso	Design	Comments
6-1/6-2	85	85	12	11.81	FDI main length

FDI Compensation Rules (mils)

Table	Trace	Design	Iso	Design	Comments
6-4	10	11.81	-	15.75	Using PCIe guidelines

XDP

XDP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
XDP_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
XDP_PHY	*	XDP_55S

XDP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XDP_ISO	*	=2:1_SPACING	?
CLK_JTAG_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XDP	*	*	XDP_ISO
CLK_JTAG	*	*	CLK_JTAG_ISO

Desktop Debug Design Guide (Intel Doc# 430883)

Section	Imp	Design	Iso	Design	Comments
1.5	45-65	55	-	15.75	Isolation is for JTAG clocks. All signals default are 50 Ohm SE.

SATA

Electrical Contraint Set	Physical	Spacing		
PCH SATA Port 0 (HDD)				
SATA_R2D	SATA_PHY_90	SATA	SATA_HDD_R2D_P	35
SATA_R2D	SATA_PHY_90	SATA	SATA_HDD_R2D_N	35
	SATA_PHY_90	SATA	SATA_HDD_R2D_C_P	11 35
	SATA_PHY_90	SATA	SATA_HDD_R2D_C_N	11 35
SATA_D2R	SATA_PHY_90	SATA	SATA_HDD_D2R_P	11 35
SATA_D2R	SATA_PHY_90	SATA	SATA_HDD_D2R_N	11 35
	SATA_PHY_90	SATA	SATA_HDD_D2R_C_P	35
	SATA_PHY_90	SATA	SATA_HDD_D2R_C_N	35
PCH SATA Port 1 (SSD)				
SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_P<0..1>	11 35
SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_N<0..1>	11 35
SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_C_P<0..1>	35
SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_C_N<0..1>	35
SATA_SSD_D2R	SATA_PHY	SATA	SSD_D2R_P<0..1>	11 35
SATA_SSD_D2R	SATA_PHY	SATA	SSD_D2R_N<0..1>	11 35
PCH SATA Compensation				
	COMP_SATA_PHY	COMP_SATA	PCH_SATA_RCOMP	11

FDI

Electrical Contraint Set	Physical	Spacing		
FDI				
	FDI_SE_PHY	FDI	FDI_CSYNC	5 12
	FDI_SE_PHY	FDI	FDI_INT	5 12
FDI Compensation				
	COMP_FDI_PHY	COMP_FDI	PCH_FDI_RCOMP	12

XDP

Electrical Contraint Set	Physical	Spacing		
CPU XDP				
	XDP_PHY	XDP	XDP_BPM_L<7..0>	6 18
	XDP_PHY	XDP	CPU_CFG<17..0>	6 18 89
TTP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_P	
TTP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_N	
	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_P	11 89
	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_N	11 89
	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_P	
	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_N	
	XDP_PHY	CLK_JTAG	XDP_CPU_TCK	6 18
	XDP_PHY	XDP	XDP_CPU_TMS	6 18
	XDP_PHY	XDP	XDP_CPU_TDI	6 18
	XDP_PHY	XDP	XDP_CPU_TDO	6 18
PCH XDP				
	XDP_PHY	CLK_JTAG	XDP_PCH_TCK	11 18
	XDP_PHY	XDP	XDP_PCH_TMS	11 18
	XDP_PHY	XDP	XDP_PCH_TDI	11 18
	XDP_PHY	XDP	XDP_PCH_TDO	11 18

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PCH

PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	=2:1_SPACING	?

PCI

PCI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCI	*	=2:1_SPACING	?

LPC

LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5:1_SPACING	?
CLK_LPC	*	=2:1_SPACING	?

HDA

HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

Crystal

Crystal-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

SPI

SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=2:1_SPACING	?

PCI

Electrical Contraint Set	Physical	Spacing		
PCI Clock				
B33	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIIN	11 19
B32	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIOUT	11 19

LPC

Electrical Contraint Set	Physical	Spacing		
LPC				
B32	LPC_55S	LPC	LPC_AD<3..0>	13 46 48
B33	LPC_55S	LPC	LPC_AD_R<3..0>	13
B33	LPC_55S	LPC	LPC_FRAME_L	13 46 48
B33	LPC_55S	LPC	LPC_FRAME_R_L	13
LPC Clocks				
B33	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	19 48
B34	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	11 19
B34	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	19 46
B34	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	11 19

PCH Clocks

Electrical Contraint Set	Physical	Spacing		
PCH Reference Clock				
B18	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_SB	11 19
A40	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_SB_R	11
PCH RTC 32K				
B44	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	11 19
B43	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	11 19
B52	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R	19
SMC 32K				
B26	CLK_PCH_55S	CLK_PCH	PM_CLK32K_SUSCLK_R	12 47
B50	CLK_PCH_55S	CLK_PCH	SMC_CLK32K	46 47

25 MHz Reference Clocks

Electrical Contraint Set	Physical	Spacing		
25M Reference Crystal				
B52	CLK_XTAL	XTAL	SYSCLK_CLK25M_X1	19
B50	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2	19
B51	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2_R	19
25M Reference Clocks				
B16	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET	19 37
B16	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET_R	19
B18	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT	19 28
B18	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT_R	28

HDA

Electrical Contraint Set	Physical	Spacing		
HDA				
B35	HDA_55S	HDA	HDA_BIT_CLK	11 54
B36	HDA_55S	HDA	HDA_BIT_CLK_R	11
B36	HDA_55S	HDA	HDA_RST_L	11 54
B40	HDA_55S	HDA	HDA_RST_R_L	11
B46	HDA_55S	HDA	HDA_SDOUT	11 54
B46	HDA_55S	HDA	HDA_SDOUT_R	11 19
B46	HDA_55S	HDA	HDA_SYNC	11 54
B46	HDA_55S	HDA	HDA_SYNC_R	11
B46	HDA_55S	HDA	HDA_SDIN0	11 54
B46	HDA_55S	HDA	AUD_SDI_R	54
SPDIF				
B37		HDA	AUD_SPDIF_CHIP	54
B37		HDA	AUD_SPDIF_OUT	54 58

SPI Bootrom

Electrical Contraint Set	Physical	Spacing		
SPI ROM				
B31	SPI_50S	SPI	SPI_CLK_R	13 48
B42	SPI_50S	SPI	SPI_CLK	48
B42	SPI_50S	SPI	SPI_ALT_CLK	48
A40	SPI_50S	SPI	SPI_SMC_CLK	46 48
A40	SPI_50S	SPI	SPI_MLB_CLK	48
B34	SPI_50S	SPI	SPI_CS0_R_L	13 48
B33	SPI_50S	SPI	SPI_CS0_L	48
A38	SPI_50S	SPI	SPI_ALT_CS_L	48
A40	SPI_50S	SPI	SPI_SMC_CS_L	46 48
B37	SPI_50S	SPI	SPI_MLB_CS_L	48
B39	SPI_50S	SPI	SPI_MOSI_R	13 48
A40	SPI_50S	SPI	SPI_MOSI	48
A40	SPI_50S	SPI	SPI_ALT_MOSI	48
A41	SPI_50S	SPI	SPI_SMC_MOSI	46 48
A41	SPI_50S	SPI	SPI_MLB_MOSI	48
A40	SPI_50S	SPI	SPI_MISO	13 48
A40	SPI_50S	SPI	SPI_ALT_MISO	48
A41	SPI_50S	SPI	SPI_SMC_MISO	46 48
A41	SPI_50S	SPI	SPI_MLB_MISO	48
A40	SPI_50S	SPI	SPIROM_USE_MLB	14 48

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USB

USB-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB2_PHY	*	USB_90D
USB3_PHY	*	USB_85D

USB-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2_ISO	*	=3:1_SPACING	?
USB2_ISO	TOP,BOTTOM	=3:1_SPACING	?
USB3_ISO	*	=5.5:1_SPACING	?
USB3_ISO	TOP,BOTTOM	=5.5:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB2	*	*	USB2_ISO
USB3	*	*	USB3_ISO

USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
12.2.1	90	90	12	11.81	USB 2.0
13.3.1	85	85	20	21.65	USB 3.0

Caesar IV (Ethernet/SD)

CIV-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_COMP_PHY	*	ENET_50S
ENET_DIFF_PHY	*	ENET_100D
SD_PHY	*	SD_50S
CIV_SPI	*	SPI_55S

CIV-specific Spacing Definitions

Ethernet

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF_ISO	*	=6:1_SPACING	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_TRANS_ISO	*	1.27 MM	?
COMP_ENET_ISO	*	=4:1_SPACING	?

SD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_ISO	*	=3:1_SPACING	?

Constraints

Ethernet

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

2 kV isolation

SD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SD	*	*	SD_ISO

Camera Processor-to-Camera Sensor I/F (SMIA/MIPI)

Camera Processor's SMIA Interface Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMIA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMIA_DIFF_PHY	*	SMIA_100D

Camera Processor's SMIA Interface Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMIA_DIFF_ISO	*	=6:1_SPACING	?
SMIA_DIFF2DIFF	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMIA_DIFF	*	*	SMIA_DIFF_ISO
SMIA_DIFF	SMIA_DIFF	*	SMIA_DIFF2DIFF

USB 3.0 and USB 2.0 Trixies Muxing

Electrical Contraint Set	Physical	Spacing	
External Port A (J4600)			
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_P
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_N
	USB3_PHY	USB3	USB3_EXTA_RX_F_P
	USB3_PHY	USB3	USB3_EXTA_RX_F_N
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_P
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_N
	USB3_PHY	USB3	USB3_EXTA_TX_F_P
	USB3_PHY	USB3	USB3_EXTA_TX_F_N
	USB3_PHY	USB3	USB3_EXTA_TX_C_P
	USB3_PHY	USB3	USB3_EXTA_TX_C_N
USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_EXTA_0_P
USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_EXTA_0_N
	USB2_PHY	USB2	USB2_EXTA_MUXED_P
	USB2_PHY	USB2	USB2_EXTA_MUXED_N
	USB2_PHY	USB2	USB2_EXTA_P
	USB2_PHY	USB2	USB2_EXTA_N
External Port B (J4610)			
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_P
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_N
	USB3_PHY	USB3	USB3_EXTB_RX_F_P
	USB3_PHY	USB3	USB3_EXTB_RX_F_N
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_P
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_N
	USB3_PHY	USB3	USB3_EXTB_TX_F_P
	USB3_PHY	USB3	USB3_EXTB_TX_F_N
	USB3_PHY	USB3	USB3_EXTB_TX_C_P
	USB3_PHY	USB3	USB3_EXTB_TX_C_N
USB2_CONN	USB2_PHY	USB2	USB_EXTB_8_P
USB2_CONN	USB2_PHY	USB2	USB_EXTB_8_N
	USB2_PHY	USB2	USB2_EXTB_P
	USB2_PHY	USB2	USB2_EXTB_N
External Port C (J4700)			
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_P
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_N
	USB3_PHY	USB3	USB3_EXTC_RX_F_P
	USB3_PHY	USB3	USB3_EXTC_RX_F_N
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_P
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_N
	USB3_PHY	USB3	USB3_EXTC_TX_F_P
	USB3_PHY	USB3	USB3_EXTC_TX_F_N
	USB3_PHY	USB3	USB3_EXTC_TX_C_P
	USB3_PHY	USB3	USB3_EXTC_TX_C_N
USB2_CONN	USB2_PHY	USB2	USB_EXTC_1_P
USB2_CONN	USB2_PHY	USB2	USB_EXTC_1_N
	USB2_PHY	USB2	USB2_EXTC_P
	USB2_PHY	USB2	USB2_EXTC_N
External Port D (J4710)			
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_P
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_N
	USB3_PHY	USB3	USB3_EXTD_RX_F_P
	USB3_PHY	USB3	USB3_EXTD_RX_F_N
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_P
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_N
	USB3_PHY	USB3	USB3_EXTD_TX_F_P
	USB3_PHY	USB3	USB3_EXTD_TX_F_N
	USB3_PHY	USB3	USB3_EXTD_TX_C_P
	USB3_PHY	USB3	USB3_EXTD_TX_C_N
USB2_CONN	USB2_PHY	USB2	USB_EXTD_9_P
USB2_CONN	USB2_PHY	USB2	USB_EXTD_9_N
	USB2_PHY	USB2	USB2_EXTD_P
	USB2_PHY	USB2	USB2_EXTD_N
Camera (J3510)			
USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_P
USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_N
PCH USB Compensation			
	PCH_55S	COMP_PCH	PCH_USB_RBIAS

RMH Love

Electrical Contraint Set	Physical	Spacing	
USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_P
USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_N
USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_MUX_P
USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_MUX_N

Et tu Brute?

Electrical Contraint Set	Physical	Spacing	
Ethernet			
ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_P<3..0>
ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_N<3..0>
	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_P<3..0>
	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_N<3..0>
		ENET_TRANS	ENETCONN_MCT0
		ENET_TRANS	ENETCONN_MCT1
		ENET_TRANS	ENETCONN_MCT2
		ENET_TRANS	ENETCONN_MCT3
		ENET_TRANS	ENETCONN_MCT_BS
	ENET_COMP_PHY	COMP_ENET	ENET_RDAC
SD			
SD_DATA	SD_PHY	SD	ENET_CR_DATA<7..0>
	SD_PHY	SD	SDCONN_DATA<7..0>
	SD_PHY	SD	SDCONN_DATA_R <7..0>
SD_CMD	SD_PHY	SD	ENET_SD_CMD
	SD_PHY	SD	SDCONN_CMD
	SD_PHY	SD	SDCONN_CMD_R
SD_CLK	SD_PHY	SD	ENET_SD_CLK
	SD_PHY	SD	SDCONN_CLK
	SD_PHY	SD	SDCONN_CLK_R
	SD_PHY	SD	ENET_MEDIA_SENSE
	SD_PHY	SD	ENET_SD_DETECT_L
CIV SPI			
	CIV_SPI	SPI	ENET_SCLK
	CIV_SPI	SPI	ENET_MISO
	CIV_SPI	SPI	ENET_MOSI
	CIV_SPI	SPI	ENET_CS_L

Camera Processor-Camera Sensor I/F

Electrical Contraint Set	Physical	Spacing	
SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_P
SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_N
SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_P
SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_N
	SPI_50S	SPI	CAM_SF_CLK
	SPI_50S	SPI	CAM_SF_CLK_R
	SPI_50S	SPI	CAM_SF_DIN
	SPI_50S	SPI	CAM_SF_DIN_R
	SPI_50S	SPI	CAM_SF_CS_L
	SPI_50S	SPI	CAM_SF_WP_L
	SPI_50S	SPI	CAM_SF_DOUT
	SPI_50S	SPI	CAM_SF_DOUT_R
	SMB_PHY	SMB	I2C_CAMSENSOR_SDA
	SMB_PHY	SMB	I2C_CAMSENSOR_SCL

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SMBus

SMBus-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_PHY	*	SMB_55S

SMBus-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB_ISO	*	=2x_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SMB_ISO

Sensor

Sensor-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_DIFF_PHY	*	1:1_DIFFPAIR

Sensor-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE_ISO	*	=1.5:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SENSE	*	*	SENSE_ISO
SENSE	POWER	*	PWR_P2MM
SENSE	GND	*	GND_P2MM

SMC Generic Control Line Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMC_ISO	*	=1:1_SPACING	?
SMC_3xISO	*	=3:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMC_CTRL	*	*	SMC_ISO
SMC_3XCTRL	*	*	SMC_3xISO

SMC Generic Control Line Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMC_GEN	*	SMC_50S

Current/Voltage Sense

Electrical Contraint Set	Physical	Spacing		
Common				
I3		SENSE	GND_SMC_AVSS	46 47 50 51
12V S5 (System Total)				
I4 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_P	50
I5 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_N	50
I6		SENSE	ISNS_P12VG3H_R	50 106
I7		SENSE	ISNS_P12VG3H	47 50
I8		SENSE	VSNS_P12VG3H	47 50
12V S0 (GPU Core)				
I22 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUCORE_P	50
I23 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUCORE_N	50
I24		SENSE	ISNS_P12VS0_GPUCORE_R	50
I25		SENSE	ISNS_P12VS0_GPUCORE	47 50
I26		SENSE	VSNS_P12VS0_GPUCORE	47 50
HDD				
I80 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_HDD_P	50
I82 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_HDD_N	50
I81		SENSE	ISNS_HDDS0_R	50
I83		SENSE	ISNS_HDDS0	47 50
I84		SENSE	VSNS_HDDS0	47 50
I125 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_HDD_P	50
I126 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_HDD_N	50
I127		SENSE	ISNS_P12VS0_HDD_R	50 106
I128		SENSE	ISNS_P12VS0_HDD	47 50
SSD				
I85 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_P	51
I87 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_N	51
I86		SENSE	ISNS_SSDS0_R	51
I88		SENSE	ISNS_SSDS0	47 51
I89		SENSE	VSNS_P3V3S5	47 51
GPU Core (alternate low side sense)				
I119 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_GPUCORE_P	
I120 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_GPUCORE_N	
I118		SENSE	ISNS_GPUCORE_ALT	47 50
I121		SENSE	ISNS_GPUCORE_FB	50 106
I122		SENSE	VSNS_GPUCORE_ALT	47 50
VDDQ S3 (DDR)				
I33 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_VDDQS3_DDR_P	51
I32 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_VDDQS3_DDR_N	51
I35		SENSE	ISNS_VDDQS3_DDR_R	51
I34		SENSE	ISNS_VDDQS3_DDR	47 51
I36		SENSE	VSNS_VDDQS3_DDR	47 51
VDDQ S0 (GPU FBVDDQ)				
I37 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_FBVDDQ_P	50
I38 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_FBVDDQ_N	50
I39		SENSE	ISNS_P12VS0_FBVDDQ_R	50 106
I40		SENSE	ISNS_P12VS0_FBVDDQ	47 50
CPU Core				
I42 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUVCC_P	
I43 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUVCC_N	
I44		SENSE	ISNS_CPUVCC_FB	50
I45		SENSE	ISNS_CPUVCC	47 50
I46		SENSE	VSNS_CPUVCC	47 50
PP1V05_S0_PCH				
I110		SENSE	VSNS_P1V05S0_PCH	47 50
PP1V5_S0				
I113 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P1V5S0_P	51
I114 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P1V5S0_N	51
I112		SENSE	ISNS_P1V5S0_R	51
I115		SENSE	ISNS_P1V5S0	47 51
I116		SENSE	VSNS_P1V5S0	47 51
Airport				
I102 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P3V3S4_AP_P	50
I103 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P3V3S4_AP_N	50
I104		SENSE	ISNS_P3V3S4_AP_R	50 106
I105		SENSE	ISNS_P3V3S4_AP	47 50

SMC

Electrical Contraint Set	Physical	Spacing		
SMC				
H1	CLK_XTAL	XTAL	SMC_XTAL	46 47
H2	CLK_XTAL	XTAL	SMC_EXTAL	46 47
H91	SMC_GEN	SMC_CTRL	SMC_LRESET_L	20 46
H90	SMC_GEN	SMC_CTRL	SMC_RUNTIME_SCI_L	14 46
H92	SMC_GEN	SMC_CTRL	SMC_WAKE_SCI_L	14 46
H93	SMC_GEN	SMC_CTRL	SMC_FAN_0_CTL	46 53
H94	SMC_GEN	SMC_CTRL	SMC_FAN_0_TACH	46 53
H95	CPU_ASYNC_PHY	CPU_ASYNC	SMC_PECI_L	46 47 106
H96	SMC_GEN	SMC_3XCTRL	CPU_PECI	6 14 46 47

SMBus

Electrical Contraint Set	Physical	Spacing		
SMC				
H10	SMB_PHY	SMB	SMBUS_SMC_0_S0_SCL	46 49
H9	SMB_PHY	SMB	SMBUS_SMC_0_S0_SDA	46 49
H11	SMB_PHY	SMB	SMBUS_SMC_1_S0_SCL	46 49
H12	SMB_PHY	SMB	SMBUS_SMC_1_S0_SDA	46 49
H13	SMB_PHY	SMB	SMBUS_SMC_2_S4_SCL	46 49
H14	SMB_PHY	SMB	SMBUS_SMC_2_S4_SDA	46 49
H15	SMB_PHY	SMB	SMBUS_SMC_3_SCL	46 49
H16	SMB_PHY	SMB	SMBUS_SMC_3_SDA	46 49
H19	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SCL	46 47
H20	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SDA	46 47
PCH				
H51	SMB_PHY	SMB	SMBUS_PCH_CLK	13 49
H52	SMB_PHY	SMB	SMBUS_PCH_DATA	13 49
H53	SMB_PHY	SMB	SML_PCH_0_CLK	13 49
H54	SMB_PHY	SMB	SML_PCH_0_DATA	13 49
Display TCon				
H55	SMB_PHY	SMB	SMB_DP_TCON_SCL	42 49
H56	SMB_PHY	SMB	SMB_DP_TCON_SDA	42 49

Temperature Sense

Electrical Contraint Set	Physical	Spacing		
EMC1414-1 (Production)				
H57 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_P	
H58 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_N	
H59 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_2_P	
H60 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_2_N	
H65 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_P	52 62
H66 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_N	52 62
H32	SNS_DIFF_PHY	SENSE	SNS_T1_3_P	
H24	SNS_DIFF_PHY	SENSE	SNS_T1_3_N	
TMP423 (Development)				
H57 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_P	
H58 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_N	
H62 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_P	
H70 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_N	
H61 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_SKIN_P	
H62 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_SKIN_N	
H71 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_P	
H72 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_N	
HDD Out-of-Band				
H13		SENSE	SMC_OOB1_D2R_L	36 46
H76		SENSE	SMC_OOB1_R2D_L	46 47
H16		SENSE	SMC_OOB1_D2R_R	36
SSD Out-of-Band				
H77		SENSE	SMC_OOB2_R2D_L	35 47
H78		SENSE	SMC_OOB2_D2R_L	35 47

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DC-DC

Power-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
GND_P5MM	*	Y	0.500 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
POWER_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_P6MM	*	Y	0.600 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_P5MM
GND	BGA	GND_P3MM
POWER	*	POWER_P6MM
POWER	BGA	POWER_P3MM
VR_CTL_PHY	*	POWER_P3MM
VR_CTL_PHY	BGA	STANDARD
VR_VID_PHY	*	POWER_50S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VR_DIDT_PHY	*	POWER_P6MM
VR_DIDT_PHY	BGA	STANDARD

Power-specific Spacing Definitions
Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_ISO	*	=STANDARD	?
GND_ISO	*	=STANDARD	?

Constraints
Power and Common

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	POWER_ISO
GND	*	*	GND_ISO

DC-DC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SWNODE_ISO	*	=8:1_SPACING	1000
SWNODE_SW2SW	*	=1:1_SPACING	?
SWNODE_SW2PWR	*	=2:1_SPACING	?
SWNODE_SW2GND	*	=2:1_SPACING	?

DC-DC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_SWITCH	*	*	SWNODE_ISO
VR_SWITCH	*	BGA	BGA_P1MM
VR_SWITCH	VR_SWITCH	*	SWNODE_SW2SW
VR_SWITCH	POWER	*	SWNODE_SW2PWR
VR_SWITCH	GND	*	SWNODE_SW2GND

DC-DC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_ISO	*	=3:1_SPACING	?
VR_VID_ISO	*	=4X_DIELECTRIC	?

DC-DC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CTL	*	*	VR_CTL_ISO
VR_VID	*	*	VR_VID_ISO

PCH/GPU/TBT 1.05V S0

Electrical Contraint Set		Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus								
I1		POWER	POWER	5V			REG_VCC_U7700	68
Local Ground								
I3		GND	GND	0V			AGND_P1V05S0	68
1.05V S0								
I5		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0	68
I4		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0_L	68
I7		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0	68
I6		VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P1V05S0_RC	68
I8		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0	68
I9		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0_R	68
I10		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P1V05S0	68
I12		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P1V05S0	68
I11		VR_CTL_PHY	VR_CTL				REG_P1V05S0_OCSET	68
I14		VR_CTL_PHY	VR_CTL				REG_P1V05S0_VO	68
I16	VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE				SNS_GPU_PEX_IOVDD_P	68 86
I17	VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE				SNS_GPU_PEX_IOVDD_N	68 86
I19			SENSE				REG_P1V05S0_FB	68
I18			SENSE				REG_P1V05S0_RTN	68
I21		VR_CTL_PHY	VR_CTL				REG_P1V05S0_SREF	68
I20		VR_CTL_PHY	VR_CTL				REG_P1V05S0_FSEL	68
Output Bus								
I22		POWER	POWER	1.05V			PP1V05_S0	87
FET Switched								
I23		POWER	POWER	1.05V			PP1V05_TBTLC	30 87
I66		POWER	POWER	1.05V			PP1V05_TBTCIO	87

VDDQ S3 (1.5V)/VTT S0

Physical		Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
I47	POWER	POWER	5V			REG_V5IN_U7300	66
Local Ground							
I44	GND	GND	0V			AGND_VDDQS3	66
VDDQ S3							
I45	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3	66
I43	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3_L	66
I46	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VDDQS3	66
I48	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VDDQS3_RC	66
I47	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3	66
I50	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3_R	66
I52	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_VDDQS3	66
I51	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_VDDQS3	66
I53	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VDDQSNS	66
I55	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VREF	66
I56	VR_CTL_PHY	VR_CTL				REG_VDDQS3_REFIN	66
I57	VR_CTL_PHY	VR_CTL				REG_VDDQS3_MODE	66
I58	VR_CTL_PHY	VR_CTL				REG_VDDQS3_TRIP	66
I59	VR_CTL_PHY	VR_CTL				LDO_DDRVTTS0_SNS	66
I61	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VTTREF	66
Output Bus							
I65	POWER	POWER	1.5V			PPVDDQ_S3	87
I62	POWER_DDR	POWER_DDR	0.75V			PPDDRVTT_S0	87
FET Switched							
I63	POWER	POWER	1.5V			PP1V5_S0	87
Sensed							
I64	POWER	POWER	1.5V			PPVDDQ_S3_DDR	87
I67	POWER	POWER	1.5V			PP1V5_S0_PCH	87

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CPU VCC Phases

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
H10	POWER	POWER	12V			PP12V_S0_CPUVCC_FLT — 63 64 65
H11	POWER	POWER	5V			REG_VCC_U7000 — 63
Local Ground						
H12	GND	GND	0V			AGND_CPU — 63 64 65
Phase 1						
H13	VR_CTL_PHY	VR_CTL				REG_TD_1 — 64
H14	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_1 — 63 64
H15	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_1_R — 63
H16	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_1 — 64
H17	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_1 — 64
H18	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUVCC_1_RC — 64
H19	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_1 — 64
H20	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_1 — 64
H21	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_1 — 64
H22	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_1 — 64
H23 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_1_P — 63 64
H24 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_1_N — 64
H25		SENSE				REG_ISENVCC_1_NR — 63 64
Phase 2						
H26	VR_CTL_PHY	VR_CTL				REG_TD_2 — 64
H27	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_2 — 63 64
H28	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_2_R — 63
H29	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_2 — 64
H30	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_2 — 64
H31	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUVCC_2_RC — 64
H32	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_2 — 64
H33	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_2 — 64
H34	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_2 — 64
H35	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_2 — 64
H36 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_2_P — 63 64
H37 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_2_N — 64
H38		SENSE				REG_ISENVCC_2_NR — 63 64
Phase 3						
H39	VR_CTL_PHY	VR_CTL				REG_TD_3 — 64
H40	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_3 — 63 64
H41	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_3_R — 63
H42	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_3 — 64
H43	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_3 — 64
H44	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUVCC_3_RC — 64
H45	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_3 — 64
H46	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_3 — 64
H47	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_3 — 64
H48	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_3 — 64
H49 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_3_P — 63 64
H50 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_3_N — 64
H51		SENSE				REG_ISENVCC_3_NR — 63 64
Phase 4						
H52	VR_CTL_PHY	VR_CTL				REG_TD_4 — 65
H53	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_4 — 63 65
H54	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_4_R — 63
H55	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_4 — 65
H56	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_4 — 65
H57	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUVCC_4_RC — 65
H58	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_4 — 65
H59	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_4 — 65
H60	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_4 — 65
H61	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_4 — 65
H62 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_4_P — 63 65
H63 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_4_N — 65
H64		SENSE				REG_ISENVCC_4_NR — 63 65

CPU VCC Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
ISL6372						
H102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_DVC — 63
H102	VR_CTL_PHY	VR_CTL				CPUVCC_DVC_RC — 63
H102	VR_CTL_PHY	VR_CTL				CPUVCC_FB_RC_2 — 63
H102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_COMP — 63
H102	VR_CTL_PHY	VR_CTL				CPUVCC_COMP_RC — 63
H102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FB — 63
H102	VR_CTL_PHY	VR_CTL				CPUVCC_FB_RC — 63
H103	VR_CTL_PHY	VR_CTL				CPUVCC_FB_R_1 — 63
H103	VR_CTL_PHY	VR_CTL				CPUVCC_FB_R_2 — 63
H103	VR_CTL_PHY	VR_CTL				CPUVCC_PSICOMP_RC — 63
H104	VR_CTL_PHY	VR_CTL				REG_CPUVCC_PSICOMP — 63
H104	VR_CTL_PHY	VR_CTL				REG_CPUVCC_HFCOMP — 63
H105 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_P — 8 63
H106 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_N — 9 63
H103	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_R_P — 63
H103	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_R_N — 63
H103	SNS_DIFF_PHY	SENSE	1.8V			SNS_VCC_XW_P — 63
H103	SNS_DIFF_PHY	SENSE	0V			SNS_VCC_XW_N — 63
H104		SENSE				REG_CPUVCC_VSEN — 63
H104		SENSE				REG_CPUVCC_RGND — 63
H104		SENSE				REG_CPUVCC_VIN — 63
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_IMON — 50 63
H105	VR_CTL_PHY	VR_CTL				CPUVCC_IMON_R — 63
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_TM — 63
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_IMX — 63
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_NPSI — 63
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FDVID — 63
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_TMX — 63
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_MEMVRSEL — 63
H104	VR_CTL_PHY	VR_CTL				REG_CPUVCC_RSET — 63
H106 CPU_VIDSCLK	VR_VID_PHY	VR_VID				CPU_VIDSCLK — 8 63
H106	VR_VID_PHY	VR_VID				CPU_VIDSCLK_R — 8
H106 CPU_VIDALERT_L	VR_VID_PHY	VR_VID				CPU_VIDALERT_L — 8 63
H106	VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L — 8
H106 CPU_VIDSOUT	VR_VID_PHY	VR_VID				CPU_VIDSOUT — 8 63
H106	VR_VID_PHY	VR_VID				CPU_VIDSOUT_R — 8
Output Bus						
H107	POWER	POWER	1.8V			PPCPUVCC_S0_CPU — 87

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3.3V S5/5V S4

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
B43	POWER	POWER	12V			REG_VIN_U7600	67
B125	POWER	POWER	5V			REG_VCC1_U7600	67
B125	POWER	POWER	5V			REG_VCC2_U7600	67
3.3V S5							
B849	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P3V3S5	67
B847	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5	67
B851	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P3V3S5_RC	67
B848	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P3V3S5	67
B850	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P3V3S5	67
B852	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P3V3S5	67
B107	VR_CTL_PHY	VR_CTL				REG_P3V3S5_ISEN	67
B107	VR_CTL_PHY	VR_CTL				REG_P3V3S5_OCSET	67
B113	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FSET	67
B108	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT	67
B107	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT_R	67
B107	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FB	67
5V S3							
B113	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P5VS4	67
B113	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4	67
B113	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P5VS4_RC	67
B114	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P5VS4	67
B114	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P5VS4	67
B114	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P5VS4	67
B114	VR_CTL_PHY	VR_CTL				REG_P5VS4_ISEN	67
B114	VR_CTL_PHY	VR_CTL				REG_P5VS4_OCSET	67
B115	VR_CTL_PHY	VR_CTL				REG_P5VS4_FSET	67
B114	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT	67
B114	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT_R	67
B114	VR_CTL_PHY	VR_CTL				REG_P5VS4_FB	67
Output Bus							
B115	POWER	POWER	5V			PP5V_S5	87
B115	POWER	POWER	5V			PP5V_S4	87
B114	POWER	POWER	3.3V			PP3V3_S5	87
FET Switched							
B123	POWER	POWER	5V			PP5V_S0	87
B121	POWER	POWER	3.3V			PP3V3_S4	87
B122	POWER	POWER	3.3V			PP3V3_S0	87
B145	POWER	POWER	3.3V			PP3V3_S0_SSD	
B121	POWER	POWER	3.3V			PP3V3_ENET	87
B121	POWER	POWER	3.3V			PP3V3_TBTLC	87
Sensed							
B145	POWER	POWER	3.3V			PPSSD_S0	87
B147	POWER	POWER	3.3V			PP3V3_S4_AP	87

3.42V G3H

	Physical	Spacing	Voltage	DIDT	NO_TEST		
3.42V G3H							
B146	POWER	VR_SWITCH	12V	TRUE		P3V42G3H_BOOST	62
B146	POWER	VR_SWITCH	12V	TRUE		P3V42G3H_SW	62
B146	VR_CTL_PHY	VR_CTL				P3V42G3H_FB	62
B146	VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_L	62
Output Bus							
B146	POWER	POWER	3.425V			PP3V42_G3H	87

3.3V G3

	Physical	Spacing	Voltage	DIDT	NO_TEST		
B149	POWER	POWER	3.3V			PP3V3_G3	87

HDD S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
FET Switched							
B150	POWER	POWER	5V			PPHDD_S0	87
Sensed							
B146	POWER	POWER	5V			PP5V_S0_HDD	87

12V

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
B146	POWER	POWER	12V			PP12V_ACDC	87
FET Switched							
B145	POWER	POWER	12V			PP12V_S5	87
B145	POWER	POWER	12V			PP12V_S0	87
B147	POWER	POWER	12V			PP12V_S0_BLC	87
B148	POWER	POWER	12V			PPHDD12_S0	87
Sensed							
B145	POWER	POWER	12V			PP12V_G3H	87
B147	POWER	POWER	12V			PP12V_G3H_P3V42	62
B145	POWER	POWER	12V			PP12V_S0_GPUCORE	87
B145	POWER	POWER	12V			PP12V_S0_FBVDDQ	87
B147	POWER	POWER	12V			PP12V_S0_HDD	87

Ground/Common

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Common							
B132	GND	GND	0V			GND	

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Thunderbolt

Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C	*	=2x_DIELECTRIC	?
TBT_SPI	*	=2x_DIELECTRIC	?
TBTDP	*	=5x_DIELECTRIC	?
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?
BGA_TBT_AREA	*	0.075MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_TBT	BGA_TBT_AREA

SOURCE: Bill Cornelius's T29 Routing Notes

DisplayPort

DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

Pairs should be within 100 mils of clock length.
Max length of DisplayPort traces: 12 inches

DisplayPort intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX channel intra-pair matching should be 5 ps. No relationship to other signals.

TBT IC Net Properties

Electrical Contraint Set	Physical	Spacing		
I651	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	28 83
I652	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	28 83
I653 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28
I654 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28
I655	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	28 83
I656	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	28 83
I657 DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	28
I658 DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	28
I659	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	28 83
I692	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	28 83
I693 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28
I694 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28
I695	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	28 83
I696	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	28 83
I697 DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	28
I698 DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	28
I680 DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_P<3..0>	43
I686 DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_N<3..0>	43
I681 DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	43
I687 DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	43
I682 DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_P	43
I683 DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_N	43
I650	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_P	43
I652	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_N	43
I632	TBT_I2C_55S	TBT_I2C	I2C_TBTRTR_SCL	28
I633	TBT_I2C_55S	TBT_I2C	I2C_TBTRTR_SDA	28
I634 TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	28
I635 TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	28
I636 TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	28
I638 TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	28

*: Only used on hosts supporting T29 video-in

DisplayPort

Electrical Contraint Set	Physical	Spacing		
Graphics Source				
I642 DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>	43 83
I643 DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>	43 83
I644 DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P	43 83
I645 DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N	43 83
I646	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_P	43
I647	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_N	43
Internal Panel				
I690	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_P<3..0>	43
I691	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_N<3..0>	43
I680 DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	42 43
I685 DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	42 43
I650 DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P	42 43
I651 DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N	42 43
Internal DP SPDIF				
I631		HDA	DP_INT_SPDIF_AUDIO	42 54

TBT/DP Net Properties

Electrical Contraint Set	Physical	Spacing		
Port A				
I641 TBT_A_R2D1	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<1>	28 31
I642 TBT_A_R2D1	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<1>	28 31
I643 TBT_A_R2D0	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<0>	28 31
I644 TBT_A_R2D0	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<0>	28 31
I645	TBTDP_90D	TBTDP	TBT_A_R2D_P<1..0>	31
I646	TBTDP_90D	TBTDP	TBT_A_R2D_N<1..0>	31
I650 DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	28 31
I651 DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	28 31
I648 DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	28 31
I649 DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	28 31
I652	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	31
I647	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	31
I678	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	31
I679	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	31
I640 DP_A_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	31
I639 DP_A_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	31
I653	TBTDP_90D	TBTDP	TBT_A_D2R_C_P<1..0>	31
I654	TBTDP_90D	TBTDP	TBT_A_D2R_C_N<1..0>	31
I638 TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_P<1>	28 31
I636 TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_N<1>	28 31
I637 TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_P<0>	28 31
I634 TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_N<0>	28 31
I655 TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	28 31
I656 TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	28 31
I657	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	31
I658	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	31
I660 DP_A_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	31
I661 DP_A_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	31
I630	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_P	31
I631	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_N	31
Port B				
I652 TBT_B_R2D1	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<1>	28 32
I653 TBT_B_R2D1	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<1>	28 32
I640 TBT_B_R2D0	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<0>	28 32
I641 TBT_B_R2D0	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<0>	28 32
I655	TBTDP_90D	TBTDP	TBT_B_R2D_P<1..0>	32
I656	TBTDP_90D	TBTDP	TBT_B_R2D_N<1..0>	32
I650 DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	28 32
I651 DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	28 32
I648 DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	28 32
I649 DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	28 32
I652	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	32
I647	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	32
I678	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	32
I679	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	32
I640 DP_B_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	32
I639 DP_B_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	32
I661	TBTDP_90D	TBTDP	TBT_B_D2R_C_P<1..0>	32
I660	TBTDP_90D	TBTDP	TBT_B_D2R_C_N<1..0>	32
I666 TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_P<1>	28 32
I668 TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_N<1>	28 32
I676 TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_P<0>	28 32
I677 TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_N<0>	28 32
I666 TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	28 32
I669 TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	28 32
I665	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	32
I670	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	32
I668 DP_B_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	32
I672 DP_B_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	32
I671	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_P	32
I672	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_N	32

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

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TBT/DP Constraints

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GDDR5

GDDR5-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12 MM	=STANDARD	=STANDARD
GDDR_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GDDR_MA_PHY	*	GDDR_45S
GDDR_ADBI_PHY	*	GDDR_45S
GDDR_CTRL_PHY	*	GDDR_45S
GDDR_CLK_PHY	*	GDDR_80D
GDDR_DQ_PHY	*	GDDR_45S
GDDR_EDC_PHY	*	GDDR_45S
GDDR_DBI_PHY	*	GDDR_45S
GDDR_WCK_PHY	*	GDDR_80D

Main Segment Min Spacing Rules for 4.5 Gbps or Less (AMD Doc# 49919)

	Trace-to-Trace				Isolation				
Table	Micro	Design	Strip	Design	Micro	Design	Strip	Design	Comments
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Memory address (MA). Implented 4.5 Gbps or less rules for K70.
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Address dynamic bus inversion (ADBI)
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Control (CTRL)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Clock (CLK)
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data (DQ)
5-6/5-7	7:1	7:1	7:1	7:1	7:1	7:1	7:1	7:1	Error detection pins (EDC). Using larger isolation rules,
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data dynamic bus inversion (DBI)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Forwarded clock (WCK)

GDDR5-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_ISO	*	=3X_DIELECTRIC	?
GDDR_ISO	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR_MA2MA	*	=2x_DIELECTRIC	?
GDDR_MA2MA	TOP,BOTTOM	=3X_DIELECTRIC	?
GDDR_ADBI2ADBI	*	=2x_DIELECTRIC	?
GDDR_ADBI2ADBI	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_CTRL2CTRL	*	=2x_DIELECTRIC	?
GDDR_CTRL2CTRL	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_CLK2CLK	*	=3X_DIELECTRIC	?
GDDR_CLK2CLK	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_DQ2DQ	*	=3x_DIELECTRIC	?
GDDR_DQ2DQ	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_EDC_ISO	*	=3X_DIELECTRIC	?
GDDR_EDC_ISO	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_EDC2EDC	*	=3X_DIELECTRIC	?
GDDR_EDC2EDC	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_DBI2DBI	*	=3x_DIELECTRIC	?
GDDR_DBI2DBI	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_WCK2WCK	*	=3X_DIELECTRIC	?
GDDR_WCK2WCK	TOP,BOTTOM	=5x_DIELECTRIC	?

Constraints (x in {A, B}, y in {0, 1})

Memory Address: MAxy[8:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_MA	*	*	GDDR_ISO
GDDR_*_*_MA	=SAME	*	GDDR_MA2MA

Address Dynamic Bus Inversion: ADBIxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_ADBI	*	*	GDDR_ISO
GDDR_*_*_ADBI	=SAME	*	GDDR_ADBI2ADBI

Control: Reset, CKExy, CSxy, WExy, RASxy, CASxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	=SAME	*	GDDR_CTRL2CTRL

Clock: CKxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_CLK	*	*	GDDR_ISO
GDDR_*_*_CLK	=SAME	*	GDDR_CLK2CLK

Data: DQxy[31:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DQ	*	*	GDDR_ISO
GDDR_*_*_DQ	=SAME	*	GDDR_DQ2DQ

Error Detection: EDCxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_EDC	*	*	GDDR_EDC_ISO
GDDR_*_*_EDC	=SAME	*	GDDR_EDC2EDC

Data Dynamic Bus Inversion: DDBIxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DBI	*	*	GDDR_ISO
GDDR_*_*_DBI	=SAME	*	GDDR_DBI2DBI

Forwarded Clock: WCKxy[1:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_WCK	*	*	GDDR_ISO
GDDR_*_*_WCK	=SAME	*	GDDR_WCK2WCK

GPU

GPU-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_GPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

GPU-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_GPU_ISO	*	=4:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_GPU	*	*	CLK_GPU_ISO

GDDR5 Frame Buffer A

Electrical Contraint Set	Physical	Spacing			
Memory Address					
1642 GDDR_A0_MA	GDDR_MA_PHY	GDDR_A_0_MA	FB_A0_A<8..0>	NO_TEST=TRUE	@0 @1
1643 GDDR_A1_MA	GDDR_MA_PHY	GDDR_A_1_MA	FB_A1_A<8..0>	NO_TEST=TRUE	@0 @1
Address Dynamic Bus Inv					
1644 GDDR_A0_ADBI	GDDR_ADBI_PHY	GDDR_A_0_ADBI	FB_A0_ABI_L	NO_TEST=TRUE	@0 @1
1645 GDDR_A1_ADBI	GDDR_ADBI_PHY	GDDR_A_1_ADBI	FB_A1_ABI_L	NO_TEST=TRUE	@0 @1
Control					
1646 GDDR_A0_CKE	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CKE_L	NO_TEST=TRUE	@0 @1
1648 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CS_L	NO_TEST=TRUE	@0 @1
1649 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_WE_L	NO_TEST=TRUE	@0 @1
1650 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CAS_L	NO_TEST=TRUE	@0 @1
1651 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_RAS_L	NO_TEST=TRUE	@0 @1
1652 GDDR_A1_CKE	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CKE_L	NO_TEST=TRUE	@0 @1
1654 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CS_L	NO_TEST=TRUE	@0 @1
1655 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_WE_L	NO_TEST=TRUE	@0 @1
1653 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CAS_L	NO_TEST=TRUE	@0 @1
1656 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_RAS_L	NO_TEST=TRUE	@0 @1
Clock					
1657 GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_P	NO_TEST=TRUE	@0 @1
1658 GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_N	NO_TEST=TRUE	@0 @1
1660 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_P	NO_TEST=TRUE	@0 @1
1659 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_N	NO_TEST=TRUE	@0 @1
Data					
1661 GDDR_A0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<7..0>	NO_TEST=TRUE	@0 @1
1662 GDDR_A0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<15..8>	NO_TEST=TRUE	@0 @1
1663 GDDR_A0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<23..16>	NO_TEST=TRUE	@0 @1
1664 GDDR_A0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<31..24>	NO_TEST=TRUE	@0 @1
1665 GDDR_A1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<7..0>	NO_TEST=TRUE	@0 @1
1666 GDDR_A1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<15..8>	NO_TEST=TRUE	@0 @1
1667 GDDR_A1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<23..16>	NO_TEST=TRUE	@0 @1
1668 GDDR_A1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<31..24>	NO_TEST=TRUE	@0 @1
Error Detection					
1670 GDDR_A0_EDC0	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<0>	NO_TEST=TRUE	@0 @1
1669 GDDR_A0_EDC1	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<1>	NO_TEST=TRUE	@0 @1
1671 GDDR_A0_EDC2	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<2>	NO_TEST=TRUE	@0 @1
1672 GDDR_A0_EDC3	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<3>	NO_TEST=TRUE	@0 @1
1674 GDDR_A1_EDC0	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<0>	NO_TEST=TRUE	@0 @1
1675 GDDR_A1_EDC1	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<1>	NO_TEST=TRUE	@0 @1
1676 GDDR_A1_EDC2	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<2>	NO_TEST=TRUE	@0 @1
1673 GDDR_A1_EDC3	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<3>	NO_TEST=TRUE	@0 @1
Data Dynamic Bus Inv					
1677 GDDR_A0_DBI0	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<0>	NO_TEST=TRUE	@0 @1
1678 GDDR_A0_DBI1	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<1>	NO_TEST=TRUE	@0 @1
1679 GDDR_A0_DBI2	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<2>	NO_TEST=TRUE	@0 @1
1680 GDDR_A0_DBI3	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<3>	NO_TEST=TRUE	@0 @1
1681 GDDR_A1_DBI0	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<0>	NO_TEST=TRUE	@0 @1
1682 GDDR_A1_DBI1	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<1>	NO_TEST=TRUE	@0 @1
1683 GDDR_A1_DBI2	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<2>	NO_TEST=TRUE	@0 @1
1684 GDDR_A1_DBI3	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<3>	NO_TEST=TRUE	@0 @1
Forwarded Clock					
1685 GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<0>	NO_TEST=TRUE	@0 @1
1687 GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<0>	NO_TEST=TRUE	@0 @1
1686 GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<1>	NO_TEST=TRUE	@0 @1
1688 GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<1>	NO_TEST=TRUE	@0 @1
1689 GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<0>	NO_TEST=TRUE	@0 @1
1690 GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<0>	NO_TEST=TRUE	@0 @1
1692 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<1>	NO_TEST=TRUE	@0 @1
1691 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<1>	NO_TEST=TRUE	@0 @1

GDDR5 Frame Buffer B

Electrical Contraint Set	Physical	Spacing			
Memory Address					
1652 GDDR_B0_MA	GDDR_MA_PHY	GDDR_B_0_MA	FB_B0_A<8..0>	NO_TEST=TRUE	@0 @2
1692 GDDR_B1_MA	GDDR_MA_PHY	GDDR_B_1_MA	FB_B1_A<8..0>	NO_TEST=TRUE	@0 @2
Address Dynamic Bus Inv					
1654 GDDR_B0_ADBI	GDDR_ADBI_PHY	GDDR_B_0_ADBI	FB_B0_ABI_L	NO_TEST=TRUE	@0 @2
1652 GDDR_B1_ADBI	GDDR_ADBI_PHY	GDDR_B_1_ADBI	FB_B1_ABI_L	NO_TEST=TRUE	@0 @2
Control					
1656 GDDR_B0_CKE	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CKE_L	NO_TEST=TRUE	@0 @2
1670 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CS_L	NO_TEST=TRUE	@0 @2
1660 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_WE_L	NO_TEST=TRUE	@0 @2
1670 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CAS_L	NO_TEST=TRUE	@0 @2
1670 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_RAS_L	NO_TEST=TRUE	@0 @2
1662 GDDR_B1_CKE	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CKE_L	NO_TEST=TRUE	@0 @2
1670 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CS_L	NO_TEST=TRUE	@0 @2
1660 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_WE_L	NO_TEST=TRUE	@0 @2
1670 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CAS_L	NO_TEST=TRUE	@0 @2
1670 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_RAS_L	NO_TEST=TRUE	@0 @2
Clock					
1659 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_P	NO_TEST=TRUE	@0 @2
1710 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_N	NO_TEST=TRUE	@0 @2
1709 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_P	NO_TEST=TRUE	@0 @2
1711 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_N	NO_TEST=TRUE	@0 @2
Data					
1713 GDDR_B0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<7..0>	NO_TEST=TRUE	@0 @2
1712 GDDR_B0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<15..8>	NO_TEST=TRUE	@0 @2
1715 GDDR_B0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<23..16>	NO_TEST=TRUE	@0 @2
1714 GDDR_B0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<31..24>	NO_TEST=TRUE	@0 @2
1716 GDDR_B1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<7..0>	NO_TEST=TRUE	@0 @2
1717 GDDR_B1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<15..8>	NO_TEST=TRUE	@0 @2
1718 GDDR_B1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<23..16>	NO_TEST=TRUE	@0 @2
1719 GDDR_B1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<31..24>	NO_TEST=TRUE	@0 @2
Error Detection					
1720 GDDR_B0_EDC0	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<0>	NO_TEST=TRUE	@0 @2
1721 GDDR_B0_EDC1	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<1>	NO_TEST=TRUE	@0 @2
1722 GDDR_B0_EDC2	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<2>	NO_TEST=TRUE	@0 @2
1723 GDDR_B0_EDC3	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<3>	NO_TEST=TRUE	@0 @2
1724 GDDR_B1_EDC0	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<0>	NO_TEST=TRUE	@0 @2
1725 GDDR_B1_EDC1	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<1>	NO_TEST=TRUE	@0 @2
1726 GDDR_B1_EDC2	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<2>	NO_TEST=TRUE	@0 @2
1727 GDDR_B1_EDC3	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<3>	NO_TEST=TRUE	@0 @2
Data Dynamic Bus Inv					
1728 GDDR_B0_DBI0	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<0>	NO_TEST=TRUE	@0 @2
1729 GDDR_B0_DBI1	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<1>	NO_TEST=TRUE	@0 @2
1730 GDDR_B0_DBI2	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<2>	NO_TEST=TRUE	@0 @2
1731 GDDR_B0_DBI3	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<3>	NO_TEST=TRUE	@0 @2
1732 GDDR_B1_DBI0	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<0>	NO_TEST=TRUE	@0 @2
1733 GDDR_B1_DBI1	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<1>	NO_TEST=TRUE	@0 @2
1734 GDDR_B1_DBI2	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<2>	NO_TEST=TRUE	@0 @2
1735 GDDR_B1_DBI3	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<3>	NO_TEST=TRUE	@0 @2
Forwarded Clock					
1736 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<0>	NO_TEST=TRUE	@0 @2
1737 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<0>	NO_TEST=TRUE	@0 @2
1739 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<1>	NO_TEST=TRUE	@0 @2
1738 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<1>	NO_TEST=TRUE	@0 @2
1740 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<0>	NO_TEST=TRUE	@0 @2
1741 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<0>	NO_TEST=TRUE	@0 @2
1743 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<1>	NO_TEST=TRUE	@0 @2
1742 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<1>	NO_TEST=TRUE	@0 @2

GPU

Electrical Contraint Set	Physical	Spacing			
Clocks					
1744	CLK_GPU_55S	CLK_GPU	PEX_TSTCLK_O_PL		78
1745	CLK_GPU_55S	CLK_GPU	PEX_TSTCLK_O_NG		78
1746	CLK_PCIE_PHY	CLK_PCIE	GPU_TESTMODE		@3
1856	CLK_PCIE_PHY	CLK_PCIE	GPU_PEX_TERMP		78
1762	CLK_GPU_55S	CLK_GPU	FB_A0_CK_MID	NO_TEST=TRUE	@1
1763	CLK_GPU_55S	CLK_GPU	FB_A1_CK_MID	NO_TEST=TRUE	@1
1761	CLK_GPU_55S	CLK_GPU	FB_B0_CK_MID	NO_TEST=TRUE	@2
1764	CLK_GPU_55S	CLK_GPU	FB_B1_CK_MID	NO_TEST=TRUE	@2
1765	CLK_GPU_55S	CLK_GPU	FB_C0_CK_MID	NO_TEST=TRUE	
1766	CLK_GPU_55S	CLK_GPU	FB_C1_CK_MID	NO_TEST=TRUE	ULTIMATE
1767	CLK_GPU_55S	CLK_GPU	FB_D0_CK_MID	NO_TEST=TRUE	ONLY
1768	CLK_GPU_55S	CLK_GPU	FB_D1_CK_MID	NO_TEST=TRUE	
1771	CLK_GPU_55S	CLK_GPU	GPU_JTAG_TCK		@3 @5
1772	CLK_GPU_55S	CLK_GPU	GPU_ROM_SCLK		@3 @4
1773	CLK_GPU_55S	CLK_GPU	GPU_ROM_SCLK_R		@4
1774	CLK_GPU_55S	CLK_GPU	GPU_XTALOUT		
1775	CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTALOUT		@3 @4
1776	CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTALIN		@3 @4
SMB					
1854	SMB_PHY	SMB	GPU_SMB_CLK		@3 @4
1855	SMB_PHY	SMB	GPU_SMB_DAT		@3 @4
1853	SMB_PHY	SMB	GPU_SMB_CLK_R		@3 @4
1852	SMB_PHY	SMB	GPU_SMB_DAT_R		@3 @4
PCIe Compensation					
1852	PCIE_50S	COMP_PCIE	FB_CAL_PD_VDDQ		@0
1850	PCIE_50S	COMP_PCIE	FB_CAL_PU_GND		@0
1849	PCIE_50S	COMP_PCIE	FB_CAL_TERM_GND		@0

Frame Buffer Reset

Electrical Contraint Set	Physical	Spacing			
Reset					
1784 GDDR_A0_RESET	GDDR_50S	GDDR_CTRL	FB_A0_RESET_L		@0 @1
1785 GDDR_A1_RESET	GDDR_50S	GDDR_CTRL	FB_A1_RESET_L		@0 @1
1786 GDDR_B0_RESET	GDDR_50S	GDDR_CTRL	FB_B0_RESET_L		@0 @2
1787 GDDR_B1_RESET	GDDR_50S	GDDR_CTRL	FB_B1_RESET_L		@0 @2
1788 GDDR_C0_RESET	GDDR_50S	GDDR_CTRL	FB_C0_RESET_L		
1789 GDDR_C1_RESET	GDDR_50S	GDDR_CTRL	FB_C1_RESET_L		ULTIMATE
1790 GDDR_D0_RESET	GDDR_50S	GDDR_CTRL	FB_D0_RESET_L		ONLY
1791 GDDR_D1_RESET	GDDR_50S	GDDR_CTRL	FB_D1_RESET_L		

SYNC_MASTER=D8 AARON SYNC_DATE=03/13/2012

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Backlight Controller

BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM

BLC-specific Spacing Definitions
BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	1.00MM	1000

Constraints
BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	2000
PHASE_SW2SW	*	=1:1_SPACING	?
PHASE_SW2PWR	*	=2:1_SPACING	?
PHASE_SW2GND	*	=2:1_SPACING	?

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	POWER	*	PHASE_SW2PWR
BLC_PHASE	GND	*	PHASE_SW2GND

BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	=3:1_SPACING	?

BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

BKLT MISCELLANEOUS

Electrical Contraint Set	Physical	Spacing		
SPI				
B5A0	SMB_PHY	SMB	SMB_PCH_BLC_SCL	
B5A1	SMB_PHY	SMB	SMB_PCH_BLC_SDA	
B81	SMB_PHY	SMB	SMB_TCON_BLC_SCL	
B81	SMB_PHY	SMB	SMB_TCON_BLC_SDA	
12M REFERENCE CRYSTAL				
B8F0	CLK_XTAL	XTAL	BLC_MCU_XTAL_IN	72
B8E0	CLK_XTAL	XTAL	BLC_MCU_XTAL_OUT	72
B8E1	CLK_XTAL	XTAL	BLC_MCU_XTAL_OUT_R	72
250K REFERENCE CLOCKS				
B8F1	CPU_50S	CLK_PCH	STRCLK_R1	72 73
B8F2	CPU_50S	CLK_PCH	LED_DRVR_CLK	73

Input Bus	Physical	Spacing	Voltage	DIDT	NO_TEST		
B7A0	POWER	POWER	12V			PP12V_S0_BLC_VIN2	72 73 74
B7J0	POWER	POWER	12V			PP12V_S0_BLC_VINP	72 74
B8A0	POWER	POWER	14V			PRE_REG_OUT	72 73
B8D7	POWER	POWER	3.3V			BLC_P3V3S	72 74
B8F7	POWER	POWER	3.3V			BLC_P3V3_REF	72 74
B8D0	POWER	POWER	3.3V			BLC_P3V3	
B8K0	POWER	POWER	3.3V			PP3V3_S0_BLC_R	72
B8J1	POWER	POWER	8V			SPTX_VIN	73
B8D0	POWER	POWER	8V			PP8V_BLC	72 73
B8J7	POWER	POWER	8V			BLC_VIN2	73 74
B8K2	POWER	POWER	14V			BOOST_FET_DRAIN	72
B8K5	POWER	POWER	12V			BOOST_VDD	72
B8J5	POWER	POWER	5V			PP5V_S0_BLC_R	72 73 74
B8J6	POWER	POWER	12V			PP12V_S0_BLC_F	74
Local Ground							
B7A1	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_1	73 74
B8D5	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_2	73 74
B8D6	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_3	73 74
B8J0	GND	GND	0V			AGND_BLC	73 74
Backlight							
B7S5	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE1	73
B7S6	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE1_R	73
B7T6	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE2	73
B7T7	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE2_R	73
B8D6	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE3	73
B7S7	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE3_R	73
B7S5	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_1	73
B7S6	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_2	73
B7S6	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_3	73
B8D1	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS1	73
B8D2	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS2	73
B8D3	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS3	73
B7S8	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C1	73
B7S9	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C2	73
B7S9	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C3	73
B8J2	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_1	73
B8J2	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_2	73
B8J1	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_3	73
B8J0	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK1	73
B8J1	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK2	73
B8J2	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK3	73
B8A3	BLC_CTL_PHY	BLC_CTL				BLC_PWM_1_R	72 73
B8A4	BLC_CTL_PHY	BLC_CTL				BLC_PWM_2_R	72 73
B8A5	BLC_CTL_PHY	BLC_CTL				BLC_PWM_3_R	72 73
B8E0	BLC_CTL_PHY	BLC_CTL				BLC_PWM_1	73 74
B8E5	BLC_CTL_PHY	BLC_CTL				BLC_PWM_2	73 74
B8E6	BLC_CTL_PHY	BLC_CTL				BLC_PWM_3	73 74
B8E0	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF1	73 74
B8E1	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF2	73 74
B8E2	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF3	73 74
B7A6	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP1	73
B8A6	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP2	73
B7A7	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP3	73
B8F2	BLC_CTL_PHY	BLC_CTL				BCOMP1	73
B8E3	BLC_CTL_PHY	BLC_CTL				BCOMP2	73
B8A0	BLC_CTL_PHY	BLC_CTL				BCOMP3	73
B8A1	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT1	73
B8A2	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT2	73
B8A3	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT3	73
B8A1	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_1	73
B8A2	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_2	73
B8A3	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_3	73
B8K6	BLC_CTL_PHY	BLC_CTL				PRE_REG_OUT_R	72
B8K5	BLC_CTL_PHY	BLC_CTL				BOOST_FB	72
B8K4	BLC_CTL_PHY	BLC_CTL				BOOST_COMP	72
B8K7	BLC_CTL_PHY	BLC_CTL				BOOST_COMP_C	72
B8K0	BLC_CTL_PHY	BLC_CTL			TRUE	BOOST_GDRV	72
B8K1	BLC_CTL_PHY	BLC_CTL			TRUE	BOOST_GDRV_R	72
B8K3	BLC_CTL_PHY	BLC_CTL				BOOST_ISNS	72
B8K8	BLC_CTL_PHY	BLC_CTL				BOOST_ISNS_R	72
B7S0	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_1	73
B7S1	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_2	73
B7S2	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_3	73
OUTPUT BUS							
B7A0	POWER_BLC_RET	BLC_HV	80V			IS1_BLC_F	74
B7A1	POWER_BLC_RET	BLC_HV	80V			IS2_BLC_F	74
B7A0	POWER_BLC_RET	BLC_HV	80V			IS3_BLC_F	74
B7S4	POWER_BLC_RET	BLC_HV	80V			IS1_BLC	73 74
B7S2	POWER_BLC_RET	BLC_HV	80V			IS2_BLC	73 74
B7S3	POWER_BLC_RET	BLC_HV	80V			IS3_BLC	73 74
B7S0	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_1	74
B7S0	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_1	74
B7S0	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_2	74
B7S0	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_2	74
B7S0	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_3	74
B7S0	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_3	74
B8J6	POWER_BLC	BLC_HV	80V			BLC_VOUT1	73 74
B8J4	POWER_BLC	BLC_HV	80V			BLC_VOUT2	73 74
B8J3	POWER_BLC	BLC_HV	80V			BLC_VOUT3	73 74

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PAGE TITLE

BLC Constraints

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GPU CORE PHASES

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
	POWER	POWER	12V			PP12V_S0_GPUCORE_FLT	69 70 71
	POWER	POWER	5V			PP5V_S0_GPU_VCORE_VCC	69
Local Ground							
	GND	GND	0V			AGND_GPU	69
Phase 1							
	POWER	POWER	12V			REG_LVCC_UB510	70
	POWER	POWER	12V			REG_UVCC_UB510	70
	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_1	69 70
	VR_CTL_PHY	VR_CTL				VR_GPU_PWM1_R	69
	POWER	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_1	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_1	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_1_RC	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_1	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_1	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_1	70
	POWER	POWER	0.9V			PPGPUCORE_S0_SENSE_1	70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_1_P	69 70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_1_N	69 70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS1_R_P	69
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS1_R_N	69
ISNS_GPU_CORE		SENSE				VR_GPU_ISNS1_RR_2	69
Phase 2							
	POWER	POWER	12V			REG_LVCC_UB530	70
	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_2	69 70
	VR_CTL_PHY	VR_CTL				VR_GPU_PWM2_R	69
	POWER	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_2	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_2	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_2_RC	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_2	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_2	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_2	70
	POWER	POWER	0.9V			PPGPUCORE_S0_SENSE_2	70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_2_P	69 70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_2_N	69 70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS2_R_P	69
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS2_R_N	69
ISNS_GPU_CORE		SENSE				VR_GPU_ISNS2_RR_2	69
Phase 3							
	POWER	POWER	12V			REG_VCC_UB550	70
	POWER	POWER	12V			REG_UVCC_UB550	70
	POWER	POWER	12V			REG_LVCC_UB550	70
	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_3	69 70
	VR_CTL_PHY	VR_CTL				VR_GPU_PWM3_R	69
	POWER	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_3	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_3	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_3_RC	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_3	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_3	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_3	70
	POWER	POWER	0.9V			PPGPUCORE_S0_SENSE_3	70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_3_P	69 70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_3_N	69 70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS3_R_P	69
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS3_R_N	69
ISNS_GPU_CORE		SENSE				VR_GPU_ISNS3_RR_2	69
Phase 4							
	POWER	POWER	12V			REG_LVCC_UB650	71
	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_4	69 71
	VR_CTL_PHY	VR_CTL				VR_GPU_PWM4_R	69
	POWER	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_4	71
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_4	71
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_4_RC	71
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_4	71
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_4	71
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_4	71
	POWER	POWER	0.9V			PPGPUCORE_S0_SENSE_4	71
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_4_P	69 71
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_4_N	69 71
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS4_R_P	69
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS4_R_N	69
ISNS_GPU_CORE		SENSE				VR_GPU_ISNS4_RR_2	69

GPU CORE CONTROLLER

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
ISL6334							
	VR_CTL_PHY	VR_CTL				VR_GPU_COMP	69
	VR_CTL_PHY	VR_CTL				VR_GPU_COMP_R	69
	VR_CTL_PHY	VR_CTL				VR_GPU_COMP_RC	69
	VR_CTL_PHY	VR_CTL				VR_GPU_FB	69
	VR_CTL_PHY	VR_CTL				VR_GPU_FB_R	69
	VR_CTL_PHY	VR_CTL				VR_GPU_VDIFF	69
	VR_CTL_PHY	VR_CTL				VR_VDF_R1	69
	VR_CTL_PHY	VR_CTL				VR_VDF_R2	69
	VR_CTL_PHY	VR_CTL				VR_GPU_TCOMP	69
	VR_CTL_PHY	VR_CTL				VR_GPU_OFS	69
	VR_CTL_PHY	VR_CTL				VR_GPU_FS	69
		VR_CTL				VR_GPU_EN_VTT	69
		VR_CTL				PM_EN_REG_GPUCORE_S0	69 76
		VR_CTL				PM_PGOOD_REG_GPUCORE_S0	69 76
		VR_CTL				GPU_PSI_L	69 84
	VR_CTL_PHY	VR_CTL				VR_GPU_IOUT	
	VR_CTL_PHY	VR_CTL				VR_GPU_IMON	50 69 105
	VR_CTL_PHY	VR_CTL				VR_GPU_FAN	69 105
		VR_CTL				VR_GPU_VRDHOT	69
		VR_CTL				VR_GPU_EN_PWR	
	VR_CTL_PHY	VR_CTL				VR_GPU_SS	69
	VR_CTL_PHY	VR_CTL				VR_GPU_DAC	69
	VR_CTL_PHY	VR_CTL				VR_GPU_REF	69
	VR_CTL_PHY	VR_CTL				VR_GPU_TM	69
	VR_CTL_PHY	VR_CTL				VR_GPU_IMON	50 69 105
	VR_CTL_PHY	VR_CTL				VR_GPU_FAN	69 105
	VR_CTL_PHY	VR_CTL				VR_GPU_VRHOT	
		VR_CTL				GPU_PSI_R	
		VR_CTL				GPU_PSI_L_R	
	VR_CTL_PHY	VR_CTL				VR_GPU_IMON_R	69
VSNS_GPU_VDD	SNS_DIFF_PHY	SENSE				VSNS_GPU_VDD	69 85
VSNS_GPU_VSS	SNS_DIFF_PHY	SENSE				VSNS_GPU_VSS	69 85
	SNS_DIFF_PHY	SENSE				VR_GPU_VSEN	69
	SNS_DIFF_PHY	SENSE				VR_GPU_RGND	69
GPU VIDS							
		VR_VID				REG_GPUCORE_VID7	69
		VR_VID				REG_GPUCORE_VID6	69 85
		VR_VID				REG_GPUCORE_VID5	69 85
		VR_VID				REG_GPUCORE_VID4	69 85
		VR_VID				REG_GPUCORE_VID3	69 85
		VR_VID				REG_GPUCORE_VID2	69 85
		VR_VID				REG_GPUCORE_VID1	69 85
		VR_VID				REG_GPUCORE_VID0	69
		VR_VID				GPU_VCORE_VID6	
		VR_VID				GPU_VCORE_VID5	84 85
		VR_VID				GPU_VCORE_VID4	84 85
		VR_VID				GPU_VCORE_VID3	84 85
		VR_VID				GPU_VCORE_VID2	84 85
		VR_VID				GPU_VCORE_VID1	84 85
		VR_VID				GPU_VCORE_VID0	84 85
Output Bus							
	POWER	POWER	0.9V			PPVCORE_S0_GPU	87

GPU FBVDDQ

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
	POWER	POWER	5V			REG_VCC_U7750	68
	POWER	POWER	5V			REG_PVCC_U7750	68
Local Ground							
	GND	GND	0V			AGND_FBVDDQ	68
FBVDDQ							
	POWER	VR_SWITCH	12V	TRUE		REG_PHASE_FBVDDQ	68
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_FBVDDQ	68
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_FBVDDQ_RC	68
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_FBVDDQ	68
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_FBVDDQ_R	
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_FBVDDQ	68
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_FBVDDQ	68
		SENSE				VSNS_FBVDDQ	
VSNS_GPU_VDDQ	SNS_DIFF_PHY	SENSE				VSNS_FBVDDQ_P	68 85
VSNS_GPU_VDDQ	SNS_DIFF_PHY	SENSE				VSNS_FBVDDQ_N	68 85
		SENSE				FBVDDQ_SENSE_R	
	VR_CTL_PHY	VR_CTL				REG_FBVDDQ_OCSET	68
	VR_CTL_PHY	VR_CTL				REG_FBVDDQ_VO	68
		SENSE				REG_FBVDDQ_FB	
		SENSE				REG_FBVDDQ_RTN	
		SENSE				REG_FBVDDQ_FB_R	68
		SENSE				REG_FBVDDQ_RTN_R	68
Output Bus							
	POWER	POWER	1.5V			PPFBVDDQ_S0_GPU	87

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4V5_*

	Physical	Spacing	Netname	
I2	POWER	POWER	4V5_REG_IN	54

ENET_*

	Physical	Spacing	Netname	
E104	XDP_PHY	XDP	ENET_LOW_PWR	20 37 39

GPU_*

	Physical	Spacing	Netname	
E105	SPI_50S	SPI	GPU_ROM_CS_L	83 84
E106	SPI_50S	SPI	GPU_ROM_CS_L_R	84
E107	SPI_50S	SPI	GPU_ROM_SI	83 84
E108	SPI_50S	SPI	GPU_ROM_SI_R	84
E109	SPI_50S	SPI	GPU_ROM_SO	83 84
E111	SPI_50S	SPI	GPU_ROM_SO_R	84
E110	SPI_50S	SPI	GPU_ROM_WP_L	84

GPU_*

	Physical	Spacing	Netname	
E113	XDP_PHY	XDP	GPU_JTAG_TDI	83 85
E115	XDP_PHY	XDP	GPU_JTAG_TDO	83 85
E116	XDP_PHY	XDP	GPU_JTAG_TMS	83 85
E114	XDP_PHY	XDP	GPU_JTAG_TRST_L	83

JTAG_*

	Physical	Spacing	Netname	
E112	XDP_PHY	XDP	JTAG_TBT_TDI	20 28
E118	XDP_PHY	XDP	JTAG_TBT_TDO	20 28
E117	XDP_PHY	XDP	JTAG_TBT_TMS	20 28

ISNS_*

	Physical	Spacing	Netname	
E120	SMC_50S	SENSE	ISNS_GPUCORE_FB	50 98
E119	SMC_50S	SENSE	ISNS_P12VG3H_R	50 98
E121	SMC_50S	SENSE	ISNS_P12VS0_FBVDDQ_R	50 98
E122	SMC_50S	SENSE	ISNS_P12VS0_HDD_R	50 98
E123	SMC_50S	SENSE	ISNS_P3V3S4_AP_R	50 98

SMC_*

	Physical	Spacing	Netname	
E124	CLK_XTAL	XTAL	SMC_XTAL_R	47

REG_*

	Physical	Spacing	Netname	
E125	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET0	68
E126	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET1	68
E128	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET1_R	68
E127	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SREF	68

SMBUS_*

	Physical	Spacing	Netname	
E129	SMB_PHY	SMB	SMBUS_SMC_4_ASF_SCL	46 47
E130	SMB_PHY	SMB	SMBUS_SMC_4_ASF_SDA	46 47

SMC_*

	Physical	Spacing	Netname	
E140		SENSE	SMC_OOB1_RX_CN	36
E141		SENSE	SMC_OOB1_RX_FILT	36

TSNS_*

	Electrical	Physical	Spacing	Netname	
E132	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_1_N	52
E131	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_1_P	52
E139	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_2_N	52
E140	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_2_P	52
E141	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_3_N	52
E142	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_3_P	52
E143	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_1_N	52
E144	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_1_P	52
E145	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_2_N	52
E146	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_2_P	52
E147	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_3_N	52
E148	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_3_P	52
E149	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_4_N	52
E150	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_4_P	52
E151	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_5_N	52
E152	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_5_P	52
E153	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_6_N	52
E154	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_6_P	52
E155	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_7_N	52
E156	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_7_P	52
E158	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_SKIN_N	
E157	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_SKIN_P	

BLC_*

	Physical	Spacing	Voltage	Netname	
E32	BLC_CTL_PHY	BLC_CTL	5V	BLC_MCU_AOUT_R	74
E36	SMB_PHY	SMB		BLC_MCU_B_SDA_CONN	
E43	XDP_PHY	CLK_JTAG		BLC_MCU_RTCK	72
E45	XDP_PHY	XDP		BLC_MCU_TCK	72
E46	XDP_PHY	XDP		BLC_MCU_TDI	72
E47	XDP_PHY	XDP		BLC_MCU_TDO	72
E48	XDP_PHY	XDP		BLC_MCU_TMS	72
E44	XDP_PHY	XDP		BLC_MCU_TRST	72
E49	XDP_PHY	XDP		BLC_MCU_TXD0	72

TBT_*

	Physical	Spacing	Voltage	Netname	
E134	TBT_I2C_55S	TBT_I2C		TBT_A_CONFIG1_RC	31
E135	TBT_I2C_55S	TBT_I2C		TBT_B_CONFIG1_RC	32

DP_*

	Physical	Spacing	Netname	
E99	TBT_I2C_55S	TBT_I2C	DP_TBTPA_DDC_CLK	31 33
E100	TBT_I2C_55S	TBT_I2C	DP_TBTPA_DDC_DATA	31 33
E102	TBT_I2C_55S	TBT_I2C	DP_TBTPB_DDC_CLK	32 33
E101	TBT_I2C_55S	TBT_I2C	DP_TBTPB_DDC_DATA	32 33

SML_*

	Physical	Spacing	Netname	
E133	SMB_PHY	SMB	SML_PCH_1_CLK	13 49
E136	SMB_PHY	SMB	SML_PCH_1_DATA	13 49

AYNCHRONOUS

	Electrical	Physical	Spacing	Netname	
E160		CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_L	6 46 47 63
E161		CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_R_L	6
E162		CPU_ASYNC_PHY	CPU_ASYNC	CPU_PECI_L	
E163		CPU_ASYNC_PHY	CPU_ASYNC	SMC_PECI_L	46 47 98
E164		CPU_ASYNC_PHY	CPU_ASYNC	CPU_CATERR_L	6 47
E165		CPU_ASYNC_PHY	CPU_ASYNC	CPU_PWRGD	6 14 18
E166		CPU_ASYNC_PHY	CPU_ASYNC	PM_SYNC	6 12
E167		CPU_ASYNC_PHY	CPU_ASYNC	PM_THRMTRIP_L	14 47
E168		CPU_ASYNC_PHY	CPU_ASYNC	CPU_RESET_L	6 14 18
E169		CPU_ASYNC_PHY	CPU_ASYNC	SMC_CPU_CATERR_L	46 47
E170		CPU_ASYNC_PHY	CPU_ASYNC	PCH_PROCPWRGD	14

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ASYNC_ISO	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ASYNC	*	*	CPU_ASYNC_ISO

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CPU_ASYNC_PHY	*	CPU_50S

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