IH110MS Version : 1.0

CPU :

Intel Skylake-S

System Chipset :

Intel Skylake-H Chipset

On Board Chipset :

IMVP8 -- NCP81203+NCP5230 6Phase
Gigabit LAN -- RTL8111GN Co-lay RTL8111E-VC
HDA Codec -- Realtek ALC662VD
Super I/O --IT8625E
SPI Flash 64Mb

Main Memory :

2 Channel DDR 4 * 2 (Max 16GB)

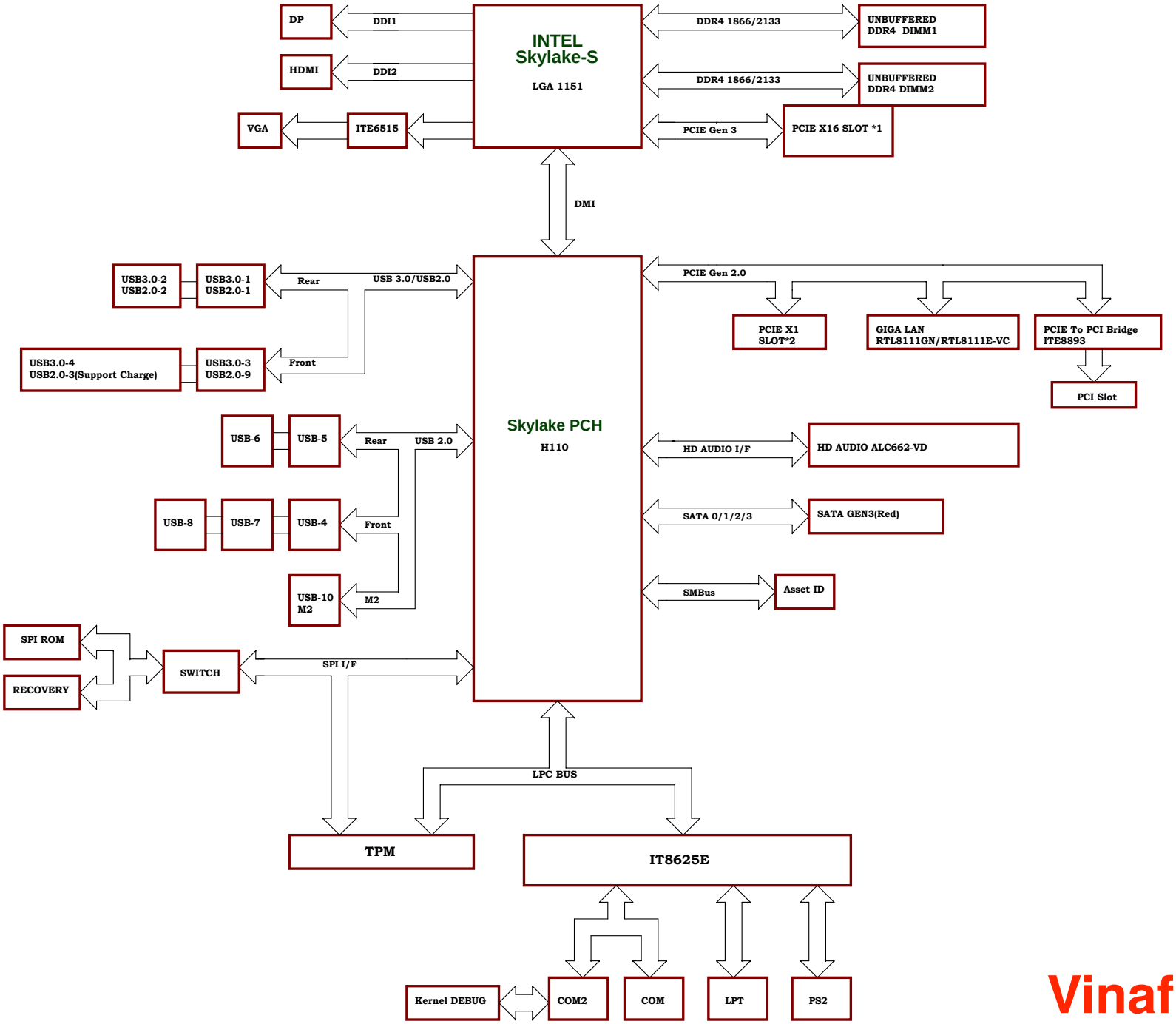
Expansion Slot :

PCI Express x16 Slot * 1
PCI Express x1 Slot * 2
PCI Slot * 1

lenovo

MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title: Cover Sheet		
Size	Document Number: IH110M	Rev: 1.0
Date: Tuesday, July 07, 2015	Sheet 1 of 43	



Slot Sequence:

PCIE X16

PCIE X1

PCIE X1

PCI

Vinafix

MSI MICRO-START INTL CO.,LTD.

Title: Block Diagram

Size | Document Number: IH110M | Rev: 1.0

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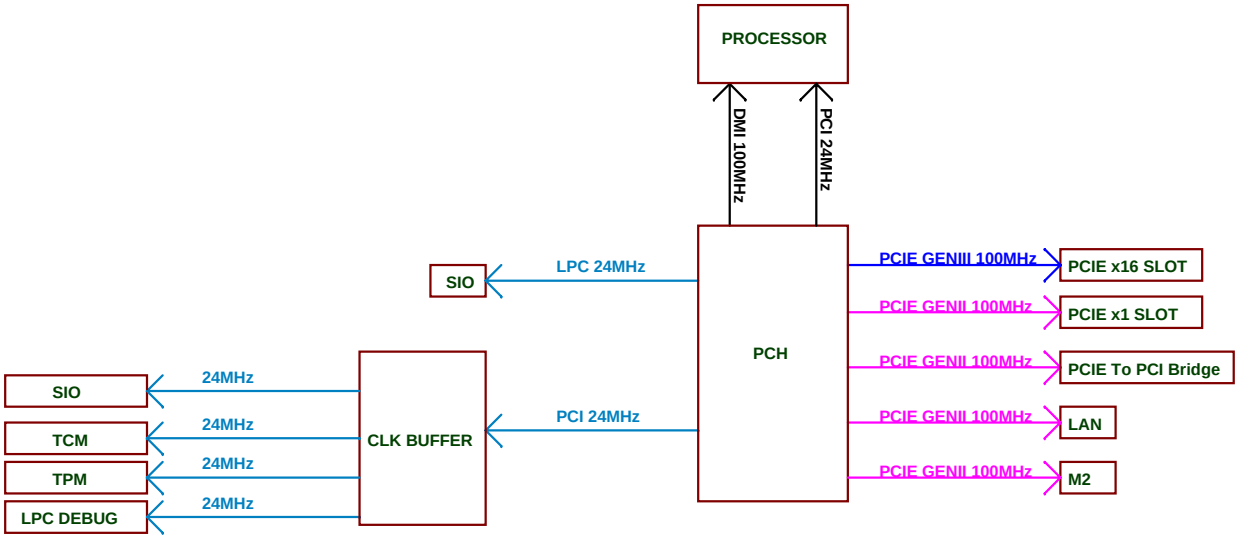
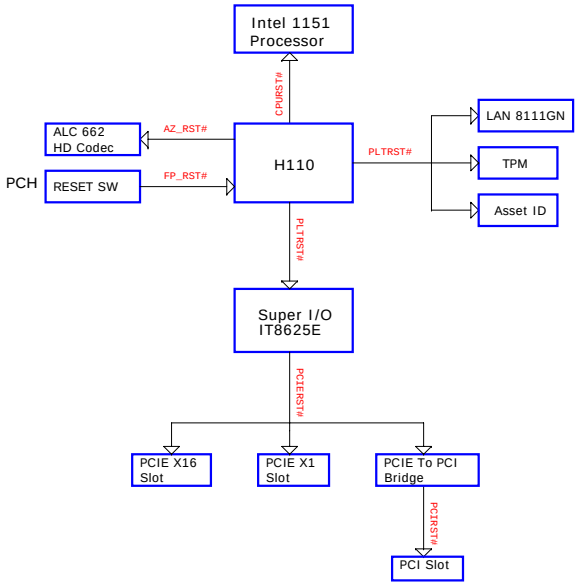


RESET MAP



MICRO-START INT'L CO.,LTD.

Title: Clock Distribution

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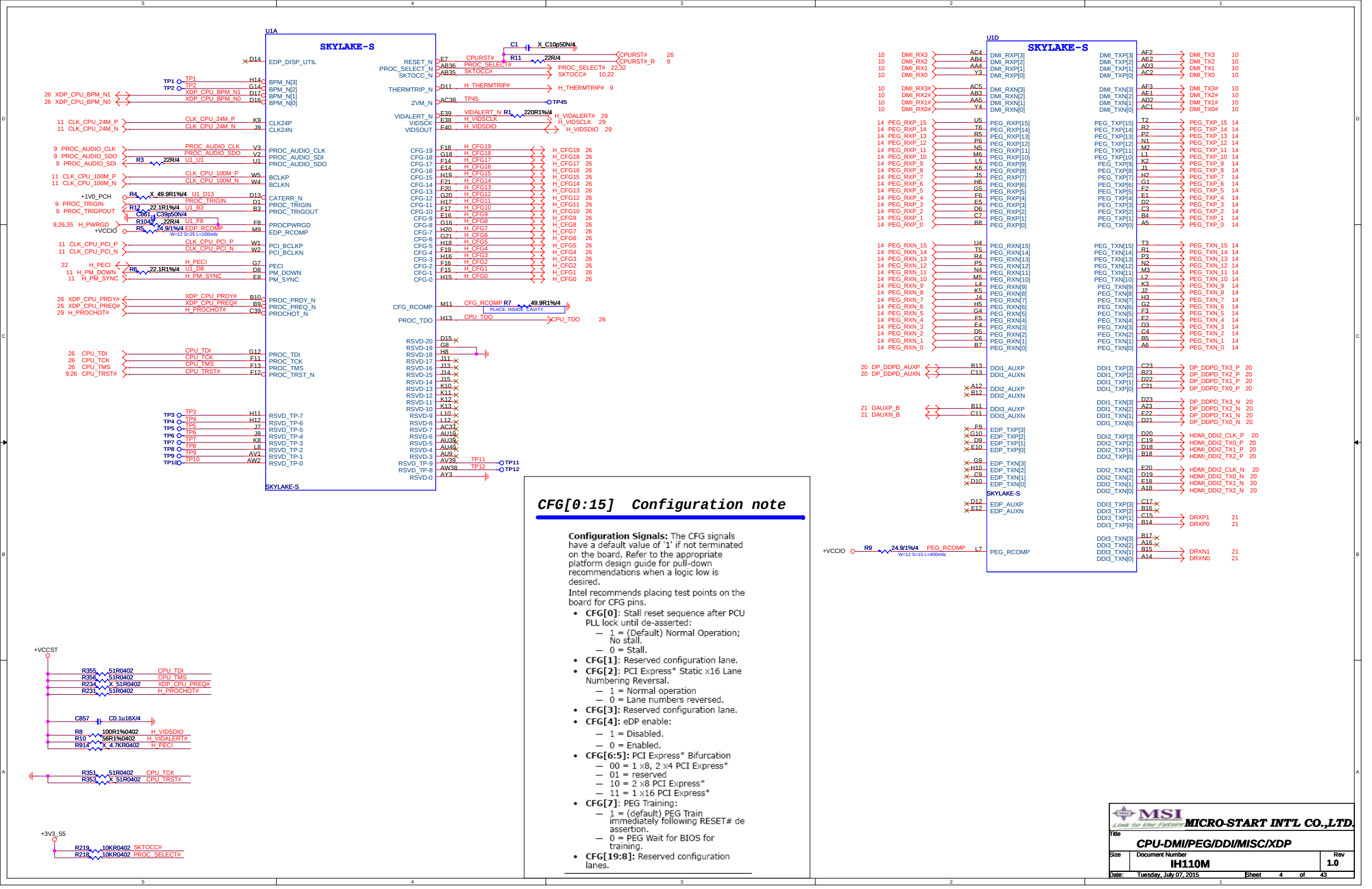
U1A
SKYLAKE-S
EDP_DISP_UTIL
BPM_N[3]
BPM_N[2]
BPM_N[1]
BPM_N[0]
CLK24P
CLK24N
PROC_AUDIO_CLK
PROC_AUDIO_SDI
PROC_AUDIO_SDO
BCLKP
BCLKN
CATERR_N
PROC_TRIGIN
PROC_TRIGOUT
PROCPWRGD
EDP_RCOMP
PCI_BCLKP
PCI_BCLKN
PECI
PM_DOWN
PM_SYNC
PROC_PRDY_N
PROC_PREQ_N
PROCHOT_N
PROC_TDI
PROC_TCK
PROC_TMS
PROC_TRST_N
RSVD_TP-7
RSVD_TP-6
RSVD_TP-5
RSVD_TP-4
RSVD_TP-3
RSVD_TP-2
RSVD_TP-1
RSVD_TP-0
SKYLAKE-S
RESET_N
PROC_SELECT_N
SKTOCC_N
THERMTRIP_N
ZVM_N
VIDALERT_N
VIDSCK
VIDSOUT
CFG_RCOMP
PROC_TDO
RSVD-20
RSVD-19
RSVD-18
RSVD-17
RSVD-16
RSVD-15
RSVD-14
RSVD-13
RSVD-12
RSVD-11
RSVD-10
RSVD-9
RSVD-8
RSVD-7
RSVD-6
RSVD-5
RSVD-4
RSVD-3
RSVD_TP-9
RSVD_TP-8
RSVD-0
CPURST#
PROC_SELECT#
SKTOCC#
H_THERMTRIP#
TP45
H_VIDALERT_N
H_VIDSCLK
H_VIDSDIO
H_CFG19
H_CFG18
H_CFG17
H_CFG16
H_CFG15
H_CFG14
H_CFG13
H_CFG12
H_CFG11
H_CFG10
H_CFG9
H_CFG8
H_CFG7
H_CFG6
H_CFG5
H_CFG4
H_CFG3
H_CFG2
H_CFG1
H_CFG0
CFG_RCOMP
CPU_TDO
TP11
TP12
U1D
SKYLAKE-S
DMI_RXP[3]
DMI_RXP[2]
DMI_RXP[1]
DMI_RXP[0]
DMI_RXN[3]
DMI_RXN[2]
DMI_RXN[1]
DMI_RXN[0]
PEG_RXP[15]
PEG_RXP[14]
PEG_RXP[13]
PEG_RXP[12]
PEG_RXP[11]
PEG_RXP[10]
PEG_RXP[9]
PEG_RXP[8]
PEG_RXP[7]
PEG_RXP[6]
PEG_RXP[5]
PEG_RXP[4]
PEG_RXP[3]
PEG_RXP[2]
PEG_RXP[1]
PEG_RXP[0]
PEG_RXN[15]
PEG_RXN[14]
PEG_RXN[13]
PEG_RXN[12]
PEG_RXN[11]
PEG_RXN[10]
PEG_RXN[9]
PEG_RXN[8]
PEG_RXN[7]
PEG_RXN[6]
PEG_RXN[5]
PEG_RXN[4]
PEG_RXN[3]
PEG_RXN[2]
PEG_RXN[1]
PEG_RXN[0]
DDI1_AUXP
DDI1_AUXN
DDI2_AUXP
DDI2_AUXN
DDI3_AUXP
DDI3_AUXN
EDP_TXP[3]
EDP_TXP[2]
EDP_TXP[1]
EDP_TXP[0]
EDP_TXN[3]
EDP_TXN[2]
EDP_TXN[1]
EDP_TXN[0]
EDP_AUXP
EDP_AUXN
PEG_RCOMP
DMI_TXP[3]
DMI_TXP[2]
DMI_TXP[1]
DMI_TXP[0]
DMI_TXN[3]
DMI_TXN[2]
DMI_TXN[1]
DMI_TXN[0]
PEG_TXP[15]
PEG_TXP[14]
PEG_TXP[13]
PEG_TXP[12]
PEG_TXP[11]
PEG_TXP[10]
PEG_TXP[9]
PEG_TXP[8]
PEG_TXP[7]
PEG_TXP[6]
PEG_TXP[5]
PEG_TXP[4]
PEG_TXP[3]
PEG_TXP[2]
PEG_TXP[1]
PEG_TXP[0]
PEG_TXN[15]
PEG_TXN[14]
PEG_TXN[13]
PEG_TXN[12]
PEG_TXN[11]
PEG_TXN[10]
PEG_TXN[9]
PEG_TXN[8]
PEG_TXN[7]
PEG_TXN[6]
PEG_TXN[5]
PEG_TXN[4]
PEG_TXN[3]
PEG_TXN[2]
PEG_TXN[1]
PEG_TXN[0]
DDI1_TXP[3]
DDI1_TXP[2]
DDI1_TXP[1]
DDI1_TXP[0]
DDI1_TXN[3]
DDI1_TXN[2]
DDI1_TXN[1]
DDI1_TXN[0]
DDI2_TXP[3]
DDI2_TXP[2]
DDI2_TXP[1]
DDI2_TXP[0]
DDI2_TXN[3]
DDI2_TXN[2]
DDI2_TXN[1]
DDI2_TXN[0]
DDI3_TXP[3]
DDI3_TXP[2]
DDI3_TXP[1]
DDI3_TXP[0]
DDI3_TXN[3]
DDI3_TXN[2]
DDI3_TXN[1]
DDI3_TXN[0]
DMI_TX3
DMI_TX2
DMI_TX1
DMI_TX0
DMI_TX3#
DMI_TX2#
DMI_TX1#
DMI_TX0#
DP_DDPD_TX3_P
DP_DDPD_TX2_P
DP_DDPD_TX1_P
DP_DDPD_TX0_P
DP_DDPD_TX3_N
DP_DDPD_TX2_N
DP_DDPD_TX1_N
DP_DDPD_TX0_N
HDMI_DDI2_CLK_P
HDMI_DDI2_TX0_P
HDMI_DDI2_TX1_P
HDMI_DDI2_TX2_P
HDMI_DDI2_CLK_N
HDMI_DDI2_TX0_N
HDMI_DDI2_TX1_N
HDMI_DDI2_TX2_N
DRXP1
DRXP0
DRXN1
DRXN0
CFG[0:15] Configuration note
Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.
Intel recommends placing test points on the board for CFG pins.
CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:
— 1 = (Default) Normal Operation; No stall.
— 0 = Stall.
CFG[1]: Reserved configuration lane.
CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
— 1 = Normal operation
— 0 = Lane numbers reversed.
CFG[3]: Reserved configuration lane.
CFG[4]: eDP enable:
— 1 = Disabled.
— 0 = Enabled.
CFG[6:5]: PCI Express* Bifurcation
— 00 = 1 x8, 2 x4 PCI Express*
— 01 = reserved
— 10 = 2 x8 PCI Express*
— 11 = 1 x16 PCI Express*
CFG[7]: PEG Training:
— 1 = (default) PEG Train immediately following RESET# de assertion.
— 0 = PEG Wait for BIOS for training.
CFG[19:8]: Reserved configuration lanes.
+VCCST
+3V3_S5
MSI
MICRO-START INT'L CO.,LTD.
Title
CPU-DMI/PEG/DDI/MISC/XDP
Size
Document Number
IH110M
Rev
1.0
Date: Tuesday, July 07, 2015
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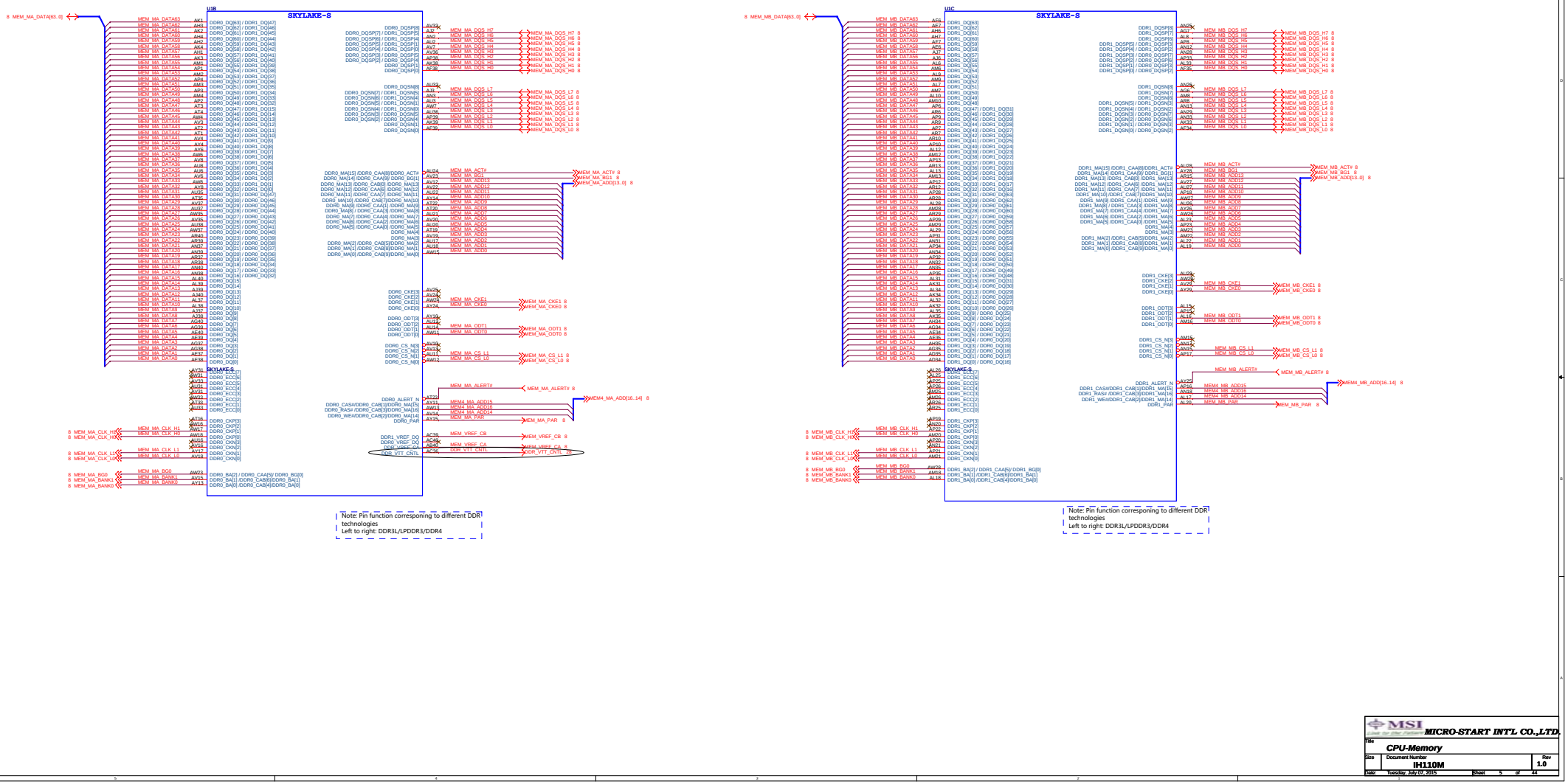

MICRO-START INT'L CO.,LTD.

Title	CPU-Memory	
Size	Document Number	Rev
	IH110M	1.0
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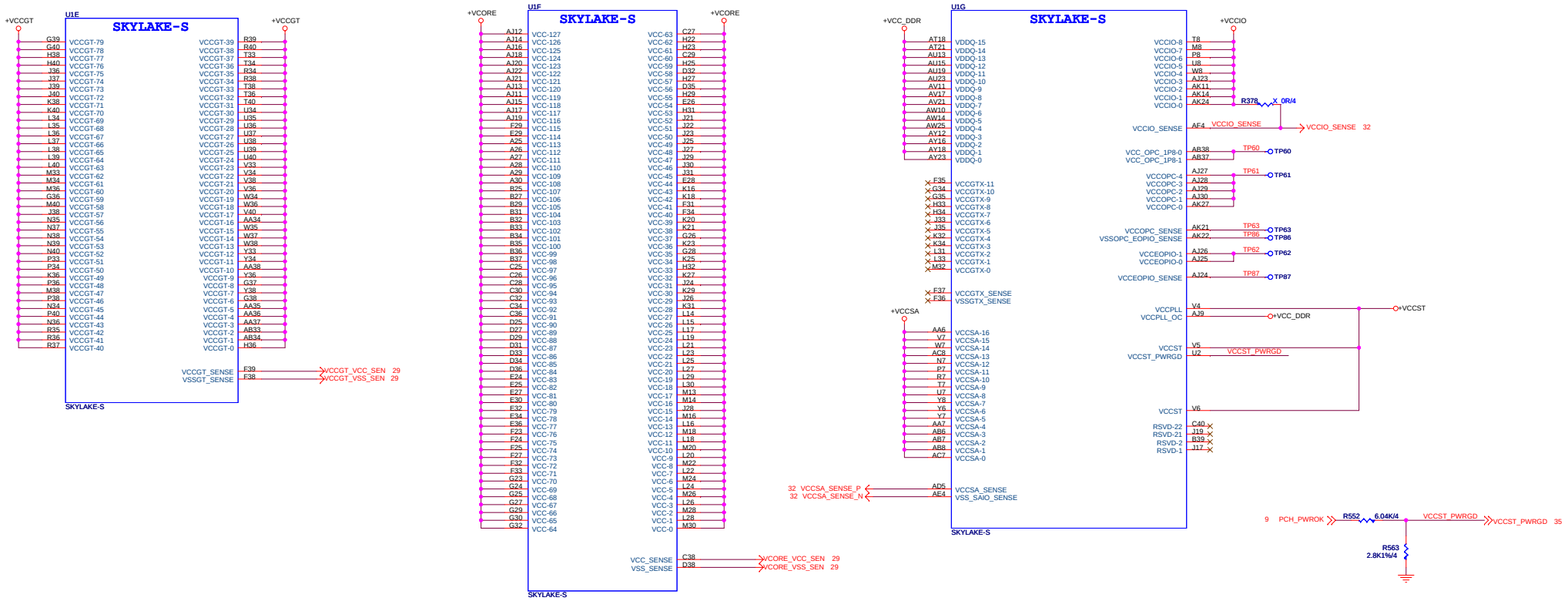

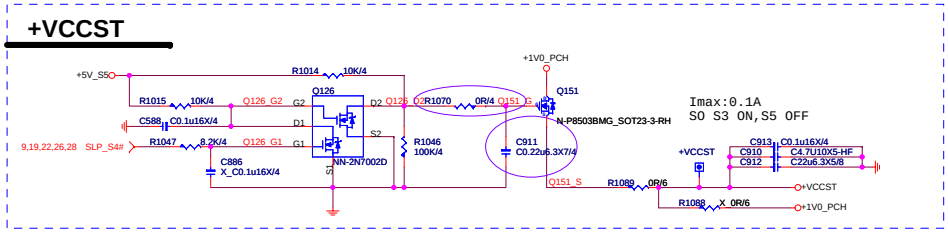

MICRO-START INT'L CO.,LTD.

Title: CPU-Power

Size	Document Number	Rev
	IH110M	1.0

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MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title	**CPU-GND**	
Size	Document Number **IH110M**	Rev **1.0**
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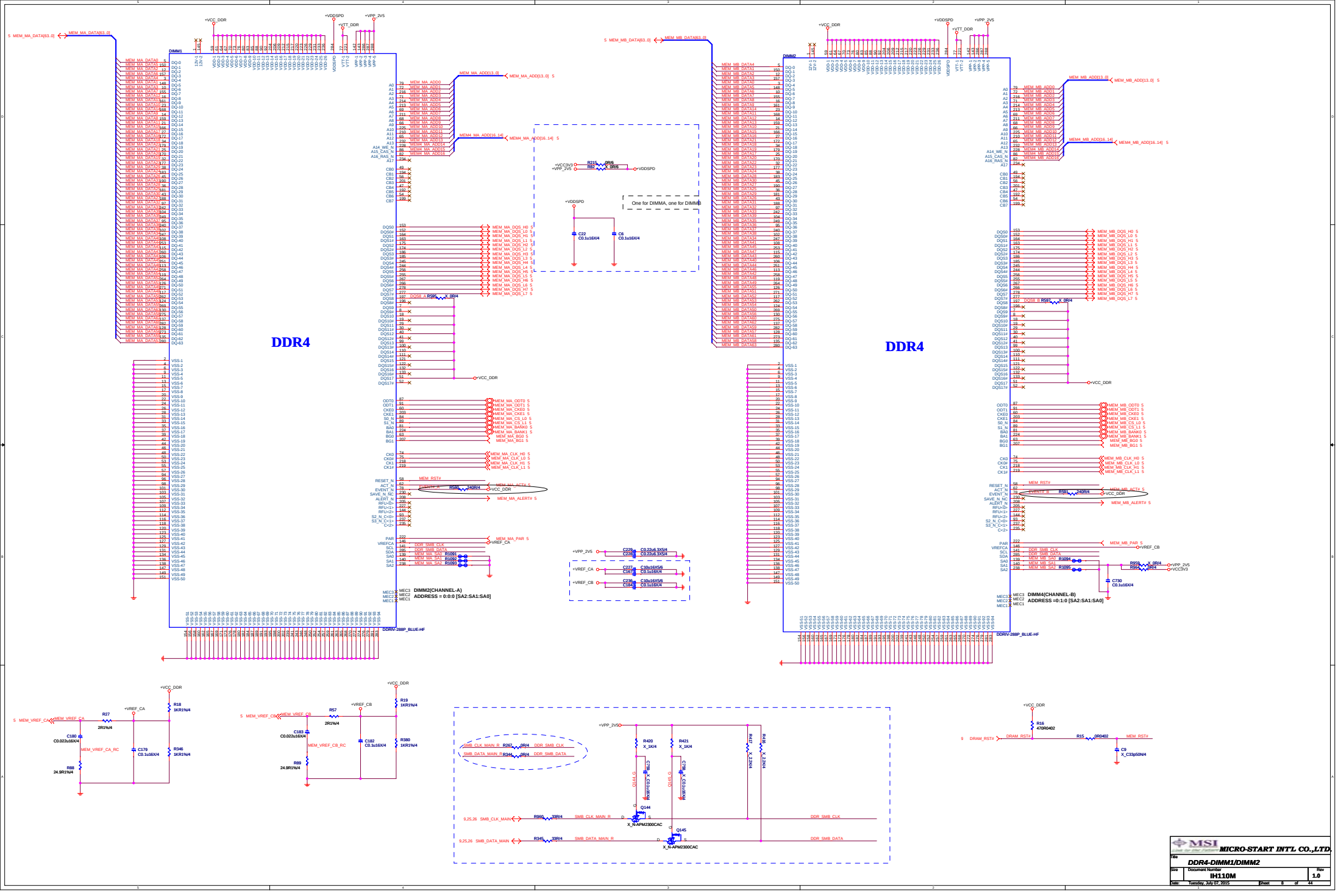
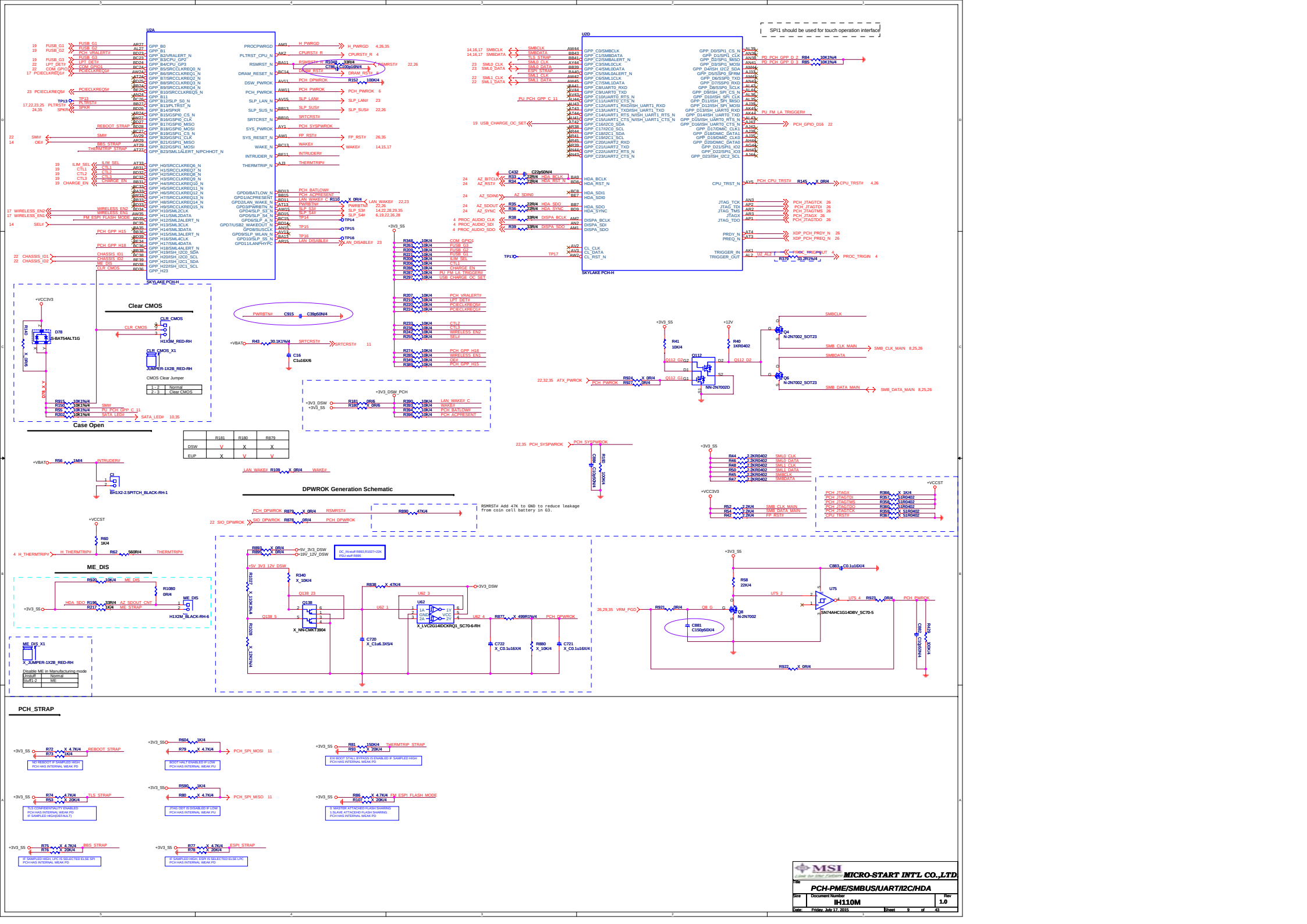

DDR4
DDR4
DIMM1
DIMM2
DIMM2(CHANNEL-A)
ADDRESS = 0:0:0 [SA2:SA1:SA0]
DIMM4(CHANNEL-B)
ADDRESS =0:1:0 [SA2:SA1:SA0]
DDR4V-288P_BLUE-HF
One for DIMMA, one for DIMMB
MICRO-START INT'L CO.,LTD.
DDR4-DIMM1/DIMM2
IH110M
1.0
Tuesday, July 07, 2015


SPI1 should be used for touch operation interface
U2A
SKYLAKE PCH-H
U2D
SKYLAKE PCH-H
Clear CMOS
CLR_CMOS
CLR_CMOS_X1
JUMPER-1X2B_RED-RH
CMOS Clear Jumper
1 - 2 Normal
2 - 3 Clear CMOS
Case Open
DSW V X X
EUP X V V
DPWROK Generation Schematic
RSMRST# Add 47K to GND to reduce leakage from coin cell battery in G3.
ME_DIS
ME_DIS_X1
X_JUMPER-1X2B_RED-RH
Disable ME in Manufacturing mode
Unstuff Normal
Stuff1-2 ME
PCH_STRAP
NO REBOOT IF SAMPLED HIGH PCH HAS INTERNAL WEAK PD
BOOT HALT ENABLED IF LOW PCH HAS INTERNAL WEAK PU
EXI BOOT STALL BYPASS IS ENABLED IF SAMPLED HIGH PCH HAS INTERNAL WEAK PD
TLS CONFIDENTIALITY ENABLED PCH HAS INTERNAL WEAK PD IF SAMPLED HIGH(DEFAULT)
JTAG DOT IS DISABLED IF LOW PCH HAS INTERNAL WEAK PU
0: MASTER ATTACHED FLASH SHARING 1:SLAVE ATTACHED FLASH SHARING PCH HAS INTERNAL WEAK PD
IF SAMPLED HIGH, LPC IS SELECTED ELSE SPI PCH HAS INTERNAL WEAK PD
IF SAMPLED HIGH, ESPI IS SELECTED ELSE LPC PCH HAS INTERNAL WEAK PD
MICRO-START INT'L CO.,LTD
PCH-PME/SMBUS/UART/I2C/HDA
Size
Document Number IH110M
Rev 1.0
Date: Friday, July 17, 2015
Sheet 9 of 43

Except these ports that has annotation, all rest are PCIE port

USB 5/6/7/8/9
PCIE 11/17/18/19/20
Above ports are disabled

PCIE 4 only can be used to support Intel LAN

PCIE 12 only can be used to support Intel LAN

PCIE Port 14/15/16 can only be used to support SATA
PCIE Port 13 can be used to support SATA or Intel LAN

U2B

SKYLAKE PCH-H

U2C

SKYLAKE PCH-H

+3V3_S5

Title	PCH-DMI/PCIE/USB/SATA/DDI
Size	Document Number: IH110M
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Date:	Friday, July 17, 2015
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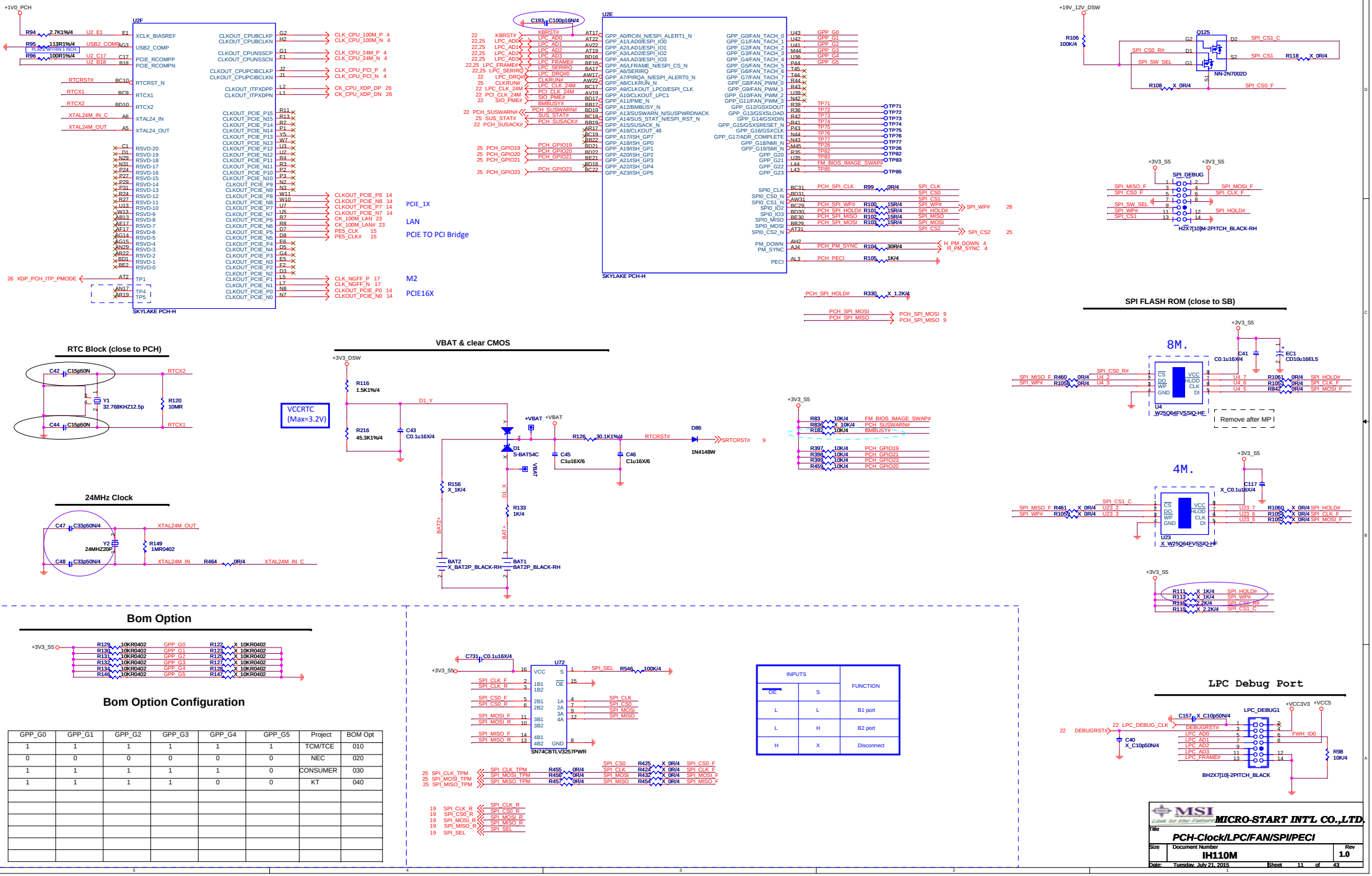
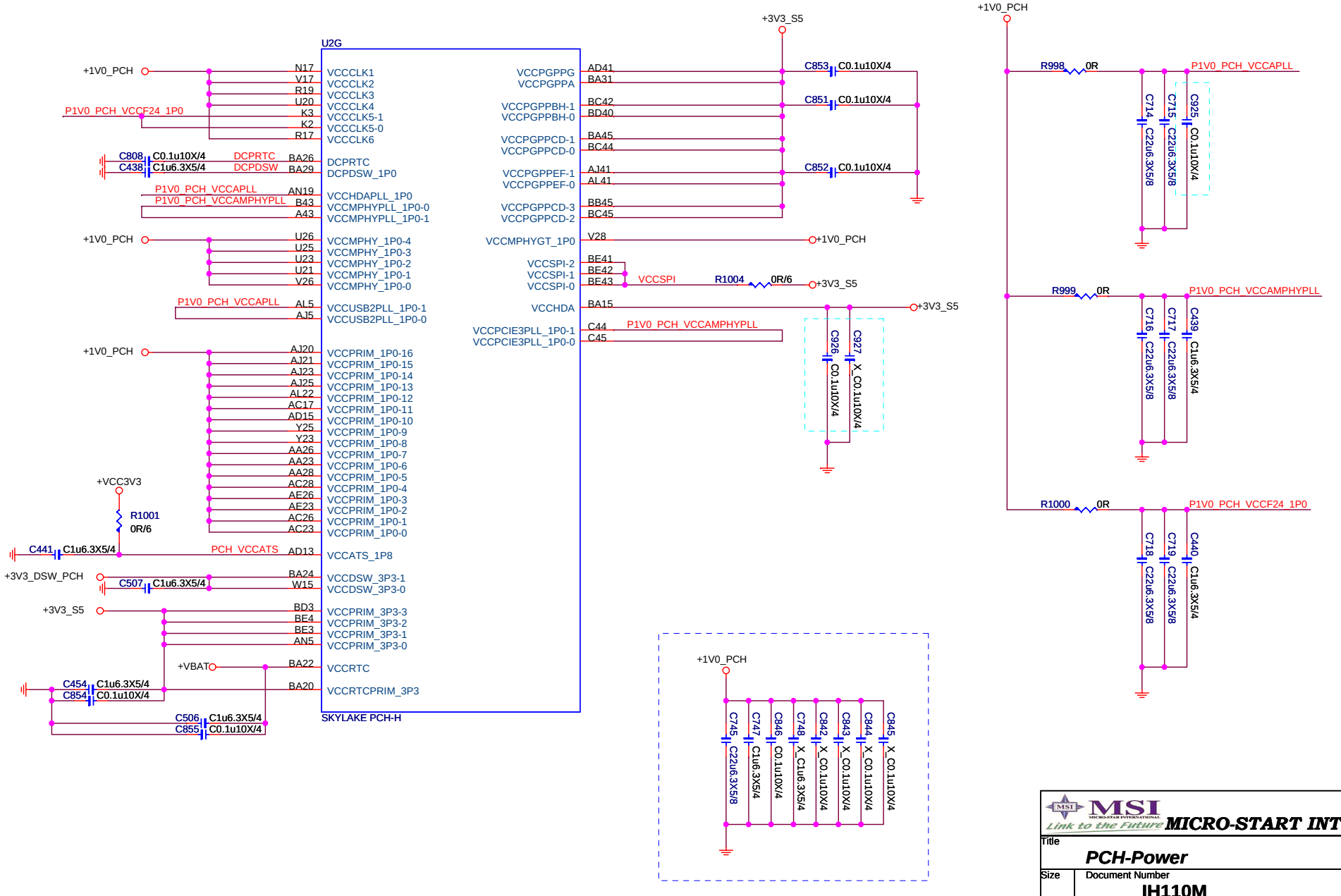
MSI Link to the Future MICRO-START INT'L CO.,LTD.



GPP_G0	GPP_G1	GPP_G2	GPP_G3	GPP_G4	GPP_G5	Project	BOM Opt
1	1	1	1	1	1	TCM/TCE	010
0	0	0	0	0	0	NEC	020
1	1	1	1	1	0	CONSUMER	030
1	1	1	1	0	0	KT	040

INPUTS		FUNCTION
OE	S	
L	L	B1 port
L	H	B2 port
H	X	Disconnect



MICRO-START INT'L CO.,LTD.

Title: PCH-Power

Size	Document Number	Rev
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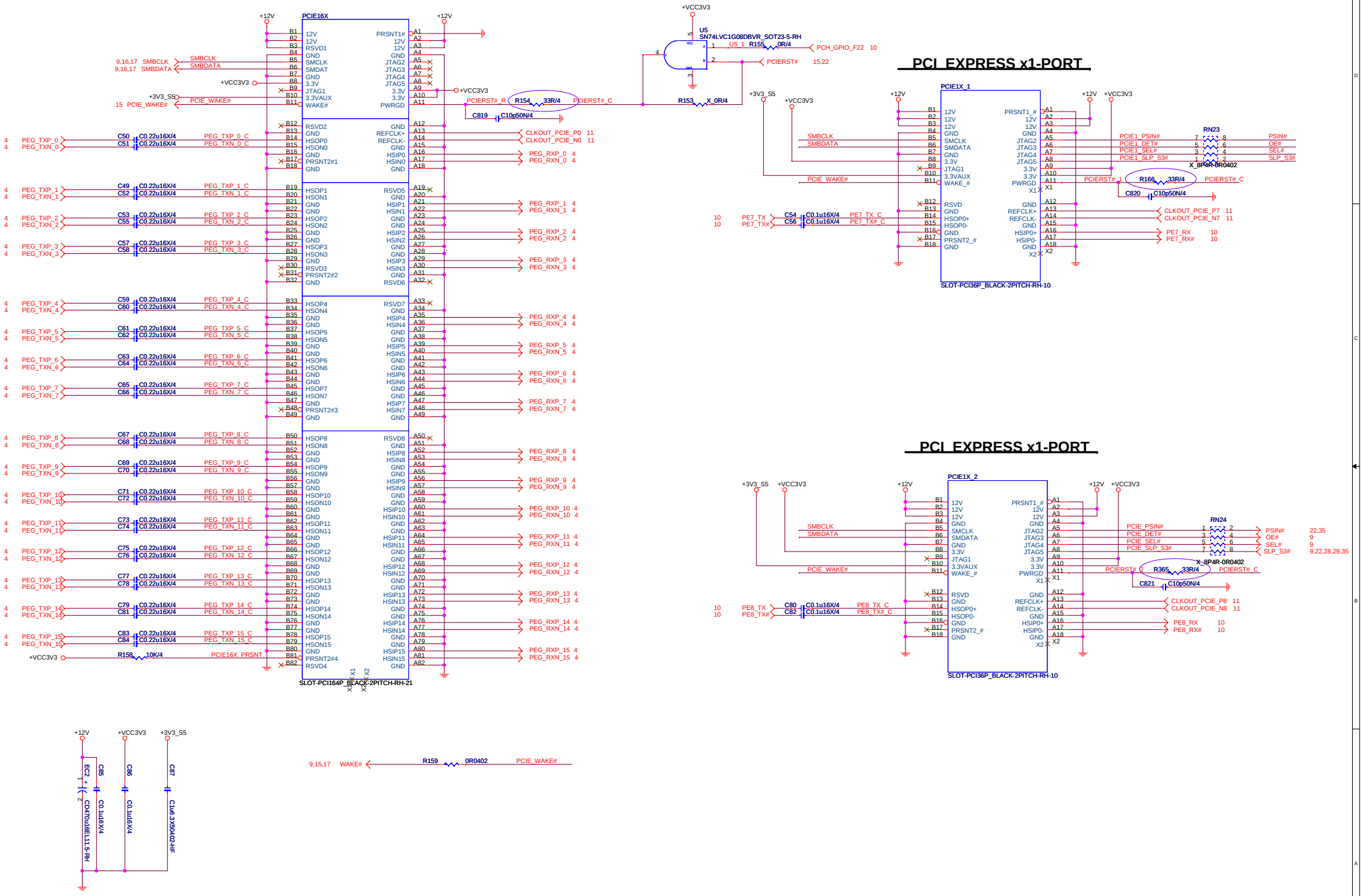
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	PCH-GND	
Size	Document Number: IH110M	Rev: 1.0
Date: Friday, July 17, 2015	Sheet 13 of 43	

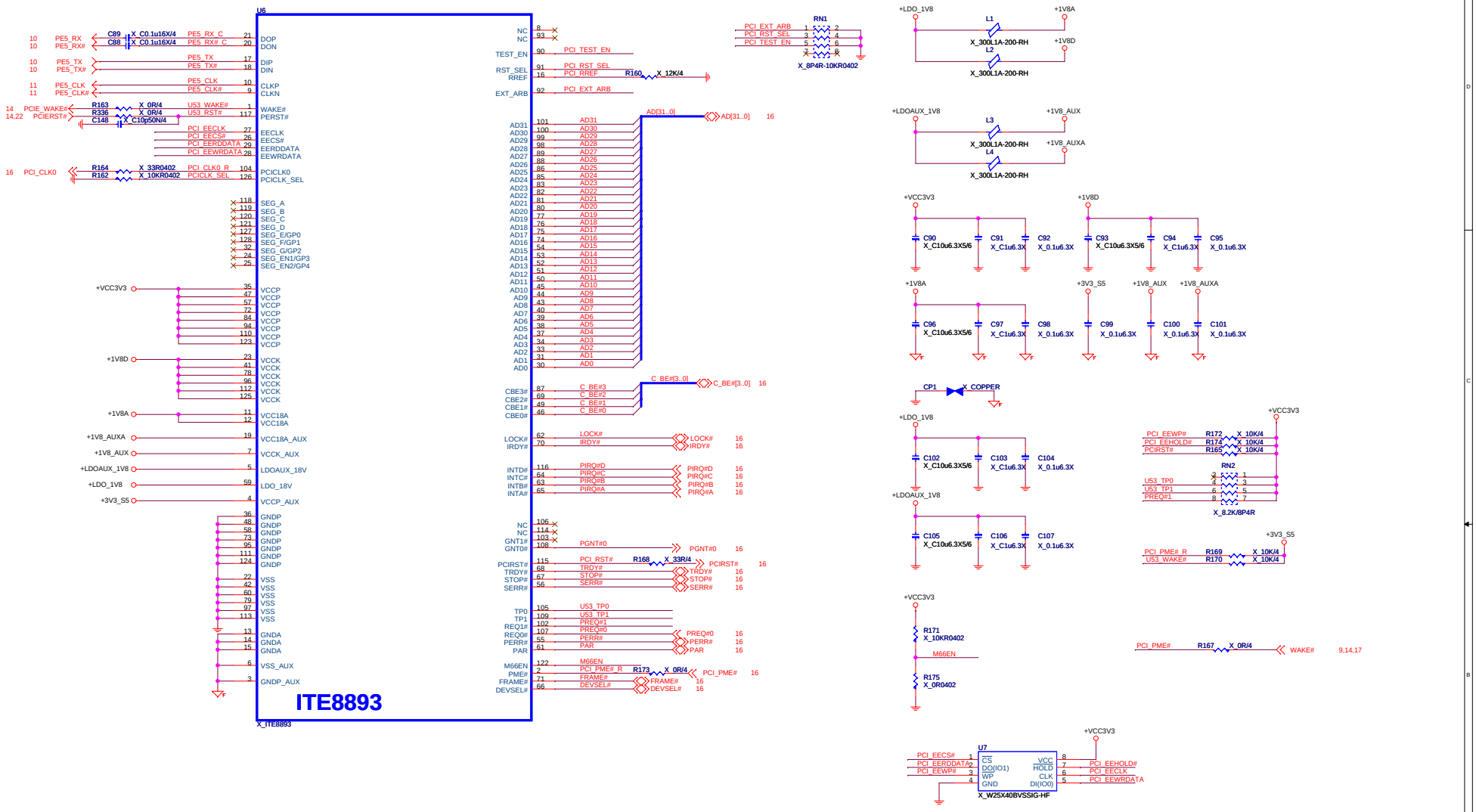
PCI_EXPRESS X16 SLOT



PCI_EXPRESS x1-PORT

PCI_EXPRESS x1-PORT

MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	PCIE x16/x1 slot		
Size	Document Number IH110M		Rev 1.0
Date: Friday, July 17, 2015	Sheet 14 of 43		

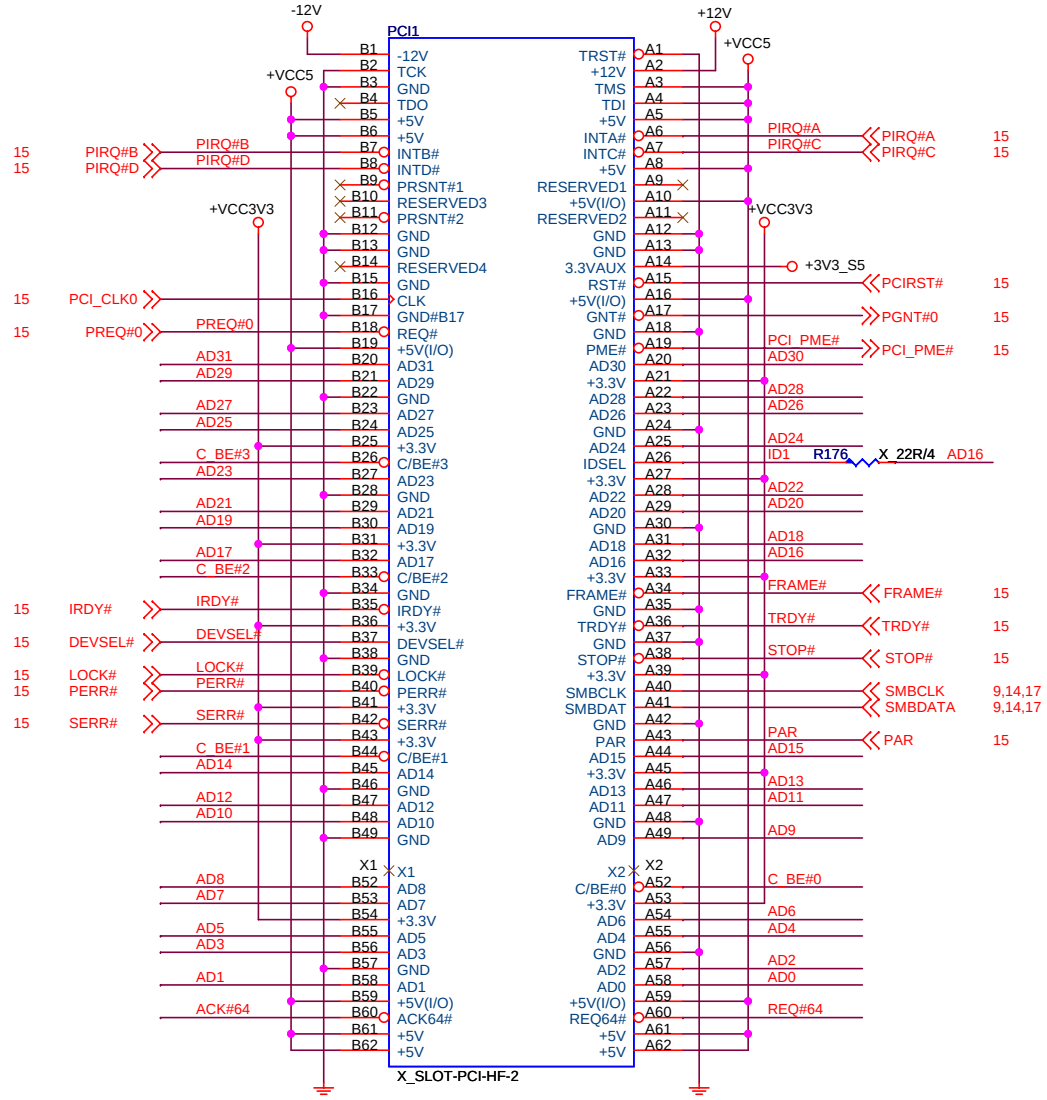


MSI MICRO-START INT'L CO.,LTD.

Title: PCIE To PCI Bridge

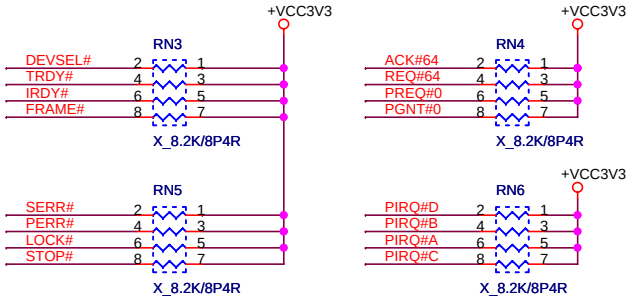
Size	Document Number	Rev
	IH110M	1.0

Date: Tuesday, July 07, 2015 Sheet 15 of 43

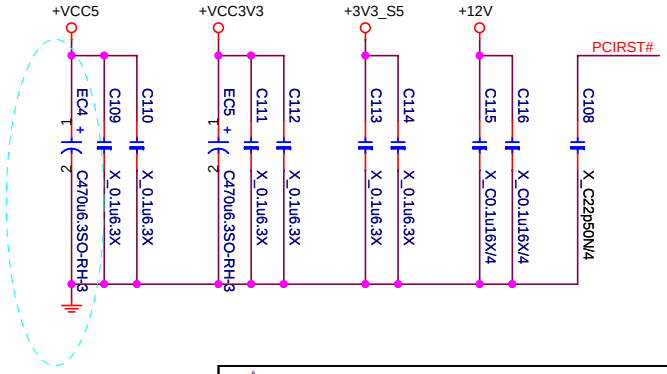


IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI PULL-UP / DOWN RESISTORS



PCI slot		
+3VSB	(wake)	- 375mA
+3VSB	(no wake)	- 20mA
+3.3V		- 7.6A
+5V		- 5A
+12V		- 0.5A



MSI MICRO-STAR INTERNATIONAL Link to the Future	MICRO-START INT'L CO.,LTD.		
Title: PCI Slot			
Size	Document Number: IH110M		Rev: 1.0
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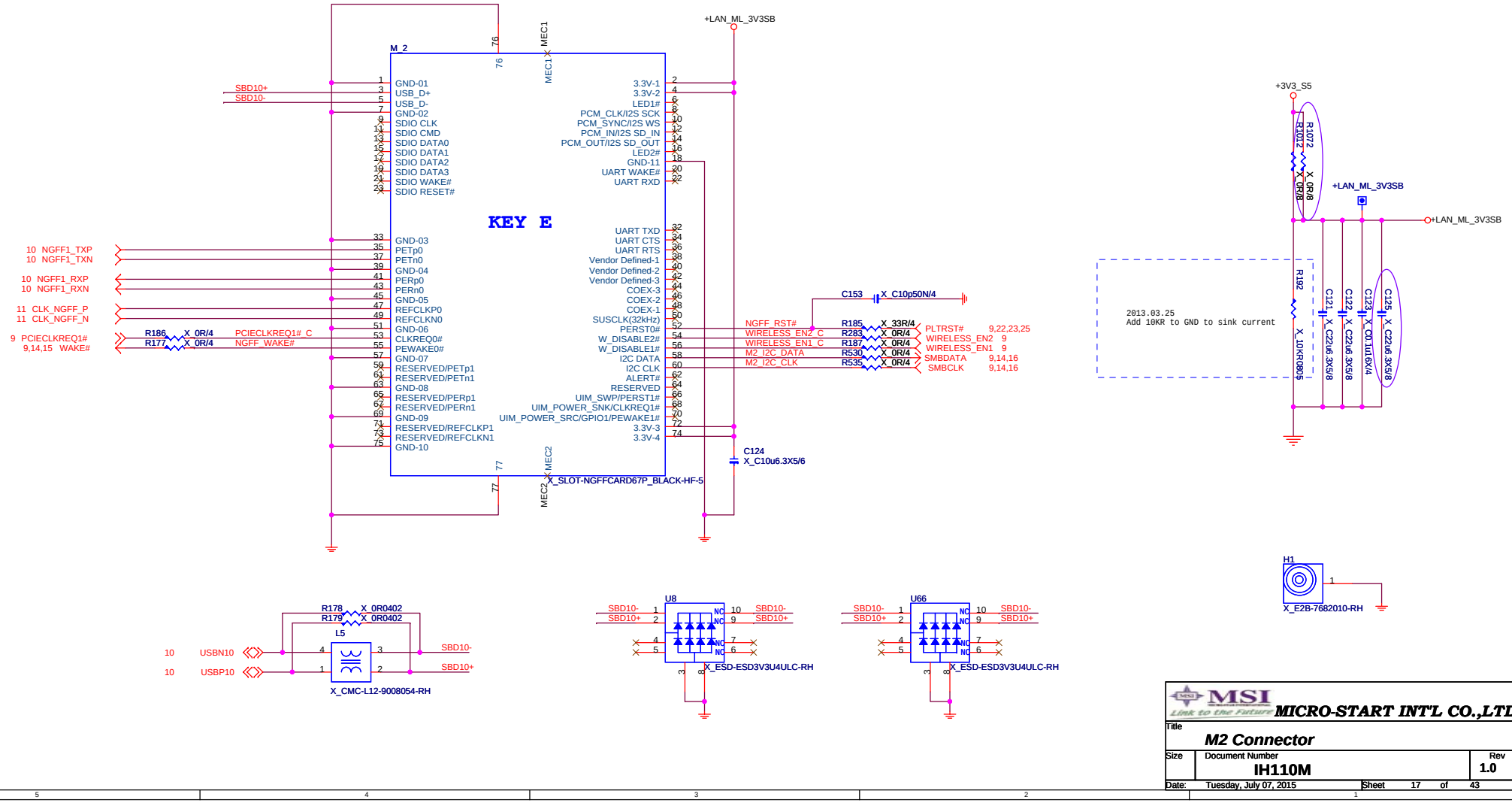
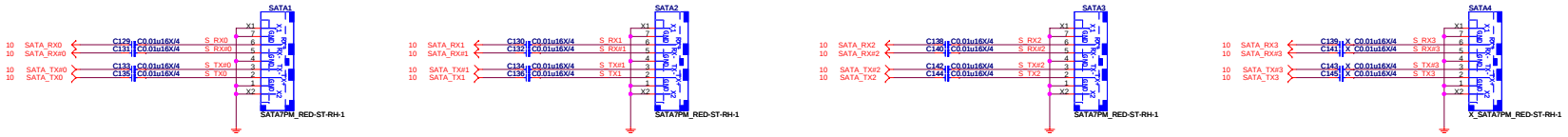
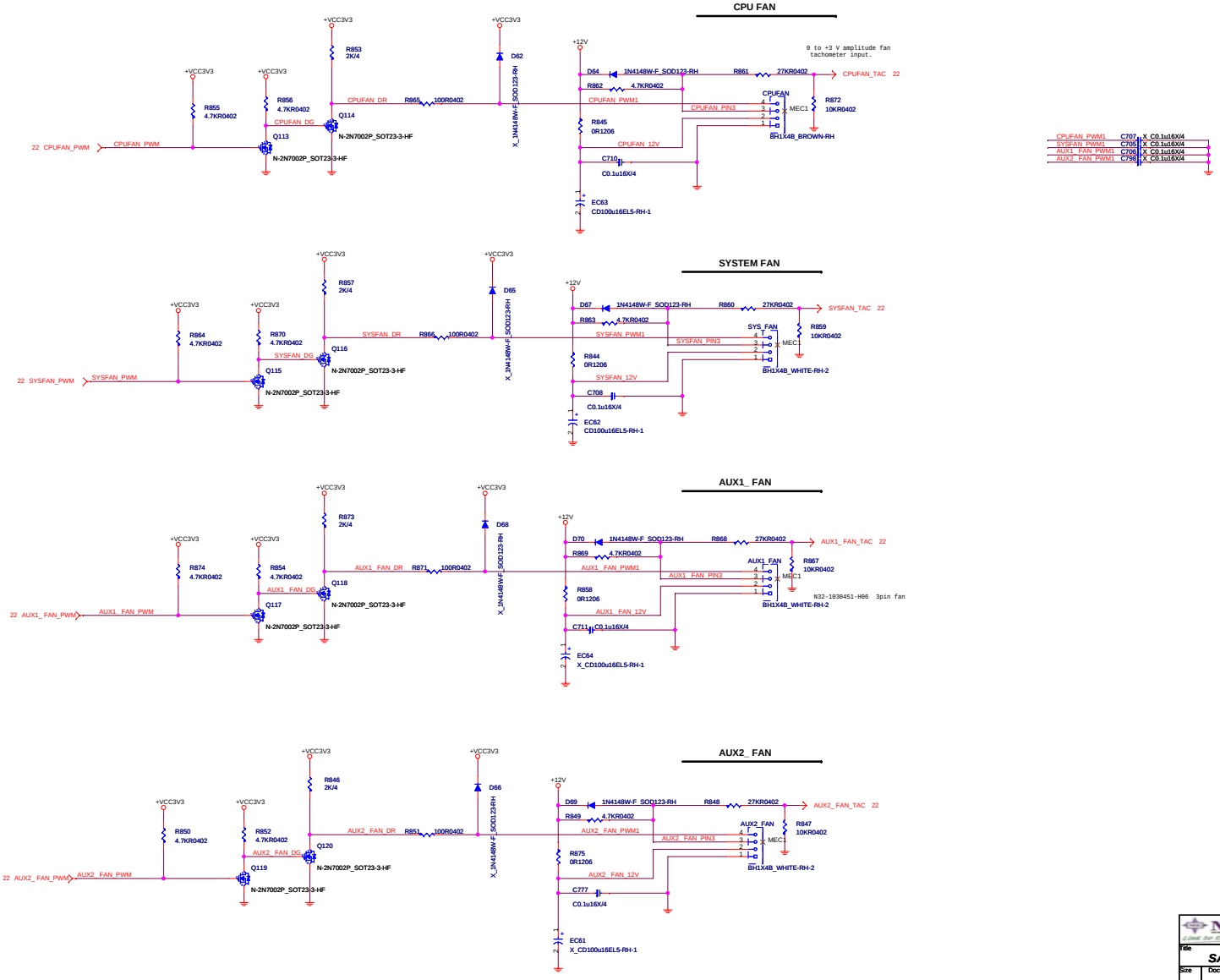


MICRO-START INT'L CO.,LTD.

Title	M2 Connector	
Size	Document Number: IH110M	Rev: 1.0
Date: Tuesday, July 07, 2015	Sheet 17 of 43	

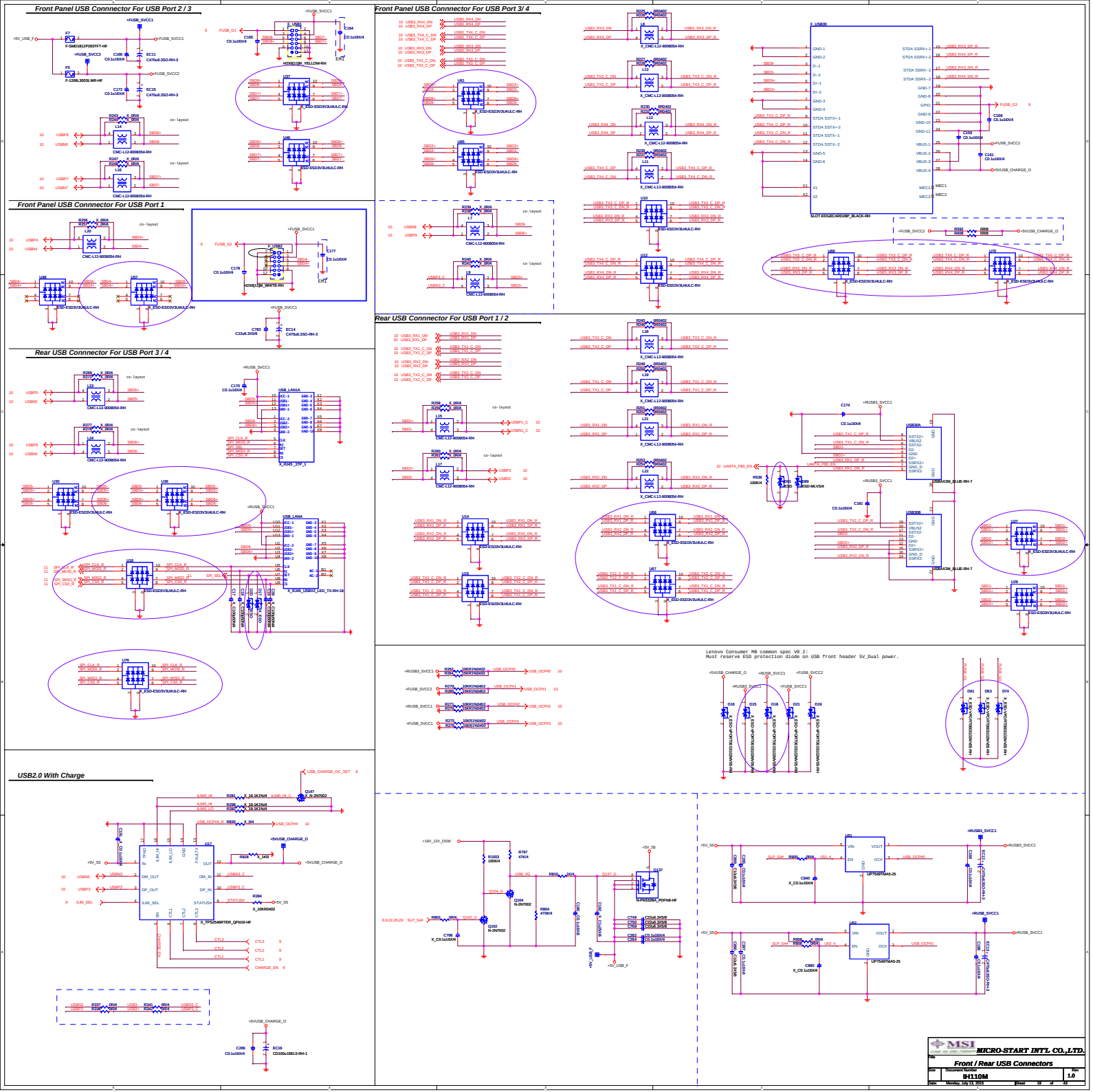


CPU FAN /SYSTEM FAN /POWER FAN

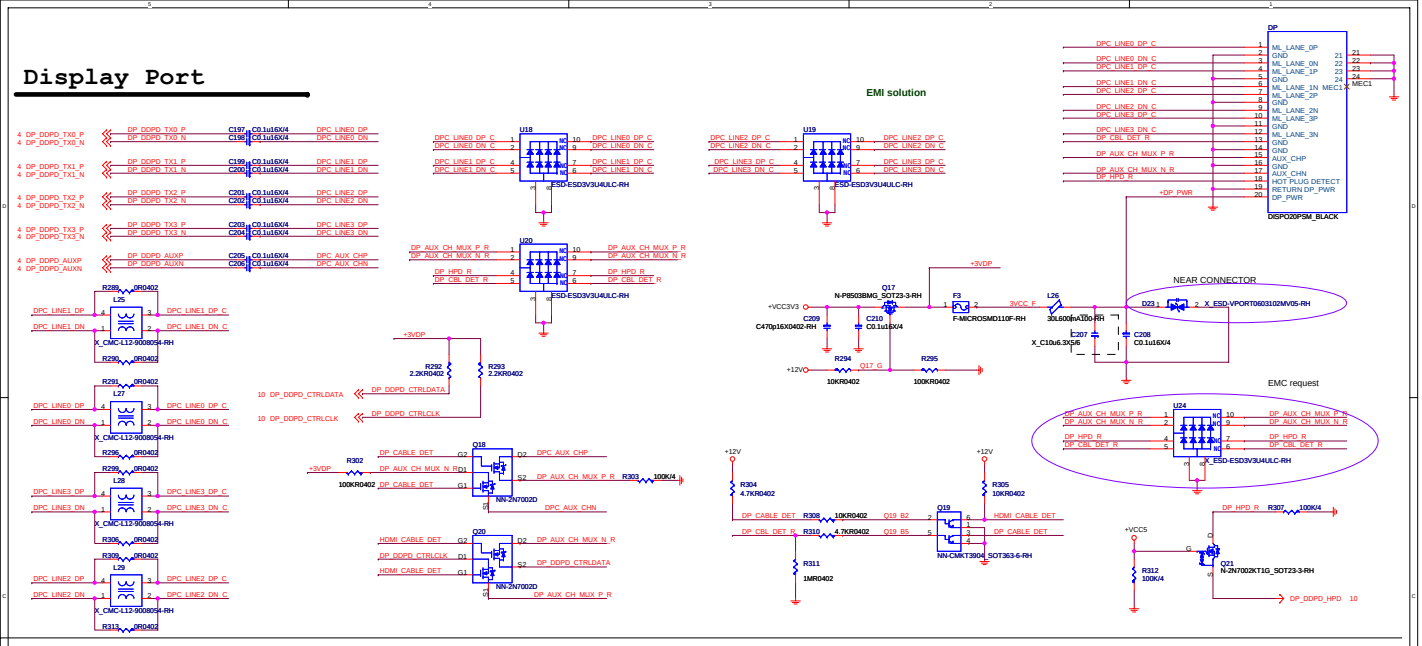


MSI MICRO-START INTL CO.,LTD.

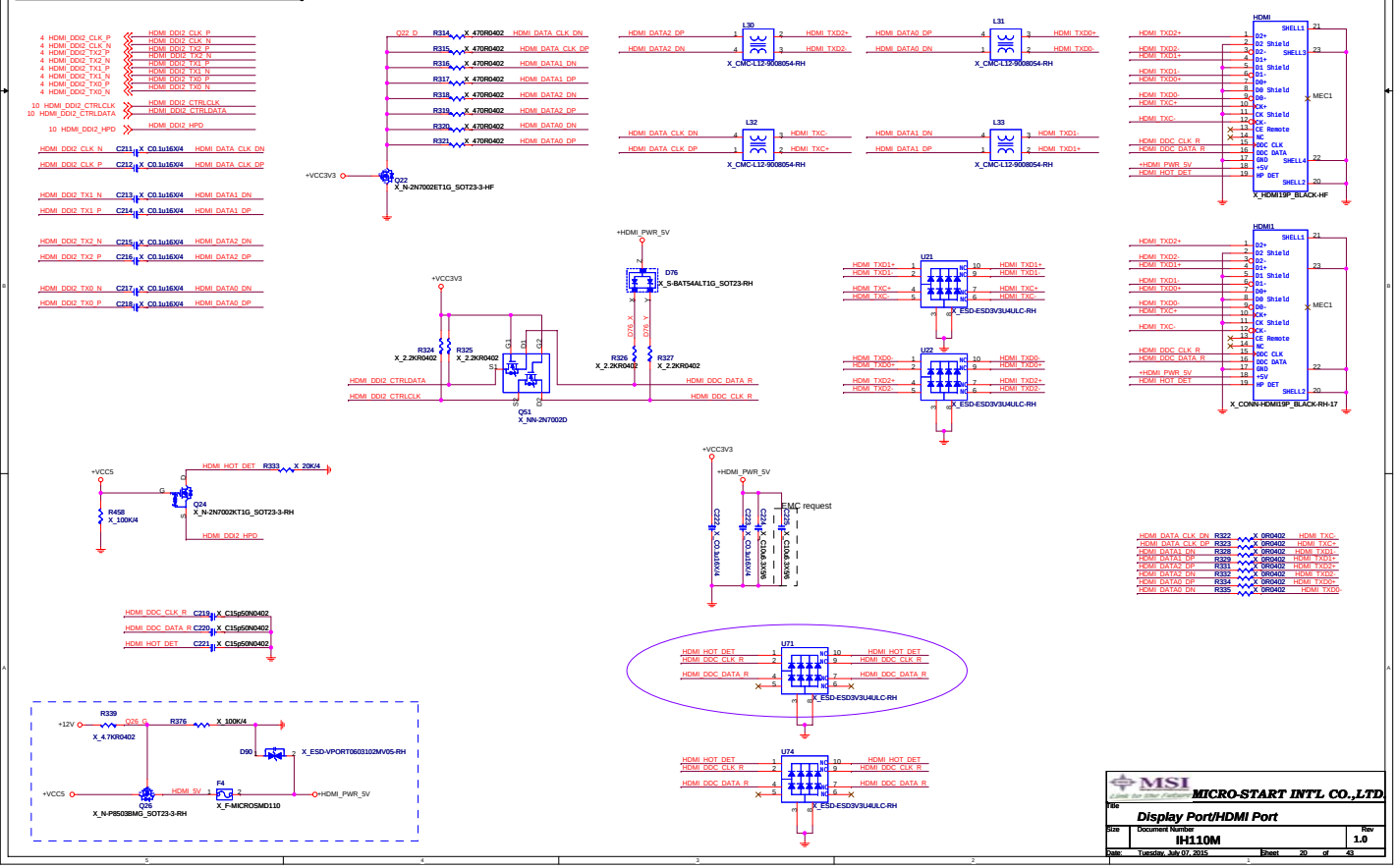
Title	SATA/FAN	
Size	Document Number: IH110M	Rev: 1.0
Date: Tuesday, July 07, 2015	Sheet 18 of 43	


Front Panel USB Connnector For USB Port 2 / 3
Front Panel USB Connnector For USB Port 3/ 4
Front Panel USB Connnector For USB Port 1
Rear USB Connnector For USB Port 3 / 4
Rear USB Connnector For USB Port 1 / 2
USB2.0 With Charge
Lenovo Consumer MB common spec V0 2:
Must reserve ESD protection diode on USB front header 5V_Dual power.
MICRO-START INT'L CO.,LTD.
Front / Rear USB Connectors
IH110M
1.0
Monday, July 13, 2015

Display Port



HDMI Port



MSI	MICRO-START INTL CO.,LTD.		
Title	Display Port/HDMI Port		
Size	Document Number		Rev
	IH110M		1.0
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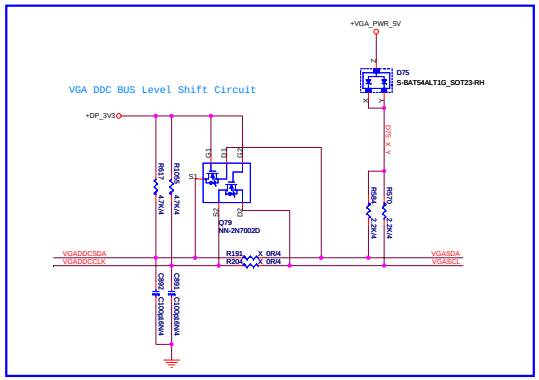

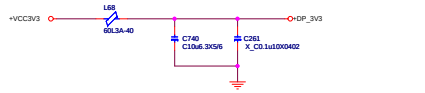

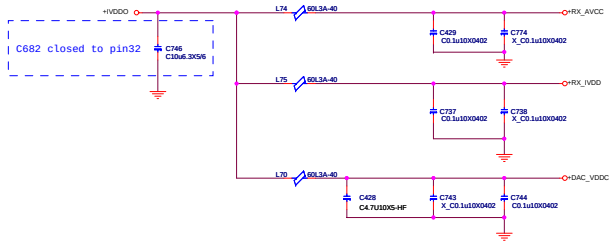

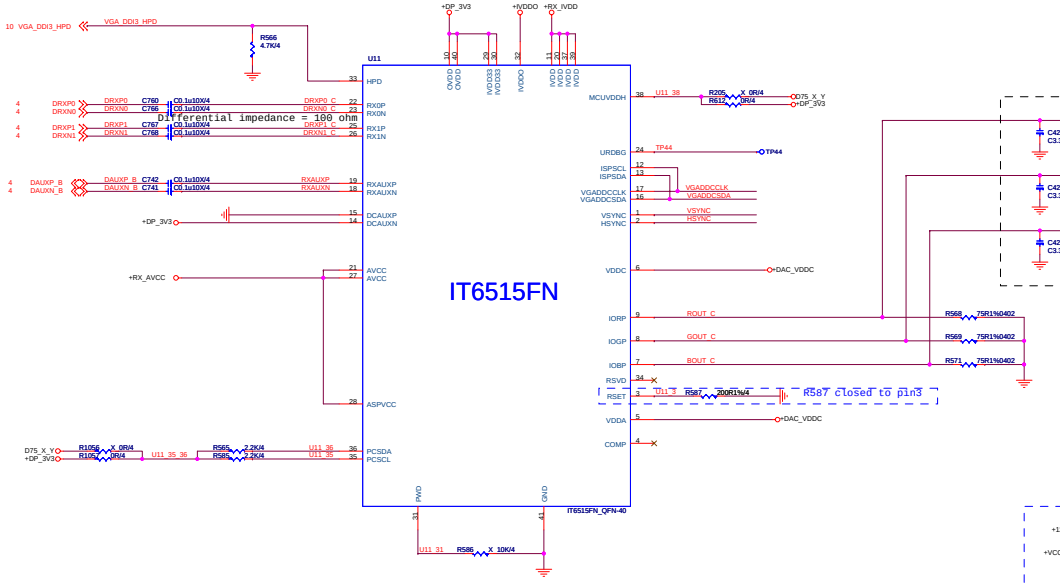

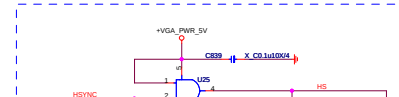

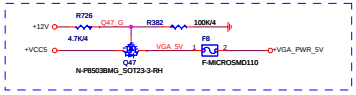

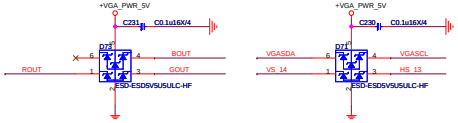

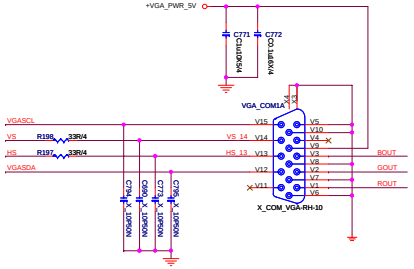

MSI MICRO-STAR INTL CO.,LTD

Title	VGA	
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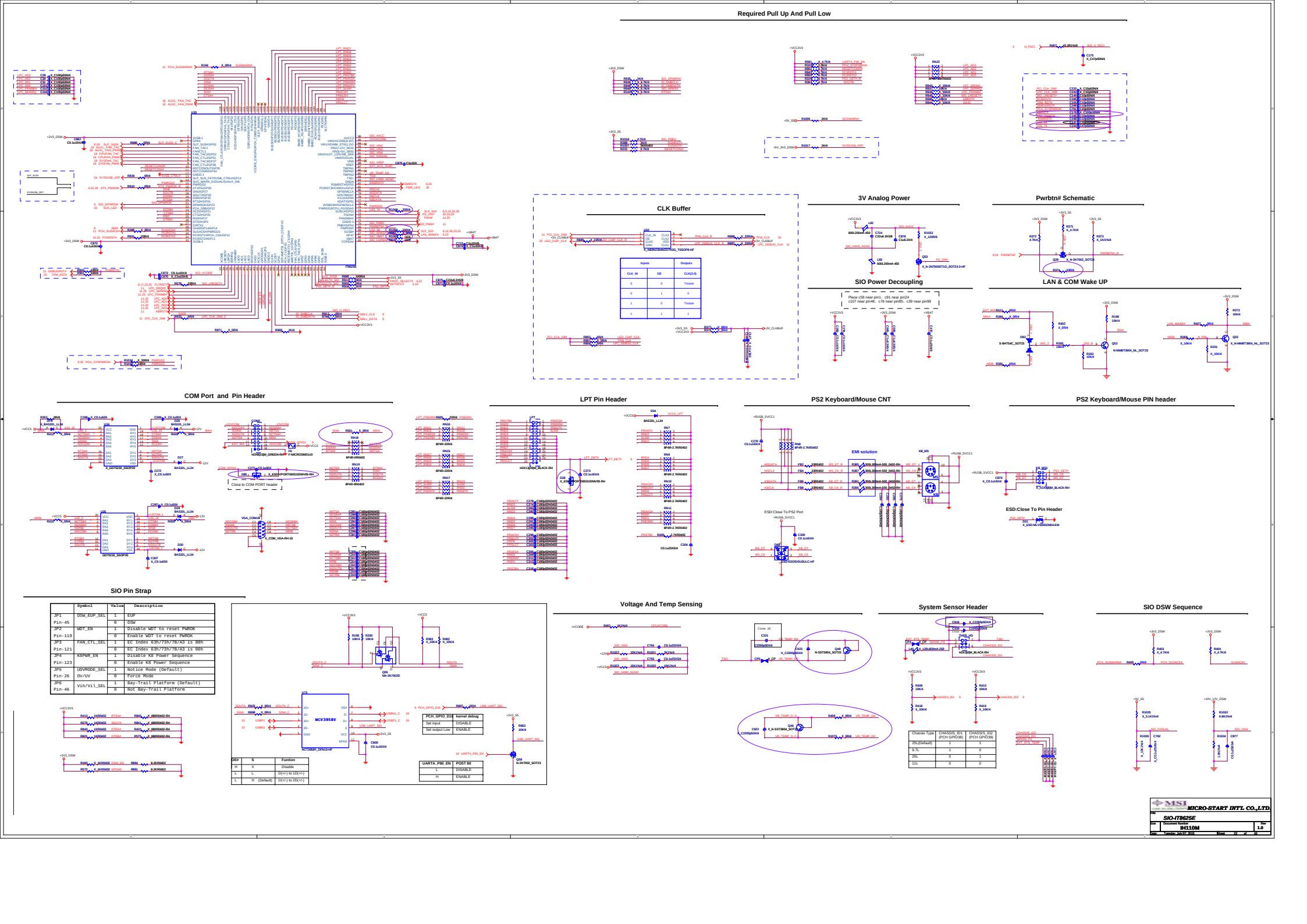
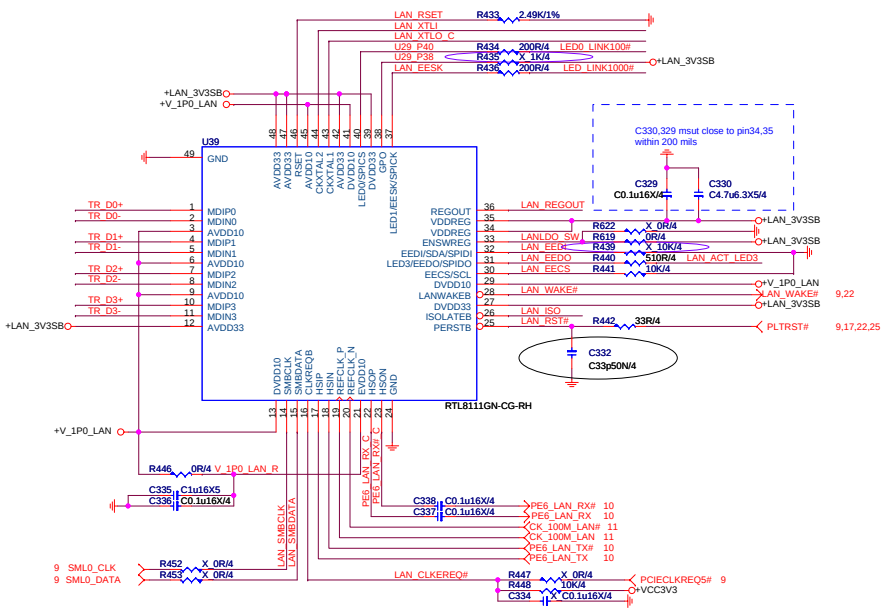
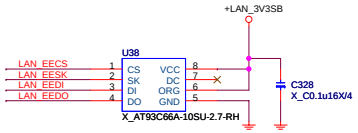

Required Pull Up And Pull Low
CLK Buffer
3V Analog Power
Pwrbtn# Schematic
SIO Power Decoupling
LAN & COM Wake UP
COM Port and Pin Header
LPT Pin Header
PS2 Keyboard/Mouse CNT
PS2 Keyboard/Mouse PIN header
SIO Pin Strap
Voltage And Temp Sensing
System Sensor Header
SIO DSW Sequence
MICRO-START INTL CO.,LTD.
SIO-IT8625E
IH110M
1.0

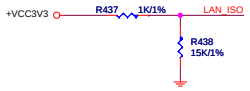
Gigabit LAN RTL8111E-VC Co-lay RTL8111GN

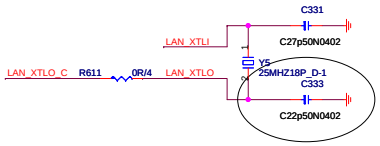
RTL8111E-VC is pin to pin compatible with RTL8111GN.
The two chips can change each other without any component change.





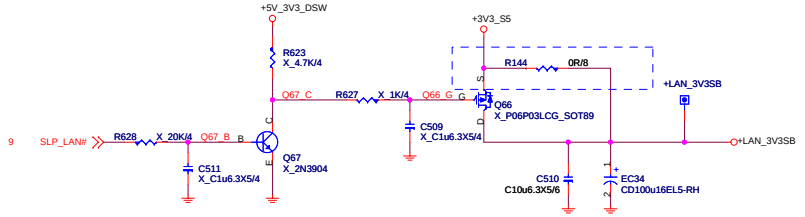
(58mA+289mA)

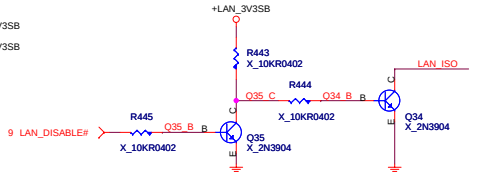




LAN Power

3.3V - 1.2A - 4W

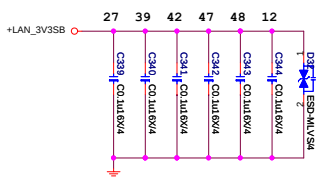




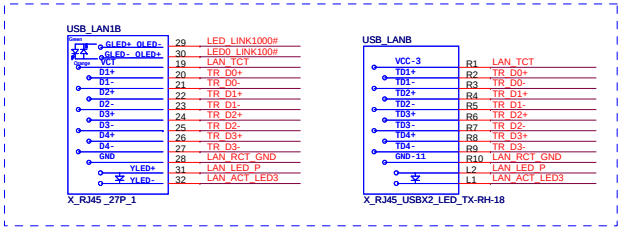
WOL	status	Yellow	Grn/Org
don't care	No Link	off	off
off	S3/S4/S5	off	off
on	S3/S4/S5	off	off
on	10M,inactive		off
on	10M,active		off
on	100M,inactive		
on	100M,active		
on	1G,inactive		
on	1G,active		

always on
always on
always on
blinking

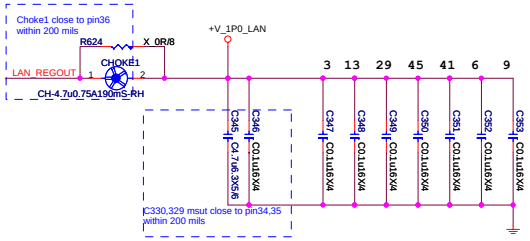
Place Near Pin



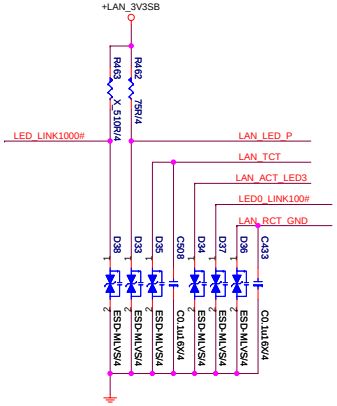
LAN Connector



Place Near Pin

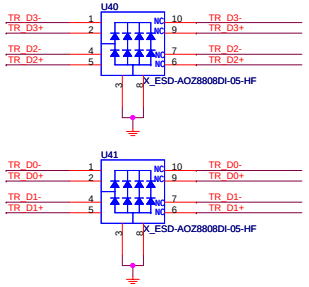


ESD

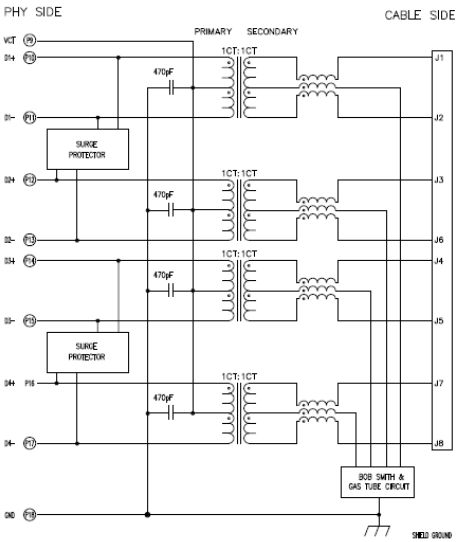


EMI solution: can be unmounted if LAN connector has surge protect

ESD



SCHEMATIC



MSI	MICRO-START INT'L CO.,LTD.
Title	LAN-RTL8111GN/RTL8111E-VC
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Rev	1.0
Date:	Friday, July 17, 2015
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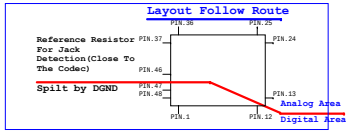
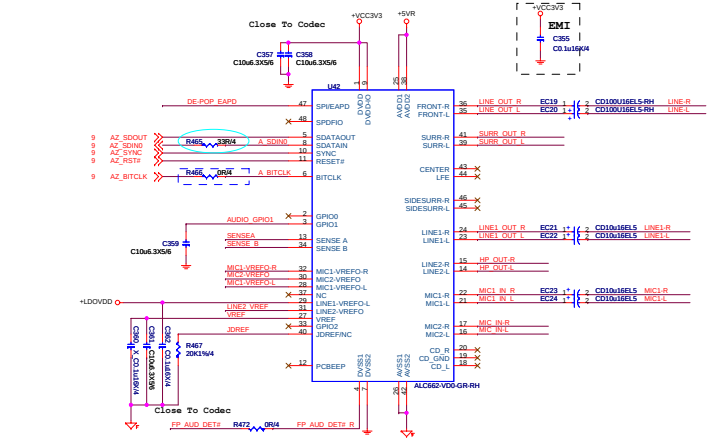
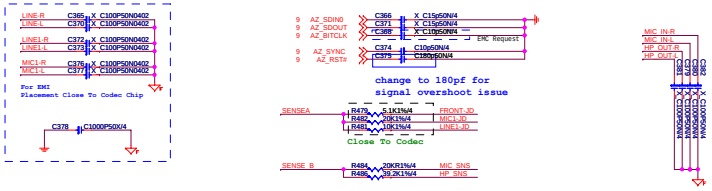
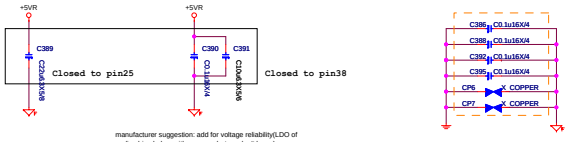
Azalia Codec - ALC662-VD

removed ALC662VC co-lay schematic on 0D



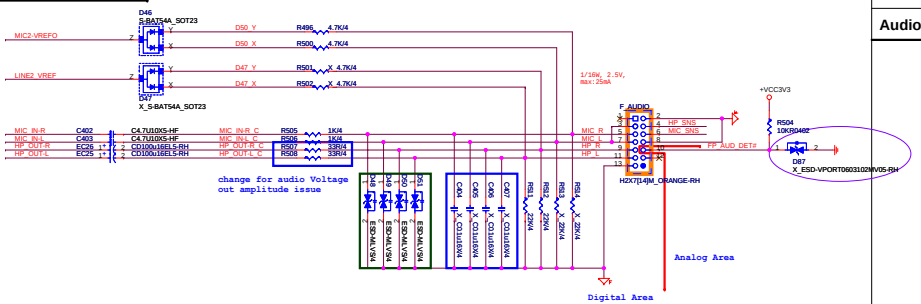






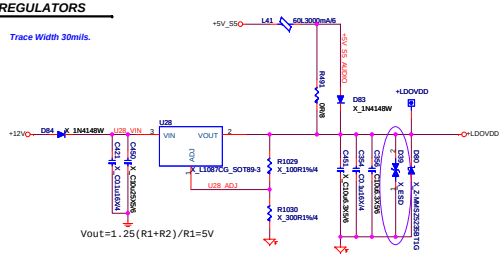
EMC Request

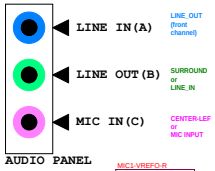
Front Audio Jack



AUDIO CODE REGULATORS

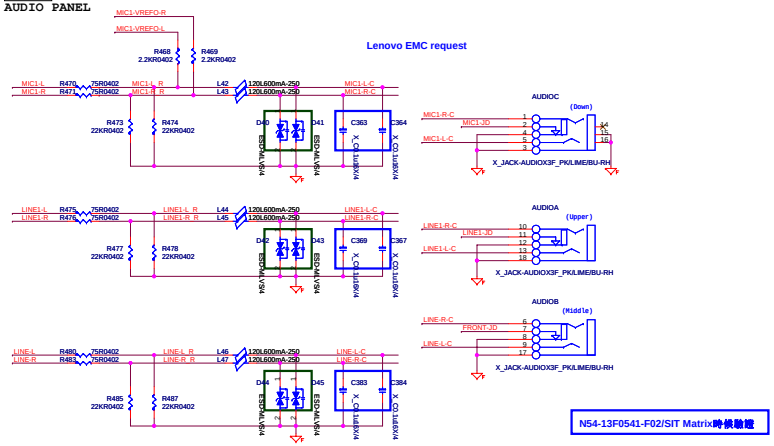
Trace Width 30mils.





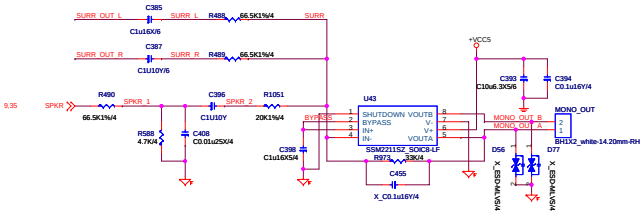
AUDIO PANEL

Lenovo EMC request

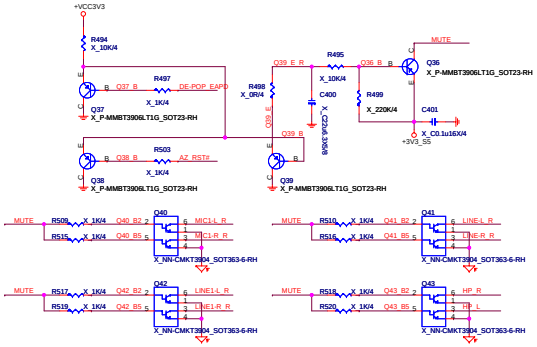


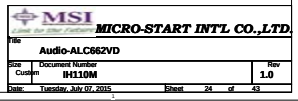
N54-13F0541-F02/SIT Matrix時候驗證

MONO Amplifier

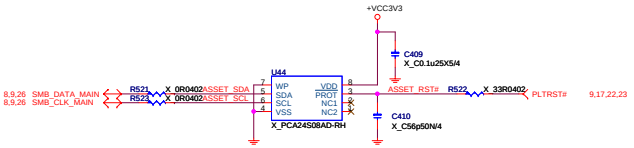


Audio DE-POP

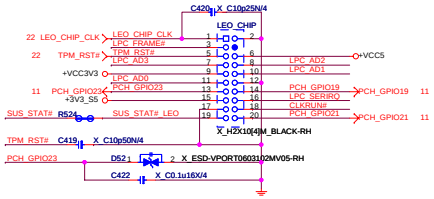




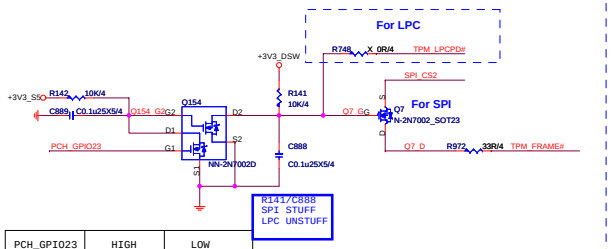
Asset ID



TCM Header

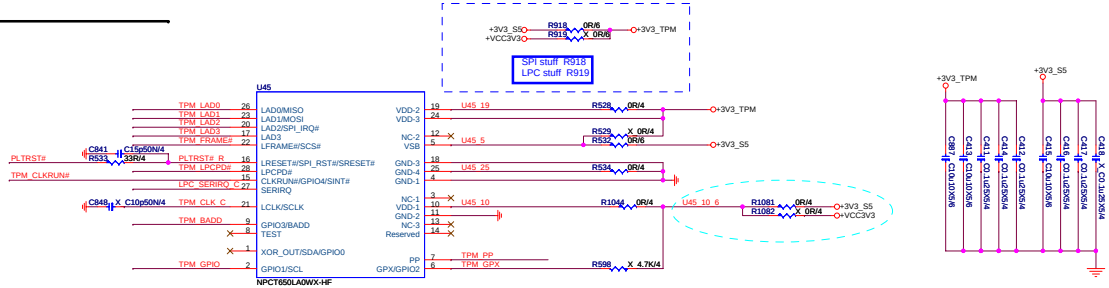


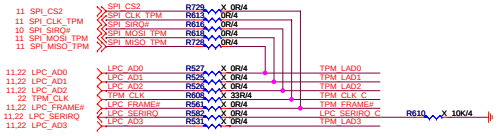
TPM disable circuit

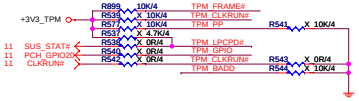


PCH_GPIO23	HIGH	LOW
TPM	ENABLE	DISABLE

TPM







	R533	R528	R529	R532	R534	R729	R613	R616	R618	R728	R527	R525	R526	R608	R561	R582	R531	R537	R538	R540	R542	R543	R539	R577	R541	R544	R598	R610	C841	C412	C414	C411	C413	C415	C416	C417	C418	R899	C848	C887	R142	C889	Q154	R141	R748	C888	Q7	R972	R918	R919	R1044	R1081	R1082
ST----ST33HTPM0028ASTL(SPI)	V	X	X	X	X	X	V	V	V	V	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	V	X	V	X	V	V	V	X	X	V	X	V	V	V	V	V	X	V	V	V	V	X	X	V	X
NPC----NPCT650LA0WX(SPI)	V	V	X	V	V	X	V	V	V	V	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	V	V	X	V	V	V	V	V	X	V	X	V	V	V	V	V	X	V	V	V	V	X	V	V	X
NPC----NPCT650LA0WX(LPC)	V	V	X	V	V	X	X	X	X	X	V	V	V	V	V	V	V	X	X	X	X	V	X	X	X	X	X	V	X	V	V	V	V	V	V	X	X	V	V	V	V	V	V	X	V	V	V	V	X	V	V	X
Nationz----ZH320TC(LPC)	V	V	X	X	V	X	X	X	X	X	V	V	V	V	V	V	V	X	X	X	V	X	X	V	X	X	X	V	X	V	V	V	V	V	V	X	X	V	V	V	V	V	V	X	V	V	V	V	X	V	V	X
Infineon----SLB9660(LPC)	V	V	V	X	V	X	X	X	X	X	V	V	V	V	V	V	V	X	X	X	X	X	X	X	X	X	X	V	X	V	X	V	V	V	V	X	X	V	V	V	V	V	V	X	V	V	V	V	X	V	V	X

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Title	TPM & Asset ID		
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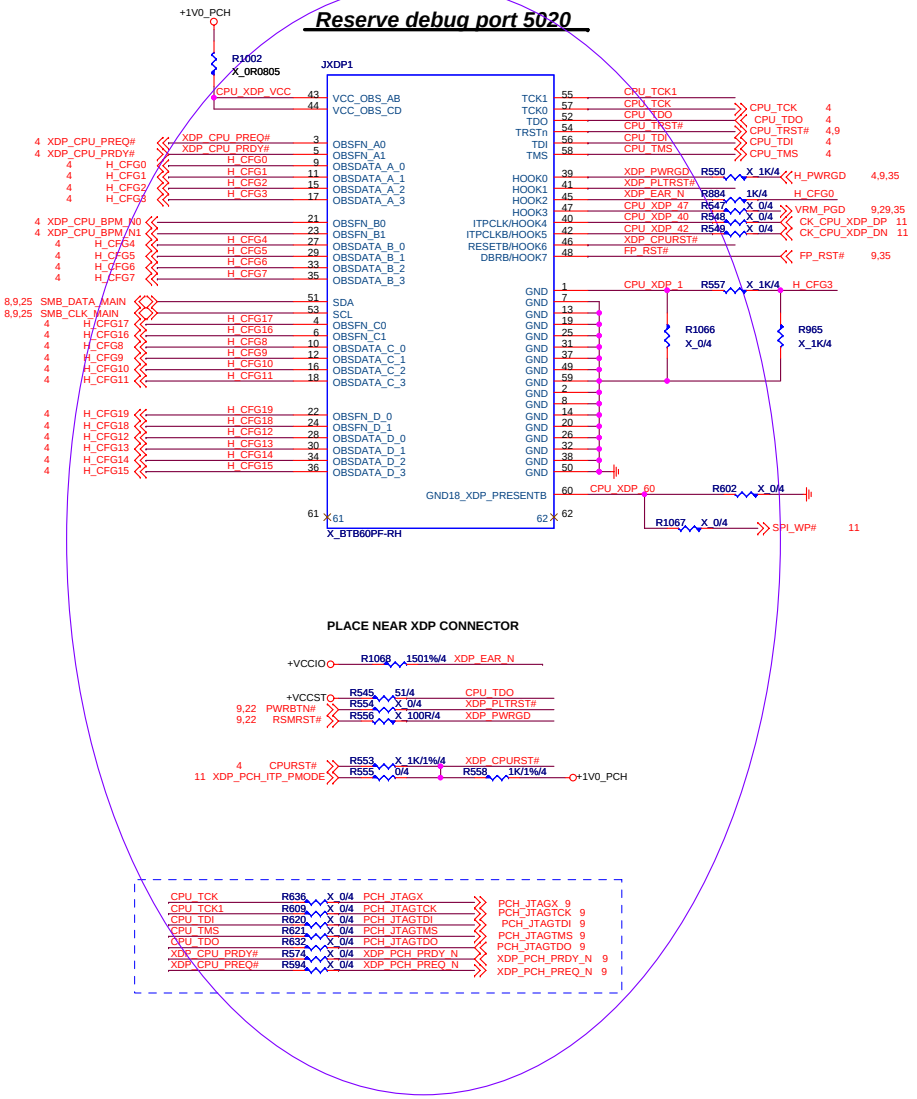
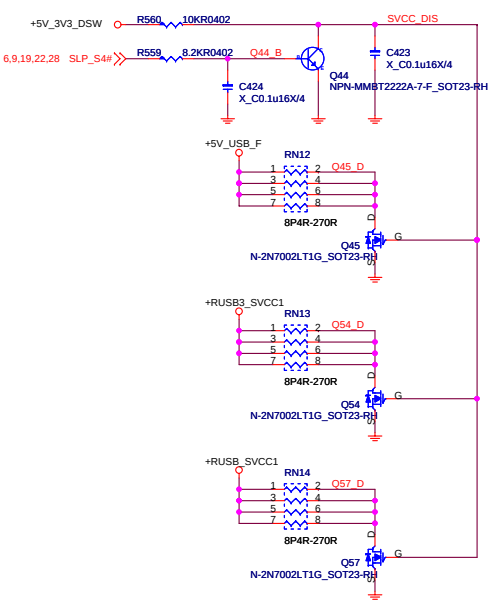
Date:	Monday, July 13, 2015	Sheet 25 of 43	

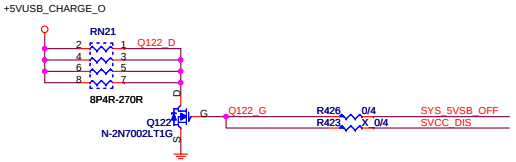
Reserve debug port 5020

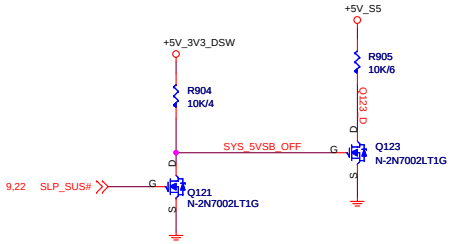


PLACE NEAR XDP CONNECTOR

USB power discharge circuit



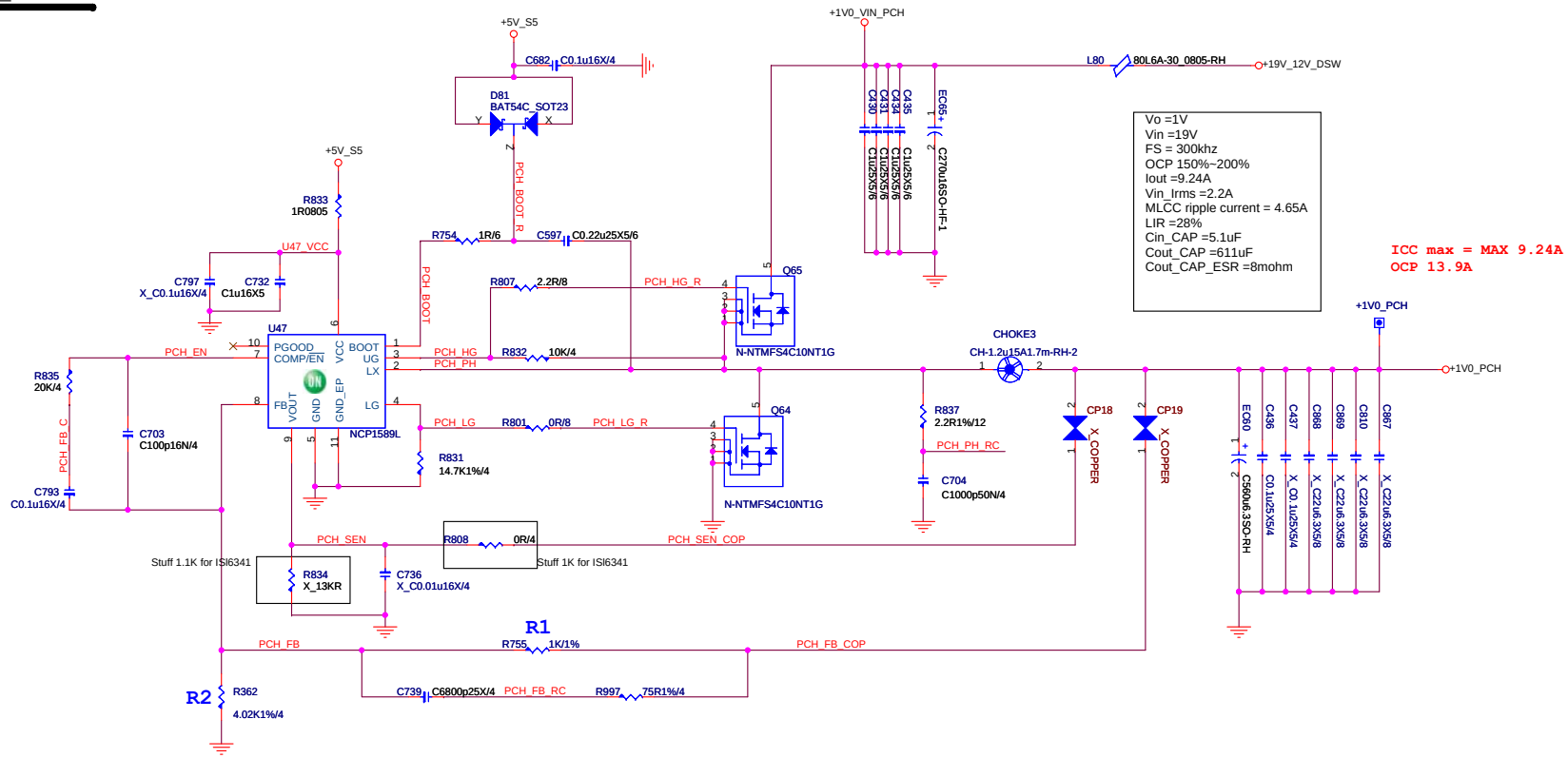




Power Supply in mounted

MSI Link to the Future	MICRO-START INTL CO.,LTD.	
Title	XDP/USB Power Dischage	
Size	Document Number: IH110M	Rev: 1.0
Date: Tuesday, July 07, 2015	Sheet 26 of 43	

+1V0_PCH



Vo =1V
Vin =19V
FS = 300khz
OCP 150%~200%
Iout =9.24A
Vin_Irms =2.2A
MLCC ripple current = 4.65A
LIR =28%
Cin_CAP =5.1uF
Cout_CAP =611uF
Cout_CAP_ESR =8mohm

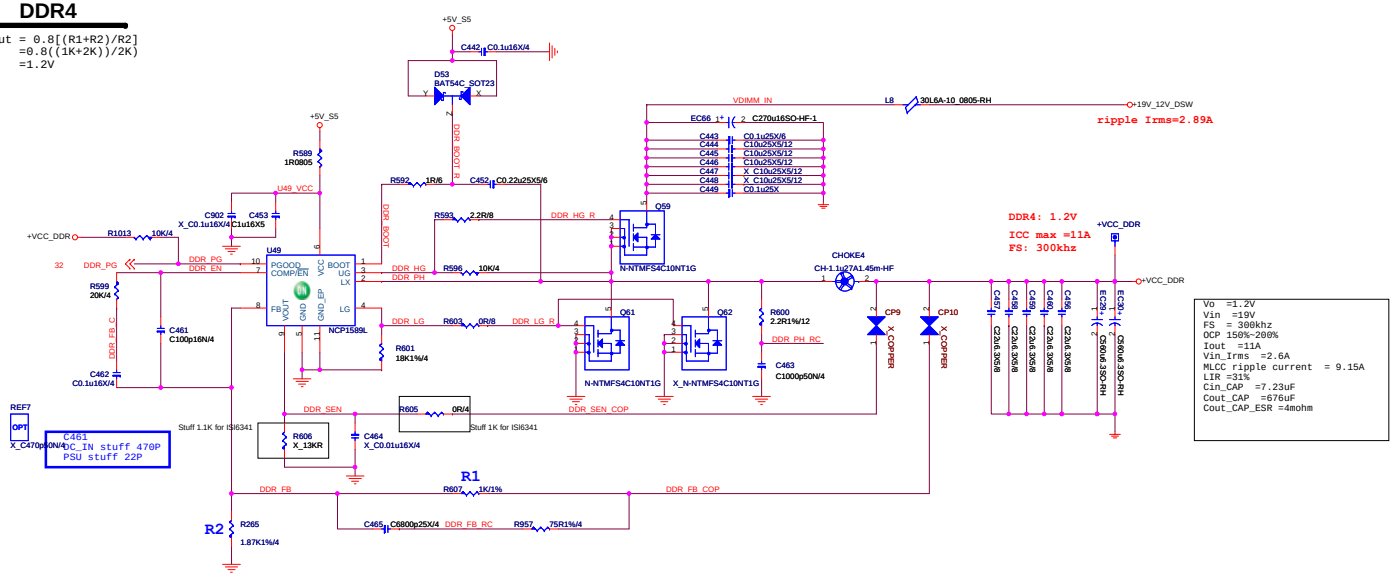
ICC max = MAX 9.24A
OCP 13.9A

MICRO-START INT'L CO.,LTD.

Title: PCH Core Power		
Size	Document Number: IH110M	Rev: 1.0
Date: Thursday, July 09, 2015	Sheet 27 of 43	

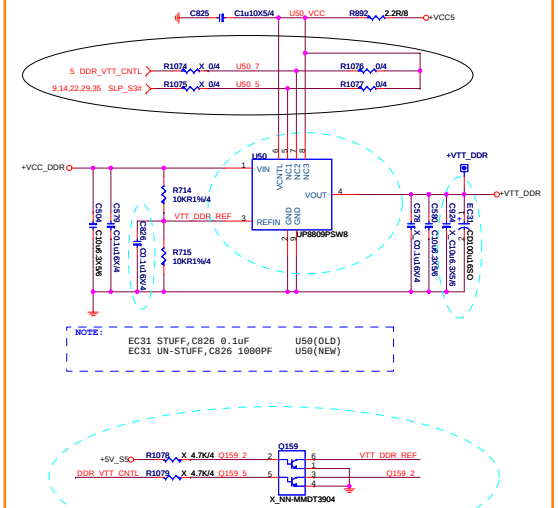
DDR4

Vout = 0.8[(R1+R2)/R2]
=0.8((1K+2K))/2K)
=1.2V



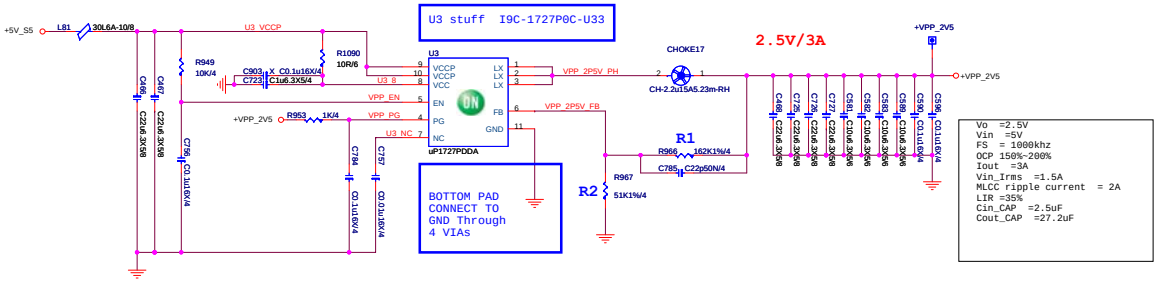
DDR4 Termination Power

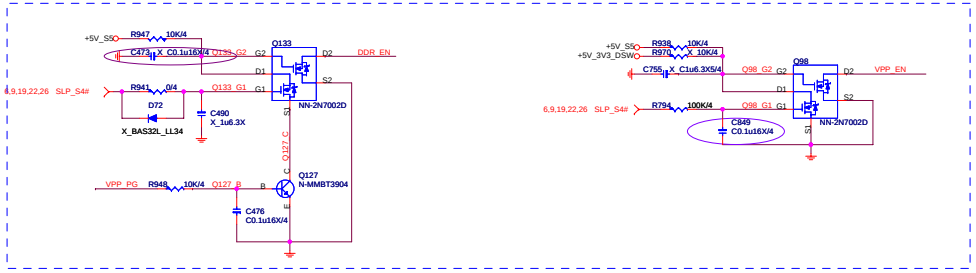
0.6V - 1.1A - 0.825W



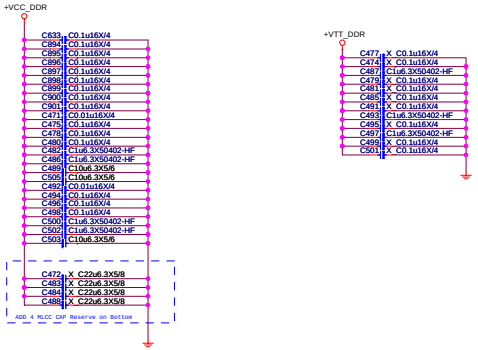
VPP_2.5V

Vout = 0.6[(R1+R2)/R2]
=0.6((10K+3.16K))/3.16K)
=2.5V





DDRIII I/O power decoulping caps.



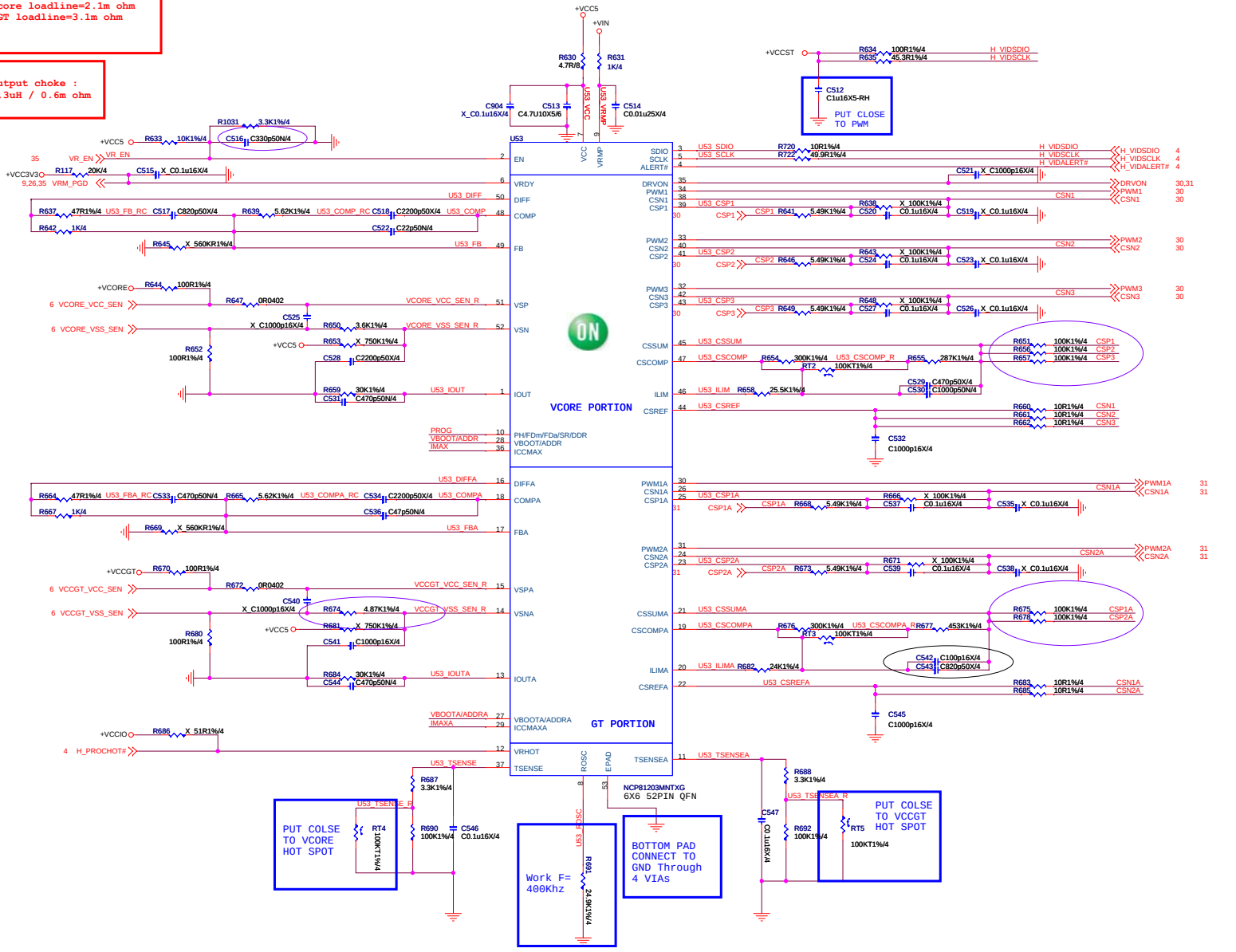
MSI MICRO-START INT'L CO.,LTD.

Title	DDR4 Power	
Size	Document Number	Rev
	IH110M	1.0
Date: Sunday, July 12, 2015	Sheet 28 of 44	

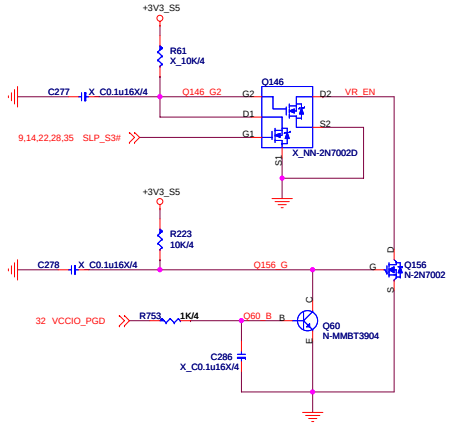
Intel SKYLAKE IMVP8 POWER CKT - 3+2 PHASE

S-line 42 95W
Vcore loadline=2.1m ohm
VGT loadline=3.1m ohm

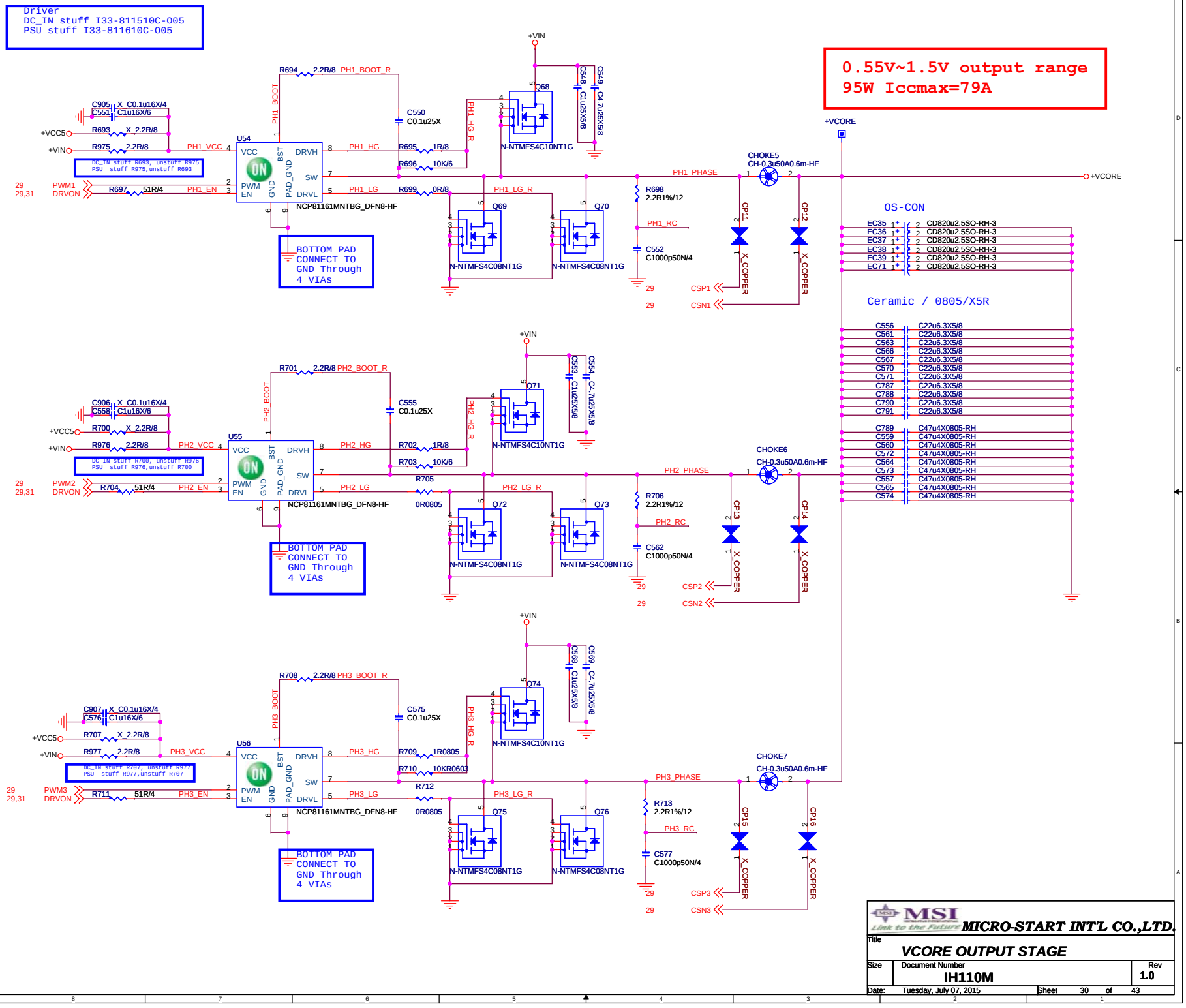
output choke :
0.3uH / 0.6m ohm



Power Sequence



MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	IMVP8-NCP81203 5 Phase		
Size	Document Number IH110M		Rev 1.0
Date: Tuesday, July 07, 2015	Sheet 29 of 43		


Driver
DC_IN stuff I33-811510C-O05
PSU stuff I33-811610C-O05
0.55V~1.5V output range
95W Iccmax=79A
+VIN
+VCORE
+VCC5
U54
U55
U56
NCP81161MNTBG_DFN8-HF
N-NTMFS4C10NT1G
N-NTMFS4C08NT1G
CHOKE5
CHOKE6
CHOKE7
CH-0.3u50A0.6m-HF
OS-CON
Ceramic / 0805/X5R
BOTTOM PAD CONNECT TO GND Through 4 VIAs
PH1_PHASE
PH2_PHASE
PH3_PHASE
CSP1
CSN1
CSP2
CSN2
CSP3
CSN3
MICRO-START INT'L CO.,LTD.
VCORE OUTPUT STAGE
IH110M
1.0
Tuesday, July 07, 2015
Sheet 30 of 43

Driver
DC_IN stuff I33-811510C-005
PSU stuff I33-811610C-005

0.55V~1.5V output range
95W Iccmax=51A

+VIN
+VCC5
PWM1A
DRVON
PWM2A
PH1A_BOOT_R
PH1A_HG
PH1A_LG
PH1A_PHASE
PH1A_VCC
PH1A_EN
PH1A_HG_R
PH1A_LG_R
PH1A_RC
PH2A_BOOT_R
PH2A_HG
PH2A_LG
PH2A_PHASE
PH2A_VCC
PH2A_EN
PH2A_HG_R
PH2A_LG_R
PH2A_RC
U63
NCP81161MNTBG_DFN8-HF
U64
NCP81161MNTBG_DFN8-HF
BOTTOM PAD CONNECT TO GND Through 4 VIAs
N-NTMFS4C10NT1G
N-NTMFS4C08NT1G
CHOKE18
CH-0.3u50A0.6m-HF
CHOKE19
CH-0.3u50A0.6m-HF
+VCCGT
OSCON
EC42 CD820u2.5SO-RH-3
EC43 CD820u2.5SO-RH-3
EC44 CD820u2.5SO-RH-3
EC41 CD820u2.5SO-RH-3
EC40 CD820u2.5SO-RH-3
Ceramic / 0805/X5R
C584 C47u4X0805-RH
C585 C47u4X0805-RH
C591 C47u4X0805-RH
C592 C47u4X0805-RH
C812 C47u4X0805-RH
C593 C47u4X0805-RH
C586 C47u4X0805-RH
C594 C22u6.3X5/8
C587 C22u6.3X5/8
C811 C10u16X50805-HF
C792 C10u16X50805-HF
CSP1A
CSN1A
CSP2A
CSN2A
X_COPPER
DC-IN stuff
L48 X_30L6A-10_0805-RH
L49 X_30L6A-10_0805-RH
+19V_12V_DSW
PSU stuff
Q142
P-PZ0703EV_SOP8-HF
CHOKE10
CH-1.1u27A1.45m-HF
OS-CON
+12V_B_DSW
ATX_12V
PWRCONN4P_NATURAL
C270u16SO-HF-1
C1u25X-HF
C189 X_C0.1u16X
R151 100K/4
D8 S-RB751V-40_SOD323-RH
12V_PS_ON# 34

MSI MICRO-START INTL CO.,LTD.
Link to the Future
Title: VCCGT OUTPUT STAGE
Size: Document Number: IH110M
Rev: 1.0
Date: Tuesday, July 07, 2015
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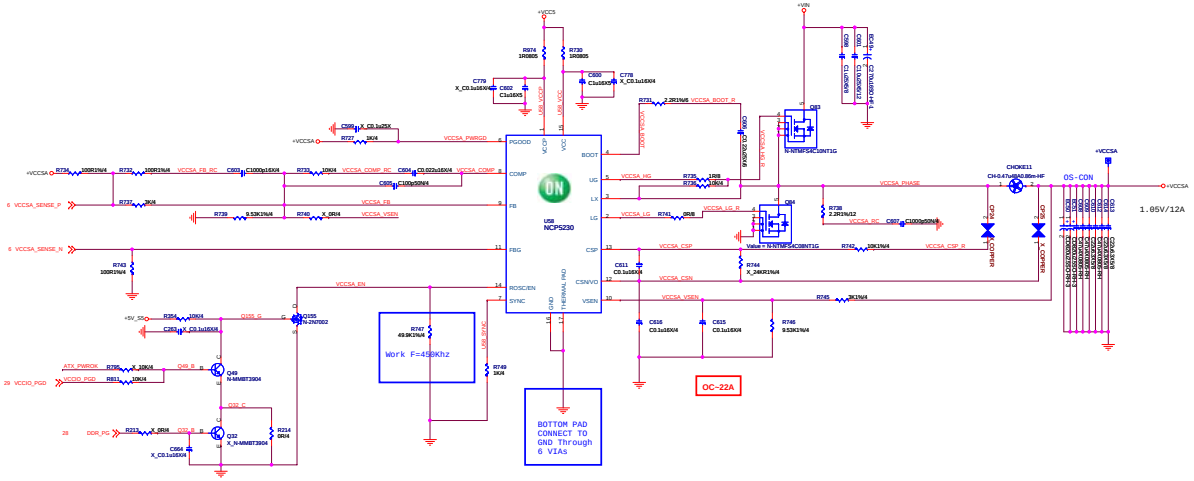
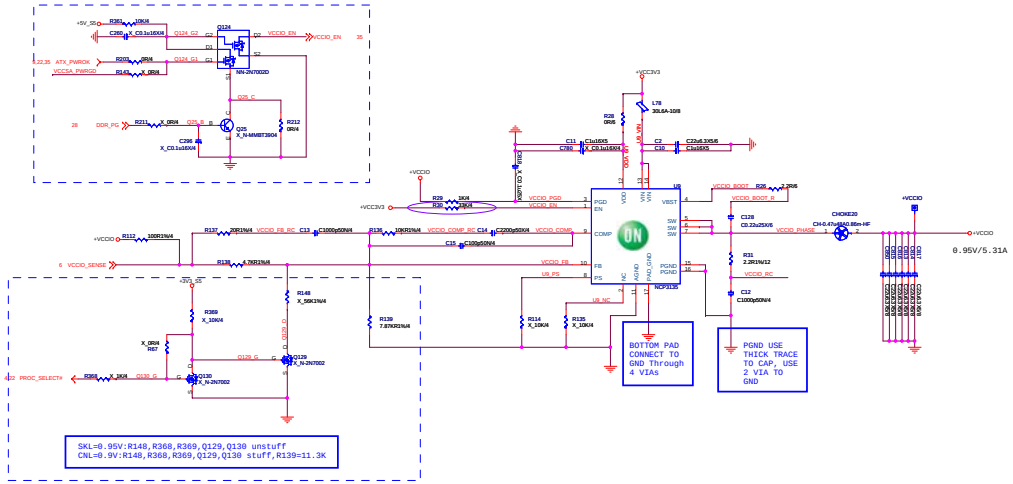
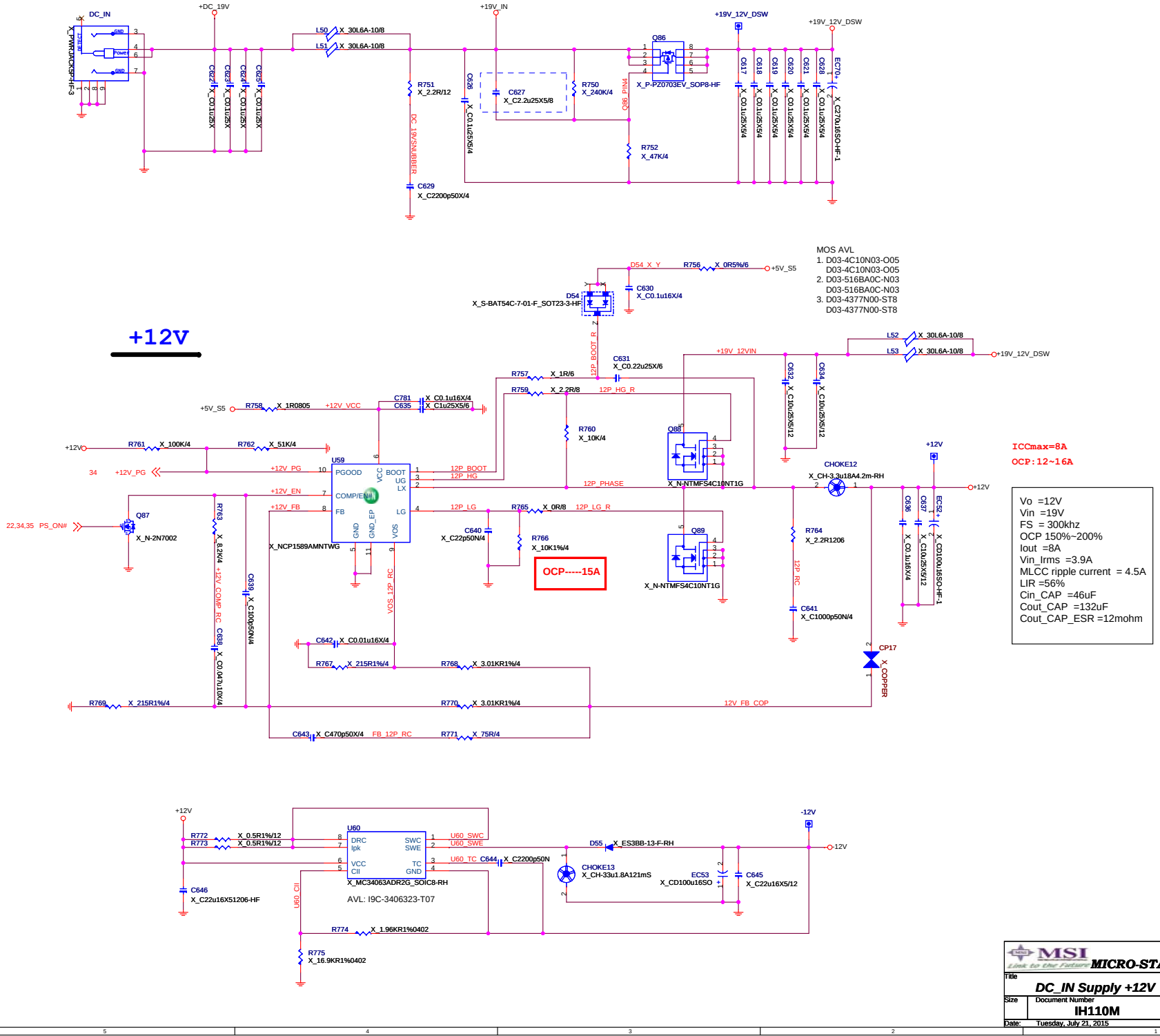
VCCSA



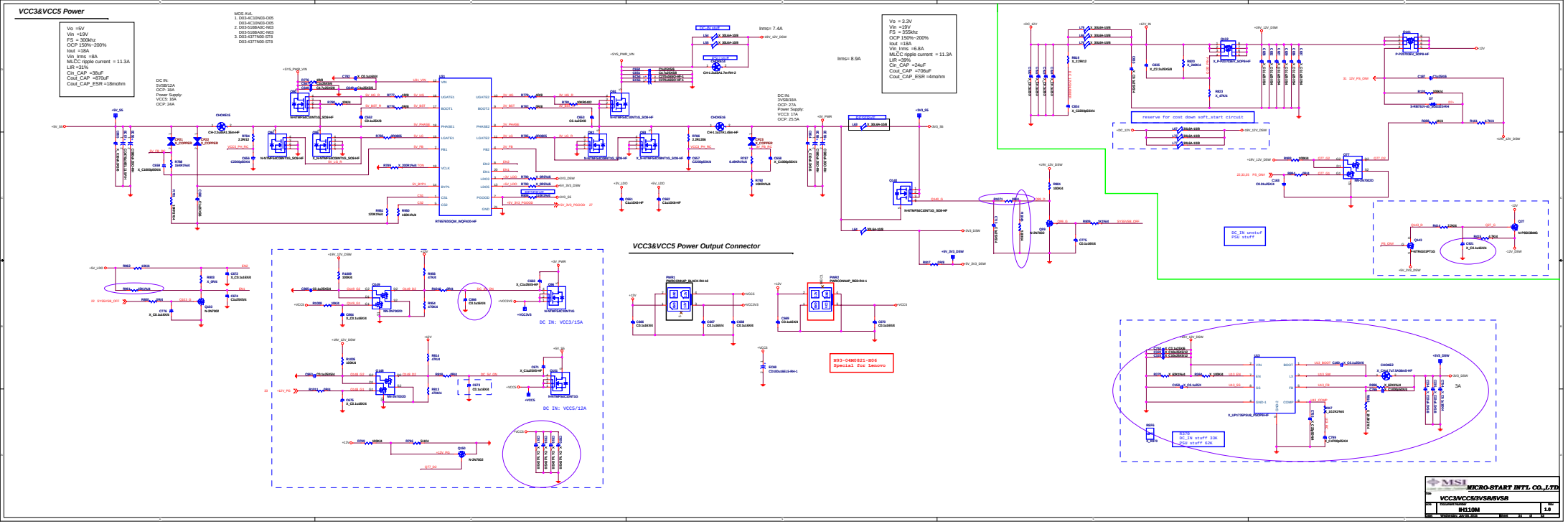
VCCIO



MSI	MICRO-START INT'L CO.,LTD.	
Title	VccSA/VccIO	
Size	Document Number: IH110M	Rev: 1.0
Date: Tuesday, July 07, 2009	Sheet 32 of 43	



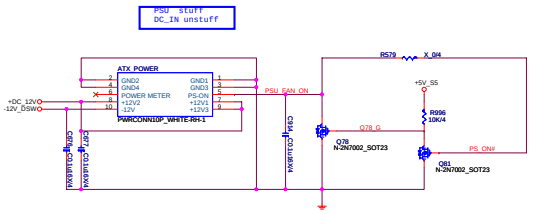
MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	DC_IN Supply +12V		
Size	Document Number IH110M		Rev 1.0
Date: Tuesday, July 21, 2015	Sheet 33 of 43		


VCC3&VCC5 Power
Vo =5V
Vin =19V
FS = 300khz
OCP 150%~200%
Iout =18A
Vin_Irms =8A
MLCC ripple current = 11.3A
LIR =31%
Cin_CAP =38uF
Cout_CAP =870uF
Cout_CAP_ESR =18mohm
MOS AVL
1. DI03-4C10ND3-O05
DI03-4C10ND3-O05
2. DI03-S18BA0C-N03
DI03-S18BA0C-N03
3. DI03-4377N00-ST8
DI03-4377N00-ST8
DC IN:
5VSB/12A
OCP: 18A
Power Supply:
VCC5: 16A
OCP: 24A
Irms= 7.4A
Irms= 8.9A
Vo = 3.3V
Vin =19V
FS = 355khz
OCP 150%~200%
Iout =18A
Vin_Irms =6.8A
MLCC ripple current = 11.3A
LIR =39%
Cin_CAP =24uF
Cout_CAP =706uF
Cout_CAP_ESR =4mohm
DC IN:
3VSB/18A
OCP: 27A
Power Supply:
VCC3: 17A
OCP: 25.5A
reserve for cost down soft_start circuit
DC_IN unstuf
PSU stuff
DC IN: VCC3/15A
DC IN: VCC5/12A
VCC3&VCC5 Power Output Connector
N93-04N0821-B04
Special for Lenovo
MICRO-START INTL CO.,LTD
VCC3/VCC5/3VSB/5VSB
IH110M
1.0

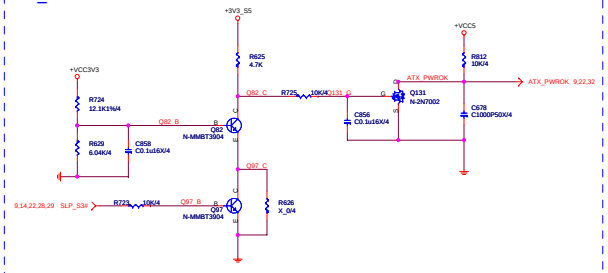
ATX Power Connector / Front Panel / LED/DSW

8 Pin ATX Power Connector

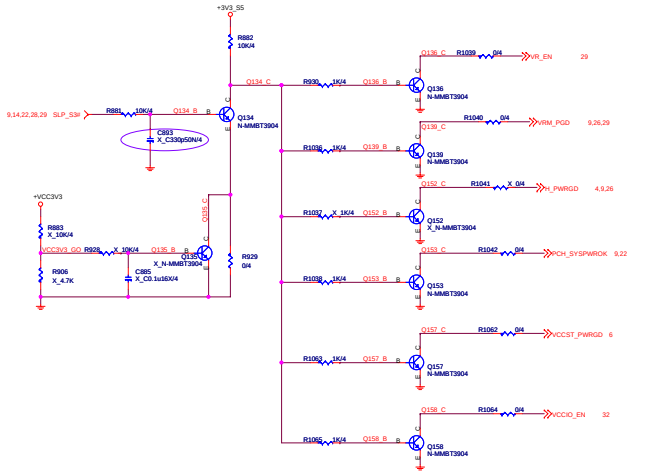
Power Supply in mounted



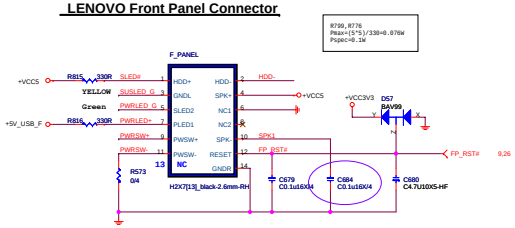
ATX_PWRGD



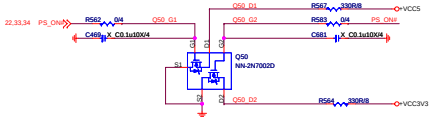
Power on/down sequencing circuit



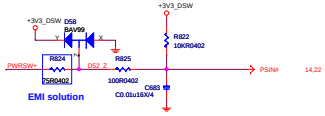
LENOVO Front Panel Connector



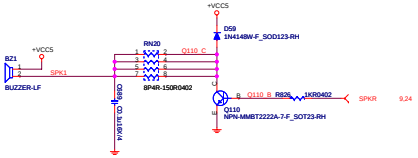
VCC3/VCC5 Discharge



Power Button

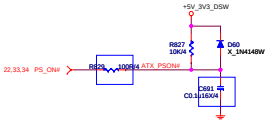


Buzzer Circuit

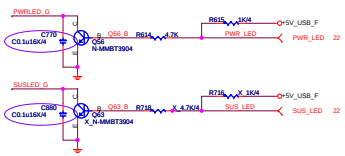


HDD LED

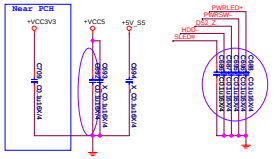
ATX Power On



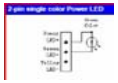
Power LED



Cap For EMI



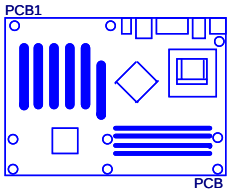
Lenovo EMC suggestion for 144MHz harmonic wave



Tile	MICRO-START INTL CO.,LTD.
	ATX/F_Panel/EMI/LED
Size	Document Number: IH110M — Rev: 1.0
Date: Tuesday, July 07, 2015	Sheet 35 of 43

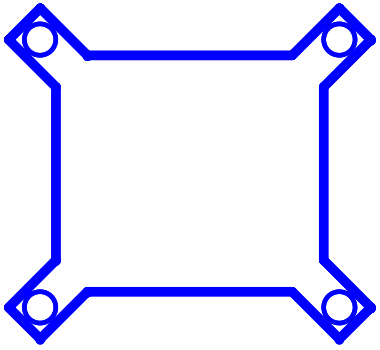
Manual Parts

PCB1



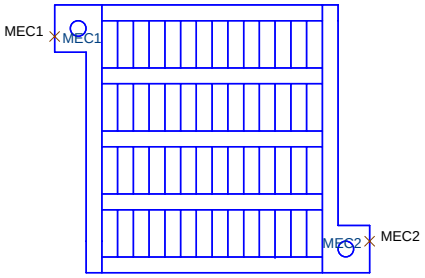
PCB

XU1_X2



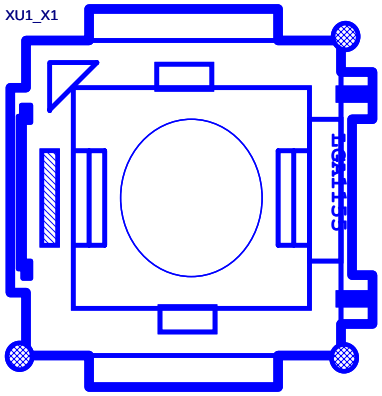
X_CPU Backplate

U2_X1



PCH Heatsink

XU1_X1



CPU SOCKET

U2_X1_1

U2_X1_2

Simulation

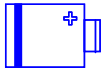
SIP1

X_PIN1*2

SIP2

X_PIN1*2

VBAT-S1



BAT-BCR2032P-RH

GASKET1 OPT

WIN8KEY1 OPT

WIN8KEY2 OPT

AMI_KEY1 OPT

HDMI_LABEL OPT

For EMI **For Moat CAP**

+VCC5

C697
C0.1u16X/4

+VCC3V3

C698
X_C0.1u16X/4

+1V0_PCH

+VCC3V3

C699
X_C0.1u16X/4

+1V0_PCH

+5V_S5

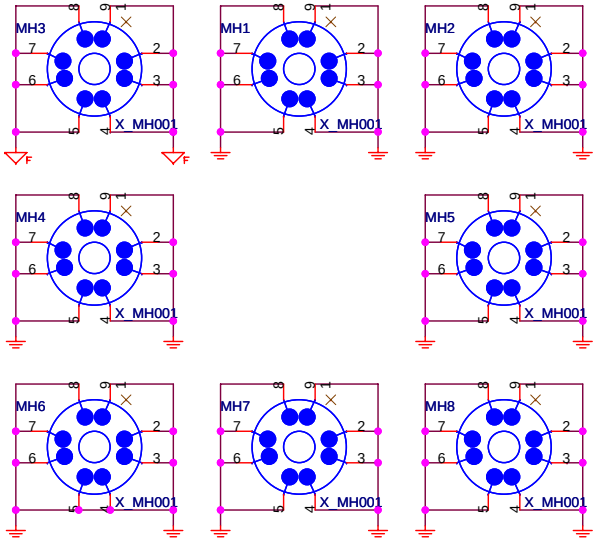
C700
X_C0.1u16X/4

EMI Suggestion
VRM part has high frequence noise

+12V

C701
X_C0.1u16X/4

Mounting Holes



Optics Orientation Holes

Optical Fiducial Marks-120

FM1 FM2 FM3 FM4 FM5 FM6 FM7 FM8

X_FM

BIOS_ROM1 OPT

AUDIO OPT

USB_LAN OPT

VGA_COM1 OPT

REF1	REF2	REF4	REF3	REF5	REF8	REF9
OPT	OPT	OPT	OPT	OPT	OPT	OPT
X_TPM	X_USB_LAN	X_USB_LAN	X_CLK_BUFFER	X_PWM_Driver	X_VGA	X_EC

MSI MICRO-START INT'L CO.,LTD.
Link to the Future

Title: Manual & Option Parts

Size | Document Number: IH110M | Rev: 1.0

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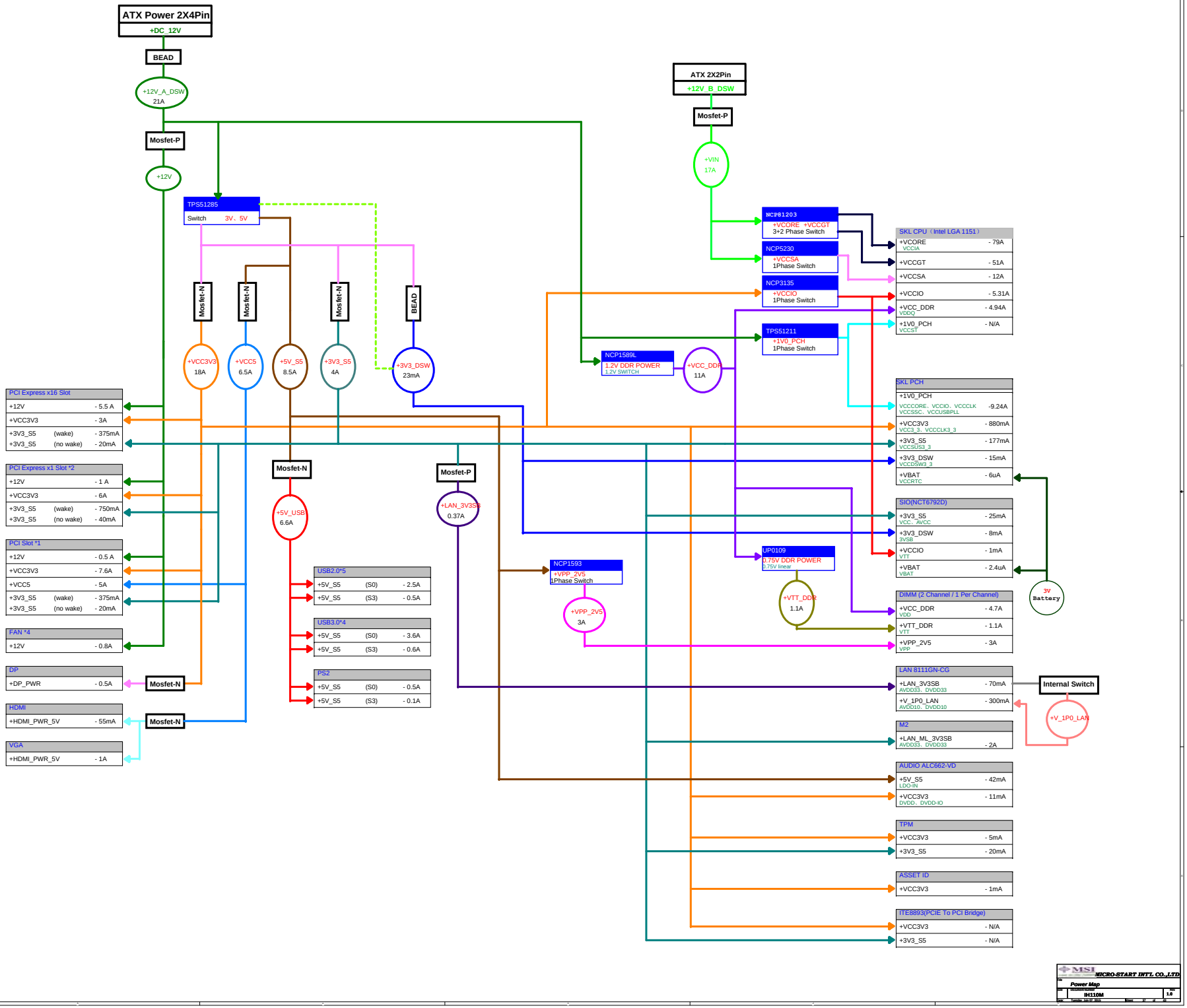
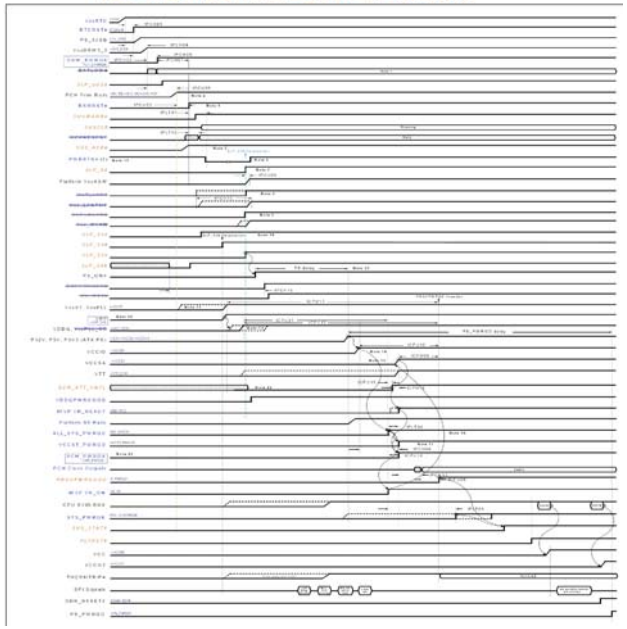
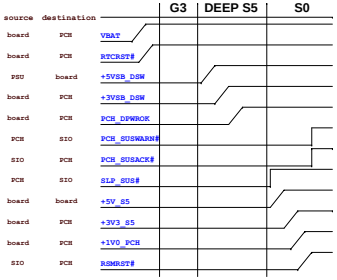

ATX Power 2X4Pin
+DC_12V
BEAD
+12V_A_DSW
21A
Mosfet-P
+12V
TPS51285
Switch 3V、5V
Mosfet-N
Mosfet-N
Mosfet-N
BEAD
+VCC3V3
18A
+VCC5
6.5A
+5V_S5
8.5A
+3V3_S5
4A
+3V3_DSW
23mA
PCI Express x16 Slot
+12V - 5.5 A
+VCC3V3 - 3A
+3V3_S5 (wake) - 375mA
+3V3_S5 (no wake) - 20mA
PCI Express x1 Slot *2
+12V - 1 A
+VCC3V3 - 6A
+3V3_S5 (wake) - 750mA
+3V3_S5 (no wake) - 40mA
PCI Slot *1
+12V - 0.5 A
+VCC3V3 - 7.6A
+VCC5 - 5A
+3V3_S5 (wake) - 375mA
+3V3_S5 (no wake) - 20mA
FAN *4
+12V - 0.8A
DP
+DP_PWR - 0.5A
Mosfet-N
HDMI
+HDMI_PWR_5V - 55mA
Mosfet-N
VGA
+HDMI_PWR_5V - 1A
Mosfet-N
+5V_USB
6.6A
USB2.0*5
+5V_S5 (S0) - 2.5A
+5V_S5 (S3) - 0.5A
USB3.0*4
+5V_S5 (S0) - 3.6A
+5V_S5 (S3) - 0.6A
PS2
+5V_S5 (S0) - 0.5A
+5V_S5 (S3) - 0.1A
Mosfet-P
+LAN_3V3SB
0.37A
NCP1589L
1.2V DDR POWER
1.2V SWITCH
+VCC_DDR
11A
NCP1593
+VPP_2V5
1Phase Switch
+VPP_2V5
3A
ATX 2X2Pin
+12V_B_DSW
Mosfet-P
+VIN
17A
NCP81203
+VCORE +VCCGT
3+2 Phase Switch
NCP5230
+VCCSA
1Phase Switch
NCP3135
+VCCIO
1Phase Switch
TPS51211
+1V0_PCH
1Phase Switch
UP0109
0.75V DDR POWER
0.75V linear
+VTT_DDR
1.1A
SKL CPU（Intel LGA 1151）
+VCORE VCCIA - 79A
+VCCGT - 51A
+VCCSA - 12A
+VCCIO - 5.31A
+VCC_DDR VDDQ - 4.94A
+1V0_PCH VCCST - N/A
SKL PCH
+1V0_PCH VCCCORE、VCCIO、VCCCLK VCCSSC、VCCUSBPLL -9.24A
+VCC3V3 VCC3_3、VCCCLK3_3 - 880mA
+3V3_S5 VCCSUS3_3 - 177mA
+3V3_DSW VCCDSW3_3 - 15mA
+VBAT VCCRTC - 6uA
SIO(NCT6792D)
+3V3_S5 VCC、AVCC - 25mA
+3V3_DSW 3VSB - 8mA
+VCCIO VTT - 1mA
+VBAT VBAT - 2.4uA
3V Battery
DIMM (2 Channel / 1 Per Channel)
+VCC_DDR VDD - 4.7A
+VTT_DDR VTT - 1.1A
+VPP_2V5 VPP - 3A
LAN 8111GN-CG
+LAN_3V3SB AVDD33、DVDD33 - 70mA
+V_1P0_LAN AVDD10、DVDD10 - 300mA
Internal Switch
+V_1P0_LAN
M2
+LAN_ML_3V3SB AVDD33、DVDD33 - 2A
AUDIO ALC662-VD
+5V_S5 LDO-IN - 42mA
+VCC3V3 DVDD、DVDD-IO - 11mA
TPM
+VCC3V3 - 5mA
+3V3_S5 - 20mA
ASSET ID
+VCC3V3 - 1mA
ITE8893(PCIE To PCI Bridge)
+VCC3V3 - N/A
+3V3_S5 - N/A
MICRO-START INTL CO.,LTD
Power Map
IH110M
1.0

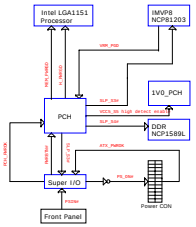
SKL-S Timing Diagram for G3 to S0 [Deep Sx Platform]



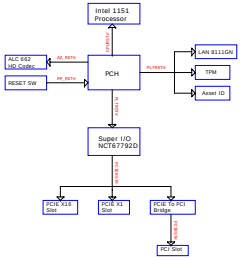
with Deep Sx support

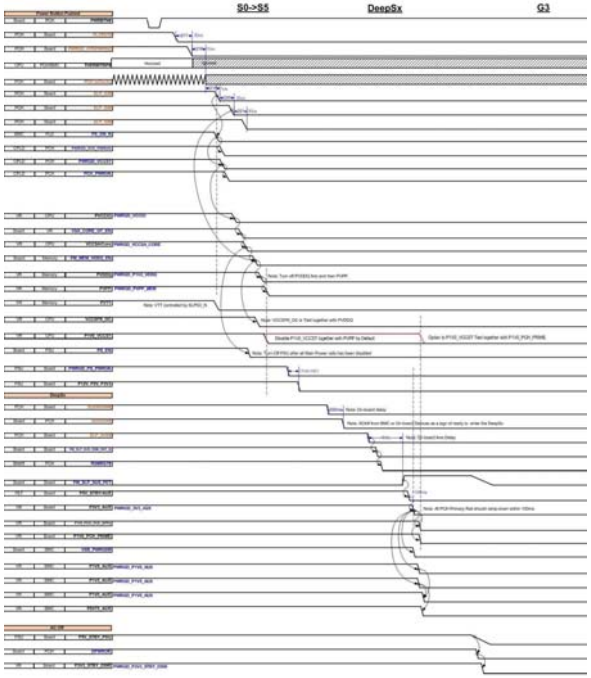


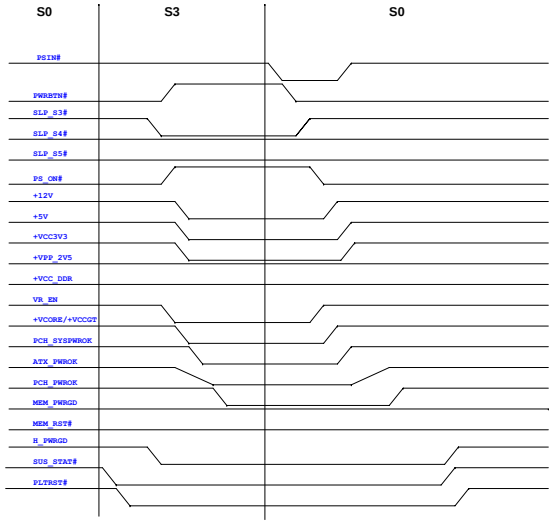
PWROK MAP



RESET MAP







MICRO-START INT'L CO.,LTD.

Power Sequence

DIS1SM

PCH_GPIO

PCH

GPIO	I/O/NC	Power	Tol	Default	Usage	Input/Output
GPP_A0	I/O	Standby	3.3V	Native	KBRST#	Native
GPP_A1	I/O	Standby	3.3V	Native	LPC_AD0	Native
GPP_A2	I/O	Standby	3.3V	Native	LPC_AD1	Native
GPP_A3	I/O	Standby	3.3V	Native	LPC_AD2	Native
GPP_A4	I/O	Standby	3.3V	Native	LPC_AD3	Native
GPP_A5	I/O	Standby	3.3V	Native	LPC_FRAME#	Native
GPP_A6	I/O	Standby	3.3V	Native	LPC_SERIRQ	Native
GPP_A7	I/O	Standby	3.3V	Native	LPC_DRQ#0	Native
GPP_A8	I/O	Standby	3.3V	Native	CLKRUN#	Native
GPP_A9	I/O	Standby	3.3V	Native	LPC_CLK_24M	Native
GPP_A10	I/O	Standby	3.3V	Native	PCI_CLK_24M	Native
GPP_A11	I/O	Standby	3.3V	Native	SIO_PME#	Native
GPP_A12	I/O	Standby	3.3V	GPI	BMBUSY#	Input
GPP_A13	I/O	Standby	3.3V	Native	PCH_SUSWARN#	Native
GPP_A14	I/O	Standby	3.3V	Native	SUS_STAT#	Native
GPP_A15	I/O	Standby	3.3V	Native	PCH_SUSACK#	Native
GPP_A16	I/O	Standby	3.3V	GPI	N/A	Input
GPP_A17	I/O	Standby	3.3V	GPI	N/A	Input
GPP_A18	I/O	Standby	3.3V	GPI	N/A	Input
GPP_A19	I/O	Standby	3.3V	GPI	N/A	Input
GPP_A20	I/O	Standby	3.3V	GPI	PCH_GPIO20	Input
GPP_A21	I/O	Standby	3.3V	GPI	PCH_GPIO21	Input
GPP_A22	I/O	Standby	3.3V	GPI	PCH_GPIO22	Input
GPP_A23	I/O	Standby	3.3V	GPI	PCH_GPIO23	Input

GPIO	I/O/NC	Power	Tol	Default	Usage	Input/Output
GPP_B0	I/O	Standby	3.3V	GPO	FUSB_G1	Input
GPP_B1	I/O	Standby	3.3V	GPO	FUSB_G2	Input
GPP_B2	I/O	Standby	3.3V	GPI	PCH_VRALERT#	Input
GPP_B3	I/O	Standby	3.3V	GPI	FUSB_G3	Input
GPP_B4	I/O	Standby	3.3V	GPI	LPT_DET#	Input
GPP_B5	I/O	Standby	3.3V	GPI	COM_GPIO1	Input
GPP_B6	I/O	Standby	3.3V	GPI	PCIECLKREQ1#	Input
GPP_B7	I/O	Standby	3.3V	GPI	N/A	Input
GPP_B8	I/O	Standby	3.3V	GPI	N/A	Input
GPP_B9	I/O	Standby	3.3V	GPI	N/A	Input
GPP_B10	I/O	Standby	3.3V	GPI	PCIECLKREQ5#	Input
GPP_B11	I/O	Standby	3.3V	GPO	N/A	Output
GPP_B12	I/O	Standby	3.3V	Native	N/A	Native
GPP_B13	I/O	Standby	3.3V	Native	PLTRST#	Native
GPP_B14	I/O	Standby	3.3V	GPO	SPKR	Input
GPP_B15	I/O	Standby	3.3V	GPI	N/A	Input
GPP_B16	I/O	Standby	3.3V	GPI	N/A	Input
GPP_B17	I/O	Standby	3.3V	GPI	N/A	Input
GPP_B18	I/O	Standby	3.3V	GPO	REBOOT_STRAP	Input
GPP_B19	I/O	Standby	3.3V	GPI	N/A	Input
GPP_B20	I/O	Standby	3.3V	GPI	SMI#	Input
GPP_B21	I/O	Standby	3.3V	GPI	OE#_R	Input
GPP_B22	I/O	Standby	3.3V	GPO	BBS_STRAP	Input
GPP_B23	I/O	Standby	3.3V	GPO	THERMTRIP_STRAP	Input

GPIO	I/O/NC	Power	Tol	Default	Usage	Input/Output
GPP_C0	I/O	Standby	3.3V	Native	SMBCLK	Native
GPP_C1	I/O	Standby	3.3V	Native	SMBDATA	Native
GPP_C2	I/O	Standby	3.3V	GPO	TLS_STRAP	Input
GPP_C3	I/O	Standby	3.3V	Native	SML0_CLK	Native
GPP_C4	I/O	Standby	3.3V	Native	SML0_DATA	Native
GPP_C5	I/O	Standby	3.3V	GPO	ESPI_STRAP	Input
GPP_C6	I/O	Standby	3.3V	GPI	SML1_CLK	Native
GPP_C7	I/O	Standby	3.3V	GPI	SML1_DATA	Native
GPP_C8	I/O	Standby	3.3V	GPI	N/A	Input
GPP_C9	I/O	Standby	3.3V	GPI	N/A	Input
GPP_C10	I/O	Standby	3.3V	GPI	N/A	Input
GPP_C11	I/O	Standby	3.3V	GPI	PU_PCH_GPP_C_11	Input
GPP_C12	I/O	Standby	3.3V	GPI	N/A	Input
GPP_C13	I/O	Standby	3.3V	GPI	N/A	Input
GPP_C14	I/O	Standby	3.3V	GPI	N/A	Input
GPP_C15	I/O	Standby	3.3V	GPI	N/A	Input
GPP_C16	I/O	Standby	3.3V	GPI	USB_CHARGE_OC_SET	Output
GPP_C17	I/O	Standby	3.3V	GPI	N/A	Input
GPP_C18	I/O	Standby	3.3V	GPI	N/A	Input
GPP_C19	I/O	Standby	3.3V	GPI	N/A	Input
GPP_C20	I/O	Standby	3.3V	GPI	N/A	Input
GPP_C21	I/O	Standby	3.3V	GPI	N/A	Input
GPP_C22	I/O	Standby	3.3V	GPI	N/A	Input
GPP_C23	I/O	Standby	3.3V	GPI	N/A	Input

GPIO	I/O/NC	Power	Tol	Default	Usage	Input/Output
GPP_D0	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D1	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D2	I/O	Standby	3.3V	GPI	PD_PCH_GPP_D_2	Input
GPP_D3	I/O	Standby	3.3V	GPI	PD_PCH_GPP_D_3	Input
GPP_D4	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D5	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D6	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D7	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D8	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D9	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D10	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D11	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D12	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D13	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D14	I/O	Standby	3.3V	GPI	PU_FM_LA_TRIGGER#	Input
GPP_D15	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D16	I/O	Standby	3.3V	GPI	PCH_GPIO_D16	Output
GPP_D17	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D18	I/O	Standby	3.3V	GPI	PCH_GPIO_D18	Output
GPP_D19	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D20	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D21	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D22	I/O	Standby	3.3V	GPI	N/A	Input
GPP_D23	I/O	Standby	3.3V	GPI	N/A	Input

GPIO	I/O/NC	Power	Tol	Default	Usage	Input/Output
GPP_E0	I/O	DSW	3.3V	Native	N/A	Native
GPP_E1	I/O	DSW	3.3V	Native	N/A	Native
GPP_E2	I/O	DSW	3.3V	Native	N/A	Native
GPP_E3	I/O	DSW	3.3V	GPI	PCH_CPU_GP0	Input
GPP_E4	I/O	DSW	3.3V	GPI	N/A	Input
GPP_E5	I/O	DSW	3.3V	GPI	N/A	Input
GPP_E6	I/O	DSW	3.3V	GPI	N/A	Input
GPP_E7	I/O	DSW	3.3V	GPI	N/A	Input
GPP_E8	I/O	DSW	3.3V	GPI	SATA_LED#	Output
GPP_E9	I/O	DSW	3.3V	GPI	USB_OCP#0	Input
GPP_E10	I/O	DSW	3.3V	GPI	USB_OCP#1	Input
GPP_E11	I/O	DSW	3.3V	GPI	USB_OCP#2	Input
GPP_E12	I/O	DSW	3.3V	GPI	USB_OCP#3	Input

GPIO	I/O/NC	Power	Tol	Default	Usage	Input/Output
GPP_F0	I/O	Standby	3.3V	Native	N/A	Native
GPP_F1	I/O	Standby	3.3V	Native	N/A	Native
GPP_F2	I/O	Standby	3.3V	Native	N/A	Native
GPP_F3	I/O	Standby	3.3V	Native	N/A	Native
GPP_F4	I/O	Standby	3.3V	Native	N/A	Native
GPP_F5	I/O	Standby	3.3V	GPI	SPI_SIRQ#	Input
GPP_F6	I/O	Standby	3.3V	GPI	N/A	Input
GPP_F7	I/O	Standby	3.3V	GPI	N/A	Input
GPP_F8	I/O	Standby	3.3V	GPI	N/A	Input
GPP_F9	I/O	Standby	3.3V	GPI	N/A	Input
GPP_F10	I/O	Standby	3.3V	GPI	N/A	Input
GPP_F11	I/O	Standby	3.3V	GPI	N/A	Input
GPP_F12	I/O	Standby	3.3V	GPI	N/A	Input
GPP_F13	I/O	Standby	3.3V	GPI	N/A	Input
GPP_F14	I/O	Standby	3.3V	GPI	SKTOCC#_C	Input
GPP_F15	I/O	Standby	3.3V	GPI	USB_OCP#4	Input
GPP_F16	I/O	Standby	3.3V	GPI	USB_OCP#5	Input
GPP_F17	I/O	Standby	3.3V	GPI	USB_OCP#6	Input
GPP_F18	I/O	Standby	3.3V	GPI	USB_OCP#7	Input
GPP_F19	I/O	Standby	3.3V	GPI	N/A	Input
GPP_F20	I/O	Standby	3.3V	GPI	N/A	Input
GPP_F21	I/O	Standby	3.3V	GPI	N/A	Input
GPP_F22	I/O	Standby	3.3V	GPI	N/A	Input
GPP_F23	I/O	Standby	3.3V	GPI	N/A	Input

GPIO	I/O/NC	Power	Tol	Default	Usage	Input/Output
GPP_G0	I/O	Standby	3.3V	GPI	GPP_G0	Input
GPP_G1	I/O	Standby	3.3V	GPI	GPP_G1	Input
GPP_G2	I/O	Standby	3.3V	GPI	GPP_G2	Input
GPP_G3	I/O	Standby	3.3V	GPI	GPP_G3	Input
GPP_G4	I/O	Standby	3.3V	GPI	GPP_G4	Input
GPP_G5	I/O	Standby	3.3V	GPI	GPP_G5	Input
GPP_G6	I/O	Standby	3.3V	GPI	N/A	Input
GPP_G7	I/O	Standby	3.3V	GPI	N/A	Input
GPP_G8	I/O	Standby	3.3V	Native	N/A	Native
GPP_G9	I/O	Standby	3.3V	Native	N/A	Native
GPP_G10	I/O	Standby	3.3V	Native	N/A	Native
GPP_G11	I/O	Standby	3.3V	Native	N/A	Native
GPP_G12	I/O	Standby	3.3V	GPI	N/A	Input
GPP_G13	I/O	Standby	3.3V	GPI	N/A	Input
GPP_G14	I/O	Standby	3.3V	GPI	N/A	Input
GPP_G15	I/O	Standby	3.3V	GPI	N/A	Input
GPP_G16	I/O	Standby	3.3V	GPI	N/A	Input
GPP_G17	I/O	Standby	3.3V	GPI	N/A	Input
GPP_G18	I/O	Standby	3.3V	GPI	N/A	Input
GPP_G19	I/O	Standby	3.3V	GPI	N/A	Input
GPP_G20	I/O	Standby	3.3V	GPI	N/A	Input
GPP_G21	I/O	Standby	3.3V	GPI	N/A	Input
GPP_G22	I/O	Standby	3.3V	GPI	FM_BIOS_IMAGE_SWAP#	Input
GPP_G23	I/O	Standby	3.3V	GPI	N/A	Input

GPIO	I/O/NC	Power	Tol	Default	Usage	Input/Output
GPP_H0	I/O	Standby	3.3V	GPI	ILIM_SEL	Output
GPP_H1	I/O	Standby	3.3V	GPI	CTL1	Output
GPP_H2	I/O	Standby	3.3V	GPI	CTL2	Output
GPP_H3	I/O	Standby	3.3V	GPI	CTL3	Output
GPP_H4	I/O	Standby	3.3V	GPI	CHARGE_EN	Output
GPP_H5	I/O	Standby	3.3V	GPI	N/A	Input
GPP_H6	I/O	Standby	3.3V	GPI	N/A	Input
GPP_H7	I/O	Standby	3.3V	GPI	N/A	Input
GPP_H8	I/O	Standby	3.3V	GPI	N/A	Input
GPP_H9	I/O	Standby	3.3V	GPI	N/A	Input
GPP_H10	I/O	Standby	3.3V	GPI	WIRELESS_EN2	Output
GPP_H11	I/O	Standby	3.3V	GPI	WIRELESS_EN1	Output
GPP_H12	I/O	Standby	3.3V	GPO	FM_ESPI_FLASH_MODE	Input
GPP_H13	I/O	Standby	3.3V	GPI	SEL#_R	Input
GPP_H14	I/O	Standby	3.3V	GPI	N/A	Input
GPP_H15	I/O	Standby	3.3V	GPI	PCH_GPP_H15	Input
GPP_H16	I/O	Standby	3.3V	GPI	N/A	Input
GPP_H17	I/O	Standby	3.3V	GPI	N/A	Input
GPP_H18	I/O	Standby	3.3V	GPI	PCH_GPP_H18	Input
GPP_H19	I/O	Standby	3.3V	GPI	N/A	Input
GPP_H20	I/O	Standby	3.3V	GPI	CHASSIS_ID1	Input
GPP_H21	I/O	Standby	3.3V	GPI	CHASSIS_ID2	Input
GPP_H22	I/O	Standby	3.3V	GPI	ME_DIS	Input
GPP_H23	I/O	Standby	3.3V	GPI	CLR_CMOS	Input

GPIO	I/O/NC	Power	Tol	Default	Usage	Input/Output
GPP_I0	I/O	Standby	3.3V	GPI	DP_DDPD_HPD	Native
GPP_I1	I/O	Standby	3.3V	GPI	HDMI_DDI2_HPD	Native
GPP_I2	I/O	Standby	3.3V	GPI	VGA_DDI3_HPD	Native
GPP_I3	I/O	Standby	3.3V	GPI	U2_BA4	Input
GPP_I4	I/O	Standby	3.3V	GPI	U2_BD7	Input
GPP_I5	I/O	Standby	3.3V	GPI	DP_DDPD_CTRLCLK	Native
GPP_I6	I/O	Standby	3.3V	GPO	DP_DDPD_CTRLDATA	Native
GPP_I7	I/O	Standby	3.3V	GPI	HDMI_DDI2_CTRLCLK	Native
GPP_I8	I/O	Standby	3.3V	GPO	HDMI_DDI2_CTRLDATA	Native
GPP_I9	I/O	Standby	3.3V	GPI	N/A	Input
GPP_I10	I/O	Standby	3.3V	GPO	DDPD_CTRLDATA	Input

GPIO	I/O/NC	Power	Tol	Default	Usage	Input/Output
GPD0	I/O	DSW	3.3V	Native	PCH_BATLOW#	Input
GPD1	I/O	DSW	3.3V	Native	PCH_ACPRESENT	Input
GPD2	I/O	DSW	3.3V	Native	LAN_WAKE#_C	Native
GPD3	I/O	DSW	3.3V	Native	PWRBTN#	Native
GPD4	I/O	DSW	3.3V	Native	SLP_S3#	Native
GPD5	I/O	DSW	3.3V	Native	SLP_S4#	Native
GPD6	I/O	DSW	3.3V	Native	N/A	Native
GPD7	I/O	DSW	3.3V	Native	N/A	Native
GPD8	I/O	DSW	3.3V	Native	N/A	Native
GPD9	I/O	DSW	3.3V	Native	N/A	Native
GPD10	I/O	DSW	3.3V	Native	N/A	Native
GPD11	I/O	DSW	3.3V	Native	LAN_DISABLE#	Native

SIO_GPIO(IT8625E)

GPIO	USAGE	Input/Output	NOTES
GP10	PWR_LED	Output	LED drive signal
GP11	PCIRST#2	Output	PCIE reset signal
GP12	PCIRST#1	Output	LPC Debug & TPM reset signal
GP13	5VSB_CTRL#	Output	DSW signal
GP14	SMI#	Output	SMI signal
GP15	AUX2_ FAN_PWM	Output	Fan speed control
GP16	AUX2_ FAN_TAC	Input	Fan speed sense
GP17	RIB#	Input	Com port signal
GP20	CTSB#	Input	Com port signal
GP21	DCDB#	Input	Com port signal
GP22	SUS_LED	Output	LED drive signal
GP23	SIO_DPWROK	Output	DSW signal
GP24	RTSB#	Output	Com port signal
GP25	DSRB#	Input	Com port signal
GP26	SOUTB	Output	Com port signal
GP27	SINB	Input	Com port signal
GP30	ATX_PWROK_R	Output	PSU power OK
GP31	CTSA#	Input	Com port signal
GP32	RIA#	Input	COM port signal
GP33	DCDA#	Input	COM port signal
GP34	RESETCONI#	Input	De-bounce signal

GPIO	USAGE	Input/Output	NOTES
GP35	RESETCONO#	Input	De-bounce signal
GP36	SYSFAN_PWM	Output	Fan speed control
GP37	SYSFAN_TAC	Input	Fan speed sense
GP40	NA	NA	NA
GP41	SINA	Input	COM port signal
GP42	SUSWARN#	Input	DSW signal
GP43	IO_SMBDATA	Output	SM BUS
GP44	SIO_H_PECI	Input	PECI Signal
GP45	DSRA#	Input	Com port signal
GP47	SIO_WAKE#	Input	Wake up signal from LAN
GP50	DSW_EN	Input	Pin strap which enable DSW
GP51	CPUFAN_PWM	Output	Fan speed control
GP52	CPUFAN_TAC	Input	Fan speed sense
GP53	SLP_S4#	Output	ACPI signal
GP54	SIO_PME#	Output	Power manager signal
GP55	RSMRST#	Output	DSW signal
GP56	MSCLK	Output	Mouse clock out
GP57	MSDATA	Input	Mouse data in
GP60	KBCLK	Output	keyboard clock out
GP61	KBDATA	Input	Keyboard data in
GP62	KBRST#	Input	Keyboard reset

GPIO	USAGE	Input/Output	NOTES
GP63	SLP_SUS#_C	Input	DSW signal
GP64	NA	NA	NA
GP65	NA	NA	NA
GP66	NA	NA	NA
GP67	NA	NA	NA
GP70	RND0	I/O	LPT signal
GP71	RND1	I/O	LPT signal
GP72	RND2	I/O	LPT signal
GP73	RND3	I/O	LPT signal
GP74	RND4	I/O	LPT signal
GP75	RND5	I/O	LPT signal
GP76	RND6	I/O	LPT signal
GP77	RND7	I/O	LPT signal
GP80	PRSLCT	Input	LPT signal
GP81	PRPE	Input	LPT signal
GP82	PRBUSY	Input	LPT signal
GP83	PRACK#	Input	LPT signal
GP84	LPT_SLIN#	Output	LPT signal
GP85	PRINIT#	Output	LPT signal
GP86	PRAFD#	Output	LPT signal
GP87	PRSTB#	Output	LPT signal

GPIO	USAGE	Input/Output	NOTES
GP90	NA	NA	NA
GP91	NA	NA	NA
GP92	NA	NA	NA
GP93	NA	NA	NA
GP94	NA	NA	NA
GP95	PS2_DET#_R	Input	PS2 Detect
GP96	SKTOCCT#_SIO	Input	PROC detect signal
GP97	SELECT#_SIO	Input	PROC SELECT
GPOA0	GPOA0	Input	Pin strap for Bay-Trail or Not Bay-Trail Platform
GPA1	NA	NA	NA
GPA2	IO_SMBCLK	Input	SMB signal
GPA3	NA	NA	NA

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GPIO Table

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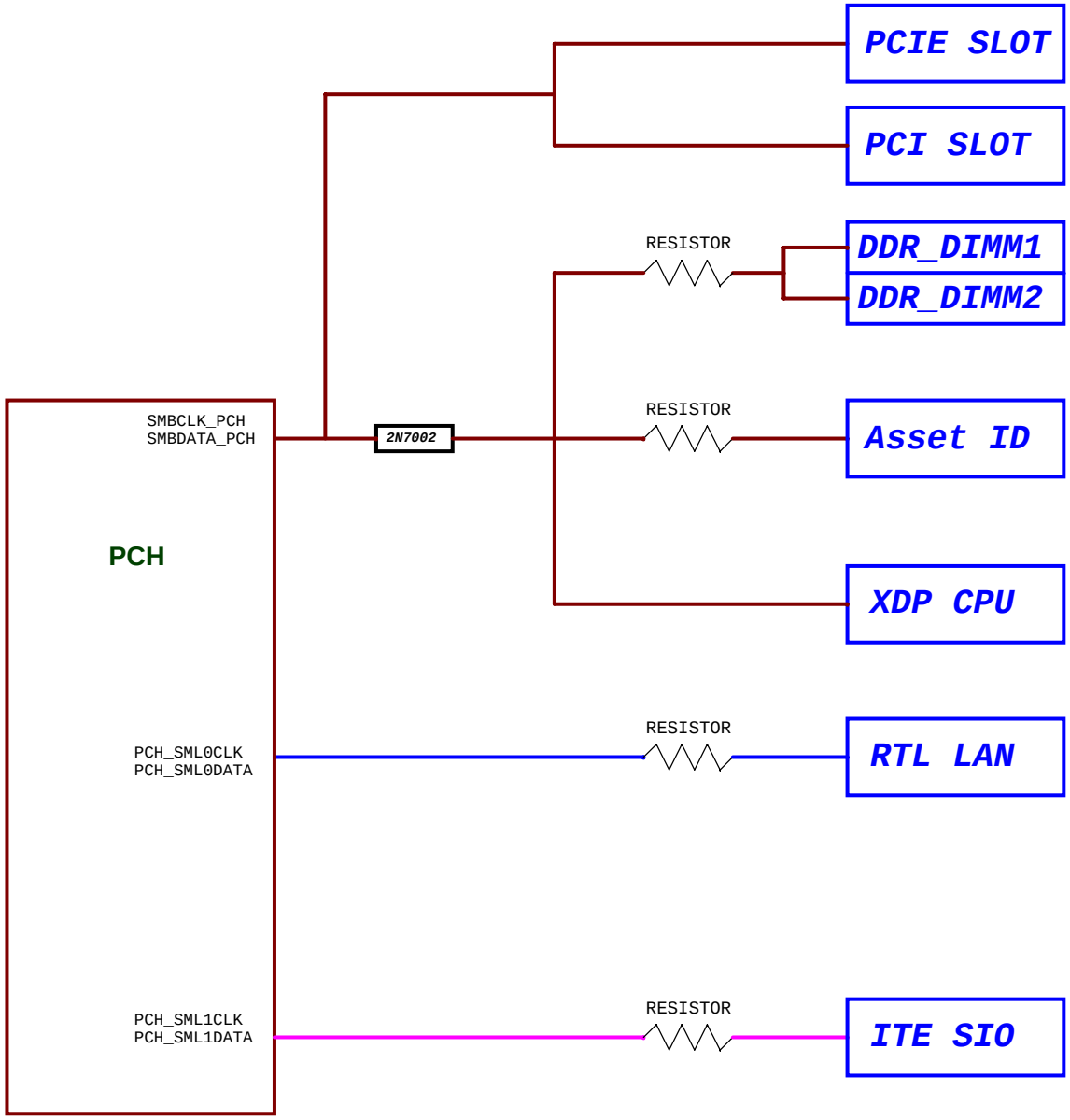
1.0



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Title: SMBUS Block Diagram		
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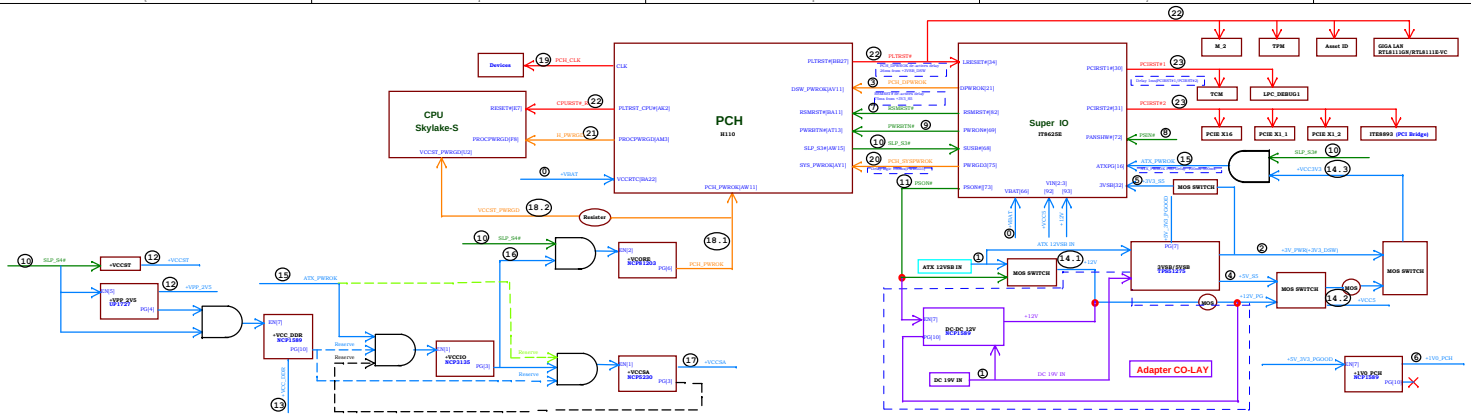


DSW Timings

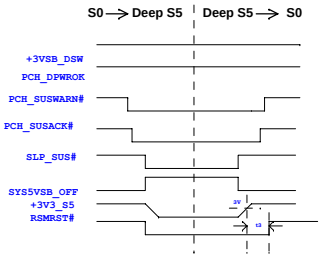


Table 11-2. DSW Timings Parameter

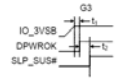
Symbol	Typ.	Description
t_1	75ms	SYS_3VSB voltage over 3.0V to the rising edge of RSMRST#

G3 → Deep S5 → S5

source	destination		G3	DEEP S5	S5
board	PCH	VBAT			
board	PCH	RTCRST#			
PSU	board	+5VSB_DSW			
board	PCH	+3VSB_DSW			
board	PCH	PCH_DPWROK			
PCH	SIO	PCH_SUSWARN#			
SIO	PCH	PCH_SUSACK#			
PCH	SIO	SLP_SUS#			
board	board	+5V_S5			
board	PCH	+3V3_S5			
board	PCH	+1V0_PCH			
SIO	PCH	RSMRST#			

Symbol	Typ.	Description
t_1	26ms	The rising edge of IO_3VSB to rising edge of DPWORK

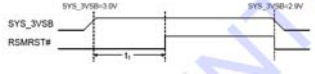
Figure 11-20. DPWORK Timings



11.12 RSMRST# and ACPI Power Control Signal Timings

Symbol	Parameter	Typ.	Unit
t_1	RSMRST# de-actives delay from SYS_3VSB=3V	75	msec

Figure 11-11. RSMRST# Timings



VR Start up Timings

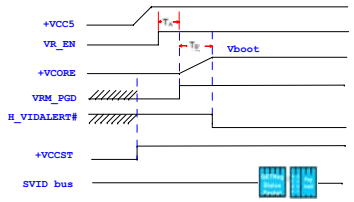


Table 5-1. VR Start up and Enable Timings

	Description	Min	Typ	Max	Note
T_A	VR_EN to VR_Ready. Controller ready accept SVID command			2.5 ms	PWM IC must complete all internal analog and digital configurations and reset protocols during T_A. Duration may be disclosed to CPU through register 2Dh. With Multi-VR Config bit 0 set, VR_Ready should only de-assert for faults.
T_B	Non-zero V_{BOOT} ramp time. May start during T_A but not later than at the end of T_A –to Alert# assertion.			VID/ Slow	SetVID_Slow rate is required soft start ramp for non-zero V_{BOOT}

Figure 40-1. SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

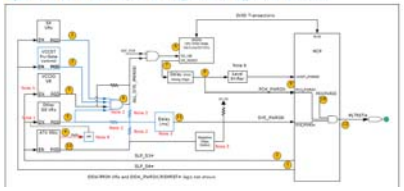


Figure 40-2. SKL S Flow Diagram for RSMRST_PWRGD# Generation

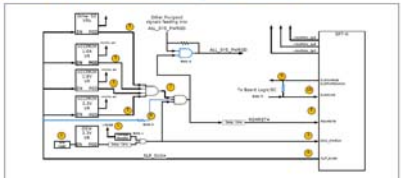


Figure 11-16. PCIRST#1, PCIRST#2 and PCIRST#3 Signal Timings

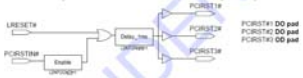
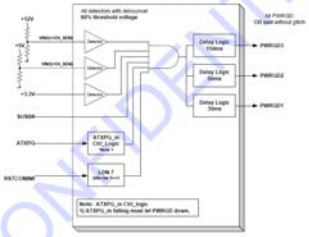


Figure 11-14. PWRGD1/2/3 Signal Condition



MSI MICRO-STAR INT'L CO.,LTD.
Power Sequence Block Diagram
B41GBM

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title

Error/Interrupt Diagram

Size	Document Number	Rev
	IH110M	1.0

Date: Tuesday, July 07, 2015 Sheet 42 of 43

0.1 to 0.2 change list

Page6: Reserve +VCCST circuit
Page9: R190 change to 100K
Page9: Add SW disable ME
Page9: Update PCH_PWROK circuit
Page9: PCH_SPI_MOSI/PCH_SPI_MISO add pull high
Page14: Remove CLR_CMOS1
Page11: SPIO_IO3 add pull down
Page11: SPI power change to +3V3_S5
Page12: SPI power change to +3V3_S5
Page19: Update USB power circuit
Page19: Change kernel debug detect pin
Page21: Update VGA power circuit
Page22: SIO change to ITE8625E
Page22: Update PCH_SYSPWROK circuit
Page22: U73 change to I94-3956YOC-N62
Page24: Update AUDIO power circuit
Page24: Update AUDIO power circuit
Page24: MONO IC change to I71-2823B0D-005
Page25: TPM power change to +3V3_S5
Page27: Update +1V0_PCH enable circuit
Page27: +1V0_PCH IC change to I32-1589L0C-005
Page28: Update NET name
Page28: U3 change to I9C-1727P0C-U33
Page28: Update +VPP_2V5/ +VCC_DDR EN circuit
Page29: Update VR_EN circuit
Page32: Update +VCC1O enable circuit
Page32: Update +VCCSA enable circuit
Page34: GND name fail
Page34: Update +VCCS/+VCC3V3 sequence
Page35: Update ATX_PWRGD circuit
Page35: Reserve dual power LED circuit
Page35: Add Power on/down sequencing circuit

WITE: Detailed information refer to document

0.2 to 0.2-1 change list

Page3-7: CPU PCB Footprint change to ZIF_SOCK1151_Y_7963
Page6: Remove EC67/68
Page9: Change some single resister to RES ARRAY
Page11: Change some single resister to RES ARRAY
Page14: PCIERST# GPIO change
Page14: Change some single resister to RES ARRAY
Page18: Update SYS_FAN name
Page19: D11/D12/D13/D14/D20/D22/D23 change to DOG-0200529-A68
Page20: D25 change to DOG-0200529-A68
Page22: SIO CLKIN reserve
Page22: D28 change to DOG-0200529-A68
Page22: SIO_PME# pull high power change to +3V3_S5
Page22: Change some single resister to RES ARRAY
Page25: TCM change GPIO
Page26: R556 change to 100ohm
Page26: Rear IO USB power update circuit
Page26: Update USB discharge circuit
Page27: R831 change to 16K,R362 change to 4.02K
Page28: C461 change to 22p
Page28: R601 change to 18K,C461 change to 470P
Page32: C612/609/608 change to 47uF
Page33: C639 change to 100P
Page34: EC56 change to C71-5610611-N07
Page34: Update +3V3_S5 circuit
Page34: PWR2 change to N93-04M0821-H06
Page35: C856 change to 10u
Page35: ATX POWER change to N93-10M0251-H06

0.2-1 to 0.3 change list

Page3-7: CPU PCB Footprint change to ZIF_SOCK1151_Y_7963_1
Page4: R1043/C861 remove to close CPU
Page8: C9 change to 33pf
Page8: C108 change to 82pf
Page8: C227/C236 change to 10u
Page9: add C861 39pf
Page9: R81 stuff 150K
Page9: add R972 33ohm
Page9: C881 BOM remove
Page9: C108 change to 22PF
Page9: RES ARRAY change to single resister
Page11: R99 change to 0ohm
Page11: RES ARRAY change to single resister
Page11: add 4M BOM, remove Lenovo SPI debug head
Page14: add R154
Page14: add R155
Page17: R185 change to 33ohm
Page17: stuff D15/D18/C779/C778/ C797/C780
Page17/20: U8/U18/U19/U20/U21/U22 change to DOG-05A0300-I14
Page19: reserve D89
Page19: U51/U52 EN circuit update
Page19: stuff D15/D18/C779/C778/ C797/C780
Page20: stuff D23/D18/D19/D20/D21/D22
Page21: C743 unstuff ,C744 stuff
Page22: stuff C300
Page22: Q53&R1033 BOM reserve
Page22: R1033 change to 0603 size
Page22: C878 change to 1u,C724 change to 22uf
Page22: Follow Lenovo request change R1033 to 120ohm
Page22: stuff R995、C176 change to 100pf、R374 change to 24ohm
Page23: C332 change to 15pf
Page24: C703 change to 100pf
Page24: R465 change to 30ohm , C374 stuff 10pf
Page25: add R1049
Page25: add R972
Page25: C410 change to 56pf
Page25: C410 change to 56pf
Page25: Follow power team request change R831 to 14.7K
Page28: C461 change to 100pf
Page28: +VCC_DDR add some caps
Page29: BOM remove C189
Page29: VRM EN circuit update
Page29: Update MONO Amplifier circuit
Page29: add R1048、C786 change to 47pf
Page31: BOM remove C189
Page32: VCCIO_PGD/VCCSA_EN circuit update
Page33: C461 change to 100pf
Page34: PWR2 Update library and add note
Page35: reserve C684
Page35: Power down sequence circuit update

0.3 to 0.4 change list

Page6: Add R1070
Page6: C911 change to 0.22U
Page9: C786 change to 100PF 、add C915、C881 change to 150PF
Page11: C47/C48 change to 33pF
Page14: R154/R166/R365 change to 33Ω
Page19: Add D20、U76U、 D91
Page19: U16 stuff,U76 un-stuff
Page19: BOM remove U27/U67/U68/U36/U16/U17/U61/U69/U70/U37/U57
Page22: Reserve C922/C923
Page22: Reserve R406/R1073
Page22: R1049/R1050/R374change to 33Ω、add R1069/ R551、C154 change to 47Pf、C137 remove close SIO PIN68
Page23: BOM remove U40/U41
Page23: Remove RT1/RT6/R406
Page24: BOM remove U24/U71
Page26: Remove XDP port
Page26: Add R1072/ reserve C125
Page26: Update XDP port footprint
Page28: C473 BOM remove
Page28: C849 change to 0.1U
Page29: C516 change to 330pF
Page29: R674 change to 4.87K、R651/R656/R657/R675/R678 size change to 0402
Page32:R30 change to 33K
Page34: R961 change to 15K
Page34: Add R1071,reserve C921
Page34: Reserve C917/C918/C919/C920
Page34: Remove reserve +3V3_DSW circuit
Page34: C866 stuff 、R961 change to 14.7k
Page34: BOM stuff C684/C692/C686/C687/C695/C696C/C688/C770
Page35: C880 stuff
Page35: C893 BOM remove
Page35: C893 change to 330pF

0.4 to 0.5 change list

Page8: R580/R591 change to 240Ω
Page19: F_USB2 PIN2 connect to GND
Page28: U50 change to NCT3103S
Page28: Add R1074/R1075/R1076/R1077/R1078/R1079/Q159
Page28: Reserve C924,C826 change to 1000pF,EC31 un-stuff
Page29: C542 change to 100pF/C543 change to 820pF

0.5 to 1.0 change list

Page9: ME_DIS 3PIN change to 2PIN,reserve R1080
Page12: Add C925/C926,reserve C927
Page16: BOM add EC4
Page27: BOM remove C751

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1.0