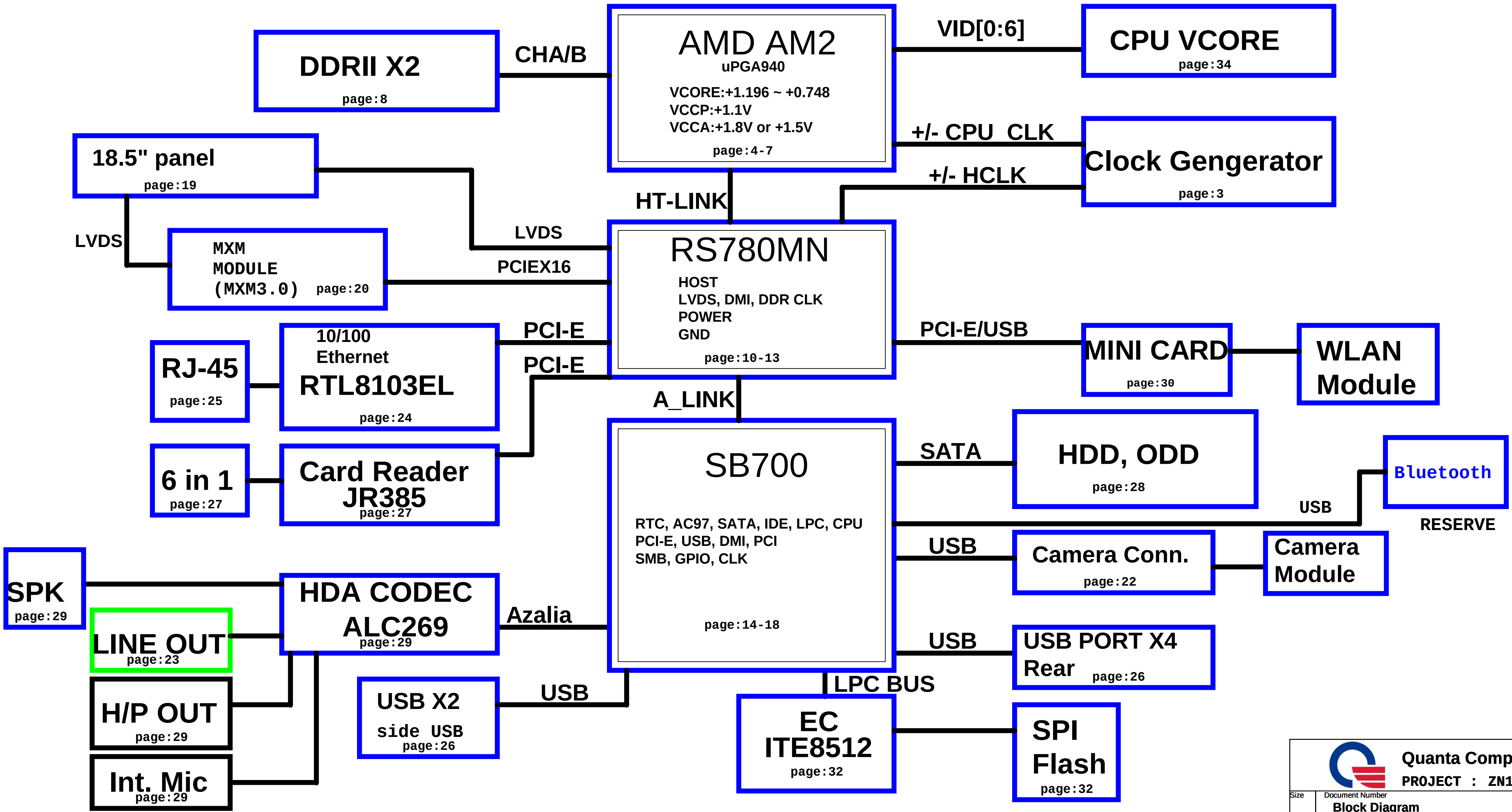
Amazon LCD PC Block Diagram

1



Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	Block Diagram	B
Date: Friday, May 08, 2009	Sheet 1 of 41	

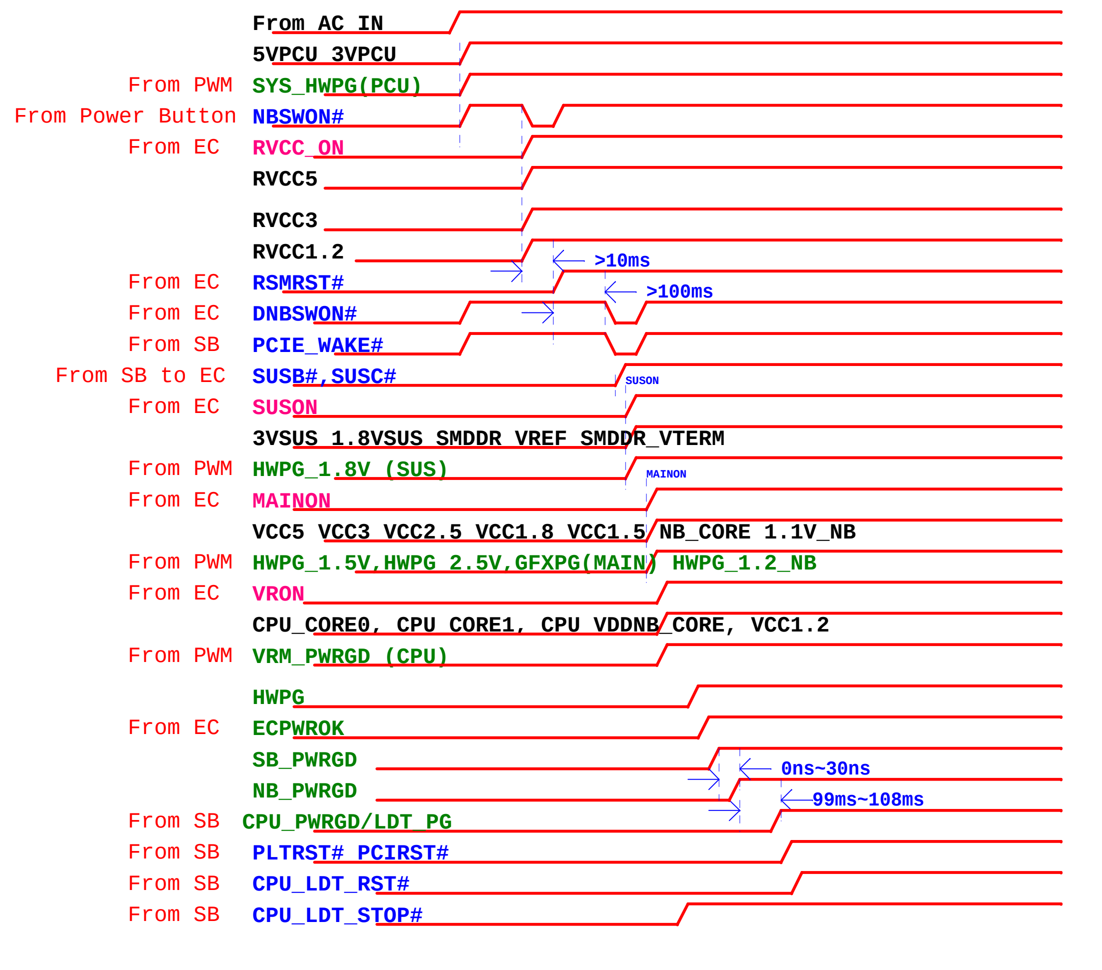
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : VCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6 : BOT

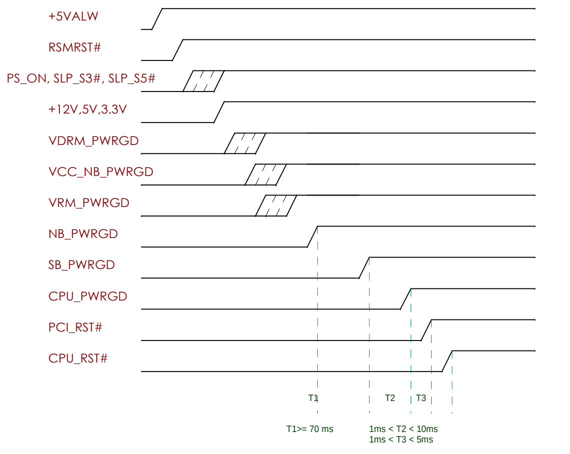
Voltage Rails

Power	Voltage	S0~S2	S3	S4	S5	Ctl Signal
15VPCU	15V	V	V	V	V	
5VPCU	5V	V	V	V	V	VIN
3VPCU	3V	V	V	V	V	VIN
RVCC3	3V	V	V	V	V	RVCC_ON
RVCC1.2	1.2V	V	V	V	V	RVCC_ON
5VSUS	5V	V	V			SUSD
1.8VSUS	1.8V	V	V			SUSON
VCC5	5V	V				MAIND
VCC3	3V	V				MAIND
VCC1.8	1.8V	V				MAIND
VCC1.5	1.5V	V				MAINON
VCC1.2	1.2V	V				MAINON
CPU_VDDA	2.5V	V				VCC3
NB_CORE	1.2V	V				VRON
SMDDR_VTERM	0.9V	V				SUSON
CPU_CORE	By CPU	V				VR_ON

Power On Sequence

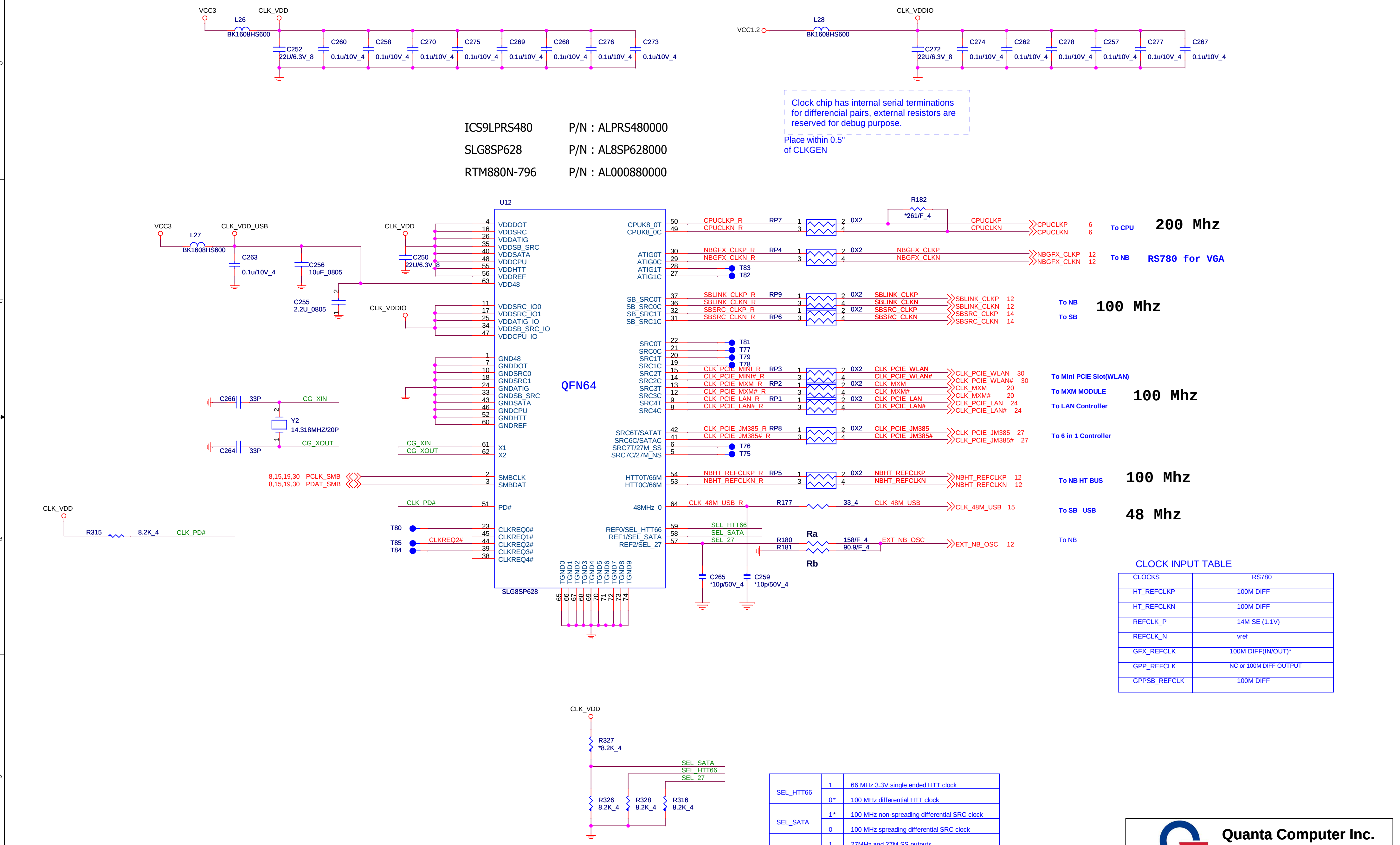


BONEFISH POWER UP SEQUENCE



CLK_GEN_SLG8SP628

ICS9LPRS480	P/N : ALPRS480000
SLG8SP628	P/N : AL8SP628000
RTM880N-796	P/N : AL000880000



CLOCK INPUT TABLE

CLOCKS	RS780
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

Quanta Computer Inc.

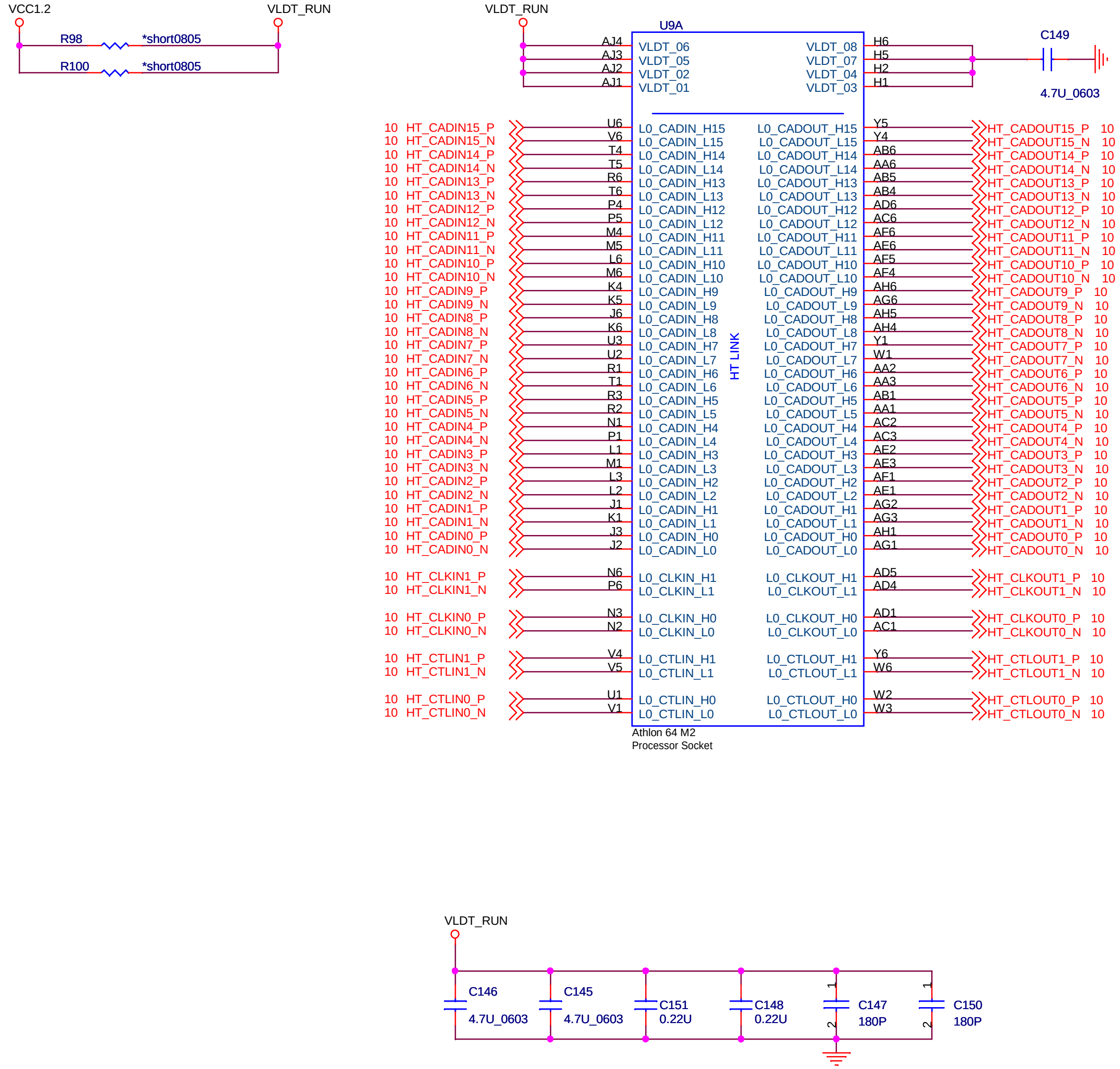
PROJECT : ZN1

Size	Document Number	Rev
	Clock Generator	1A

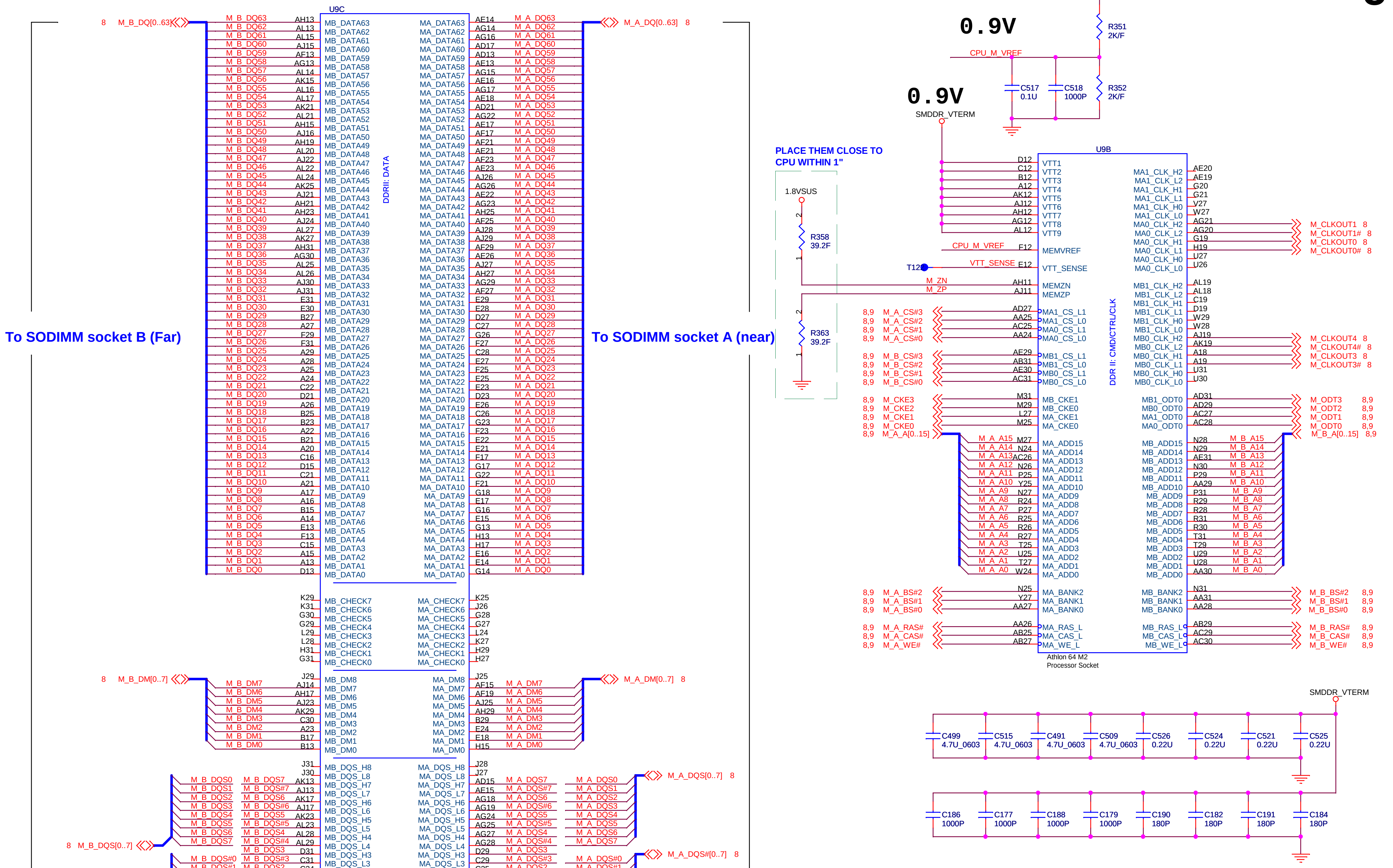
Date: Friday, May 08, 2009 Sheet 3 of 41

CPU HyperTransport Interface

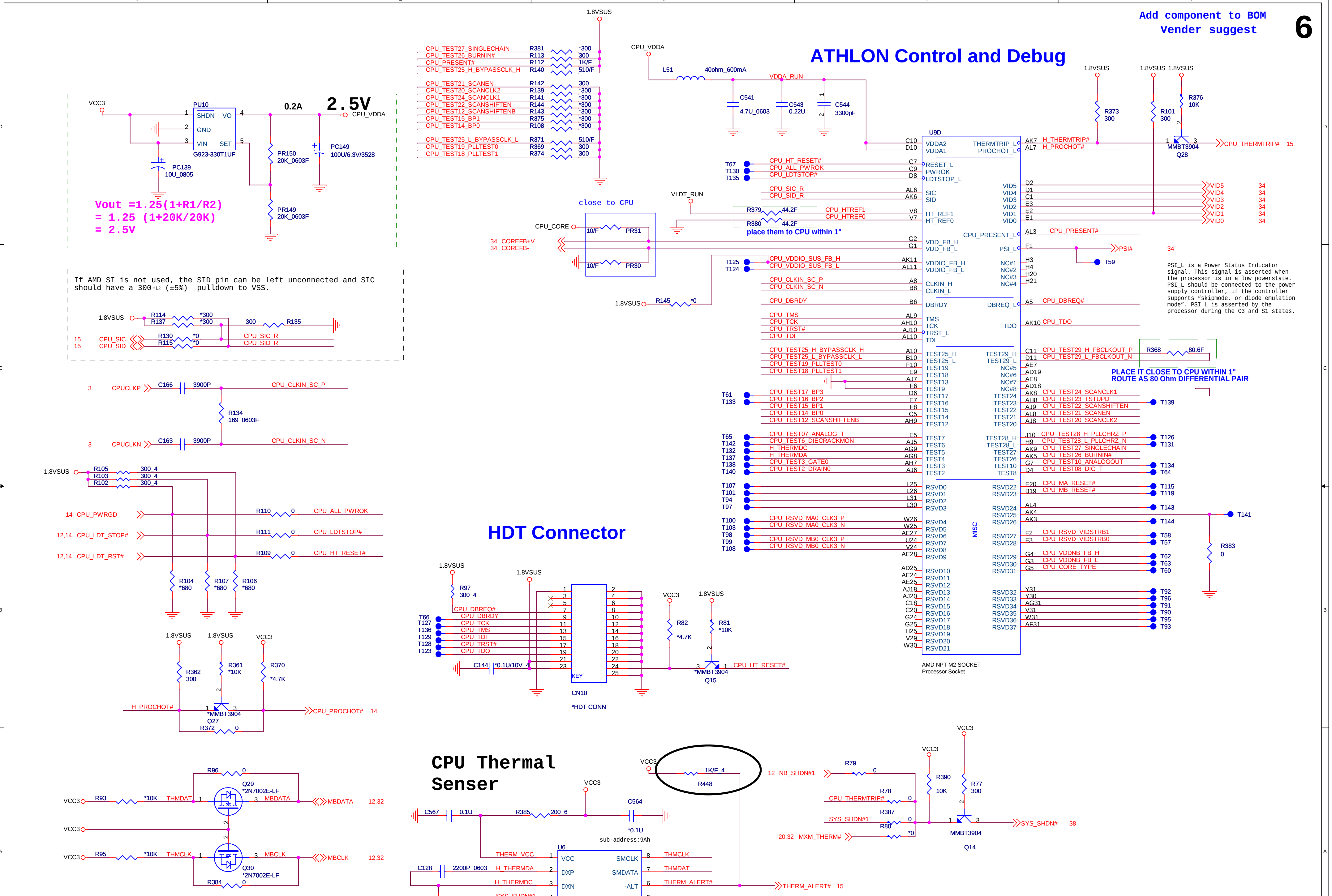
VDDLDTRUNCPU is connected to the VDD_LDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



Processor DDR2 Memory Interface



Quanta Computer Inc.	
PROJECT : ZN1	
Size	Document Number: AMD AM2 DDR II Memory I/F	Rev 1A
Date: Friday, May 08, 2009	Sheet 5 of 41



SMBUS SLAVE ADDRESS	
G781	98 (CPU)

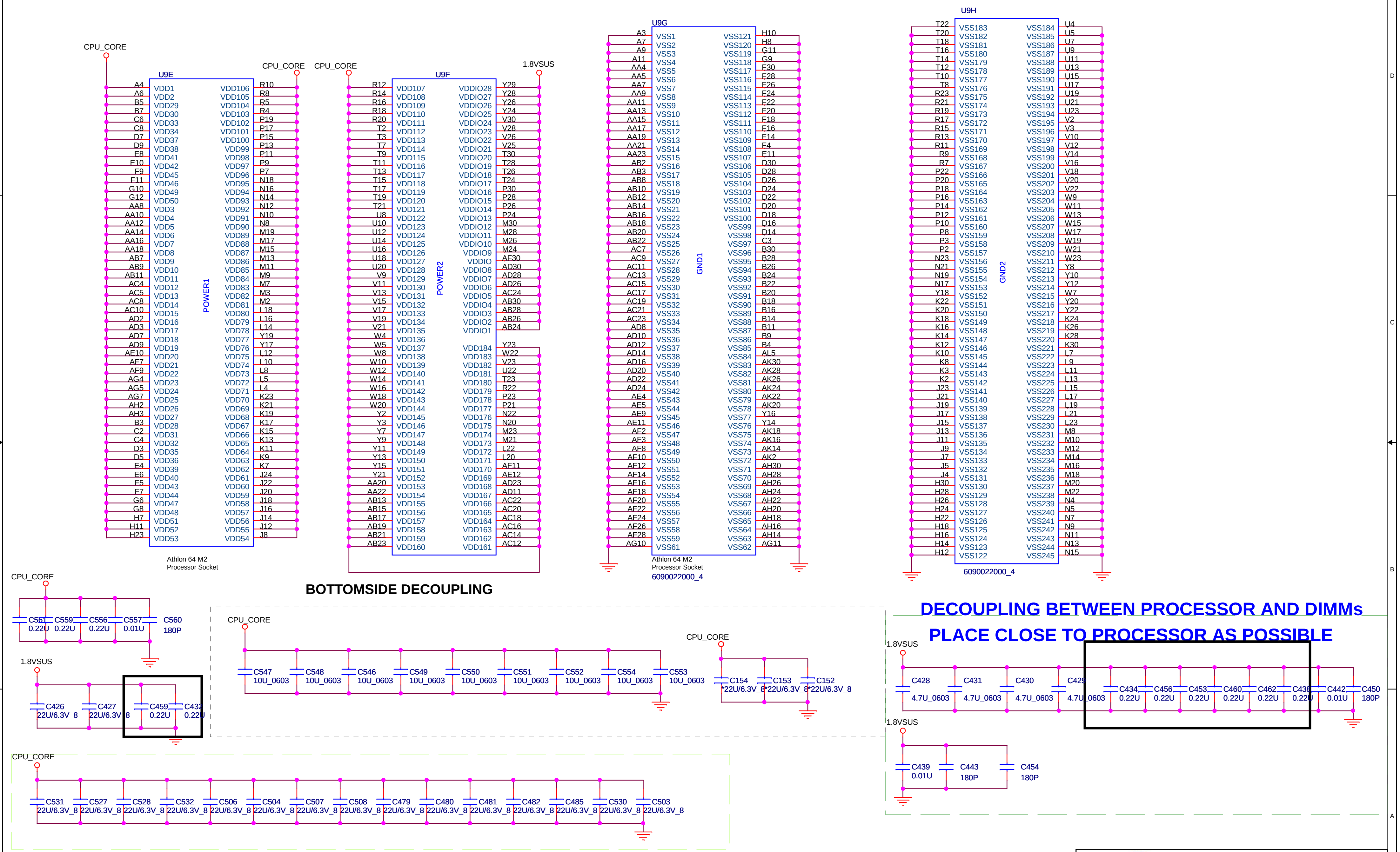
Quanta Computer Inc.

PROJECT : ZN1

Size | Document Number: AMD AM2 CTRL & DEBUG | Rev 1A

Date: Friday, May 08, 2009 | Sheet 6 of 41

PROCESSOR POWER AND GROUND

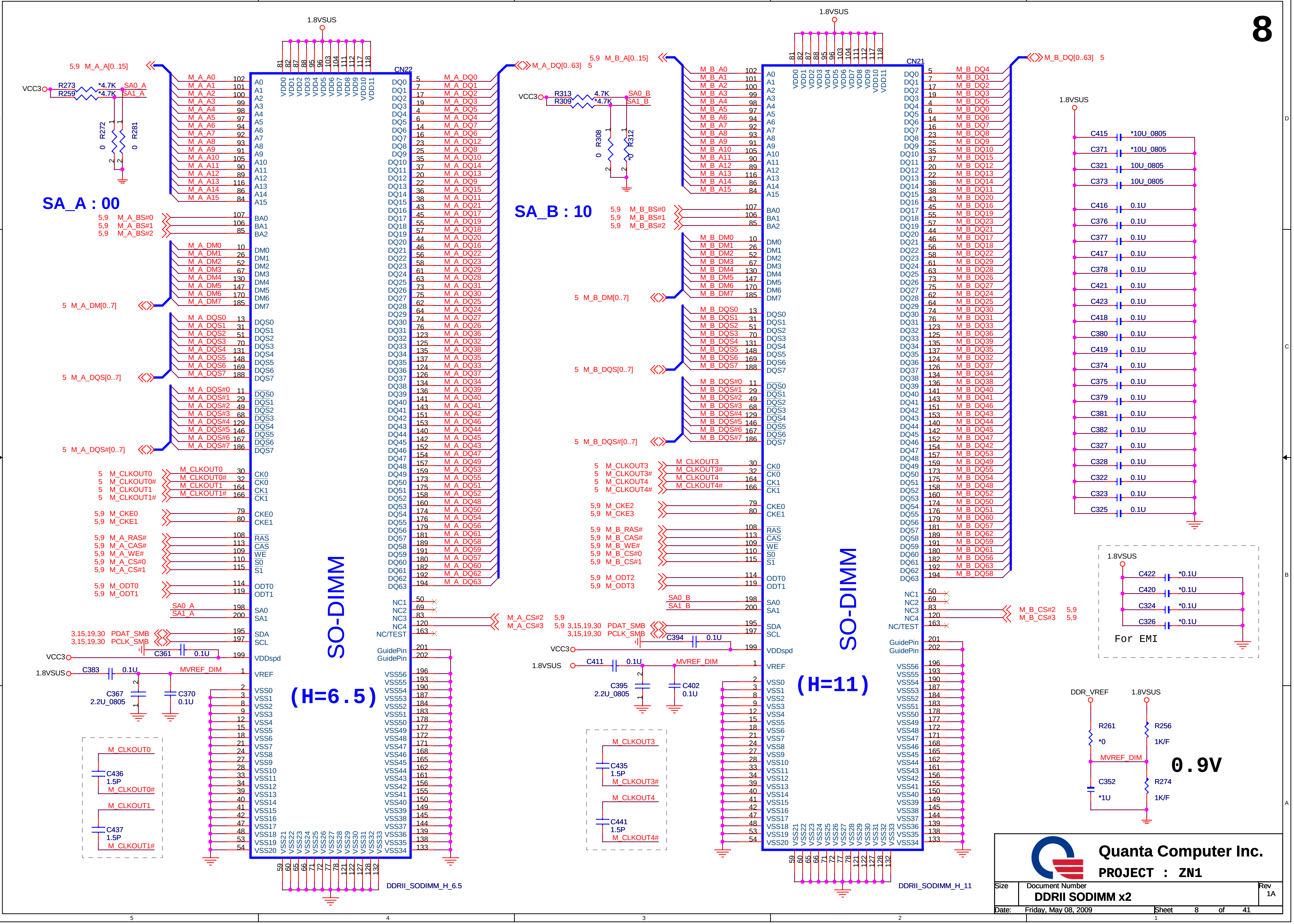


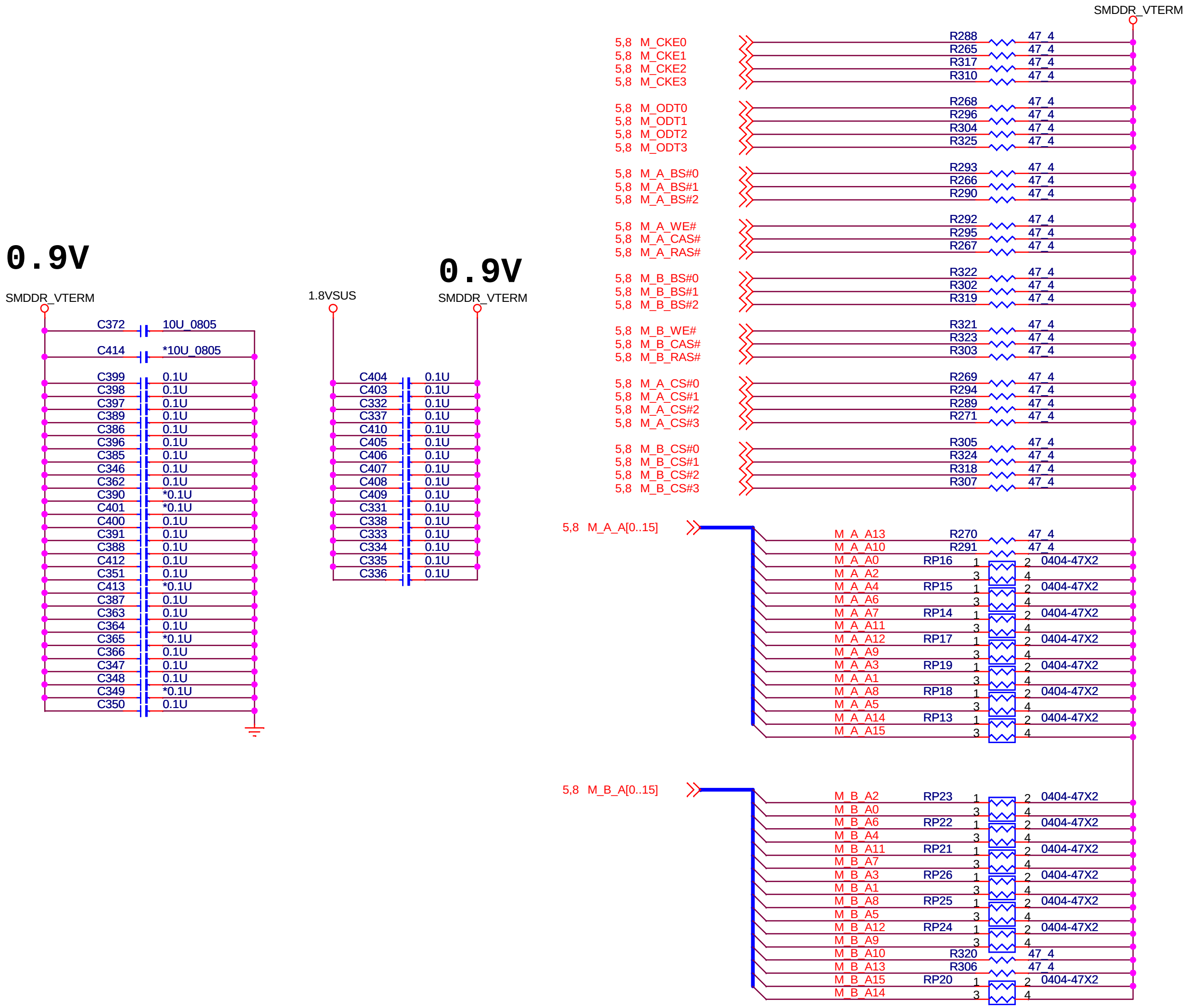
Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	AMD AM2 PWR & GND	1A

Date: Friday, May 08, 2009 | Sheet 7 of 41

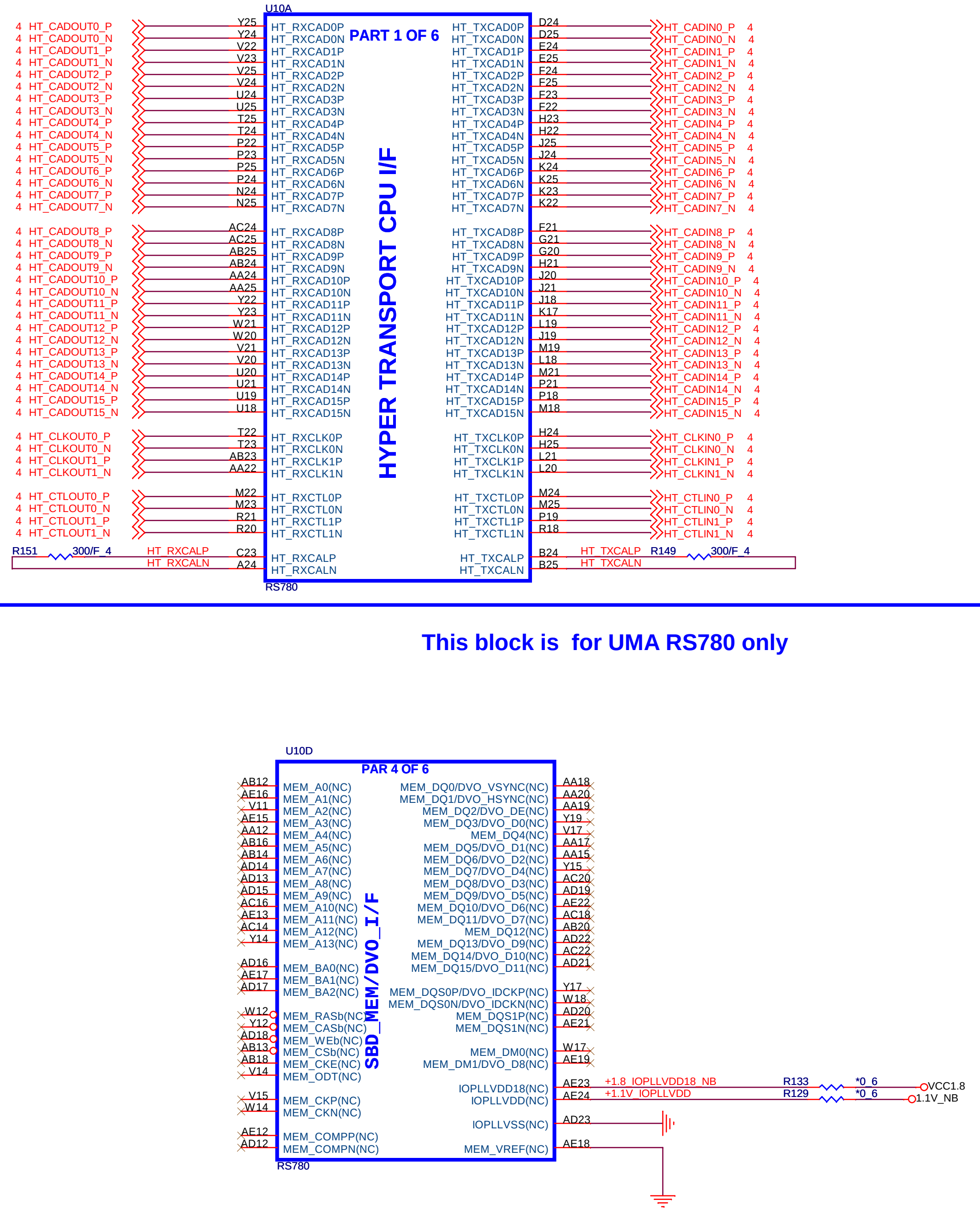

8
SA_A : 00
SA_B : 10
SO-DIMM
(H=6.5)
SO-DIMM
(H=11)
CN22
CN21
1.8VSUS
VCC3
DDR_VREF
MVREF_DIM
0.9V
For EMI
DDRII_SODIMM_H_6.5
DDRII_SODIMM_H_11
Quanta Computer Inc.
PROJECT : ZN1
Size
Document Number
DDRII SODIMM x2
Rev
1A
Date: Friday, May 08, 2009
Sheet 8 of 41



Quanta Computer Inc.

PROJECT : ZN1

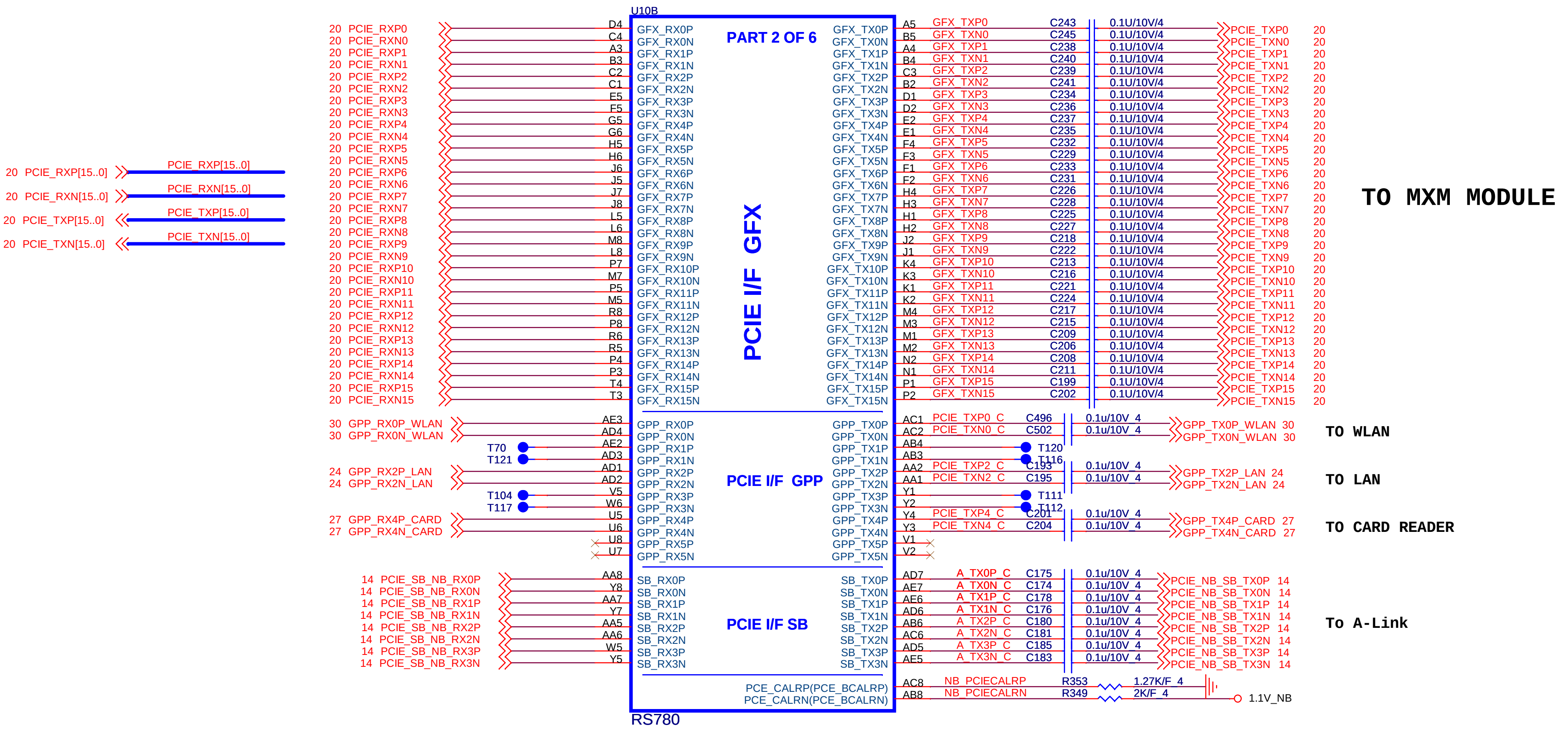
Size	Document Number	Rev
	DDRII TERMINATION	1A
Date: Friday, May 08, 2009	Sheet 9 of 41	



This block is for UMA RS780 only

Quanta Computer Inc.
PROJECT : ZN1

Size	Document Number	Rev
	RS780M HT LINK I/F 1/4	1A
Date: Friday, May 08, 2009	Sheet 10 of 41	

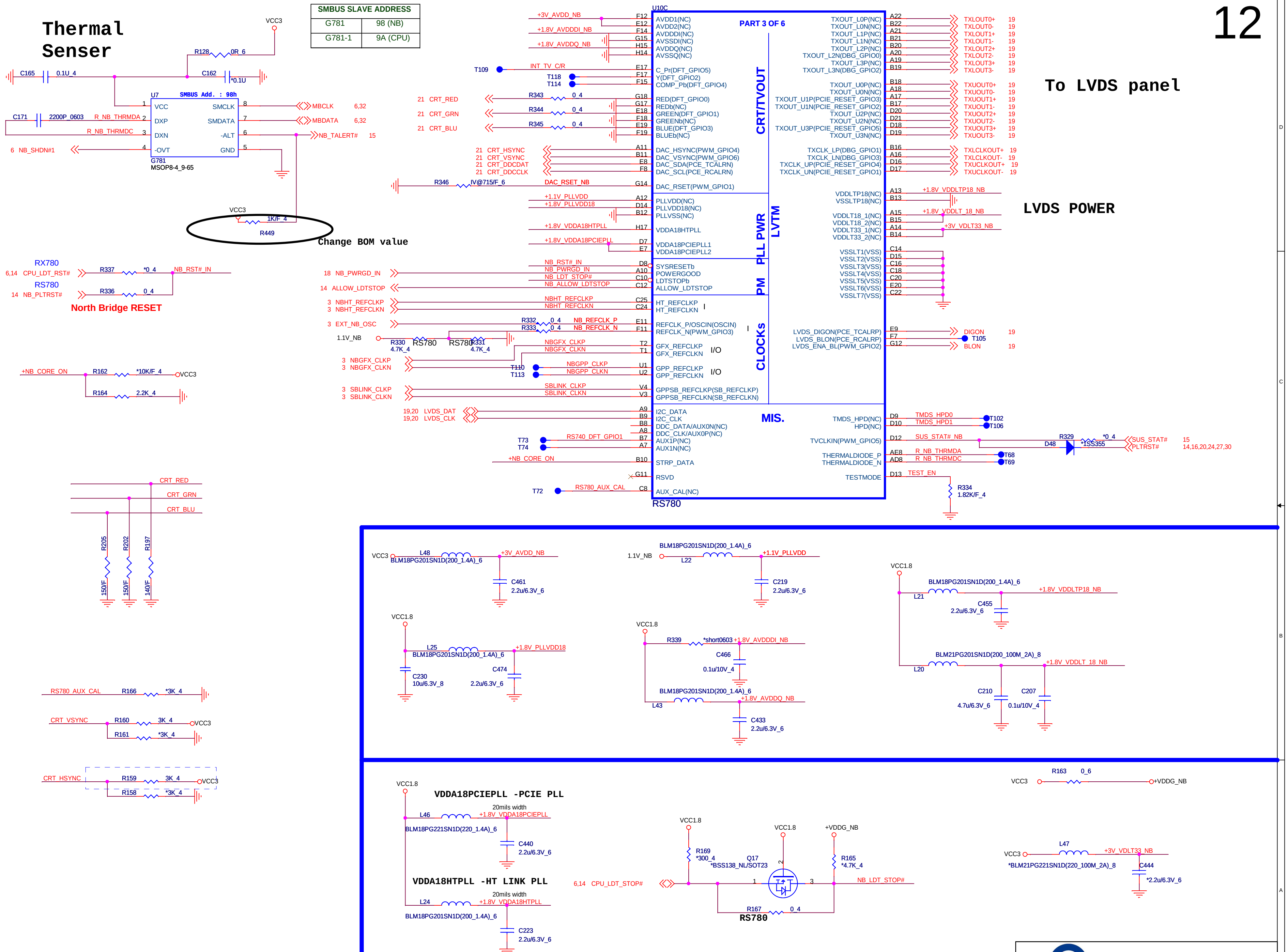


Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	RS780M-PCIE I/F 2/4	1A
Date: Friday, May 08, 2009	Sheet 11 of 41	

SMBUS SLAVE ADDRESS	
G781	98 (NB)
G781-1	9A (CPU)

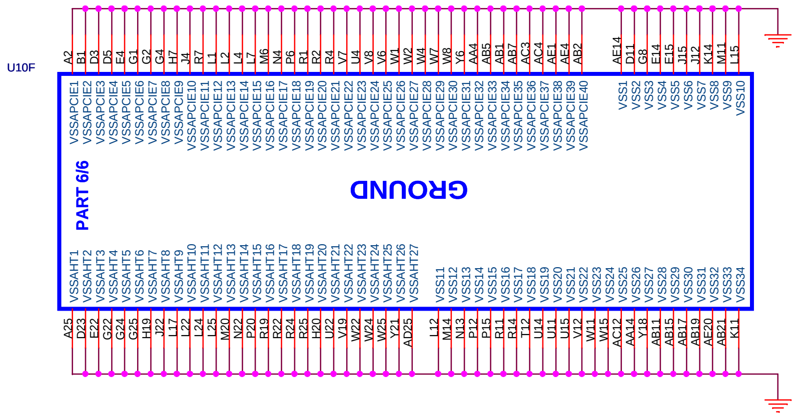


Quanta Computer Inc.

PROJECT : ZN1

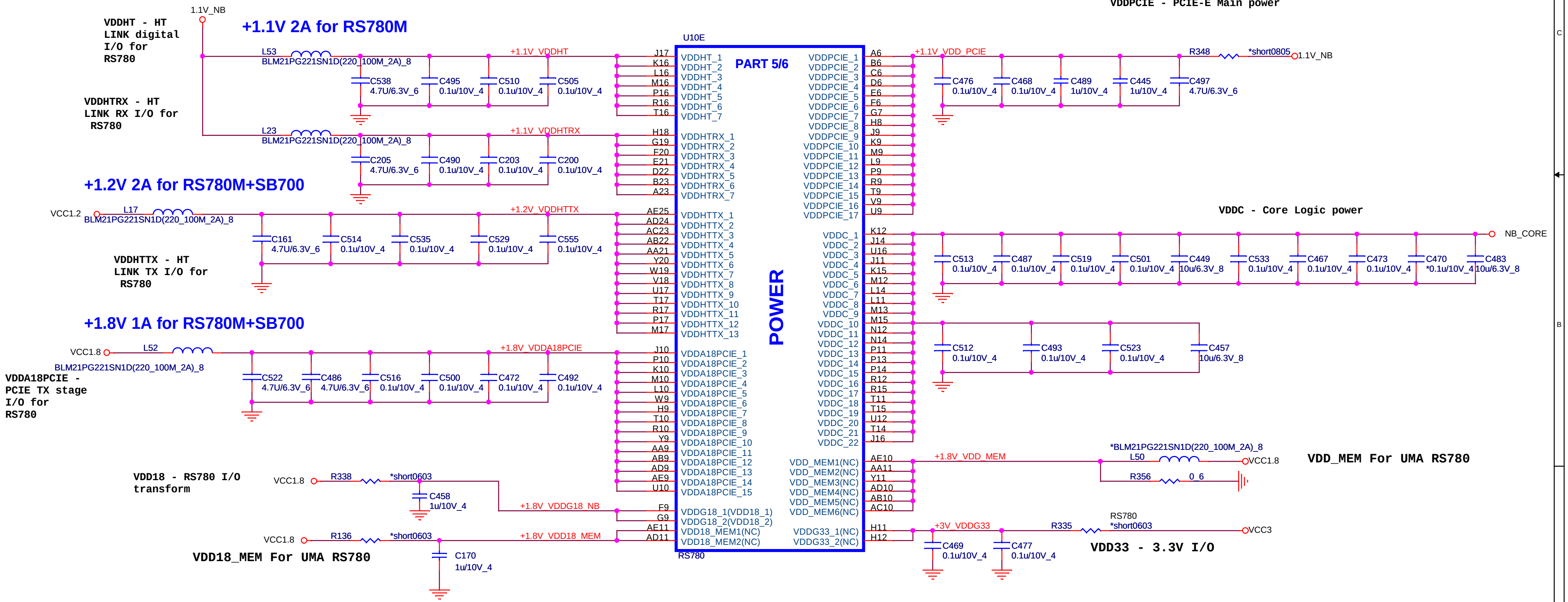
Size	Document Number	Rev
	RS780M-SYSTEM I/F 3/4	1A

Date: Friday, May 08, 2009 Sheet 12 of 41



RS780 POWER DIFFERENCE TABLE

PIN NAME	RS780	PIN NAME	RS780
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

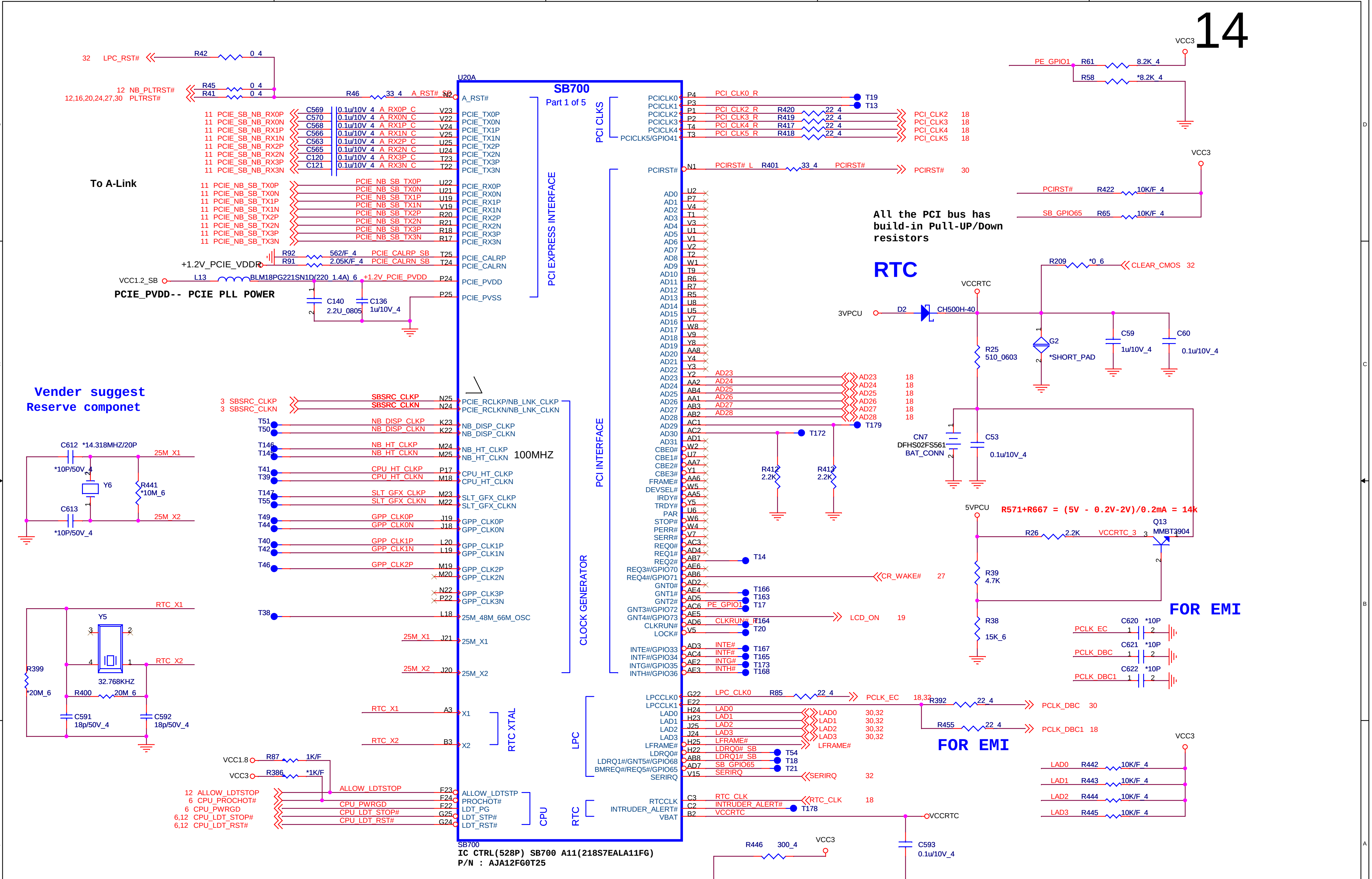


Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	RS780M-POWER4/4	1A

Date: Friday, May 08, 2009 Sheet 13 of 41

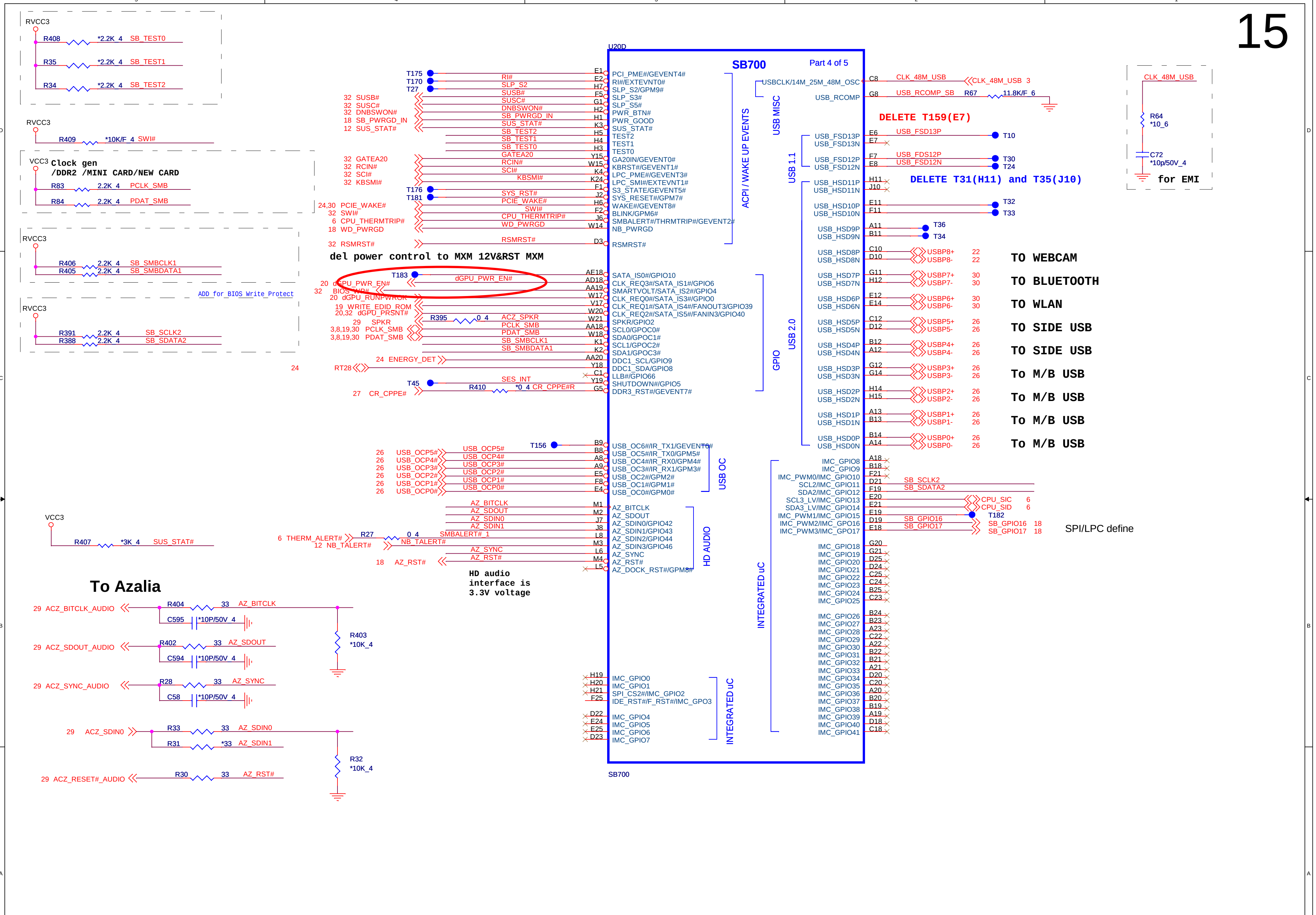


Quanta Computer Inc.

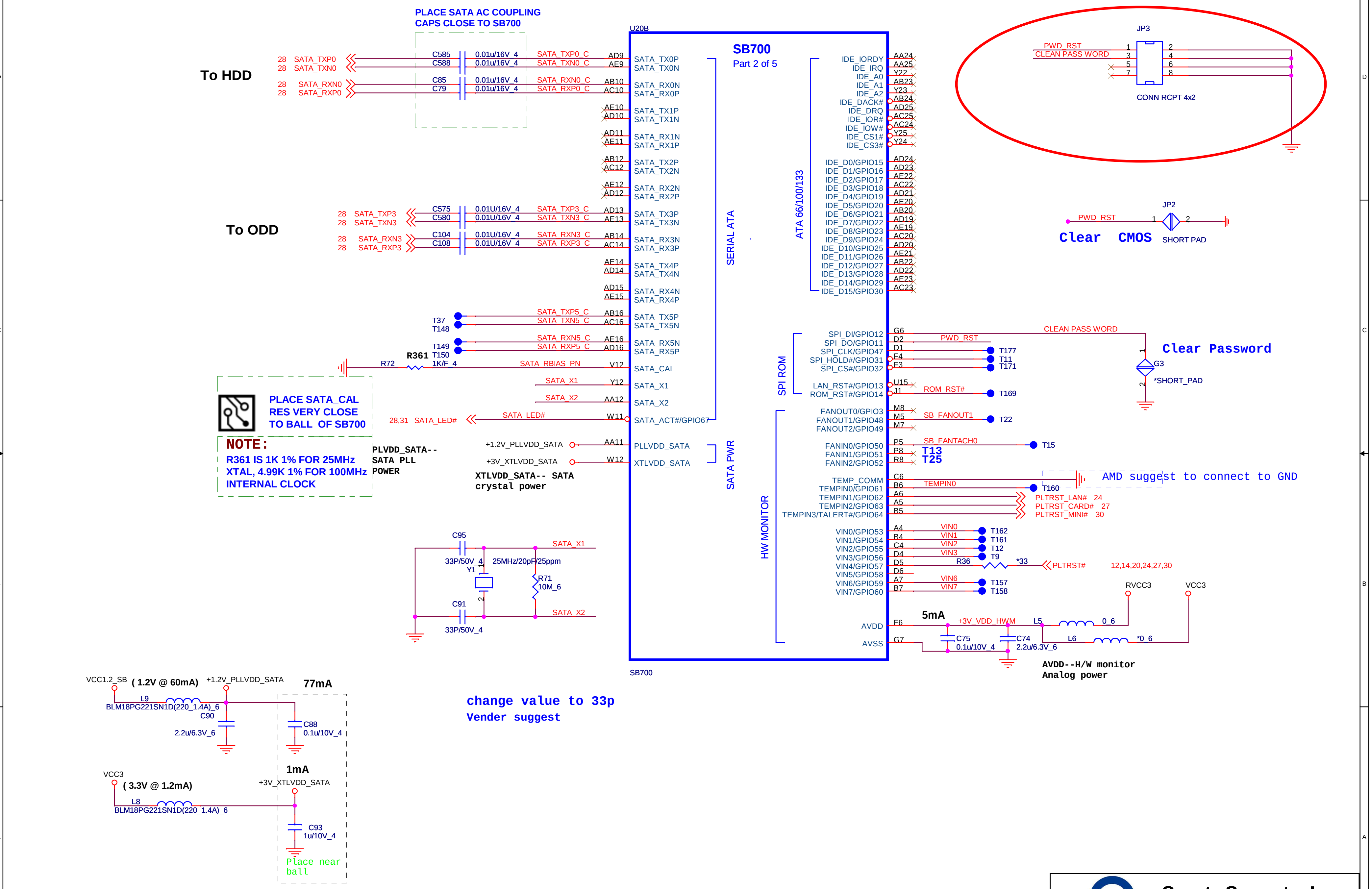
PROJECT : ZN1

Size	Document Number	Rev
	SB700-PCIE/PCI/CPU/LPC 1/4	B

Date: Friday, May 08, 2009 Sheet 14 of 41



Quanta Computer Inc.	
PROJECT : ZN1	
Size	Document Number: SB700-ACPI/GPIO/USB 2/4	Rev 1A
Date: Friday, May 08, 2009	Sheet 15 of 41



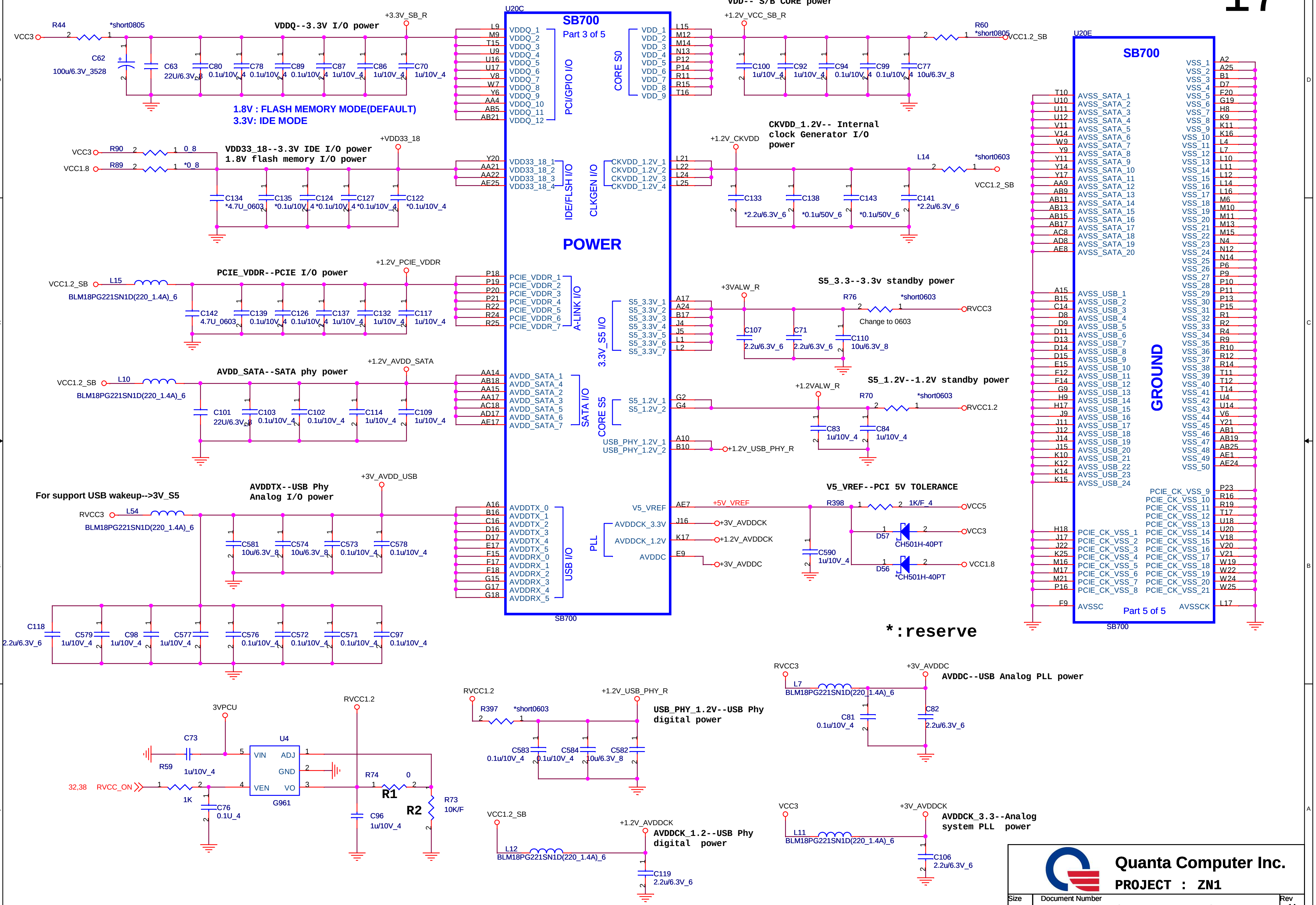
Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	SB700-SATA/IDE/HWM/SPI 3/4	1A

Date: Friday, May 08, 2009 Sheet 16 of 41

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



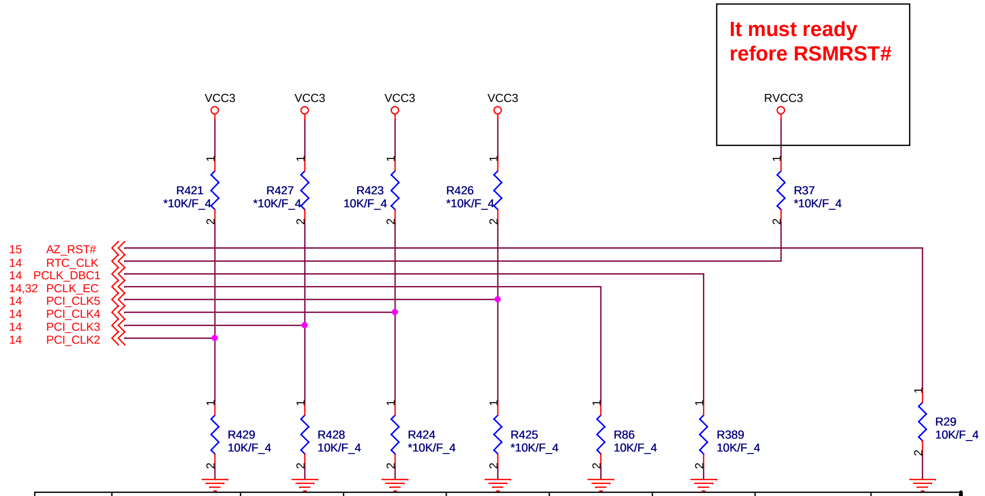
Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	SB700-PWR/DECOUPLING 4/4	1A

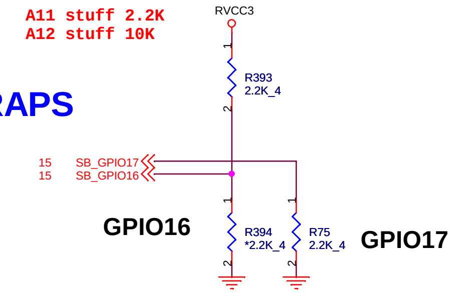
Date: Friday, May 08, 2009 Sheet 17 of 41

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

A11 stuff 2.2K
A12 stuff 10K



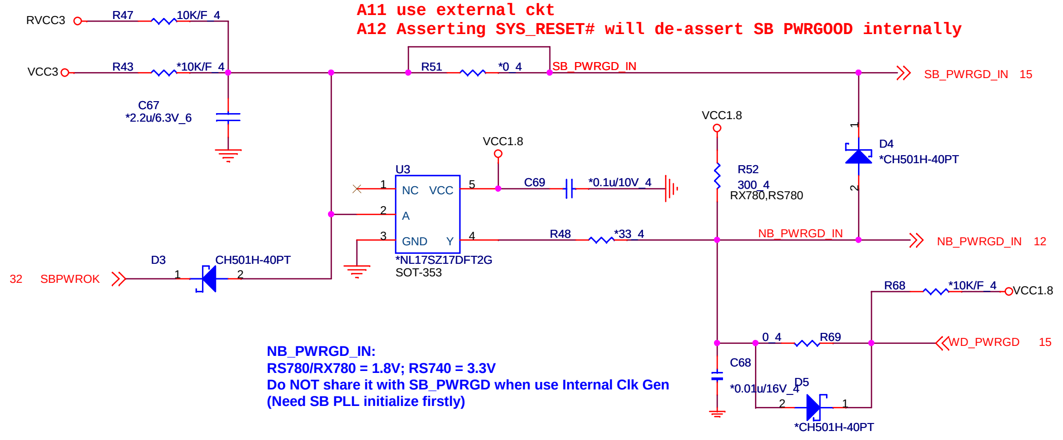
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

EC ENABLED

ENABLE PCI MEM BOOT

TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

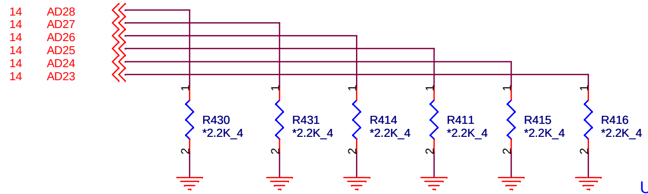
SB_PWRGD
A11 use external ckt
A12 Asserting SYS_RESET# will de-assert SB PWRGOOD internally



NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

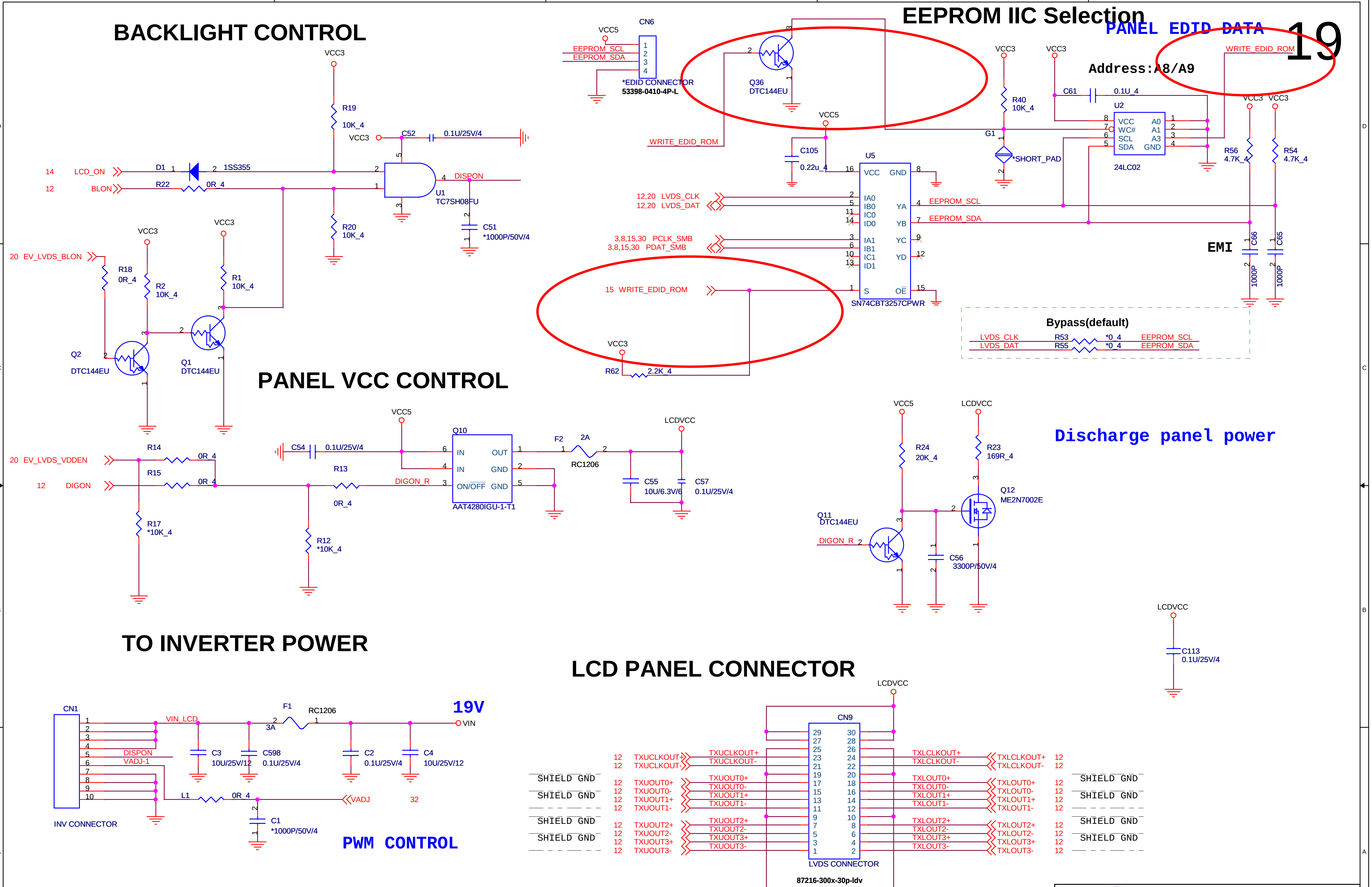
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



Quanta Computer Inc.

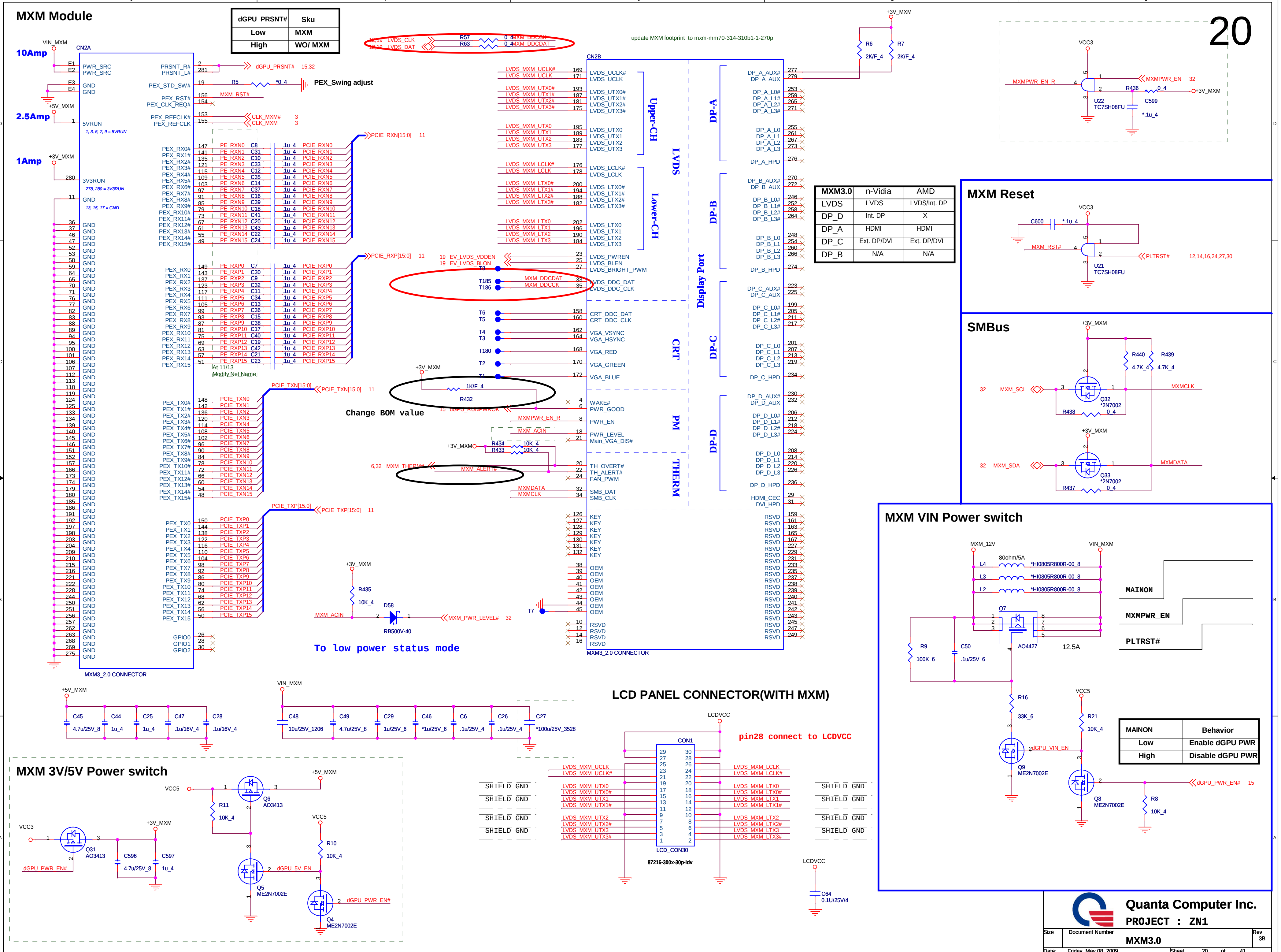
PROJECT : ZN1

Size	Document Number	Rev
	LCD PANEL/WEBCAM	A

Date: Friday, May 08, 2009 Sheet 19 of 41

MXM Module

dGPU_PRSNT#	Sku
Low	MXM
High	WO/ MXM



MXM3.0	n-Vidia	AMD
LVDS	LVDS	LVDS/Int. DP
DP_D	Int. DP	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A

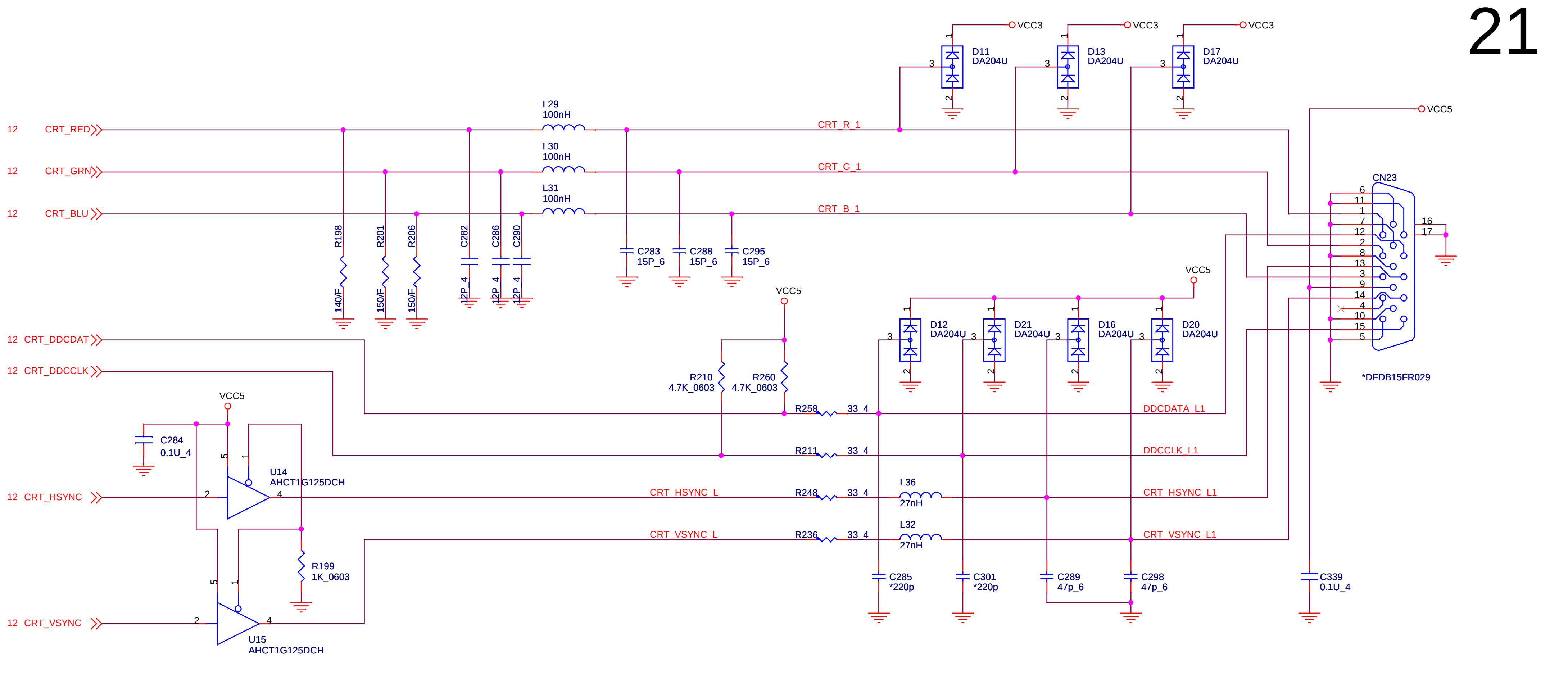
MAINON	Behavior
Low	Enable dGPU PWR
High	Disable dGPU PWR

Quanta Computer Inc.

PROJECT : ZN1

Size | Document Number: MXM3.0 | Rev: 3B

Date: Friday, May 08, 2009 | Sheet 20 of 41



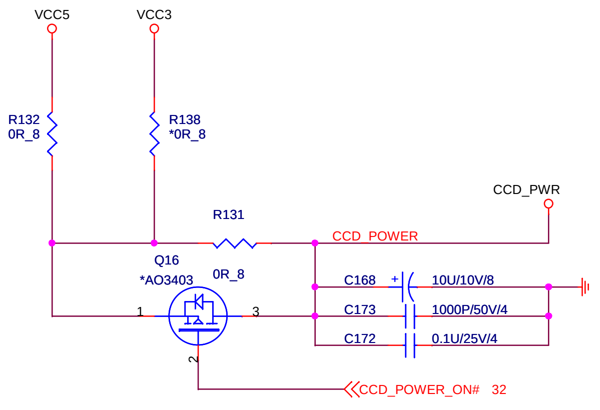
Quanta Computer Inc.

PROJECT : ZN1

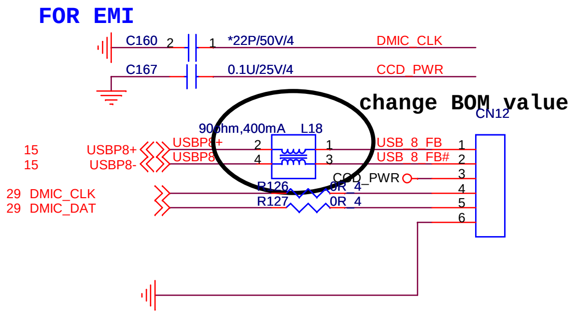
Size	Document Number	Rev
	CRT (Reserved for Debug only)	1A

Date: Friday, May 08, 2009 Sheet 21 of 41

CAMERA POWER CONTROL



TO WEB CAM MODULE

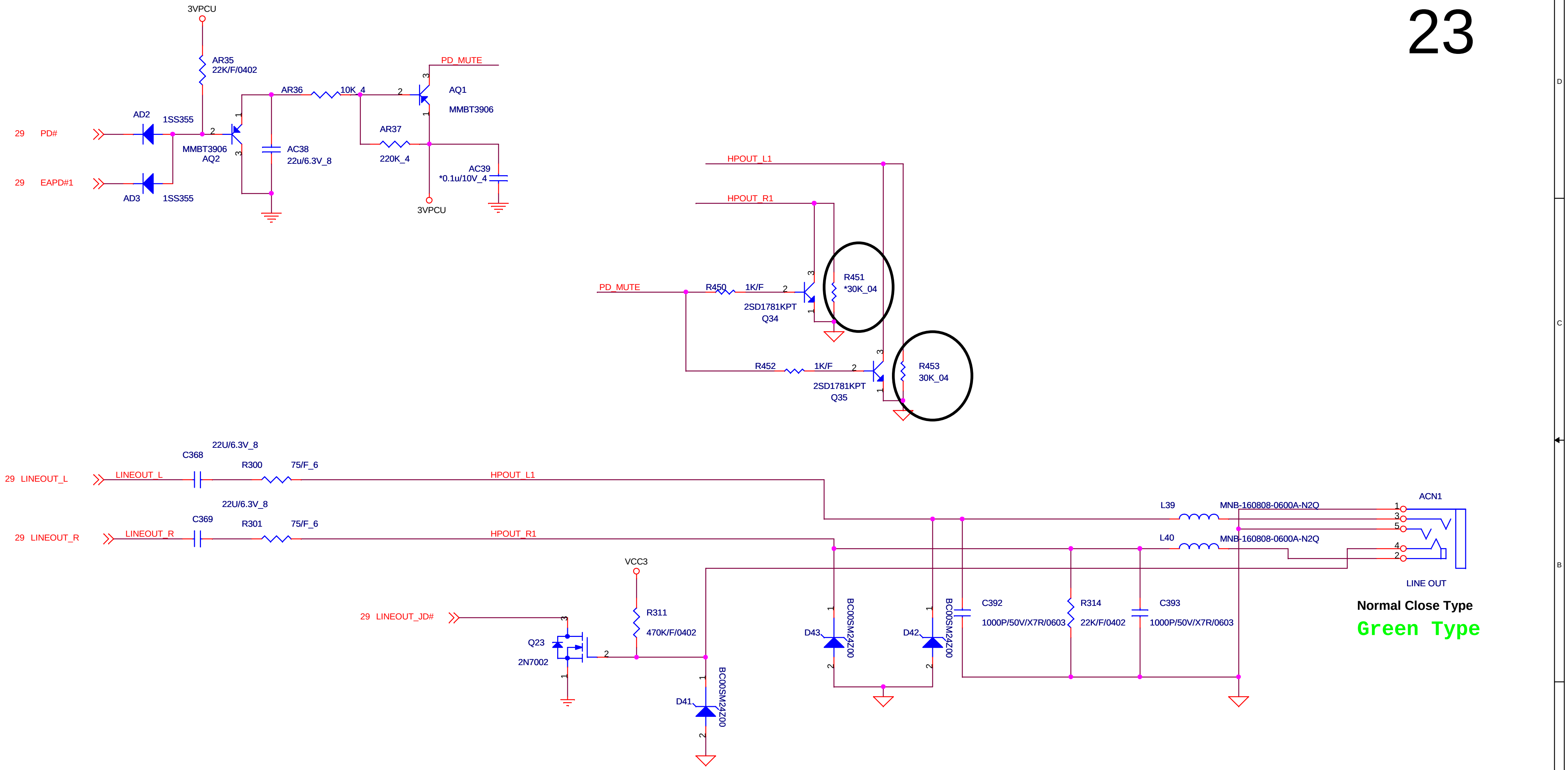


Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	WEBCAM	1A

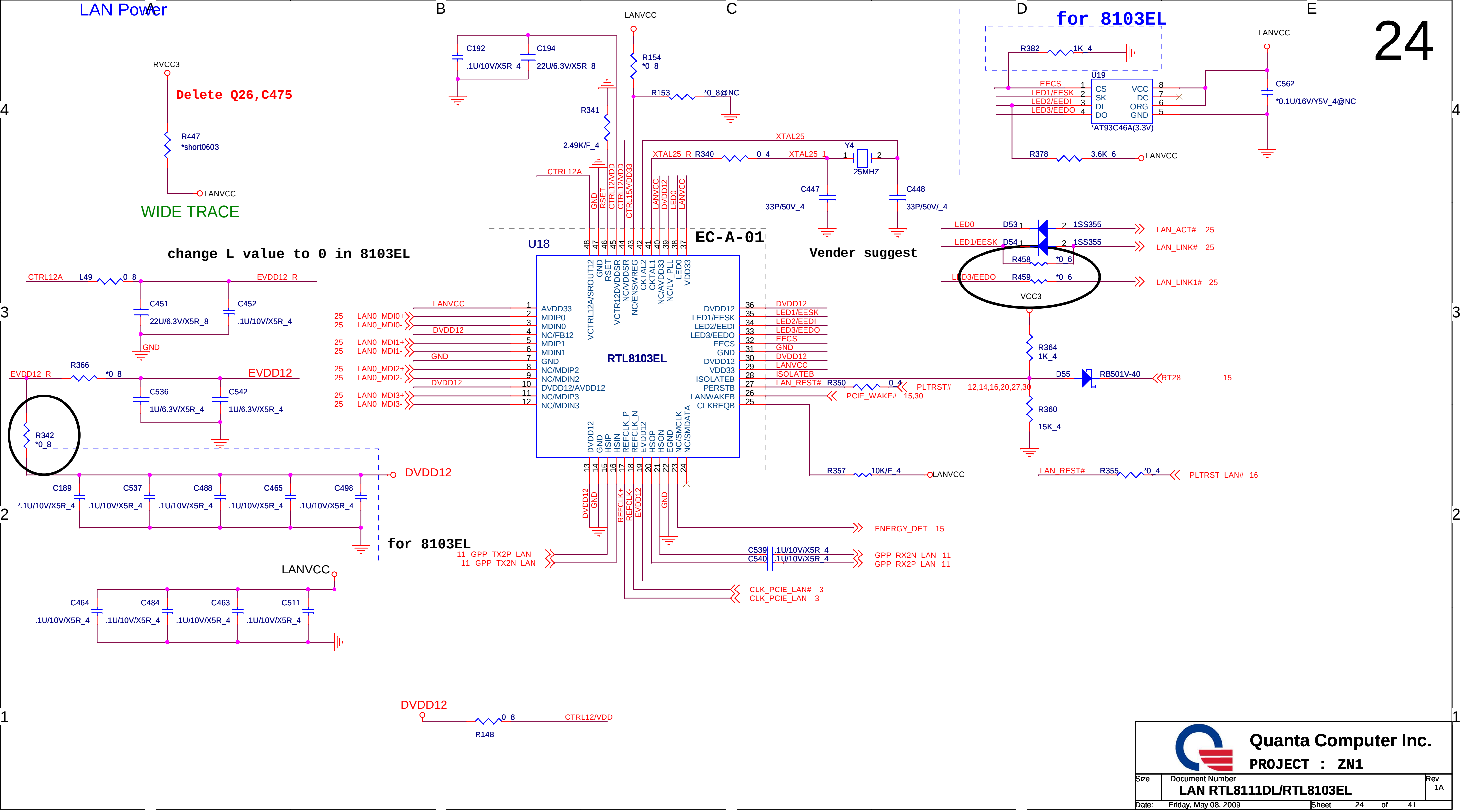
Date: Friday, May 08, 2009 Sheet 22 of 41



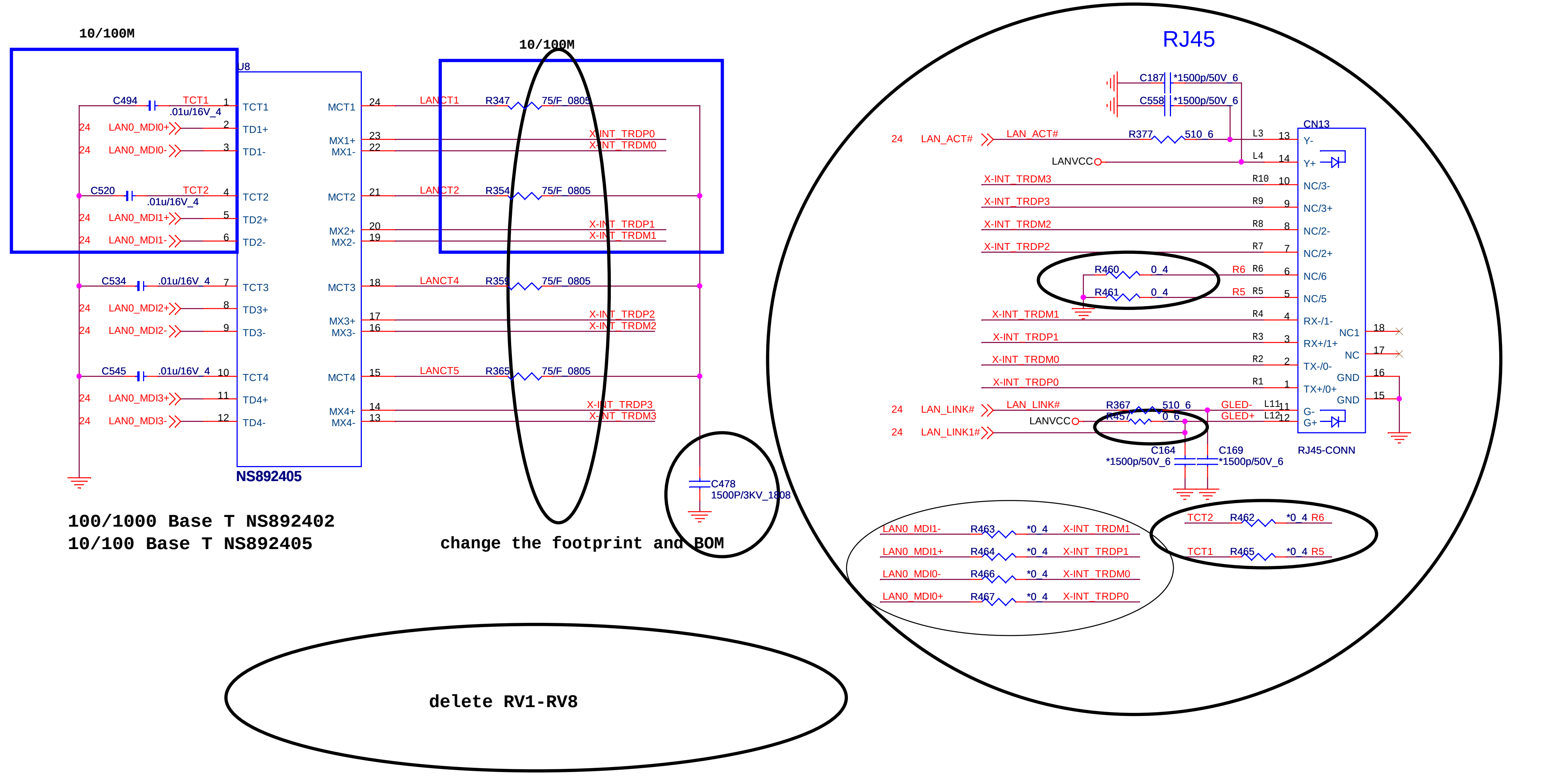
Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	Line Out	1A
Date: Friday, May 08, 2009	Sheet 23 of 41	


LAN Power
Delete Q26,C475
WIDE TRACE
change L value to 0 in 8103EL
for 8103EL
EC-A-01
Vender suggest
U18
RTL8103EL
U19
*AT93C46A(3.3V)
Y4
25MHZ
LANVCC
RVCC3
DVDD12
EVDD12
EVDD12_R
CTRL12A
CTRL12/VDD
VCC3
R447
*short0603
L49
R366
R342
R148
R154
R153
R341
R340
R350
R357
R355
R360
R364
R378
R382
R458
R459
D53
D54
D55
1SS355
RB501V-40
C192
C194
C447
C448
C451
C452
C536
C542
C189
C537
C488
C465
C498
C464
C484
C463
C511
C539
C540
C562
LAN_ACT#
LAN_LINK#
LAN_LINK1#
PLTRST#
PCIE_WAKE#
PLTRST_LAN#
ENERGY_DET
GPP_TX2P_LAN
GPP_TX2N_LAN
GPP_RX2N_LAN
GPP_RX2P_LAN
CLK_PCIE_LAN#
CLK_PCIE_LAN
RT28
24
Quanta Computer Inc.
PROJECT : ZN1
Size
Document Number
LAN RTL8111DL/RTL8103EL
Rev
1A
Date: Friday, May 08, 2009
Sheet 24 of 41

LAN Transformer & WIRE CONN to RJ45

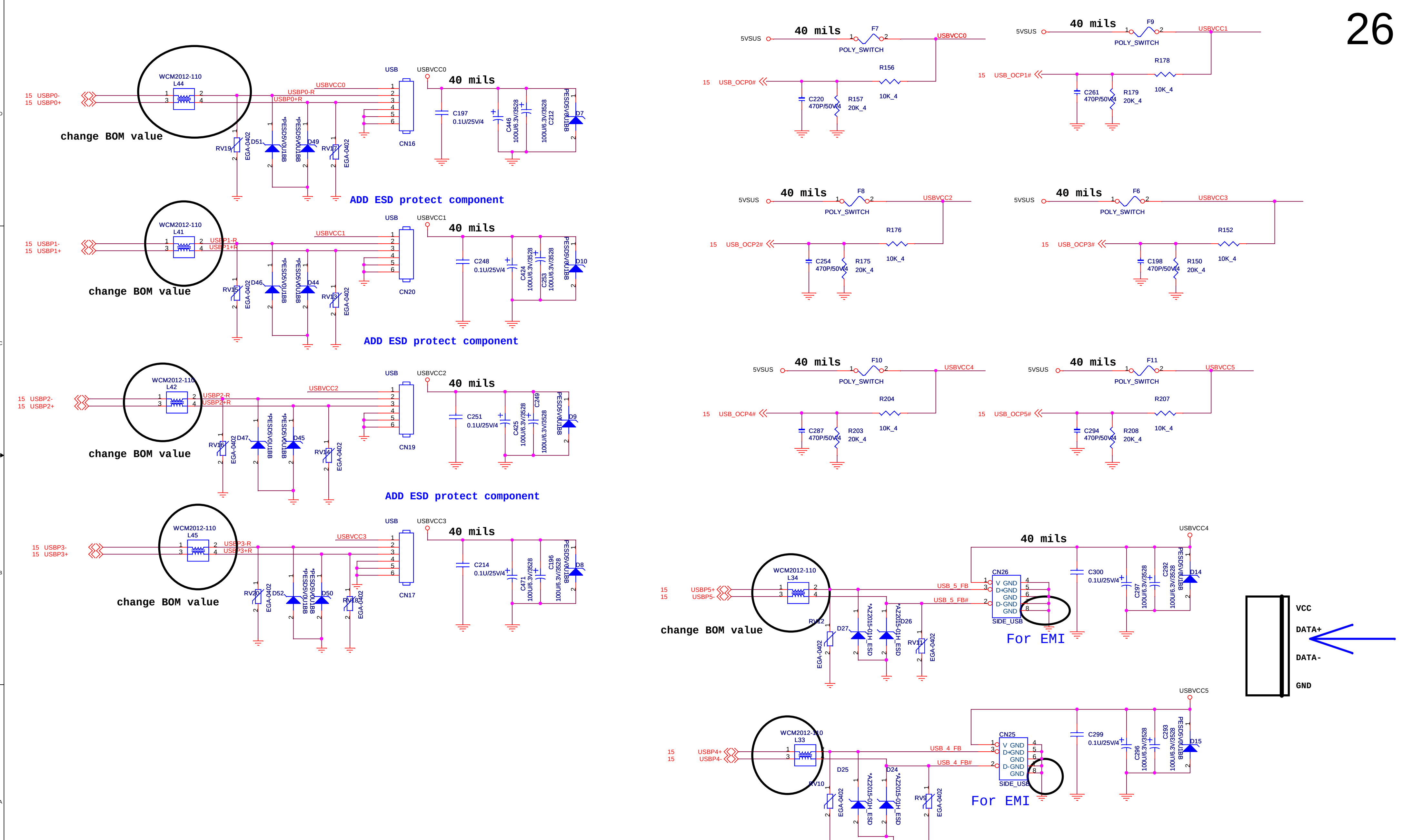


Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	LAN Transformer & RJ45	1A

Date: Friday, May 08, 2009 Sheet 25 of 41



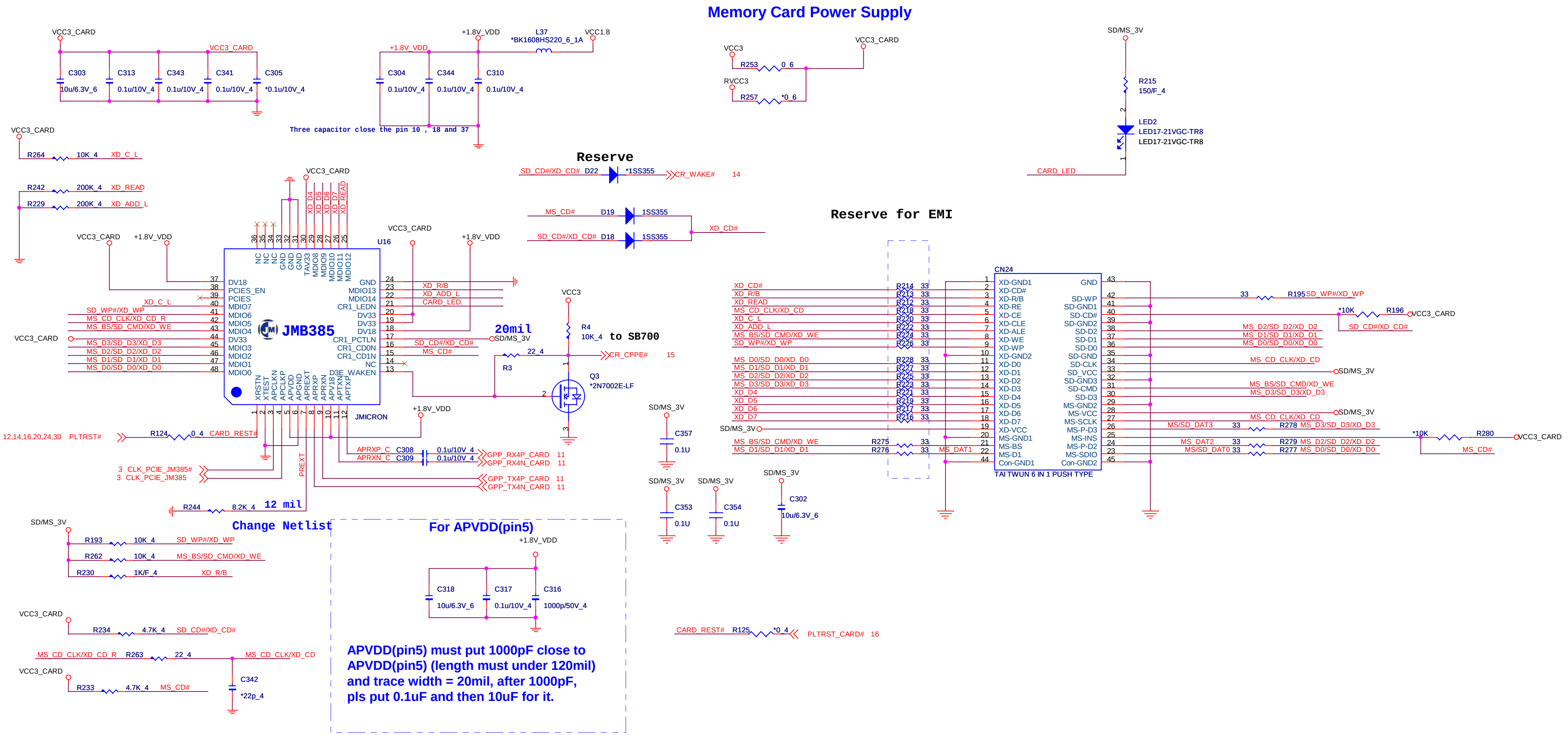
Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	USB Port X6	A

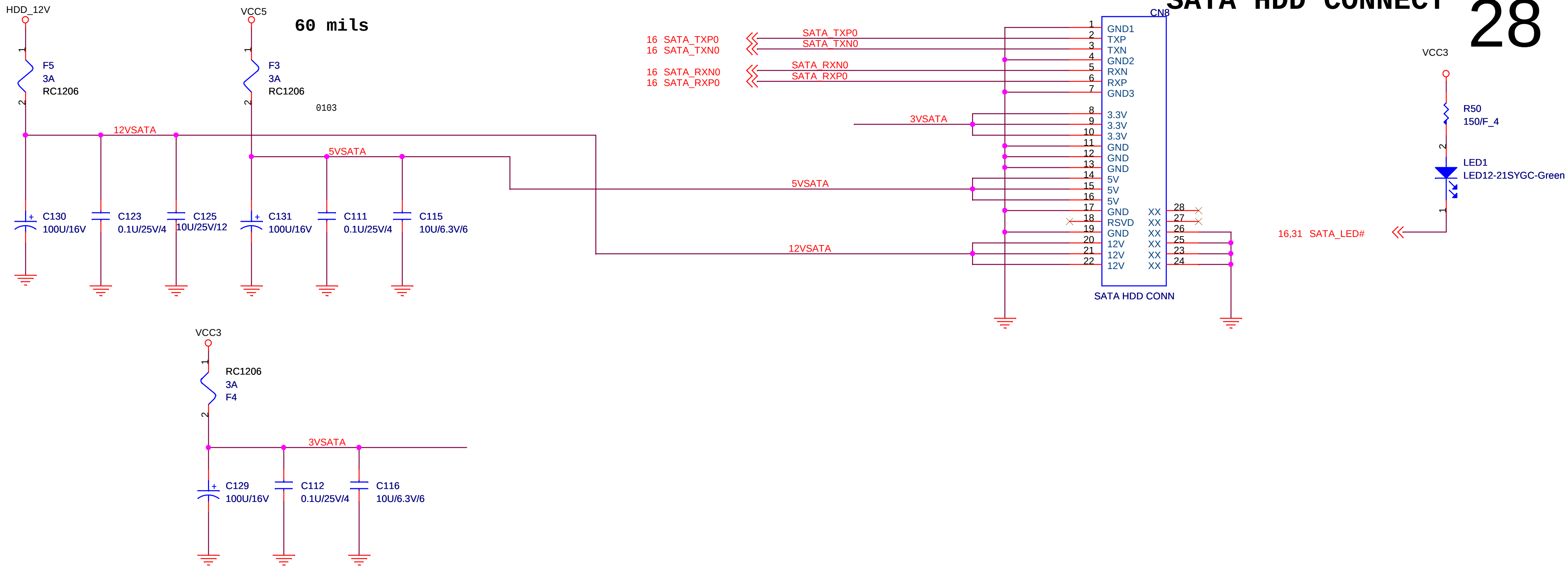
Date: Friday, May 08, 2009 | Sheet 26 of 41

Memory Card Power Supply



Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: Card Reader	Rev: 1A
Date: Friday, May 08, 2009	Sheet 27 of 41	

SATA HDD CONNECT



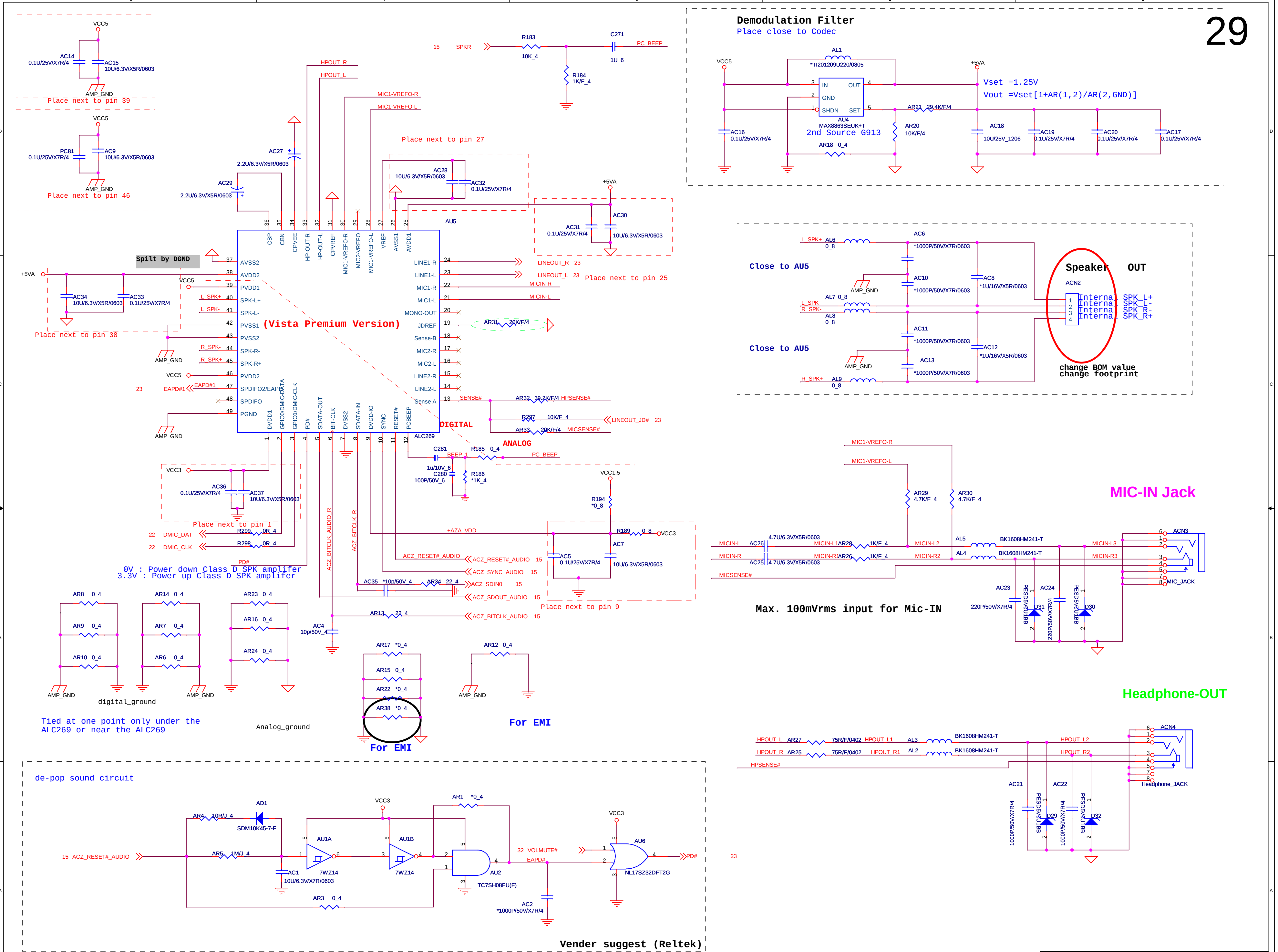
SATA ODD CONNECTOR

Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	SATA HDD/ODD	A

Date: Friday, May 08, 2009 Sheet 28 of 41



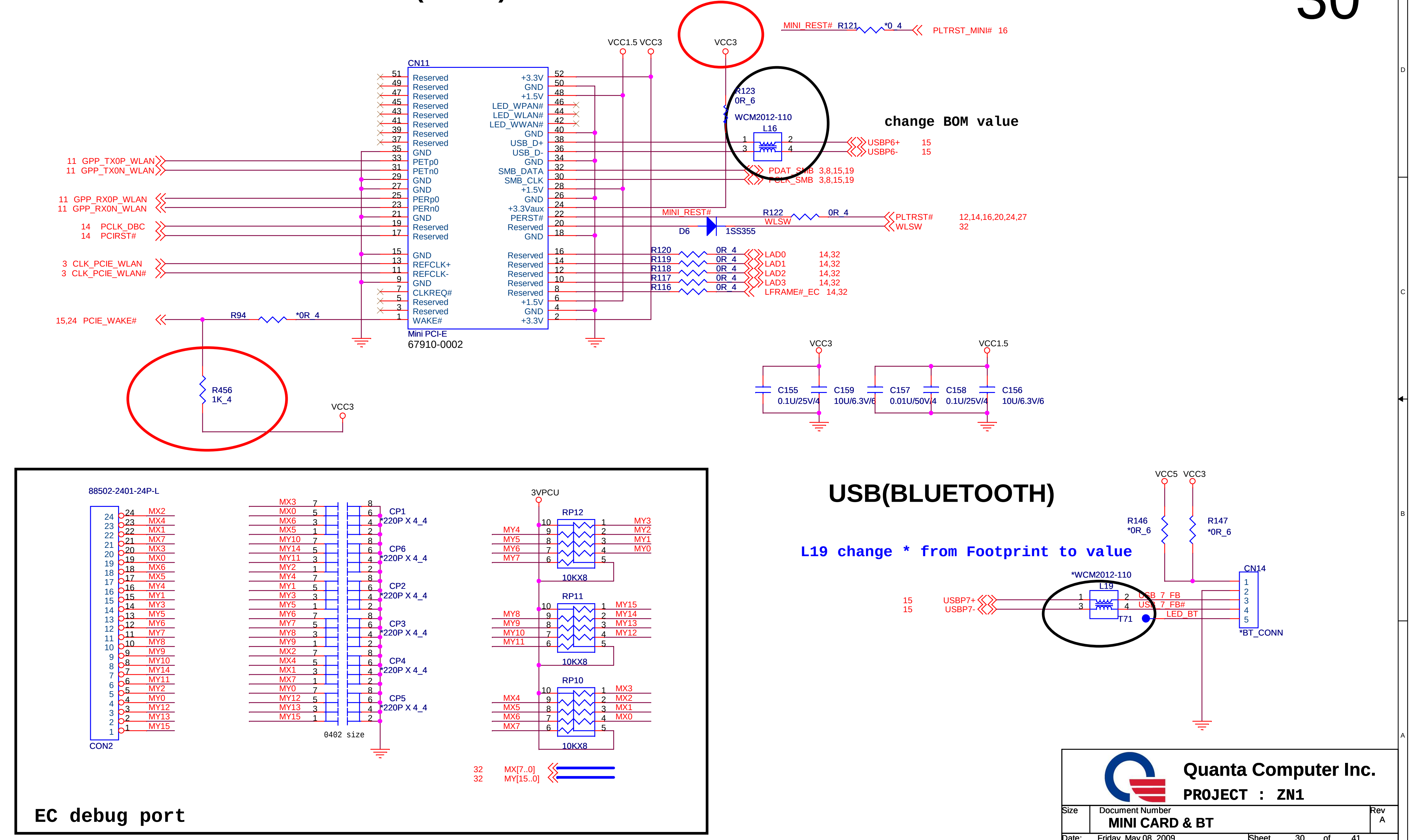
Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	Realtek ALC269	1A

Date: Friday, May 08, 2009 Sheet 29 of 41

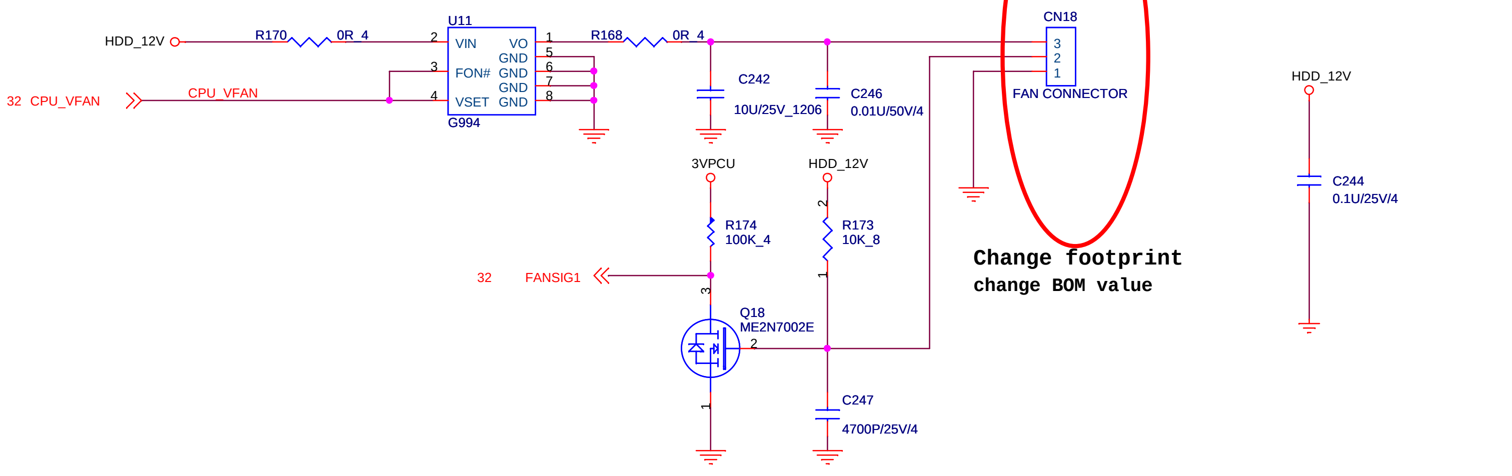
Mini Card (WLAN)



Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: MINI CARD & BT	Rev A
Date: Friday, May 08, 2009	Sheet 30 of 41	

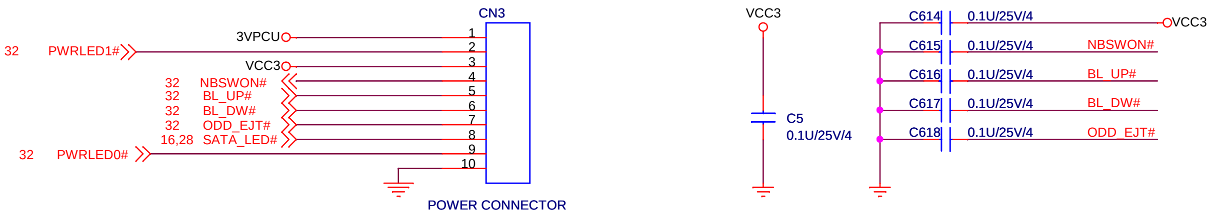
SYSTEM FAN CONN

FANPWR = 1.6*VSET



Change footprint
change BOM value

FOR EMI



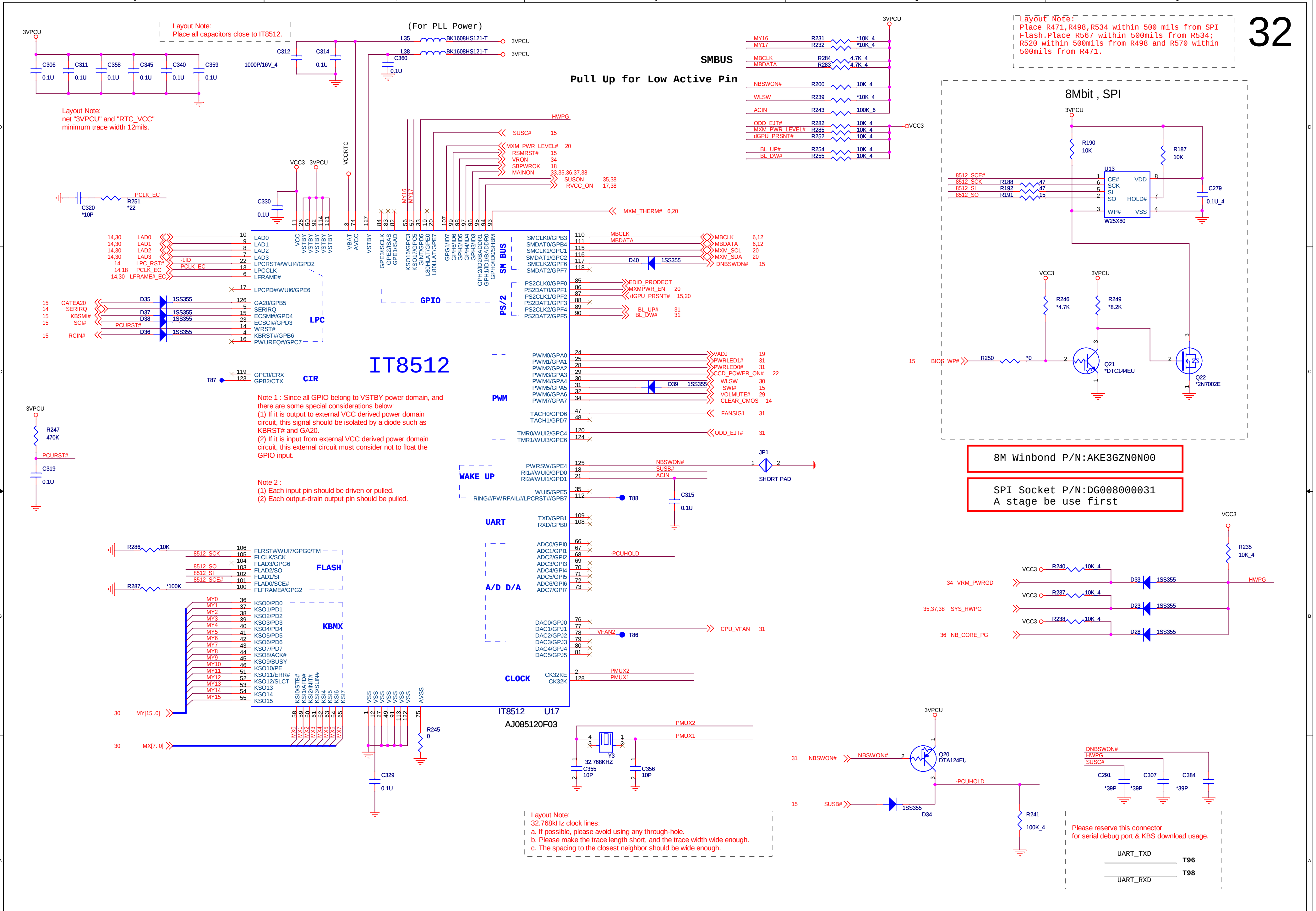
TO POWER BUTTON & LED LIGHT

Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	FAN	A

Date: Friday, May 08, 2009 | Sheet 31 of 41



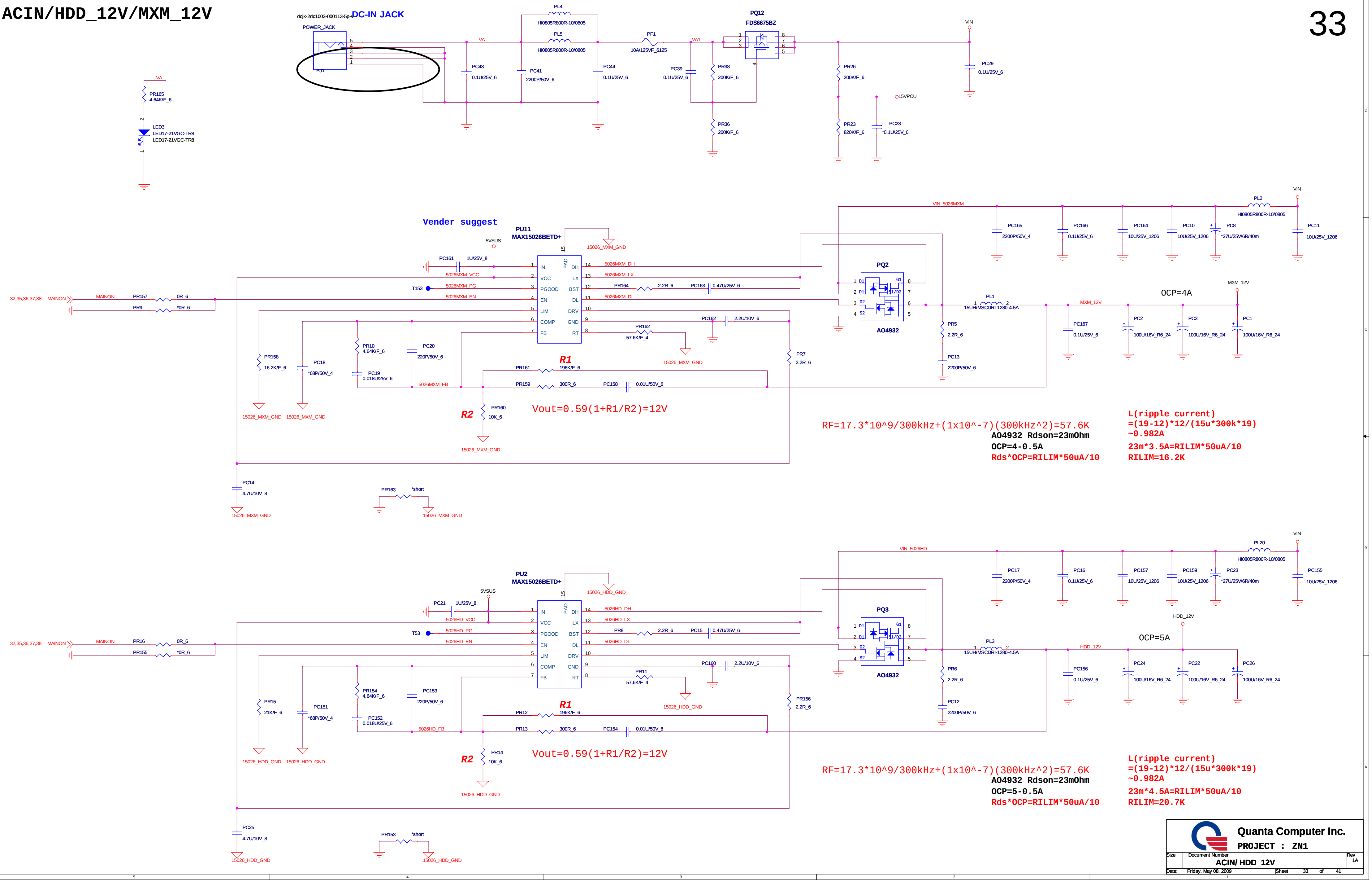
Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	EC ITE8512	1A

Date: Friday, May 08, 2009 Sheet 32 of 41

ACIN/HDD_12V/MXM_12V



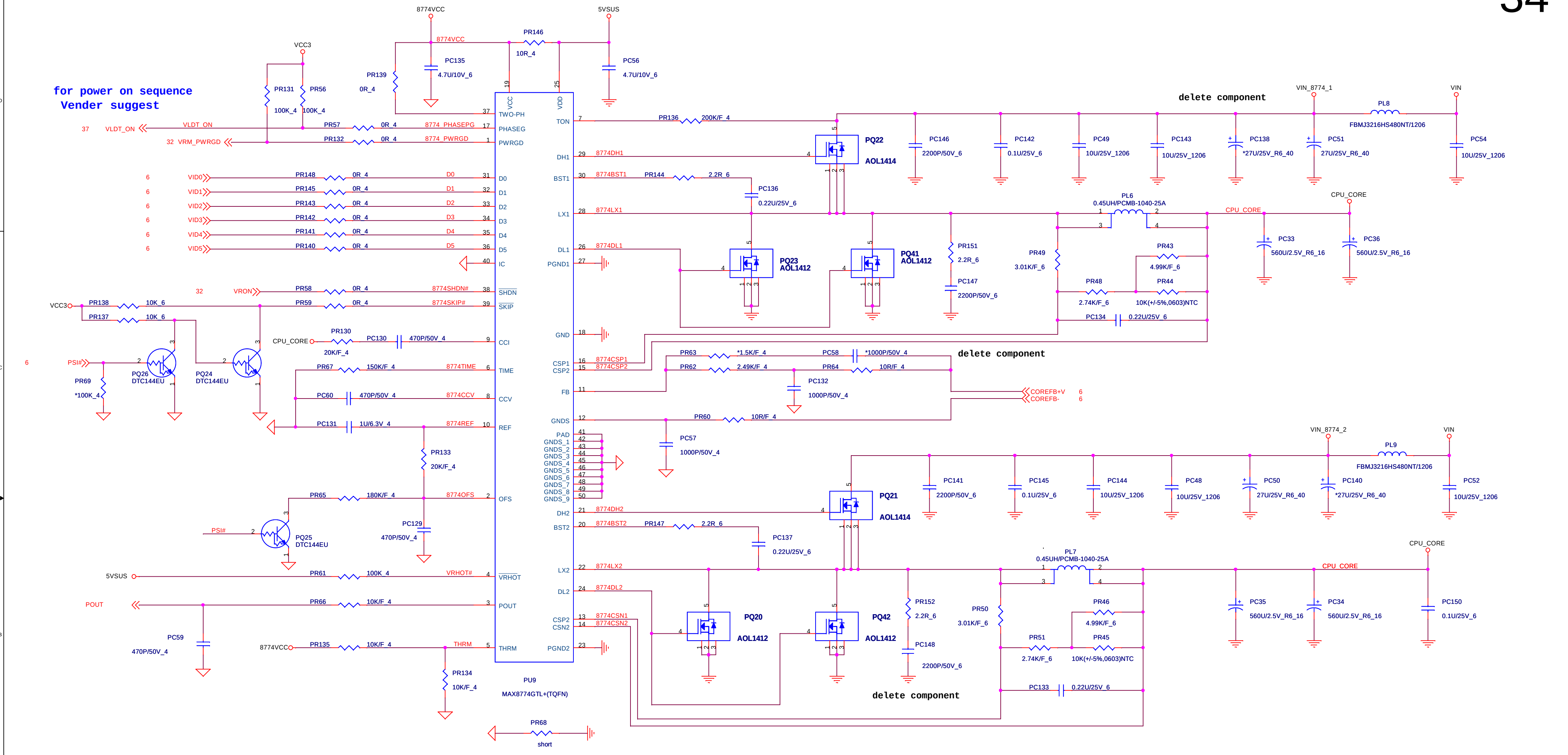
Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	ACIN/ HDD_12V	1A

Date: Friday, May 08, 2009 | Sheet 33 of 41

CPU_CORE and CPU_VDDNB_RUN



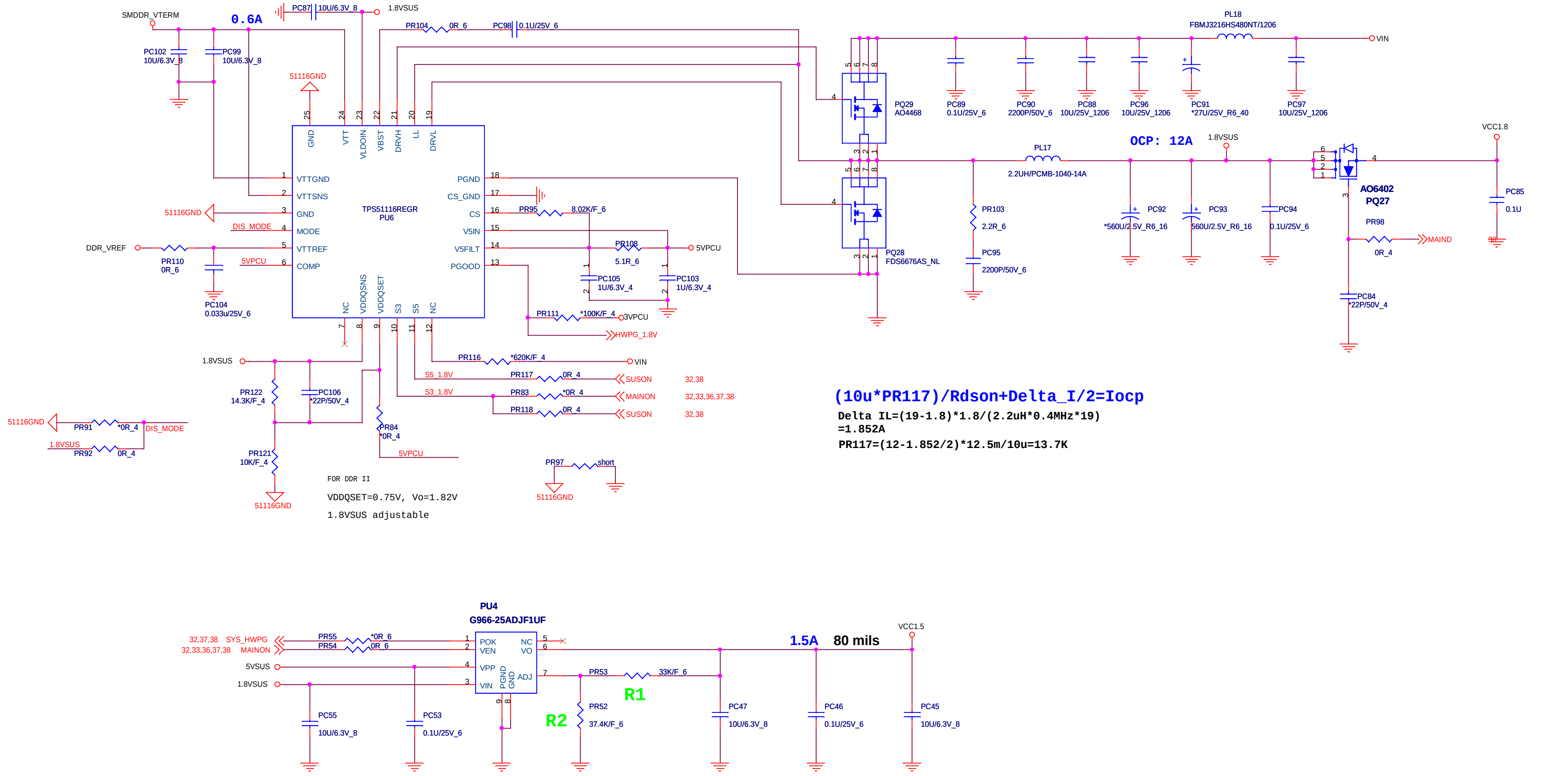
For AMD AM2 CORE

Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	CPU CORE(MAX8774)	1A

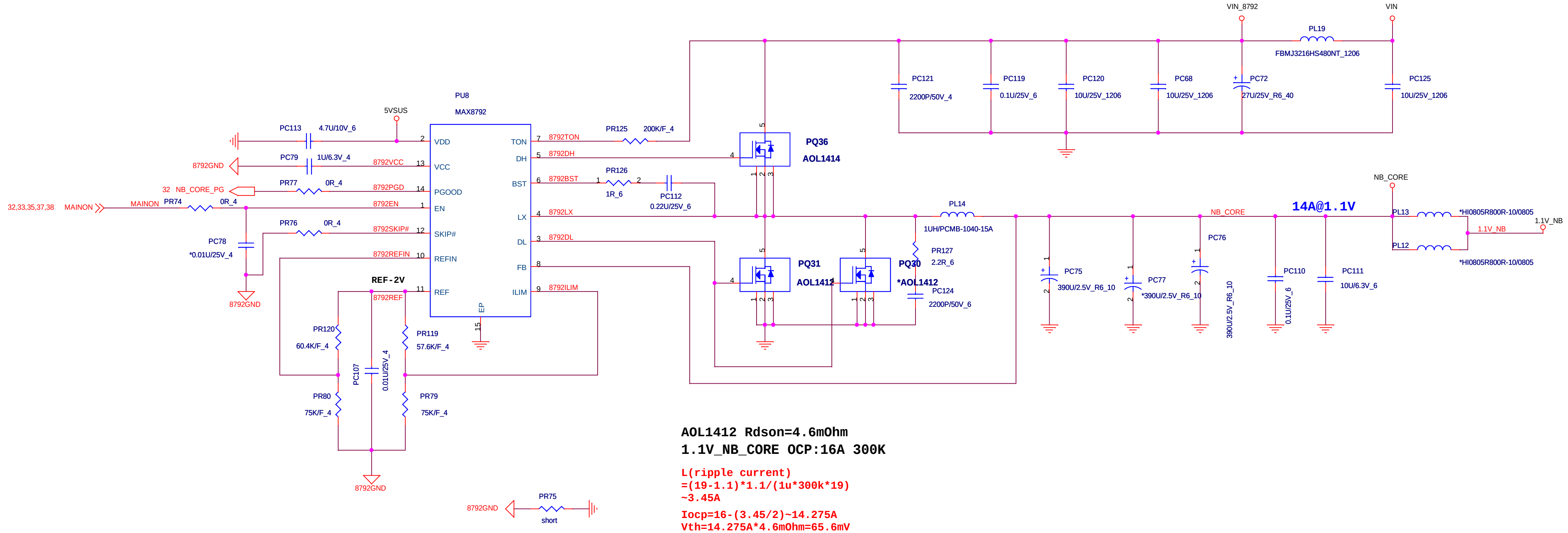
Date: Friday, May 08, 2009 Sheet 34 of 41



Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	DDR 1.8V(TPS51116&VTERM)	2B
Date: Friday, May 08, 2009	Sheet 35 of 41	



AOL1412 Rdson=4.6mOhm
1.1V_NB_CORE OCP:16A 300K

L(ripple current)
=(19-1.1)*1.1/(1u*300k*19)
~3.45A

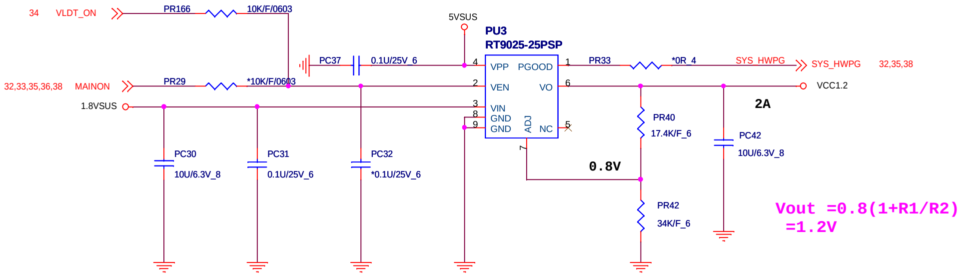
Iocp=16-(3.45/2)~14.275A
Vth=14.275A*4.6mOhm=65.6mV

VCC1.2 & VCC1.2SB

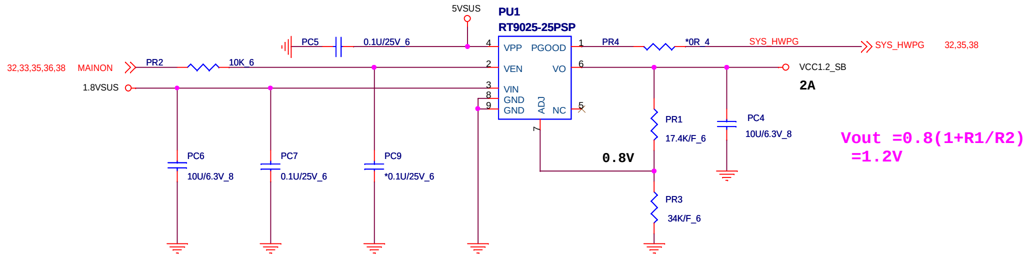
Change netlist for HT BUS power

Vender suggest

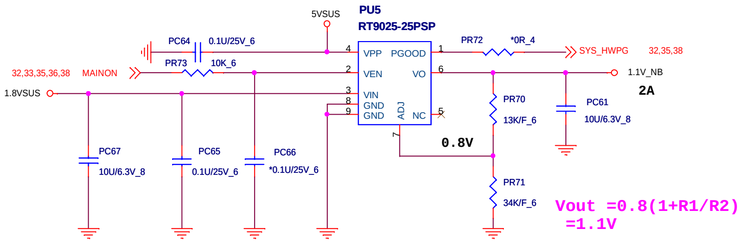
Colsed to CPU/NB



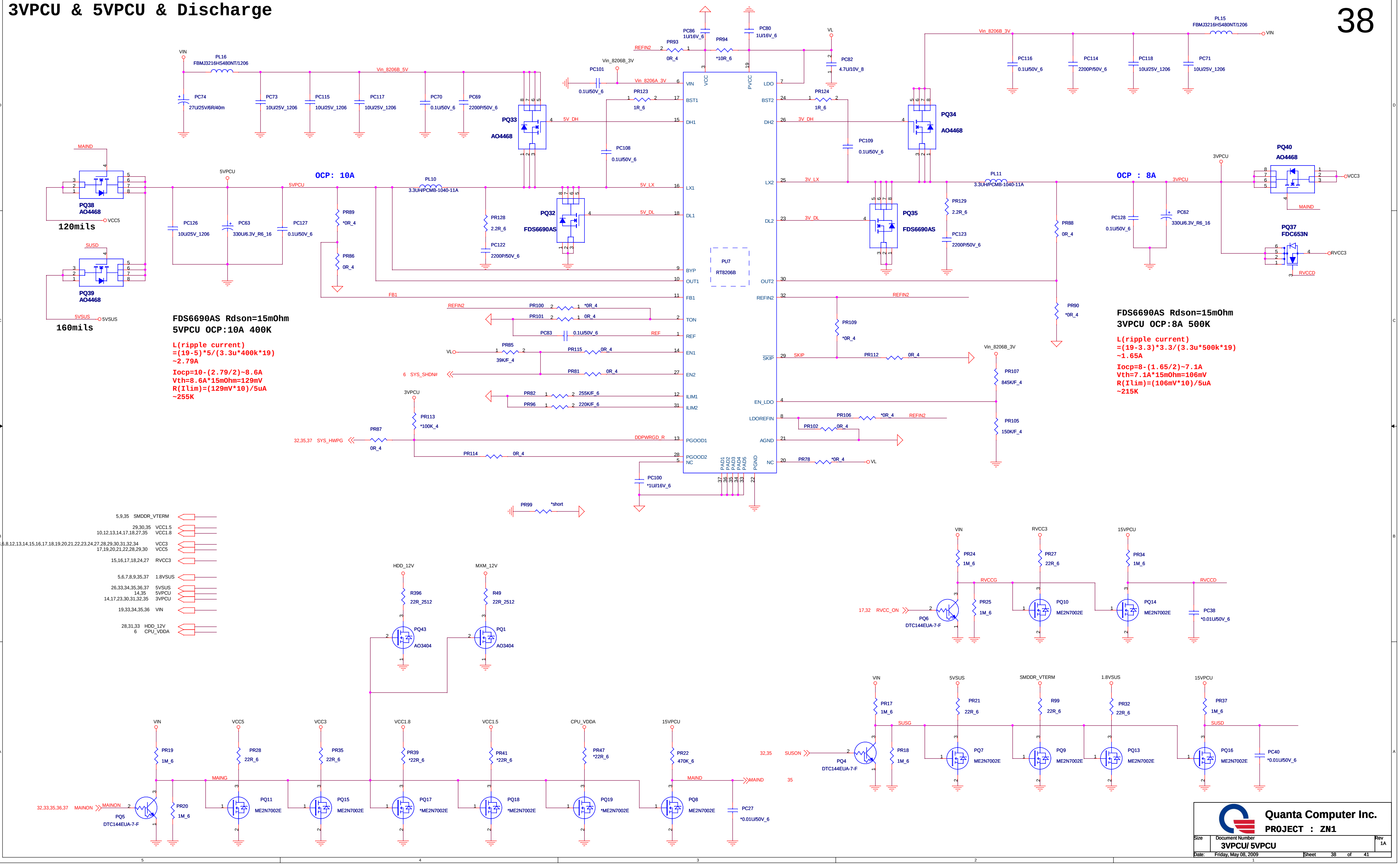
Colsed to SB

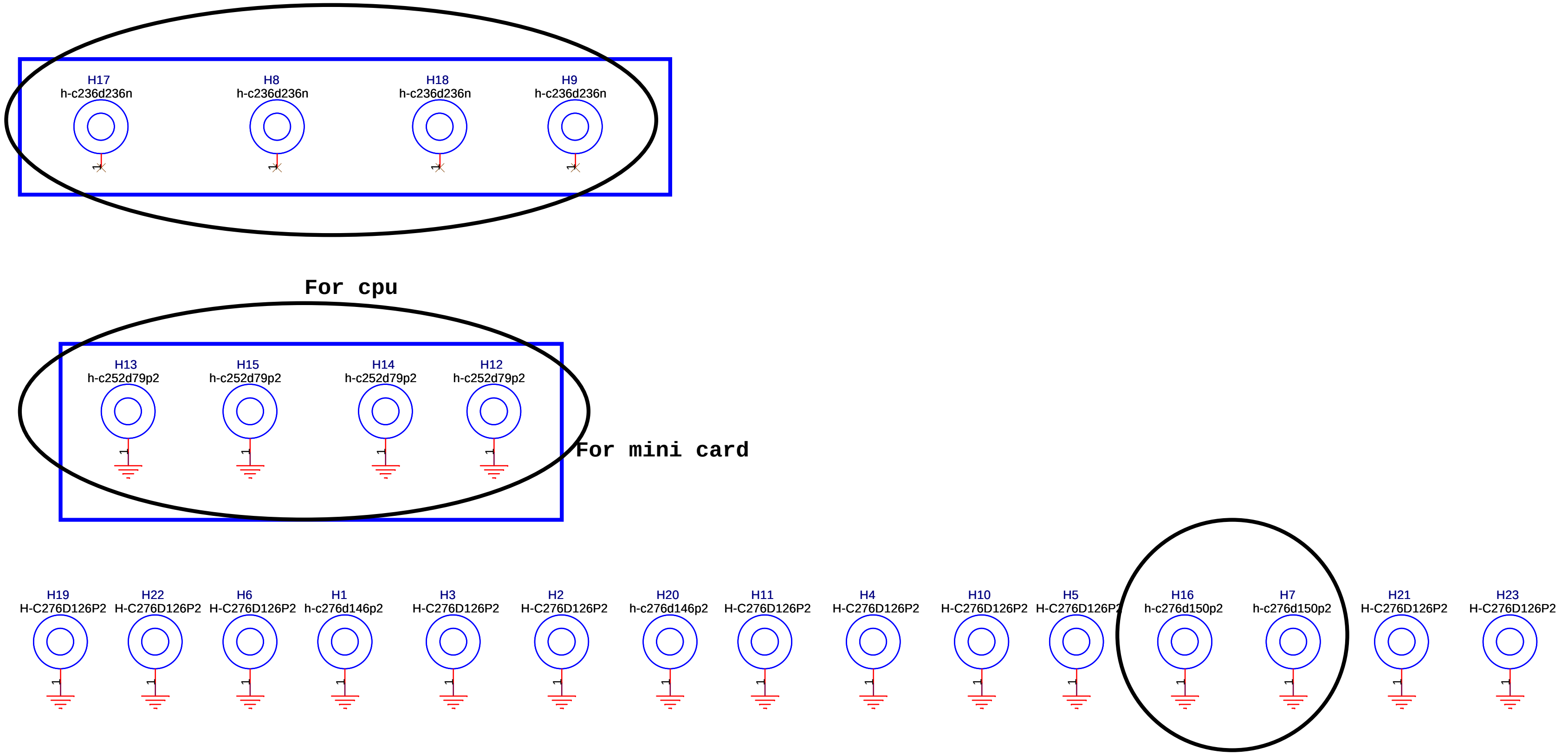


Colsed to NB



3VPCU & 5VPCU & Discharge





Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	SCREW HOLE & EMI	A
Date: Friday, May 08, 2009	Sheet 39 of 41	

DATE	Description	Note	Page
2009 **0320**	1.change RP1-RP9 to 47 ohm (AMD suggestion)----PAGE 3 2.add R448 10k to VCC3---PAGE 6 3.add R101 300ohm to 1.8VSUS---PAGE 6 4.add R449 10K ohm to VCC3---PAGE12 5.Reserve C612,C613,R441,Y6 to schmatic---page14 6.add D59 and R446 10k to VCC3---page14 7.add R455,C621,C622 to schmatic for EMI---page14 8.add write EDID rom net to control ---page15 9.delete R403 and R32 --page 15 10.change C91,c95 value to 33p---page 16 11.Add 2 short pin for clear cmos and clear password --page16 12.add R86 10k--page 18 13.delete D4,D5 ,C68 component and add R69 0ohm---page18 14.change netlist to SB control (write_edid _rom)and add R62 2.2k ohm--- page19 15.change Q8 control pin to main pin---page 20 16.change MXM reset from pltrst.---page20 17.add ine out mute function---page23 add component ar35,ar36,ar37,ac38,aq1,aq2,ad2,ad3,q34,q35,r450,r452--page23 18.delete Q26,c475 and change LANVCC net to RVCC3 to control ---page24 19.change C447,C448 to 33p---page 24 20.change CN13 footprint for LED pin change---page 25 21.add ESD protect RV17,RV19,RV13,RV15,RV14,RV16, RV18,RV20,RV9,RV10,RV11,RV12---PAGE 26 22.Change CN25,CN26 footprint for ME---page26 23.add D18,D19 for XD detect and change net SD_WP#/XD_WP for SD write protect ---page27 24.change LED2 to Green type---page 27 25.change CN8 to rightangle and change odd connect to vertical type for ME---page 28 26.change au6 to OR-gate from AND-gate for pop sound---page 29 27.change fan control net from Vender suggestion.---page 31 28.add c614--618 0.1u for EMI--- page 31 29.add pr165 ,led3 for power line in ---page33 30.change VLDT_ON net for power on sequence--PAGE 34 31.change pr137,pr138 type to BOM---page 34	**B2B**	
	33.LED RT value need to change		

DATE	ZN1 Board file	ZN1 Schematic
11th Mar. 2009	ZN1-0311-17-152.brd	AH1_A_FEB23_01.DSN
31th Mar. 2009	ZN1-0325-1830.brd	ZN1_B_HP_MAR31.DSN

Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	CHANGE LIST	C

Date: Friday, May 08, 2009 Sheet 41 of 41