UMA & Optimus Schematics Document

IVY Bridge(rPGA989)

Intel PCH(Panther Point)

DY :NotInstalled
UMA:UMA platform installed
OPS:Optimus
HR:Huron River
CR:Chief River
V: V-Series installed

<Core Design>

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Title	**Cover Page**		
Size A4	Document Number **LA480**		Rev SD
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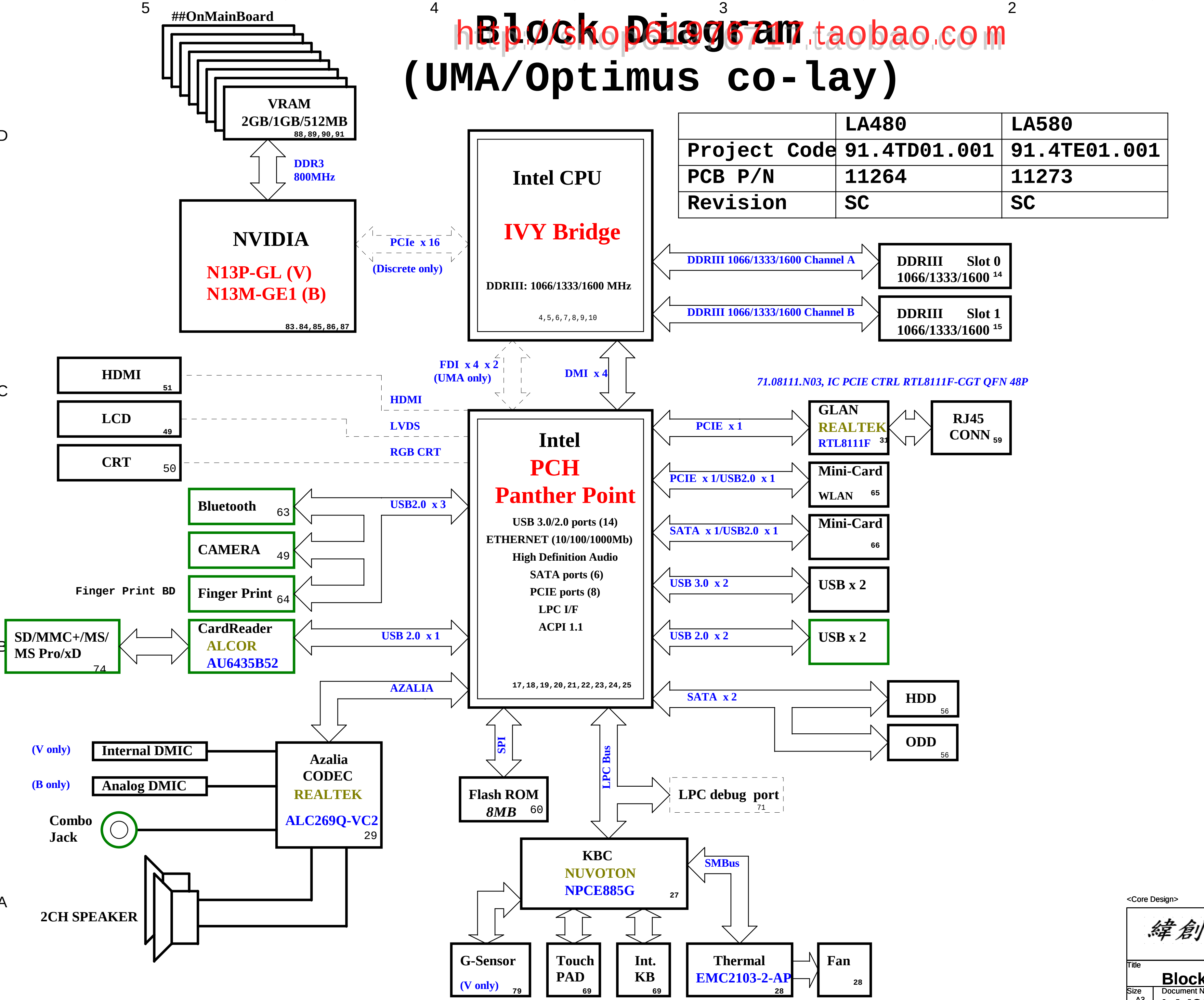
Block Diagram
(UMA/Optimus co-lay)

	LA480	LA580
Project Code	91.4TD01.001	91.4TE01.001
PCB P/N	11264	11273
Revision	SC	SC



CPU DC/DC TPS51640 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51219 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51225 41	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207M 46	
INPUTS	OUTPUTS
DCBATOUT	0D75V_S0 1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC TPS51640 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA TPS51728 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24737 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC RT8068A 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO RT8207 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

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Title		
Block Diagram		
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PCH Strapping
Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIe Routing

LANE1	X
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	Intel GBE LAN / LAN
LANE7	X
LANE8	Express Card

USB Table
port9 is debug port

Pair	Device
0	USB3.0 ext port 1
1	USB3.0 ext port 2
2	USB3.0 ext port 3
3	USB3.0 ext port 4
4	BLUETOOTH (USB1.1)
5	Fingerprint (USB1.1)
6	X
7	X
8	Mini Card2 (WWAN)
9	USB ext. port 4 / E-SATA /USB CHARGER
10	CARD READER
11	Mini Card1 (WLAN)
12	CCD
13	New Card

Processor Strapping
Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1D0V_S0 VCCSA 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

SATA Table

Pair	SATA Device
0	HDD1
1	mSATA
2	N/A
3	N/A
4	ODD
5	ESATA

SMBus ADDRESSES

I²C / SMBus Addresses Device	Ref Des	Chief River CRV Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

SSID = CPU

01.00IVY.000 IVY BRIDGE ORCAD SYMBOL.

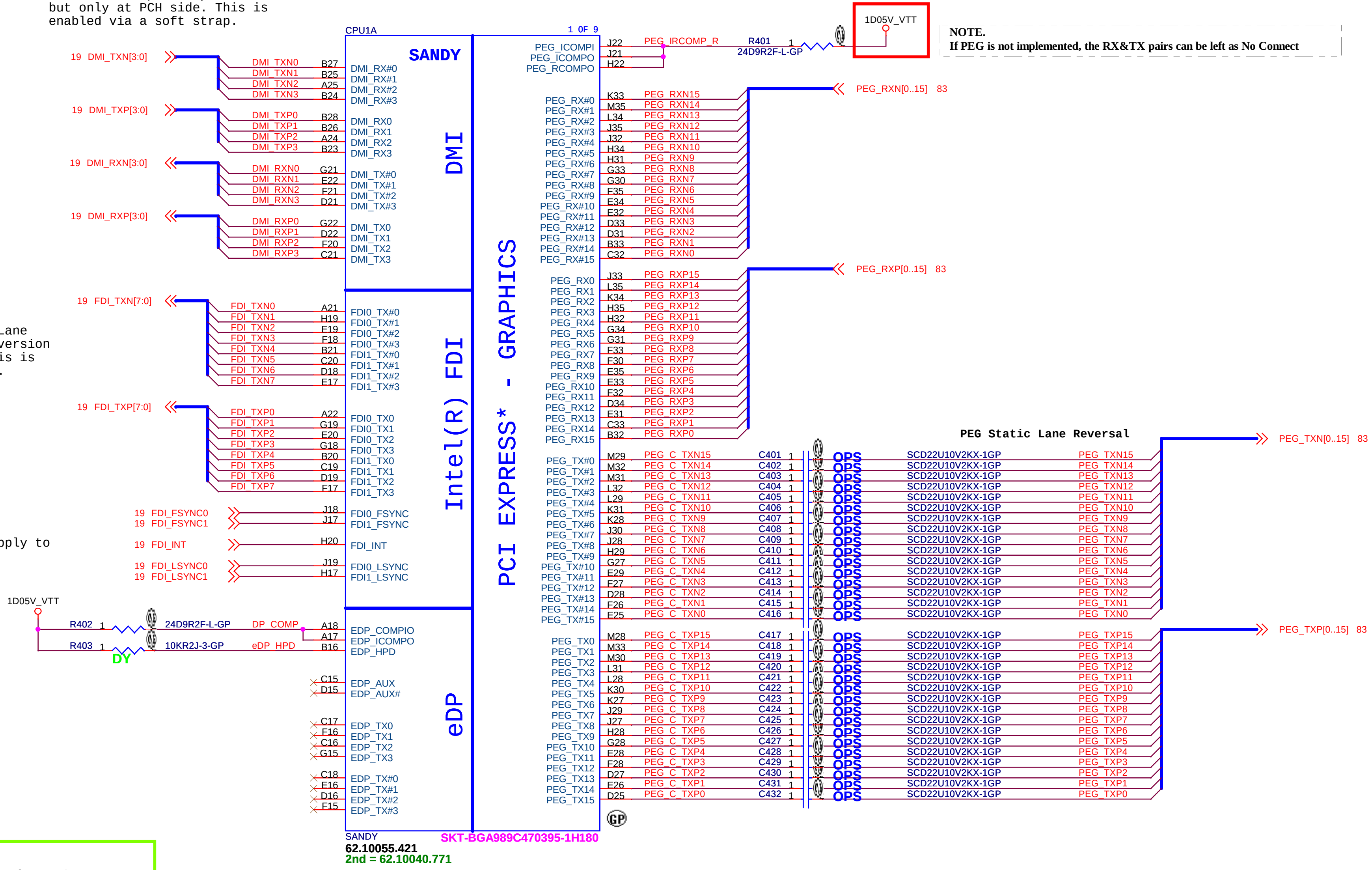
Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.



NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

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Title	CPU (PCIE/DMI/FDI)	
Size A3	Document Number LA480	Rev SD
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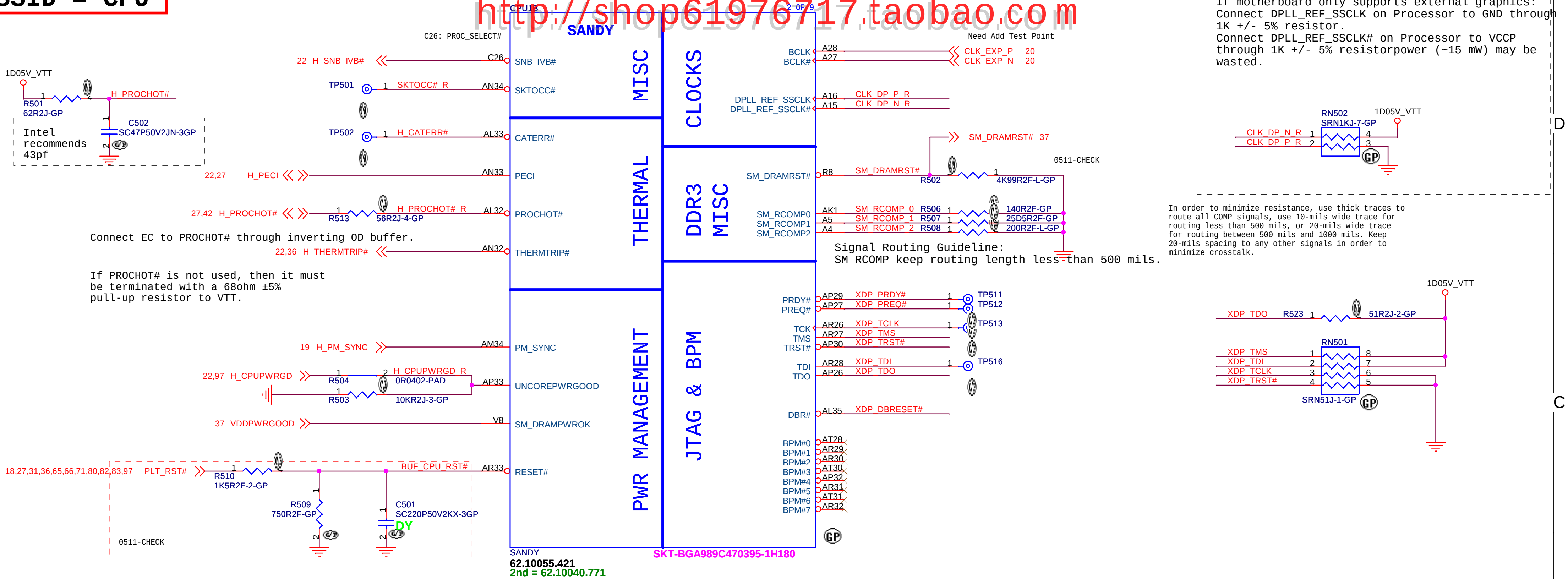
SSID = CPU



Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

Connect EC to PROCHOT# through inverting OD buffer.

If PROCHOT# is not used, then it must be terminated with a 68ohm ±5% pull-up resistor to VTT.

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

In order to minimize resistance, use thick traces to route all COMP signals, use 10-mils wide trace for routing less than 500 mils, or 20-mils wide trace for routing between 500 mils and 1000 mils. Keep 20-mils spacing to any other signals in order to minimize crosstalk.

DEL U501
DEL R519
DEL C503
DEL R517
DEL R515

ASM R510
ASM R509

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Title	CPU (THERMAL/CLOCK/PM)	
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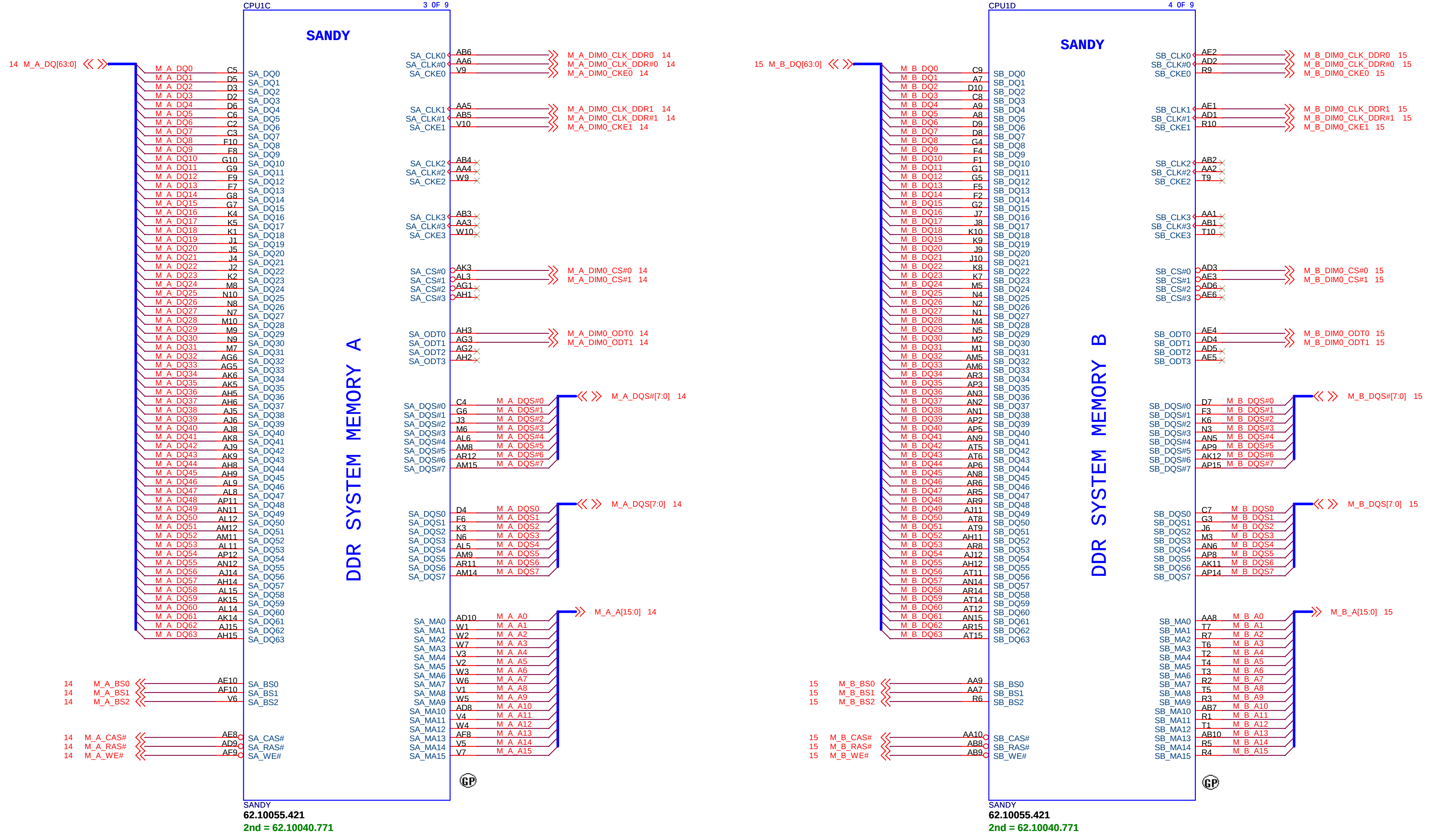
SSID = CPU



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Title	CPU (DDR)	
Size A3	Document Number LA480	Rev SD
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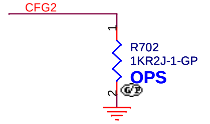
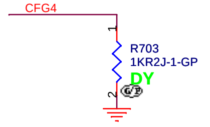
SSID = CPU



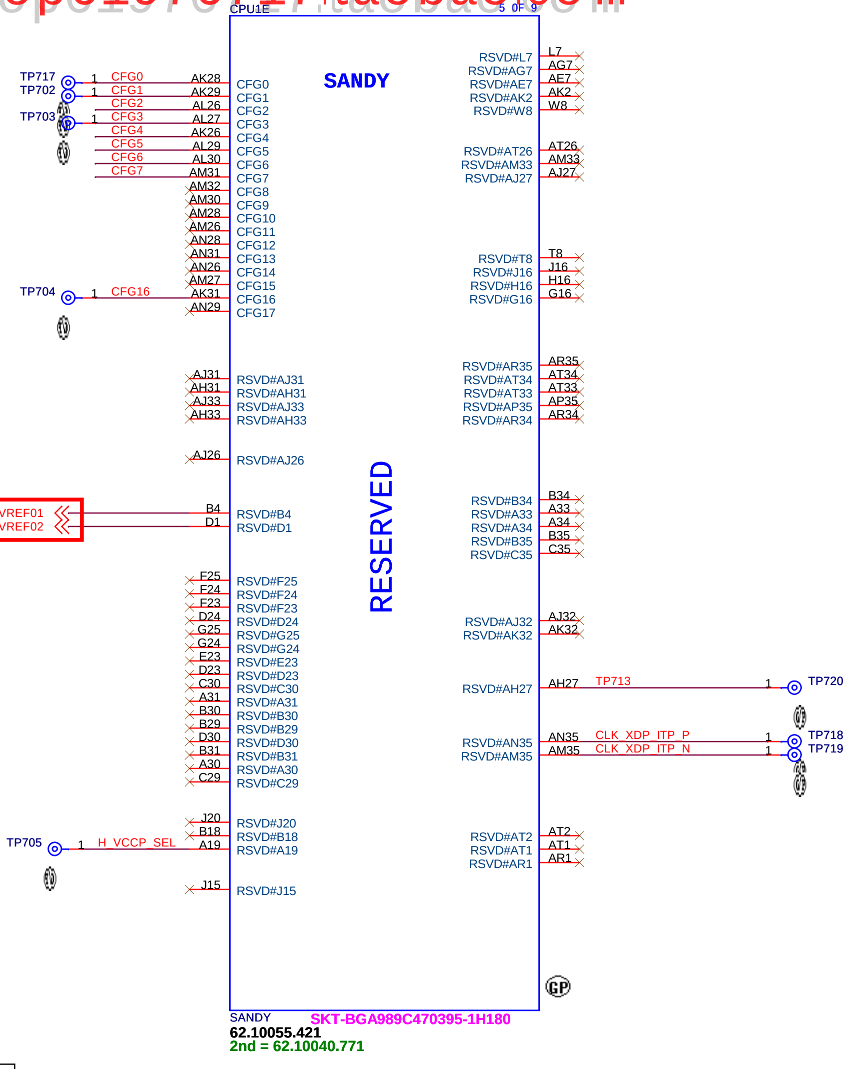
PEG Static Lane Reversal - CFG2 is for the 16x

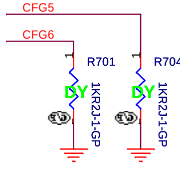
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap

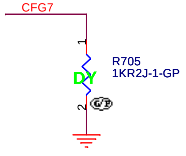
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port





PCIE Port Bifurcation Straps

CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING

CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title		
	CPU (RESERVED)	
Size A3	Document Number LA480	Rev SD
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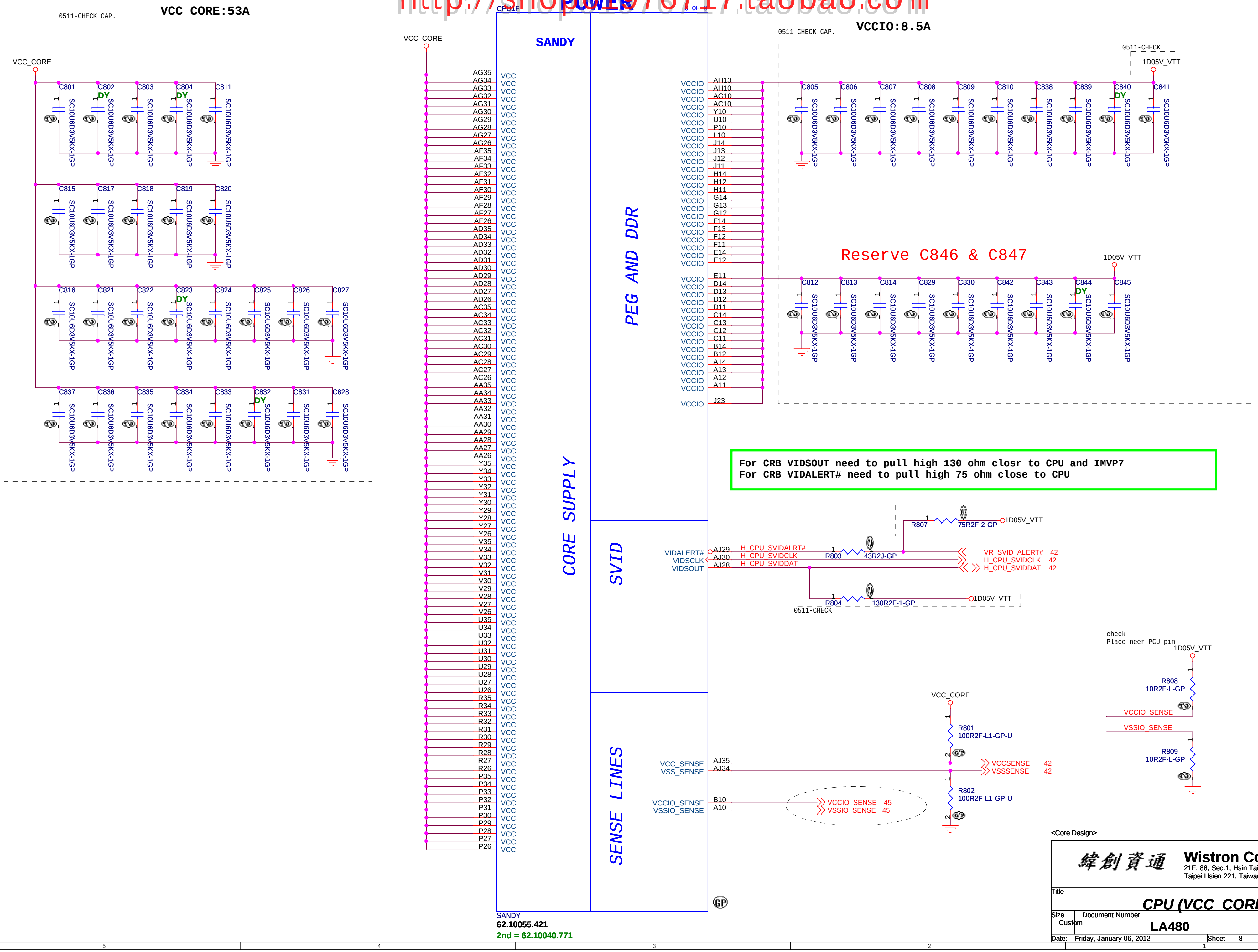
POWER



For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

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Title	CPU (VCC_CORE)	
Size: Custom	Document Number: LA480	Rev: SD
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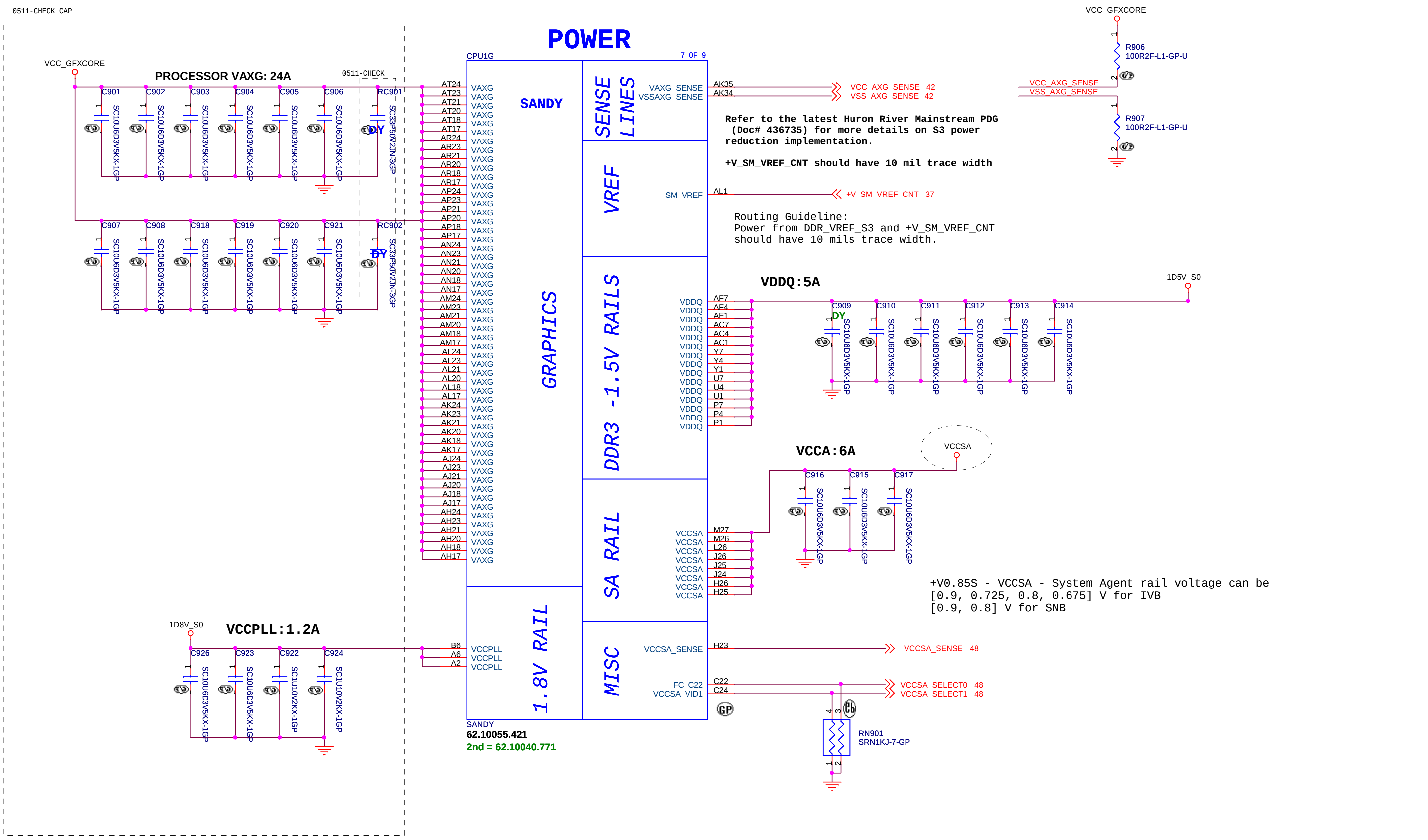
POWER



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Title	*CPU (VCC_GFXCORE)*
Size: A3	Document Number: LA480 — Rev: SD
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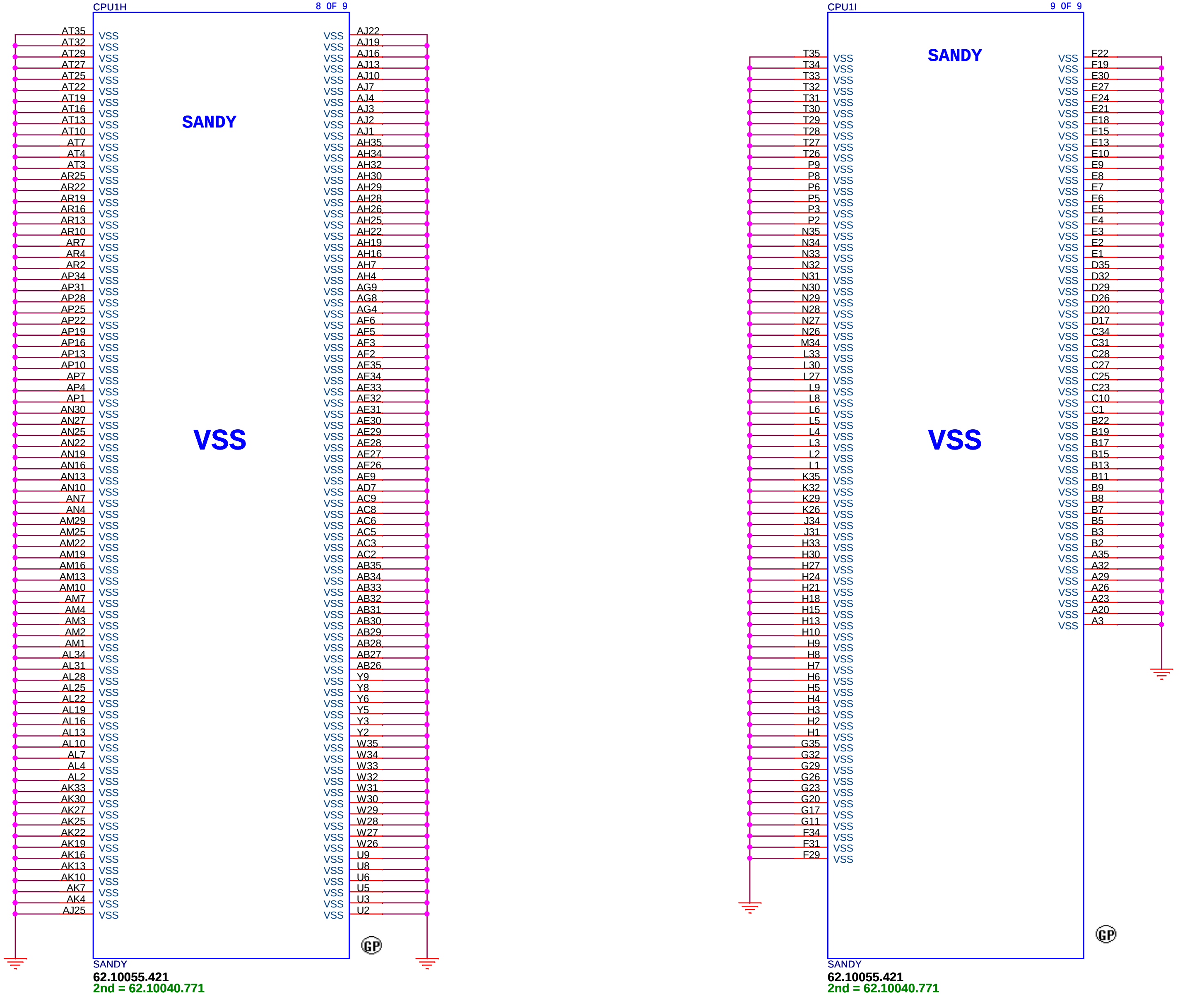
SSID = CPU



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Title: ***CPU (VSS)***

Size	Document Number	Rev
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5 4 3 2 1

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Title <Title>		
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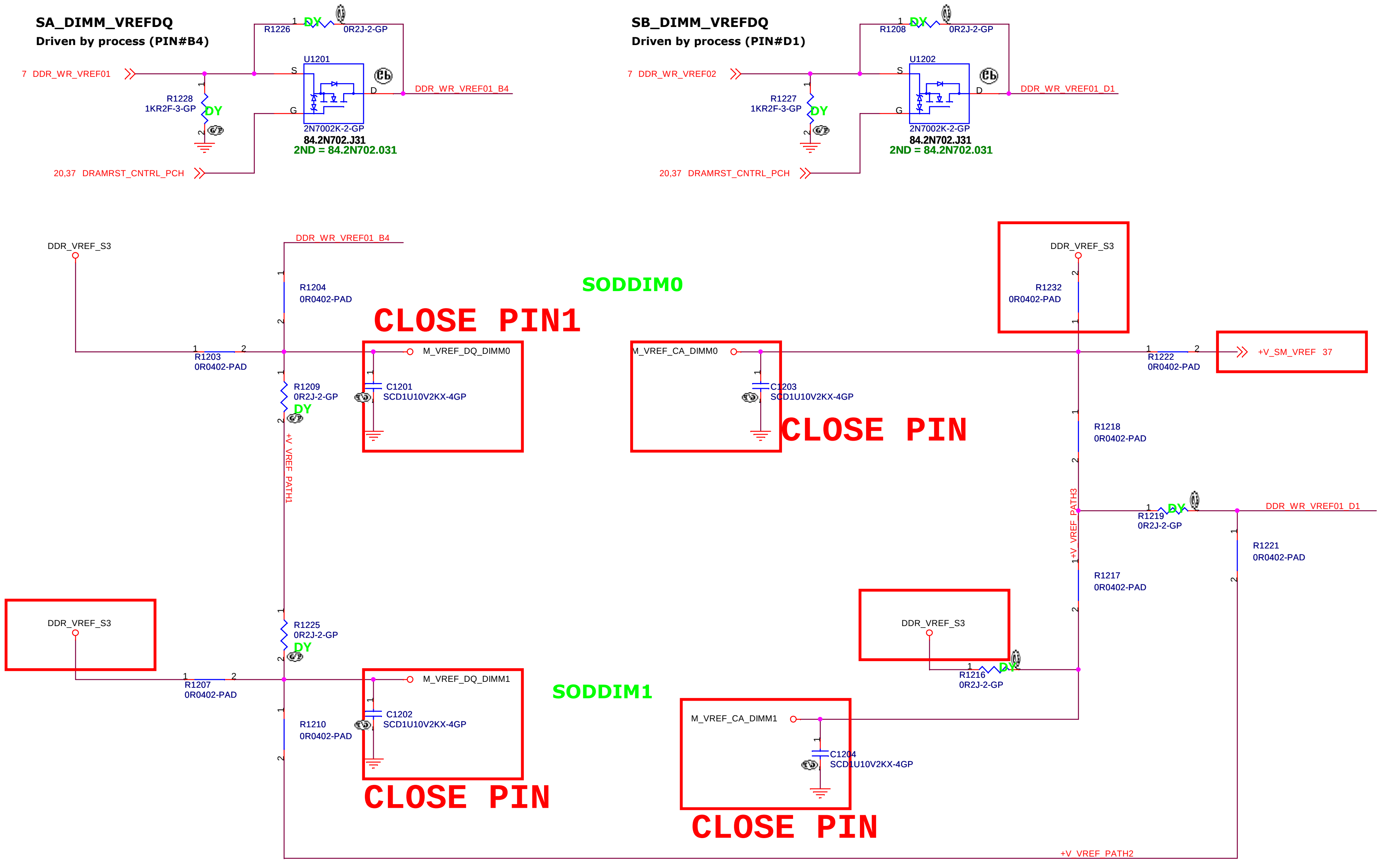
VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

CAD Note: All VREF traces should have 20:20 mil trace geometry. Note that while 20 mil trace width is optimal, short violations is acceptable if required due to tight routing constraints.



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Title	M3		
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5 4 3 2 1

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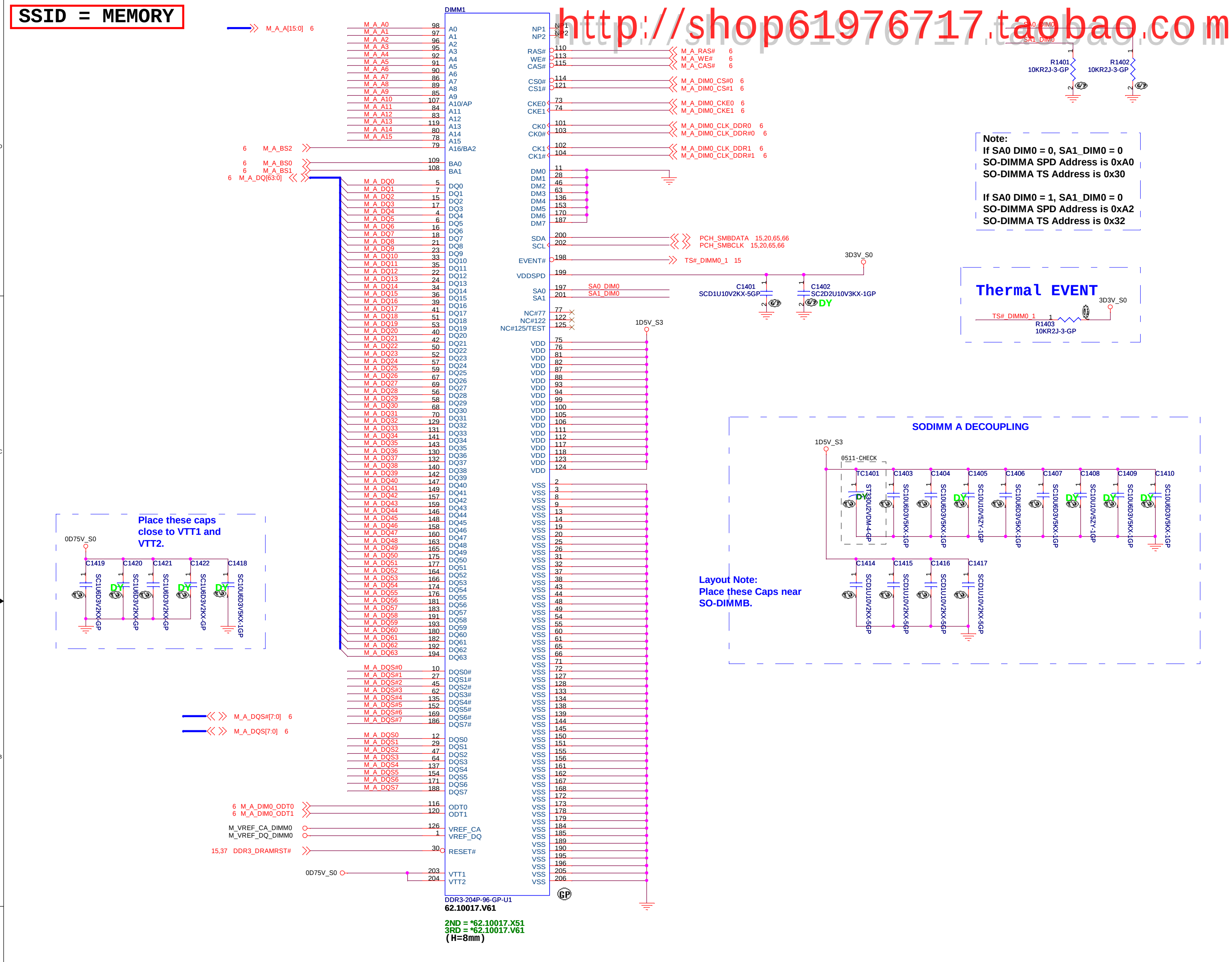
SSID = MEMORY



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Title	DDR3-SODIMM1	
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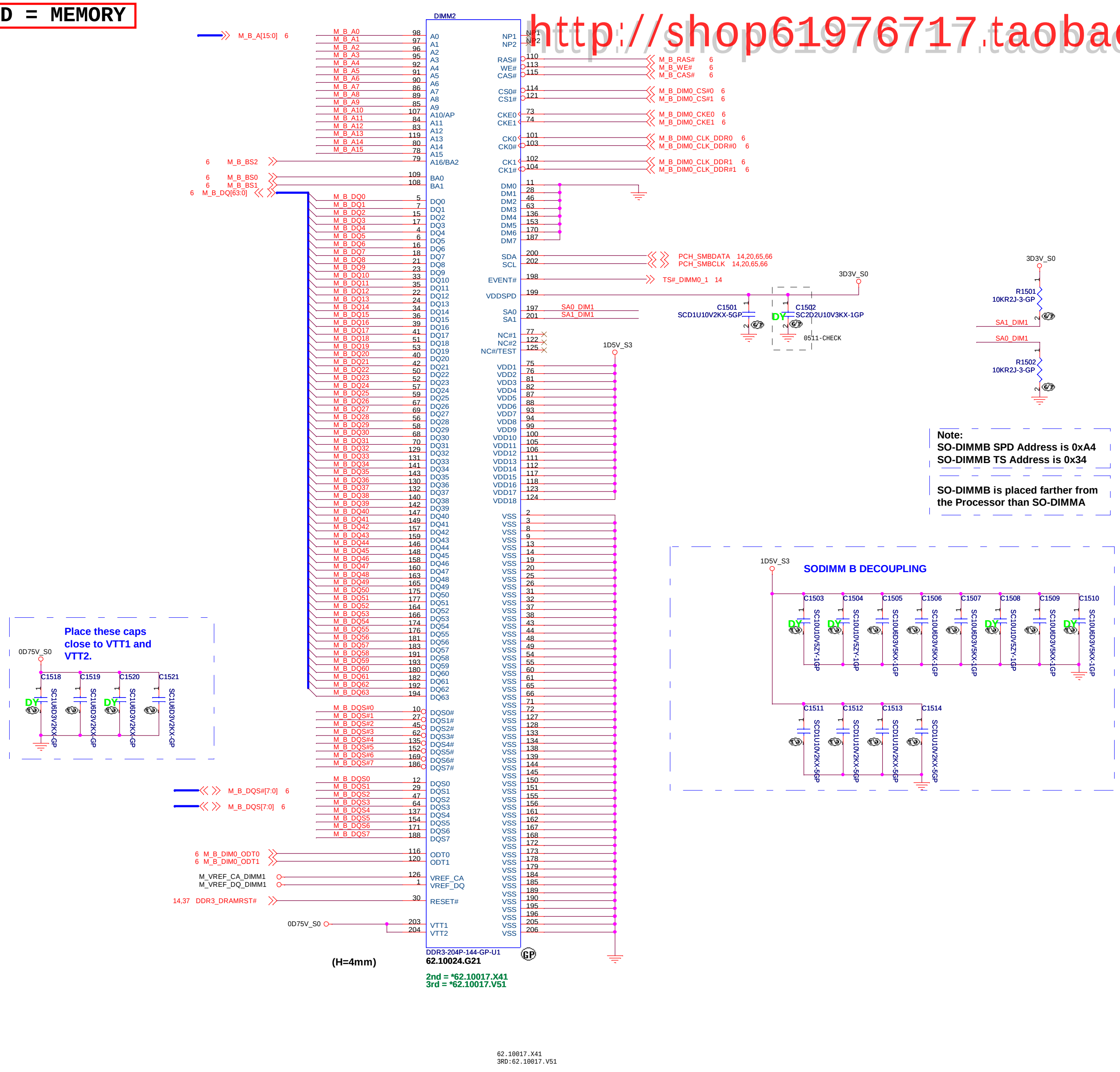
SSID = MEMORY



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Title: **DDR3-SODIMM2**

Size: A2 | Document Number: **LA480** | Rev: **SD**

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Title	***DDR3-SODIMM2***	
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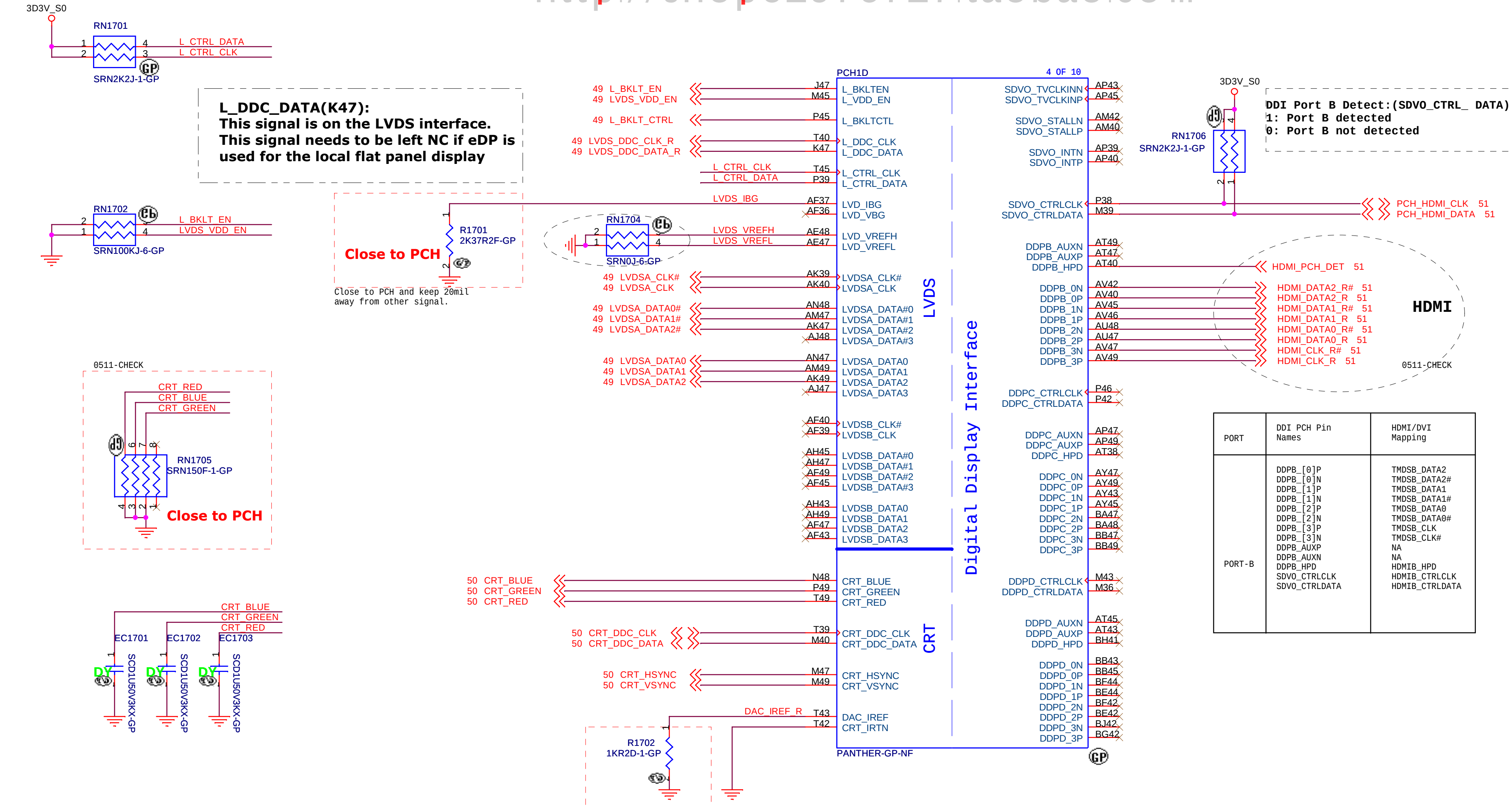

L_DDC_DATA(K47):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is used for the local flat panel display

DDI Port B Detect:(SDVO_CTRL_ DATA)
1: Port B detected
0: Port B not detected

PORT	DDI PCH Pin Names	HDMI/DVI Mapping
PORT-B	DDPB_[0]P DDPB_[0]N DDPB_[1]P DDPB_[1]N DDPB_[2]P DDPB_[2]N DDPB_[3]P DDPB_[3]N DDPB_AUXP DDPB_AUXN DDPB_HPD SDVO_CTRLCLK SDVO_CTRLDATA	TMDSB_DATA2 TMDSB_DATA2# TMDSB_DATA1 TMDSB_DATA1# TMDSB_DATA0 TMDSB_DATA0# TMDSB_CLK TMDSB_CLK# NA NA HDMIB_HPD HDMIB_CTRLCLK HDMIB_CTRLDATA

Notes:
1K 0.5% 0402

The recommended value for this external resistor is 1.0 k ±0.5%. The CRT DAC outputs may be measured when the display is completely white. If CRT DAC signal voltage value is between 665 mV to 770 mV, then the video level is within VESA specification and the reference resistor value is optimal for the motherboard design.

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Title: **PCH : LVDS/CRT/DDI**

Size	Document Number	Rev
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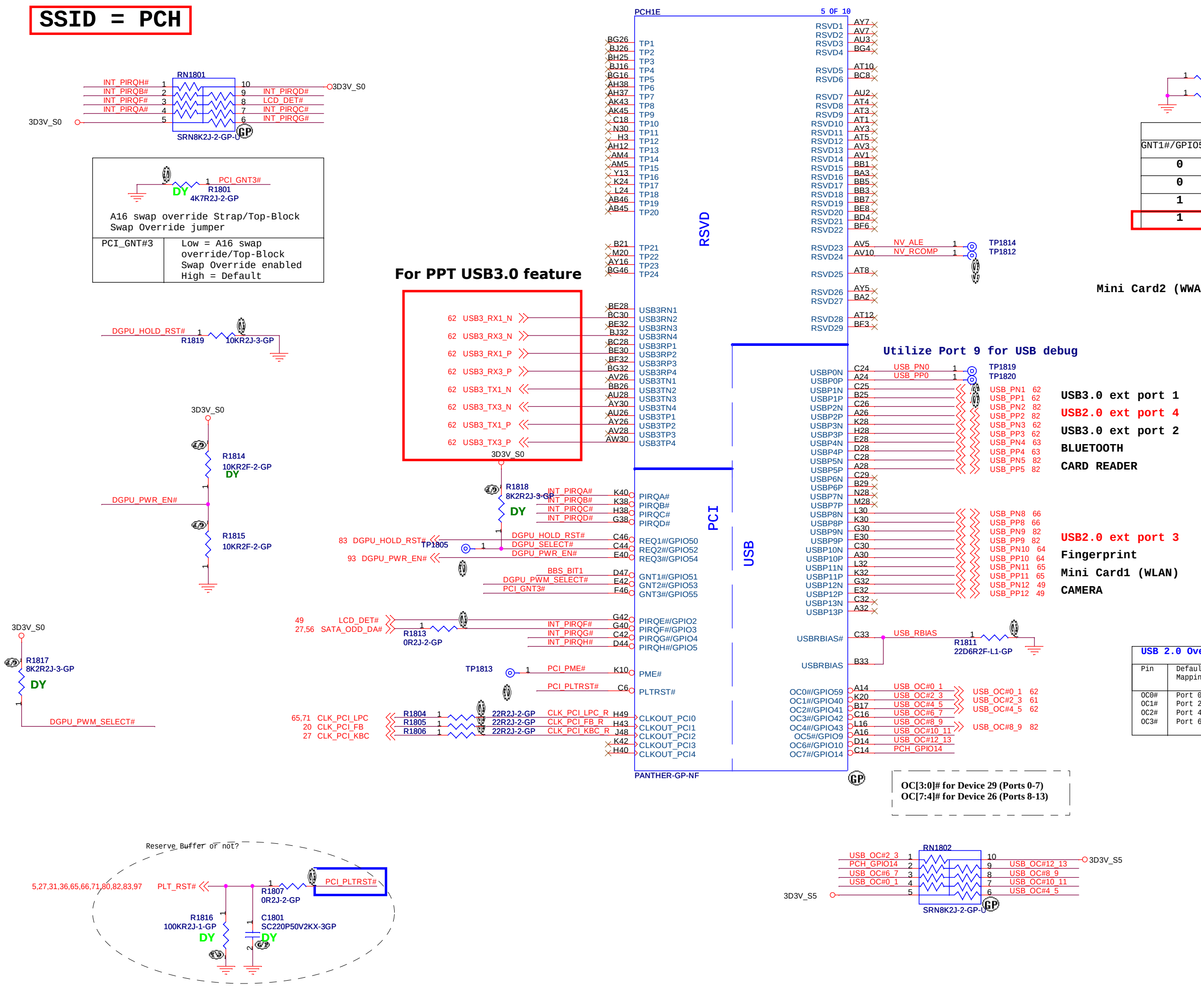

R1802 1KR2J-1-GP BBS_BIT1

R1803 1KR2J-1-GP BBS_BIT0 21

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

Mini Card2 (WWAN)

Gx8 USB Table

Pair	Device
0	X
1	USB3.0, ext port1
2	USB2.0, ext port4
3	USB3.0, ext port2
4	Bluetooth
5	CARD READER
6	X
7	X
8	3G
9	USB2.0, ext. port 3
10	Finger Print
11	Mini Card1 (WLAN)
12	CAMERA
13	X

USB 2.0 Overcurrent Pin Default Usage			
Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

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Title: PCH : PCI/USB/NVRAM/RSVD

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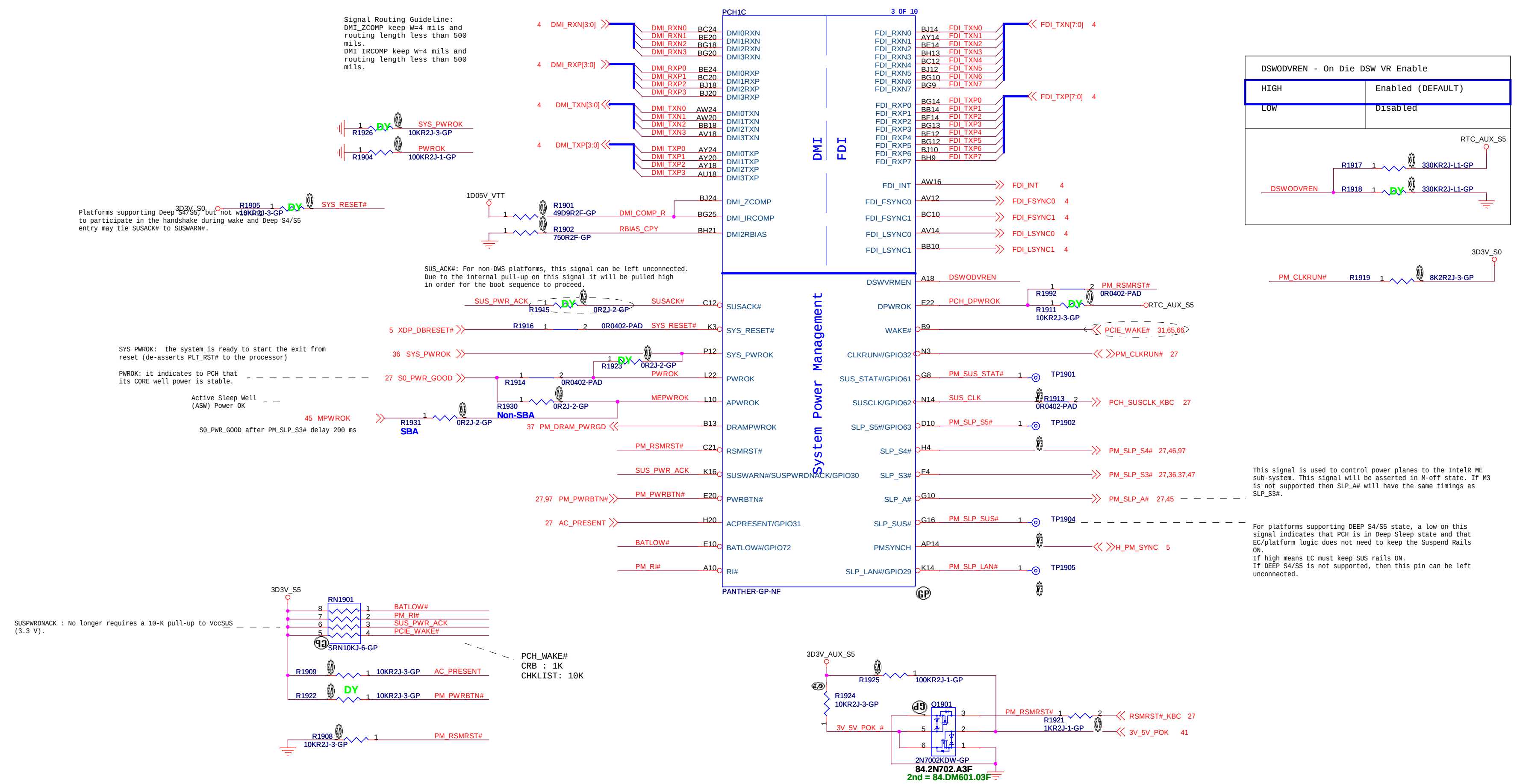
SSID = PCH

For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30



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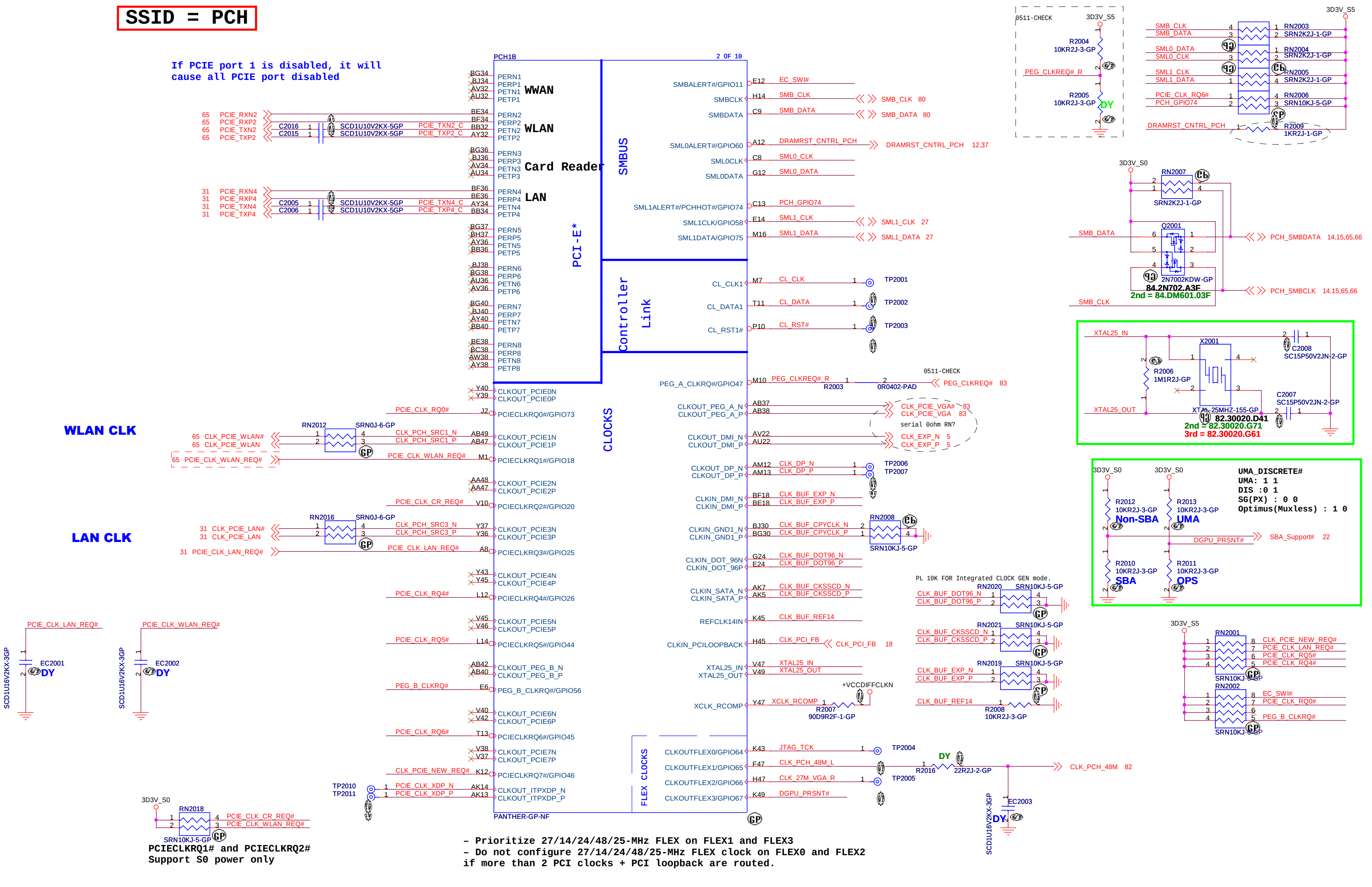
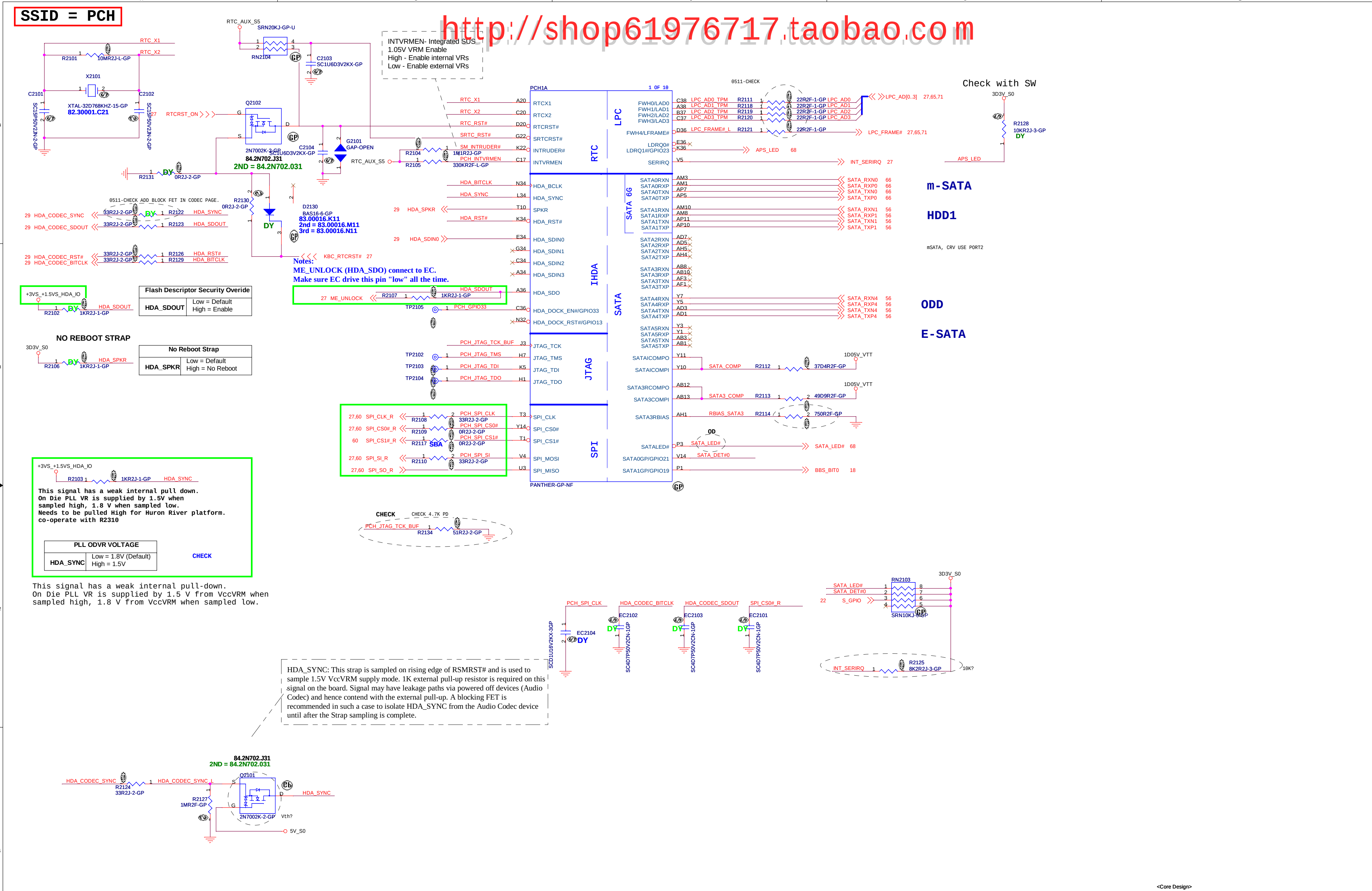
Title	**PCH : DMI/FDI/PM**	
Size A2	Document Number **LA480**	Rev **SD**
Date: Friday, January 06, 2012	Sheet 19 of 103	



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

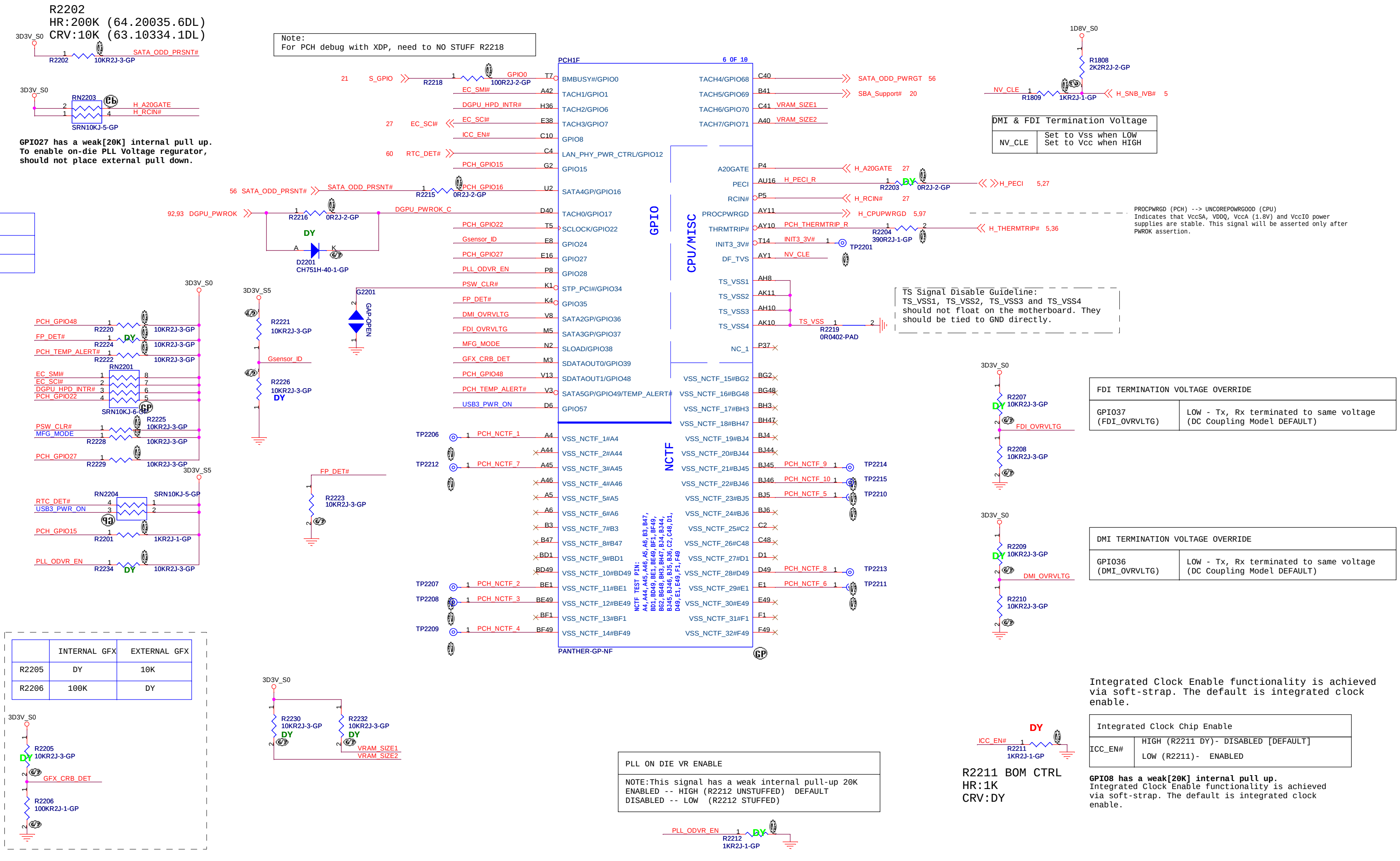
Title	PCH : PCIE/SMBUS/CLK
Size	A2
Document Number	LA480
Rev	SD
Date	Friday, January 06, 2012
Sheet	20 of 103



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
PCH : HDA/JTAG/SATA		
Size A2	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 21 of 103	



G-Sensor	ST	KIXNOK
R2226	DY	10K
R2221	10K	DY

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

<Core Design>

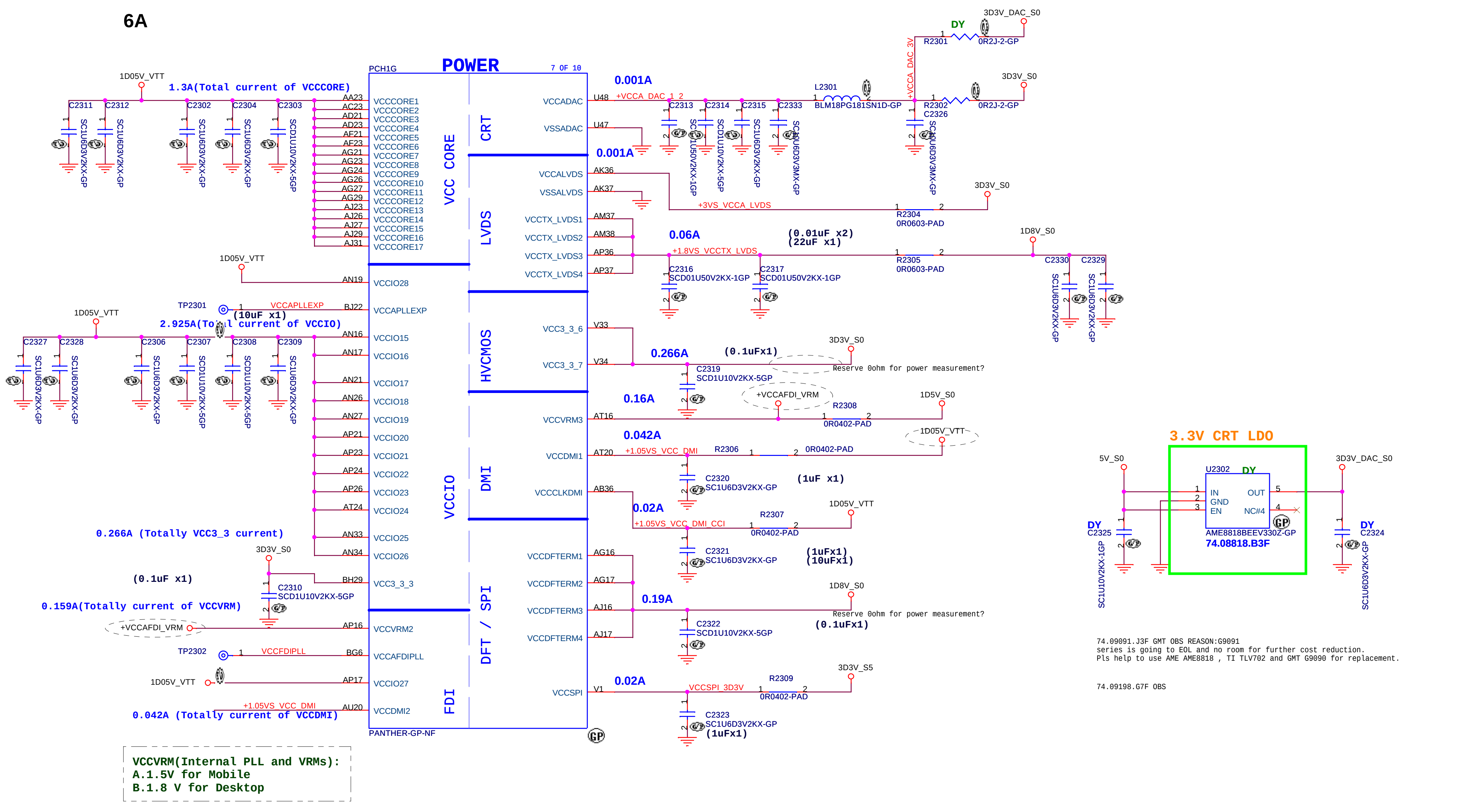
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH : GPIO/NTCF/MISC**

Size	Document Number	Rev
A2	LA480	SD

SSID = PCH

6A



Refer to NPCE795 shared SPI flash architecture

<Core Design>

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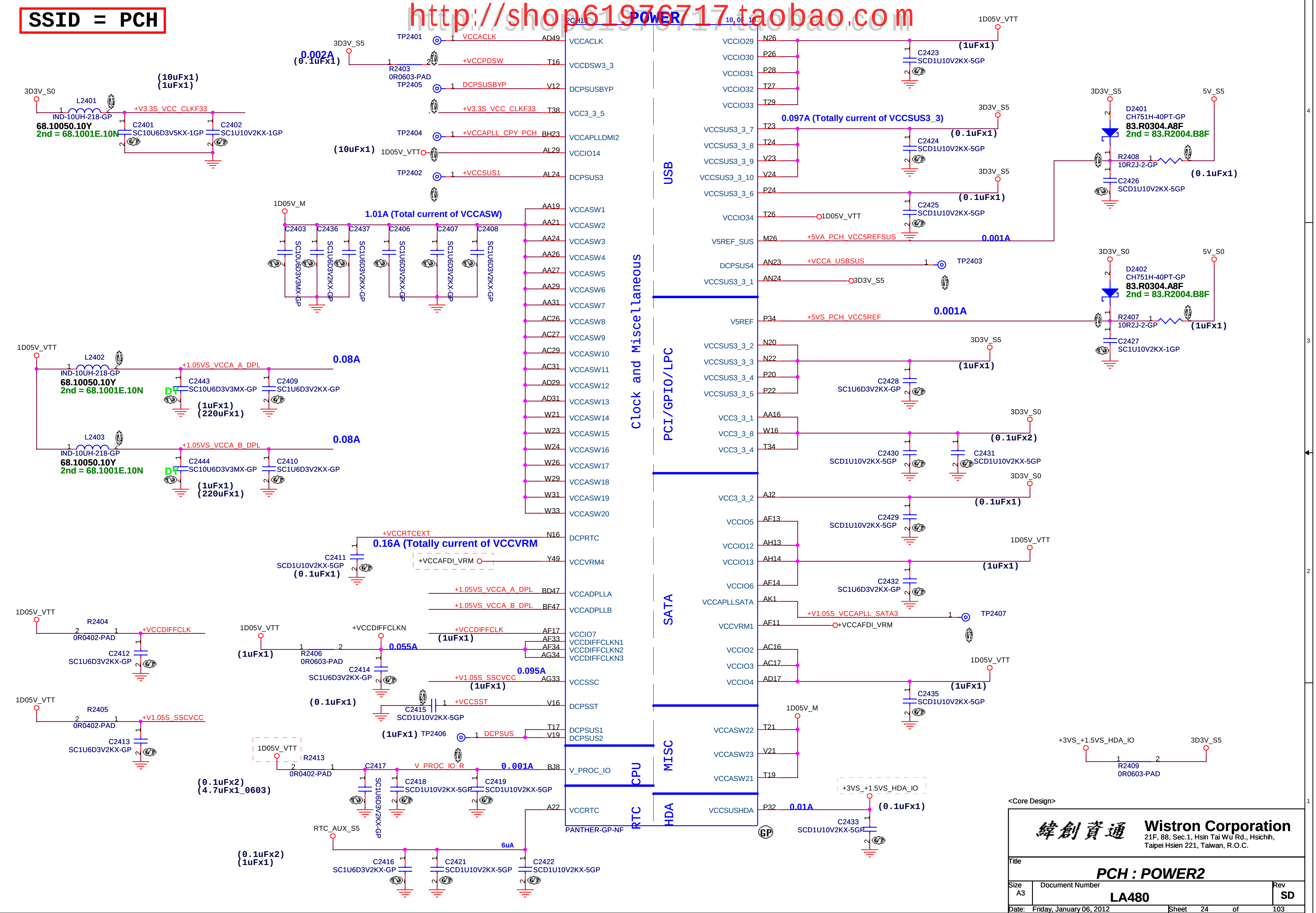
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
PCH : POWER1		
Size: A3	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet 23 of 103	

SSID = PCH



<Core Design>

緯創資通 **Wistron Corporation**
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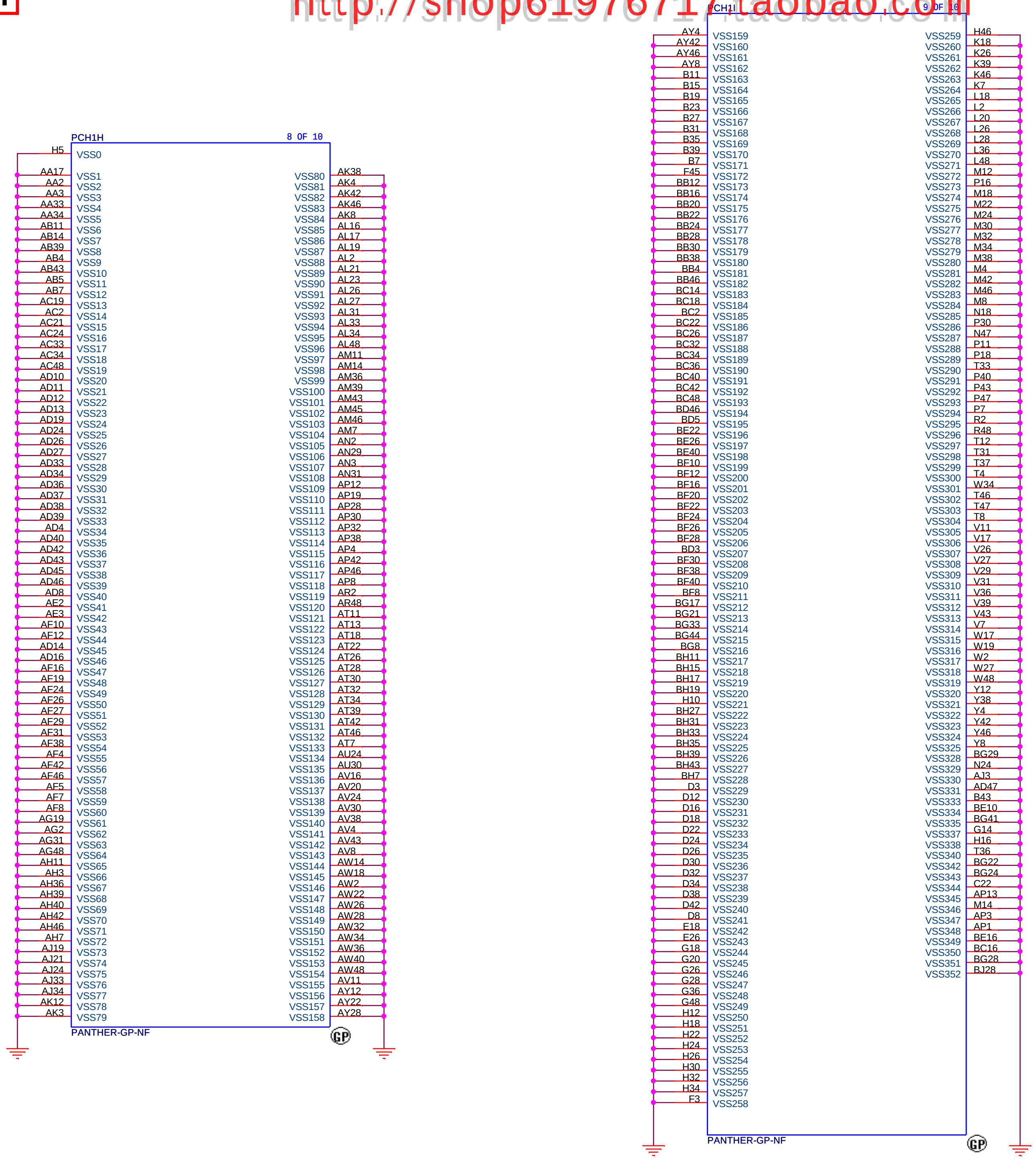
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH : POWER2**

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 24 of 103

SSID = PCH



<Core Design>

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH : VSS**

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 25 of 103

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<Core Design>

緯創資通 **Wistron Corporation**

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Taipei Hsien 221, Taiwan, R.O.C.

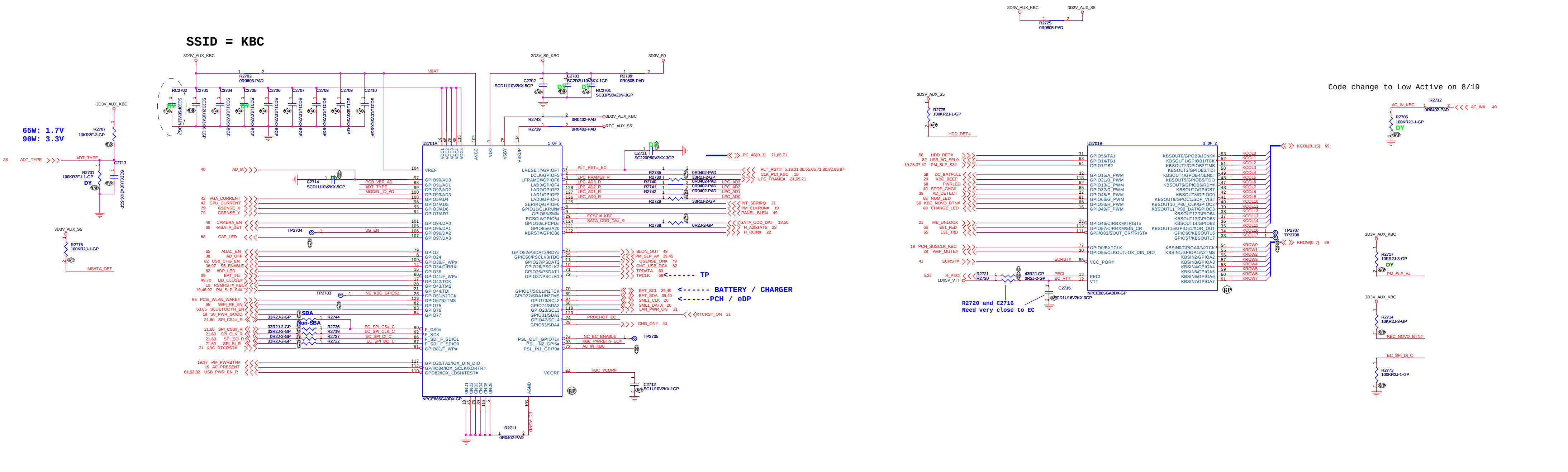
Title	***Reserved***	
Size A4	Document Number **LA480**	Rev **SD**
Date: Friday, January 06, 2012	Sheet 26 of 103	

SSID = KBC

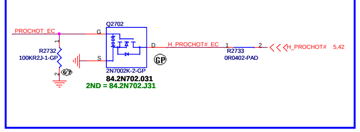
65W: 1.7V
90W: 3.3V

Code change to Low Active on 8/19

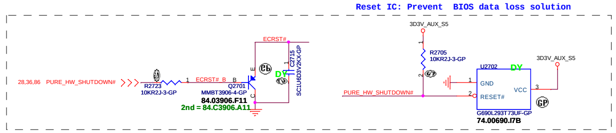
R2720 and C2716
Need very close to EC

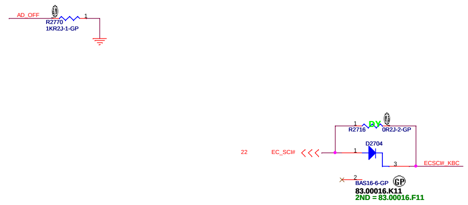


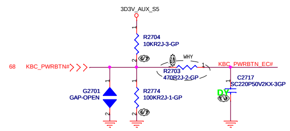
EC_GPIO47 High Active

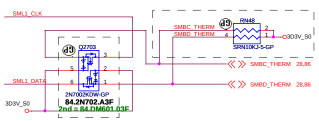


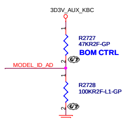
Reset IC: Prevent BIOS data loss solution





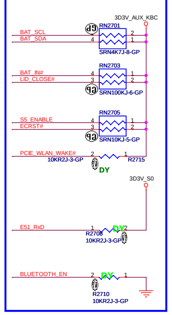


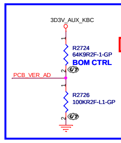




MODEL_ID_AD (Pin100)	Pull Down	Pull High	Voltage
UMA	100.0K	33.0K	2.481V
OPTIMUS	100.0K	47.0K	2.245V

EC GPIO standard PH/PL





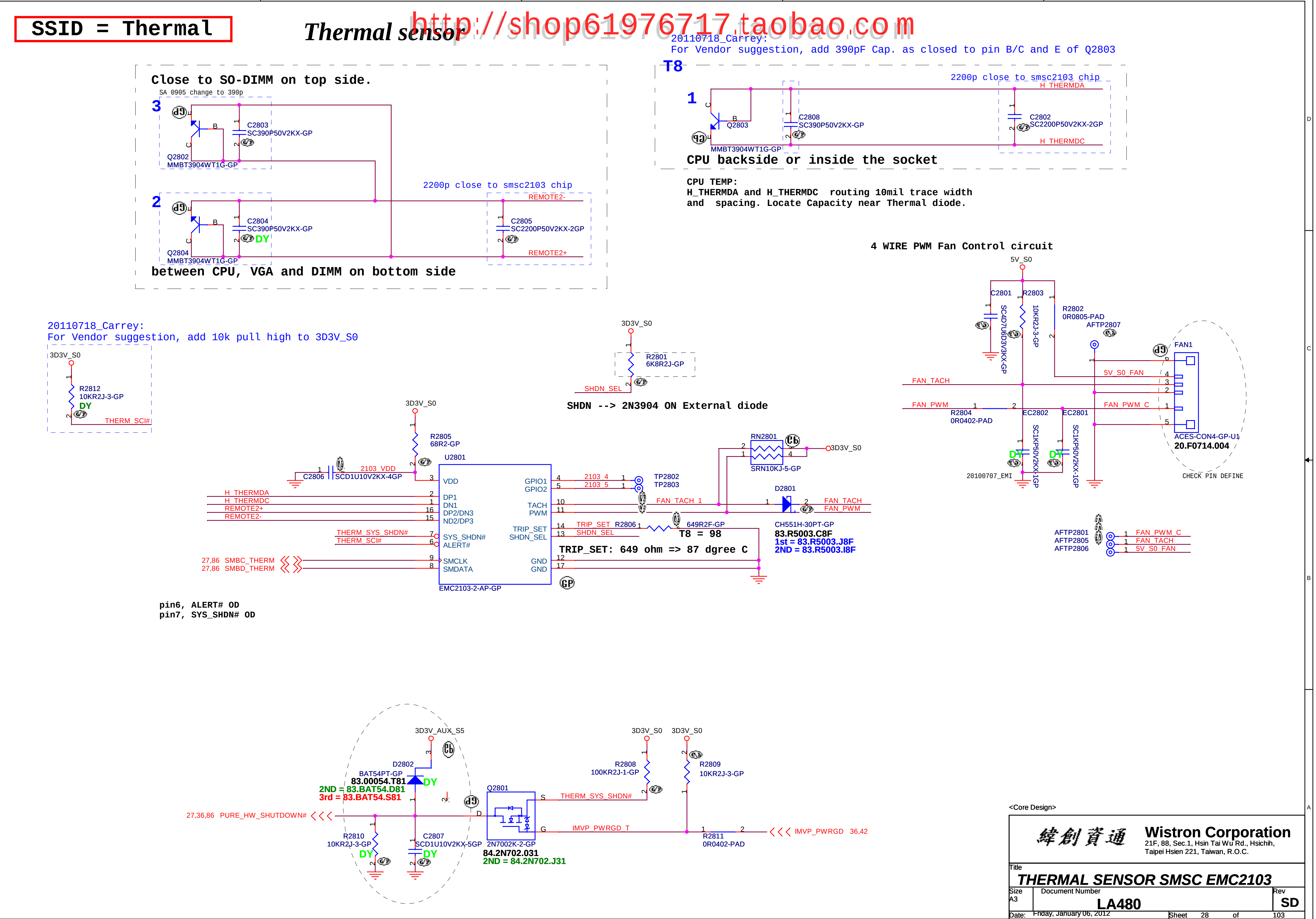
PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

71.00885.A0G
IC EMB CTRL NPCE885PA0DX LQFP 128P

<Core Design>

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

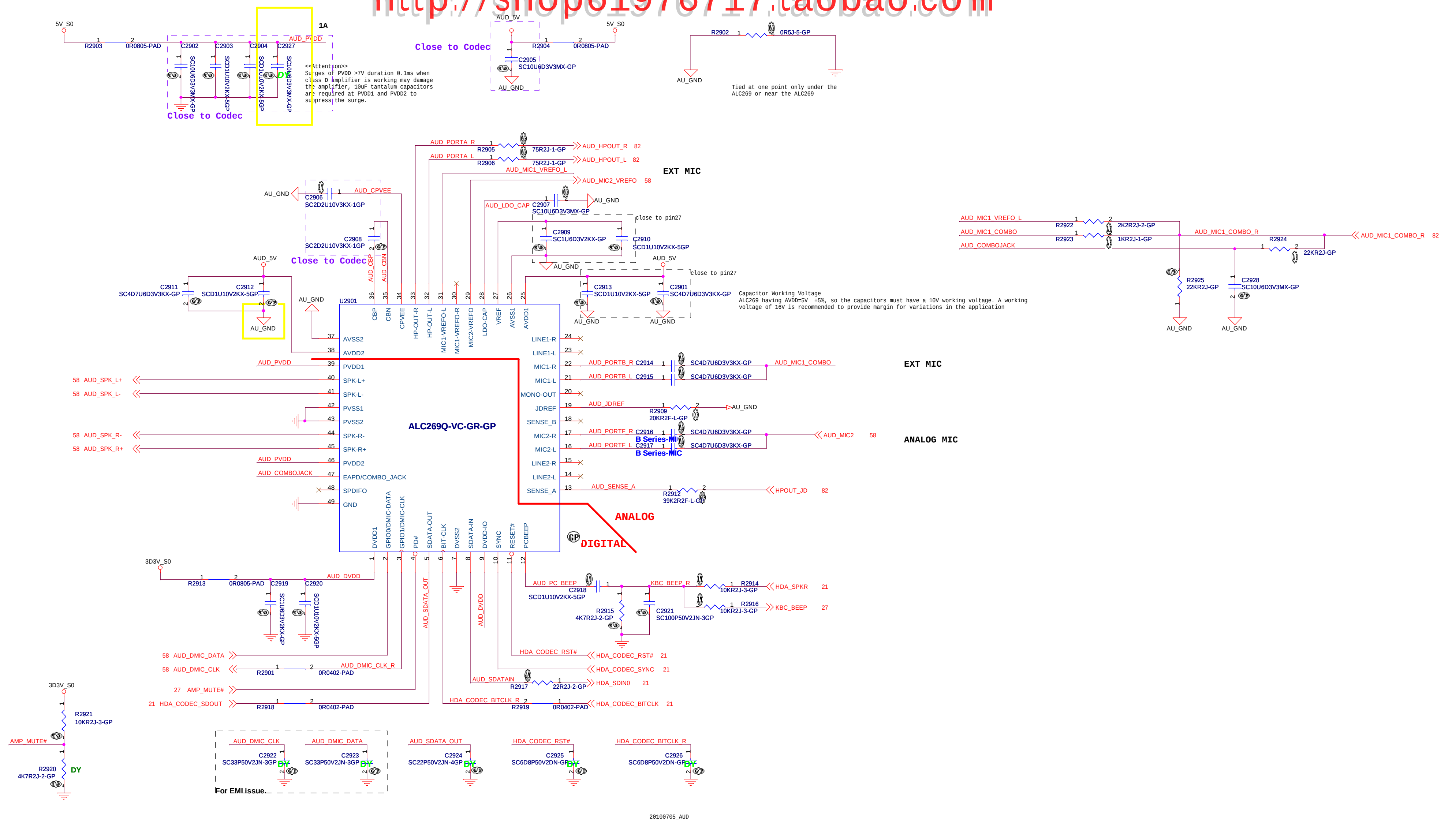
Title: <Title>
Size: A1 | Document Number: LA480 | Rev: SD
Date: Friday, January 06, 2012 | Sheet 27 of 103



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	THERMAL SENSOR SMSC EMC2103	
Size A3	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 28 of 103	



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO CODEC	
Size A2	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 29 of 103	

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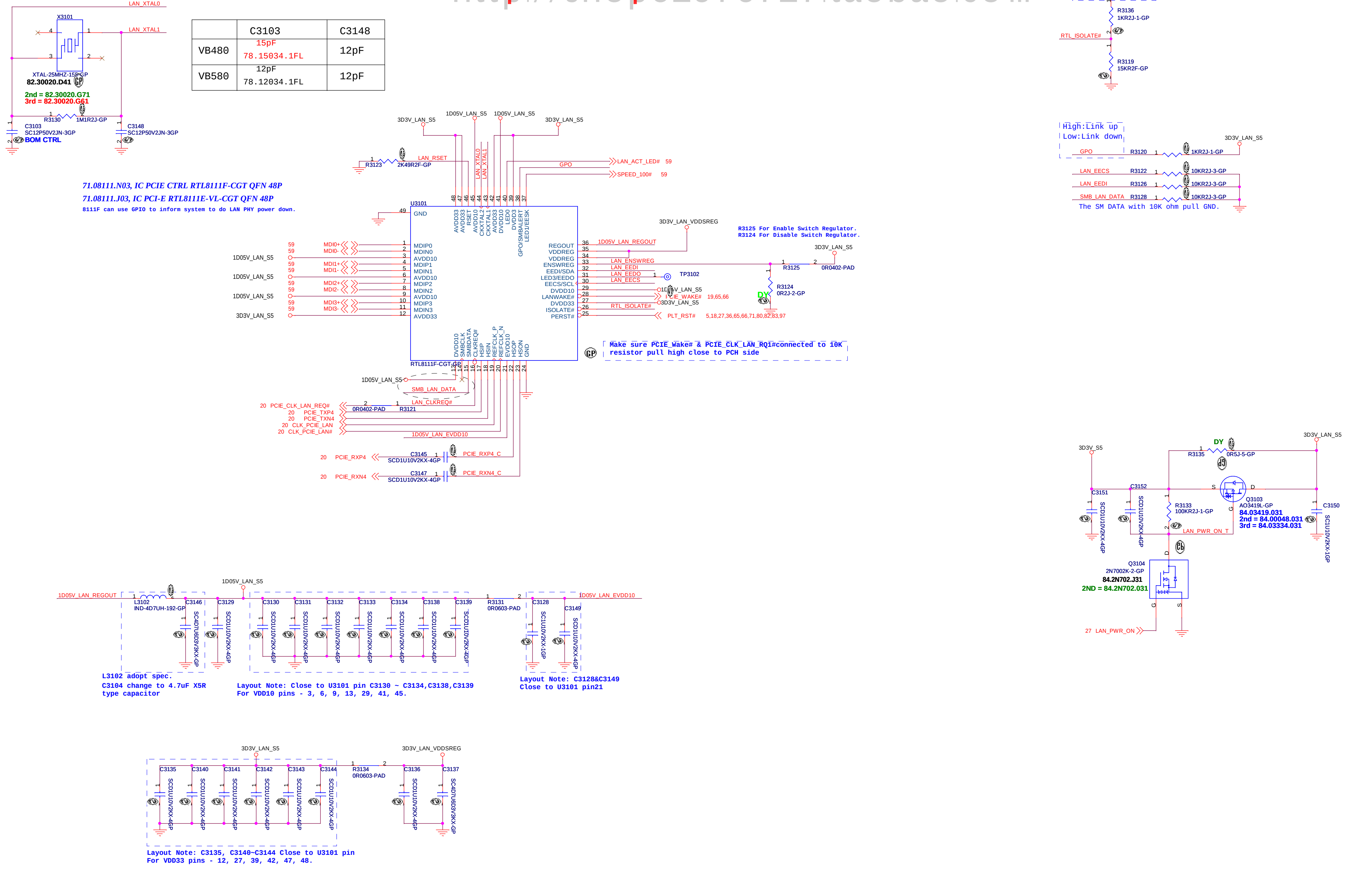
25MHz XTAL

	C3103	C3148
VB480	15pF 78.15034.1FL	12pF
VB580	12pF 78.12034.1FL	12pF



71.08111.N03, IC PCIE CTRL RTL8111F-CGT QFN 48P

71.08111.J03, IC PCI-E RTL8111E-VL-CGT QFN 48P

8111F can use GPIO to inform system to do LAN PHY power down.

L3102 adopt spec.
C3104 change to 4.7uF X5R type capacitor

Layout Note: Close to U3101 pin C3130 ~ C3134,C3138,C3139 For VDD10 pins - 3, 6, 9, 13, 29, 41, 45.

Layout Note: C3128&C3149 Close to U3101 pin21

Layout Note: C3135, C3140~C3144 Close to U3101 pin For VDD33 pins - 12, 27, 39, 42, 47, 48.

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**R5U220 (CARD READER)**
Size A1	Document Number **LA480** — Rev **SD**
Date: Friday, January 06, 2012	Sheet 32 of 103

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<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Reserved***	
Size A4	Document Number **LA480**	Rev **SD**
Date: Friday, January 06, 2012	Sheet 33 of 103	

5 4 3 2 1

D C B A

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Reserved	
Size A4	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 34 of 103	

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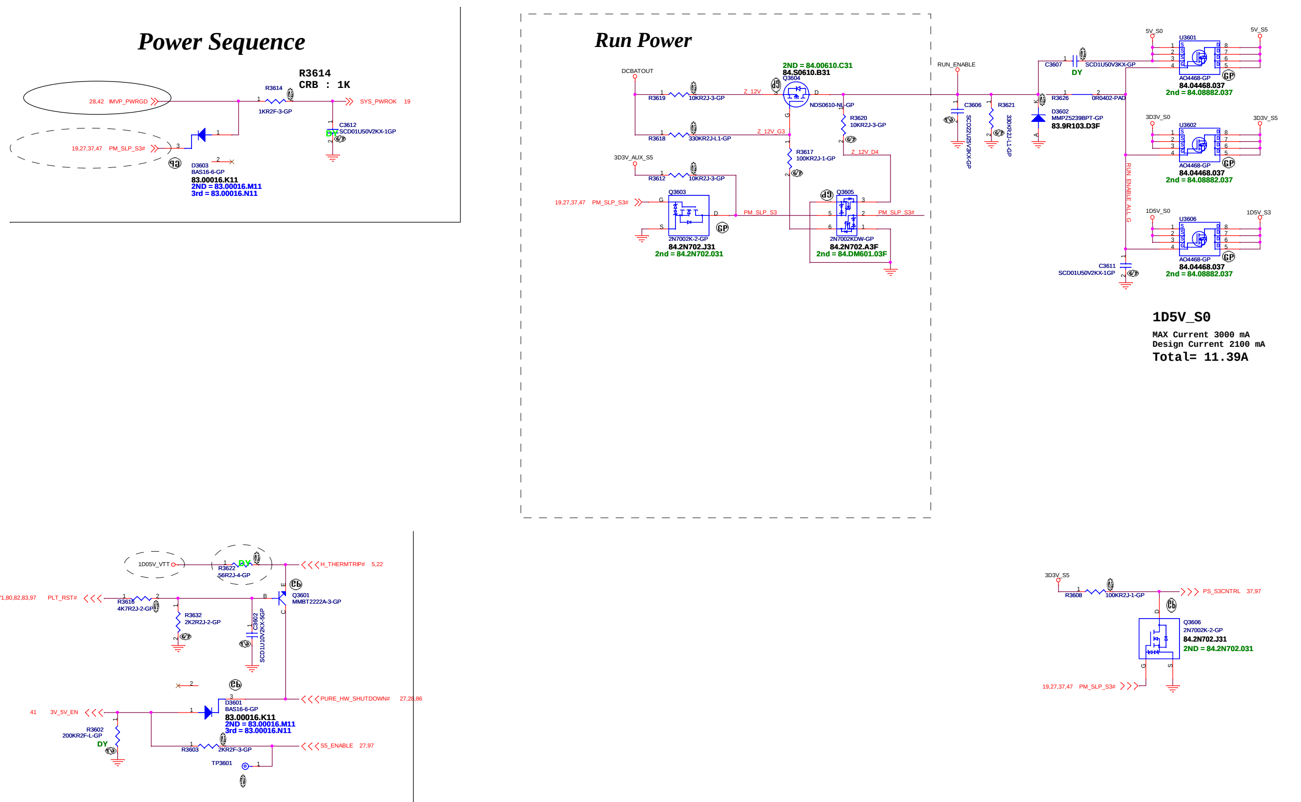
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***USB 3.0 Controller***	
Size A4	Document Number **LA480**	Rev **SD**
Date: Friday, January 06, 2012	Sheet 35 of 103	



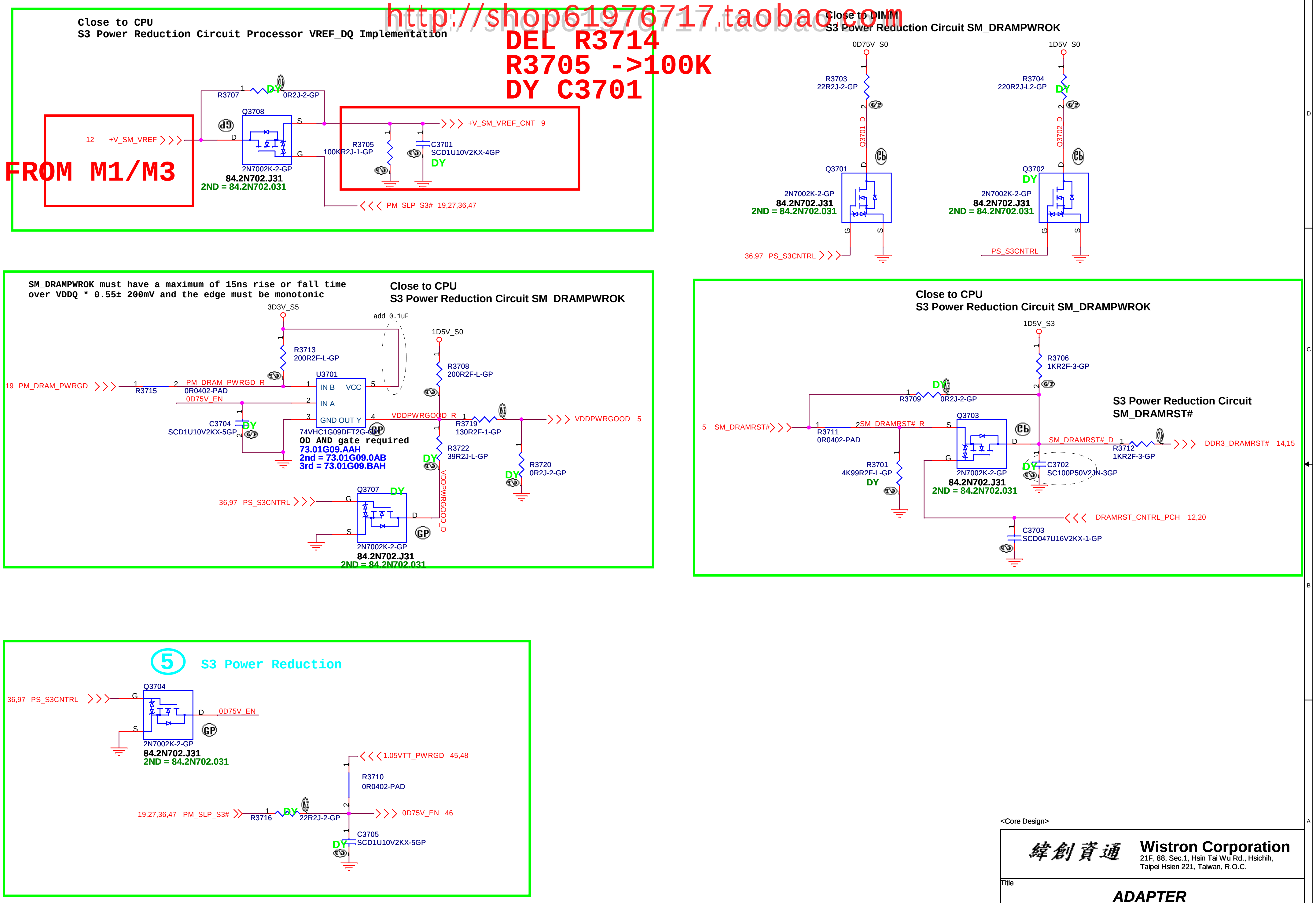
1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	*Power Plane Enable*	
Size A1	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 36 of 103	



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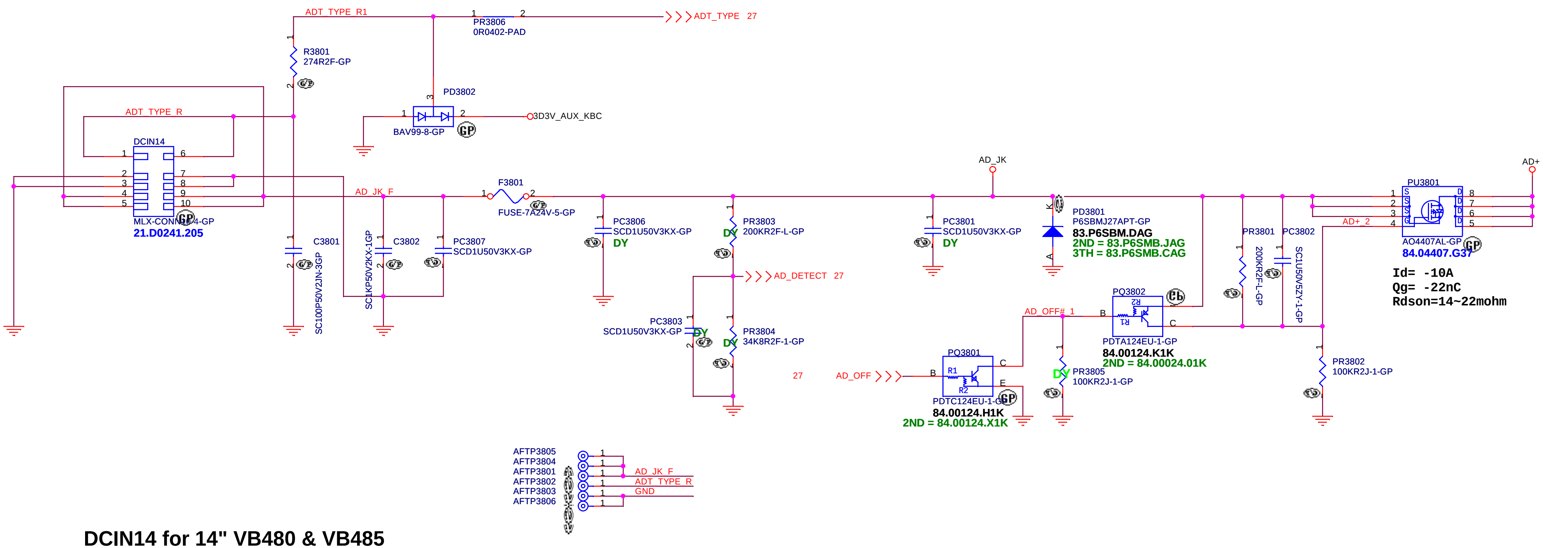
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ADAPTER	
Size A3	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 37 of 103	

Adaptor in to generate DCBATOUT



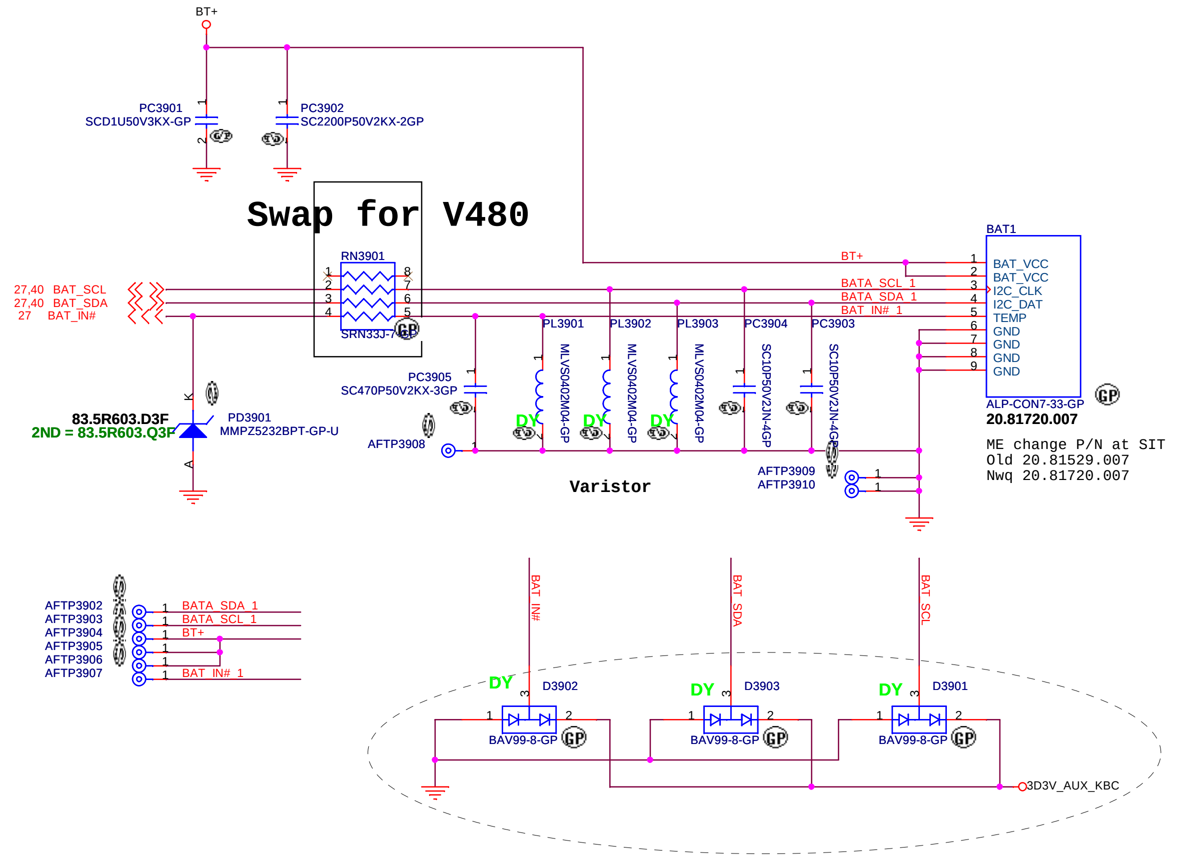
DCIN14 for 14" VB480 & VB485
DCIN15 for 15" VB580 & VB585

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*DCIN_JACK*	
Size A3	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 38 of 103	

BATTERY CONNECTOR



DY on LAB stage

<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BATT_CONN	
Size	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 39 of 103	

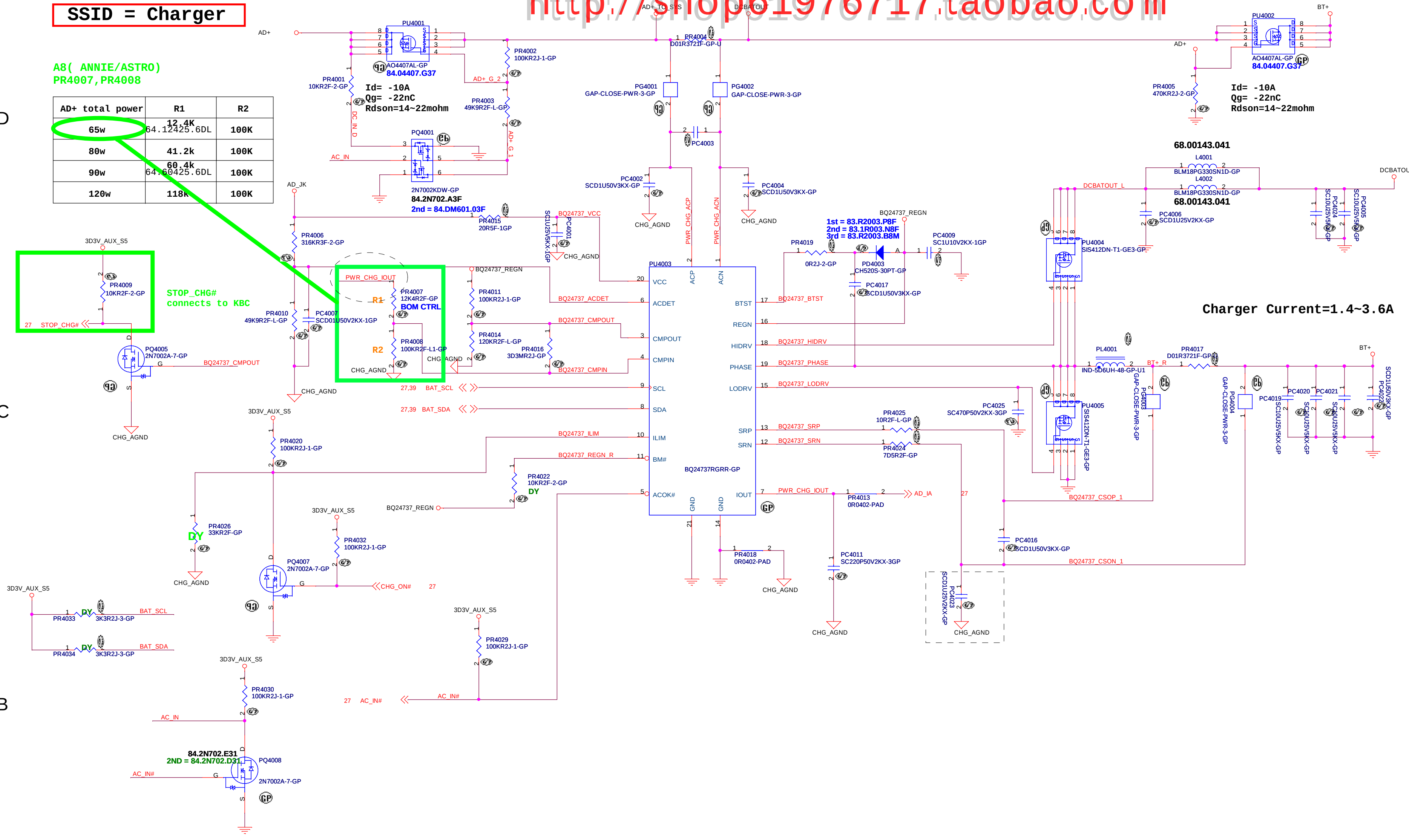
SSID = Charger

A8(ANNIE/ASTRO)
PR4007,PR4008

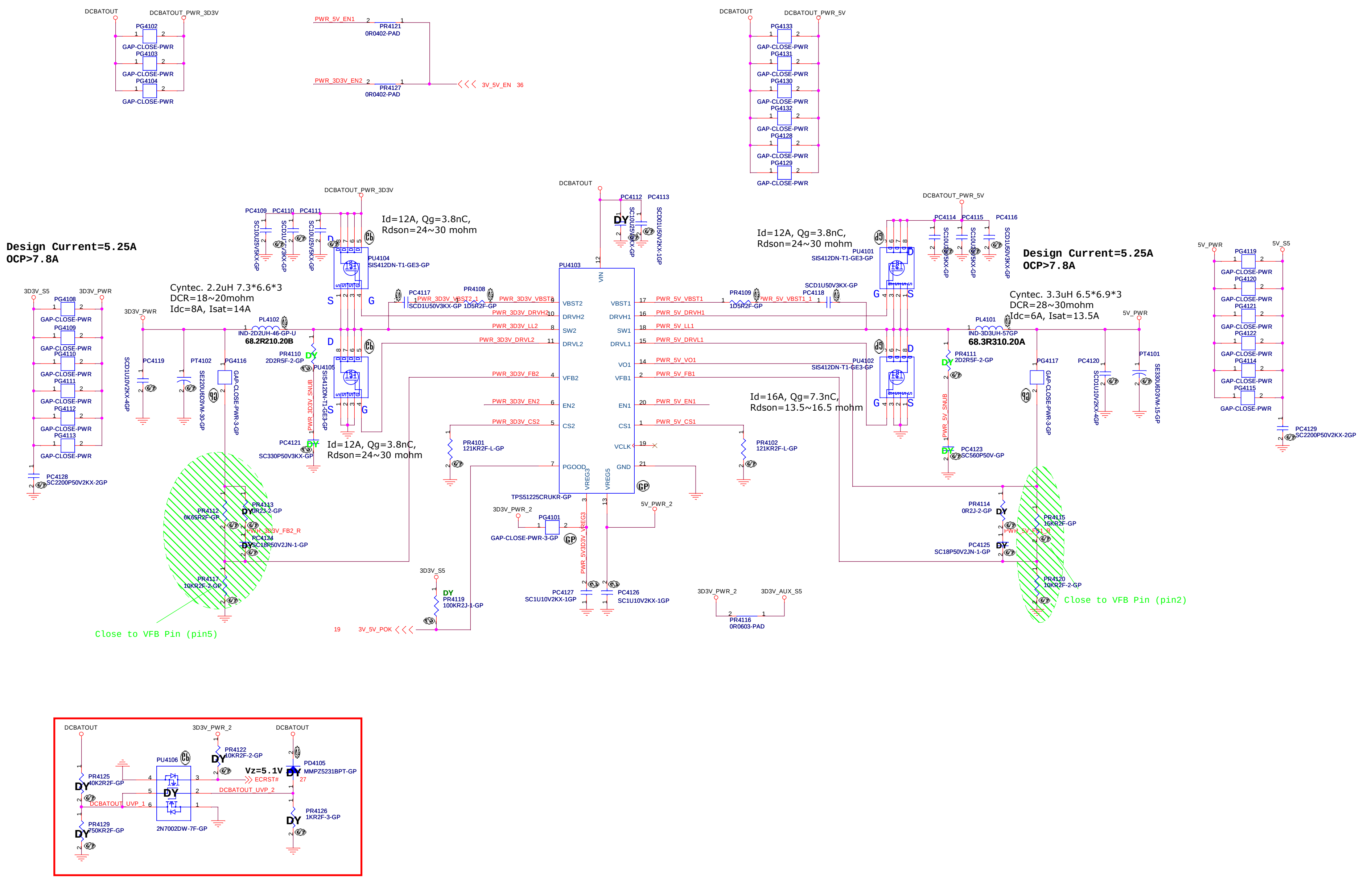
AD+ total power	R1	R2
65w	12.4K 64.12425.6DL	100K
80w	41.2k	100K
90w	60.4k 64.60425.6DL	100K
120w	118K	100K

STOP_CHG# connects to KBC

Charger Current=1.4~3.6A

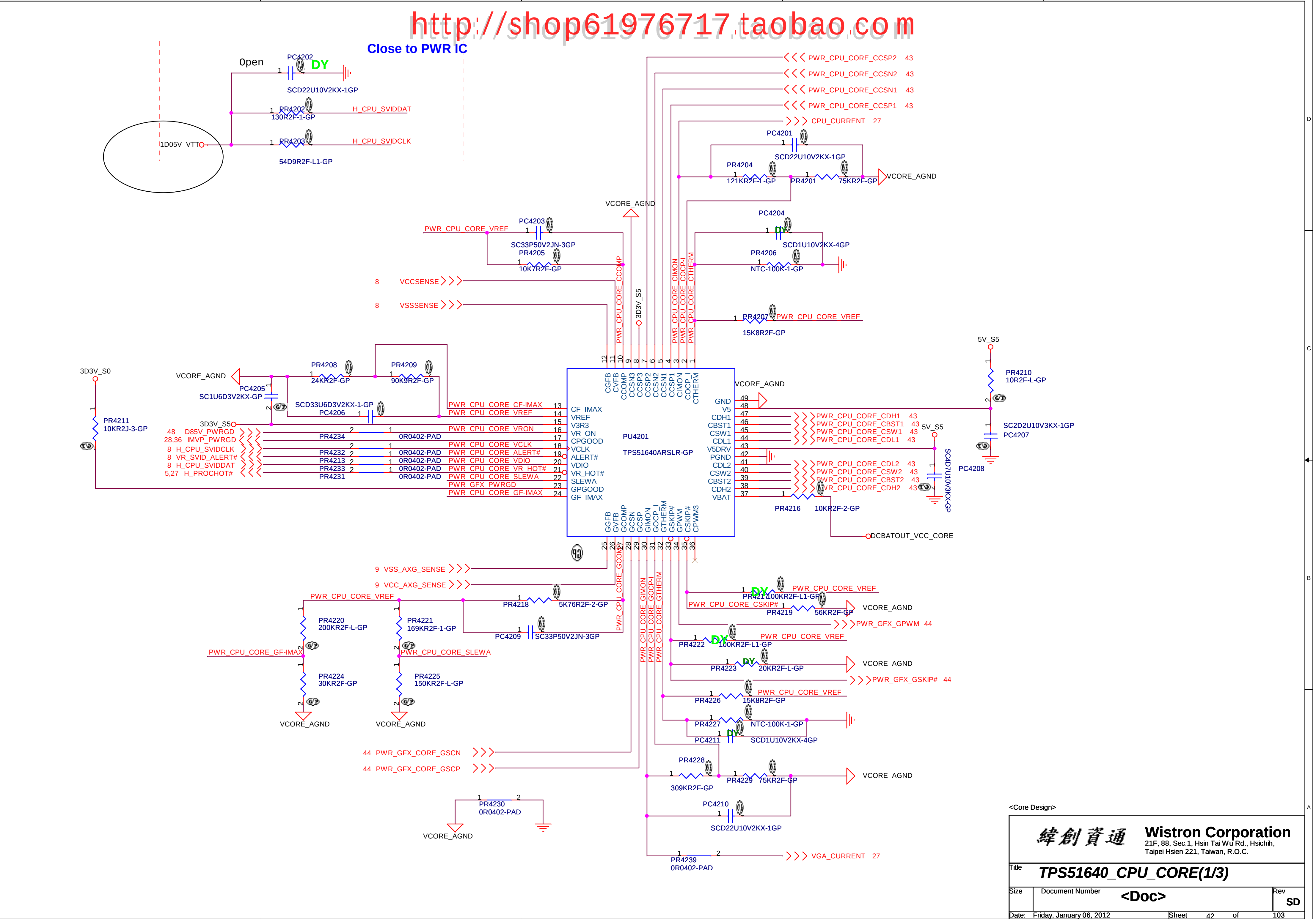


SSID = PWR.Plane.Regulator_5v3p3v



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	TPS51123_5V_3D3V
Size / Document Number	Rev SD
Date: Friday, January 06, 2012	Sheet 41 of 103

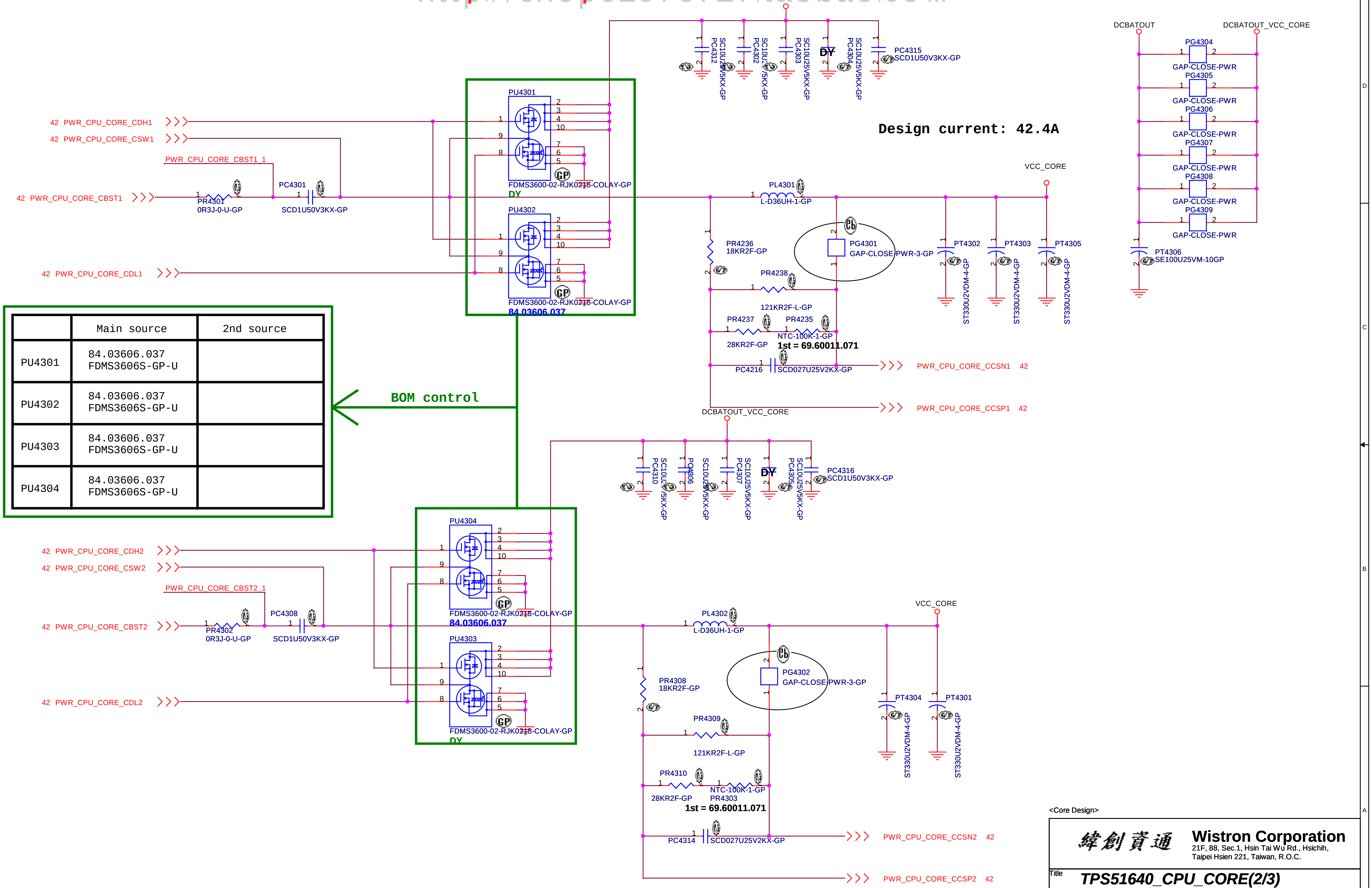


<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51640_CPU_CORE(1/3)	
Size	Document Number: <Doc>	Rev: SD
Date: Friday, January 06, 2012	Sheet 42 of 103	



	Main source	2nd source
PU4301	84.03606.037 FDMS3606S-GP-U	
PU4302	84.03606.037 FDMS3606S-GP-U	
PU4303	84.03606.037 FDMS3606S-GP-U	
PU4304	84.03606.037 FDMS3606S-GP-U	

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

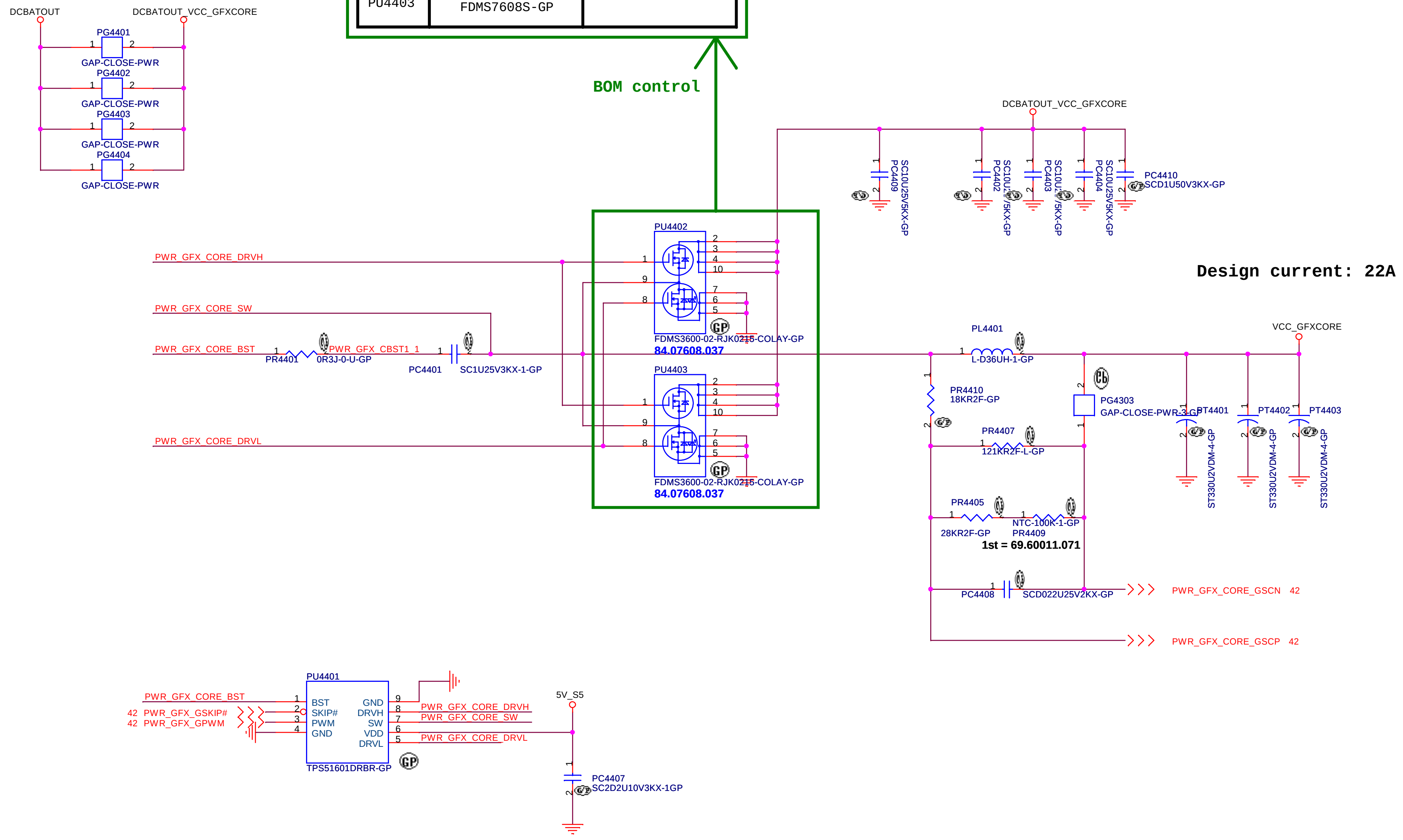
Title: **TPS51640_CPU_CORE(2/3)**

Size | Document Number: <Doc> | Rev: SD

Date: Friday, January 06, 2012 | Sheet 43 of 103

	Main source	2nd source
PU4402	84.07608.037 FDMS7608S-GP	
PU4403	84.07608.037 FDMS7608S-GP	

BOM control



<Core Design>

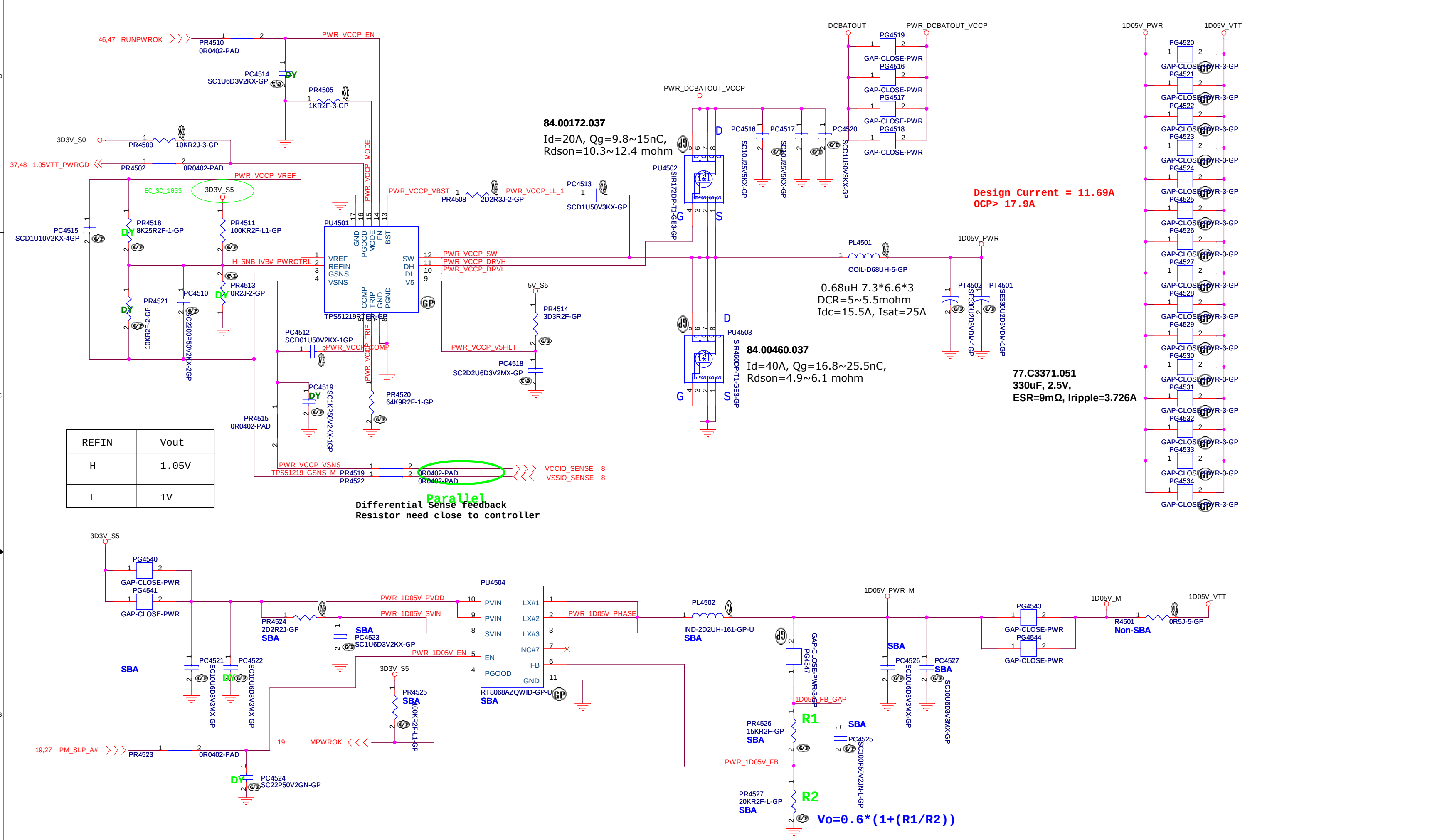
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: *TPS51640_CPU_CORE(3/3)*

Size	Document Number	Rev
	<Doc>	SD

Date: Friday, January 06, 2012 | Sheet 44 of 103

TPS51219 for 1D05V



REFIN	Vout
H	1.05V
L	1V

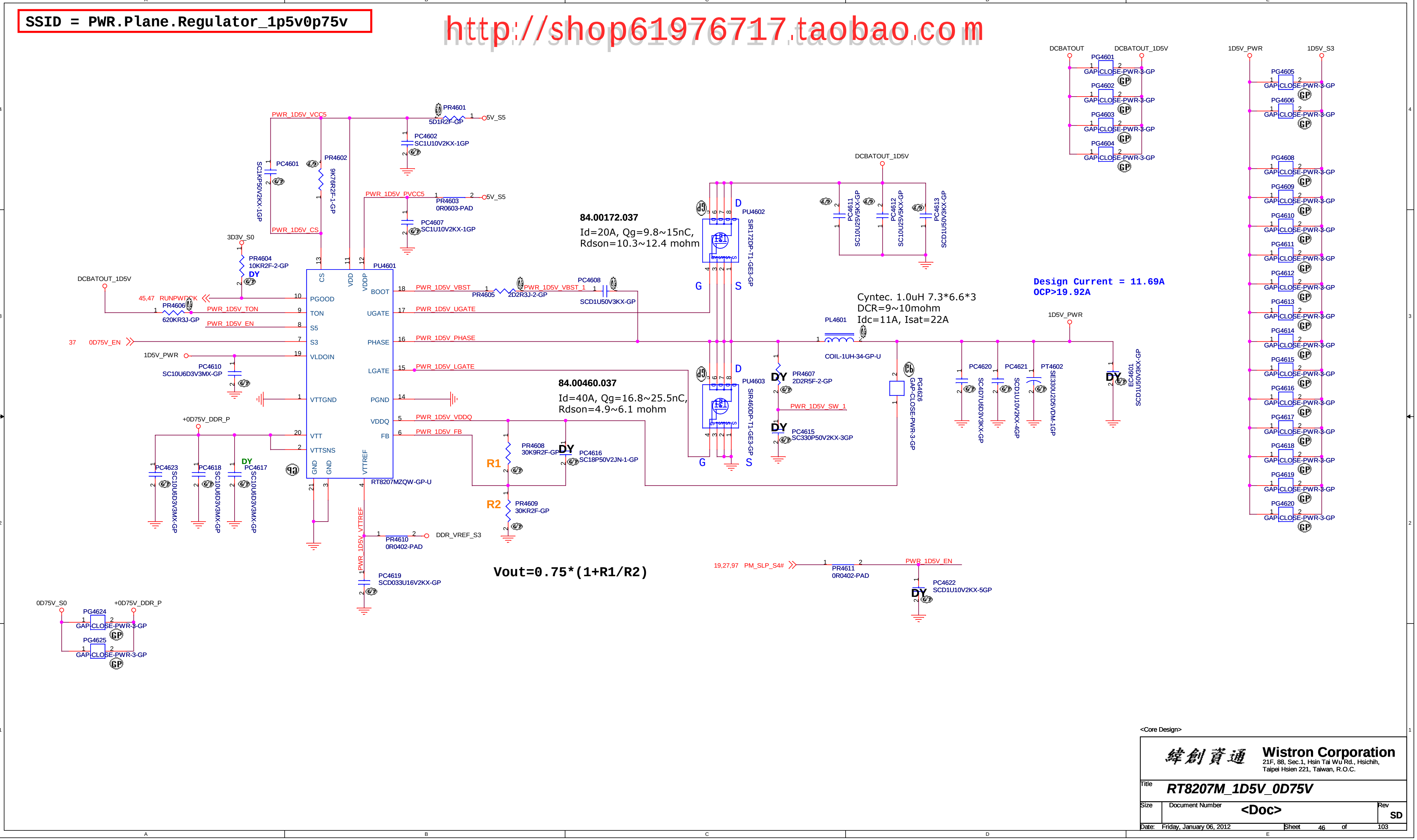
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51211_1D05V

Size | Document Number | Rev SD

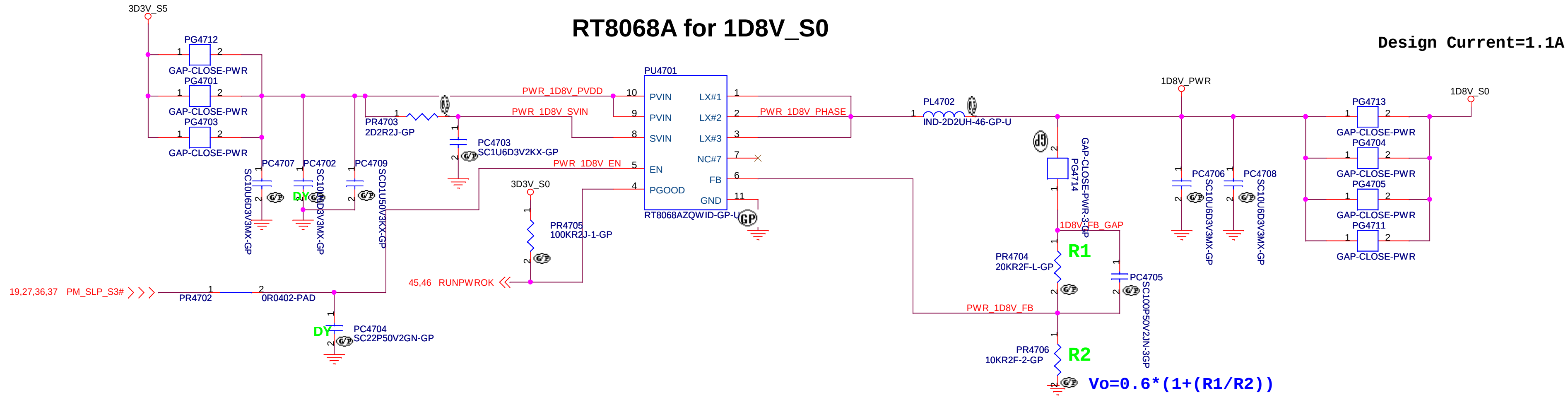
Date: Friday, January 06, 2012 Sheet 45 of 103


SSID = PWR.Plane.Regulator_1p5v0p75v
84.00172.037
Id=20A, Qg=9.8~15nC,
Rdson=10.3~12.4 mohm
84.00460.037
Id=40A, Qg=16.8~25.5nC,
Rdson=4.9~6.1 mohm
Cyntec. 1.0uH 7.3*6.6*3
DCR=9~10mohm
Idc=11A, Isat=22A
Design Current = 11.69A
OCP>19.92A
Vout=0.75*(1+R1/R2)
R1
R2
PU4601
RT8207MZQW-GP-U
PGOOD
TON
S5
S3
VLDOIN
VTTGND
VTT
VTTSNS
GND
VTTREF
BOOT
UGATE
PHASE
LGATE
PGND
VDDQ
FB
CS
VDD
VDDP
PU4602
SIR172DP-T1-GE3-GP
PU4603
SIR460DP-T1-GE3-GP
PL4601
COIL-1UH-34-GP-U
PR4601 5D1R2F-GP
PR4602 9K76R2F-1-GP
PR4603 0R0603-PAD
PR4604 10KR2F-2-GP
PR4605 2D2R3J-2-GP
PR4606 620KR3J-GP
PR4607 2D2R5F-2-GP
PR4608 30K9R2F-GP
PR4609 30KR2F-GP
PR4610 0R0402-PAD
PR4611 0R0402-PAD
PC4601 SC1KP50V2KX-1GP
PC4602 SC1U10V2KX-1GP
PC4607 SC1U10V2KX-1GP
PC4608 SCD1U50V3KX-GP
PC4610 SC10U6D3V3MX-GP
PC4611 SC10U25V5KX-GP
PC4612 SC10U25V5KX-GP
PC4613 SCD1U50V3KX-GP
PC4615 SC330P50V2KX-3GP
PC4616 SC18P50V2JN-1-GP
PC4617 SC10U6D3V3MX-GP
PC4618 SC10U6D3V3MX-GP
PC4619 SCD033U16V2KX-GP
PC4620 SC4D7U6D3V3KX-GP
PC4621 SCD1U10V2KX-4GP
PC4622 SCD1U10V2KX-5GP
PC4623 SC10U6D3V3MX-GP
PT4602 SE330U2D5VDM-1GP
EC4601 SCD1U50V3KX-GP
PG4626 GAP-CLOSE-PWR-3-GP
PG4601–PG4620, PG4624, PG4625 GAP-CLOSE-PWR-3-GP
PWR_1D5V_VCC5
PWR_1D5V_CS
PWR_1D5V_PVCC5
PWR_1D5V_VBST
PWR_1D5V_VBST_1
PWR_1D5V_UGATE
PWR_1D5V_PHASE
PWR_1D5V_LGATE
PWR_1D5V_VDDQ
PWR_1D5V_FB
PWR_1D5V_TON
PWR_1D5V_EN
PWR_1D5V_SW_1
PWR_1D5V_VTTREF
5V_S5
3D3V_S0
DCBATOUT
DCBATOUT_1D5V
1D5V_PWR
1D5V_S3
0D75V_S0
+0D75V_DDR_P
DDR_VREF_S3
45,47 RUNPWROK
37 0D75V_EN
19,27,97 PM_SLP_S4#
DY
G
D
S
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title RT8207M_1D5V_0D75V
Size Document Number <Doc> Rev SD
Date: Friday, January 06, 2012 Sheet 46 of 103

SSID = PWR.Plane.Regulator_1p8v

RT8068A for 1D8V_S0

Design Current=1.1A



<Core Design>

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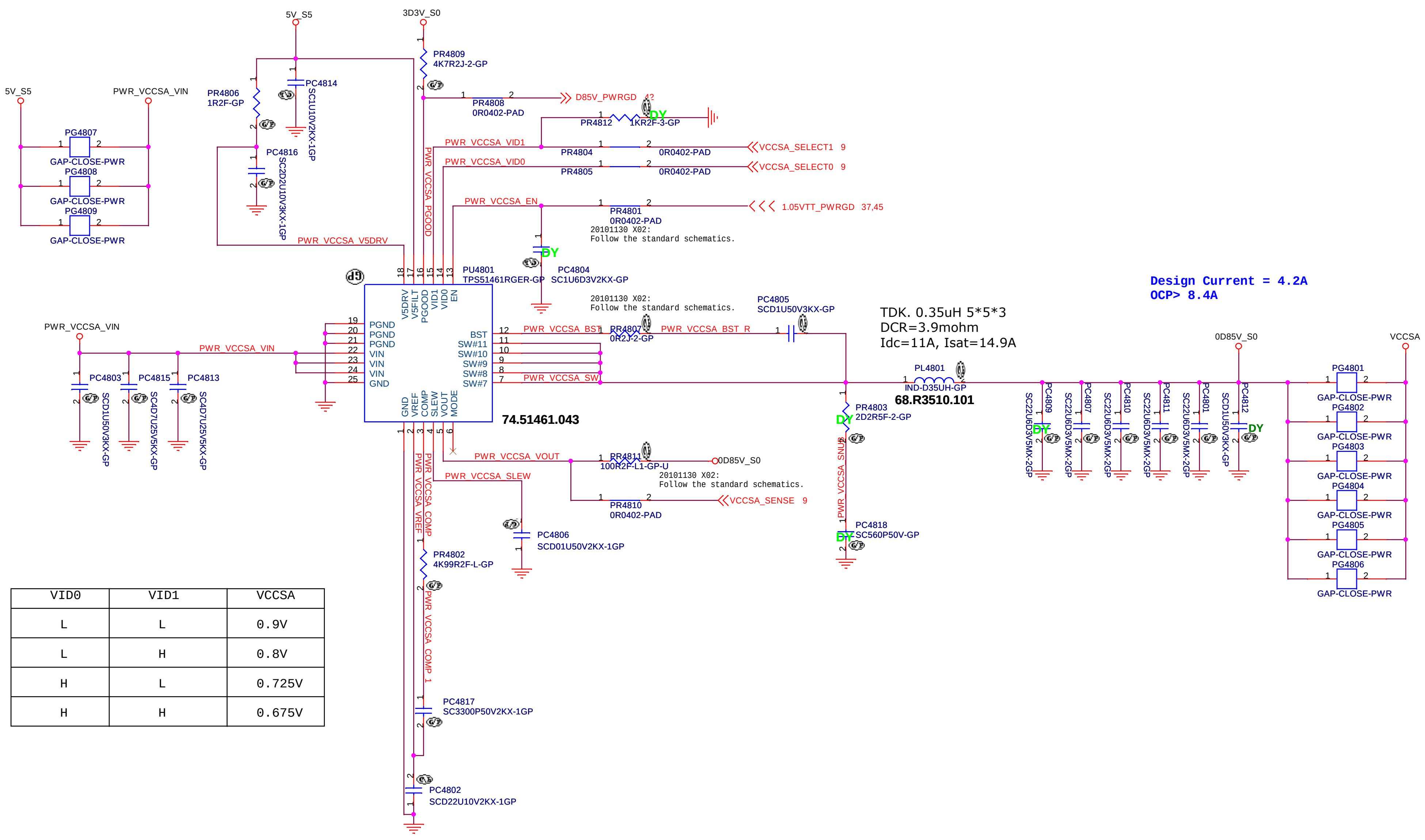
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PWM_1D8V_RT8015B
Size	Document Number
Rev	SD
Date:	Friday, January 06, 2012
Sheet	47 of 103

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VCCSA_TPS51461**

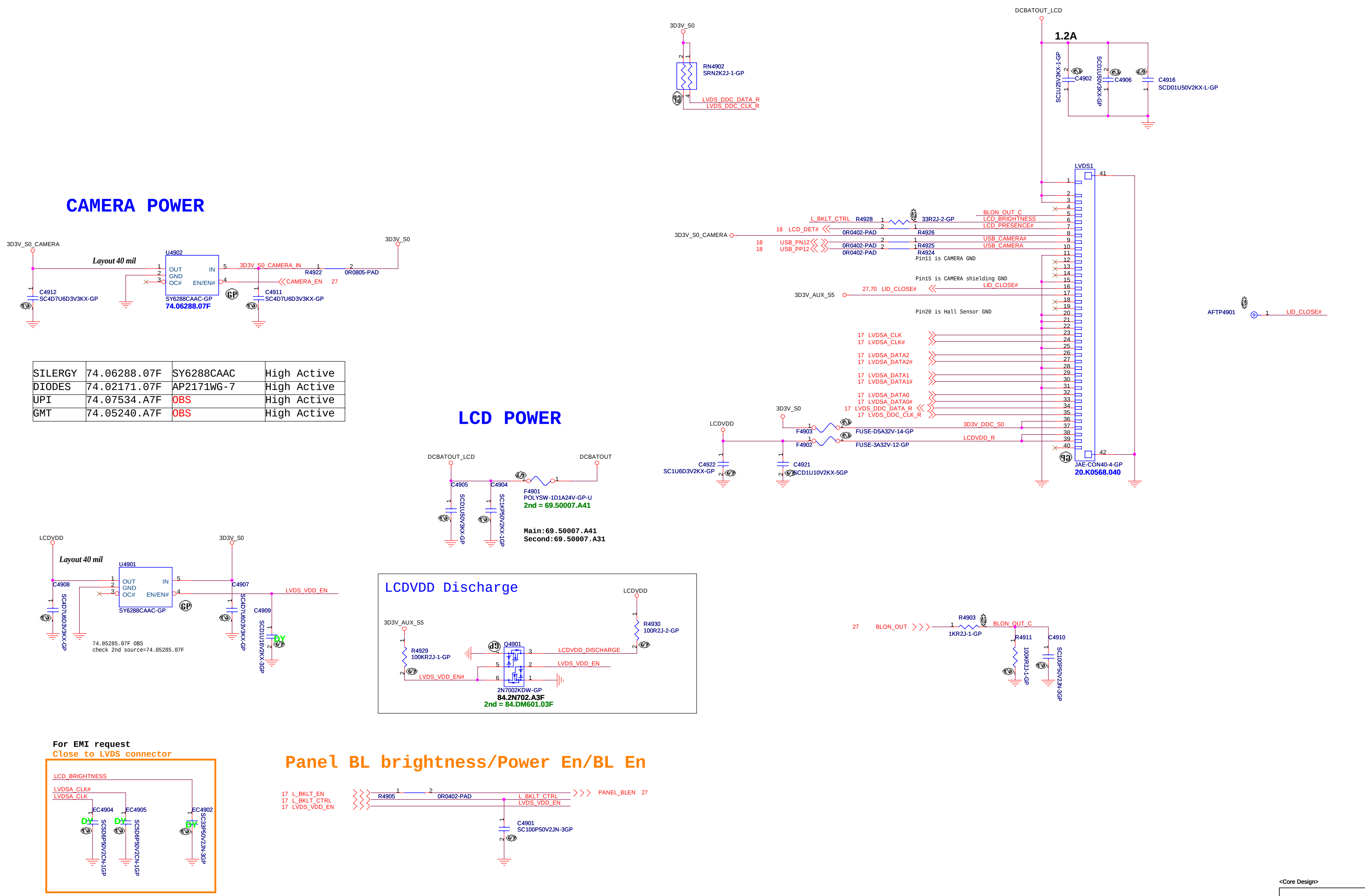
Size | Document Number: <Doc> | Rev: SD

Date: Friday, January 06, 2012 | Sheet 48 of 103

SSID = VIDEO

LVDS connector

LCD / Inverter Connector



SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active
GMT	74.05240.A7F	OBS	High Active

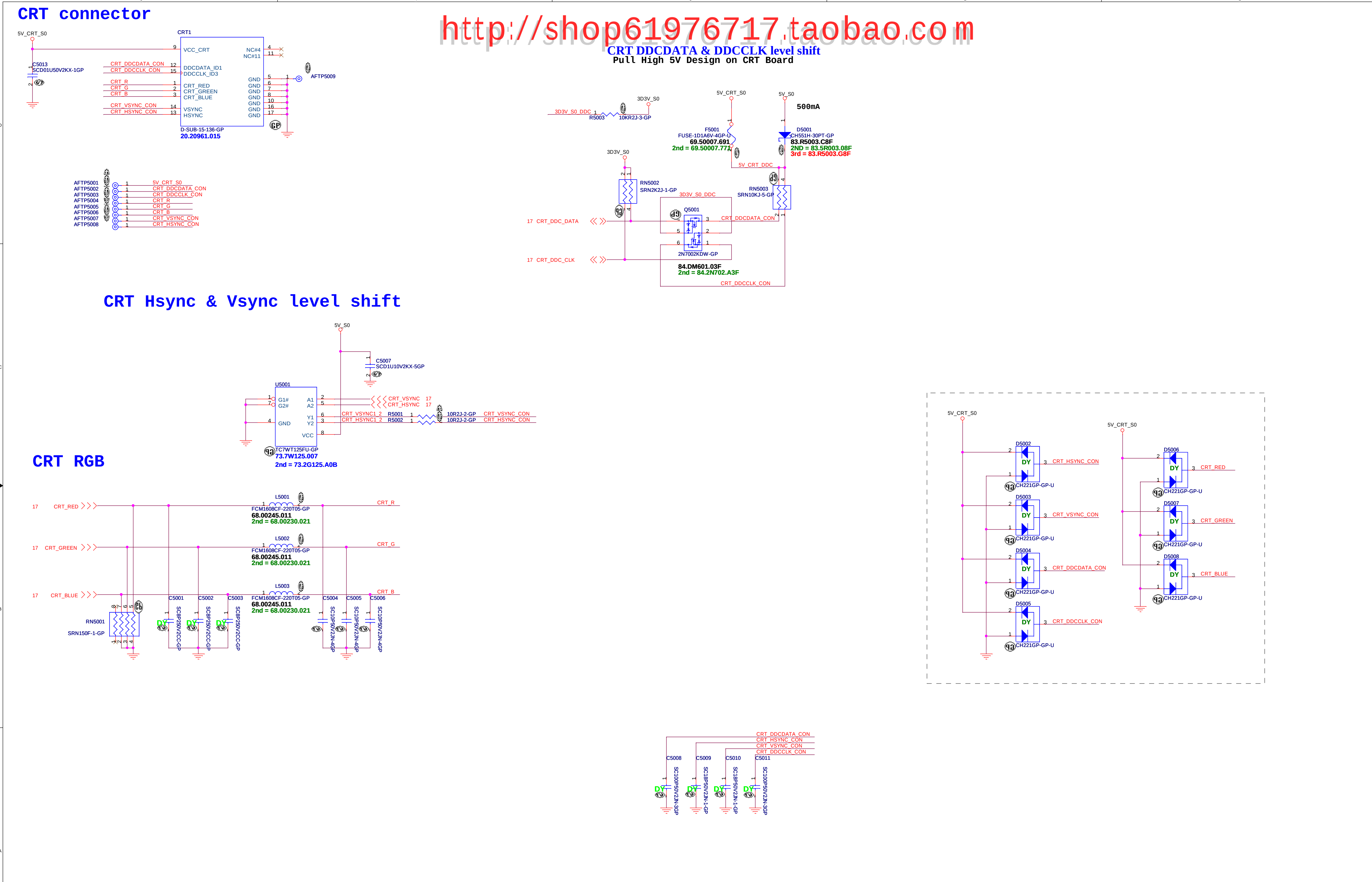
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

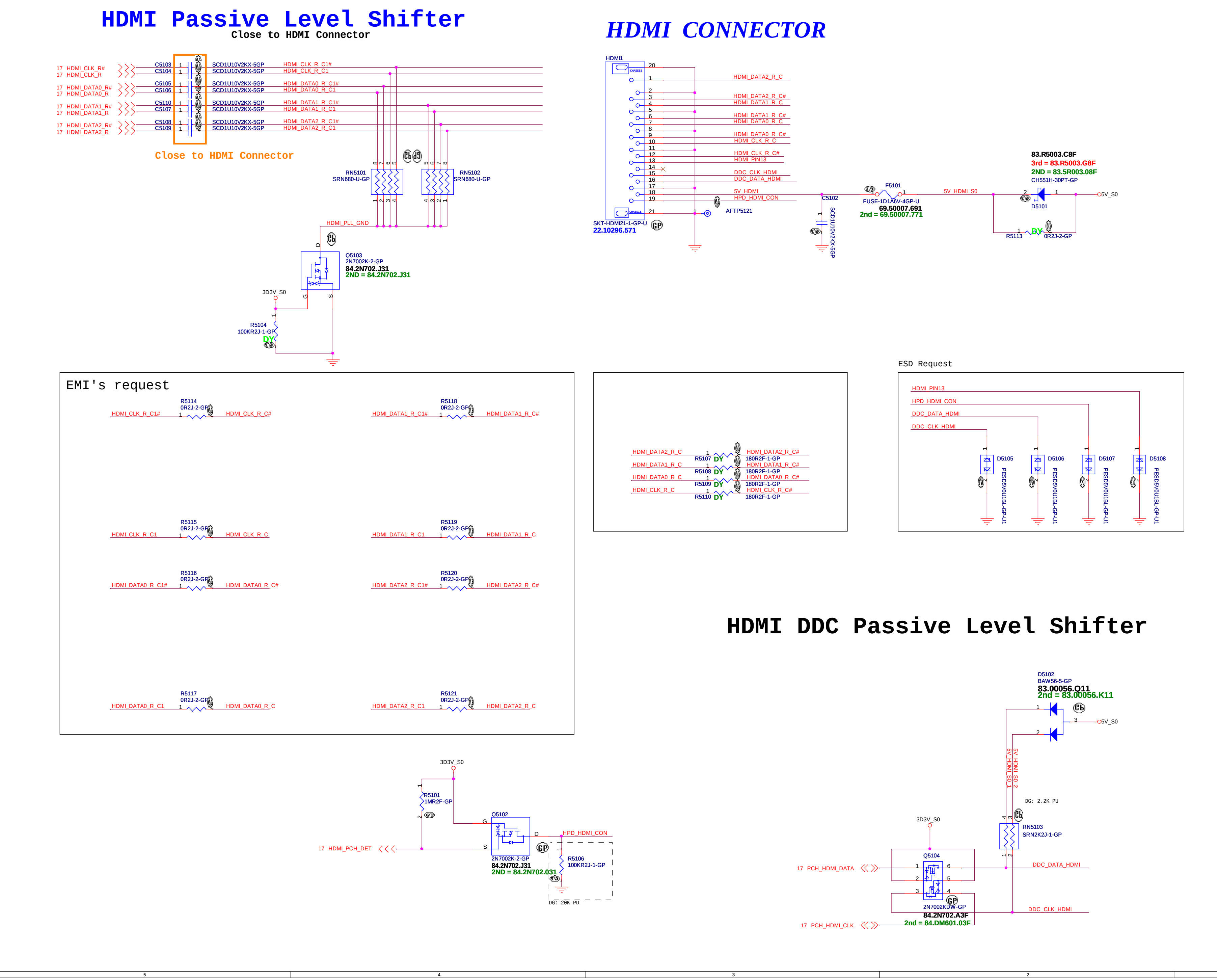
Title: **LCD Connector**

Size: A2 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 49 of 103


CRT connector
CRT1
VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
NC#4
NC#11
GND
D-SUB-15-136-GP
20.20961.015
5V_CRT_S0
C5013
SCD01U50V2KX-1GP
AFTP5009
AFTP5001
AFTP5002
AFTP5003
AFTP5004
AFTP5005
AFTP5006
AFTP5007
AFTP5008
CRT_DDCDATA_CON
CRT_DDCCLK_CON
CRT_R
CRT_G
CRT_B
CRT_VSYNC_CON
CRT_HSYNC_CON
CRT DDCDATA & DDCCLK level shift
Pull High 5V Design on CRT Board
3D3V_S0_DDC
R5003
10KR2J-3-GP
3D3V_S0
5V_CRT_S0
5V_S0
500mA
F5001
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771
D5001
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.08F
3rd = 83.R5003.G8F
5V_CRT_DDC
RN5002
SRN2K2J-1-GP
RN5003
SRN10KJ-5-GP
Q5001
2N7002KDW-GP
84.DM601.03F
2nd = 84.2N702.A3F
17 CRT_DDC_DATA
17 CRT_DDC_CLK
CRT Hsync & Vsync level shift
5V_S0
C5007
SCD1U10V2KX-5GP
U5001
G1#
G2#
GND
A1
A2
Y1
Y2
VCC
TC7WT125FU-GP
73.7W125.007
2nd = 73.2G125.A0B
CRT_VSYNC 17
CRT_HSYNC 17
CRT_VSYNC1_2
CRT_HSYNC1_2
R5001
R5002
10R2J-2-GP
CRT RGB
17 CRT_RED
17 CRT_GREEN
17 CRT_BLUE
L5001
L5002
L5003
FCM1608CF-220T05-GP
68.00245.011
2nd = 68.00230.021
RN5001
SRN150F-1-GP
C5001
C5002
C5003
C5004
C5005
C5006
SC8P250V2CC-GP
SC10P50V2JN-4GP
DY
D5002
D5003
D5004
D5005
D5006
D5007
D5008
CH221GP-GP-U
CRT_HSYNC_CON
CRT_VSYNC_CON
CRT_DDCDATA_CON
CRT_DDCCLK_CON
CRT_RED
CRT_GREEN
CRT_BLUE
C5008
C5009
C5010
C5011
SC100P50V2JN-3GP
SC18P50V2JN-1-GP

SSID = VIDEO



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	HDMI Level Shifter/Connector	
Size A2	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 51 of 103	

5 4 3 2 1

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<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	eDP	
Size A4	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 52 of 103	

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **S-VIDEO**		
Size: A4	Document Number: **LA480**	Rev: **SD**
Date: Friday, January 06, 2012	Sheet 53 of 103	

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<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size: A4

Document Number: **LA480**

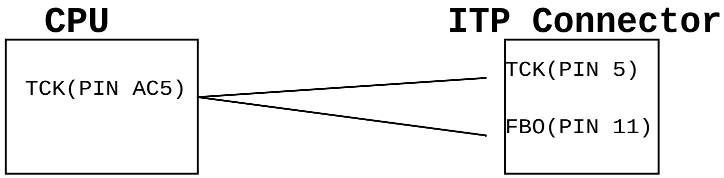
Rev: **SD**

Date: Friday, January 06, 2012

SSID = User.Interface

ITP Connector

**H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.**

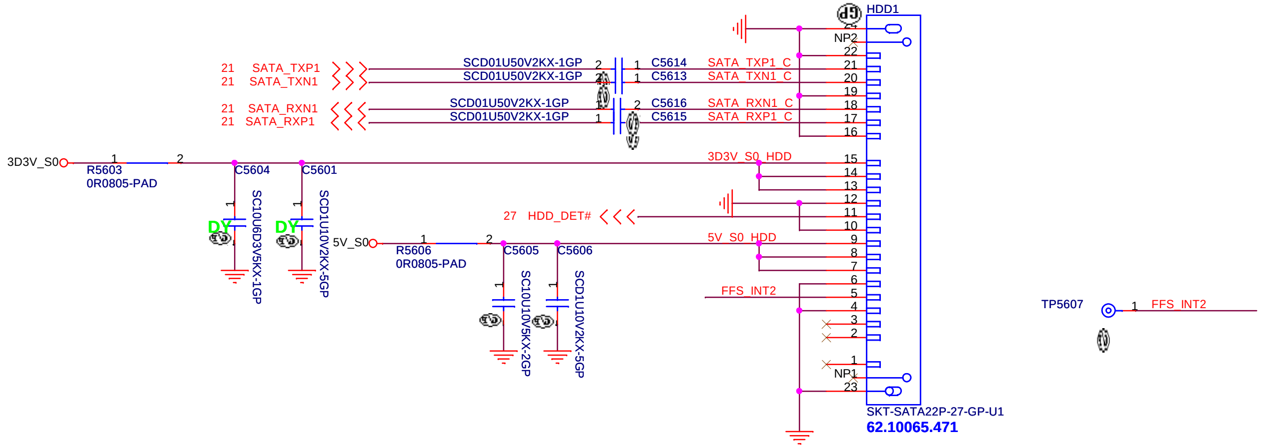


<Core Design>

緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ITP**		
Size: A4	Document Number: **LA480**	Rev: **SD**
Date: Friday, January 06, 2012	Sheet 55 of 103	

SATA HDD Connector



ODD Connector

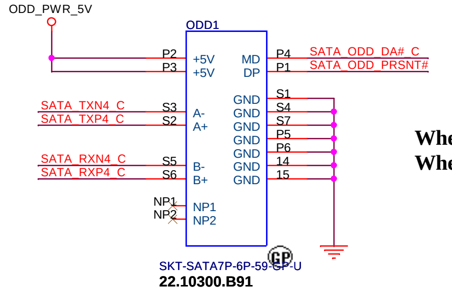
SATA_RX- and SATA_RX+ Trace Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.

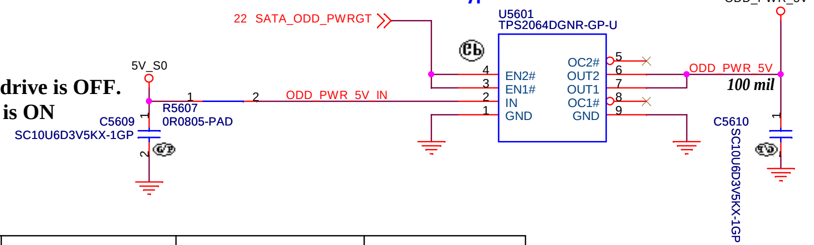
SATA Zero Power ODD

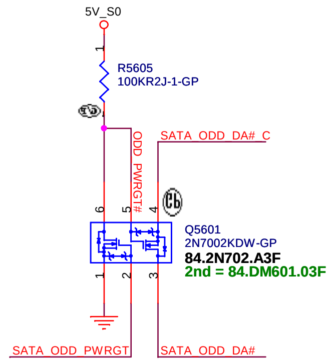
Current limit
Active High
typ =>2A

74.02069.079 TI TPS2069DGNR MSOP 8P
74.07534.D79 UPI UP7534PRA8-15 MSOP 8P
74.00547.C79 GMT G547F1P81U MSOP 8P (OBS)
74.07534.A79 UPI UP7534ARA8-15 MSOP8P

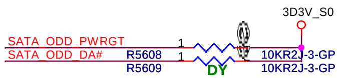


When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON





TI	74.02069.079	TPS2069DGNR	High Active
DIODES		AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active



SUPPORT ZERO SATA ODD

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	HDD/ODD	
Size A3	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 56 of 103	

5 4 3 2 1

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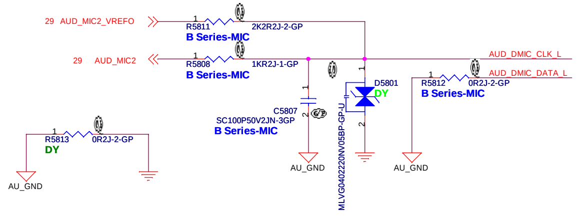
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***E-SATA+USB***
Size A4	Document Number **LA480** Rev **SD**
Date: Friday, January 06, 2012	Sheet 57 of 103

Int. Digital MIC for V series

Int. Mono Analog MIC for B series



INTERNAL STEREO SPEAKERS

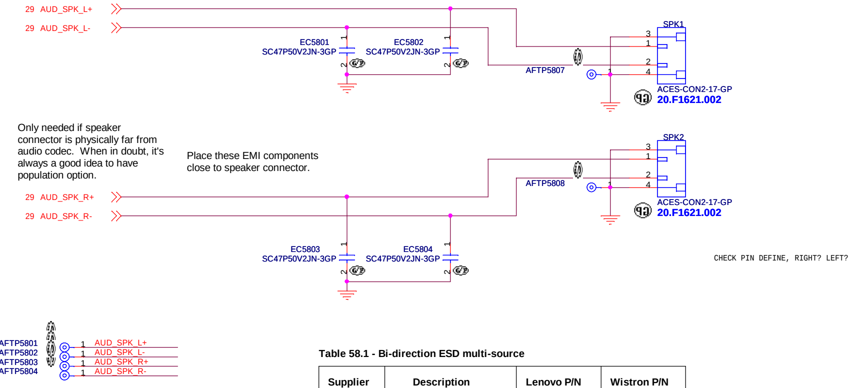


Table 58.1 - Bi-direction ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	RSB5.6SMT2R	N/A	83.RSB56.BAF
ON SEMI	ESD5B5.0ST1G	N/A	83.ESD5B.0AF
NXP	PESD5V0S1BB	N/A	83.0005V.0AF

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Jack**

Size: A2 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 58 of 103

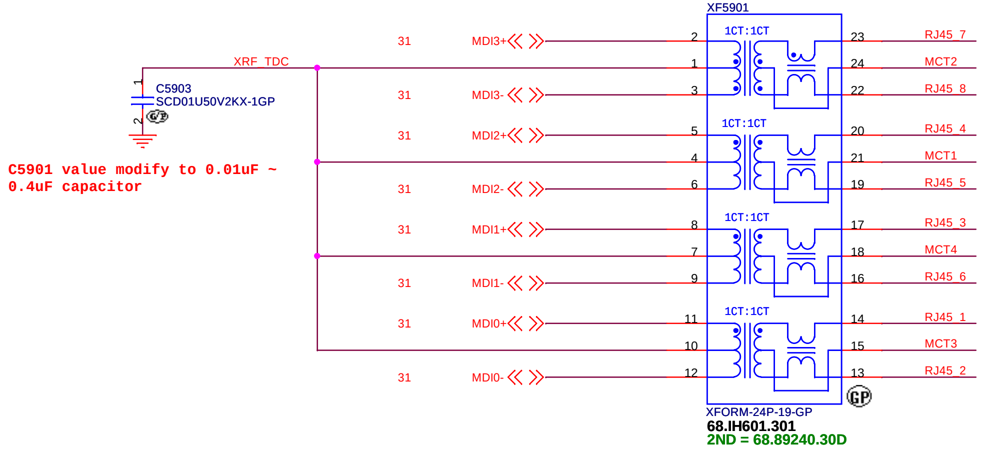
FOR CO-LAY

GIGA Lan Transformer

TVS
83.00005.BAE
DIODE ARR SRV05-4.TCT SOT-23-6

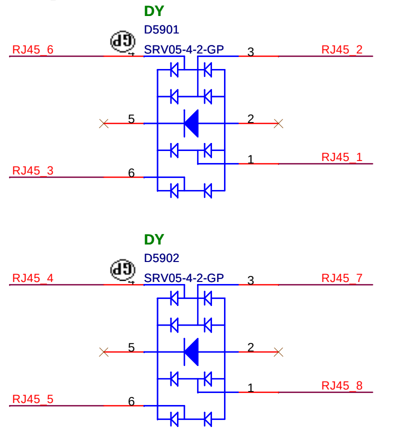
83.09904.AAE
DIODE ESD AZC099-04S SOT23-6L

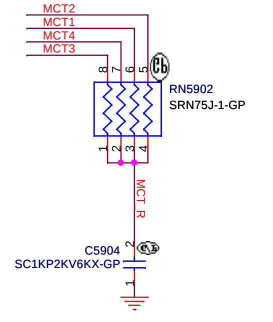
C5901 value modify to 0.01uF ~ 0.4uF capacitor



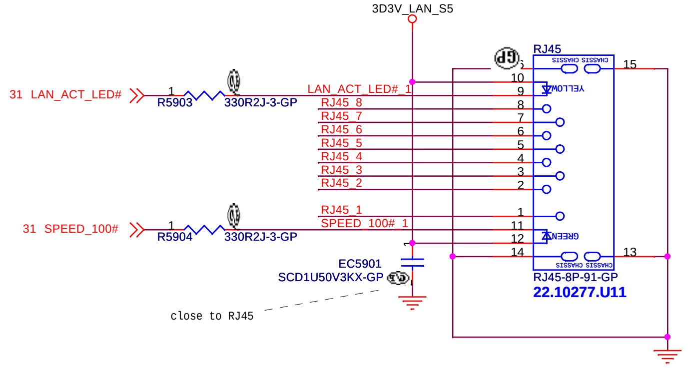
1st
68.IH601.301(Taimag) for 1000
68.HH035.301(Taimag) for 10/100
2nd
68.2413S.30A(Lankom) for 1000
68.H6441.301(Lankom) for 10/100

Swap for V480





LAN Connector



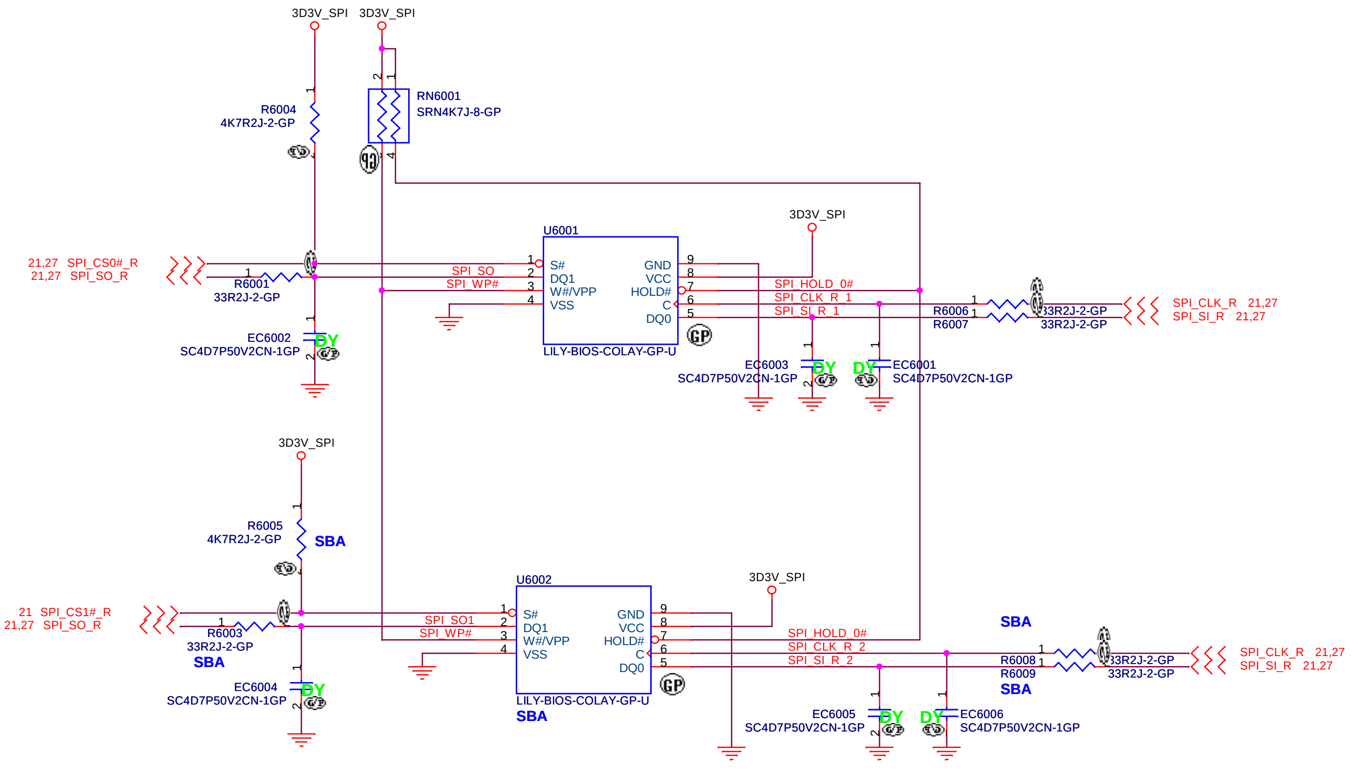
<Core Design>

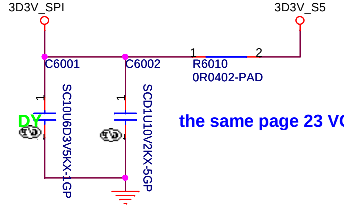
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	RJ45 / Transformer	
Size A3	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 59 of 103	

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

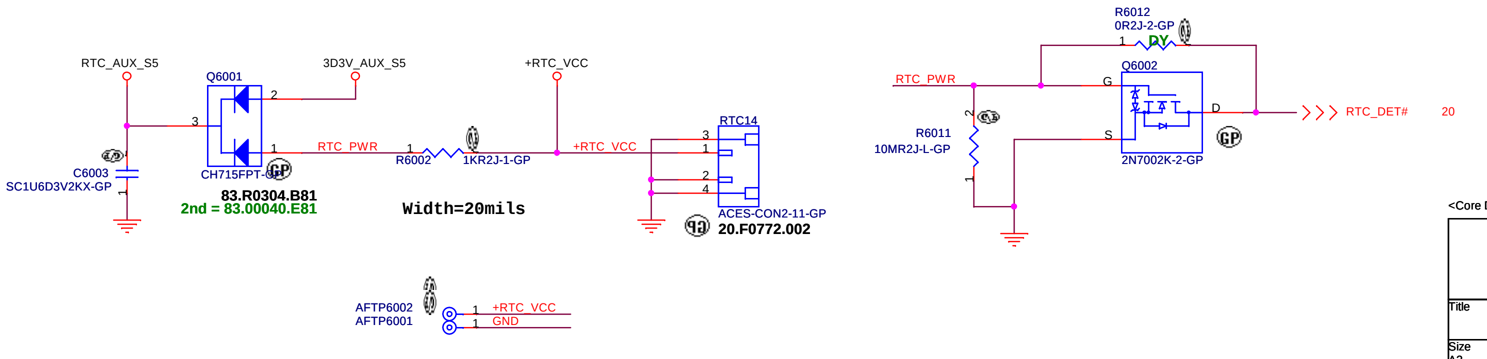




the same page 23 VCCSPI power

4MB			
SO8	Marcronix	MX25L3206EM2I-12G	72.25320.C01
	Winbond	W25Q032BVSSIG	72.25Q32.A01
	Numonyx	N25Q032A13ESE40	72.25032.H01
8MB			
SO8	Marcronix	MX25L6406EM2I-12G	72.25640.D01
	Winbond	W25Q064CVSSIG	72.25Q64.B01
	Numonyx	N25Q064A13ESE40	72.25Q64.D01
16MB			
WSON	Marcronix	MX25L12836EZNI-10G	72.25128.X01
		MX25L12835EZNI-10G	72.25128.Y01
	Winbond	W25Q128BVEIG	72.25128.I01
	Numonyx	N25Q128A13EF840	72.25128.B03

SSID = RBATT



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

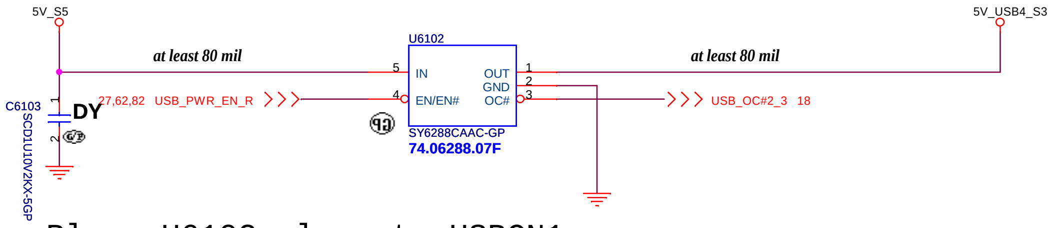
Title: Flash/RTC

Size: A3 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 60 of 103

USB Board CONN.

Support 2A

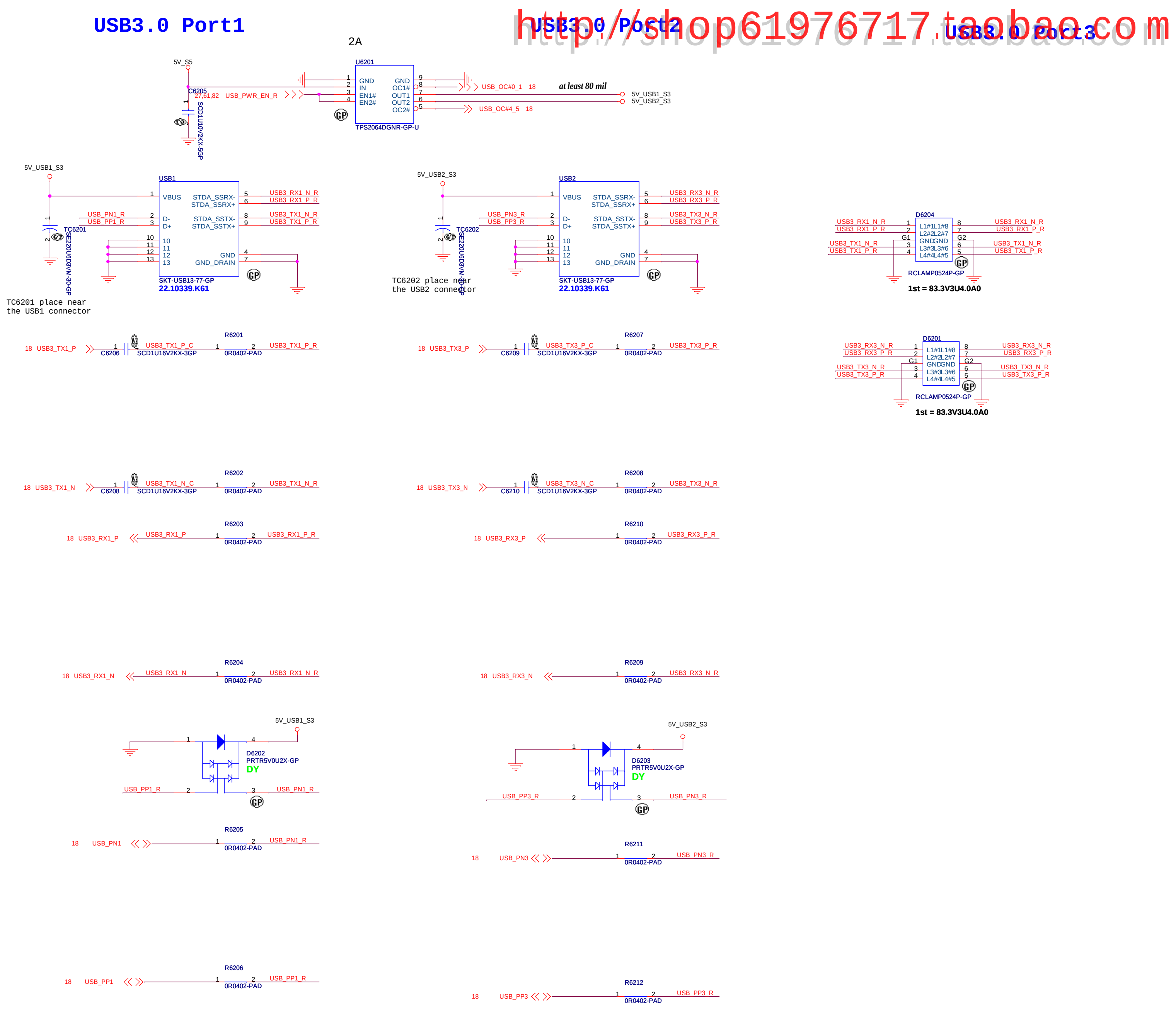


Place U6102 close to USBCN1

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB Connector		
Size A3	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 61 of 103	



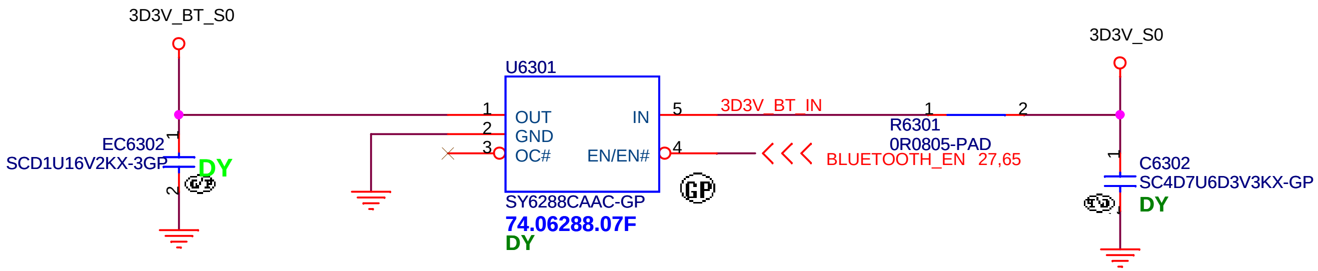
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB 3.0 Port*2	
Size A2	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 62 of 103	

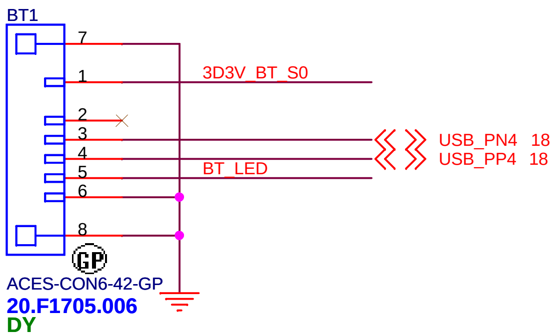
SSID = User.Interface

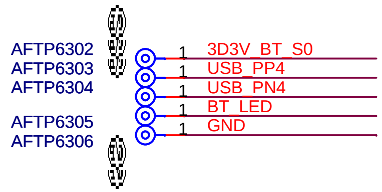
Bluetooth conn.



SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active
GMT	74.05240.A7F	OBS	High Active

BT Module pin definition is same as LA470





<Core Design>

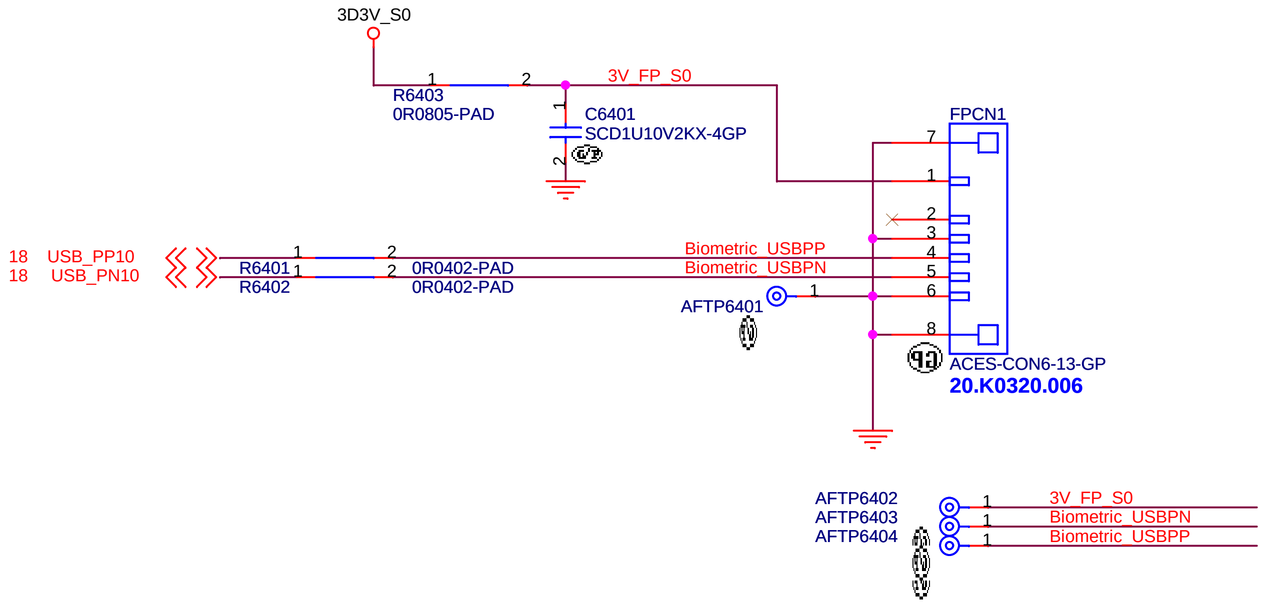
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Bluetooth**

Size: A4 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 63 of 103

Finger Printer Connector

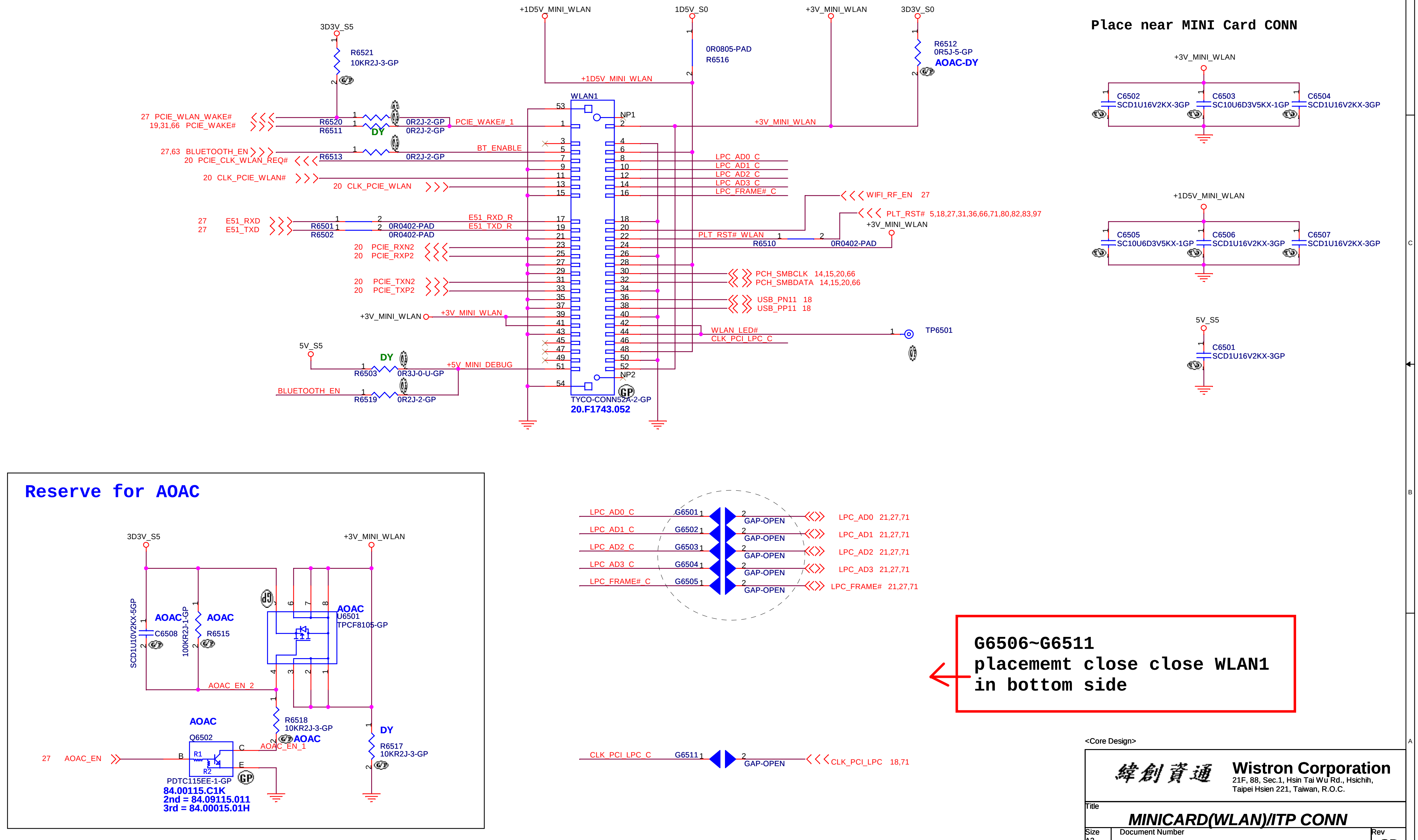


<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Finger Printer Connector***	
Size A4	Document Number **LA480**	Rev **SD**
Date: Friday, January 06, 2012	Sheet 64 of 103	

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

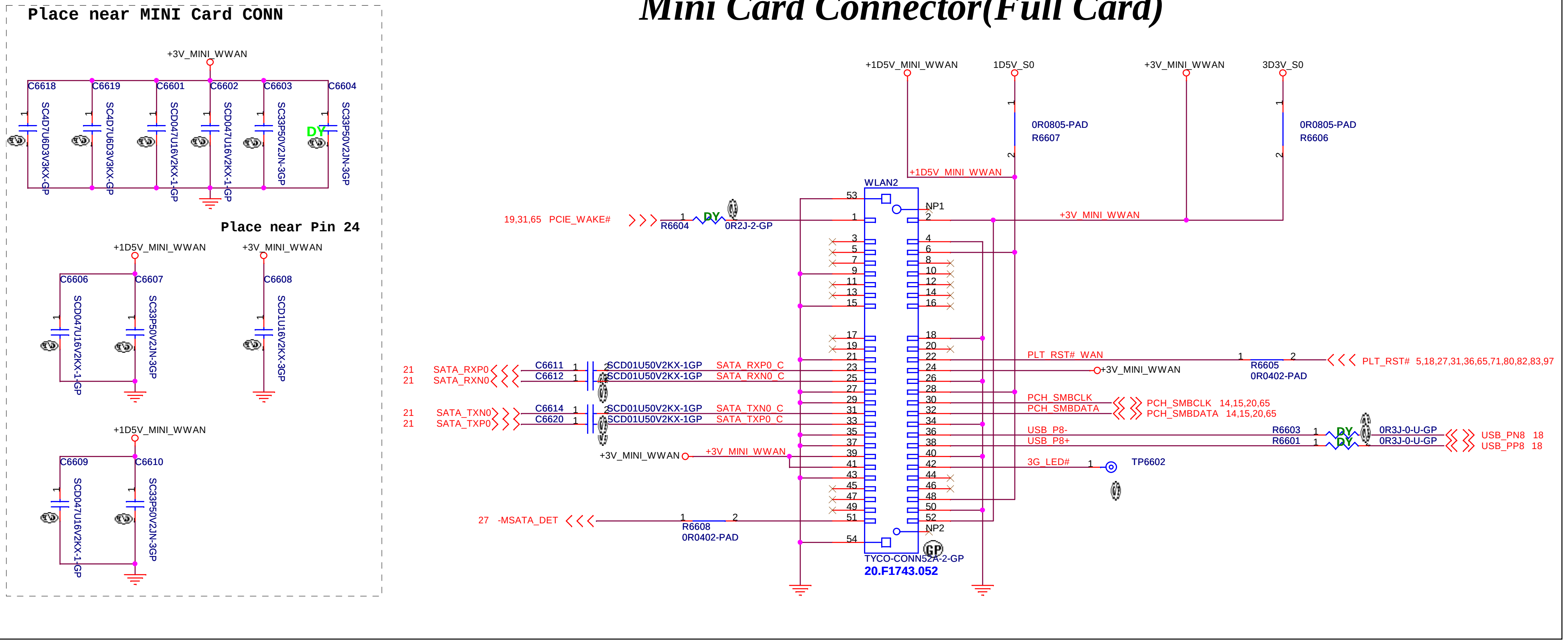
Size: A3 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 65 of 103

SSID = Wireless

mSATA for V Series Only

Mini Card Connector(Full Card)



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: WWAN Connector
Size: A3 | Document Number: LA480 | Rev: SD
Date: Friday, January 06, 2012 | Sheet 66 of 103

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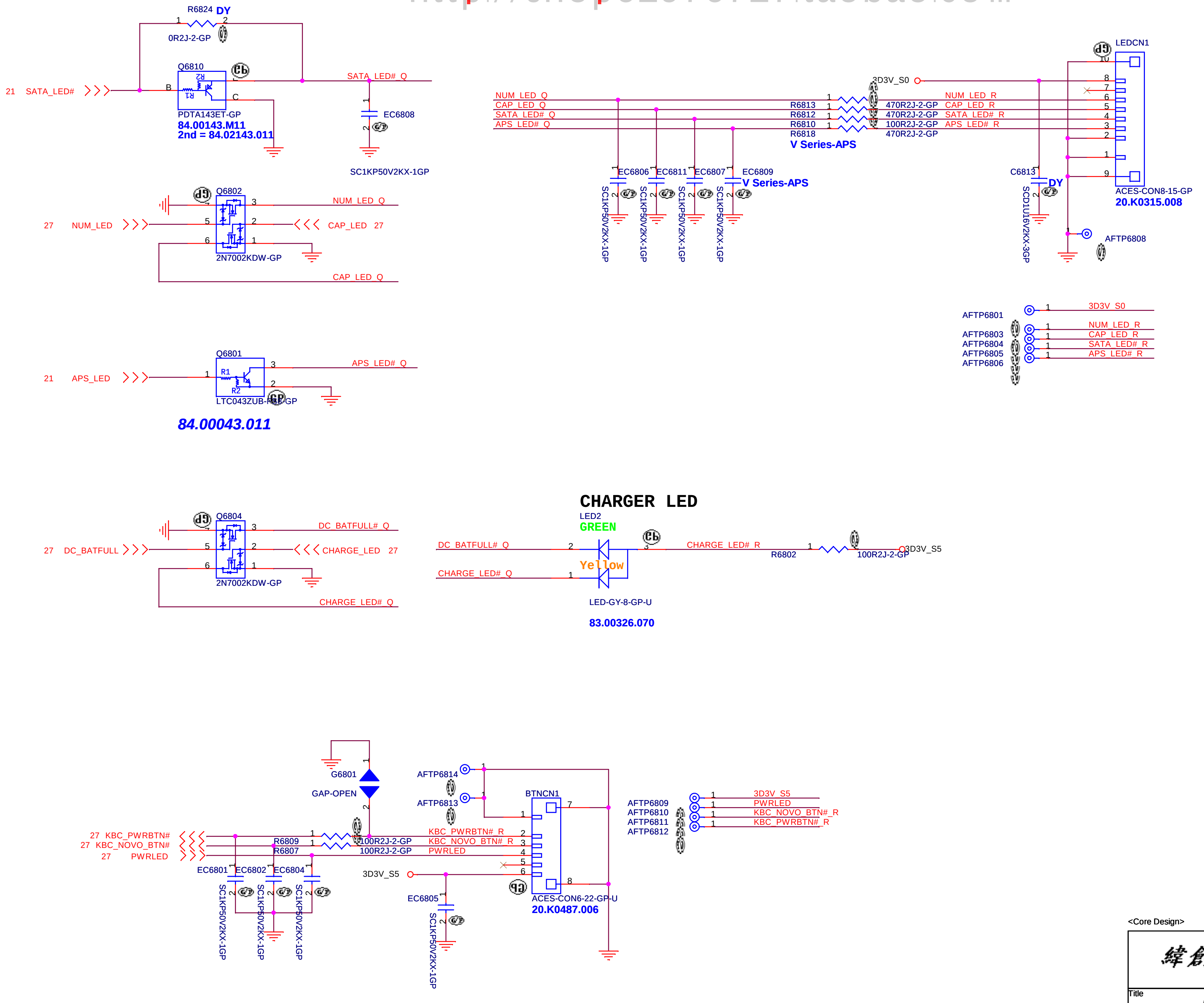
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Reserved***	
Size A4	Document Number **LA480**	Rev **SD**
Date: Friday, January 06, 2012	Sheet 67 of 103	

SSID = User.Interface



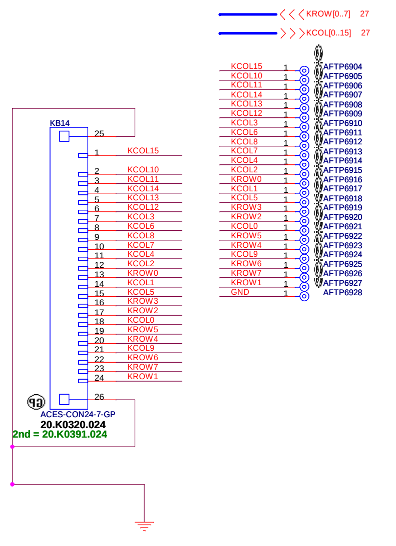
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
LED Bard/Power Button			
Size: A3	Document Number: LA480		Rev: SD
Date: Friday, January 06, 2012		Sheet 68 of 103	

SSID = KBC

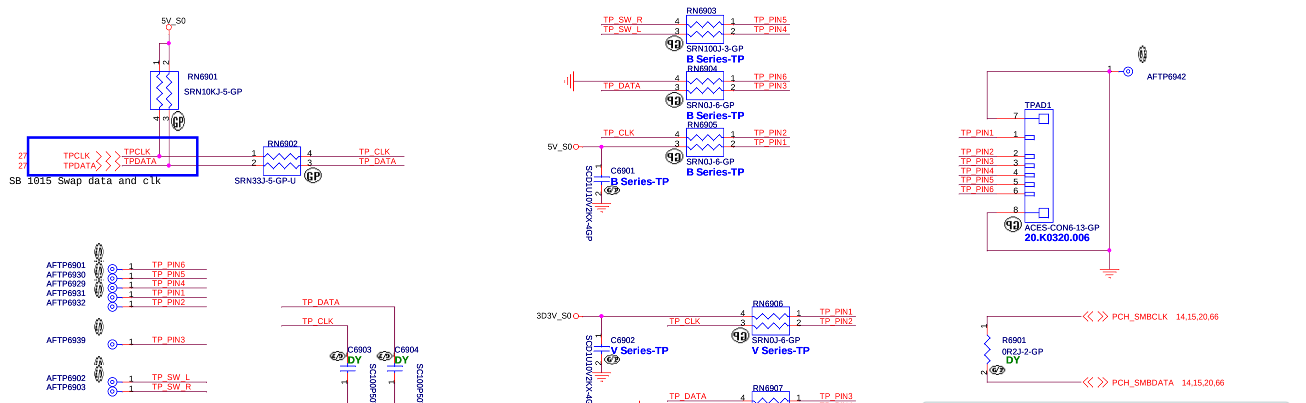
Internal KeyBoard Connector



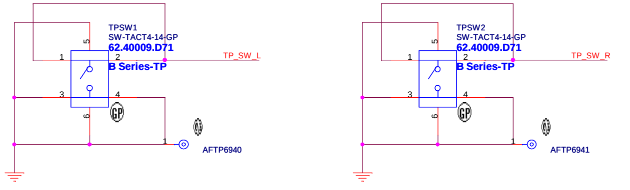
KB14 for 14" VB480 & VB485
KB15 for 15" VB580 & VB585

SSID = Touch Pad

Normal Pad for B Series 5V
ClickPad for V Series 3.3V



	Models			
Synaptics P/N	B480	V480	B580	V580
TM-01146-006	✓			
TM-02023-001		✓		
TM-02060-001			✓	
TM-02045-001				✓
VDD	5V	3.3V	5V	3.3V
Pin 1	VDD	VDD	VDD	VDD
Pin 2	CLK	CLK	CLK	CLK
Pin 3	DAT	DAT	DAT	DAT
Pin 4	Left button	GND	GND	GND
Pin 5	Right button	NC	Left button	NC
Pin 6	GND	NC	Right button	NC



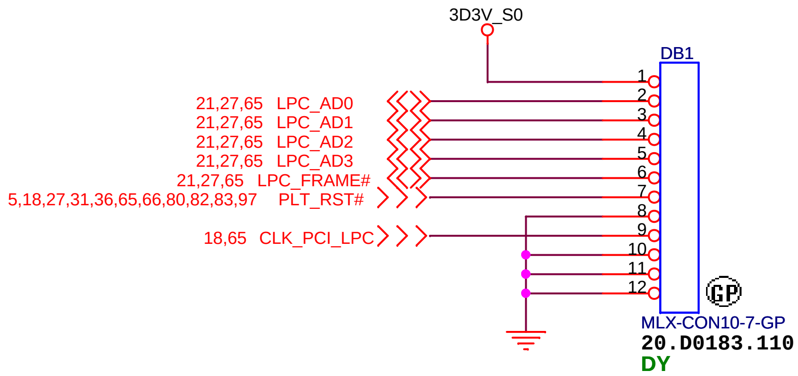
* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Hall Sensor*	
Size A4	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 70 of 103	



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Title	***Dubug connector***	
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Title	***Reserved***	
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Title	***Reserved***	
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Title

CARD Reader CONN

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A2	**LA480**	**SD**

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Title: New Card		
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Title	*Reserved*	
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Title: ***Reserved***		
Size: A4	Document Number: **LA480**	Rev: **SD**
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Title
Reserved

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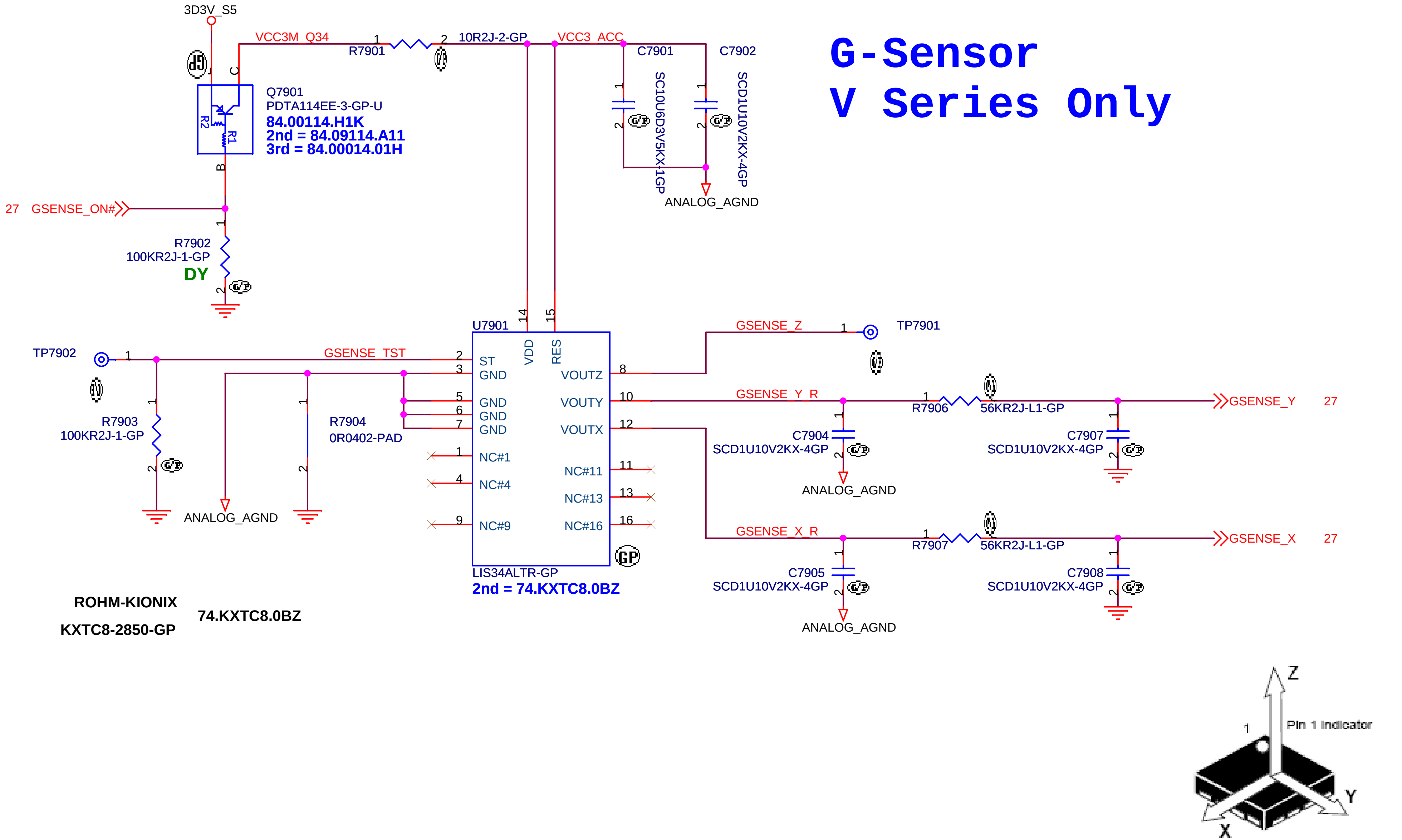
G-Sensor
V Series Only



Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.

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Title	**G-Sensor**
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RFID

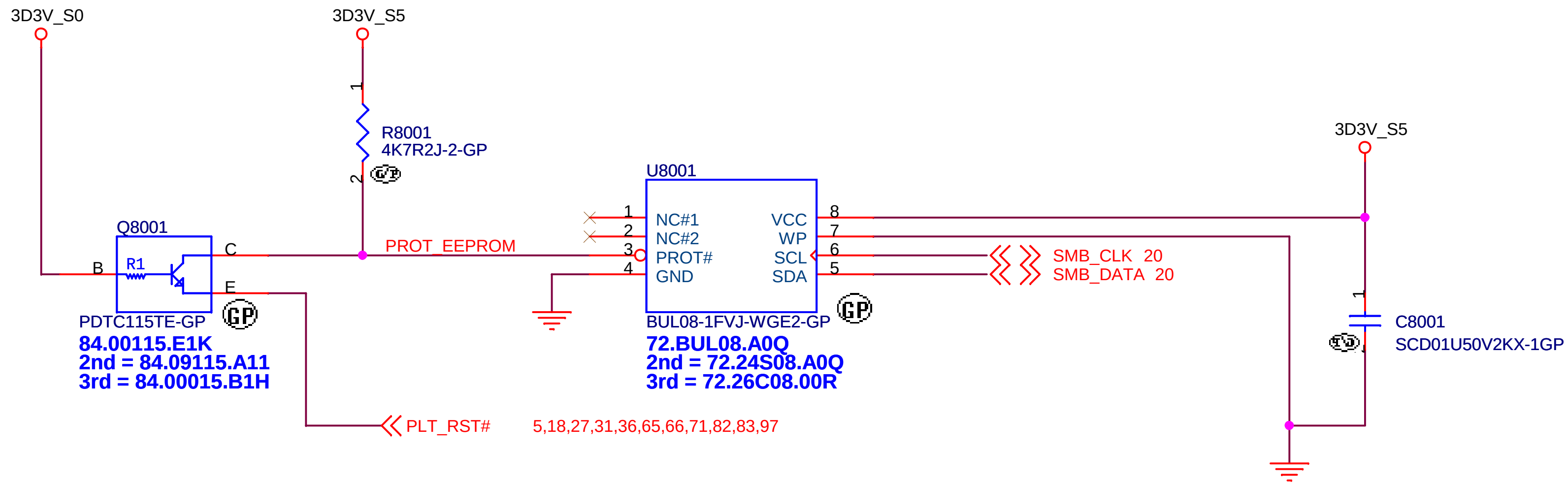

Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC115TE	N/A	84.00115.E1K
ROHM	LTC015TEB	N/A	84.00015.B1H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	N/A	72.BUL08.A0Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	N/A	72.26C08.00R

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Title: **RF ID**

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Title	***Reserved***
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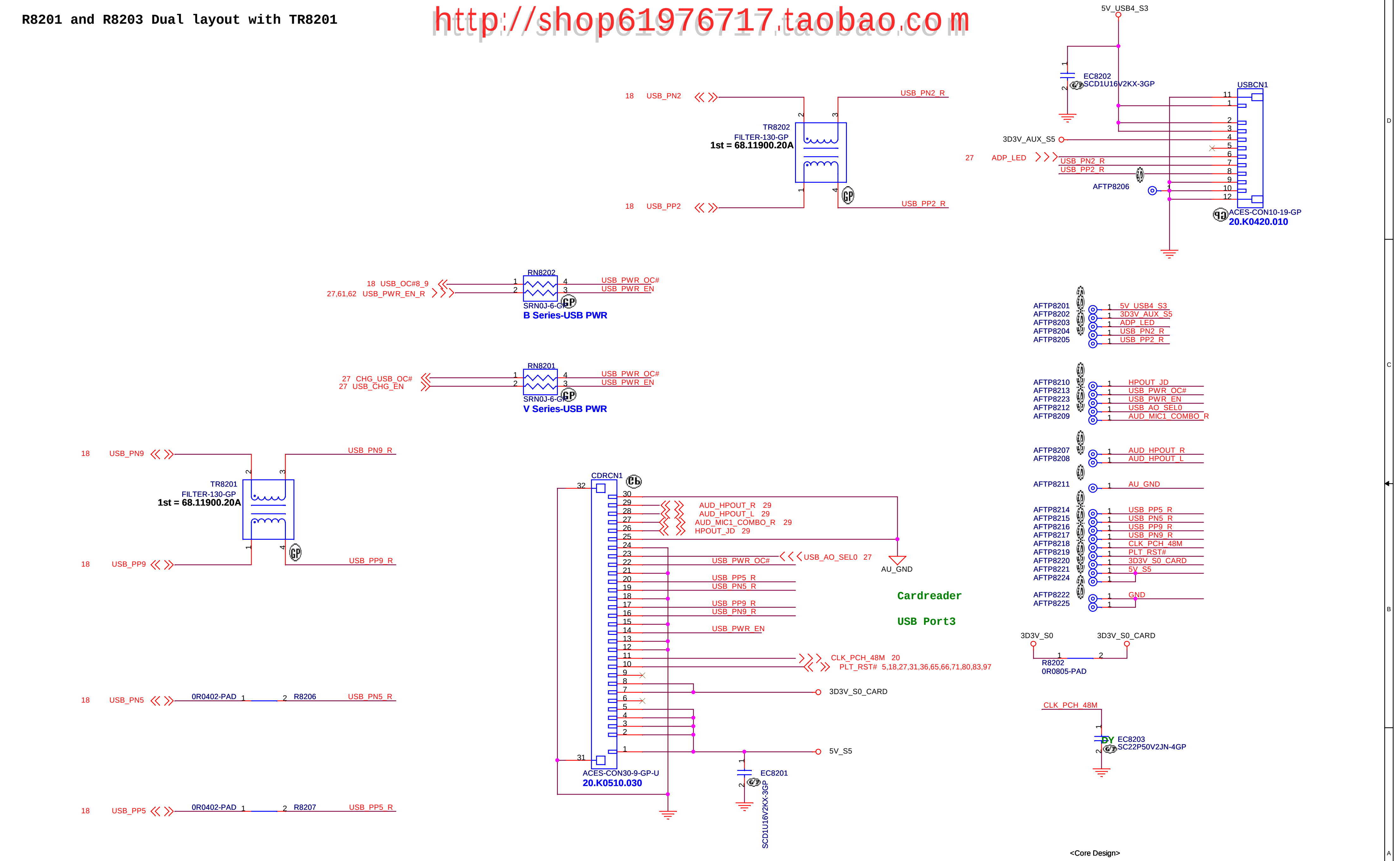
R8201 and R8203 Dual layout with TR8201



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Title	*IO Board Connector*	
Size A3	Document Number LA480	Rev SD
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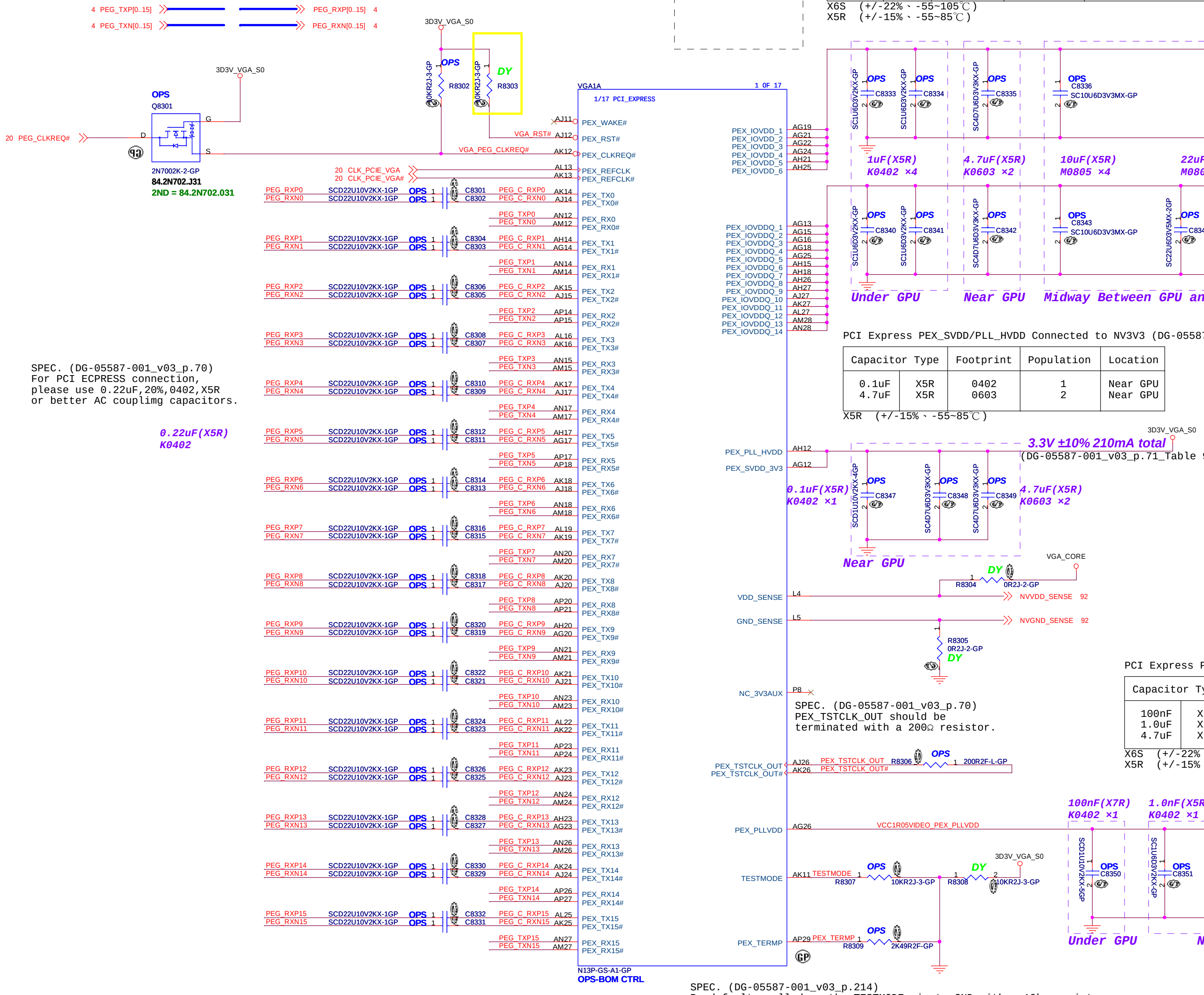
PCI Express PEX_IOVVD/Q Combined (DG-05587-001_v03_p.72_Table 10)

Capacitor	Type	Footprint	Population	Location
1.0uF	X6S	0402	4	Under GPU
4.7uF	X6S	0603	2	Near GPU
10uF	X5R	0805	4	Midway Between GPU and Power Supply
22uF	X5R	0805	4	Midway Between GPU and Power Supply

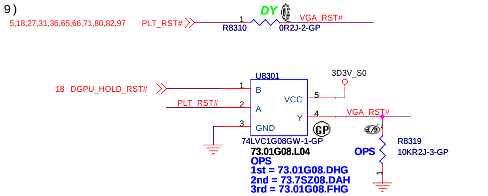
X6S (+/-22%、-55~105℃)
X5R (+/-15%、-55~85℃)

SPEC. (DG-05587-001_v03_p.70)
PEX_CLK_REQ_N is an open-drain bi-directional signal;
by default it should have a 10 kΩ pull-up to 3.3V.
This signal is an active low signal.

SPEC. (DG-05587-001_v03_p.70)
For PCI ECPRESS connection,
please use 0.22uF,20%,0402,X5R
or better AC couplimg capacitors.



dGPU reset



PCI Express PEX_SVDD/PLL_HVDD Connected to NV3V3 (DG-05587-001_v03_p.72_Table 12)

Capacitor	Type	Footprint	Population	Location
0.1uF	X5R	0402	1	Near GPU
4.7uF	X5R	0603	2	Near GPU

X5R (+/-15%、-55~85℃)

PCI Express PEX_PLLVDD (DG-05587-001_v03_p.72_Table 11)

Capacitor	Type	Footprint	Population	Location
100nF	X6S	0402	1	Under GPU
1.0uF	X5R	0603	1	Near GPU
4.7uF	X5R	0805	1	Near GPU

X6S (+/-22%、-55~105℃)
X5R (+/-15%、-55~85℃)

SPEC. (DG-05587-001_v03_p.70)
PEX_TSTCLK_OUT should be
terminated with a 200Ω resistor.

Stuff 0 ohm(63.00000.00L) for N13P-GS/N13M-GS,
Stuff bead(68.00082.001) for N13P-GL/N13M-GE

SPEC. (DG-05587-001_v03_p.214)
By default, pull-down the TESTMODE pin to GND with a 10kΩ resistor.
For XOR tree testing, TESTMODE should be pulled up to 3v3 with a 10 kΩ resistor.

SPEC. (DG-05587-001_v03_p.70)
PEX_TERMP is used for internal calibration;
pull-down this signal with 2.49 kΩ,1% resistor.

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Title	N13P_GPU (1/5): PEG	
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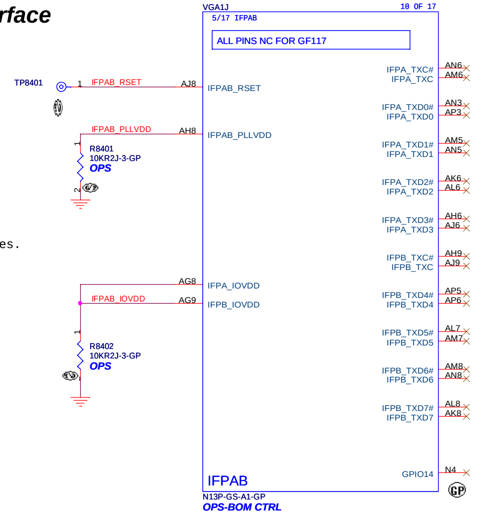
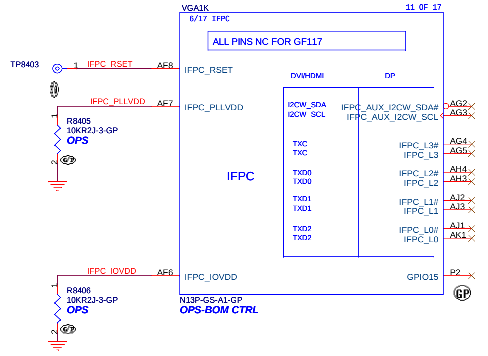
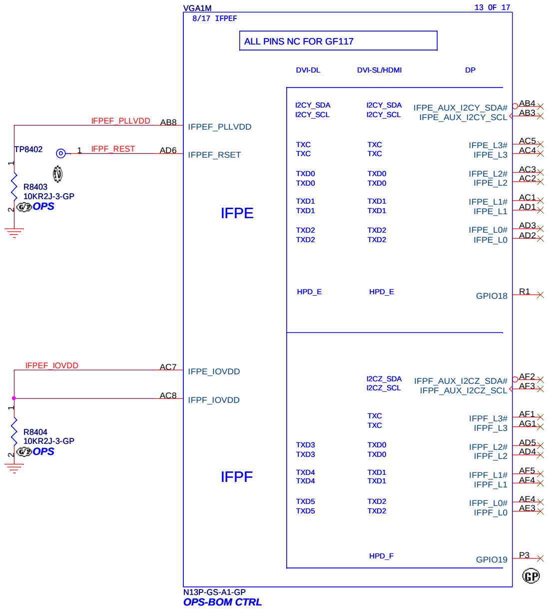
LVDS Interface

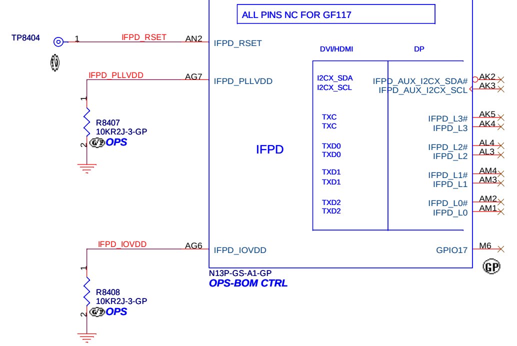
SPEC. (DG-05587-001_v03_p.160)
Pull down IFPxy IOVDD with 10kΩ resistor.
Pull down IFPxy PLLVDD with 10kΩ resistor.
The other IO pins can be NC, this includes unused data lines.







HDMI Interface



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Title	N13P_GPU (2/5): DIGITALOUT	
Size A2	Document Number LA48	Rev SD
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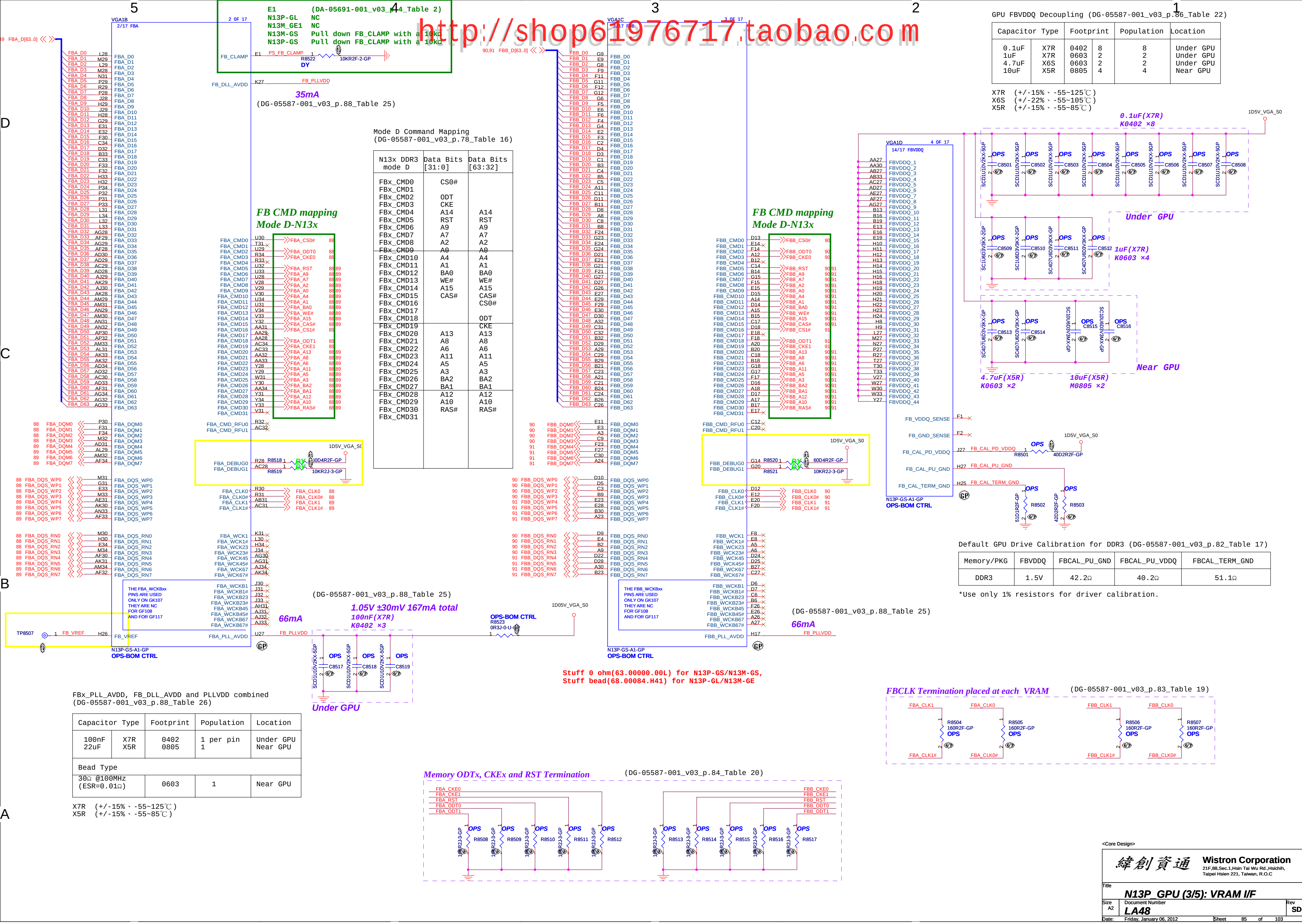

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GPU FBVDDQ Decoupling (DG-05587-001_v03_p.86_Table 22)

Capacitor	Type	Footprint		Population	Location
0.1uF	X7R	0402	8	8	Under GPU
1uF	X7R	0603	2	2	Under GPU
4.7uF	X6S	0603	2	2	Under GPU
10uF	X5R	0805	4	4	Near GPU

X7R (+/-15%、-55~125℃)
X6S (+/-22%、-55~105℃)
X5R (+/-15%、-55~85℃)

Mode D Command Mapping
(DG-05587-001_v03_p.78_Table 16)

N13x DDR3 mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#
FBx_CMD31		

Default GPU Drive Calibration for DDR3 (DG-05587-001_v03_p.82_Table 17)

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PU_VDDQ	FBCAL_TERM_GND
DDR3	1.5V	42.2Ω	40.2Ω	51.1Ω

*Use only 1% resistors for driver calibration.

(DG-05587-001_v03_p.88_Table 25)

Stuff 0 ohm(63.00000.00L) for N13P-GS/N13M-GS,
Stuff bead(68.00084.H41) for N13P-GL/N13M-GE

FBx_PLL_AVDD, FB_DLL_AVDD and PLLVDD combined
(DG-05587-001_v03_p.88_Table 26)

Capacitor	Type	Footprint	Population	Location
100nF	X7R	0402	1 per pin	Under GPU
22uF	X5R	0805	1	Near GPU
Bead Type				
30Ω @100MHz (ESR=0.01Ω)		0603	1	Near GPU

X7R (+/-15%、-55~125℃)
X5R (+/-15%、-55~85℃)

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Title	N13P_GPU (3/5): VRAM I/F	
Size A2	Document Number LA48	Rev SD
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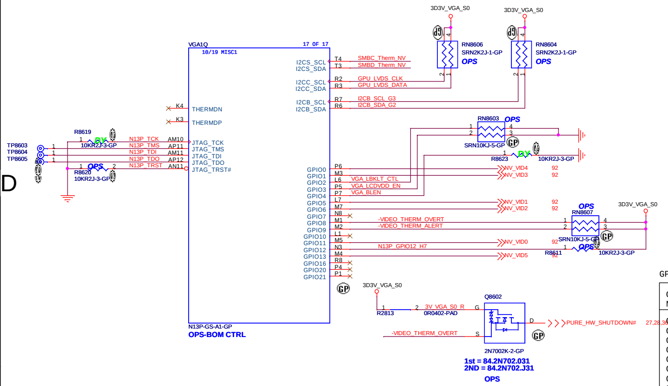
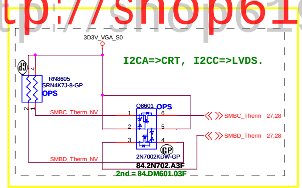
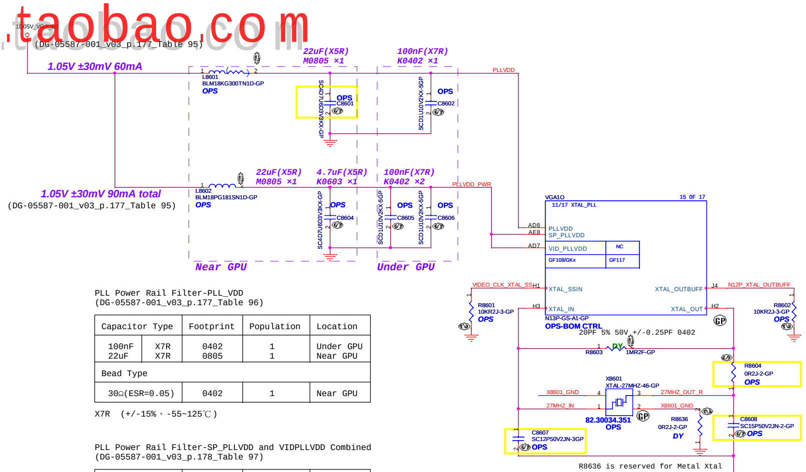




I2CA=>CRT, I2CC=>LVDS.

GPIO Description (DG-05587-001_v03_p.82_Tale 98)

GPIO pin Name	Normal Function	I/O	Function Description
GPIO0	GPU_VID4	O	GPU Core VDD VID4
GPIO1	GPU_VID3	O	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC	O	Panel Power Enable
GPIO4	LCD_BLEN	O	panel Backlight Enale
GPIO5	GPU_VID1	O	GPU Core VDD VID1
GPIO6	GPU_VID2	O	GPU Core VDD VID2
GPIO7	3D Vision	O	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC Power Detect Input. High = AC, Low = Battery
GPIO13	GPU_VID5	O	GPU Core VDD VID5
GPIO14	HPD_AB	I	Hot Plog Detect for IFPAB
GPIO15	HPD_C	I	Hot Plog Detect for IFPC
GPIO16	MEM_VDD_CTL	O	Memory VDD VID
GPIO17	HPD_D	I	Hot Plog Detect for IFPD
GPIO18	HPD_E	I	Hot Plog Detect for IFPE
GPIO19	HPD_F	I	Hot Plog Detect for IFPF
GPIO20	Reserved		
GPIO21	Reserved		



PLL Power Rail Filter-PLL_VDD
(DG-05587-001_v03_p.177_Table 96)

Capacitor Type		Footprint	Population	Location
100nF 22uF	X7R X7R	0402 0805	1 1	Under GPU Near GPU
Bead Type				
30Ω(ESR=0.05)		0402	1	Near GPU

X7R (+/-15%、-55~125℃)

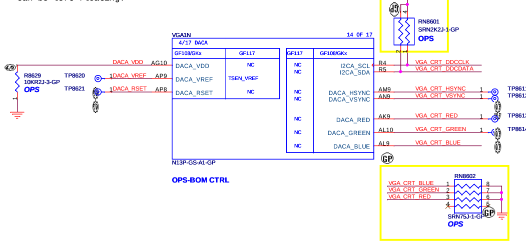
PLL Power Rail Filter-SP_PLLVDD and VIDPLLVDD Combined
(DG-05587-001_v03_p.178_Table 97)

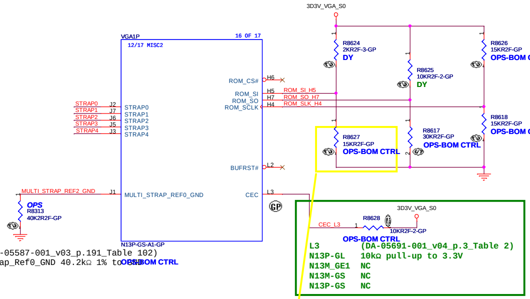
Capacitor Type		Footprint	Population	Location
100nF 4.7uF 22uF	X7R X7R X7R	0402 0402 0805	2 1 1	Under GPU Near GPU Near GPU
Bead Type				
180Ω(ESR=0.2)		0603	1	Near GPU

X7R (+/-15%、-55~125℃)

SPEC. (DG-05587-001_v03_p.176)
XTALOUTBUFF signal should be pull down using a 10kΩ resistor.
XTALSSIN signal should be pull down using a 10kΩ resistor.
REmember to place components as close ti the GPU as possible.

SPEC. (DG-05587-001_v03_p.162)
Adding a pull down to the DACA_VDD with a 10kΩ resistor to GND.
All other DAC I/O pins (including DACA_VREF, DACA_REST)
can be left floating.





SPEC. (DG-05587-001_v03_p.191_Table 102)
Multi_Strap_Ref0_GND 40.2kΩ 1% to GND.

L3 (DA-05691-001_v04_p.3_Table 2)
N13P-GL 10kΩ pull-up to 3.3V
N13M_GE1 NC
N13M-GS NC
N13P-GS NC

TABLE VIDEO MEMORY

	HYNIX 128Mx16 0110	SAMSUNG 128Mx16 0111	HYNIX 64Mx16 0010	Samsung 64Mx16 0011
900MHz	72.52G63.A0U 1-007155	72.42164.D0U 1-007156	72.51G63.H0U 1-007157	72.41164.Q0U 1-007356
ROM_SI PD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

The GB4-128 package is available in a 29 mm × 29mm footprint.
128-bit memory interfaces respectively.

Recommended NVVDD Voltage Regulator Phase Coount

GPU SKU	Phase Count Target
N13M-GE1 N13M-GS N13P-GL N13P-GS	Single phase Two phase Two phase Two phase

29 x 29 PACKAGE
V: N13P-GS/GL (25~30W)
B: N13M-GS/GE (15~20W)

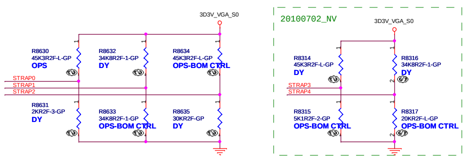
128Mx16:

hynix - H5TQ2G63BFR-11C
Samsung - K4W2G1646C-HC11

64Mx16:

Hynix - H5TQ1G63DFR-11C
Samsung - K4W1G1646G-BC11

	TABLE NVIDIA	N12P-GE DEV ID: 0xDF5 0101	N12P-GV DEV ID: 0x0DF7(ES)	N12M-GE DEV ID: 0xA7A 1010
STRAP1	R8632	DY	DY	35Kohm 64.34825.6DL
	R8633	35Kohm 64.34825.6DL	35Kohm 64.34825.6DL	DY
STRAP2	R8634	DY	45Kohm 64.45325.6DL	15Kohm 64.15025.6DL
	R8635	30Kohm 64.30025.6DL	DY	DY



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Title: N13P_GPU (4/5): GPIO/STRAP

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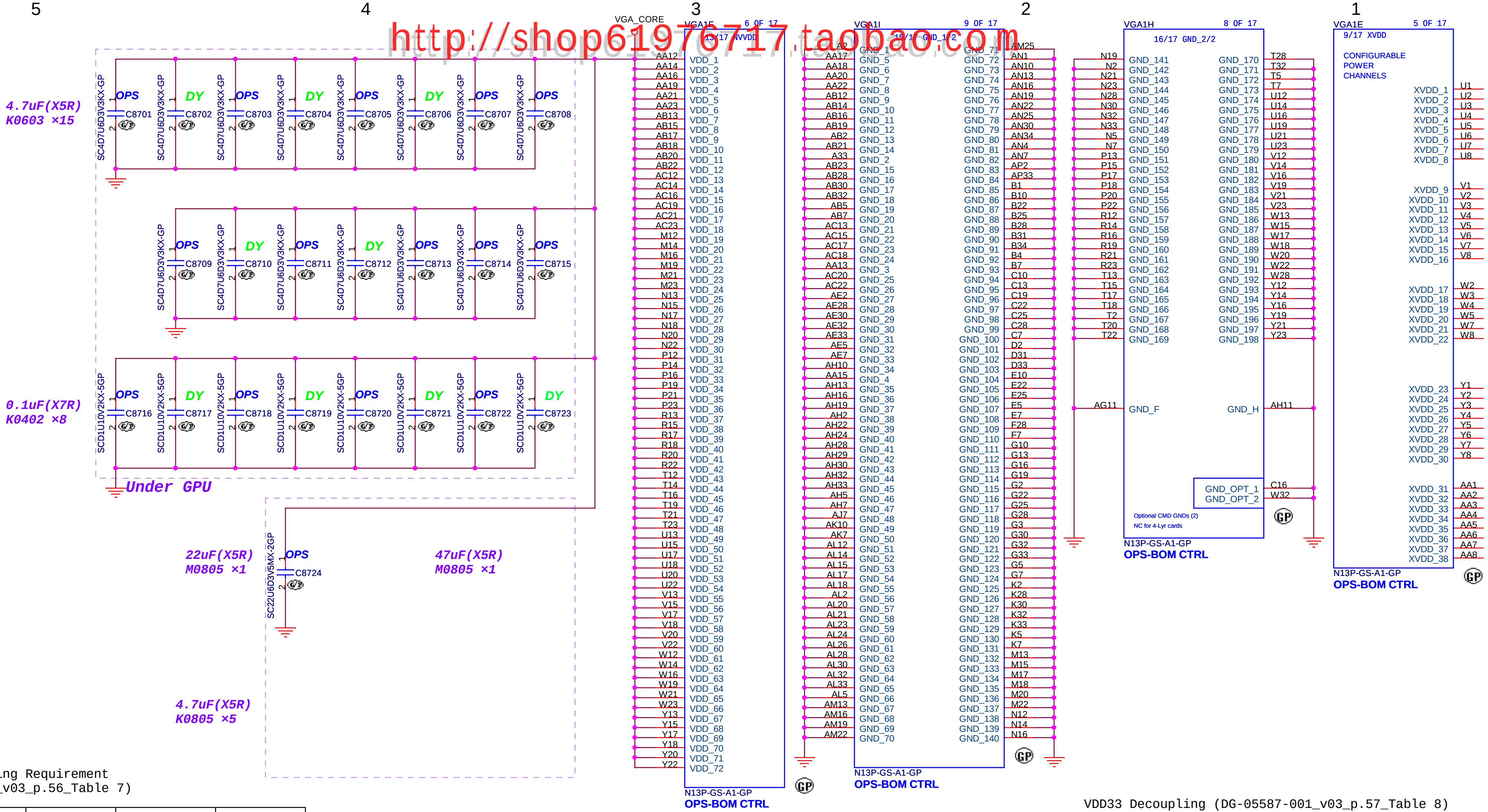
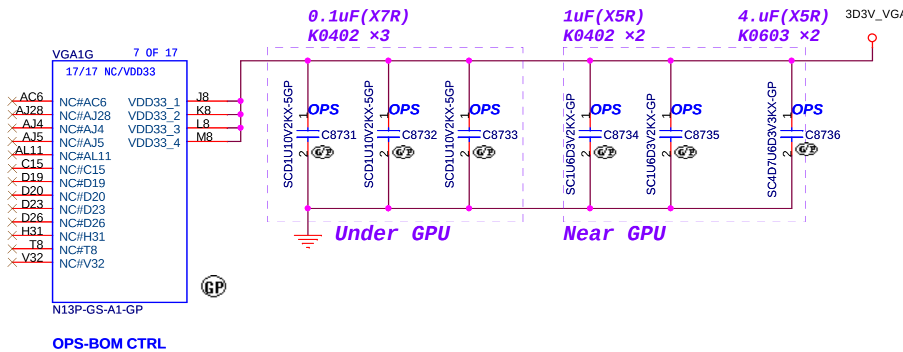


NVVDD Decoupling Requirement
(DG-05587-001_v03_p.56_Table 7)

Capacitor Type		Footprint		Population	Location
4.7uF	X6S	0603	15	10	Under GPU
0.1uF	X7R	0402	8	4	Under GPU
47uF	X5R	0805	1	1	Near GPU
22uF	X5R	0805	1	1	Near GPU
4.7uF	X5R	0805	5	5	Near GPU

X7R (+/-15%、-55~125℃)
X6S (+/-22%、-55~105℃)
X5R (+/-15%、-55~85℃)



VDD33 Decoupling (DG-05587-001_v03_p.57_Table 8)

Capacitor Type		Footprint		Population	Location
0.1uF	X7R	0402	3	3	Under GPU
1uF	X5R	0402	2	2	Near GPU
4.7uF	X5R	0603	1	1	Near GPU

X7R (+/-15%、-55~125℃)
X5R (+/-15%、-55~85℃)

<Core Design>

緯創資通 **Wistron Corporation**
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **N13P_GPU (5/5): PWR/GND**

Size: A3 | Document Number: **LA48** | Rev: SD

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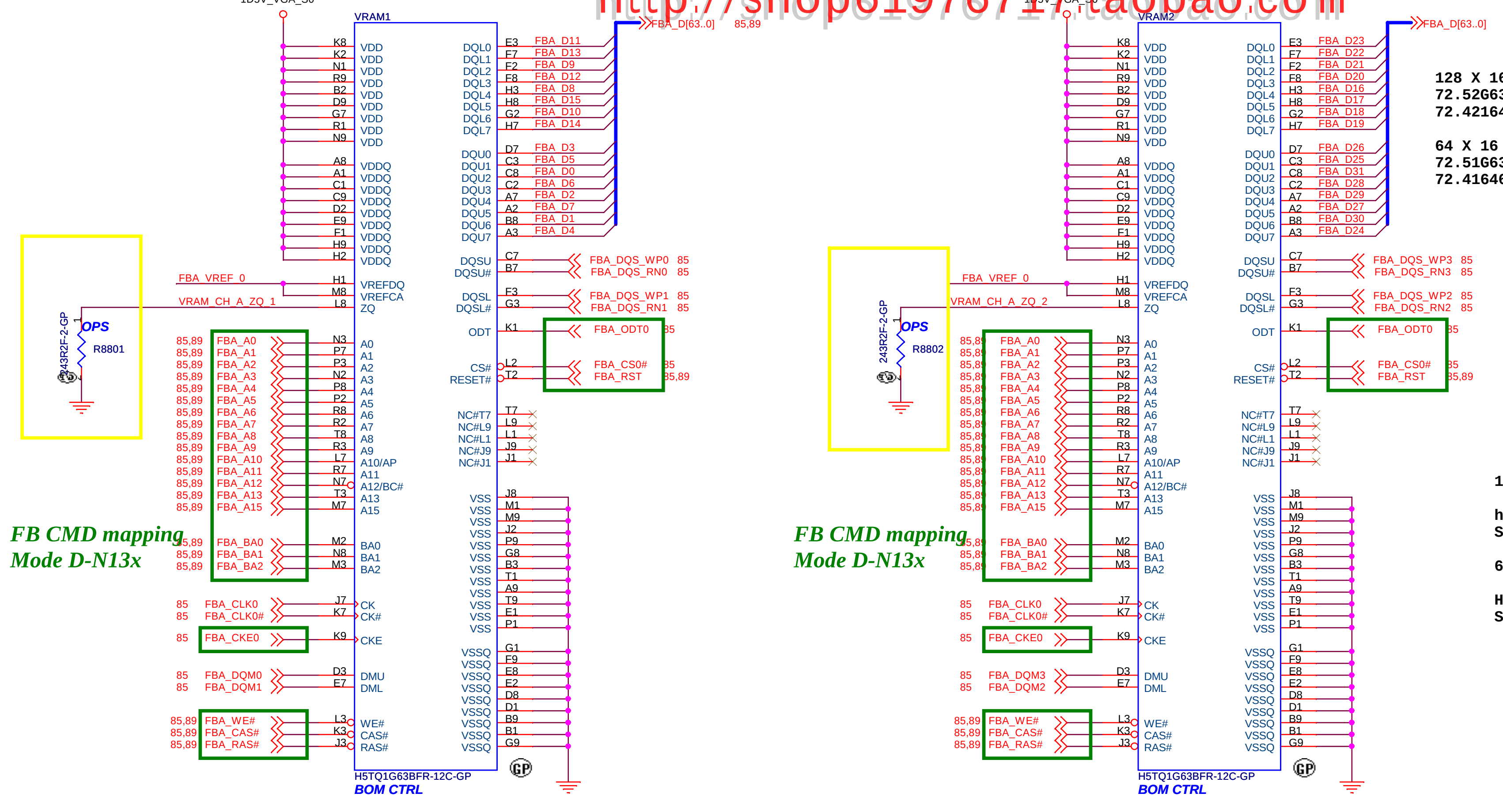
VIDEO FRAME BUFFER PORT A



128 X 16
72.52G63.A0U
72.42164.D0U IC VRAM K4W2G1646C-HC11 FBGA96

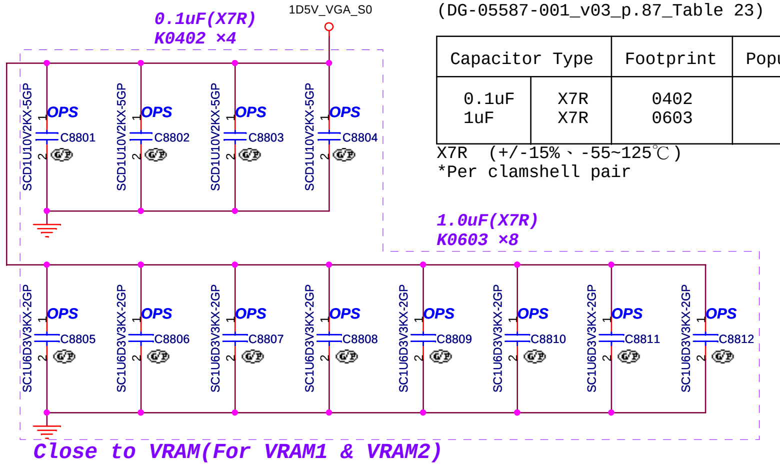
64 X 16
72.51G63.H0U IC VRAM H5TQ1G63DFR-11C FBGA 96BALLS
72.41646.Q0U IC VRAM K4W1G1646G-BC11 FBGA 96BALLS

128Mx16:

hynix - H5TQ2G63BFR-11C
Samsung - K4W2G1646C-HC11

64Mx16:

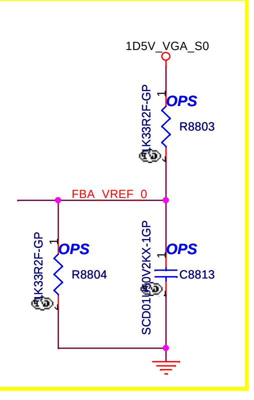
Hynix - H5TQ1G63DFR-11C
Samsung - K4W1G1646G-BC11



Combined Memory FBVDD/Q Decoupling DDR3×16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type		Footprint	Population	Location
0.1uF	X7R	0402	4	Close to VRAM
1uF	X7R	0603	8	Close to VRAM

X7R (+/-15%、-55~125℃)
*Per clamshell pair



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Title		
CHANNEL-A_VRAM1,2 (1/4)		
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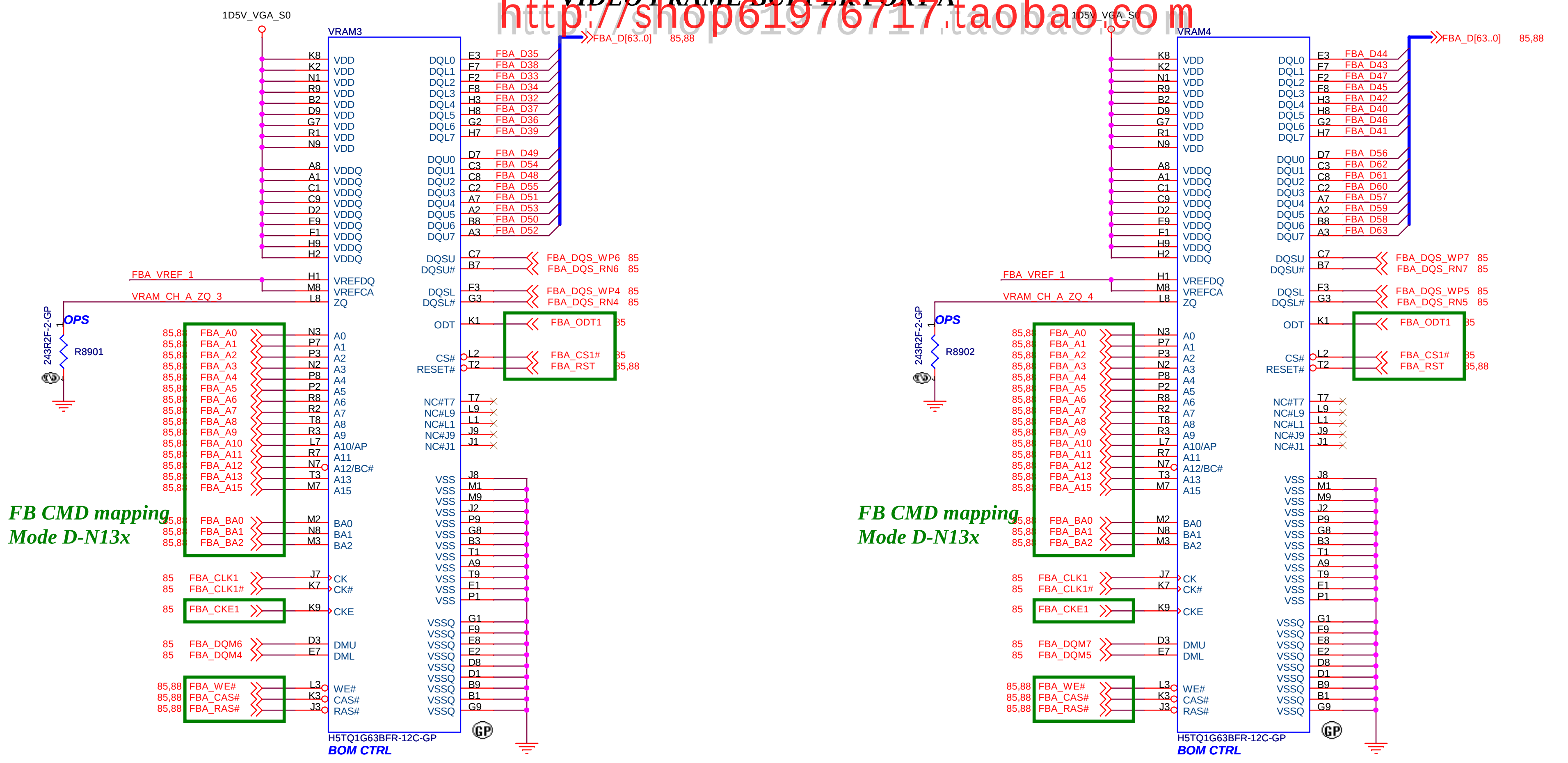
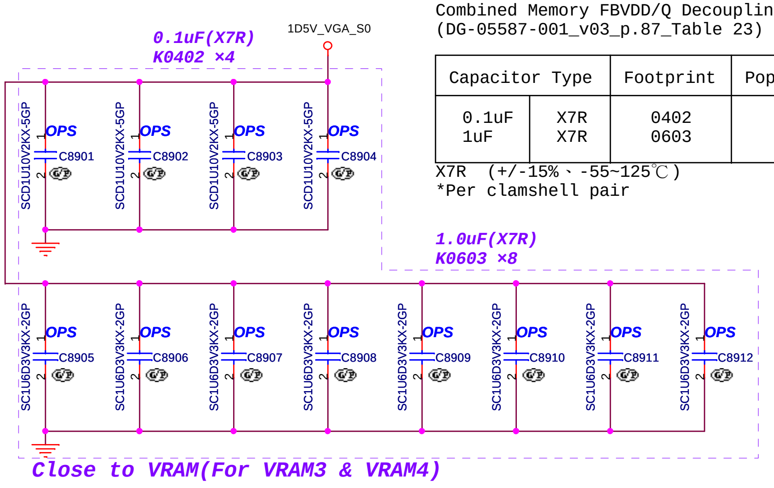
VIDEO FRAME BUFFER PORT A

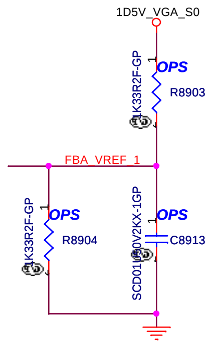


Combined Memory FBVDD/Q Decoupling DDR3×16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type		Footprint	Population	Location
0.1uF	X7R	0402	4	Close to VRAM
1uF	X7R	0603	8	Close to VRAM

X7R (+/-15%、-55~125℃)
*Per clamshell pair





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Title	CHANNEL-A_VRAM3,4 (2/4)
Size	A3
Document Number	LA48
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Date:	Friday, January 06, 2012
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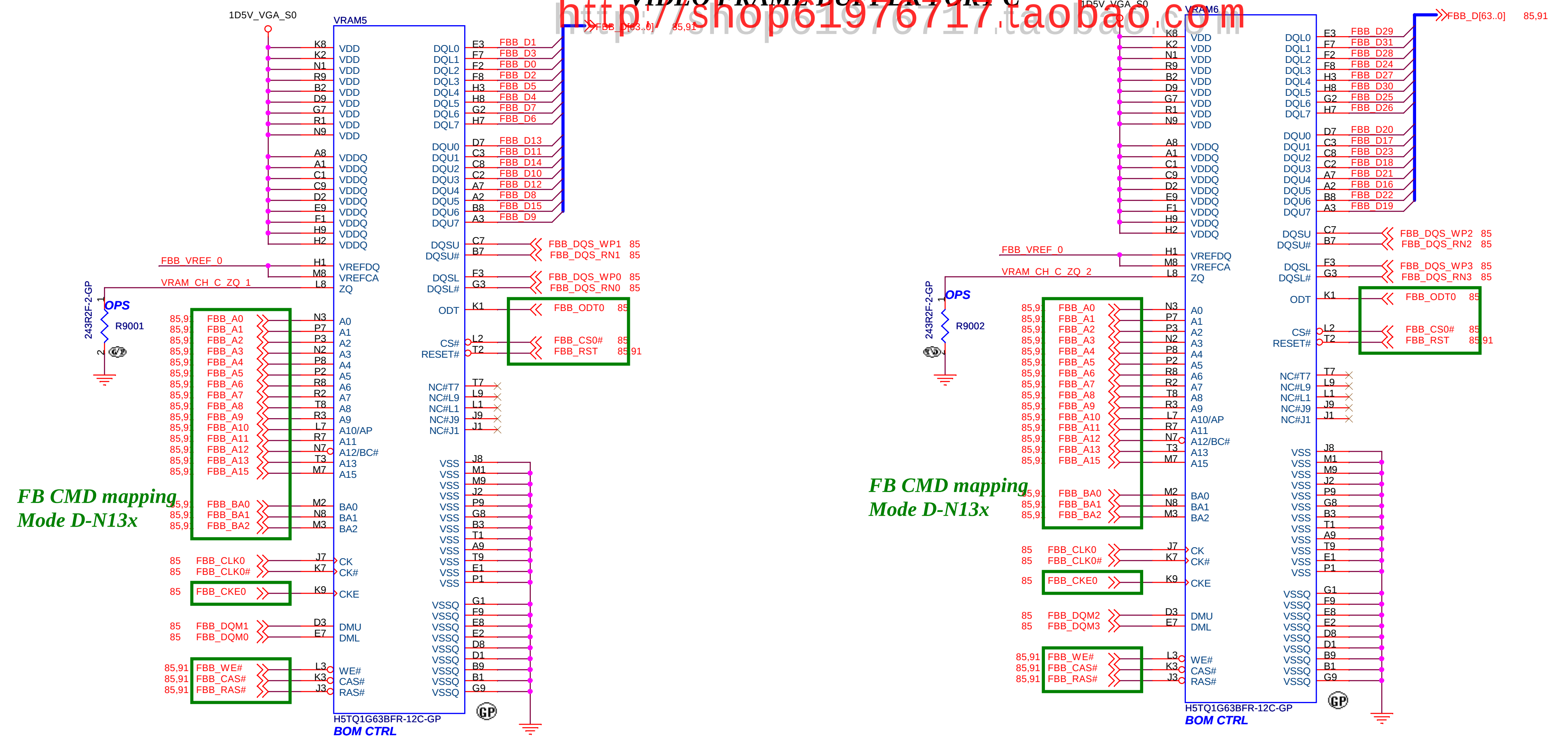
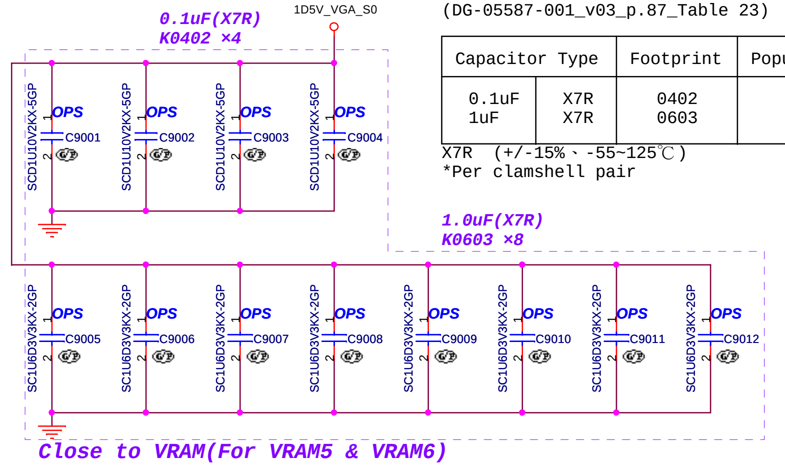
VIDEO FRAME BUFFER PORT C

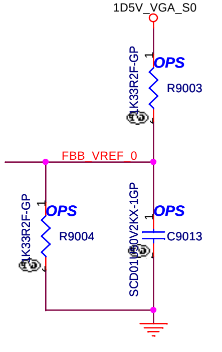


Combined Memory FBVDD/Q Decoupling DDR3×16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type		Footprint	Population	Location
0.1uF	X7R	0402	4	Close to VRAM
1uF	X7R	0603	8	Close to VRAM

X7R (+/-15%、-55~125℃)
*Per clamshell pair





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Title	CHANNEL-C_VRAM5,6 (3/4)
Size	A3
Document Number	LA48
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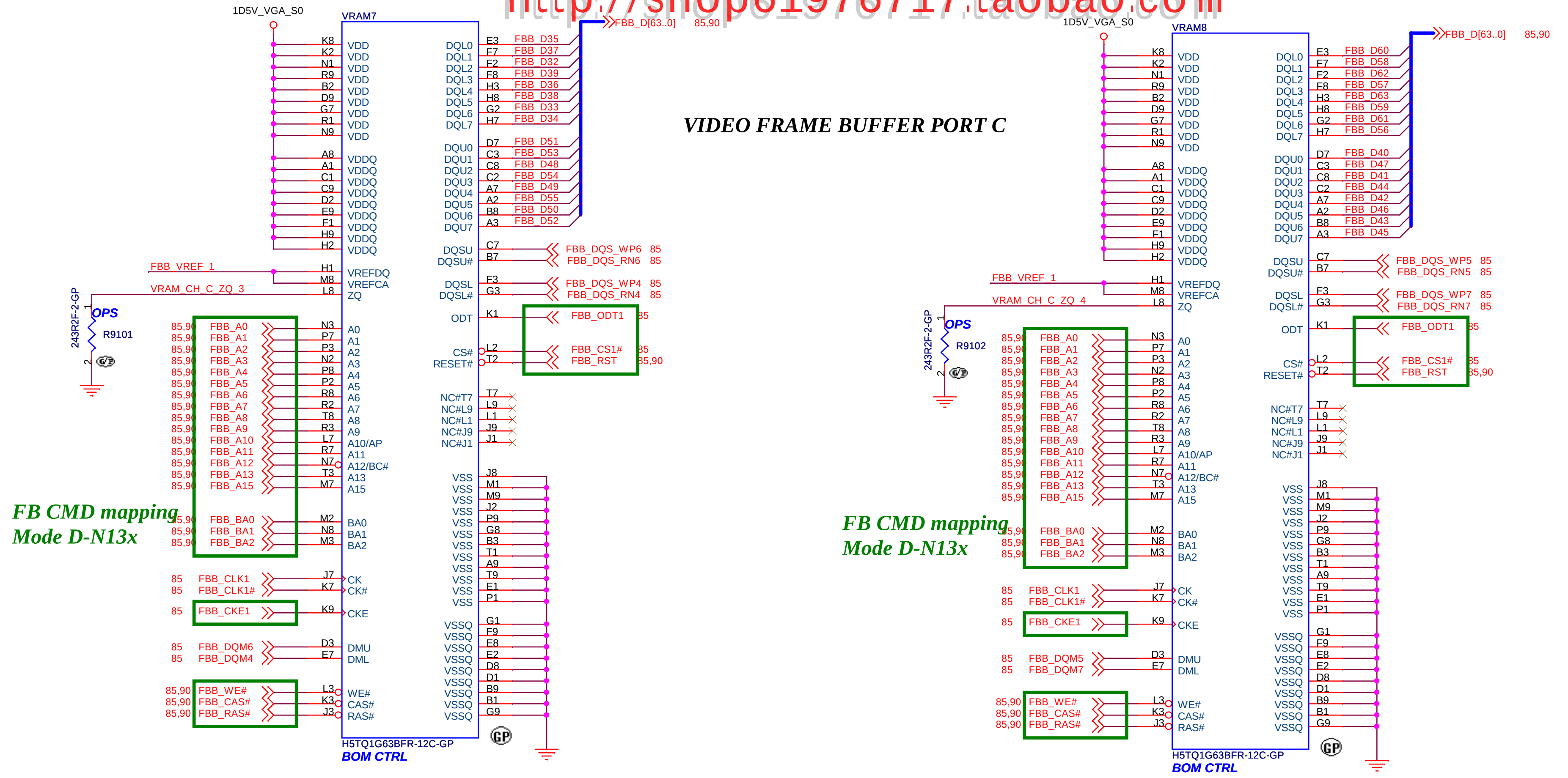
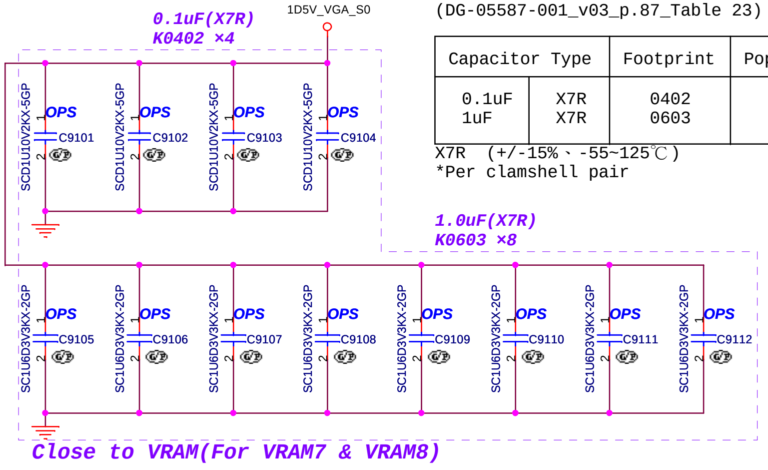
VIDEO FRAME BUFFER PORT C

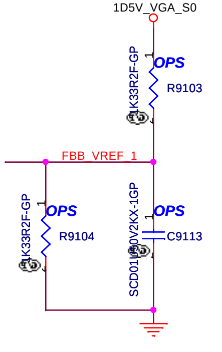


Combined Memory FBVDD/Q Decoupling DDR3×16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type		Footprint	Population	Location
0.1uF	X7R	0402	4	Close to VRAM
1uF	X7R	0603	8	Close to VRAM

X7R (+/-15%、-55~125℃)
*Per clamshell pair



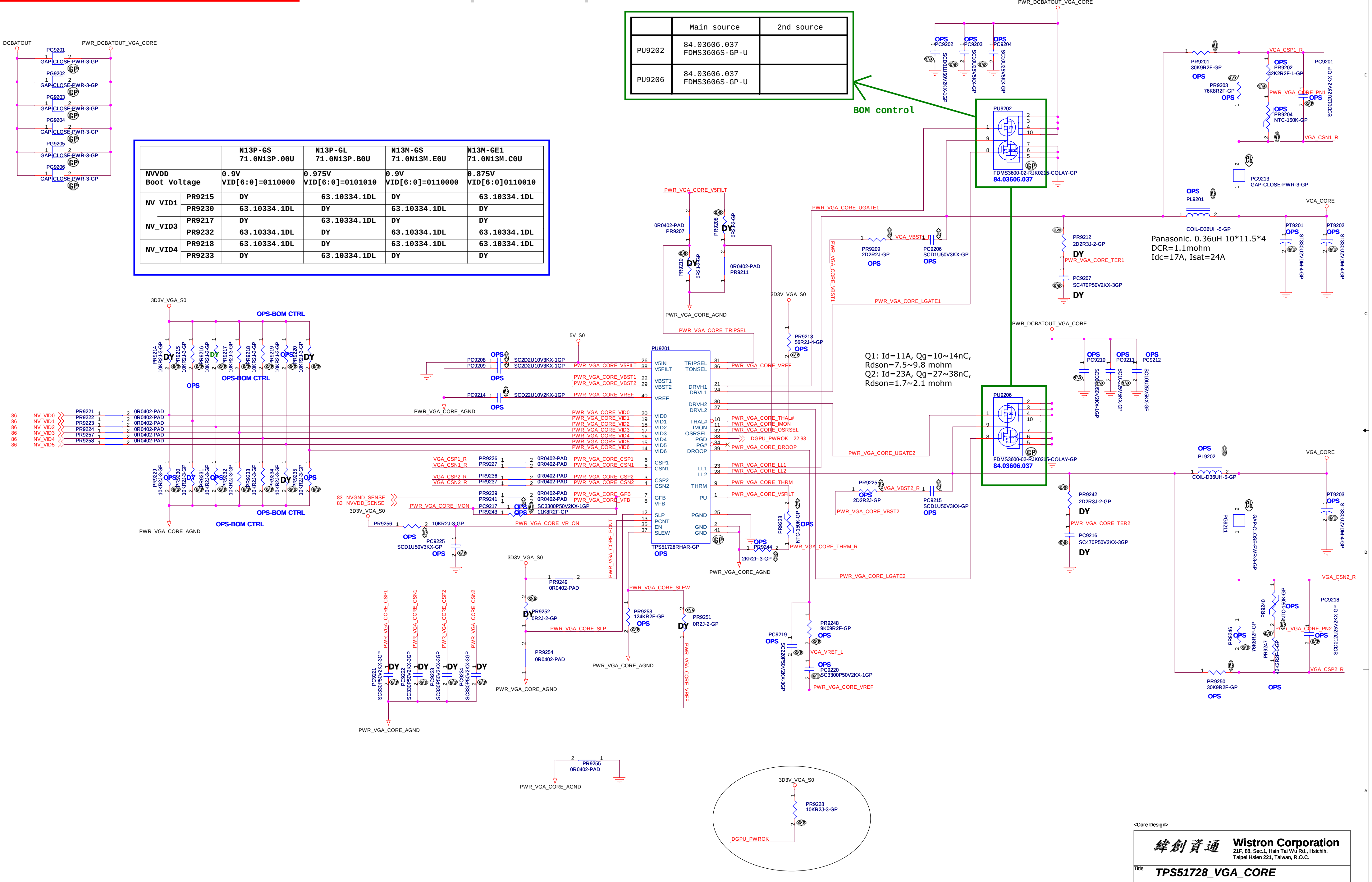


SSID = PWR.Plane.Regulator_GFX

	Main source	2nd source
PU9202	84.03606.037 FDMS3606S-GP-U	
PU9206	84.03606.037 FDMS3606S-GP-U	

BOM control

		N13P-GS 71.0N13P.00U	N13P-GL 71.0N13P.B0U	N13M-GS 71.0N13M.E0U	N13M-GE1 71.0N13M.C0U
NVVDD Boot Voltage		0.9V VID[6:0]=0110000	0.975V VID[6:0]=0101010	0.9V VID[6:0]=0110000	0.875V VID[6:0]0110010
NV_VID1	PR9215	DY	63.10334.1DL	DY	63.10334.1DL
	PR9230	63.10334.1DL	DY	63.10334.1DL	DY
NV_VID3	PR9217	DY	63.10334.1DL	DY	DY
	PR9232	63.10334.1DL	DY	63.10334.1DL	63.10334.1DL
NV_VID4	PR9218	63.10334.1DL	DY	63.10334.1DL	63.10334.1DL
	PR9233	DY	63.10334.1DL	DY	DY



Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A

Q1: Id=11A, Qg=10~14nC,
Rdson=7.5~9.8 mohm
Q2: Id=23A, Qg=27~38nC,
Rdson=1.7~2.1 mohm

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Title	TPS51728_VGA_CORE	
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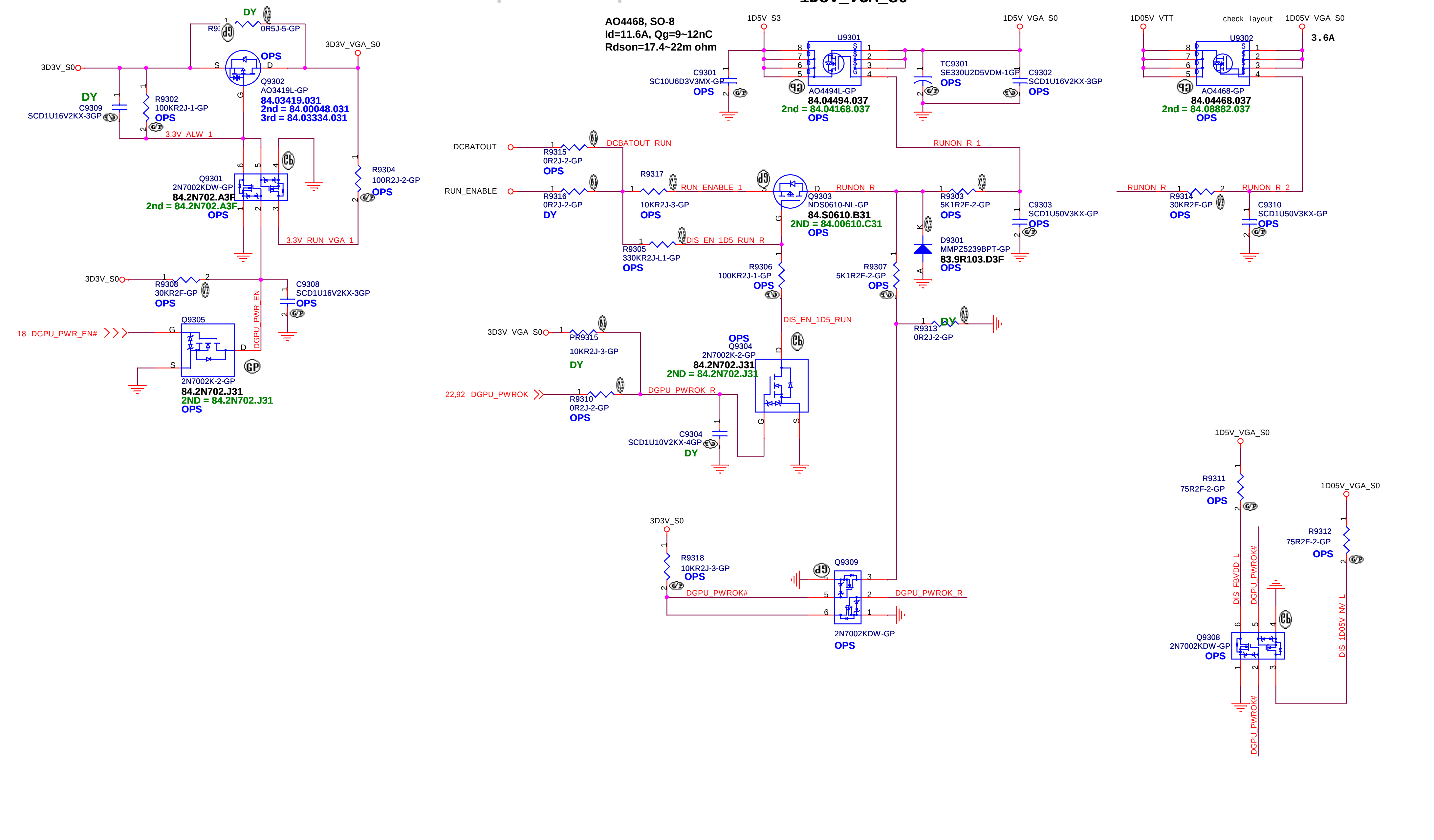
+3VS to 3.3V_DELAY Transfer

1D5V_VGA_S0

1.05V to 1.05V_VGA_S0 Transfer



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Title	**DISCRETE VGA POWER**	
Size A3	Document Number **LA480**	Rev SD
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Title	<Title>	
Size A4	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 94 of 103	

5 4 3 2 1

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Title	***Reserved***	
Size A4	Document Number **LA480**	Rev **SD**
Date: Friday, January 06, 2012	Sheet 95 of 103	

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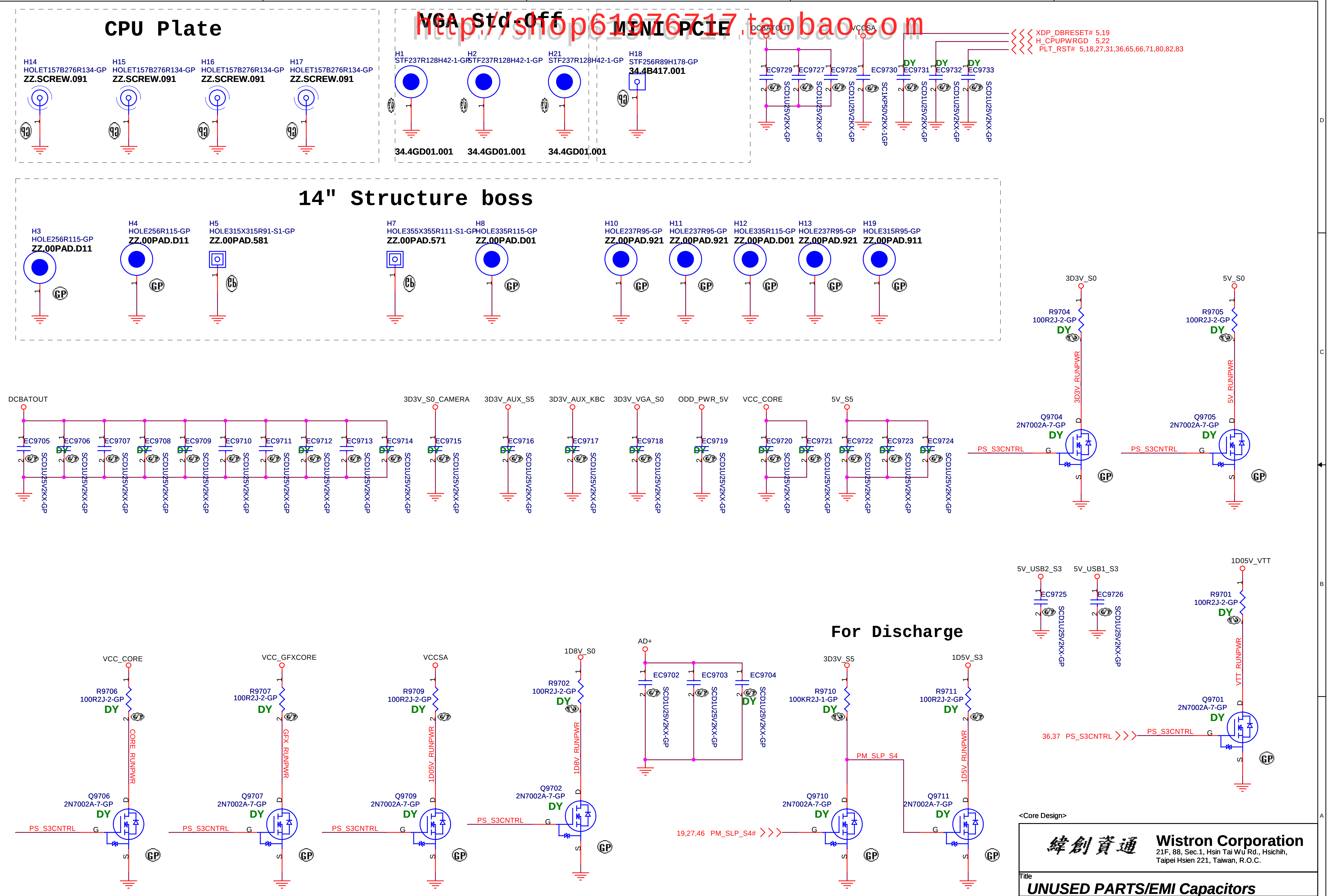
Title	***TOUCH PANEL***	
Size A4	Document Number **LA480**	Rev **SD**
Date: Friday, January 06, 2012	Sheet 96 of 103	



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Title: **UNUSED PARTS/EMI Capacitors**

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 — Sheet 97 of 103

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Title	*Change History*	
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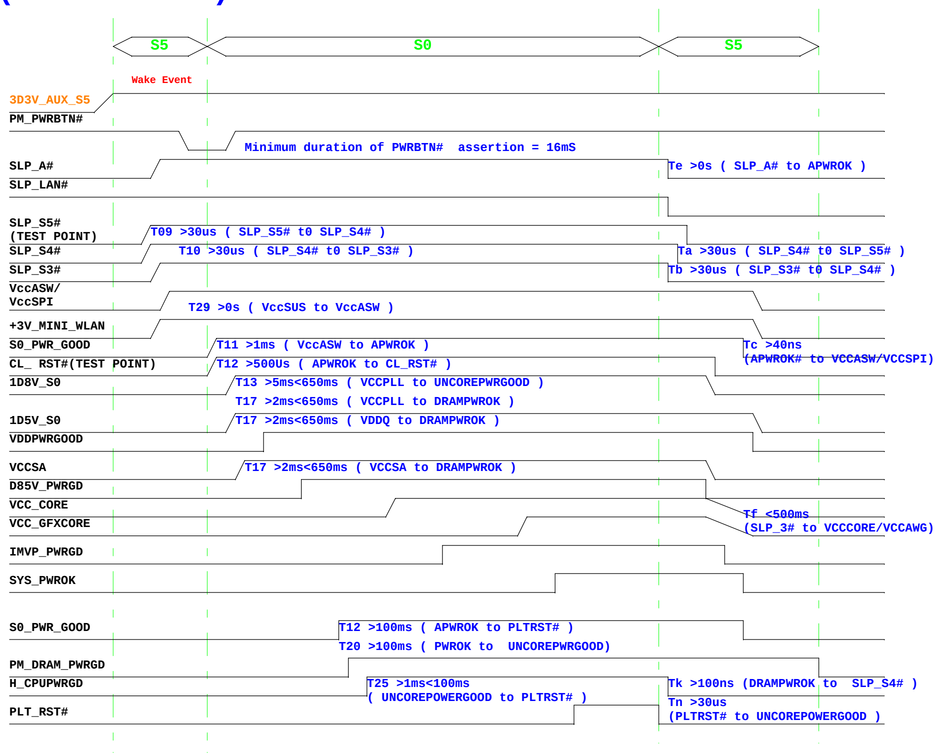
Date: Friday, January 06, 2012	Sheet 98 of 103	

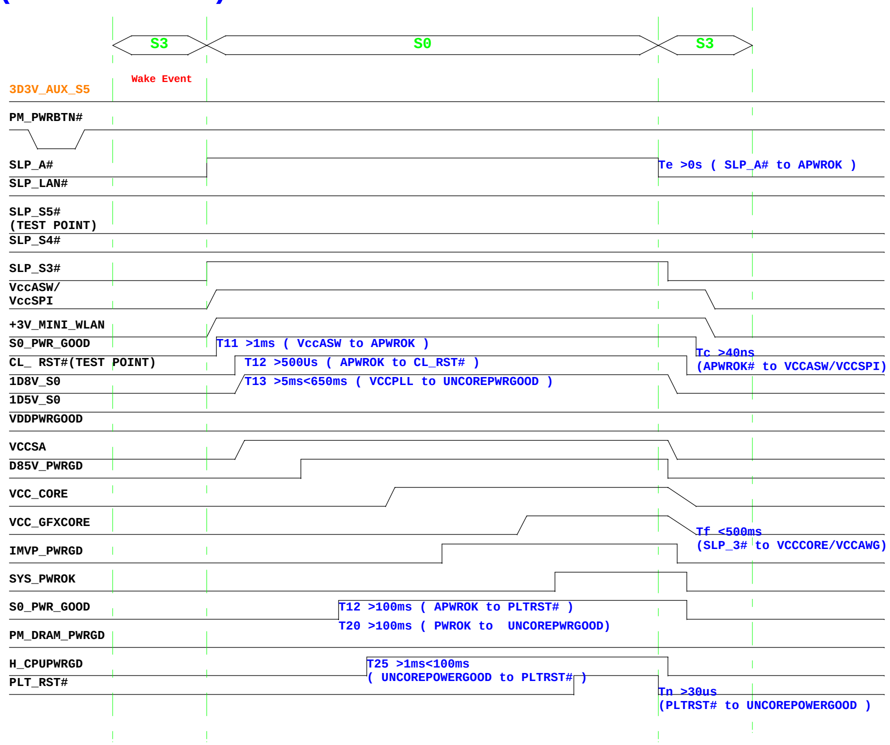
Intel-Power Sequence

(S5-to-S0-to-S5)



Intel PCH Pin Name	Main board PCH Pin Name
VccSUS (5V/3V)	3D3V_AUX_S5
PWRBTN#	PM_PWRBTN#
SLP_A#	SLP_A#
SLP_LAN#	SLP_LAN#
SLP_S5#	PM_SLP_S5#
SLP_S4#	PM_SLP_S4#
SLP_S3#	PM_SLP_S3#
VccASW/ VccSPI	VccASW/ VccSPI
Vcc_WLAN	+3V_MINI_WLAN
PWROK/APWROK	S0_PWR_GOOD
CL_ RST#	CL_ RST#
VCCPLL	1D8V_S0
VDDQ	1D5V_S0
VR_VDDQPWRGOOD	VDDPWRGOOD
VCCSA	VCCSA
IMVP7_VR_EN	D85V_PWRGD
VccCore	VCC_CORE
VccAXG	VCC_GFXCORE
IMVP7_PWRGD	IMVP_PWRGD
SYS_PWROK	SYS_PWROK
PWROK	S0_PWR_GOOD
DRAMPWROK	PM_DRAM_PWRGD
UNCOREPWRGOOD	H_CPUPWRGD
PLTRST#	PLT_RST#

(S3-to-S0-to-S3)



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Title: *Change History*

Size: A2 | Document Number: LA480 | Rev: SD

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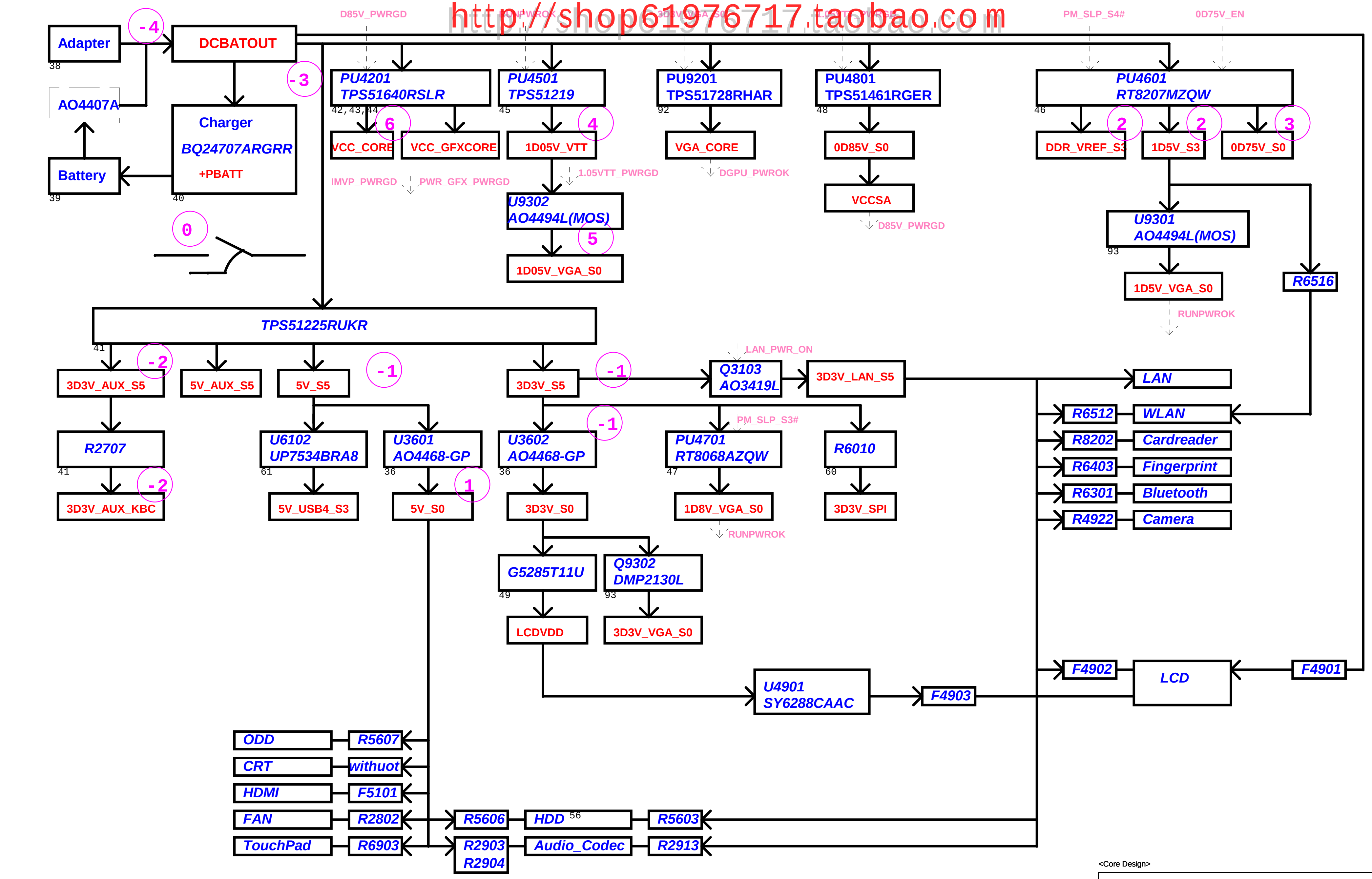

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Title	**Power Block Diagram**	
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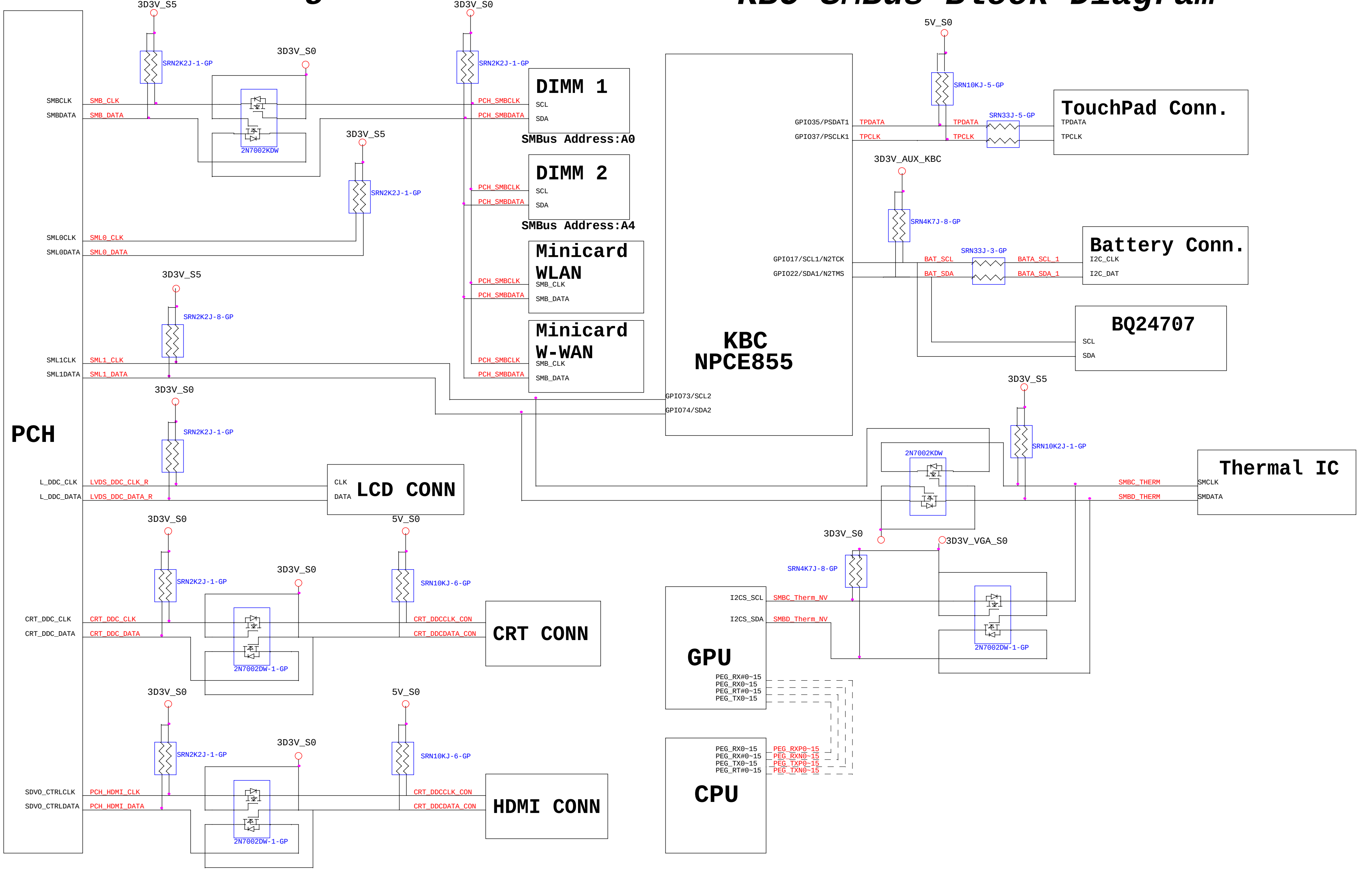
PCH SMBus Block Diagram

KBC SMBus Block Diagram



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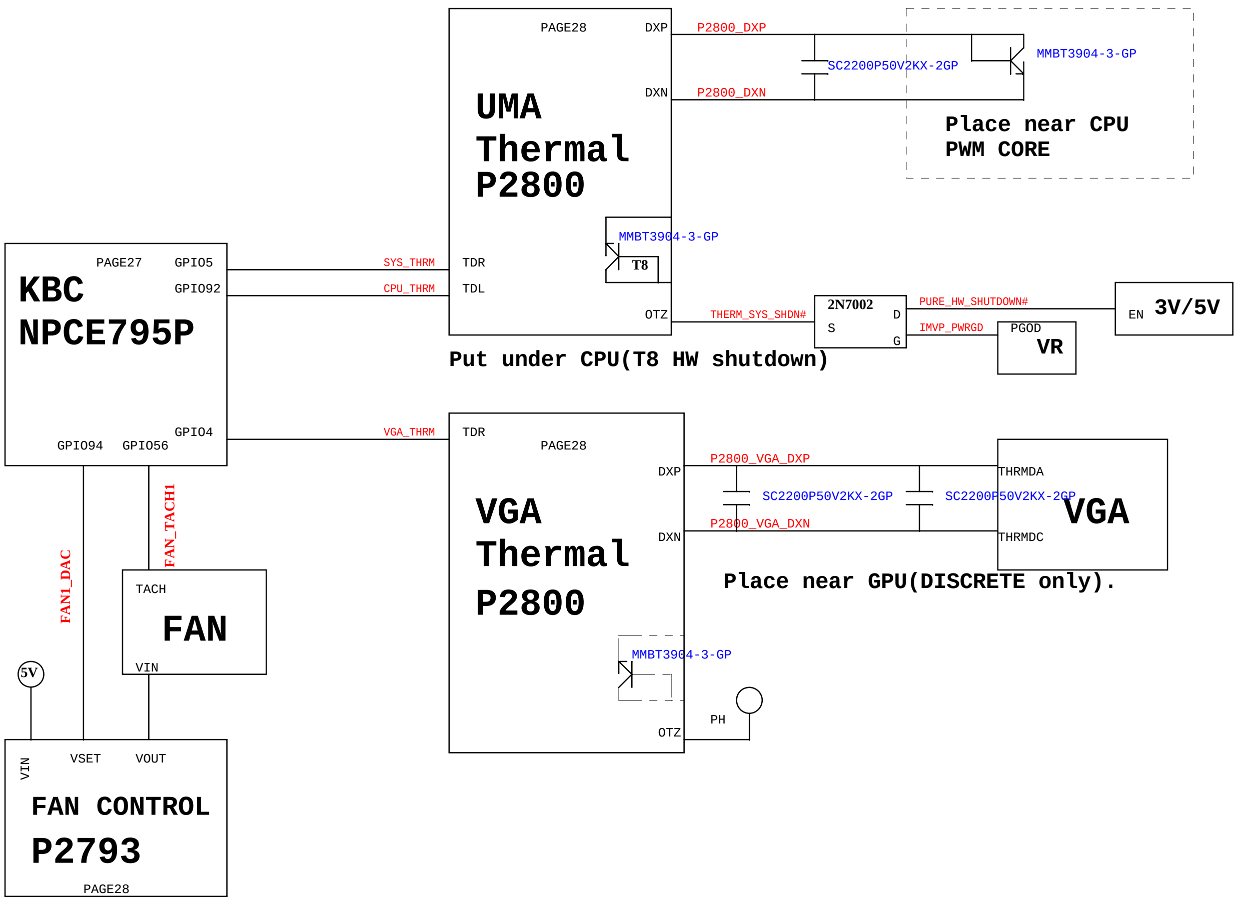
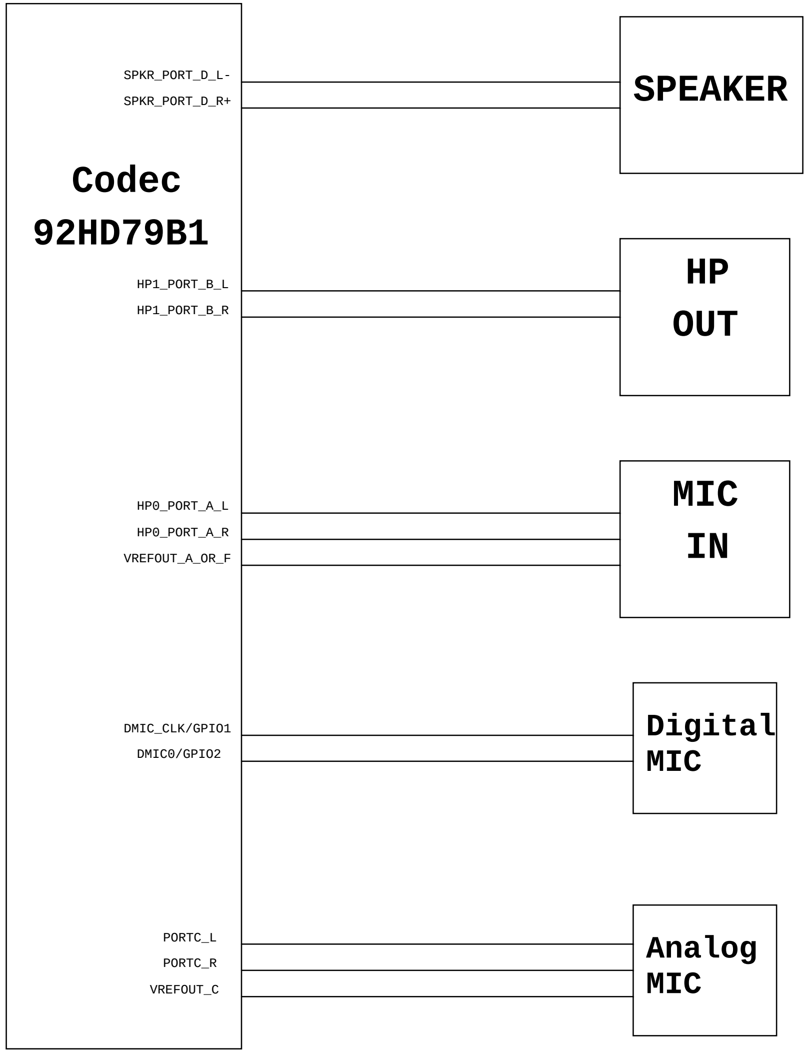
Title	SMBUS Block Diagram	
Size A2	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 101 of 103	

Thermal Block Diagram



Audio Block Diagram



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Title: *Thermal/Audio Block Diagram*		
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Title	*Change History*	
Size A4	Document Number LA480	Rev SD
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