LCFC NM-C711

GS44D/GS54D MB Schematics Document

ICL U42 with DDR4 + Nvidia N16V-GM

2019-06

REV:0.1

Security Classification	LC Future Center Secret Data		
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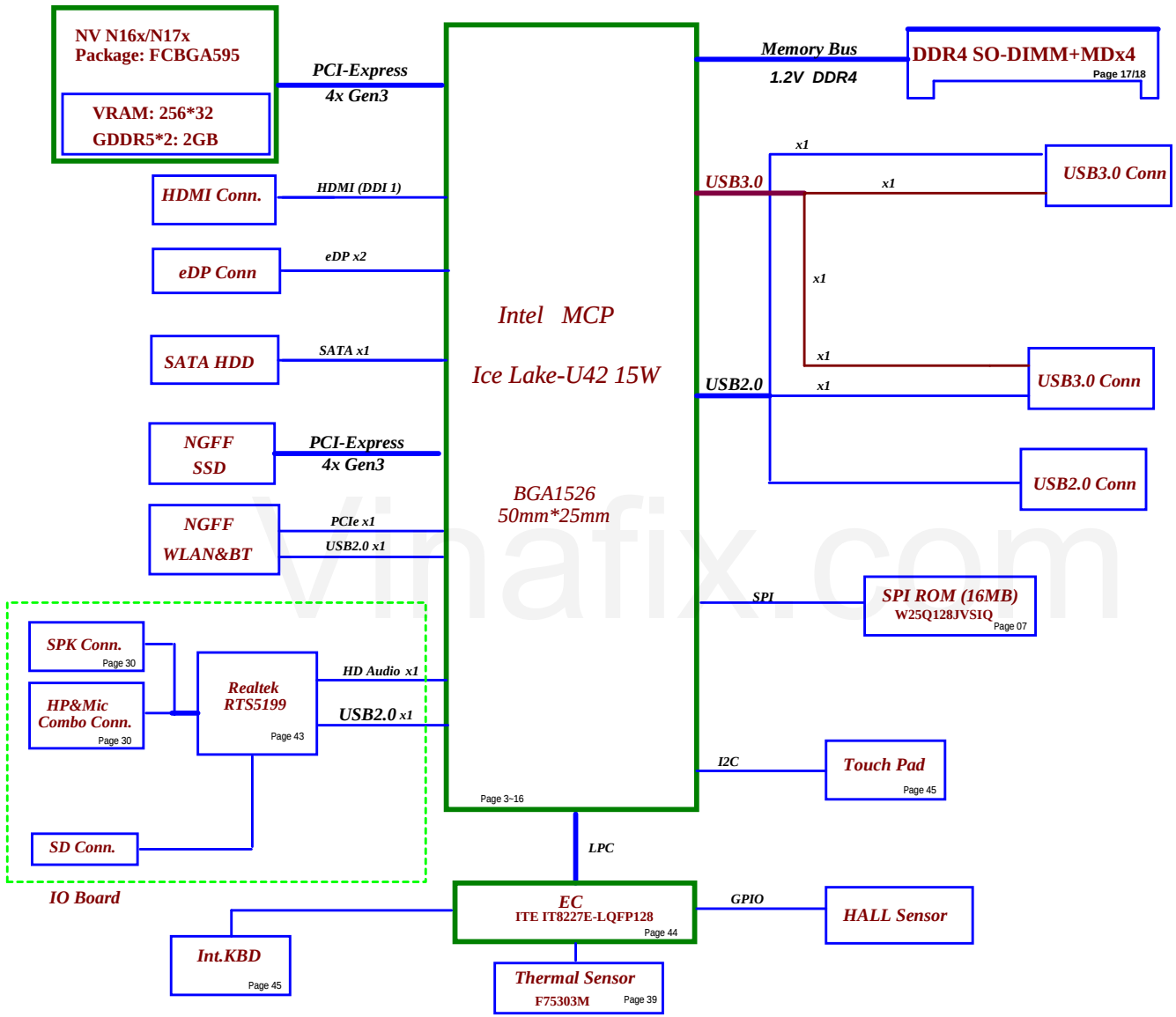

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Title: **Block Diagram**

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V9B+	+3VALW +5VALW +3VALW_PCH +1.8VALW VCC_AUX	+1.2V +2.5V_DDR +VCCST +VCCSTG	+5VS +3VS +1.8VS +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT		Function
USB3.0	1	USB3.0 Conn
	2	USB3.0 Conn
	3	NC
	4	NC
	5	
	6	
USB2.0	1	USB3.0 Conn
	2	USB3.0 Conn
	3	NC
	4	NC
	5	Camere
	6	Touch Screen
	7	Finger Print
	8	Card Reader
	9	USB2.0 conn
	10	Bluetooth
PCIE	5~8 X4	DGPU
	9	WLAN
	10	NC
	11	SATA HDD
	12	NC
	13~16 X4	PCIE/SATA SSD

BOM Structure	BTO Item
@	Un-stuff
14@	For 14" part
15@	For 15" part
CD@	For cost down
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC un-stuff part
ME@	For ME part
UMA@	For UMA part
OPT@	For NV GPU part
OPTN16@	For NV N16S-GTR GPU part
OPTN17@	For NV N17S-G1 GPU part
TS@	For touch screen part
TP@	For TOuch Pad Part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8227E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8227E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK0 EC_SMB_DA0	IT8227E +3VS	X	X	V +3VG_AON	V +3VS	X	X	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8227E +3VAWL	X	X	X	V	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	X

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update

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Title: **Notes List**

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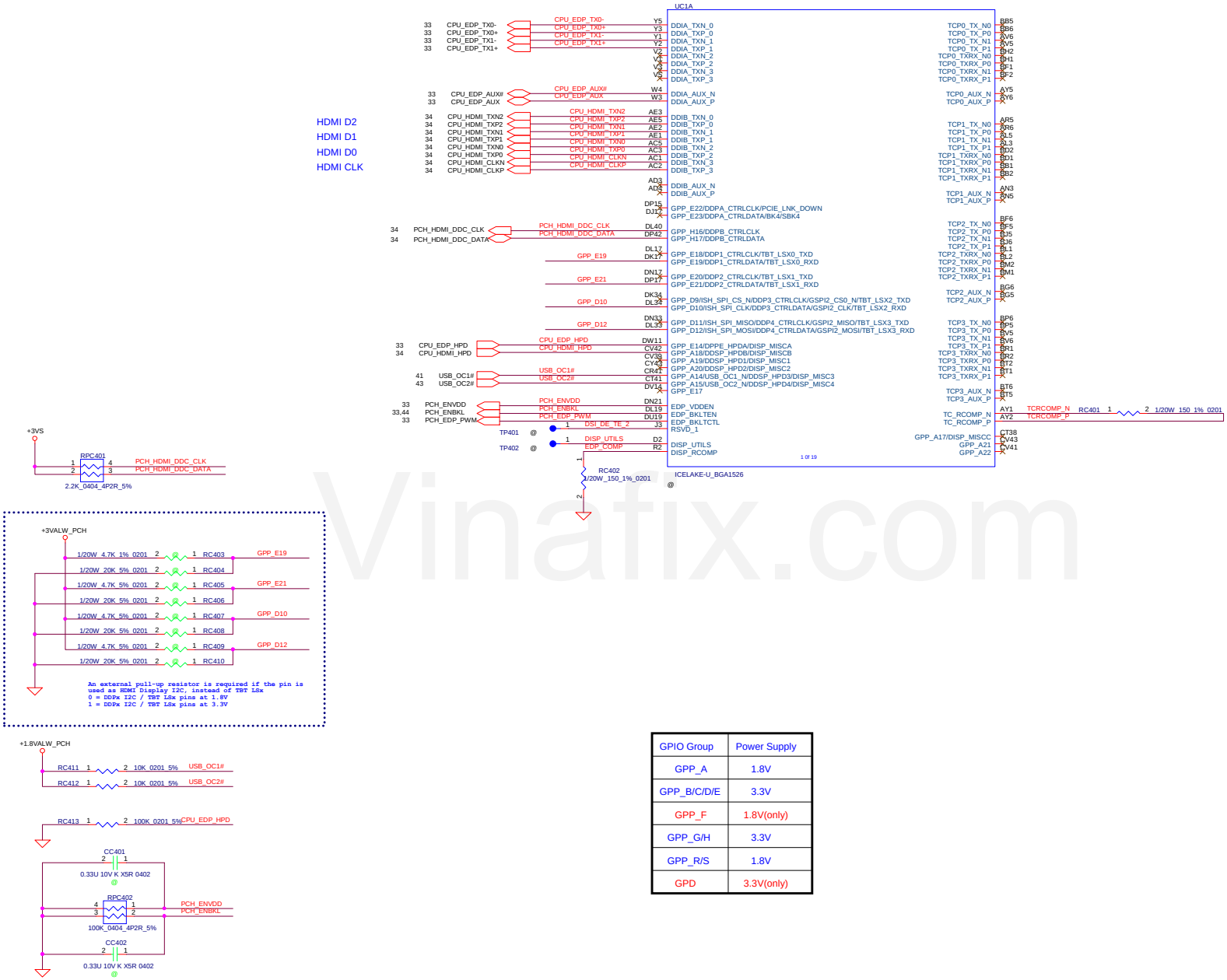

GPIO Group	Power Supply
GPP_A	1.8V
GPP_B/C/D/E	3.3V
GPP_F	1.8V(only)
GPP_G/H	3.3V
GPP_R/S	1.8V
GPD	3.3V(only)

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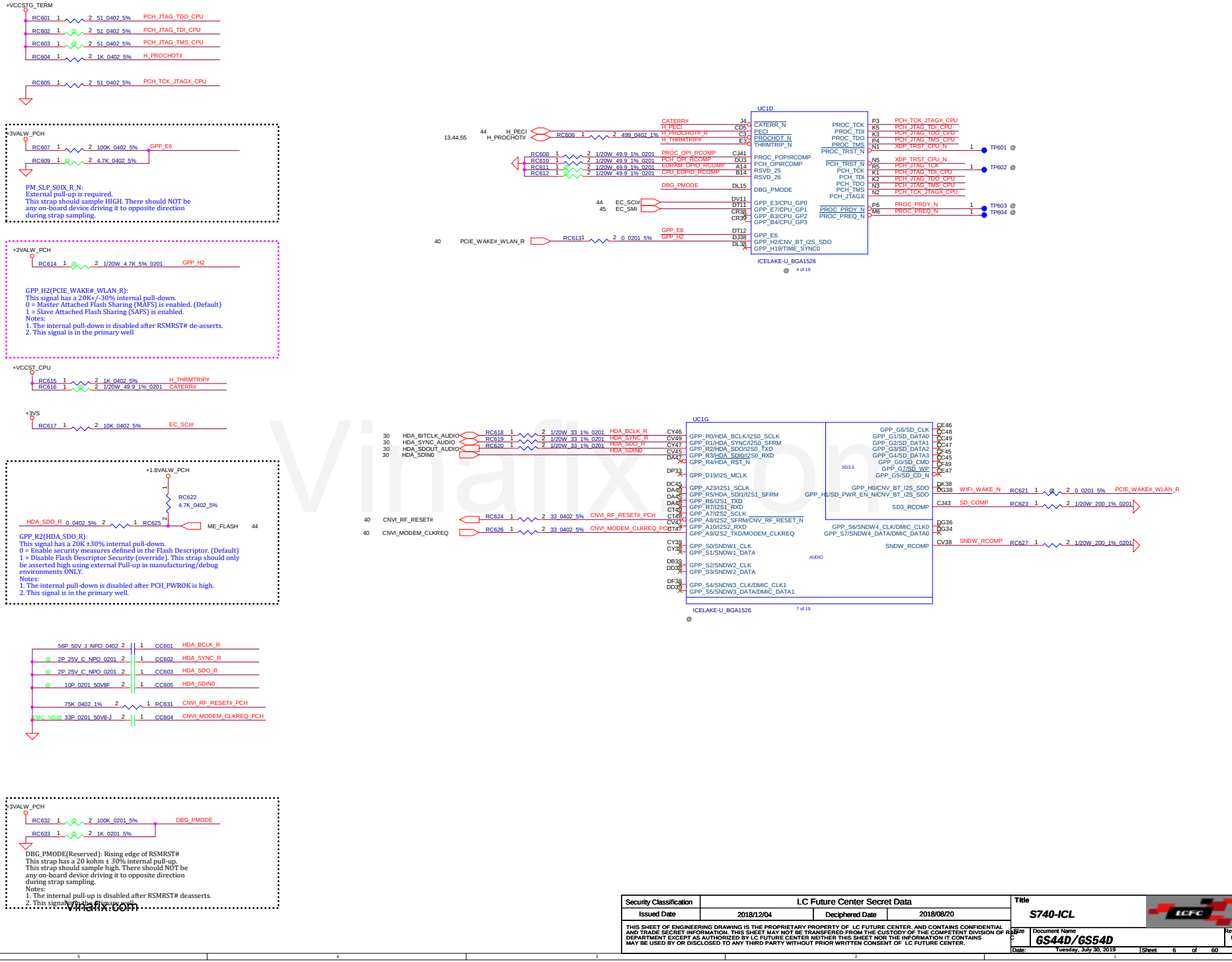

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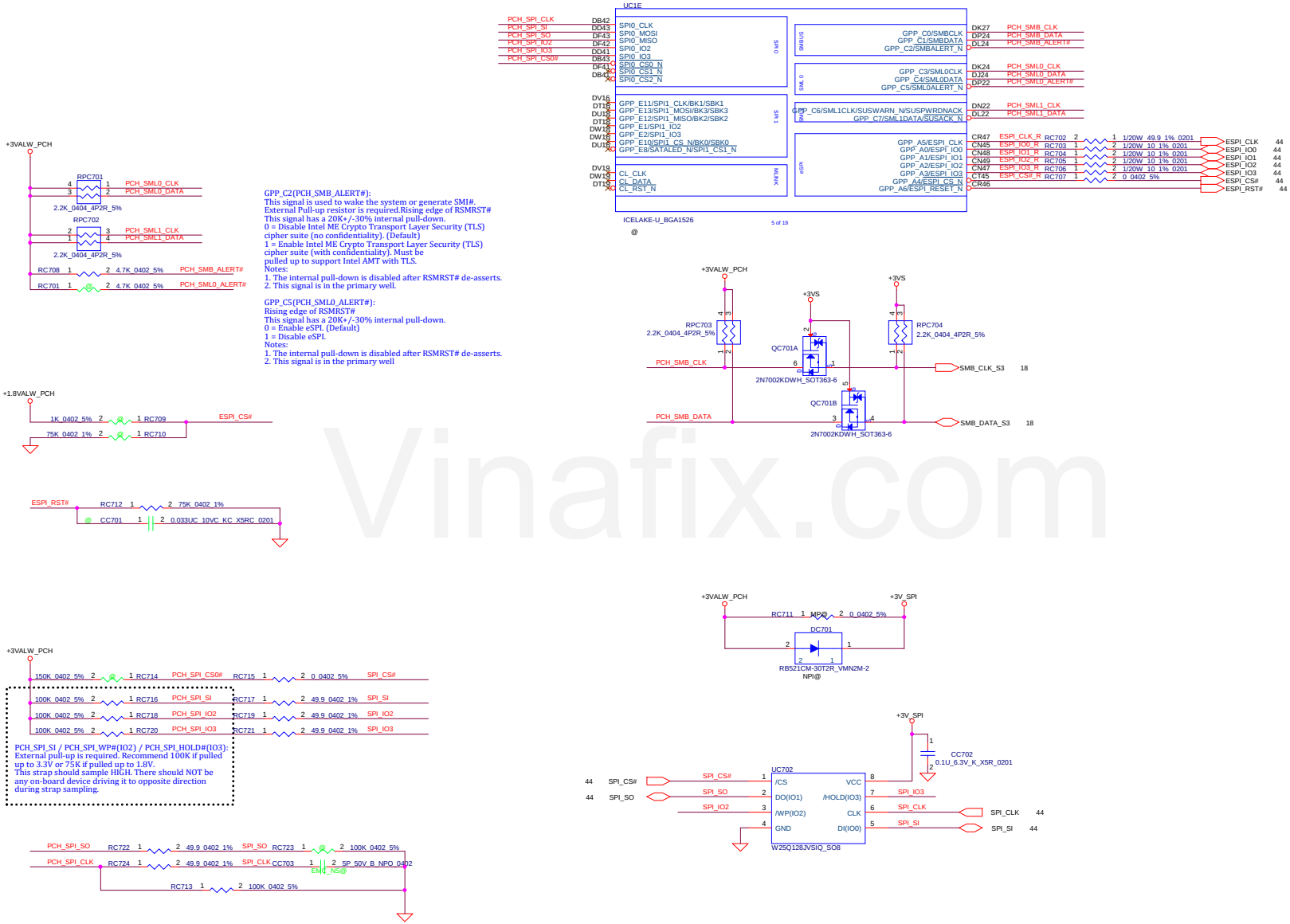

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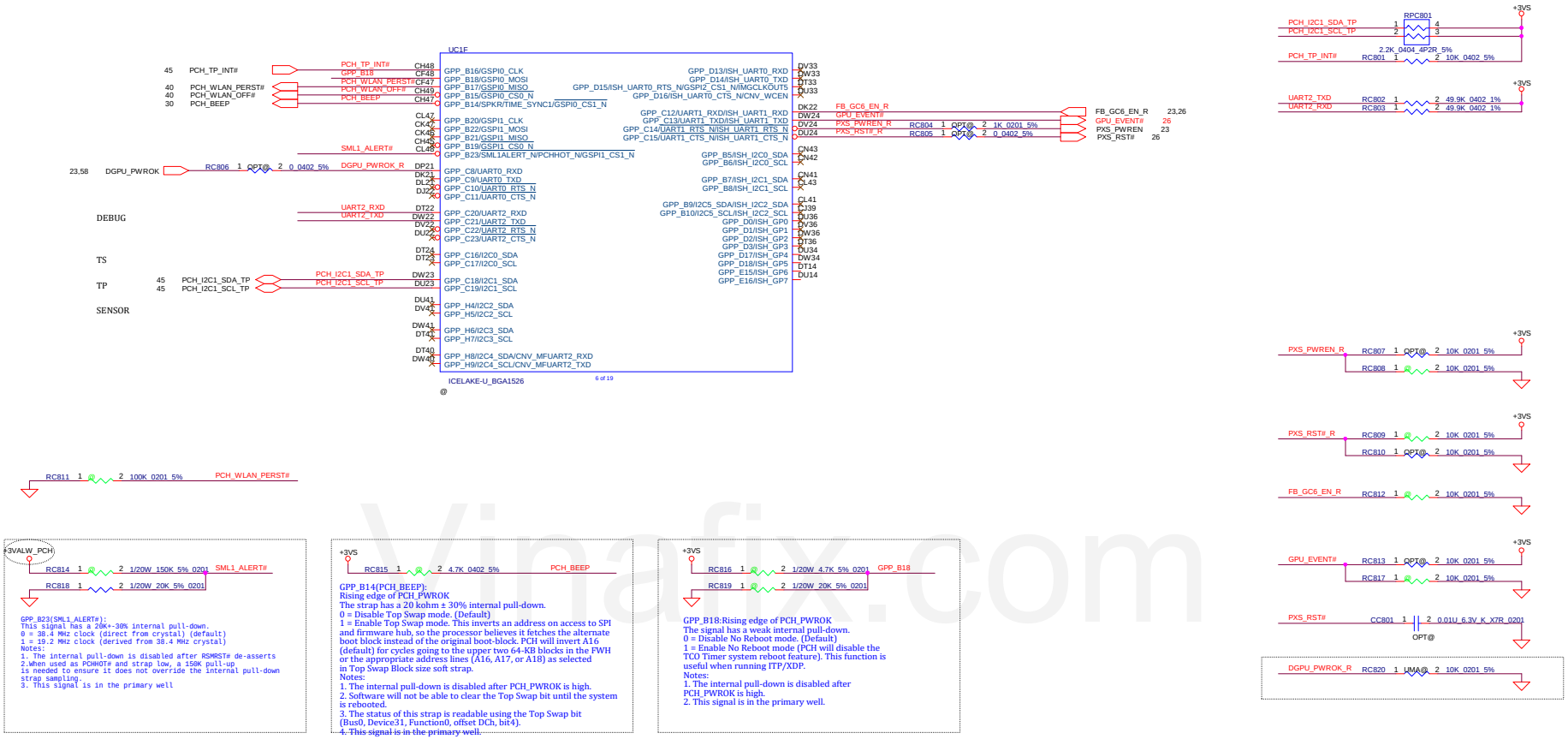

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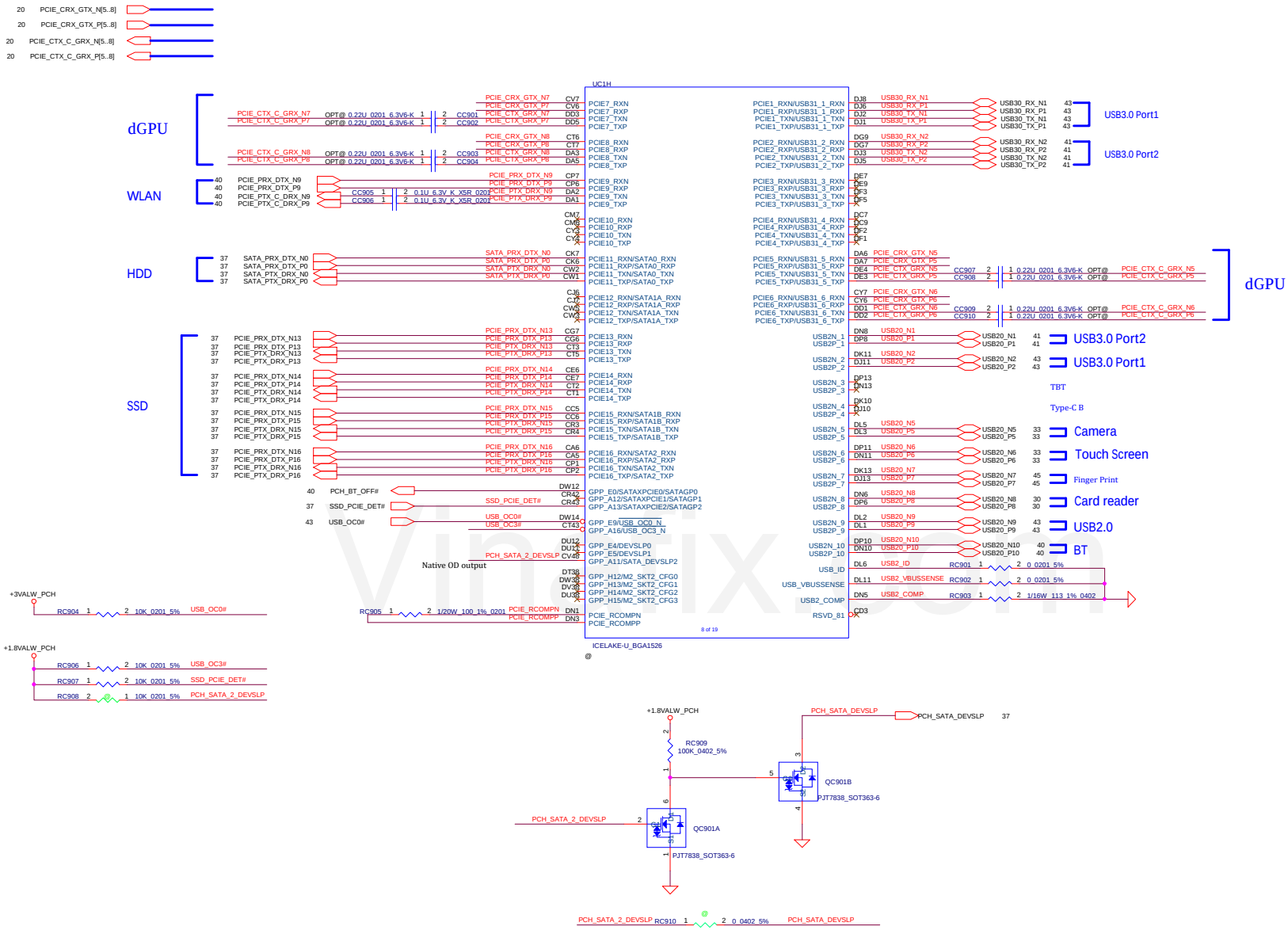

1. DEVSLP is an open-drain pin on the PCH side and is not required external pull-up orpull-down. The PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATAdevice, per DEVSLP specification). PCH will drive pin low to signal an exit fromDEVSLP state.
2. DEVSLP is supported in direct connect, mSATA/mPCIe, uSSD, M.2.
3. 1 DEVSLP pin is required to support EACH DEVSLP enabled RAID storage device.
(Example: 2 DEVSLP pins are required to support 2 DEVSLP RAID storage devices).

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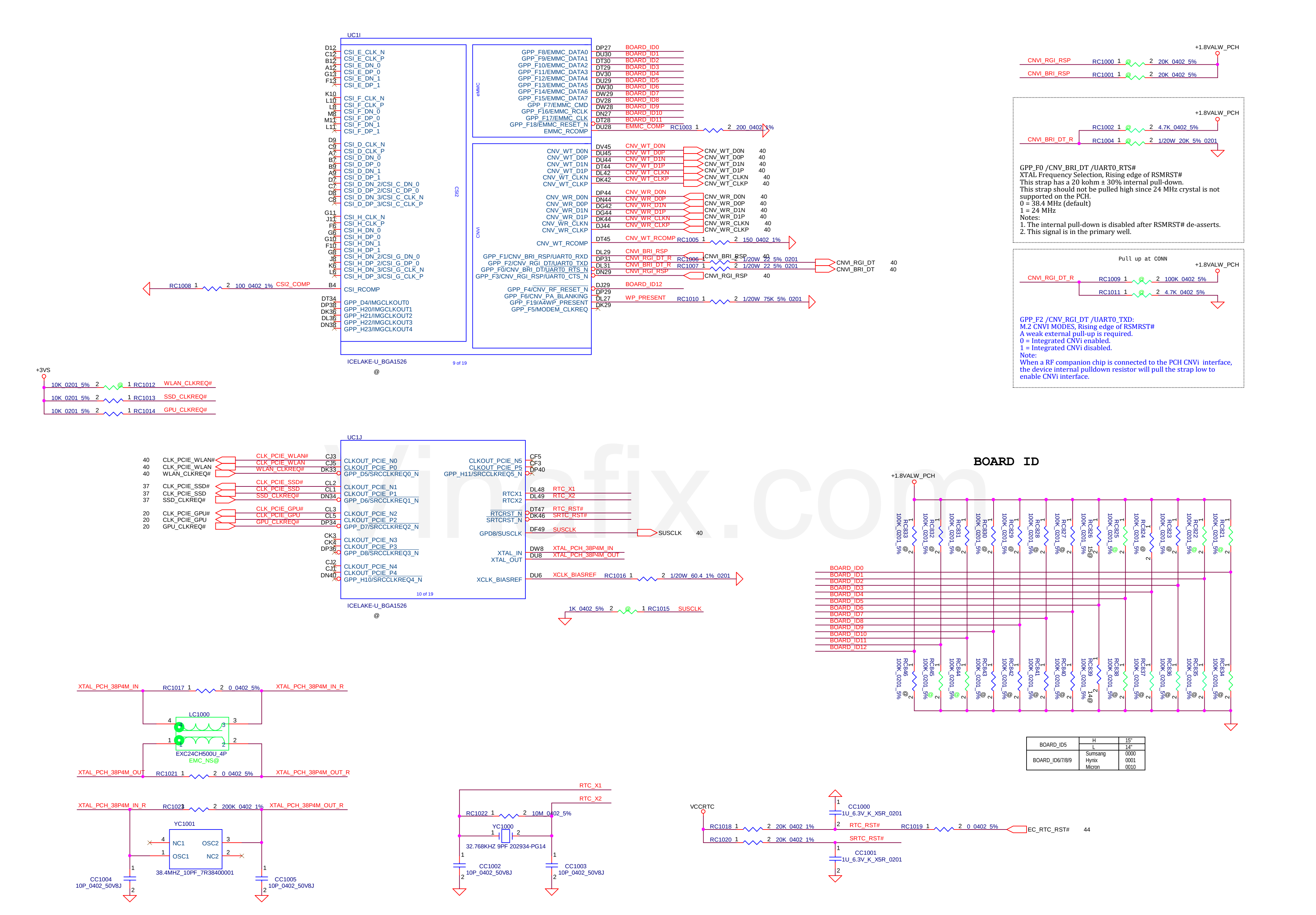

UC1I
CSI_E_CLK_N
CSI_E_CLK_P
CSI_E_DN_0
CSI_E_DP_0
CSI_E_DN_1
CSI_E_DP_1
CSI_F_CLK_N
CSI_F_CLK_P
CSI_F_DN_0
CSI_F_DP_0
CSI_F_DN_1
CSI_F_DP_1
CSI_D_CLK_N
CSI_D_CLK_P
CSI_D_DN_0
CSI_D_DP_0
CSI_D_DN_1
CSI_D_DP_1
CSI_D_DN_2/CSI_C_DN_0
CSI_D_DP_2/CSI_C_DP_0
CSI_D_DN_3/CSI_C_CLK_N
CSI_D_DP_3/CSI_C_CLK_P
CSI_H_CLK_N
CSI_H_CLK_P
CSI_H_DN_0
CSI_H_DP_0
CSI_H_DN_1
CSI_H_DP_1
CSI_H_DN_2/CSI_G_DN_0
CSI_H_DP_2/CSI_G_DP_0
CSI_H_DN_3/CSI_G_CLK_N
CSI_H_DP_3/CSI_G_CLK_P
CSI_RCOMP
GPP_D4/IMGCLKOUT0
GPP_H20/IMGCLKOUT1
GPP_H21/IMGCLKOUT2
GPP_H22/IMGCLKOUT3
GPP_H23/IMGCLKOUT4
CSI2
eMMC
GPP_F8/EMMC_DATA0
GPP_F9/EMMC_DATA1
GPP_F10/EMMC_DATA2
GPP_F11/EMMC_DATA3
GPP_F12/EMMC_DATA4
GPP_F13/EMMC_DATA5
GPP_F14/EMMC_DATA6
GPP_F15/EMMC_DATA7
GPP_F7/EMMC_CMD
GPP_F16/EMMC_RCLK
GPP_F17/EMMC_CLK
GPP_F18/EMMC_RESET_N
EMMC_RCOMP
BOARD_ID0
BOARD_ID1
BOARD_ID2
BOARD_ID3
BOARD_ID4
BOARD_ID5
BOARD_ID6
BOARD_ID7
BOARD_ID8
BOARD_ID9
BOARD_ID10
BOARD_ID11
EMMC_COMP
RC1003 1 2 200_0402_1%
CNVi
CNV_WT_D0N
CNV_WT_D0P
CNV_WT_D1N
CNV_WT_D1P
CNV_WT_CLKN
CNV_WT_CLKP
CNV_WR_D0N
CNV_WR_D0P
CNV_WR_D1N
CNV_WR_D1P
CNV_WR_CLKN
CNV_WR_CLKP
CNV_WT_RCOMP
RC1005 1 2 150_0402_1%
GPP_F1/CNV_BRI_RSP/UART0_RXD
GPP_F2/CNV_RGI_DT/UART0_TXD
GPP_F0/CNV_BRI_DT/UART0_RTS_N
GPP_F3/CNV_RGI_RSP/UART0_CTS_N
CNVI_BRI_RSP
CNVI_RGI_DT_R
CNVI_BRI_DT_R
CNVI_RGI_RSP
RC1006 1 2 1/20W_22_5%_0201
RC1007 1 2 1/20W_22_5%_0201
CNVI_RGI_DT 40
CNVI_BRI_DT 40
GPP_F4/CNV_RF_RESET_N
GPP_F6/CNV_PA_BLANKING
GPP_F19/A4WP_PRESENT
GPP_F5/MODEM_CLKREQ
BOARD_ID12
WP_PRESENT
RC1010 1 2 1/20W_75K_5%_0201
RC1008 1 2 100_0402_1% CSI2_COMP
ICELAKE-U_BGA1526
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+1.8VALW_PCH
CNVI_RGI_RSP RC1000 1 2 20K_0402_5%
CNVI_BRI_RSP RC1001 1 2 20K_0402_5%
CNVI_BRI_DT_R RC1002 1 2 4.7K_0402_5%
RC1004 1 2 1/20W_20K_5%_0201
GPP_F0 /CNV_BRI_DT /UART0_RTS#
XTAL Frequency Selection, Rising edge of RSMRST#
This strap has a 20 kohm ± 30% internal pull-down.
This strap should not be pulled high since 24 MHz crystal is not supported on the PCH.
0 = 38.4 MHz (default)
1 = 24 MHz
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.
Pull up at CONN
CNVI_RGI_DT_R RC1009 1 2 100K_0402_5%
RC1011 1 2 4.7K_0402_5%
GPP_F2 /CNV_RGI_DT /UART0_TXD:
M.2 CNVI MODES, Rising edge of RSMRST#
A weak external pull-up is required.
0 = Integrated CNVi enabled.
1 = Integrated CNVi disabled.
Note:
When a RF companion chip is connected to the PCH CNVi interface, the device internal pulldown resistor will pull the strap low to enable CNVi interface.
+3VS
10K_0201_5% 2 1 RC1012 WLAN_CLKREQ#
10K_0201_5% 2 1 RC1013 SSD_CLKREQ#
10K_0201_5% 2 1 RC1014 GPU_CLKREQ#
UC1J
CLK_PCIE_WLAN#
CLK_PCIE_WLAN
WLAN_CLKREQ#
CLK_PCIE_SSD#
CLK_PCIE_SSD
SSD_CLKREQ#
CLK_PCIE_GPU#
CLK_PCIE_GPU
GPU_CLKREQ#
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
GPP_D5/SRCCLKREQ0_N
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
GPP_D6/SRCCLKREQ1_N
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
GPP_D7/SRCCLKREQ2_N
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
GPP_D8/SRCCLKREQ3_N
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
GPP_H10/SRCCLKREQ4_N
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
GPP_H11/SRCCLKREQ5_N
RTCX1
RTCX2
RTCRST_N
SRTCRST_N
GPD8/SUSCLK
XTAL_IN
XTAL_OUT
XCLK_BIASREF
RTC_X1
RTC_X2
RTC_RST#
SRTC_RST#
SUSCLK
SUSCLK 40
XTAL_PCH_38P4M_IN
XTAL_PCH_38P4M_OUT
XCLK_BIASREF
RC1016 1 2 1/20W_60.4_1%_0201
ICELAKE-U_BGA1526
10 of 19
1K_0402_5% 2 1 RC1015 SUSCLK
BOARD ID
+1.8VALW_PCH
RC833 RC832 RC831 RC830 RC829 RC828 RC827 RC826 RC825 RC824 RC823 RC822 RC821
100K_0201_5%
RC846 RC845 RC844 RC843 RC842 RC841 RC840 RC839 RC838 RC837 RC836 RC835 RC834
BOARD_ID0
BOARD_ID1
BOARD_ID2
BOARD_ID3
BOARD_ID4
BOARD_ID5
BOARD_ID6
BOARD_ID7
BOARD_ID8
BOARD_ID9
BOARD_ID10
BOARD_ID11
BOARD_ID12
BOARD_ID5 | H | 15"
 | L | 14"
BOARD_ID6/7/8/9 | Samsung | 0000
 | Hynix | 0001
 | Micron | 0010
XTAL_PCH_38P4M_IN RC1017 1 2 0_0402_5% XTAL_PCH_38P4M_IN_R
LC1000
EXC24CH500U_4P
EMC_NS@
XTAL_PCH_38P4M_OUT RC1021 1 2 0_0402_5% XTAL_PCH_38P4M_OUT_R
XTAL_PCH_38P4M_IN_R RC1023 1 2 200K_0402_1% XTAL_PCH_38P4M_OUT_R
YC1001
NC1
OSC1
OSC2
NC2
38.4MHZ_10PF_7R38400001
CC1004
10P_0402_50V8J
CC1005
10P_0402_50V8J
RTC_X1
RTC_X2
RC1022 1 2 10M_0402_5%
YC1000
32.768KHZ 9PF 202934-PG14
CC1002
10P_0402_50V8J
CC1003
10P_0402_50V8J
VCCRTC
CC1000
1U_6.3V_K_X5R_0201
RC1018 1 2 20K_0402_1% RTC_RST#
RC1019 1 2 0_0402_5%
EC_RTC_RST# 44
RC1020 1 2 20K_0402_1% SRTC_RST#
CC1001
1U_6.3V_K_X5R_0201

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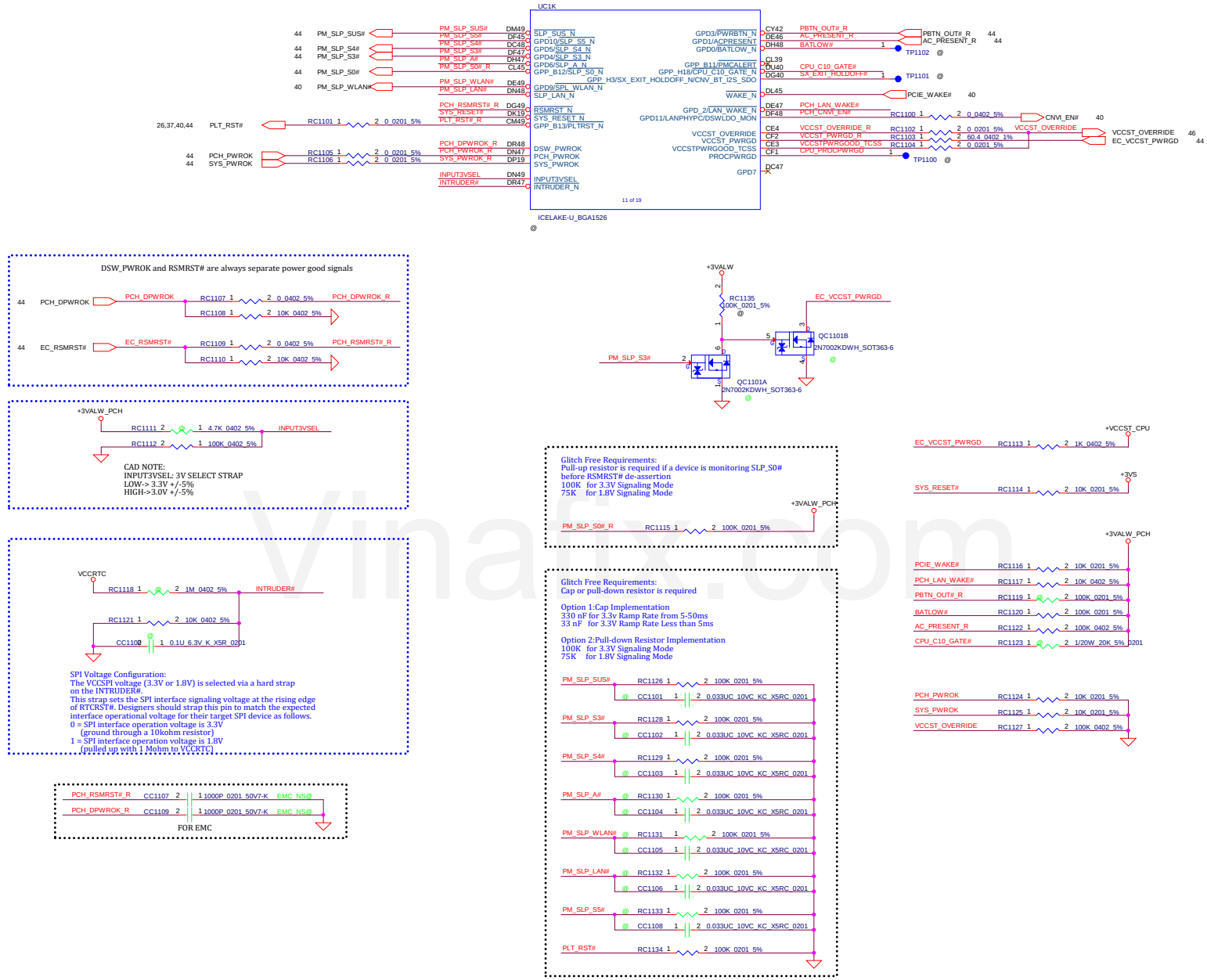

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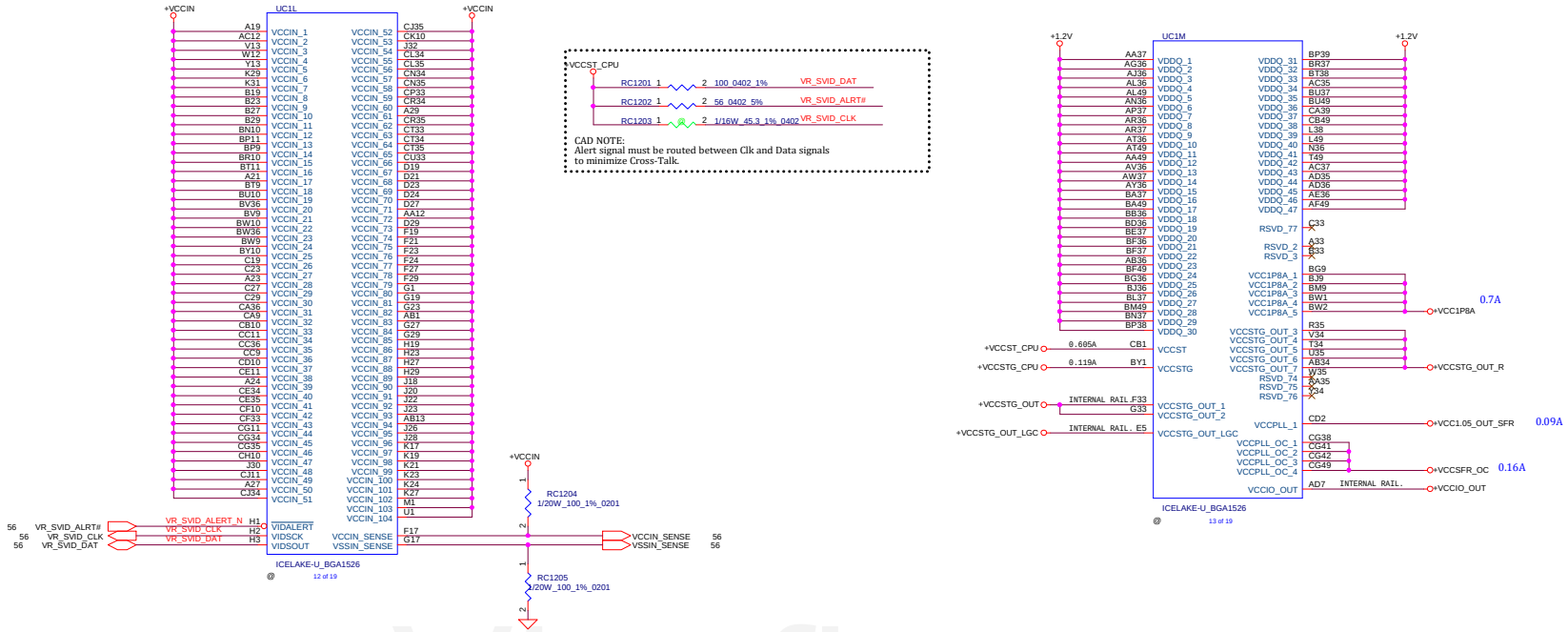

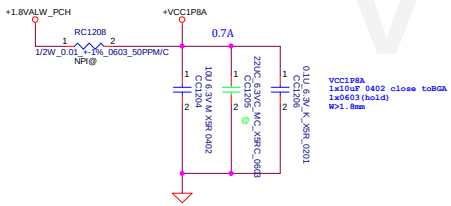

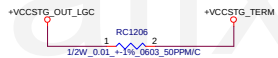

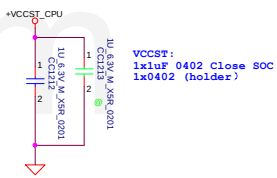

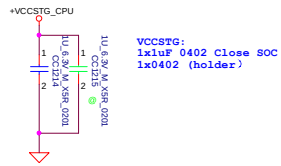

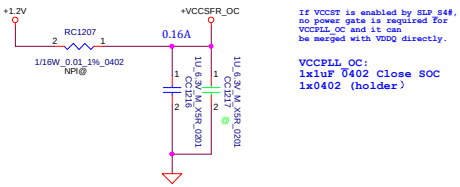

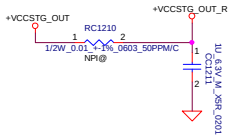

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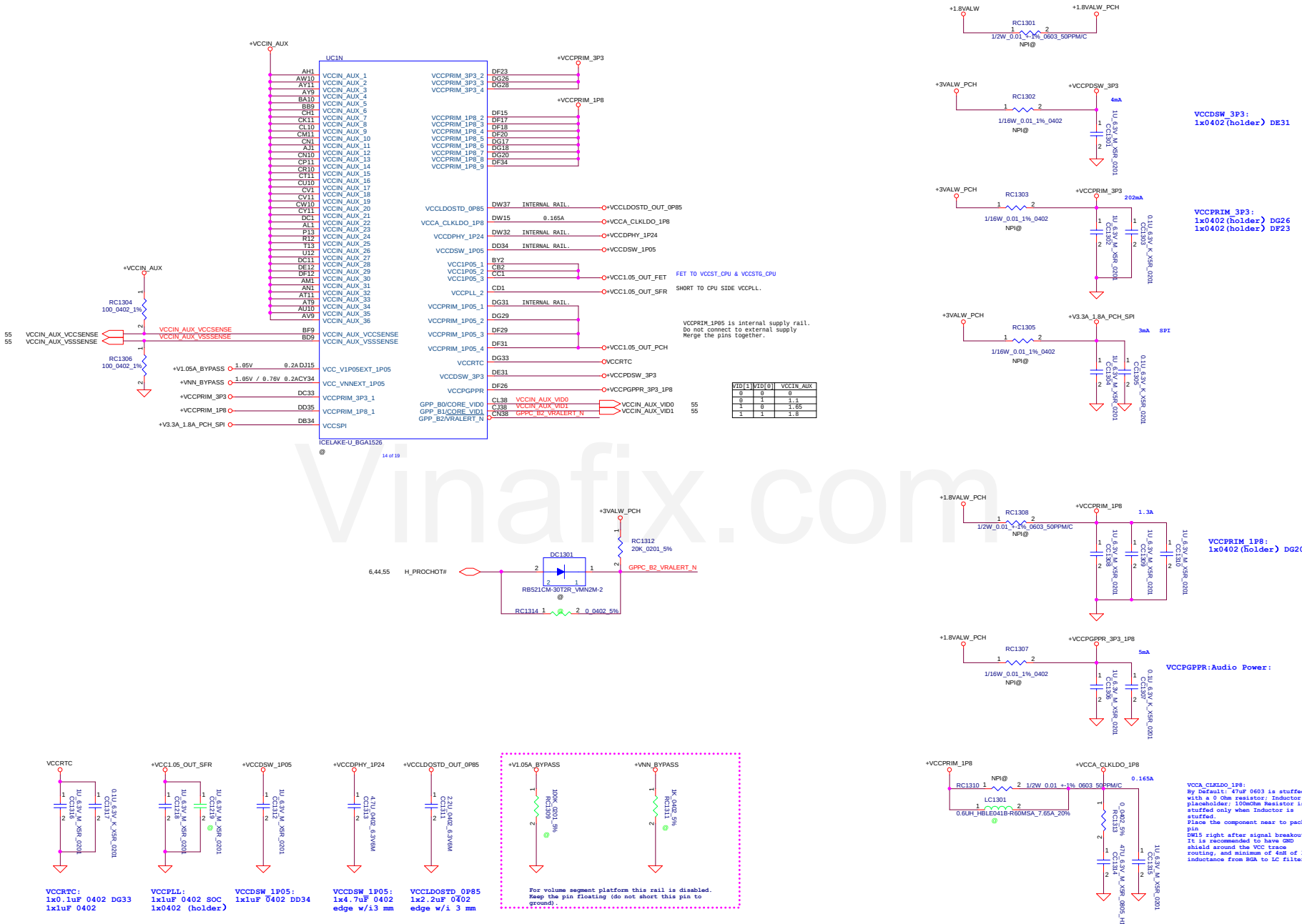

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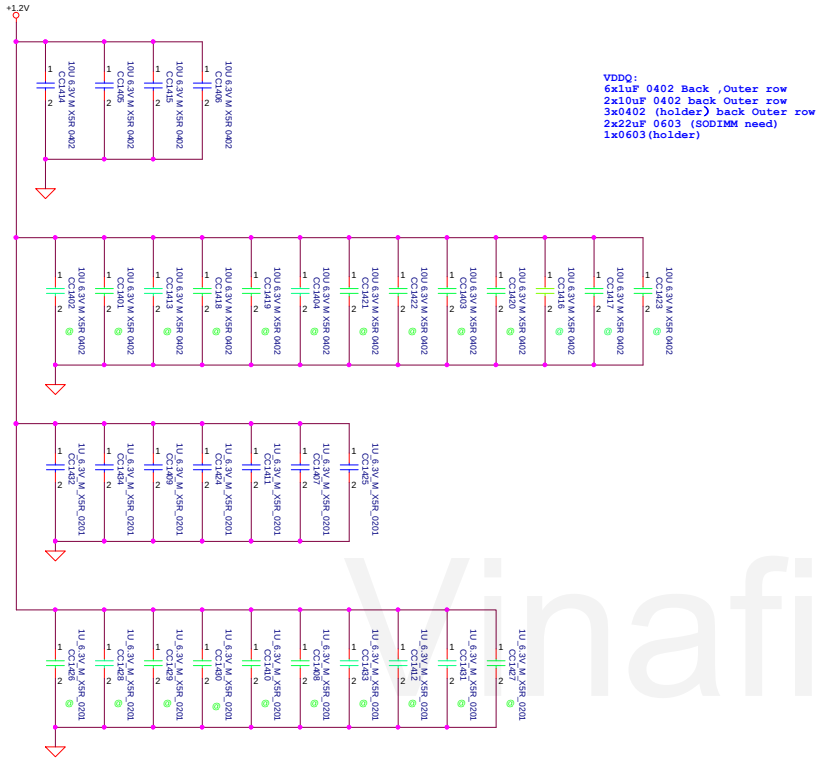
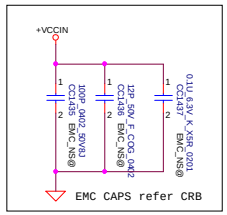
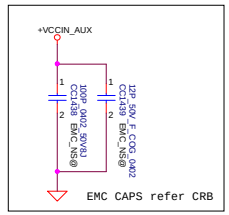


VDDQ:
6x1uF 0402 Back ,Outer row
2x10uF 0402 back Outer row
3x0402 (holder) back Outer row
2x22uF 0603 (SODIMM need)
1x0603(holder)





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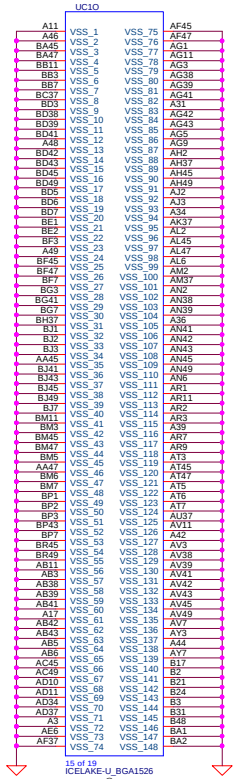

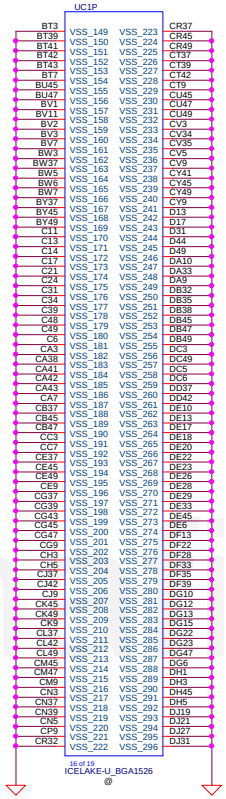

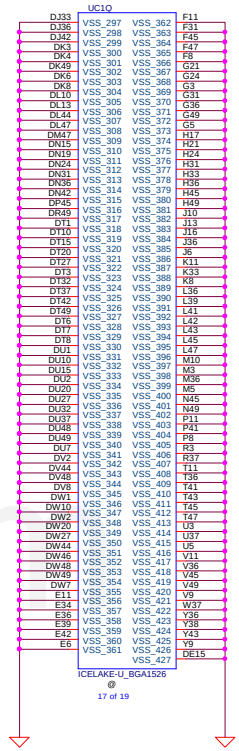

Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2018/08/20

Title: **S740-ICL**

Size	Document Name	Rev
C	GS44D/GS54D	0.1

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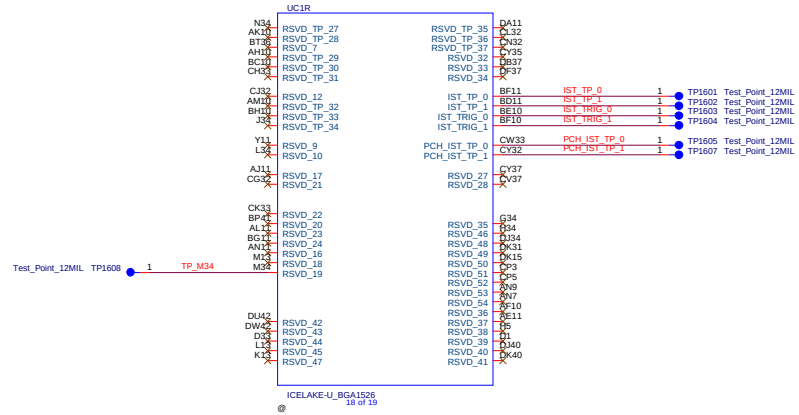
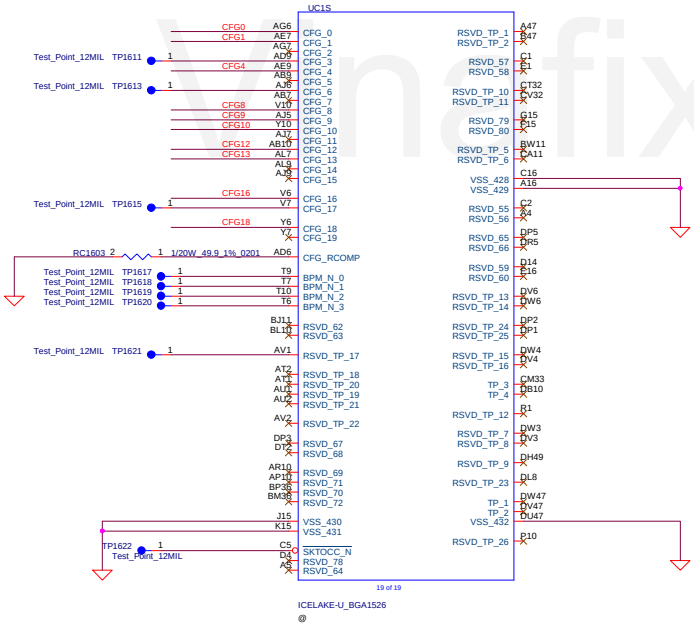
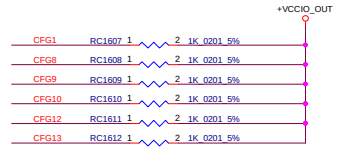


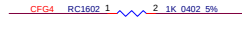


PROCESSOR CFG STRAPS

Stall reset sequence after PCU PLL lock until de-asserted

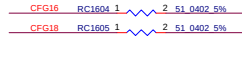
CFG0	1:Normal(Default) *
	0:Stall





Embedded Display Port Presence Strap

CFG4	1:Disable
	0:Enable(Default) *



Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2018/08/20

Title	S740-ICL		
Size C	Document Name	GS44D/GS54D	Rev 0.1
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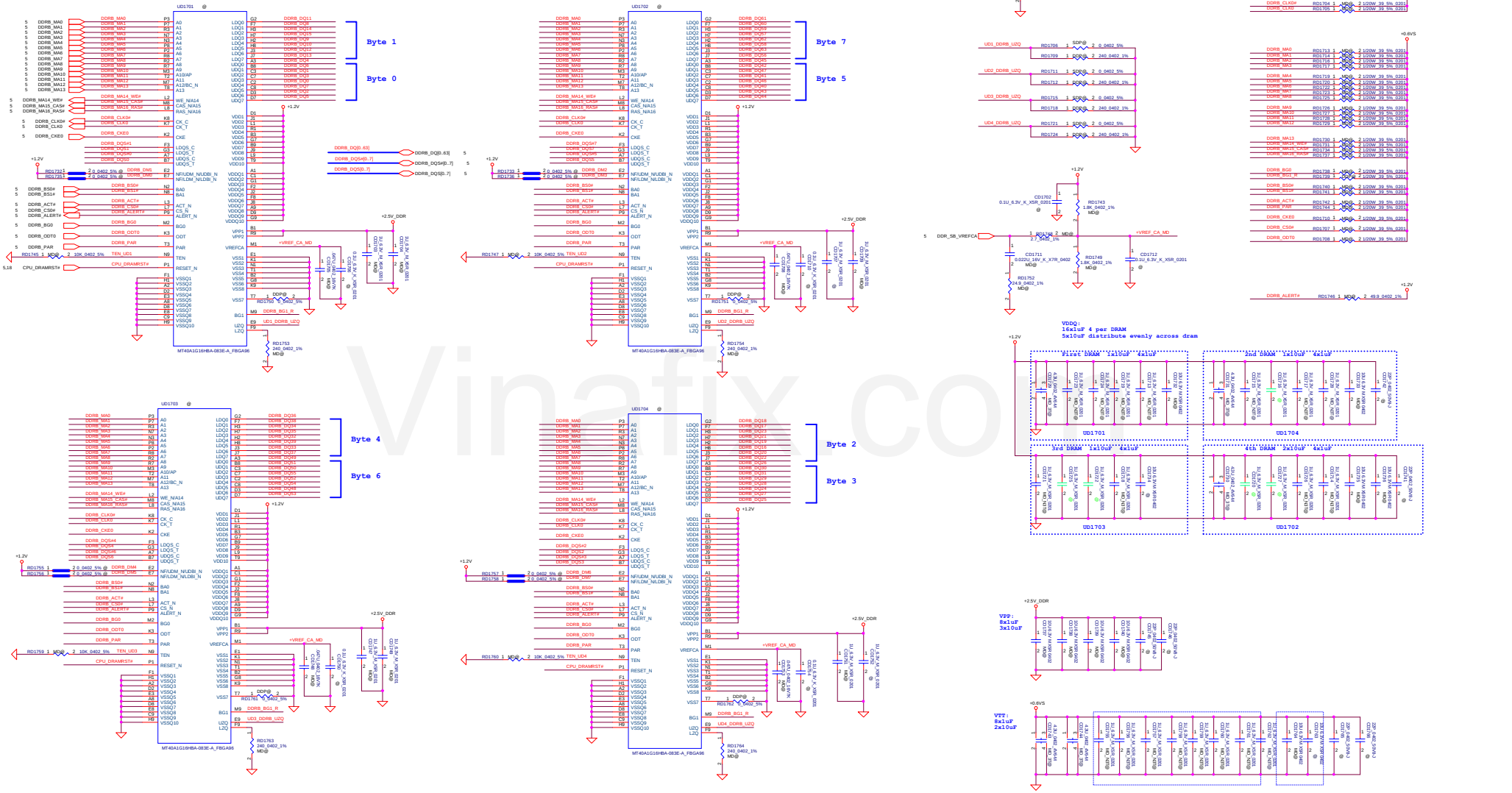
DDR4 Memory Down



Security Classification	LC Future Center Secret Data		
Issued Date	2017/06/24	Deciphered Date	2018/06/23

Title	DDR4 Memory Down		
Size	Document Number		Rev
Custom	GS44D/GS54D		0.1
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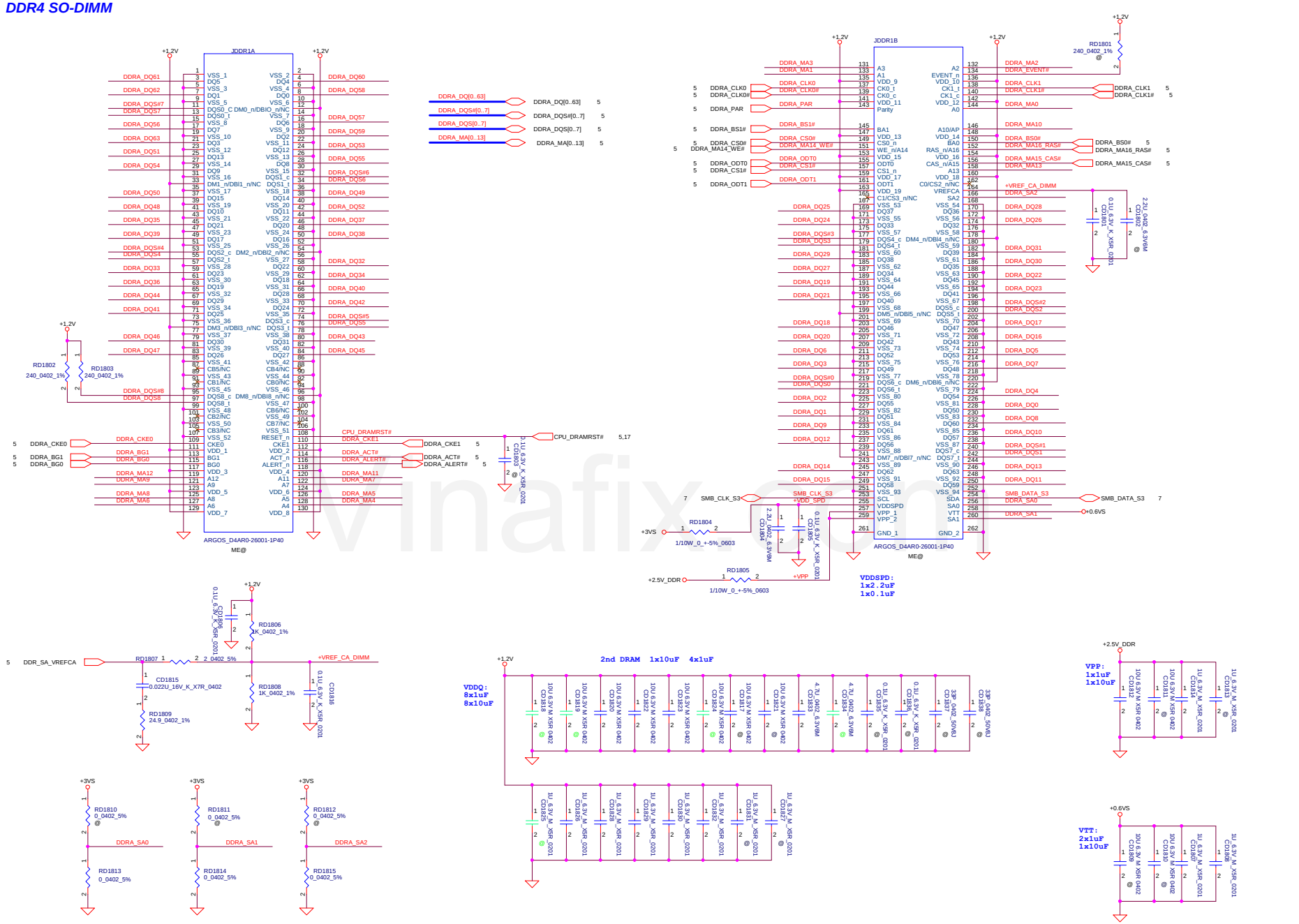
DDR4 SO-DIMM



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title	DDR4 SO-DIMM		
Size	Document Number		Rev
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N16x GPIO

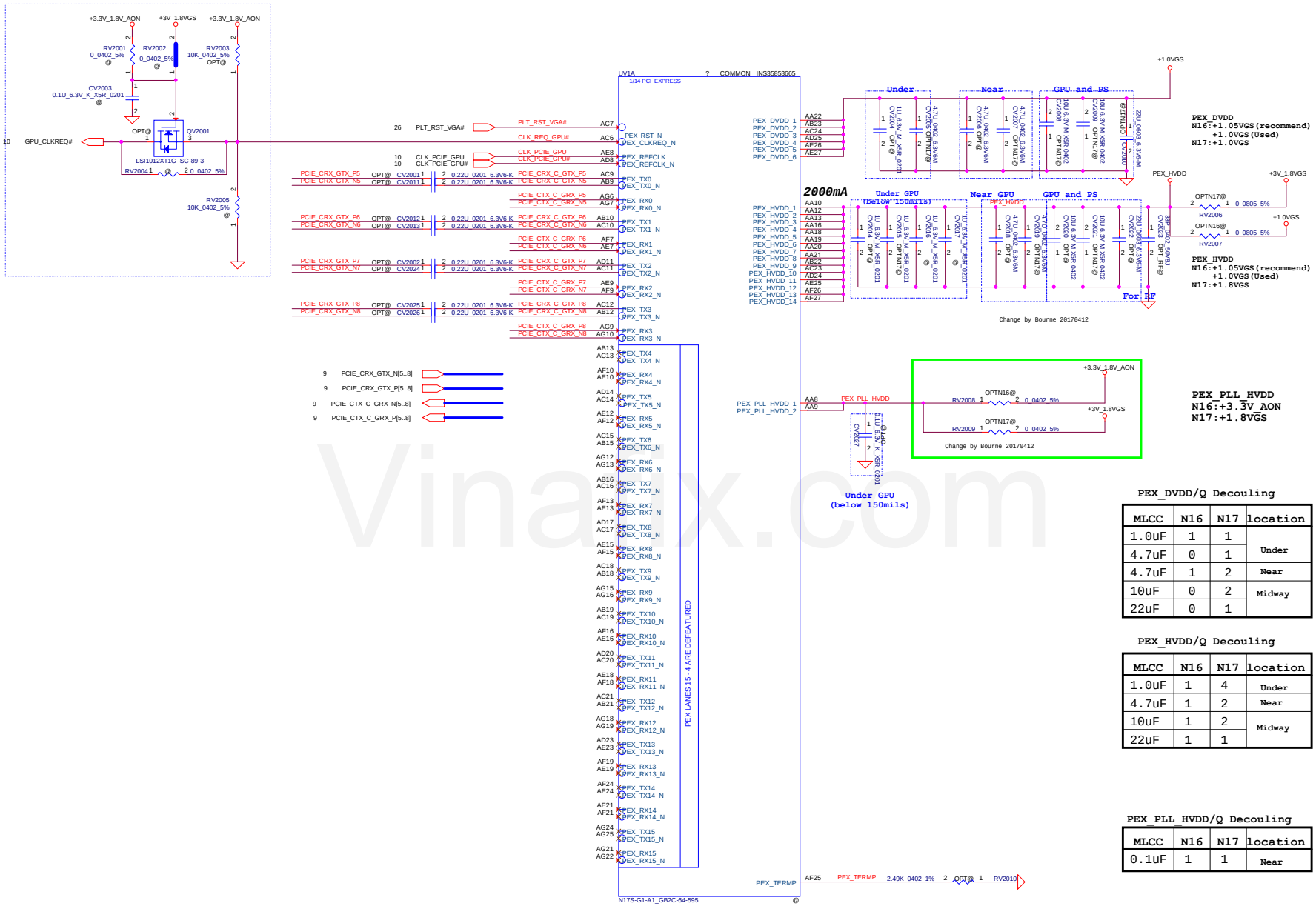
GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU Core VDD PWM control signal
GPIO1	OUT	N/A	FB Enable for GC6 2.0
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

Products	GPU (W)	Mem (W)	Min Core Clk (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	(1.05V) (6) (mA)	(1.05V) (6) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

N16x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				



PEX_DVDD/Q Decouling

MLCC	N16	N17	location
1.0uF	1	1	Under
4.7uF	0	1	
4.7uF	1	2	Near
10uF	0	2	Midway
22uF	0	1	

PEX_HVDD/Q Decouling

MLCC	N16	N17	location
1.0uF	1	4	Under
4.7uF	1	2	Near
10uF	1	2	Midway
22uF	1	1	

PEX_PLL_HVDD/Q Decouling

MLCC	N16	N17	location
0.1uF	1	1	Near

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **GPU_PCIE Interface**

Size: C	Document Number: GS44D/GS54D	Rev: 0.1
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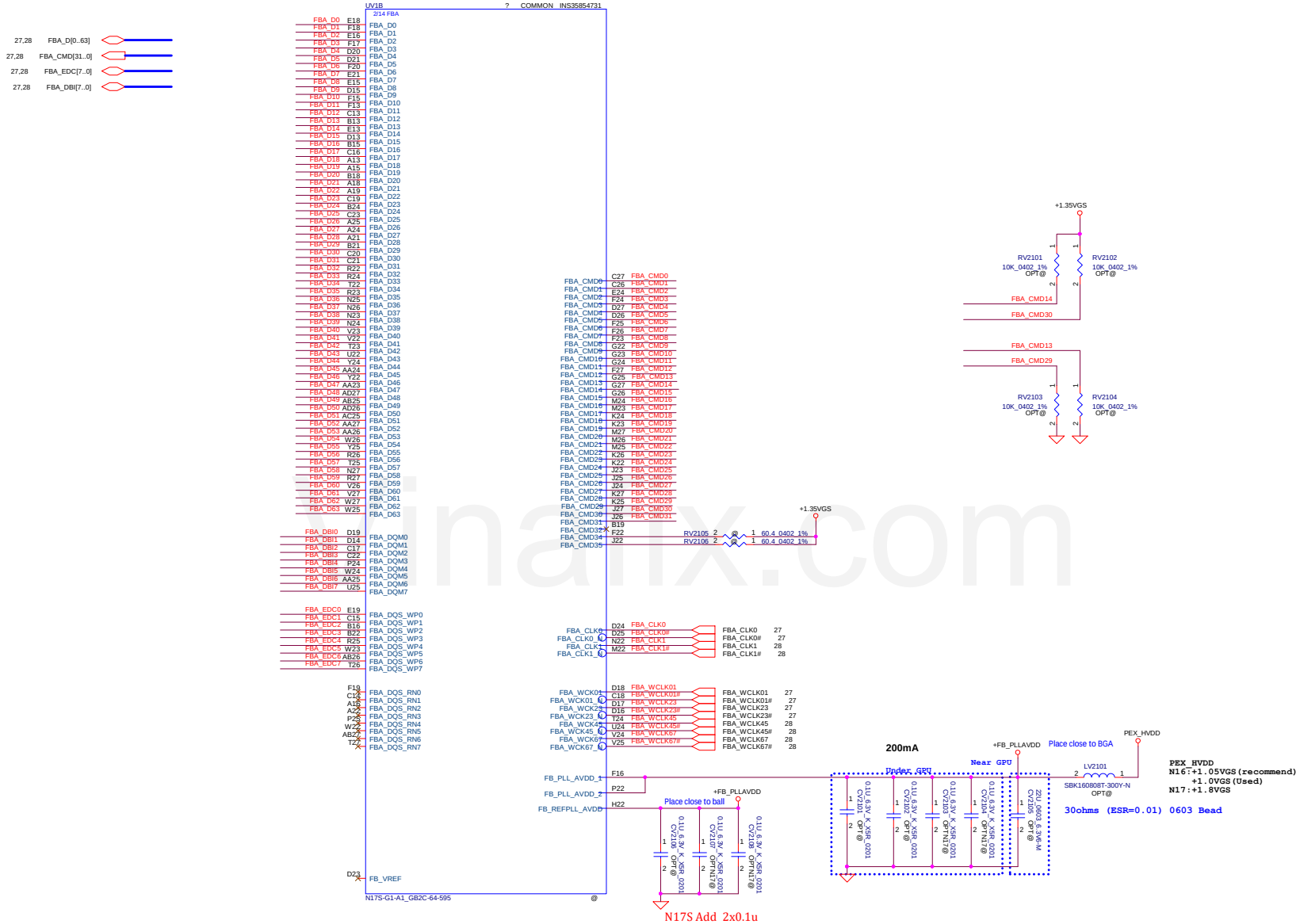

FB_PLL/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	4	Under
22uF	1	1	Near

Vinafix.com

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Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	GPU_MEM Interface		
Size C	Document Number	GS44D/GS54D	Rev 0.1
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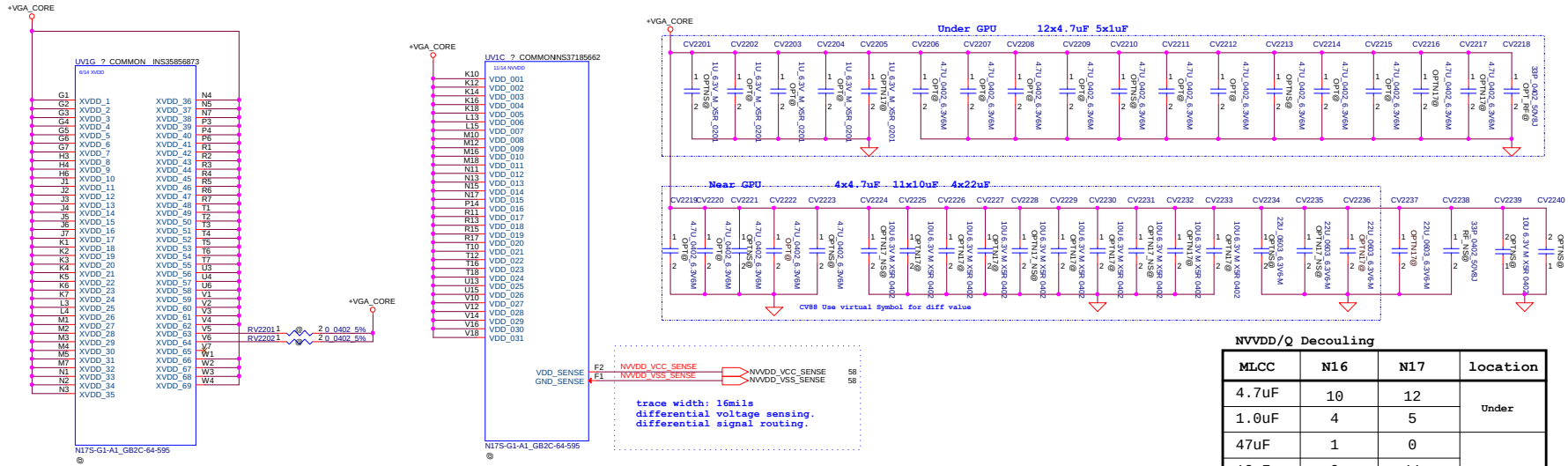
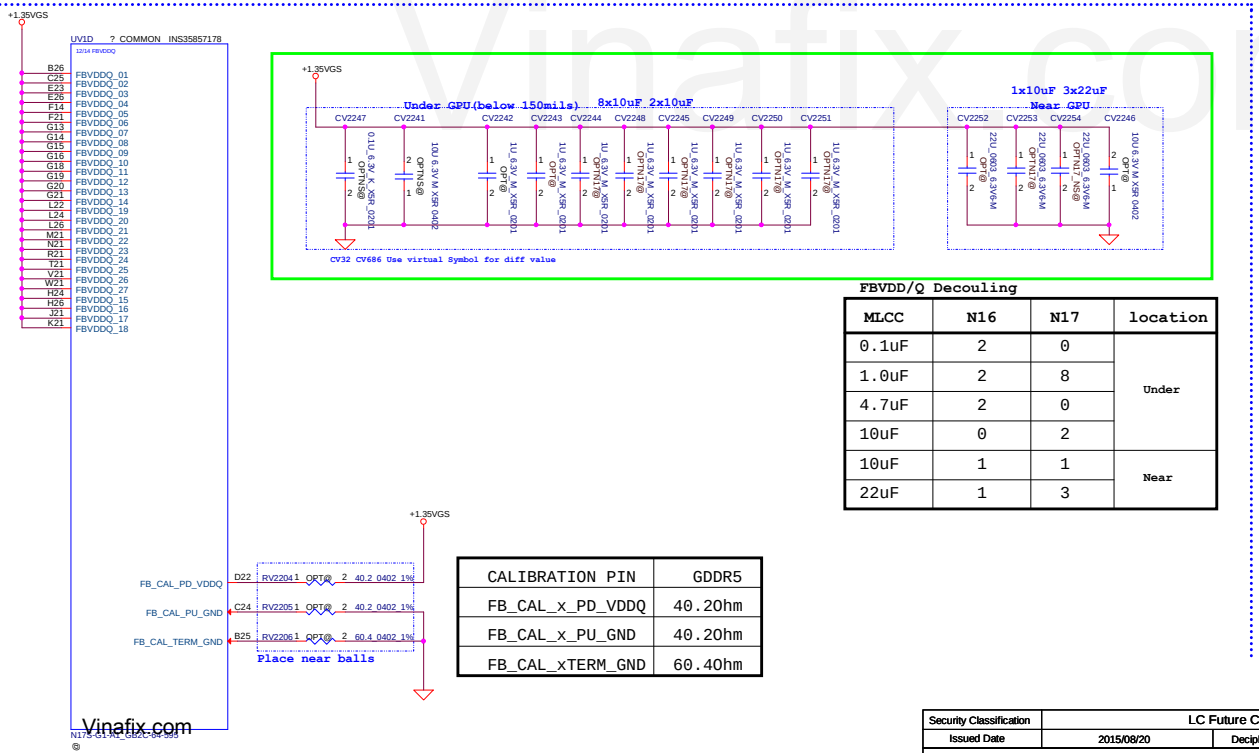


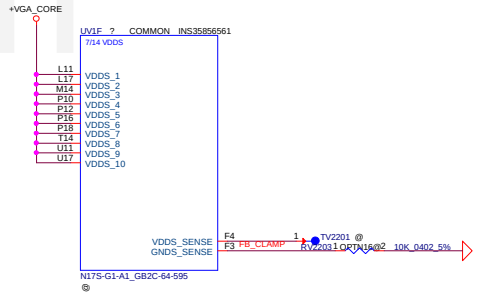
NVDD/Q Decoupling

MLCC	N16	N17	location
4.7uF	10	12	Under
1.0uF	4	5	
47uF	1	0	Near
10uF	0	11	
22uF	1	4	
4.7uF	5	4	
330uF	1	2	



FBVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	0	Under
1.0uF	2	8	
4.7uF	2	0	
10uF	0	2	
10uF	1	1	Near
22uF	1	3	



CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm

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Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title: GPU_+VGA_CORE,FBVDDQ

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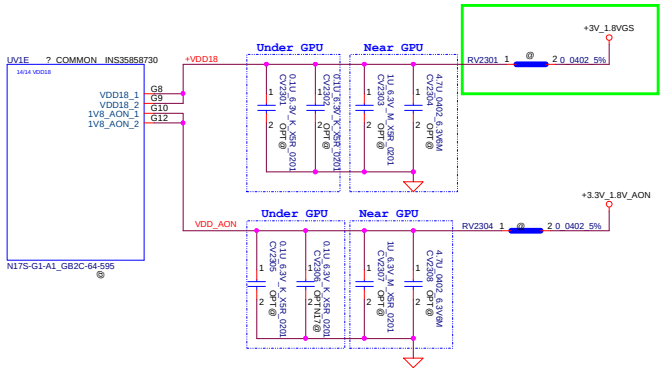


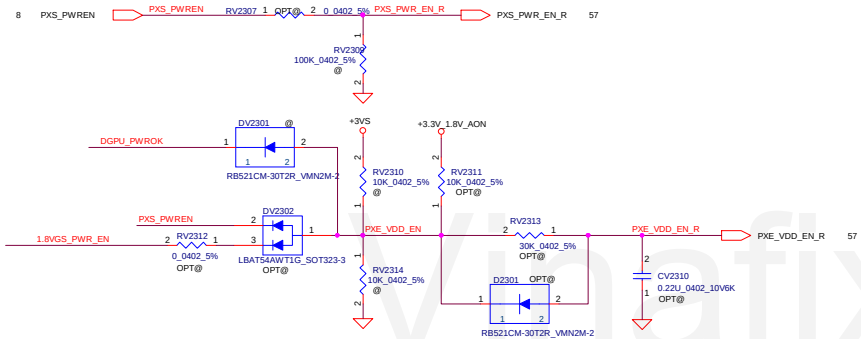
N16 3V3_MAIN(N17 VDD_18) Decouling

MLCC	N16	N17	location
0.1uF	2	2	Under
1.0uF	1	1	Near
4.7uF	1	1	

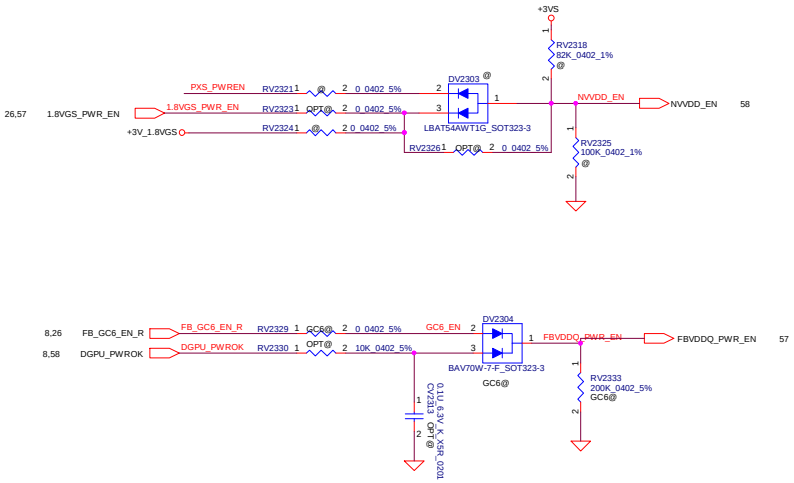
N16 3V3_AON(N17 1V8_AON) Decouling

MLCC	N16	N17	location
0.1uF	1	2	Under
1.0uF	1	1	Near
4.7uF	1	1	

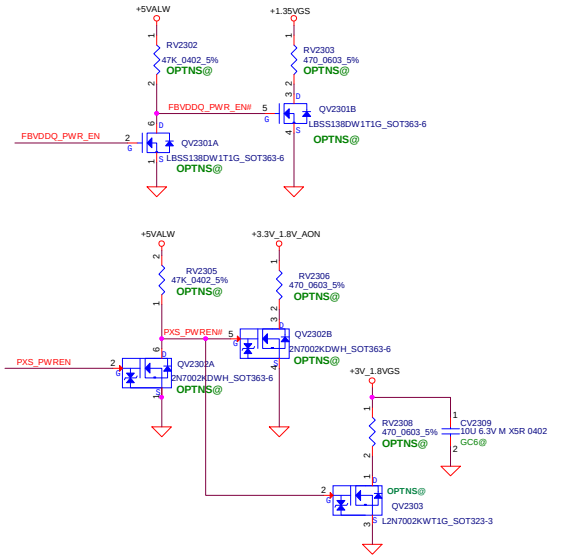
PXE_VDD & 1V8_AON



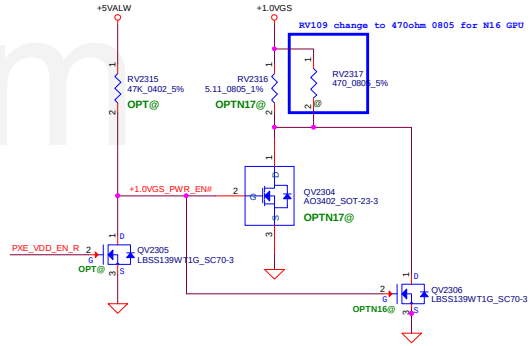
+1.8VG_AON TO +1.8VGS

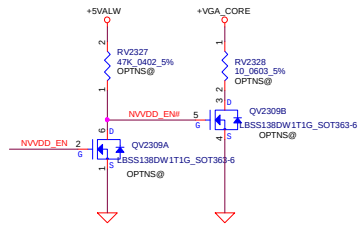


Discharge



RV2316 建虚拟料号,N16=470 ohm,N17=5.11 ohm





Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_AON/MAIN PWR/SEQ

Size	Document Number	Rev
C	GS44D/GS54D	0.1

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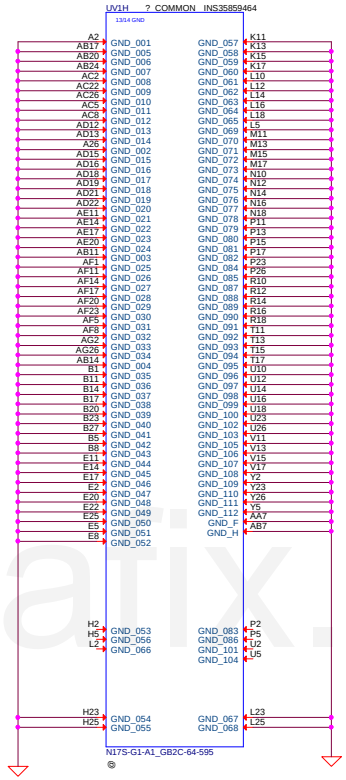

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **GPU_GND**

Size: C	Document Number: GS44D/GS54D	Rev: 0.1
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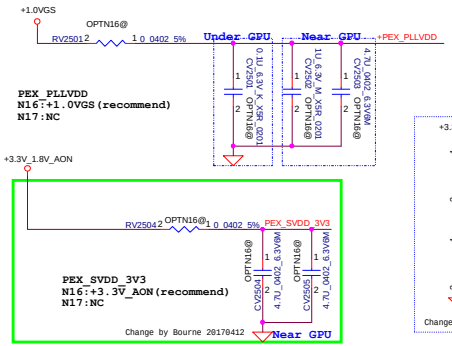
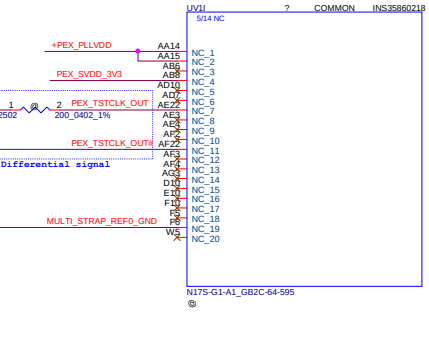
PEX_PLLVDD/Q Decouling

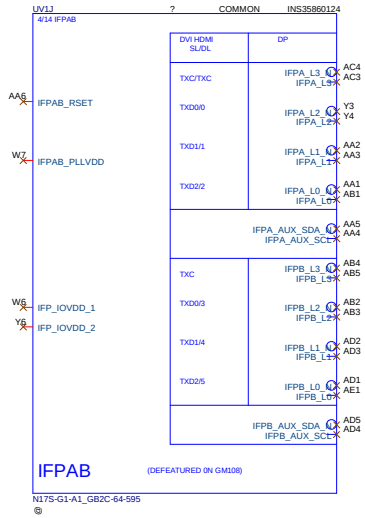
MLCC	N16	N17	location
1.0uF	1	NA	Under
1uF	1	NA	Near
4.7uF	1	NA	

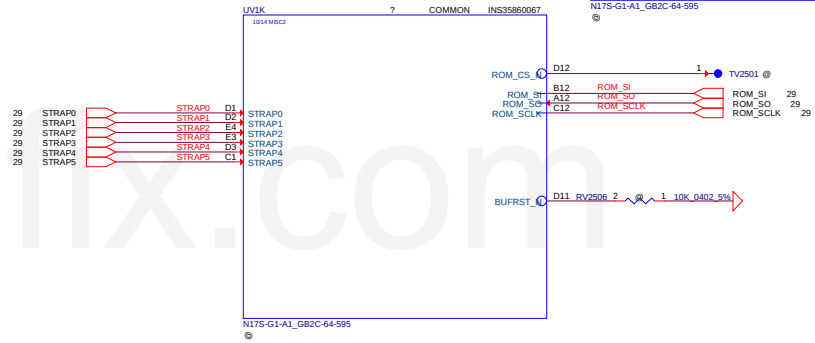


PEX_SVDD/Q Decouling

MLCC	N16	N17	location
4.7uF	2	NA	Near

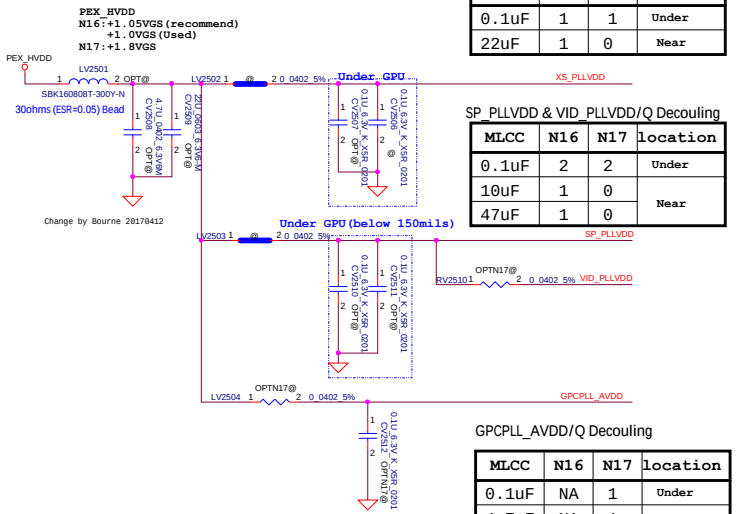






XS_PLLVDD/Q Decouling

MLCC	N16	N17	location
0.1uF	1	1	Under
22uF	1	0	Near

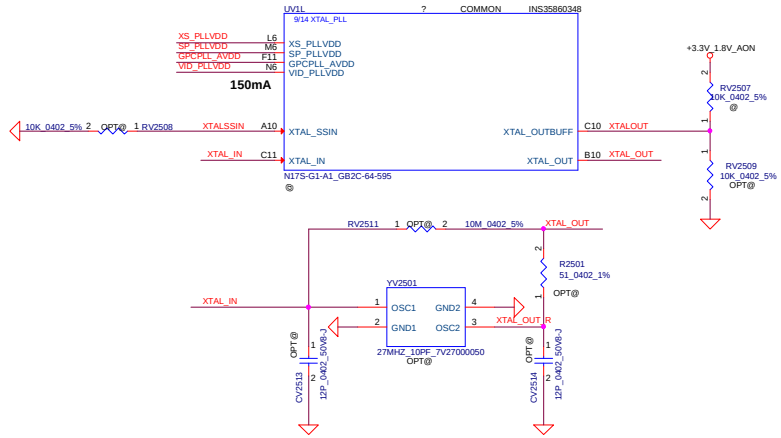


SP_PLLVDD & VID_PLLVDD/Q Decouling

MLCC	N16	N17	location
0.1uF	2	2	Under
10uF	1	0	Near
47uF	1	0	

GPCPLL_AVDD/Q Decouling

MLCC	N16	N17	location
0.1uF	NA	1	Under
4.7uF	NA	1	Near
22uF	NA	1	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	GPU_STRAP/DP/HDMI		
Size C	Document Number	GS44D/GS54D	Rev 0.1
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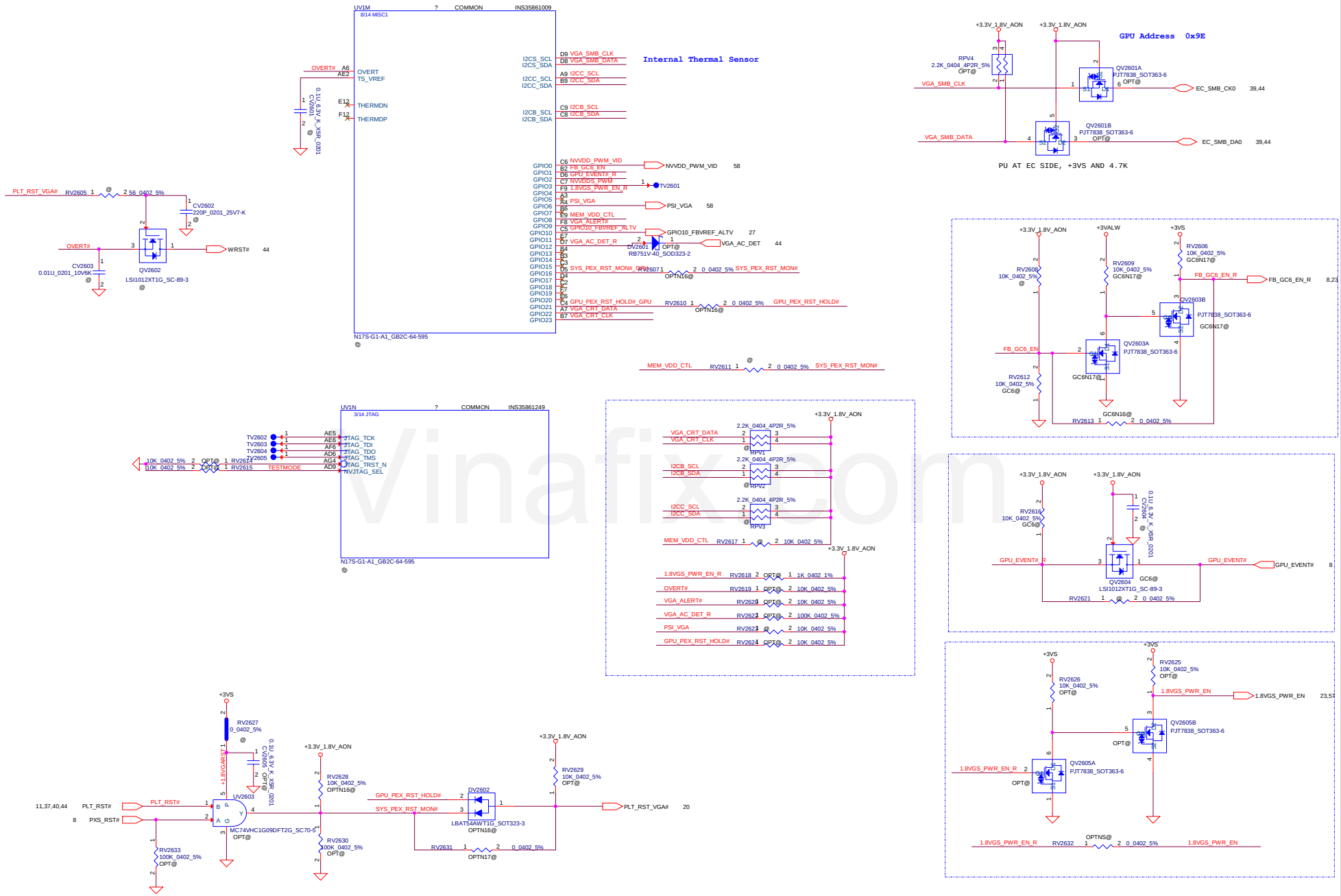

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	GPU_GPIO/JTAG		
Size C	Document Number GS44D/GS54D		Rev 0.1
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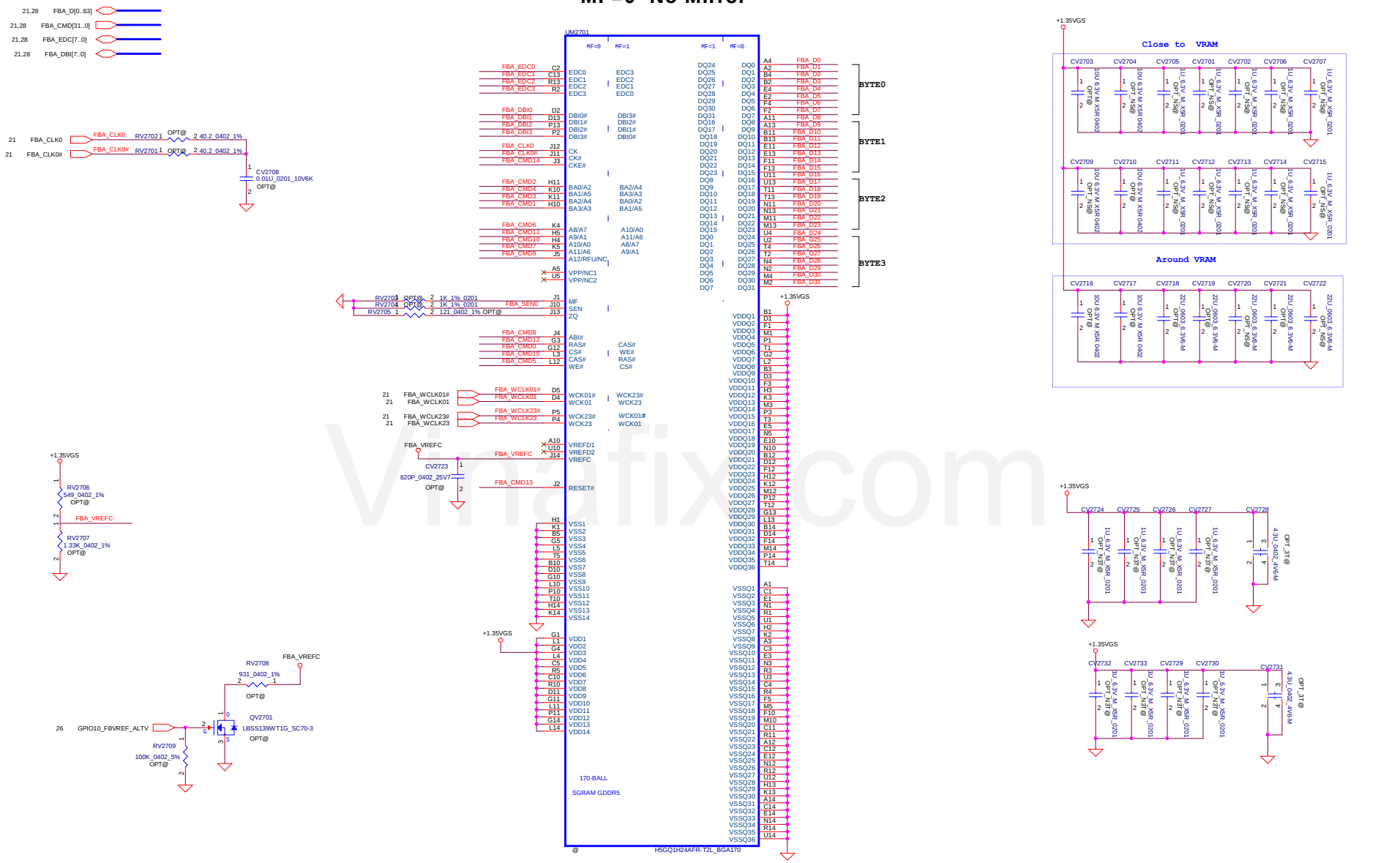
Lower 32 bits

MF=0 No Mirror

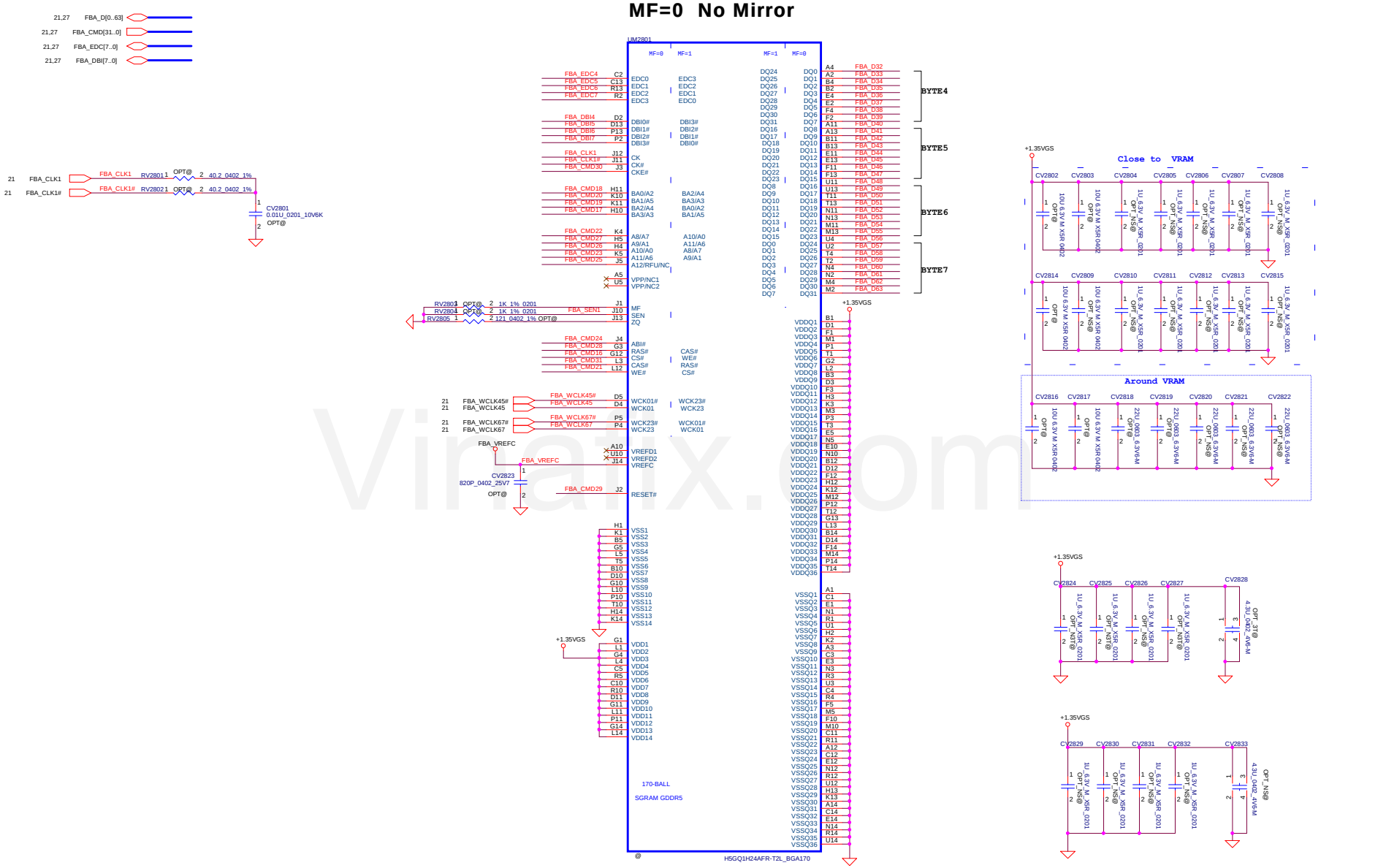


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	GPU_GDDR5_Rank0_[31:0]		
Size C	Document Number GS44D/GS54D		Rev 0.1
Date: Tuesday, July 30, 2019	Sheet 27 of 60		

upper 32 bits

MF=0 No Mirror



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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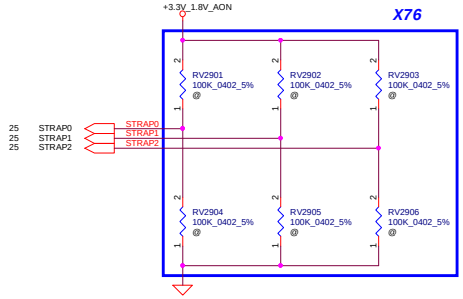
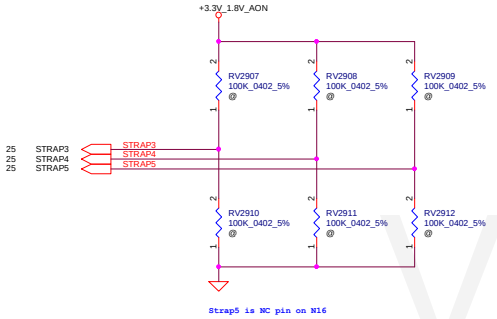
Title	GPU_GDDR5_Rank0_[64:32]		
Size C	Document Number GS44D/GS54D		Rev 0.1
Date: Tuesday, July 30, 2019	Sheet 28 of 60		



GPU	FB Memory (GDDR5)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	K4G80325FB-HC28	0(0x0000)	L	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1(0x0001)	L	L	H
	Hynix 8Gb	H5GC8H24MJR-R0C	2(0x0010)	L	H	L



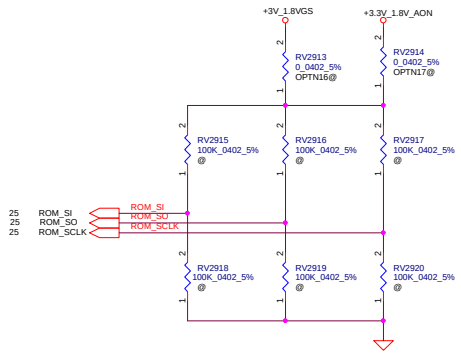
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE



	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N17S-G1	H	H	M	0000
N16S-GTR				

1:ENABLE 0:DISABLE

SOR0/1/2/3 DISABLE

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_MISC

Size	Document Number	Rev
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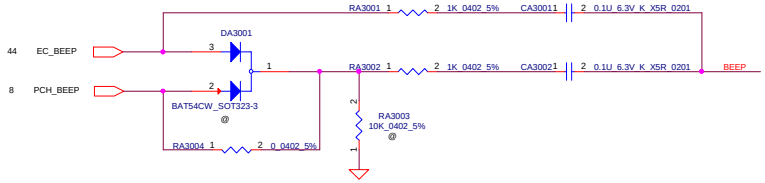
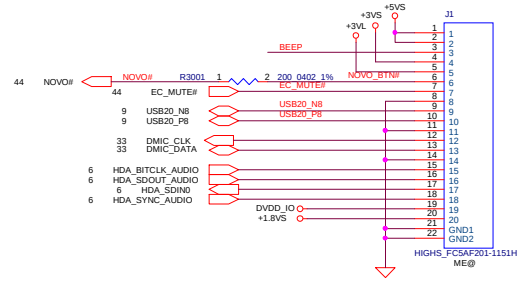
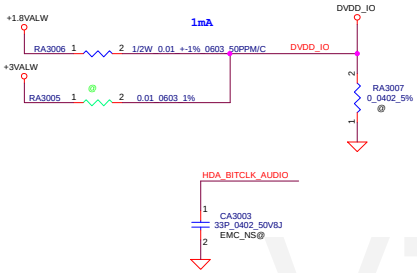
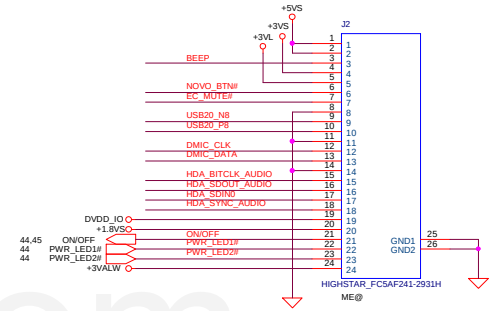
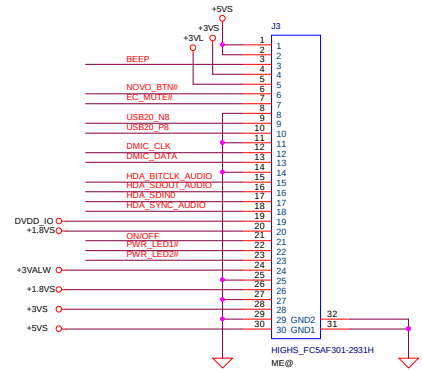




CPU HDA BUS power 1.8VALW







Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: ***Blank***

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Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title **TPM**

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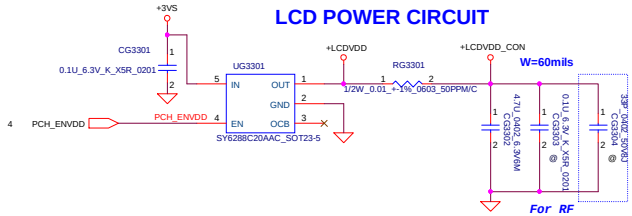
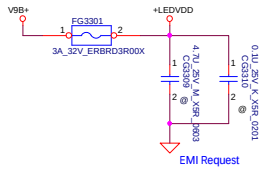
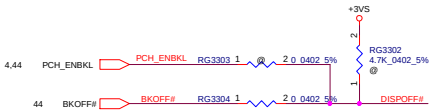
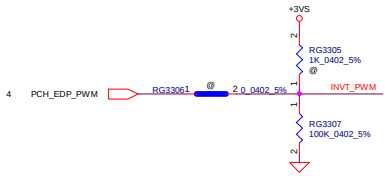
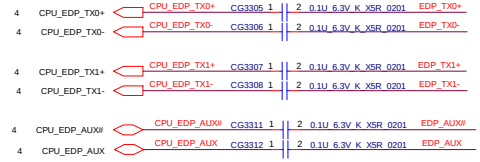
LCD POWER CIRCUIT

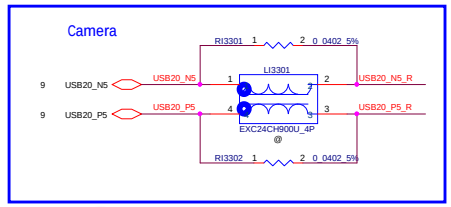


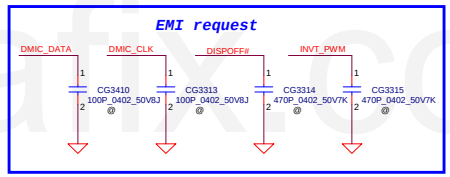




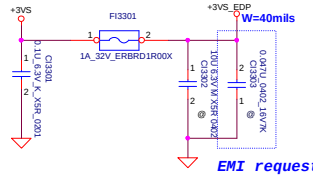


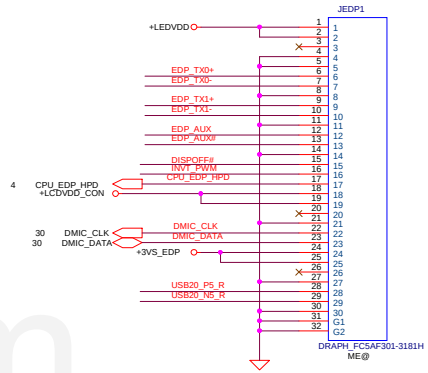




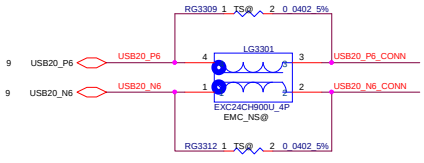


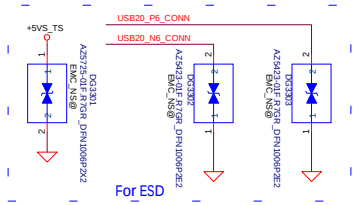
CMOS Camera

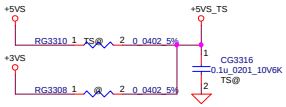


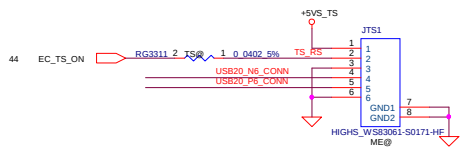


Touch Screen









Security Classification	LC Future Center Secret Data		
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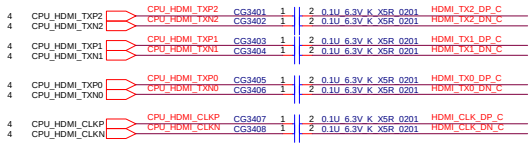
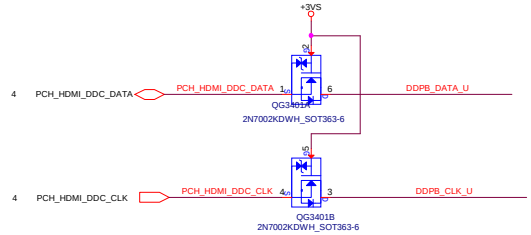
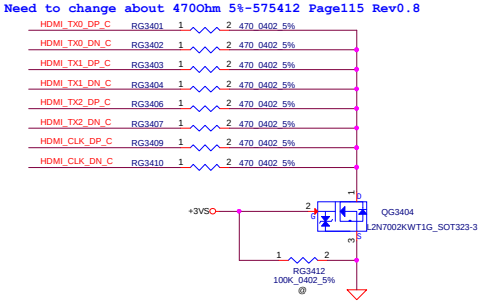
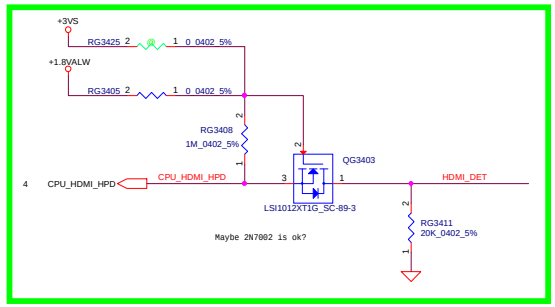
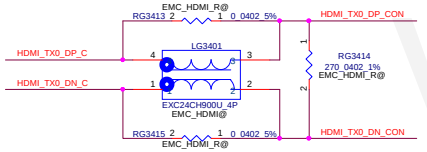


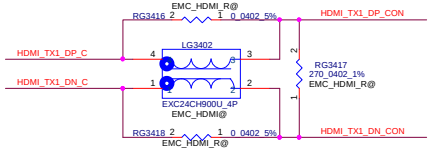


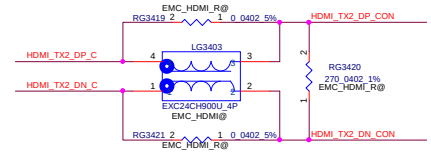
Need to change about 470Ohm 5%-575412 Page115 Rev0.8

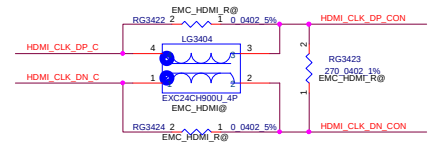




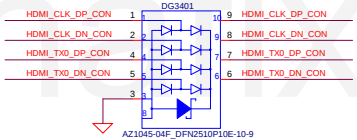


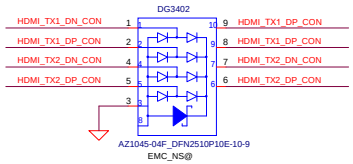


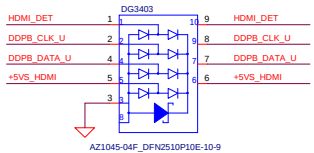




For EMC

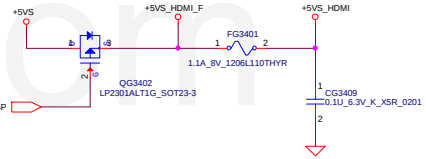


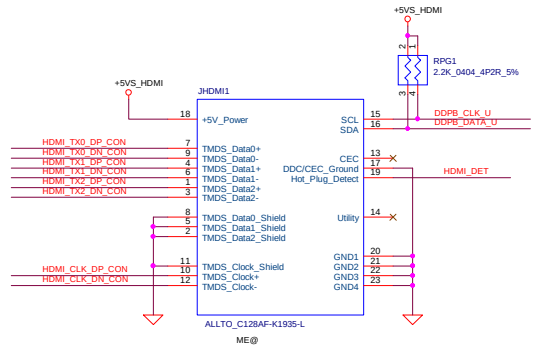




For EMC

F1 use 1.1A





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Title	HDMI_CONN		
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Title: ***Blank***

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Title

HALL Sensor

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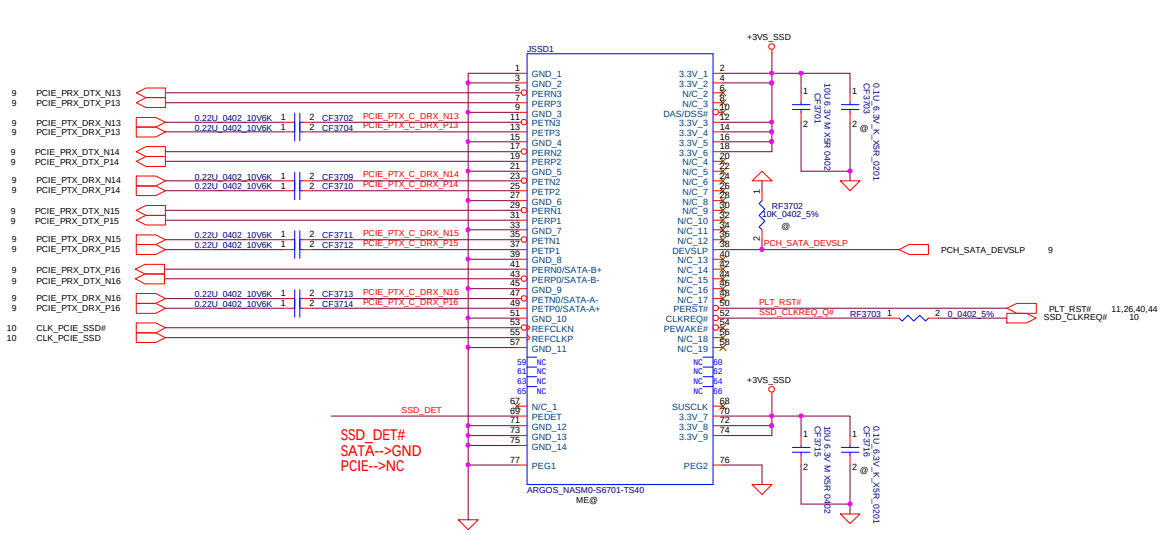
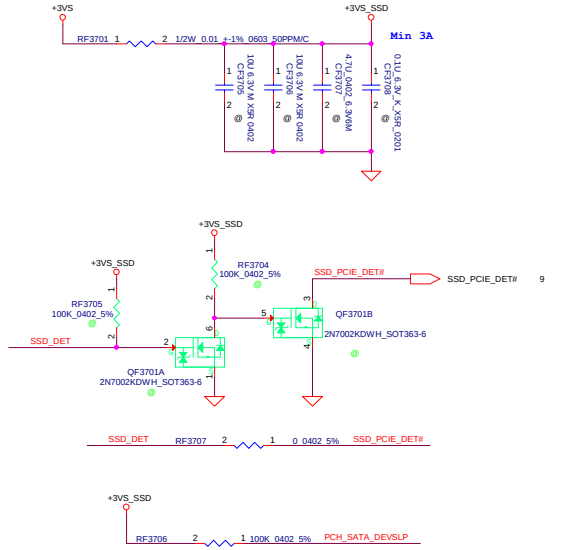
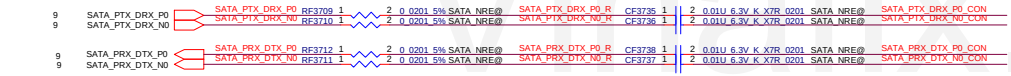
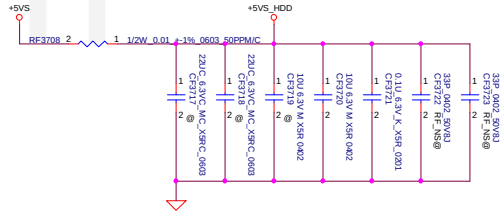
M.2 SSD



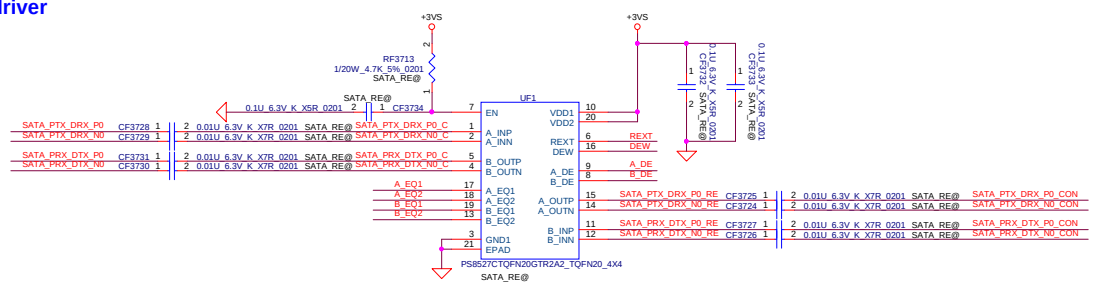


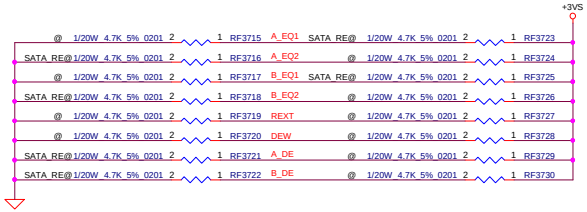
SATA

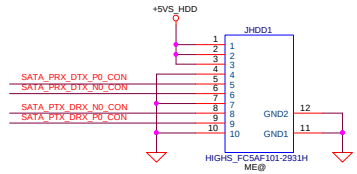




SATA Redriver







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Title: **SATA HDD CONN**

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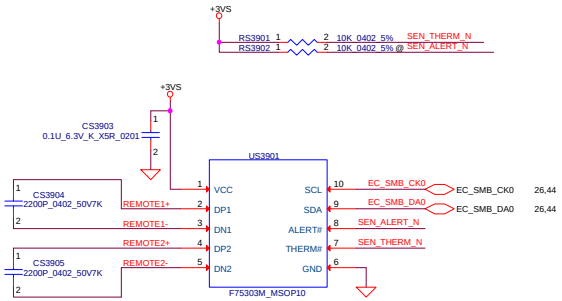
SMSC thermal sensor



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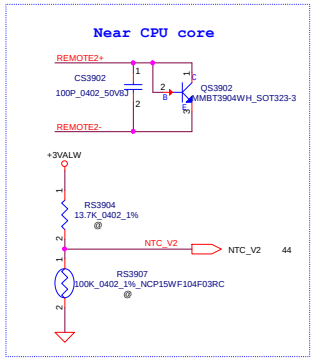
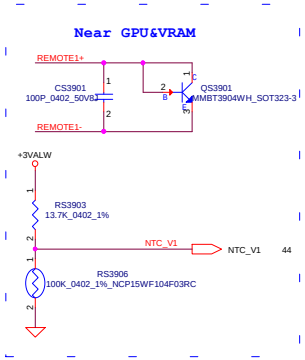
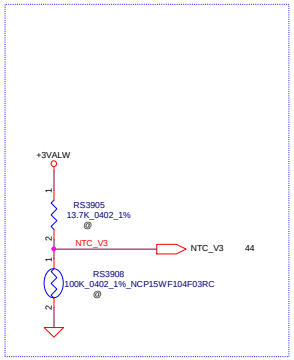
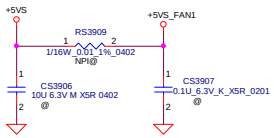
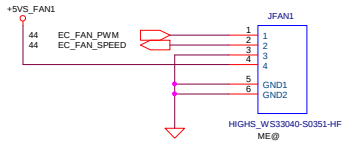






FAN Conn





Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title	Thermal sensor/FAN CONN		
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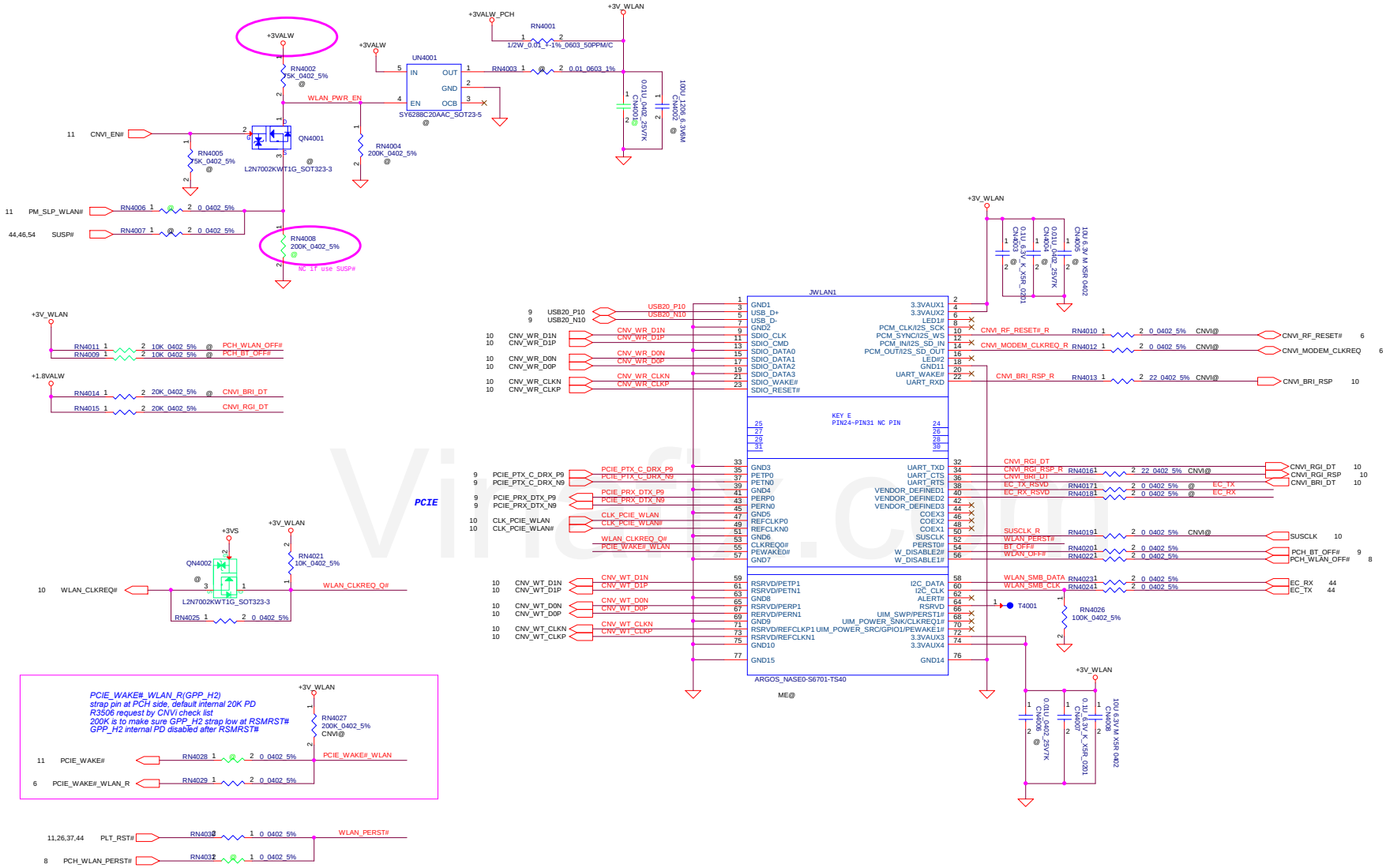
Mini-Express Card(WLAN/WiMAX)



Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

Title	NGFF_WLAN
Size	C
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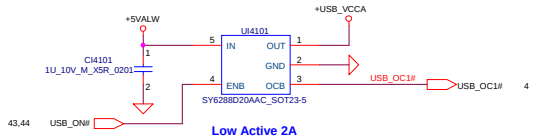
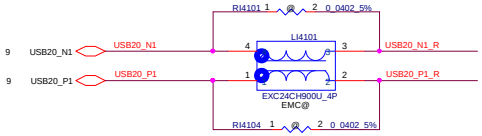
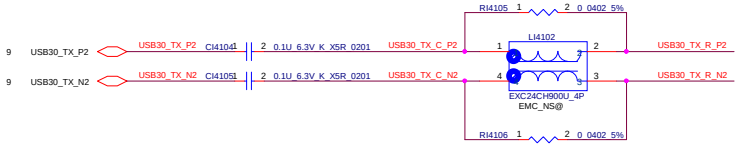
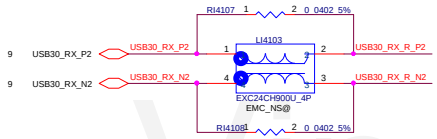
USB3.0 Port1

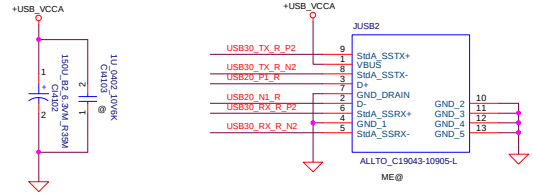


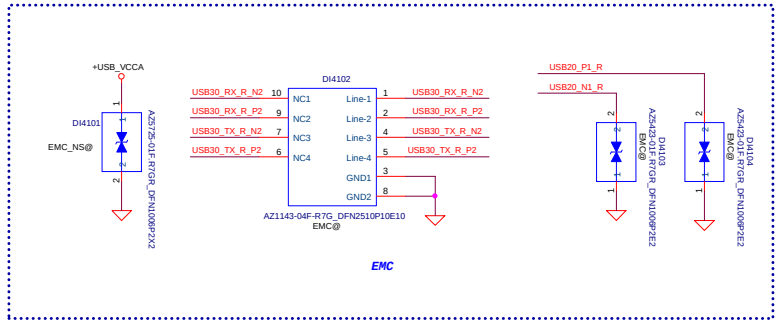
Low Active 2A



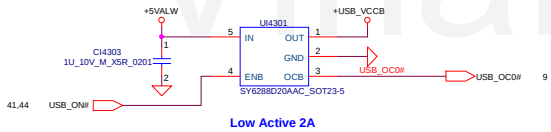




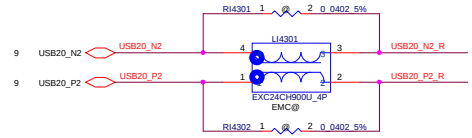


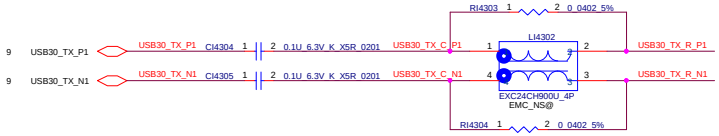


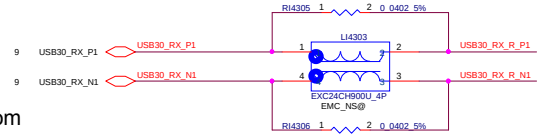
USB3.0 Port2

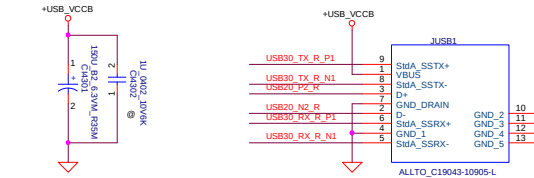


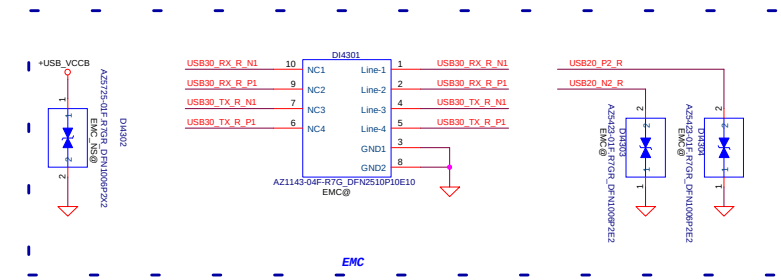
Low Active 2A











Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	USB3 PORT_LEFT		
Size	Document Number		Rev
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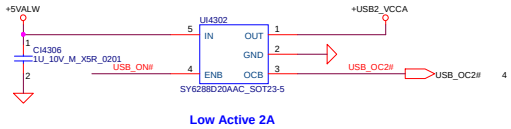
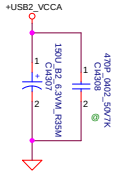
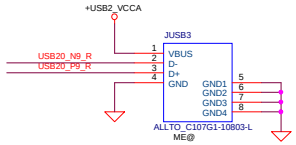
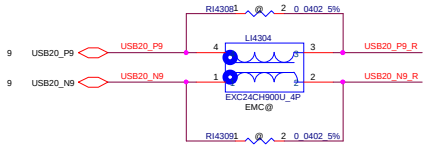
USB2.0 PORT x1

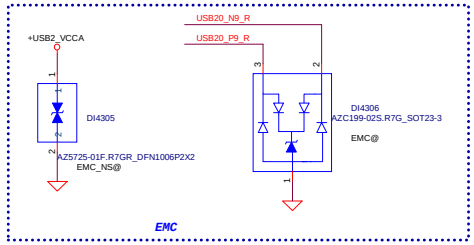


Low Active 2A









Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	USB3 Port_Right & USB2.0		
Size: C	Document Number: GS44D/GS54D		Rev: 0.1
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Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: ***Blank***

Size: C	Document Number: ***GS44D/GS54D***	Rev: 0.1
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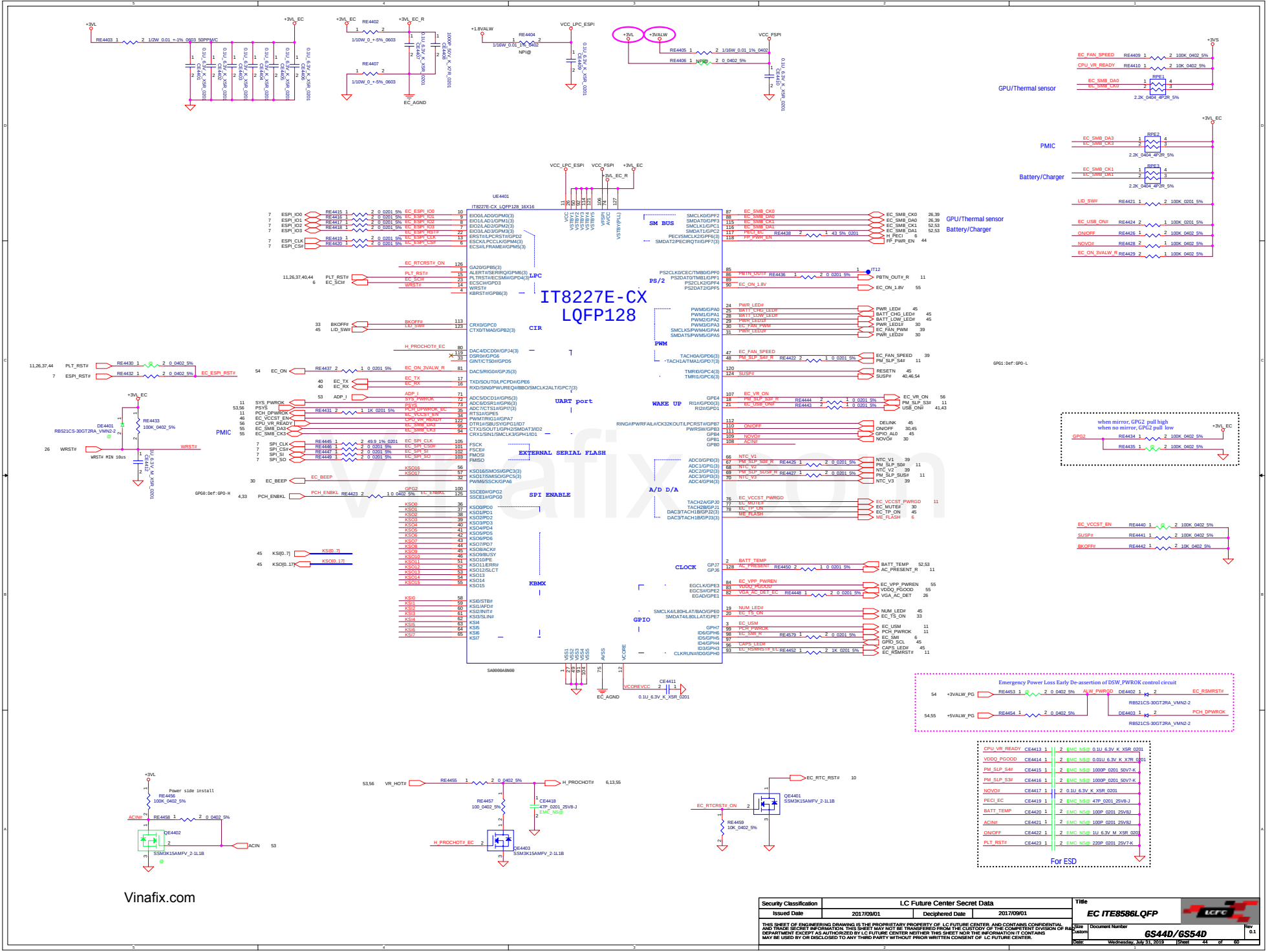

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Issued Date	2017/09/01	Deciphered Date	2017/09/01

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Size: Custom | Document Number: GS44D/6S54D | Rev: 0.1

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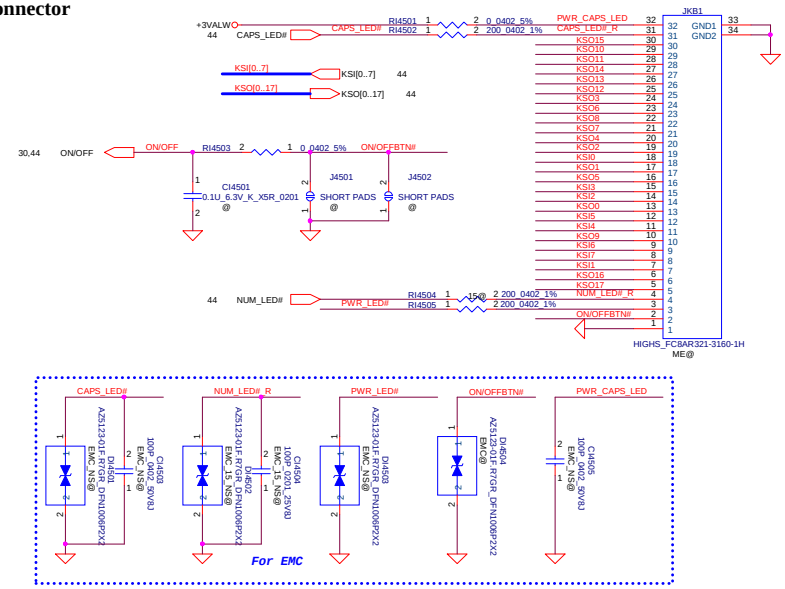
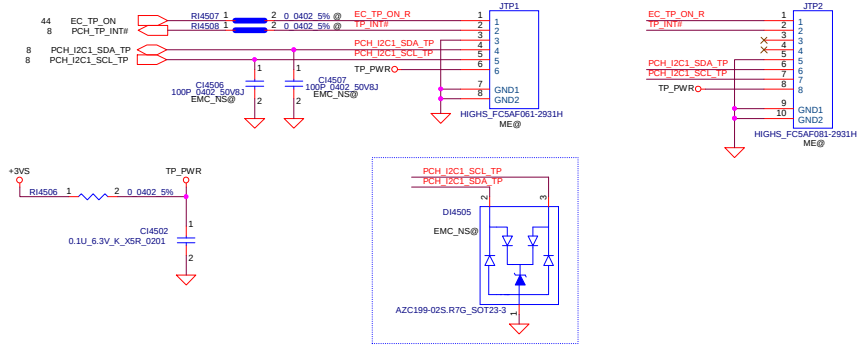
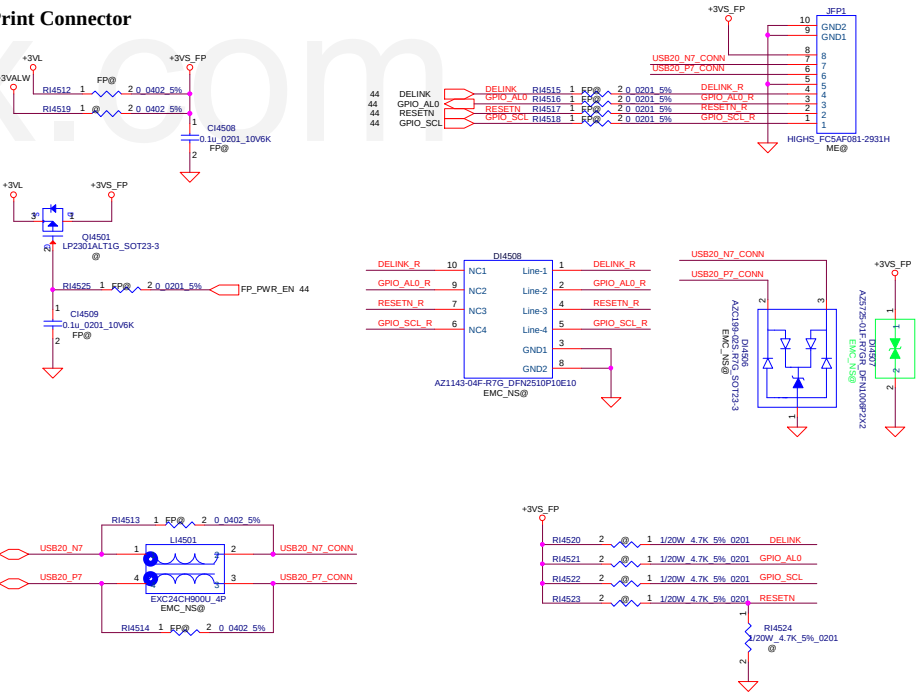
K/B Connector



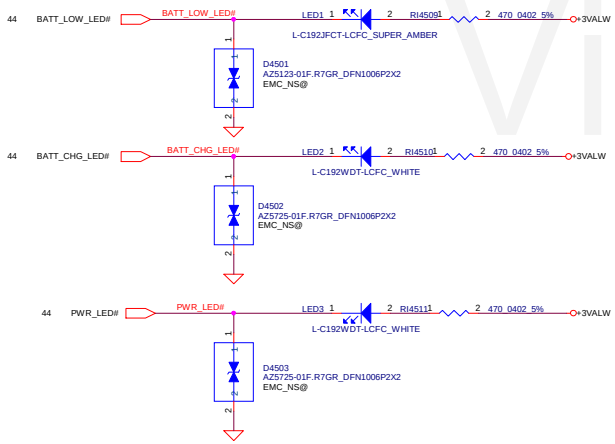
TP/B Connector



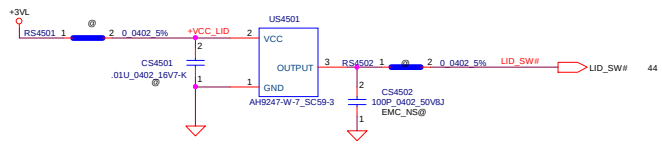
Finger Print Connector



LED



HALL Sensor

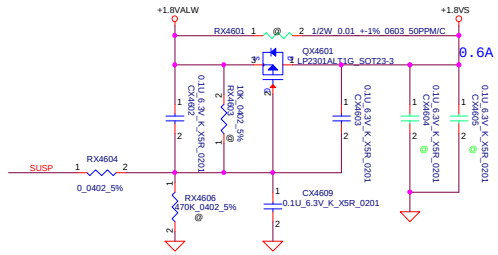


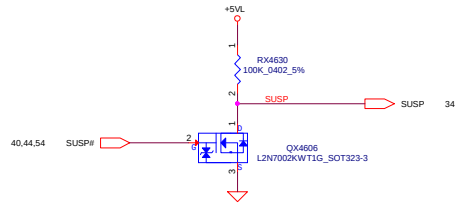
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	KB/TP_CONN.		
Size C	Document Number	GS44D/GS54D	Rev 0.1
Date:	Wednesday, July 31, 2019	Sheet 45 of 60	

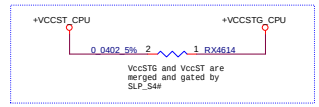
+3VALW to PCH

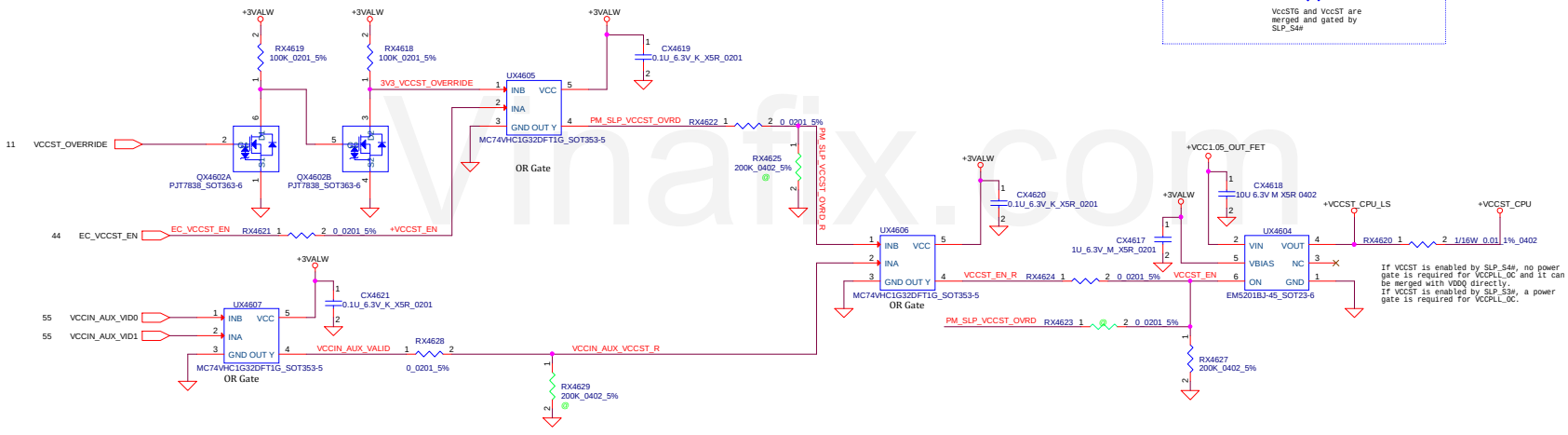
+1.8VALW to +1.8VS





VCCST&VCCSTG





Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	DC V TO VS INTERFACE		
Size C	Document Number GS44D/GS54D		Rev 0.1
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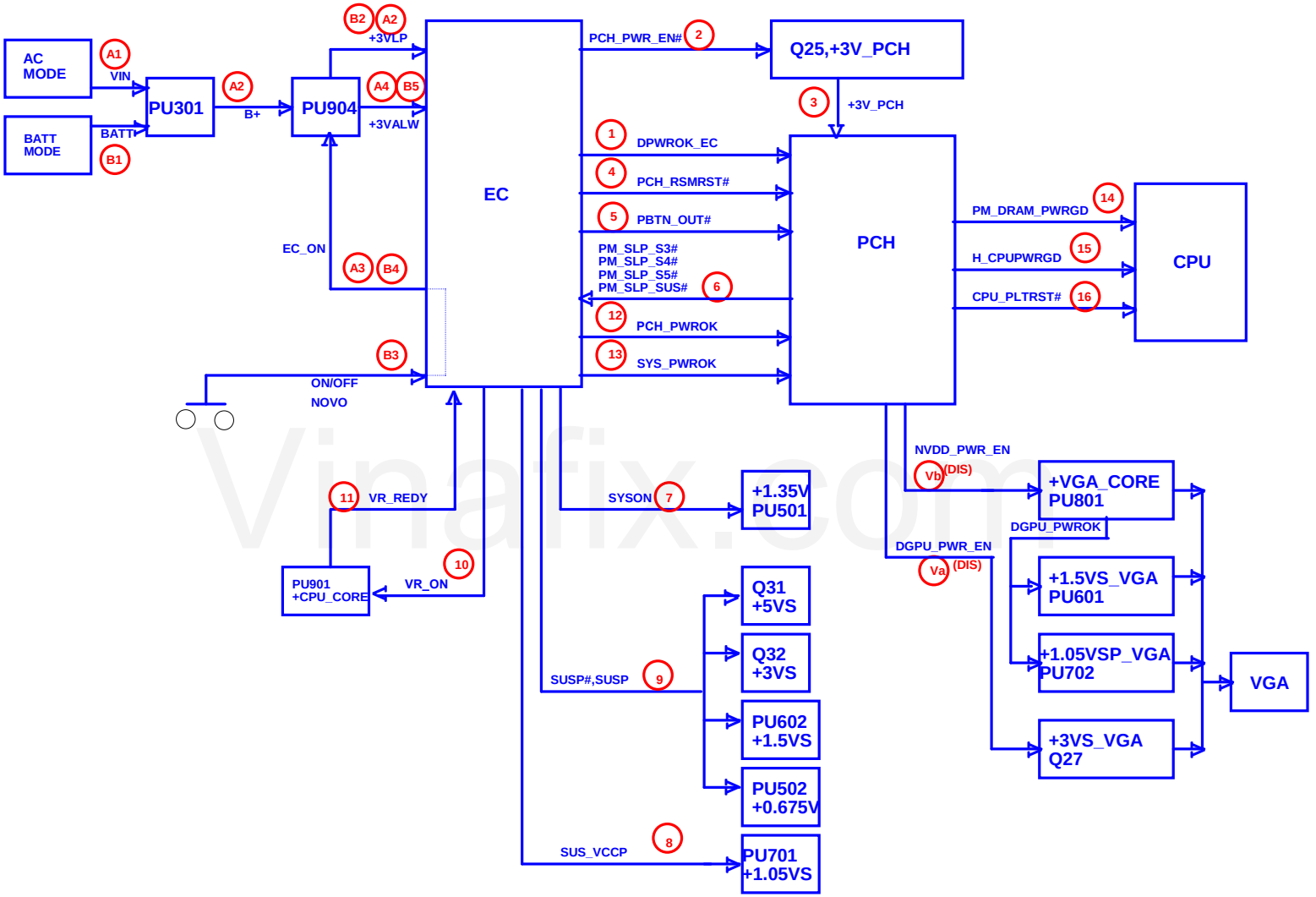

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Power sequence block**

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CPU

UC1	1035G4@	UC1	1035G1@	UC1	1005G1@	UC1	1065G7@
MP PN		MP PN		MP PN		MP PN	
Intel i5-1035G4 1.1G/4C		Intel i5-1035G1 1G/4C/6M		Intel i3-1005G1 1.2G/2C/4M		Intel i7-1065G7 1.3G/4C/8M	
SA0000A4T20		SA0000A8W30		SA0000A9V10		SA0000A4U10	

GPU

RV2317	OPTN17@	RV2317	OPTN16@
5.11_0805_1%		470_0805_5%	
SD00001NQ00		SD00247008J	

VRAM

DRAM_Samsung

ZZZ1	SAM_DRAM@
D4G SAM	
X7648112001	

DRAM_Hynix

ZZZ1	Hyn_DRAM@
HYNIX D4G	
X7648112002	

DRAM_Micron

ZZZ1	Mic_DRAM@
D4G MIC	
X7648112003	

SO_DIMM only

PCB_MB

ZZZ
NM-C711
DA600016F00

HDMI Royalty

ZZZ2	HDMI@
HDMI PN	
RO000000040J	

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: ***Virtual symbol***

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PCB Fedical Mark PAD

FD4901 FD4902 FD4903 FD4904 FD4905 FD4906

CPU Thermal Hole

H4902 HOLEA — PAD_CT7P0B6P0D3P2
H4904 HOLEA — PAD_CT7P0B6P0D3P2
H4906 HOLEA — PAD_CT7P0B6P0D3P2
H4907 HOLEA — PAD_CT7P0B6P0D3P2

GPU Thermal Hole

H4903 HOLEA — PAD_CT7P0B6P0D3P2
H4905 HOLEA — PAD_CT7P0B6P0D3P2

H4908 HOLEA — PAD_C7P0D4P0
H4909 HOLEA — PAD_C7P0D4P0
H4910 HOLEA — PAD_O2P5X3P0D2P5X3P0N
H4911 HOLEA — PAD_O2P5X3P0D2P5X3P0N

H4912 HOLEA — PAD_C7P0D2P8
H4913 HOLEA — PAD_C7P0D2P8
H4914 HOLEA — PAD_C7P0D2P8
H4901 HOLEA — PAD_C10P0D8P0

H4915 HOLEA — PAD_C7P0D2P4
H4916 HOLEA — PAD_CT7P0B10P0D4P0
H4917 HOLEA — PAD_CT7P0B10P0D4P0

Vinafix.com

MD Shielding

SH4901 SH4902 SH4903 SH4904 SH4905 SH4906

SPRING_FINGER_6.2X1.64 (×6)

SODIMM Shielding

SH4907 SH4908 SH4909 SH4910 SH4911

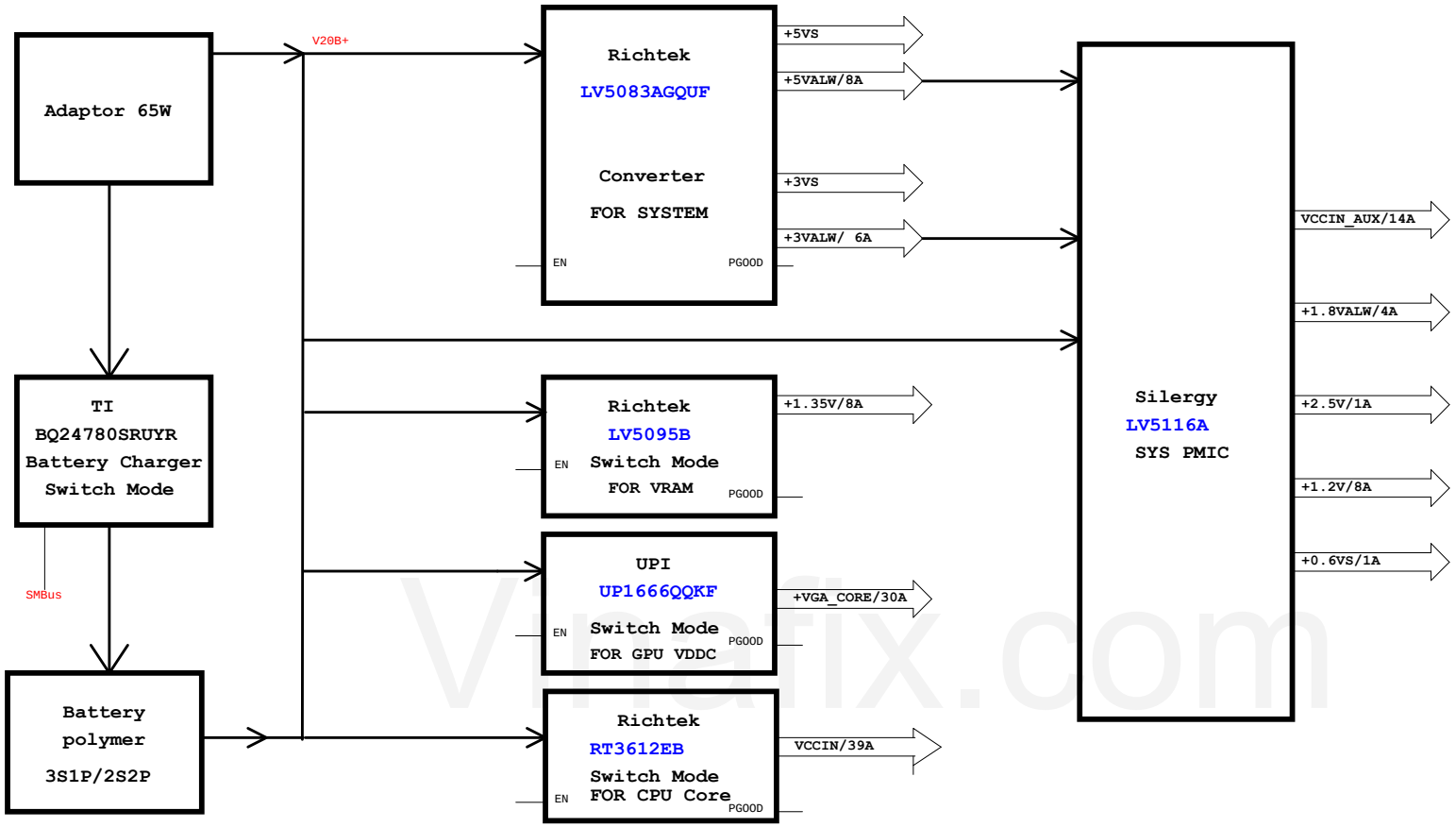
SHIELDING_SUL-35A2M_9P2X3P3_1P (×5)

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Hole**

Size	Document Number	Rev
B	GS44D/GS54D	0.1

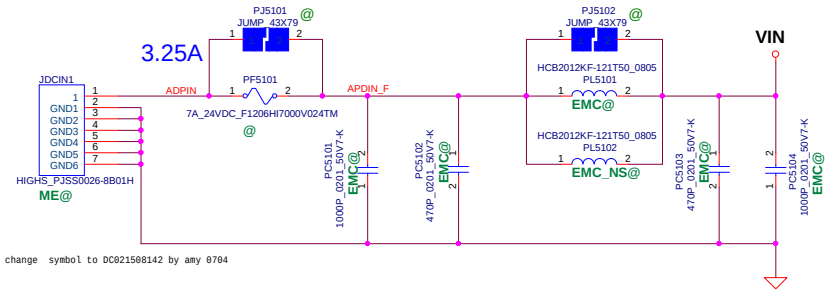
Date: Tuesday, July 30, 2019 Sheet 49 of 60

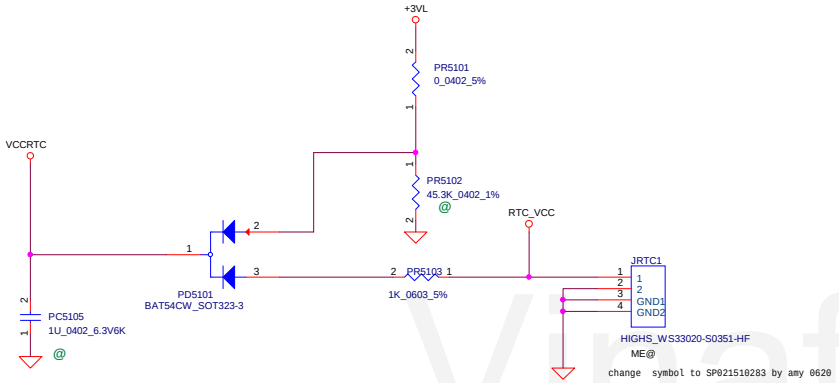


Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-Power Diagram

Size: C	Document Number: GS44D/GS54D	Rev: 0.3
Date: Tuesday, July 30, 2019	Sheet 50 of 60	





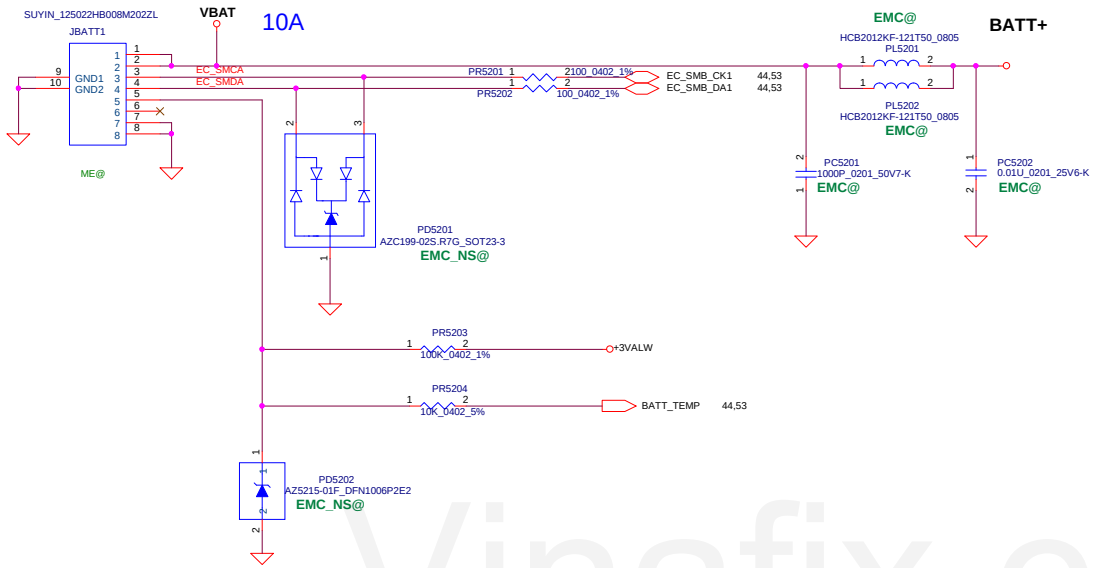
RTC_VCC 20MIL
+3VL 20MIL
VCCRTC 20MIL

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-DCIN / RTC charger

Size: Custom | Document Number: GS44D/GS54D | Rev: 0.3

Date: Tuesday, July 30, 2019 | Sheet 51 of 60



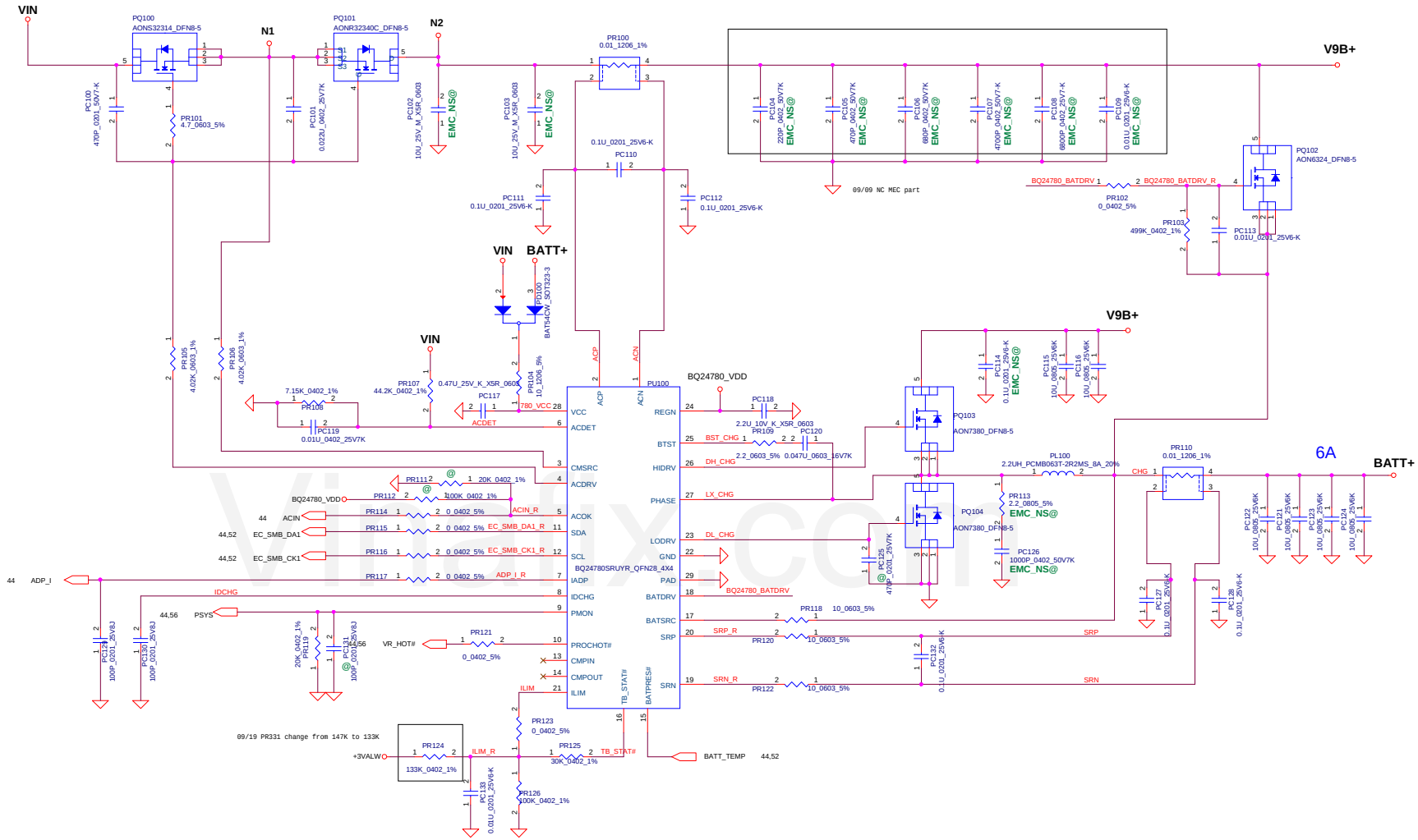
2S1P polymer battery voltage level: +5.5V ~ 8.8 V

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-BATTERY CONN/OTP

Size	Document Number	Rev
Custom	GS44D/GS54D	0.3

Date: Tuesday, July 30, 2019 Sheet 52 of 60



ACDECT setting 17.2V
Charge current limit HW=7A
DC discharge limit =26A
Discharge current limit HW=9A during Turbo boost

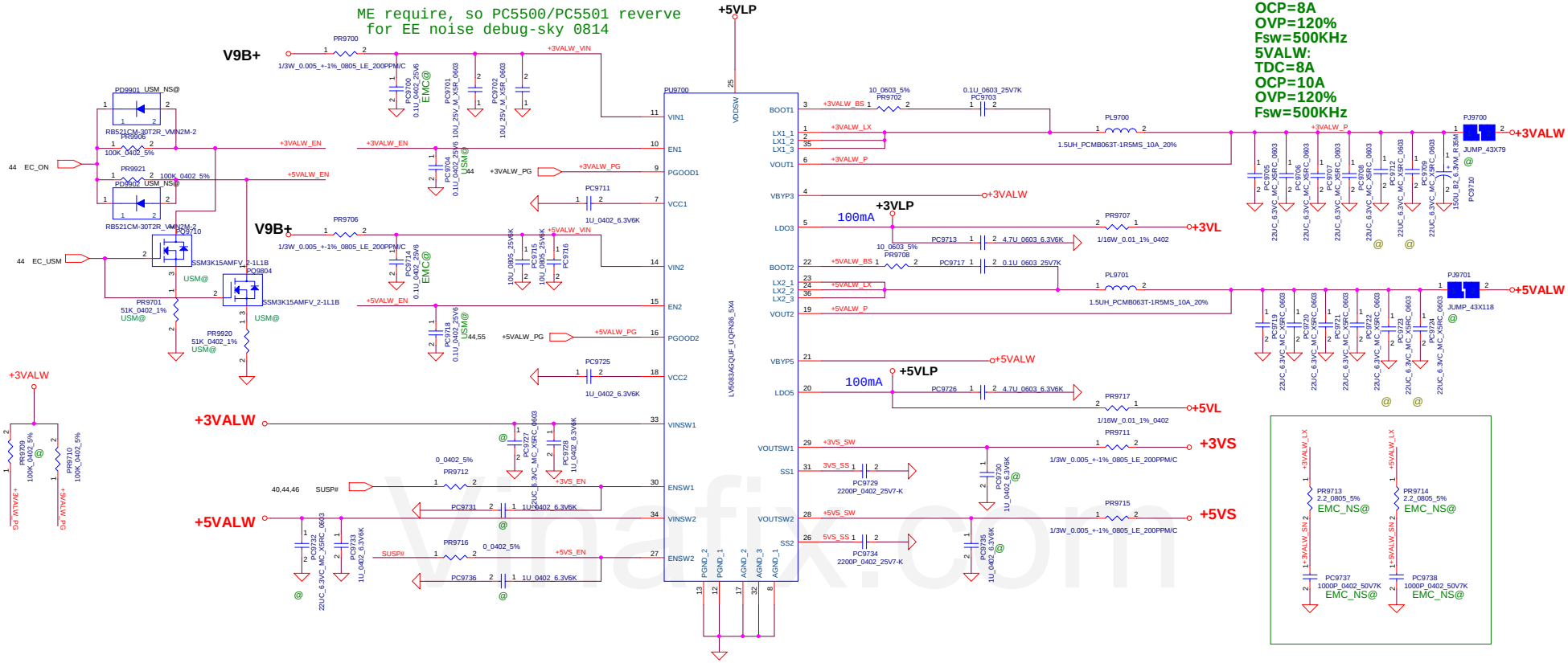
Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title	PWR-CHARGER		
Size: C	Document Number: GS44D/GS54D		Rev: 0.3
Date: Tuesday, July 30, 2019	Sheet 53 of 1		

EC_ON pull high reserve at EC,
no need USM enable=1.57V USM

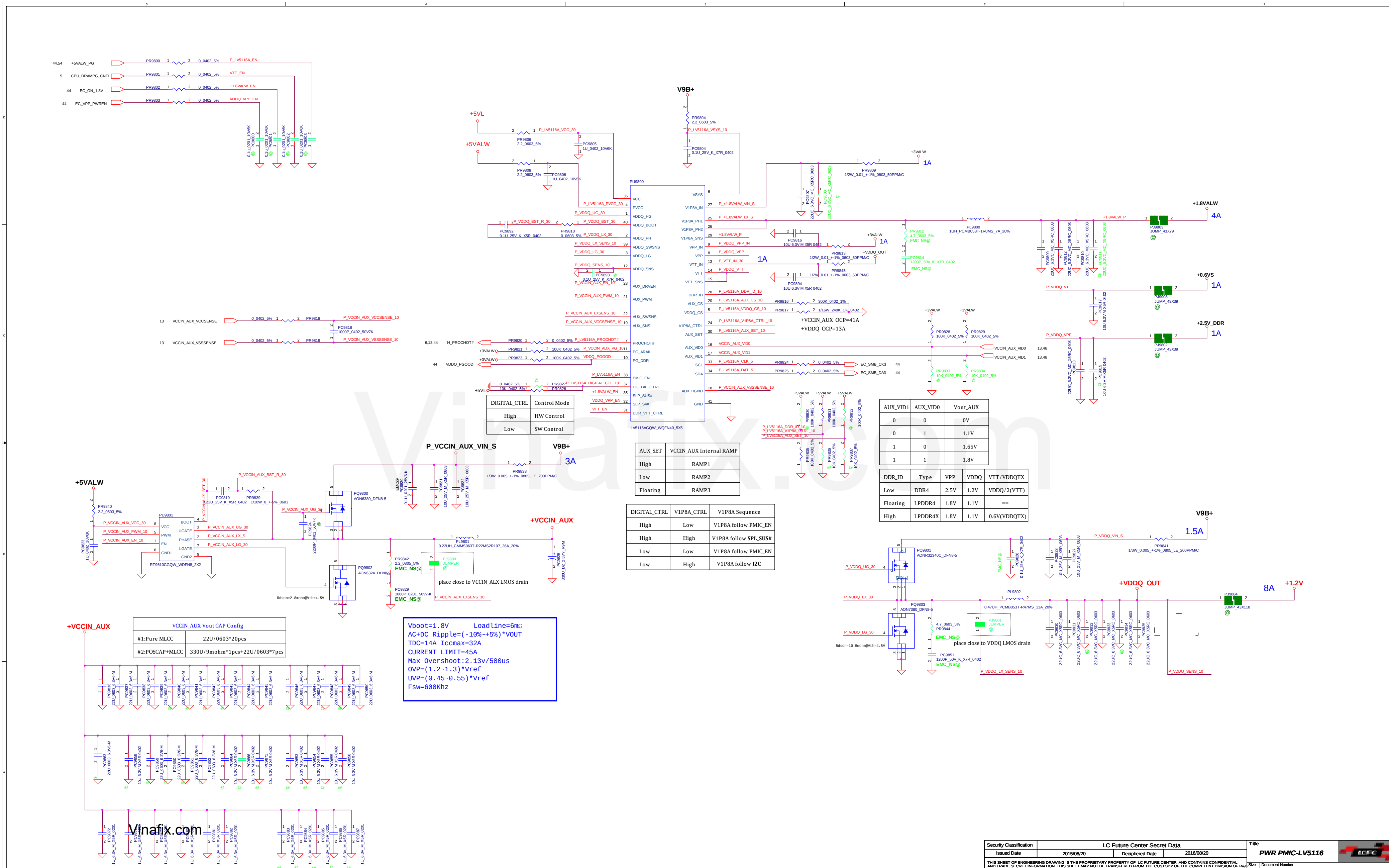
ME require, so PC5500/PC5501 reverve
for EE noise debug-sky 0814

3VALW:
TDC=6A
OCP=8A
OVP=120%
Fsw=500KHz
5VALW:
TDC=8A
OCP=10A
OVP=120%
Fsw=500KHz



Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title	PWR_3VALW/5VALW		
Size: C	Document Number: GS44D/GS54D		Rev: 0.2
Date: Wednesday, July 31, 2019	Sheet 54 of 1		



DIGITAL_CTRL	Control Mode
High	HW Control
Low	SW Control

AUX_SET	VCCIN_AUX Internal RAMP
High	RAMP1
Low	RAMP2
Floating	RAMP3

DIGITAL_CTRL	V1P8A_CTRL	V1P8A Sequence
High	Low	V1P8A follow PMIC_EN
High	High	V1P8A follow **SPL_SUS#**
Low	Low	V1P8A follow PMIC_EN
Low	High	V1P8A follow **I2C**

AUX_VID1	AUX_VID0	Vout_AUX
0	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V

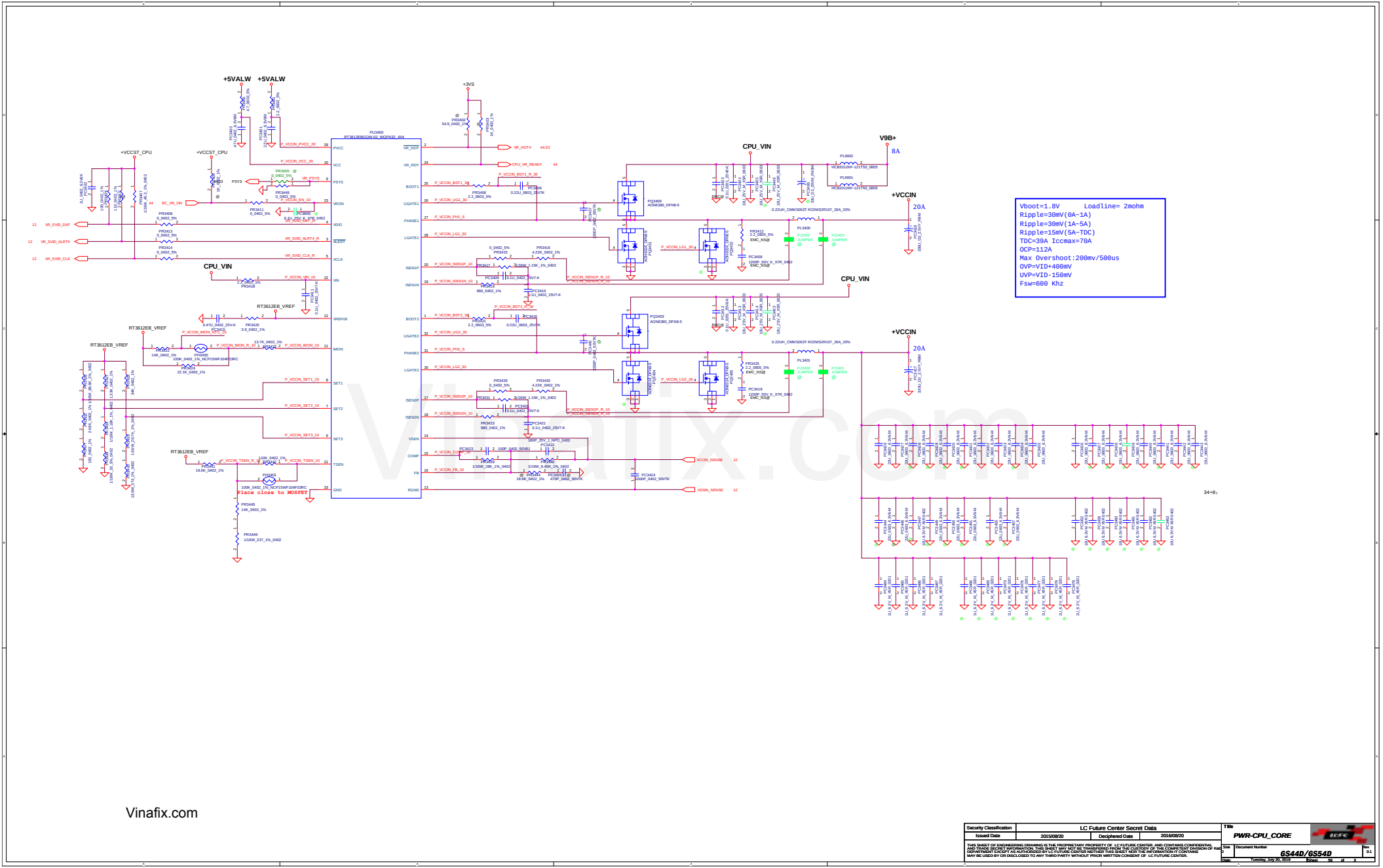
DDR_ID	Type	VPP	VDDQ	VTT/VDDQTX
Low	DDR4	2.5V	1.2V	VDDQ/2(VTT)
Floating	LPDDR4	1.8V	1.1V	--
High	LPDDR4X	1.8V	1.1V	0.6V(VDDQTX)

VCCIN_AUX Vout CAP Config	
#1:Pure MLCC	22U/0603*20pcs
#2:POSCAP+MLCC	330U/9mohm*1pcs+22U/0603*7pcs

```
Vboot=1.8V      Loadline=6mΩ
AC+DC Ripple=(-10%~+5%)*VOUT
TDC=14A Iccmax=32A
CURRENT LIMIT=45A
Max Overshoot:2.13v/500us
OVP=(1.2~1.3)*Vref
UVP=(0.45~0.55)*Vref
Fsw=600Khz
```

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **PWR PMIC-LV5116**
Document Number: **GS44D/GS54D**
Rev: 0.1
Date: Tuesday, July 30, 2019



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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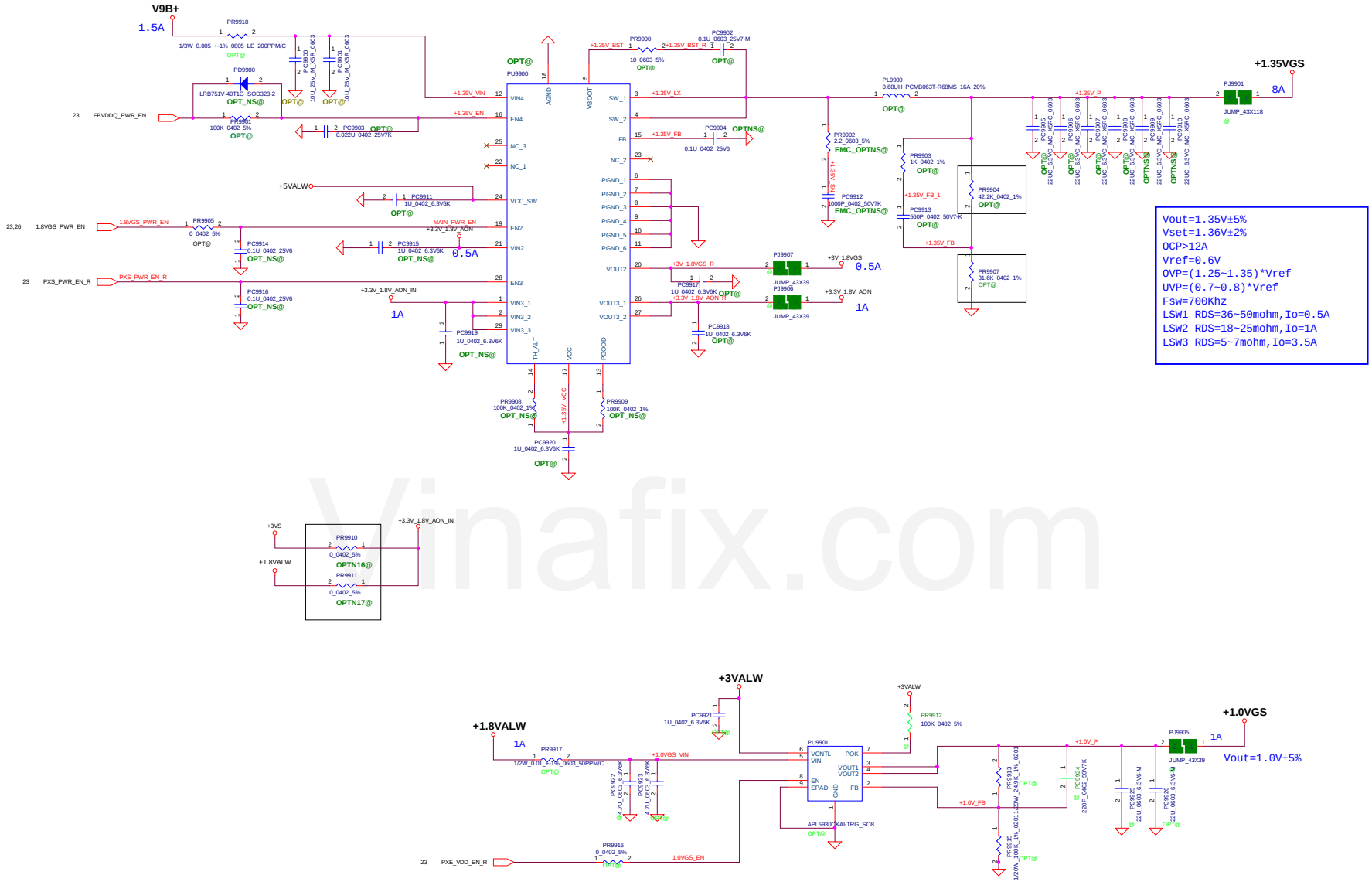
Title	PWR-CPU_CORE		
Size	Document Number		Rev
D	6S44D/6S54D		0.1
Date: Tuesday, July 30, 2015	Sheet 36 of 3		

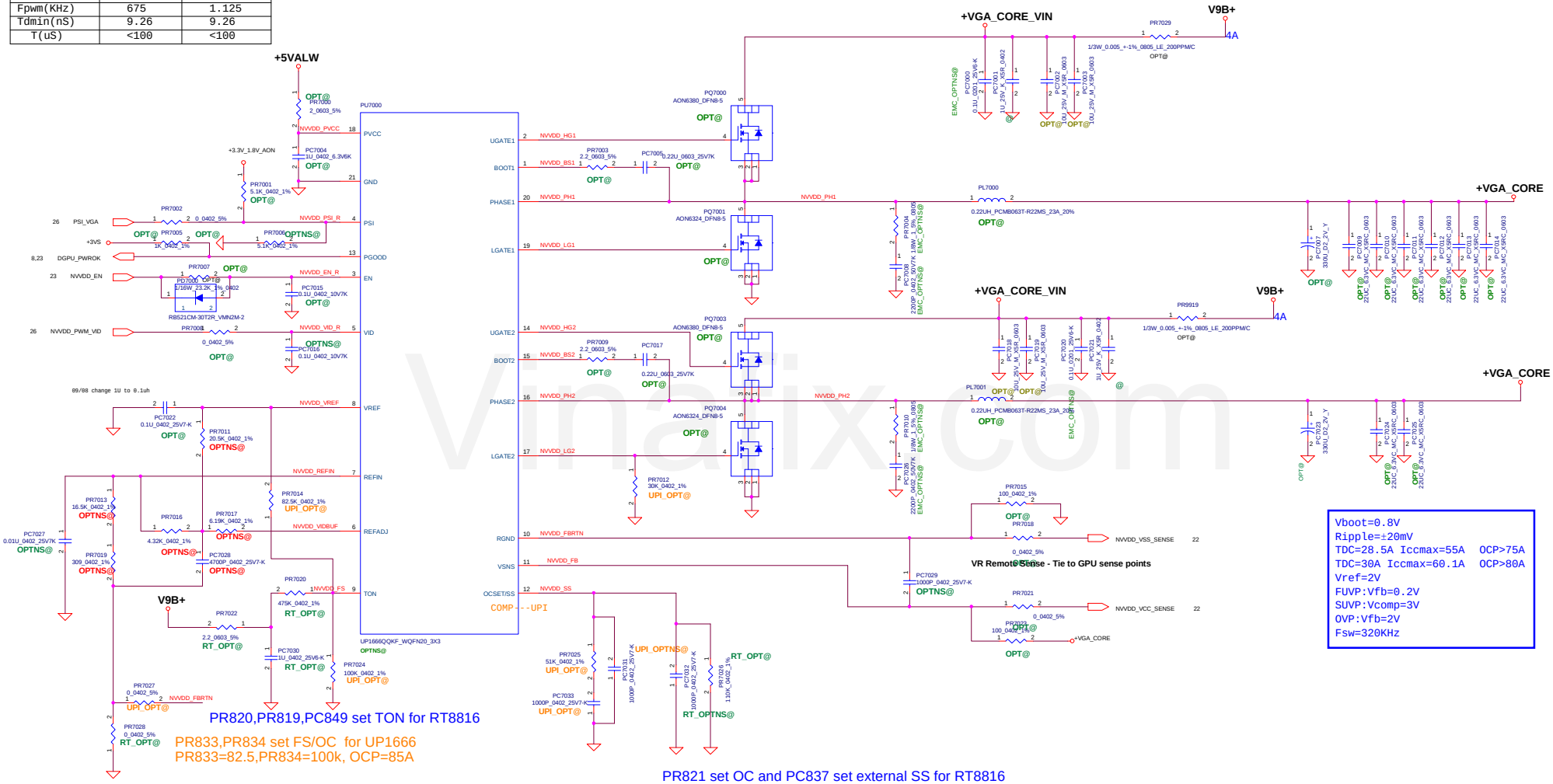


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	PWR-VGA-PMIC		
Size: Custom	Document Number: GS44D/GS54D		Rev: 0.3
Date: Tuesday, July 30, 2019	Sheet 57 of 5		

PWM-VID Specification		
	N17 Config	N16 Config B
Vmin(V)	0.3	0.6
Vmax(V)	1.3	1.2
Vboot(V)	0.8	0.9
Vstep(mV)	6.25	6.25
N(level)	160	96
Fpwm(KHz)	675	1.125
Tdmin(nS)	9.26	9.26
T(uS)	<100	<100

RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM



PR816,PR812,PR815,PR813,PR818,PC826 BOM structure control for N16 or N17

Component	Value	N17	N16
R1(KΩ)	PR7017	6.19	20
R2(KΩ)	PR7011	20.5	20
R3(KΩ)	PR7016	4.32	2
R4(KΩ)	PR7013	16.5	18
R5(KΩ)	PR7019	0.309	0
C(nF)	PC7028	4.7	2.7

UPI_OPT@ : for UP1666
RT_OPT@ : for RT8816A

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR-VGA_CORE
Size: A3 | Document Number: GS44D/GS54D | Rev: 0.1
Date: Tuesday, July 30, 2019 | Sheet 58 of 4

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title

POWER CHANGE LIST

Size: C	Document Number: GS44D/GS54D	Rev: 0.1
Date: Tuesday, July 30, 2019	Sheet 59 of 62	

Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2018/08/20

Title: ***S740-ICL***

Size: C | Document Name: ***GS44D/GS54D*** | Rev: 0.1

Date: Tuesday, July 30, 2019 | Sheet 61 of 62