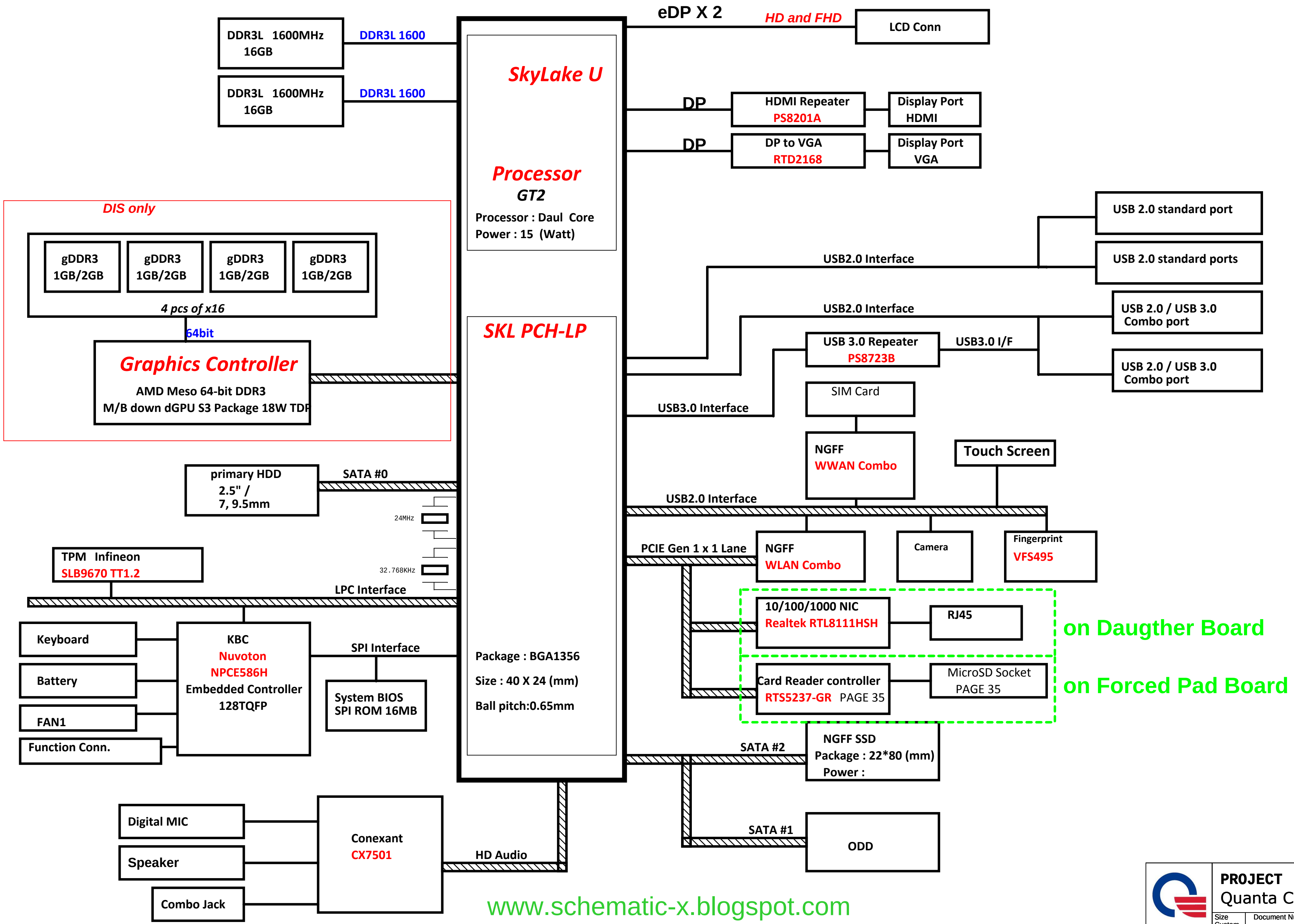
2015 400 series SkyLake U 15"/ 17" (UMA/DIS) Block Diagram 01



PCB 6L STACK UP(1.2mm)

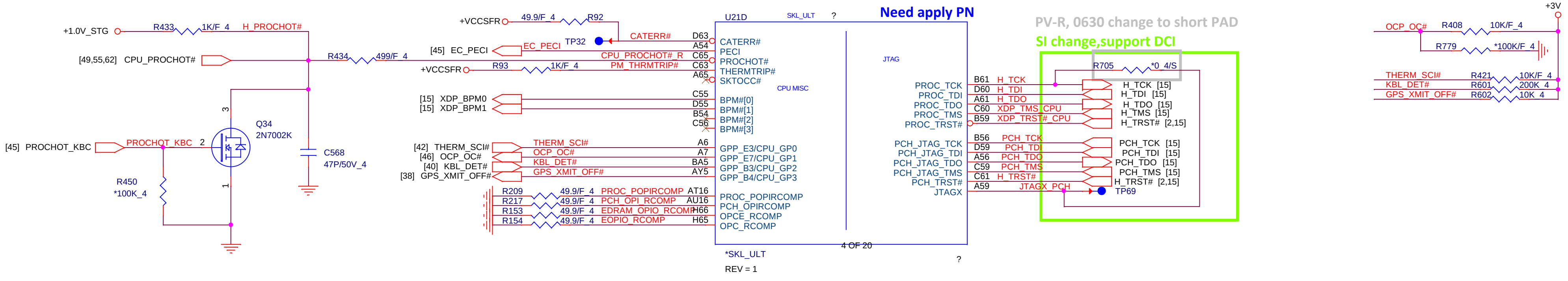
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

NB5

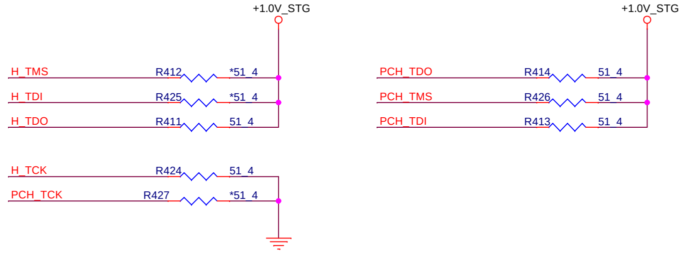
PROJECT : S400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Tuesday, October 13, 2015 Sheet 1 of 65



Processor pull-up (CPU)



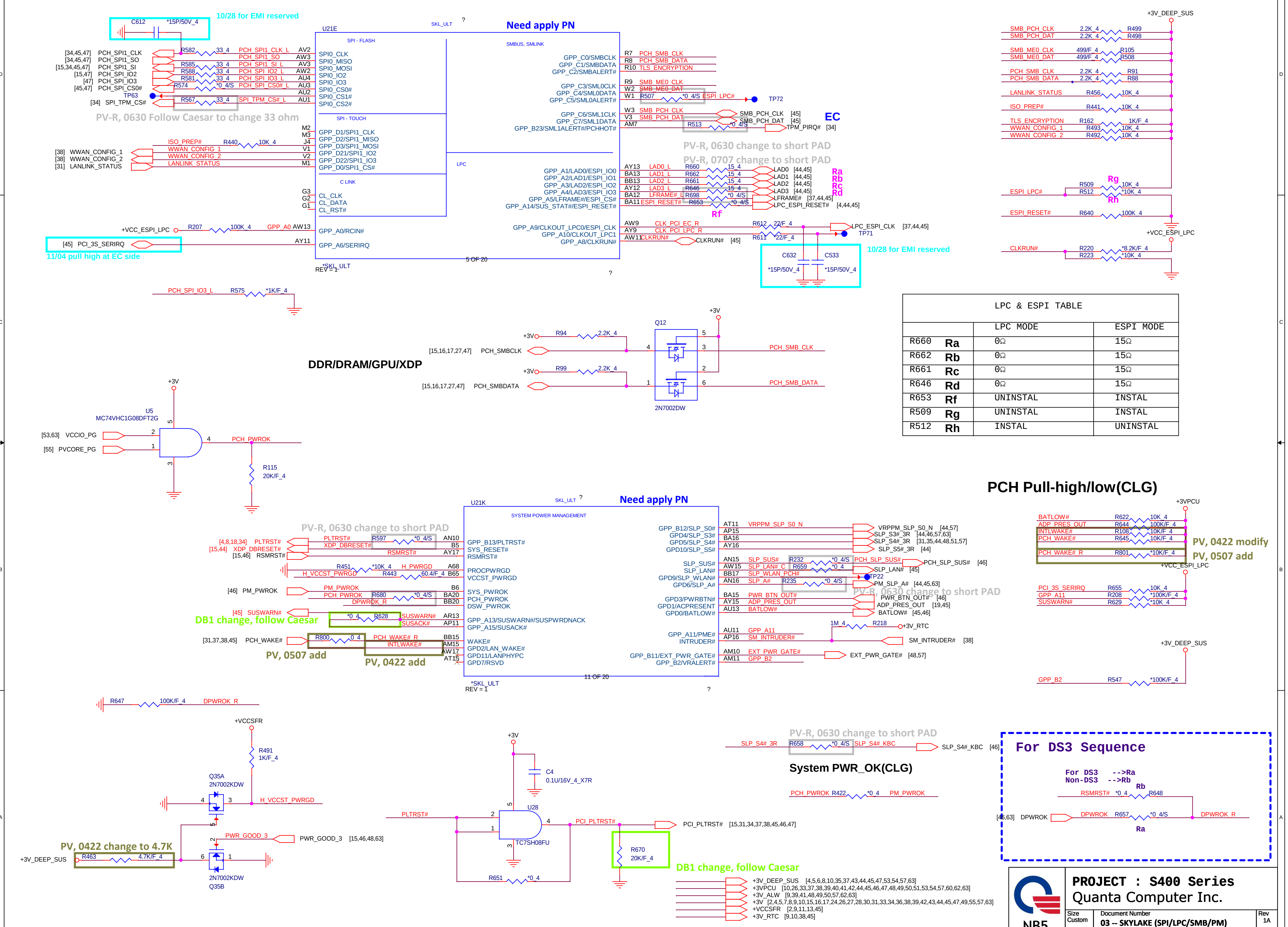
+1.0V_STG [11,13]
+VCCSFR [3,9,11,13,45]
+3V [3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,39,42,43,44,45,47,49,55,57,63]

NB5

PROJECT : S400 Series

Quanta Computer Inc.

Size	Document Number	Rev
Custom	02 -- SKYLAKE 2/20(MISC/ JTAG)	1A



LPC & ESPI TABLE			
		LPC MODE	ESPI MODE
R660	Ra	0Ω	15Ω
R662	Rb	0Ω	15Ω
R661	Rc	0Ω	15Ω
R646	Rd	0Ω	15Ω
R653	Rf	UNINSTAL	INSTAL
R509	Rg	UNINSTAL	INSTAL
R512	Rh	INSTAL	UNINSTAL

NB5

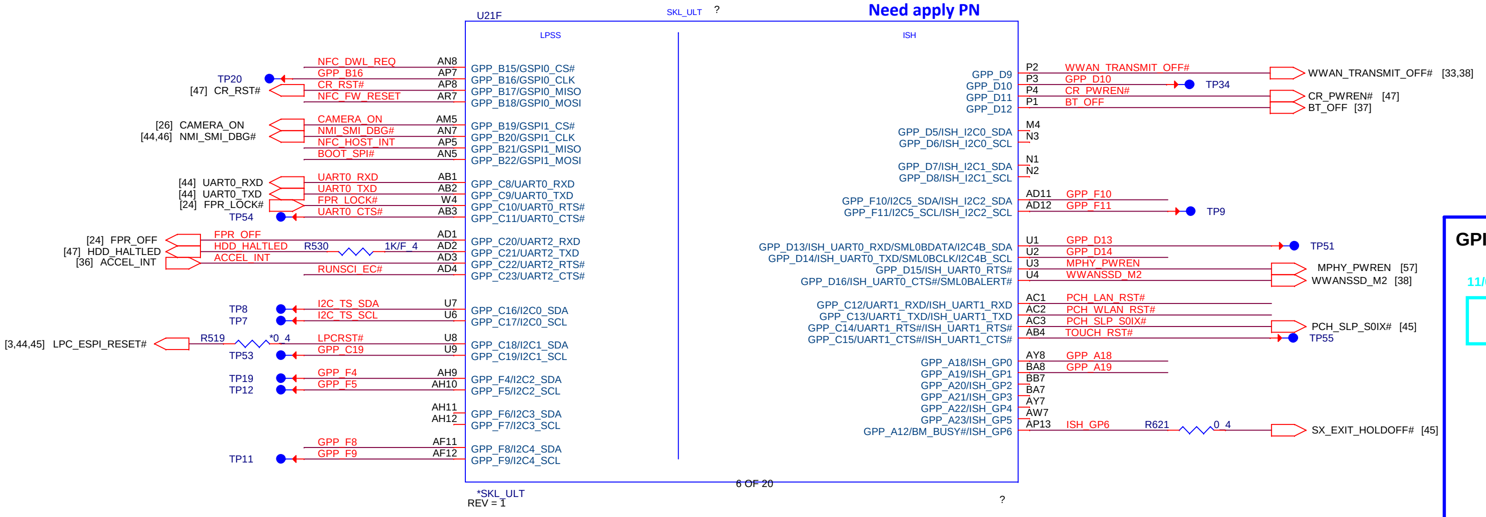
PROJECT : S400 Series
Quanta Computer Inc.

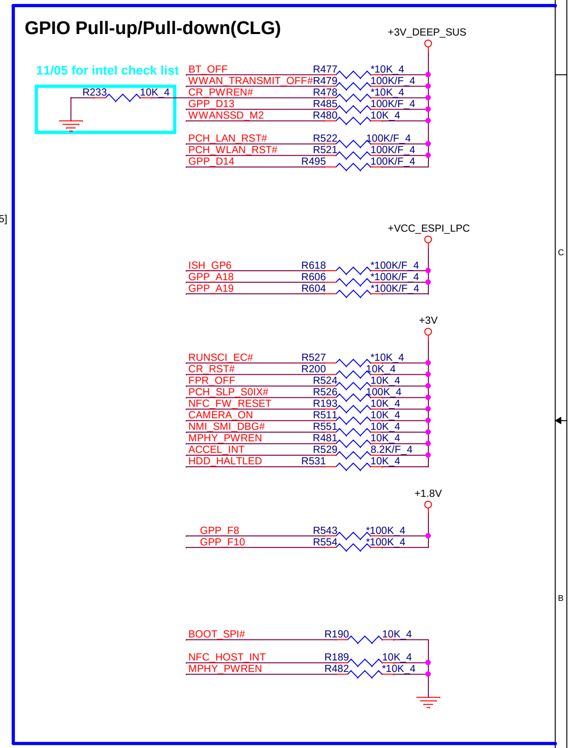
Size: Custom | Document Number: 03 -- SKYLAKE (SPI/LPC/SMB/PM) | Rev: 1A

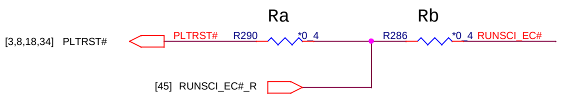
Date: Tuesday, November 17, 2015 | Sheet 3 of 65

Skylake (GPIO)

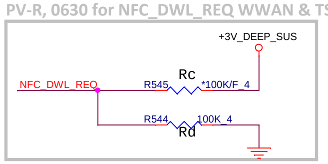
Need apply PN







PV-R, 0630 for NFC_DWL_REQ WWAN & TS TABLE



LPC & ESPI TABLE

	LPC MODE	ESPI MODE
Ra	UNINSTAL	UNINSTAL
Rb	INSTAL	UNINSTAL

WWAN & TS TABLE

	WWAN MODE	TS MODE
Rc	INSTALL	UNINSTALL
Rd	UNINSTALL	INSTALL

+1.8V [5,8,30,52,60,63]
+3VPCU [3,10,26,33,37,38,39,40,41,42,44,45,46,47,48,49,50,51,53,54,57,60,62,63]
+3V_DEEP_SUS [3,5,6,8,10,35,37,43,44,45,47,53,54,57,63]
+3V [2,3,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,39,42,43,44,45,47,49,55,57,63]

NB5

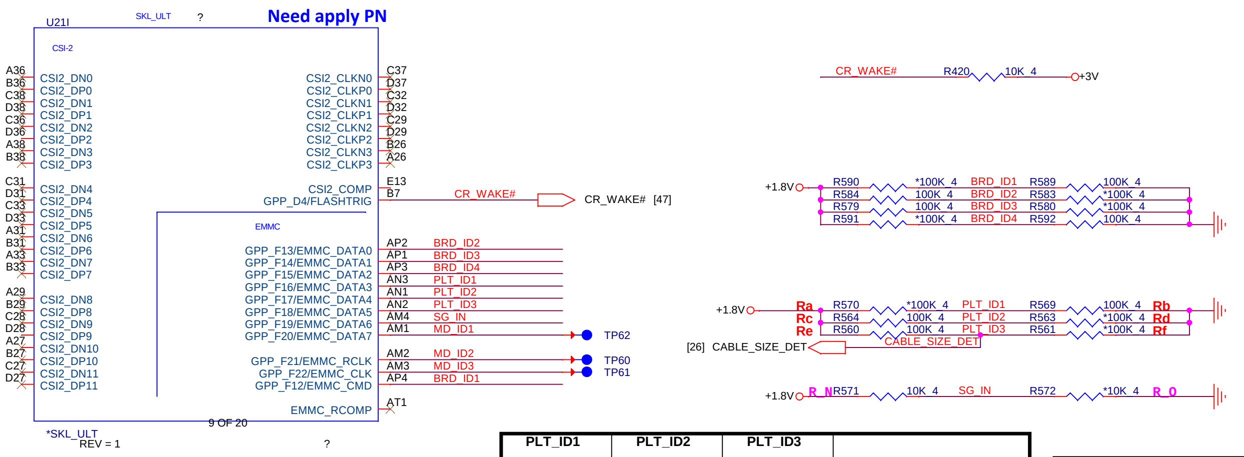
PROJECT : S400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	04 -- SKYLAKE (GPIO)	1A

Date: Friday, November 27, 2015 Sheet 4 of 65

	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	
	GPIO201	GPIO202	GPIO203	GPIO204	AMD_FCH
	GPIO14	GPIO34	GPIO35	GPIO40	PPMT
	GPIO15	GPIO34	GPIO35	GPIO40	LPI-H
BOARD REVISION	GPIO76	GPIO77	GPIO78	GPIO79	LPT-LP
DB0	0	0	0	0	
DB1	0	0	0	1	
DB2 (DDR4)	0	0	1	0	
	0	0	1	1	
SI1	0	1	0	0	
SIB	0	1	0	1	
SI2 (DDR4)	0	1	1	0	
	0	1	1	1	
PV1	1	0	0	0	
PV-R	1	0	0	1	
PV2 (DDR4)	1	0	1	0	
	1	0	1	1	
MV1	1	1	0	0	
MV2 (DDR4)	1	1	0	1	
	1	1	1	0	
	1	1	1	1	

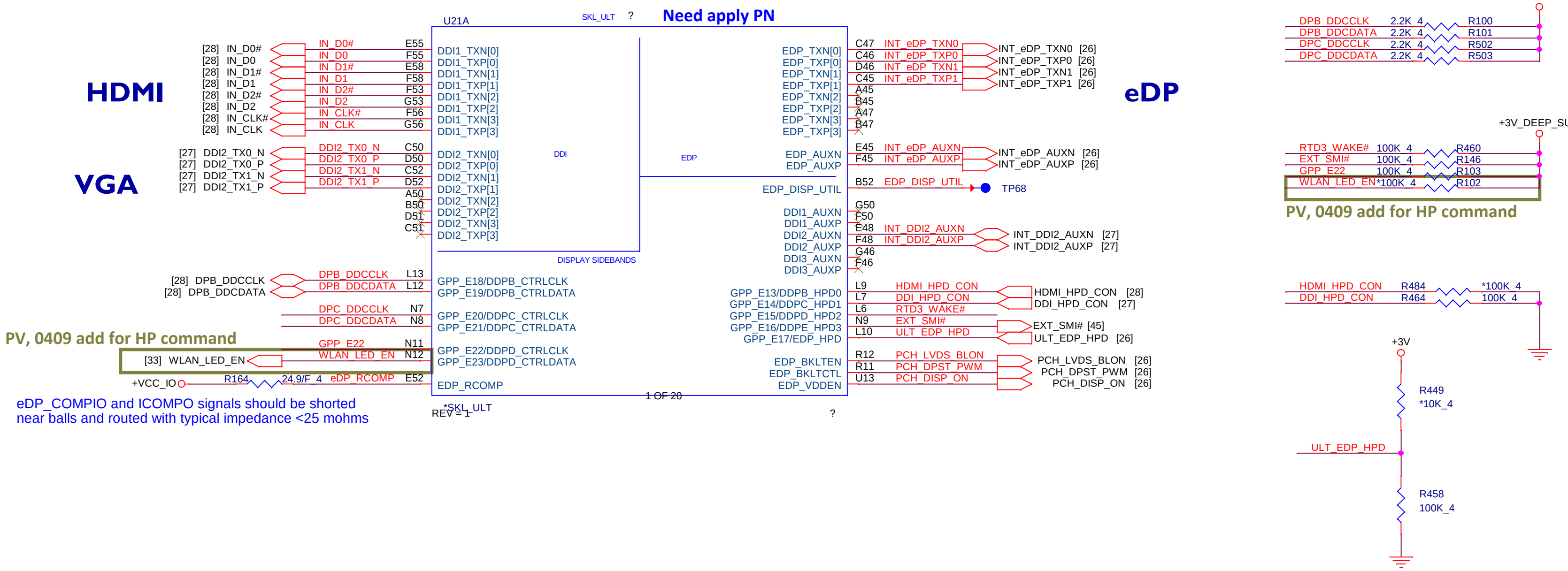
PV-R, 0707



PLT_ID1	PLT_ID2	PLT_ID3	
Ra	Rc	Re	H
Rb	Rd	Rf	L
0	0	0	13.3"
0	0	1	14"
0	1	1	15.6"
0	1	1	17.3"

SG_IN	Install	Un-Install
UMA	R572 R_O	R571 R_N
DIS	R571 R_N	R572 R_O

02/10
SI CHANGE：Cable detect



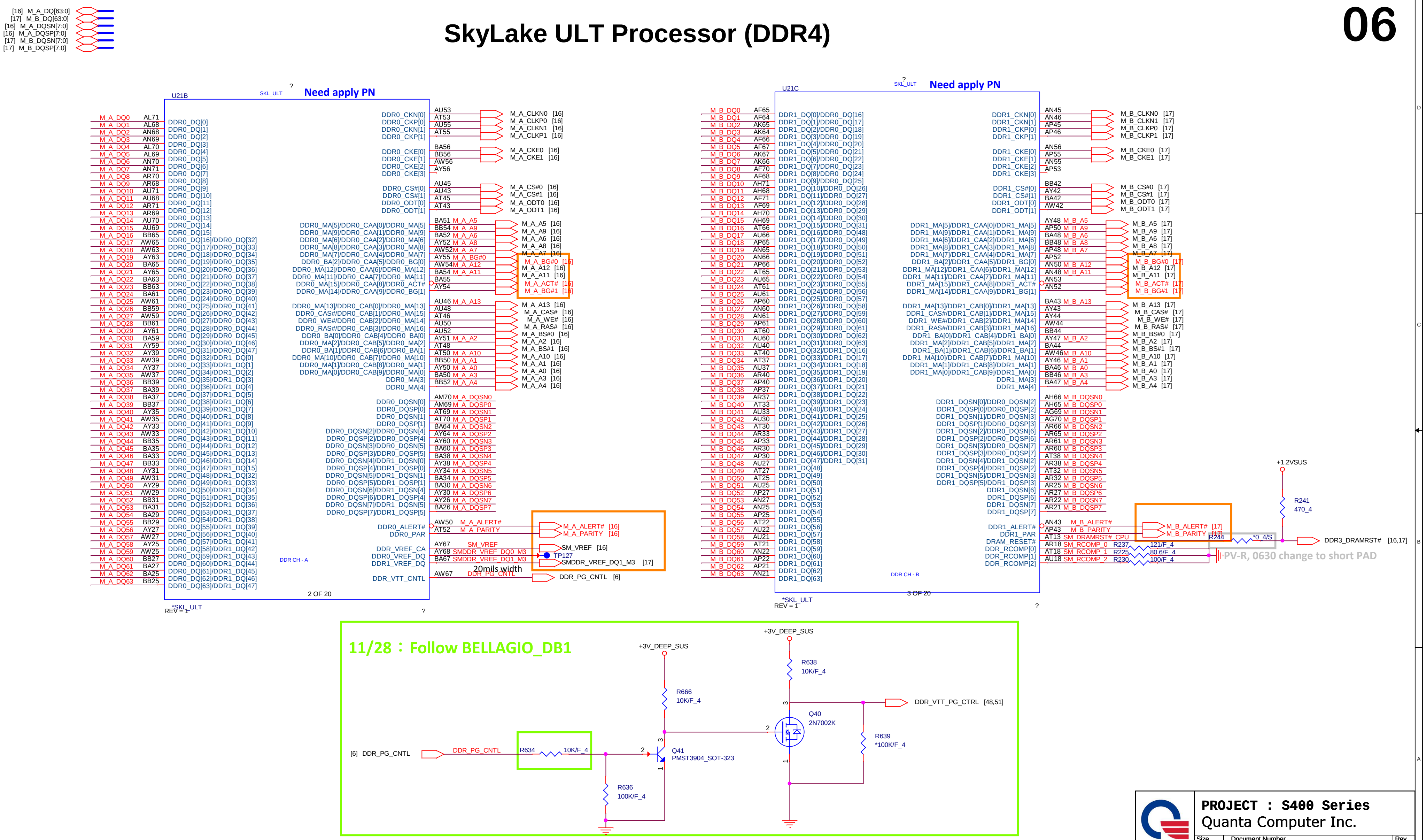
PV, 0409 add for HP command

eDP_COMPIO and ICOMPO signals should be shorted
near balls and routed with typical impedance <25 mohms

PV, 0409 add for HP command

SkyLake ULT Processor (DDR4)

06



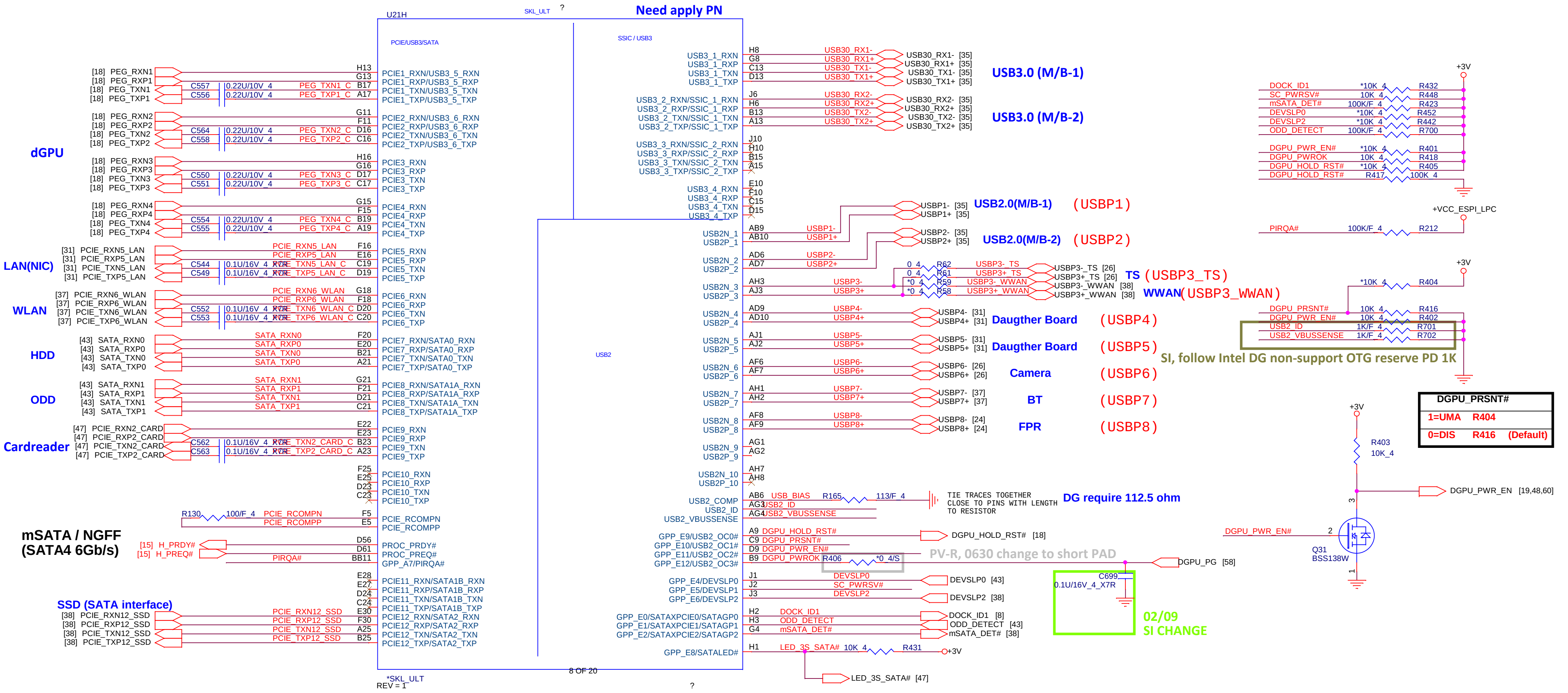
NB5

PROJECT : S400 Series

Quanta Computer Inc.

Size	Document Number	Rev
Custom	06 -- SKYLAKE (DDR3-A/B I/F)	1A

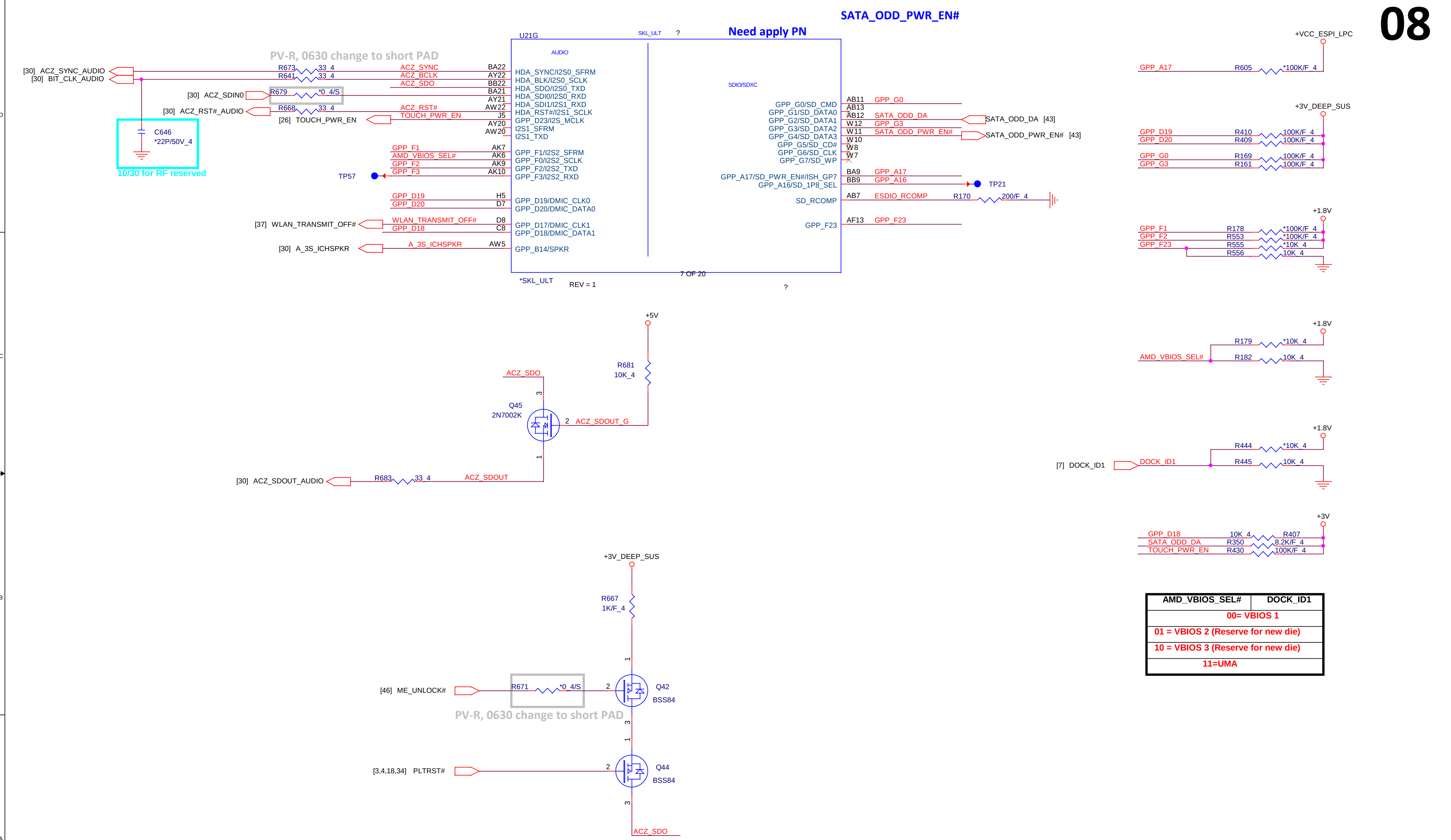
Date: Tuesday, November 17, 2015 Sheet 6 of 65



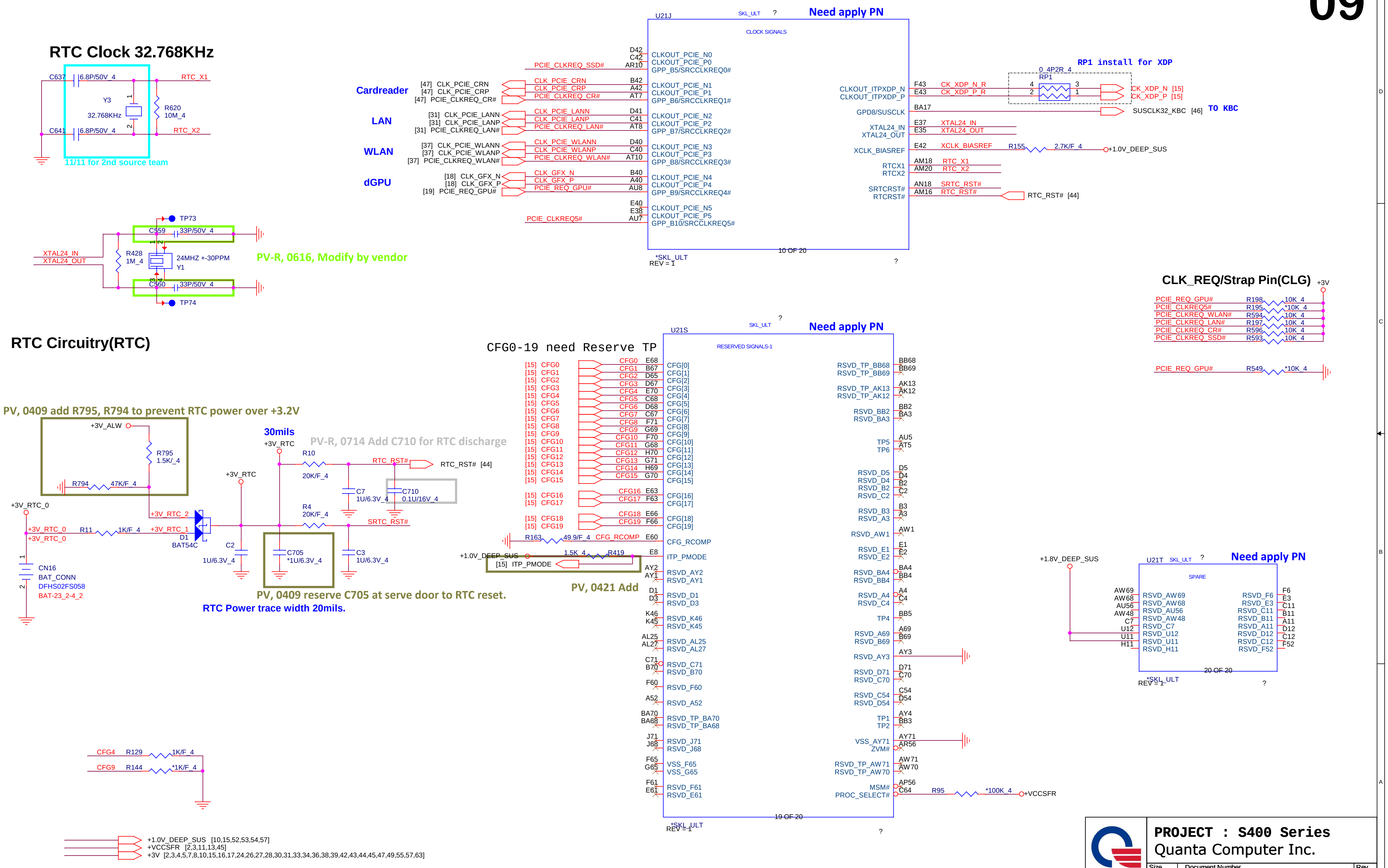
[2,3,4,5,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,39,42,43,44,45,47,49,55,57,63] +3V
[3,4,5,6,8,10,35,37,43,44,45,47,53,54,57,63] +3V_DEEP_SUS

PROJECT : S400 Series			
Quanta Computer Inc.			
Size: Custom	Document Number: 07 -- SKYLAKE (PCIE/USB)		Rev: 1A
Date: Tuesday, December 01, 2015	Sheet 7	of 65	

NB5



AMD_VBIOS_SEL#	DOCK_ID1
00= VBIOS 1	
01 = VBIOS 2 (Reserve for new die)	
10 = VBIOS 3 (Reserve for new die)	
11=UMA	

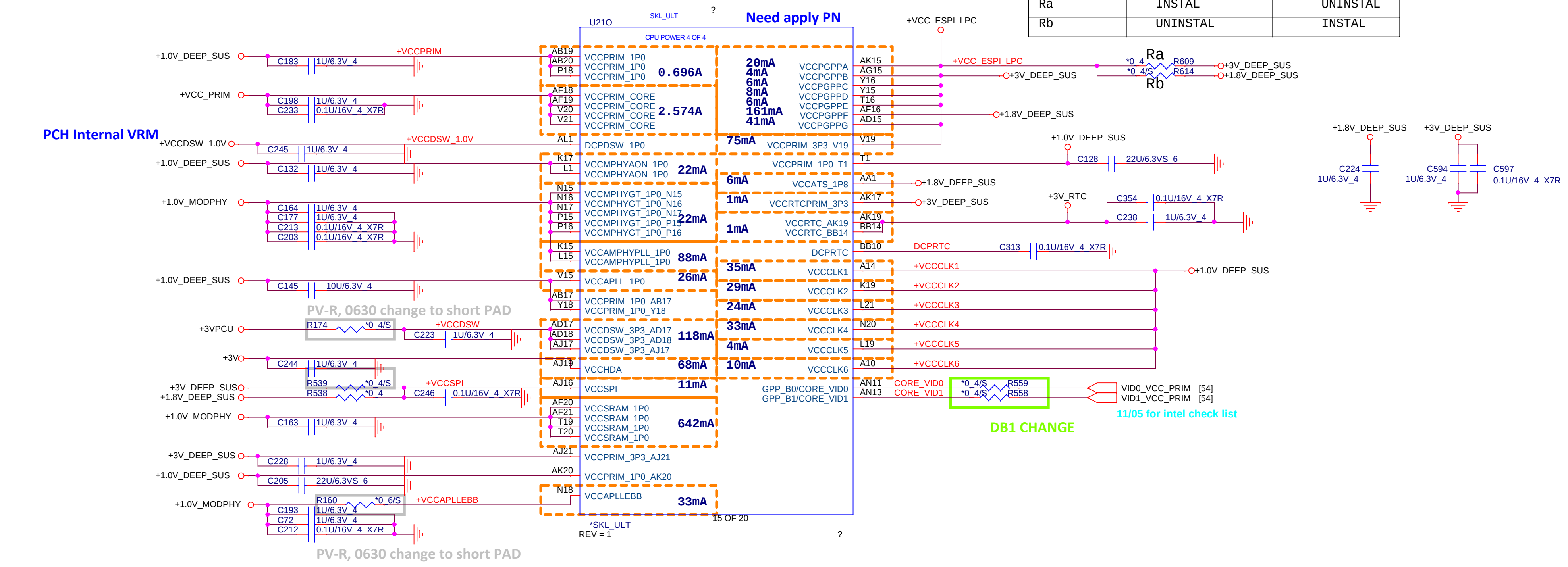


PROJECT : S400 Series
Quanta Computer Inc.
NB5

Size	Document Number	Rev
Custom	09 -- SKYLAKE (CLK/RSV/RTC)	1A

Date: Monday, November 30, 2015 Sheet 9 of 65

LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
Ra	INSTAL	UNINSTAL
Rb	UNINSTAL	INSTAL



+3V_DEEP_SUS [3,4,5,6,8,35,37,43,44,45,47,53,54,57,63]
+3VPCU [3,26,33,37,38,39,40,41,42,44,45,46,47,48,49,50,51,53,54,57,60,62,63]
+1.0V_DEEP_SUS [9,15,52,53,54,57]
+VCC_PRIM [54]
+3V [2,3,4,5,7,8,9,15,16,17,24,26,27,28,30,31,33,34,36,38,39,42,43,44,45,47,49,55,57,63]
+1.8V_DEEP_SUS [9,45,47,52,63]

PROJECT : S400 Series

Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	10 -- SKYLAKE (PCH POWER)	1A

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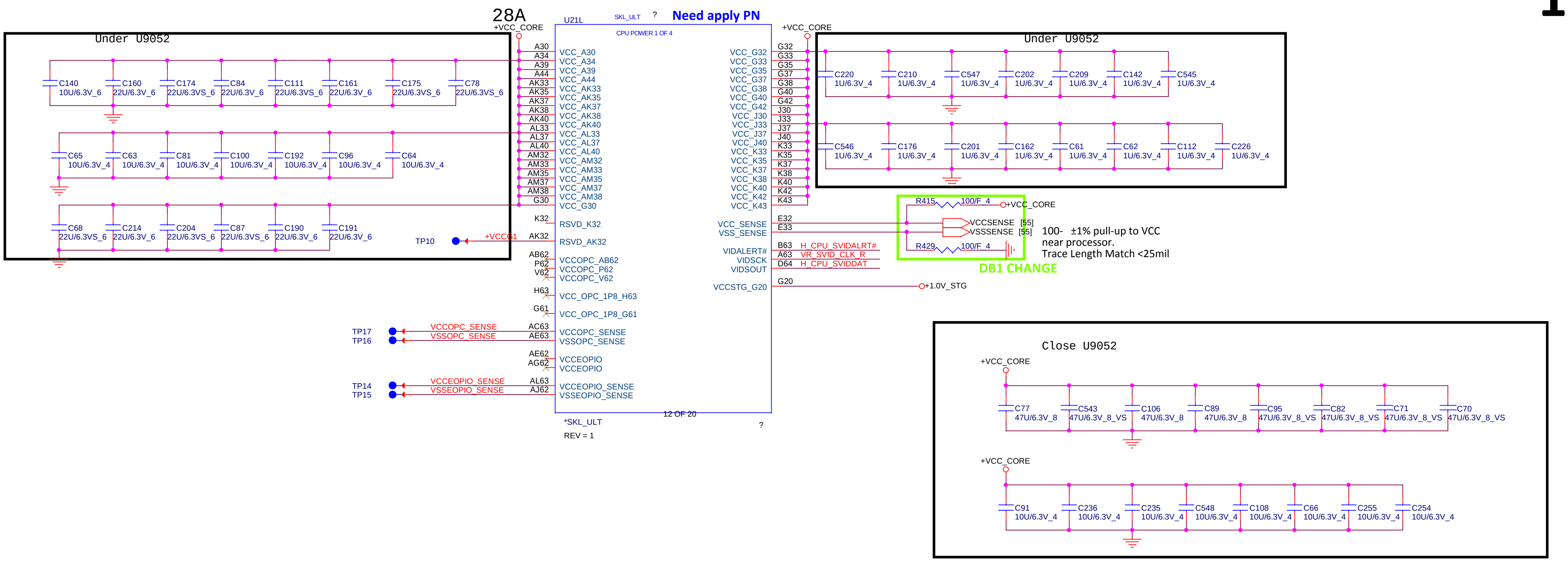
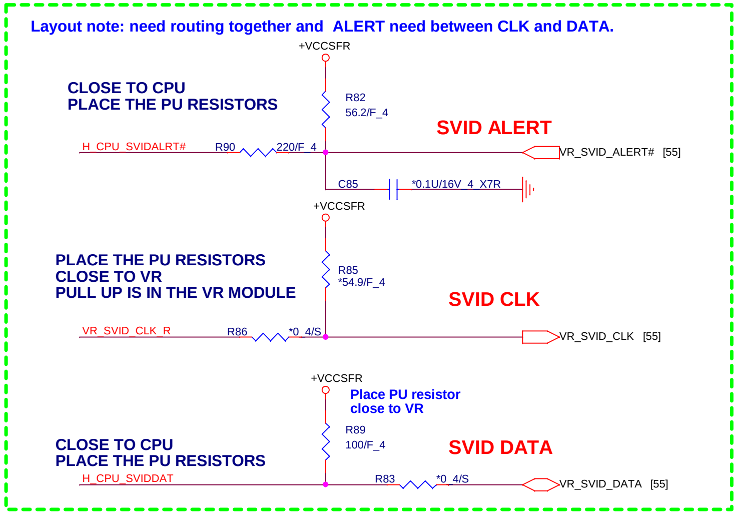
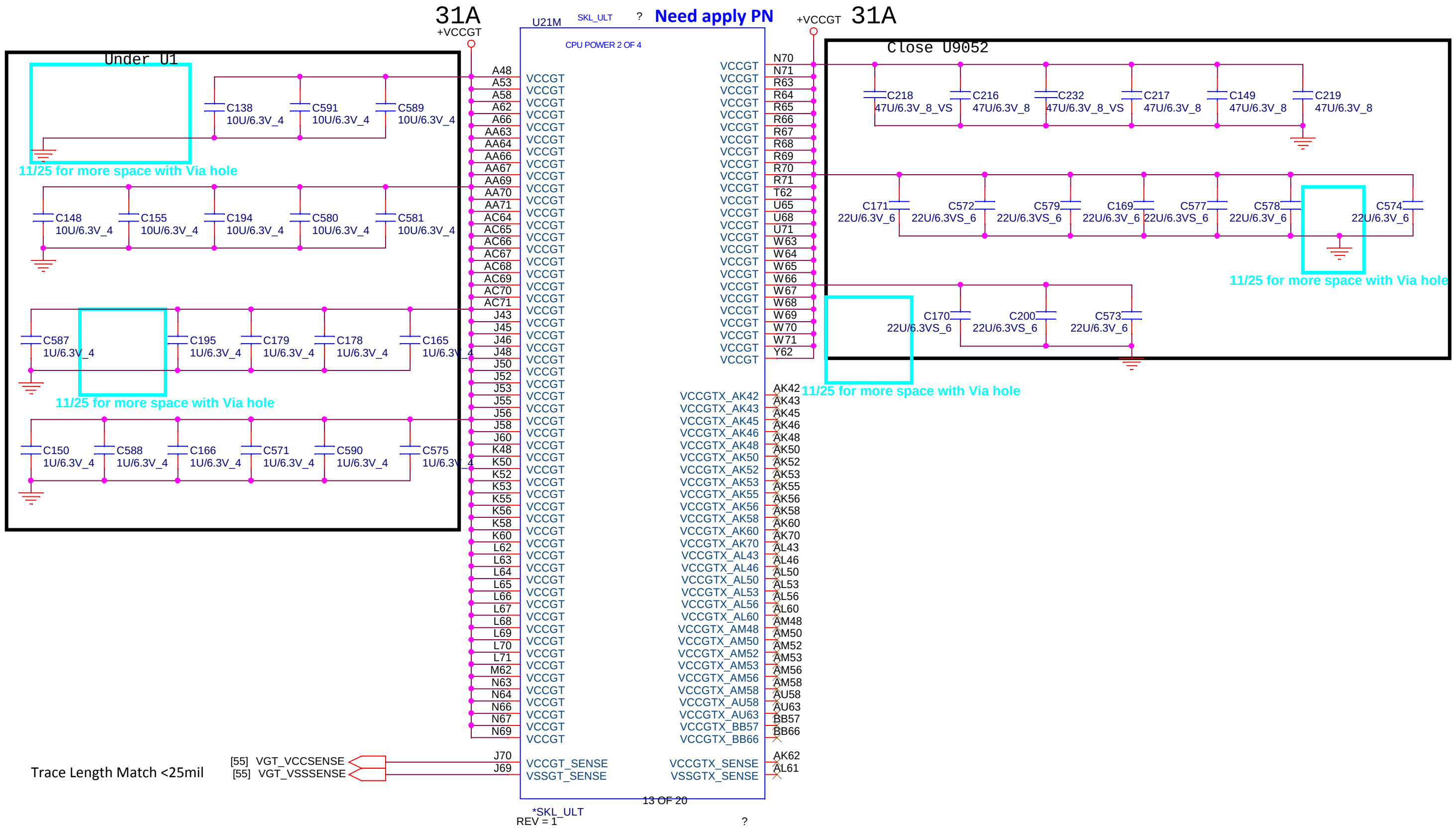


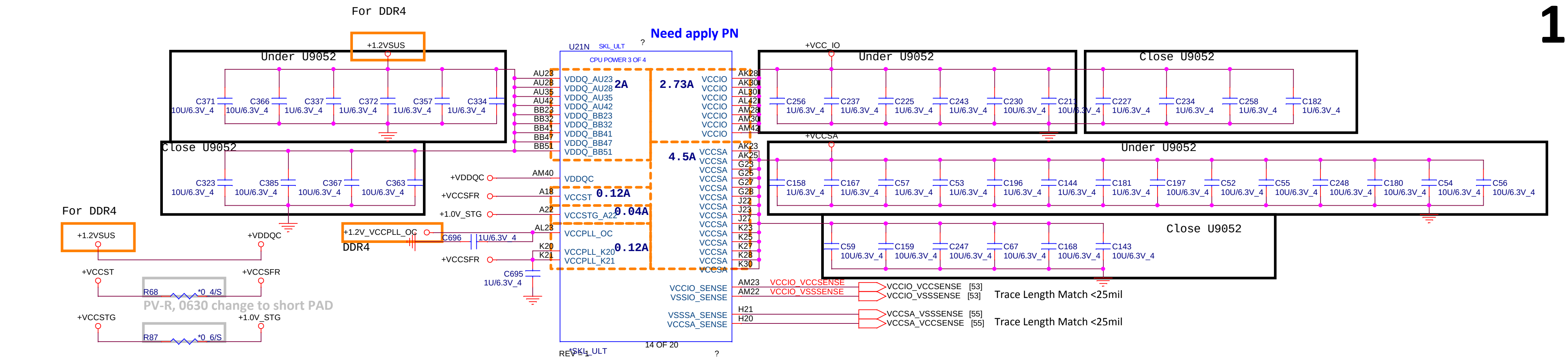


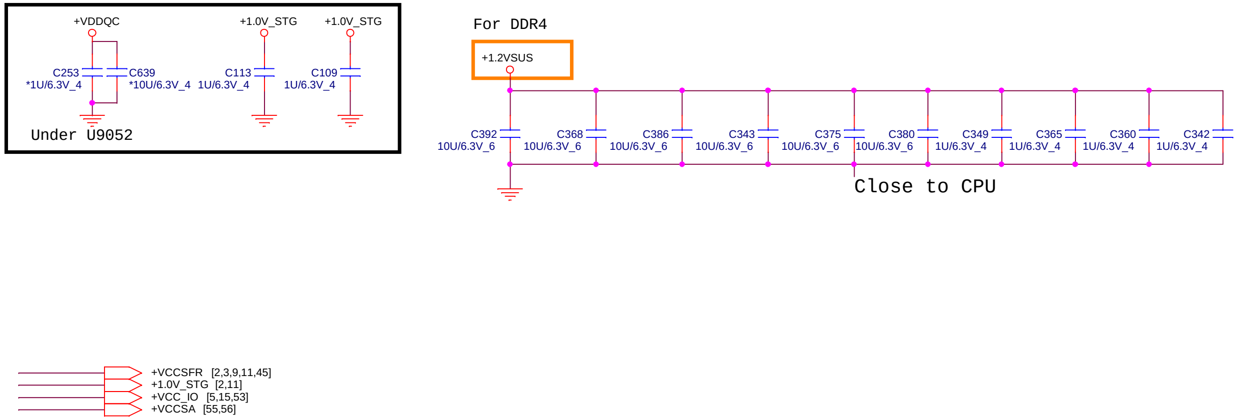
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

+1.8V [4,5,8,30,52,60,63]
+VCC_CORE [55]
+VCCSFR [2,3,9,13,45]
+1.0V_STG [2,13]



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



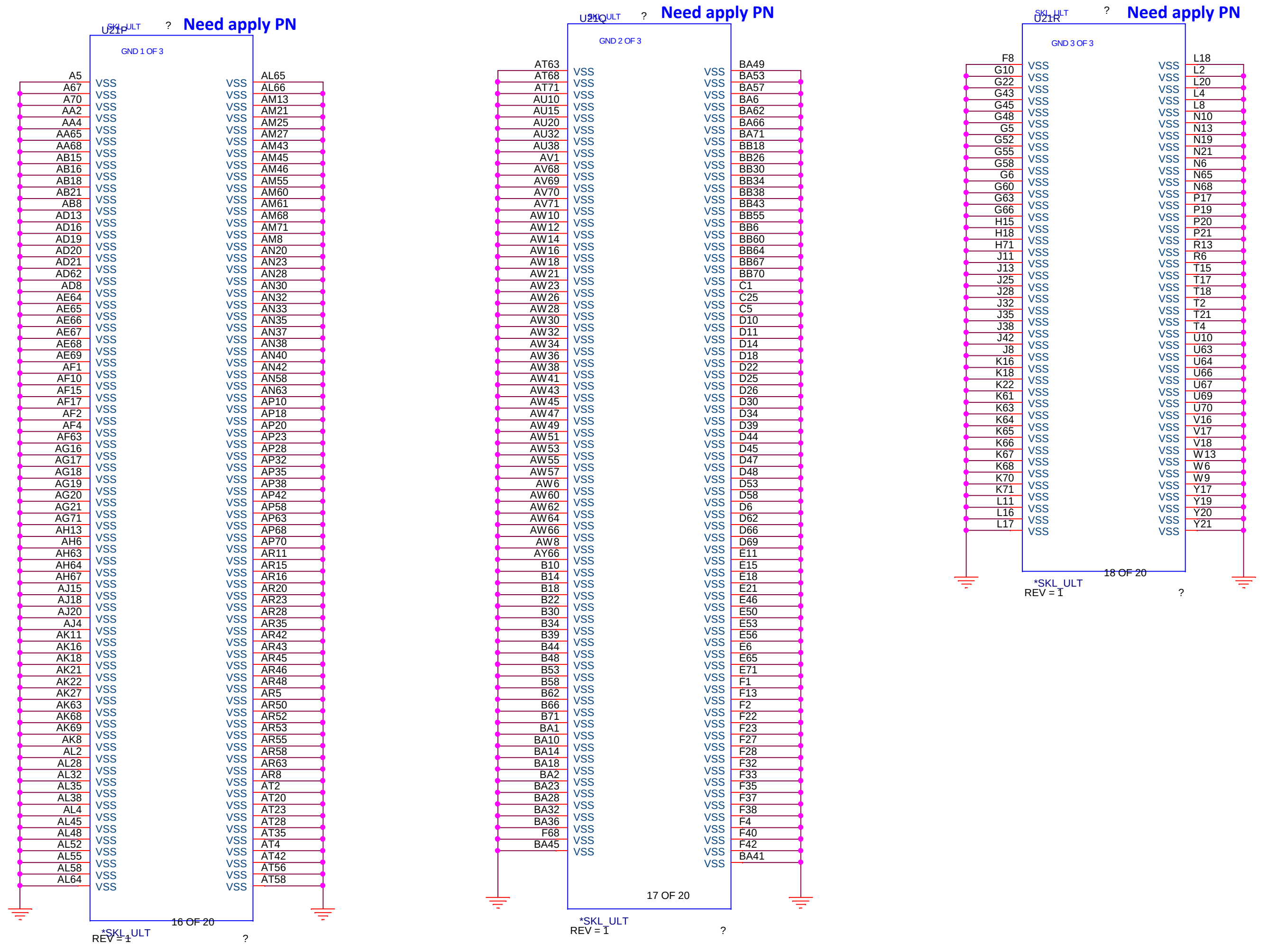


Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

NB5

PROJECT : S400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	13 -- SKYLAKE (POWER-3)	1A



NB5

PROJECT : S400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	14 -- SKYLAKE (GND)	1A

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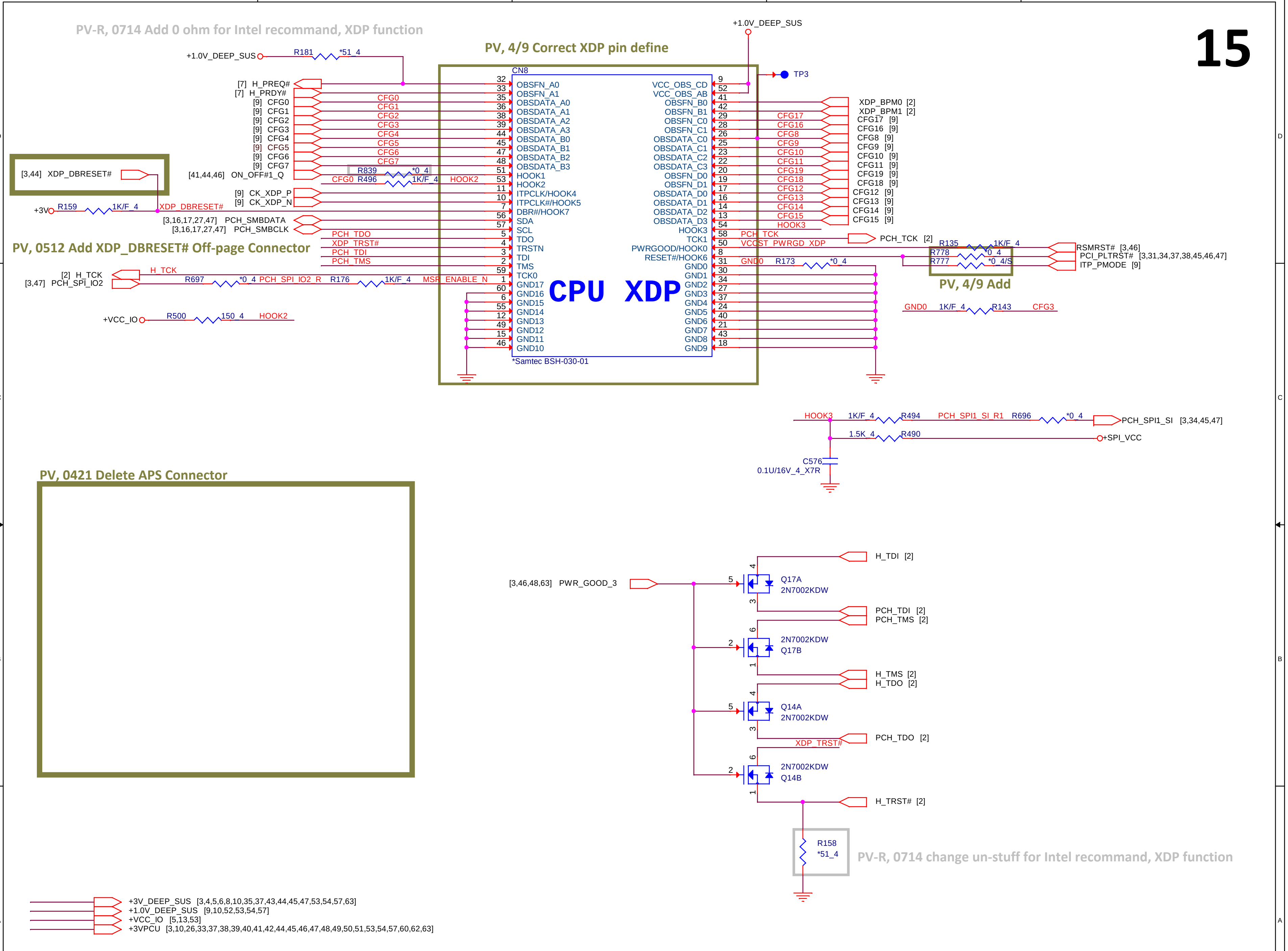


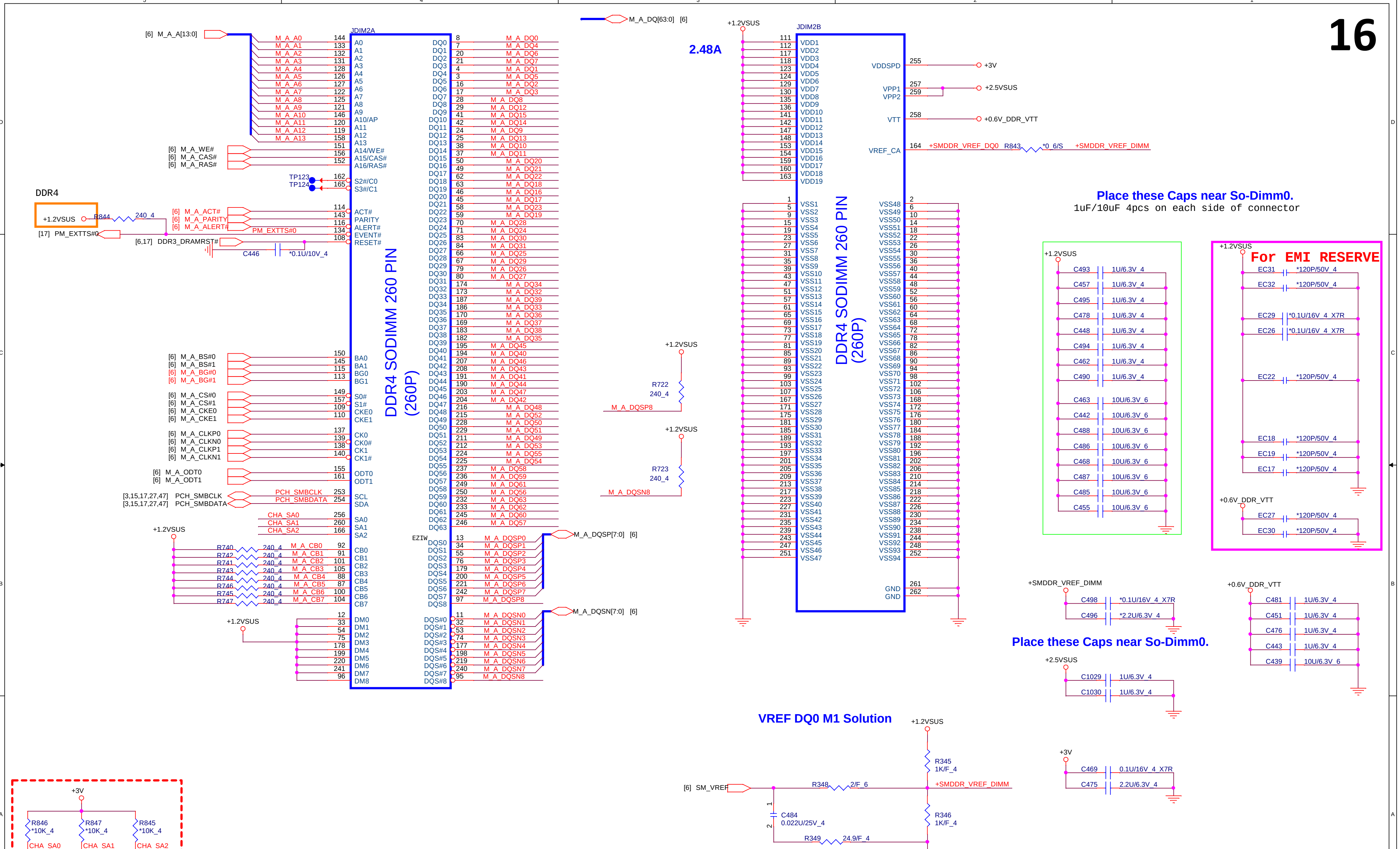
NB5

PROJECT : S400 Series

Quanta Computer Inc.

Size	Document Number	Rev
	15 -- HSW XDP & APS	1A

Date: Tuesday, November 17, 2015 | Sheet 15 of 65



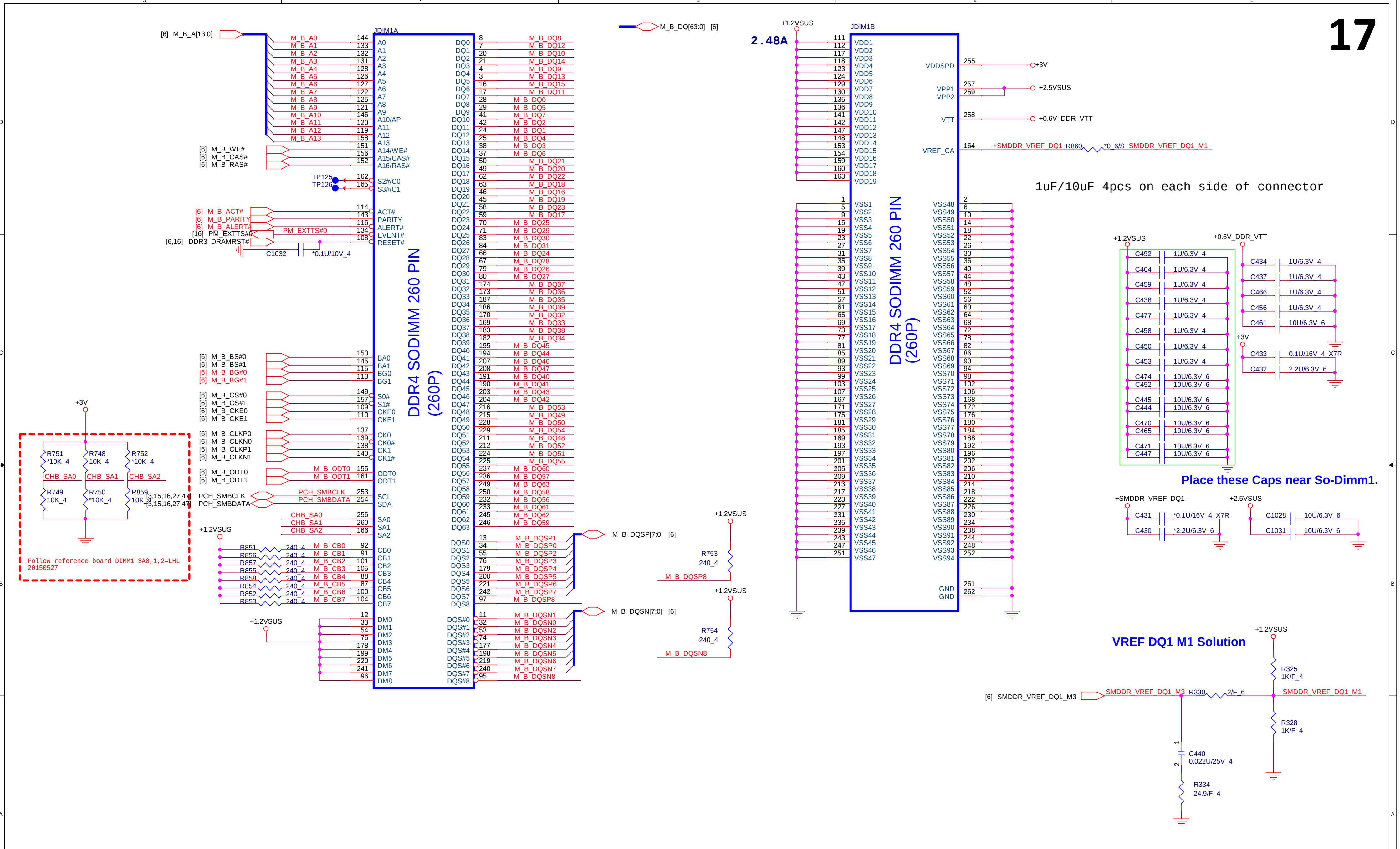
NB5

PROJECT : S400 Series

Quanta Computer Inc.

Size	Document Number	Rev
Custom	16 -- DDR3 DIMM0-STD(4.0H)	1A

Date: Monday, November 30, 2015 Sheet 16 of 65



NB5

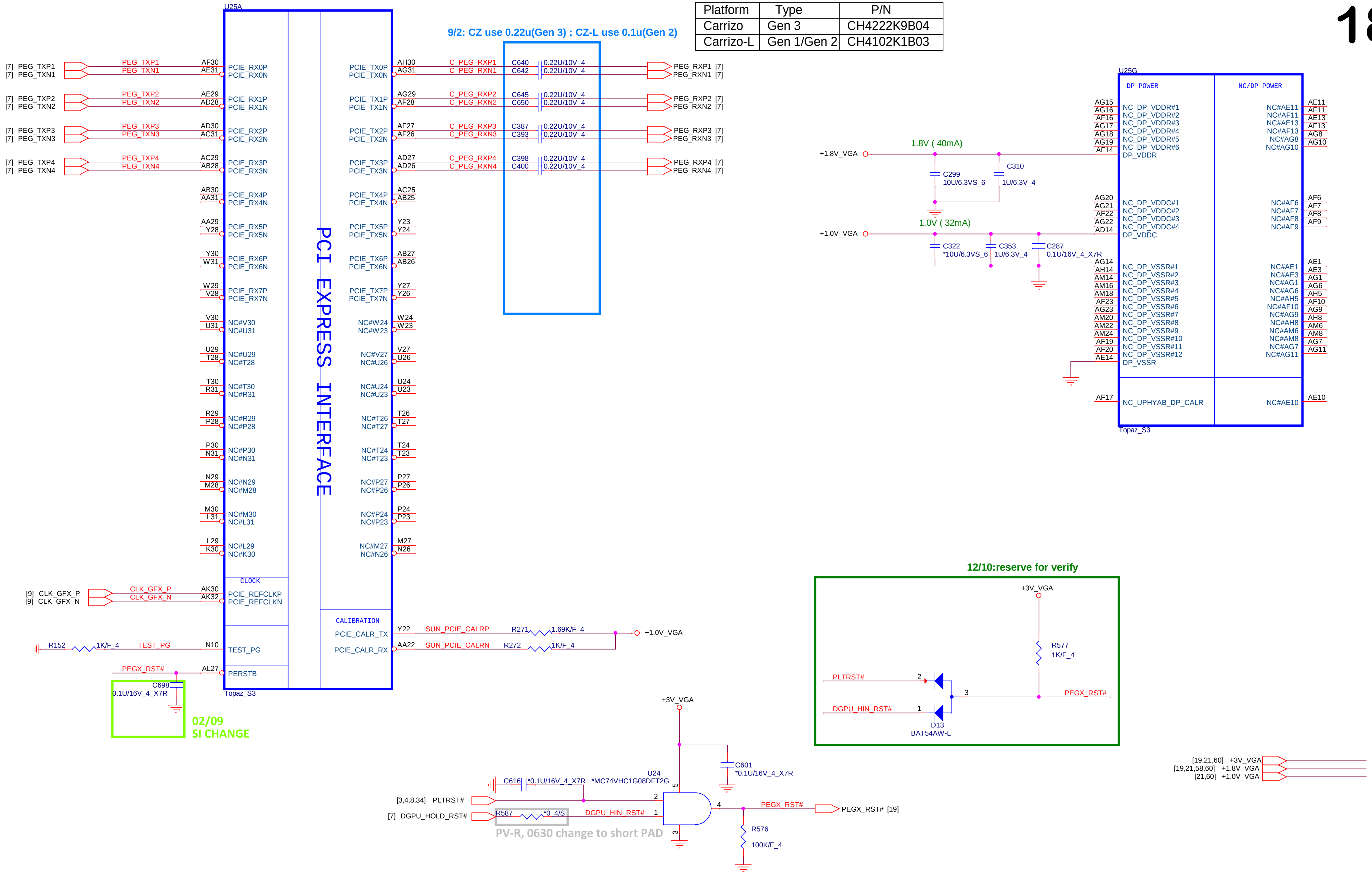
PROJECT : S400 Series

Quanta Computer Inc.

Size	Document Number	Rev
Custom	17 -- DDR3 DIMM1-RVS(4.0H)	1A

Date: Monday, November 30, 2015 Sheet 17 of 65

Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4102K1B03



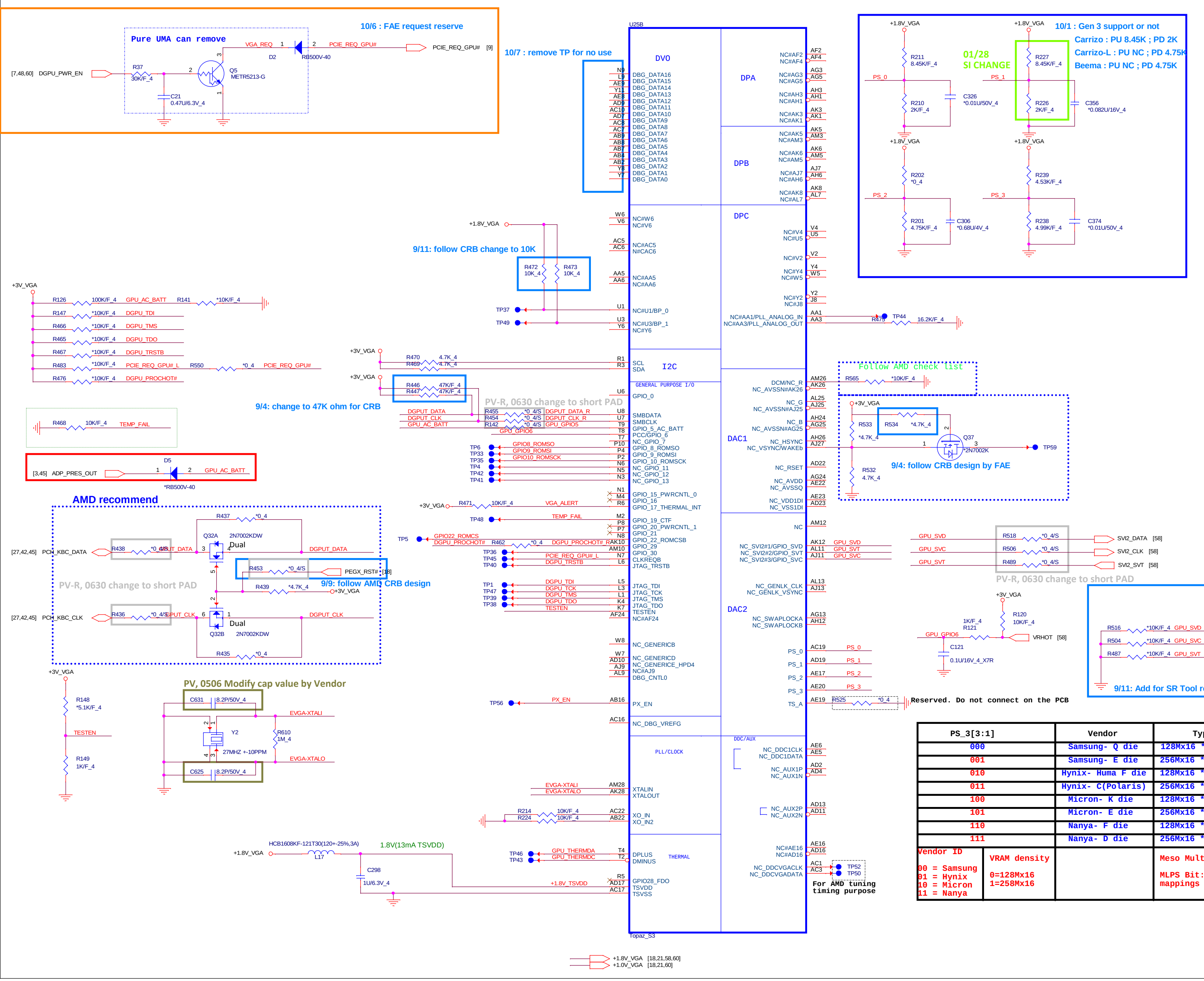
PROJECT : S400 Series

Quanta Computer Inc.

NB5

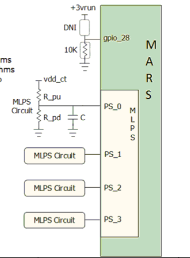
Size	Document Number	Rev
	18 -- Meso_S3_PCIE/DP POWER	1A

Date: Monday, November 30, 2015 Sheet 18 of 65



MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance



Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

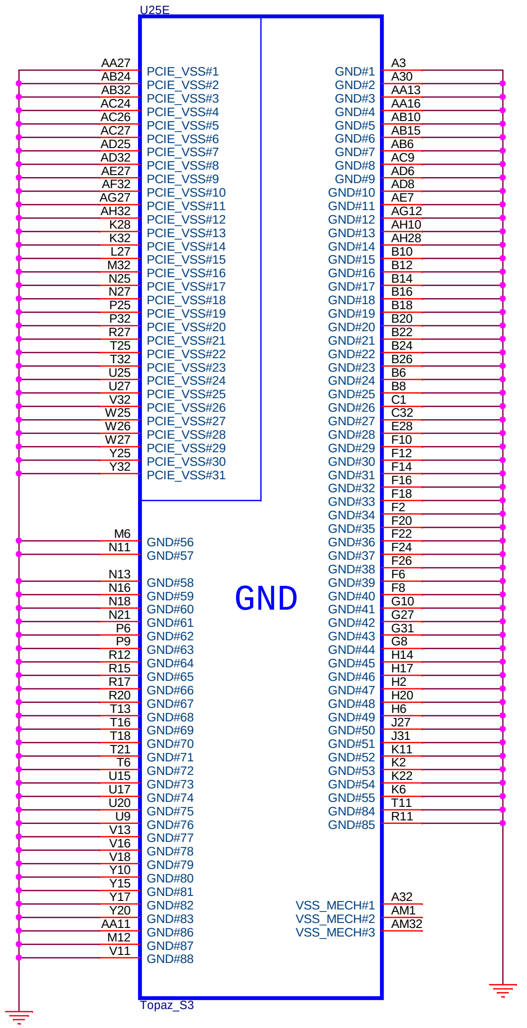
BIT5 => BIT0

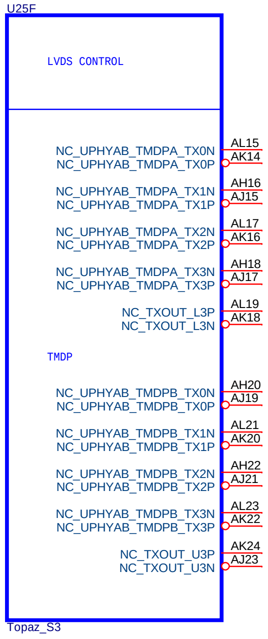
PS0 => 11001
PS1 => 11000
PS2 => 11000
PS3 => 11000

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. See Primary Memory Aperture Size (p. 29).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	N/A	Reserved.	1
PS_1[1]	STRAP_BIF_ GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[4]	N/A	Reserved.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[4]	N/A	Reserved.	1
PS_3[5]	N/A	Reserved.	1

PS_3[3:1]	Vendor	Type	Vendor P/N	QCI P/N	PU	PD
000	Samsung- Q die	128Mx16 *4, 900Mhz	K4W2G1646Q-BC1A	AKD5MGST508/AKD5MGST509	NC	4.75K
001	Samsung- E die	256Mx16 *4, 900Mhz	K4W4G1646E-BC1A	AKD5PGDT500/AKD5PGDT501	8.45K	2K
010	Hynix- Huma F die	128Mx16 *4, 900Mhz	H5TC2G63FFR-11C	AKD5MZDTW02/AKD5MZDTW03	4.53K	2K
011	Hynix- C(Polaris)	256Mx16 *4, 900Mhz	H5TC4G63CFR-N0C	AKD5PZDTW01/AKD5PZDTW02	6.98K	4.99K
100	Micron- K die	128Mx16 *4, 900Mhz	MT41J128M16JT-093G:K	AKD5MGSTL16/AKD5MGSTL17	4.53K	4.99K
101	Micron- E die	256Mx16 *4, 900Mhz	MT41J256M16HA-093G:E	AKD5PZSTL00/AKD5PZSTL01	3.24K	5.62K
110	Nanya- F die	128Mx16 *4, 900Mhz	NT5CB128M16FP-FL	AKD5MGDTF00/AKD5MGDTF01	3.4K	10K
111	Nanya- D die	256Mx16 *4, 900Mhz	NT5CB256M16DP-FL	Apply New P/N	4.75K	NC

Vendor ID 00 = Samsung 01 = Hynix 10 = Micron 11 = Nanya	VRAM density 0=128Mx16 1=258Mx16		Meso Multi-level Pin Straps MLPS Bit: PS_3 mappings between the bit values and resistor values





CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

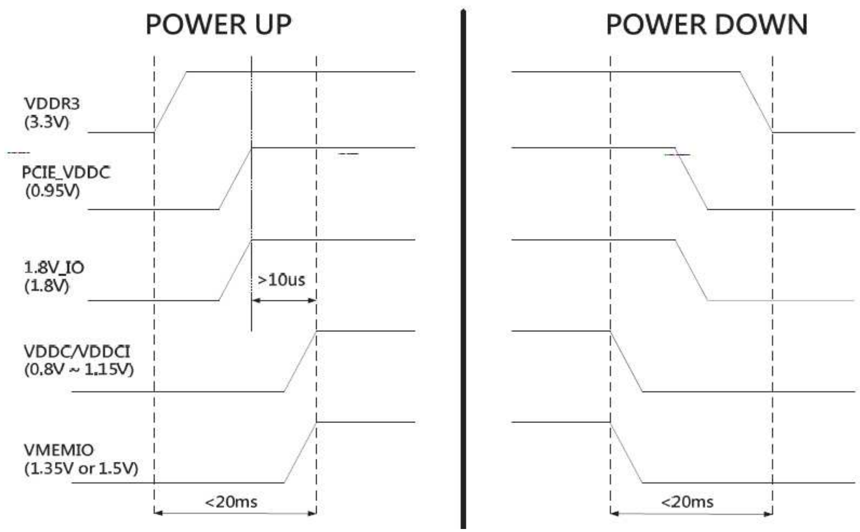
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

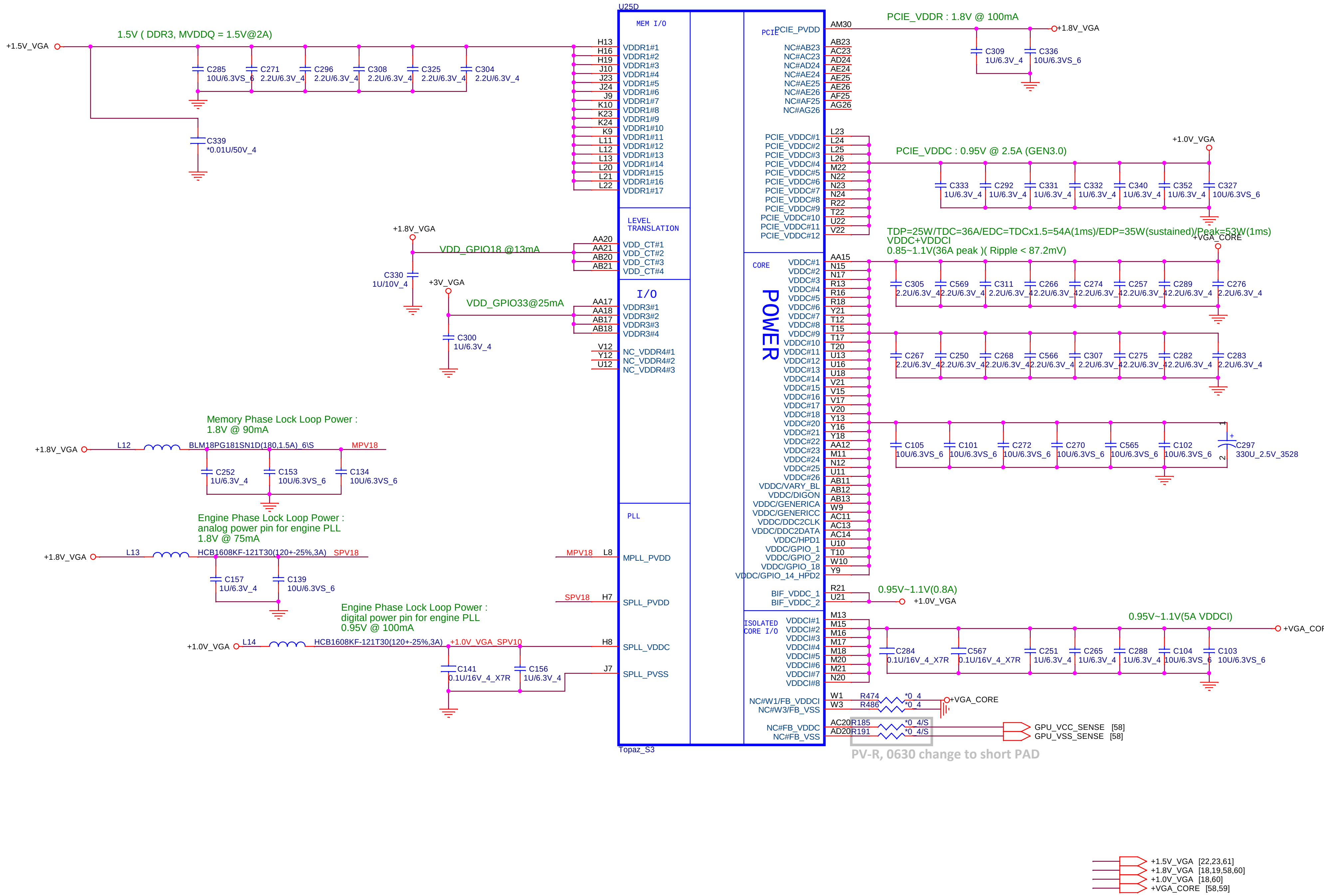
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

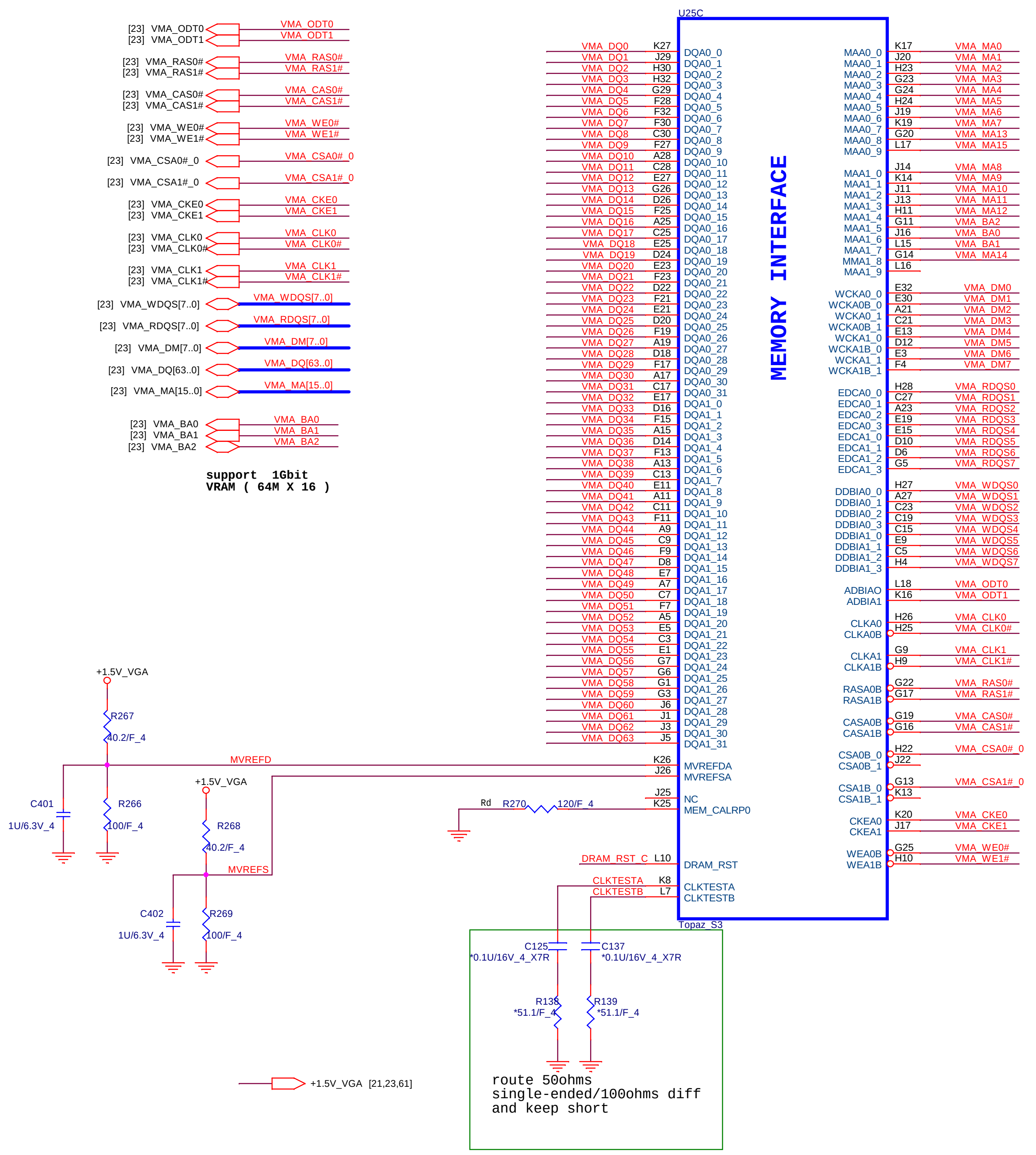
POWER UP / POWER DOWN SEQUENCE

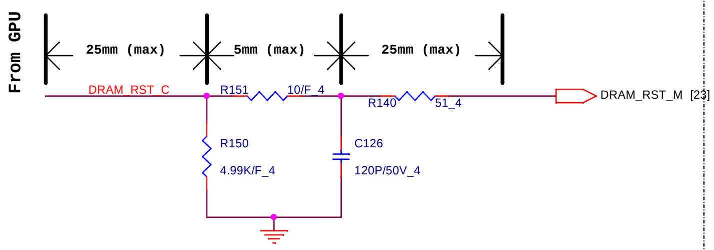


NB5	**PROJECT : S400 Series** Quanta Computer Inc.	
Size	Document Number: **20 -- Meso_S3_GND/LVDS/Strap**	Rev 1A
Date: Tuesday, November 17, 2015	Sheet 20 of 65	



NB5	**PROJECT : S400 Series** Quanta Computer Inc.	
Size	Document Number 21 -- Meso_S3_Power	Rev 1A
Date: Monday, November 30, 2015	Sheet 21 of 65	



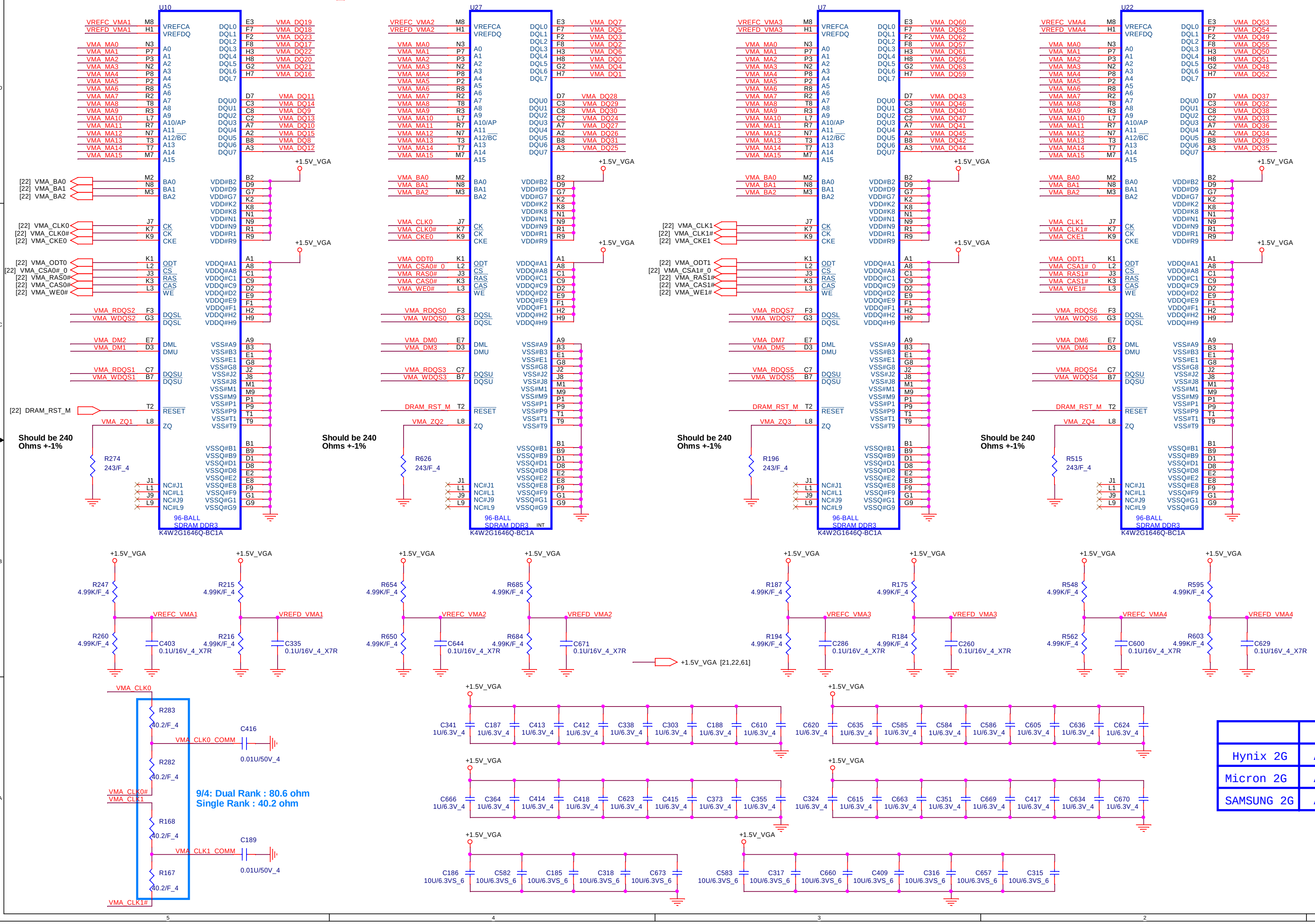


Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

NB5	**PROJECT : S400 Series**	
	Quanta Computer Inc.	
Size	Document Number: 22 -- Meso_S3_MEM_Interface	Rev: 1A
Date: Monday, November 30, 2015	Sheet 22 of 65	

1G/2G DDR3L



	QBCON PN
Hynix 2G	AKD5PGWTW08
Micron 2G	AKD5PZSTL01
SAMSUNG 2G	AKD5PGWT501

NB5

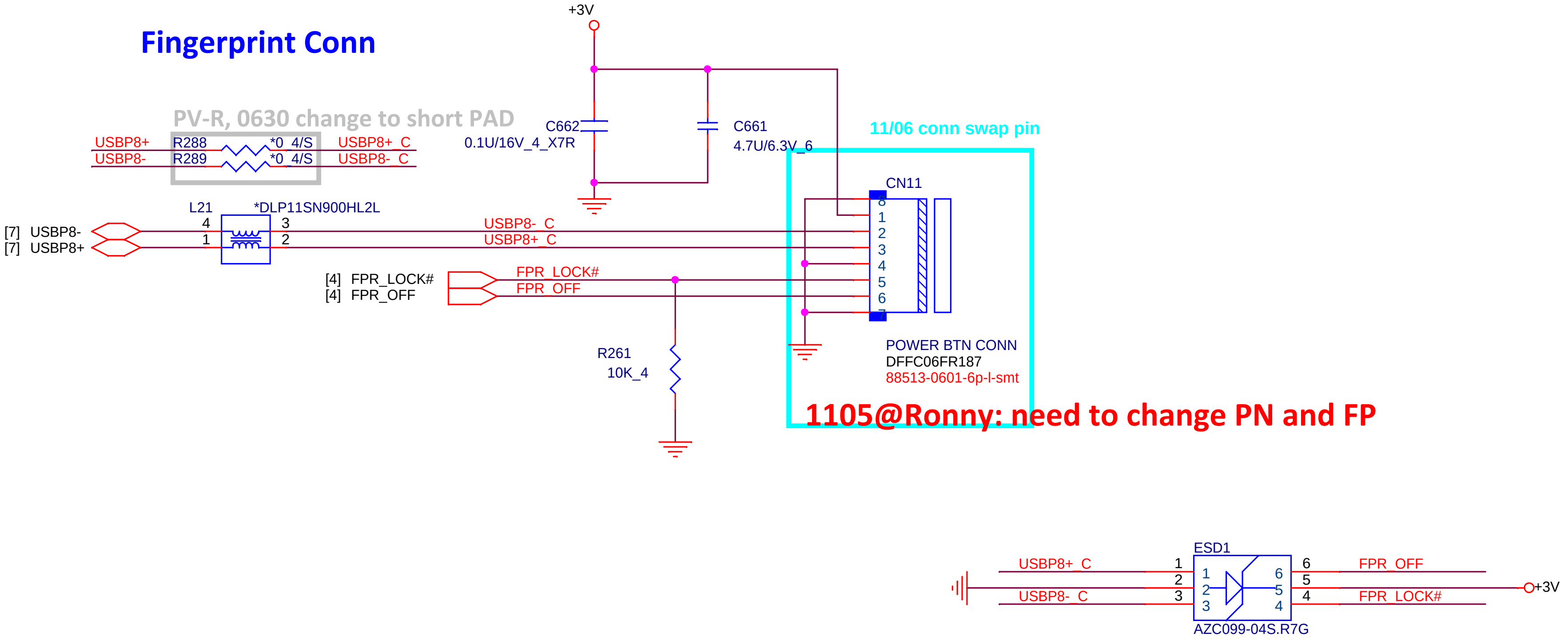
PROJECT : S400 Series

Quanta Computer Inc.

Size	Document Number	Rev
Custom	23 -- Meso_S3_VRAM_DDR3L BGA96	1A

Date: Tuesday, November 17, 2015 Sheet 23 of 65

Fingerprint Conn



PROJECT : S400 Series
Quanta Computer Inc.

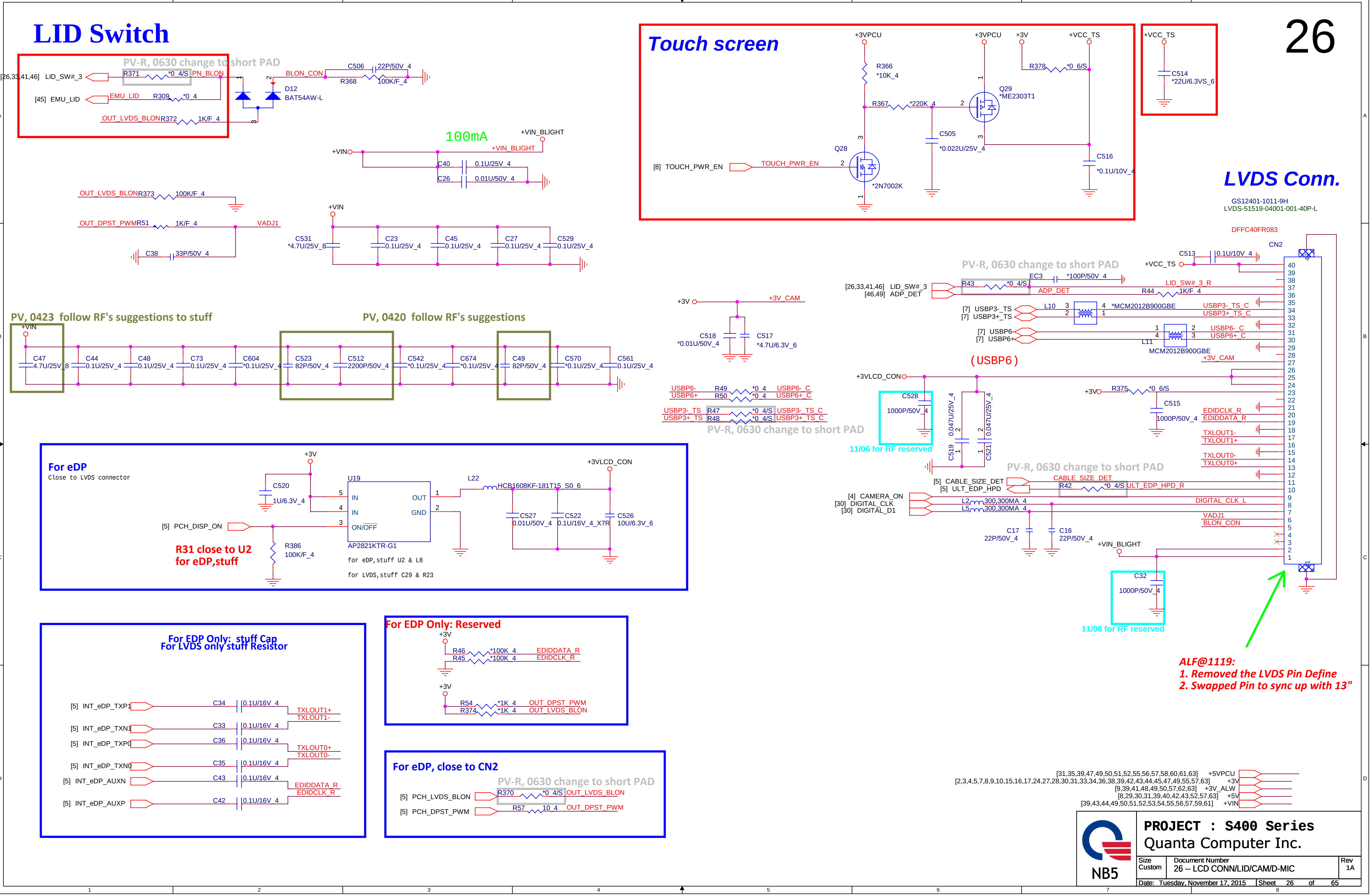
NB5

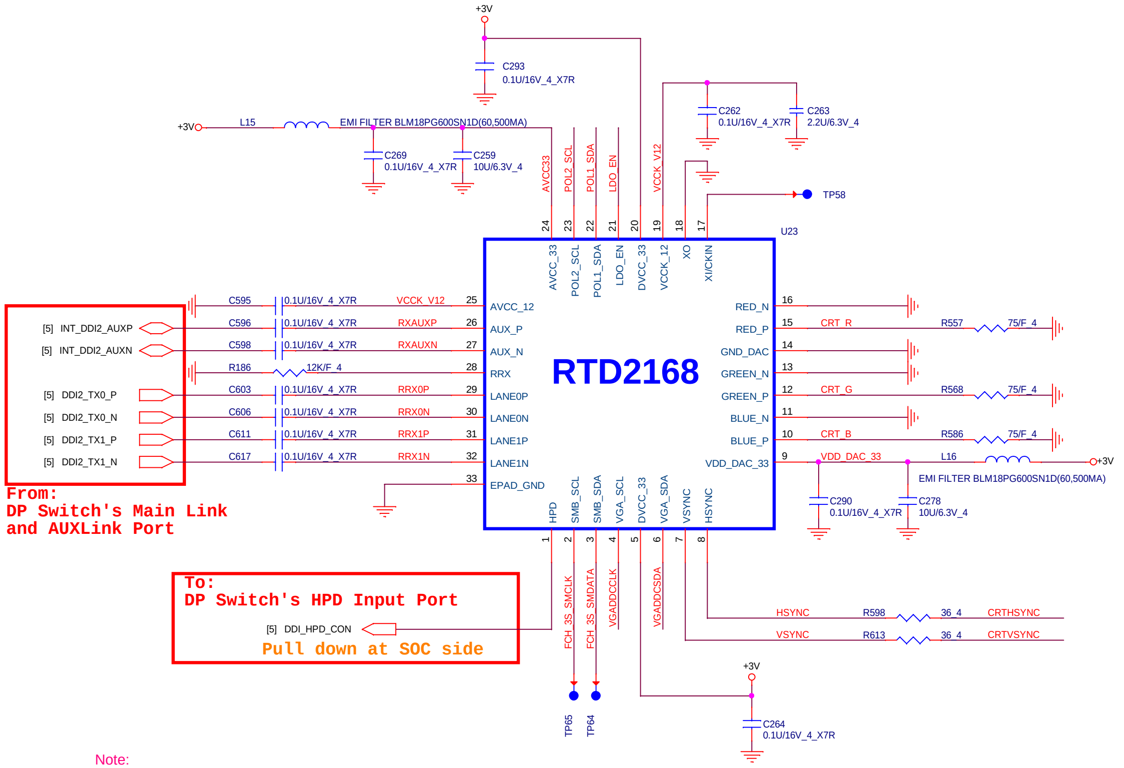
Size	Document Number	Rev
Custom	24 -- FPR	1A

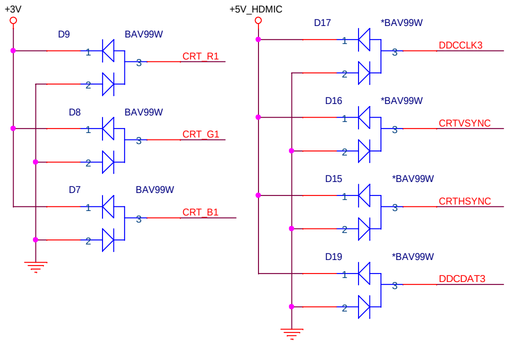
Date: Tuesday, November 17, 2015 | Sheet 24 of 65

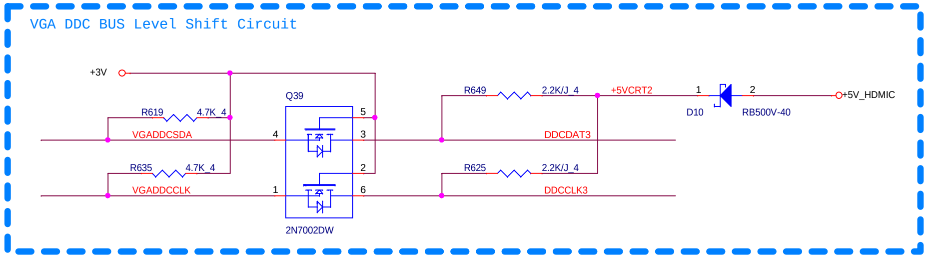
ALF@1119:
HP confirmed to remove the eDP to LVDS convertor.

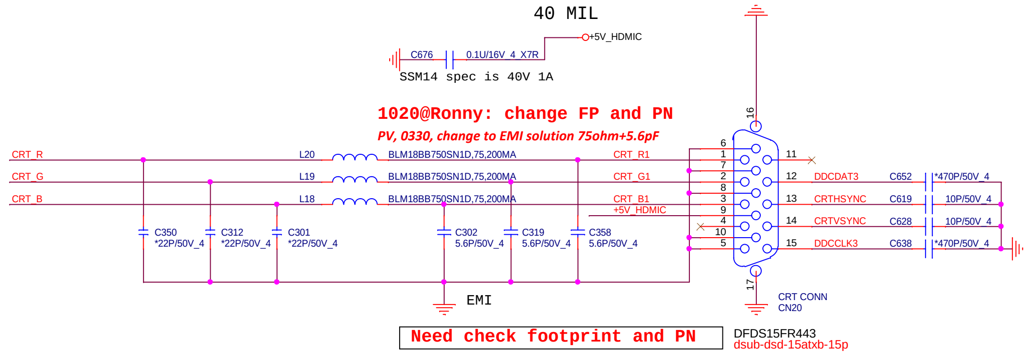
[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,39,42,43,44,45,47,49,55,57,63] +3V


26
LID Switch
PV-R, 0630 change to short PAD
100mA
Touch screen
LVDS Conn.
GS12401-1011-9H
LVDS-51519-04001-001-40P-L
DFFC40FR083
PV, 0423 follow RF's suggestions to stuff
PV, 0420 follow RF's suggestions
(USBP6)
11/06 for RF reserved
For eDP
Close to LVDS connector
R31 close to U2
for eDP,stuff
AP2821KTR-G1
for eDP,stuff U2 & L8
for LVDS,stuff C29 & R23
For EDP Only: stuff Cap
For LVDS only stuff Resistor
For EDP Only: Reserved
For eDP, close to CN2
ALF@1119:
1. Removed the LVDS Pin Define
2. Swapped Pin to sync up with 13"
PROJECT : S400 Series
Quanta Computer Inc.
NB5
Size Custom
Document Number 26 -- LCD CONN/LID/CAM/D-MIC
Rev 1A
Date: Tuesday, November 17, 2015
Sheet 26 of 65





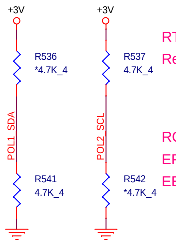




Note:
1- C1,C3,C6,C8,C9,C11,C12,C19,C20
Should be close to chip
2- C12 shold be X5R material
3- R1 should be 12K ohm with +/-1%
4- R8, R9, R10 should be 75 ohm with +/-1%

Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE



RTD2168 Supports three operation mode for system design.
Reserve 4.7K resistor pull high/low for mode selection

ROM ONLY Mode : PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high

EEPROM MODE

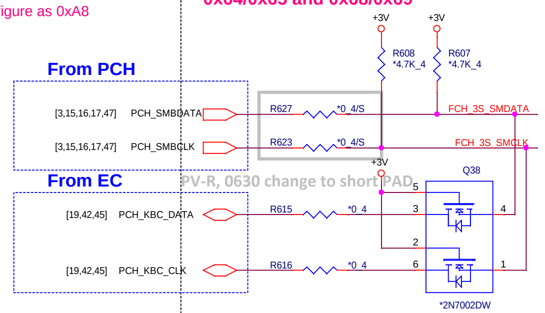
In EEPROM mode,an additional EEPROM is needed.
EEPROM should configure with following conditions.

1- EEPROM with a size of 16K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

CIIC_SCL, CIIC_SDA Connection

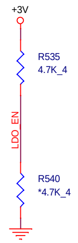
EP mode: Pin2, Pin3 connect to EC SMBUS
ROM or EEPROM mode: connect to PCH SMBUS
IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69

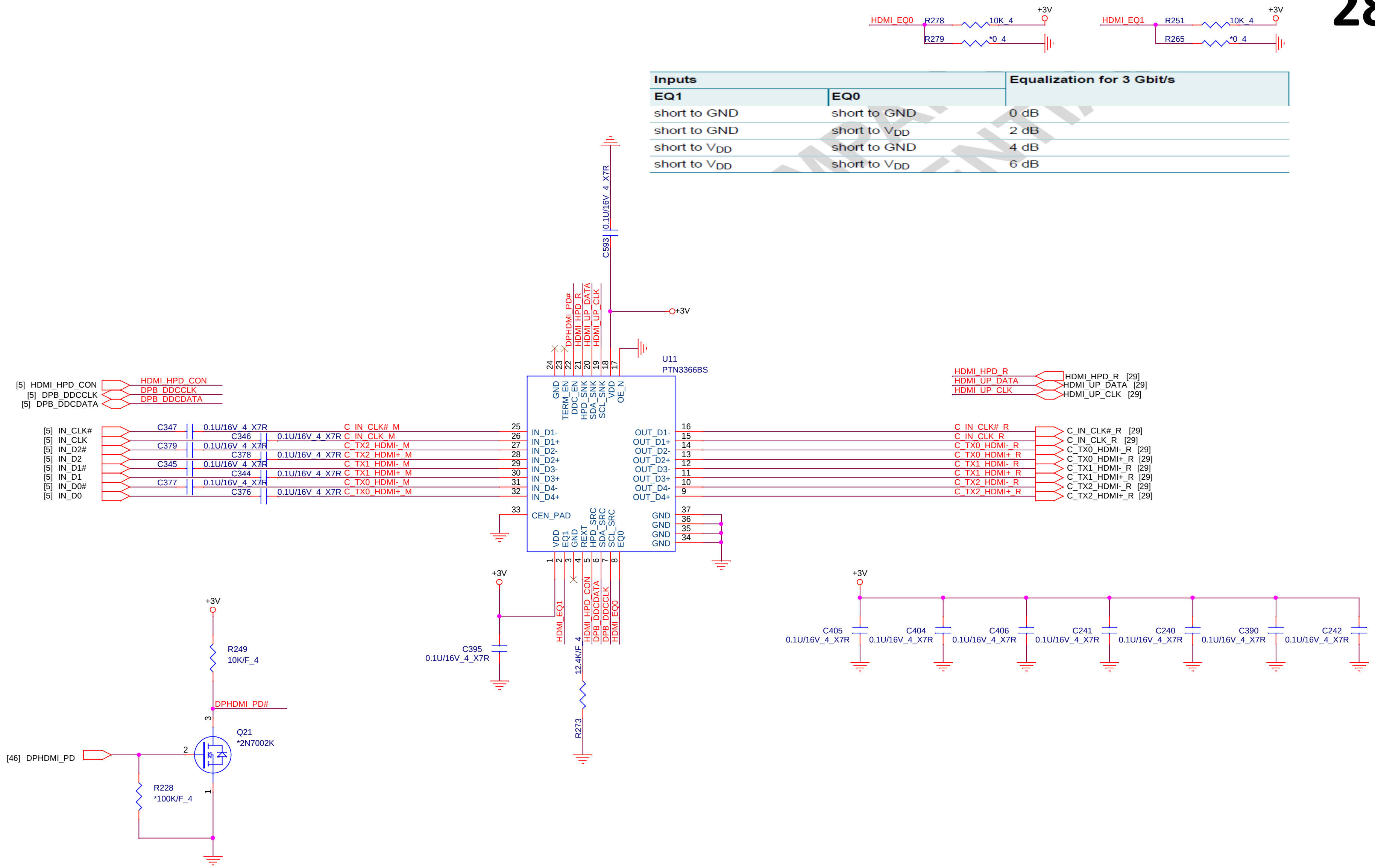


Embedded LDO

Select VCCK_V12 source from external 1.2V or embedded LDO



LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO



Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V_{DD}	2 dB
short to V_{DD}	short to GND	4 dB
short to V_{DD}	short to V_{DD}	6 dB

OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

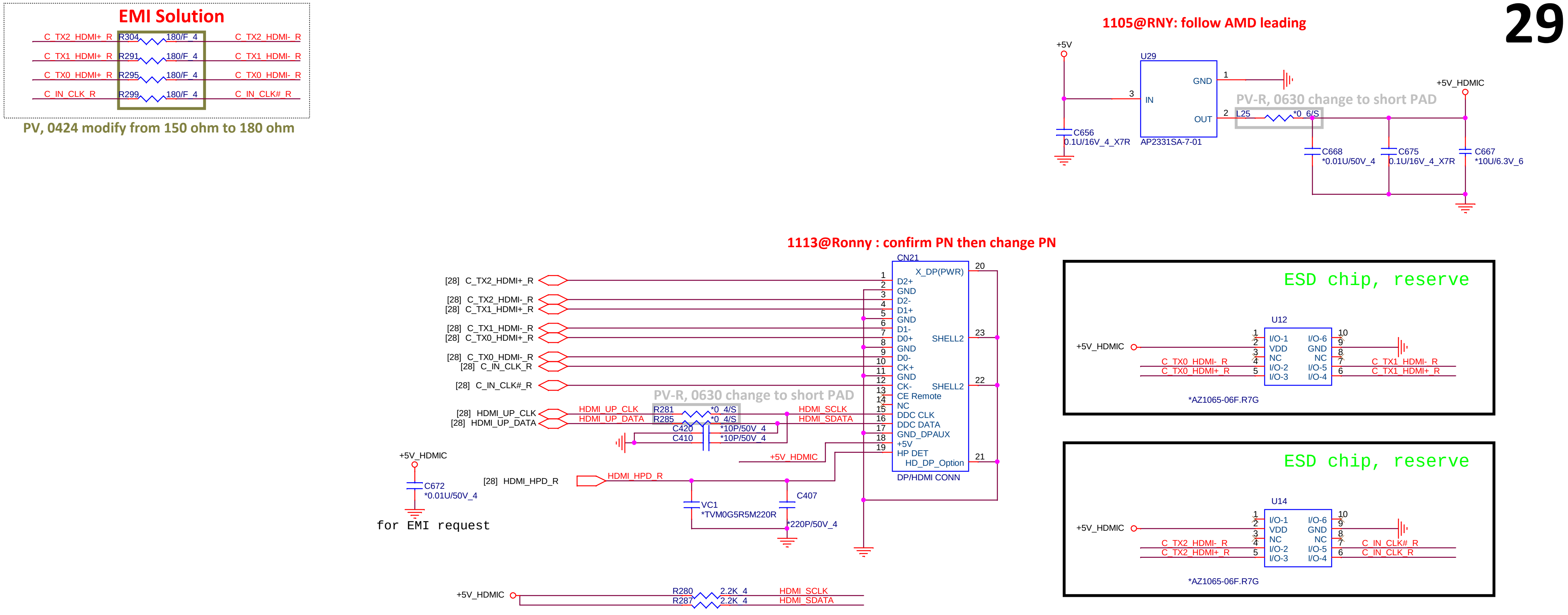
PROJECT : S400 Series

Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	28 -- REPEATER PTN3366	1A

Date: Tuesday, November 17, 2015 Sheet 28 of 65



PROJECT : S400 Series

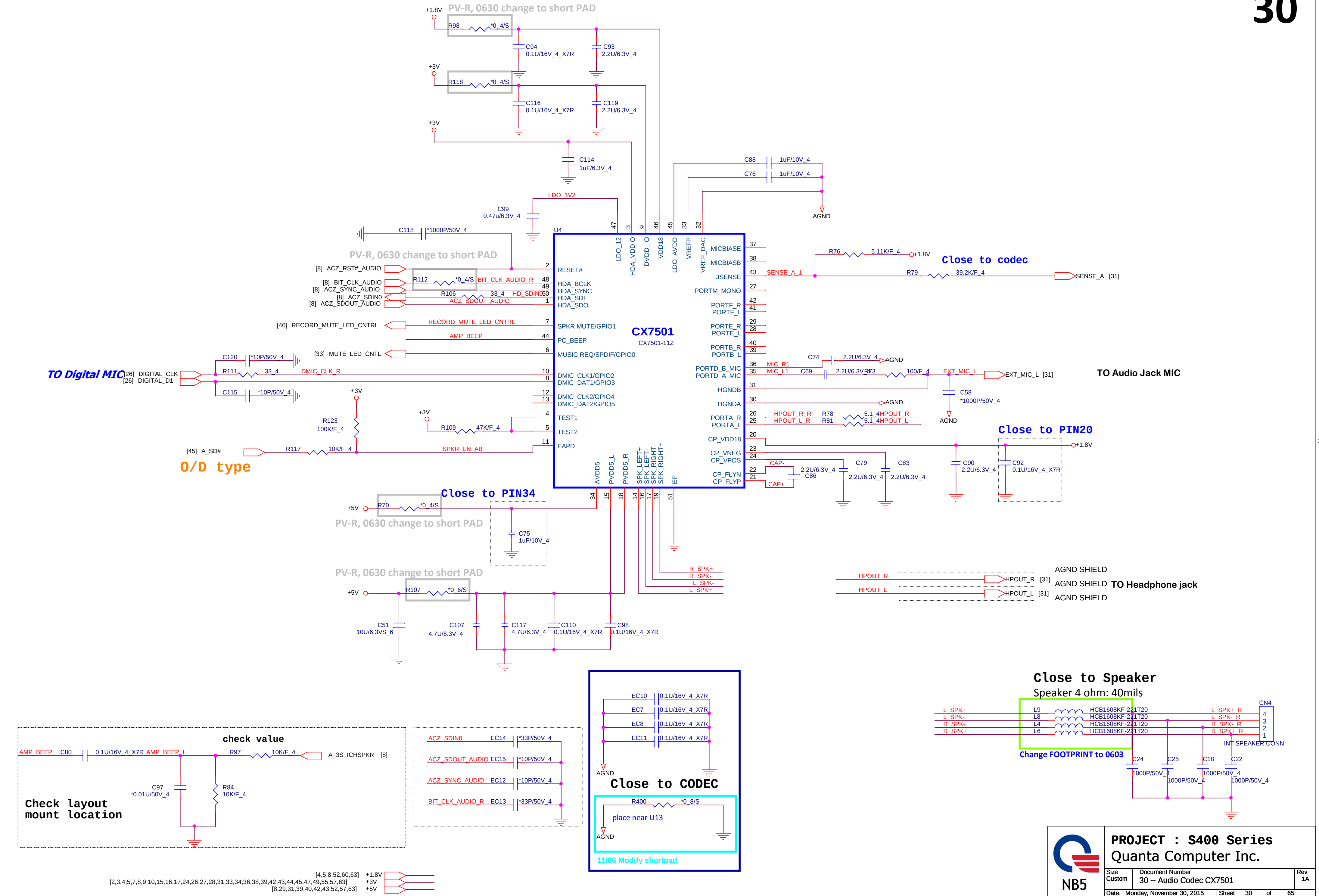
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	29 -- HDMI CONNECTOR	1A

Date: Tuesday, November 17, 2015 Sheet 29 of 65

Audio Codec



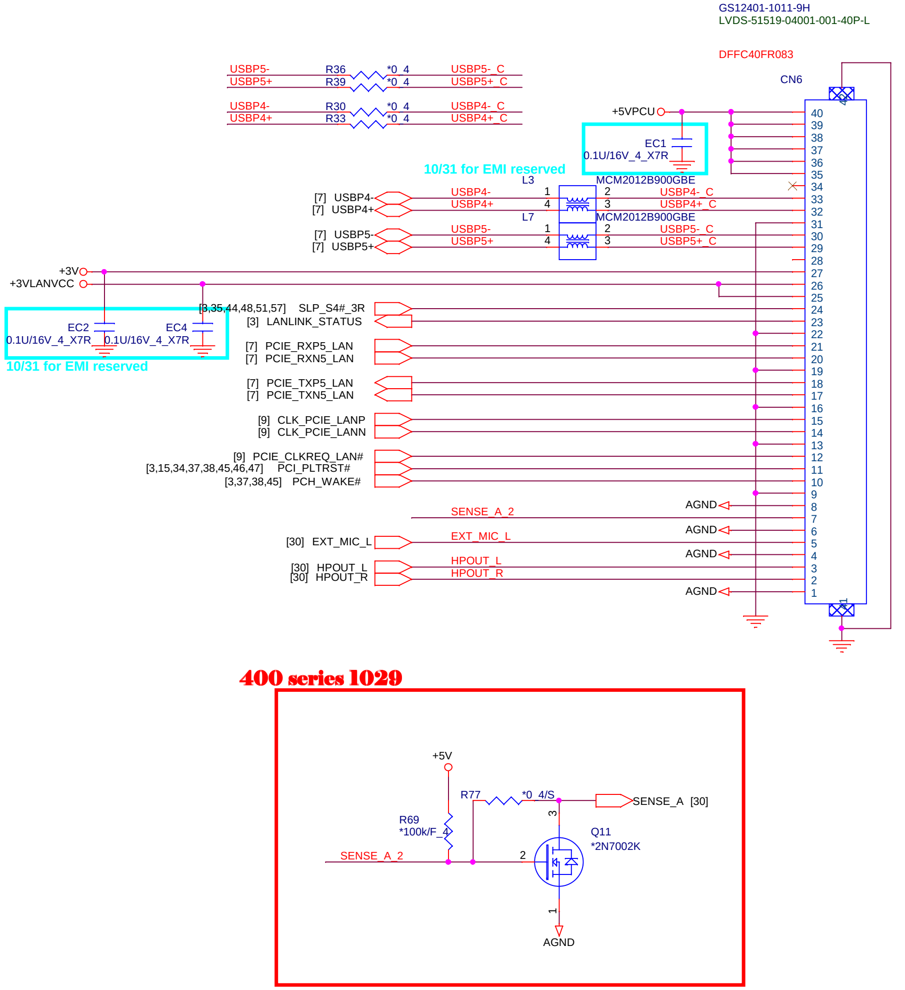
NB5

PROJECT : S400 Series
Quanta Computer Inc.

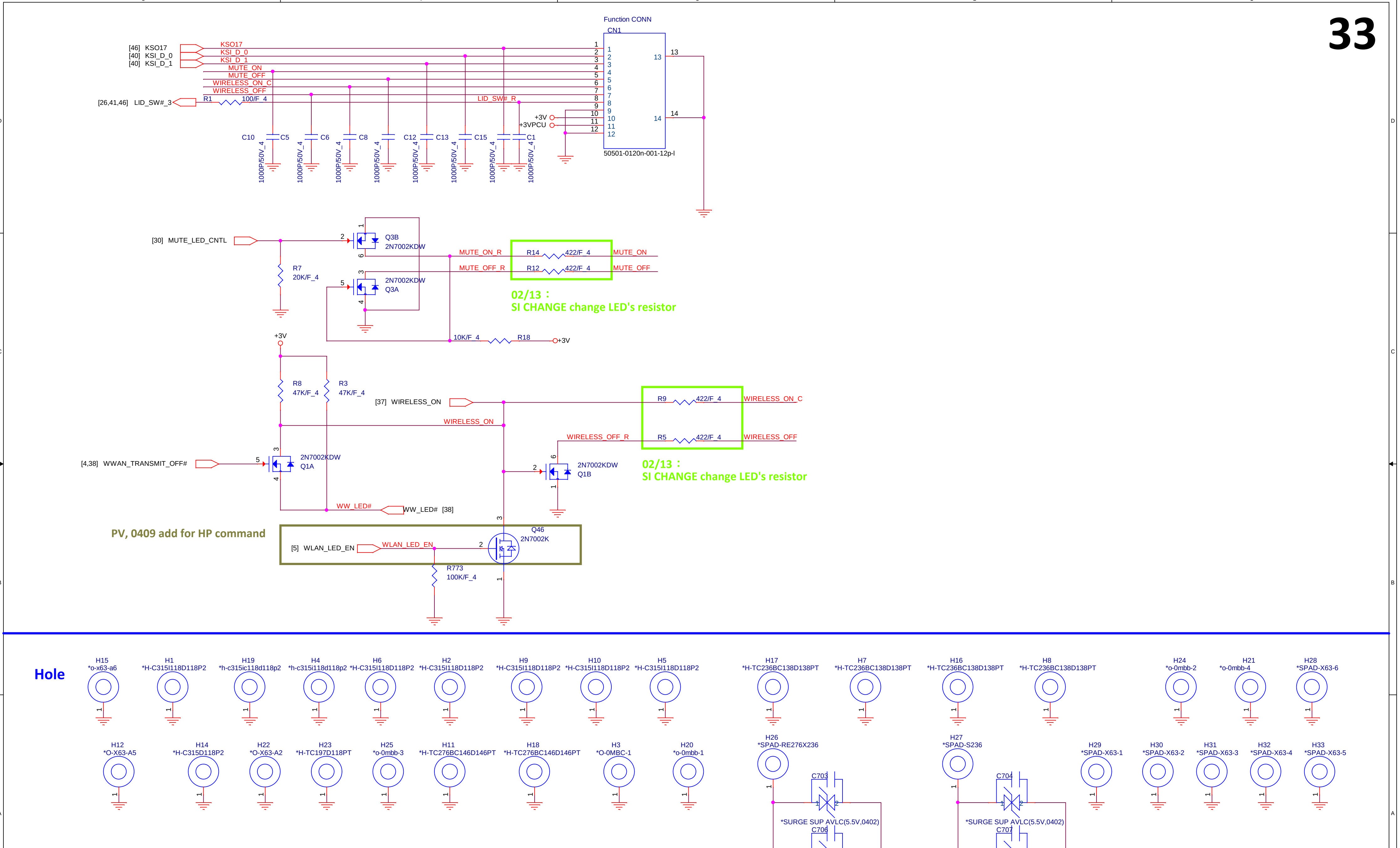
Size	Document Number	Rev
Custom	30 -- Audio Codec CX7501	1A

Date: Monday, November 30, 2015 Sheet 30 of 65

USB2.0 x2/LAN/Headphone_Mic Combo Jack Daugther Board Connector



	PROJECT : S400 Series	
NB5	Quanta Computer Inc.	
Size: Custom	Document Number: 31 -- DAUGTHER BOARD CONN.	Rev: 1A
Date: Tuesday, November 17, 2015	Sheet 31 of 65	



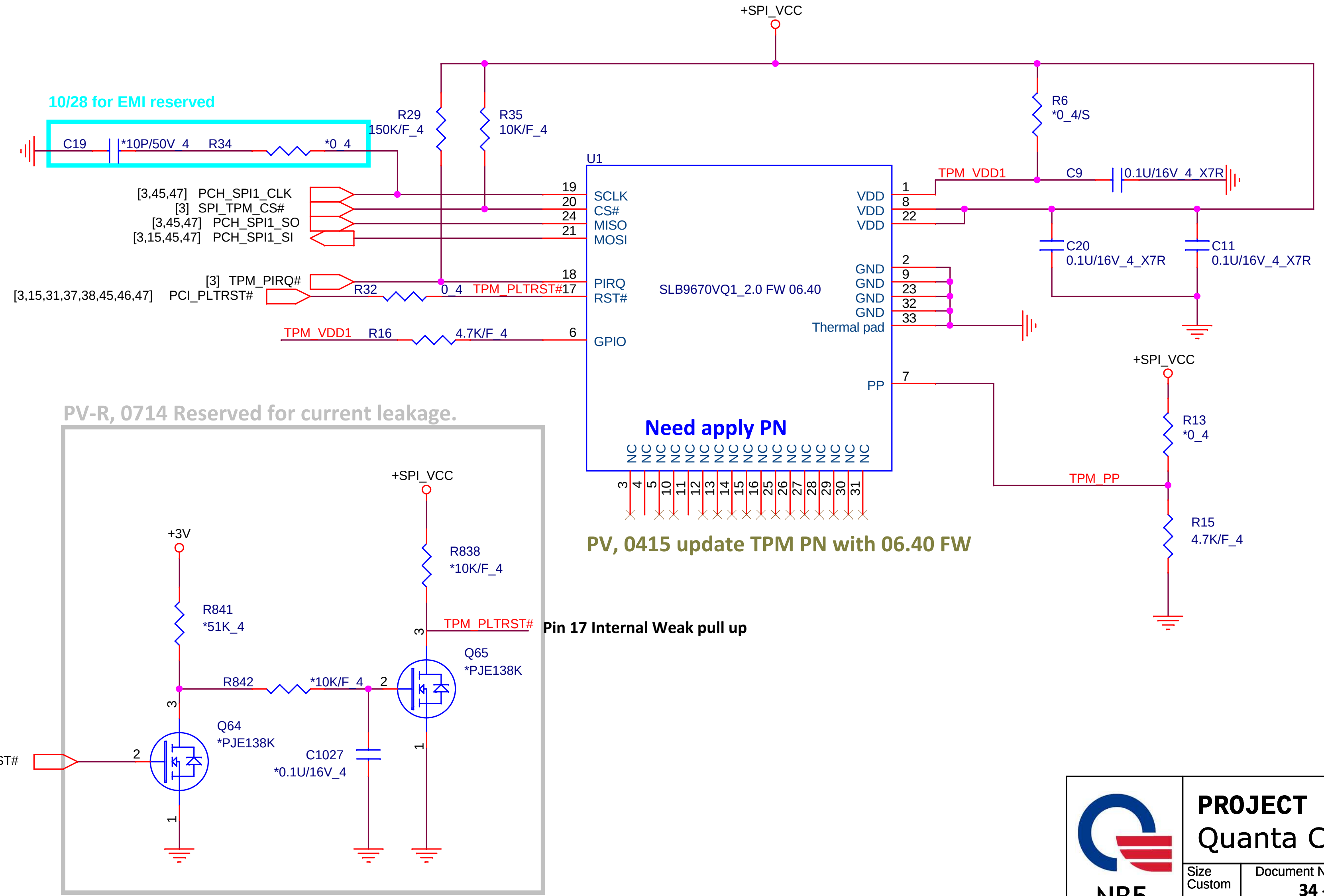
NB5

PROJECT : S400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	33 -- Function Conn./Hole	1A

Date: Tuesday, November 17, 2015 Sheet 33 of 65

TPM (1.2 or 2.0)



PROJECT : S400 Series

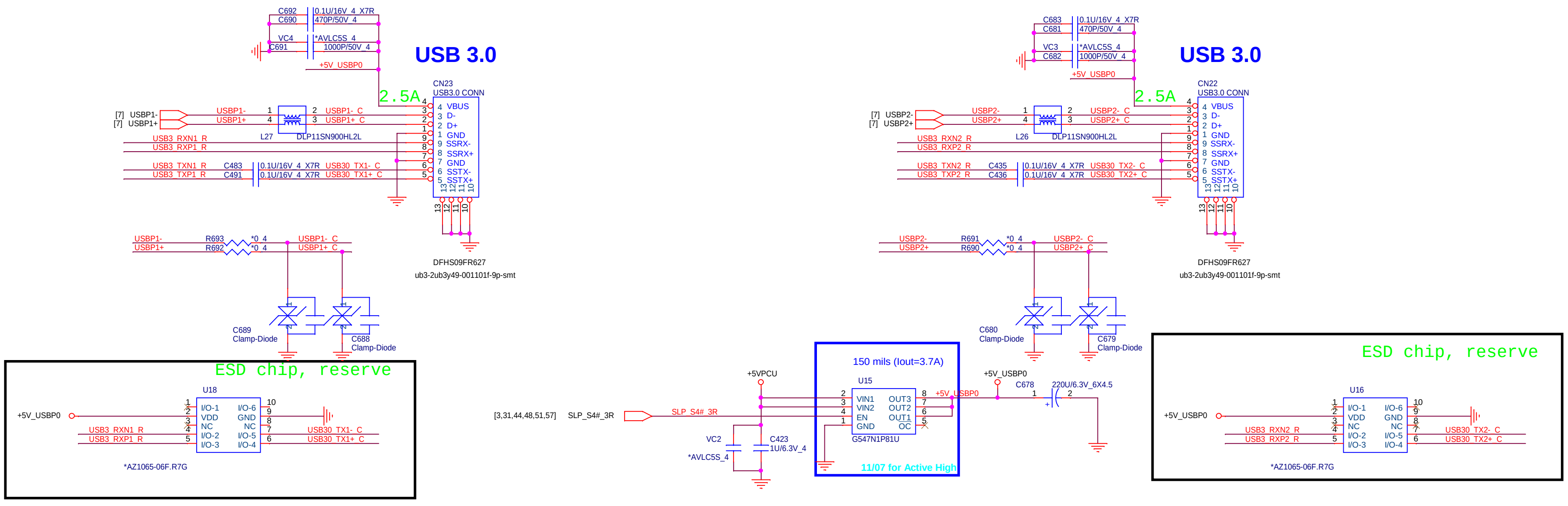
Quanta Computer Inc.

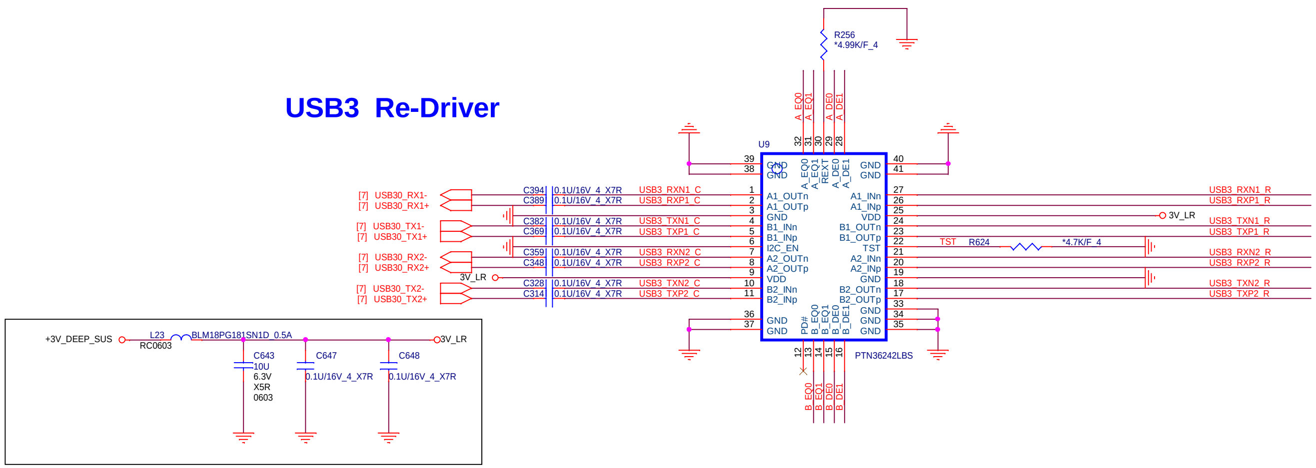
NB5

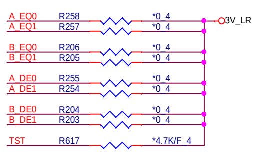
Size	Document Number	Rev
Custom	34 -- TPM SLB9670_QFN	1A

Date: Monday, November 30, 2015 | Sheet 34 of 65

USB 2.0/3.0 Combo

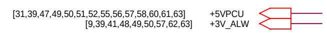






A_EQ0	A_EQ1		A_DE0	A_DE1	
B_EQ0	B_EQ1		B_DE0	B_DE1	
0	0	9dB	0	0	-3.5dB
0	1	3dB	0	1	no de-emphasis
1	0	6dB	1	0	-7dB
1	1	7.5dB	1	1	-5dB

TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing



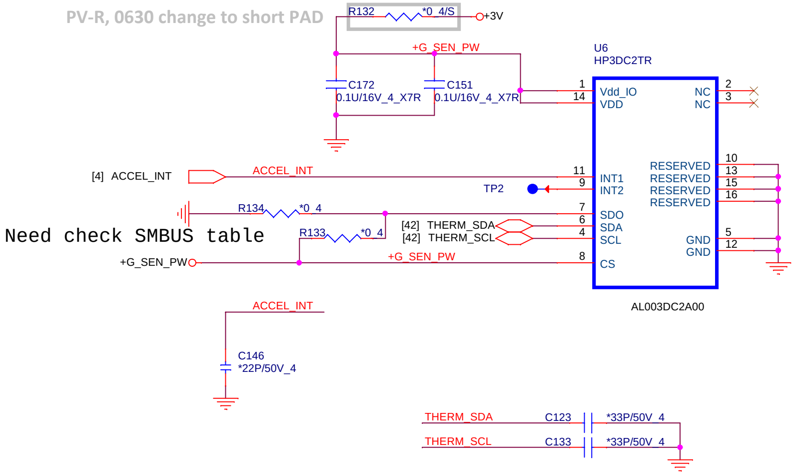
PROJECT : S400 Series
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	35 -- USB3.0 x2	1A

Accelerometer Sensor

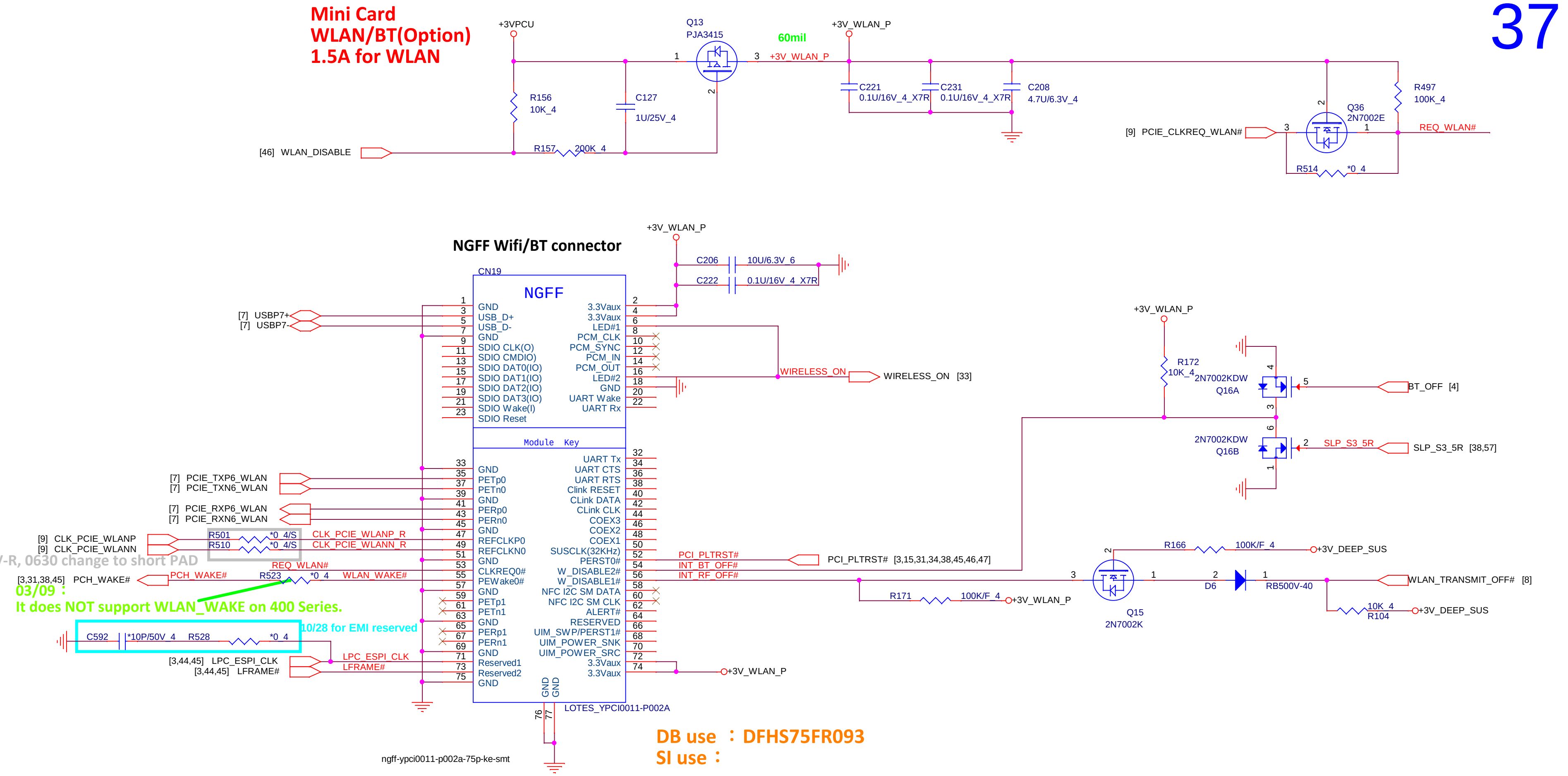
G-Sensor Power need check



[31,35,39,47,49,50,51,52,55,56,57,58,60,61,63] +5VPCU
[9,39,41,48,49,50,57,62,63] +3V_ALW

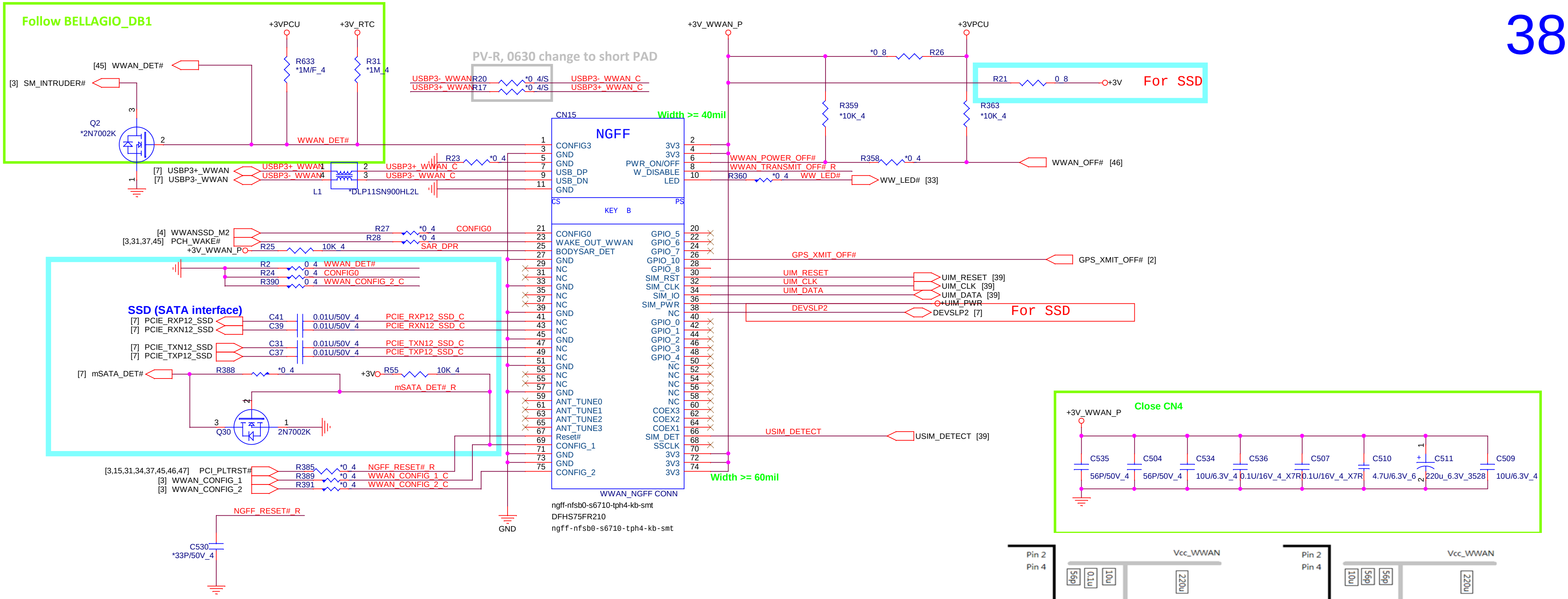
NGFF WLAN/BT

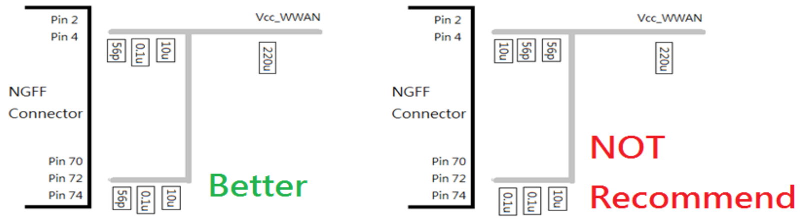
EC-B-03



[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,39,42,43,44,45,47,49,55,57,63] +3V
[8,29,30,31,39,40,42,43,52,57,63] +5V
[9,39,41,48,49,50,57,62,63] +3V_ALW

PROJECT : S400 Series	
Quanta Computer Inc.	
Size: Custom	Document Number: 37 -- NGFF WLAN/BT	Rev: 1A
Date: Thursday, November 26, 2015	Sheet 37 of 65

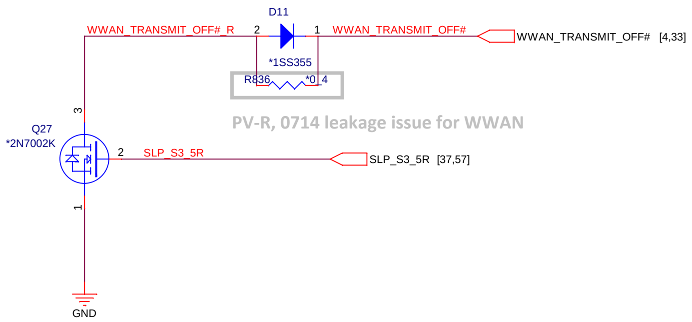




WWAN(Option)

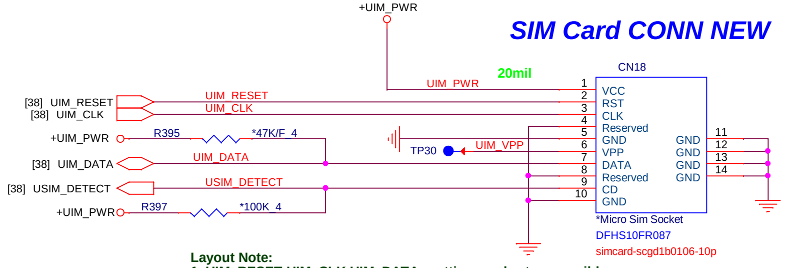
Control of power must be allowed in all S0, S3, S4 and S5 states.

	M.2 Pinout	S0	S3 – S5
WWAN 3.3V	2, 4, 70, 72, 74	On	Off

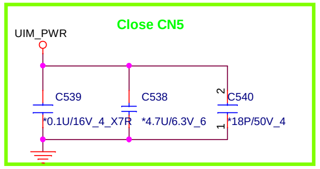


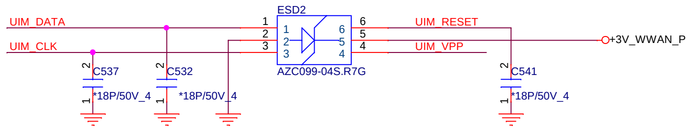
	+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0	ON	High	High	High
S3	ON	High	Low	Low
S4	ON	Low	Low	Low
S5	ON	Low	Low	Low

SIM Card CONN NEW



Layout Note:
1. UIM_RESET,UIM_CLK,UIM_DATA routting as short as possible
Roue into ESD then go out
2. Avoid routing the SIM_CLK and SIM_DATA lines in parallel over distances >= 2 cm
3. Position the SIM connector from the WWAN module <= 100mm if possible,
NOT exceed length is 150mm.





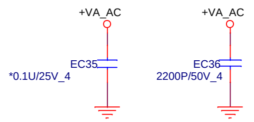
Trace Length and Routing

- Special attention should be paid to SIM traces (UIM_CLK, UIM_DATA and UIM_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.
- Minimum distance between UIM_CLK and UIM_DATA should be 20 mils. Static signals such as UIM_RST can be routed between UIM_CLK and UIM_DATA to conserve space if needed.
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM_CLK, UIM_DATA and any other high-speed switching signals.
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.

SIM Power

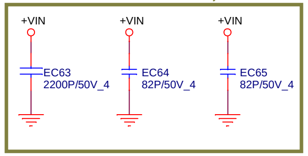
- The UIM_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM_PWR supply and locate near the SIM connector.

EMI cap



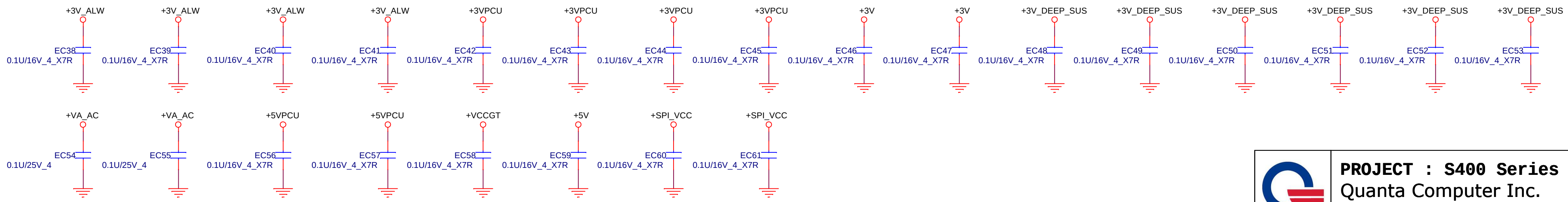
RF cap

PV, 0423 add

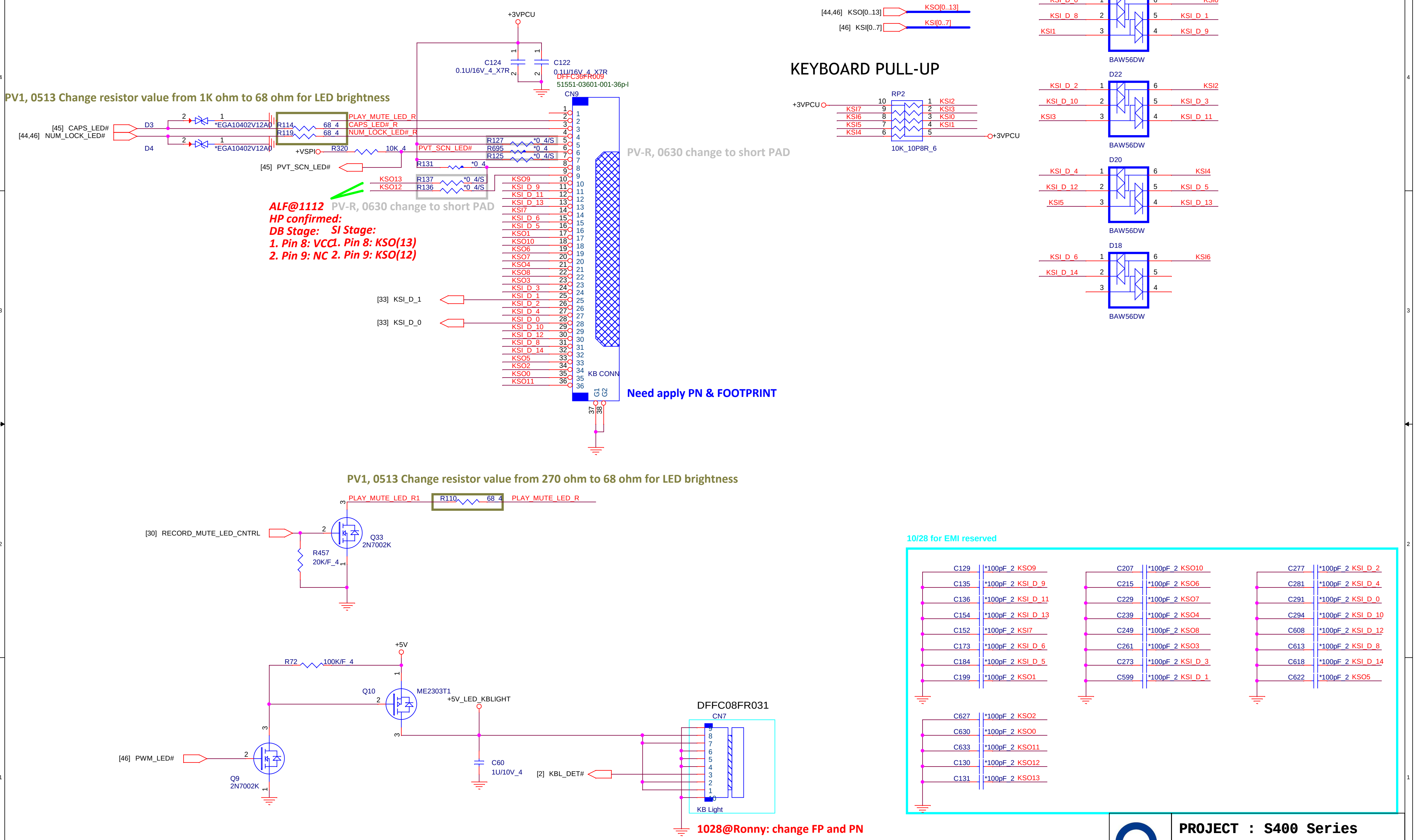


EMI cap

SI : 2/2 Add



KEYBOARD Con.



[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,39,42,43,44,45,47,49,55,57,63] +3V
[8,29,30,31,39,42,43,52,57,63] +5V
[9,39,41,48,49,50,57,62,63] +3V_ALW

NB5

PROJECT : S400 Series

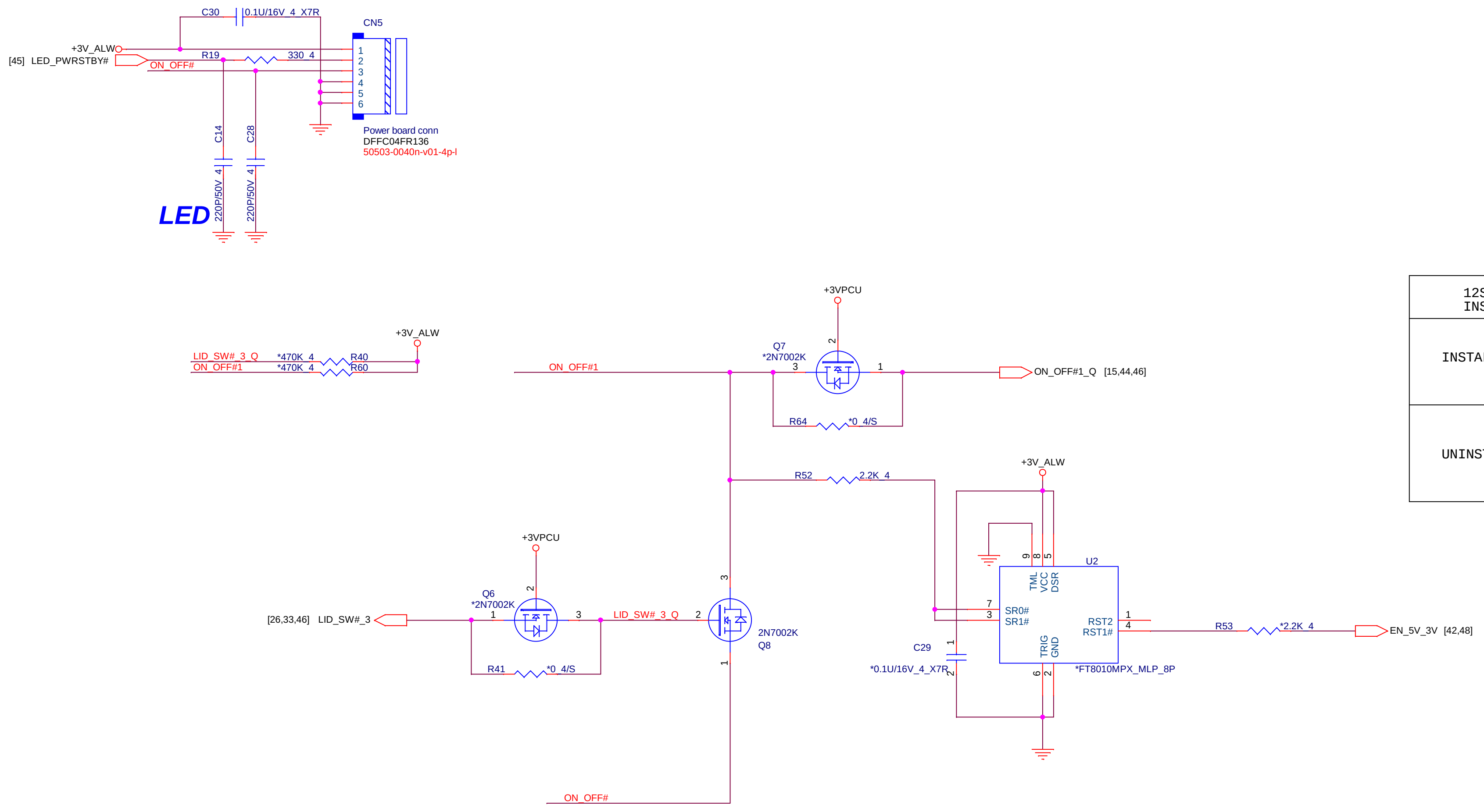
Quanta Computer Inc.

Size	Document Number	Rev
Custom	40 -- KB/ KB light CONN	1A

Date: Tuesday, November 17, 2015 Sheet 40 of 65

Power Botton Connector

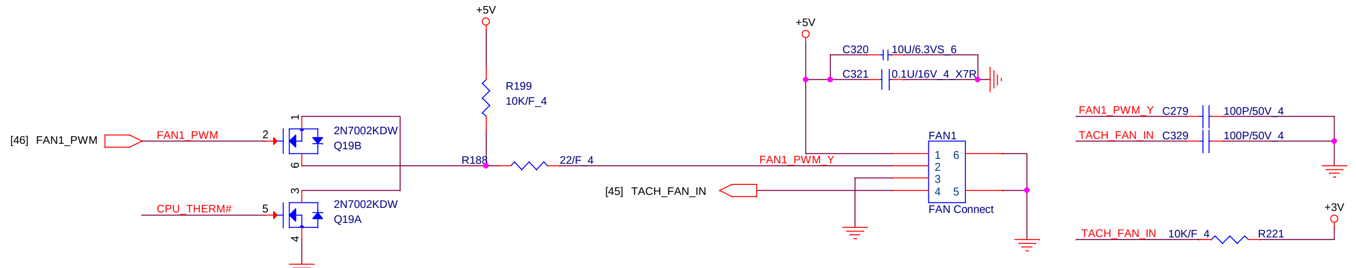
1112@RNY: change to 4Pin FP and PN



12S RESET MODE INSTAL FOR DB0	
INSTAL	R10702 R10703 R10704 R? R10701 R? U9068
UNINSTAL	R? R? Q7080 Q7081

[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,39,42,43,44,45,47,49,55,57,63] +3V
[8,29,30,31,39,40,42,43,52,57,63] +5V
[9,39,48,49,50,57,62,63] +3V_ALW

FAN

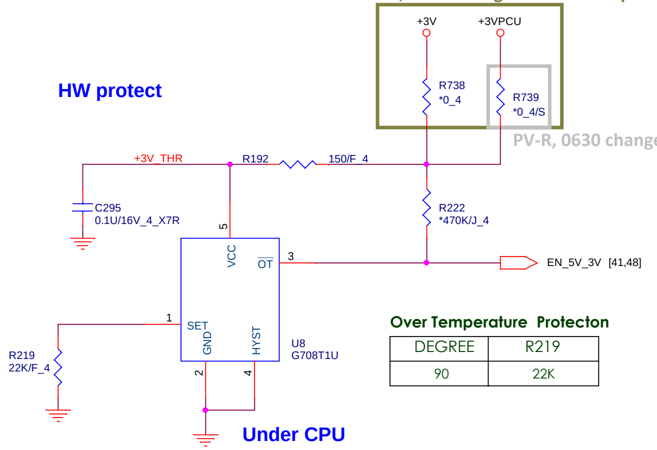


@1217:
Changed the Pin Define as Rex

Thermal sensor

PV, 0417 Change HW thermal protect to +3VPCU

HW protect

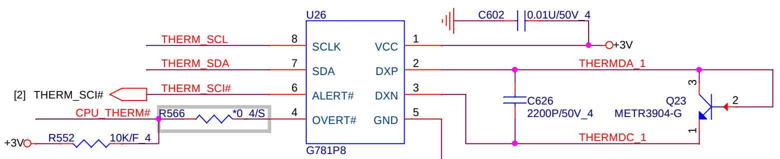


Under CPU

Over Temperature Protecton

DEGREE	R219
90	22K

CPU Thermal Sensor



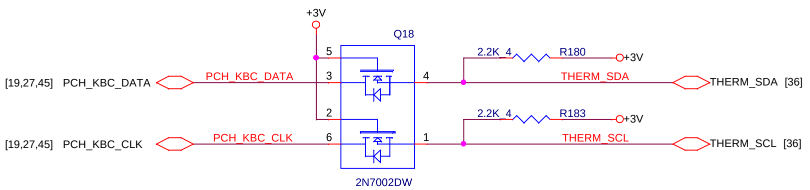
PV-R, 0630 change to short PAD

Under Heat Pipe

Main: AL000781012 G781P8(98h)

2nd:AL000431014 TMP431ADGKR

RSET (K OHM) = 0.0012T^2 - 0.9308T + 96.147

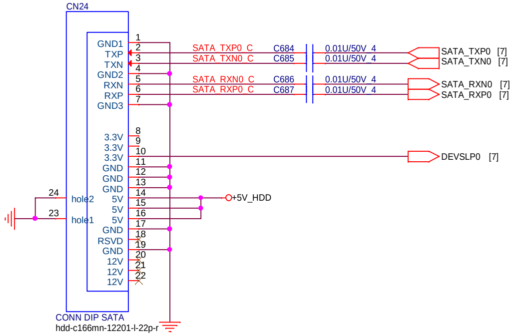


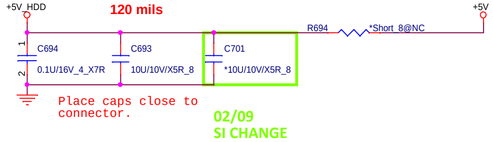
[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,39,43,44,45,47,49,55,57,63] +3V
[9,39,41,48,49,50,57,62,63] +3V_ALW

PROJECT : S400 Series
Quanta Computer Inc.
NB5

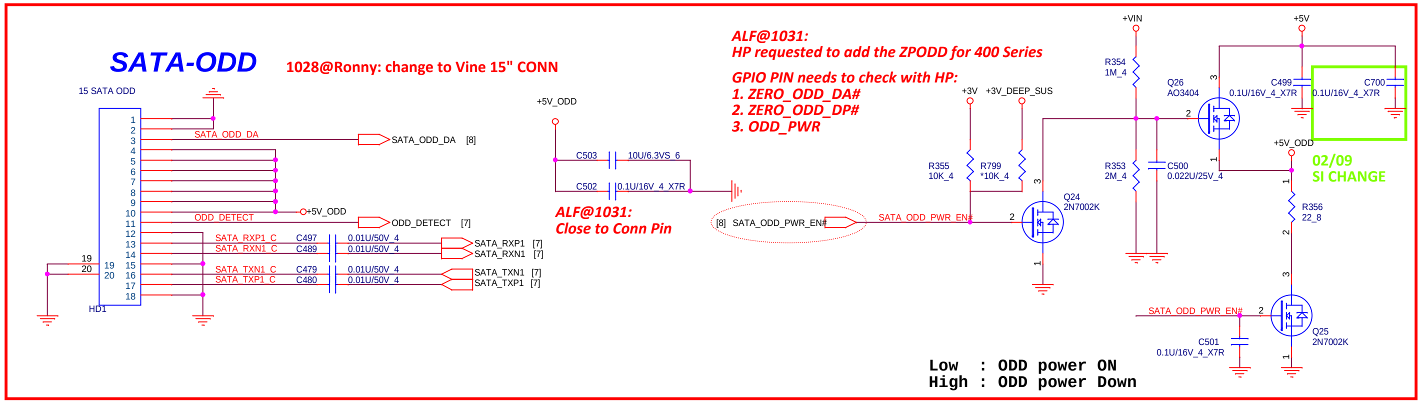
Size	Document Number	Rev
Custom	42-- FAN and Thermal IC	1A

SATA-HDD

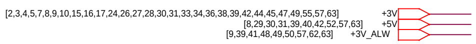




SATA-ODD



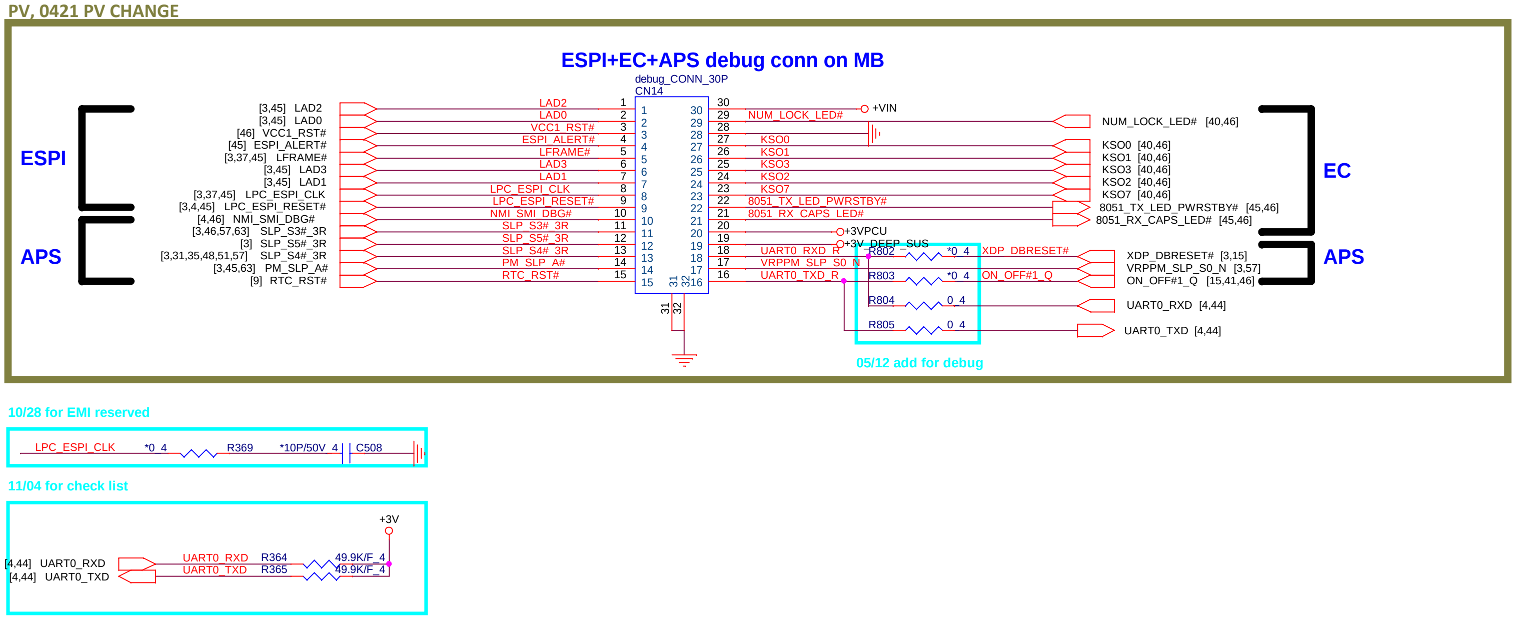
EMI cap



PROJECT : S400 Series
Quanta Computer Inc.
NB5

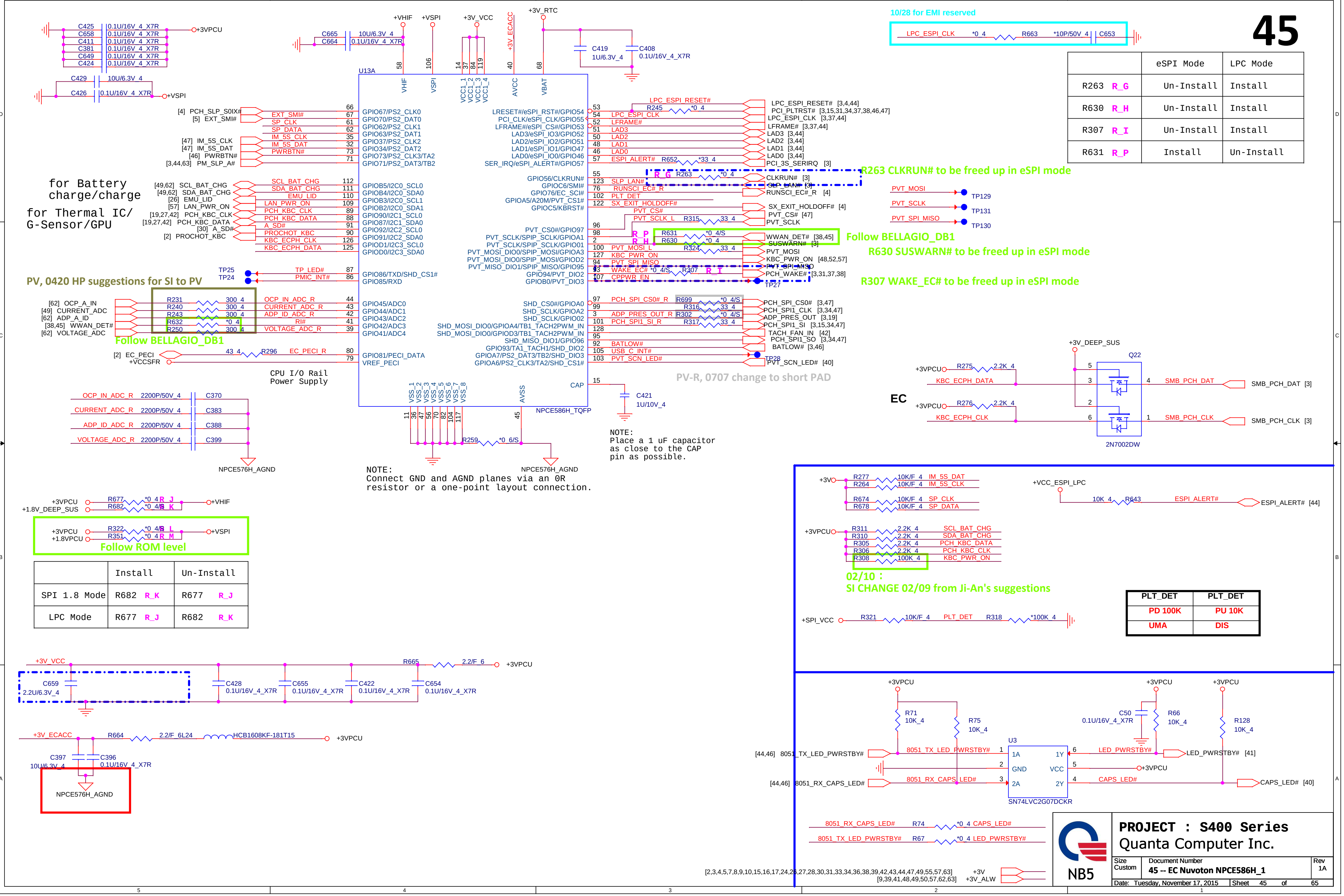
Size	Document Number	Rev
C	43 -- HDD/ EMI cap	1A

Date: Tuesday, November 17, 2015 Sheet 43 of 65



PROJECT : S400 Series		
Quanta Computer Inc.		
Size: Custom	Document Number: 44 -- EC & eSPI/UART debug conn	Rev: 1A
Date: Tuesday, November 17, 2015	Sheet 44 of 65	

NB5



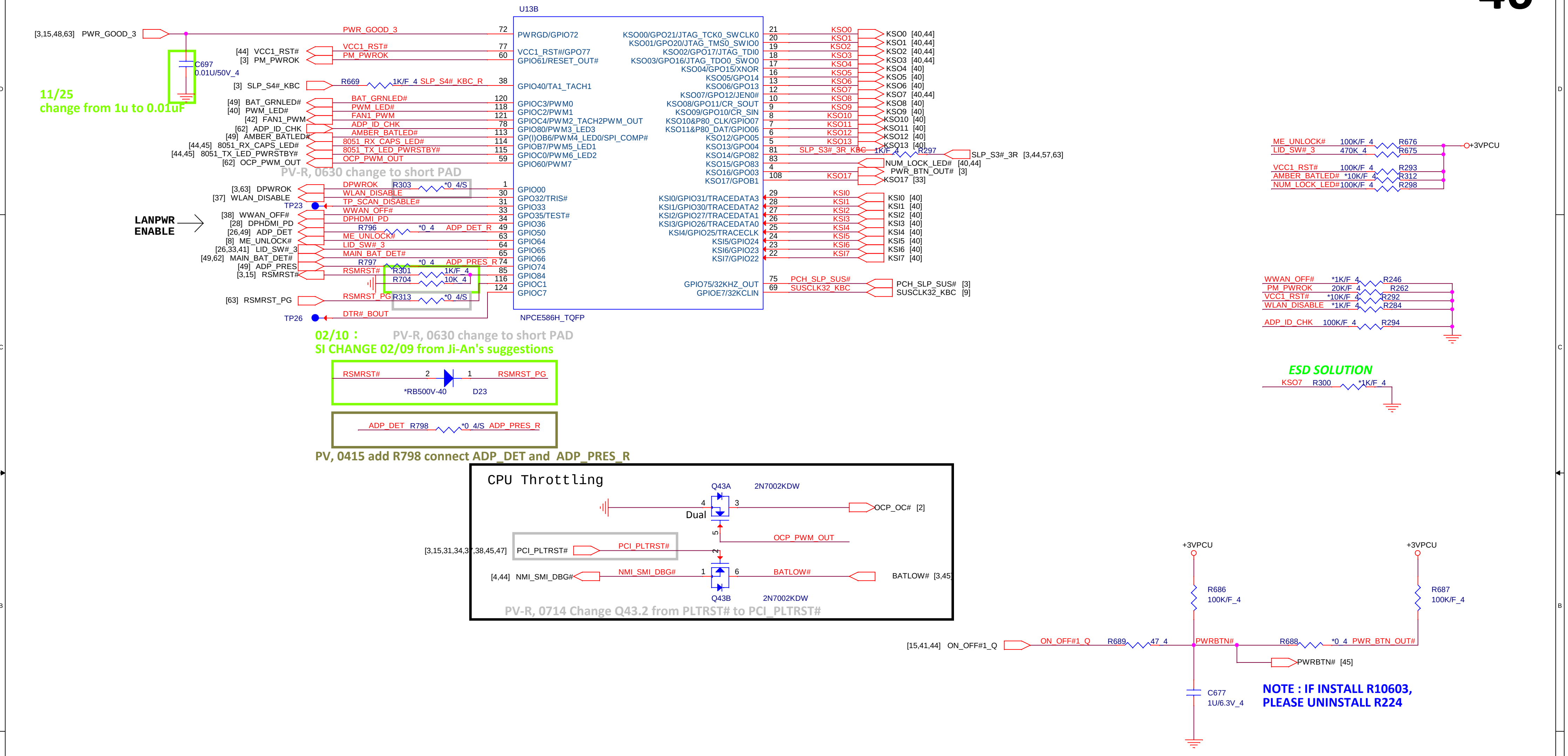
	eSPI Mode	LPC Mode
R263 R_G	Un-Install	Install
R630 R_H	Un-Install	Install
R307 R_I	Un-Install	Install
R631 R_P	Install	Un-Install

	Install	Un-Install
SPI 1.8 Mode	R682 R_K	R677 R_J
LPC Mode	R677 R_J	R682 R_K

PLT_DET	PLT_DET
PD 100K	PU 10K
UMA	DIS

PROJECT : S400 Series
Quanta Computer Inc.
NB5

Size	Document Number	Rev
Custom	45 -- EC Nuvoton NPCE586H_1	1A



PROJECT : S400 Series
Quanta Computer Inc.
NB5

Size	Document Number	Rev
Custom	46 -- EC Nuvoton NPCE586H_2	1A

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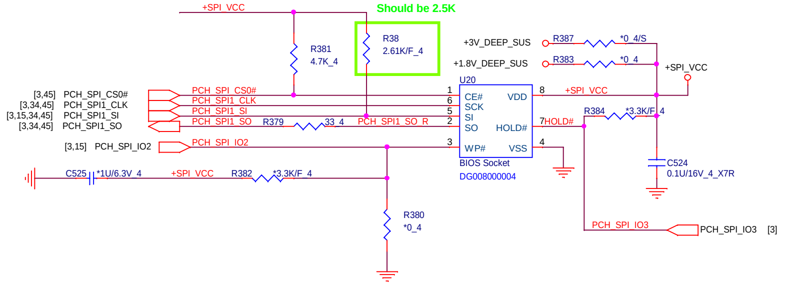
SPI ROM

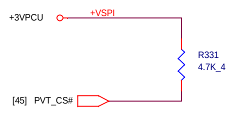
Vender	Size	P/N
Winbond	8MB	AKE3EFPKN01
Winbond	16MB	AKE3DZN0N01 SI : 02/02
Socket		DFHS08FS046

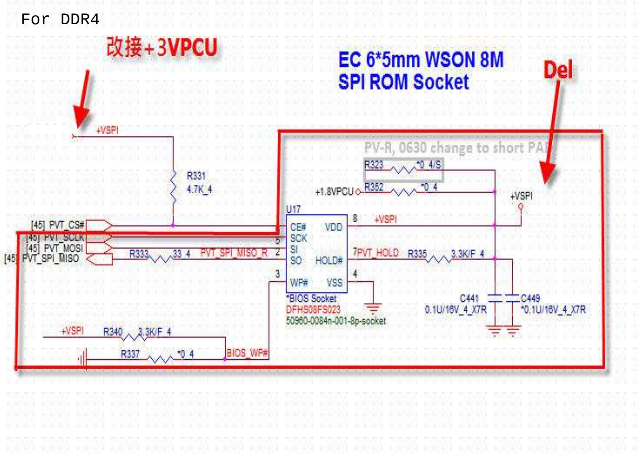
PCH SPI ROM(CLG)

PCH 6*5mm WSON 16M SPI ROM Socket



EC 6*5mm WSON 8M SPI ROM Socket





Touch pad

12/17 for EMI reserved

10/31 for EMI reserved

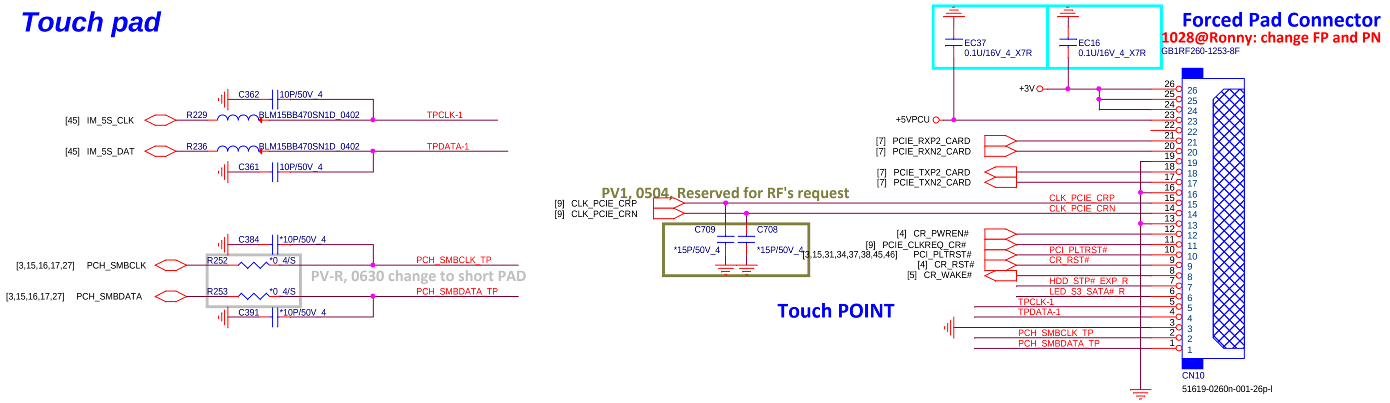
Forced Pad Connector

1028@Ronny: change FP and PN

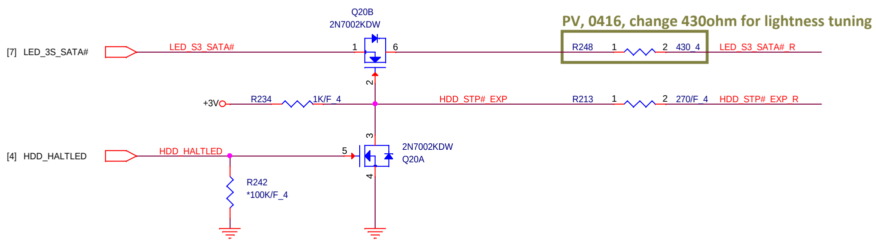
PV1, 0504, Reserved for RF's request

PV-R, 0630 change to short PAD

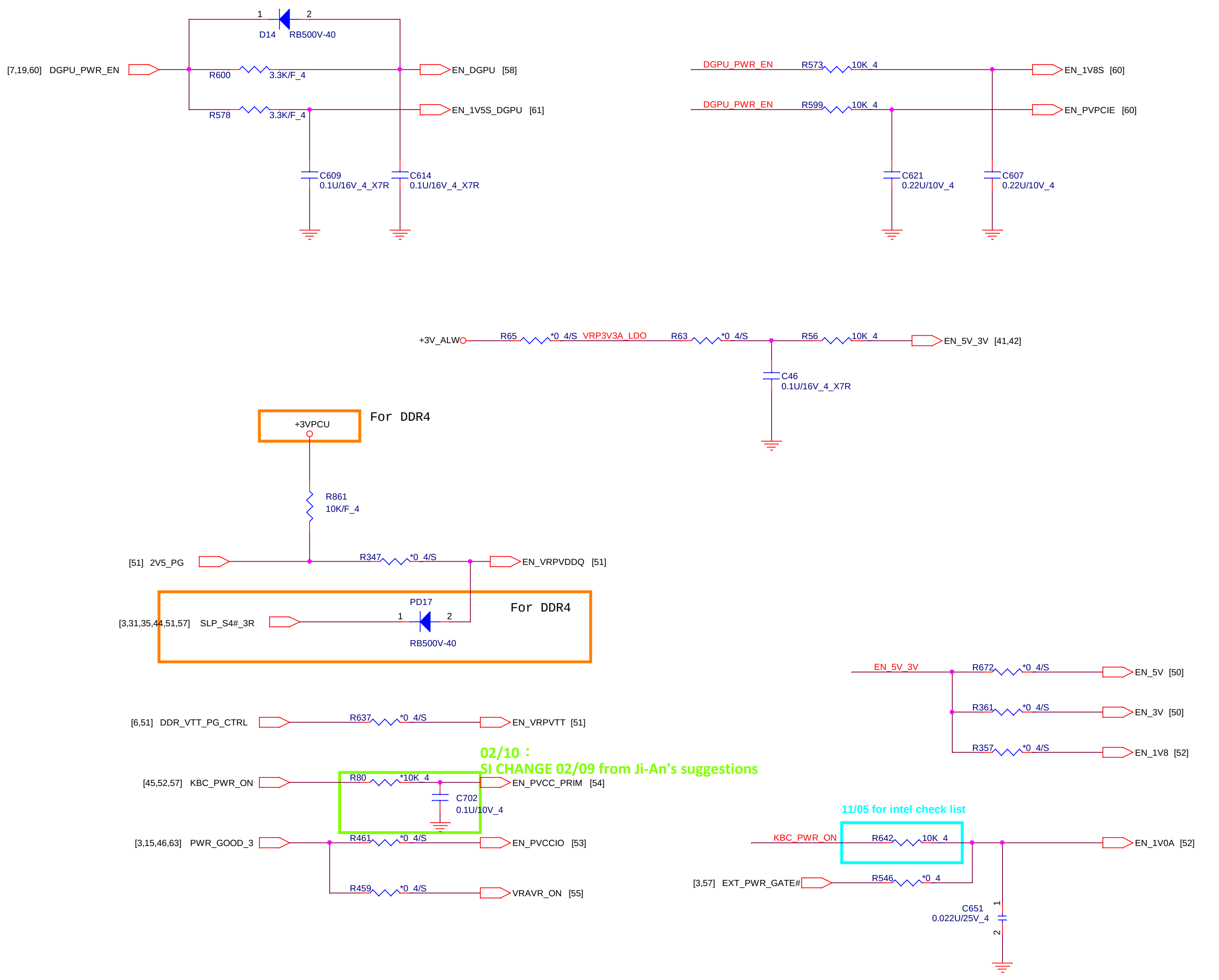
Touch POINT



PV, 0416, change 430ohm for lightness tuning



POWER TO EE NET NAME CONNECTION



PROJECT : S400 Series
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	48 -- POWER ENABLE	1A

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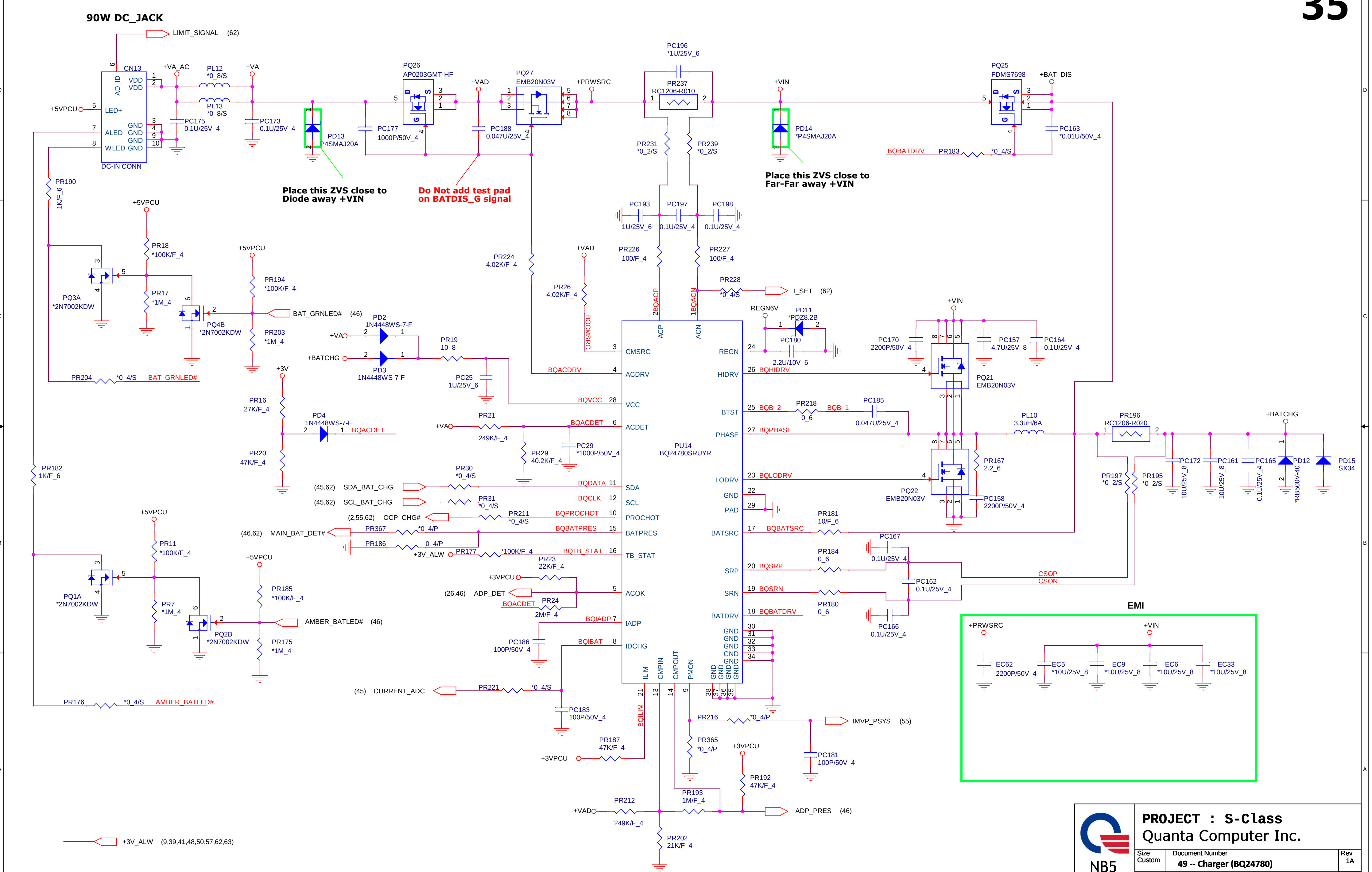
35



PROJECT : S-Class

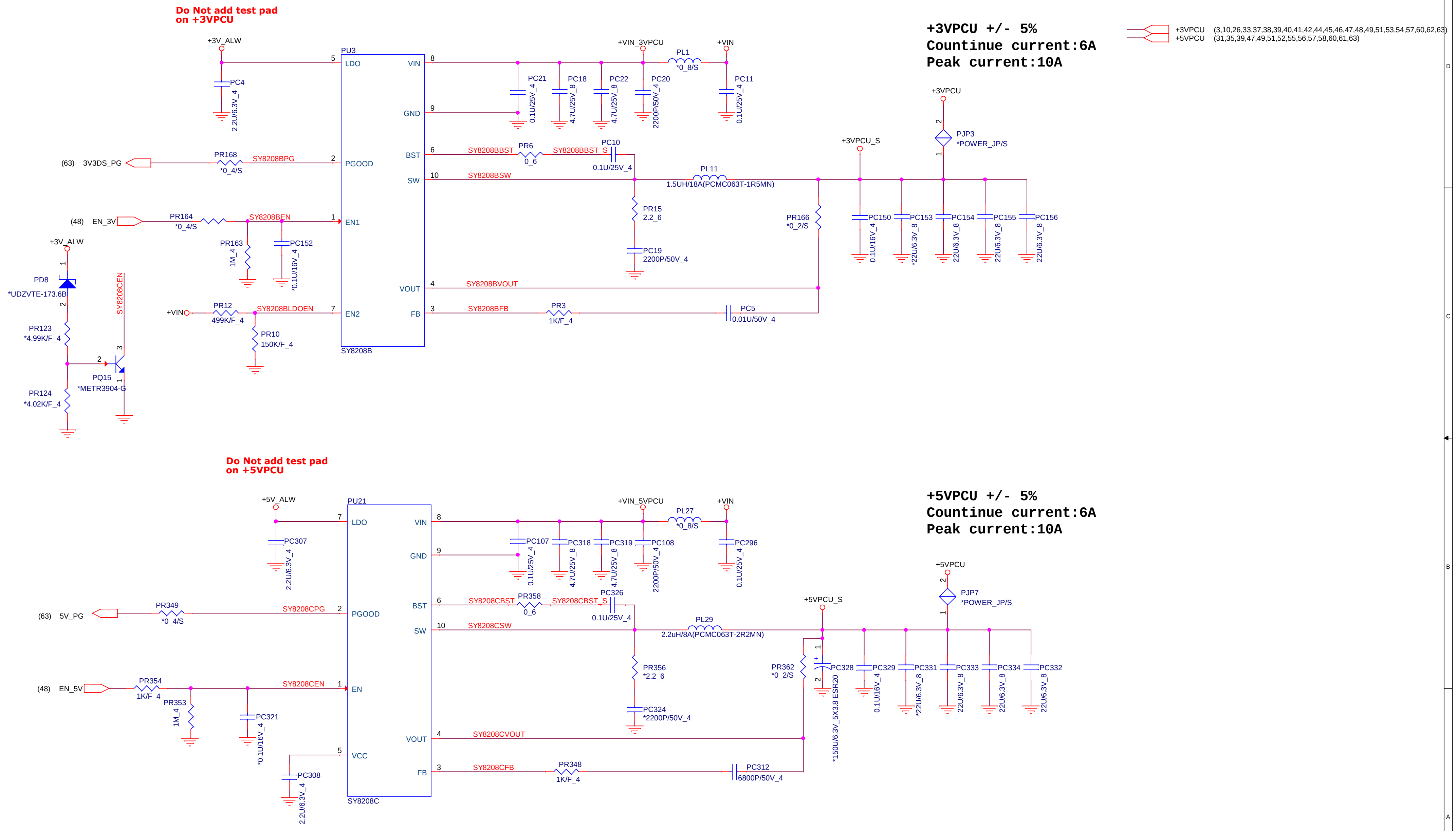
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	49 -- Charger (BQ24780)	1A

Date: Monday, November 30, 2015 | Sheet 49 of 65

DC/DC +3VS5/+5VS5

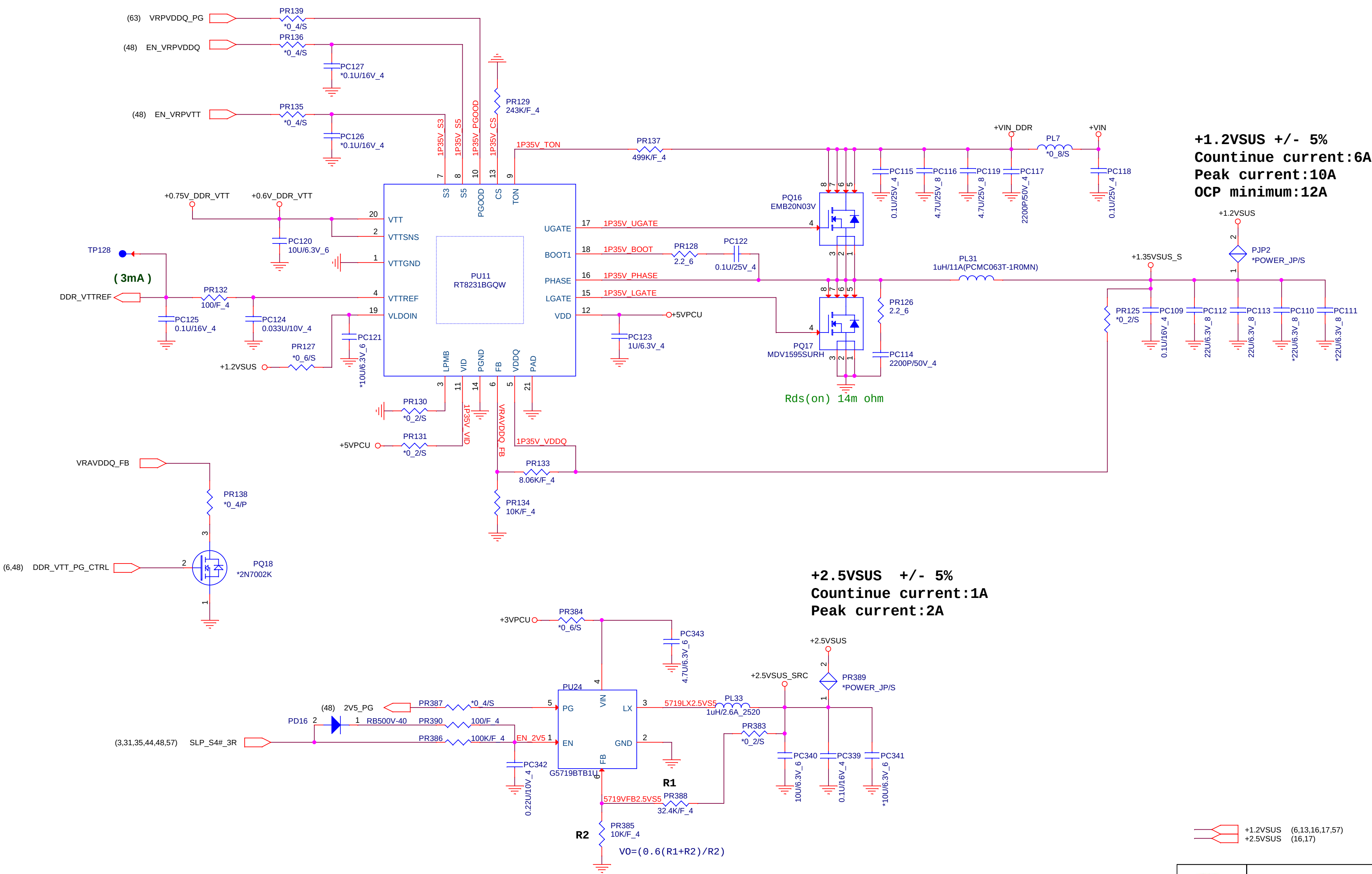


PROJECT : S-Class
Quanta Computer Inc.

NB5

Size	Document Number	Rev
	50 -- 3/5VS5 (SY8208B/SY8208C)	1A

Date: Monday, November 30, 2015 Sheet 50 of 65



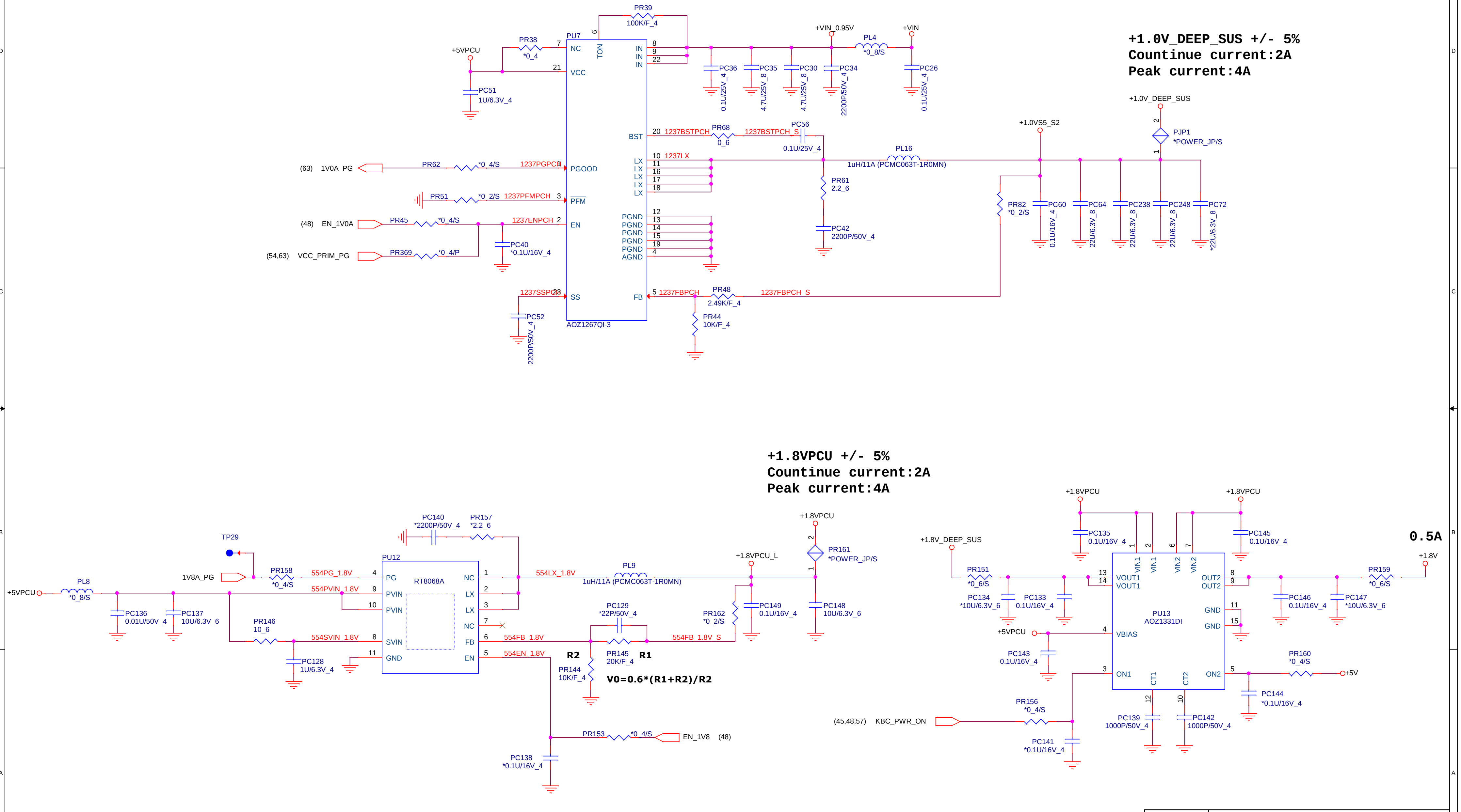
PROJECT : S-Class

Quanta Computer Inc.

NB5

Size	Document Number	Rev
	51 -- DDR4 (RT8231B)	1A

Date: Monday, November 30, 2015 Sheet 51 of 65



+VIN (26,39,43,44,49,50,51,53,54,55,56,57,59,61)
+3VPCU (3,10,26,33,37,38,39,40,41,42,44,45,46,47,48,49,50,51,53,54,57,60,62,63)
+5VPCU (31,35,39,47,49,50,51,55,56,57,58,60,61,63)

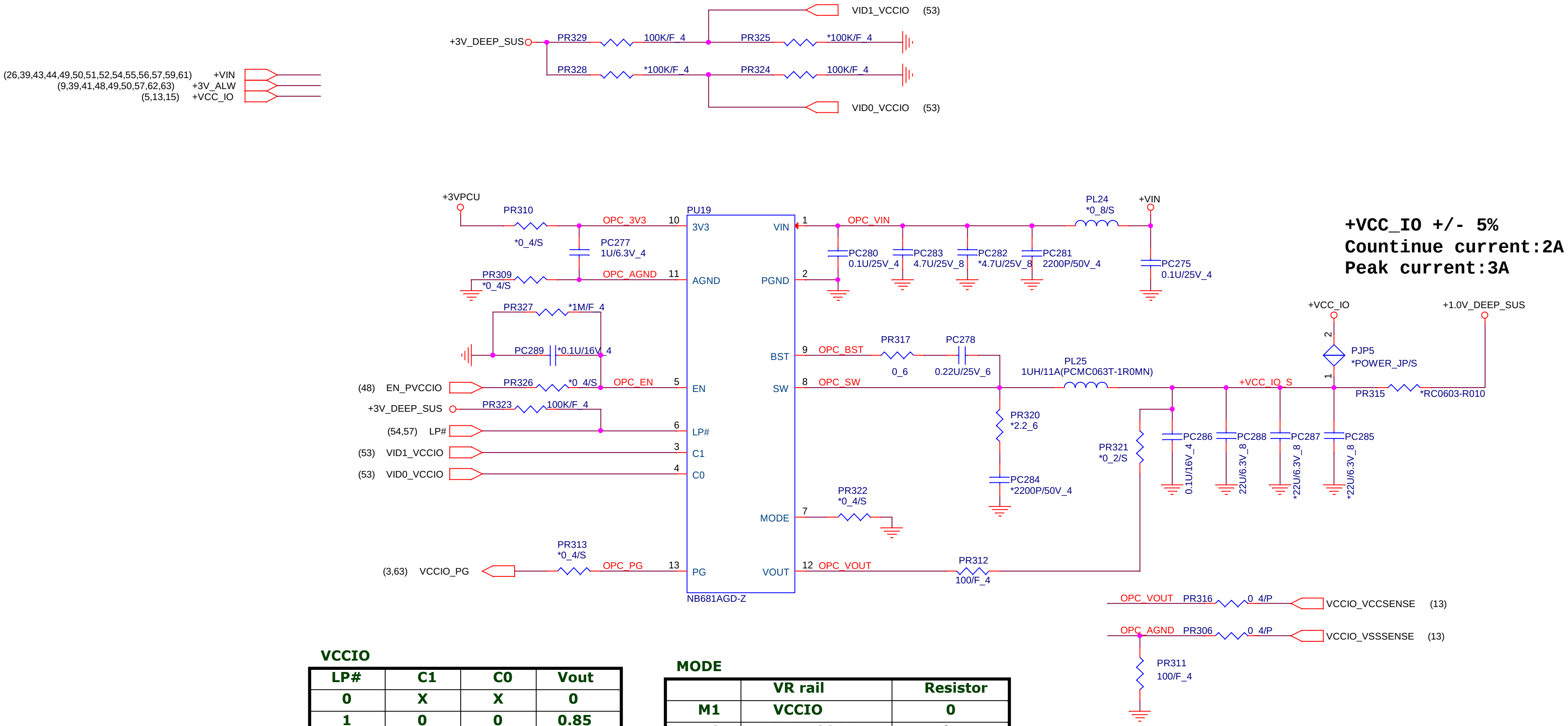
NB5

PROJECT : S-Class

Quanta Computer Inc.

Size	Document Number	Rev
	52 -- +1.0VS5/1.8VS5	1A

Date: Friday, December 04, 2015 Sheet 52 of 65



VCCIO

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

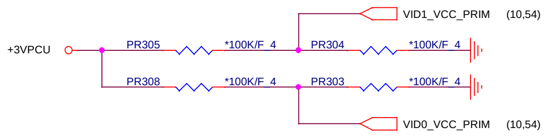
NB5

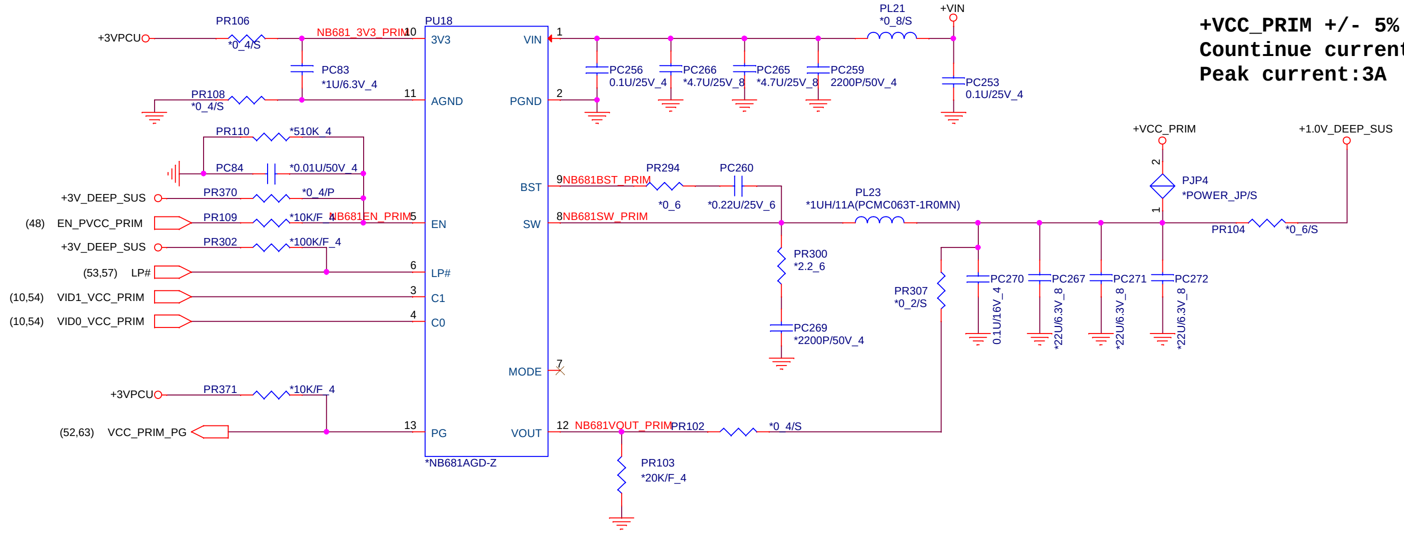
PROJECT : S-Class

Quanta Computer Inc.

Size	Document Number	Rev
	53 -- +VCC_IO (NB681)	1A

Date: Monday, November 30, 2015 Sheet 53 of 65





+VCC_PRIM +/- 5%
Countinue current:2A
Peak current:3A

VCC_PRIM

LP#	C1	C0	Vout
0	X	X	0.7
1	0	0	0.8
1	0	1	0.9
1	1	0	0.95
1	1	1	1.0

MODE

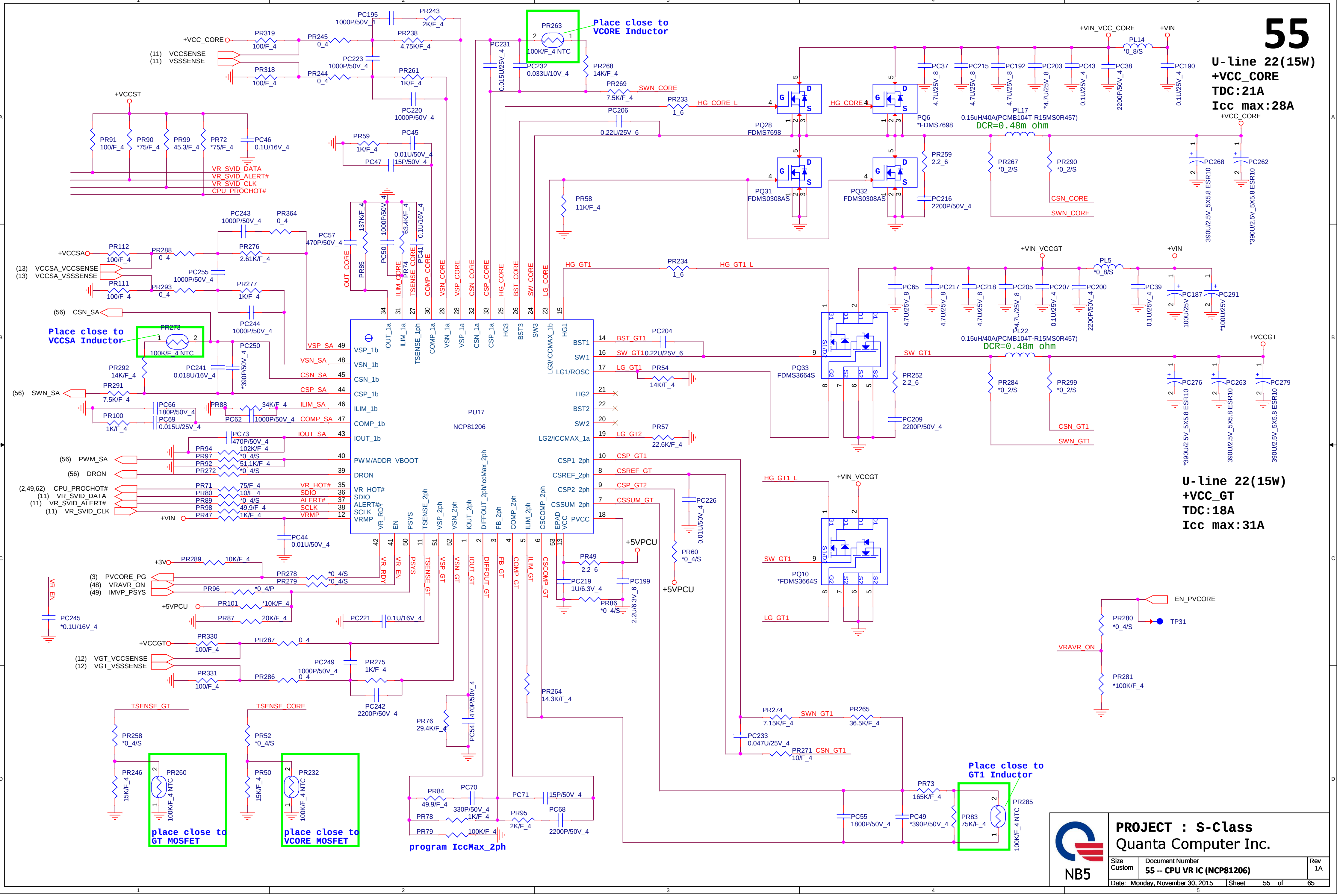
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

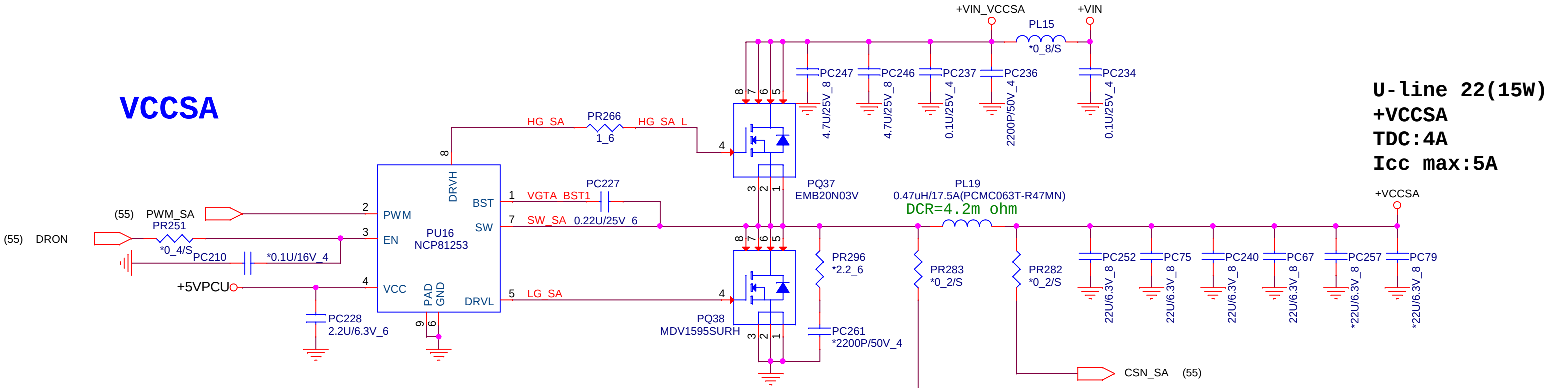
NB5

PROJECT : S-Class
Quanta Computer Inc.

Size	Document Number	Rev
	54 -- +VCC_PRIM (NB681)	1A

Date: Monday, November 30, 2015 Sheet 54 of 65


55
U-line 22(15W)
+VCC_CORE
TDC:21A
Icc max:28A
U-line 22(15W)
+VCC_GT
TDC:18A
Icc max:31A
Place close to
VCORE Inductor
Place close to
VCCSA Inductor
Place close to
GT1 Inductor
place close to
GT MOSFET
place close to
VCORE MOSFET
program IccMax_2ph
DCR=0.48m ohm
DCR=0.48m ohm
PU17
NCP81206
PROJECT : S-Class
Quanta Computer Inc.
NB5
Size Custom
Document Number
55 -- CPU VR IC (NCP81206)
Rev 1A
Date: Monday, November 30, 2015
Sheet 55 of 65



PROJECT : S-Class

Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	56 -- +VCCSA (NCP81253)	1A

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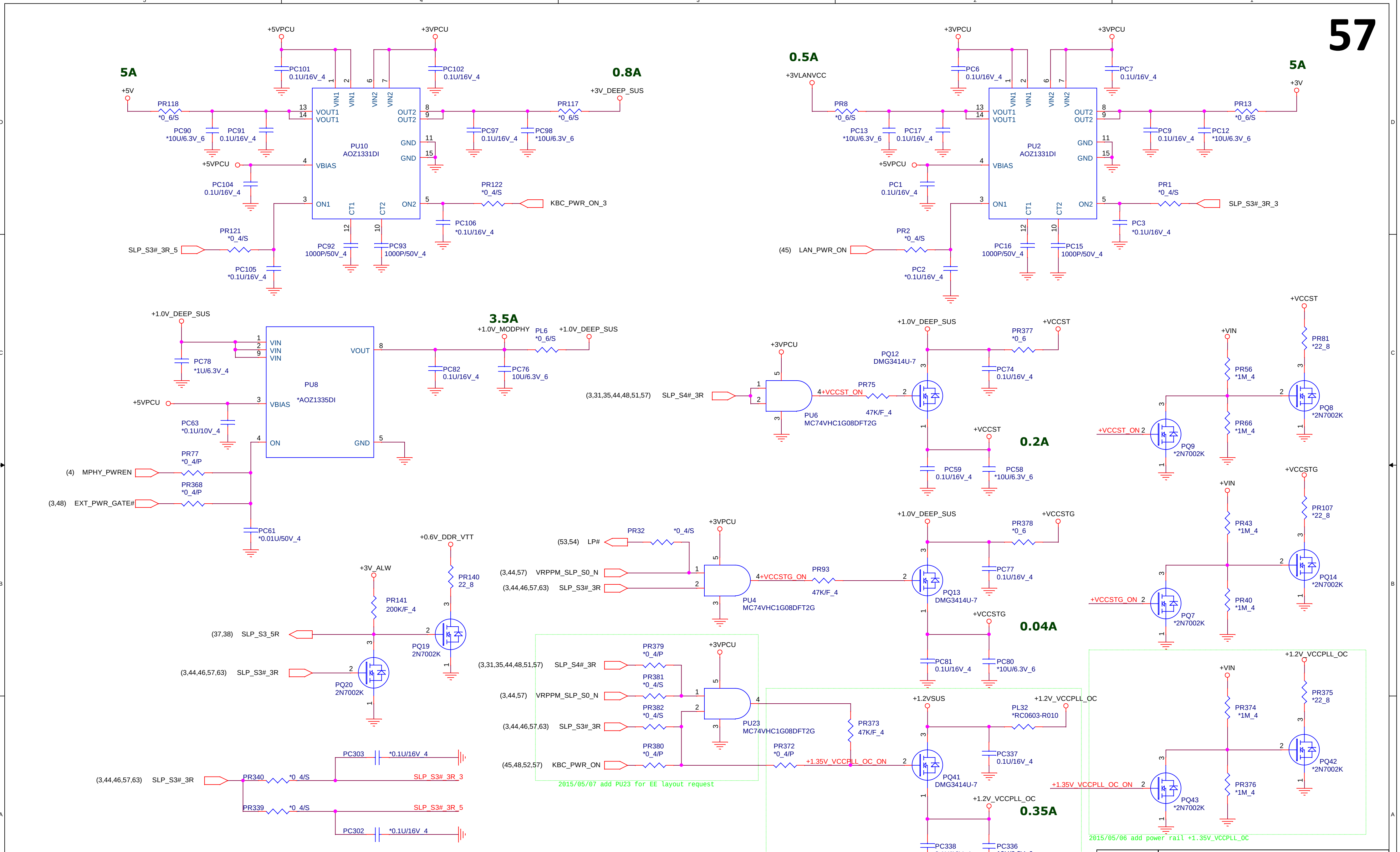


NB5

PROJECT : S-Class

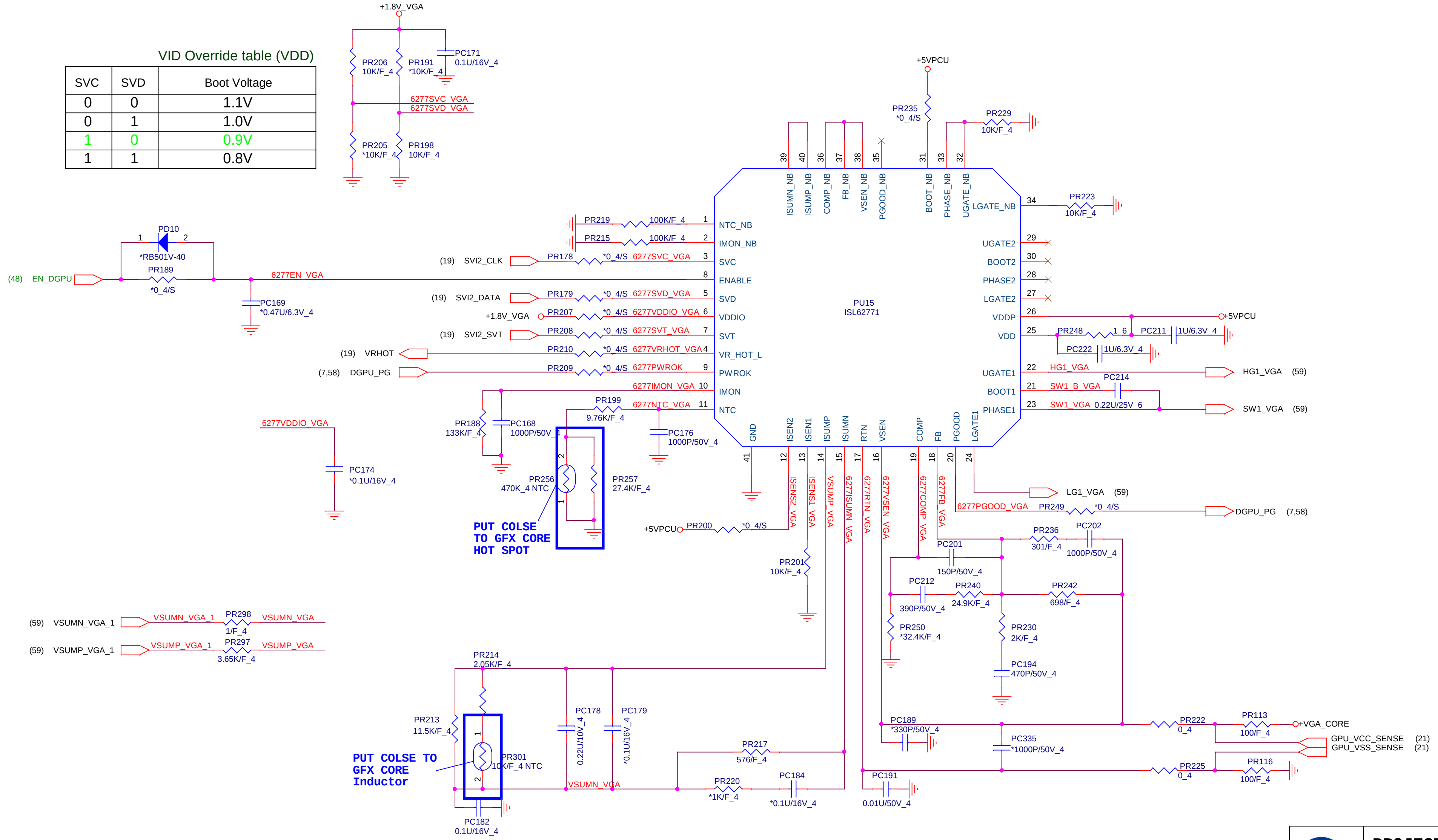
Quanta Computer Inc.

Size	Document Number	Rev
Custom	57 -- Load switch IC (APL3523A)	1A

Date: Monday, November 30, 2015 Sheet 57 of 65

VID Override table (VDD)

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



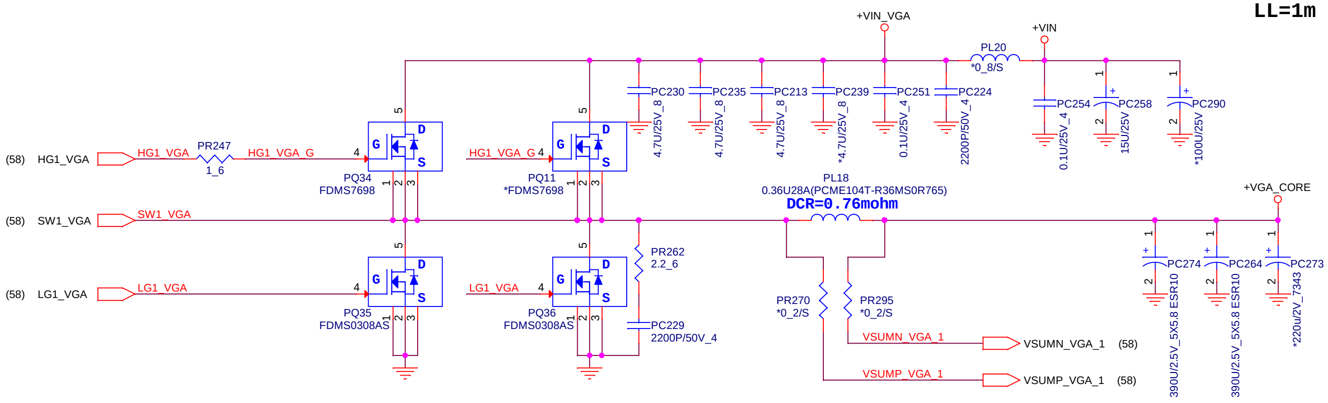
NB5

PROJECT : S-Class

Quanta Computer Inc.

Size	Document Number	Rev
Custom	58 -- VGA Core1 (ISL62771)	1A

VGACORE (Meso PRO (DDR3)_ 25W/38W(1ms))
Countinue current:28A
OCP_SPIKE=47A(1ms)
LL=1m V/A



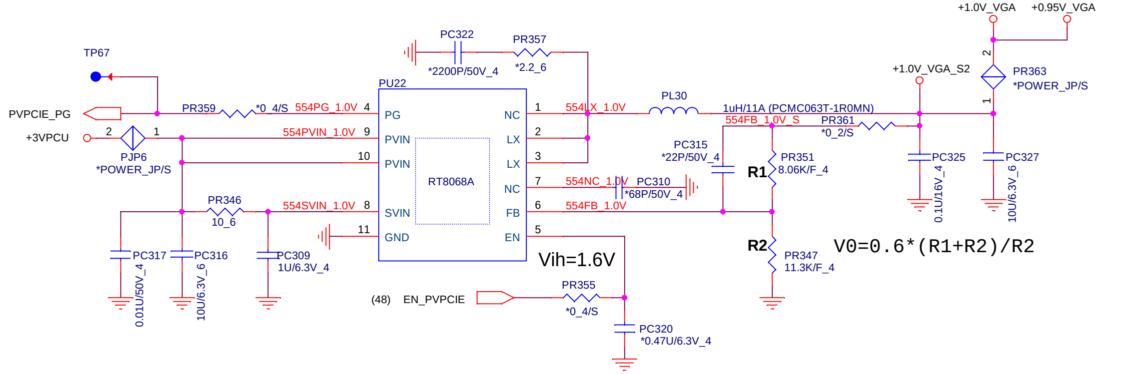
PROJECT : S-Class
Quanta Computer Inc.

NB5

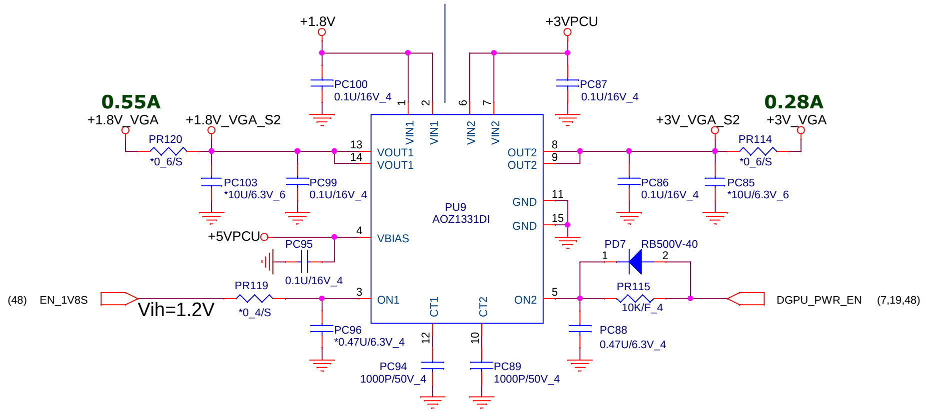
Size	Document Number	Rev
Custom	59 -- VGA Core2	1A

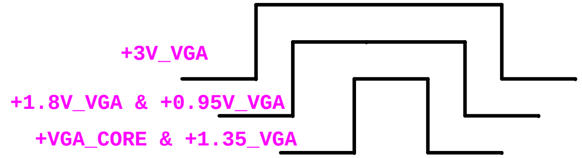
Date: Monday, November 30, 2015 Sheet 59 of 65

+1.0V_VGA +/- 3%
Countinue current:2A
Peak current:3A



PUT COLSE TO +1.8V power.



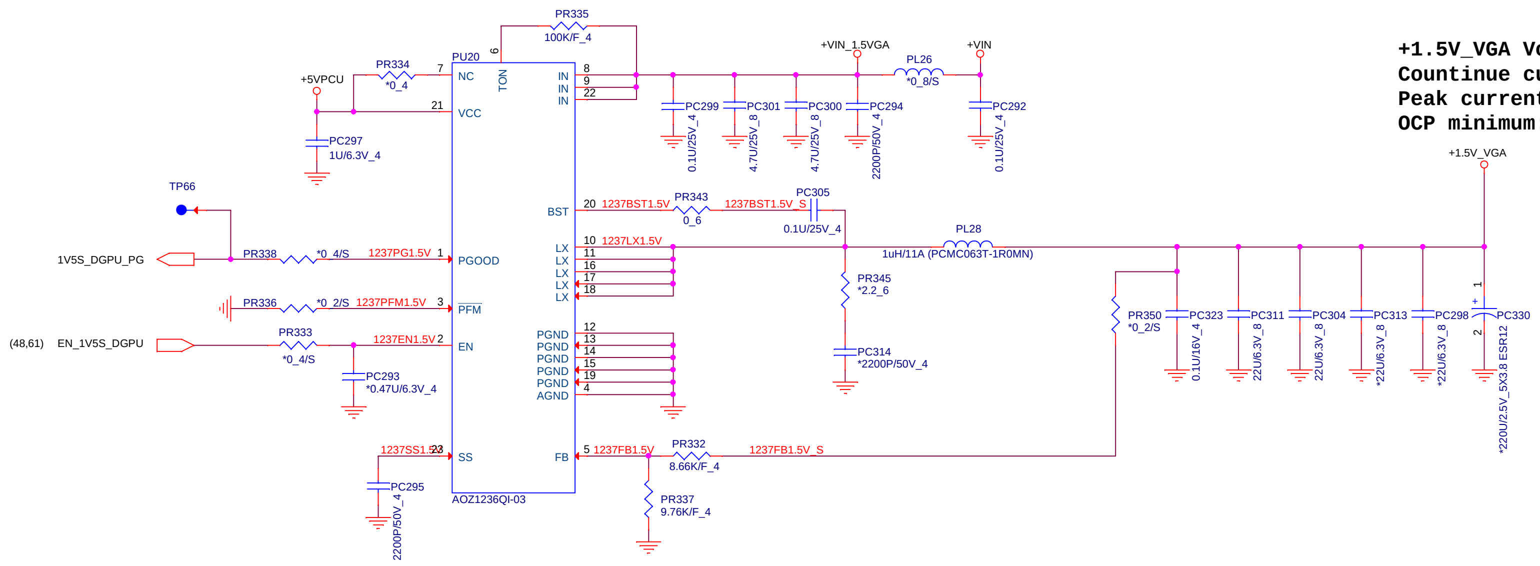


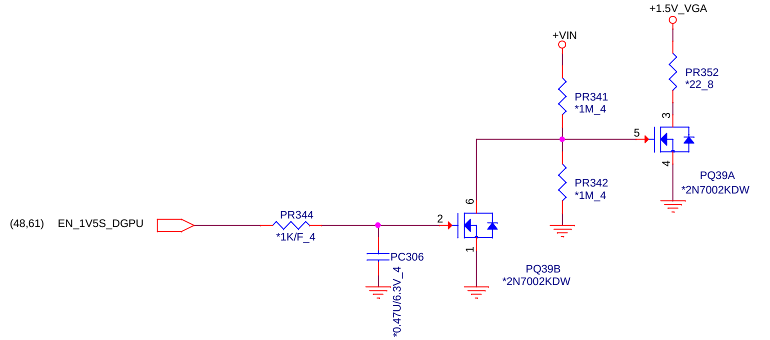
PROJECT : S-Class
Quanta Computer Inc.
NB5

Size	Document Number	Rev
Custom	60 -- +1.0V_VGA/1.8V_VGA/3V_VGA	1A

Date: Monday, November 30, 2015 Sheet 60 of 65

+1.5V_VGA Volt +/- 5%
Countinue current:4A
Peak current:5A
OCP minimum:12A





PROJECT : S-Class
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	61 -- +1.35V_GFX (AOZ1267)	1A

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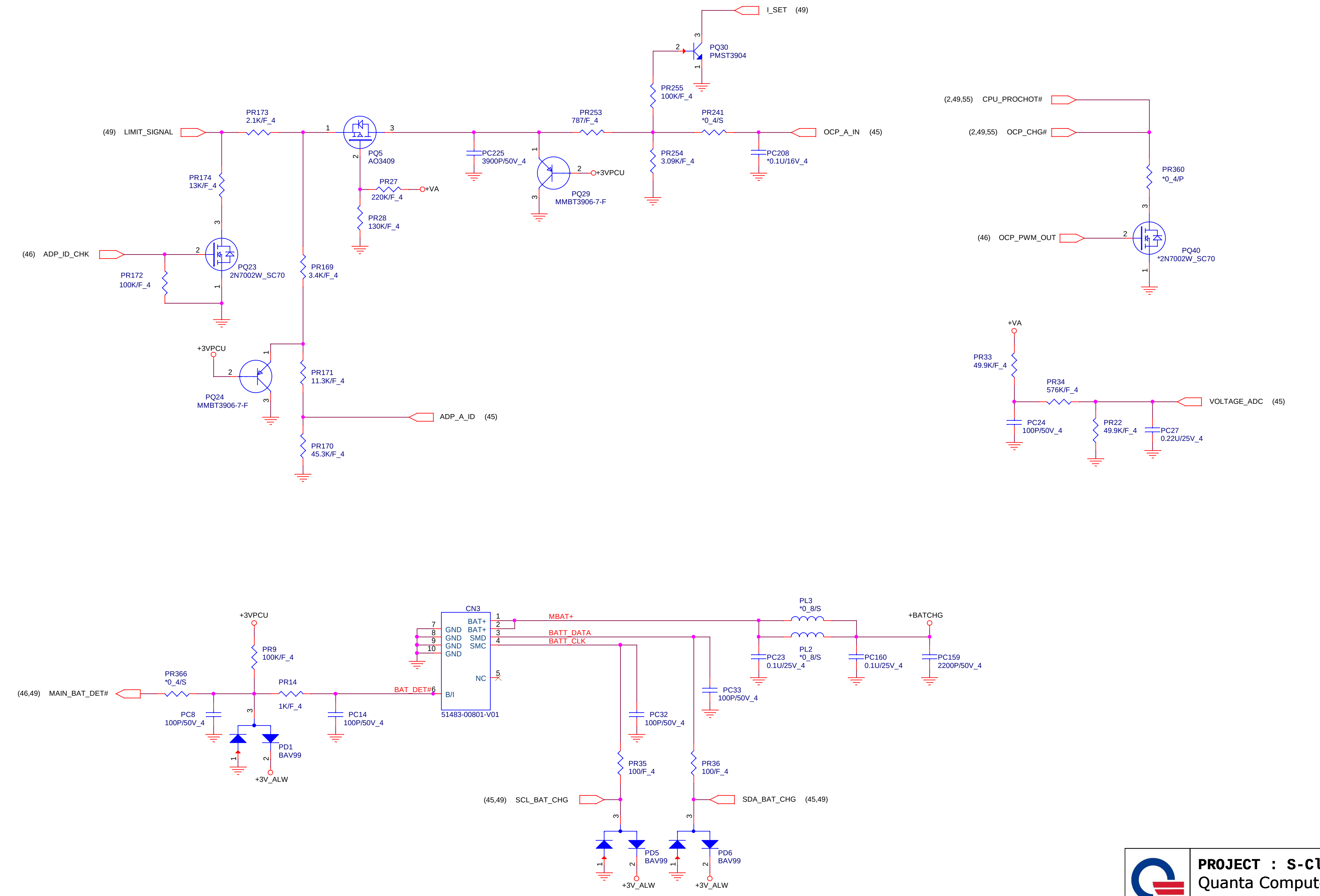
Adapter OCP



PROJECT : S-Class

Quanta Computer Inc.

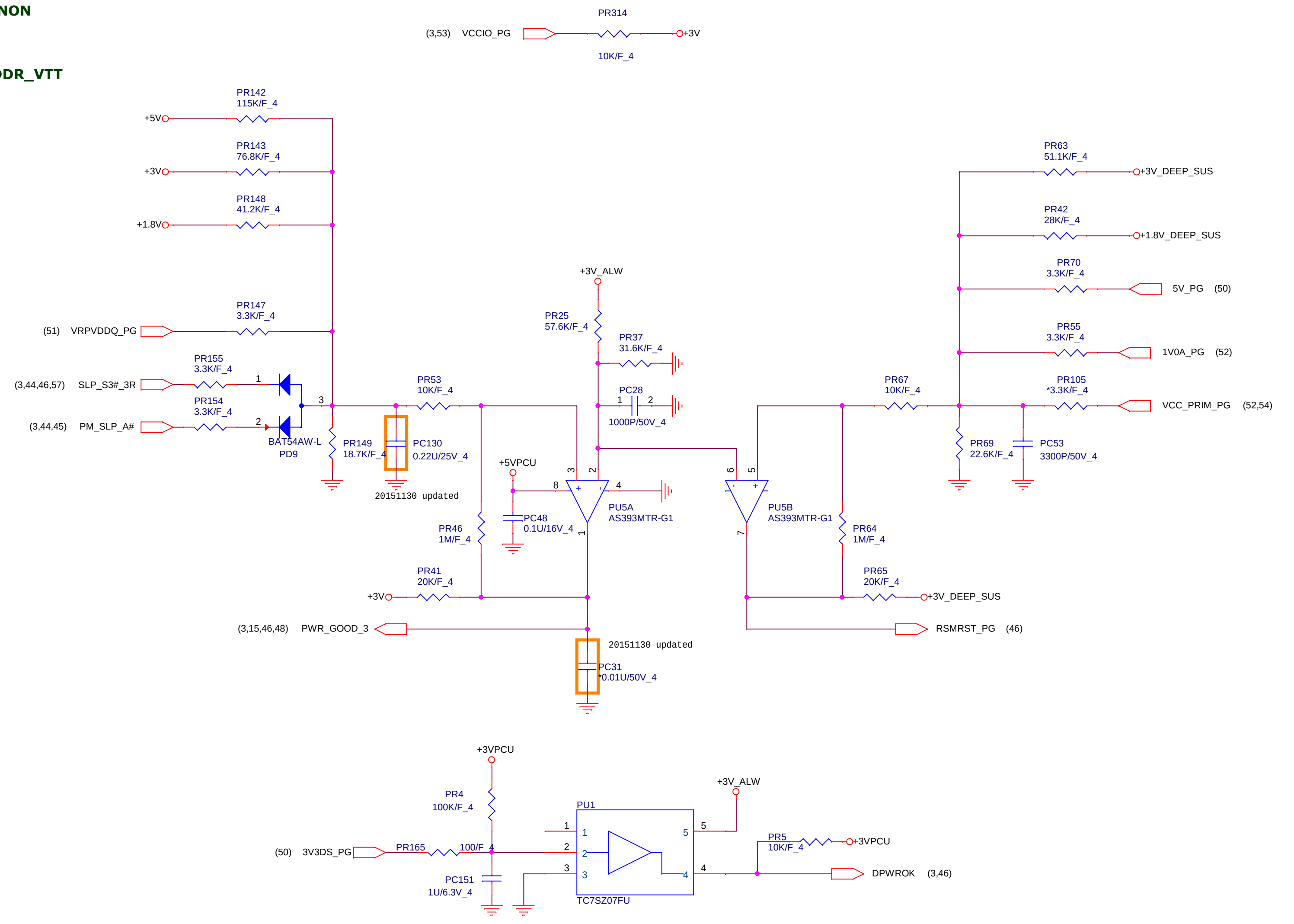
NB5

Size	Document Number	Rev
	62 -- CHARGER II	1A

Date: Monday, November 30, 2015 Sheet 62 of 65

POK CKT

PM_SLP_S4# = SUSON
PM_SLP_S3# = MAINON
+V5S = +5V
+V3S = +3V
+V0.75S =+0.75V_DDR_VTT



(2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,39,42,43,44,45,47,49,55,57) +3V
(8,29,30,31,39,40,42,43,52,57) +5V
(9,39,41,48,49,50,57,62) +3V_ALW

PROJECT : S-Class
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	63 -- PWROK	1A

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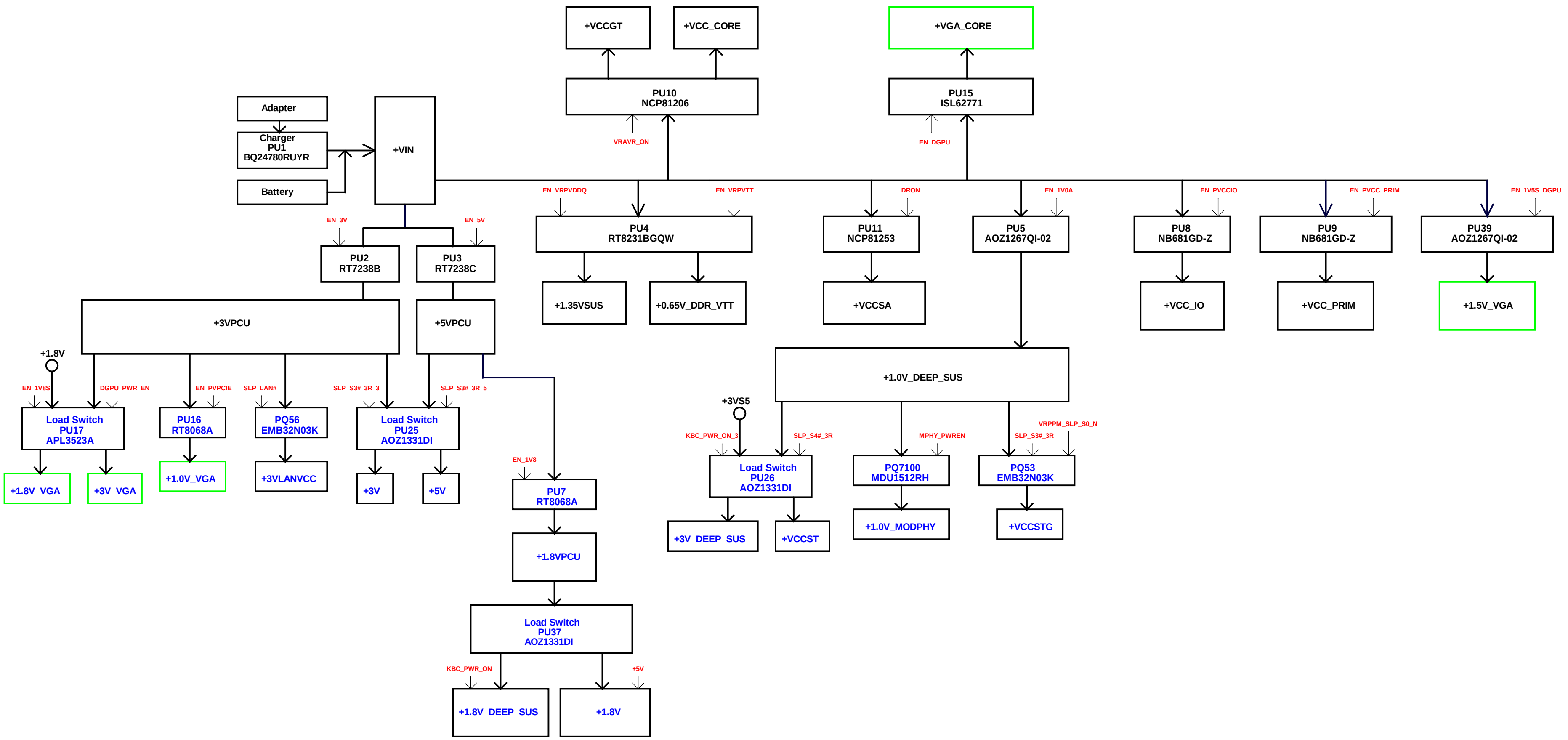
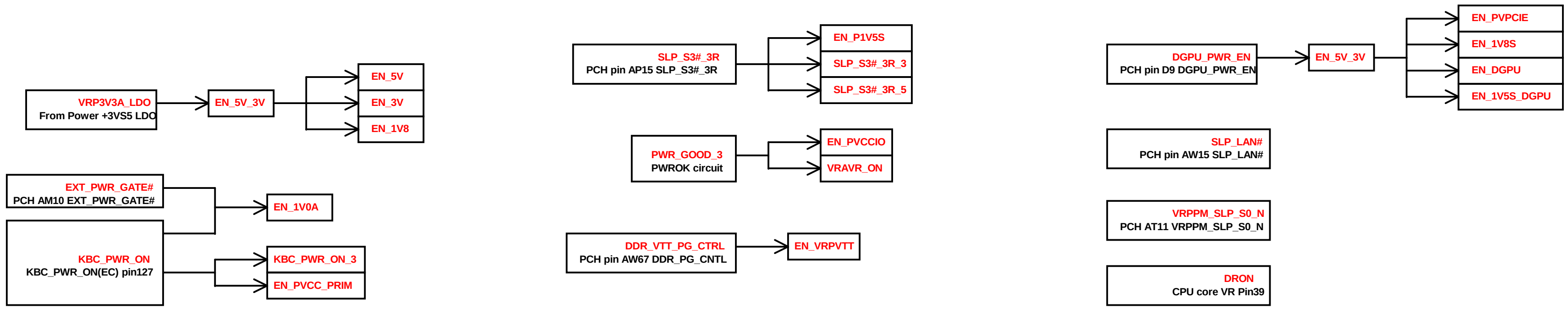
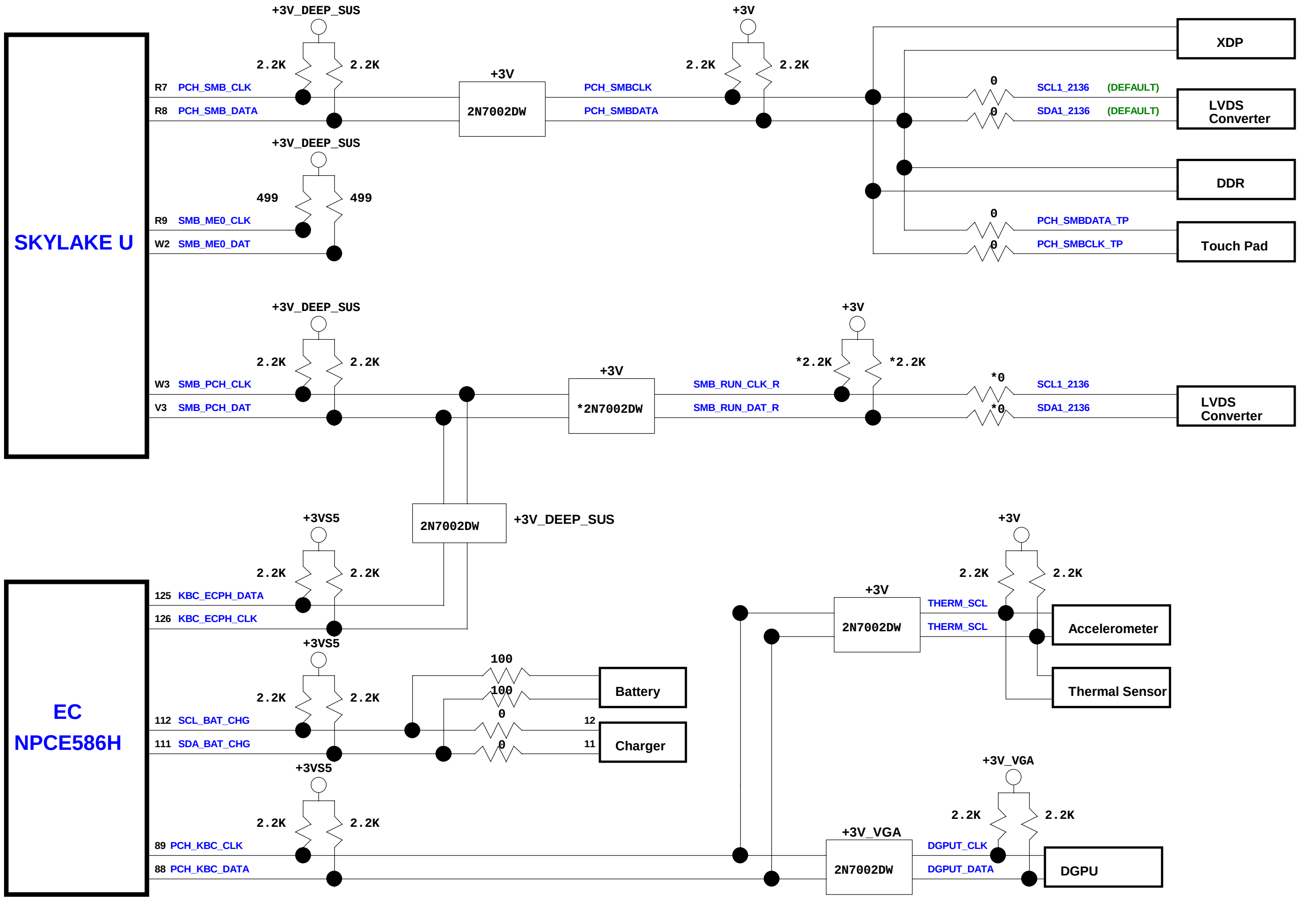
POWER BLOCK DIAGRAM



POWER ENABLE PIN



NB5	PROJECT : S-Class
	Quanta Computer Inc.
Size: Custom	Document Number: 64 -- Power Block Diagram	Rev: 1A
Date: Monday, November 30, 2015	Sheet 64 of 65



Example: *499/F_4 and *0_6/S
* means none-installed
499 means value
F means 1%
_4 means 0402 size
/S means short pad

Multiplexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Left side up)
USB3 #3 / SSIC #2	NC
USB3 #4	NC
PCIE1 / USB3 #5	dGPU
PCIE2 / USB3 #6	dGPU
PCIE3	dGPU
PCIE4	dGPU
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	HDD (SATA)
PCIE8 / SATA #1	ODD (SATA)
PCIE9	Cardreader (PCIE)
PCIE10	NC
PCIE11 / SATA #1*	NC
PCIE12 / SATA #2	SSD (SATA)

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB2 #2	USB2.0/USB3.0 Combo Jack(Left side up)
USB2 #3	WWAN
USB2 #4	USB2.0(Right side on USB Board)
USB2 #5	USB2.0(Right side on USB Board)
USB2 #6	Touch Screen
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	NC

NB5

PROJECT : S-Class
Quanta Computer Inc.

Size	Document Number	Rev
Custom	65 -- SMBus/Port Assignment	1A

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