LF14M
Schematics Document

M40

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

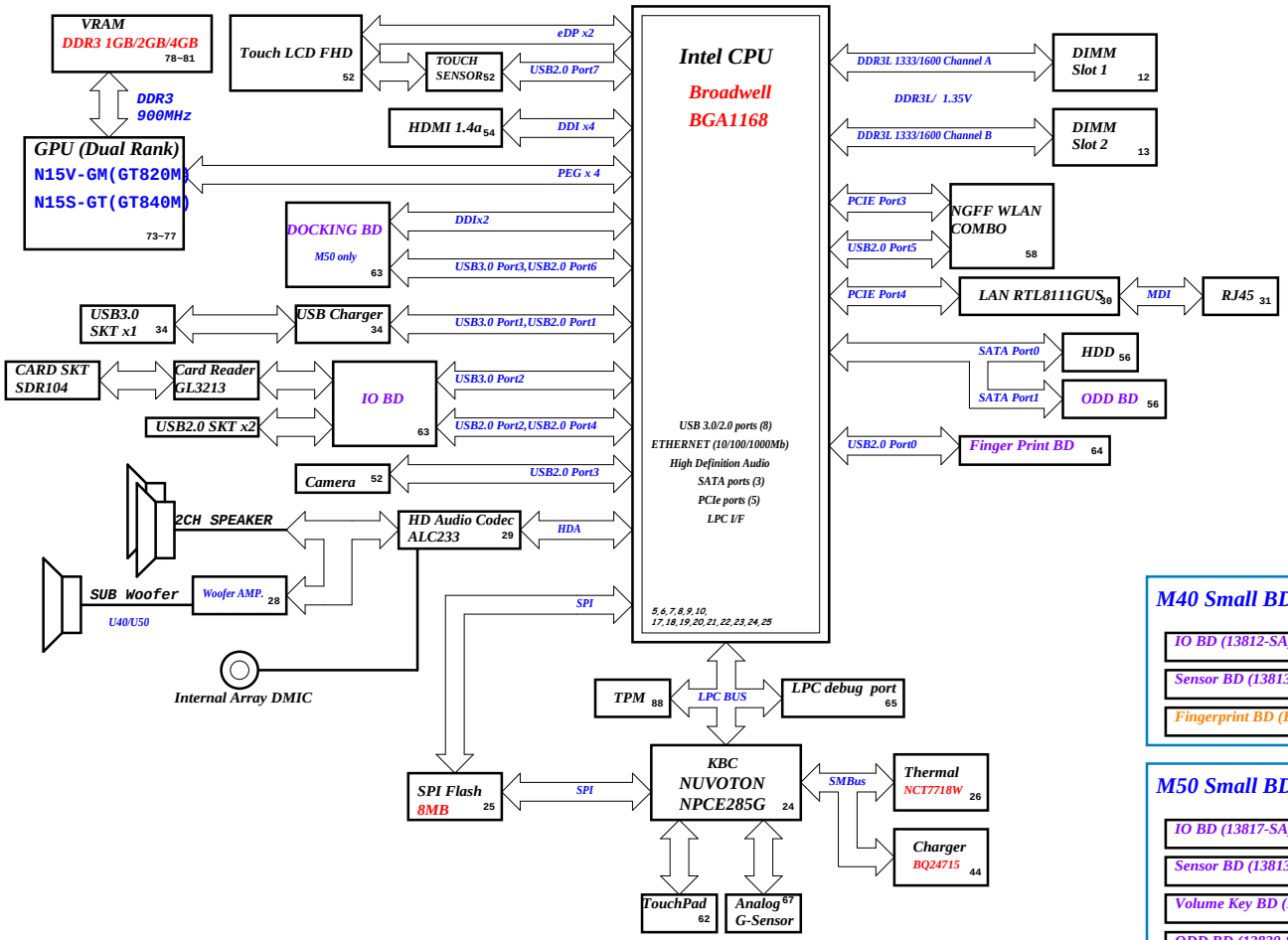
Title: **Cover Page**

Size	Document Number	Rev
A3	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 1 of 102

LF14M Board Block Diagram

Project code : 4PD00X010001
PCB P/N : 13281
Revision : SC



M40 Small BD & PCB P/N:

IO BD (13812-SA)	63
Sensor BD (13813-SA)	63
Fingerprint BD (Buy)	63

Mybo14 Small BD & PCB P/N:

IO BD (13812-SA)	63
Sensor BD (13813-SA)	63

M50 Small BD & PCB P/N:

IO BD (13817-SA)	63
Sensor BD (13813-SA)	63
Volume Key BD (13819-SA)	63
ODD BD (13820-SA)	63
DOCKING BD (13818-SA)	63
Fingerprint BD (Buy)	63

Mybo15 Small BD & PCB P/N:

IO BD (13814-SA)	63
Sensor BD (13813-SA)	63
Volume Key BD (13816-SA)	63
ODD BD (13820-SA)	63
Power BTN BD (13815-SA)	63

CHARGER BQ24715 44

INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC TPS51275 45

INPUTS	OUTPUTS
DCBATOUT	5V_Charger 3D3V_S5

CPU DC/DC TPS51624 46-47

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC SYS8208A 48

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8207 49

INPUTS	OUTPUTS
DCBATOUT	1D35V_S3

SYSTEM DC/DC

INPUTS	OUTPUTS

SYSTEM DC/DC TLV70215 51

INPUTS	OUTPUTS
DCBATOUT	1D5V_S0

RT8812A 82

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

Switches 83

INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D35V_S0	1D35V_VGA_S0
1D05V_VTT	1D05V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

<Core Design>

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Title: Block Diagram

Size: A2 | Document Number: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet 2 of 102

SSID = CPU

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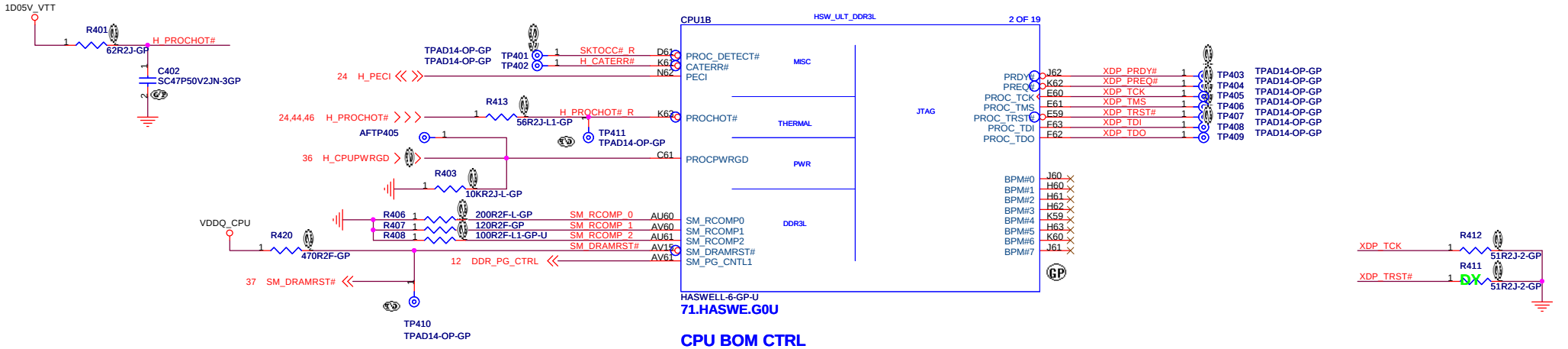
Title: ***CPU (Reserved)***

Size	Document Number	Rev
A3	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 3 of 102

SSID = CPU



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<Core Design>

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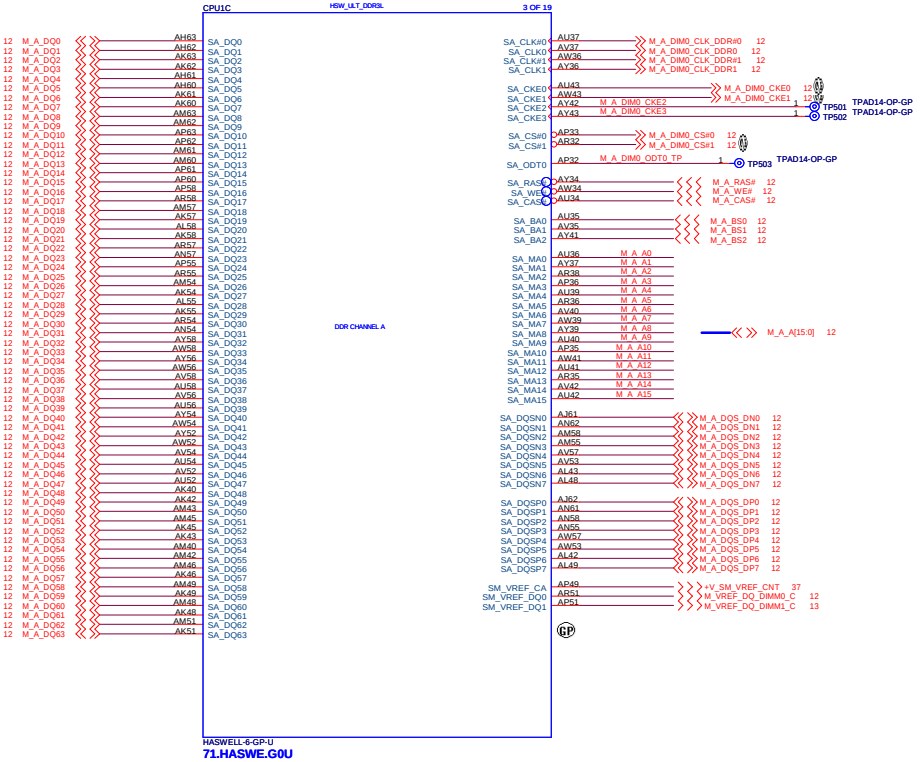
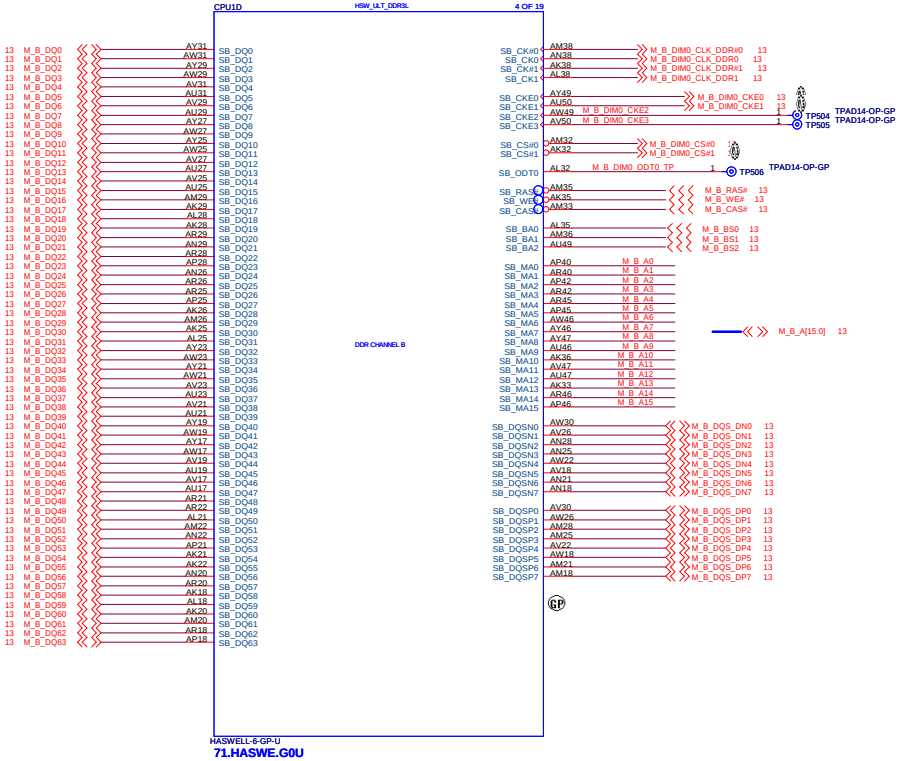
Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
A3	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 4 of 102

SSID = CPU





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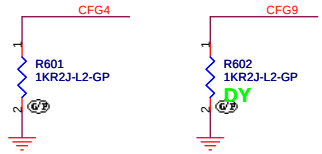
Title: CPU (DDR)

Size	Document Number	Rev
A2	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 5 of 102

SSID = CPU

eDP Enable	
CFG4	1:Disable 0:Enable

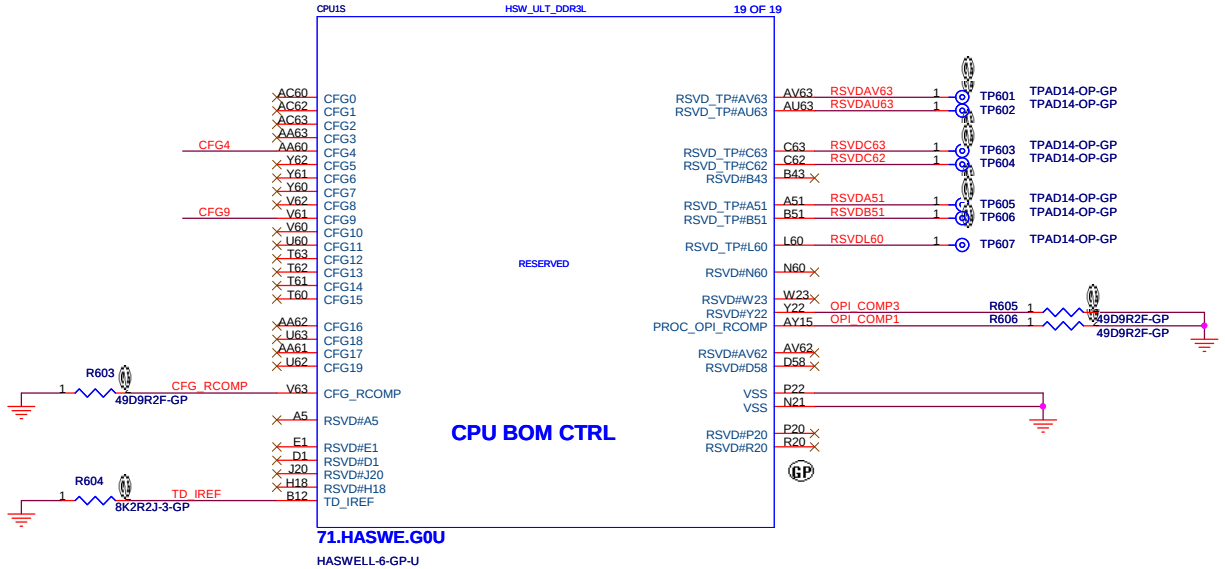


Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[3:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • PCI Express* Static x16 Lane Numbering Reversal. — — • • **CFG[4]: eDP enable** — 1 = Disabled — 0 = Enabled • **[19:5]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	
		continued...

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected



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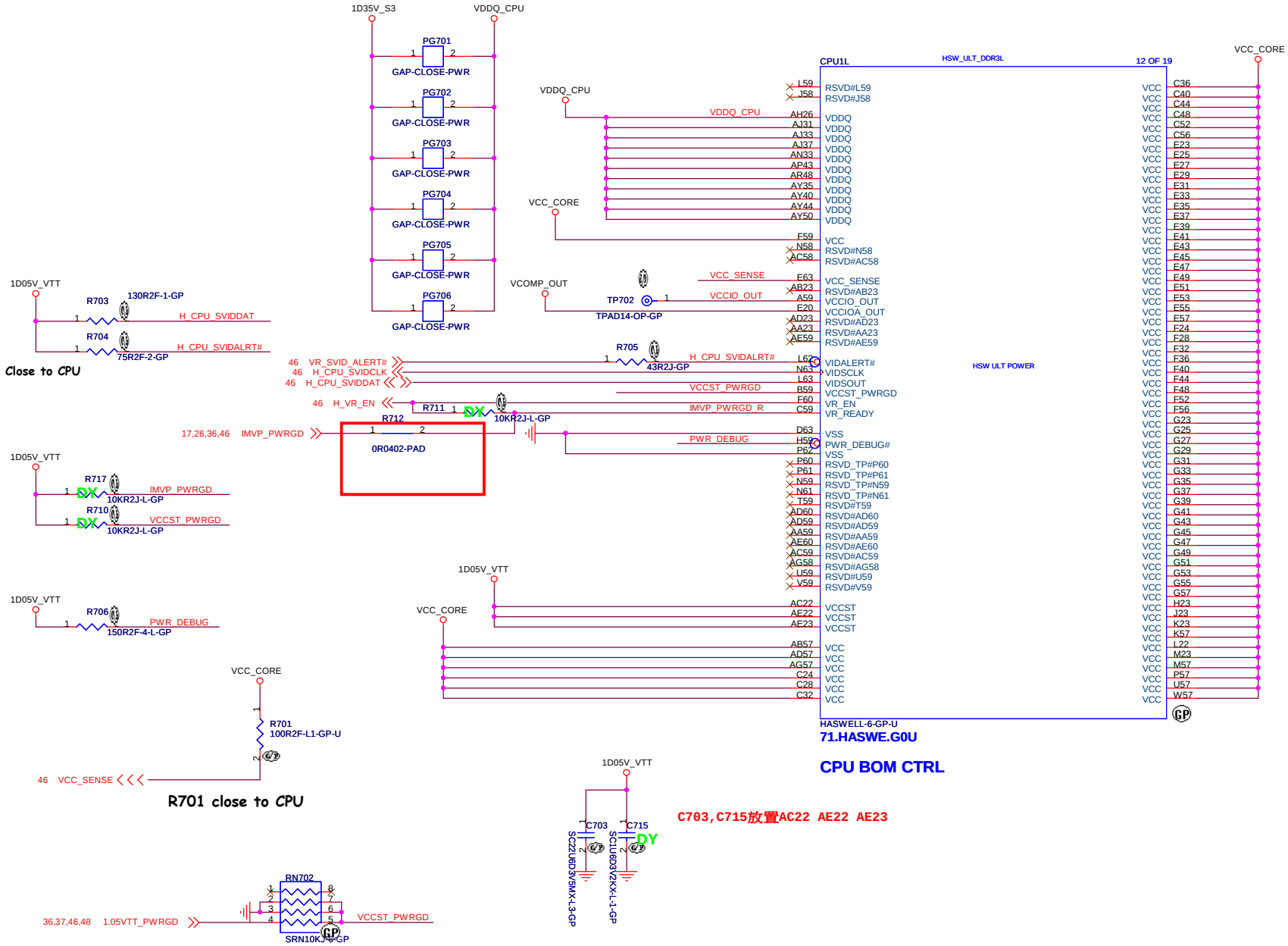
Title: CPU (CFG)		
Size: Custom	Document Number: LF14M	Rev: -1
Date: Wednesday, February 26, 2014	Sheet 6 of 102	

SSID = CPU



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Title	CPU (VCC_CORE)	
Size A3	Document Number LF14M	Rev -1
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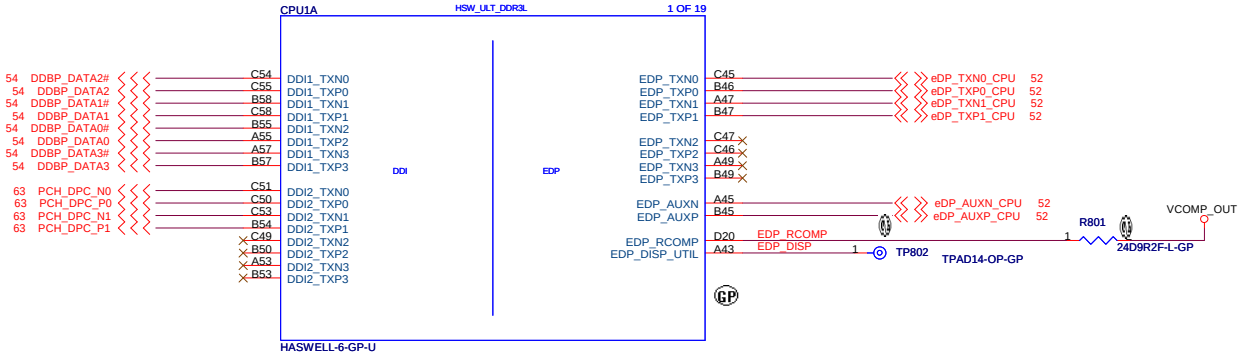
SSID = CPU

HDMI

DP to DOCKING



CPU BOM CTRL

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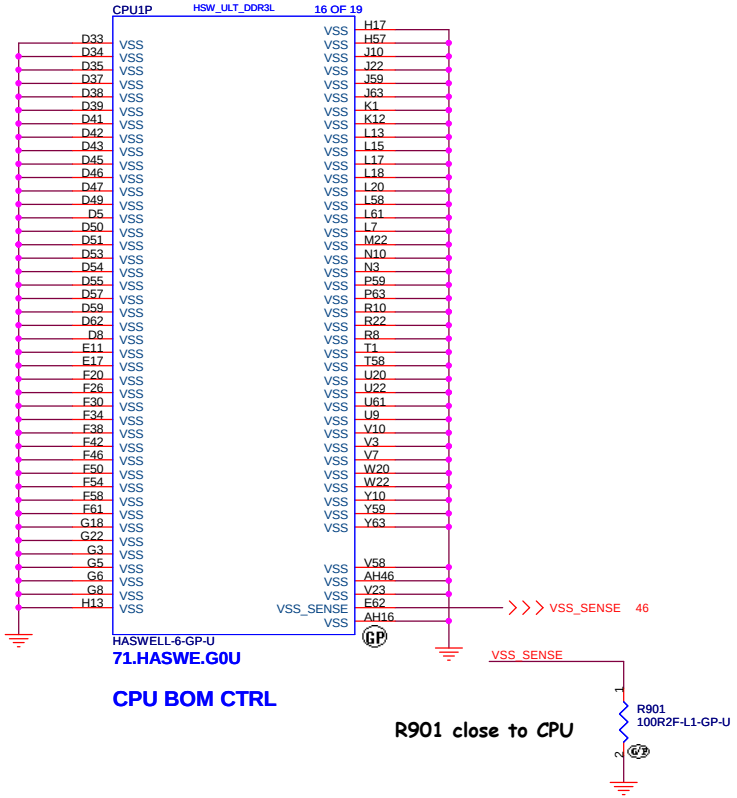
Title: ***CPU (DDI/EDP)***

Size	Document Number	Rev
Custom	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 8 of 102

SSID = CPU



CPU BOM CTRL

R901 close to CPU

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Title: **CPU (VSS)**

Size: A3 | Document Number: **LF14M** | Rev: **-1**

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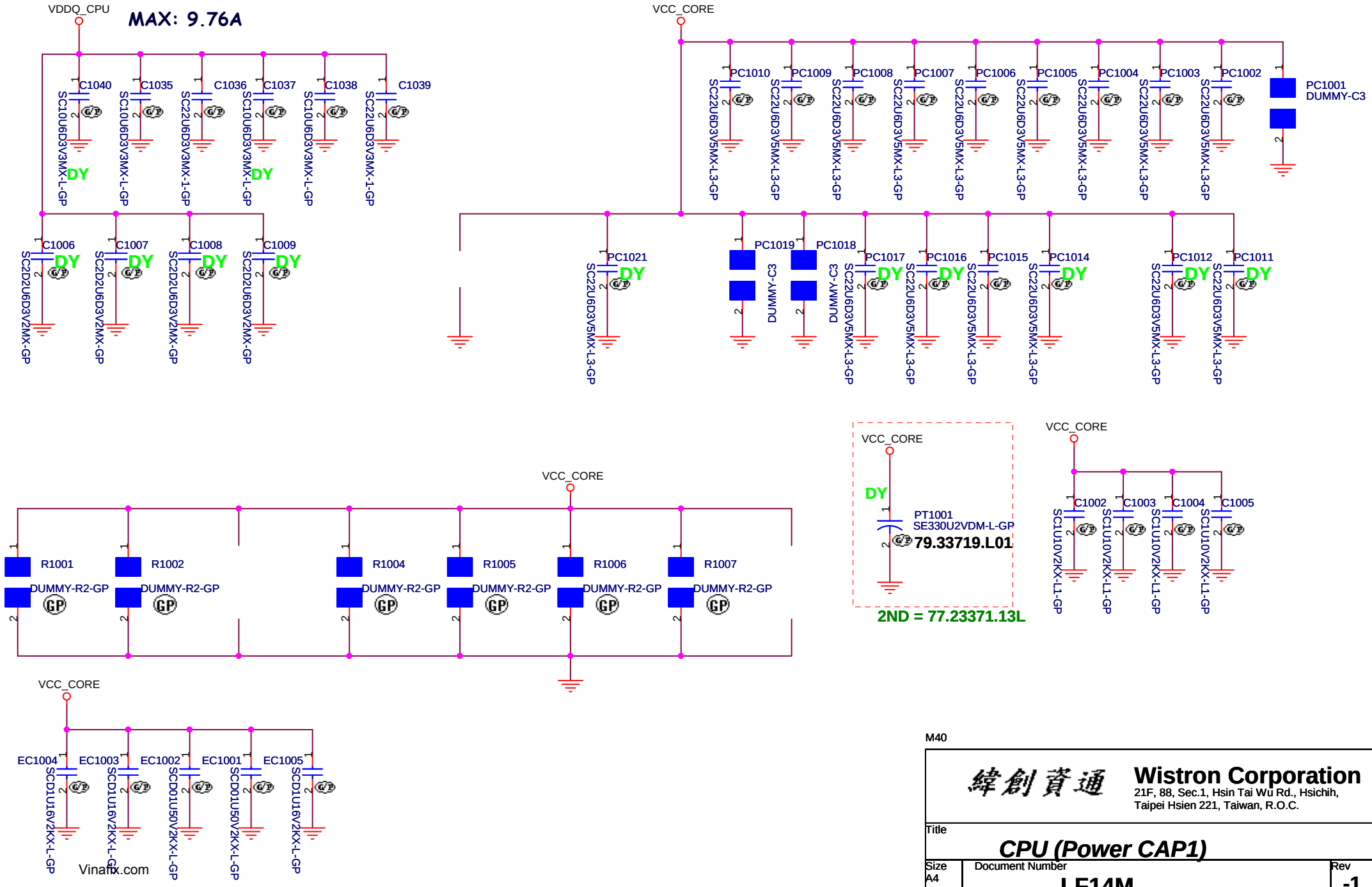

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Title: ***CPU (Power CAP1)***

Size	Document Number	Rev
A4	LF14M	-1

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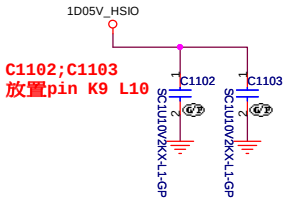
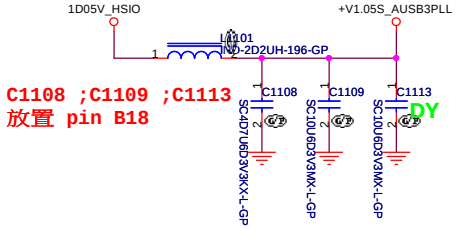
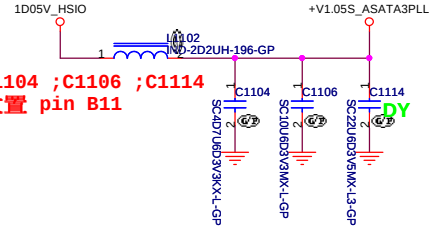
MAX: 1.92A



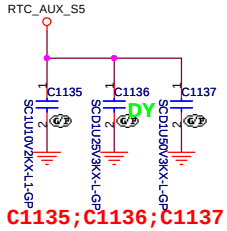
C1102;C1103
放置pin K9 L10



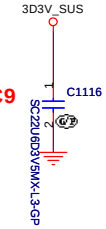
C1108 ;C1109 ;C1113
放置 pin B18



C1104 ;C1106 ;C1114
放置 pin B11

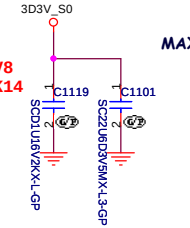


C1135;C1136;C1137
放置 pin AG10



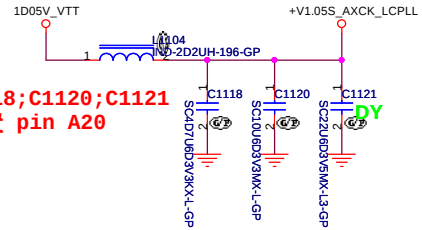
C1116放置 pin AC9

MAX: 0.285A

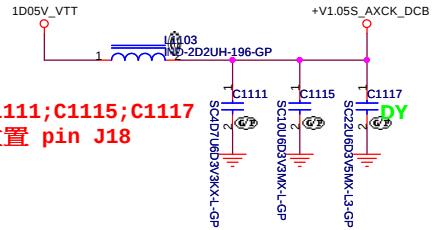


C1101 放置 pin V8
C1119 放置 pin K14

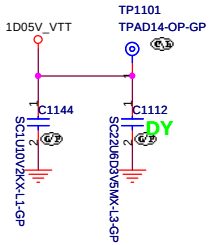
MAX: 3.51A



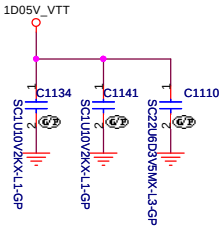
C1118;C1120;C1121
放置 pin A20



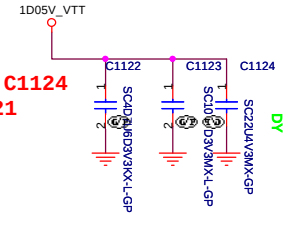
C1111;C1115;C1117
放置 pin J18



C1144;C1112
放置 pin AE9



C1110 放置 pin J11
C1134 C1141 放置 pin J11, AE8



C1122;C1123;C1124
放置 pin AA21

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Title: CPU (Power CAP2)

Size	Document Number	Rev
Custom	LF14M	-1

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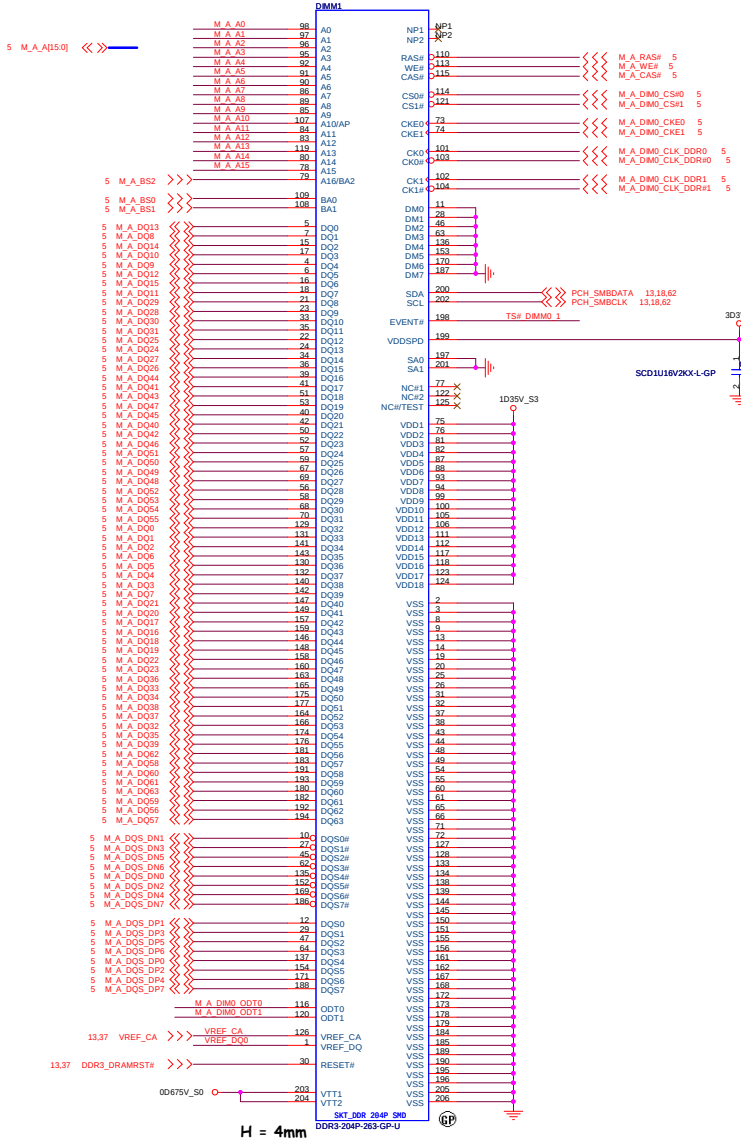
SSID = MEMORY

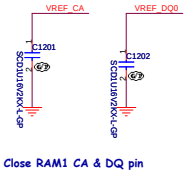


H = 4mm

62.10024.S61

1ST = 62.10024.S61

2ND = 62.10024.M51

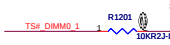


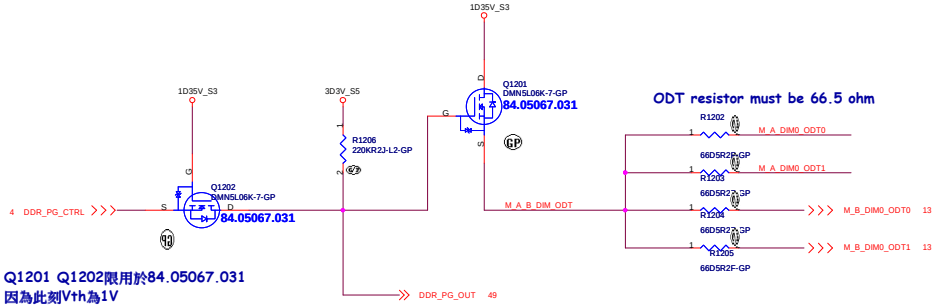
Close RAM1 CA & DQ pin

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

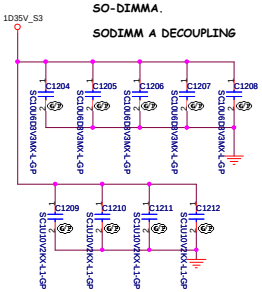


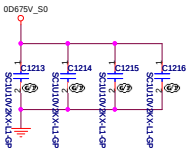


Q1201 Q1202限用於84.05067.031
因為此刻Vth為1V

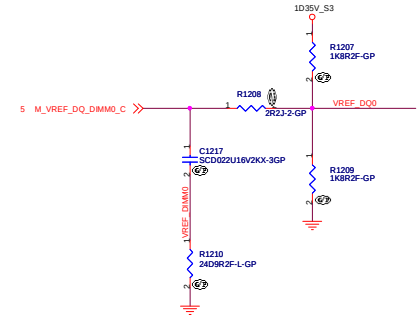
Layout Note:
Place these Caps near
SO-DIMMA.

SODIMM A DECOUPLING





Place these caps
close to VTT1 and
VTT2.



For Intel Recommend Close to DIMM

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Title: DDR3L-SODIMM1

Size	Document Number	Rev
A2	LF14M	-1

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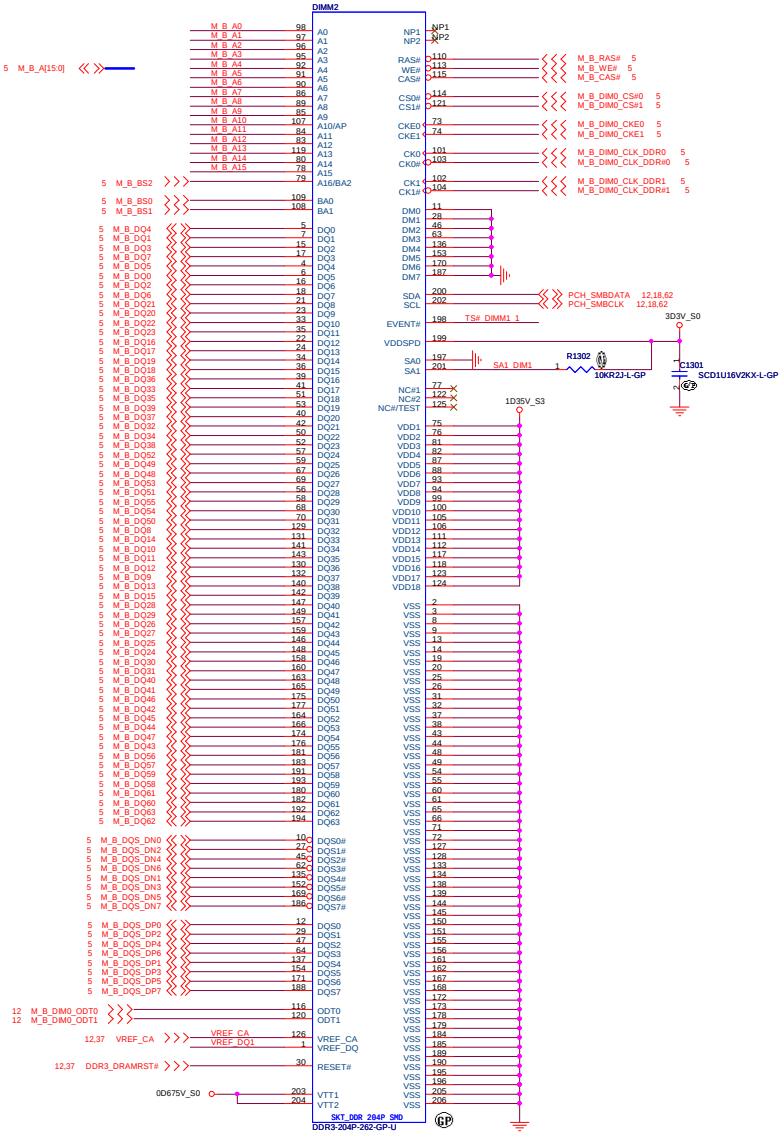
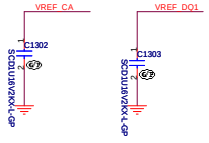
SSID = MEMORY



62.10024.S21

1ST = 62.10024.S21

2ND = 62.10024.M31

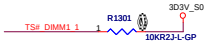


Close RAM3 CA & DQ pin

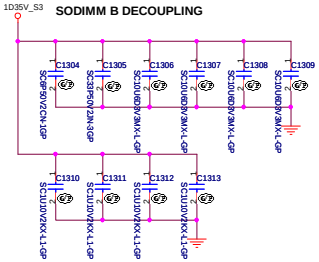
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

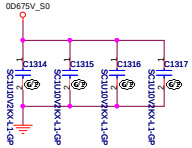
SO-DIMMB is placed farther from the Processor than SO-DIMMA

Thermal EVENT

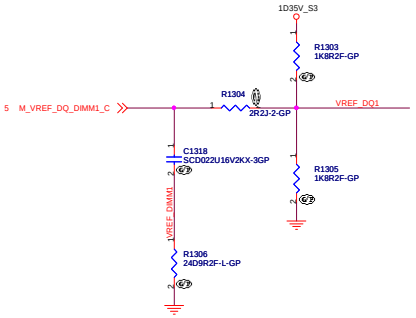


Layout Note:
Place these Caps near SO-DIMMB.





Place these caps close to VTT1 and VTT2.



For Intel Recommend Close to DIMM

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Title: *DDR3L-SODIMM2*

Size: A2 | Document Number: LF14M | Rev: -1

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Title
(Reserved)_SODIMM_SODIMM4

Size	Document Number	Rev
A4	**LF14M**	**-1**

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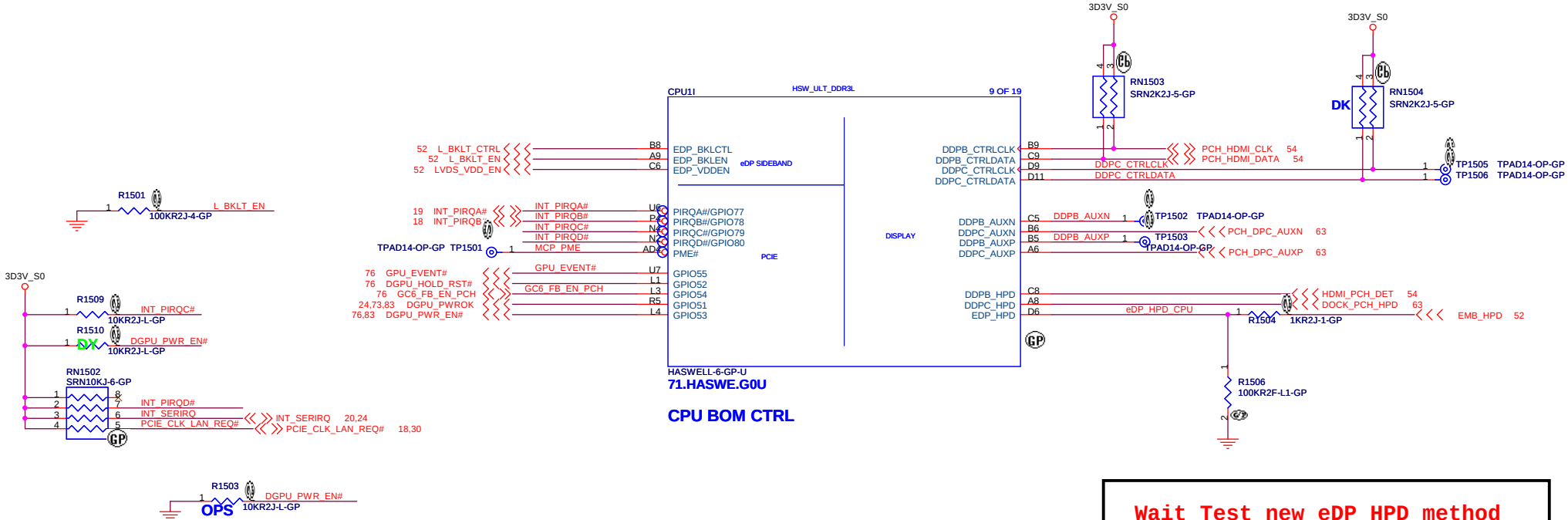

Wait Test new eDP_HPD method
(Simulation HPD signal)
Reduce Cable Pin

<Core Design>

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Title: CPU(EDP SIDEBAND/GPIO/DDI)

Size	Document Number	Rev
A3	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 15 of 102

SSID = PCH

2014/2/6
USB_PP1/PN1改接到USB2.0 Port 0
USB_PP0/PN0改接到USB2.0 Port 1
NET維持不變

USB2.0 Table

Pair	Device
0	USB3.0 Port 1 (with Debug Function)
1	Fingerprint / USB3.0 Card Reader(DY)
2	USB2.0 Port 2
3	Camera
4	USB2.0 Port 3
5	WLAN(Bluetooth)
6	USB3.0 to DOCKING
7	Panel Touch

USB 3.0 Table

Pair	Device
1	Combined with USB2.0 port1
2	Reserved
3	USB3.0 to DOCKING
4	USB 3.0 Card Reader

USB OverCurrent (OC#)

Pair	Device
0C#0	USB3.0 port1
0C#1	USB2.0 port2
0C#2	USB2.0 port3
0C#3	Reserved

GPU PEG BUS

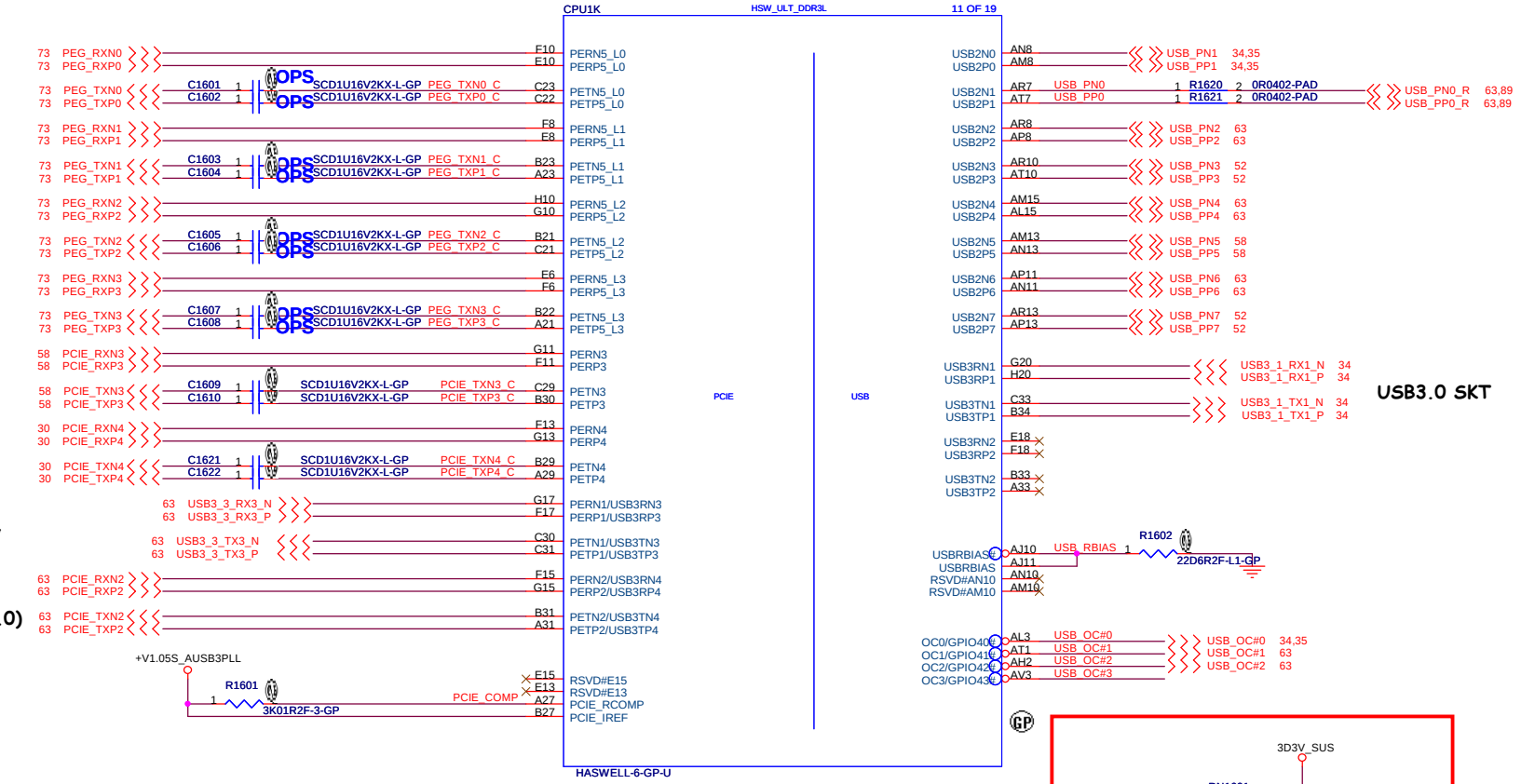
WLAN

LAN

DOCKING

Card Reader (PCIE/USB3.0)

USB3.0 SKT



71.HASWE.G0U

CPU BOM CTRL

Need Test if not Stuff

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCI/USB)

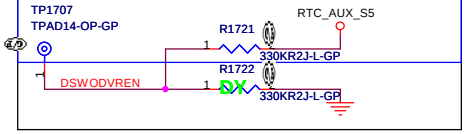
Size: A3 | Document Number: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet 16 of 102

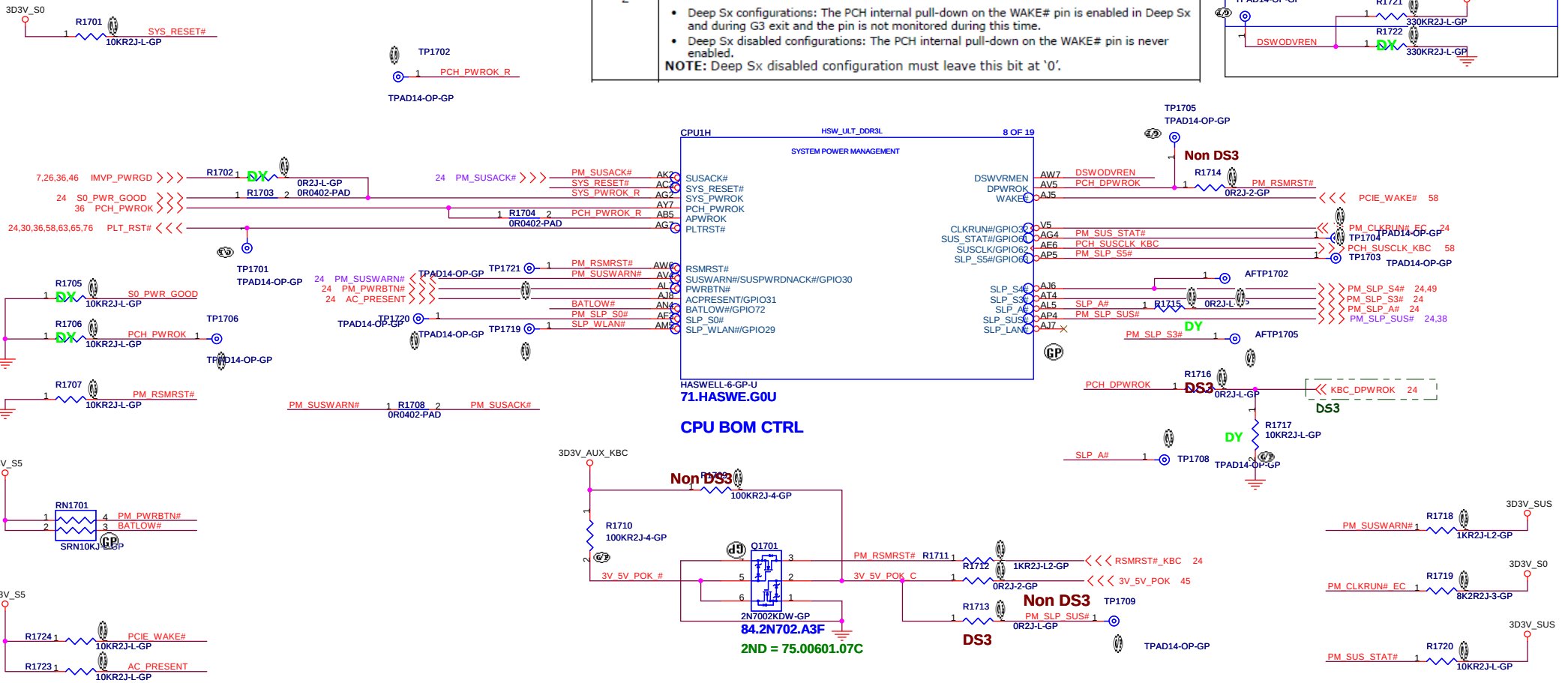
SSID = PCH

Bit	Description
31:3	Reserved
2	**WAKE# Pin Deep Sx Enable (WAKE_PIN__DSX_EN)** - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0': • Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. • Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. **NOTE:** Deep Sx disabled configuration must leave this bit at '0'.

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



Follow Intel CRB



Vinafix.com

<Core Design>

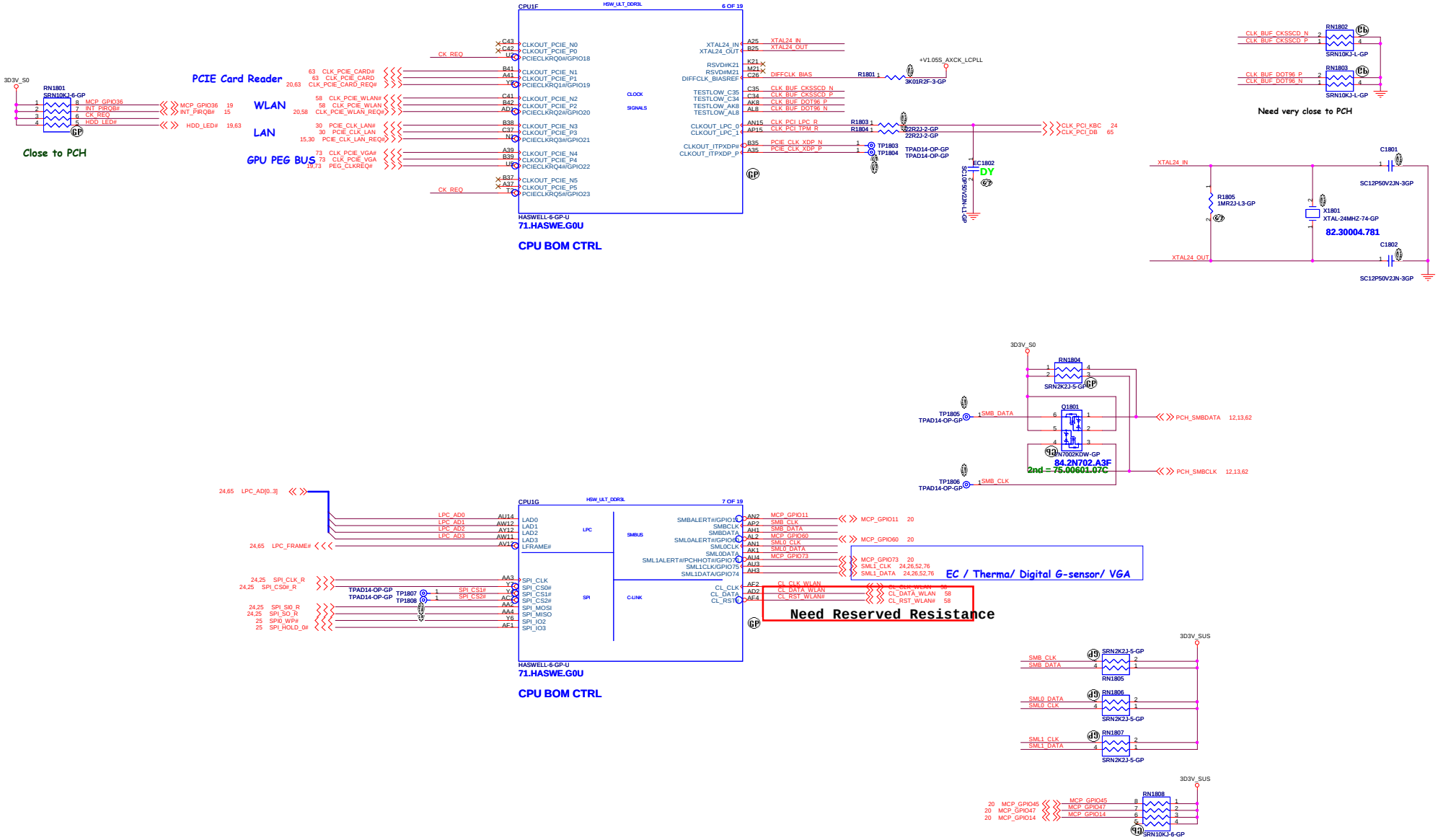
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DMI/FDI/PM)

Size: A3 | Document Number: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet 17 of 102

SSID = PCH



Vinafix.com

<Core Design>

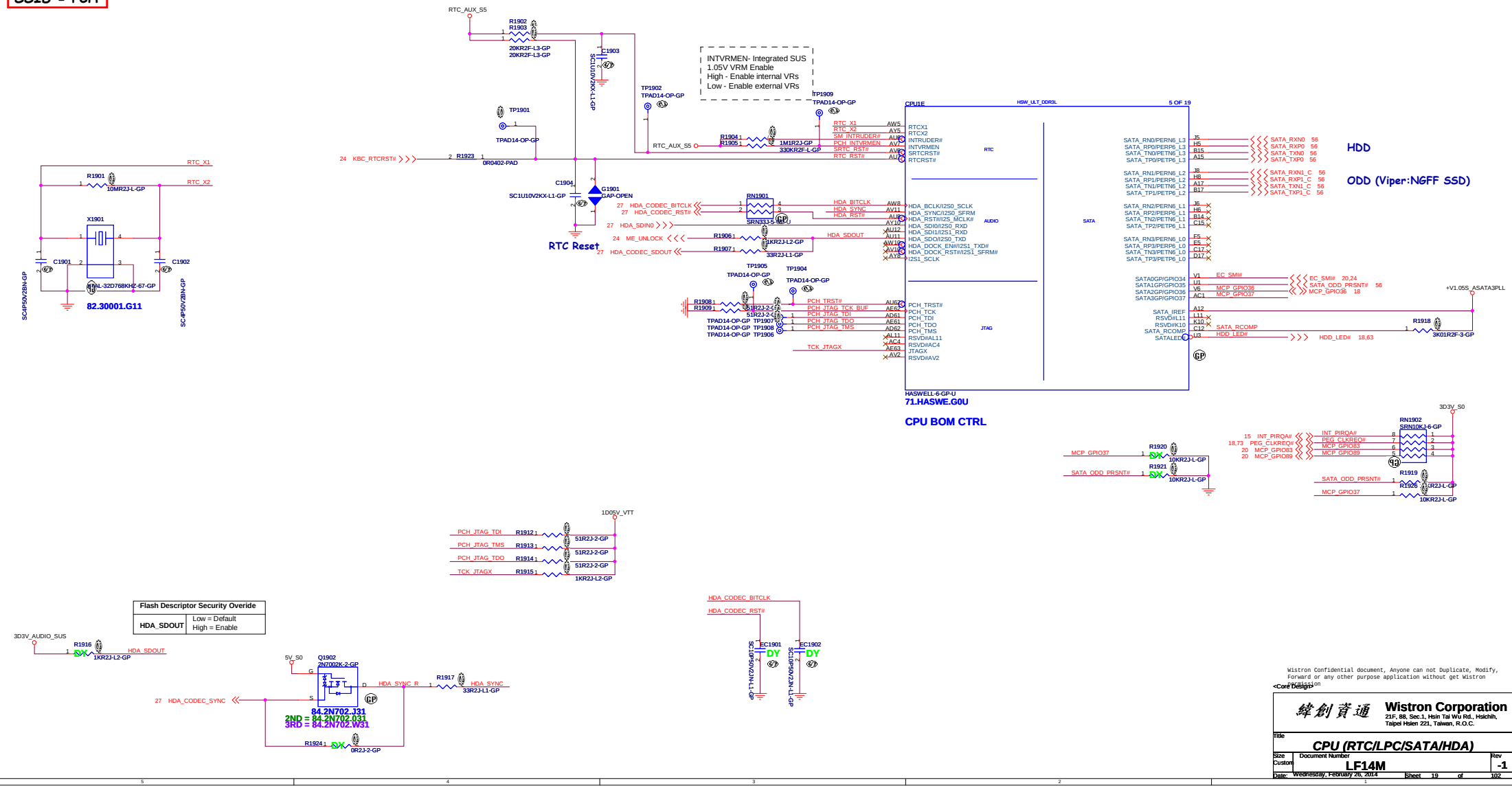
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCI-E/SMBUS/CLOCK/CL)

Size: A2 | Document Number: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet 18 of 102

SSID = PCH



Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

<Core Design>

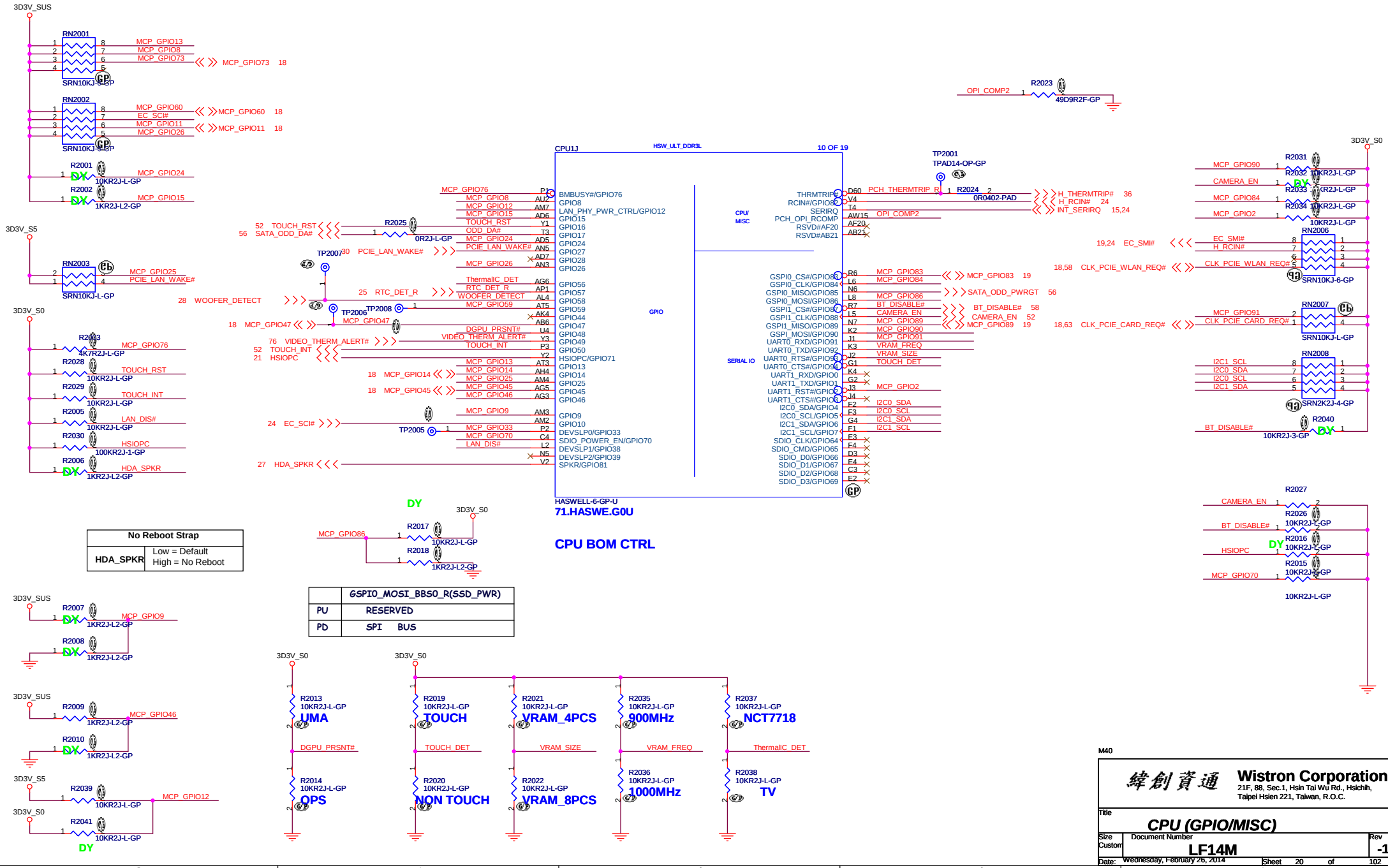
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RTC/LPC/SATA/HDA)

Size: Custom | Document Number: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet 19 of 102

SSID = PCH



M40

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

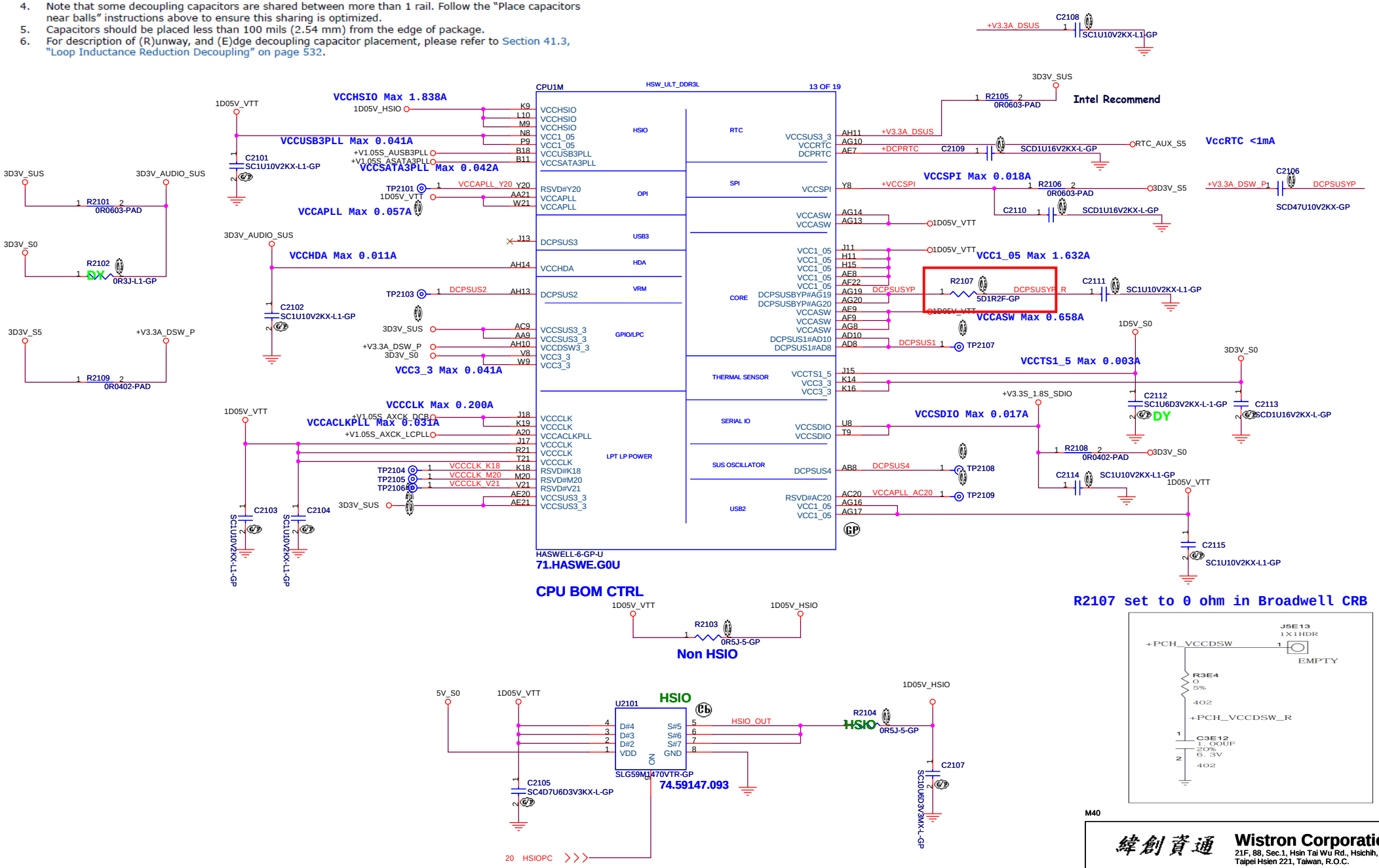
Title: CPU (GPIO/MISC)

Size	Document Number	Rev
Custom	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 20 of 102

Notes:

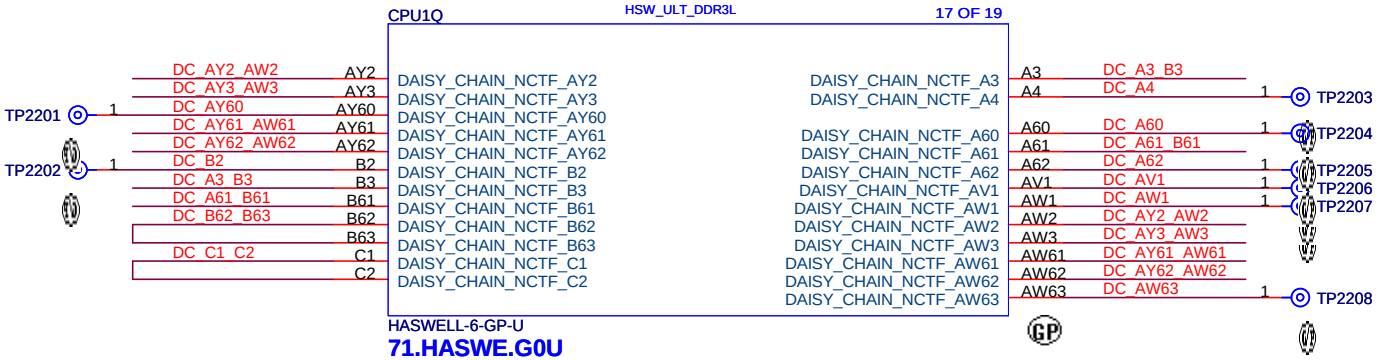
1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to Section 41.3, "Loop Inductance Reduction Decoupling" on page 532.



M40

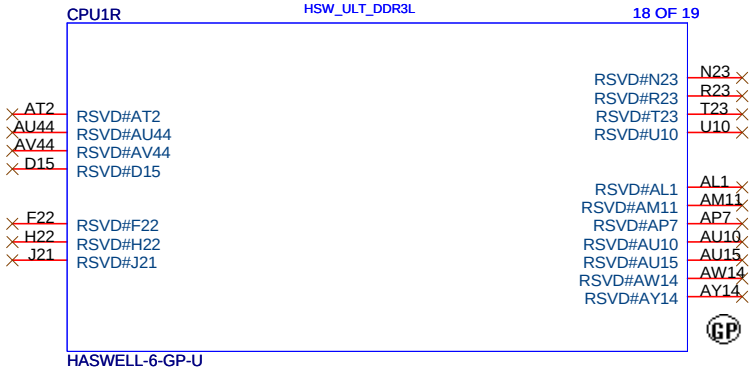
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (POWER1)	
Size A3	Document Number LF14M	Rev -1
Date: Wednesday, February 26, 2014	Sheet 21 of 102	



71.HASWE.G0U

CPU BOM CTRL



71.HASWE.G0U

CPU BOM CTRL

M40

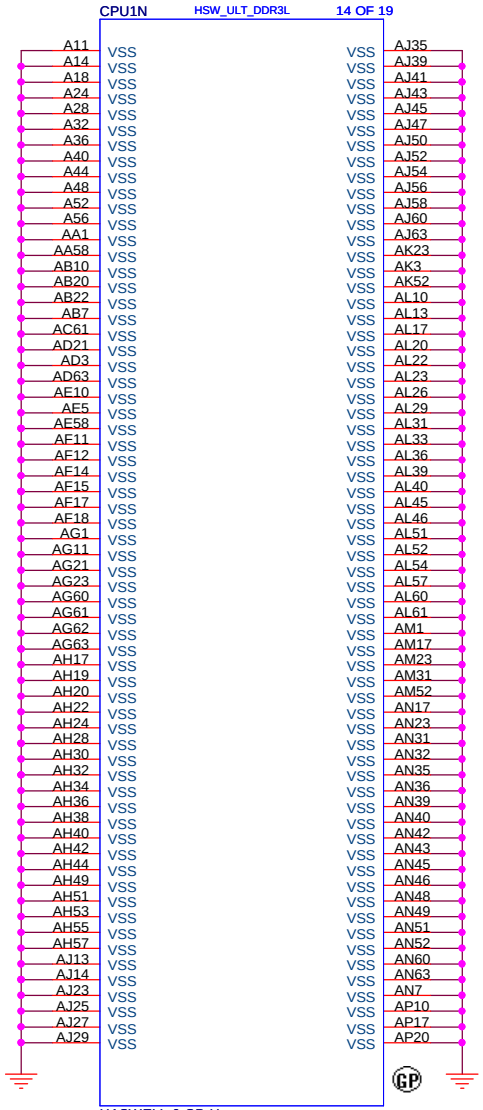
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

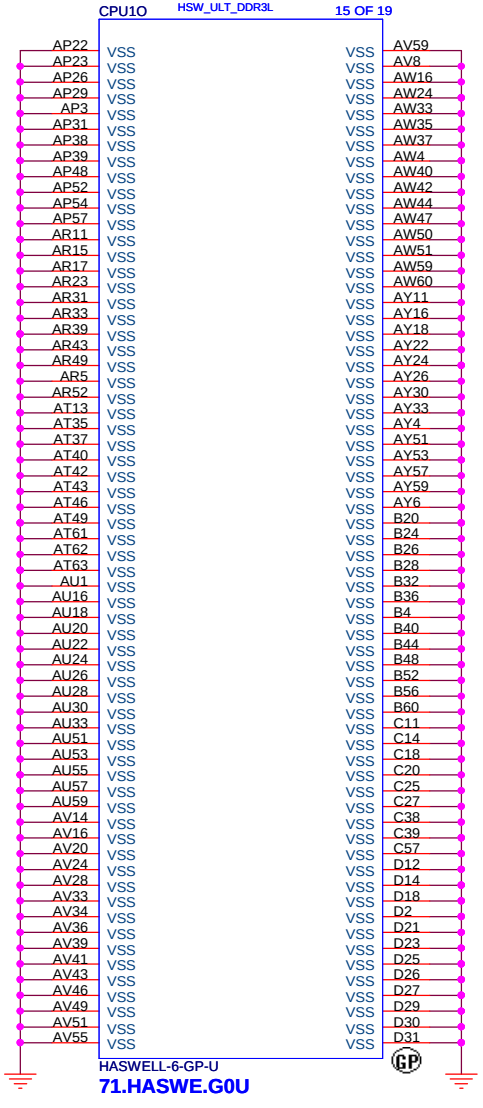
Title: ***CPU (RSVD)***

Size	Document Number	Rev
Custom	**LF14M**	**-1**

Date: Wednesday, February 26, 2014 Sheet 22 of 102

SSID = PCH





M40

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size	Document Number	Rev
Custom	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 23 of 102

SSID = KBC

Model_ID_BOM Ctrl (2013/9/16 update)

MODEL ID

BOM Ctrl_Model

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
LF14M, Intel (Broadwell)	100.0K	10.0K 64.10025.6DL	3.0V
LF15M, Intel (Broadwell)	100.0K	20.0K 64.20025.1DL	2.75V
LF15V, Intel, (Broadwell)	100.0K	33.0K 64.33025.1DL	2.48V
LM40L Intel (Broadwell)	100.0K	47.0K 64.47025.6DL	2.24V
LM50L Intel (Broadwell)	100.0K	64.9K 64.64925.DL	2.0V
LF14M, Intel (Haswell)	100.0K	76.8K 64.76825.6DL	1.87V
LF15M, Intel (Haswell)	100.0K	100K 64.10035.6DL	1.65V
LM40L Intel (Haswell)	100.0K	143K 64.14335.6DL	1.358V
LM50L Intel (Haswell)	100.0K	174K 64.17435.6DL	1.204V
Reserved	100.0K	215K 64.21535.6DL	1.048V

PCB VERSION (2013/10/17 update)

BOM Ctrl_VER

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

AC Adapter	ADT_TYPE	System Power Limit
130W	1.663V < ID <= 2.102V	90W
90W	1.172V < ID <= 1.618V	90W
65W	0.693V < ID <= 1.134V	65W
45W	0.214V < ID <= 0.663V	45W

Prevent BIOS data loss solution

Nuvoton KBC PSL Power Logic

84.02130.031

84.2N702.J31

2ND = 84.2N702.031

EC_GPIO47 High Active

84.2N702.J31

2nd = 84.2N702.031

3RD = 84.2N702.W31

NPCE285G

071.00285.001G

BATTERY / CHARGER ---->

PCH / GPU N15S / Gsensor /NCT7718

TP ---->

Non AOAC

AOAC

Reserved for AOAC

C2422 close to Pin44

R2472 close to Pin103

2013/9/12

GPIO83/SOUT_CR & GPIO87/SIN_CR

Need reserved TP for Debug

NOTE:
Please be aware that the SPI interface trace length between PCH and EC should not exceed 650mils. The mismatch of SPI interface signals between EC and SPI flash should not exceed 500mils.

NOTE:
Locate resistors R2415 and R2417 close to the U24H.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

NOTE:
PWM Signal :
1. If unused, select altrnative GPIO function and enable internal pull-down.
2. Please measure and make sure that the rise time of VCC_POR is less than 10us.

EC GPIO PH

EC GPIO PL

Vinafix.com

<Core Design>

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

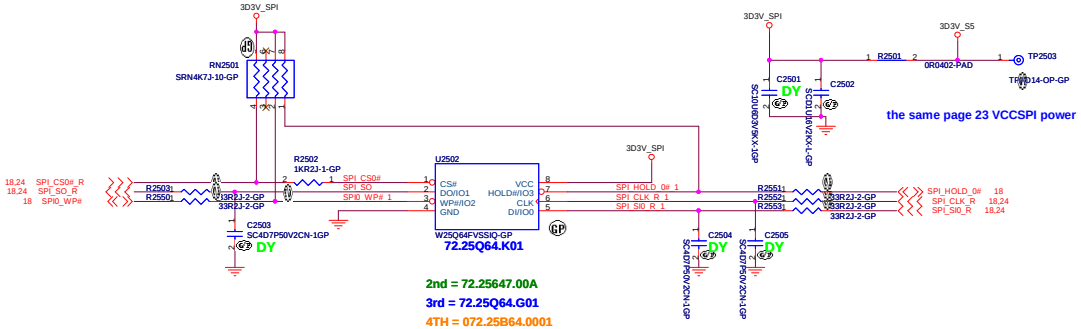
Title: KBC_NPCE985P

Size: A3 | Document Number: LF14M | Rev: -1

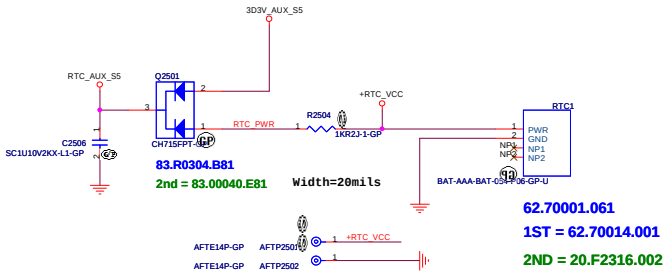
Date: Wednesday, February 26, 2014 | Sheet 24 of 102

SSID = Flash.ROM

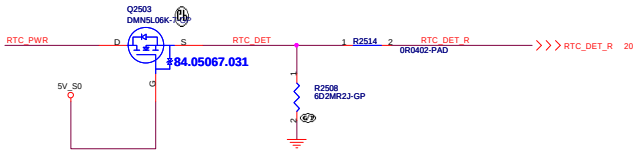
SPI ROM Equal length need to less than 500mil



SSID = RBATT



High Detect
Need to Check whether to PD in PCH Side



M40

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Flash(KBC+PCH)/RTC***

Size: A2 | Document Number: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet 25 of 102

SSID = Thermal

Thermal sensor NCT 7718W

Layout 15 mil

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

2.System Sensor, Put on palm test

ALERT# /T_CRIT#
Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

T8=85 degree

PTC Function M40/M50 (All Series Reserved)

5V *100K/(100K+40K) = 3.57V

	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low

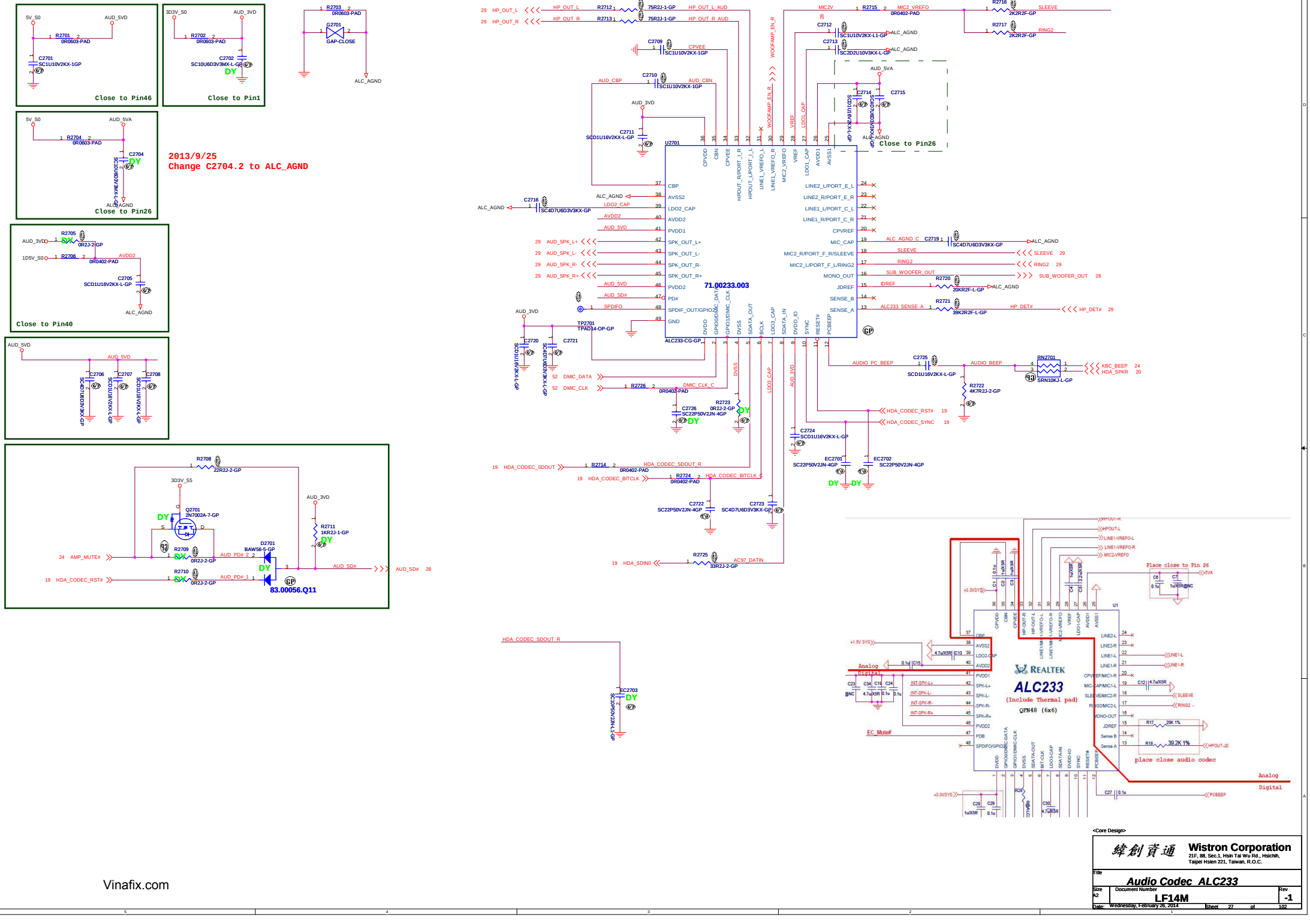
PTC Placement List

	PTC Position
RT2606	5V_PWR_DC/DC_High_side_FET (PU4507)
RT2605	3V_PWR_DC/DC_High_side_FET (PU4504)
RT2609	BT+ High side FET (PU4403)
RT2607	1D05V_PWR_DC/DC_High_side_FET (PU4802)
RT2603	1D35V_S3_DC/DC_High_side_FET (PU4902)
RT2610	1D5V_PWR_VGA_DC/DC_High_side_FET(PU5110)
RT2602	VCC_CORE_Driver-1 (PU4702)
RT2601	VCC_CORE_Driver-2 (PU4701)
RT2608	VGA_CORE_DC/DC_MOSFET (PU8202)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal 7718/Fan Controllor P2793
Size: A2 | Document Number: LF14M | Rev: -1
Date: Wednesday, February 26, 2014 | Sheet 26 of 102



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<Core Design>

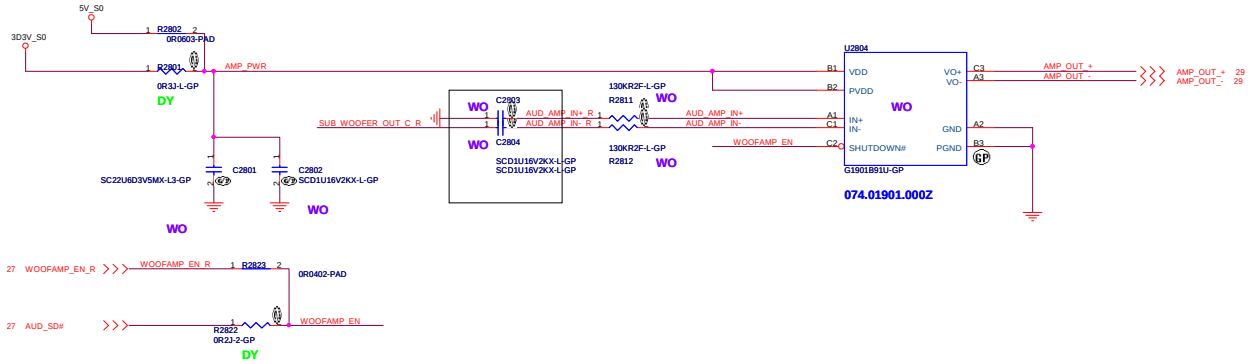
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Codec ALC233**

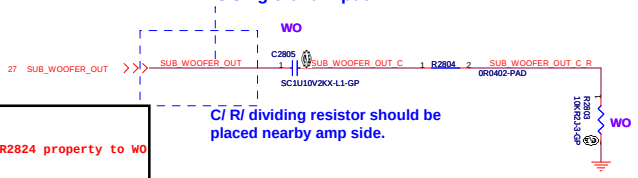
Size	Document Number	Rev
A2	LF14M	-1

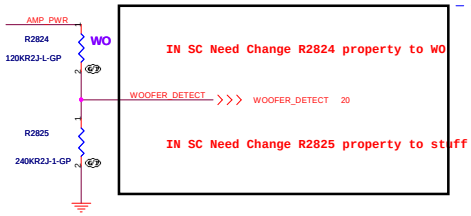
Date: Wednesday, February 26, 2014 Sheet 27 of 102

WOOFER AMP. U40/U50



1.2V vrms single-end input





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio Codec ALC233***

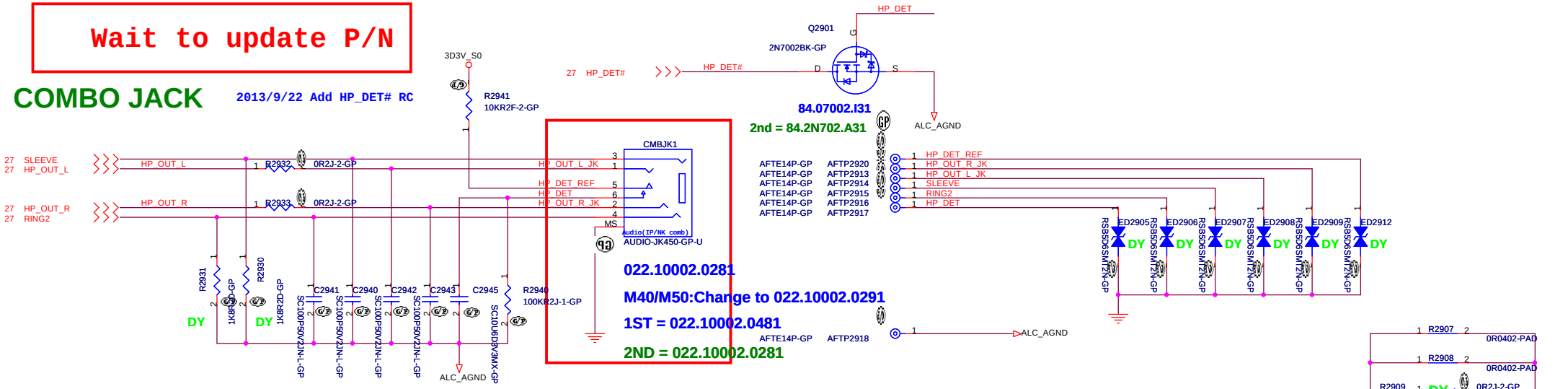
Size: A2 | Document Number: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet 28 of 102

Wait to update P/N

COMBO JACK

2013/9/22 Add HP_DET# RC



022.10002.0281

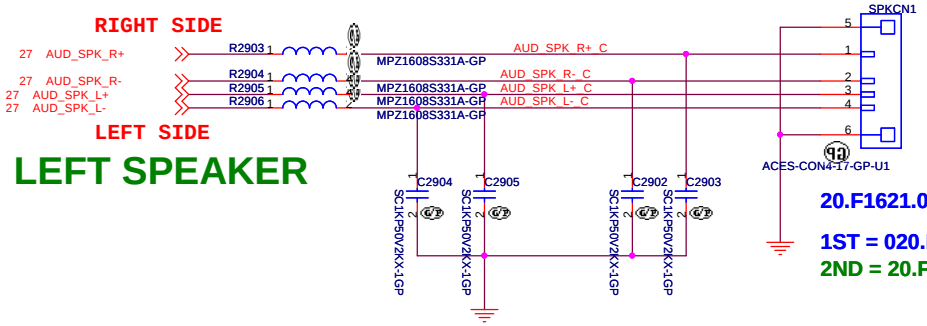
M40/M50:Change to 022.10002.0291

1ST = 022.10002.0481

2ND = 022.10002.0281

RIGHT SPEAKER

RIGHT SIDE



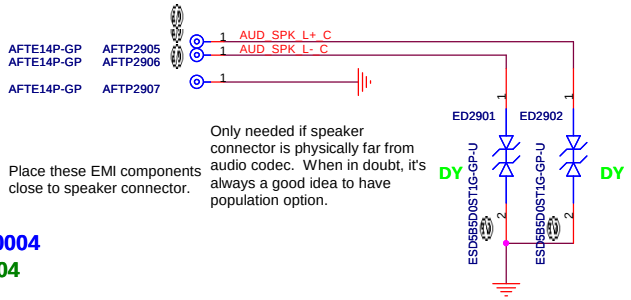
LEFT SIDE

LEFT SPEAKER

20.F1621.004

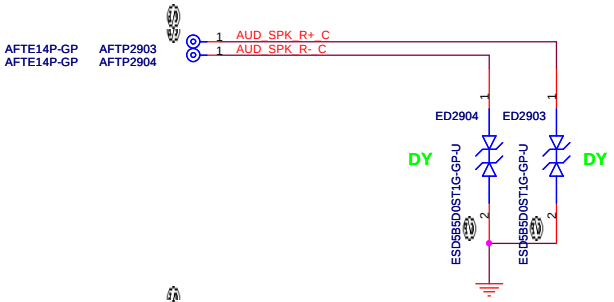
1ST = 020.F0156.0004

2ND = 20.F1937.004

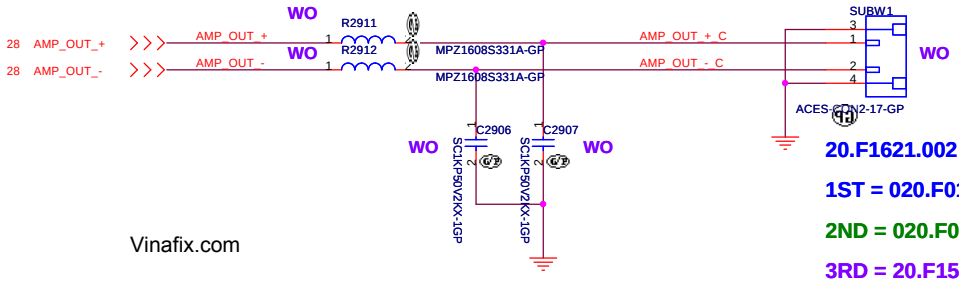


Place these EMI components close to speaker connector.

Only needed if speaker connector is physically far from audio codec. When in doubt, it's always a good idea to have population option.



SUB WOOFER (U40/U50)



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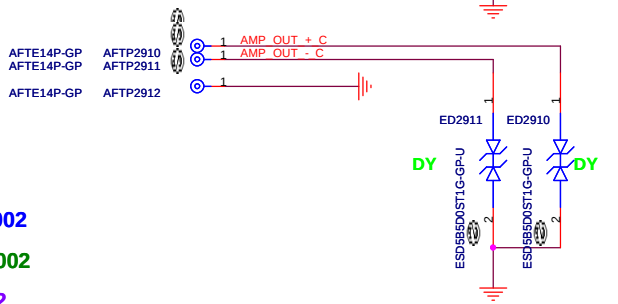
20.F1621.002

1ST = 020.F0156.0002

2ND = 020.F0157.0002

3RD = 20.F1561.002



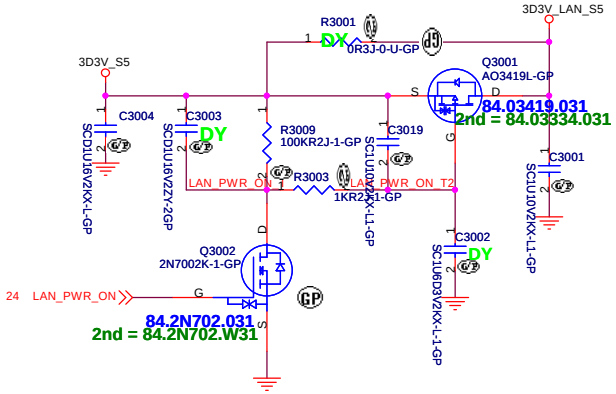
<Core Design>

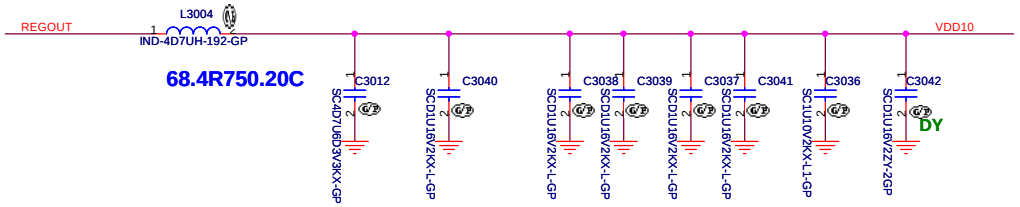
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MIC/SPEAKER/AUDIO JACK

Size: A3 | Document Number: LF14M | Rev: -1

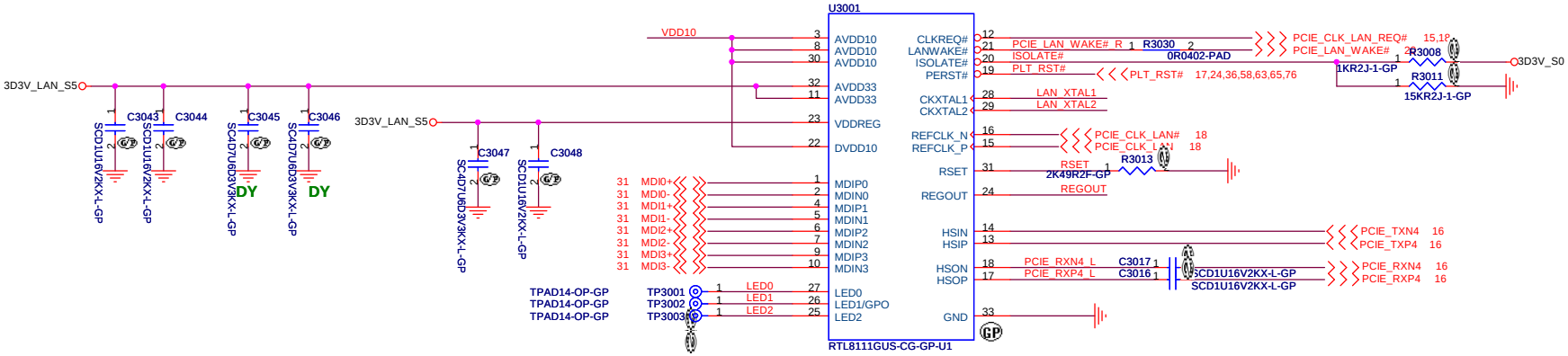
Date: Wednesday, February 26, 2014 | Sheet 29 of 102





For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
***Place C3038 to C3041 close to each VDD10 pin-- 3, 8, 22, 30**

For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
***Place C20 and C21 close to each VDD10 pin-- 22 (Reserved)**



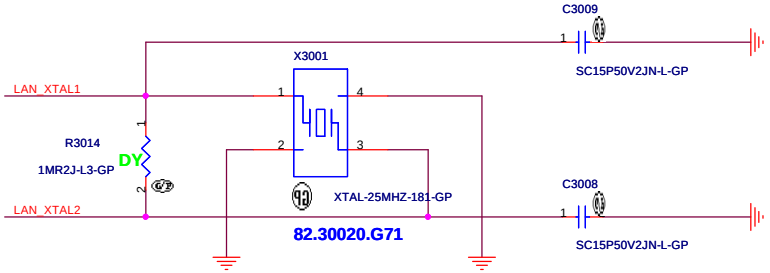
71.08111.W03

10/100 = 71.08106.003

GIGA = 71.08111.W03

LAN BOM CTRL

25MHz XTAL



<Core Design>

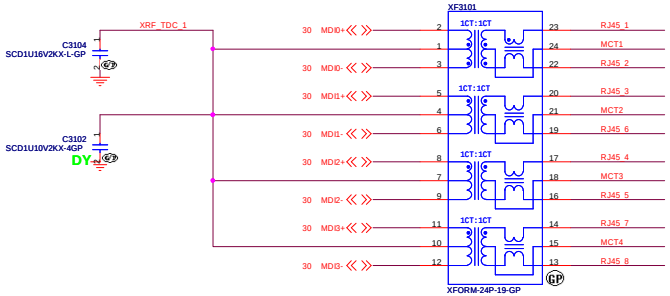
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN RTL8111GUL RTL8106EUL***

Size	Document Number	Rev
A3	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 30 of 102

10/100M/1000M Lan Transformer

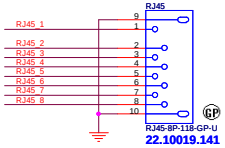


68.IH601.301

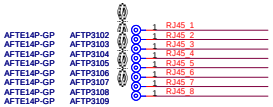
1ST = 068.IH219.3001

2ND = 68.89246.301

LAN Connector

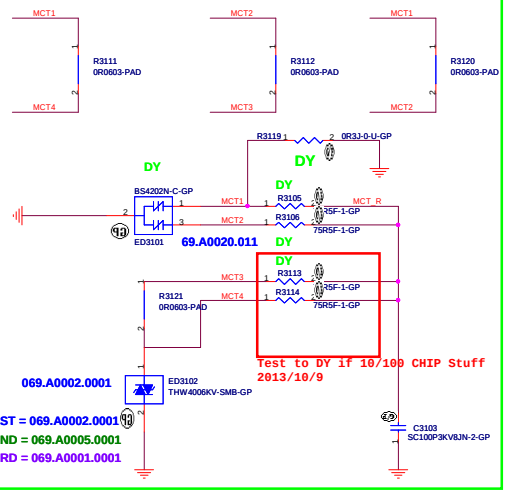


22.10019.141



10/100/1000 LAN surge circuit

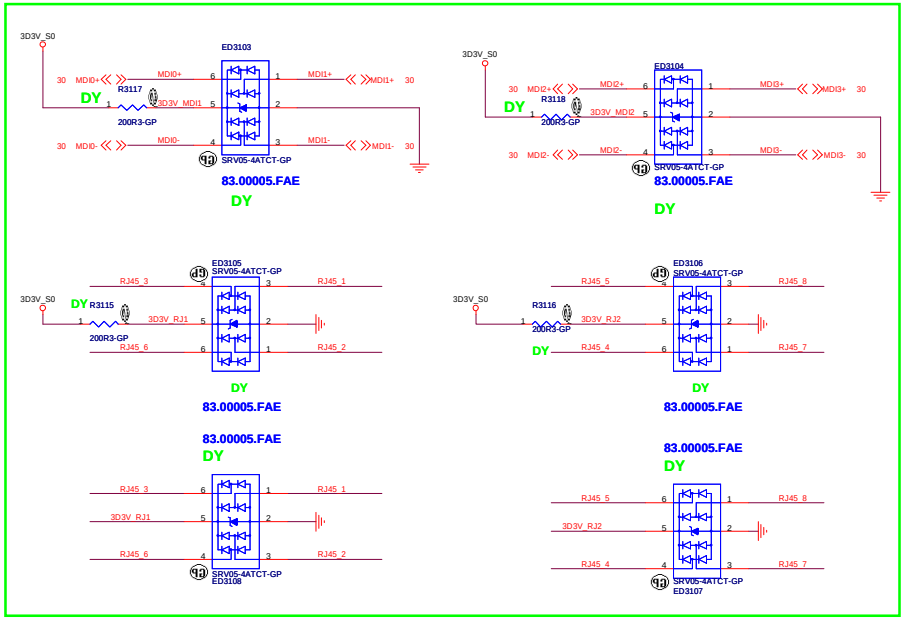
For test stuff



1ST = 069.A0002.0001

2ND = 069.A0005.0001

3RD = 069.A0001.0001



83.00005.FAE

DY

83.00005.FAE

DY

83.00005.FAE

DY

83.00005.FAE

DY

83.00005.FAE

DY

83.00005.FAE

DY

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<Core Design>

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Title: LAN CONNECTOR

Size: A2 | Document Number: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet 31 of 102

M40

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Title

CARD READER(Reserved)

Size	Document Number	Rev
Custom	**LF14M**	**-1**

Date: Wednesday, February 26, 2014 Sheet 32 of 102

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Title
CARD Reader

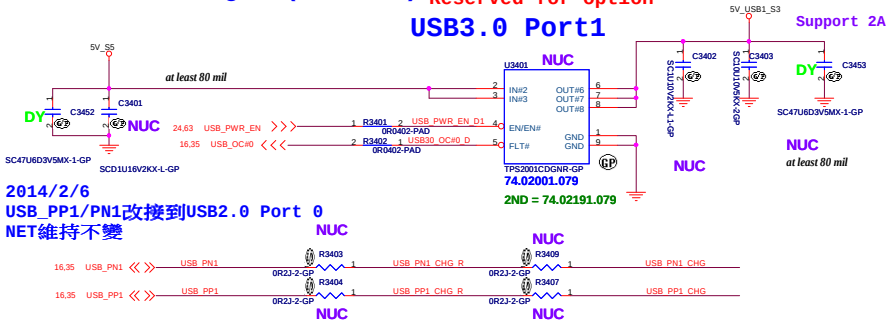
Size	Document Number	Rev
A4	**LF14M**	**-1**

Date: Wednesday, February 26, 2014 Sheet 33 of 102

Non USB Charger (U40/U50)

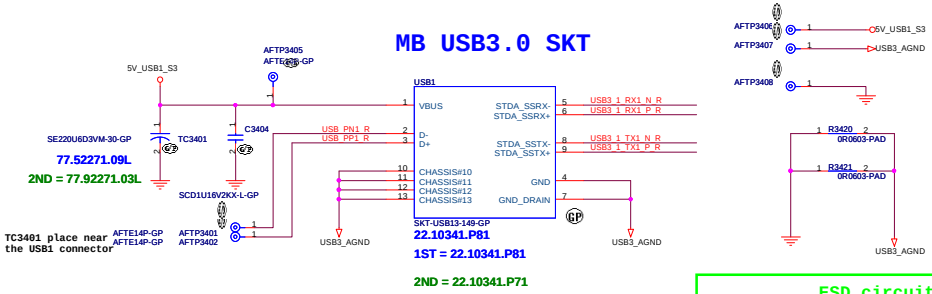
2013/8/30 update
Reserved for option

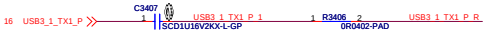
USB3.0 Port1

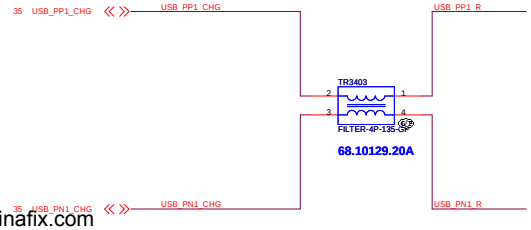


2014/2/6
USB_PP1/PN1改接到USB2.0 Port 0
NET維持不變

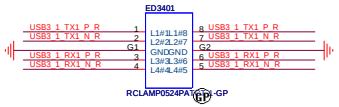
MB USB3.0 SKT



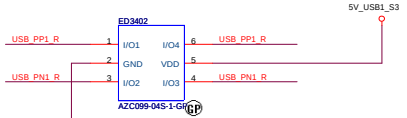




ESD circuit



DY



75.09904.07C

DY

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<Core Design>

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Title: USB 2.0 / 3.0 Port

Size: A2 | Document Number: LF14M | Rev: -1

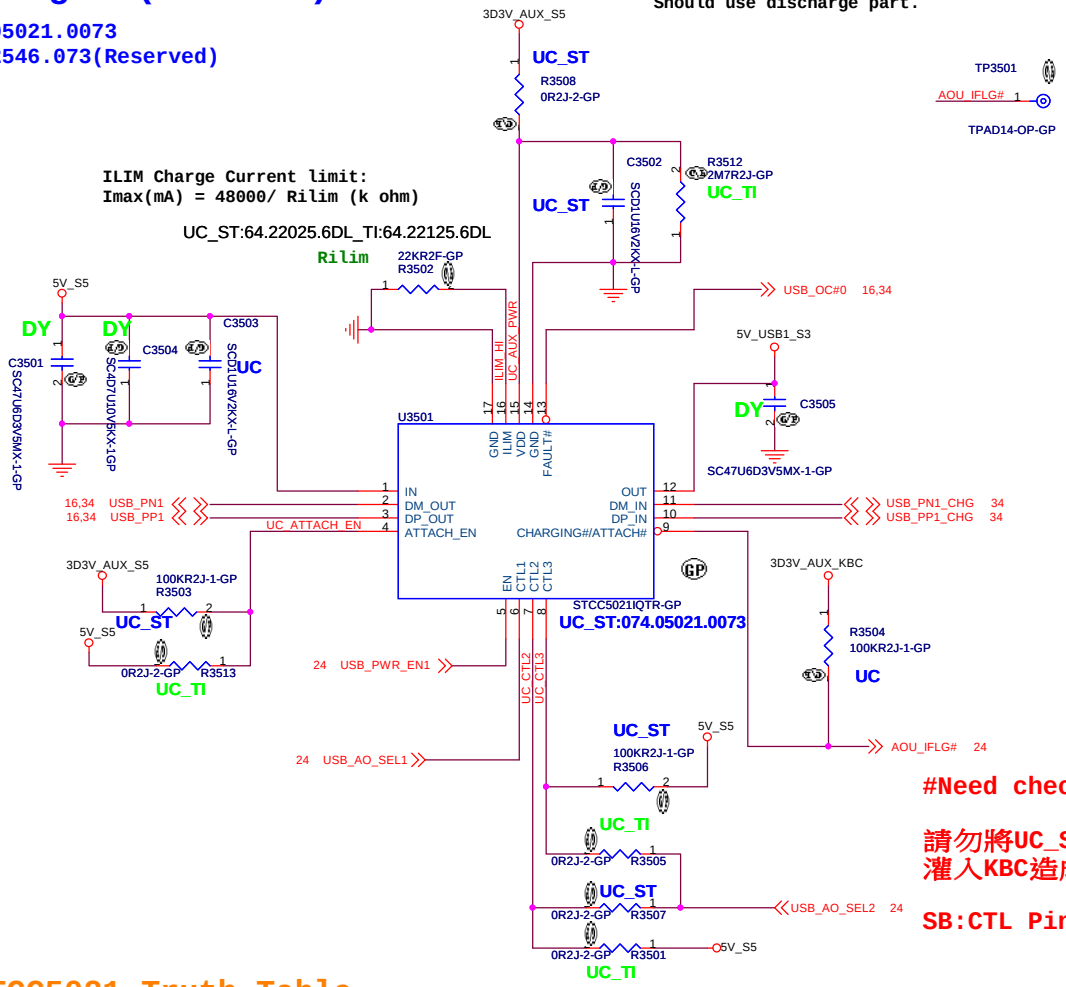
Date: Wednesday, February 26, 2014 | Sheet 34 of 102

USB Charger (M40/M50)

ST:074.05021.0073
TI:74.02546.073(Reserved)

2013/9/10 Change Power Source to 5V_S5
2013/9/18 Change Charger IC to STCC5021

Should use discharge part.



#Need check KBC GPIO Port is PSL_IN

請勿將UC_ST和UC_TI同時上件，以免5V電壓灌入KBC造成損壞

SB:CTL Pin改成3D3V_S5 Source

STCC5021 Truth Table

Table 5. Truth table control pins CTLx

Host state	CTL1	CTL2	CTL3	Mode description
S0, S1	1	1	1	CDP BC1.2 with charging detection.
S3	0	1	1	CDP with remote wakeup for low-speed USB devices / DCP auto-mode for full-speed or high-speed USB devices or after a USB device detached
S4, S5	0	0	1	DCP auto-detect mode without remote wakeup, with charging detection

Table 6. Attach detector truth table

ATTACH_EN	EN	Attach detector
0	x	OFF
1	1	OFF
Vinafix.com1	0	ON

M40

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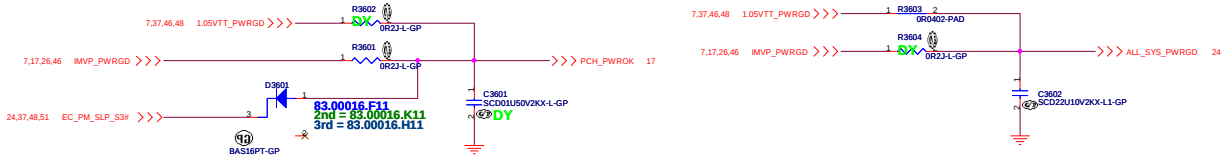
Title: USB 3.0

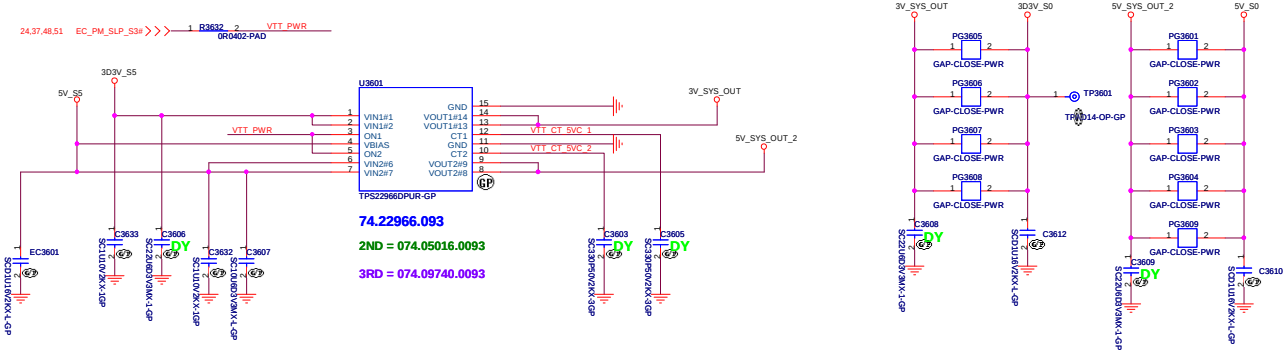
Size: A3 | Document Number: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet 35 of 102

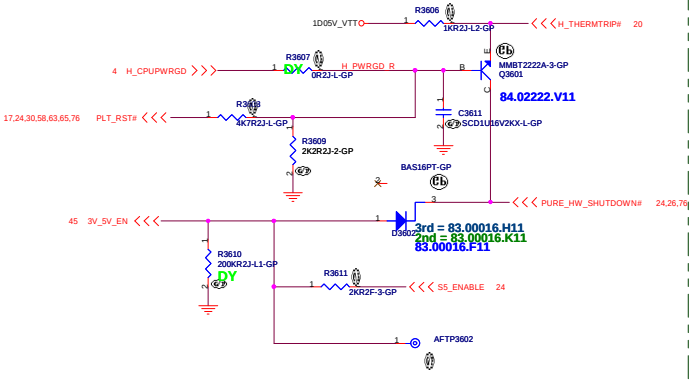
Power Sequence

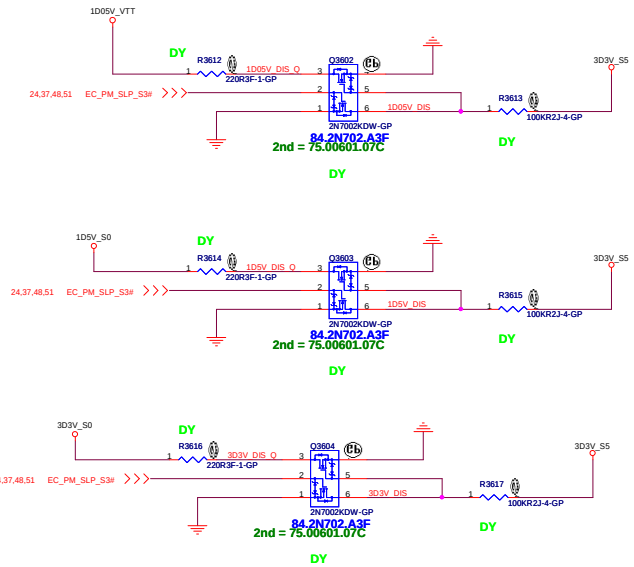


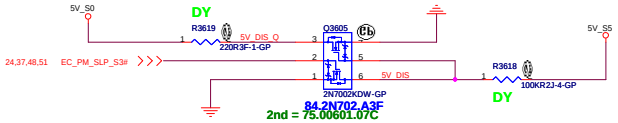
Run Power



Discharge circuit







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Title: **Power Plane Enable & SEQUENCE**

Size	Document Number	Rev
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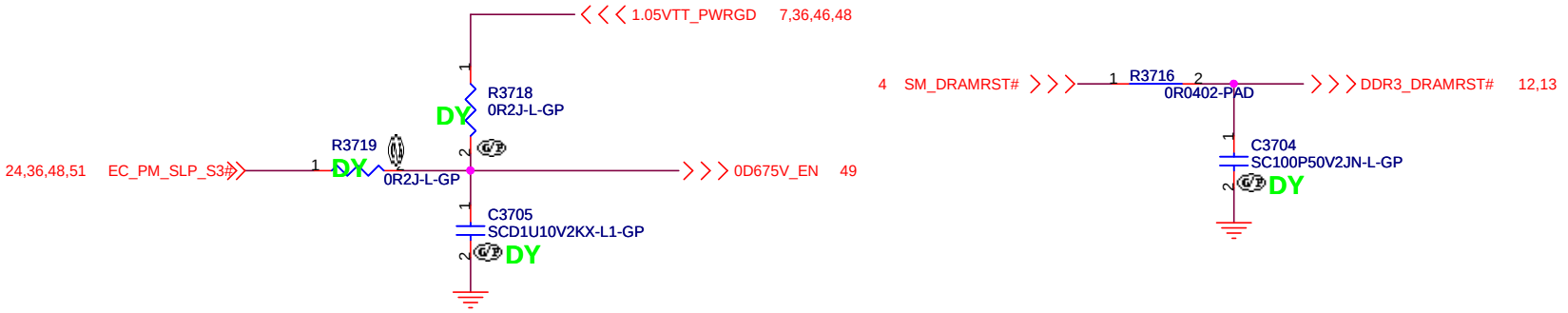

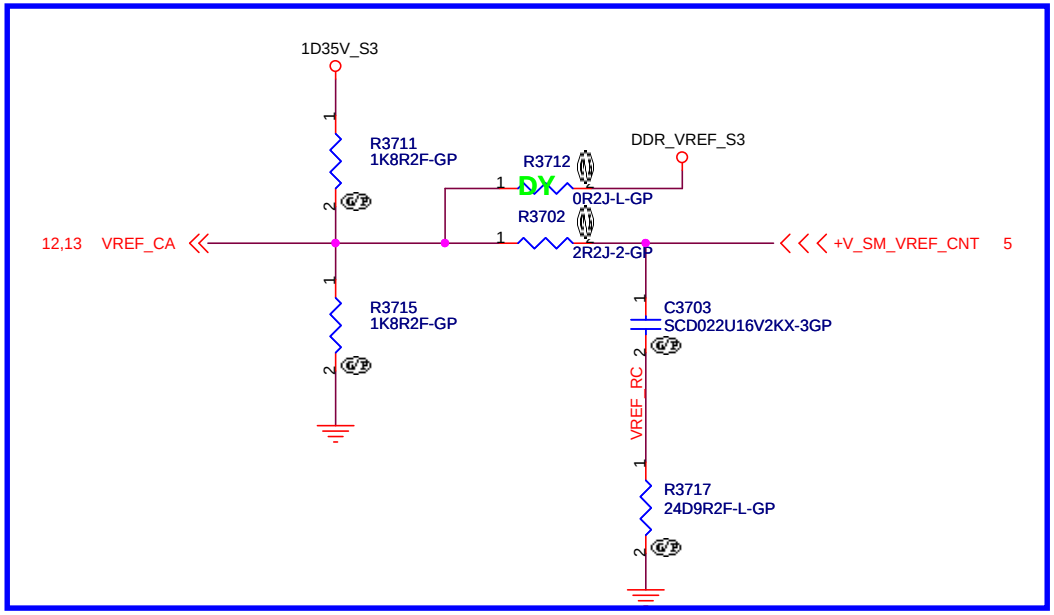

For Intel Recommend Close to DIMM

M40

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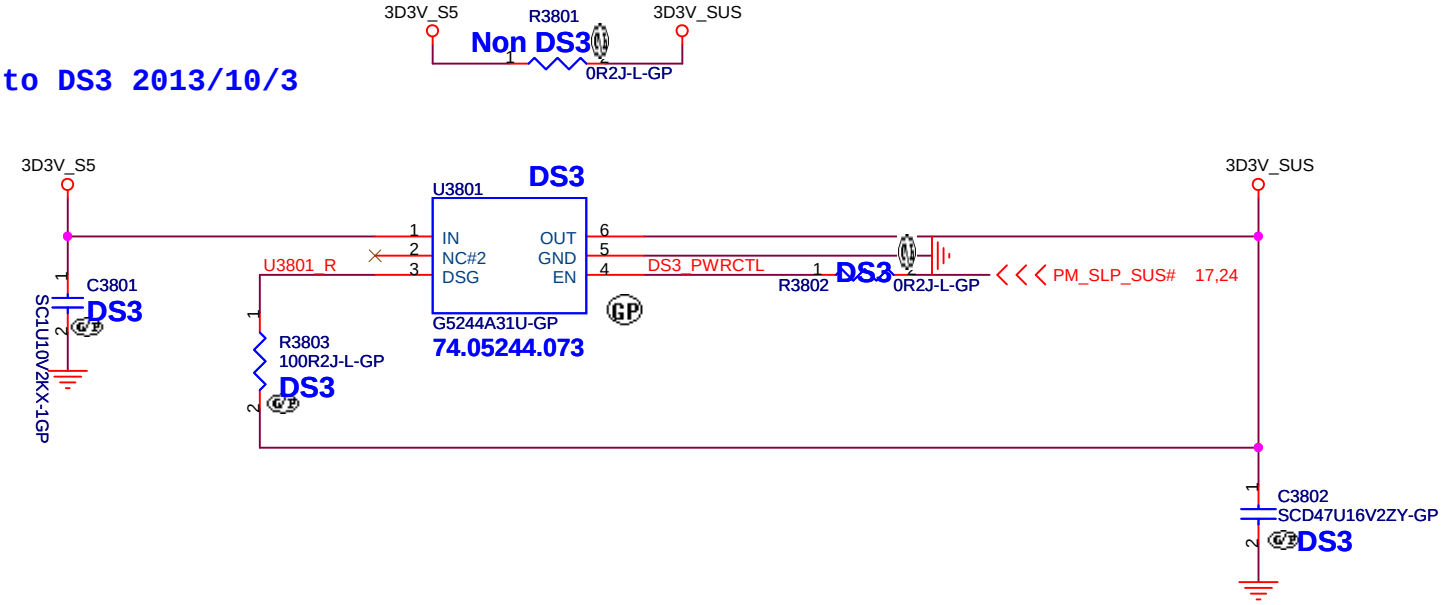
Title	***ADAPTER OCP / S3 reduction***
Size: Custom	Document Number: **LF14M** — Rev: **-1**
Date: Wednesday, February 26, 2014	Sheet 37 of 102

C3801 Change to DS3 2013/10/3



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Title: *(Reserved)*		
Size: A4	Document Number: LF14M	Rev: -1
Date: Wednesday, February 26, 2014	Sheet 38 of 102	

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Title	***1D05_M***	
Size: Custom	Document Number: **LF14M**	Rev: **-1**
Date: Wednesday, February 26, 2014	Sheet 39 of 102	

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緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Connected Standby1

Size	Document Number	Rev
A	**LF14M**	**-1**

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緯創資通

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Title

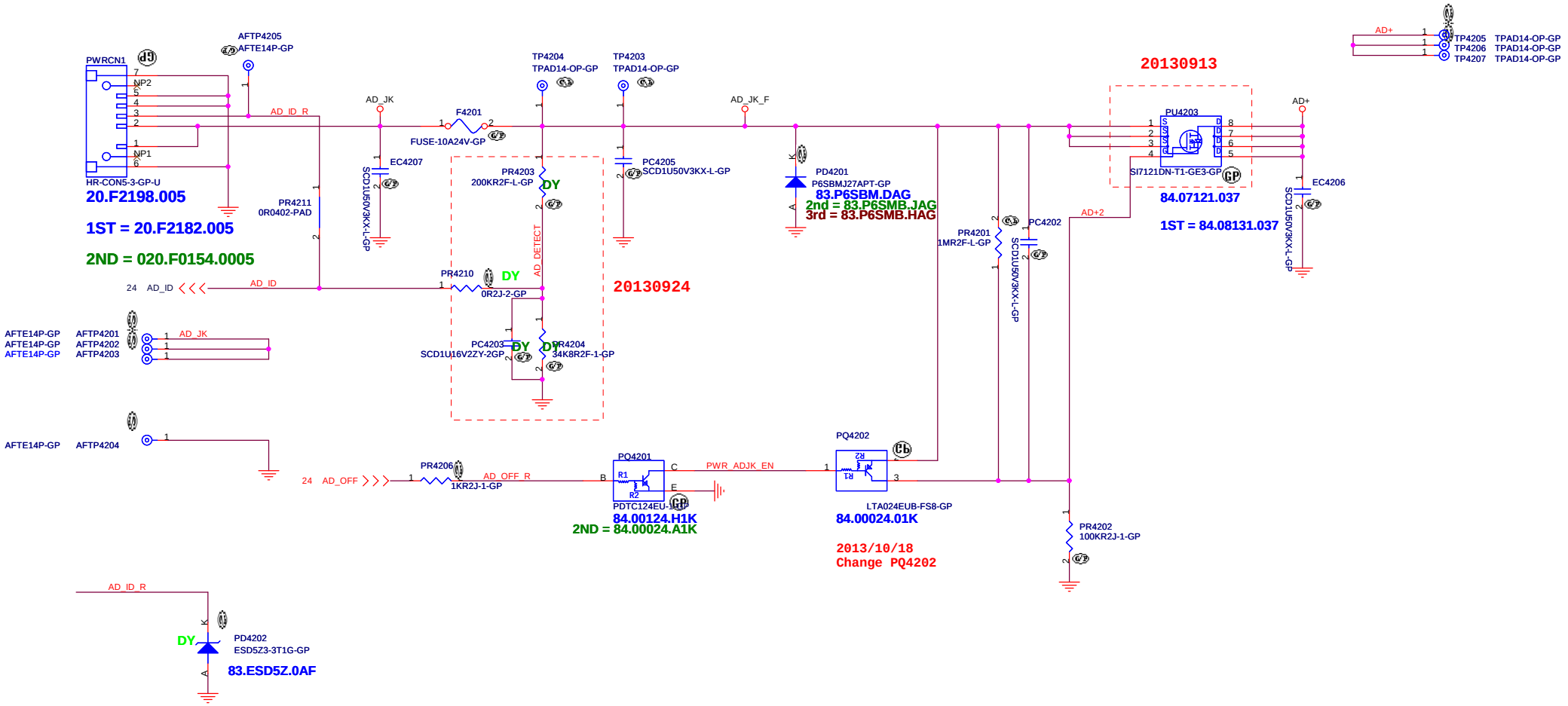
Connected Standby2

Size	Document Number	Rev
A	**LF14M**	**-1**

Date: Wednesday, February 26, 2014 Sheet 41 of 102

DC Jack

Adaptor in to generate DCBATOUT



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<Core Design>

緯創資通 **Wistron Corporation**
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Title	***DCIN JACK***	
Size A3	Document Number **LF14M**	Rev **-1**
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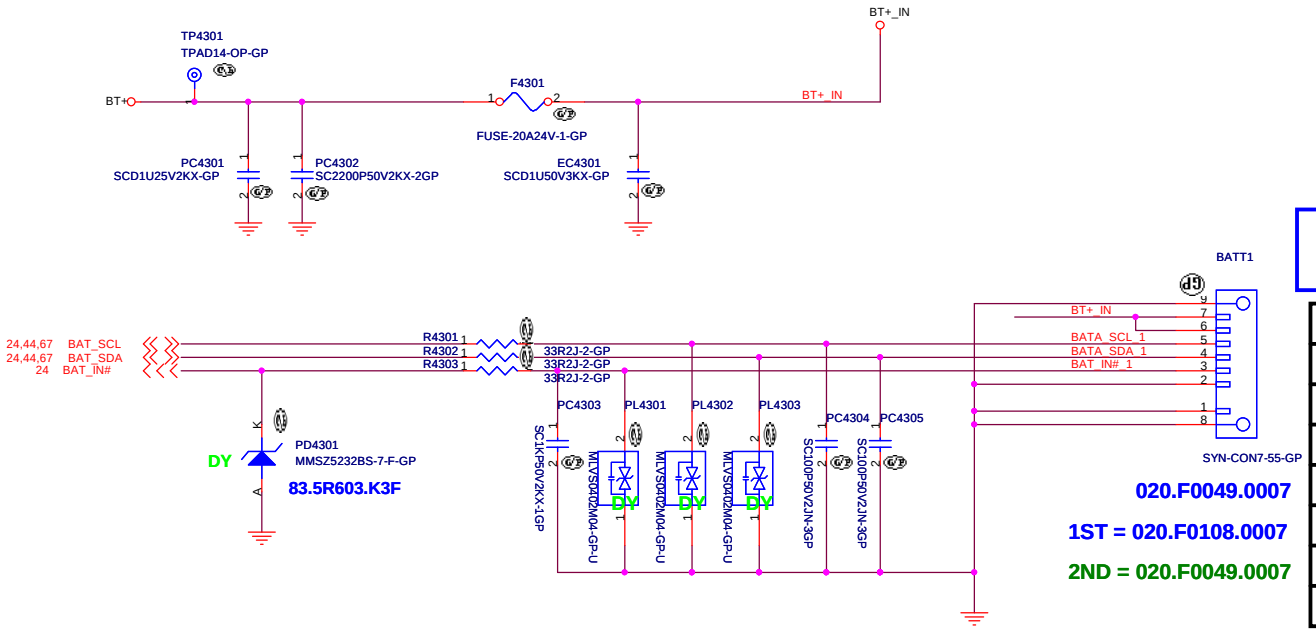
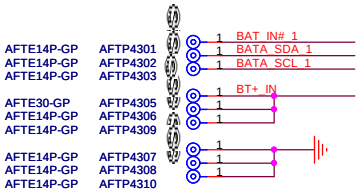
BATTERY CONNECTOR



2013/10/4
Pin Define

Pin#	Comments	Color
1	GND-	BLACK
2	GND-	BLACK
3	ID	WHITE
4	SMD	GREEN
5	SMC	BLUE
6	BATT+	RED
7	BATT+	RED



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Title: BATT CONN
Size: A3
Document Number: LF14M
Rev: -1
Date: Wednesday, February 26, 2014
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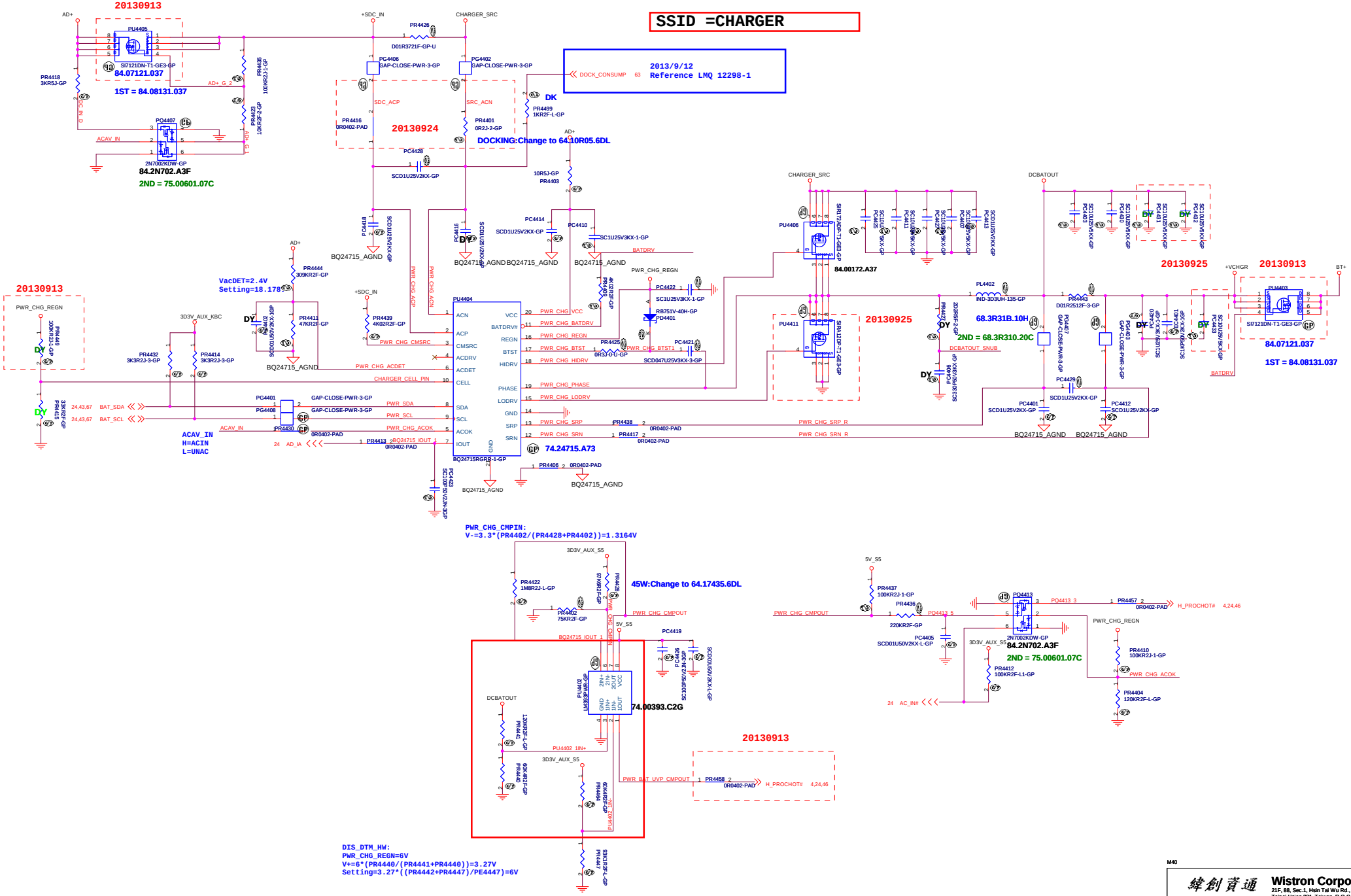
SSID =CHARGER
20130913
2013/9/12
Reference LMQ 12298-1
DOCK_CONSUMP 63
DOCKING:Change to 64.10R05.6DL
20130924
20130925
84.07121.037
1ST = 84.08131.037
84.2N702.A3F
2ND = 75.00601.07C
84.00172.A37
68.3R31B.10H
2ND = 68.3R310.20C
74.24715.A73
74.00393.C2G
VacDET=2.4V
Setting=18.178
ACAV_IN
H=ACIN
L=UNAC
PWR_CHG_CMPIN:
V-=3.3*(PR4402/(PR4428+PR4402))=1.3164V
45W:Change to 64.17435.6DL
DIS_DTM_HW:
PWR_CHG_REGN=6V
V+=6*(PR4440/(PR4441+PR4440))=3.27V
Setting=3.27*((PR4442+PR4447)/PE4447)=6V
BQ24715RGRR-1-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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CHARGER_BQ24715
LF14M
Wednesday, February 26, 2014
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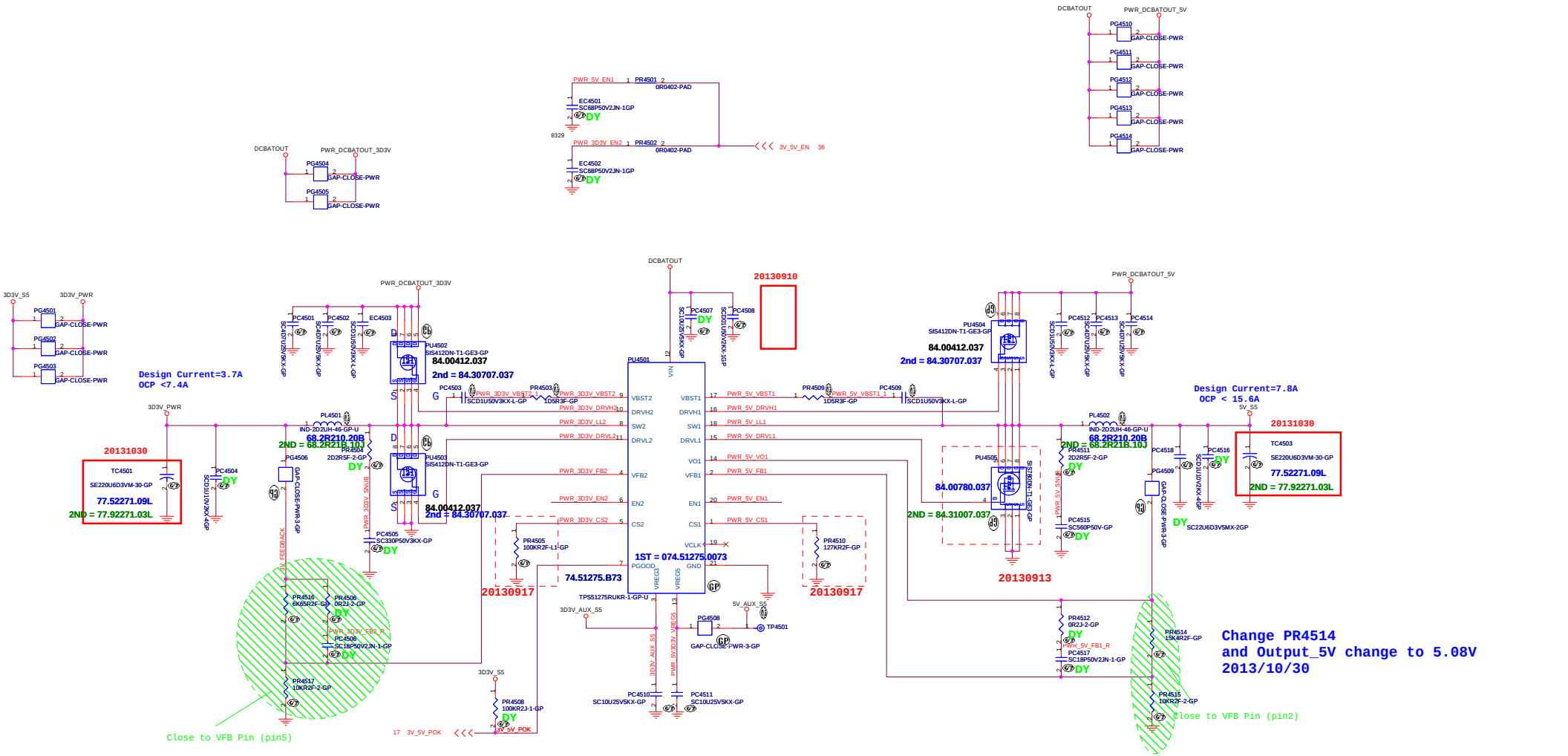

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Title: TPS51225 5V/3D3V

Size: A2 | Document Number: LF14M | Rev: -1

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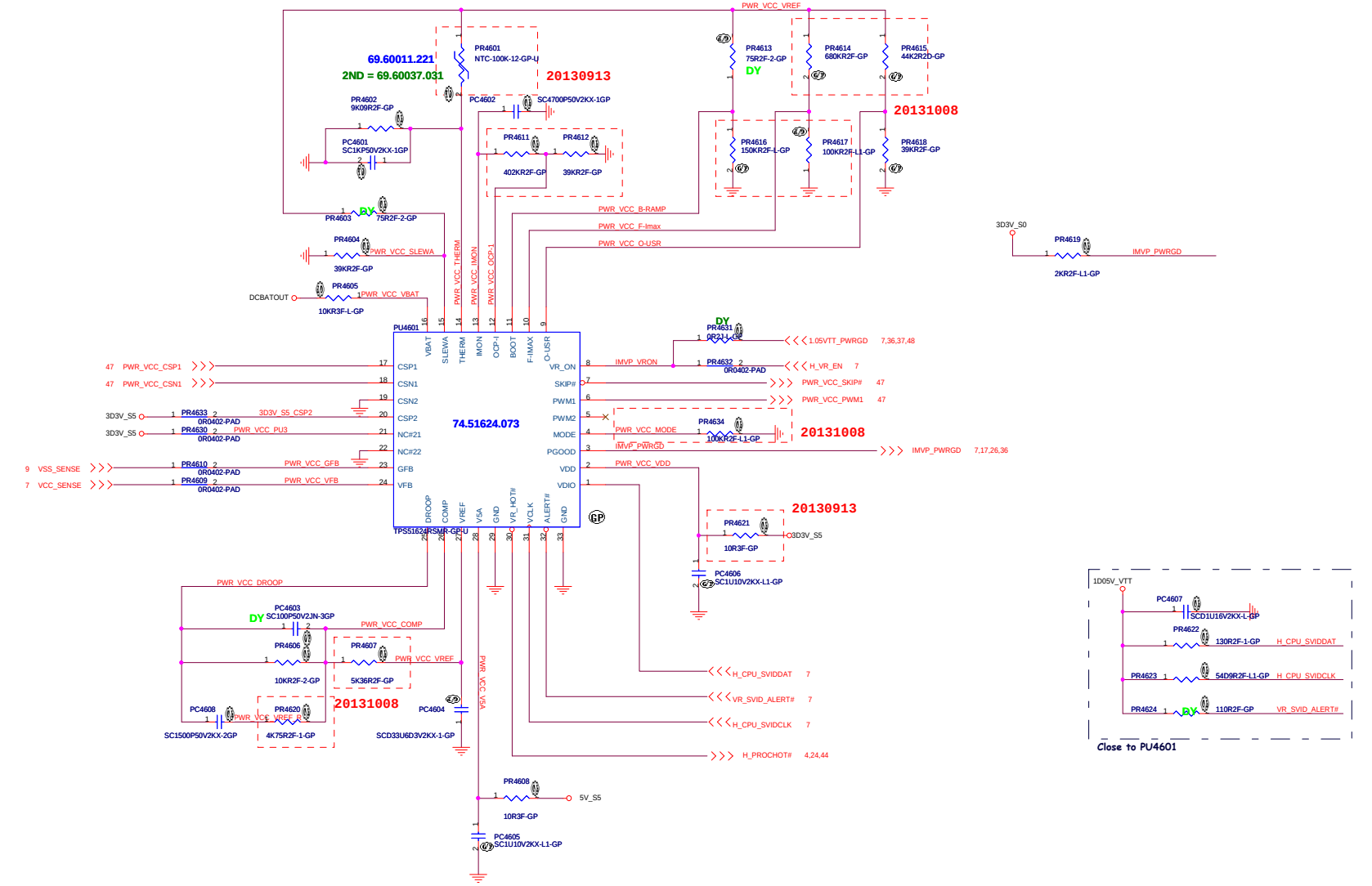
SSID = CPU.Regulator



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Title: TPS51624_CPUCORE(1/2)		
Size: C	Document Number: LF14M	Rev: -1
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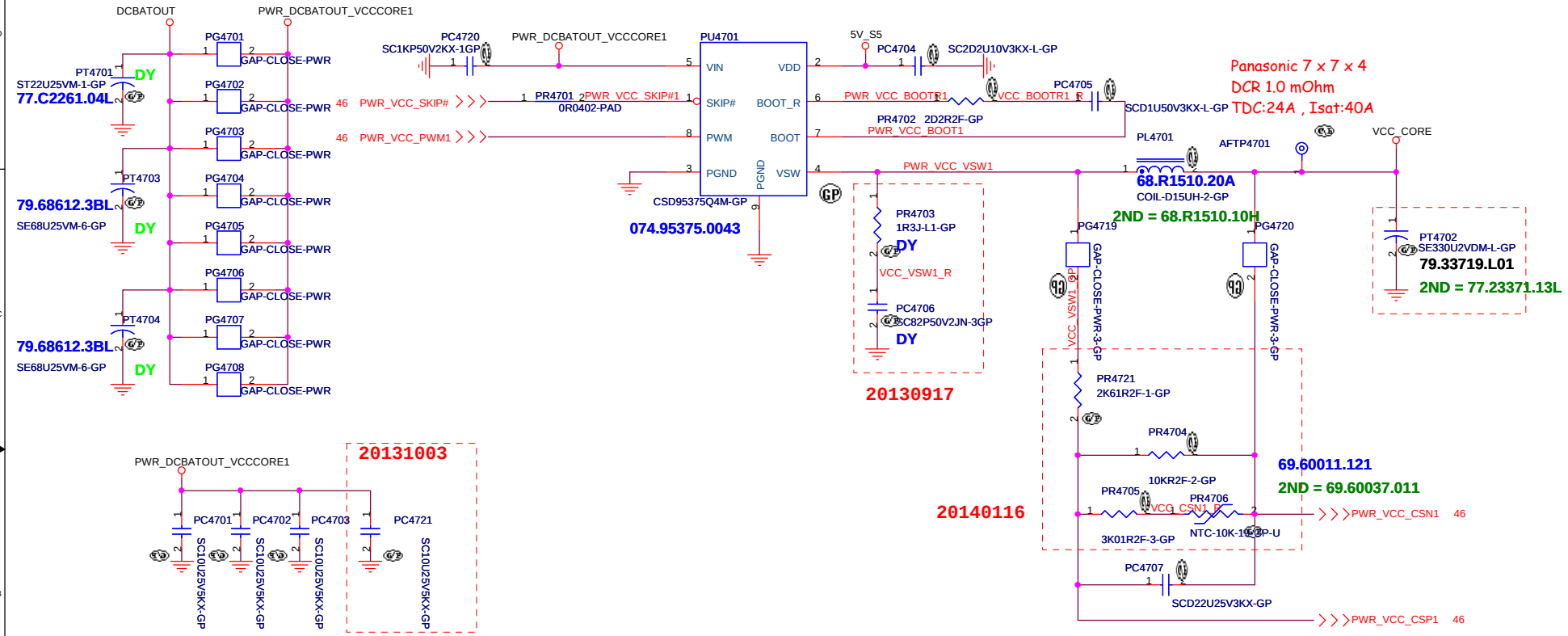

M40

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TPS51624_CPUCORE(2/2)		
Size: B	Document Number: LF14M	Rev: -1
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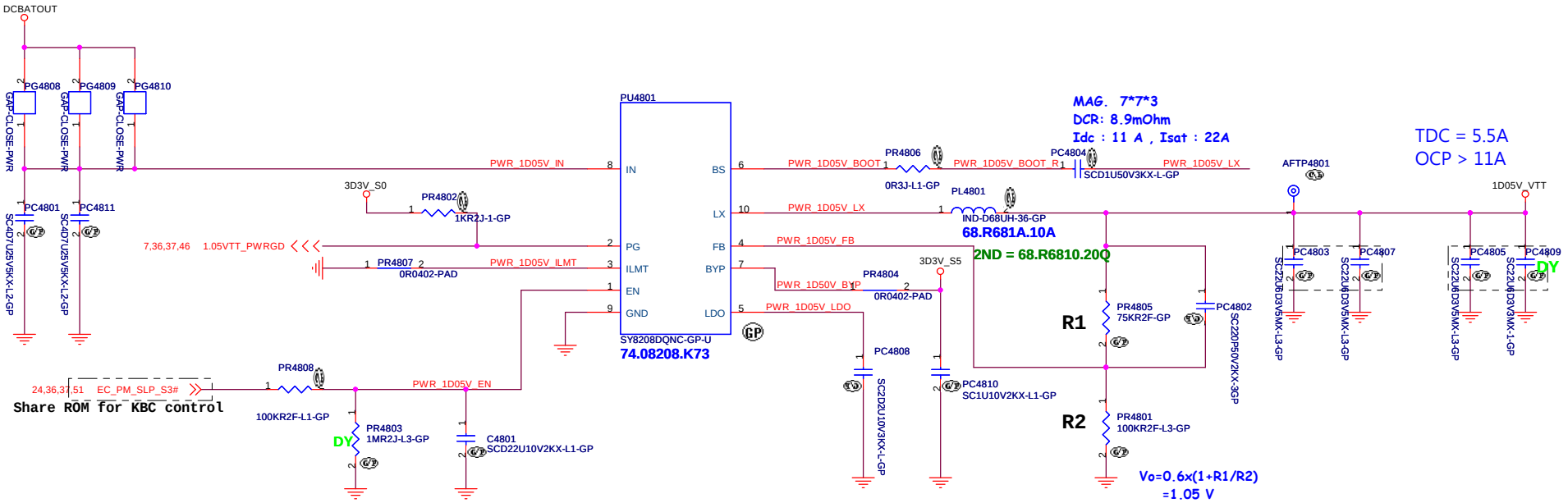
SY8208D for 1D05V



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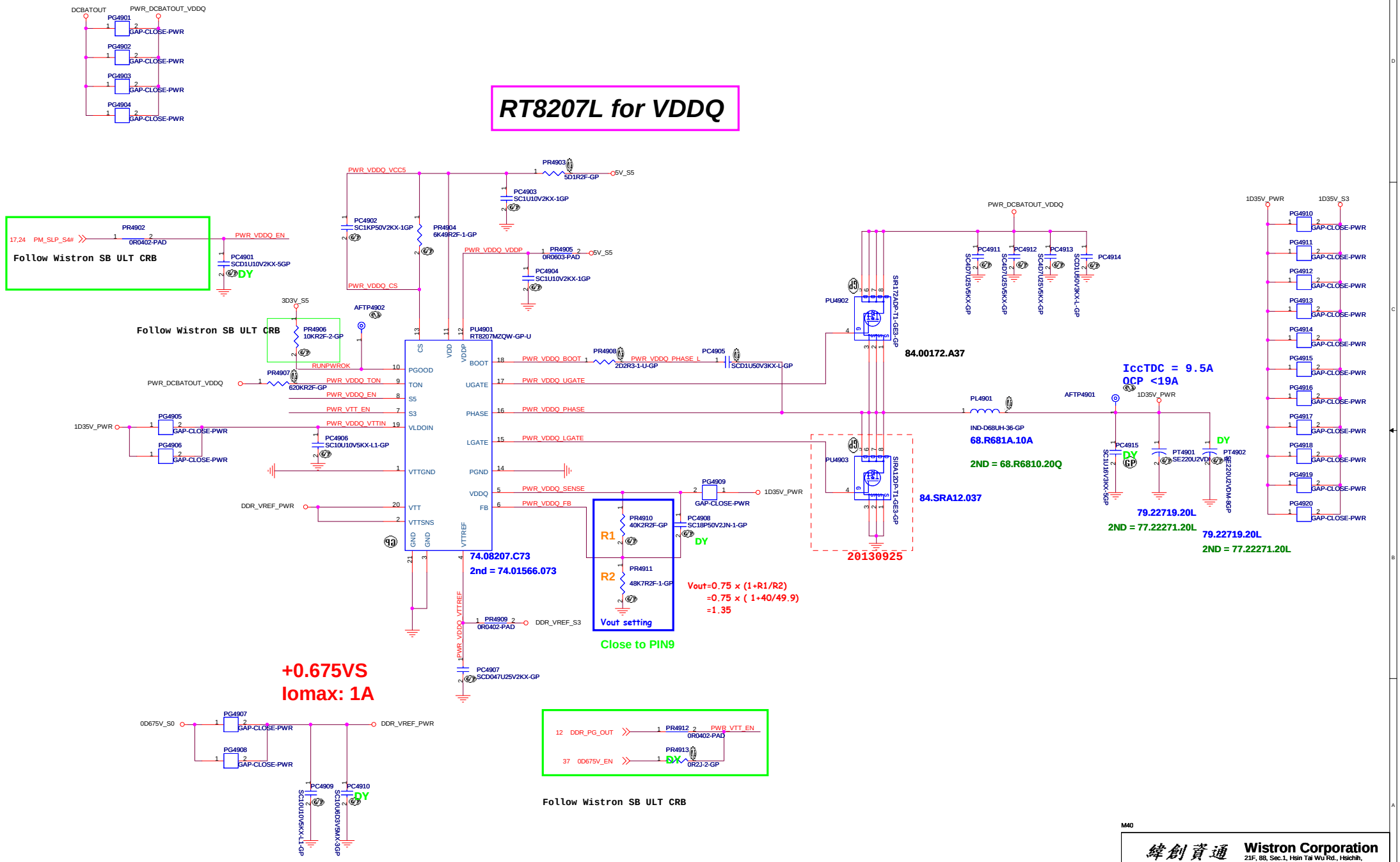
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DC to DC_1D05V(SY8208)	
Size A3	Document Number LF14M	Rev -1
Date: Wednesday, February 26, 2014	Sheet 48 of 102	

SSID = PWR.Plane.Regulator_1p2v0p6v

RT8207L for VDDQ



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緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: RT8207(VDDQ_VTT)		
Size: Custom	Document Number: LF14M	Rev: -1
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Title: ***1D8V_S0***

Size	Document Number	Rev
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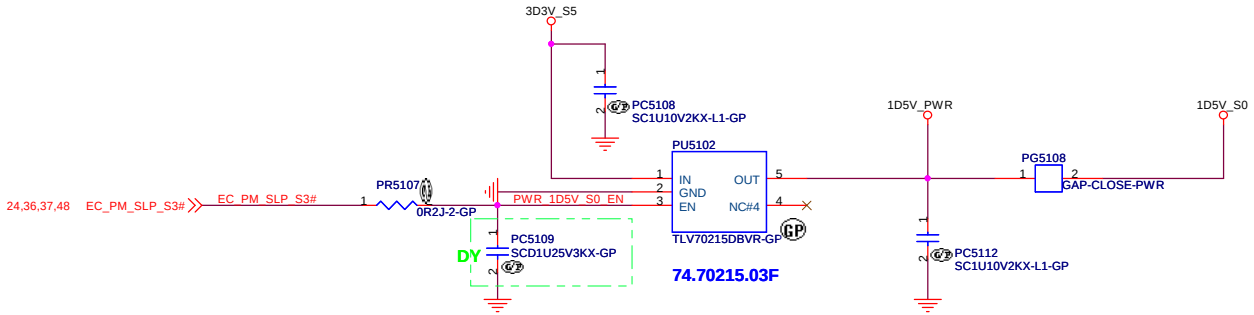
TLV70215 for 1D5V_S0



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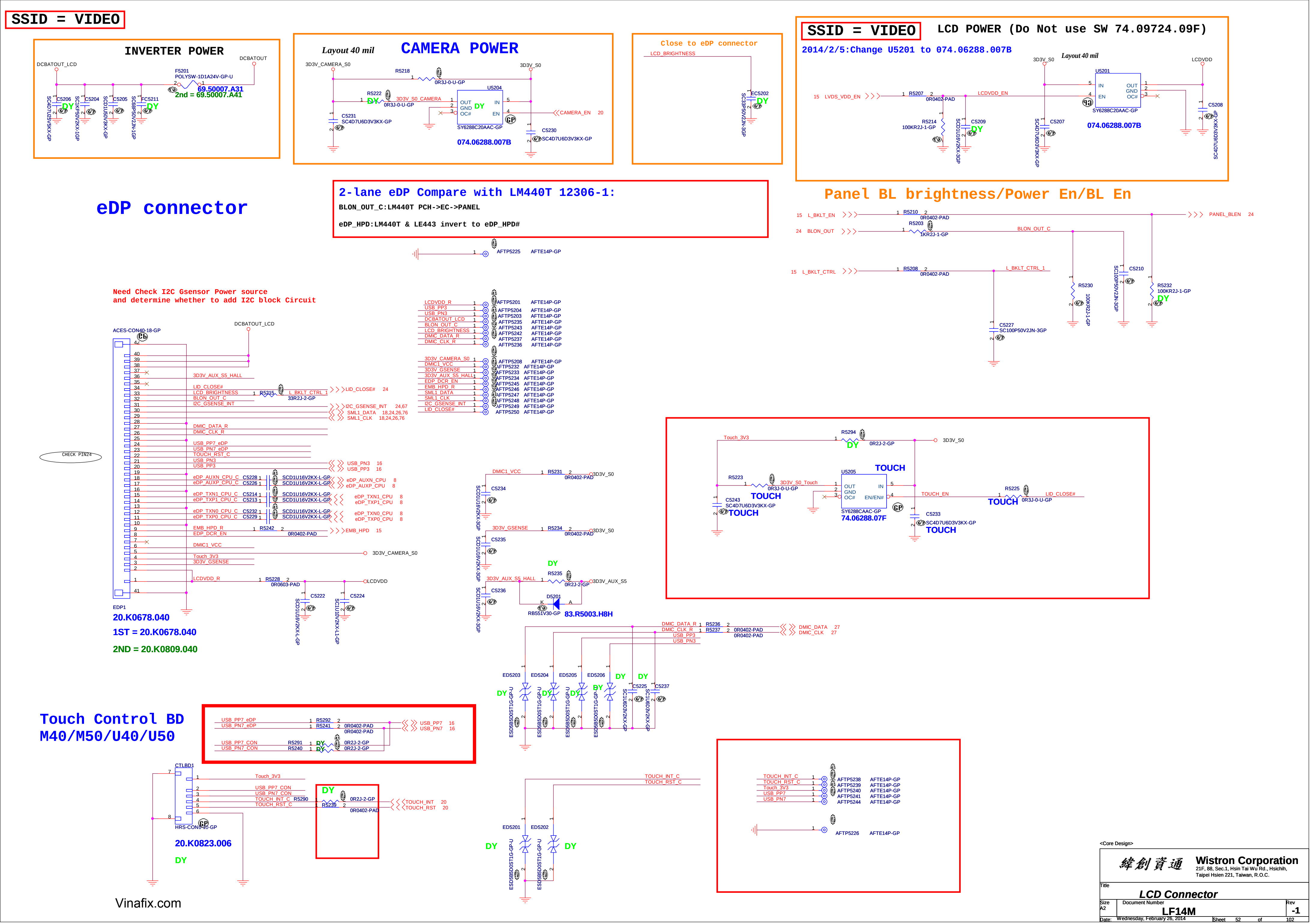
Title: *1D5V_S0 TLV70215*		
Size: A3	Document Number: LF14M	Rev: -1
Date: Wednesday, February 26, 2014	Sheet 51 of 102	



SSID = VIDEO
INVERTER POWER
DCBATOUT_LCD
DCBATOUT
F5201
POLYSW-1D1A24V-GP-U
69.50007.A31
2nd = 69.50007.A41
C5206
C5204
C5205
FC5211
DY
CAMERA POWER
Layout 40 mil
3D3V_CAMERA_S0
3D3V_S0
R5218
0R3J-0-U-GP
R5222
0R3J-0-U-GP
3D3V_S0_CAMERA
U5204
SY6288C20AAC-GP
074.06288.007B
C5231
SC4D7U6D3V3KX-GP
C5230
SC4D7U6D3V3KX-GP
CAMERA_EN 20
Close to eDP connector
LCD_BRIGHTNESS
EC5202
SC33P50V2JN-3GP
SSID = VIDEO
LCD POWER (Do Not use SW 74.09724.09F)
2014/2/5:Change U5201 to 074.06288.007B
Layout 40 mil
3D3V_S0
LCDVDD
U5201
15 LVDS_VDD_EN
R5207
0R0402-PAD
LCDVDD_EN
SY6288C20AAC-GP
074.06288.007B
R5214
100KR2J-1-GP
C5209
C5207
C5208
eDP connector
2-lane eDP Compare with LM440T 12306-1:
BLON_OUT_C:LM440T PCH->EC->PANEL
eDP_HPD:LM440T & LE443 invert to eDP_HPD#
Panel BL brightness/Power En/BL En
15 L_BKLT_EN
R5210
0R0402-PAD
PANEL_BLEN 24
24 BLON_OUT
R5203
1KR2J-1-GP
BLON_OUT_C
15 L_BKLT_CTRL
R5208
0R0402-PAD
L_BKLT_CTRL_1
C5210
R5230
100KR2J-1-GP
R5232
100KR2J-1-GP
C5227
SC100P50V2JN-3GP
AFTP5225 AFTE14P-GP
Need Check I2C Gsensor Power source
and determine whether to add I2C block Circuit
ACES-CON40-18-GP
CHECK PIN24
3D3V_AUX_S5_HALL
LID_CLOSE#
LCD_BRIGHTNESS
BLON_OUT_C
I2C_GSENSE_INT
R5215
33R2J-2-GP
L_BKLT_CTRL_1
LID_CLOSE# 24
I2C_GSENSE_INT 24,67
SML1_DATA 18,24,26,76
SML1_CLK 18,24,26,76
DMIC_DATA_R
DMIC_CLK_R
USB_PP7_eDP
USB_PN7_eDP
TOUCH_RST_C
USB_PN3
USB_PP3
USB_PN3 16
USB_PP3 16
eDP_AUXN_CPU_C
eDP_AUXP_CPU_C
eDP_TXN1_CPU_C
eDP_TXP1_CPU_C
eDP_TXN0_CPU_C
eDP_TXP0_CPU_C
SCD1U16V2KX-L-GP
eDP_AUXN_CPU 8
eDP_AUXP_CPU 8
eDP_TXN1_CPU 8
eDP_TXP1_CPU 8
eDP_TXN0_CPU 8
eDP_TXP0_CPU 8
EMB_HPD_R
EDP_DCR_EN
R5242
0R0402-PAD
EMB_HPD 15
DMIC1_VCC
Touch_3V3
3D3V_GSENSE
3D3V_CAMERA_S0
LCDVDD_R
R5228
0R0603-PAD
LCDVDD
C5222
C5224
EDP1
20.K0678.040
1ST = 20.K0678.040
2ND = 20.K0809.040
AFTP5201 ... AFTP5250 AFTE14P-GP
DMIC1_VCC
R5231
0R0402-PAD
3D3V_S0
C5234
3D3V_GSENSE
R5234
0R0402-PAD
C5235
3D3V_AUX_S5_HALL
R5235
0R2J-2-GP
3D3V_AUX_S5
C5236
D5201
RB551V30-GP
83.R5003.H8H
TOUCH
Touch_3V3
R5294
0R2J-2-GP
3D3V_S0
R5223
0R3J-0-U-GP
3D3V_S0_Touch
U5205
SY6288CAAC-GP
74.06288.07F
TOUCH_EN
R5225
0R3J-0-U-GP
LID_CLOSE#
C5243
SC4D7U6D3V3KX-GP
C5233
SC4D7U6D3V3KX-GP
DMIC_DATA_R
DMIC_CLK_R
R5236
R5237
0R0402-PAD
DMIC_DATA 27
DMIC_CLK 27
ED5203
ED5204
ED5205
ED5206
ESD5B5D0ST1G-GP-U
C5225
C5237
Touch Control BD
M40/M50/U40/U50
USB_PP7_eDP
USB_PN7_eDP
R5292
R5241
0R0402-PAD
USB_PP7 16
USB_PN7 16
USB_PP7_CON
USB_PN7_CON
R5291
R5240
0R2J-2-GP
CTLBD1
Touch_3V3
TOUCH_INT_C
TOUCH_RST_C
R5290
R5239
0R2J-2-GP
0R0402-PAD
TOUCH_INT 20
TOUCH_RST 20
HRS-CON6-46-GP
20.K0823.006
ED5201
ED5202
AFTP5238
AFTP5239
AFTP5240
AFTP5241
AFTP5244
AFTP5226
AFTE14P-GP
Vinafix.com
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
LCD Connector
Size A2
Document Number
LF14M
Rev -1
Date: Wednesday, February 26, 2014
Sheet 52 of 102

M40

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Title

CRT Board Connector

Size	Document Number	Rev
Custom	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 53 of 102

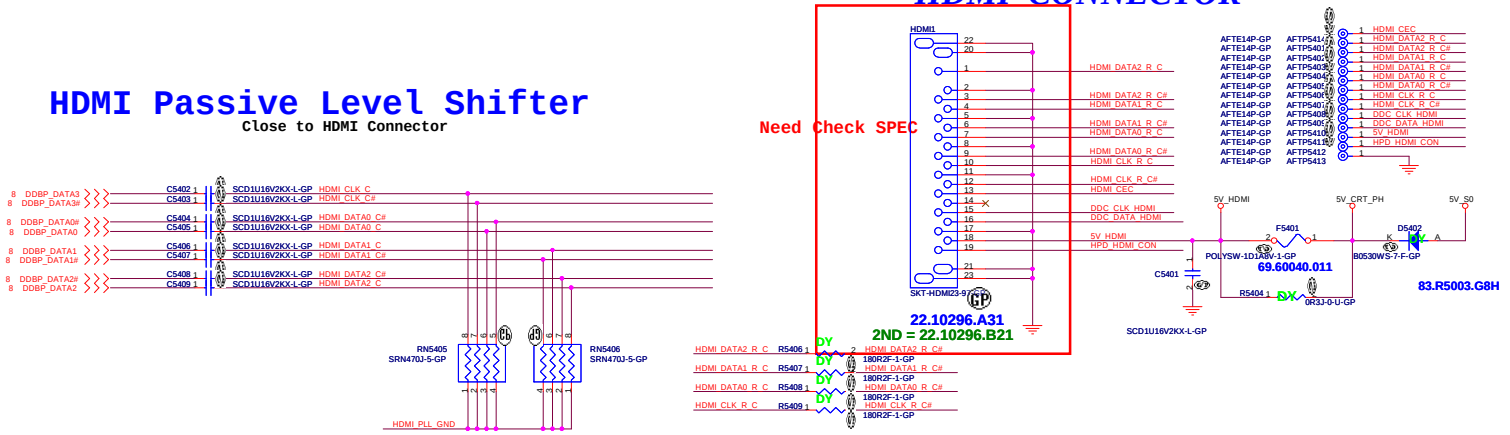
SSID = VIDEO

HDMI CONNECTOR

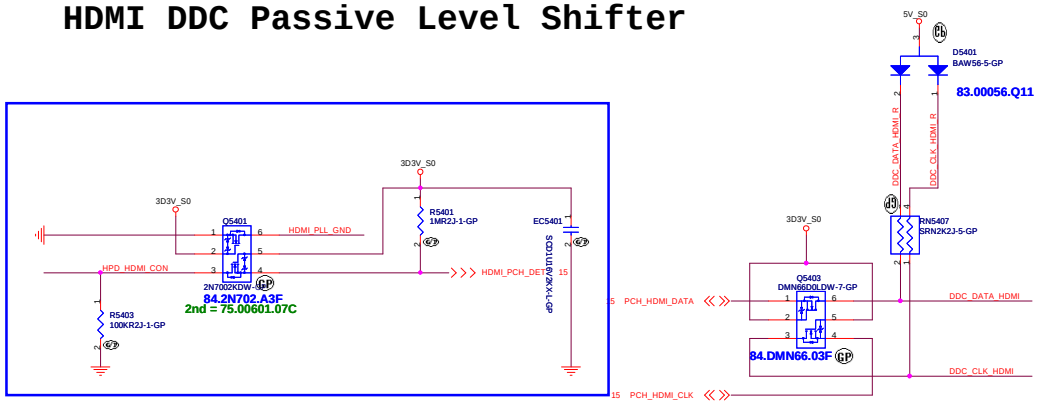
HDMI Passive Level Shifter

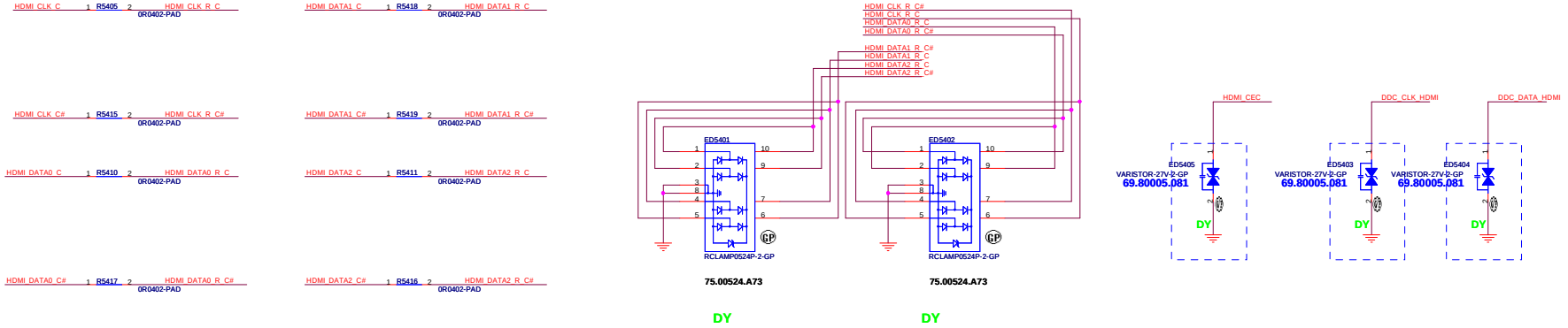
Close to HDMI Connector

Need Check SPEC



HDMI DDC Passive Level Shifter





DY

DY

Vinafix.com

<Core Design>

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size: A2 | Document Number: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet 54 of 102

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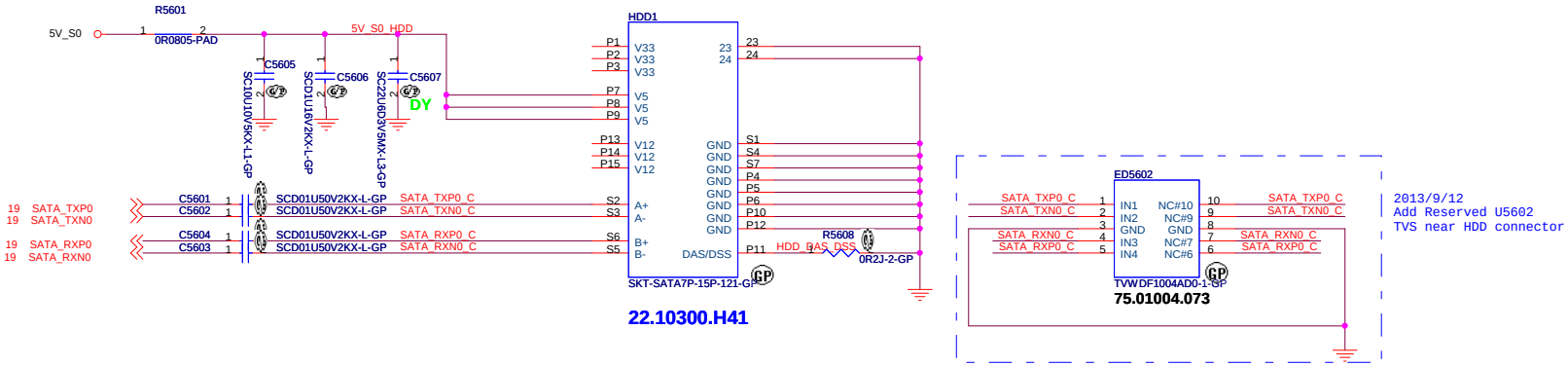
Title: ***TRAVIS***

Size	Document Number	Rev
A2	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 55 of 102

SSID = SATA

SATA HDD Connector



ODD Connector

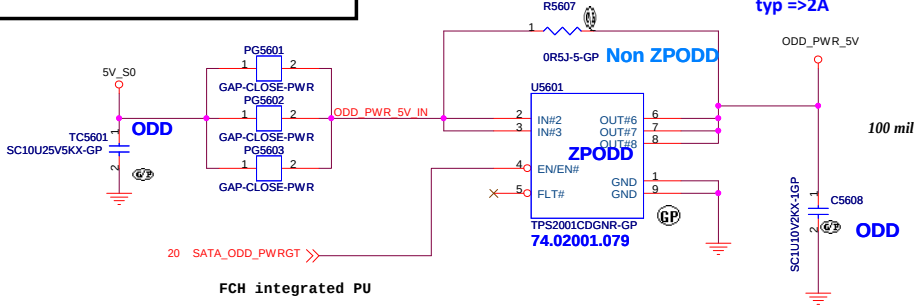
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.

Need Check 2spindle series & Components

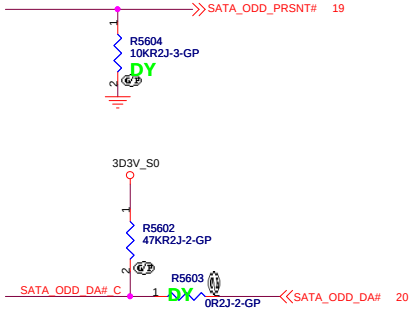
SATA Zero Power ODD

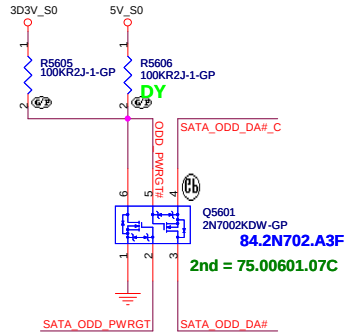
Current limit
Active High
typ =>2A



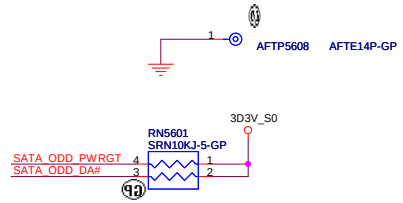
Follow Intel Zero Power ODD SPEC

ODD (M50/U50)

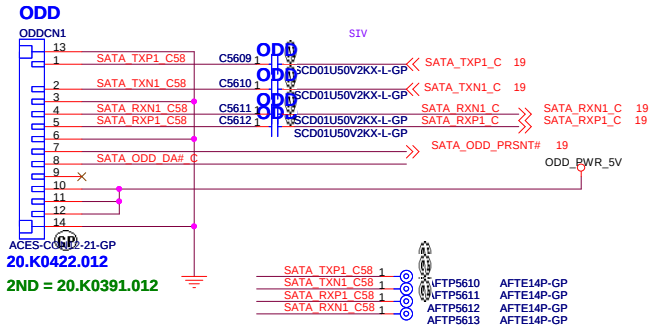




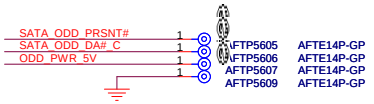
Vinafix.com



SUPPORT ZERO SATA ODD



原TC5602,TC5603,FC5604移動到小板



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD / ODD / NGFF_SSD

Size: Custom | Document Number: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet 56 of 102

M40

緯創資通

Wistron Corporation
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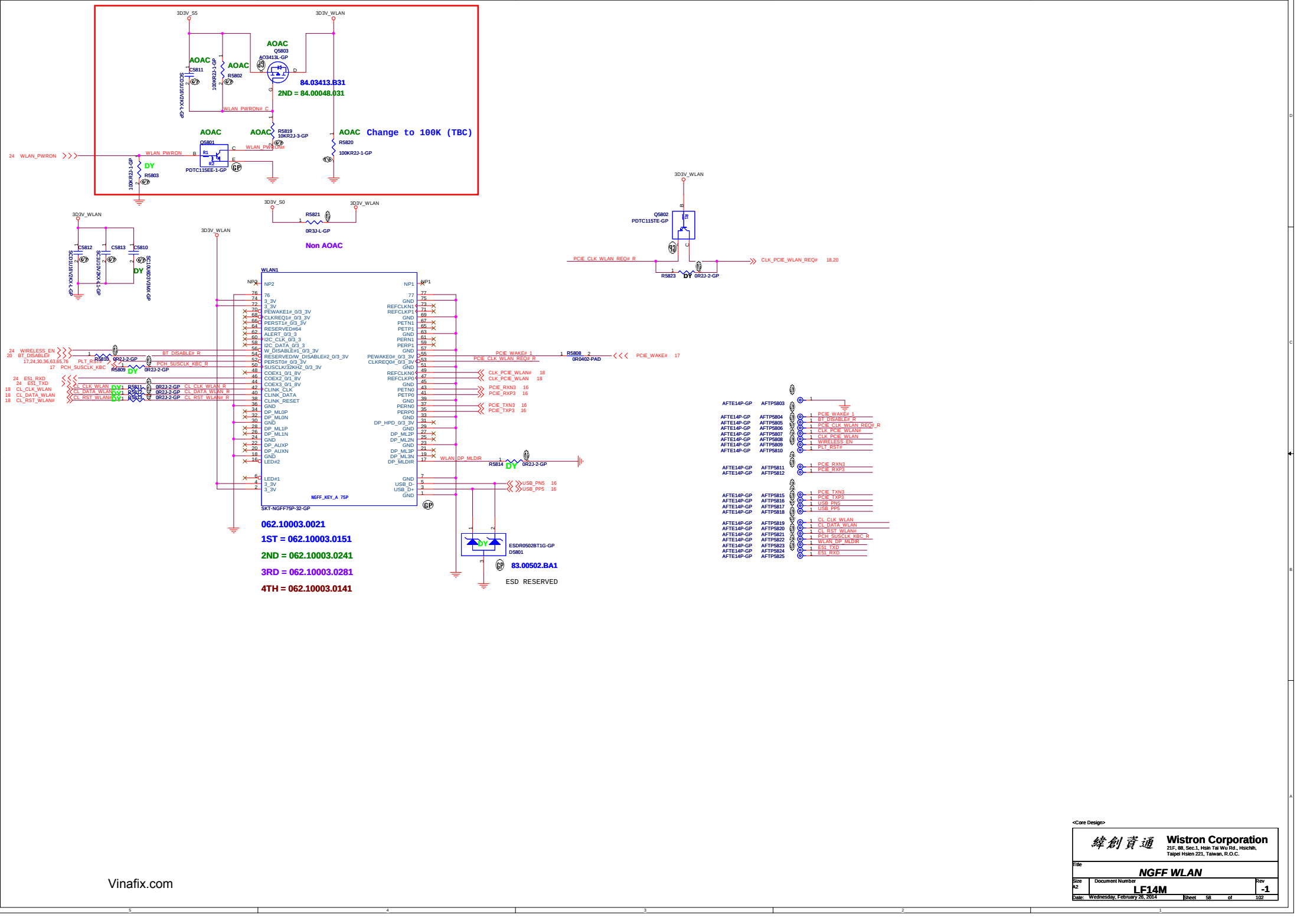
Title

E-SATA

Size	Document Number	Rev
A4	**LF14M**	**-1**

Date: Wednesday, February 26, 2014 Sheet 57 of 102


3D3V_S5
3D3V_WLAN
AOAC
Q5803
AO3413L-GP
84.03413.B31
2ND = 84.00048.031
WLAN_PWRON# C
R5819
10KR2J-3-GP
R5820
100KR2J-1-GP
Change to 100K (TBC)
Q5801
PDTC115EE-1-GP
24 WLAN_PWRON
WLAN_PWRON
R5803
3D3V_S0
R5821
0R3J-L-GP
Non AOAC
WLAN1
SKT-NGFF75P-32-GP
NGFF_KEY_A 75P
062.10003.0021
1ST = 062.10003.0151
2ND = 062.10003.0241
3RD = 062.10003.0281
4TH = 062.10003.0141
Q5802
PDTC115TE-GP
PCIE_CLK_WLAN_REQ# R
CLK_PCIE_WLAN_REQ#
R5823
0R2J-2-GP
R5808
0R0402-PAD
PCIE_WAKE#
ESDR0502BT1G-GP
D5801
83.00502.BA1
ESD RESERVED
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
NGFF WLAN
LF14M
-1
Wednesday, February 26, 2014
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102

SSID = Wireless

M40

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Title: *NGFF_SATA*		
Size: A3	Document Number: LF14M	Rev: -1
Date: Wednesday, February 26, 2014	Sheet 59 of 102	

SSID = mSATA

Mini Card Connector(mSATA)

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M40

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Title: *mSATA Connector*		
Size: A4	Document Number: LF14M	Rev: -1
Date: Wednesday, February 26, 2014	Sheet 60 of 102	

M40

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

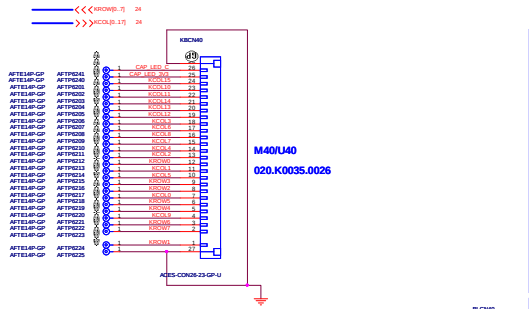
LED Bard/Power Button

Size	Document Number	Rev
A3	**LF14M**	**-1**

Date: Wednesday, February 26, 2014 Sheet 61 of 102

SSID = KBC

Internal KeyBoard Connector

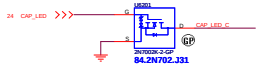


Check Date:2013/9/15

14" (Ref. Chicony G40 BL KB CCY 2D 0905 X7)

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2	25	26
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8	VCC	Caps

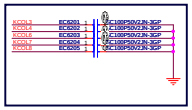
CAP LED:all series



84.2N702.J31

2ND = 84.2N702.031

3RD = 84.2N702.W31



For EMC Recommend

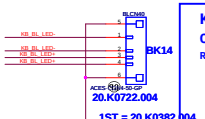
AFTP6201~AFTP6225

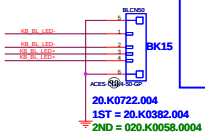
CLOSE keyboard connector

Keyboard Backlight CN

Check Date:2013/9/15

Ref. Chicony G40 BL KB CCY 2D 0905 X7



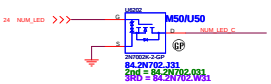


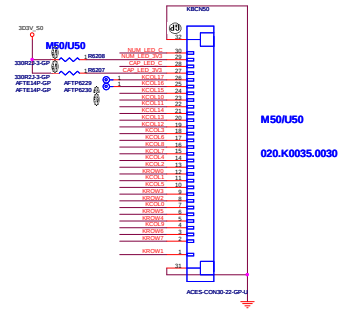
Check Date:2013/9/15

15" (Ref. Chicony G50 NBL KB CCY 2D 0904 X8)

Membrane PIN Out Top View

Pin #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	25	26	12	1	8	9	5	6	3	2
AS-sign	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	S1	S2	S3	S4	S5	S6	S7	S8





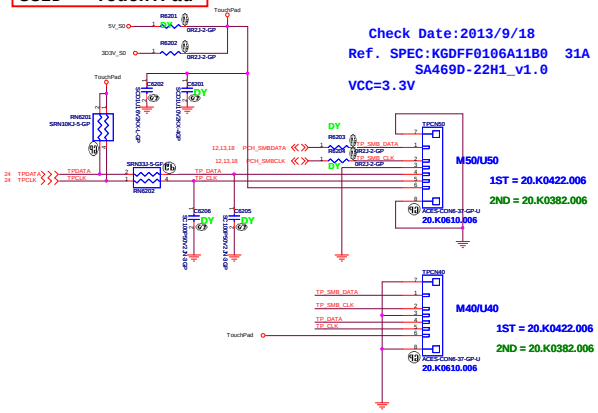
SSID = Touch.Pad

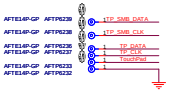
Check Date:2013/9/18

Ref. SPEC:KGDFF0106A11B0 31A

SA469D-22H1_v1.0

VCC=3.3V





M40

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Title: Key Board/Touch Pad

Size: A1 | Document Number: LF14M | Rev: -1

Date: Wednesday, February 26, 2014 | Sheet 62 of 102

USB 2.0 port2/4 Power SW

U6301 place near to IOCN1 **add 47uF input/output**

at least 80 mil

High Enable

74.02064.B79

IO BD M40/U40/M50/U50

2014/2/6
USB_PP0/PN0改接到USB2.0 Port 1
NET維持不變

Reserved for USB2.0 Card Reader (DY)

USB3.0 CARD READER

USB2.0 PORT4

USB2.0 PORT2

Change P/N
2013/11/1

84.00024.01M

Change IOCN1 P/N
Need Check Pin Define with Small BD
2013/10/30

主板Pin定義不動
只動小板
小板CN端只接所需PIN
其餘NC

20.K0678.044

1ST = 20.K0678.044
2ND = 20.K0809.044

2014/2/12 Add for GL3213 Card Reader
If PCIE Card Reader is stuff,then dummy R6317
U40/U50 only

Volume BD M50/U50

+ PH 3d3v_s0

2014/2/7
SPEC變更為取消音量鍵

主板Pin定義不動
只動小板
小板CN端只接所需PIN
其餘NC

20.K0397.004

DOCKING BD M50 only

Modified 10/5

AC CAP IN SMALL BD

20.K0848.030

2ND = 20.K0809.030

Figure 14-2. USB 3.0 Docking Topology Overview

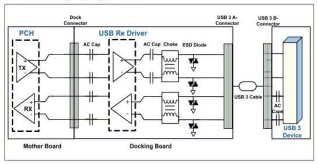
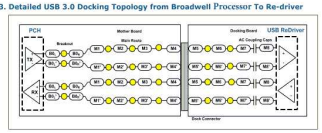


Figure 14-3. Detailed USB 3.0 Docking Topology from Broadwell Processor To Re-driver



BTN BD U50 only

Check with small BD 9/25

20.K0529.008

2ND = 20.K0481.008

Novo Button M40/U40

M40/U40 Novo Button

69.80007.021

062.40001.0141

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: IO Board Connector
Size: A1 | Document Number: LF14M | Rev: -1
Date: Wednesday, February 26, 2014 | Sheet 63 of 102

M40

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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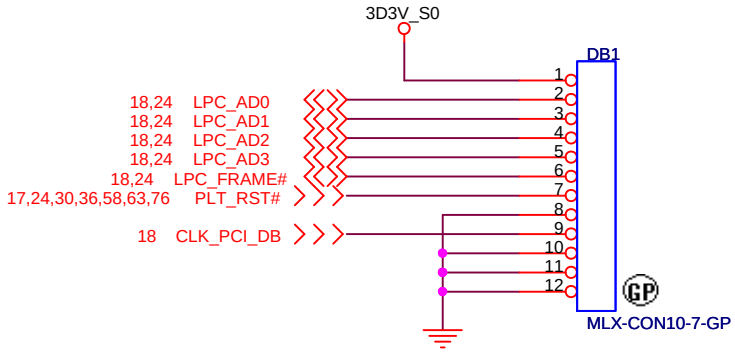
Title

Hall Sensor

Size	Document Number	Rev
A4	**LF14M**	**-1**

Date: Wednesday, February 26, 2014 Sheet 64 of 102

Debug Connector



20.D0183.110

DB Change to 20.F0714.010

M40

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Debug connector***

Size	Document Number	Rev
A4	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 65 of 102

(Blanking)

M40

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SENSOR HUB***	
Size A3	Document Number **LF14M**	Rev **-1**
Date: Wednesday, February 26, 2014	Sheet 66 of 102	

Free Fall Sensor

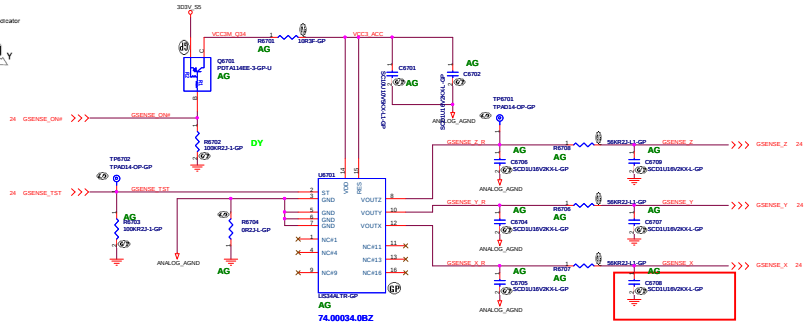
Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Need Stuff

Analog G-Sensor

SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"



74.00034.0BZ
1ST = 74.00034.0BZ
2ND = 74.KXTC8.0BZ

STMicro LIS34AL: 74.00034.0BZ
2nd = 74.KXTC8.0BZ

Layout Comment :

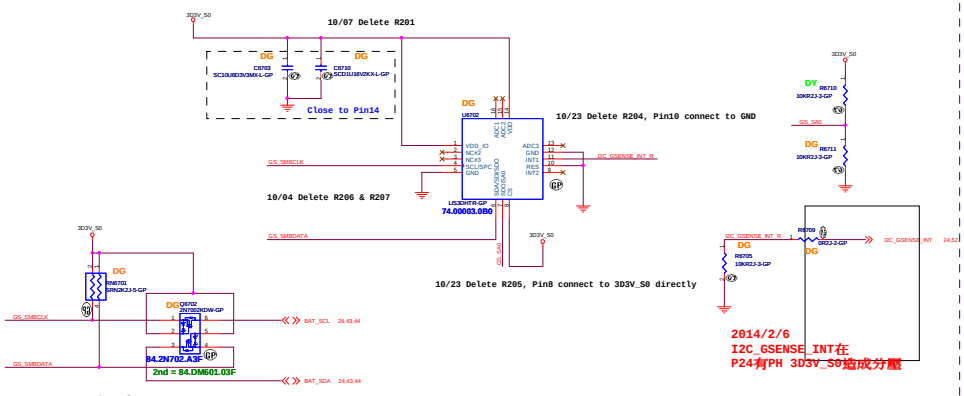
(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.

If Analog Gsensor Not USE Please Change C6708 to 10K ohm

SC _Digital_G-sensor

The Slave ADdress (SAD) associated to the LIS3DH is 001100xb. SDO/SA0 pad can be used to modify less significant bit of the device address. If SA0 pad is connected to voltage supply, LSb is '1' (address 0011001b) else if SA0 pad is connected to ground, LSb value is '0' (address 0011000b). This solution permits to connect and address two different accelerometers to the same I2C lines.



2014/2/6
I2C_GSENSE_INT在P24有PH 3D3V_S0造成分壓

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Title: G Sensor		
Size: A1	Document Number: LF14M	Rev: -1
Date: Wednesday, February 26, 2014	Sheet 67 of 102	

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緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Thunderbolt (1/5)

Size	Document Number	Rev
Custom	**LF14M**	**-1**

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M40

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Title

Thunderbolt (2/5)

Size	Document Number	Rev
Custom	**LF14M**	**-1**

Date: Wednesday, February 26, 2014 Sheet 69 of 102

M40

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Title: ***Thunderbolt (3/5)***

Size	Document Number	Rev
Custom	LF14M	-1

Date: Wednesday, February 26, 2014 Sheet 70 of 102

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Title: ***Thunderbolt (4/5)***

Size	Document Number	Rev
Custom	**LF14M**	**-1**

Date: Wednesday, February 26, 2014 Sheet 71 of 102

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緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt (5/5)

Size	Document Number	Rev
A4	**LF14M**	**-1**

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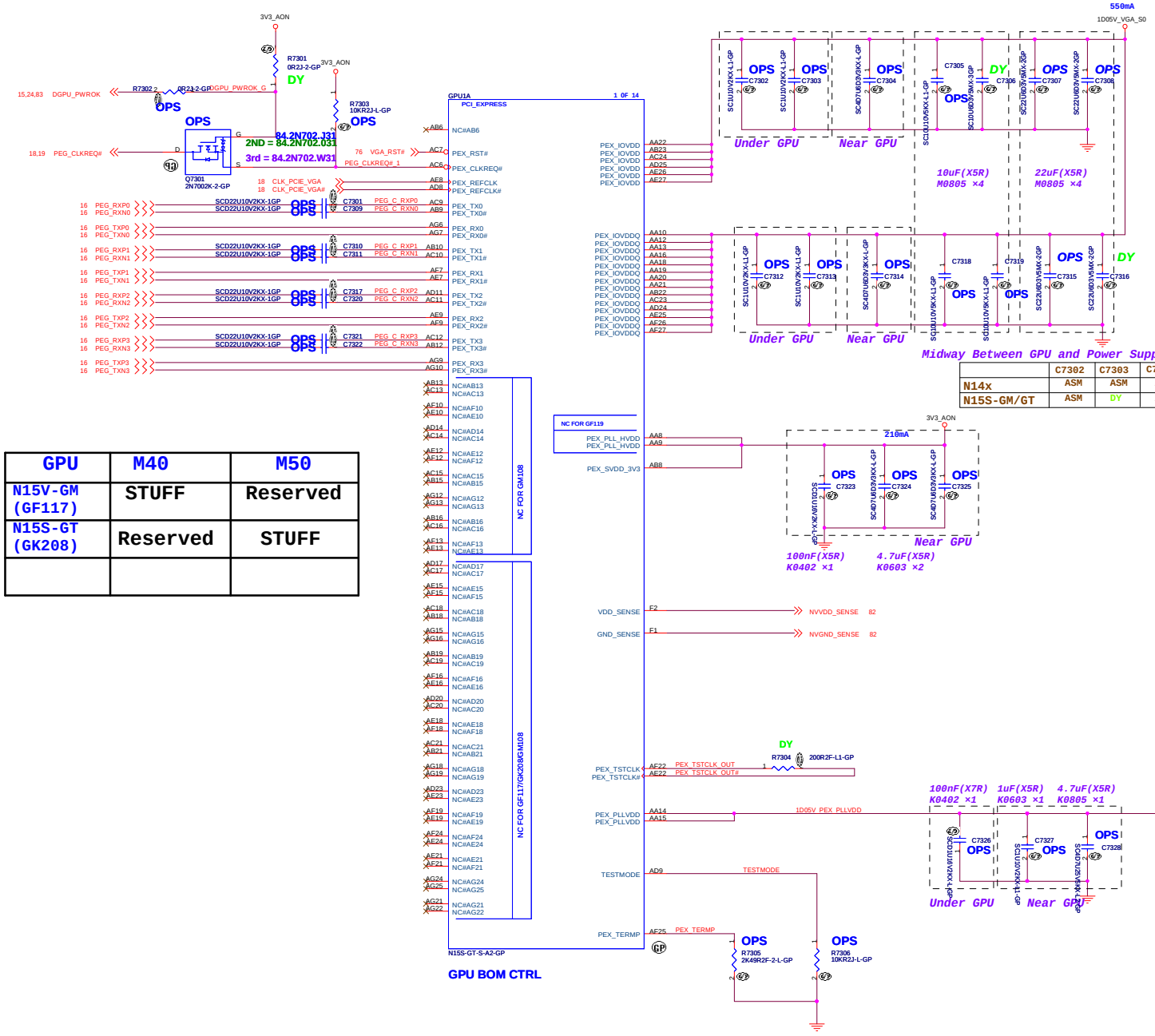

GPU	M40	M50
N15V-GM (GF117)	STUFF	Reserved
N15S-GT (GK208)	Reserved	STUFF

Table 3. PEX_IOVDD/Q Decoupling

Capacitor Type			Typical N14x Population	N15V-GM Population	N15S-GV Population	N15S-GM/-GT Population	Location
1uUF	X6S	0402	4	4	4	1	Under GPU
4.7uF	X6S	0603	2	2	2	1	Under GPU
10uF	X5R	0805	4	4	4	1	Near GPU
22uF	X5R	0805	4	4	4	1	Near GPU

	C7302	C7303	C7304	C7305	C7306	C7307	C7308	C7312	C7313	C7314	C7318	C7319	C7315	C7316
N14x	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM
N15S-GM/GT	ASM	DY	ASM	ASM	DY	ASM	DY	DY	DY	DY	DY	DY	DY	DY

M40

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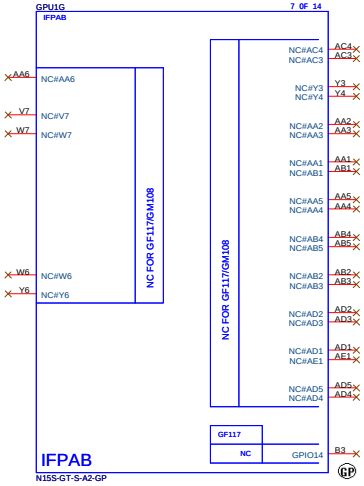
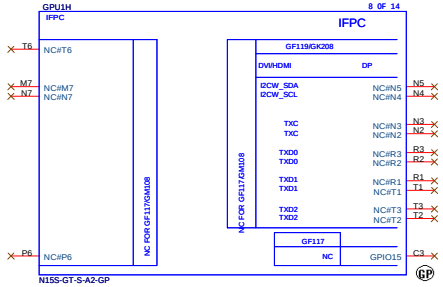
Title: GPU(PEG)

Size: A2 | Document Number: LF14M | Rev: -1

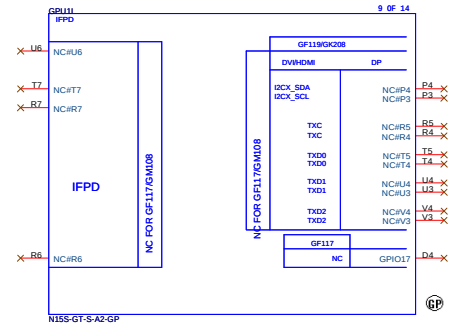
Date: Wednesday, February 26, 2014 | Sheet 73 of 102



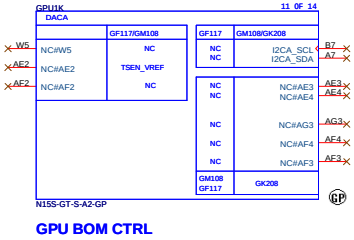
GPU BOM CTRL



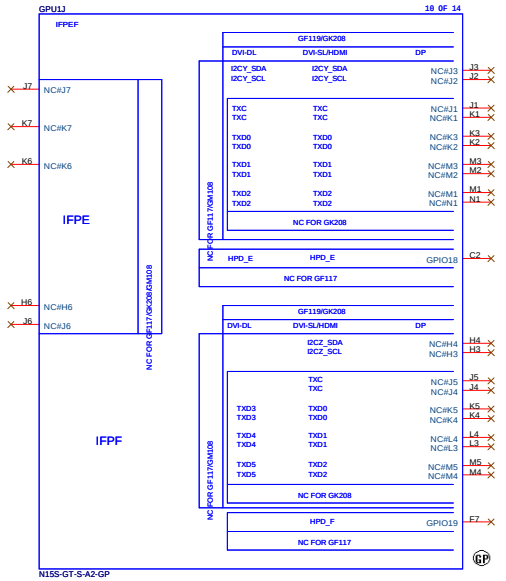
GPU BOM CTRL



GPU BOM CTRL



GPU BOM CTRL



GPU BOM CTRL

M40

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Title: GPU (DIGITALOUT)

Size	Document Number	Rev
A2	LF14M	-1

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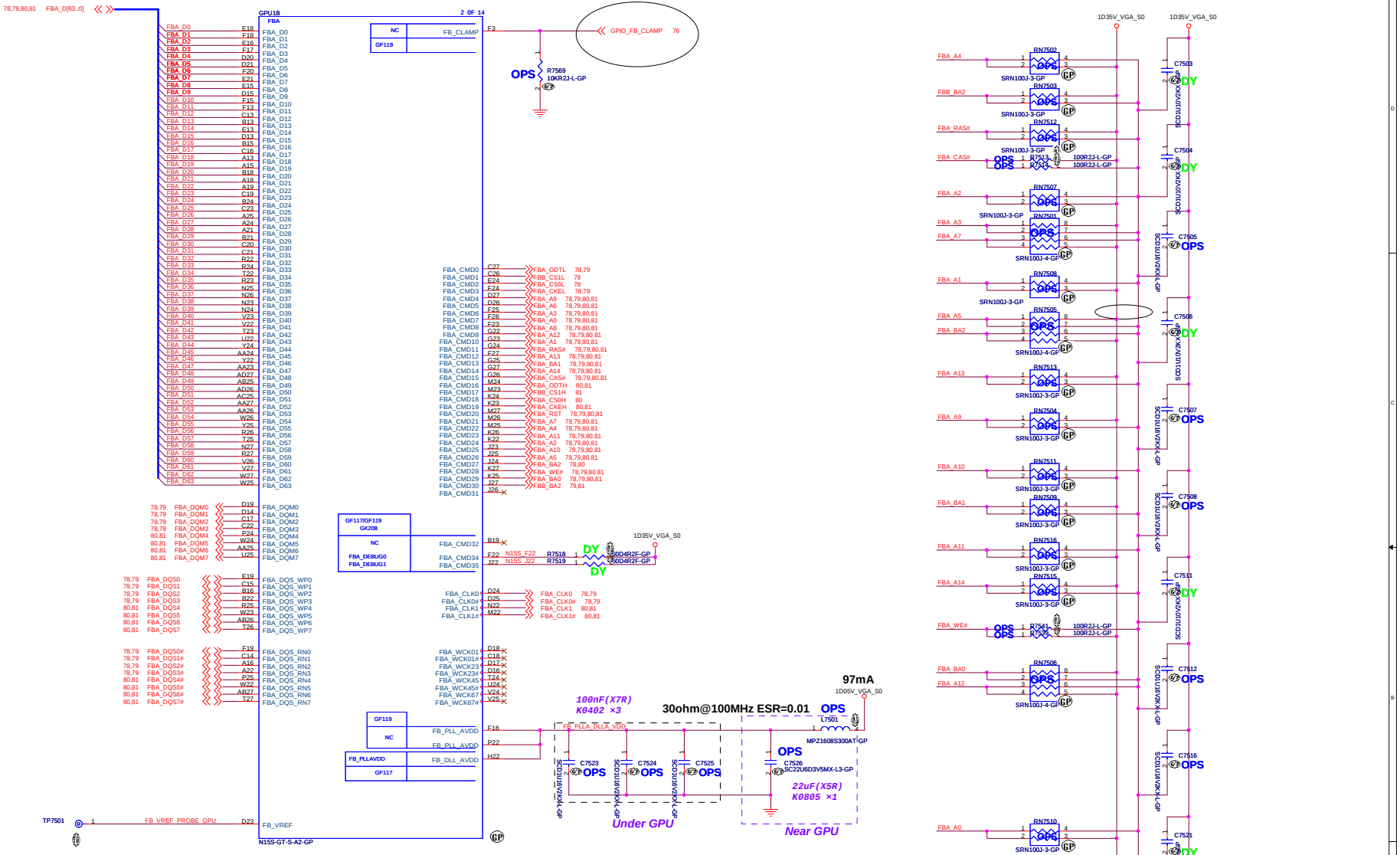
check "EC_FB_CLAMP" is original name



Vinafix.com

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (VRAM I/F)

Size	Document Number	Rev
Custom	LF14M	-1

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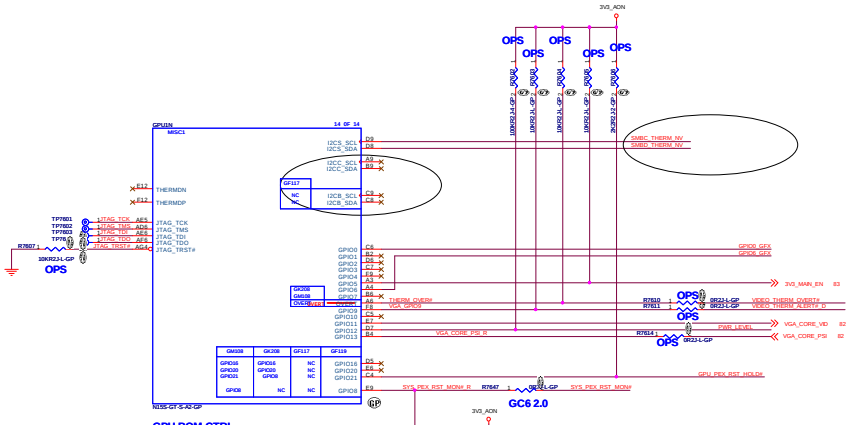

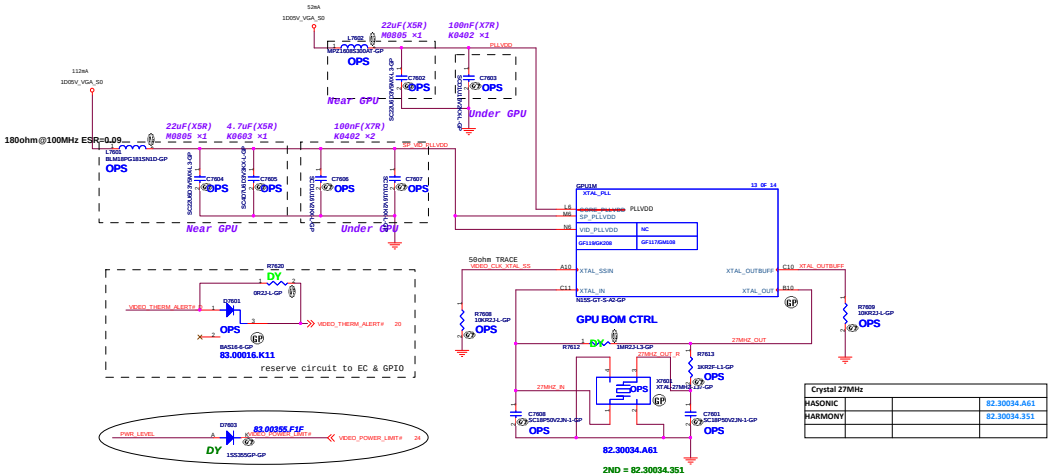

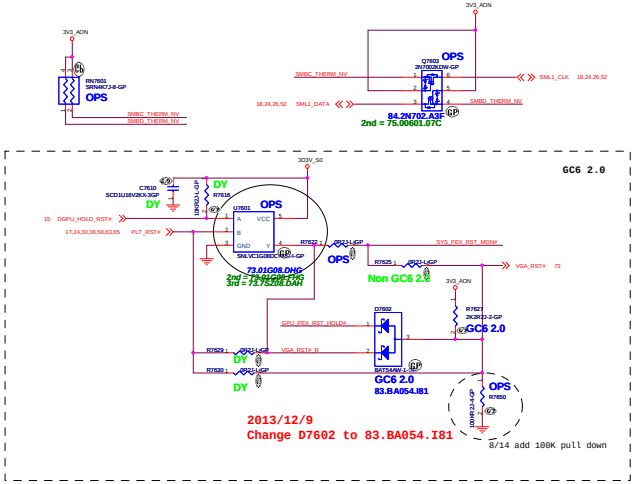

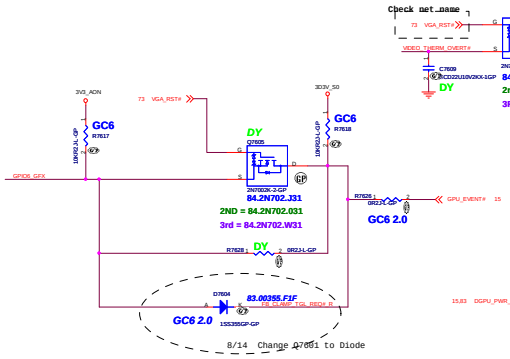

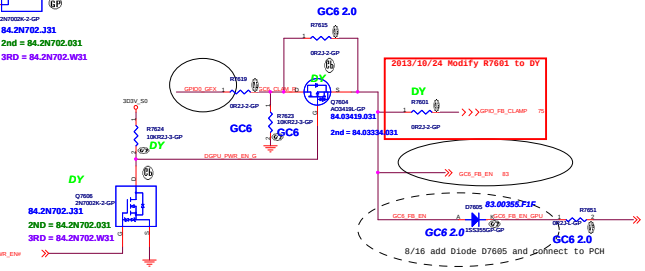

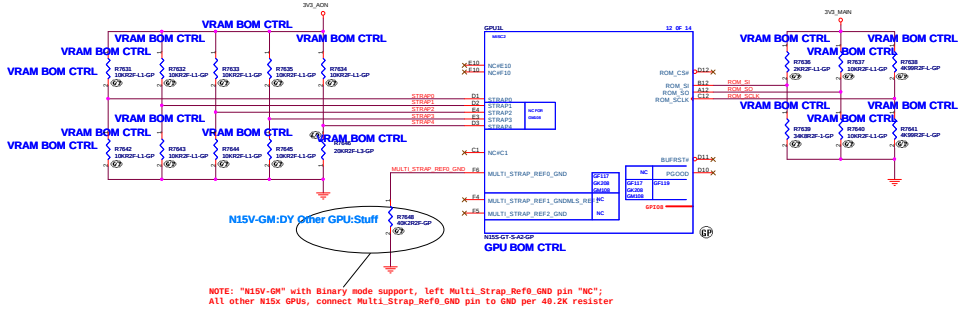

1D35V Compatible VRAM P/N List			
Vendor	Vendor P/N	Lenovo P/N	Size
Samsung	K4W2G1646E-BY11		256MB
Samsung	K4W2G1646Q-BC1A	1101028	256MB
Samsung	K4W4G1646D-BC1A	1101019	512MB
Hynix	H5TC2G63FFR-11C	1100788	256MB
Hynix	H5TC4G63AFR-11C	1100897	512MB
Micron	MT41K128M16JT-107G:K	1101057	256MB
Micron	MT41K256M16HA-107G:E	1100677	512MB

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Title: GPU (GPIO/STRAP)
Size: Custom | Document Number: LF14M | Rev: -1
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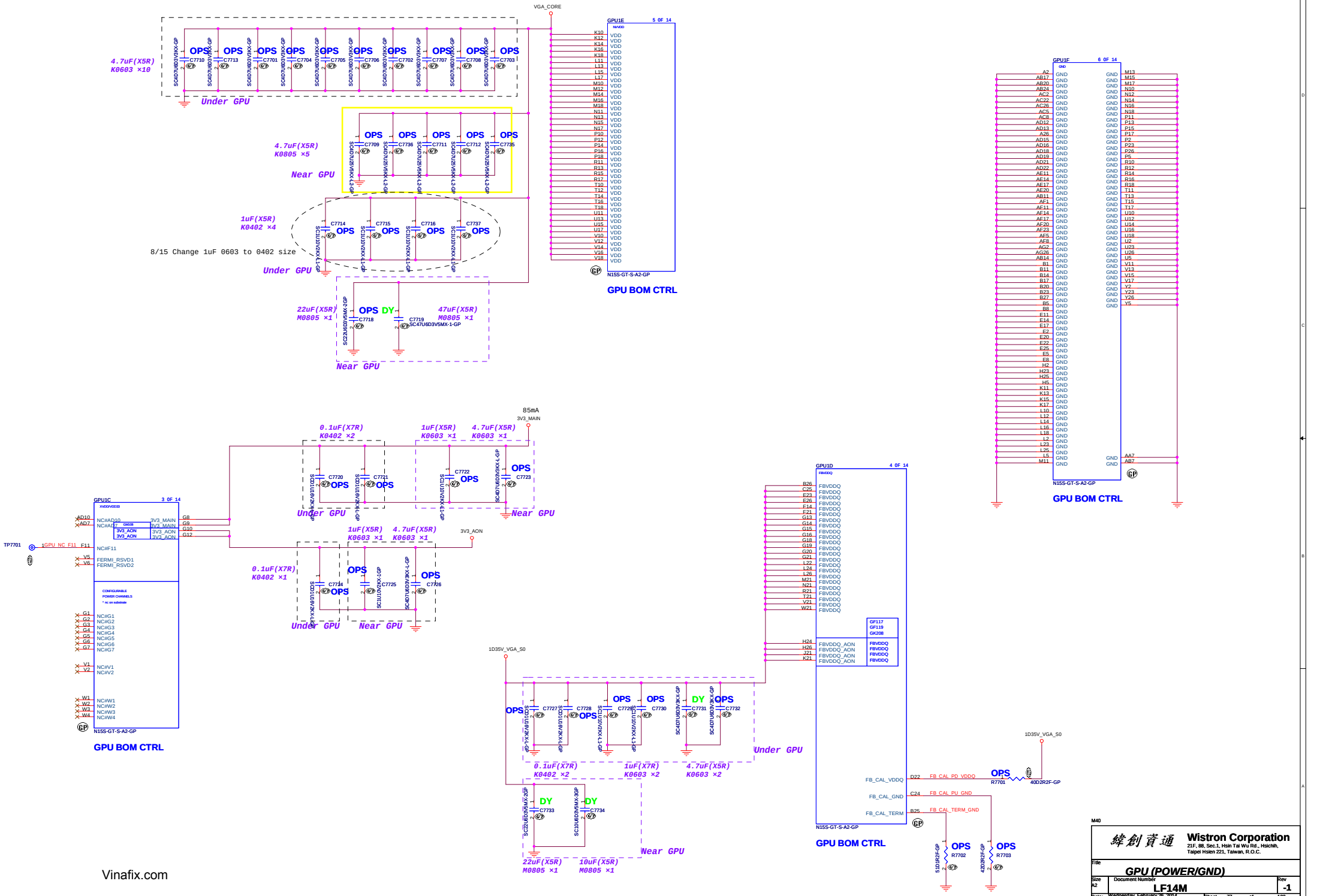
VGA_CORE
GPU1E 5 OF 14
N15S-GT-S-A2-GP
GPU BOM CTRL
4.7uF(X5R) K0603 ×10
Under GPU
4.7uF(X5R) K0805 ×5
Near GPU
1uF(X5R) K0402 ×4
8/15 Change 1uF 0603 to 0402 size
Under GPU
22uF(X5R) M0805 ×1
47uF(X5R) M0805 ×1
Near GPU
GPU1F 6 OF 14
N15S-GT-S-A2-GP
GPU BOM CTRL
85mA
3V3_MAIN
0.1uF(X7R) K0402 ×2
1uF(X5R) K0603 ×1
4.7uF(X5R) K0603 ×1
Under GPU
Near GPU
GPU1C 3 OF 14
N15S-GT-S-A2-GP
GPU BOM CTRL
TP7701
3V3_AON
0.1uF(X7R) K0402 ×1
Under GPU
Near GPU
1D35V_VGA_S0
Under GPU
0.1uF(X7R) K0402 ×2
1uF(X7R) K0603 ×2
4.7uF(X5R) K0603 ×2
22uF(X5R) M0805 ×1
10uF(X5R) M0805 ×1
Near GPU
GPU1D 4 OF 14
N15S-GT-S-A2-GP
GPU BOM CTRL
FB_CAL_VDDQ
FB_CAL_GND
FB_CAL_TERM
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
R7701
R7702
R7703
Vinafix.com
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Title
GPU (POWER/GND)
Size A2
Document Number LF14M
Rev -1
Date: Wednesday, February 26, 2014
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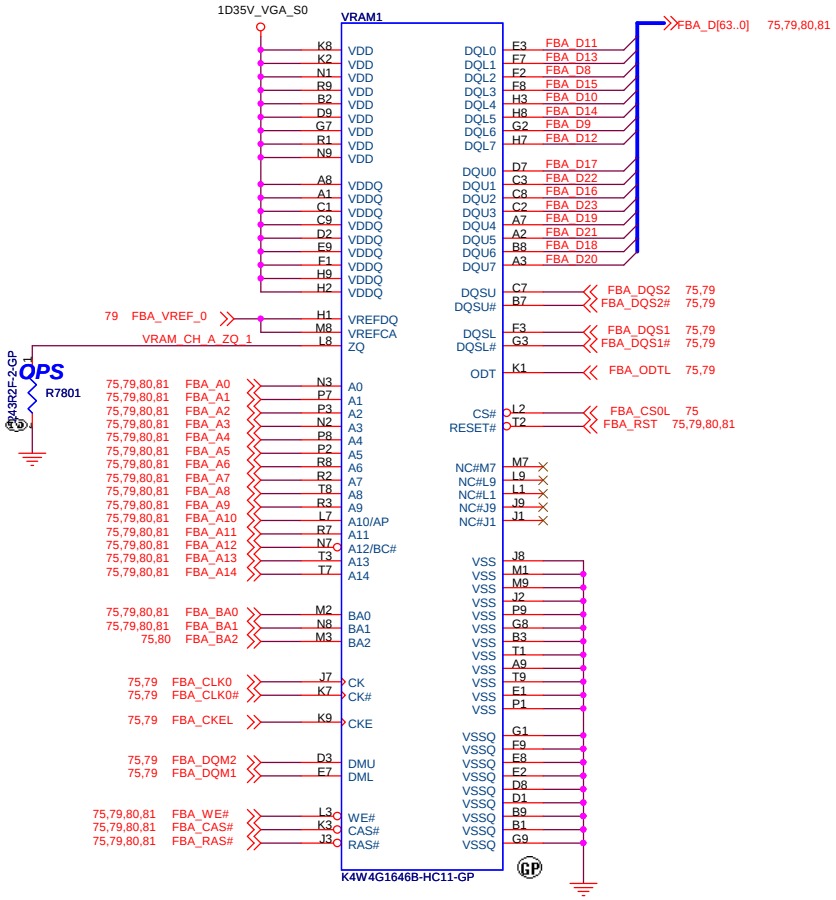
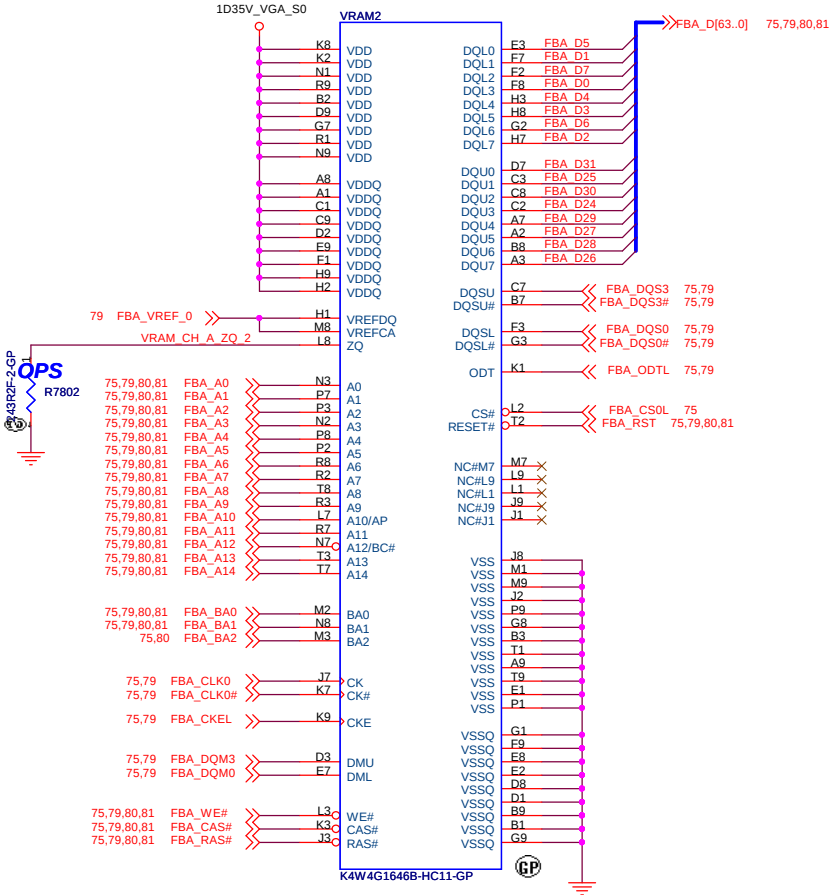
Data Bits 31:0 RANK 0



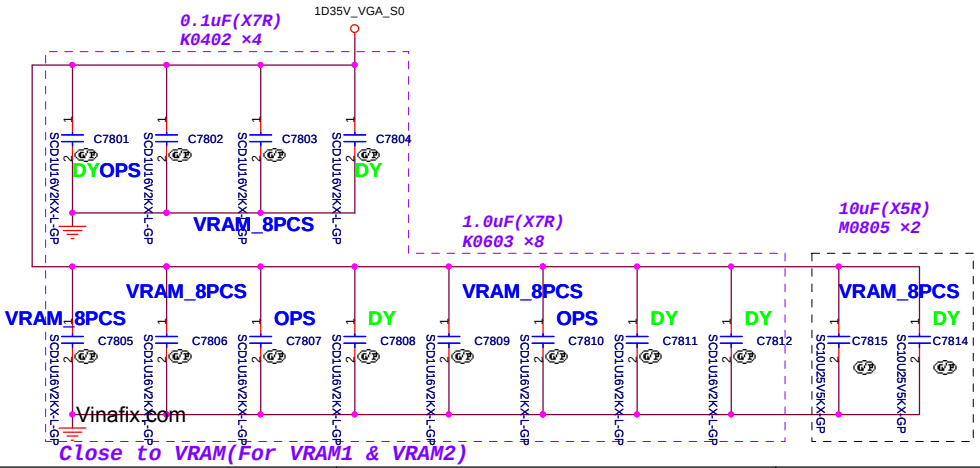
72.41646.00U

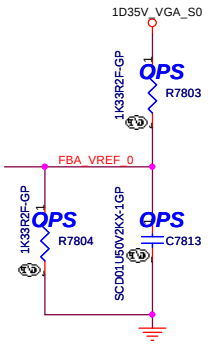
VRAM BOM CTRL



72.41646.00U

VRAM BOM CTRL





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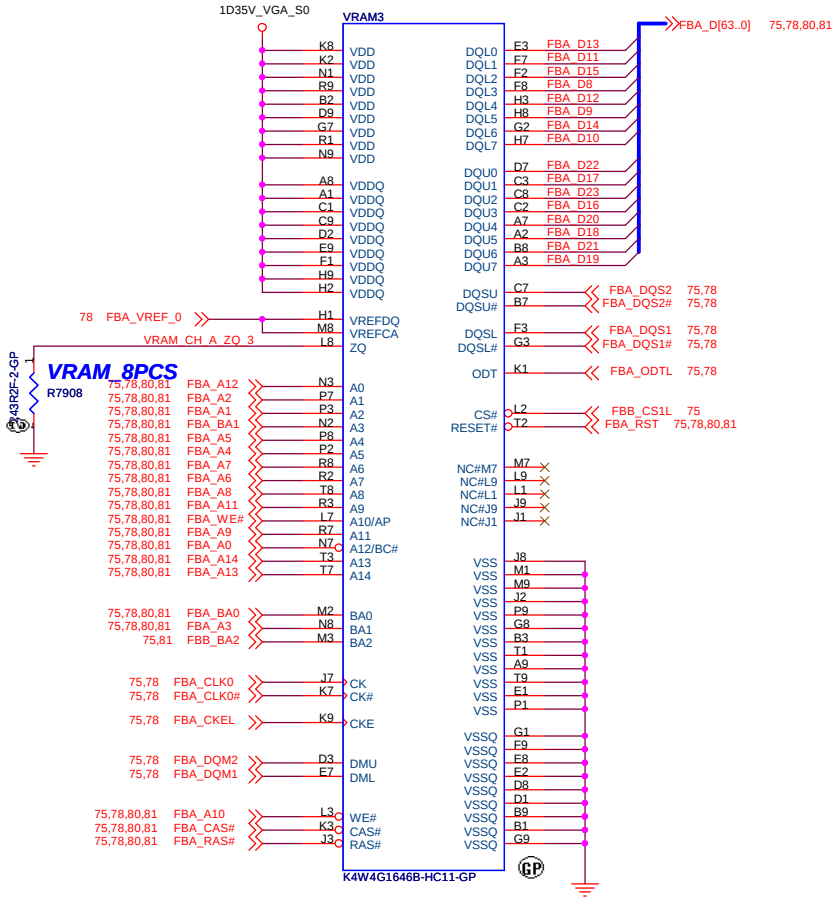
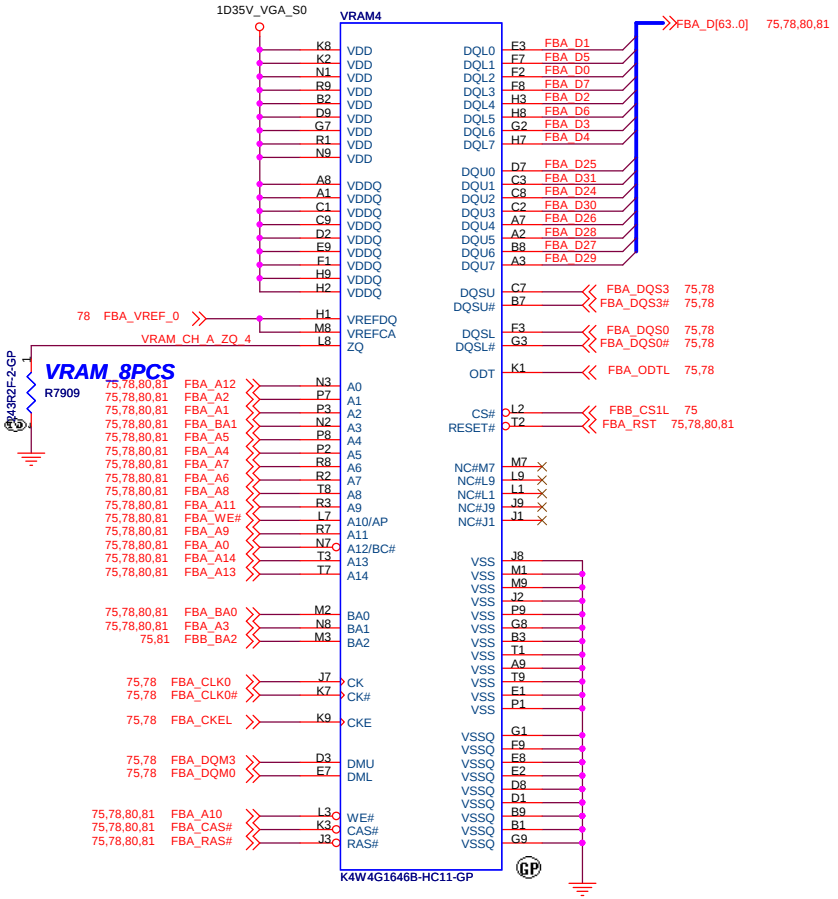
Title: GPU-VRAM1,2 (1/4)		
Size: A3	Document Number: LF14M	Rev: -1
Date: Wednesday, February 26, 2014	Sheet 78 of 102	

Data Bits 31:0 RANK 1



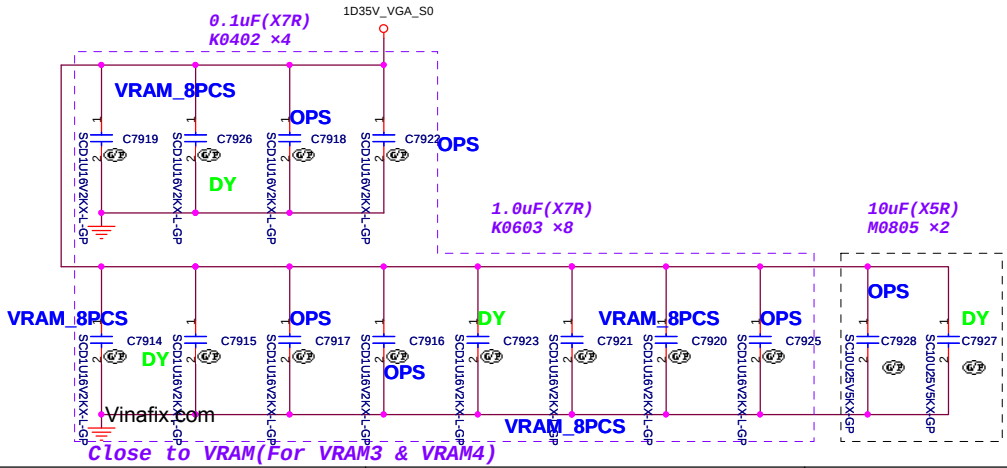
72.41646.00U

VRAM BOM CTRL



72.41646.00U

VRAM BOM CTRL



M40

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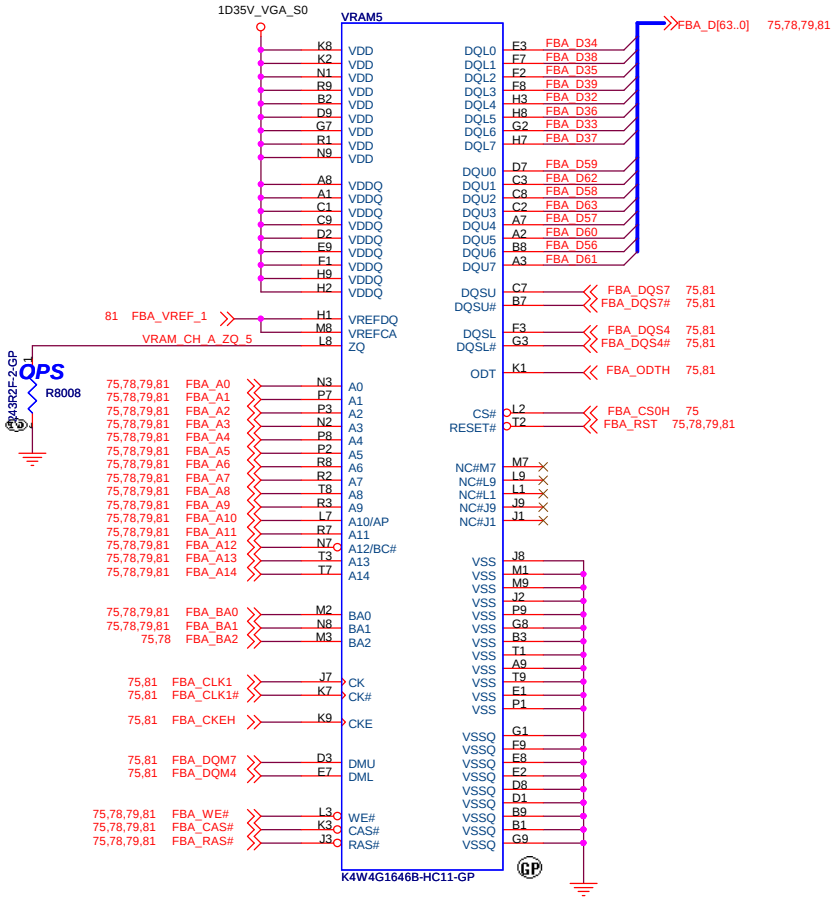
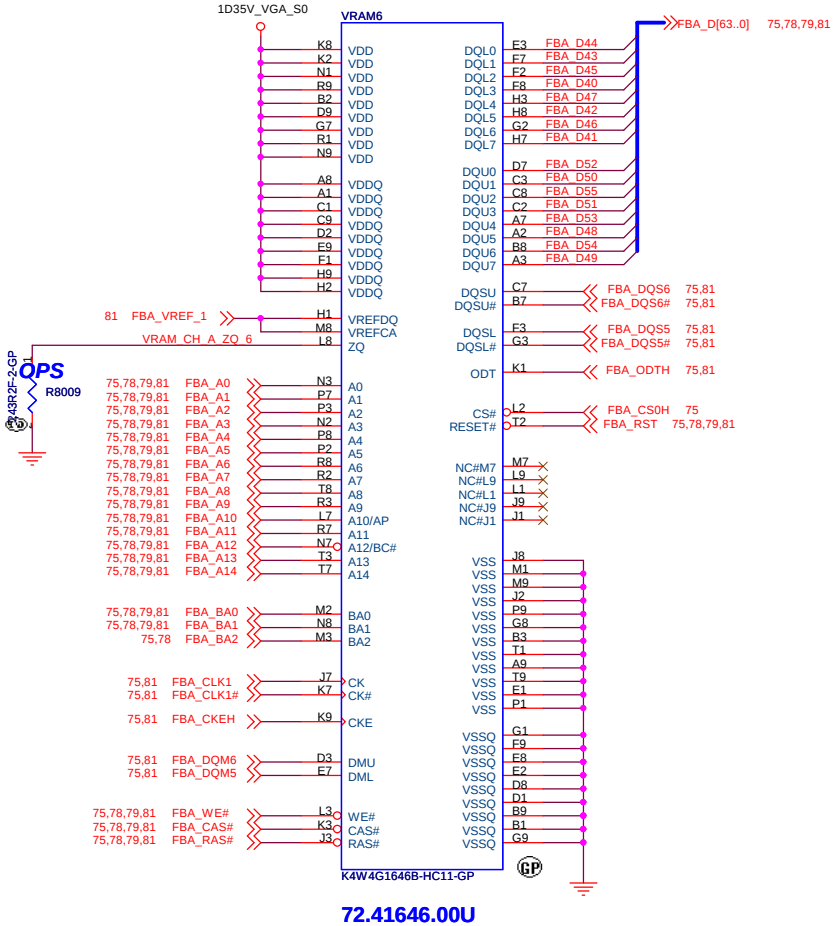
Title	**GPU-VRAM3,4 (2/4)**	
Size A3	Document Number **LF14M**	Rev **-1**
Date: Wednesday, February 26, 2014	Sheet 79 of 102	

Data Bits 63:32 RANK 0



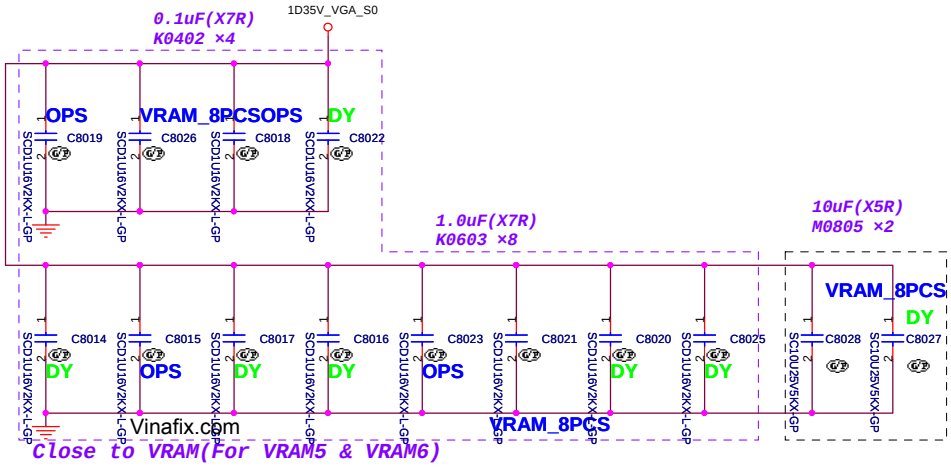
72.41646.00U

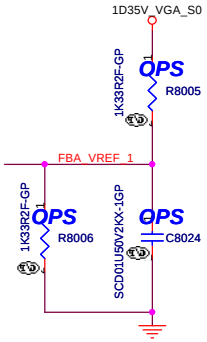
VRAM BOM CTRL



72.41646.00U

VRAM BOM CTRL





M40

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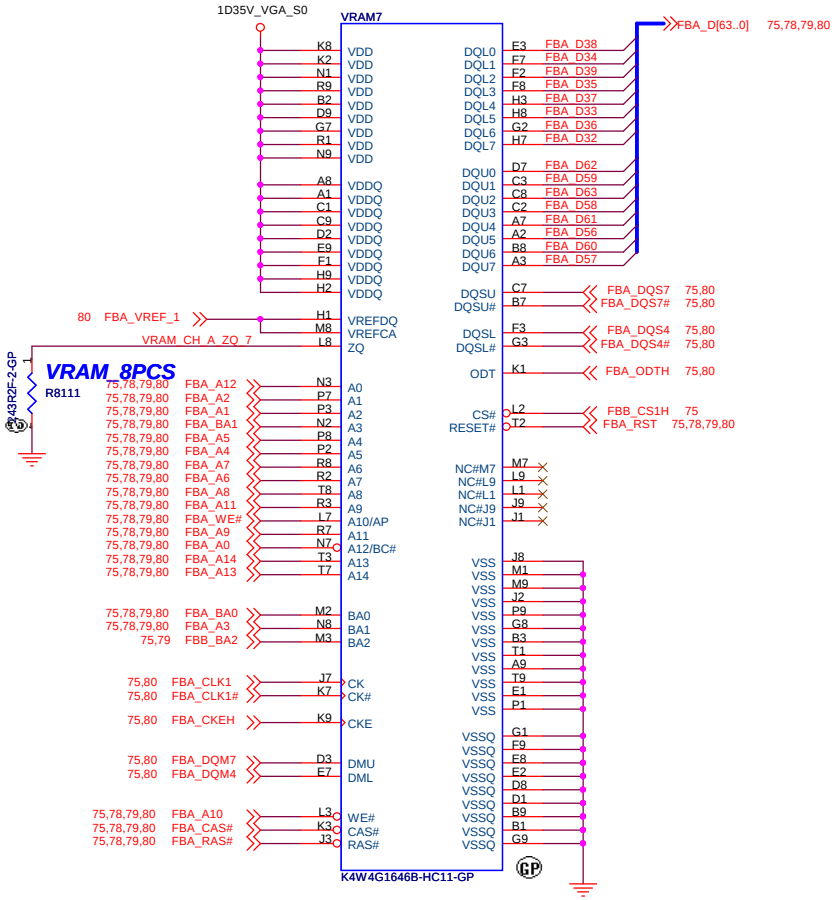
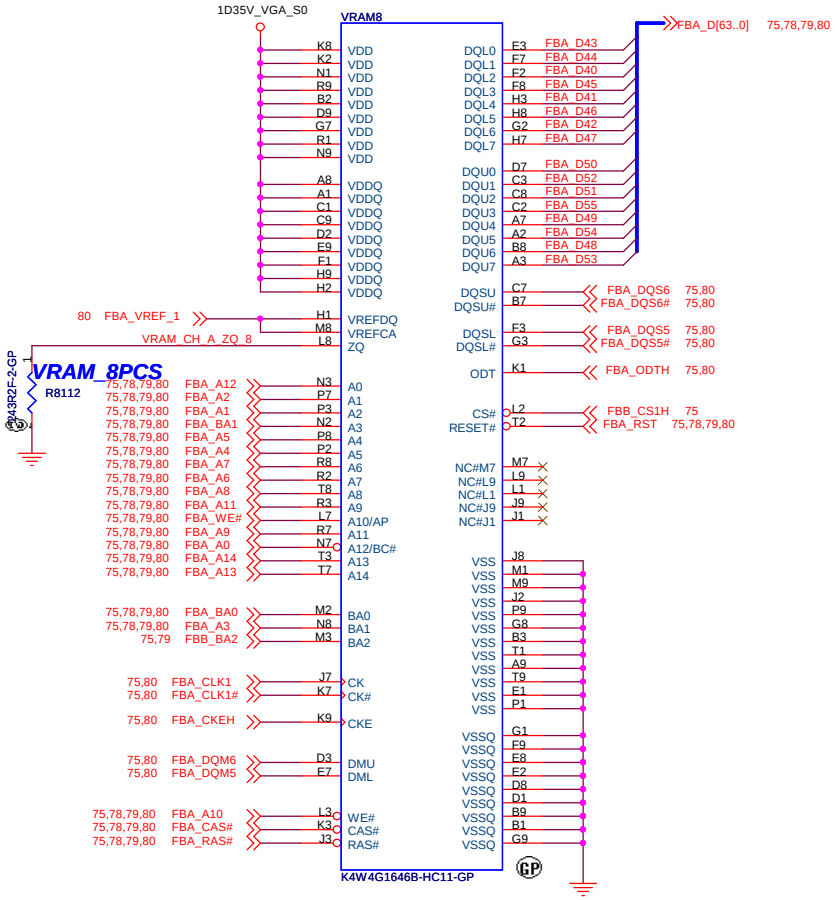
Title: GPU-VRAM5,6 (3/4)		
Size: A3	Document Number: LF14M	Rev: -1
Date: Wednesday, February 26, 2014	Sheet 80 of 102	

Data Bits 63:32 RANK 1



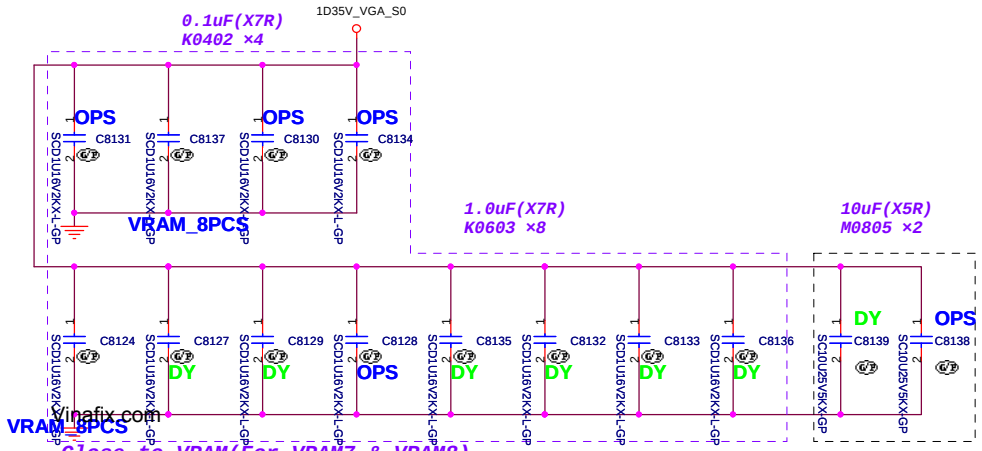
72.41646.00U

VRAM BOM CTRL



72.41646.00U

VRAM BOM CTRL



M40

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size: A3 | Document Number: LF14M | Rev: -1

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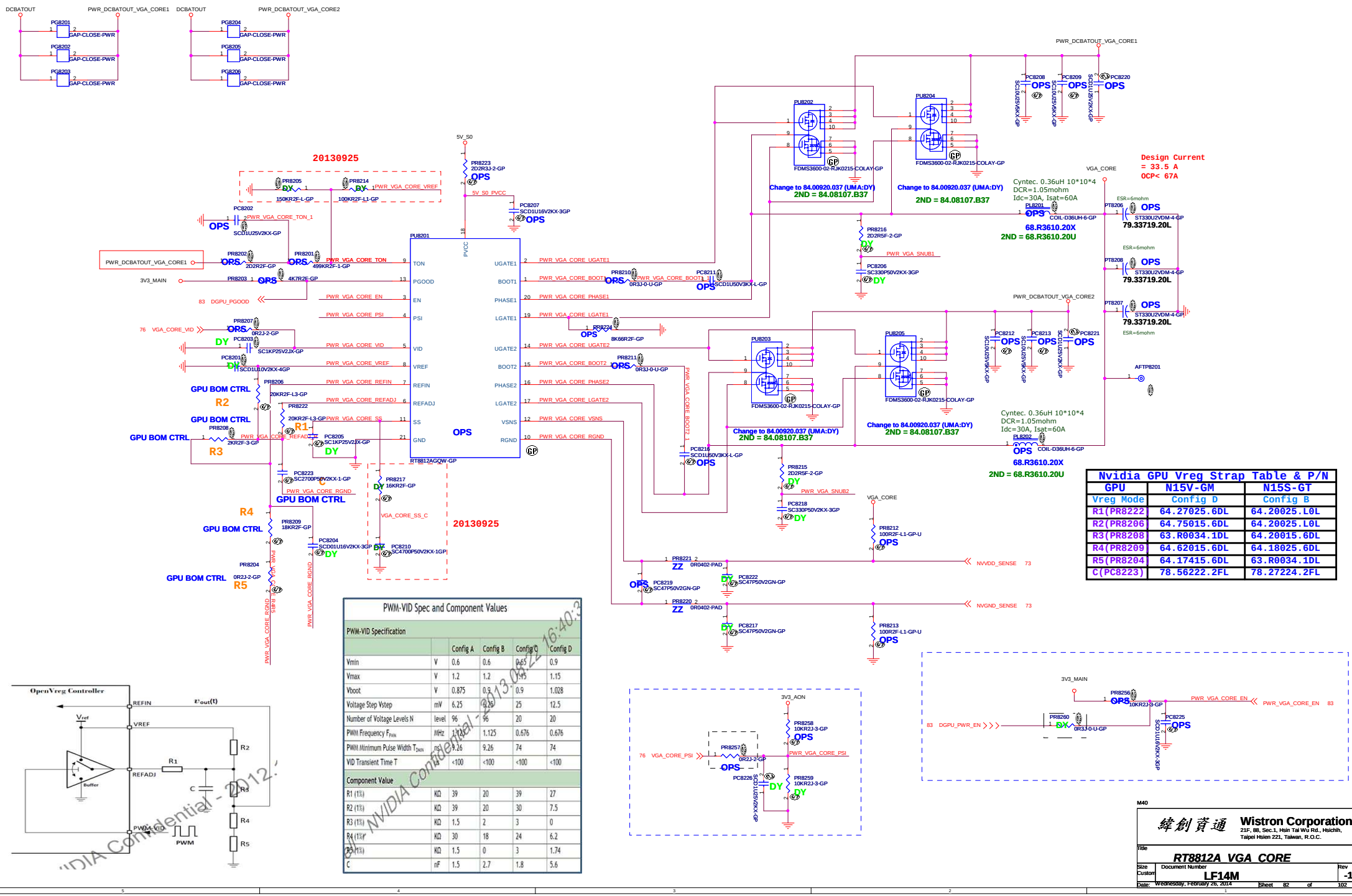

Nvidia GPU Vreg Strap Table & P/N		
GPU	N15V-GM	N15S-GT
Vreg Mode	Config D	Config B
R1(PR8222)	64.27025.6DL	64.20025.L0L
R2(PR8206)	64.75015.6DL	64.20025.L0L
R3(PR8208)	63.R0034.1DL	64.20015.6DL
R4(PR8209)	64.62015.6DL	64.18025.6DL
R5(PR8204)	64.17415.6DL	63.R0034.1DL
C(PC8223)	78.56222.2FL	78.27224.2FL

PWM-VID Spec and Component Values					
PWM-VID Specification					
		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.15	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	9.26	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26	74	74
VID Transient Time T		<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	20	39	27
R2 (1%)	KΩ	39	20	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	18	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6

M40	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: RT8812A VGA CORE		
Size: Custom	Document Number: LF14M	Rev: -1
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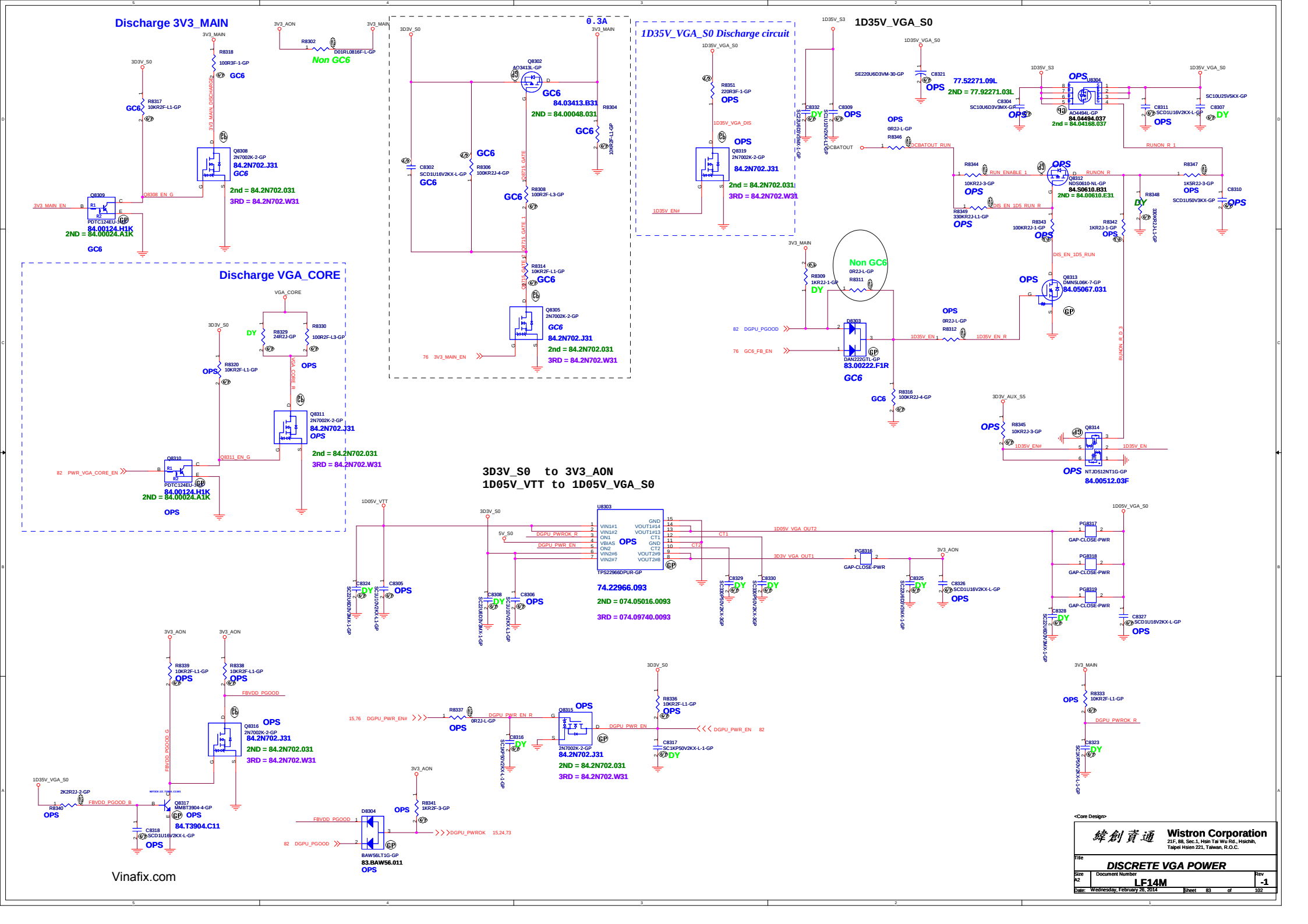
Discharge 3V3_MAIN
3V3_AON
3V3_MAIN
R8302
D01RL0816F-L-GP
Non GC6
3V3_MAIN
R8318
100R3F-1-GP
GC6
3V3_MAIN_DISCHARGE
3D3V_S0
R8317
10KR2F-L1-GP
GC6
Q8308
2N7002K-2-GP
84.2N702.J31
GC6
2nd = 84.2N702.031
3RD = 84.2N702.W31
Q8308_EN_G
3V3_MAIN_EN
Q8309
PDTC124EU-GP
84.00124.H1K
2ND = 84.00024.A1K
GC6
0.3A
3D3V_S0
3V3_MAIN
Q8302
AO3413L-GP
GC6
84.03413.B31
2ND = 84.00048.031
R8304
GC6
10KR2F-L1-GP
C8302
SCD1U16V2KX-L-GP
GC6
R8306
100KR2J-4-GP
GC6
R8308
100R2F-L3-GP
Q0215_GATE
Q0215_GATE_1
R8314
10KR2F-L1-GP
GC6
Q8305
2N7002K-2-GP
GC6
84.2N702.J31
2nd = 84.2N702.031
3RD = 84.2N702.W31
76 3V3_MAIN_EN
1D35V_VGA_S0 Discharge circuit
1D35V_VGA_S0
R8351
220R3F-1-GP
OPS
1D35V_VGA_DIS
Q8319
2N7002K-2-GP
84.2N702.J31
2nd = 84.2N702.031
3RD = 84.2N702.W31
1D35V_EN#
1D35V_S3
1D35V_VGA_S0
1D35V_VGA_S0
SE220U6D3VM-30-GP
C8321
OPS
77.52271.09L
2ND = 77.92271.03L
C8332
DY
C8309
OPS
SC220U6D3VM-GP
SCU100U2KX-L-GP
OPS
0R2J-L-GP
R8346
CBATOUT
CBATOUT_RUN
1D35V_S3
OPS
U8304
AO4494L-GP
84.04494.037
2nd = 84.04168.037
C8304
SC10U6D3V3MX-GP
OPS
1D35V_VGA_S0
SC10U25V5KX-GP
C8311
SCD1U16V2KX-L-GP
OPS
C8307
DY
RUNON_R_1
R8344
10KR2J-3-GP
OPS
RUN_ENABLE_1
Q8312
NDS0610-NL-GP
84.S0610.B31
2ND = 84.00610.E31
RUNON_R
R8347
1KR2J-3-GP
OPS
SCD1U50V3KX-GP
C8310
OPS
R8348
DY
330KR2J-L-GP
R8349
330KR2J-L-GP
OPS
DIS_EN_1D5_RUN_R
R8343
100KR2J-1-GP
OPS
R8342
1KR2J-1-GP
OPS
DIS_EN_1D5_RUN
Discharge VGA_CORE
VGA_CORE
3D3V_S0
DY
R8329
24R2J-GP
R8330
100R2F-L3-GP
R8320
10KR2F-L1-GP
OPS
OPS
VGA_CORE_R
Q8311
2N7002K-2-GP
84.2N702.J31
OPS
2nd = 84.2N702.031
3RD = 84.2N702.W31
Q8311_EN_G
82 PWR_VGA_CORE_EN
Q8310
PDTC124EU-GP
84.00124.H1K
2ND = 84.00024.A1K
OPS
3V3_MAIN
Non GC6
0R2J-LP
R8311
R8309
1KR2J-1-GP
DY
82 DGPU_PGOOD
R8303
DAN222GTL-GP
83.00222.F1R
GC6
76 GC6_FB_EN
GC6
R8316
100KR2J-4-GP
OPS
0R2J-L-GP
R8312
1D35V_EN_1
1D35V_EN_R
Q8313
DMNSL06K-7-GP
84.05067.031
OPS
RUNON_R_0_3
3D3V_AUX_S5
OPS
R8345
10KR2J-3-GP
1D35V_EN#
Q8314
NTJD5121NT1G-GP
84.00512.03F
OPS
1D35V_EN
3D3V_S0 to 3V3_AON
1D05V_VTT to 1D05V_VGA_S0
1D05V_VTT
3D3V_S0
5V_S0
DGPU_PWROK_R
DGPU_PWR_EN
U8303
TPS22966DPUR-GP
OPS
74.22966.093
2ND = 074.05016.0093
3RD = 074.09740.0093
1D05V_VGA_OUT2
3D3V_VGA_OUT1
CT1
CT2
PG8316
GAP-CLOSE-PWR
3V3_AON
C8324
DY
C8305
OPS
C8308
DY
C8306
OPS
C8329
DY
C8330
DY
C8325
DY
C8326
SCD1U16V2KX-L-GP
OPS
1D05V_VGA_S0
PG8317
GAP-CLOSE-PWR
PG8318
GAP-CLOSE-PWR
PG8319
GAP-CLOSE-PWR
C8328
DY
C8327
SCD1U16V2KX-L-GP
OPS
3V3_AON
3V3_AON
R8339
10KR2F-L1-GP
OPS
R8338
10KR2F-L1-GP
OPS
FBVDD_PGOOD
Q8316
2N7002K-2-GP
84.2N702.J31
OPS
2ND = 84.2N702.031
3RD = 84.2N702.W31
FBVDD_PGOOD_G
1D35V_VGA_S0
2K2R2J-2-GP
R8340
OPS
FBVDD_PGOOD_B
Q8317
MMBT3904-4-GP
OPS
84.T3904.C11
C8318
SCD1U16V2KX-L-GP
OPS
15,76 DGPU_PWR_EN#
R8337
0R2J-L-GP
OPS
DGPU_PWR_EN_R
Q8315
2N7002K-2-GP
84.2N702.J31
OPS
2ND = 84.2N702.031
3RD = 84.2N702.W31
DGPU_PWR_EN
C8316
DY
3D3V_S0
R8336
10KR2F-L1-GP
OPS
C8317
SC1KP50V2KX-L-1-GP
DY
DGPU_PWR_EN
82
3V3_AON
R8341
1KR2F-3-GP
OPS
FBVDD_PGOOD
D8304
BAW56LT1G-GP
83.BAW56.011
OPS
82 DGPU_PGOOD
DGPUPWROK 15,24,73
3V3_MAIN
R8333
10KR2F-L1-GP
OPS
DGPU_PWROK_R
C8323
DY
Vinafix.com
<Core Design>
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Wistron Corporation
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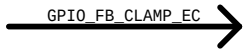
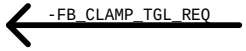
Taipei Hsien 221, Taiwan, R.O.C.
Title
DISCRETE VGA POWER
Size A2
Document Number
LF14M
Rev -1
Date: Wednesday, February 26, 2014
Sheet 83 of 102

Undefined Sys <-> GPU IO

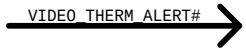
KBC <-> GPU



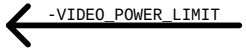
KBC output



KBC input

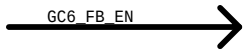


KBC GPIO (Reserved)

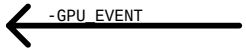


KBC output (Reserved)

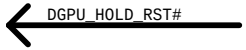
PCH <-> GPU



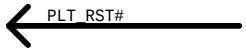
PCH input



PCH output

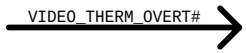


PCH output

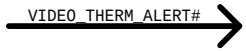


PCH output

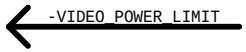
Thermal IC <-> GPU



Thermal IC input(Reserved)



Thermal IC GPIO(Reserved)



Thermal IC output(Reserved)

M40

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Title: *Switchable GFX LCD(1/2)*		
Size: A4	Document Number: LF14M	Rev: -1
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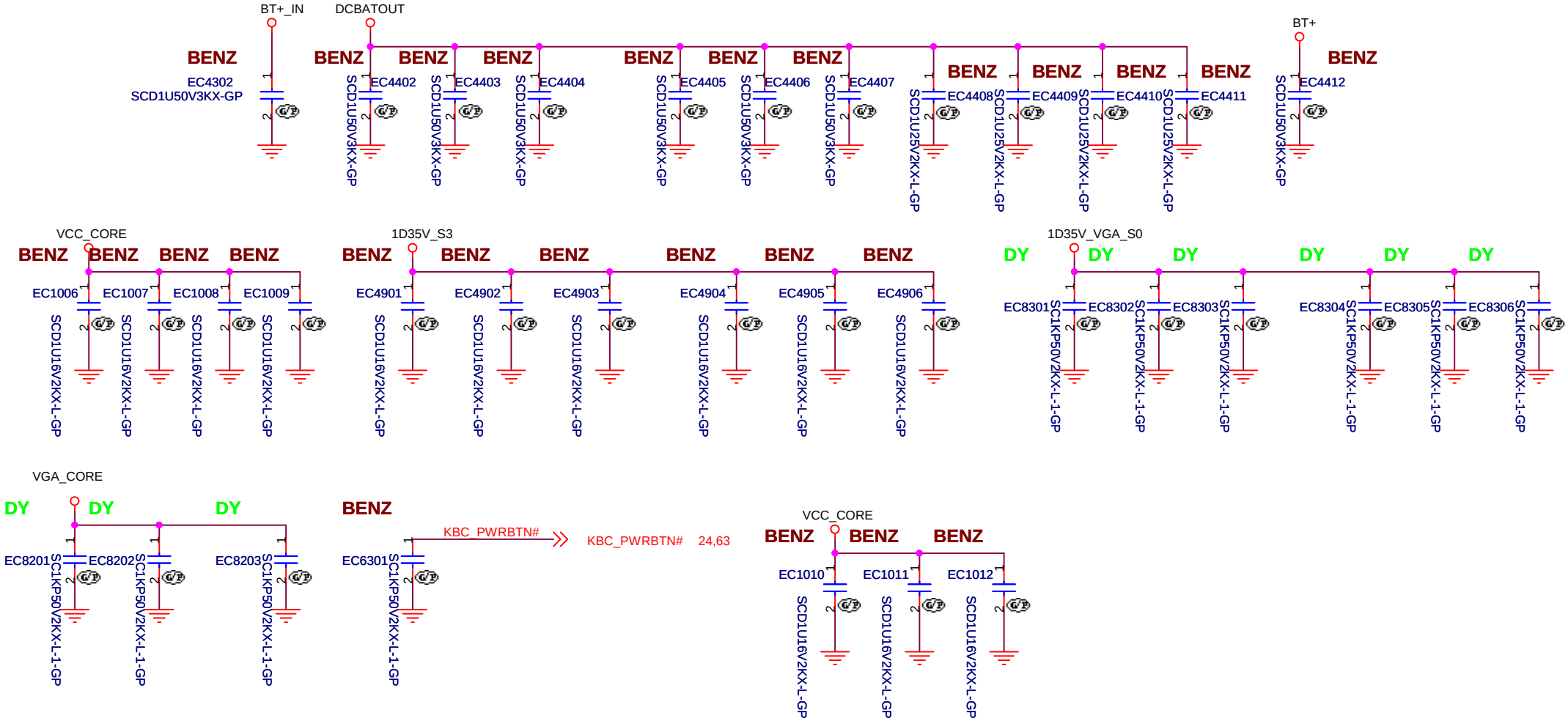

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Title: ***Benz Only***

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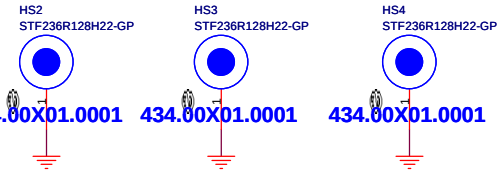
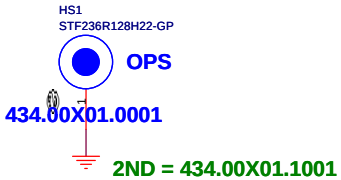
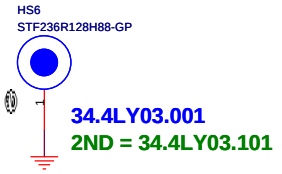
CPU Std-Off



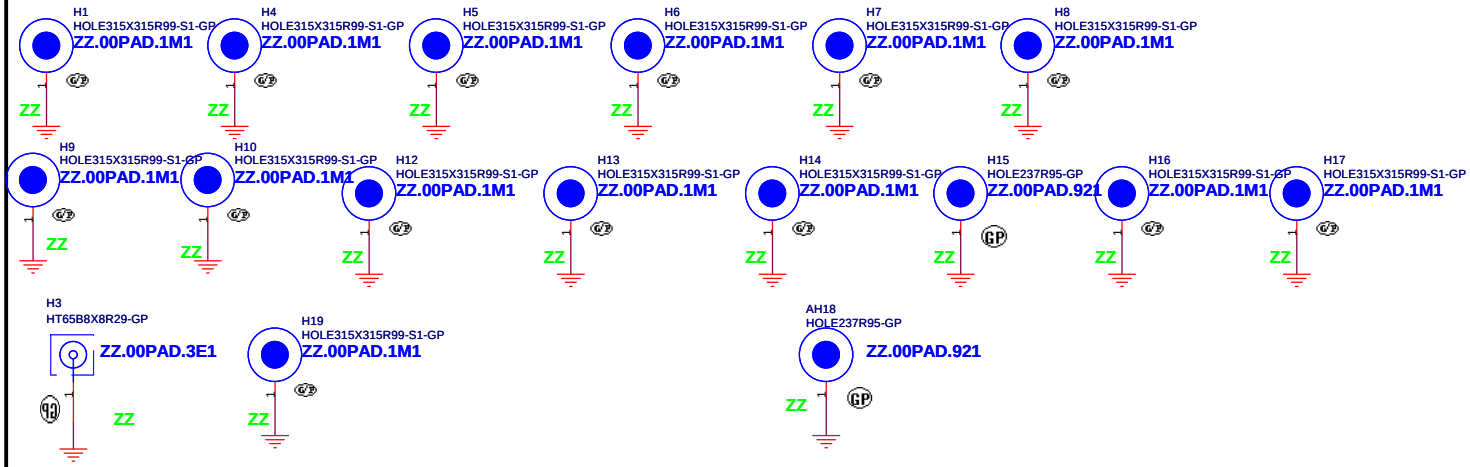
VGA Std-Off



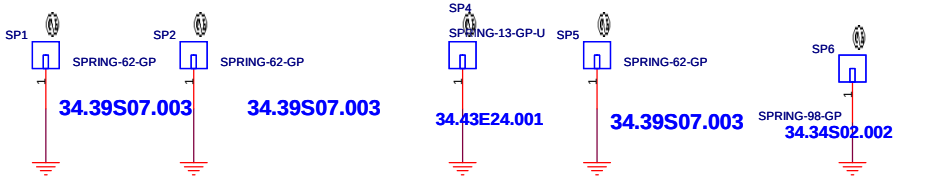
WLAN Std-Off



Structure boss



EMI



M40

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Title: *UNUSED PARTS/EMI Capacitors*

Size	Document Number	Rev
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Title

NFC

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TPM (M40/M50)

M40

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Title: *TPM*		
Size: A3	Document Number: LF14M	Rev: -1
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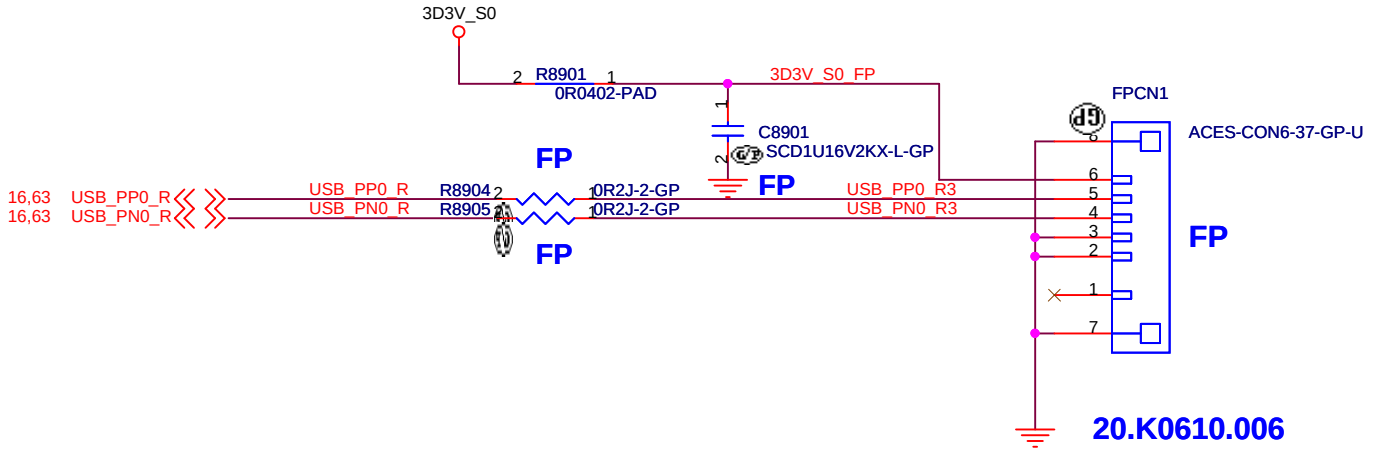
Check Date:2013/9/18

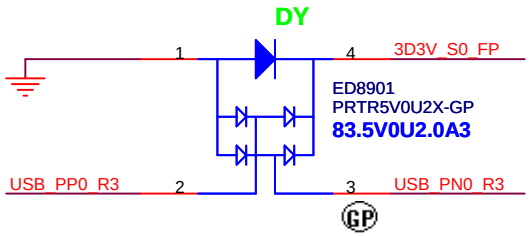
2014/2/6
USB_PP0/PN0改接到USB2.0 Port 1
NET維持不變

FingerPrint BD
M40/M50

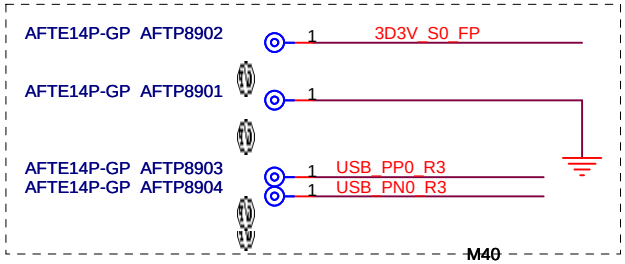


M40,M50 have Finger Print, USB2.0 Port isn't enough,
USB2.0 PN1/PP1 combine CR2.0 with FP

For EMI Test



Near FPCN1



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Title: *Finger Print*		
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Express Card***

Size	Document Number	Rev
A2	LF14M	-1

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Title

Smart Card socket

Size	Document Number	Rev
A	**LF14M**	**-1**

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Title

Switchable GFX eDP

Size	Document Number	Rev
A	**LF14M**	**-1**

Date: Wednesday, February 26, 2014 Sheet 92 of 102

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Title

Bottom Docking

Size	Document Number	Rev
A	**LF14M**	**-1**

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Title
Inter LAN WG1217LM

Size	Document Number	Rev
A3	**LF14M**	**-1**

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Title

LAN Switch

Size	Document Number	Rev
A	**LF14M**	**-1**

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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0[1]	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST#[1]	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4[1]	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST#[1]	0	System	18	HOOK7	DBR#[1]	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRST#	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

M40

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Title

PCH_XDP

Size	Document Number	Rev
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BOM Option Table		BOM Models (V=Stuff)			
Function	Acronym	M40	M50	U40	U50
Woofer AMP	WO			V	V
USB Charger	UC	V with UC_ST	V with UC_ST		
Non USB Charger	NUC			V	V
TPM	TPM	V	V		
PTC	PTC	V	V		
ODD	ODD		V with ZPODD		V with Non ZPODD
Thermal VD	TV				
DOCKING	DK		V		
Fingerprint	FP	V	V		
Backlight Keyboard	BK	V with BK14	V with BK15		
Analog Esesor	AG	V	V	V	V
For Debug CN	DB	V (in SA)	V (in SA)	V (in SA)	V (in SA)
HighSpeed I/O	HSIO				
Non HighSpeed I/O	Non HSIO	V	V	V	V
Platform type					
Haswell	BOM Ctrl_Model R2441	64.14335.6DL	64.17435.6DL	64.76825.6DL	64.10035.6DL
Broadwell		64.47025.6DL	64.64925.6DL	64.10025.6DL	64.20025.L0L
PCB Ver. (in SA)	BOM Ctrl_VER R2437	64.10025.6DL	64.10025.6DL	64.10025.6DL	64.10025.6DL
CPU	CPU BOM CTRL	See Config	See Config	See Config	See Config
LAN	LAN BOM CTRL LAN_SURGE	See Config	See Config	See Config	See Config
GIGA LAN	GIGA LAN_SURGE_GIGA	See Config	See Config	See Config	See Config
Touch Panel	TOUCH (DY:Non Touch)	See Config	See Config	See Config	See Config
Do Not Stuff	DY/ZZ				

GPU BOM CTRL		For Detail see P82
GPU	N15V-GM	N15S-GT
Lenovo P/N	11202477	11202478
OPS (UMA:DY)	V	V
PR8222	64.27025.6DL	64.20025.L0L
PR8206	64.75015.6DL	64.20025.L0L
PR8208	63.R0034.1DL	64.20015.6DL
PR8209	64.62015.6DL	64.18025.6DL
PR8204	64.17415.6DL	63.R0034.1DL
PC8223	78.56222.2FL	78.27224.2FL

NVIDIA GC6 Power Management		
GPU	N15V-GM	N15S-GT
GC6 Support	Not Support	GC6 2.0 only
GC6		V
GC6 2.0		V
Non GC6	V	
Non GC6 2.0	V	

VRAM BOM CTRL	(Default Setting:900MHZ)							
Lenovo P/N	1101057	1101018	1100788	1100897	1101028	1101019	1100661	1100677
IC Vendor	Micron	Micron	Hynix	Hynix	Samsung	Samsung	Micron	Micron
IC Vendor P/N	MT41K128M16JY-107G:K N15V-GM only	MT41J256M16HA-093G:E N15S-GT only	H5TC2G63FFR-11C N15V-GM/N15S-GT	H5TC4G63AFR-11C N15V-GM/N15S-GT	K4W2G1646Q-BC1A	K4W4G1646D-BC1A N15V-GM/N15S-GT	MT41J128M16JT-093G:K N15S-GT only	MT41K256M16HA-107G:E N15V-GM only
RANK0 VRAM1,VRAM2,VRAM5,VRAM6	Stuff with Discrete 1GB	Stuff with Discrete 2GB/4GB	Stuff with Discrete 1GB	Stuff with Discrete 2GB/4GB		Stuff with Discrete 2GB/4GB	Stuff with Discrete 1GB	
RANK1 VRAM3,VRAM4,VRAM7,VRAM8		Stuff with Discrete 4GB		Stuff with Discrete 4GB		Stuff with Discrete 4GB		
R7642(Strap0-L)			N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L				
R7631(Strap0-H)	N15V-GM:64.10025.L0L	N15S-GT:64.49925.6DL	N15S-GT:64.49925.6DL	N15S-GT:64.49925.6DL		N15V-GM:64.10025.L0L N15S-GT:64.49925.6DL	N15S-GT:64.49925.6DL	N15V-GM:64.10025.L0L
R7643(Strap1-L)	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L
R7632(Strap1-H)								
R7644(Strap2-L)	N15V-GM:64.10025.L0L					N15V-GM:64.10025.L0L		
R7633(Strap2-H)			N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L				N15V-GM:64.10025.L0L
R7645(Strap3-L)	N15V-GM:64.10025.L0L			N15V-GM:64.10025.L0L				
R7635(Strap3-H)			N15V-GM:64.10025.L0L			N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L
R7646(Strap4-L)	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L
R7634(Strap4-H)								
R7639(ROM_SI-L)	N15V-GM:64.10025.L0L	N15S-GT:64.24925.6DL	N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L N15S-GT:64.20025.L0L		N15V-GM:64.10025.L0L N15S-GT:64.30025.6DL		N15V-GM:64.10025.L0L
R7636(ROM_SI-H)			N15S-GT:64.10025.L0L				N15S-GT:64.15025.6DL	
R7640(ROM_SO-L)	N15V-GM:64.10025.L0L	N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL		N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL	N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L
R7637(ROM_SO-H)								
R7641(ROM_SCLK-L)	N15V-GM:64.10025.L0L	N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL		N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL	N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L
R7638(ROM_SCLK-H)								

M40

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Title: ***Change History***

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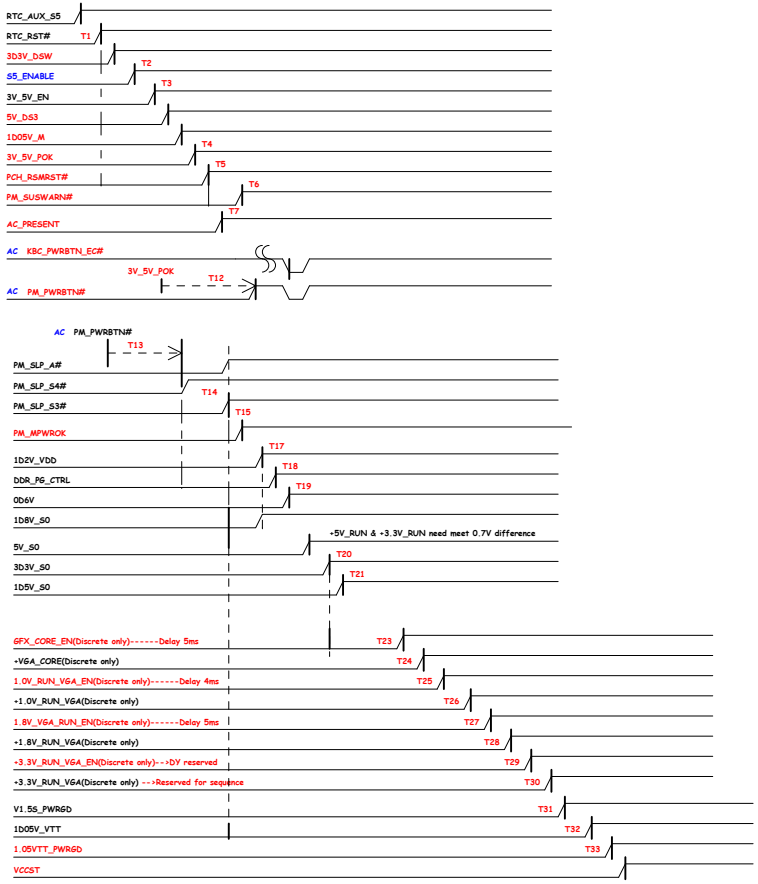
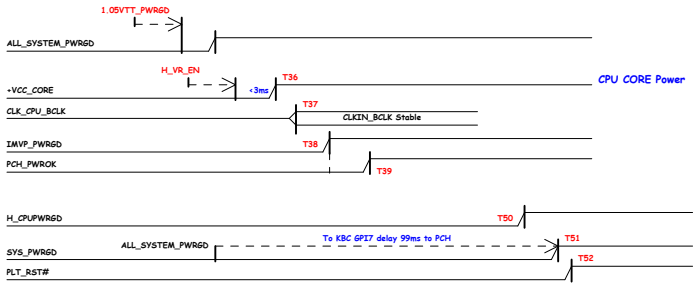
Intel-Power Up Sequence

(AC mode)





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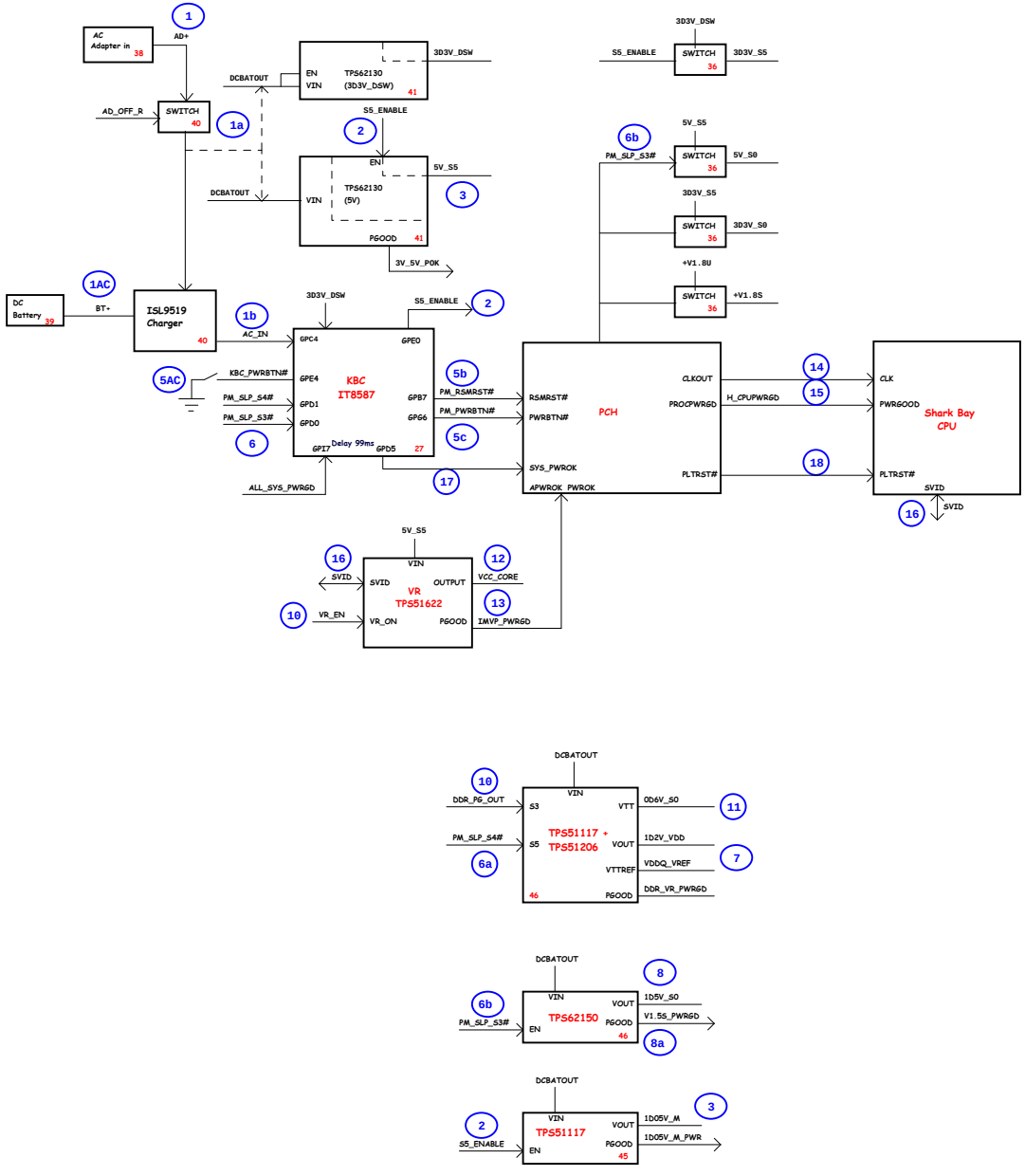
SHARK BAY POWER UP SEQUENCE DIAGRAM



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Title: Power Sequence

Size: A1 | Document Number: LF14M | Rev: -1

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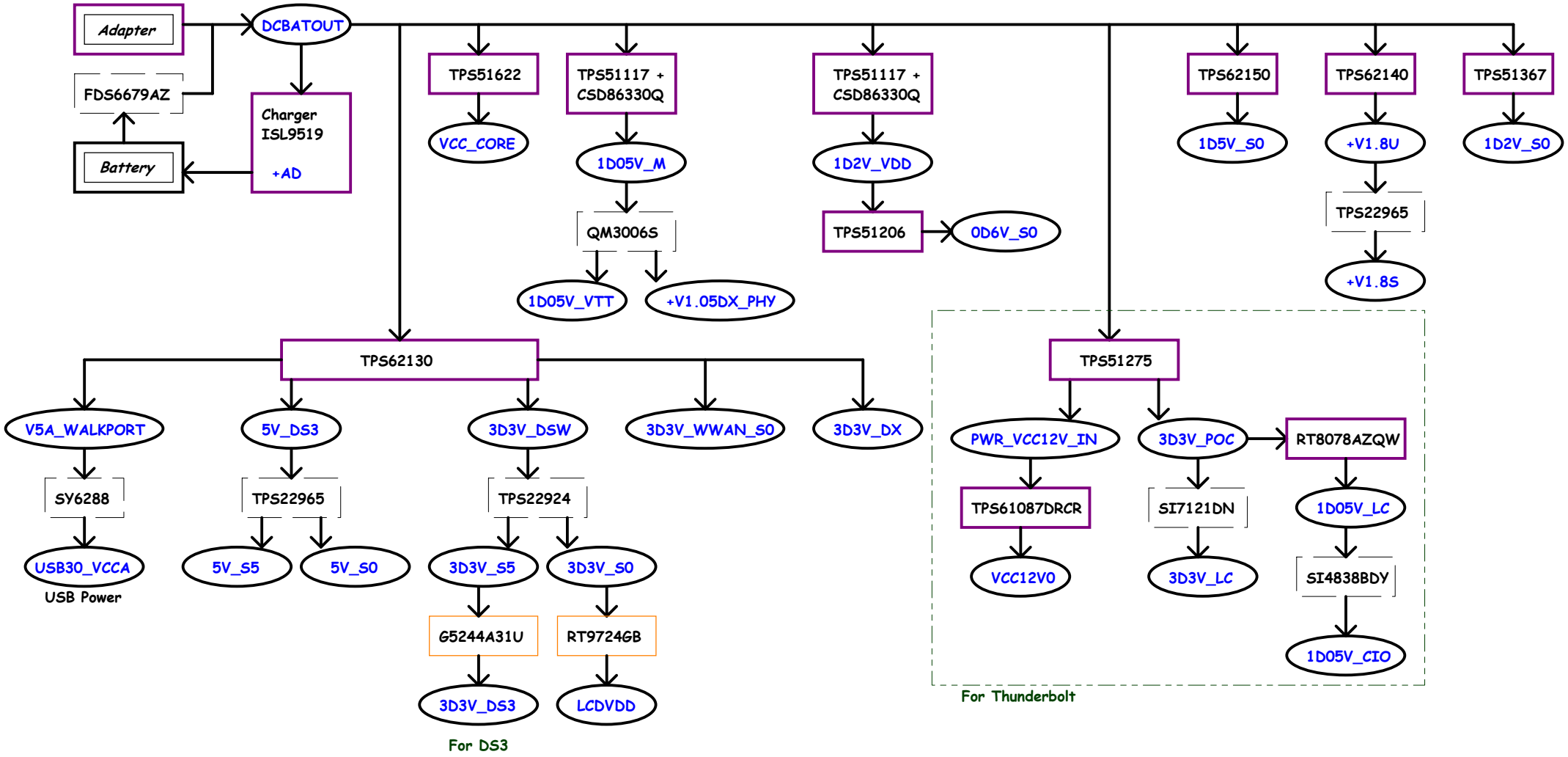

Power Shape

Regulator | LDO | Switch

Vinafix.com

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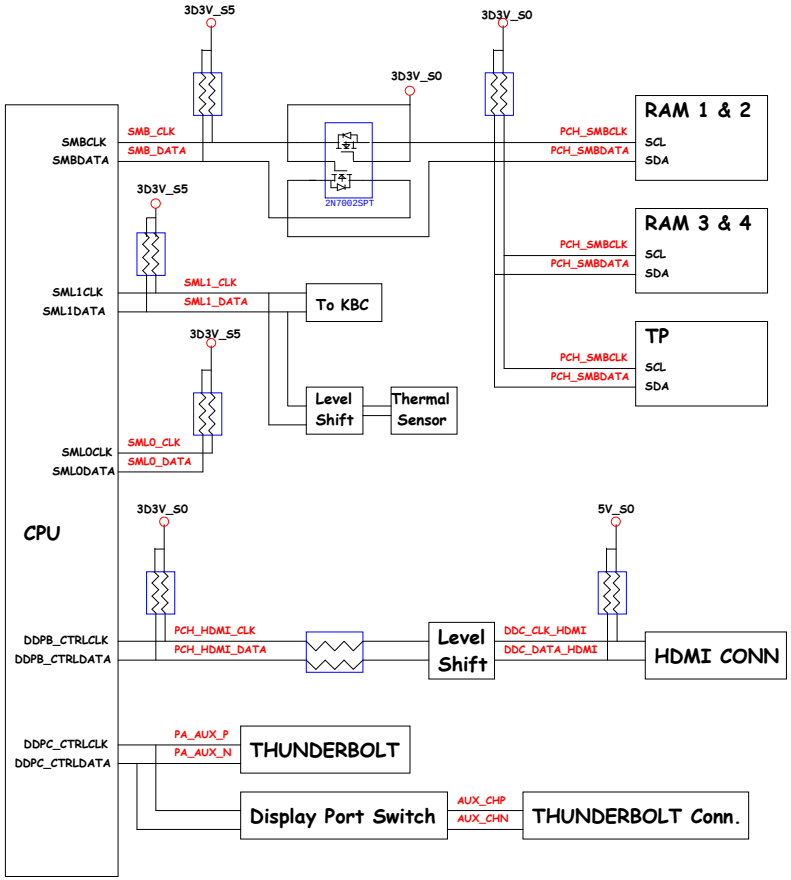
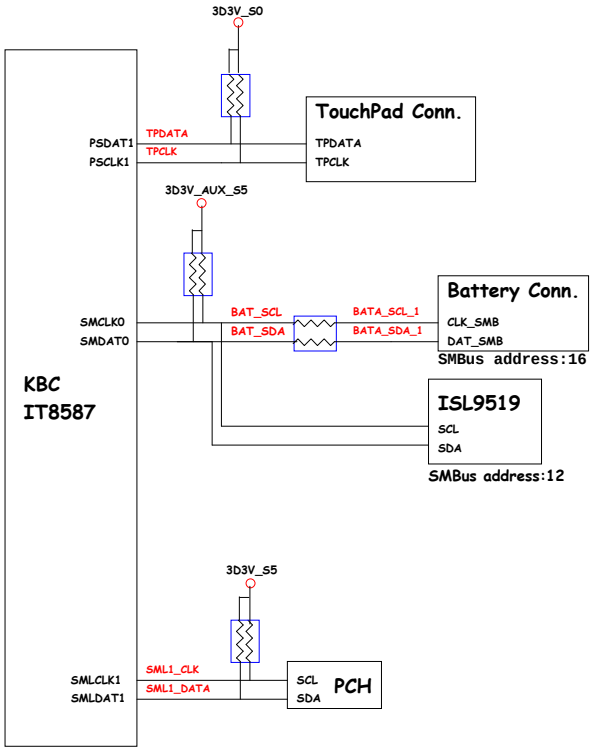
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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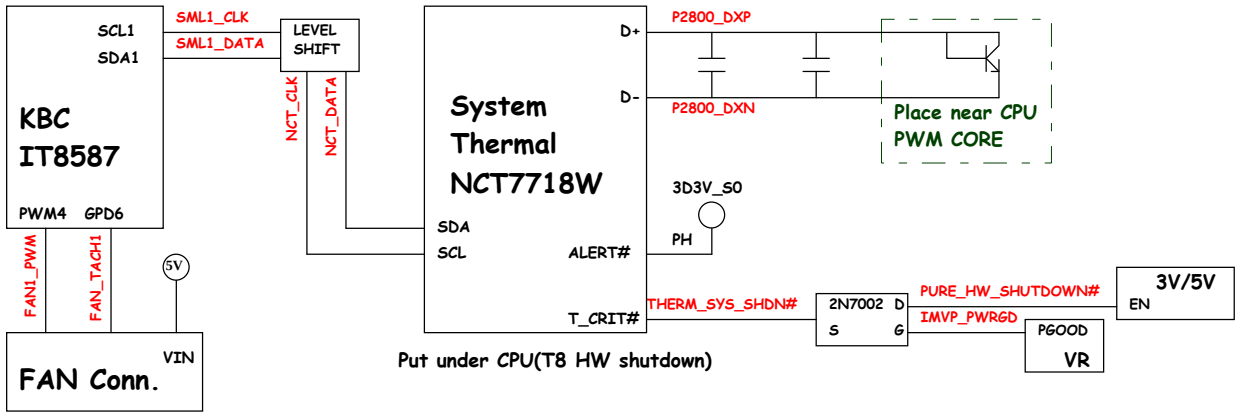
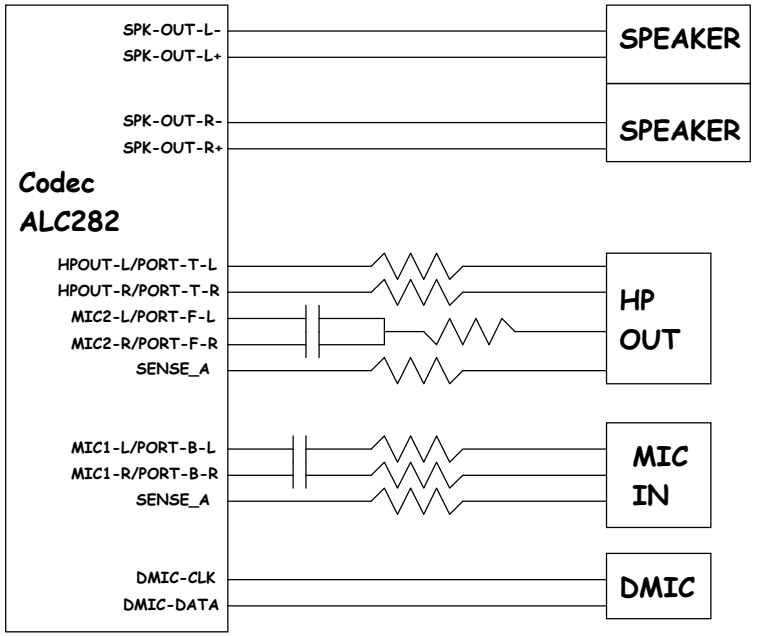
Thermal Block Diagram



Put under CPU(T8 HW shutdown)

Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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