

Model Name: GA-H81M-S2PV

Revision 1.01

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS X1 SLOT
16	PCI SLOT 1,2
17	ITE 8620 LPC IO
18	COM,LPT,KB_MS
19	HWM,FAN CTRL,OV,-PROCHOT
20	DUAL BIOS
21	R_USB30,FP,FUSB,SPK,SATALED
22	Realtek ALC887-VD2
23	REAR AUDIO JACK
24	REALTEK RTL8111F
25	DISCRETE POWER
26	ATX
27	VCORE ISL95812_1

SHEET

TITLE

28	VCORE ISL95812_2
29	RT8120_DDR POWER
31	DVI
32	IT8892E

[www.vinafix.com](http://www.vinafix.com)

Gigabyte Technology		
Cover Sheet		
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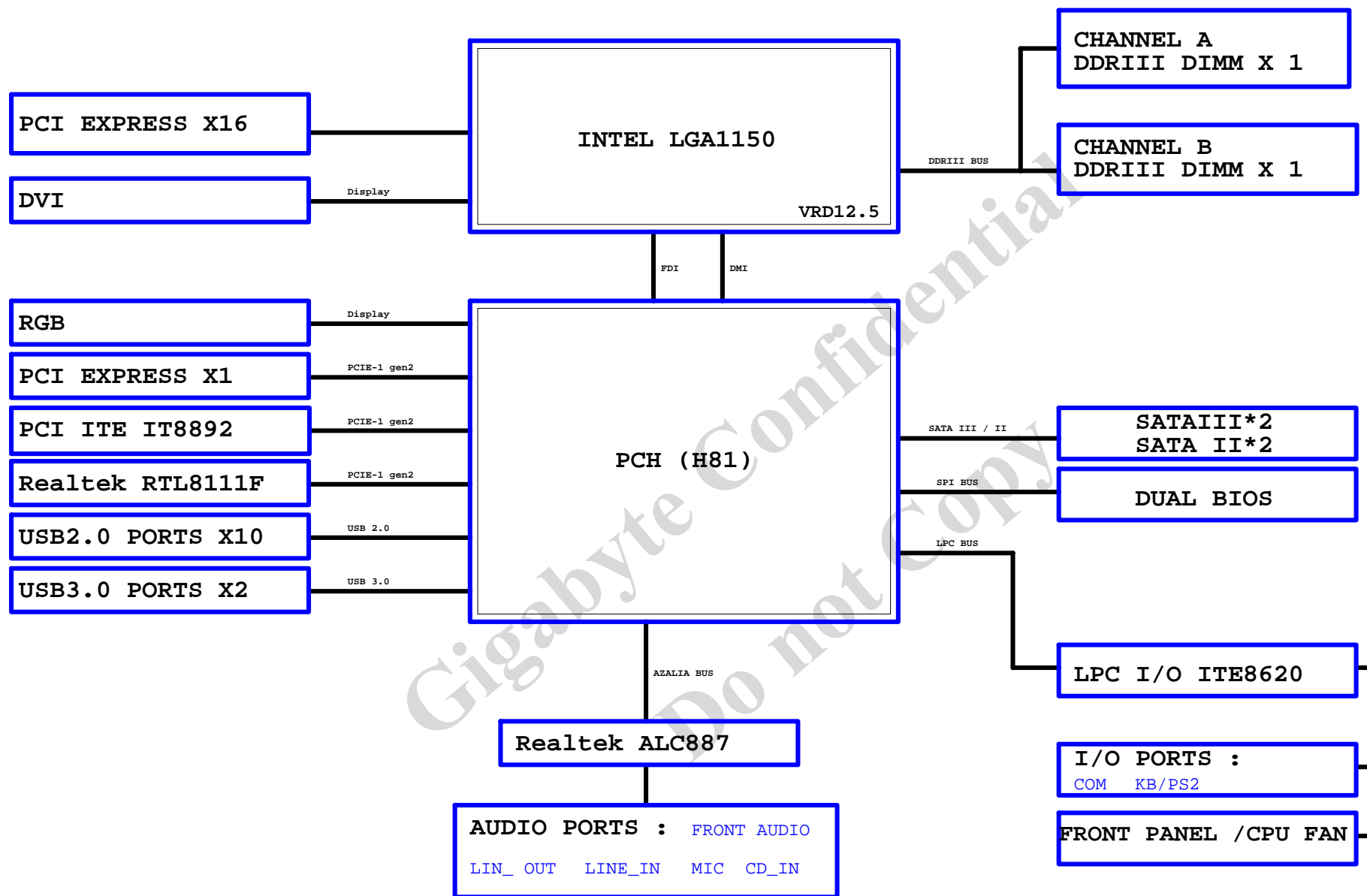
1

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C

D

## BLOCK DIAGRAM



**1.1V分壓**

VCC3

WR26  
2K4/1/X

WR31  
1K4/1/X

BC102  
1n4/XTR/50V/K

A\_CPURST [11,17]

**For IT8620 Ctrl**

CPU\_VTT\_OR

WR3	90.9/4/1/X	PVIDSLCK
WR2	115/4/1	PVIDSOUT
WR4	75/4/1	-PVIDALRT

Figure 10 shows the pin connections for CPU VTT OR and CPU\_VTT\_OR0. The connections are as follows:

- CPU\_VTT\_OR** is connected to:
  - WR16 (514/1/X) to **TMS**
  - WR16 (514/1/X) to **TDO**
  - WR17 (514/1/X) to **TDI**
  - WR30 (514/1) to **HPRDY**
  - WR11 (514/4) to **TCK**
  - WR9 (514/4) to **TRST**
  - WR29 (1K/41/X) to **PECl**
  - WR10 (1K/41/X) to **CATERR**
  - WR25 (1K/41) to **PROCHOT**
  - WR56 (514/1/X) to **CPUFWROT**
  - WR55 (1K/41/X) to **CPUFWROT**
  - WR8 (1K/41) to **VCC1\_05\_PCH**
  - WR34 (150/41) to **VCC1\_05\_PCH**
  - WR33 (10K/41/X) to **VCC1\_05\_PCH**
  - WR21 (8.2K/4/X) to **3VDUAL**
  - WR20 (0/4/X) to **N\_SYS\_RST**
- CPU\_VTT\_OR0** is connected to:
  - A\_THRMTRIP**
  - A\_PWR\_DEBUG**
  - A\_DBR**
  - A\_DDR\_COMP0**
  - A\_DDR\_COMP1**
  - A\_DDR\_COMP2**
  - A\_TESTFLOW\_1**
  - A\_TESTFLOW\_2**
  - A\_HSW\_CFG\_RCOMP**

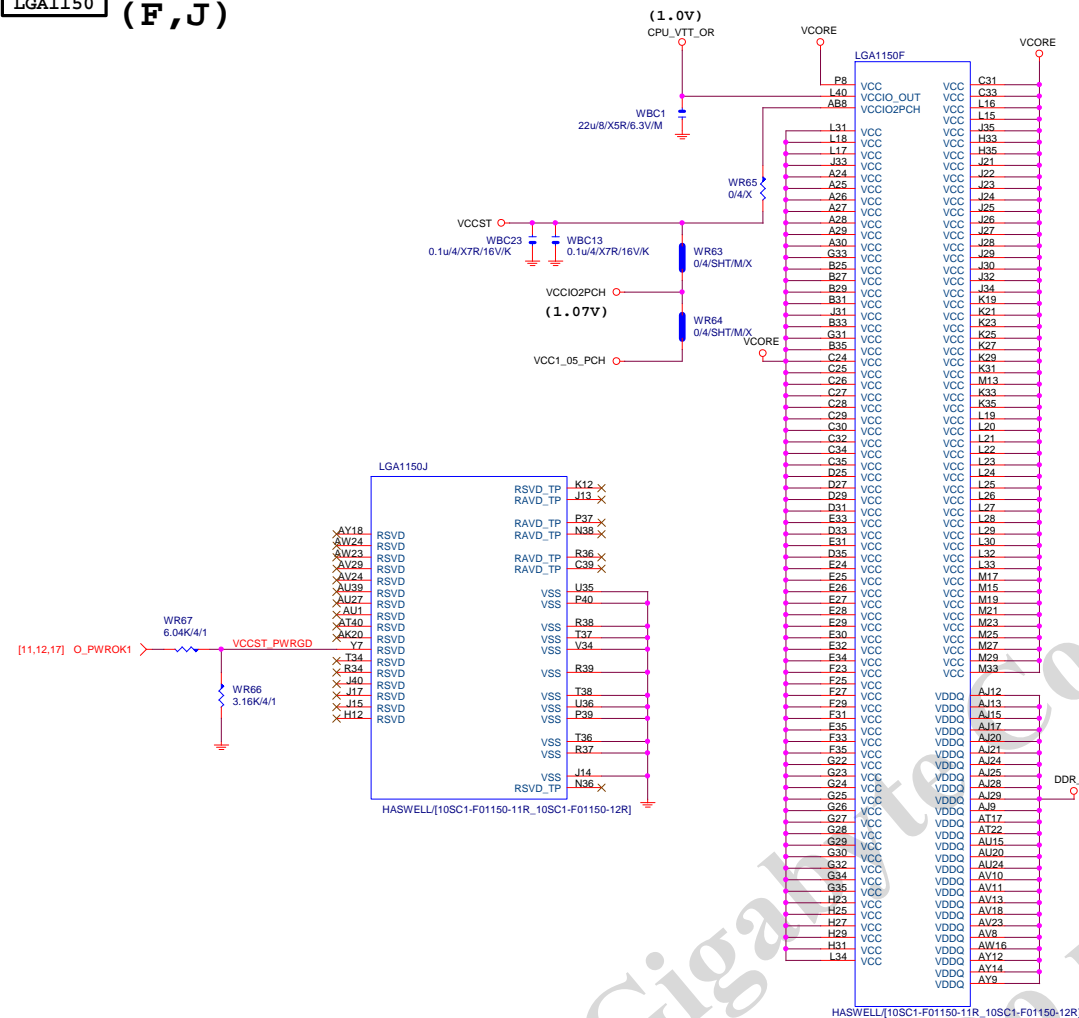
The legend at the bottom defines the pin names:

- A\_DDR\_COMP0**
- A\_DDR\_COMP1**
- A\_DDR\_COMP2**
- A\_TESTFLOW\_1**
- A\_TESTFLOW\_2**
- A\_HSW\_CFG\_RCOMP**

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CPU LGA1150-A			
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# LGA1150 (F,J)

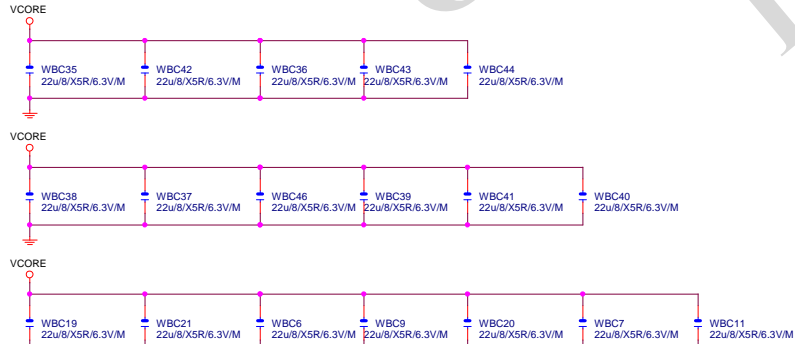


# LGA1155 (G,H,I)



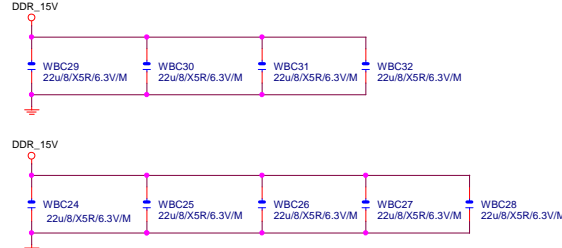
## VCore CAP

(X18)



## DDR CAP

(X9)

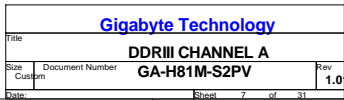


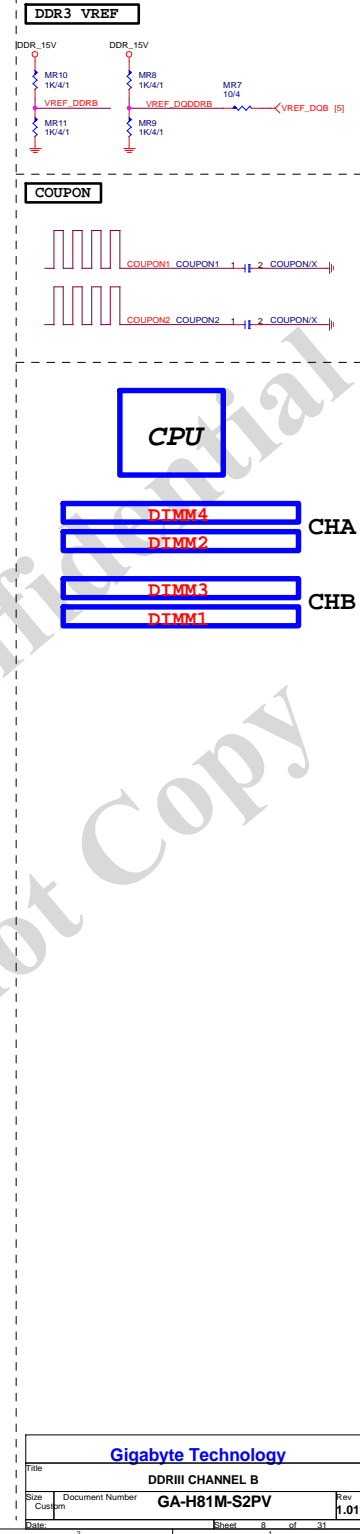
Gigabyte Technology

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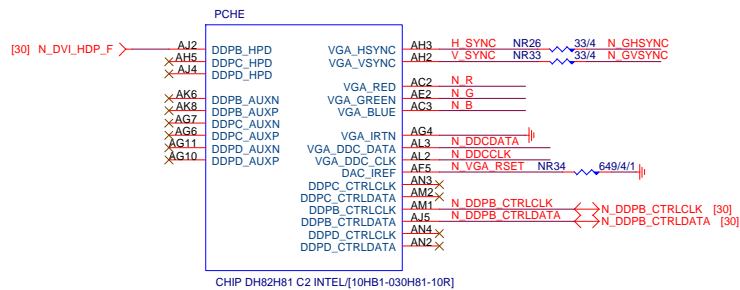
(A)



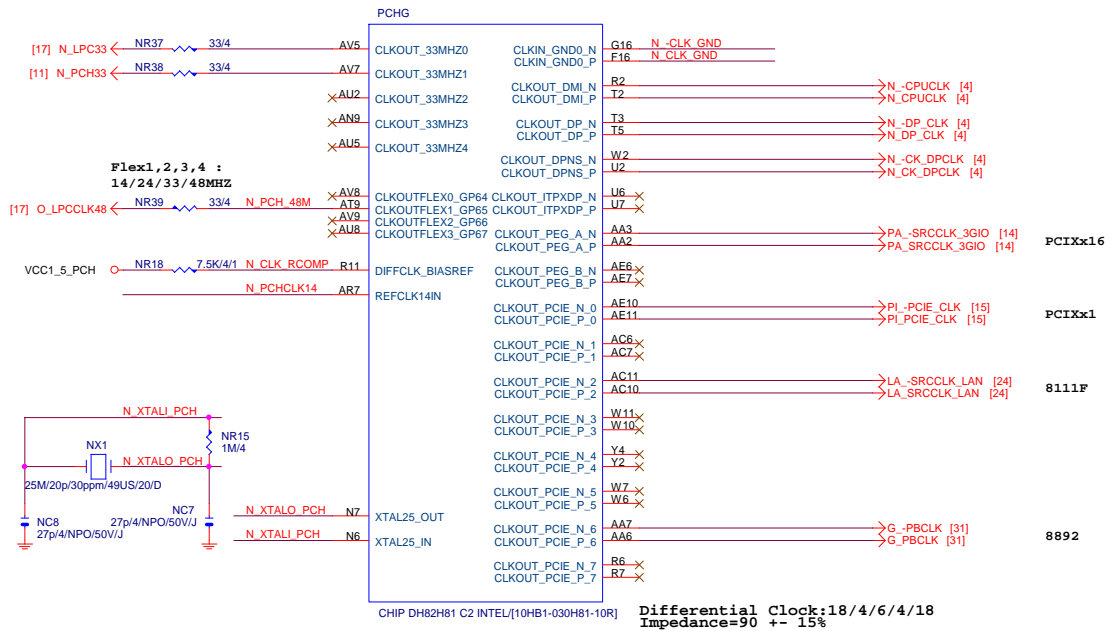




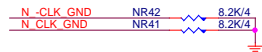
**PCH (E)**



**PCH (G)**



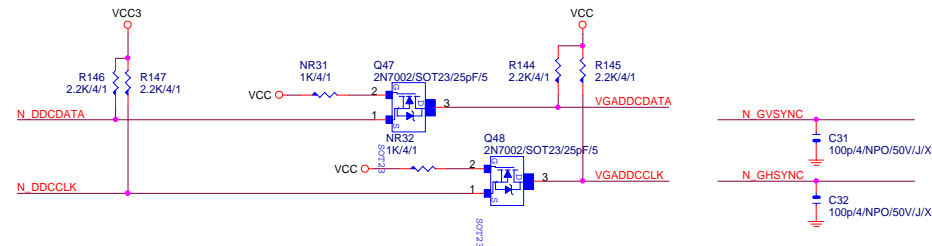
PCH CLK PD



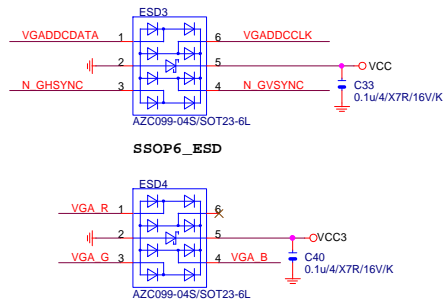
Mount for integrated clock Generation  
Mode



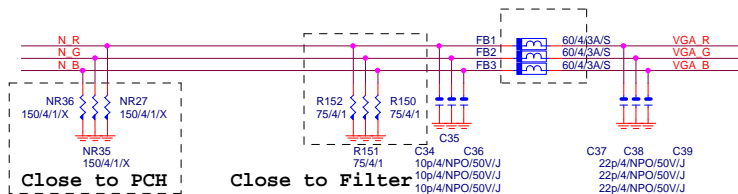
## VGA DDC



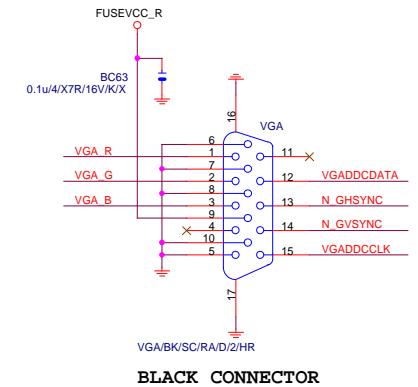
## VGA ESD



## VGA DDC



## VGA CONNECTOR



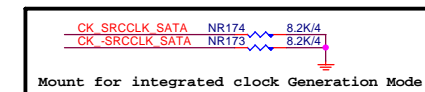
## Gigabyte Technology

### PCH DISPLAY ,CLK BUFFER

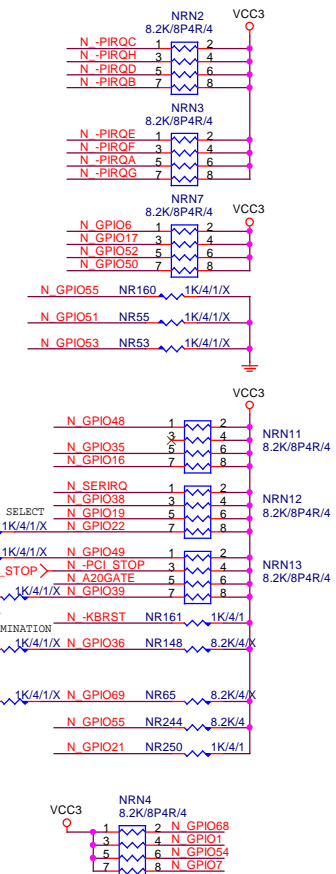
GA-H81M-S2PV

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SATA3 : 20/7.5/4.5/7.5/20 (breakout min 8/4/4/4/8)  
Impedance=90 +- 17.5%  
SATA2 : 15/7.5/4.5/7.5/15 (breakout min 8/4/4/4/8)  
Impedance=90 +- 17.5%



PCH	PU/PD
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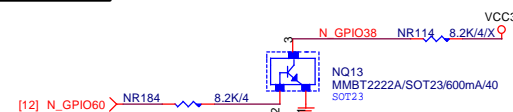
**SATA2\_2**  
SATA2/7/BK/H/OP/NA/D/1/B

**BLACK CONNECTOR**

**SATA2\_3**  
SATA2/7/BK/H/OP/NA/D/1/B

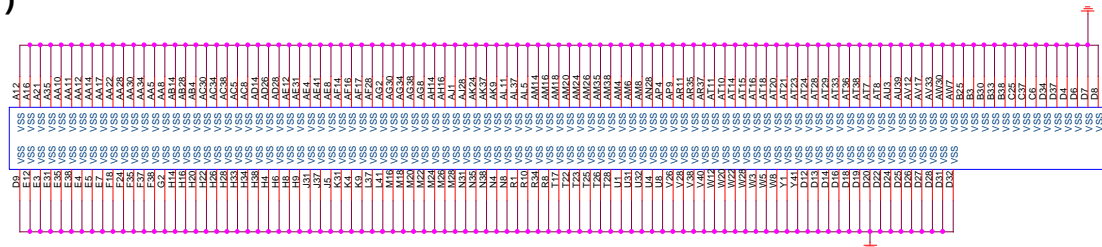
**BLACK CONNECTOR**

GPIO38 Ctrl

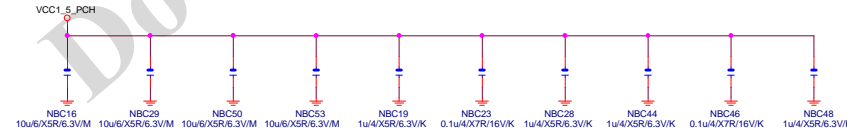
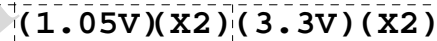
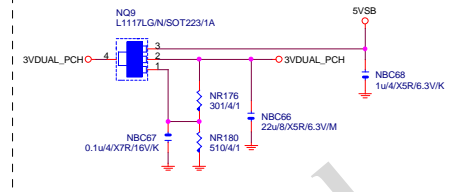




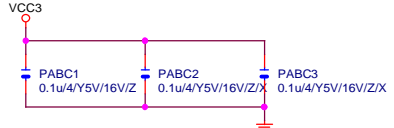
**PCH (I)**



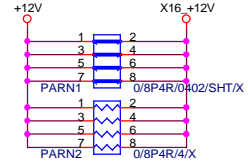
SHT PWR



PCIEX16 CAP



PCIEX16 PROTECT SHT

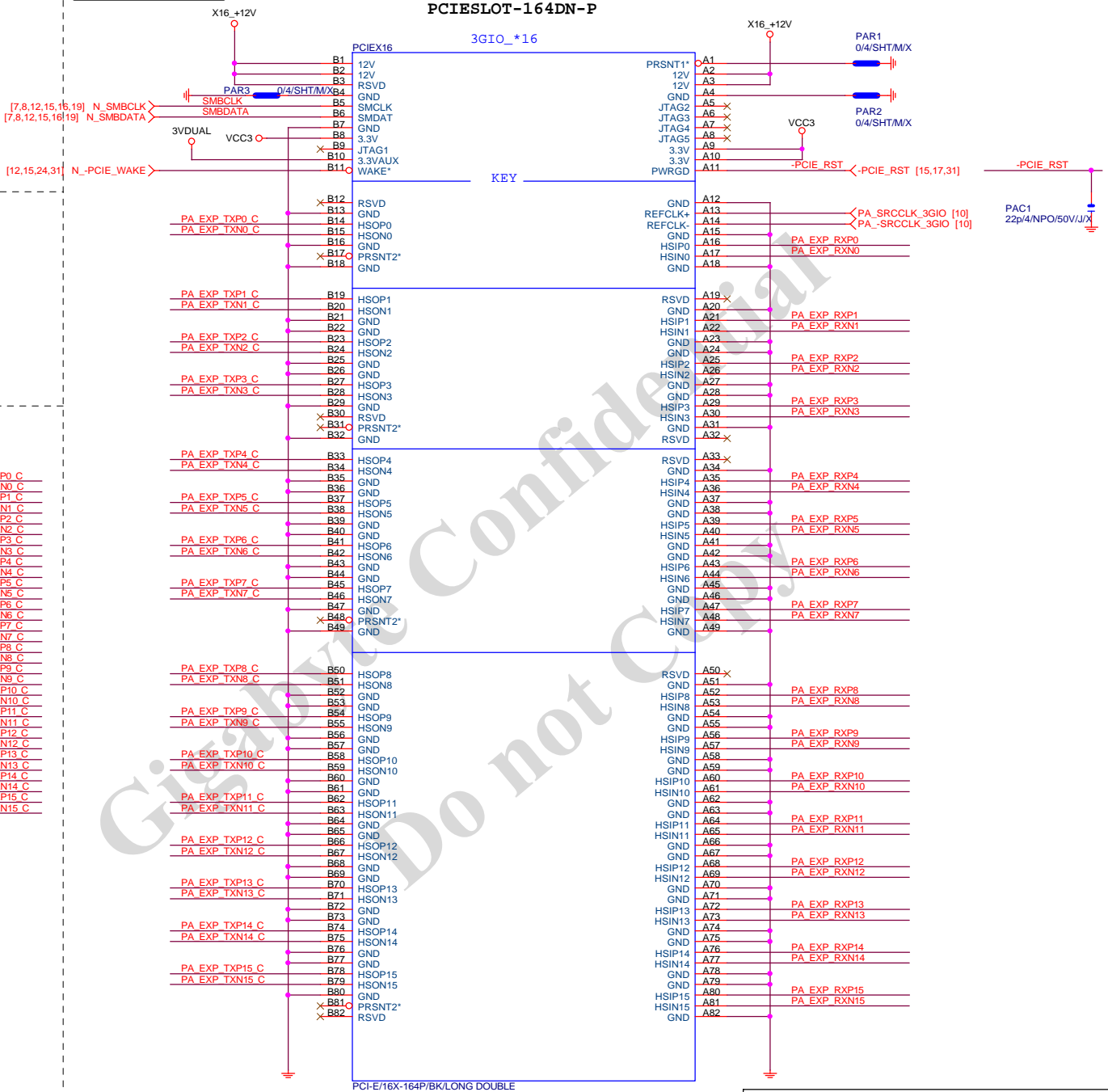


PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC19	0.22u4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC18	0.22u4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R/6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R/6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R/6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R/6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R/6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R/6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R/6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R/6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R/6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R/6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R/6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R/6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R/6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R/6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R/6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R/6.3V/K	PA EXP TXN15 C

PA EXP RXP0.[15] >>> PA\_EXP\_RXP[0..15] [4]  
PA EXP RXN0.[15] >>> PA\_EXP\_RXN[0..15] [4]  
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PA EXP TXN0.[15] >>> PA\_EXP\_TXN[0..15] [4]

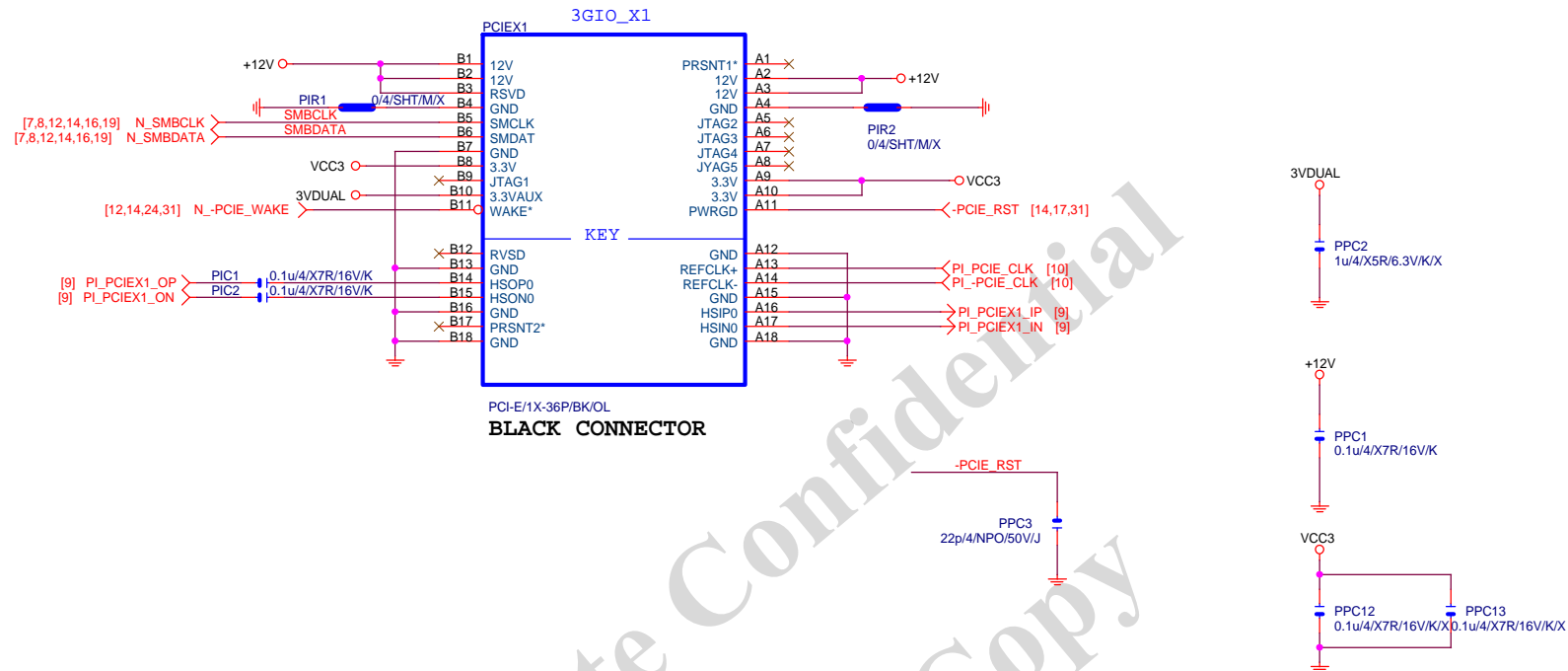
PCIEX16 SLOT



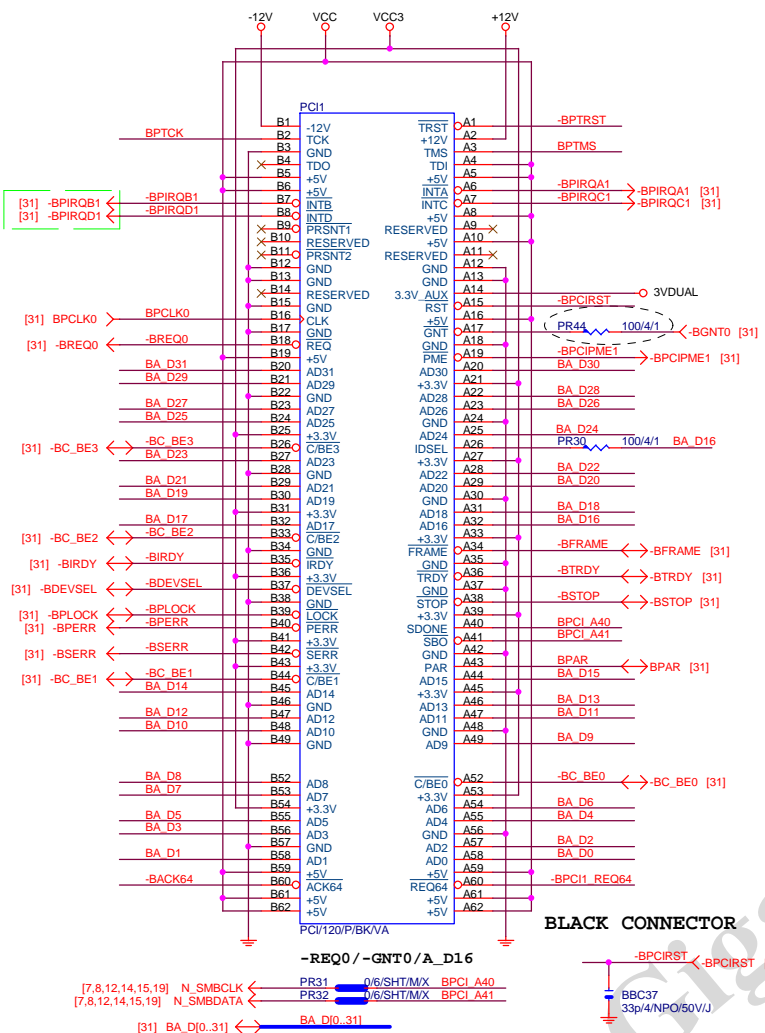
BLACK CONNECTOR

Gigabyte Technology		
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PCI EXPRESS * 16		
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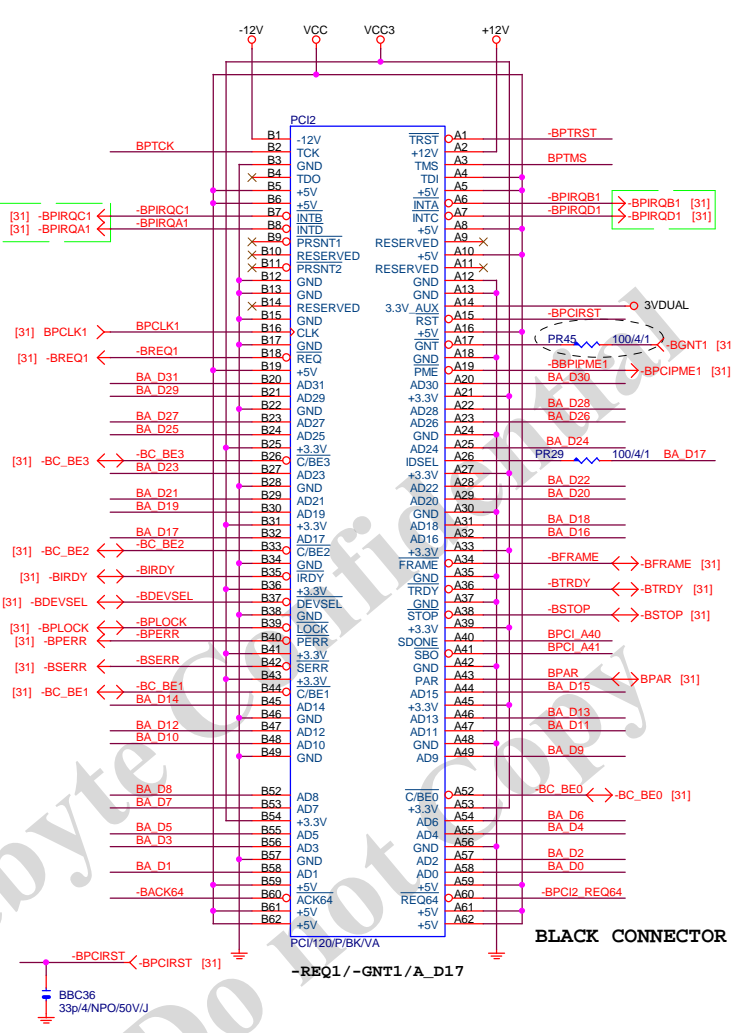
# PCIEX1 SLOT



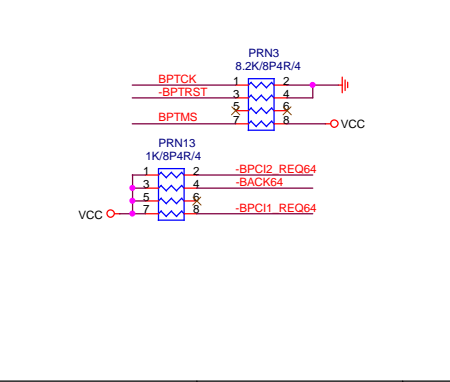
# PCI SLOT 1



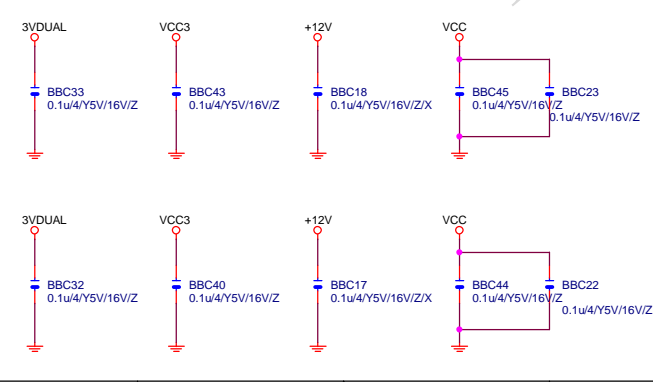
# PCI SLOT 2



# PCI PU

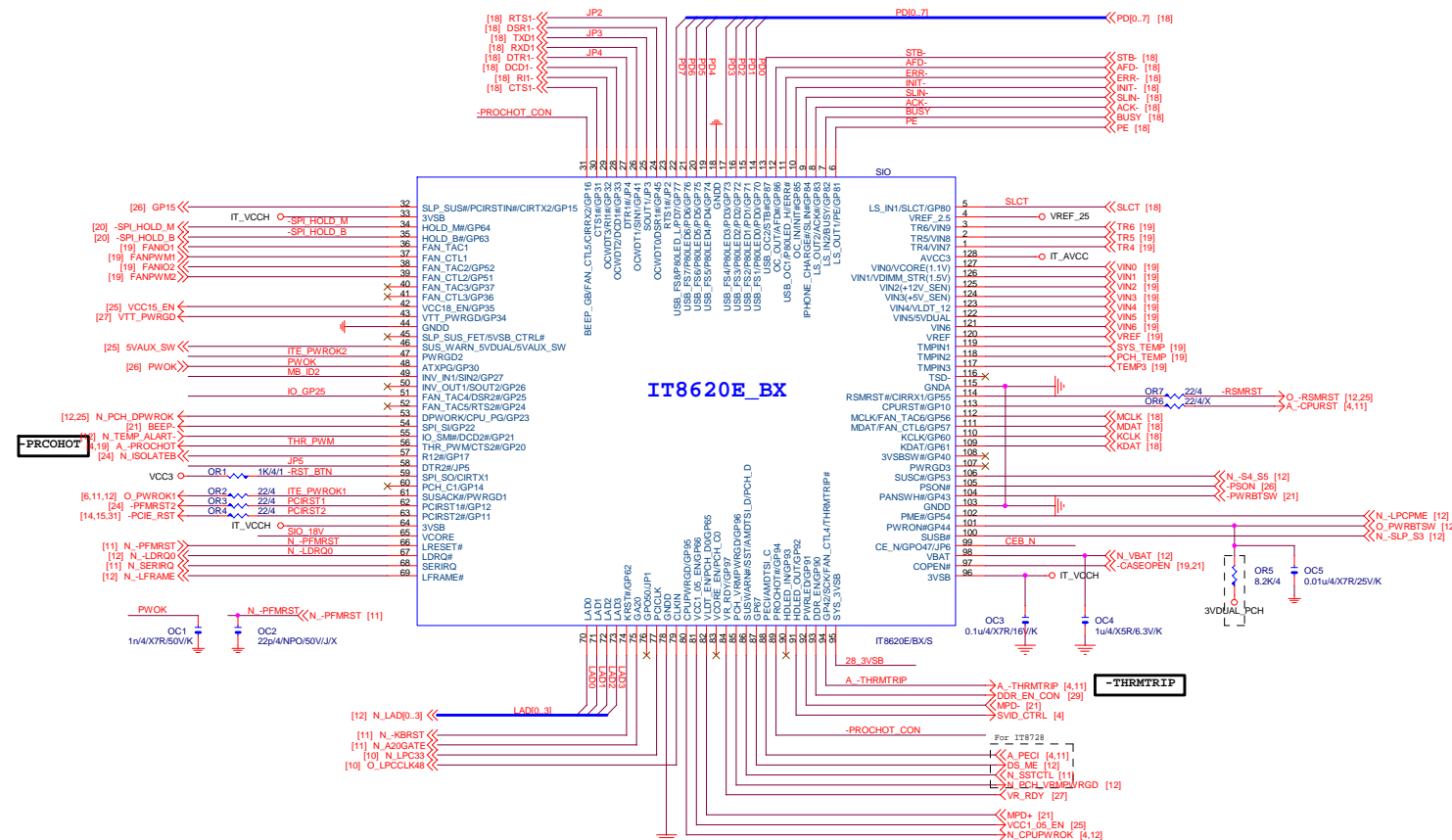


# PCI CAP

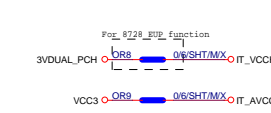


Gigabyte Technology			
Title			
PCI SLOT 1&2			
Size Custom			
Document Number			
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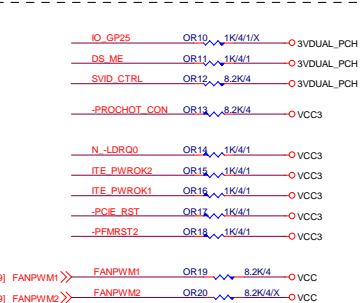
SIO IT8620



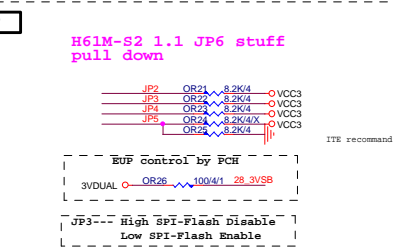
PWR SHT



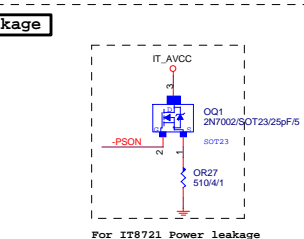
SIO PU



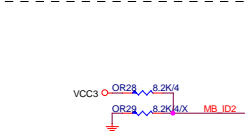
SIO STRAP



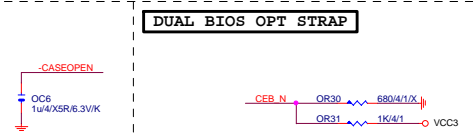
Power leakage



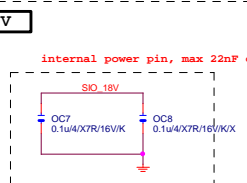
MB ID



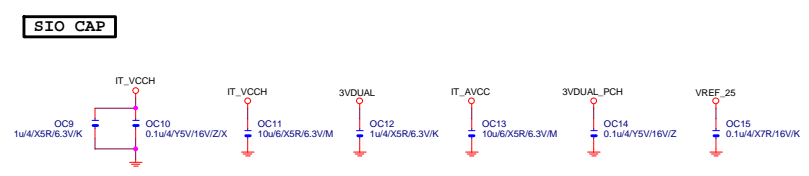
DUAL BIOS OPT STRAP



SIO 18V

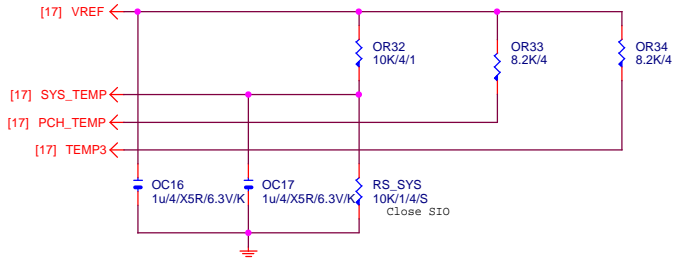


SIO CAP

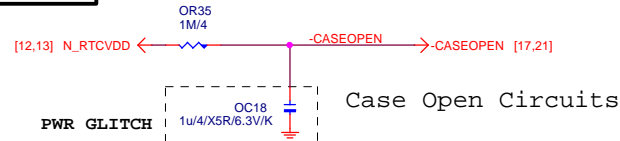




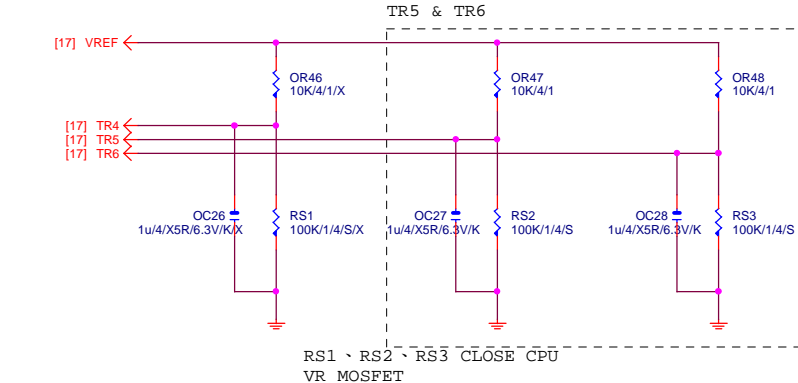
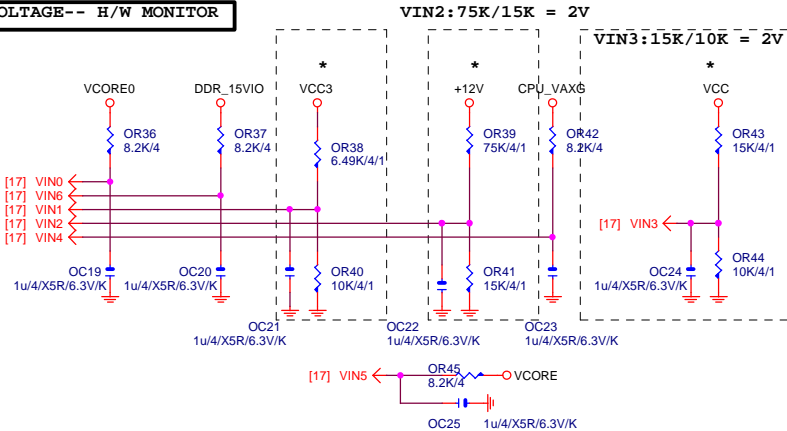
# TEMP H/W MONITOR



# CASE OPEN

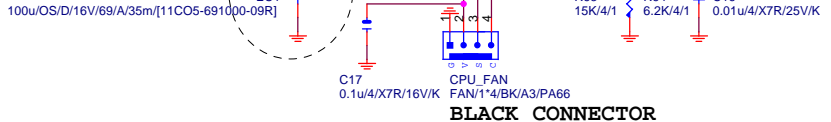


# VOLTAGE-- H/W MONITOR

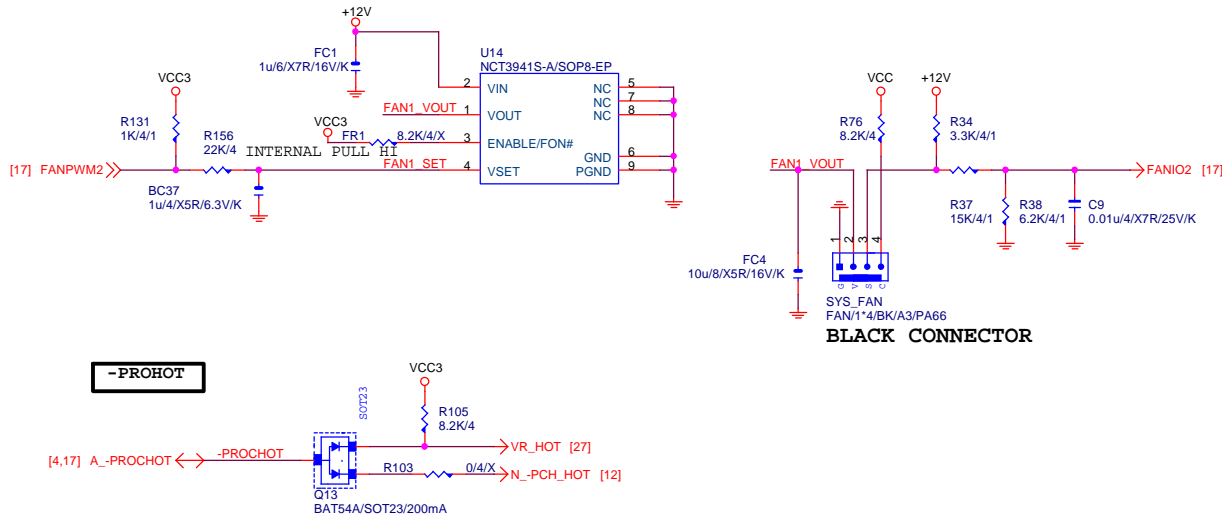


# CPU SMART FAN

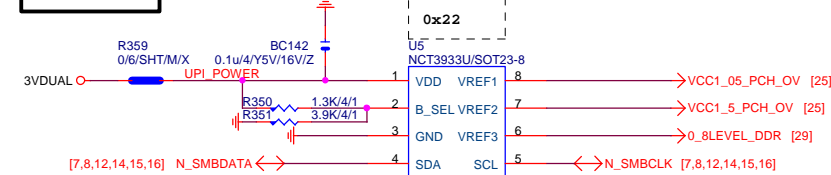
## FOR HOT-PLUG ISSUE

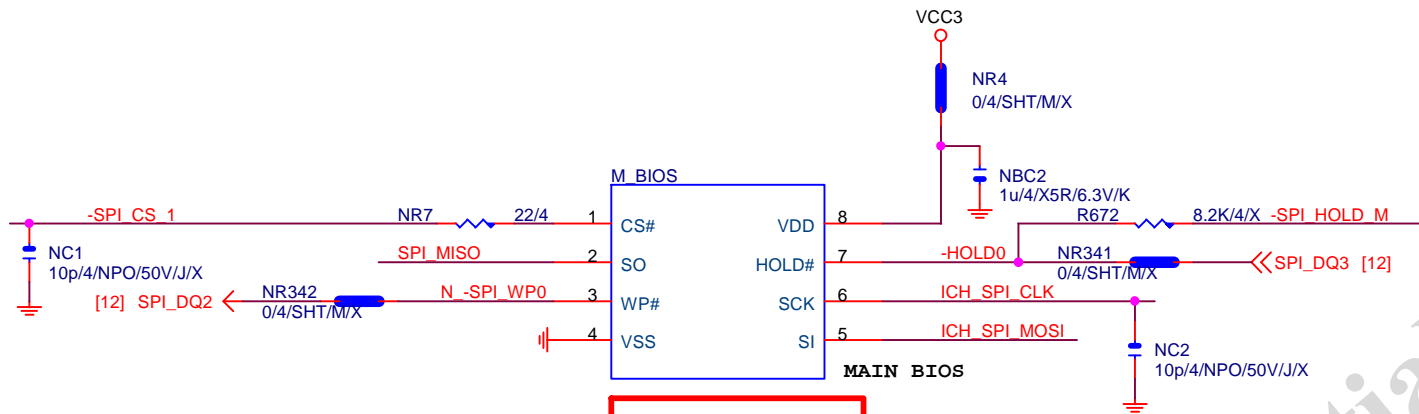


# SYS SMART FAN

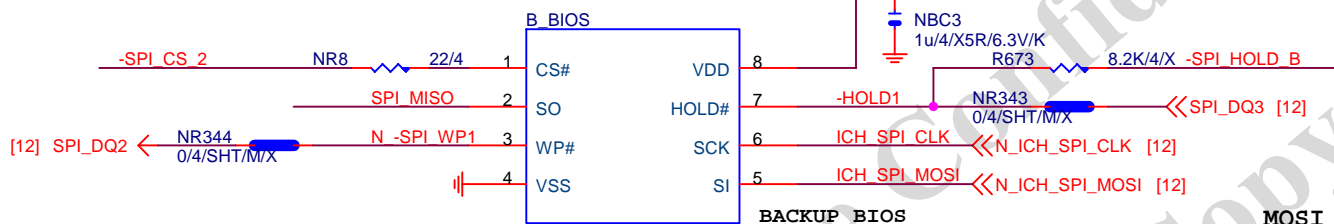


## OV NCT3933





64M/Q/SPI/SO8/S

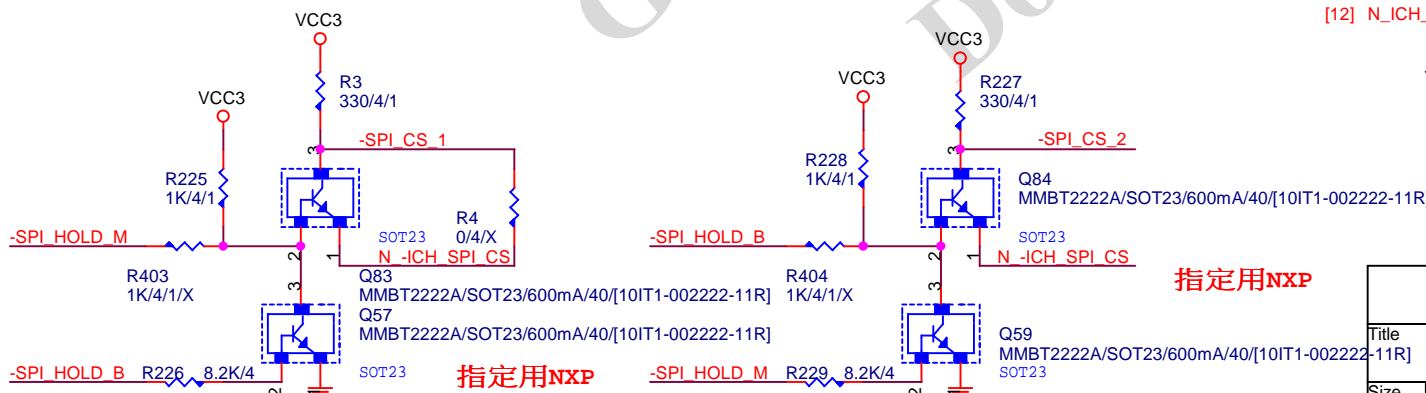
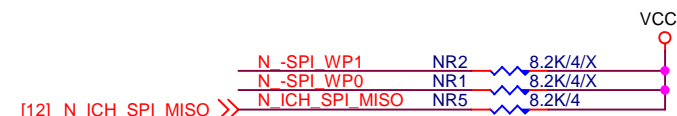
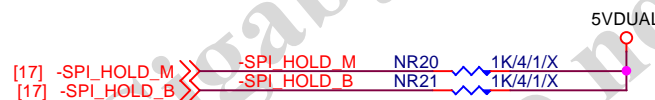
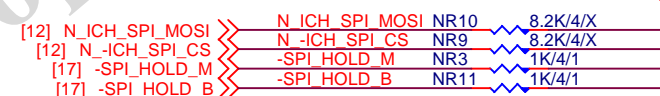


64M/Q/SPI/SO8/S

BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

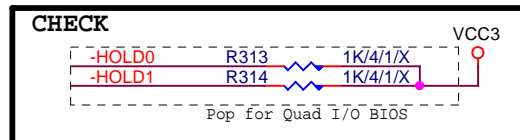
1 means floating  
0 means PD 1K

#### MOSI For DMI RX Termination Voltage



指定用NXP

指定用NXP



Gigabyte Technology

DUAL BIOS

GA-H81M-S2PV

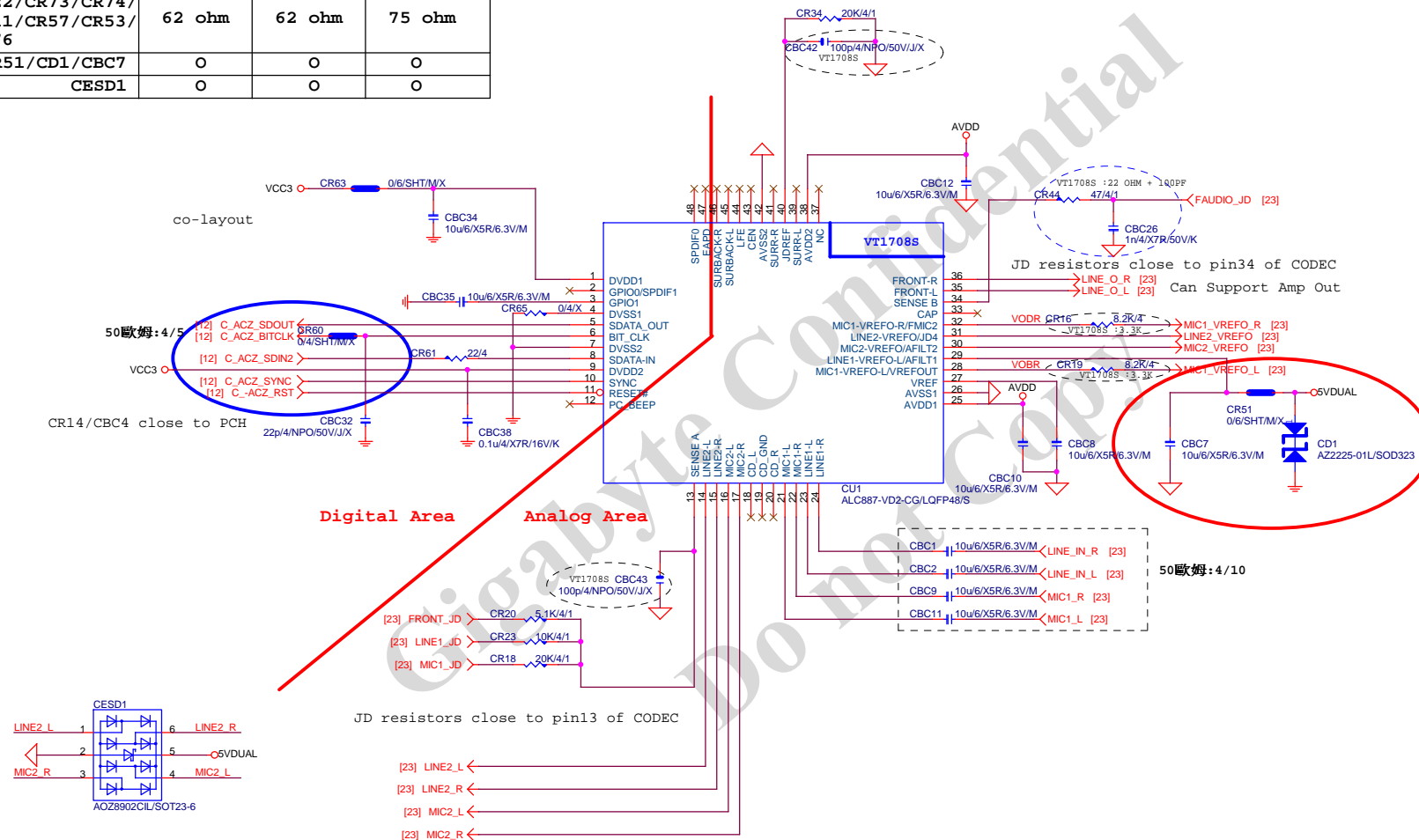
Rev 1.01

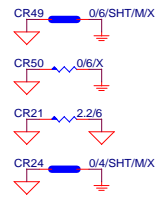
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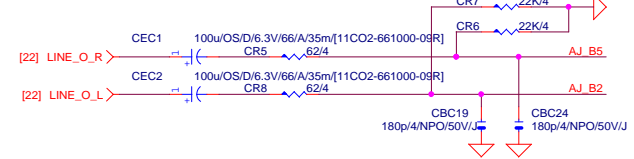
AZALIA CODEC ALC892/ALC887-VD2/VT1708-CE Colay

	ALC892	ALC887-VD2	VT1708S-CE
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P
CBC42/CBC43	X	X	100P/4
CR6/CR7/CR58/CR54/ CR67/CR68/CR69/CR70	22K/4	22K/4	10K/4/1
CR5/CR8/CR1/CR14/ CR17/CR22/CR73/CR74/ CR13/CR11/CR57/CR53/ CR75/CR76	62 ohm	62 ohm	75 ohm
CR51/CD1/CBC7	O	O	O
CESD1	O	O	O





## LINE-OUT



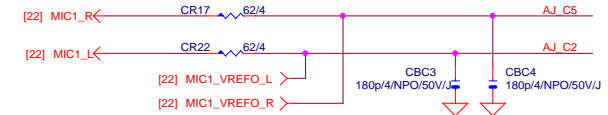
Only reserved for ALC888

## LINE-IN

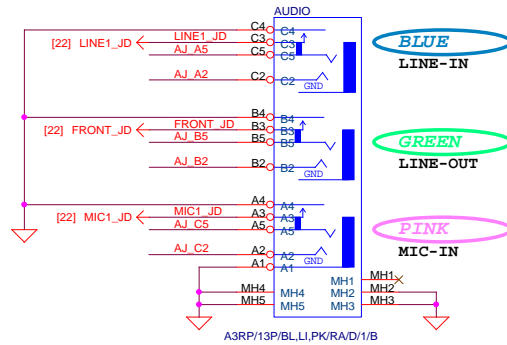
Verify MIC function  
in LINE-in

For 889A/888

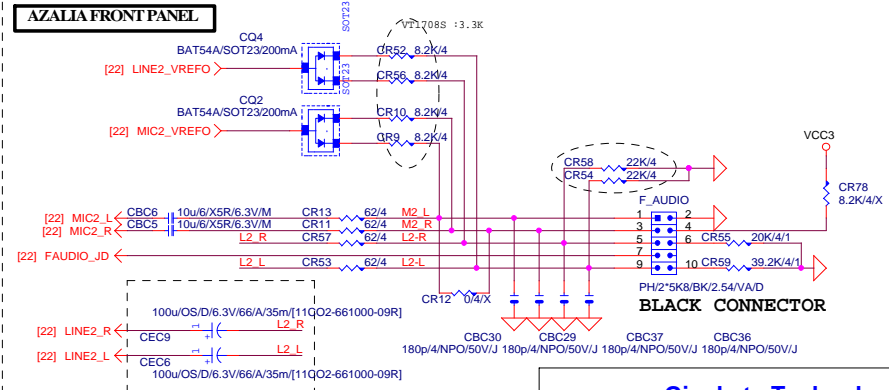
## MIC-IN



## SPDIF\_OUT

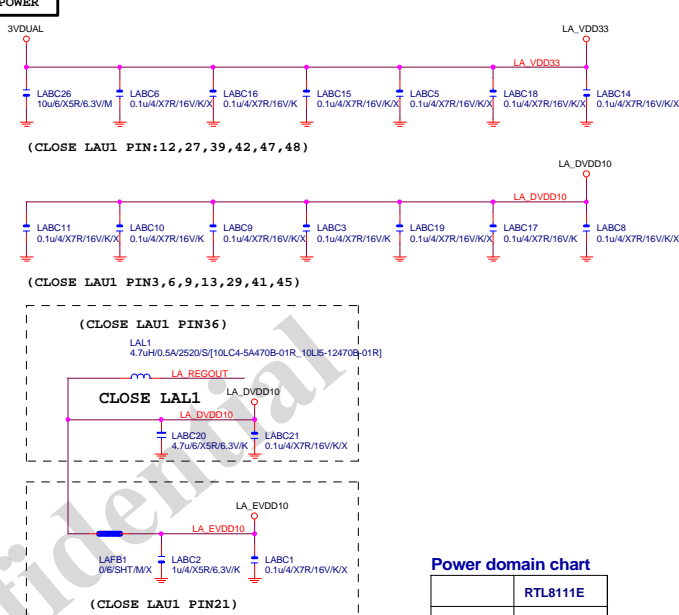
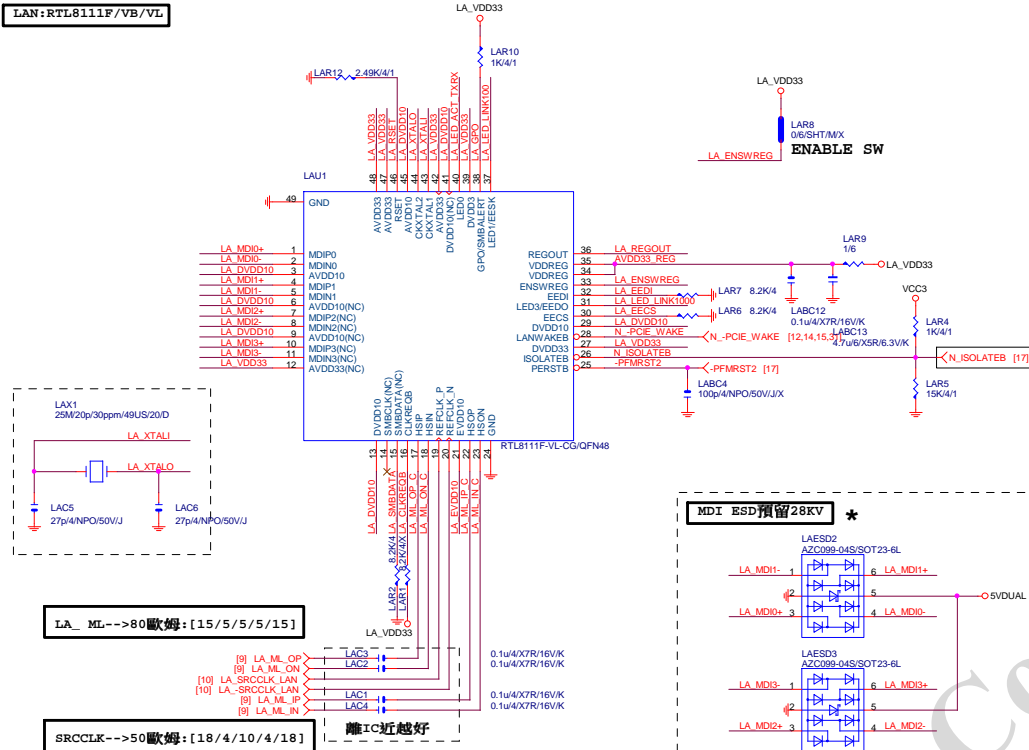


## AZALIA FRONT PANEL



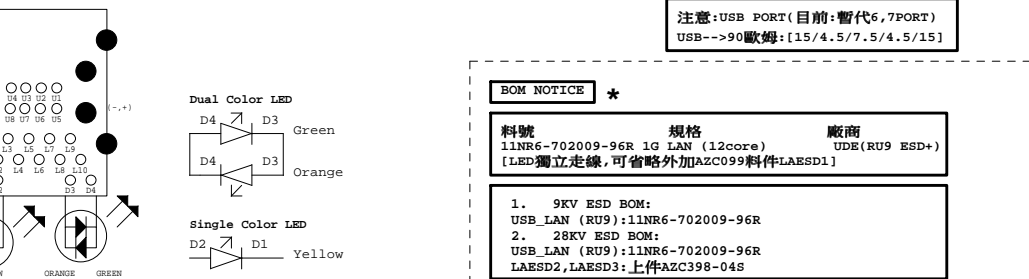
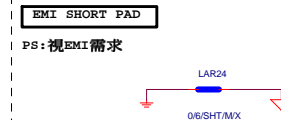
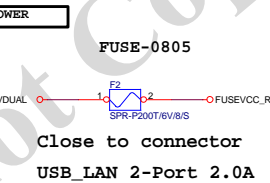
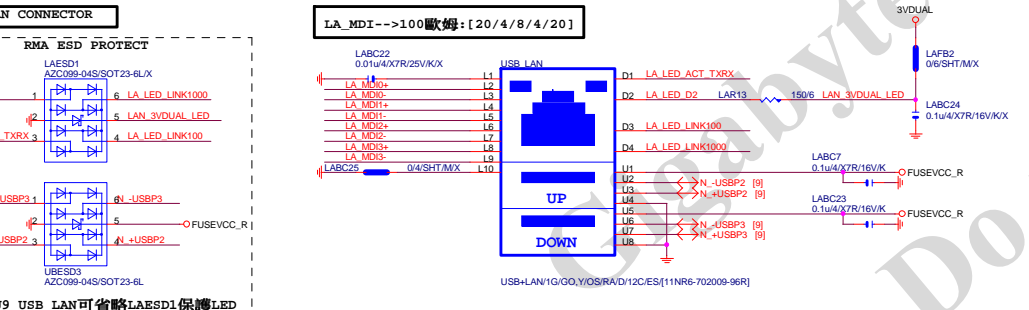
Gigabyte Technology

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AUDIO JACK		
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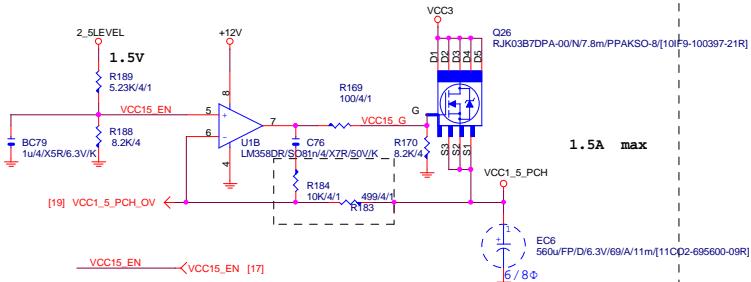
### Power domain chart

	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V

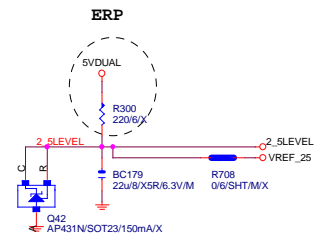


<b>Gigabyte Technology</b>			
Title			
<b>Realtek RTL8111G</b>			
Size	Document Number	<b>GA-H81M-S2PV</b>	Rev
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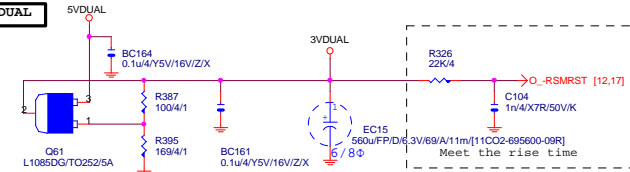
## VCC1\_5\_PCH



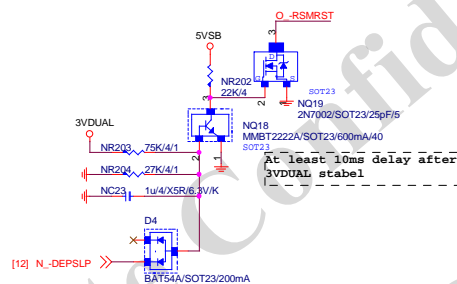
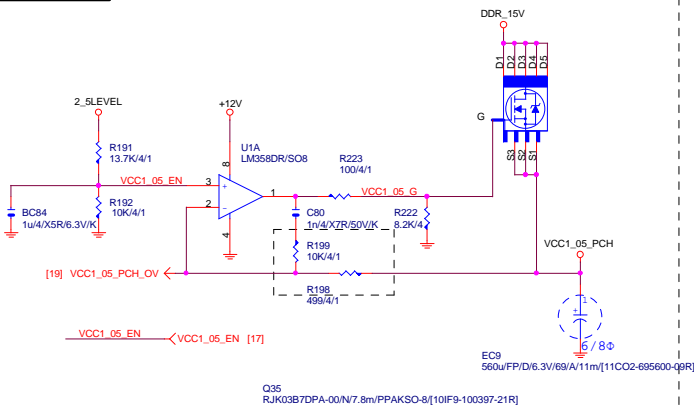
## 2\_5LEVEL



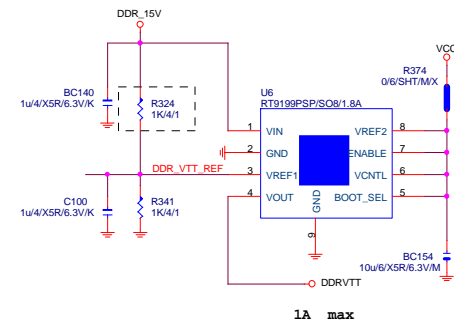
## 3VDUAL



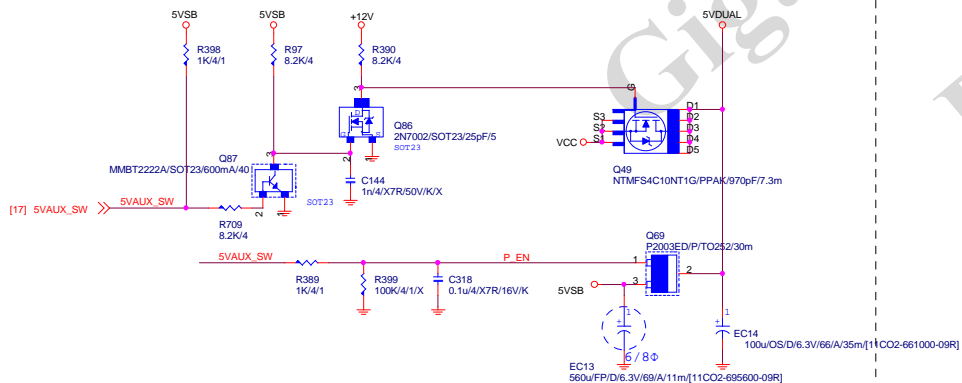
## VCC1\_05\_PCH



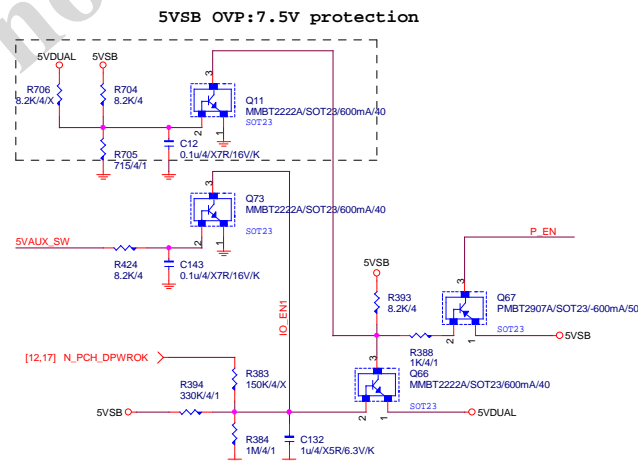
## DDRVTT



## 5VDUAL

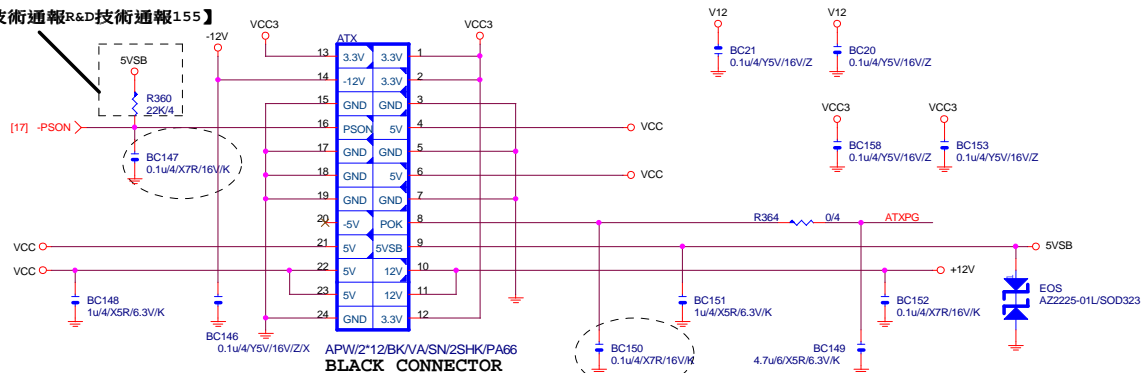


## 5VDUAL SHORT PROTECT

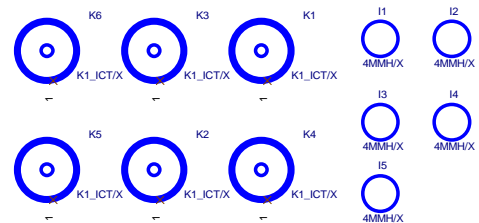
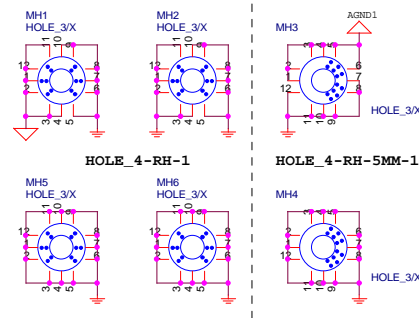


# ATXX24 POWER CONNECTOR

【技術通報R&D技術通報155】



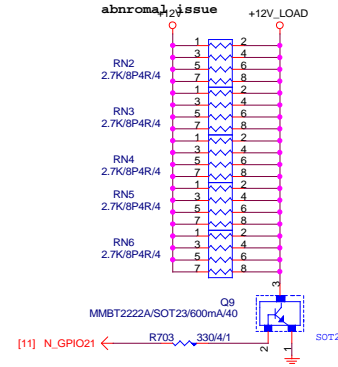
BLACK CONNECTOR



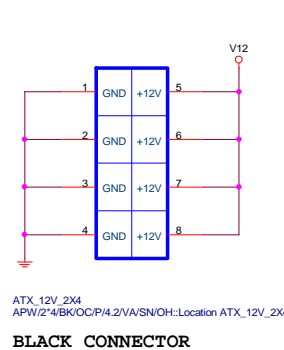
To prevent the 5VSB under loading when boot

【技術通報R&D技術通報153】

To fix 12V light load abnormal issue



# ATXX4 POWER CONNECTOR

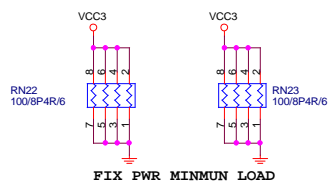
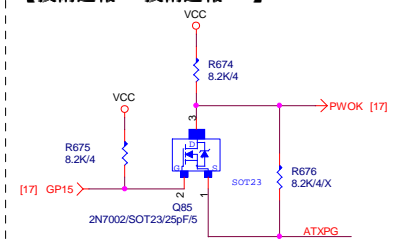


ATX\_12V\_2X4  
APW/2'4BK/OC/P/4.2/V/A/SN/OH:Location ATX\_12V\_2X4

BLACK CONNECTOR

# PWOK PATCH

【技術通報R&D技術通報154】



FIX PWR MINMUN LOAD

Gigabyte Technology

ATX CONNECTOR

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R_PROG1 (Kohm)	3-Phase Iccmax(A)
24.9	105
28.7	114
34.0	129
42.2	144

R_PROG2 (Kohm)	Fsw(KHz)	VBOOT
64.9	315	1.75
73.2	315	1.70
80.6	315	1.65
90.9	315	0

R_PROG3 (Kohm)	Fast Slew Rate (mV/us)
3.24	12
5.76	24
9.31	40
13.3	45

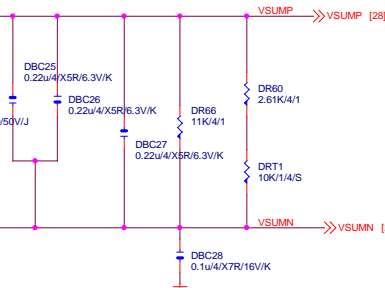
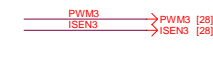
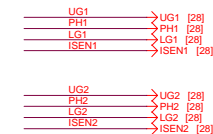
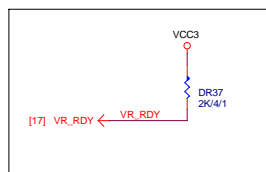
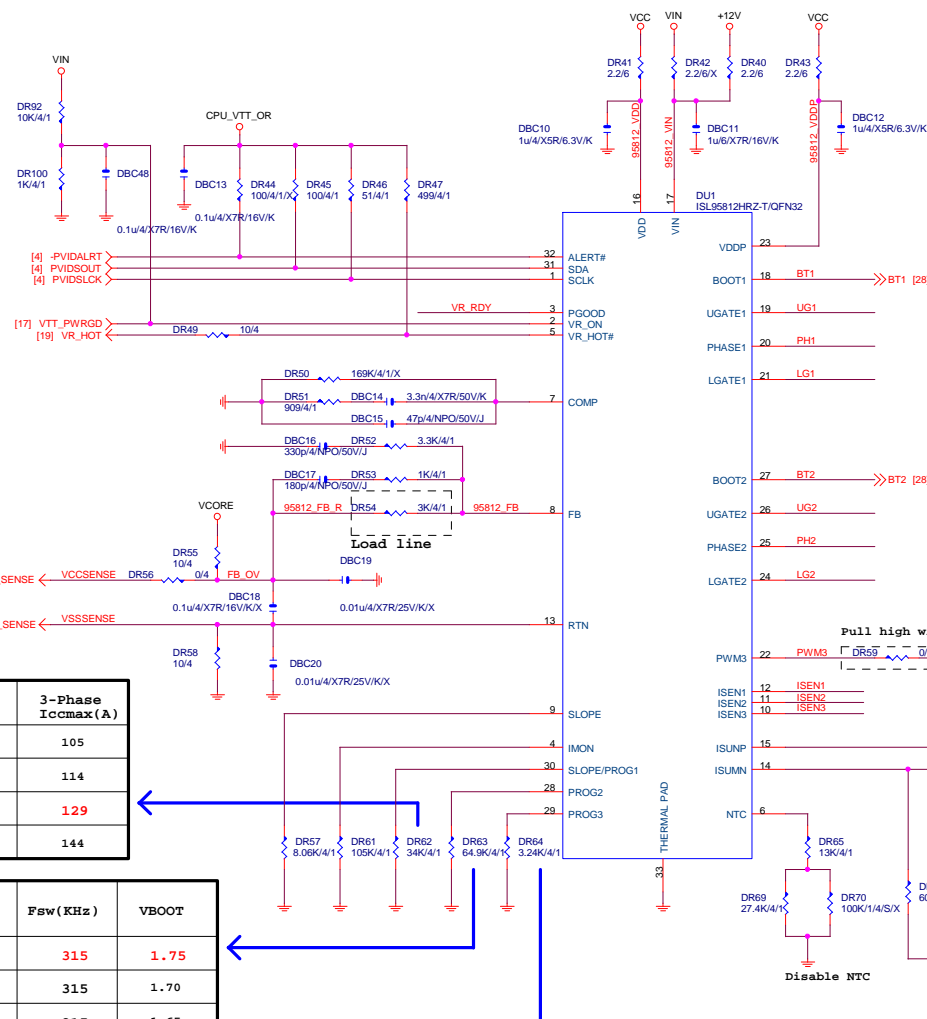
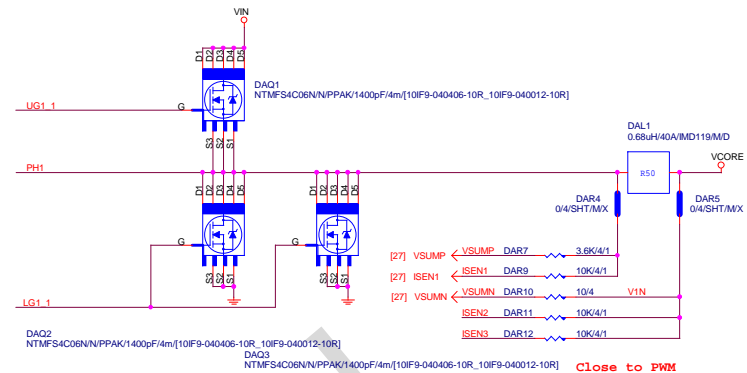


Diagram illustrating a signal path with three input lines (UG1, PH1, LG1) and three output lines (UG1, PH1, LG1). The output lines are labeled with a delay of 27%.



PWM3 → PWM3 [27]

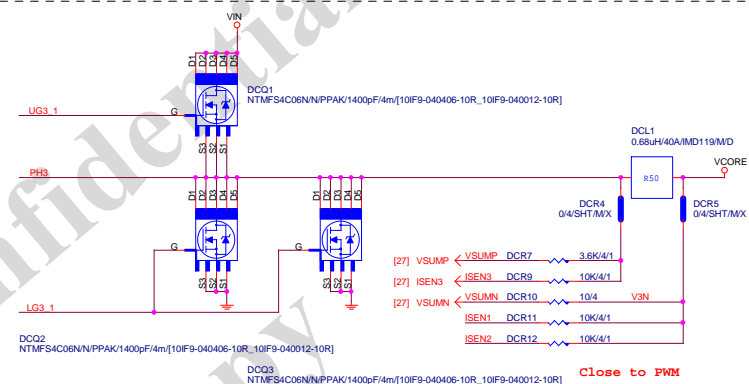
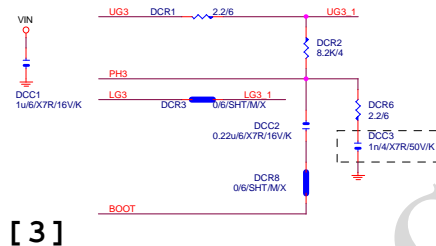
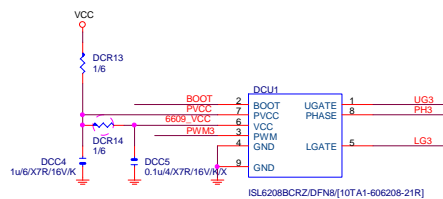
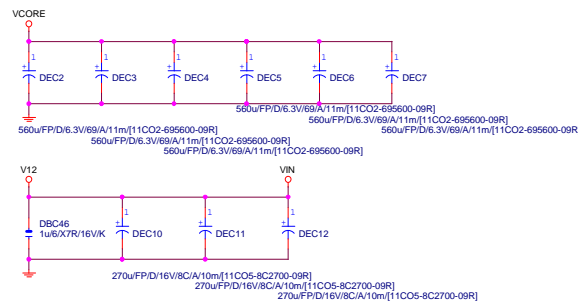
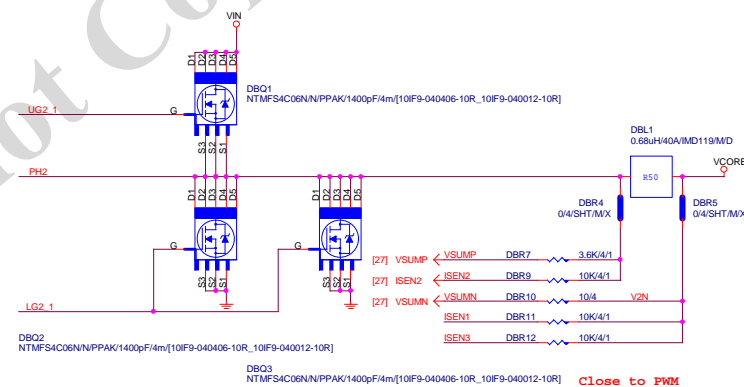
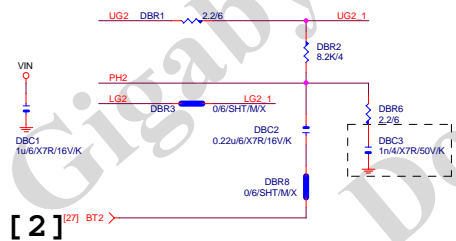
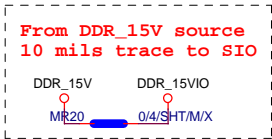


Diagram illustrating the mapping of variables to their corresponding values in the context of the 27th slide:

- UG2 maps to UG2 [27]
- PH2 maps to PH2 [27]
- LG2 maps to LG2 [27]



DDR15V



PWR SEQ

$$\begin{aligned} \text{Rocset} &= (\text{Iocp} * \text{Lgate}, \text{rdson}) / \text{Iocset} \\ \text{Rocset} &= (45\text{A} * 6.7\text{mOhm}) / 10\text{uA} = 30\text{K} \\ \text{Iocset} &= 10\text{uA} \end{aligned}$$

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# DVI LEVEL SHIFT

