MS-7885

ATX

Ver: 31

Haswell-E Platform

CPU:

Haswell-E

System Chipset:

Wellsburg

Onboard Chip:

HD Audio Codec:ALC1150

LAN-Killer E2205

SIO:NTC6792D

Dual Flash ROM: SPI 64 MB X2

Main Memory:

*DDRIV (1666MHz) * 8 (Dual Channel)*

ACPI:

UPI

PWM:

VRD12.5 -ISL6388

Expansion Slots:

*PCI Express (X16) Slot * 2*

*PCI Express (X8) Slot * 1*

*PCI Express (X1) Slot * 5*

Other:

*SATA-EX *1*

*SATA3.0 *8*

*USB2.0 *8*

*REAL USB3.0 *8*

*FRONT USB3.0 *2*

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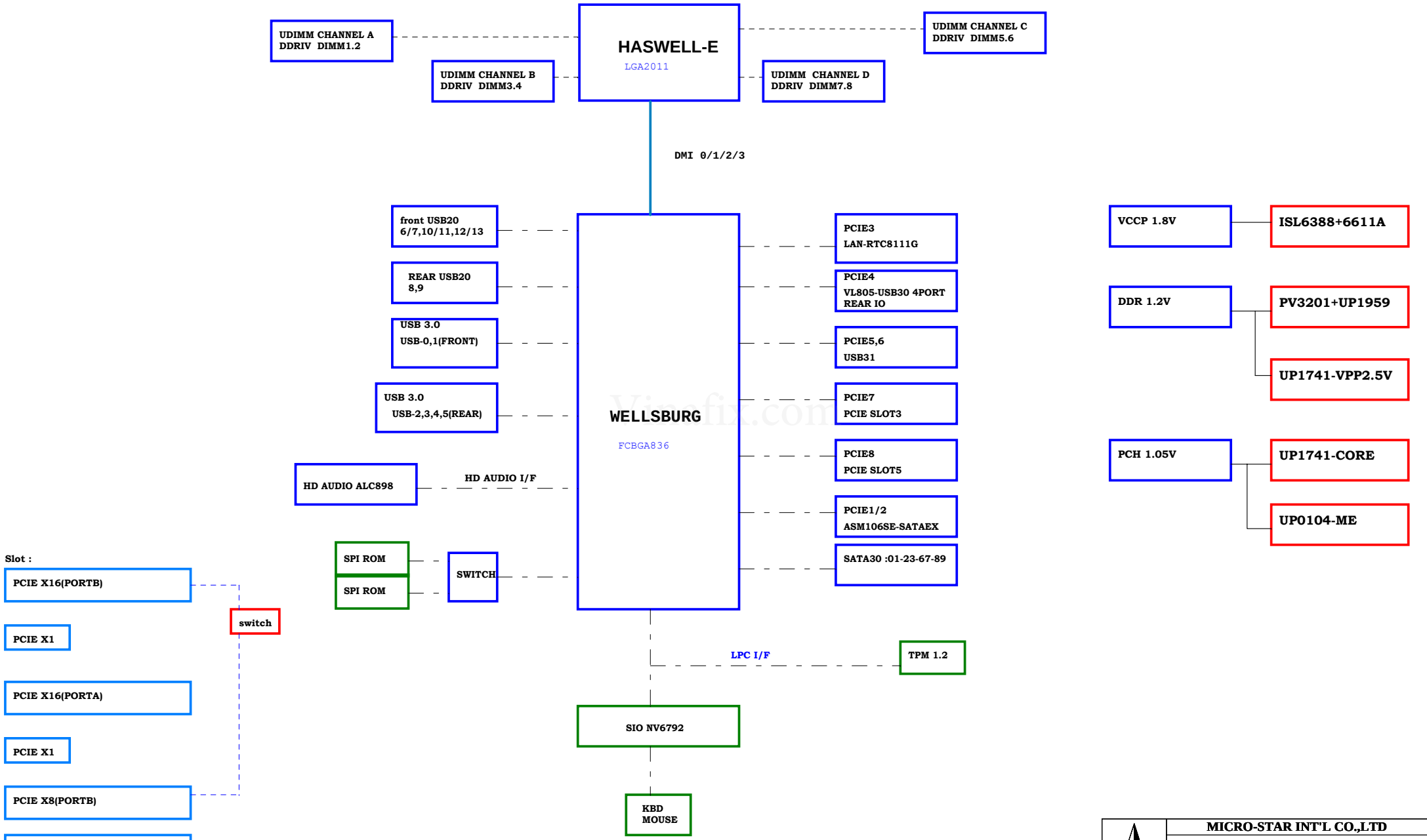
MS-7885 Block Diagram



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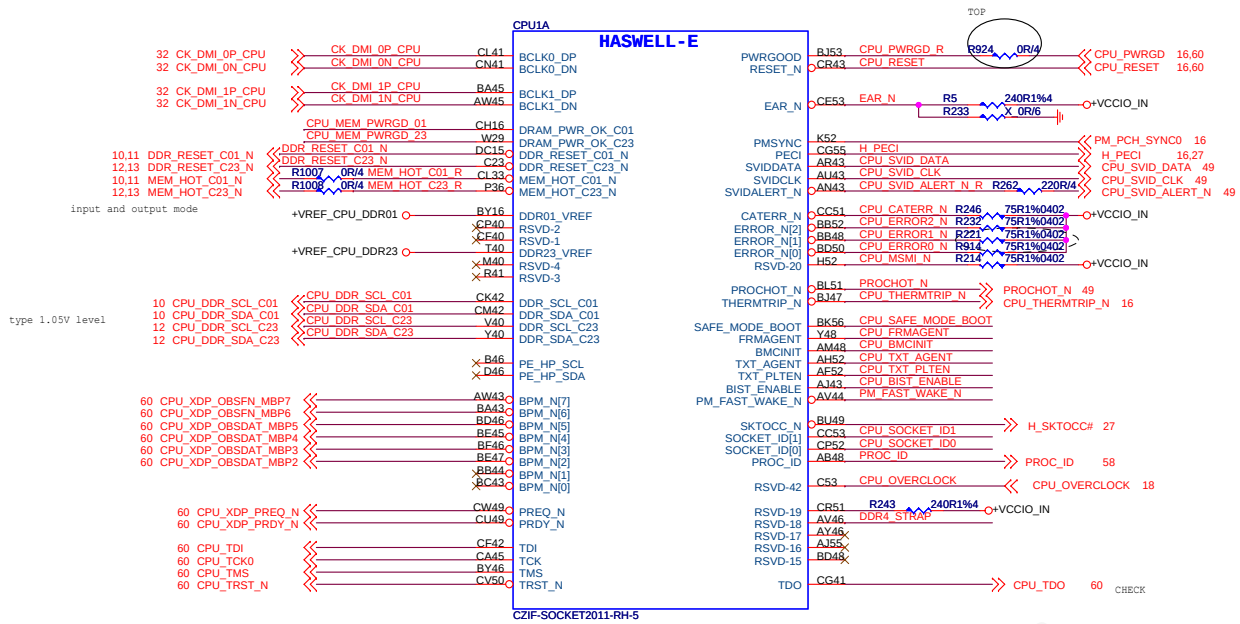
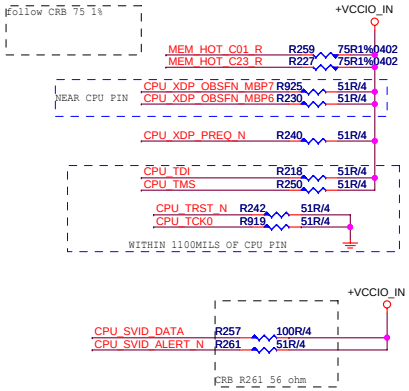
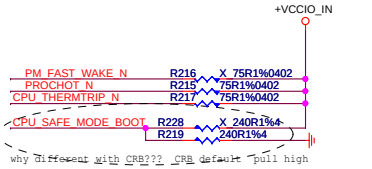
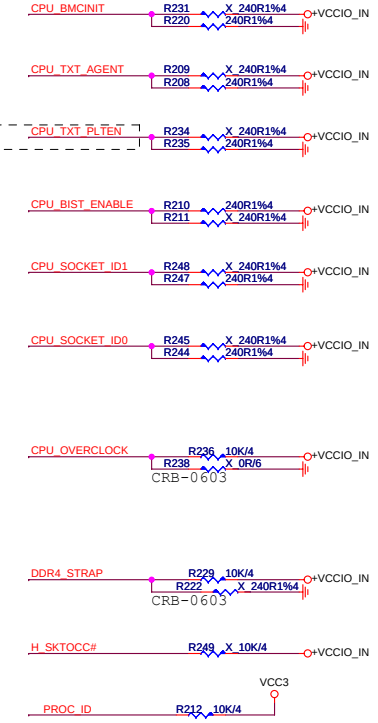
CPU-CLK/Control/MISC

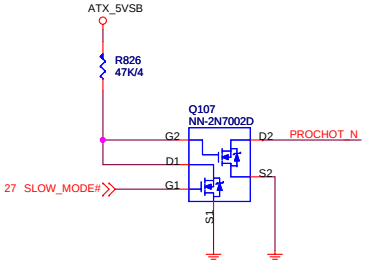
OR:R278 REMOVED

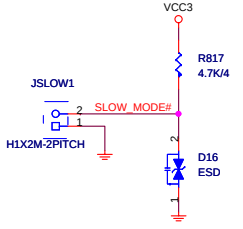


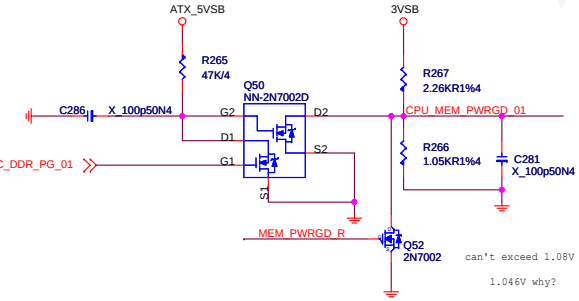


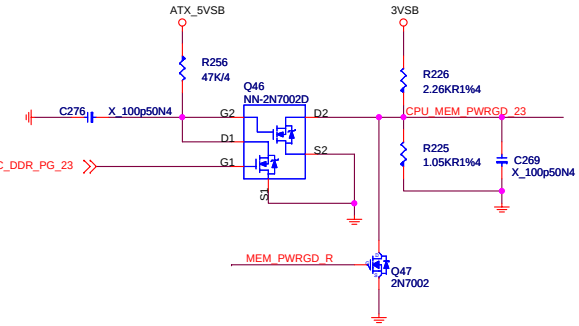


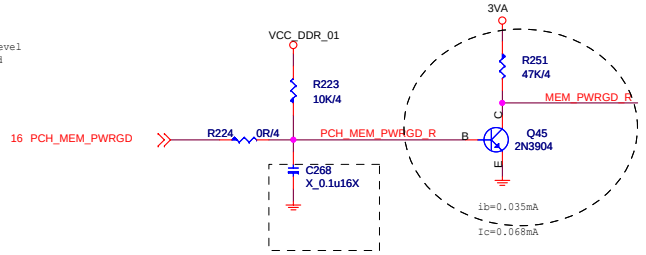












PROC_ID	+VCCIO_IN
0	0.95V
1	1.05V

Vinafix

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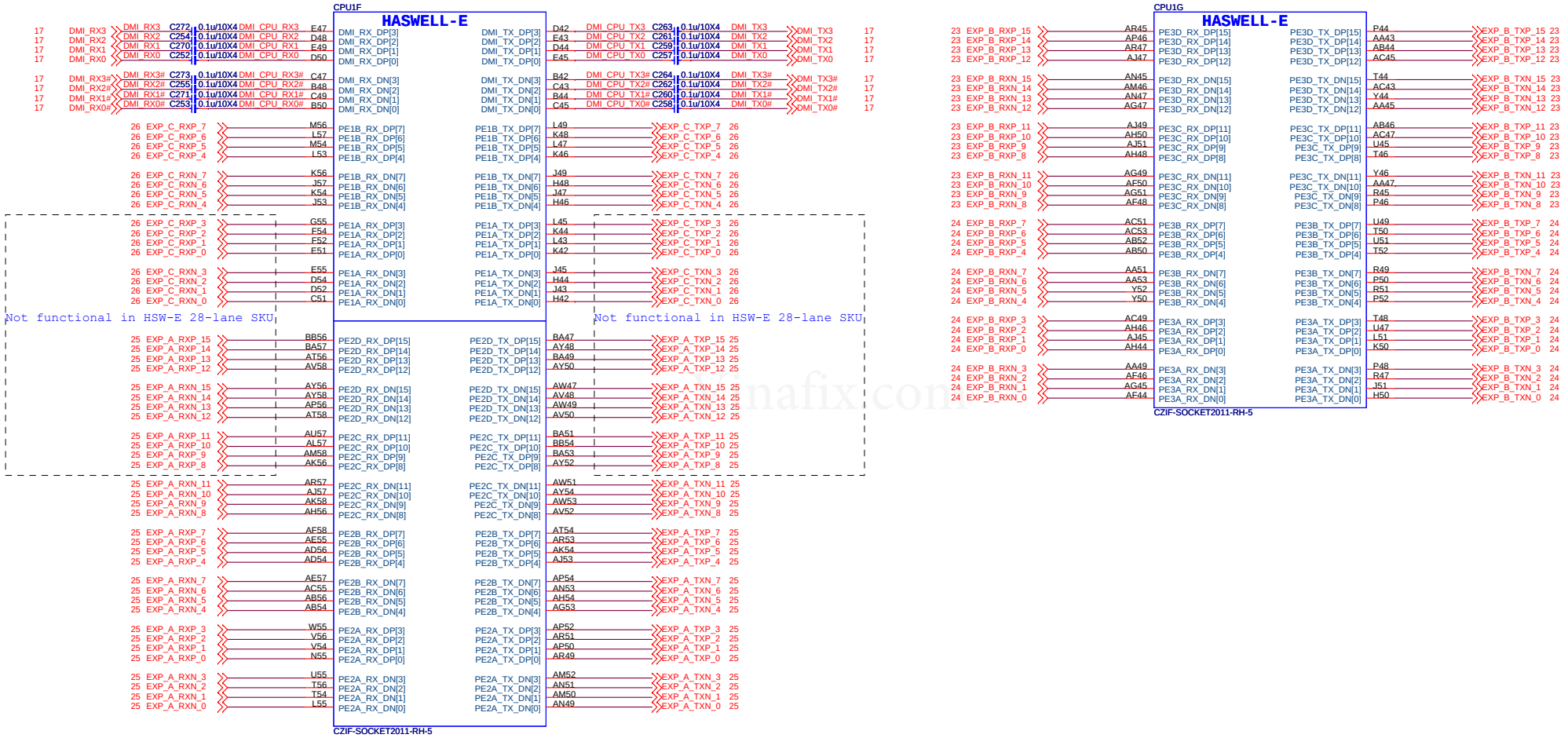
CPU-DMI/PEG



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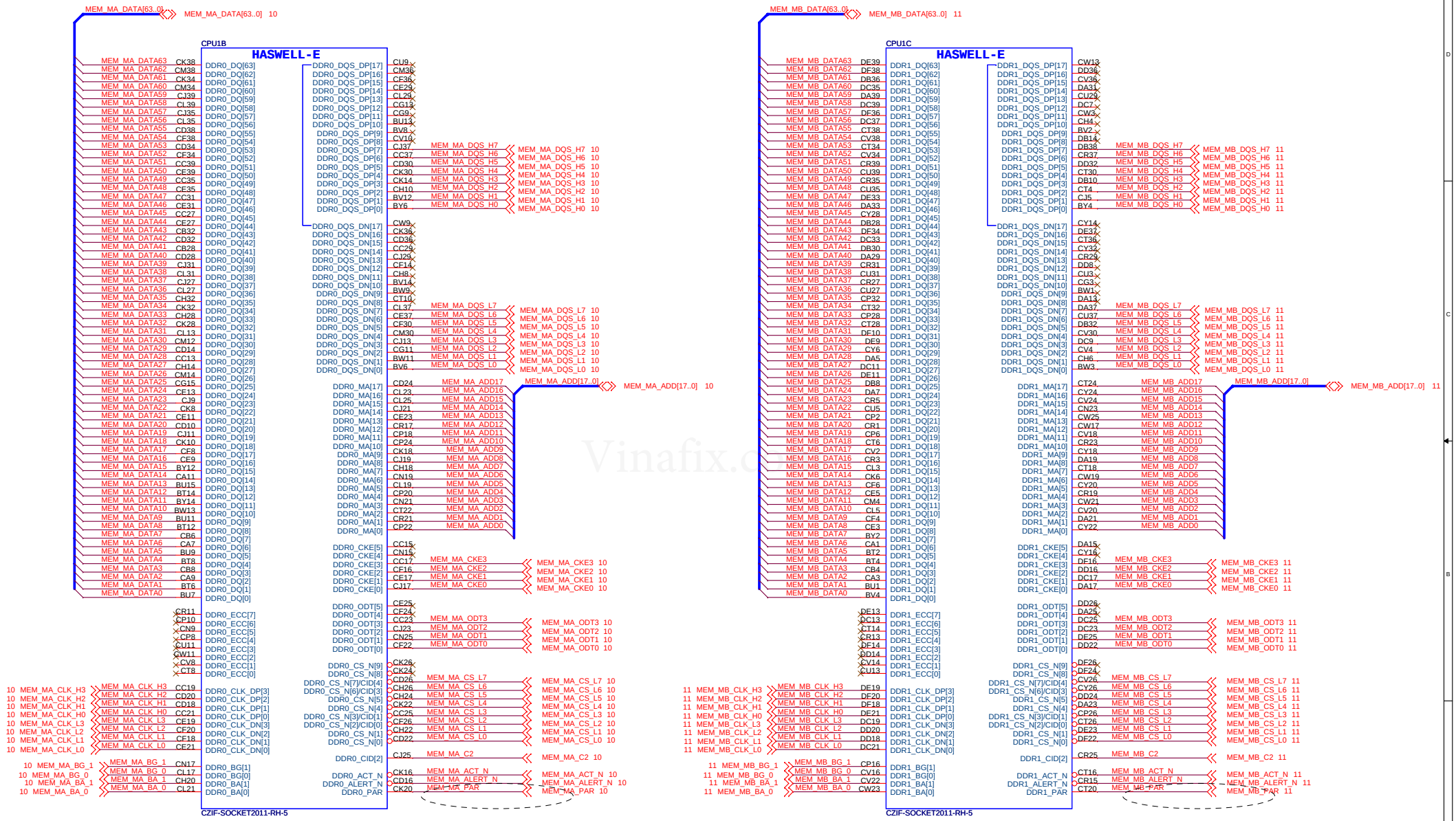
CPU-Memory0/1



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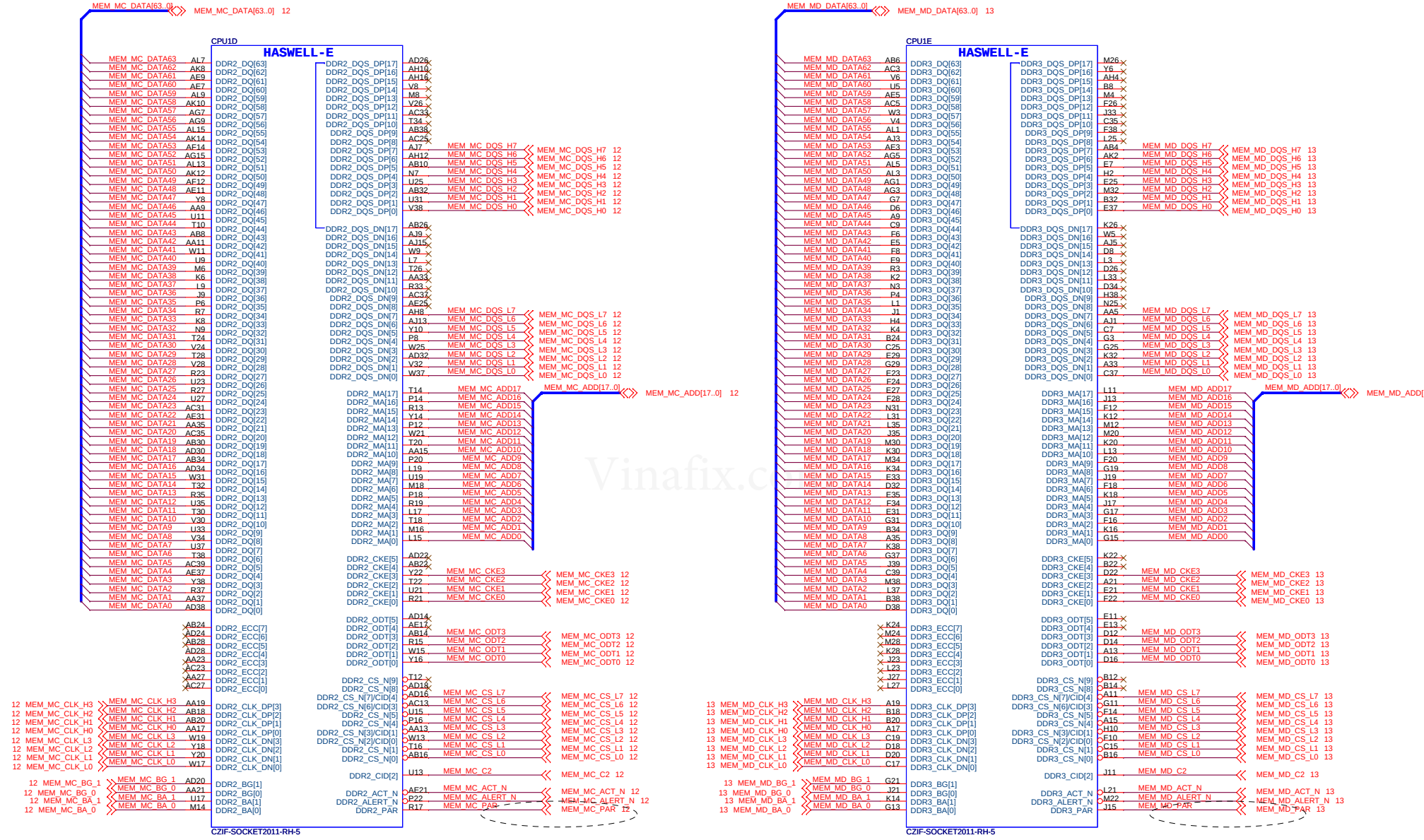
CPU-Memory2/3



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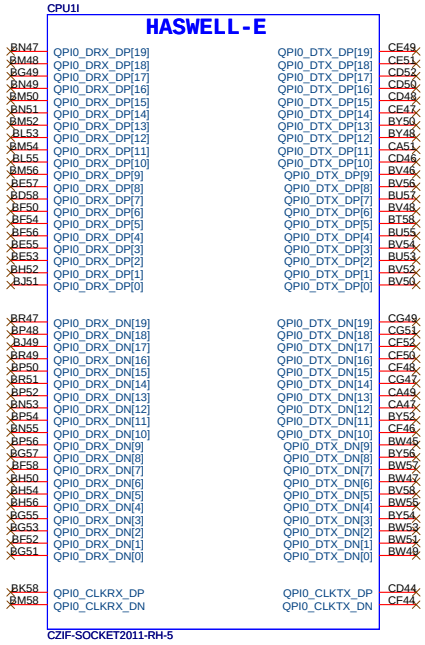
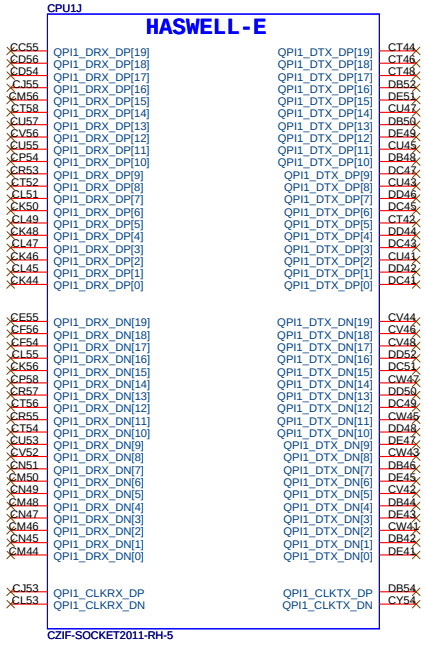
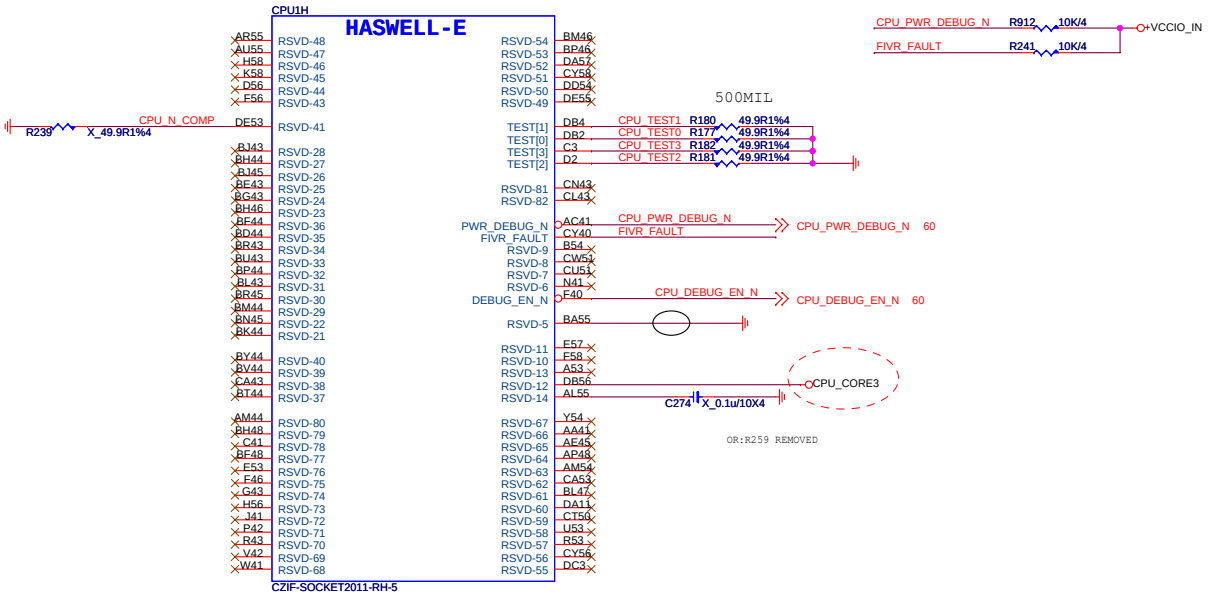
CPU-QPI/RESERVE







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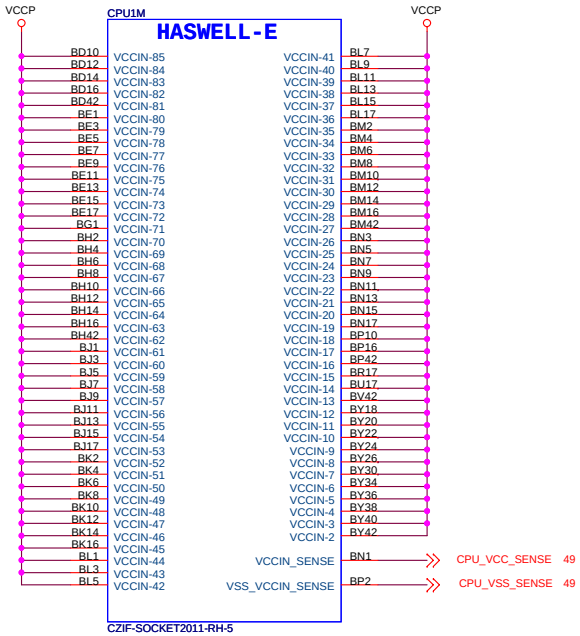
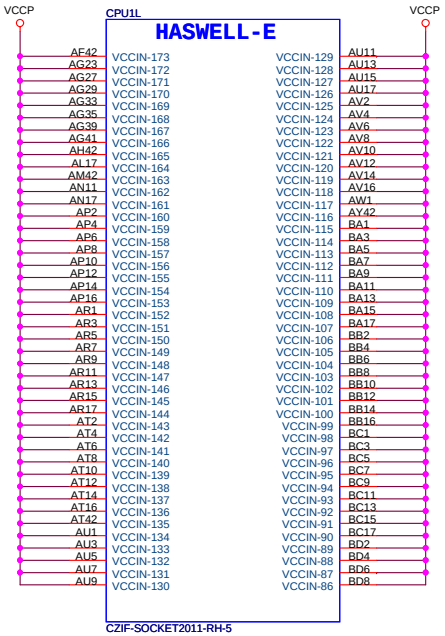
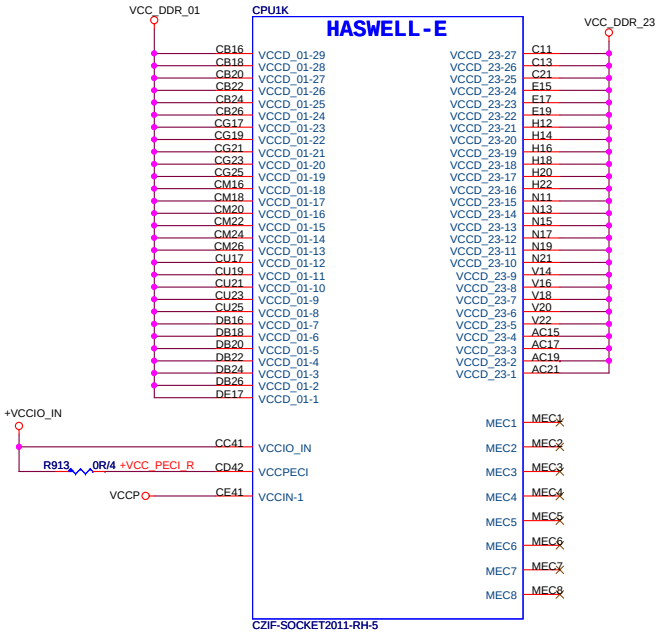
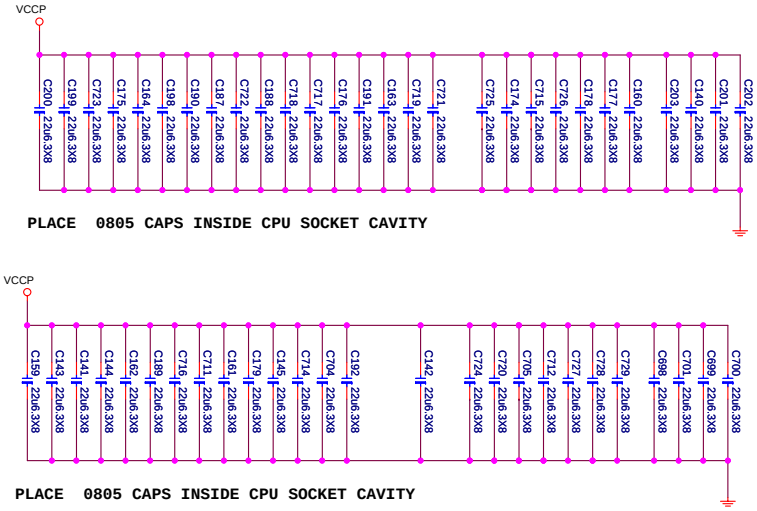
CPU-Power







+CPU_VCCP-Decoupling

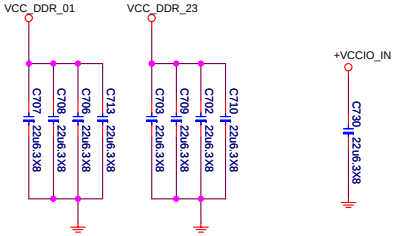


PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

Skt cavity caps, place: 28 on top side & 26 on back side.

+CPU_DDR-Decoupling



PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

MICRO-STAR INT'L CO.,LTD

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CPU-GND

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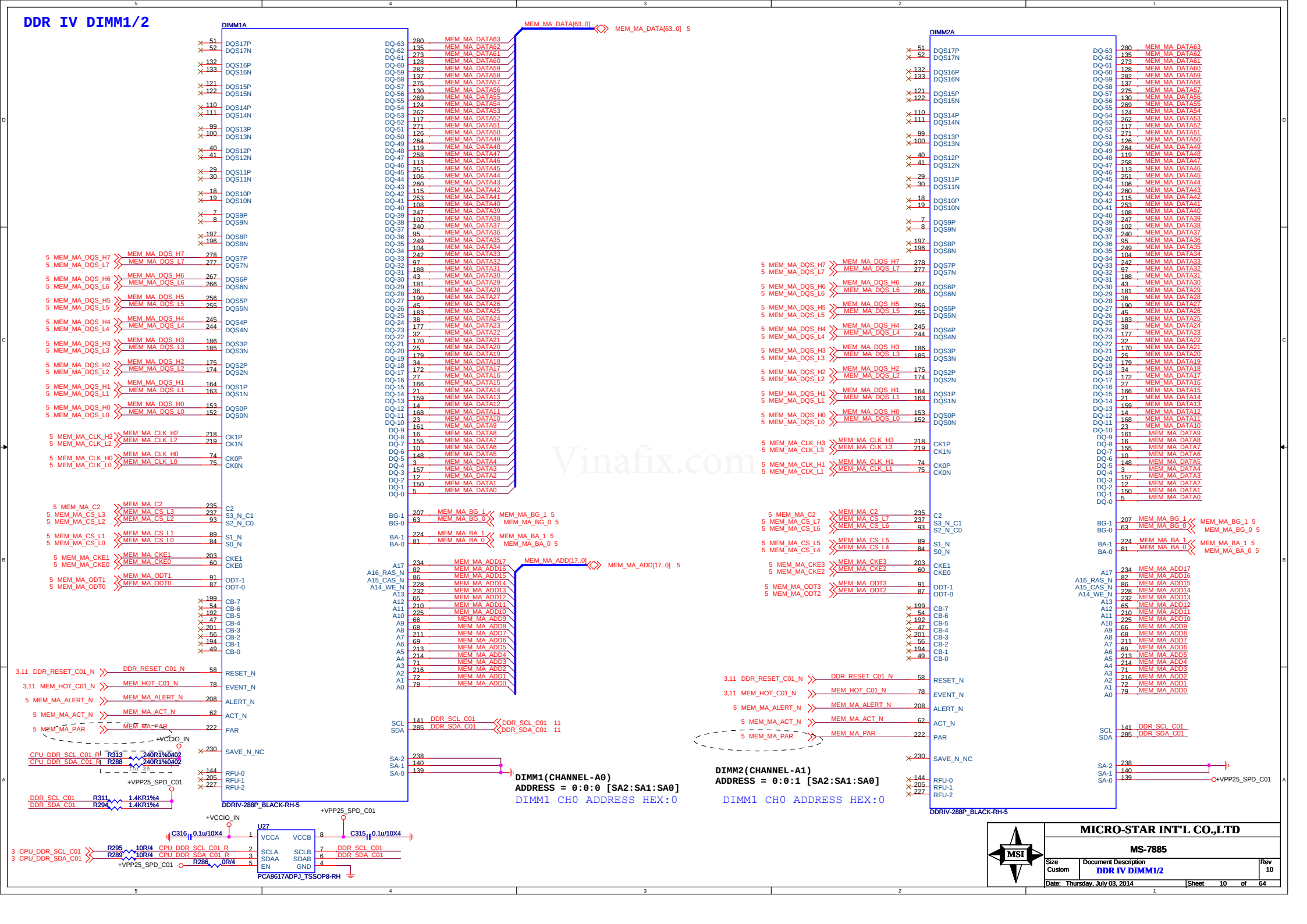
DDR IV DIMM1/2



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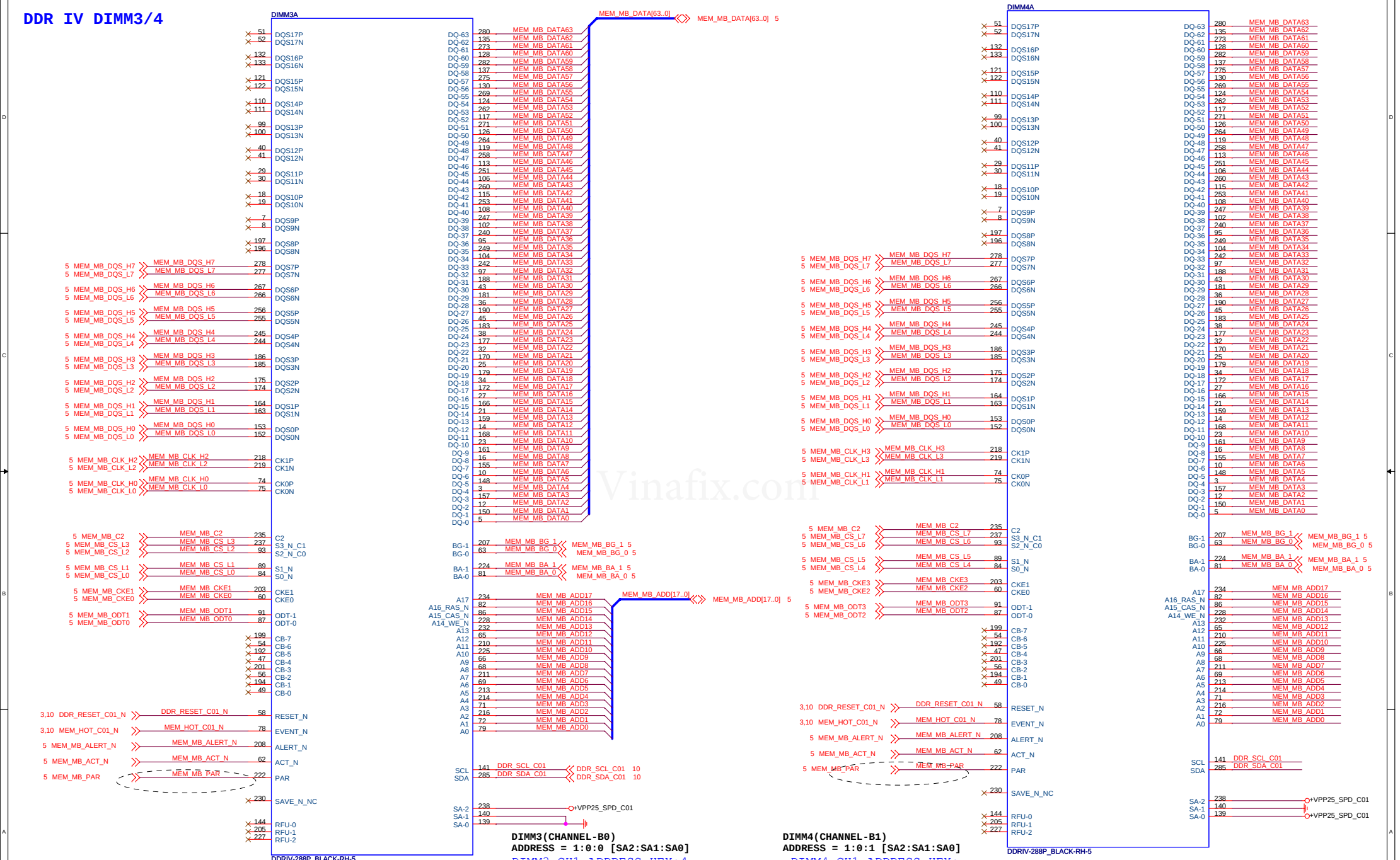
DDR IV DIMM3/4



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Size: Custom	Document Description: DDR IV DIMM3/4
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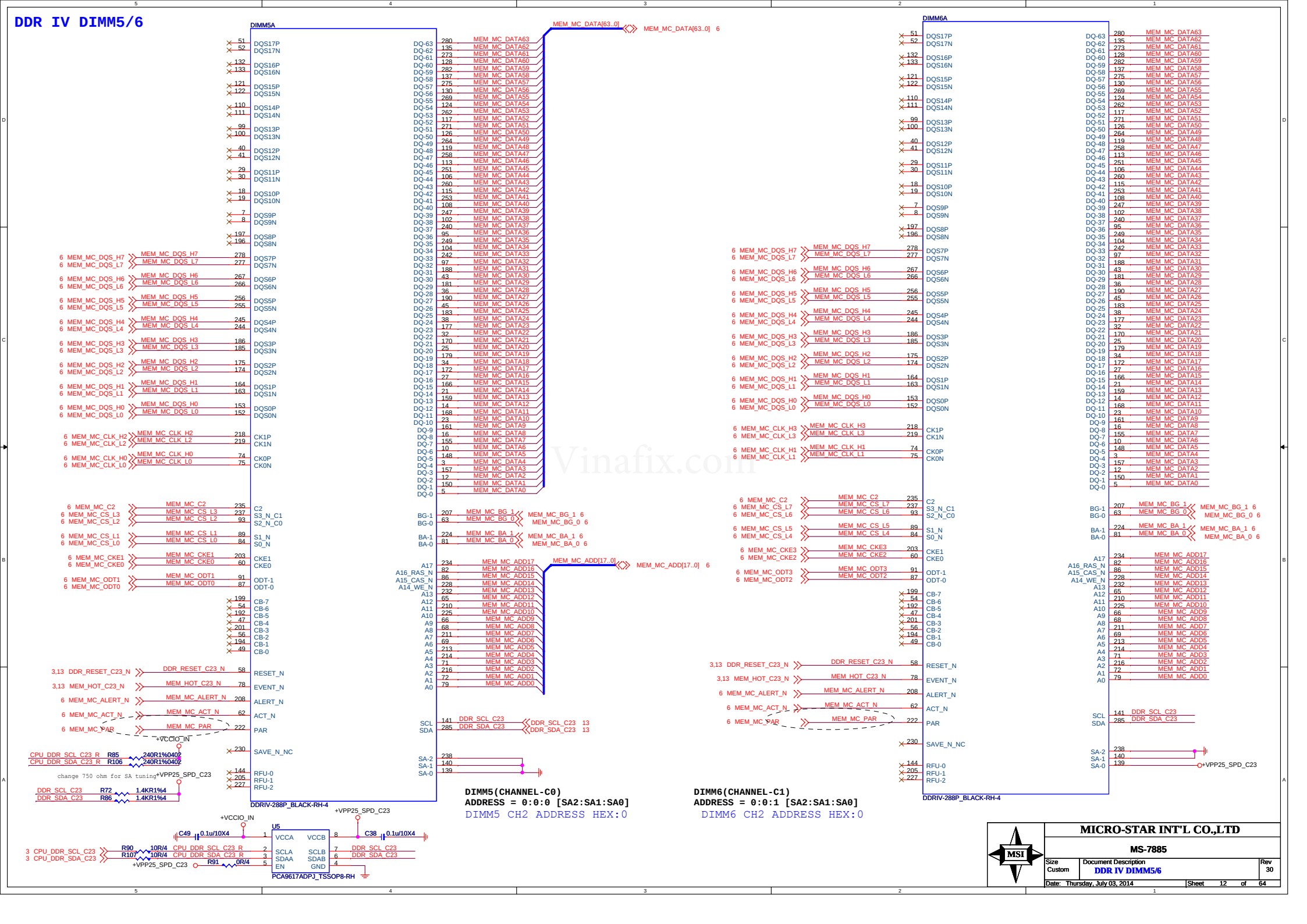
DDR IV DIMM5/6



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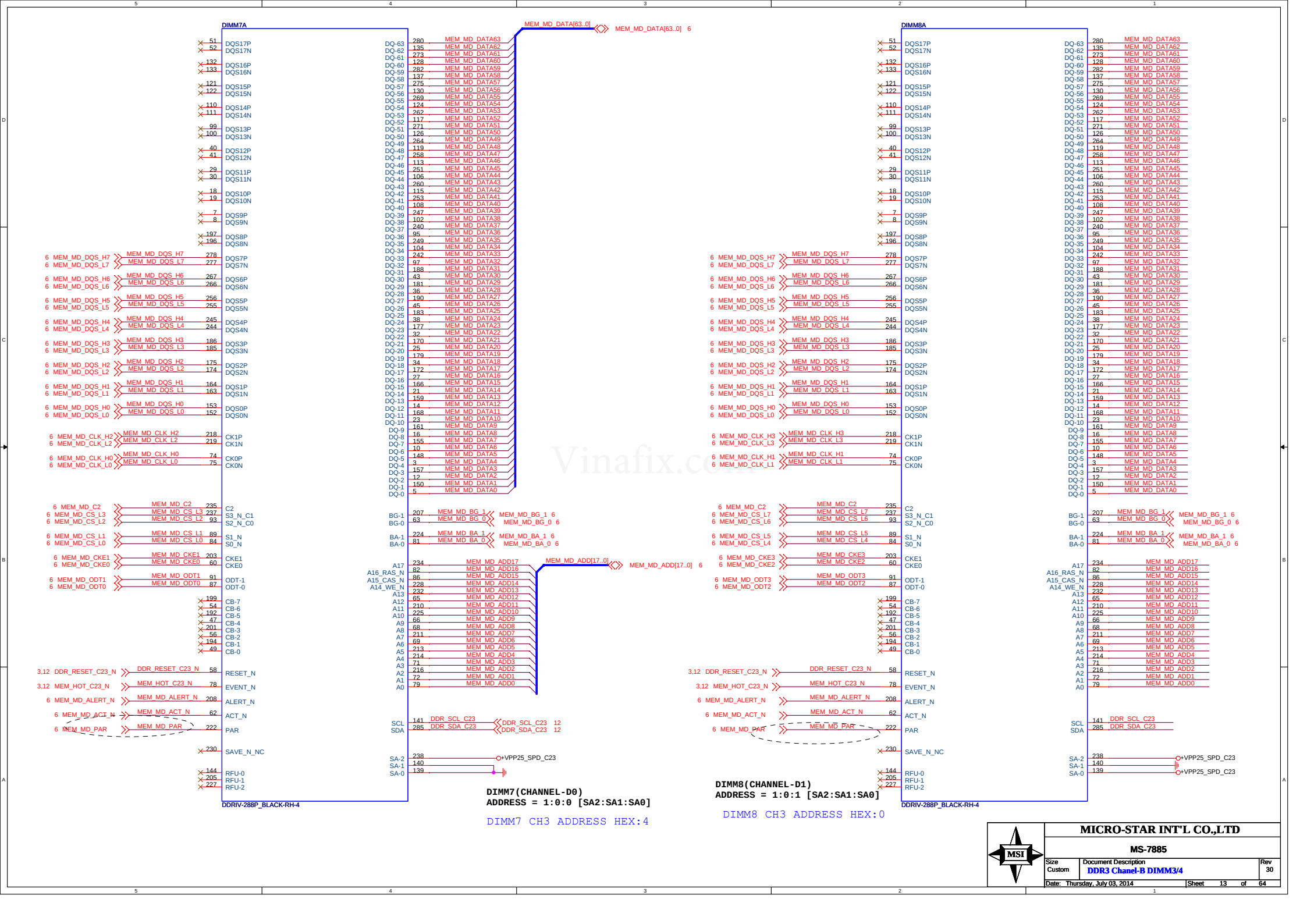

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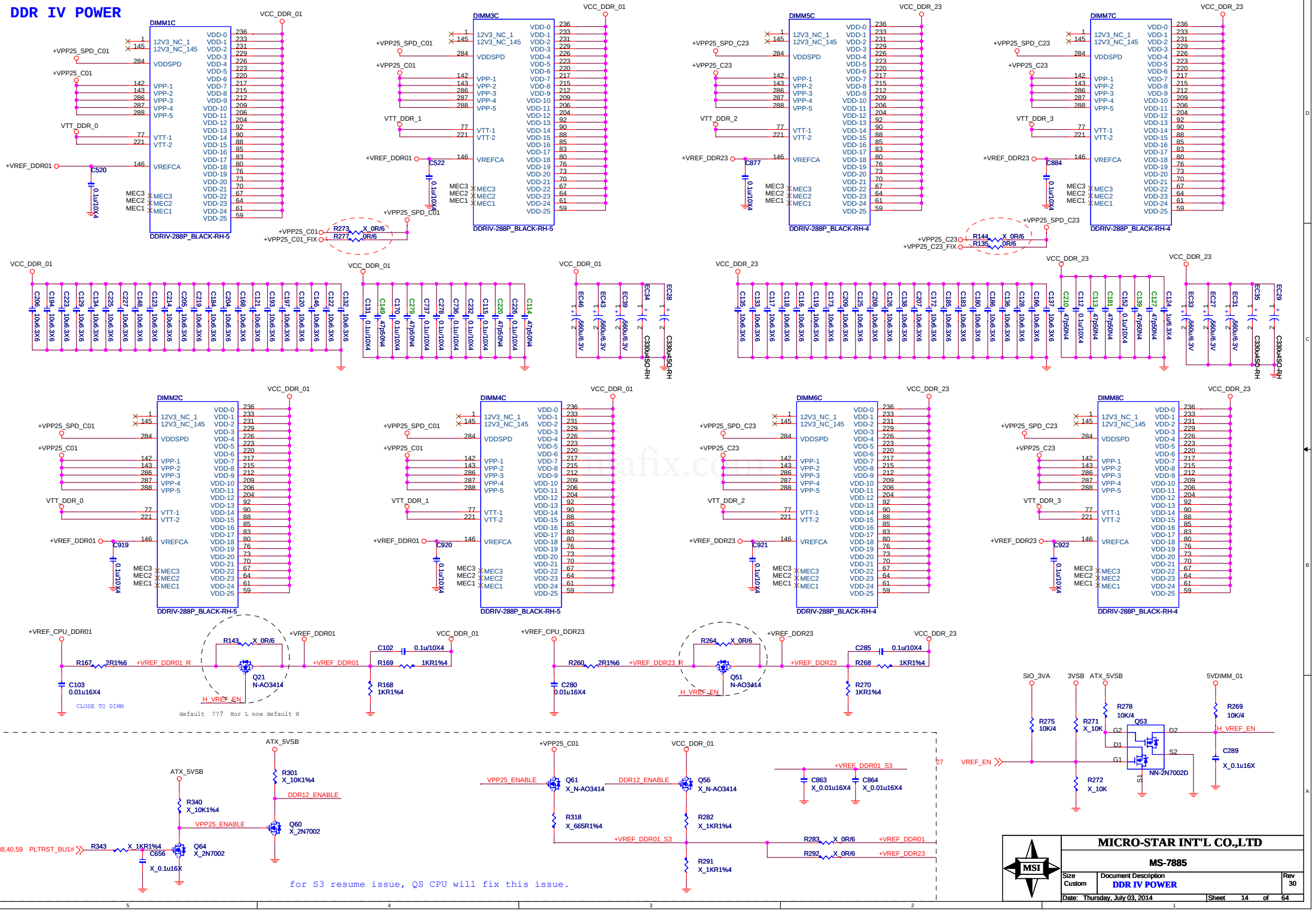
DDR IV POWER



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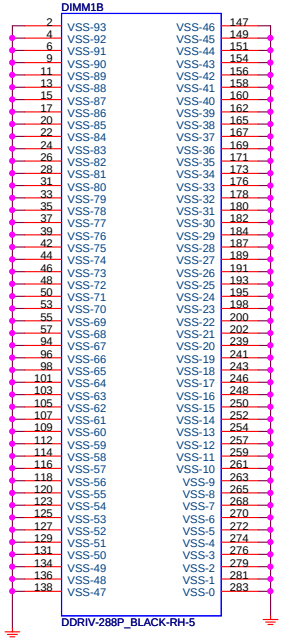
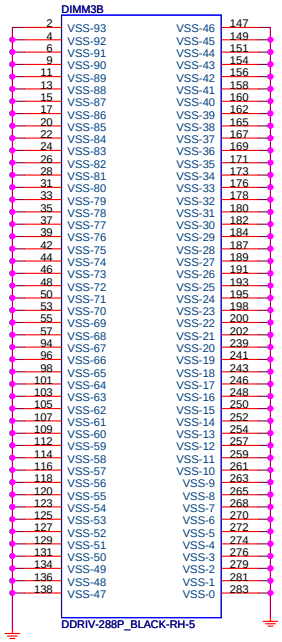
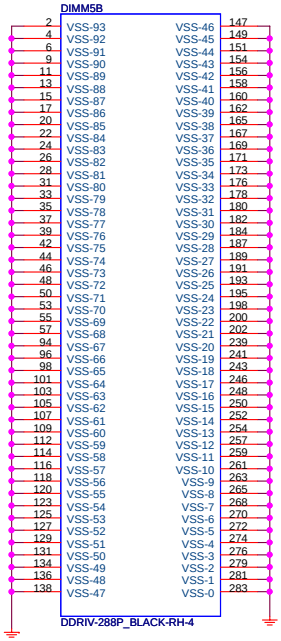
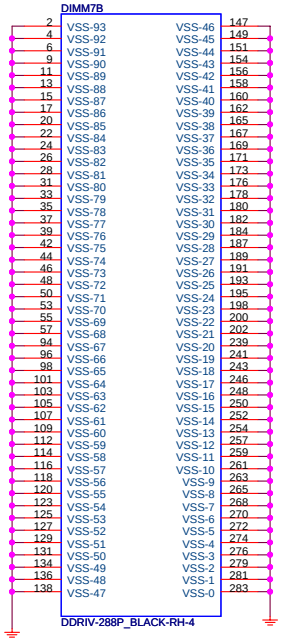
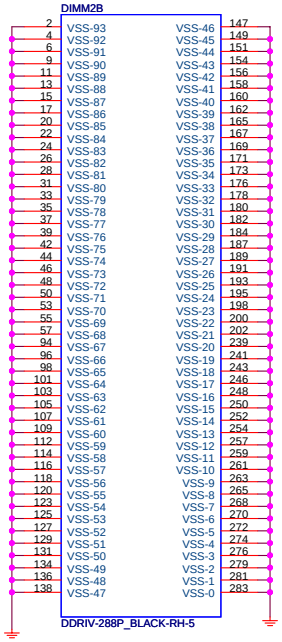
DDR IV GND

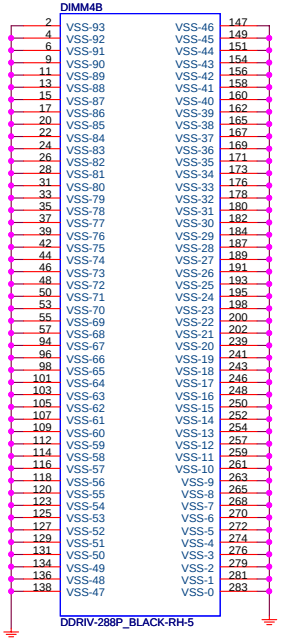


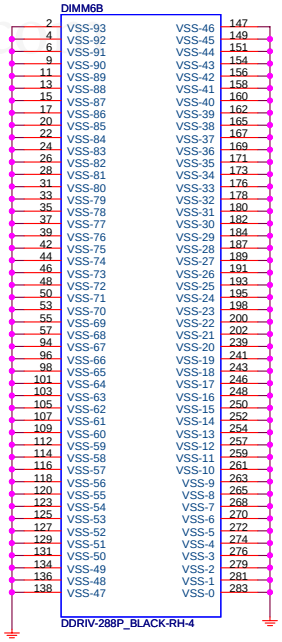


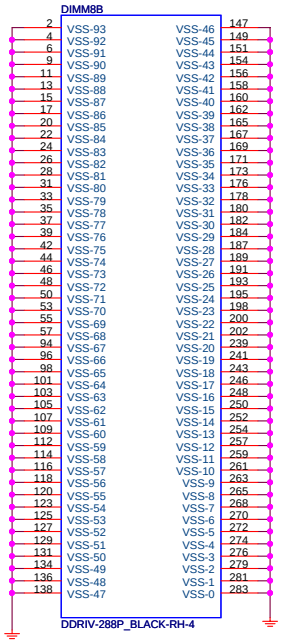












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PCH-LPC/HDA/RTC/MISC/SPI

PCH1D

LPC
HDA
RTC
SPI
power management

Chassis Intrusion

RTC Block

Close to PCH

note CRB 18pf ,need confirm SA result

Trace length of APWROK must be less than PCH_PWROK

The negative min timing implies that DRAMPWROK must either fall before SLP_S4# or within 100 ns after it.

CHECK LIST

CHECK LIST

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PCH-DMI/PCIE/USB/SATA

Vinafix

PCH1B

DMI

DMI_RXP3 DMI_RXN3 DMI_RXP2 DMI_RXN2 DMI_RXP1 DMI_RXN1 DMI_RXP0 DMI_RXN0 DMI_RCOMP DMI_IREF

DMI_TXP3 DMI_TXN3 DMI_TXP2 DMI_TXN2 DMI_TXP1 DMI_TXN1 DMI_TXP0 DMI_TXN0

DMI_TX3 DMI_TX3# DMI_TX2 DMI_TX2# DMI_TX1 DMI_TX1# DMI_TX0 DMI_TX0#

DMI_RX3 DMI_RX3# DMI_RX2 DMI_RX2# DMI_RX1 DMI_RX1# DMI_RX0 DMI_RX0#

PCH_RCOMP_VCC — R367 7.5K1%4 — DMI_RCOMP — DMI_IREF1P5 — R366 0R/4

PCIE

PERP_8 PERN_8 PERP_7 PERN_7 PERP_6 PERN_6 PERP_5 PERN_5 PERP_4 PERN_4 PERP_3 PERN_3 PERP_2/USB3RP_4 PERN_2/USB3RN_4 PERP_1/USB3RP_3 PERN_1/USB3RN_3

PETP_8 PETN_8 PETP_7 PETN_7 PETP_6 PETN_6 PETP_5 PETN_5 PETP_4 PETN_4 PETP_3 PETN_3 PETP_2/USB3TP_4 PETN_2/USB3TN_4 PETP_1/USB3TP_3 PETN_1/USB3TN_3

PE_SLOT5_RX PE_SLOT5_RX# PE_SLOT3_RX PE_SLOT3_RX# PE6_USB31_RX PE6_USB31_RX# PE5_USB31_RX PE5_USB31_RX# PE_NEC_USB_RX PE_NEC_USB_RX# PE_LAN_RX PE_LAN_RX# MB_USB30_RX5+ MB_USB30_RX5- MB_USB30_RX4+ MB_USB30_RX4-

PE_SLOT5_TX PE_SLOT5_TX# PE_SLOT3_TX PE_SLOT3_TX# PE6_USB31_TX PE6_USB31_TX# PE5_USB31_TX PE5_USB31_TX# PE_NEC_USB_TX PE_NEC_USB_TX# PE_LAN_TX PE_LAN_TX# MB_USB30_TX5+ MB_USB30_TX5- MB_USB30_TX4+ MB_USB30_TX4-

PCH_RCOMP_VCC — R978 7.5K1%4 — PCIE_RCOMP — R979 0R/4 — PCIE_IREF1P5

PCIE_RCOMP PCIE_IREF

USB

USB3RP6 USB3RN6 USB3RP5 USB3RN5 USB3RP2 USB3RN2 USB3RP1 USB3RN1

USB3TP6 USB3TN6 USB3TP5 USB3TN5 USB3TP2 USB3TN2 USB3TP1 USB3TN1

MB_USB30_RX3+ MB_USB30_RX3- MB_USB30_RX2+ MB_USB30_RX2- MB_USB30_RX1+ MB_USB30_RX1- MB_USB30_RX0+ MB_USB30_RX0-

MB_USB30_TX3+ MB_USB30_TX3- MB_USB30_TX2+ MB_USB30_TX2- MB_USB30_TX1+ MB_USB30_TX1- MB_USB30_TX0+ MB_USB30_TX0-

USB2P13 USB2N13 USB2P12 USB2N12 USB2P11 USB2N11 USB2P10 USB2N10 USB2P9 USB2N9 USB2P8 USB2N8 USB2P7 USB2N7 USB2P6 USB2N6 USB2P5 USB2N5 USB2P4 USB2N4 USB2P3 USB2N3 USB2P2 USB2N2 USB2P1 USB2N1 USB2P0 USB2N0

MB_USB_13D+ MB_USB_13D- MB_USB_12D+ MB_USB_12D- MB_USB_11D+ MB_USB_11D- MB_USB_10D+ MB_USB_10D- MB_USB_9D+ MB_USB_9D- MB_USB_8D+ MB_USB_8D- MB_USB_5D+ MB_USB_5D- MB_USB_4D+ MB_USB_4D- MB_USB_3D+ MB_USB_3D- MB_USB_2D+ MB_USB_2D- MB_USB_1D+ MB_USB_1D- MB_USB_0D+ MB_USB_0D-

SIO_PME_N — OC#6 OC#5 USB3_SMI1 OC#4 OC#3 OC#2 OC#1 OC#0

OC7_N/GPIO14 OC6_N/GPIO10 OC5_N/GPIO9 OC4_N/GPIO43 OC3_N/GPIO42 OC2_N/GPIO41 OC1_N/GPIO40 OC0_N/GPIO59

USB_COMP — R529 22.6R1%4 — USBRBIAS — USBRBIAS_N

3VSB

R515 10K/4 SIO_PME_N
R524 X_10K/4 OC#6
R532 10K/4 USB3_SMI1
R514 X_10K/4 OC#4
R551 10K/4 OC#3
R481 10K/4 OC#2
R482 X_10K/4 OC#1
R508 10K/4 OC#0

PCH_1P5 — R376 0R/8
PCH_1P05 — R368 X_0R/8
PCH_RCOMP_VCC

USB0,1	USB2,3	USB4,5	no using	usb8,9 VIA USB controller	USB3_SMI1	usb10,11 usb12,13
OC0# supper charge	OC1# FUSB_VCC2	OC2# AMP_PWR	OC3#	OC4# 5V_RUSB1 5V_RUSB5 5V_RUSB6	OC5#	OC6# FUSB_VCC1

PCH_RCOMP_VCC — C841 0.1u/10X4 — C842 0.1u/10X4 — C843 0.1u/10X4 — C844 0.1u/10X4

option bom

VCC3
PCH_GP69 R603 10K/4
PCH_GP70 R573 10K/4
PCH_GP71 R572 10K/4

PCH_GP69 R604 X_10K/4
PCH_GP70 R568 X_10K/4
PCH_GP71 R567 X_10K/4

PCH1C

SATA

SATA_RXP_3 SATA_RXN_3 SATA_RXP_2 SATA_RXN_2 SATA_RXP_1 SATA_RXN_1 SATA_RXP_0 SATA_RXN_0

SATA_TXP_3 SATA_TXN_3 SATA_TXP_2 SATA_TXN_2 SATA_TXP_1 SATA_TXN_1 SATA_TXP_0 SATA_TXN_0

SATA_RXP_5/PERP_2 SATA_RXN_5/PERN_2 SATA_RXP_4/PERP_1 SATA_RXN_4/PERN_1

SATA_TXP_5/PETP_2 SATA_TXN_5/PETN_2 SATA_TXP_4/PETP_1 SATA_TXN_4/PETN_1

SATA_RCOMP SATA_IREF

SATA0GP SATA1GP SATA2GP SATA3GP

PWM3 PWM2 PWM1 PWM0

SATA0GP/GPIO21 SATA1GP/GPIO19 SATA2GP/GPIO36 SATA3GP/GPIO37

TACH7/GPIO71 TACH6/GPIO70 TACH5/GPIO69 TACH4/GPIO68 TACH3/GPIO7 TACH2/GPIO6 TACH1/GPIO1 TACH0/GPIO17

SATA4GP/GPIO16/MGPIO9 SATA5GP/GPIO49/MGPIO10 SDATAOUT0/GPIO39 SDATAOUT1/GPIO48 sSDATAOUT0 sSDATAOUT1

SCLOCK/GPIO22 SLOAD/GPIO38

sSLOAD sSCLOCK

SATA_RX9 SATA_RX#9 SATA_RX8 SATA_RX#8 SATA_RX7 SATA_RX#7 SATA_RX6 SATA_RX#6 SATA_RX5 SATA_RX#5 SATA_RX4 SATA_RX#4 SATA_RX3 SATA_RX#3 SATA_RX2 SATA_RX#2 SATA_RX1 SATA_RX#1 SATA_RX0 SATA_RX#0

SATA_TX9 SATA_TX#9 SATA_TX8 SATA_TX#8 SATA_TX7 SATA_TX#7 SATA_TX6 SATA_TX#6 SATA_TX5 SATA_TX#5 SATA_TX4 SATA_TX#4 SATA_TX3 SATA_TX#3 SATA_TX2 SATA_TX#2 SATA_TX1 SATA_TX#1 SATA_TX0 SATA_TX#0

SATA_LED_N — SATAS_LED_N_R

PCH_SATAS0_GP PCH_SATAS1_GP PCH_SATAS2_GP PCH_SATAS3_GP

PCH_GP21 PCH_GP19 PCH_GP36 PCH_GP37

PCH_GP16 PCH_GP49 PCH_GP39 PCH_GP48 SSDATAOUT0 SSDATAOUT1

chipset internal 20 K pull up

PCH_RCOMP_VCC — R479 7.5K1%4 — SATAS_RCOMP — R478 0R/4 — SATAS_IREF1P5

PCH_RCOMP_VCC — R380 7.5K1%4 — SATA_RCOMP — R379 0R/4 — SATA_IREF1P5

PCH_GP71 PCH_GP70 PCH_GP69 PCH_GP68 PCH_GP7 PCH_GP6 PCH_GP1 PCH_GP17

PCH_GP22 PCH_GP38

PCH_GP1 — 27,59 GEAR1# — Q76 2N7002

VCC3
PCH_GP39 R1011 2K/4
PCH_GP48 R418 2K/4
SSDATAOUT0 R487 2K/4
SSDATAOUT1 R467 2K/4
SSLOAD R459 10K/4
SSCLOCK R462 10K/4

VCC3
PCH_GP1 R571 10K/4
PCH_GP7 R585 10K/4

RN3
PCH_GP38 PCH_GP21 PCH_GP22 — 8P4R-10KR0402

RN9
PCH_GP17 PCH_GP68 PCH_GP6 — 8P4R-10KR0402

VCC3 — RN12
PCH_SATAS0_GP PCH_SATAS1_GP PCH_SATAS2_GP PCH_SATAS3_GP — 8P4R-10KR0402

VCC3 — R703 X_10K/4 — 42,45 PCH_M.2_DET — PU on M.2 side
R421 0R/4 PCH_GP16
R423 0R/4 PCH_GP49

	GPIO16	GPIO49
0	PCIE	PCIE
1	SATA (Default)	SATA

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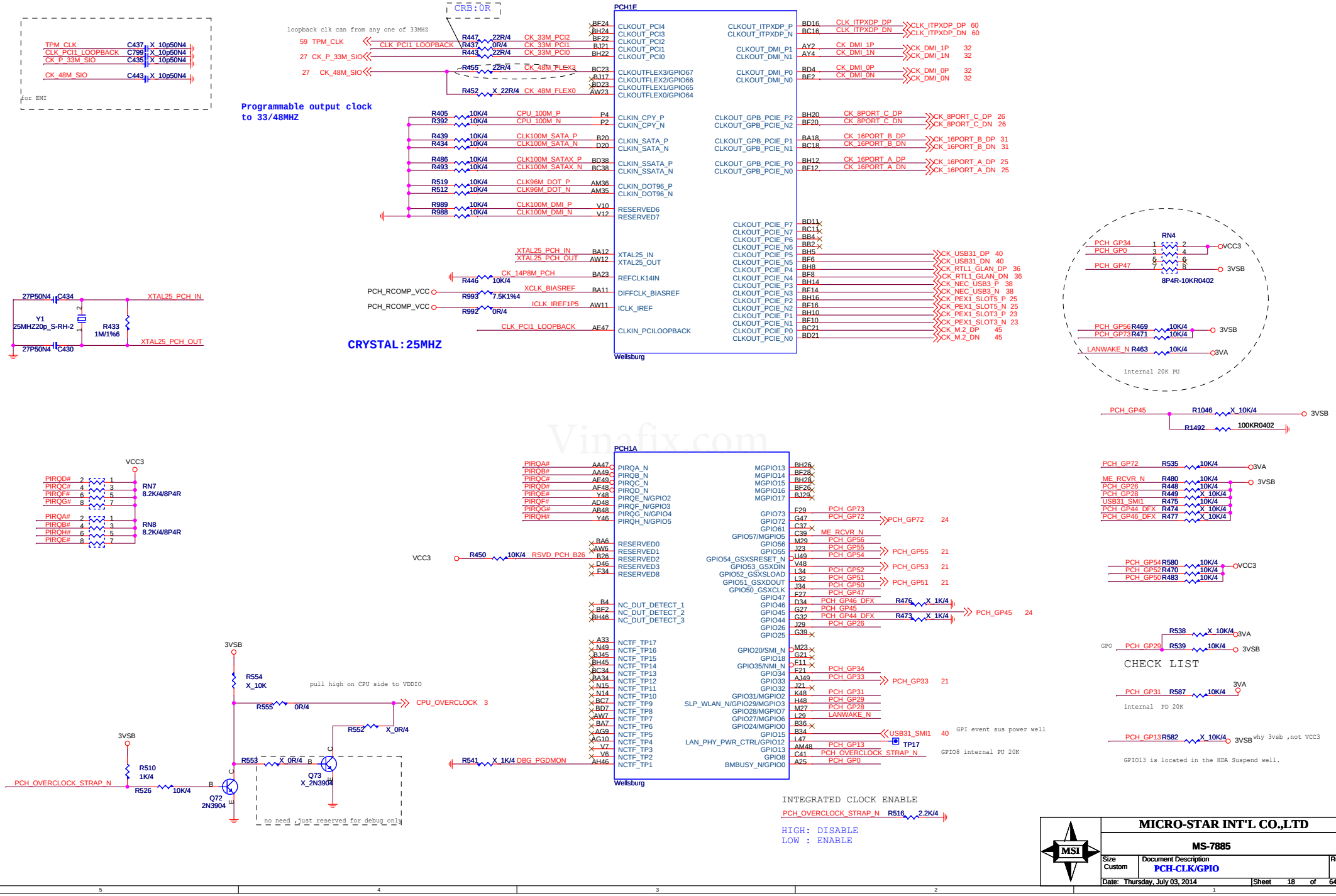
PCH-CLK/GPIO



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Size: Custom	Document Description: PCH-CLK/GPIO	Rev: 30
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PCH-POWER

PCH_1P05:5.83A

+1P05V_ME:0.67A

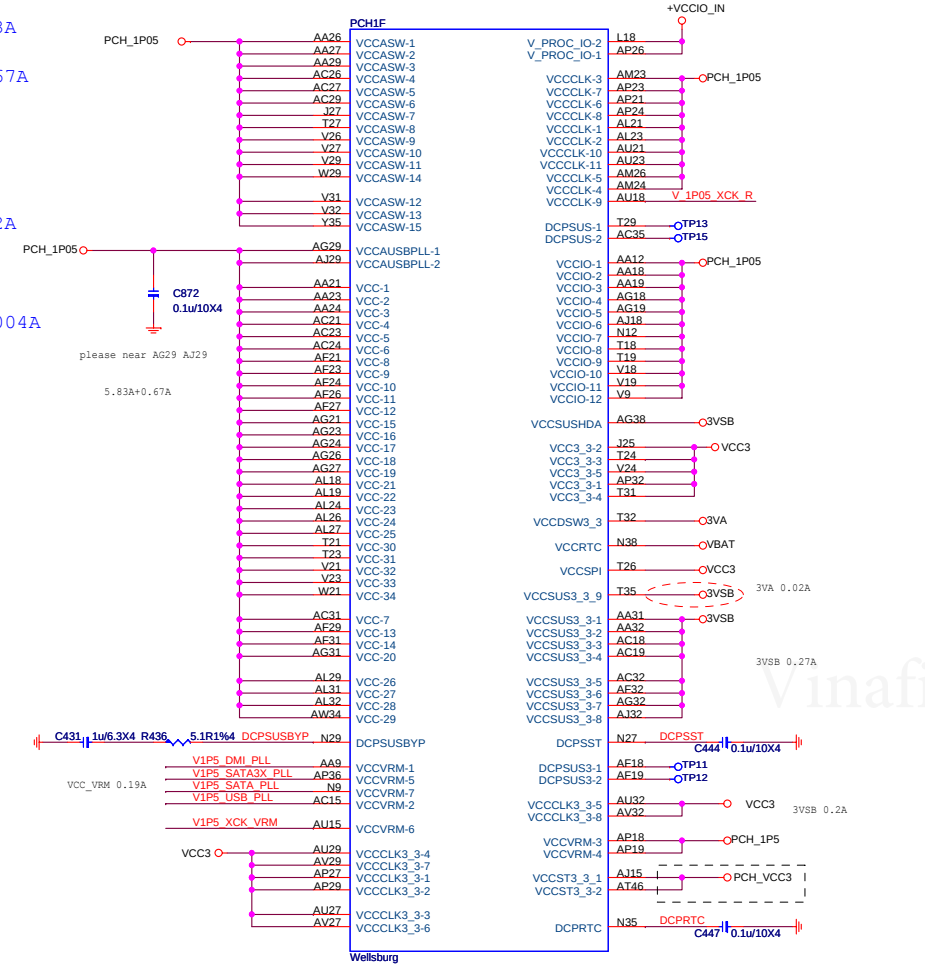
VCC3:0.2A

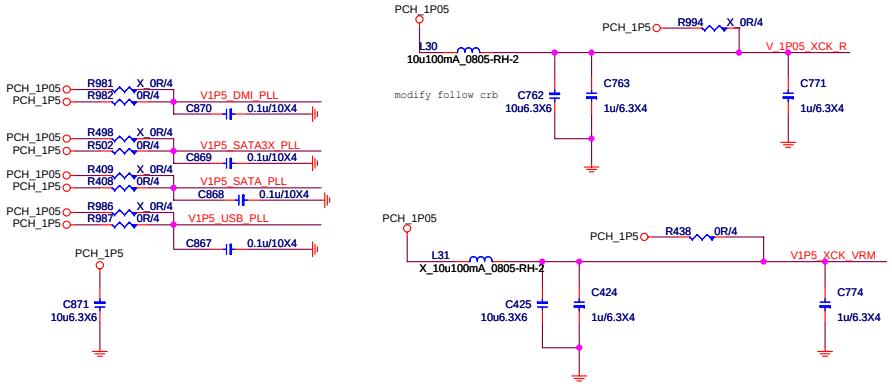
3VSB:0.27A

SPI_VCC3:0.02A

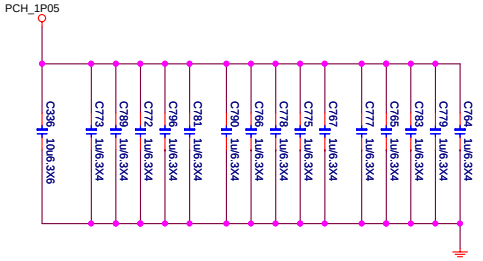
3VA:0.02A

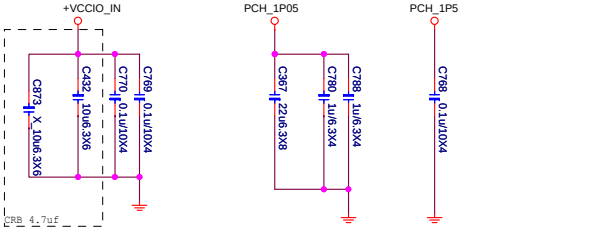
+VCCIO_IN:0.004A

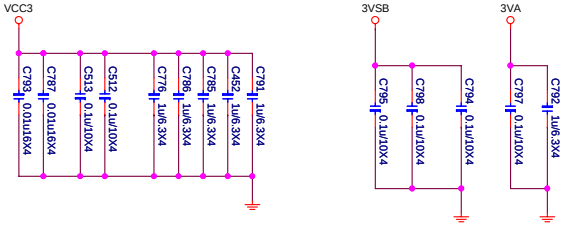


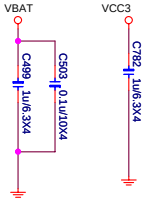


PCH decoupling cap









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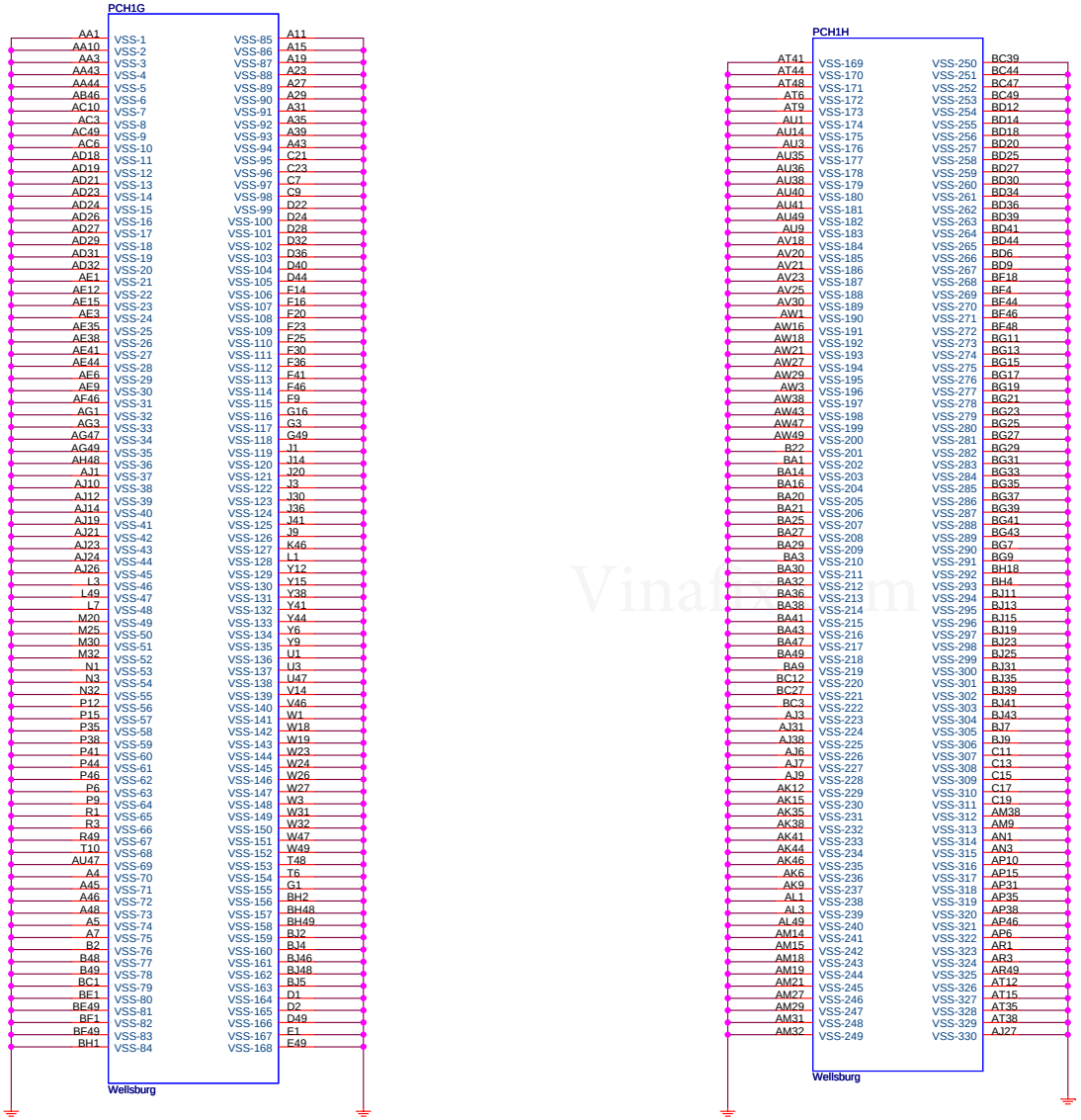
PCH-GND



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MS-7885		
Size: Custom	Document Description: PCH-GND	Rev: 30
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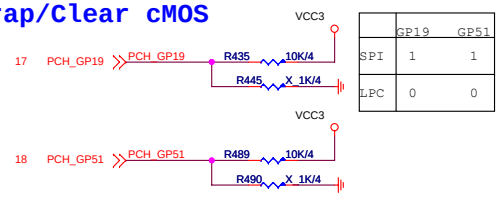
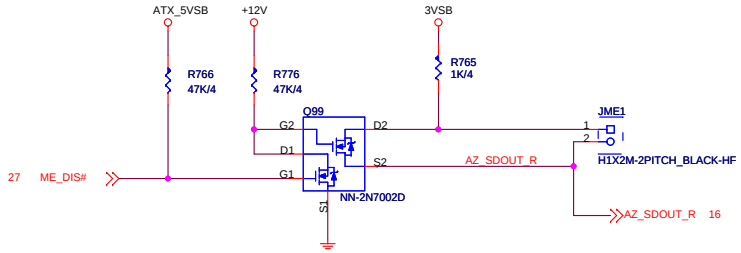
PCH Strap/Clear cMOS



	GP19	GP51
SPI	1	1
LPC	0	0



HIGH (1-2):SECURITY MEASURES OVERRIDEN
LOW (0-1) : SECURITY PER FLASH DESCRIPTOR (DEFAULT)

INTEGRATED SUS 1.05V VRM ENABLE

HIGH: ENABLE (INTERNAL SUPPLY) (DEFAULT)
LOW: DISABLE (EXTERNAL SUPPLY)

DMI RX Termination

This signal has a weak internal pull-down.
This signal only take effect if DMI is configured in AC-coupled mode.
0 = DMI RX is terminated to VSS.
1 = option not supported.

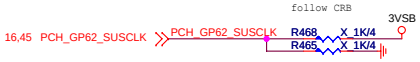
TLS CONFIDENTIALITY ENABLE STRAP

HIGH :TLS CONFIDENTIALITY ENABLE (DEFAULT)
LOW : RING OSCILLATOR BYPASS
LOW :TLS CONFIDENTIALITY DISABLE

DEEP SLEEP WELL ON-DIE VRM ENABLE

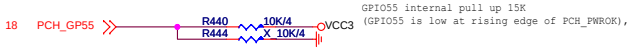
HIGH: ENABLE (INTERNAL SUPPLY) (DEFAULT)
LOW: DISABLE (EXTERNAL SUPPLY)

PLL ON-DIE VR ENABLE



HIGH :PLL ON-DIE VR ENABLE. INT PU. (DEFAULT)
LOW :PLL ON-DIE VR DISABLE

Top-Block Swap Override



DMI TX TERMINATION (DEFENSIVE)

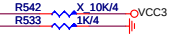
This signal has a weak internal pull-down.
This signal only takes effect if DMI is configured in DC-coupled mode.
0 = DMI TX is terminated to VSS.
1 = DMI TX is terminated to VCC/2.

NO REBOOT OPTION STRAP

LOW : REBOOT
HIGH: NO-REBOOT

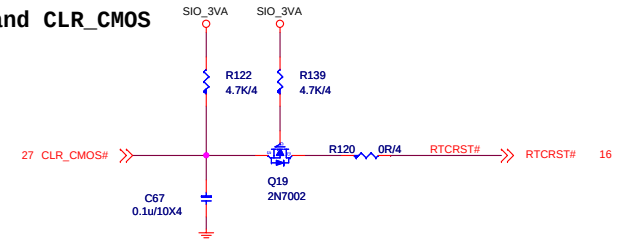
DMI AC Coupling

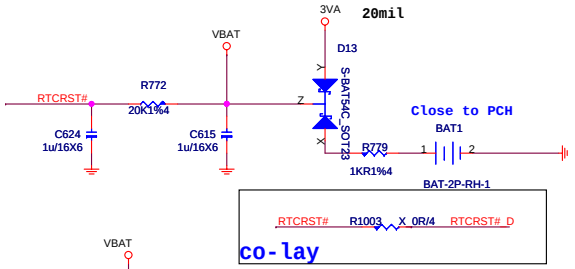
CHECK LIST

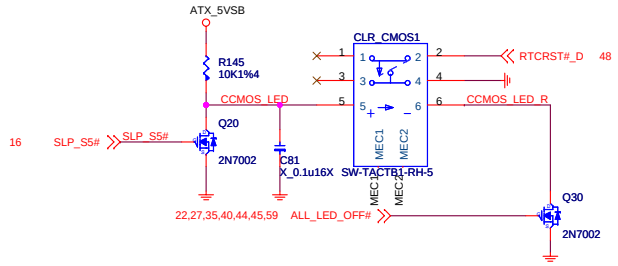


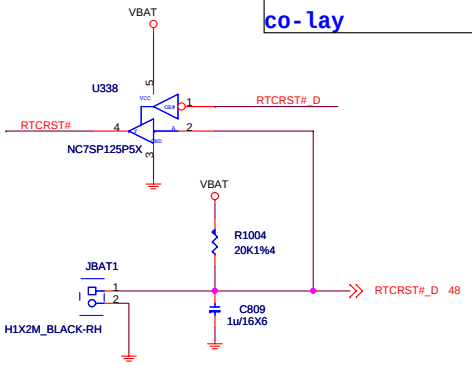
This Signal has a weak internal pull-up.
0= Configures DMI for AC coupling mode.
1 = Configures DMI for DC coupling mode.

RTC and CLR_CMOS









LED LIGHTING RULE
S0/S3/S4 : LED OFF
S5 : LED ON

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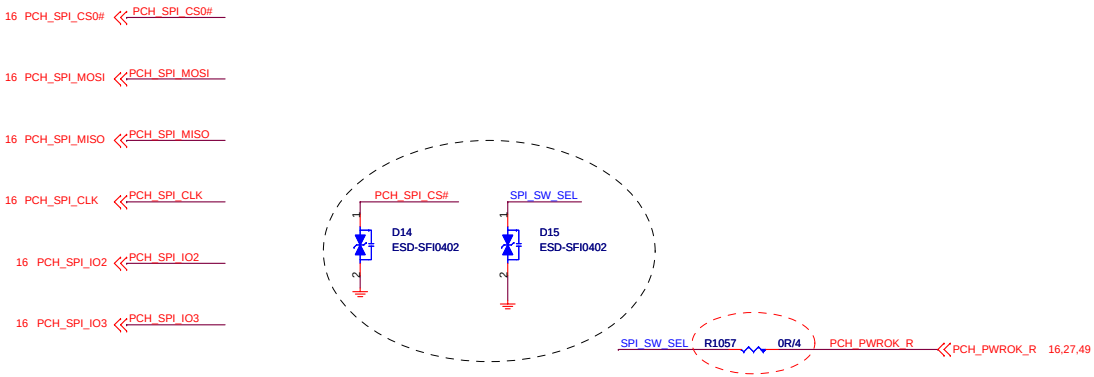
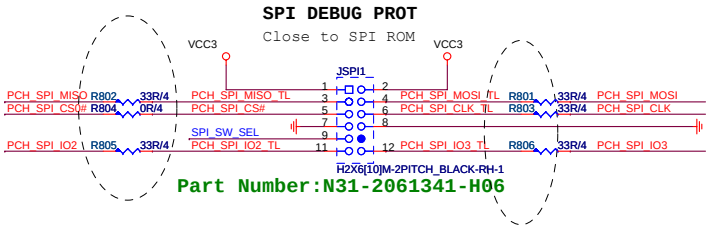
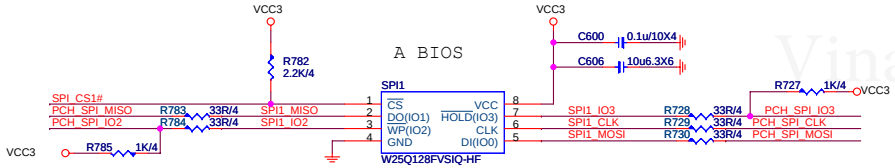
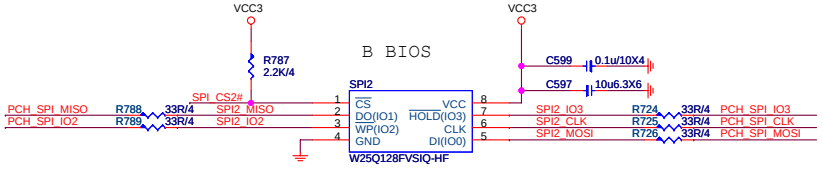








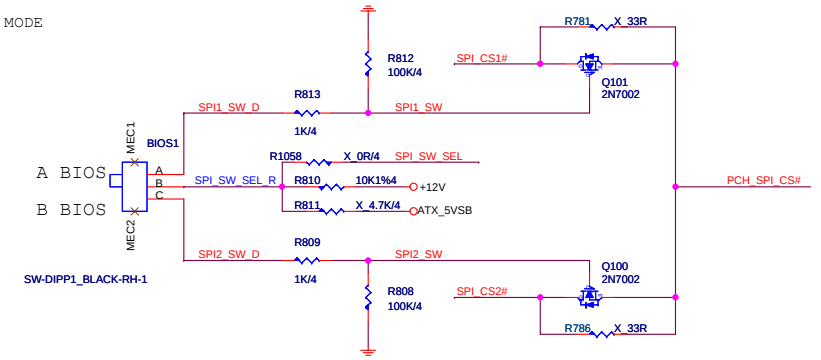
SPI FLASH ROM

Place close to SB.

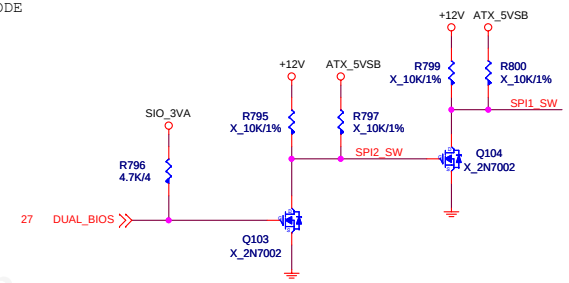
*SPI_CLK & SPI_MOSI must be length matched to within 500mils.
*SPI_CLK & SPI_CS0# must be length matched to within 500mils.

OPTION BIOS

HW MODE



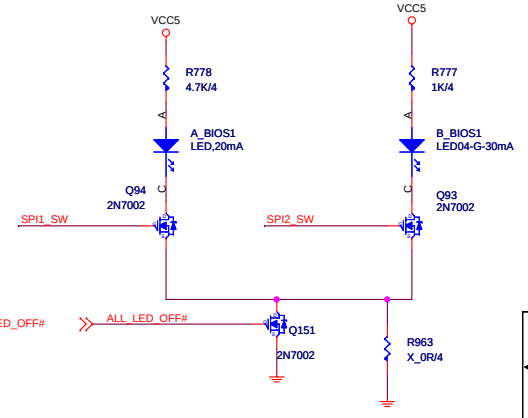
BIOS MODE

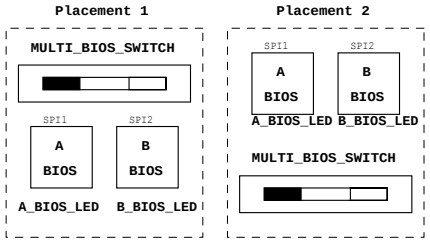


* if you not support Standby power in S5 Status, component "MULTI_BIOS_SWITCH1.B(PIN B) " Pull-high to +12V & Q12/Q13 MOS select 2N7002

* if you support Standby power in S5 Status(Ex; PCH is B75 Chipset) , component "MULTI_BIOS_SWITCH1.B(PIN B)" pull-igh to ATX_5VSB , component Q12/Q13 must select "Vth" under 1V (Component Suggestion as below)

D03-0341409-A68 / D03-0230019-A30





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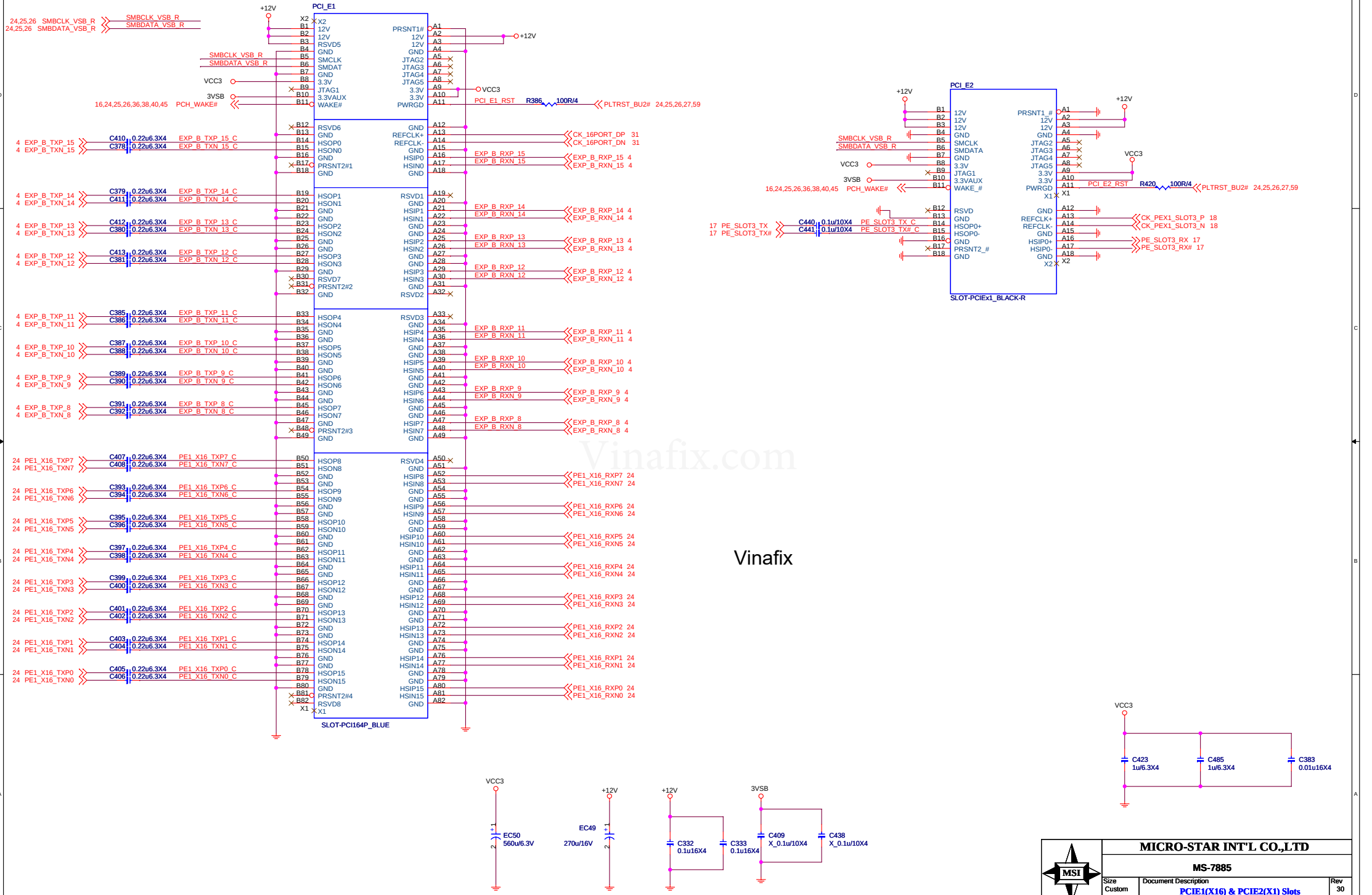
PCIE1(X16) & PCIE2(X1) Slots



Vinafix

Vinafix.com

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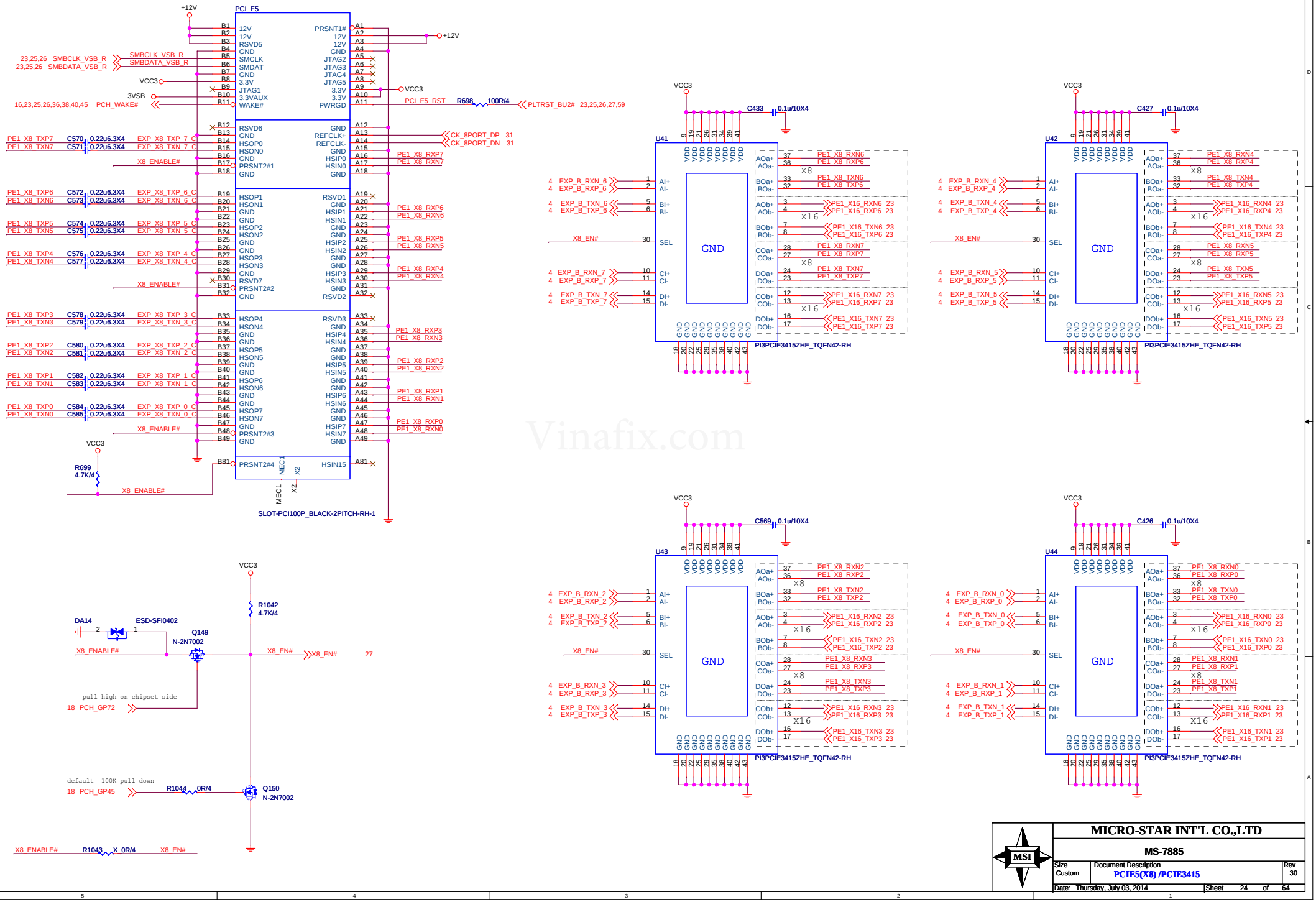
PCIE5(X8) /PCIE3415



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Size: Custom	Document Description: PCIE5(X8) /PCIE3415
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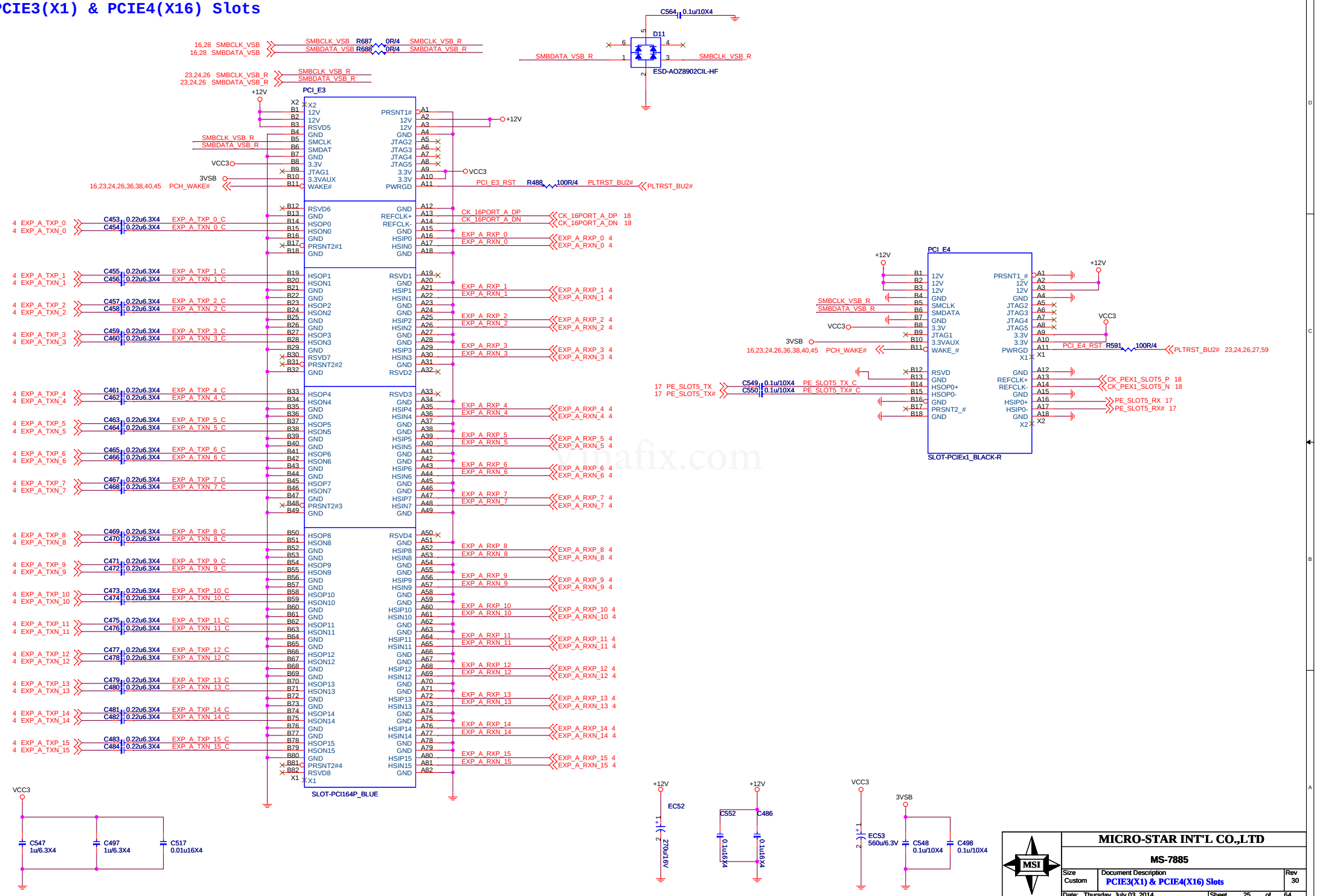
PCIE3(X1) & PCIE4(X16) Slots



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Size: Custom	Document Description: PCIE3(X1) & PCIE4(X16) Slots
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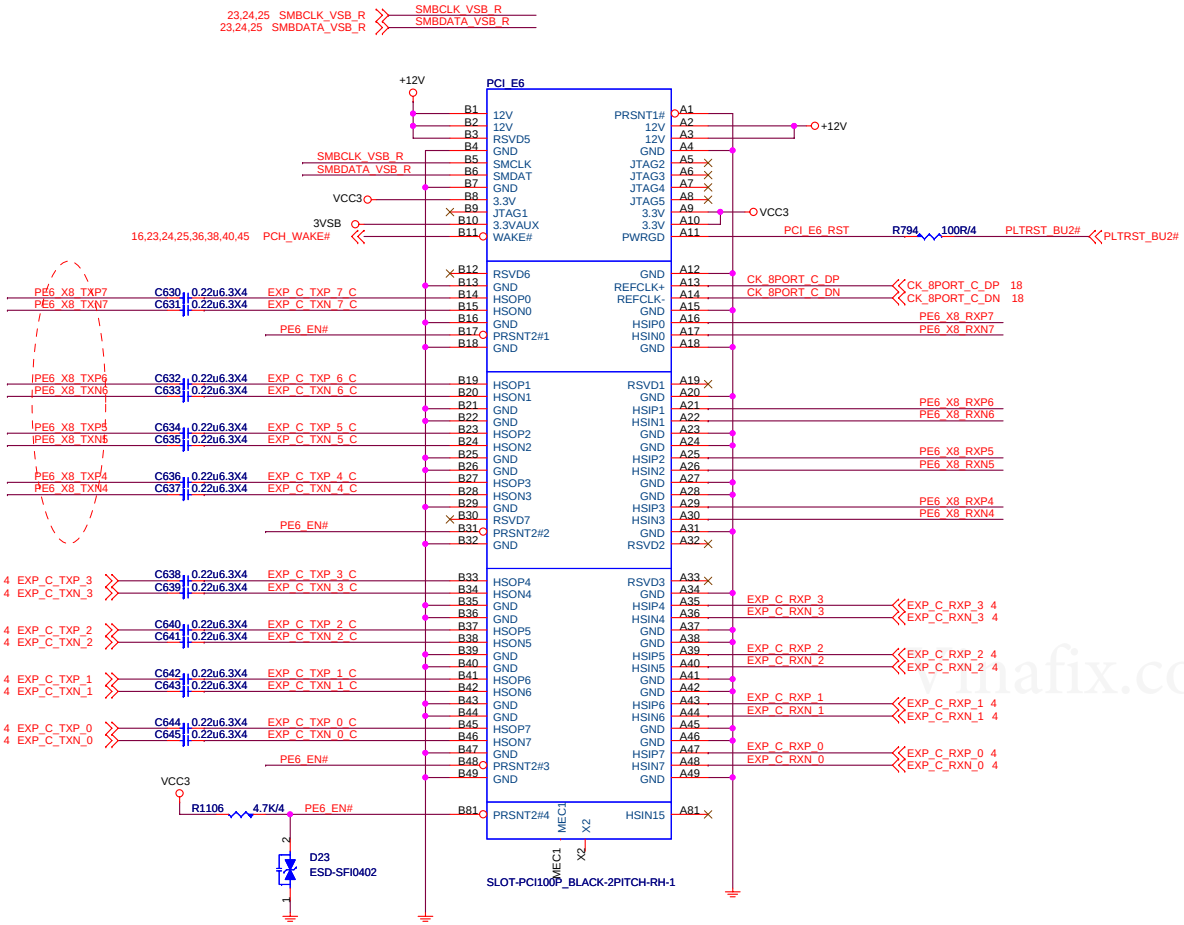
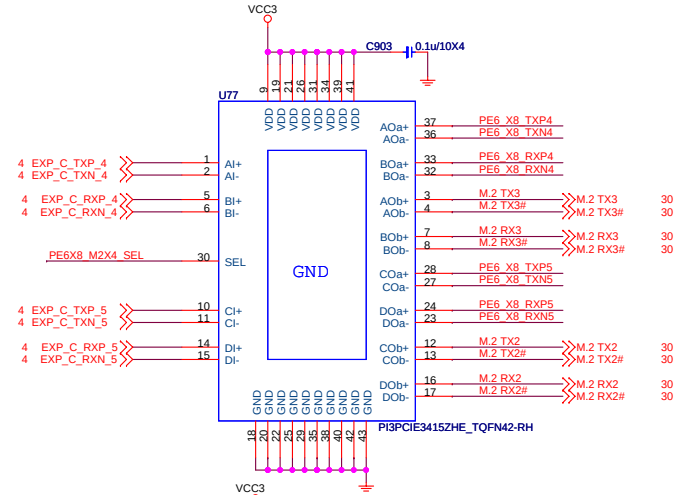
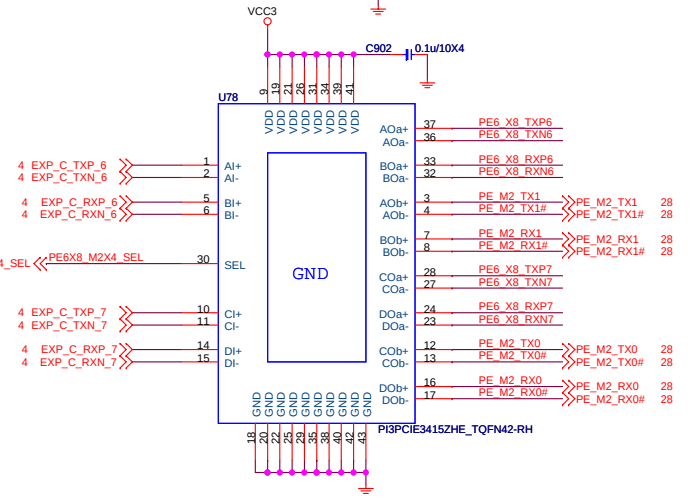
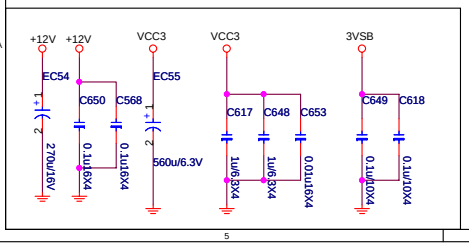
PCIE6(X8) Slots

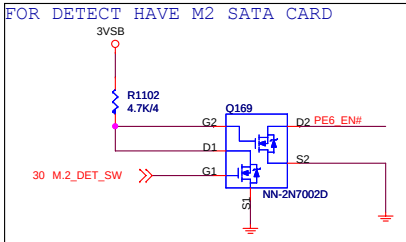




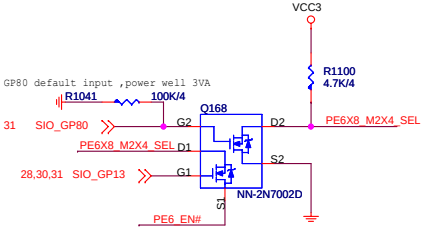




FOR DETECT HAVE M2 SATA CARD



M.2_DET_SW:
0:m2-sata
1:m2-pcie or no m2 device



PE6X8_M2X4_SEL
high:CPU_PCIEto m2
low:CPU_PCIE to PE6

when PE6 and m2_pcie plug on ,but PE6 on first

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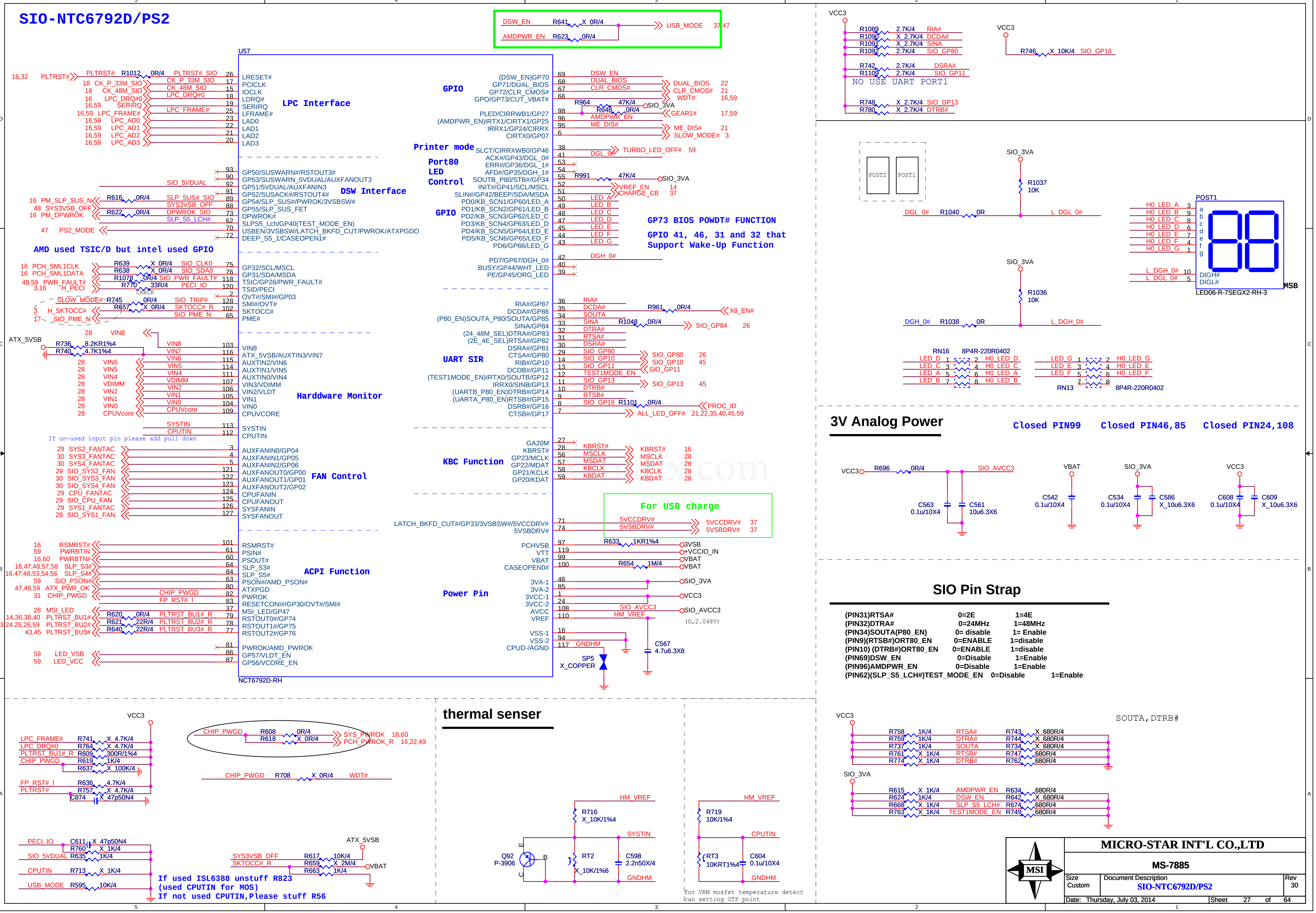

SIO-NTC6792D/PS2
U57
NCT6792D-RH
LPC Interface
GPIO
Printer mode
Port80 LED Control
DSW Interface
AMD used TSIC/D but intel used GPIO
Harddware Monitor
If un-used input pin please add pull down
FAN Control
KBC Function
UART SIR
ACPI Function
Power Pin
For USB charge
NO USE UART PORT1
GP73 BIOS POWDT# FUNCTION
GPIO 41, 46, 31 and 32 that Support Wake-Up Function
POST1
LED06-R-7SEGX2-RH-3
MSB
3V Analog Power
Closed PIN99
Closed PIN46,85
Closed PIN24,108
SIO Pin Strap
(PIN31)RTSA# 0=2E 1=4E
(PIN32)DTRA# 0=24MHz 1=48MHz
(PIN34)SOUTA(P80_EN) 0= disable 1= Enable
(PIN9)(RTSB#)ORT80_EN 0=ENABLE 1=disable
(PIN10) (DTRB#)ORT80_EN 0=ENABLE 1=disable
(PIN69)DSW_EN 0=Disable 1=Enable
(PIN96)AMDPWR_EN 0=Disable 1=Enable
(PIN62)(SLP_S5_LCH#)TEST_MODE_EN 0=Disable 1=Enable
thermal senser
If used ISL6388 unstuff R823
(used CPUTIN for MOS)
If not used CPUTIN,Please stuff R56
for VRM mosfet temperature detect
can setting OTP point
SOUTA,DTRB#
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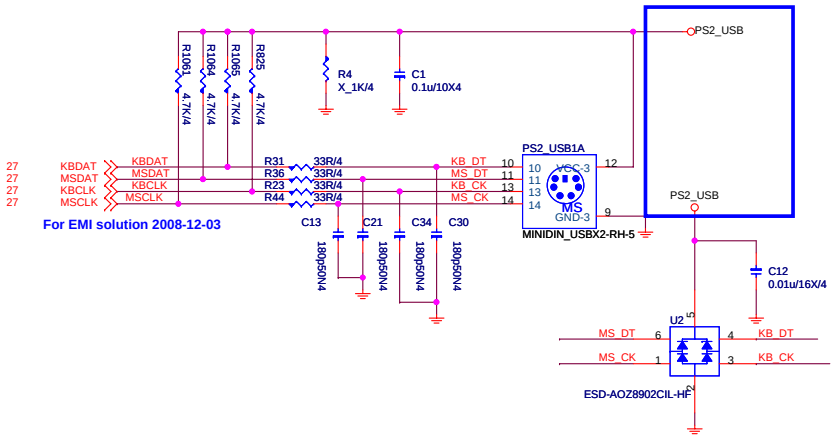
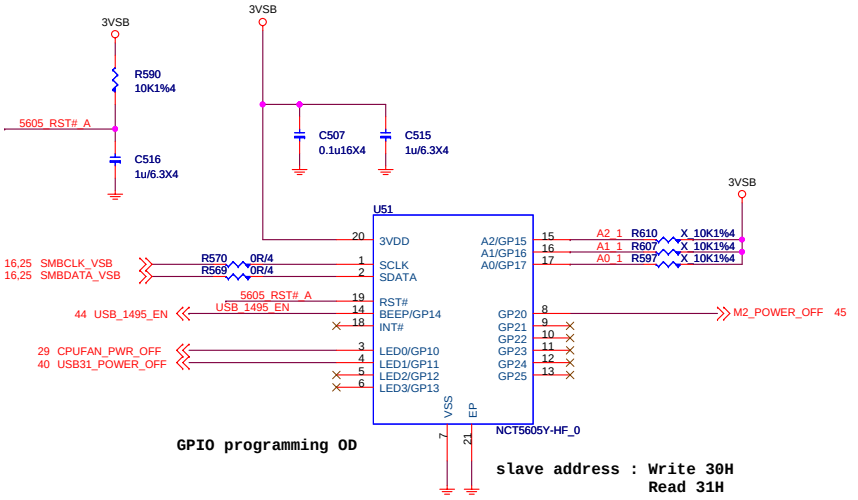
PS2 KEYBOARD & MOUSE CONNECTOR

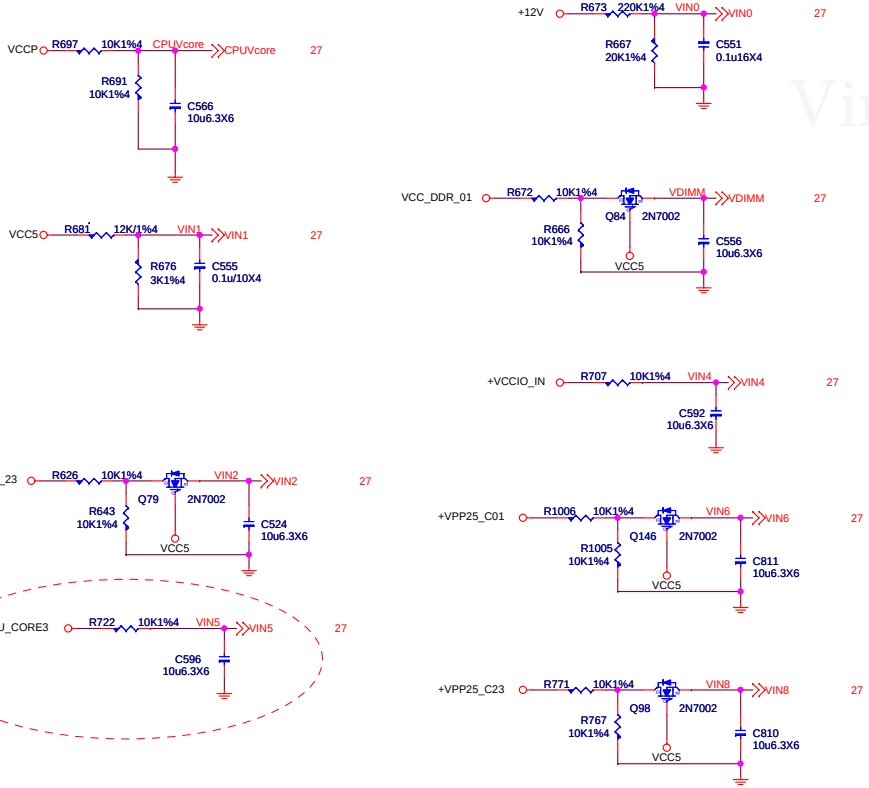




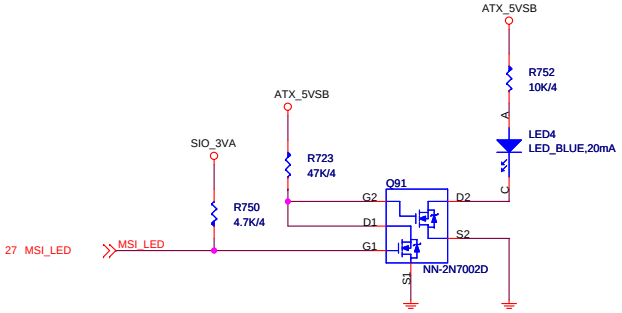
GPIO programming OD

slave address : Write 30H
Read 31H

HW Monitor - Voltage



MSI_LED



MICRO-STAR INT'L CO.,LTD

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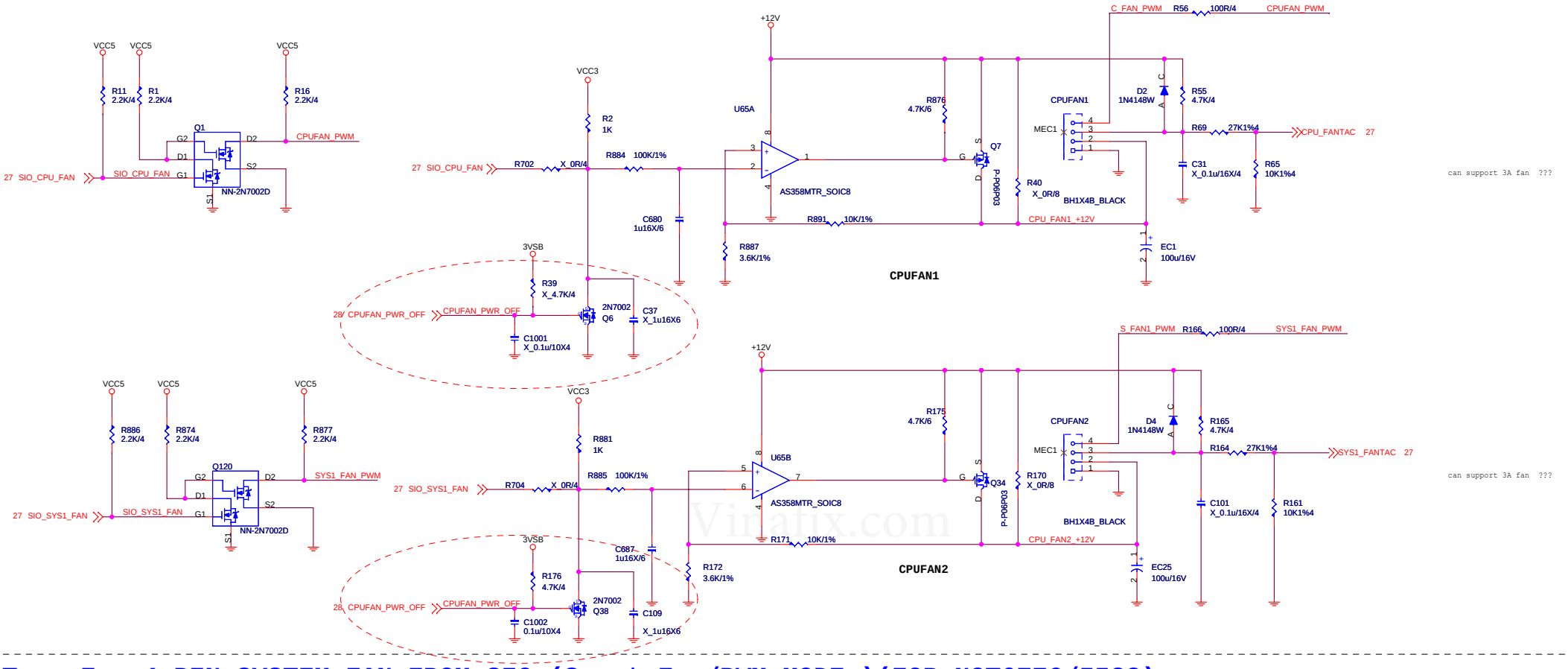
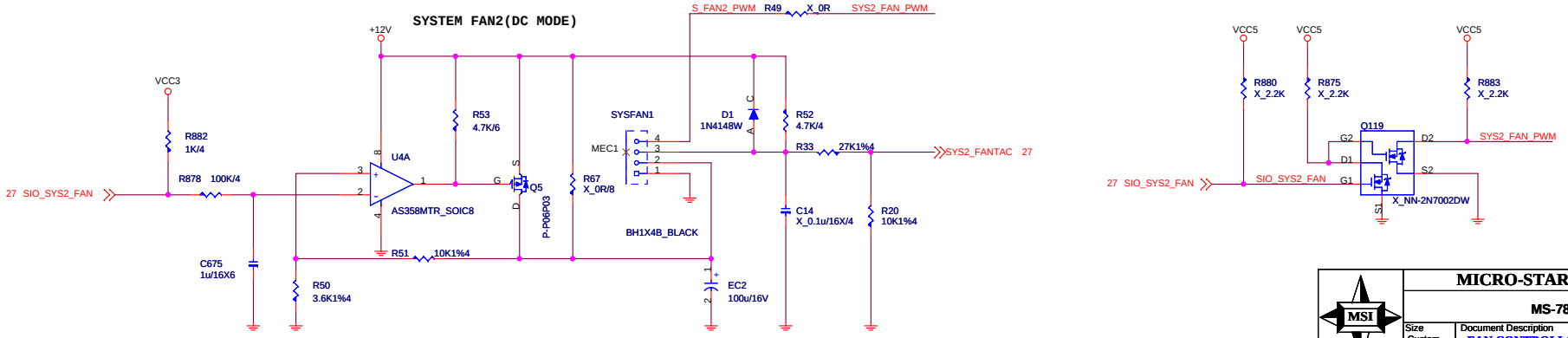
Type E : 4 PIN CPU FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6776/5533)



Type F : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6776/5533)



MICRO-STAR INT'L CO.,LTD

MS-7885

Size	Document Description	Rev
Custom	FAN CONTROLLOR-1	30

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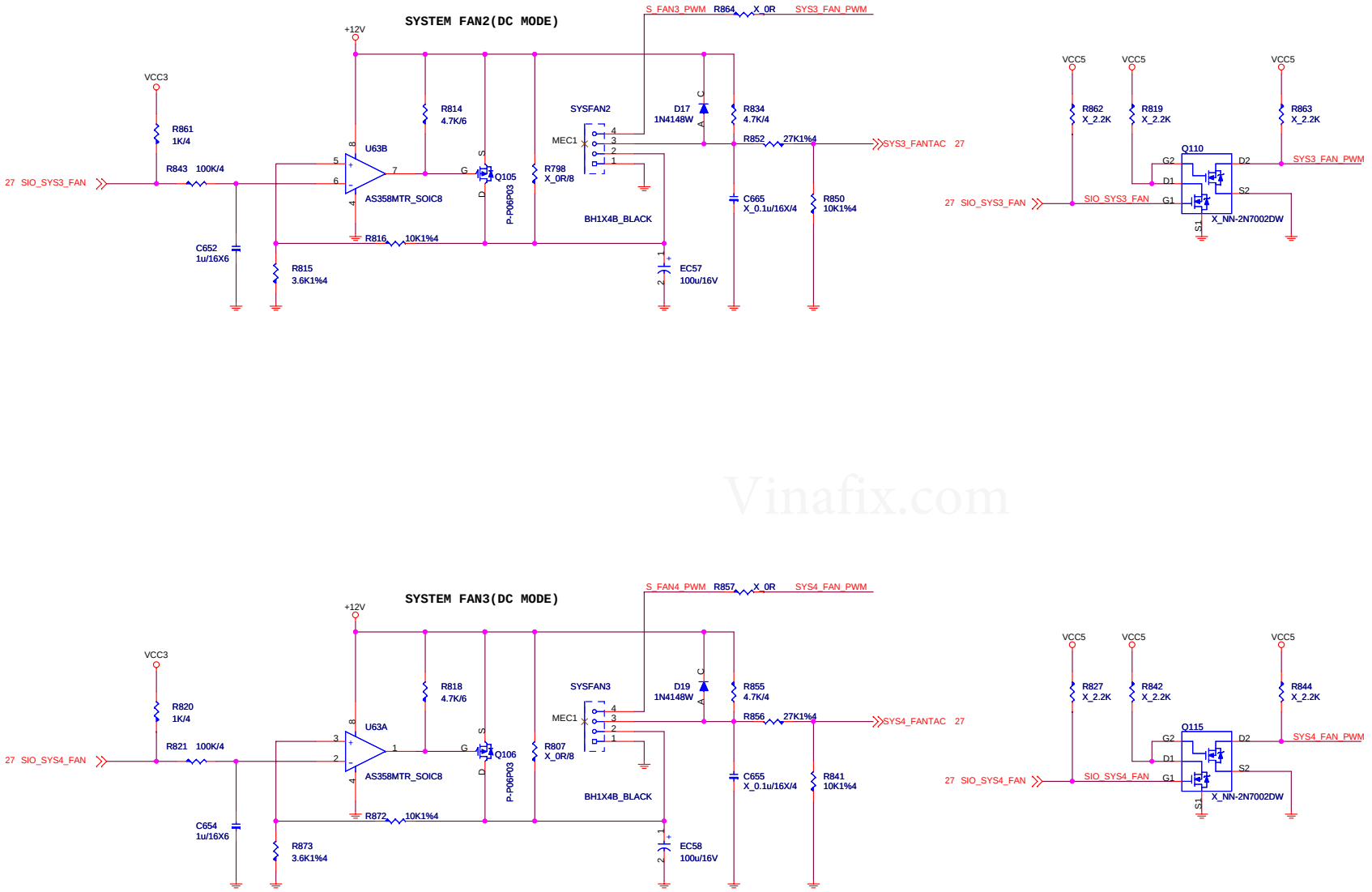
Type F : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6776/5533)



MICRO-STAR INT'L CO.,LTD

MS-7885

Size	Document Description	Rev
Custom	FAN CONTROLLOR-2	30

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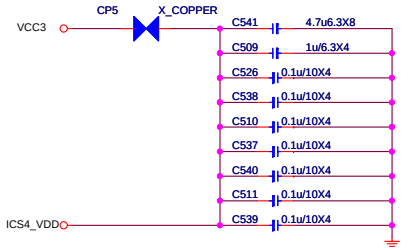
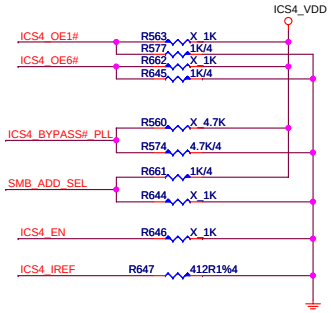
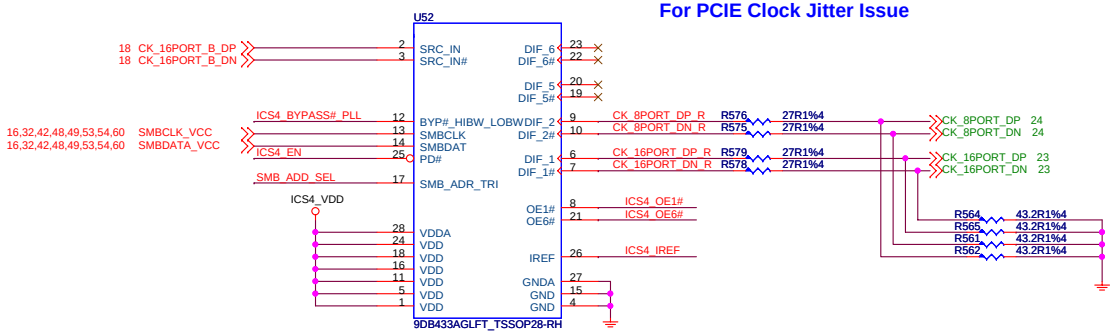
CLK Buffer_9DB433

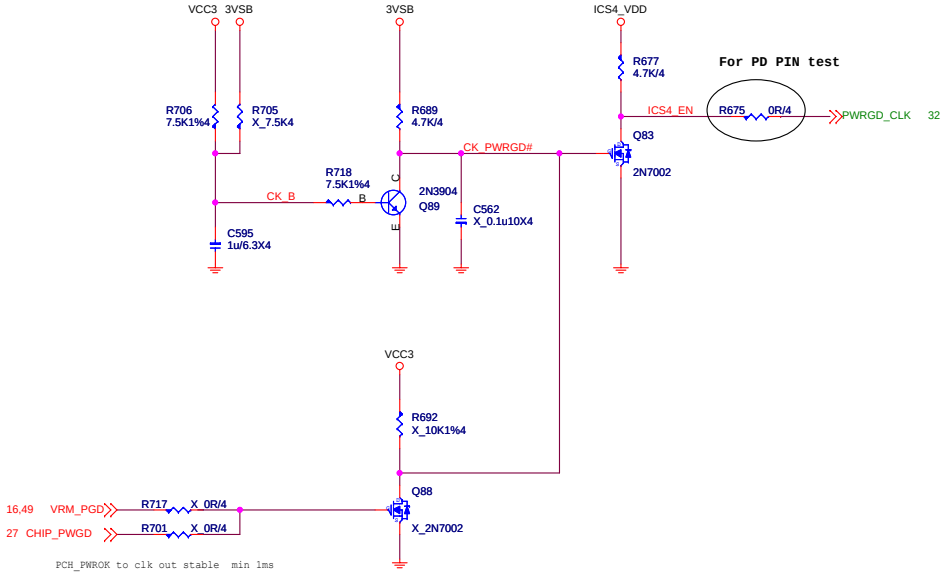






For PCIE Clock Jitter Issue

Address: D8/D9



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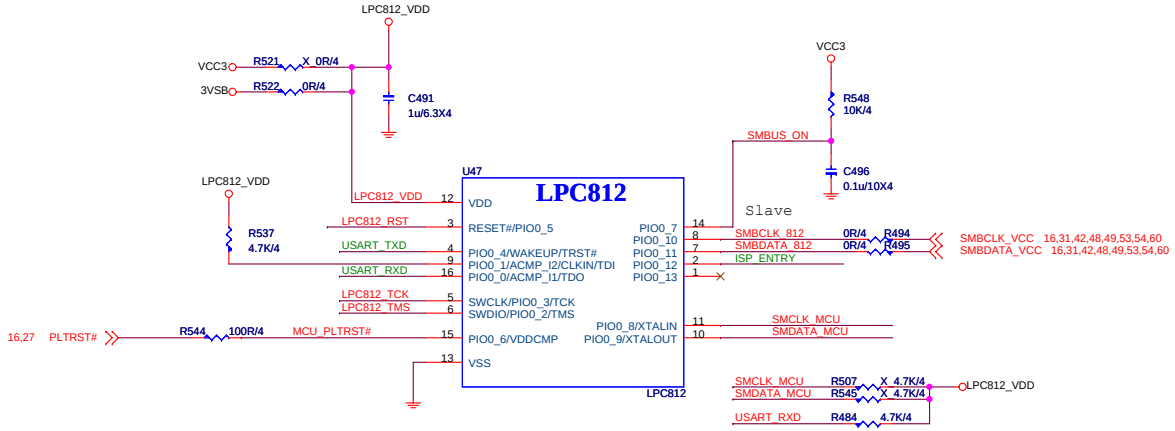
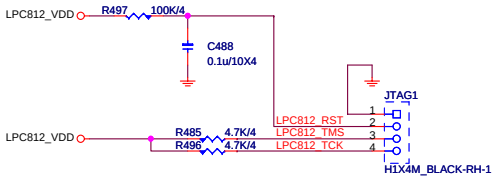
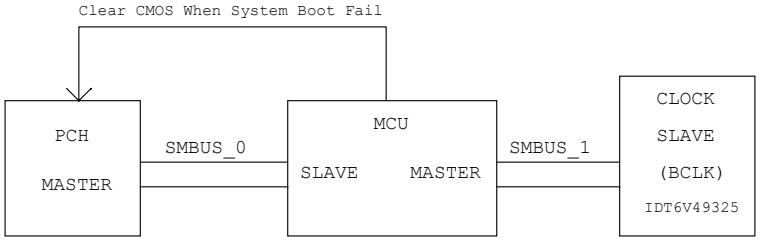
SIO 6792 , GPIO13
default low , active high

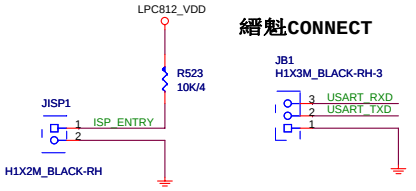


JTAG for SW DEBUG

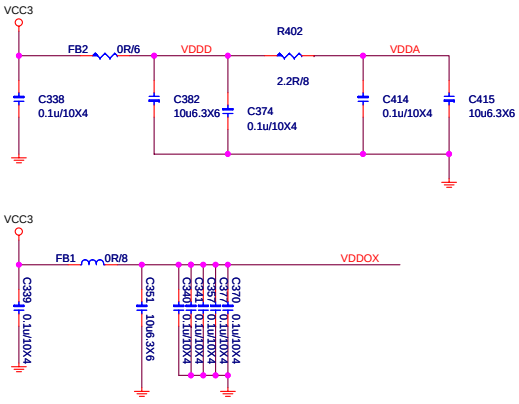


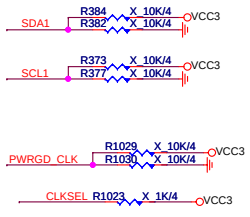


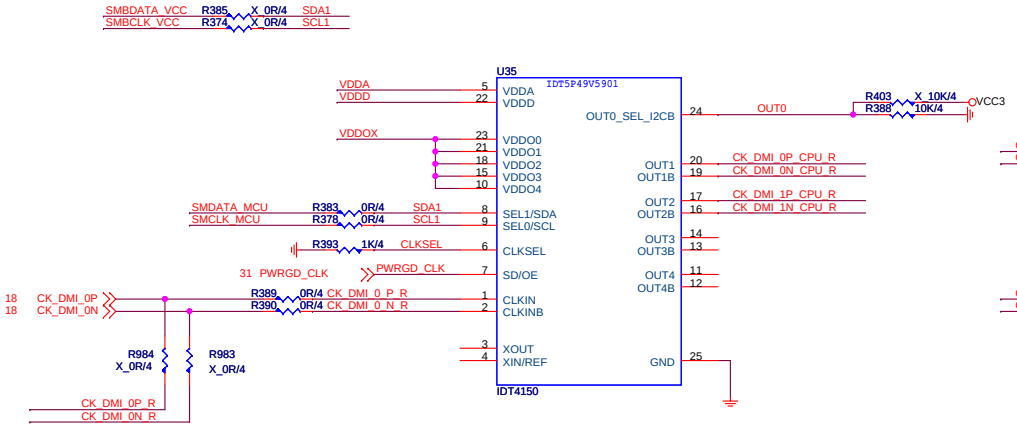
繙魁CONNECT

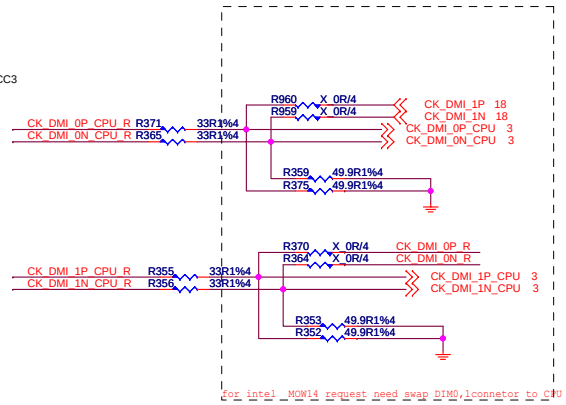


CLK GEN-IDT5P49V5901









Length match DMI1-to-BCLK0 pair and DMI0-to-BCLK1 within +/- 250 mils.
When length matching, recommend DMI0-to-BCLK1 have the shorter route length compared to DMI1-to-BCLK0.

PIN:CLKSEL. Input clock select. Selects the active input reference source in manual switchover mode.
0 = XIN/REF, XOUT (default)
1 = CLKIN, CLKINB

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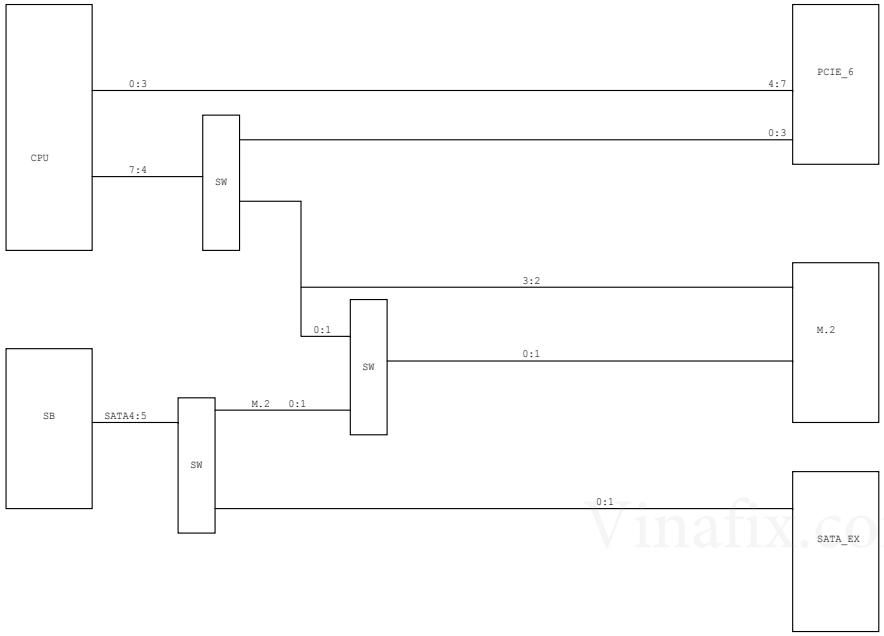

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MS-7885		
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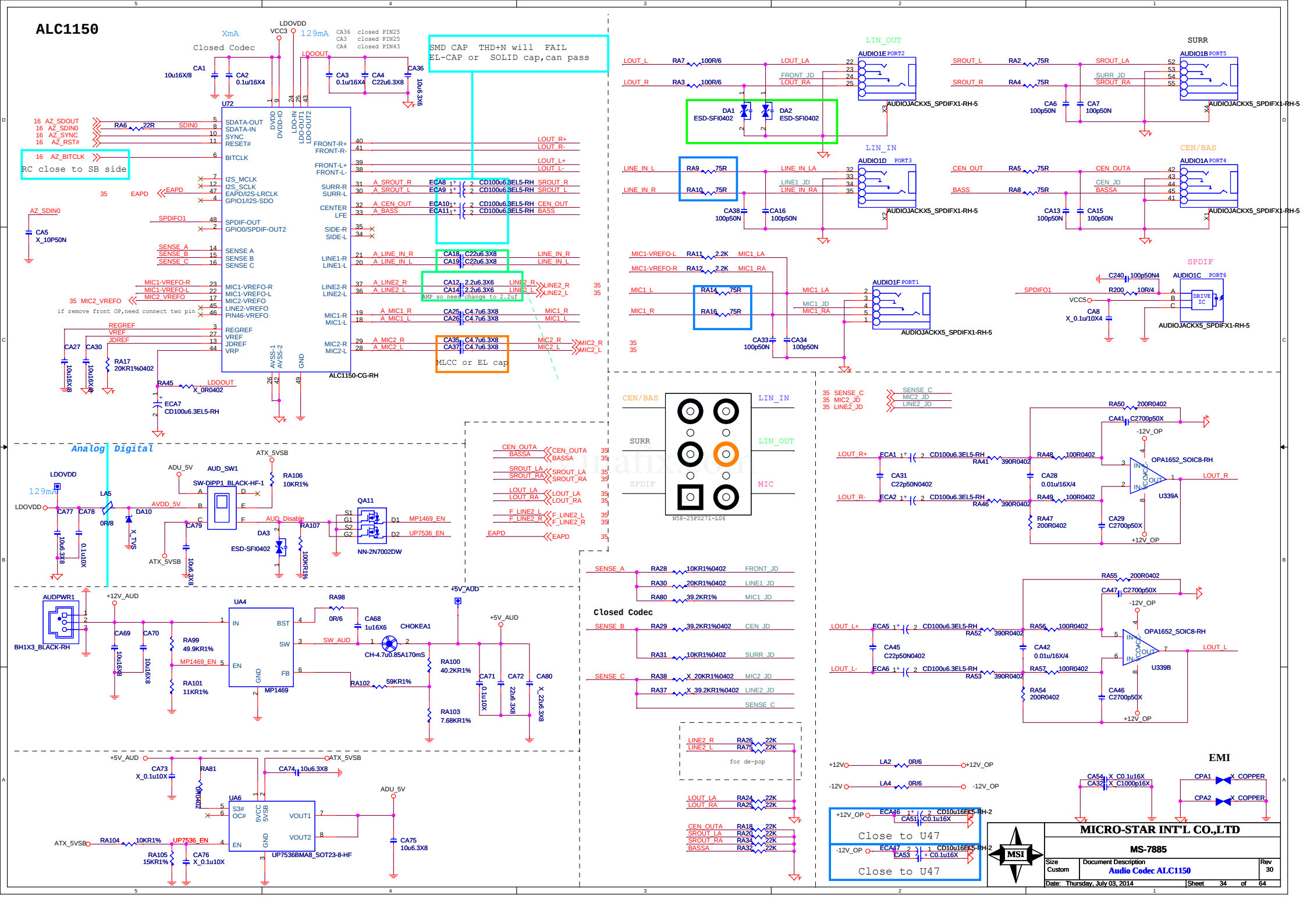
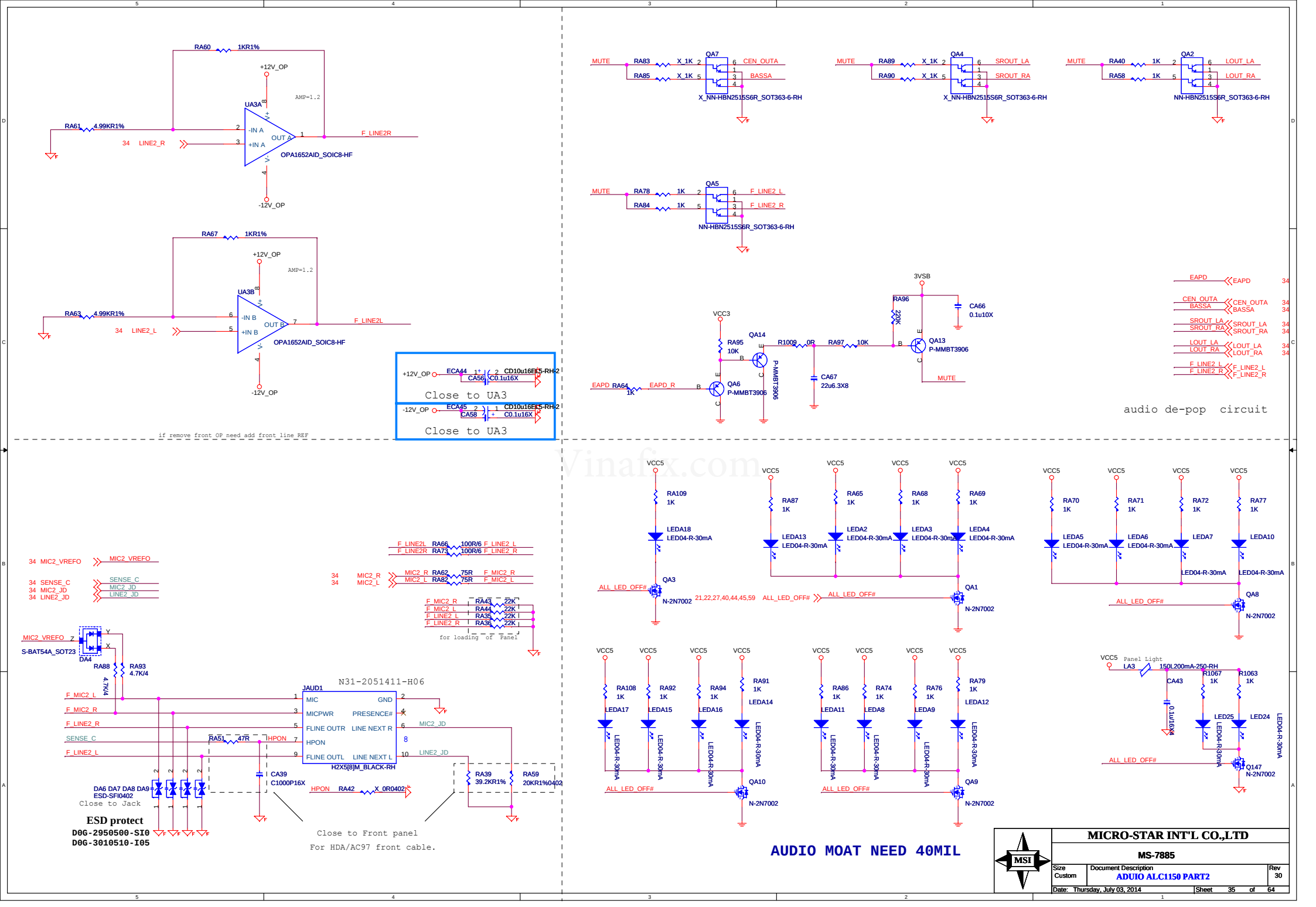
ALC1150


XmA
Closed Codec
129mA
SMD CAP THD+N will FAIL
EL-CAP or SOLID cap,can pass
U72
ALC1150-CG-RH
RC close to SB side
MLCC or EL cap
LIN_OUT
SURR
LIN_IN
CEN/BAS
SPDIF
AUDIOJACKX5_SPDIFX1-RH-5
Analog
Digital
Closed Codec
MICRO-STAR INT'L CO.,LTD
MS-7885
Audio Codec ALC1150
Thursday, July 03, 2014
EMI


RA60 1KR1%
+12V_OP
AMP=1.2
UA3A
RA61 4.99KR1%
34 LINE2_R
-IN A
+IN A
OUT A
OPA1652AID_SOIC8-HF
F_LINE2R
-12V_OP
RA67 1KR1%
UA3B
RA63 4.99KR1%
34 LINE2_L
-IN B
+IN B
OUT B
F_LINE2L
if remove front OP need add front line REF
ECA44 CA56 CD10u16E5-RH-2 C0.1u16X
Close to UA3
ECA45 CA58 CD10u16E5-RH-2 C0.1u16X
Close to UA3
MUTE RA83 RA85 X_1K QA7 CEN_OUTA BASSA X_NN-HBN2515S6R_SOT363-6-RH
MUTE RA89 RA90 X_1K QA4 SROUT_LA SROUT_RA X_NN-HBN2515S6R_SOT363-6-RH
MUTE RA40 RA58 1K QA2 LOUT_LA LOUT_RA NN-HBN2515S6R_SOT363-6-RH
MUTE RA78 RA84 1K QA5 F_LINE2_L F_LINE2_R NN-HBN2515S6R_SOT363-6-RH
3VSB
VCC3
RA95 10K
QA14
RA96 220K
CA66 0.1u10X
R1009 0R
RA97 10K
QA13 P-MMBT3906
CA67 22u6.3X8
EAPD RA64 1K EAPD_R
QA6 P-MMBT3906
MUTE
EAPD
CEN_OUTA
BASSA
SROUT_LA
SROUT_RA
LOUT_LA
LOUT_RA
F_LINE2_L
F_LINE2_R
audio de-pop circuit
34 MIC2_VREFO
34 SENSE_C
34 MIC2_JD
34 LINE2_JD
F_LINE2L RA66 100R/6 F_LINE2_L
F_LINE2R RA73 100R/6 F_LINE2_R
34 MIC2_R
34 MIC2_L
RA62 75R F_MIC2_R
RA82 75R F_MIC2_L
RA43 22K
RA44 22K
RA35 22K
RA36 22K
for loading of Panel
S-BAT54A_SOT23
DA4
RA88 4.7K/4
RA93 4.7K/4
N31-2051411-H06
JAUD1
MIC
GND
MICPWR
PRESENCE#
FLINE OUTR
LINE NEXT R
HPON
FLINE OUTL
LINE NEXT L
H2X5[8]M_BLACK-RH
RA51 47R
CA39 C1000P16X
DA6 DA7 DA8 DA9 ESD-SFI0402
Close to Jack
ESD protect
D0G-2950500-SI0
D0G-3010510-I05
HPON RA42 X_0R0402
RA39 39.2KR1%
RA59 20KR1%0402
Close to Front panel
For HDA/AC97 front cable.
VCC5
RA109 1K
LEDA18 LED04-R-30mA
QA3 N-2N7002
ALL_LED_OFF#
21,22,27,40,44,45,59
RA87 RA65 RA68 RA69 1K
LEDA13 LEDA2 LEDA3 LEDA4 LED04-R-30mA
QA1 N-2N7002
RA70 RA71 RA72 RA77 1K
LEDA5 LEDA6 LEDA7 LEDA10 LED04-R-30mA
QA8 N-2N7002
RA108 RA92 RA94 RA91 1K
LEDA17 LEDA15 LEDA16 LEDA14
QA10 N-2N7002
RA86 RA74 RA76 RA79 1K
LEDA11 LEDA8 LEDA9 LEDA12
QA9 N-2N7002
Panel Light
LA3 150L200mA-250-RH
CA43 0.1u16X
R1067 1K
R1063 1K
LEDA25 LEDA24
Q147 N-2N7002
AUDIO MOAT NEED 40MIL
MICRO-STAR INT'L CO.,LTD
MS-7885
Size Custom
Document Description
ADUIO ALC1150 PART2
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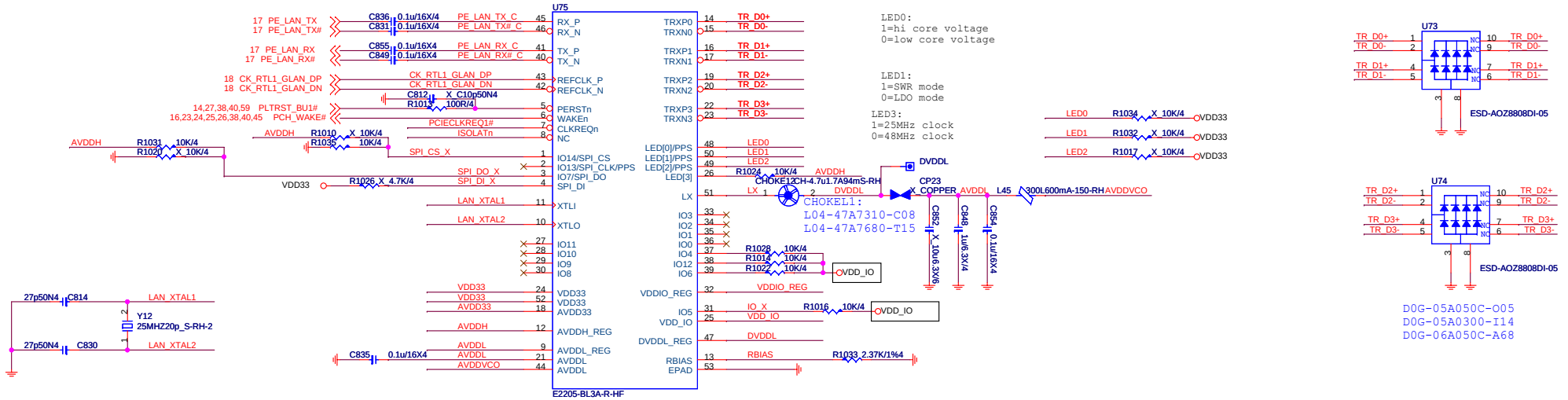
Reserve ESD Protect



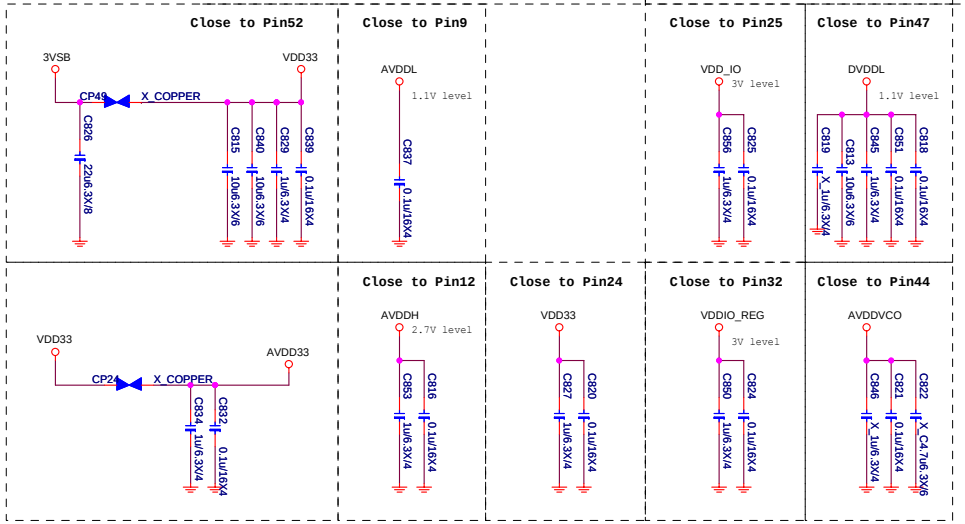
VDD33 power trace should be wider than 30mils;
AVDD33 power trace should be wider than 30mils;
VDD_IO power trace should be wider than 30mils;
VDDIO_REG power trace should be wider than 20mils;
AVDDH power trace should be wider than 20mils;
AVDDL power traces should be wider than 20mils.
DVDDL power traces should be wider than 20mils.

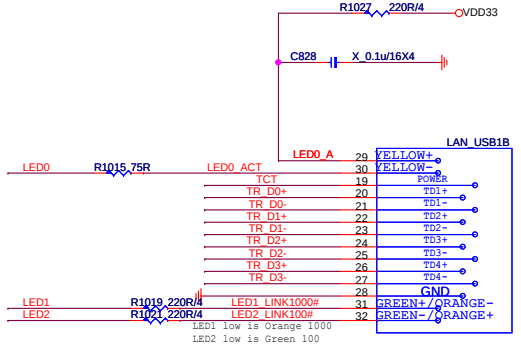
Remove pull-up R if R4 existence on motherboard
(or SB has internal pull-up R).

PCIECLKREQ1# R1025 X 4.7K/4 VDD33

AVDDH R1018 10K/4 ISOLATn

IO:
1. Support xD, not support SPI
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFus
01:
1. Support SPI, not support xD
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFus
11:
1. Not support xD, not support SPI
2. Only support PPS, PPS always at CRIO13.





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MS-7885	
Size: Custom	Document Description: LAN-E2205 — Rev: 30
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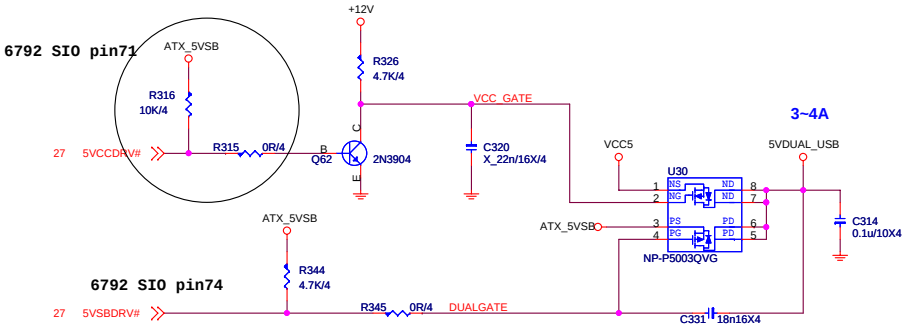
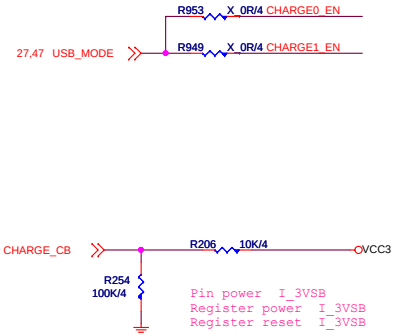
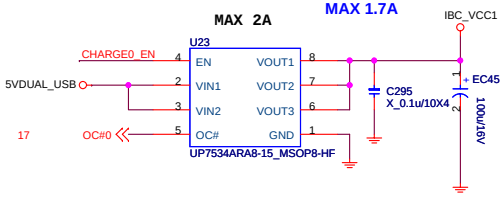
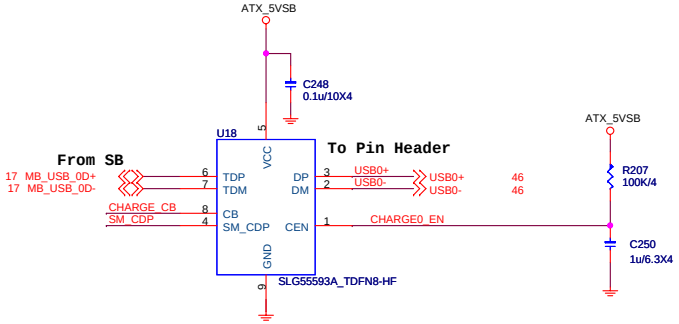
5VDUAL_USB - uP7501





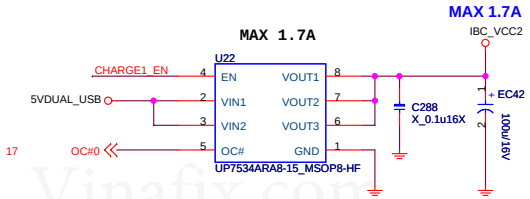
USB POWER PORT 0 For USB Charging

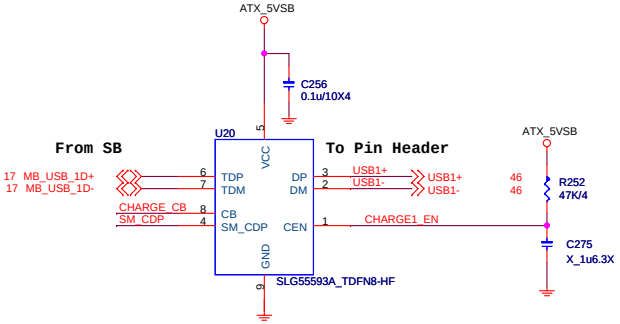


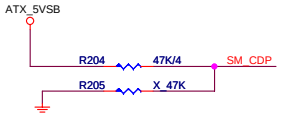


Switch Control Bit
0 = autodetection charger identification active
1 = charging downstream port with active USB2.0 data communication mode with 1.5A support

USB POWER PORT 1 For USB Charging







Vinafix

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MS-7885		
Size: Custom	Document Description: USB CHARGE_SLG55593A	Rev: 30
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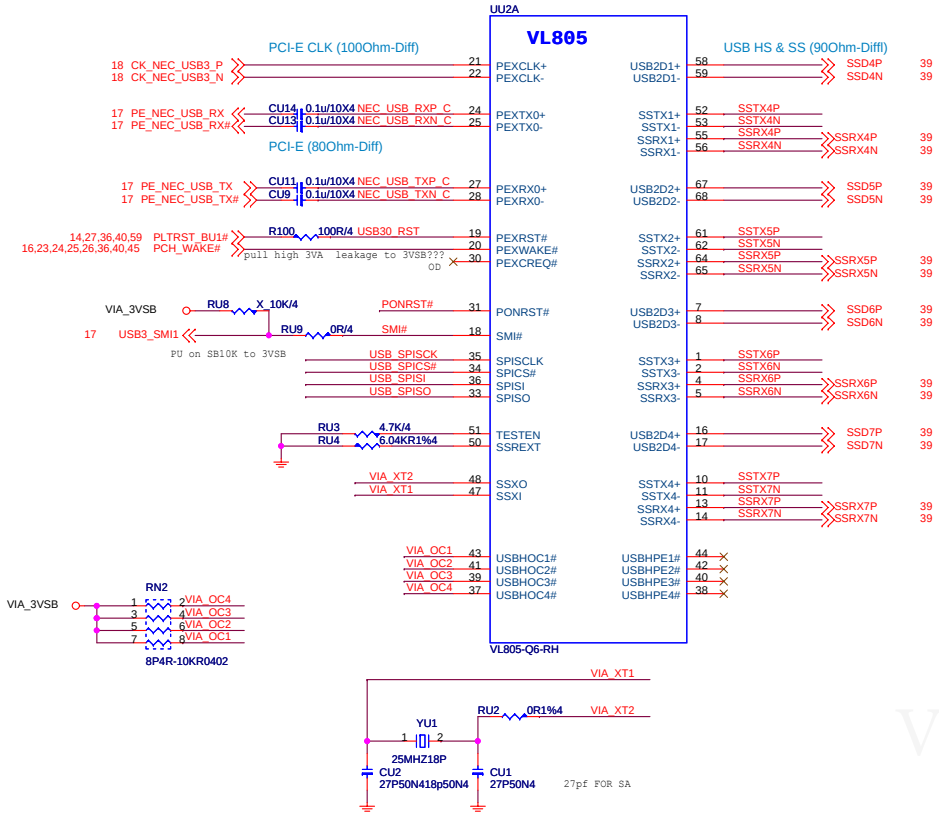
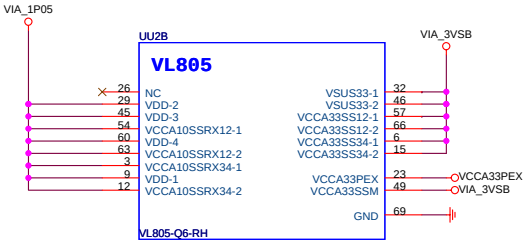
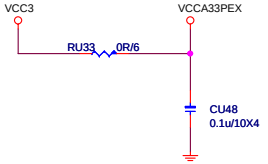
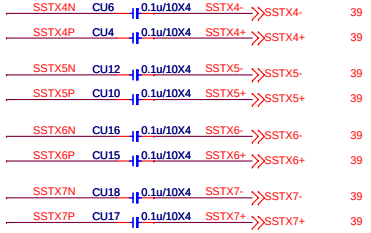
nec-USB30-4PORT

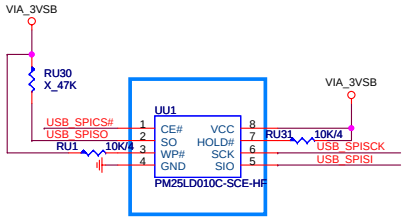


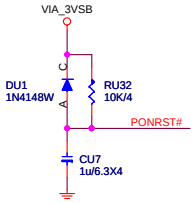






EEPROM



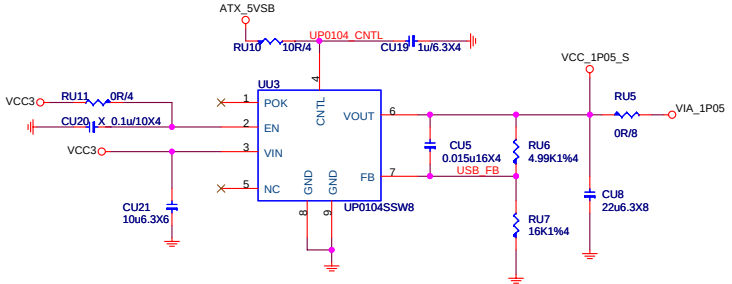


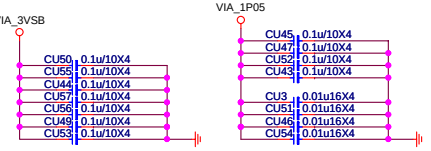
3VSB R895 0R/8 VIA_3VSB

Resered Bead.

1.05V core Power

Max Power disspation: (3.3 V-1.05V)*0.247A=0.55575W
VIA Core Power: VIA_1P05 247mA





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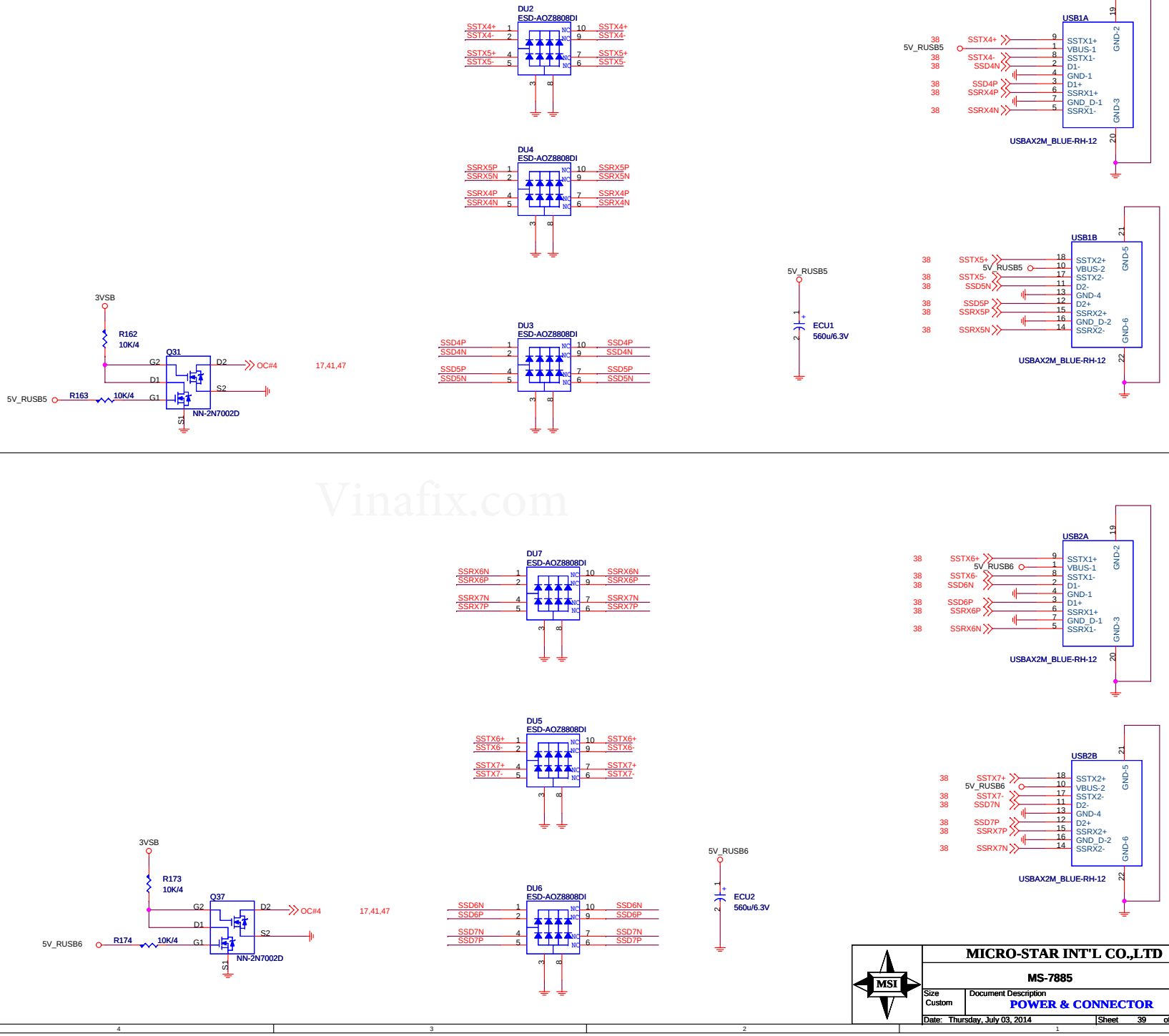
VL805-USB30-4PORT CONN

Rear I/O

Close to Connector



MICRO-STAR INT'L CO.,LTD		
MS-7885		
Size: Custom	Document Description: POWER & CONNECTOR	Rev: 30
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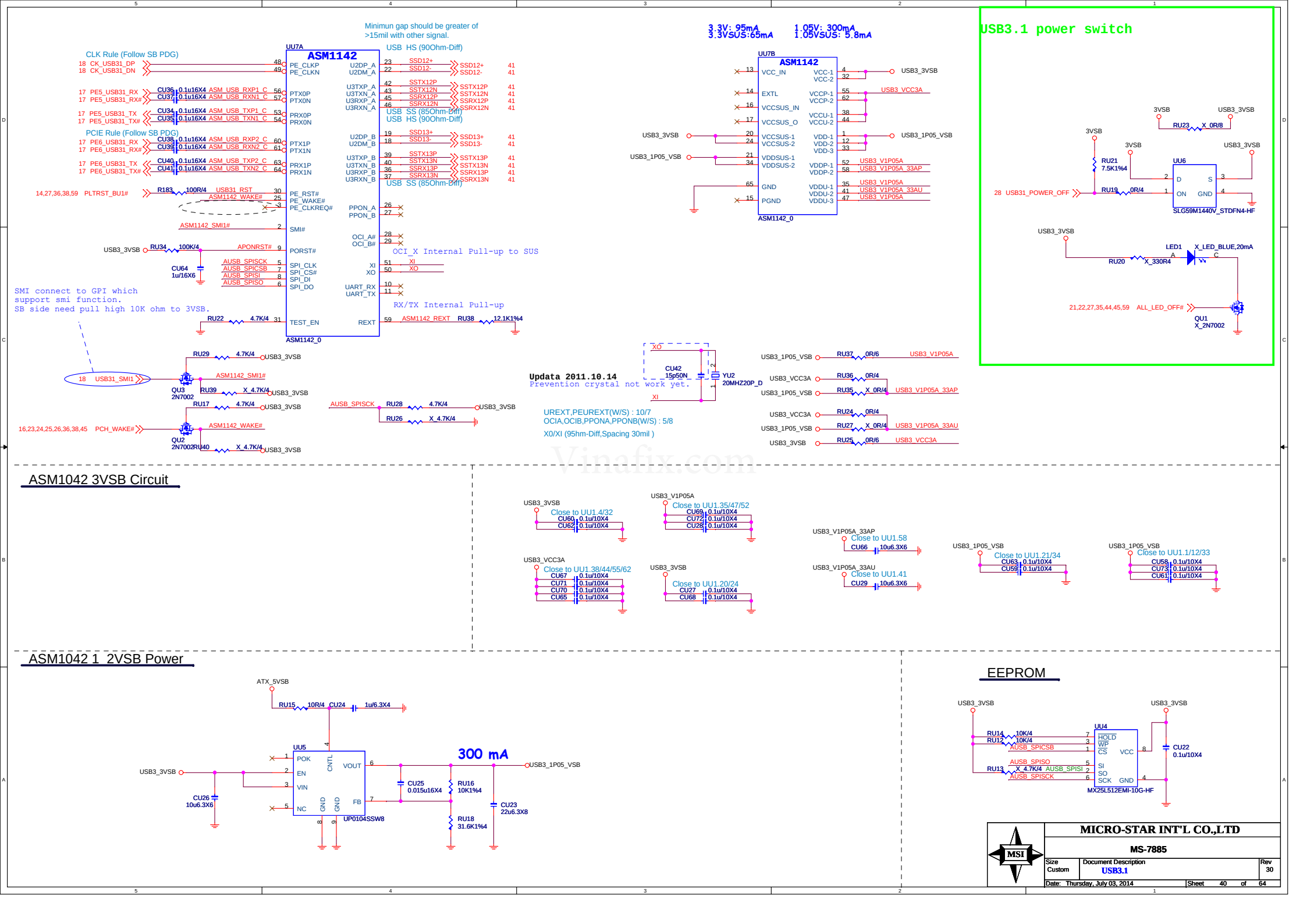
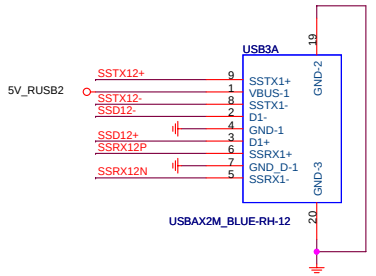
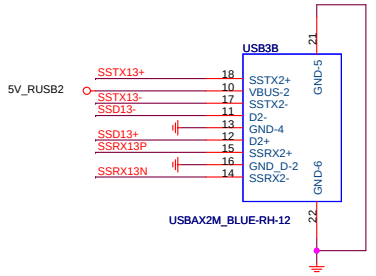
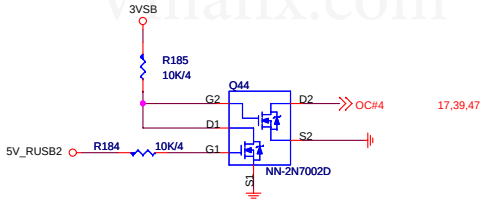

USB3.1 power switch
ASM1042 3VSB Circuit
ASM1042 1_2VSB Power
EEPROM
ASM1142
ASM1142_0
Minimun gap should be greater of
>15mil with other signal.
3.3V: 95mA
3.3VSUS:65mA
1.05V: 300mA
1.05VSUS: 5.8mA
CLK Rule (Follow SB PDG)
PCIE Rule (Follow SB PDG)
USB HS (90Ohm-Diff)
USB SS (85Ohm-Diff)
OCI_X Internal Pull-up to SUS
RX/TX Internal Pull-up
SMI connect to GPI which
support smi function.
SB side need pull high 10K ohm to 3VSB.
Updata 2011.10.14
Prevention crystal not work yet.
UREXT,PEUREXT(W/S) : 10/7
OCIA,OCIB,PPONA,PPONB(W/S) : 5/8
X0/XI (95hm-Diff,Spacing 30mil)
300 mA
MICRO-STAR INT'L CO.,LTD
MS-7885
USB3.1
Thursday, July 03, 2014

Rear USB3 CONN

Important~~
If USB3.0 signal conect to front pin header,
please must less than 0.6 inch,short trace
has better eye diagram with some bad fly cable by SI customer.

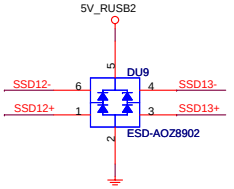


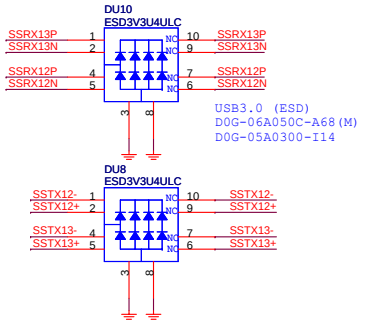


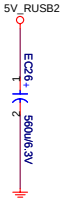


ESD Protection

NEAR CONNECTOR







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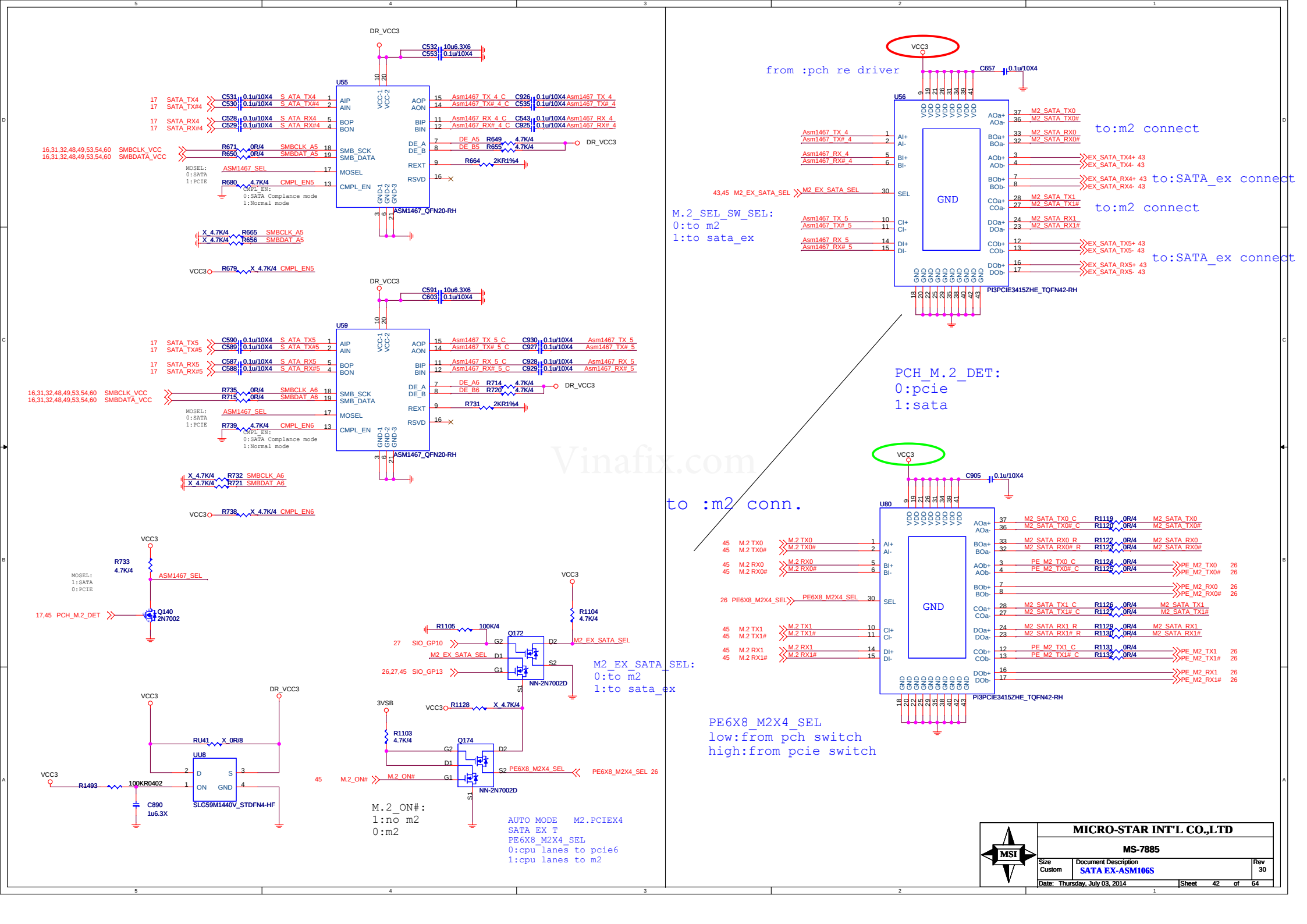
DR_VCC3
U55
ASM1467_QFN20-RH
SATA_TX4
SATA_TX#4
SATA_RX4
SATA_RX#4
SMBCLK_VCC
SMBDATA_VCC
SMBCLK_A5
SMBDAT_A5
ASM1467_SEL
CMPL_EN5
MOSEL:
0:SATA
1:PCIE
CMPL_EN:
0:SATA Complance mode
1:Normal mode
U59
SATA_TX5
SATA_TX#5
SATA_RX5
SATA_RX#5
SMBCLK_A6
SMBDAT_A6
CMPL_EN6
VCC3
R733
4.7K/4
Q140
2N7002
17,45 PCH_M.2_DET
RU41 X_0R/8
UU8
SLG59M1440V_STDFN4-HF
R1493
100KR0402
C890
1u6.3X
R1105
100K/4
Q172
NN-2N7002D
27 SIO_GP10
M2_EX_SATA_SEL
26,27,45 SIO_GP13
R1104
4.7K/4
R1128
X_4.7K/4
R1103
4.7K/4
Q174
3VSB
45 M.2_ON#
PE6X8_M2X4_SEL 26
M.2_ON#:
1:no m2
0:m2
M2_EX_SATA_SEL:
0:to m2
1:to sata_ex
AUTO MODE M2.PCIEX4
SATA EX T
PE6X8_M2X4_SEL
0:cpu lanes to pcie6
1:cpu lanes to m2
from :pch re driver
U56
PI3PCIE3415ZHE_TQFN42-RH
GND
M2_SATA_TX0
M2_SATA_TX0#
M2_SATA_RX0
M2_SATA_RX0#
M2_SATA_TX1
M2_SATA_TX1#
M2_SATA_RX1
M2_SATA_RX1#
EX_SATA_TX4+ 43
EX_SATA_TX4- 43
EX_SATA_RX4+ 43
EX_SATA_RX4- 43
EX_SATA_TX5+ 43
EX_SATA_TX5- 43
43,45 M2_EX_SATA_SEL
to:m2 connect
to:SATA_ex connect
to:m2 connect
to:SATA_ex connect
M.2_SEL_SW_SEL:
0:to m2
1:to sata_ex
PCH_M.2_DET:
0:pcie
1:sata
to :m2 conn.
U80
PE6X8_M2X4_SEL
low:from pch switch
high:from pcie switch
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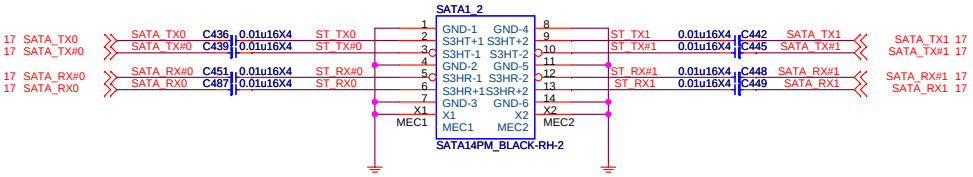
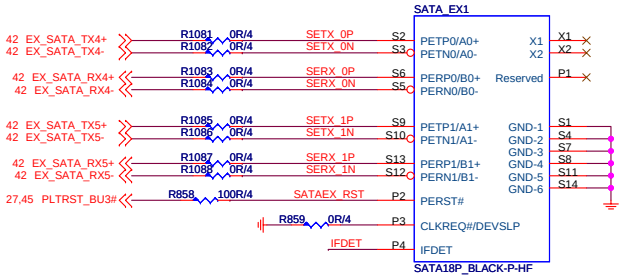
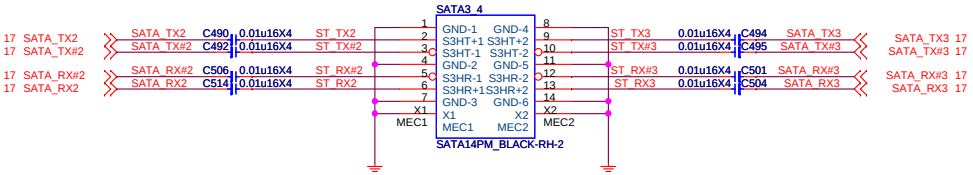
SATA 6G PORT 0.1

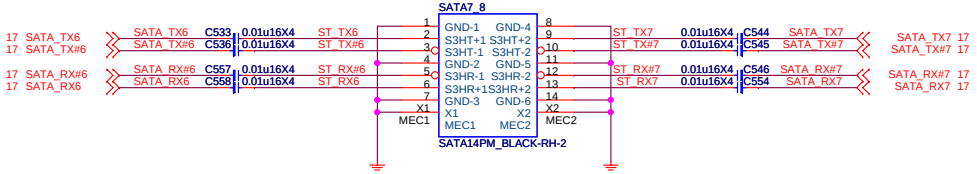


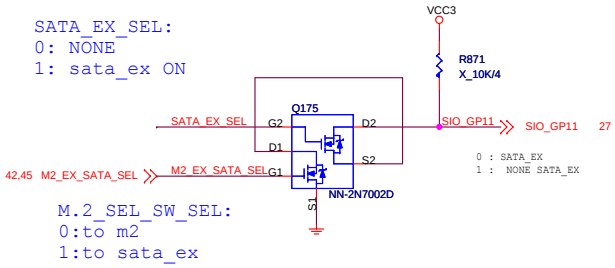


SATA 6G PORT 2.3

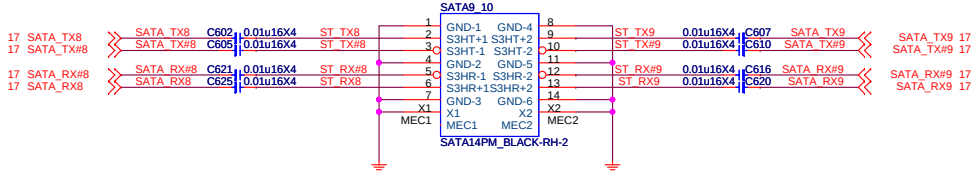


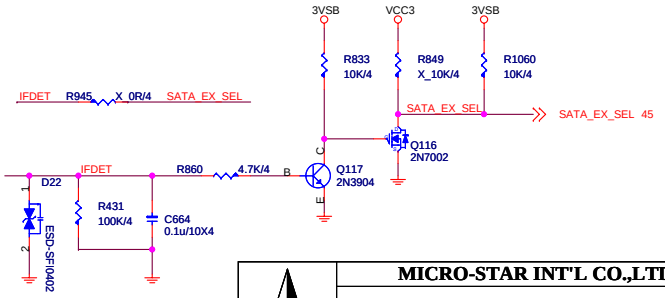
SATA 6G PORT 67





SATA 6G PORT 8.9





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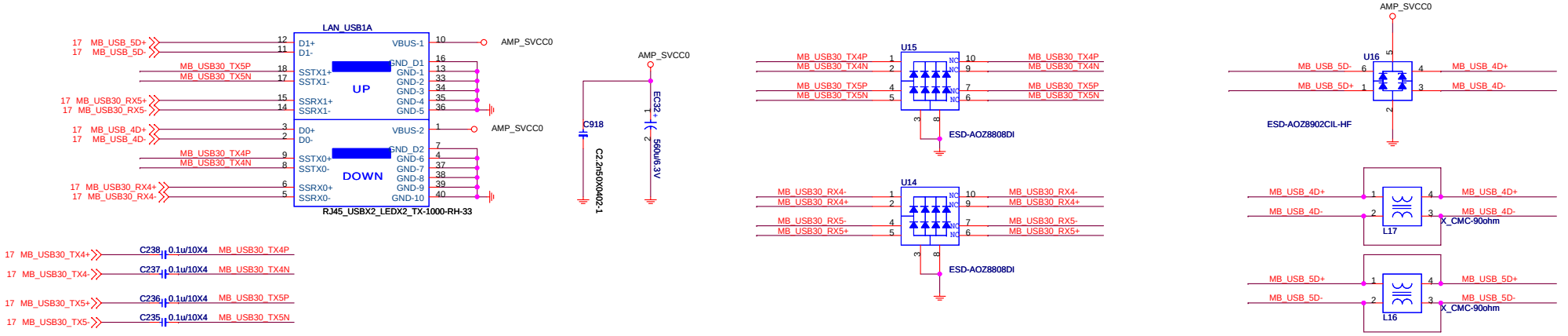
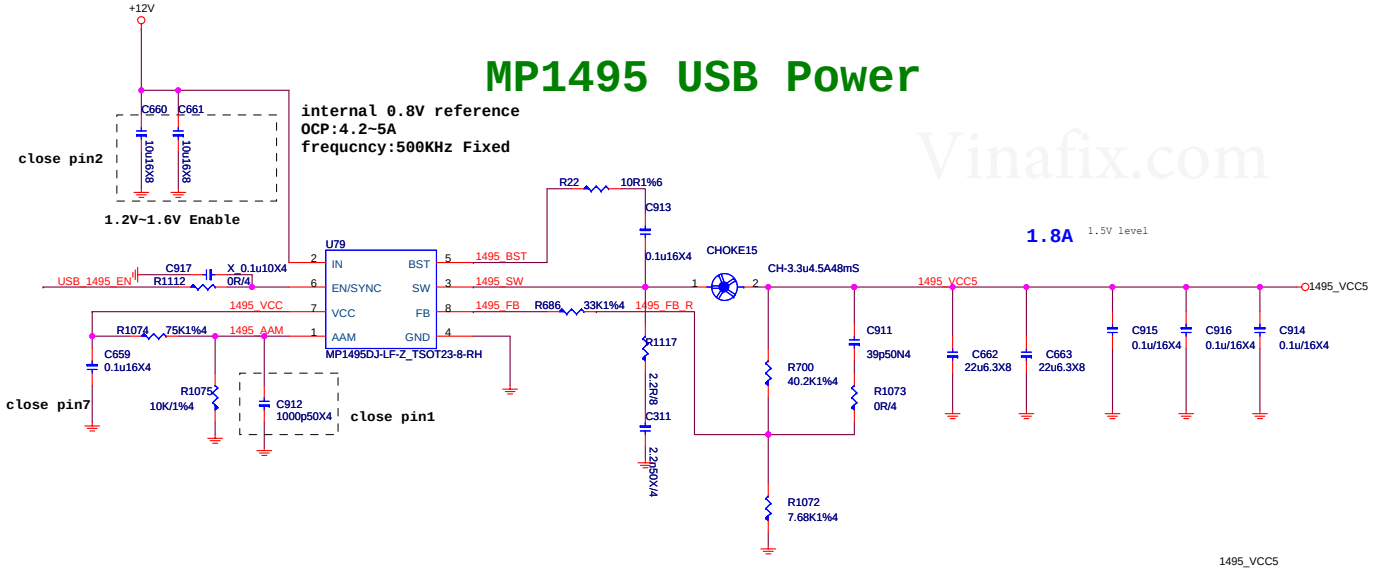
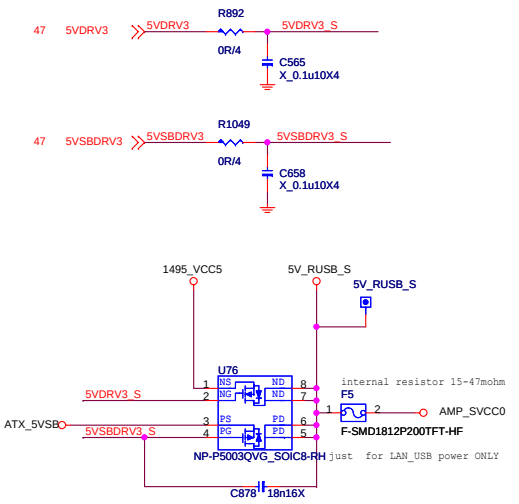
USB3.0 Connector

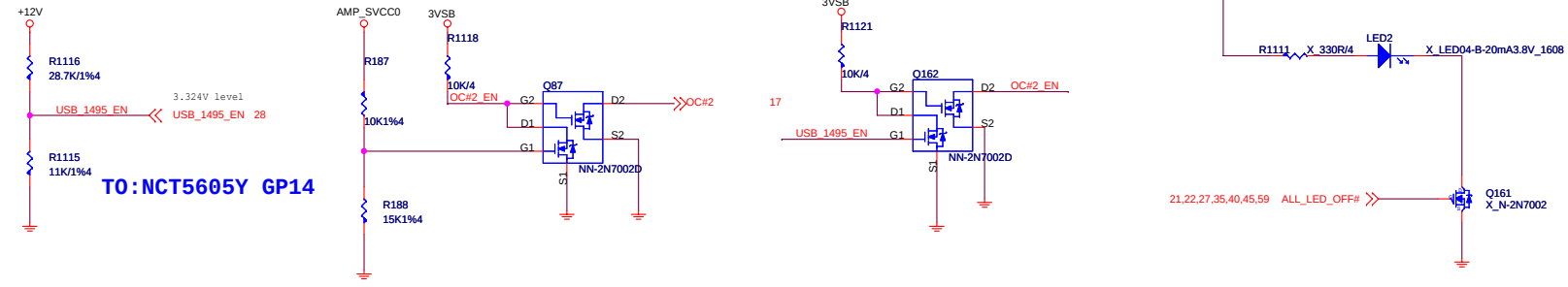


MP1495 USB Power



REAR USB PORT POWER





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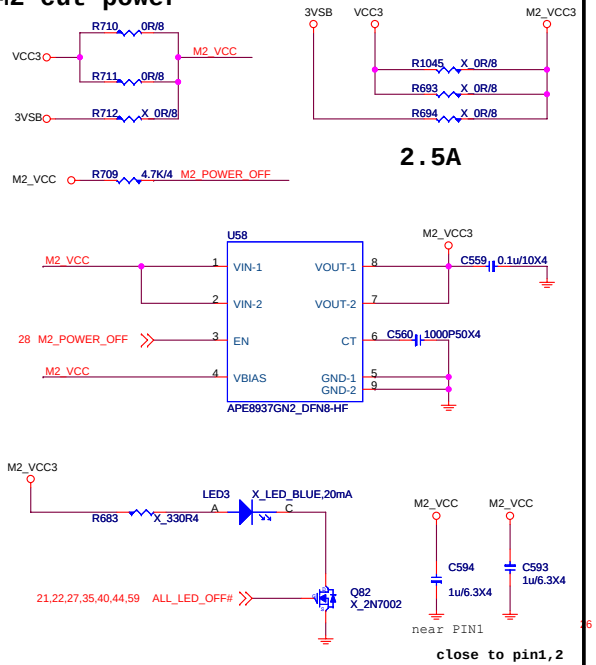
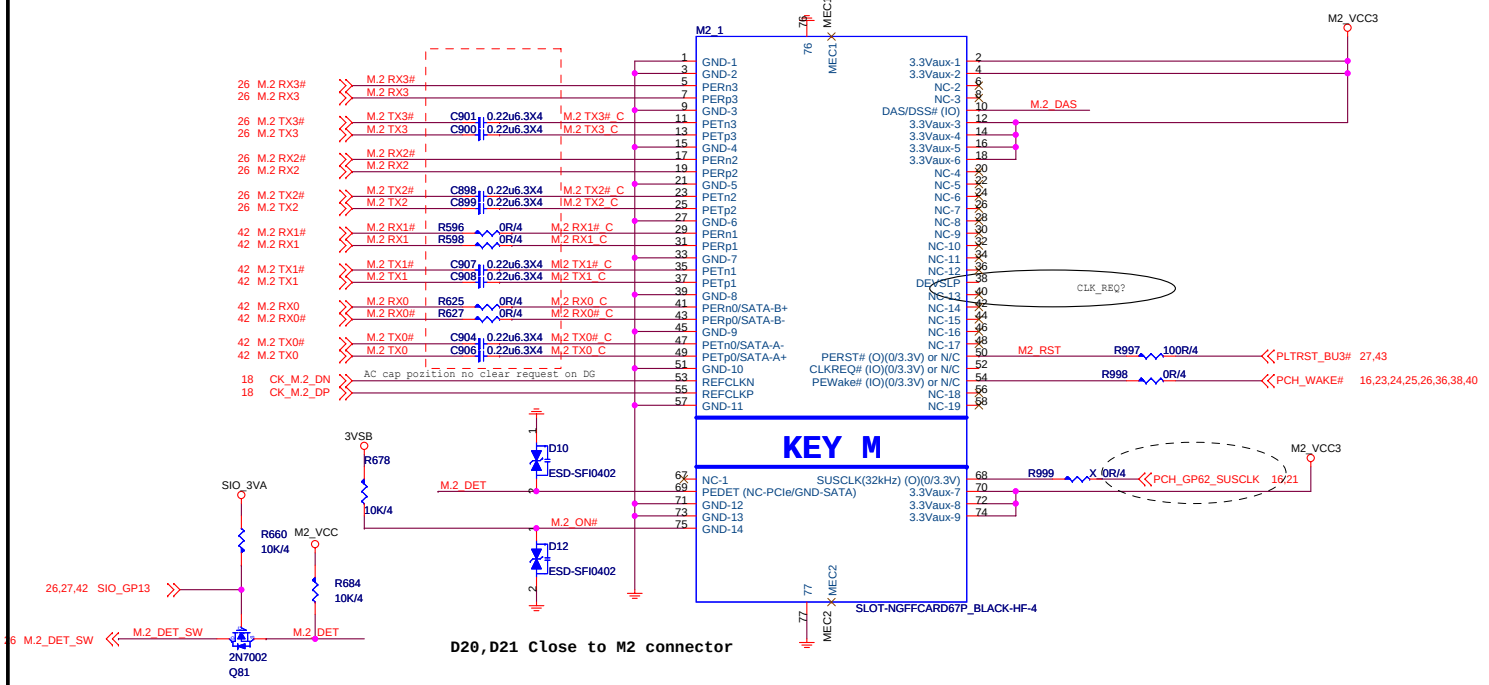
M2 cut power

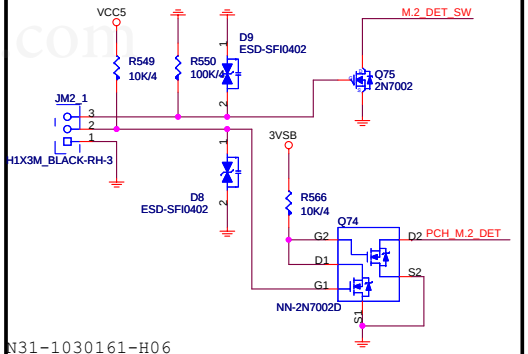


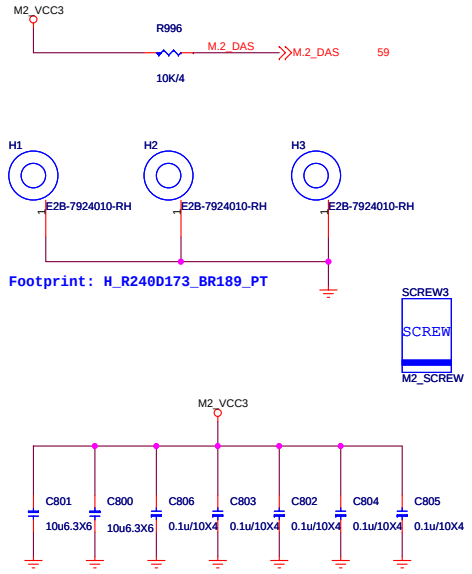


D20,D21 Close to M2 connector

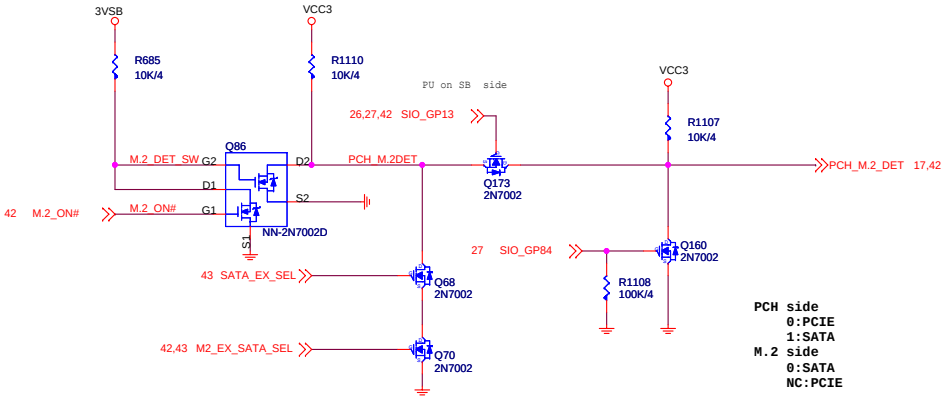
BIOS_MODE

GP10	GP11	SIO_GP84	Mode
0	0	0	M2-SATA
1	0	0	M2-PCIE
1	1	1	AUTO





SATA & PCIE SWITCH



PCH side
0:PCIE
1:SATA
M.2 side
0:SATA
NC:PCIE

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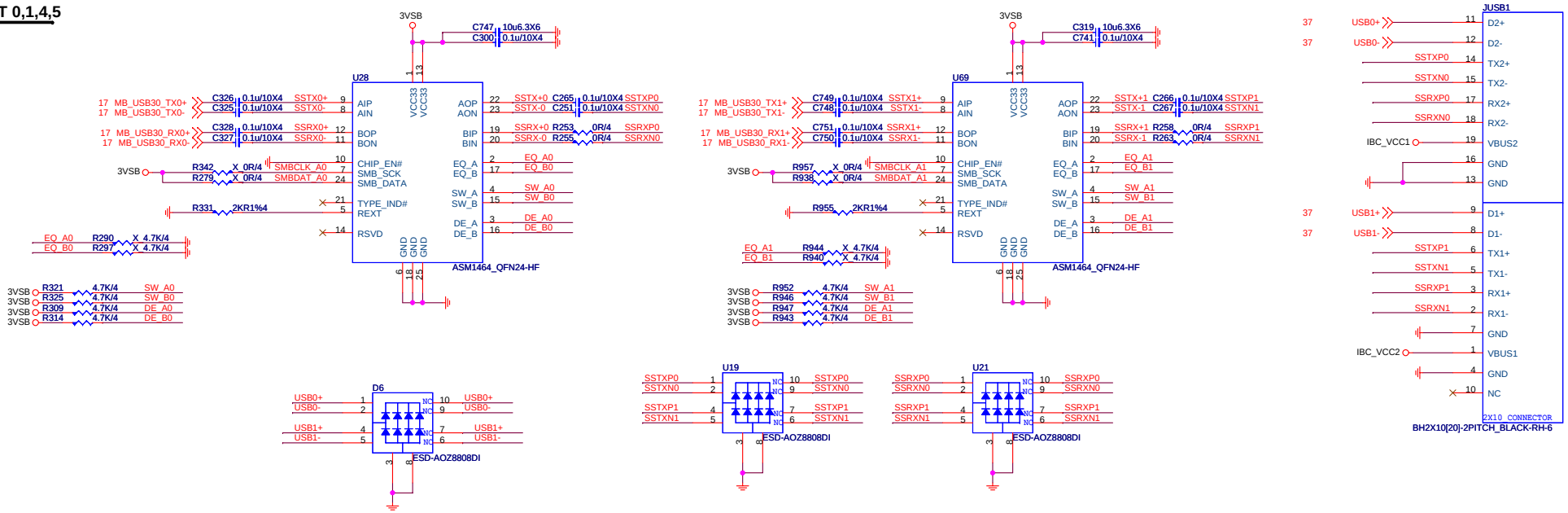
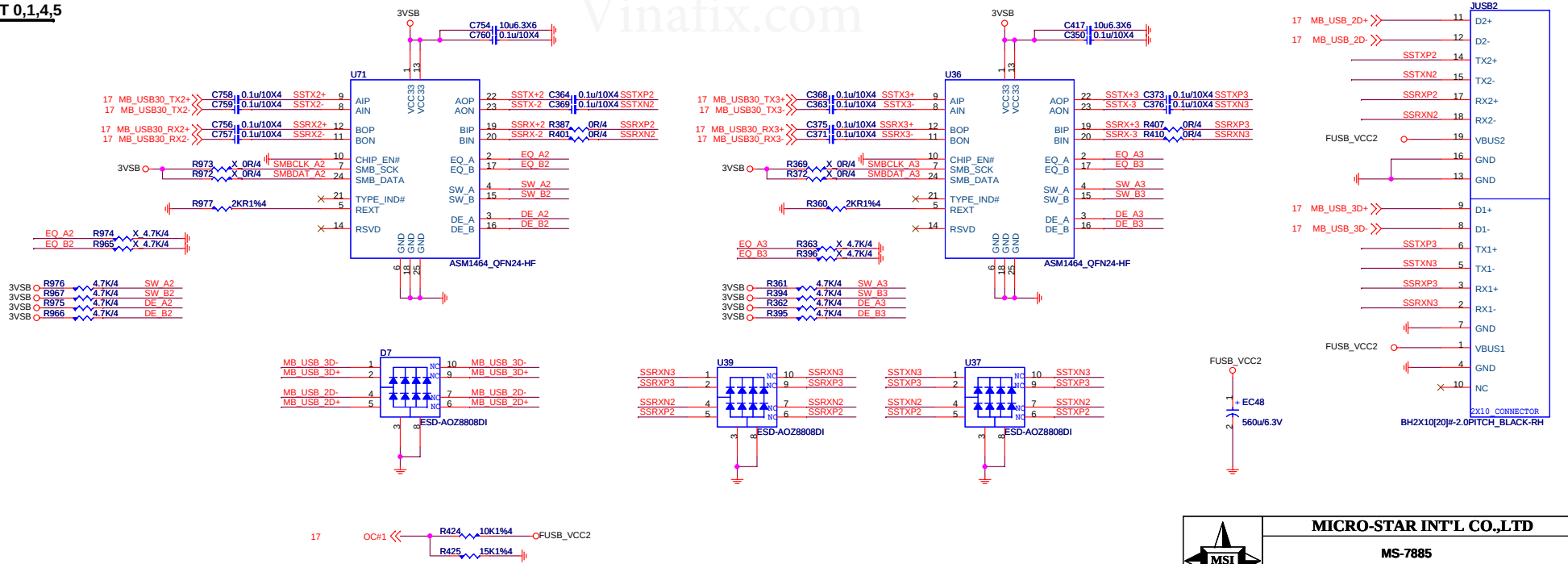
FRONT USB30 PORT 0,1,4,5

USB3.0 FRONT



FRONT USB30 PORT 0,1,4,5

USB3.0 FRONT



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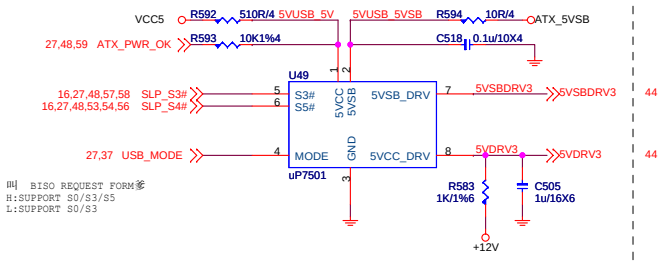
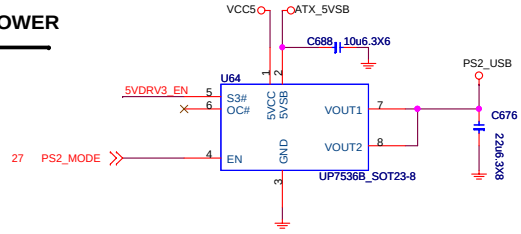
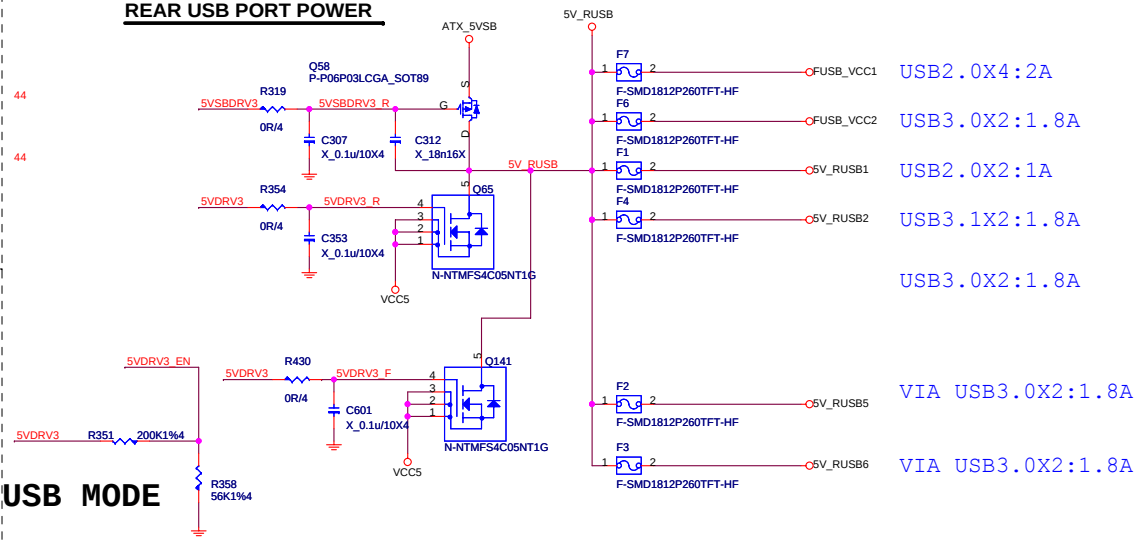
USB POWER



PS2 POWER

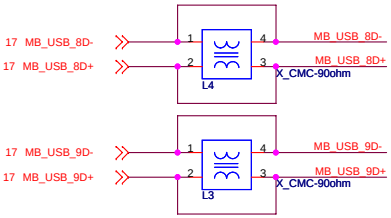


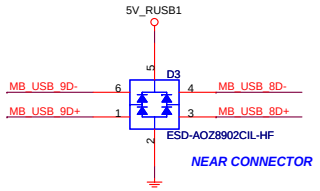
REAR USB PORT POWER

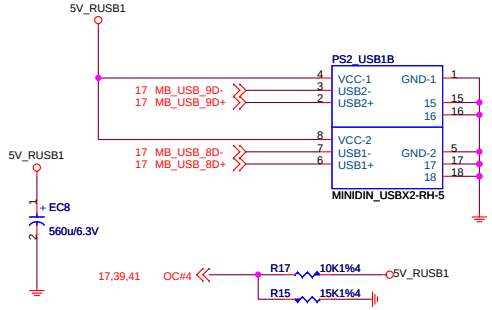


USB MODE

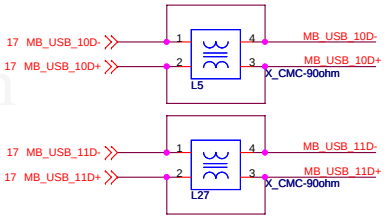
REAR USB PORT 8,9 (With PS2)

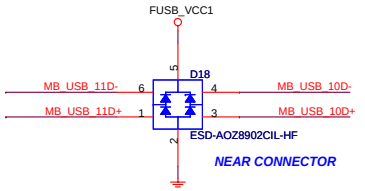


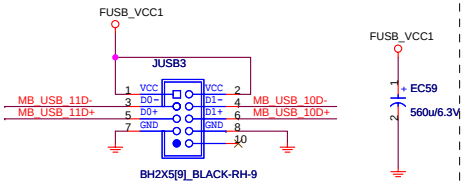




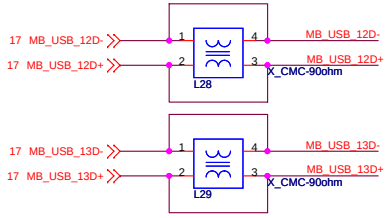
FRONT USB PORT 10.11

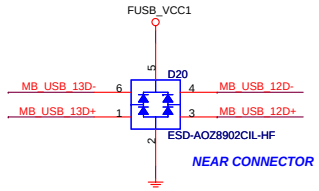


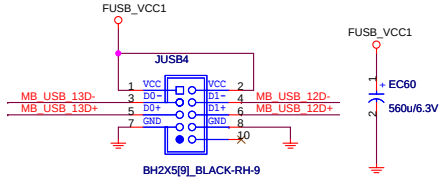




FRONT USB PORT 12,13







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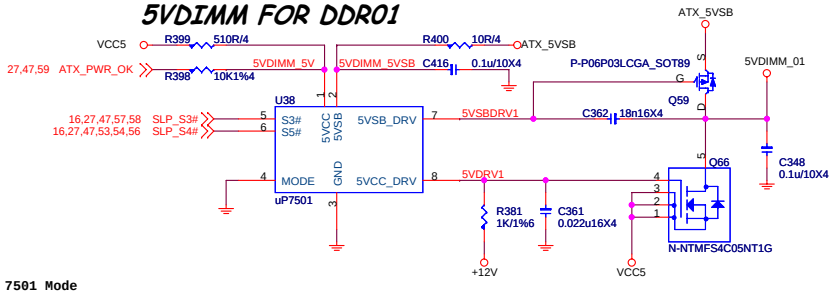

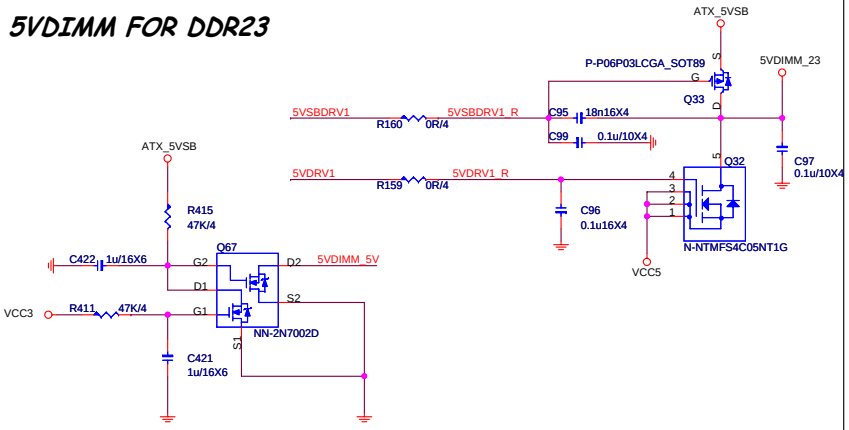

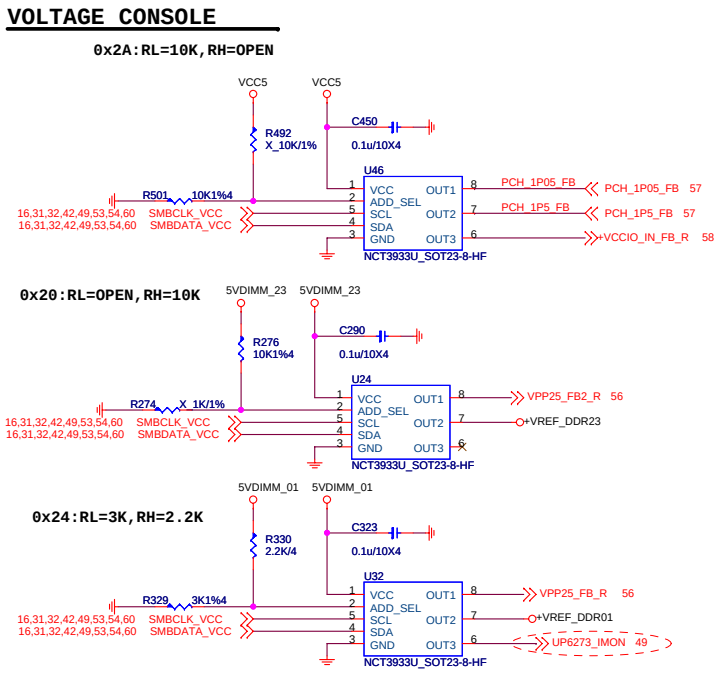

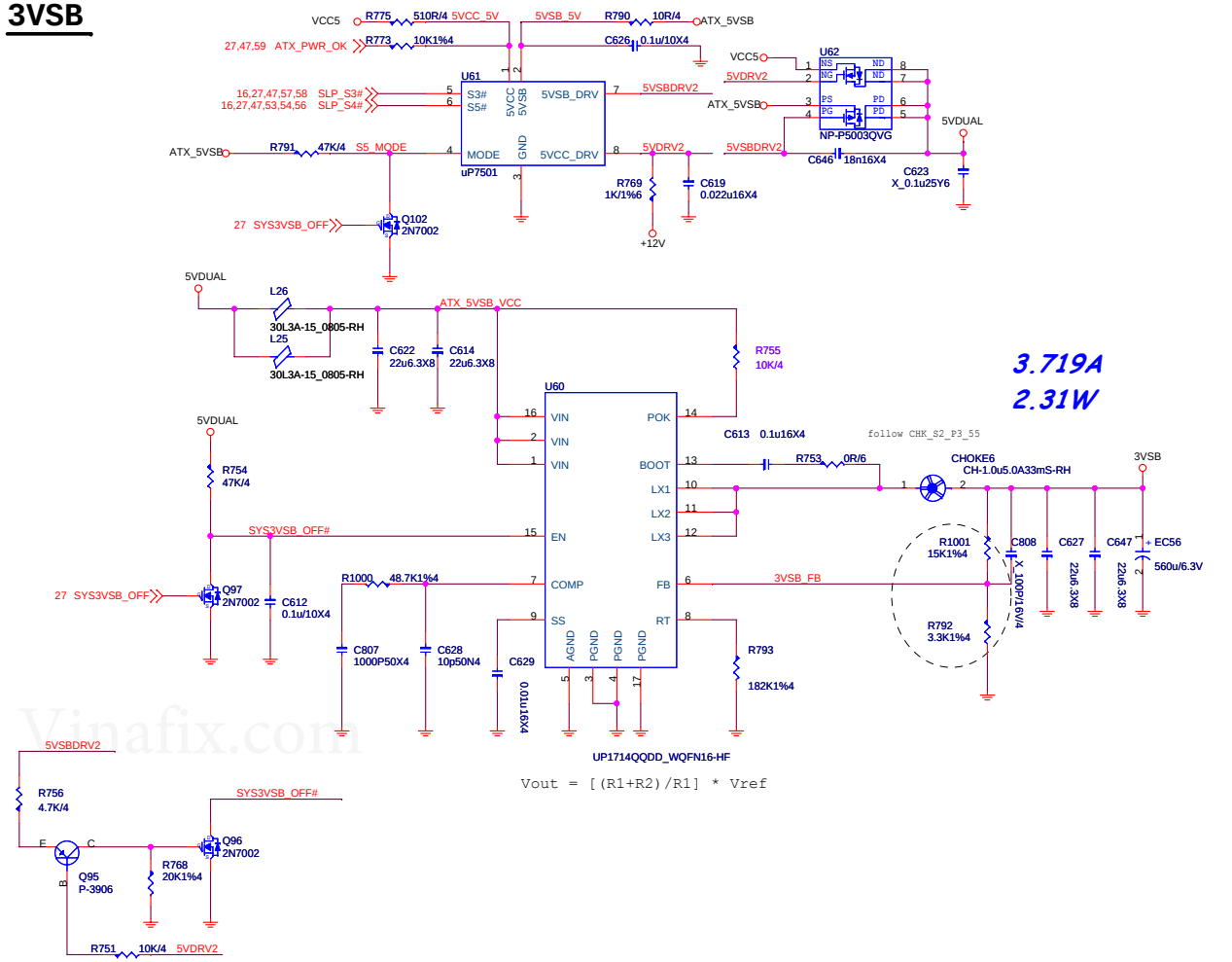

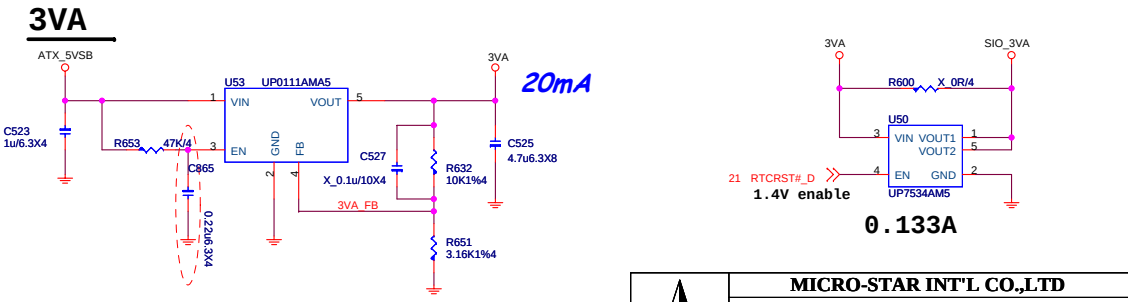

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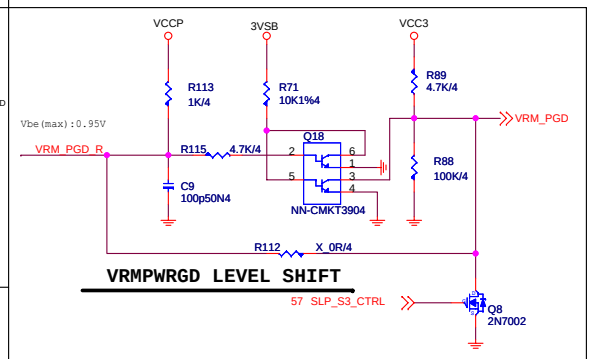
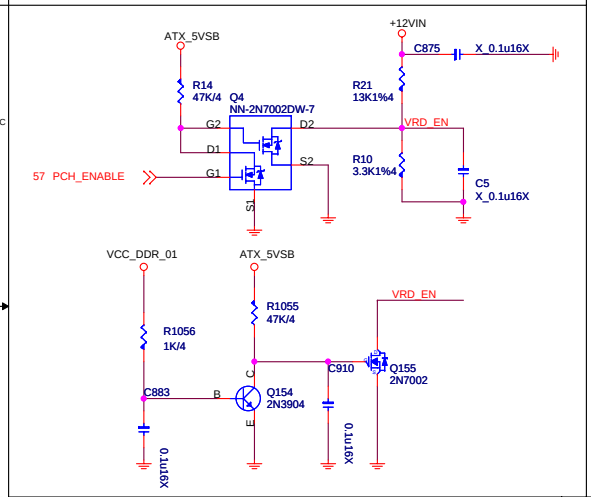
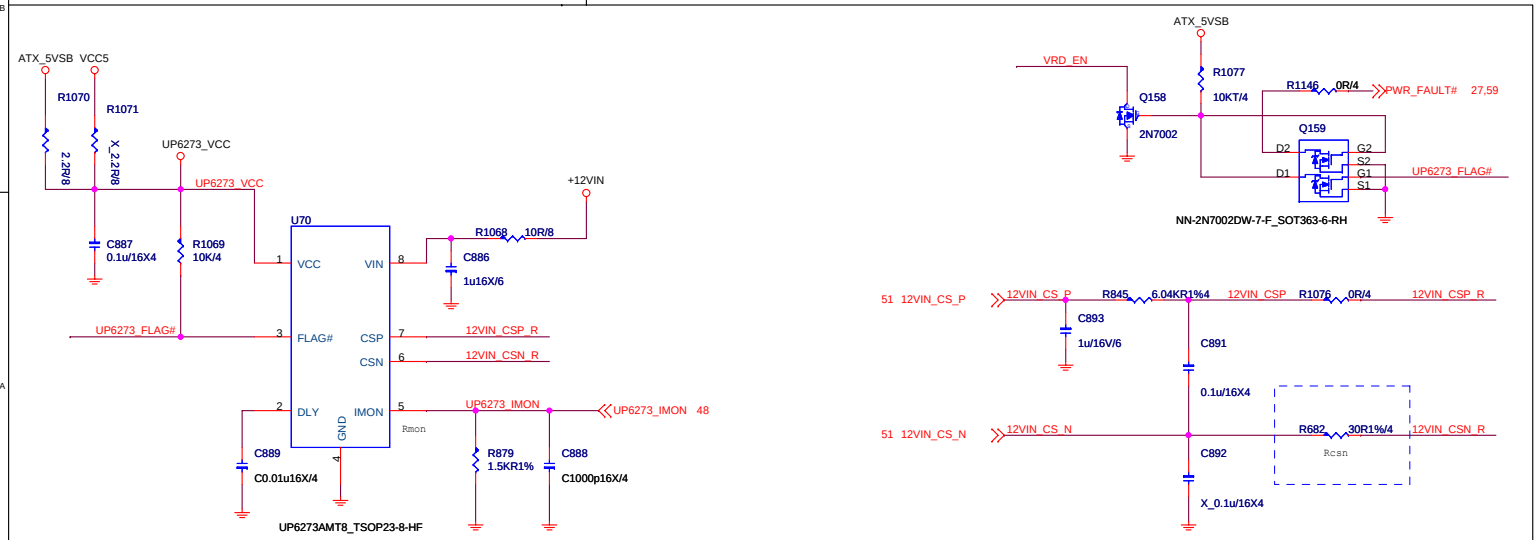
CPU Power-ISL6388 6Phase

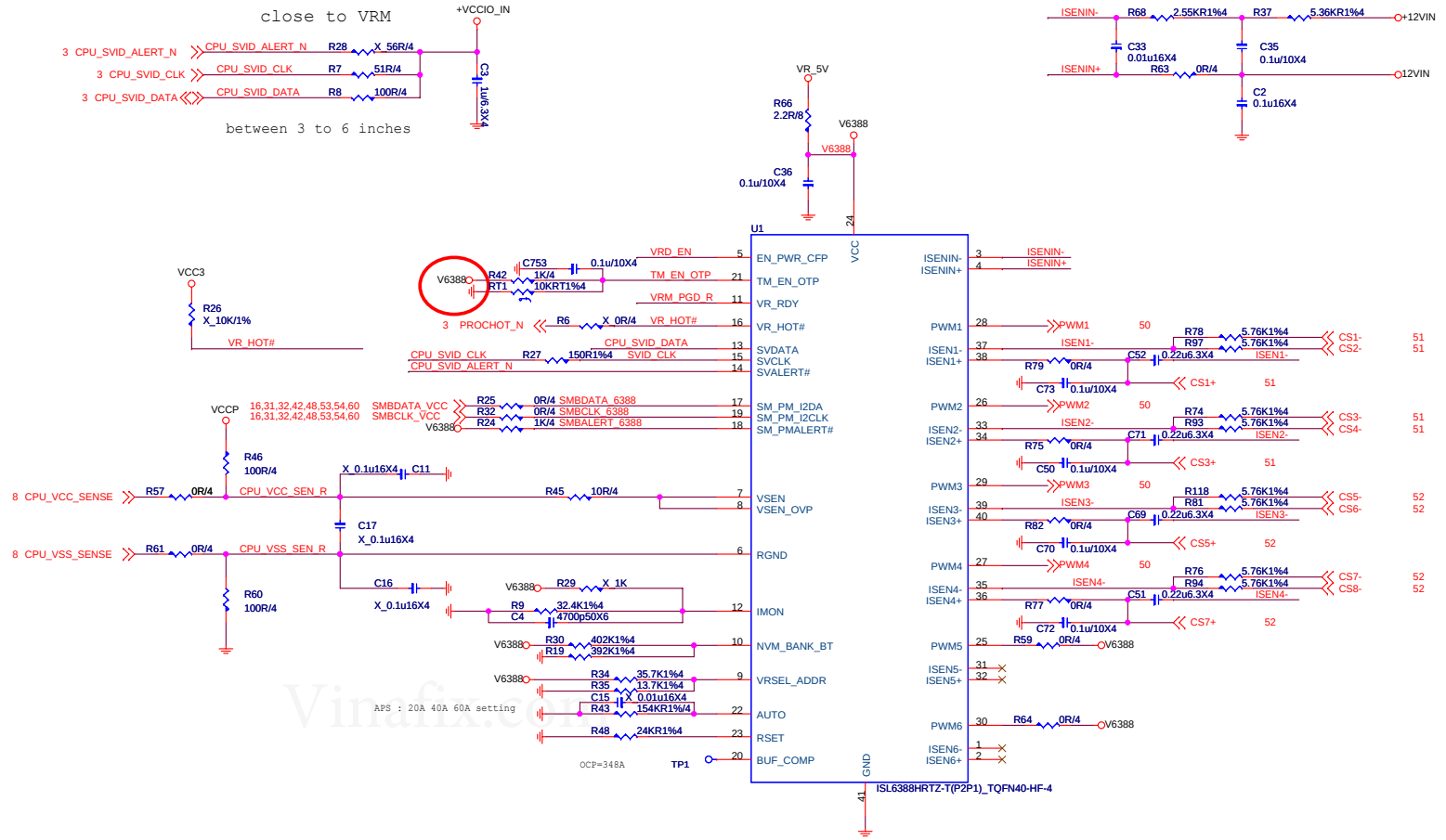
VCCP_1.8V 180A,OC margin 2.5V=240A

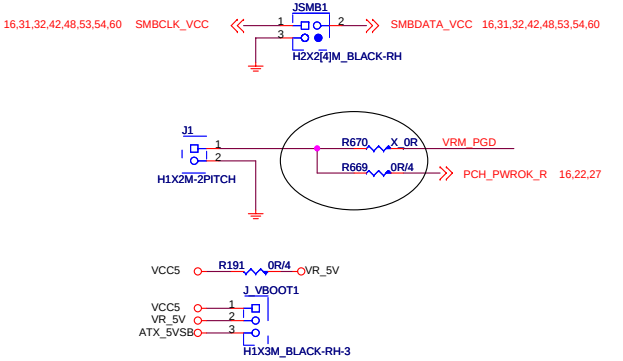
OCP:348.8A for 8Phase











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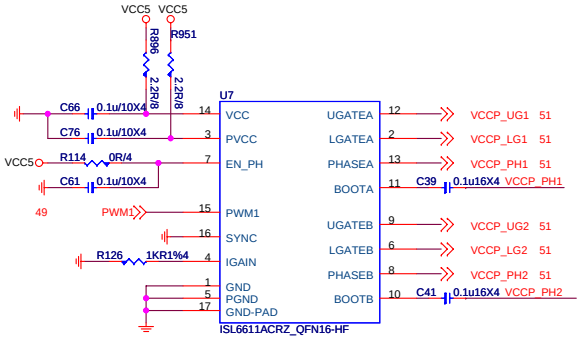

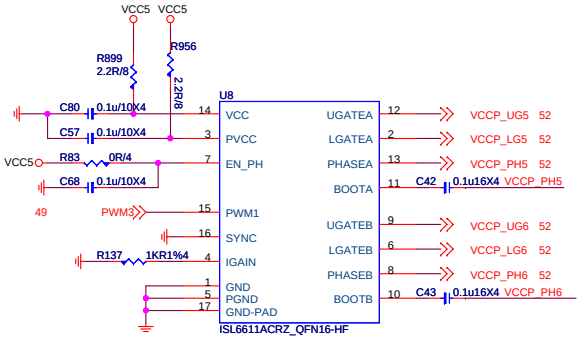

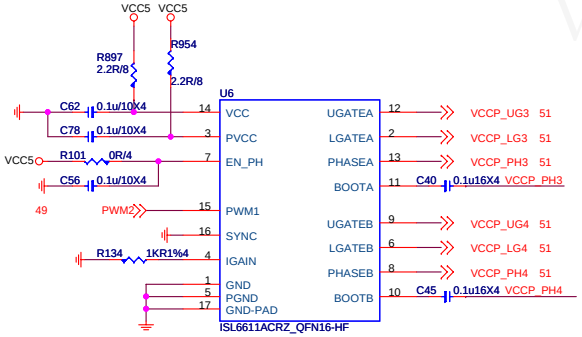

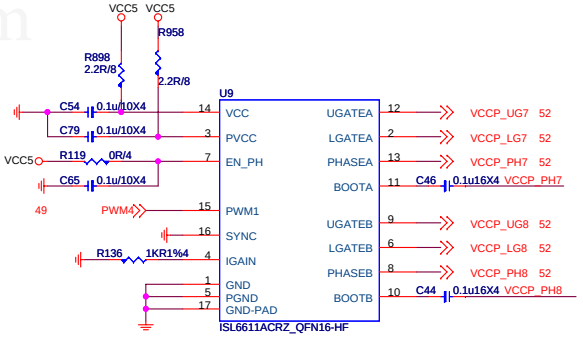

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Custom	VCORE IR3599+IR3598 PHASE1-12	10

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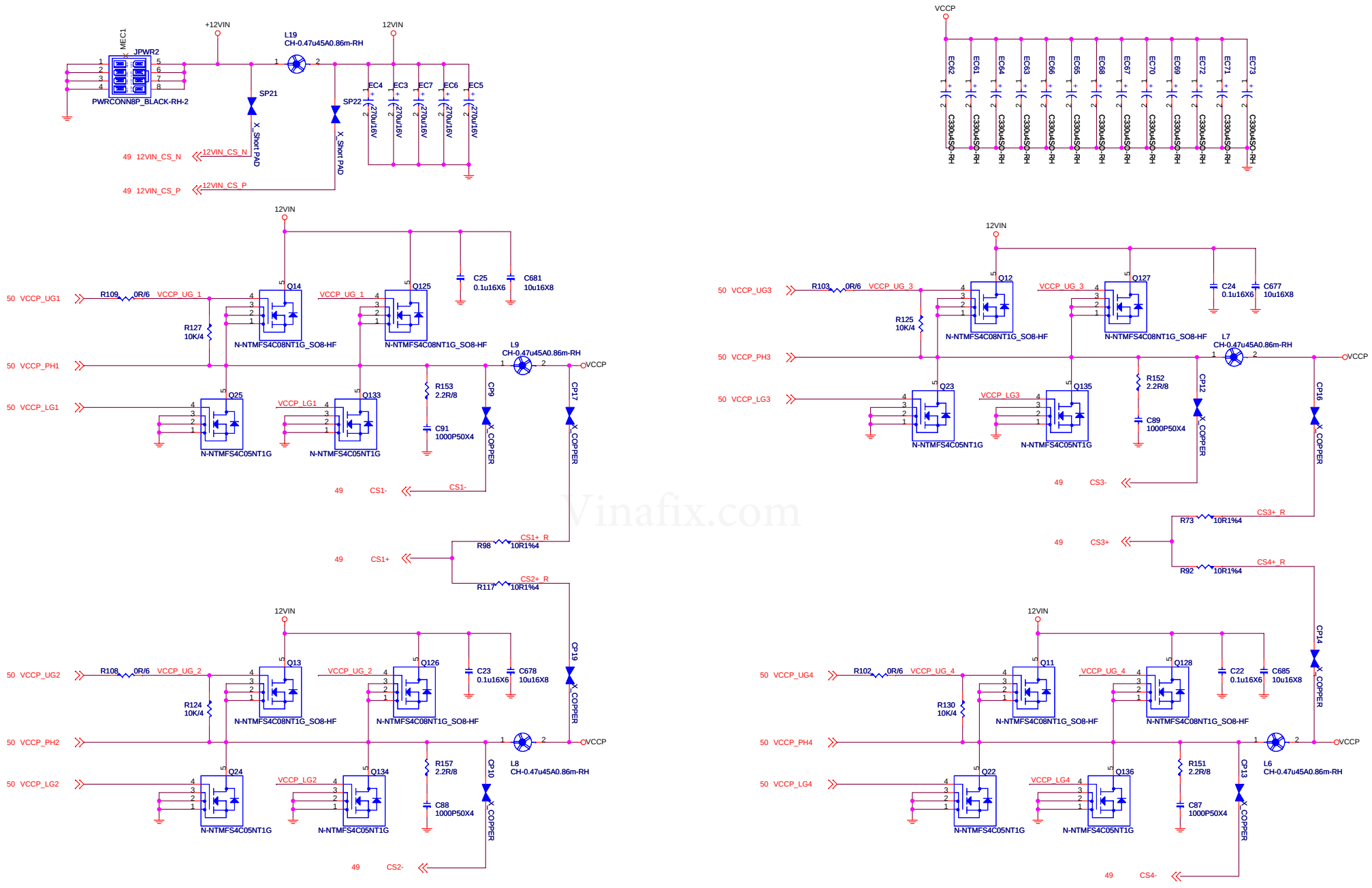

Vinafix

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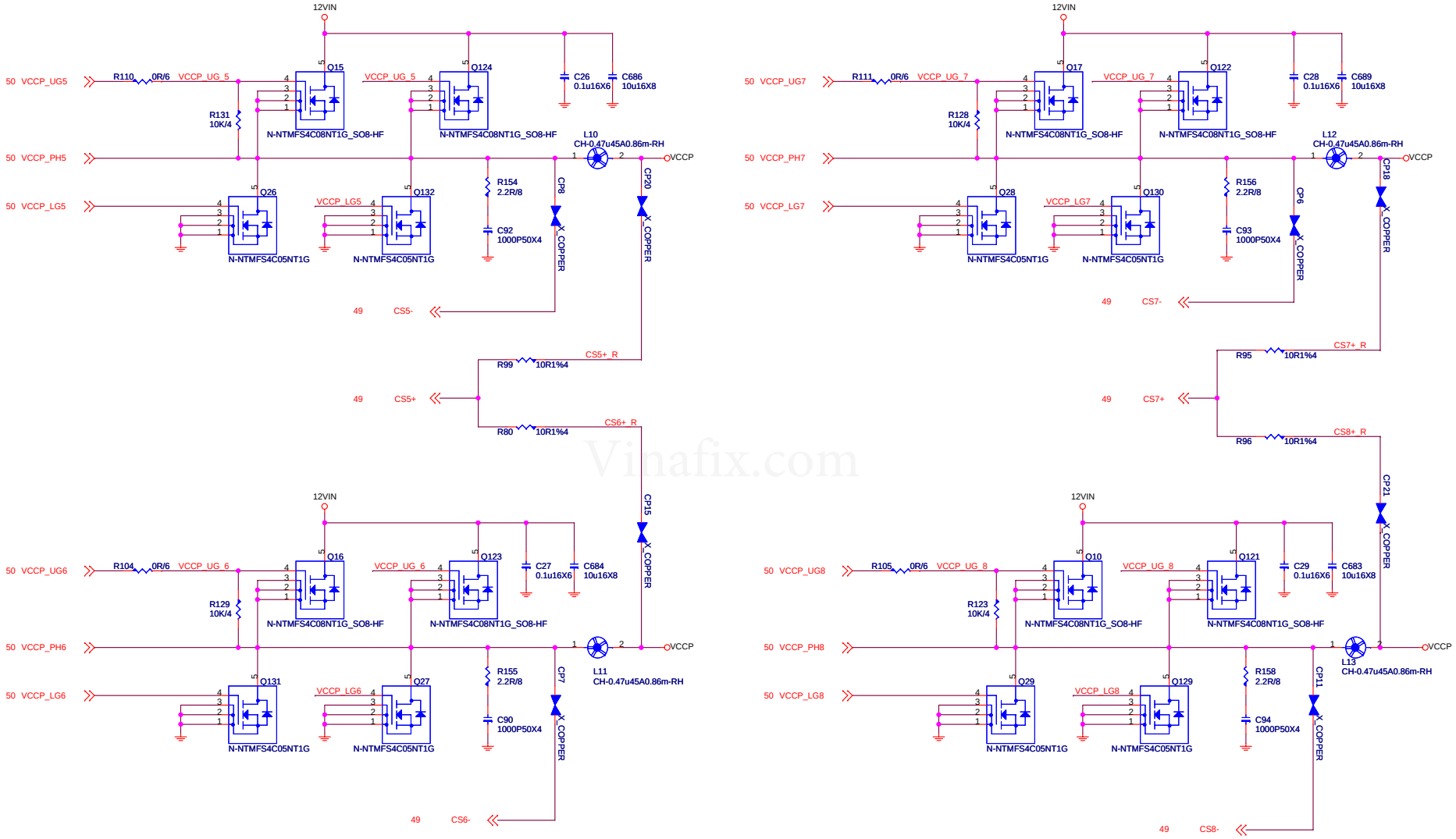

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DDR Power1-PV3203-2-Phase

DDR3_1.2V 12.2A,OC margin=44A

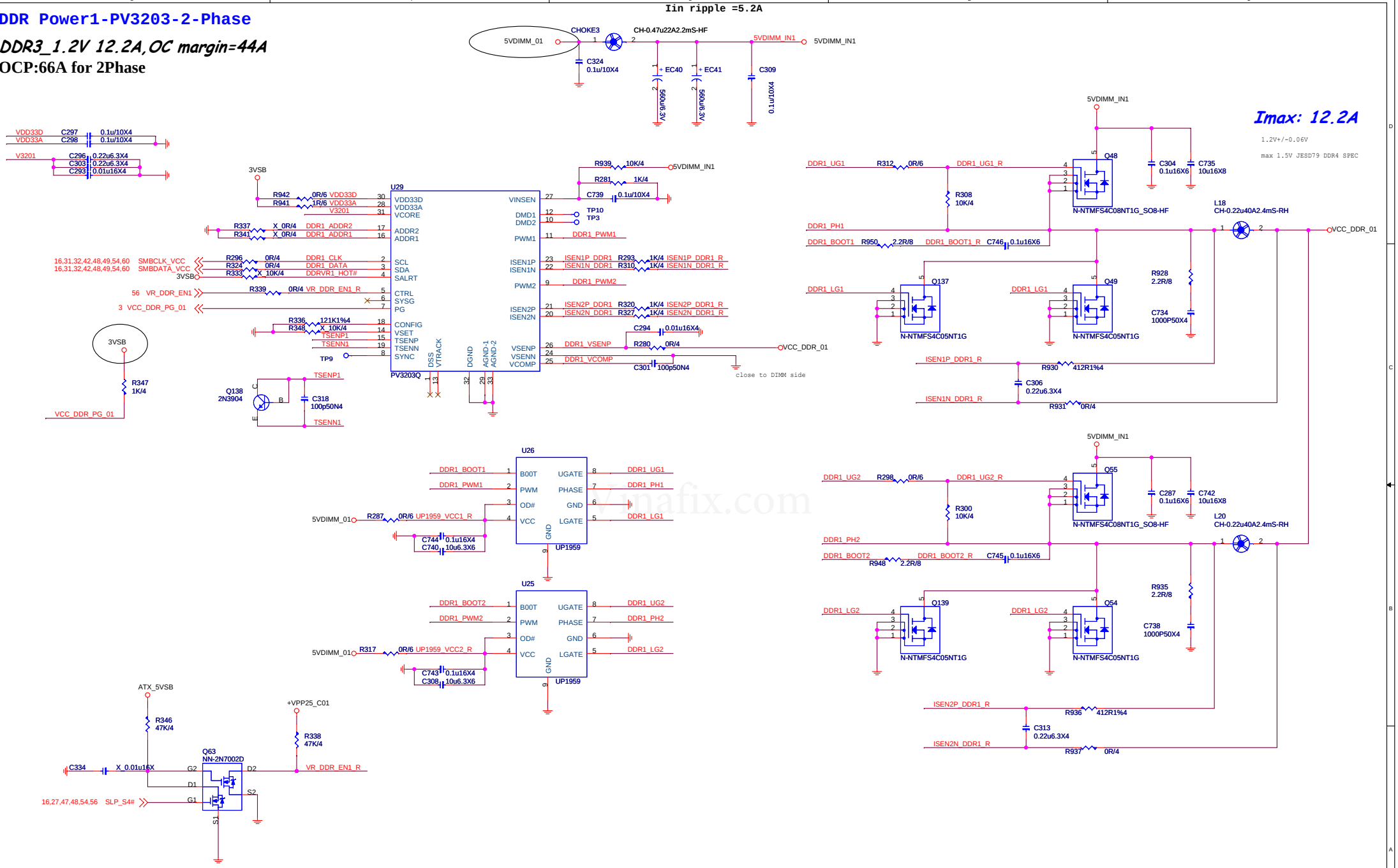
OCP:66A for 2Phase

Iin ripple =5.2A

Imax: 12.2A

1.2V+/-0.06V

max 1.5V JESD79 DDR4 SPEC



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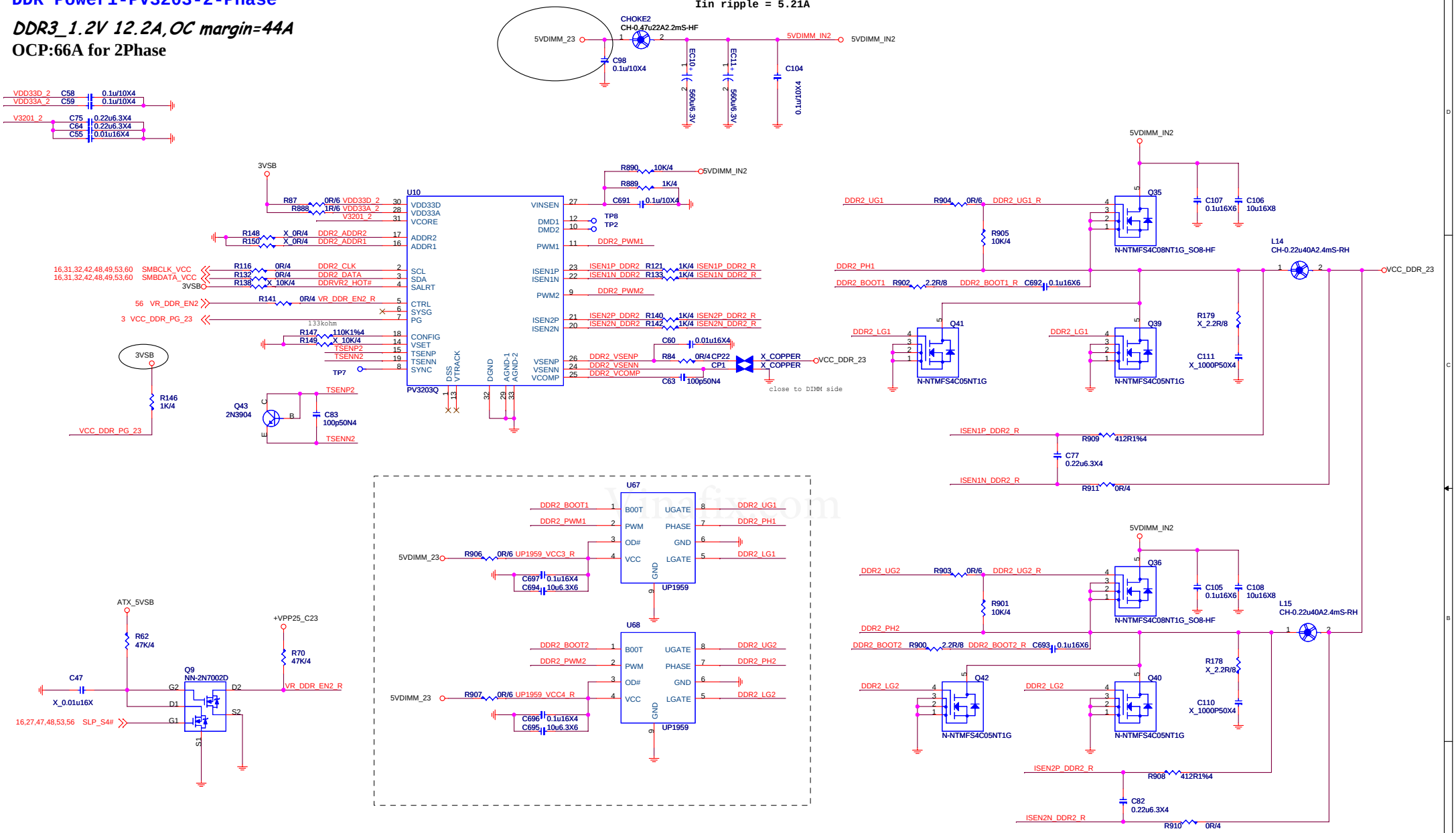
DDR Power1-PV3203-2-Phase

DDR3_1.2V 12.2A,OC margin=44A

OCP:66A for 2Phase

Iin ripple = 5.21A



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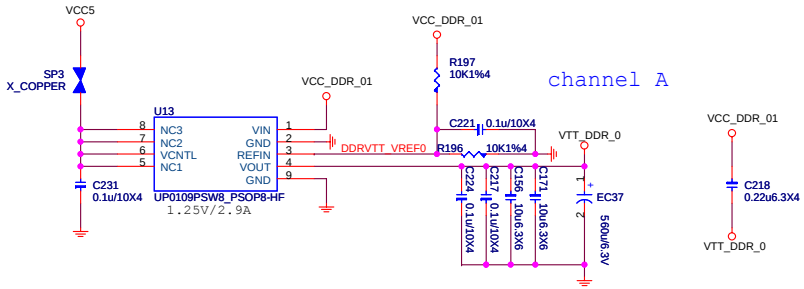
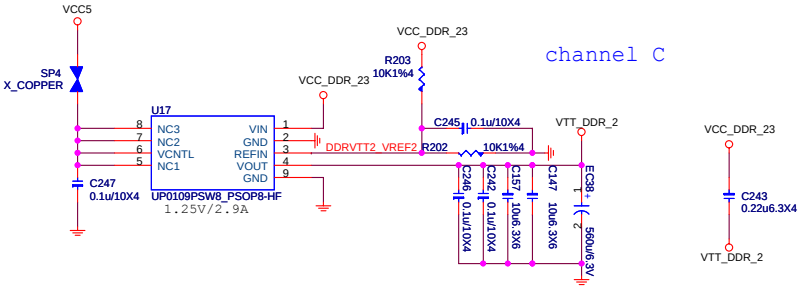
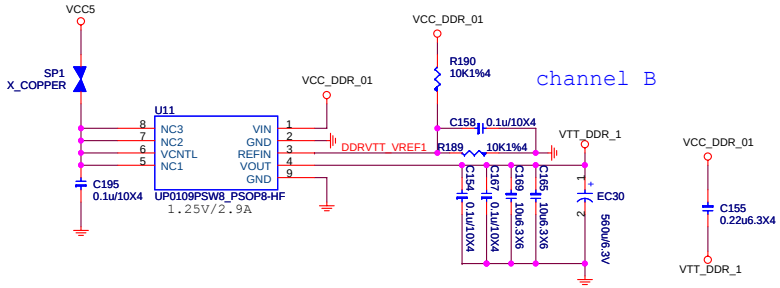
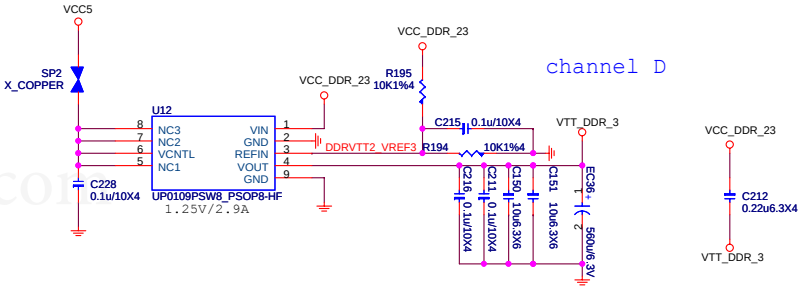
4DIMM :1.2A FOR DDR VTT

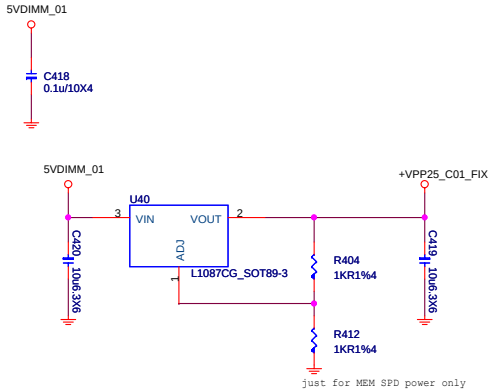
4DIMM :3A FOR OC margin

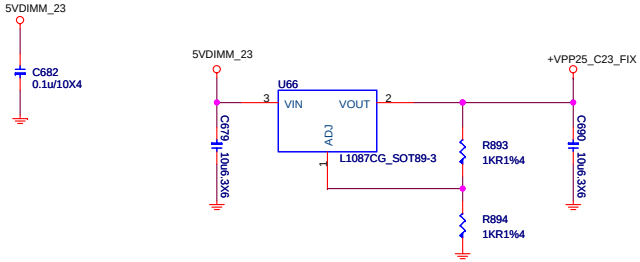












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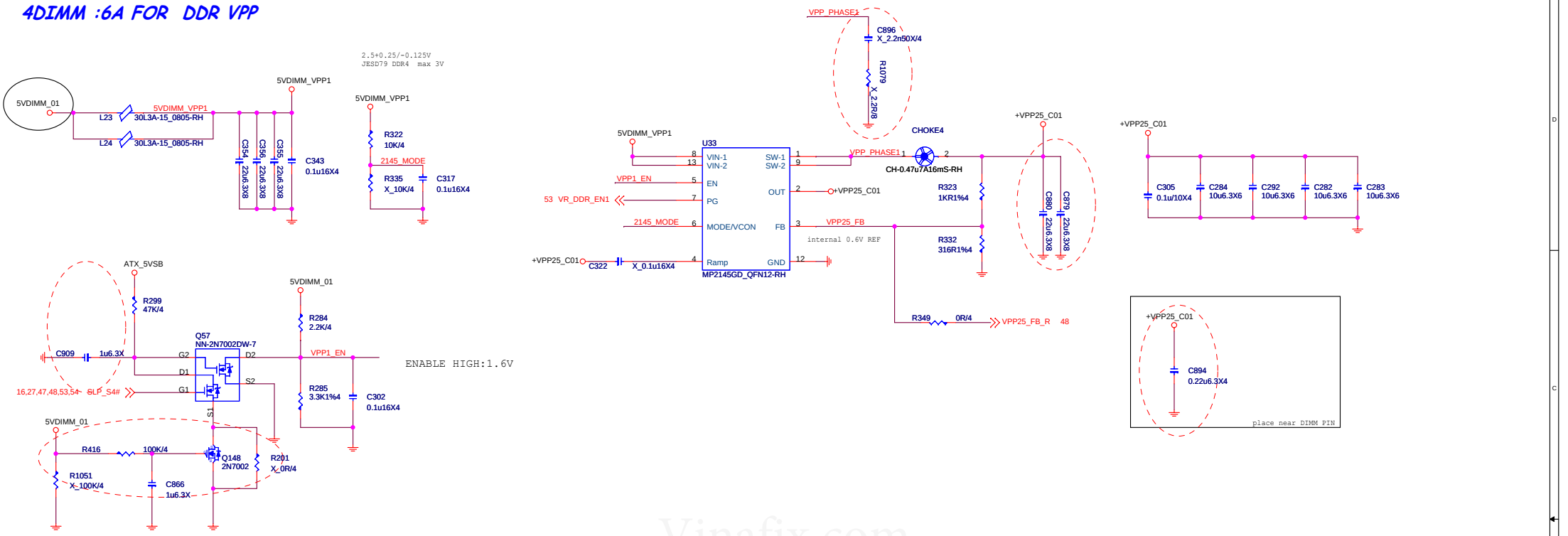
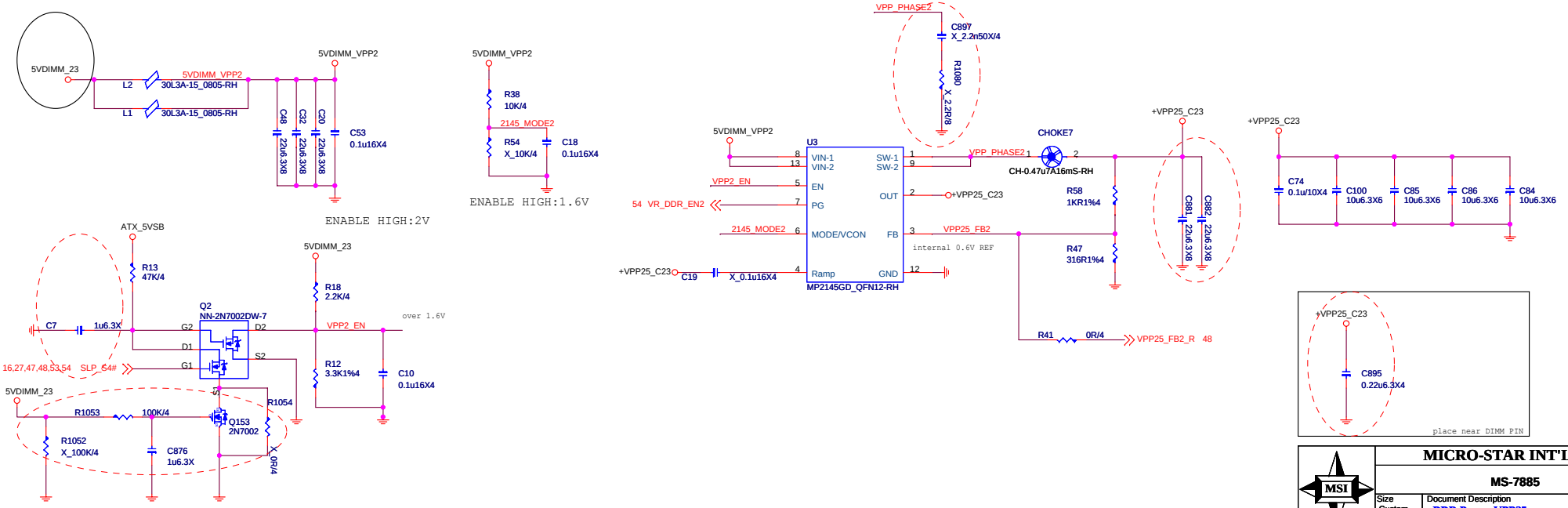
4DIMM :6A FOR DDR VPP





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PCH Power:1.05V

PCH Core 6.504A

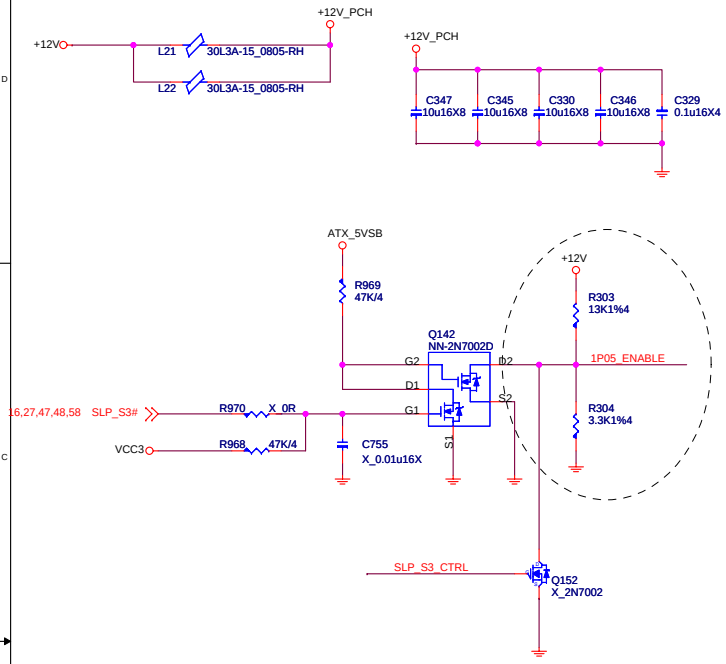
OCP calculate:

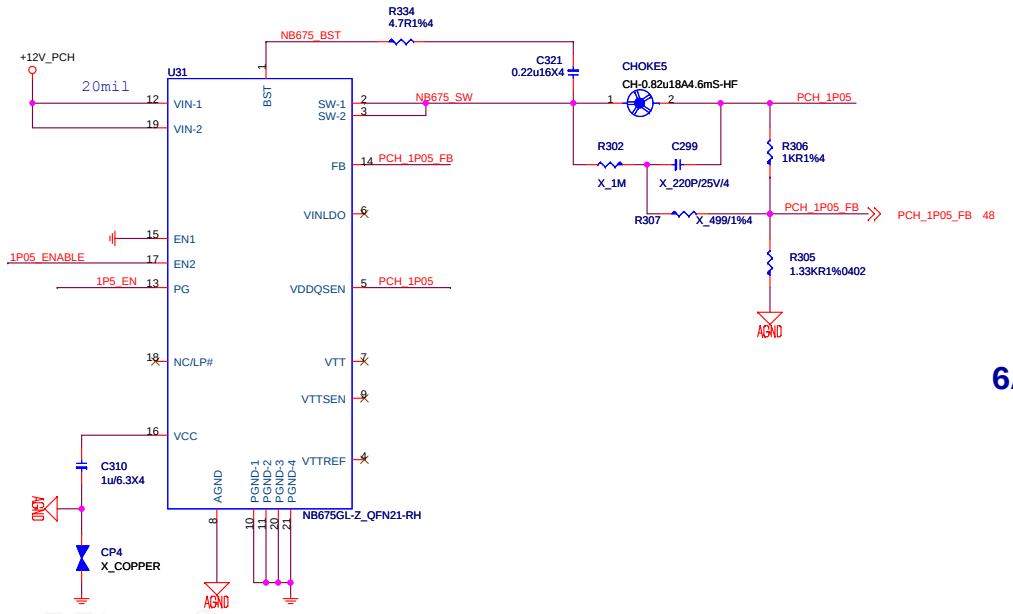
(20mA * Rocs) / 4 * Rds-on = IOCP

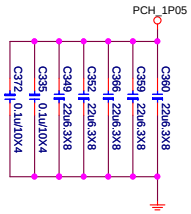
(20mA * 12.1K) / 4 * 4mohm = 15.5A

MAX 10A

ILIMIT=10A~12A 可調

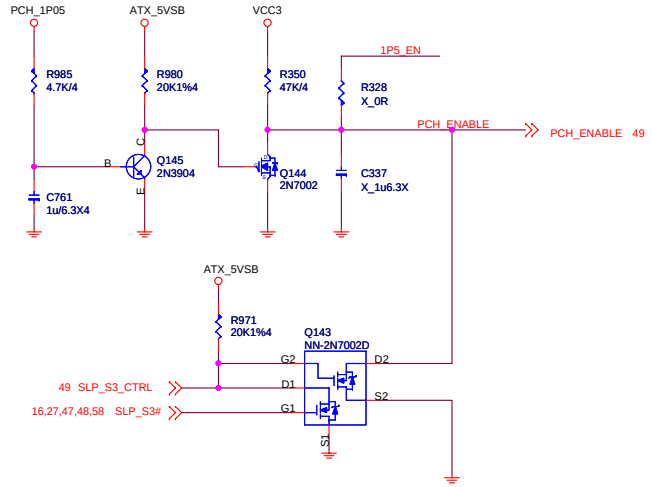


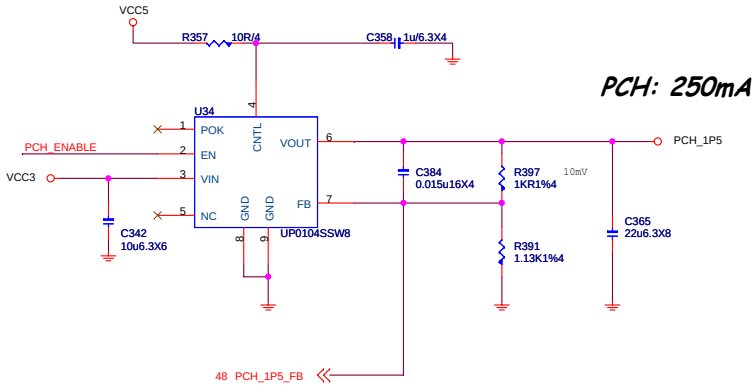




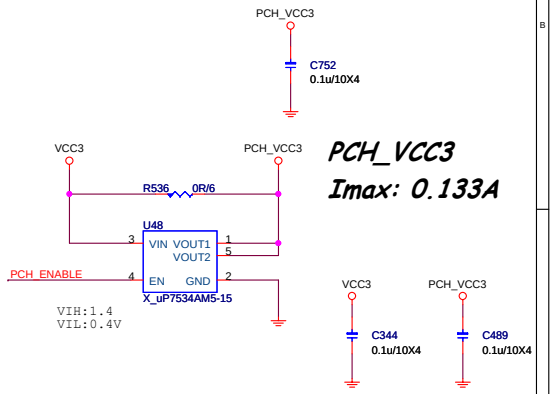
6A

Waitting PCH_1P05 Ready





PCH: 250mA



PCH_VCC3

Imax: 0.133A

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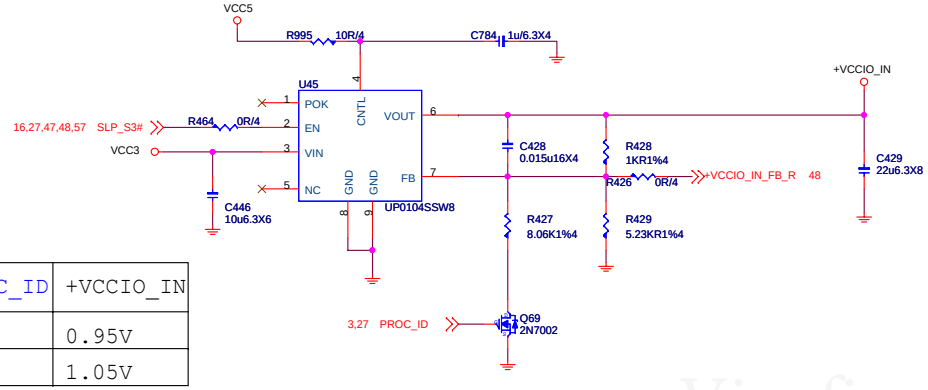
VCCIO_IN_1.05V 431mA,OC margin 1.6V=1A



PROC_ID	+VCCIO_IN
0	0.95V
1	1.05V

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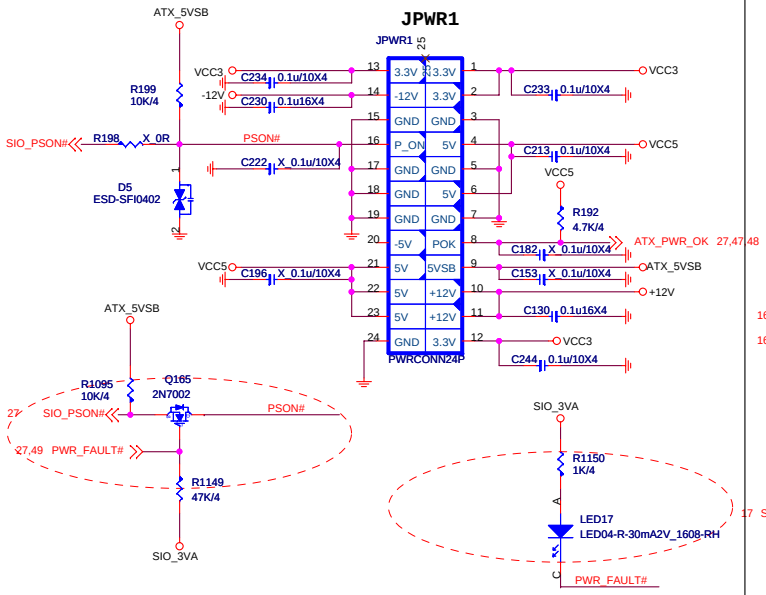
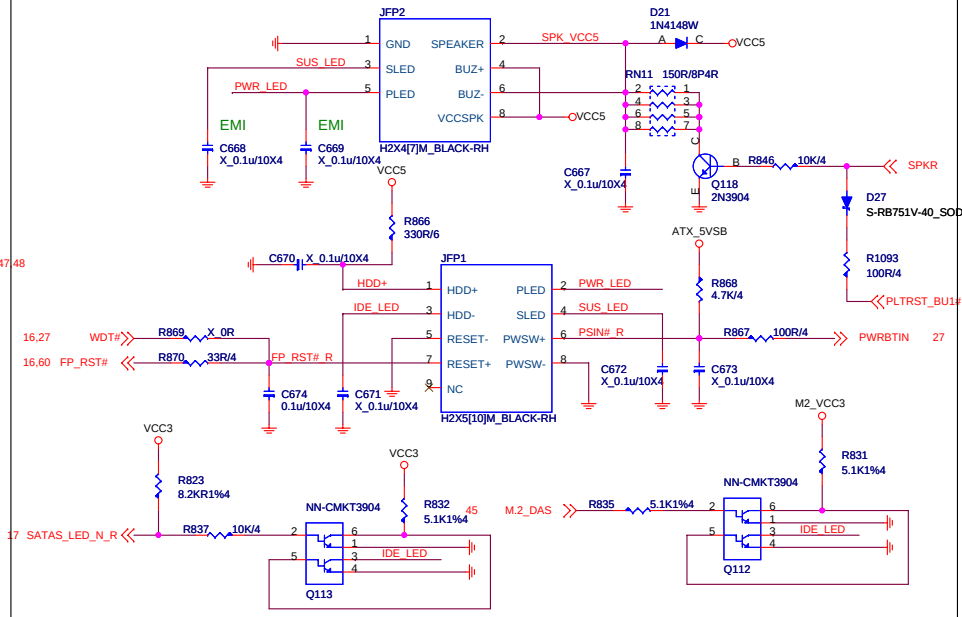
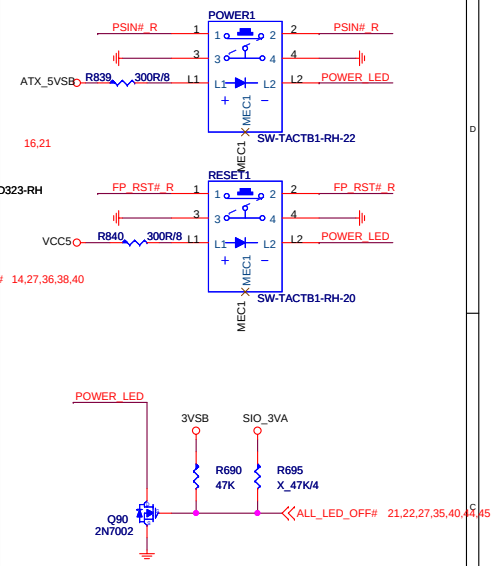
ATX POWER CONNECTOR



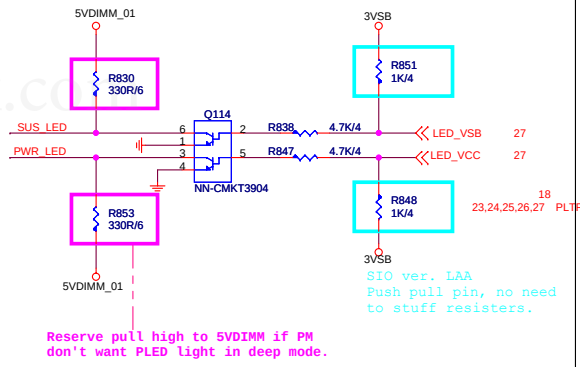
FRONT PANNEL



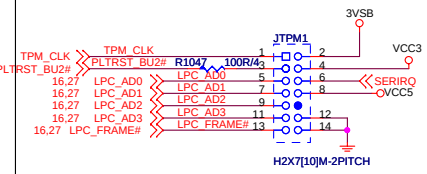
PWR/RST Botton

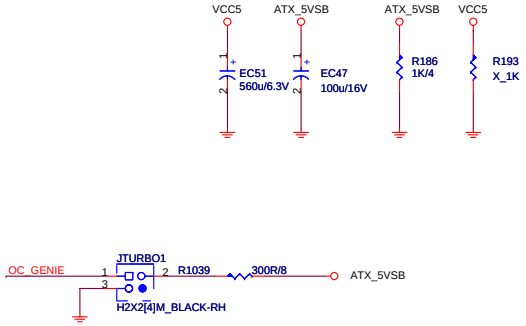


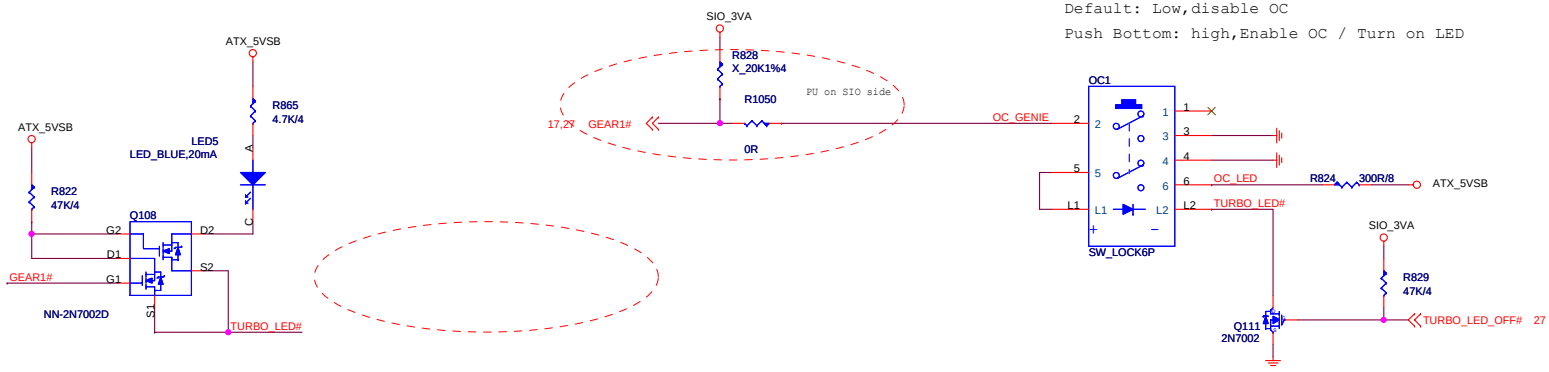
Front Panel LED



TPM







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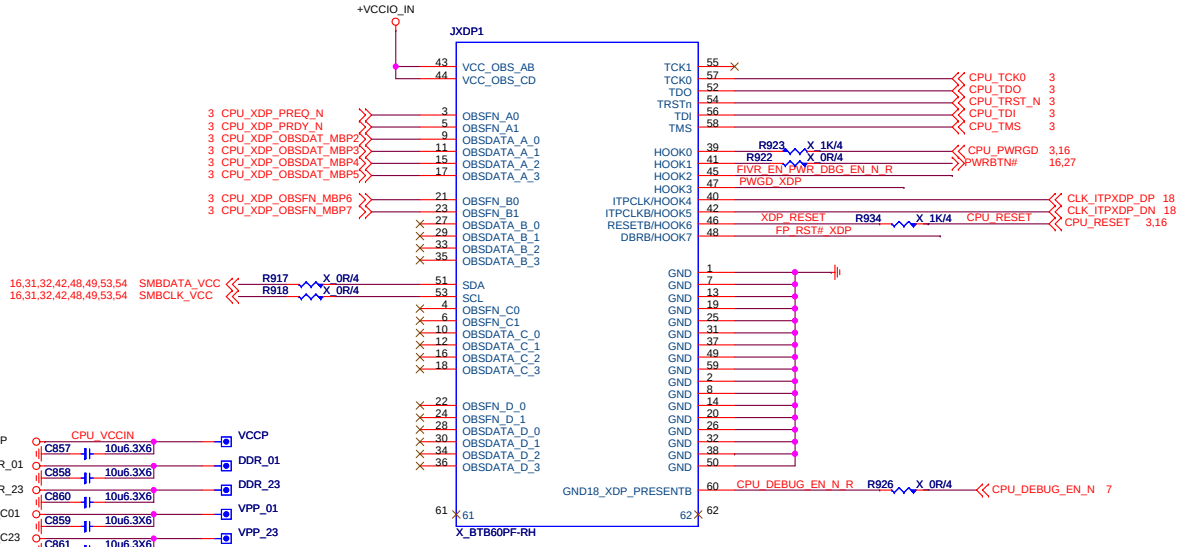
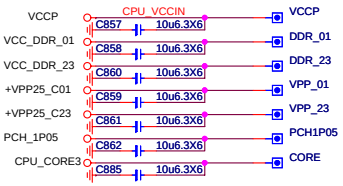
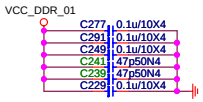
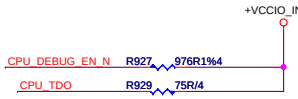
Reserve debug port 5020

Vinafix

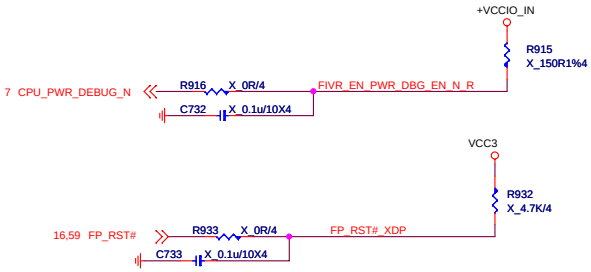


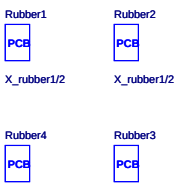


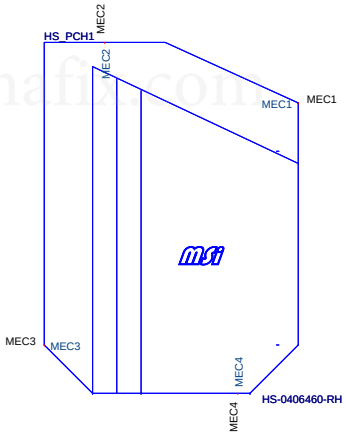


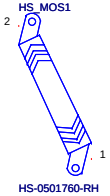


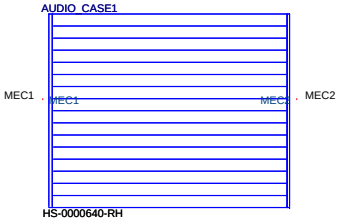
WITHIN 250MILS OF XDP CONNECTOR PIN

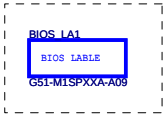


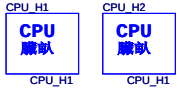


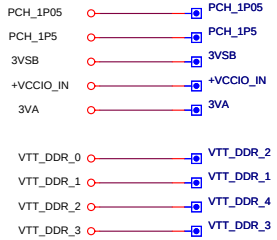


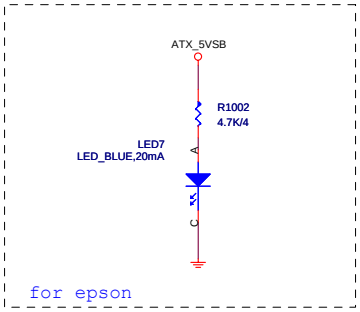


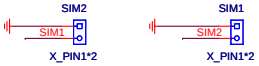




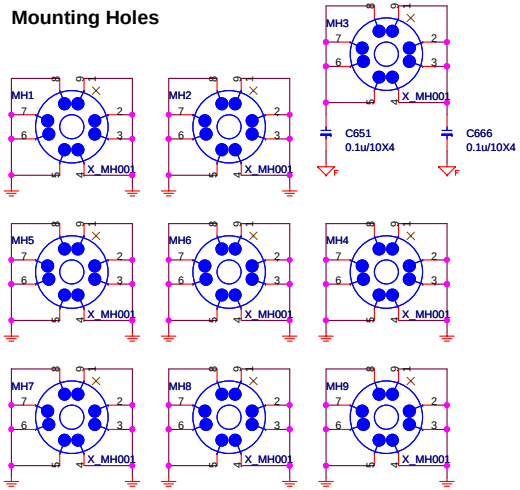




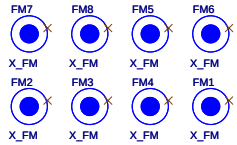




Mounting Holes



Optical Fiducial Marks-120



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