1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,WHITE_ARROW,MLB,K18

02/01/10

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8504	1	SCHEM,WHITE_ARROW,MLB,K18	SCH	CRITICAL	
820-2850	1	PCBF,WHITE_ARROW,MLB,K18	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 1 10:13:48 2010

DRAWING TITLE: SCHEM,WHITE_ARROW,MLB,K18

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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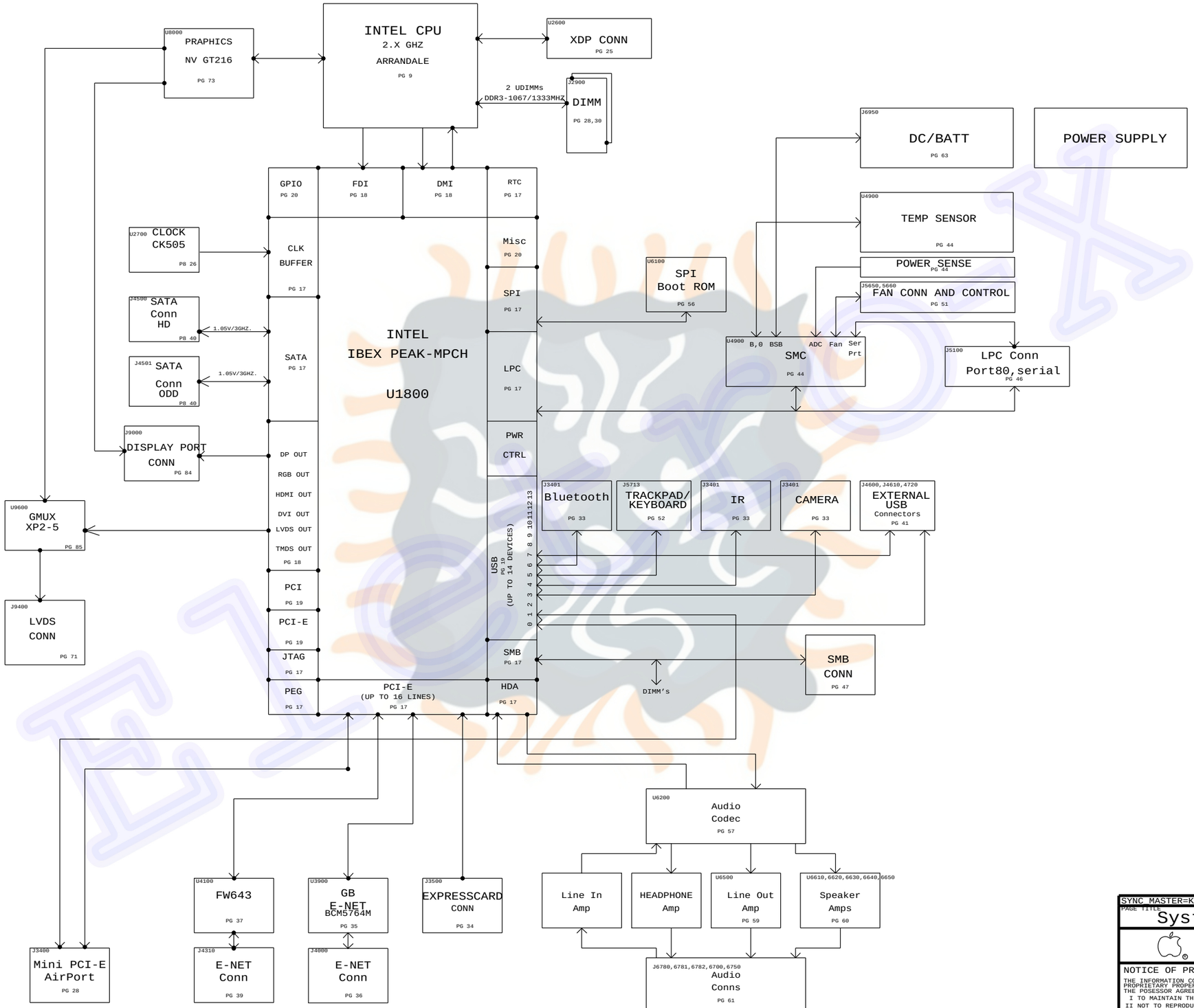

SYNC_MASTER=K17_REF SYNC_DATE=06/30/2009

PAGE TITLE
System Block Diagram

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DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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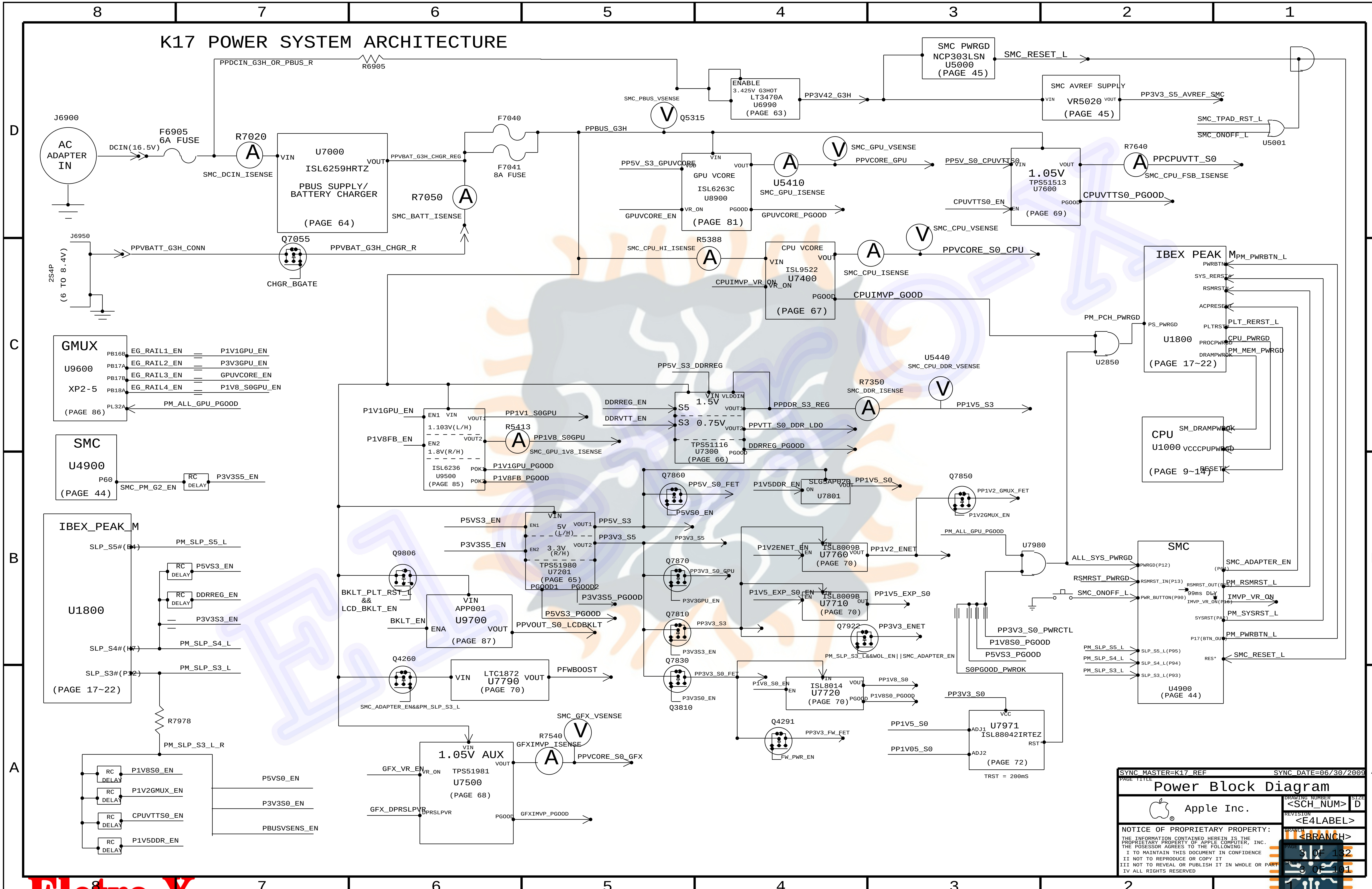
SHEET 2 OF 101


K17 POWER SYSTEM ARCHITECTURE
AC ADAPTER IN
J6900
DCIN(16.5V)
F6905 6A FUSE
R7020
SMC_DCIN_ISENSE
U7000 ISL6259HRTZ
PBUS SUPPLY/ BATTERY CHARGER
(PAGE 64)
PPDCIN_G3H_OR_PBUS_R
R6905
PPBAT_G3H_CHGR_REG
F7040
F7041 8A FUSE
R7050
SMC_BATT_ISENSE
PPBUS_G3H
SMC_PBUS_VSENSE
Q5315
ENABLE 3.425V G3HOT LT3470A U6990 (PAGE 63)
PP3V42_G3H
SMC PWRGD NCP303LSN U5000 (PAGE 45)
SMC_RESET_L
SMC AVREF SUPPLY VR5020 (PAGE 45)
PP3V3_S5_AVREF_SMC
SMC_TPAD_RST_L
SMC_ONOFF_L
U5001
J6950
PPVBATT_G3H_CONN
2S4P (6 TO 8.4V)
Q7055
PPVBAT_G3H_CHGR_R
CHGR_BGATE
PP5V_S3_GPUVCORE
GPU VCORE ISL6263C U8900 (PAGE 81)
GPUVCORE_EN
GPUVCORE_PGOOD
U5410
SMC_GPU_ISENSE
SMC_GPU_VSENSE
PPVCORE_GPU
PP5V_S0_CPUVTTS0
1.05V TPS51513 U7600 (PAGE 69)
CPUVTTS0_EN
CPUVTTS0_PGOOD
R7640
PPCPUVTT_S0
SMC_CPU_FSB_ISENSE
SMC_CPU_HI_ISENSE
R5388
CPU VCORE ISL9522 U7400 (PAGE 67)
CPUIMVP_VR_ON
CPUIMVP_PGOOD
SMC_CPU_ISENSE
SMC_CPU_VSENSE
PPVCORE_S0_CPU
IBEX PEAK M
U1800 (PAGE 17~22)
PM_PWRBTN_L
PLT_RERST_L
CPU_PWRGD
PM_MEM_PWRGD
PM_PCH_PWRGD
U2850
GMUX U9600 XP2-5 (PAGE 86)
EG_RAIL1_EN P1V1GPU_EN
EG_RAIL2_EN P3V3GPU_EN
EG_RAIL3_EN GPUVCORE_EN
EG_RAIL4_EN P1V8_S0GPU_EN
PM_ALL_GPU_PGOOD
SMC U4900 (PAGE 44)
SMC_PM_G2_EN
RC DELAY
P3V3S5_EN
PP5V_S3_DDRREG
DDRREG_EN
DDRVTT_EN
1.5V S5 S3 0.75V TPS51116 U7300 (PAGE 66)
PPDDR_S3_REG
PPVTT_S0_DDR_LDO
DDRREG_PGOOD
R7350
SMC_DDR_ISENSE
U5440
SMC_CPU_DDR_VSENSE
PP1V5_S3
P1V1GPU_EN
P1V8FB_EN
ISL6236 U9500 (PAGE 85)
PP1V1_S0GPU
R5413
PP1V8_S0GPU
SMC_GPU_1V8_ISENSE
P1V1GPU_PGOOD
P1V8FB_PGOOD
CPU U1000 (PAGE 9~14)
IBEX_PEAK_M U1800 (PAGE 17~22)
PM_SLP_S5_L
P5VS3_EN
DDRREG_EN
P3V3S3_EN
PM_SLP_S4_L
PM_SLP_S3_L
R7978
PM_SLP_S3_L_R
P1V8S0_EN
P1V2GMUX_EN
CPUVTTS0_EN
P1V5DDR_EN
P5VS0_EN
P3V3S0_EN
PBUSVSENS_EN
P5VS3_EN
P3V3S5_EN
5V 3.3V TPS51980 U7201 (PAGE 65)
PP5V_S3
PP3V3_S5
P3V3S5_PGOOD
P5VS3_PGOOD
Q9806
BKLT_PLT_RST_L && LCD_BKLT_EN
APP001 U9700 (PAGE 87)
BKLT_EN
PPVOUT_S0_LCDBKLT
Q4260
LTC1872 U7790 (PAGE 70)
PFWBOOST
SMC_ADAPTER_EN&&PM_SLP_S3_L
1.05V AUX TPS51981 U7500 (PAGE 68)
GFX_VR_EN
GFX_DPRSLPVR
R7540
GFXIMVP_ISENSE
SMC_GFX_VSENSE
PPVCORE_S0_GFX
GFXIMVP_PGOOD
Q7860
PP5V_S0_FET
P5VS0_EN
P1V5DDR_EN
SLG5AP020 U7801
PP1V5_S0
Q7850
PP1V2_GMUX_FET
P1V2GMUX_EN
P1V2ENET_EN
ISL8009B U7760 (PAGE 70)
PP1V2_ENET
P1V5_EXP_S0_EN
ISL8009B U7710 (PAGE 70)
PP1V5_EXP_S0
Q7870
PP3V3_S0_GPU
P3V3GPU_EN
Q7810
PP3V3_S3
P3V3S3_EN
Q7922
PP3V3_ENET
PM_SLP_S3_L&&WOL_EN||SMC_ADAPTER_EN
Q7830
PP3V3_S0_FET
P3V3S0_EN
Q3810
P1V8_S0_EN
ISL8014 U7720 (PAGE 70)
PP1V8_S0
P1V8S0_PGOOD
Q4291
PP3V3_FW_FET
FW_PWR_EN
PM_ALL_GPU_PGOOD
U7980
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
PP3V3_S0_PWRCTL
P1V8S0_PGOOD
P5VS3_PGOOD
S0PGOOD_PWROK
PP3V3_S0
PP1V5_S0
PP1V05_S0
U7971 ISL88042IRTEZ (PAGE 72)
TRST = 200mS
SMC U4900 (PAGE 44)
SMC_ADAPTER_EN
PM_RSMRST_L
IMVP_VR_ON
PM_SYSRST_L
PM_PWRBTN_L
SMC_RESET_L
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
SYNC_MASTER=K17_REF
SYNC_DATE=06/30/2009
Power Block Diagram
Apple Inc.
<SCH_NUM>
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<E4LABEL>
<BRANCH>
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0952	PCBA,2.0G,512SAM_VRAM,K18	K18_COMMON,CPU_2_4GHZ,FB_256_SAMSUNG,K18_PVT,EEEE_DCJ7
639-0953	PCBA,2.0G,512HYN_VRAM,K18	K18_COMMON,CPU_2_4GHZ,FB_256_HYNIX,K18_PVT,EEEE_DCJ8
639-0954	PCBA,2.13G,512SAM_VRAM,K18	K18_COMMON,CPU_2_53GHZ,FB_512_SAMSUNG,K18_PVT,EEEE_DCJ9
639-0955	PCBA,2.13G,512HYN_VRAM,K18	K18_COMMON,CPU_2_53GHZ,FB_512_HYNIX,K18_PVT,EEEE_DCJC
639-0956	PCBA,2.4G,512SAM_VRAM,K18	K18_COMMON,CPU_2_66GHZ,FB_512_SAMSUNG,K18_PVT,EEEE_DCJD
639-0957	PCBA,2.4G,512HYN_VRAM,K18	K18_COMMON,CPU_2_66GHZ,FB_512_HYNIX,K18_PVT,EEEE_DCJF
085-1404	K18 DEVELOPMENT BOM	

K18 BOM GROUPS

BOM GROUP	BOM OPTIONS
K18_COMMON	ALTERNATE,COMMON,K18_COMMON1,K18_COMMON2,K18_PROGPARTS,USBHUB_2061,RDRV:8515A2,DCI
K18_COMMON1	BATT_3S,BCM5764M,GL137,CPUPOC_IMAX_40_50,CPUMEM_S0,SMC_EXCARD_NOT,SMC_DEBUG_YES,HUB1_2NONREM,HUB2_3NONREM
K18_COMMON2	GMUXPLL_3V3,GPU_SS_INT,MIKEY,GPUVID_0P90V,DPMUX_EN_PLD,DP_CA_DET_EG_PLD,DP_ESD,VFRQ_SLPS3,SMC_OSC_YES,RAIL_MON
K18_PVT	BMON_PROD,VREFMRGN_NOT,XDP,XDP_NORMAL,XDP_CPU_BPM
K18_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4,VRAM_256_SAMSUNG,FB1V55
FB_256_HYNIX	VRAM4,VRAM_256_HYNIX,FB1V55
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG,FB1V35
FB_512_HYNIX	VRAM4,VRAM_512_HYNIX,FB1V35

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
333S0506	333S0535		ALL	Hynix 900M alt to 1000M
516S0805	516S0806		ALL	Molex alt to Foxconn
152S1102	152S1088		ALL	Mag layer alt to Vishay
353S2805	353S2603		ALL	Fairchild wafer option
333S0542	333S0507		ALL	Samsung I die alt to H
128S0264	128S0257		ALL	Sanyo alt to Kemet
128S0303	128S0282		ALL	Panasonic alt to Sanyo
337S3808	337S3839		ALL	A02 alt to A03 GPU
128S0305	128S0294		ALL	6.3V alt to 11V Sanyo

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJ7]	CRITICAL	EEEE_DCJ7
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJ8]	CRITICAL	EEEE_DCJ8
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJ9]	CRITICAL	EEEE_DCJ9
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJC]	CRITICAL	EEEE_DCJC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJD]	CRITICAL	EEEE_DCJD
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJF]	CRITICAL	EEEE_DCJF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3848	1	ARD,SLBPE,PRQ,2.66G,35W,C2,3M,BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3847	1	ARD,SLBPF,PRQ,2.53G,35W,C2,3M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3846	1	ARD,SLBNA,PRQ,2.4G,35W,C2,4M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3849	1	IC,PCH,IBEX PEAK-M,SLGZS,PRQ,B3,BGA	U1800	CRITICAL	
337S3839	1	IC,GPU,NV GT216 LP++,969BGA,40NM,A03	U8000	CRITICAL	
343S0493	1	IC,ASIC,BCM5764M,ENET CONTROLLER,8x8,64 QFN	U3900	CRITICAL	BCM5764M
341S2731	1	IC,1MBIT,SPI FLASH,K17/K18	U3990	CRITICAL	
338S0753	1	IC,FW643-E2,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341T0233	1	IC,SMC,K18	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2562	1	IC,EFI ROM,DEVELOPMENT,K18	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
341S2616	1	IC,PSOC +W/USB,56PIN,MLF,K18	U5701	CRITICAL	TPAD_PROG
336S0025	1	IC,XP2-5,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_5K_BLANK
341S2566	1	IC,CPLD,LATTICE,132CSBGA,K18	U9600	CRITICAL	GMUX_PROG
333S0507	4	IC,SGRAM,GDDR3,16MX32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0483	4	IC,SDRAM,GDDR3,16MX32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX
333S0533	4	IC,SGRAM,GDDR3,32MX32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0535	4	IC,SDRAM,GDDR3,32MX32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_HYNIX

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1404	1	K18 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

SYNC_MASTER=K17_REF SYNC_DATE=05/28/2009

PAGE TITLE
BOM Configuration

Apple Inc.

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Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST

TRUE	PP5V_S0	70 72 86 88 8, 7, 29 42 47 52 54 68 69	3 TPs per Fan
TRUE	FAN_LT_PWM	52	
TRUE	FAN_LT_TACH	52	

J5660 (RIGHT FAN CONN)

TRUE	FAN_RT_PWM	52	
TRUE	FAN_RT_TACH	52	
TRUE	GND		5 TPs per Fan

J6780 (MIC CONN)

TRUE	BI_MIC_N	62 63	
TRUE	BI_MIC_SHIELD	62 63	
TRUE	BI_MIC_P	62 63	

J6781 & J6782 (SPEAKERS CONN)

TRUE	SPKRCONN_L_OUT_P	61 62 99
TRUE	SPKRCONN_L_OUT_N	61 62 99
TRUE	SPKRCONN_R_OUT_P	61 62 99
TRUE	SPKRCONN_R_OUT_N	61 62 99
TRUE	SPKRCONN_S_OUT_P	61 62 99
TRUE	SPKRCONN_S_OUT_N	61 62 99

J9000 (LVDS CONN)

TRUE	PP3V3_SW_LCD	84 85 87 88 98	
TRUE	PP3V3_S0	60 61 71 74 75 76 79 82 83 84 98	
TRUE	PPVOUT_S0_LCDBKLT	62 63 68 69 72 77 78 80 81 23 24 25 26 73 80 83	2 TP needed
TRUE	LVDS_DDC_CLK	83 84	
TRUE	LVDS_DDC_DATA	83 84	
TRUE	LVDS_CONN_A_DATA_P<0>	83 84 98	
TRUE	LVDS_CONN_A_DATA_N<0>	83 84 98	
TRUE	LVDS_CONN_A_DATA_P<1>	83 84 98	
TRUE	LVDS_CONN_A_DATA_N<1>	83 84 98	
TRUE	LVDS_CONN_A_DATA_P<2>	83 84 98	
TRUE	LVDS_CONN_A_DATA_N<2>	83 84 98	
TRUE	LVDS_CONN_A_CLK_F_P	83 98	
TRUE	LVDS_CONN_A_CLK_F_N	83 98	
TRUE	LVDS_CONN_B_DATA_P<0>	83 84 98	
TRUE	LVDS_CONN_B_DATA_N<0>	83 84 98	
TRUE	LVDS_CONN_B_DATA_P<1>	83 84 98	
TRUE	LVDS_CONN_B_DATA_N<1>	83 84 98	
TRUE	LVDS_CONN_B_DATA_P<2>	83 84 98	
TRUE	LVDS_CONN_B_DATA_N<2>	83 84 98	
TRUE	LVDS_CONN_B_CLK_F_P	83 98	
TRUE	LVDS_CONN_B_CLK_F_N	83 98	
TRUE	LED_RETURN_1	83 88	
TRUE	LED_RETURN_2	83 88	
TRUE	LED_RETURN_3	83 88	
TRUE	LED_RETURN_4	83 88	
TRUE	LED_RETURN_5	83 88	
TRUE	LED_RETURN_6	83 88	
TRUE	GND		4 TPs

J4500 (SATA ODD CONN)

TRUE	PP5V_SW_ODD	42 56	3 TPs
TRUE	SMC_ODD_DETECT	42 45	
TRUE	SATA_ODD_D2R_C_P	42 93	
TRUE	SATA_ODD_D2R_C_N	42 93	
TRUE	SATA_ODD_R2D_P	42 93	
TRUE	SATA_ODD_R2D_N	42 93	
TRUE	GND		5 TPs

J4501 (SATA HDD CONN)

TRUE	PP5V_S0_HDD_FLT	42
TRUE	SATA_HDD_R2D_P	42 93
TRUE	SATA_HDD_R2D_N	42 93
TRUE	SATA_HDD_D2R_C_N	42 93
TRUE	SATA_HDD_D2R_C_P	42 93
TRUE	GND	

J5815 (KBD BACKLIGHT CONN)

TRUE	KBDLED_ANODE	54	
TRUE	SMC_KDBLED_PRESENT_L	54	
TRUE	GND		

FUNC_TEST

TRUE	GND	
TRUE	GND	6 TPs

USB PORTS

TRUE	PP5V_S3_RTUSB_A_F	43	
TRUE	USB2_LT1_N	43 99	
TRUE	USB2_LT1_P	43 99	
TRUE	GND		
TRUE	PP5V_S3_RTUSB_B_F	43	
TRUE	USB_LT2_N	43 99	
TRUE	USB_LT2_P	43 99	
TRUE	GND		

J3401 & J3402 (AIRPORT/BT/CAMERA CONN)

TRUE	PCIE_AP_D2R_P	17 33 94	
TRUE	PCIE_AP_D2R_N	17 33 94	
TRUE	PCIE_AP_R2D_P	33 94	
TRUE	PCIE_AP_R2D_N	33 94	
TRUE	PCIE_CLK100M_AP_CONN_P	33 99	
TRUE	PCIE_CLK100M_AP_CONN_N	33 99	
TRUE	AP_CLKREQ_Q_L	33	
TRUE	PCIE_WAKE_L	18 27 33	
TRUE	AP_RESET_CONN_L	33	
TRUE	PP3V3_WLAN	33	
TRUE	PP5V_S3_ALSCAMERA_F	33	
TRUE	SMBUS_SMC_A_S3_SDA	6 33 45 48 54 97	
TRUE	SMBUS_SMC_A_S3_SCL	6 33 45 48 54 97	
TRUE	USB_CAMERA_CONN_P	33 93	
TRUE	USB_CAMERA_CONN_N	33 93	
TRUE	CONN_USB2_BT_P	33 99	
TRUE	CONN_USB2_BT_N	33 99	

J3500 (SD CARD CONN)

TRUE	SD_D<7..0>	34	
TRUE	SD_CMD	34	
TRUE	SD_CLK	34	
TRUE	SD_CD_L	34 37	
TRUE	SD_WP	34 37	
TRUE	GND		2 TPs

J5713 (KEY BOARD CONN)

TRUE	PP3V3_S3	25 72 87 101	
TRUE	PP3V42_G3H	47 73 87 99	
TRUE	WS_KBD1	7 17 21 23 53	
TRUE	WS_KBD2	43 46 46 47 53 48 49 53 64 65 66 73	
TRUE	WS_KBD3	53	
TRUE	WS_KBD4	53	
TRUE	WS_KBD5	53	
TRUE	WS_KBD6	53	
TRUE	WS_KBD7	53	
TRUE	WS_KBD8	53	
TRUE	WS_KBD9	53	
TRUE	WS_KBD10	53	
TRUE	WS_KBD11	53	
TRUE	WS_KBD12	53	
TRUE	WS_KBD13	53	
TRUE	WS_KBD14	53	
TRUE	WS_KBD15_CAP	53	
TRUE	WS_KBD16_NUM	53	
TRUE	WS_KBD17	53	
TRUE	WS_KBD18	53	
TRUE	WS_KBD19	53	
TRUE	WS_KBD20	53	
TRUE	WS_KBD21	53	
TRUE	WS_KBD22	53	
TRUE	WS_KBD23	53	
TRUE	WS_KBD_ONOFF_L	53	
TRUE	WS_LEFT_SHIFT_KBD	53	
TRUE	WS_LEFT_OPTION_KBD	53	
TRUE	WS_CONTROL_KBD	53	

J6950 (BIL CABLE CONN)

TRUE	PP5V_S3_IR_R	42	
TRUE	SMC_LID_R	64	
TRUE	IR_RX_OUT	42 44	
TRUE	SYS_LED_ANODE	42 46	
TRUE	GND		

J5800 (IPD FLEX CONN)

TRUE	PP18V5_S3	6 54	
TRUE	Z2_CS_L	53 54	
TRUE	Z2_DEBUG3	53 54	
TRUE	Z2_MISO	53 54	
TRUE	Z2_BOOST_EN	54	
TRUE	Z2_SCLK	53 54	
TRUE	Z2_CLKIN	53 54	
TRUE	Z2_KEY_ACT_L	53 54	
TRUE	Z2_RESET	53 54	
TRUE	PSOC_F_CS_L	53 54	
TRUE	PICKB_L	53 54	
TRUE	PSOC_MISO	53 54	
TRUE	PSOC_MOSI	53 54	
TRUE	PSOC_SCLK	53 54	
TRUE	SMBUS_SMC_A_S3_SCL	6 33 45 48 54 97	
TRUE	SMBUS_SMC_A_S3_SDA	6 33 45 48 54 97	

J6900 (DC POWER CONN)

TRUE	ADAPTER_SENSE	64	
TRUE	PP18V5_DCIN_FUSE	64	
TRUE	GND		

J6950 (MAIN BATT CONN)

TRUE	PPVBAT_G3H_CONN	64 65	
TRUE	SMBUS_SMC_BSA_SCL	6 45 48 64 65 97	
TRUE	SMBUS_SMC_BSA_SDA	6 45 48 64 65 97	
TRUE	NC_SMC_BS_ALRT_L	6	
TRUE	GND		

J6995 (BAT LED CONN)

TRUE	PP3V42_G3H	73 64 65 66 48 49 53 21 23 43 45 46 47 17 6 65 97	
TRUE	SMBUS_SMC_BSA_SDA	6 45 48 64 65 97	
TRUE	SMBUS_SMC_BSA_SCL	6 45 48 64 17 6	
TRUE	SMC_BIL_BUTTON_L	45 46 64	
TRUE	GND		

FUNC_TEST

TRUE	BKLT_EN	88	
TRUE	TP_ISSP_SCLK_P1_1	8 53	
TRUE	TP_ISSP_SDATA_P1_0	8 53	
TRUE	LCD_BKLT_PWM	87 88	
TRUE	LPCPLUS_GPIO	20 47	
TRUE	LPCPLUS_RESET_L	27 47 87 94	
TRUE	LPC_AD<0..3>	17 45 47 87 94	
TRUE	LPC_CLK33M_LPCPLUS	27 47 94	
TRUE	LPC_FRAME_L	17 45 47 87 94	
TRUE	LPC_PWRDWN_L	18 45 47	
TRUE	LPC_SERIRQ	17 45 47	
TRUE	PM_CLKRUN_L	18 45 47	
TRUE	PM_SYSRST_L	18 27 45	
TRUE	SMC_MD1	45 47	
TRUE	SMC_NMI	45 47	
TRUE	SMC_ONOFF_L	45 46 53	
TRUE	SMC_RESET_L	45 46 47 65	
TRUE	SMC_RX_L	43 45 46 47	
TRUE	SMC_TCK	45 46 47	
TRUE	SMC_TDI	45 46 47	
TRUE	SMC_TDO	45 46 47	
TRUE	SMC_TMS	45 46 47	
TRUE	SMC_TRST_L	45 47	
TRUE	SMC_TX_L	43 45 46 47	
TRUE	SPIROM_USE_MLB	20 47 57	
TRUE	SPI_ALT_CLK	47	
TRUE	SPI_ALT_CS_L	47	
TRUE	SPI_ALT_MISO	47	
TRUE	SPI_ALT_MOSI	47	
TRUE	SYS_LED_ANODE_R	42	

POWER RAILS

FUNC_TEST

TRUE	PM_SLP_S3_L	18 31 45 73 85	
TRUE	PP0V75_S0_DDRVTT	7 28 30 31 67	
TRUE	PP18V5_S3	6 54	
TRUE	PP1V05_S0	7 19 12 13 15 17 18 20 21 23 24 25 26 40 78 79 86	
TRUE	PP1V05_S0GPU	7 74 76 79 81 86	
TRUE	PP1V05_S5	7 17 71	
TRUE	PP1V0_FW_FWPHY	7 39 40	
TRUE	PP1V2_ENET	7 37 71 72	
TRUE	PP1V2_S0	7 72 87	
TRUE	PP1V5_S3	7 28 30 31 67 72	
TRUE	PP1V5_S3RS0	7 13 16 31 42 72 73 99	
TRUE	PP1V8R1V55_S0GPU_ISNS	7 8 50 56 75 76 77 78	
TRUE	PP1V8R1V55_S0GPU_ISNS_R	7 50 86	
TRUE	PP1V8_GPUIFPX	7 72 81	
TRUE	PP1V8_S0	7 12 16 21 23 24 58 71 72 87	
TRUE	PP3V3_ENET	7 27 37 73	
TRUE	PP3V3_FW_FWPHY	7 39 40 41	
TRUE	PP3V3_S0	50 51 52 54 83 84 85 87 88 99	
TRUE	PP3V3_S0GPU	6 7 13 14 19 20 21 23 24 25 26 27 28 30 34 37 40 42 46 47 48	
TRUE	PP3V3_S3	7 72 74 79 80 81 82 84 73 89	
TRUE	PP3V3_S5	6 7 21 31 32 33 34 35 36 48 59 53 54 55 72 73 87 101	
TRUE	PP3V3_S5_AVREF_SMC	7 17 18 19 21 22 23 27 31 35 57 45 46 71 72 73 83 85 99	
TRUE	PP3V42_G3H	6 7 17 21 23 43 45 46 47 48 49 53 64 65 66 73	
TRUE	PP5V_S0	6 7 23 42 47 52 54 68 69 70 72 86 88	
TRUE	PP5V_S3	7 31 33 42 43 44 46 54 56 58 61 66 67 72 82 101	
TRUE	PP5V_S5	7 23 66 72	
TRUE	PPBUS_G3H	7 40 49 65 66 67 69 70 82 86 89	
TRUE	PPDCIN_G3H	7 64 65	
TRUE	PPVCORE_GPU	7 49 75 82	
TRUE	PPVCORE_S0_CPU	7 12 15 49 68	
TRUE	PPVCORE_S0_GFX	7 13 24 49 69	
TRUE	PPVP_FW	7 40 41	
TRUE	PPVTTDDR_S3	7 32 67	

ICT Test Points

CPU NO_TESTs

NO_TEST

TRUE	TP_CPU_RSVD<65..62>	MAKE_BASE=TRUE	NC_TP_CPU_RSVD<65..62>
TRUE	TP_CPU_RSVD<58..45>	MAKE_BASE=TRUE	NC_TP_CPU_RSVD<58..45>
TRUE	TP_CPU_RSVD<43..32>	MAKE_BASE=TRUE	NC_TP_CPU_RSVD<43..32>
TRUE	TP_CPU_RSVD<27..26>	MAKE_BASE=TRUE	NC_TP_CPU_RSVD<27..26>
TRUE	TP_CPU_RSVD<24..15>	MAKE_BASE=TRUE	NC_TP_CPU_RSVD<24..15>
TRUE	TP_CPU_RSVD<2..1>	MAKE_BASE=TRUE	NC_TP_CPU_RSVD<2..1>
TRUE	TP_CPU_RSVD_NCTF<8..5>	MAKE_BASE=TRUE	NC_TP_CPU_RSVD_NCTF<8..5>

NC NO_TESTs

NO_TEST

TRUE	NC_CRT_IG_BLUE	MAKE_BASE=TRUE	NC_CRT_IG_BLUE
TRUE	NC_CRT_IG_GREEN	MAKE_BASE=TRUE	NC_CRT_IG_GREEN
TRUE	NC_CRT_IG_RED	MAKE_BASE=TRUE	NC_CRT_IG_RED
TRUE	NC_CRT_IG_DDC_CLK	MAKE_BASE=TRUE	NC_CRT_IG_DDC_CLK
TRUE	NC_CRT_IG_DDC_DATA	MAKE_BASE=TRUE	NC_CRT_IG_DDC_DATA
TRUE	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE	NC_CRT_IG_HSYNC
TRUE	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE	NC_CRT_IG_VSYNC
TRUE	NC_LVDS_IG_CTRL_CLK	MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_CLK
TRUE	NC_LVDS_IG_CTRL_DATA	MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_DATA
TRUE	NC_PCH_LVDS_VBG	MAKE_BASE=TRUE	NC_PCH_LVDS_VBG
TRUE	NC_HDA_SDIN1	MAKE_BASE=TRUE	NC_HDA_SDIN1
TRUE	NC_HDA_SDIN2	MAKE_BASE=TRUE	NC_HDA_SDIN2
TRUE	NC_HDA_SDIN3	MAKE_BASE=TRUE	NC_HDA_SDIN3

NC NO_TESTs

NO_TEST

TRUE	TP_PCI_AD<31..0>	MAKE_BASE=TRUE	NC_PCI_AD<31..0>
TRUE	TP_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE	NC_PCI_C_BE_L<3..0>
TRUE	NC_PCI_GNT3_L	MAKE_BASE=TRUE	NC_PCI_GNT3_L
TRUE	NC_PCI_GNT2_L	MAKE_BASE=TRUE	NC_PCI_GNT2_L
TRUE	NC_PCI_GNT1_L	MAKE_BASE=TRUE	NC_PCI_GNT1_L
TRUE	NC_PCI_GNT0_L	MAKE_BASE=TRUE	NC_PCI_GNT0_L
TRUE	NC_PCI_PAR	MAKE_BASE=TRUE	NC_PCI_PAR
TRUE	NC_PCI_RESET_L	MAKE_BASE=TRUE	NC_PCI_RESET_L
TRUE	NC_PCI_PME_L	MAKE_BASE=TRUE	NC_PCI_PME_L
TRUE	NC_PCI_CLK33M_OUT3	MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT3
TRUE	NC_PCH_NV_RCOMP	MAKE_BASE=TRUE	NC_PCH_NV_RCOMP
TRUE	TP_NV_DQ<15..0>	MAKE_BASE=TRUE	NC_NV_DQ<15..0>
TRUE	TP_NV_DQS<1..0>	MAKE_BASE=TRUE	NC_NV_DQS<1..0>
TRUE	TP_NV_CE_L<3..0>	MAKE_BASE=TRUE	NC_NV_CE_L<3..0>
TRUE	NC_NV_ALE	MAKE_BASE=TRUE	NC_NV_ALE
TRUE	NC_NV_CLE	MAKE_BASE=TRUE	NC_NV_CLE
TRUE	NC_NV_RB_L	MAKE_BASE=TRUE	NC_NV_RB_L
TRUE	TP_NV_WR_RE_L<1..0>	MAKE_BASE=TRUE	NC_NV_WR_RE_L<1..0>
TRUE	TP_NV_WE_CK_L<1..0>	MAKE_BASE=TRUE	NC_NV_WE_CK_L<1..0>
TRUE	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4N
TRUE	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4P
TRUE	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5N
TRUE	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5P
TRUE	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6N
TRUE	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6P
TRUE	NC_PCIE_CLK100M_PE7N	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7N
TRUE	NC_PCIE_CLK100M_PE7P	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7P
TRUE	NC_PSOC_P1_3	MAKE_BASE=TRUE	NC_PSOC_P1_3
TRUE	NC_SATA_C_D2RN	MAKE_BASE=TRUE	NC_SATA_C_D2RN
TRUE	NC_SATA_C_D2RP	MAKE_BASE=TRUE	NC_SATA_C_D2RP
TRUE	NC_SATA_C_R2D_CN	MAKE_BASE=TRUE	NC_SATA_C_R2D_CN
TRUE	NC_SATA_C_R2D_CP	MAKE_BASE=TRUE	NC_SATA_C_R2D_CP
TRUE	NC_SATA_D_D2RN	MAKE_BASE=TRUE	NC_SATA_D_D2RN
TRUE	NC_SATA_D_D2RP	MAKE_BASE=TRUE	NC_SATA_D_D2RP
TRUE	NC_SATA_D_R2D_CN	MAKE_BASE=TRUE	NC_SATA_D_R2D_CN
TRUE	NC_SATA_D_R2D_CP	MAKE_BASE=TRUE	NC_SATA_D_R2D_CP
TRUE	NC_SATA_SSD2_D2RN	MAKE_BASE=TRUE	NC_SATA_SSD2_D2RN
TRUE	NC_SATA_SSD2_D2RP	MAKE_BASE=TRUE	NC_SATA_SSD2_D2RP
TRUE	NC_SATA_SSD2_R2D_CN	MAKE_BASE=TRUE	NC_SATA_SSD2_R2D_CN
TRUE	NC_SATA_SSD2_R2D_CP	MAKE_BASE=TRUE	NC_SATA_SSD2_R2D_CP
TRUE	TP_SMC_P41	MAKE_BASE=TRUE	NC_SMC_P41

NC NO_TESTs

NO_TEST

TRUE	NC_PCIE_PE5_D2RN	MAKE_BASE=TRUE	NC_PCIE_PE5_D2RN
TRUE	NC_PCIE_PE5_D2RP	MAKE_BASE=TRUE	NC_PCIE_PE5_D2RP
TRUE	NC_PCIE_PE5_R2D_CN	MAKE_BASE=TRUE	NC_PCIE_PE5_R2D_CN
TRUE	NC_PCIE_PE5_R2D_CP	MAKE_BASE=TRUE	NC_PCIE_PE5_R2D_CP
TRUE	NC_PCIE_PE6_D2RN	MAKE_BASE=TRUE	NC_PCIE_PE6_D2RN
TRUE	NC_PCIE_PE6_D2RP	MAKE_BASE=TRUE	NC_PCIE_PE6_D2RP
TRUE	NC_PCIE_PE6_R2D_CN	MAKE_BASE=TRUE	NC_PCIE_PE6_R2D_CN
TRUE	NC_PCIE_PE6_R2D_CP	MAKE_BASE=TRUE	NC_PCIE_PE6_R2D_CP
TRUE	NC_PCIE_PE7_D2RN	MAKE_BASE=TRUE	NC_PCIE_PE7_D2RN
TRUE	NC_PCIE_PE7_D2RP	MAKE_BASE=TRUE	NC_PCIE_PE7_D2RP
TRUE	NC_PCIE_PE7_R2D_CN	MAKE_BASE=TRUE	NC_PCIE_PE7_R2D_CN
TRUE	NC_PCIE_PE7_R2D_CP	MAKE_BASE=TRUE	NC_PCIE_PE7_R2D_CP
TRUE	NC_PCIE_PE8_D2RN	MAKE_BASE=TRUE	NC_PCIE_PE8_D2RN
TRUE	NC_PCIE_PE8_D2RP	MAKE_BASE=TRUE	NC_PCIE_PE8_D2RP
TRUE	NC_PCIE_PE8_R2D_CN	MAKE_BASE=TRUE	NC_PCIE_PE8_R2D_CN
TRUE	NC_PCIE_PE8_R2D_CP	MAKE_BASE=TRUE	NC_PCIE_PE8_R2D_CP

NC NO_TESTs

NO_TEST

TRUE	NC_CLINK_CLK	MAKE_BASE=TRUE	NC_CLINK_CLK
TRUE	NC_CLINK_DATA	MAKE_BASE=TRUE	NC_CLINK_DATA
TRUE	NC_CLINK_RESET_L	MAKE_BASE=TRUE	NC_CLINK_RESET_L
TRUE	NC_PCIE_CLK100M_PEBN	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBN
TRUE	NC_PCIE_CLK100M_PEBP	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBP

NC NO_TESTs

NO_TEST

TRUE	NC_SMC_FAN_3_TACH	MAKE_BASE=TRUE	NC_SMC_FAN_3_TACH
TRUE	NC_SMC_FAN_3_CTL	MAKE_BASE=TRUE	NC_SMC_FAN_3_CTL
TRUE	NC_SMC_FAN_2_TACH	MAKE_BASE=TRUE	NC_SMC_FAN_2_TACH
TRUE	NC_SMC_FAN_2_CTL	MAKE_BASE=TRUE	NC_SMC_FAN_2_CTL
TRUE	NC_FW2_TPBP	MAKE_BASE=TRUE	NC_FW2_TPBP
TRUE	NC_FW2_TPBN	MAKE_BASE=TRUE	NC_FW2_TPBN
TRUE	NC_FW2_TPBIAS	MAKE_BASE=TRUE	NC_FW2_TPBIAS
TRUE	NC_FW2_TPAP	MAKE_BASE=TRUE	NC_FW2_TPAP
TRUE	NC_FW2_TPAN	MAKE_BASE=TRUE	NC_FW2_TPAN
TRUE	NC_FW0_TPBP	MAKE_BASE=TRUE	NC_FW0_TPBP
TRUE	NC_FW0_TPBN	MAKE_BASE=TRUE	NC_FW0_TPBN
TRUE	NC_FW0_TPAP	MAKE_BASE=TRUE	NC_FW0_TPAP
TRUE	NC_ESTARLDO_EN	MAKE_BASE=TRUE	NC_ESTARLDO_EN
TRUE	NC_ALS_GAIN	MAKE_BASE=TRUE	NC_ALS_GAIN
TRUE	NC_FW643_AVREG	MAKE_BASE=TRUE	NC_FW643_AVREG
TRUE	NC_FW643_TDI	MAKE_BASE=TRUE	NC_FW643_TDI
TRUE	NC_DP_IG_C_HPD	MAKE_BASE=TRUE	NC_DP_IG_C_HPD
TRUE	NC_DP_IG_C_CTRL_CLK	MAKE_BASE=TRUE	NC_DP_IG_C_CTRL_CLK
TRUE	NC_DP_IG_C_CTRL_DATA	MAKE_BASE=TRUE	NC_DP_IG_C_CTRL_DATA
TRUE	TP_DP_IG_C_MLP<3..0>	MAKE_BASE=TRUE	NC_DP_IG_C_MLP<3..0>
TRUE	TP_DP_IG_C_MLN<3..0>	MAKE_BASE=TRUE	NC_DP_IG_C_MLN<3..0>
TRUE	NC_DP_IG_C_AUXP	MAKE_BASE=TRUE	NC_DP_IG_C_AUXP
TRUE	NC_DP_IG_C_AUXN	MAKE_BASE=TRUE	NC_DP_IG_C_AUXN
TRUE	NC_DP_IG_D_HPD	MAKE_BASE=TRUE	NC_DP_IG_D_HPD
TRUE	NC_DP_IG_D_CTRL_CLK	MAKE_BASE=TRUE	NC_DP_IG_D_CTRL_CLK
TRUE	NC_DP_IG_D_CTRL_DATA	MAKE_BASE=TRUE	NC_DP_IG_D_CTRL_DATA
TRUE	TP_DP_IG_D_MLP<3..0>	MAKE_BASE=TRUE	NC_DP_IG_D_MLP<3..0>
TRUE	TP_DP_IG_D_MLN<3..0>	MAKE_BASE=TRUE	NC_DP_IG_D_MLN<3..0>
TRUE	NC_DP_IG_D_AUXP	MAKE_BASE=TRUE	NC_DP_IG_D_AUXP
TRUE	NC_DP_IG_D_AUXN	MAKE_BASE=TRUE	NC_DP_IG_D_AUXN
TRUE	NC_SDVO_TVCLKINN	MAKE_BASE=TRUE	NC_SDVO_TVCLKINN
TRUE	NC_SDVO_TVCLKINP	MAKE_BASE=TRUE	NC_SDVO_TVCLKINP
TRUE	NC_SDVO_STALLN	MAKE_BASE=TRUE	NC_SDVO_STALLN
TRUE	NC_SDVO_STALLP	MAKE_BASE=TRUE	NC_SDVO_STALLP
TRUE	NC_SDVO_INTN	MAKE_BASE=TRUE	NC_SDVO_INTN
TRUE	NC_SDVO_INTP	MAKE_BASE=TRUE	NC_SDVO_INTP
TRUE	NC_GPU_BUFRST_L	MAKE_BASE=TRUE	NC_GPU_BUFRST_L
TRUE	TP_GPU_GSTATE<0>	MAKE_BASE=TRUE	NC_GPU_GSTATE<0>
TRUE	TP_GPU_GSTATE<1>	MAKE_BASE=TRUE	NC_GPU_GSTATE<1>
TRUE	TP_GPU_MIOA_D<9..0>	MAKE_BASE=TRUE	NC_GPU_MIOA_D<9..0>
TRUE	TP_GPU_MIOA_DE	MAKE_BASE=TRUE	NC_GPU_MIOA_DE
TRUE	NC_LVDS_EG_BKL_PWM	MAKE_BASE=TRUE	NC_LVDS_EG_BKL_PWM
TRUE	TP_LVDS_IG_B_CLKN	MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKN
TRUE	TP_LVDS_IG_B_CLKP	MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKP
TRUE	TP_LVDS_IG_BKL_PWM	MAKE_BASE=TRUE	NC_LVDS_IG_BKL_PWM
TRUE	NC_SMC_BS_ALRT_L	MAKE_BASE=TRUE	NC_SMC_BS_ALRT_L
TRUE	NC_PCH_SST	MAKE_BASE=TRUE	NC_PCH_SST
TRUE	NC_PCH_NC1	MAKE_BASE=TRUE	NC_PCH_NC1
TRUE	NC_PCH_NC2	MAKE_BASE=TRUE	NC_PCH_NC2
TRUE	NC_PCH_NC3	MAKE_BASE=TRUE	NC_PCH_NC3
TRUE	NC_PCH_NC4	MAKE_BASE=TRUE	NC_PCH_NC4
TRUE	NC_PCH_NC5	MAKE_BASE=TRUE	NC_PCH_NC5
TRUE	NC_PCH_TP19	MAKE_BASE=TRUE	NC_PCH_TP19
TRUE	NC_PCH_TP18	MAKE_BASE=TRUE	NC_PCH_TP18
TRUE	NC_PCH_TP17	MAKE_BASE=TRUE	NC_PCH_TP17
TRUE	NC_PCH_TP16	MAKE_BASE=TRUE	NC_PCH_TP16
TRUE	NC_PCH_TP15	MAKE_BASE=TRUE	NC_PCH_TP15
TRUE	NC_PCH_TP14	MAKE_BASE=TRUE	NC_PCH_TP14
TRUE	NC_PCH_TP13	MAKE_BASE=TRUE	NC_PCH_TP13
TRUE	NC_PCH_TP12	MAKE_BASE=TRUE	NC_PCH_TP12
TRUE	NC_PCH_TP11	MAKE_BASE=TRUE	NC_PCH_TP11
TRUE	NC_PCH_TP10	MAKE_BASE=TRUE	NC_PCH_TP10
TRUE	NC_PCH_TP9	MAKE_BASE=TRUE	NC_PCH_TP9
TRUE	NC_PCH_TP8	MAKE_BASE=TRUE	NC_PCH_TP8
TRUE	NC_PCH_TP7	MAKE_BASE=TRUE	NC_PCH_TP7
TRUE	NC_PCH_TP6	MAKE_BASE=TRUE	NC_PCH_TP6
TRUE	NC_PCH_TP5	MAKE_BASE=TRUE	NC_PCH_TP5
TRUE	NC_PCH_TP4	MAKE_BASE=TRUE	NC_PCH_TP4
TRUE	NC_PCH_TP3	MAKE_BASE=TRUE	NC_PCH_TP3
TRUE	NC_PCH_TP2	MAKE_BASE=TRUE	NC_PCH_TP2
TRUE	NC_PCH_TP1	MAKE_BASE=TRUE	NC_PCH_TP1
TRUE	PCH_VSS_NCTF<1>		PCH_VSS_NCTF<15>
TRUE	PCH_VSS_NCTF<2>		PCH_VSS_NCTF<17>
TRUE	PCH_VSS_NCTF<5>		PCH_VSS_NCTF<19>
TRUE	PCH_VSS_NCTF<7>		PCH_VSS_NCTF<21>
TRUE	PCH_VSS_NCTF<9>		PCH_VSS_NCTF<25>
TRUE	PCH_VSS_NCTF<11>		PCH_VSS_NCTF<27>
TRUE	PCH_VSS_NCTF<12>		PCH_VSS_NCTF<29>

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Functional / ICT Test

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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"G3Hot" (Always-Present) Rails

PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H

PPBUS_CPU_IMVP_ISNS
PPBUS_CPU_IMVP_ISNS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
PPBUS_CPU_IMVP_ISNS

PPDCIN_G3H
PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18V
MAKE_BASE=TRUE
PPDCIN_G3H

PP3V42_G3H
PP3V42_G3H
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
PP3V42_G3H (×16)

5V Rails

PP5V_S5
PP5V_S5
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S5 (×3)

PP5V_S3
PP5V_S3
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S3 (×16)

PP5V_S0
PP5V_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S0 (×16)

3.3V Rails

PP3V_S5
PP3V_S5
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V_S5 (×30)

PP3V_S3
PP3V_S3
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V_S3 (×50)

PP3V_S0
PP3V_S0
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V_S0 (×50)

PP1V2_S0
PP1V2_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.09 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
PP1V2_S0

PP1V05_S5
PP1V05_S5
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
PP1V05_S5

PP1V05_S0
PP1V05_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
PP1V05_S0 (×50)

PP3V3_S0
PP3V3_S0
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S0 (×50)

PP1V2_ENET
PP1V2_ENET
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE
PP1V2_ENET

1.8V/1.5V/1.2V/1.05V Rails

PP1V8_S0 — 2A max supply
PP1V8_S0
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_S0 (×10)

PP1V5_S3
PP1V5_S3
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
PP1V5_S3 (×6)

PP1V5_S3RS0
PP1V5_S3RS0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
PP1V5_S3RS0 (×4)

PPVTTDDR_S3
PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

PP0V75_S0_DDRVTT
PP0V75_S0_DDRVTT
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
PP0V75_S0_DDRVTT (×4)

ENET Rails

PP3V3_ENET
PP3V3_ENET
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_ENET

"FW" (FireWire) Rails

PPVP_FW
PPVP_FW
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
PPVP_FW
PPVP_FW

PP3V3_FW_FWPHY
PP3V3_FW_FWPHY
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_FW_FWPHY (×2)

PP1V0_FW_FWPHY
PP1V0_FW_FWPHY
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
MAKE_BASE=TRUE
PP1V0_FW_FWPHY

"GPU" Rails

PP3V3_S0GPU
PP3V3_S0GPU
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S0GPU (×4)

PP1V8_GPUIFPX
PP1V8_GPUIFPX
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_GPUIFPX

PP1V8R1V55_S0GPU_ISNS
PP1V8R1V55_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8R1V55_S0GPU_ISNS (×4)

PP1V8R1V55_S0GPU_ISNS_R
PP1V8R1V55_S0GPU_ISNS_R
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8R1V55_S0GPU_ISNS_R

PP1V05_S0GPU
PP1V05_S0GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
PP1V05_S0GPU (×16)

PPVCORE_GPU
PPVCORE_GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
PPVCORE_GPU

Chipset "VCore" Rails

PPVCORE_S0_CPU
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
PPVCORE_S0_CPU

PPVCORE_S0_GFX
PPVCORE_S0_GFX
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
PPVCORE_S0_GFX

PPVCORE_S0_CPU_VCAP0
PPVCORE_S0_CPU_VCAP0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE

PPVCORE_S0_CPU_VCAP1
PPVCORE_S0_CPU_VCAP1
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE

PPVCORE_S0_CPU_VCAP2
PPVCORE_S0_CPU_VCAP2
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE

SYNC_MASTER=MASTER
SYNC_DATE=MASTER
PAGE TITLE
Power Aliases
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REVISION <E4LABEL>
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Thermal Module Holes

ZT0984 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0987 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0980 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0981 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0985 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0986 STDOFF-4.50D.98H-1.1-3.48-TH

Fan Holes

ZT0930 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0988 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0989 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0991 STDOFF-4.50D.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P5 — GND
ZT0940 3R2P5 — GND
ZT0950 TH — GND — SL-3.1X2.7-6CIR-NSP
ZT0960 3R2P5 — GND
ZT0990 3R2P5 — GND

Left Speaker Holes

ZT0934 STDOFF-4.0OD3.0H-TH
ZT0935 STDOFF-4.0OD3.0H-TH

Keyboard / IPD Conn Protect

ZT0952 4.0OD1.85H-M1.6X0.35
ZT0953 4.0OD1.85H-M1.6X0.35

Tall EMI pogo pins

SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98
SH0904 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0916 2.0DIA-TALL-EMI-MLB-M97-M98

Short (IO Row) EMI pogo pins

SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0901 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0917 1.4DIA-SHORT-EMI-MLB-M97-M98

GND_CHASSIS_AUDIO_JACK

GMUX ALIASES

PM_ALL_GPU_PGOOD — PM_ALL_GPU_PGOOD
TP_LVDS_MUX_SEL_EG — TP_LVDS_MUX_SEL_EG
EG_RESET_L — EG_RESET_L
LVDS_IG_BKL_ON — LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR — LVDS_IG_PANEL_PWR
LCD_BKLT_EN — LCD_BKLT_EN
PEX_CLKREQ_L — PEX_CLKREQ_L
PEG_CLKREQ_L — PEG_CLKREQ_L
PM_ENET_EN — PM_ENET_EN
FW_PLUG_DET_L — FW_PLUG_DET_L
FW643_WAKE_L — FW643_WAKE_L
TP_SMC_EXCARD_PWR_EN — TP_SMC_EXCARD_PWR_EN
NC_SATA_EXTA_D2R_N — NC_SATA_EXTA_D2R_N
NC_SATA_EXTA_D2R_P — NC_SATA_EXTA_D2R_P
NC_SATA_EXTA_R2D_C_N — NC_SATA_EXTA_R2D_C_N
NC_SATA_EXTA_R2D_C_P — NC_SATA_EXTA_R2D_C_P
NC_PCIE_EXCARD_D2R_N — NC_PCIE_EXCARD_D2R_N
NC_PCIE_EXCARD_D2R_P — NC_PCIE_EXCARD_D2R_P
NC_PCIE_EXCARD_R2D_C_N — NC_PCIE_EXCARD_R2D_C_N
NC_PCIE_EXCARD_R2D_C_P — NC_PCIE_EXCARD_R2D_C_P
NC_PCIE_CLK100M_EXCARD_N — NC_PCIE_CLK100M_EXCARD_N
NC_PCIE_CLK100M_EXCARD_P — NC_PCIE_CLK100M_EXCARD_P
TP_ISSP_SCLK_P1_1 — TP_ISSP_SCLK_P1_1
TP_ISSP_SDATA_P1_0 — TP_ISSP_SDATA_P1_0

GND
GND
GND
GND
GND

CPU signals

CPU_VID<0..6> — CPUIMVP_VID<0..6>
GFX_VID<0..6> — GFXIMVP_VID<0..6>
MEMVTT_EN — MEMVTT_EN
TP_CPU_VTT_SELECT — TP_CPU_VTT_SELECT

GPU signals

PEG_D2R_P<15..0> — =PEG_D2R_P<0..15>
PEG_D2R_N<15..0> — =PEG_D2R_N<0..15>
PEG_R2D_C_P<15..0> — =PEG_R2D_C_P<0..15>
PEG_R2D_C_N<15..0> — =PEG_R2D_C_N<0..15>

** PEG LANES REVERSED. ARD STRAP REQ'D. **

R0902 3.0K 5% 1/16W MF-LF 402
CPU_CFG<3>

DP_IG_ML_P<3..0> — DP_IG_B_ML_P<3..0>
DP_IG_ML_N<3..0> — DP_IG_B_ML_N<3..0>
DP_IG_AUX_CH_P — DP_IG_AUX_CH_P
DP_IG_AUX_CH_N — DP_IG_AUX_CH_N
DP_IG_DDC_CLK — DP_IG_DDC_CLK
DP_IG_DDC_DATA — DP_IG_DDC_DATA
DP_IG_HPD — DP_IG_HPD

TP_LVDS_IG_B_CLKP — TP_LVDS_IG_B_CLKP
TP_LVDS_IG_B_CLKN — TP_LVDS_IG_B_CLKN
TP_LVDS_IG_BKL_PWM — TP_LVDS_IG_BKL_PWM
NC_GPU_XTALOUT — NC_GPU_XTALOUT
NC_LVDS_IG_A_DATAP<3> — NC_LVDS_IG_A_DATAP<3>
NC_LVDS_IG_A_DATAN<3> — NC_LVDS_IG_A_DATAN<3>
NC_LVDS_IG_B_DATAP<3> — NC_LVDS_IG_B_DATAP<3>
NC_LVDS_IG_B_DATAN<3> — NC_LVDS_IG_B_DATAN<3>
NC_USB_HUB1_OCS4 — NC_USB_HUB1_OCS4
NC_USB_HUB2_OCS3 — NC_USB_HUB2_OCS3
USB_SDCARD_P — USB_SDCARD_P
USB_SDCARD_N — USB_SDCARD_N

PP3V3_S3
R0903 10K 5% 1/16W MF-LF 402
R0904 10K 5% 1/16W MF-LF 402
USB_EXTC_N
USB_EXTC_P

PP1V8R1V55_S0GPU_ISNS
R0900 10 1% 1/10W MF-LF 402 — GPU_FB_A_VREF_DIV
GPU_FB_A_VREF_DIV
R0901 10 1% 1/10W MF-LF 402 — GPU_FB_B_VREF_DIV
GPU_FB_B_VREF_DIV

Digital Ground

GND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.095 mm
VOLTAGE=0V

SYNC_MASTER=K17_REF SYNC_DATE=06/11/2009

PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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ARRANDALE
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DMI

DMI_S2N_N<0>	F7	DMI_RX0*
DMI_S2N_N<1>	J8	DMI_RX1*
DMI_S2N_N<2>	K8	DMI_RX2*
DMI_S2N_N<3>	J4	DMI_RX3*
DMI_S2N_P<0>	F9	DMI_RX0
DMI_S2N_P<1>	J6	DMI_RX1
DMI_S2N_P<2>	K9	DMI_RX2
DMI_S2N_P<3>	J2	DMI_RX3
DMI_N2S_N<0>	H17	DMI_TX0*
DMI_N2S_N<1>	K15	DMI_TX1*
DMI_N2S_N<2>	J13	DMI_TX2*
DMI_N2S_N<3>	F16	DMI_TX3*
DMI_N2S_P<0>	G17	DMI_TX0
DMI_N2S_P<1>	M15	DMI_TX1
DMI_N2S_P<2>	G13	DMI_TX2
DMI_N2S_P<3>	J11	DMI_TX3

FLEXIBLE DISPLAY INTERFACE

FDI_DATA_N<0>	L2	FDI_TX0*
FDI_DATA_N<1>	N7	FDI_TX1*
FDI_DATA_N<2>	M4	FDI_TX2*
FDI_DATA_N<3>	P1	FDI_TX3*
FDI_DATA_N<4>	N10	FDI_TX4*
FDI_DATA_N<5>	R7	FDI_TX5*
FDI_DATA_N<6>	U7	FDI_TX6*
FDI_DATA_N<7>	W8	FDI_TX7*
FDI_DATA_P<0>	K1	FDI_TX0
FDI_DATA_P<1>	N5	FDI_TX1
FDI_DATA_P<2>	N2	FDI_TX2
FDI_DATA_P<3>	R2	FDI_TX3
FDI_DATA_P<4>	N9	FDI_TX4
FDI_DATA_P<5>	R8	FDI_TX5
FDI_DATA_P<6>	U6	FDI_TX6
FDI_DATA_P<7>	W10	FDI_TX7
FDI_FSYNC<0>	AC7	FDI_FSYNC0
FDI_FSYNC<1>	AC9	FDI_FSYNC1
FDI_INT	AB5	FDI_INT
FDI_LSYNC<0>	AA1	FDI_LSYNC0
FDI_LSYNC<1>	AB2	FDI_LSYNC1

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI	B12	CPU_PEG_COMP
PEG_ICOMPO	A13	
PEG_RCOMPO	D12	
PEG_RBIAS	B11	CPU_PEG_RBIAS

R1012 750 1% 1/16W MF-LF 402
R1010 49.9 1% 1/16W MF-LF 402

PEG_RX0*	G40	=PEG_D2R_N<0>
PEG_RX1*	G38	=PEG_D2R_N<1>
PEG_RX2*	H34	=PEG_D2R_N<2>
PEG_RX3*	P34	=PEG_D2R_N<3>
PEG_RX4*	G28	=PEG_D2R_N<4>
PEG_RX5*	H25	=PEG_D2R_N<5>
PEG_RX6*	H24	=PEG_D2R_N<6>
PEG_RX7*	D29	=PEG_D2R_N<7>
PEG_RX8*	B26	=PEG_D2R_N<8>
PEG_RX9*	D26	=PEG_D2R_N<9>
PEG_RX10*	B23	=PEG_D2R_N<10>
PEG_RX11*	D22	=PEG_D2R_N<11>
PEG_RX12*	A20	=PEG_D2R_N<12>
PEG_RX13*	D19	=PEG_D2R_N<13>
PEG_RX14*	A17	=PEG_D2R_N<14>
PEG_RX15*	B14	=PEG_D2R_N<15>
PEG_RX0	F40	PEG_D2R_P<15>
PEG_RX1	J38	PEG_D2R_P<14>
PEG_RX2	G34	PEG_D2R_P<13>
PEG_RX3	M34	PEG_D2R_P<12>
PEG_RX4	J28	PEG_D2R_P<11>
PEG_RX5	G25	PEG_D2R_P<10>
PEG_RX6	K24	PEG_D2R_P<9>
PEG_RX7	B28	PEG_D2R_P<8>
PEG_RX8	A27	PEG_D2R_P<7>
PEG_RX9	B25	PEG_D2R_P<6>
PEG_RX10	A24	PEG_D2R_P<5>
PEG_RX11	B21	PEG_D2R_P<4>
PEG_RX12	B19	PEG_D2R_P<3>
PEG_RX13	B18	PEG_D2R_P<2>
PEG_RX14	B16	PEG_D2R_P<1>
PEG_RX15	D15	PEG_D2R_P<0>

Embedded DisplayPort (eDP) pins (Auburndale only):

eDP_AUX#

NOTE: HPD must be inverted and level-shifted for Auburndale (1.05V).

eDP_HPD#
eDP_AUX

PEG_TX0*	N40	=PEG_R2D_C_N<0>
PEG_TX1*	L38	=PEG_R2D_C_N<1>
PEG_TX2*	M32	=PEG_R2D_C_N<2>
PEG_TX3*	D40	=PEG_R2D_C_N<3>
PEG_TX4*	A38	=PEG_R2D_C_N<4>
PEG_TX5*	G32	=PEG_R2D_C_N<5>
PEG_TX6*	B33	=PEG_R2D_C_N<6>
PEG_TX7*	B35	=PEG_R2D_C_N<7>
PEG_TX8*	L30	=PEG_R2D_C_N<8>
PEG_TX9*	A31	=PEG_R2D_C_N<9>
PEG_TX10*	B32	=PEG_R2D_C_N<10>
PEG_TX11*	L28	=PEG_R2D_C_N<11>
PEG_TX12*	N26	=PEG_R2D_C_N<12>
PEG_TX13*	M24	=PEG_R2D_C_N<13>
PEG_TX14*	G21	=PEG_R2D_C_N<14>
PEG_TX15*	J20	=PEG_R2D_C_N<15>
PEG_TX0	L40	PEG_R2D_C_P<15>
PEG_TX1	N38	PEG_R2D_C_P<14>
PEG_TX2	N32	PEG_R2D_C_P<13>
PEG_TX3	B39	PEG_R2D_C_P<12>
PEG_TX4	B37	PEG_R2D_C_P<11>
PEG_TX5	H32	PEG_R2D_C_P<10>
PEG_TX6	A34	PEG_R2D_C_P<9>
PEG_TX7	D36	PEG_R2D_C_P<8>
PEG_TX8	J30	PEG_R2D_C_P<7>
PEG_TX9	B30	PEG_R2D_C_P<6>
PEG_TX10	D33	PEG_R2D_C_P<5>
PEG_TX11	N28	PEG_R2D_C_P<4>
PEG_TX12	M25	PEG_R2D_C_P<3>
PEG_TX13	N24	PEG_R2D_C_P<2>
PEG_TX14	F21	PEG_R2D_C_P<1>
PEG_TX15	L20	PEG_R2D_C_P<0>

eDP_TX#<3>
eDP_TX#<2>
eDP_TX#<1>
eDP_TX#<0>

eDP_TX<3>
eDP_TX<2>
eDP_TX<1>
eDP_TX<0>

OMIT

U1000
ARRANDALE
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RESERVED

CPU_CFG<0>	AL4	CFG0 (IPU)
CPU_CFG<1>	AM2	CFG1 (IPU)
CPU_CFG<2>	AK1	CFG2 (IPU)
CPU_CFG<3>	AK2	CFG3 (IPU)
CPU_CFG<4>	AK4	CFG4 (IPU)
CPU_CFG<5>	AJ2	CFG5 (IPU)
CPU_CFG<6>	AT2	CFG6 (IPU)
CPU_CFG<7>	AG7	CFG7 (IPU)
CPU_CFG<8>	AF4	CFG8 (IPU)
CPU_CFG<9>	AG2	CFG9 (IPU)
CPU_CFG<10>	AH1	CFG10 (IPU)
CPU_CFG<11>	AC2	CFG11 (IPU)
CPU_CFG<12>	AC4	CFG12 (IPU)
CPU_CFG<13>	AE2	CFG13 (IPU)
CPU_CFG<14>	AD1	CFG14 (IPU)
CPU_CFG<15>	AF8	CFG15 (IPU)
CPU_CFG<16>	AF6	CFG16 (IPU)
CPU_CFG<17>	AB7	CFG17 (IPU)
TP_CPU_RSVD_TP0	AU1	RSVD_TP0
TP_CPU_RSVD<15>	T4	RSVD15
TP_CPU_RSVD<16>	T2	RSVD16
TP_CPU_RSVD<17>	U1	RSVD17
TP_CPU_RSVD<18>	V2	RSVD18
TP_CPU_RSVD<19>	AV71	RSVD19
TP_CPU_RSVD<20>	AW70	RSVD20
TP_CPU_RSVD<21>	AY69	RSVD21
TP_CPU_RSVD<22>	BB69	RSVD22
TP_CPU_RSVD<23>	D8	RSVD23
TP_CPU_RSVD<24>	B7	RSVD24
TP_CPU_RSVD<26>	A10	RSVD26
TP_CPU_RSVD<27>	B9	RSVD27
NC_TP_CPU_RSVD_NCTF<7>	C5	RSVD_NCTF7
NC_TP_CPU_RSVD_NCTF<8>	A6	RSVD_NCTF8
NC_TP_CPU_RSVD_NCTF<6>	E3	RSVD_NCTF6
NC_TP_CPU_RSVD_NCTF<5>	F1	RSVD_NCTF5

RSVD32	W66	NC_TP_CPU_RSVD<32>
RSVD33	W64	NC_TP_CPU_RSVD<33>
RSVD34	AC69	NC_TP_CPU_RSVD<34>
RSVD35	AC71	NC_TP_CPU_RSVD<35>
RSVD36	AA71	NC_TP_CPU_RSVD<36>
RSVD37	AA69	NC_TP_CPU_RSVD<37>
RSVD38	R66	NC_TP_CPU_RSVD<38>
RSVD39	R64	NC_TP_CPU_RSVD<39>
RSVD_NCTF3	BT5	NC_TP_CPU_RSVD<40>
RSVD_NCTF4	BR5	NC_TP_CPU_RSVD<41>
RSVD_NCTF2	BV6	NC_TP_CPU_RSVD<42>
RSVD_NCTF1	BV8	NC_TP_CPU_RSVD<43>
RSVD45	AV69	TP_CPU_RSVD<45>
RSVD46	AK71	TP_CPU_RSVD<46>
RSVD47	AN69	TP_CPU_RSVD<47>
RSVD48	AP66	TP_CPU_RSVD<48>
RSVD49	AH66	TP_CPU_RSVD<49>
RSVD50	AK66	TP_CPU_RSVD<50>
RSVD51	AR71	TP_CPU_RSVD<51>
RSVD52	AM66	TP_CPU_RSVD<52>
RSVD53	AK69	TP_CPU_RSVD<53>
RSVD54	AU71	TP_CPU_RSVD<54>
RSVD55	AT70	TP_CPU_RSVD<55>
RSVD56	AR69	TP_CPU_RSVD<56>
RSVD57	AU69	TP_CPU_RSVD<57>
RSVD58	AT67	TP_CPU_RSVD<58>
RSVD_TP2	AP2	TP_CPU_RSVD<2>
RSVD_TP1	AN7	TP_CPU_RSVD<1>
RSVD62	AV4	CPU_THERMD_P
RSVD63	AU2	CPU_THERMD_N
RSVD64	BE69	TP_CPU_RSVD<64>
RSVD65	BE71	TP_CPU_RSVD<65>
DC_TEST_BV71	BV71	CPU_TEST_BV71_BV69
DC_TEST_BV69	BV69	
DC_TEST_BV68	BV68	TP_CPU_TEST_BV68
DC_TEST_BV5	BV5	TP_CPU_TEST_BV5
DC_TEST_BV3	BV3	CPU_TEST_BV3_BT3
DC_TEST_BV1	BV1	CPU_TEST_BV1_BT1
DC_TEST_BT71	BT71	CPU_TEST_BT71_BT69
DC_TEST_BT69	BT69	
DC_TEST_BT3	BT3	
DC_TEST_BT1	BT1	
DC_TEST_BR71	BR71	TP_CPU_TEST_BR71
DC_TEST_BR1	BR1	TP_CPU_TEST_BR1
DC_TEST_E71	E71	TP_CPU_TEST_E71
DC_TEST_E1	E1	TP_CPU_TEST_E1
DC_TEST_C71	C71	CPU_TEST_C71_A71
DC_TEST_C69	C69	CPU_TEST_C69_A69
DC_TEST_C3	C3	TP_CPU_TEST_C3
DC_TEST_A71	A71	
DC_TEST_A69	A69	
DC_TEST_A68	A68	TP_CPU_TEST_A68
DC_TEST_A5	A5	TP_CPU_TEST_A5

CFG0: PCIe Configuration Select 1 = Single PEG 0 = Bifurcation Enabled
CFG3: PCIe Lane Reversal 1 = Normal Operation 0 = Lanes Reversed
CFG4: Display Port Presence 1 = eDP Disabled 0 = Embedded Display Port Enabled

WF: RSVD nets with arrows have offpage marks on CRB schematic.
WF: RSVD nets with red wires have 0-ohm resistors to GND in CRB schematic.

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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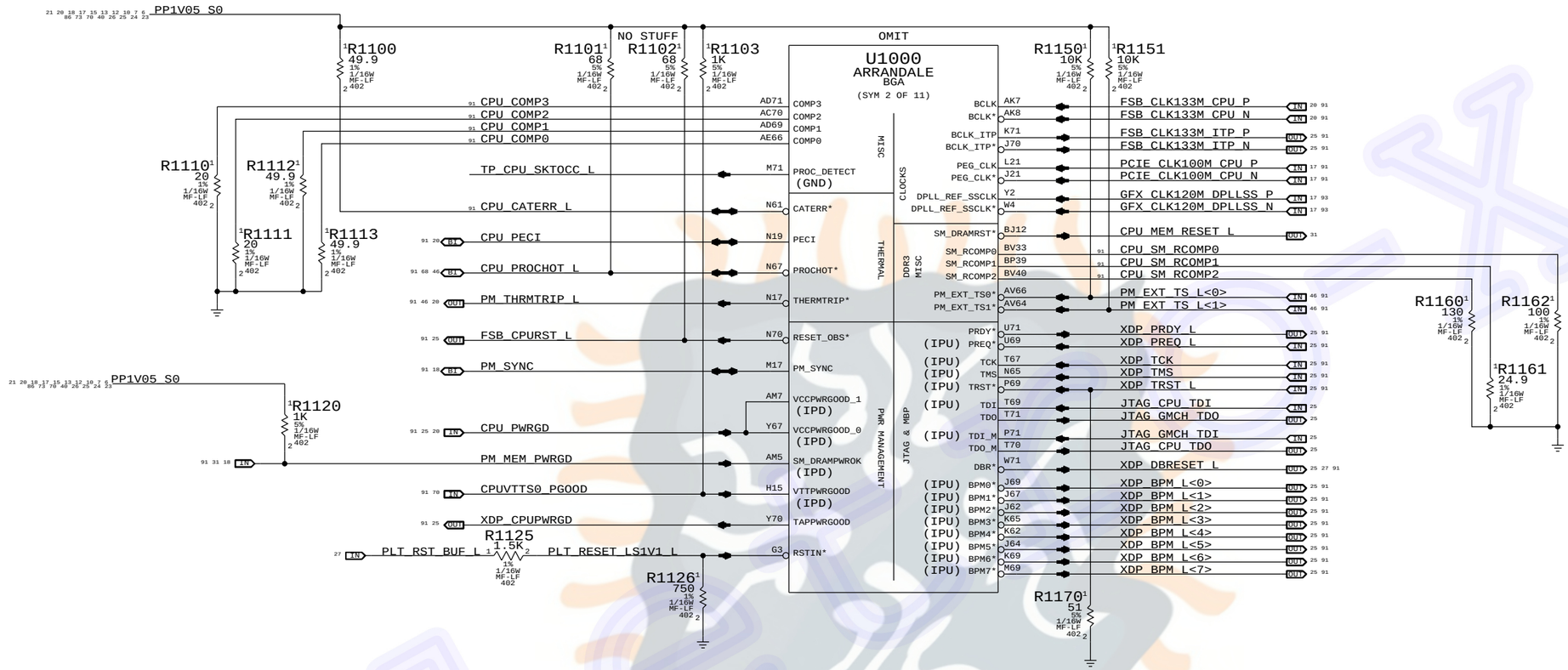

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
CPU Clock/Misc/JTAG

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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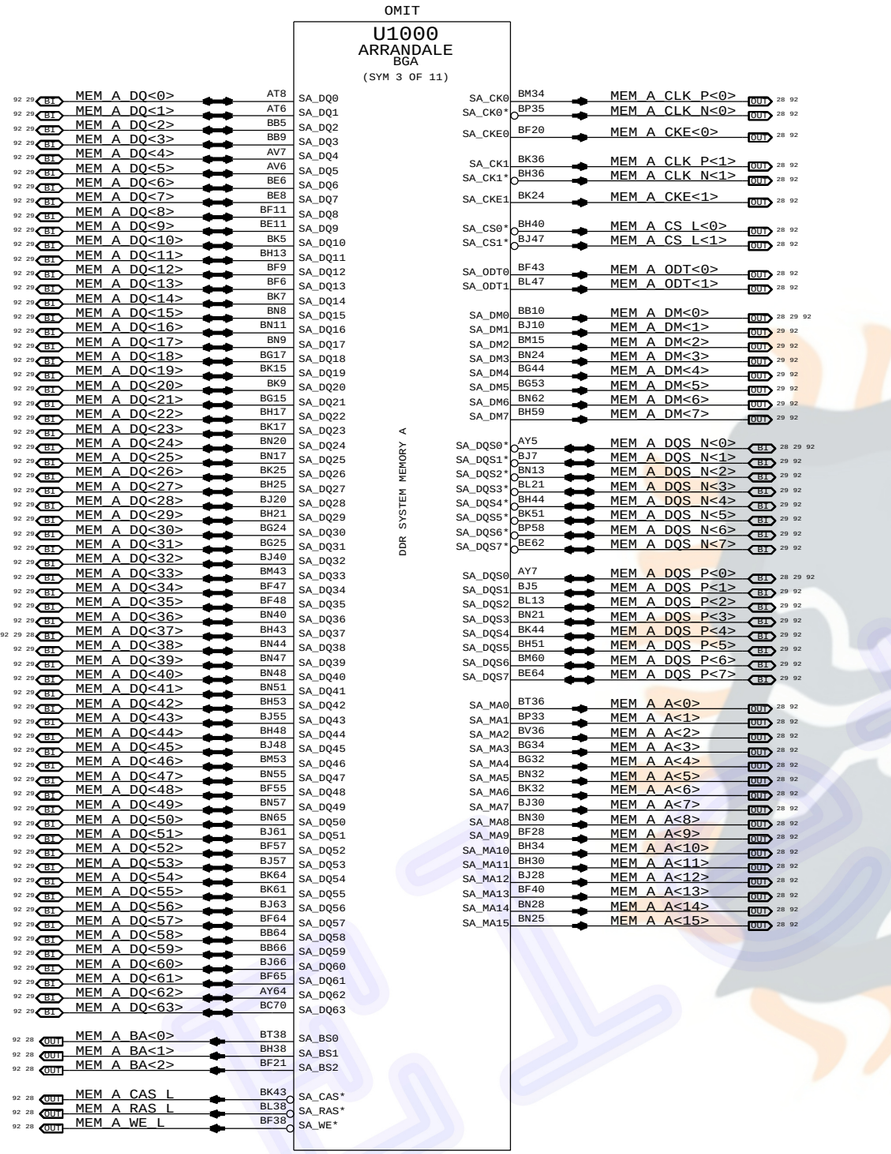

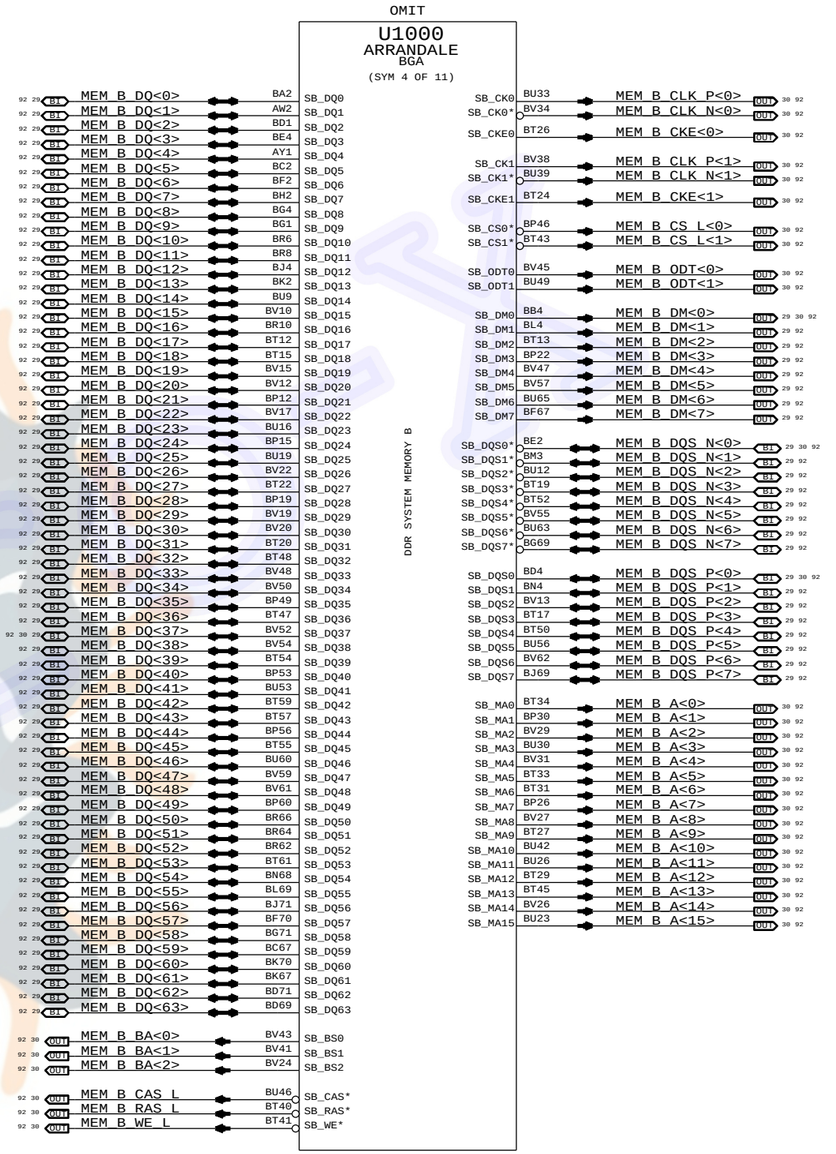

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PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

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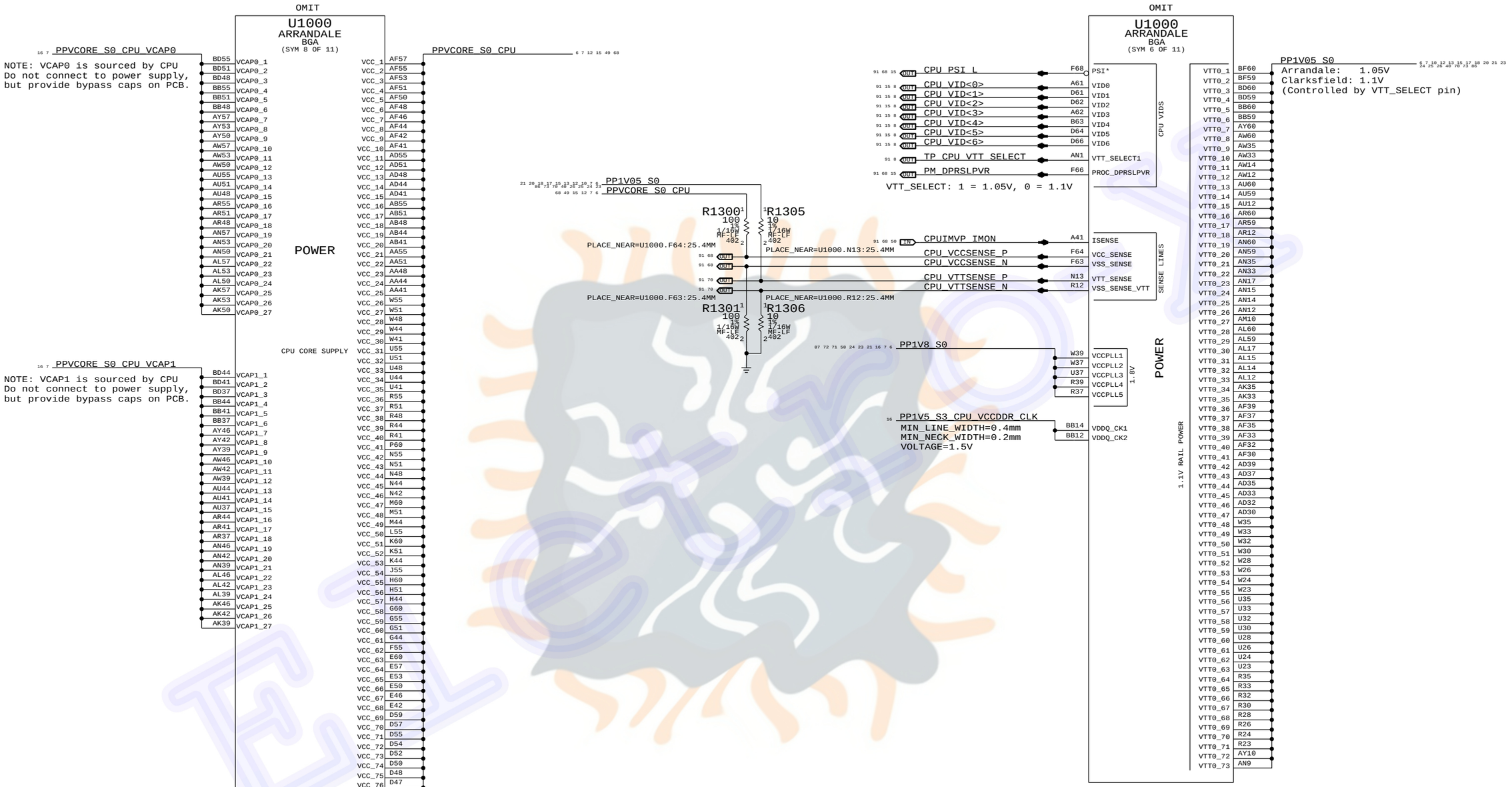

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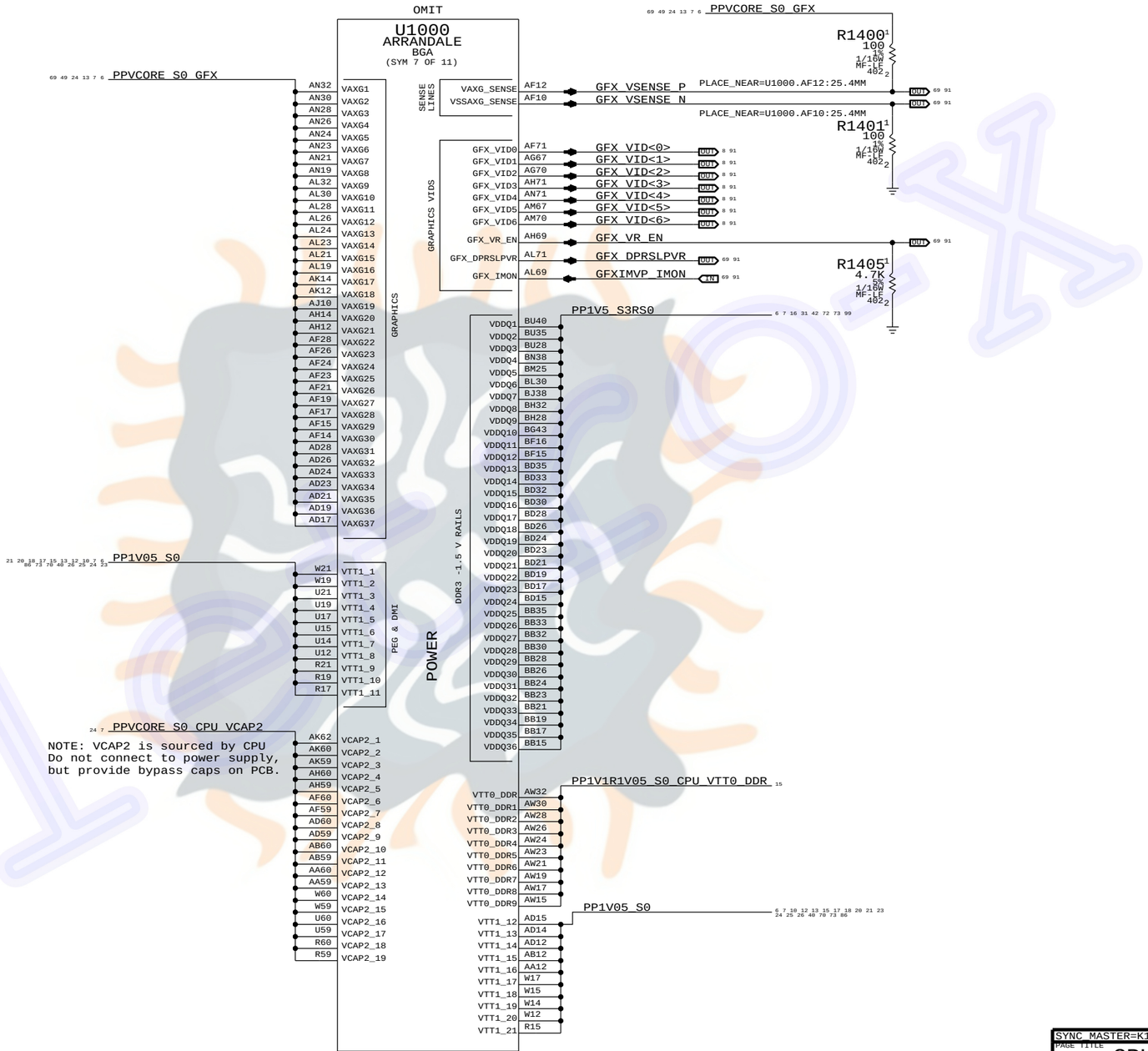

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U1000 ARRANDALE BGA (SYM 9 OF 11)

BU62	VSS1	VSS76	AY62
BU58	VSS2	VSS77	AY59
BU55	VSS3	VSS78	AY55
BU51	VSS4	VSS79	AY51
BU48	VSS5	VSS80	AY48
BU44	VSS6	VSS81	AY44
BU37	VSS7	VSS82	AY41
BU32	VSS8	VSS83	AY37
BU25	VSS9	VSS84	AY35
BU21	VSS10	VSS85	AY33
BU18	VSS11	VSS86	AY32
BU14	VSS12	VSS87	AY30
BU11	VSS13	VSS88	AY28
BU7	VSS14	VSS89	AY26
BP42	VSS15	VSS90	AY24
BN64	VSS16	VSS91	AY23
BN6	VSS17	VSS92	AY21
BM70	VSS18	VSS93	AY19
BM51	VSS19	VSS94	AY17
BM44	VSS20	VSS95	AY15
BM32	VSS21	VSS96	AY14
BM24	VSS22	VSS97	AY12
BM17	VSS23	VSS98	AY8
BL57	VSS24	VSS99	AY4
BL55	VSS25	VSS100	AW67
BL48	VSS26	VSS101	AW62
BL40	VSS27	VSS102	AW59
BL28	VSS28	VSS103	AW55
BL20	VSS29	VSS104	AW51
BK63	VSS30	VSS105	AW48
BK60	VSS31	VSS106	AW44
BK53	VSS32	VSS107	AW41
BK34	VSS33	VSS108	AW37
BK10	VSS34	VSS109	AV9
BJ64	VSS35	VSS110	AV1
BJ21	VSS36	VSS111	AU70
BJ9	VSS37	VSS112	AU62
BJ1	VSS38	VSS113	AU57
BH70	VSS39	VSS114	AU53
BH57	VSS40	VSS115	AU50
BH55	VSS41	VSS116	AU46
BH47	VSS42	VSS117	AU42
BH24	VSS43	VSS118	AU39
BH20	VSS44	VSS119	AU35
BH15	VSS45	VSS120	AU33
BG51	VSS46	VSS121	AU32
BG36	VSS47	VSS122	AU30
BF62	VSS48	VSS123	AU28
BF30	VSS49	VSS124	AU26
BF13	VSS50	VSS125	AU24
BF8	VSS51	VSS126	AU23
BE70	VSS52	VSS127	AU21
BE65	VSS53	VSS128	AU19
BE9	VSS54	VSS129	AU17
BE1	VSS55	VSS130	AU15
BD57	VSS56	VSS131	AU14
BD53	VSS57	VSS132	AU4
BD50	VSS58	VSS133	AT64
BD46	VSS59	VSS134	AT10
BD42	VSS60	VSS135	AR62
BD39	VSS61	VSS136	AR57
BD14	VSS62	VSS137	AR53
BB71	VSS63	VSS138	AR50
BB62	VSS64	VSS139	AR46
BB57	VSS65	VSS140	AR42
BB53	VSS66	VSS141	AR39
BB50	VSS67	VSS142	AR35
BB46	VSS68	VSS143	AR33
BB42	VSS69	VSS144	AR32
BB39	VSS70	VSS145	AR30
BB7	VSS71	VSS146	AR28
BB1	VSS72	VSS147	AR26
BA76	VSS73	VSS148	AR24
AY71	VSS74	VSS149	AR23
AY66	VSS75	VSS150	AR21

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U1000 ARRANDALE BGA (SYM 10 OF 11)

AR19	VSS151	VSS226	BN71
AR17	VSS152	VSS227	E68
AR15	VSS153	VSS228	AH28
AR14	VSS154	VSS229	AH41
AR4	VSS155	VSS230	A66
AR1	VSS156	VSS231	AH26
AP70	VSS157	VSS232	BN1
AP64	VSS158	VSS233	A64
AN62	VSS159	VSS234	AH24
AN55	VSS160	VSS235	AH39
AN51	VSS161	VSS236	E5
AN48	VSS162	VSS237	AH23
AN44	VSS163	VSS238	C68
AN41	VSS164	VSS239	AH21
AN37	VSS165	VSS240	AH19
AN5	VSS166	VSS241	AH17
AN4	VSS167	VSS242	AH15
AM64	VSS168	VSS243	AH4
AM8	VSS169	VSS244	AG64
AL62	VSS170	VSS245	AG9
AL55	VSS171	VSS246	AG6
AL51	VSS172	VSS247	AF69
AL48	VSS173	VSS248	AF62
AL44	VSS174	VSS249	AF1
AL41	VSS175	VSS250	AE70
AL37	VSS176	VSS251	AE64
AL35	VSS177	VSS252	AD62
AL33	VSS178	VSS253	AD57
AL1	VSS179	VSS254	AD53
AK70	VSS180	VSS255	AD50
AK64	VSS181	VSS256	AD46
AK55	VSS182	VSS257	AD42
AK51	VSS183	VSS258	AD4
AK48	VSS184	VSS259	AC67
AK44	VSS185	VSS260	AC64
AK41	VSS186	VSS261	AC10
AK37	VSS187	VSS262	AC5
AK32	VSS188	VSS263	AC1
AK30	VSS189	VSS264	AB70
AK28	VSS190	VSS265	AB62
AK26	VSS191	VSS266	AB57
AK24	VSS192	VSS267	AB53
AK23	VSS193	VSS268	AB50
AK21	VSS194	VSS269	AB46
AK19	VSS195	VSS270	AB42
AK17	VSS196	VSS271	AB39
AK15	VSS197	VSS272	AB37
AJ70	VSS198	VSS273	AB35
AH62	VSS199	VSS274	AB33
AH57	VSS200	VSS275	AB32
AH55	VSS201	VSS276	AB30
AH53	VSS202	VSS277	AB28
BV66	VSS203	VSS278	AB26
AH51	VSS204	VSS279	AB24
BV64	VSS205	VSS280	AB23
AH50	VSS206	VSS281	AB21
BT68	VSS207	VSS282	AB19
AH48	VSS208	VSS283	AB17
BR69	VSS209	VSS284	AB15
BL71	VSS210	VSS285	AB14
AH46	VSS211	VSS286	AB9
BL1	VSS212	VSS287	AA66
AH37	VSS213	VSS288	AA64
BR68	VSS214	VSS289	AA62
R14	VSS215	VSS290	AA57
AH35	VSS216	VSS291	AA53
AH44	VSS217	VSS292	AA50
H71	VSS218	VSS293	AA46
AH33	VSS219	VSS294	AA42
BR3	VSS220	VSS295	AA39
F71	VSS221	VSS296	AA37
AH32	VSS222	VSS297	AA35
AH42	VSS223	VSS298	AA33
E69	VSS224	VSS299	AA32
AH30	VSS225	VSS300	AA30

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U1000 ARRANDALE BGA (SYM 11 OF 11)

AA28	VSS301	VSS367	K6
AA26	VSS302	VSS368	K4
AA24	VSS303	VSS369	J65
AA23	VSS304	VSS370	J57
AA21	VSS305	VSS371	J48
AA19	VSS306	VSS372	J47
AA17	VSS307	VSS373	J40
AA15	VSS308	VSS374	J9
AA14	VSS309	VSS375	H53
AA4	VSS310	VSS376	H43
W69	VSS311	VSS377	H36
W62	VSS312	VSS378	H1
W57	VSS313	VSS379	G70
W53	VSS314	VSS380	G57
W50	VSS315	VSS381	G53
W46	VSS316	VSS382	G48
W42	VSS317	VSS383	G47
W6	VSS318	VSS384	G43
W1	VSS319	VSS385	G30
V70	VSS320	VSS386	G24
U64	VSS321	VSS387	G20
U62	VSS322	VSS388	G15
U57	VSS323	VSS389	F61
U53	VSS324	VSS390	F48
U50	VSS325	VSS391	F47
U46	VSS326	VSS392	F28
U42	VSS327	VSS393	F20
U39	VSS328	VSS394	F4
U9	VSS329	VSS395	E37
U4	VSS330	VSS396	E33
T1	VSS331	VSS397	E30
R70	VSS332	VSS398	E16
R62	VSS333	VSS399	E12
R57	VSS334	VSS400	D41
R53	VSS335	VSS401	D38
R50	VSS336	VSS402	D34
R46	VSS337	VSS403	D31
R42	VSS338	VSS404	D27
R5	VSS339	VSS405	D24
P4	VSS340	VSS406	D20
N63	VSS341	VSS407	D17
N57	VSS342	VSS408	D13
N53	VSS343	VSS409	D10
N50	VSS344	VSS410	D6
N46	VSS345	VSS411	B65
N30	VSS346	VSS412	B62
N21	VSS347	VSS413	B58
N15	VSS348	VSS414	B55
M53	VSS349	VSS415	B51
M42	VSS350	VSS416	B48
M36	VSS351	VSS417	B44
M1	VSS352	VSS418	A59
L70	VSS353	VSS419	A55
L57	VSS354	VSS420	A52
L48	VSS355	VSS421	A48
L47	VSS356	VSS422	A45
L13	VSS357	VSS423	A40
K64	VSS358	VSS424	A36
K53	VSS359	VSS425	A33
K43	VSS360	VSS426	A29
K36	VSS361	VSS427	A26
K34	VSS362	VSS428	A22
K32	VSS363	VSS429	A19
K25	VSS364	VSS430	A15
K17	VSS365	VSS431	A12
K11	VSS366	VSS432	A8
		VSS433	B40

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CPU Grounds

Apple Inc.

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CPU VCore HF and Bulk Decoupling

4x 470uF 4.5mOhm, 3x 62uF B2, 10x 22uF 0603, 25x 1uF 0402

PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C1624):

Place on bottom side of U1000..

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612
1UF 10% 16V X5R 402

C1613 C1614 C1615 C1616 C1617 C1618 C1619 C1620 C1621 C1622 C1623 C1624
1UF 10% 16V X5R 402

PLACEMENT_NOTE (C1625-C1634):

Place near U1000 on bottom side.

NO STUFF C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1634 C1691 C1692 C1693 C1694 C1698
22UF 20% 6.3V X5R-CERM 603

PLACEMENT_NOTE (C1635-C1648):

Place near inductors on bottom side.

NO STUFF C1635 C1636 C1637 C1638 C1640 C1641 C1642 C1643 C1644 C1645 C1646
22UF 20% 6.3V X5R-CERM 603

C1648
22UF 20% 6.3V X5R-CERM 603

C1649 C1650 C1651 C1652
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

NO STUFF C16A0 C16A1 C16A2 C16A3 C16A4
62UF 20% 11V ELEC CASE-B2

CPU Power On Configuration (POC) Straps

Intel recommends all option straps should be provided in layout

PP1V05_S0

R1600 R1602 CPUPOC4U R1604 NO STUFF R1606 NO STUFF R1608
1K 5% 1/16W MF-LF 402

R1601 CPUPOC3U R1603 CPUPOC5U R1605 R1607
1K 5% 1/16W MF-LF 402

CPU_VID<0>
CPU_VID<1>
CPU_VID<2>
CPU_VID<3>
CPU_VID<4>
CPU_VID<5>
CPU_VID<6>
PM_DPRSLPVR
CPU_PSI_L

NO STUFF R1610 NO STUFF R1612 CPUPOC4D R1614 R1616 R1618
1K 5% 1/16W MF-LF 402

NO STUFF R1611 CPUPOC3D R1613 CPUPOC5D R1615 NO STUFF R1617
1K 5% 1/16W MF-LF 402

VID[2:0] = Reserved (111)
VID[5:3] = GPU Gain Setting (See below)
VID[6] = Reserved (0)
DPRSLPVR = 1 - IMVP-6.5 compliant controller
PSI# = Reserved (0)

BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPOC_IMAX_DIS		000	CPUPOC3D,CPUPOC4D,CPUPOC5D	
CPUPOC_IMAX_0_20	20A	001	CPUPOC3D,CPUPOC4D,CPUPOC5U	45
CPUPOC_IMAX_20_30	30A	010	CPUPOC3D,CPUPOC4U,CPUPOC5D	30
CPUPOC_IMAX_30_40	40A	011	CPUPOC3D,CPUPOC4U,CPUPOC5U	22.5
CPUPOC_IMAX_40_50	50A	100	CPUPOC3U,CPUPOC4D,CPUPOC5D	18
CPUPOC_IMAX_50_60	60A	101	CPUPOC3U,CPUPOC4D,CPUPOC5U	15
CPUPOC_IMAX_60_70	70A	110	CPUPOC3U,CPUPOC4U,CPUPOC5D	12.857
CPUPOC_IMAX_70_90	90A	111	CPUPOC3U,CPUPOC4U,CPUPOC5U	10

NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONs directly. Instead call out appropriate BOM GROUP defined in tables above.

VTT (CPU Uncore) DECOUPLING

3x 330uF 6 mOhm, 4x 22uF 0805, 7x 10uF 0603, 24x 1uF 0402

PP1V05_S0

PLACEMENT_NOTE (C1653-C1656):

Place on bottom side of U1000.

C1653 C1654 C1655 C1656
22UF 20% 6.3V X5R-CERM 603

PLACEMENT_NOTE (C1657-C1663):

Place on bottom side of U1000..

C1657 C1658 C1659 C1660 C1661 C1662 C1663
10UF 20% 6.3V X5R 603

PLACEMENT_NOTE (C1664-C1687):

Place on bottom side of U1000.

C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671 C1672 C1673 C1674 C1675
1UF 10% 16V X5R 402

C1676 C1677 C1678 C1679 C1680 C1681 C1682 C1683 C1684 C1685 C1686 C1687
1UF 10% 16V X5R 402

C1688 C1689 C1690
330UF 20% 2.0V POLY-TANT D2T-SM2

VTT0_DDR DECOUPLING

3x 1uF 0402

L1695
30-OHM-5A
0603

PLACEMENT_NOTE (C1695-C1697):

Place on bottom side of U1000.

PP1V1R1V05_S0_CPU_VTT0_DDR
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V

C1695 C1696 C1697
1UF 10% 16V X5R 402

Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form Factor Schematic Check List Rev 1.1 (doc #395914) table 3.26.

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PAGE TITLE: CPU Non-GFX Decoupling (1 of 2)

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VCAP0 (CPU BSC Package) DECOUPLING

12x 1uF 0402

PLACEMENT_NOTE (C1700-C1711):

Place on bottom side of U1000.

PPVCORE_S0_CPU_VCAP0

C1700 C1701 C1702 C1703 C1704 C1705 C1706 C1707 C1708 C1709 C1710 C1711
1UF 20% 10V X5R 402

VCAP1 (CPU BSC Package) DECOUPLING

12x 1uF 0402

PLACEMENT_NOTE (C1712-C1723):

Place on bottom side of U1000.

PPVCORE_S0_CPU_VCAP1

C1712 C1713 C1714 C1715 C1716 C1717 C1718 C1719 C1720 C1721 C1722 C1723
1UF 20% 10V X5R 402

Memory (CPU VCCDDR) DECOUPLING

5x 1uF 0402

NOTE: 3x 330uF 6 mOhm caps to be shared between CPU and SO-DIMMs. DG recommends 2x 22uF at SO_DIMM not provided. Decoupling caps at SO-DIMMs on CSA 29 and CSA 31.

PP1V5_S3RS0

C1724 C1725 C1726 C1727 C1728
1UF 20% 10V X5R 402

NOTE: 19x 1uF 0402 caps per Apple SI for CMD and CNTRL lines.

C1735 C1736 C1737 C1738 C1739 C1740 C1741 C1742 C1743 C1744 C1745 C1746 C1747 C1748 C1749 C1750 C1751 C1752 C1753
1UF 20% 10V X5R 402

C1729
330UF 20% 2.0V POLY-TANT D2T-SM2

PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603

PP1V8_S0

C1732 22UF 20% 6.3V CERM-X5R 805
C1733 4.7UF 10% 6.3V X6S-CERM 603

DDR Clock (CPU VDDQ_CK) DECOUPLING

1x 1uF 0402

PP1V5_S3RS0 — L1734 30-OHM-5A 0603 — PP1V5_S3_CPU_VCCDDR_CLK

C1734 1UF 10% 10V X5R 402

Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form F
actor Schematic Check List Rev 1.1 (doc #395914) table 3.26.

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

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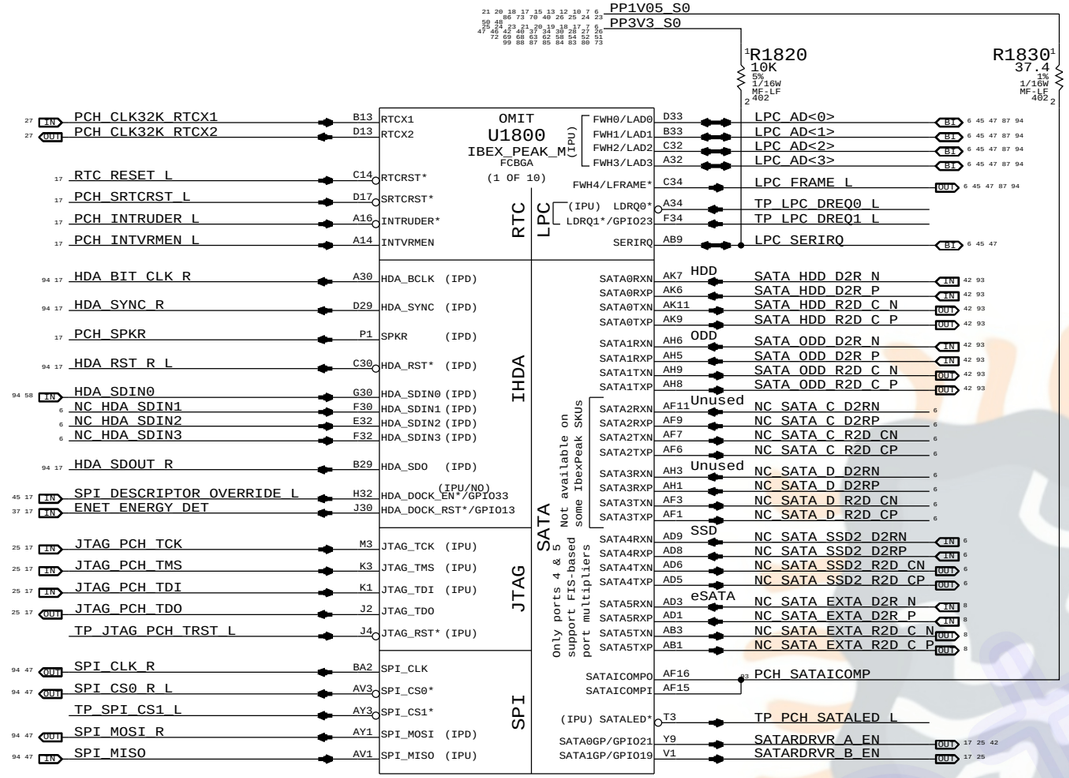

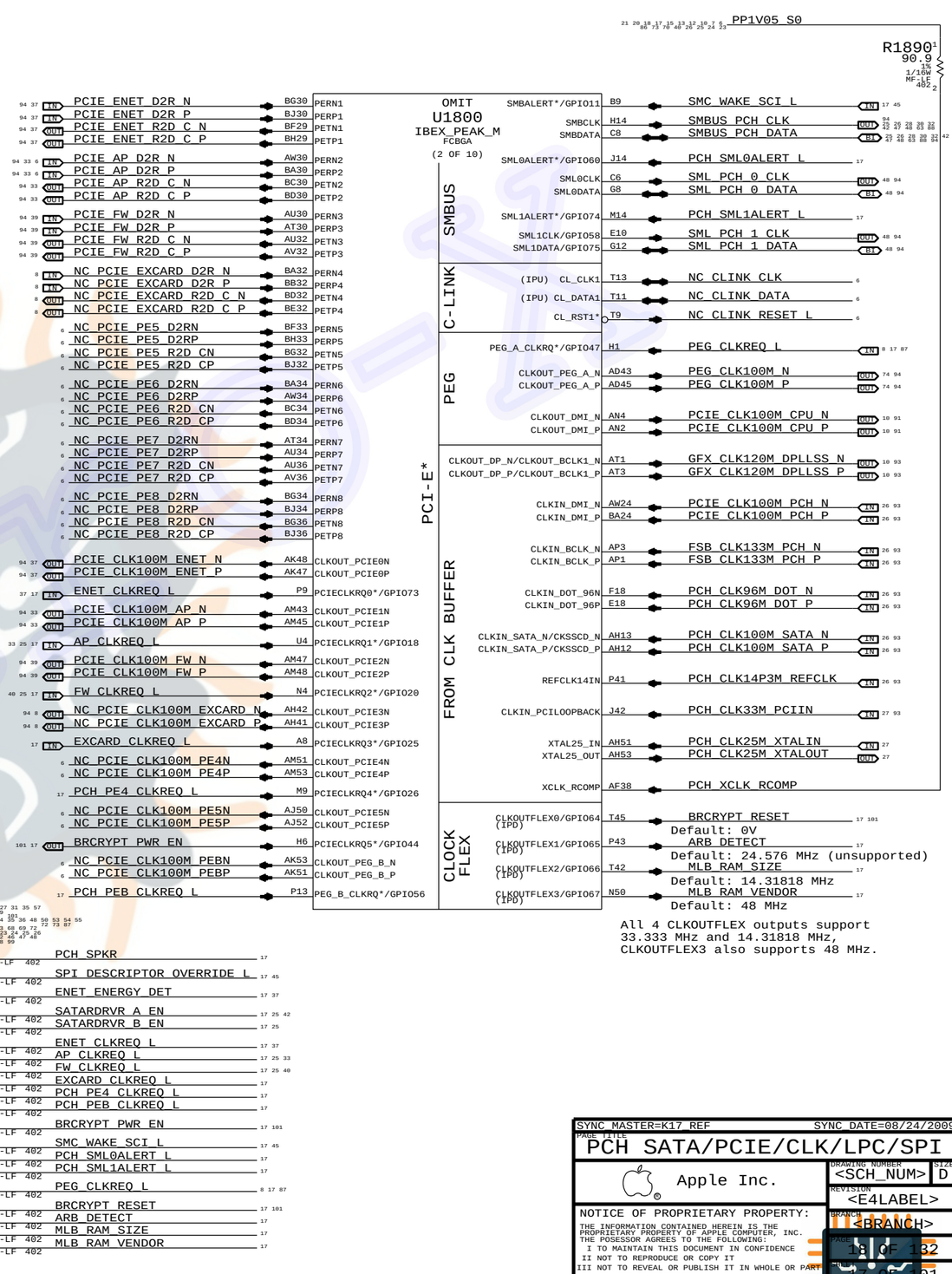

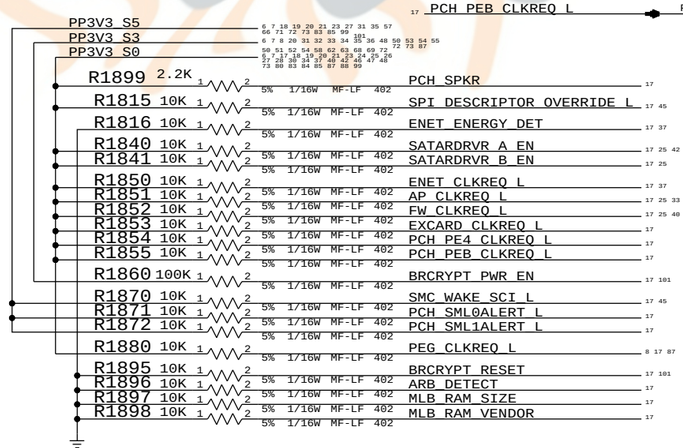

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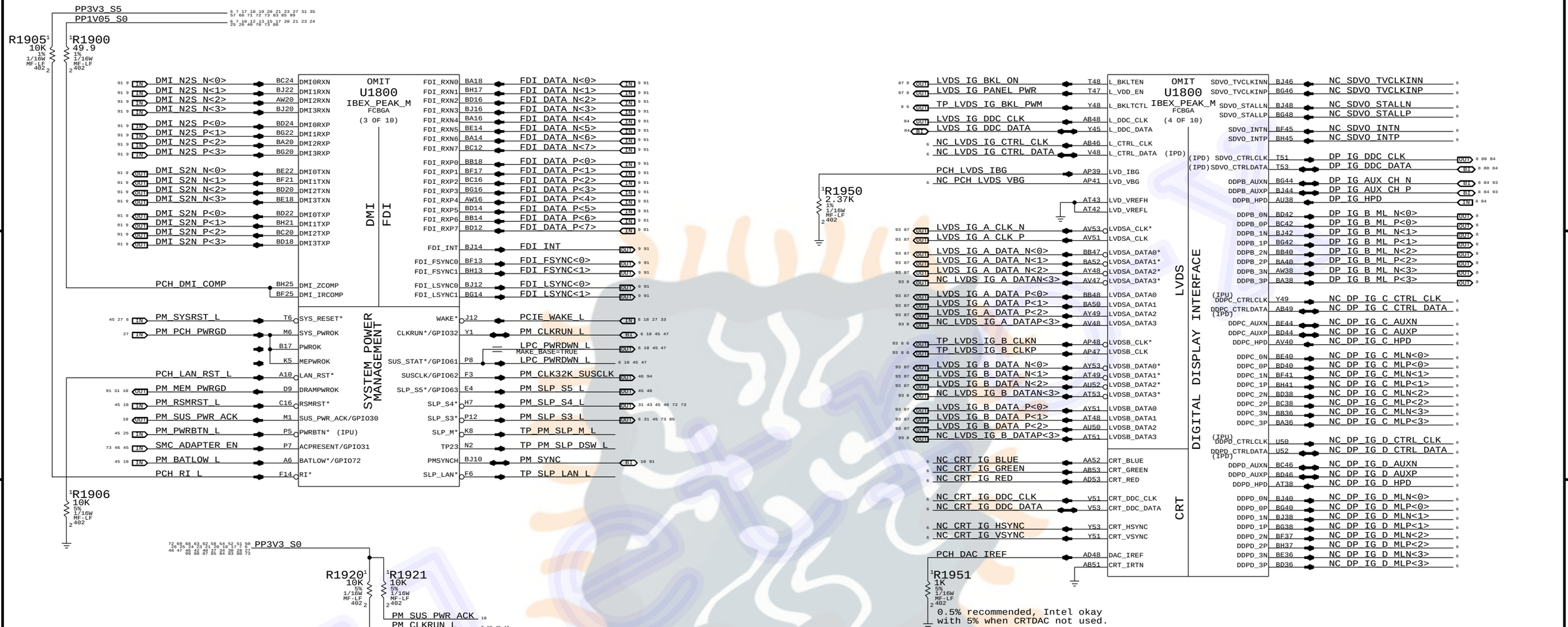

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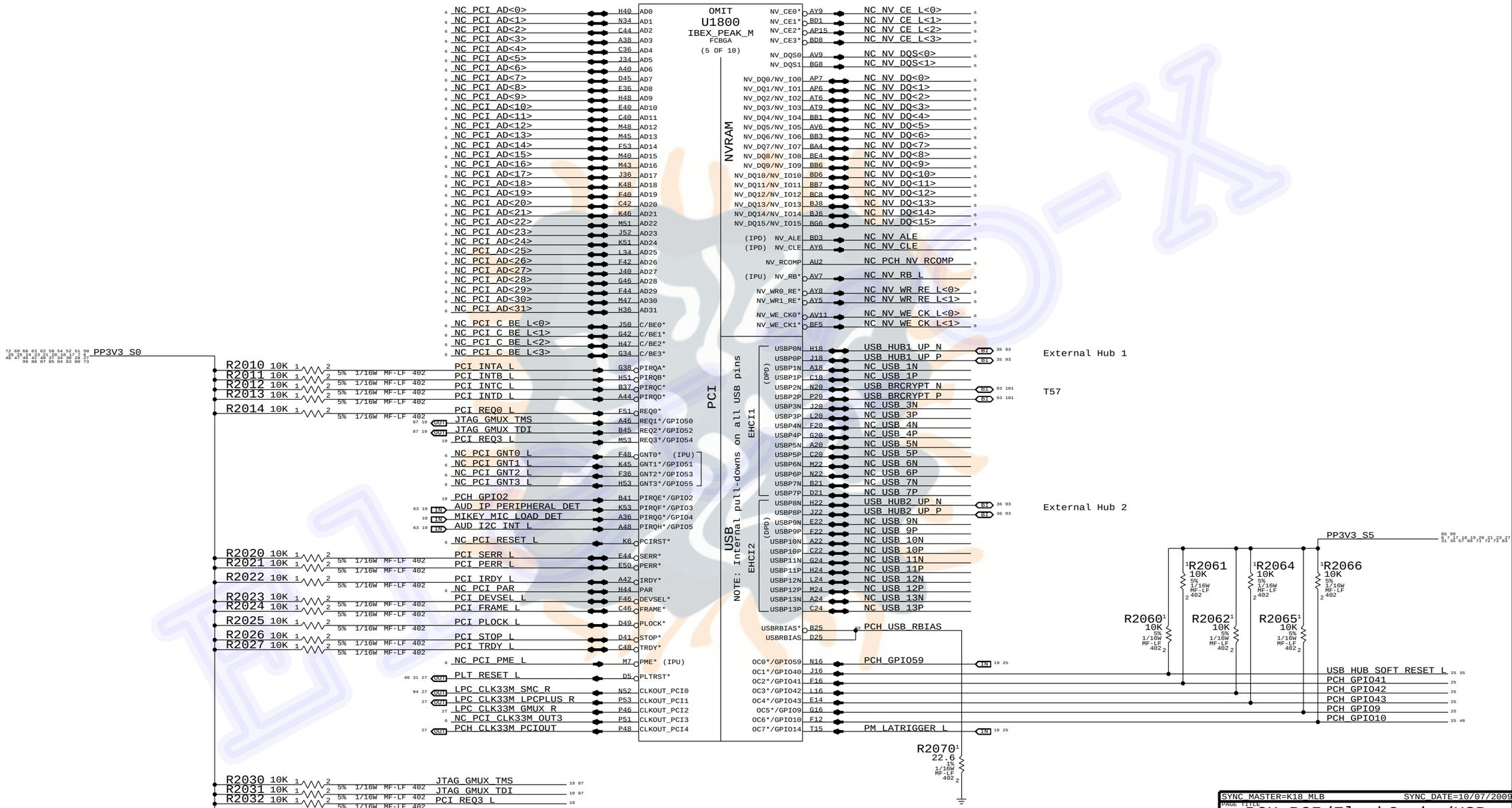
OMIT
U1800
IBEX_PEAK_M
FCBGA
(5 OF 10)
PCI
NVRAM
USB
NOTE: Internal pull-downs on all USB pins
EHCI1
EHCI2
(DPD)
NC_PCI_AD<0>
NC_PCI_AD<1>
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NC_PCI_AD<3>
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PCI_INTA_L
PCI_INTB_L
PCI_INTC_L
PCI_INTD_L
PCI_REQ0_L
JTAG_GMUX_TMS
JTAG_GMUX_TDI
PCI_REQ3_L
NC_PCI_GNT0_L
NC_PCI_GNT1_L
NC_PCI_GNT2_L
NC_PCI_GNT3_L
PCH_GPIO2
AUD_IP_PERIPHERAL_DET
MIKEY_MIC_LOAD_DET
AUD_I2C_INT_L
NC_PCI_RESET_L
PCI_SERR_L
PCI_PERR_L
PCI_IRDY_L
NC_PCI_PAR
PCI_DEVSEL_L
PCI_FRAME_L
PCI_PLOCK_L
PCI_STOP_L
PCI_TRDY_L
NC_PCI_PME_L
PLT_RESET_L
LPC_CLK33M_SMC_R
LPC_CLK33M_LPCPLUS_R
LPC_CLK33M_GMUX_R
NC_PCI_CLK33M_OUT3
PCH_CLK33M_PCIOUT
NV_CE0*
NV_CE1*
NV_CE2*
NV_CE3*
NV_DQS0
NV_DQS1
NV_DQ0/NV_IO0
NV_DQ1/NV_IO1
NV_DQ2/NV_IO2
NV_DQ3/NV_IO3
NV_DQ4/NV_IO4
NV_DQ5/NV_IO5
NV_DQ6/NV_IO6
NV_DQ7/NV_IO7
NV_DQ8/NV_IO8
NV_DQ9/NV_IO9
NV_DQ10/NV_IO10
NV_DQ11/NV_IO11
NV_DQ12/NV_IO12
NV_DQ13/NV_IO13
NV_DQ14/NV_IO14
NV_DQ15/NV_IO15
(IPD) NV_ALE
(IPD) NV_CLE
NV_RCOMP
(IPU) NV_RB*
NV_WR0_RE*
NV_WR1_RE*
NV_WE_CK0*
NV_WE_CK1*
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USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P
USBP12N
USBP12P
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USBP13P
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NC_USB_1P
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USB_BRCRYPT_P
NC_USB_3N
NC_USB_3P
NC_USB_4N
NC_USB_4P
NC_USB_5N
NC_USB_5P
NC_USB_6N
NC_USB_6P
NC_USB_7N
NC_USB_7P
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NC_USB_10N
NC_USB_10P
NC_USB_11N
NC_USB_11P
NC_USB_12N
NC_USB_12P
NC_USB_13N
NC_USB_13P
PCH_USB_RBIAS
External Hub 1
External Hub 2
T57
PP3V3_S0
PP3V3_S5
R2010 10K
R2011 10K
R2012 10K
R2013 10K
R2014 10K
R2020 10K
R2021 10K
R2022 10K
R2023 10K
R2024 10K
R2025 10K
R2026 10K
R2027 10K
R2030 10K
R2031 10K
R2032 10K
R2035 10K
R2036 10K
R2037 10K
R2038 10K
R2080 10K
R2081 10K
R2060 10K
R2061 10K
R2062 10K
R2064 10K
R2065 10K
R2066 10K
R2070 22.6
5% 1/16W MF-LF 402
1%
PCH_GPIO59
PM_LATRIGGER_L
PCH_GPIO41
PCH_GPIO42
PCH_GPIO43
PCH_GPIO9
PCH_GPIO10
USB_HUB_SOFT_RESET_L
SYNC_MASTER=K18_MLB
SYNC_DATE=10/07/2009
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PCH PCI/FlashCache/USB
Apple Inc.
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<SCH_NUM>
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<E4LABEL>
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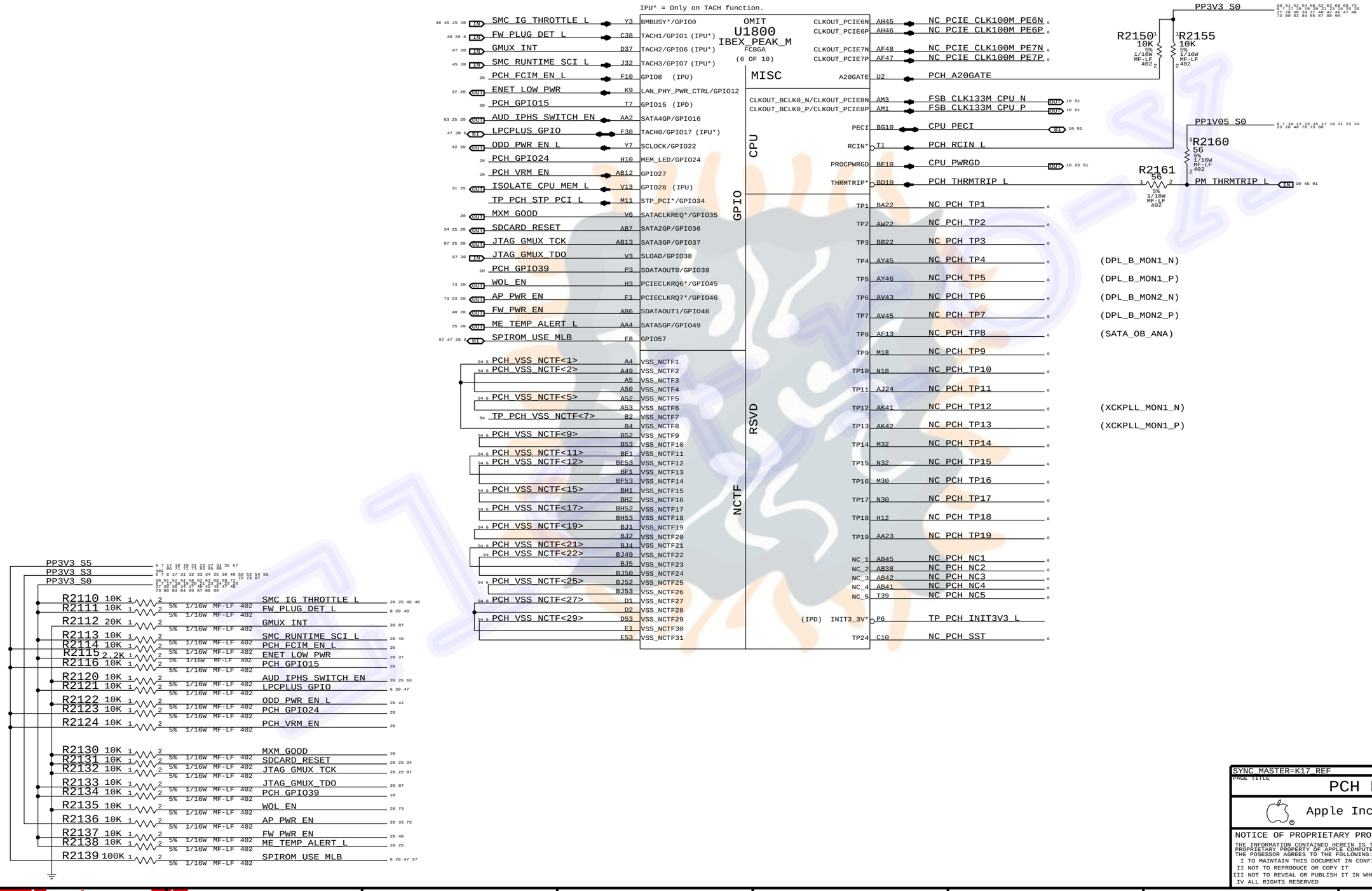

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Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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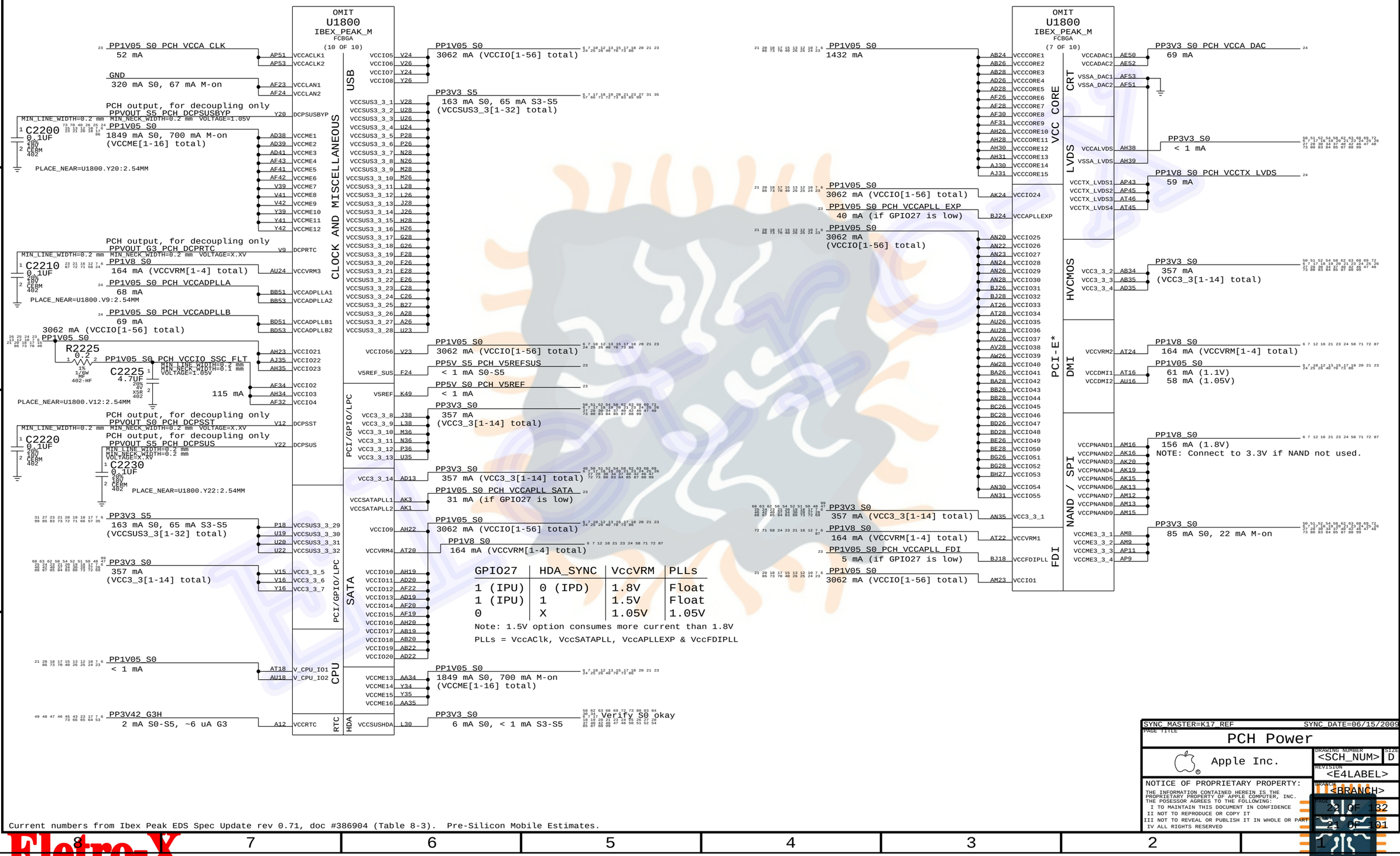
	SHEET 20 OF 101


OMIT
U1800
IBEX_PEAK_M
FCBGA
(10 OF 10)
PP1V05_S0_PCH_VCCA_CLK
52 mA
GND
320 mA S0, 67 mA M-on
PCH output, for decoupling only
PPVOUT_S5_PCH_DCPSUSBYP
MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.05V
PP1V05_S0
1849 mA S0, 700 mA M-on
(VCCME[1-16] total)
C2200
0.1UF
PLACE_NEAR=U1800.Y20:2.54MM
PCH output, for decoupling only
PPVOUT_G3_PCH_DCPRTC
MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=X.XV
PP1V8_S0
164 mA (VCCVRM[1-4] total)
C2210
0.1UF
PLACE_NEAR=U1800.V9:2.54MM
PP1V05_S0_PCH_VCCADPLLA
68 mA
PP1V05_S0_PCH_VCCADPLLB
69 mA
3062 mA (VCCIO[1-56] total)
PP1V05_S0
R2225
0.2
1% 1/8W MF 402-HF
PP1V05_S0_PCH_VCCIO_SSC_FLT
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.05V
C2225
4.7UF
20% 4V X5R 402
115 mA
PLACE_NEAR=U1800.V12:2.54MM
PCH output, for decoupling only
PPVOUT_S0_PCH_DCPSST
MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=X.XV
C2220
0.1UF
PCH output, for decoupling only
PPVOUT_S5_PCH_DCPSUS
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=X.XV
C2230
0.1UF
PLACE_NEAR=U1800.Y22:2.54MM
PP3V3_S5
163 mA S0, 65 mA S3-S5
(VCCSUS3_3[1-32] total)
PP3V3_S0
357 mA
(VCC3_3[1-14] total)
PP1V05_S0
< 1 mA
PP3V42_G3H
2 mA S0-S5, ~6 uA G3
CLOCK AND MISCELLANEOUS
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
PP1V05_S0
3062 mA (VCCIO[1-56] total)
PP5V_S5_PCH_V5REFSUS
< 1 mA S0-S5
PP5V_S0_PCH_V5REF
< 1 mA
PP3V3_S0
357 mA
(VCC3_3[1-14] total)
PP3V3_S0
357 mA (VCC3_3[1-14] total)
PP1V05_S0_PCH_VCCAPLL_SATA
31 mA (if GPIO27 is low)
PP1V05_S0
3062 mA (VCCIO[1-56] total)
PP1V8_S0
164 mA (VCCVRM[1-4] total)
PP1V05_S0
3062 mA (VCCIO[1-56] total)
PP1V05_S0
1849 mA S0, 700 mA M-on
(VCCME[1-16] total)
PP3V3_S0
6 mA S0, < 1 mA S3-S5
Verify S0 okay
GPIO27 | HDA_SYNC | VccVRM | PLLs
1 (IPU) | 0 (IPD) | 1.8V | Float
1 (IPU) | 1 | 1.5V | Float
0 | X | 1.05V | 1.05V
Note: 1.5V option consumes more current than 1.8V
PLLs = VccAClk, VccSATAPLL, VccAPLLEXP & VccFDIPLL
OMIT
U1800
IBEX_PEAK_M
FCBGA
(7 OF 10)
PP1V05_S0
1432 mA
PP1V05_S0
3062 mA (VCCIO[1-56] total)
PP1V05_S0_PCH_VCCAPLL_EXP
40 mA (if GPIO27 is low)
PP1V05_S0
3062 mA
(VCCIO[1-56] total)
PP3V3_S0
357 mA (VCC3_3[1-14] total)
PP1V8_S0
164 mA (VCCVRM[1-4] total)
PP1V05_S0_PCH_VCCAPLL_FDI
5 mA (if GPIO27 is low)
PP1V05_S0
3062 mA (VCCIO[1-56] total)
VCC CORE
LVDS
CRT
HVCMOS
PCI-E*
DMI
NAND / SPI
FDI
PP3V3_S0_PCH_VCCA_DAC
69 mA
PP3V3_S0
< 1 mA
PP1V8_S0_PCH_VCCTX_LVDS
59 mA
PP3V3_S0
357 mA
(VCC3_3[1-14] total)
PP1V8_S0
164 mA (VCCVRM[1-4] total)
PP1V05_S0
61 mA (1.1V)
58 mA (1.05V)
PP1V8_S0
156 mA (1.8V)
NOTE: Connect to 3.3V if NAND not used.
PP3V3_S0
85 mA S0, 22 mA M-on
SYNC_MASTER=K17_REF
SYNC_DATE=06/15/2009
PAGE TITLE
PCH Power
Apple Inc.
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<SCH_NUM>
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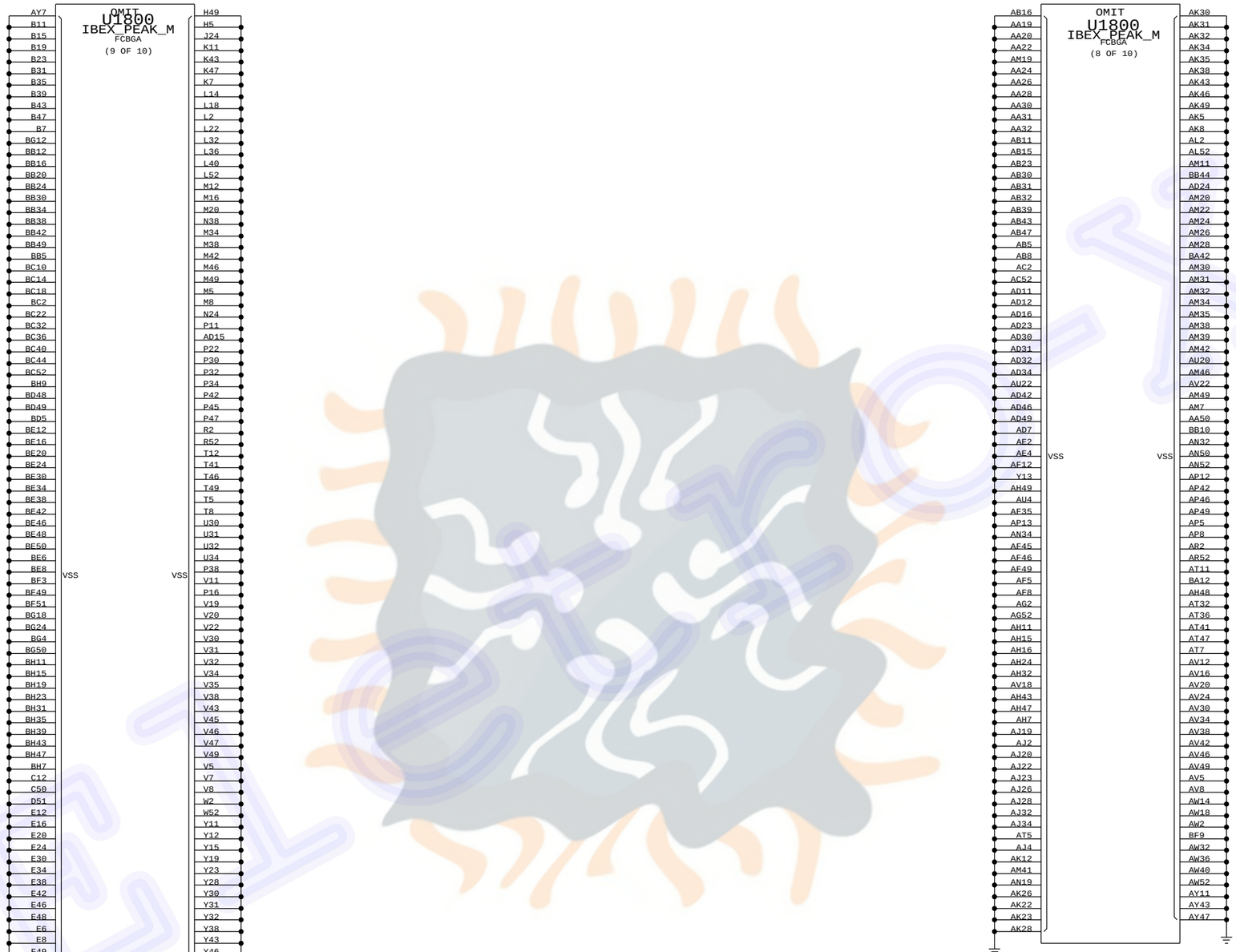
Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.



SYNC_MASTER=K17 REF SYNC_DATE=06/15/2009

PAGE TITLE

PCH Grounds

Apple Inc.

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PP3V3_S5
PP5V_S5
1 mA S0-S5

PCH V5REF_SUS Filter & Follower
(PCH Reference for 5V Tolerance on USB)

R2400 10 5% 1/16W MF-LF 402
D2400 BAT54DW-X-G SOT-363
PP5V_S5_PCH_V5REFSUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM 1 mA S0-S5
VOLTAGE=5V
C2400 1UF 10% 10V X5R 402
PLACE_NEAR=U1800.F24:2.54MM

PP3V3_S0
PP5V_S0
1 mA

PCH V5REF Filter & Follower
(PCH Reference for 5V Tolerance on PCI)

R2401 100 5% 1/16W MF-LF 402
D2400 BAT54DW-X-G SOT-363
PP5V_S0_PCH_V5REF
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM 1 mA
VOLTAGE=5V
C2401 1UF 10% 10V X5R 402
PLACE_NEAR=U1800.K49:2.54MM

PCH VCCRTC BYPASS
(PCH RTC 3.3V PWR)
PP3V42_G3H
2 mA S0-S5 /
6 uA G3
C2420 1UF 10% 6.3V X5R 402
C2421 0.1UF 10% 10V X5R 402
C2422 0.1UF 10% 10V X5R 402
PLACE_NEAR=U1800.A12:2.54MM

PCH VCCSUS3_3 BYPASS
(PCH SUSPEND PCI 3.3V PWR)
PP3V3_S5
C2425 0.1UF 10% 10V X5R 402
PLACE_NEAR=U1800.P18:2.54MM

163 mA S0 /
65 mA S3-S5
(VCCSUS3_3 Total)

PCH USB/VCCSUS3_3 BYPASS
(PCH SUSPEND USB 3.3V PWR)
PP3V3_S5
C2426 0.1UF 10% 10V X5R 402
C2427 0.1UF 10% 10V X5R 402
PLACE_NEAR=U1800.A26:2.54MM
PLACE_NEAR=U1800.U23:2.54MM

PCH VCCME3_3 BYPASS
(PCH ME 3.3V PWR)
PP3V3_S0
C2430 0.1UF 10% 10V X5R 402
PLACE_NEAR=U1800.AM8:2.54MM

PCH CORE/VCC3_3 BYPASS
(PCH MISC 3.3V PWR)
PP3V3_S0
C2435 0.1UF 10% 10V X5R 402
PLACE_NEAR=U1800.V15:2.54MM

PCH VCCAPLLEXP Filter
(PCH PCIe PLL PWR)
PP1V05_S0_PCH_VCCAPLL_EXP
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
C2413 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.BJ24:2.54MM
OMIT_WF: C2311 not in DG or CRB

PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)
PP3V3_S0
C2436 0.1UF 10% 10V X5R 402
PLACE_NEAR=U1800.J38:2.54MM

PCH VCCFDIPLL Filter
(PCH FDI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_FDI
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
C2415 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.BJ18:2.54MM
OMIT_WF: C2413 not in DG or CRB

PCH VCC3_3 BYPASS
(PCH SATA 3.3V PWR)
PP3V3_S0
C2437 0.1UF 10% 10V X5R 402
PLACE_NEAR=U1800.AD13:2.54MM

PCH VCCSATAPLL Filter
(PCH SATA PLL PWR)
PP1V05_S0_PCH_VCCAPLL_SATA
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
C2417 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AK1:2.54MM
BB: C2417 removed from DG
NO STUFF

PCH VCC3_3 BYPASS
(PCH PCIe/DMI 3.3V PWR)
PP3V3_S0
C2438 0.1UF 10% 10V X5R 402
PLACE_NEAR=U1800.AN35:2.54MM

PCH VCCACLK Filter
(PCH Misc PLL PWR)
PP1V05_S0_PCH_VCCA_CLK
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
C2419 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AP51:2.54MM
BB: C2419 removed from DG
NO STUFF

PCH VCC3_3 BYPASS
(PCH CLK/HVCMOS 3.3V PWR)
PP3V3_S0
C2439 0.1UF 10% 10V X5R 402
PLACE_NEAR=U1800.AB34:2.54MM

PCH VCCPNAND BYPASS
(PCH NAND 1.8V/3.3V PWR)
PP1V8_S0
C2440 0.1UF 10% 10V X5R 402
PLACE_NEAR=U1800.AK13:2.54MM

PCH VCCSUSHDA BYPASS
(PCH HD Audio 3.3V/1.5V PWR)
PP3V3_S0
C2445 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.L30:2.54MM

PCH V_CPU_IO BYPASS
(PCH 1.1V/1.05V CPU I/O PWR)
PP1V05_S0
C2450 4.7UF 20% 6.3V X5R 603
C2451 0.1UF 10% 10V X5R 402
C2452 0.1UF 10% 10V X5R 402
PLACE_NEAR=U1800.AT18:2.54MM
PLACE_NEAR=U1800.AT18:2.54MM
PLACE_NEAR=U1800.AT18:2.54MM

PCH VCCIO BYPASS
(PCH DMI 1.05V PWR)
PP1V05_S0
C2455 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AT16:2.54MM

PCH VCCLAN BYPASS
(PCH 1.05V LAN Core PWR)
GND
NO STUFF
C2460 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AF23:2.54MM

PCH VCCME BYPASS
(PCH 1.05V ME Core PWR)
PP1V05_S0
C2465 22UF 20% 6.3V X5R-CERM 603
C2466 22UF 20% 6.3V X5R-CERM 603
C2467 22UF 20% 6.3V X5R-CERM 603
C2468 1UF 10% 6.3V CERM 402
C2469 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AD38:2.54MM
PLACE_NEAR=U1800.V39:2.54MM
PLACE_NEAR=U1800.AD38:2.54MM
PLACE_NEAR=U1800.AD38:2.54MM
PLACE_NEAR=U1800.V39:2.54MM

PCH VCCCORE BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C2470 10UF 20% 6.3V X5R 603
C2471 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AB24:2.54MM
PLACE_NEAR=U1800.AB24:2.54MM

PCH VCCIO BYPASS
(PCH CLK 1.05V PWR)
PP1V05_S0
C2475 1UF 10% 6.3V CERM 402
C2476 1UF 10% 6.3V CERM 402
C2477 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AF32:2.54MM
PLACE_NEAR=U1800.AH23:2.54MM
PLACE_NEAR=U1800.AH35:2.54MM

PCH VCCIO BYPASS
(PCH USB 1.05V PWR)
PP1V05_S0
C2480 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.V24:2.54MM

PCH VCCIO BYPASS
(PCH SATA 1.05V PWR)
PP1V05_S0
C2485 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AB19:2.54MM

PCH VCCIO BYPASS
(PCH PCIE 1.05V PWR)
PP1V05_S0
C2490 10UF 20% 6.3V X5R 603
C2491 1UF 10% 6.3V CERM 402
C2492 1UF 10% 6.3V CERM 402
C2493 1UF 10% 6.3V CERM 402
C2494 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AN20:2.54MM
PLACE_NEAR=U1800.AN20:2.54MM
PLACE_NEAR=U1800.AN20:2.54MM
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Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
PCH Non-GFX Decoupling

Apple Inc.

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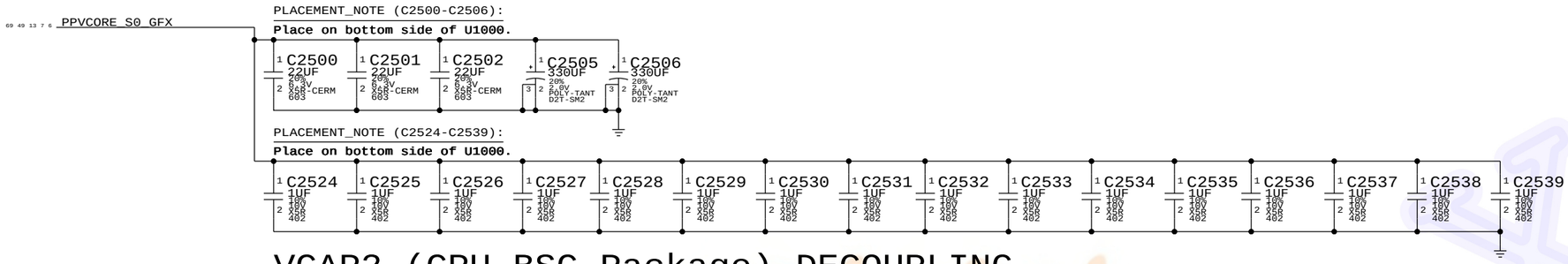
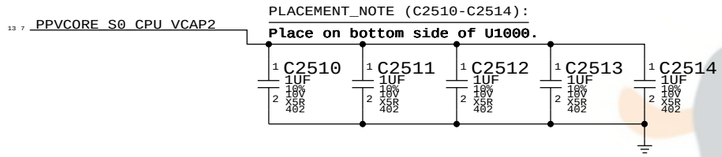
GFX (CPU VCCAXG) DECOUPLING

3x 330uF 6 mOhm (2 stuffed), 3x 22uF 0603, 16x 1uF 0402

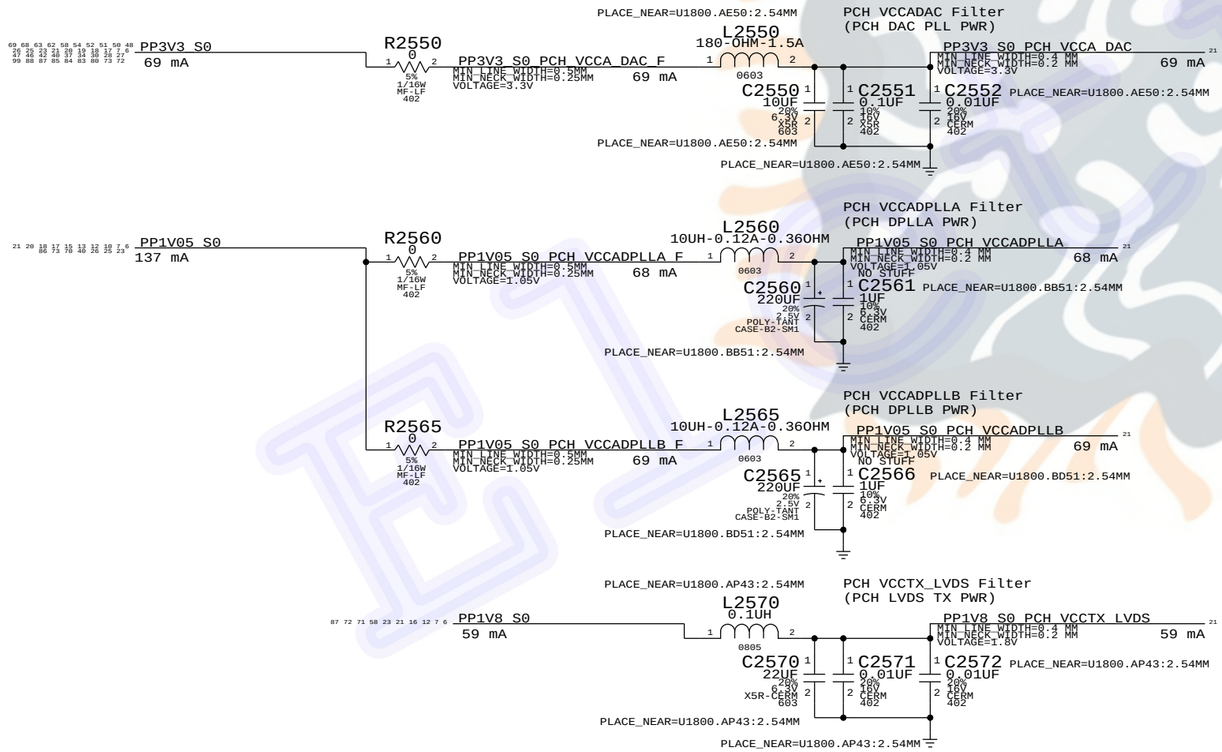


VCAP2 (CPU BSC Package) DECOUPLING

5x 1uF 0402



Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form F actor Schematic Check List Rev 1.1 (doc #395914) table 3.26.



Design recommendations from Calpella Design Guide Rev 1.5 (doc #398905) Section 3.25.3 tables 161 and 162.

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

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CPU/PCH GFX Decoupling

Apple Inc.

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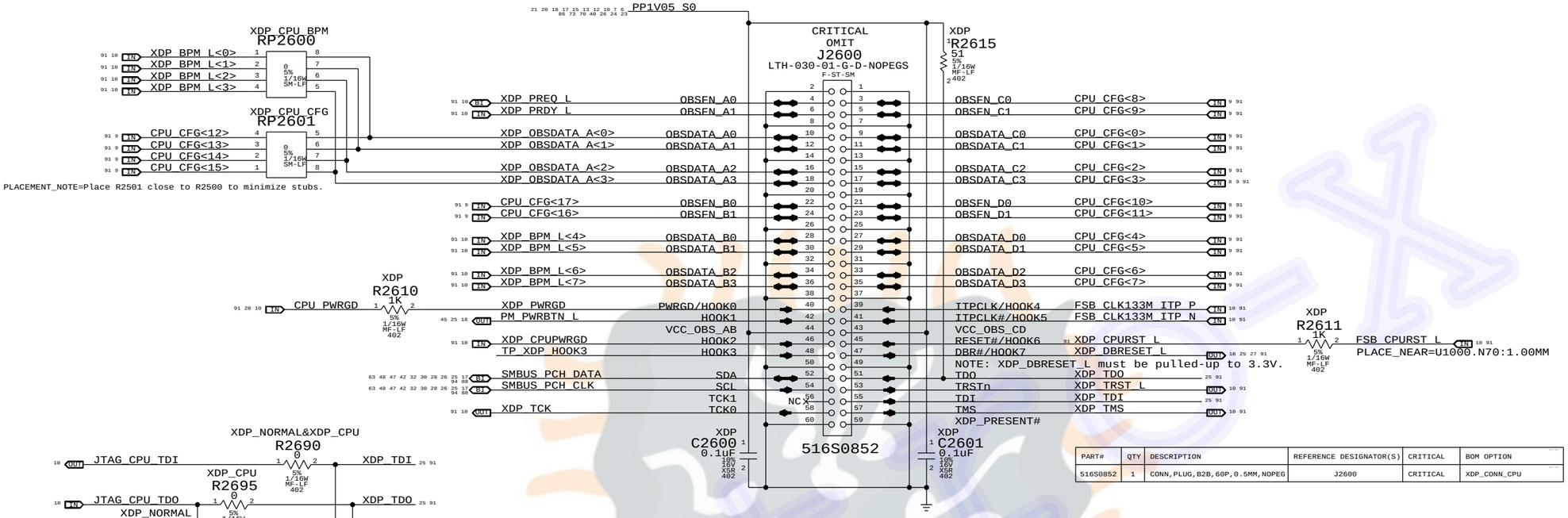
Calpella Processor mini XDP



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
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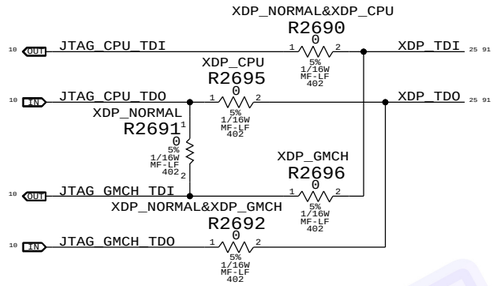
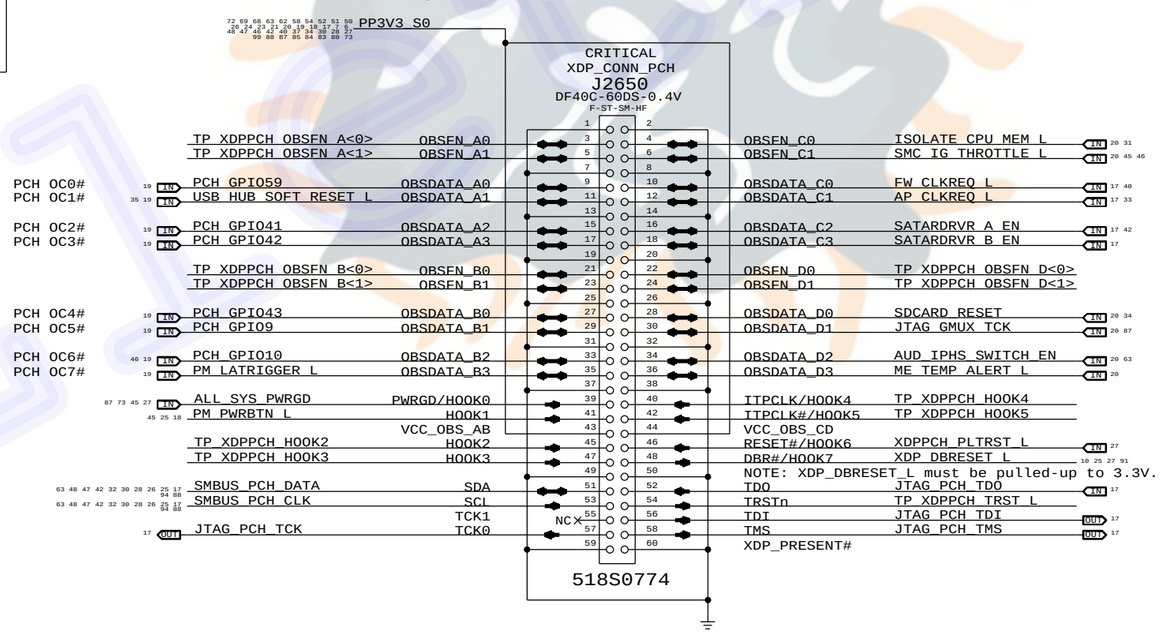


Calpella PCH mini XDP



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PAGE TITLE

eXtended Debug Port (XDP)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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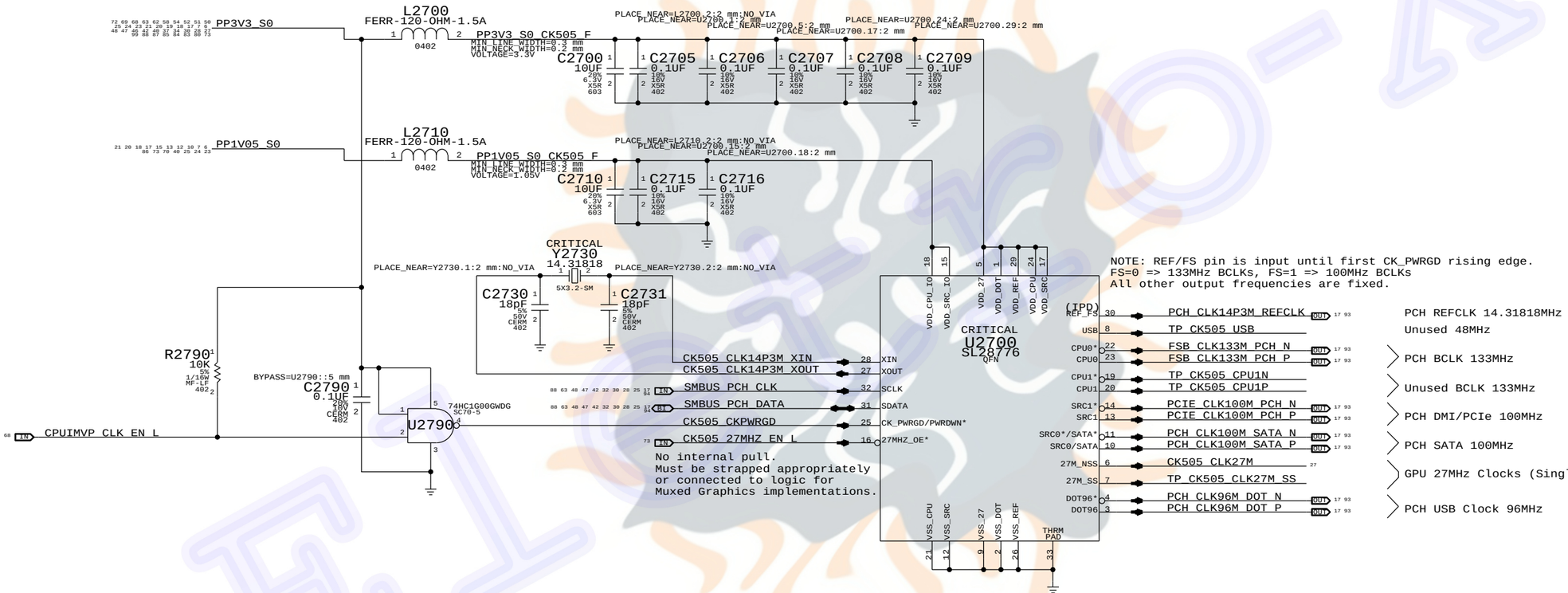
DATE 25 Jun 2009



SYNC_MASTER=K17_MLB SYNC_DATE=06/23/2009

PAGE TITLE: Clock (CK505)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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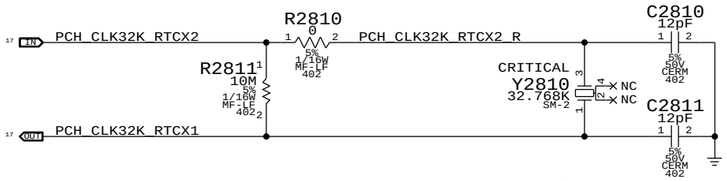
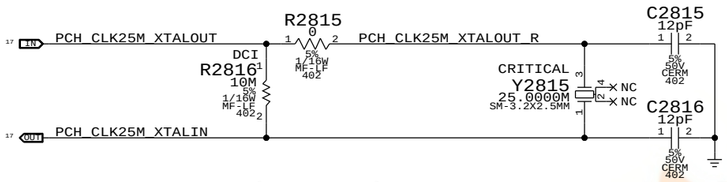
SHEET: 20 OF 101

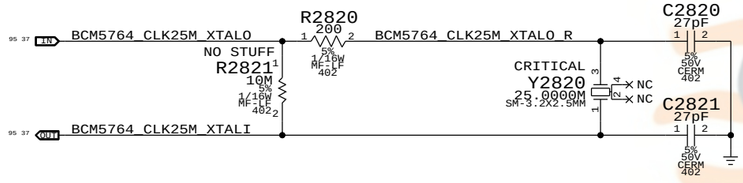
PCH RTC Crystal



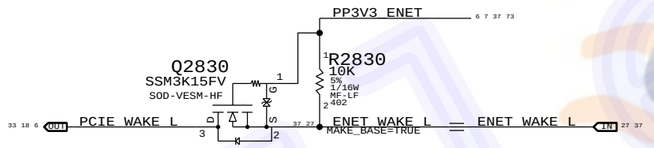
PCH 25MHz Crystal



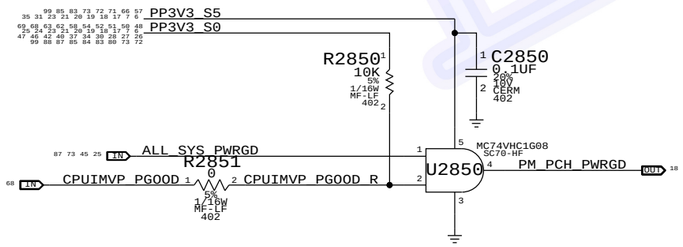
Caesar II (ENET) 25MHz Crystal



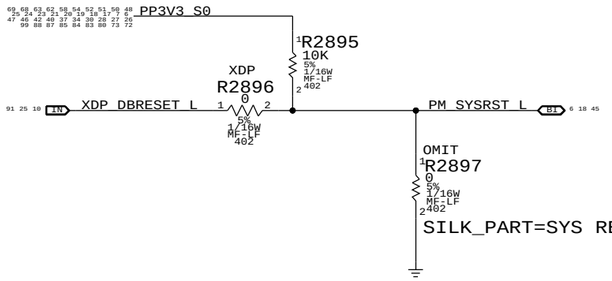
Ethernet WAKE# Isolation



PCH S0 PWRGD

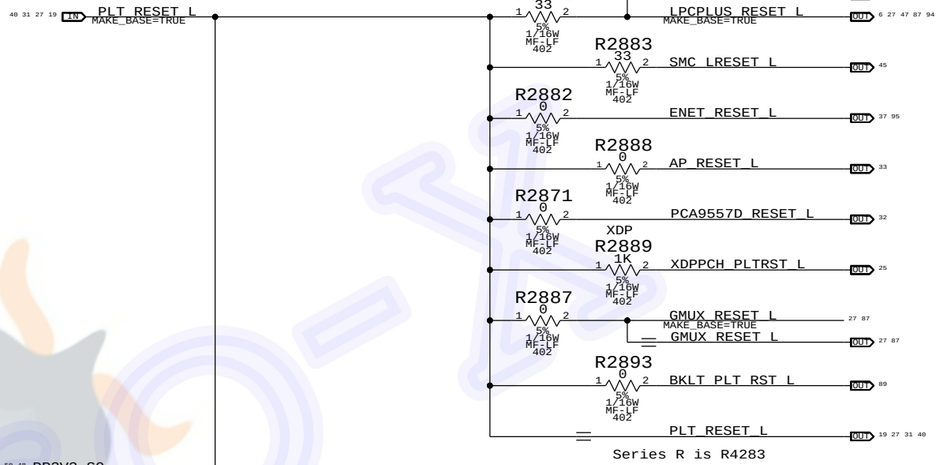


PCH Reset Button



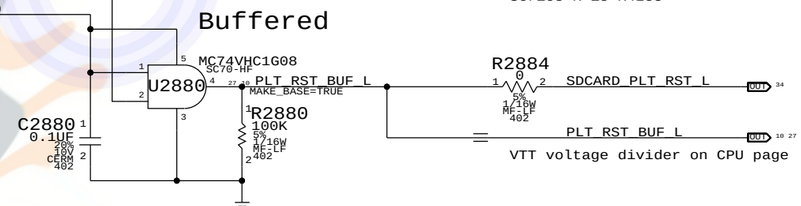
Platform Reset Connections

Unbuffered



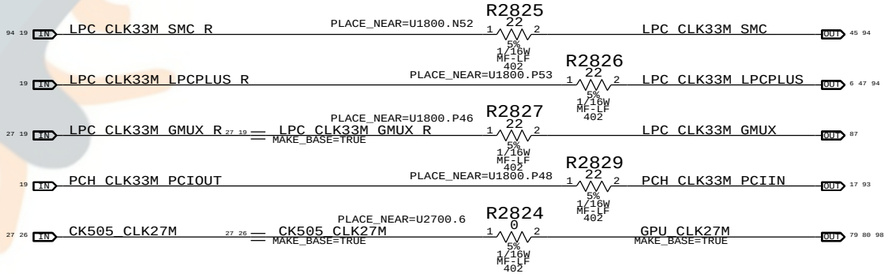
Series R is R4283

Buffered



VTT voltage divider on CPU page

PCH Clock Buffers



SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE

Chipset Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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DATE 27 OF 01

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C2900 10UF 20% 6.3V X6S 603
C2901 10UF 20% 6.3V X6S 603
C2910 0.1UF 20% 10V CERM 402
C2911 0.1UF 20% 10V CERM 402
C2912 0.1UF 20% 10V CERM 402
C2913 0.1UF 20% 10V CERM 402
C2914 0.1UF 20% 10V CERM 402
C2915 0.1UF 20% 10V CERM 402
C2916 0.1UF 20% 10V CERM 402
C2917 0.1UF 20% 10V CERM 402
C2918 0.1UF 20% 10V CERM 402
C2919 0.1UF 20% 10V CERM 402
C2920 0.1UF 20% 10V CERM 402
C2921 0.1UF 20% 10V CERM 402
C2922 0.1UF 20% 10V CERM 402
C2923 0.1UF 20% 10V CERM 402

PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

J2900 F-RT-THB
DDR3-SODIMM-DUAL-K6 (SYMBOL 2 OF 2)

73	CKE0	CKE1	74
75	VDD	VDD	76
77	NC	A15	78
79	BA2	A14	80
81	VDD	VDD	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD	VDD	88
89	A8	A6	90
91	A5	A4	92
93	VDD	VDD	94
95	A3	A2	96
97	A1	A0	98
99	VDD	VDD	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD	VDD	106
107	A10/AP	BA1	108
109	BA0	RAS*	110
111	VDD	VDD	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD	VDD	118
119	A13	ODT1	120
121	S1*	NC	122
123	VDD	VDD	124
125	TEST	VREFCA	126
127	VSS	VSS	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS	VSS	134
135	DQS4*	DM4	136
137	DQS4	VSS	138
139	VSS	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS	144
145	VSS	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS	150
151	VSS	DQS5*	152
153	DM5	DQS5	154
155	VSS	VSS	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS	VSS	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS	VSS	168
169	DQS6*	DM6	170
171	DQS6	VSS	172
173	VSS	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS	178
179	VSS	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS	184
185	VSS	DQS7*	186
187	DM7	DQS7	188
189	VSS	VSS	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS	VSS	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT	VTT	204

NC
KEY
516-0229
SPD ADDR=0xA0(WR)/0xA1(RD)

MEM_A_CKE<0>, MEM_A_CKE<1>
MEM_A_BA<2>, MEM_A_BA<1>, MEM_A_BA<0>
MEM_A_A<12>, MEM_A_A<11>, MEM_A_A<9>, MEM_A_A<8>, MEM_A_A<7>, MEM_A_A<6>, MEM_A_A<5>, MEM_A_A<4>, MEM_A_A<3>, MEM_A_A<2>, MEM_A_A<1>, MEM_A_A<0>, MEM_A_A<10>, MEM_A_A<13>
MEM_A_CLK_P<0>, MEM_A_CLK_N<0>, MEM_A_CLK_P<1>, MEM_A_CLK_N<1>
MEM_A_WE_L, MEM_A_CAS_L, MEM_A_RAS_L, MEM_A_CS_L<1>, MEM_A_CS_L<0>, MEM_A_ODT<0>, MEM_A_ODT<1>
MEM_A_DQ<32>, MEM_A_DQ<33>, MEM_A_DQS_N<4>, MEM_A_DQS_P<4>, MEM_A_DQ<34>, MEM_A_DQ<35>, MEM_A_DQ<40>, MEM_A_DQ<41>, MEM_A_DM<5>, MEM_A_DQ<42>, MEM_A_DQ<43>, MEM_A_DQ<48>, MEM_A_DQ<49>, MEM_A_DQS_N<6>, MEM_A_DQS_P<6>, MEM_A_DQ<50>, MEM_A_DQ<51>, MEM_A_DQ<56>, MEM_A_DQ<57>, MEM_A_DM<7>, MEM_A_DQ<58>, MEM_A_DQ<59>
MEM_A_DQ<36>, MEM_A_DQ<37>, MEM_A_DM<4>, MEM_A_DQ<38>, MEM_A_DQ<39>, MEM_A_DQ<44>, MEM_A_DQ<45>, MEM_A_DQS_N<5>, MEM_A_DQS_P<5>, MEM_A_DQ<46>, MEM_A_DQ<47>, MEM_A_DQ<52>, MEM_A_DQ<53>, MEM_A_DM<6>, MEM_A_DQ<54>, MEM_A_DQ<55>, MEM_A_DQ<60>, MEM_A_DQ<61>, MEM_A_DQS_N<7>, MEM_A_DQS_P<7>, MEM_A_DQ<62>, MEM_A_DQ<63>
MEM_EVENT_A_L
SMBUS_PCH_DATA
SMBUS_PCH_CLK

PP0V75_S0_DDRVTT

J2900 F-RT-THB
DDR3-SODIMM-DUAL-K6 (SYMBOL 1 OF 2)
CRITICAL

1	VREFDQ	VSS	2
3	VSS	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS	8
9	VSS	DQS0*	10
11	DM0	DQS0	12
13	VSS	VSS	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS	VSS	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS	VSS	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS	VSS	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS	VSS	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS	VSS	44
45	DQS2*	DM2	46
47	DQS2	VSS	48
49	VSS	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS	54
55	VSS	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS	60
61	VSS	DQS3*	62
63	DM3	DQS3	64
65	VSS	VSS	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS	VSS	72

KEY
516-0229

MEM_A_DQ<0>, MEM_A_DQ<1>, MEM_A_DM<0>, MEM_A_DQ<2>, MEM_A_DQ<3>, MEM_A_DQ<8>, MEM_A_DQ<9>, MEM_A_DQS_N<1>, MEM_A_DQS_P<1>, MEM_A_DQ<10>, MEM_A_DQ<11>, MEM_A_DQ<16>, MEM_A_DQ<17>, MEM_A_DQS_N<2>, MEM_A_DQS_P<2>, MEM_A_DQ<18>, MEM_A_DQ<19>, MEM_A_DQ<24>, MEM_A_DQ<25>, MEM_A_DM<3>, MEM_A_DQ<26>, MEM_A_DQ<27>
MEM_A_DQ<4>, MEM_A_DQ<5>, MEM_A_DQS_N<0>, MEM_A_DQS_P<0>, MEM_A_DQ<6>, MEM_A_DQ<7>, MEM_A_DQ<12>, MEM_A_DQ<13>, MEM_A_DM<1>, MEM_RESET_L, MEM_A_DQ<14>, MEM_A_DQ<15>, MEM_A_DQ<20>, MEM_A_DQ<21>, MEM_A_DM<2>, MEM_A_DQ<22>, MEM_A_DQ<23>, MEM_A_DQ<28>, MEM_A_DQ<29>, MEM_A_DQS_N<3>, MEM_A_DQS_P<3>, MEM_A_DQ<30>, MEM_A_DQ<31>

PP0V75_S3_MEM_VREFCA_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

PP3V3_S0

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

"Factory" (top) slot

SYNC_MASTER=MASTER SYNC_DATE=MASTER
PAGE TITLE: DDR3 SO-DIMM Connector A
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 29 OF 132
DATE: 28 OF 101

Eletro-X

CPU CHANNEL A DQS 0 -> DIMM A DQS 0

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	⟷	MEM_A_DQS_N<0>	MEM_B_DQS_N<0>	MAKE_BASE=TRUE	⟷	MEM_B_DQS_N<0>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	⟷	MEM_A_DQS_P<0>	MEM_B_DQS_P<0>	MAKE_BASE=TRUE	⟷	MEM_B_DQS_P<0>
MEM_A_DM<0>	MAKE_BASE=TRUE	⟷	MEM_A_DM<0>	MEM_B_DM<0>	MAKE_BASE=TRUE	⟷	MEM_B_DM<0>
MEM_A_DQ<7>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<7>	MEM_B_DQ<7>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<7>
MEM_A_DQ<6>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<6>	MEM_B_DQ<6>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<6>
MEM_A_DQ<5>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<1>	MEM_B_DQ<5>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<2>
MEM_A_DQ<4>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<0>	MEM_B_DQ<4>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<4>
MEM_A_DQ<3>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<2>	MEM_B_DQ<3>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<3>
MEM_A_DQ<2>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<3>	MEM_B_DQ<2>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<1>
MEM_A_DQ<1>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<5>	MEM_B_DQ<1>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<5>
MEM_A_DQ<0>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<4>	MEM_B_DQ<0>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<0>

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

MEM_A_DQS_N<1>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_N<1>	MEM_B_DQS_N<1>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_N<1>
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_P<1>	MEM_B_DQS_P<1>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_P<1>
MEM_A_DM<1>	MAKE_BASE=TRUE	⟷	=MEM_A_DM<1>	MEM_B_DM<1>	MAKE_BASE=TRUE	⟷	=MEM_B_DM<1>
MEM_A_DQ<15>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<11>	MEM_B_DQ<15>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<15>
MEM_A_DQ<14>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<10>	MEM_B_DQ<14>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<14>
MEM_A_DQ<13>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<8>	MEM_B_DQ<13>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<13>
MEM_A_DQ<12>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<9>	MEM_B_DQ<12>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<8>
MEM_A_DQ<11>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<15>	MEM_B_DQ<11>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<11>
MEM_A_DQ<10>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<14>	MEM_B_DQ<10>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<10>
MEM_A_DQ<9>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<13>	MEM_B_DQ<9>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<12>
MEM_A_DQ<8>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<12>	MEM_B_DQ<8>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<9>

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

MEM_A_DQS_N<2>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_N<2>	MEM_B_DQS_N<2>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_N<2>
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_P<2>	MEM_B_DQS_P<2>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_P<2>
MEM_A_DM<2>	MAKE_BASE=TRUE	⟷	=MEM_A_DM<2>	MEM_B_DM<2>	MAKE_BASE=TRUE	⟷	=MEM_B_DM<2>
MEM_A_DQ<23>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<23>	MEM_B_DQ<23>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<23>
MEM_A_DQ<22>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<19>	MEM_B_DQ<22>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<18>
MEM_A_DQ<21>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<20>	MEM_B_DQ<21>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<20>
MEM_A_DQ<20>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<22>	MEM_B_DQ<20>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<17>
MEM_A_DQ<19>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<21>	MEM_B_DQ<19>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<19>
MEM_A_DQ<18>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<18>	MEM_B_DQ<18>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<22>
MEM_A_DQ<17>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<17>	MEM_B_DQ<17>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<21>
MEM_A_DQ<16>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<16>	MEM_B_DQ<16>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<16>

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

MEM_A_DQS_N<3>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_N<3>	MEM_B_DQS_N<3>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_N<3>
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_P<3>	MEM_B_DQS_P<3>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_P<3>
MEM_A_DM<3>	MAKE_BASE=TRUE	⟷	=MEM_A_DM<3>	MEM_B_DM<3>	MAKE_BASE=TRUE	⟷	=MEM_B_DM<3>
MEM_A_DQ<31>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<27>	MEM_B_DQ<31>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<27>
MEM_A_DQ<30>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<26>	MEM_B_DQ<30>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<26>
MEM_A_DQ<29>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<25>	MEM_B_DQ<29>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<24>
MEM_A_DQ<28>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<24>	MEM_B_DQ<28>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<30>
MEM_A_DQ<27>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<31>	MEM_B_DQ<27>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<28>
MEM_A_DQ<26>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<30>	MEM_B_DQ<26>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<29>
MEM_A_DQ<25>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<28>	MEM_B_DQ<25>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<31>
MEM_A_DQ<24>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<29>	MEM_B_DQ<24>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<25>

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

MEM_A_DQS_N<4>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_N<4>	MEM_B_DQS_N<4>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_N<4>
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_P<4>	MEM_B_DQS_P<4>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_P<4>
MEM_A_DM<4>	MAKE_BASE=TRUE	⟷	=MEM_A_DM<4>	MEM_B_DM<4>	MAKE_BASE=TRUE	⟷	=MEM_B_DM<4>
MEM_A_DQ<39>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<33>	MEM_B_DQ<39>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<35>
MEM_A_DQ<38>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<39>	MEM_B_DQ<38>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<38>
MEM_A_DQ<37>	MAKE_BASE=TRUE	⟷	MEM_A_DQ<37>	MEM_B_DQ<37>	MAKE_BASE=TRUE	⟷	MEM_B_DQ<37>
MEM_A_DQ<36>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<38>	MEM_B_DQ<36>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<32>
MEM_A_DQ<35>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<35>	MEM_B_DQ<35>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<33>
MEM_A_DQ<34>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<34>	MEM_B_DQ<34>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<39>
MEM_A_DQ<33>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<32>	MEM_B_DQ<33>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<37>
MEM_A_DQ<32>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<36>	MEM_B_DQ<32>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<36>

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

MEM_A_DQS_N<5>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_N<5>	MEM_B_DQS_N<5>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_N<5>
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_P<5>	MEM_B_DQS_P<5>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_P<5>
MEM_A_DM<5>	MAKE_BASE=TRUE	⟷	=MEM_A_DM<5>	MEM_B_DM<5>	MAKE_BASE=TRUE	⟷	=MEM_B_DM<5>
MEM_A_DQ<47>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<43>	MEM_B_DQ<47>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<47>
MEM_A_DQ<46>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<42>	MEM_B_DQ<46>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<43>
MEM_A_DQ<45>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<45>	MEM_B_DQ<45>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<45>
MEM_A_DQ<44>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<44>	MEM_B_DQ<44>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<41>
MEM_A_DQ<43>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<47>	MEM_B_DQ<43>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<46>
MEM_A_DQ<42>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<46>	MEM_B_DQ<42>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<42>
MEM_A_DQ<41>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<40>	MEM_B_DQ<41>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<44>
MEM_A_DQ<40>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<41>	MEM_B_DQ<40>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<40>

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

MEM_A_DQS_N<6>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_N<6>	MEM_B_DQS_N<6>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_N<6>
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_P<6>	MEM_B_DQS_P<6>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_P<6>
MEM_A_DM<6>	MAKE_BASE=TRUE	⟷	=MEM_A_DM<6>	MEM_B_DM<6>	MAKE_BASE=TRUE	⟷	=MEM_B_DM<6>
MEM_A_DQ<55>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<49>	MEM_B_DQ<55>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<50>
MEM_A_DQ<54>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<50>	MEM_B_DQ<54>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<55>
MEM_A_DQ<53>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<54>	MEM_B_DQ<53>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<54>
MEM_A_DQ<52>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<53>	MEM_B_DQ<52>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<53>
MEM_A_DQ<51>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<55>	MEM_B_DQ<51>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<49>
MEM_A_DQ<50>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<51>	MEM_B_DQ<50>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<51>
MEM_A_DQ<49>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<48>	MEM_B_DQ<49>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<48>
MEM_A_DQ<48>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<52>	MEM_B_DQ<48>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<52>

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

MEM_A_DQS_N<7>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_N<7>	MEM_B_DQS_N<7>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_N<7>
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	⟷	=MEM_A_DQS_P<7>	MEM_B_DQS_P<7>	MAKE_BASE=TRUE	⟷	=MEM_B_DQS_P<7>
MEM_A_DM<7>	MAKE_BASE=TRUE	⟷	=MEM_A_DM<7>	MEM_B_DM<7>	MAKE_BASE=TRUE	⟷	=MEM_B_DM<7>
MEM_A_DQ<63>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<62>	MEM_B_DQ<63>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<63>
MEM_A_DQ<62>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<63>	MEM_B_DQ<62>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<62>
MEM_A_DQ<61>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<56>	MEM_B_DQ<61>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<57>
MEM_A_DQ<60>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<61>	MEM_B_DQ<60>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<56>
MEM_A_DQ<59>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<59>	MEM_B_DQ<59>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<59>
MEM_A_DQ<58>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<58>	MEM_B_DQ<58>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<58>
MEM_A_DQ<57>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<57>	MEM_B_DQ<57>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<60>
MEM_A_DQ<56>	MAKE_BASE=TRUE	⟷	=MEM_A_DQ<60>	MEM_B_DQ<56>	MAKE_BASE=TRUE	⟷	=MEM_B_DQ<61>

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
DDR3 Byte/Bit Swaps

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 30 OF 132

DATE 29 05 2001

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

72 67 31 28 7 6 PP1V5_S3

C3100 10UF 20% 6.3V X6S CERM 603
C3101 10UF 20% 6.3V X6S CERM 603
C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

32 PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 F-RT-BGA6 DDR3-SODIMM (2 OF 2)

92 11 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 11 92
	NC	75	VDD	VDD	76		
92 11 IN	MEM_B_BA<2>	77	NC	A15	78	MEM_B_A<15>	IN 11 92
		79	BA2	A14	80	MEM_B_A<14>	IN 11 92
92 11 IN	MEM_B_A<12>	81	VDD	VDD	82		
92 11 IN	MEM_B_A<9>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 11 92
		85	A9	A7	86	MEM_B_A<7>	IN 11 92
92 11 IN	MEM_B_A<8>	87	VDD	VDD	88		
92 11 IN	MEM_B_A<5>	89	A8	A6	90	MEM_B_A<6>	IN 11 92
		91	A5	A4	92	MEM_B_A<4>	IN 11 92
92 11 IN	MEM_B_A<3>	93	VDD	VDD	94		
92 11 IN	MEM_B_A<1>	95	A3	A2	96	MEM_B_A<2>	IN 11 92
		97	A1	A0	98	MEM_B_A<0>	IN 11 92
92 11 IN	MEM_B_CLK_P<0>	99	VDD	VDD	100		
92 11 IN	MEM_B_CLK_N<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 11 92
		103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 11 92
92 11 IN	MEM_B_A<10>	105	VDD	VDD	106		
92 11 IN	MEM_B_BA<0>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 11 92
		109	BA0	RAS*	110	MEM_B_RAS_L	IN 11 92
92 11 IN	MEM_B_WE_L	111	VDD	VDD	112		
92 11 IN	MEM_B_CAS_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 11 92
		115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 11 92
92 11 IN	MEM_B_A<13>	117	VDD	VDD	118		
92 11 IN	MEM_B_CS_L<1>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 11 92
		121	S1*	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
29 BI	=MEM_B_DQ<32>	129	DQ32	DQ36	130	=MEM_B_DQ<36>	BI 29
29 BI	=MEM_B_DQ<33>	131	DQ33	DQ37	132	=MEM_B_DQ<37>	BI 29
		133	VSS	VSS	134		
29 BI	=MEM_B_DQS_N<4>	135	DQS4*	DM4	136	=MEM_B_DM<4>	IN 29
29 BI	=MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	=MEM_B_DQ<38>	BI 29
92 29 11 BI	MEM_B_DQ<37>	141	DQ34	DQ39	142	=MEM_B_DQ<39>	BI 29
29 BI	=MEM_B_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	=MEM_B_DQ<44>	BI 29
29 BI	=MEM_B_DQ<40>	147	DQ40	DQ45	148	=MEM_B_DQ<45>	BI 29
29 BI	=MEM_B_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	=MEM_B_DQS_N<5>	BI 29
29 IN	=MEM_B_DM<5>	153	DM5	DQS5	154	=MEM_B_DQS_P<5>	BI 29
		155	VSS	VSS	156		
29 BI	=MEM_B_DQ<42>	157	DQ42	DQ46	158	=MEM_B_DQ<46>	BI 29
29 BI	=MEM_B_DQ<43>	159	DQ43	DQ47	160	=MEM_B_DQ<47>	BI 29
		161	VSS	VSS	162		
29 BI	=MEM_B_DQ<48>	163	DQ48	DQ52	164	=MEM_B_DQ<52>	BI 29
29 BI	=MEM_B_DQ<49>	165	DQ49	DQ53	166	=MEM_B_DQ<53>	BI 29
		167	VSS	VSS	168		
29 BI	=MEM_B_DQS_N<6>	169	DQS6*	DM6	170	=MEM_B_DM<6>	IN 29
29 BI	=MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	=MEM_B_DQ<54>	BI 29
29 BI	=MEM_B_DQ<50>	175	DQ50	DQ55	176	=MEM_B_DQ<55>	BI 29
29 BI	=MEM_B_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	=MEM_B_DQ<60>	BI 29
29 BI	=MEM_B_DQ<56>	181	DQ56	DQ61	182	=MEM_B_DQ<61>	BI 29
29 BI	=MEM_B_DQ<57>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	=MEM_B_DQS_N<7>	BI 29
29 IN	=MEM_B_DM<7>	187	DM7	DQS7	188	=MEM_B_DQS_P<7>	BI 29
		189	VSS	VSS	190		
29 BI	=MEM_B_DQ<58>	191	DQ58	DQ62	192	=MEM_B_DQ<62>	BI 29
29 BI	=MEM_B_DQ<59>	193	DQ59	DQ63	194	=MEM_B_DQ<63>	BI 29
		195	VSS	VSS	196		
	MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_A_L	OUT 28 45 46
		199	VDDSPD	SDA	200	SMBUS_PCH_DATA	BI 17 25 26 28 32 42 47 48 63 88 94
	MEM_B_SA<1>	201	SA1	SCL	202	SMBUS_PCH_CLK	IN 17 25 26 28 32 42 47 48 63 88 94
		203	VTT	VTT	204		PP0V75_S0_DDRVTT 6 7 28 31 67
		205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

MTG PINS

516S0806
SPD ADDR=0xA4(WR)/0xA5(RD)

J3100 F-RT-BGA6 DDR3-SODIMM (1 OF 2) CRITICAL

		1	VREFDQ	VSS	2		
29 BI	=MEM_B_DQ<0>	3	VSS	DQ4	4	=MEM_B_DQ<4>	BI 29
29 BI	=MEM_B_DQ<1>	5	DQ0	DQ5	6	=MEM_B_DQ<5>	BI 29
		7	DQ1	VSS	8		
92 29 11 IN	MEM_B_DM<0>	9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 11 29 92
		11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 11 29 92
		13	VSS	VSS	14		
29 BI	=MEM_B_DQ<2>	15	DQ2	DQ6	16	=MEM_B_DQ<6>	BI 29
29 BI	=MEM_B_DQ<3>	17	DQ3	DQ7	18	=MEM_B_DQ<7>	BI 29
		19	VSS	VSS	20		
29 BI	=MEM_B_DQ<8>	21	DQ8	DQ12	22	=MEM_B_DQ<12>	BI 29
29 BI	=MEM_B_DQ<9>	23	DQ9	DQ13	24	=MEM_B_DQ<13>	BI 29
		25	VSS	VSS	26		
29 BI	=MEM_B_DQS_N<1>	27	DQS1*	DM1	28	=MEM_B_DM<1>	IN 29
29 BI	=MEM_B_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN 28 31
		31	VSS	VSS	32		
29 BI	=MEM_B_DQ<10>	33	DQ10	DQ14	34	=MEM_B_DQ<14>	BI 29
29 BI	=MEM_B_DQ<11>	35	DQ11	DQ15	36	=MEM_B_DQ<15>	BI 29
		37	VSS	VSS	38		
29 BI	=MEM_B_DQ<16>	39	DQ16	DQ20	40	=MEM_B_DQ<20>	BI 29
29 BI	=MEM_B_DQ<17>	41	DQ17	DQ21	42	=MEM_B_DQ<21>	BI 29
		43	VSS	VSS	44		
29 BI	=MEM_B_DQS_N<2>	45	DQS2*	DM2	46	=MEM_B_DM<2>	IN 29
29 BI	=MEM_B_DQS_P<2>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	=MEM_B_DQ<22>	BI 29
29 BI	=MEM_B_DQ<18>	51	DQ18	DQ23	52	=MEM_B_DQ<23>	BI 29
29 BI	=MEM_B_DQ<19>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	=MEM_B_DQ<28>	BI 29
29 BI	=MEM_B_DQ<24>	57	DQ24	DQ29	58	=MEM_B_DQ<29>	BI 29
29 BI	=MEM_B_DQ<25>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	=MEM_B_DQS_N<3>	BI 29
29 IN	=MEM_B_DM<3>	63	DM3	DQS3	64	=MEM_B_DQS_P<3>	BI 29
		65	VSS	VSS	66		
29 BI	=MEM_B_DQ<26>	67	DQ26	DQ30	68	=MEM_B_DQ<30>	BI 29
29 BI	=MEM_B_DQ<27>	69	DQ27	DQ31	70	=MEM_B_DQ<31>	BI 29
		71	VSS	VSS	72		

KEY

516S0806

PP0V75_S3_MEM_VREFCA_B 32

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

PP3V3_S0 40 32 24 23 20 19 18 17 16 15 14 13 12 11 10 9 8 7 4 3 2 99

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

"Expansion" (bottom) slot

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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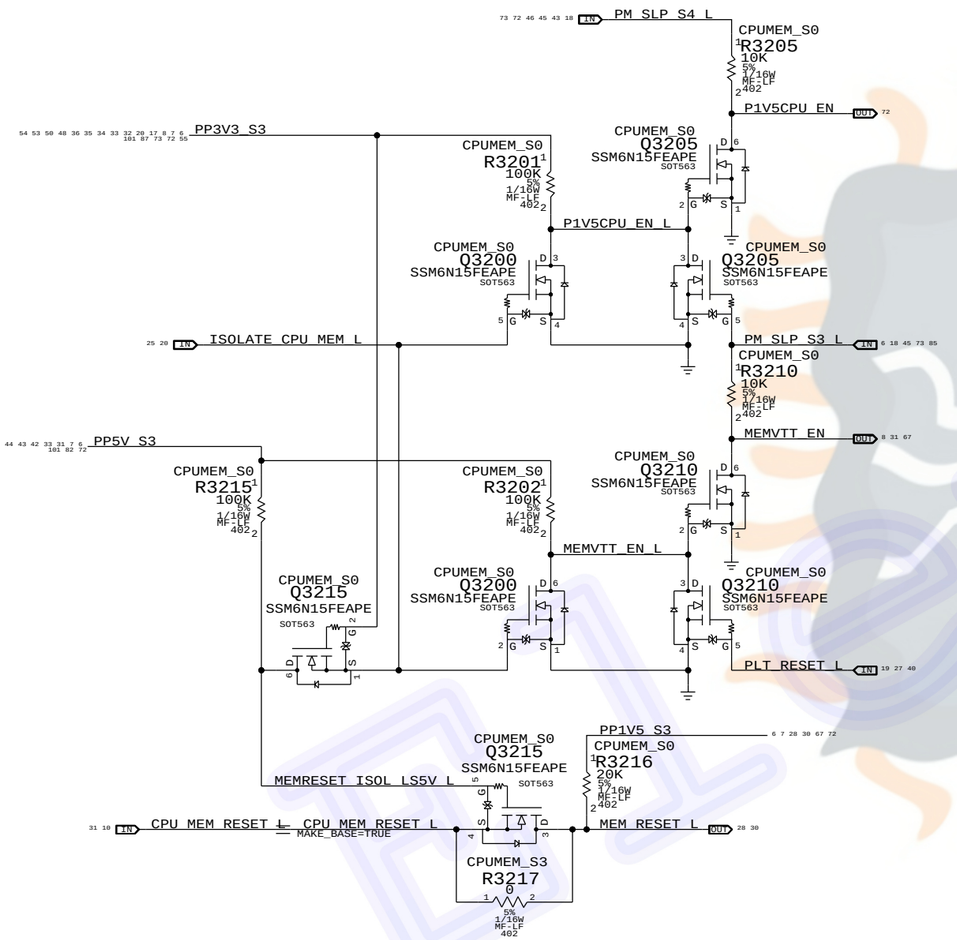
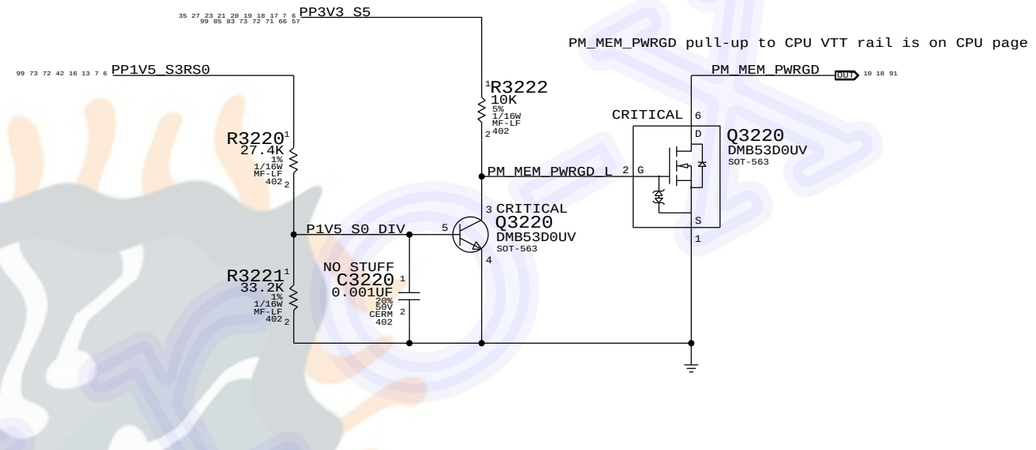
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

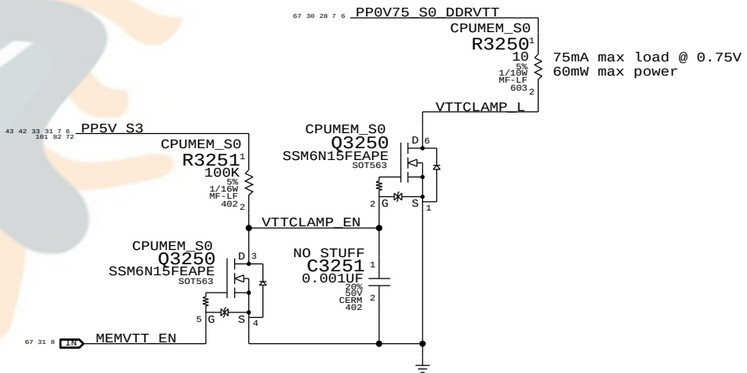


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: CPU Memory S3 Support

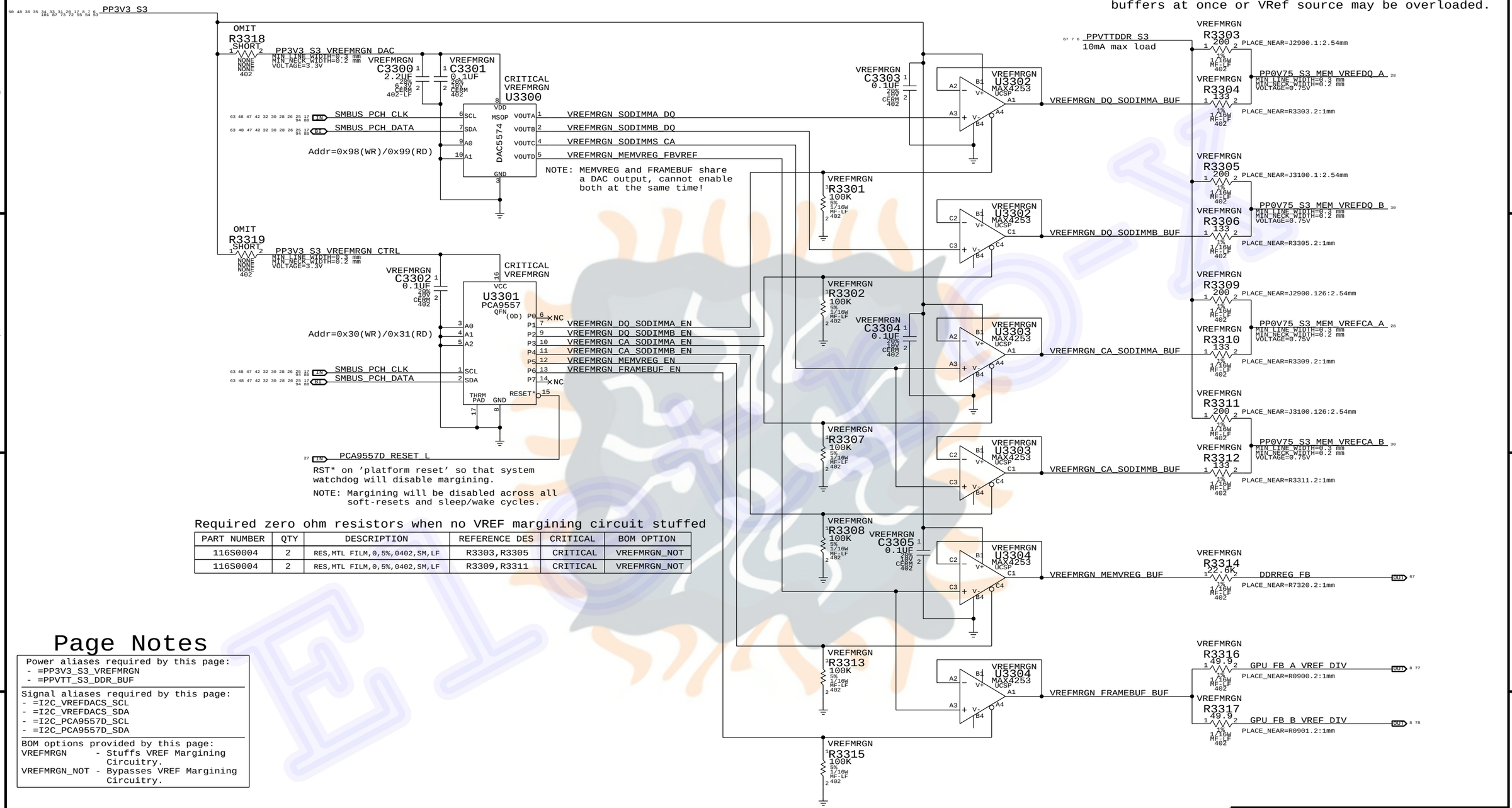
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 31 OF 132



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305	CRITICAL	VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311	CRITICAL	VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

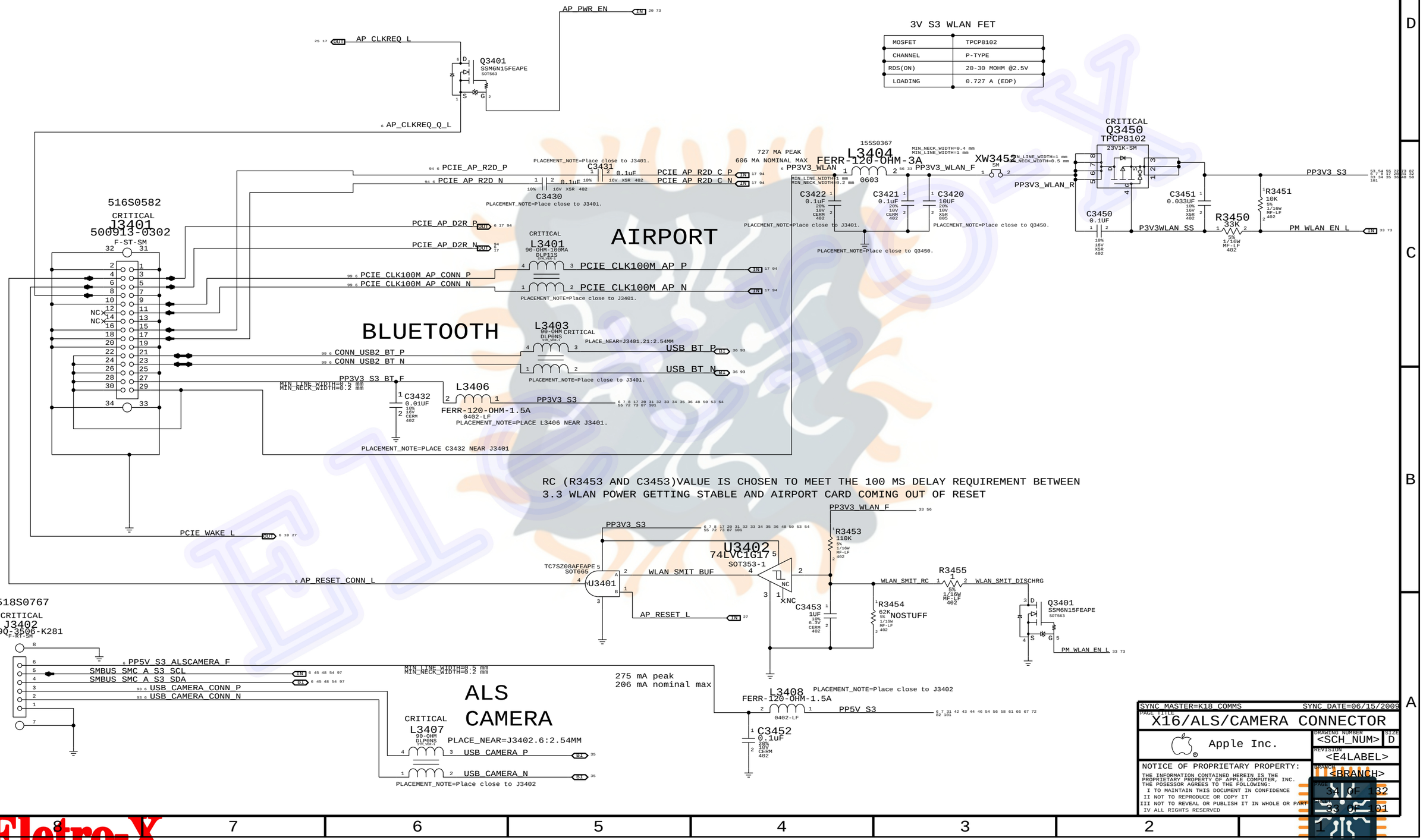
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 33 OF 132


AP_PWR_EN
AP_CLKREQ_L
Q3401
SSM6N15FEAPE
AP_CLKREQ_Q_L
PCIE_AP_R2D_P
PCIE_AP_R2D_N
C3431
0.1uF
C3430
PCIE_AP_R2D_C_P
PCIE_AP_R2D_C_N
PLACEMENT_NOTE=Place close to J3401.
516S0582
CRITICAL
J3401
500913-0302
F-ST-SM
PCIE_AP_D2R_P
PCIE_AP_D2R_N
AIRPORT
CRITICAL
L3401
90-OHM-100MA
DLP11S
PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_CONN_N
PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_N
BLUETOOTH
L3403
90-OHM CRITICAL
DLP0NS
PLACE_NEAR=J3401.21:2.54MM
CONN_USB2_BT_P
CONN_USB2_BT_N
USB_BT_P
USB_BT_N
PP3V3_S3_BT_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
C3432
0.01UF
L3406
FERR-120-OHM-1.5A
0402-LF
PP3V3_S3
PLACEMENT_NOTE=PLACE C3432 NEAR J3401
PLACEMENT_NOTE=PLACE L3406 NEAR J3401.
PCIE_WAKE_L
AP_RESET_CONN_L
3V S3 WLAN FET
MOSFET | TPCP8102
CHANNEL | P-TYPE
RDS(ON) | 20-30 MOHM @2.5V
LOADING | 0.727 A (EDP)
727 MA PEAK
606 MA NOMINAL MAX
155S0367
L3404
FERR-120-OHM-3A
0603
PP3V3_WLAN
PP3V3_WLAN_F
XW3452
PP3V3_WLAN_R
CRITICAL
Q3450
TPCP8102
23V1K-SM
C3422
C3421
C3420
C3450
C3451
R3450
33K
R3451
10K
PP3V3_S3
P3V3WLAN_SS
PM_WLAN_EN_L
RC (R3453 AND C3453)VALUE IS CHOSEN TO MEET THE 100 MS DELAY REQUIREMENT BETWEEN
3.3 WLAN POWER GETTING STABLE AND AIRPORT CARD COMING OUT OF RESET
PP3V3_WLAN_F
PP3V3_S3
U3402
74LVC1G17
SOT353-1
TC7SZ08AFEAPE
SOT665
U3401
WLAN_SMIT_BUF
AP_RESET_L
R3453
110K
R3455
1
WLAN_SMIT_RC
WLAN_SMIT_DISCHRG
C3453
1UF
R3454
62K
NOSTUFF
Q3401
SSM6N15FEAPE
PM_WLAN_EN_L
518S0767
CRITICAL
J3402
8190-3506-K281
F-RT-SM
PP5V_S3_ALSCAMERA_F
SMBUS_SMC_A_S3_SCL
SMBUS_SMC_A_S3_SDA
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
ALS
CAMERA
CRITICAL
L3407
90-OHM
DLP0NS
PLACE_NEAR=J3402.6:2.54MM
USB_CAMERA_P
USB_CAMERA_N
PLACEMENT_NOTE=Place close to J3402
275 mA peak
206 mA nominal max
L3408
FERR-120-OHM-1.5A
PLACEMENT_NOTE=Place close to J3402
PP5V_S3
C3452
0.1uF
SYNC_MASTER=K18_COMMS
SYNC_DATE=06/15/2009
PAGE TITLE
X16/ALS/CAMERA CONNECTOR
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
34 OF 132
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Caesar IV Support

PP3V3_S3

GL137 R3511 0 5% 1/16W MF-LF 402

PP3V3_S3_CARDREADER_DVDD
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

GL137 L3500 0.22UH 0805-1

GL137 C3500 10UF 20% 6.3V X5R 603
GL137 C3501 0.1UF 20% 10V CERM 402
GL137 C3502 0.1UF 20% 10V CERM 402
GL137 C3503 0.1UF 20% 10V CERM 402

BYPASS=U3500.15:16:5 mm
BYPASS=U3500.26:27:5 mm
BYPASS=U3500.35:34:5 mm

PP3V3_S3_CARDREADER_AVDD
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

GL137 C3514 10UF 20% 6.3V X5R 603
GL137 C3504 0.1UF 20% 10V CERM 402
GL137 C3508 0.1UF 20% 10V CERM 402

BYPASS=U3500.6:5:5 mm
BYPASS=U3500.11:12:5 mm

PP1V8_S3_CARDREADER
MIN_LINE_WIDTH=0.20MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=1.8V

BYPASS=U3500.4:5:5 mm
GL137 C3506 0.1UF 20% 10V CERM 402

GL137 R3507 10K 5% 1/16W MF-LF 402
NO STUFF R3508 10K 5% 1/16W MF-LF 402
NO STUFF R3509 10K 5% 1/16W MF-LF 402
GL137 R3510 10K 5% 1/16W MF-LF 402

NO STUFF R3503 1M 5% 1/16W MF-LF 402
GL137 CRITICAL Y3500 12.000M-100PPM 8X4.5X1.4-SM
GL137 C3511 33PF 5% 50V CERM 402
GL137 C3512 33PF 5% 50V CERM 402

GL137 R3506 715 1% 1/16W MF-LF 402
GL137 R3502 0 5% 1/16W MF-LF 402
NO STUFF C3513 0.1UF 20% 10V CERM 402

GL137 Q3500 SSM6N15FEAPE SOT563
SDCARD_RESET
SDCARD_PLT_RST
GL137 Q3500 SSM6N15FEAPE SOT563
SDCARD_PLT_RST_L

U3500 GL137A LQFP
CRITICAL GL137

USB_SDCARD_N	7	DM
USB_SDCARD_P	8	DP
GL137_GPIO1	48	GPIO1
GL137_GPIO2	47	GPIO2
	46	GPIO3
NC	19	SK
NC	20	CS
NC	21	DO
NC	22	DI (IPD)
GL137_CLK12M_X1	13	X1
GL137_CLK12M_X2	14	X2
GL137_RREF	10	RREF
GL137_TESTMOD	17	TESTMOD (IPD)
GL137_RESET_L	18	EXTRSTZ* (IPU)
	4	VDD180
	6	AVDD
	11	AVDD
	15	DVDD
	26	DVDD
	35	DVDD
NC	25	VDD5V
	36	PMOSO
	40	D0
	43	D1
	37	D2
	29	D3
	28	D4
	30	D5
	32	D6
	38	D7
SD_CLK_R	39	CLK
(IPD) SD_WP	3	
(IPD) SD_CMD	41	
(IPU) PDMOD	2	GL137_PDMOD
(IPU) SD_CDZ	23	
(IPU) XD_CDZ	1	NC
XD_CE	31	NC
(IPD) XD_WEZ	42	NC
(IPD) XD_RBZ	44	NC
(IPD) XD_WPZ	45	NC
(IPU) MS_INS	24	NC
(IPU) MS_BS	33	NC
GND	5, 9, 12, 16, 27, 34	

GL137 R3512 10K 5% 1/16W MF-LF 402

Keep this net short!

GL137 C3507 2.2UF 20% 6.3V CERM1 603
GL137 C3505 0.1UF 20% 10V CERM 402
R3505 39K 5% 1/16W MF-LF 402

PP3V3_SW_SD_PWR
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

Max Current = 250 mA

NO STUFF R3513 10K 5% 1/16W MF-LF 402

GL137 R3504 0 5% 1/16W MF-LF 402
NO STUFF C3515 10PF 5% 50V CERM 402-1

PDMOD: POWER DOWN MODES
NC = DISABLE (DEFAULT)
10K LOW = POWER SAVING MODE ENABLE
10K HIGH = REMOTE WAKE UP ENABLE

SDCONN_DATA<0>	R3550 0	SD_D<0>
SDCONN_DATA<1>	R3551 0	SD_D<1>
SDCONN_DATA<2>	R3552 0	SD_D<2>
SDCONN_DATA<3>	R3553 0	SD_D<3>
SDCONN_DATA<4..7>		SD_D<4..7> MAKE_BASE=TRUE
SDCONN_CLK	R3554 0	SD_CLK
SDCONN_CMD	R3556 0	SD_CMD
SD_WP		SD_WP
SD_CD_L		SD_CD_L

BCM57765 5% 1/16W MF-LF 402

PP3V3_S0
BCM57765 R3555 0 5% 1/16W MF-LF 603

CRITICAL J3500 SD-CARD-K19-K24 F-RT-TH

3	VSS
6	VSS
5	CLK
2	CMD
7	DAT0
8	DAT1
9	DAT2
1	CD/DAT3
10	DAT4
11	DAT5
12	DAT6
13	DAT7
14	CARD_DETECT_SW
15	CARD_DETECT_GND
16	WRITE_PROTECT_SW
4	VDD
17	SHLD_PIN
18	SHLD_PIN
19	SHLD_PIN
20	SHLD_PIN

516-0225

SD_CLK
SD_CMD
SD_D<0>
SD_D<1>
SD_D<2>
SD_D<3>
SD_D<4>
SD_D<5>
SD_D<6>
SD_D<7>
SD_WP
SD_CD_L

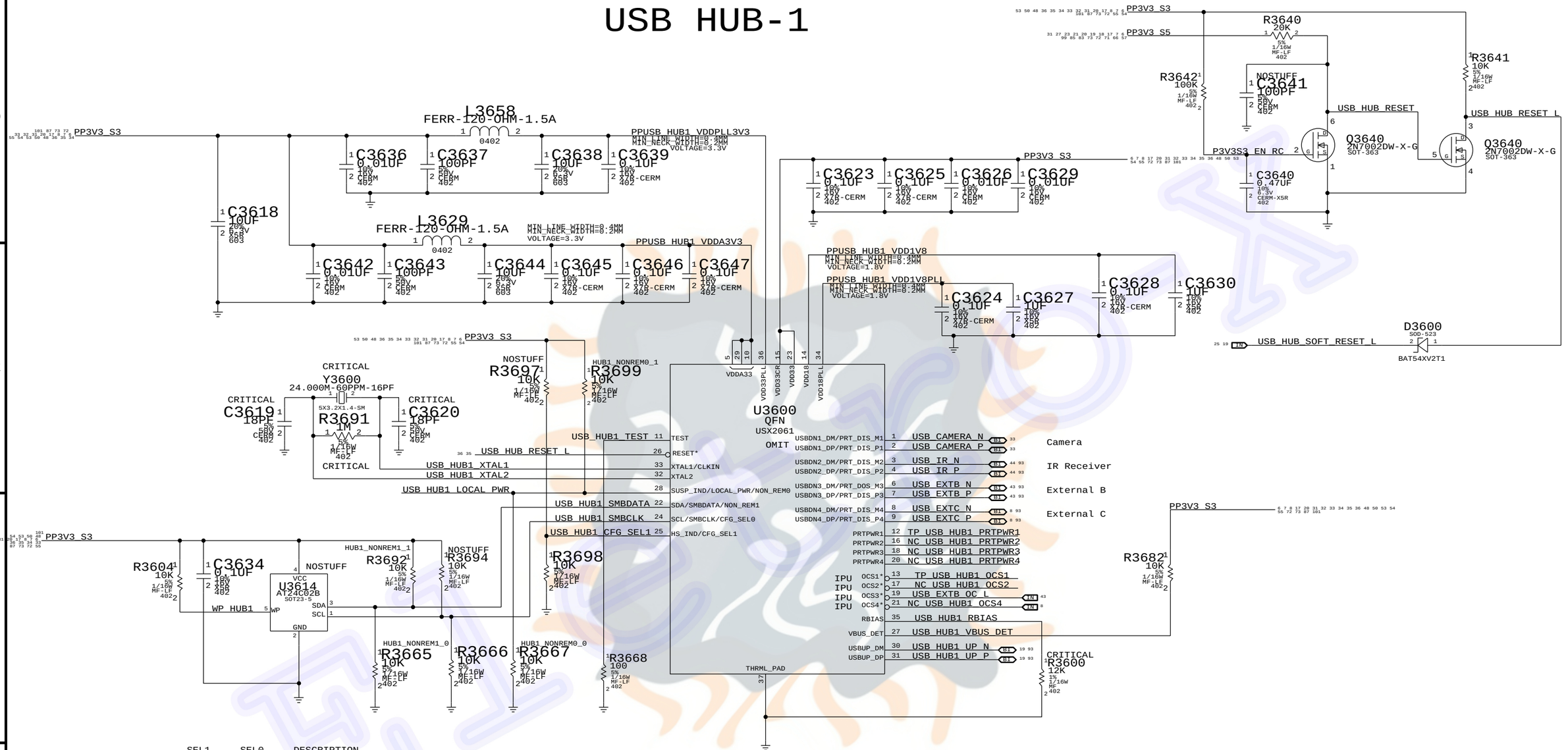
SYNC_MASTER=T27_REF SYNC_DATE=08/26/2009

PAGE TITLE: SecureDigital Card Reader

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 34 OF 132
SHEET: 34 OF 101

USB HUB-1



	SEL1	SEL0	DESCRIPTION
K17/K18 configuration:	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U3600,U3700	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U3600,U3700	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U3600,U3700	CRITICAL	USBHUB_2061

BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1

SYNC_MASTER=K18_MLB SYNC_DATE=10/07/2009

PAGE TITLE: USB HUB 1

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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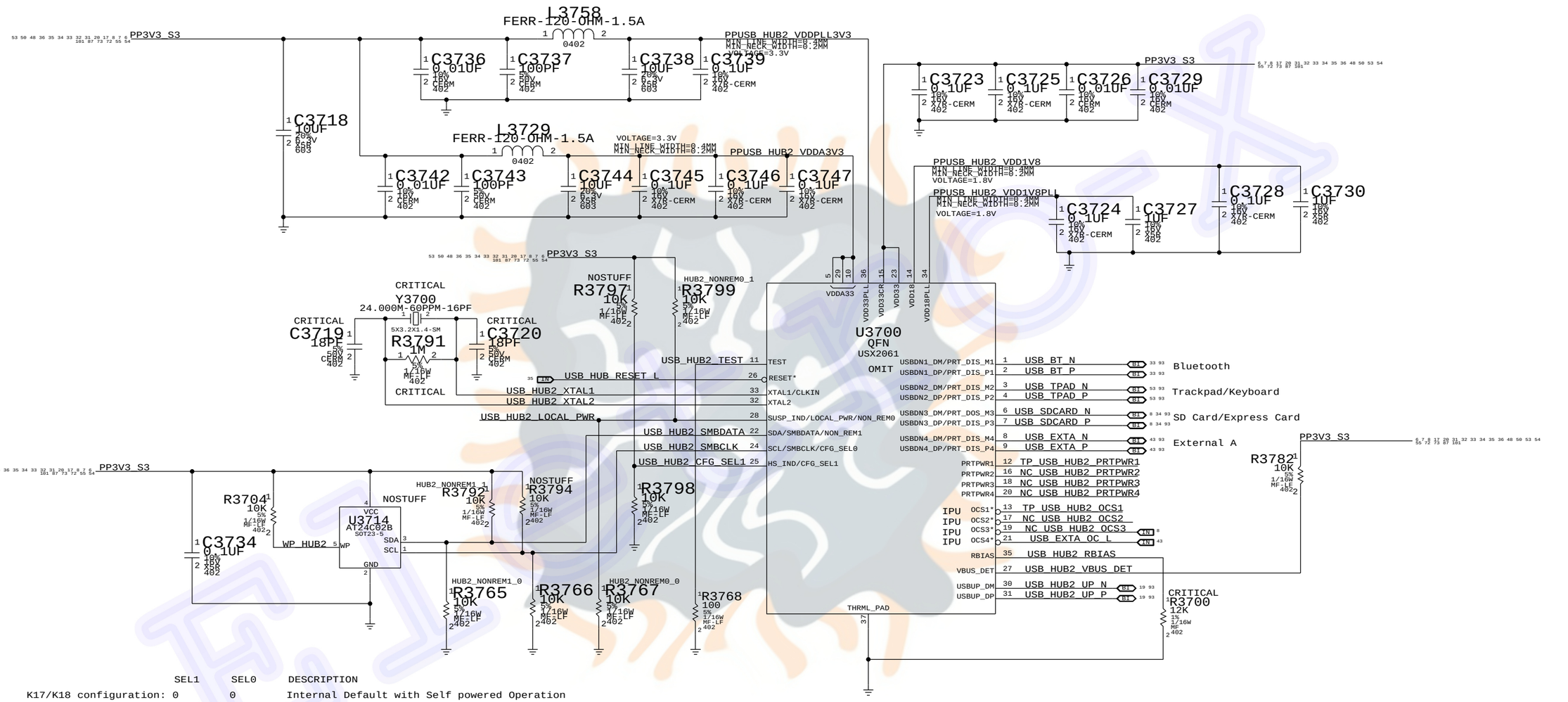
USB HUB-2



	SEL1	SEL0	DESCRIPTION
K17/K18 configuration:	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM GROUP	BOM OPTIONS
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

SYNC_MASTER=K23F SYNC_DATE=10/06/2009

PAGE TITLE: USB HUB 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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BCM57765 SR pins are internal 1.2V switching regulator.
If unused: Okay to float all 4 pins. (Broadcom not so sure now)
If used: VDD/VDDP connect to =PP3V3_ENET_PHY (add bypassing), LX connects to inductor, VFB to =PP1V2_ENET_PHY

PP3V3_ENET
86mA (1000base-T, Caesar II)

PP1V2_ENET
396mA (1000base-T, Caesar II)

BCM57765 SR_VDDP
BCM57765 SR_VDD
BCM57765 VDDO_PIN20
BCM57765 XTALVDDH
BCM57765 SR_LX
BCM57765 SR_VFB

PP3V3_ENET_PHY_XTALVDDH
PP3V3_ENET_PHY_BIASVDDH
PP3V3_ENET_PHY_AVDDH
PP1V2_ENET_PHY_AVDDL
PP1V2_ENET_PHY_PCIEPLL
PP1V2_ENET_PHY_GPHYPLL

PP3V3_S0

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
ENET_WAKE_L (See note)

BCM57765_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L
BCM57765_WAKE_L
ENET_LOW_PWR
BCM57765_SMB_CLK
BCM57765_SMB_DATA
BCM5764_SCLK
BCM5764_MISO
BCM5764_MOSI
BCM5764_CS_L
TP_BCM5764_SPD100LED_L
TP_BCM5764_TRAFFICLED_L
BCM5764_CLK25M_XTALI
BCM5764_CLK25M_XTALO
BCM5764_RDAC

CRITICAL OMIT
U3900
BCM5764M
QFN-8X8
VERSION 2

BCM57765 MEDIA_SENSE
BCM57765 SD_DETECT
BCM57765 CR_CMD
BCM57765 CR_DATA<4>
BCM57765 CR_DATA<5>
BCM57765 CR_DATA<6>
BCM57765 CR_DATA<7>
BCM57765 CE_L_MS_INS_L
BCM57765 CR_LED
TP_BCM57765_XD_DET

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

PP3V3R1V8_SW_SD_VIO
ENET_ENERGY_DET
SD_CD_L
SDCONN_CMD
SDCONN_CLK
SDCONN_DATA<0>
SDCONN_DATA<1>
SDCONN_DATA<2>
SDCONN_DATA<3>
SDCONN_DATA<4>
SDCONN_DATA<5>
SDCONN_DATA<6>
SDCONN_DATA<7>
SD_WP

CR_BUS_PWR is not for SD Card power, just decoupling for BCM57765 CR I/Os.

BCM57765 All resistors above BOMOPTIONed BCM57765

BCM57765 supports both active-levels for WP.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation. (Required ROM size TBD)

U3990
AT45DB011D
SOIC-8S1
OMIT

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures BCM57765 for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: BCM5764M requires SI pull-down instead of SO.

BCM5764M Support

All parts below BOMOPTIONed BCM5764M

BCM5764M pin-function
60-ENERGY_DET
13-WAKE*
53-VMAIN_PRSNT
59-SMB_CLK
58-SMB_DATA
54-VAUX_PRSNT
16-VDDIO
20-XTALVDDH
55-VDDC
17-VDDC
14-VDDC
06-VDDC
26-PCIE_VDDL

Keep net short, with no stubs.

BCM57765 CR_LED	R3980	0		ENET_ENERGY_DET
BCM57765 SR_VFB	R3981	0		ENET_WAKE_L (See note)
BCM57765 CR_DATA<5>	R3982	1K		PP3V3_S0
BCM57765 CE_L_MS_INS_L	R3983	4.7K		PP3V3_ENET
BCM57765 VMAIN_PRSNT	R3984	4.7K		
BCM57765 CR_DATA<6>	R3985	1K		
BCM57765 SR_LX	R3986	0		
BCM57765 VDDO_PIN20	R3987	0		PP3V3_ENET_PHY_XTALVDDH
BCM57765 CR_DATA<7>	R3988	0		PP1V2_ENET
BCM57765 XTALVDDH	R3989	0		
BCM57765 SR_VDD	R3998	0		
BCM57765 SMB_CLK	R3999	0		

BCM57765 CR_CMD — PLACE_NEAR=U3900.26:2 mm — L3999 FERR-600-OHM-0.5A (SM CRITICAL)
C3999 0.1UF — PLACE_NEAR=U3900.26:1 mm
C3998 4.7UF — PLACE_NEAR=L3999.1:1 mm

SYNC_MASTER=T27_REF SYNC_DATE=08/20/2009
PAGE TITLE: Ethernet PHY (Caesar II/IV)
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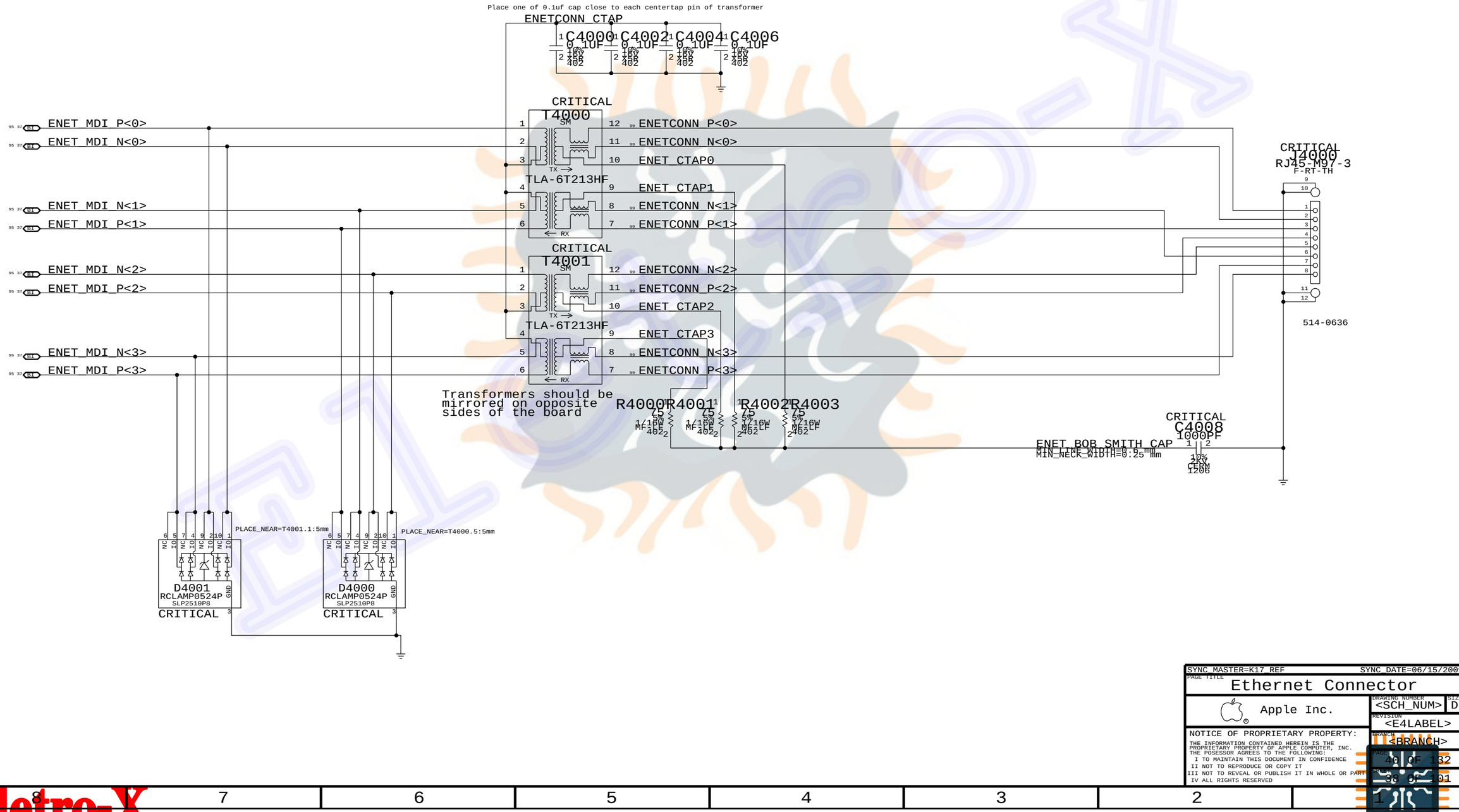
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 39 OF 132

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K17_REF	SYNC_DATE=06/15/2009
PAGE TITLE	Ethernet Connector
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0557	1	RES,0.475 ohm,1%,1/16W,0402	R4100	CRITICAL	

PP1V0_FW_FWPHY 40 7 6
135 mA
OMIT
R4100 0.2 1% 1/10W MF-LF 402
PP1V0_FW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
L4110 120-OHM-0.3A-EMI 0402-LF
PP1V0_FW_FWPHY_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V

25 mA PCIe SerDes
C4110 1UF 10% 6.3V CERM 402
C4111 1UF 10% 6.3V CERM 402

110 mA Digital Core
C4100 1UF 10% 6.3V CERM 402
C4101 1UF 10% 6.3V CERM 402
C4102 1UF 10% 6.3V CERM 402
C4103 1UF 10% 6.3V CERM 402
C4104 1UF 10% 6.3V CERM 402
C4105 1UF 10% 6.3V CERM 402
C4106 1UF 10% 6.3V CERM 402

7 mA I/O
C4120 1UF 10% 6.3V CERM 402
C4121 1UF 10% 6.3V CERM 402
C4122 1UF 10% 6.3V CERM 402
C4123 1UF 10% 6.3V CERM 402
C4124 1UF 10% 6.3V CERM 402
PP3V3_FW_FWPHY 6 7 39 40 41
138 mA

L4130 120-OHM-0.3A-EMI 0402-LF

114 mA FireWire PHY
PP3V3_FW_FWPHY_VDDA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C4130 1UF 10% 6.3V CERM 402
C4131 1UF 10% 6.3V CERM 402
C4132 1UF 10% 6.3V CERM 402

L4135 120-OHM-0.3A-EMI 0402-LF

17 mA PCIe SerDes
PP3V3_FW_FWPHY_VP25
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C4135 1UF 10% 6.3V CERM 402
C4136 1UF 10% 6.3V CERM 402

0 mA VReg PWR
C4141 0.1UF 20% 16V CERM 402
C4140 1UF 10% 6.3V CERM 402

VDD10 VDD33 VDDH VP VP25 VREG_PWR

OMIT
CRITICAL
U4100
FW643
BGA

NC ATBUSB B13
NC ATBUSH A13
NC ATBUSN A11

FWPHY_DS0 41 IN → DS0 (IPD) NT-19 F12
FWPHY_DS1 41 IN → DS1 (IPD) NT-20 E12
FWPHY_DS2 41 IN → DS2 (IPD) NT-21 E13

NC_FW0_TPAN 96 41 6 B1 → TPA0N B8
NC_FW0_TPAP 96 41 6 B1 → TPA0P A8
FW_PORT1_TPA_N 96 41 40 B1 → TPA1N B5
FW_PORT1_TPA_P 96 41 40 B1 → TPA1P A5
NC_FW2_TPAN 41 6 B1 → TPA2N B3
NC_FW2_TPAP 41 6 B1 → TPA2P A3
NC_FW0_TPBN 96 41 6 B1 → TPB0N B9
NC_FW0_TPBP 96 41 6 B1 → TPB0P A9
FW_PORT1_TPB_N 96 41 40 B1 → TPB1N B6
FW_PORT1_TPB_P 96 41 40 B1 → TPB1P A6
NC_FW2_TPBN 41 6 B1 → TPB2N B4
NC_FW2_TPBP 41 6 B1 → TPB2P A4

NC_FW0_TPBIAS 43 B1 → TPBIAS0 B7
FW_P1_TPBIAS 41 40 B1 → TPBIAS1 C3
NC_FW2_TPBIAS 41 6 B1 → TPBIAS2 A2

FW643_R0 → R0 B11
FW643_TPCPS → TPCPS B10

TP_FW643_NAND_TREE → NAND_TREE NT-OUT K1
FW643_REXT → REXT L8
FW_CLK24P576M_XO_R → XO F13
FW_CLK24P576M_XI → XI NT-9 G13

TP_FW643_SE → SE (IPD) M13
TP_FW643_SM → SM (IPD) N13
TP_FW643_MODE_A → MODE_A (IPD) NT-18 J2
TP_FW643_CE → CE (IPD) L13
TP_FW643_FW620_L → FW620* (IPD) D12
TP_FW643_JASI_EN → JASI_EN (IPD) NT-11 D1
6 NC_FW643_AVREG → AVREG A10
TP_FW643_VBUF → VBUF H13
FW643_PU_RST_L → FW_RESET* (IPD) NT-8 K13

TP_FW643_OCR10_CTL → OCR_CTL_V10 J12
NC → OCR_CTL_V12 (Reserved) J13

NOTE: NT-xx notes show NAND tree order.

VSS VREG_VSS

PCI EXPRESS PHY
PCIE_RXD0N → PCIE_FW_R2D_N N8 94
PCIE_RXD0P → PCIE_FW_R2D_P N7 94
PCIE_TXD0N → PCIE_FW_D2R_C_N N5 94
PCIE_TXD0P → PCIE_FW_D2R_C_P N6 94
REFCLKN → PCIE_CLK100M_FW_N N9 IN 17 94
REFCLKP → PCIE_CLK100M_FW_P N10 IN 17 94

PLACEMENT_NOTE=Place C4170 close to U1800
PLACEMENT_NOTE=Place C4171 close to U1800
C4170 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_N IN 17 94
C4171 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_P IN 17 94
C4175 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_N OUT 17 94
C4176 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_P OUT 17 94
PLACEMENT_NOTE=Place C4175 close to U4100
PLACEMENT_NOTE=Place C4176 close to U4100

1394 PHY
TEST CONTROLLER
NT-4 (IPU) TCK → TP_FW643_TCK M4
NT-3 (IPU) TDI → NC_FW643_TDI N2 6
(IPU) TDO → TP_FW643_TDO M1
NT-1 (IPU) TMS → TP_FW643_TMS M3
NT-2 (IPU) TRST* → FW643_TRST_L N1

PP3V3_FW_FWPHY 6 7 39 40 41
FW643_LDO
R4165 10K 5% 1/16W MF-LF 402
R4166 10K 5% 1/16W MF-LF 402
R4164 10K 5% 1/16W MF-LF 402

POWER MANAGEMENT
FIXME!!! - TYPO IN SYMBOL REGCTL
NT-10 (IPD) WAKE* → FW643_WAKE_L C2 OUT 8 40
REGCLT → FW643_REGCTL D13
VAUX_DETECT → FW643_VAUX_DETECT E1
NT-12 (IPD) VAUX_DISABLE → TP_FW643_VAUX_ENABLE D2
NT-13 (OD) CLKREQN → FW_CLKREQ_PHY_L L2 OUT 40

SCIF
NT-16 (IPD) SCIFCLK → TP_FW643_SCIFCLK G2
NT-14 (IPD) SCIFDAIN → TP_FW643_SCIFDAIN G1
NT-17 SCIFDOUT → TP_FW643_SCIFDOUT H1
NT-15 (IPD) SCIFMC → TP_FW643_SCIFMC F2

SERIAL EEPROM CONTROLLER
NT-7 SCL → FW643_SCL N12
NT-6 SDA → TP_FW643_SDA M11

MISCELLANEOUS
CHIP RESET
NT-5 PERST* → FW_RESET_L N4 IN 40
R4163 10K 5% 1/16W MF-LF 402

PPVP_FW_CPS 41
R4160 200K 1% 1/16W MF-LF 402
PLACE_NEAR=U4100.B10:2mm

C4150 22PF 5% 50V CERM 402
C4151 22PF 5% 50V CERM 402
FW_CLK24P576M_XO
CRITICAL
Y4150 24.576MHZ SM-3.2X2.5MMZ
NC NC
R4150 412 1% 1/10W MF-LF 402
R4161 2.94K 1% 1/10W MF-LF 402
R4170 191 1% 1/16W MF-LF 402
R4162 470K 5% 1/10W MF-LF 402
C4162 0.33UF 10% 6.3V CERM-X5R 402

SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009
PAGE TITLE
FireWire LLC/PHY (FW643)
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

3.3V FW FET

I(max) = 1.7A (85C)

PP3V3_S0 → C4201 1UF 10% 6.3V CERM 402 → U4201 TPS22924 CSP (A2 VIN, B2 VIN, A1 VOUT, B1 VOUT, C2 ON, GND, C1) CRITICAL → PP3V3_FW_FWPHY

FW_PWR_EN → U4201 ON

1.05V FW FET

PP1V05_S0 → C4202 1UF 10% 6.3V CERM 402 → U4202 TPS22924 CSP (A2 VIN, B2 VIN, A1 VOUT, B1 VOUT, C2 ON, GND, C1) CRITICAL → PP1V0_FW_FWPHY

U4202 ON ← FW_PWR_EN

PP3V3_FW_FWPHY

PP3V3_FW_FWPHY → R4277 10K 5% 1/16W MF-LF 402 → FW_WAKE

PP3V3_FW_FWPHY → R4276 100K 5% 1/16W MF-LF 402 → FW_WAKE

FW_WAKE → NOSTUFF C4276 0.1UF 10% 10V X5R 402

FW_WAKE → Q4276 DMB53D0UV SOT-563 (CRITICAL) → FW_PLUG_DET_L (OUT)

FW643_WAKE_L (IN) → Q4276 G

FW_CLKREQ_L

FW_CLKREQ_L (OUT) ← Q4261 SSM6N15FEAPE SOT563

FW_CLKREQ_PHY_L (IN) → Q4261

FW_CLKREQ_PHY_L = FW_CLKREQ_PHY_L (MAKE_BASE=TRUE)

FireWire Port Power Switch

PPBUS_G3H → R4260 470K 5% 1/16W MF-LF 402 → FWPWR_EN_L_DIV

PPBUS_G3H → C4260 0.1UF 10% 25V X5R 402 → FWPWR_EN_L_DIV

FWPWR_EN_L_DIV → Q4260 NDS9407 SOI-HF (CRITICAL)

Q4260 → PPBUS_FW_FWPWRSW_F (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.6V)

PPBUS_FW_FWPWRSW_F → F4260 1.1A-24V MINISMDC110H24 (CRITICAL) → PPBUS_FW_FWPWRSW_D (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.6V)

PPBUS_FW_FWPWRSW_D → D4260 SM CRS08-1.5A-30V (CRITICAL) → PPVP_FW

FWPWR_EN_L_DIV → R4262 10K 5% 1/16W MF-LF 402 → FWPWR_EN_TRI

FWPWR_EN_TRI → Q4262 BSS8402DW SOT-363 (SYM-VER1) Q4262

FWPWR_EN_TRI → R4263 10 5% 1/16W MF-LF 402 → FWPWR_EN_TRI_R

FWPWR_EN_TRI_R → Q4262

FWPWR_EN_L_DIV → R4261 330K 5% 1/16W MF-LF 402 → FWPWR_EN_L

FWPWR_EN_L → Q4261 SSM6N15FEAPE SOT563

FWPWR_EN_L → NOSTUFF C4261 0.1UF 10% 10V X5R 402

PP1V05_S0 → R4275 1K 5% 1/16W MF-LF 402 → FW_PWR_EN_L

FW_PWR_EN_L → Q4270 BC847CDXV6TXG SOT563 (CRITICAL)

PP1V05_S0 → R4270 330K 5% 1/16W MF-LF 402 → FW_DET_MIRROR

FW_DET_MIRROR → Q4270

PP1V05_S0 → R4271 56K 5% 1/16W MF-LF 402 → FW_PLUG_DET

FW_PLUG_DET → C4270 0.1UF 10% 10V X5R 402

FW_PLUG_DET → Q4275 DMB53D0UV SOT-563 (CRITICAL) → FW_PLUG_DET_L (OUT)

FW_P1_TPBIAS_R → R4272 1K 5% 1/16W MF-LF 402

FW_DET_EMIT → R4273 12K 5% 1/16W MF-LF 402

PLACE_NEAR=C4360.1:2mm

FW_PWR_EN → Q4275

FW_P1_TPBIAS (IN) → FW_P1_TPBIAS_R

Late-VG Protection

PP3V3_S0 → C4200 0.1UF 10% 10V X5R 402

PLACE_NEAR=U4200.1:2mm

PLACE_NEAR=J4310.1:2mm

U4200 TPD4S1394 LLP (VCC, D1+ FW_PORT1_TPB_P, D1- FW_PORT1_TPB_N, D2+ FW_PORT1_TPA_P, D2- FW_PORT1_TPA_N, VCLMP → TP_FW_LATEVG_VCLMP, FWPWR_EN ← FWPWR_EN, GND) CRITICAL

FWPWR_EN → R4201 100K 5% 1/16W MF-LF 402 → PPBUS_G3H

PP1V05_FW PGOOD/FW_RESET_L

PP3V3_S0 → R4281 100K 5% 1/16W MF-LF 402 → P1V0_FW_RC

PP1V0_FW_FWPHY → R4280 10K 5% 1/16W MF-LF 402 → P1V0_FW_RC

P1V0_FW_RC → C4281 1UF 10% 6.3V CERM 402

P1V0_FW_RC → Q4299 DMB53D0UV SOT-563 (CRITICAL)

P1V0_RESET_GATE → R4283 10K 5% 1/16W MF-LF 402 → PLT_RESET_L (IN)

P1V0_RESET_GATE → Q4299

Q4299 → FW_RESET_L (OUT)

SYNC_MASTER=K19_MLB	SYNC_DATE=05/29/2009
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Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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	BRANCH <BRANCH>
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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

41 40 39 7 6 PP3V3_FW_FWPHY

R4382 10K 1% 1/10W MF-LF 402

R4380 10K 1% 1/10W MF-LF 402

41 39 FWPHY_DS0 MAKE_BASE=TRUE — FWPHY_DS0 39 41

41 39 FWPHY_DS2 MAKE_BASE=TRUE — FWPHY_DS2 39 41

41 39 FWPHY_DS1 MAKE_BASE=TRUE — FWPHY_DS1 39 41

R4381 10K 1% 1/10W MF-LF 402

41 39 NC_FW0_TPBIAS — NC_FW0_TPBIAS MAKE_BASE=TRUE 39 41

41 39 6 NC_FW2_TPBIAS — NC_FW2_TPBIAS MAKE_BASE=TRUE 6 39 41

96 41 39 NC_FW0_TPAN — NC_FW0_TPAN MAKE_BASE=TRUE 39 41 96

96 41 39 6 NC_FW0_TPAP — NC_FW0_TPAP MAKE_BASE=TRUE 6 39 41 96

41 39 6 NC_FW2_TPAN — NC_FW2_TPAN MAKE_BASE=TRUE 6 39 41

41 39 6 NC_FW2_TPAP — NC_FW2_TPAP MAKE_BASE=TRUE 6 39 41

96 41 39 6 NC_FW0_TPBN — NC_FW0_TPBN MAKE_BASE=TRUE 6 39 41 96

96 41 39 6 NC_FW0_TPBP — NC_FW0_TPBP MAKE_BASE=TRUE 6 39 41 96

41 39 6 NC_FW2_TPBN — NC_FW2_TPBN MAKE_BASE=TRUE 6 39 41

41 39 6 NC_FW2_TPBP — NC_FW2_TPBP MAKE_BASE=TRUE 6 39 41

Termination

Place close to FireWire PHY

40 39 FW_P1_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 16V CERM-X5R 402

SIGNAL_MODEL=EMPTY SIGNAL_MODEL=EMPTY

R4360 56.2 1% 1/16W MF-LF 402 — PLACE_NEAR=U4100.A5:2mm

R4361 56.2 1% 1/16W MF-LF 402 — PLACE_NEAR=U4100.B5:2mm

96 41 40 39 FW_PORT1_TPA_P — FW_PORT1_TPA_P MAKE_BASE=TRUE 39 40 41 96

96 41 40 39 FW_PORT1_TPA_N — FW_PORT1_TPA_N MAKE_BASE=TRUE 39 40 41 96

96 41 40 39 FW_PORT1_TPB_P — FW_PORT1_TPB_P MAKE_BASE=TRUE 39 40 41 96

96 41 40 39 FW_PORT1_TPB_N — FW_PORT1_TPB_N MAKE_BASE=TRUE 39 40 41 96

SIGNAL_MODEL=EMPTY SIGNAL_MODEL=EMPTY

R4362 56.2 1% 1/16W MF-LF 402 — PLACE_NEAR=U4100.B6:4mm

R4363 56.2 1% 1/16W MF-LF 402 — PLACE_NEAR=U4100.A6:4mm

FW_PORT1_TPB_C

C4364 220pF 5% 25V CERM 402

R4364 4.99K 1% 1/16W MF-LF 402

41 40 7 6 PPVP_FW

R4311 470K 5% 1/16W MF-LF 402

CPS_EN_L_DIV

R4312 330K 5% 1/16W MF-LF 402

CPS_EN_L

PP3V3_FW_FWPHY

Q4300 BSS8402DW SOT-363 (SYM-VER1)

41 39 PPVP_FW_CPS MAKE_BASE=TRUE — PPVP_FW_CPS 39 41

MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=12.6V

Cable Power

41 40 7 6 PPVP_FW

CRITICAL L4310 FERR-250-OHM SM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V

C4314 0.01UF 10% 50V X7R 402

PORT 1

BILINGUAL

CRITICAL J4310 1394B-M97 F-RT-TH

OUTPUT: TPB- TPB(R) TPB<R> TPB+ VP VP

NC VCC/NC

INPUT: TPA- VG TPA<R> TPA+ TPA(R)

CHASSIS GND

96 41 40 39 FW_PORT1_TPB_N

96 41 40 39 FW_PORT1_TPB_P

(FW_PORT1_BREF)

(GND_FW_PORT1_VG)

96 41 40 39 FW_PORT1_TPA_N

FW_PORT1_AREF

96 41 40 39 FW_PORT1_TPA_P

C4319 0.1uF 10% 50V X7R 603-1

R4319 1M 5% 1/16W MF-LF 402

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

514S0605

SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE: FireWire Ports

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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ODD Power Control

PP5V_S3 → R4596 100K 5% 1/10W MF-LF 402 → ODD_PWR_EN_LS5V_L

C4595 0.068UF 10% 10V CERM 402 (PP5V_S3 → ODD_PWR_SS)

R4595 100K 5% 1/10W MF-LF 402 (ODD_PWR_SS → ODD_PWR_EN_LS5V_L)

CRITICAL
Q4590
TPCP8102
23V1K-SM

PP5V_SW_ODD_R

C4596 0.01UF 10% 16V CERM 402 (ODD_PWR_SS → GND)

J4500 connection separated to support debug sense resistor. Alias together if no sense R.

NOTE: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.

PP3V3_S0 → R4597 100K 5% 1/10W MF-LF 402 → ODD_PWR_EN

Q4596 SSM6N15FEAPE SOT563 (D 6, G 2, S 1)

Q4596 SSM6N15FEAPE SOT563 (D 3, G 5, S 4)

ODD_PWR_EN → ODD_PWR_EN_L (IN)

PP5V_SW_ODD → R4590 33K 5% 1/16W MF-LF 402 → SMC_ODD_DETECT (OUT)

Indicates disc presence

CRITICAL
J4500
54722-0164
F-ST-SM

516S0616

SATA_ODD_R2D_P
SATA_ODD_R2D_N
SATA_ODD_D2R_UF_N
SATA_ODD_D2R_UF_P

CRITICAL
FL4520
90-OHM-100MA
DLP11S

SATA_ODD_R2D_UF_P → C4521 0.01UF 10% 16V CERM 402 → SATA_ODD_R2D_C_P (IN)

SATA_ODD_R2D_UF_N → C4520 0.01UF 10% 16V CERM 402 → SATA_ODD_R2D_C_N (IN)

CRITICAL
FL4525
90-OHM-100MA
DLP11S

SATA_ODD_D2R_C_N → C4526 0.01UF 10% 16V CERM 402 → SATA_ODD_D2R_N (OUT)

SATA_ODD_D2R_C_P → C4525 0.01UF 10% 16V CERM 402 → SATA_ODD_D2R_P (OUT)

SATA ODD Connector

PS8511A / PS8515A Straps

PP1V5_S3RS0

PS8511A:

PIN	NAME	
9	A_PRE	(IPD)
8	B_PRE	(IPD)
20	A_BST#	(IPU)
10	B_BST#	(IPU)
19	A_EQ	(IPD)
18	B_EQ	(IPD)

RDRV:8515A1&RDRV:8515A2
NO STUFF R4511 10K 5% 1/16W MF-LF 402
R4515 10K 5% 1/16W MF-LF 402
R4517 10K NO STUFF 5% 1/16W MF-LF 402

SATARDRVR_A_B_SD
SATARDRVR_A_I2C_ADDR
SATARDRVR_A_A_SD
SATARDRVR_A_I2C_EN

RDRV:8515A1&RDRV:8515A2
NO STUFF R4519 10K 5% 1/16W MF-LF 402
NO STUFF R4520 10K 5% 1/16W MF-LF 402
R4512 10K 5% 1/16W MF-LF 402
NO STUFF R4516 10K 5% 1/16W MF-LF 402
NO STUFF R4518 10K 5% 1/16W MF-LF 402

SMBUS_PCH_CLK → R4513 0 5% 1/16W MF-LF 402 → SATARDRVR_A_I2C_SCL

SMBUS_PCH_DATA → R4514 0 5% 1/16W MF-LF 402 → SATARDRVR_A_I2C_SDA

RDRV:8515A1&RDRV:8515A2

SATA HDD/IR/SIL Connector

PP5V_S0_HDD_FLT (MIN_LINE_WIDTH=0.6mm, MIN_NECK_WIDTH=0.4mm, VOLTAGE=5V)

PLACE_NEAR=L4500.1:2mm
CRITICAL
L4500
FERR-70-OHM-4A
0603

PP5V_S0_HDD_R (MIN_LINE_WIDTH=0.6mm, MIN_NECK_WIDTH=0.4mm, VOLTAGE=5V)

C4501 0.1UF 20% 10V CERM 402

C4502 0.1UF 20% 10V CERM 402 PLACE_NEAR=L4500.2:2mm

XW4599 SM: PP5V_S0_HDD_R → PP5V_S0

PP5V_S3 → R4532 10 5% 1/16W MF-LF 402 → PP5V_S3_IR_R (MIN_LINE_WIDTH=0.5mm, MIN_NECK_WIDTH=0.2mm, VOLTAGE=5V)

C4532 0.1UF 10% 10V X7R-CERM 402

CRITICAL
J4501
54722-0224
F-ST-SM

IR_RX_OUT (OUT)

SYS_LED_ANODE_R → R4531 4.7 5% 1/16W MF-LF 402 → SYS_LED_ANODE (IN)

C4531 0.001UF 10% 50V CERM 402

SATA_HDD_D2R_C_P
SATA_HDD_D2R_C_N

516S0687

CRITICAL
FL4501
90-OHM-100MA
DLP11S

SATA_HDD_R2D_N
SATA_HDD_R2D_P

SATA_HDD_R2D_UF_N
SATA_HDD_R2D_UF_P

SATA Redriver

PLACE_NEAR=U4510.16:3mm

PP1V5_S3RS0

RDRV:8511&RDRV:8515A1&RDRV:8515A2
R4510 10K (C4514, C4519 & R4510)

C4514 1UF 10% 6.3V CERM-X5R 402

C4519 0.01UF 10% 16V CERM 402

CRITICAL
RDRV:8515A2
U4510
PS8515A-A2
TQFN

(All 4 C's)
RDRV:8511&RDRV:8515A1&RDRV:8515A2

C4516 0.01UF 10% 16V CERM 402 — SATA_HDD_D2R_RDRV_IN_P
C4515 0.01UF 10% 16V CERM 402 — SATA_HDD_D2R_RDRV_IN_N
C4511 0.01UF 10% 16V CERM 402 — SATA_HDD_R2D_RDRV_OUT_N
C4510 0.01UF 10% 16V CERM 402 — SATA_HDD_R2D_RDRV_OUT_P

SATARDRVR_A_EN
SATARDRVR_A_AUTOPWR_EN
SATARDRVR_A_I2C_EN
SATARDRVR_A_I2C_ADDR
SATARDRVR_A_I2C_SCL
SATARDRVR_A_I2C_SDA

NOTE: Internal pulls are ~150K

GND THRM PAD

338S0848 (PS8515A2)
Addr: 0x94(Wr)/0x95(Rd)

PS8515A:
x_SD pins are outputs

(All 4 C's)
RDRV:8511&RDRV:8515A1&RDRV:8515A2

C4518 0.01UF 10% 16V CERM 402 — SATA_HDD_D2R_RDRV_OUT_P
C4517 0.01UF 10% 16V CERM 402 — SATA_HDD_D2R_RDRV_OUT_N
C4513 0.01UF 10% 16V CERM 402 — SATA_HDD_R2D_RDRV_IN_N
C4512 0.01UF 10% 16V CERM 402 — SATA_HDD_R2D_RDRV_IN_P

SATARDRVR_A_A_SD
SATARDRVR_A_B_SD

(All 4 R's, 2 C's)
SIGNAL_MODEL=EMPTY
RDRV:NO

C4582 10PF 5% 50V CERM 402
R4580 51.1 1% 1/16W MF-LF 402
C4583 10PF 5% 50V CERM 402
R4581 51.1 1% 1/16W MF-LF 402

CRITICAL
FL4502
90-OHM-100MA
DLP11S

SATA_HDD_D2R_UF_P → SATA_HDD_D2R_P (OUT)
SATA_HDD_D2R_UF_N → SATA_HDD_D2R_N (OUT)
SATA_HDD_R2D_C_N (IN)
SATA_HDD_R2D_C_P (IN)

(All 4 C's)
SIGNAL_MODEL=EMPTY
RDRV:NO

Redriver Bypass Path

C4580 0.01UF 10% 16V CERM 402 — SATA_HDD_R2D_NORDRV_P
C4581 0.01UF 10% 16V CERM 402 — SATA_HDD_R2D_NORDRV_N
C4585 0.01UF 10% 16V CERM 402 — SATA_HDD_D2R_NORDRV_N
C4586 0.01UF 10% 16V CERM 402 — SATA_HDD_D2R_NORDRV_P

R4585 0 5% 1/16W MF-LF 402
R4586 0 5% 1/16W MF-LF 402

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0769	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV:8511
338S0778	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV:8515A1

BOMOPTIONs:
- RDRV:8511 stuffs PS8511A & associated parts (STRAPS TBD!!!)
- RDRV:8515A1&RDRV:8515A2 stuffs PS8515A & associated parts
- RDRV:NO stuffs bypass path (neither IC or associated parts stuffed)

SYNC_MASTER=T27_REF SYNC_DATE=10/01/2009

PAGE TITLE: SATA Connectors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 46 OF 132
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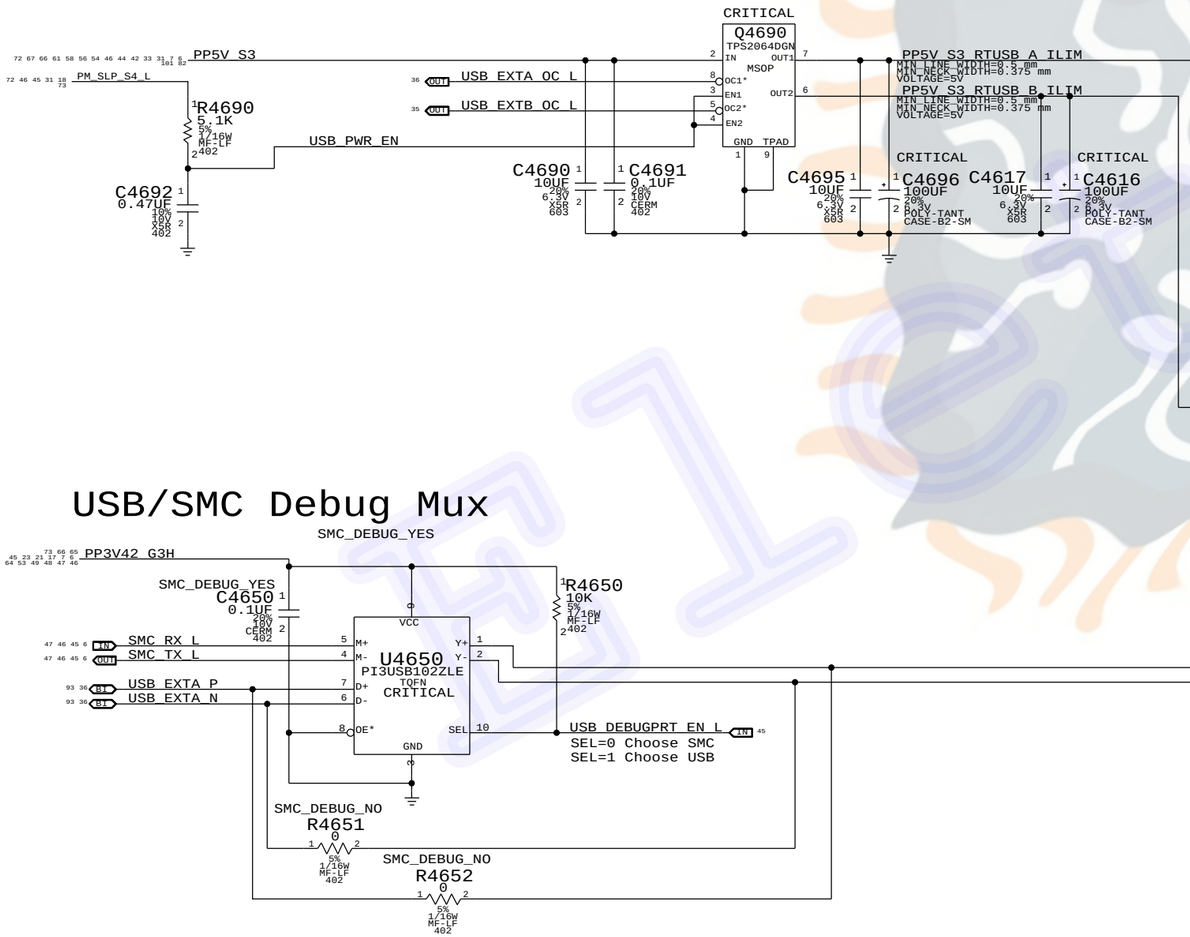
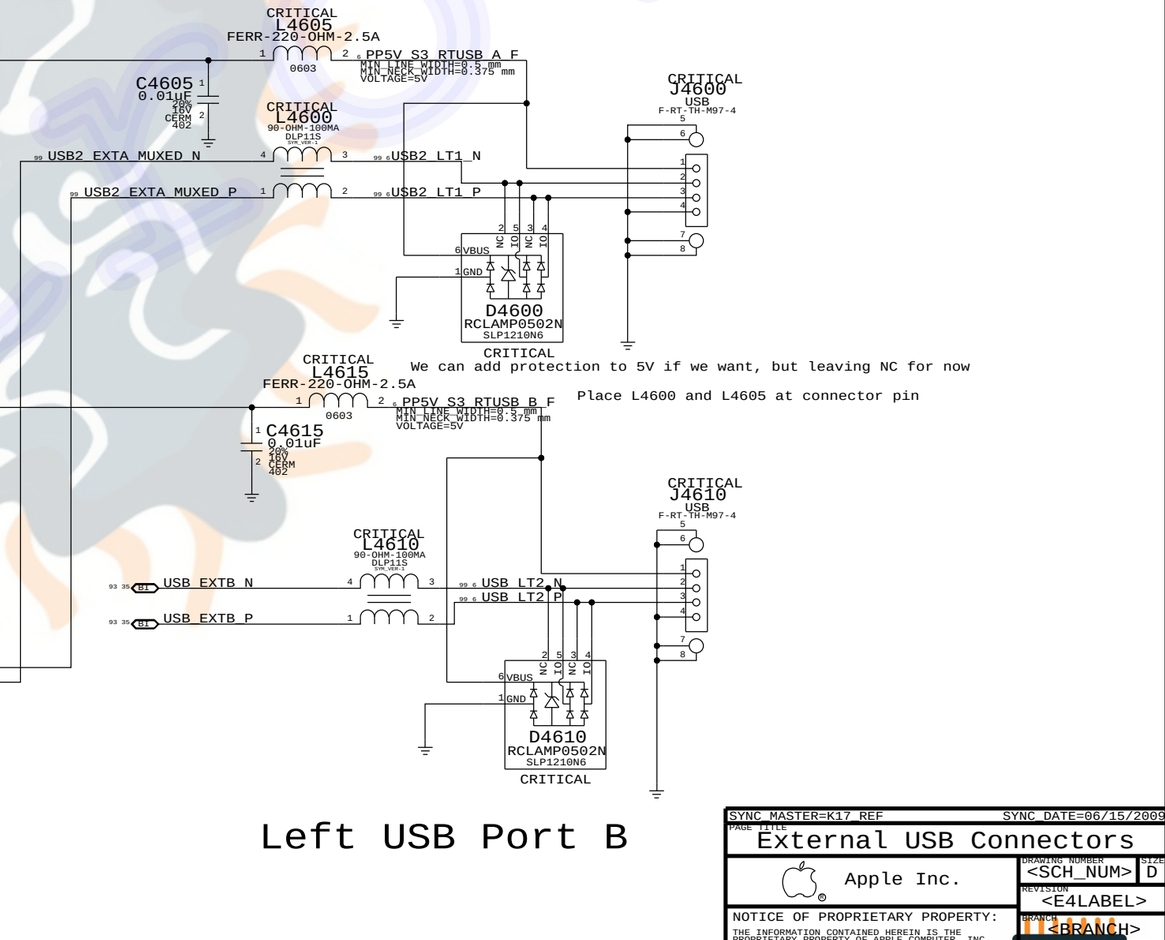
Port Power Switch



Left USB Port A



USB/SMC Debug Mux

Left USB Port B

SYNC_MASTER=K17_REF	SYNC_DATE=06/15/2009
PAGE TITLE	External USB Connectors
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 46 OF 132
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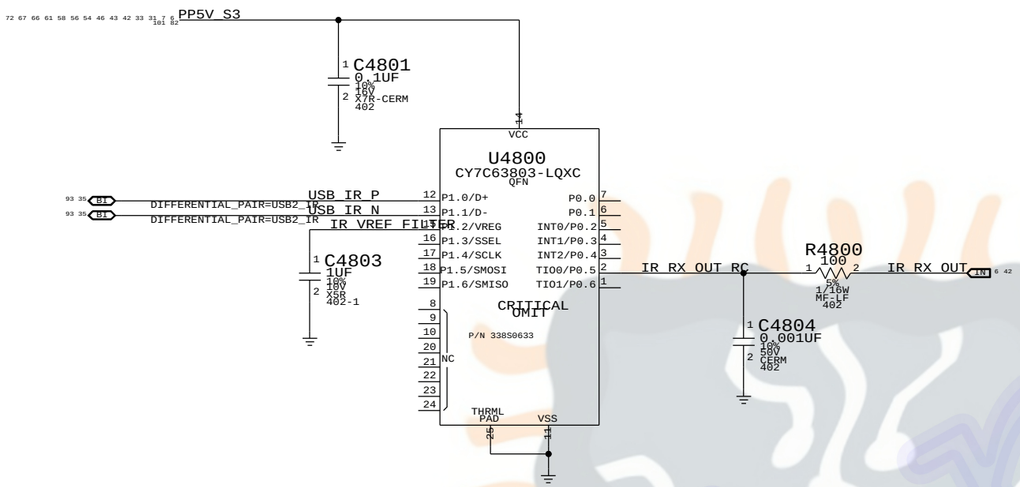
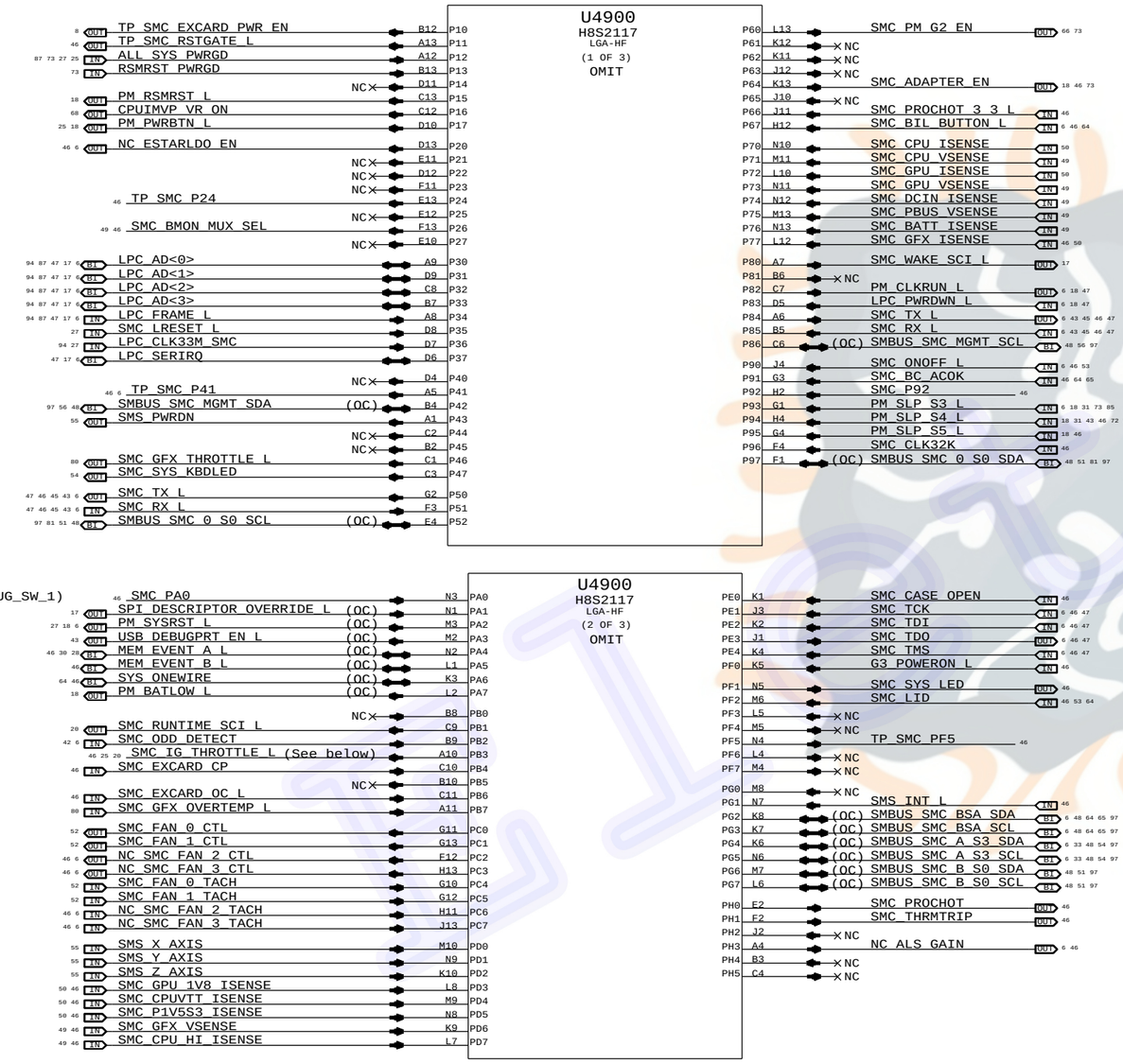
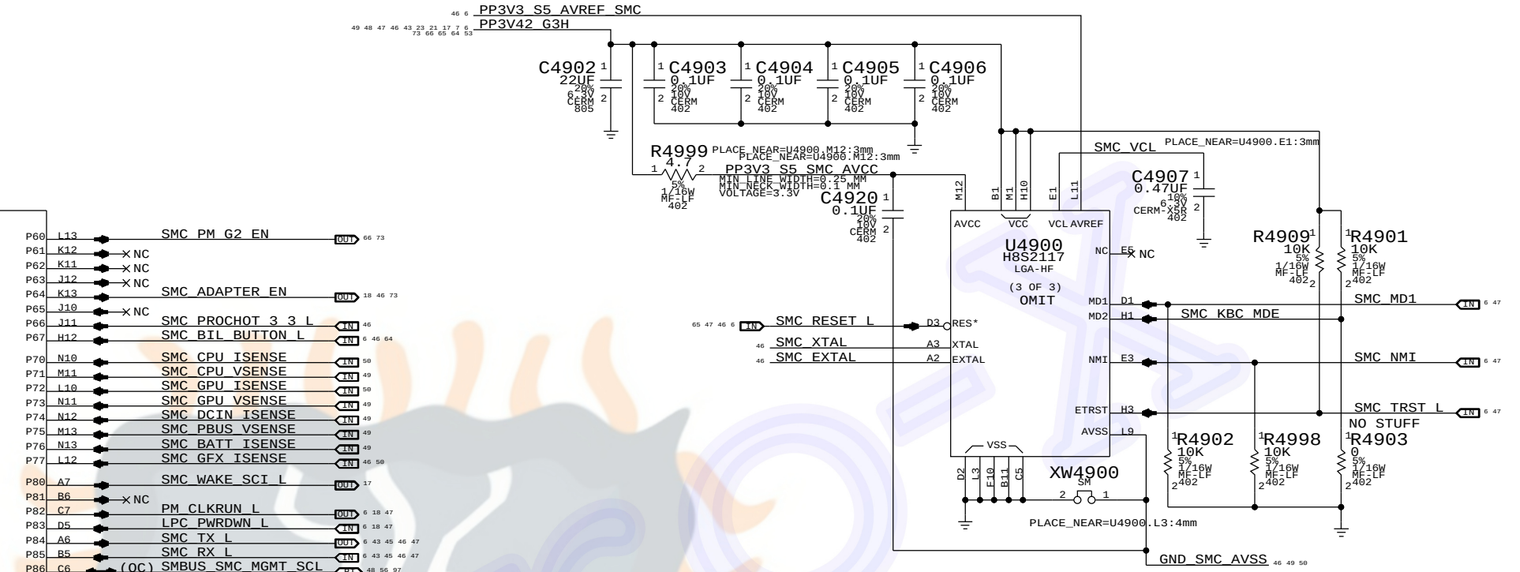
IR SUPPORT



SYNC_MASTER=K19_MLB	SYNC_DATE=05/29/2009
PAGE TITLE: Front Flex Support	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
NOTICE OF PROPRIETARY PROPERTY:	BRANCH: <BRANCH>
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	PAGE: 43 OF 132
	SHEET: 44 OF 101

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SYNC_MASTER=K17_REF	SYNC_DATE=06/15/2009
PAGE TITLE	SMC
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
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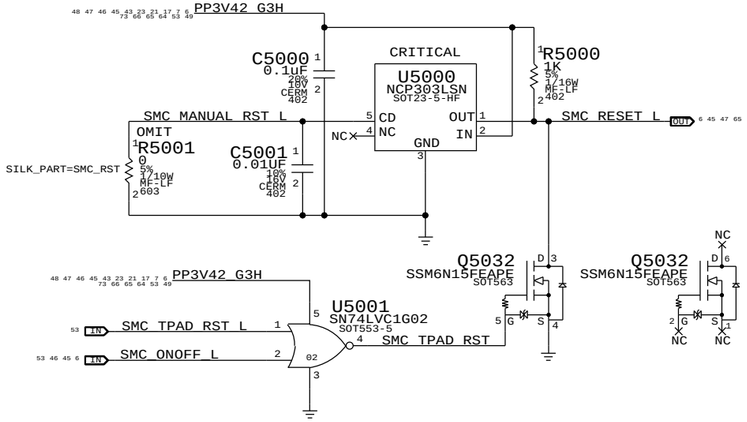
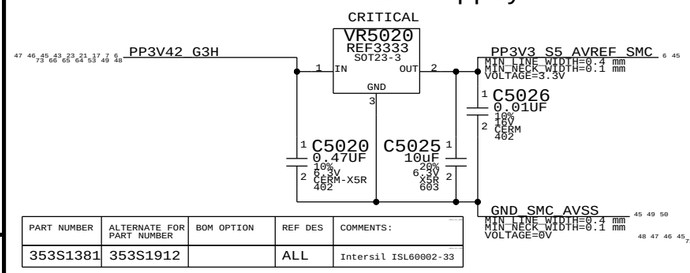
SMC Reset "Button" / Brownout Detect

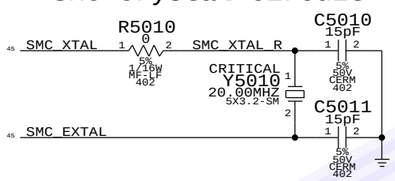


SMC AVREF Supply



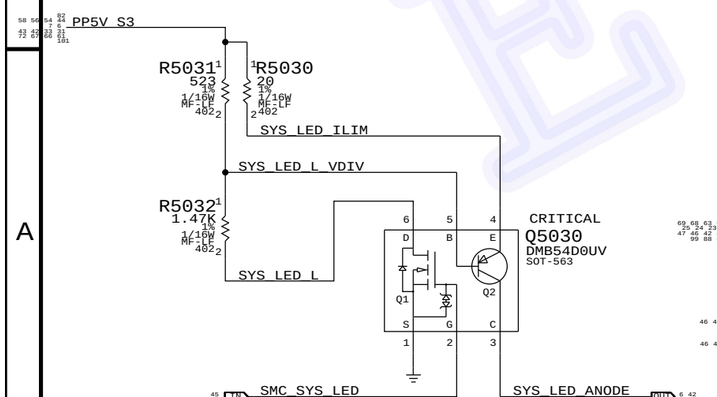
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

SMC Crystal Circuit

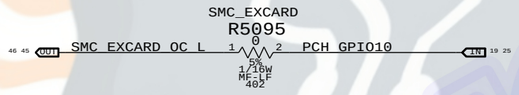


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0350	1	OSC,XTAL,32.768KHZ,LF,HF	U5010	CRITICAL	SMC_OSC_YES

System (Sleep) LED Circuit

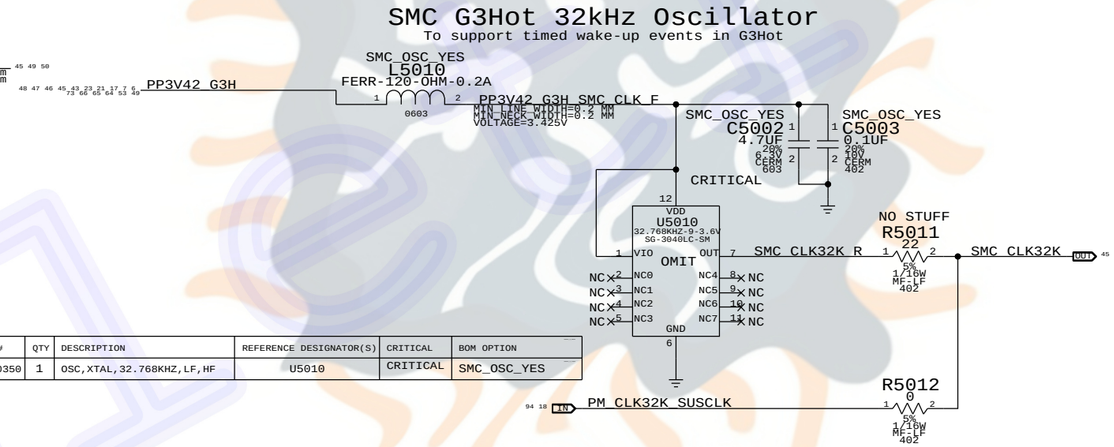


SMC_EXCARD

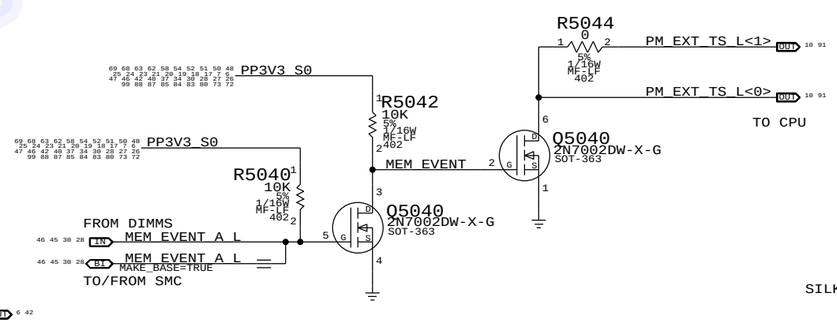


SMC G3Hot 32kHz Oscillator

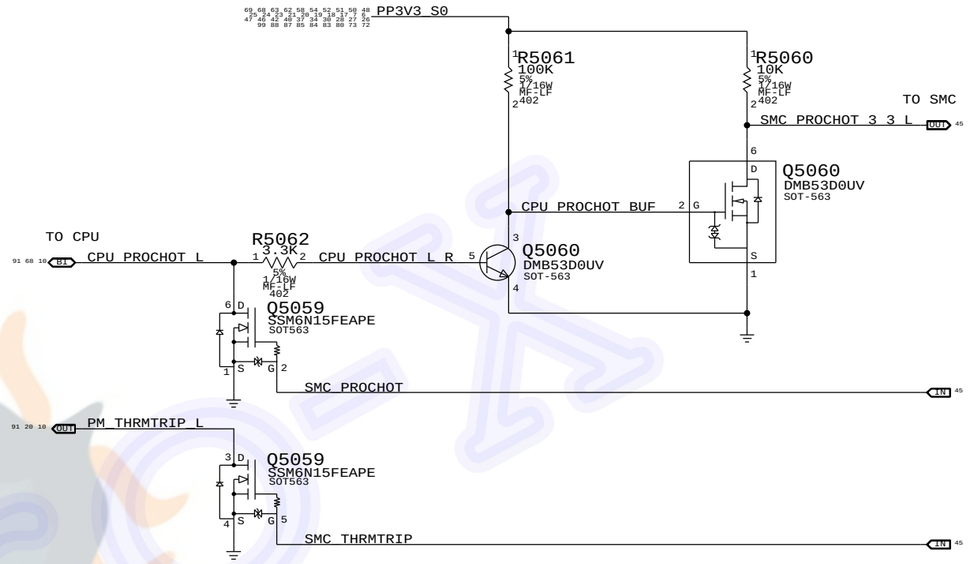
To support timed wake-up events in G3Hot



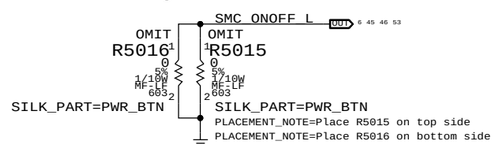
CPU PM_EXTTS_L / MEM_EVENT_L Level Shifting

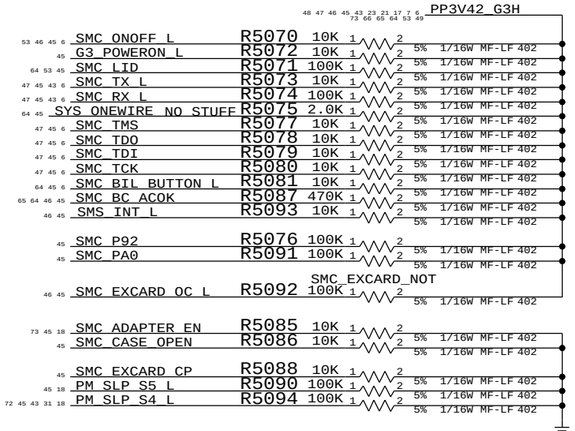


SMC FSB to 3.3V Level Shifting

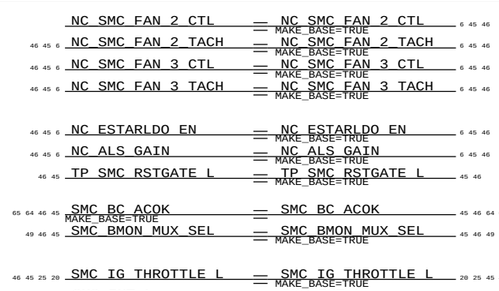


Debug Power "Buttons"





SMC_XXXX



SYNC_MASTER=K18_SENSORS	SYNC_DATE=06/29/2009
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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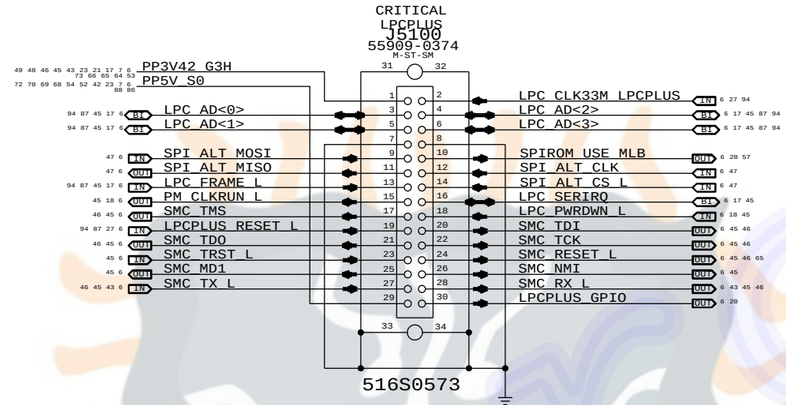
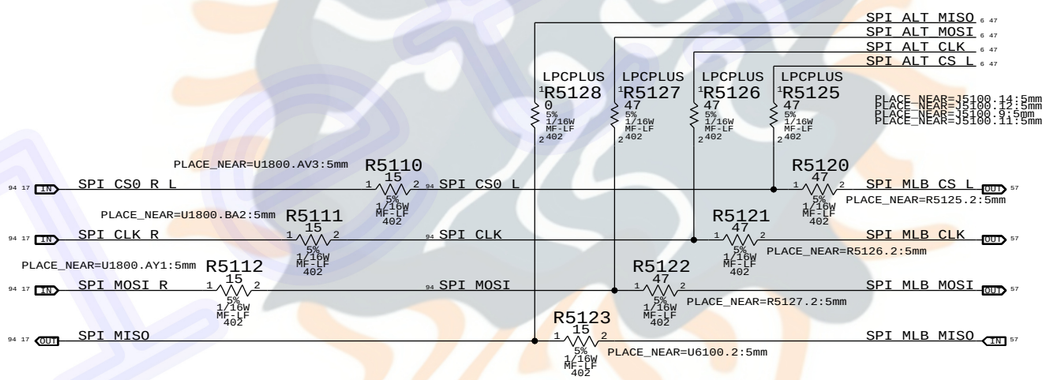
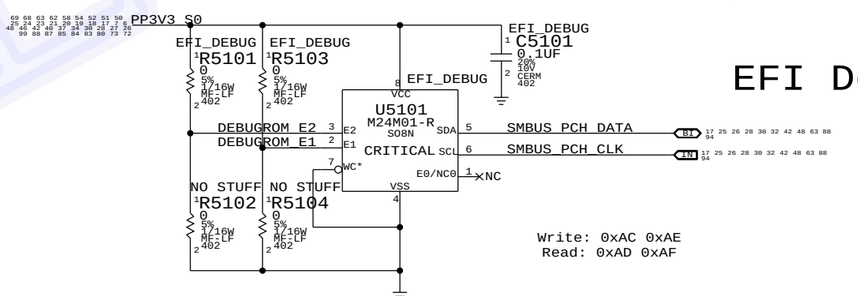
LPC+SPI Connector



SPI Bus Series Termination



EFI Debug ROM



SYNC_MASTER=K17_MLB SYNC_DATE=06/23/2009

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

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PCH SMBus "0" Connections

PP3V3_S0

Ibex Peak-M
U1800
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA
MAKE_BASE=TRUE

R5200 1K 5% 1/16W MF-LF 402
R5201 1K 5% 1/16W MF-LF 402

SO-DIMM "A"
J2900
(Write: 0xA0 Read: 0xA1)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

VRef DACs
U2900
(Write: 0x98 Read: 0x99)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SO-DIMM "B"
J3100
(Write: 0xA4 Read: 0xA5)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Margin Control
U2901
(Write: 0x30 Read: 0x31)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

CK505 (Clock)
U2700
(Write: 0xD2 Read: 0xD3)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

EFI Debug Serial
U5101
(Write: 0xAC/AE Read: 0xAD/AF)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

LED BACKLIGHT
U9701
(WRITE: 0x58 READ: 0x59)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

XDP Connectors
J2600 & J2650
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Mikey
U6800
(Write: 0x72 Read: 0x73)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

HDD Redriver Control A
U4510
(Write: 0x94 Read: 0x95)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

PCH "SMLink 0" Connections

PP3V3_S0

Ibex Peak-M
U1800
(MASTER)
- SML_PCH_0_CLK
- SML_PCH_0_DATA
MAKE_BASE=TRUE

R5210 8.2K 5% 1/16W MF-LF 402
R5211 8.2K 5% 1/16W MF-LF 402

PCH "SMLink 1" Connections

PP3V3_S0

Ibex Peak-M
U1800
(Write: 0x90 Read: 0x91)
- SML_PCH_1_CLK
- SML_PCH_1_DATA
MAKE_BASE=TRUE

NO STUFF
R5220 8.2K 5% 1/16W MF-LF 402
NO STUFF
R5221 8.2K 5% 1/16W MF-LF 402

R5223 0 5% 1/16W MF-LF 402
R5222 0 5% 1/16W MF-LF 402

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

PP3V3_S0

SMC
U4900
(MASTER)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA
MAKE_BASE=TRUE

R5250 4.7K 5% 1/16W MF-LF 402
R5251 4.7K 5% 1/16W MF-LF 402

GPU Temp (Ext)
EMC1414-A: U5550
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

GPU Temp (Int)
GT216: U8000
(Write: 0x9E Read: 0x9F)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S3

SMC
U4900
(MASTER)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA
MAKE_BASE=TRUE

R5270 1K 5% 1/16W MF-LF 402
R5271 1K 5% 1/16W MF-LF 402

Trackpad
J5800
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

ALS
J3401
(Write: 0x72 Read: 0x73)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

SMC "B" SMBus Connections

PP3V3_S0

SMC
U4900
(MASTER)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA
MAKE_BASE=TRUE

R5260 4.7K 5% 1/16W MF-LF 402
R5261 4.7K 5% 1/16W MF-LF 402

CPU Temp
EMC1414-A: U5570
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

SMC "Battery A" SMBus Connections

PP3V42_G3H

SMC
U4900
(MASTER)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA
MAKE_BASE=TRUE

R5280 1K 5% 1/16W MF-LF 402
R5281 1K 5% 1/16W MF-LF 402

Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery
J6955
(See Table)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

PP3V3_S3

SMC
U4900
(MASTER)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA
MAKE_BASE=TRUE

R5290 4.7K 5% 1/16W MF-LF 402
R5291 4.7K 5% 1/16W MF-LF 402

Sensor ADC A
U5930
(Write: 0x10 Read: 0x11)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

SYNC_MASTER=K18_SENSORS SYNC_DATE=06/18/2009

PAGE TITLE
K18 SMBus Connections

Apple Inc.

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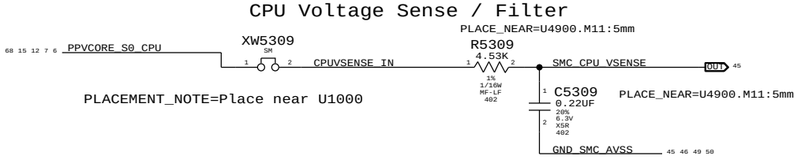
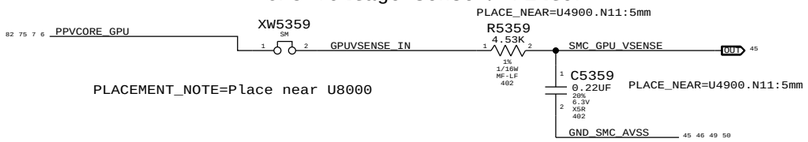
DATE 2009-06-01

CPU Voltage Sense / Filter



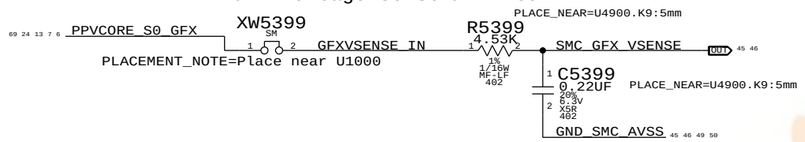
PLACEMENT_NOTE=Place near U1000

GPU Voltage Sense / Filter



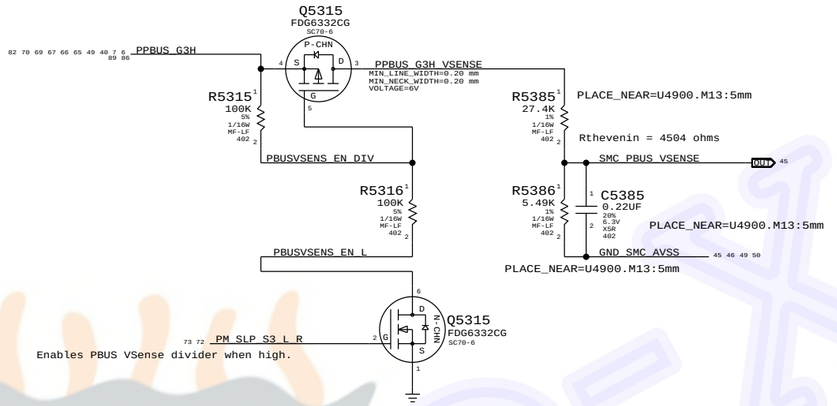
PLACEMENT_NOTE=Place near U8000

GFX Voltage Sense / Filter



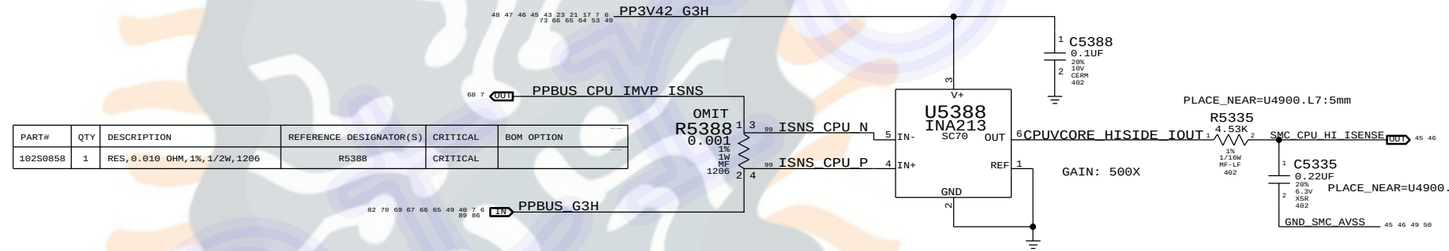
PLACEMENT_NOTE=Place near U1000

PBUS Voltage Sense & Filter



Enables PBUS VSense divider when high.

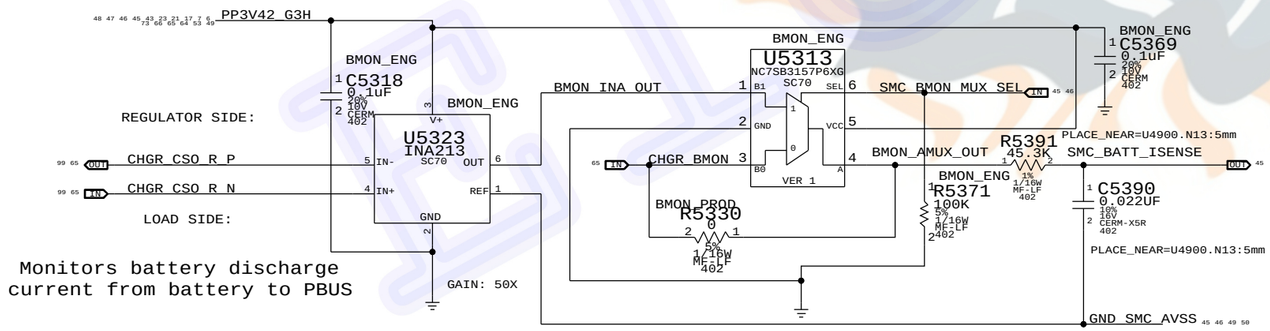
CPU VCore High Side Current Sensor



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
102S0858	1	RES,0.010 OHM,1%,1/2W,1206	R5388	CRITICAL	

EDP for PPVIN_S5_CPU_IMVP_ISNS_R = 5.867 amps for K18.

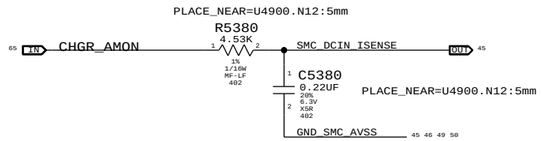
BMON Current Sense - Entire circuit must be near SMC (U4900)



Monitors battery discharge current from battery to PBUS

U5303 only senses current up to 6.6A

DCIN Current Sense Filter



SYNC_MASTER=K18_SENSORS SYNC_DATE=06/29/2009

PAGE TITLE
Current & Voltage Sensing

Apple Inc.

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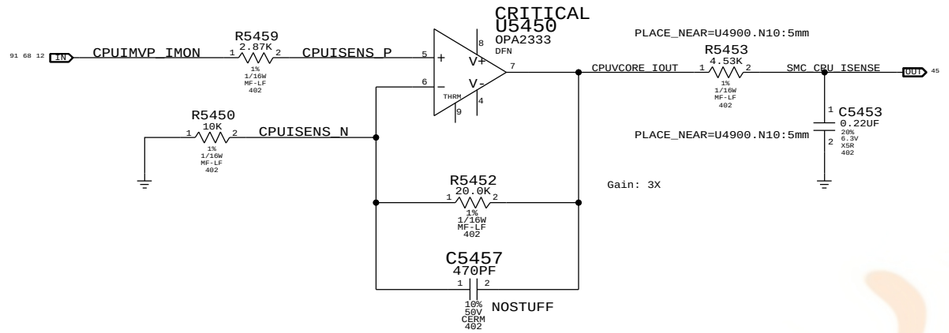
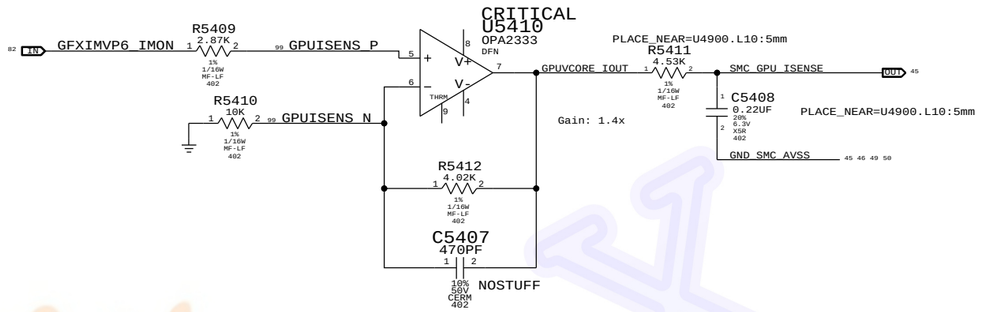
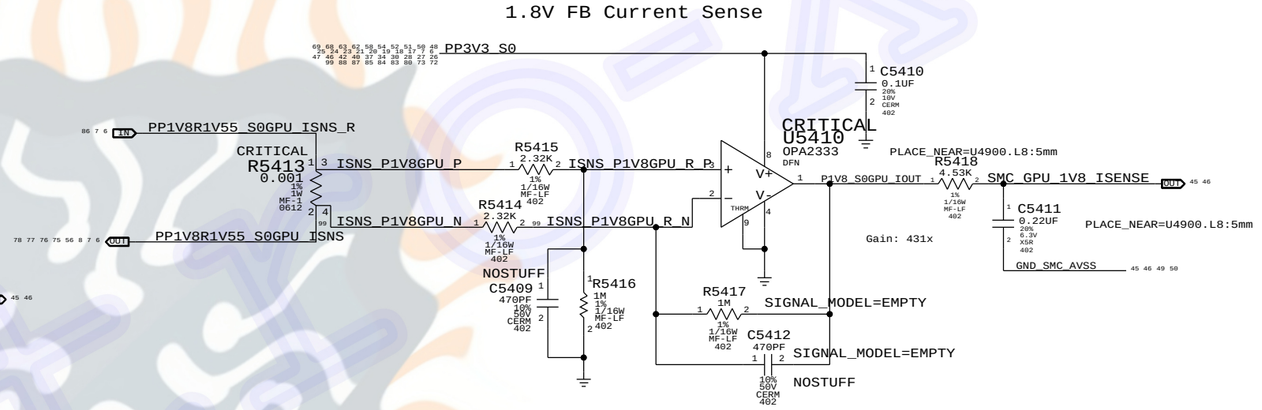
CPU VCore Load Side Current Sense / Filter



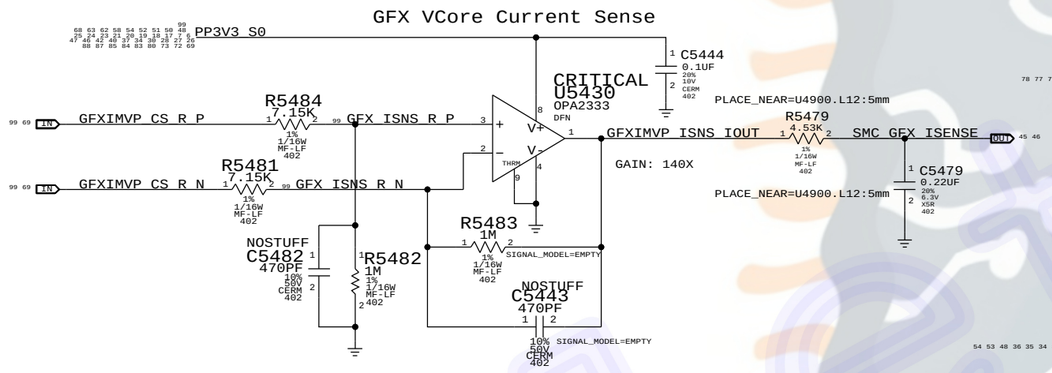
GPU VCore Current Sense



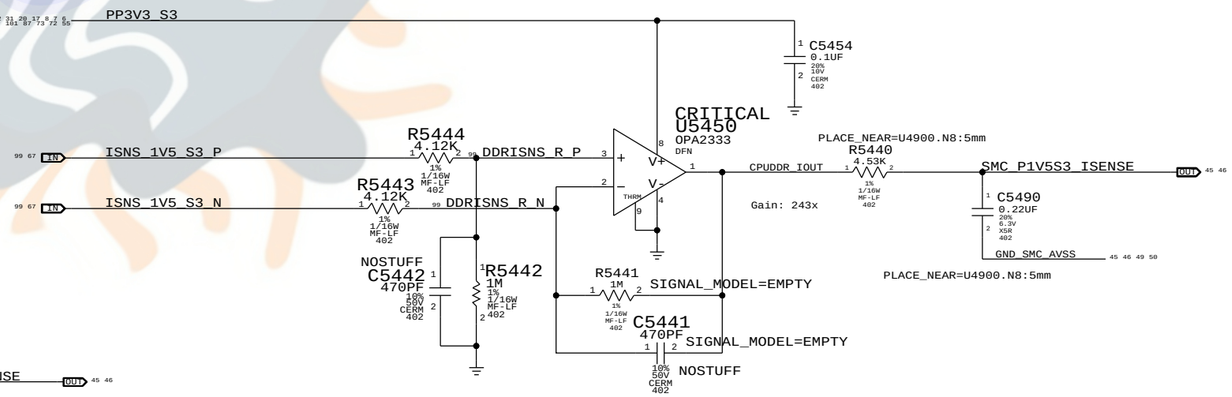
1.8V FB Current Sense



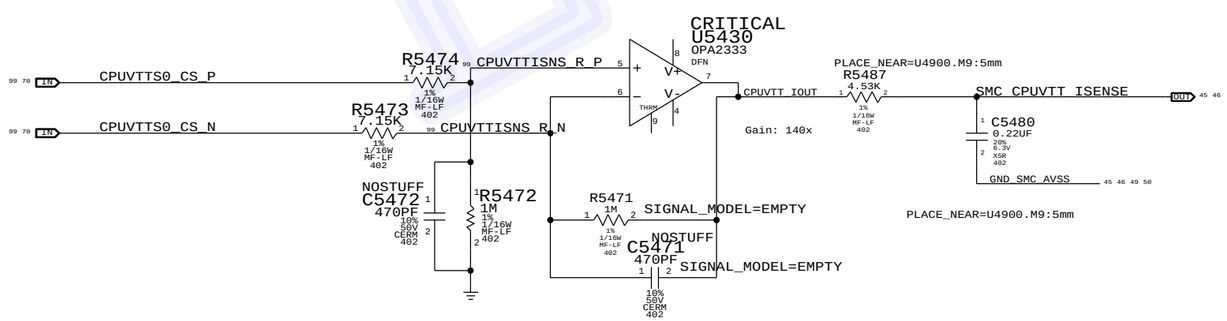
GFX VCore Current Sense



CPU & MEM 1.5V S3 (DDR) Current Sense



CPUVTT 1.05V Current Sense



SYNC_MASTER=K18_SENSORS SYNC_DATE=07/02/2009

PAGE TITLE

Current Sensing

Apple Inc.

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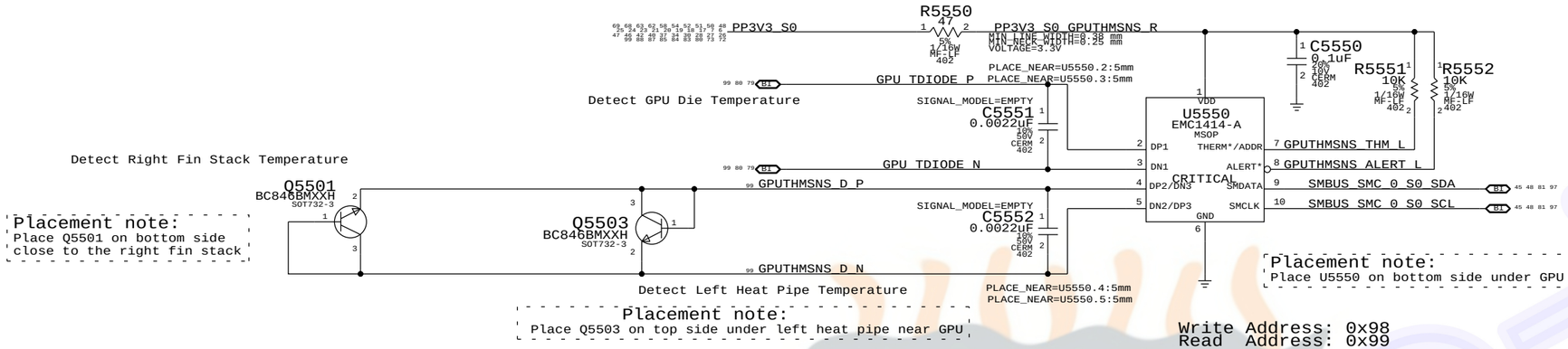
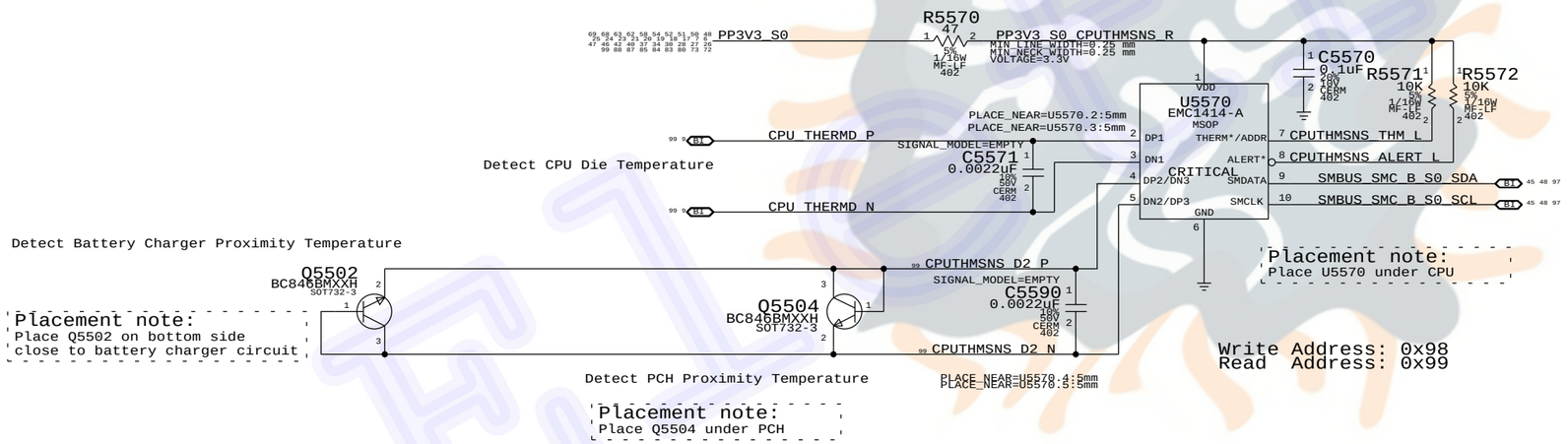
GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack



CPU Proximity/CPU Die/PCH Proximity/Battery Charger Proximity



Note: EMC1414 can perform Beta Compensation for External Diode 1 only

SYNC_MASTER=K18_SENSORS SYNC_DATE=06/18/2009

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

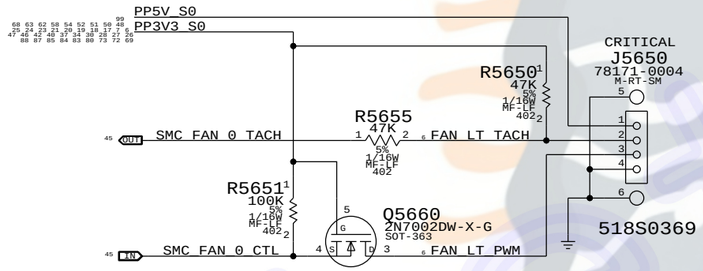
REVISION: <E4LABEL>

BRANCH: <BRANCH>

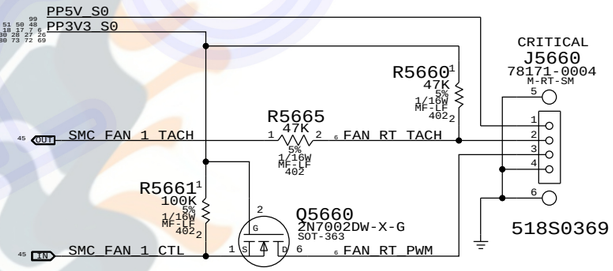
PAGE: 56 OF 132

SHEET: 56 OF 101

Left Fan



Right Fan



SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE
Fan Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 56 OF 132
SHEET 52 OF 101

PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

TRACKPAD PICK BUTTONS
KEYBOARD SCANNER

PP3V3_S3_PSOC 53

PICKB_L 54 6
BUTTON_DISABLE 53
Z2_HOST_INTN 54
WS_LEFT_SHIFT_KEY 53
WS_LEFT_OPTION_KEY 53

WS_KBD23 6 53
WS_KBD22 6 53
WS_KBD21 6 53
WS_KBD20 6 53
WS_KBD19 6 53
WS_KBD18 6 53

56	55	54	53	52	51	50	49
P2_5	P2_7	P0_1	P0_3	P0_5	P0_7	VSS	VDD

48	47	46	45	44	43		
P0_6	P0_4	P0_2	P0_0	P2_6	P2_4		

WS_CONTROL_KEY 53 — 1 P2_3
Z2_KEY_ACT_L 54 6 — 2 P2_1
TP_BOOT_CFG1 — 3 P4_7
TP_P4_5 — 4 P4_5
Z2_DEBUG3 54 6 — 5 P4_3
Z2_RESET 54 6 — 6 P4_1
PSOC_MISO 54 6 — 7 P3_7
PSOC_F_CS_L 54 6 — 8 P3_5
PSOC_MOSI 54 6 — 9 P3_3
PSOC_SCLK 54 6 — 10 P3_1
Z2_MISO 54 6 — 11 P5_7
Z2_CS_L 54 6 — 12 P5_5
Z2_MOSI 54 — 13 P5_3
Z2_SCLK 54 6 — 14 P5_1

P2_2 — 42 — WS_KBD17 6 53
P2_0 — 41 — WS_KBD16N 53
P4_6 — 40 — WS_KBD15_C 53
P4_4 — 39 — WS_KBD14 6 53
P4_2 — 38 — WS_KBD13 6 53
P4_0 — 37 — WS_KBD12 6 53
P3_6 — 36 — WS_KBD11 6 53
P3_4 — 35 — WS_KBD10 6 53
P3_2 — 34 — WS_KBD9 6 53
P3_0 — 33 — WS_KBD8 6 53
P5_6 — 32 — WS_KBD7 6 53
P5_4 — 31 — WS_KBD1 6 53
P5_2 — 30 — WS_KBD2 6 53
P5_0 — 29 — WS_KBD3 6 53
THRMLPAD — 57

CRITICAL
U5701
CY8C24794
MLF
(SYM-VER2)
APN 337S2983
OMIT

15	16	17	18	19	20	21	22	23	24	25	26	27	28	
P1_7	P1_5	P1_3	P1_1	VSS	VD+	D-	VDD	P7_7	P7_0	P1_0	P1_2	P1_4	P1_6	

TP_PSOC_SCL
TP_PSOC_SDA
NC_PSOC_P1_3 6
TP_ISSP_SCLK_P1_1 8 6
ISSP SCLK/I2C SCL

WS_BKD4 6 53
WS_BKD5 6 53
WS_BKD6 6 53
TP_ISSP_SDATA_P1_0
ISSP SDATA/I2C SDA
Z2_CLKIN 6 54
TP_P7_7

DIFFERENTIAL_PAIR=USB2_TPAD
USB_TPAD_P 93 36 — R5701 24 5% 1/16W MF-LF 402 — 1 2 — USB_TPAD_R_P
DIFFERENTIAL_PAIR=USB2_TPAD
NET_SPACING_TYPE=USB
NET_PHYSICAL_TYPE=USB_85D

PP3V3_S3_PSOC 53

TO MLB CONNECTOR
USB_TPAD_N 93 36 — R5702 24 5% 1/16W MF-LF 402 — 1 2 — USB_TPAD_R_N
DIFFERENTIAL_PAIR=USB2_TPAD
NET_SPACING_TYPE=USB
NET_PHYSICAL_TYPE=USB_85D

U5701 CHIP DECOUPLING

PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

PP3V3_S3_PSOC 53
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

R5704 1.5 5% 1/10W MF-LF 603 — 1 2 — PP3V3_S3 7 8 17 20 31 32 33 34 35 36 48 50 53 54 55 72 73 87 101

C5701	C5702	C5703	C5704	C5705	C5706
4.7UF	100PF	0.1UF	100PF	0.1UF	4.7UF
20%	5%	10%	5%	10%	20%
6.3V	50V	16V	50V	16V	6.3V
X5R	C0G	X7R-CERM	C0G	X7R-CERM	X5R
603	402	402	402	402	603

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

ISOLATION CIRCUIT

PP3V42_G3H 49 48 47 46 45 43 23 21 17 7 6 73 66 65 64 53
C5725 0.1UF 20% 10V CERM 402 — 2 1
PP3V3_S3 34 33 32 31 20 17 8 7 6 72 55 54 53 50 48 36 35 101 87 73
WS_LEFT_SHIFT_KBD 53 6
U5725 TC7SZ08AFEAPE SOT665 CRITICAL
WS_LEFT_SHIFT_KEY 53

PP3V42_G3H 48 47 46 45 43 23 21 17 7 6 73 66 65 64 53 49
PP3V3_S3 36 35 34 33 32 31 20 17 8 7 6 101 87 73 72 55 54 53 50 48
WS_LEFT_OPTION_KBD 53 6
U5726 TC7SZ08AFEAPE SOT665 CRITICAL
WS_LEFT_OPTION_KEY 53

PP3V42_G3H 49 48 47 46 45 43 23 21 17 7 6 73 66 65 64 53
PP3V3_S3 48 36 35 34 33 32 31 20 17 8 7 6 101 87 73 72 55 54 53 50
WS_CONTROL_KBD 53 6
U5727 TC7SZ08AFEAPE SOT665 CRITICAL
WS_CONTROL_KEY 53

TPAD BUTTONS DISABLE

BUTTON_DISABLE 53
Q5701 SSM3K15FV SOD-VESM-HF
SMC_LID 64 46 45 IN

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR

J5713
APN 518S0637
NC 32
PP3V3_S3 IN
30 WS_KBD1 53 6
29 WS_KBD2 53 6
28 WS_KBD3 53 6
27 WS_KBD4 53 6
26 WS_KBD5 53 6
25 WS_KBD6 53 6
24 WS_KBD7 53 6
23 WS_KBD8 53 6
22 WS_KBD9 53 6
21 WS_KBD10 53 6
20 WS_KBD11 53 6
19 WS_KBD12 53 6
18 WS_KBD13 53 6
17 WS_KBD14 53 6
16 WS_KBD15_CAP 6
15 WS_KBD16_NUM 6
14 WS_KBD17 53 6
13 WS_KBD18 53 6
12 WS_KBD19 53 6
11 WS_KBD20 53 6
10 WS_KBD21 53 6
9 WS_KBD22 53 6
8 WS_KBD23 53 6
7 WS_KBD_ONOFF_L 6
6 PP3V42_G3H
5 WS_LEFT_SHIFT_KBD 53 6
4 WS_LEFT_OPTION_KBD 53 6
3 WS_CONTROL_KBD 53 6
2 1
NC 31
F-RT-SM
FF14-30A-R11B-B-3H

WS_KBD15_C 53 — R5714 470 1% 1/16W MF-LF 402 — 1 2
WS_KBD16N 53 — R5715 10K 1% 1/16W MF-LF 402 — 1 2
SMC_ONOFF_L 46 45 6 OUT — R5710 1K 5% 1/16W MF-LF 402 — 1 2
C5710 0.1UF 20% 10V CERM 402 — 1 2
PLACEMENT_NOTE=NEAR J5713

SMC_MANUAL_RESET_LOGIC

PP3V42_G3H 48 47 46 45 43 23 21 17 7 6 73 66 65 64 53 49
C5758 0.1UF 10% 10V X7R-CERM 402 — 1 2

APN 311S0406
CRITICAL
U5703 SN74LVC1G10 SC70

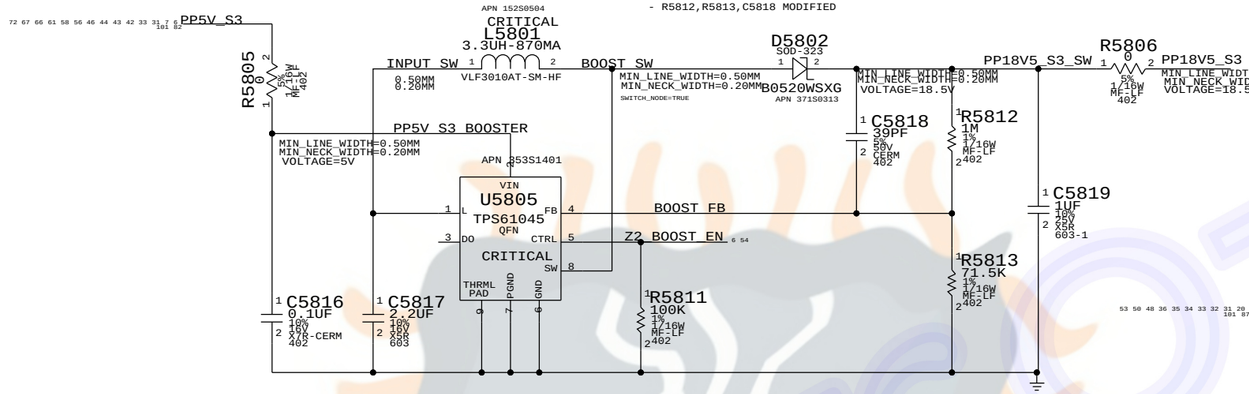
WS_LEFT_SHIFT_KBD 53 6
WS_LEFT_OPTION_KBD 53 6
WS_CONTROL_KBD 53 6
SMC_TPAD_RST_L 46

R5769 33K 5% 1/16W MF-LF 402 — 1 2
R5770 33K 5% 1/16W MF-LF 402 — 1 2
R5771 33K 5% 1/16W MF-LF 402 — 1 2

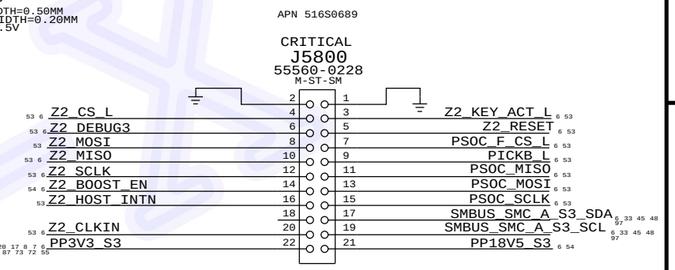
SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009
PAGE TITLE: WELLSPRING 1
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 5 OF 132

BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



Keyboard LED Driver

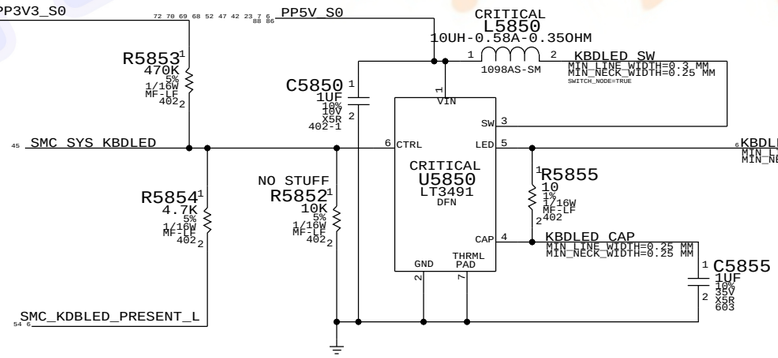
To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

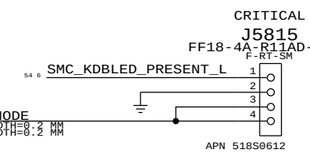
LOW = keyboard backlight present

HIGH= keyboard backlight not present

BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT





J5815 pin 1 is grounded on keyboard backlight flex

KBD BACKLIGHT CONNECTOR

SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

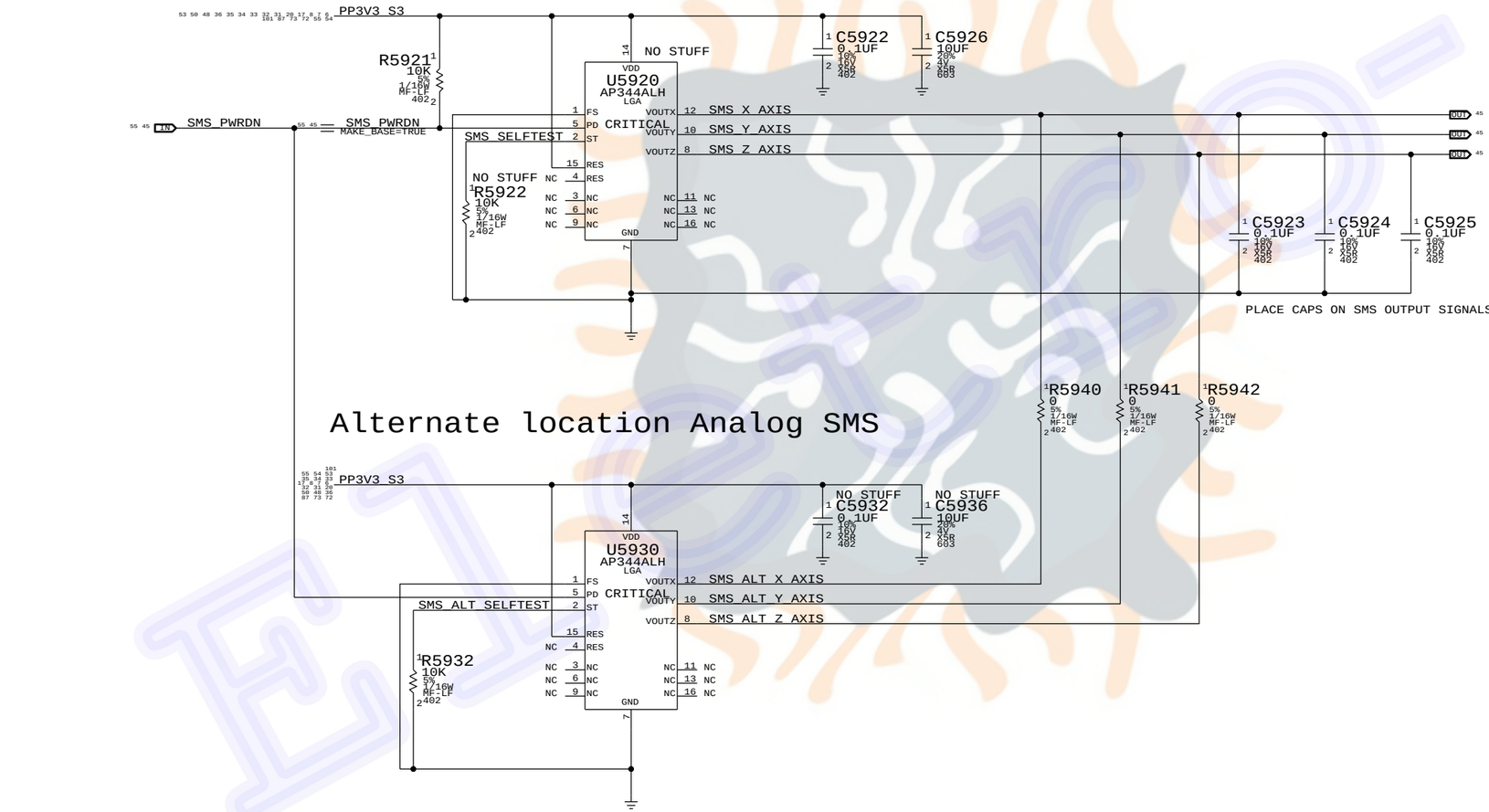
BRANCH: <BRANCH>

PAGE: 58 OF 132

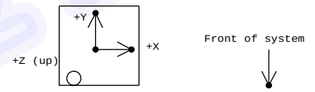
SCALE: 5 4 3 2 1

Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



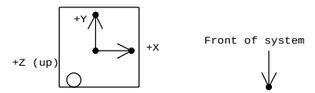
Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

Alternate location Analog SMS

Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE: Sudden Motion Sensor (SMS)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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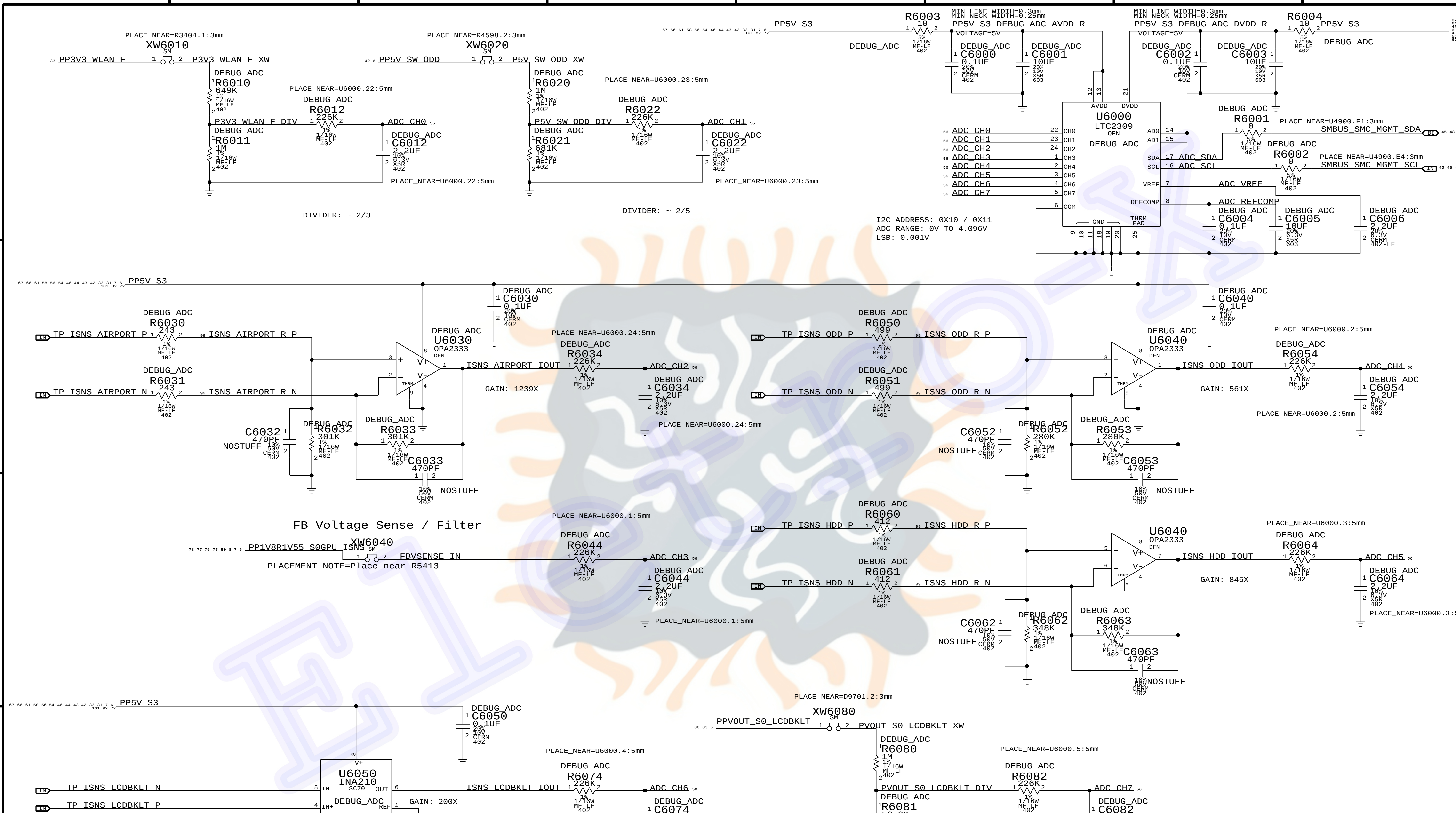

XW6010
P3V3_WLAN_F
P3V3_WLAN_F_XW
R6010 649K
R6011 1M
P3V3_WLAN_F_DIV
R6012 226K
ADC_CH0
C6012 2.2UF
DIVIDER: ~ 2/3
XW6020
PP5V_SW_ODD
P5V_SW_ODD_XW
R6020 1M
R6021 681K
P5V_SW_ODD_DIV
R6022 226K
ADC_CH1
C6022 2.2UF
DIVIDER: ~ 2/5
PP5V_S3
R6003 10
PP5V_S3_DEBUG_ADC_AVDD_R
C6000 0.1UF
C6001 10UF
R6004 10
PP5V_S3_DEBUG_ADC_DVDD_R
C6002 0.1UF
C6003 10UF
U6000
LTC2309
QFN
R6001 0
SMBUS_SMC_MGMT_SDA
R6002 0
SMBUS_SMC_MGMT_SCL
ADC_SDA
ADC_SCL
ADC_VREF
ADC_REFCOMP
C6004 0.1UF
C6005 10UF
C6006 2.2UF
I2C ADDRESS: 0X10 / 0X11
ADC RANGE: 0V TO 4.096V
LSB: 0.001V
TP_ISNS_AIRPORT_P
TP_ISNS_AIRPORT_N
R6030 243
R6031 243
ISNS_AIRPORT_R_P
ISNS_AIRPORT_R_N
U6030
OPA2333
C6030 0.1UF
ISNS_AIRPORT_IOUT
R6034 226K
ADC_CH2
C6034 2.2UF
GAIN: 1239X
C6032 470PF
R6032 301K
R6033 301K
C6033 470PF
NOSTUFF
TP_ISNS_ODD_P
TP_ISNS_ODD_N
R6050 499
R6051 499
ISNS_ODD_R_P
ISNS_ODD_R_N
U6040
C6040 0.1UF
ISNS_ODD_IOUT
R6054 226K
ADC_CH4
C6054 2.2UF
GAIN: 561X
C6052 470PF
R6052 280K
R6053 280K
C6053 470PF
FB Voltage Sense / Filter
PP1V8R1V55_S0GPU_ISNS
XW6040
FBVSENSE_IN
PLACEMENT_NOTE=Place near R5413
R6044 226K
ADC_CH3
C6044 2.2UF
TP_ISNS_HDD_P
TP_ISNS_HDD_N
R6060 412
R6061 412
ISNS_HDD_R_P
ISNS_HDD_R_N
U6040
OPA2333
ISNS_HDD_IOUT
R6064 226K
ADC_CH5
C6064 2.2UF
GAIN: 845X
C6062 470PF
R6062 348K
R6063 348K
C6063 470PF
C6050 0.1UF
U6050
INA210
TP_ISNS_LCDBKLT_N
TP_ISNS_LCDBKLT_P
ISNS_LCDBKLT_IOUT
GAIN: 200X
R6074 226K
ADC_CH6
C6074 2.2UF
XW6080
PPVOUT_S0_LCDBKLT
PPVOUT_S0_LCDBKLT_XW
R6080 1M
R6081 52.3K
PPVOUT_S0_LCDBKLT_DIV
R6082 226K
ADC_CH7
C6082 2.2UF
DIVIDER: ~ 1/20

SYNC_MASTER=K18_SENSORS SYNC_DATE=07/07/2009

PAGE TITLE

DEBUG SENSORS AND ADC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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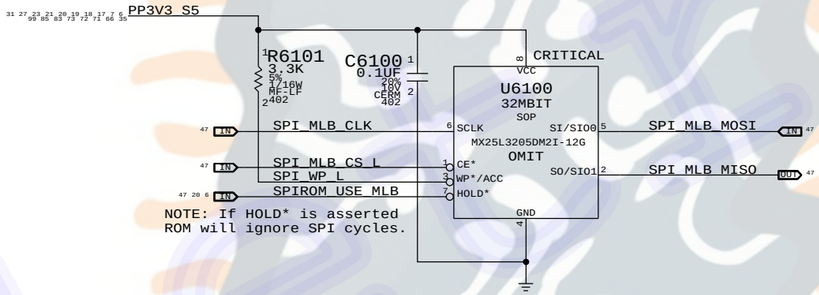
SHEET 56 OF 101



SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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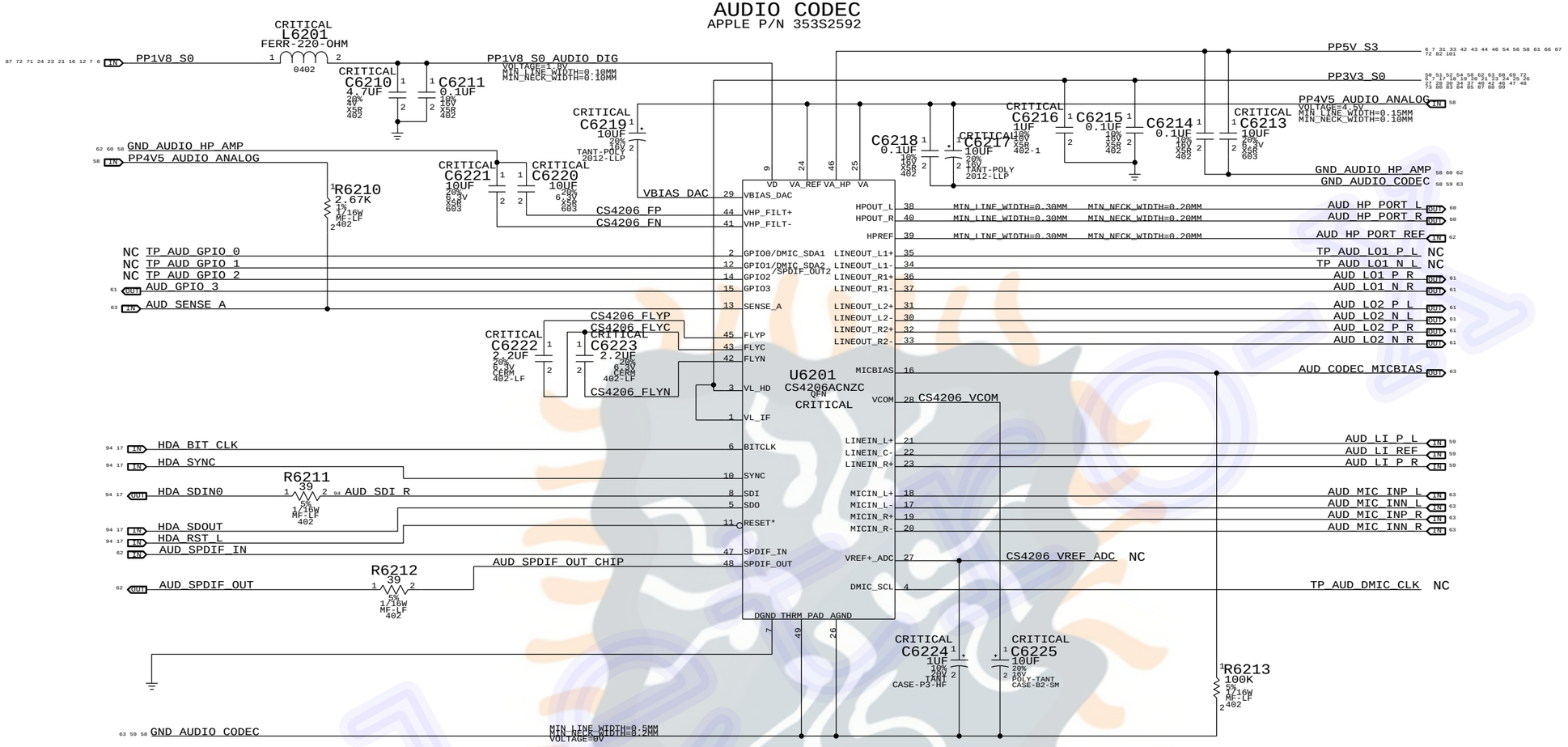
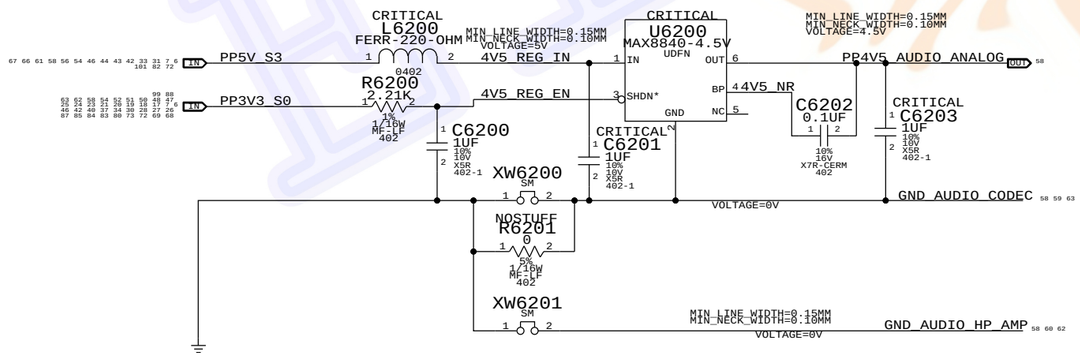
AUDIO CODEC
APPLE P/N 353S2592



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2234



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=K18_AUDIO SYNC_DATE=09/21/2009

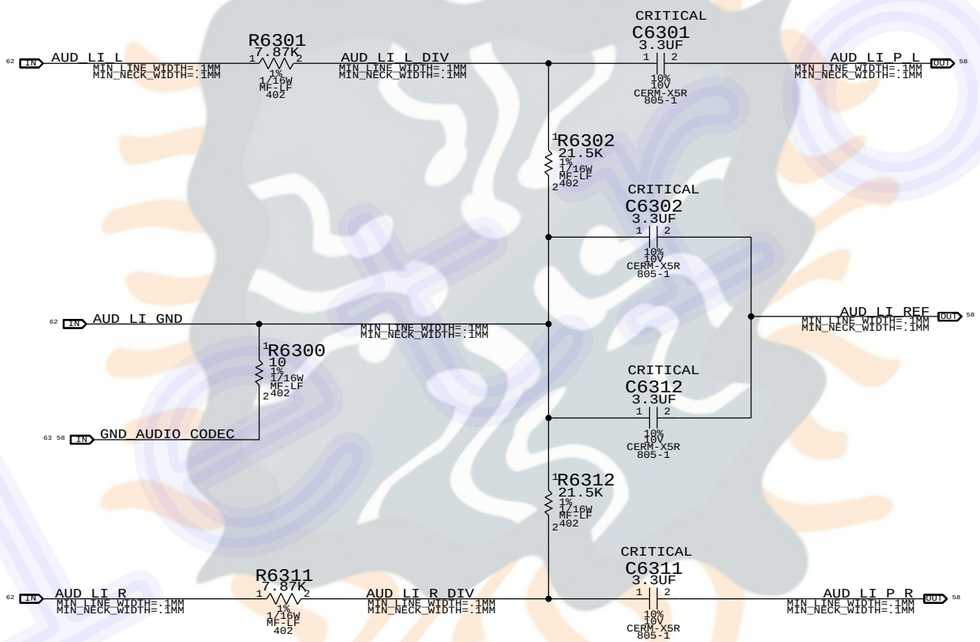
PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 62 OF 132
SHEET 58 OF 101

LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 18K OHMS
FC = 8 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



SYNC_MASTER=K18_AUDIO SYNC_DATE=07/29/2009

PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 63 OF 132
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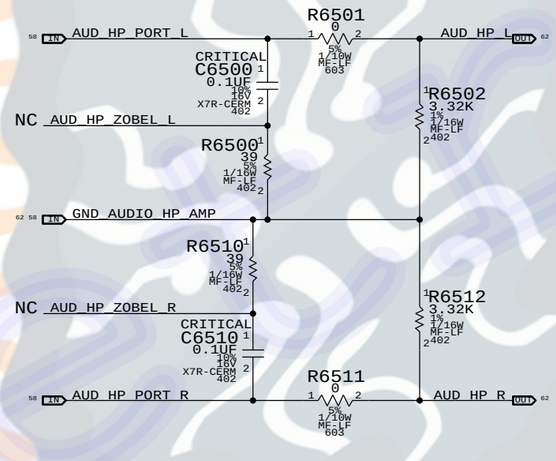
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=K18_AUDIO SYNC_DATE=07/29/2009

PAGE TITLE
AUDIO: HEADPHONE FILTER

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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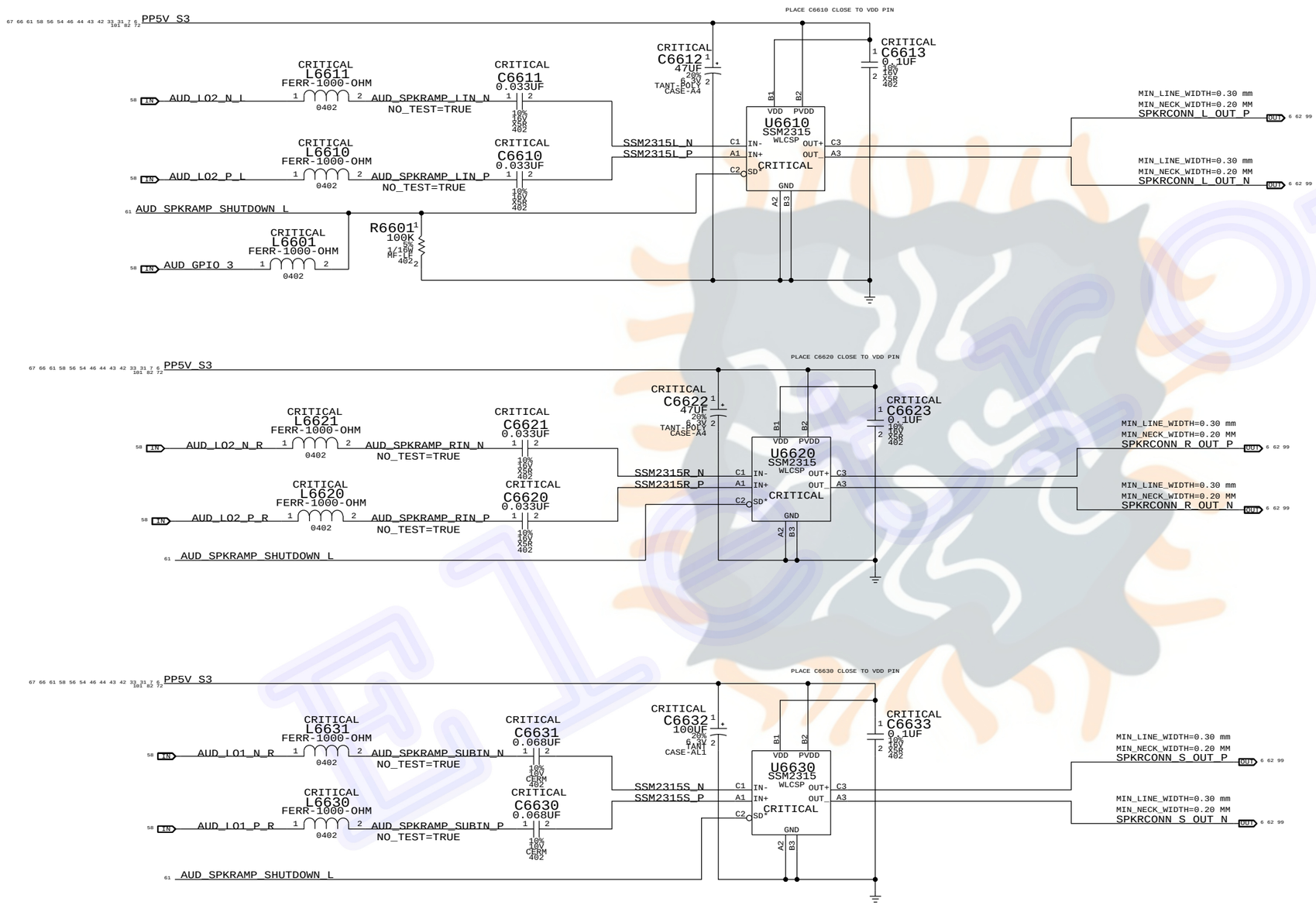
SHEET 60 OF 101

3X MONO SPEAKER AMPLIFIERS (SSM2315)
APN: 353S2500

GAIN = 6DB
1ST ORDER FC (L&R) = 120 HZ +/- 30%
1ST ORDER FC (SUB) = 58HZ +/- 30%



SYNC_MASTER=K18_AUDIO SYNC_DATE=07/29/2009

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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ECN 61 OF 201

AUDIO JACK 1 LO/HP JACK, SPDIF TX

PP3V3_S0

APN: 514-0671

J6700
SPDIF-TXRX-K24
F-RT-TH

AUDIO
MIC
DETECT
SWITCH
LEFT
RIGHT
GND
SHELL
SHIELD PINS

AUD_CONNJ1_SLEEVE2
AUD_CONNJ1_SLEEVEDET
AUD_CONNJ1_TIPDET
AUD_CONNJ1_TIP
AUD_CONNJ1_RING
AUD_CONNJ1_SLEEVE

A - VIN
B - VCC
C - GND
OPERATING VOLTAGE 3.3
POF

C6700 0.1UF 10% 10V X5R 402
C6701 2.2UF 20% 6.3V CERM 402-LF

AUD_SPDIF_OUT
L6703 FERR-1000-OHM CRITICAL 0402
HS_MIC_P
L6702 FERR-1000-OHM CRITICAL 0402
HS_MIC_N
L6707 CRITICAL FERR-220-OHM 0402
AUD_HP_PORT_REF
L6701 CRITICAL FERR-220-OHM-2.5A 0603
GND_AUDIO_HP_AMP
L6704 CRITICAL FERR-220-OHM 0402
AUD_HP_R
L6706 CRITICAL FERR-220-OHM 0402
AUD_HP_L
R6700 10K 5% 1/16W MF-LF 402
AUD_J1_SLEEVEDET_R
L6705 FERR-1000-OHM CRITICAL 0402
AUD_J1_TIPDET_R

DZ6703 CRITICAL 6.8V-100PF 402
DZ6704 CRITICAL 6.8V-100PF 402
DZ6700 CRITICAL 6.8V-100PF 402
DZ6706 CRITICAL 6.8V-100PF 402
DZ6701 CRITICAL 6.8V-100PF 402

C6705 100PF 5% 50V CERM 402

MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.10 MM
VOLTAGE=0V

GND_CHASSIS_AUDIO_JACK

XW6701 SM
XW6702 SM
GND PATCH
R6701 0 5% 1/16W MF-LF 402
GND_CHASSIS_AUDIO_JACK

MIC CONNECTOR

APN: 518S0520

J6780 CRITICAL
78171-0003
M-RT-SM

BI_MIC_N
BI_MIC_SHIELD
BI_MIC_P

SPEAKER CONNECTOR

APN: 518S0519

J6781 CRITICAL
78171-0002
M-RT-SM

SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N

J6782 CRITICAL
78171-0004
M-RT-SM

APN: 518S0521

SPKRCONN_S_OUT_P
SPKRCONN_S_OUT_N
SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N

NOSTUFF CRITICAL C6781 33PF 5% 50V CERM 402
NOSTUFF CRITICAL C6782 33PF 5% 50V CERM 402
NOSTUFF CRITICAL C6783 33PF 5% 50V CERM 402
NOSTUFF CRITICAL C6784 33PF 5% 50V CERM 402

AUDIO JACK 2 LINE IN JACK, SPDIF RX

PP3V3_S0

APN: 514-0635

J6750
AUDIO-RCVR-M97
F-RT-TH5

DETECT_FOR_PLUG_TYPE
SWITCH
LEFT
RIGHT
GROUND
AUDIO
SHELL
SHIELD PINS

AUD_J2_OPT_OUT
R6749 4.7 5% 1/16W MF-LF 402
AUD_SPDIF_IN

AUD_CONNJ2_TIPDET
AUD_CONNJ2_RING
AUD_CONNJ2_TIP
AUD_CONNJ2_SLEEVE

A - VDD
B - GND
C - VOUT
OPERATING VOLTAGE 3.3
POF

C6750 1UF 10% 10V X5S 402-1

L6754 CRITICAL FERR-1000-OHM 0402
AUD_LI_R
L6756 CRITICAL FERR-1000-OHM 0402
AUD_LI_L
L6758 CRITICAL 600-OHM-300MA 0402
AUD_LI_GND
L6752 CRITICAL FERR-1000-OHM 0402
AUD_J2_TIPDET_R

DZ6758 CRITICAL ESDALC5-1BM2 SOD882
DZ6757 CRITICAL ESDALC5-1BM2 SOD882
DZ6754 CRITICAL 6.8V-100PF 402
DZ6756 CRITICAL 6.8V-100PF 402

C6756 100PF 5% 50V CERM 402

GND_CHASSIS_AUDIO_JACK

SYNC_MASTER=K18_AUDIO SYNC_DATE=07/29/2009

PAGE TITLE: AUDIO: JACKS

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 67 OF 132
SHEET: 02 OF 01

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

PORT B LEFT(HEADSET MIC)
CRITICAL HP=80HZ, LP=8.82KHZ
MIKEY MIN_LINE_WIDTH=0.1MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=3.3V
DRC MIKEY
APN:353S2256
PULLUPS ON MCP PAGE
PORT A DETECT (HEADPHONES)
PORT B DETECT(SPDIF DELEGATE)
APN:376S0613
EXTRACTION NOTIFICATION
PORT B RIGHT(BUILT-IN MIC)
HP=80HZ
PORT C DETECT (LINE-IN)
APN:376S0612

SYNC_MASTER=K18_AUDIO SYNC_DATE=07/29/2009

PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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BRANCH <BRANCH>
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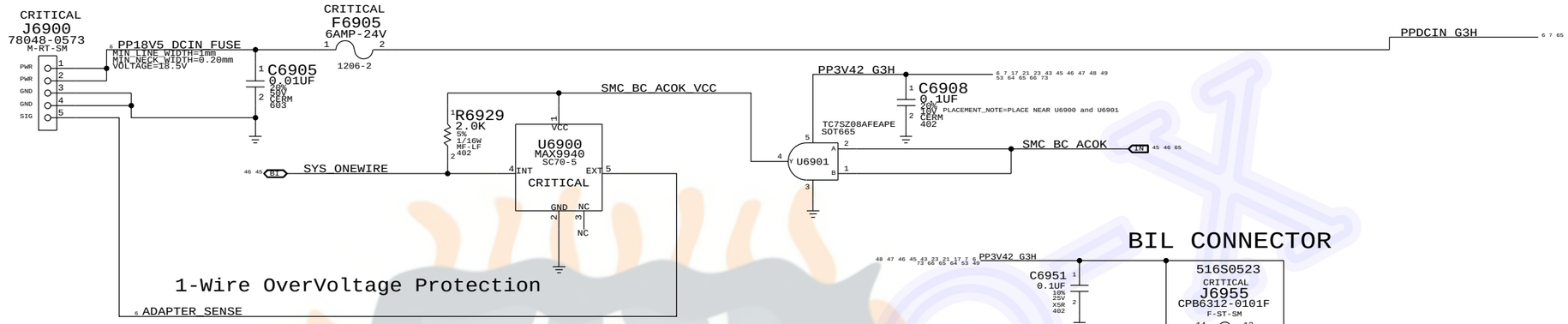
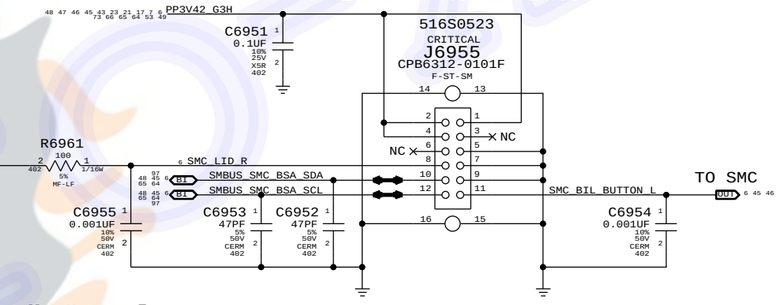
MagSafe DC Power Jack



1-Wire OverVoltage Protection

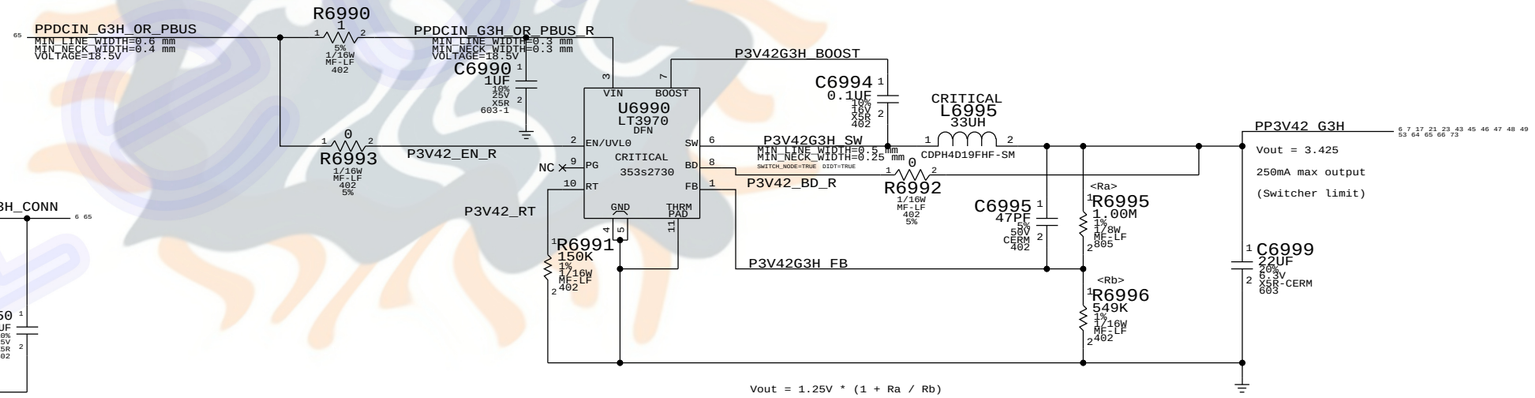
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

BIL CONNECTOR



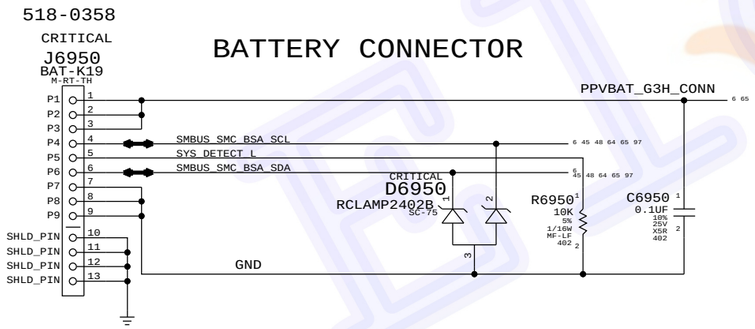
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



Vout = 1.25V * (1 + Ra / Rb)

BATTERY CONNECTOR



SYNC_MASTER=K18_POWER	SYNC_DATE=06/30/2009
PAGE TITLE: DC-In & Battery Connectors	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 69 OF 132
	SHEET: 64 OF 101

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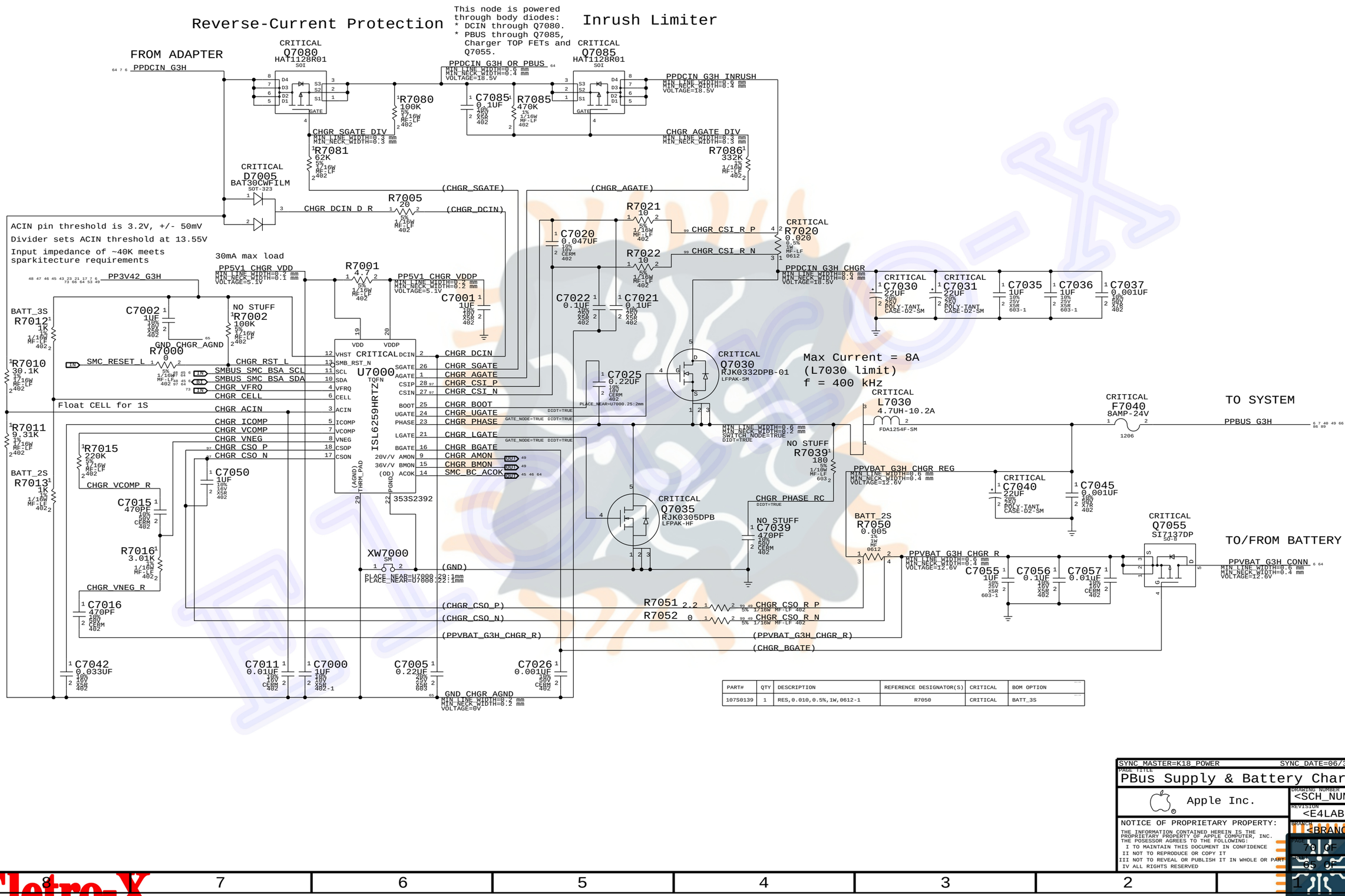

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0139	1	RES,0.010,0.5%,1W,0612-1	R7050	CRITICAL	BATT_3S

SYNC_MASTER=K18_POWER SYNC_DATE=06/30/2009

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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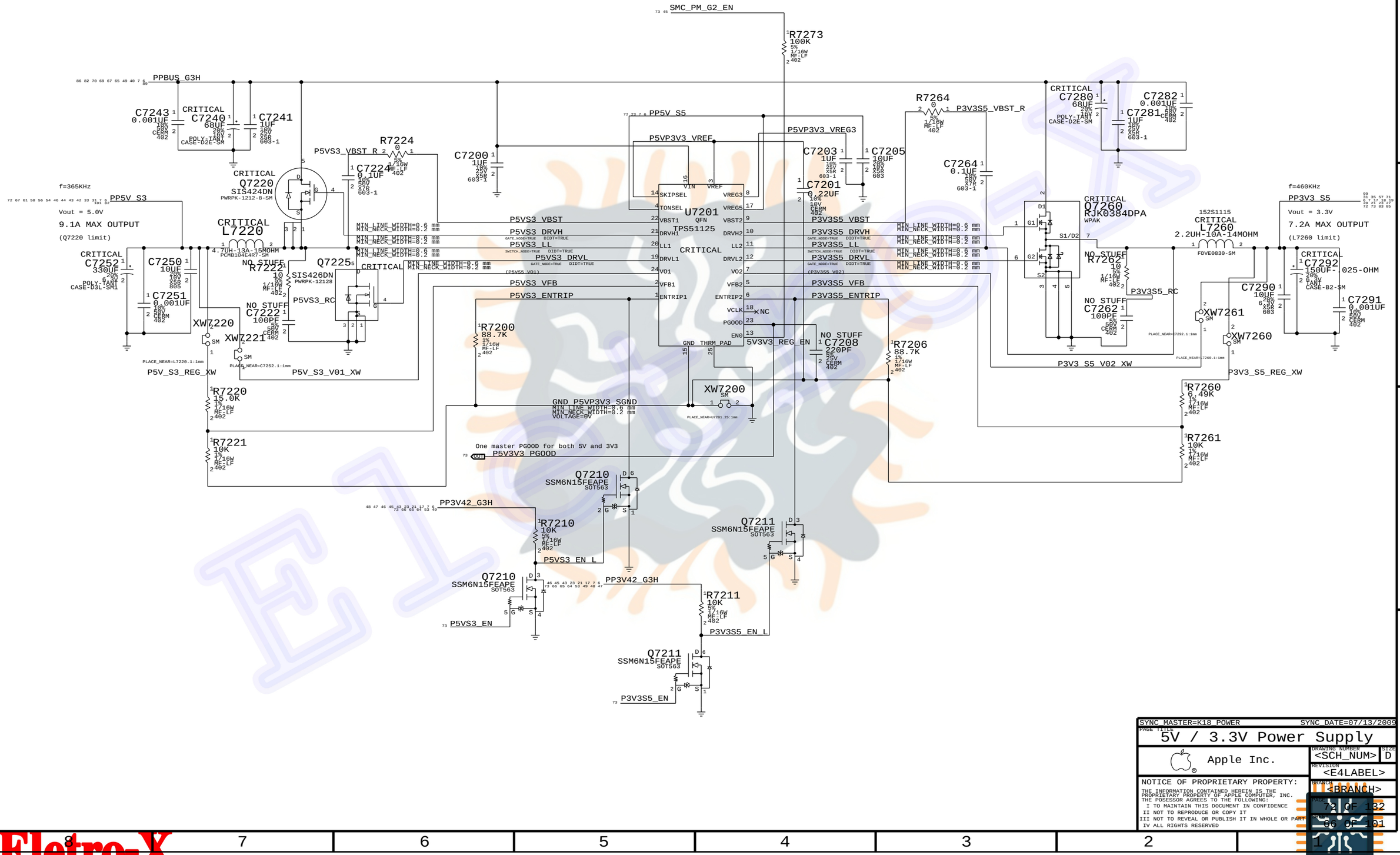

SYNC_MASTER=K18_POWER SYNC_DATE=07/13/2009

PAGE TITLE: 5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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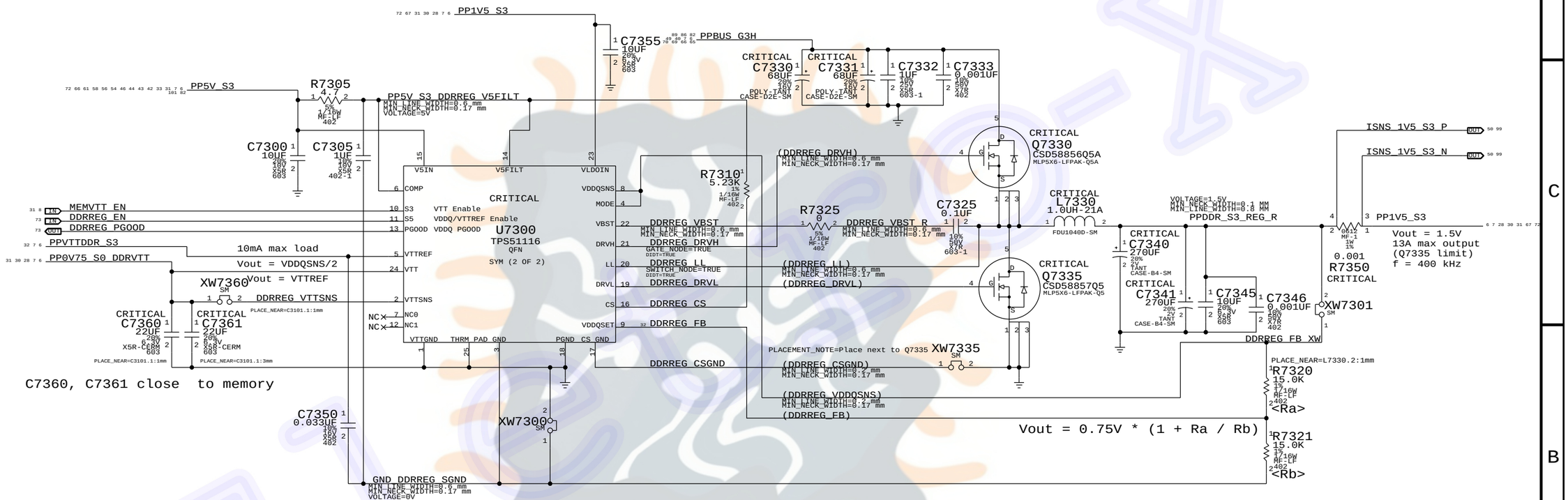

SYNC_MASTER=K18_POWER	SYNC_DATE=07/14/2009
PAGE TITLE	1.5V DDR3 Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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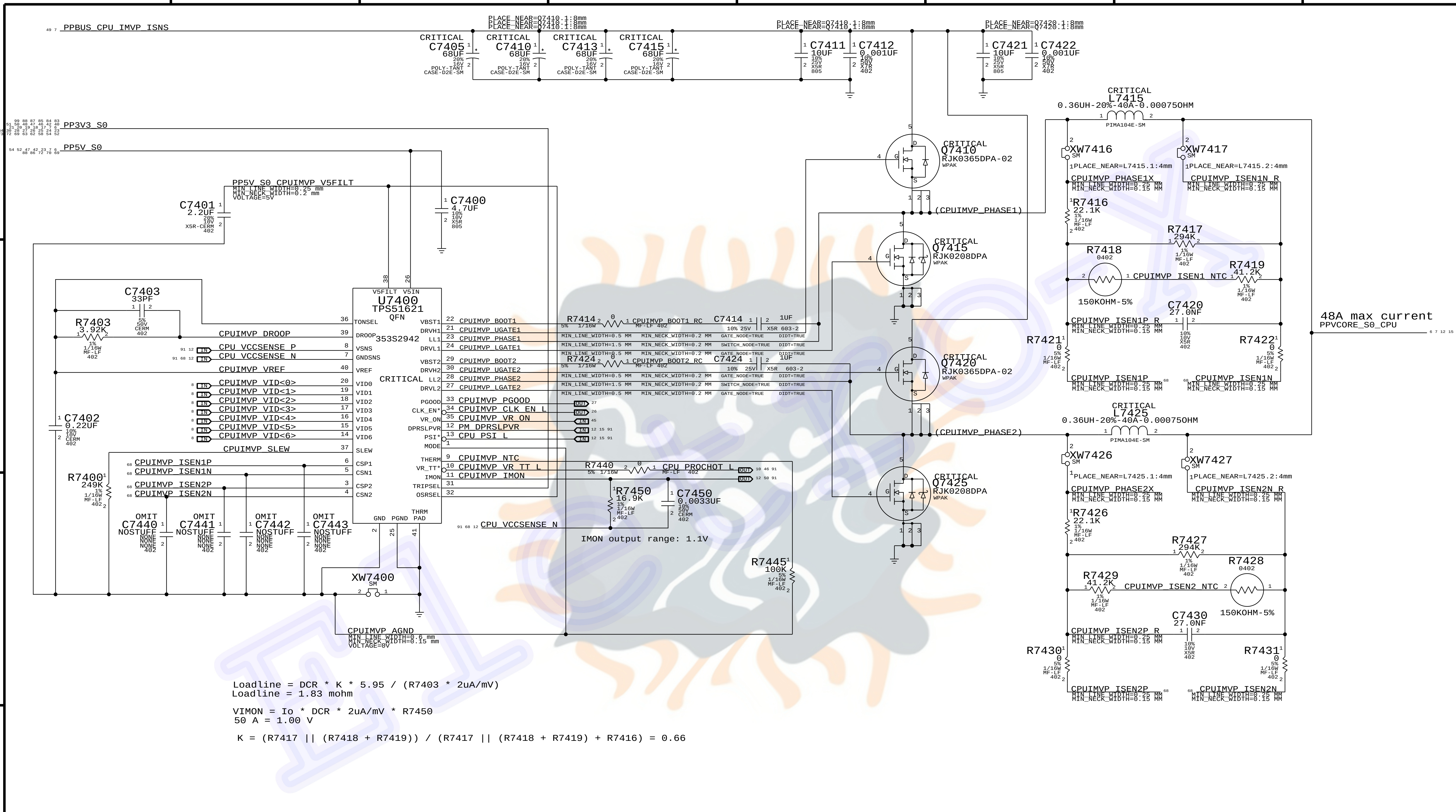
	SHEET 67 OF 101



PPBUS_CPU_IMVP_ISNS
PP3V3_S0
PP5V_S0
PP5V_S0_CPUIMVP_V5FILT
CRITICAL C7405 68UF
CRITICAL C7410 68UF
CRITICAL C7413 68UF
CRITICAL C7415 68UF
PLACE_NEAR=Q7410.1:8mm
PLACE_NEAR=Q7420.1:8mm
C7411 10UF
C7412 0.001UF
C7421 10UF
C7422 0.001UF
CRITICAL L7415 0.36UH-20%-40A-0.00075OHM
CRITICAL Q7410 RJK0365DPA-02
CRITICAL Q7415 RJK0208DPA
CRITICAL Q7420 RJK0365DPA-02
CRITICAL Q7425 RJK0208DPA
CRITICAL L7425 0.36UH-20%-40A-0.00075OHM
(CPUIMVP_PHASE1)
(CPUIMVP_PHASE2)
C7401 2.2UF
C7400 4.7UF
C7403 33PF
R7403 3.92K
C7402 0.22UF
R7400 249K
U7400 TPS51621 QFN 353S2942 CRITICAL
CPUIMVP_DROOP
CPU_VCCSENSE_P
CPU_VCCSENSE_N
CPUIMVP_VREF
CPUIMVP_VID<0>
CPUIMVP_VID<1>
CPUIMVP_VID<2>
CPUIMVP_VID<3>
CPUIMVP_VID<4>
CPUIMVP_VID<5>
CPUIMVP_VID<6>
CPUIMVP_SLEW
CPUIMVP_ISEN1P
CPUIMVP_ISEN1N
CPUIMVP_ISEN2P
CPUIMVP_ISEN2N
CPUIMVP_BOOT1
CPUIMVP_UGATE1
CPUIMVP_PHASE1
CPUIMVP_LGATE1
CPUIMVP_BOOT2
CPUIMVP_UGATE2
CPUIMVP_PHASE2
CPUIMVP_LGATE2
CPUIMVP_PGOOD
CPUIMVP_CLK_EN_L
CPUIMVP_VR_ON
PM_DPRSLPVR
CPU_PSI_L
CPUIMVP_NTC
CPUIMVP_VR_TT_L
CPUIMVP_IMON
R7414 0
CPUIMVP_BOOT1_RC
C7414 1UF
R7424 0
CPUIMVP_BOOT2_RC
C7424 1UF
R7440 0
CPU_PROCHOT_L
R7450 16.9K
C7450 0.0033UF
IMON output range: 1.1V
R7445 100K
CPU_VCCSENSE_N
OMIT C7440 NOSTUFF
OMIT C7441 NOSTUFF
OMIT C7442 NOSTUFF
OMIT C7443 NOSTUFF
XW7400 SM
CPUIMVP_AGND
XW7416 SM
XW7417 SM
CPUIMVP_PHASE1X
CPUIMVP_ISEN1N_R
R7416 22.1K
R7417 294K
R7418 0402 150KOHM-5%
CPUIMVP_ISEN1_NTC
R7419 41.2K
C7420 27.0NF
CPUIMVP_ISEN1P_R
R7421 0
R7422 0
CPUIMVP_ISEN1P
CPUIMVP_ISEN1N
48A max current
PPVCORE_S0_CPU
XW7426 SM
XW7427 SM
PLACE_NEAR=L7425.1:4mm
PLACE_NEAR=L7425.2:4mm
CPUIMVP_PHASE2X
CPUIMVP_ISEN2N_R
R7426 22.1K
R7427 294K
R7428 0402 150KOHM-5%
R7429 41.2K
CPUIMVP_ISEN2_NTC
C7430 27.0NF
CPUIMVP_ISEN2P_R
R7430 0
R7431 0
CPUIMVP_ISEN2P
CPUIMVP_ISEN2N

Loadline = DCR * K * 5.95 / (R7403 * 2uA/mV)
Loadline = 1.83 mohm

VIMON = Io * DCR * 2uA/mV * R7450
50 A = 1.00 V

K = (R7417 || (R7418 + R7419)) / (R7417 || (R7418 + R7419) + R7416) = 0.66

SYNC_MASTER=K18_POWER SYNC_DATE=06/29/2009

CPU IMVP VCore Regulator

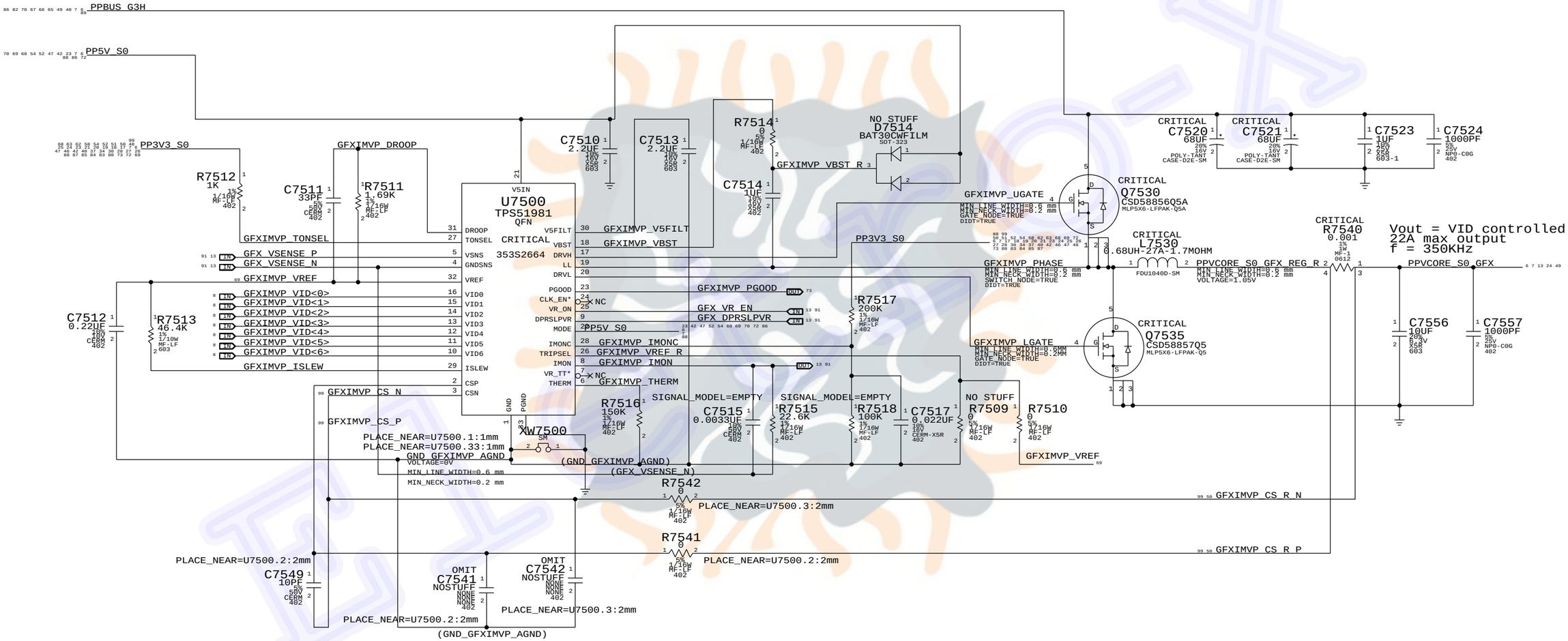
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

GFX IMVP VCORE



Imon= Io xR7540 x2uA/mV x R7515

Imon= Io x45.2mV/A

22A => 1V

SYNC_MASTER=K18_POWER SYNC_DATE=07/08/2009

PAGE TITLE: GFX IMVP VCore Regulator

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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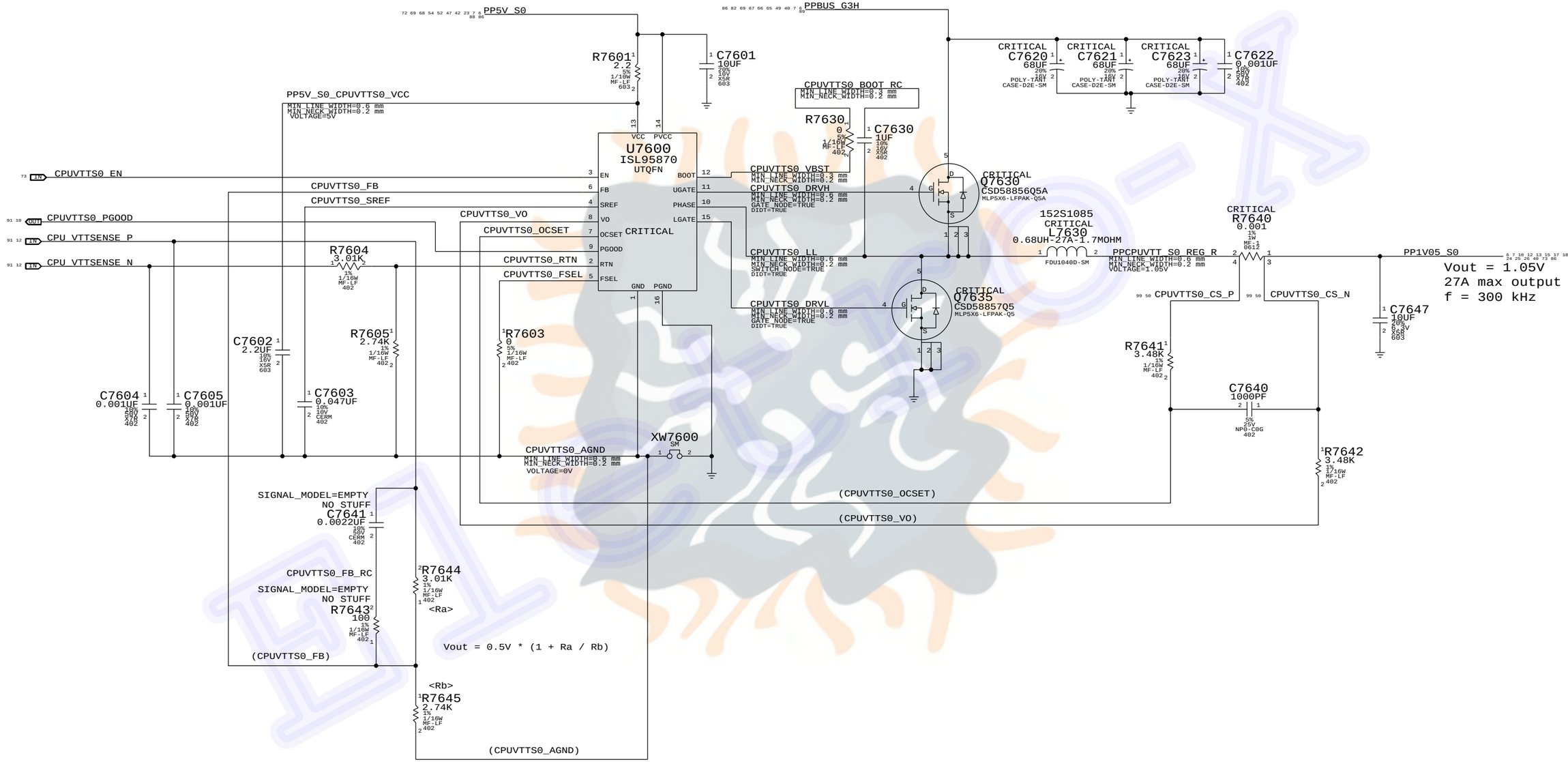
CPU VTT (1.05V S0) Regulator



SYNC_MASTER=K18_POWER SYNC_DATE=07/14/2009

PAGE TITLE
CPUVTT (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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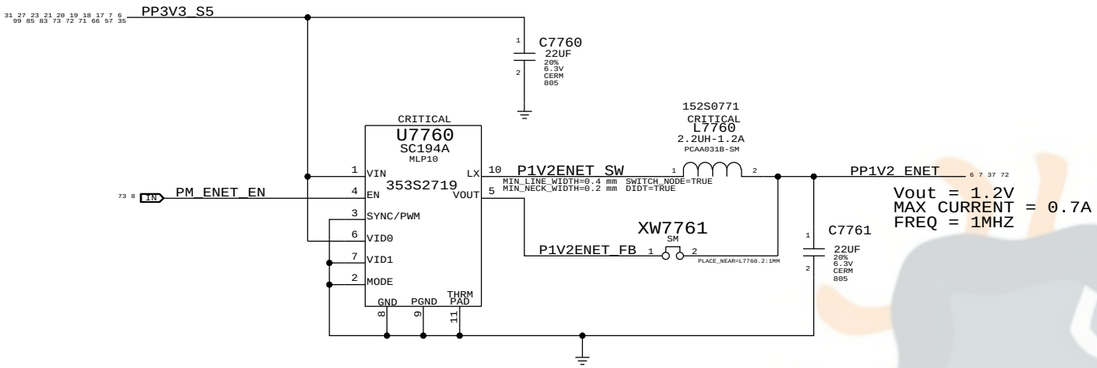
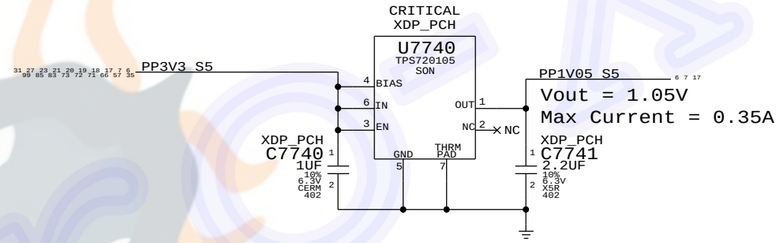
1.2V S3 Regulator

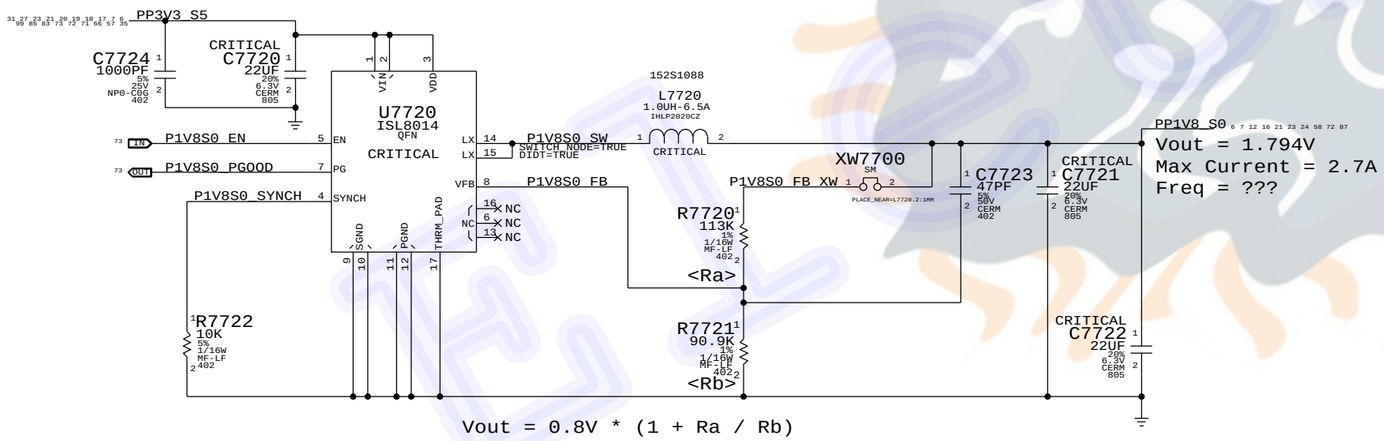


1.05V S5 LDO

Ibex Peak-M requires JTAG pull-ups to be powered at 1.05V in S5.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.8V S0 Regulator



Vout = 0.8V * (1 + Ra / Rb)

SYNC_MASTER=K18_POWER SYNC_DATE=06/29/2009

PAGE TITLE
Misc Power Supplies

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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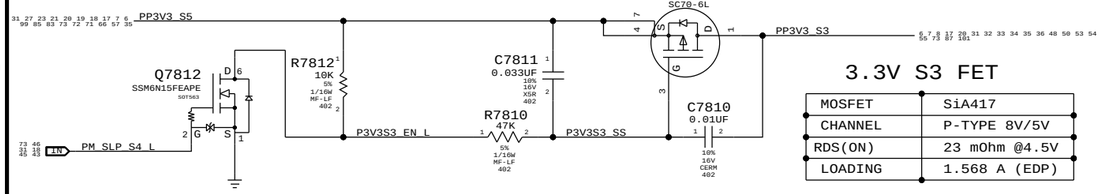
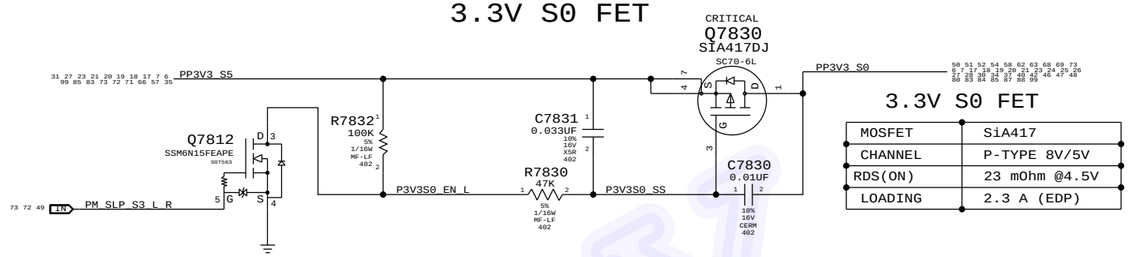
3.3V S3 FET



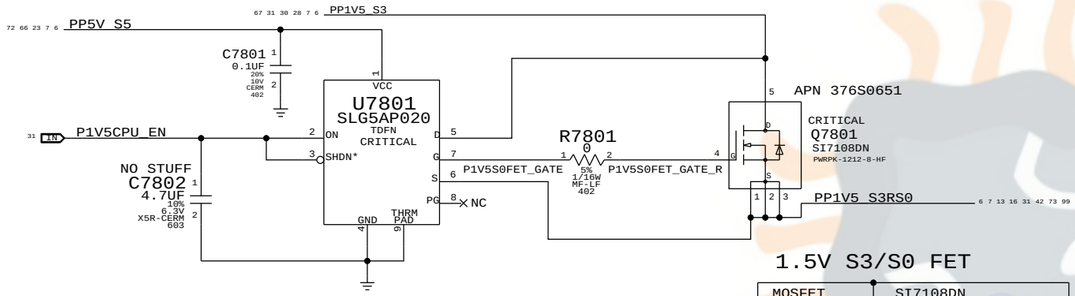
3.3V S3 FET	
MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	1.568 A (EDP)

3.3V S0 FET



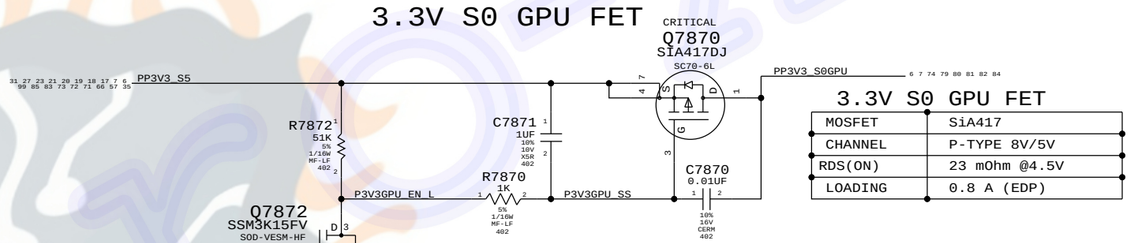
3.3V S0 FET	
MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	2.3 A (EDP)

1.5V S3/S0 FET



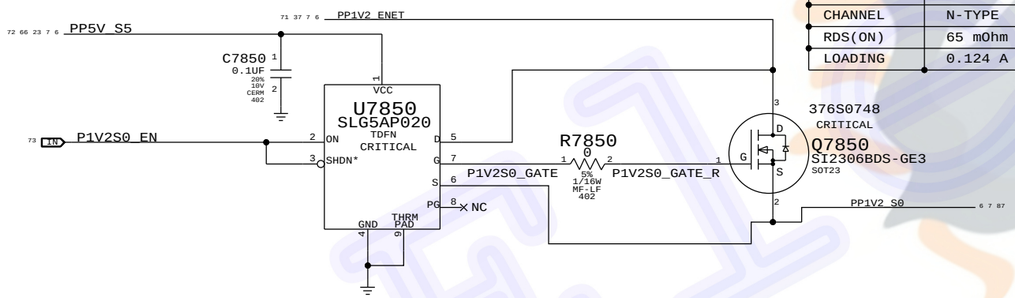
1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	3.2 A (EDP)

3.3V S0 GPU FET



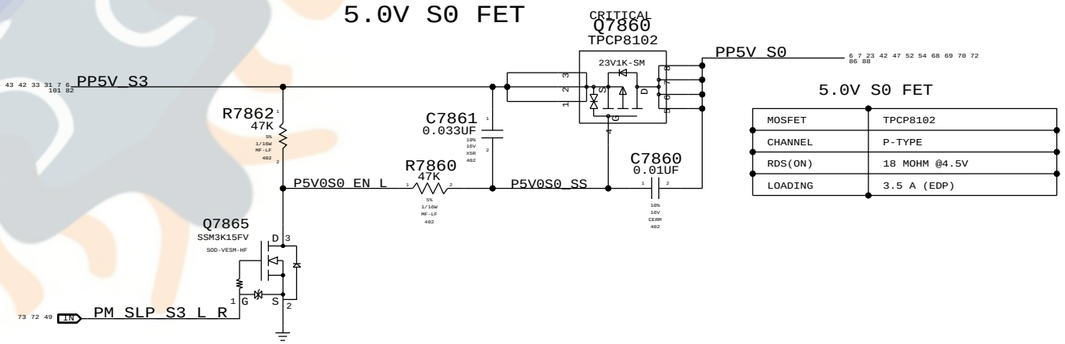
3.3V S0 GPU FET	
MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	0.8 A (EDP)

1.2V S0 FET



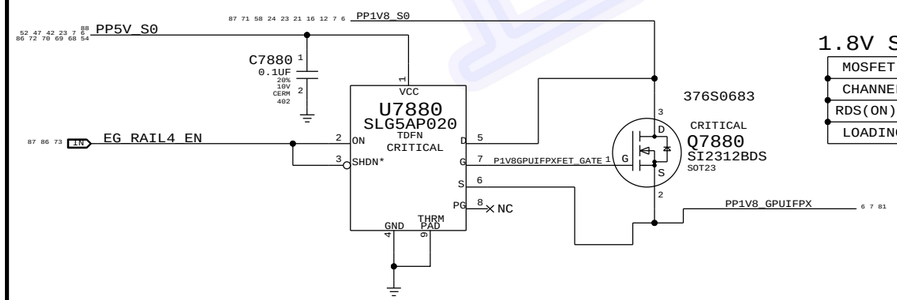
1.2V S0 FET	
MOSFET	SI2306BDS-GE3
CHANNEL	N-TYPE
RDS(ON)	65 mOhm @4.5V
LOADING	0.124 A (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	3.5 A (EDP)

1.8V S0 GPU_IFPX FET



1.8V S0 GPU_IFPX FET	
MOSFET	SI2312BDS
CHANNEL	N-TYPE
RDS(ON)	31 mOhm @4.5V
LOADING	0.3 A (EDP)

SYNC_MASTER=K18_POWER SYNC_DATE=06/10/2009

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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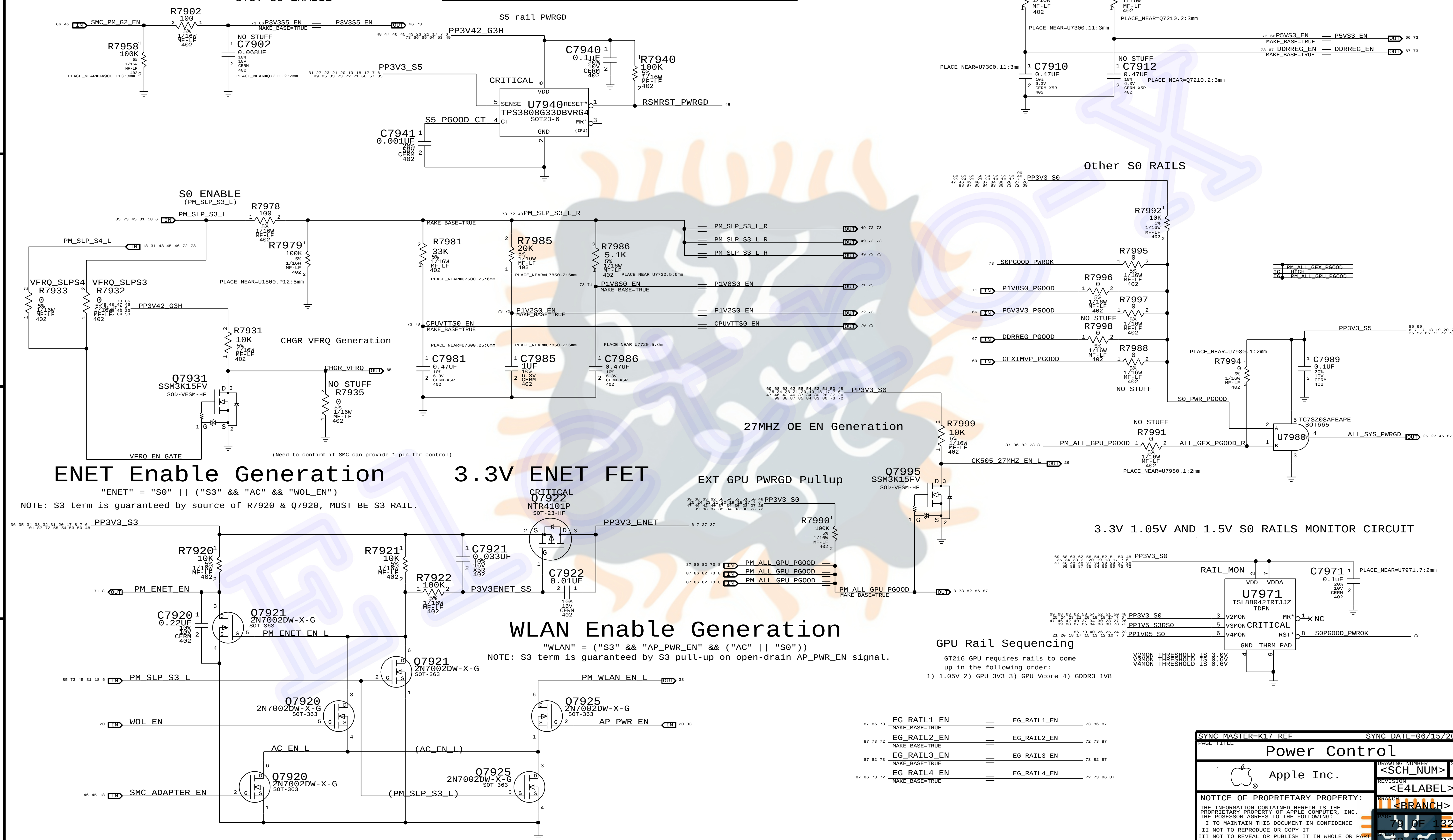
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0



3.3V S5 ENABLE
SMC_PM_G2_EN
R7902 100
P3V3S5_EN
R7958 100K
NO STUFF C7902 0.068UF
S5 rail PWRGD
PP3V42_G3H
PP3V3_S5
C7940 0.1UF
R7940 100K
CRITICAL
U7940 TPS3808G33DBVRG4 SOT23-6
RSMRST_PWRGD
S5_PGOOD_CT
C7941 0.001UF
3.3V,5V S3 ENABLE
PM_SLP_S4_L
(PM_S4_STATE_L)
R7911 5.1K
R7912 0
P5VS3_EN
DDRREG_EN
C7910 0.47UF
NO STUFF C7912 0.47UF
S0 ENABLE (PM_SLP_S3_L)
PM_SLP_S3_L
R7978 100
PM_SLP_S4_L
R7979 100K
VFRQ_SLPS4
VFRQ_SLPS3
R7933 0
R7932 0
PP3V42_G3H
R7931 10K
CHGR VFRQ Generation
CHGR_VFRQ
Q7931 SSM3K15FV SOD-VESM-HF
NO STUFF R7935 0
VFRQ_EN_GATE
(Need to confirm if SMC can provide 1 pin for control)
PM_SLP_S3_L_R
R7981 33K
R7985 20K
R7986 5.1K
P1V8S0_EN
P1V2S0_EN
CPUVTTS0_EN
C7981 0.47UF
C7985 1UF
C7986 0.47UF
Other S0 RAILS
PP3V3_S0
R7992 10K
S0PGOOD_PWROK
R7995 0
P1V8S0_PGOOD
R7996 0
P5V3V3_PGOOD
R7997 0
DDRREG_PGOOD
NO STUFF R7998 0
GFXIMVP_PGOOD
R7988 0
NO STUFF
PM_ALL_GFX_PGOOD
HIGH
PM_ALL_GPU_PGOOD
PP3V3_S5
R7994 0
C7989 0.1UF
S0_PWR_PGOOD
NO STUFF R7991 0
ALL_GFX_PGOOD_R
TC7SZ08AFEAPE SOT665
U7980
ALL_SYS_PWRGD
27MHZ OE EN Generation
PP3V3_S0
R7999 10K
CK505_27MHZ_EN_L
Q7995 SSM3K15FV SOD-VESM-HF
EXT GPU PWRGD Pullup
R7990 100K
PM_ALL_GPU_PGOOD
ENET Enable Generation
"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")
NOTE: S3 term is guaranteed by source of R7920 & Q7920, MUST BE S3 RAIL.
3.3V ENET FET
CRITICAL Q7922 NTR4101P SOT-23-HF
PP3V3_S3
PP3V3_ENET
R7920 10K
R7921 10K
C7921 0.033UF
R7922 100K
P3V3ENET_SS
C7922 0.01UF
PM_ENET_EN
C7920 0.22UF
Q7921 2N7002DW-X-G SOT-363
PM_ENET_EN_L
PM_SLP_S3_L
WOL_EN
Q7920 2N7002DW-X-G SOT-363
AC_EN_L
(AC_EN_L)
SMC_ADAPTER_EN
(PM_SLP_S3_L)
Q7925 2N7002DW-X-G SOT-363
WLAN Enable Generation
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.
PM_WLAN_EN_L
AP_PWR_EN
GPU Rail Sequencing
GT216 GPU requires rails to come up in the following order:
1) 1.05V 2) GPU 3V3 3) GPU Vcore 4) GDDR3 1V8
EG_RAIL1_EN
EG_RAIL2_EN
EG_RAIL3_EN
EG_RAIL4_EN
3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT
RAIL_MON
U7971 ISL88042IRTJJZ TDFN
C7971 0.1UF
PP3V3_S0
PP1V5_S3RS0
PP1V05_S0
S0PGOOD_PWROK
V2MON THRESHOLD IS 3.0V
V3MON THRESHOLD IS 0.6V
V4MON THRESHOLD IS 0.6V

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: Power Control

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PP1V05_S0GPU
PP1V05_S0GPU
PP1V05_S0GPU

PEX 1.1V Current = 2A

250mA

C8002 1UF 10% 6.3V CERM 402
C8001 4.7UF 20% 6.3V CERM 603
C8000 22UF 20% 6.3V CERM-X5R 805
C8003 1UF 10% 6.3V CERM 402
C8004 0.1UF 20% 10V CERM 402
C8005 0.1UF 20% 10V CERM 402

1500mA

C8008 1UF 10% 6.3V CERM 402
C8007 4.7UF 20% 6.3V CERM 603
C8006 22UF 20% 6.3V CERM-X5R 805
C8018 10UF 20% 6.3V X5R 603
C8009 1UF 10% 6.3V CERM 402
C8010 0.1UF 20% 10V CERM 402
C8011 0.1UF 20% 10V CERM 402

L8015 100NH-700MA-0.14OHM 0603

120 mA: GT216 A01 DG v3 01/09

PP1V1_GPU_PEX_PLLVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.1V

C8017 1UF 10% 6.3V CERM 402
C8016 4.7UF 20% 6.3V CERM 603
C8015 4.7UF 20% 6.3V CERM 603

NC_GPU_DFM
NO_TEST=TRUE

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H32	PEX_IOVDD1	AK16
M7	PEX_IOVDD2	AK17
P6	PEX_IOVDD3	AK21
A5	PEX_IOVDD4	AK24
U7	PEX_IOVDD5	AK27
V6		
AB7		
AD6		
AF6	PEX_IOVDDQ1	AG11
AG6	PEX_IOVDDQ2	AG12
AJ5	PEX_IOVDDQ3	AG13
AK15	PEX_IOVDDQ4	AG15
AL7	PEX_IOVDDQ5	AG16
E7	PEX_IOVDDQ6	AG17
A2	PEX_IOVDDQ7	AG18
A7	PEX_IOVDDQ8	AG22
B7	PEX_IOVDDQ9	AG23
C5	NC PEX_IOVDDQ10	AG24
C7	PEX_IOVDDQ11	AG25
D5	PEX_IOVDDQ12	AG26
D6	PEX_IOVDDQ13	AJ14
D7	PEX_IOVDDQ14	AJ15
E5	PEX_IOVDDQ15	AJ19
E4	PEX_IOVDDQ16	AJ21
G5	PEX_IOVDDQ17	AJ22
J18	PEX_IOVDDQ18	AJ24
J19	PEX_IOVDDQ19	AJ25
J25	PEX_IOVDDQ20	AJ27
J26	PEX_IOVDDQ21	AK18
AA4	PEX_IOVDDQ22	AK20
AB4	PEX_IOVDDQ23	AK23
AC5	PEX_IOVDDQ24	AK26
Y4	PEX_IOVDDQ25	AL16
AG20		
D35		
P7	VDD_SENSE PEX_PLLVDD	AG14
E35		
R7	GND_SENSE VDD_SENSE	AD20
A4	BUFRST* GND_SENSE	AD19

GPU_VDD_SENSE 82
GPU_GND_SENSE 82

NC_GPU_BUFRST_L OUT 6

PEG_R2D_C_P<0>	C8020 0.1uF	PEG_R2D_P<0>	AP17	PEX_RX0
PEG_R2D_C_N<0>	C8021 0.1uF	PEG_R2D_N<0>	AN17	PEX_RX0*
PEG_R2D_C_P<1>	C8022 0.1uF	PEG_R2D_P<1>	AN19	PEX_RX1
PEG_R2D_C_N<1>	C8023 0.1uF	PEG_R2D_N<1>	AP19	PEX_RX1*
PEG_R2D_C_P<2>	C8024 0.1uF	PEG_R2D_P<2>	AR19	PEX_RX2
PEG_R2D_C_N<2>	C8025 0.1uF	PEG_R2D_N<2>	AR20	PEX_RX2*
PEG_R2D_C_P<3>	C8026 0.1uF	PEG_R2D_P<3>	AP20	PEX_RX3
PEG_R2D_C_N<3>	C8027 0.1uF	PEG_R2D_N<3>	AN20	PEX_RX3*
PEG_R2D_C_P<4>	C8028 0.1uF	PEG_R2D_P<4>	AN22	PEX_RX4
PEG_R2D_C_N<4>	C8029 0.1uF	PEG_R2D_N<4>	AP22	PEX_RX4*
PEG_R2D_C_P<5>	C8030 0.1uF	PEG_R2D_P<5>	AR22	PEX_RX5
PEG_R2D_C_N<5>	C8031 0.1uF	PEG_R2D_N<5>	AR23	PEX_RX5*
PEG_R2D_C_P<6>	C8032 0.1uF	PEG_R2D_P<6>	AP23	PEX_RX6
PEG_R2D_C_N<6>	C8033 0.1uF	PEG_R2D_N<6>	AN23	PEX_RX6*
PEG_R2D_C_P<7>	C8034 0.1uF	PEG_R2D_P<7>	AN25	PEX_RX7
PEG_R2D_C_N<7>	C8035 0.1uF	PEG_R2D_N<7>	AP25	PEX_RX7*
PEG_R2D_C_P<8>	C8036 0.1uF	PEG_R2D_P<8>	AR25	PEX_RX8
PEG_R2D_C_N<8>	C8037 0.1uF	PEG_R2D_N<8>	AR26	PEX_RX8*
PEG_R2D_C_P<9>	C8038 0.1uF	PEG_R2D_P<9>	AP26	PEX_RX9
PEG_R2D_C_N<9>	C8039 0.1uF	PEG_R2D_N<9>	AN26	PEX_RX9*
PEG_R2D_C_P<10>	C8040 0.1uF	PEG_R2D_P<10>	AN28	PEX_RX10
PEG_R2D_C_N<10>	C8041 0.1uF	PEG_R2D_N<10>	AP28	PEX_RX10*
PEG_R2D_C_P<11>	C8042 0.1uF	PEG_R2D_P<11>	AR28	PEX_RX11
PEG_R2D_C_N<11>	C8043 0.1uF	PEG_R2D_N<11>	AR29	PEX_RX11*
PEG_R2D_C_P<12>	C8044 0.1uF	PEG_R2D_P<12>	AP29	PEX_RX12
PEG_R2D_C_N<12>	C8045 0.1uF	PEG_R2D_N<12>	AN29	PEX_RX12*
PEG_R2D_C_P<13>	C8046 0.1uF	PEG_R2D_P<13>	AN31	PEX_RX13
PEG_R2D_C_N<13>	C8047 0.1uF	PEG_R2D_N<13>	AP31	PEX_RX13*
PEG_R2D_C_P<14>	C8048 0.1uF	PEG_R2D_P<14>	AR31	PEX_RX14
PEG_R2D_C_N<14>	C8049 0.1uF	PEG_R2D_N<14>	AR32	PEX_RX14*
PEG_R2D_C_P<15>	C8050 0.1uF	PEG_R2D_P<15>	AR34	PEX_RX15
PEG_R2D_C_N<15>	C8051 0.1uF	PEG_R2D_N<15>	AP34	PEX_RX15*

PEG_CLK100M_P AR16 PEX_REFCLK
PEG_CLK100M_N AR17 PEX_REFCLK*
EG_RESET_L R8020 0 5% 1/16W MF-LF 402 GPU_RESET_R_L AM16 PEX_RST*
PEX_CLKREQ_L AR13 PEX_CLKREQ*

PP3V3_S0GPU
R8021 10K 5% 1/16W MF-LF 402

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PEX_TX0	AL17	PEG_D2R_C_P<0>	C8055 0.1uF	PEG_D2R_P<0>
PEX_TX0*	AM17	PEG_D2R_C_N<0>	C8056 0.1uF	PEG_D2R_N<0>
PEX_TX1	AM18	PEG_D2R_C_P<1>	C8057 0.1uF	PEG_D2R_P<1>
PEX_TX1*	AM19	PEG_D2R_C_N<1>	C8058 0.1uF	PEG_D2R_N<1>
PEX_TX2	AL19	PEG_D2R_C_P<2>	C8059 0.1uF	PEG_D2R_P<2>
PEX_TX2*	AK19	PEG_D2R_C_N<2>	C8060 0.1uF	PEG_D2R_N<2>
PEX_TX3	AL20	PEG_D2R_C_P<3>	C8061 0.1uF	PEG_D2R_P<3>
PEX_TX3*	AM20	PEG_D2R_C_N<3>	C8062 0.1uF	PEG_D2R_N<3>
PEX_TX4	AM21	PEG_D2R_C_P<4>	C8063 0.1uF	PEG_D2R_P<4>
PEX_TX4*	AM22	PEG_D2R_C_N<4>	C8064 0.1uF	PEG_D2R_N<4>
PEX_TX5	AL22	PEG_D2R_C_P<5>	C8065 0.1uF	PEG_D2R_P<5>
PEX_TX5*	AK22	PEG_D2R_C_N<5>	C8066 0.1uF	PEG_D2R_N<5>
PEX_TX6	AL23	PEG_D2R_C_P<6>	C8067 0.1uF	PEG_D2R_P<6>
PEX_TX6*	AM23	PEG_D2R_C_N<6>	C8068 0.1uF	PEG_D2R_N<6>
PEX_TX7	AM24	PEG_D2R_C_P<7>	C8069 0.1uF	PEG_D2R_P<7>
PEX_TX7*	AM25	PEG_D2R_C_N<7>	C8070 0.1uF	PEG_D2R_N<7>
PEX_TX8	AL25	PEG_D2R_C_P<8>	C8071 0.1uF	PEG_D2R_P<8>
PEX_TX8*	AK25	PEG_D2R_C_N<8>	C8072 0.1uF	PEG_D2R_N<8>
PEX_TX9	AL26	PEG_D2R_C_P<9>	C8073 0.1uF	PEG_D2R_P<9>
PEX_TX9*	AM26	PEG_D2R_C_N<9>	C8074 0.1uF	PEG_D2R_N<9>
PEX_TX10	AM27	PEG_D2R_C_P<10>	C8075 0.1uF	PEG_D2R_P<10>
PEX_TX10*	AM28	PEG_D2R_C_N<10>	C8076 0.1uF	PEG_D2R_N<10>
PEX_TX11	AL28	PEG_D2R_C_P<11>	C8077 0.1uF	PEG_D2R_P<11>
PEX_TX11*	AK28	PEG_D2R_C_N<11>	C8078 0.1uF	PEG_D2R_N<11>
PEX_TX12	AK29	PEG_D2R_C_P<12>	C8079 0.1uF	PEG_D2R_P<12>
PEX_TX12*	AL29	PEG_D2R_C_N<12>	C8080 0.1uF	PEG_D2R_N<12>
PEX_TX13	AM29	PEG_D2R_C_P<13>	C8081 0.1uF	PEG_D2R_P<13>
PEX_TX13*	AM30	PEG_D2R_C_N<13>	C8082 0.1uF	PEG_D2R_N<13>
PEX_TX14	AM31	PEG_D2R_C_P<14>	C8083 0.1uF	PEG_D2R_P<14>
PEX_TX14*	AM32	PEG_D2R_C_N<14>	C8084 0.1uF	PEG_D2R_N<14>
PEX_TX15	AN32	PEG_D2R_C_P<15>	C8085 0.1uF	PEG_D2R_P<15>
PEX_TX15*	AP32	PEG_D2R_C_N<15>	C8086 0.1uF	PEG_D2R_N<15>

NO STUFF
R8060 200 1% 1/16W MF-LF 402

PEX_TSTCLK_OUT AJ17 PEX_TSTCLK_P
PEX_TSTCLK_OUT* AJ18 PEX_TSTCLK_N
PEX_TERMP AG21 PEX_TERMP_PD
R8050 2.49K 1% 1/16W MF-LF 402
PEX_SVDD_3V3 AG19 F7

C8013 4.7UF 10% 6.3V X5R-CERM 603
C8012 0.1UF 10% 10V X5R 402

NO STUFF
R8012 0 5% 1/16W MF-LF 402
R8013 0 5% 1/16W MF-LF 402

PP1V05_S0GPU
PP3V3R1V1_GPU_PEX_SVDD
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
NV GT216 PCI-E

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 1UF 10% 16V X5R 402
C8101 0.22UF 10% 6.3V CERM-X5R 402
C8102 0.22UF 10% 6.3V CERM-X5R 402
C8103 0.1UF 10% 16V X7R-CERM 402
C8104 0.047UF 10% 16V X7R 402
C8105 0.047UF 10% 16V X7R 402
C8106 0.047UF 10% 16V X7R 402
C8107 0.022UF 10% 16V CERM-X5R 402
C8108 0.022UF 10% 16V CERM-X5R 402
C8109 0.022UF 10% 16V CERM-X5R 402
C8110 0.015UF 10% 16V X7R 402
C8111 0.015UF 10% 16V X7R 402
C8112 0.01UF 10% 25V X7R 402
C8113 0.01UF 10% 25V X7R 402
C8114 0.01UF 10% 25V X7R 402
C8115 0.01UF 10% 25V X7R 402
C8116 0.01UF 10% 25V X7R 402
C8117 0.01UF 10% 25V X7R 402
C8118 0.0068UF 10% 25V CERM 402
C8119 0.0047UF 10% 25V CERM 402

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VDD

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GND

PP1V8R1V55_S0GPU_ISNS

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8156 4.7UF 20% 6.3V CERM 603
C8157 0.1UF 10% 16V CERM 402
C8158 0.1UF 10% 16V CERM 402
C8159 0.1UF 10% 16V CERM 402
C8160 0.047UF 10% 16V X7R 402
C8162 0.047UF 10% 16V X7R 402
C8163 0.047UF 10% 16V X7R 402
C8164 0.01UF 10% 25V X7R 402
C8165 0.01UF 10% 25V X7R 402
C8166 0.01UF 10% 25V X7R 402

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FBVDDQ

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
NV GT216 CORE/FB POWER

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

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FB_A_DQ<0> L32 FBA_D00
FB_A_DQ<1> N33 FBA_D01
FB_A_DQ<2> L33 FBA_D02
FB_A_DQ<3> N34 FBA_D03
FB_A_DQ<4> N35 FBA_D04
FB_A_DQ<5> P35 FBA_D05
FB_A_DQ<6> P33 FBA_D06
FB_A_DQ<7> P34 FBA_D07
FB_A_DQ<8> K35 FBA_D08
FB_A_DQ<9> K33 FBA_D09
FB_A_DQ<10> K34 FBA_D10
FB_A_DQ<11> H33 FBA_D11
FB_A_DQ<12> G34 FBA_D12
FB_A_DQ<13> G33 FBA_D13
FB_A_DQ<14> E34 FBA_D14
FB_A_DQ<15> E33 FBA_D15
FB_A_DQ<16> G31 FBA_D16
FB_A_DQ<17> F30 FBA_D17
FB_A_DQ<18> G30 FBA_D18
FB_A_DQ<19> G32 FBA_D19
FB_A_DQ<20> K30 FBA_D20
FB_A_DQ<21> K32 FBA_D21
FB_A_DQ<22> H30 FBA_D22
FB_A_DQ<23> K31 FBA_D23
FB_A_DQ<24> L31 FBA_D24
FB_A_DQ<25> L30 FBA_D25
FB_A_DQ<26> M32 FBA_D26
FB_A_DQ<27> N30 FBA_D27
FB_A_DQ<28> M30 FBA_D28
FB_A_DQ<29> P31 FBA_D29
FB_A_DQ<30> R32 FBA_D30
FB_A_DQ<31> R30 FBA_D31
FB_A_DQ<32> AG30 FBA_D32
FB_A_DQ<33> AG32 FBA_D33
FB_A_DQ<34> AH31 FBA_D34
FB_A_DQ<35> AF31 FBA_D35
FB_A_DQ<36> AF30 FBA_D36
FB_A_DQ<37> AE30 FBA_D37
FB_A_DQ<38> AC32 FBA_D38
FB_A_DQ<39> AD30 FBA_D39
FB_A_DQ<40> AN33 FBA_D40
FB_A_DQ<41> AL31 FBA_D41
FB_A_DQ<42> AM33 FBA_D42
FB_A_DQ<43> AL33 FBA_D43
FB_A_DQ<44> AK30 FBA_D44
FB_A_DQ<45> AK32 FBA_D45
FB_A_DQ<46> AJ30 FBA_D46
FB_A_DQ<47> AH30 FBA_D47
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FB_A_DQ<49> AH35 FBA_D49
FB_A_DQ<50> AH34 FBA_D50
FB_A_DQ<51> AH32 FBA_D51
FB_A_DQ<52> AJ33 FBA_D52
FB_A_DQ<53> AL35 FBA_D53
FB_A_DQ<54> AM34 FBA_D54
FB_A_DQ<55> AM35 FBA_D55
FB_A_DQ<56> AF33 FBA_D56
FB_A_DQ<57> AE32 FBA_D57
FB_A_DQ<58> AF34 FBA_D58
FB_A_DQ<59> AE35 FBA_D59
FB_A_DQ<60> AE34 FBA_D60
FB_A_DQ<61> AE33 FBA_D61
FB_A_DQ<62> AB32 FBA_D62
FB_A_DQ<63> AC35 FBA_D63

NC: NCX H29, NCX G29, NCX J29, NCX M29, NCX AD29, NCX AE29, NCX AG29, NCX AH29

FBA_CMD0 V32 FB_A_LMA<4>
FBA_CMD1 W31 FB_A_RAS_L
FBA_CMD2 U31 FB_A_LMA<5>
FBA_CMD3 Y32 FB_A_BA<1>
FBA_CMD4 AB35 FB_A_UMA<2>
FBA_CMD5 AB34 FB_A_UMA<4>
FBA_CMD6 W35 FB_A_UMA<3>
FBA_CMD7 W33 FB_A_UCKE
FBA_CMD8 W30 FB_A_UCS0_L
FBA_CMD9 T34 FB_A_MA<11>
FBA_CMD10 T35 FB_A_LCAS_L
FBA_CMD11 AB31 FB_A_WE_L
FBA_CMD12 Y30 FB_A_BA<0>
FBA_CMD13 Y34 FB_A_UMA<5>
FBA_CMD14 W32 FB_A_MA<12>
FBA_CMD15 AA30 FB_A_DRAM_RST
FBA_CMD16 AA32 FB_A_MA<7>
FBA_CMD17 Y33 FB_A_MA<10>
FBA_CMD18 U32 FB_A_LCKE
FBA_CMD19 Y31 FB_A_MA<0>
FBA_CMD20 U34 FB_A_MA<9>
FBA_CMD21 Y35 FB_A_MA<6>
FBA_CMD22 W34 FB_A_LMA<2>
FBA_CMD23 V30 FB_A_MA<8>
FBA_CMD24 U35 FB_A_LMA<3>
FBA_CMD25 U30 FB_A_MA<1>
FBA_CMD26 U33 NC_FBA_MA<13>
FBA_CMD27 AB30 FB_A_BA<2>
FBA_CMD28 AB33 NC_FB_A_UCS1_L
FBA_CMD29 T33 FB_A_LCS0_L
FBA_CMD30 W29 NC_FB_A_LCS1_L

FBA_CLK0 T32 FB_A_CLK_P<0>
FBA_CLK0* T31 FB_A_CLK_N<0>
FBA_CLK1 AC31 FB_A_CLK_P<1>
FBA_CLK1* AC30 FB_A_CLK_N<1>

FBA_DQM0 P32 FB_A_DQM_L<0>
FBA_DQM1 H34 FB_A_DQM_L<1>
FBA_DQM2 J30 FB_A_DQM_L<2>
FBA_DQM3 P30 FB_A_DQM_L<3>
FBA_DQM4 AF32 FB_A_DQM_L<4>
FBA_DQM5 AL32 FB_A_DQM_L<5>
FBA_DQM6 AL34 FB_A_DQM_L<6>
FBA_DQM7 AF35 FB_A_DQM_L<7>

FBA_DQS_RN0 L35 FB_A_RDQS<0>
FBA_DQS_RN1 G35 FB_A_RDQS<1>
FBA_DQS_RN2 H31 FB_A_RDQS<2>
FBA_DQS_RN3 N32 FB_A_RDQS<3>
FBA_DQS_RN4 AD32 FB_A_RDQS<4>
FBA_DQS_RN5 AJ31 FB_A_RDQS<5>
FBA_DQS_RN6 AJ35 FB_A_RDQS<6>
FBA_DQS_RN7 AC34 FB_A_RDQS<7>

FBA_DQS_WP0 L34 FB_A_WDQS<0>
FBA_DQS_WP1 H35 FB_A_WDQS<1>
FBA_DQS_WP2 J32 FB_A_WDQS<2>
FBA_DQS_WP3 N31 FB_A_WDQS<3>
FBA_DQS_WP4 AE31 FB_A_WDQS<4>
FBA_DQS_WP5 AJ32 FB_A_WDQS<5>
FBA_DQS_WP6 AJ34 FB_A_WDQS<6>
FBA_DQS_WP7 AC33 FB_A_WDQS<7>

FB_DLLAVDD AG27 PP1V1_GPU_FBPLLAVDD_F
FB_PLLAVDD AF27
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.1V

FBA_DEBUG T30 FB_A_UCAS_L

FB_CAL_PD_VDDQ K27 FBCAL_PD_VDDQ
FB_CAL_PU_GND L27 FBCAL_PU_GND
FB_CAL_TERM_GND M27 FBCAL_TERM_GND

R8203 1 10K 5% 1/16W MF-LF 402 2
R8200 1 10K 5% 1/16W MF-LF 402 2
R8201 1 10K 5% 1/16W MF-LF 402 2

PP1V05_S0GPU
CRITICAL
L8200
300-OHM-0.5A
0603-1
C8202 1 1UF 10% 6.3V CERM 402
C8200 1 4.7UF 10% 6.3V X5R-CERM 603
C8201 1 4.7UF 10% 6.3V X5R-CERM 603

PP1V8R1V55_S0GPU_ISNS
R8290 1 56.2 1% 1/16W MF-LF 402 2
PLACE_NEAR=U8000.K27:3mm
R8292 1 40.2 1% 1/16W MF-LF 402 2
PLACE_NEAR=U8000.M27:3mm
R8291 1 31.6 1% 1/16W MF-LF 402 2
PLACE_NEAR=U8000.L27:3mm

OMIT
U8000
NV-GT216
BGA
(4 OF 9)

FB_B_DQ<0> B13 FBC_D00
FB_B_DQ<1> D13 FBC_D01
FB_B_DQ<2> A13 FBC_D02
FB_B_DQ<3> A14 FBC_D03
FB_B_DQ<4> C16 FBC_D04
FB_B_DQ<5> B16 FBC_D05
FB_B_DQ<6> A17 FBC_D06
FB_B_DQ<7> D16 FBC_D07
FB_B_DQ<8> C13 FBC_D08
FB_B_DQ<9> B11 FBC_D09
FB_B_DQ<10> C11 FBC_D10
FB_B_DQ<11> A11 FBC_D11
FB_B_DQ<12> C10 FBC_D12
FB_B_DQ<13> C8 FBC_D13
FB_B_DQ<14> B8 FBC_D14
FB_B_DQ<15> A8 FBC_D15
FB_B_DQ<16> F8 FBC_D16
FB_B_DQ<17> F8 FBC_D17
FB_B_DQ<18> F10 FBC_D18
FB_B_DQ<19> F9 FBC_D19
FB_B_DQ<20> F12 FBC_D20
FB_B_DQ<21> D8 FBC_D21
FB_B_DQ<22> D11 FBC_D22
FB_B_DQ<23> E11 FBC_D23
FB_B_DQ<24> D12 FBC_D24
FB_B_DQ<25> E13 FBC_D25
FB_B_DQ<26> F13 FBC_D26
FB_B_DQ<27> F14 FBC_D27
FB_B_DQ<28> F15 FBC_D28
FB_B_DQ<29> E16 FBC_D29
FB_B_DQ<30> F16 FBC_D30
FB_B_DQ<31> F17 FBC_D31
FB_B_DQ<32> D29 FBC_D32
FB_B_DQ<33> F27 FBC_D33
FB_B_DQ<34> F28 FBC_D34
FB_B_DQ<35> E28 FBC_D35
FB_B_DQ<36> D26 FBC_D36
FB_B_DQ<37> F25 FBC_D37
FB_B_DQ<38> D24 FBC_D38
FB_B_DQ<39> E25 FBC_D39
FB_B_DQ<40> E32 FBC_D40
FB_B_DQ<41> F32 FBC_D41
FB_B_DQ<42> D33 FBC_D42
FB_B_DQ<43> E31 FBC_D43
FB_B_DQ<44> C33 FBC_D44
FB_B_DQ<45> F29 FBC_D45
FB_B_DQ<46> D30 FBC_D46
FB_B_DQ<47> E29 FBC_D47
FB_B_DQ<48> B29 FBC_D48
FB_B_DQ<49> C31 FBC_D49
FB_B_DQ<50> C29 FBC_D50
FB_B_DQ<51> B31 FBC_D51
FB_B_DQ<52> C32 FBC_D52
FB_B_DQ<53> B32 FBC_D53
FB_B_DQ<54> B35 FBC_D54
FB_B_DQ<55> B34 FBC_D55
FB_B_DQ<56> A29 FBC_D56
FB_B_DQ<57> B28 FBC_D57
FB_B_DQ<58> A28 FBC_D58
FB_B_DQ<59> C28 FBC_D59
FB_B_DQ<60> C26 FBC_D60
FB_B_DQ<61> D25 FBC_D61
FB_B_DQ<62> B25 FBC_D62
FB_B_DQ<63> A25 FBC_D63

NC: NCX C11, NCX C12, NCX C14, NCX C15, NCX C24, NCX C25, NCX C27, NCX C28

FBC_CMD0 C17 FB_B_LMA<4>
FBC_CMD1 B19 FB_B_RAS_L
FBC_CMD2 D18 FB_B_LMA<5>
FBC_CMD3 F21 FB_B_BA<1>
FBC_CMD4 A23 FB_B_UMA<2>
FBC_CMD5 D21 FB_B_UMA<4>
FBC_CMD6 B23 FB_B_UMA<3>
FBC_CMD7 E20 FB_B_UCKE
FBC_CMD8 G21 FB_B_UCS0_L
FBC_CMD9 F20 FB_B_MA<11>
FBC_CMD10 F19 FB_B_LCAS_L
FBC_CMD11 F23 FB_B_WE_L
FBC_CMD12 A22 FB_B_BA<0>
FBC_CMD13 C22 FB_B_UMA<5>
FBC_CMD14 B17 FB_B_MA<12>
FBC_CMD15 F24 FB_B_DRAM_RST
FBC_CMD16 C25 FB_B_MA<7>
FBC_CMD17 E22 FB_B_MA<10>
FBC_CMD18 C20 FB_B_LCKE
FBC_CMD19 B22 FB_B_MA<0>
FBC_CMD20 A19 FB_B_MA<9>
FBC_CMD21 D22 FB_B_MA<6>
FBC_CMD22 D20 FB_B_LMA<2>
FBC_CMD23 E19 FB_B_MA<8>
FBC_CMD24 D19 FB_B_LMA<3>
FBC_CMD25 F18 FB_B_MA<1>
FBC_CMD26 C19 NC_FBB_MA<13>
FBC_CMD27 F22 FB_B_BA<2>
FBC_CMD28 C23 NC_FB_B_UCS1_L
FBC_CMD29 B20 FB_B_LCS0_L
FBC_CMD30 A20 NC_FB_B_LCS1_L

FBC_CLK0 E17 FB_B_CLK_P<0>
FBC_CLK0* D17 FB_B_CLK_N<0>
FBC_CLK1 D23 FB_B_CLK_P<1>
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FBC_DQM6 A34 FB_B_DQM_L<6>
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FBC_DQS_RN7 A26 FB_B_RDQS<7>

FBC_DQS_WP0 C14 FB_B_WDQS<0>
FBC_DQS_WP1 A10 FB_B_WDQS<1>
FBC_DQS_WP2 E10 FB_B_WDQS<2>
FBC_DQS_WP3 D14 FB_B_WDQS<3>
FBC_DQS_WP4 F26 FB_B_WDQS<4>
FBC_DQS_WP5 D32 FB_B_WDQS<5>
FBC_DQS_WP6 A32 FB_B_WDQS<6>
FBC_DQS_WP7 B26 FB_B_WDQS<7>

FBC_DEBUG G19 FB_B_UCAS_L
FB_VREF J27 GPU_FB_VREF

R8252 1 10K 5% 1/16W MF-LF 402 2
R8250 1 10K 5% 1/16W MF-LF 402 2
R8251 1 10K 5% 1/16W MF-LF 402 2

PP1V8R1V55_S0GPU_ISNS
R8295 1 1.07K 1% 1/16W MF-LF 402 2
R8296 1 2.49K 1% 1/16W MF-LF 402 2

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009
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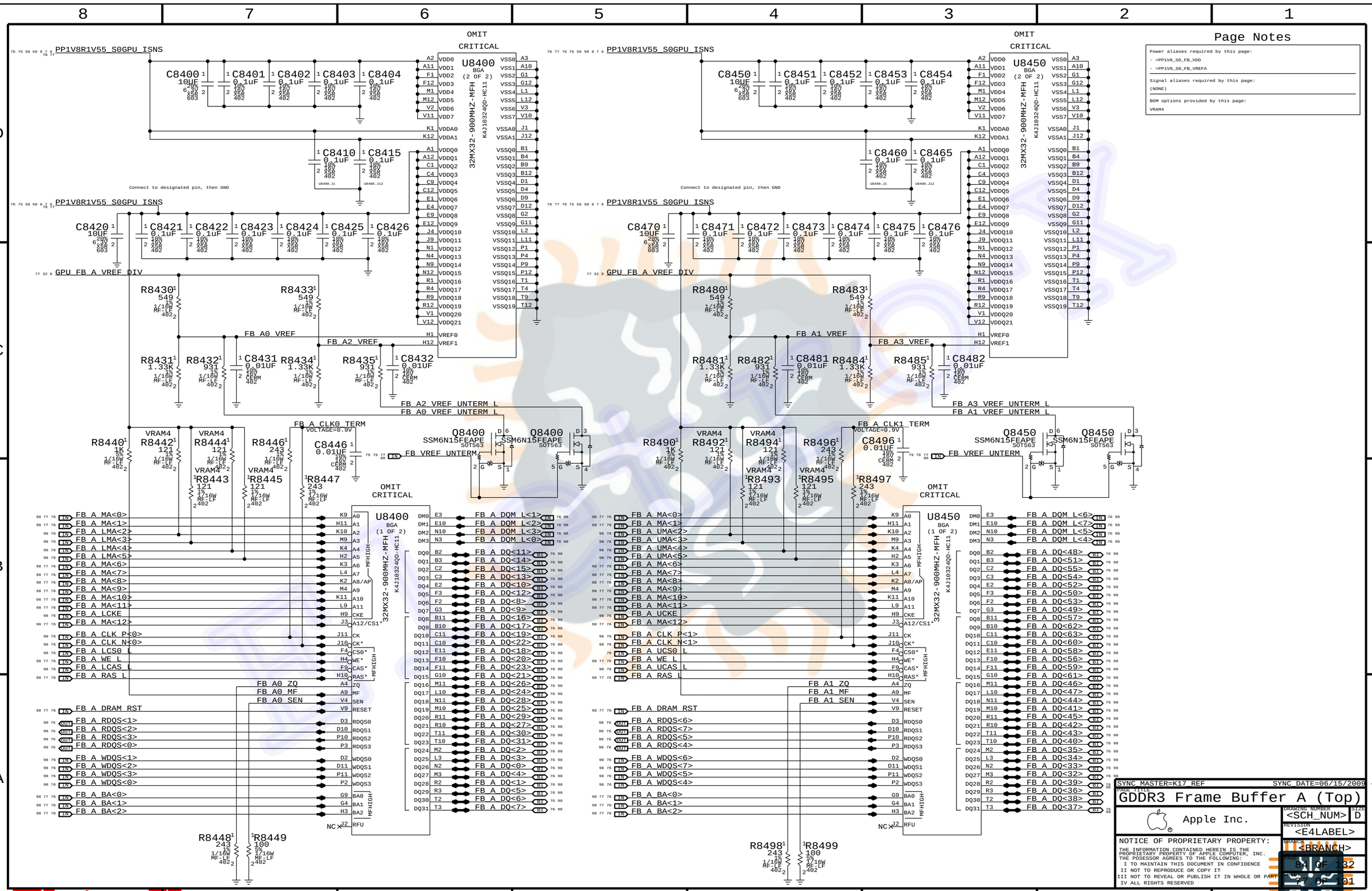
NV GT216 FRAME BUFFER I/F
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 82 OF 132
SHEET 70 OF 101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CRITICAL
U8400
BGA
(2 OF 2)
32MX32-900MHZ-MFH
K4J10324QD-HC11
U8400
BGA
(1 OF 2)
32MX32-900MHZ-MFH
K4J10324QD-HC11
OMIT
CRITICAL
U8450
BGA
(2 OF 2)
32MX32-900MHZ-MFH
K4J10324QD-HC11
U8450
BGA
(1 OF 2)
32MX32-900MHZ-MFH
K4J10324QD-HC11
PP1V8R1V55_S0GPU_ISNS
Connect to designated pin, then GND
GPU_FB_A_VREF_DIV
FB_A0_VREF
FB_A2_VREF
FB_A2_VREF_UNTERM_L
FB_A0_VREF_UNTERM_L
FB_A_CLK0_TERM
VOLTAGE=0.9V
FB_VREF_UNTERM
FB_A1_VREF
FB_A3_VREF
FB_A3_VREF_UNTERM_L
FB_A1_VREF_UNTERM_L
FB_A_CLK1_TERM
FB_A0_ZQ
FB_A0_MF
FB_A0_SEN
FB_A1_ZQ
FB_A1_MF
FB_A1_SEN
OMIT
CRITICAL
OMIT
CRITICAL
Q8400
SSM6N15FEAPE
SOT563
Q8450
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SOT563
VRAM4
FB_A_MA<0>
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FB_A_LMA<2>
FB_A_LMA<3>
FB_A_LMA<4>
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FB_A_MA<11>
FB_A_LCKE
FB_A_MA<12>
FB_A_CLK_P<0>
FB_A_CLK_N<0>
FB_A_LCS0_L
FB_A_WE_L
FB_A_LCAS_L
FB_A_RAS_L
FB_A_UMA<2>
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FB_A_MA<11>
FB_A_UCKE
FB_A_MA<12>
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FB_A_CLK_N<1>
FB_A_UCS0_L
FB_A_WE_L
FB_A_UCAS_L
FB_A_RAS_L
FB_A_DRAM_RST
FB_A_RDQS<1>
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FB_A_WDQS<4>
FB_A_DQM_L<1>
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FB_A_DQM_L<0>
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FB_A_DQM_L<7>
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FB_A_DQM_L<4>
Page Notes
Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREFA
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
VRAM4
SYNC_MASTER=K17_REF
SYNC_DATE=06/15/2009
PAGE TITLE
GDDR3 Frame Buffer A (Top)
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
84 OF 132
SHEET
77 OF 101
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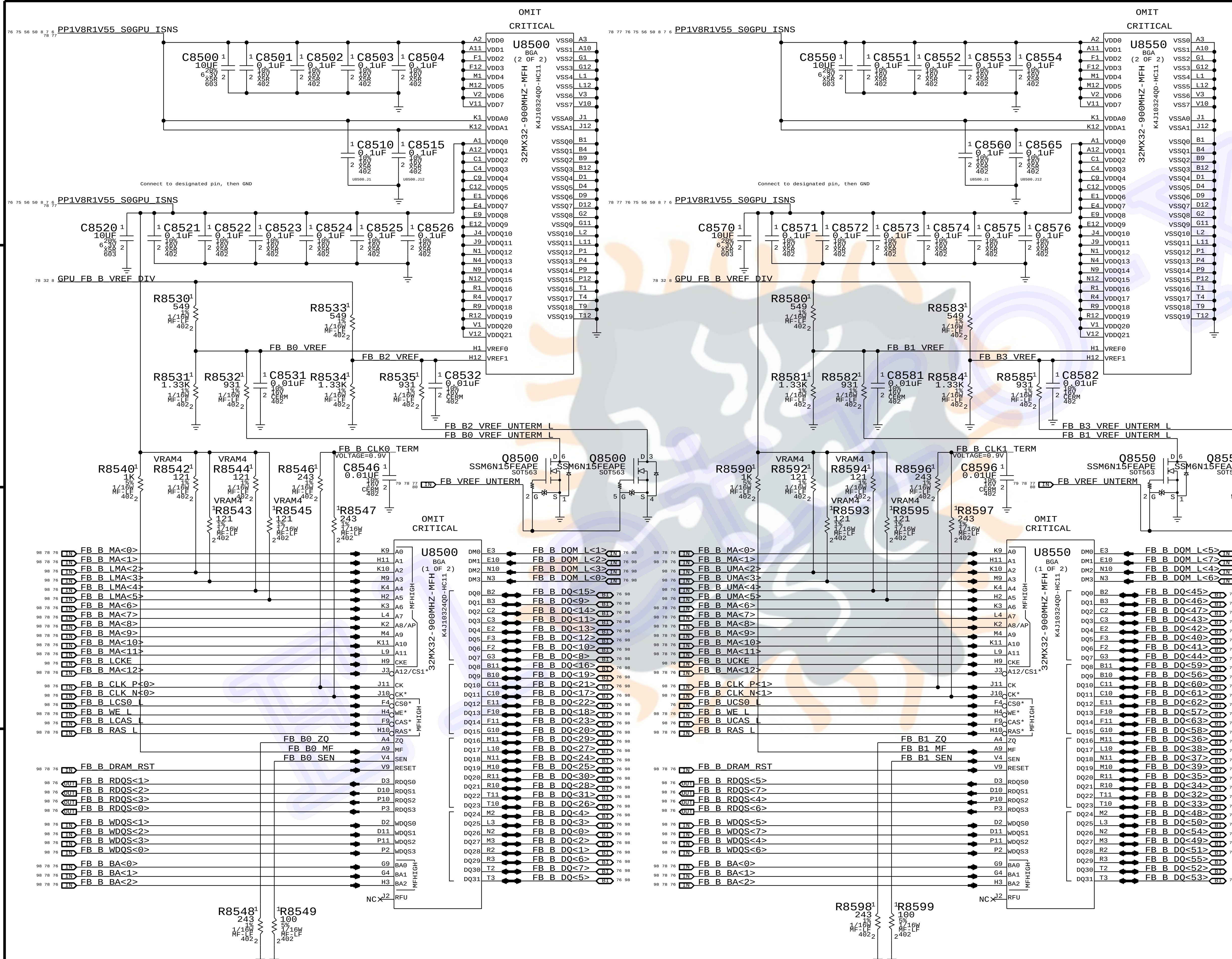

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- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREF_B

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE

GDDR3 Frame Buffer B (Top)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT

U8000
NV-GT216
BGA
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PP3V3_S0GPU
C8694 0.1UF 10% 10V CERM 402
C8696 1UF 10% 6.3V X5R 402
C8698 4.7UF 20% 6.3V X5R-CERM1 402
J9 J10 J11 J12 J13 VDD33

NC_GPU_ROM_CS_L C3 ROM_CS*
GPU_ROM_SCLK D4 ROM_SCLK
GPU_ROM_SI D3 ROM_SI
GPU_ROM_SO C4 ROM_SO
R8696 40.2K 1% 1/16W MF-LF 402
R8697 40.2K 1% 1/16W MF-LF 402
GPU_STRAP_REF_3V3_PD N9 MULTI_STRAP_REF0_GND
GPU_STRAP_REF_MIOB_PD P9 MULTI_STRAP_REF1_GND

PP3V3_S0GPU
R8620 49.9 1% 1/10W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402
GPU_MIOA_PD_VDDQ
GPU_MIOB_PD_VDDQ
GPU_MIOA_PU_GND
GPU_MIOB_PU_GND
R8622 49.9 1% 1/10W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402
R8616 10K 5% 1/10W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
R8617 10K 5% 1/10W MF-LF 402
C8617 0.1UF 10% 10V X5R 402
R8619 10K 5% 1/16W MF-LF 402
C8619 0.1UF 10% 10V X5R 402
R8660 10K 5% 1/16W MF-LF 402
C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402

P9 MIOA_VDDQ_1
R9 MIOA_VDDQ_2
T9 MIOA_VDDQ_3
U9 MIOA_VDDQ_4
AA9 MIOB_VDDQ_1
AB9 MIOB_VDDQ_2
W9 MIOB_VDDQ_3
Y9 MIOB_VDDQ_4
GPU_TESTMODE_PD AP35 TESTMODE
GPU_MIOA_VREF N5 MIOA_VREF
GPU_MIOB_VREF AF1 MIOB_VREF
GPU_MIOA_PD_VDDQ U5 MIOA_CAL_PD_VDDQ
GPU_MIOA_PU_GND T5 MIOA_CAL_PU_GND
GPU_MIOB_PD_VDDQ AA7 MIOB_CAL_PD_VDDQ
GPU_MIOB_PU_GND AA6 MIOB_CAL_PU_GND

L8635 100NH-700MA-0.14OHM 0603
PP1V05_S0GPU
PP1V1_GPU_H_PLLVDD_F 25mA
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 1UF 10% 6.3V X5R 402

L8640 100NH-700MA-0.14OHM 0603
PP1V05_S0GPU
PP1V1_GPU_VID_PLLVDD_F 50mA
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 1UF 10% 6.3V X5R 402
C8631 0.1UF 10% 10V X5R 402

AF9 SP_PLLVDD
65mA
AE9 PLLVDD
AD9 VID_PLLVDD

GPU_CLK27M B1 XTAL_IN
NC_GPU_XTALOUT B2 XTAL_OUT
GPU_XTALOUTBUFF D1 XTAL_OUTBUFF
GPU_CLK27M_SS D2 XTAL_SSIN

GPU_STRAP<0> W5 STRAP0
GPU_STRAP<1> W7 STRAP1
GPU_STRAP<2> V7 STRAP2

GPIO0	K1	GPU_VCORE_VID3	B3
GPIO1	K2	DP_EG_HPD	B3
GPIO2	K3	GPU_VCORE_VID4	B3
GPIO3	H3	EG_LCD_PWR_EN	B3
GPIO4	H2	EG_BKLT_EN	B3
GPIO5	H1	GPU_VCORE_VID0	B3
GPIO6	H4	GPU_VCORE_VID1	B3
GPIO7	H5	GPU_VCORE_VID2	B3
GPIO8	H6	SMC_GFX_OVERTEMP_R	OD
GPIO9	J7	TP_GPU_GSTATE<0>	B3
GPIO10	K4	FB_VREF_UNTERM	B3
GPIO11	K5	GPU_GPIO_11	B3
GPIO12	H7	SMC_GFX_THROTTLE_R	OD
GPIO13	J4	FBVDD_ALTVO	B3
GPIO14	J6	NC_GPU_GPIO_14	B3
GPIO15	L1	NC_GPU_GPIO_15	B3
GPIO16	L2	GPU_GPIO_16	B3
GPIO17	L4	NC_GPU_GPIO_17	B3
GPIO18	M4	NC_GPU_GPIO_18	B3
GPIO19	L7	NC_GPU_GPIO_19	B3
GPIO20	L5	NC_GPU_GPIO_20	B3
GPIO21	K6	NC_GPU_GPIO_21	B3
GPIO22	L6	NC_GPU_GPIO_22	B3
GPIO23	M6	NC_GPU_GPIO_23	B3
JTAG_TCK	AP14	TP_GPU_JTAG_TCK	IN
JTAG_TDI	AN14	TP_GPU_JTAG_TDI	IN
JTAG_TDO	AN16	TP_GPU_JTAG_TDO	OUT
JTAG_TMS	AR14	TP_GPU_JTAG_TMS	IN
JTAG_TRST*	AP16	TP_GPU_JTAG_TRST_L	IN
MIOA_CLKIN	N4	NC_GPU_MIOA_CLKIN	IN
MIOA_CLKOUT	R4	NC_GPU_MIOA_CLKOUT_P	DIFF
MIOA_CLKOUT*	T4	NC_GPU_MIOA_CLKOUT_N	DIFF
MIOA_CTL3	P5	NC_GPU_MIOA_CTL3	B3
MIOA_DE	N2	TP_GPU_MIOA_DE	B3
MIOA_D0	N1	TP_GPU_MIOA_D<0>	B3
MIOA_D1	P4	TP_GPU_MIOA_D<1>	B3
MIOA_D2	P1	TP_GPU_MIOA_D<2>	B3
MIOA_D3	P2	TP_GPU_MIOA_D<3>	B3
MIOA_D4	P3	TP_GPU_MIOA_D<4>	B3
MIOA_D5	T3	TP_GPU_MIOA_D<5>	B3
MIOA_D6	T2	TP_GPU_MIOA_D<6>	B3
MIOA_D7	T1	TP_GPU_MIOA_D<7>	B3
MIOA_D8	U4	TP_GPU_MIOA_D<8>	B3
MIOA_D9	U1	TP_GPU_MIOA_D<9>	B3
MIOA_D10	U2	GPU_MIOA_D<10>	B3
MIOA_D11	U3	GPU_MIOA_D<11>	B3
MIOA_D12	R6	GPU_MIOA_D<12>	B3
MIOA_D13	T6	GPU_MIOA_D<13>	B3
MIOA_D14	N6	GPU_MIOA_D<14>	B3
MIOA_HSYNC	N3	NC_GPU_MIOA_HSYNC	B3
MIOA_VSYNC	L3	NC_GPU_MIOA_VSYNC	B3
MIOB_CLKIN	AE1	NC_GPU_MIOB_CLKIN	IN
MIOB_CLKOUT	V4	NC_GPU_MIOB_CLKOUT_P	DIFF
MIOB_CLKOUT*	W4	NC_GPU_MIOB_CLKOUT_N	DIFF
MIOB_CTL3	W3	NC_GPU_MIOB_CTL3	B3
MIOB_DE	Y5	NC_GPU_MIOB_DE	B3
MIOB_D0	Y1	NC_GPU_MIOB_D<0>	B3
MIOB_D1	Y2	NC_GPU_MIOB_D<1>	B3
MIOB_D2	Y3	NC_GPU_MIOB_D<2>	B3
MIOB_D3	AB3	NC_GPU_MIOB_D<3>	B3
MIOB_D4	AB2	NC_GPU_MIOB_D<4>	B3
MIOB_D5	AB1	NC_GPU_MIOB_D<5>	B3
MIOB_D6	AC4	NC_GPU_MIOB_D<6>	B3
MIOB_D7	AC1	NC_GPU_MIOB_D<7>	B3
MIOB_D8	AC2	NC_GPU_MIOB_D<8>	B3
MIOB_D9	AC3	NC_GPU_MIOB_D<9>	B3
MIOB_D10	AE3	NC_GPU_MIOB_D<10>	B3
MIOB_D11	AE2	NC_GPU_MIOB_D<11>	B3
MIOB_D12	U6	NC_GPU_MIOB_D<12>	B3
MIOB_D13	W6	NC_GPU_MIOB_D<13>	B3
MIOB_D14	Y6	NC_GPU_MIOB_D<14>	B3
MIOB_HSYNC	W1	NC_GPU_MIOB_HSYNC	B3
MIOB_VSYNC	W2	NC_GPU_MIOB_VSYNC	B3
THERMDP	B5	GPU_TDIODE_P	IN
THERMDN	B4	GPU_TDIODE_N	OUT

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
NV GT216 GPIO/MIO/MISC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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DATE 2009-07-01

GPIOs

GPU_VCORE_VID3	GP	GPU_VCORE_VID3	MAKE_BASE=TRUE		79 80 82
DP_EG_HPD	HPDC	DP_EG_HPD	MAKE_BASE=TRUE	IN	79 80 84
GPU_VCORE_VID4	LCD0_BL_PWM	GPU_VCORE_VID4	MAKE_BASE=TRUE		79 80 82
EG_LCD_PWR_EN	LCD0_VDD	EG_LCD_PWR_EN	MAKE_BASE=TRUE		79 80 87
EG_BKLT_EN	LCD0_BL_EN	EG_BKLT_EN	MAKE_BASE=TRUE		79 80 87
GPU_VCORE_VID0	VID0	GPU_VCORE_VID0	MAKE_BASE=TRUE		79 80 82
GPU_VCORE_VID1	VID1	GPU_VCORE_VID1	MAKE_BASE=TRUE		79 80 82
GPU_VCORE_VID2	VID2/MEM_VID	GPU_VCORE_VID2	MAKE_BASE=TRUE		79 80 82
SMC_GFX_OVERTEMP_R_L	THERM	SMC_GFX_OVERTEMP_R_L	MAKE_BASE=TRUE		79 80
TP_GPU_GSTATE<0>	FAN_PWM	TP_GPU_GSTATE<0>	MAKE_BASE=TRUE		6 79 80
FB_VREF_UNTERM	MEM_VREF	FB_VREF_UNTERM	MAKE_BASE=TRUE		77 78 79 80
GPU_GPIO_11	SLI_SYNC	TP_GPU_GSTATE<1>	MAKE_BASE=TRUE	OUT	6
SMC_GFX_THROTTLE_R_L	PWR_CTL	SMC_GFX_THROTTLE_R_L	MAKE_BASE=TRUE	OUT	79 80
FBVDD_ALTVO	PWR_CTL0	FBVDD_ALTVO	MAKE_BASE=TRUE	OUT	79 80 86
NC_GPU_GPIO_14	PWR_CTL1	NC_GPU_GPIO_14	MAKE_BASE=TRUE		79 80

GPIOs

NC_GPU_GPIO_15	HPDE	NC_GPU_GPIO_15	MAKE_BASE=TRUE		79 80
GPU_GPIO_16	DVI_MODE0	EG_DP_CA_DET			80
NC_GPU_GPIO_17	HDMI_DETECT0	NC_GPU_GPIO_17	MAKE_BASE=TRUE		79 80
NC_GPU_GPIO_18	DVI_MODE1	NC_GPU_GPIO_18	MAKE_BASE=TRUE		79 80
NC_GPU_GPIO_19	HDMI_DETECT1	NC_GPU_GPIO_19	MAKE_BASE=TRUE		79 80
NC_GPU_GPIO_20	HPDD	NC_GPU_GPIO_20	MAKE_BASE=TRUE		79 80
NC_GPU_GPIO_21	HPDF	NC_GPU_GPIO_21	MAKE_BASE=TRUE		79 80
NC_GPU_GPIO_22	SWAPRDY_A	NC_GPU_GPIO_22	MAKE_BASE=TRUE		79 80
NC_GPU_GPIO_23	GP	NC_GPU_GPIO_23	MAKE_BASE=TRUE	NO_TEST=TRUE	79 80

Renamed signals

GPU_CLK27M	MAKE_BASE=TRUE	GPU_CLK27M		98 80 79 27
GPU_CLK27M_SS	MAKE_BASE=TRUE	GPU_CLK27M_SS		98 80 79
GPU_TDIODE_P	MAKE_BASE=TRUE	GPU_TDIODE_P		99 80 79 51
GPU_TDIODE_N	MAKE_BASE=TRUE	GPU_TDIODE_N		99 80 79 51
LVDS_EG_DDC_CLK	MAKE_BASE=TRUE	LVDS_EG_DDC_CLK		84 81 80
LVDS_EG_DDC_DATA	MAKE_BASE=TRUE	LVDS_EG_DDC_DATA		84 81 80
DP_EG_DDC_CLK	MAKE_BASE=TRUE	DP_EG_DDC_CLK		84 81 80
DP_EG_DDC_DATA	MAKE_BASE=TRUE	DP_EG_DDC_DATA		84 81 80

Unused signals

TP_GPU_JTAG_TCK	MAKE_BASE=TRUE	TP_GPU_JTAG_TCK		80 79
TP_GPU_JTAG_TDI	MAKE_BASE=TRUE	TP_GPU_JTAG_TDI		80 79
TP_GPU_JTAG_TDO	MAKE_BASE=TRUE	TP_GPU_JTAG_TDO		80 79
TP_GPU_JTAG_TMS	MAKE_BASE=TRUE	TP_GPU_JTAG_TMS		80 79
TP_GPU_JTAG_TRST_L	MAKE_BASE=TRUE	TP_GPU_JTAG_TRST_L		80 79
NC_FBA_MA<13>	MAKE_BASE=TRUE	NC_FBA_MA<13>	NO_TEST=TRUE	76 80
NC_FBB_MA<13>	MAKE_BASE=TRUE	NC_FBB_MA<13>	NO_TEST=TRUE	76 80

Unused I2C Buses

NC_GPU_I2CC_SCL	MAKE_BASE=TRUE	NC_GPU_I2CC_SCL	NO_TEST=TRUE	81 80
NC_GPU_I2CC_SDA	MAKE_BASE=TRUE	NC_GPU_I2CC_SDA	NO_TEST=TRUE	81 80
NC_GPU_I2CH_SCL	MAKE_BASE=TRUE	NC_GPU_I2CH_SCL	NO_TEST=TRUE	81 80
NC_GPU_I2CH_SDA	MAKE_BASE=TRUE	NC_GPU_I2CH_SDA	NO_TEST=TRUE	81 80

I2C5 ties into SMBus connection page

(I2C5 requires pullups even if not used)

NC_FB_B_UCS1_L	MAKE_BASE=TRUE	NC_FB_B_UCS1_L	NO_TEST=TRUE	76 80
NC_FB_B_LCS1_L	MAKE_BASE=TRUE	NC_FB_B_LCS1_L	NO_TEST=TRUE	76 80
NC_GPU_ROM_CS_L	MAKE_BASE=TRUE	NC_GPU_ROM_CS_L	NO_TEST=TRUE	79 80
NC_FB_A_UCS1_L	MAKE_BASE=TRUE	NC_FB_A_UCS1_L	NO_TEST=TRUE	76 80
NC_FB_A_LCS1_L	MAKE_BASE=TRUE	NC_FB_A_LCS1_L	NO_TEST=TRUE	76 80
NC_LVDS_EG_B_CLK_P	MAKE_BASE=TRUE	NC_LVDS_EG_B_CLK_P		80 81
NC_LVDS_EG_B_CLK_N	MAKE_BASE=TRUE	NC_LVDS_EG_B_CLK_N		80 81
NC_LVDS_EG_A_DATA_P<3>	MAKE_BASE=TRUE	NC_LVDS_EG_A_DATA_P<3>	NO_TEST=TRUE	80 81 98
NC_LVDS_EG_A_DATA_N<3>	MAKE_BASE=TRUE	NC_LVDS_EG_A_DATA_N<3>	NO_TEST=TRUE	80 81 98
NC_LVDS_EG_B_DATA_P<3>	MAKE_BASE=TRUE	NC_LVDS_EG_B_DATA_P<3>	NO_TEST=TRUE	80 81 98
NC_LVDS_EG_B_DATA_N<3>	MAKE_BASE=TRUE	NC_LVDS_EG_B_DATA_N<3>	NO_TEST=TRUE	80 81 98

G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.

NC_GPU_MIOA_CLKOUT_P	MAKE_BASE=TRUE	NC_GPU_MIOA_CLKOUT_P	NO_TEST=TRUE	80 79
NC_GPU_MIOA_CLKOUT_N	MAKE_BASE=TRUE	NC_GPU_MIOA_CLKOUT_N	NO_TEST=TRUE	80 79
NC_GPU_MIOA_CTL3	MAKE_BASE=TRUE	NC_GPU_MIOA_CTL3	NO_TEST=TRUE	80 79
TP_GPU_MIOA_DE	MAKE_BASE=TRUE	TP_GPU_MIOA_DE		80 79 6
TP_GPU_MIOA_D<9..0>	MAKE_BASE=TRUE	GPU_MIOA_D<9..0>		79 6
NC_GPU_MIOA_CLKIN	MAKE_BASE=TRUE	NC_GPU_MIOA_CLKIN	NO_TEST=TRUE	80 79
NC_GPU_MIOA_D<14..10>	MAKE_BASE=TRUE	GPU_MIOA_D<14..10>	NO_TEST=TRUE	79
NC_GPU_MIOA_HSYNC	MAKE_BASE=TRUE	NC_GPU_MIOA_HSYNC	NO_TEST=TRUE	80 79
NC_GPU_MIOA_VSYNC	MAKE_BASE=TRUE	NC_GPU_MIOA_VSYNC	NO_TEST=TRUE	80 79
NC_GPU_MIOB_CLKIN	MAKE_BASE=TRUE	NC_GPU_MIOB_CLKIN	NO_TEST=TRUE	80 79
NC_GPU_MIOB_CLKOUT_P	MAKE_BASE=TRUE	NC_GPU_MIOB_CLKOUT_P	NO_TEST=TRUE	80 79
NC_GPU_MIOB_CLKOUT_N	MAKE_BASE=TRUE	NC_GPU_MIOB_CLKOUT_N	NO_TEST=TRUE	80 79
NC_GPU_MIOB_CTL3	MAKE_BASE=TRUE	NC_GPU_MIOB_CTL3	NO_TEST=TRUE	80 79
NC_GPU_MIOB_DE	MAKE_BASE=TRUE	NC_GPU_MIOB_DE	NO_TEST=TRUE	80 79
NC_GPU_MIOB_D<14..0>	MAKE_BASE=TRUE	GPU_MIOB_D<14..0>	NO_TEST=TRUE	79
NC_GPU_MIOB_VSYNC	MAKE_BASE=TRUE	NC_GPU_MIOB_VSYNC	NO_TEST=TRUE	80 79
NC_GPU_MIOB_HSYNC	MAKE_BASE=TRUE	NC_GPU_MIOB_HSYNC	NO_TEST=TRUE	80 79

Config Straps

Physical

Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

PP3V3_S0GPU

R8707 2.0K 5% 1/10W MF-LF 402 — OMIT

R8709 4.99K 1% 1/10W MF-LF 402 — NO STUFF

R8711 15.0K 1% 1/10W MF-LF 402 — NO STUFF

GPU_ROM_SI (OUT)

GPU_ROM_SO (IN)

GPU_ROM_SCLK (IN)

R8708 45.3K 1% 1/10W MF-LF 402 — OMIT

R8710 10K 1% 1/10W MF-LF 402

R8712 15.0K 1% 1/10W MF-LF 402

Strap S1/S2 Bit[3:0] PU/PD Rval

0 0000 PD 5k
1 0001 PD 10k
2 0010 PD 15k (HYN 256)
3 0011 PD 20k (SAM 256)
4 0100 PD 25k (SAM 512)
5 0101 PD 30k
6 0110 PD 35k (HYN 512)
7 0111 PD 45k

Strap S1/S2 Bit[3:0] PU/PD Rval

8 1000 PU 5k
9 1001 PU 10k
A 1010 PU 15k
B 1011 PU 20k
C 1100 PU 25k
D 1101 PU 30k
E 1110 PU 35k
F 1111 PU 45k

PCI_DEVID[4:0]=0x14

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0353	1	RES,MTL FILM,1/16W,24.9K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0368	1	RES,MTL FILM,1/16W,35.7K,1,0402,SMD,LF	R8708		VRAM_512_HYNIX
114S0343	1	RES,MTL FILM,1/16W,20.0K,1,0402,SMD,LF	R8708		VRAM_256_SAMSUNG
114S0331	1	RES,MTL FILM,1/16W,15.0K,1,0402,SMD,LF	R8708		VRAM_256_HYNIX

PP3V3_S0GPU

R8701 45.3K 1% 1/10W MF-LF 402

R8703 34.8K 1% 1/10W MF-LF 402

R8705 10K 1% 1/10W MF-LF 402

GPU_STRAP<0> (BI)

GPU_STRAP<1> (BI)

GPU_STRAP<2> (BI)

R8702 2.0K 5% 1/10W MF-LF 402 — NO STUFF

R8704 10K 1% 1/10W MF-LF 402 — NO STUFF

R8706 24.9K 1% 1/10W MF-LF 402 — NO STUFF

PP3V3_S0

PP3V3_S0GPU

R8750 2.2K 5% 1/10W MF-LF 402

R8751 2.2K 5% 1/10W MF-LF 402

R8752 4.7K 5% 1/10W MF-LF 402

R8753 4.7K 5% 1/10W MF-LF 402

DP_EG_DDC_CLK (IN)

DP_EG_DDC_DATA (BI)

DP_IG_DDC_CLK (IN)

DP_IG_DDC_DATA (BI)

PP3V3_S0GPU

DP_CA_DET_EG_FET

R8742 100K 1% 1/10W MF-LF 402

Q8742 SOD-VESM-HF SSM3K15FV

EG_DP_CA_DET — DP_CA_DET (IN)

R8743 0 5% 1/10W MF-LF 402 — DP_CA_DET_EG (IN)

DP_CA_DET_EG_PLD

Isolation FETs for DP MUX inputs

PP3V3_S0GPU

R8796 2.2K 5% 1/10W MF-LF 402

R8797 2.2K 5% 1/10W MF-LF 402

SMC_GFX_OVERTEMP_R_L — R8798 0 NO STUFF 5% 1/16W MF-LF 402 — SMC_GFX_OVERTEMP_L (OUT)

SMC_GFX_THROTTLE_R_L — R8799 0 5% 1/16W MF-LF 402 — SMC_GFX_THROTTLE_L (OUT)

EG_LCD_PWR_EN (OUT)

EG_BKLT_EN (OUT)

FBVDD_ALTVO (OUT)

FB_VREF_UNTERM (OUT)

R8792 10K 5% 1/10W MF-LF 402

R8793 10K 5% 1/10W MF-LF 402

R8794 10K 5% 1/10W MF-LF 402

R8795 10K 5% 1/10W MF-LF 402 — NO STUFF

Unused Clocks

GPU_CLK27M_SS

GPU_XTALOUTBUFF

R8780 10K 5% 1/10W MF-LF 402 — GPU_SS_INT

R8781 10K 5% 1/10W MF-LF 402

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: GT216 GPIOS & STRAPS

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

72 7 6 PP1V8_GPUIFPX

CRITICAL
L8800
300-OHM-0.5A
0603-1

?mA peak per diff pair
?mA peak for all pairs

C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402

Place at AG9
Place at AG10

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

81 79 76 74 7 6 PP1V05_S0GPU

L8805
180-OHM-1.5A
0603

80mA peak

PP1V1_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V

C8805 4.7UF 20% 6.3V CERM 603
C8806 1UF 20% 6.3V CERM 402

GPU_IFPEF_RSET 81
GPU_IFPC_RSET 81
GPU_IFPAB_RSET 81
GPU_IFPD_RSET 81

R8855 1K 1% 1/16W MF-LF 402
R8850 1K 1% 1/16W MF-LF 402
R8851 1K 1% 1/16W MF-LF 402
R8858 1K 1% 1/16W MF-LF 402

86 81 79 76 74 7 6 PP1V05_S0GPU

L8810
180-OHM-1.5A
0603

?mA peak per diff pair
?mA peak for all pairs

PP1V1_GPU_IFPCD_IOVDD_F 81
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V

C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402

Place at AJ8
Place at AK8

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

CRITICAL
L8815
300-OHM-0.5A
0603-1

84 82 81 80 79 74 72 7 6 PP3V3_S0GPU

160mA peak

PP3V3_GPU_IFPC_PLLVDD_F 81
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C8815 4.7UF 20% 6.3V CERM 603
C8816 1UF 10% 6.3V CERM 402

I2CS must be pulled up if not used.
I2CS addr fixed at 0x9E,0x9F

PP1V1_GPU_IFPEF_IOVDD_F 81
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V

PP1V8_GPU_IFPEF_PLLVDD_F 81
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.8V

Power inputs must be pulled down if not used

R8856 10K 5% 1/16W MF-LF 402
R8857 10K 5% 1/16W MF-LF 402

OMIT

U8000
NV-GT216
BGA
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AG9	IFPA_IOVDD		
AG10	IFPB_IOVDD		
AJ8	IFPC_IOVDD		
AK8	IFPD_IOVDD		
AE7	IFPE_IOVDD		
AD7	IFPF_IOVDD		
AK9	IFPAB_PLLVDD		
AJ11	IFPAB_RSET		
AJ9	IFPC_PLLVDD		
AK7	IFPC_RSET		
AJ6	IFPEF_PLLVDD		
AL1	IFPEF_RSET		
G1	I2CA_SCL		
G4	I2CA_SDA		
E3	I2CC_SCL		
E4	I2CC_SDA		
E2	I2CS_SCL		
E1	I2CS_SDA		
F6	I2CH_SCL		
G6	I2CH_SDA		
G3	I2CB_SCL		
G2	I2CB_SDA		
AJ12	DACA_VDD		
AK12	DACA_VREF		
AK13	DACA_RSET		
AG7	DACB_VDD		
AK6	DACB_VREF		
AK7	DACB_RSET		
AC6	IFPD_PLLVDD		
AB6	IFPD_RSET		
		IFPA_TXC	AM11
		IFPA_TXC*	AM12
		IFPA_TXD0	AM8
		IFPA_TXD0*	AL8
		IFPA_TXD1	AM10
		IFPA_TXD1*	AM9
		IFPA_TXD2	AK10
		IFPA_TXD2*	AL10
		IFPA_TXD3	AK11
		IFPA_TXD3*	AL11
		IFPB_TXC	AP13
		IFPB_TXC*	AN13
		IFPB_TXD4	AN8
		IFPB_TXD4*	AP8
		IFPB_TXD5	AP10
		IFPB_TXD5*	AN10
		IFPB_TXD6	AR11
		IFPB_TXD6*	AR10
		IFPB_TXD7	AN11
		IFPB_TXD7*	AP11
		IFPC_AUX_I2CW_SCL	AP2
		IFPC_AUX_I2CW_SDA*	AN3
		IFPC_L0	AM7
		IFPC_L0*	AM6
		IFPC_L1	AL5
		IFPC_L1*	AM5
		IFPC_L2	AM3
		IFPC_L2*	AM4
		IFPC_L3	AP1
		IFPC_L3*	AR2
		IFPD_AUX_I2CX_SCL	AP4
		IFPD_AUX_I2CX_SDA*	AN4
		IFPD_L0	AP6
		IFPD_L0*	AP7
		IFPD_L1	AP5
		IFPD_L1*	AN7
		IFPD_L2	AN6
		IFPD_L2*	AR5
		IFPD_L3	AR6
		IFPD_L3*	AR4
		IFPE_AUX_I2CY_SCL	AE4
		IFPE_AUX_I2CY_SDA*	AD4
		IFPE_L0	AH6
		IFPE_L0*	AH5
		IFPE_L1	AJ4
		IFPE_L1*	AG5
		IFPE_L2	AE5
		IFPE_L2*	AE6
		IFPE_L3	AF6
		IFPE_L3*	AF5
		IFPF_AUX_I2CZ_SCL	AF3
		IFPF_AUX_I2CZ_SDA*	AF2
		IFPF_L0	AL2
		IFPF_L0*	AL3
		IFPF_L1	AJ3
		IFPF_L1*	AJ2
		IFPF_L2	AJ1
		IFPF_L2*	AH1
		IFPF_L3	AH2
		IFPF_L3*	AH3
		DACA_RED	AM16
		DACA_GREEN	AM14
		DACA_BLUE	AL14
		DACA_HSYNC	AM13
		DACA_VSYNC	AL13
		DACB_RED	AK4
		DACB_GREEN	AL4
		DACB_BLUE	AJ4
		CEC	AB5
		DACB_HSYNC	AM1
		DACB_VSYNC	AM2

LVDS_EG_DDC_CLK 84 86 B1
LVDS_EG_DDC_DATA 84 86 B1

NC_GPU_I2CC_SCL 86 B1
NC_GPU_I2CC_SDA 86 B1

SMBUS_SMC_0_S0_SCL 97 51 48 45 B1
SMBUS_SMC_0_S0_SDA 97 51 48 45 B1

NC_GPU_I2CH_SDA 86 B1
NC_GPU_I2CH_SCL 86 B1

DP_EG_DDC_CLK 84 86 B1
DP_EG_DDC_DATA 84 86 B1

IFPA_L0 OUT 87 98
IFPA_L0* OUT 87 98
IFPA_L1 OUT 87 98
IFPA_L1* OUT 87 98
IFPA_L2 OUT 87 98
IFPA_L2* OUT 87 98
IFPA_L3 OUT 87 98
IFPA_L3* OUT 87 98

LVDS_EG_A_CLK_P
LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>
LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<1>
LVDS_EG_A_DATA_N<1>
LVDS_EG_A_DATA_P<2>
LVDS_EG_A_DATA_N<2>
NC_LVDS_EG_A_DATA_P<3>
NC_LVDS_EG_A_DATA_N<3>

IFPB_L0 OUT 87 98
IFPB_L0* OUT 87 98
IFPB_L1 OUT 87 98
IFPB_L1* OUT 87 98
IFPB_L2 OUT 87 98
IFPB_L2* OUT 87 98
IFPB_L3 OUT 87 98
IFPB_L3* OUT 87 98

NC_LVDS_EG_B_CLK_P
NC_LVDS_EG_B_CLK_N
LVDS_EG_B_DATA_P<0>
LVDS_EG_B_DATA_N<0>
LVDS_EG_B_DATA_P<1>
LVDS_EG_B_DATA_N<1>
LVDS_EG_B_DATA_P<2>
LVDS_EG_B_DATA_N<2>
NC_LVDS_EG_B_DATA_P<3>
NC_LVDS_EG_B_DATA_N<3>

IFPC_AUX_I2CW_SCL OUT 84 98
IFPC_AUX_I2CW_SDA* OUT 84 98

DP_EG_AUX_CH_P
DP_EG_AUX_CH_N

IFPC_L0 OUT 84 98
IFPC_L0* OUT 84 98
IFPC_L1 OUT 84 98
IFPC_L1* OUT 84 98
IFPC_L2 OUT 84 98
IFPC_L2* OUT 84 98
IFPC_L3 OUT 84 98
IFPC_L3* OUT 84 98

DP_EG_ML_P<0>
DP_EG_ML_N<0>
DP_EG_ML_P<1>
DP_EG_ML_N<1>
DP_EG_ML_P<2>
DP_EG_ML_N<2>
DP_EG_ML_P<3>
DP_EG_ML_N<3>

NO STUFF
R8861 1K 5% 1/10W MF-LF 402

NO STUFF
R8860 1K 5% 1/10W MF-LF 402

IFPD_AUX_I2CX_SCL NC
IFPD_AUX_I2CX_SDA* NC
IFPD_L0 NC
IFPD_L0* NC
IFPD_L1 NC
IFPD_L1* NC
IFPD_L2 NC
IFPD_L2* NC
IFPD_L3 NC
IFPD_L3* NC

IFPE_AUX_I2CY_SCL NC
IFPE_AUX_I2CY_SDA* NC
IFPE_L0 NC
IFPE_L0* NC
IFPE_L1 NC
IFPE_L1* NC
IFPE_L2 NC
IFPE_L2* NC
IFPE_L3 NC
IFPE_L3* NC

IFPF_AUX_I2CZ_SCL NC
IFPF_AUX_I2CZ_SDA* NC
IFPF_L0 NC
IFPF_L0* NC
IFPF_L1 NC
IFPF_L1* NC
IFPF_L2 NC
IFPF_L2* NC
IFPF_L3 NC
IFPF_L3* NC

DACA_RED NC
DACA_GREEN NC
DACA_BLUE NC
DACA_HSYNC NC
DACA_VSYNC NC
DACB_RED NC
DACB_GREEN NC
DACB_BLUE NC
DACB_HSYNC NC
DACB_VSYNC NC

GPU_DACA_VDD
GPU_DACB_VDD
PP1V8_GPU_IFPD_PLLVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.8V

R8852 10K 5% 1/16W MF-LF 402
R8853 10K 5% 1/16W MF-LF 402
R8854 10K 5% 1/16W MF-LF 402

GPU_IFPD_RSET 81

PP3V3_S0GPU
6 7 72 74 79 80 81 82 84

R8859 10K 5% 1/16W MF-LF 402

GPU_CEC

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
NV GT216 VIDEO INTERFACES

Apple Inc.

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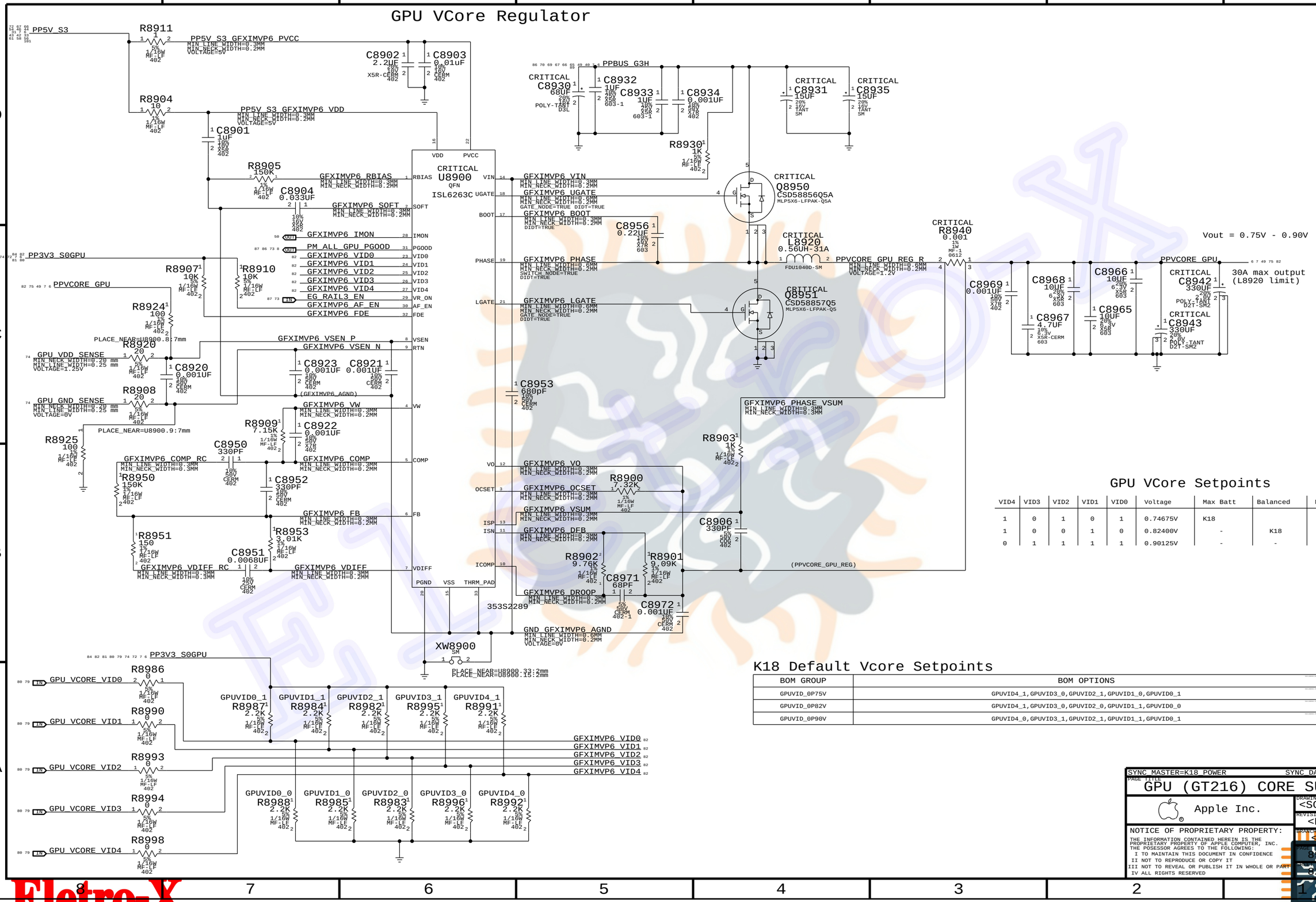
GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K18		-
1	0	0	1	0	0.82400V	-	K18	-
0	1	1	1	1	0.90125V	-	-	K18

K18 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P75V	GPUVID4_1,GPUVID3_0,GPUVID2_1,GPUVID1_0,GPUVID0_1
GPUVID_0P82V	GPUVID4_1,GPUVID3_0,GPUVID2_0,GPUVID1_1,GPUVID0_0
GPUVID_0P90V	GPUVID4_0,GPUVID3_1,GPUVID2_1,GPUVID1_1,GPUVID0_1

SYNC_MASTER=K18_POWER SYNC_DATE=07/14/2009

PAGE TITLE
GPU (GT216) CORE SUPPLY

Apple Inc.

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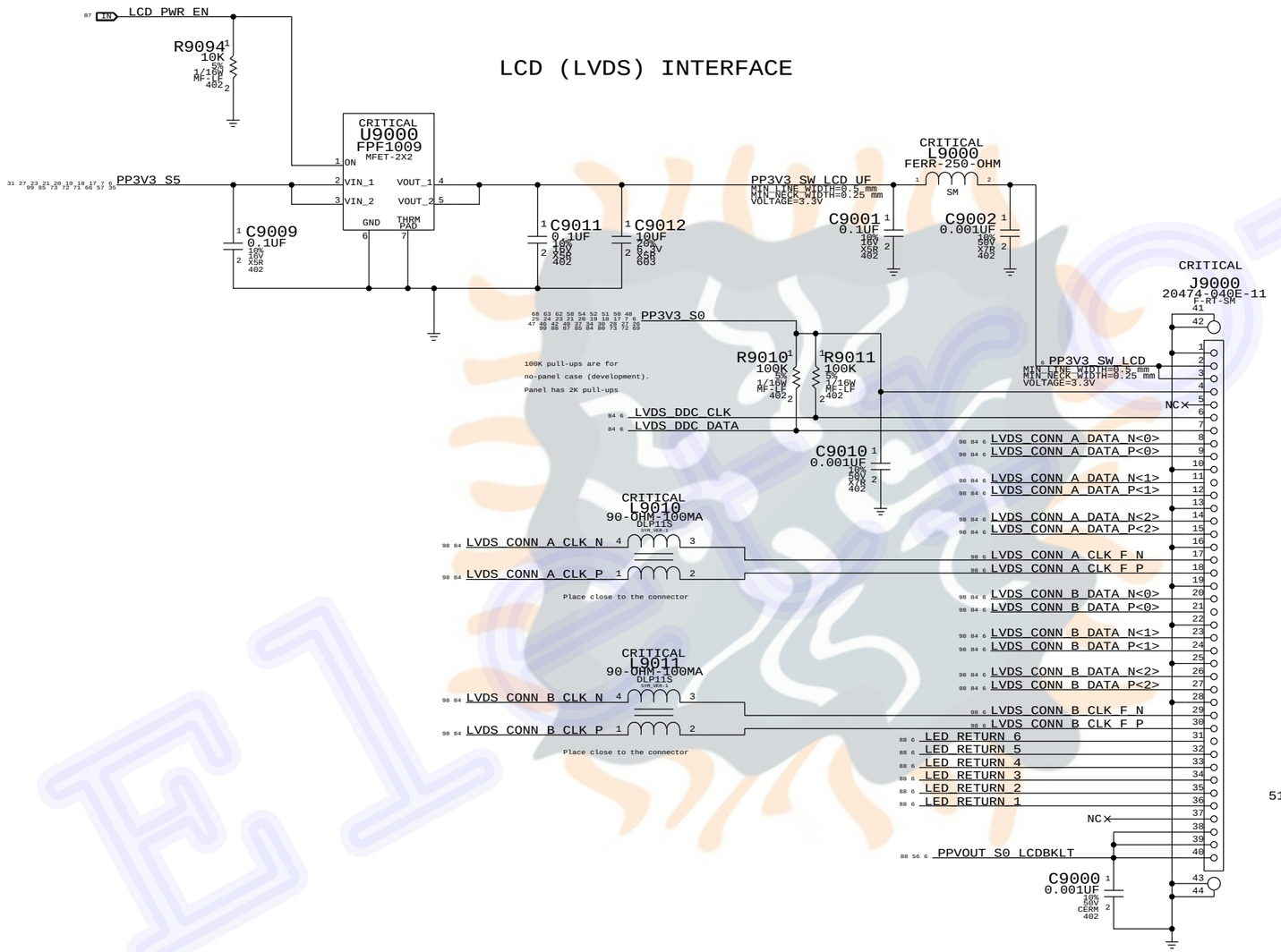
LCD (LVDS) INTERFACE



518S0651

SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE
LVDS Display Connector

Apple Inc.

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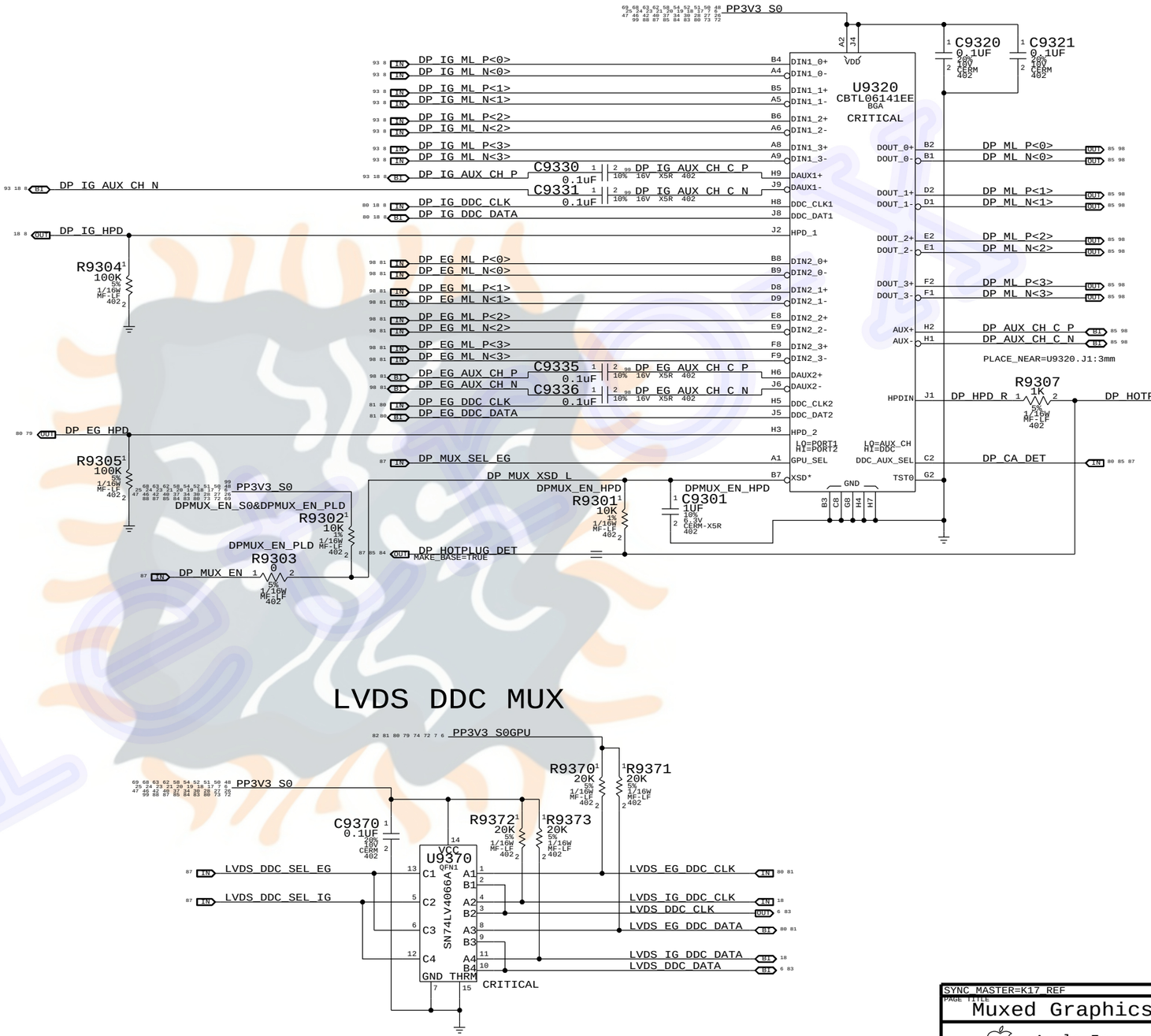
LVDS Transmitter Termination

All emulated LVDS outputs require this termination

DisplayPort Mux



LVDS DDC MUX

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE

Muxed Graphics Support

Apple Inc.

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Port Power Switch

CRITICAL
U9480
TPS2051B
SOT23

PP3V3_S5
PM_SLP_S3_L
TP_DPPWR_OC_L
PP3V3_S0_DPILIM
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
PP3V3_S0_DPPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

L9400
FERR-120-OHM-3A
0603

C9400 0.01UF 20% 50V CERM 603
C9480 10UF 20% 6.3V X5R 603
C9481 0.1UF 20% 16V CERM 402
C9485 0.1UF 20% 16V CERM 402
CRITICAL
C9486 22UF 20% 6.3V X5R CERM 603
CRITICAL
C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM
R9420 100K 5% 1/16W MF-LF 402

DP_ESD
CRITICAL
D9410
RCLAMP0524P
SLP2510P8

DP_ESD
CRITICAL
D9410
RCLAMP0524P
SLP2510P8

R9400 0 NO STUFF 5% 1/16W MF-LF 402
R9430 0 NO STUFF 5% 1/16W MF-LF 402
R9401 0 NO STUFF 5% 1/16W MF-LF 402
R9431 0 NO STUFF 5% 1/16W MF-LF 402

HDMI_CEC

R9425 1M 5% 1/16W MF-LF 402

R9403 0 NO STUFF 5% 1/16W MF-LF 402
R9413 0 NO STUFF 5% 1/16W MF-LF 402

CRITICAL
FL9403
12-OHM-100MA
TCM1210-4SM

DP_ML_P<3> C9414 0.1uF 10% 16V X5R 402 DP_ML_C_P<3>
DP_ML_N<3> C9415 0.1uF 10% 16V X5R 402 DP_ML_C_N<3>
DP_AUX_CH_C_P
DP_AUX_CH_C_N

DP_ML_CONN_P<3>
DP_ML_CONN_N<3>

CRITICAL
J9400
DSPLYPRT-M97-1
F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS
	HOT_PLUG_DETECT	GND
	CONFIG1	ML_LANE0P
	CONFIG2	ML_LANE0N
	GND	GND
	ML_LANE3P	ML_LANE1P
	ML_LANE3N	ML_LANE1N
	GND	GND
	AUX_CHP	ML_LANE2P
	AUX_CHN	ML_LANE2N
	DP_PWR	RETURN

SHIELD PINS

DP_ML_CONN_P<0>
DP_ML_CONN_N<0>
DP_ML_CONN_P<1>
DP_ML_CONN_N<1>
DP_ML_CONN_P<2>
DP_ML_CONN_N<2>

FL9401
12-OHM-100MA
TCM1210-4SM

CRITICAL
FL9400
12-OHM-100MA
TCM1210-4SM

DP_ML_C_P<0> C9410 0.1uF 10% 16V X5R 402 DP_ML_P<0>
DP_ML_C_N<0> C9411 0.1uF 10% 16V X5R 402 DP_ML_N<0>
DP_ML_C_P<1> C9412 0.1uF 10% 16V X5R 402 DP_ML_P<1>
DP_ML_C_N<1> C9413 0.1uF 10% 16V X5R 402 DP_ML_N<1>
DP_ML_C_P<2> C9416 0.1uF 10% 16V X5R 402 DP_ML_P<2>
DP_ML_C_N<2> C9417 0.1uF 10% 16V X5R 402 DP_ML_N<2>

FL9402
12-OHM-100MA
TCM1210-4SM
CRITICAL

R9402 0 NO STUFF 5% 1/16W MF-LF 402
R9432 0 NO STUFF 5% 1/16W MF-LF 402

PP3V3_S0

R9443 100K 5% 1/16W MF-LF 402
R9442 100K 5% 1/16W MF-LF 402

DP_CA_DET
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_L_Q
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q

R9421 100K 5% 1/16W MF-LF 402

DP_ESD
CRITICAL
D9411
RCLAMP0524P
SLP2510P8

DP_ESD
CRITICAL
D9400
RCLAMP0504F
SC70-6-1

DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

R9422 1M 5% 1/16W MF-LF 402

Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm

DP_ESD
CRITICAL
D9411
RCLAMP0524P
SLP2510P8

PP3V3_S0

R9445 10K 5% 1/16W MF-LF 402
R9444 10K 5% 1/16W MF-LF 402

DP_HOTPLUG_DET
Q9441 2N7002DW-X-G SOT-363
DP_HPD_L_Q
Q9441 2N7002DW-X-G SOT-363
DP_HPD_Q

R9423 100K 5% 1/16W MF-LF 402

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

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DisplayPort Connector

Apple Inc.

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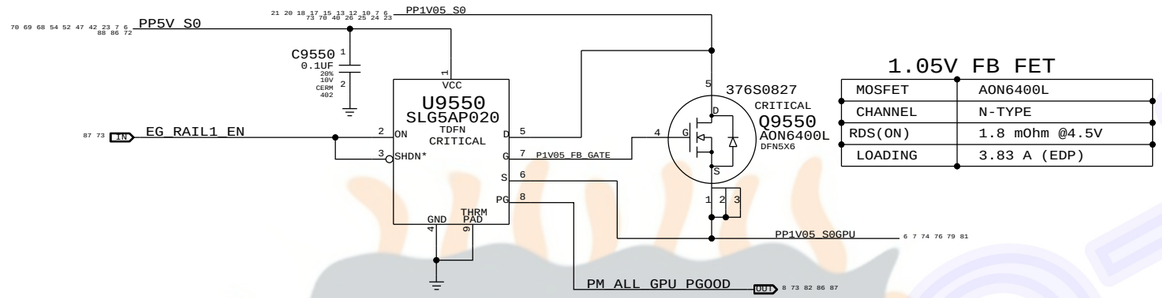
1V05 S0 GPU FET

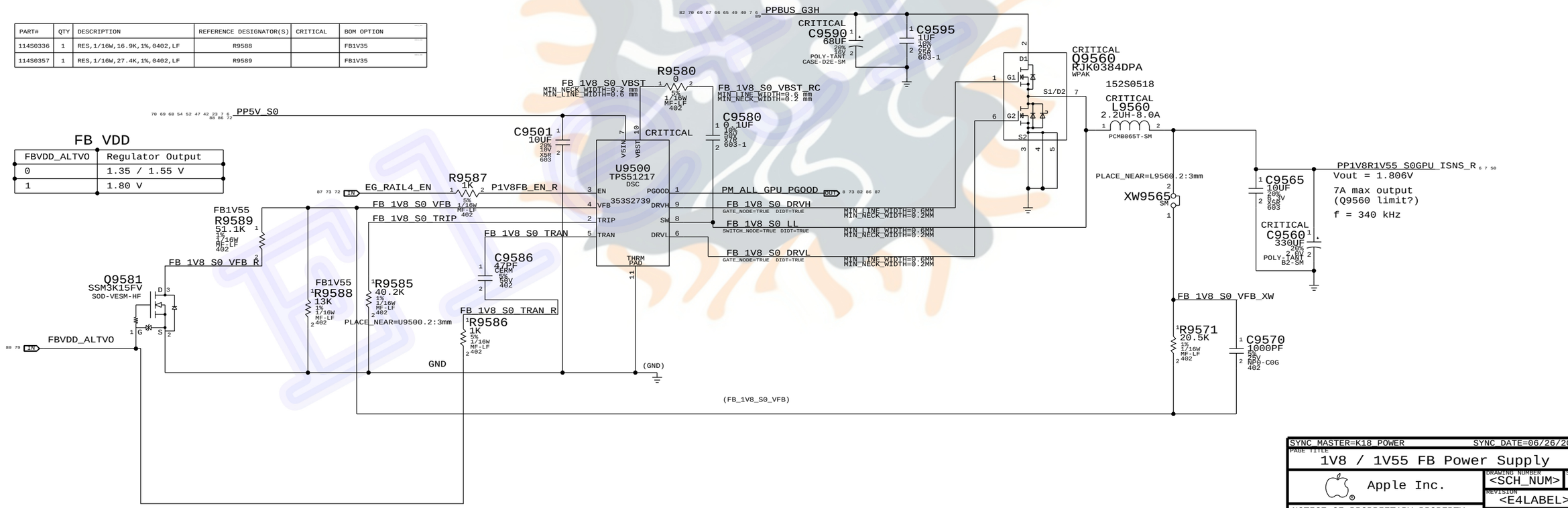


1.05V FB FET	
MOSFET	AON6400L
CHANNEL	N-TYPE
RDS(ON)	1.8 mOhm @4.5V
LOADING	3.83 A (EDP)

1V8 / 1V55 / 1V35 S0 FRAMEBUFFER REGULATOR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0336	1	RES,1/16W,16.9K,1%,0402,LF	R9588		FB1V35
114S0357	1	RES,1/16W,27.4K,1%,0402,LF	R9589		FB1V35

FB_VDD	
FBVDD_ALTVO	Regulator Output
0	1.35 / 1.55 V
1	1.80 V



SYNC_MASTER=K18_POWER	SYNC_DATE=06/26/2009
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GMUX CPLD

LVDS Receiver Termination

LVDS_IG_A_CLK_P	R9650	100	PLACE_NEAR=U9600.H3:5mm	LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_P<0>	R9651	100	PLACE_NEAR=U9600.E1:5mm	LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<1>	R9652	100	PLACE_NEAR=U9600.E3:5mm	LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<2>	R9653	100	PLACE_NEAR=U9600.G1:5mm	LVDS_IG_A_DATA_N<2>
LVDS_IG_B_DATA_P<0>	R9654	100	PLACE_NEAR=U9600.G2:5mm	LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_P<1>	R9655	100	PLACE_NEAR=U9600.G3:5mm	LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_P<2>	R9656	100	PLACE_NEAR=U9600.B2:5mm	LVDS_IG_B_DATA_N<2>
LVDS_EG_A_CLK_P	R9660	100	PLACE_NEAR=U9600.J12:5mm	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>	R9661	100	PLACE_NEAR=U9600.D13:5mm	LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<1>	R9662	100	PLACE_NEAR=U9600.E14:5mm	LVDS_EG_A_DATA_N<1>
LVDS_EG_A_DATA_P<2>	R9663	100	PLACE_NEAR=U9600.E12:5mm	LVDS_EG_A_DATA_N<2>
LVDS_EG_B_DATA_P<0>	R9664	100	PLACE_NEAR=U9600.G14:5mm	LVDS_EG_B_DATA_N<0>
LVDS_EG_B_DATA_P<1>	R9665	100	PLACE_NEAR=U9600.G13:5mm	LVDS_EG_B_DATA_N<1>
LVDS_EG_B_DATA_P<2>	R9666	100	PLACE_NEAR=U9600.H12:5mm	LVDS_EG_B_DATA_N<2>

All: 1% 1/16W MF-LF 402

Required Pullups

SIGNAL_MODEL=EMPTY

PP3V3_S0

GMUX_DEBUG_RESET_L	R9680	1K	5% 1/16W MF-LF 402
EG_PWRSEQ_EN	R9684	1K	5% 1/16W MF-LF 402

NO STUFF
R9679 10K 1% 1/16W MF-LF 402
SILK_PART=GMUX_RST

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K	5% 1/16W MF-LF 402
LVDS_DDC_SEL_IG	R9682	10K	5% 1/16W MF-LF 402
LVDS_DDC_SEL_EG	R9683	10K	5% 1/16W MF-LF 402
EG_RESET_L	R9691	100K	5% 1/16W MF-LF 402
LCD_BKLT_PWM	R9693	100K	5% 1/16W MF-LF 402

NO STUFF

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

PP3V3_S0 — R9600 0 5% 1/16W MF-LF 402

C9610–C9629 0.1UF 20% 10V CERM 402

PP1V8_S0 — R9610 0 5% 1/16W MF-LF 402

C9611–C9617 0.1UF 20% 10V CERM 402

PP1V2_S0

C9600 4.7UF 20% 10V X5R 402

C9604–C9609 0.1UF 20% 10V CERM 402

PP1V8_S0_GMUX_R — MIN_LINE_WIDTH=0.4mm MIN_NECK_WIDTH=0.09mm VOLTAGE=1.8V

GMUXPLL_1V8 — R9611 0 5% 1/16W MF-LF 402 — PP3V3R1V8_S0_GMUX — MIN_LINE_WIDTH=0.4mm MIN_NECK_WIDTH=0.2mm VOLTAGE=3.3V

GMUXPLL_3V3 — R9612 0 5% 1/16W MF-LF 402 — PP3V3_S0

PP3V3R1V8_S0_GMUX_ULC_VCCPLL — MIN_LINE_WIDTH=0.4mm MIN_NECK_WIDTH=0.09mm VOLTAGE=3.3V — L9621 FERR-220-OHM 0402 — C9631 0.1UF 20% 10V CERM 402

PP3V3R1V8_S0_GMUX_LRC_VCCPLL — MIN_LINE_WIDTH=0.4mm MIN_NECK_WIDTH=0.09mm VOLTAGE=3.3V — L9620 FERR-220-OHM 0402 — C9630 0.1UF 20% 10V CERM 402

PP3V3_S0

R9640 10K 1% 1/16W MF-LF 402 — R9645 10K 1% 1/16W MF-LF 402

NO STUFF R9641 10K 1% 1/16W MF-LF 402 — NO STUFF R9646 10K 1% 1/16W MF-LF 402

CRITICAL
J9600
1909782
M-RT-SM
GMUX_JTAG_CONN

1	PP3V3_S0
2	JTAG_GMUX_TDO
3	JTAG_GMUX_TDI
4	JTAG_GMUX_TMS
6	JTAG_GMUX_TCK

NO STUFF R9647 10K 1% 1/16W MF-LF 402

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

PP3V3_S0 — NO STUFF R9670 10K 1% 1/16W MF-LF 402 — GMUX_VSYNC

U9600
XP25-5
CSBGA

OMIT
CRITICAL

JTAG_GMUX_TCK	K14	TCK	
JTAG_GMUX_TDI	L13	TDI	
JTAG_GMUX_TDO	K13	TDO	
JTAG_GMUX_TMS	L12	TMS	
GMUX_TOE	K2	TOE	
GMUX_CFG0	K1	CFG0	
LCD_BKLT_EN	P2	PB7A	
LCD_BKLT_PWM	N2	PB7B	
LVDS_DDC_SEL_EG	P4	PB14A	
LVDS_DDC_SEL_IG	N4	PB14B	
DP_MUX_EN	N3	PB15A(OD)	
DP_MUX_SEL_EG	M4	PB15B	
EG_RESET_L	P5	PB16A	
EG_RAIL1_EN	M5	PB16B	
EG_RAIL2_EN	P6	PB17A	
EG_RAIL3_EN	M6	PB17B	
EG_RAIL4_EN	P7	PB18A	
PEG_CLKREQ_L	M7	PB18B(OD)	
DP_CA_DET_EG	N7	PB19A	
LCD_PWR_EN	N8	PB19B	
LPC_AD<0>	P9	PB20A	BANK4
LPC_AD<1>	N9	PB20B	
LPC_AD<2>	P10	PB26A	
LPC_AD<3>	M10	PB26B	
LPC_FRAME_L	P12	PB27A	
LPCPLUS_RESET_L	P13	PB27B	
LPC_CLK33M_GMUX	N12	PB28A	
GMUX_INT	P14	PB28B	
LVDS_IG_B_DATA_P<2>	B1	PL2A	BANK7
LVDS_IG_B_DATA_N<2>	B2	PL2B	
GMUX_PL10A	C2	PL6A	
TP_GMUX_PL10B	D3	PL6B	
LVDS_IG_A_DATA_P<0>	D1	PL7A	
LVDS_IG_A_DATA_N<0>	E1	PL7B	
LVDS_IG_A_DATA_P<1>	D2	PL8A	
LVDS_IG_A_DATA_N<1>	E3	PL8B	
LVDS_IG_A_DATA_P<2>	F1	PL9A	
LVDS_IG_A_DATA_N<2>	G1	PL9B	
LVDS_IG_B_DATA_P<0>	F3	PL10A	
LVDS_IG_B_DATA_N<0>	G2	PL10B	
LVDS_IG_B_DATA_P<1>	H2	PL11A	
LVDS_IG_B_DATA_N<1>	G3	PL11B	
LVDS_IG_A_CLK_P	H1	PL12A	
LVDS_IG_A_CLK_N	H3	PL12B	
TP_LVDS_MUX_SEL_EG	L1	PL14A	BANK6
GMUX_VSYNC	L3	PL14B	
GMUX_RESET_L	K3	PL15A	
GMUX_VSYNC	L2	PL15B	
PM_ALL_GPU_PGOOD	N1	PL25A	
PEX_CLKREQ_L	P1	PL25B	

VCC: C4 J3 J13 N11 P8 C11
VCCAUX: J2 J14 M8
VCCIO06 B5, VCCIO01 B7, VCCIO02 A12, VCCIO03 C14, VCCIO04 F13, VCCIO05 M12, VCCIO06 M9, VCCIO07 M3, N5, M1, C3, F2, K12
VCCJ A4
ULC_VCCPLL P11
LRC_VCCPLL

GND: J1 B8 C6 C12 C13 C13 F13 M14 N10 N6 P3 M2 C1 E2 B4 M11
GNDIO0 GNDIO1 GNDIO2 GNDIO3 GNDIO4 GNDIO5 GNDIO6 GNDIO7 ULC_GNDPLL LRC_GNDPLL

PT7A	A2	LVDS_B_DATA_P<0>	BANK0
PT7B	A3	LVDS_B_DATA_N<0>	
PT8A	A1	LVDS_B_DATA_P<1>	
PT8B	B3	LVDS_B_DATA_N<1>	
PT9A	C5	LVDS_B_DATA_P<2>	
PT9B	A5	LVDS_B_DATA_N<2>	
PT14A	B6	EG_PWRSEQ_EN	
PT14B	C7	GMUX_DEBUG_RESET_L	
PT15A	A6	LVDS_A_CLK_P	
PT15B	A7	LVDS_A_CLK_N	
PT16A	C8	LVDS_B_CLK_P	
PT16B	C9	LVDS_B_CLK_N	
PT17A	A8	LVDS_A_DATA_P<0>	
PT17B	B9	LVDS_A_DATA_N<0>	
PT18A	A9	LVDS_A_DATA_P<1>	
PT18B	C10	LVDS_A_DATA_N<1>	
PT19A	B10	LVDS_A_DATA_P<2>	
PT19B	A10	LVDS_A_DATA_N<2>	
PT20A	A11	GND	BANK1
PT20B	B12	GND	
PT28A	B13	GND	
PT28B	A13	GND	
PR2A	A14	DP_CA_DET	BANK2
PR2B	B14	DP_HOTPLUG_DET	
PR6A	D12	LVDS_EG_A_DATA_P<0>	
PR6B	D13	LVDS_EG_A_DATA_N<0>	
PR7A	D14	LVDS_EG_A_DATA_P<1>	
PR7B	E14	LVDS_EG_A_DATA_N<1>	
PR8A	E12	LVDS_EG_A_DATA_P<2>	
PR8B	F12	LVDS_EG_A_DATA_N<2>	
PR9A	F14	LVDS_EG_B_DATA_P<0>	
PR9B	G14	LVDS_EG_B_DATA_N<0>	
PR10A	G12	LVDS_EG_B_DATA_P<1>	
PR10B	G13	LVDS_EG_B_DATA_N<1>	
PR11A	H13	LVDS_EG_B_DATA_P<2>	
PR11B	H12	LVDS_EG_B_DATA_N<2>	
PR12A	H14	LVDS_EG_A_CLK_P	
PR12B	J12	LVDS_EG_A_CLK_N	
PR14A	L14	LVDS_IG_PANEL_PWR	BANK3
PR14B	M13	EG_LCD_PWR_EN	
PR24A	N14	LVDS_IG_BKL_ON	
PR24B	N13	EG_BKLT_EN	

EG_RAIL1_EN, EG_RAIL2_EN, EG_RAIL3_EN, EG_RAIL4_EN, LCD_PWR_EN

R9678 4.7K 5% 1/16W MF-LF 402
R9671 4.7K 5% 1/16W MF-LF 402
R9672 4.7K 5% 1/16W MF-LF 402
R9673 4.7K 5% 1/16W MF-LF 402
R9674 4.7K 5% 1/16W MF-LF 402

GMUX_S3_PD_GND

NO STUFF R9675 0 5% 1/16W MF-LF 402

PP3V3_S3 — R9676 100K 5% 1/16W MF-LF 402 — GMUX_S3_PD_EN

Q9607 SSM6N15FEAPE SOT563

Q9607 SSM6N15FEAPE SOT563

ALL_SYS_PWRGD

SYNC_MASTER=K17_REF		SYNC_DATE=06/15/2009	
PAGE TITLE	Graphics MUX (GMUX)		
Apple Inc.		DRAWING NUMBER <SCH_NUM>	SIZE D
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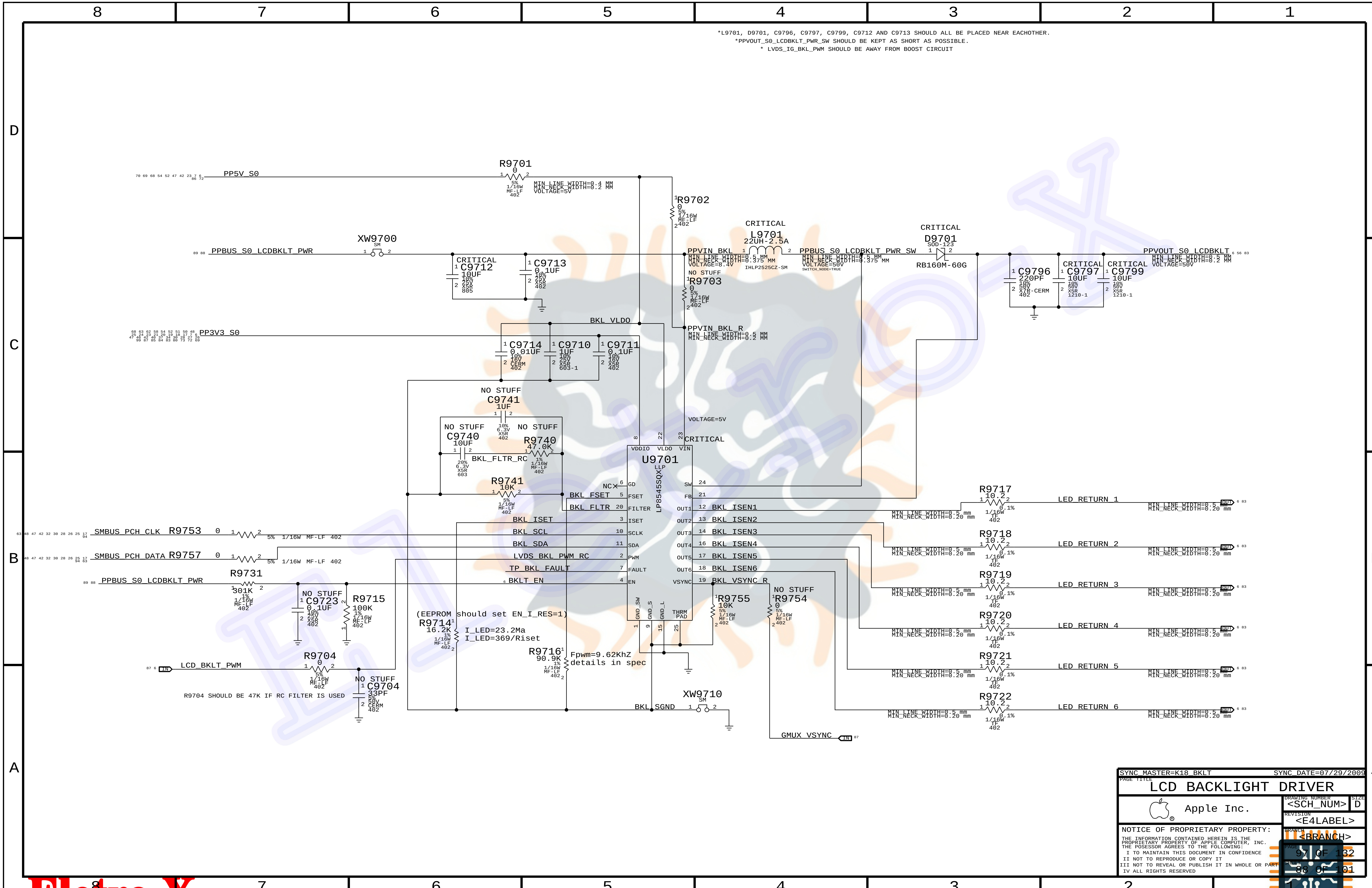

*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPVOUT_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
* LVDS_IG_BKL_PWM SHOULD BE AWAY FROM BOOST CIRCUIT
PP5V_S0
R9701
0
5%
1/16W
MF-LF
402
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
R9702
PPBUS_S0_LCDBKLT_PWR
XW9700
SM
CRITICAL
C9712
10UF
C9713
0.1UF
PPVIN_BKL
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=8.4V
CRITICAL
L9701
22UH-2.5A
IHLP2525CZ-SM
PPBUS_S0_LCDBKLT_PWR_SW
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=50V
SWITCH_NODE=TRUE
CRITICAL
D9701
SOD-123
RB160M-60G
PPVOUT_S0_LCDBKLT
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=50V
C9796
220PF
X7R-CERM
CRITICAL
C9797
10UF
1210-1
CRITICAL
C9799
10UF
1210-1
NO STUFF
R9703
PPVIN_BKL_R
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
BKL_VLDO
PP3V3_S0
C9714
0.01UF
C9710
1UF
C9711
0.1UF
NO STUFF
C9741
1UF
NO STUFF
C9740
10UF
NO STUFF
R9740
47.0K
BKL_FLTR_RC
VOLTAGE=5V
CRITICAL
U9701
LP8545SQX
LLP
VDDIO VLDO VIN
GD FSET FILTER ISET SCLK SDA PWM FAULT EN
SW FB OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 VSYNC
GND_SW GND_S GND_L THRM PAD
R9741
10K
BKL_FSET
BKL_FLTR
BKL_ISET
BKL_SCL
BKL_SDA
LVDS_BKL_PWM_RC
TP_BKL_FAULT
BKLT_EN
SMBUS_PCH_CLK R9753 0 5% 1/16W MF-LF 402
SMBUS_PCH_DATA R9757 0 5% 1/16W MF-LF 402
PPBUS_S0_LCDBKLT_PWR
R9731
301K
NO STUFF
C9723
0.1UF
R9715
100K
(EEPROM should set EN_I_RES=1)
R9714
16.2K
I_LED=23.2Ma
I_LED=369/Riset
R9716
90.9K
Fpwm=9.62KhZ
details in spec
LCD_BKLT_PWM
R9704
0
NO STUFF
C9704
33PF
R9704 SHOULD BE 47K IF RC FILTER IS USED
BKL_SGND
XW9710
SM
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6
BKL_VSYNC_R
R9755
10K
NO STUFF
R9754
0
GMUX_VSYNC
R9717 10.2 0.1%
R9718 10.2 0.1%
R9719 10.2 0.1%
R9720 10.2 0.1%
R9721 10.2 0.1%
R9722 10.2 0.1%
LED_RETURN_1
LED_RETURN_2
LED_RETURN_3
LED_RETURN_4
LED_RETURN_5
LED_RETURN_6
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm
SYNC_MASTER=K18_BKLT
SYNC_DATE=07/29/2009
PAGE TITLE
LCD BACKLIGHT DRIVER
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
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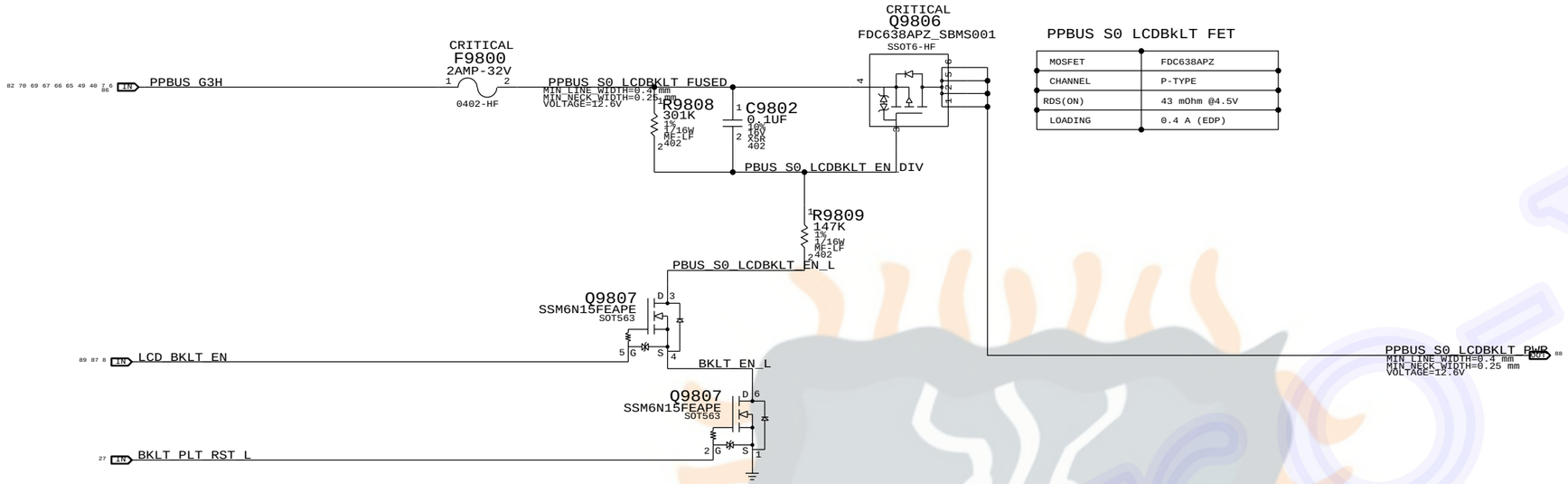
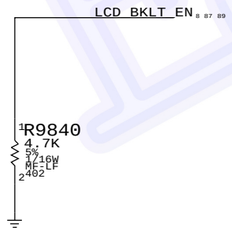


PPBUS S0 LCDBkLT FET	
MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)



SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE
LCD Backlight Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.1 and Table 4-184.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	9 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 18
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI_INT	9 18
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 20
FSB_CPURST_L	CPU_50S	CPU_AGTL	FSB_CPURST_L	10 25
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 18 31
CPU_VTT_S0_PGOOD	CPU_50S	CPU_AGTL	CPUVTTS0_PGOOD	10 70
XDP_XPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPUPWRGD	10 25
XDP_BDRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 25 27
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_PRDY_L	10 25
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_PREQ_L	10 25
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	10 46
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	10 46
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	10
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	8 9 25
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8 12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 46 68
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 20 25
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 20 46
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_CPU_P	10 20
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_CPU_N	10 20
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_ITP_P	10 25
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_ITP_N	10 25
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_CPU_P	10 17
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_CPU_N	10 17
	CPU_55S	CPU_8MIL	CPU_PSI_L	12 15 68
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	12 15 68
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	9
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	10
XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	25
XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	25
XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	10 25
XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	10 25
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<6..0>	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7>	10 25
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	25
	CPU_55S	CPU_8MIL	CPU_VID<6..0>	8 12 15
	CPU_50S	CPU_AGTL	CPUIMVP_IMON	12 50 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VTTSENSE_P	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VTTSENSE_N	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX_VSENSE_P	13 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX_VSENSE_N	13 69
	CPU_55S	CPU_8MIL	GFX_VID<6..0>	8 13
PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	13 69
	CPU_50S	CPU_AGTL	GFX_VR_EN	13 69
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	13 69
	PCIE_85D	PCIE	PEG_R2D_P<15..0>	74
	PCIE_85D	PCIE	PEG_R2D_N<15..0>	74
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8 9 74
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8 74
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8 9 74
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8 74
	PCIE_85D	PCIE	PEG_D2R_C_P<15..0>	74
	PCIE_85D	PCIE	PEG_D2R_C_N<15..0>	74

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: CPU Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0> 11 28
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0> 11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0> 11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0> 11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0> 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 11 28
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0> 11 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8> 11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16> 11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24> 11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32> 11 28 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40> 11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48> 11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56> 11 29
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DM<0> 11 28 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DM<1> 11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DM<2> 11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DM<3> 11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DM<4> 11 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DM<5> 11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DM<6> 11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DM<7> 11 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 11 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 11 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 11 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 11 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 11 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 11 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 11 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 11 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 11 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 11 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 11 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 11 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 11 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 11 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 11 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0> 11 30
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0> 11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0> 11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0> 11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0> 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 11 30
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0> 11 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8> 11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16> 11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24> 11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32> 11 29 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40> 11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48> 11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56> 11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DM<0> 11 29 30
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DM<1> 11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DM<2> 11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DM<3> 11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DM<4> 11 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DM<5> 11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DM<6> 11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DM<7> 11 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 11 29 30
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 11 29 30
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 11 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 11 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 11 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 11 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 11 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 11 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 11 29

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_P<3..0> 8 84
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_N<3..0> 8 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P 8 18 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N 8 18 84
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P 18 87
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N 18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0> 18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0> 18 87
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAP<3> 8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAN<3> 8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP_LVDS_IG_B_CLKP 6 8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP_LVDS_IG_B_CLKN 6 8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0> 18 87
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0> 18 87
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_B_DATAP<3> 8 18
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_B_DATAN<3> 8 18
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P 17 42
	SATA_90D	SATA	SATA_HDD_R2D_C_N 17 42
	SATA_90D	SATA	SATA_HDD_R2D_P 6 42
	SATA_90D	SATA	SATA_HDD_R2D_N 6 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P 17 42
	SATA_90D	SATA	SATA_HDD_D2R_N 17 42
	SATA_90D	SATA	SATA_HDD_D2R_C_P 6 42
	SATA_90D	SATA	SATA_HDD_D2R_C_N 6 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P 17 42
	SATA_90D	SATA	SATA_ODD_R2D_C_N 17 42
	SATA_90D	SATA	SATA_ODD_R2D_P 6 42
	SATA_90D	SATA	SATA_ODD_R2D_N 6 42
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P 17 42
	SATA_90D	SATA	SATA_ODD_D2R_N 17 42
	SATA_90D	SATA	SATA_ODD_D2R_C_P 6 42
	SATA_90D	SATA	SATA_ODD_D2R_C_N 6 42
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_P 42
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_N 42
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_P 42
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_N 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_P 42
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_N 42
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_P 42
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_N 42
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP 17
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P 19 35
	USB_85D	USB	USB_HUB1_UP_N 19 35
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P 19 36
	USB_85D	USB	USB_HUB2_UP_N 19 36
USB_EXTA	USB_85D	USB	USB_EXTA_P 36 43
	USB_85D	USB	USB_EXTA_N 36 43
USB_EXTB	USB_85D	USB	USB_EXTB_P 35 43
	USB_85D	USB	USB_EXTB_N 35 43
USB_EXTC	USB_85D	USB	USB_EXTC_P 8 35
	USB_85D	USB	USB_EXTC_N 8 35
USB_EXTD	USB_85D	USB	USB_EXTD_P
	USB_85D	USB	USB_EXTD_N
USB_MINI	USB_85D	USB	USB_MINI_P
	USB_85D	USB	USB_MINI_N
USB_WM	USB_85D	USB	USB_WM_P
	USB_85D	USB	USB_WM_N
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P 6 33
	USB_85D	USB	USB_CAMERA_CONN_N 6 33
USB_BT	USB_85D	USB	USB_BT_P 33 36
	USB_85D	USB	USB_BT_N 33 36
USB_TPAD	USB_85D	USB	USB_TPAD_P 36 53
	USB_85D	USB	USB_TPAD_N 36 53
USB_IR	USB_85D	USB	USB_IR_P 35 44
	USB_85D	USB	USB_IR_N 35 44
USB_SDCARD	USB_85D	USB	USB_SDCARD_P 8 34 36
	USB_85D	USB	USB_SDCARD_N 8 34 36
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT_P 19 101
	USB_85D	USB	USB_BRCRYPT_N 19 101
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS 19
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P 17 26
PCH_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N 17 26
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_P 17 26
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_N 17 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P 17 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N 17 26
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P 17 26
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N 17 26
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK 17 26
	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN 17 27
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_P 10 17
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_N 10 17

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 17 45 47 87
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 17 45 47 87
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 27 47 87
MCP_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	19 27
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	27 45
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 27 47
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	17 25 26 28 30 32 42 47 48 63 88
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	17 25 26 28 30 32 42 47 48 63 88
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	17 48
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	17 48
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	17 48
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	17 48
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	17 58
	HDA_50S	HDA	HDA_BIT_CLK_R	17
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	17 58
	HDA_50S	HDA	HDA_SYNC_R	17
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	17
	HDA_50S	HDA	HDA_RST_L	17 58
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	17 58
	HDA_50S	HDA	AUD_SDI_R	58
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	17 58
	HDA_50S	HDA	HDA_SDOUT_R	17
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	18 46
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	17 47
	SPI_55S	SPI	SPI_CLK	47
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	17 47
	SPI_55S	SPI	SPI_MOSI	47
SPI_MISO	SPI_55S	SPI	SPI_MISO	17 47
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	17 47
	SPI_55S	SPI	SPI_CS0_L	47
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	37
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	37
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	17 37
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	17 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	37
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 33
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 33
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	17 33
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	17 33
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 17 33
	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 17 33
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	17 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	17 39
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
PCIE_AP_D2R	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_N	
PCIE_AP_R2D	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_N	
MCP_PE0_REFCLK	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	17 74
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	17 74
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	17 37
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	17 37
MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	17 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	17 33
MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	17 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	17 39
MCP_PE3_REFCLK	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_P	8 17
	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_N	8 17
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<1>	6 20
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<2>	6 20
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<5>	6 20
	CPU_27P4S	CPU_COMP	TP_PCH_VSS_NCTF<7>	20
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 20 94
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 20 94
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<11>	6 20
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<12>	6 20
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<15>	6 20
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<17>	6 20
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<19>	6 20
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<21>	6 20
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<22>	20
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<25>	6 20
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<27>	6 20
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<29>	6 20

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CAESAR II (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

CAESAR II (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI 27 37
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO 27 37
	ENET_50S	ENET_3X	ENET_RESET_L 27 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0> 37 38
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0> 37 38

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: Ethernet Constraints

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP 6 39 41
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN 39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP 6 39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN 6 39 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P 39 40 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N 39 40 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P 39 40 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N 39 40 41
Port 2 Not Used			

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: FireWire Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL 6 33 45 48 54
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA 6 33 45 48 54
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL 45 48 51
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA 45 48 51
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL 45 48 51 81
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA 45 48 51 81
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL 6 45 48 64 65
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA 6 45 48 64 65
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL 45 48 56
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA 45 48 56

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 65
	1TO1_DIFFPAIR		CHGR_CSI_N 65
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 65
	1TO1_DIFFPAIR		CHGR_CSO_N 65

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

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SMC Constraints

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.095 MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_A_CLK	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>
FB_B_CLK	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<12..6>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_UCAS_L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_UCKE
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCKE
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCS0_L
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2>
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2>
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<0>
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<1>
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<2>
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<3>
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0>
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1>
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2>
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3>
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0>
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8>
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16>
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24>
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0>
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1>
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2>
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3>
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4>
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5>
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6>
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7>
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4>
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5>
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6>
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<7>
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32>
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40>
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48>
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56>
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4>
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5>
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6>
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7>

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(CK505_DATOBL)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0>
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0>
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_P<3>
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_N<3>
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0>
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0>
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_P<3>
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_N<3>
DP_ML	DP_85D	DISPLAYPORT	DP_EG_ML_P<3..0>
DP_ML	DP_85D	DISPLAYPORT	DP_EG_ML_N<3..0>
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_P
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_N
	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_C_P
	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_C_N

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_C_CLK	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>
FB_D_CLK	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<12..6>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_UCAS_L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_UCKE
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCKE
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCS0_L
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2>
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2>
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0>
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1>
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2>
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3>
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0>
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1>
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2>
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3>
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0>
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8>
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16>
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24>
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0>
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1>
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2>
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3>
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4>
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5>
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6>
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7>
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4>
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5>
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6>
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7>
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32>
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40>
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48>
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56>
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4>
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5>
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6>
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCAS_L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCAS_L

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0>
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0>
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0>
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0>
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0>
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0>
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0>
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0>
DP_ML	DP_85D	DISPLAYPORT	DP_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_ML_C_N<3..0>
DP_ML	DP_85D	DISPLAYPORT	DP_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_ML_N<3..0>
DP_ML	DP_85D	DISPLAYPORT	DP_ML_CONN_P<3..0>
	DP_85D	DISPLAYPORT	DP_ML_CONN_N<3..0>
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_AUX_CH_C_P
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_AUX_CH_C_N

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: GPU (GT216) CONSTRAINTS

Apple Inc.

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Eletro-X

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

K18 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	ENET_100D	ENETCONN	ENETCONN_P<3..0> 38
	ENET_100D	ENETCONN	ENETCONN_N<3..0> 38
	SATA_90D	SATA	SATA_ODD_R2D_UF_P 42
	SATA_90D	SATA	SATA_ODD_R2D_UF_N 42
	SATA_90D	SATA	SATA_ODD_D2R_UF_P 42
	SATA_90D	SATA	SATA_ODD_D2R_UF_N 42
	SATA_90D	SATA	SATA_HDD_D2R_UF_P 42
	SATA_90D	SATA	SATA_HDD_D2R_UF_N 42
	SATA_90D	SATA	SATA_HDD_R2D_UF_P 42
	SATA_90D	SATA	SATA_HDD_R2D_UF_N 42
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P 51
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N 51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P 9 51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_N 9 51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P 51
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N 51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P 51 79 80
	THERM_1TO1_55S	THERM	GPU_TDIODE_N 51 79 80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVTTISNS_R_N 50
	SENSE_1TO1_55S	SENSE	CPUVTTISNS_R_P 50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_N 50 70
	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_P 50 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_R_N 50
	SENSE_1TO1_55S	SENSE	DDRISNS_R_P 50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_N 69
	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_P 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_R_N 50 69
	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_R_P 50 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFX_ISNS_R_N 50
	SENSE_1TO1_55S	SENSE	GFX_ISNS_R_P 50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N 50
	SENSE_1TO1_55S	SENSE	GPUISENS_P 50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N 50 67
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P 50 67
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N 99
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N 99
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P 99
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P 99
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N 56
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P 56
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_N 49
	SENSE_1TO1_55S	SENSE	ISNS_CPU_P 49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N
	SENSE_1TO1_55S	SENSE	ISNS_HDD_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N 56
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P 56
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N
	SENSE_1TO1_55S	SENSE	ISNS_ODD_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N 56
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P 56
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_N 50
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_P 50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_N 50
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_P 50

K18 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P 6 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N 6 33
	1TO1_DIFFPAIR		CHGR_CSI_R_P 65
	1TO1_DIFFPAIR		CHGR_CSI_R_N 65
	1TO1_DIFFPAIR		CHGR_CSO_R_P 49 65
	1TO1_DIFFPAIR		CHGR_CSO_R_N 49 65
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P 43
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N 43
(USB_EXTA)	USB_85D	USB	USB2_LT1_P 6 43
(USB_EXTA)	USB_85D	USB	USB2_LT1_N 6 43
	USB_85D	USB	CONN_USB2_BT_P 6 33
	USB_85D	USB	CONN_USB2_BT_N 6 33
	USB_85D	USB	USB_LT2_P 6 43
	USB_85D	USB	USB_LT2_N 6 43
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_P 84
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_N 84
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P 6 61 62
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N 6 61 62
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P 6 61 62
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N 6 61 62
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P 6 61 62
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N 6 61 62
	USB_85D	USB	USB_TPAD_R_P 53
	USB_85D	USB	USB_TPAD_R_N 53
		SB_POWER	PP3V3_S5 6 7 17 18 19 20 21 23 27 31 35 57 68 71 72 73 83 85
		SB_POWER	PP3V3_S0 6 7 17 18 19 20 21 23 27 28 30 34 37 40 42 54 56 59 63 64 80 88 93 85
		SB_POWER	PP1V5_S3RS0 6 7 13 16 31 42 72 73
		GND	GND

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

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K18 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

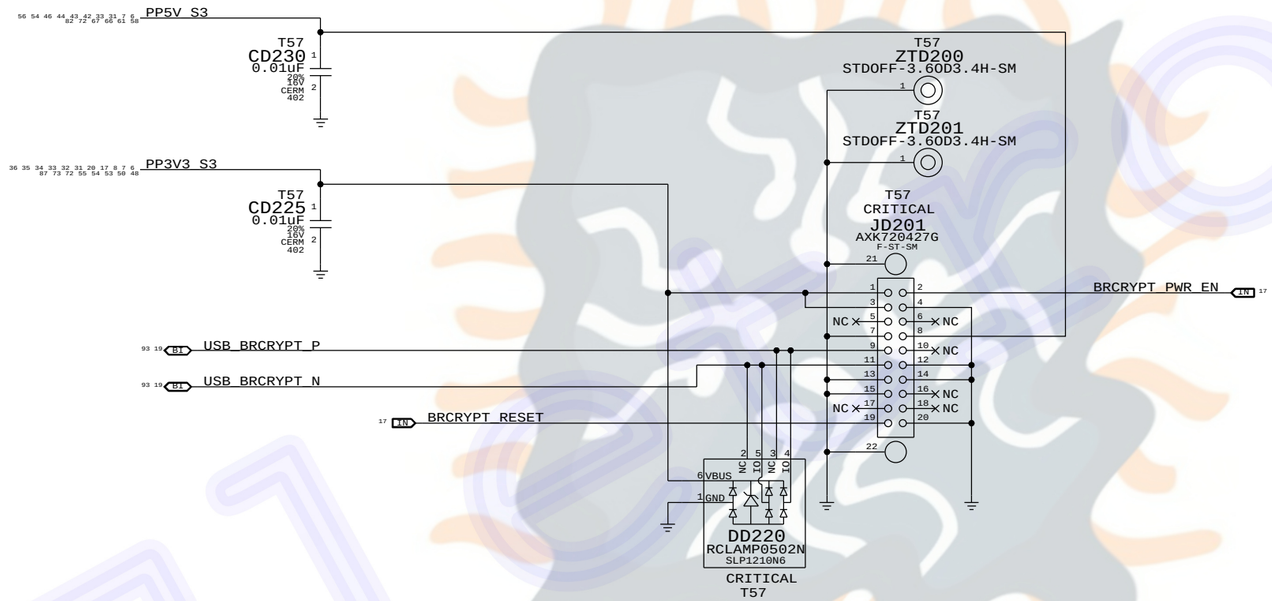
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.



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