

Table of Contents

GENEVA 2 EXT

CPU : Penryn
Chip Set : Cantiga + ICH9M
Remarks : Mobility Platform

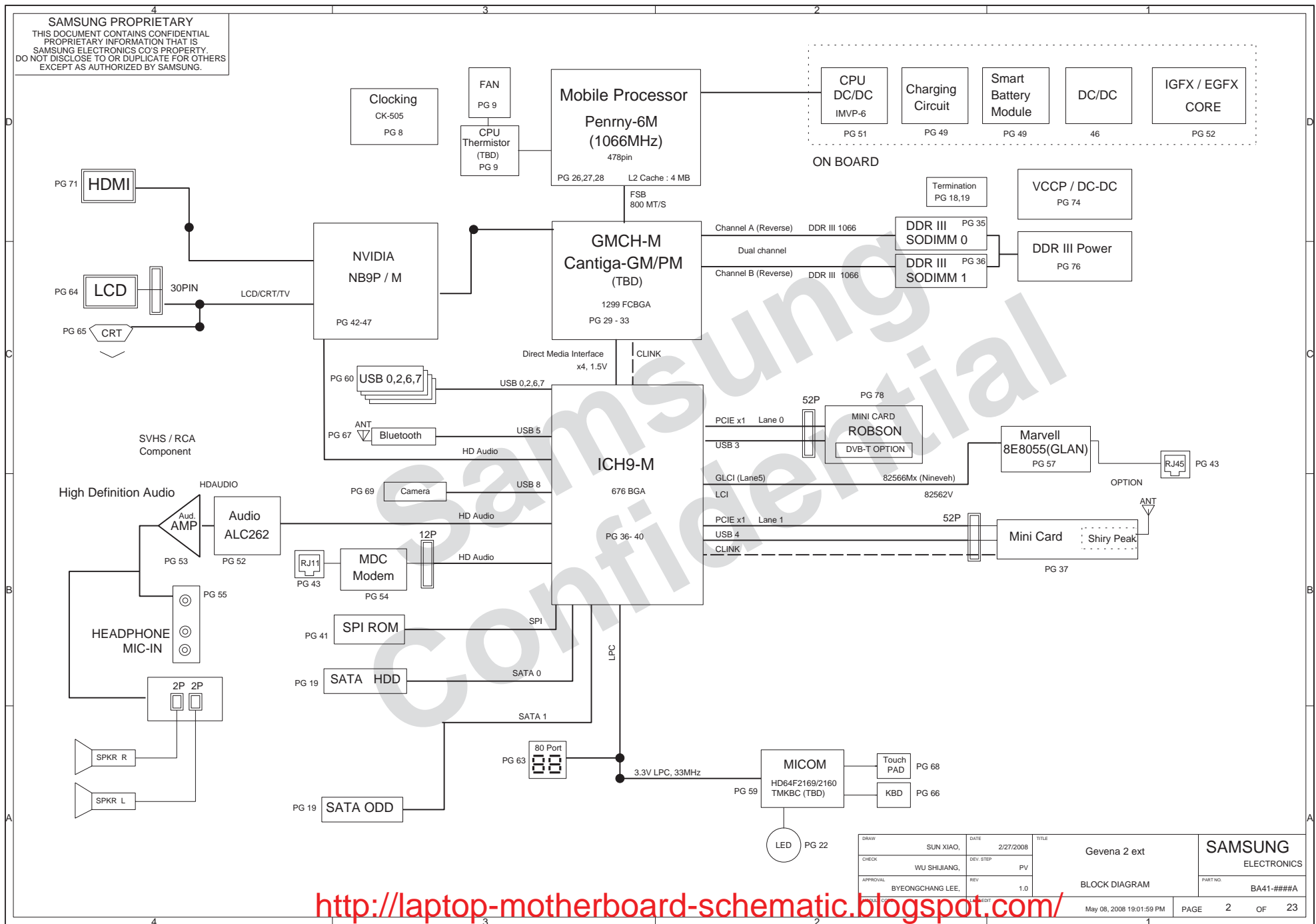
Model Name : GENEVA 2 EXT
PBA Name : MAIN
PCB Code : SGCE BA41-00930A
NAYA BA41-00936A
Dev. Step : PV1.0
Revision : 1.0
T.R. Date :

DRAW	CHECK	APPROVAL
SUN XIAO	WUSHIJIANG	BC.LEE

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0		COVER	
May 08, 2008 19:01:59 PM				PAGE	1	OF 23

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DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
DATE	May 08, 2008 19:01:59 PM					
BLOCK DIAGRAM						PAGE 2 OF 23

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	B,C,D
DT PCI SLOT	AD22	1	B,C,D,C
MiniPCI SLOT	AD23	2	A,B
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
MCH_CORE	Core Voltage for CPU
ICH1_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P1.05V_M	1.05V switched power rail for ME (on in M0/M1)
P1.25V_M	1.25V switched power rail for ME (on in M0/M1)
P3.3V_M	3.3V switched power rail for ME (on in M0/M1)
P3.3V_A	3.3V always power rail (by KBC3_ALWS_ON)
MICOM_P3V	3.3V always power rail (for Microm)
LAN_3.3V	3.3V always power rail (for LAN)
P1.5V	1.5V switched off power rail (off in S3-S5)
P1.5V_AUX	1.5V switched on power rail
P2.5V	2.5V switched off power rail (off in S3-S5)
P1.8V	1.8V switched off power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR
P0.9V	0.9V power rail for DDR
P3.3V	3.3V switched off power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail
PSV	5.0V switched off power rail (off in S3-S5)
PSV_AUX	5.0V switched on power rail

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	DMB
3	Expresas Card
4	DOCKING PORT 0
5	Bluetooth
6	Mini PCI Express
7	Aux Display
8	Test Port (RSVD)
9	WWAN/WIBRO (TBD)

PCI Express Assign

PORT #	ASSIGNED TO
0	PCIe x1 Slot
1	Mini Card (Golan)
2	Mini Card (WIBRO : RSVD)
3	Expresas Card
4	DOCKING PORT 0
5	GLAN

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	Intel LAN
Crystal	27MHz (TBD)	VIDEO	PEG
Crystal	24.576MHz (TBD)	HD Audio	Audio

LCD Pannel Detect

(TBD)

Devices	Resolution	PANNEL_DETECT_0

I²C / SMB Address

Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	1001 110x	9Ch	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
DB400 (PCI Express Clocks)	1101 110x	DCh	Clock Buffer for PCI Express
TBD	0100 1100	4Ch	Thermal Sensor
TBD : (LVDS BackLight Inverter)	0101 1000	58h	-
TBD : (ALS)	0111 0010	72h	Ambient Light Sensor
TBD : (AUX DISPLAY)	0011 110x	3Ch	EMA
LAN	1100 1000	C8h	82566
PCI Express Docking	TBD	TBD	TBD
TPM	TBD	TBD	TBD

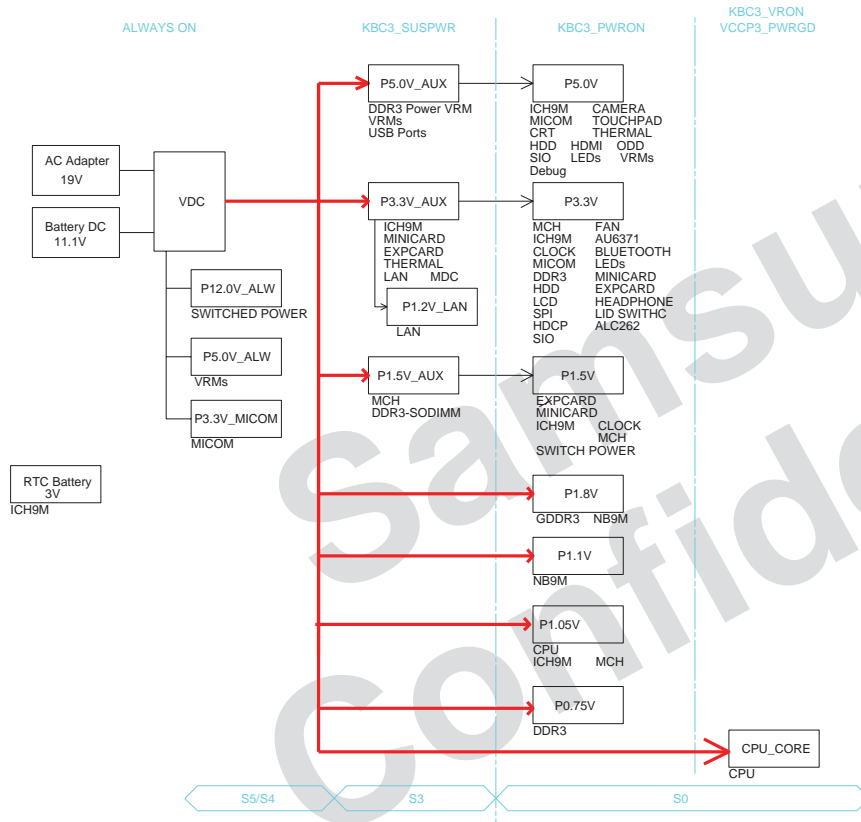
REVISION HISTORY

See rev notes for more information.

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG
CHECK	WU SHUIJIANG,	DEV. STEP	PV			ELECTRONICS
APPROVAL	BYEONGCHANG LEE,	REV	1.0	BOARD INFO	PART NO.	BA41-####A
DESIGN		DATE				
				May 08, 2008 19:01:59 PM	PAGE	3 OF 23

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POWER DIAGRAM

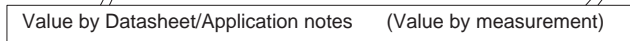


Rail	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	OFF	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG ELECTRONICS
CHECK	WU SHUJIANG,	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0		POWER DIAGRAM	
DESIGNED		DATE	May 08, 2008 19:01:59 PM	PAGE	4	OF 23

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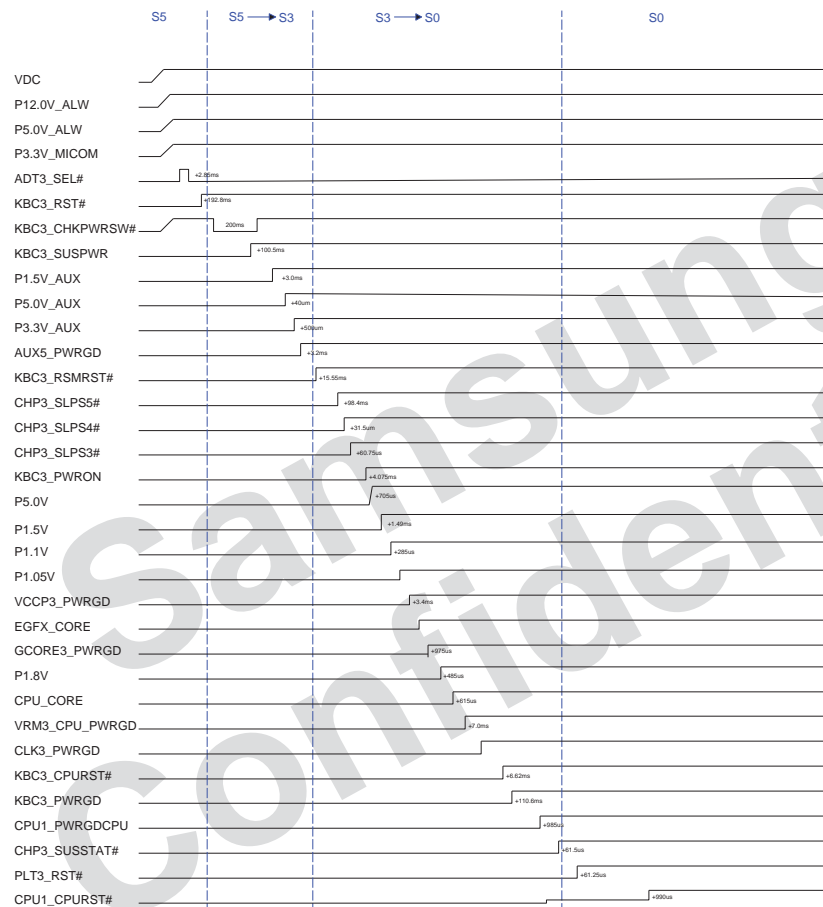
This sheet should be updated !!!



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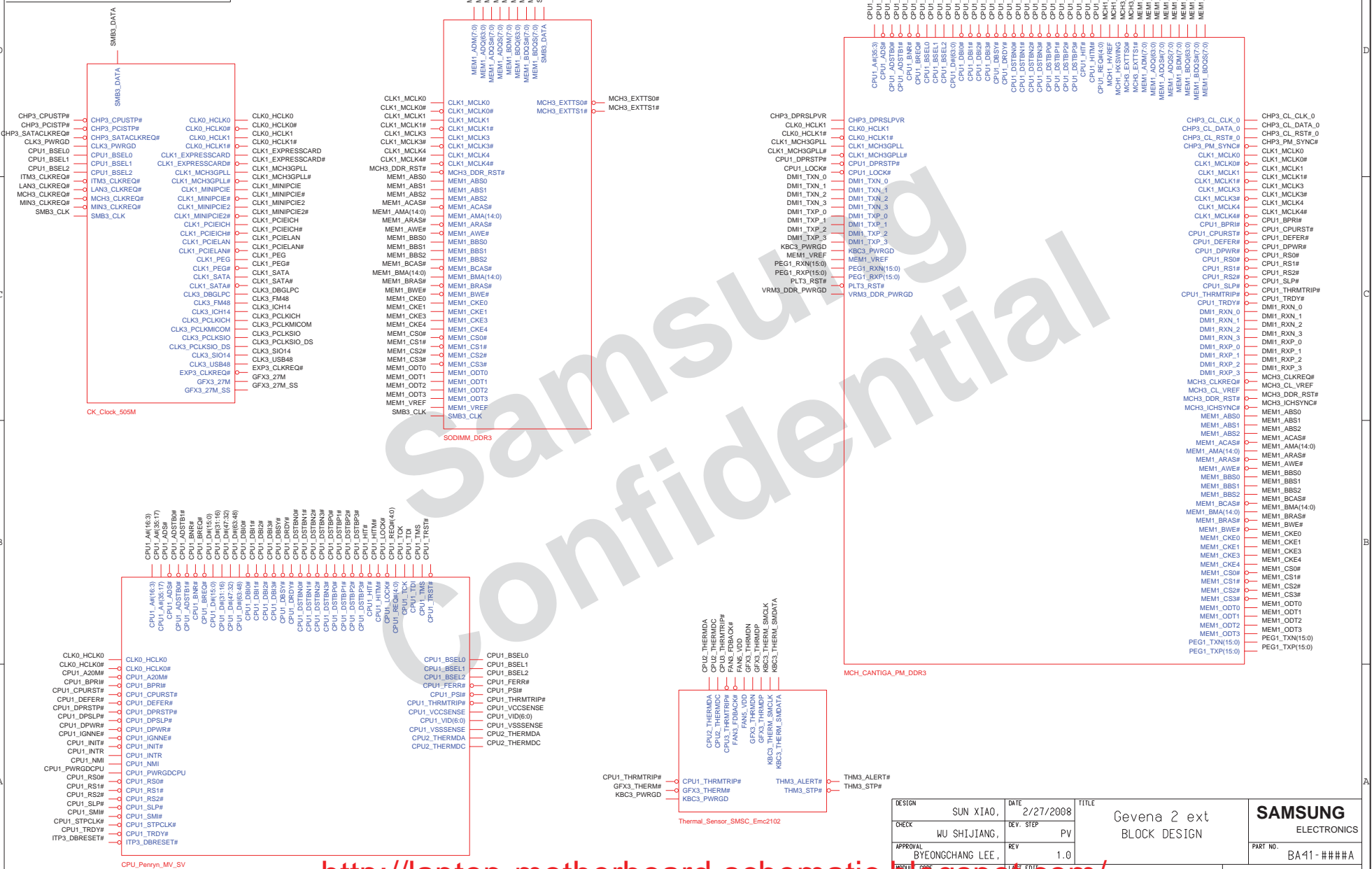
Timing Diagram, Power ON Rev. 1.0 2008-05--5



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG
CHECK	WU SHUJIANG,	DEV. STEP	PV			ELECTRONICS
APPROVAL	BYEONGCHANG LEE,	REV	1.0	CLOCK DIAGRAM	PART NO.	BA41-####A
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DESIGN	SUN XIAO,	DATE	2/27/2008	TITLE	Gena 2 ext BLOCK DESIGN	SAMSUNG ELECTRONICS PART NO. BA11-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
DATE	08, 2008 19:01:59 PM	PAGE	8	OF	23	

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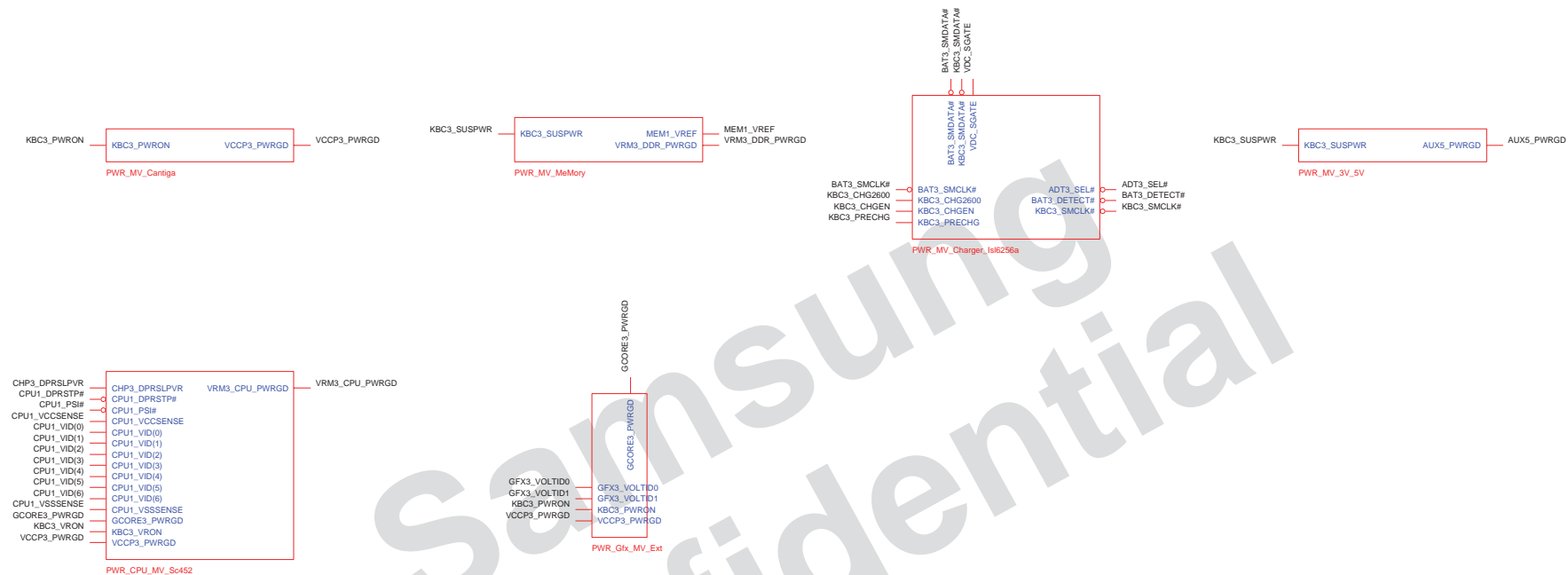
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COM-22C-015(1996.6.5) REV. 3

[illegible]

DRAW	SUN XIAO,	DATE	2/27/2008	Gevena 2 ext Block Design	SAMSUNG ELECTRONICS
CHECK	WU SHUIJANG,	DEV. STEP	PV		
APPROVAL	BYEONGCHANG LEE,	REV.	1.0		
PART NO.				BA41-####A	
MAY 08, 2008 19:01:59 PM				PAGE	11 OF 23

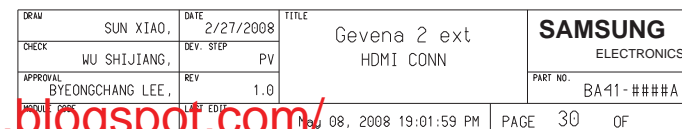
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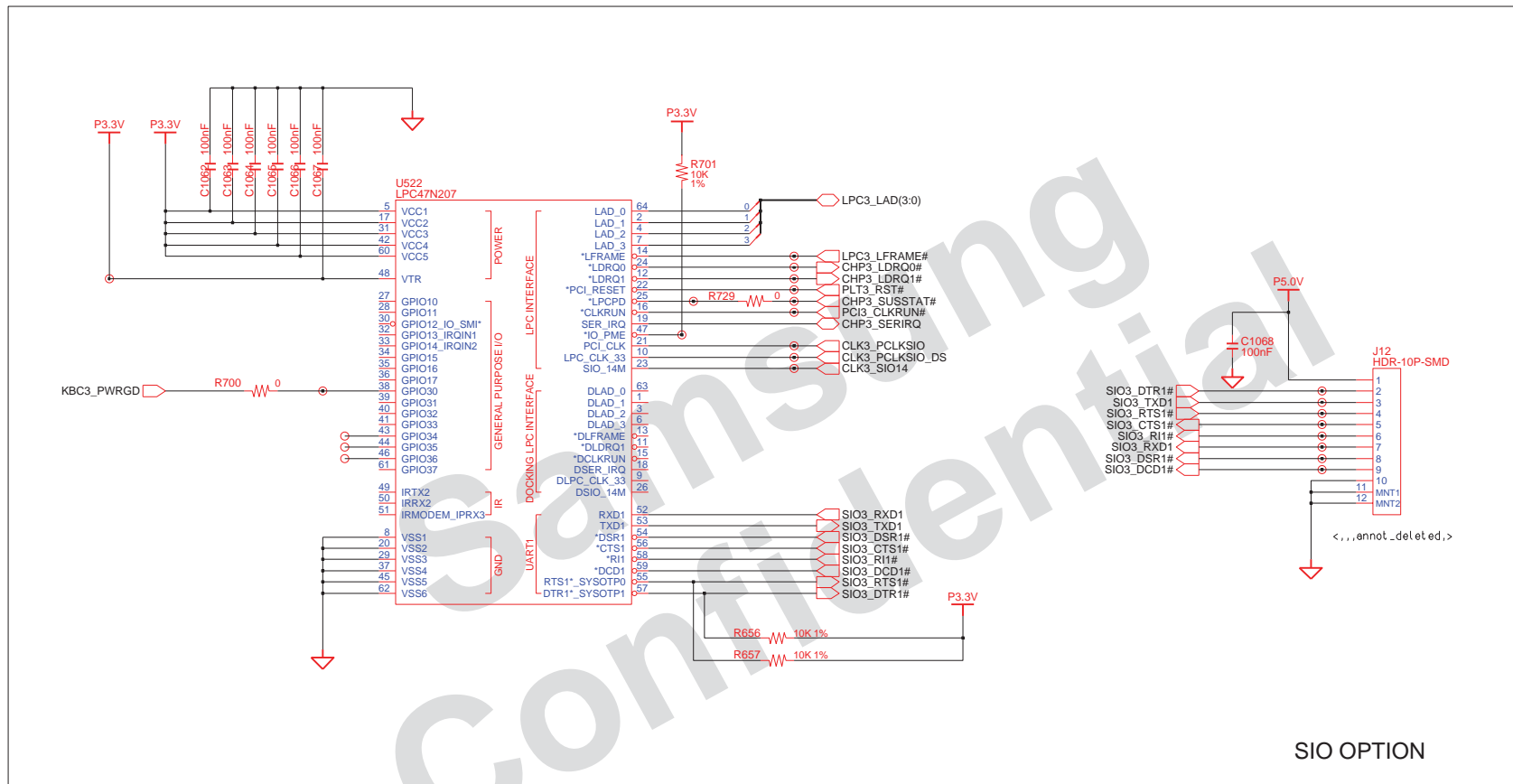
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CHECK	WU SHIJIANG,	DEV. STEP	PV	Block Design	Power Block	ELECTRONICS
APPROVAL	BYEONGCHANG LEE,	REV	1.0			PART NO. BA41-####A
DESIGNED BY	WU SHIJIANG	DATE	May 08, 2008 19:01:59 PM	PAGE	12	OF 23

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DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext SIO CHIPSET	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
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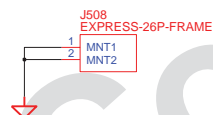
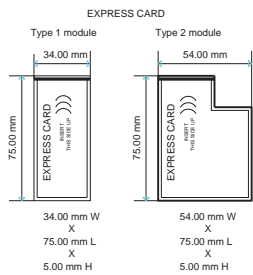
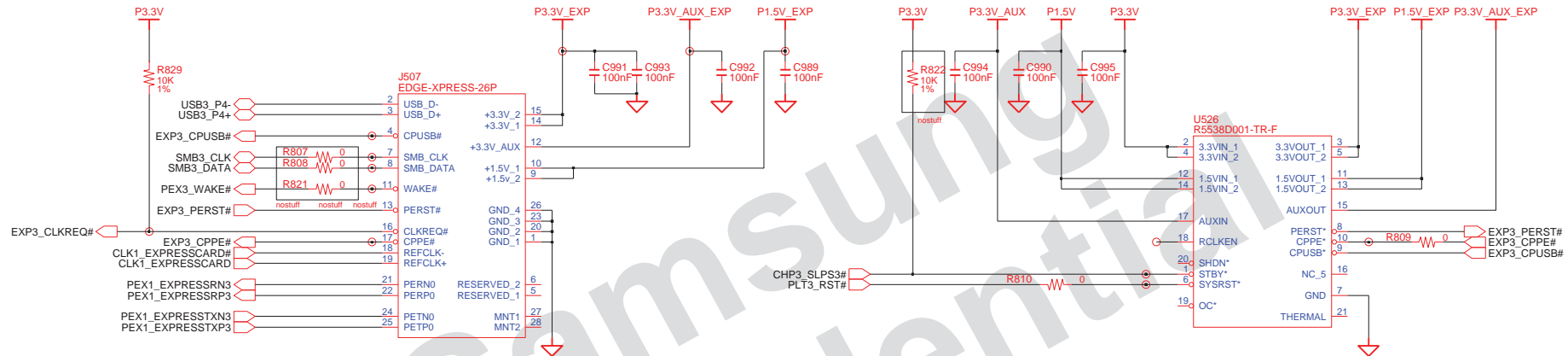
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EMI502
EMI
CONTACT-PLATE-EMI

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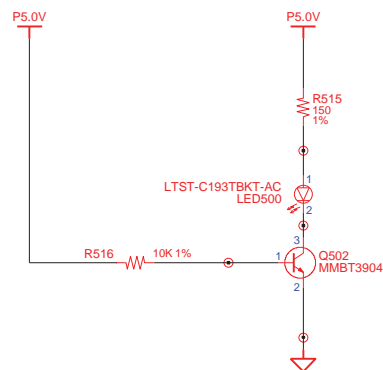


DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext MIO BOARD EXPRESS CARD	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
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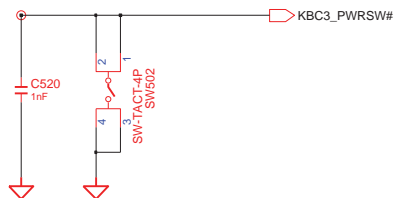
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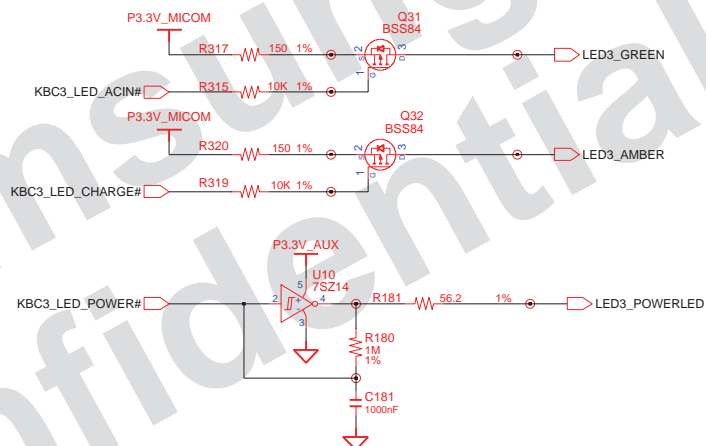
POWER ON LED



POWER ON SW BUTTON



ADAPTERIN/CHARGING LED



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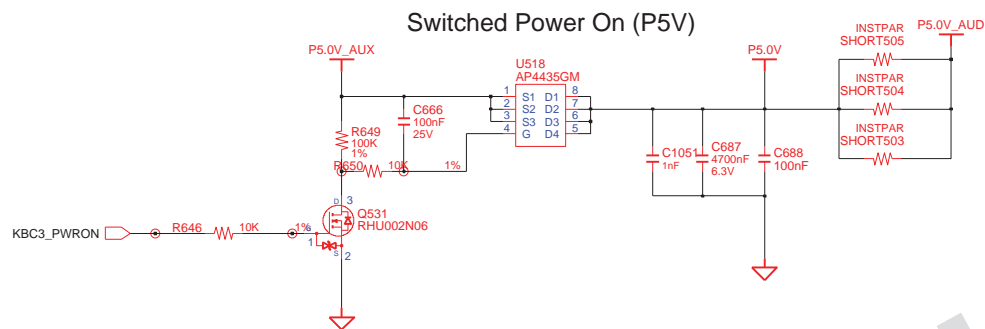
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CHECK	WU SHIJIANG,	DEV. STEP	PV		MICOM	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		MICOM LOGIC SCH	
PART NO.	BA41-###A					

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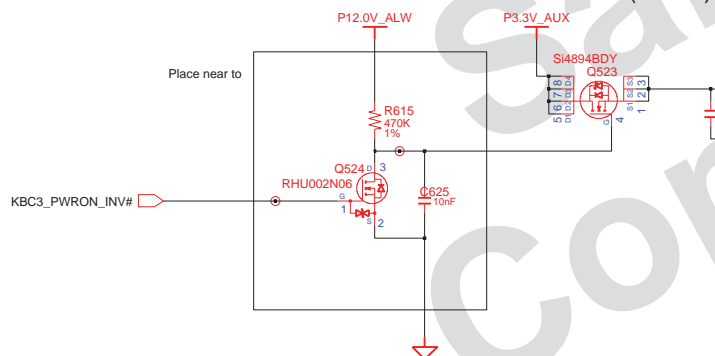
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SIGNAL SWITCH

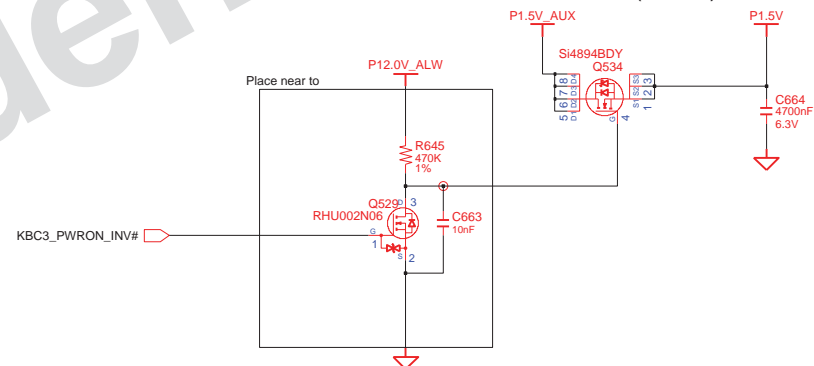
Switched Power On (P5V)



Switched Power On (P3.3V)



Switched Power On (P1.5V)

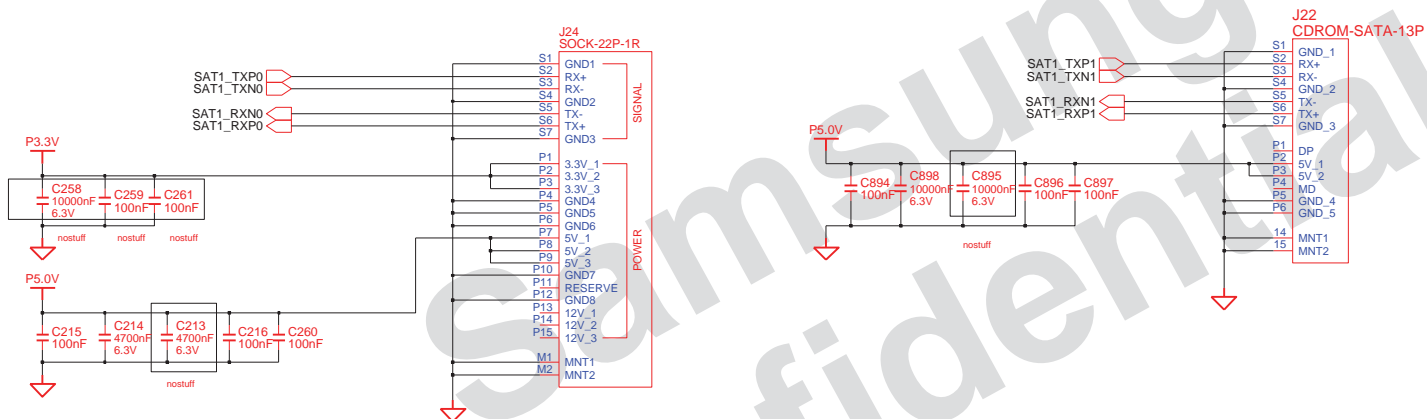


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CHECK	WU SHIJIANG,	DEV. STEP	PV		MAIN	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		SWITCH POWER P1.5V	
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Main to HDD



EMI4
EMI
CONTACT-PLATE-EMI

EMI500
EMI
CONTACT-PLATE-EMI

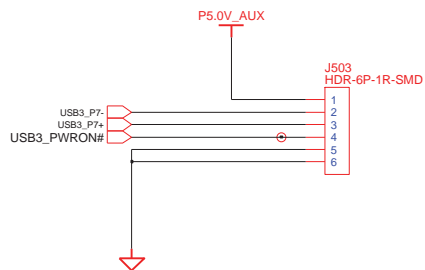
EMI501
EMI
CONTACT-PLATE-EMI

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext CONNECTOR	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0		HDD & ODD CONNECTOR	PART NO. BA41-####A
DESIGN	COM-22C-015(1996.6.5) REV. 3	DATE	May 08, 2008 19:01:59 PM	PAGE	19	OF 23

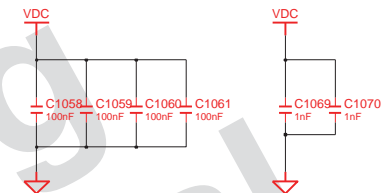
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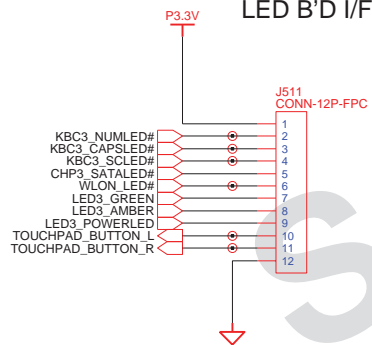
USB I/F B'D



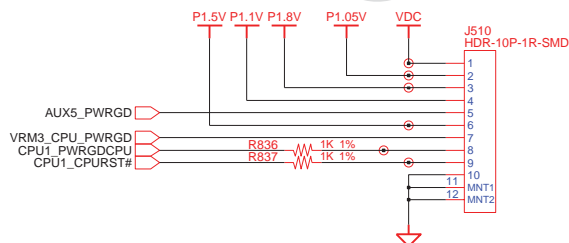
EMC ADD decap CAP



LED B'D I/F



ICT PORT

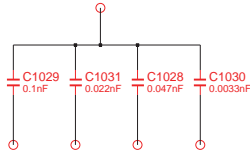


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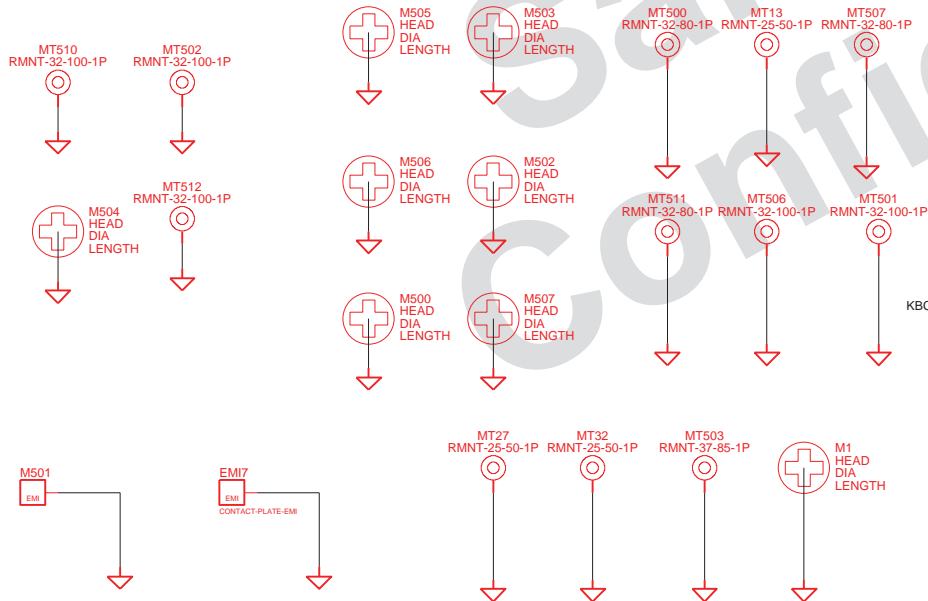
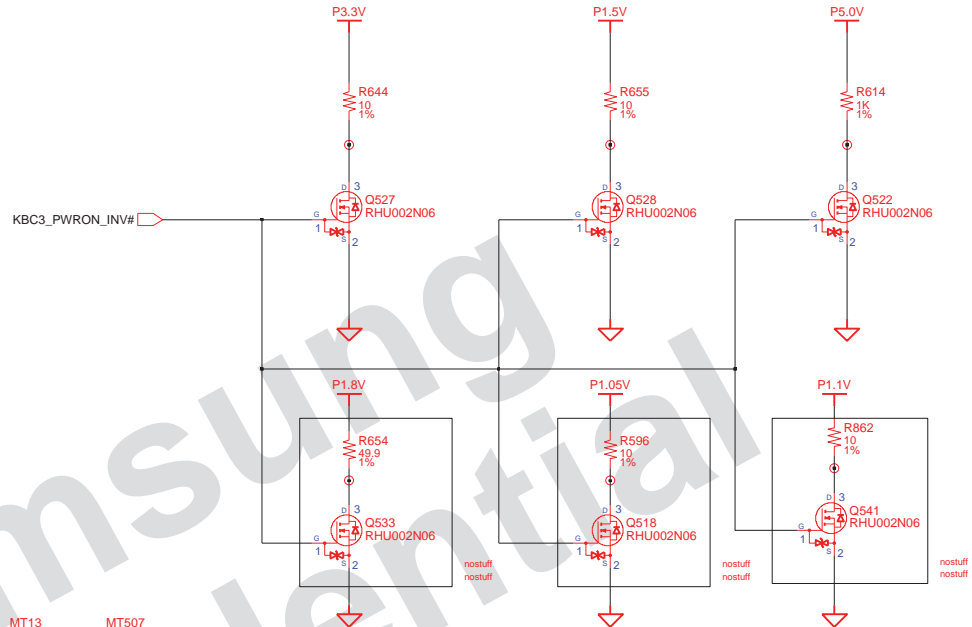
DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG
CHECK	WU SHIJIAN,	DEV. STEP	PV	KEYBOARD 80PORT ICT PORT		ELECTRONICS
APPROVAL	BYEONGCHANG LEE,	REV	1.0	LID SWITCH LED B'D USB I/O B'D	PART NO.	BA41-####A
DATE	May 08, 2008 19:01:59 PM	PAGE	20	OF	23	

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TOP SIDE



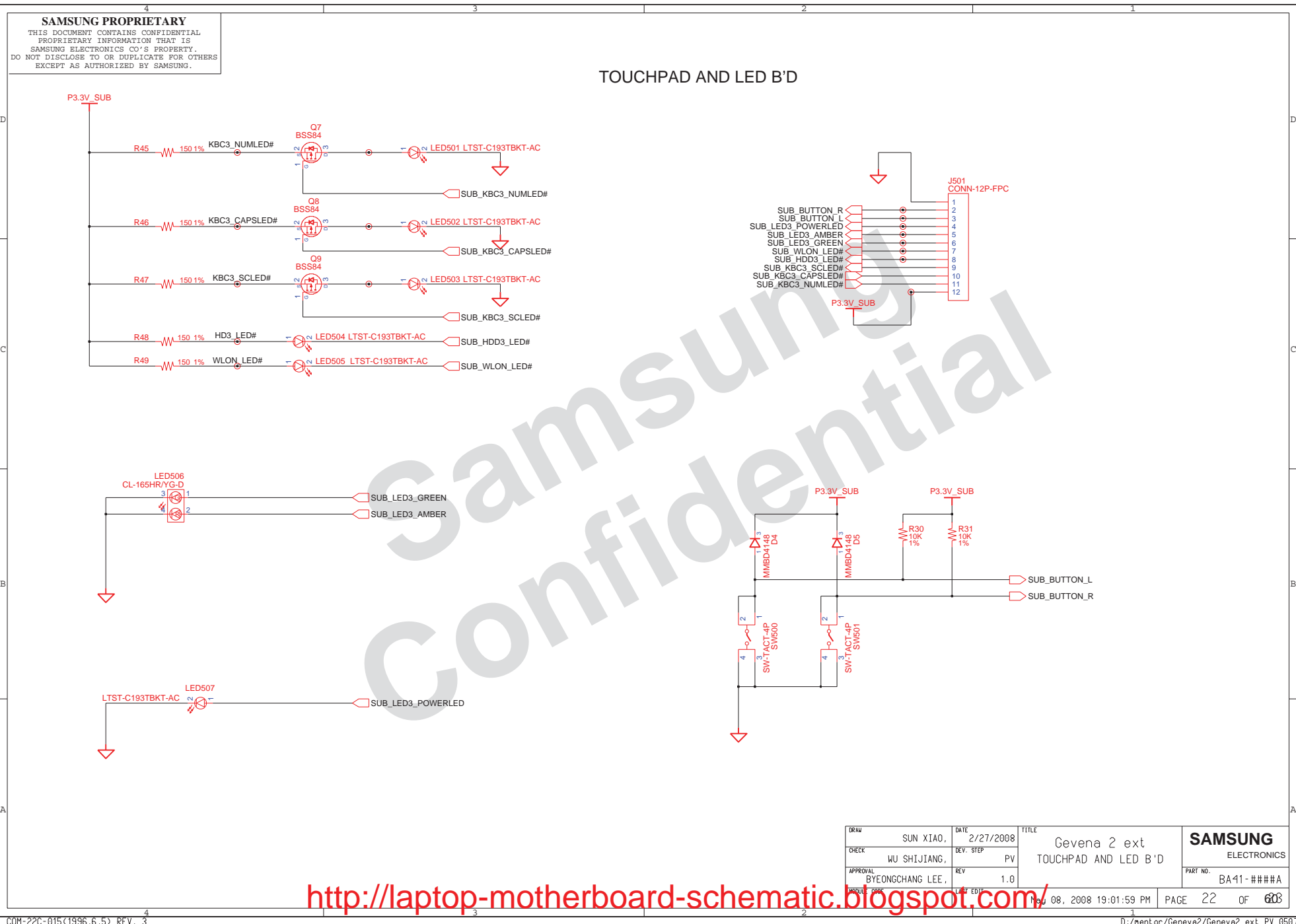
BOTTOM SIDE



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext OTHERS	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
DESIGNER	CHANG LEE,	LAST EDIT				

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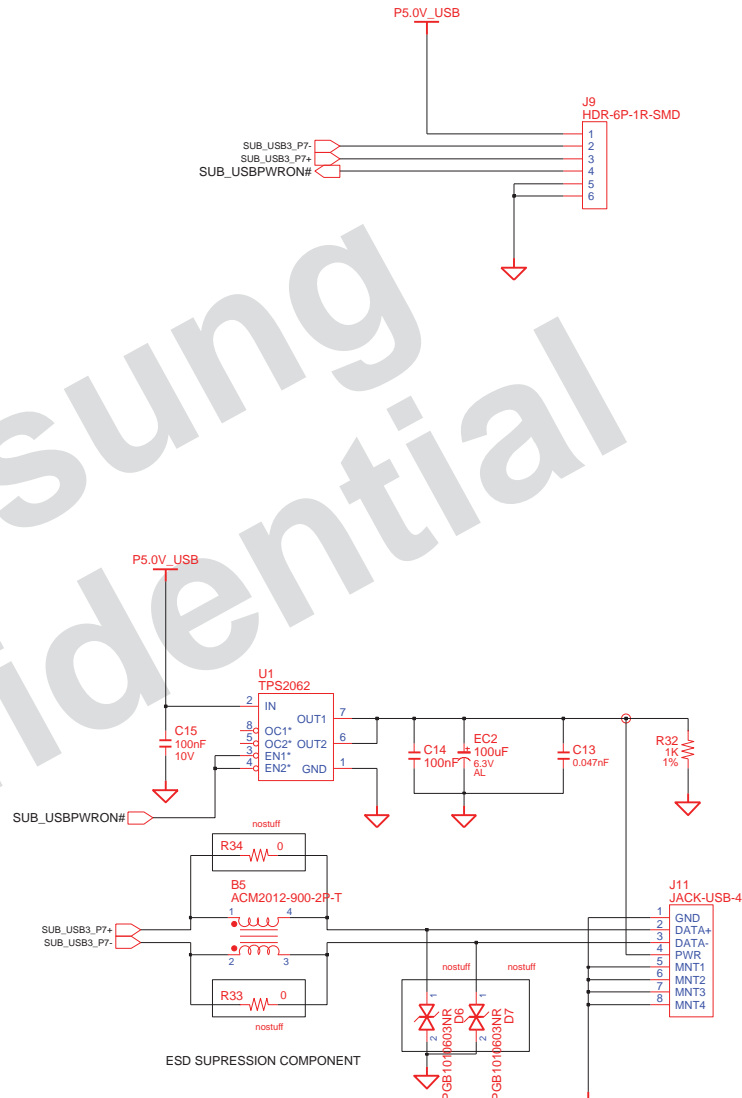
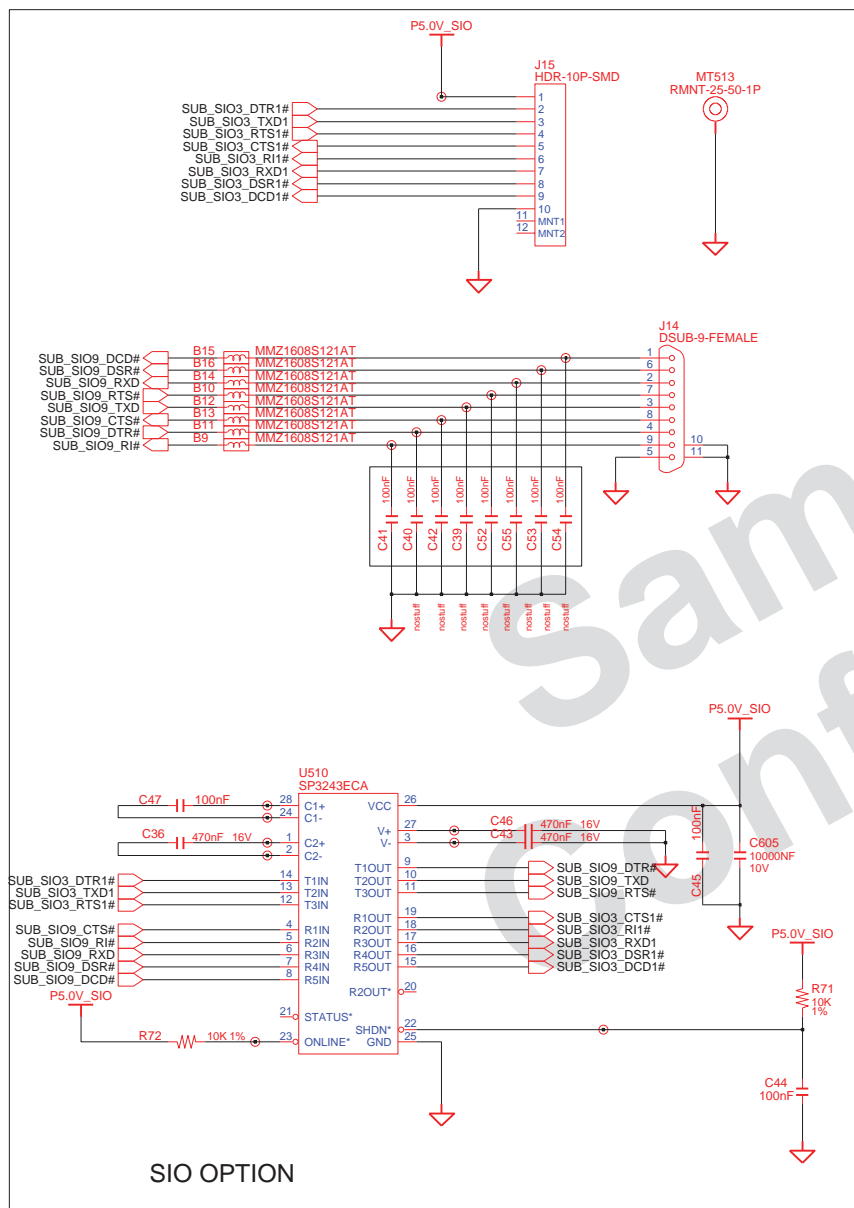
<http://laptop-motherboard-schematic.blogspot.com/>

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext TOUCHPAD AND LED B'D	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
DESIGN		DATE	08/08/2008 19:01:59 PM	PAGE	22 OF 60	

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SIO AND USB SUB B'D



DRAW	SUN XIAO	DATE	2/27/2008	TITLE	Geneva 2 ext MIO BOARD	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE	REV	1.0			
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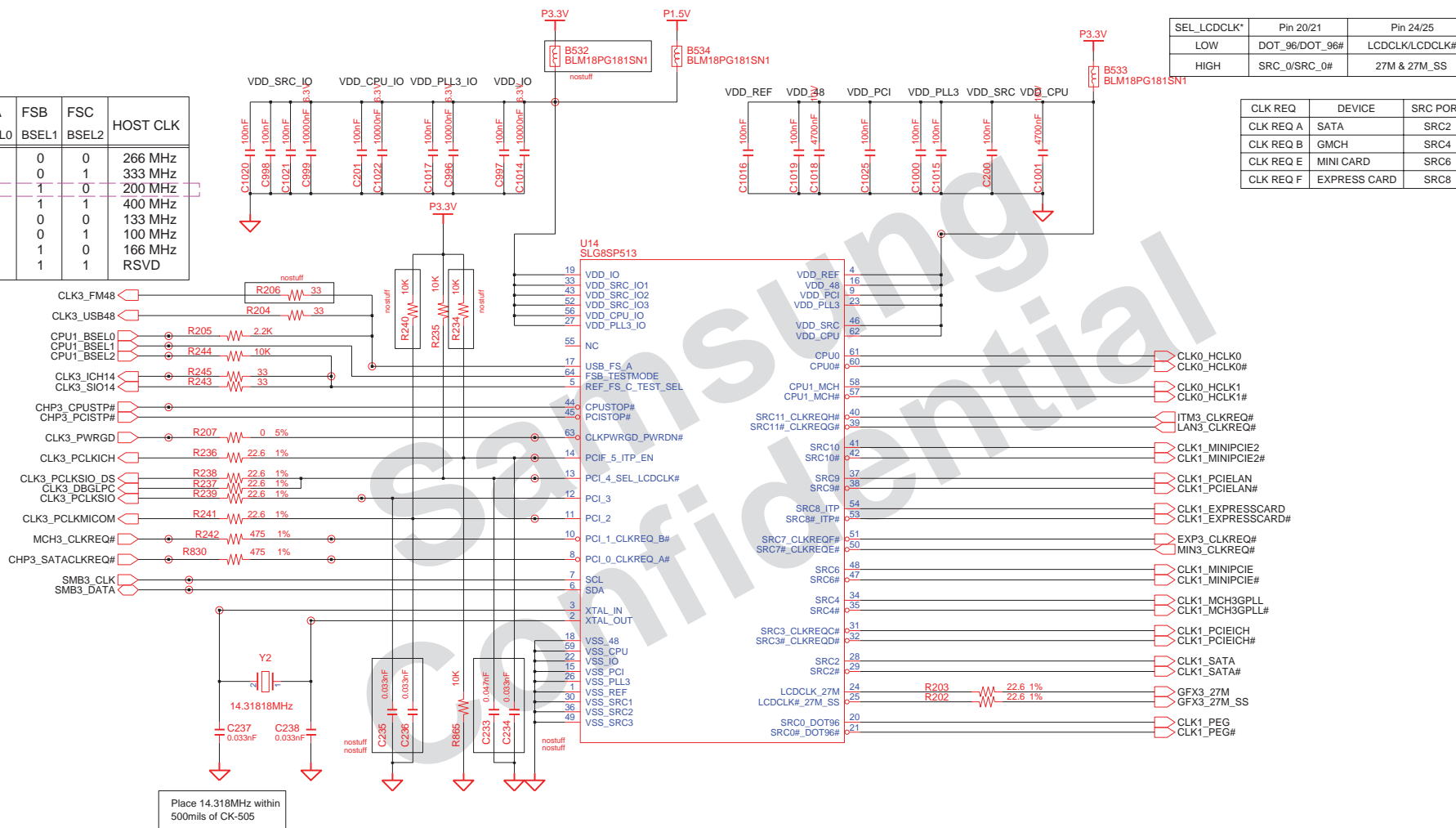
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FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

SEL_LCDCCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	LCDCCLK/LCDCCLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXPRESS CARD	SRC8



Place 14.318MHz within
 500mils of CK-505

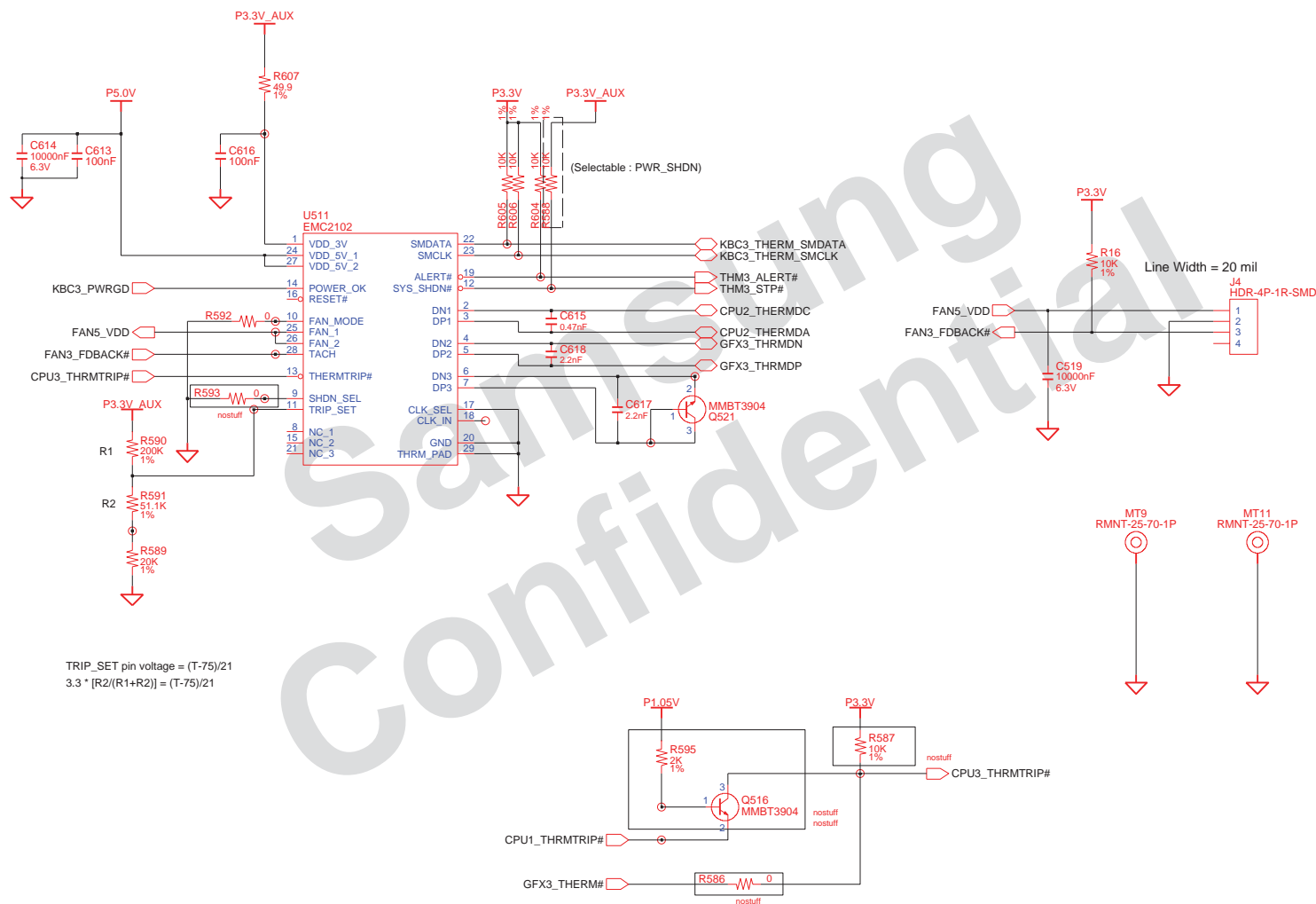
DRAW	SUN XIAO,	DATE	2/27/2007	TITLE	Gevena 2 ext Main_Clock_Circuit CK_Clock_505M	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
DESIGNED	UNSEI YAMADA	DATE	08/08/2008	TIME	19:01:59 PM	PAGE 1 OF 1

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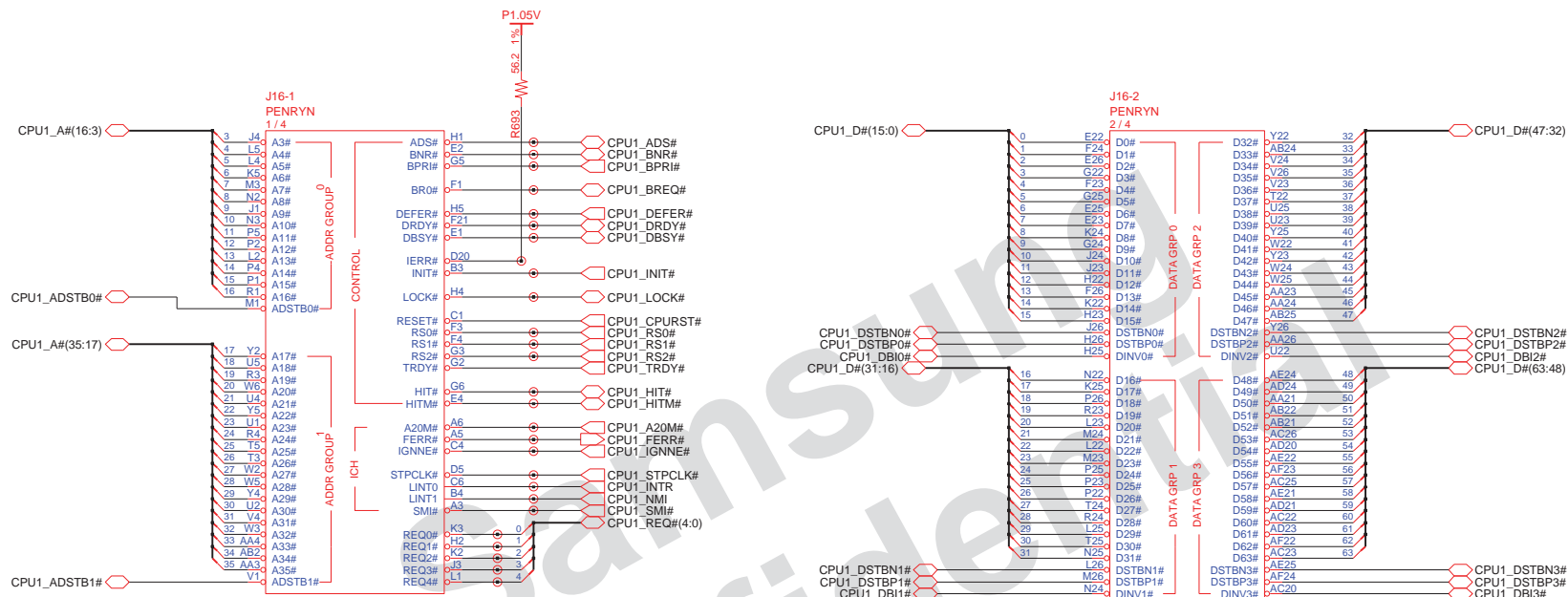
THERMAL SENSOR & FAN CONTROL



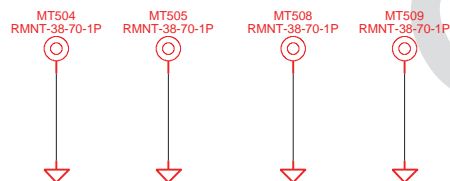
DESIGN	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP		PVTHERMAL_SENSOR_SMSC-EMC2102		
APPROVAL	BYEONGCHANG LEE,	REV	1.0	THERMAL_SENSOR_SMSC-EMC2102	PART NO.	
DESIGNER		DATE	Nov 08, 2008 19:01:59 PM	PAGE	1 OF 1	

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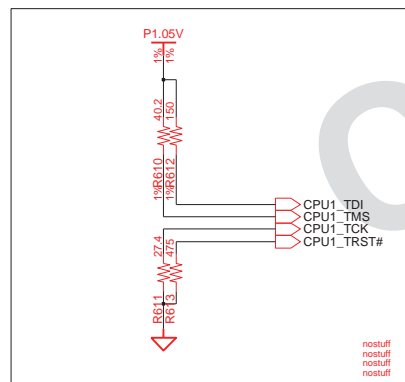


CPU CONNECTOR P/N 3704-001153



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext CPU	SAMSUNG ELECTRONICS PART NO. BA11-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
DATE	2008.08.08	TIME	19:01:59 PM	PAGE	1 OF 3	

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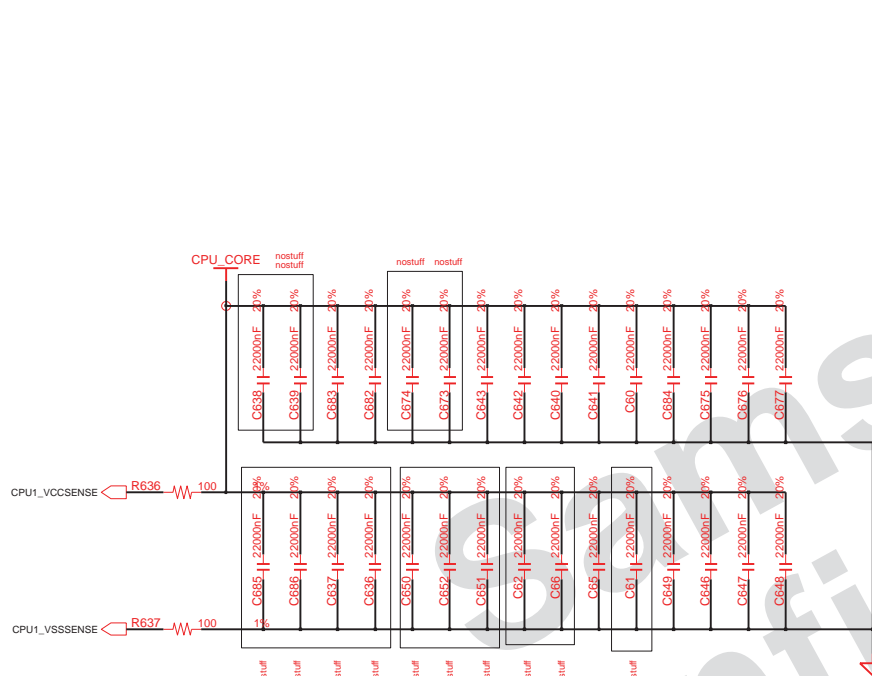
Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(E0)	Voltage	VID(E0)	Voltage	VID(E0)	Voltage
0 0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0 0	1.0000 V	1 0 1 0 0 0 0 1	0.4875 V
0 0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 0 1	0.9875 V	1 0 1 0 0 0 1 0	0.4625 V
0 0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 0 1 0	0.9750 V	1 0 1 0 0 0 1 1	0.4625 V
0 0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 0 1 1	0.9625 V	1 0 1 0 1 0 0 0	0.4500 V
0 0 0 0 0 0 1 0	1.4500 V	0 1 0 1 0 1 1 0	0.9500 V	1 0 1 0 1 0 1 0	0.4375 V
0 0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 0 1	0.9375 V	1 0 1 0 1 0 1 1	0.4250 V
0 0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 0 1 0	0.9250 V	1 0 1 0 1 0 1 1	0.4125 V
0 0 0 0 0 1 1 1	1.4125 V	0 1 0 1 0 1 1 1	0.9125 V	1 0 1 1 0 0 0 0	0.4000 V
0 0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0 0	0.9000 V	1 0 1 1 0 0 0 1	0.3875 V
0 0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 0 1	0.8875 V	1 0 1 1 0 0 1 0	0.3750 V
0 0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 0 1 0	0.8750 V	1 0 1 1 0 0 1 1	0.3625 V
0 0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 0 1 1	0.8625 V	1 0 1 1 0 1 0 0	0.3500 V
0 0 0 0 1 1 0 0	1.3500 V	0 1 1 0 0 1 0 0	0.8500 V	1 0 1 1 0 1 0 1	0.3375 V
0 0 0 0 1 1 0 1	1.3375 V	0 1 1 0 0 1 0 1	0.8375 V	1 0 1 1 0 1 1 0	0.3250 V
0 0 0 0 1 1 1 0	1.3250 V	0 1 1 0 0 1 1 0	0.8250 V	1 0 1 1 0 1 1 1	0.3125 V
0 0 0 0 1 1 1 1	1.3125 V	0 1 1 0 0 1 1 1	0.8125 V	1 1 0 0 0 0 0 0	0.3000 V
0 0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0 0	0.8000 V	1 1 0 0 0 0 0 1	0.2875 V
0 0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 0 1	0.7875 V	1 1 0 0 0 0 1 0	0.2750 V
0 0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 0 1 0	0.7750 V	1 1 0 0 0 0 1 1	0.2625 V
0 0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 0 1 1	0.7625 V	1 1 0 0 0 1 0 0	0.2500 V
0 0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0 0	0.7500 V	1 1 0 0 0 1 0 1	0.2375 V
0 0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 0 1	0.7375 V	1 1 0 0 0 1 1 0	0.2250 V
0 0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 0 1 0	0.7250 V	1 1 0 0 0 1 1 1	0.2125 V
0 0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 0 1 1	0.7125 V	1 1 0 0 0 1 1 1	0.2000 V
0 0 0 1 0 1 2000	1.2000 V	1 0 0 0 0 0 0 0	0.7000 V	1 1 0 0 0 1 1 1	0.1875 V
0 0 0 1 1 0 0 0	1.1875 V	1 0 0 0 0 0 0 1	0.6875 V	1 1 0 0 1 0 1 0	0.1750 V
0 0 0 1 1 0 0 1	1.1750 V	1 0 0 0 0 0 1 0	0.6750 V	1 1 0 0 1 0 1 1	0.1625 V
0 0 0 1 1 0 1 0	1.1625 V	1 0 0 0 0 0 1 1	0.6625 V	1 1 0 0 1 1 0 0	0.1500 V
0 0 0 1 1 0 1 1	1.1500 V	1 0 0 0 0 1 0 0	0.6500 V	1 1 0 0 1 1 0 1	0.1375 V
0 0 0 1 1 1 0 0	1.1375 V	1 0 0 0 0 1 0 1	0.6375 V	1 1 0 0 1 1 0 1	0.1250 V
0 0 0 1 1 1 0 1	1.1250 V	1 0 0 0 0 1 1 0	0.6250 V	1 1 0 0 1 1 1 0	0.1125 V
0 0 0 1 1 1 1 0	1.1125 V	1 0 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0 0	0.1000 V
0 0 0 1 0 0 0 0	1.1000 V	1 0 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 0 1	0.0875 V
0 0 0 1 0 0 0 1	1.0875 V	1 0 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 0 1 0	0.0750 V
0 0 0 1 0 0 1 0	1.0750 V	1 0 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 0 1 1	0.0625 V
0 0 1 0 0 0 1 1	1.0625 V	1 0 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0 0	0.0500 V
0 0 1 0 0 1 0 0	1.0500 V	1 0 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 0 1	0.0375 V
0 0 1 0 0 1 0 1	1.0375 V	1 0 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 0 1 0	0.0250 V
0 0 1 0 0 1 1 0	1.0250 V	1 0 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1 1	0.0125 V
0 0 1 0 0 1 1 1	1.				

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with $Z_0=55\Omega$ trace. Minimize coupling of any switching signals to this net.

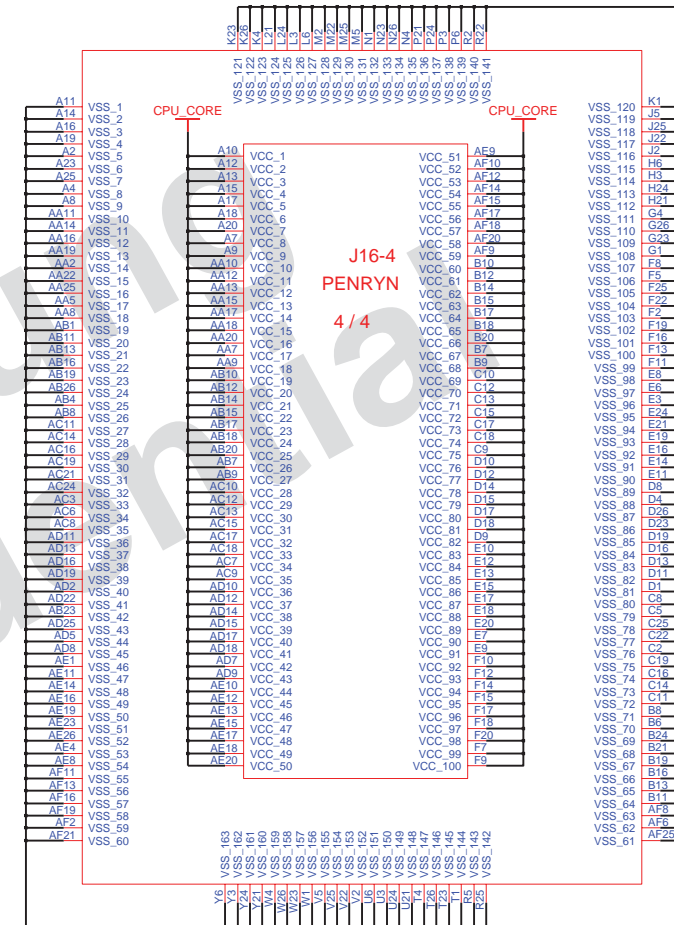
GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a $Z_0=55\text{ohm}$ traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

DRAM	SUN XIAO,	DATE	2/27/2008	TITLE Gevena 2 ext CPU PENRYN (2/3)	SAMSUNG ELECTRONICS PART NO. BA11-####
CHECK	WU SHIJIANG,	DEV. STEP	PV		
APPROVAL	BYEONGCHANG LEE,	REV	1.0		
PRODUCT CODE	UNIVERSAL	LAST EDIT	Nov. 08, 2008 19:01:59 PM		
				PAGE	2 OF 3

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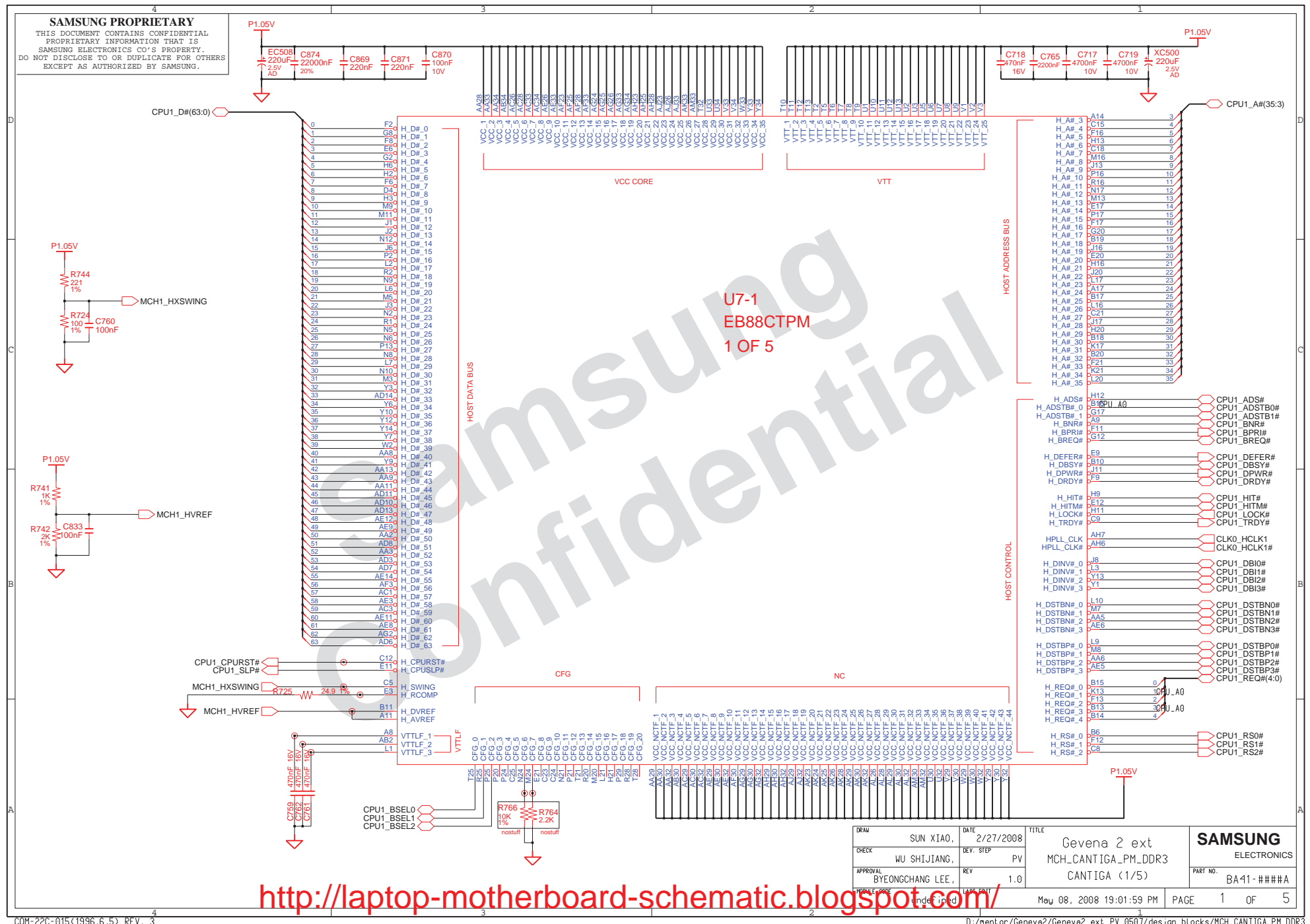
6x 330 uF : CPU VR side
Be Caution the placement of decap!!



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext CPU PENRYN (3/3)	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO.
APPROVAL	BYEONGCHANG LEE,	REV	1.0			BA41-####A
DATE	08, 2008 19:01:59 PM	PAGE	3	OF	3	

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DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV	
APPROVAL	BYEONGCHANG LEE,	REV	1.0	
DATE	2/27/2008	TIME	19:01:59 PM	

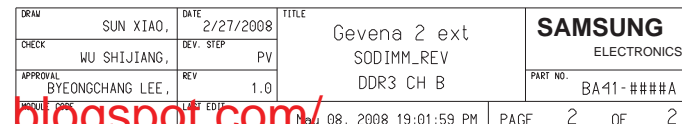


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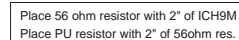


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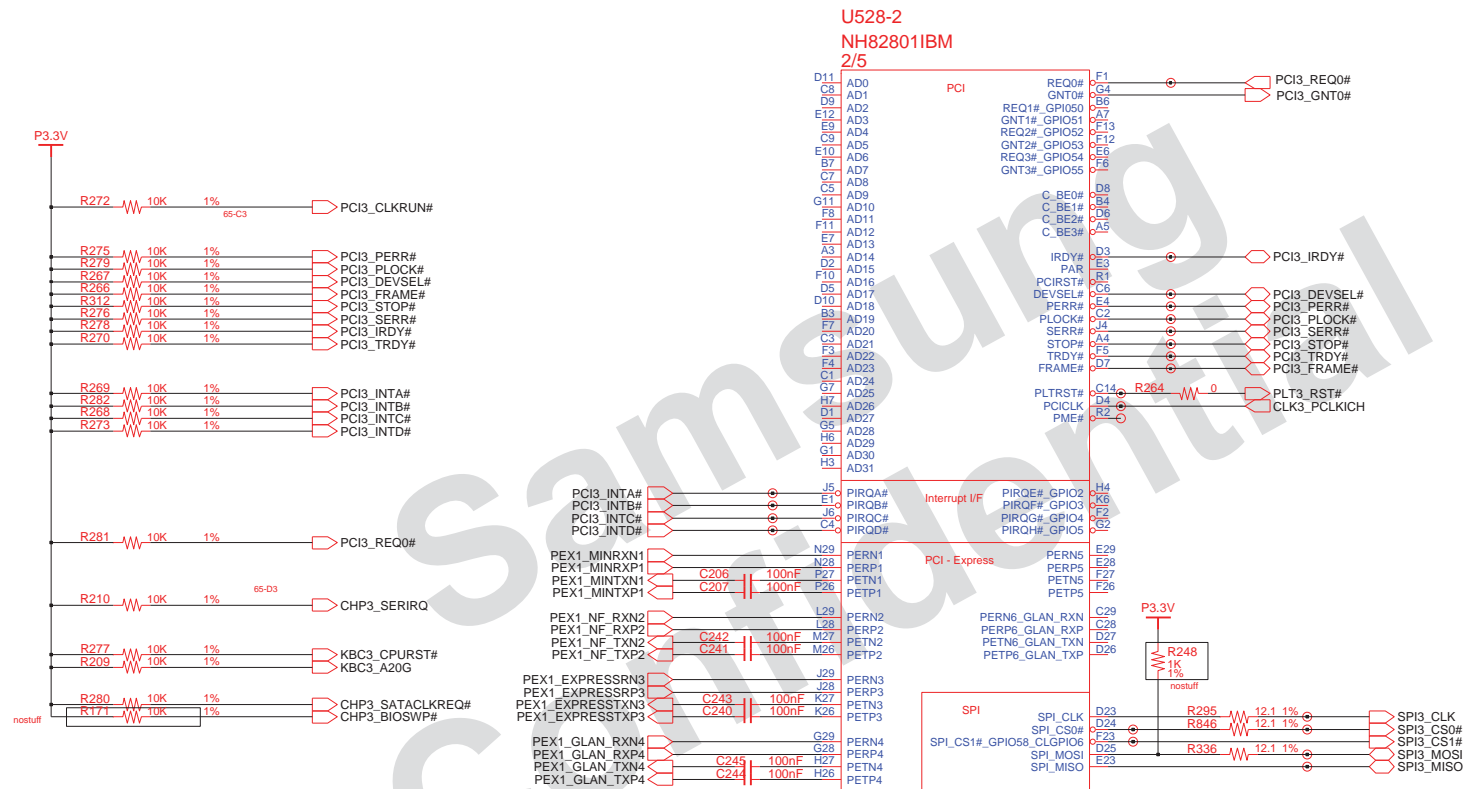


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SATA Cap. Placement :
Distance b/w the ICH8-M & cap on the "P" signal should be identical
distance b/w the ICH8-M & cap on the "N" signal same pair.

DRAM	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext ICH9_M_B ICH9-M (1/5)	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
PART NO.				BA41-####A		
PRINTED				LAST EDITED		
08. 08. 2008 19:01:59 PM				PAGE 1 OF 5		



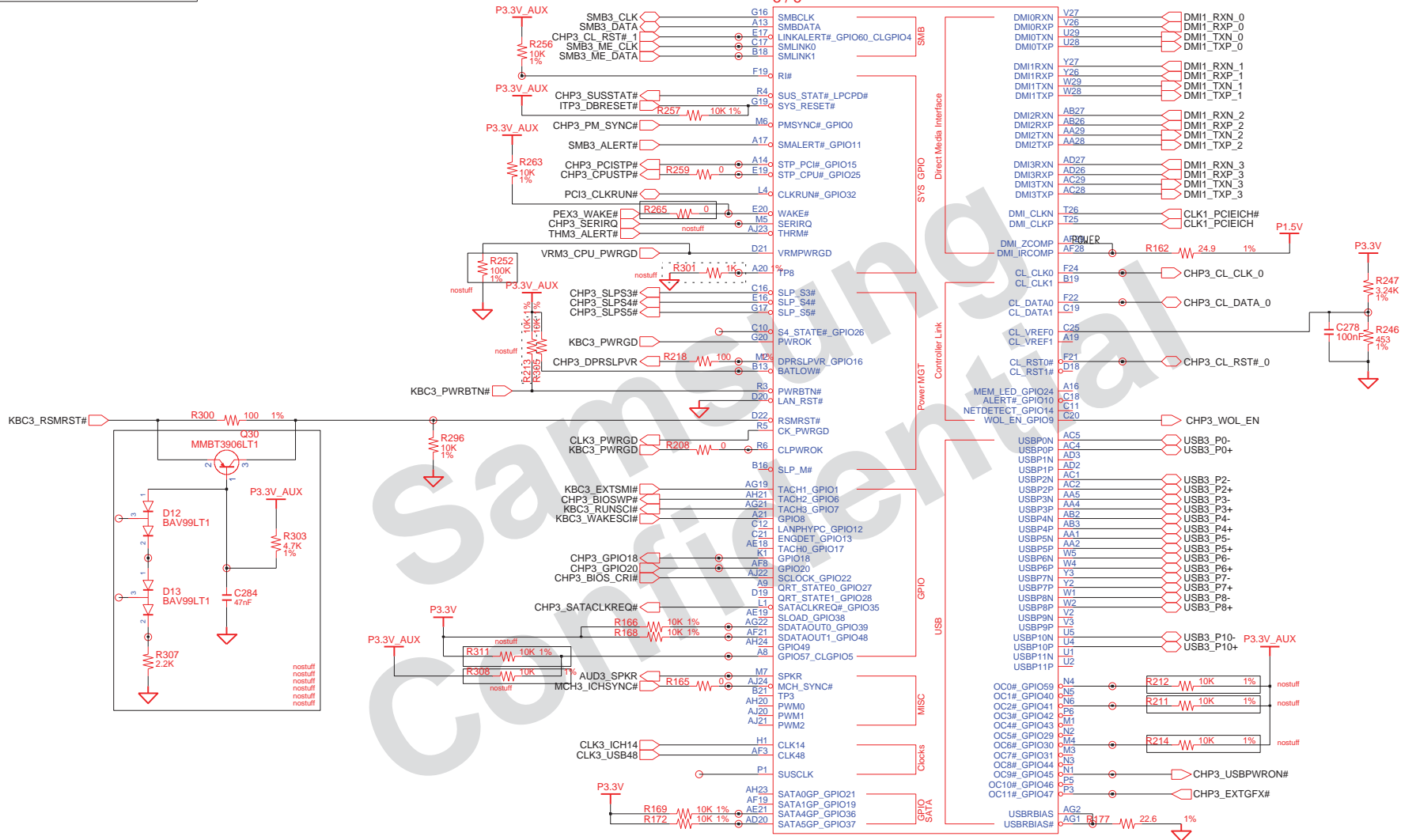
AC caps : PCIE need to be within 250mils of the driver
Resistor for Test : Place Stuffed Option to minimize stubs

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV		ICH9M_B	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		ICH9-M (2/5)	
PART NO.	BA41-####A					
DATE	Nov 08, 2008 19:01:59 PM					
PAGE	2					OF 5

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U528-3
NH82801IBM
3 / 5



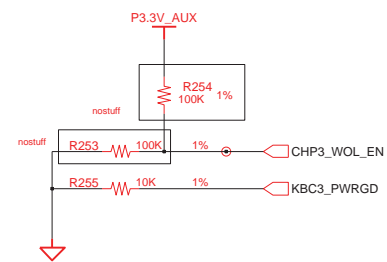
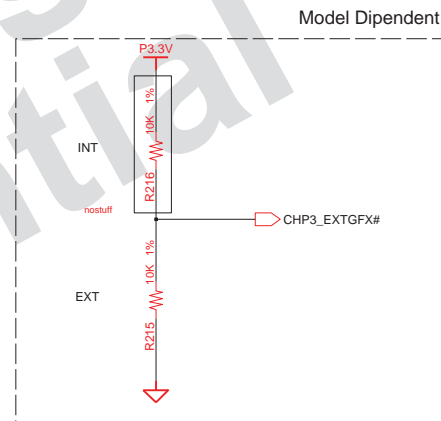
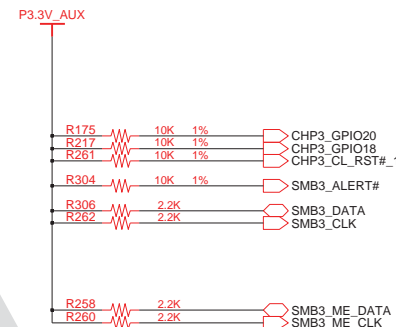
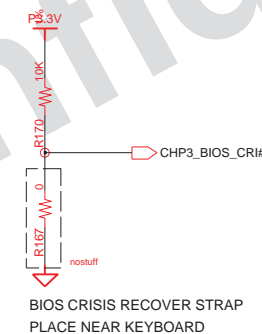
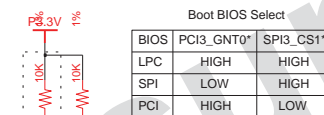
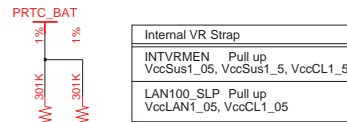
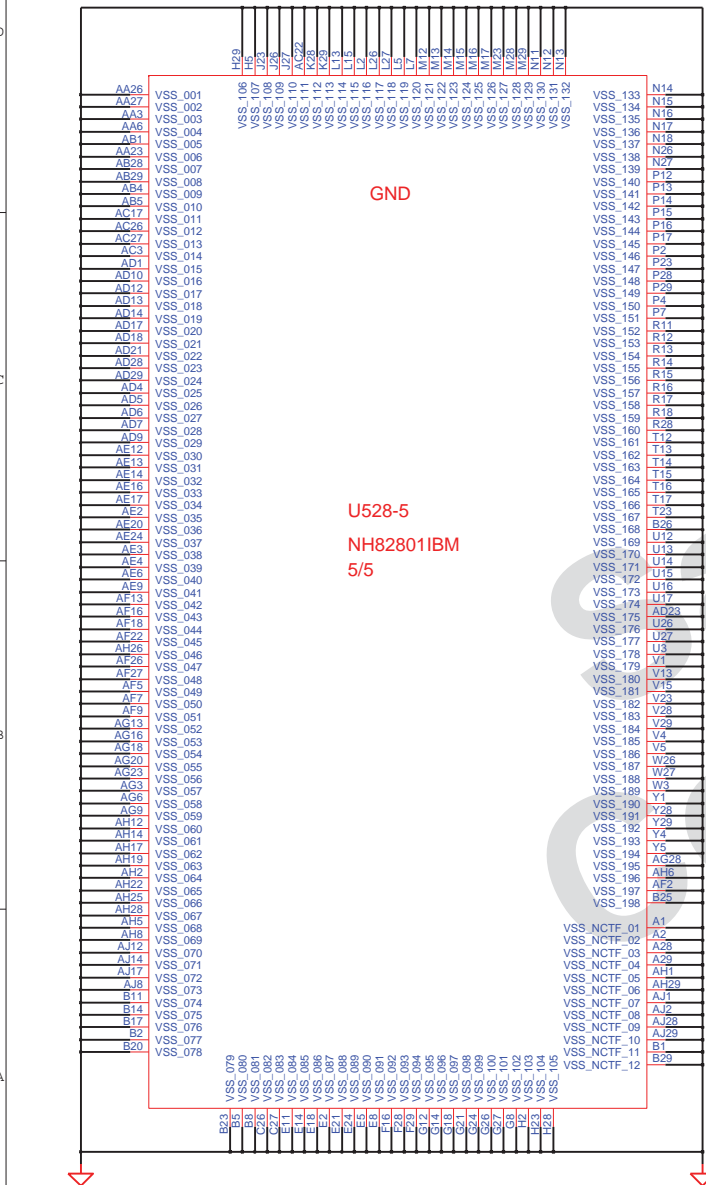
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CHECK	WU SHIJIANG,	DEV. STEP	PV		ICH-9M_B	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		ICH9-M (3/5)	
DESIGN	BYEONGCHANG LEE,	DATE	2/27/2008			

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DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		ICH9M_B	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		ICH9-M (5/5)	
INQUIRY CODE		LAST EDIT				
Nov 08, 2008 19:01:59 PM						PAGE 5 OF 5

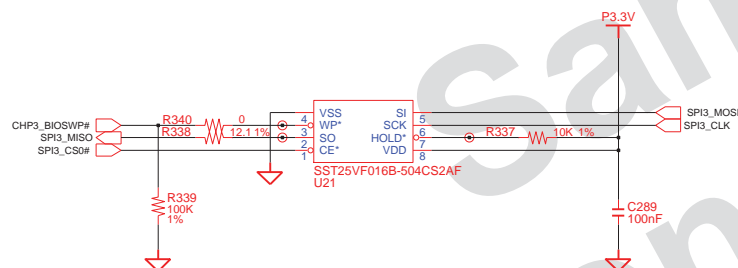
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- SPI ROM LIST -

- Macronix - MX25L8005M2C-15G
 - STM - M25PE80
 - ATMEL - AT26DF081A-SU
- SST - 25VF080B-50-4C-S2AF
WINBOND - W25X80-VSSI-G



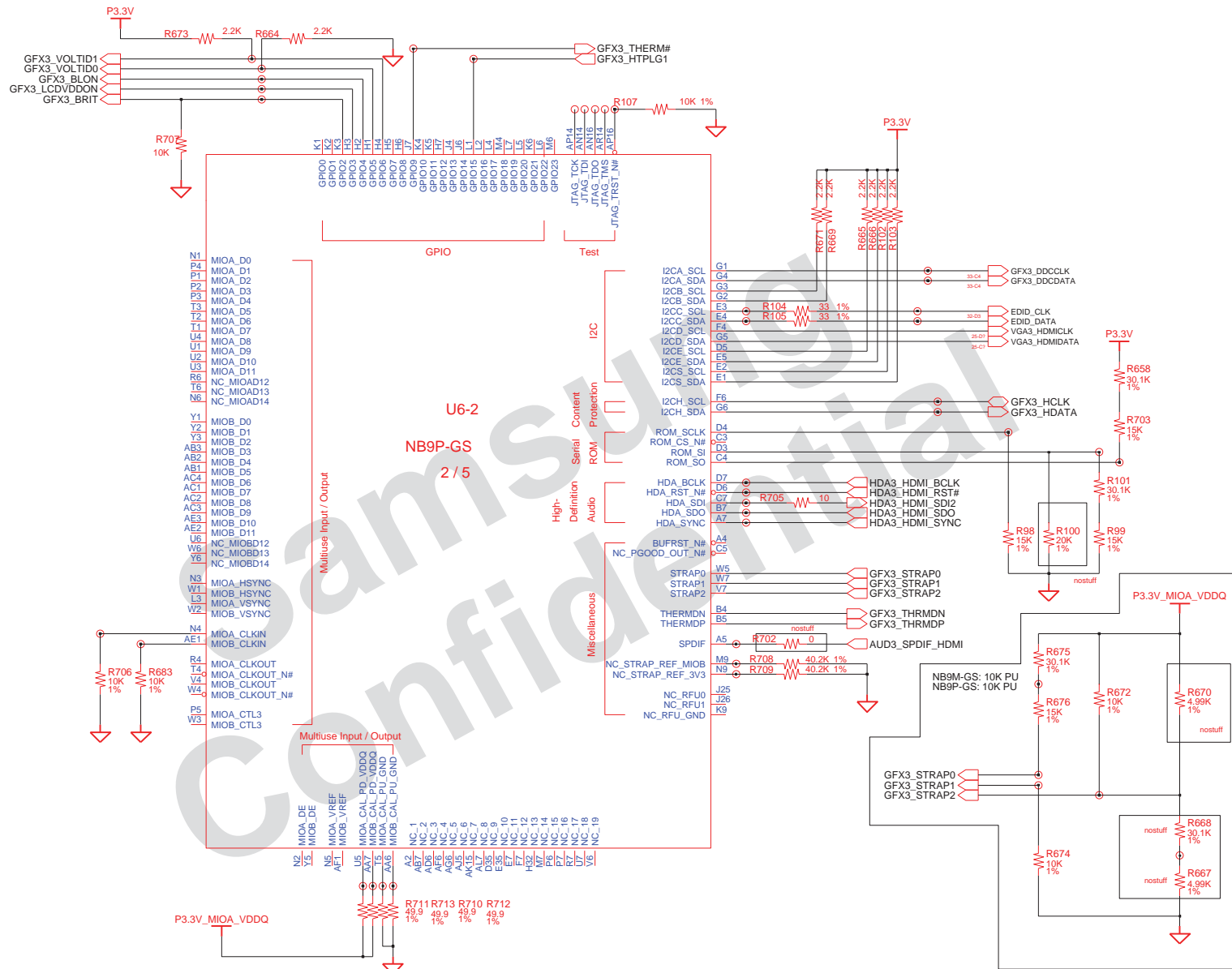
02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE	86	RE-INIT. ON-BOARD I/O PORT
14	INIT. KEYBOARD CONTROLLER	88	INIT. BIOS DATA ROM
16	CHECK CHECKSUM	8A	INIT.EXTENDED BIOS DATA AREA
18	8254 TIMER INIT.	8C	INIT. FDD CONTROLLER
1A	8237 DMA CONTROLLER INIT.	9A	SHADOW OPTION ROMS
1C	RESET INTERRUPT CONTROLLER	9C	SETUP POWER MANAGEMENT
20	TEST DRAM REFRESH	9E	ENABLE H/W INTERRUPT
22	TEST 8742 KEYBOARD CONTROLLER	A0	SET TIME OF DAY
24	SET ES SEGMENT REG. TO 4GB	A4	INIT. TYPEMATIC RATE
26	ENABLE A20	A8	ERASE F2 PROMPT
28	AUTO SIZING DRAM	AA	SCAN FOR F2 KEY STROKE
32	COMPUTE THE CPU SPEED	AC	ENTER SETUP
34	TESET CMOS RAM	AE	CLEAR IN POST FLAG
38	SHADOW SYSTEM BIOS ROM	B0	CHECK FOR ERRORS
3A	AUTO SIZING CACHE	B2	POST DONE-PREPARE TO BOOT O/S
3C	CONFIGURE ADVANCED CHIPSET REG.	B4	ONE BEEP
3D	LOAD ALTER REG. WITH CMOS VALUE	B6	CHECK PASSWORD (OPTION)
42	INIT. INTERRUPT VECTOR	B7	ACPI INIT
44	INIT. BIOS INTERRUPT	BA	DMI INIT
46	CHECK ROM COPYRIGHT NOTICE	BE	CLEAR SCREEN
47	INIT. I20 SUPPORT IF INSTALLED	C0	TRY BOOT WITH INT19
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D0	INTERRUPT HANDLER ERROR
49	INIT. PCI BUS AND DEVICE	D2	UNKNOWN INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D4	PENDING INTERRUPT ERROR
4C	SHADOW VIDEO BIOS ROM	D6	SHUTDOWN 5
50	DISPLAY CPU TYPE AND SPEED	D8	SHUTDOWN ERROR
52	TEST KEYBOARD	DA	EXTENDED BLOCK MOVE
54	SET KEYCLICK IF ENABLED	DC	SHUTDOWN 10
56	ENABLE KEYBOARD	89	ENABLE NMI
58	TEST FOR UNEXPECTED INTERRUPTS	90	INIT. HDD CONTROLLER
5A	DISPLAY "PRESS SETUP"	91	INIT. LOCAL BUS HDD CONTROLLER
5C	TEST RAM BETWEEN 512K AND 640K	92	JUMP TO USER PATCH 2
60	TEST EXTENDED MEMORY	94	DISABLE A20 ADDRESS LINE
62	TEST EXTENDED MEMORY ADDRESS LINE	96	CLEAR HUGE ES SEGMENT REG.
64	JUMP TO USER PATCH 1	98	SEARCH FOR OPTION ROMS

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		SPI_BIOS_ROM	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		SPI_BIOS_ROM	
DATE	08, 2008 19:01:59 PM					

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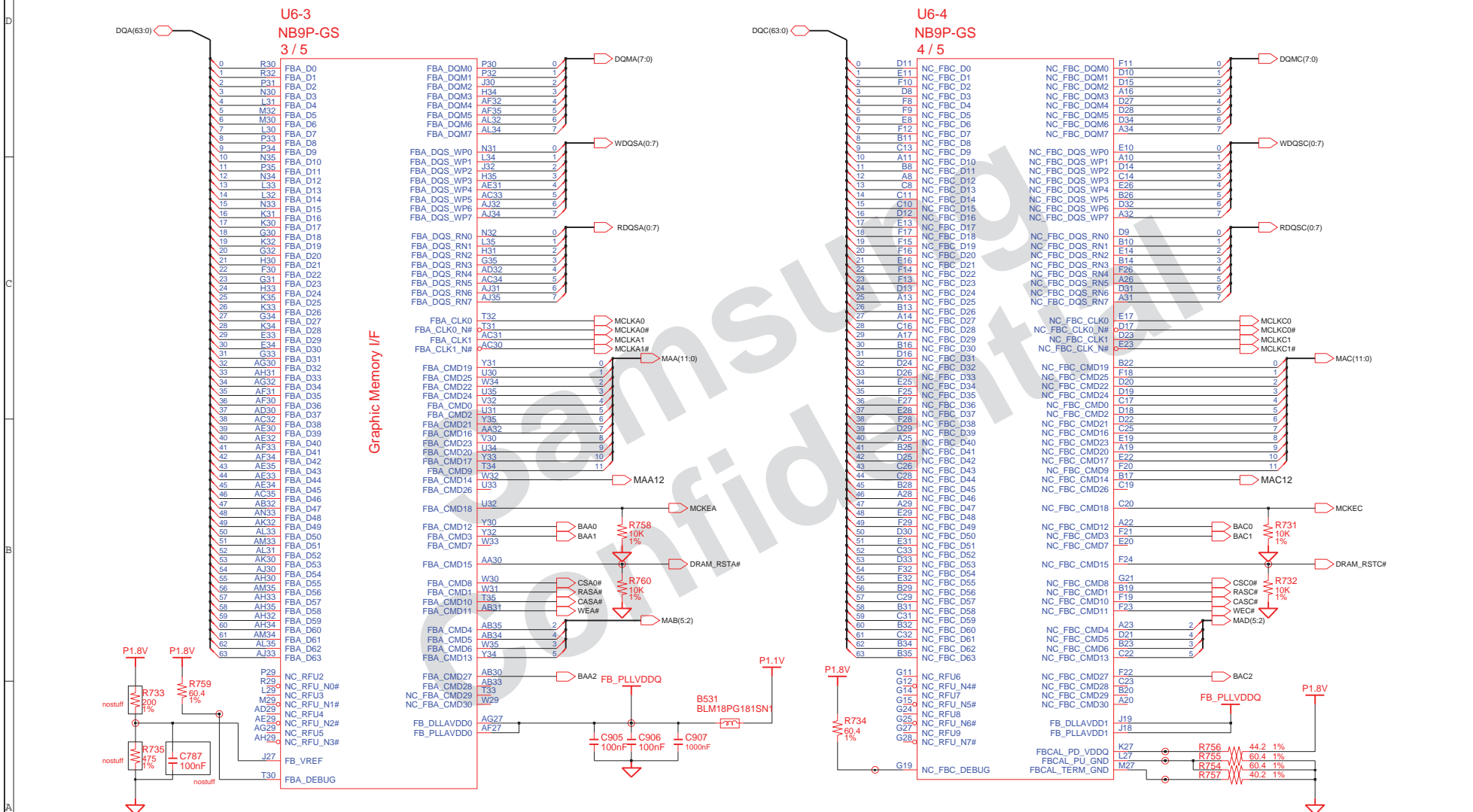
DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext EXT NB9X NB9X CHIP (2/5)	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
DATE	08, 2008 19:01:59 PM	PAGE	2	OF	6	

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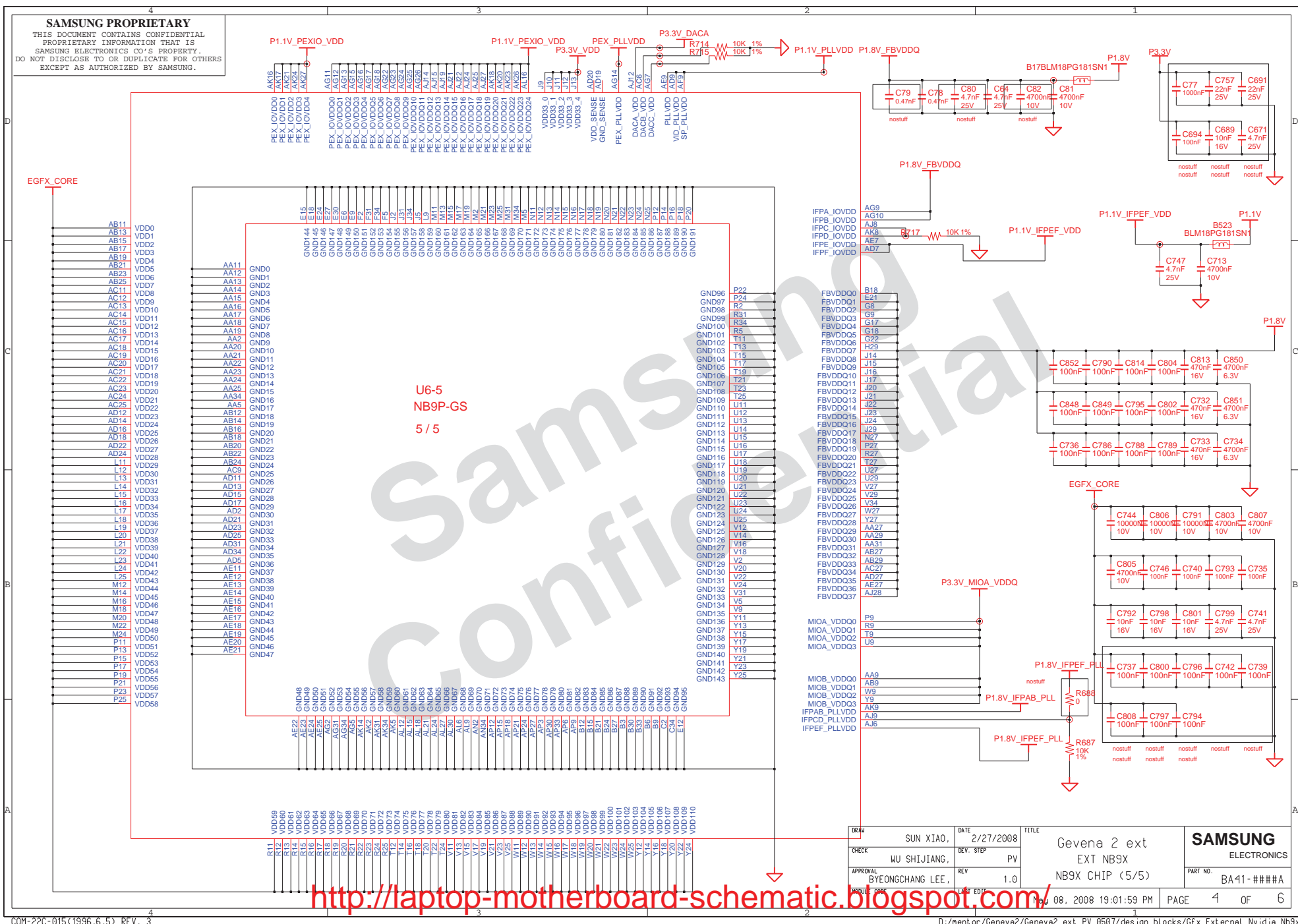
Graphic Memory I/F (Using FBA Channel)

Graphic Memory I/F (Using FBC Channel)



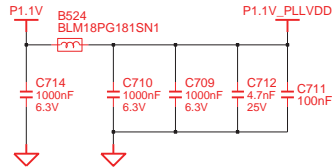
<http://laptop-motherboard-schematic.blogspot.com/>

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		EXT NB9X	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		NB9X CHIP (3/5) (4/5)	
DATE	08. 2008 19:01:59 PM	PAGE	3	OF	6	

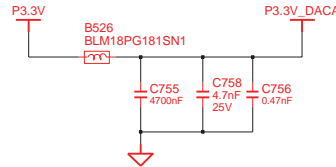


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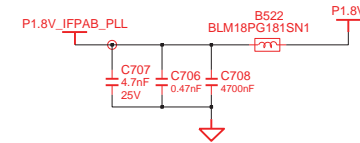
PLL_VDD



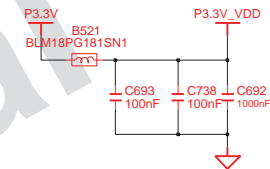
DACA/B/C



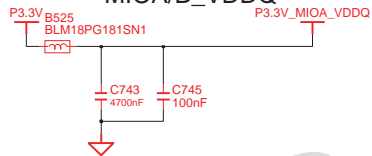
IFPAB_PLLVDD



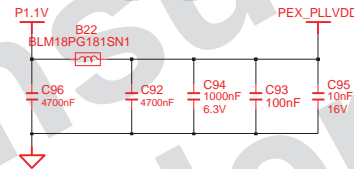
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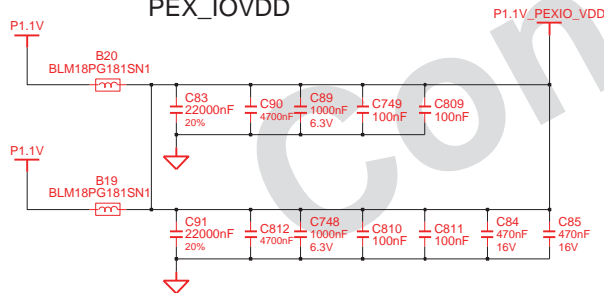
MIOA/B_VDDQ



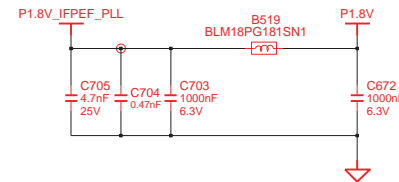
PEX_PLL_VDD



PEX_IOVDD



IFPEF_PLLVDD

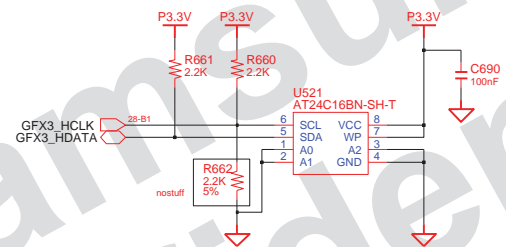


DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext EXT NB9X NB9X POWER RAIL	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
DESIGNED	CHANG	LAST EDIT				

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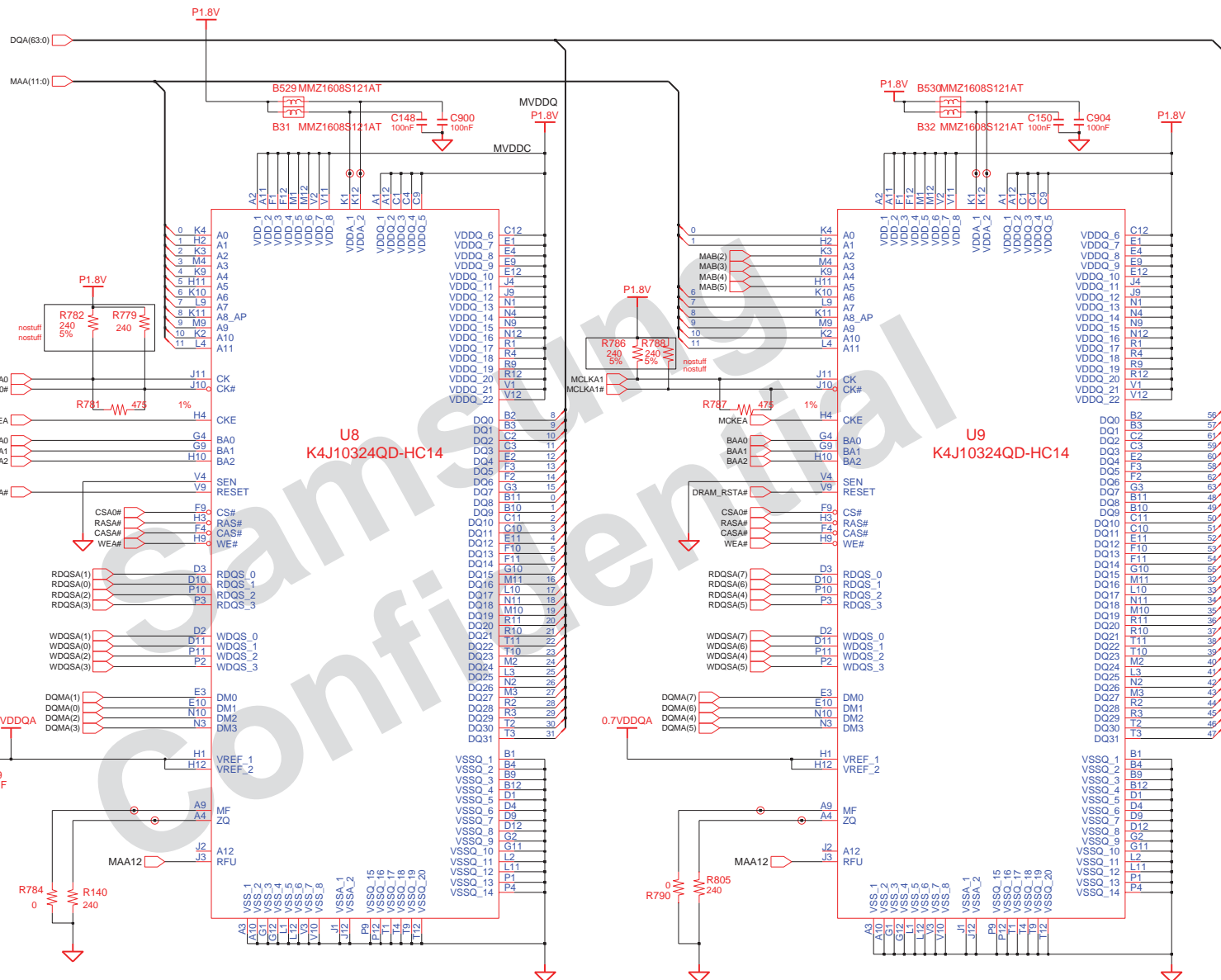
HDCP



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext EXT NB9X HDCP	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0			

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Video Memory (A Channel)



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV		Graphics_Memory	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		Graphics_Memory.Nvidia #1	
DESIGN	CHANG LEE,	DATE	08/08/2008 19:01:59 PM	PAGE	1 OF 2	

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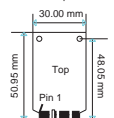
DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		Graphics_Memory	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		Graphics_Memory_Nvidia #3	
DESIGN	CHANG	LAST EDIT				

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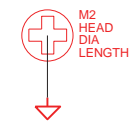
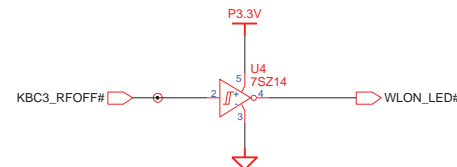
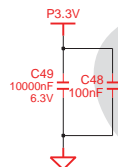
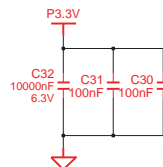
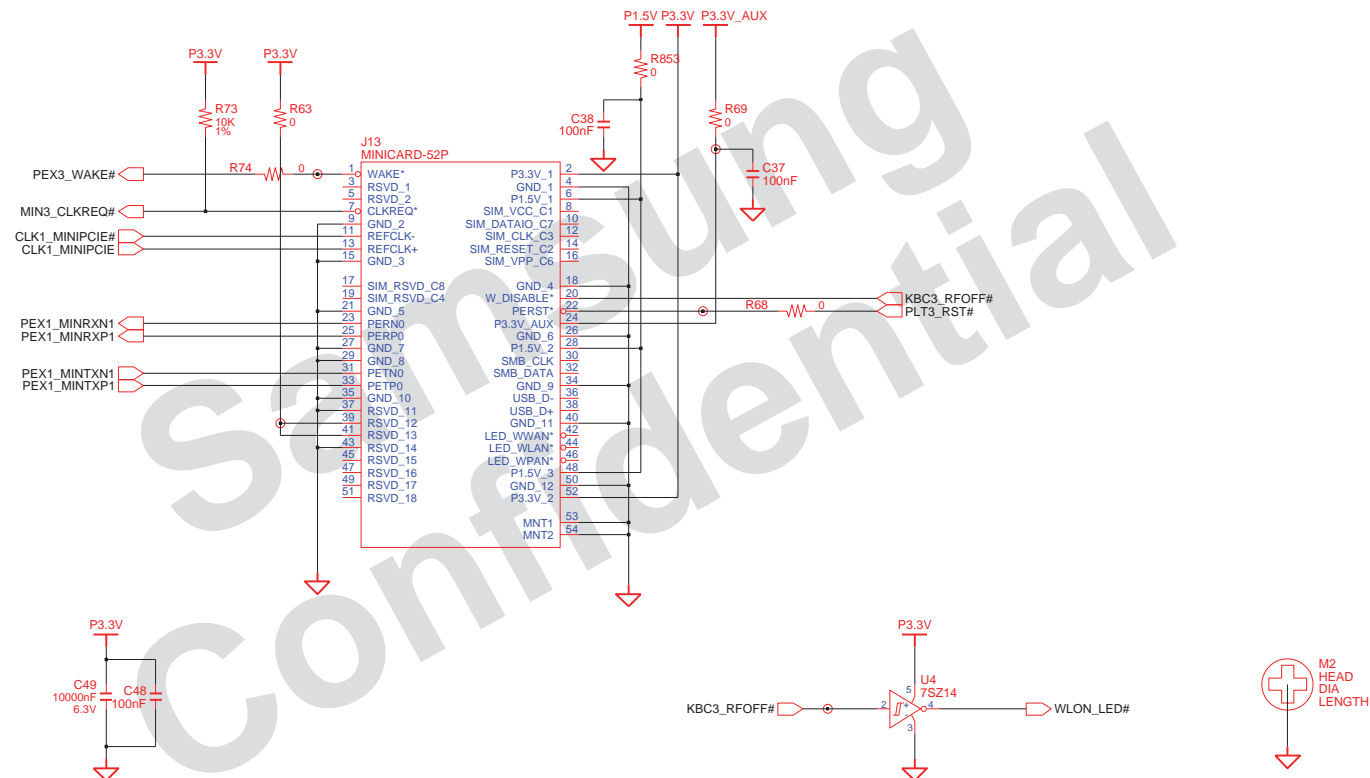
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Mini Card

Mini PCI Express Card



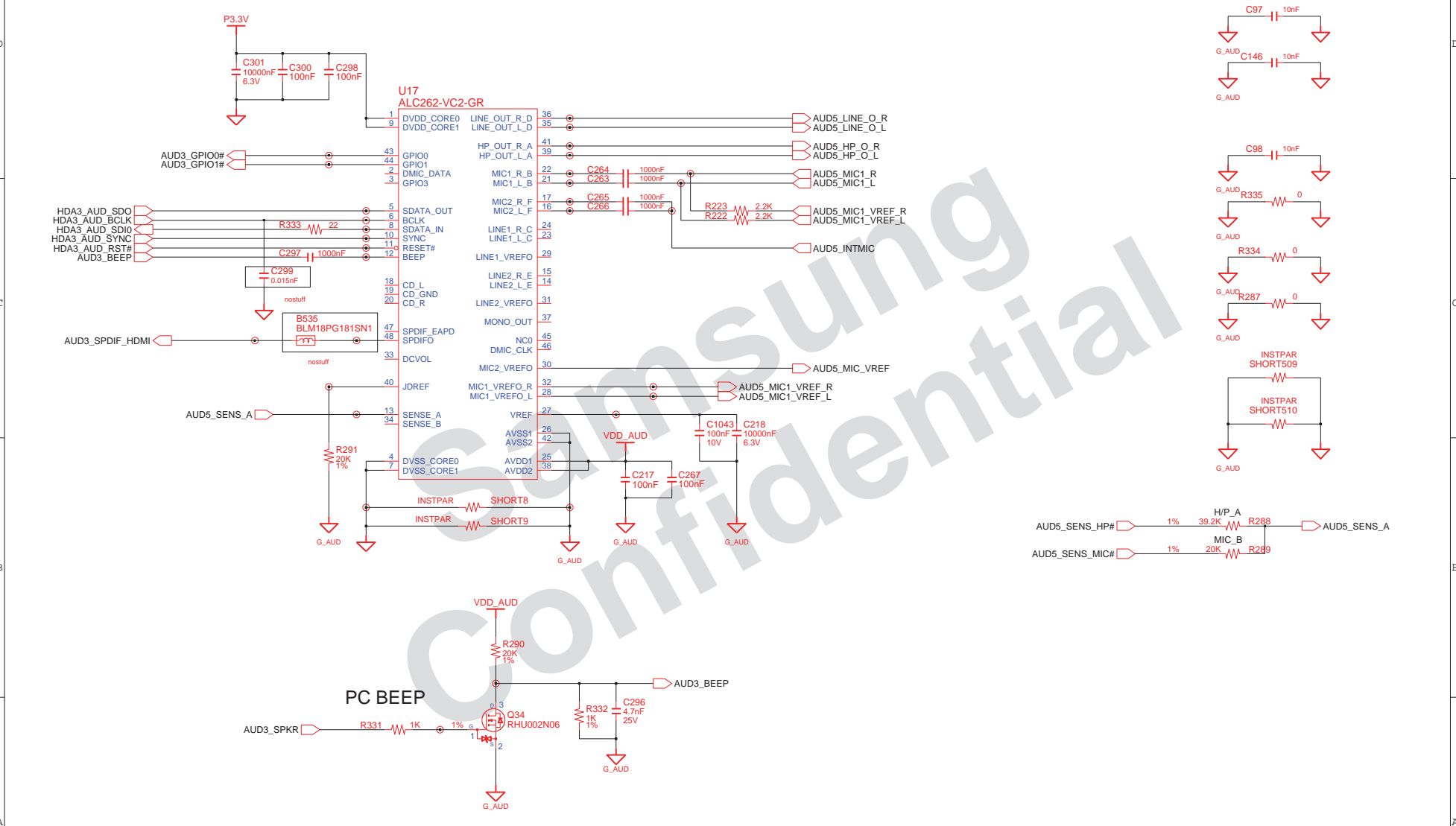
Odd Pins : Top side
 Even Pins : Bottom Side



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		PCIE_Minicard_Slot	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		PCIE_Minicard_Slot	
DESIGNED	UNDESIGNED	LAST EDIT				
Nov 08, 2008 19:01:59 PM						PAGE 1 OF 1

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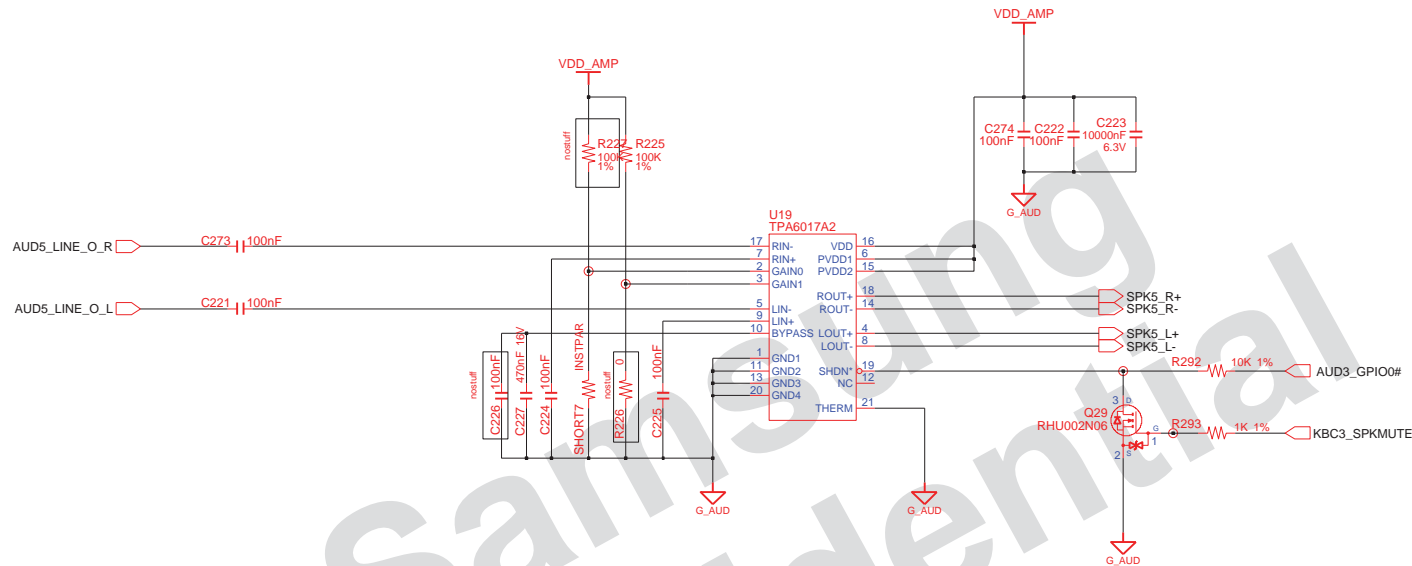
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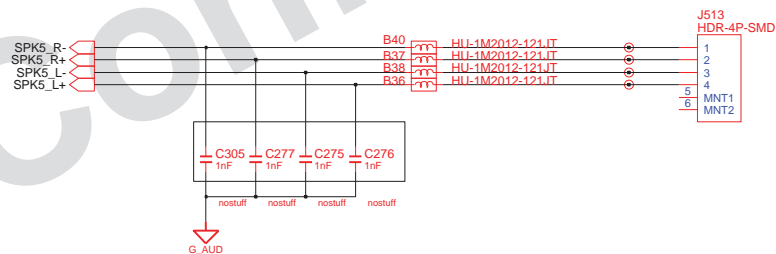
DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		HDA_Codec_Alc262	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		HDA_Codec_Alc262 #1	
DESIGNED	UNISE-THIRD	LAST EDIT				
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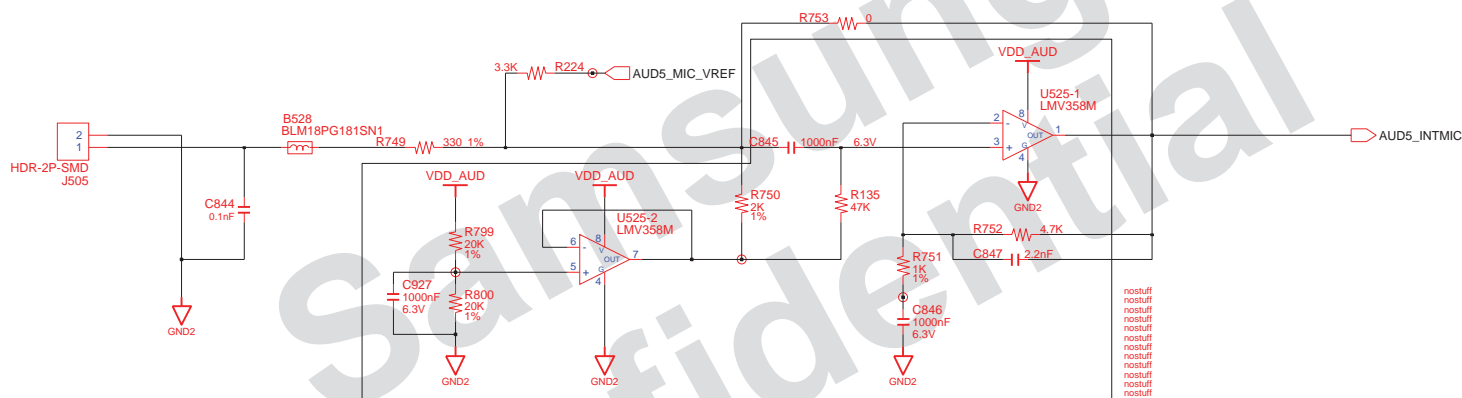
INTERNAL STEREO SPEAKERS



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	SAMSUNG ELECTRONICS PART NO. BA41-####A	
CHECK	WU SHIJIANG,	DEV. STEP	PV	HDA_Codec_Alc262		
APPROVAL	BYEONGCHANG LEE,	REV	1.0	HDA_Codec_Alc262 #2		
DESIGN	CHANG	DATE	Nov 08, 2008 19:01:59 PM	PAGE	2	OF 5

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Internal MIC

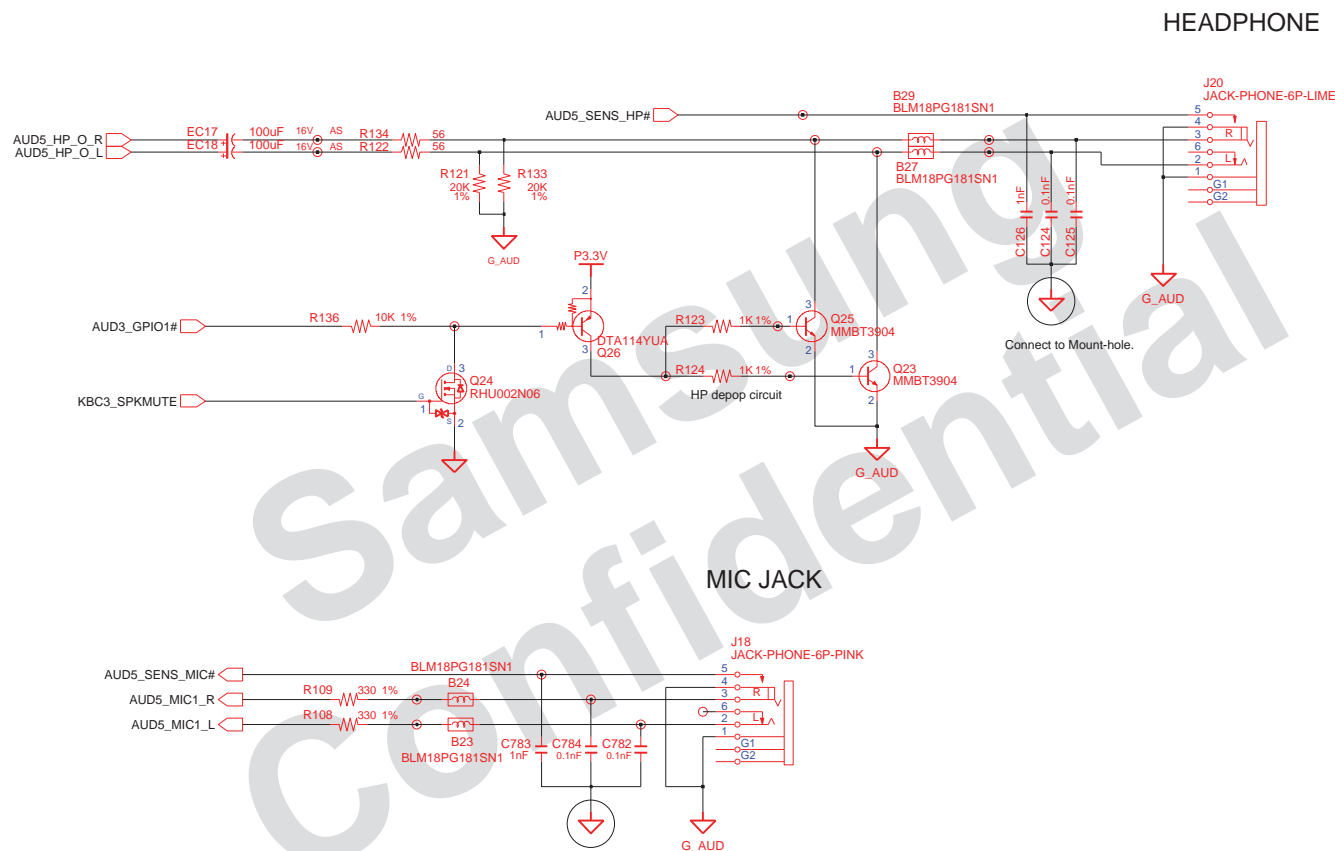


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DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		HDA_Codec_Alc262	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		HDA_Codec_Alc262 #3	
DESIGN	CHANG	UNDESIGNED	LAST EDIT			
Nov 08, 2008 19:01:59 PM						PAGE 3 OF 5

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The traces led to Audio Jacks have the width over 10mil

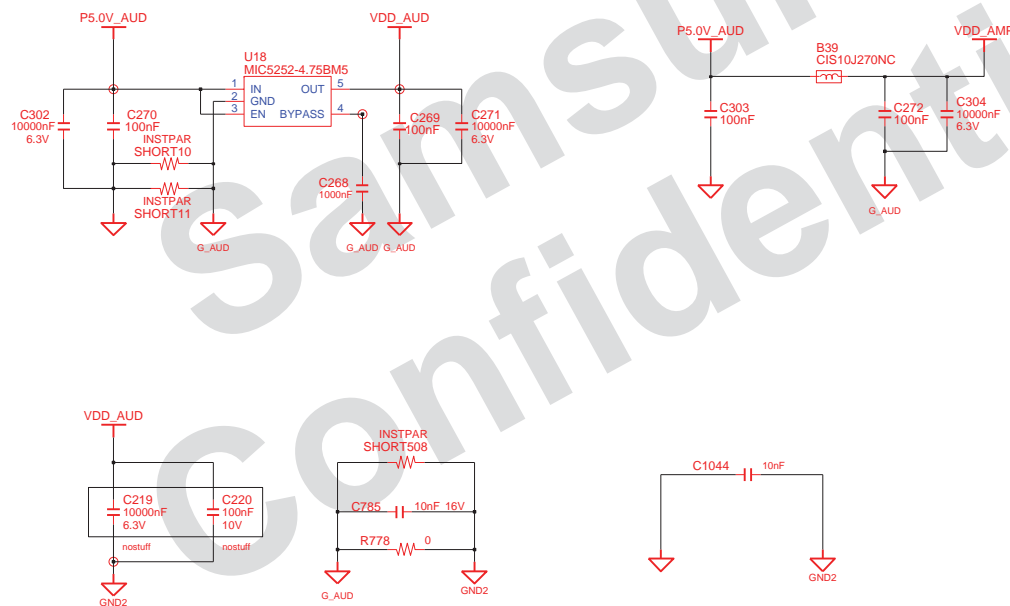
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CHECK	WU SHIJIANG,	DEV. STEP	PV		HDA_Codec_Alc262	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		HDA_Codec_Alc262 #4	
DESIGN	CHANG LEE,	LAST EDIT	Nov 08, 2008 19:01:59 PM	PAGE	4 OF 5	

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AUDIO POWER



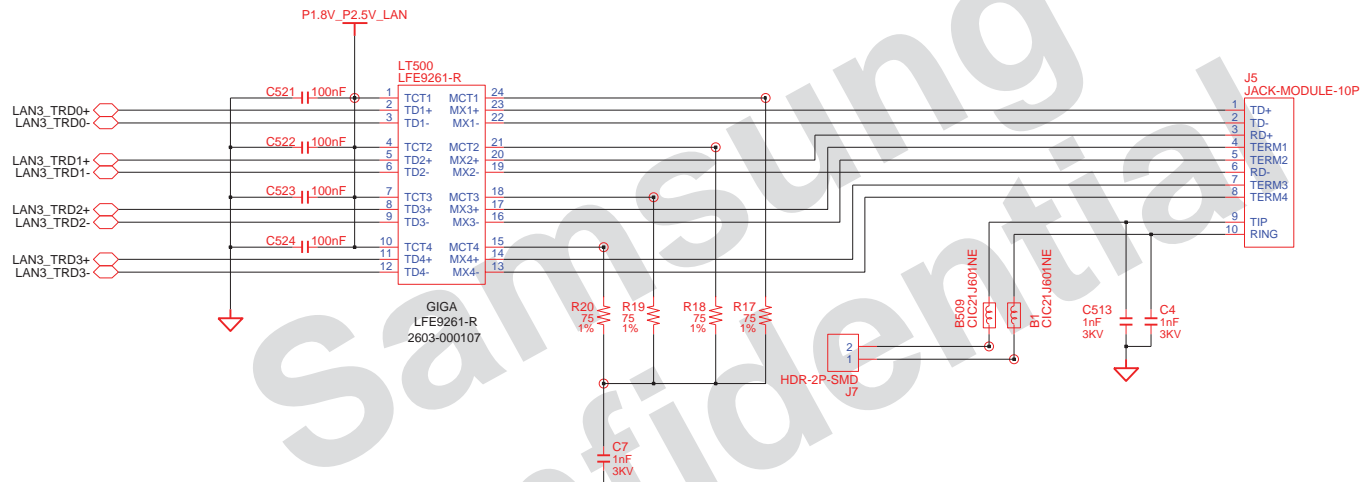
DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		HDA_Codec_Alc262	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		HDA_Codec_Alc262 #5	
DESIGNED	UNSE-1000	LAST EDIT				
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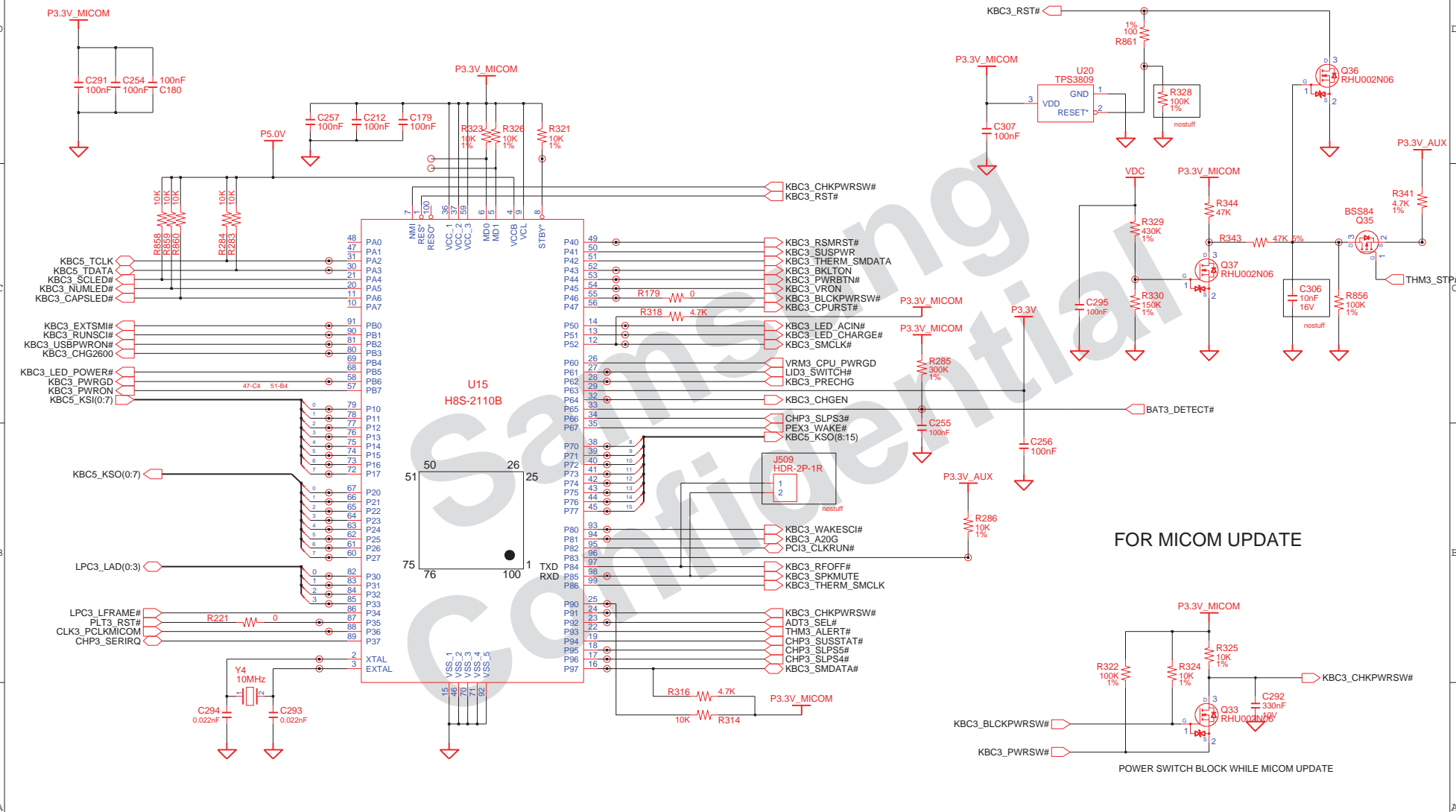
The distance between LAN controller
 and transformer is designed to extend less than two inches.



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		LAN_Marvell_8055	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		LAN_Marvell_8055	
DESIGN	CHANG LEE,	DATE	Nov 08, 2008 19:01:59 PM	PAGE	2 OF 2	

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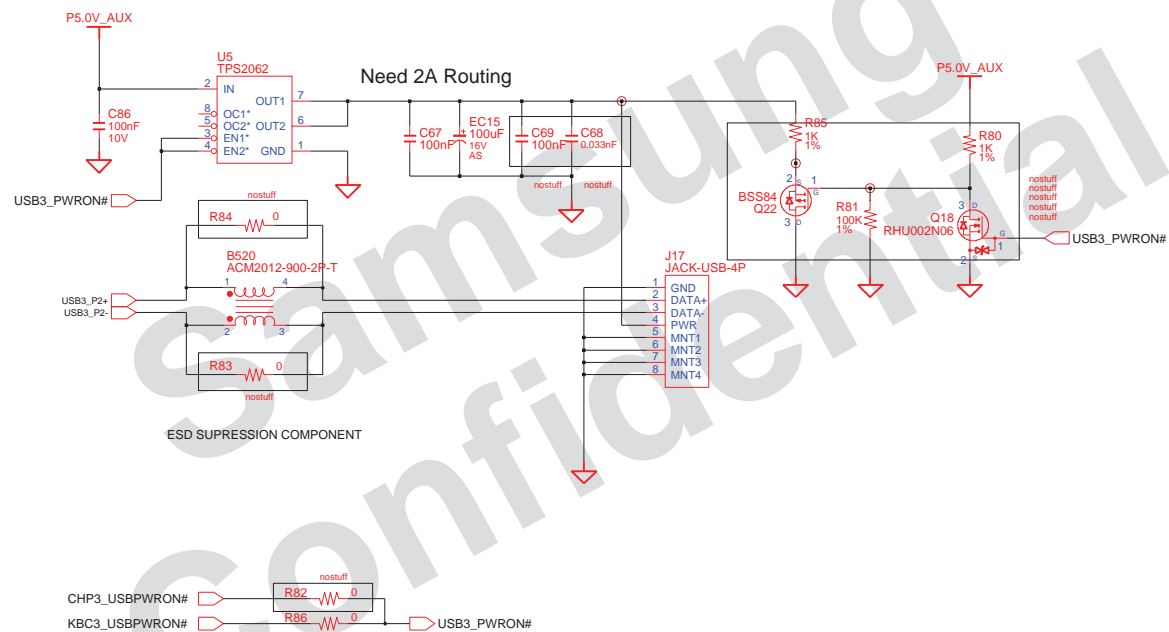


DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		MICOM_Renesas2110_100p	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		MICOM_Renesas2110_100p	
DATE	08, 2008 19:01:59 PM	PAGE	1	OF	1	

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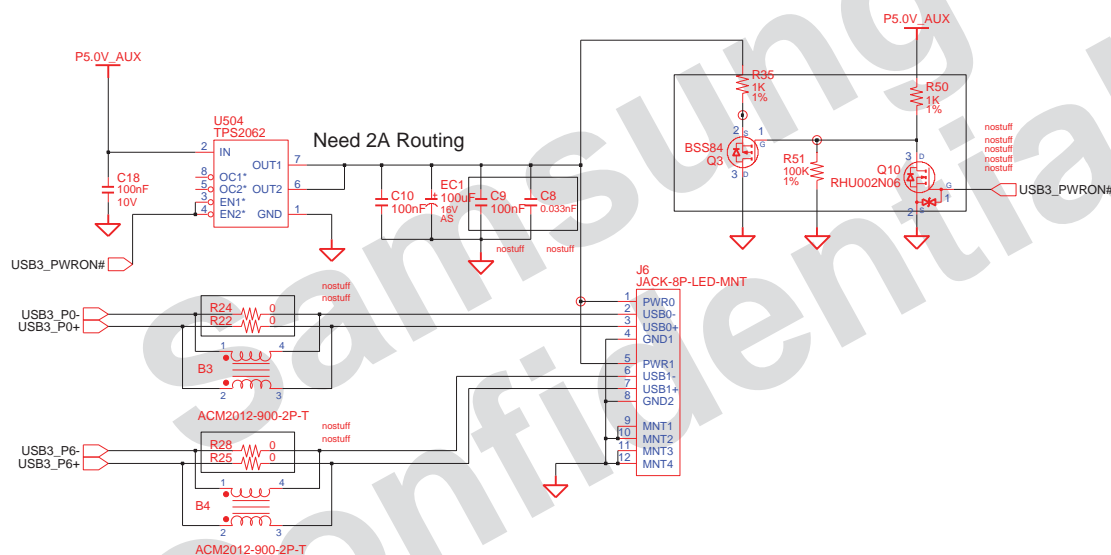
1 PORT USB CONNECTOR

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		USB_1Port	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		USB_1Port	

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2 PORT USB CONNECTOR

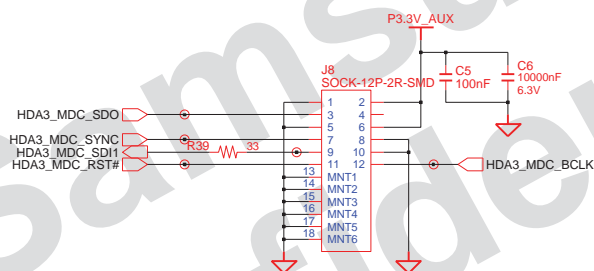


DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		USB_2Port	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		USB_2Port	
DESIGN		LAST EDIT				

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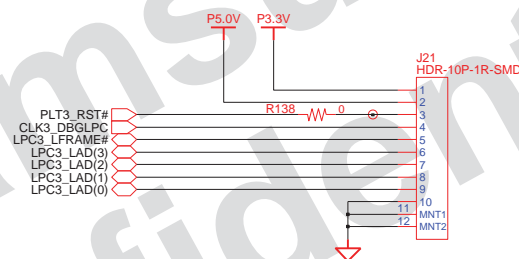
MDC Connector

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV		HDA_Modem	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		HDA_Modem	
DESIGN	CHANG LEE,	LAST EDIT	Nov 08, 2008 19:01:59 PM	PAGE	1 OF 1	PART NO. BA41-####A

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80H DECODER CONNECTOR

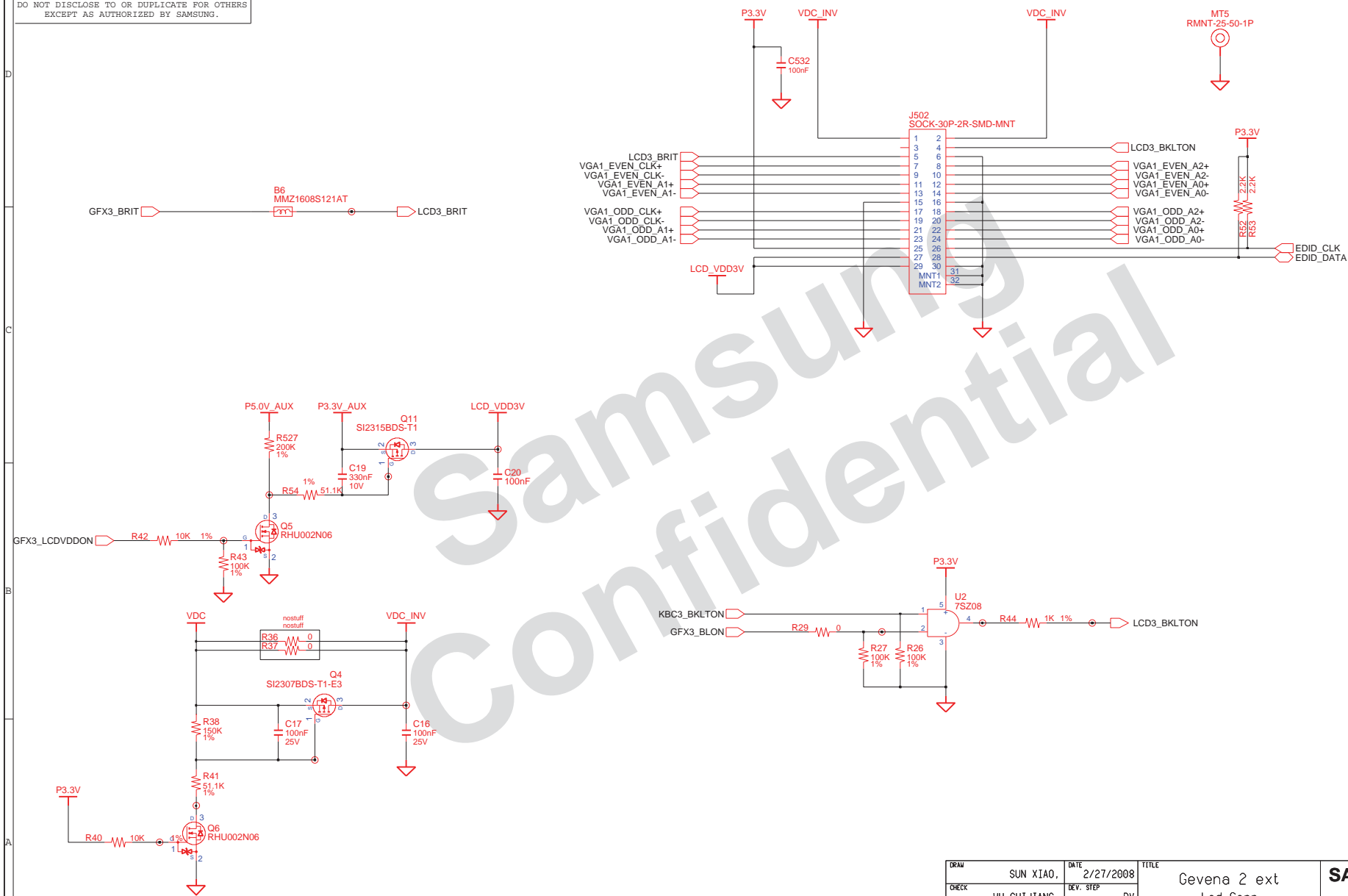


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DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		Other_Debug_80	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		Other_Debug_80	
DESIGNER	CHANG LEE,	LAST EDIT	Nov 08, 2008 19:01:59 PM	PAGE	1	OF 1

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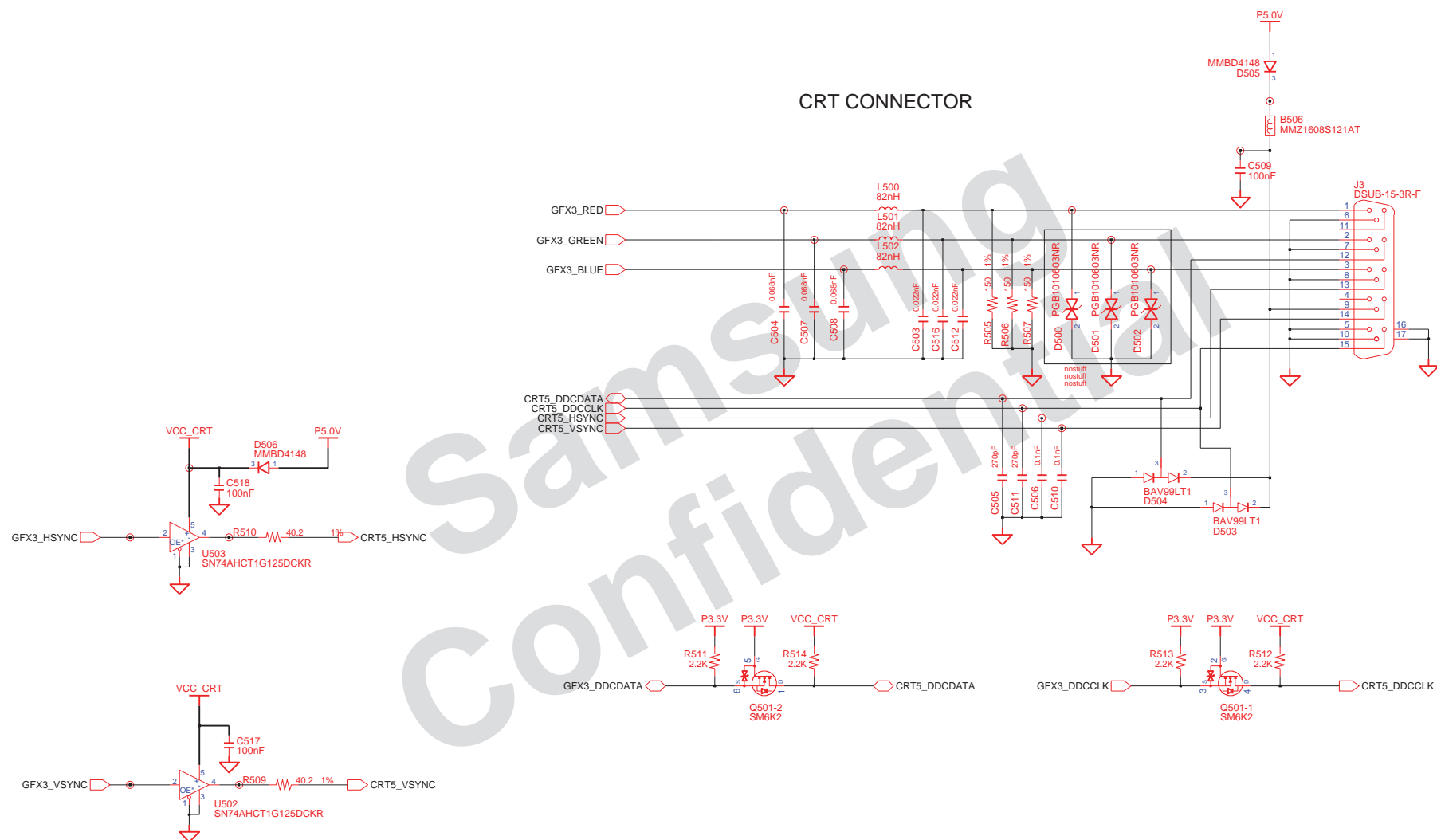


DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext Lcd Conn	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
DATE	2008.08.08	TIME	19:01:59 PM	PAGE	1 OF 1	

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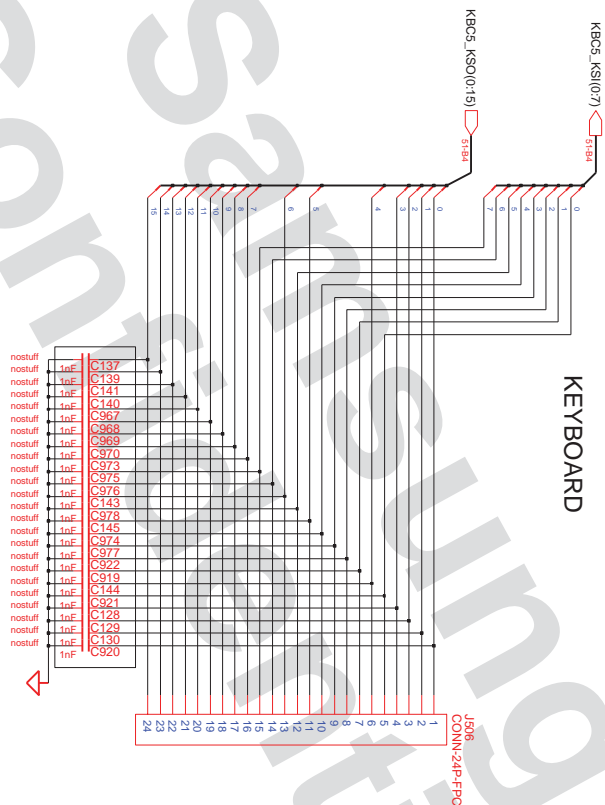
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CRT CONNECTOR

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext Interface_Circuit Graphics_IF_CRT	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
DATE	08, 2008 19:01:59 PM	PAGE	1	OF	1	

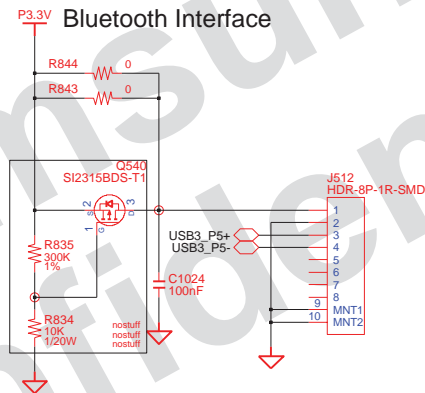
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REV	DATE	TITLE	SAMSUNG
0001	2/27/2008	Geveva 2 ext	ELECTRONICS
0002	REV. STEP	KBD_IF_Conn	
0003	PV	KBD_IF_Conn	
0004	REV	1.0	BA-11-####A
0005	LAST EDIT	May 08, 2008 19:01:59 PM	
0006	ROUTE CODE	PAGE 1	OF 1

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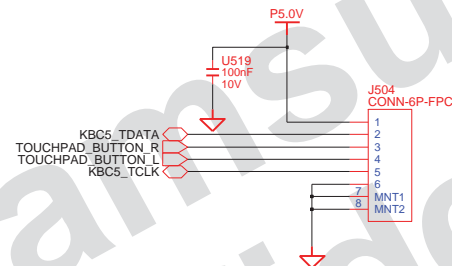


DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext Bluetooth_IF_Conn Bluetooth_IF_Conn	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
DESIGNER	CHANG	LAST EDIT	Nov 08, 2008 19:01:59 PM	PAGE	1 OF 1	

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TOUCHPAD CONNECTOR

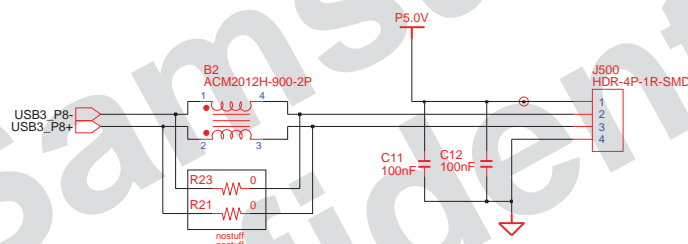


DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext Touchpad_IF_Conn Touchpad_IF_Conn	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
DESIGNER	CHANG LEE,	LAST EDIT	Nov 08, 2008 19:01:59 PM	PAGE	1 OF 1	

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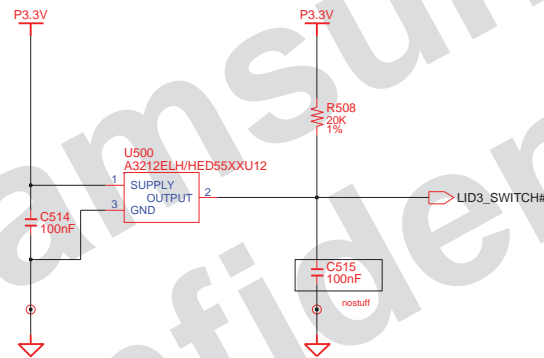
USB CAMERA FUNCTION

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext Camera_IF_Conn	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		Camera_IF_Conn	
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
DESIGNER		LAST EDIT		Nov 08, 2008 19:01:59 PM		PAGE 1 OF 1

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LID_SWITCH



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext LID_Switch LID_Switch	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
DESIGNER	CHANG LEE,	LAST EDIT	Nov 08, 2008 19:01:59 PM	PAGE	1 OF 1	

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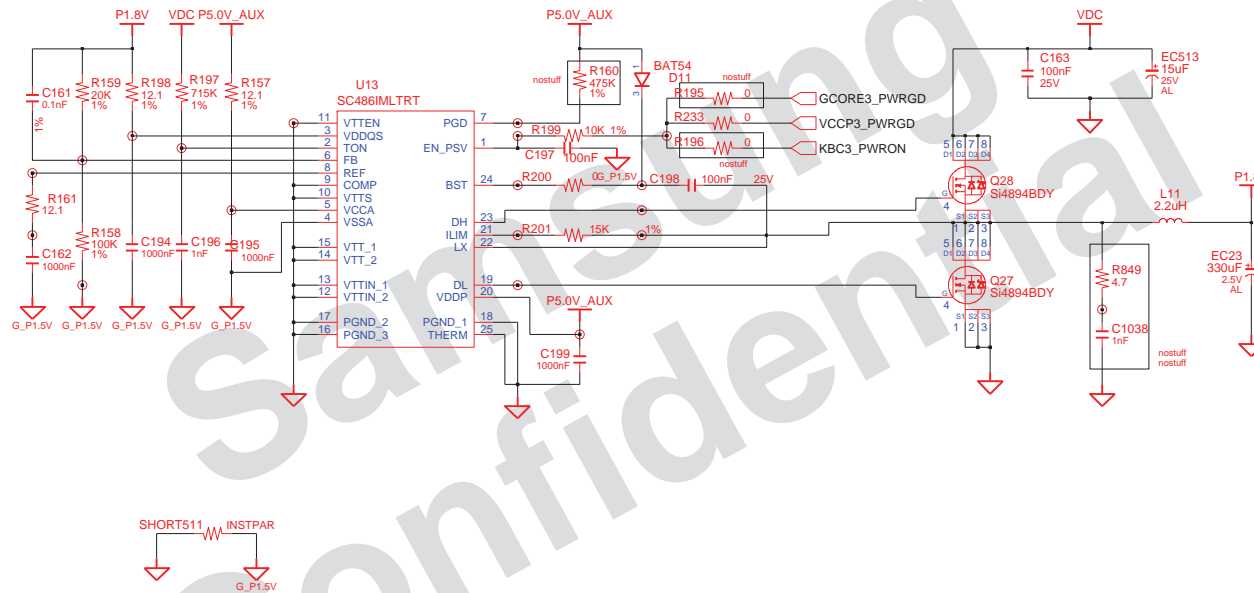
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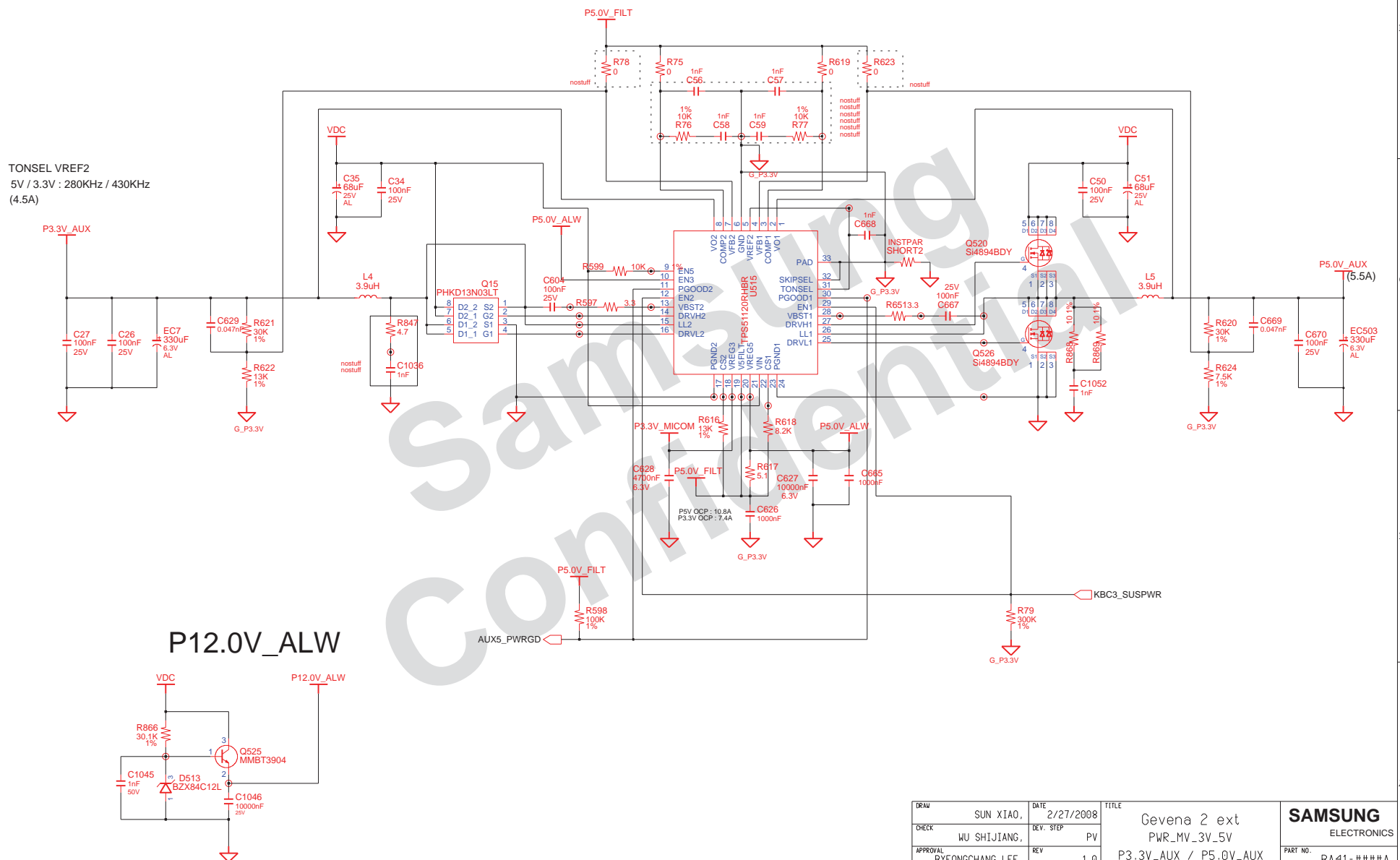


DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV	Geneva 2 ext PWR_Gfx_MV_Ext	
APPROVAL	BYEONGCHANG LEE,	REV	1.0	Ext Gfx Memory(SC486)	
DESIGNER	CHANG LEE,	LAST EDIT	Nov 08, 2008 19:01:59 PM		
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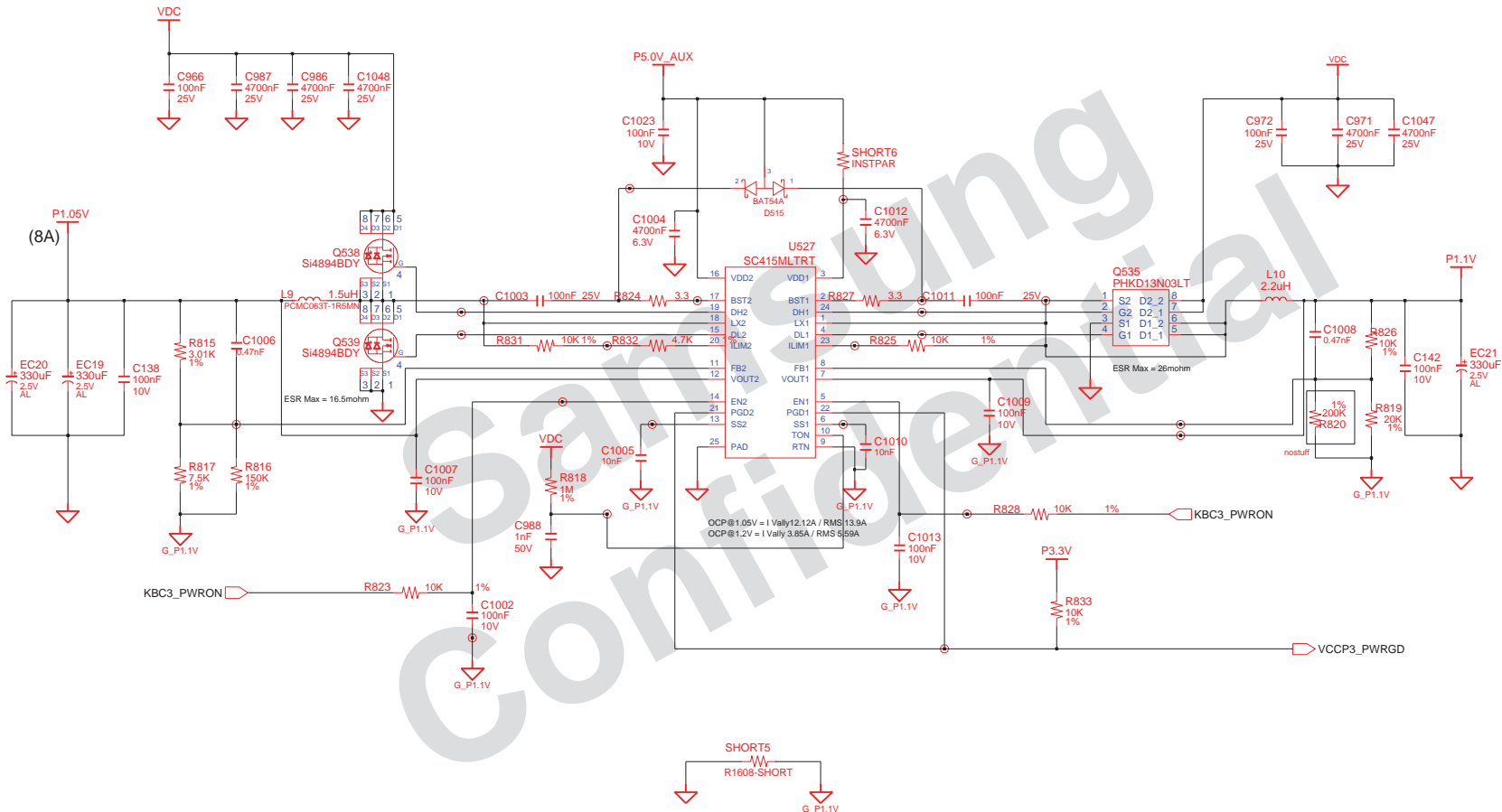
P3.3V_AUX & P5.0V_AUX



DRAW SUN XIAO.		DATE 2/27/2008		TITLE Gevena 2 ext PWR_MV_3V_5V		SAMSUNG ELECTRONICS	
CHECK WU SHIJIANG.		REV. STEP PV					
APPROVAL BYEONGCHANG LEE.		REV 1.0		P3.3V_AUX / P5.0V_AUX		PART NO. BA41-####A	
PREPARED BY DESIGNED BY CHECKED BY DATE 08_08_2008 19:01:59 PM		LAST EDIT 1 OF 1		PAGE 1 OF 1			

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CHIPSET POWER(P1.05V & P1.1V)



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV		PWR_MV_Cantiga	
APPROVAL	BYEONGCHANG LEE,	REV	1		Chipset Power (P1.05V_M,P1.1V)	
DESIGN	CHANG LEE,	LAST EDIT	Nov 08, 2008 19:01:59 PM		PART NO. BA41-####A	
PAGE 1 OF 1						

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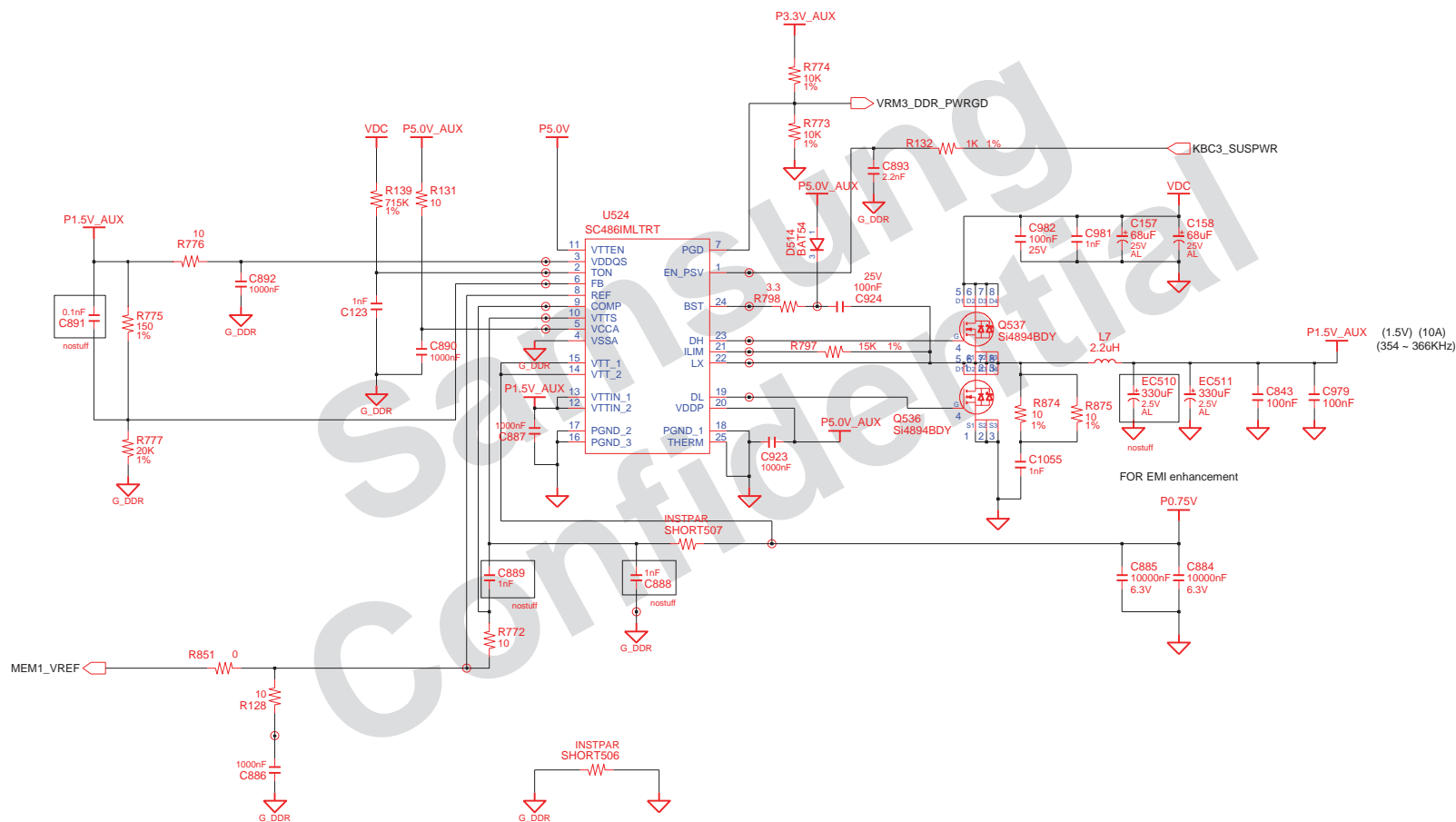
CHARGER & POWER MANAGEMENT



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DDR3 Power

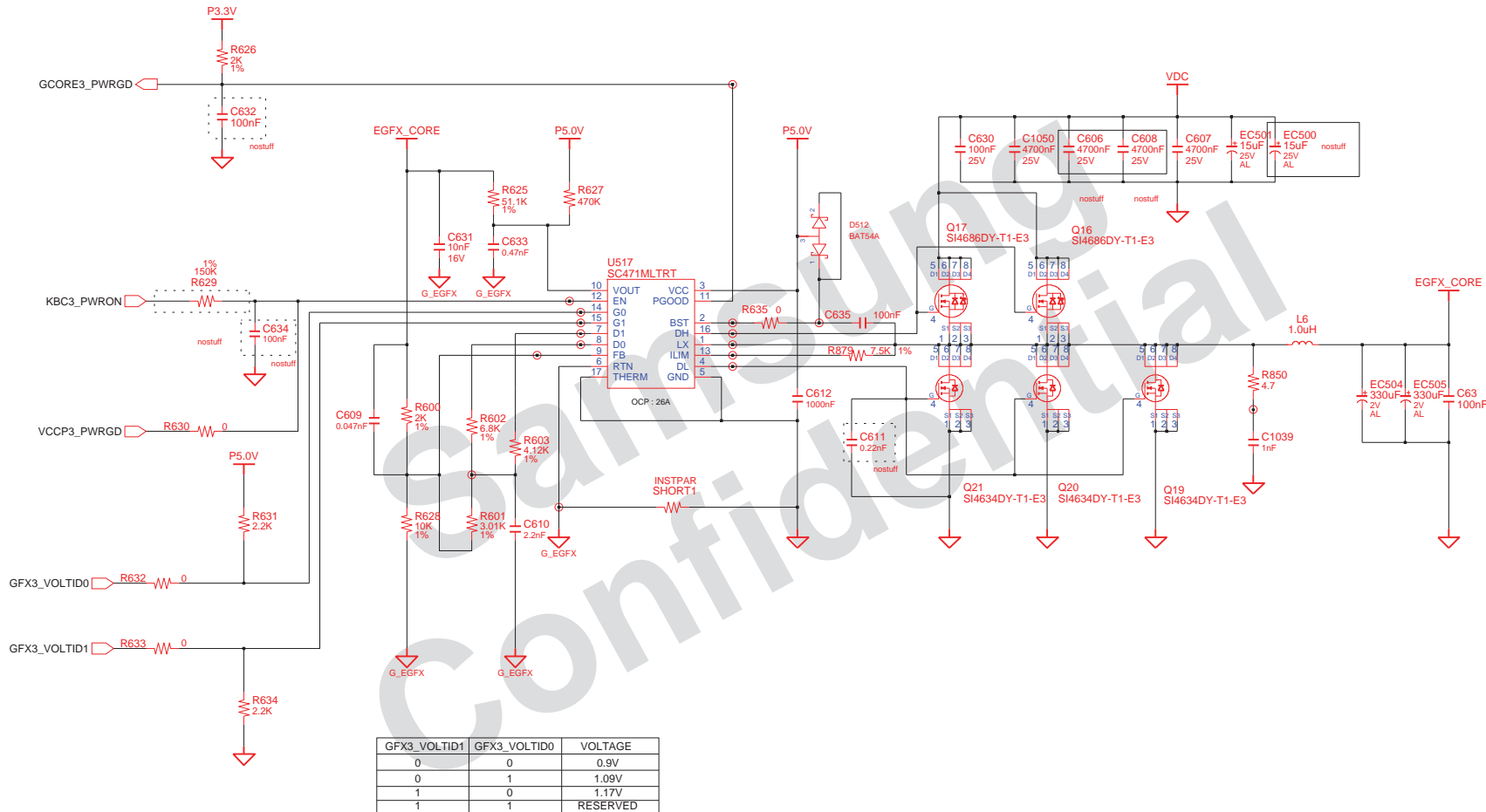


DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		PWR_MV_Memory	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		DDR3 POWER (P1.5V_AUX)	
DESIGNED	UNSEI YAMADA	LAST EDIT	Nov 08, 2008 19:01:59 PM	PAGE	1 OF 1	

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Graphic Core Power



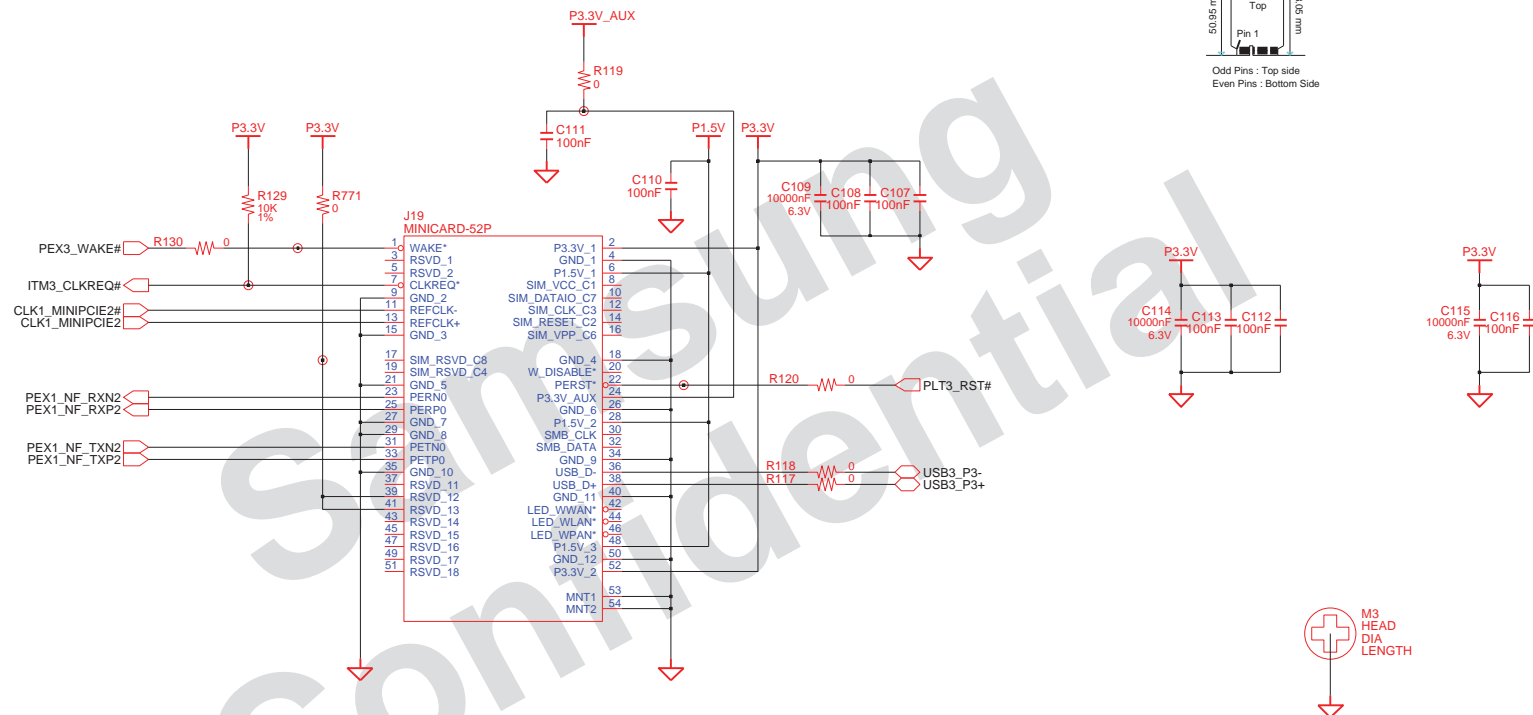
DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	SAMSUNG ELECTRONICS PART NO. BA41-####A	
CHECK	WU SHIJIANG,	DEV. STEP	PV	Geneva 2 ext PWR_Gfx_MV_Ext		
APPROVAL	BYEONGCHANG LEE,	REV	1.0	Ext Gfx Core(SC471)		
DESIGN	CHANG LEE,	DATE	08/08/2008	TIME	19:01:59 PM	
PAGE				2	OF	2

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MINI CARD FOR ROBSON



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext Robson_PCIE Robson_PCIE	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0			

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