CR-1 : 8@FROSTBURG_FABC_LIB.FROSTBURG_FABC(SCH_1):PAGE1

PAGE #	COMPONENT/FUNCTION
[1.	INDEX]
[2.	BLOCK DIAGRAM]
[3.	RESET MAP]
[4.	CLOCK DISTRIBUTION]
[5.	GPIO, IRQ, IDSEL MAP]
[6.	CPU-SOCKET 1 OF 2]
[7.	CPU SOCKET 2 OF 2]
[8.	CPU TERMINATION & MISC P/U P/D]
[9.	CPU PLL FILTERED SUPPLY]
[10.	MCH SECTIONS PAGE 1 OF 6]
[11.	MCH SECTIONS PAGE 2 OF 6]
[12.	MCH SECTIONS PAGE 3 OF 6]
[13.	MCH SECTIONS PAGE 4 OF 6]
[14.	MCH SECTIONS PAGE 5 OF 6]
[15.	MCH SECTIONS PAGE 6 OF 6]
[16.	PLL & CRT FILTERS]
[17.	MCH DECOUPLING AND COMP]
[18.	MCH DCPL & VGA TERMINATION]
[19.	MCH VREFS & TERMINATION]
[20.	VGA CONNECTOR]
[21.	PCI EXPRESS X16]
[22.	PCI EXPRESS X16]
[23.	PCI EXPRESS X16 COUPLING]
[24.	240P CONN DDR2, CH A]
[25.	240P CONN DDR2, CH B]
[26.	DDR VTT TERMINATION]
[27.	DDR VTT DECOUPLING]
[28.	CK505 PAGE 1 OF 2]
[29.	CK505 PAGE 2 OF 2]
[30.	ICH9 1 0F 6 CONTROL]
[31.	ICH9 2 OF 6 CONTROL]
[32.	ICH9 3 OF 6 CONTROL]
[33.	ICH9 4 OF 6 - CONTROL]
[34.	ICH 5 OF 6 - CONTROL]
[35.	ICH 6 OF 6 - GROUND BODY]
[36.	GPIO TERMINATION & RST STRAPS]
[37.	ICH PIN STRAPS]
[38.	ICH DECOUPLING]
[39.	ME & CONTROL BUFFERS/ICH CIRCUITS]
[40.	SERIAL FLASH PRIMARY]
[41.	SATA CONNECTORS]
[42.	USB FP HDR 1]
[43.	USB FP HDR 2]
[44.	USB FP HDR 2]
[45.	BACK PANEL USB]
[46.	BACK PANEL USB WITH ESATA]
[47.	PCI EXPRESS X1 #1]
[48.	PCI CONN 1]
[49.	PCI CONN 2]

PAGE #	COMPONENT/FUNCTION
[50.	PCI TERMINATION]
[51.	STD FRONT PANEL HDR]
[52.	USB_FP_HEADER_POWER]
[53.	1394 CONTROLLER]
[54.	1394 BP REV1]
[55.	1394 PWR/DCPL]
[56.	LAN NINEVEH]
[57.	LAN NINEVEH]
[58.	LAN NINEVEH]
[59.	AUDIO CODEC]
[60.	AUDIO DECOUPLING & JACK SENSE]
[61.	AUDIO SPDIF]
[62.	AUDIO JACK (BLUE GREEEN PINK]
[63.	AUDIO JACK (BLACK ORANGE]
[64.	AUDIO FP HEADERS & HDA HEADER]
[65.	AUDIO MIC BIAS]
[66.	AUDIO VREG]
[67.	SPDIF HEADER]
[68.	TPM 1.2]
[69.	PORT ANGELES 1 OF 2]
[70.	PORT ANGELES 2 OF 2]
[71.	FDD CONN]
[72.	PS/2 CONNECTOR]
[72.	LPT SIGNALS]
[73.	LPT SIGNALS]
[74.	SERIAL PORT A]
[75.	STUDIES PURPOSE]
[76.	SST SENSOR]
[77.	FAN CONFIGURATION]
[78.	MTG HOLES/LABELS]
[79.	CORE VREG]
[80.	CORE VREG]
[81.	VREG_SM_VTT]
[82.	VREG_1P25_CORE MCH]
[83.	MCH DCPL]
[84.	CORE VREG]
[85.	VREG_FSB VTT & SFR]
[86.	VREG 1.25 MCH CL]
[87.	CORE VREG]
[88.	CORE VREG]
[89.	CORE VREG]
[90.	NO PAGE TITLE FOUND!!!]
[91.	WAKE CONTROL SWITCH PS2/USB (BP RIGHT)]
[92.	VREG: DECOUPLING AND STITCHING]
[93.	VCCP VREG]
[94.	VCCP VREG]
[95.	VCCP VREG]
[96.	VREG: VCCP DECOUPLING / 2X2 CONN]

PAGE #	COMPONENT/FUNCTION
[97.	PRIMARY XDP-LITE]
[98.	PATA]
[99.	PATA]
[100.	TEST SITE CAPS]
[101.	PCI EXPRESS X1 #2]
[102.	PCI EXPRESS X1 #3]
[103.	PCI CONN 3]
[104.	AUX FAN CONFIGURATION]
[105.	HARDWARE MANAGEMENT: HECETA]
[106.	ITE IT8211F 1 OF 2]
[107.	PATA 2ND CONNECTOR]

REVISIONS

REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
2.02	DESIGN		2006				

BEARLAKE-B ATX

CLASSIC SKU

FROSTBURG DRAGONTAIL PEAK

FAB C

TAPE-OUT: WWXX-2006
FAB A REV 3.03

CONROE, BEARLAKE, DDR?, ICH9,
2-CHANNEL DDR2, PCIEXPRESS GFX, ATX
CUSTOMER REFERENCE BOARD

POWER SYMBOLS USED:
VCC3
VCC
+12V
-12V

NOTES:

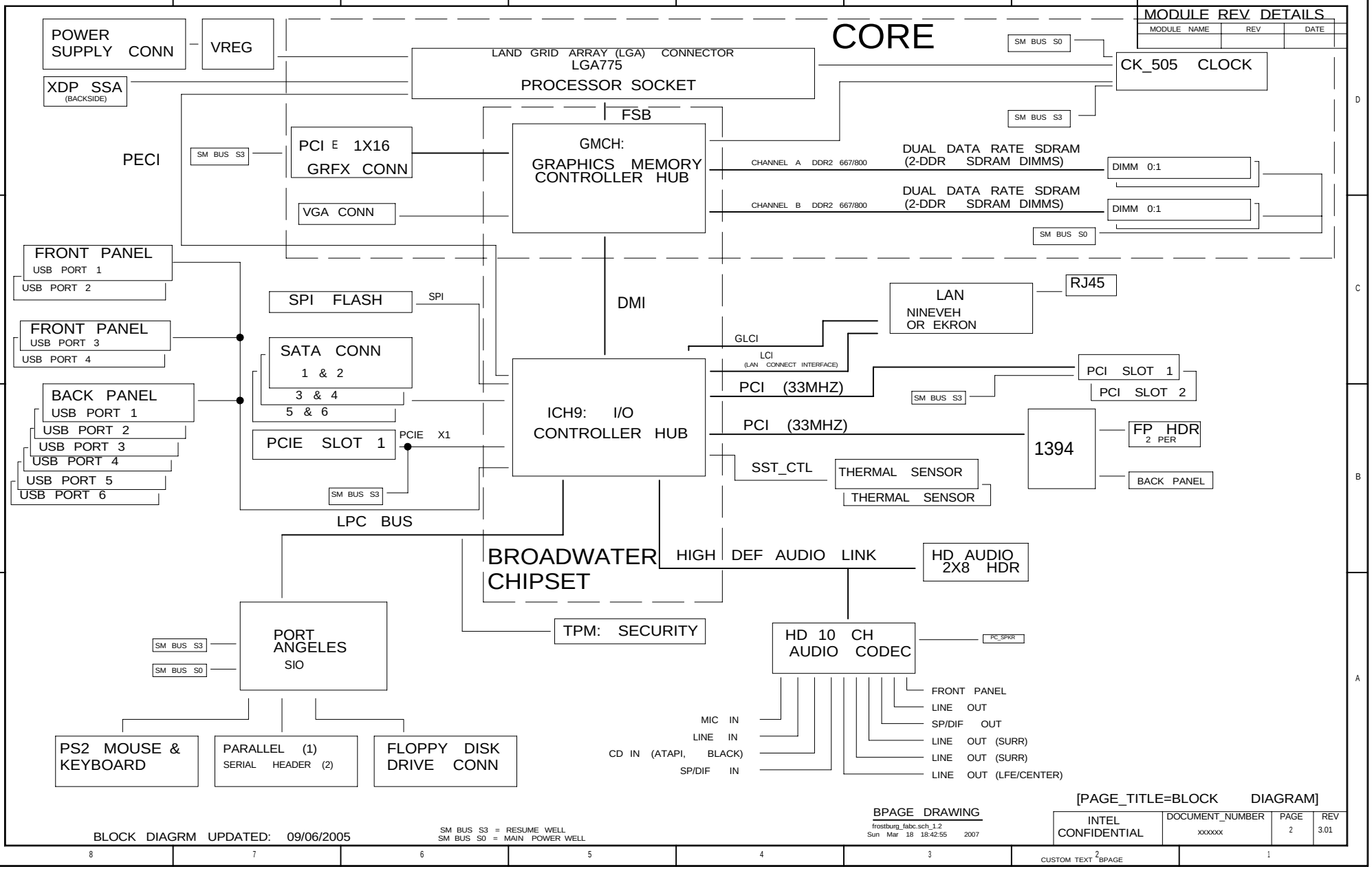
1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPL s FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

[PAGE_TITLE=INDEX]

BPAGE DRAWING

frostburg_fabc.sch_1.1
Sun Mar 18 18:42:55 2007

BOM_RELEASE_DATE	↑	PB_NUMBER ?	
SIGNATURE	DATE	inte	3065 BOWERS AVE SANTA CLARA, CA 95051
DRN_BY ↑	↑		
CHK_BY ↑	↑	TITLE ?	
ENGR_APVD ↑	↑		
CUSTOM TEXT B-PAGE		INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxx / PAGE 1/107 / REV 3.01



BLOCK DIAGRM UPDATED: 09/06/2005

SM BUS S3 = RESUME WELL
SM BUS S0 = MAIN POWER WELL

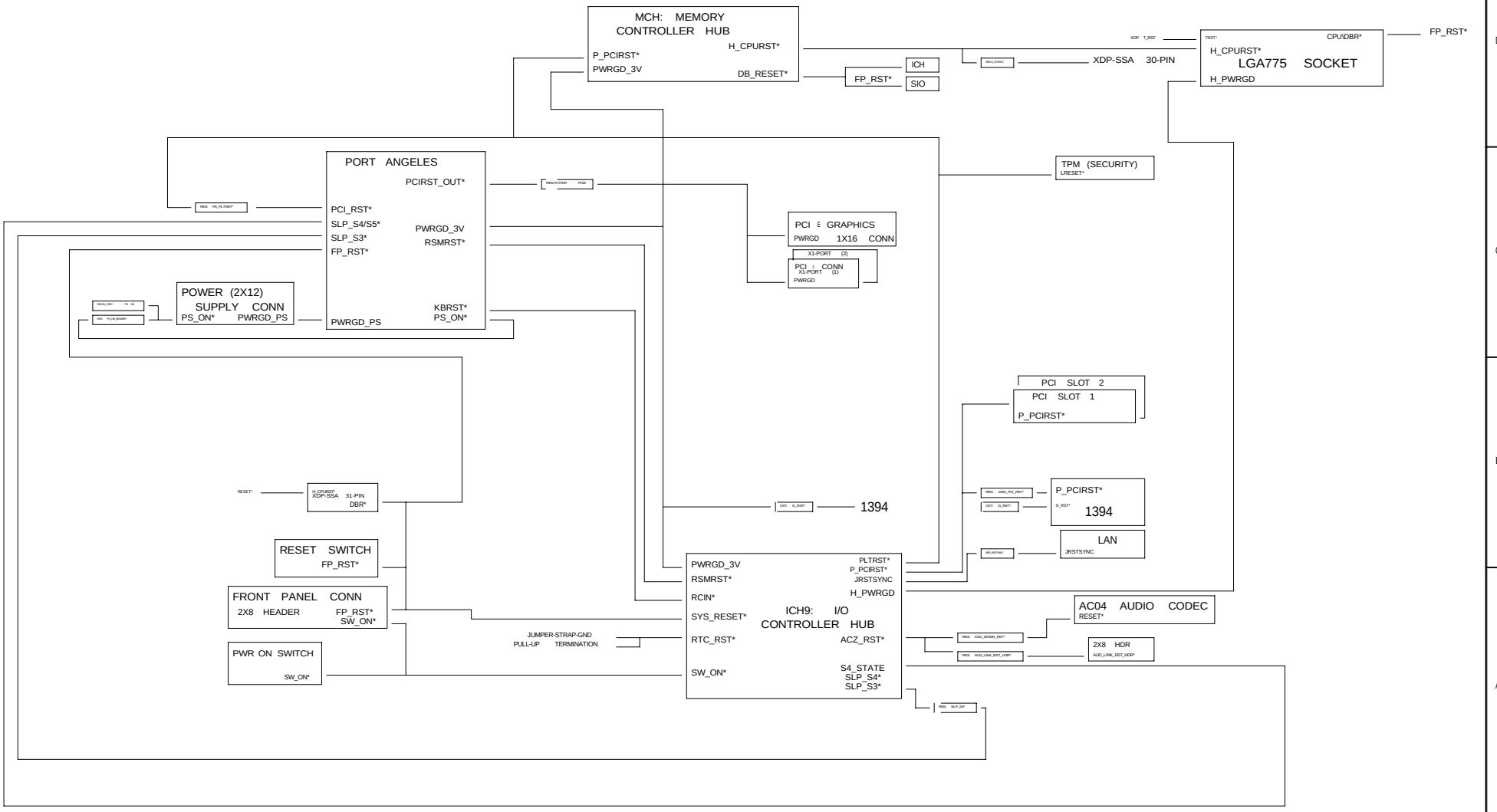
BPAGE DRAWING
frostburg_fabc.sch_1.2
Sun Mar 18 18:42:55 2007

[PAGE_TITLE=BLOCK DIAGRAM]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	2	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE

AFTER P_PCIRST*, HANDSHAKE (ON HL BUS) BETWEEN ICH/MCH MUST HAPPEN BEFORE H_CPURST* WILL BE ASSERTED/DE-ASSERTED



RESET MAP UPDATED: 09/06/2005

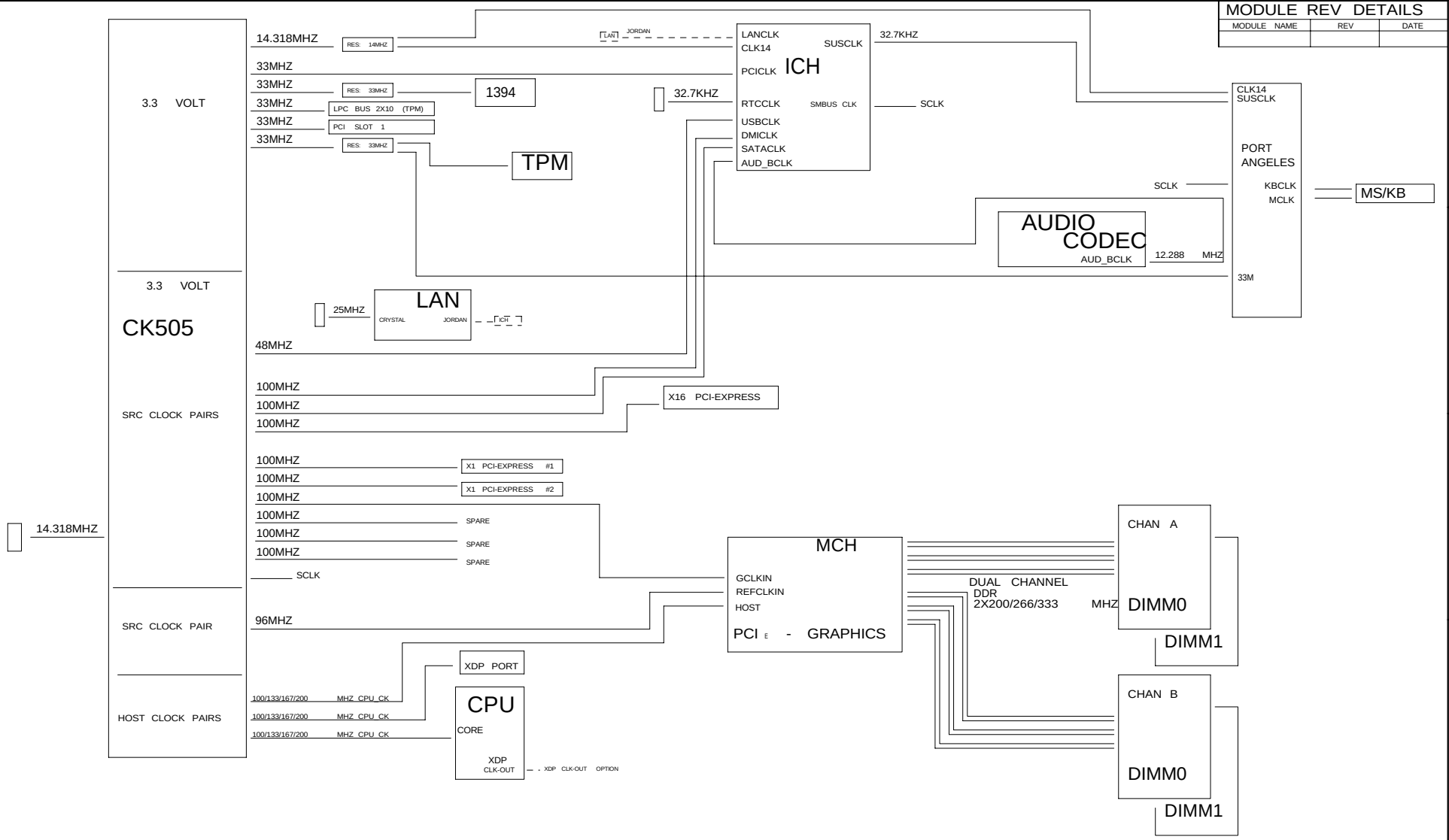
BPAGE DRAWING

frostburg_fabc.sch_1.3
Sun Mar 18 18:42:56 2007

[PAGE_TITLE=RESET MAP]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	3	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=CLOCK DISTRIBUTION]

CLOCK DISTRIBUTION UPDATED: 09/07/2005

BPAGE DRAWING
frostburg_fabc.sch_1.4
Sun Mar 18 18:42:56 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	4	3.01

ICH

GPIO SIGNALS NOT USED: GP40-47

PIN NAME	POWER WELL	USAGE	AFTER PLTRST	S3/S5	NOTES
GP[0]	MAIN (CORE)	FP AUD DETECT	IN		10K P/U TO VCC3
GP[1]	MAIN (CORE)	FRONT FAN TACH	IN		3.3K P/U TO +12V (THRU 15K)
GP[2]	MAIN (CORE)	P_INTE	IN		8.2K P/U TO VCC
GP[3]	MAIN (CORE)	P_INTF	IN		8.2K P/U TO VCC
GP[4]	MAIN (CORE)	P_INTG	IN		8.2K P/U TO VCC
GP[5]	MAIN (CORE)	P_INTH	IN		8.2K P/U TO VCC
GP[6]	MAIN (CORE)	REAR FAN TACH	IN		3.3K P/U TO +12V (THRU 15K)
GP[7]	MAIN (CORE)	EV FAN TACH	IN		3.3K P/U TO +12V (THRU 15K),10K VCC3
GP[8]	RESUME (STBY)	SATA/HOT-SWAP	IN		10K P/U TO V_3P3_STBY
GP[9]	RESUME (STBY)	WOL	OUT		100K P/D TO GND
GP[10]	RESUME (STBY)	NOT USED (RVP)	OUT		10K P/U TO V_3P3_STBY
GP[11]	RESUME (STBY)	PORT 80 LED	OUT(ALERT)		10K P/U TO V_3P3_STBY
GP[12]	RESUME (STBY)	BOARD ID 3	IN		10K P/U TO V_3P3_STBY, 10K P/D
GP[13]	RESUME (STBY)	LPC_SIO_PME	IN		10K P/U TO V_3P3_STBY
GP[14]	RESUME (STBY)	NOT USED (RVP)	IN		
GP[15]	RESUME (STBY)	LAN DISABLE	OUT		
GP[16]	MAIN (CORE)	BOARD ID 1	IN		10K P/U TO VCC3, 10K P/D
GP[17]	MAIN (CORE)	CPU FAN TACH	IN		3.3K P/U TO +12V (THRU 15K)
GP[18]	MAIN (CORE)	BOARD ID 2	IN		10K P/U TO VCC3, 10K P/D
GP[19]	MAIN (CORE)	SATA1GP	IN		10K P/U TO VCC3
GP[20]	MAIN (CORE)	NOT USED (TP): SATA HOTSWAP CTL	OUT		
GP[21]	MAIN (CORE)	SATA0GP	IN		10K P/U TO VCC3
GP[22]	MAIN (CORE)	NOT USED	IN		10K P/U TO VCC3
GP[23]	MAIN (CORE)	LDRQ1	OUT		10K P/U TO VCC3
GP[24]	RESUME (STBY)	V_SM LED CONTROL	OUT		1K P/U TO V_SM (THRU EMPTY 0 OHM RES)
GP[25]	RESUME (STBY)	BOARD ID 4	IN		10K P/U TO V_3P3_STBY, 10K P/D
GP[26]	RESUME (STBY)	S4_STATE	OUT		10K P/U TO V_3P3_STBY (EV DESIGN ONLY)
GP[27]	RESUME (STBY)	NOT USED (TP)	LOW		ENERGY LAKE STATUS LED: GREEN
GP[28]	RESUME (STBY)	NOT USED (TP)	LOW		ENERGY LAKE STATUS LED: YELLOW
GP[29]	RESUME (STBY)	OC5	IN		NOA SHARED WITH OVER-CURRENT
GP[30]	RESUME (STBY)	OC6	IN		NOA SHARED WITH OVER-CURRENT
GP[31]	RESUME (STBY)	OC7	IN		NOA SHARED WITH OVER-CURRENT
GP[32]	MAIN (CORE)	BOARD ID 0	IN		10K P/U TO VCC3, 10K P/D
GP[33]	MAIN (CORE)	MFG_MODE (RVP)	IN		4.7K P/U TO VCC3
GP[34]	MAIN (CORE)	ICH CFG JUMPER	IN		1K P/U TO VCC3 (SUITCASE JMPR); 4.7K P/D TO GND: BIOS NORMAL, RECOVER, CONFIGURE
GP[35]	MAIN (CORE)	NOT USED (TP)	IN		
GP[36]	MAIN (CORE)	SATA2GP	IN		10K P/U TO VCC3
GP[37]	MAIN (CORE)	SATA3GP	IN		10K P/U TO VCC3
GP[38]	MAIN (CORE)	NOT USED	IN		10K P/U TO VCC3
GP[39]	MAIN (CORE)	NOT USED	IN		10K P/D TO GND
GP[48]	MAIN (CORE)	NOT USED	IN		10K P/U TO VCC3
GP[49]	CPU	CPUPWRGD	IN		EMPTY 100 OHM P/U (VTT)

PORT ANGELES (BASED ON NATIONAL PA3.0, MAY 2004, REV 1.1; MULTI-PLEXED/PROGRAMMABLE GPIO PINS)

GPXX (PIN 103/118)	STBY/VCC3	NOT USED (TP)	I/O			
GPXX (PIN 104/119)	STBY/VCC3	1394 ENABLE	I/O			1K P/D TO GND
GPXX (PIN 105/120)	STBY/VCC3	NOT USED (TP)	I/O			
GPXX (PIN 106/121)	STBY/VCC3	1 WATT VREG CONTROL	I/O			
GPXX (PIN 108/124)	STBY/VCC3	1 WATT VREG CONTROL+	I/O			
GPXX (PIN 109/126)	STBY/VCC3	MEM. OVERVOLTAGE CONTROL1	I/O			10K EMPTY P/U TO V_3P3_STBY (1.8/1.9 VREG CTL)
GPXX (PIN 111/127)	STBY/VCC3	MEM. OVERVOLTAGE CONTROL2 (TP)	I/O			
GPXX (PIN 112/128)	STBY/VCC3	BOARD ID 5	I/O			
GPXX (PIN 116)	STBY	5V_DDCSDA	I/O			2.2K P/U TO VCC
GPXX (PIN 114)	STBY	5V_DDCSCL	I/O			2.2K P/U TO VCC
GPXX (PIN 74/115/122)	STBY/STBY/VCC3	3V_DDCSDA	I/O			2.2K P/U TO VCC3
GPXX (PIN 75/113/125)	STBY/STBY/VCC3	3V_DDCSCL	I/O			2.2K P/U TO VCC3
GPXX (PIN 101)	STBY	2X12 HDR DETECT	I/O			
GPXX (PIN 100)	STBY	NOT USED (TP)	I/O			
GPXX (PIN 102)	N/C (PA30)	NOT USED (PA30)	N/C (PA30)			

MULTI-PLEXED GPIO PINS ON PORT ANGELES WHICH ARE USED FOR SPECIFIC FUNCTIONS (NOT AS GPIO) ARE NOT IDENTIFIED HERE
UN-USED GPIO PINS ON PORT ANGELES ARE NOT IDENTIFIED HERE
TOTAL OF (33) POSSIBLE GPIO PINS ON PORT ANGELES (POWER WELL: STBY OR V_3P3_STBY = RESUME, VCC3 = MAIN).
NOTE: (0-4) GP'S FROM THE FWH WERE NOT USED (POWER WELL = CORE, INPUT ONLY)

MODULE REV DETAILS

MODULE NAME	REV	DATE

IRQ ROUTING TABLE (EXCERPT FROM ICH BIOS BKM REV 0.72)

	SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	AUDIO	LAN	USB1 2.0	USB2 2.0	PCI X1 #1	PCI X1 #2	PCI X1 #3	PCI X16 #1	PCI X16 #2	SMBUS
P_INTA*			IRQD		IRQC							B		A		
P_INTB*			IRQC			IRQA					A					
P_INTC*			IRQA	IRQB	IRQA					C			C			
P_INTD*			IRQB	IRQA												C
P_INTE*	IRQD	IRQC			IRQD	IRQB		A								
P_INTF*	IRQA	IRQB		IRQC		IRQD										
P_INTG*	IRQB	IRQA		IRQD		IRQC	A									
P_INTH*	IRQC	IRQD			IRQB				A							
REQ/GNT	0	1	2	3												
IDSEL	16	17	18	19	20	21		24								

SMBUS ADDRESS LINES SA [2-0]

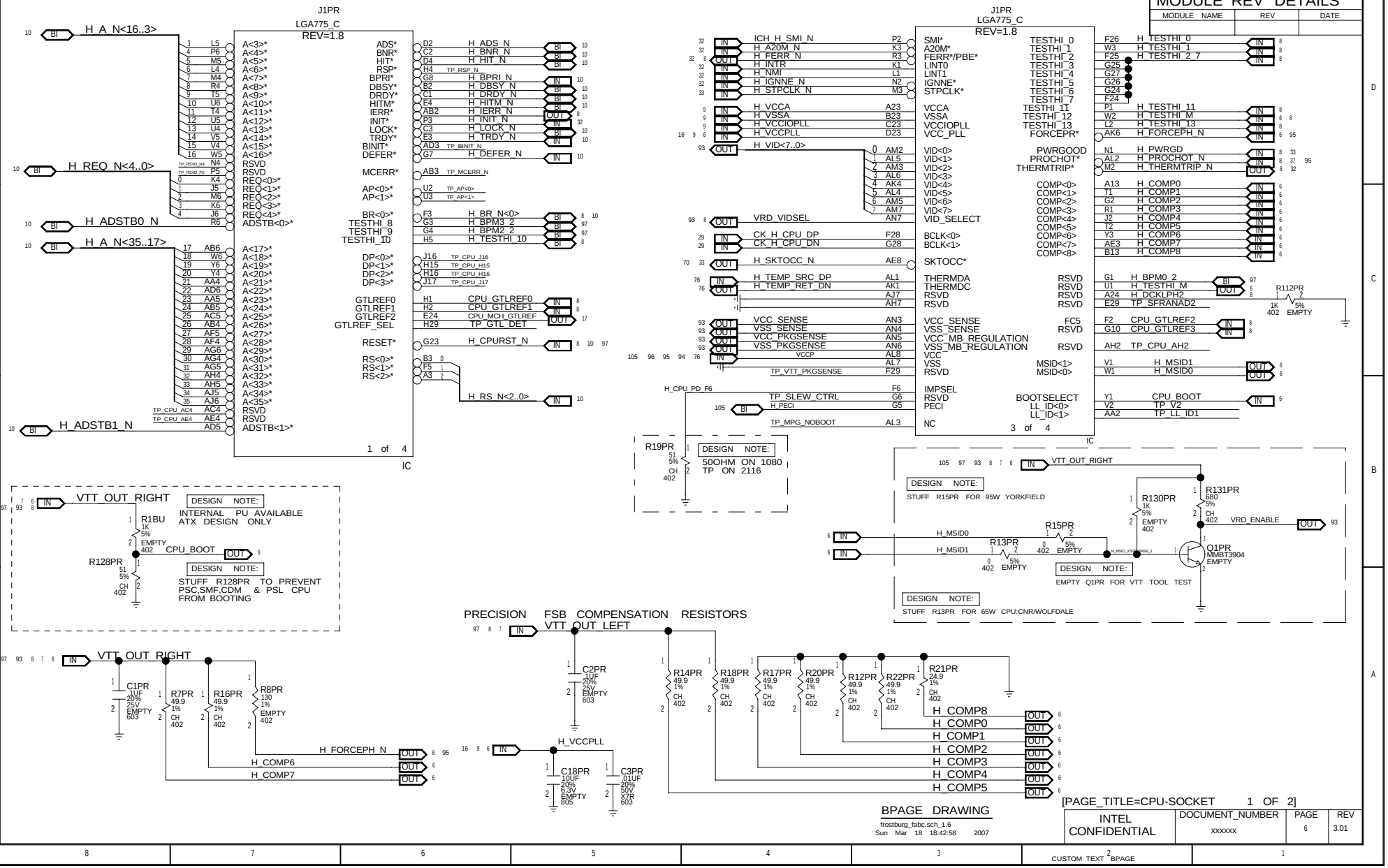
			SMBUS ADDRESS
MEMORY SLOT-0	(CHANNEL-A:	SLOT-0)	0 0 0 0A1H 0A0H
MEMORY SLOT-1	(CHANNEL-A:	SLOT-1)	0 0 1 0A3H 0A2H
MEMORY SLOT-2	(CHANNEL-B:	SLOT-0)	0 1 0 0A5H 0A4H
MEMORY SLOT-3	(CHANNEL-B:	SLOT-1)	0 1 1 0A7H0 A6H
CK410	- - -		0D3H 0D2H
DB800/DB400	- - -		0DDH 0DCH

SMBUS DATA (EXCERPT FROM ICH BIOS BKM REV 0.72)

[PAGE_TITLE=GPIO, IRQ, IDSEL MAP]

BPAGE DRAWING
frostburg_fabc.sch_1.5
Sun Mar 18 18:42:57 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	5	3.01


J1PR
LGA775_C
REV=1.8
H_A_N<16..3>
H_REQ_N<4..0>
H_ADSTB0_N
H_A_N<35..17>
H_ADSTB1_N
1 of 4
IC
J1PR
LGA775_C
REV=1.8
3 of 4
IC
MODULE REV DETAILS
MODULE NAME
REV
DATE
VTT_OUT_RIGHT
DESIGN NOTE:
INTERNAL PU AVAILABLE
ATX DESIGN ONLY
CPU_BOOT
R128PR
STUFF R128PR TO PREVENT PSC,SMF,CDM & PSL CPU FROM BOOTING
R19PR
50OHM ON 1080
TP ON 2116
STUFF R15PR FOR 95W YORKFIELD
STUFF R13PR FOR 65W CPU:CNR/WOLFDALE
EMPTY Q1PR FOR VTT TOOL TEST
VRD_ENABLE
PRECISION FSB COMPENSATION RESISTORS
VTT_OUT_LEFT
H_VCCPLL
H_FORCEPH_N
H_COMP6
H_COMP7
H_COMP8
H_COMP0
H_COMP1
H_COMP2
H_COMP3
H_COMP4
H_COMP5
BPAGE DRAWING
frostburg_fabc.sch_1.6
Sun Mar 18 18:42:58 2007
[PAGE_TITLE=CPU-SOCKET 1 OF 2]
INTEL CONFIDENTIAL
DOCUMENT_NUMBER
xxxxxx
PAGE
6
REV
3.01
CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS

MODULE NAME	REV	DATE

R124PR
39 93 IN VR_READY 1 0 402 2 5% CH H_VR_READY OUT 7

CAD NOTE:
PLACE CLOSE TO VR CONTROLLER

J1PR
LGA775_C
REV=1.8

97 IN	H_TCK	AE1	TCK	VTT	A29
97 IN	H_TDI	AD1	TDI	VTT	B25
97 OUT	H_TDO	AF1	TDO	VTT	B29
97 IN	H_TMS	AC1	TMS	VTT	B30
97 IN	H_TRST_N	AG1	TRST*	VTT	C29
				VTT	A26
97 BI	H_BPM_N<5..0>	0 AJ2	BPM<0>*	VTT	B27
		1 AJ1	BPM<1>*	VTT	C28
		2 AD2	BPM<2>*	VTT	A25
		3 AG2	BPM<3>*	VTT	A28
		4 AF2	BPM<4>*	VTT	A27
		5 AG3	BPM<5>*	VTT	C30
				VTT	A30
97 70 51 36 33 OUT	FP_RST_N	AC2	DBR*	VTT	C25
				VTT	C26
97 OUT	XDP_CLKOUT_DP	AK3	ITPCLK<0>	VTT	C27
97 OUT	XDP_CLKOUT_DN	AJ3	ITPCLK<1>	VTT	B26
				VTT	D27
28 13 8 OUT	H_FSBSEL0	G29	BSEL<0>	VTT	D28
28 13 8 OUT	H_FSBSEL1	H30	BSEL<1>	VTT	D25
28 13 8 OUT	H_FSBSEL2	G30	BSEL<2>	VTT	D26
				VTT	B28
				VTT	D29
CPU_N5		N5	RSVD	VTT	D30
97 BI H_BPM1_2		C9	RSVD	VTT_PWRGD	AM6
TP_CPU_E7		E7	RSVD		
TP_CPU_AE6		AE6	RSVD	VTT_OUT_RIGHT	AA1
				VTT_OUT_LEFT	J1
TP_CPU_D16		D16	RSVD	VTT_SEL	F27
TP_ACLKPH2		A20	RSVD		
TP_SFRANAC2		E23	RSVD		
				RSVD	F23 TP_EXTBGREF
				RSVD	D14 TP_SFRANAD
				RSVD	E6 TP_SFRANAC
				RSVD	E5 H_DCLKPH
				RSVD	J3 H_ACLKPH
				RSVD	D1 TP_HFPLL

4 of 4

V_FSB_VTT IN 8 9 14 17 34 38 85
H_VR_READY IN 7
VTT_OUT_RIGHT OUT 6 8 93 97 105
VTT_OUT_LEFT OUT 6 8 97
VTT_SEL OUT 85

C4PR 1UF 10% 16V X7R 603
C5PR 1UF 10% 16V X7R 603

R33PR 1K 5% EMPTY 402

DESIGN NOTE:
FOR DEBUG ONLY

R32PR 2 1 1K 5% EMPTY 402
R31PR 2 1 1K 5% EMPTY 402

DESIGN NOTE:
ENG FEATURE: 1K RES (EMPTY)

CAD NOTE:
PLACE A GND VIA NEAR TP ON PIN D1

J1PR
LGA775_C
REV=1.8

10 BI	H_D_N<15..0>	0 B4	D<0>*	D<32>*	G16 32
		1 C5	D<1>*	D<33>*	E15 33
		2 A4	D<2>*	D<34>*	E16 34
		3 C6	D<3>*	D<35>*	G18 35
		4 A5	D<4>*	D<36>*	G17 36
		5 B6	D<5>*	D<37>*	F17 37
		6 B7	D<6>*	D<38>*	F18 38
		7 A7	D<7>*	D<39>*	E18 39
		8 A10	D<8>*	D<40>*	E19 40
		9 A11	D<9>*	D<41>*	F20 41
		10 B10	D<10>*	D<42>*	E21 42
		11 C11	D<11>*	D<43>*	F21 43
		12 D8	D<12>*	D<44>*	G21 44
		13 B12	D<13>*	D<45>*	E22 45
		14 C12	D<14>*	D<46>*	D22 46
		15 D11	D<15>*	D<47>*	G22 47
10 BI	H_DBI_N<0>	A8	DBI<0>*	DBI<2>*	D19
10 BI	H_STBN_N<0>	C8	DSTBN<0>*	DSTBN<2>*	G20
10 BI	H_STBP_N<0>	B9	DSTBP<0>*	DSTBP<2>*	G19
10 BI	H_D_N<31..16>				
		16 G9	D<16>*	D<48>*	D20 48
		17 F8	D<17>*	D<49>*	D17 49
		18 F9	D<18>*	D<50>*	A14 50
		19 E9	D<19>*	D<51>*	C15 51
		20 D7	D<20>*	D<52>*	C14 52
		21 E10	D<21>*	D<53>*	B15 53
		22 D10	D<22>*	D<54>*	C18 54
		23 F11	D<23>*	D<55>*	B16 55
		24 F12	D<24>*	D<56>*	A17 56
		25 D13	D<25>*	D<57>*	B18 57
		26 E13	D<26>*	D<58>*	C21 58
		27 G13	D<27>*	D<59>*	B21 59
		28 F14	D<28>*	D<60>*	B19 60
		29 G14	D<29>*	D<61>*	A19 61
		30 F15	D<30>*	D<62>*	A22 62
		31 G15	D<31>*	D<63>*	B22 63
10 BI	H_DBI_N<1>	G11	DBI<1>*	DBI<3>*	C20
10 BI	H_STBN_N<1>	G12	DSTBN<1>*	DSTBN<3>*	A16
10 BI	H_STBP_N<1>	E12	DSTBP<1>*	DSTBP<3>*	C17

H_D_N<47..32> BI 10
H_DBI_N<2> BI 10
H_STBN_N<2> BI 10
H_STBP_N<2> BI 10
H_D_N<63..48> BI 10
H_DBI_N<3> BI 10
H_STBN_N<3> BI 10
H_STBP_N<3> BI 10

2 of 4

IC

VCCP=AG22,K29,AM26,AE12,AE11
VCCP=W23,W24,W25,T25,Y28,AL18,AC25,W30,Y30,AN14,AD28,Y26,AC29,M29,U24,J23,AC27,AM18,AM19,AB8
VCCP=AC26,J8,J28,T30,AM9,AF15,AC8,AE14,N23,W29,U29,AC24,AC23,Y23,AN26,AN25,AN11,AN18,Y27,Y25
VCCP=U27,AD24,AE23,AE22,AN19,V8,K8,AE21,AM30,AE19,AC30,AE15,M30,K27,M24,AN21,T8,AC28,N25,AE18,W26
VCCP=AD25,M8,N30,AD26,AJ26,AM29,M25,M26,L8,U25,Y8,AJ12,AD27,U23,M23,AG29,N27,AM22,U28,K28
VCCP=U8,AK18,AD8,K24,AH28,AH21,AK12,AH22,T29,AM14,AM25,AE9,Y29,AK25,AK19,AG15,J22,T24,AG21,AM21
VCCP=J25,U30,AL21,AG25,AJ18,J19,AH30,J15,AG12,AJ22,J20,AH18,AH26,W27,AL25,AN8,AH14,T23,R8
VCCP=AK22,AN29,AG11,AK26,J10,AJ15,AG26,AN9,AH15,AF18,AL15,J26,J18,J21,AG27,AK15,AF11,AD23,AM15,AF8
VCCP=AK21,AG30,AJ21,AM11,AL11,AJ11,K30,AL14,AN30,AH25,AL12,AJ9,AK11,AG14,N29,AL30,AJ25,AH9,J29,J11
VCCP=K25,P8,K23,AL19,AM8,T26,N28,AH12,AL22,AN15,AJ8,U26,AJ19,T27,AK8,AN12,AG9,N26,AF9,AF22
VCCP=AH11,AJ14,AH19,AH29,AH27,AG28,AL26,AM12,J24,J13,T28,W28,J12,J27,AG19,AL9,AD30,AF21,Y24,AK14
VCCP=J9,M7,AF14,J30,AG18,AA8,AG8,AL29,AD29,W8,AH8,N24,AN22,J14,K26,AF19,N8,AF12,M28,AK9
GND=C10,D12,C24,K2,C22,AN1,B14,K7,AE16,B11,AL10,AK23,H12,AF7,AK7
GND=H7,E14,L28,Y5,E11,AL16,AL24,AK13,D21,AL20,D18,AN2,AK16,AK20,AM27,AM1,AL13,AL17,C19
GND=E28,AK30,D24,AL23,A12,L25,J7,AE28,AE29,K5,J4,AE30,AN20,AF10,AE24,AM24,AN23,H9,H8
GND=H13,AC6,AC7,AH6,C16,AM16,AE25,AE27,AJ28,F19,AH13,AD7,AH16,AK17,E17,AH17,AH20,AE5,AH23
GND=AE7,AM13,AH24,AJ30,AJ10,AF3,AK5,AJ16,AF6,AK29,AJ17,F22,AH3,AK10,AM10,F16,AJ23,F13,AG7,F10
GND=L26,AD4,H11,L24,L23,AM23,A15,AH10,B24,L3,H27,A21,AE2,AJ29,AK27,AK28,B20,AM20
GND=H26,B17,H25,H24,AA3,AA7,H23,AA6,H10,H22,H21,H20,H19,H18,AB7,H17,AJ24,AM17,AC3,H14
GND=P28,V6,AK2,P27,P26,AM28,AJ13,W4,P25,AJ20,W7,P23,C7,L30,L29,D15,AL27,Y7,L27
GND=AA29,N6,N7,AA28,AN13,AA27,AA26,P4,AA25,AA24,P7,E26,V30,R2,V29,V28,R5,V27,R7,E20
GND=AN10,V25,T3,V24,V23,T6,E25,R29,R28,R27,R26,R25,U7,R24,R23,P30,V3,P29
GND=AF16,AE10,AF13,H6,A18,A2,E2,D9,C4,A6,D6,D5,A9,D3,B1,B5,B8,AJ4,AE26,AH1
GND=V7,C13,AK24,AB30,L6,L7,AB29,M1,AB28,AN17,AB27,AB26,AN16,M7,AB25,AB24,AB23,N3,AA30
GND=F4,AG10,AE13,AF30,H28,F7,AF29,AF28,AF27,AF26,AF25,AN28,AN27,AF24,AF23,AG24,AF17,AN24,H3
GND=Y2,P24,AE20,AE17,E27,T7,R30,AJ27,AB1,AM4,V26,AA23,AL28,AF20,AG23,AG20,E8,AG17,AG16,AG13

BPAGE DRAWING
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Sun Mar 18 18:42:59 2007

[PAGE_TITLE=CPU SOCKET 2 OF 2]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	7	3.01

CPU GTLREF

DESIGN NOTE:
GTLREF VOLTAGE SHOULD BE 0.67*VTT
(67% OF 1.2V) = 0.80V
<FOR THIS DESIGN>
100OHM OVER 200 OHM RESISTORS

VTT_OUT_RIGHT → R59PR 115 1% CH 402 → CPU_GTLREF0_DIVIDER → R63PR 10 402 5% CH → CPU_GTLREF0 → OUT
R65PR 200 1% CH 402
C9PR 1.0UF 20% 10V Y5V 603
C8PR 220PF 10% 50V EMPTY 402

DESIGN NOTE:
GTLREF VOLTAGE SHOULD BE 0.67*VTT
(67% OF 1.2V) = 0.80V
<FOR THIS DESIGN>
100OHM OVER 200 OHM RESISTORS

VTT_OUT_RIGHT → R60PR 115 1% CH 402 → CPU_GTLREF1_DIVIDER → R57PR 10 402 5% CH → CPU_GTLREF1 → OUT
R56PR 200 1% CH 402
C10PR 1.0UF 20% 10V Y5V 603
C7PR 220PF 10% 50V EMPTY 402

DESIGN NOTE:
PRODUCT MAY
TIE GTLREFS
TOGETHER

CPU_GTLREF1 → R62PR 0 402 5% EMPTY → CPU_GTLREF0

DESIGN NOTE:
GTLREF VOLTAGE SHOULD BE 0.67*VTT
(67% OF 1.2V) = 0.80V
<FOR THIS DESIGN>
100OHM OVER 200 OHM RESISTORS

VTT_OUT_LEFT → R114PR 115 1% CH 402 → CPU_GTLREF2_DIVIDER → R116PR 10 402 5% CH → CPU_GTLREF2 → OUT
R115PR 200 1% CH 402
C14PR 1.0UF 20% 10V Y5V 603
C15PR 220PF 10% 50V EMPTY 402

DESIGN NOTE:
GTLREF VOLTAGE SHOULD BE 0.67*VTT
(67% OF 1.2V) = 0.80V
<FOR THIS DESIGN>
100OHM OVER 200 OHM RESISTORS

VTT_OUT_LEFT → R117PR 115 1% CH 402 → CPU_GTLREF3_DIVIDER → R119PR 10 402 5% CH → CPU_GTLREF3 → OUT
R118PR 200 1% CH 402
C16PR 1.0UF 20% 10V Y5V 603
C17PR 220PF 10% 50V EMPTY 402

DESIGN NOTE:
PRODUCT MAY
TIE GTLREFS
TOGETHER

DESIGN NOTE:
KF CPU GTLREF: DEFAULT EMPTY

FSB SELECTS

V_FSB_VTT → R67PR 470 402 5% CH → H_FSBSEL0 → OUT
R68PR 470 402 5% CH → H_FSBSEL1 → OUT
R69PR 470 402 5% CH → H_FSBSEL2 → OUT

CPU SIGNAL TERMINATION

CAD NOTE:
PLACE AT CPU END OF ROUTE

VTT_OUT_RIGHT
VTT_OUT_LEFT
R55PR 62 5% CH 402
R52PR 100 5% EMPTY 402
R51PR 62 5% CH 402
R75PR 680 5% CH 402
R76PR 330 5% CH 402
R66PR 130 1% EMPTY 402

CAD NOTE:
PLACE AT ICH END OF ROUTE

V_FSB_VTT
R71PR 62 5% CH 402
R72PR 62 5% CH 402

H_THERMTRIP_N → OUT
H_FERR_N → OUT
H_PROCHOT_N → OUT
VR_READY → IN
VRD_VIDSEL → OUT
H_CPURST_N → OUT
H_PWRGD → OUT
H_BR_N<0> → OUT

TESTHI PULLUPS

V_FSB_VTT
VTT_OUT_RIGHT
VTT_OUT_LEFT
R54PR 51 5% CH 402
R49PR 51 5% CH 402
R53PR 51 5% CH 402
R64PR 51 5% CH 402
R50PR 51 5% CH 402
R48PR 62 5% CH 402
R70PR 51 5% CH 402
R35PR 51 5% CH 402

TESTHI PIN NAME MAPPING	
TESTHI[0]	BYPASSEN
TESTHI[1]	ODT
TESTHI[5:2]	MCLK[3:0]
TESTHI[7:6]	MCLKIO[1:0]
TESTHI[10:8]	BR#[3:1]
TESTHI[11]	DPSLP#
TESTHI[12]	DT_SVR#
TESTHI[13]	SLP#

DESIGN NOTE:
CHANGE TO H_TESTHI_2-7
FOR CRB

H_TESTHI_0 → OUT
H_TESTHI_2_7 → OUT
H_IERR_N → OUT
H_TESTHI_1 → OUT
H_TESTHI_10 → OUT
H_TESTHI_11 → OUT
H_TESTHI_M → OUT
H_TESTHI_13 → OUT

MODULE REV DETAILS

MODULE NAME	REV	DATE

[PAGE_TITLE=CPU TERMINATION & MISC P/U P/D]
BPAGE DRAWING
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Sun Mar 18 18:43:01 2007

PLL SUPPLY FILTER

MODULE REV DETAILS		
MODULE NAME	REV	DATE

VCCPLL SUPPLY

V_SFR_OUT → R90PR (0 603 1A CH) → H_VCCPLL

DESIGN NOTE: DO NOT STUFF BOTH R90PR, R87PR

DESIGN NOTE: COST REDUCTION EXP

V_1P5_ICH → R87PR (0 603 1A EMPTY)

V_FSB_VTT

V_FSB_VTT → 693286-014 FB1PR EMPTY → 10UH L1PR EMPTY 721891-026

DESIGN NOTE: INDUCTOR: 125 MA 0805 PACKAGE

H_VCCIOPLL

DESIGN NOTE: COST REDUX EXPERIMENT EMPTY ONE INDUCTOR TO EVALUATE

R86PR 0 5% EMPTY 402

C11PR 1.0UF 20% 10V EMPTY 603

V_FSB_VTT

V_FSB_VTT → 10UH L3PR EMPTY 721891-026

693286-014 FB2PR EMPTY → 10UH L2PR EMPTY 721891-026

DESIGN NOTE: INDUCTOR: 125 MA 0805 PACKAGE

DESIGN NOTE: L3PR: DUAL CORE SUPPORT

H_VCCA

C13PR 33UF 20% 25V EMPTY RDL

C12PR 1.0UF 20% 10V EMPTY 603

H_VSSA

CAD NOTE:

PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12 MIL

VCC3

V_3P3_STBY\G → R146PR 10K 5% EMPTY 402

R139PR 1K 5% EMPTY 402

R140PR 1K 5% EMPTY 402

V_3P3_STBY\G → R145PR 10K 5% EMPTY 402

GTLREF_FET0 OUT

GTLREF_FET1 OUT

Q4PR MBT3904DUAL EMPTY

SIO_PIN_108 → R137PR 1K 5% EMPTY 402 → SIO_PIN_108_R

SIO_PIN_106_R → R138PR 1K 5% EMPTY 402 → SIO_PIN_106

DESIGN NOTE: PULL UP FOR PIN 106 IS AVAILABLE ON SIO PAGE

Q3PR BSS138N

CPU_GTLREF0_DIVIDER_R → R142PR 0 402 5% EMPTY → CPU_GTLREF0_DIVIDER OUT

GTLREF_FET0 → Q3PR BSS138N EMPTY

GTLREF_FET0_Q → R143PR 1.3K 1% EMPTY 402

CAD NOTE: PLACE CLOSE TO THE GTLREF DIVIDER

Q2PR BSS138N

CPU_GTLREF1_DIVIDER_R → R141PR 0 402 5% EMPTY → CPU_GTLREF1_DIVIDER OUT

GTLREF_FET1 → Q2PR BSS138N EMPTY

GTLREF_FET1_Q → R144PR 576 1% EMPTY 402

CAD NOTE: PLACE CLOSE TO THE GTLREF DIVIDER

[PAGE_TITLE=CPU PLL FILTERED SUPPLY]

BPAGE DRAWING
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Sun Mar 18 18:43:02 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	9	3.01

CUSTOM TEXT 2 BPAGE

U1UB
BRLK_B
REV=1

PCIE

EXP_A_RX_0_DP	F13	PEG_RXP_0	PEG_TXP_0	D11	EXP_A_TX_0_DP
EXP_A_RX_0_DN	E13	PEG_RXN_0	PEG_TXN_0	D12	EXP_A_TX_0_DN
EXP_A_RX_1_DP	K15	PEG_RXP_1	PEG_TXP_1	B11	EXP_A_TX_1_DP
EXP_A_RX_1_DN	J15	PEG_RXN_1	PEG_TXN_1	A10	EXP_A_TX_1_DN
EXP_A_RX_2_DP	F12	PEG_RXP_2	PEG_TXP_2	C10	EXP_A_TX_2_DP
EXP_A_RX_2_DN	E12	PEG_RXN_2	PEG_TXN_2	D9	EXP_A_TX_2_DN
EXP_A_RX_3_DP	J12	PEG_RXP_3	PEG_TXP_3	B9	EXP_A_TX_3_DP
EXP_A_RX_3_DN	H12	PEG_RXN_3	PEG_TXN_3	B7	EXP_A_TX_3_DN
EXP_A_RX_4_DP	J11	PEG_RXP_4	PEG_TXP_4	D7	EXP_A_TX_4_DP
EXP_A_RX_4_DN	H11	PEG_RXN_4	PEG_TXN_4	D6	EXP_A_TX_4_DN
EXP_A_RX_5_DP	F7	PEG_RXP_5	PEG_TXP_5	B5	EXP_A_TX_5_DP
EXP_A_RX_5_DN	E7	PEG_RXN_5	PEG_TXN_5	B6	EXP_A_TX_5_DN
EXP_A_RX_6_DP	E5	PEG_RXP_6	PEG_TXP_6	B3	EXP_A_TX_6_DP
EXP_A_RX_6_DN	F6	PEG_RXN_6	PEG_TXN_6	B4	EXP_A_TX_6_DN
EXP_A_RX_7_DP	C2	PEG_RXP_7	PEG_TXP_7	F2	EXP_A_TX_7_DP
EXP_A_RX_7_DN	D2	PEG_RXN_7	PEG_TXN_7	E2	EXP_A_TX_7_DN
EXP_A_RX_8_DP	G6	PEG_RXP_8	PEG_TXP_8	F4	EXP_A_TX_8_DP
EXP_A_RX_8_DN	G5	PEG_RXN_8	PEG_TXN_8	G4	EXP_A_TX_8_DN
EXP_A_RX_9_DP	L9	PEG_RXP_9	PEG_TXP_9	J4	EXP_A_TX_9_DP
EXP_A_RX_9_DN	L8	PEG_RXN_9	PEG_TXN_9	K3	EXP_A_TX_9_DN
EXP_A_RX_10_DP	M8	PEG_RXP_10	PEG_TXP_10	L2	EXP_A_TX_10_DP
EXP_A_RX_10_DN	M9	PEG_RXN_10	PEG_TXN_10	K1	EXP_A_TX_10_DN
EXP_A_RX_11_DP	M4	PEG_RXP_11	PEG_TXP_11	N2	EXP_A_TX_11_DP
EXP_A_RX_11_DN	L4	PEG_RXN_11	PEG_TXN_11	M2	EXP_A_TX_11_DN
EXP_A_RX_12_DP	M5	PEG_RXP_12	PEG_TXP_12	P3	EXP_A_TX_12_DP
EXP_A_RX_12_DN	M6	PEG_RXN_12	PEG_TXN_12	N4	EXP_A_TX_12_DN
EXP_A_RX_13_DP	R9	PEG_RXP_13	PEG_TXP_13	R2	EXP_A_TX_13_DP
EXP_A_RX_13_DN	R10	PEG_RXN_13	PEG_TXN_13	P1	EXP_A_TX_13_DN
EXP_A_RX_14_DP	T4	PEG_RXP_14	PEG_TXP_14	U2	EXP_A_TX_14_DP
EXP_A_RX_14_DN	R4	PEG_RXN_14	PEG_TXN_14	T2	EXP_A_TX_14_DN
EXP_A_RX_15_DP	R6	PEG_RXP_15	PEG_TXP_15	V3	EXP_A_TX_15_DP
EXP_A_RX_15_DN	R7	PEG_RXN_15	PEG_TXN_15	U4	EXP_A_TX_15_DN

DMI

DMI_IT_MR_0_DP	W2	DMI_RXP_0	DMI_TXP_0	V7	DMI_MT_IR_0_DP
DMI_IT_MR_0_DN	V1	DMI_RXN_0	DMI_TXN_0	V6	DMI_MT_IR_0_DN
DMI_IT_MR_1_DP	Y8	DMI_RXP_1	DMI_TXP_1	W4	DMI_MT_IR_1_DP
DMI_IT_MR_1_DN	Y9	DMI_RXN_1	DMI_TXN_1	Y4	DMI_MT_IR_1_DN
DMI_IT_MR_2_DP	AA7	DMI_RXP_2	DMI_TXP_2	AC8	DMI_MT_IR_2_DP
DMI_IT_MR_2_DN	AA6	DMI_RXN_2	DMI_TXN_2	AC9	DMI_MT_IR_2_DN
DMI_IT_MR_3_DP	AB3	DMI_RXP_3	DMI_TXP_3	Y2	DMI_MT_IR_3_DP
DMI_IT_MR_3_DN	AA4	DMI_RXN_3	DMI_TXN_3	AA2	DMI_MT_IR_3_DN

CK_PE_100M_MCH_DP	B12	EXP_CLKINP	EXP_COMPO	AC11	GRCOMP
CK_PE_100M_MCH_DN	B13	EXP_CLKINN	EXP_COMPI	AC12	
SDVO_CTRL_DATA	G17	SDVO_CTRLDATA			
SDVO_CTRL_CLK	E17	SDVO_CTRLCLK			

2 OF 8

IC

CAD NOTE:

MCH COMP0/1 SIGNALS: TIE TOGETHER AT PINS.

SIGNAL NAMING CONVENTION

EXP: PCI EXPRESS

DMI: DIRECT MEDIA INTERFACE

ITP: ICH TRANSMIT POSITIVE

ITN: ICH TRANSMIT NEGATIVE

IRP: ICH RECEIVE POSITIVE

IRN: ICH RECEIVE NEGATIVE

MTP: MCH TRANSMIT POSITIVE

MTN: MCH TRANSMIT NEGATIVE

MRP: MCH RECEIVE POSITIVE

MRN: MCH RECEIVE NEGATIVE

SDVO CTRL DATA

1	SDVO CARD PRESENT, PEG DISABLED
0	SDVO DISABLED (DEFAULT)

J3UB — NC — HDR — C85576-001

J2UB — NC — HDR

J9UB — NC — HDR

J7UB — NC — HDR

HS1UB
BRDWTR_ATX_HS
NC_1, NC_2, NC_3, NC_4, NC_5, NC_6, NC_7, NC_8
HEATSINK

U1UB
BRLK_B
REV=1

FSB

H_A_N<35..3>

J42	FSB_AB_3	FSB_DB_0	R40
L39	FSB_AB_4	FSB_DB_1	R41
J40	FSB_AB_5	FSB_DB_2	R41
L37	FSB_AB_6	FSB_DB_3	N40
L36	FSB_AB_7	FSB_DB_4	R42
K42	FSB_AB_8	FSB_DB_5	M39
N32	FSB_AB_9	FSB_DB_6	N41
N34	FSB_AB_10	FSB_DB_7	N42
M38	FSB_AB_11	FSB_DB_8	L41
N37	FSB_AB_12	FSB_DB_9	J39
M36	FSB_AB_13	FSB_DB_10	L42
R34	FSB_AB_14	FSB_DB_11	J41
N35	FSB_AB_15	FSB_DB_12	K41
N38	FSB_AB_16	FSB_DB_13	G40
U37	FSB_AB_17	FSB_DB_14	F41
N39	FSB_AB_18	FSB_DB_15	F42
R37	FSB_AB_19	FSB_DB_16	C42
P42	FSB_AB_20	FSB_DB_17	D41
R39	FSB_AB_21	FSB_DB_18	E38
V36	FSB_AB_22	FSB_DB_19	G37
R38	FSB_AB_23	FSB_DB_20	E42
U36	FSB_AB_24	FSB_DB_21	E39
U33	FSB_AB_25	FSB_DB_22	E37
R35	FSB_AB_26	FSB_DB_23	C39
V33	FSB_AB_27	FSB_DB_24	B39
V35	FSB_AB_28	FSB_DB_25	C33
Y34	FSB_AB_29	FSB_DB_26	A37
V42	FSB_AB_30	FSB_DB_27	F33
V38	FSB_AB_31	FSB_DB_28	E35
Y36	FSB_AB_32	FSB_DB_29	K32
Y38	FSB_AB_33	FSB_DB_30	H32
Y39	FSB_AB_34	FSB_DB_31	B34
AA37	FSB_AB_35	FSB_DB_32	J31
		FSB_DB_33	F32
		FSB_DB_34	M31
		FSB_DB_35	E31
		FSB_DB_36	K31
		FSB_DB_37	G31
		FSB_DB_38	K29
		FSB_DB_39	F31
		FSB_DB_40	J29
		FSB_DB_41	F29
		FSB_DB_42	L27
		FSB_DB_43	K27
		FSB_DB_44	H26
		FSB_DB_45	L26
		FSB_DB_46	J26
		FSB_DB_47	M26
		FSB_DB_48	C33
		FSB_DB_49	D35
		FSB_DB_50	E41
		FSB_DB_51	B41
		FSB_DB_52	D42
		FSB_DB_53	C40
		FSB_DB_54	C35
		FSB_DB_55	B40
		FSB_DB_56	D38
		FSB_DB_57	D37
		FSB_DB_58	B33
		FSB_DB_59	D33
		FSB_DB_60	C34
		FSB_DB_61	B35
		FSB_DB_62	A32
		FSB_DB_63	D32

H_D_N<63..0>

H_REQ_N<4..0>

F40	FSB_REQB_0
L35	FSB_REQB_1
L38	FSB_REQB_2
G43	FSB_REQB_3
J37	FSB_REQB_4

H_ADSTB0_N	M34	FSB_ADSTBB_0
H_ADSTB1_N	U34	FSB_ADSTBB_1

H_STBP_N<0>	M42	FSB_DSTBPB_0
H_STBN_N<0>	M43	FSB_DSTBNB_0
H_DBI_N<0>	M40	FSB_DINVB_0
H_STBP_N<1>	G35	FSB_DSTBPB_1
H_STBN_N<1>	H33	FSB_DSTBNB_1
H_DBI_N<1>	J33	FSB_DINVB_1
H_STBP_N<2>	G27	FSB_DSTBPB_2
H_STBN_N<2>	H27	FSB_DSTBNB_2
H_DBI_N<2>	G29	FSB_DINVB_2
H_STBP_N<3>	B38	FSB_DSTBPB_3
H_STBN_N<3>	C38	FSB_DSTBNB_3
H_DBI_N<3>	E33	FSB_DINVB_3

H_ADS_N	W40	FSB_ADSB
H_TRDY_N	Y40	FSB_TRDYB
H_DRDY_N	W41	FSB_DRDYB
H_DEFER_N	T43	FSB_DEFERB
H_HITM_N	Y43	FSB_HITMB
H_HIT_N	U42	FSB_HITB
H_LOCK_N	V41	FSB_LOCKB
H_BR_N<0>	AA42	FSB_BREQOB
H_BNR_N	W42	FSB_BNRB
H_BPRI_N	G39	FSB_BPRIB
H_DBSY_N	U40	FSB_DBSYB

	U41	FSB_RSB_0
H_RS_N<2..0>	AA41	FSB_RSB_1
	U39	FSB_RSB_2
H_CPURST_N	C31	FSB_CPURSTB

1 OF 8

FSB_SWING	B25	HXSWING
FSB_RCOMP	D23	HXRCOMP
FSB_SCOMP	C25	HXSCOMP
FSB_SCOMPB	D25	HXSCOMPB
FSB_DVREF	D24	MCH_GTLREF
FSB_ACCVREF	B24	
HPL_CLKINP	R32	CK_H_MCH_DP
HPL_CLKINN	U32	CK_H_MCH_DN

IC

DESIGN NOTE:

MCH GTLREF0/1: SEPARATE SIGNALS ON EV ONLY; TIE TOGETHER AT PINS ON CRB.

MODULE REV DETAILS

MODULE NAME	REV	DATE

BPAGE DRAWING

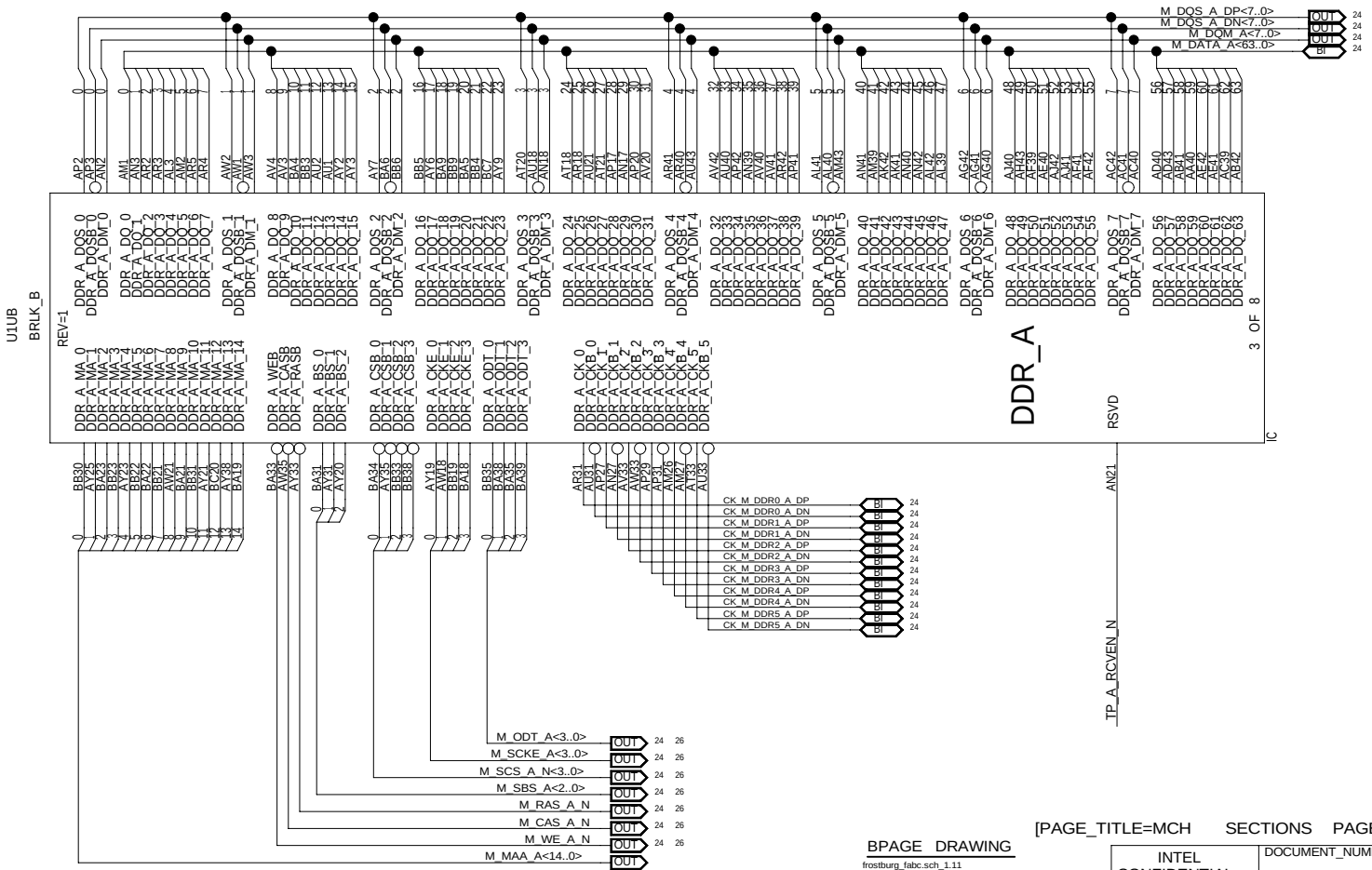
frostburg_fabc.sch_1.10
Sun Mar 18 18:43:03 2007

[PAGE_TITLE=MCH SECTIONS PAGE 1 OF 6]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	10	3.01

CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



BPAGE DRAWING

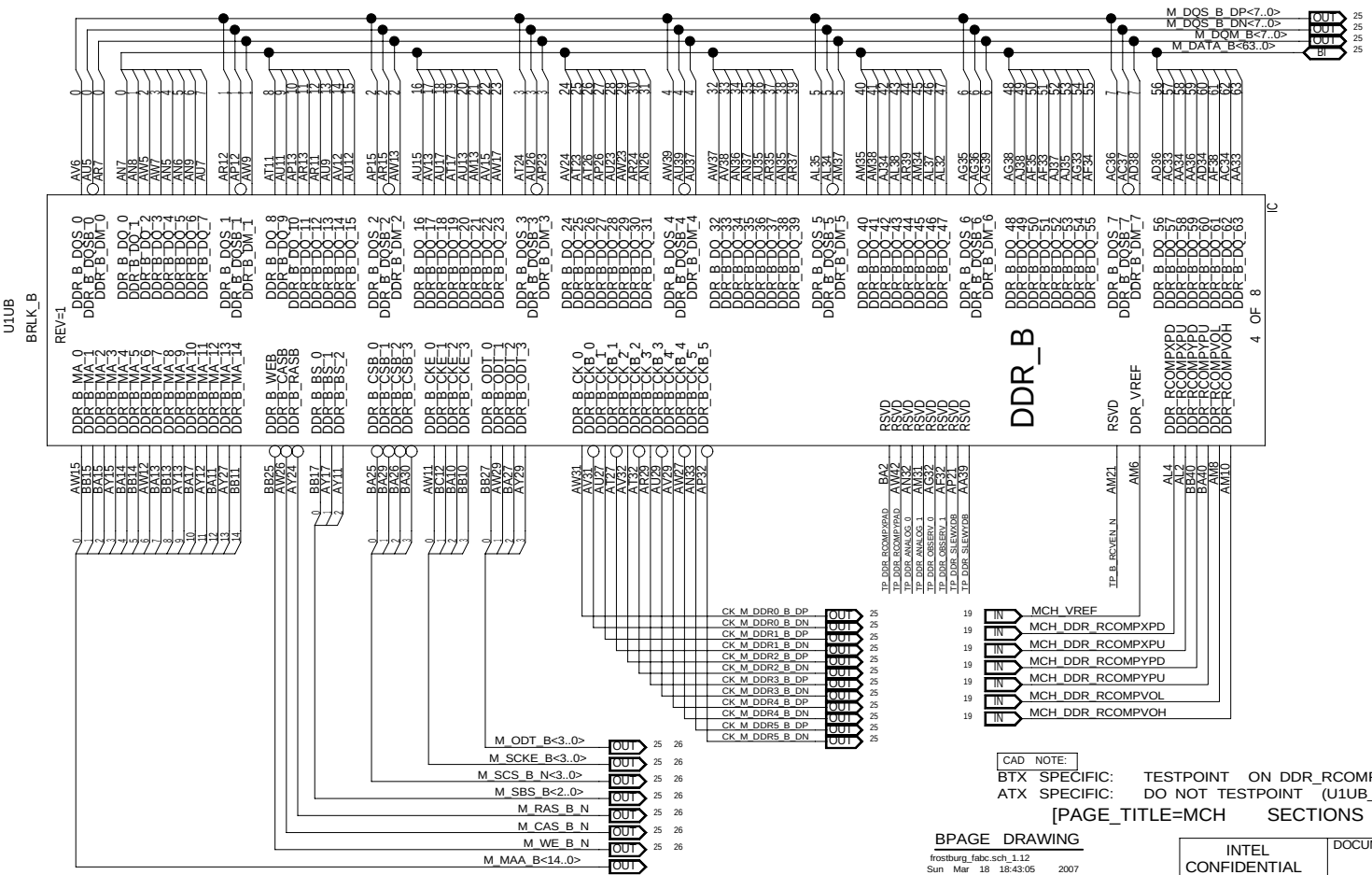
frostburg_fabc.sch_1.11
Sun Mar 18 18:43:04 2007

[PAGE_TITLE=MCH SECTIONS PAGE 2 OF 6]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	11	3.01

CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



CAD NOTE:

BTX SPECIFIC: TESTPOINT ON DDR_RCOMPY_PAD (U1UB)

ATX SPECIFIC: DO NOT TESTPOINT (U1UB_PIN AW42)

[PAGE_TITLE=MCH SECTIONS PAGE 3 OF 6]

BPAGE DRAWING

frostburg_fabc.sch_1.12
Sun Mar 18 18:43:05 2007

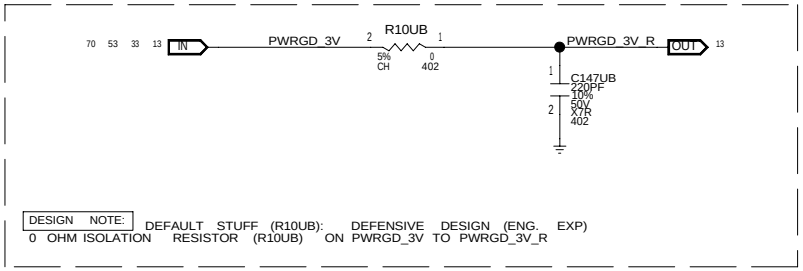
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	12	3.01

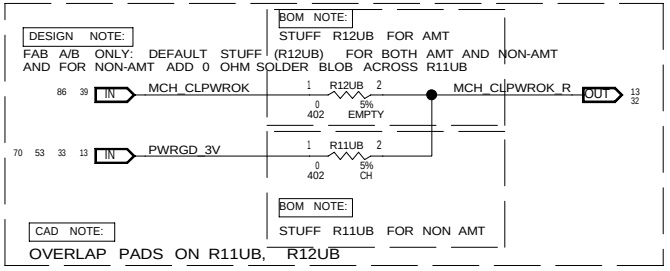
CUSTOM TEXT BPAGE

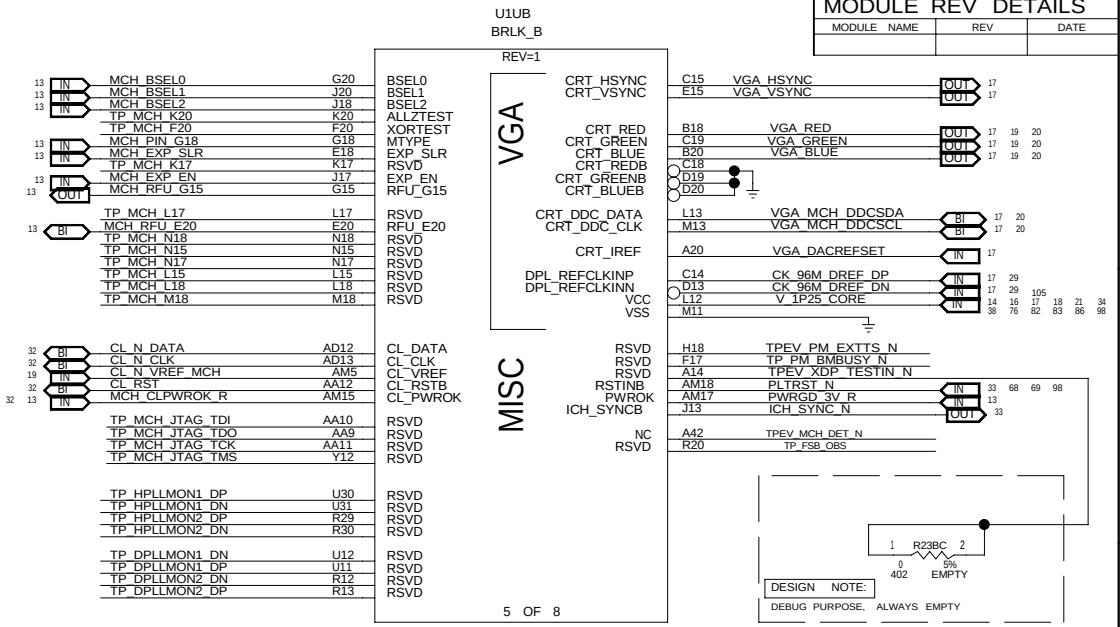
MODULE REV DETAILS

MODULE NAME	REV	DATE

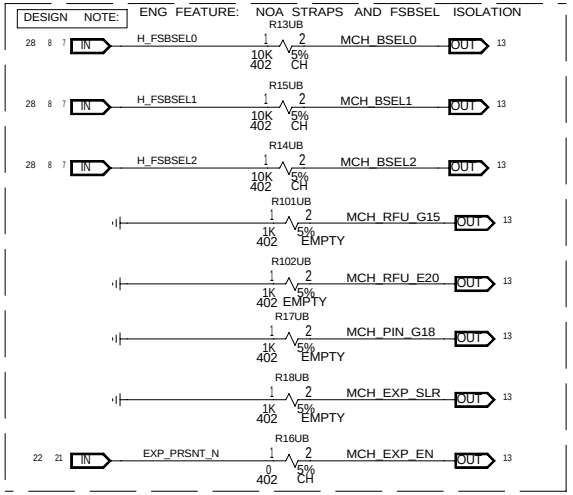
U1UB
BRLK_B
REV=1







IC



NOA	H	L	DESCRIPTION
0	SEE BSEL TABLE		BSEL0
1	SEE BSEL TABLE		BSEL1
2	SEE BSEL TABLE		BSEL2
4:3	SEE DFT MODE TABLE		DFT MODE
5	DDR2	DDR3	MEMORY TYPE
6	NORM	REVERSE	PCI-EXPRESS LANE REVERSAL
7	DISABLE	ENABLE	FSB HARDWARE STRAPS
8	CONCURRENT	NON-CONCURRENT	PCI-E / SDVO CO-EXISTENCE
9	DISABLE	ENABLE	ITPM HOST INTERFACE
11	ENABLE	DISABLE	ME CRYPTO

3,4,5,6,7,8,9 ALL HAVE INTERNAL PULL-UPS

BSEL TABLE

2	1	0	PSB FREQUENCY
0	0	0	267 MHZ (1067)
0	0	1	133 MHZ (533)
0	1	0	200 MHZ (800)
0	1	1	167 MHZ (133)
1	0	0	333 MHZ (1333)
1	0	1	100 MHZ (133)
1	1	0	400 MHZ (RSVD)
1	1	1	533 MHZ (133)

[PAGE_TITLE=MCH SECTIONS PAGE 4 OF 6]

BPAGE DRAWING
frostburg_fabc.sch_1.13
Sun Mar 18 18:43:08 2007

U1UB
BRLK_B
REV=1

POWER

V_1P25_CORE
V_1P25_CL_MCH
V_FSB_VTT
V_SM
V_1P25_PCIEXPRESS

BRLK_B

POWER

MODULE REV DETAILS

MODULE NAME	REV	DATE

CAD NOTE:
PLACE BACKSIDE RESISTOR R19BC CLOSE TO MCH BALL/PIN

R19BC 0 1A EMPTY 603

DESIGN NOTE:
ENG FEATURE: 0 OHM RES R19BC (EMPTY)

C7BC .1UF 10% 16V EMPTY 603

CAD NOTE:
PLACE CAPS AND MULTI-SITE CLOSE TO MCH BALLS FOR V_CKDDR

M1UB MULTI
V_CKDDR
C3UB .1UF 20% 25V Y5V 603
C2UB 22UF 20% 6.3V X5R 805
R94UB 402 5% CH
R95UB 402 5% CH

BOM NOTE:
DEFAULT: MULTI SITE M1UB TO USE 721891-022 (1UH INDUCTOR)

DESIGN NOTE:
FOR CRB, TIE THIS PIN TO VSS
EV: CONNECT TO EVMC OR VREG (TBD)

BOM NOTE:
DEFAULT (M22UB): 1 OHM 0402 5%
OPTION (M22UB): 600 OHM FB (A51464-006)

DESIGN NOTE:
EMPTY M22UB FOR NON-GRAPHIC SKU'S

M22UB MULTI CH 402

DESIGN NOTE:
STUFF R92UB FOR NON-GRAPHIC SKU'S

R92UB 0 402 5% EMPTY

BOM NOTE:
DEFAULT (M24UB): 1 OHM 0402 5%
OPTION (M24UB): 600 OHM FB (A51464-006)

M24UB MULTI CH 402

DESIGN NOTE:
ETCH R22BC 0OHM SM
ENG FEATURE: R22BC

BPAGE DRAWING
frostburg_fabc.sch 14
Sun Mar 18 18:43:09 2007

[PAGE_TITLE=MCH SECTIONS PAGE 5 OF 6]

U1UB
BRLK_B
REV=1

GND

7 OF 8

U1UB
BRLK_B
REV=1

GND

IC

U1UB
BRLK_B
REV=1

DDR3

DDR3_DRAMRSTB
DDR3_DRAM_PWROK

DDR3_A_CSB1
DDR3_A_MA0
DDR3_A_WEB
DDR3_B_ODT3

NC

TEST0
TEST1
TEST2

8 OF 8

IC

BC16	TP_DDR_DRAMRST	
AN15	DRAM_PWROK_DDR3	
AY37	DDR3_SCS_A_N1	
BB29	DDR3_MAA_A0	
BB34	DDR3_WE_A_N	
AW32	DDR3_B_ODT_B3	
BC43	TP_CGC_NCTF_BC43	
BC1	TP_CGC_NCTF_BC1	
A43	TP_CGC_NCTF_A43	

DESIGN NOTE:
NO TESTPOINT NEEDED ON DDR2 SKEW

R109UB
0
5%
CH
402

DESIGN NOTE:
DDR2 BOARDS,STUFF R109UB= 0OHM

MODULE REV DETAILS

MODULE NAME	REV	DATE

[PAGE_TITLE=MCH SECTIONS PAGE 6 OF 6]

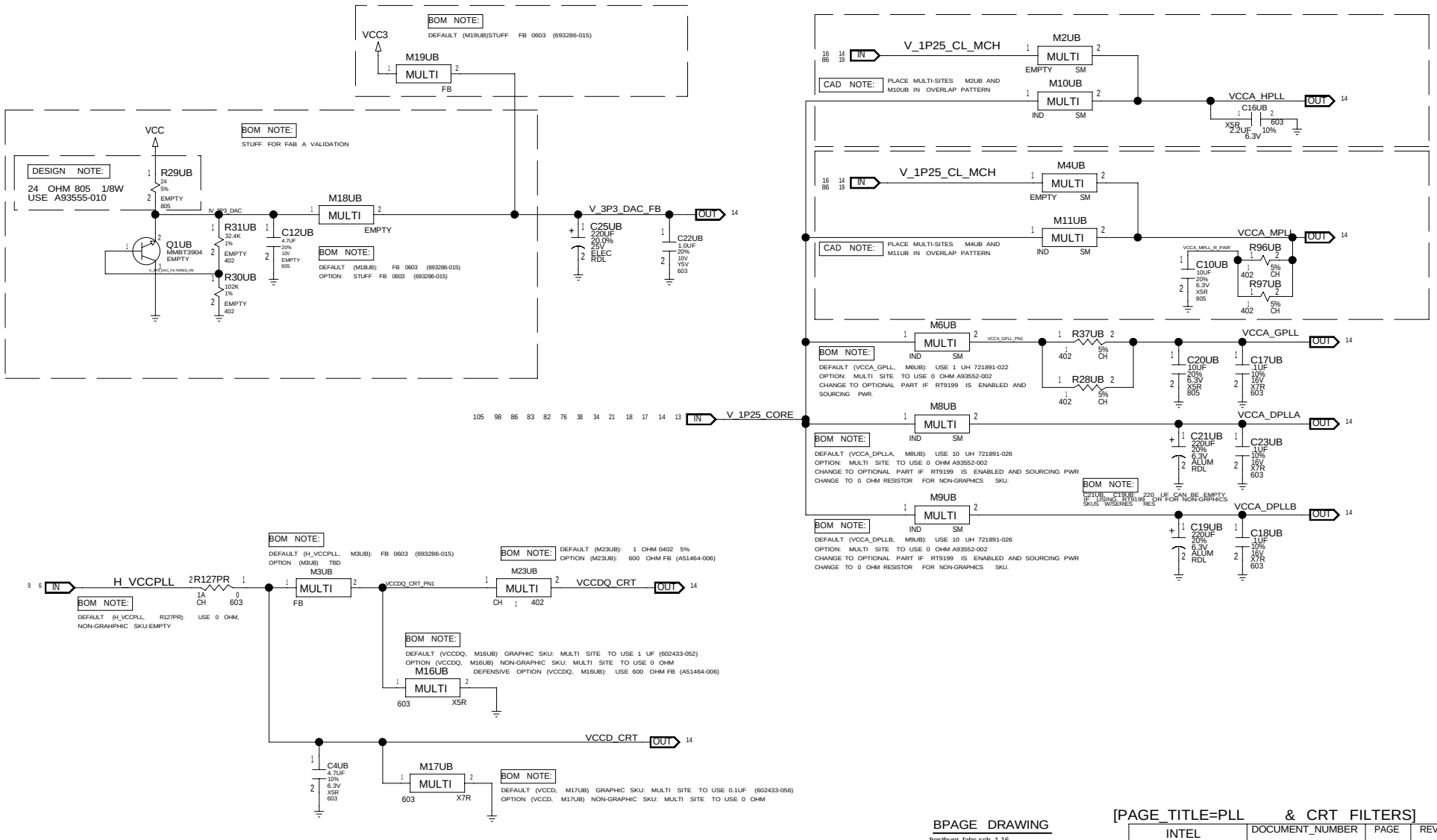
BPAGE DRAWING
frostburg_fabc.sch_1.15
Sun Mar 18 18:43:10 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	15	3.01

CUSTOM TEXT BPAGE

MODULE REV DETAILS

MODULE NAME	REV	DATE

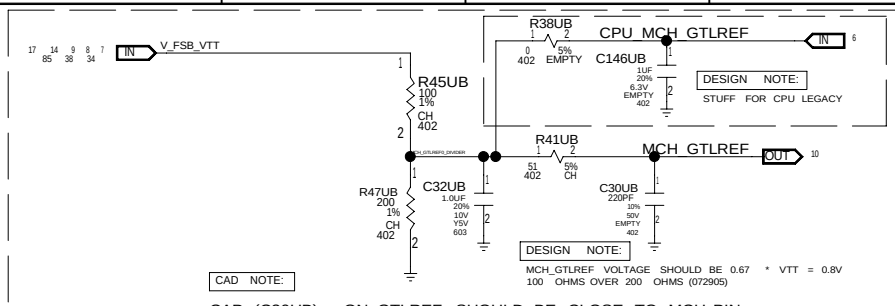


BPAGE DRAWING

frostburg_fabc.sch_1.16
Sun Mar 18 18:43:11 2007

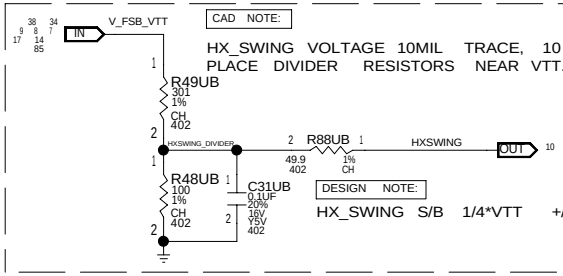
[PAGE_TITLE=PLL & CRT FILTERS]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	16	3.01



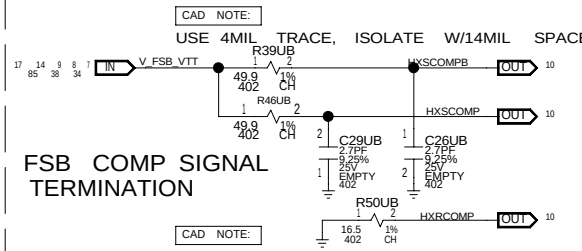
CAD NOTE:

CAP (C30UB) ON GTLREF SHOULD BE CLOSE TO MCH PIN
USE 10MIL TRACE, ISOLATE W/7MIL SPACE AFTER 250 MIL BREAKOUT



CAD NOTE:

HX_SWING VOLTAGE 10MIL TRACE, 10 MIL SPACE AFTER 250 MIL BREAKOUT.
PLACE DIVIDER RESISTORS NEAR VTT.



FSB COMP SIGNAL TERMINATION

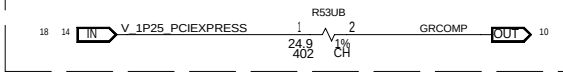
CAD NOTE:

USE 4MIL TRACE, ISOLATE W/14MIL SPACE AFTER 300 MIL BREAKOUT

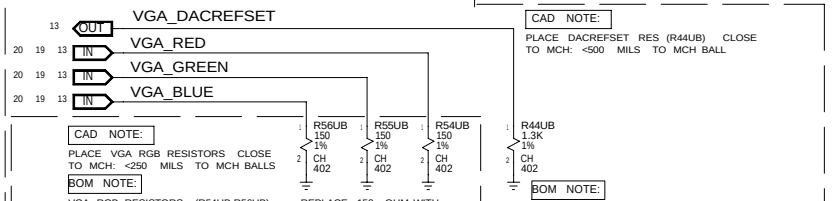
CAD NOTE:

USE 5MIL TRACE, ISOLATE W/5MIL SPACE; IF >250MILS INCREASE TO 10/7

PCIE COMP SIGNAL TERMINATION



DACREFSET & RGB MCH-SIDE TERMINATION



CAD NOTE:

PLACE VGA RGB RESISTORS CLOSE TO MCH: <250 MILS TO MCH BALLS

BOM NOTE:

VGA RGB RESISTORS (R54UB-R56UB): REPLACE 150 OHM WITH 0 OHM (A93549-001) FOR NON-GRAPHICS SKUS

CAD NOTE:

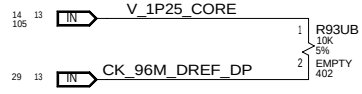
PLACE DACREFSET RES (R44UB) CLOSE TO MCH: <500 MILS TO MCH BALL

BOM NOTE:

DACREFSET RESISTOR (R44UB): REPLACE 1.3K WITH 0 OHM FOR NON-GRAPHICS SKUS

BOM NOTE:

STUFF R93UB FOR NON-GRAPHICS SKUS



BOM NOTE:

STUFF R98UB FOR NON-GRAPHICS SKUS

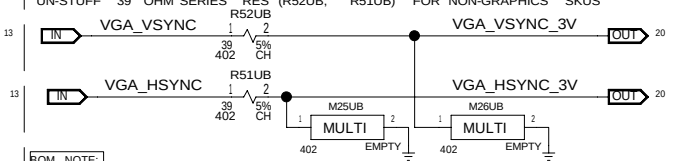
HSYNC/VSYNC SLEW RATE & EMI CONTROL

CAD NOTE:

HSYNC/VSYNC; LOCATE SERIES RESISTOR STRAPS (R52UB, R51UB) WITHIN 750 MILS OF MCH

BOM NOTE:

UN-STUFF 39 OHM SERIES RES (R52UB, R51UB) FOR NON-GRAPHICS SKUS



BOM NOTE:

STUFF 0 OHM RES (M25UB, M26UB) FOR NON-GRAPHICS SKUS

DESIGN NOTE:

MULTI-SITES TO BE USED FOR SLEW RATE/EMI CAPS ON GRAPHIC SKUS

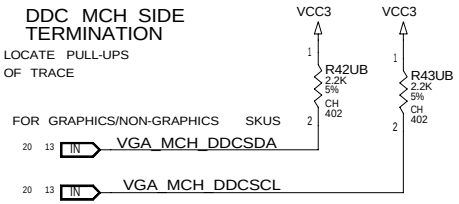
DDC MCH SIDE TERMINATION

CAD NOTE:

DDC_DATA/DDC_CLK; LOCATE PULL-UPS ANYWHERE ON ROUTE OF TRACE

BOM NOTE:

STUFF R42UB, R43UB FOR GRAPHICS/NON-GRAPHICS SKUS



MODULE REV DETAILS

MODULE NAME	REV	DATE

[PAGE_TITLE=MCH DECOUPLING AND COMP]

BPAGE DRAWING

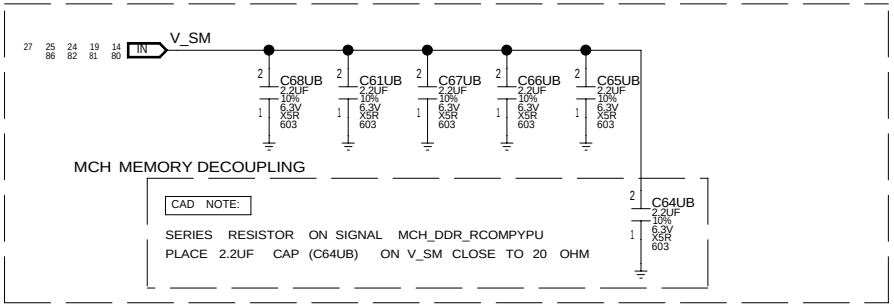
frostburg_fabc.sch_1.17
Sun Mar 18 18:43:12 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	17	3.01

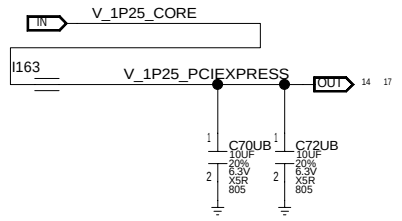
MODULE REV DETAILS

MODULE NAME	REV	DATE

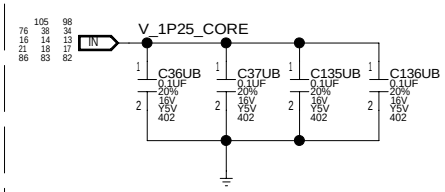
MCH MEMORY DECOUPLING



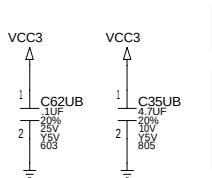
PCI EXPRESS DECOUPLING



PCI-E SIGNAL TRANSITION STICHING CAPS



VCC_HVGIO DECOUPLING



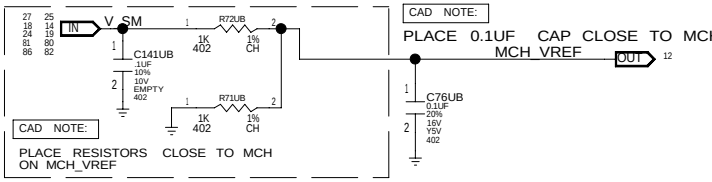
BPAGE DRAWING

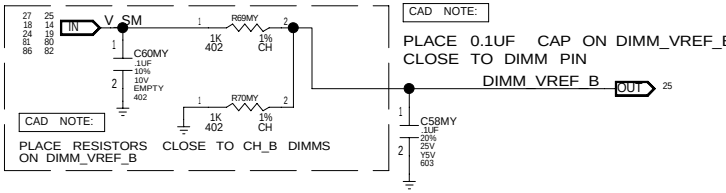
frostburg_fabc.sch_1.18
Sun Mar 18 18:43:13 2007

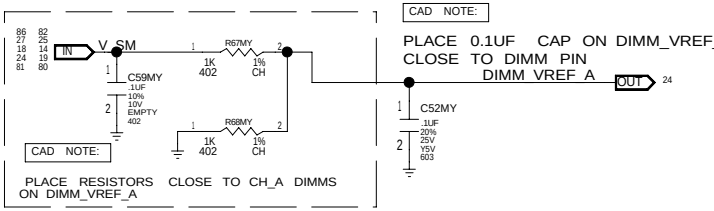
[PAGE_TITLE=MCH DCPL & VGA TERMINATION]

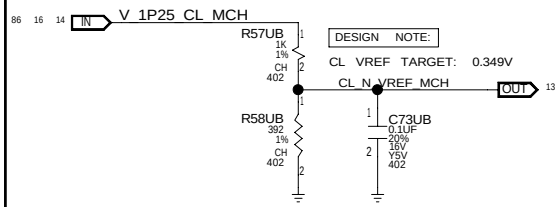
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	18	3.01

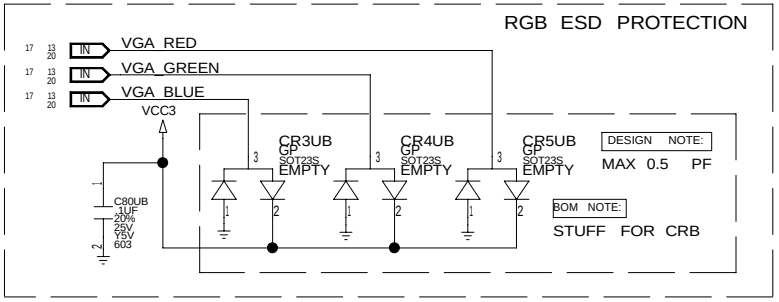
MODULE REV DETAILS		
MODULE NAME	REV	DATE

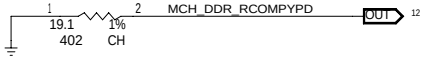


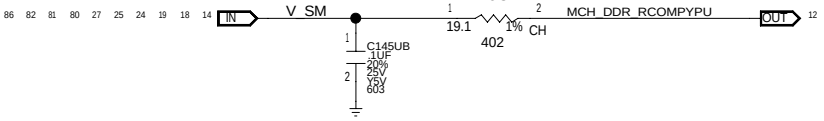


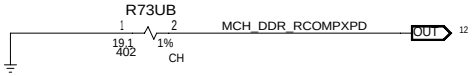


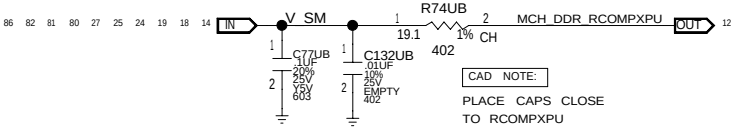


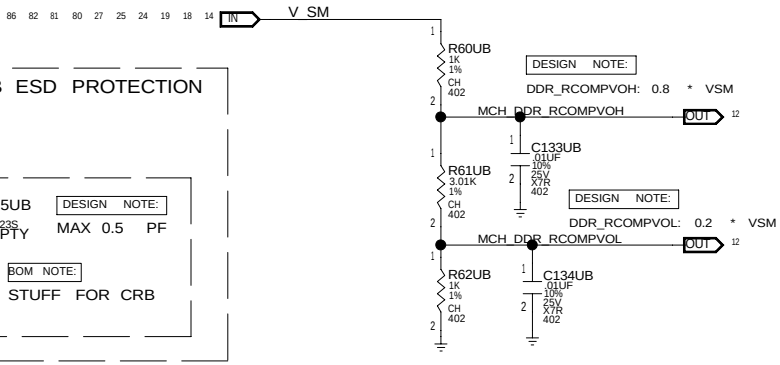












[PAGE_TITLE=MCH VREFS & TERMINATION]

BPAGE DRAWING

frostburg_fabc.sch_1.19
Sun Mar 18 18:43:14 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	19	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BW_ATX_CORE	1.06.00	5-5-06

BOM NOTE:
CHANGE FOR BANDWIDTH OPTIMIZE FOR CRB

BOM NOTE:
DEFAULT: STUFF FERRITE BEAD <693286-006> FOR <200MHZ BANDWIDTH CUTOFF
REPLACE WITH 0OHM 603 FOR >200MHZ BANDWIDTH CUTOFF

VGA_RED
VGA_GREEN
VGA_BLUE
VGA_HSYNC_3V
VGA_VSYNC_3V

693286-006 FB3UB FB
693286-006 FB4UB FB
693286-006 FB5UB FB

M13UB MULTI FB
M14UB MULTI FB
M15UB MULTI FB

VCC
C92281-003
RT1UB THRMSTR 1.10
VGA_THERM_PN1
M12UB MULTI CH 805
C94UB .1UF 20% 25V Y5V 603

J4UB RCPT
VGA_RED_CONN
VGA_THERM_9
VGA_GREEN_CONN
VGA_BLUE_CONN
TP_VGACONN_11_CORE_R
TP_VGACONN_4_CORE

C89UB 10PF 5% 50V COG 402
C90UB 22PF 5% 50V COG 402
C92UB 10PF 5% 50V COG 402 "COG"
C93UB 10PF 5% 50V COG 402
C81UB 22PF 5% 50V COG 402
C82UB 10PF 5% 50V COG 402 "COG"
C85UB 10PF 5% 50V COG 402
C84UB 22PF 5% 50V COG 402
C83UB 10PF 5% 50V COG 402 "COG"

BOM NOTE:
DEFAULT: STUFF 10PF <A36094-025> FOR BANDWIDTH <200MHZ
REPLACE WITH 3.3PF FOR BANDWITH >200MHZ

BOM NOTE:
DEFAULT: STUFF 22PF <A36095-030> FOR BANDWIDTH <200MHZ
REPLACE WITH 3.3PF FOR BANDWITH >200MHZ

BOM NOTE:
DEFAULT: STUFF 10PF <A36094-025> FOR BANDWIDTH <200MHZ
EMPTY FOR BANDWITH >200MHZ

A36094-025

C87UB 100PF 5% 50V EMPTY 402
C88UB 100PF 5% 50V EMPTY 402

R84UB 150 1% CH 402
R85UB 150 1% CH 402
R86UB 150 1% CH 402

CAD NOTE:
PLACE RESISTORS CLOSE TO FILTERS
(CAPS / FERRITE-BEADS)

VCC
R13BU 0 1A EMPTY 603
CR7UB BAT54C SOT23C DIO
VGA_DDCSDA_5V_R
R80UB 2.2K 5% CH 402
R82UB 2.2K 5% CH 402

VCC3
CR1UB GP SOT23S EMPTY
CR2UB GP SOT23S EMPTY
C144UB .1UF 10% 10V EMPTY 402

VCC3
Q2UB EMPTY
BOM NOTE:
REPLACE 603400-001 WITH C79254-001 (PB FREE #)
VGA_DDCSDA_5V_R

VGA_MCH_DDCSDA
R112UB 0 402 5% EMPTY
VGA_MCH_DDCSDA_R
R110UB 0 402 5% EMPTY
VGA_DDCSDA_5V
R83UB 0 402 5% CH
VGA_DDCSDA_CONN

VGA_MCHSIO_DDCSDA
R114UB 0 402 5% CH

VCC3
Q3UB EMPTY
BOM NOTE:
REPLACE 603400-001 WITH C79254-001 (PB FREE #)
VGA_DDCSCL_5V_R

R111UB 0 402 5% EMPTY
VGA_DDCSCL_5V
R81UB 0 402 5% CH
VGA_DDCSCL_CONN

VGA_MCH_DDCSCL
R113UB 0 402 5% EMPTY
VGA_MCH_DDCSCL_R

VGA_MCHSIO_DDCSCL
R115UB 0 402 5% CH

R116UB 100 402 5% CH
VGA_SIO_DDCSDA_5V
R117UB 100 402 5% CH
VGA_SIO_DDCSCL_5V

6.2V EMPTY
CR6UB TVS6_2V
TP_VGA_5V_PINA
TP_VGA_5V_PINB

C86UB 100PF 5% 50V EMPTY 402
C91UB 100PF 5% 50V EMPTY 402

BOM NOTE:
UN-STUFF ALL COMPONENTS ON PAGE FOR NON-GRAPHICS SKUS

BPAGE DRAWING
frostburg_fabc.sch_1.20
Sun Mar 18 18:43:15 2007

[PAGE_TITLE=VGA CONNECTOR]

BW_ATX_CORE

CR-21 : @FROSTBURG_FABC_LIB.FROSTBURG_FABC(SCH_1):PAGE21

SLOT 1

PCI EXPRESS
16-PORT
RIGHT LATCH
(DEFAULT)

BOM NOTE:
STUFF J6UB
EMPTY J10UB

J6UB
3GIO_X16
REV=2.0

KEY

CONN

C73571-001
J5UB
PCIE_RM
EMPTY
PCI E RETENTION MODEL

DESIGN NOTE:
ALWAYS STUFF C99UB & C95UB
EVEN IF J6UB IS EMPTY
FOR X1 DECOUPLING

CAD NOTE:
PLACE NEAR EDGE OF PEG SLOT
FOR SIGNAL TRANSITION REF

DESIGN NOTE:
ATX FF ONLY

BPAGE DRAWING
frostburg_fabc.sch_1.21
Sun Mar 18 18:43:16 2007
1 OF 1

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BW_ATX_CORE	1.06.00	5-5-06

[PAGE_TITLE=PCI EXPRESS X16]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	21	3.01

CUSTOM TEXT 2 BPAGE

SLOT 1

PCI EXPRESS
16-PORT
LEFT LATCH

BOM NOTE:
STUFF J6UB
EMPTY J10UB

J10UB
3GIO_X16
REV=2.0

DESIGN NOTE:
PCIE X16 GRAPHIC CONNECTOR WITH LEFT LATCH

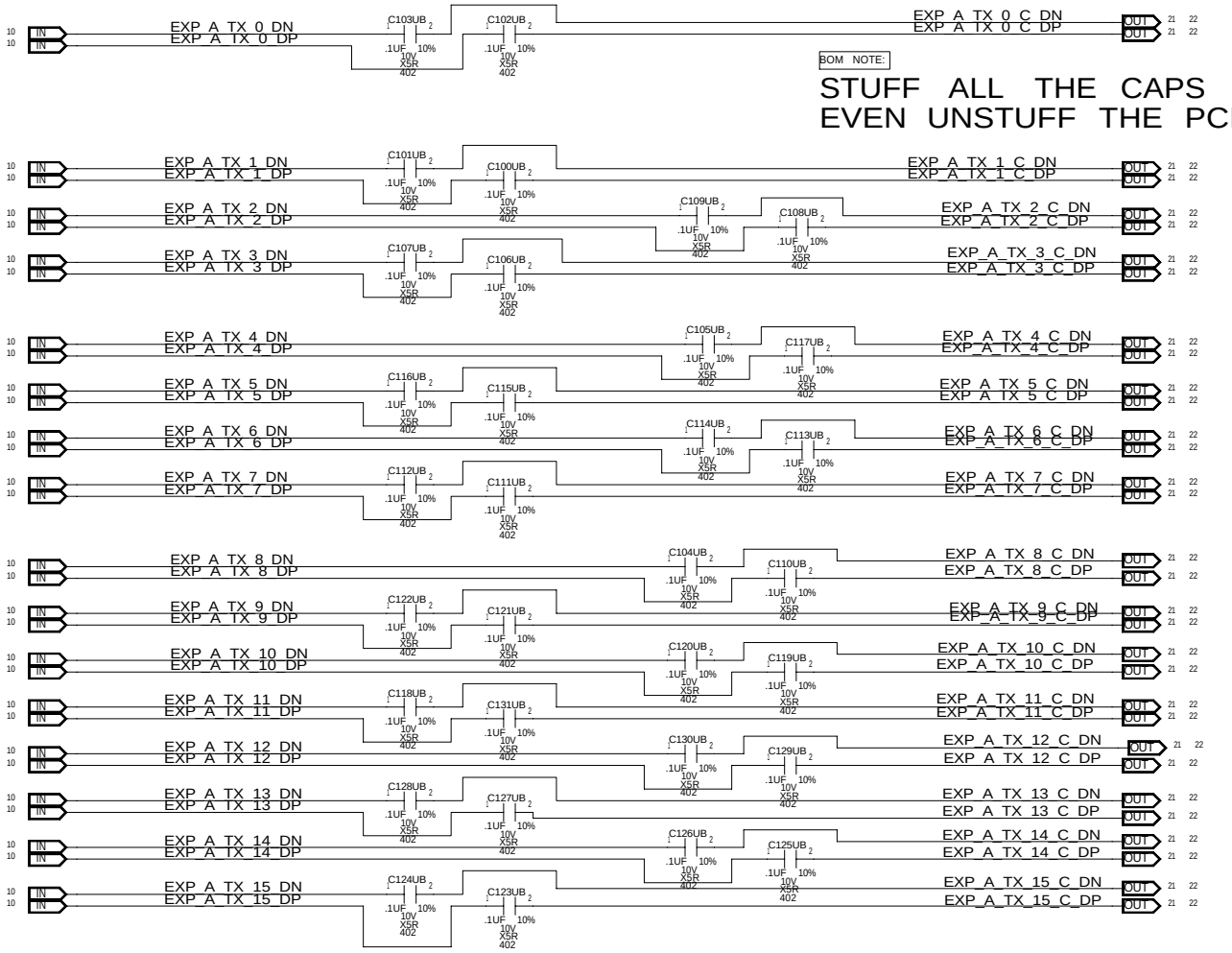
MODULE REV DETAILS		
MODULE NAME	REV	DATE
BW_ATX_CORE	1.06.00	5-5-06

BPAGE DRAWING
frostburg_fabc.sch_1.22
Sun Mar 18 18:43:17 2007

[PAGE_TITLE=PCI EXPRESS X16]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	22	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BW_ATX_CORE	1.06.00	5-5-06



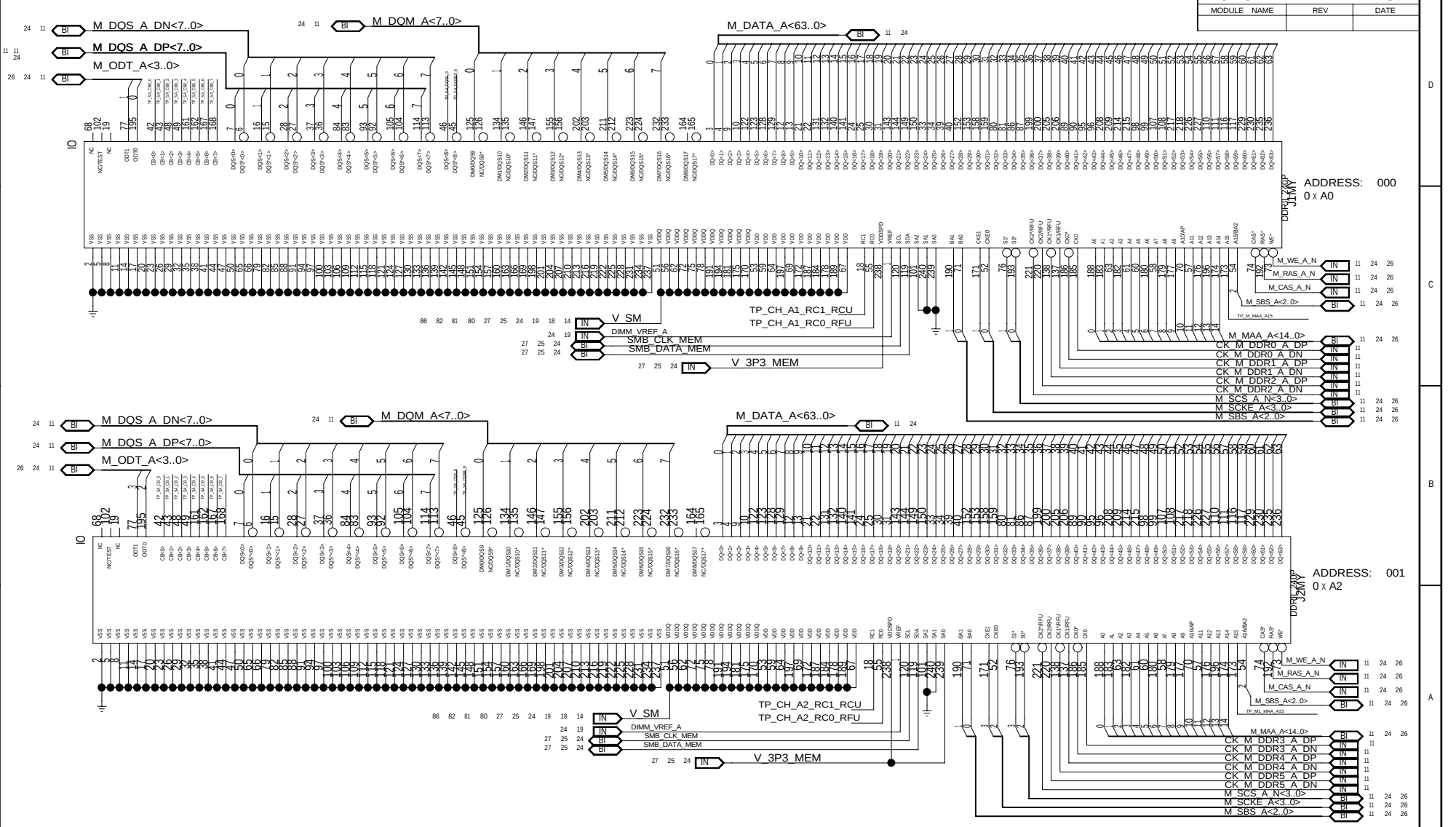
[PAGE_TITLE=PCI EXPRESS X16 COUPLING]

BPAGE DRAWING
frostburg_fabc.sch_1.23
Sun Mar 18 18:43:18 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	23	3.01

CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE



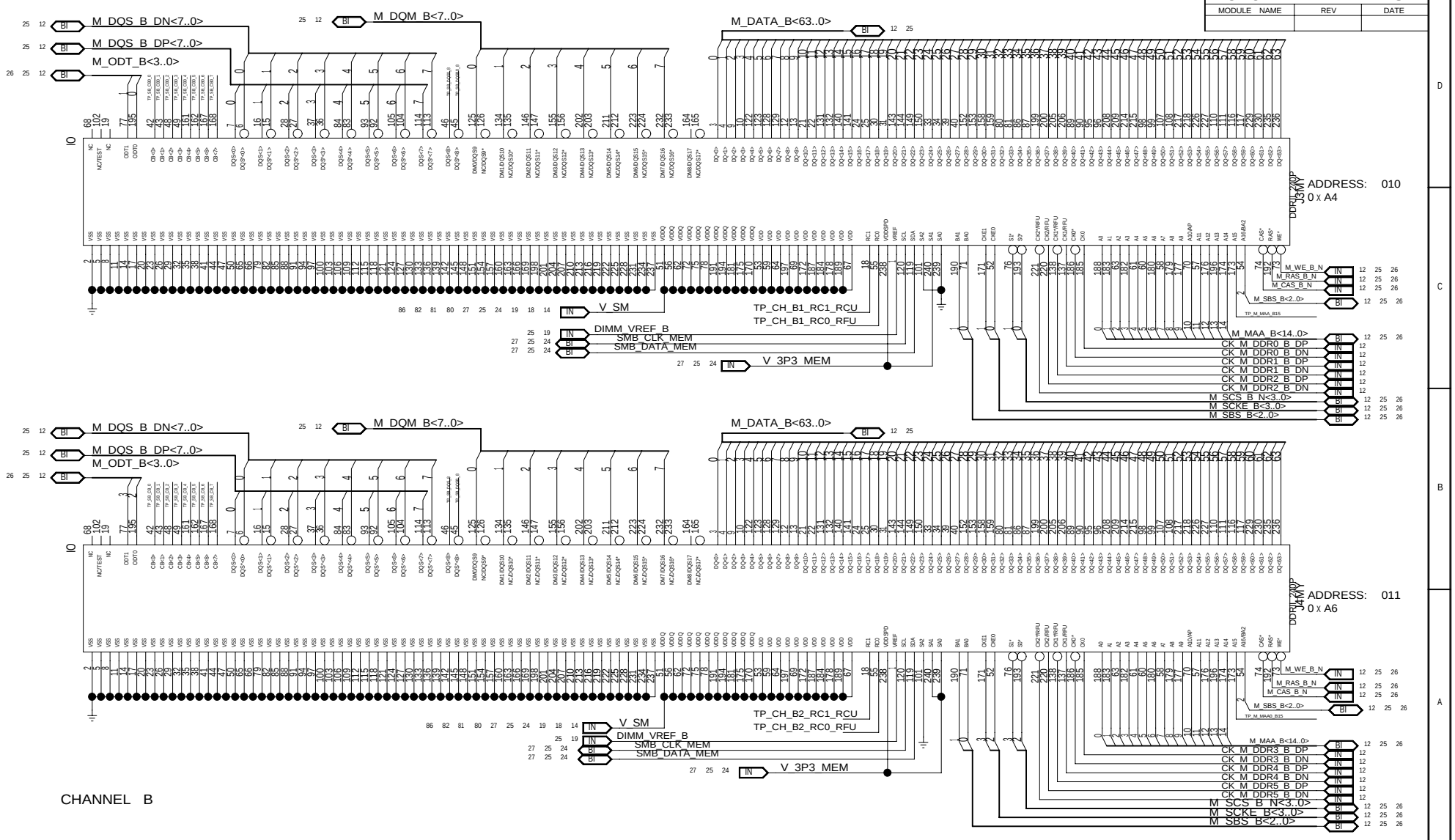
CHANNEL A

[PAGE_TITLE=240P CONN DDR2, CH A]

BPAGE DRAWING
frostburg_fabc.sch_1.24
Sun Mar 18 18:43:19 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	24	3.01

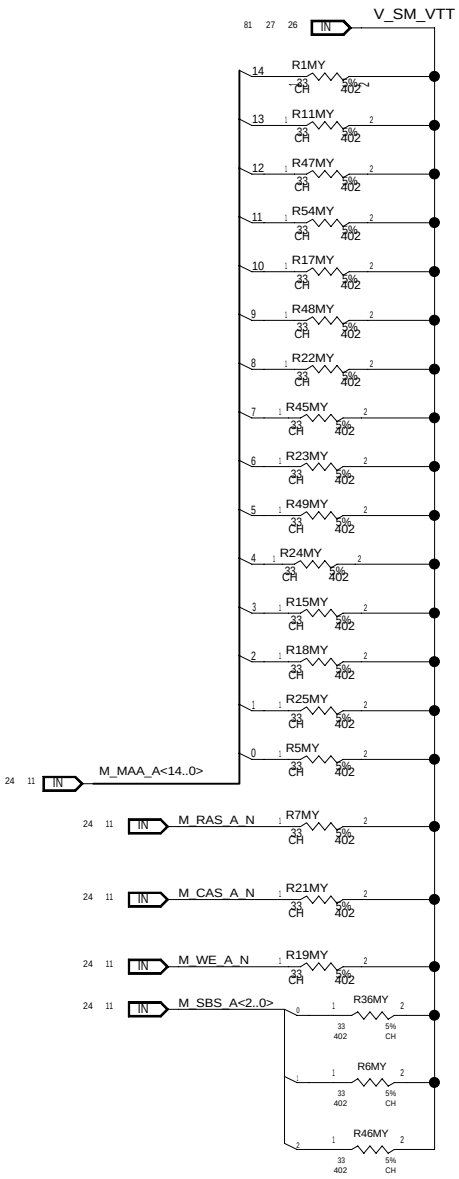
MODULE REV DETAILS		
MODULE NAME	REV	DATE

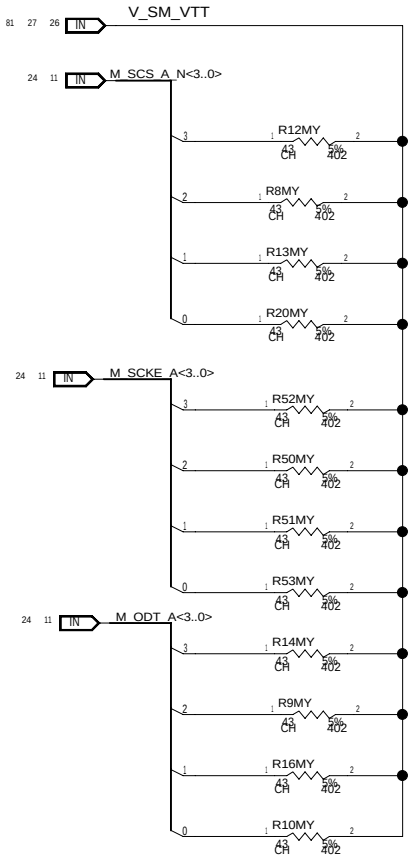


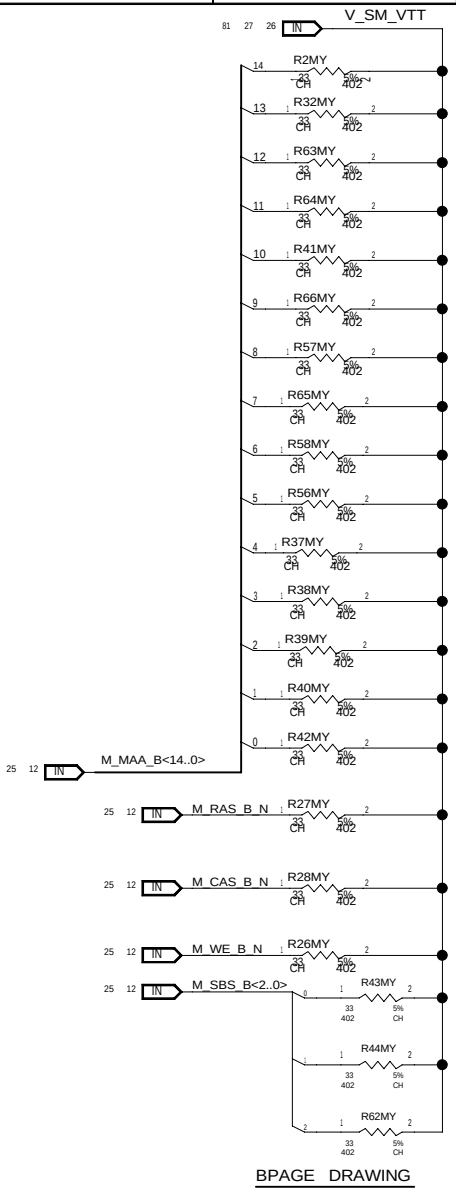
[PAGE_TITLE=240P CONN DDR2, CH B]

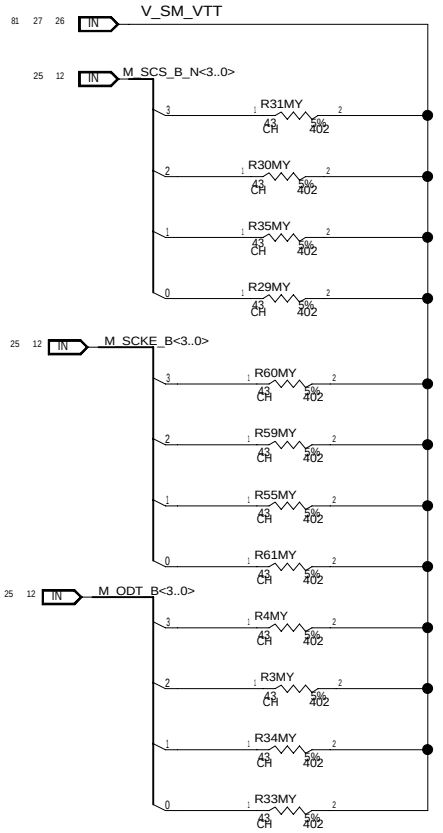
BPAGE DRAWING
frostburg_fabc.sch_1.25
Sun Mar 18 18:43:25 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	25	3.01









BPAGE DRAWING

frostburg_fabc.sch_1.26
Sun Mar 18 18:43:30 2007

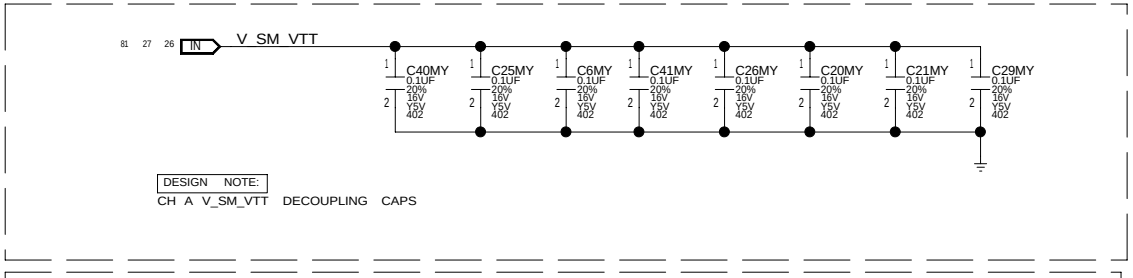
[PAGE_TITLE=DDR VTT TERMINATION]

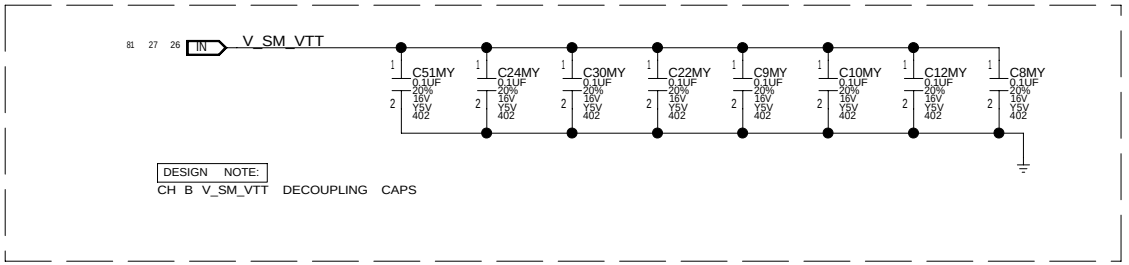
MODULE REV DETAILS		
MODULE NAME	REV	DATE

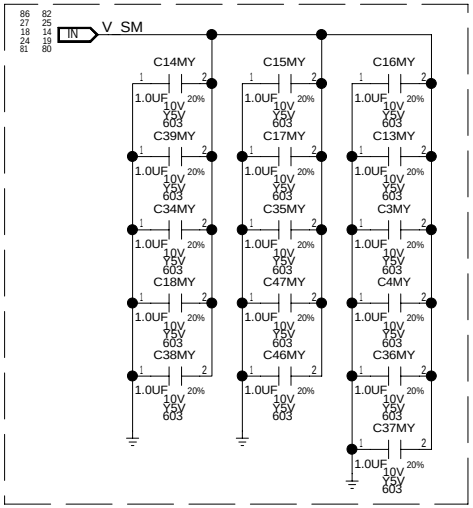
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	26	3.01

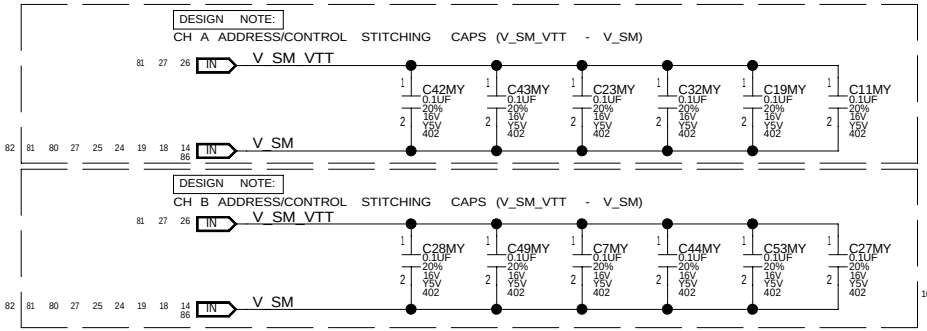
DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS

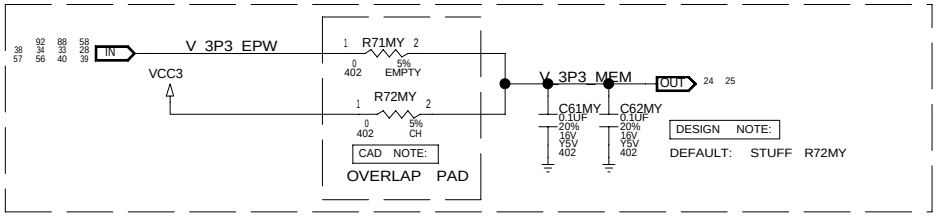
MODULE REV DETAILS		
MODULE NAME	REV	DATE

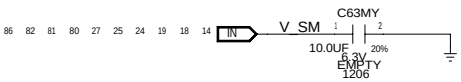


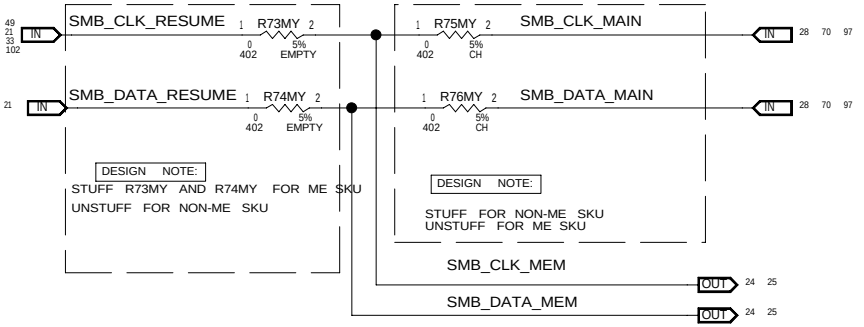










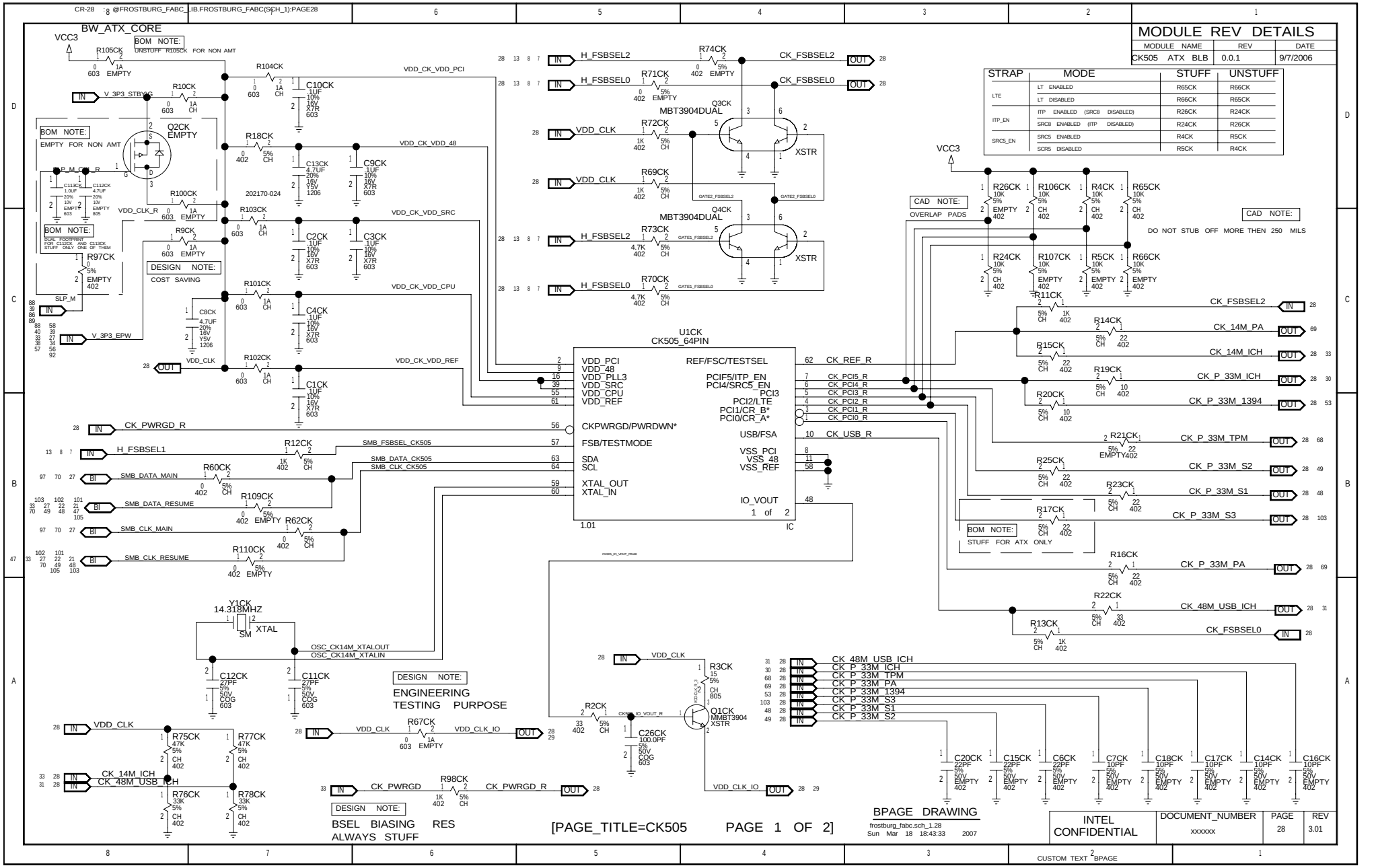


[PAGE_TITLE=DDR VTT DECOUPLING]

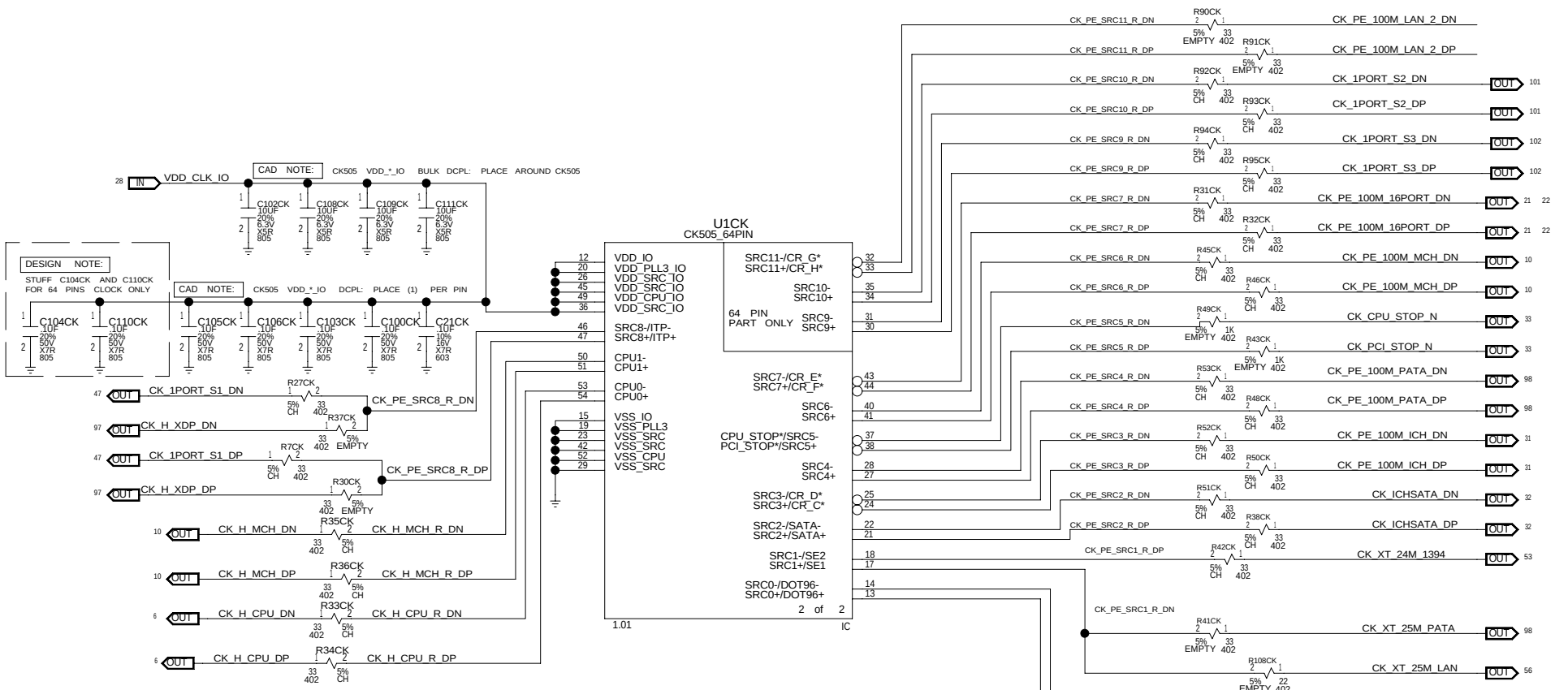
BPAGE DRAWING
frostburg_fabc.sch_1.27
Sun Mar 18 18:43:31 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	27	3.01

CUSTOM TEXT BPAGE


CR-28 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(SCH_1):PAGE28
BW_ATX_CORE
MODULE REV DETAILS
MODULE NAME | REV | DATE
CK505 ATX BLB | 0.0.1 | 9/7/2006
STRAP | MODE | STUFF | UNSTUFF
LTE | LT ENABLED | R65CK | R66CK
LTE | LT DISABLED | R66CK | R65CK
ITP_EN | ITP ENABLED (SRC8 DISABLED) | R26CK | R24CK
ITP_EN | SRC8 ENABLED (ITP DISABLED) | R24CK | R26CK
SRC5_EN | SRC5 ENABLED | R4CK | R5CK
SRC5_EN | SCR5 DISABLED | R5CK | R4CK
U1CK
CK505_64PIN
VDD_PCI
VDD_48
VDD_PLL3
VDD_SRC
VDD_CPU
VDD_REF
CKPWRGD/PWRDWN*
FSB/TESTMODE
SDA
SCL
XTAL_OUT
XTAL_IN
REF/FSC/TESTSEL
PCIF5/ITP_EN
PCI4/SRC5_EN
PCI3
PCI2/LTE
PCI1/CR_B*
PCI0/CR_A*
USB/FSA
VSS_PCI
VSS_48
VSS_REF
IO_VOUT
CK_REF_R
CK_PCI5_R
CK_PCI4_R
CK_PCI3_R
CK_PCI2_R
CK_PCI1_R
CK_PCI0_R
CK_USB_R
1 of 2
1.01
IC
DESIGN NOTE:
ENGINEERING TESTING PURPOSE
DESIGN NOTE:
BSEL BIASING RES ALWAYS STUFF
CAD NOTE:
OVERLAP PADS
CAD NOTE:
DO NOT STUB OFF MORE THEN 250 MILS
BOM NOTE:
STUFF FOR ATX ONLY
BPAGE DRAWING
frostburg_fabc.sch_1.28
Sun Mar 18 18:43:33 2007
[PAGE_TITLE=CK505 PAGE 1 OF 2]
INTEL CONFIDENTIAL
DOCUMENT_NUMBER
xxxxxx
PAGE
28
REV
3.01
CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE
CK505 ATX BLB	0.0.1	9-7-2006



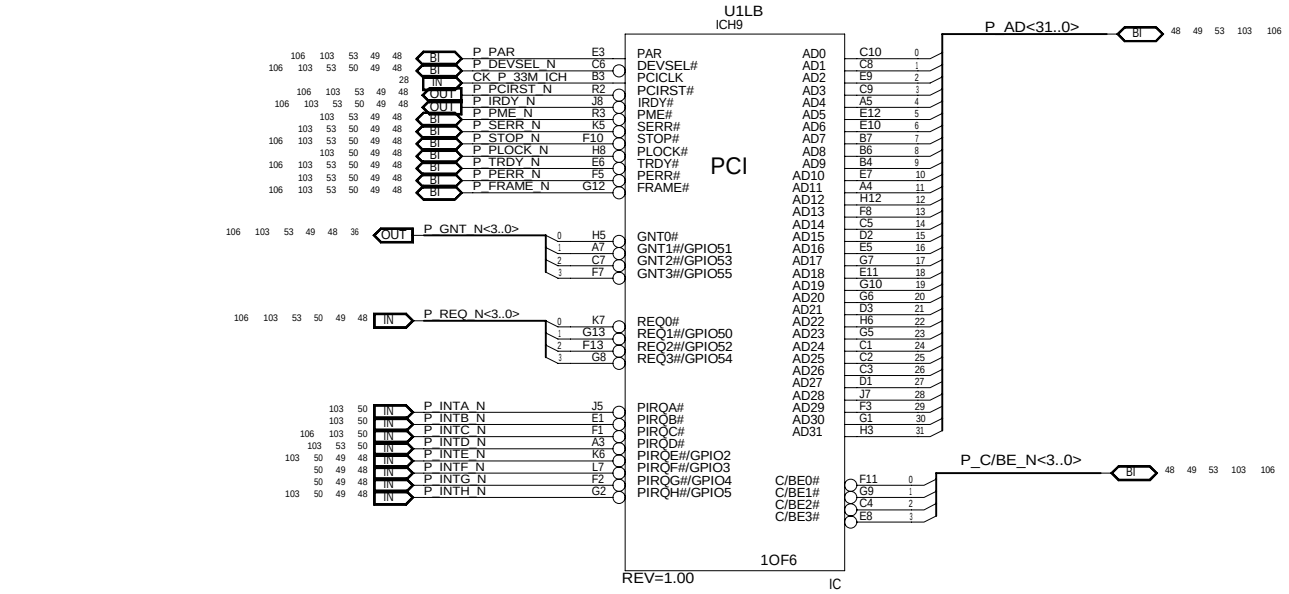
[PAGE_TITLE=CK505 PAGE 2 OF 2]

BPAGE DRAWING
frostburg_fabc.sch_1.29
Sun Mar 18 18:43:34 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	29	3.01

CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE
ICH9	0.2.1	08/30/06



J1LB
ICH6_HSK
IC C46655-001

NOTE:
NO PHYSICAL PINS
ON ALLEGRO MODEL

J3LB NC HDR A13494-008

J2LB NC HDR A13494-008

[PAGE_TITLE= ICH9 1 0F 6 CONTROL]

BPAGE DRAWING
frostburg_fabc.sch_1.30
Sun Mar 18 18:43:35 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	30	3.01

CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE
ICH9	0.2.1	08/30/06

CAD NOTE:
PLACE ALL NEAR ICH

HSO1_DP — C54LB (.1UF 10V X5R 402) — TP_HSO1_DP
HSO1_DN — C51LB (.1UF 10V X5R 402) — TP_HSO1_DN
HSO2_DP — C55LB (.1UF 10V X5R 402) — HSO2_C_DP
HSO2_DN — C53LB (.1UF 10V X5R 402) — HSO2_C_DN
HSO3_DP — C49LB (.1UF 10V X5R 402) — HSO3_C_DP
HSO3_DN — C48LB (.1UF 10V X5R 402) — HSO3_C_DN
HSO4_DP — C46LB (.1UF 10V X5R 402) — HSO4_C_DP
HSO4_DN — C47LB (.1UF 10V X5R 402) — HSO4_C_DN

CAD NOTE: ATX: HSO5 ROUTE TO 2ND PCIEX1

HSO5_DP — C44LB (.1UF 10V X5R 402) — HSO5_C_DP
HSO5_DN — C45LB (.1UF 10V X5R 402) — HSO5_C_DN

BOM NOTE:
STUFF C44LB AND C45LB FOR TEST TOOL

HSO6_DP — C52LB (.1UF 10V X5R 402) — HSO6_C_DP — TO LAN
HSO6_DN — C50LB (.1UF 10V X5R 402) — HSO6_C_DN

U1LB
ICH9

DMI_MT_IR_0_DN W28
DMI_MT_IR_0_DP W26
DMI_IT_MR_0_DN V30
DMI_IT_MR_0_DP V29
DMI_MT_IR_1_DN AA26
DMI_MT_IR_1_DP AA28
DMI_IT_MR_1_DN Y30
DMI_IT_MR_1_DP Y29
DMI_MT_IR_2_DN AC26
DMI_MT_IR_2_DP AC28
DMI_IT_MR_2_DN AB30
DMI_IT_MR_2_DP AB29
DMI_MT_IR_3_DN AF26
DMI_MT_IR_3_DP AE26
DMI_IT_MR_3_DN AD29
DMI_IT_MR_3_DP AD30

DMI0RXN DMI0RXP DMI0TXN DMI0TXP DMI1RXN DMI1RXP DMI1TXN DMI1TXP DMI2RXN DMI2RXP DMI2TXN DMI2TXP DMI3RXN DMI3RXP DMI3TXN DMI3TXP — DMI

HSI6_C_DN D29
HSI6_C_DP D30
HSO6_DN E26
HSO6_DP E28
TP_HSI1_DN P30
TP_HSI1_DP P29
HSO1_DN R26
HSO1_DP R28
HSI2_DN M30
HSI2_DP M29
HSO2_DN N26
HSO2_DP N28
HSI3_DN K30
HSI3_DP K29
HSO3_DN L26
HSO3_DP L28
HSI4_DN H30
HSI4_DP H29
HSO4_DN J26
HSO4_DP J28
HSI5_DN F30
HSI5_DP F29
HSO5_DN G26
HSO5_DP G28

PERN6/GLAN_RXN PERP6/GLAN_RXP PETN6/GLAN_TXN PETP6/GLAN_TXP PERn1 PERp1 PETn1 PETp1 PERn2 PERp2 PETn2 PETp2 PERn3 PERp3 PETn3 PETp3 PERn4 PERp4 PETn4 PETp4 PERn5 PERp5 PETn5 PETp5 — PCI-E

R9LB: V_1P5_FILTER — 402 24.9 1% CH — DMICOMP AF28 / AF30
DMI_IRCOMP
DMI_ZCOMP

CK_PE_100M_ICH_DN U26
CK_PE_100M_ICH_DP U25
DMI_CLKN
DMI_CLKP

2OF6
REV=1.00
IC

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P — USB

AD6 USB_FRONT1_DN
AD5 USB_FRONT1_DP
AE3 USB_FRONT2_DN
AE2 USB_FRONT2_DP
AD1 USB_FRONT5_DN
AD2 USB_FRONT5_DP
AB6 USB_FRONT6_DN
AB5 USB_FRONT6_DP
AC3 USB_FRONT4_DN
AC2 USB_FRONT4_DP
AB1 USB_FRONT3_DN
AB2 USB_FRONT3_DP
Y6 USB_BACK6_DN
Y5 USB_BACK6_DP
AA3 USB_BACK5_DN
AA2 USB_BACK5_DP
Y1 USB_BACK4_DN
Y2 USB_BACK4_DP
V6 USB_BACK2_DN
V5 USB_BACK2_DP
W2 USB_BACK3_DN
W3 USB_BACK3_DP
V1 USB_BACK1_DN
V2 USB_BACK1_DP

OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8#/GPIO44 OC9#/GPIO45 OC10#/GPIO46 OC11#/GPIO47
P5 USB_OC0_R_N
N3 USB_OC1_R_N
P7 USB_OC2_R_N
R7 USB_OC3_R_N
N2 USB_OC4_R_N
N1 USB_OC5_R_N
N5 USB_OC6_R_N
M1 USB_OC7_R_N
P3 USB_OC8_R_N
R6 USB_OC9_R_N
T7 USB_OC10_R_N
P1 USB_OC11_R_N

USBRBIAS# USBRBIAS
AG1 USBRBIAS_ICH
AG2

CLK48
AG3 CK_48M_USB_ICH

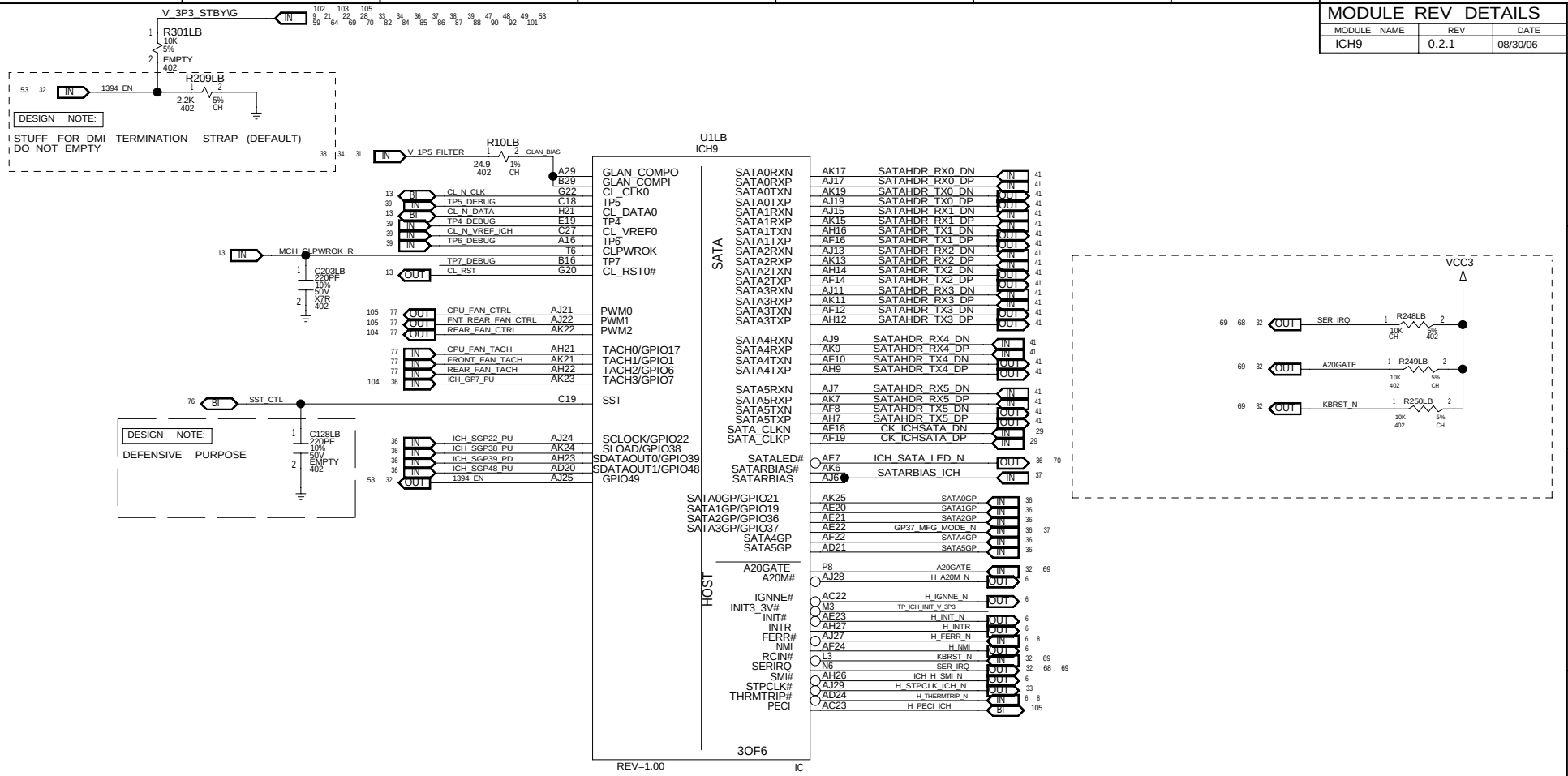
USB_OC_FRONT1_N — I86 USB_OC0_R_N; I85 USB_OC1_R_N
USB_OC_FRONT3_N — I87 USB_OC2_R_N; I84 USB_OC3_R_N
USB_OC_FRONT2_N — I89 USB_OC4_R_N; I88 USB_OC5_R_N
USB_OC_BACK1_N — I90 USB_OC6_R_N; I92 USB_OC7_R_N
USB_OC_BACK0_N — I99 USB_OC8_R_N; I139 USB_OC9_R_N
USB_OC_BACK2_N — I140 USB_OC10_R_N; I141 USB_OC11_R_N

[PAGE_TITLE=ICH9 2 OF 6 CONTROL]

BPAGE DRAWING
frostburg_fabc.sch_1.31
Sun Mar 18 18:43:36 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	31	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
ICH9	0.2.1	08/30/06



[PAGE_TITLE=ICH9 3 OF 6 CONTROL]

BPAGE DRAWING

frostburg_fabc.sch_1.32
Sun Mar 18 18:43:38 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	32	3.01

CUSTOM TEXT 2 BPAGE

CR-33 : 8 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(SCH_1):PAGE33

MODULE REV DETAILS

MODULE NAME	REV	DATE
ICH9	0.2.1	08/30/06

CAD NOTE:
PLACE AT ICH
DESIGN NOTE:
DO NOT STUFF CIRCUIT. INTERNAL PULL-UP EXIST IN ICH9.

VCC3 R270LB 10K 5% EMPTY 402
VCC3 R15LB 10K 5% EMPTY 402

U1LB
ICH9

LPC: LDRQ1#/GPIO23, FWH0/LAD0, FWH1/LAD1, FWH2/LAD2, FWH3/LAD3, LDRQ0#, FWH4/LFRAME#
AUDIO: HDA_BIT_CLK, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDOUT, HDA_SYNC, CLK14
LAN: GLAN_CLK, LAN_RSTSYNC, LAN_RST#, LAN_RXD0, LAN_RXD1, LAN_RXD2, LAN_TXD0, LAN_TXD1, LAN_TXD2
RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#
SMB: SMBALERT#/GPIO11, SMBCLK, SMBDATA, LINKALERT#/GPIO60/CLGPIO4, SMLINK0, SMLINK1
SPI: SPI_MOSI, SPI_MISO, SPI_CS0#, SPI_CLK, SPI_CS1#/GPIO58/CLGPIO6
GPIO: GPIO0, GPIO8, WOL_EN/GPIO9, ALERT#/GPIO10, GPIO12, GPIO13, GPIO14/CLGPIO2, GPIO15, GPIO16, GPIO18, GPIO20, GPIO24/CLGPIO0, GPIO25, S4_STATE#/GPIO26, QRT_STATE0/GPIO27, QRT_STATE1/GPIO28, GPIO32, GPIO33, GPIO34, SATACLKREQ#/GPIO35, GPIO56, GPIO57/CLGPIO5
CSI: CPUPWRGD, LAN100_SLP, THRM#, VRMPWRGD, MCH_SYNC#, PWRBTN#, RI#, SUS_STAT#/LPCPD, SUSCLK, SYS_RESET#, PLTRST#, WAKE#, INTRUDER#, PWROK, RSMRST#, INTVRMEN, SPKR
SLP_S3#, SLP_S4#, SLP_S5#, SLP_M#, CK_PWRGD, TP0, TP1, TP2, TP3
4OF6
REV=1.00
IC

L_DRQ1_N, L_AD<3..0>, L_DRQ_N, L_FRAME_N
AUD_LINK_BCLK_R, AUD_LINK_RST_R_N, AUD_LINK_SDI0, AUD_LINK_SDI1, AUD_LINK_SDI2, TP_AUD_LINK_SDI3, AUD_LINK_SDO_R, AUD_LINK_SYNC_R, CK_14M_ICH
ICH_LAN_JCLK, ICH_LAN_JRST, LAN_PWROK, ICH_LAN_JRX0, ICH_LAN_JRX1, ICH_LAN_JRX2, ICH_LAN_JTX0, ICH_LAN_JTX1, ICH_LAN_JTX2
ICH_RTCX1, ICH_RTCX2, ICH_RTCRST_PULLUP, ICH_SRTCRSTB_PULLUP, ICH_PORT80_LED, SMB_CLK_RESUME, SMB_DATA_RESUME, SMLALERT_ICH, SMLINK0_ICH, SMLINK1_ICH
SPI_MOSI, SPI_MISO, SPI_CS0_N, SPI_CLK, SPI_CS1_N

CAD NOTE:
PLACE 15 OHM SERIES STRAPS CLOSE TO ICH
SPI_MOSI R158LB 15 1% 402 CH SPI_MOSI_PRI_SEC_FLSH
SPI_CLK R159LB 15 1% 402 CH SPI_CLK_PRI_SEC_FLSH
SPI_CS0_N R201LB 47 5% 402 CH SPI_CS0_ISOLATE_N

BOM NOTE:
STUFF TO ENABLE NO-REBOOT OPTION AT POWER-UP (CONFIGURATION STRAPPING).
VCC3 R17LB 1K 5% EMPTY 402
SPKR R18LB 1K 5% 402 CH CORE_SPKR_R
C1LB 1000PF 10% 50V EMPTY 603
VCC Q1LB MMBT3904 XSTR SPKR_OUT_R R16LB 47 5% EMPTY 402
R309LB 30 5% 402 CH SPKR_OUT
J8LB 1X2HDR EMPTY
LS1LB XDCR AT-08

ICH9_MGP1 R283LB 0 5% 402 EMPTY H_SKTOCC_N
DESIGN NOTE: STUFF R283LB FOR ME ON CPU PRESENT DETECTION
V_3P3_EPW R280LB 10K 5% 402 EMPTY SPI_MOSI
DESIGN NOTE: STUFF TO ENABLE ITPM

SLP_S3_ICH_N R11LB 0 5% 402 CH SLP_S3_N
VCC3 R222LB 1K 5% 402 EMPTY
ICH_SYNC_N R12LB 0 5% 402 CH ICH_SYNC_R_N
H_STPCLK_ICH_N R14LB 0 1A 603 CH H_STPCLK_N

V_3P3_STBYG R281LB 10K 5% 402 R313LB 10K 5% 402 EMPTY
FP_AUD_DETECT
TPEV_ICH_GPIO8, WOL_ONLY, ICH9_MGP1, LAN_DISABLE_N, IO_PME_N, 1_WATT_CTRL_2, CK_PCI_STOP_N, BOARDID<0>, BOARDID<1>, TP_ICH_GP20, GPIO_VSM_AMT_LED, CK_CPU_STOP_N, S4_STATE_N, ICH_QRT0, ICH_QRT1, CDC_DWN_DISABLE, GP33_SOP, ICH_CONFIG_JUMPER, 2X12_POWER_DETECT, ICH_GP56, TP_SATA_HOT_SWAP_POWER_CTRL
H_PWRGD, ICH_LAN100SLP_EN, ICH_THRM_N, ICH_VRMPWRGD, ICH_SYNC_R_N, SW_ON_N, ICH_RI_PU, LPCPD_N, SUSCLK, FP_RST_N, PLTRST_N_R, WAKE_N, ICH_INTRUDER_HDR_N, PWRGD_3V, ICH_RSMRST_N, ICH_INTVRMEN, SPKR
SLP_S3_ICH_N, SLP_S4_N, TP_SLP_S5_N, ICH_SLP_M_N, CK_PWRGD, ICH_BATLOW_PU, TP_DPRSTP, TP_DPSLP_N, TP_DFXTEST_N
R217LB 0 5% 402 CH PLTRST_N
C202LB 100PF 5% 50V EMPTY 402

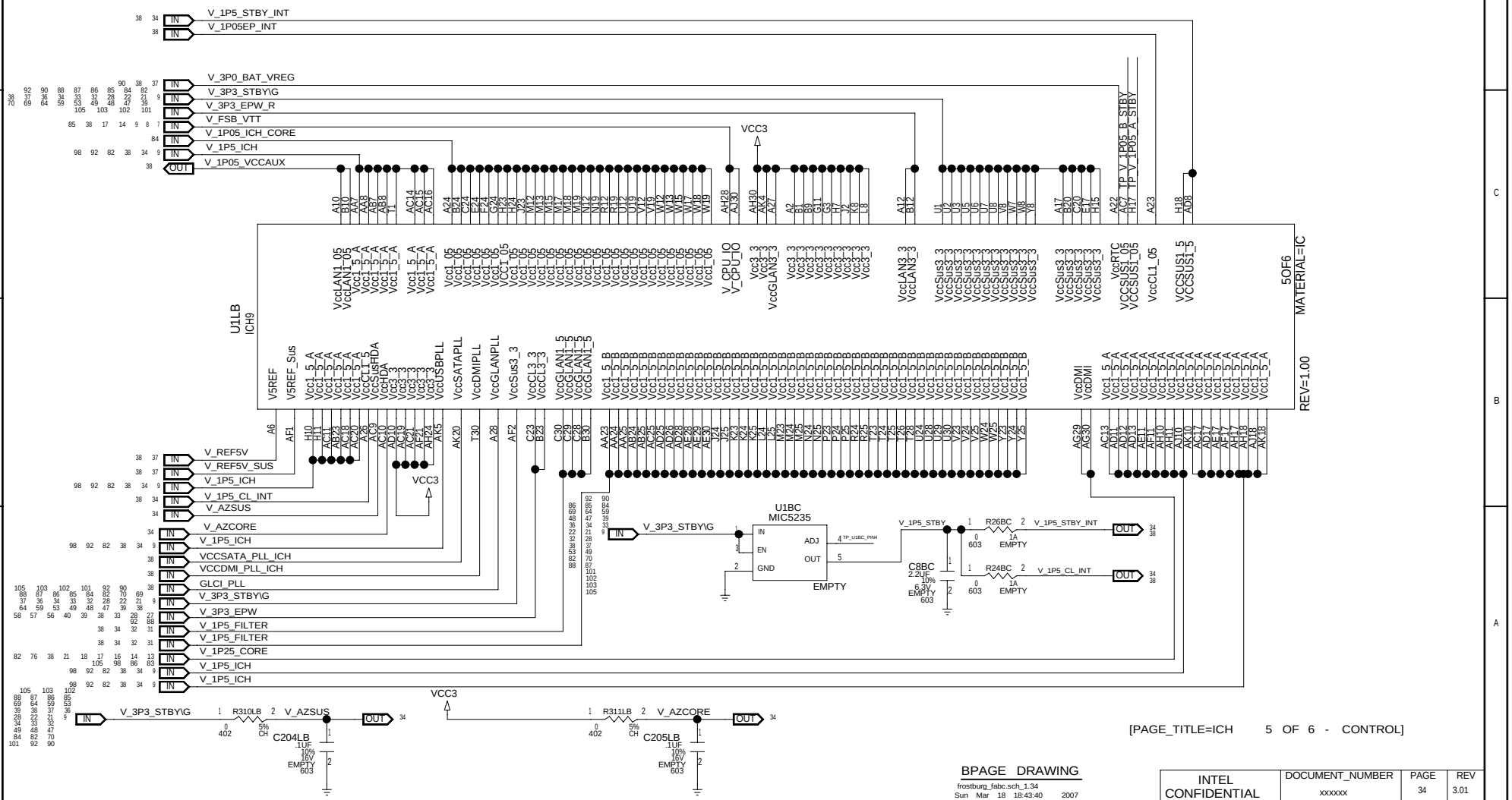
BPAGE DRAWING
frostburg_fabc.sch_1.33
Sun Mar 18 18:43:39 2007

[PAGE_TITLE=ICH9 4 OF 6 - CONTROL]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	33	3.01

CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE
ICH9	0.2.1	08/30/06



BPAGE DRAWING

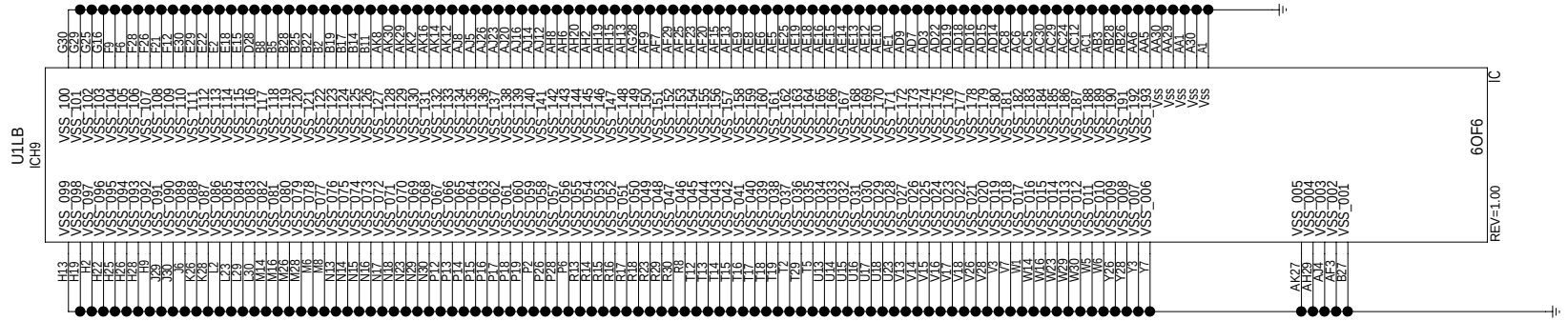
frostburg_fabc.sch_1.34
Sun Mar 18 18:43:40 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	34	3.01

CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS

MODULE NAME	REV	DATE
ICH9	0.2.1	08/30/06



[PAGE_TITLE=ICH 6 OF 6 - GROUND BODY]

BPAGE DRAWING

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Sun Mar 18 18:43:41 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	35	3.01

CR-36 : 8 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(SCH_1):PAGE36

MODULE REV DETAILS		
MODULE NAME	REV	DATE
ICH9	0.2.1	08/30/06

BOM NOTE:

DEFAULT EMPTY: STUFF 10K OHM RES (R54LB) FOR ICH PORT80 LED FEATURE (TDE EXPERIMENT)

V_3P3_STBY\G

R198LB R54LB R51LB R53LB R55LB R52LB R50LB R49LB R44LB R28LB R48LB
10K 5% CH 402 (R28LB: 220; R50LB: 1K)

TPEV_ICH_GPIO8
FP_RST_N
ICH_GP56
1_WATT_CTRL_2
WAKE_N
ICH_BATLOW_PU
SMLALERT_ICH
SMLINK0_ICH
SMLINK1_ICH
ICH_PORT80_LED
ICH_RI_PU

BOOT SELECT STRAPS

BOM NOTE:
STUFF FOR PRODUCT

P_GNT_N<3..0> — R34LB 1K 5% CH 402

SPI_CS1_N — R32LB 1K 5% EMPTY 402

VCC3

R29LB 3.24K 1% EMPTY 402
R33LB 3.24K 1% EMPTY 402

AUD_LINK_SDO_R
AUD_LINK_SYNC_R

R30LB 5% EMPTY 1K 402
R31LB 5% EMPTY 1K 402

P_GNT_N<3..0>

VCC3

R46LB R47LB R35LB R36LB R37LB R38LB R39LB R210LB R40LB R41LB R45LB R42LB R43LB
10K 5% CH 402 (R41LB: EMPTY 402)

ICH_GP7_PU
ICH_SGP22_PU
ICH_SGP38_PU
ICH_SGP39_PD
ICH_SGP48_PU

R19LB 10K 5% EMPTY 402

SATA4GP
SATA5GP
SATA0GP
SATA1GP
SATA2GP
GP37_MFG_MODE_N
FP_AUD_DETECT
ICH_SATA_LED_N

V_3P3_STBY\G

R229LB 10K 5% CH 402

GPIO_VSM_AMT_LED

R230LB 2.7K 5% EMPTY 402

DESIGN NOTE:
DEFAULT: CRYPTO ENGINE ENABLED
STUFF PU (R229LB) AND UN-STUFF PD (R230LB)

[PAGE_TITLE=GPIO TERMINATION & RST STRAPS]

BPAGE DRAWING
frostburg_fabc.sch_1.36
Sun Mar 18 18:43:43 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	36	3.01

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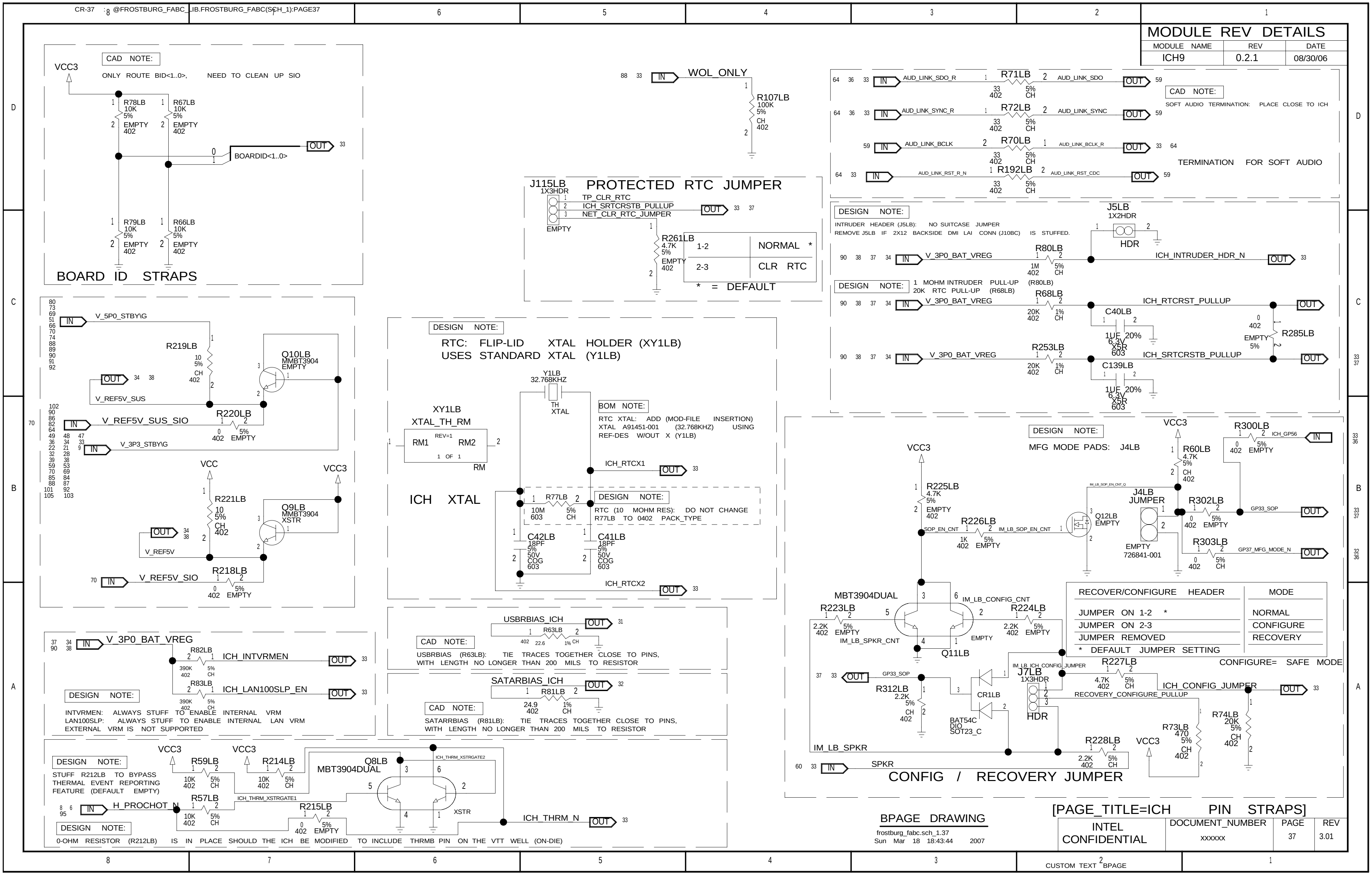
CR-37 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(SCH_1):PAGE37
MODULE REV DETAILS
MODULE NAME REV DATE
ICH9 0.2.1 08/30/06
CAD NOTE:
ONLY ROUTE BID<1..0>, NEED TO CLEAN UP SIO
VCC3
R78LB 10K 5% EMPTY 402
R67LB 10K 5% EMPTY 402
BOARDID<1..0>
R79LB 10K 5% EMPTY 402
R66LB 10K 5% EMPTY 402
BOARD ID STRAPS
WOL_ONLY
R107LB 100K 5% CH 402
J115LB 1X3HDR
PROTECTED RTC JUMPER
TP_CLR_RTC
ICH_SRTCRSTB_PULLUP
NET_CLR_RTC_JUMPER
EMPTY
R261LB 4.7K 5% EMPTY 402
1-2 NORMAL *
2-3 CLR RTC
* = DEFAULT
AUD_LINK_SDO_R R71LB AUD_LINK_SDO
AUD_LINK_SYNC_R R72LB AUD_LINK_SYNC
AUD_LINK_BCLK R70LB AUD_LINK_BCLK_R
AUD_LINK_RST_R_N R192LB AUD_LINK_RST_CDC
CAD NOTE:
SOFT AUDIO TERMINATION: PLACE CLOSE TO ICH
TERMINATION FOR SOFT AUDIO
DESIGN NOTE:
INTRUDER HEADER (J5LB): NO SUITCASE JUMPER
REMOVE J5LB IF 2X12 BACKSIDE DMI LAI CONN (J10BC) IS STUFFED.
J5LB 1X2HDR HDR
V_3P0_BAT_VREG R80LB 1M 402 5% CH ICH_INTRUDER_HDR_N
DESIGN NOTE:
1 MOHM INTRUDER PULL-UP (R80LB)
20K RTC PULL-UP (R68LB)
R68LB 20K 402 1% CH ICH_RTCRST_PULLUP
C40LB 1UF 20% 6.3V X5R 603
R285LB 0 402 EMPTY 5%
R253LB 20K 402 1% CH ICH_SRTCRSTB_PULLUP
C139LB 1UF 20% 6.3V X5R 603
V_5P0_STBY\G
R219LB 10 5% CH 402
Q10LB MMBT3904 EMPTY
V_REF5V_SUS
V_REF5V_SUS_SIO R220LB 0 402 5% EMPTY
V_3P3_STBY\G
VCC
R221LB 10 5% CH 402
VCC3
Q9LB MMBT3904 XSTR
V_REF5V
V_REF5V_SIO R218LB 0 402 5% EMPTY
DESIGN NOTE:
RTC: FLIP-LID XTAL HOLDER (XY1LB)
USES STANDARD XTAL (Y1LB)
Y1LB 32.768KHZ TH XTAL
XY1LB XTAL_TH_RM RM1 RM2 REV=1 1 OF 1 RM
BOM NOTE:
RTC XTAL: ADD (MOD-FILE INSERTION) XTAL A91451-001 (32.768KHZ) USING REF-DES W/OUT X (Y1LB)
ICH_RTCX1
ICH XTAL
R77LB 10M 603 5% CH
DESIGN NOTE:
RTC (10 MOHM RES): DO NOT CHANGE R77LB TO 0402 PACK_TYPE
C42LB 18PF 5% 50V COG 603
C41LB 18PF 5% 50V COG 603
ICH_RTCX2
V_3P0_BAT_VREG
R82LB 390K 402 5% CH ICH_INTVRMEN
R83LB 390K 402 5% CH ICH_LAN100SLP_EN
DESIGN NOTE:
INTVRMEN: ALWAYS STUFF TO ENABLE INTERNAL VRM
LAN100SLP: ALWAYS STUFF TO ENABLE INTERNAL LAN VRM
EXTERNAL VRM IS NOT SUPPORTED
USBRBIAS_ICH R63LB 402 22.6 1% CH
CAD NOTE:
USBRBIAS (R63LB): TIE TRACES TOGETHER CLOSE TO PINS, WITH LENGTH NO LONGER THAN 200 MILS TO RESISTOR
SATARBIAS_ICH R81LB 24.9 402 1% CH
CAD NOTE:
SATARRBIAS (R81LB): TIE TRACES TOGETHER CLOSE TO PINS, WITH LENGTH NO LONGER THAN 200 MILS TO RESISTOR
DESIGN NOTE:
STUFF R212LB TO BYPASS THERMAL EVENT REPORTING FEATURE (DEFAULT EMPTY)
R59LB 10K 402 5% CH
R214LB 10K 402 5% CH
Q8LB MBT3904DUAL
ICH_THRM_XSTRGATE2
ICH_THRM_XSTRGATE1
H_PROCHOT_N R57LB 10K 402 5% CH
R215LB 0 402 5% EMPTY
XSTR
ICH_THRM_N
DESIGN NOTE:
0-OHM RESISTOR (R212LB) IS IN PLACE SHOULD THE ICH BE MODIFIED TO INCLUDE THRMB PIN ON THE VTT WELL (ON-DIE)
DESIGN NOTE:
MFG MODE PADS: J4LB
R300LB 0 402 5% EMPTY ICH_GP56
R60LB 4.7K 5% CH 402
R225LB 4.7K 5% EMPTY 402
R226LB 1K 402 5% EMPTY
SOP_EN_CNT IM_LB_SOP_EN_CNT
Q12LB EMPTY
J4LB JUMPER EMPTY 726841-001
R302LB 0 402 5% EMPTY GP33_SOP
R303LB 0 402 5% CH GP37_MFG_MODE_N
MBT3904DUAL IM_LB_CONFIG_CNT
R223LB 2.2K 402 5% EMPTY
R224LB 2.2K 402 5% EMPTY
IM_LB_SPKR_CNT Q11LB
RECOVER/CONFIGURE HEADER MODE
JUMPER ON 1-2 * NORMAL
JUMPER ON 2-3 CONFIGURE
JUMPER REMOVED RECOVERY
* DEFAULT JUMPER SETTING
CONFIGURE= SAFE MODE
GP33_SOP R312LB 2.2K 5% CH 402
CR1LB BAT54C DIO SOT23_C
IM_LB_ICH_CONFIG_JUMPER
J7LB 1X3HDR HDR
R227LB 4.7K 402 5% CH ICH_CONFIG_JUMPER
RECOVERY_CONFIGURE_PULLUP
R73LB 470 5% CH 402
R74LB 20K 5% CH 402
R228LB 2.2K 402 5% CH
IM_LB_SPKR
SPKR
CONFIG / RECOVERY JUMPER
BPAGE DRAWING
frostburg_fabc.sch_1.37
Sun Mar 18 18:43:44 2007
[PAGE_TITLE=ICH PIN STRAPS]
INTEL CONFIDENTIAL
DOCUMENT_NUMBER xxxxxx
PAGE 37
REV 3.01
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE
ICH9	0.2.1	08/30/06

PCI

VCC3 C12LB .1UF 20% 25V Y5V 603; C13LB .1UF 20% 25V Y5V 603; C14LB .1UF 20% 25V Y5V 603

PCI-E

VCC3 C16LB .1UF 20% 25V Y5V 603

USB CLASSIC FILTER

IN V_3P3_STBY\G C17LB .022UF 10% 50V X7R 603; C120LB .022UF 10% 50V X7R 603; C18LB .022UF 10% 50V X7R 603

CAD NOTE: PLACE V3P3_STBY DCPL CAPS AT ENDS OF POWER CORRIDOR (VCCP_USB)

IN V_1P5_FILTER C112LB 4.7UF 10% 6.3V X5R 603

CAD NOTE: PLACE C112LB NEAR NE CORNER OF ICH

IN V_1P25_CORE C137LB 22UF 20% 6.3V X5R 1206; C61LB 0.1UF 20% 16V Y5V 402

ICH

VCC3 C15LB .1UF 20% 25V Y5V 603; C20LB .1UF 20% 25V Y5V 603

L1LB 721891-026 10UH IND

SATA PLL FILTER

IN V_1P5_ICH → VCCSATA_PLL_ICH OUT; C21LB 10UF 10% 6.30V X7R 1206; C22LB 1.0UF 20% 10V Y5V 603

CAD NOTE: PLACE VCCSATA DCPL CAPS AT ENDS OF POWER CORRIDOR

PCI-E FILTER

IN V_1P5_ICH → M4LB MULTI CH 805 → V_1P5_FILTER OUT; C23LB 220UF 20% 6.3V ALUM RDL

DESIGN NOTE: DEFAULT M4LB: 0 OHM RES A93552-002 OPTIONAL WITH 0.5UH FB 656554-026

V_1P5_STBY_INT OUT; C35LB 1UF 10% 16V X7R 603

BOM NOTE: 4.7UF (C34LB) STUFF FOR SIGNAL QUALITY

PCI EXPRESS DECOUPLING FILTER

IN V_1P5_FILTER C24LB 22UF 20% 6.3V X5R 1206; C25LB 2.2UF 10% 6.3V X5R 603; C26LB 22UF 20% 6.3V EMPTY 1206

CAD NOTE: V_1P5-FILTER CAPS: PLACE NEAR ENDS OF POWER CORRIDOR

DMI PLL FILTER

IN V_1P5_ICH → M2LB MULTI IND SM → VCCDMI_PLL_ICH OUT; R27LB 0 5% 402 CH; C28LB .01UF 20% 50V X7R 603; C27LB 10.0UF 20% 6.3V X5R 805

DESIGN NOTE: DEFAULT: 1UH INDUCTOR M2LB WITH IPN 201005-546

USB HS (HI-SPEED) FILTER

IN V_1P5_ICH C19LB .1UF 10% 16V X7R 603; C9LB .1UF 10% 16V X7R 603

IN V_3P0_BAT_VREG C39LB .1UF 20% 25V Y5V 603

IN V_REF5V C38LB .1UF 20% 25V Y5V 603

IN V_FSB_VTT C37LB .1UF 20% 25V Y5V 603

IN V_REF5V_SUS C36LB .1UF 20% 25V Y5V 603

CAD NOTE: PLACE 0.1UF DCPL CAPS (C36LB TO C39LB) WITHIN 40 MILS OF ICH.

SATA BG

VCC3 C11LB .1UF 20% 25V Y5V 603

SATA RX/TX

IN V_1P5_ICH C33LB 1UF 20% 6.3V X5R 603; C8LB 1.0UF 20% 10V Y5V 603

IN V_FSB_VTT C29LB 4.7UF 20% 10V Y5V 805; C30LB .1UF 20% 25V Y5V 603

USB VCCUABG

IN V_3P3_STBY\G C32LB .1UF 20% 25V Y5V 603

CAD NOTE: PLACE DCPL CAP (C32LB) AT PIN F3 OF ICH

LAN VCCPAUX

IN V_3P3_EPW C31LB .1UF 20% 25V EMPTY 603

IN V_1P5_ICH → M13LB MULTI IND SM → V_1P5_ICH_R R20LB 0 5% 402 CH → GLCK_PLL OUT; C2LB 10UF 20% 6.3V X5R 805; C3LB 2.2UF 10% 6.3V X5R 603

DESIGN NOTE: DEFAULT: 1UH INDUCTOR M13LB WITH IPN 201005-546; NON-LAN SKU: CHANGE M13LB TO 0OHM RES; NON-LAN SKU: EMPTY C2LB AND C3LB

IN V_1P05_VCCAUX C102LB .1UF 20% 16V Y5V 402; C10LB 1.0UF 20% 10V Y5V 603

V_1P5_CL_INT OUT; C4LB 1.0UF 20% 10V EMPTY 603; C5LB .1UF 20% 25V Y5V 603

V_1P05EP_INT OUT; C6LB 1.0UF 20% 10V EMPTY 603; C7LB .1UF 20% 25V Y5V 603

VCC3 C126LB .1UF 20% 25V Y5V 603; C125LB .1UF 20% 25V Y5V 603

DESIGN NOTE: GENERAL PURPOSE DCPL CAPS

IN V_3P3_EPW → R22LB 0 1A 603 CH → V_3P3_EPW_R OUT; C111LB .1UF 20% 25V Y5V 603; C201LB 0.1UF 20% 16V Y5V 402

DESIGN NOTE: DEFAULT STUFFED: 0 OHM 0603 TRAP (R22LB) OPTION: EMPTY (R22LB) FOR NON-INTEL LAN

R21LB 0 1A EMPTY 603

BOM NOTE: STUFF R21LB FOR NON-INTEL LAN

BPAGE DRAWING

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Sun Mar 18 18:43:46 2007

[PAGE_TITLE=ICH DECOUPLING]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	38	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
ICH9	0.2.1	08/30/06

DESIGN NOTE: VRMPWRGD SEQUENCE CIRCUIT

V_3P3_STBY\G, VCC3, R92LB 1K 5% EMPTY 402, R91LB 10K 5% EMPTY 402, R216LB 10K 5% CH 402, R93LB 1K 5% CH 402, ICH_VRMPWRGD OUT 33

VR_READY, R200LB 0 402 5% CH

SLP_S3_ICH_N, R199LB 0 402 5% EMPTY, SLP_S3_VR_READY, R90LB 10K 402 5% CH, SLP_S3_VR_READY_PIN5

Q2LB MBT3904DUAL, VCC3_3P3STBY_PIN2, C58LB 1.0UF 20% 10V EMPTY 603, R94LB 100K 5% CH 402, XSTR, C59LB 1UF 20% 25V EMPTY 603

BOM NOTE: EMPTY FOR NON-AMT

DESIGN NOTE: CL DEBUG FEATURE, MAY NOT NEED FOR PRODUCT

V_3P3_STBY\G, R97LB 150 5% EMPTY 402, SLP_S3_ICH_N, R194LB 0 402 EMPTY, SLP_M OUT 28 86 88 89

ICH_SLP_M_N, R98LB 10K 402 5% EMPTY, ICH_SLP_M_N_PIN5, Q4LB MMBT3904 EMPTY, C127LB 1.0UF 20% 10V EMPTY 603

BOM NOTE: STUFF R203LB & EMPTY R103LB FOR NON AMT

ICH_RSMRST_N, R203LB 0 402 5% CH

V_3P3_EPW_R, R103LB 15K 402 1% EMPTY, LAN_PWROK OUT 33

R105LB 0 402 5% EMPTY, C119LB 1.0UF 20% 10V EMPTY 603

BOM NOTE: STUFF FOR NON INTEL LAN

SLP_S3_ICH_N, V_3P3_STBY\G, R282LB 402 22 EMPTY 5%

DESIGN NOTE: DEBUG CL FEATURE FORCE MEPWR BEFORE PS_ON IS VALID

R99LB 3.3K 5% EMPTY 402, MCH_CLPWROK_XSTR_GATES, MCH_CLPWROK_DUAL2

Q3LB MBT3904DUAL, MCH_CLPWROK, R100LB 1K 402 5% EMPTY, MCH_CLPWROK_PIN5, EMPTY

CL VREF

V_3P3_EPW, R110LB 3.24K 402 1% CH, R111LB 453 402 1% CH, C56LB 20% 0.1UF 16V Y5V 402, CL_N_VREF_ICH OUT 32

TP5_DEBUG, R87LB 1K 402 5% EMPTY

TP4_DEBUG, R88LB 1K 402 5% EMPTY

DESIGN NOTE: DEBUG PURPOSE.

V_3P3_STBY\G, R108LB 1K 402 1% EMPTY, R109LB 3.24K 402 1% EMPTY, C57LB 20% 0.1UF 16V EMPTY 402, TP6_DEBUG OUT 32

[PAGE_TITLE=ME & CONTROL BUFFERS/ICH CIRCUITS]

BPAGE DRAWING

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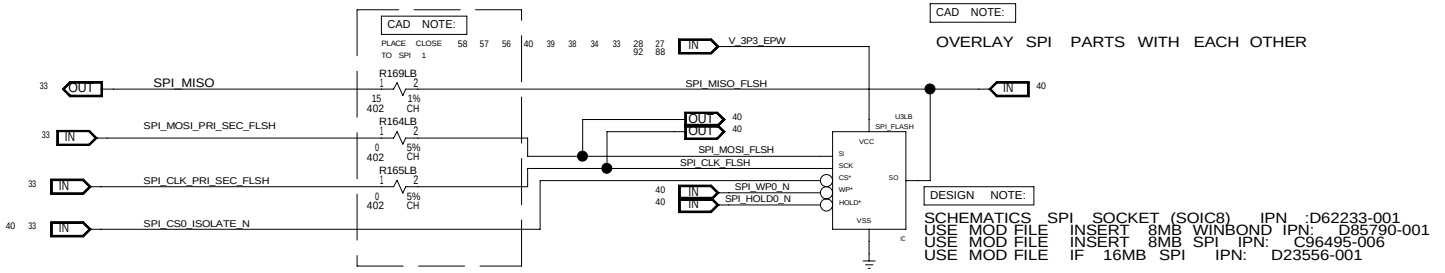
Sun Mar 18 18:43:47 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	39	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
ICH9	0.2.1	08/30/06

PRIMARY SERIAL FLASH



CAD NOTE:

OVERLAY SPI PARTS WITH EACH OTHER

DESIGN NOTE:

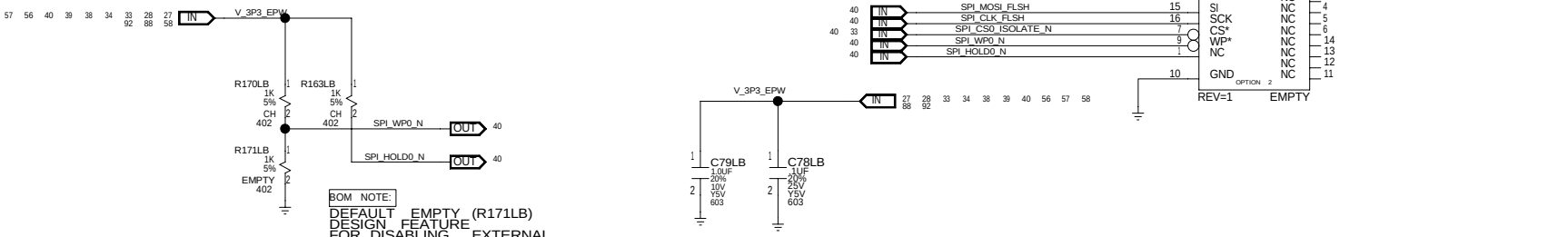
SCHEMATICS SPI SOCKET (SOIC8) IPN :D62233-001
USE MOD FILE INSERT 8MB WINBOND IPN: D85790-001
USE MOD FILE INSERT 8MB SPI IPN: C96495-006
USE MOD FILE IF 16MB SPI IPN: D23556-001

DESIGN NOTE:

OVERLAPPING PARTS: ONLY STUFF ONE(XU3LB) OR (U2LB)

CAD NOTE:

OVERLAY SPI (XU3LB) & (U2LB) WITH EACH OTHER



BOM NOTE:

DEFAULT EMPTY (R171LB)
DESIGN FEATURE
FOR DISABLING EXTERNAL
FLASH PROTECTION

[MODULE=ICH]

[PAGE_TITLE=SERIAL FLASH PRIMARY]

BPAGE DRAWING

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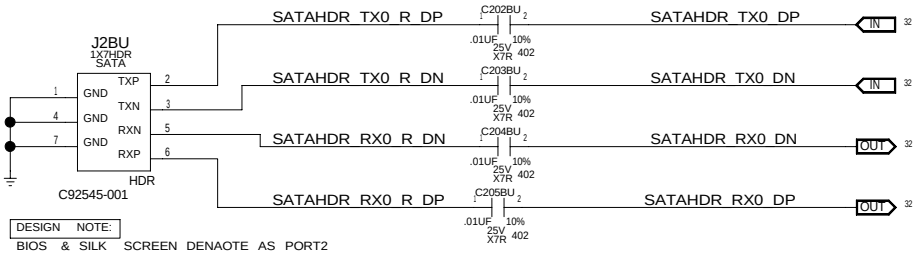
Sun Mar 18 18:43:49 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	40	3.01

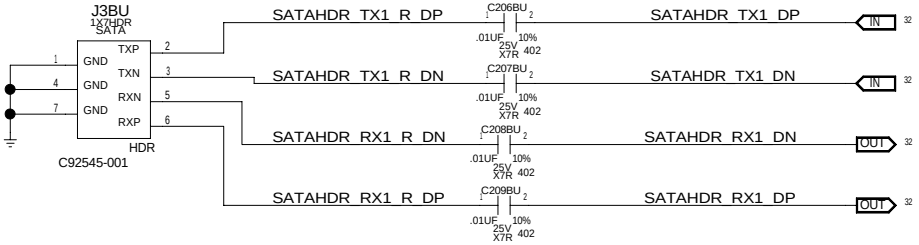
MODULE_REV_DETAILS		
MODULE_NAME	REV	DATE

BOM NOTE:
DEFAULT 0.01UF, 0402, A36096-008, 10%, 25V, X7R
OPTIONAL 0 OHM, 0402, A36093-001

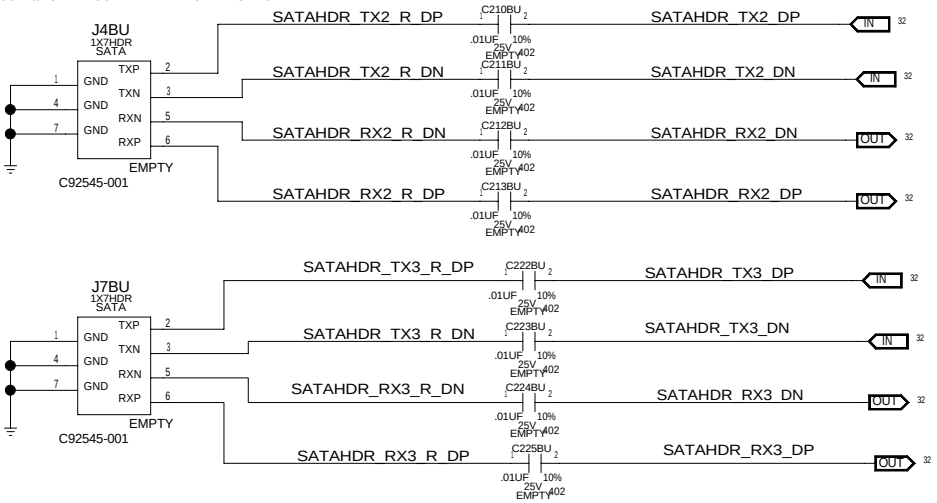
DESIGN NOTE:
BIOS & SILK SCREEN DENAOTE AS PORT0



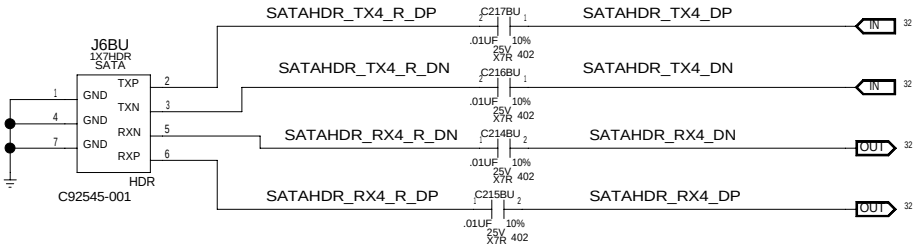
DESIGN NOTE:
BIOS & SILK SCREEN DENAOTE AS PORT2



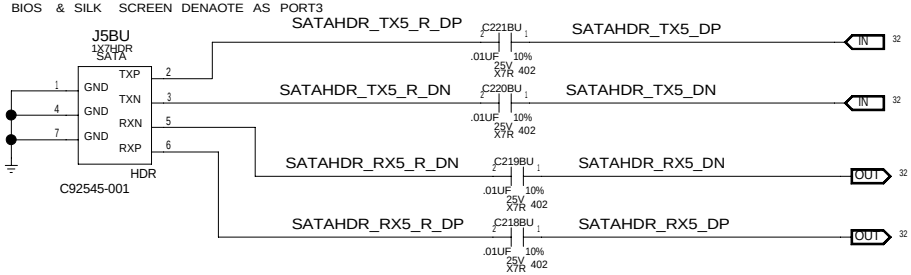
DESIGN NOTE:
BIOS & SILK SCREEN DENAOTE AS PORT4



DESIGN NOTE:
BIOS & SILK SCREEN DENAOTE AS PORT1



DESIGN NOTE:
BIOS & SILK SCREEN DENAOTE AS PORT3



BPAGE DRAWING
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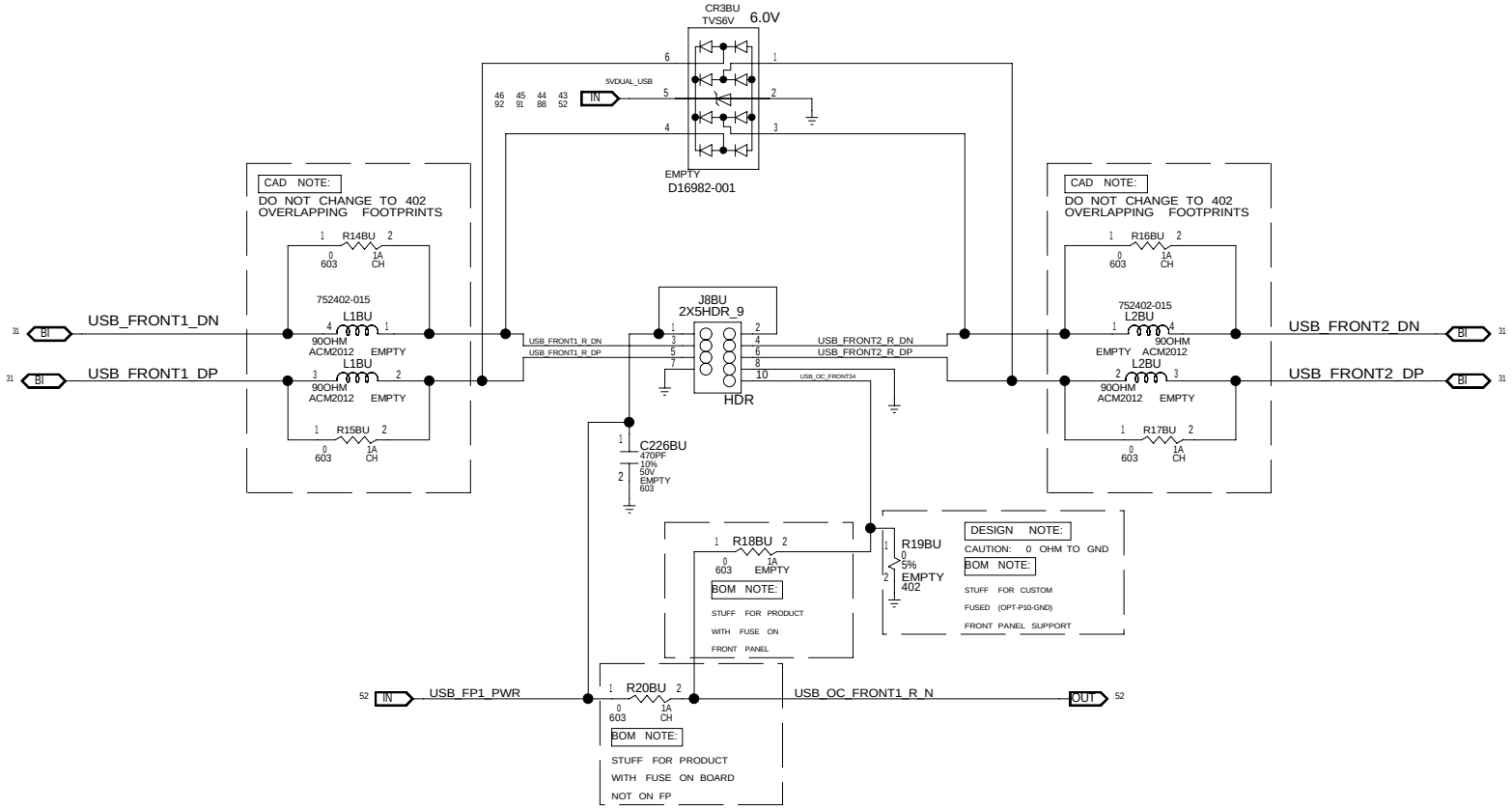
Sun Mar 18 18:43:50 2007

[PAGE_TITLE=SATA CONNECTORS]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	41	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE

FRONT PANEL HEADER #1



[PAGE_TITLE=USB FP HDR 1]

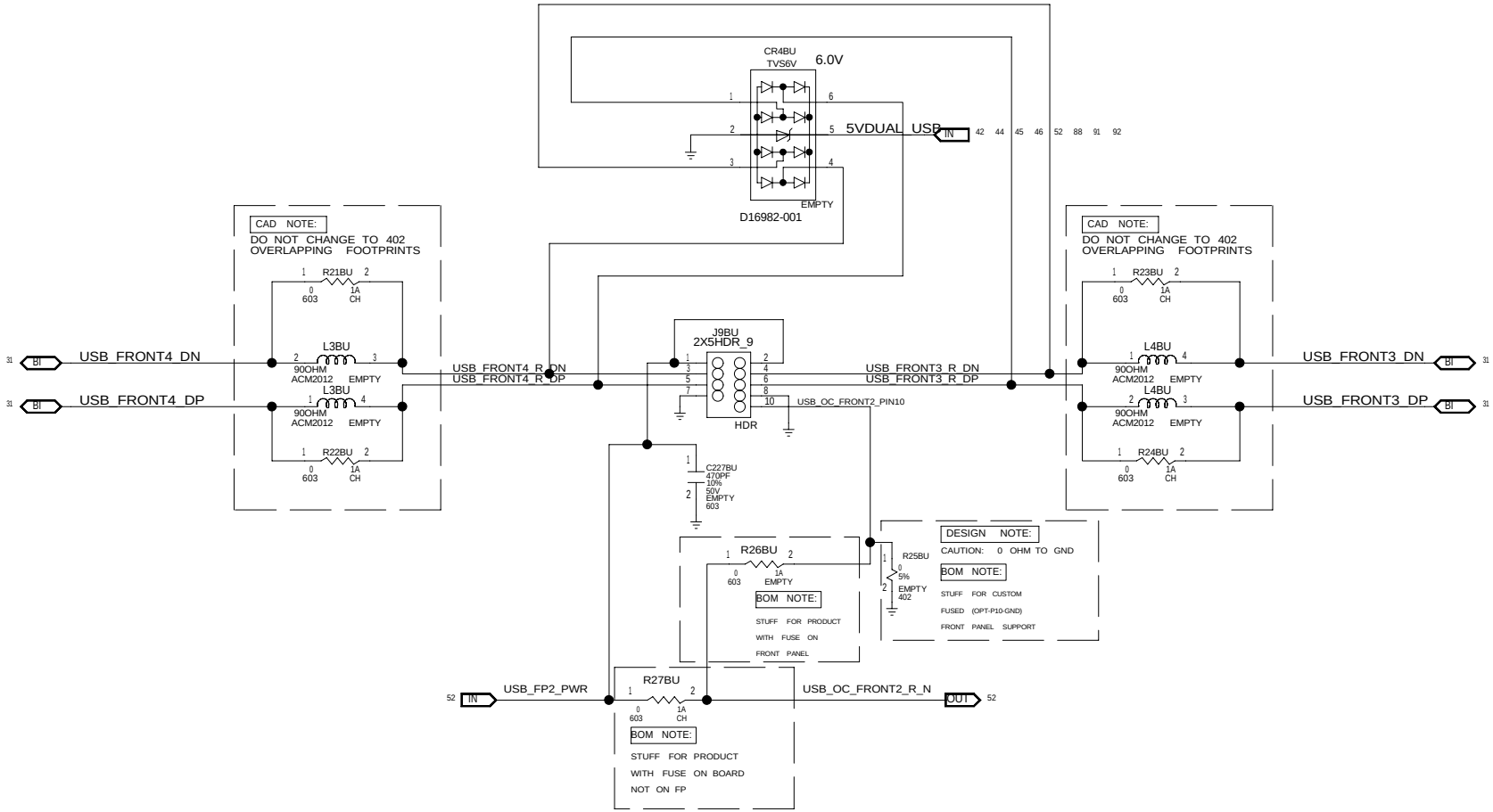
BPAGE DRAWING

frostburg_fabc.sch_1.42
Sun Mar 18 18:43:51 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	42	3.01

FRONT PANEL HEADER #2

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=USB FP HDR 2]

BPAGE DRAWING

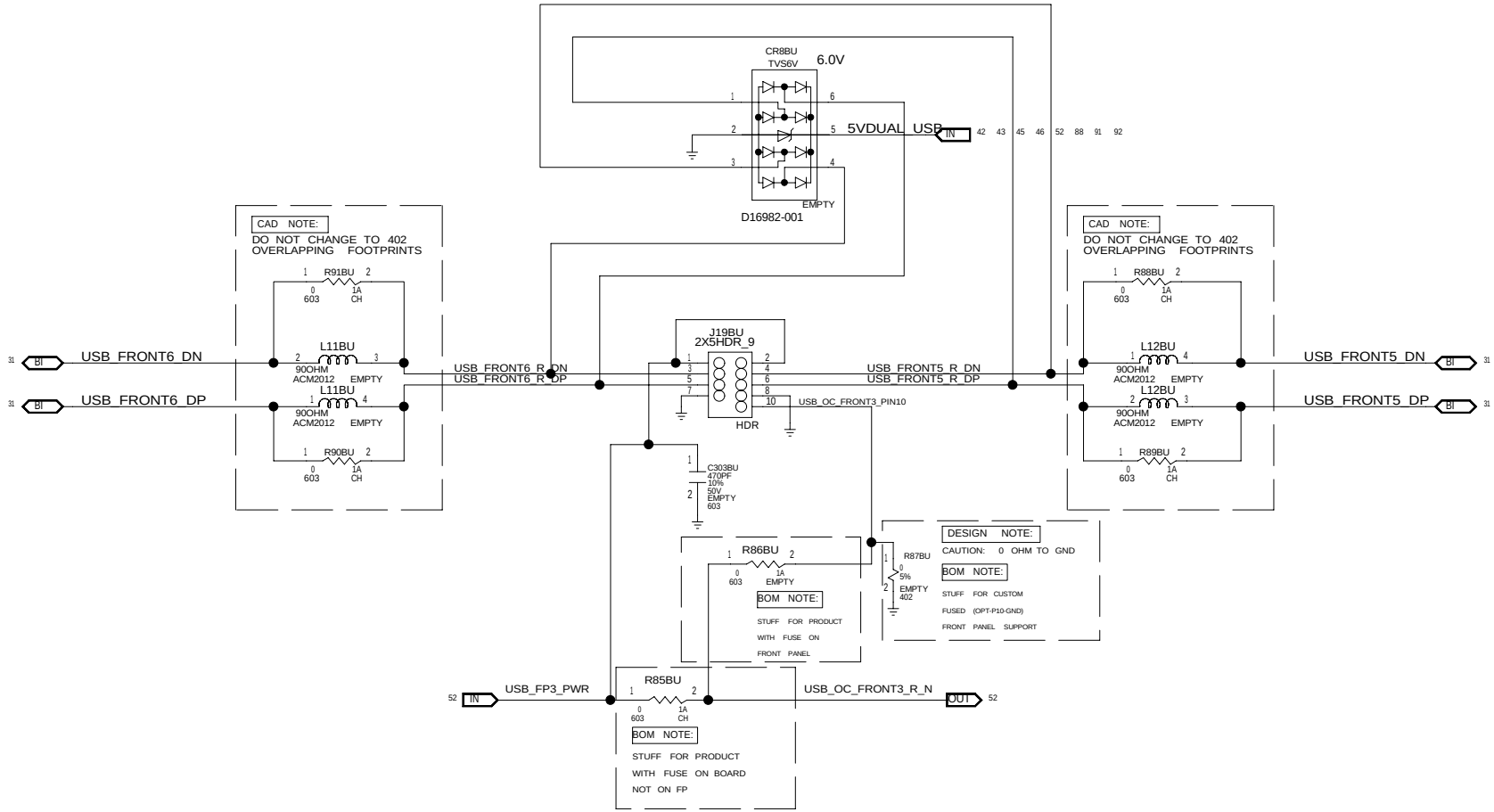
frostburg_fabc.sch_1.43
Sun Mar 18 18:43:52 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	43	3.01

CUSTOM TEXT 2 BPAGE

FRONT PANEL HEADER #3

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=USB FP HDR 2]

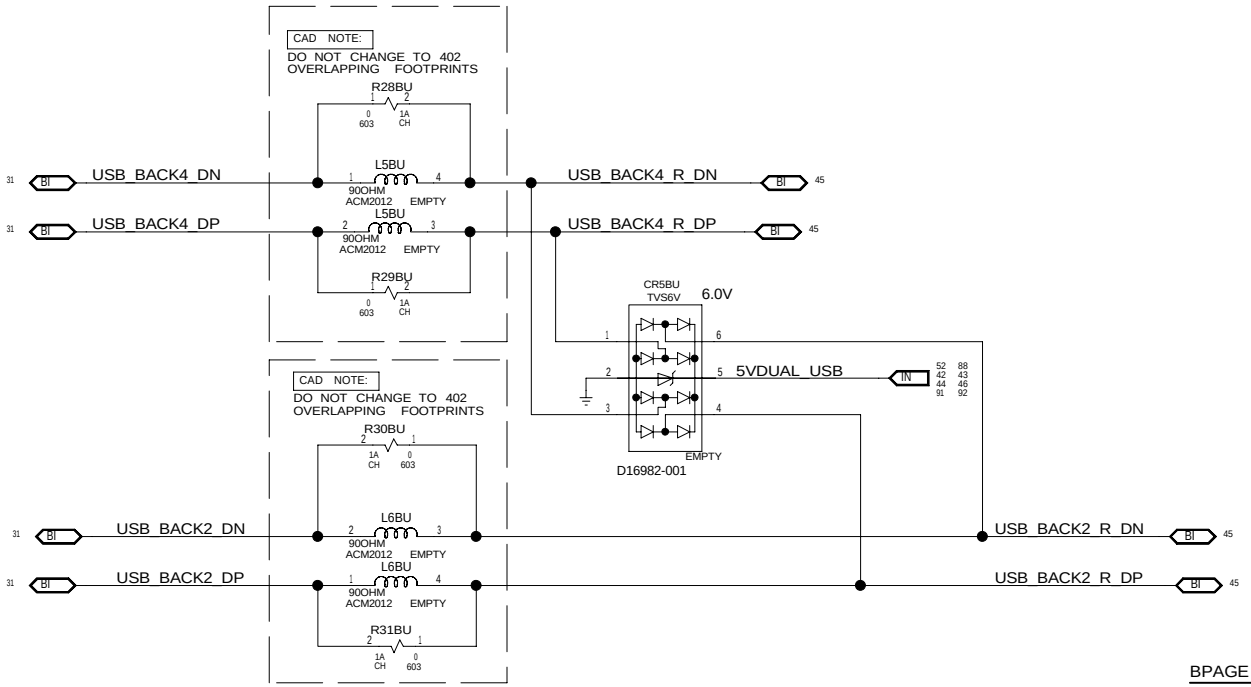
BPAGE DRAWING

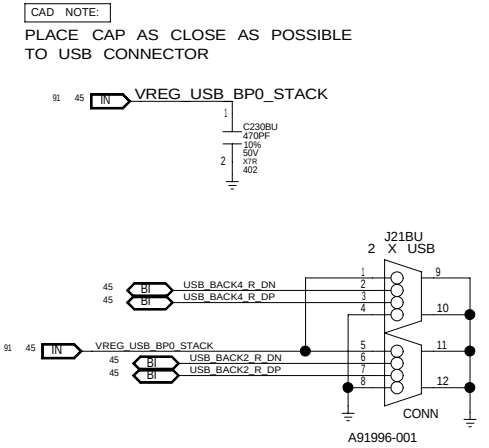
frostburg_fabc.sch_1.44
Sun Mar 18 18:43:53 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	44	3.01

BACK PANEL USB

MODULE REV DETAILS		
MODULE NAME	REV	DATE





[PAGE_TITLE=BACK PANEL USB]

BPAGE DRAWING

frostburg_fabc.sch_1.45
Sun Mar 18 18:43:54 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	45	3.01

[PAGE_TITLE=BACK PANEL USB WITH ESATA]

MODULE REV DETAILS

MODULE NAME	REV	DATE

DESIGN NOTE:
MJ/USB DUAL

CAD NOTE:
DO NOT CHANGE TO 402 OVERLAPPING FOOTPRINTS

BOM NOTE:
CONNECTOR STUFFING OPTIONS:

RJ45/2 USB - C73572-001 (DEFAULT)
DOUBLE STACK USB - 749193-001, NOT 642575-124

DOUBLE-STACK CONNECTOR FOR USB/LAN IS ON OTHER PAGE WITH THE REST OF THE CONNECTOR

R32BU 0 603 1A CH
R33BU 0 603 1A CH
R34BU 0 603 1A CH
R35BU 0 603 1A CH

L7BU 90OHM ACM2012 EMPTY
L8BU 90OHM ACM2012 EMPTY

CR6BU TVS6V 6.0V EMPTY

31 BI USB_BACK1_DN → USB_BACK1_R_DN BI 46 57
31 BI USB_BACK1_DP → USB_BACK1_R_DP BI 46 57
31 BI USB_BACK3_DN → USB_BACK3_R_DN BI 46 57
31 BI USB_BACK3_DP → USB_BACK3_R_DP BI 46 57

5VDUAL_USB IN 42 43 44 45 46 52 88 91 92

CAD NOTE:
OVERLAP WITH MAGJACK FOOTPRINT

BOM NOTE:
EMPTY, EXCEPT FOR USB W/NO-LAN OPTION
CONNECTOR STUFFING OPTIONS:
RJ45/2 USB - A11509-001 (OLDER DESIGNS, PRE-GIGABIT LAN)
DOUBLE STACK USB (NO LAN) - 749193-001

J11BU 2 X USB
91 57 46 IN VREG_USB_BP_MJ
57 46 BI USB_BACK1_R_DN
57 46 BI USB_BACK1_R_DP
91 57 46 IN VREG_USB_BP_MJ
57 46 BI USB_BACK3_R_DN
57 46 BI USB_BACK3_R_DP
EMPTY

CAD NOTE:
PLACE CAP AS CLOSE AS POSSIBLE TO USB CONNECTOR

91 57 46 IN VREG_USB_BP_MJ
C405BU 470PF 10% 50V EMPTY 402
C229BU 470PF 10% 50V X7R 402

DESIGN NOTE:
USB/ESATA DUAL STACK

R36BU 0 603 1A CH
R37BU 0 603 1A CH
R38BU 0 603 1A CH
R39BU 0 603 1A CH

L9BU 90OHM ACM2012 EMPTY
L10BU 90OHM ACM2012 EMPTY

CAD NOTE:
DO NOT CHANGE TO 402 OVERLAPPING FOOTPRINTS

31 BI USB_BACK5_DN → USB_BACK5_R_DN BI 46
31 BI USB_BACK5_DP → USB_BACK5_R_DP BI 46
31 BI USB_BACK6_DP → USB_BACK6_R_DP BI 46
31 BI USB_BACK6_DN → USB_BACK6_R_DN BI 46

CR7BU TVS6V 6.0V EMPTY

45 44 43 92 42 91 88 52 46 IN 5VDUAL_USB

CAD NOTE:
PLACE CAP AS CLOSE AS POSSIBLE TO USB CONNECTOR

91 46 IN VREG_USB_BP1_STACK
C228BU 470PF 10% 50V X7R 402

J12BU 2 X USB
91 46 IN VREG_USB_BP1_STACK
46 BI USB_BACK6_R_DN
46 BI USB_BACK6_R_DP
46 BI USB_BACK5_R_DN
46 BI USB_BACK5_R_DP
CONN
A91996-001

BPAGE DRAWING
frostburg_fabc.sch_1.46
Sun Mar 18 18:43:56 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	46	3.01

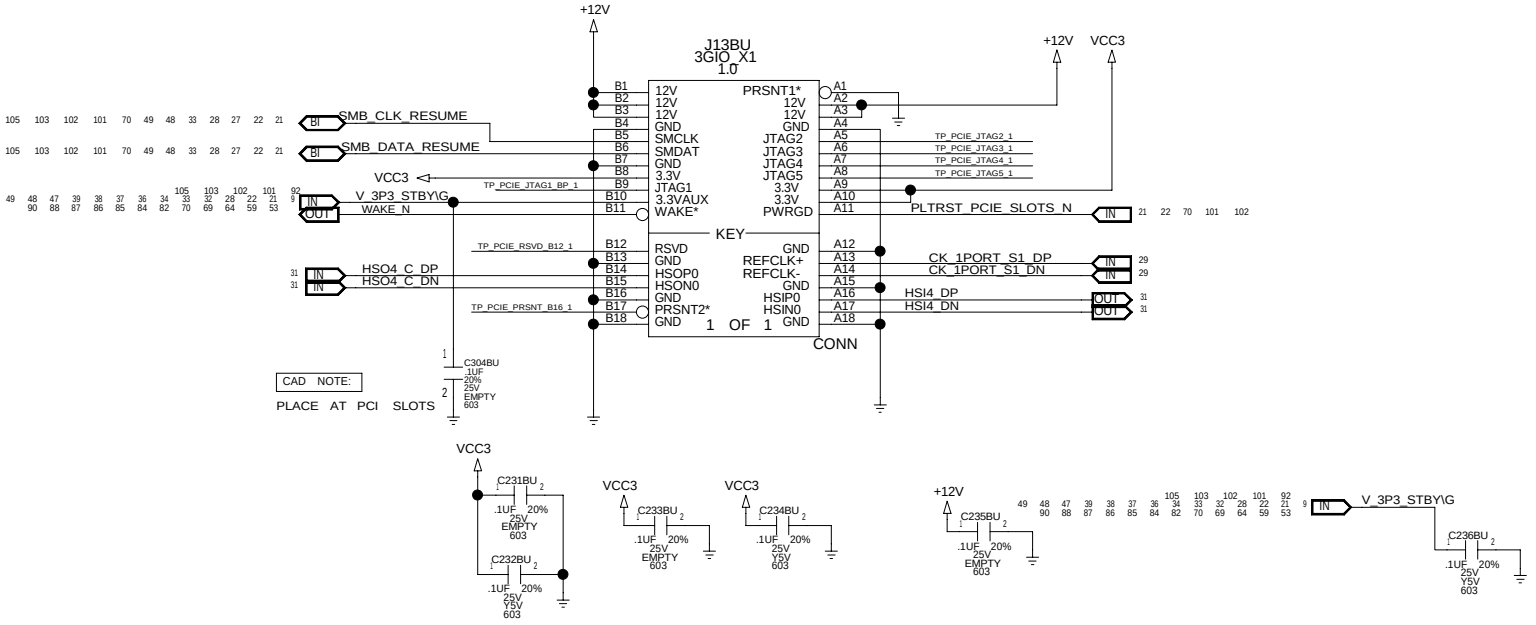
MODULE REV DETAILS		
MODULE NAME	REV	DATE

EXPANSION SLOT 2

CAD NOTE:

PCI-E X1 SLOT 1 CLOSEST TO PEGX16

PCI EXPRESS
1-PORT



[PAGE_TITLE=PCI EXPRESS X1 #1]

BPAGE DRAWING

frostburg_fabc.sch_1.47
Sun Mar 18 18:43:58 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	47	3.01

CUSTOM TEXT 2 BPAGE

EXPANSION SLOT 3

PCI SLOT 1

J20BU
PCI CONN2_2 CONN

MODULE REV DETAILS

MODULE NAME	REV	DATE

NOTE: PCI SLOTS= VCC3 SHOULD GET 470UF DECOUPLING,
VCC SHOULD GET 100UF (ALLOWS 1000UF OPTION FOR VCC3)

DESIGN NOTE:
PCI2.2 COMPATIBLE

DESIGN NOTE:
IRQ MAP
IRQ MAP A B C D
F G H E
IDSEL 16
REQ/GNT 0

NC=1,2

[PAGE_TITLE=PCI CONN 1]

BPAGE DRAWING
frostburg_fabc.sch_1.48
Sun Mar 18 18:44:00 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	48	3.01

CUSTOM TEXT 2 BPAGE

EXPANSION SLOT 4 (FURTHEST FROM CPU)

PCI SLOT 2

J15BU
PCI CONN2_2 CONN

MODULE REV DETAILS

MODULE NAME	REV	DATE

NOTE: PCI SLOTS= VCC3 SHOULD GET 470UF DECOUPLING,
VCC SHOULD GET 100UF (ALLOWS 1000UF OPTION FOR VCC3)

DESIGN NOTE:
PCI2.2 COMPATIBLE

DESIGN NOTE:
IRQ MAP
IRQ MAP A B C D
G F E H
IDSEL 17
REQ/GNT 1

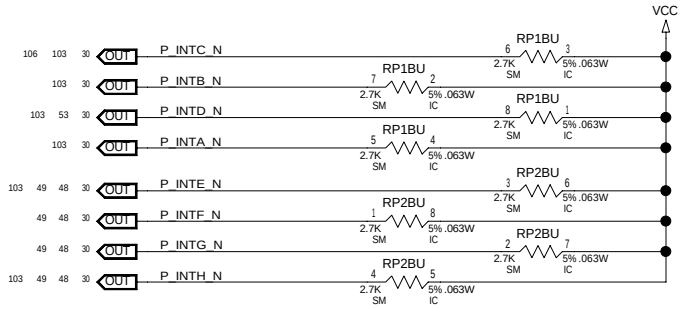
[PAGE_TITLE=PCI CONN 2]

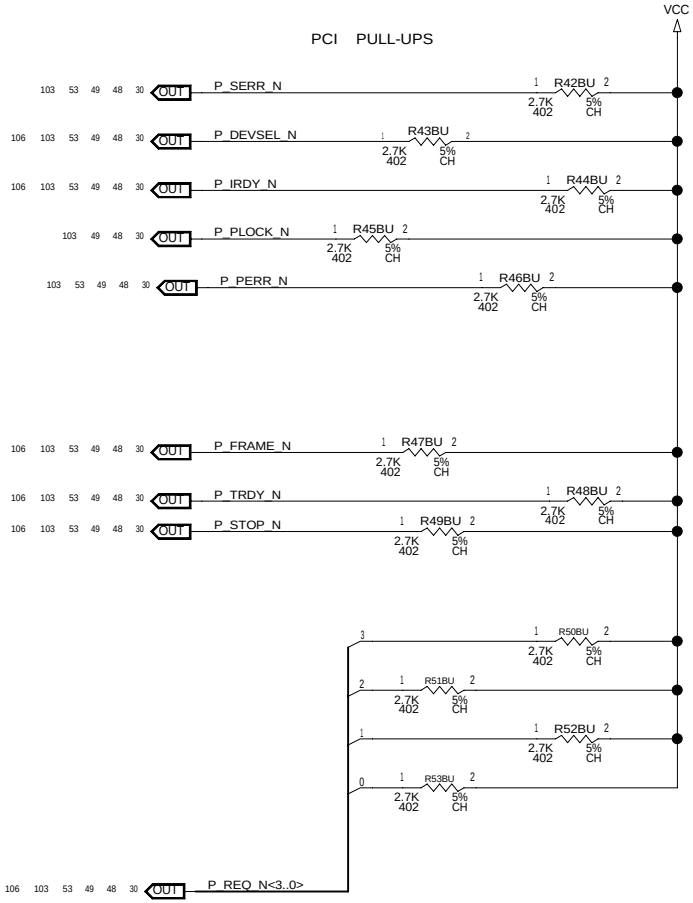
BPAGE DRAWING
frostburg_fabc.sch_1.49
Sun Mar 18 18:44:02 2007

INTEL CONFIDENTIAL | DOCUMENT_NUMBER xxxxxx | PAGE 49 | REV 3.01

CUSTOM TEXT 2 BPAGE

MODULE_REV_DETAILS		
MODULE_NAME	REV	DATE





[PAGE_TITLE=PCI TERMINATION]

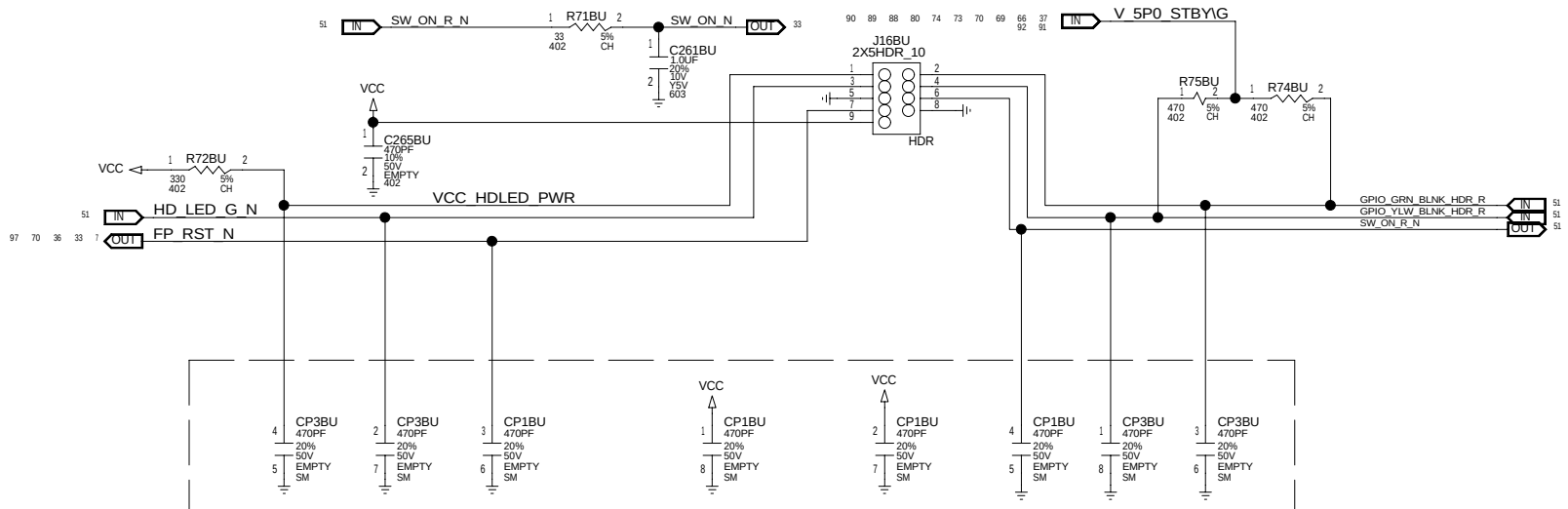
BPAGE DRAWING

frostburg_fabc.sch_1.50
Sun Mar 18 18:44:04 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	50	3.01

CUSTOM TEXT BPAGE

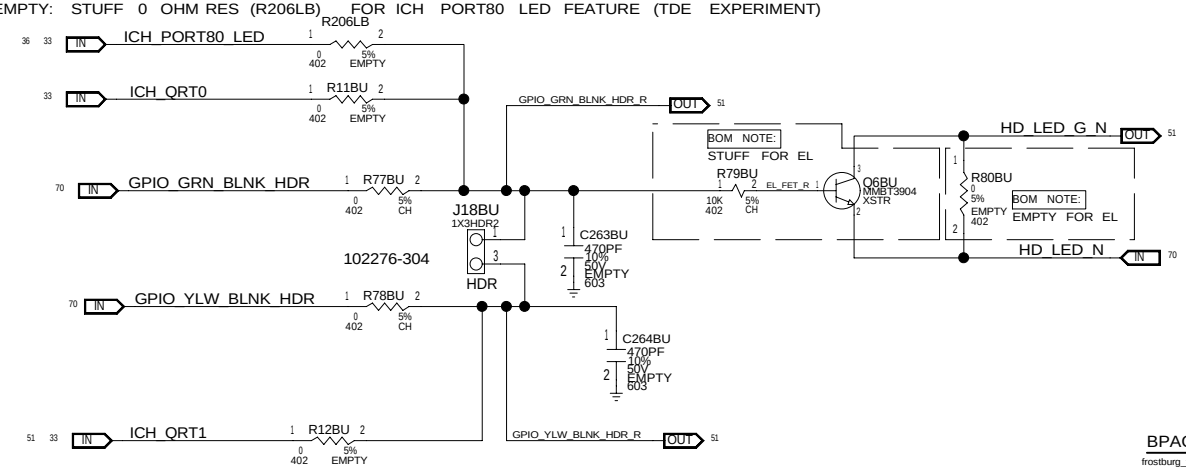
MODULE_REV_DETAILS		
MODULE_NAME	REV	DATE

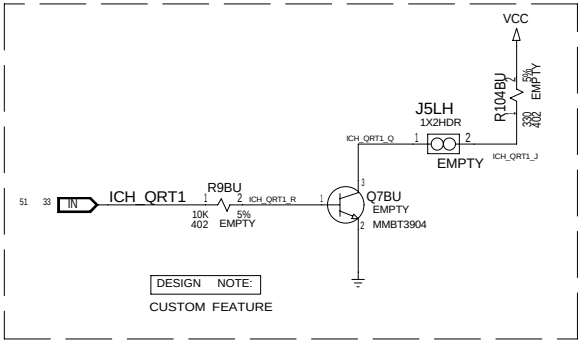


BOM_NOTE:

BOM=CORE_STDFNTPNL_E

DEFAULT EMPTY: STUFF 0 OHM RES (R206LB) FOR ICH PORT80 LED FEATURE (TDE EXPERIMENT)





[PAGE_TITLE=STD FRONT PANEL HDR]

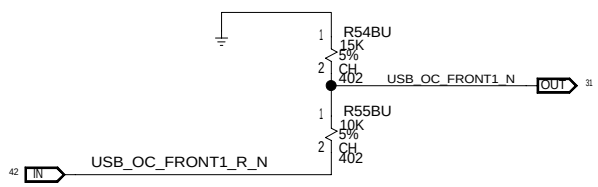
BPAGE_DRAWING

frostburg_fabc.sch_1.51
Sun Mar 18 18:44:06 2007

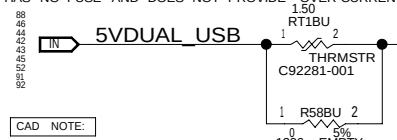
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	51	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE

FRONT PANEL POWER #1

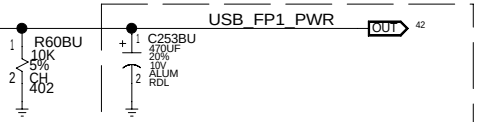


DESIGN NOTE:
STUFFING THE THERMISTOR ASSUMES FRONT PANEL CARD HAS NO FUSE AND DOES NOT PROVIDE OVER-CURRENT PROTECTION



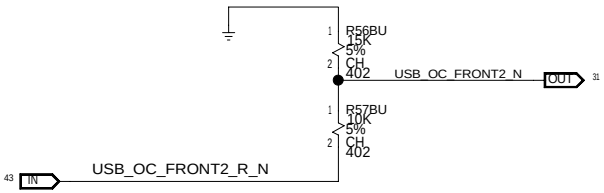
CAD NOTE:
DUAL FOOTPRINT: PLACE 0 OHM 1206 IN PARALLEL WITH THERMISTOR

BOM NOTE:
STUFF 0 OHM INSTEAD OF THERMISTOR FOR PRODUCT WITH FUSE ON FRONT PANEL

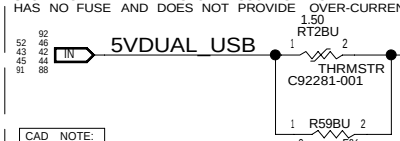


CAD NOTE:
PLACE DECOUPLING AS CLOSE AS POSSIBLE TO USB CONNECTOR

FRONT PANEL POWER #2

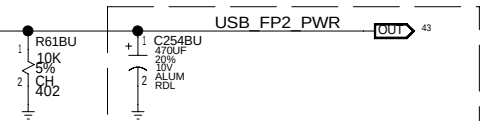


DESIGN NOTE:
STUFFING THE THERMISTOR ASSUMES FRONT PANEL CARD HAS NO FUSE AND DOES NOT PROVIDE OVER-CURRENT PROTECTION



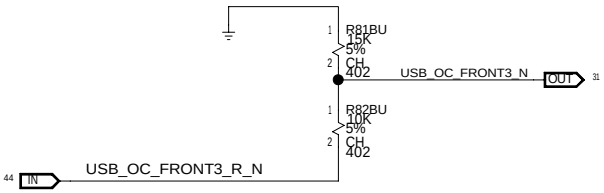
CAD NOTE:
DUAL FOOTPRINT: PLACE 0 OHM 1206 IN PARALLEL WITH THERMISTOR

BOM NOTE:
STUFF 0 OHM INSTEAD OF THERMISTOR FOR PRODUCT WITH FUSE ON FRONT PANEL

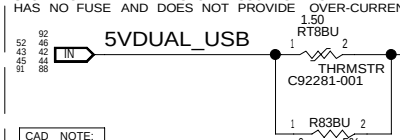


CAD NOTE:
PLACE DECOUPLING AS CLOSE AS POSSIBLE TO USB CONNECTOR

FRONT PANEL POWER #3

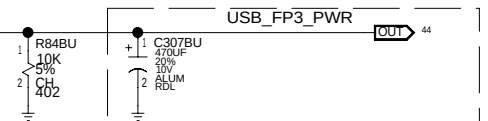


DESIGN NOTE:
STUFFING THE THERMISTOR ASSUMES FRONT PANEL CARD HAS NO FUSE AND DOES NOT PROVIDE OVER-CURRENT PROTECTION



CAD NOTE:
DUAL FOOTPRINT: PLACE 0 OHM 1206 IN PARALLEL WITH THERMISTOR

BOM NOTE:
STUFF 0 OHM INSTEAD OF THERMISTOR FOR PRODUCT WITH FUSE ON FRONT PANEL

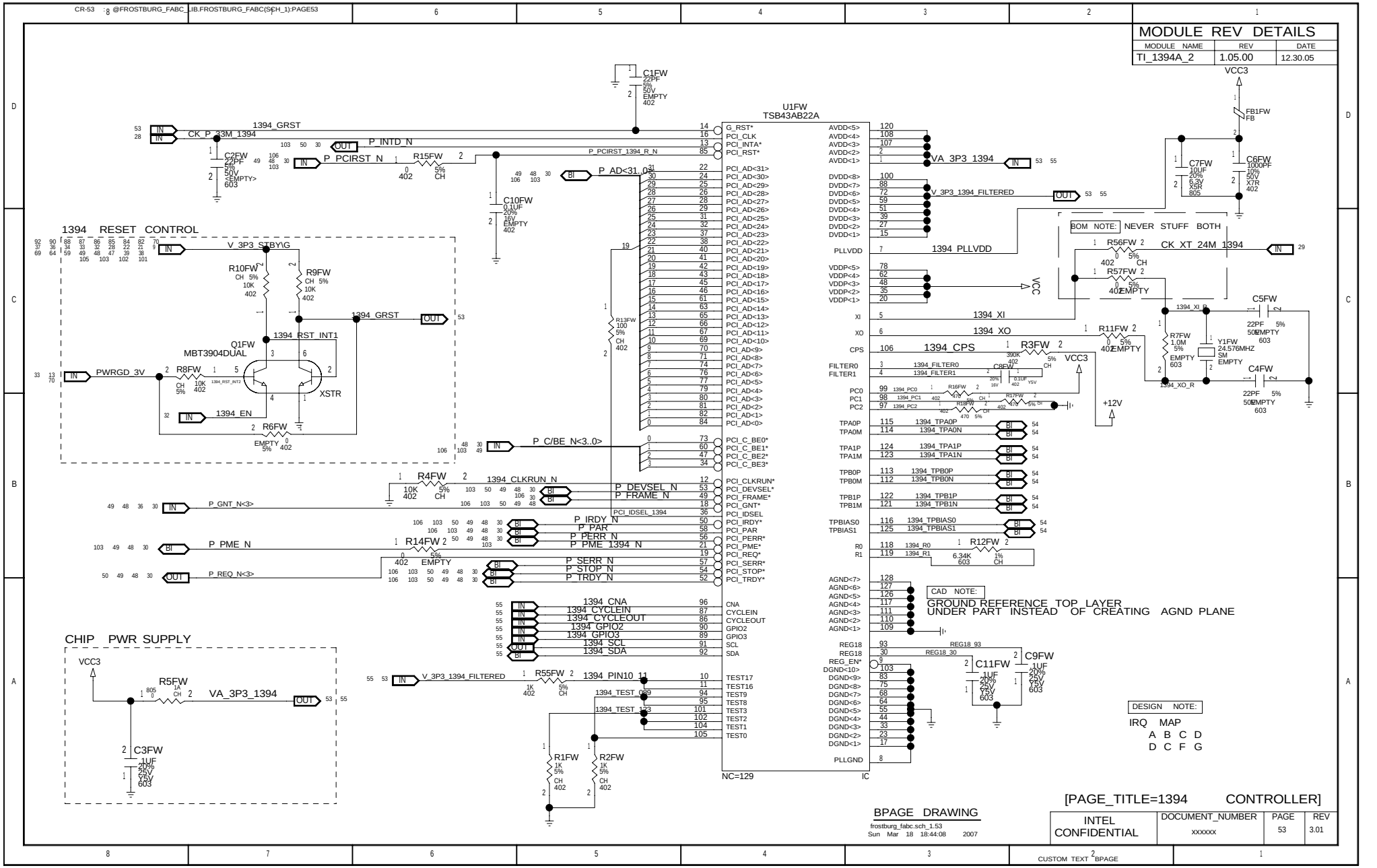


CAD NOTE:
PLACE DECOUPLING AS CLOSE AS POSSIBLE TO USB CONNECTOR

[PAGE_TITLE=USB_FP_HEADER_POWER]

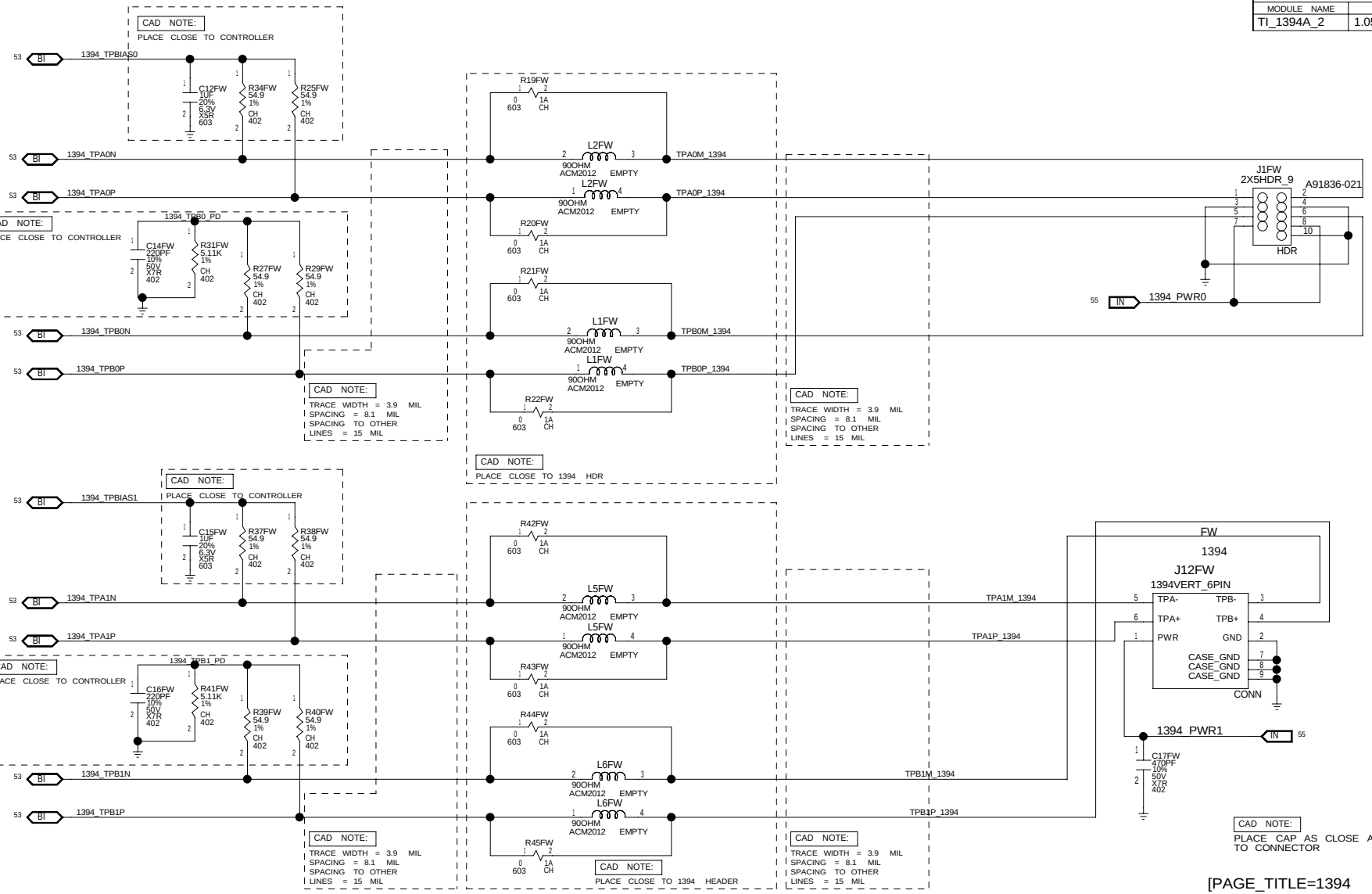
BPAGE DRAWING
frostburg_fabc.sch_1.52
Sun Mar 18 18:44:07 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	52	3.01


MODULE REV DETAILS
MODULE NAME | REV | DATE
TI_1394A_2 | 1.05.00 | 12.30.05
U1FW
TSB43AB22A
1394 RESET CONTROL
CHIP PWR SUPPLY
BOM NOTE: NEVER STUFF BOTH
CAD NOTE:
GROUND REFERENCE TOP LAYER
UNDER PART INSTEAD OF CREATING AGND PLANE
DESIGN NOTE:
IRQ MAP
A B C D
D C F G
BPAGE DRAWING
frostburg_fabc.sch_1.53
Sun Mar 18 18:44:08 2007
[PAGE_TITLE=1394 CONTROLLER]
INTEL CONFIDENTIAL
DOCUMENT_NUMBER
xxxxxx
PAGE
53
REV
3.01
CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS

MODULE NAME	REV	DATE
TI_1394A_2	1.05.00	12.30.05



BPAGE DRAWING

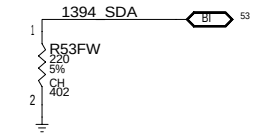
frostburg_fabc.sch_1.54
Sun Mar 18 18:44:10 2007

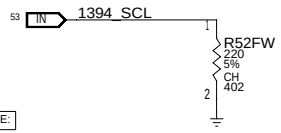
[PAGE_TITLE=1394 BP REV1]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	54	3.01

CR-55 : 8 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(SCH_1):PAGE55

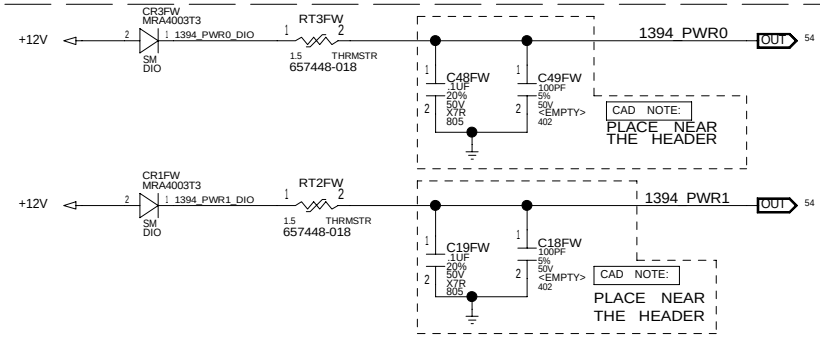
MODULE REV DETAILS		
MODULE NAME	REV	DATE
TI_1394A_2	1.05.00	12.30.05

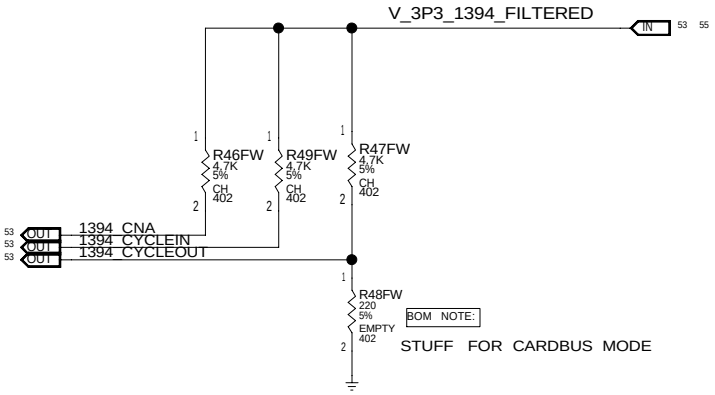


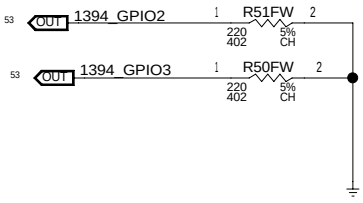


BOM NOTE:
STUFF BOTH RESISTORS FOR 1394 DOWN W/O EEPROM

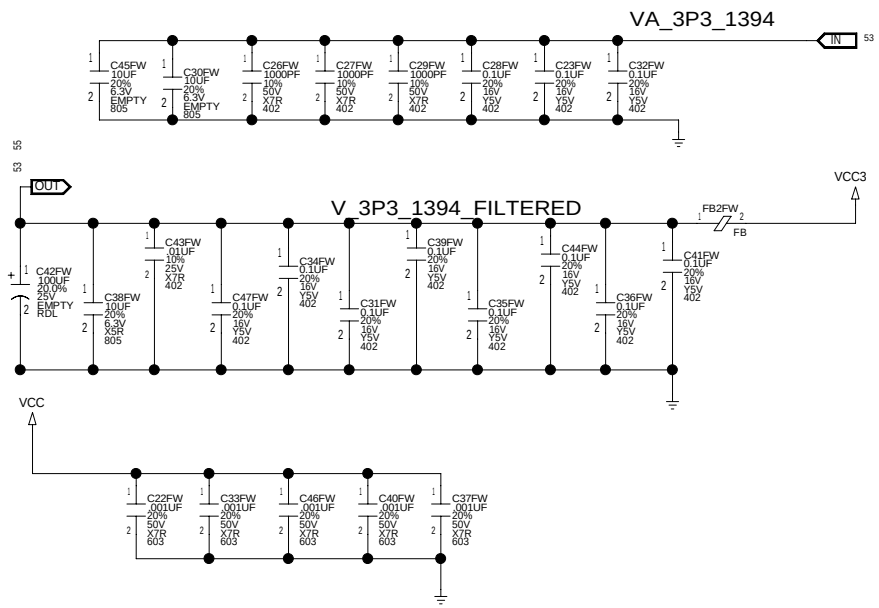
EEPROM







- GLOBAL RESET IS A POWER ON RESET
- 1394 CONTROLLER IS COMPLETELY NON-FUNCTIONAL WHEN ASSERTED
- ALL REGISTERS ARE SET TO THEIR DEFAULT STATES, INCLUDING ONES NOT RESET BY PCI_RST



1394 DECOUPLING

BPAGE DRAWING
[PAGE_TITLE=1394 PWR/DCPL] frostburg_fabc.sch_1.55
Sun Mar 18 18:44:11 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	55	3.01

CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_INTEL_LAN	01.03.00	12-08-06

BOM NOTE:
FOR EKRON USE IPN D23402-001

D20909-002
U1LN
NINEVEH0P99B

56 OUT	HSI6_DP	H2	GLAN_TXP/NC	MDI_PLUS0/TDP	B8 LAN_MDI0_DP BI 57
56 OUT	HSI6_DN	J2	GLAN_TXN/NC	MDI_MINUS0/TDN	B9 LAN_MDI0_DN BI 57
31 IN	HSO6_C_DP	J4	GLAN_RXP/NC	MDI_PLUS1/RDP	D9 LAN_MDI1_DP BI 57
31 IN	HSO6_C_DN	H4	GLAN_RXN/NC	MDI_MINUS1/RDN	D8 LAN_MDI1_DN BI 57
	TP_LAN_J6	J6	RSVD_J6/NC	MDI_PLUS2/NC	F9 LAN_MDI2_DP BI 57
	TP_LAN_J7	J7	RSVD_J7/NC	MDI_MINUS2/NC	F8 LAN_MDI2_DN BI 57
56 IN	KMRN_RCOMP_DP	G7	KBIAS_P/RBIAS100	MDI_PLUS3/NC	H8 LAN_MDI3_DP BI 57
56 IN	KMRN_RCOMP_DN	H7	KBIAS_N/RBIAS10	MDI_MINUS3/NC	H9 LAN_MDI3_DN BI 57
	LAN_RBIAS_P	E7	RBIAS_P/NC	JTXD0	D1 ICH_LAN_JTX0 IN 33
		E6	RBIAS_N/NC	JTXD1	F3 ICH_LAN_JTX1 IN 33
	TP_LAN_1P0_CTRL	C3	CTRL_10/NC	JTXD2	F1 ICH_LAN_JTX2 IN 33
58 OUT	LAN_1P8_CTRL	B2	CTRL_18/NC	JRXD0	D3 ICH_LAN_JRX0 OUT 33
	TP_LAN_THERM_DP	A2	THERM_D_P/NC	JRXD1	D2 ICH_LAN_JRX1 OUT 33
	TP_LAN_THERM_DN	A3	THERM_D_N/NC	JRXD2	C1 ICH_LAN_JRX2 OUT 33
	IEEE_TEST_LAN_P	A7	IEEE_TEST_P/NC	JKCLK/JCLK	E2 ICH_LAN_JCLK_R OUT 56
	IEEE_TEST_LAN_N	B7	IEEE_TEST_N/NC	JRSTSYNC	E3 ICH_LAN_JRST IN 33
56 IN	LAN_ISOL_TCK_R	G1	JTAG_TCK/ISOL_TCK	LED0/LINK_UP*	A4 LAN_LED0 OUT 57
56 IN	LAN_ISOL_TI_R	H1	JTAG_TDI/ISOL_TI	LED1/ACT_LED*	B4 LAN_LED1 OUT 57
	TP_LAN_JTDO_G3	G3	JTAG_TDO/TOUT	LED2/SPEED_LED*	A5 LAN_LED2 OUT 57
56 IN	LAN_ISOL_EXEC_R	G2	JTAG_TMS/ISOL_EXEC	XTAL1/X1	H6 LAN_XTL_DP IN 56
				XTAL2/X2	H5 LAN_XTL_DN OUT 56
				TEST_EN	B6 LAN_TESTEN IN 56
				RSVD	B5 TP_LAN_TEST0
				RSVD_A6/ADV10-LAN_DIS*	A6 LAN_DISABLE_N_R IN 56
				RSVD_C5/NC	C5 TP_LAN_C5

1 of 2
IC

BOM NOTE:
STUFF FOR NINEVEH
EMPTY FOR EKRON

R5LN 1.4K 1% 402 CH

01.03.00
INTEL_LAN

R6LN
RES_TESTPROBE
A B
EMPTY

BOM NOTE:
EKRON MODE SELECT OPTIONS: FOLLOW BELOW FOR RESISTOR STUFFING CONFIGURATION

	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4
TESTEN	NOT SUPPORTED	0 (EXTERNAL)	1 (EXTERNAL)	1 (EXTERNAL)	1 (EXTERNAL)
ISOL_TCK	NOT SUPPORTED	0 (INTERNAL)	0 (EXTERNAL)	0 (INTERNAL)	1 (EXTERNAL)
ISOL_TI	NOT SUPPORTED	1 (EXTERNAL)	0 (EXTERNAL)	1 (EXTERNAL)	0 (INTERNAL)
ISOL_EXEC	NOT SUPPORTED	1 (EXTERNAL)	1 (EXTERNAL)	1 (EXTERNAL)	0 (INTERNAL)

33 IN V_3P3_EPW
R36LN 220 5% 2 EMPTY 402
R37LN 220 5% 2 EMPTY 402
R45LN 220 5% 2 EMPTY 402
R41LN 220 5% 2 EMPTY 402
LAN_TESTEN OUT 56
LAN_ISOL_TCK_R OUT 56
LAN_ISOL_TI_R OUT 56
LAN_ISOL_EXEC_R OUT 56
R39LN 1K 5% 2 EMPTY 402
R40LN 1K 5% 2 EMPTY 402
R11LN 100 5% 2 CH 402

BOM NOTE:
STUFF R11LN FOR NINEVEH
ALL OTHERS ARE EMPTY

BOM NOTE:
PLACE JCLK TERMINATION (R16LN) CLOSE TO LAN

33 OUT ICH_LAN_JCLK — R16LN 33 402 5% CH — ICH_LAN_JCLK_R IN 56
TO ICH
FROM LAN

R38LN 0 603 1A EMPTY
33 IN LAN_DISABLE_N — LAN_DISABLE_N_R OUT 56

BOM NOTE:
STUFF 0 OHM STRAP (BETWEEN LAN_DISABLE_N AND LAN_DISABLE_N_R FOR EKRON
EMPTY FOR NINEVEH

56 IN HSI6_DP — C1LN .1UF 10V 10% X5R 402 — HSI6_C_DP OUT 31

56 IN HSI6_DN — C2LN .1UF 10V 10% X5R 402 — HSI6_C_DN OUT 31

CAD NOTE:
PLACE NEAR LAN / NINEVEH CONTROLLER

BOM NOTE:
EMPTY FOR EKRON
STUFF FOR NINEVEH

R2LN 649 1% EMPTY 402
KMRN_RCOMP_DP OUT
R7LN 1.4K 1% CH 402
KMRN_RCOMP_DN OUT 56

BOM NOTE:
STUFF (A93548-011) 649 OHM FOR EKRON
EMPTY FOR NINEVEH

BOM NOTE:
EMPTY FOR EKRON
STUFF FOR NINEVEH

01.03.00
INTEL_LAN
R3LN 619 1% EMPTY 402

BOM NOTE:
STUFF 619 1% FOR EKRON
EMPTY 619 OHM FOR NINEVEH

92 56 58 OUT LAN_V_1P0 — R1LN 0 603 1A CH

D20909-002
U1LN
NINEVEH0P99B

92 56 58 IN	LAN_V_1P0	D7	V1P0_OUT/NC	VSS/NC	A1
	LAN_V_1P0_OUT	B1	VDD1P0/VCCR	VSS	C4
		D4	VCC	VSS/VSSP	E1
		E4	VCC/VCC	VSS/VSS	F4
		E8	VDD1P0/VCCT	VSSA/NC	J9
		E5	VCCF1P0/VCC	VSSA/NC	J8
		G4	VCC1P0/VCCA2	VSSA/VSSA2	J5
		F7	VDD1P0/VCCA	VSSA/VSS	J3
		H3	VCCFC1P0/VCC	VSSA/NC	J1
				VSSA/VSS	G9
57 IN	LAN_V_1P8	C2	VCC1P8/NC	VSSA/VSS	G8
58		D5	VCC1P8/NC	VSSA/VSS	G6
88		F5	VCC1P8/NC	VSSA/VSS	F6
57		G5	VCC1P8/NC	VSSA/VSS	E9
40				VSSA/VSS	D6
38				VSSA/VSS	C9
33				VSSA/VSS	C8
27				VSSA/VSS	C7
28				VSSA/VSS	C6
34				VSSA/VSS	A9
39				VSSA/VSS	A8
56					
58					
92					
27 IN	V_3P3_EPW	F2	VCC3P3/VCCP		
28		B3	VCC3P3/VCC		

2 of 2
IC

LAN CRYSTAL

LAN_XTL_DP_R — R46LN 0 402 5% CH — LAN_XTL_DP OUT 56
C35LN 10PF 5% 50V EMPTY 402
C36LN 10PF 5% 50V EMPTY 402
CK_XT_25M_LAN_R
R47LN 33 402 5% EMPTY
CK_XT_25M_LAN IN 29

BOM NOTE:
STUFF R46LN FOR CRYSTAL, EMPTY FOR CLK GEN
STUFF C35LN, EMPTY FOR CRYSTAL

C22LN 27PF 5% 50V COG 402
Y1LN 25.000MHZ SM XTAL A93545-056
C23LN 27PF 5% 50V COG 402
56 IN LAN_XTL_DN

[PAGE_TITLE= LAN NINEVEH]

BPAGE DRAWING
frostburg_fabc.sch_1.56
Sun Mar 18 18:44:12 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	56	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_INTEL_LAN	01.03.00	12-08-06

BOM NOTE:
DEFAULT: STUFF C24LN FOR NINEVEH
EMPTY (UN-STUFF) CAP FOR EKRON

LAN_V_1P8 — C24LN 1000PF 10% 50V X7R 402

LAN CONNECTOR
DEFAULT GIGABIT

MAGJACK BI-COLOR SPEED LED	
10 MBPS	OFF
100 MBPS	GREEN
1000 MBPS	YELLOW

JA1LN
GBE_MAGJACK3_10

LAN_MDI0_DP 10 TD0+
LAN_MDI0_DN 11 TD0-
LAN_MDI1_DP 12 TD1+
LAN_MDI1_DN 13 TD1-
LAN_MDI2_DP 14 TD2+
LAN_MDI2_DN 15 TD2-
LAN_MDI3_DP 16 TD3+
LAN_MDI3_DN 17 TD3-
VCT 9 — LAN_VCT — R27LN 0 805 1A CH
SGND 18
IO
GND=23..30
C73572-005

CAD NOTE:
PLACE CAP/RES NEAR MAGJACK_PIN9

C27LN 470PF 10% 50V X7R 402

BOM NOTE:
DEFAULT: STUFF FOR NINEVEH
EMPTY (UN-STUFF) CAP/RES FOR EKRON

BOM NOTE:
DEFAULT (JA1LN): C73572-005 (NINEVEH)
OPTIONAL(JA1LN): C51242-005 (EKRON-N)

USB STACK

JA1LN
2 X USB
1000

VREG_USB_BP_MJ
USB_BACK3_R_DN
USB_BACK3_R_DP
VREG_USB_BP_MJ
USB_BACK1_R_DN
USB_BACK1_R_DP
IO

BOM NOTE:
STUFF RES (R23LN, R25LN)
FOR NINEVEH

BOM NOTE:
STUFF RES (R24LN, R26LN)
FOR EKRON

V_3P3_EPW — R23LN 0 402 5% CH — V_3P3_R_LAN
LAN_LED1 — R24LN 0 402 5% EMPTY
V_3P3_EPW — R26LN 0 402 5% EMPTY — LAN_R_LED1
LAN_LED1 — R25LN 0 402 5% CH

JA1LN GRN_LED 20 19 IO — LAN_LED0 OUT
C29LN 470PF 10% 50V X7R 402
C28LN 470PF 10% 50V X7R 402
JA1LN GRN_LED 22 21 YLW_LED IO — LAN_LED2 BI
C26LN 470PF 10% 50V X7R 402
C25LN 470PF 10% 50V X7R 402

LAN_MDI0_DP — LAN_DIFF_TAP_0 — C33LN 1UF 10% 10V X5R 402 — R35LN 49.9 1% CH 402 — R34LN 49.9 1% CH 402 — LAN_MDI0_DN
LAN_MDI1_DP — LAN_DIFF_TAP_1 — C32LN 1UF 10% 10V X5R 402 — R33LN 49.9 1% CH 402 — R32LN 49.9 1% CH 402 — LAN_MDI1_DN

BOM NOTE:
DEFAULT: STUFF FOR NINEVEH
EMPTY (UN-STUFF) CAPS FOR EKRON

BOM NOTE:
DEFAULT: STUFF (4) RES WITH 49.9 OHM (A93548-045) FOR NINEVEH
CHANGE (4) RES TO 54.9 OHM (A93548-279) FOR EKRON

LAN_MDI2_DP — LAN_DIFF_TAP_2 — C31LN 1UF 10% 10V X5R 402 — R31LN 49.9 1% CH 402 — R30LN 49.9 1% CH 402 — LAN_MDI2_DN
LAN_MDI3_DP — LAN_DIFF_TAP_3 — C30LN 1UF 10% 10V X5R 402 — R29LN 49.9 1% CH 402 — R28LN 49.9 1% CH 402 — LAN_MDI3_DN

BOM NOTE:
DEFAULT: STUFF FOR NINEVEH
EMPTY (UN-STUFF) CAPS, RESISTORS FOR EKRON

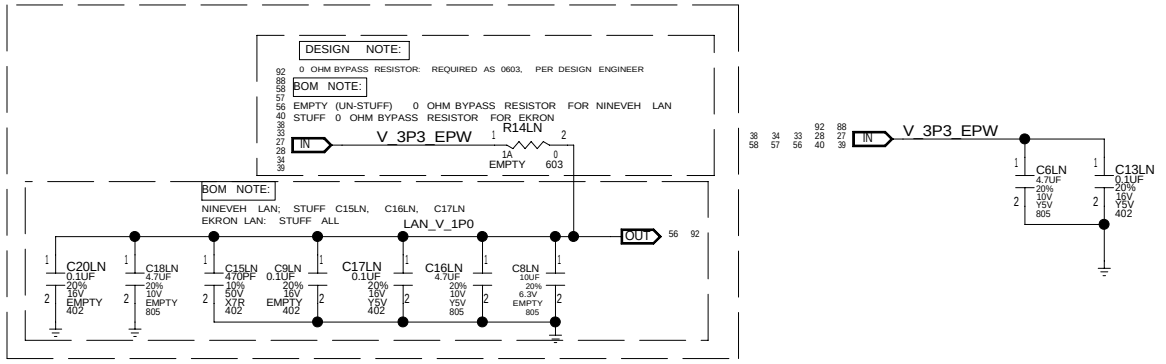
DIFFERENTIAL PAIR TERMINATONS

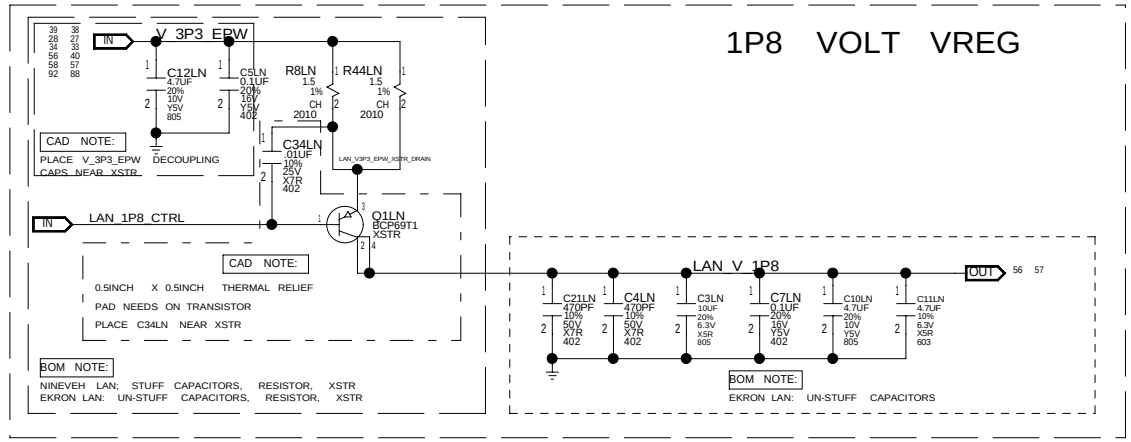
[PAGE_TITLE= LAN NINEVEH]

BPAGE DRAWING
frostburg_fabc.sch_1.57
Sun Mar 18 18:44:14 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	57	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_INTEL_LAN	01.03.00	12-08-06





[PAGE_TITLE= LAN NINEVEH]

BPAGE DRAWING
frostburg_fabc.sch_1.58
Sun Mar 18 18:44:15 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	58	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL AUDIO	0.06.00	10-12-06

BOM NOTE:
ALC268- D72688-001
ALC888- D72853-001
STAC9271D- D35875-004

U1AU
ALC885
REV=1

60 IN AUD_CODEC_VREF	27	VREF	
37 OUT AUD_LINK_BCLK	6	BCLK	
60 OUT AUD_LINK_SDI2_R	8	SDATA_IN	
37 IN AUD_LINK_SDO	5	SDATA_OUT	
37 IN AUD_LINK_SYNC	10	SYNC	
59 IN AUD_LINK_RST_N	11	RESET*	
60 IN AUD_PC_BEEP	12	BEEP	
TP_AUD_CD_IN_L	18	CD_L	
TP_AUD_CD_GND	19	CD_GND	
TP_AUD_CD_IN_R	20	CD_R	
TP_AUD_SPDIF_IN	47	SPDIFI/EAPD	
67 61 OUT AUD_SPDIF_OUT	48	SPDIFO	
64 62 60 OUT AUD_SENSE_A	13	SENSE_A	
63 62 60 OUT AUD_SENSE_B	34	SENSE_B	
	39	PORT_A_L	AUD_PORT_A_L BI 64
	41	PORT_A_R	AUD_PORT_A_R BI 64
	21	PORT_B_L	AUD_PORT_B_L BI 64
	22	PORT_B_R	AUD_PORT_B_R BI 64
	23	PORT_C_L	AUD_PORT_C_L BI 62
	24	PORT_C_R	AUD_PORT_C_R BI 62
	35	PORT_D_L	AUD_PORT_D_L BI 62
	36	PORT_D_R	AUD_PORT_D_R BI 62
	14	PORT_E_L	AUD_PORT_E_L BI 62
	15	PORT_E_R	AUD_PORT_E_R BI 62
	16	PORT_F_L	AUD_PORT_F_L BI 62 63
	17	PORT_F_R	AUD_PORT_F_R BI 62 63
	43	PORT_G_L	AUD_PORT_G_L BI 63
	44	PORT_G_R	AUD_PORT_G_R BI 63
	45	PORT_H_L	TP_AUD_PORT_H_L
	46	PORT_H_R	TP_AUD_PORT_H_R
	37	VRP	TP_AUD_VREF_37
	28	PORT_B_VREFO	AUD_VREF_28 OUT 65
	29	PORT_C_VREFO	TP_AUD_VREF_29
	32	PORT_D_VREFO	AUD_VREF_32 OUT 65
	31	PORT_E_VREFO	AUD_VREF_31 OUT 65
	30	PORT_F_VREFO	AUD_VREF_30 OUT 65
	33	PORT_A_VREFO/DCVOL	AUD_FILTER_33 OUT 60
	40	JDREF	AUD_DVDD_CORE_40
66 60 IN V_AUD_ANALOG	25	AVDD1	
	38	AVDD2	
TP_AUD_GPIO1	3	GPIO1	
V_AUD_DIGITAL	1	DVDD	
	9	DVDD_IO	
	26	AVSS1	
	42	AVSS2	AUD
	2	GPIO0	TP_AUD_VOL_2
	4	DVSS	
	7	DVSS	

1 OF 1 IC

C4AU 5% 10PF 50V COG 402

C98AU 10PF 5% 50V EMPTY 402

SURR REAR L/R PORT F
CEN / LFE PORT G
S/PDIFF OUT
LINE IN / SURR SIDE PORT C
FRONT / LINE OUT PORT D
MIC IN PORT F/E

FACING BACK PANEL

HEADPHONE PORT A
MIC PORT B
SIGMATEL, REALTEK

DESIGN NOTE:
AZALIA:
SIGMATEL-STAC9271D (5 STACKS)
REALTEK- ALC268/888 (3 STACKS)

DESIGN NOTE: CODEC DOWN DISABLE CIRCUIT
IN V_3P3_STBY\G
R70AU 1K 5% EMPTY 402
R71AU 1K 5% EMPTY 402
AUD_LINK_RST_N OUT 59
AUD_LINK_RST_N_PIN3
Q4AU EMPTY
R74AU 100 5% EMPTY 402
R73AU 100 5% EMPTY 402
Q3AU
IN CDC_DWN_DISABLE
AUD_LINK_RST_CDC
R75AU 0 5% CH 402

DESIGN NOTE:
GPIO LOW=CODEC DOWN ENABLE
GPIO HIGH=CODEC DOWN DISABLE

BOM NOTE:
STUFF:MEDIA SKU
EMPTY:CLASSIC SKU

BOM NOTE:
STUFF:CLASSIC SKU
EMPTY:MEDIA SKU

BOM NOTE:
DEFAULT: STUFF 0 OHM (108506-004, 0603)
OPTIONAL: FERRITE BEAD (693286-014, 0603)

VCC3 M17AU MULTI CH 603 OUT 59

C1AU 10UF 20% 6.3V X5R 805
C5AU 1UF 10% 16V X7R 603
C3AU 1UF 10% 16V X7R 603
C110AU 10UF 20% 6.3V X5R 805

CAD NOTE: PLACE NEXT TO PIN 1
CAD NOTE: PLACE NEXT TO PINS 9

R148AU 0 5% EMPTY 402 V_AUD_DIGITAL IN 59
R149AU 20K 1% CH 402

BOM NOTE:
DEFAULT: ALC268/888- R148AU= EMPTY, R149AU=STUFF
OPTION: STAC9271D- R148AU=STUFF, R149AU=EMPTY

BPAGE DRAWING
frostburg_fabc.sch_1.59
Sun Mar 18 18:44:16 2007

[PAGE_TITLE=AUDIO CODEC]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	59	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL AUDIO	0.06.00	10-12-06

CAD NOTE: PLACE NEAR CDC PINS

59 IN AUD_LINK_SDI2_R — R14AU 33 402 5% CH — AUD_LINK_SDI2 OUT 33

AUD_FILTER_33 OUT 59

C9AU 10UF 20% 6.3V EMPTY 805

BOM NOTE:
DEFAULT: ALC268/888 EMPTY
OPTION: STAC9271D STUFF

CAD NOTE: PLACE CIRCUIT NEXT TO PIN 33

AUD

JACK DETECT NETWORK

66 60 59 IN V_AUD_ANALOG — R9AU 5.11K 1% EMPTY 402 — AUD_SENSE_B OUT 59 62 63

BOM NOTE:
DEFAULT:ALC268/888 EMPTY
OPTION:STAC9271D STUFF

CAD NOTE: PLACE NEAR PIN 34

C10AU 1000PF 10% 50V EMPTY 402

AUD

60 59 66 IN V_AUD_ANALOG — R11AU 5.11K 1% EMPTY 402 — AUD_SENSE_A OUT 59 62 64

BOM NOTE:
DEFAULT:ALC268/888 EMPTY
OPTION:STAC9271D STUFF

CAD NOTE: PLACE NEAR PIN 13

C15AU 1000PF 10% 50V EMPTY 402

AUD

AUD_CODEC_VREF OUT 59

C20AU .1UF 10% 10V X5R 402

C19AU 10UF 20% 6.3V X5R 805

VREF SUPPLY

CAD NOTE: PLACE NEAR PIN 27

AUD

CAD NOTE: PLACE NEXT TO PIN 25

C13AU 10UF 20% 6.3V X5R 805

C11AU 1UF 10% 10V X5R 402

CAD NOTE: PLACE NEXT TO PIN 38

C16AU 10UF 20% 6.3V X5R 805

C17AU 1UF 10% 10V X5R 402

V_AUD_ANALOG OUT 59 60 66

AUD

SUPPLY DECOUPLING

37 33 IN SPKR — R13AU 10K 402 5% CH — AUD_PC_BEEP_PIN1 — C18AU .1UF 10% 10V X5R 402 — AUD_PC_BEEP OUT 59

R12AU 100 5% CH 402

C8AU .01UF 10% 25V EMPTY 402

AUD AUD

PC BEEP

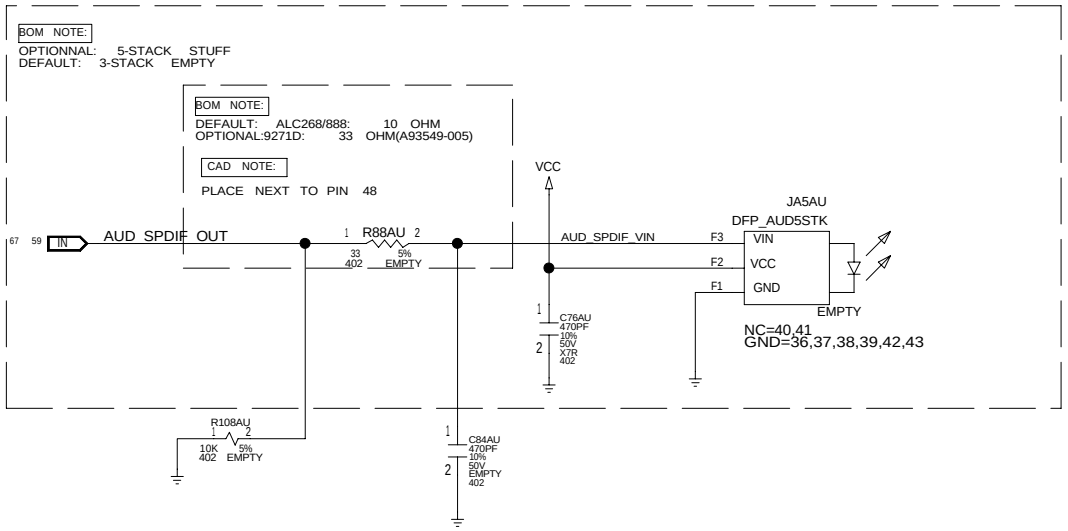
BPAGE DRAWING

frostburg_fabc.sch_1.60
Sun Mar 18 18:44:18 2007

[PAGE_TITLE=AUDIO DECOUPLING & JACK SENSE]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	60	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL AUDIO	0.06.00	10-12-06



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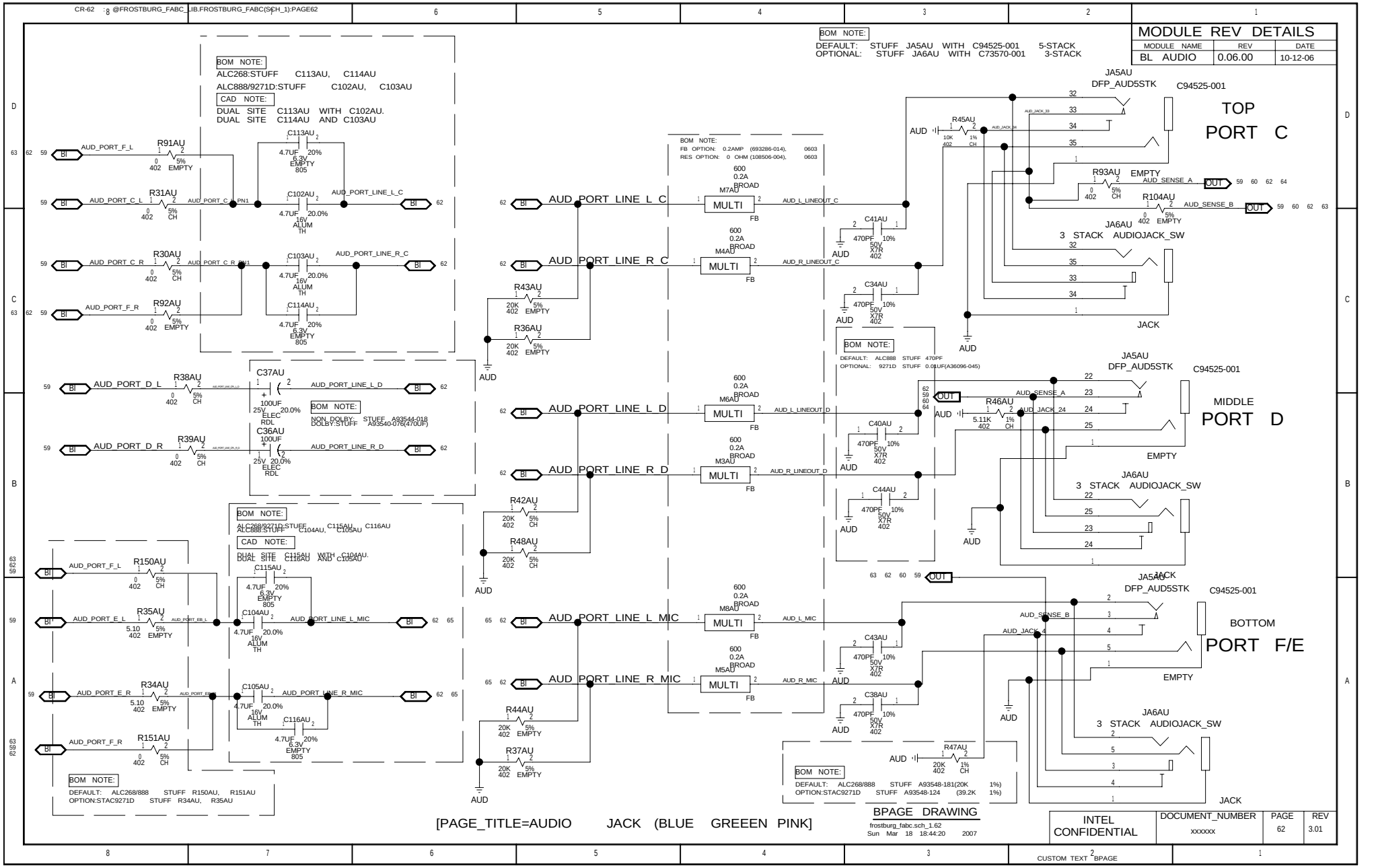
BPAGE DRAWING

frostburg_fabc.sch_1.61
Sun Mar 18 18:44:19 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	61	3.01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MODULE REV DETAILS
MODULE NAME | REV | DATE
BL AUDIO | 0.06.00 | 10-12-06
BOM NOTE:
DEFAULT: STUFF JA5AU WITH C94525-001 5-STACK
OPTIONAL: STUFF JA6AU WITH C73570-001 3-STACK
BOM NOTE:
ALC268:STUFF C113AU, C114AU
ALC888/9271D:STUFF C102AU, C103AU
CAD NOTE:
DUAL SITE C113AU WITH C102AU.
DUAL SITE C114AU AND C103AU
AUD_PORT_F_L
R91AU
C113AU
4.7UF 20% 6.3V EMPTY 805
AUD_PORT_C_L
R31AU
C102AU
AUD_PORT_LINE_L_C
4.7UF 20.0% 16V ALUM TH
AUD_PORT_C_R
R30AU
C103AU
AUD_PORT_LINE_R_C
AUD_PORT_F_R
R92AU
C114AU
AUD_PORT_D_L
R38AU
C37AU
100UF 25V 20.0% ELEC RDL
AUD_PORT_LINE_L_D
AUD_PORT_D_R
R39AU
C36AU
AUD_PORT_LINE_R_D
BOM NOTE:
NON_DOLBY: STUFF A93544-018
DOLBY:STUFF A93540-076(470UF)
BOM NOTE:
ALC268/9271D:STUFF C104AU, C105AU C115AU C116AU
ALC888:STUFF
CAD NOTE:
DUAL SITE C115AU WITH C104AU.
DUAL SITE C116AU AND C105AU
AUD_PORT_F_L
R150AU
C115AU
AUD_PORT_E_L
R35AU
C104AU
AUD_PORT_LINE_L_MIC
AUD_PORT_E_R
R34AU
C105AU
AUD_PORT_LINE_R_MIC
AUD_PORT_F_R
R151AU
C116AU
BOM NOTE:
DEFAULT: ALC268/888 STUFF R150AU, R151AU
OPTION:STAC9271D STUFF R34AU, R35AU
BOM NOTE:
FB OPTION: 0.2AMP (693286-014), 0603
RES OPTION: 0 OHM (108506-004), 0603
600 0.2A BROAD
M7AU MULTI FB
AUD_PORT_LINE_L_C
AUD_L_LINEOUT_C
M4AU MULTI FB
AUD_PORT_LINE_R_C
AUD_R_LINEOUT_C
M6AU MULTI FB
AUD_PORT_LINE_L_D
AUD_L_LINEOUT_D
M3AU MULTI FB
AUD_PORT_LINE_R_D
AUD_R_LINEOUT_D
M8AU MULTI FB
AUD_PORT_LINE_L_MIC
AUD_L_MIC
M5AU MULTI FB
AUD_PORT_LINE_R_MIC
AUD_R_MIC
R43AU 20K 5% 402 EMPTY
R36AU 20K 5% 402 EMPTY
R42AU 20K 5% 402 CH
R48AU 20K 5% 402 CH
R44AU 20K 5% 402 EMPTY
R37AU 20K 5% 402 EMPTY
C41AU 470PF 10% 50V X7R 402
C34AU 470PF 10% 50V X7R 402
C40AU 470PF 10% 50V X7R 402
C44AU 470PF 10% 50V X7R 402
C43AU 470PF 10% 50V X7R 402
C38AU 470PF 10% 50V X7R 402
BOM NOTE:
DEFAULT: ALC888 STUFF 470PF
OPTIONAL: 9271D STUFF 0.01UF(A36096-045)
R45AU 10K 1% 402 CH
R93AU EMPTY 0 5% 402 CH
R104AU 0 5% 402 EMPTY
AUD_SENSE_A
AUD_SENSE_B
JA5AU DFP_AUD5STK C94525-001
TOP PORT C
JA6AU 3 STACK AUDIOJACK_SW
JACK
R46AU 5.11K 1% 402 CH
MIDDLE PORT D
EMPTY
BOTTOM PORT F/E
R47AU 20K 1% 402 CH
BOM NOTE:
DEFAULT: ALC268/888 STUFF A93548-181(20K 1%)
OPTION:STAC9271D STUFF A93548-124 (39.2K 1%)
[PAGE_TITLE=AUDIO JACK (BLUE GREEEN PINK]
BPAGE DRAWING
frostburg_fabc.sch_1.62
Sun Mar 18 18:44:20 2007
INTEL CONFIDENTIAL
DOCUMENT_NUMBER
xxxxxx
PAGE 62
REV 3.01
CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL AUDIO	0.06.00	10-12-06

BOM NOTE:
STUFF THIS PAGE FOR 5-STACK

BOM NOTE:
5STACK:STUFF C106AU,C107AU
3STACK:EMPTY ALL

BOM NOTE:
FB OPTION: 0.2AMP (693286-014), 0603
RES OPTION: 0 OHM (108506-004), 0603

BOM NOTE:
5STACK:STUFF C108AU,C109AU
3STACK:EMPTY ALL

AUD_PORT_F_L
AUD_PORT_F_R
AUD_PORT_G_L
AUD_PORT_G_R
AUD_PORT_F_C_L
AUD_PORT_F_C_R
AUD_PORT_FG_L
AUD_PORT_FG_R
AUD_PORT_REAR_L
AUD_PORT_REAR_R
AUD_PORT_CNT_L
AUD_PORT_LFE_R
AUD_PORT_REAR_L_JACK
AUD_PORT_REAR_R_JACK
AUD_PORT_CNT_L_JACK
AUD_PORT_LFE_R_JACK
AUD_SENSE_B
AUD_JACK_D3
AUD_JACK_E3

R60AU 0 402 5% EMPTY
R61AU 0 402 5% EMPTY
R59AU 0 402 5% EMPTY
R58AU 0 402 5% EMPTY
R62AU 20K 402 1% EMPTY
R67AU 10K 402 1% EMPTY
R66AU 20K 402 5% EMPTY
R64AU 20K 402 5% EMPTY
R114AU 20K 402 5% EMPTY
R130AU 20K 402 5% EMPTY

C117AU 4.7UF 20% 6.3V EMPTY 805
C118AU 4.7UF 20% 6.3V EMPTY 805
C119AU 4.7UF 20% 6.3V EMPTY 805
C120AU 4.7UF 20% 6.3V EMPTY 805
C106AU 4.7UF 20.0% 16V EMPTY TH
C107AU 4.7UF 20.0% 16V EMPTY TH
C108AU 4.7UF 20.0% 16V EMPTY TH
C109AU 4.7UF 20.0% 16V EMPTY TH
C54AU 470PF 10% 50V EMPTY 402
C51AU 470PF 10% 50V EMPTY 402
C53AU 470PF 10% 50V EMPTY 402
C56AU 470PF 10% 50V EMPTY 402

M12AU 600 0.2A BROAD MULTI EMPTY
M14AU 600 0.2A BROAD MULTI EMPTY
M11AU 600 0.2A BROAD MULTI EMPTY
M13AU 600 0.2A BROAD MULTI EMPTY

JA5AU DFP_AUD5STK C94525-001
D1 D2 D3 D4 G1 EMPTY
PORT F TOP

JA5AU DFP_AUD5STK C94525-001
E1 E2 E3 E4 G1 EMPTY
PORT G BOTTOM

AUD

[PAGE_TITLE=AUDIO JACK (BLACK ORANGE]

BPAGE DRAWING
frostburg_fabc.sch_1.63
Sun Mar 18 18:44:21 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	63	3.01

CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL AUDIO	0.06.00	10-12-06

CAD NOTE:
EMI CAP
PLACE NEXT TO PIN 1

C100AU 10PF 5% 50V EMPTY 402

IN V_3P3_STBY\G
VCC3 +12V

J7AU
2X8HDR12
EMPTY
A91836-016

R80AU 33 402 5% EMPTY
R69AU 33 402 5% EMPTY
R81AU 33 402 5% EMPTY
R72AU 33 402 5% EMPTY

IN AUD_LINK_BCLK_R
IN AUD_LINK_RST_R_N
IN AUD_LINK_SYNC_R
IN AUD_LINK_SDO_R

AUD_LINK_BCLK_HDR
AUD_LINK_RST_HDR
AUD_LINK_SYNC_HDR
AUD_LINK_SDO_HDR

TP_AUD_RSVD3
TP_AUD_RSVD2

R156AU 0 402 5% EMPTY
AUD_LINK_SDI1 OUT 33
AUD_LINK_SDI0 OUT 33

BOM NOTE:
DEFAULT: EMPTY FOR CLASSIC SKU
OPTION: STUFF FOR MEDIA SKU

BOM NOTE:
ALC268/888- EMPTY
STAC9271D-STUFF

AUD_SENSE_A OUT 59 60 62
C57AU 220PF 10% 50V EMPTY 402
AUD

J6AU
2X5HDR_8
HDR

BI AUD_PORT_B_L_HDR 65 64
BI AUD_PORT_B_R_HDR 65 64
BI AUD_PORT_A_R_HDR 64
BI AUD_PORT_A_L_HDR 64

R94AU 0 402 5% CH
AUD_FP_DETECT_HDR
FP_AUD_DETECT OUT 33 36
AUD_FP_SENSE_MIC
AUD_FP_SENSE_HP

R95AU 39.2K 1% CH 402
R96AU 20K 1% CH 402

BOM NOTE:
ALC26/888- 0OHM A93549-001
STAC9271D- 5.1OHM A93549-060

R89AU 0 402 5% CH
AUD_PORT_B_R_C_HDR
C67AU 4.7UF 6.3V X5R 805 20%
AUD_PORT_B_R_HDR

R85AU 0 402 5% CH
AUD_PORT_B_L_C_HDR
C70AU 4.7UF 6.3V X5R 805 20%
AUD_PORT_B_L_HDR

BOM NOTE:
NON DOLBY: STUFF A93544-018
DOLBY:STUFF A93540-076(470UF)

R90AU 5.10 402 5% CH
AUD_PORT_A_R_C_HDR
C93AU 100UF 25V 20.0% ELEC RDL
AUD_PORT_A_R_HDR

R86AU 5.10 402 5% CH
AUD_PORT_A_L_C_HDR
C94AU 100UF 25V 20.0% ELEC RDL
AUD_PORT_A_L_HDR

R146AU 20K 5% CH 402
R145AU 20K 5% CH 402
R144AU 20K 5% EMPTY 402
R143AU 20K 5% EMPTY 402

C60AU 470PF 10% 50V X7R 402
C65AU 470PF 10% 50V X7R 402
C58AU 220PF 10% 50V X7R 402
C59AU 220PF 10% 50V X7R 402
C66AU 220PF 10% 50V X7R 402
C64AU 220PF 10% 50V EMPTY 402
C61AU 220PF 10% 50V EMPTY 402

BOM NOTE:
DEFAULT: ALC888 STUFF 470PF
OPTION: 9271D STUFF 0.01UF(A36096-045)

CAD NOTE:
PLACE 220PF CAPS CLOSE TO 2X5 AUDIO FRONT PANEL CONNECTOR

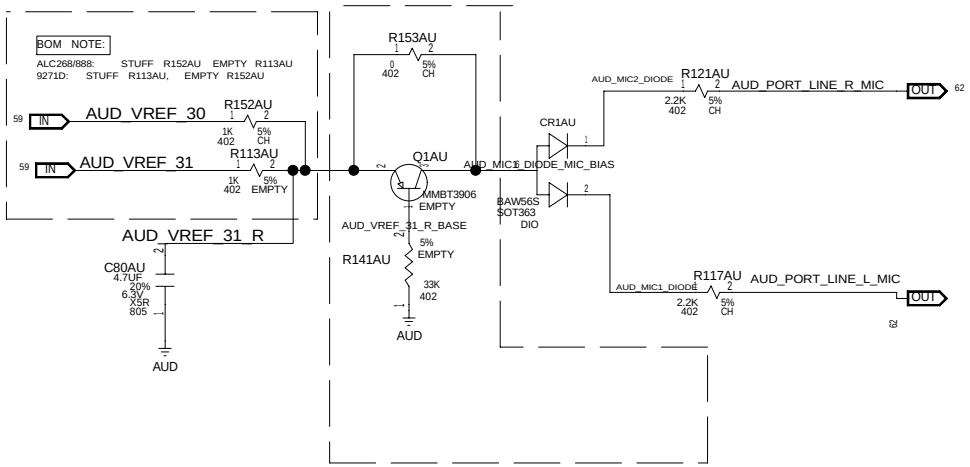
[PAGE_TITLE=AUDIO FP HEADERS & HDA HEADER]

BPAGE DRAWING
frostburg_fabc.sch_1.64
Sun Mar 18 18:44:23 2007

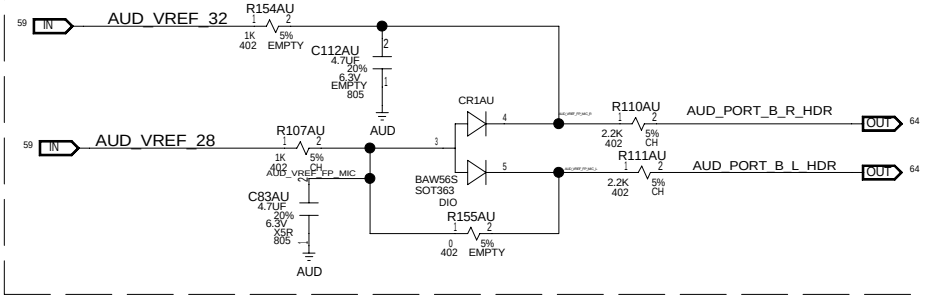
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	64	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL AUDIO	0.06.00	10-12-06

REAR MIC BIAS



FRONT MIC BIAS



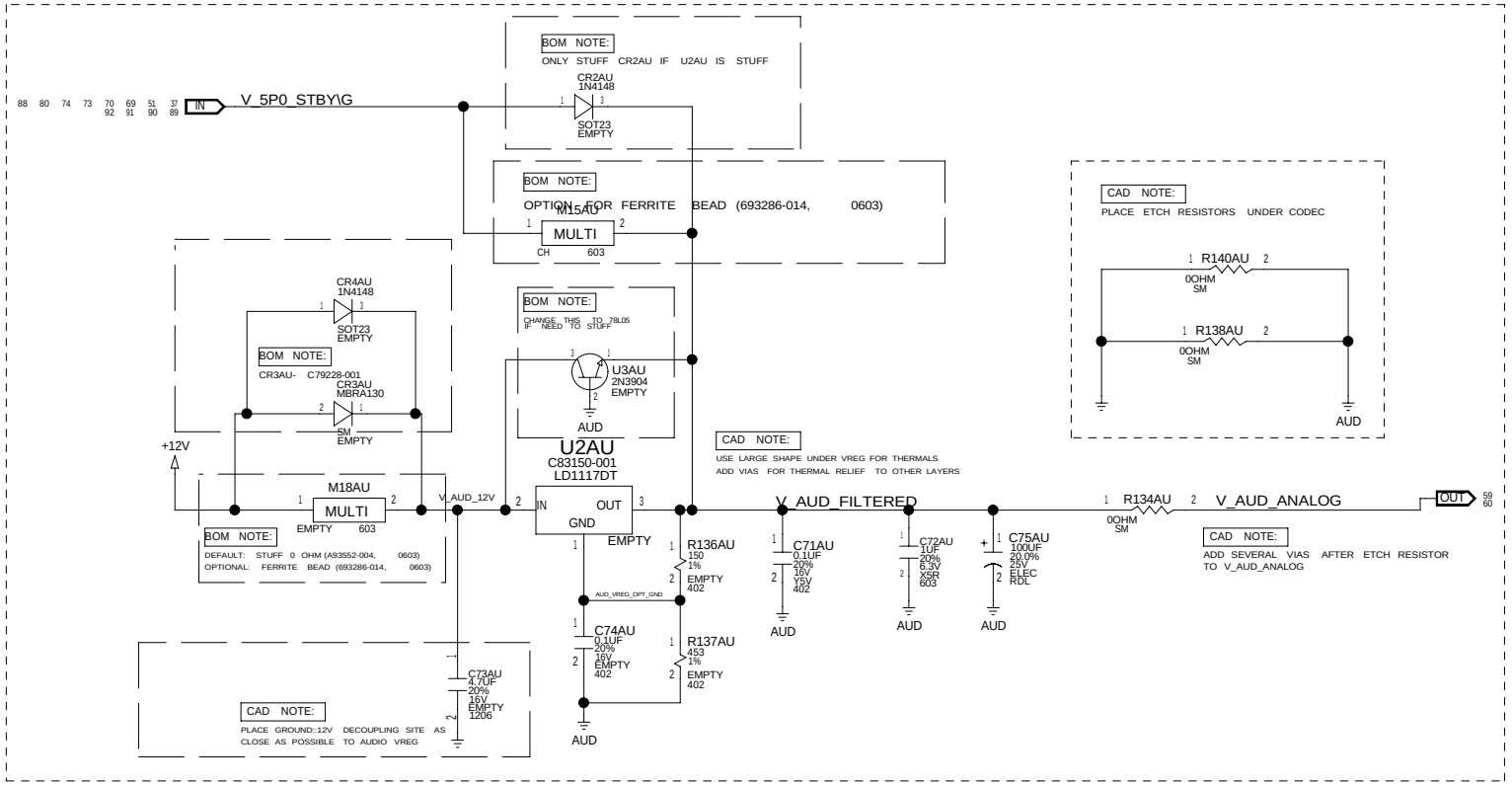
[PAGE_TITLE=AUDIO MIC BIAS]

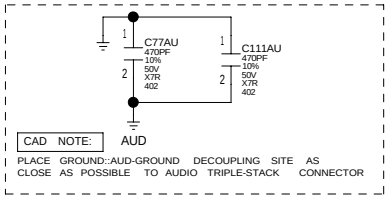
BPAGE DRAWING
frostburg_fabc.sch_1.65
Sun Mar 18 18:44:24 2007

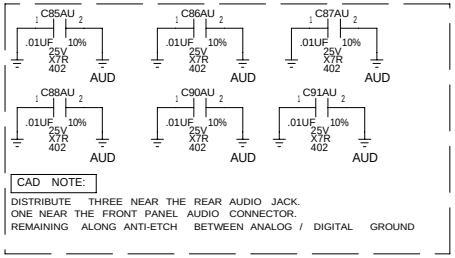
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	65	3.01

CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL AUDIO	0.06.00	10-12-06







BPAGE DRAWING

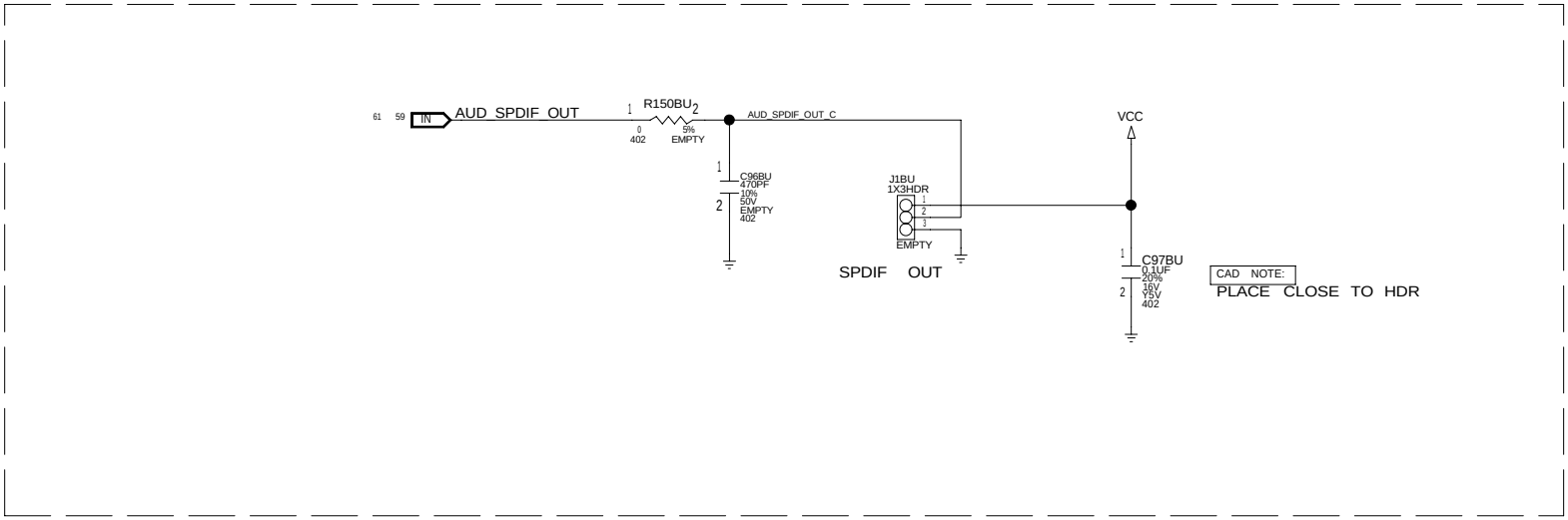
frostburg_fabc.sch_1.66
Sun Mar 18 18:44:25 2007

[PAGE_TITLE=AUDIO VREG]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	66	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL AUDIO	0.06.00	10-12-06

ATX CUSTOM SPDIF HEADER



BPAGE DRAWING

frostburg_fabc.sch_1.67
Sun Mar 18 18:44:27 2007

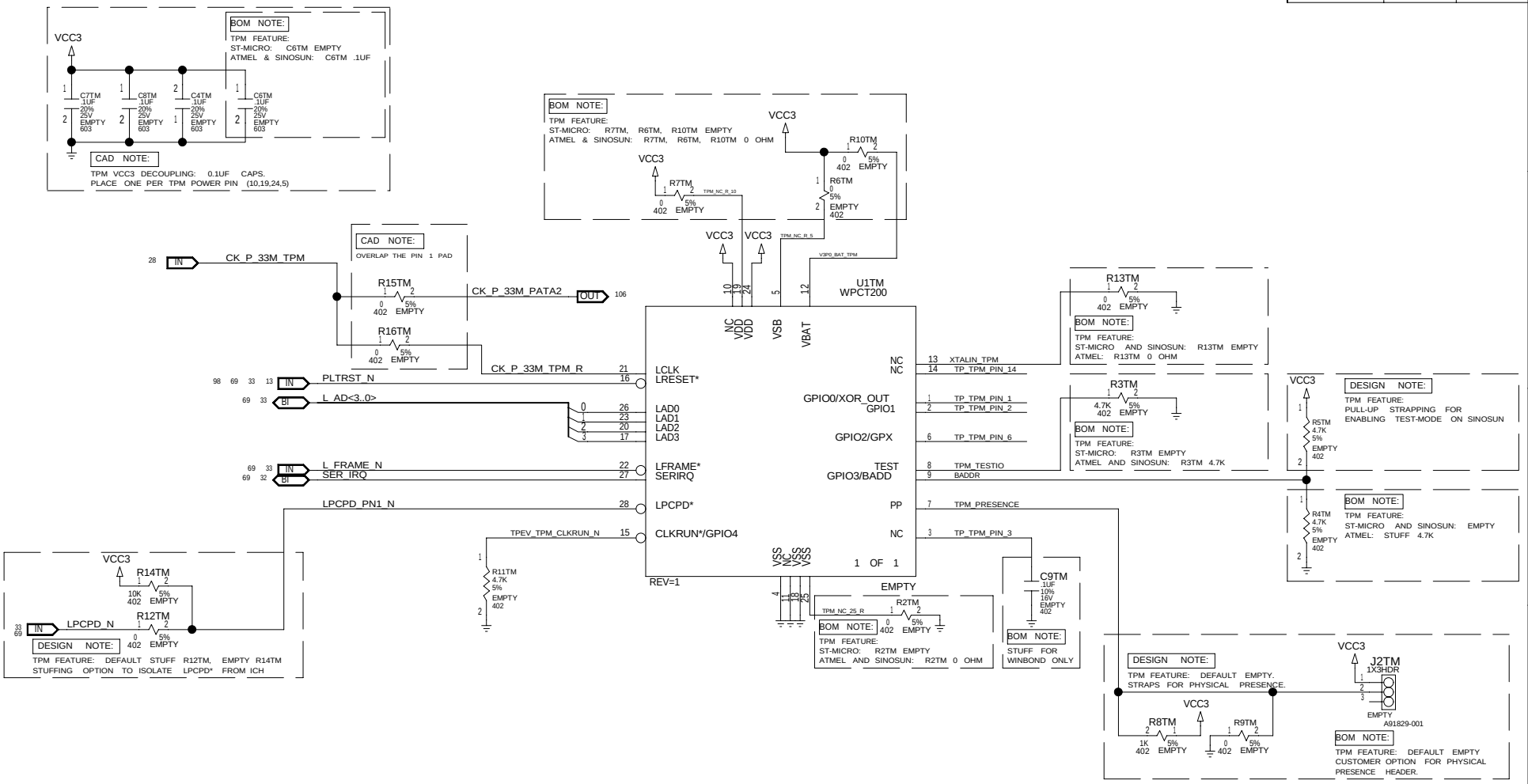
[PAGE_TITLE=SPDIF HEADER]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	67	3.01

CUSTOM TEXT 2 BPAGE

TPM 1.2

MODULE REV DETAILS		
MODULE NAME	REV	DATE
TPM1.2	1.2.0	41.4.06



[PAGE_TITLE=TPM 1.2]

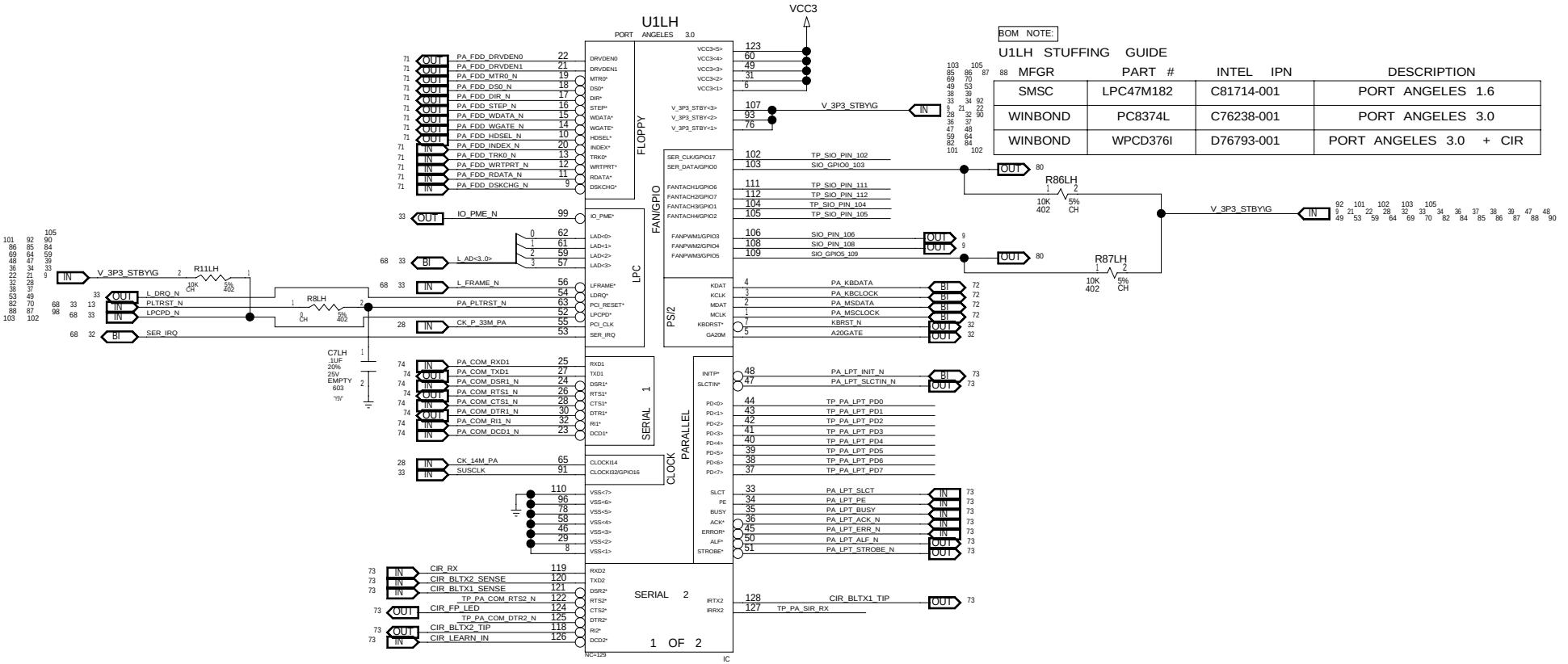
BPAGE DRAWING

frostburg_fabc.sch_1.68
Sun Mar 18 18:44:28 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	68	3.01

SIO TRIPLE SITE (SMSC LPC47M182, WINBOND PC8347L, WINBOND WPCD376I)

MODULE REV DETAILS		
MODULE NAME	REV	DATE
SIO_CIR_ICH9	1.01.00	01.22.07

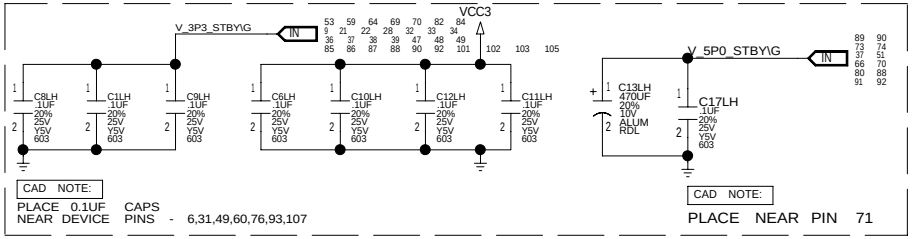


BOM NOTE:

U1LH STUFFING GUIDE

MFGR	PART #	INTEL IPN	DESCRIPTION
SMSC	LPC47M182	C81714-001	PORT ANGELES 1.6
WINBOND	PC8374L	C76238-001	PORT ANGELES 3.0
WINBOND	WPCD376I	D76793-001	PORT ANGELES 3.0 + CIR

DECOUPLING



CAD NOTE:
PLACE 0.1UF CAPS NEAR DEVICE PINS - 6,31,49,60,76,93,107

CAD NOTE:
PLACE NEAR PIN 71

BPAGE DRAWING
frostburg_fabc.sch_1.69
Sun Mar 18 18:44:29 2007

[PAGE_TITLE=PORT ANGELES 1 OF 2]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	69	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
SIO_CIR_ICH9	1.01.00	01.22.07

NOTE: DEFAULT TYPE IS LISTED FIRST
SEE PORT ANGELES SPEC P. 16 FOR TYPE DESCRIPTION

PIN	FUNCTION	TYPE
1	TEST_EN	3IPD
2	AUD_LINK_RST*	5I
3	CDC_DWN_ENAB/GPIO12*	5I/O12
70	PRIMARY_HD*	3ISPU_400
71	SECONDARY_HD*	3ISPU_400
72	SCSI*	3ISPU_400
75	FPRST*	3ISPU_400
80	PWRGD_PS	3ISPU_400
81	CPU_PRESENT*	3ISPU_400
83	SLP_S3*	3IS_400
84	SLP_S5*	3IS_400
87	SMB_CLK_M	3IOD6
88	SMB_CLK_R	3IOD6
89	SMB_DAT_M	3IOD6
90	SMB_DAT_R	3IOD6
124	5V_DDCSDA/GPIO8	5IOD6/3IO8
125	5V_DDCSCL/GPIO9	5IOD6/3IO8
126	3V_DDCSDA/GPIO10	3IOD6/3IO8
127	3V_DDCSCL/GPIO11	3IOD6/3IO8

VCC3

V_3P3_STBY\G (IN) — R22LH 2.7K 5% CH 402 — R23LH 2.7K 5% CH 402

R13LH 8.2K 5% CH 402 — R21LH 8.2K 5% CH 402

V_3P3_STBY\G (IN) — R20LH 1K 5% CH 402

SMB_CLK_MAIN (BI)
SMB_CLK_RESUME (BI)
SMB_DATA_MAIN (BI)
SMB_DATA_RESUME (BI)
VGA_SIO_DDCSDA_5V (BI)
VGA_SIO_DDCSCL_5V (BI)
VGA_MCHSIO_DDCSDA (BI)
VGA_MCHSIO_DDCSCL (BI)
GPIO_GRN_BLNK_HDR (OUT)
GPIO_YLW_BLNK_HDR (OUT)
HD_LED_N (OUT)
IDE_PRI_ACT_N (IN)
ICH_SATA_LED_N (IN)
SCSI_ACT_N (IN)
FP_RST_N (IN)
SLP_S3_N (IN)
S4_STATE_N (IN)

U1LH
PORT ANGELES 3.0

SMB_CLK_MAIN	87	V_5P0_STBY	71
SMB_CLK_RESUME	88	REF_5V_STBY	72
SMB_DAT_MAIN	89	REF_5V	70
SMB_DAT_RESUME	90	PWRGD_3V	84
		PWRGD_PS	82
5V_DDCSDA/GPIO8	116		
5V_DDCSCL/GPIO9	114		
3V_DDCSDA/GPIO10	115	PCIRST_OUT*	73
3V_DDCSCL/GPIO11	113	PCIRST_OUT2*	74
		IDE_RSTDRV*	64
		RSMRST*	92
GRN_LED	94		
YLW_LED	95		
HD_LED*	66	BACKFEED_CUT*	77
HDD_ACT_1*	67	LATCHED_BF_CUT	79
HDD_ACT_2*	68	SCK_BJT_GATE	80
HDD_ACT_3*	69	PS_ON*	81
FPRST*/GPIO14	75	CPU_PRESENT*	83
SLP_S3*	85	GPIO12	100
SLP_S4*/S5*	86	GPIO13	101
		GPO11	117
VBAT	98		
F_CAP/GPIO15	97		

POWER, VT, DDC, VGA, LED, PWR SEQ
2 OF 2
NC=129 IC

PLTRST_PCIE_SLOTS_R_N — R19LH 0 402 5% CH — PLTRST_PCIE_SLOTS_N (OUT) — C16LH 100PF 5% 50V COG 402

TP_PCIRST_OUT2_R_N
TP_IDE_RST_N
ICH_RSMRST_N
BACKFEED_CUT
LATCHED_BACKFEED_CUT
TP_SCK_BJT_GATE
PS_ON_SIO_N
H_SKTOCC_R_N — R64LH 0 402 5% CH — H_SKTOCC_N (IN)

R65LH 10K 5% EMPTY 402

TP_SIO_PIN_100
TP_SIO_PIN_101
TP_SIO_PIN_117

TP_PA_TESTEN_1

PA_F_CAP — C14LH 4.7UF 20% 16V Y5V 1206 — C15LH .1UF 10% 16V X7R 603

R72LH 8.2K 5% CH 402

CAD NOTE:
PLACE AS CLOSE TO PIN AS POSSIBLE

SCSI ACTIVITY HEADER

SCSI_ACT_N (OUT) — J2LH 1X2HDR — TP_SCSI_ACT_PIN2
EMPTY

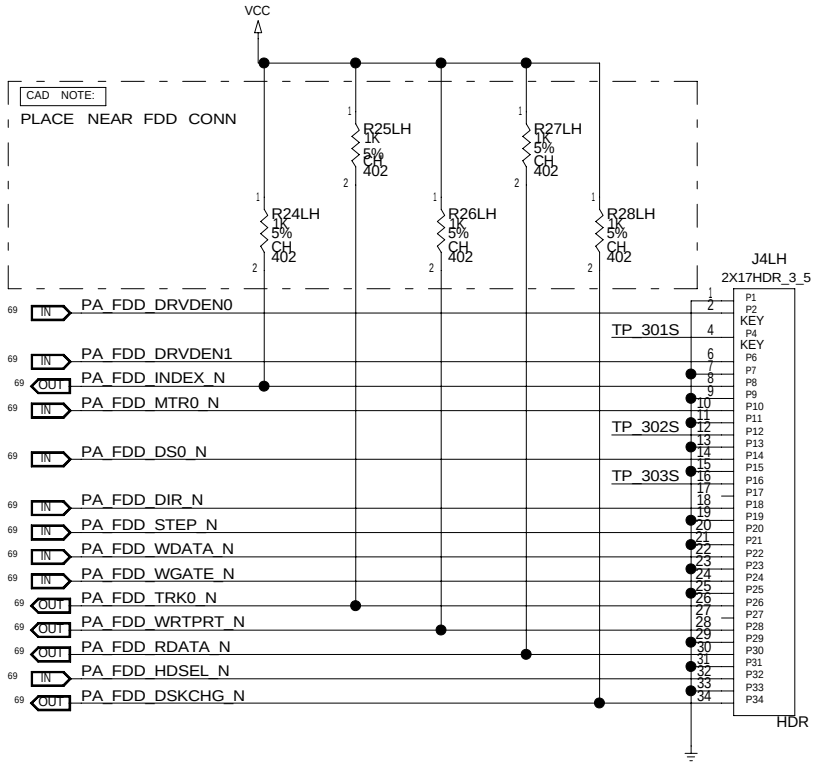
BPAGE DRAWING
frostburg_fabc.sch_1.70
Sun Mar 18 18:44:31 2007

[PAGE_TITLE=PORT ANGELES 2 OF 2]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	70	3.01

CUSTOM TEXT 2 BPAGE

MODULE_REV_DETAILS		
MODULE_NAME	REV	DATE
SIO_CIR_ICH9	1.01.00	01.22.07



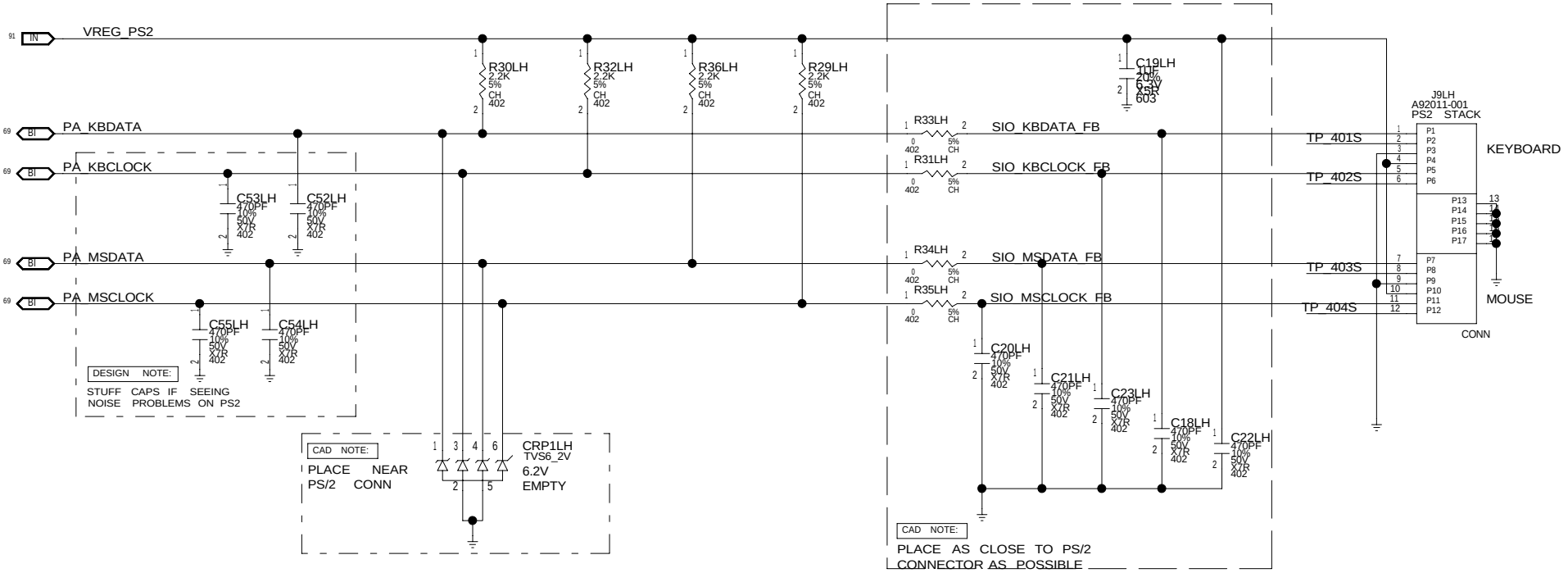
BPAGE DRAWING

frostburg_fabc.sch_1.71
Sun Mar 18 18:44:32 2007

[PAGE_TITLE=FDD CONN]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	71	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
SIO_CIR_ICH9	1.01.00	01.22.07



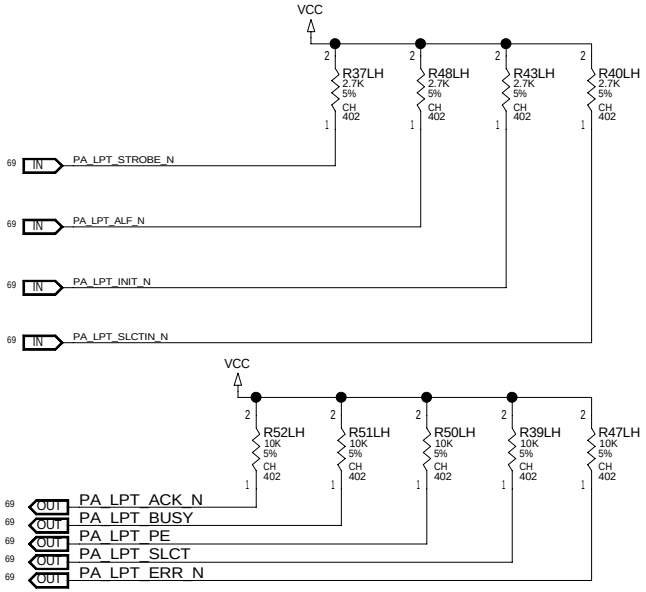
BPAGE DRAWING

frostburg_fabc.sch_1.72
Sun Mar 18 18:44:34 2007

[PAGE_TITLE=PS/2 CONNECTOR]

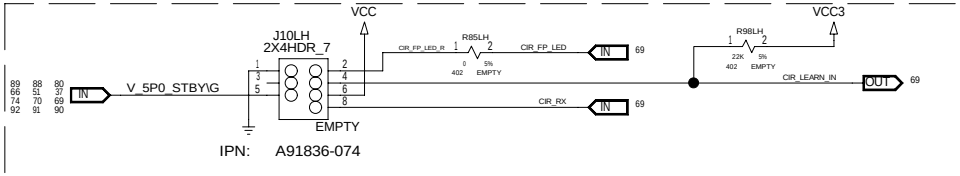
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	72	3.01

LPT PULLUPS



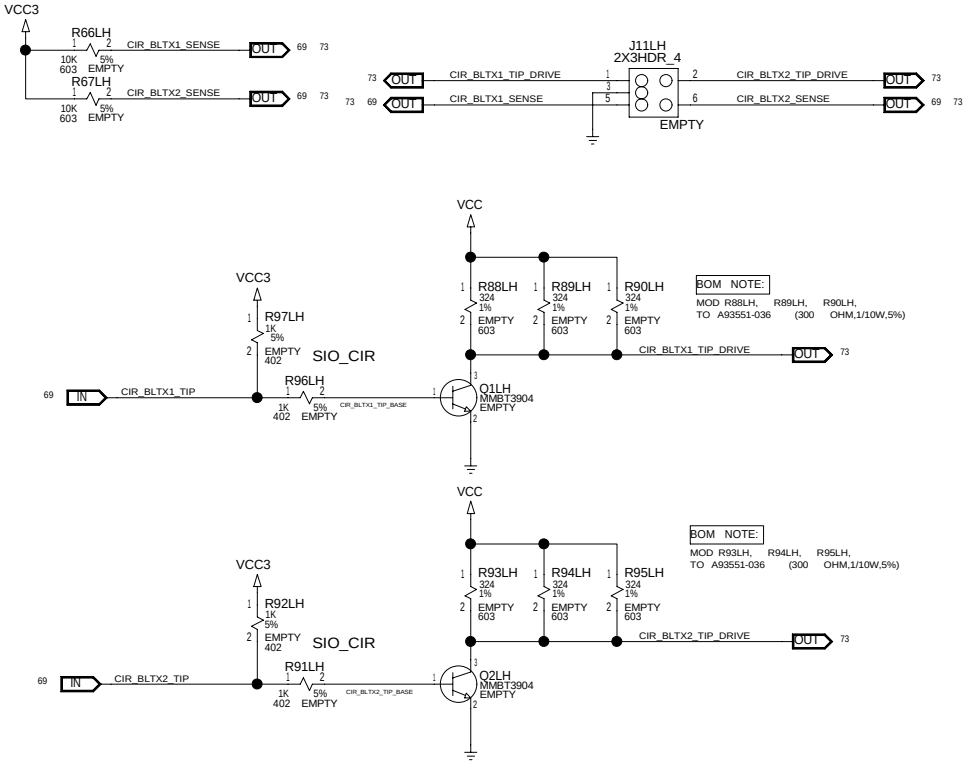
BOM NOTE:
STUFF FOR CONSUMER IR SUPPORT
STUFF ONLY WITH WINBOND -376I DEVICE

FRONT PANEL RECEIVERS



IPN: A91836-074

BACK PANEL BLASTERS



MODULE REV DETAILS		
MODULE NAME	REV	DATE
SIO_CIR_ICH9	1.01.00	01.22.07

BPAGE DRAWING
frostburg_fabc.sch_1.73
Sun Mar 18 18:44:35 2007

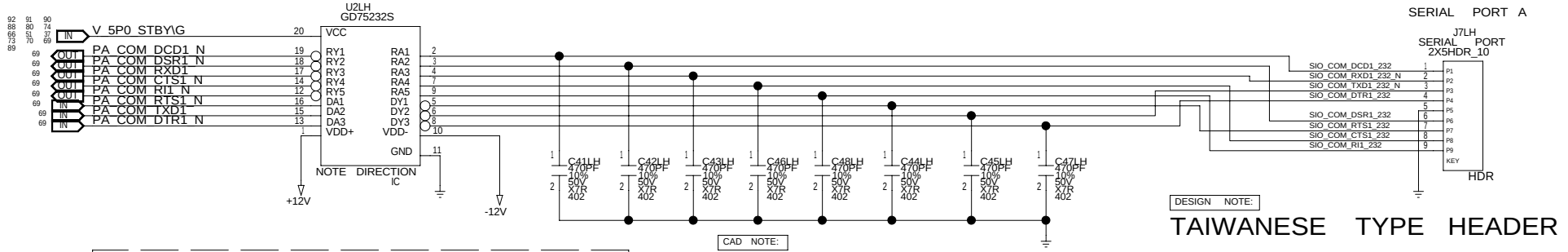
[PAGE_TITLE=LPT SIGNALS]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	73	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
SIO_CIR_ICH9	1.01.00	01.22.07

BOM NOTE:

DO NOT USE NATIONAL OR GOLDSTAR PARTS OF THIS BASE PN

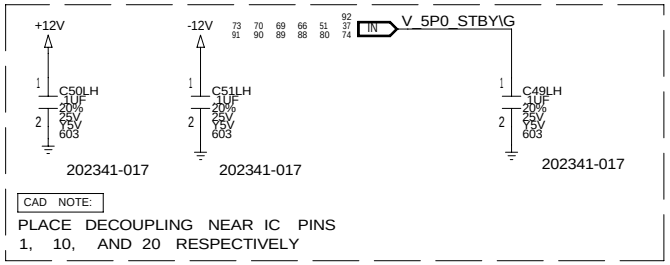


CAD NOTE:

PLACE NEAR CONNECTOR

DESIGN NOTE:

TAIWANESE TYPE HEADER



CAD NOTE:

PLACE DECOUPLING NEAR IC PINS 1, 10, AND 20 RESPECTIVELY

BPAGE DRAWING

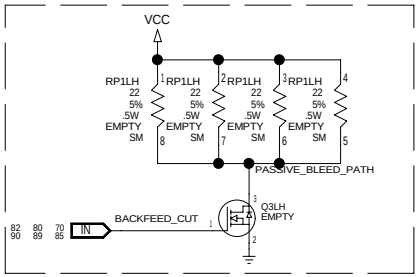
frostburg_fabc.sch_1.74
Sun Mar 18 18:44:36 2007

[PAGE_TITLE=SERIAL PORT A]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	74	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
SUPER_IO	1.08.01	2.10.06

PASSIVE BLEED CIRCUIT



BPAGE DRAWING

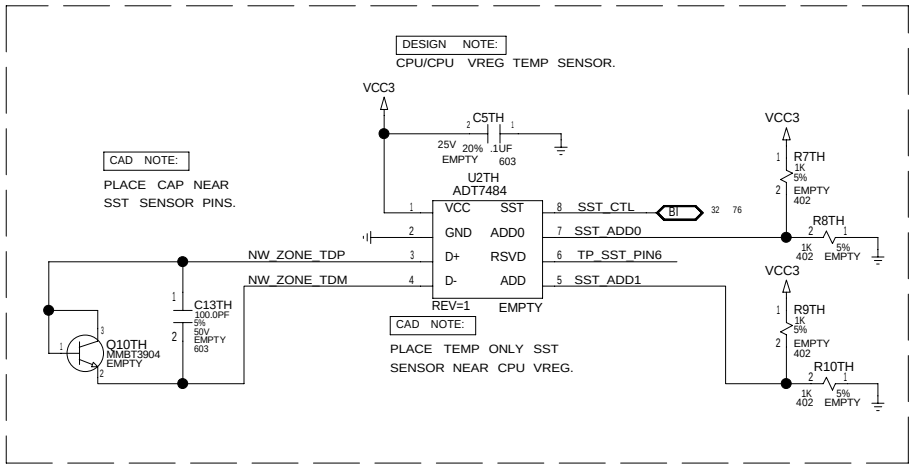
frostburg_fabc.sch_1.75
Sun Mar 18 18:44:38 2007

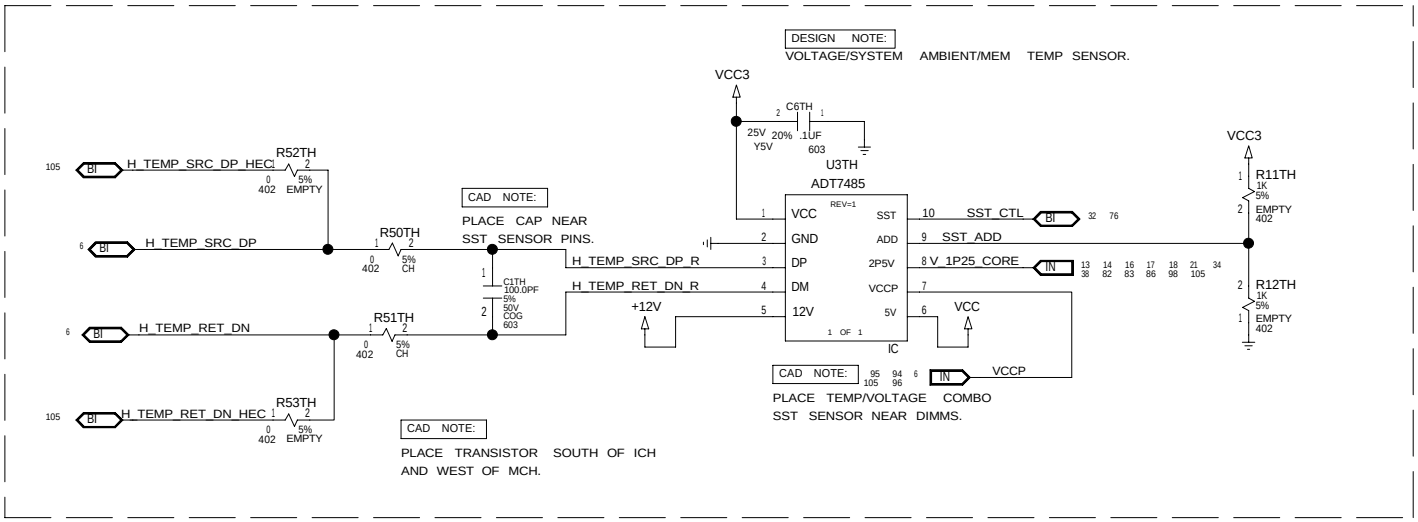
[PAGE_TITLE=STUDIES PURPOSE]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	75	3.01

SST SENSORS

MODULE REV DETAILS		
MODULE NAME	REV	DATE
SST	1.3.0	41.3.06





BPAGE DRAWING

frostburg_fabc.sch_1.76
Sun Mar 18 18:44:39 2007

[PAGE_TITLE=SST SENSOR]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	76	3.01

CUSTOM TEXT 2 BPAGE

FAN CONFIGURATION

MODULE REV DETAILS		
MODULE NAME	REV	DATE
SST	1.3.0	41.3.06

CAD NOTE:
CPU FAN:
BTX/ATX: PLACE BELOW/RIGHT OF CPU SOCKET

CAD NOTE:
FRONT/REAR CHASSIS FAN:
BTX: PLACE ABOVE/RIGHT OF CPU SOCKET
ATX: PLACE NEAR BACKPANEL

CAD NOTE:
REAR/FRONT CHASSIS FAN:
BTX/ATX: PLACE BELOW/LEFT OF DIMMS

BPAGE DRAWING
frostburg_fabc.sch_1.77
Sun Mar 18 18:44:40 2007

[PAGE_TITLE=FAN CONFIGURATION]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	77	3.01

CUSTOM TEXT BPAGE

MODULE_REV_DETAILS		
MODULE_NAME	REV	DATE

DESIGN NOTE:

PB MOUNTING HOLE

J1PB
MTG_HOLE
NC9
EMPTY

J8PB
MTG_HOLE
NC9
EMPTY

J9PB
MTG_HOLE
NC9
EMPTY

J2PB
MTG_HOLE
NC9
EMPTY

J7PB
MTG_HOLE
NC9
EMPTY

J10PB
MTG_HOLE
NC9
EMPTY

J4PB
MTG_HOLE
NC9
EMPTY

J6PB
MTG_HOLE
NC9
EMPTY

J11PB
MTG_HOLE
NC9
EMPTY

J3PB
MTG_HOLE
NC9
EMPTY

J5PB
MTG_HOLE
NC9
EMPTY

DESIGN NOTE:

LABELS

CHINA_ROHS
LB25PB
LABEL
EMPTY

B2_SILK
LB19PB
LABEL
EMPTY

VCCI_SILK
LB17PB
LABEL
EMPTY

SILK
LB9PB
C-TICK
EMPTY

E210882_LB
LB16PB
LABEL
EMPTY

BSMI_SILK
LB10PB
LABEL
EMPTY

UL_LABEL
LB15PB
LABEL
EMPTY

E2_SILK
LB18PB
LABEL
EMPTY

MIC_CPU
LB13PB
LABEL
EMPTY

E1_SILK
LB2PB
LABEL
EMPTY

FCCSILK
LB12PB
LABEL
EMPTY

PB_FREE_2LI
LB3PB
LABEL
EMPTY

CE_LABEL
LB11PB
LABEL
EMPTY

CANADA
LB21PB
LABEL
EMPTY

EMPTY
LB7PB
LABEL
INTEL_LOGO

1500X150_TARGET
LB6PB
LABEL
A30094-001

DESIGN NOTE:

CAD NOTE:

LB6PB: PLACE KOZ TARGET NEAR CPU AND DIMMS FOR BUILD/WOC NOTES

DESIGN NOTE: 200956-001 (NO CONCEPT MODEL): CE MARK SHOULD BE COVERED WITH BLANK WHITE LABEL UNTIL CERTIFIED (MAY NOT BE ON RVP DESIGNS)

DESIGN NOTE: 628492-001: FCC MARK SHOULD BE COVERED WITH BLANK WHITE LABEL UNTIL CERTIFIED (MAY NOT BE ON RVP DESIGNS)

DESIGN NOTE: 622954-001: C-TICK MARK SHOULD BE COVERED WITH BLANK WHITE LABEL UNTIL CERTIFIED (MAY NOT BE ON RVP DESIGNS)

DESIGN NOTE: KOREAN CERT (NO IPN, NO CONCEPT MODEL) SHOULD BE COVERED WITH BLANK WHITE LABEL UNTIL CERTIFIED (NOT ON RVP DESIGNS)

1375X250_TARGET
LB5PB
LABEL
A19177-001

DESIGN NOTE:

LB5PB: ISN BLANK LABEL AND KOZ

EMPTY
LB20PB
LABEL
1000X187

DESIGN NOTE:

SILK TARGET FOR PRODUCT CODE LABEL

[PAGE_TITLE=MTG HOLES/LABELS]

BPAGE DRAWING

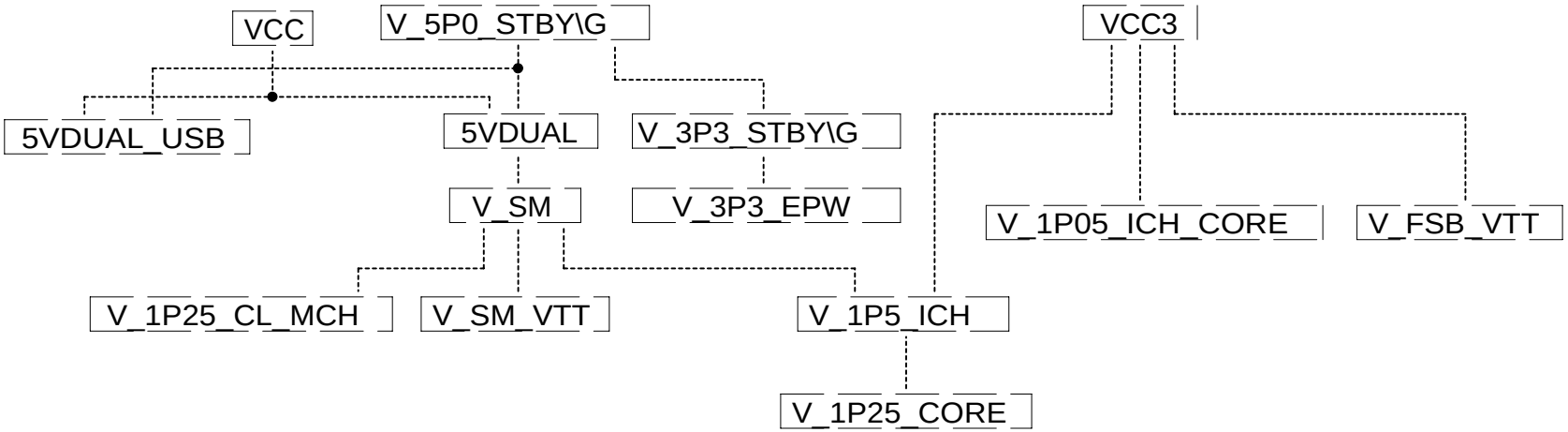
frostburg_fabc.sch_1.78
Sun Mar 18 18:44:42 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	78	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_B_ATX	06.12.2	2/8/07

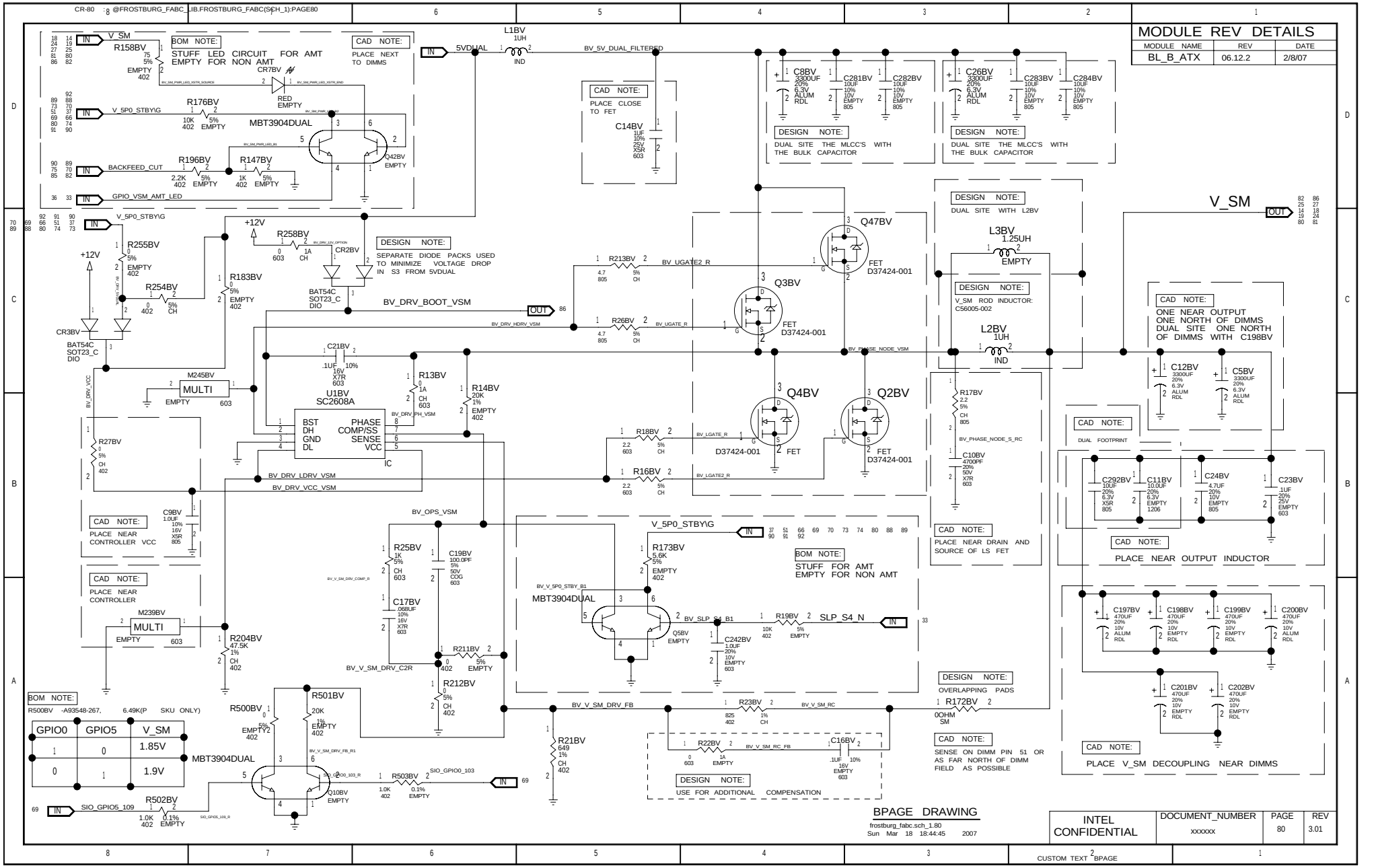
CORE VR MODULE

V_SM POWERED BY 5VDUAL
V_SM_VTT POWERED BY V_SM
V_1P5_ICH POWERED BY V_SM OR VCC3
V_1P25_CORE POWERED BY V_1P5_ICH
V_1P05_ICH_CORE POWERED BY VCC3
V_FSB_VTT POWERED BY VCC3
V_1P25_CL_MCH POWERED BY V_SM
5VDUAL_USB POWERED BY V_5P0_STBY\G AND VCC
5VDUAL POWERED BY V_5P0_STBY\G AND VCC
V_3P3_STBY\G POWERED BY V_5P0_STBY\G
V_3P3_EPW POWERED BY V_3P3_STBY\G



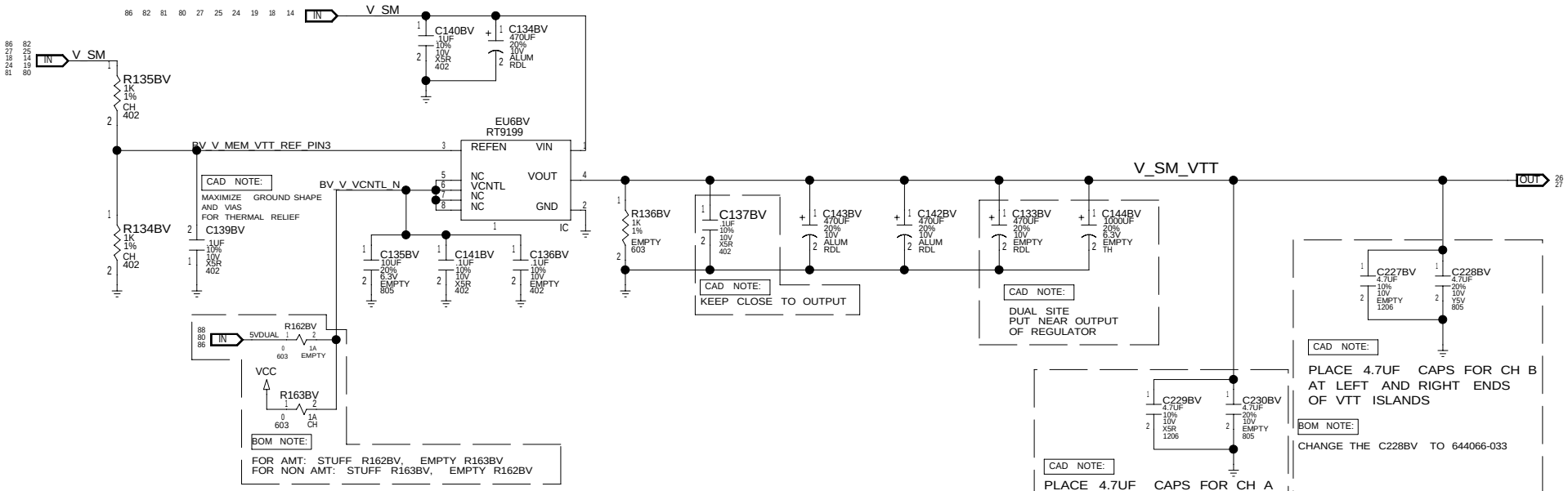
BPAGE DRAWING
frostburg_fabc.sch_1.79
Sun Mar 18 18:44:43 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	79	3.01


CR-80 : 8 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(SCH_1):PAGE80
MODULE REV DETAILS
MODULE NAME | REV | DATE
BL_B_ATX | 06.12.2 | 2/8/07
V_SM
R158BV
BOM NOTE:
STUFF LED CIRCUIT FOR AMT
EMPTY FOR NON AMT
CAD NOTE:
PLACE NEXT TO DIMMS
CR7BV
RED
EMPTY
V_5P0_STBY\G
R176BV
MBT3904DUAL
Q42BV
BACKFEED_CUT
R196BV
R147BV
GPIO_VSM_AMT_LED
5VDUAL
L1BV
1UH
IND
BV_5V_DUAL_FILTERED
CAD NOTE:
PLACE CLOSE TO FET
C14BV
C8BV
C281BV
C282BV
C26BV
C283BV
C284BV
DESIGN NOTE:
DUAL SITE THE MLCC'S WITH THE BULK CAPACITOR
DESIGN NOTE:
DUAL SITE WITH L2BV
L3BV
1.25UH
EMPTY
DESIGN NOTE:
V_SM ROD INDUCTOR: C5600S-002
L2BV
1UH
IND
V_SM
OUT
CAD NOTE:
ONE NEAR OUTPUT
ONE NORTH OF DIMMS
DUAL SITE ONE NORTH OF DIMMS WITH C198BV
C12BV
C5BV
CAD NOTE:
DUAL FOOTPRINT
C292BV
C11BV
C24BV
C23BV
CAD NOTE:
PLACE NEAR OUTPUT INDUCTOR
C197BV
C198BV
C199BV
C200BV
C201BV
C202BV
CAD NOTE:
PLACE V_SM DECOUPLING NEAR DIMMS
+12V
R255BV
R254BV
R258BV
CR2BV
BAT54C SOT23_C DIO
DESIGN NOTE:
SEPARATE DIODE PACKS USED TO MINIMIZE VOLTAGE DROP IN S3 FROM 5VDUAL
CR3BV
R183BV
BV_DRV_BOOT_VSM
Q47BV
Q3BV
Q4BV
Q2BV
FET D37424-001
R213BV
R26BV
BV_UGATE2_R
BV_UGATE_R
BV_DRV_HDRV_VSM
BV_PHASE_NODE_VSM
M245BV
MULTI
C21BV
U1BV
SC2608A
BST
DH
GND
DL
PHASE
COMP/SS
SENSE
VCC
IC
R13BV
R14BV
R18BV
R16BV
BV_LGATE_R
BV_LGATE2_R
R17BV
BV_PHASE_NODE_S_RC
C10BV
CAD NOTE:
PLACE NEAR DRAIN AND SOURCE OF LS FET
BV_DRV_VCC
R27BV
BV_DRV_LDRV_VSM
BV_DRV_VCC_VSM
C9BV
CAD NOTE:
PLACE NEAR CONTROLLER VCC
CAD NOTE:
PLACE NEAR CONTROLLER
M239BV
R204BV
BV_OPS_VSM
R25BV
C19BV
C17BV
BV_V_SM_DRV_C2R
R211BV
R212BV
V_5P0_STBY\G
R173BV
BOM NOTE:
STUFF FOR AMT
EMPTY FOR NON AMT
BV_V_5P0_STBY_B1
MBT3904DUAL
Q5BV
BV_SLP_S4_B1
R19BV
SLP_S4_N
C242BV
BV_V_SM_DRV_FB
R23BV
BV_V_SM_RC
R172BV
0OHM
SM
DESIGN NOTE:
OVERLAPPING PADS
CAD NOTE:
SENSE ON DIMM PIN 51 OR AS FAR NORTH OF DIMM FIELD AS POSSIBLE
R22BV
C16BV
DESIGN NOTE:
USE FOR ADDITIONAL COMPENSATION
R21BV
BOM NOTE:
R500BV -A93548-267, 6.49K(P SKU ONLY)
GPIO0 | GPIO5 | V_SM
1 | 0 | 1.85V
0 | 1 | 1.9V
R500BV
R501BV
MBT3904DUAL
Q10BV
SIO_GPIO0_103
R503BV
SIO_GPIO5_109
R502BV
BPAGE DRAWING
frostburg_fabc.sch_1.80
Sun Mar 18 18:44:45 2007
INTEL CONFIDENTIAL
DOCUMENT_NUMBER: xxxxxx
PAGE: 80
REV: 3.01
CUSTOM TEXT 2 BPAGE

CR-81 : 8 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(SCH_1):PAGE81

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_B_ATX	06.12.2	2/8/07



[PAGE_TITLE=VREG_SM_VTT]

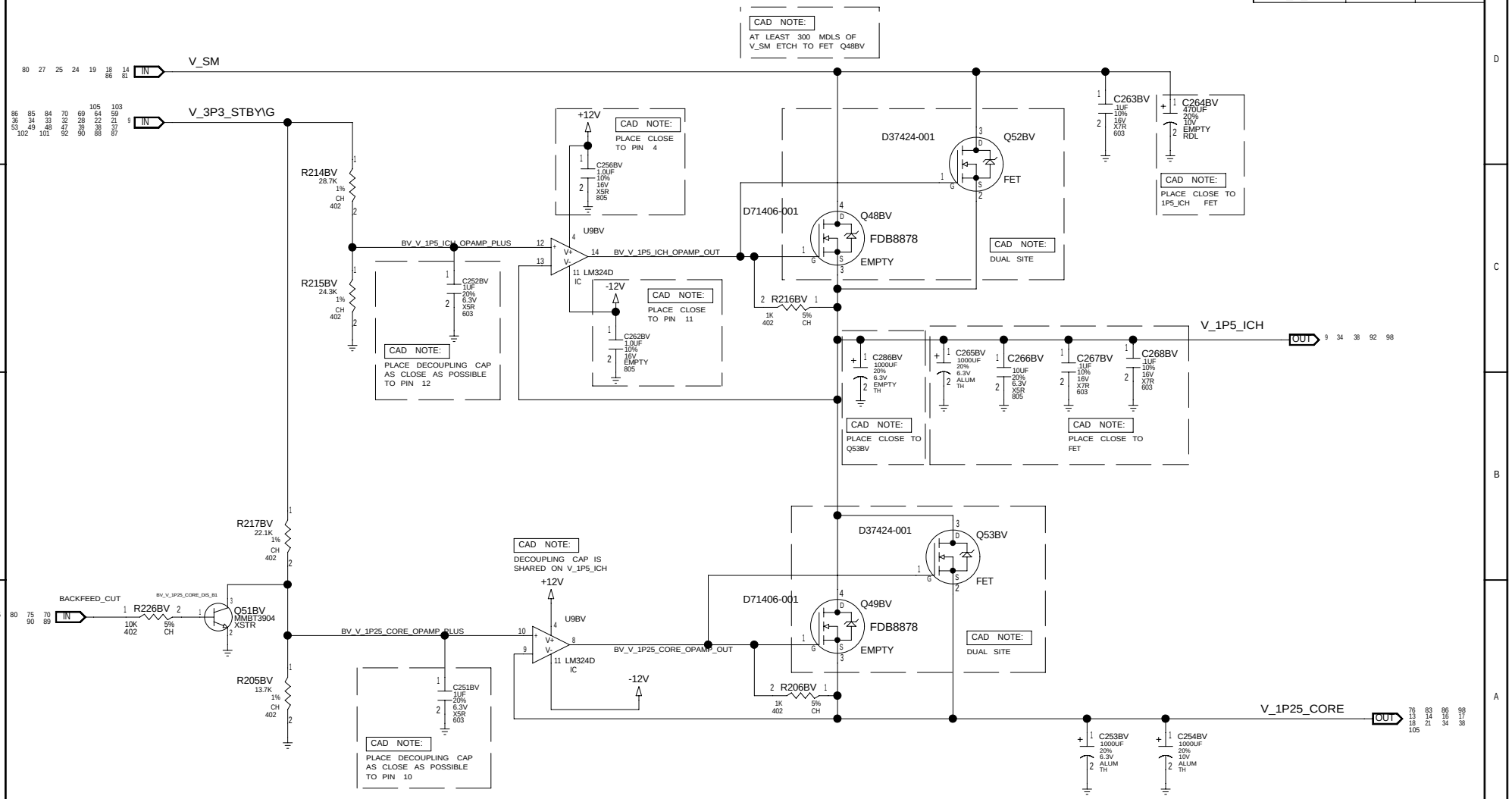
BPAGE DRAWING

frostburg_fabc.sch_1.81
Sun Mar 18 18:44:45 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	81	3.01

CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_B_ATX	06.12.2	2/8/07



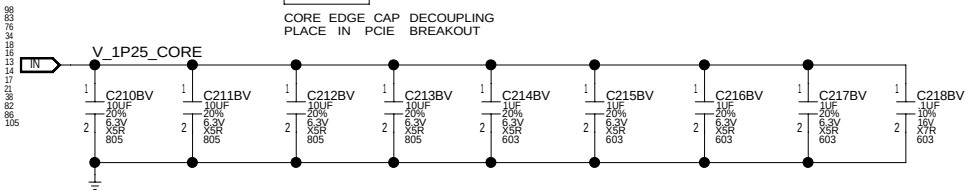
[PAGE_TITLE=VREG_1P25_CORE MCH]

BPAGE DRAWING
frostburg_fabc.sch_1.82
Sun Mar 18 18:44:47 2007

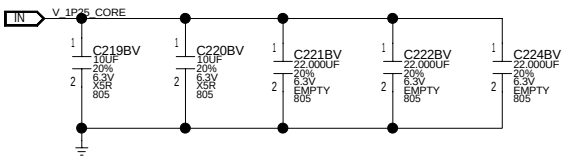
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	82	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_B_ATX	06.12.2	2/8/07

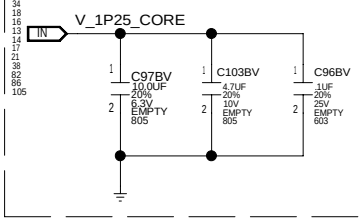
CAD NOTE:
CORE EDGE CAP DECOUPLING
PLACE IN PCIE BREAKOUT



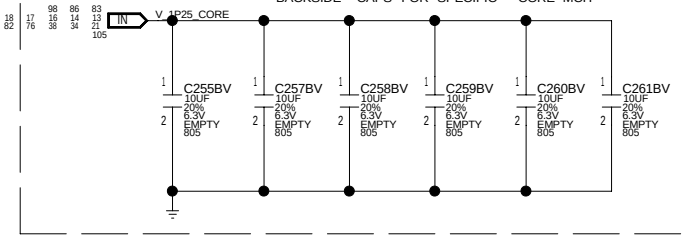
CAD NOTE:
CORE DECOUPLING CAPS FOR MCH
PLACE NEXT TO PWR CORRIDOR



CAD NOTE:
DECOUPLING CAPS AT OUTPUT OF REGULATOR



DESIGN NOTE:
BACKSIDE CAPS FOR SPECIFIC CORE MCH

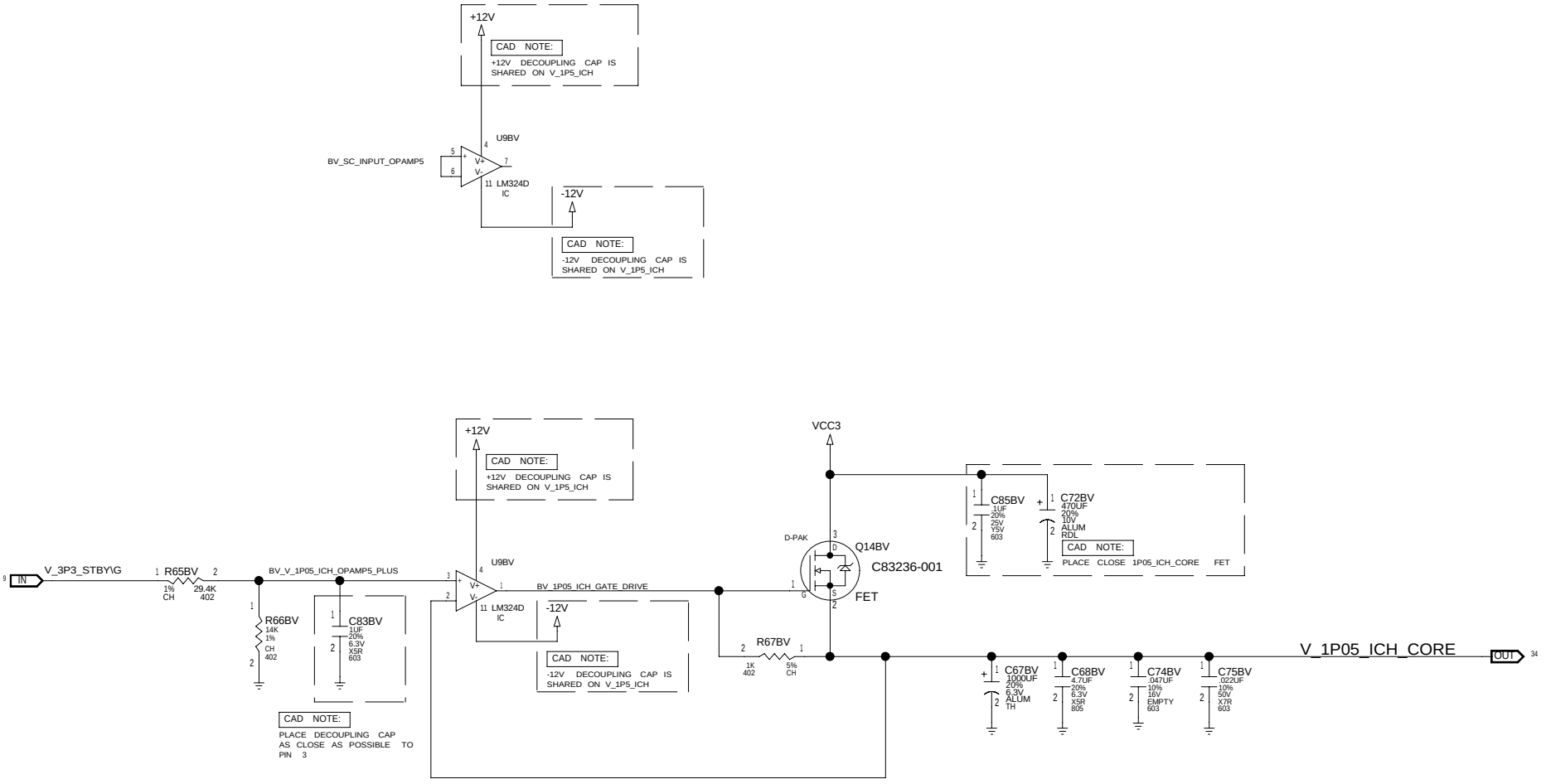


[PAGE_TITLE=MCH DCPL]

BPAGE DRAWING
frostburg_fabc.sch_1.83
Sun Mar 18 18:44:48 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	83	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_B_ATX	06.12.2	2/8/07

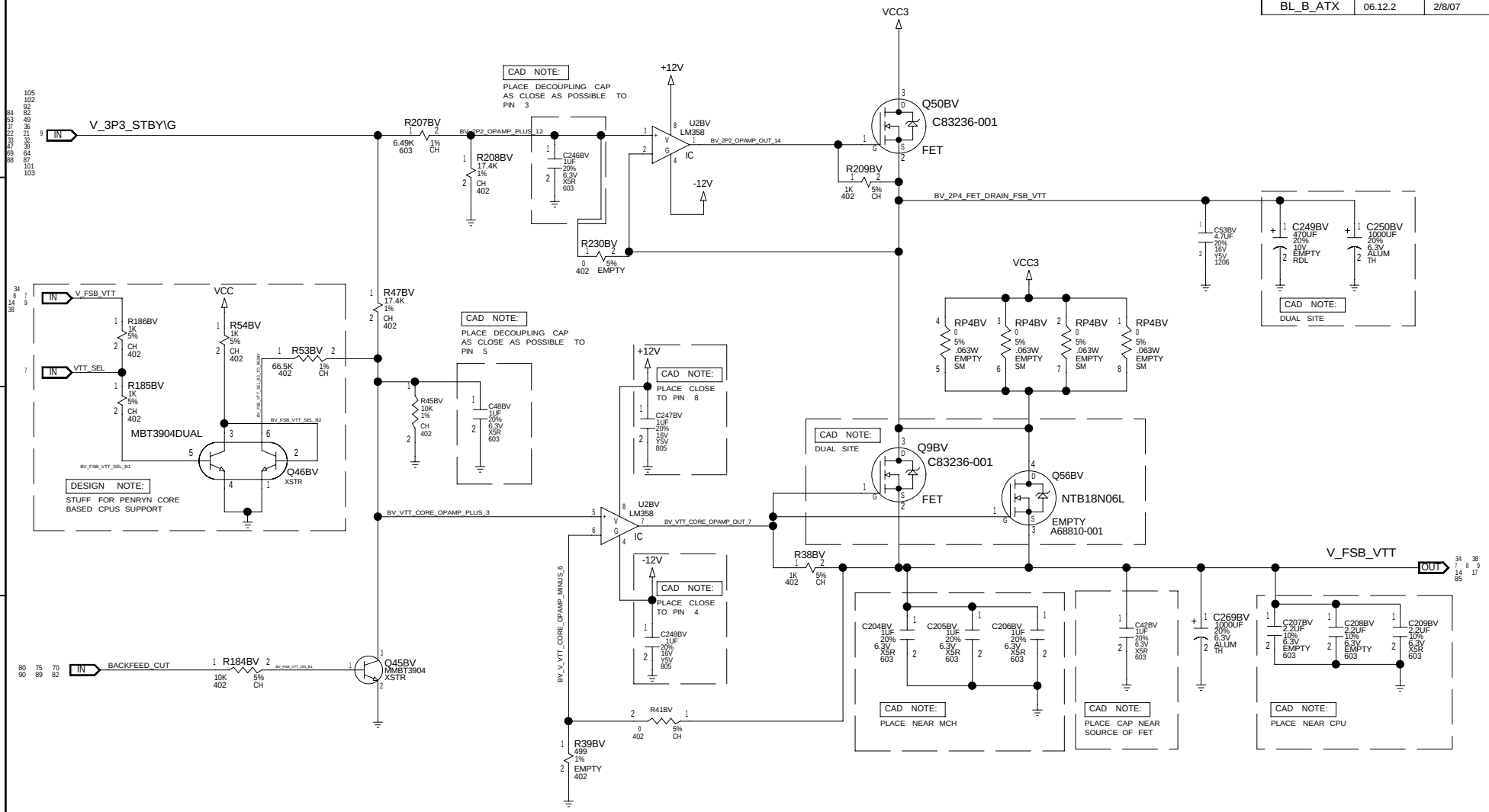


BPAGE DRAWING

frostburg_fabc.sch_1.84
Sun Mar 18 18:44:50 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	84	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_B_ATX	06.12.2	2/8/07



BPAGE DRAWING

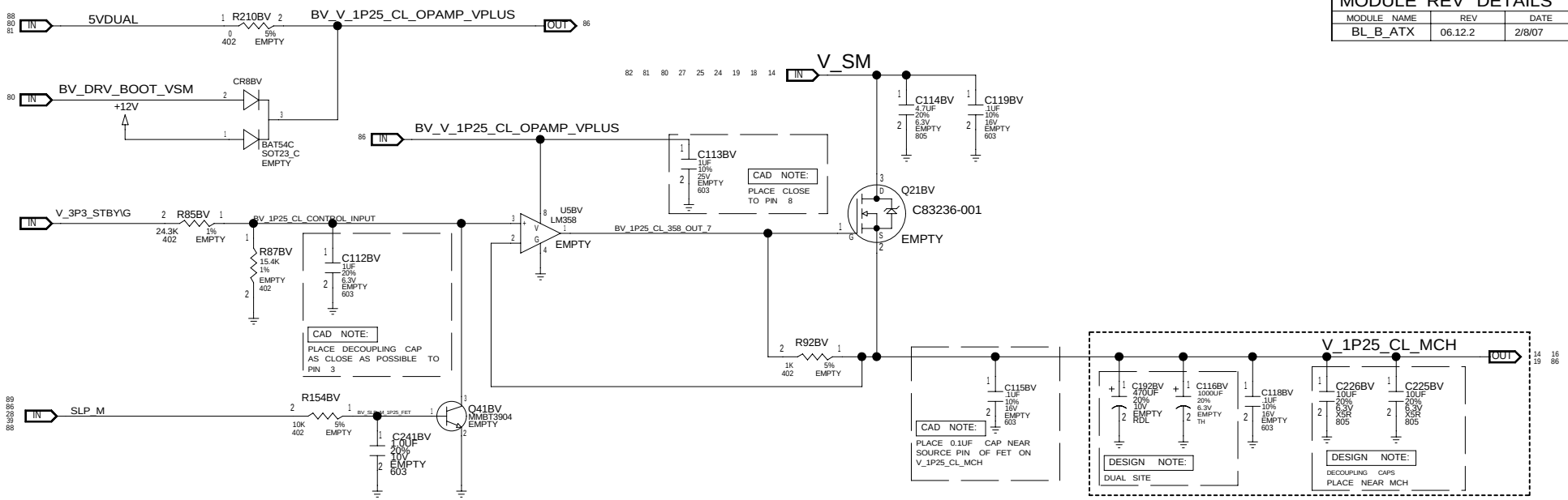
frostburg_fabc.sch_1.85
Sun Mar 18 18:44:51 2007

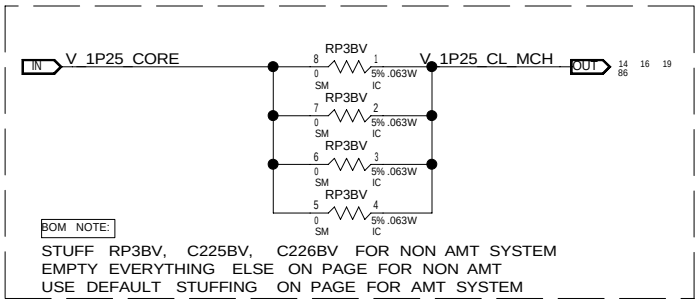
[PAGE_TITLE=VREG_FSB VTT & SFR]

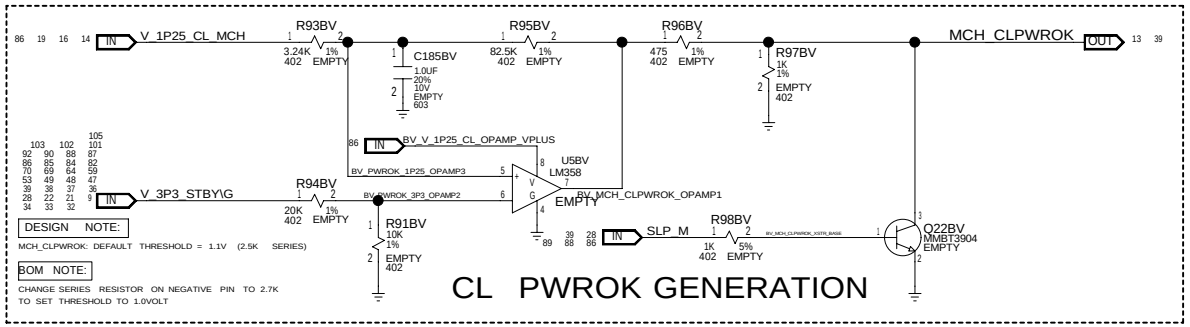
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	85	3.01

CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_B_ATX	06.12.2	2/8/07





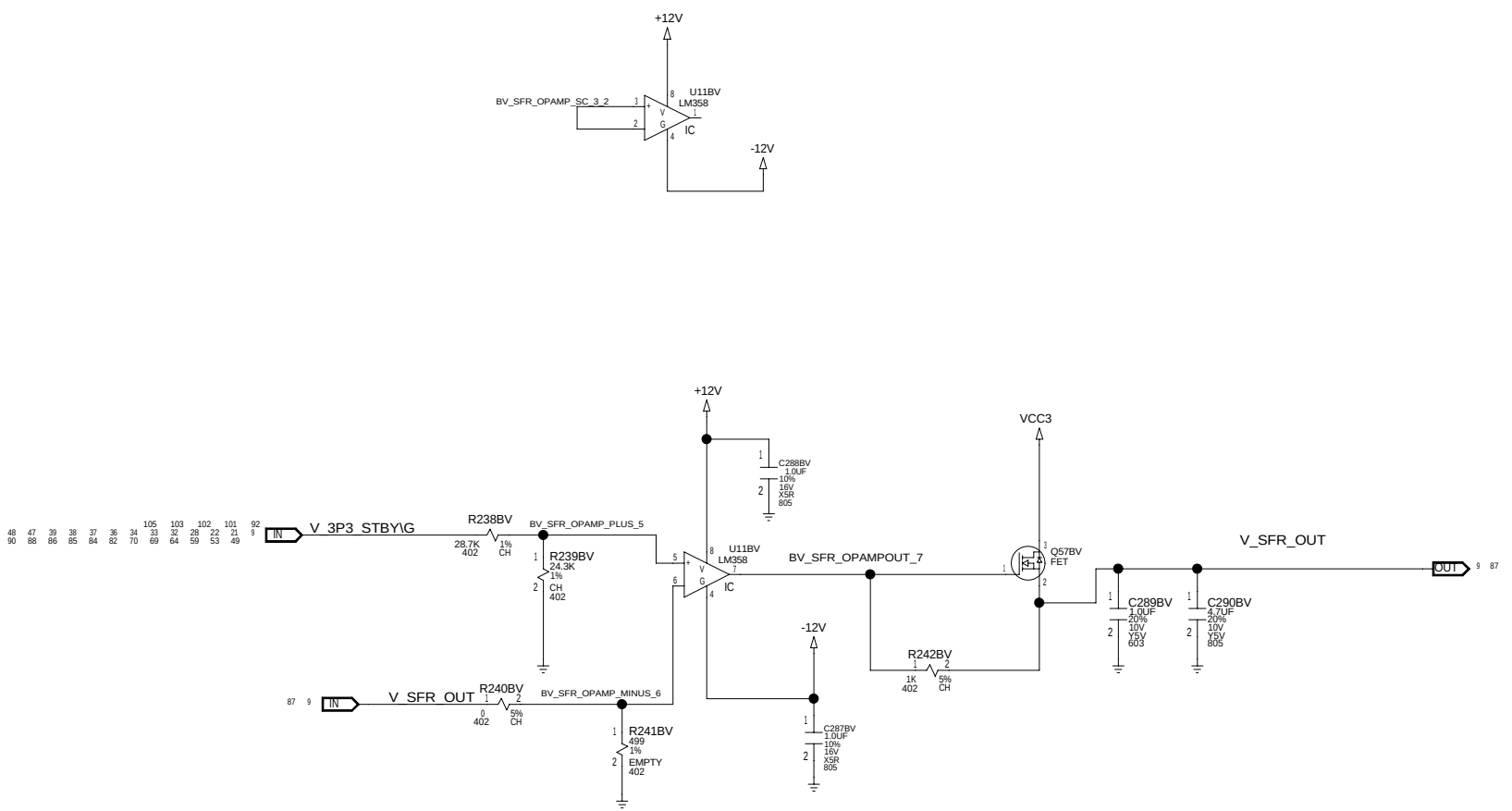


[PAGE_TITLE=VREG 1.25 MCH CL]

BPAGE DRAWING
frostburg_fabc.sch_1.86
Sun Mar 18 18:44:53 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	86	3.01

MODULE_REV_DETAILS		
MODULE_NAME	REV	DATE
BL_B_ATX	06.12.2	2/8/07



[PAGE_TITLE=CORE VREG]

BPAGE DRAWING

frostburg_fabc.sch_1.87
Sun Mar 18 18:44:54 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	87	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_B_ATX	06.12.2	2/8/07

5V_DUAL

BOM NOTE:
NON AMT STUFF
Q34BV Q35BV

Q34BV
PMOSFET
C77877-001

Q36BV
FDC638P

IN VREG_5VDUAL_PCH
IN V_5P0_STBY\G

BOM NOTE:
(DEFAULT) AMT STUFF
Q36BV Q35BV

EMPTY
1.0

5VDUAL OUT 80 81 86 88

Q35BV

IN VREG_5VDUAL_NCH

FET
D37438-001

CAD NOTE:
0.1 INCH COPPER ON DRAIN AND SOURCE

VCC

V_3P3_EPW

IN V_3P3_STBY\G

IN V_3P3_STBY\G

IN SLP_M
R137BV 1K 402 5% EMPTY

BV_SLP_M_R

Q31BV
EMPTY
D32396-001

IN WOL_ONLY
R138BV 10K 402 5% EMPTY
BV_WOL_CNTL_BASE

Q30BV
MMBT3904
EMPTY

C233BV
1UF 20% 6.3V
EMPTY
603

R140BV 0 1A CH 805

VCC3

R139BV 0 1A EMPTY 805

BOM NOTE:
STUFF FOR NON-INTEL LAN OR M0 ONLY

V_3P3_EPW OUT

BOM NOTE:
STUFF FOR NINEVEH + AMT

BOM NOTE:
STUFF FOR NON AMT

5VDUAL

IN 5VDUAL

R235BV 0 5% CH 402
R143BV 0 1A CH 603
RP2BV 0 5% .063W IC SM
RP2BV 0 5% .063W IC SM
RP2BV 0 5% .063W IC SM
RP2BV 0 5% .063W IC SM
R224BV 0 5% CH 402
R225BV 0 1A CH 603
R234BV 0 5% CH 402
R231BV 0 5% CH 402
R232BV 0 5% CH 402
R233BV 0 5% CH 402
R236BV 0 5% CH 402
R237BV CH 0 402 5%

BOM NOTE:
STUFF ONLY IF 5V_DUAL USB VR IS EMPTY

5VDUAL_USB OUT 42 43 44 45 46 52 88 91 92

5V_DUAL USB VR

Q32BV

IN VREG_USB_PCH
EMPTY
C77877-001

IN V_5P0_STBY\G

BOM NOTE:
NON AMT STUFF R143BV, RP2BV, R224BV, R225BV
EMPTY Q32BV, Q33BV
(DEFAULT) AMT STUFF Q32BV, Q33BV
EMPTY R143BV, RP2BV, R224BV, R225BV

5VDUAL_USB OUT 42 43 44 45 46 52 88 91 92

Q33BV

CAD NOTE:
0.1 INCH COPPER ON DRAIN AND SOURCE

IN VREG_USB_NCH
EMPTY
D37438-001

VCC

CAD NOTE:
OVERLAPPING SITE

U7BV
LD1117DT
IN OUT GND
EMPTY

BOM NOTE:
STUFF FOR 10/100 LAN SKUS
EMPTY FOR GB LAN SKUS

U8BV
AD1086
IN OUT GND
SM

IN V_5P0_STBY\G

C182BV 1.0UF 20% 10V Y5V 603

V_3P3_STBY\G OUT

C183BV 220UF 20.0% 25V ELEC RDL

R142BV 274 1% EMPTY 402

BV_V_STBY_ADJ

R141BV 0 5% CH 402

C184BV .1UF 20% 25V EMPTY 603

BOM NOTE:
STUFF FOR LD1117 (10/100 LAN SKUS)
EMPTY FOR EZ1086 (GB LAN SKUS)

BOM NOTE:
STUFF 453 OHM (A93548-165) FOR LD1117 (10/100 LAN SKUS)
STUFF O OHM (A93549-001) FOR EZ1086 (GB SKUS)

BPAGE DRAWING
frostburg_fabc.sch_1.88
Sun Mar 18 18:44:56 2007

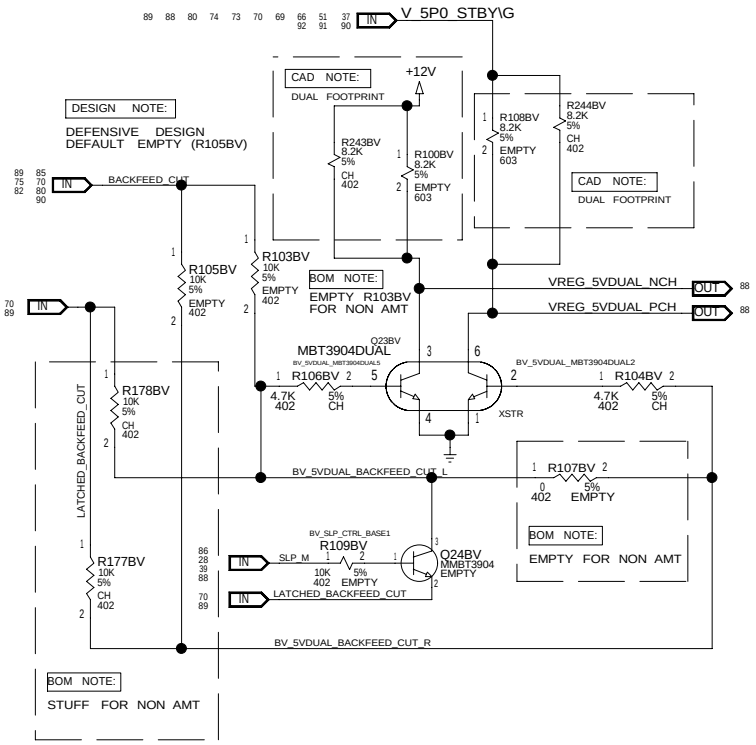
[PAGE_TITLE=CORE VREG]

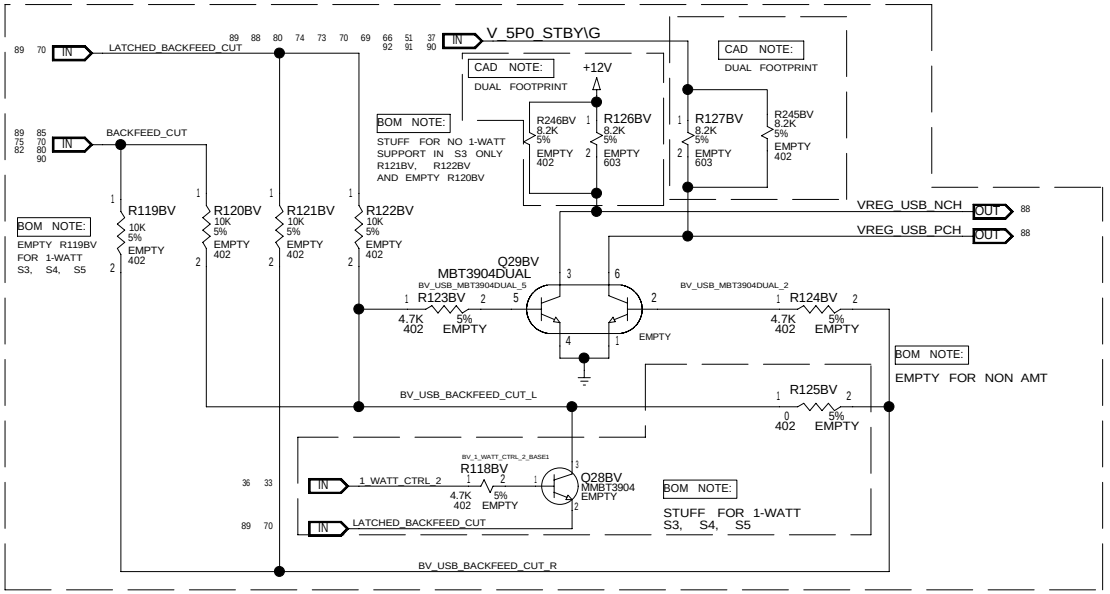
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	88	3.01

CUSTOM TEXT 2 BPAGE

CR-89 : 8 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(SCH_1):PAGE89

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_B_ATX	06.12.2	2/8/07





BPAGE DRAWING

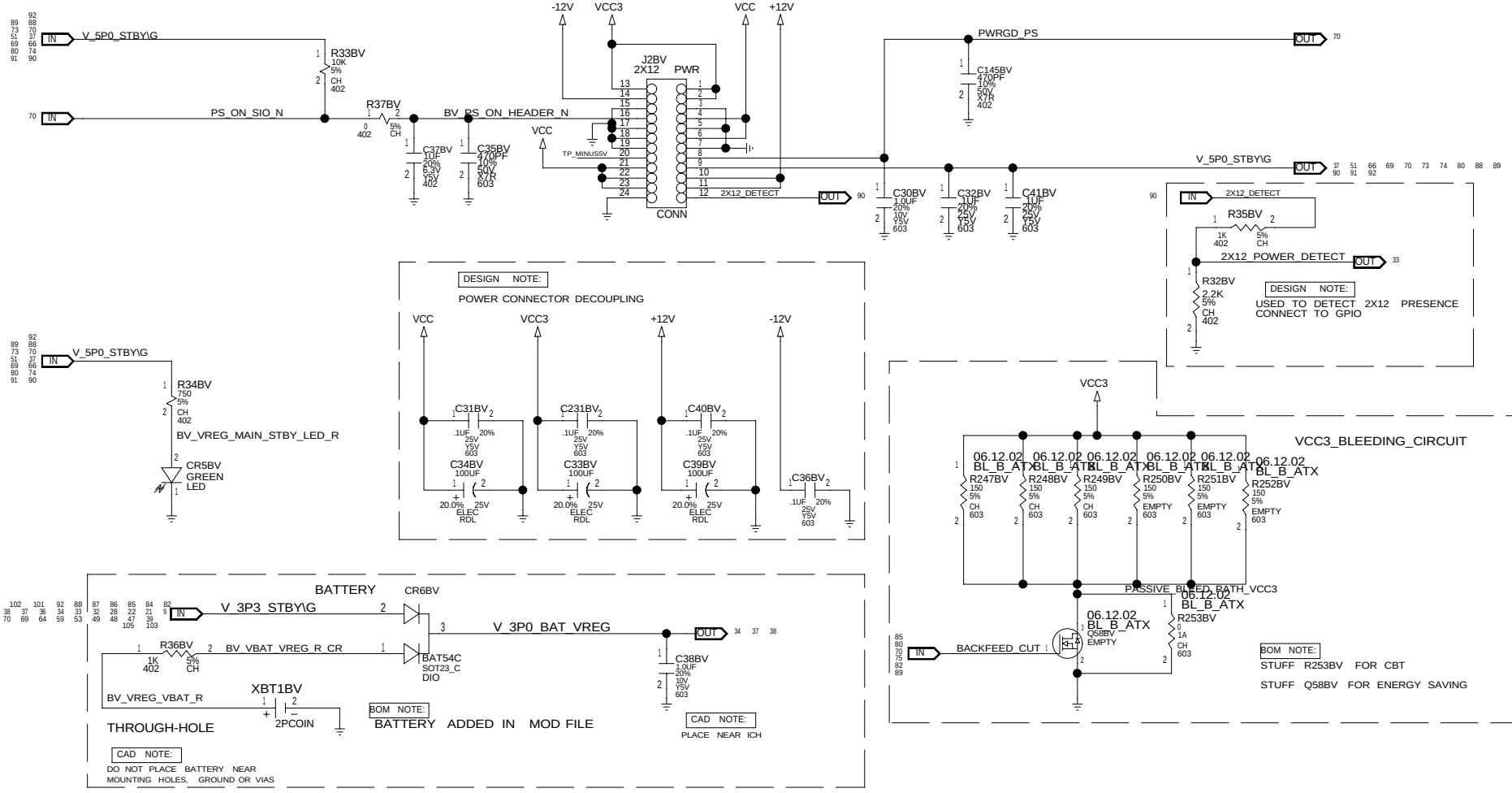
frostburg_fabc.sch_1.89
Sun Mar 18 18:44:57 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	89	3.01

CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS

MODULE NAME	REV	DATE
BL_B_ATX	06.12.2	2/8/07

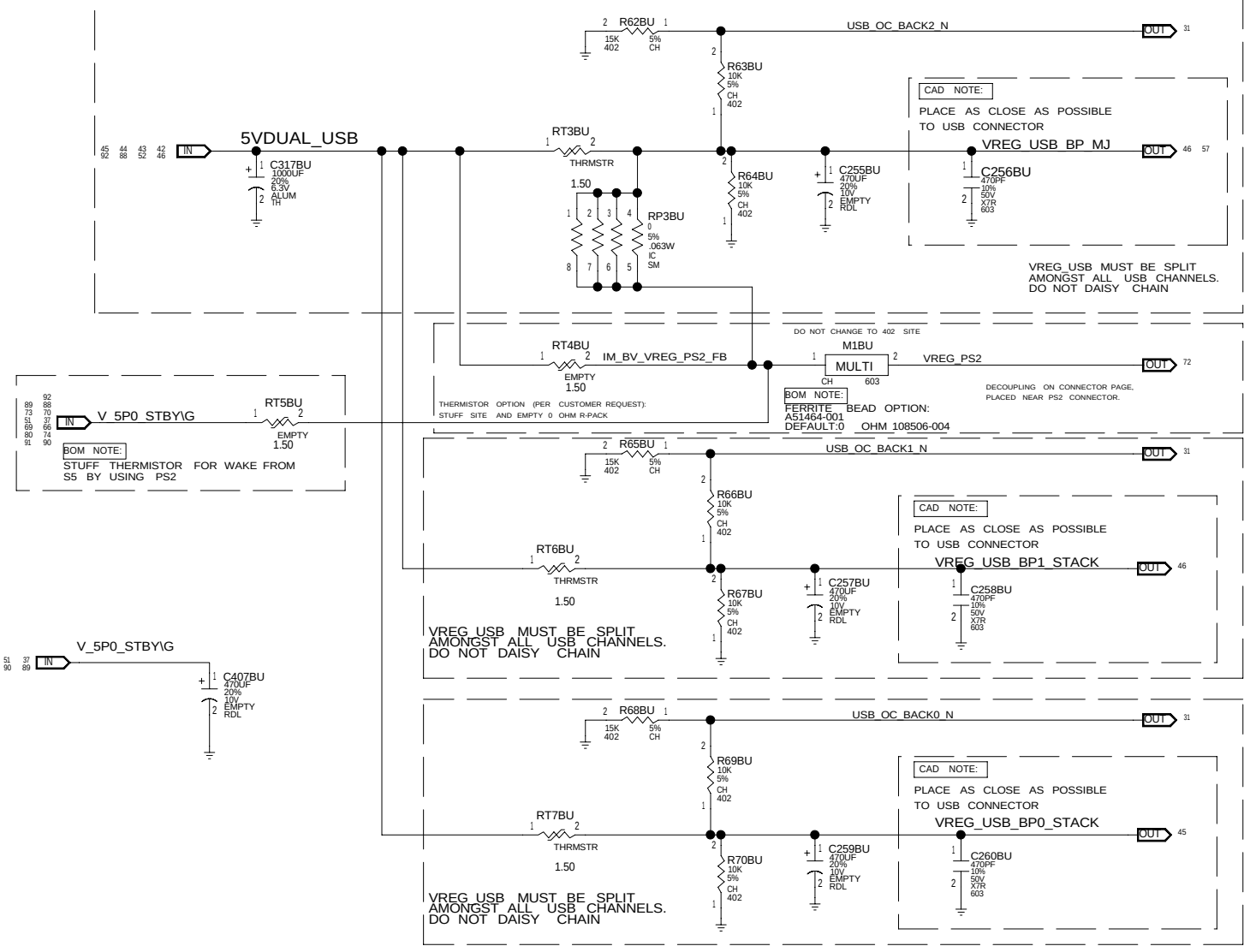


BPAGE DRAWING

frostburg_fabc.sch_1.90
Sun Mar 18 18:44:59 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	90	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=CORE VREG]

[PAGE_TITLE=WAKE CONTROL SWITCH PS2/USB (BP RIGHT)]

BPAGE DRAWING

frostburg_fabc.sch_1.91
Sun Mar 18 18:45:00 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	91	3.01

MODULE REV DETAILS		
MODULE NAME	REV	DATE

DESIGN NOTE: BOARD GENERAL DCPL CAPS

CAD NOTE: EMI CAPS PLACE CLOSE BP AUDIO CONN

AUD_GND — IN — C79BU .1UF 25V Y5V 603

CAD NOTE: PEG SLOT — C53BU .1UF 20% 25V EMPTY 603

V_5P0_STBY\G — IN — VCC — C41BU .1UF 20% 25V EMPTY 603 — CAD NOTE: PWR CONN

C42BU .1UF 20% 25V Y5V 603 — CAD NOTE: PCI SLOT

C43BU .1UF 20% 25V Y5V 603 — CAD NOTE: PCI SLOT

C167BU .1UF 20% 25V EMPTY 603 — CAD NOTE: FP HDR

C169BU 22UF 20.0% 25V ELEC RDL "THMNT ALUM ELEC"

DESIGN NOTE: GNR BULK DCPL

-12V — C178BU .1UF 20% 25V EMPTY 603 — CAD NOTE: PWR CONN

C173BU .1UF 20% 25V EMPTY 603 — CAD NOTE: PCI SLOT

V_1P5_ICH — IN — VCC — C401BU .1UF 10% 10V X5R 402 — C413BU .1UF 10% 10V EMPTY 402

VCC3 — C352BU .1UF 10% 10V EMPTY 402 — C350BU .1UF 20% 25V EMPTY 603 — C353BU .1UF 10% 10V EMPTY 402

V_3P3_STBY\G — IN — CAD NOTE: VCC3 AZ_HDR EMI CAPS PLACE NEAR J7AU — C25BU .1UF 20% 25V EMPTY 603

VCC3 — C406BU .1UF 10% 10V EMPTY 402

CAD NOTE: FOR HSYNC & VSYNC ABOVE NORTH OF MCH TRANSITION — C152BU .1UF 20% 25V EMPTY 603

+12V — C333BU .1UF 10% 10V X5R 402 — CAD NOTE: CLOSE TO PATA

+12V — C323BU .1UF 20% 25V Y5V 603

+12V — C324BU .1UF 20% 25V Y5V 603 — CAD NOTE: USB AND CLOCK

VCC — C402BU .1UF 10% 10V X5R 402

VCC3 — C403BU .1UF 10% 10V X5R 402

DESIGN NOTE: STITCHING CAPS

+12V — C148BU .1UF 20% 25V Y5V 603 — CAD NOTE: FOR ICH_LAN_JCLK PLACE BELOW Y1LN

+12V — C19BU .1UF 20% 25V Y5V 603 — LAN_V_1P0 — OUT 56 58

C20BU .1UF 20% 25V Y5V 603 — CAD NOTE: GCL STITCHING CAPS PLACE NEAR LEFT SIDE OF U1LN

CAD NOTE: BP USB PLACE NEAR THE JA1LN — 5VDUAL_USB — OUT 42 43 44 45 46 52 88 91 92

C15BU .1UF 20% 25V Y5V 603 — C320BU .1UF 20% 25V Y5V 603

C8BU .1UF 20% 25V Y5V 603 — C321BU .1UF 20% 25V Y5V 603

C5BU .1UF 20% 25V Y5V 603

+12V — C388BU .1UF 20% 25V Y5V 603

VCC — C389BU .1UF 10% 10V X5R 402 — +12V

CAD NOTE: FP USB STITCHING CAPS PLACE CLOSE TO J8BU AND J9BU

+12V — C66BU .1UF 20% 25V Y5V 603 — C67BU .1UF 20% 25V Y5V 603

VCC — C409BU .1UF 10% 10V X5R 402 — C411BU .1UF 10% 10V EMPTY 402

+12V — C410BU .1UF 10% 10V X5R 402

DESIGN NOTE: CLOCK STITCHING CAPS

VCC3 — CAD NOTE: PLACE CLOSE TO Q50BV — C331BU .1UF 20% 25V Y5V 603

VCC3 — CAD NOTE: FOR CK_PE_100M_PATA — C299BU .1UF 20% 25V Y5V 603

V_5P0_STBY\G — OUT — C334BU 0.1UF 20% 16V Y5V 402

V_3P3_EPW — OUT 27 28 33 34 38 39 40 56 57 58 — C335BU 0.1UF 20% 16V Y5V 402

5VDUAL_USB — IN — C354BU 0.1UF 20% 16V EMPTY 402 — C355BU .01UF 10% 25V EMPTY 402

+12V — C356BU .1UF 20% 25V EMPTY 603

+12V — C385BU .1UF 10% 10V X5R 402 — C386BU .1UF 10% 10V X5R 402

C387BU .1UF 10% 10V X5R 402 — C412BU .1UF 10% 10V X5R 402

CAD NOTE: CK_P_33M_PA PLACE NEXT TO SOUTH OF U1CK — VCC3 — C70BU .1UF 10% 16V X7R 603

+12V — CAD NOTE: CK_1PORT_S3_DN/S2_DN PLACE NEAR LEFT SIDE OF U1LN — C271BU .1UF 10% 10V X5R 402 — C31BU .1UF 20% 25V Y5V 603

BOM NOTE: STUFF FOR ATX ONLY

VCC3 — C71BU .1UF 10% 16V X7R 603 — C26BU .1UF 20% 25V Y5V 603

VCC3 — C332BU .1UF 10% 10V X5R 402

CAD NOTE: CK_14M_ICH PLACE NEAR C244BU

VCC — C400BU .1UF 10% 10V X5R 402 — C351BU .1UF 10% 10V X5R 402

CAD NOTE: CK_P_33M_TPM\PA PLACE NEAR C72BV

VCC3 — VCC — C146BU .1UF 10% 10V X5R 402

CAD NOTE: CK_PE_33M_TPM PLACE NEAR C12BV

VCC3 — C277BU .1UF 10% 10V X5R 402

VCC — C282BU .1UF 10% 10V X5R 402

CAD NOTE: CK_P_33M_TPM PLACE NEXT TO C12BV

DESIGN NOTE: PATA STITCHING CAPS

CAD NOTE: PLACE BETWEEN JIPT AND U1PT

+12V — C30BU .1UF 10% 10V EMPTY 402 — C33BU .1UF 10% 10V EMPTY 402

DESIGN NOTE: PCIEX1 STITCHING CAPS

CAD NOTE: PLACE NEAR SOUTH OF U1FW

VCC — C38BU .1UF 10% 10V X5R 402 — C34BU .1UF 10% 10V X5R 402

C275BU .1UF 10% 10V X5R 402 — C276BU .1UF 10% 10V X5R 402

CAD NOTE: PLACE NEAR SOUTH OF Y1PT

VCC — C278BU .1UF 10% 10V X5R 402 — C279BU .1UF 10% 10V X5R 402

C280BU .1UF 10% 10V X5R 402 — C281BU .1UF 10% 10V X5R 402

DESIGN NOTE: AZALIA STITCHING CAPS

+12V — C330BU 0.1UF 20% 16V Y5V 402

+12V — C287BU 0.1UF 20% 16V EMPTY 402

+12V — C305BU 0.1UF 20% 16V Y5V 402

C408AU 470PF 10% 50V X7R 402 — V_AUD

CAD NOTE: 1394 STITCHING CAPS PLACE NEXT TO J33LB

VCC3 — C61BU .1UF 20% 25V Y5V 603

VCC — C329BU .1UF 20% 25V Y5V 603

VCC3 — C102BU 0.1UF 20% 16V Y5V 402

+12V — C103BU 0.1UF 20% 16V Y5V 402

+12V — C104BU 0.1UF 20% 16V Y5V 402

CAD NOTE: STITCHING CAPS FOR CK505

[PAGE_TITLE=VREG: DECOUPLING AND STITCHING]

BPAGE DRAWING

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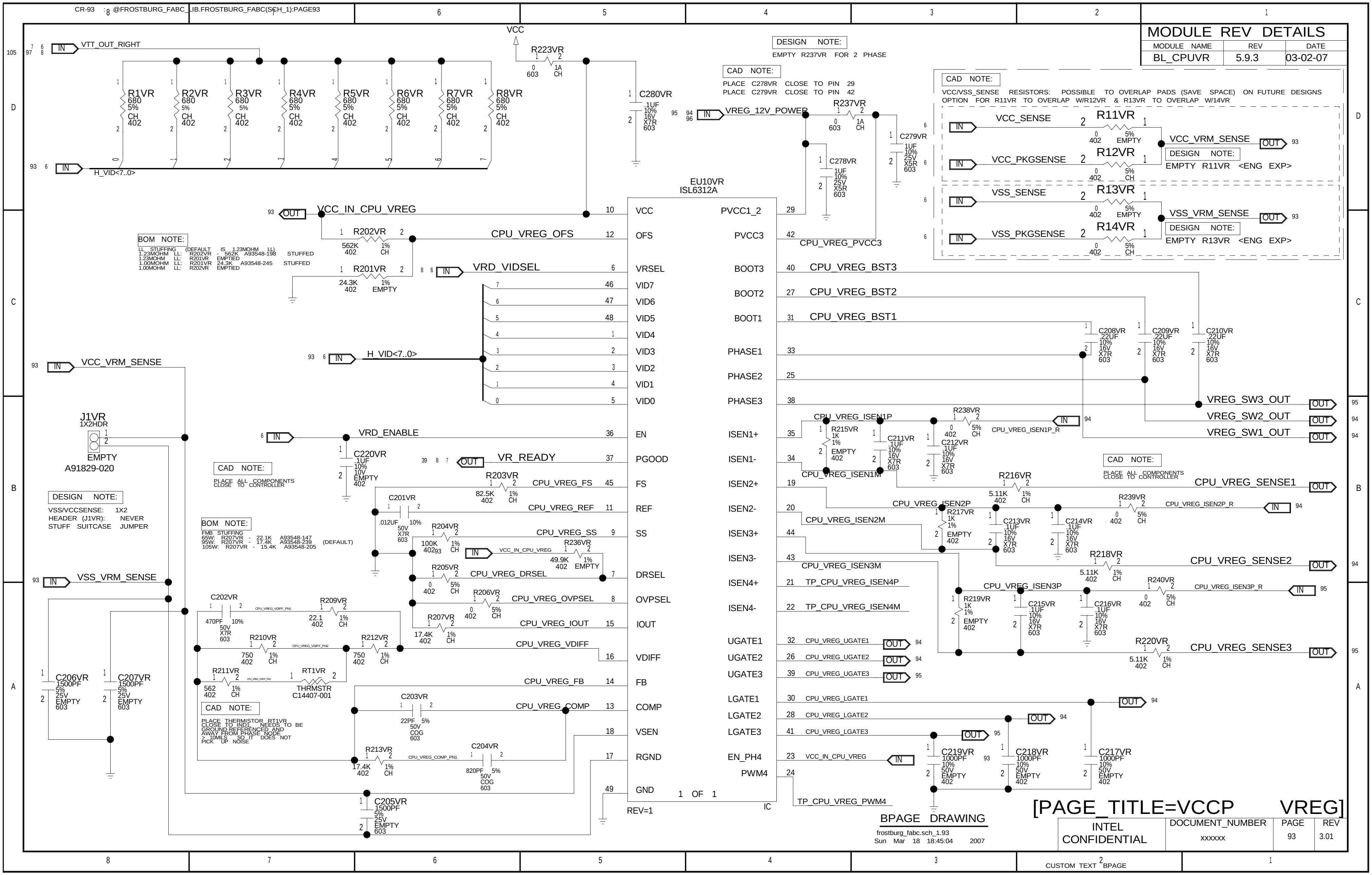
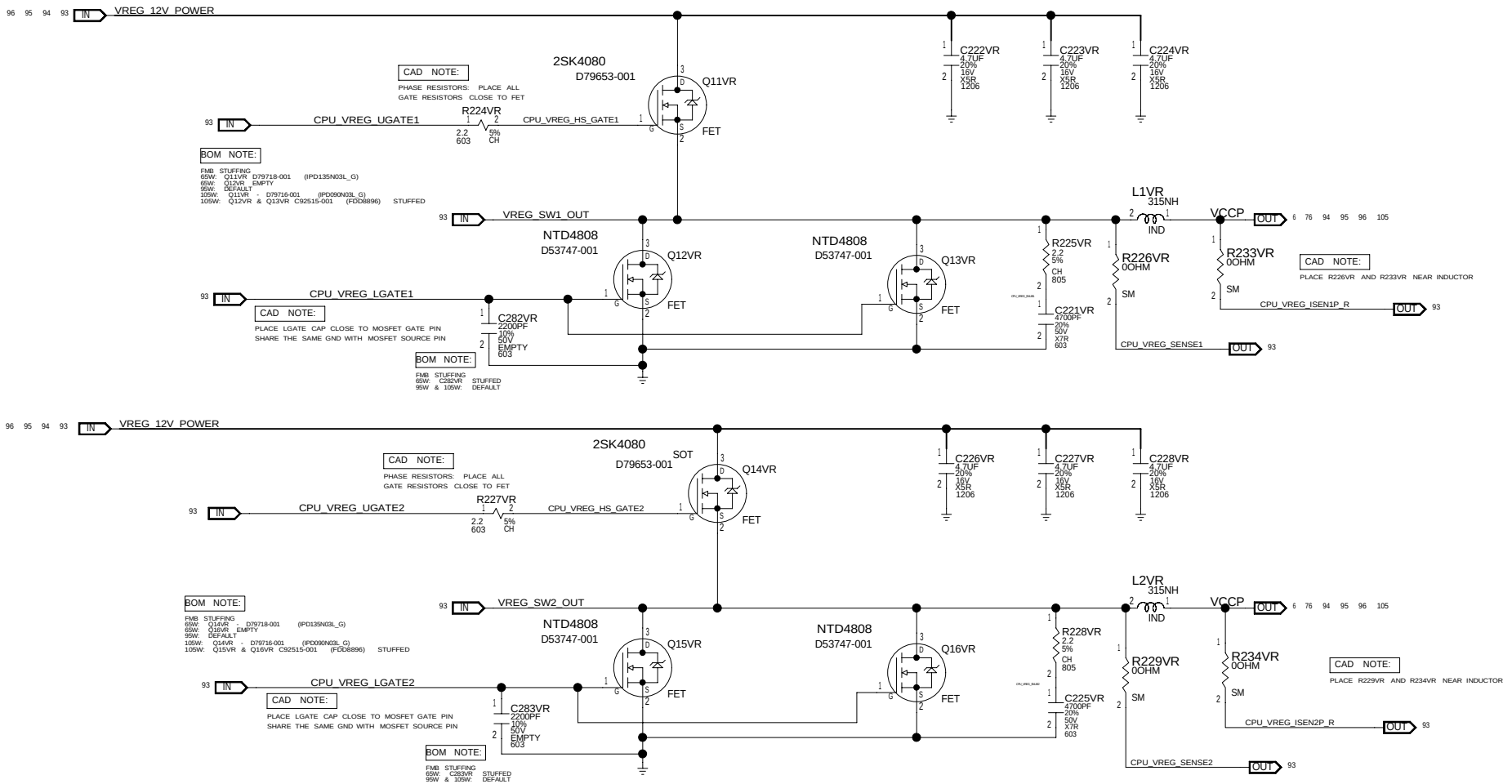
Sun Mar 18 18:45:02 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	92	3.01


CR-93 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(SCH_1):PAGE93
MODULE REV DETAILS
MODULE NAME
REV
DATE
BL_CPUVR
5.9.3
03-02-07
VCC
R223VR
603
1A
CH
VTT_OUT_RIGHT
R1VR 680 5% CH 402
R2VR 680 5% CH 402
R3VR 680 5% CH 402
R4VR 680 5% CH 402
R5VR 680 5% CH 402
R6VR 680 5% CH 402
R7VR 680 5% CH 402
R8VR 680 5% CH 402
H_VID<7..0>
C280VR
.1UF
10%
16V
X7R
603
DESIGN NOTE:
EMPTY R237VR FOR 2 PHASE
CAD NOTE:
PLACE C278VR CLOSE TO PIN 29
PLACE C279VR CLOSE TO PIN 42
VREG_12V_POWER
R237VR
C279VR
1UF
10%
25V
X5R
603
C278VR
1UF
10%
25V
X5R
603
CAD NOTE:
VCC/VSS_SENSE RESISTORS: POSSIBLE TO OVERLAP PADS (SAVE SPACE) ON FUTURE DESIGNS
OPTION FOR R11VR TO OVERLAP W/R12VR & R13VR TO OVERLAP W/14VR
VCC_SENSE
R11VR
VCC_VRM_SENSE
VCC_PKGSENSE
R12VR
DESIGN NOTE:
EMPTY R11VR <ENG EXP>
VSS_SENSE
R13VR
VSS_VRM_SENSE
VSS_PKGSENSE
R14VR
DESIGN NOTE:
EMPTY R13VR <ENG EXP>
EU10VR
ISL6312A
VCC_IN_CPU_VREG
R202VR
562K
402
1%
CH
CPU_VREG_OFS
BOM NOTE:
LL STUFFING (DEFAULT IS 1.23MOHM LL)
1.23MOHM LL: R202VR - 562K A93548-198 STUFFED
1.23MOHM LL: R201VR EMPTIED
1.00MOHM LL: R201VR 24.3K A93548-245 STUFFED
1.00MOHM LL: R202VR EMPTIED
R201VR
24.3K
402
1%
EMPTY
VRD_VIDSEL
VCC
OFS
VRSEL
VID7
VID6
VID5
VID4
VID3
VID2
VID1
VID0
EN
PGOOD
FS
REF
SS
DRSEL
OVPSEL
IOUT
VDIFF
FB
COMP
VSEN
RGND
GND
PVCC1_2
PVCC3
BOOT3
BOOT2
BOOT1
PHASE1
PHASE2
PHASE3
ISEN1+
ISEN1-
ISEN2+
ISEN2-
ISEN3+
ISEN3-
ISEN4+
ISEN4-
UGATE1
UGATE2
UGATE3
LGATE1
LGATE2
LGATE3
EN_PH4
PWM4
1 OF 1
REV=1
IC
CPU_VREG_PVCC3
CPU_VREG_BST3
CPU_VREG_BST2
CPU_VREG_BST1
C208VR .22UF 10% 16V X7R 603
C209VR .22UF 10% 16V X7R 603
C210VR .22UF 10% 16V X7R 603
VREG_SW3_OUT
VREG_SW2_OUT
VREG_SW1_OUT
VCC_VRM_SENSE
J1VR
1X2HDR
EMPTY
A91829-020
VRD_ENABLE
C220VR
.1UF
10%
10V
EMPTY
402
VR_READY
CAD NOTE:
PLACE ALL COMPONENTS CLOSE TO CONTROLLER
R203VR
82.5K
402
1%
CH
CPU_VREG_FS
C201VR
.012UF
10%
50V
X7R
603
CPU_VREG_REF
R204VR
100K
402
1%
CH
CPU_VREG_SS
R236VR
49.9K
402
1%
EMPTY
R205VR
CPU_VREG_DRSEL
R206VR
CPU_VREG_OVPSEL
R207VR
17.4K
402
1%
CH
CPU_VREG_IOUT
DESIGN NOTE:
VSS/VCCSENSE: 1X2
HEADER (J1VR): NEVER
STUFF SUITCASE JUMPER
BOM NOTE:
FMB STUFFING
65W: R207VR - 22.1K A93548-147
95W: R207VR - 17.4K A93548-239 (DEFAULT)
105W: R207VR - 15.4K A93548-205
VSS_VRM_SENSE
C202VR
470PF
10%
50V
X7R
603
R209VR
22.1
402
1%
CH
CPU_VREG_VDIFF_PN1
R210VR
750
402
1%
CH
R212VR
750
402
1%
CH
CPU_VREG_VDIFF
R211VR
562
402
1%
CH
RT1VR
THRMSTR
C14407-001
CPU_VREG_FB
CAD NOTE:
PLACE THERMISTOR RT1VR CLOSE TO IND1. NEEDS TO BE GROUND REFERENCED AND AWAY FROM PHASE NODE > 10MILS SO IT DOES NOT PICK UP NOISE
C203VR
22PF
5%
50V
COG
603
CPU_VREG_COMP
R213VR
17.4K
402
1%
CH
CPU_VREG_COMP_PN1
C204VR
820PF
5%
50V
COG
603
C206VR
1500PF
5%
25V
EMPTY
603
C207VR
1500PF
5%
25V
EMPTY
603
C205VR
1500PF
5%
25V
EMPTY
603
CPU_VREG_ISEN1P
R238VR
CPU_VREG_ISEN1P_R
R215VR
1K
1%
EMPTY
402
C211VR
.1UF
10%
16V
X7R
603
C212VR
.1UF
16V
X7R
603
CPU_VREG_ISEN1M
R216VR
5.11K
402
1%
CH
CPU_VREG_SENSE1
CAD NOTE:
PLACE ALL COMPONENTS CLOSE TO CONTROLLER
CPU_VREG_ISEN2P
R239VR
CPU_VREG_ISEN2P_R
R217VR
1K
1%
EMPTY
402
CPU_VREG_ISEN2M
C213VR .1UF 10% 16V X7R 603
C214VR .1UF 10% 16V X7R 603
R218VR
5.11K
402
1%
CH
CPU_VREG_SENSE2
CPU_VREG_ISEN3M
CPU_VREG_ISEN3P
R240VR
CPU_VREG_ISEN3P_R
TP_CPU_VREG_ISEN4P
TP_CPU_VREG_ISEN4M
R219VR
1K
1%
EMPTY
402
C215VR .1UF 10% 16V X7R 603
C216VR .1UF 10% 16V X7R 603
R220VR
5.11K
402
1%
CH
CPU_VREG_SENSE3
CPU_VREG_UGATE1
CPU_VREG_UGATE2
CPU_VREG_UGATE3
CPU_VREG_LGATE1
CPU_VREG_LGATE2
CPU_VREG_LGATE3
VCC_IN_CPU_VREG
TP_CPU_VREG_PWM4
C219VR 1000PF 10% 50V EMPTY 402
C218VR 1000PF 10% 50V EMPTY 402
C217VR 1000PF 10% 50V EMPTY 402
BPAGE DRAWING
frostburg_fabc.sch_1.93
Sun Mar 18 18:45:04 2007
[PAGE_TITLE=VCCP VREG]
INTEL CONFIDENTIAL
DOCUMENT_NUMBER
xxxxxx
PAGE
93
REV
3.01
CUSTOM TEXT BPAGE

CR-94 : 8 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(SCH_1):PAGE94

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_CPUVR	5.9.3	03-02-07



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Sun Mar 18 18:45:06 2007

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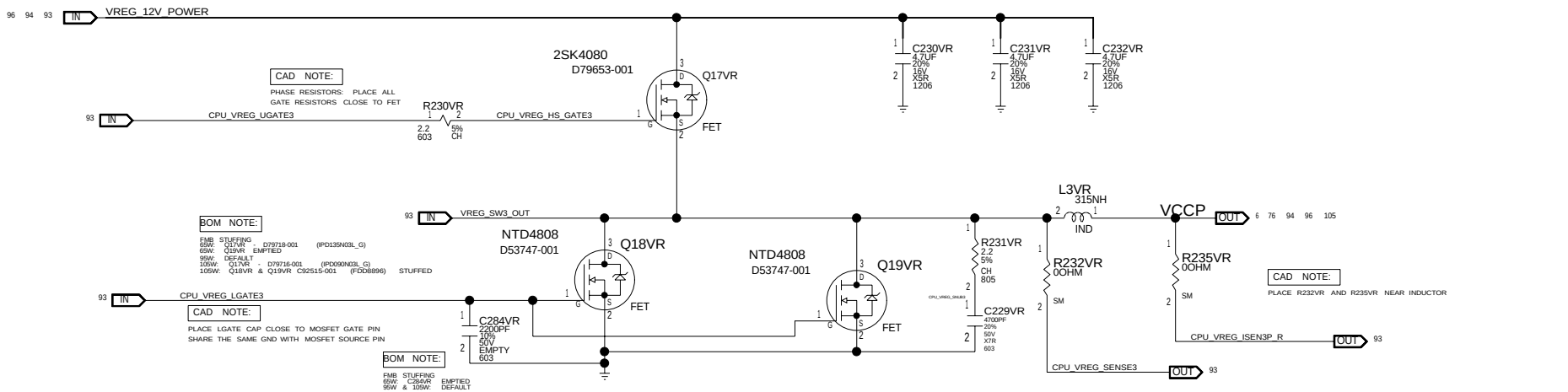
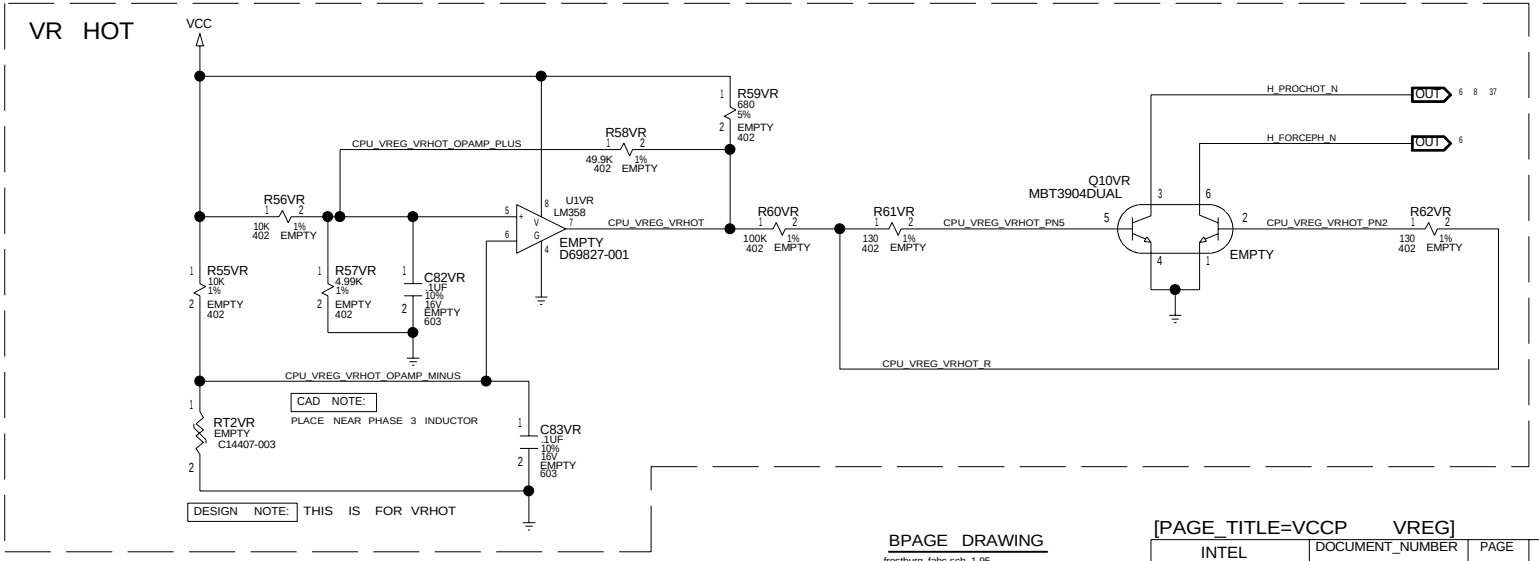
INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	94	3.01

CUSTOM TEXT 2 BPAGE

CR-95 : 8 @FROSTBURG_FABC_LIB.FROSTBURG_FABC(SCH_1):PAGE95

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_CPUVR	5.9.3	03-02-07





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frostburg_fabc.sch_1.95
Sun Mar 18 18:45:08 2007

[PAGE_TITLE=VCCP VREG]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	95	3.01

CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BL_CPUVR	5.9.3	01-12-07

CAD NOTE:
PLACE ALL (14) 1206 CAPS INSIDE CPU SOCKET CAVITY

105 96 95 94 76 6 IN VCCP

C233VR 22UF 20% 6.3V X5R 1206
C234VR 22UF 20% 6.3V X5R 1206
C235VR 22UF 20% 6.3V X5R 1206
C236VR 22UF 20% 6.3V X5R 1206
C237VR 22UF 20% 6.3V X5R 1206
C238VR 22UF 20% 6.3V X5R 1206
C239VR 22UF 20% 6.3V EMPTY X5R 1206
C240VR 22UF 20% 6.3V EMPTY 1206
C241VR 22UF 20% 6.3V X5R 1206
C242VR 22UF 20% 6.3V EMPTY 1206
C243VR 22UF 20% 6.3V EMPTY 1206
C244VR 22UF 20% 6.3V X5R 1206
C281VR 100UF 20% 2V ALUM 7343
C247VR 22UF 20% 6.3V X5R 1206
C250VR 22UF 20% 6.3V EMPTY 1206

BOM NOTE:
FMB STUFFING
65W & 95W: DEFAULT
105W: STUFF C250VR

CAD NOTE:
PLACE ON TOP NORTH/NORTHEAST SIDE OF SOCKET

105 96 95 94 76 6 IN VCCP

C263VR 150UF 20% 2V EMPTY 7343
C264VR 560UF 20% 2.5V EMPTY RDL
C265VR 560UF 20% 2.5V EMPTY RDL
C266VR 560UF 20% 2.5V ALUM RDL
C267VR 560UF 20% 2.5V ALUM RDL

BOM NOTE:
NIPPON (PCS 2.5VB 560QH08)
628955-074

CAD NOTE:
PLACE ON EAST/SOUTHEAST SIDE OF SOCKET

C268VR 560UF 20% 2.5V ALUM RDL
C269VR 560UF 20% 2.5V ALUM RDL
C270VR 560UF 20% 2.5V EMPTY RDL
C271VR 560UF 20% 2.5V EMPTY RDL

BOM NOTE:
FMB STUFFING
65W : EMPTY C269VR
95W & 105W: DEFAULT

95 94 93 IN VREG 12V POWER

J2VR 2X2HDR
CONN A91848-001

C276VR .1UF 10% 16V EMPTY 402
C277VR .1UF 10% 16V EMPTY 402

BOM NOTE:
RUBICON (16MHZ680M INL)
A46887-048

C273VR 680UF 20% 16V ALUM RDL
C274VR 680UF 20% 16V ALUM RDL
C275VR 680UF 20% 16V EMPTY RDL

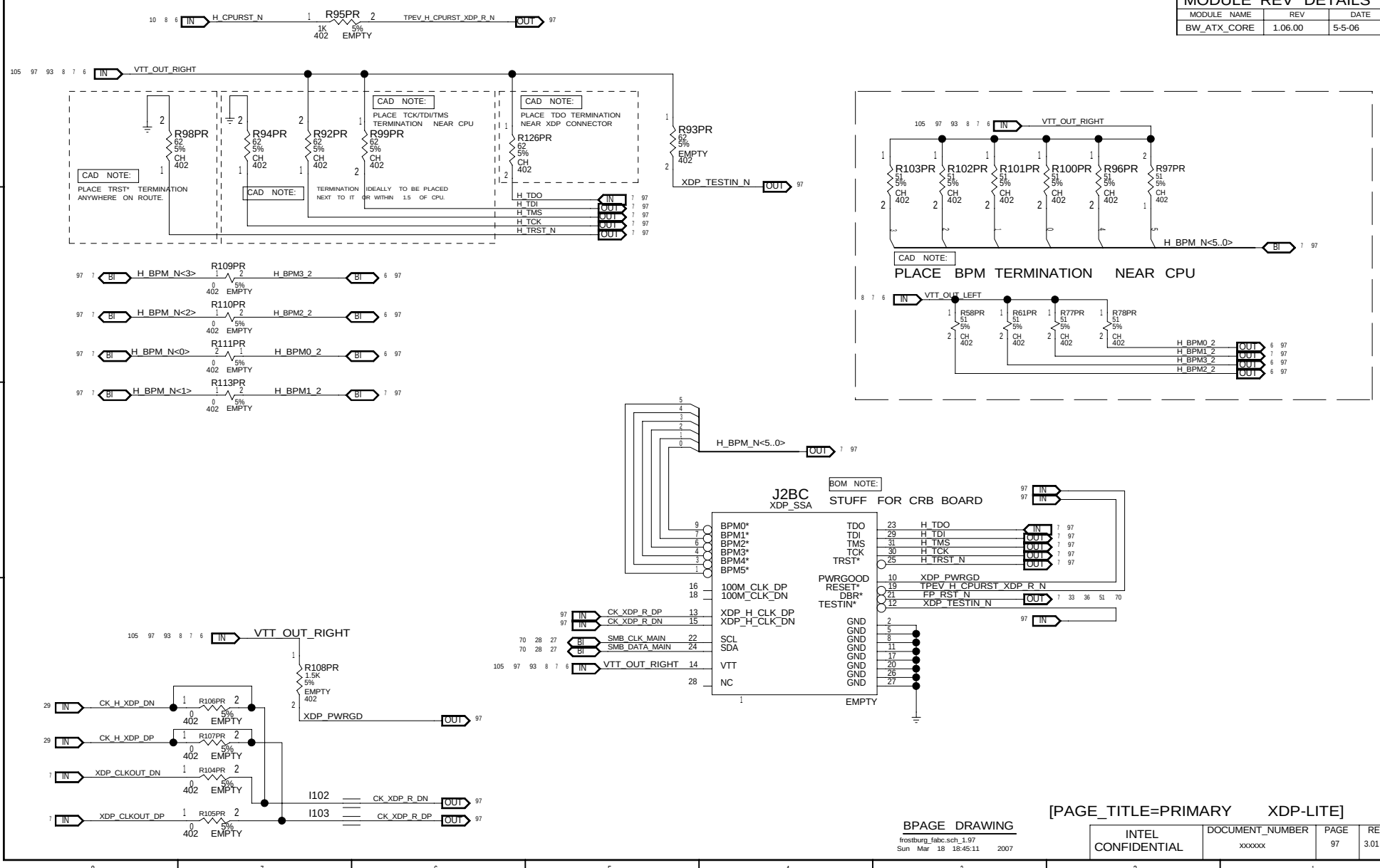
[PAGE_TITLE=VREG: VCCP DECOUPLING / 2X2 CONN]

BPAGE DRAWING
frostburg_fabc.sch_1.96
Sun Mar 18 18:45:09 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	96	3.01

CUSTOM TEXT 2 BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BW_ATX_CORE	1.06.00	5-5-06



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frostburg_fabc.sch_1.97
Sun Mar 18 18:45:11 2007

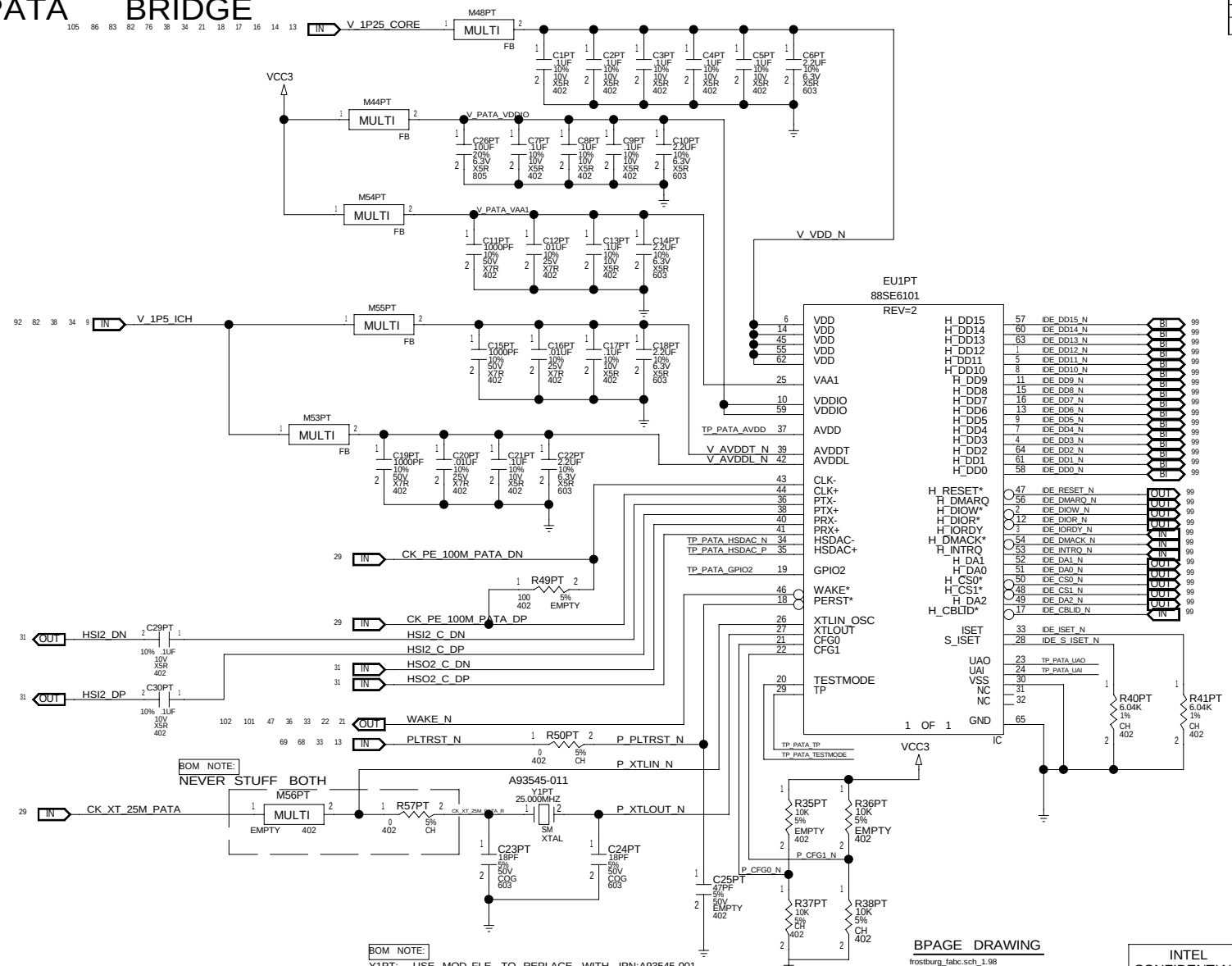
[PAGE_TITLE=PRIMARY XDP-LITE]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	97	3.01

CUSTOM TEXT 2 BPAGE

PCIE/PATA BRIDGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE
PCIE_PATA	1.2.7	39.2.06



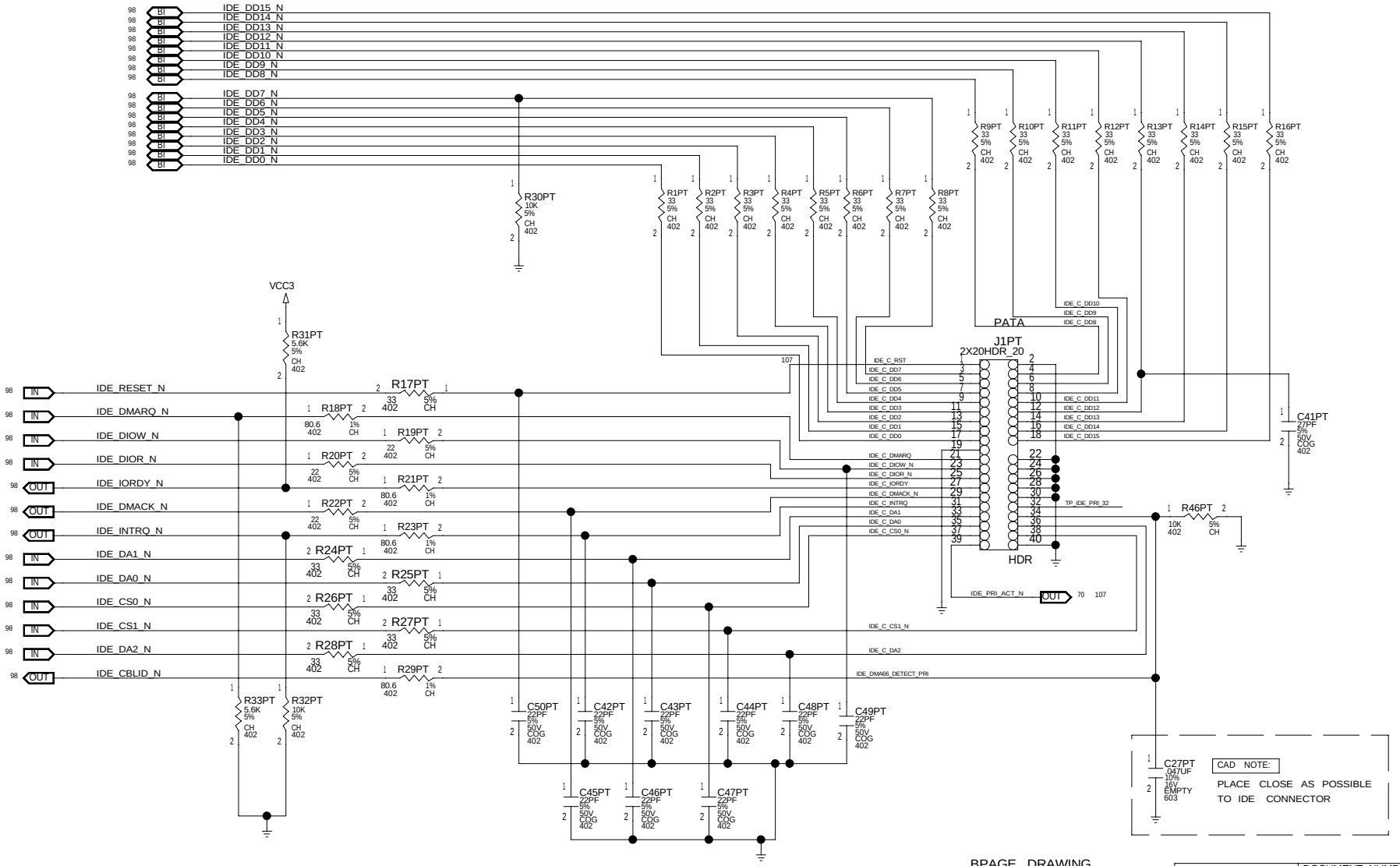
BPAGE DRAWING

frostburg_fabc.sch_1.98
Sun Mar 18 18:45:13 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	98	3.01

PATA CONNECTOR

MODULE REV DETAILS		
MODULE NAME	REV	DATE
PCIE_PATA	1.2.7	39.2.06



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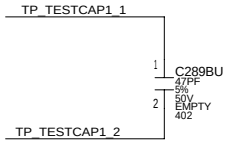
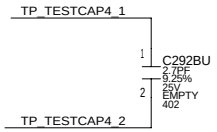
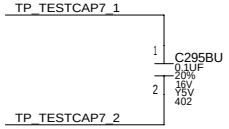
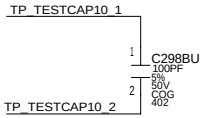
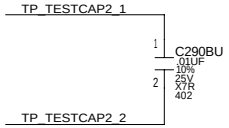
MODULE_REV_DETAILS		
MODULE_NAME	REV	DATE

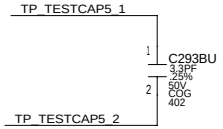


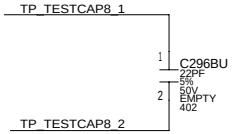


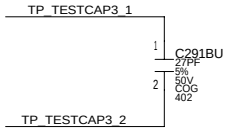


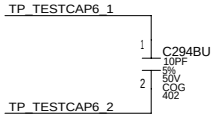


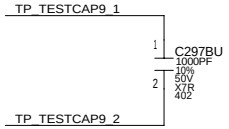








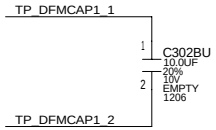


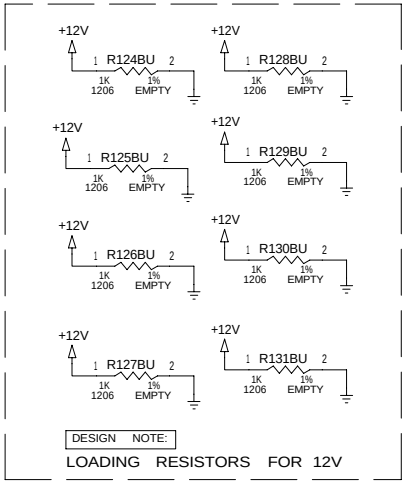


DESIGN NOTE:

FOR DFM

CORNER PROTECTION





DESIGN NOTE:

LOADING RESISTORS FOR 12V

BPAGE DRAWING

frostburg_fabc.sch_1.100

Sun Mar 18 18:45:16 2007

[PAGE_TITLE=TEST SITE CAPS]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	100	3.01

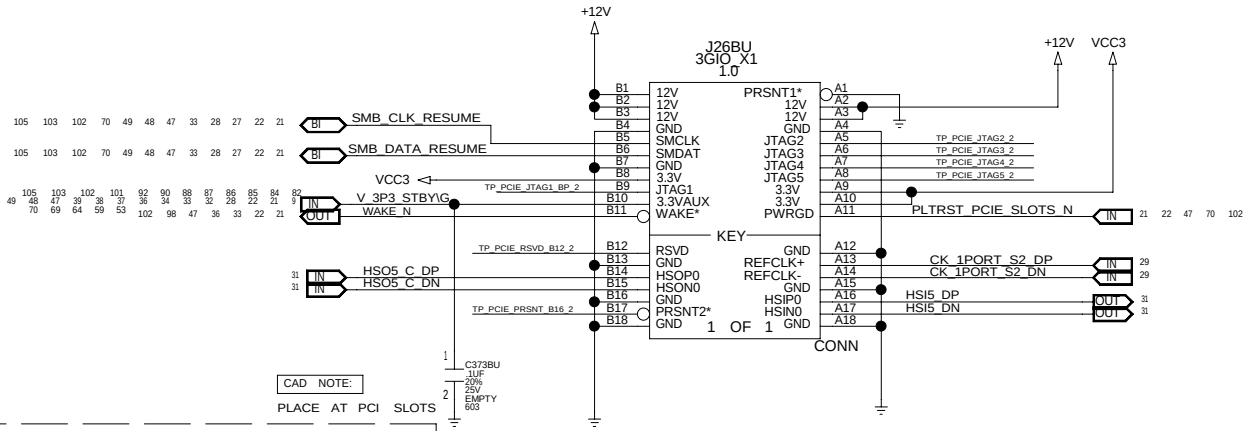
MODULE REV DETAILS		
MODULE NAME	REV	DATE

EXPANSION SLOT 5

CAD NOTE:

PCI-E X1 SLOT 2

PCI EXPRESS
1-PORT

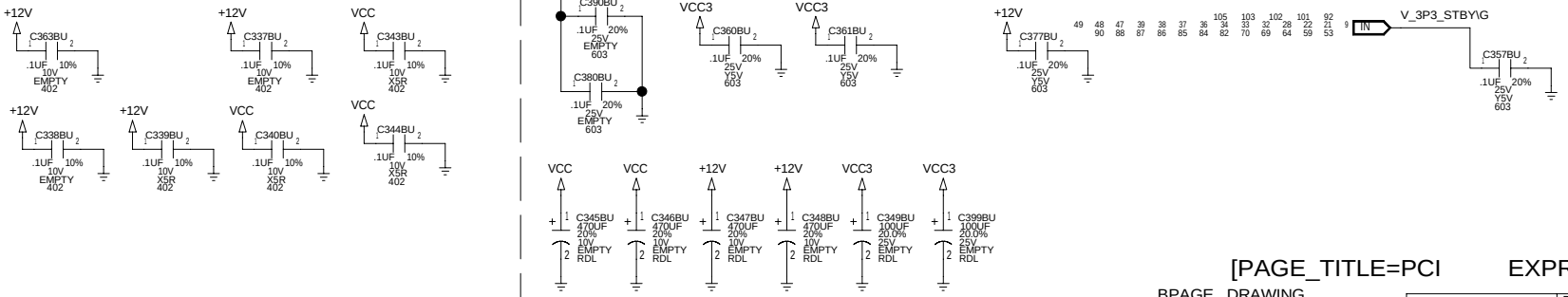


CAD NOTE:

PLACE AT PCI SLOTS

CAD NOTE:

STICHING CAPS FOR TRACE OF PCIE SLOT 2 AND 3



[PAGE_TITLE=PCI EXPRESS X1 #2]

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frostburg_fabc.sch_1.101
Sun Mar 18 18:45:18 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	101	3.01

CUSTOM TEXT 2 BPAGE

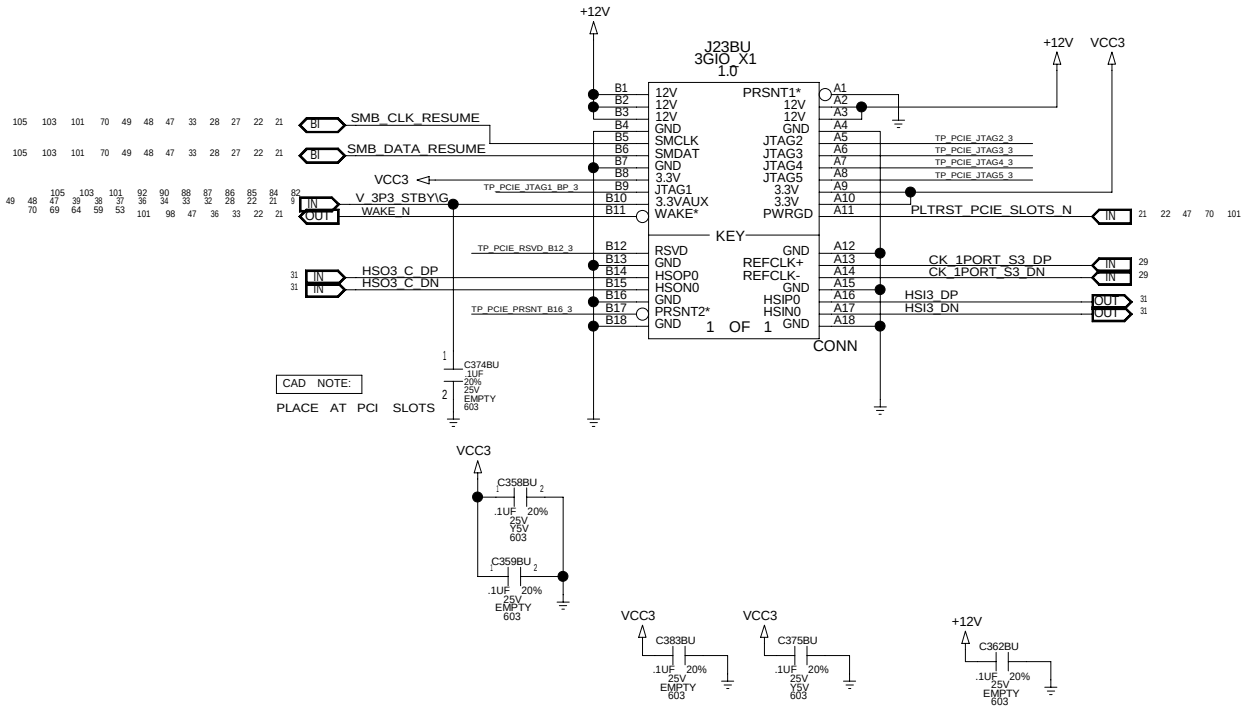
MODULE REV DETAILS		
MODULE NAME	REV	DATE

EXPANSION SLOT 6

CAD NOTE:

PCI-E X1 SLOT 3

PCI EXPRESS
1-PORT



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frostburg_fabc.sch_1.102
Sun Mar 18 18:45:19 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	102	3.01

CUSTOM TEXT 2 BPAGE

EXPANSION SLOT 7 (FURTHEST FROM CPU)

MODULE REV DETAILS		
MODULE NAME	REV	DATE

CAD NOTE:
STICHING CAP ACROSS VCC AND VCC3

PCI SLOT 3

J24BU
PCI CONN2_2 CONN

NOTE: PCI SLOTS= VCC3 SHOULD GET 470UF DECOUPLING,
VCC SHOULD GET 100UF (ALLOWS 1000UF OPTION FOR VCC3)

DESIGN NOTE:
PCI2.2 COMPATIBLE

DESIGN NOTE:
IRQ MAP
IRQ MAP A B C D
C D B A
IDSEL 18
REQ/GNT 2

[PAGE_TITLE=PCI CONN 3]

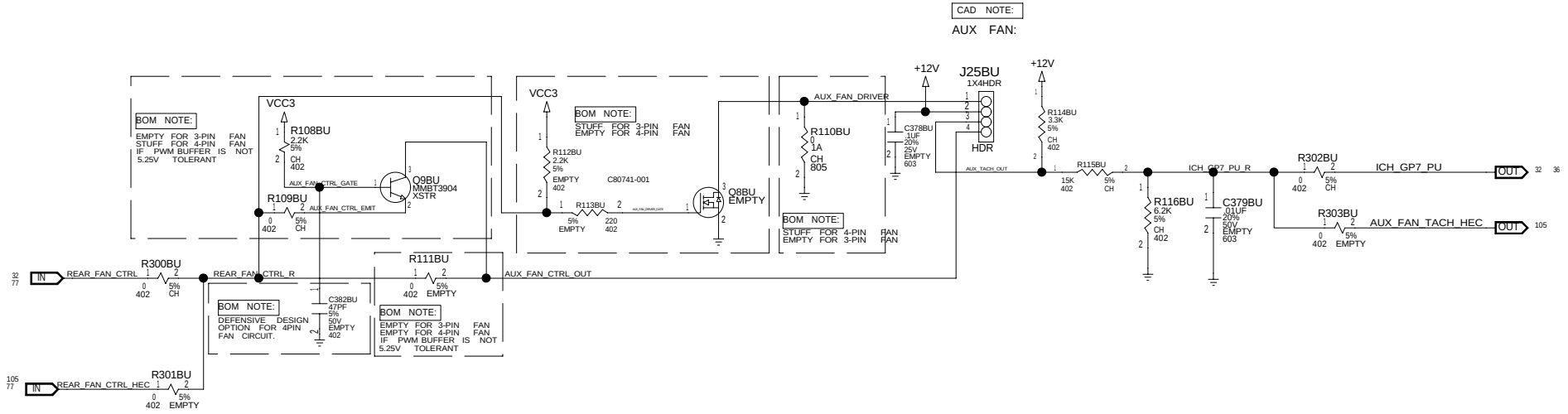
BPAGE DRAWING
frostburg_fabc.sch_1.103
Sun Mar 18 18:45:21 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxx	103	3.01

CUSTOM TEXT 2 BPAGE

AUX FAN CONFIGURATION

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=AUX FAN CONFIGURATION]

BPAGE DRAWING

frostburg_fabc.sch_1.104
Sun Mar 18 18:45:24 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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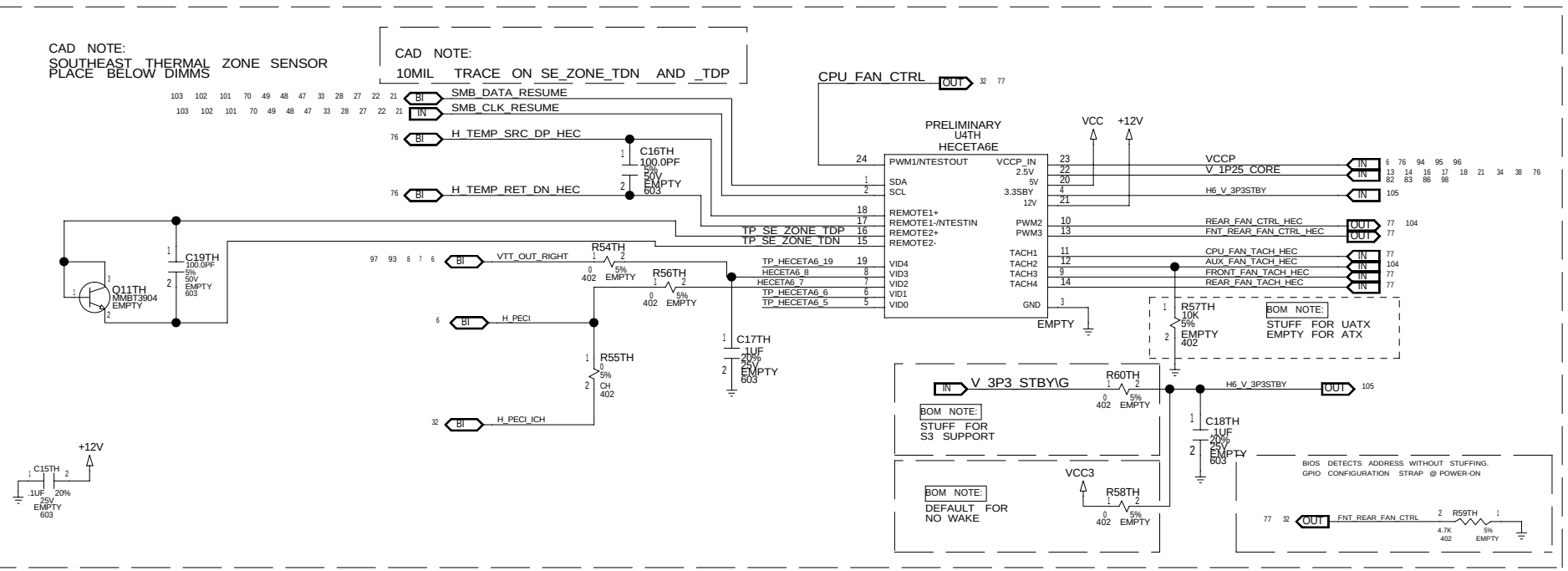
CUSTOM TEXT BPAGE



DRAWING [PAGE_TITLE=HARDWARE MANAGEMENT: HECETA]

SORRENTO SANDUSKY FAB C.SCH_1.68
Sun Mar 18 18:45:26 2007

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
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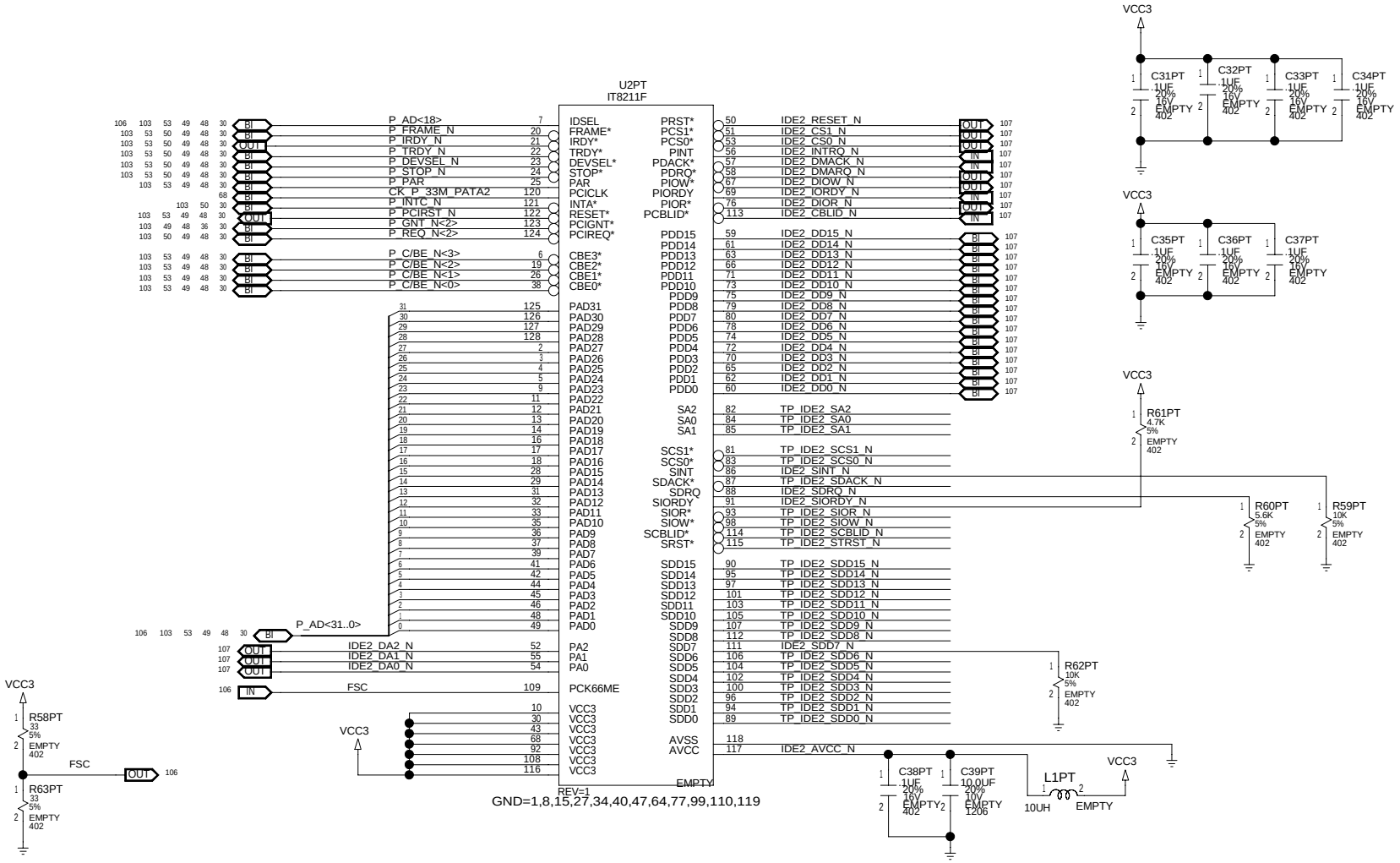

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Sun Mar 18 18:45:27 2007

[PAGE_TITLE=ITE IT8211F 1 OF 2]

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PATA 2ND CONNECTOR

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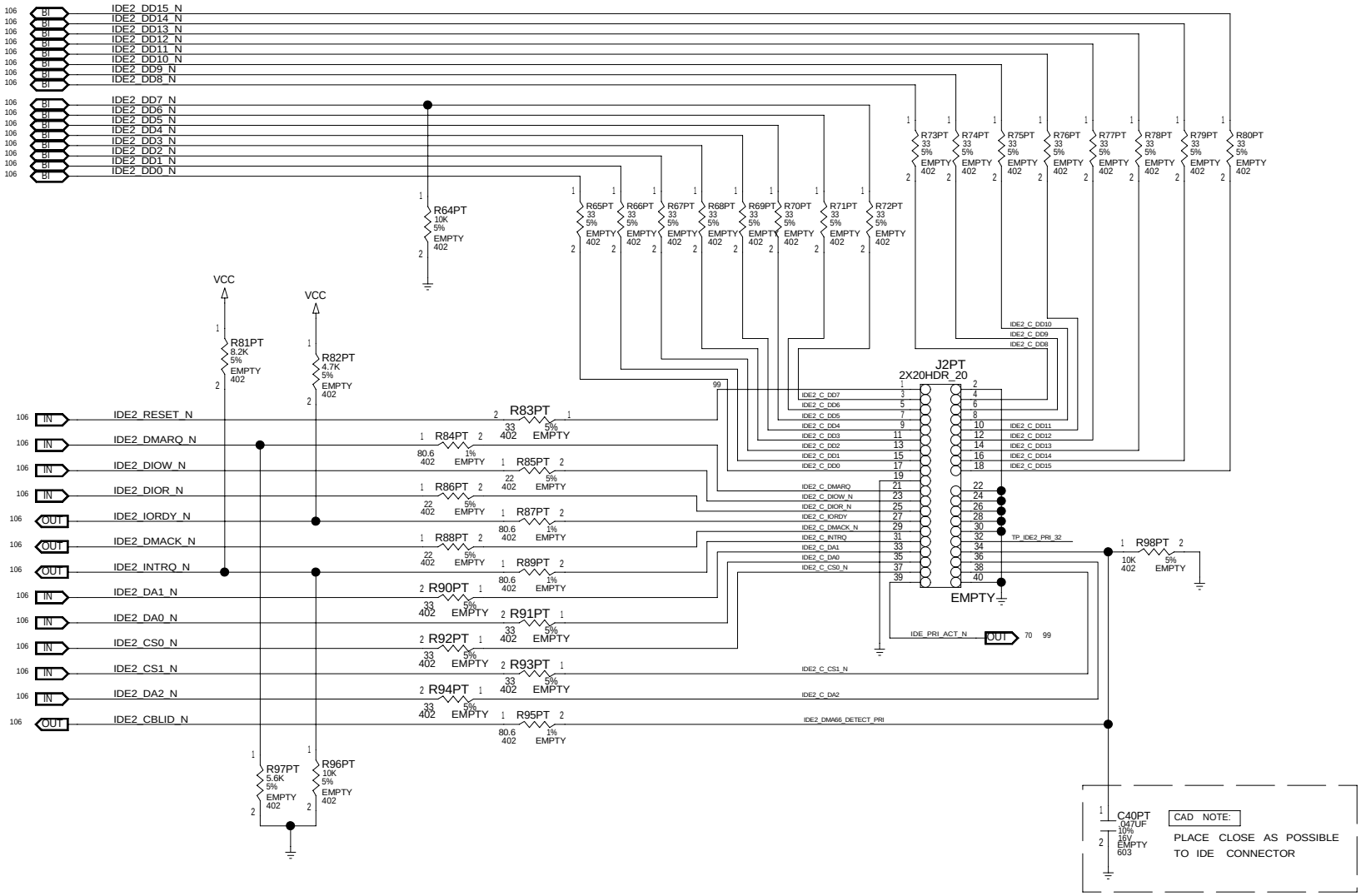

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frostburg_fabc.sch_1.107
Sun Mar 18 18:45:29 2007

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
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CUSTOM TEXT BPAGE