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Title: **Index Page**

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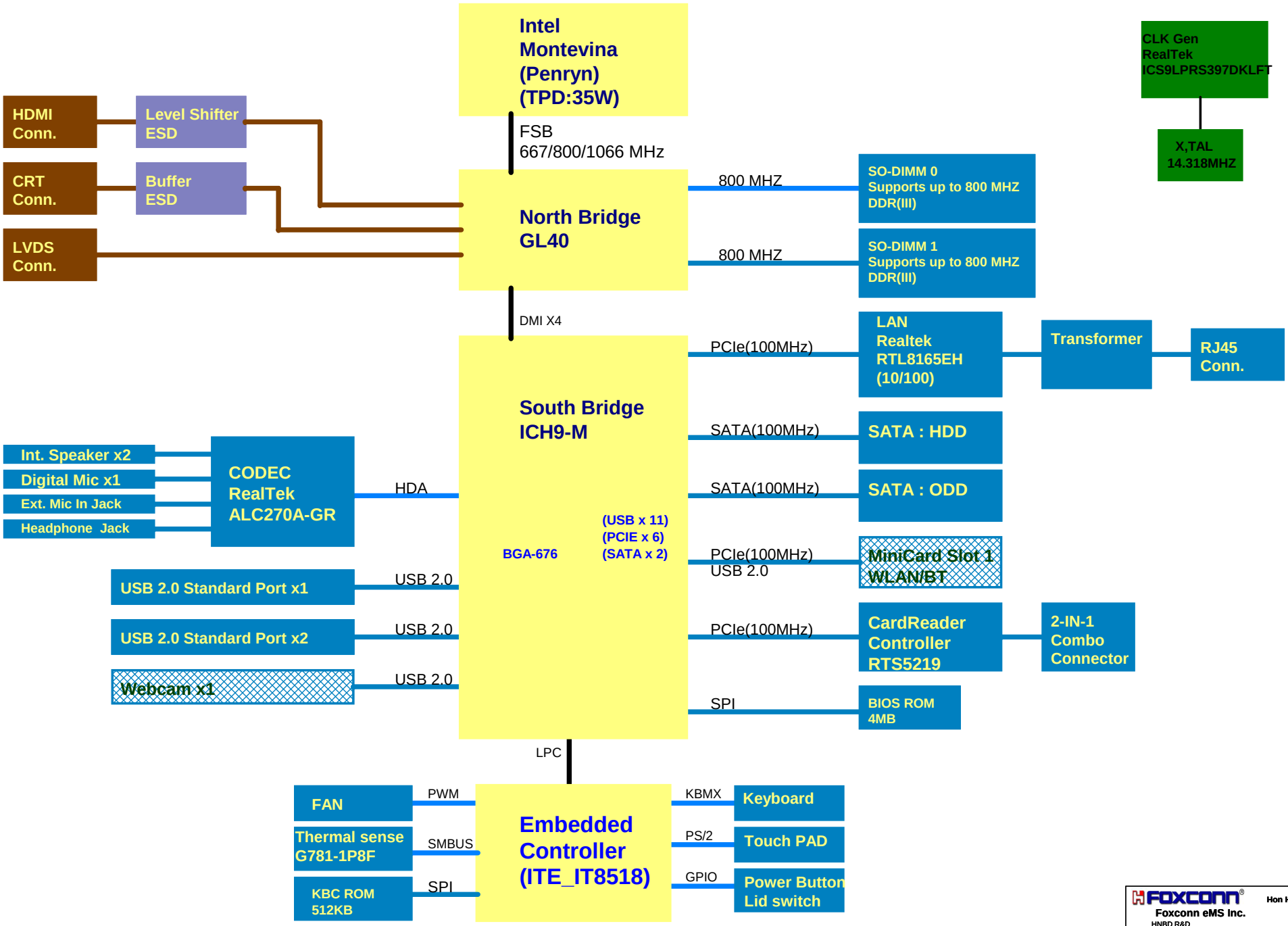

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Title: SYSTEM BLOCK DIAGRAM

Size | Document Number | Rev
Custom TPN-F101/TPN-F102 Montevina platform | 0.1

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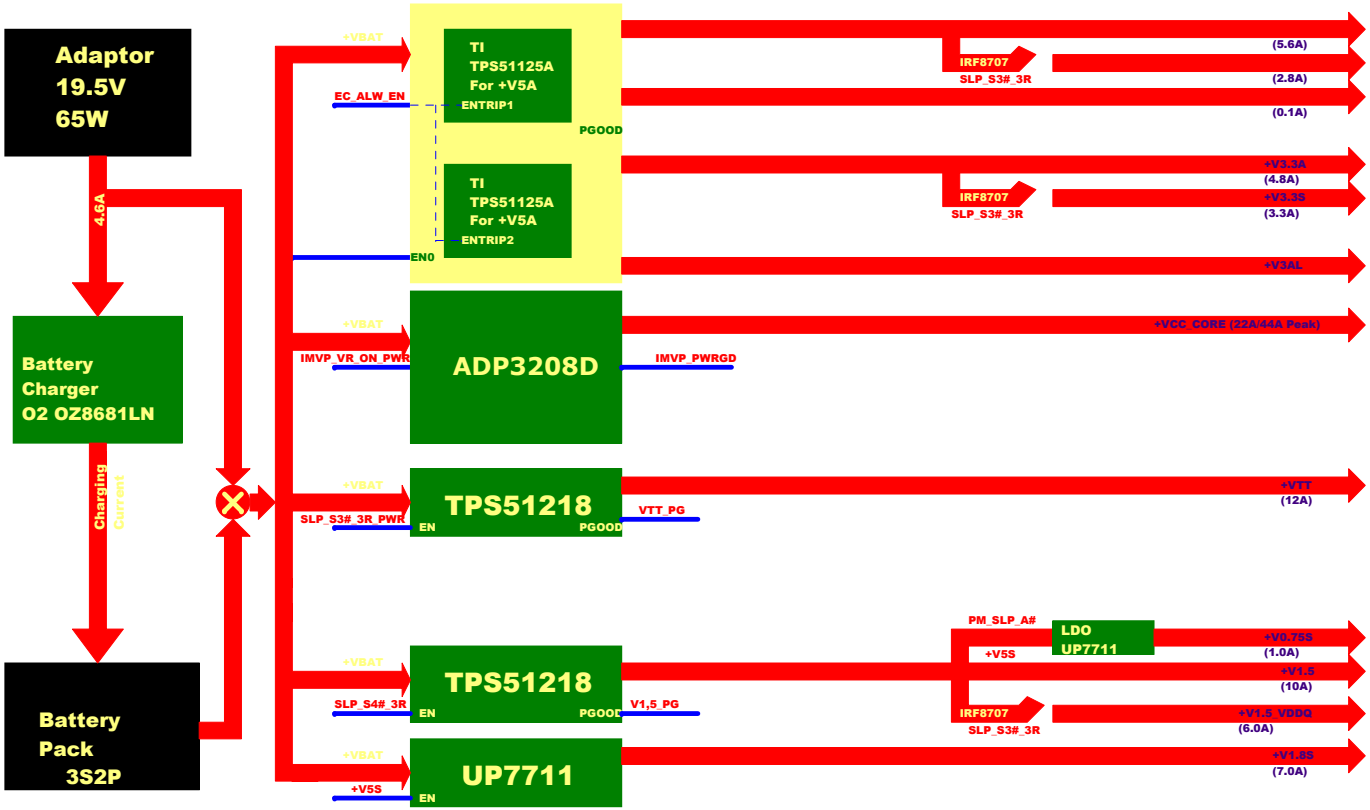
POWER MAP



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Title: History

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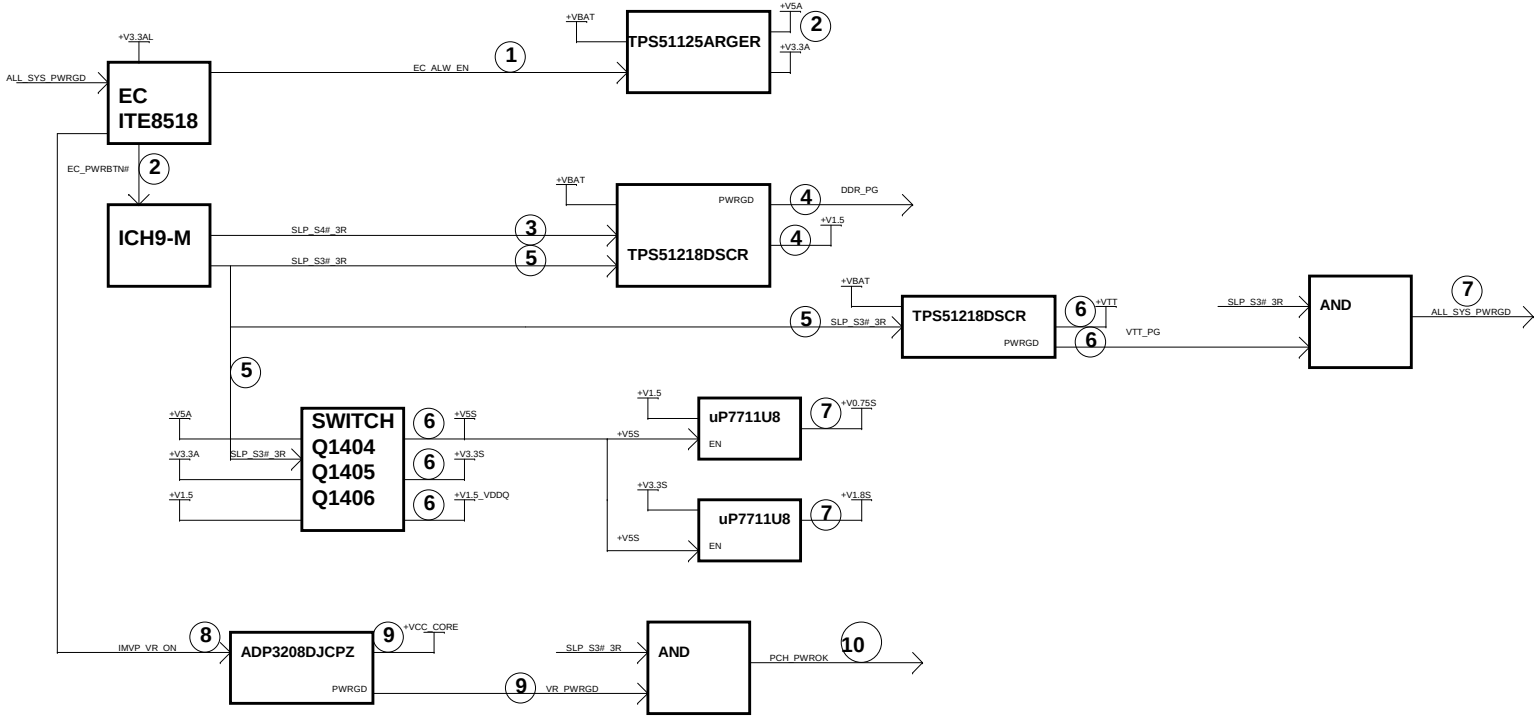

Power on Sequence required:

GL40:
1, +V3.3A ramp before +V1.1A
2, +V3.3S ramp before +V1.8S
3, +V1.8S ramp before +V1.1S
4, +V3.3S ramp before +V1.1S

ICH9-M:
1, 0 <(+V3.3S) - (+V1.8S) < 2.1
2, +V1.8S ramp before +V1.1S
3. +V1.1S ramp before VCC_NB

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Title: **POWER SEQUENCY DIAGRAM**

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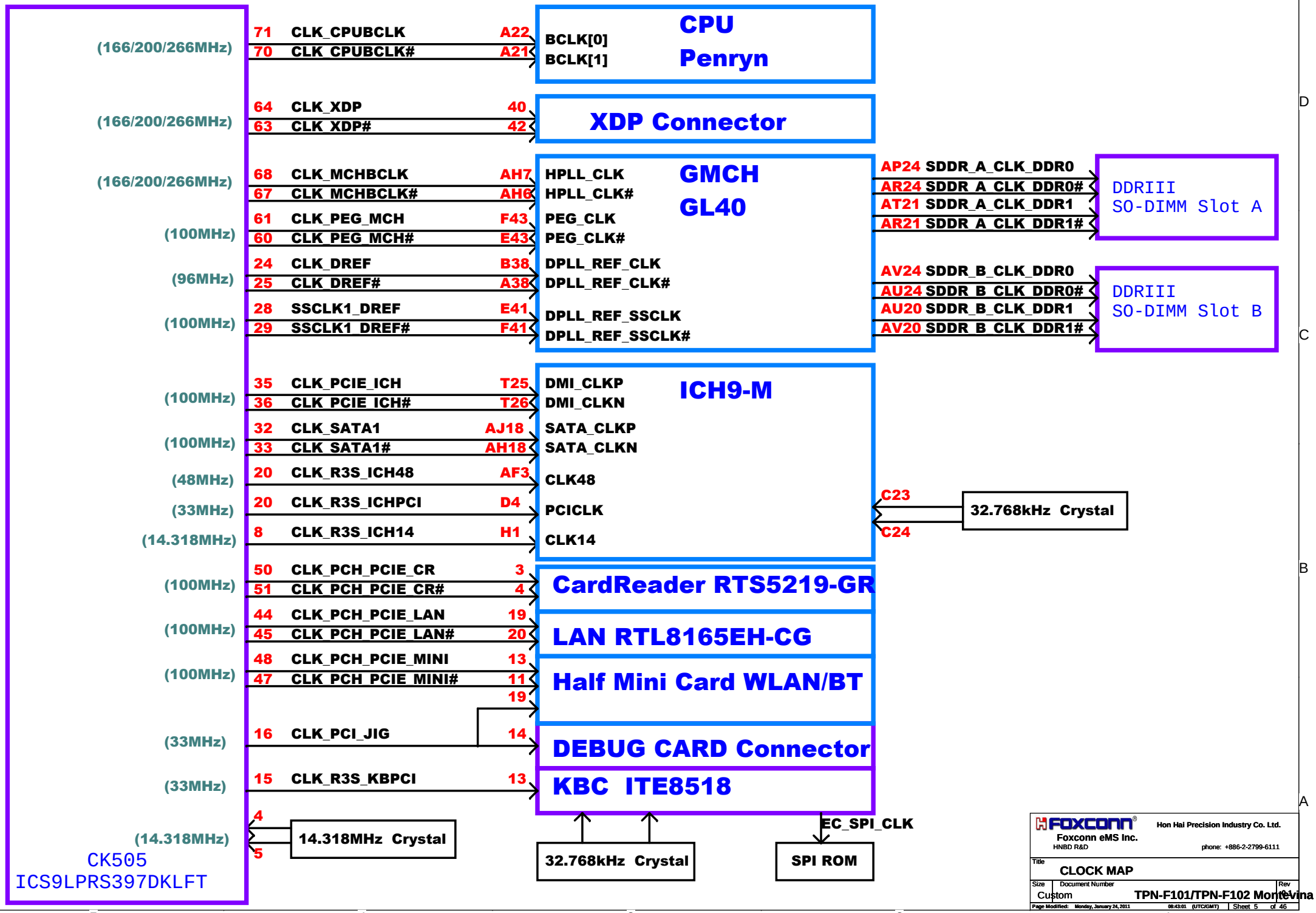
CK505
ICS9LPRS397DKLFT
(166/200/266MHz)
71 CLK_CPUBCLK
70 CLK_CPUBCLK#
A22
A21
BCLK[0]
BCLK[1]
CPU
Penryn
(166/200/266MHz)
64 CLK_XDP
63 CLK_XDP#
40
42
XDP Connector
(166/200/266MHz)
68 CLK_MCHBCLK
67 CLK_MCHBCLK#
AH7
AH6
HPLL_CLK
HPLL_CLK#
(100MHz)
61 CLK_PEG_MCH
60 CLK_PEG_MCH#
F43
E43
PEG_CLK
PEG_CLK#
(96MHz)
24 CLK_DREF
25 CLK_DREF#
B38
A38
DPLL_REF_CLK
DPLL_REF_CLK#
(100MHz)
28 SSCLK1_DREF
29 SSCLK1_DREF#
E41
F41
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
GMCH
GL40
AP24 SDDR_A_CLK_DDR0
AR24 SDDR_A_CLK_DDR0#
AT21 SDDR_A_CLK_DDR1
AR21 SDDR_A_CLK_DDR1#
DDRIII
SO-DIMM Slot A
AV24 SDDR_B_CLK_DDR0
AU24 SDDR_B_CLK_DDR0#
AU20 SDDR_B_CLK_DDR1
AV20 SDDR_B_CLK_DDR1#
DDRIII
SO-DIMM Slot B
(100MHz)
35 CLK_PCIE_ICH
36 CLK_PCIE_ICH#
T25
T26
DMI_CLKP
DMI_CLKN
(100MHz)
32 CLK_SATA1
33 CLK_SATA1#
AJ18
AH18
SATA_CLKP
SATA_CLKN
(48MHz)
20 CLK_R3S_ICH48
AF3
CLK48
(33MHz)
20 CLK_R3S_ICHPCI
D4
PCICLK
(14.318MHz)
8 CLK_R3S_ICH14
H1
CLK14
ICH9-M
C23
C24
32.768kHz Crystal
(100MHz)
50 CLK_PCH_PCIE_CR
51 CLK_PCH_PCIE_CR#
3
4
CardReader RTS5219-GR
(100MHz)
44 CLK_PCH_PCIE_LAN
45 CLK_PCH_PCIE_LAN#
19
20
LAN RTL8165EH-CG
(100MHz)
48 CLK_PCH_PCIE_MINI
47 CLK_PCH_PCIE_MINI#
13
11
Half Mini Card WLAN/BT
19
(33MHz)
16 CLK_PCI_JIG
14
DEBUG CARD Connector
(33MHz)
15 CLK_R3S_KBPCI
13
KBC ITE8518
(14.318MHz)
4
5
14.318MHz Crystal
32.768kHz Crystal
EC_SPI_CLK
SPI ROM
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CLOCK MAP
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Custom
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Rev
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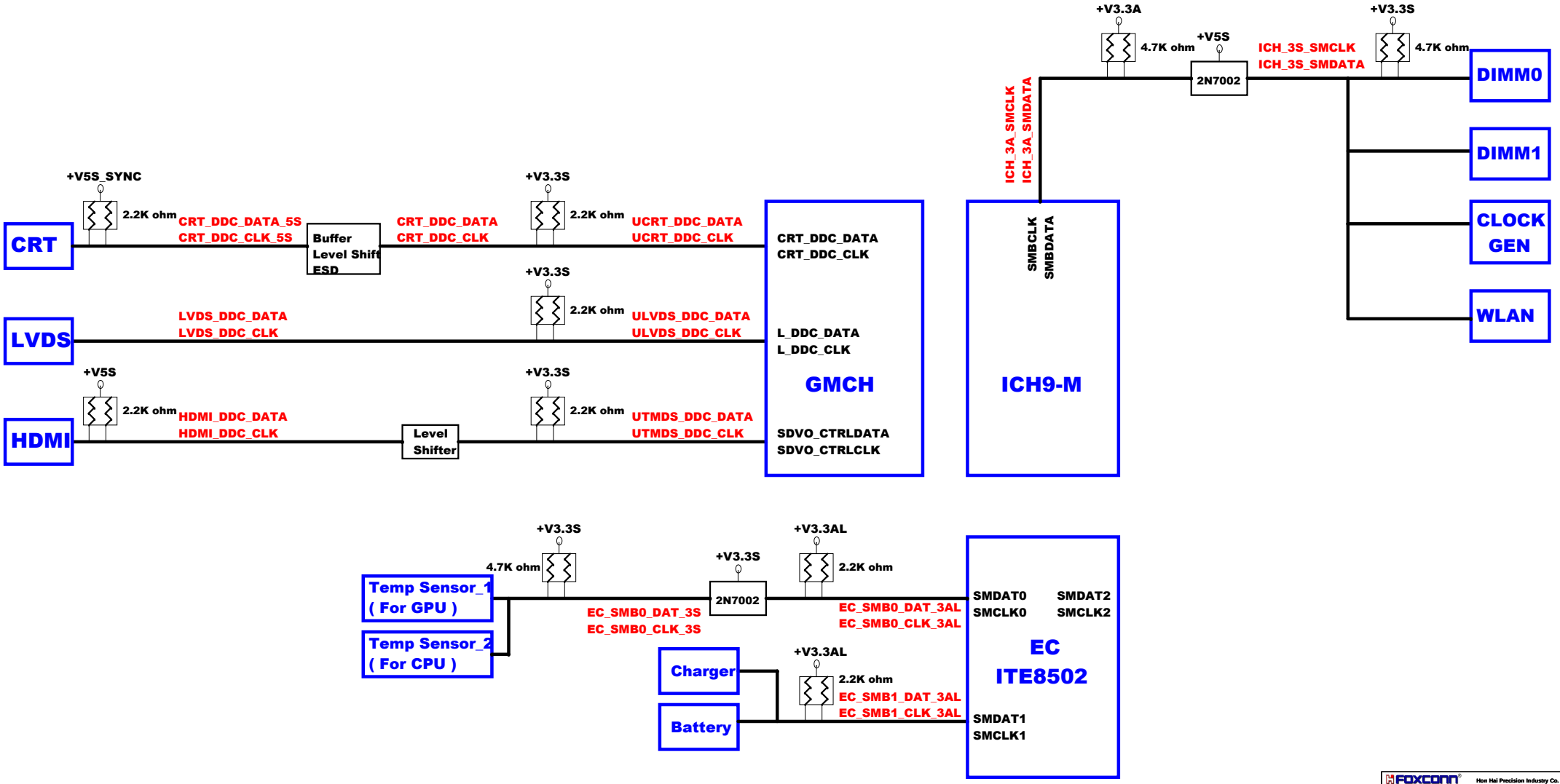

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Title: SMBUS&I2C MAP

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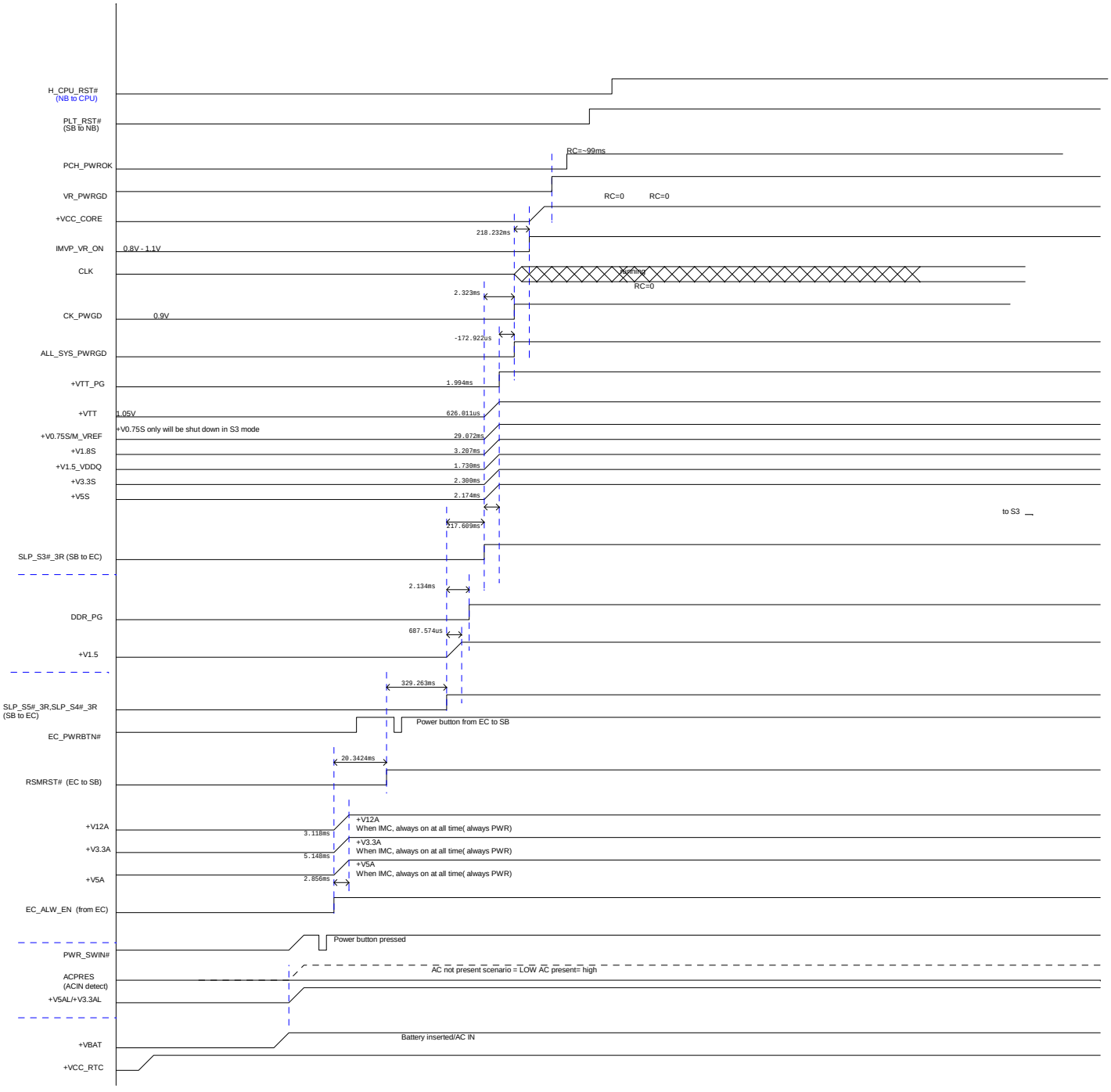

Power on Sequence required:

ICH9M:
1, +V3.3A ramp before +V1.1A
2, +V3.3S ramp before +V1.8S
3, +V1.8S ramp before +V1.1S
5, +V3.3A ramping down time > 300us
6, 50uS <= All power rails except +V3.3A <= 40mS
7, 100uS <= +V3.3A <= 40mS

GMCH:
1, 0 <(+V3.3S) - (+V1.8S) < 2.1
2, +V1.8S ramp before +V1.1S
3. +V1.1S ramp before +VCC_NB

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Title: POWER SEQUENCE

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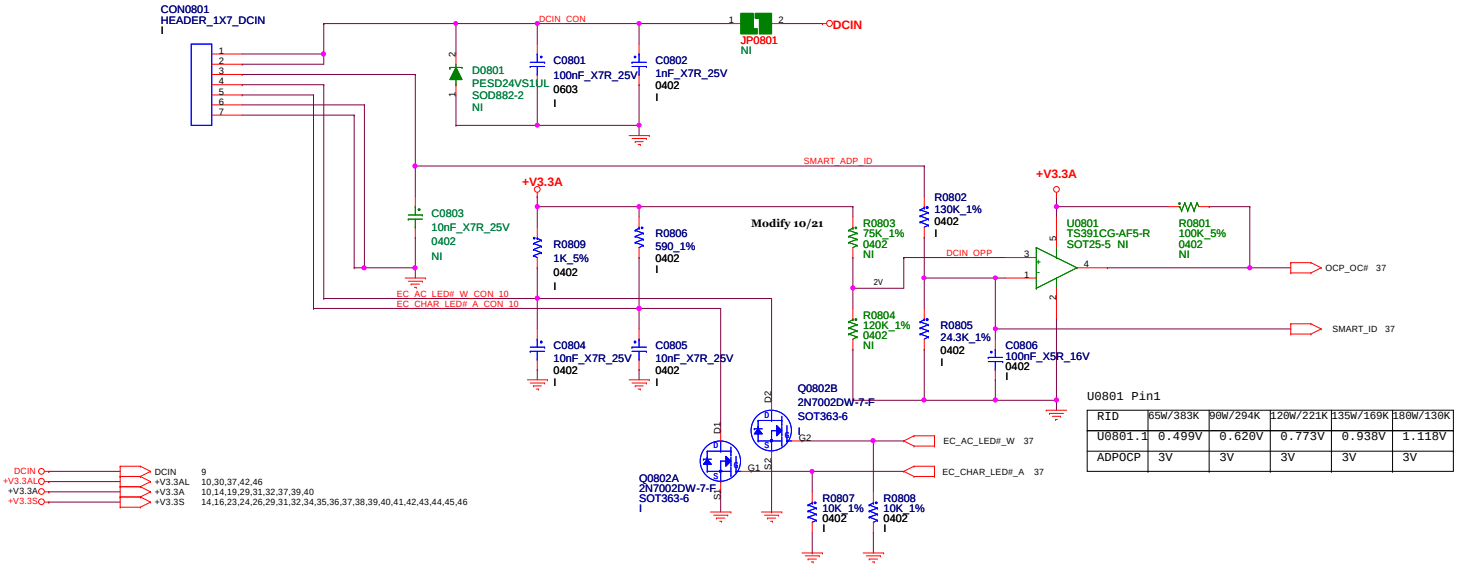
DC_JACK WIRE to BOARD CONNECTOR

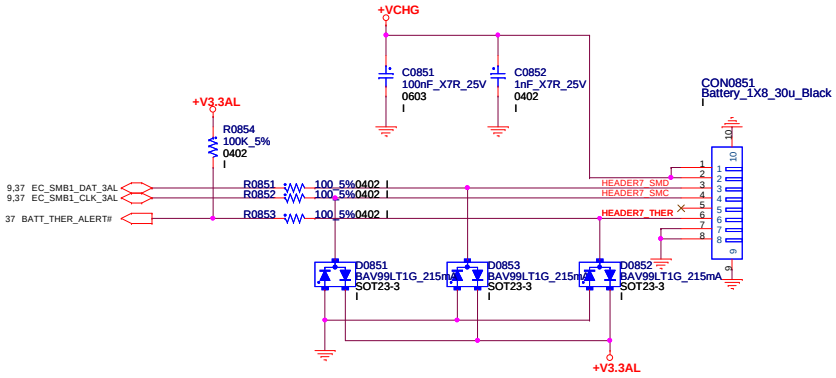


U0801 Pin1

RID	65W/383K	90W/294K	120W/221K	135W/169K	180W/130K
U0801.1	0.499V	0.620V	0.773V	0.938V	1.118V
ADPOCP	3V	3V	3V	3V	3V

BATTERY CONNECTOR

2010.0914.0



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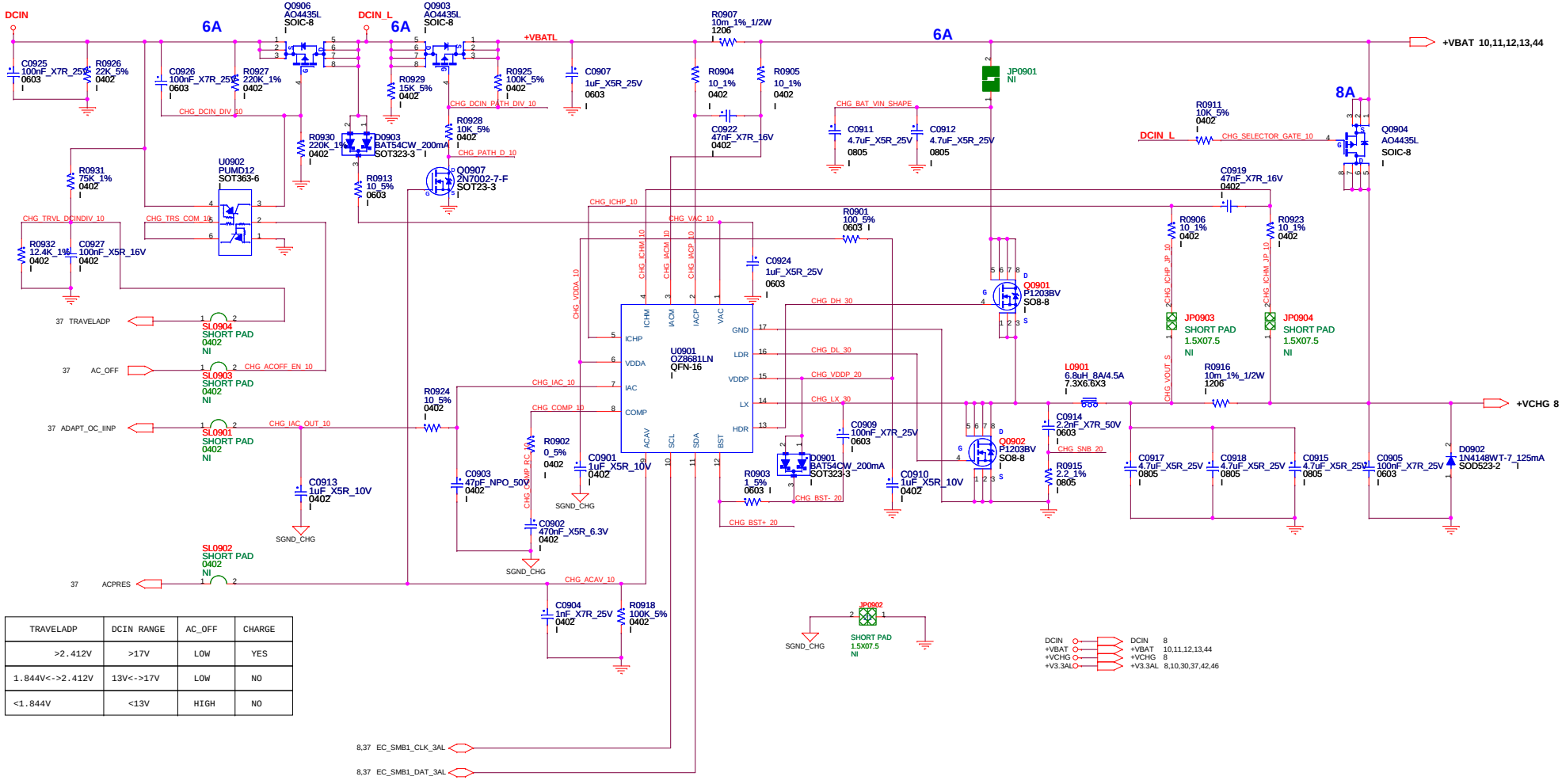
BATTERY CHARGER



TRAVELADP	DCIN RANGE	AC_OFF	CHARGE
>2.412V	>17V	LOW	YES
1.844V<->2.412V	13V<->17V	LOW	NO
<1.844V	<13V	HIGH	NO

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Title: PWR_Charger

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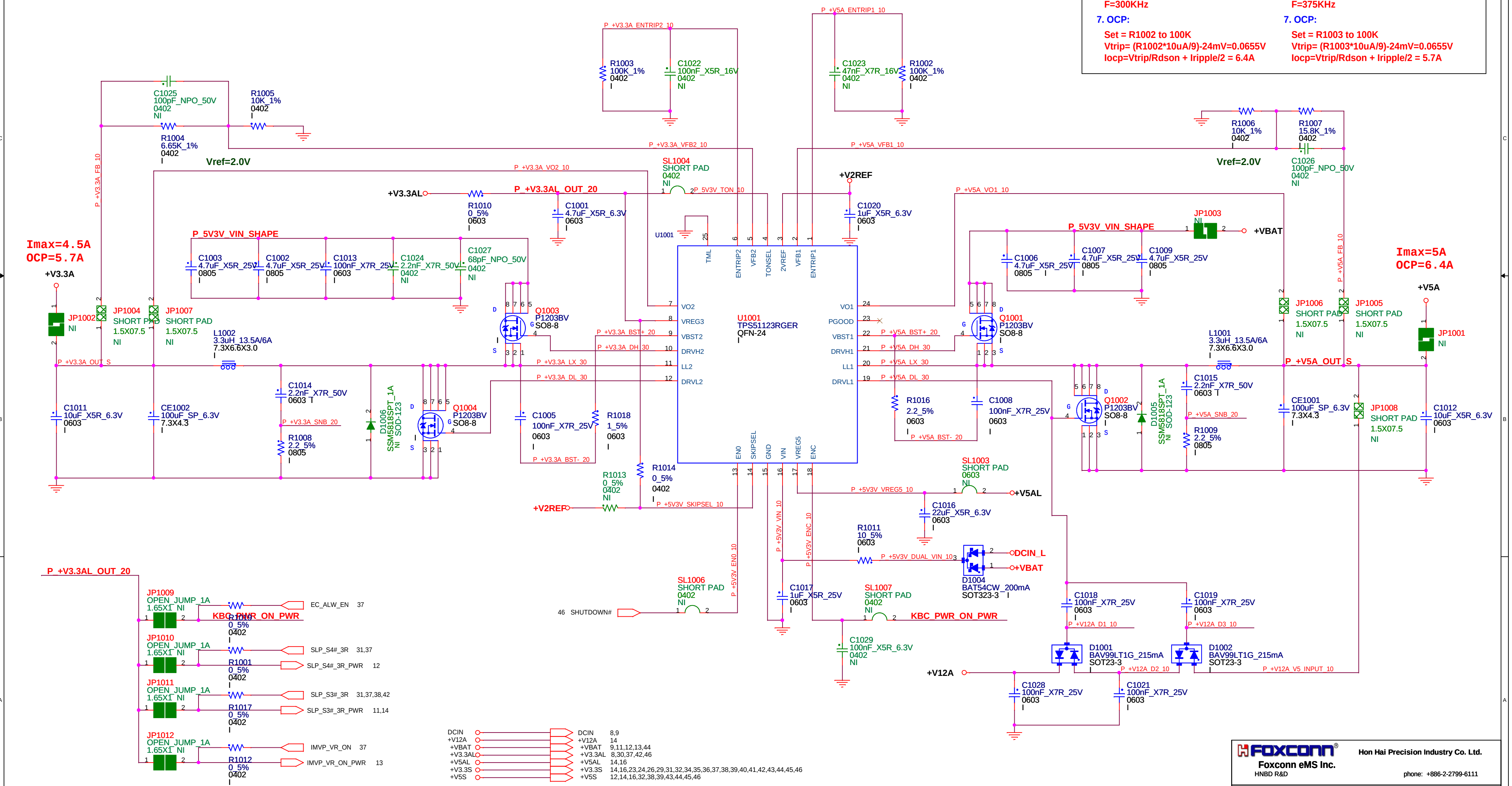
+V5A / +V3.3A POWER SUPPLY

2010.1103.0

+V5A:	+V3.3A:
1. I/P Current:	1.I/P Current:
Iin=Vo*Io/(0.75*Vin)=3.7A	Iin=Vo*Io/(0.75*Vin)=2.2A
2. Ripple Current:	2.Ripple Current:
Irip=3.72A	Irip=2.21A
3. Ripple Voltage:	3.Ripple Voltage:
ESR/1=15mohm Vrip=55.8mV	ESR/1=15mohm Vrip=33.15mV
4. Inductor Spec:	4.Inductor Spec:
Isat=13.5A Idc=6A DCR=30mohm	Isat=13.5A Idc=6A DCR=30mohm
5.MOSFET Spec:	
H-side MOSFET: IRF8707PBF Rds(ON)=17.5mohm (Vgs=4.5 V) I cont = 11A (T =25 ℃) I peak = 88A (Pause =10 us)	L-side MOSFET: IRF8707PBF Rds(ON)=17.5mohm (Vgs=4.5 V) I cont = 11A (T =25 ℃) I peak = 88A (Pause =10 us)
6. Frequency:	6. Frequency:
F=300KHz	F=375KHz
7. OCP:	7. OCP:
Set = R1002 to 100K Vtrip= (R1002*10uA/9)-24mV=0.0655V Iocp=Vtrip/Rdson + Iripple/2 = 6.4A	Set = R1003 to 100K Vtrip= (R1003*10uA/9)-24mV=0.0655V Iocp=Vtrip/Rdson + Iripple/2 = 5.7A



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Title	5V/3.3V	
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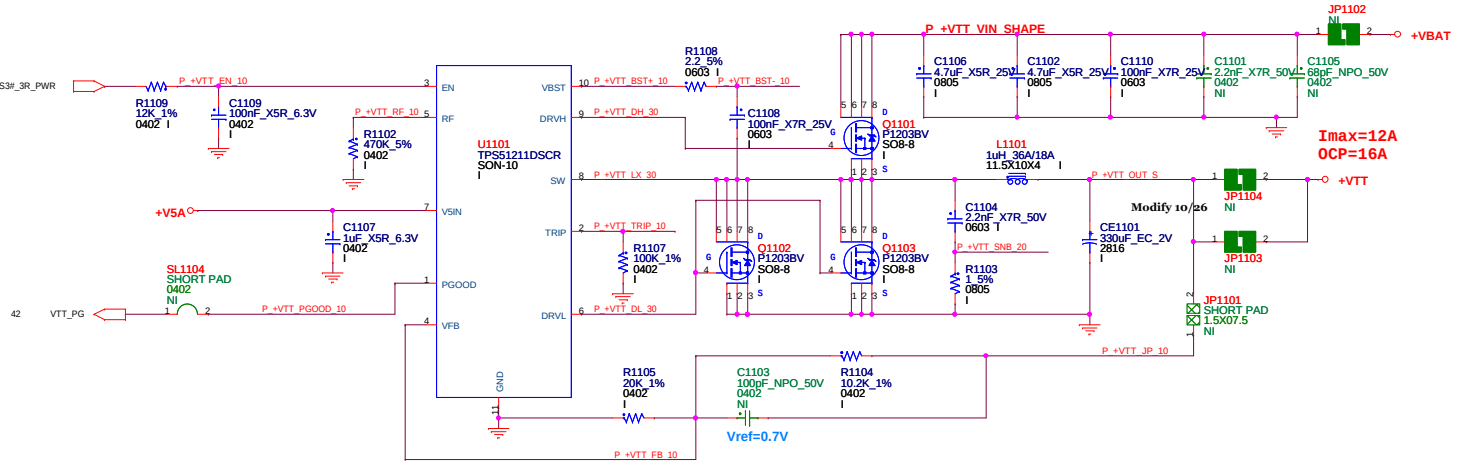
+VTT POWER SUPPLY



+V3.3S	+V3.3S	14,16,23,24,26,29,31,32,34,35,36,37,38,39,40,41,42,43,44,45,46
+V5S	+V5S	12,14,16,32,38,39,43,44,45,46
+VBAT	+VBAT	9,10,12,13,44
+VTT	+VTT	13,14,19,20,21,22,23,24,26,27,30,32,36,46

+VTT:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.86A

2. Ripple Current:

Irip=3.42A

3. Ripple Voltage:

ESR/1=9mohm
Vrip=30.78mV

4. Inductor Spec:

Isat=36A
Idc=18A
DCR=3.3mohm

5.MOSFET Spec:

H-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)

L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)

6. Frequency:

F=290KHz (R0802=470K)

7. OCP:

Set = R0807 to 100K
Vtrip= R0807*10uA=1V
Iocp=(Vtrip/8*Rdson) + Iripple/2 = 16A

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Title	TPS51124 +V1.5/+V1.05	
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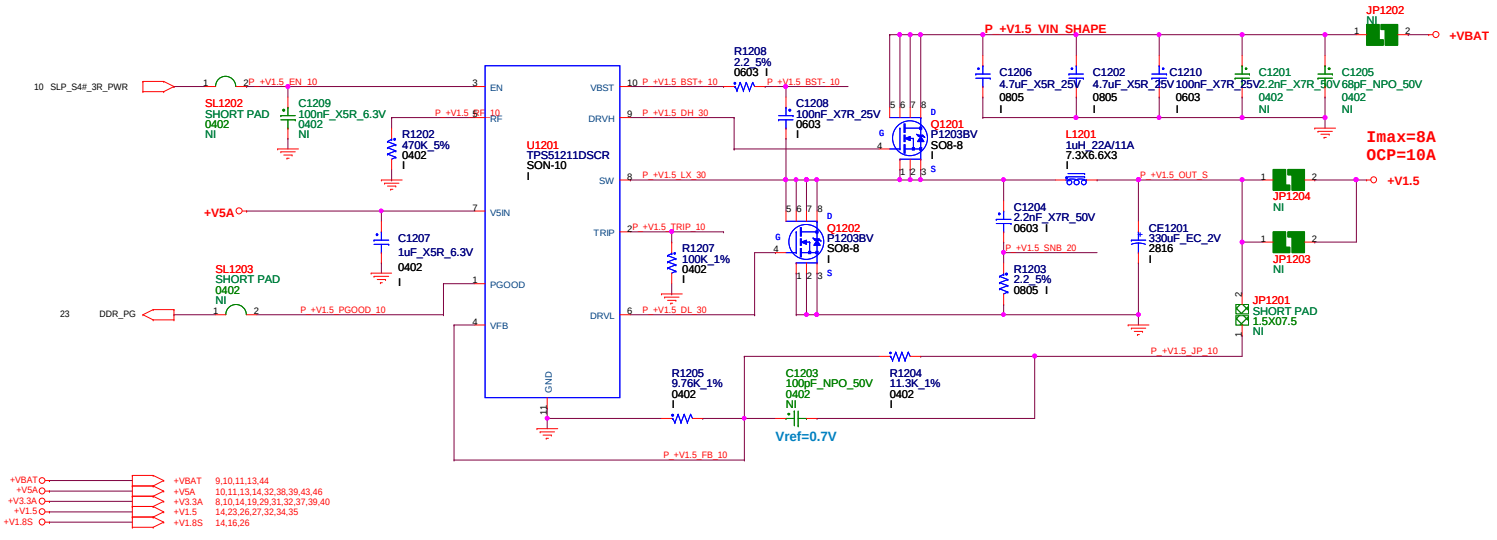
+V1.5 POWER SUPPLY



+V1.5:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.78A

2. Ripple Current:

Irip=3.34A

3. Ripple Voltage:

ESR/1=9mohm
Vrip=30.6mV

4. Inductor Spec:

Isat=36A
Idc=18A
DCR=3.3mohm

5.MOSFET Spec:

H-side MOSFET: IRF8707PBF		L-side MOSFET: IRF8707PBF	
Rds(ON)=17.5mohm	(Vgs=4.5 V)	Rds(ON)=17.5mohm	(Vgs=4.5 V)
I cont = 11A	(T =25 ℃)	I cont = 11A	(T =25 ℃)
I peak = 88A	(Pause =10 us)	I peak = 88A	(Pause =10 us)

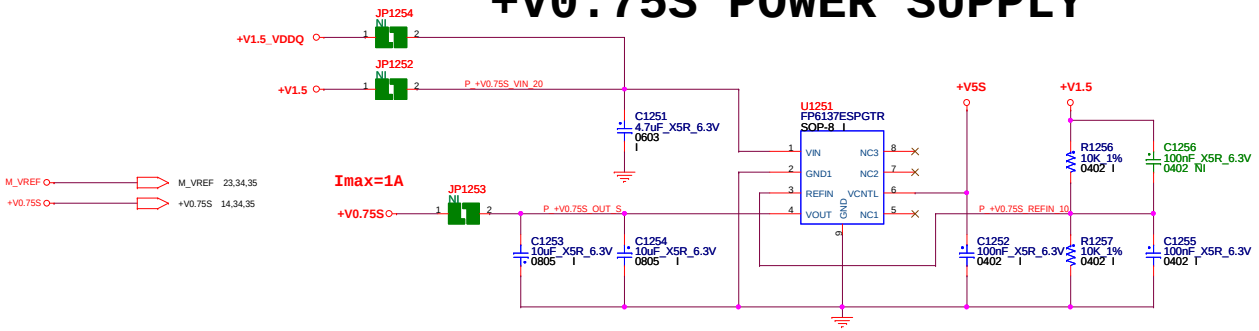
6. Frequency:

F=290KHz (R0902=470K)

7. OCP:

Set = R0907 to 100K
Vtrip= R0907*10uA=1V
Iocp=(Vtrip/8*Rdson) + Iripple/2 = 9.5A

+V0.75S POWER SUPPLY



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Title: +V0.75/+V1.8S			
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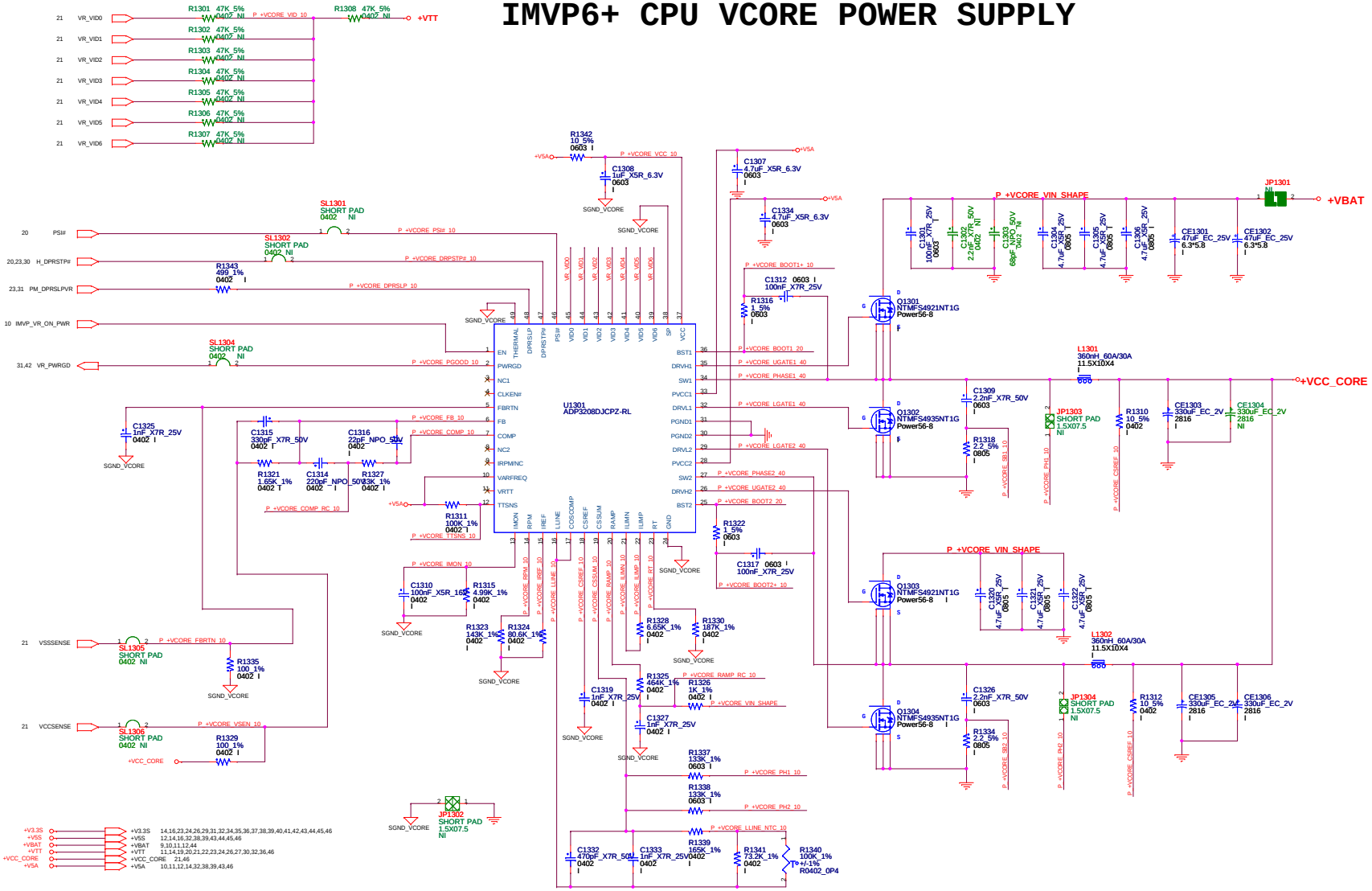
IMVP6+ CPU VCORE POWER SUPPLY



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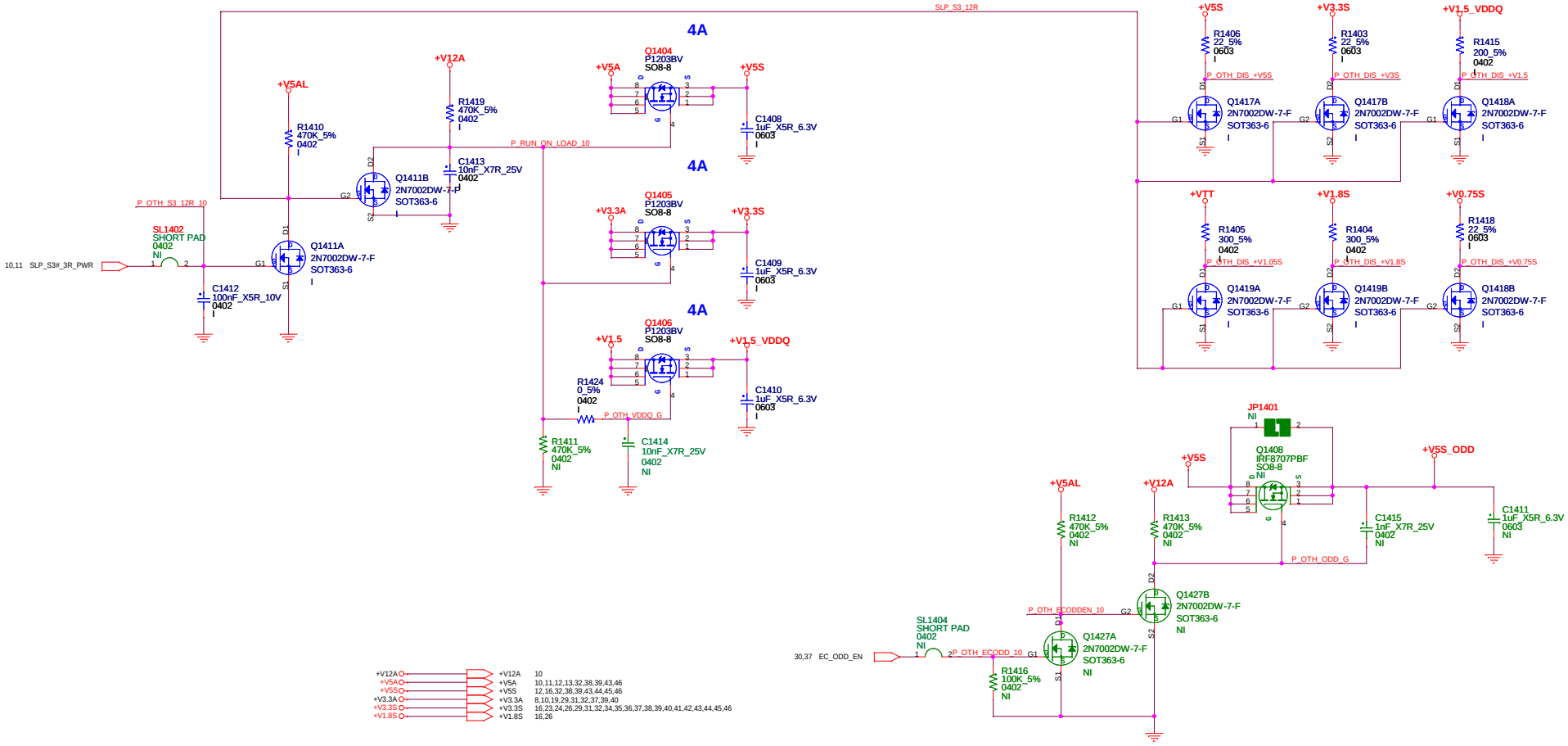
OTHER POWER / DISCHARGE CIRCUITS



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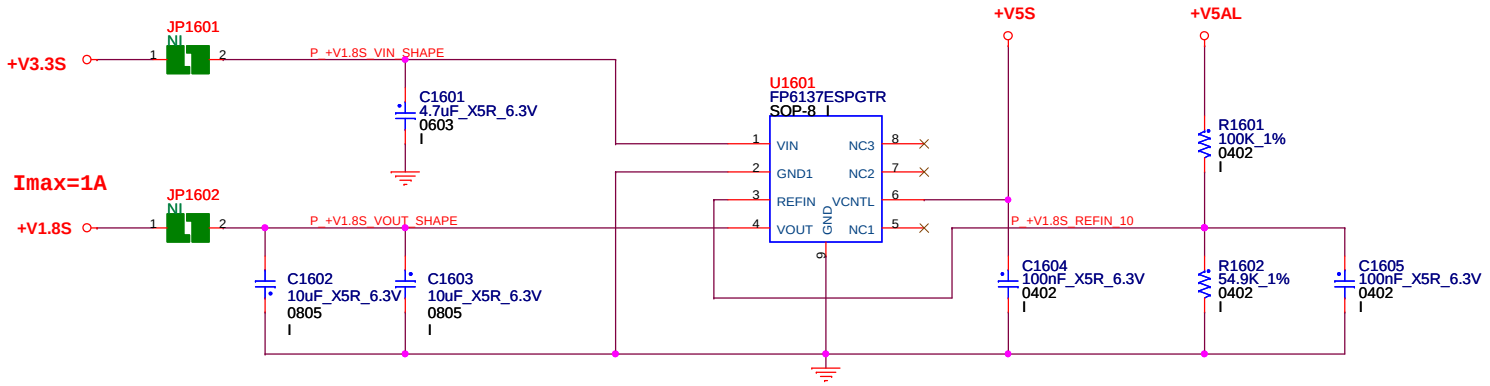
+V1.8S POWER SUPPLY



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Title		
PWR_1.8VS		
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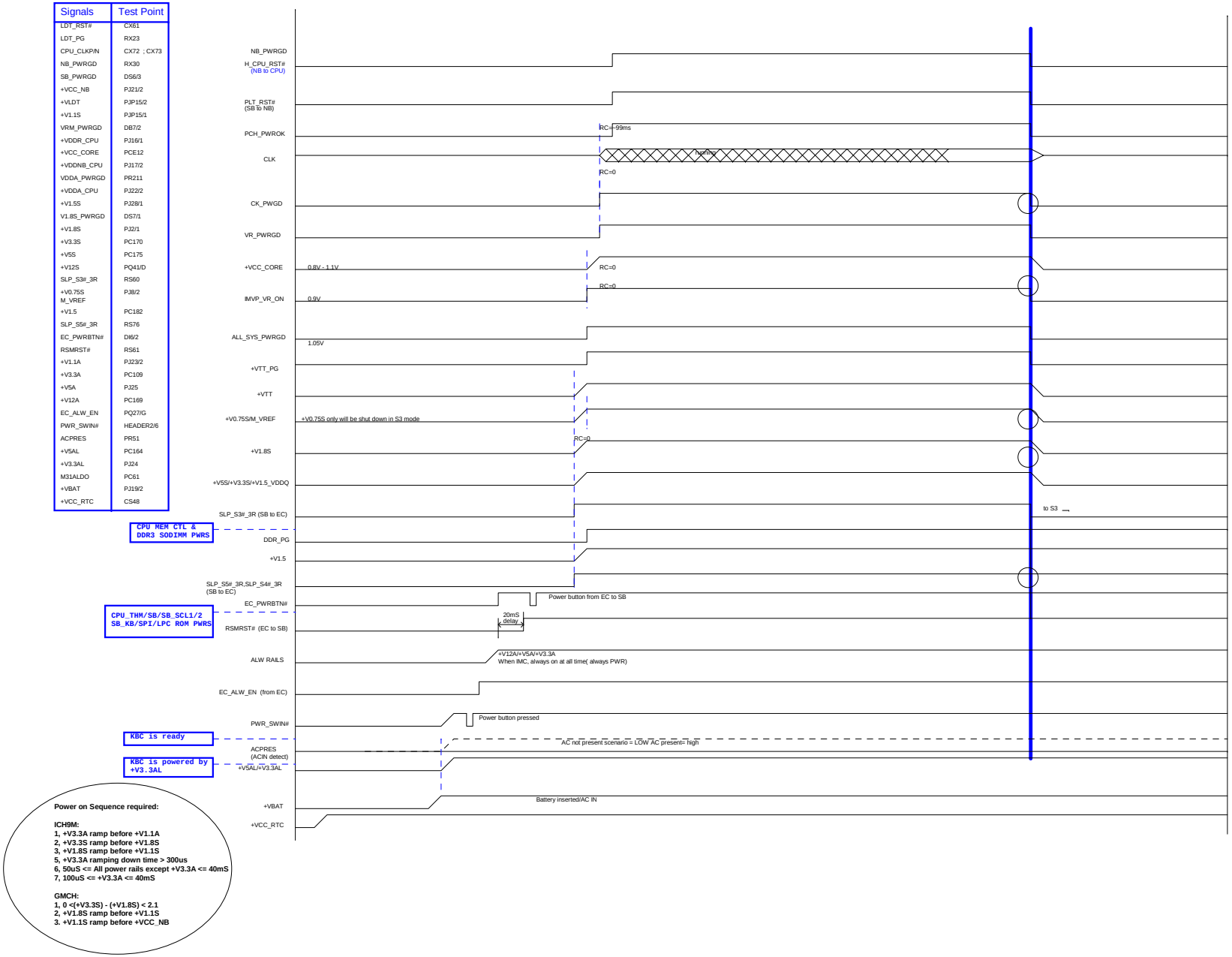
Signals	Test Point
LDT_RST#	CX61
LDT_PG	RX23
CPU_CLKP/N	CX72 ; CX73
NB_PWRGD	RX30
SB_PWRGD	DS6/3
+VCC_NB	PJ21/2
+VLDT	PJP15/2
+V1.1S	PJP15/1
VRM_PWRGD	DB7/2
+VDDR_CPU	PJ16/1
+VCC_CORE	PCE12
+VDDNB_CPU	PJ17/2
VDDA_PWRGD	PR211
+VDDA_CPU	PJ22/2
+V1.5S	PJ28/1
V1.8S_PWRGD	DS7/1
+V1.8S	PJ2/1
+V3.3S	PC170
+V5S	PC175
+V12S	PQ41/D
SLP_S3#_3R	RS60
+V0.75S M_VREF	PJ8/2
+V1.5	PC182
SLP_S5#_3R	RS76
EC_PWRBTN#	DI6/2
RSMRST#	RS61
+V1.1A	PJ23/2
+V3.3A	PC109
+V5A	PJ25
+V12A	PC169
EC_ALW_EN	PQ27/G
PWR_SWIN#	HEADER2/6
ACPRES	PR51
+V5AL	PC164
+V3.3AL	PJ24
M31ALDO	PC61
+VBAT	PJ19/2
+VCC_RTC	CS48



Power on Sequence required:

ICH9M:
1, +V3.3A ramp before +V1.1A
2, +V3.3S ramp before +V1.8S
3, +V1.8S ramp before +V1.1S
5, +V3.3A ramping down time > 300us
6, 50uS <= All power rails except +V3.3A <= 40mS
7, 100uS <= +V3.3A <= 40mS

GMCH:
1, 0 <(+V3.3S) - (+V1.8S) < 2.1
2, +V1.8S ramp before +V1.1S
3. +V1.1S ramp before +VCC_NB

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Title: **POWER SEQUENCE TIMING**

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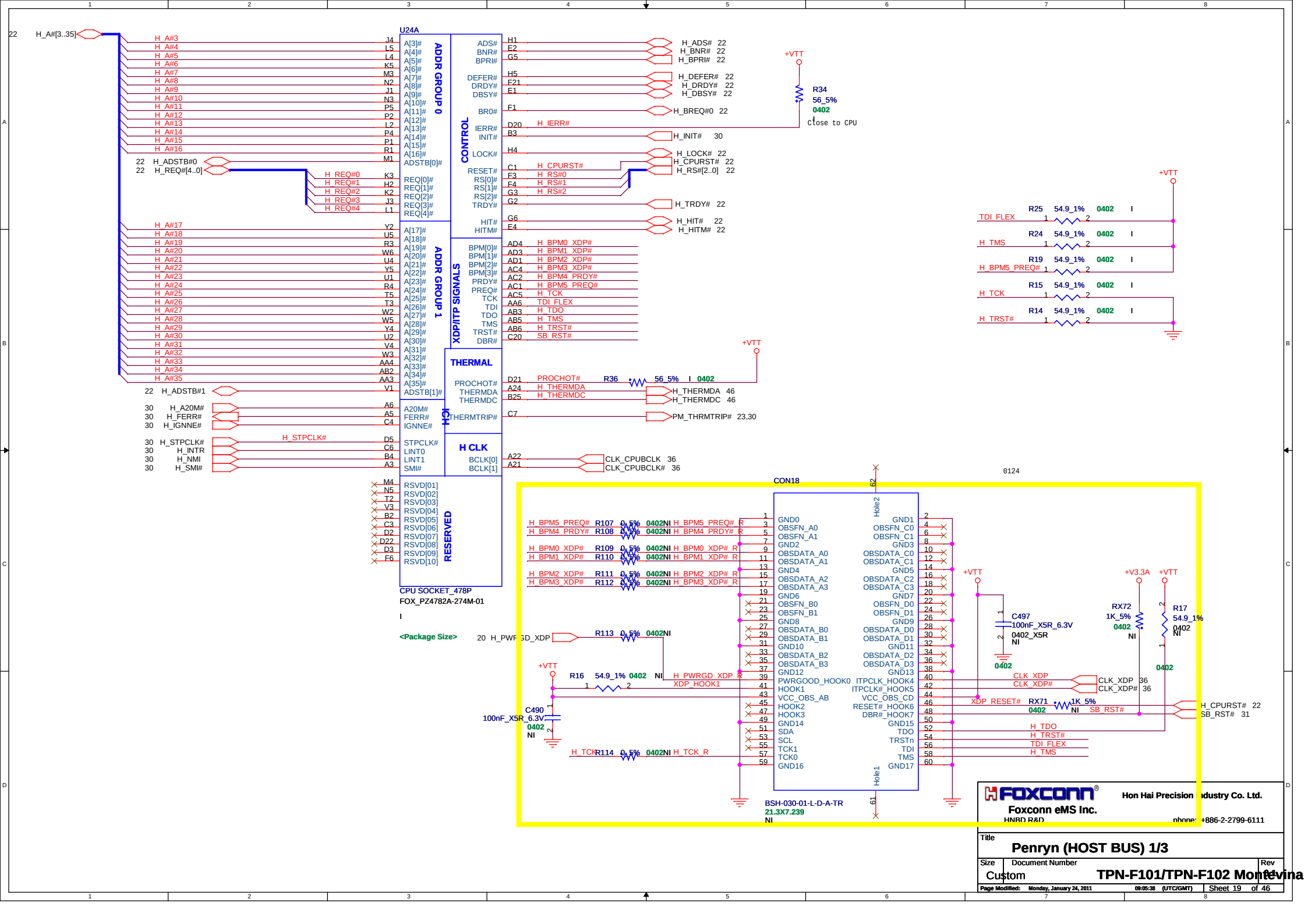
U24A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
CPU SOCKET_478P
FOX_PZ4782A-274M-01
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CON18
BSH-030-01-L-D-A-TR
21.3X7.239
Penryn (HOST BUS) 1/3
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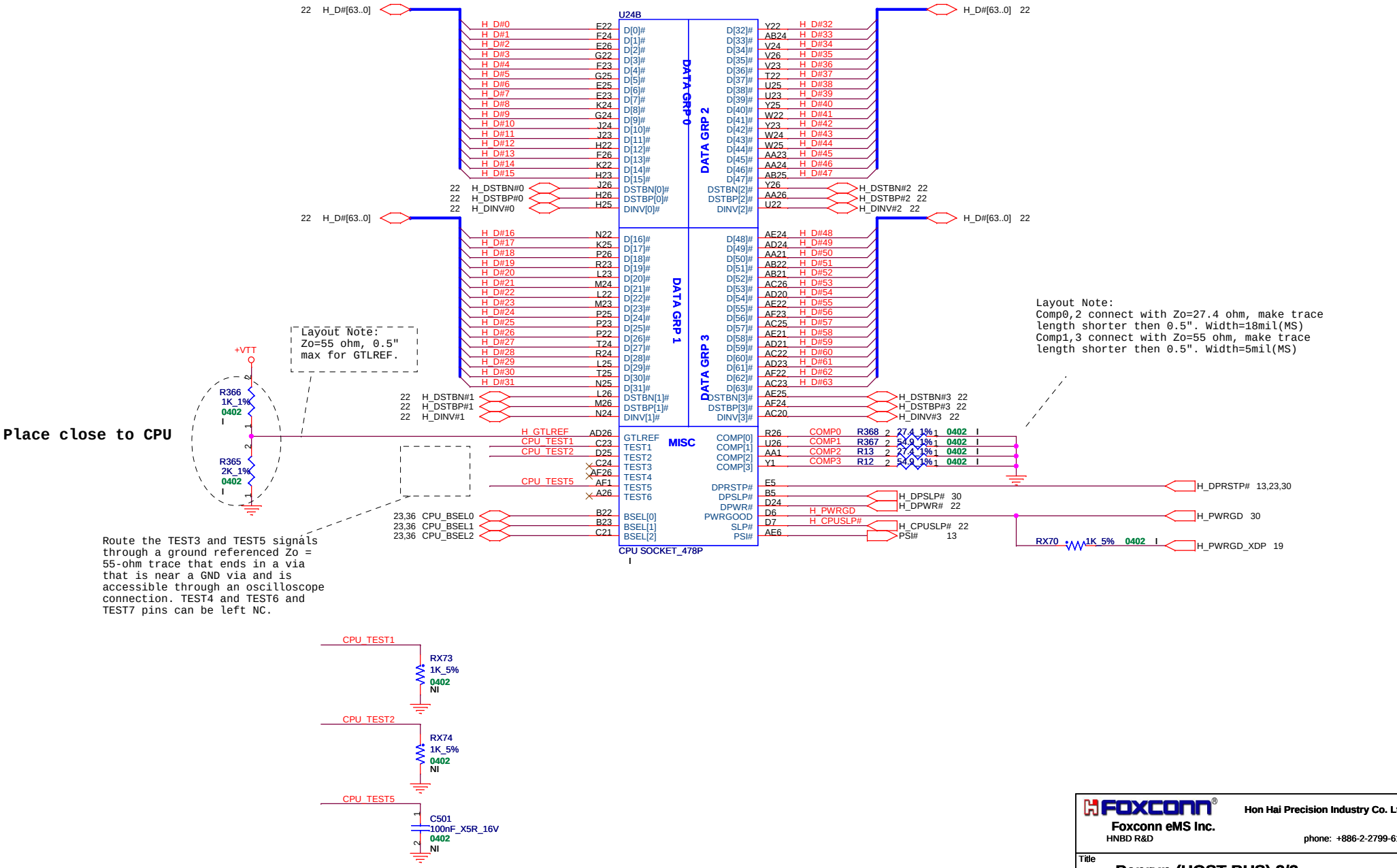

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Title: Penryn (HOST BUS) 2/3		
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina	Rev: 0.1
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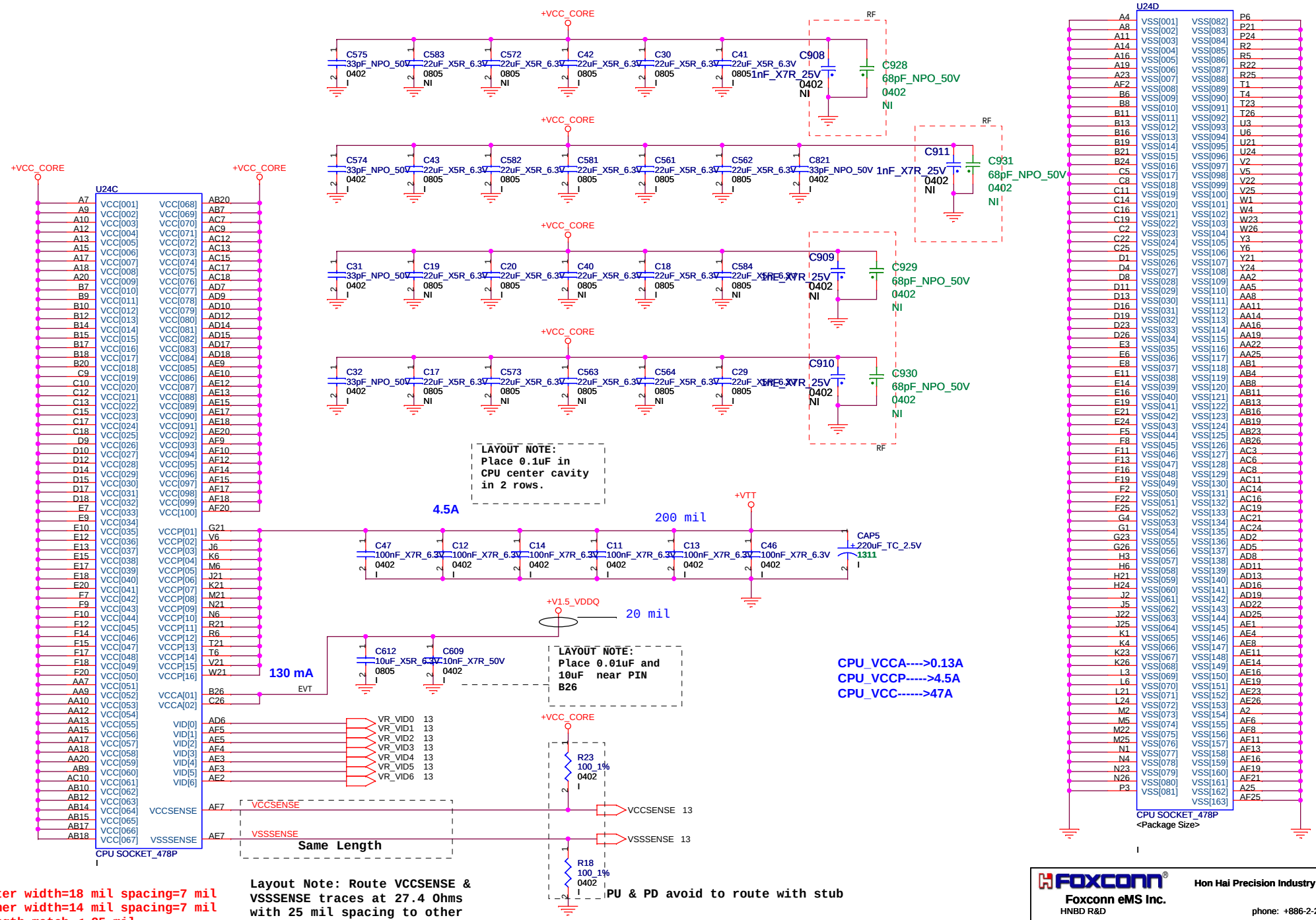

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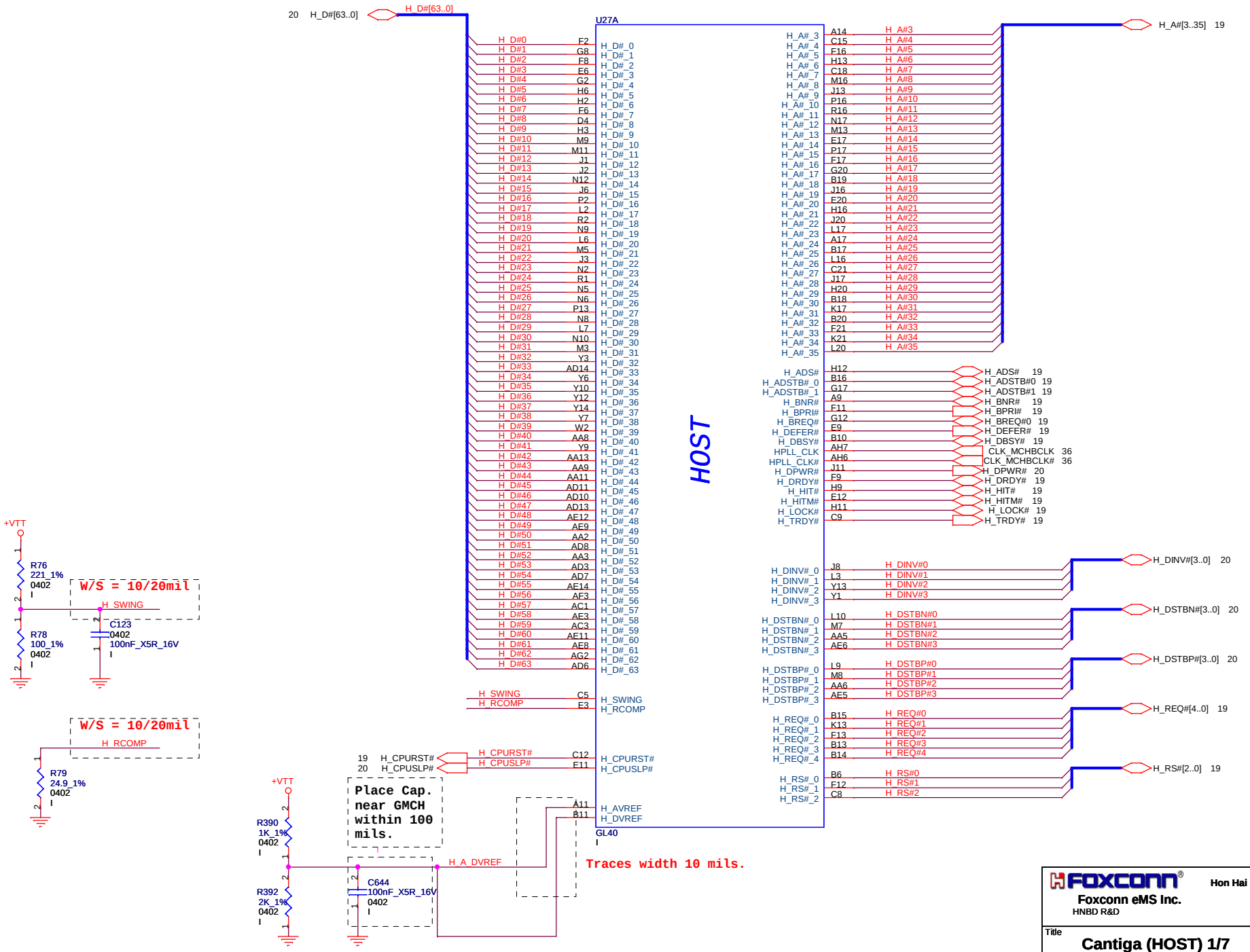
HNBD R&D	phone: +886-2-2799-6111
Title	Penryn (POWER/GROUND) 3/3
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina
Rev: 1A	
Page Modified: Monday, January 24, 2011 09:05:39 (UTC/GMT)	Sheet 21 of 46



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Title: **Cantiga (HOST) 1/7**

Size	Document Number	Rev
Custom	TPN-F101/TPN-F102 Montevina	1A

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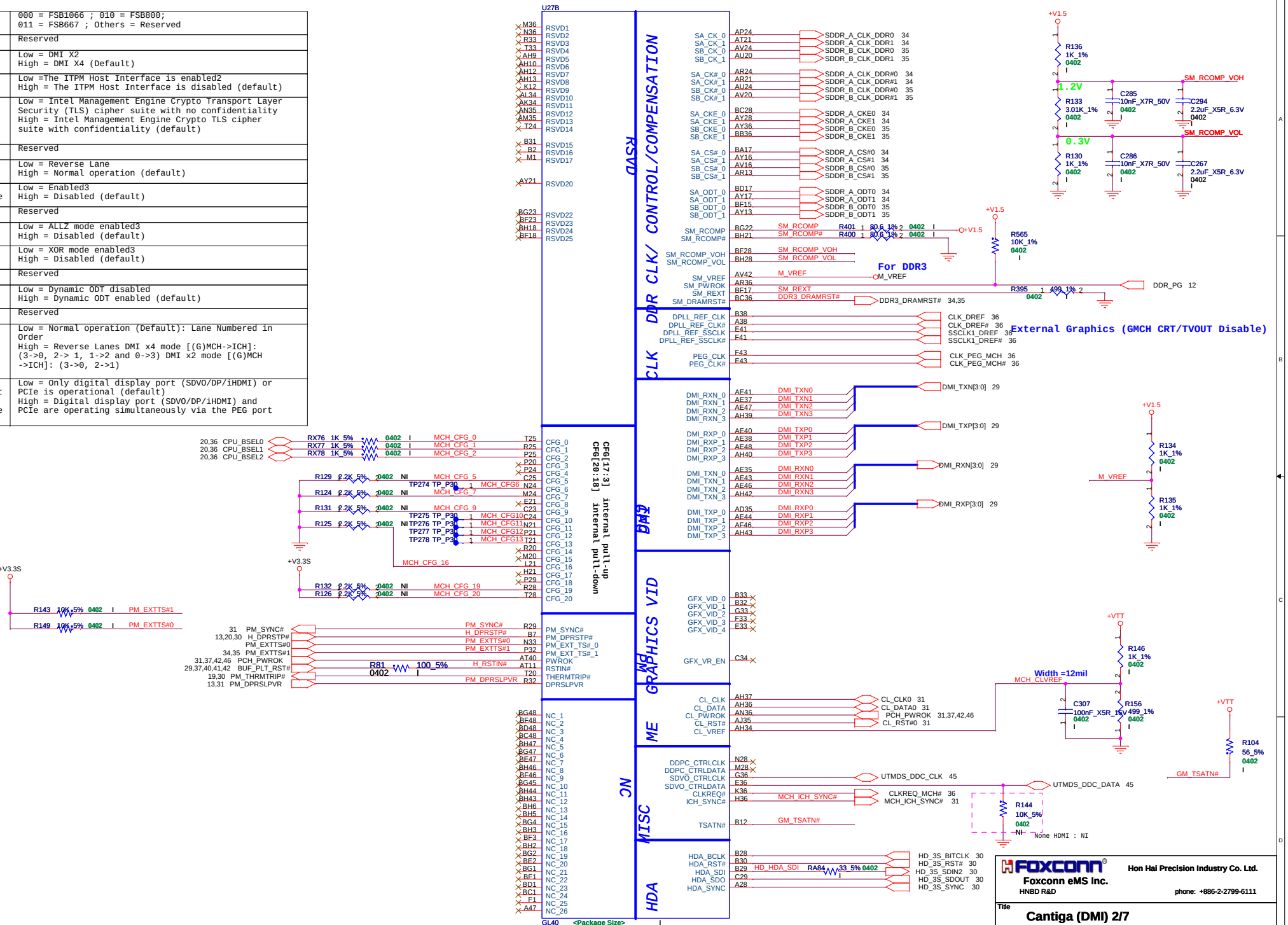
MCH_CFG_0~2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3~4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low =The ITPM Host Interface is enabled2 High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIE Graphics Lane	Low = Reverse Lane High = Normal operation (default)
MCH_CFG_10 PCIE Loopback enable	Low = Enabled3 High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled3 High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled3 High = Disabled (default)
MCH_CFG_14~15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17~18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2-> 1, 1->2 and 0->3) DMI x2 mode [(G)MCH ->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/ DP/iHDMI) Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port



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Title: Cantiga (DMI) 2/7

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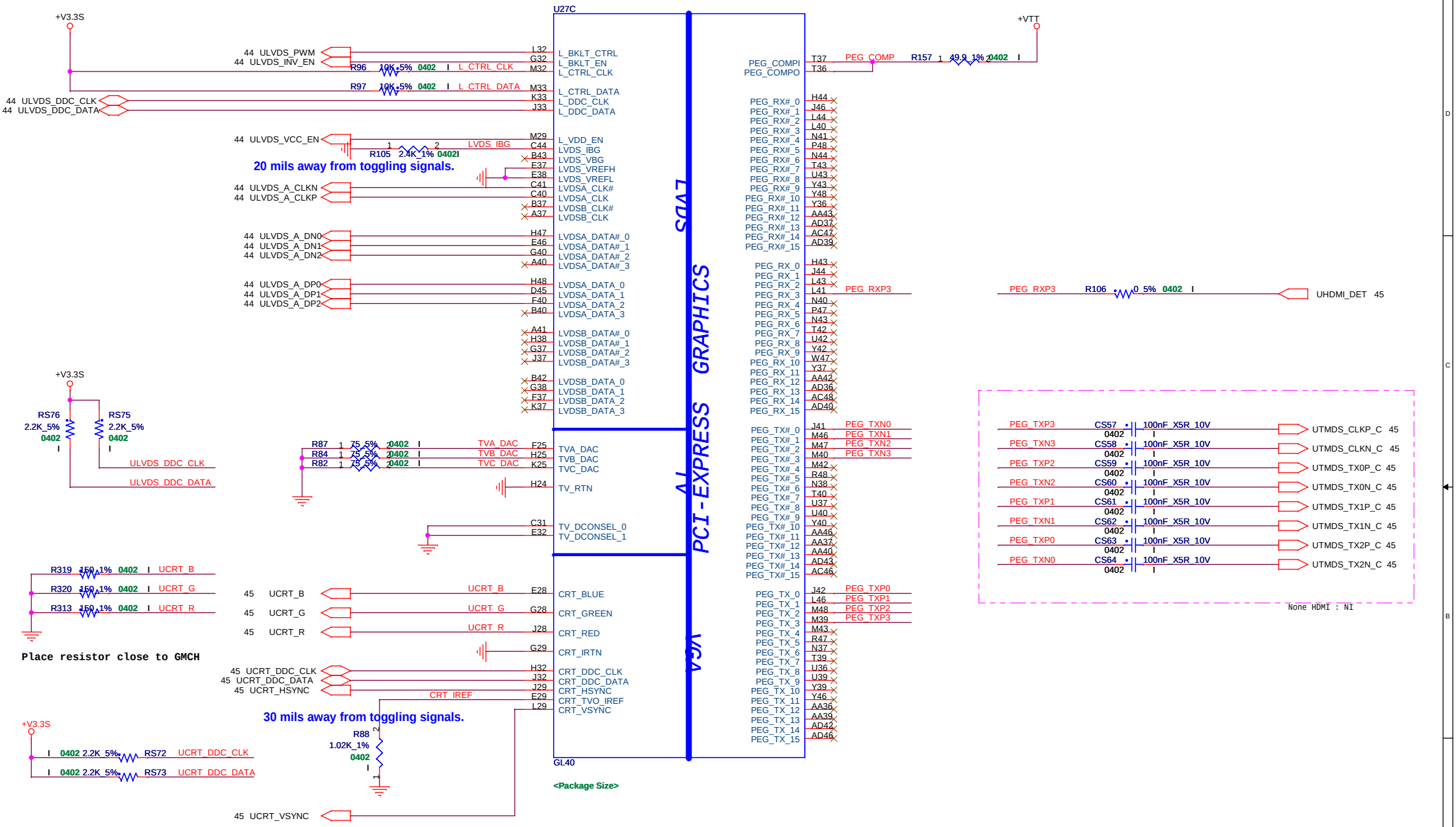

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Title: Cantiga (GRAPHIC) 3/7

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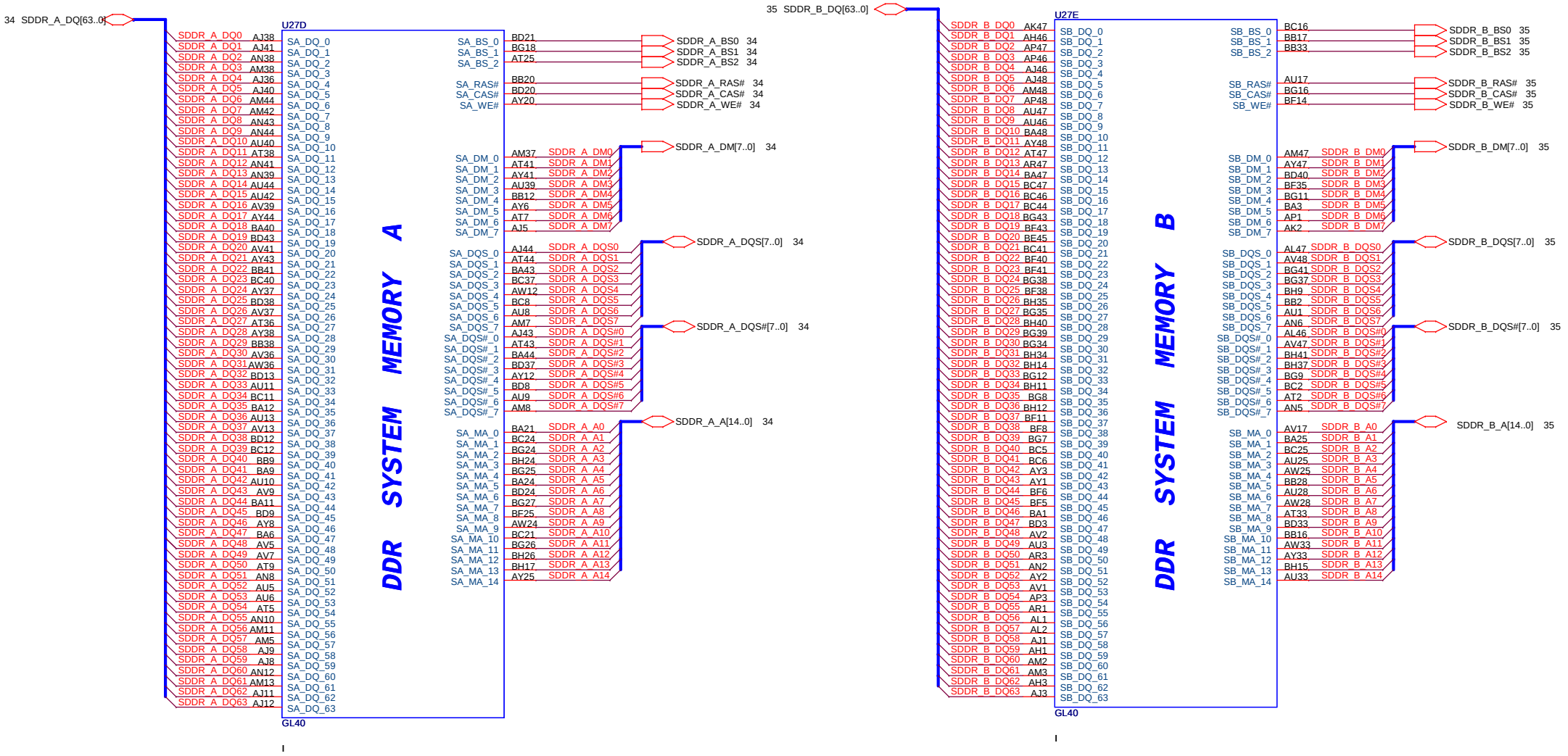

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Cantiga (DDR3) 4/7

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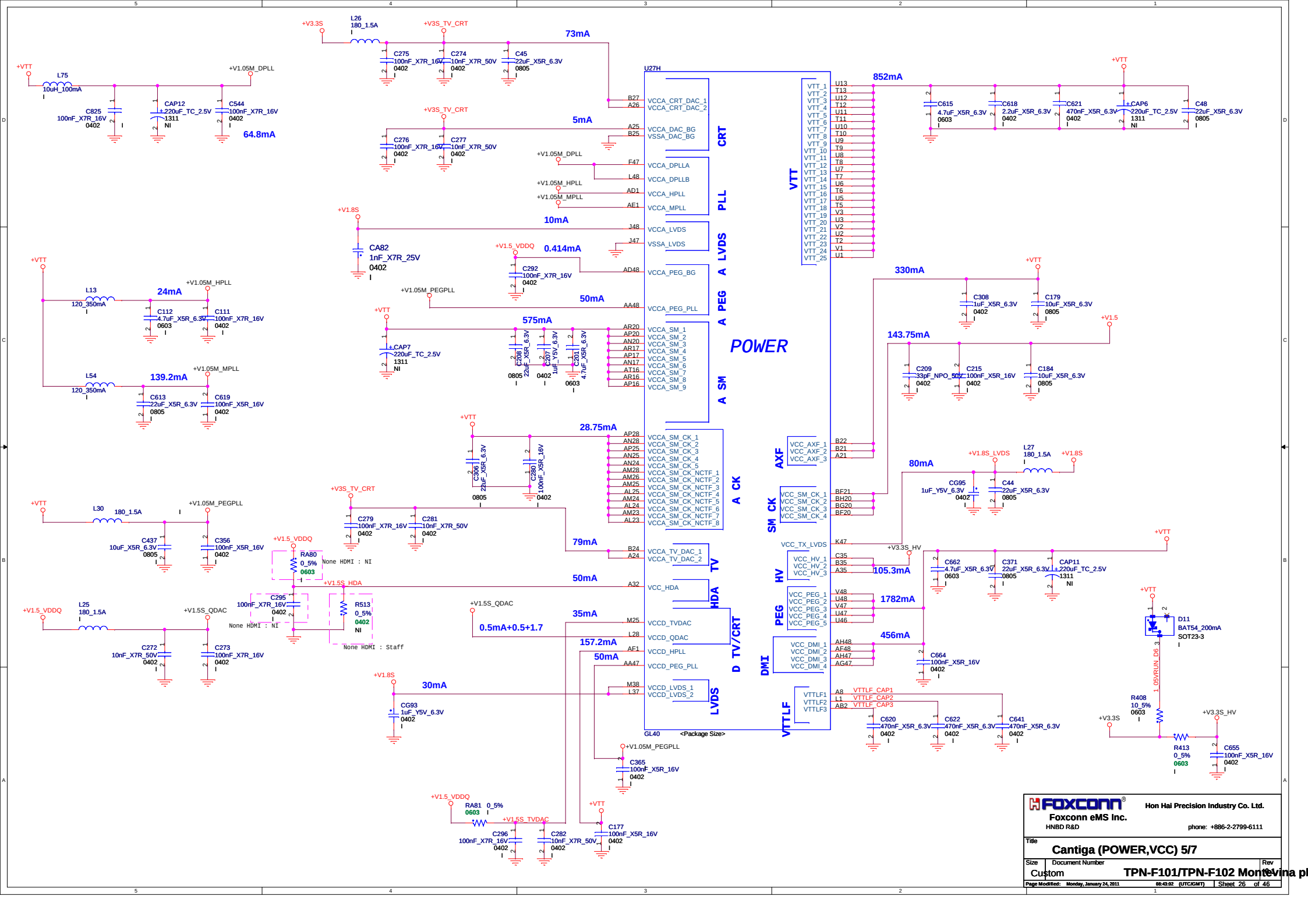
POWER
U27H
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
73mA
5mA
64.8mA
10mA
0.414mA
50mA
575mA
24mA
139.2mA
28.75mA
79mA
50mA
35mA
0.5mA+0.5+1.7
157.2mA
50mA
30mA
852mA
330mA
143.75mA
80mA
105.3mA
1782mA
456mA
L75
10uH_100mA
L26
180_1.5A
L13
120_350mA
L54
120_350mA
L30
180_1.5A
L25
180_1.5A
L27
180_1.5A
CA82
1nF_X7R_25V
0402
RA80
0_5%
0603
None HDMI : NI
RA81
0_5%
0603
R513
0_5%
0402
NI
R408
10_5%
0603
R413
0_5%
0603
D11
BAT54_200mA
SOT23-3
1.05VRUN_D6_3
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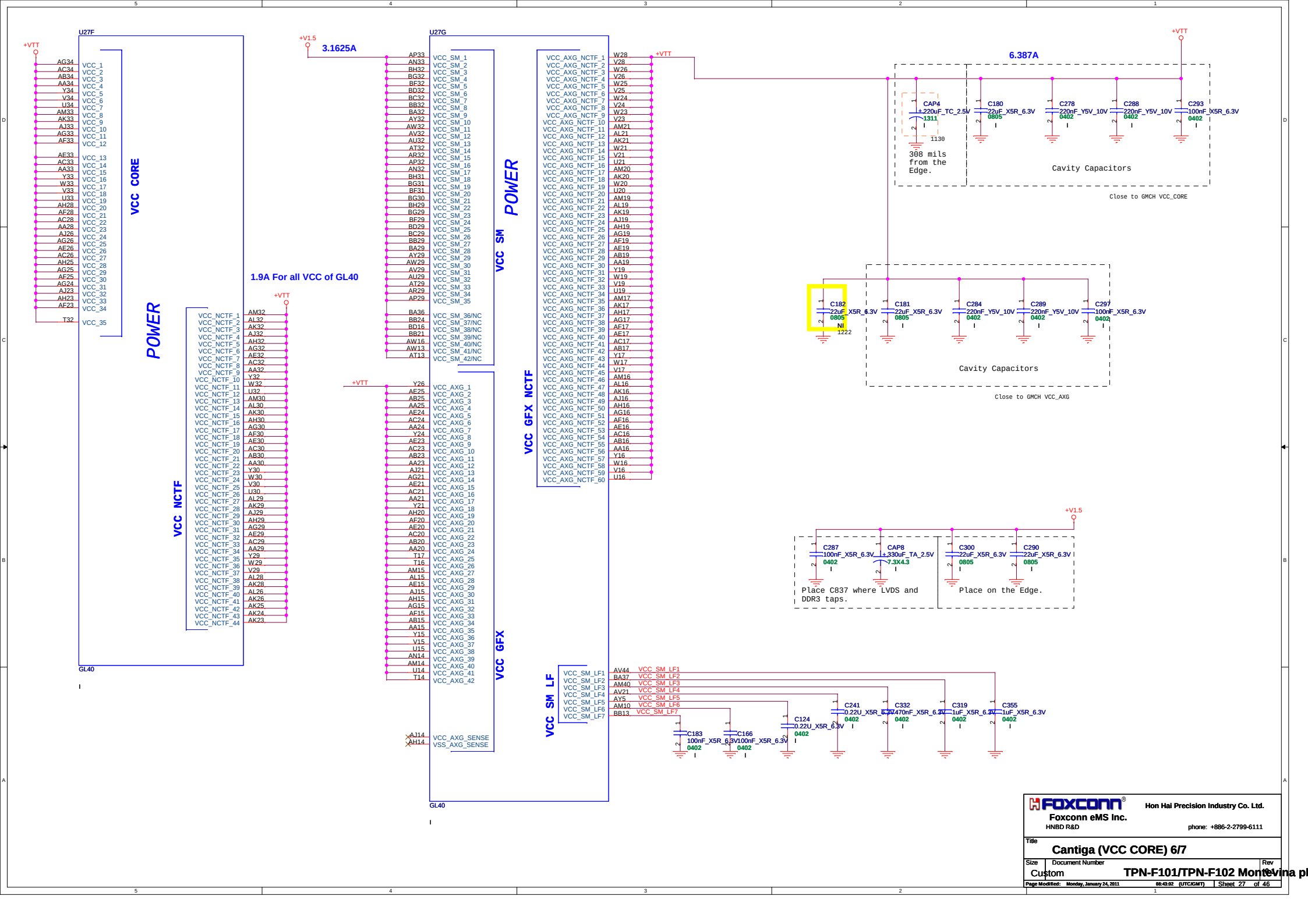
Cantiga (POWER,VCC) 5/7
Custom
TPN-F101/TPN-F102 Montevina pl
Sheet 26 of 46



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Title: Cantiga (VCC CORE) 6/7

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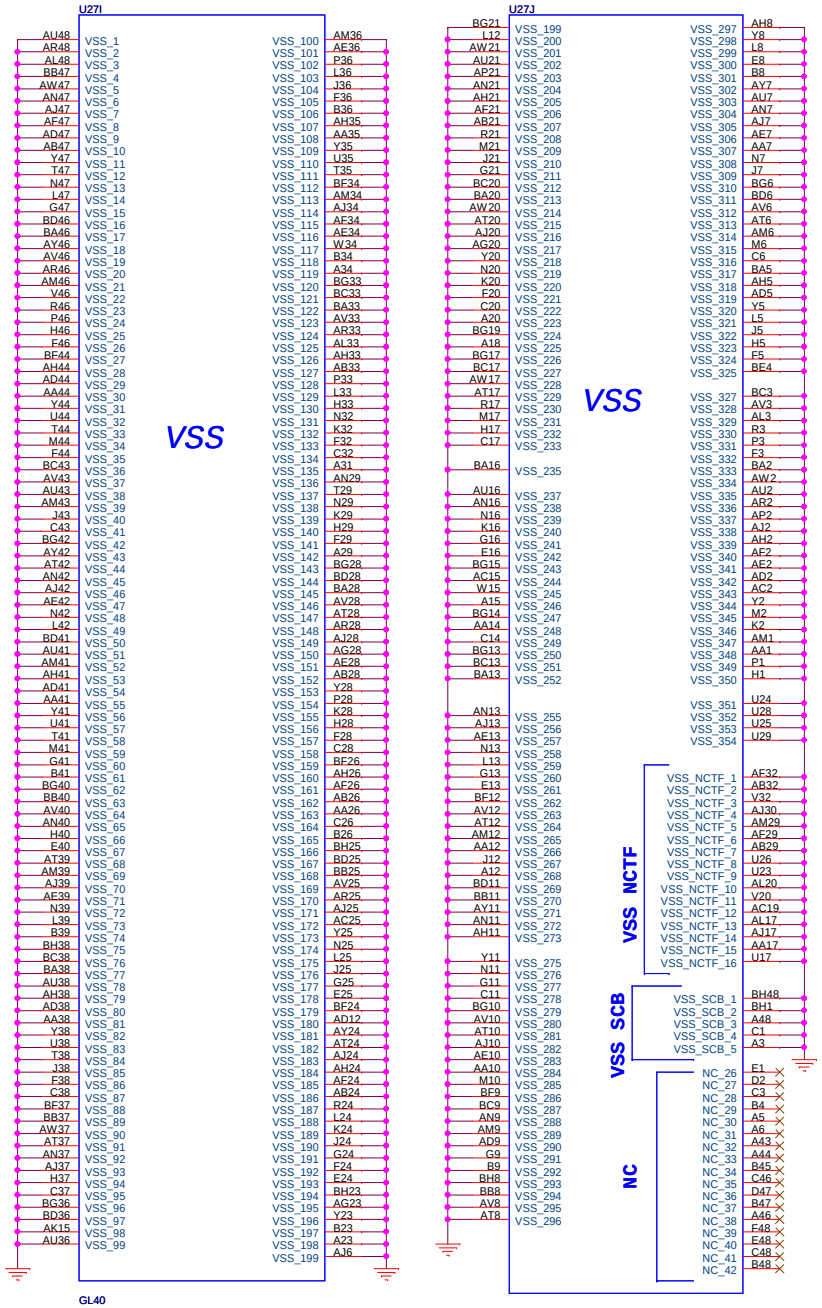
Page Modified: Monday, January 24, 2011 08:43:02 (UTC/GMT) | Sheet 27 of 46



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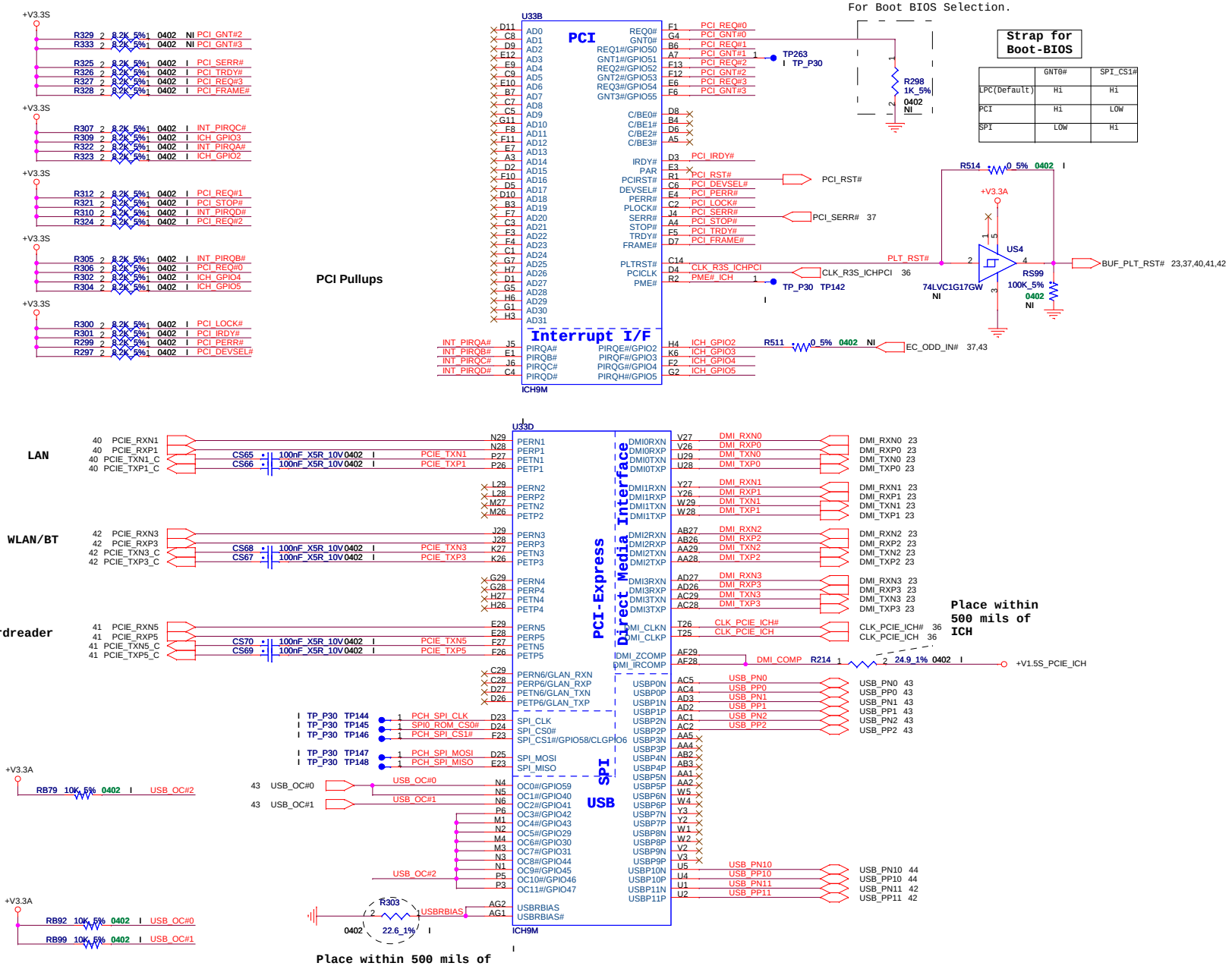
Title	Cantiga (VSS) 7/7
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina pl
Rev: 1.0	
Page Modified: Monday, January 24, 2011 08:43:03 (UTC/GMT)	Sheet 28 of 46



USB PORT	Function	OC pin
PORT-0	Ext. USB 0	
PORT-1	Ext. USB 1	
PORT-2	Ext. USB 2	
PORT-3		
PORT-4		
PORT-5		
PORT-6		
PORT-7		
PORT-8		
PORT-9		
PORT-10	Camera	
PORT-11	WLAN/BT	
PORT-12		
PORT-13		

	GNT0#	SPI_CS1#
LPC(Default)	Hi	Hi
PCI	Hi	LOW
SPI	LOW	Hi

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Title: ICH9-M(PCI/DMI/USB/PCIE) 1/5

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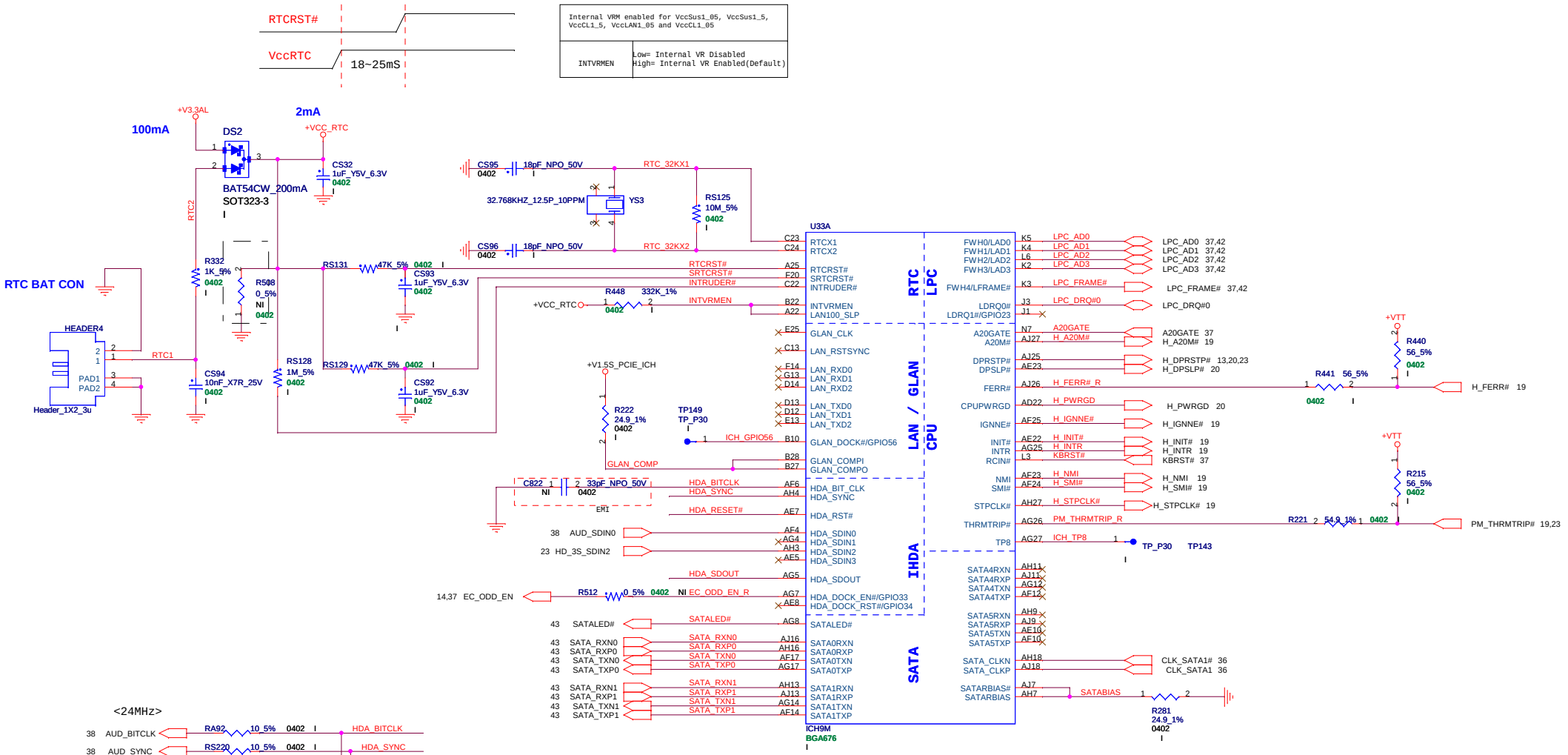

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Title	ICH9-M(LPC,IDE,SATA) 2/5
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina pl
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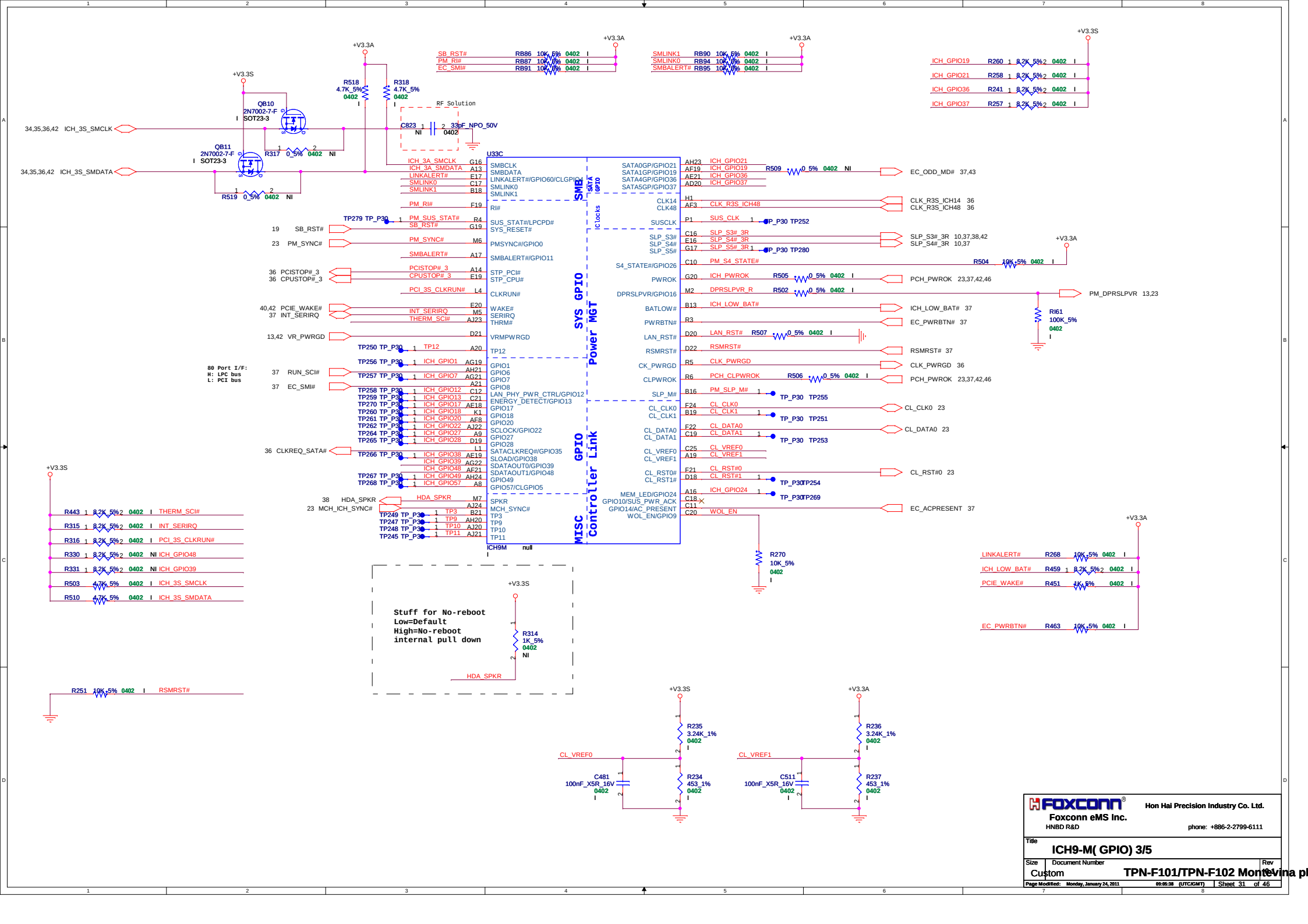
Page Modified: Monday, January 24, 2011 09:05:39 (UTC/GMT)	Sheet 30 of 46


U33C
ICH9M
SMB
SATA GPIO
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP12
GPIO1
GPIO6
GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
TP9
TP10
TP11
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#0
CL_RST#1
MEM_LED/GPIO24
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
WOL_EN/GPIO9
+V3.3S
+V3.3A
QB10
2N7002-7-F
SOT23-3
QB11
2N7002-7-F
SOT23-3
R317 0_5% 0402 NI
R518 4.7K_5% 0402
R318 4.7K_5% 0402
RF Solution
C823 NI 33pF_NPO_50V 0402
R519 0_5% 0402 NI
34,35,36,42 ICH_3S_SMCLK
34,35,36,42 ICH_3S_SMDATA
SB_RST# RB86 10K_5% 0402
PM_RI# RB87 10K_5% 0402
EC_SMI# RB91 10K_5% 0402
SMLINK1 RB90 10K_5% 0402
SMLINK0 RB94 10K_5% 0402
SMBALERT# RB95 10K_5% 0402
ICH_GPIO19 R260 8.2K_5% 0402
ICH_GPIO21 R258 8.2K_5% 0402
ICH_GPIO36 R241 8.2K_5% 0402
ICH_GPIO37 R257 8.2K_5% 0402
ICH_3A_SMCLK
ICH_3A_SMDATA
LINKALERT#
SMLINK0
SMLINK1
PM_RI#
TP279 TP_P30 PM_SUS_STAT#
SB_RST#
PM_SYNC#
SMBALERT#
PCISTOP#_3
CPUSTOP#_3
PCI_3S_CLKRUN#
INT_SERIRQ
THERM_SCI#
VR_PWRGD
TP250 TP_P30 TP12
TP256 TP_P30 ICH_GPIO1
TP257 TP_P30 ICH_GPIO7
TP258 TP_P30 ICH_GPIO12
TP259 TP_P30 ICH_GPIO13
TP270 TP_P30 ICH_GPIO17
TP260 TP_P30 ICH_GPIO18
TP261 TP_P30 ICH_GPIO20
TP262 TP_P30 ICH_GPIO22
TP264 TP_P30 ICH_GPIO27
TP265 TP_P30 ICH_GPIO28
TP266 TP_P30 ICH_GPIO38
ICH_GPIO39
ICH_GPIO48
TP267 TP_P30 ICH_GPIO49
TP268 TP_P30 ICH_GPIO57
HDA_SPKR
TP249 TP_P30 TP3
TP247 TP_P30 TP9
TP248 TP_P30 TP10
TP245 TP_P30 TP11
80 Port I/F:
H: LPC bus
L: PCI bus
19 SB_RST#
23 PM_SYNC#
36 PCISTOP#_3
36 CPUSTOP#_3
40,42 PCIE_WAKE#
37 INT_SERIRQ
13,42 VR_PWRGD
37 RUN_SCI#
37 EC_SMI#
36 CLKREQ_SATA#
38 HDA_SPKR
23 MCH_ICH_SYNC#
AH23 ICH_GPIO21
AF19 ICH_GPIO19
AE21 ICH_GPIO36
AD20 ICH_GPIO37
R509 0_5% 0402 NI
EC_ODD_MD# 37,43
CLK_R3S_ICH14 36
CLK_R3S_ICH48 36
SUS_CLK
SLP_S3#_3R 10,37,38,42
SLP_S4#_3R 10,37
PM_S4_STATE#
R504 10K_5% 0402
ICH_PWROK R505 0_5% 0402
PCH_PWROK 23,37,42,46
DPRSLPVR_R R502 0_5% 0402
PM_DPRSLPVR 13,23
RI61 100K_5% 0402
ICH_LOW_BAT# 37
EC_PWRBTN# 37
LAN_RST# R507 0_5% 0402
RSMRST# 37
CLK_PWRGD 36
PCH_CLPWROK R506 0_5% 0402
PCH_PWROK 23,37,42,46
CL_CLK0 23
CL_DATA0 23
CL_RST#0 23
EC_ACPRESENT 37
R270 10K_5%
R443 8.2K_5% 0402 THERM_SCI#
R315 8.2K_5% 0402 INT_SERIRQ
R316 8.2K_5% 0402 PCI_3S_CLKRUN#
R330 8.2K_5% 0402 NI ICH_GPIO48
R331 8.2K_5% 0402 NI ICH_GPIO39
R503 4.7K_5% 0402 ICH_3S_SMCLK
R510 4.7K_5% 0402 ICH_3S_SMDATA
LINKALERT# R268 10K_5% 0402
ICH_LOW_BAT# R459 8.2K_5% 0402
PCIE_WAKE# R451 1K_5% 0402
EC_PWRBTN# R463 10K_5% 0402
Stuff for No-reboot
Low=Default
High=No-reboot
internal pull down
R314 1K_5% 0402 NI
HDA_SPKR
R251 10K_5% 0402 RSMRST#
R235 3.24K_1% 0402
R234 453_1% 0402
C481 100nF_X5R_16V 0402
CL_VREF0
R236 3.24K_1% 0402
R237 453_1% 0402
C511 100nF_X5R_16V 0402
CL_VREF1
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Title
ICH9-M(GPIO) 3/5
Size Custom
Document Number
TPN-F101/TPN-F102 Montevina pl
Rev
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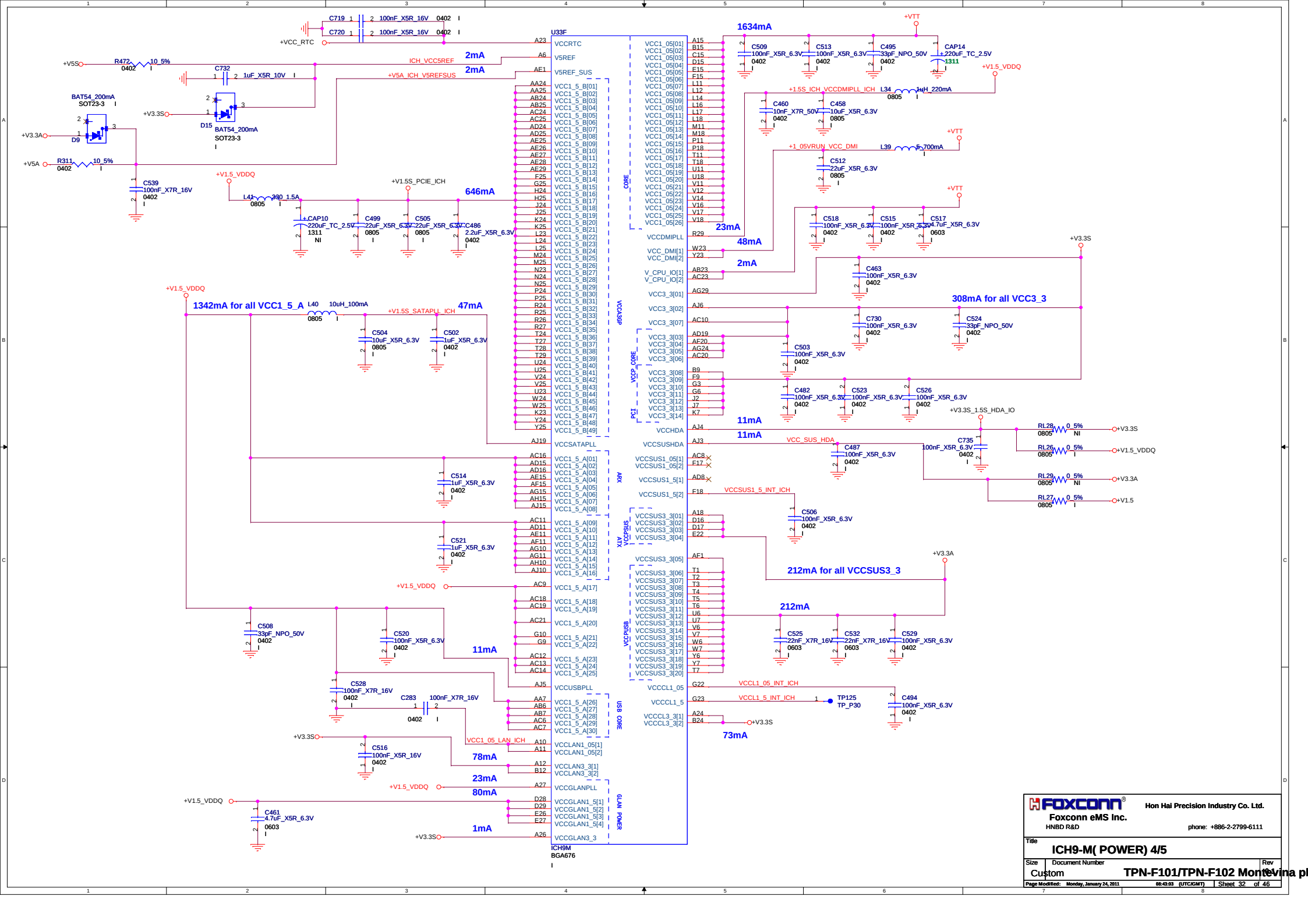
U33F
ICH9M
BGA676
1634mA
23mA
48mA
2mA
2mA
646mA
1342mA for all VCC1_5_A
47mA
11mA
11mA
11mA
78mA
23mA
80mA
1mA
73mA
308mA for all VCC3_3
212mA for all VCCSUS3_3
212mA
+VTT
+V1.5_VDDQ
+V3.3S
+V3.3A
+V5S
+V5A
+VCC_RTC
+V1.5S_PCIE_ICH
+V1.5S_SATAPLL_ICH
+V3.3S_1.5S_HDA_IO
+1.5S_ICH_VCCDMIPLL_ICH
+1_05VRUN_VCC_DMI
ICH_VCC5REF
+V5A_ICH_V5REFSUS
VCC_SUS_HDA
VCCSUS1_5_INT_ICH
VCC1_05_LAN_ICH
VCCL1_05_INT_ICH
VCCL1_5_INT_ICH
TP125
TP_P30
CORE
VCCP_CORE
VCCSUS
VCCPUSB
USB CORE
GLAN POWER
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ICH9-M(POWER) 4/5
Custom
TPN-F101/TPN-F102 Montevina pl
Monday, January 24, 2011
08:43:03 (UTC/GMT)
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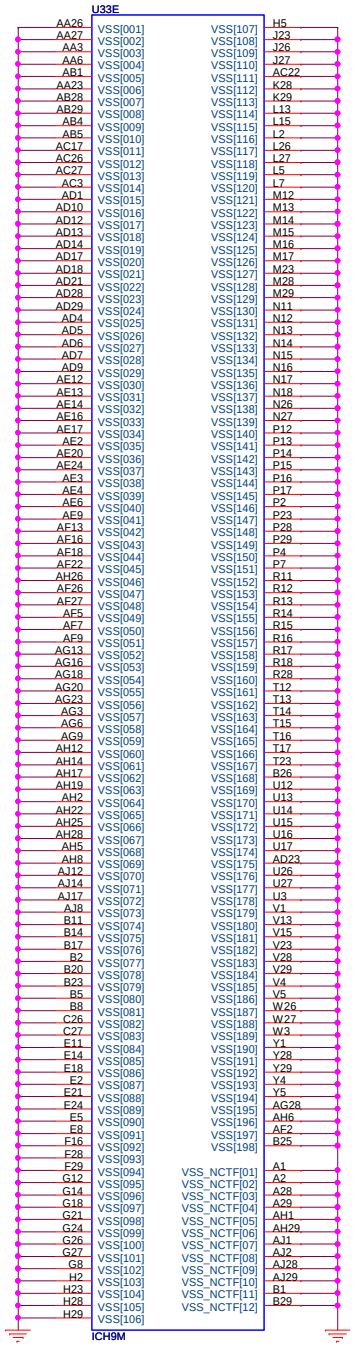

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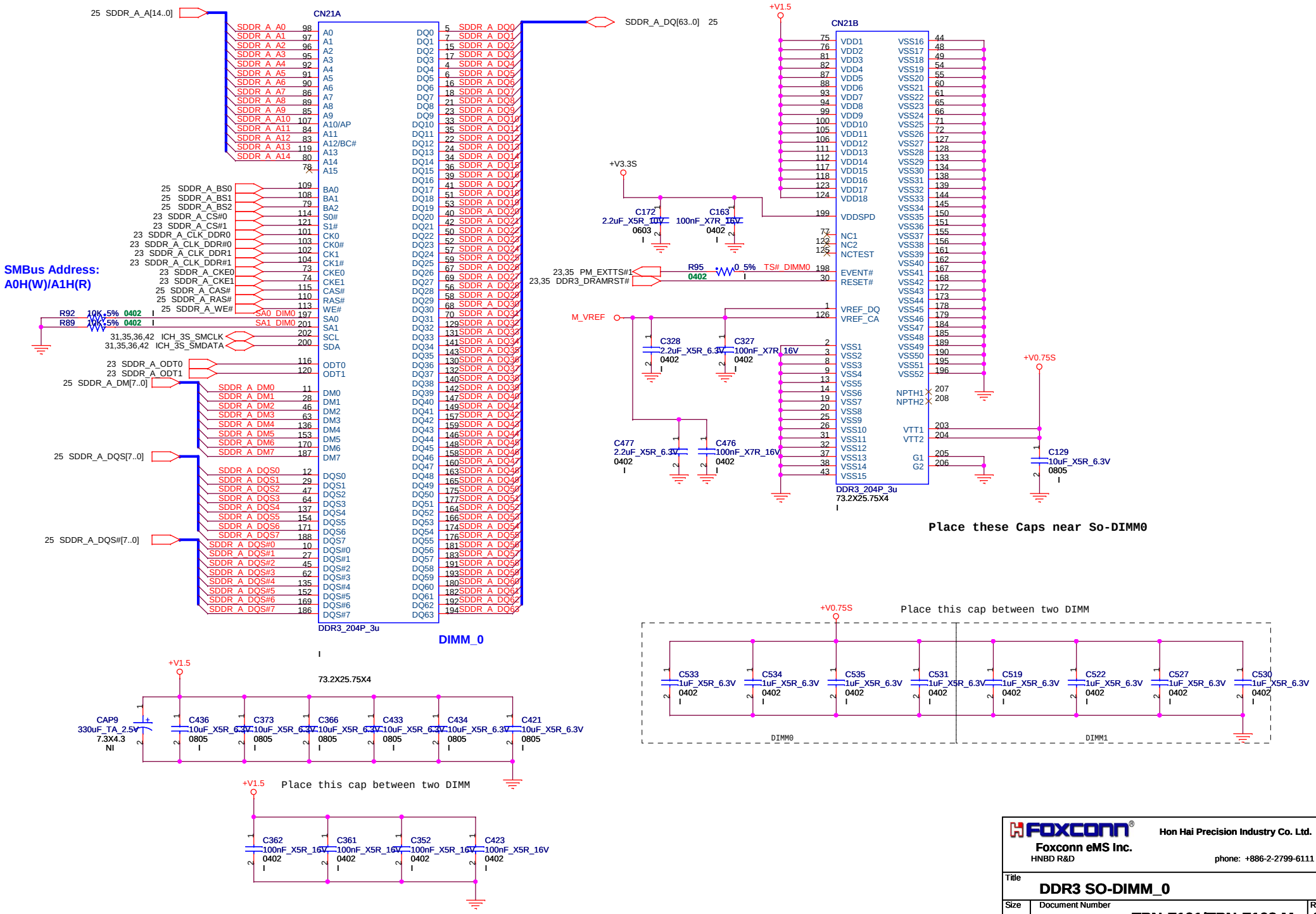
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina pl
Rev: 1.0	
Page Modified: Monday, January 24, 2011 08:43:02 (UTC/GMT)	Sheet 33 of 46



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Title	DDR3 SO-DIMM_0
Size	Custom
Document Number	TPN-F101/TPN-F102 Montevina
Rev	0.1
Page Modified:	Monday, January 24, 2011 09:05:38 (UTC/GMT)
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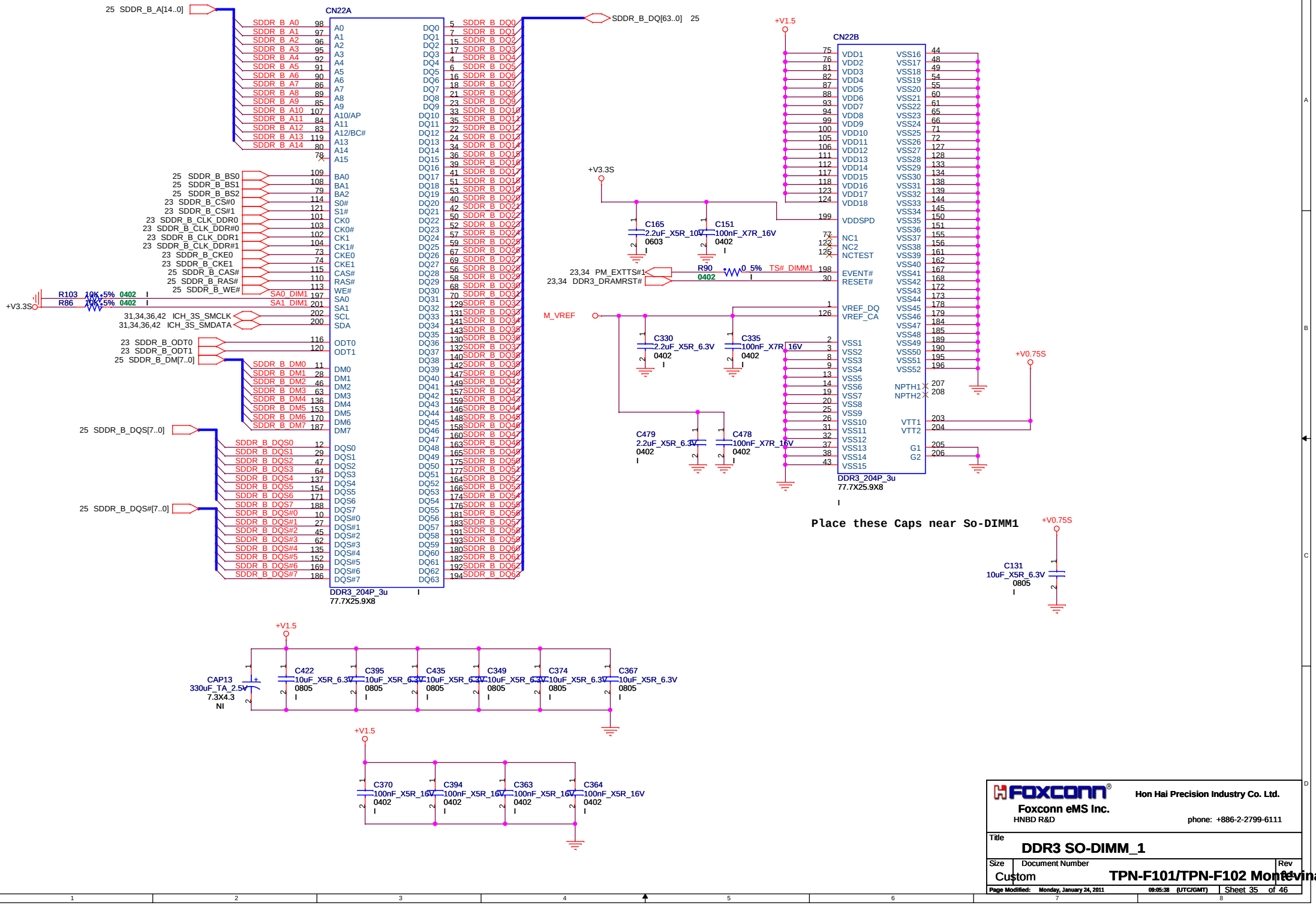

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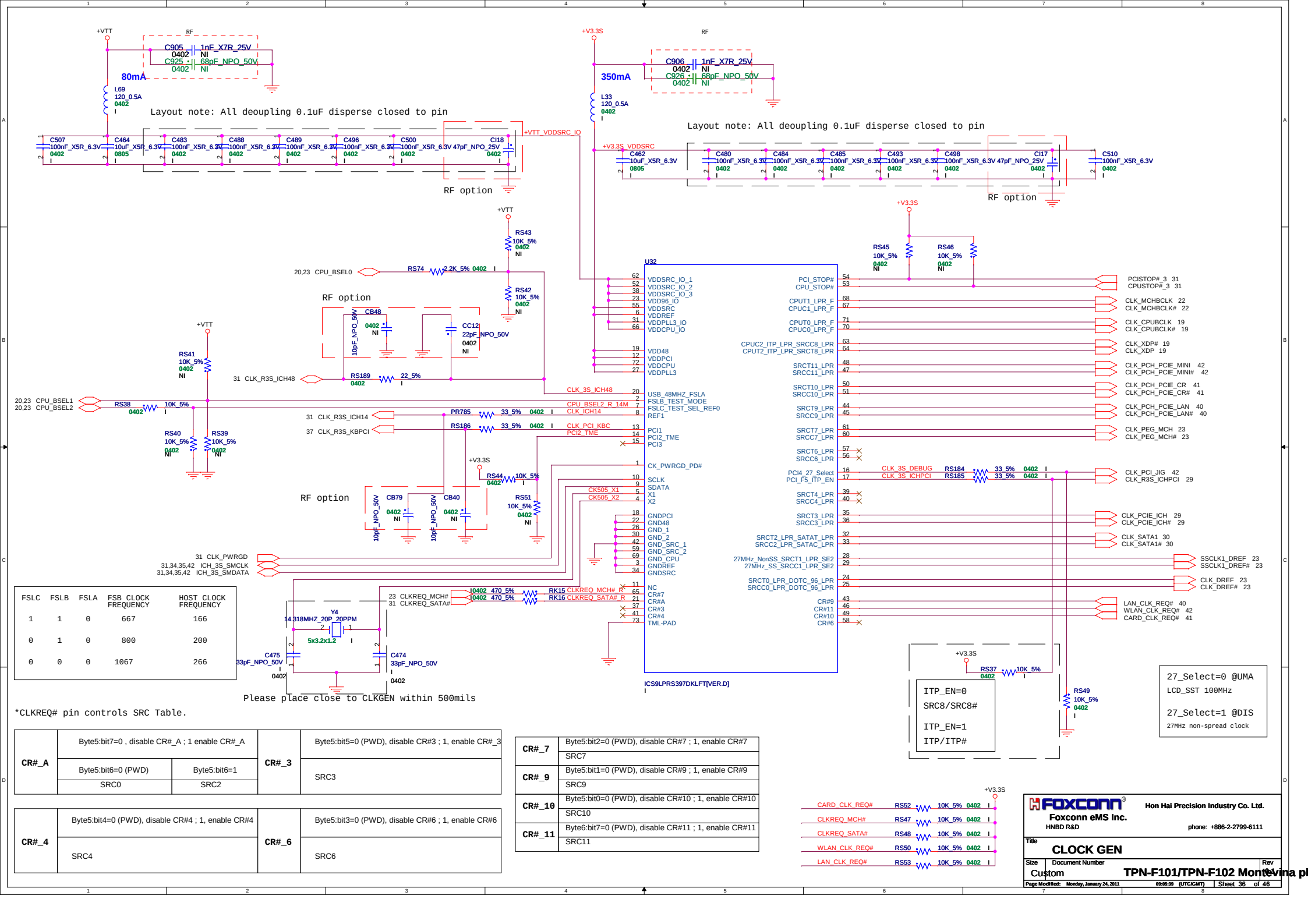
Foxconn eMS Inc.	
HNBD R&D	phone: +886-2-2799-6111
Title	DDR3 SO-DIMM_1
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina
Rev: 0.1	
Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT)	Sheet 35 of 46



FSLC	FSLB	FSLA	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1067	266

*CLKREQ# pin controls SRC Table.

CR#_A	Byte5:bit7=0 , disable CR#_A ; 1 enable CR#_A		**CR#_3**	Byte5:bit5=0 (PWD), disable CR#3 ; 1, enable CR#_3
	Byte5:bit6=0 (PWD)	Byte5:bit6=1		SRC3
	SRC0	SRC2		

CR#_4	Byte5:bit4=0 (PWD), disable CR#4 ; 1, enable CR#4		**CR#_6**	Byte5:bit3=0 (PWD), disable CR#6 ; 1, enable CR#6
	SRC4			SRC6

CR#_7	Byte5:bit2=0 (PWD), disable CR#7 ; 1, enable CR#7
	SRC7
CR#_9	Byte5:bit1=0 (PWD), disable CR#9 ; 1, enable CR#9
	SRC9
CR#_10	Byte5:bit0=0 (PWD), disable CR#10 ; 1, enable CR#10
	SRC10
CR#_11	Byte6:bit7=0 (PWD), disable CR#11 ; 1, enable CR#11
	SRC11

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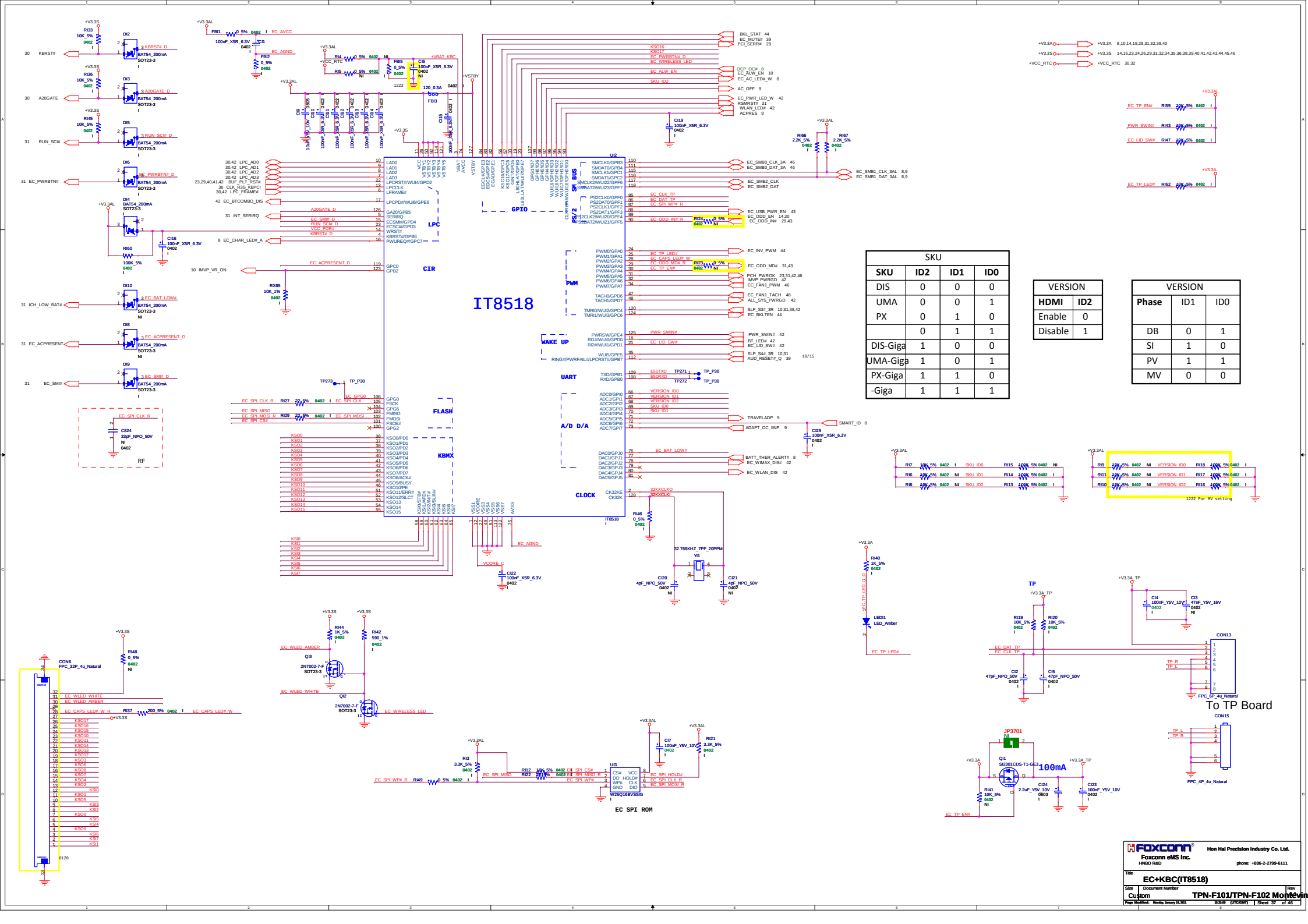
Size: Custom
Document Number: TPN-F101/TPN-F102 Montevina pl
Rev: 1.0
Page Modified: Monday, January 24, 2011 09:05:39 (UTC/GMT)
Sheet 36 of 46


IT8518
LPC
FWH
GPIO
SPI BUS
PS/2
CIR
PWM
WAKE UP
UART
A/D D/A
FLASH
KBMX
CLOCK
RF
EC SPI ROM
To TP Board
SKU
SKU ID2 ID1 ID0
DIS 0 0 0
UMA 0 0 1
PX 0 1 0
0 1 1
DIS-Giga 1 0 0
UMA-Giga 1 0 1
PX-Giga 1 1 0
-Giga 1 1 1
VERSION
HDMI ID2
Enable 0
Disable 1
VERSION
Phase ID1 ID0
DB 0 1
SI 1 0
PV 1 1
MV 0 0
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phone: +886-2-2799-6111
EC+KBC(IT8518)
Custom
TPN-F101/TPN-F102 Monkevin
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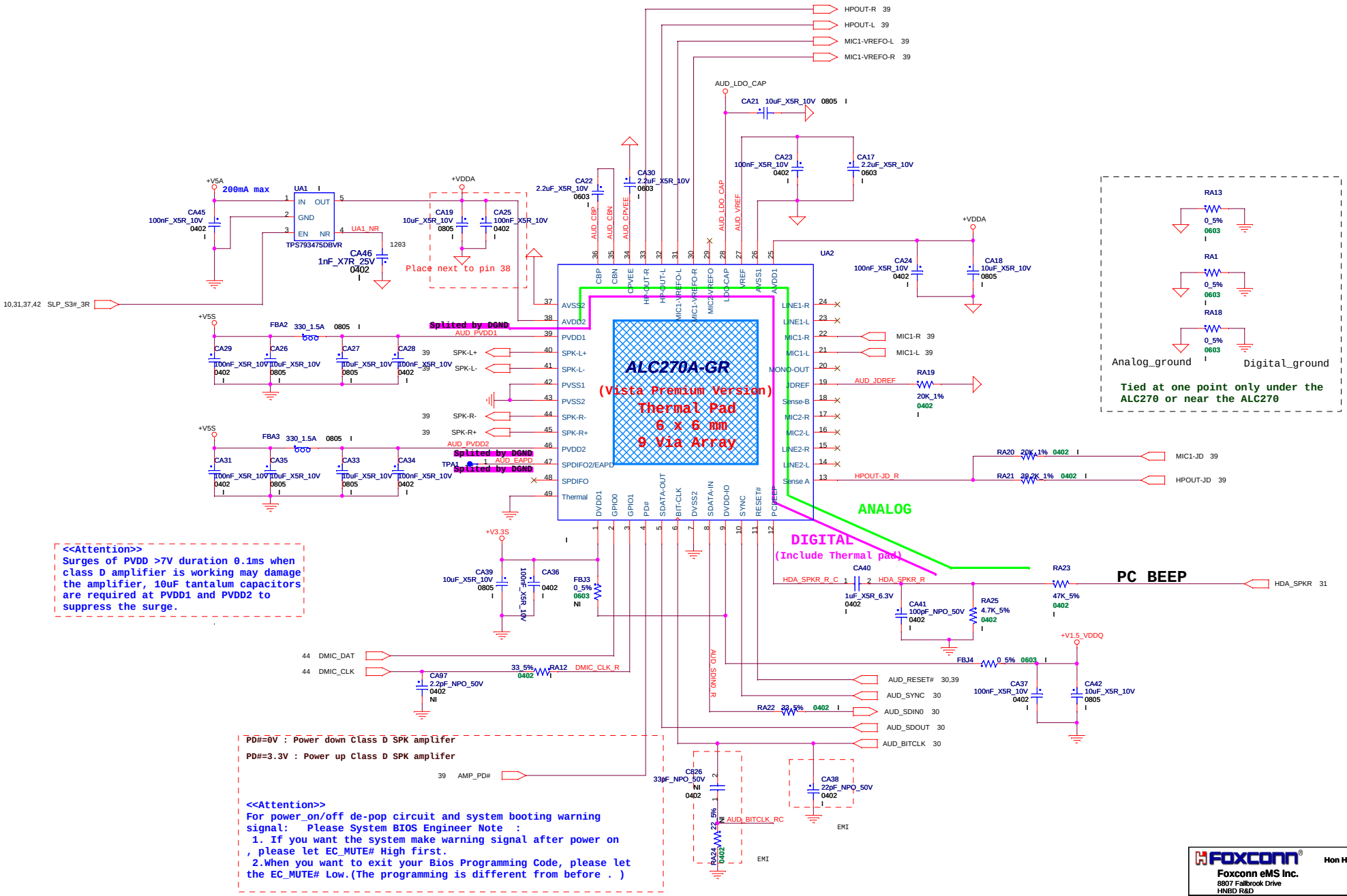
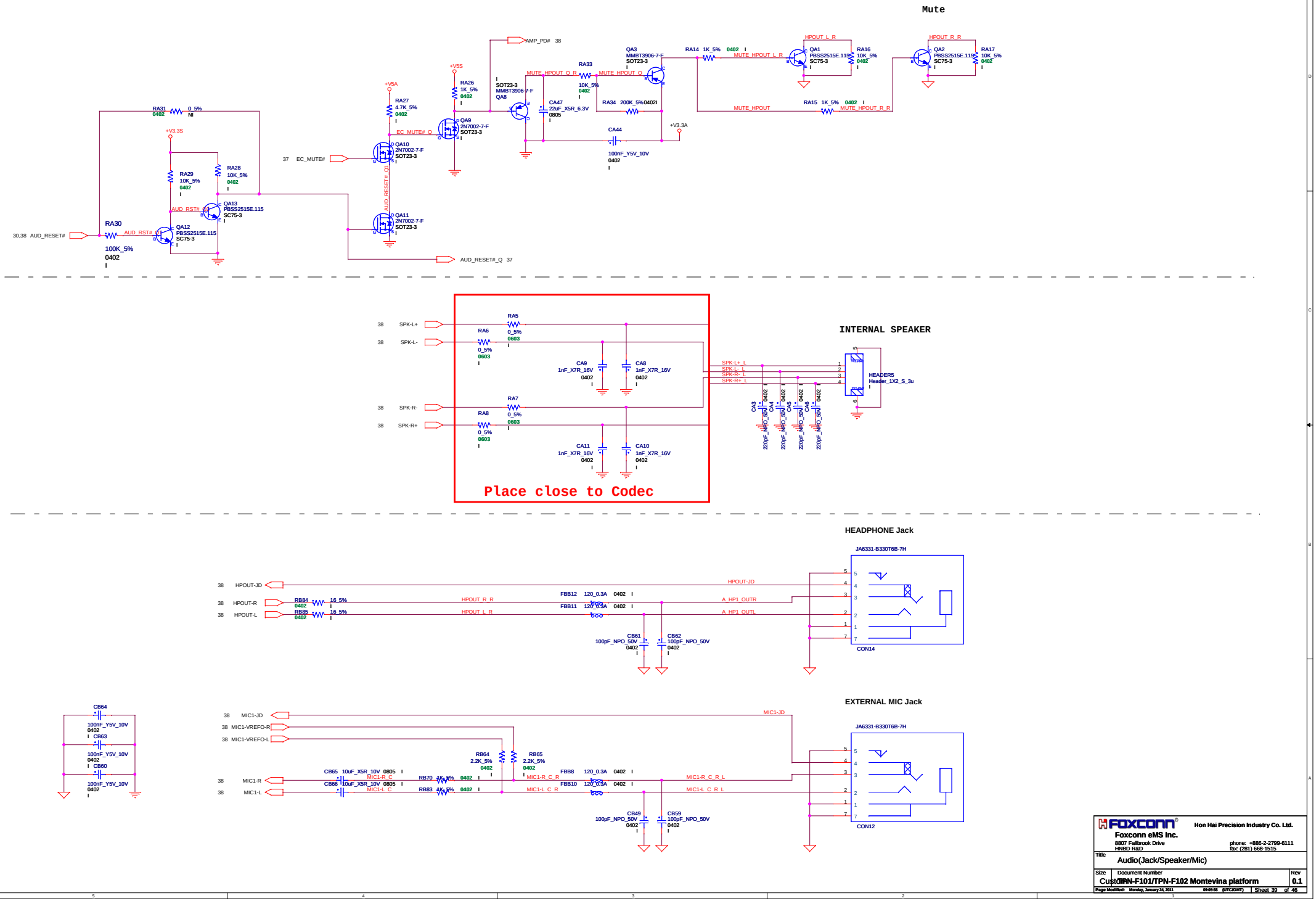


Foxconn eMS Inc.	Hon Hai Precision Industry Co. Ltd.
8807 Fallbrook Drive HNBD R&D	phone: +886-2-2799-6111 fax: (281) 668-1515
Title	Audio(Codec)
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina platform
Rev: 0.1	
Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT)	Sheet 38 of 46


Mute
AMP_PD# 38
HPOUT_L_R
HPOUT_R_R
QA3 MMBT3906-7-F SOT23-3
RA14 1K_5% 0402
QA1 PBSS2515E.115 SC75-3
RA16 10K_5% 0402
QA2 PBSS2515E.115 SC75-3
RA17 10K_5% 0402
MUTE_HPOUT_L_R
MUTE_HPOUT_Q_R
MUTE_HPOUT_Q
RA33 10K_5% 0402
SOT23-3 MMBT3906-7-F QA8
CA47 22uF_X5R_6.3V 0805
RA34 200K_5% 0402
MUTE_HPOUT
RA15 1K_5% 0402
MUTE_HPOUT_R_R
CA44 100nF_Y5V_10V 0402
+V3.3A
+V5S
RA26 1K_5% 0402
QA9 2N7002-7-F SOT23-3
+V5A
RA27 4.7K_5% 0402
EC_MUTE# Q
QA10 2N7002-7-F SOT23-3
37 EC_MUTE#
AUD_RESET# Q
QA11 2N7002-7-F SOT23-3
AUD_RESET#_Q 37
RA31 0_5% NI
+V3.3S
RA29 10K_5% 0402
RA28 10K_5% 0402
AUD_RST#
QA13 PBSS2515E.115 SC75-3
QA12 PBSS2515E.115 SC75-3
RA30 100K_5% 0402
30,38 AUD_RESET#
INTERNAL SPEAKER
38 SPK-L+
38 SPK-L-
38 SPK-R-
38 SPK-R+
RA5 0_5% 0603
RA6 0_5% 0603
RA7 0_5% 0603
RA8 0_5% 0603
CA9 1nF_X7R_16V 0402
CA8 1nF_X7R_16V 0402
CA11 1nF_X7R_16V 0402
CA10 1nF_X7R_16V 0402
Place close to Codec
SPK-L+_L
SPK-L-_L
SPK-R-_L
SPK-R+_L
CA3 220pF_NPO_50V 0402
CA4 220pF_NPO_50V 0402
CA5 220pF_NPO_50V 0402
CA6 220pF_NPO_50V 0402
CA7 220pF_NPO_50V 0402
HEADER5 Header_1X2_S_3u
HEADPHONE Jack
JA6331-B330T6B-7H
38 HPOUT-JD
38 HPOUT-R
38 HPOUT-L
RB84 16_5% 0402
RB85 16_5% 0402
HPOUT_R_R
HPOUT_L_R
FBB12 120_0.3A 0402
FBB11 120_0.3A 0402
HPOUT-JD
A_HP1_OUTR
A_HP1_OUTL
CB61 100pF_NPO_50V 0402
CB62 100pF_NPO_50V 0402
CON14
EXTERNAL MIC Jack
CB64 100nF_Y5V_10V 0402
CB63 100nF_Y5V_10V 0402
CB60 100nF_Y5V_10V 0402
38 MIC1-JD
38 MIC1-VREFO-R
38 MIC1-VREFO-L
38 MIC1-R
38 MIC1-L
CB65 10uF_X5R_10V 0805
CB66 10uF_X5R_10V 0805
MIC1-R_C
MIC1-L_C
RB70 1K_5% 0402
RB83 1K_5% 0402
RB64 2.2K_5% 0402
RB65 2.2K_5% 0402
MIC1-R_C_R
MIC1-L_C_R
FBB8 120_0.3A 0402
FBB10 120_0.3A 0402
MIC1-JD
MIC1-R_C_R_L
MIC1-L_C_R_L
CB49 100pF_NPO_50V 0402
CB59 100pF_NPO_50V 0402
CON12
FOXCONN
Hon Hai Precision Industry Co. Ltd.
Foxconn eMS Inc.
8807 Fallbrook Drive
HNBD R&D
phone: +886-2-2799-6111
fax: (281) 668-1515
Title
Audio(Jack/Speaker/Mic)
Size
Document Number
Custom
TPN-F101/TPN-F102 Montevina platform
Rev
0.1
Page Modified: Monday, January 24, 2011 09:45:38 (UTC/GMT)
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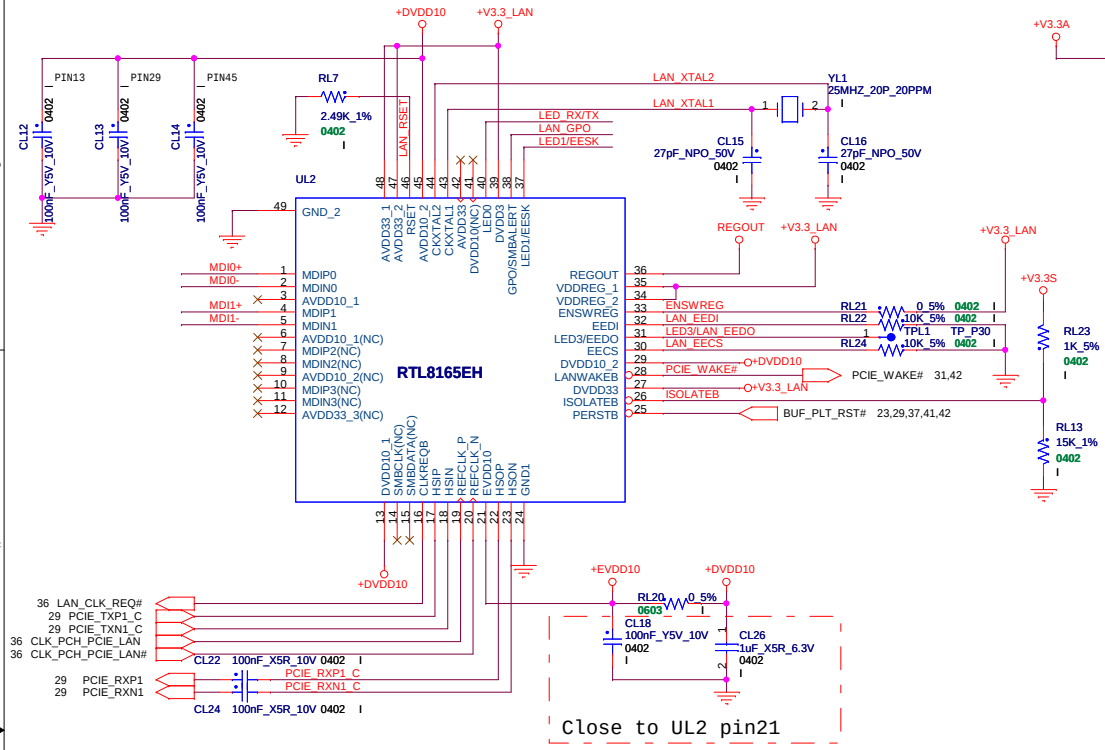
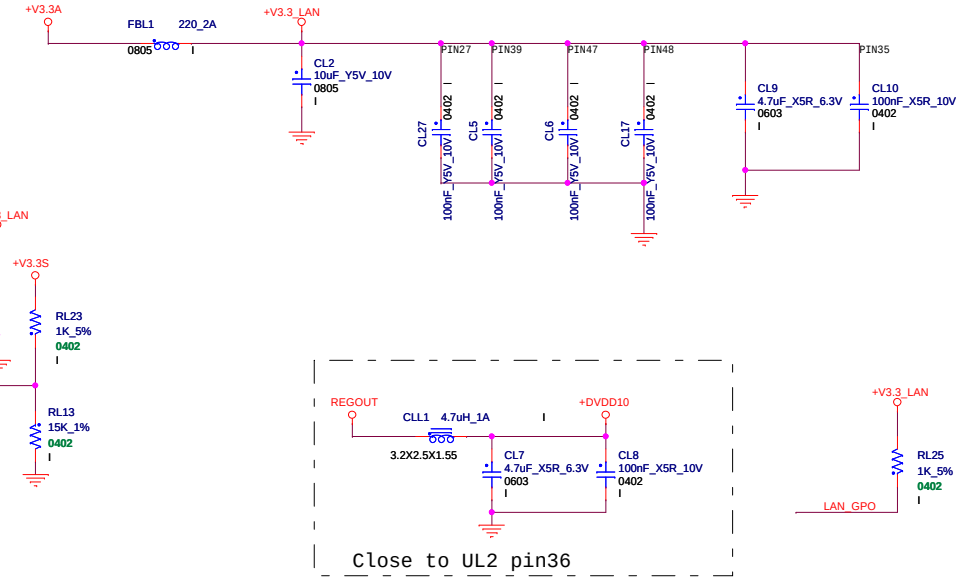
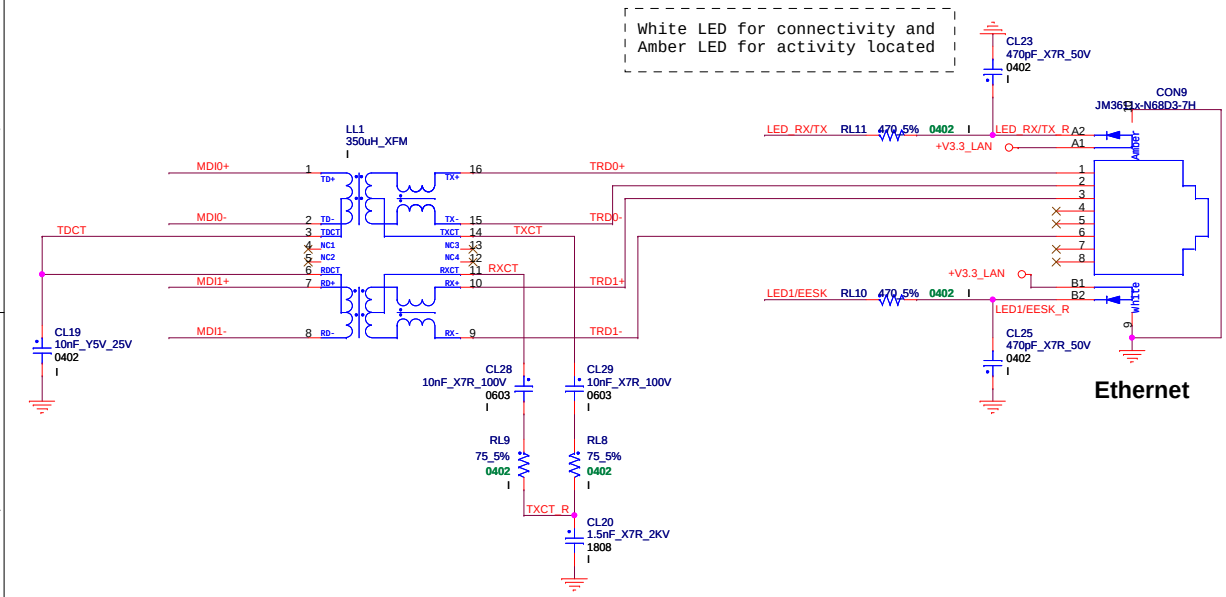


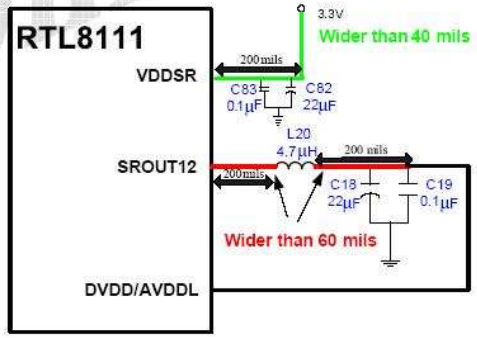




7.1. PCB Layout

- The input 3.3V power trace connected to the VDDSR pin should be wider than 40mils.
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200mils (0.5cm) of the VDDSR pin to prevent input voltage overshoot.
- The output power trace out of the SROUT12 pin should be wider than 60mils.
- Keep L20 within 200mils (0.5cm) of the SROUT12 pin.
- Keep C18 and C19 within 200mils (0.5cm) of L20 to ensure stable output power and better power efficiency.
- Both C18 and C82 are strongly recommended to be ceramic capacitors.

Note: Violation of the above rules will damage the IC.



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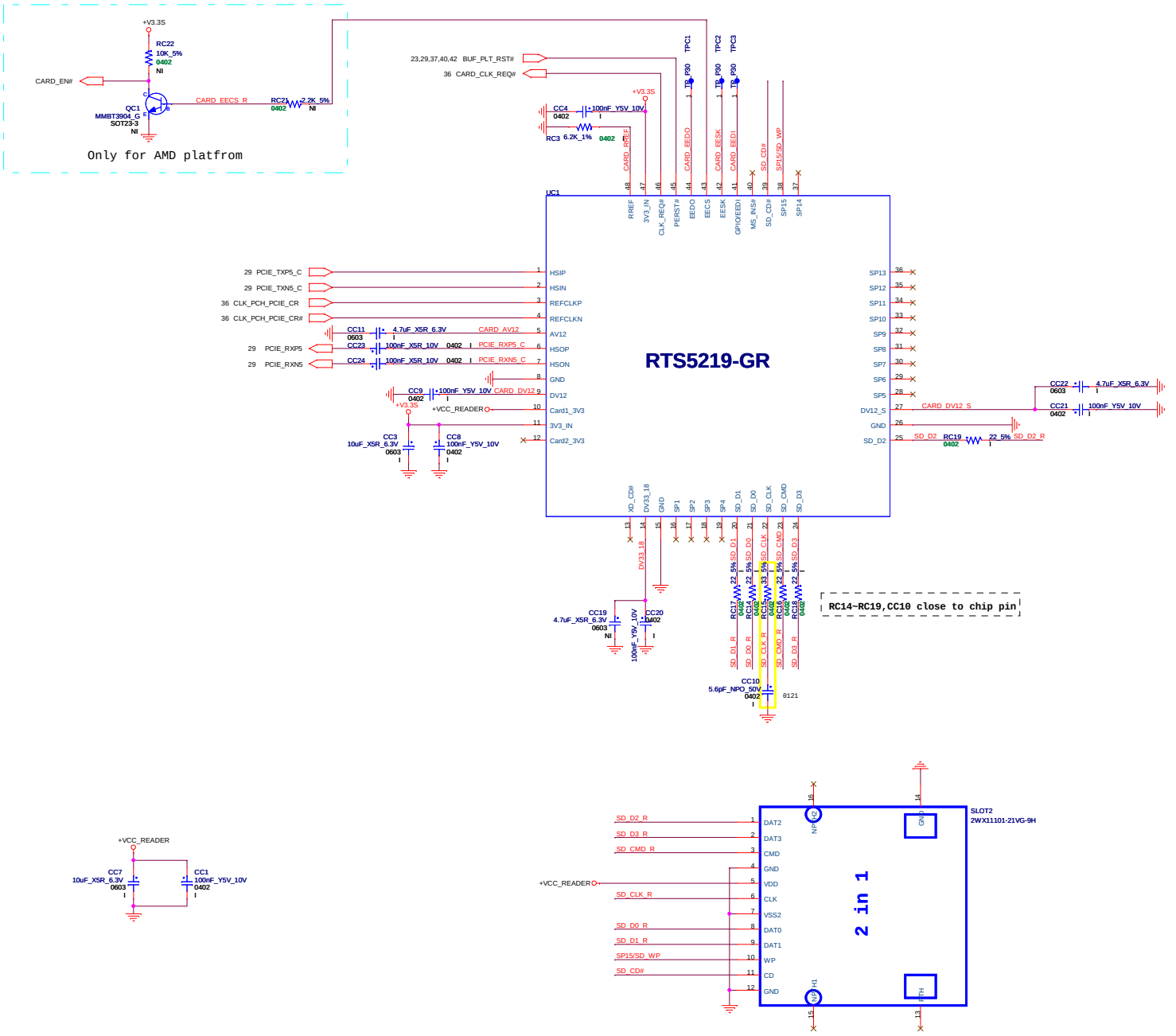
Title: LAN	
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina platform
Rev: 0.1	
Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT)	Sheet 40 of 46



Foxconn	Hon Hai Precision Industry Co. Ltd.
Foxconn eMS Inc.	
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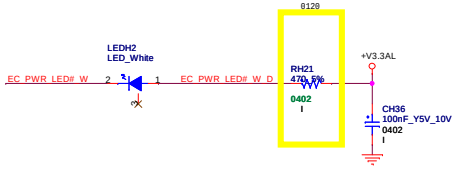
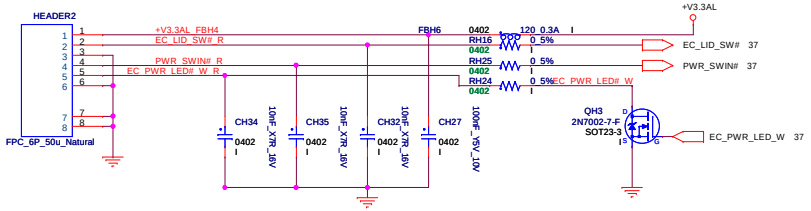
Title	Card Reader
Size	Document Number: Custom TPN-F101/TPN-F102 Montevina platform
Rev	0.1
Page Modified: Monday, January 24, 2011 09:05:39 (UTC/GMT)	Sheet 41 of 46



PWR LED

PWR Board CONN.



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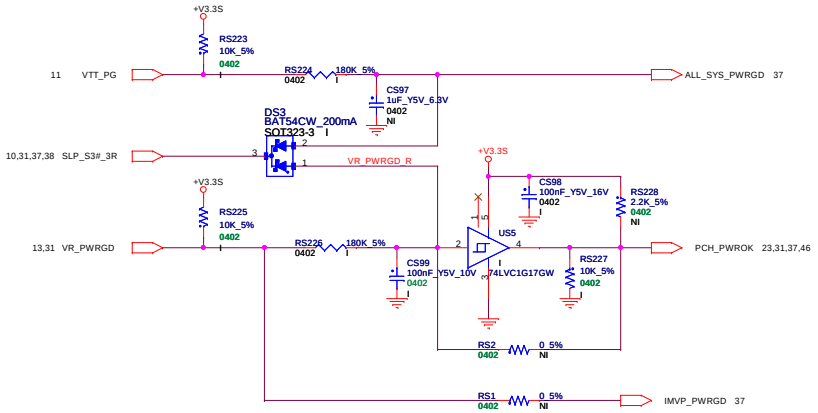
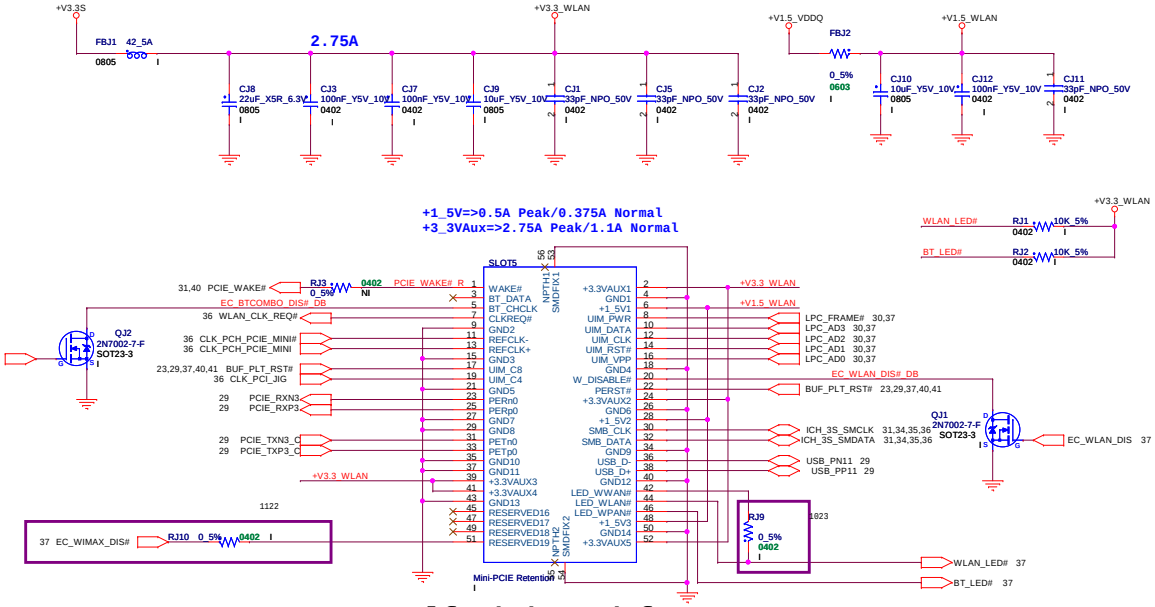
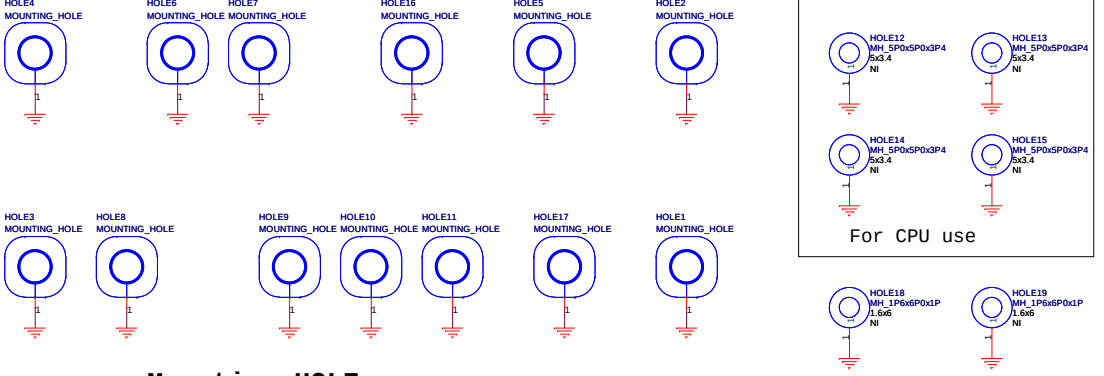
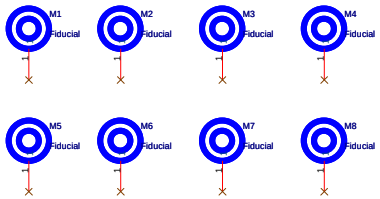




Half Mini Card for WLAN



Mounting HOLE



Fiducial Mark

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Foxconn eMS Inc.
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HNBD R&D
phone: +886-2-2799-6111
fax: (281) 668-1515

Title: Mini PCIE&BT

Size	Document Number	Rev
Custom	TPN-F101/TPN-F102 Montevina platform	0.1

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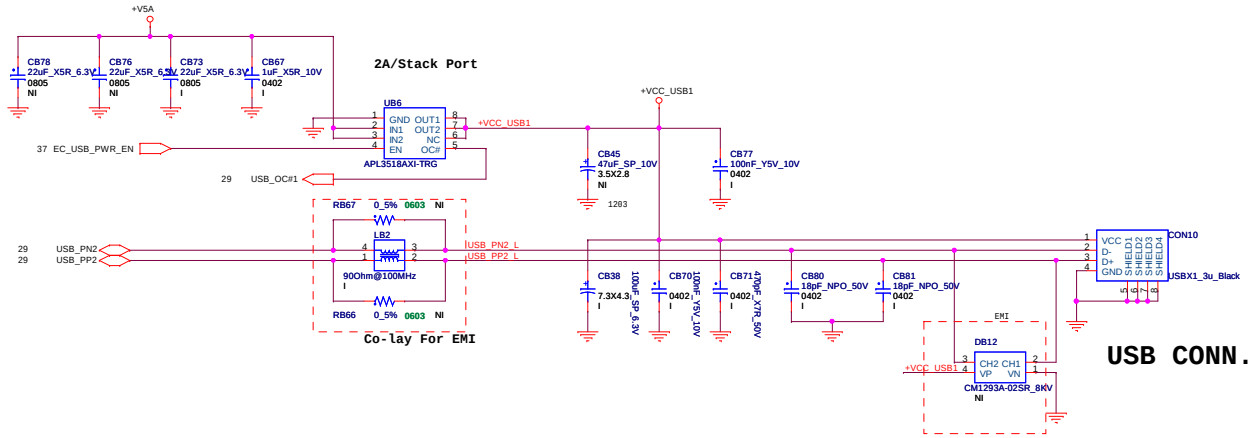

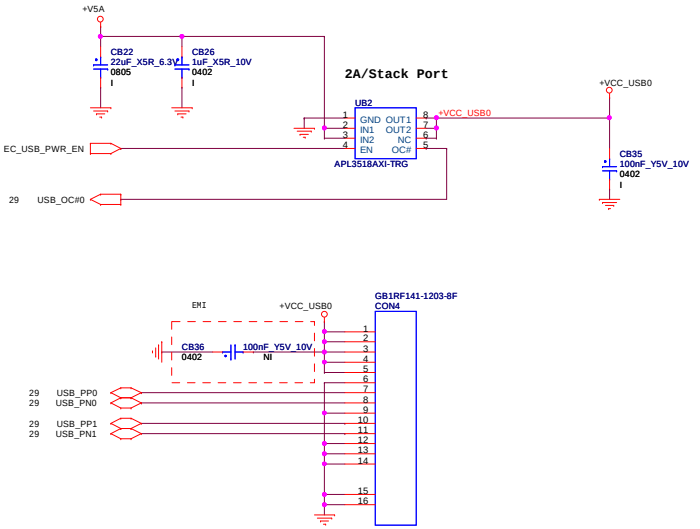

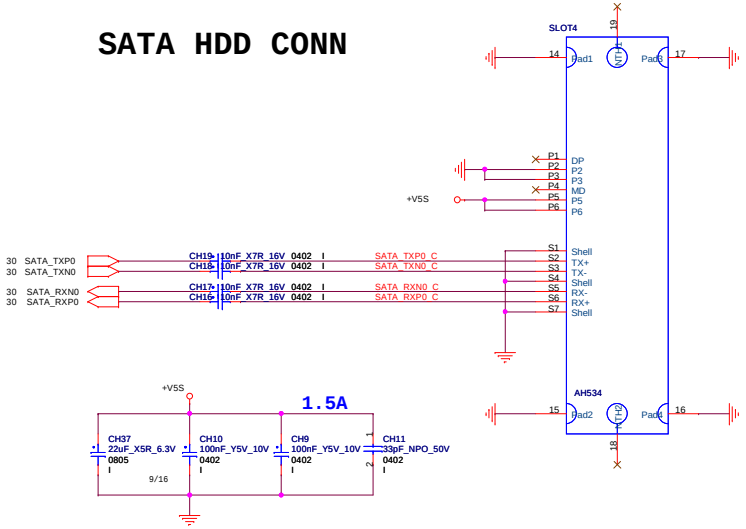

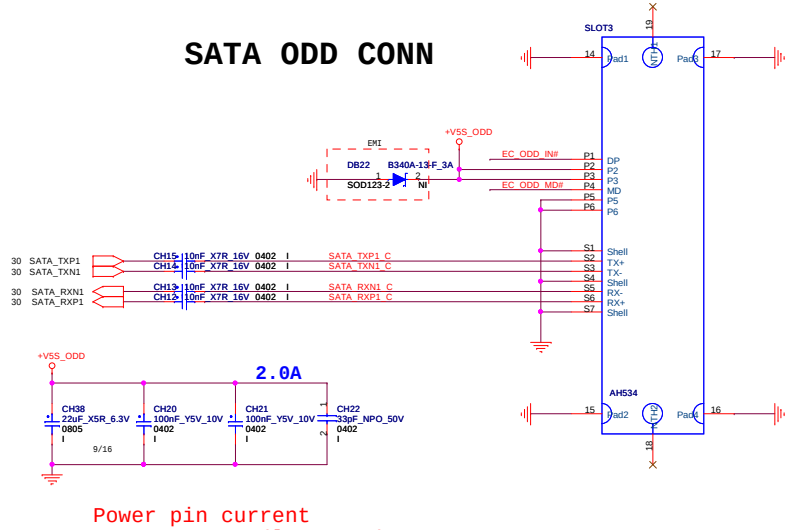

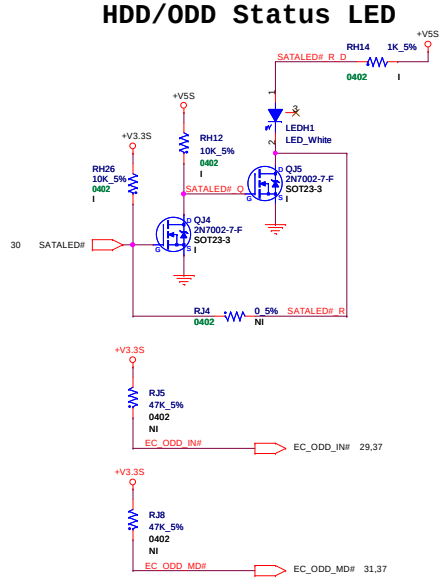

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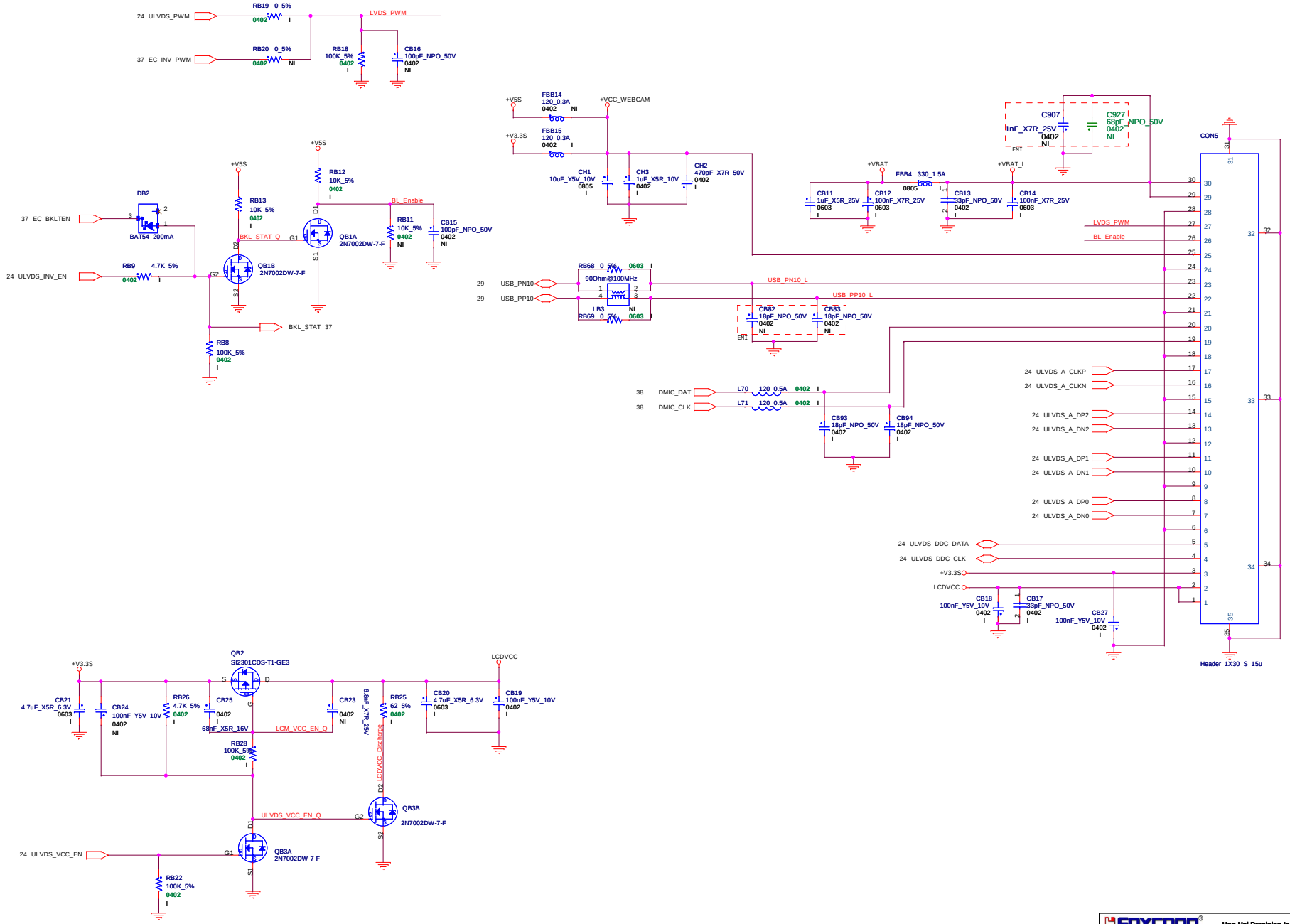
Title: USB/HDD/ODD		
Size	Document Number: Custom TPN-F101/TPN-F102 Montevina platform	Rev: 0.1
Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT)	Sheet 43 of 46	



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8807 Fallbrook Drive	phone: +886-2-2799-6111	
HNBD R&D	fax: (281) 668-1515	
Title: LVDS/Webcam		
Size	Document Number	Rev
Custom	TPN-F101/TPN-F102 Montevina platform	0.1
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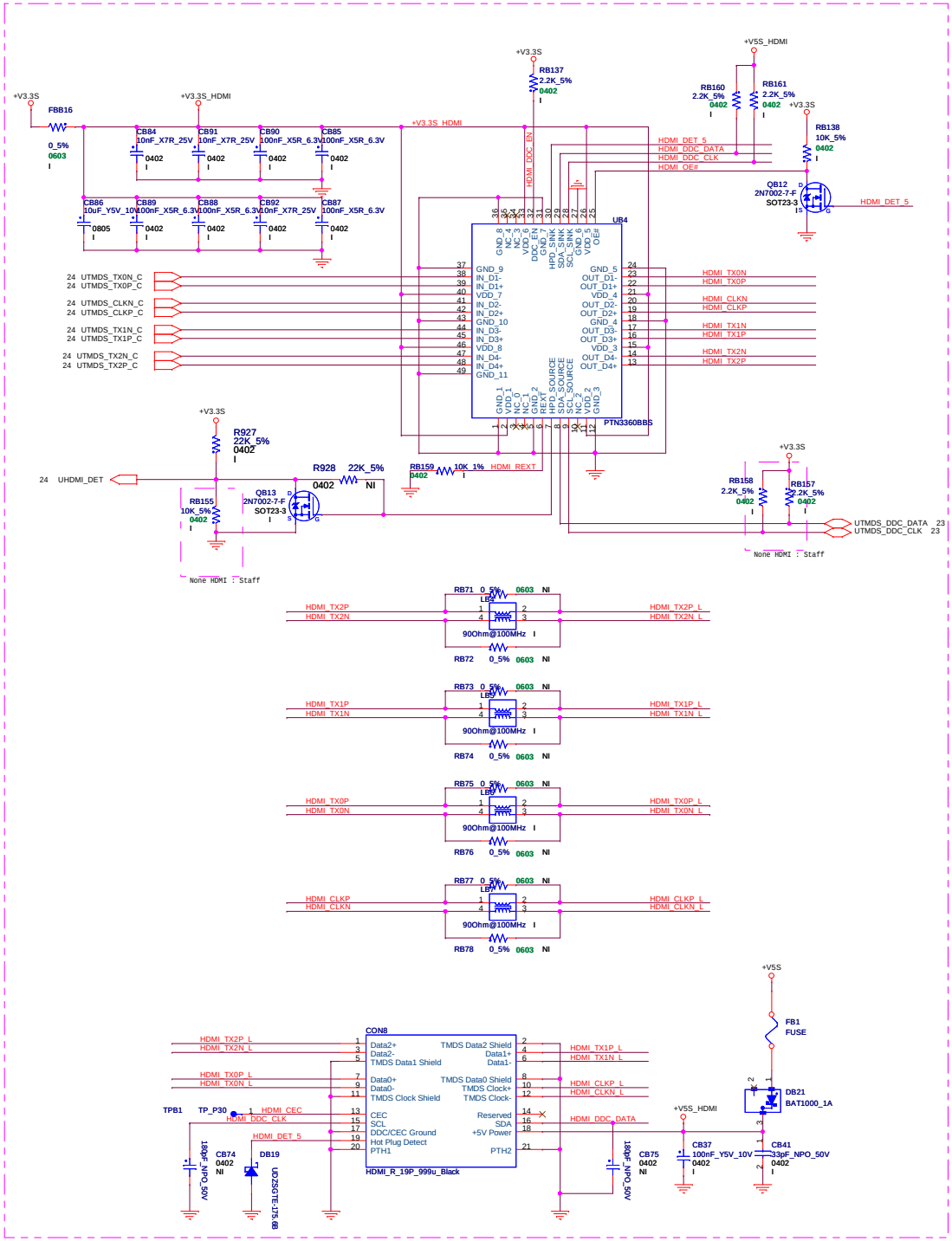
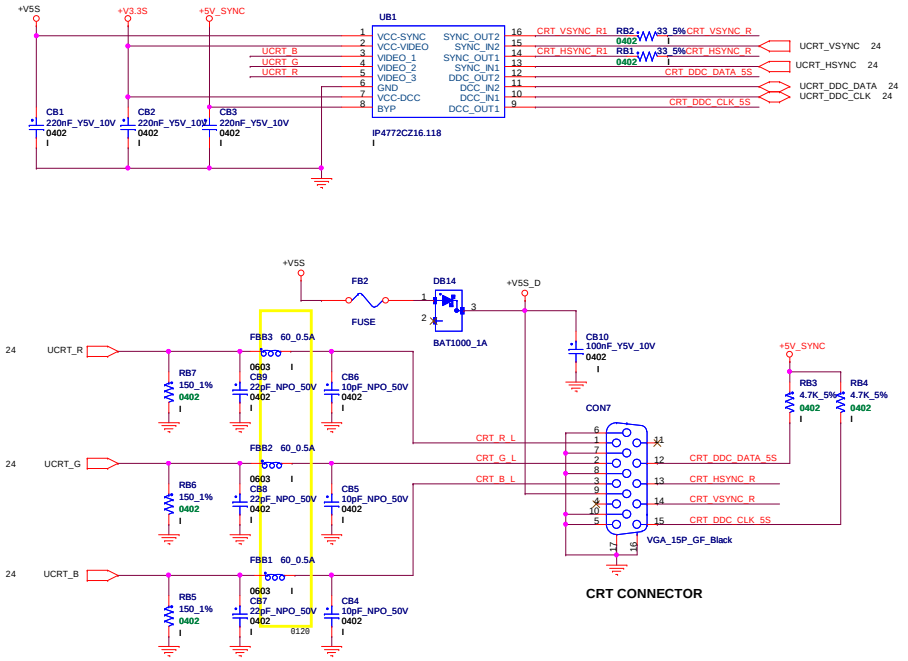


CRT



CRT CONNECTOR

Foxconn eMS Inc. 8807 Fallbrook Drive HNBD R&D	Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111 fax: (281) 668-1515	
Title: HDMI/CRT		
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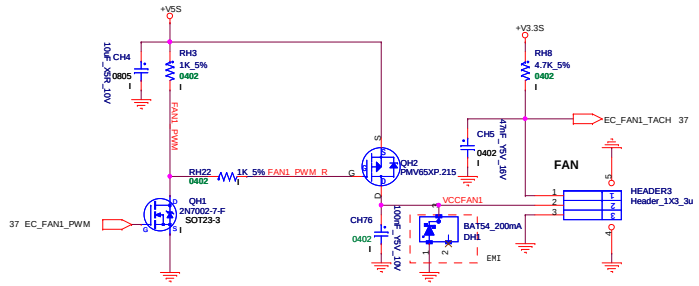
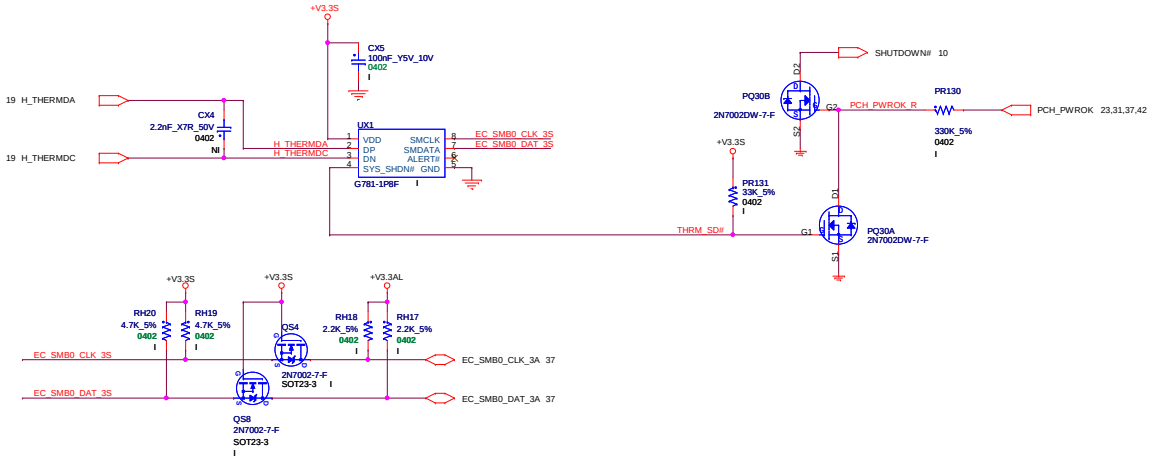
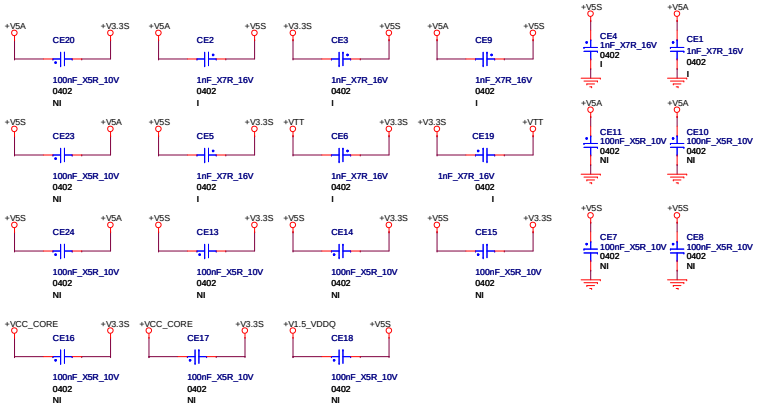
FAN



THERMAL SENSOR



stitch cap



RF Solution

Foxconn eMS Inc.	Hon Hai Precision Industry Co. Ltd.	
8807 Fallbrook Drive HNBD R&D	phone: +886-2-2799-6111 fax: (281) 668-1515	
Title: Thermal/Fan/Control		
Size: Custom	Document Number: TPN-F101/TPN-F102 Montevina platform	Rev: 0.1
Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT)		Sheet 46 of 46