RTS5210

POWER

- AC/BATT CONNECTOR
- BATT CHARGER
- CPU CORE
- 5V/ 3.3VSTBY
- 1.5V/ 0.75_VTT_DDR
- 1.1VS
- 1.05VS
- 1.8VS LDO
- 2.5VS LDO
- 1.1VSTBY_SB LDO
- DGPU VCORE
- SUS/ RUN PWR Switch

Page 39 ~ 47

EMI/ Moat CAP Page 48

History Page 49, 50

DDR3-SODIMM Page 5 — DDR III 1066/ 1333MHZ

DDR3-SODIMM Page 6 — DDR III 1066/1333MHZ

Dual/ Single Core CPU
AMD
Danube
Dual:35W Page 2, 3, 4

1066 MHz HT

VRAM Page 22, 23

64MX16
HYNIX: HPMH-14-00D0000040G
SAMSUNG: HPMH-14-00D0000042G
128MX16:
Hynix: HPMH-14-00D0000039G
Samsung: HPMH-14-00D0000043G

DGPU with Muxless
ATI
Seymour/ Whistler
15.6"/17.3" Muxless Hybrid:
Seymour 64bit 15W + DDR3 x4
Whistler 128bit 25W + DDR3 x8
M2 package 29 x 29 FCBGA962
Seymour XT:
HPMH-10-0020000049G
Whistler Pro:
HPMH-10-0020000050G
Page 15, 16, 17, 18, 19, 20, 21

PCIE 8X

Side-Port 128M Page 9

North Bridge
ATI
RS880M
HPMH-10-0010000096G
Page 7, 8, 9, 10

HDMI — **HDMI Conn** Page 25

CRT — **D-sub Conn** Page 26

Cable/ 2ch LVDS — **LVDS + Touch**
LVDS 15"/17": 2 ch HD+ 1600x900
2 ch FHD 1920x1080
Page 24

USB2.0 x 1

Page 27

HDD Conn 2nd for 17.3" only — Cable

HDD Conn — Cable

ODD Conn Zero Power ODD Intel Saving 100 ~ 160mW — Cable

SATA 3: 6Gbps

SATA 2: 3Gbps

PCI-E

A-link (PCIE x 4)

PCI-E x 1 — **Cardreader** Realtek RTS5209 Page 31 — **BToB Conn** — **2 in 1 Slot** 1) SD/SDHC/SDXC 2) MMC (17.3": daughter Board)

PCI-E x 1 — **USB3.0** TI **TUSB7320** Page 33 — USB2.0/ 3.0 — USB2.0 — **USB2.0/3.0 cnn** Wake Up; **USB2.0/3.0 cnn** Wake Up Page 34

PCI-E x 1 / USB2.0 x 1 — **WLAN Half MINI-CARD** Page 30

USB2.0 x 2 — **Conn** Cable — **USB Conn** Wake Up; **USB Conn** Wake Up; **Standby LED** White blink; **HDD LED** Dual LED White: Normal , Amber: Park (15.6"/17.3" x2 daughter board)

USB2.0

Int. CLK

South Bridge
AMD
SB820M
HPMH-10-0010000106G
Page 11, 12, 13, 14

WebCam Conn White LED: Enable Sensor OVT 9726 Dual DMic Page 28 — Cable

Fingerprint Validaty Module VFM5131 Dual LED x1: White normal, Amber not reconized Page 28 — Cable

SATA

USB2.0

SPI BIOS — SPI

G SENSOR ST Micro HP3DC Page 27

RTC Cell Conn — Cable

25M **32.768K** Crystal

LPC

HDA

PCI-E x 1 — **Realtek Gb LAN** RTL8111E-VB-GR W/ASPM Page 32 — No cable: NIC auto disabled. — **Magnetic** — **RJ45** LED White x1 for connectivity, Amber x1 for activity

15.6"/17.3" daughter board — Cable embeded — **TouchPad LED daughter board** — **Conn**

Dual LED White: AC in Amber: Charging — **Charge LED**

SPI 512KB 25

Module board — **HP Logo LED Module** — **Conn** — Cable embeded

Crystal Free **32.768K**

SIO
ITE
ITE8518
Page 29

Lid Switch Page 28

Thermal Page 30

FAN Conn Page 30 — Cable embeded

Cable — **Keyboard Conn** Page 29 — KB with: White LEDx1: Cap lock, Amber LEDx1:Mute, White/Amber dual LEDx1: wireless, NumLock LED x1: 17" only

Cable — **Touchpad Conn** Page 28 — Amber LED x1: Amber: T/P off On/Off by tapping LED

Conn — **PWR Button / White LEDx1** Blink White: Standby; **Quick Web Button / LED x1** — 15.6"/17.3" daughter board

AUDIO CODEC
IDT
92HD80TA
Page 35, 36, 37

LDO TPS793475DBVR

SPK AMP TPA3113D2 — **Internal Speaker Conn x4 speakers**

Correct should be: TI TPA2012 — **Internal DMic Conn To Webcam**

Microphone x1

HP AMP TPA6130A2 — **Headphone Microphone Combo Conn x2**

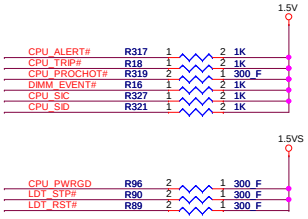
Woofer AMP TPA3111D1 — **WOOFER CONN** for 17.3" only

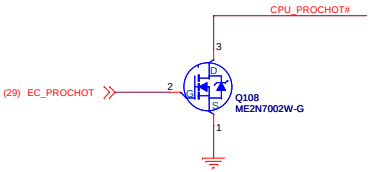
FLEXComputing

Project Name: H510UA1	Title: Block Diagram	
Size:	Document Number: HPMH-40GAB6300-D	Rev: D
Date: Thursday, December 30, 2010	Sheet: 1 of 51	

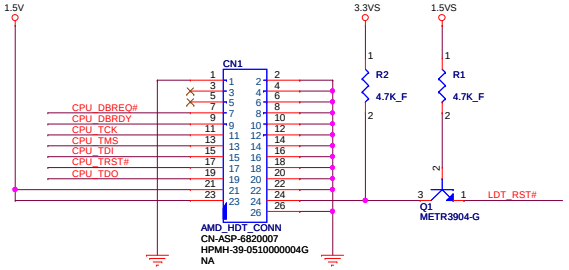
AMD Debug Termination

Signal Name	Type	Connection	Termination	Voltage
TEST6 TEST7 TEST8		Remain unconnected	-	
TEST9	I	Tie to VSS	-	VSS
TEST10		S1g2: Leave unconnected S1g3: Pulled up to VLDT (0603 DNI)		
TEST12		Test point access required for scan function. Connection to scan header preferred but not required.	1 K Ω to VSS No pop	VSS
TEST14 TEST15 TEST16 TEST17		Test point access required, header is preferred	-	-
TEST18,		Test point access required for scan function. Connection to scan header preferred but not required.	1 K Ω to VSS No pop	VSS
TEST19			1 K Ω to VSS No pop	VSS
TEST20			300 Ω[6]	VSS
TEST21			300 Ω[6]	VSS
TEST22			1 K Ω to VSS No pop	VSS
TEST23			300 Ω[6]	VSS
TEST24	I	Test point access required for scan function. Connection to scan header preferred but not required.	300 Ω[6]	VSS
TEST25_H			510 Ω[6]	VSS
TEST25_L			510 Ω[6]	VDDIO
TEST27 TEST28_H TEST28_L TEST29_H TEST29_L		Need test point on board	-	-

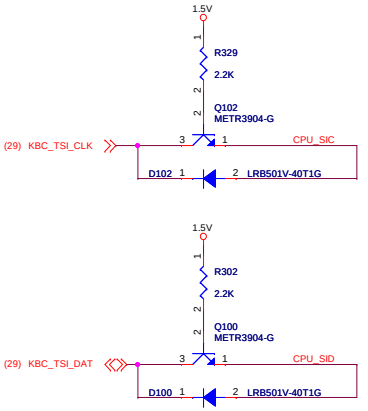


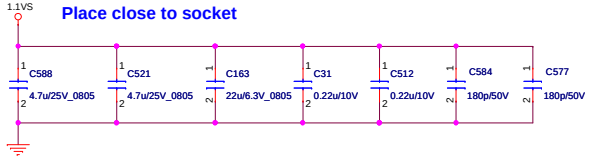


HDT Header

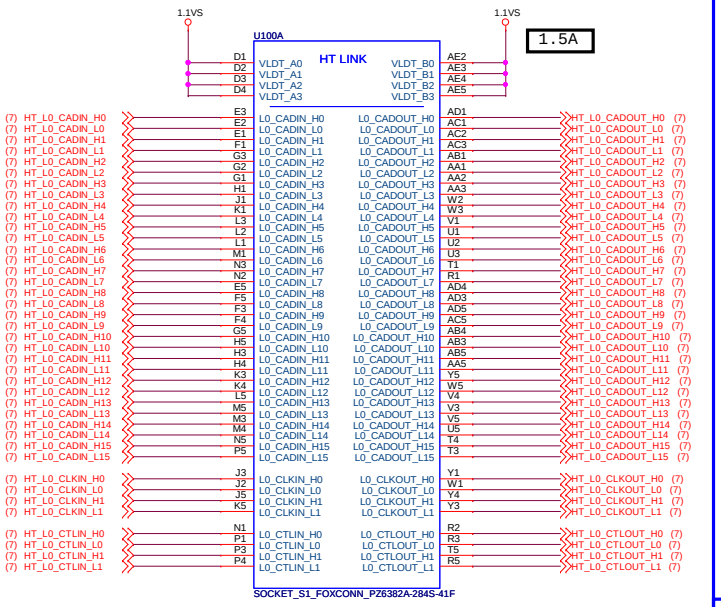


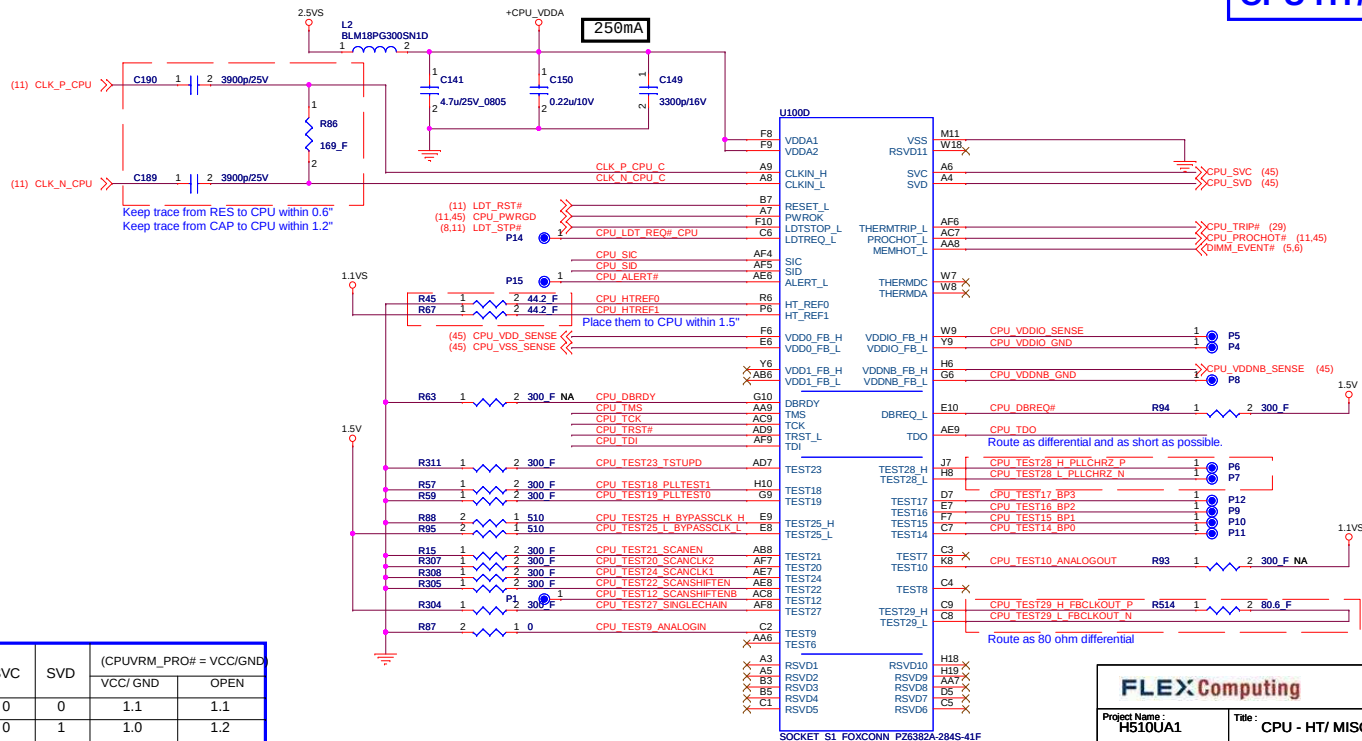
TSI Function





CPU HT/ MISC



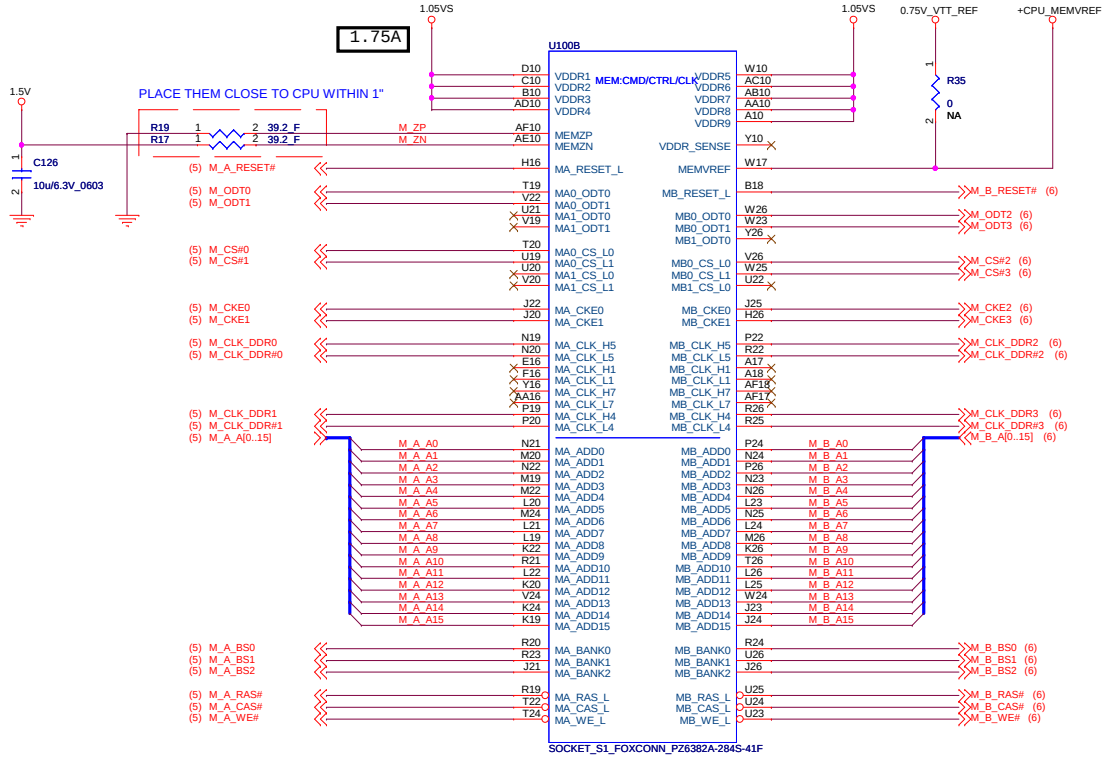


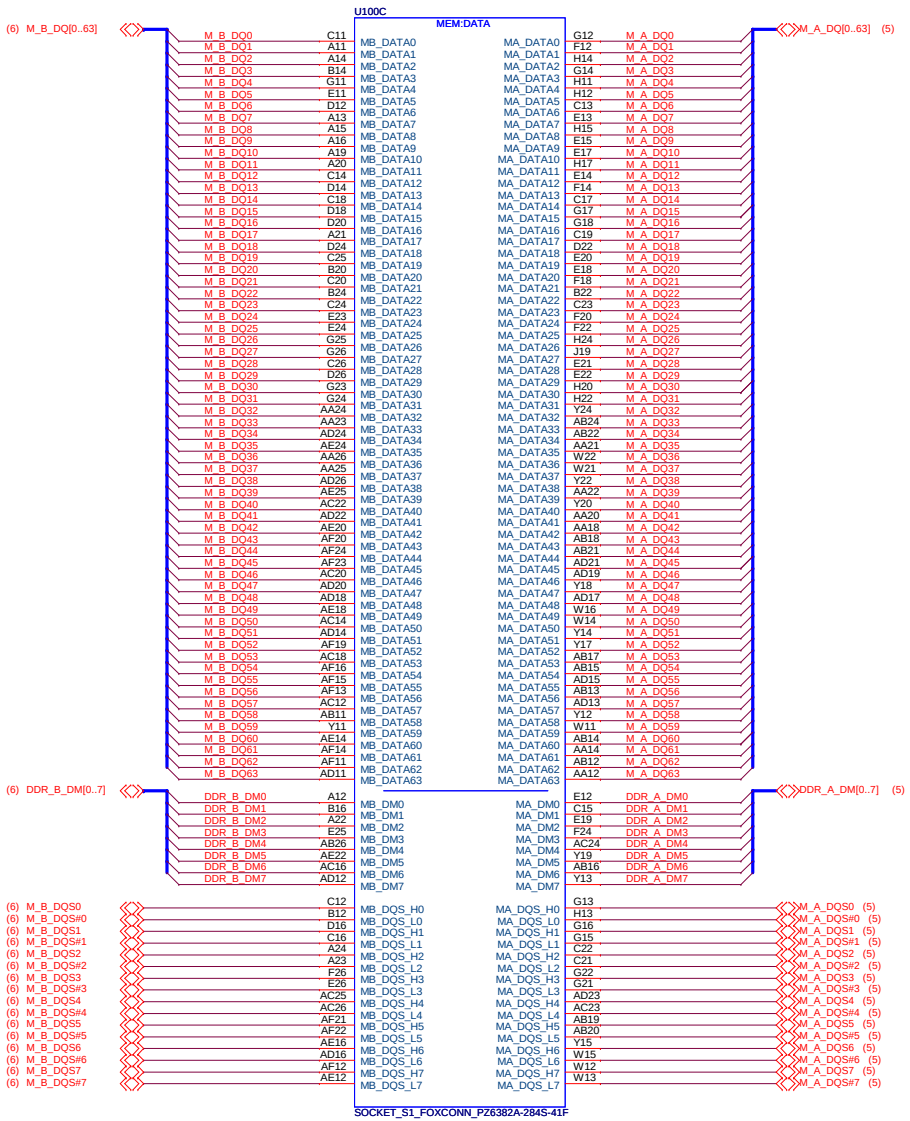
SVC	SVD	(CPUVRM_PRO# = VCC/GND)	
		VCC/ GND	OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

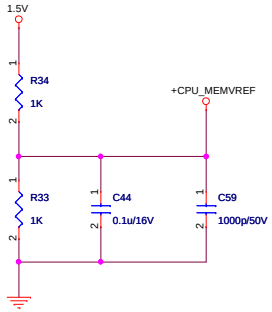
FLEX Computing

Project Name : H510UA1	Title : CPU - HT/ MISC I/F
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 2 of 51

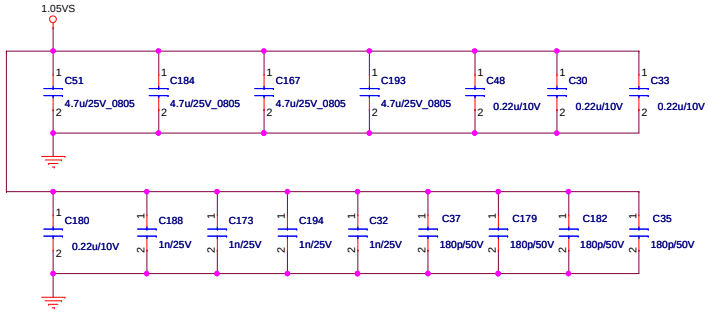
CPU Memory





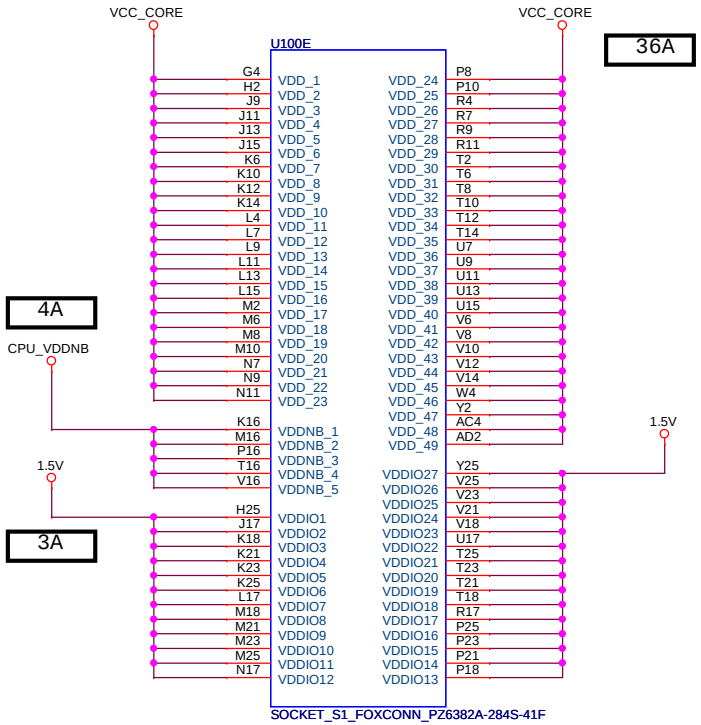


Place close to socket

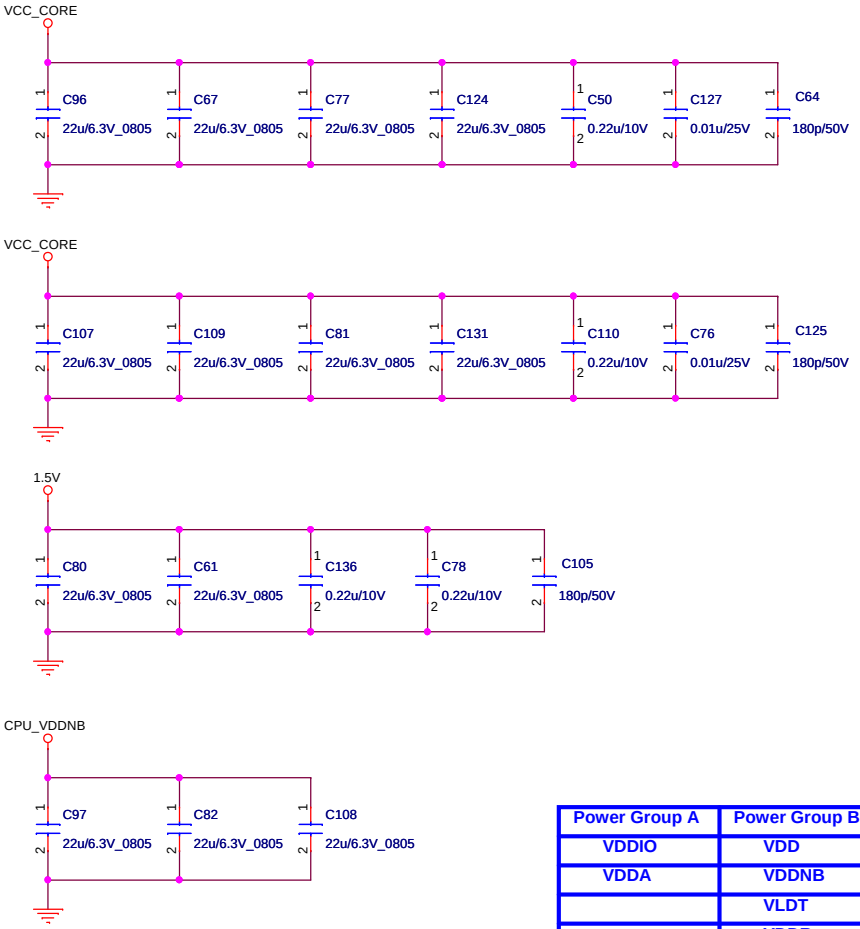


FLEX Computing	
Project Name : H510UA1	Title : CPU - MEM I/F
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 3 of 51

CPU PWR

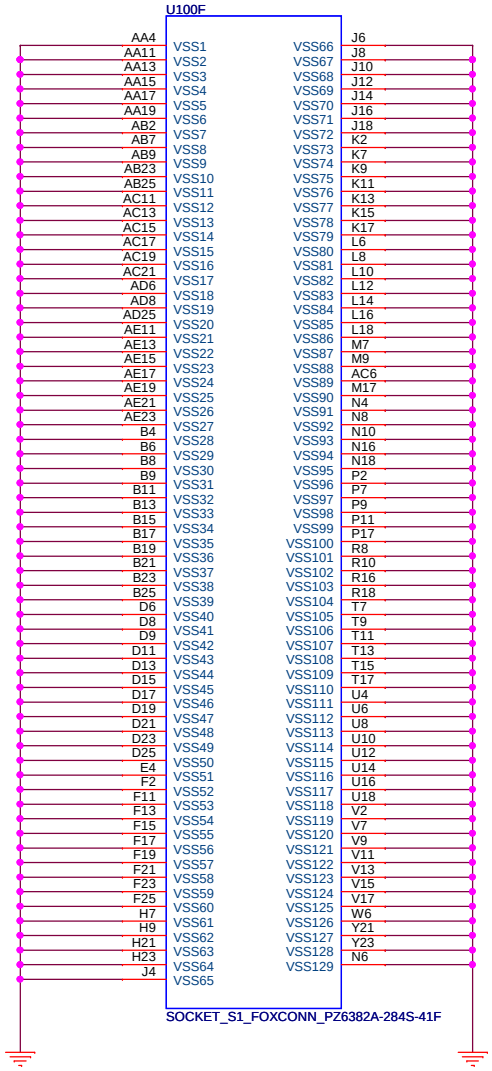


BOTTOM SIDE DECOUPLING

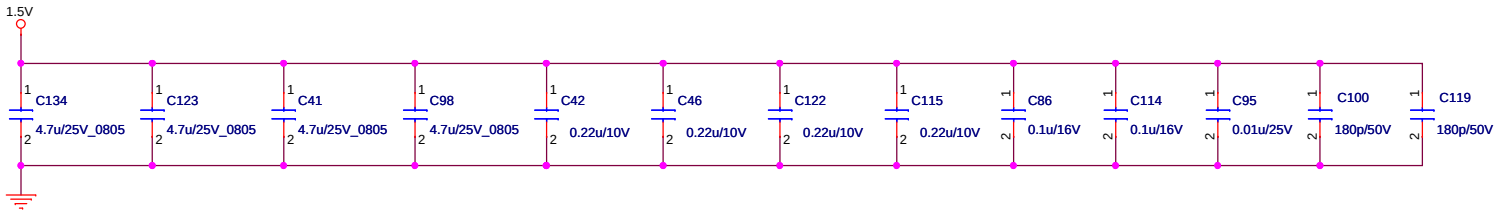


Power Group A	Power Group B
VDDIO	VDD
VDDA	VDDNB
	VLDT
	VDDR

CPU GND



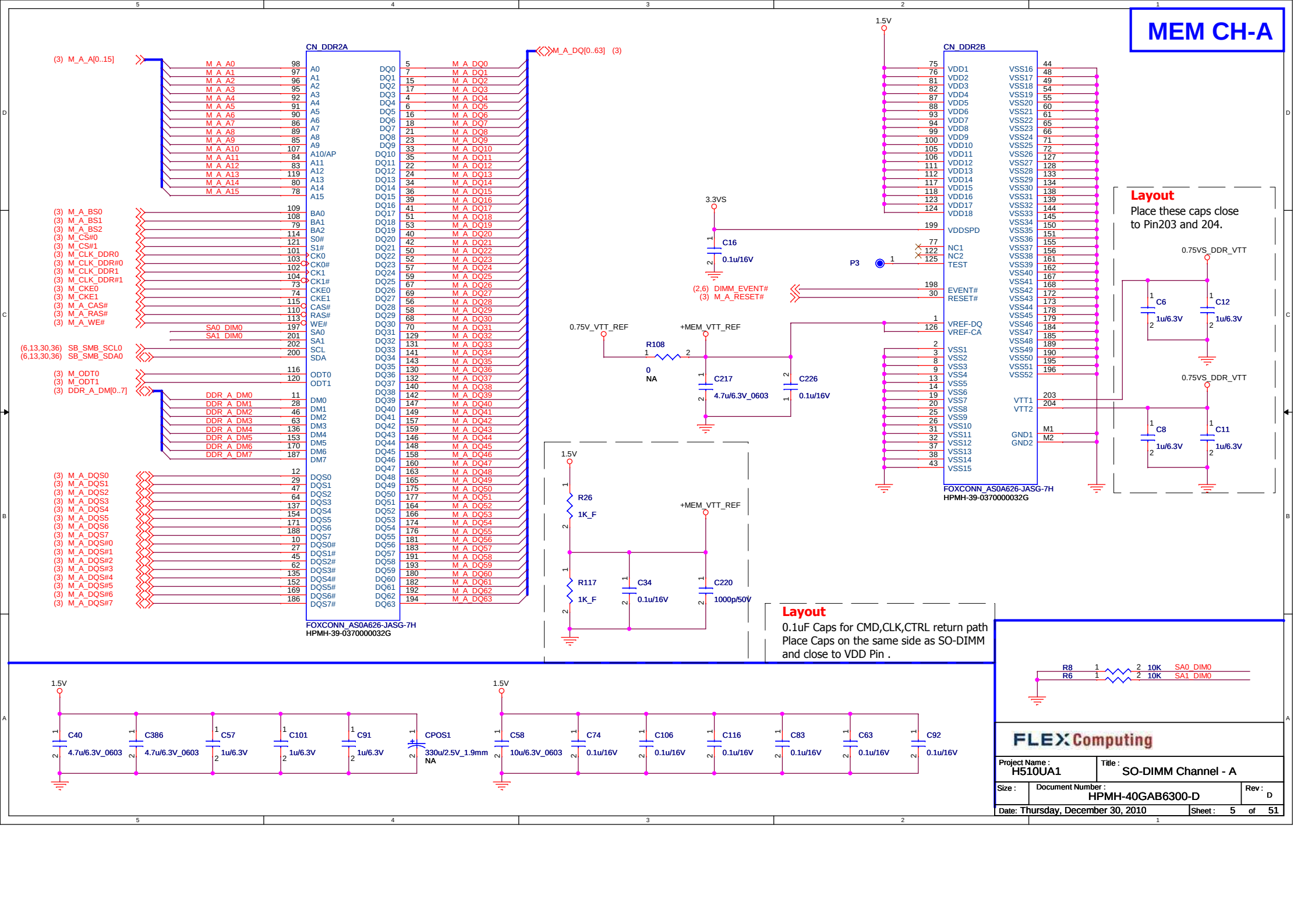
DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



FLEXComputing

Project Name : H510UA1	Title : CPU - PWR/ GND	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 4 of 51	

MEM CH-A



Layout

Place these caps close to Pin203 and 204.

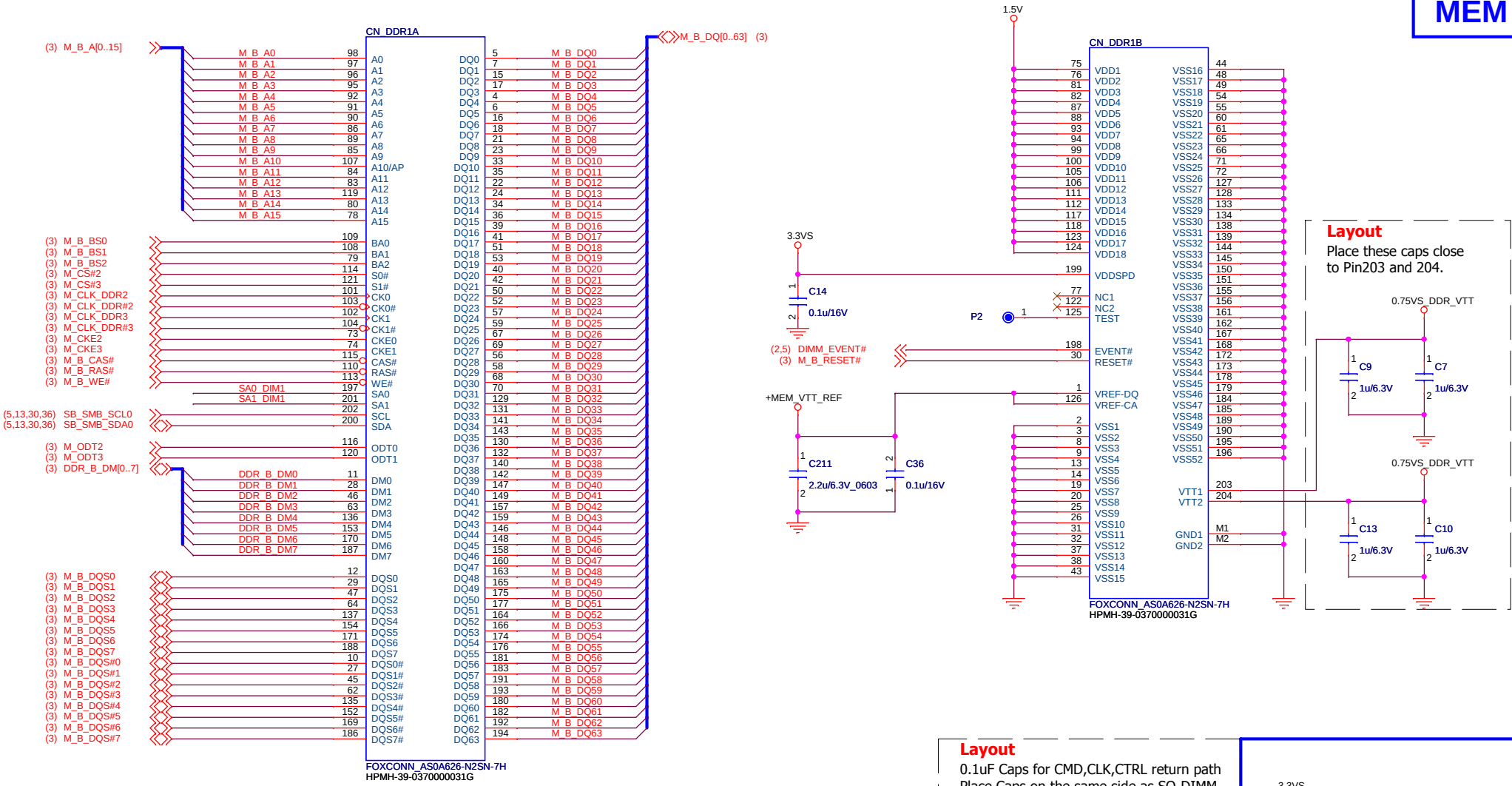
Layout

0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM and close to VDD Pin .

FLEXComputing

Project Name : H510UA1	Title : SO-DIMM Channel - A
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Thursday, December 30, 2010	Sheet : 5 of 51

MEM CH-B

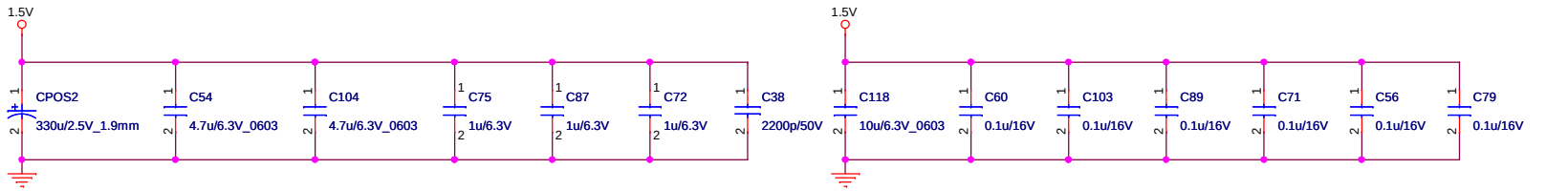


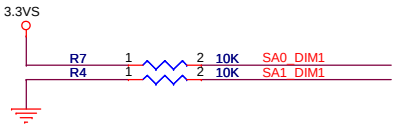
Layout

Place these caps close to Pin203 and 204.

Layout

0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM and close to VDD Pin .



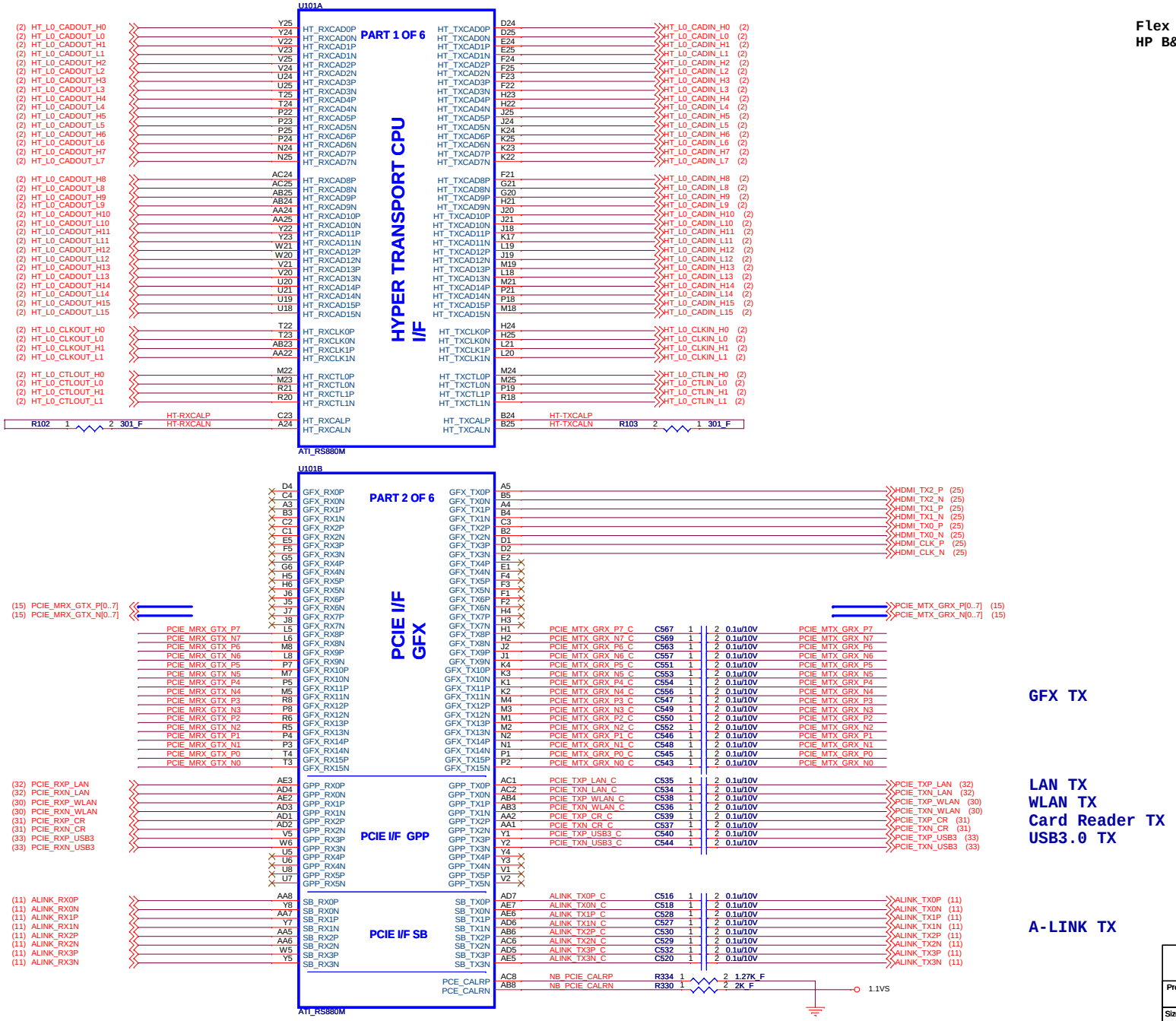


FLEXComputing

Project Name : H510UA1	Title : SO-DIMM Channel - B
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Thursday, December 30, 2010	Sheet : 6 of 51

NB HT/ PCIE

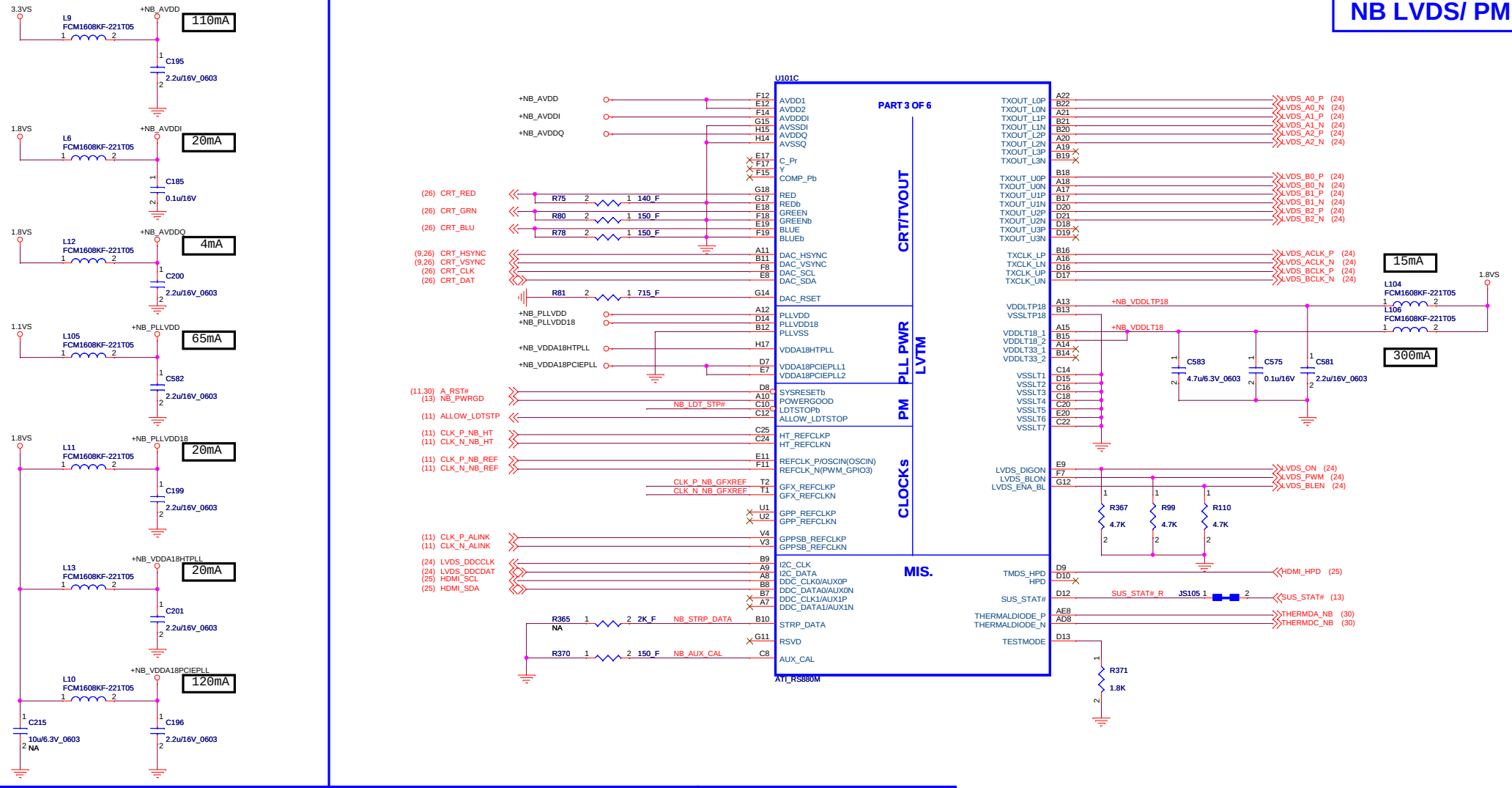
Flex P/N: HPMH-10-0010000096G
HP B&S P/N: HPMJ-534109-001 (UMA)
HPMJ-604096-001 (DGPU)

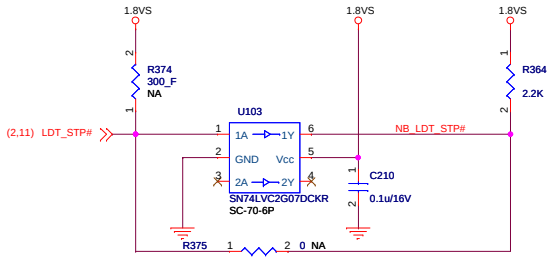


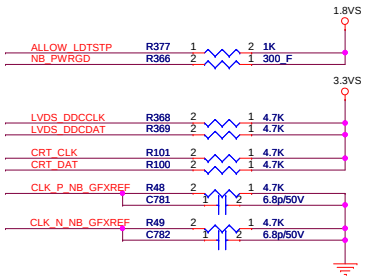
Project Name : H510UA1	Title : RS880M - HT/ PCI-E I/F
Size :	Document Number : HPMH-40GAB6300-D
Rev : D	
Date: Thursday, December 30, 2010	Sheet : 7 of 51

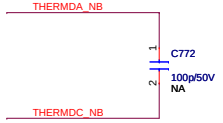
FLEX Computing

NB LVDS/ PM





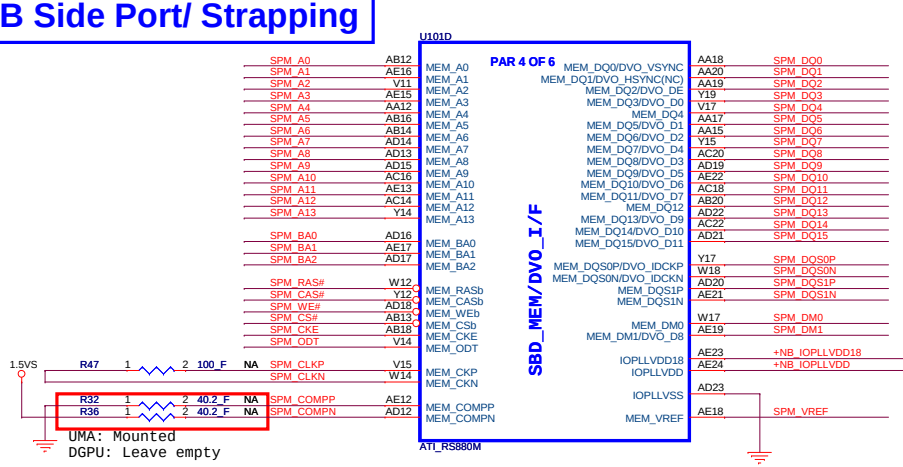


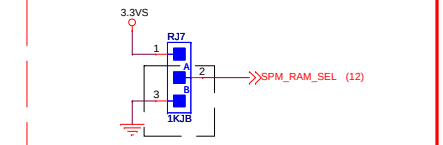


FLEX Computing

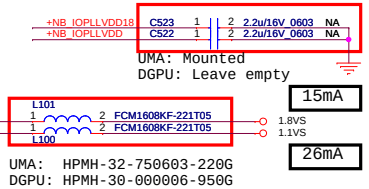
Project Name : H510UA1	Title : RS880M - LVDS/ PM I/F
Size :	Document Number : HPMH-40GAB6300-D
Rev : D	
Date: Thursday, December 30, 2010	Sheet : 8 of 51

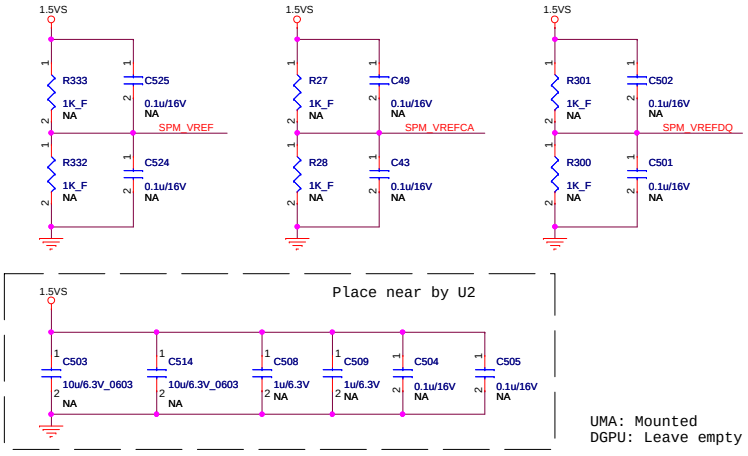
NB Side Port/ Strapping





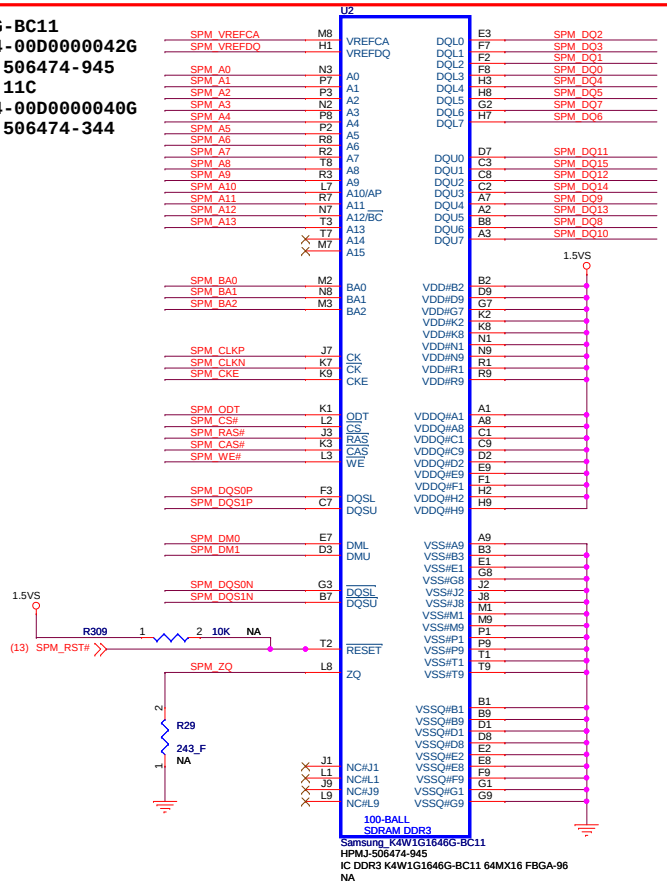
Low (1Komh): H5TQ1G63DFR-11C (HYNIX)
HPMH-14-00D0000040G
High (10Kohm): K4W1G1646G-BC11 (SAMSUNG)
HPMH-14-00D0000042G





Samsung/ K4W1G1646G-BC11
Flex P/N: HPMH-14-00D0000042G
HP B&S P/N: HPMJ-506474-945
Hynix/ H5TQ1G63DFR-11C
Flex P/N: HPMH-14-00D0000040G
HP B&S P/N: HPMJ-506474-344

UMA: Mounted
DGPU: Leave empty

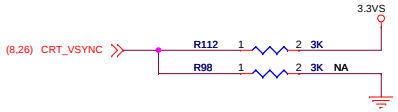


RS880M H/W STRAPS

The strap values are latched into internal registers after the assertion of the POWERGOOD signal to the RS880M

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
DAC_VSYNC (RS880.Pin B11)
1 = Disable (default)
0 = Ensable

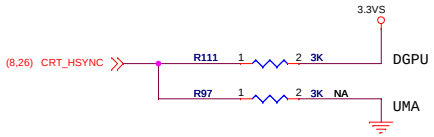


DFT_GPIO1: LOAD_EEPROM_STRAPS

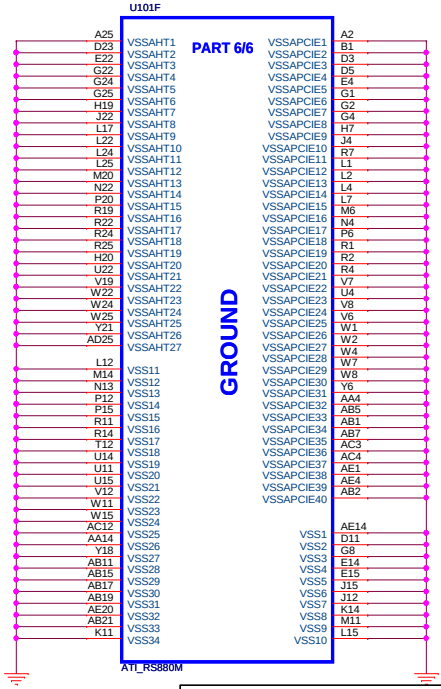
Selects Loading of STRAPS from EPROM.
SUS_STAT# (RS880.Pin D12)
1 = Bypass the loading of EEPROM straps and use Hardware Default Values
0 = I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880: Enable Side Port Memory

Selects if Memory SIDE PORT is available or not
DAC_HSYNC (RS880.Pin A11)
1 : Disable (default)
0 : Enable
Register Readback of strap:
NB_CLKCFG:CLK_TOP_SPARE_D[1]



NB GND



FLEX Computing

Project Name : H510UA1	Title : RS880M - Side Port/ Strap/ GND
Size :	Document Number : HPMH-40GAB6300-D
Rev : D	
Date: Thursday, December 30, 2010	Sheet : 9 of 51

NB PWR

RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.1V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

600mA

1.1VS — C169 4.7u/6.3V_0603 — C166 0.1u/16V — C160 0.1u/16V — C85 0.1u/16V

700mA

1.1VS — C176 4.7u/6.3V_0603 — C121 0.1u/16V — C137 0.1u/16V — C580 0.1u/16V

400mA

1.1VS — C132 4.7u/6.3V_0603 — C143 0.1u/16V — C117 0.1u/16V — C579 0.1u/16V — C154 0.1u/16V

700mA

+NB_VDDA18PCIE — C133 4.7u/6.3V_0603 — C113 4.7u/6.3V_0603 — C139 0.1u/16V — C88 0.1u/16V — C99 0.1u/16V — C112 0.1u/16V

10mA + 25mA

1.8VS — C526 1u/6.3V

RJ4 0JB — +NB_VDD18_MEM

A& Mounted for UMA
B& NA for DGPU

C84 1u/6.3V NA

1.8VS — L1 QT2012RL220HC3A-LF — +NB_VDDA18PCIE

U101E — PART 5/6 — POWER — ATI_RS880M

J17	VDDHT_1	A6	VDDPCIE_1
K16	VDDHT_2	B6	VDDPCIE_2
L16	VDDHT_3	C6	VDDPCIE_3
M16	VDDHT_4	D6	VDDPCIE_4
P16	VDDHT_5	E6	VDDPCIE_5
R16	VDDHT_6	F6	VDDPCIE_6
T16	VDDHT_7	G7	VDDPCIE_7
		H8	VDDPCIE_8
H18	VDDHTRX_1	J9	VDDPCIE_9
G19	VDDHTRX_2	K9	VDDPCIE_10
F20	VDDHTRX_3	M9	VDDPCIE_11
E21	VDDHTRX_4	L9	VDDPCIE_12
D22	VDDHTRX_5	P9	VDDPCIE_13
B23	VDDHTRX_6	R9	VDDPCIE_14
A23	VDDHTRX_7	T9	VDDPCIE_15
		V9	VDDPCIE_16
AE25	VDDHTTX_1	U9	VDDPCIE_17
AD24	VDDHTTX_2		
AC23	VDDHTTX_3	K12	VDDC_1
AB22	VDDHTTX_4	J14	VDDC_2
AA21	VDDHTTX_5	U16	VDDC_3
Y20	VDDHTTX_6	J11	VDDC_4
W19	VDDHTTX_7	K15	VDDC_5
V18	VDDHTTX_8	M12	VDDC_6
U17	VDDHTTX_9	L14	VDDC_7
T17	VDDHTTX_10	L11	VDDC_8
R17	VDDHTTX_11	M13	VDDC_9
P17	VDDHTTX_12	M15	VDDC_10
M17	VDDHTTX_13	N12	VDDC_11
		N14	VDDC_12
J10	VDDA18PCIE_1	P11	VDDC_13
P10	VDDA18PCIE_2	P13	VDDC_14
K10	VDDA18PCIE_3	P14	VDDC_15
M10	VDDA18PCIE_4	R12	VDDC_16
L10	VDDA18PCIE_5	R15	VDDC_17
W9	VDDA18PCIE_6	T11	VDDC_18
H9	VDDA18PCIE_7	T15	VDDC_19
T10	VDDA18PCIE_8	U12	VDDC_20
R10	VDDA18PCIE_9	T14	VDDC_21
Y9	VDDA18PCIE_10	J16	VDDC_22
AA9	VDDA18PCIE_11		
AB9	VDDA18PCIE_12	AE10	VDD_MEM1
AD9	VDDA18PCIE_13	AA11	VDD_MEM2
AE9	VDDA18PCIE_14	Y11	VDD_MEM3
U10	VDDA18PCIE_15	AD10	VDD_MEM4
		AB10	VDD_MEM5
F9	VDD18_1	AC10	VDD_MEM6
G9	VDD18_2		
AE11	VDD18_MEM1	H11	VDD33_1
AD11	VDD18_MEM2	H12	VDD33_2

2.5A

1.1VS — C578 0.1u/16V — C120 0.1u/16V — C111 1u/6.3V — C151 1u/6.3V — C135 4.7u/6.3V_0603

12A

1.1VS — C183 0.1u/16V — C68 0.1u/16V — C140 0.1u/16V — C93 0.1u/16V — C147 0.1u/16V — C144 0.1u/16V — C102 0.1u/16V — C69 10u/6.3V_0603 — C162 10u/6.3V_0603

Mounte for UMA
Leave empty for DGPU

+NB_VDD_MEM — C517 0.1u/16V NA — C73 0.1u/16V NA — C513 1u/6.3V NA — C62 1u/6.3V NA — C531 10u/6.3V_0603 NA — C519 10u/6.3V_0603 NA

100mA

1.5VS — RJ3 0_0603JB

A for UMA
B for DGPU

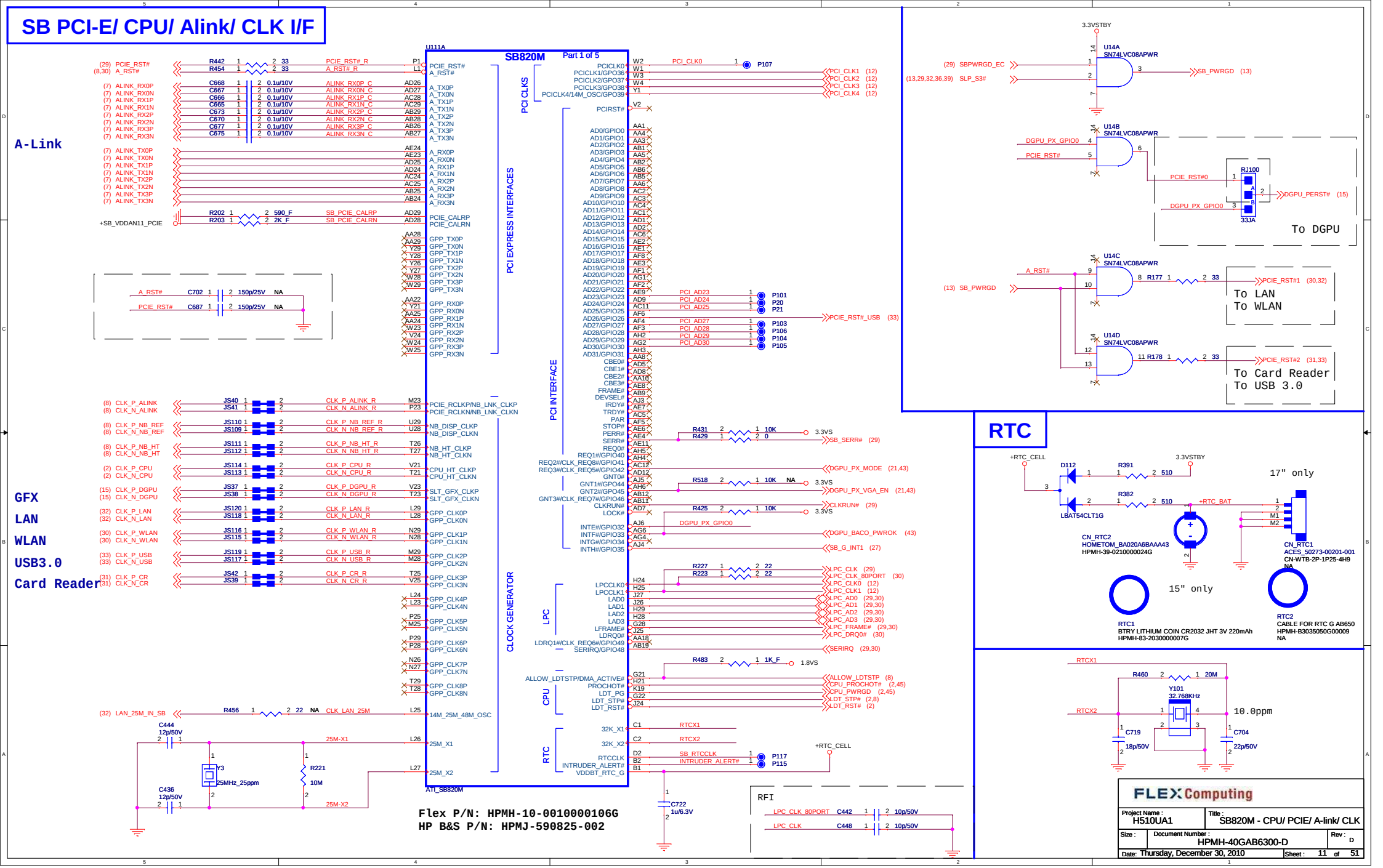
60mA

3.3VS — C213 0.1u/16V — C161 0.1u/16V

FLEXComputing

Project Name : H510UA1	Title : RS880M - PWR		
Size :	Document Number : HPMH-40GAB6300-D	Rev : D	
Date: Thursday, December 30, 2010	Sheet : 10 of 51		

SB PCI-E/ CPU/ Alink/ CLK I/F



SB820M Debug Straps

PciPllByp (PCI AD27)

Bypass PCI PLL
(Used in funcitonal test at tester):

L: Bypass internal PLL clock
H: Use internal PLL generated PLL CLK (Internal Pull-Up of 15Kohm)

ILAAutorunEnB (PCI AD26)

ILA Auto run Enable

L: ILA Auto run enable
H: ILA Auto run disable (Internal Pull-Up of 15Kohm)

FCClkByP (PCI AD25)

Bypass FC CLK

L: Bypass internal FC CLK (Used in funcitonal test at tester)
H: Use internal FC CLK

I2CROMEn (PCI AD24)

I2C ROM Enable. Load the setting for A-Link Express/ PLL/ music control from I2C ROM

L: Getting the value from I2C EPROM
H: Disable I2C ROM
(Internal Pull-Up of 15Kohm)

PCI_ROM_BOOT (PCI AD23)

Booting from PCI memory

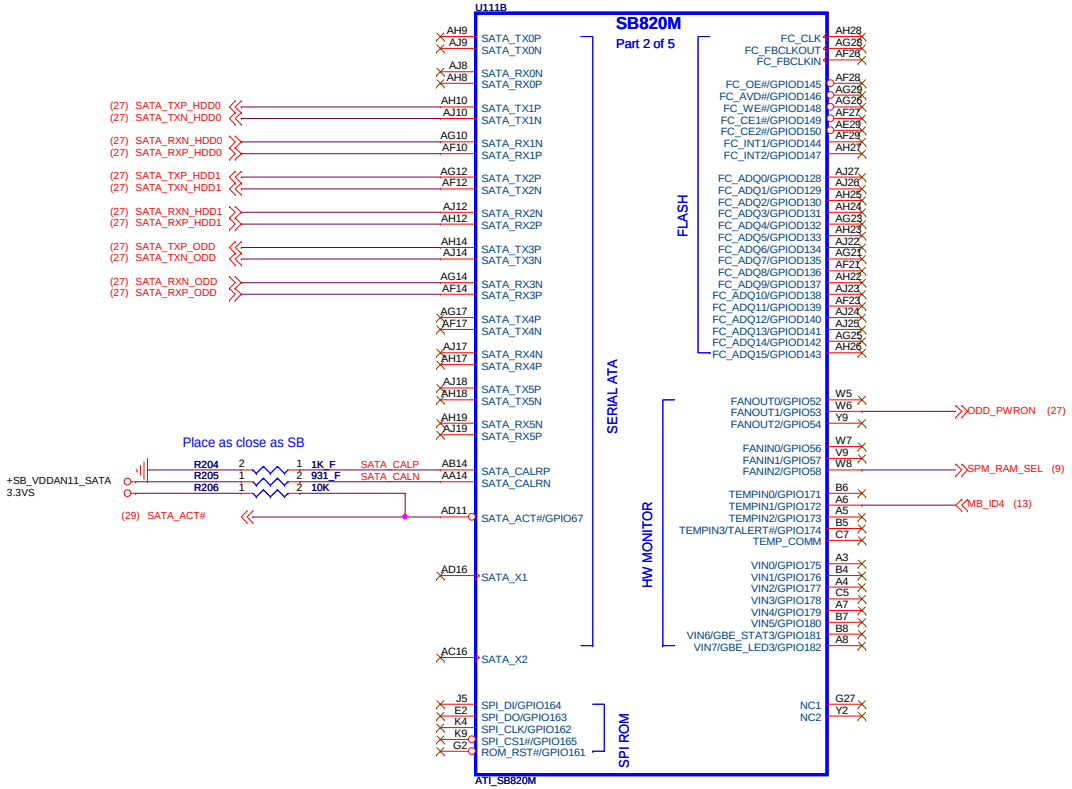
L: Route ROM fetch tp PCI bus on the very first boot. Use ROMTYPE to determine the ROM type on the subsequent boots.
H: Use ROMTYPE straps to determine the ROM type
(Internal Pull-Up of 15Kohm)

PCIe EEPROM Data/ Clock (PCI_REQ3/ PCI_GNT3)

PCIe EEPROM Data/ Clock

Connected to PCIe EEPROM SDA/ SCL pin or provided test point access for lad use.

SB SATA/ SPI/ STRAP



SB820M H/W STRAPS

Type I are captured on RSMRST#
Type II are captured on PWRGD.

ECEnableStrap (LPCCLK0)

Embedded Controller (EC):

L: Disable
H: Enable

(11) LPC_CLK0 R222 10K

CLKGEN (LPCCLK1)

Define Clock Generator:

L: External clock mode
H: Internal clock mode

3.3VSTBY_SB
(11) LPC_CLK1 R226 10K

ROMTYPE_1&0 (EC_PWM3& EC_PWM2)

ROMTYPE_1 EC_PWM3	ROMTYPE_0 EC_PWM2	ROM type
0	0	FWH
0	1	LPC& PMC ROM
1	0	SPI
1	1	Reserve

Default Pull-High Pull-Low --> 2.2Kohm

Reserved for Pull-Low selection.

(13) SB_EC_PWM3 R478 2.2K
(13) SB_EC_PWM2 R225 2.2K NA

BIF_GEN2_COMPLIANCE_Strap (PCI CLK1)

Set PCIe to Gen II mode:

SB820M: Omly provision for Pull down is required, not install by default.

(11) PCI_CLK1 R437 10K NA

BootFailTmrEn (PCI CLK2)

Watchdog function:

L: Disable BootFailtmr function
H: Enable BootFailtmr function

(11) PCI_CLK2 R436 10K

DefaulStrapMode (PCI CLK3)

Default Debug Straps:

L: Disable Debug Straps
H: Select external Debug Straps

(11) PCI_CLK3 R432 10K

CPUClkSel (PCI CLK4)

CPU/ NB HT Clock Selection:

L: Reserved
H: Required setting for integrated clock mode

3.3VS
(11) PCI_CLK4 R434 10K

PCB0
PCB
HPMH-41-AB6300-D00G

CoreSpeedMode (AZ_SDOUT)

Slow down core clock for low power mobile platform:

L: Performance Mode
H: Low Power Mode

(13) HDA_SDATA_OUT_R R447 10K

HDMI0
HDMI
HPMH-B2995007G00001

BIOS0
BIOS
HPMH-B2685310G00016

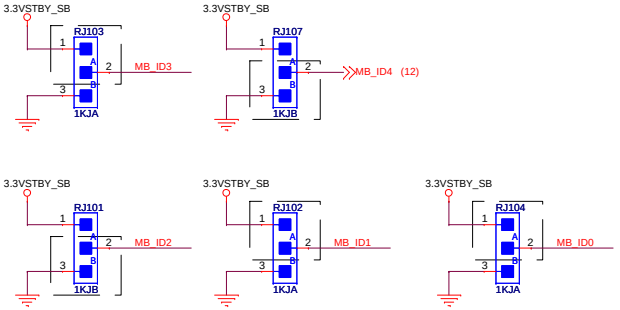
Type I : LPCCLK0, EC_PWM3& EC_PWM2
Type II : the rest of strapping

FLEX Computing

Project Name : H510UA1	Title : SB820M - SATA/ SPI/ Strap
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 12 of 51

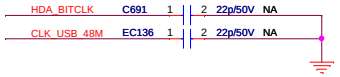
SB ACPI/ USB/ HDA

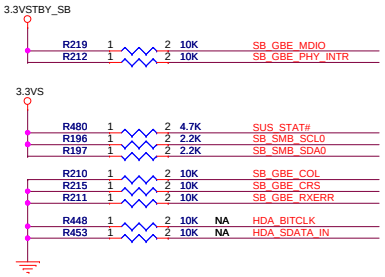
Mother Board ID:



ID4	ID3	ID2	ID1	ID0	Board ID	Board ID
0	0	1	1	0	0x366A	Kelly 1.x UMA (IMR)
0	0	1	1	1	0x366B	Kelly 1.x Seymour XT (IMR)
0	1	0	0	0	0x366C	Kelly 1.x Whistler Pro (IMR)
0	1	0	0	1	0x1649	Kelly 1.x UMA
0	1	0	1	0	0x164A	Kelly 1.x Seymour XT
0	1	0	1	1	0x164B	Kelly 1.x Whistler Pro
0	1	1	0	0	0x164C	Young 1.x UMA
0	1	1	0	1	0x164D	Young 1.x Seymour XT
0	1	1	1	0	0x164E	Young 1.x Whistler Pro

EMI





Stage ID
High --> SI (Deflaut internal PU)
Low --> PV

R461 1 2 1K MB_ID5

U111D

SB820M
Part 4 of 5

P111	PCI_PME#	J2	PCI_PME#/GEVENT4#
	CR_GPIO	K1	RI#/GEVENT22#
		D3	SPI_CS3#/GBE_STAT1/GEVENT21#
(11,29,32,36,39)	SLP_S3#	F1	SLP_S3#
(29)	SLP_S5#	H1	SLP_S5#
(29)	SB_PWRBTN#	F2	PWR_BTN#
(11)	SB_PWRGD	H5	PWR_GOOD
(8)	SUS_STAT#	G6	SUS_STAT#
P114	SB_TEST0	B3	TEST0
P116	SB_TEST1	C4	TEST1/TMS
P23	SB_TEST2	F6	TEST2
(29)	A20GATE	AD21	GA20IN/GEVENT0#
(29)	KB_RST#	AE21	KBRST#/GEVENT1#
(29)	SB_EXT_SCI#	K2	LPC_PME#/GEVENT3#
(29)	SB_EXT_SMI#	J29	LPC_SMI#/GEVENT23#
		H2	GEVENT5#
P110	SB_SYS_RST#	J1	SYS_RESET#/GEVENT19#
(32,33)	PCIE_WAKE#	H6	WAKE#/GEVENT8#
		F3	IR_RX1/GEVENT20#
P109	SB_TRIP#	J6	THRMTRIP#/SMBALERT#/GEVENT2#
(8)	NB_PWRGD	R241 1 2 0 NB_PWRGD_R	AC19 NB_PWRGD
(29)	RSMRST#	R240 1 2 33 RSMRST#_R	G1 RSMRST#
			AD19
			AA16
(31)	CR_CLKREQ#		CLK_REQ4#/SATA_IS0#/GPIO64
P19	SB_GPIO50		AB21 CLK_REQ3#/SATA_IS1#/GPIO63
(32)	LAN_CLKREQ#		AC18 SMARTVOLT1/SATA_IS2#/GPIO50
			AF20 CLK_REQ0#/SATA_IS3#/GPIO60
			AE19 SATA_IS4#/FANOUT3/GPIO55
			AF19 SATA_IS5#/FANIN3/GPIO59
(35)	SPKR		AD22 SPKR/GPIO66
(5,6,30,36)	SB_SMB_SCL0		AE22 SCL0/GPIO43
(5,6,30,36)	SB_SMB_SDA0		F5 SDA0/GPIO47
P25	SB_SMB_SCL1		F4 SCL1/GPIO227
P24	SB_SMB_SDA1		AH21 SDA1/GPIO228
(33)	USB3_CLKREQ#		AB18 CLK_REQ2#/FANIN4/GPIO62
(30)	WLAN_CLKREQ#		E1 CLK_REQ1#/FANOUT4/GPIO61
			AJ21 IR_LED#/LLB#/GPIO184
P100	SB_SMARTV2		H4 SMARTVOLT2/SHUTDOWN#/GPIO51
(9)	SPM_RST#		D5 DDR3_RST#/GEVENT7#
P113	SB_GBE_LED0		D7 GBE_LED0/GPIO183
			G5 GBE_LED1/GEVENT9#
			K3 GBE_LED2/GEVENT10#
			AA20 GBE_STAT0/GEVENT11#
			CLK_REQG#/GPIO65/OSCIN
(29)	SIO_EXT_WAKE#		H3
(31)	CR_GPIO		D1 BLINK/USB_OC7#/GEVENT18#
P112	SB_USB_OC5#		E4 USB_OC6#/IR_TX1/GEVENT6#
	SB_ODD_DA#		D4 USB_OC5#/IR_TX0/GEVENT17#
(27)	ODD_PLUGIN#		E8 USB_OC4#/IR_RX0/GEVENT16#
(33)	USB3_SMI#		F7 USB_OC3#/AC_PRES/TDO/GEVENT15#
(34)	USB_OC1#		E7 USB_OC2#/TCK/GEVENT14#
(38)	USB_OC0#		F8 USB_OC1#/TDI/GEVENT13#
			USB_OC0#/TRST#/GEVENT12#
		R451 1 2 10K NA	
(35)	HDA_BITCLK	R449 2 1 33 HDA_BITCLK_R	M3
(35)	HDA_SDATA_OUT	R444 2 1 33 HDA_SDATA_OUT_R	N1 AZ_BITCLK
(35)	HDA_SDATA_IN		L2 AZ_SDOUT
(12)	HDA_SDATA_OUT_R		M2 AZ_SDIN0/GPIO167
			M1 AZ_SDIN1/GPIO168
			M4 AZ_SDIN2/GPIO169
(35)	HDA_SYNC	R443 2 1 33 HDA_SYNC_R	N2 AZ_SDIN3/GPIO170
(35,36)	HDA_RESET#	R441 2 1 33 HDA_RESET#_R	P2 AZ_SYNC
			AZ_RST#
	SB_GBE_COL		T1 GBE_COL
	SB_GBE_CRS		T4 GBE_CRS
			L6 GBE_MDCK
	SB_GBE_MDIO		L5 GBE_MDIO
			T9 GBE_RXCLK
			U1 GBE_RXD3
			U3 GBE_RXD2
			T2 GBE_RXD1
			U2 GBE_RXD0
			T5 GBE_RXCTL/RXDV
	SB_GBE_RXERR		V5 GBE_RXERR
			P5 GBE_TXCLK
			M5 GBE_TXD3
			P9 GBE_TXD2
			T7 GBE_TXD1
			P7 GBE_TXD0
			M7 GBE_TXCTL/TXEN
			P4 GBE_PHY_PD
			M9 GBE_PHY_RST#
	SB_GBE_PHY_INTR		V7 GBE_PHY_INTR
			E23
			E24 PS2_DAT/SDA4/GPIO187
			F21 PS2_CLK/SCL4/GPIO188
			G29 SPI_CS2#/GBE_STAT2/GPIO166
			FC_RST#/GPO160
	MB_ID0		D27
	MB_ID1		F28 PS2KB_DAT/GPIO189
	MB_ID2		F29 PS2KB_CLK/GPIO190
	MB_ID3		E27 PS2M_DAT/GPIO191
			PS2M_CLK/GPIO192

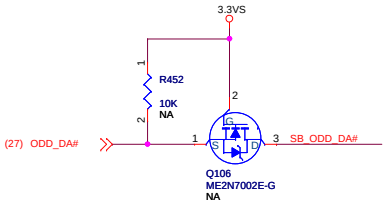
ATI_SB820M

ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
GPIO
USB 2.0
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
EMBEDDED CTRL

		USBCLK/14M_25M_48M_OSC	A10 CLK_USB_48M_R R479 1 2 22 NA CLK_USB_48M (33)
		USB_RCOMP	G19 USB-RCOMP R224 1 2 11.8K_F
		USB_FSD1P/GPIO186	J10
		USB_FSD1N	H11
		USB_FSD0P/GPIO185	H9
		USB_FSD0N	J8
		USB_HSD13P	B12
		USB_HSD13N	A12
		USB_HSD12P	F11
		USB_HSD12N	E11
		USB_HSD11P	E14 USB-TOUP_P (24)
		USB_HSD11N	E12 USB-TOUP_N (24)
		USB_HSD10P	J12 USB-WEBCAM_P (28)
		USB_HSD10N	J14 USB-WEBCAM_N (28)
		USB_HSD9P	A13
		USB_HSD9N	B13
		USB_HSD8P	D13
		USB_HSD8N	C13
		USB_HSD7P	G12 USB-FP_P (28)
		USB_HSD7N	G14 USB-FP_N (28)
		USB_HSD6P	G16 USB-WLAN_P (30)
		USB_HSD6N	G18 USB-WLAN_N (30)
		USB_HSD5P	D16
		USB_HSD5N	C16
		USB_HSD4P	B14
		USB_HSD4N	A14
		USB_HSD3P	E18 USB3_P (34)
		USB_HSD3N	E16 USB3_N (34)
		USB_HSD2P	J16 USB2_P (34)
		USB_HSD2N	J18 USB2_N (34)
		USB_HSD1P	B17 USB1_P (38)
		USB_HSD1N	A17 USB1_N (38)
		USB_HSD0P	A16 USB0_P (38)
		USB_HSD0N	B16 USB0_N (38)
		SCL2/GPIO193	D25
		SDA2/GPIO194	F23
		SCL3_LV/GPIO195	B26
		SDA3_LV/GPIO196	E26
		EC_PWM0/EC_TIMER0/GPIO197	F25
		EC_PWM1/EC_TIMER1/GPIO198	E22
		EC_PWM2/EC_TIMER2/GPIO199	F22
		EC_PWM3/EC_TIMER3/GPIO200	E21
		KSI_0/GPIO201	G24
		KSI_1/GPIO202	G25
		KSI_2/GPIO203	E28
		KSI_3/GPIO204	E29
		KSI_4/GPIO205	D29
		KSI_5/GPIO206	D28
		KSI_6/GPIO207	C29
		KSI_7/GPIO208	C28
		KSO_0/GPIO209	B28
		KSO_1/GPIO210	A27
		KSO_2/GPIO211	B27
		KSO_3/GPIO212	D26
		KSO_4/GPIO213	A26
		KSO_5/GPIO214	C26
		KSO_6/GPIO215	A24
		KSO_7/GPIO216	B25
		KSO_8/GPIO217	A25
		KSO_9/GPIO218	D24
		KSO_10/GPIO219	B24
		KSO_11/GPIO220	C24
		KSO_12/GPIO221	B23
		KSO_13/GPIO222	A23
		KSO_14/GPIO223	D22
		KSO_15/GPIO224	C22
		KSO_16/GPIO225	A22
		KSO_17/GPIO226	B22

Touch Screen
Web CAM
Finger Print
WLAN
Port 3
Port 2
Port 1
Port 0

SB_EC_PWM2 (12)
SB_EC_PWM3 (12)

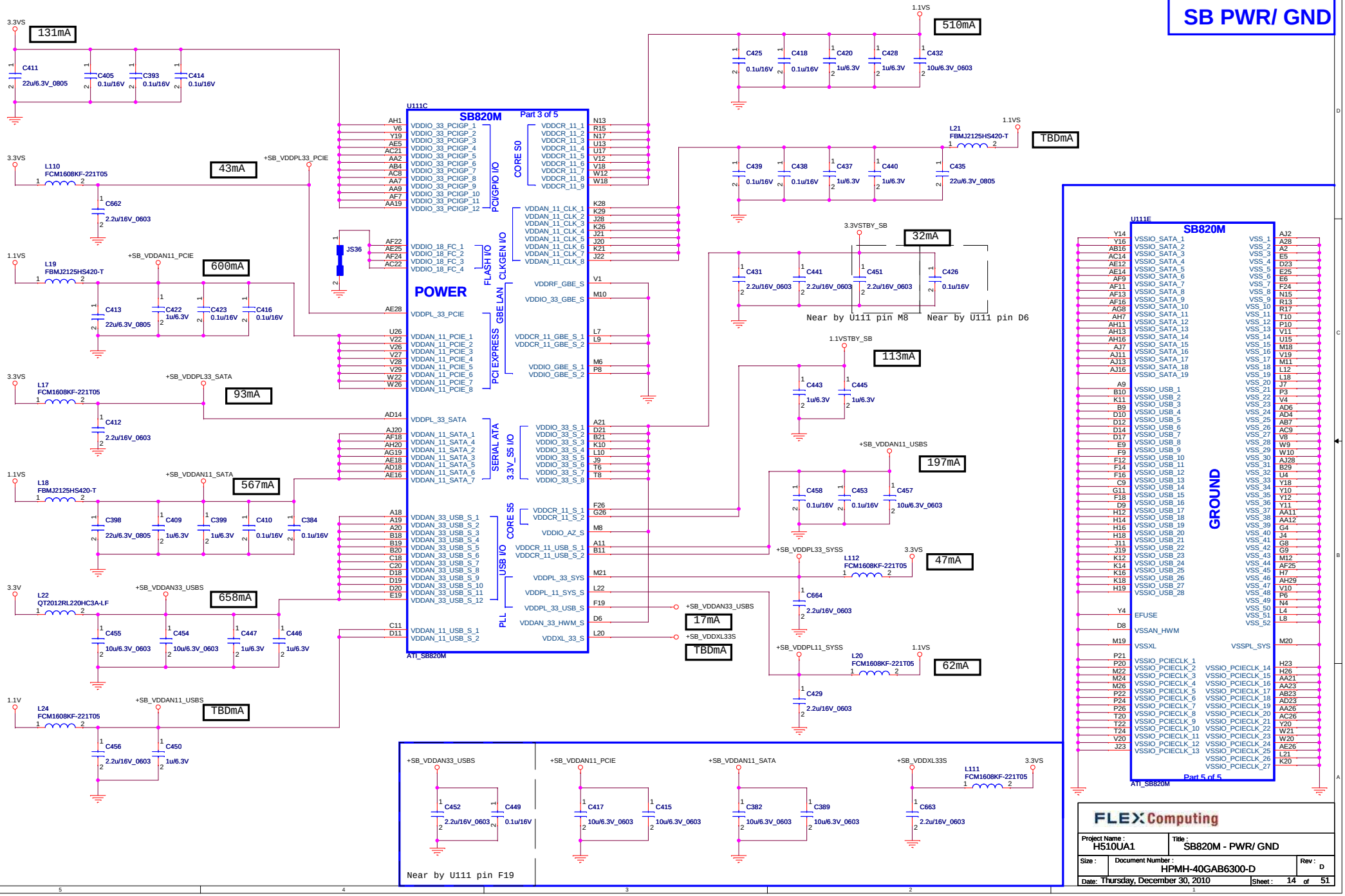


Reserve for Zero-ODD

FLEX Computing

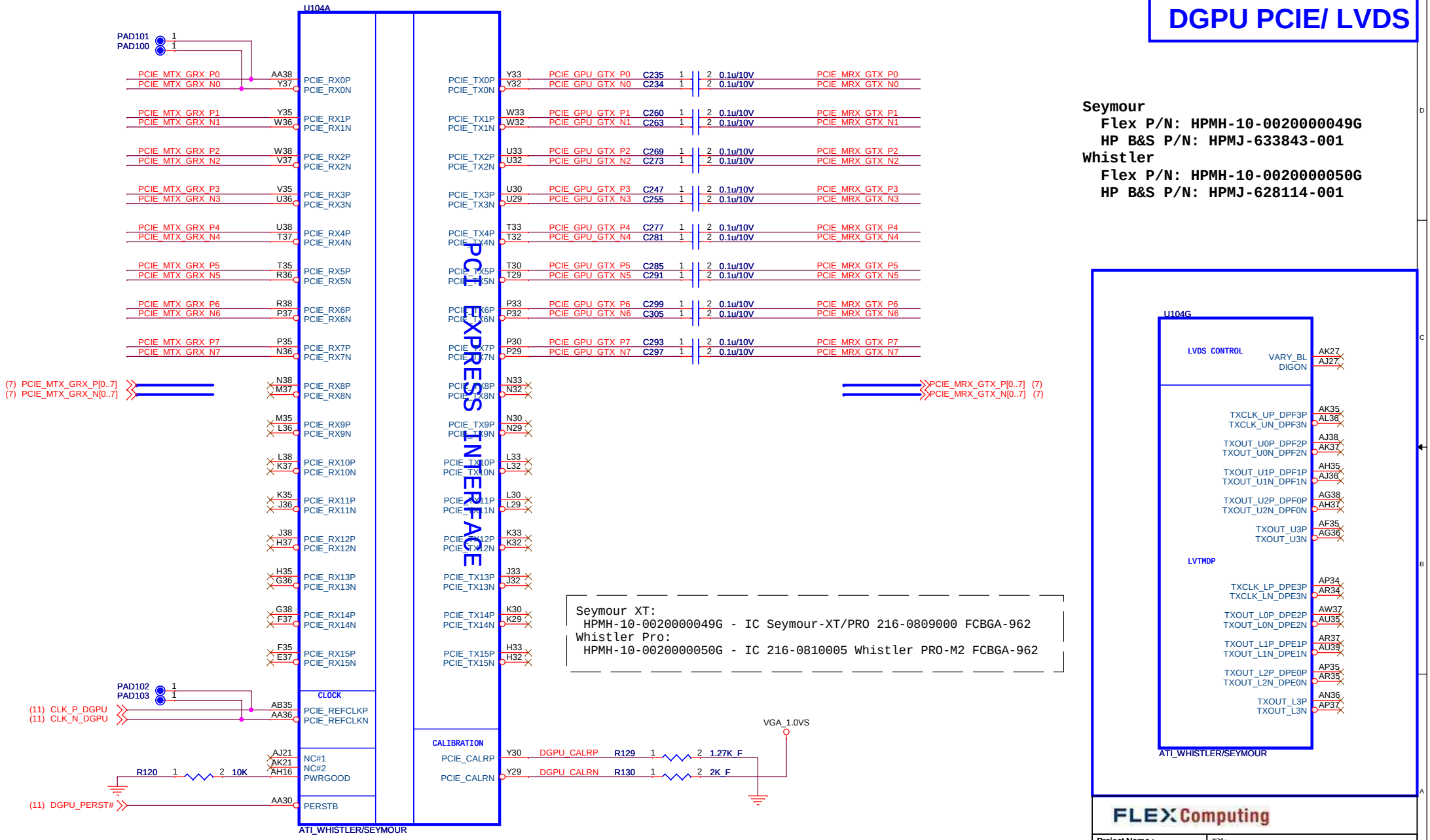
Project Name : H510UA1	Title : SB820M - ACPI/ USB/ HDA/ GLAN
Size :	Document Number : HPMH-40GAB6300-D
Rev : D	
Date: Thursday, December 30, 2010	Sheet : 13 of 51

SB PWR/ GND


U111C
SB820M
Part 3 of 5
POWER
ATI_SB820M
131mA
43mA
600mA
93mA
567mA
658mA
TBDmA
510mA
TBDmA
32mA
Near by U111 pin M8
Near by U111 pin D6
113mA
197mA
47mA
62mA
17mA
TBDmA
U111E
SB820M
GROUND
Part 5 of 5
ATI_SB820M
Near by U111 pin F19
FLEX Computing
Project Name : H510UA1
Title : SB820M - PWR/ GND
Size :
Document Number : HPMH-40GAB6300-D
Rev : D
Date: Thursday, December 30, 2010
Sheet : 14 of 51

DGPU PCIE/ LVDS

Seymour
Flex P/N: HPMH-10-00200000049G
HP B&S P/N: HPMJ-633843-001
Whistler
Flex P/N: HPMH-10-00200000050G
HP B&S P/N: HPMJ-628114-001



Seymour XT:
HPMH-10-00200000049G - IC Seymour-XT/PRO 216-0809000 FCBGA-962
Whistler Pro:
HPMH-10-00200000050G - IC 216-0810005 Whistler PRO-M2 FCBGA-962

PWRGOOD
For Broadway, Madison and Park the PWRGOOD ball must be conneccted to ground

FLEXComputing

Project Name : H510UA1	Title : DGPU - PCI-E/ LVDS I/F
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Thursday, December 30, 2010	Sheet : 15 of 51

DGPU DISP/ THRM/ PM

	DVPDATA_2	DVPDATA_1	DVPDATA_0
Hynix (64Mx16) x4pcs	0	0	0
Samsung (64Mx16) x4pcs	1	0	0
Hynix (128Mx16) x4pcs	0	1	0
Samsung (128Mx16) x4pcs	1	1	0
Hynix (64Mx16) x8pcs	0	0	1
Samsung (64Mx16) x8pcs	1	0	1
Hynix (128Mx16) x8pcs	0	1	1
Samsung (128Mx16) x8pcs	1	1	1

64MX16
HYNIX:
Flex P/N: HPMH-14-00D0000040G - IC DDR3 H5TQ1G63DFR-11C 64MX16 FBGA-96
HP B&S P/N: HPMJ-506474-945
SAMSUNG:
Flex P/N: HPMH-14-00D0000042G - IC DDR3 K4W1G1646G-BC11 64MX16 FBGA-96
HP B&S P/N: HPMJ-506474-344

128MX16:
Hynix: HPMH-14-00D0000039G - IC DDR3 H5TQ2G63BFR-11C 128MX16 FBGA-96
Samsung: HPMH-14-00D0000043G - IC K4W2G1646C-HC11 128Mb*16 96 FBGA

VMEM ID

NC on Park

NC on Park

To PWR PWM

To PWR PWM

VREF=0.6V

ADC input (range 0 1.0V). This analog input signal can be used to measure regulator current or temperature for Broadway

NC on Seymour / Whistler

NC on Seymour / Whistler

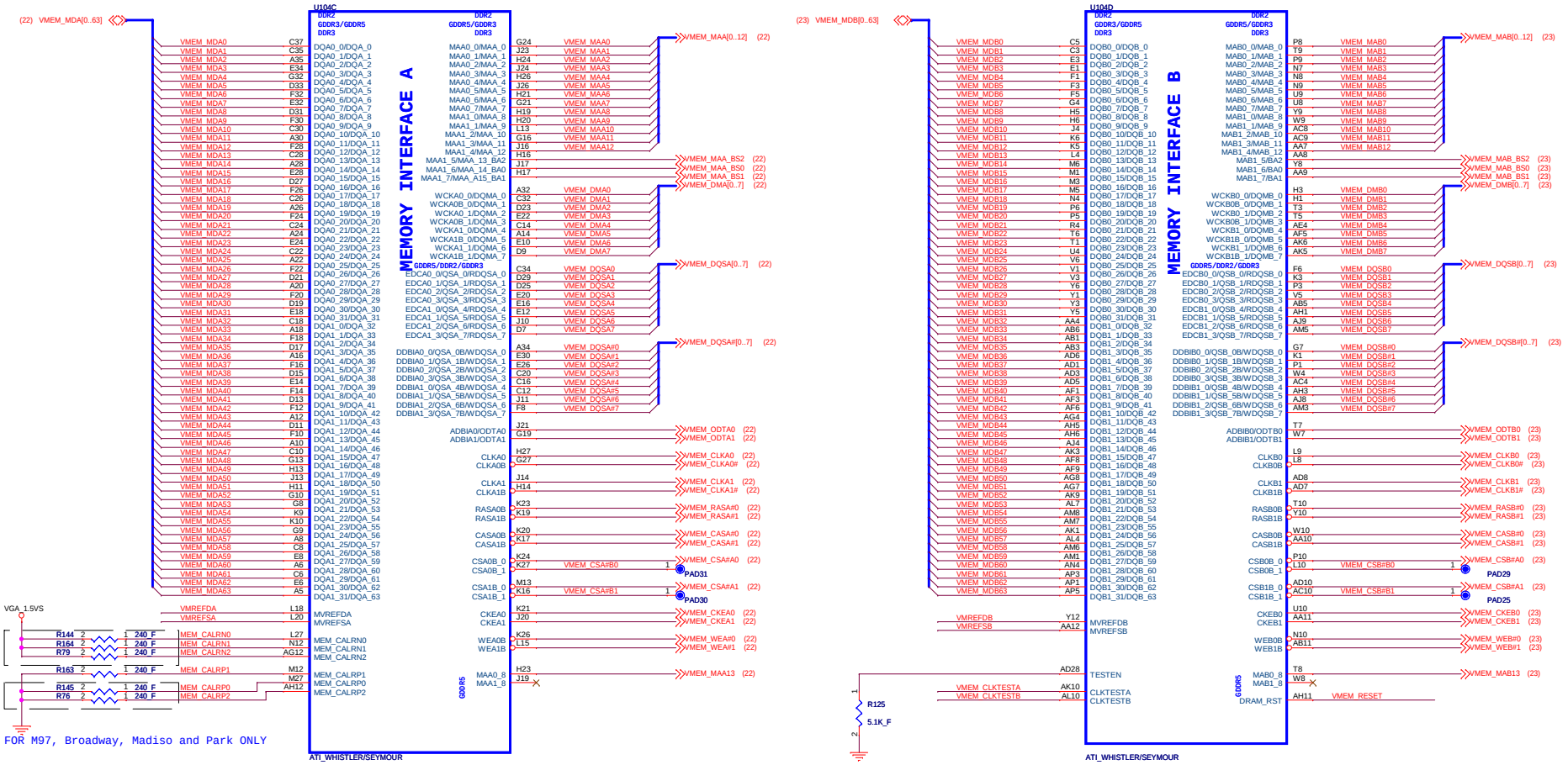
NC on Seymour / Whistler

DDCxx_AUX3x is NC on M92M2
DDCxx_AUX4x is NC on M92M2 and PARK
DDCxx_AUX7x is NC on M9x and PARK

ATI_WHISTLER/SEYMOUR

Project Name : H510UA1	Title : DGPU - Display/ Thermal/ GPIO
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 16 of 51

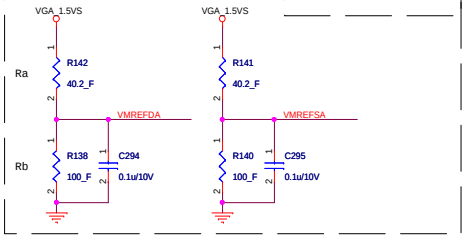
DGPU VRAM I/F



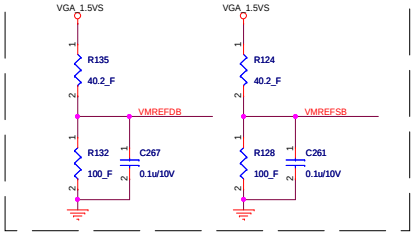
DIVIDER RESISTORS	DDR3/ GDDR3
MVREF TO 1.5V (Ra)	40.2R
MVREF TO GND (Rb)	100R

Place colse to Pin
For DDR3: 0.7 * VDDR1

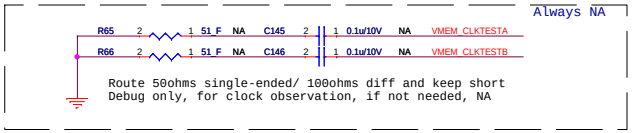
Seymour: NA
Whistler: Mounte

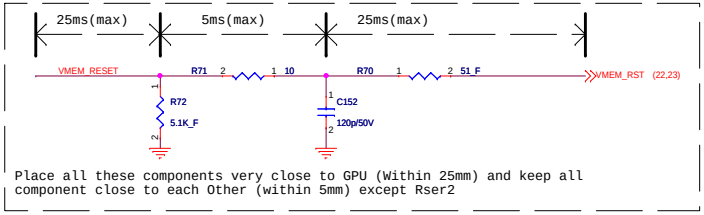


Place colse to Pin
For DDR3: 0.7 * VDDR1



Always NA





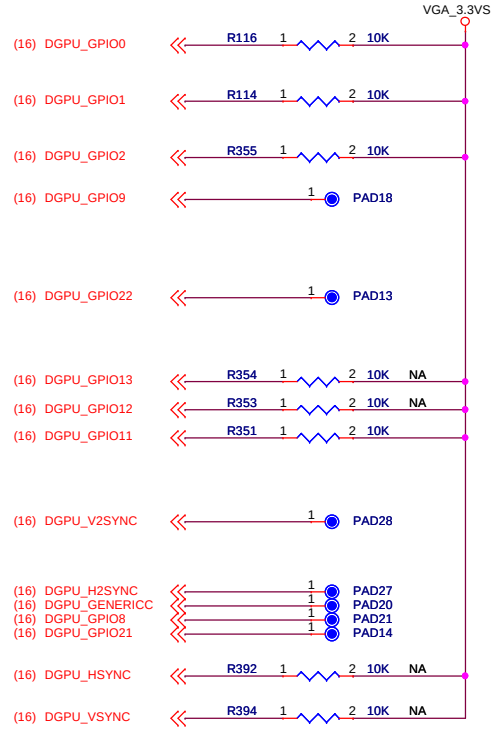
FLEX Computing

Project Name : H510UA1	Title : DGPU - VRAM I/F
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 17 of 51

DGPU STRAP

CONFIGURATION STRAPS

STRAPS	PIN	DESCRIPTION	ASIC Deault	Status
TX_PWRS_ENB	GPIO0	Transmitter (Tx) power savings enable 0: 50% Tx output swing (DEFAULT) 1: Full Tx output swing	All Internal Pull Down	Mounted
TX_DEEMPH	GPIO1	PCI Express transmitter deemphasis enable. 0: Tx de-emphasis disabled (DEFAULT) 1: Tx de-emphasis enabled		Mounted
RESERVED	GPIO2	0 : PCIe device as 2.5 GT/s capable (DEFAULT) 1 : PCIe device as 5.0 GT/s capable		Mounted
VGA_DIS	GPIO9	VGA disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space): 0 : VGA Controller capacity enabled (DEFAULT) 1 : The device will not be recognized as the system's VGA controller		NA
BIOS_ROM_EN	GPIO_22_ROMCSB	0 - Disable external BIOS ROM device (DEFAULT) 1 - Enable external BIOS ROM device		NA
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	BIOS_ROM_EN = 1, Config[2:0] defines the ROM type. BIOS_ROM_EN = 0, Config[2:0] defines the primary memory aperture size. Size of the primary memory apertures CONFIG[2:0] 128 MB 000 256 MB 001 64MB 010 32MB 011		NA NA Mounted
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS L: Ignore VIP Device Strap (DEFAULT) H: Enable VIP Device Strap		NA
RSVD RSVD RSVD RSVD	H2SYNC GENERICC GPIO8 GPIO21_BB_EN			NA NA NA NA
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI		NA NA



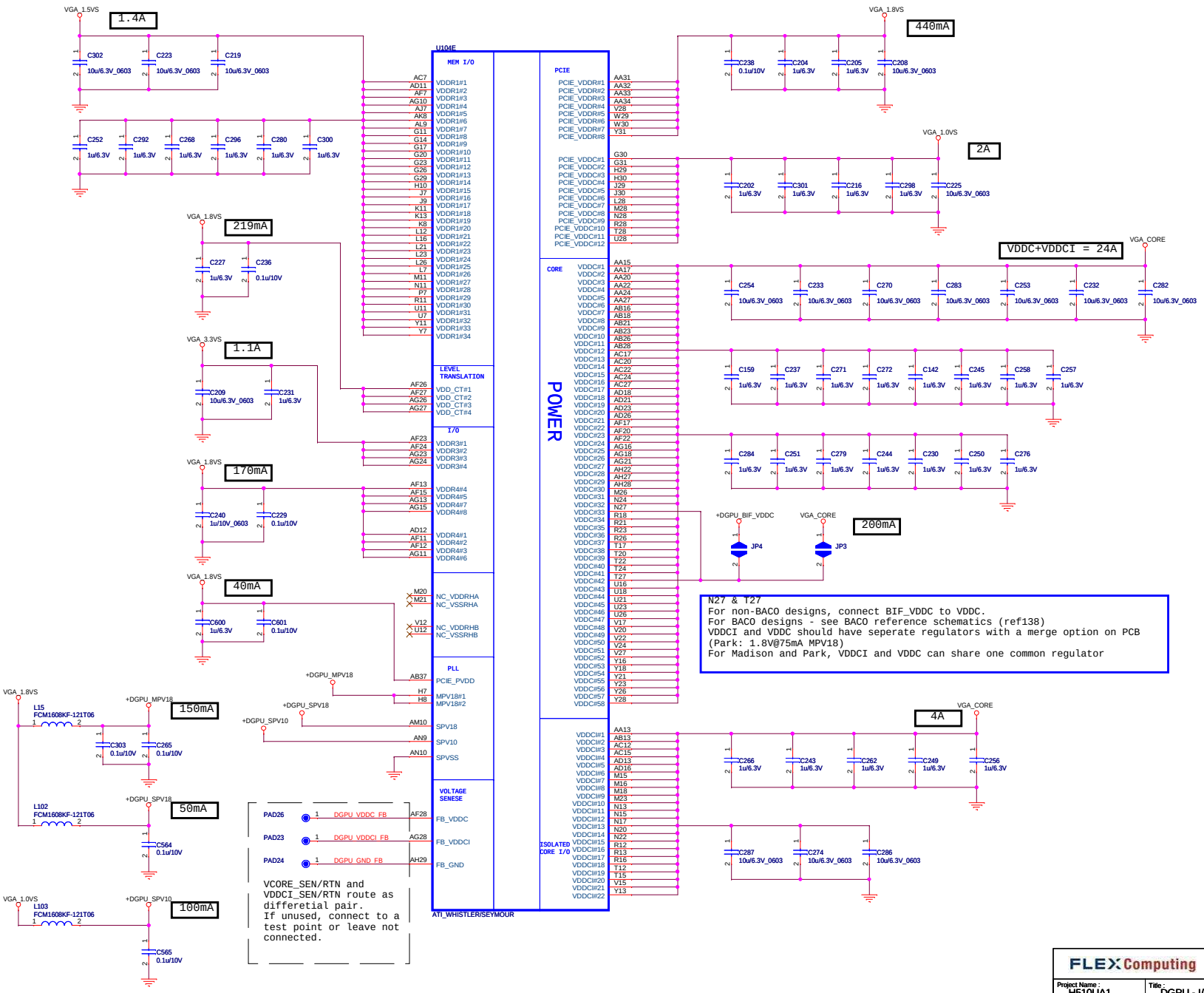
Signal	Seymour/Whistler	Robson/ Park/ Medison/ Capilano/ Broadway
Ball AJ21 on M2 Ball AG13 on S3	SWAPLOCKA SwaplockA/ B signals can be optionally used on a multi-GPU design with multiple display outputs to allow all displays in a group (group A or group B) to update at the same time and have synchronous left/ right stereo timing. Genlock of the GPUs is also needed, either via a genlock system, or by feeding all GPUs with the same reference clock. Also connecting SwaplockB is preferred, but not required. SwaplockA/ B are open drain, 3.3V signals. If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AJ21 is NC on M2 packages Ball AG13 is R2SET on S3 package
Ball AK21 on M2 Ball H12 on S3	SWAPLOCKB – see above On a multi-gpu design,SwaplockB from all GPUs are connected together with an external pull-up resistor (10K Ohms). If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AK21 is NC on M2 packages Ball AH12 is DAC2 Output - on S3 package

Signal	Seymour/Whistler	Robson/ Park/ Medison/ Capilano/ Broadway
Ball AC32 on M2	NC	DAC2 Output-C on M2 package
Ball AA29 on M2	NC	R2SET on M2 package
Ball AD32 on M2	NC	DAC2 Output- Y
Ball AG33 on M2	NC	A2VDD
Ball AD33 on M2	NC	A2VDDQ
Ball AF33 on M2	TSVSSQ	A2VSSQ
Ball AG33, AG32 on M2	NC	VDD2DI/VSS2DI
H2SYNC	GENLK_CLK (3.3V): Reference clock input (3.3V) for pixel PLL received from frame-lock/ gen-lock interface	H2SYNC
V2SYNC	GENLK_VSYNC (3.3V): Frame timing indicator.Output to frame-lock/genlock interface	V2SYNC

FLEX Computing

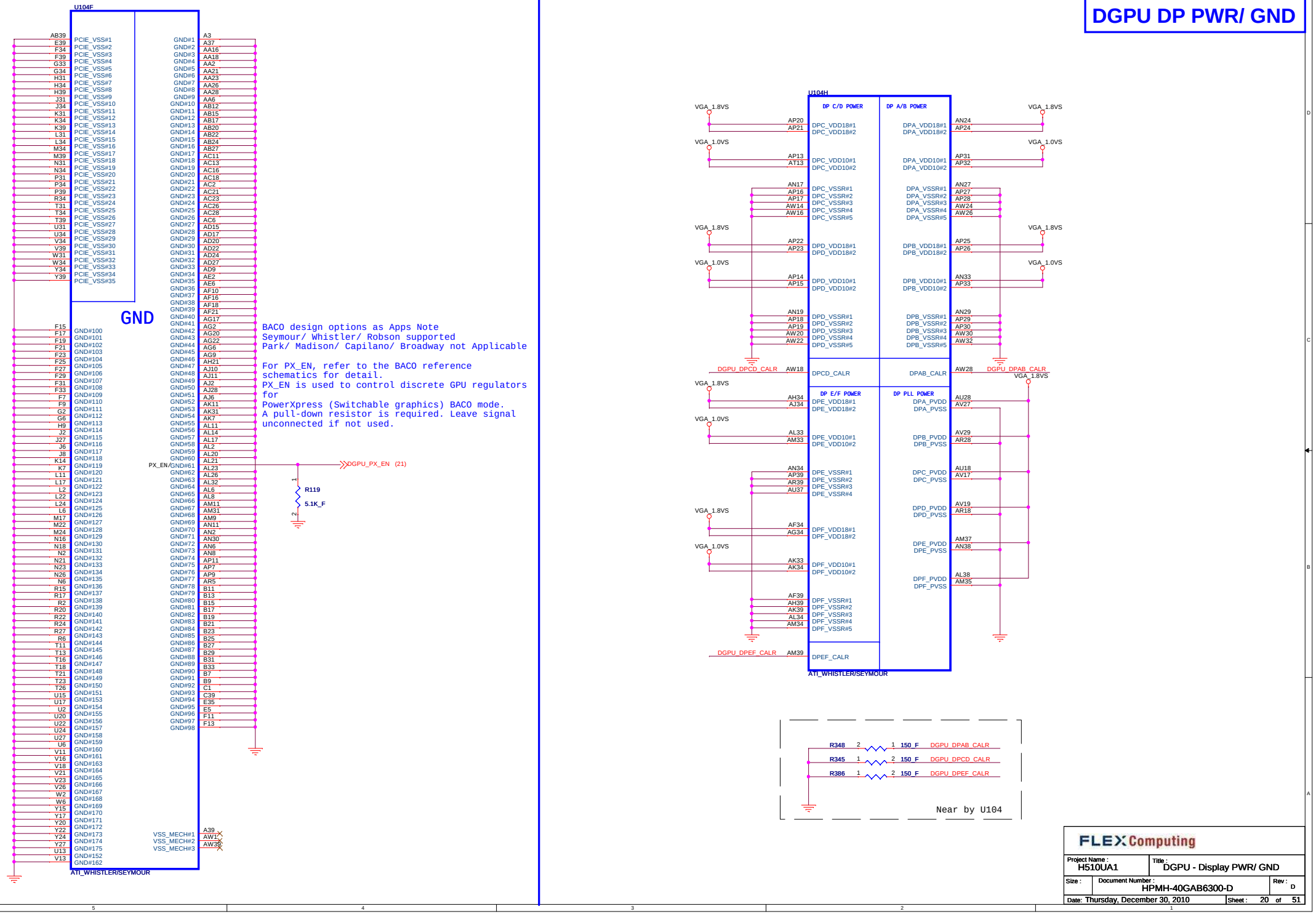
Project Name : H510UA1	Title : DGPU - Strap
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 18 of 51

DGPU IO PWR/ GND



FLEX Computing	
Project Name: H510UA1	Title: DGPU - I/O PWR
Size:	Document Number: HPMH-40GAB6300-D Rev: D
Date: Thursday, December 30, 2010	Sheet: 19 of 51

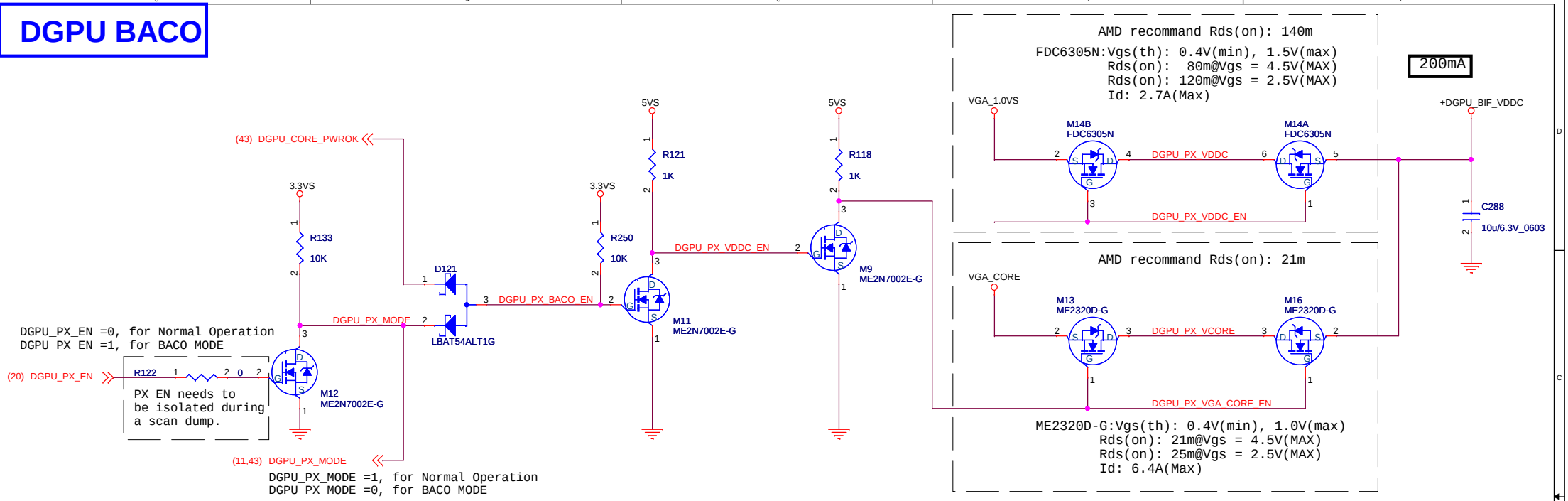
DGPU DP PWR/ GND



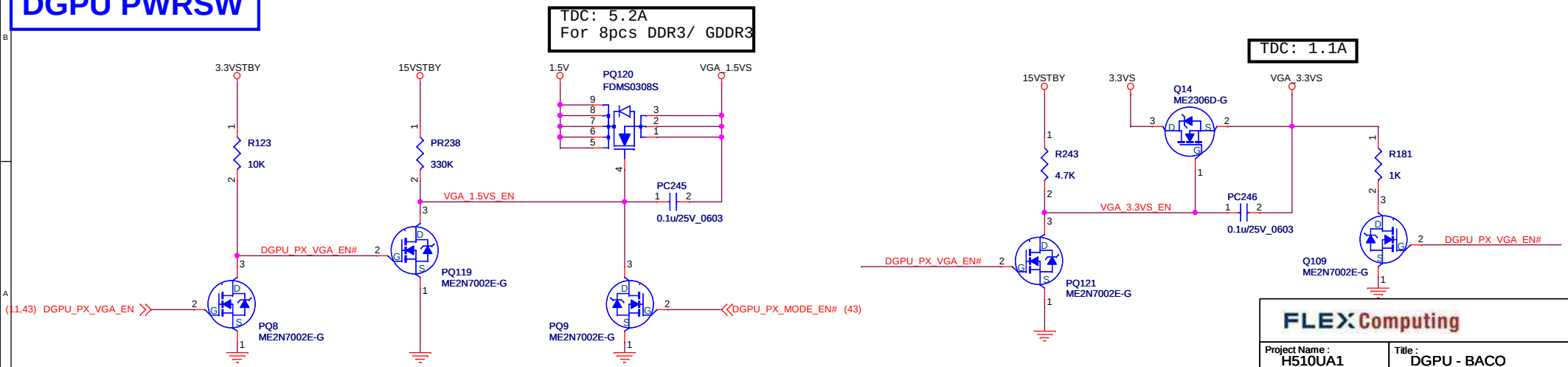
Project Name : H510UA1	Title : DGPU - Display PWR/ GND
Size :	Document Number : HPMH-40GAB6300-D
Rev : D	
Date: Thursday, December 30, 2010	Sheet : 20 of 51

FLEX Computing

DGPU BACO



DGPU PWRSW

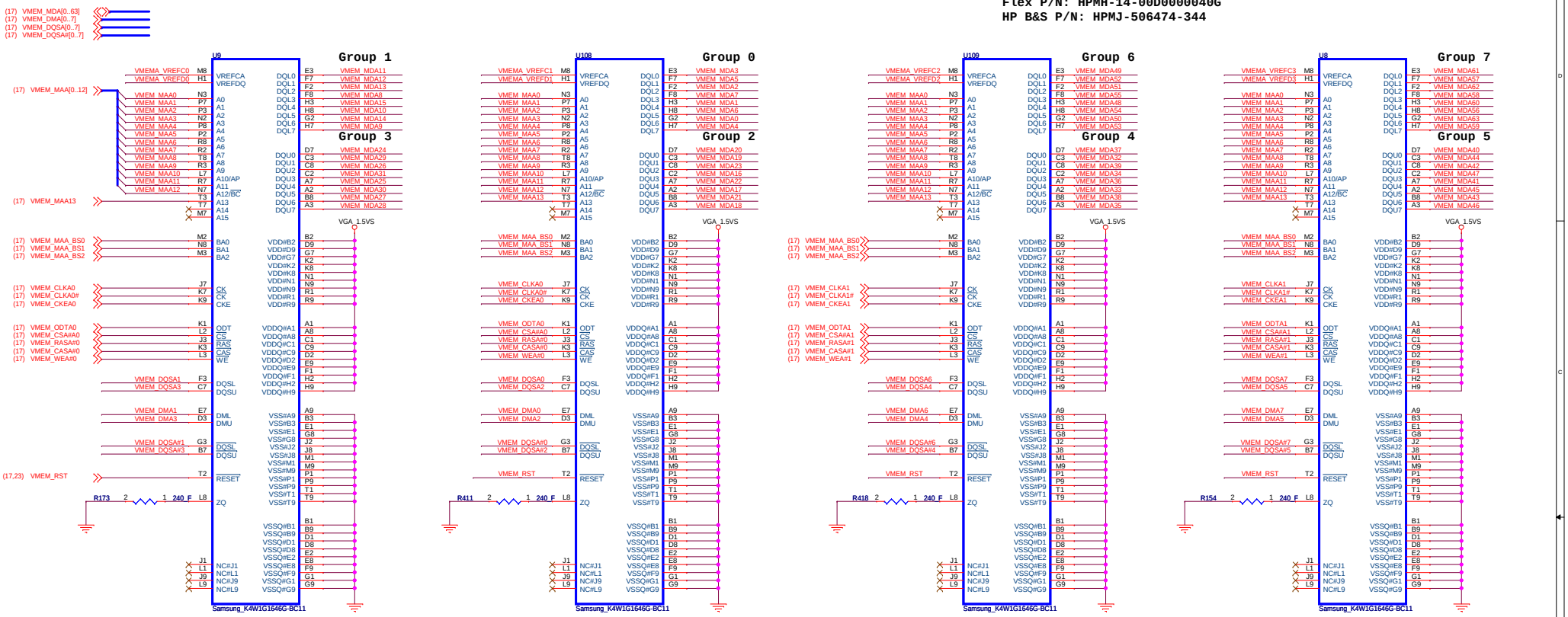


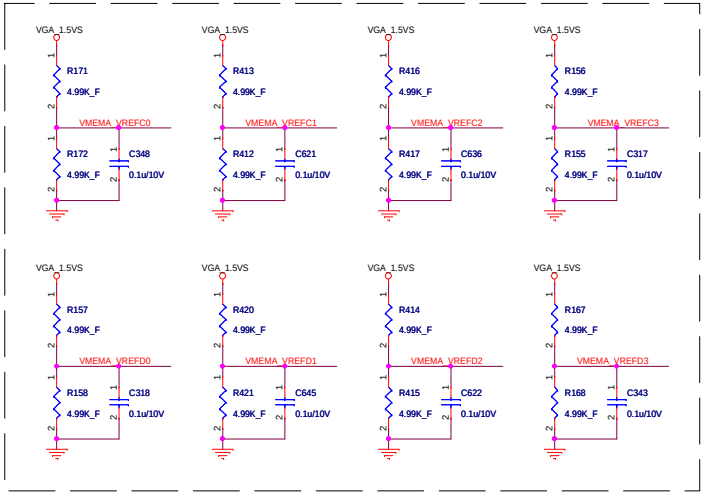
FLEXComputing

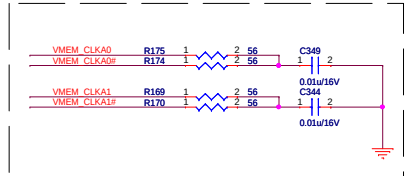
Project Name : H510UA1	Title : DGPU - BACO	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 21 of 51	

DGPU VRAM Channel - A

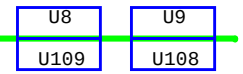
Samsung/ K4W1G1646G-BC11
Flex P/N: HPMH-14-00D0000042G
HP B&S P/N: HPMJ-506474-945
Hynix/ H5TQ1G63DFR-11C
Flex P/N: HPMH-14-00D0000040G
HP B&S P/N: HPMJ-506474-344







PCB Layout indicate

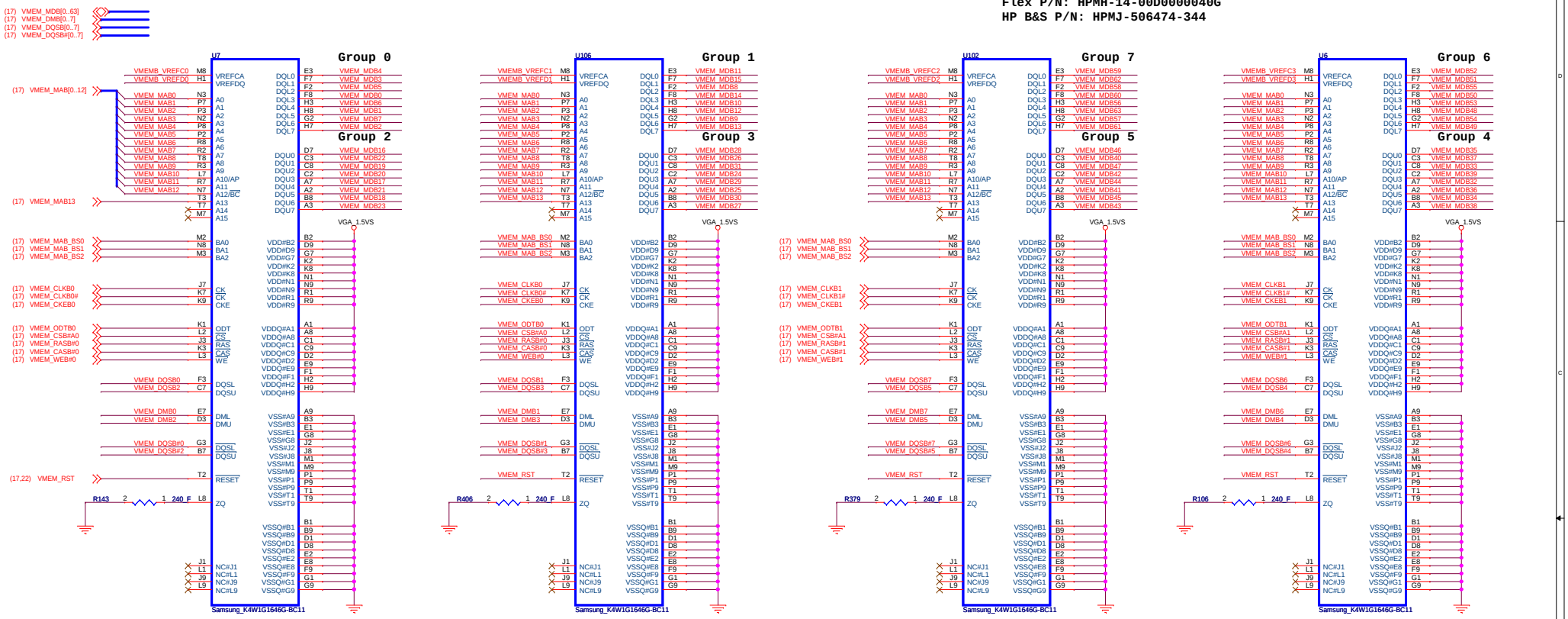


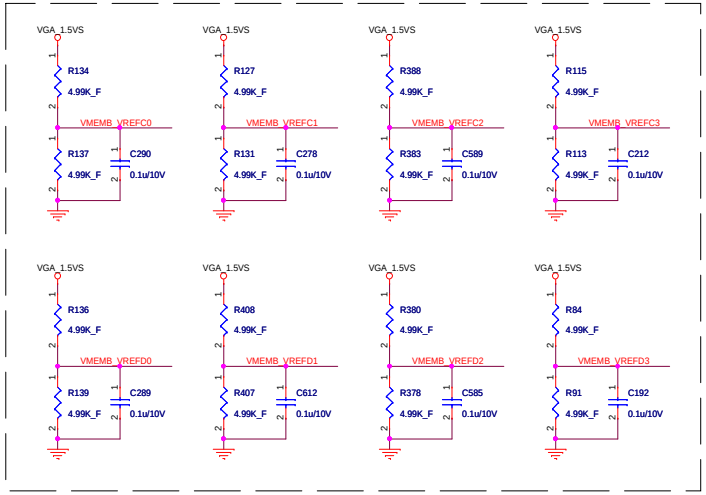
FLEX Computing

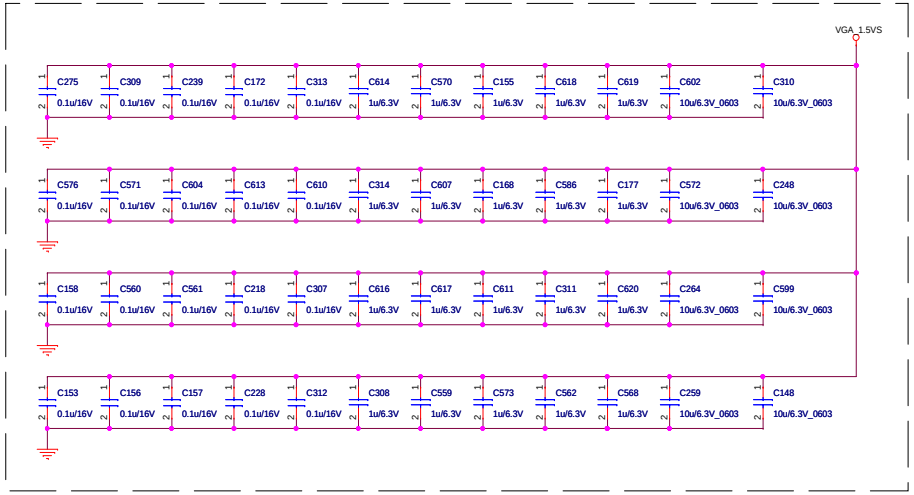
Project Name: H510UA1	Title: DGPU - VRAM Channel - A	
Size:	Document Number: HPMH-40GAB6300-D	Rev: D
Date: Thursday, December 30, 2010	Sheet: 22 of 51	

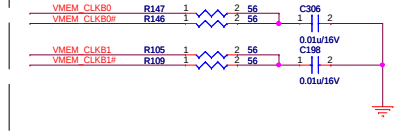
DGPU VRAM Channel - B

Samsung/ K4W1G1646G-BC11
Flex P/N: HPMH-14-00D0000042G
HP B&S P/N: HPMJ-506474-945
Hynix/ H5TQ1G63DFR-11C
Flex P/N: HPMH-14-00D0000040G
HP B&S P/N: HPMJ-506474-344

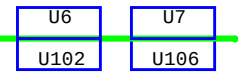








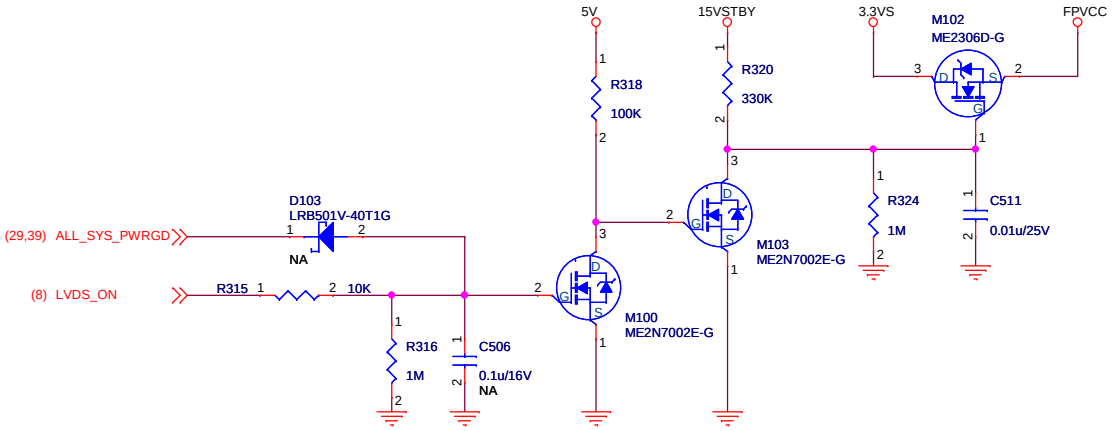
PCB Layout indicate

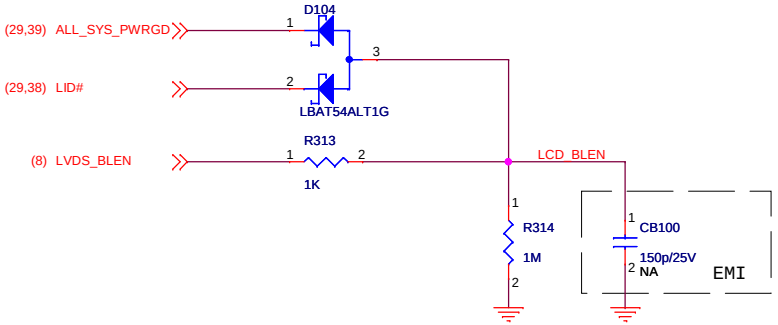


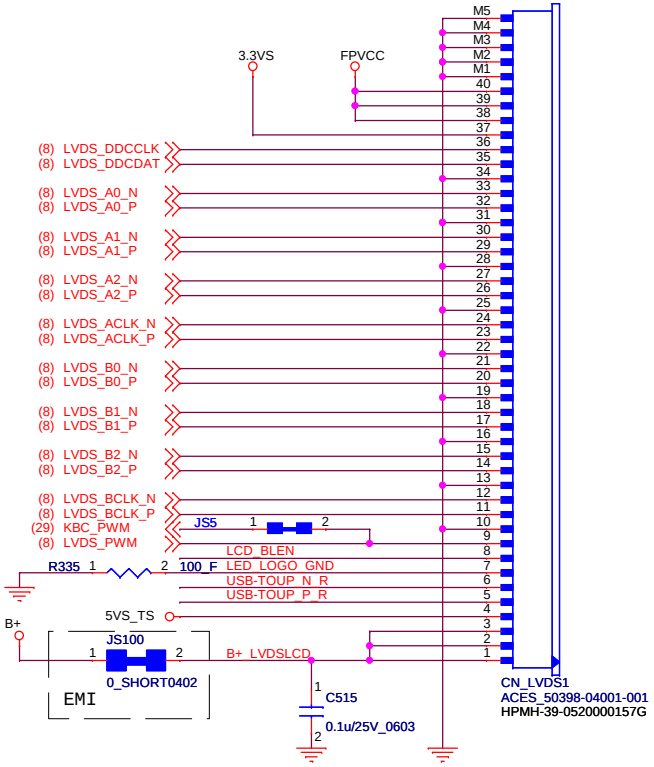
FLEX Computing

Project Name: H510UA1	Title: DGPU - VRAM Channel - B	
Size:	Document Number: HPMH-40GAB6300-D	Rev: D
Date: Thursday, December 30, 2010	Sheet: 23 of 51	

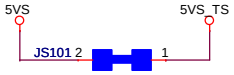
LVDS

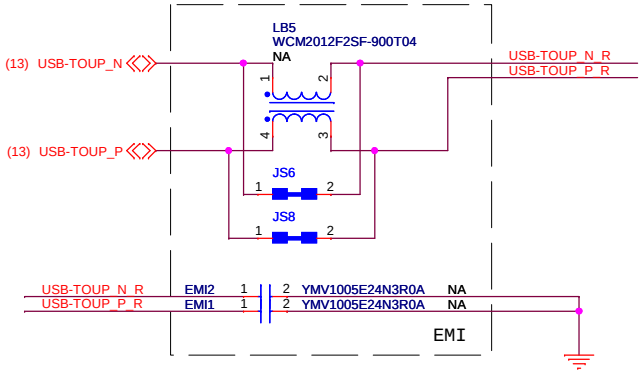


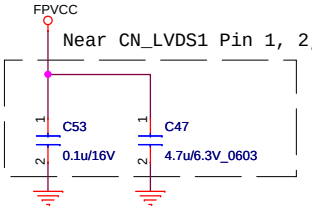


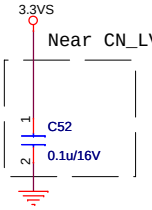


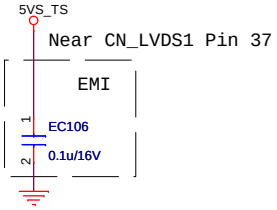
Touch Screen

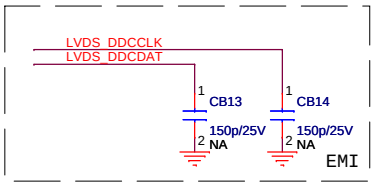








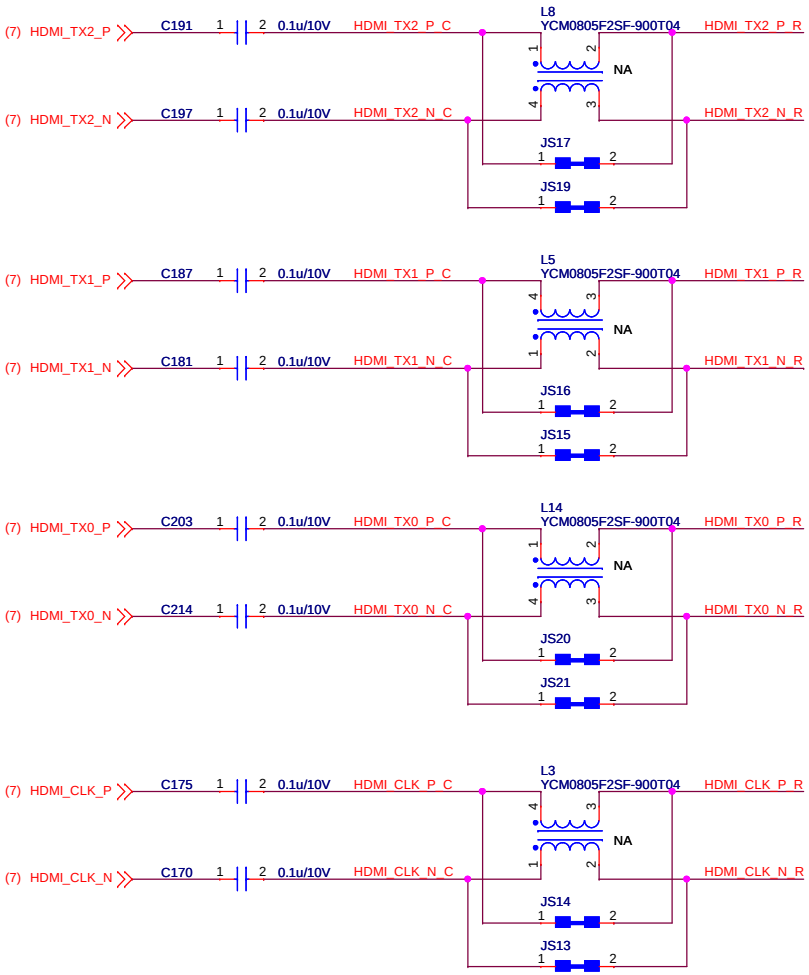


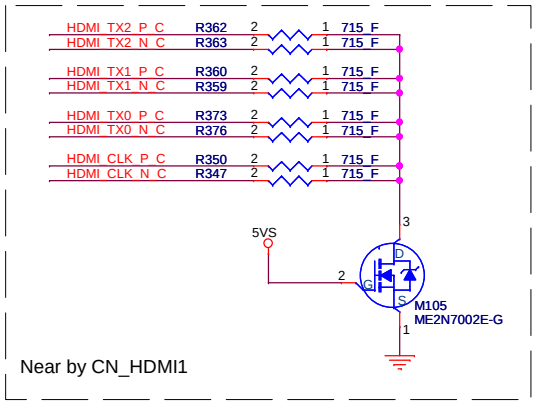


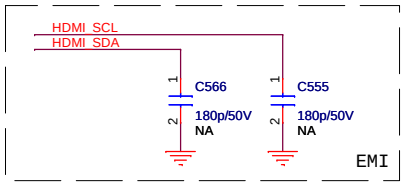
FLEXComputing

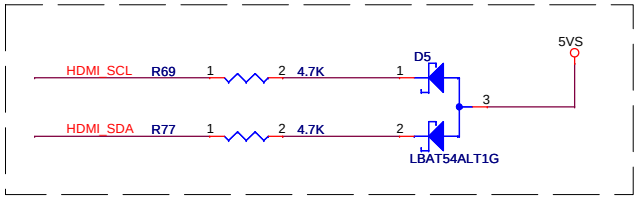
Project Name : H510UA1	Title : LVDS/ Touch Screen I/F
Size :	Document Number : HPMH-40GAB6300-D
Rev : D	
Date: Thursday, December 30, 2010	Sheet : 24 of 51

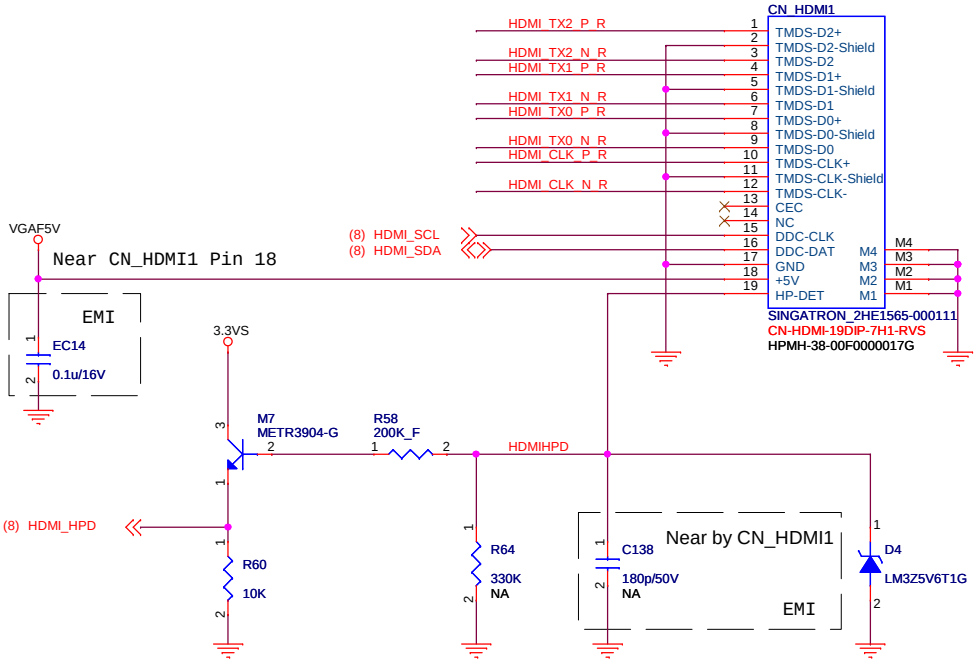
HDMI







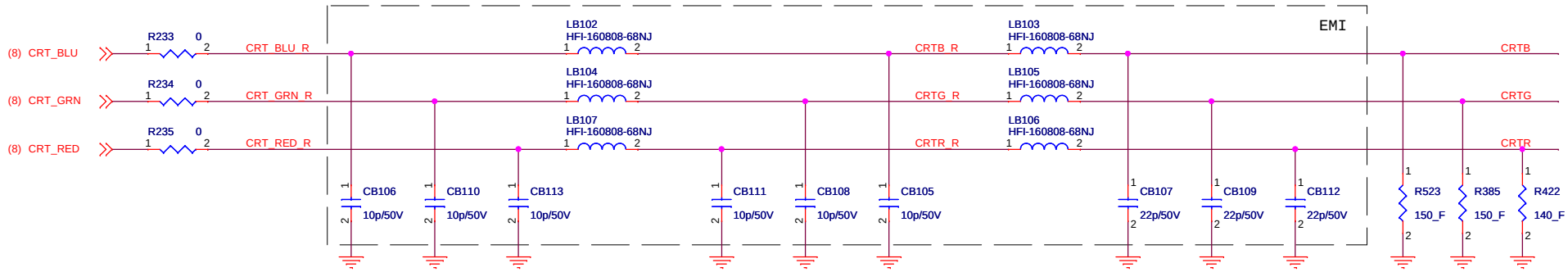


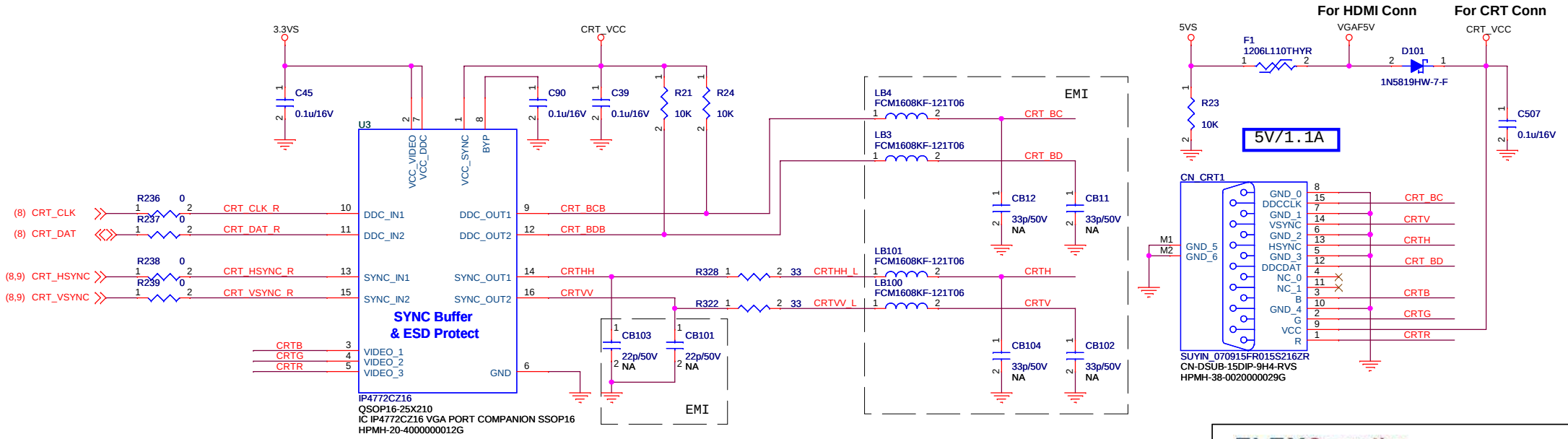


FLEXComputing

Project Name : H510UA1	Title : HDMI I/F
Size :	Document Number : HPMH-40GAB6300-D
Rev : D	
Date: Thursday, December 30, 2010	Sheet : 25 of 51

CRT

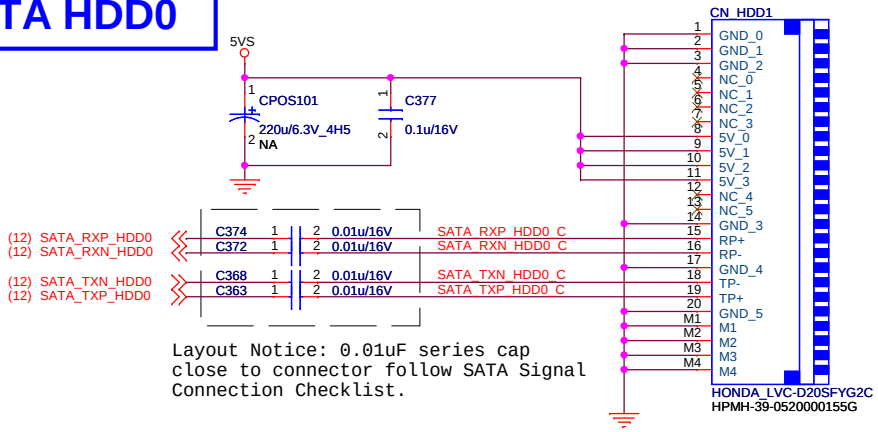




FLEXComputing

Project Name : H510UA1	Title : D-sub I/F
Size :	Document Number : HPMH-40GAB6300-D / Rev : D
Date: Thursday, December 30, 2010	Sheet : 26 of 51

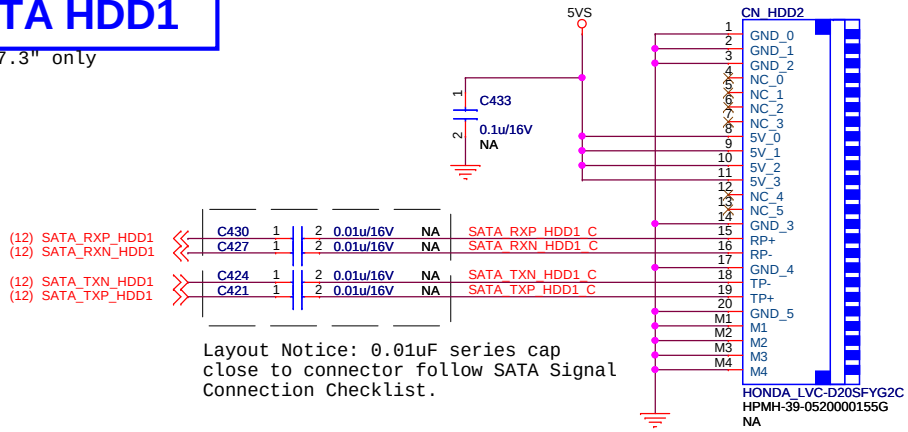
SATA HDD0



Layout Notice: 0.01uF series cap close to connector follow SATA Signal Connection Checklist.

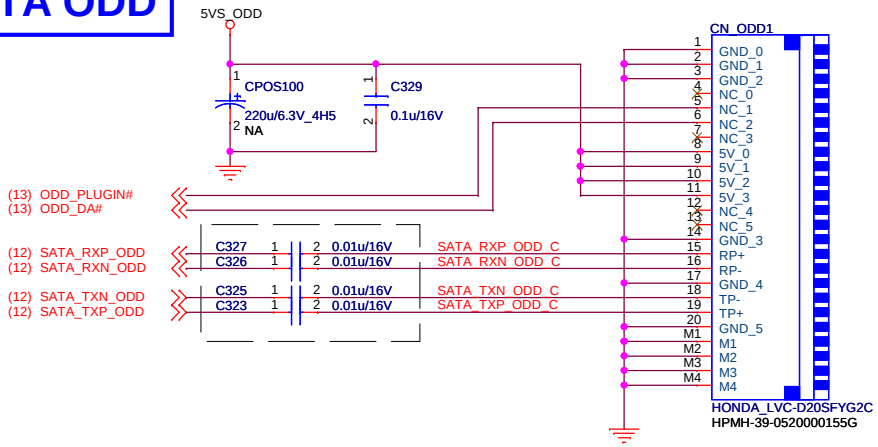
SATA HDD1

For 17.3" only

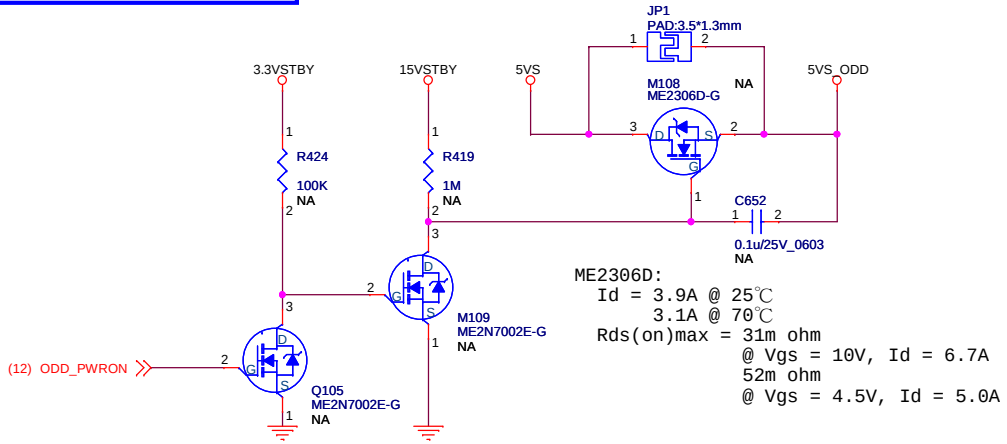


Layout Notice: 0.01uF series cap close to connector follow SATA Signal Connection Checklist.

SATA ODD

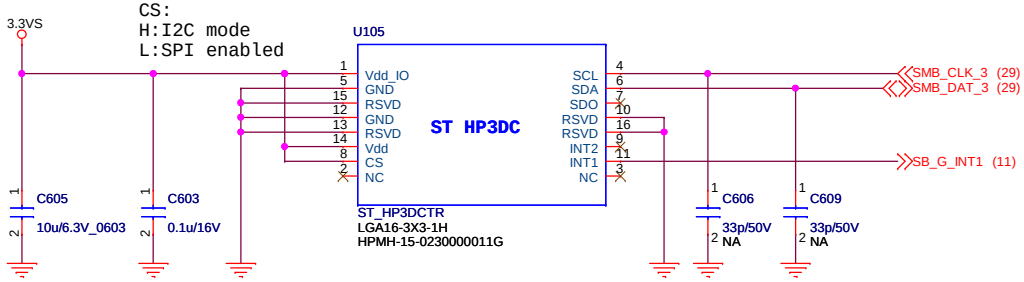


ODD Zero PWR



ME2306D:
Id = 3.9A @ 25℃
3.1A @ 70℃
Rds(on)max = 31m ohm
@ Vgs = 10V, Id = 6.7A
52m ohm
@ Vgs = 4.5V, Id = 5.0A

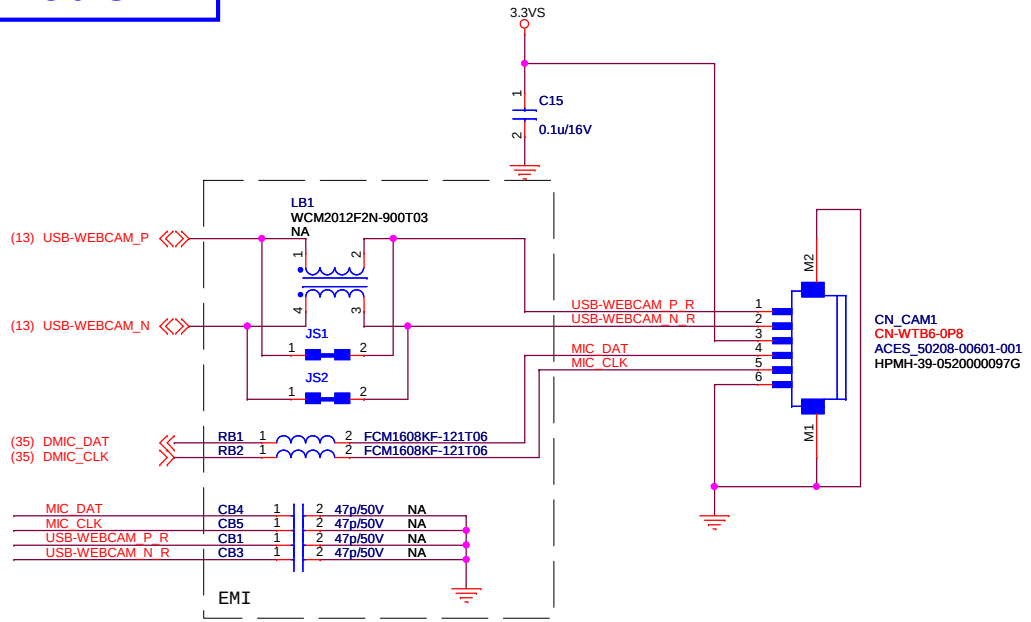
G-Sensor



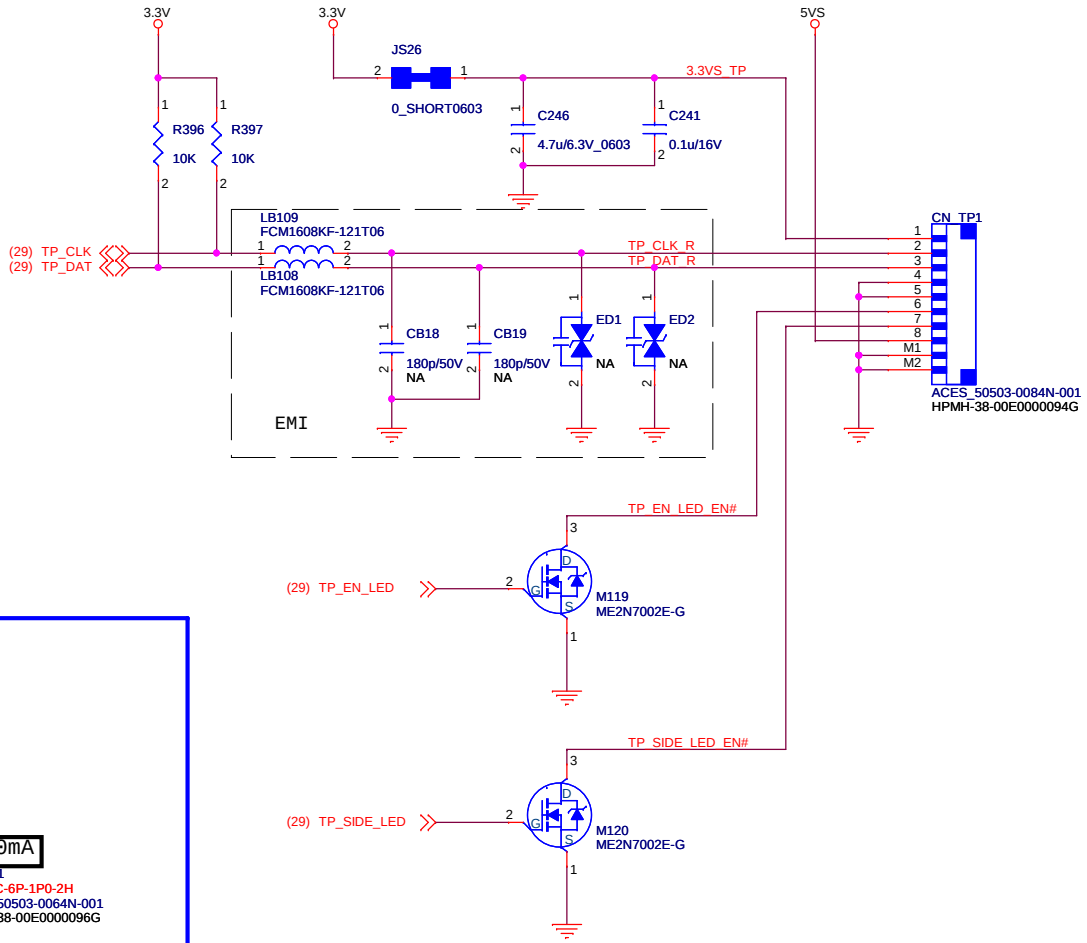
G-SENSOR - ST HP3DC
3.3VS
ADDR: 0001100x(30h) - SDO PD
ADDR: 0011101x(32h) - SDO NC
SINK: ?mA@VoL=0.33V(MAX)

FLEXComputing		
Project Name : H510UA1	Title : HDD/ ODD/ Zero PWR/ G-sensor	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 27 of 51	

Web CAM

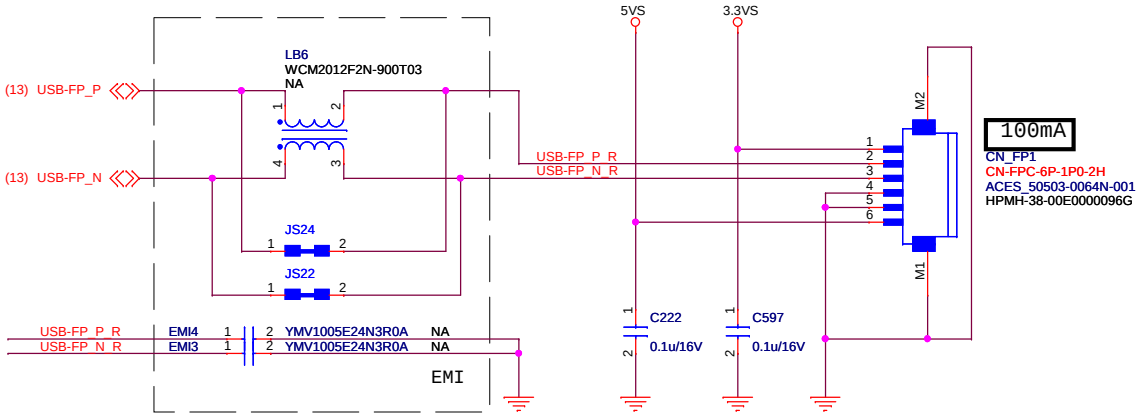


T/P



Finger Printer

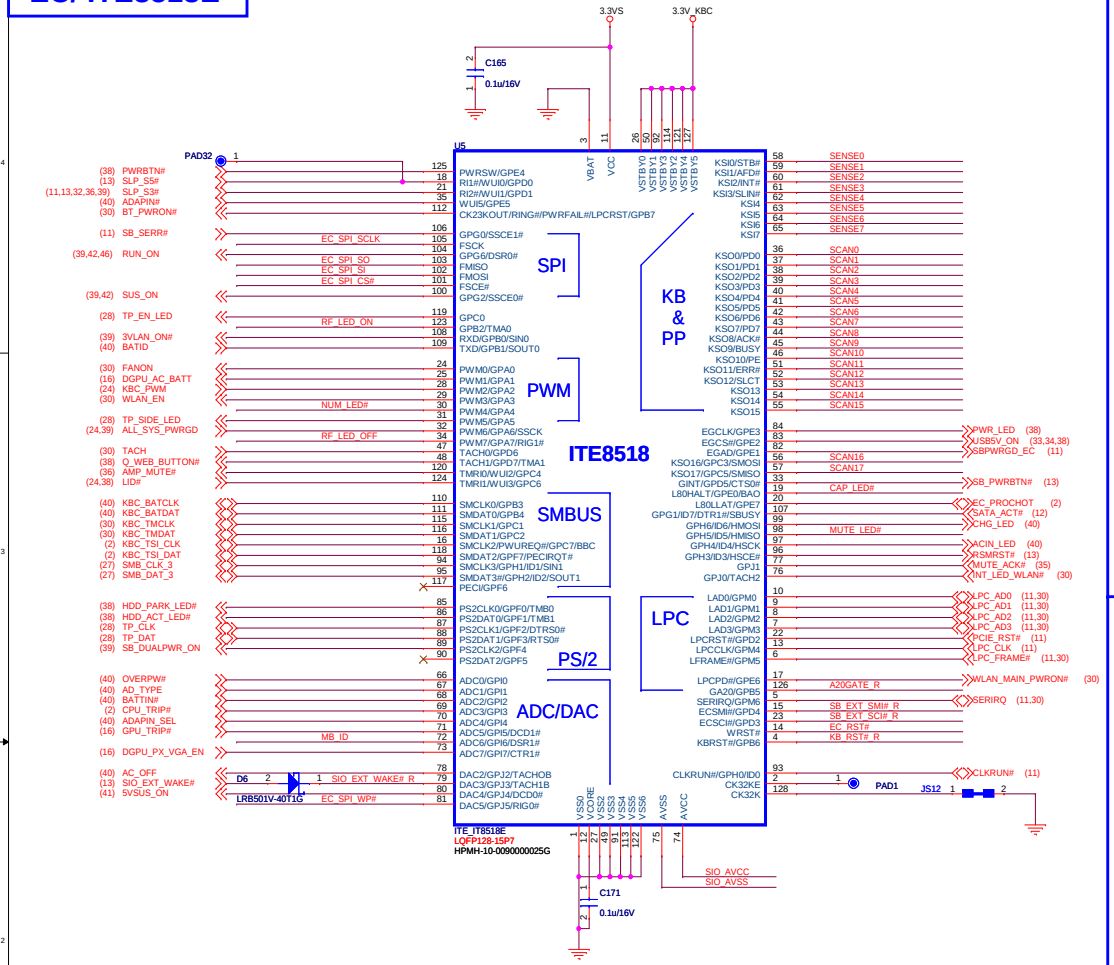
Remve Finger Printer coponents for IMR



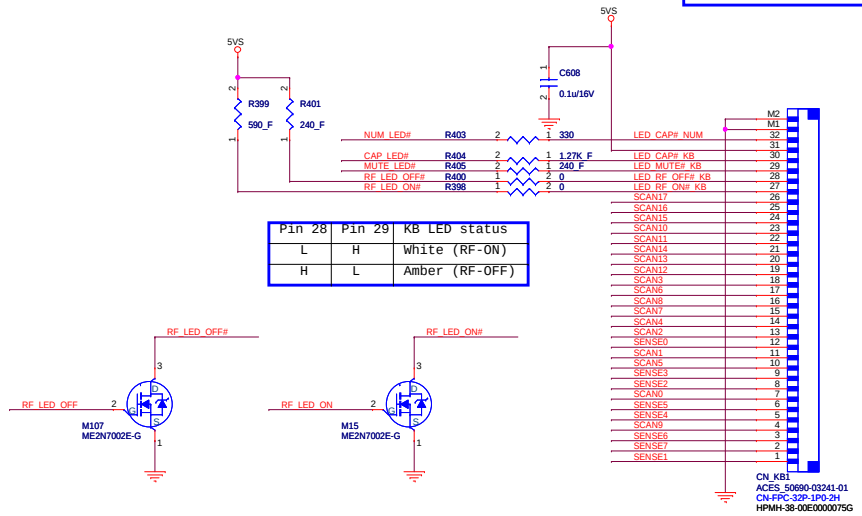
FLEXComputing

Project Name : H510UA1	Title : WebCAM/ BT/ FPt/ Touch Screen
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Thursday, December 30, 2010	Sheet : 28 of 51

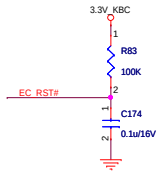
EC/ ITE8518E

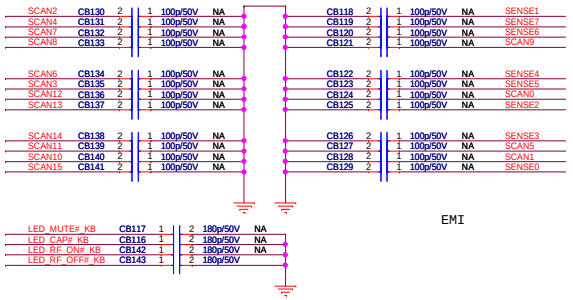


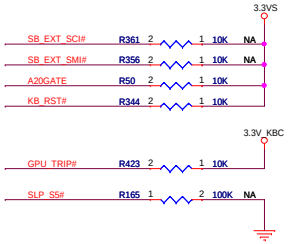
Keyboard Conn

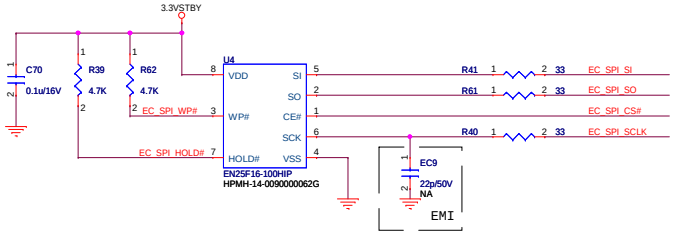


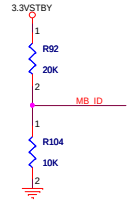
Pin 28	Pin 29	KB LED status
L	H	White (RF-ON)
H	L	Amber (RF-OFF)

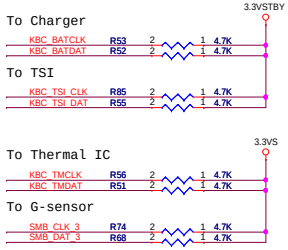


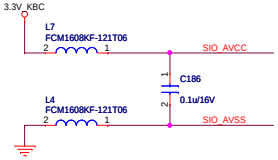


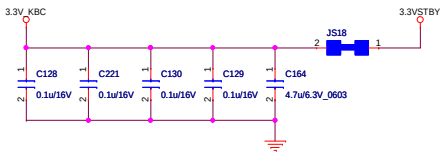


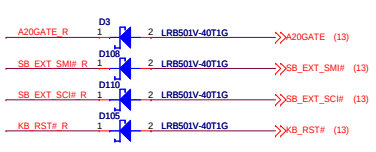












MB-ID		
3.3V	INTEL-DI	R92: 10K -- HPMH-30-301036-990G R104: NA
2.2V	INTEL-UI	R92: 10K -- HPMH-30-301036-990G R104: 20K -- HPMH-30-102036-990G
1.1V	AMD-DA	R92: 20K -- HPMH-30-102036-990G R104: 10K -- HPMH-30-301036-990G
GND	AMD-UA	R92: NA R104: 10K -- HPMH-30-301036-990G

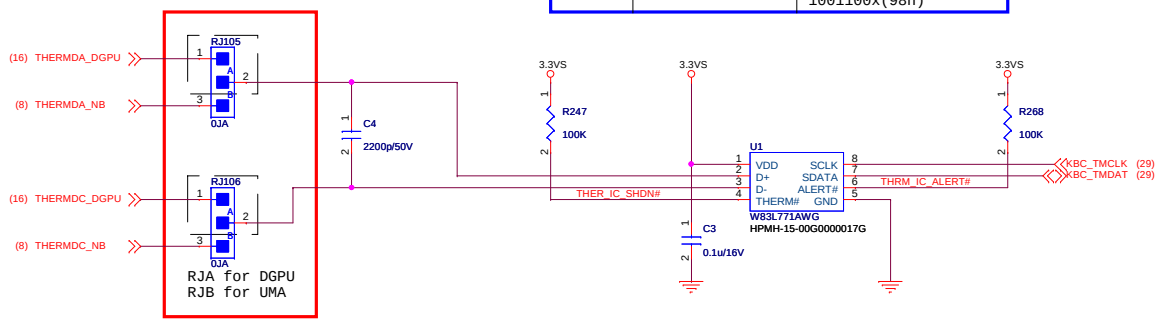
FLEXComputing

Project Name: H510UA1	Title: EC/ ITE8518E
Size:	Document Number: HPMH-40GAB6300-D Rev: D
Date: Thursday, December 30, 2010	Sheet: 29 of 51

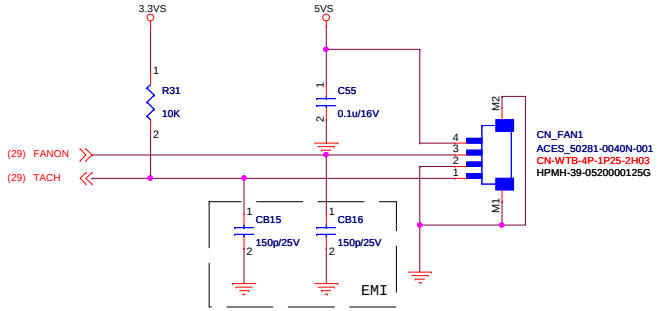
Thermal Sensor

THERMAL IC FOR CPU or DGPU

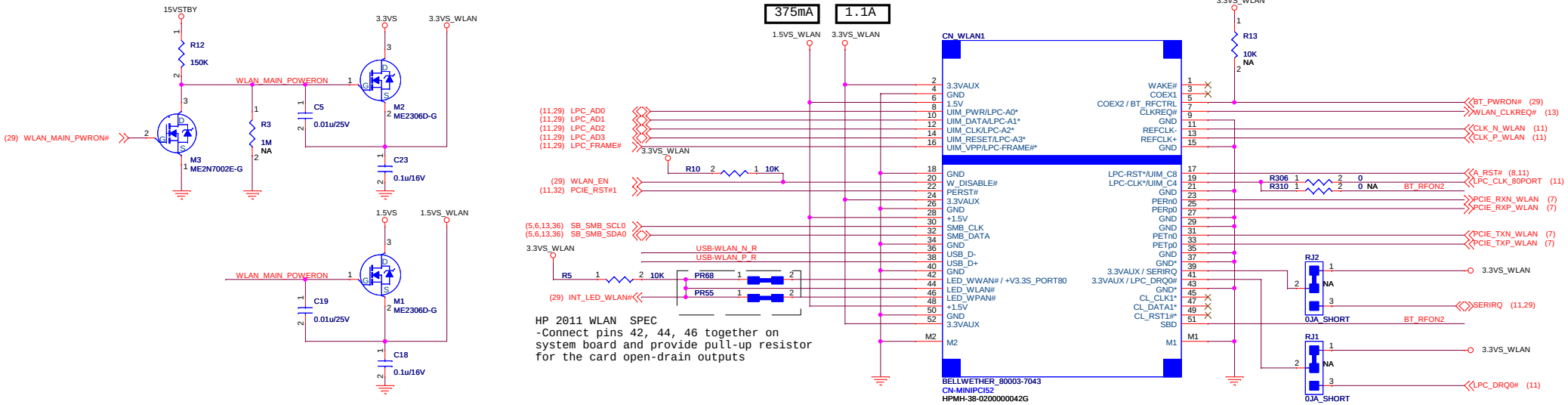
WINBOND	W83L771AWG	HPMH-15-00G0000017G 1001100x(98h)
TI	TMP431ADGKR	HPMH-15-0500000005G 1001100x(98h)



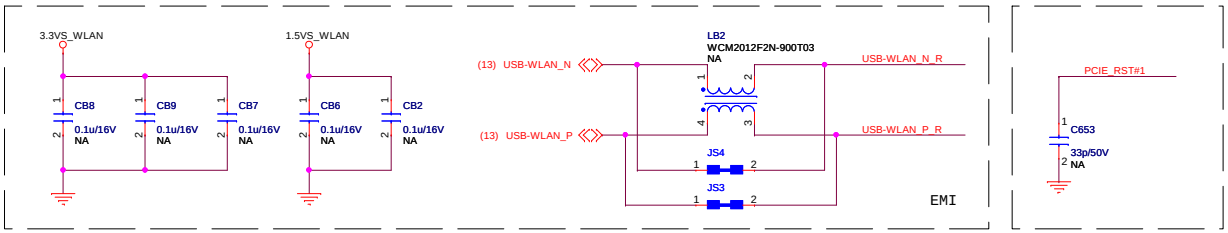
FAN

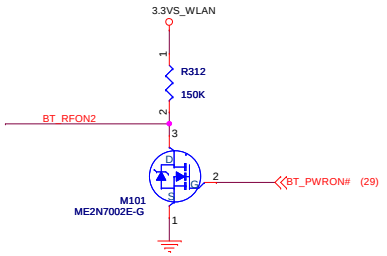


Mini PCI-E - WLAN (Half)



HP 2011 WLAN SPEC
-Connect pins 42, 44, 46 together on system board and provide pull-up resistor for the card open-drain outputs

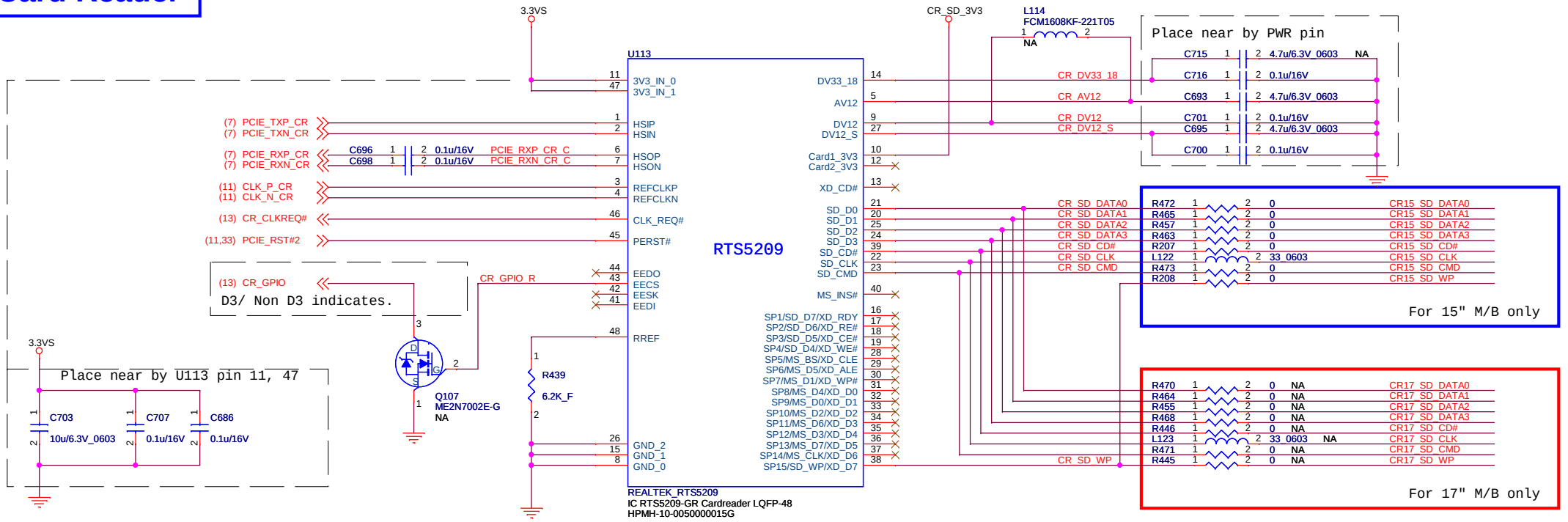




FLEX Computing

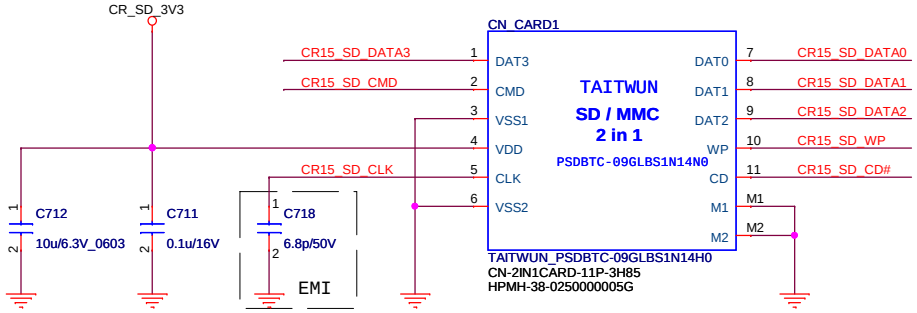
Project Name : H510UA1	Title : Thermal/ FAN/ WLAN/ HP-Logo
Size :	Document Number : HPMH-40GAB6300-D
Rev : D	
Date: Tuesday, January 11, 2011	Sheet : 30 of 51

Card Reader



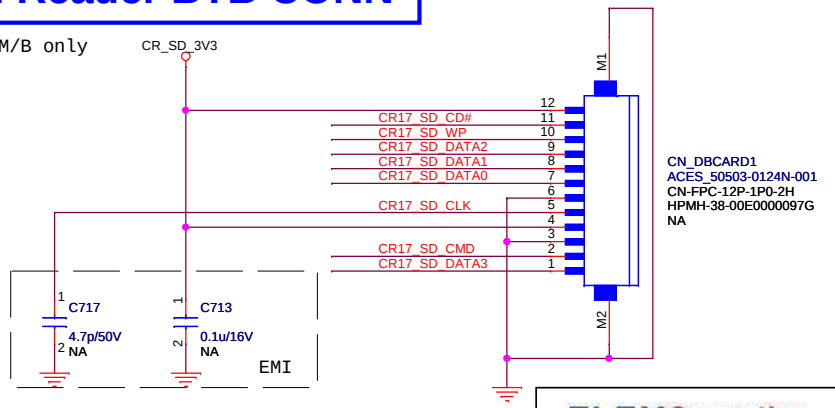
Card Reader CONN

For 15" M/B only



Card Reader BTB CONN

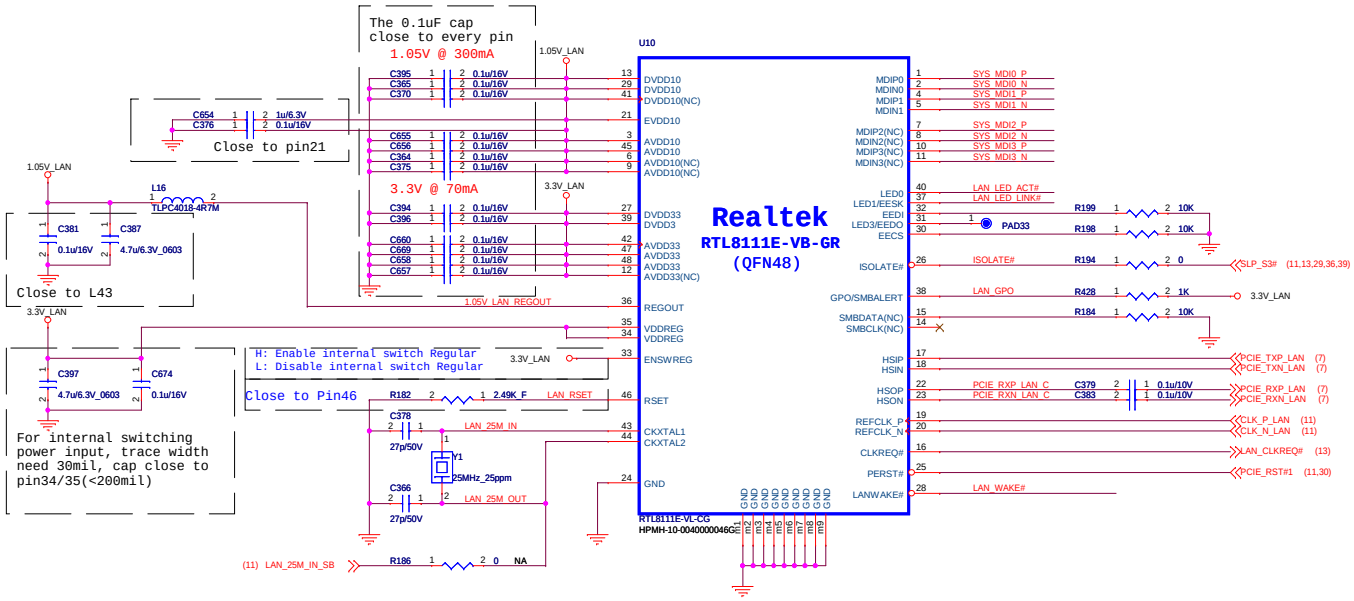
For 17" M/B only



FLEXComputing

Project Name : H510UA1	Title : Card Reader -- Realtek RTS5209
Size :	Document Number : HPMH-40GAB6300-D / Rev : D
Date: Thursday, December 30, 2010	Sheet : 31 of 51

GbLAN

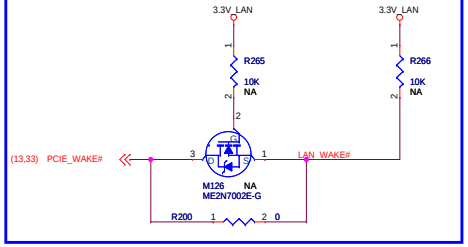


Mini-spec requirements:
10/100/1000 :
- Link :White
- Activity :Amber/Yellow

RTL8111E

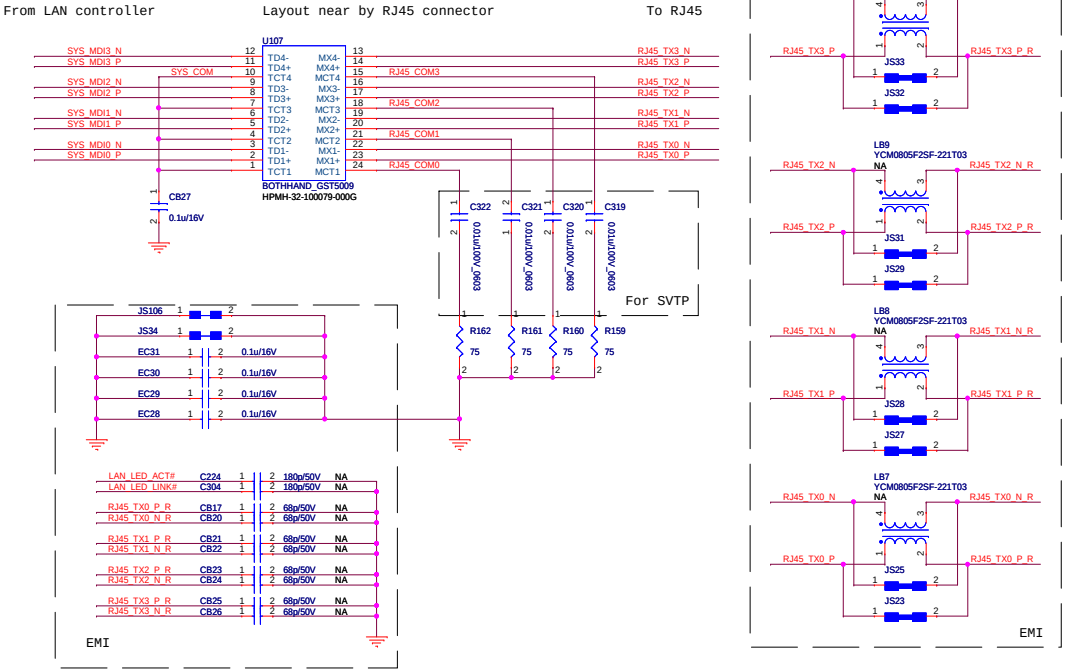
LEDS1-0	00	01	10	11
LED0	ACT ALL	LINK ALL /ACT ALL	LINK10 /ACT ALL	LINK10 /ACT10
LED1	LINK100	LINK100	LINK100	LINK100 /ACT100
LED3	LINK1000	LINK1000	LINK1000	LINK1000 /ACT1000

LEDS1-0s initial value comes from the EEPROM if there is no EEPROM, the default value is 11

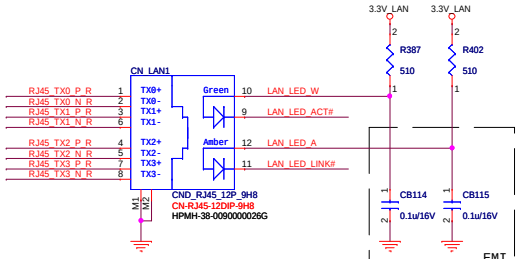


Transformer

Transformer :
Gbit P/N: 32-100079-000G(GST5009)
10/100 P/N: 32-00000000009G(TST1284)



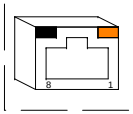
RJ45



Amber
Vf=2V If =20mA
White
Vf=3.2V If =30mA

Reference:
RJ45 Phone Jack

Pin	define:
1	TXD+0
2	TXD-0
3	TXD+1
4	TXD+2
5	TXD-2
6	TXD-1
7	TXD+3
8	TXD-3



SVTP_v4.03 - 2.6 - Ethernet Checklist - Rev C.xls

- Ch.3.1.4.4
Some older cheap RJ-45s only populate pins 1,2,3,6. 10/100 requires the other 4 pins for grounding. Gigabit Ethernet requires all 8 pins for data signals.

- Ch.3.1.4.13
Resistance from RJ-45 shell to any other chassis ground point (ohms) less than 1 ohm

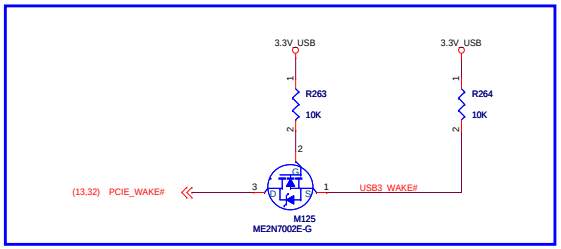
- Ch.3.1.4.14 & Ch.3.1.4.15
Protection against non-standard power-over-Ethernet (PoE) :
Resistance between pins 1,3 (TXD0P,TXD1P) and pins 4,7 (TXD2P,TXD3P) of the RJ-45 greater than 58K ohms.

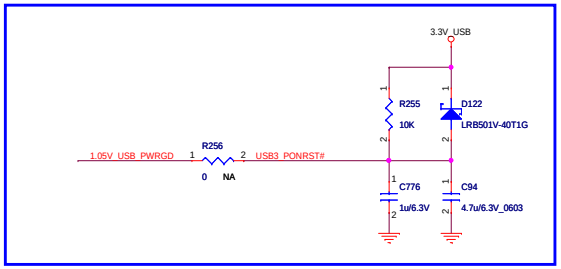
FLEXComputing

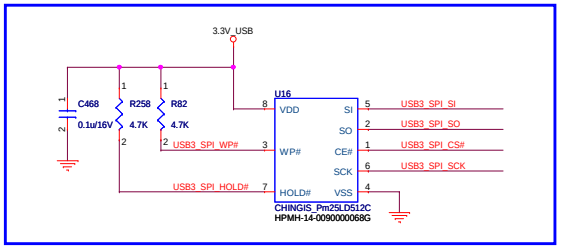
Project Name : H510UA1	Title : Gb LAN -- RL8111E-VB-GR
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 32 of 51

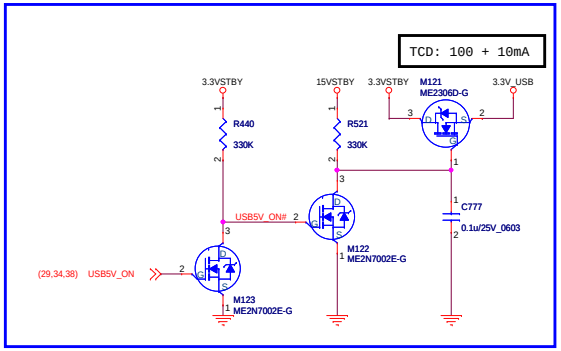
USB3.0 Controller

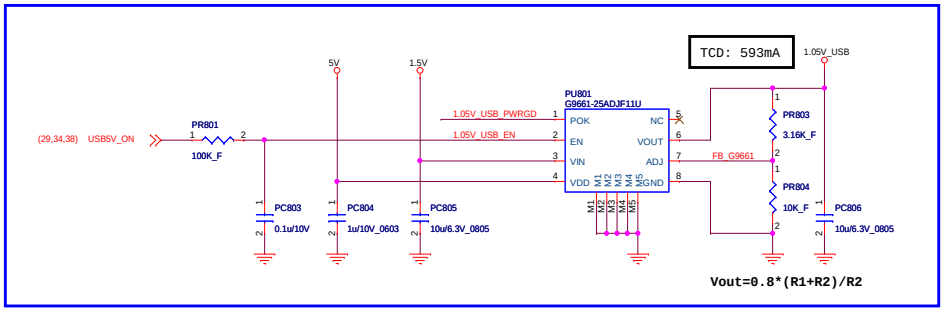
Leave empty for IMR

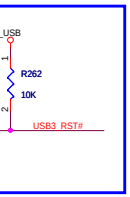


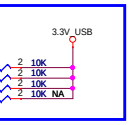


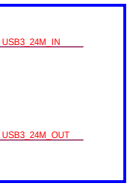


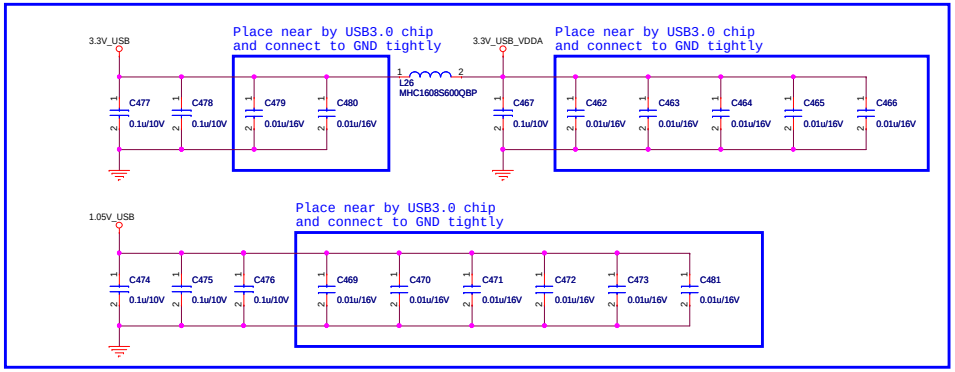








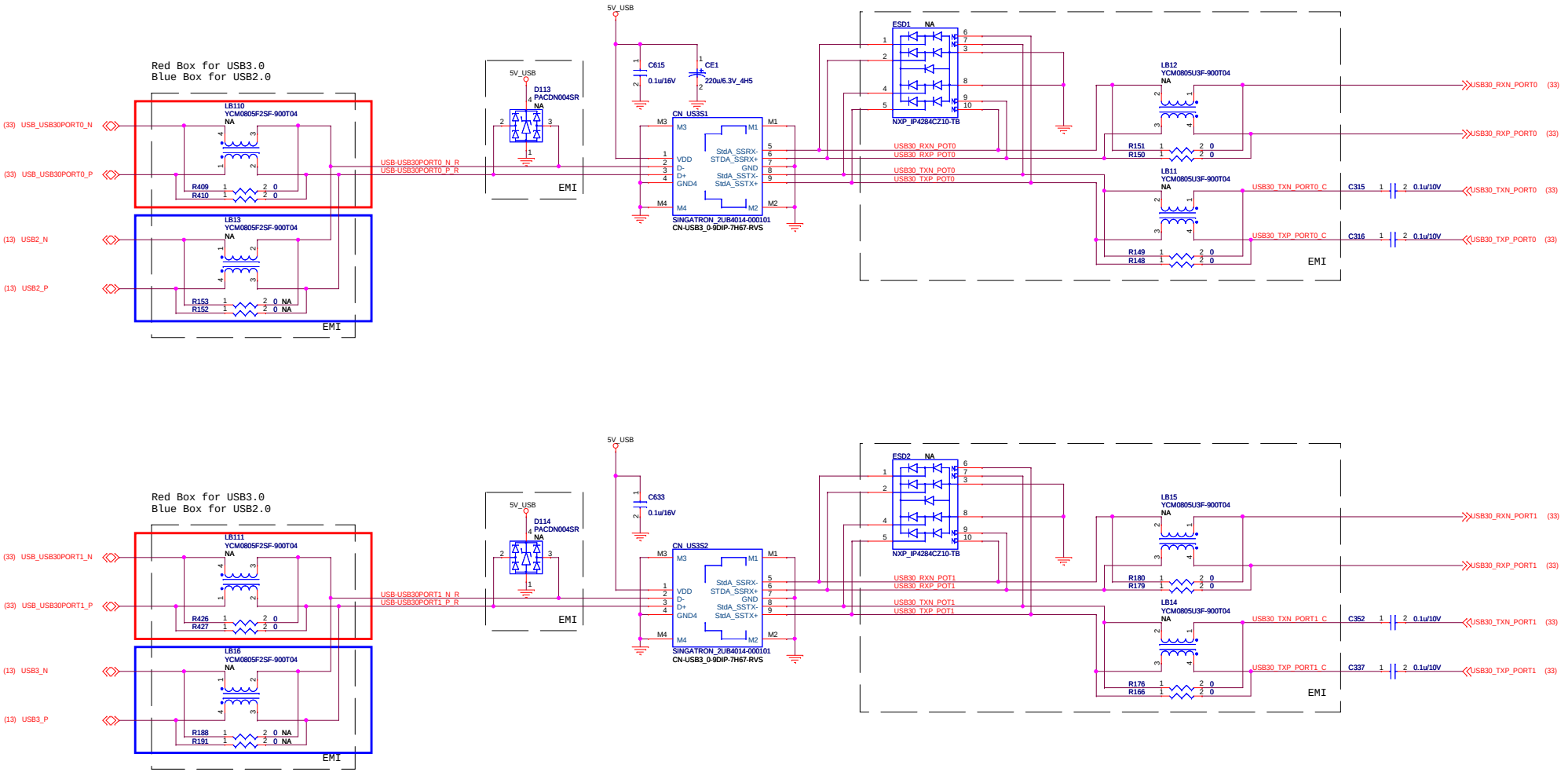




FLEX Computing

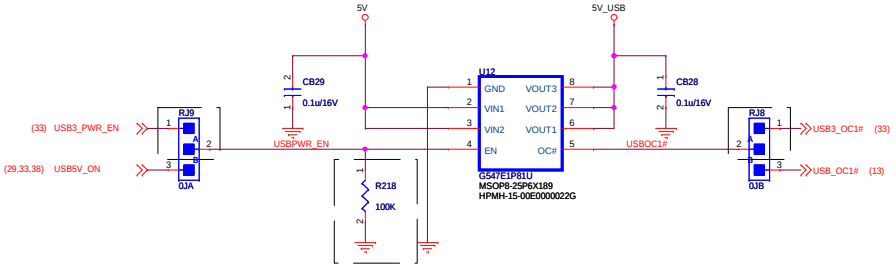
Project Name : H510UA1	Title : USB3.0 Controller -- uPD720200
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 33 of 51

USB 3.0/ 2.0



USB PWR SW

USB 3.0: RJ8& RJ9 mounted A, B.
USB 2.0: RJ8& RJ9 mounted B, B.



For disable Power SW in G3.

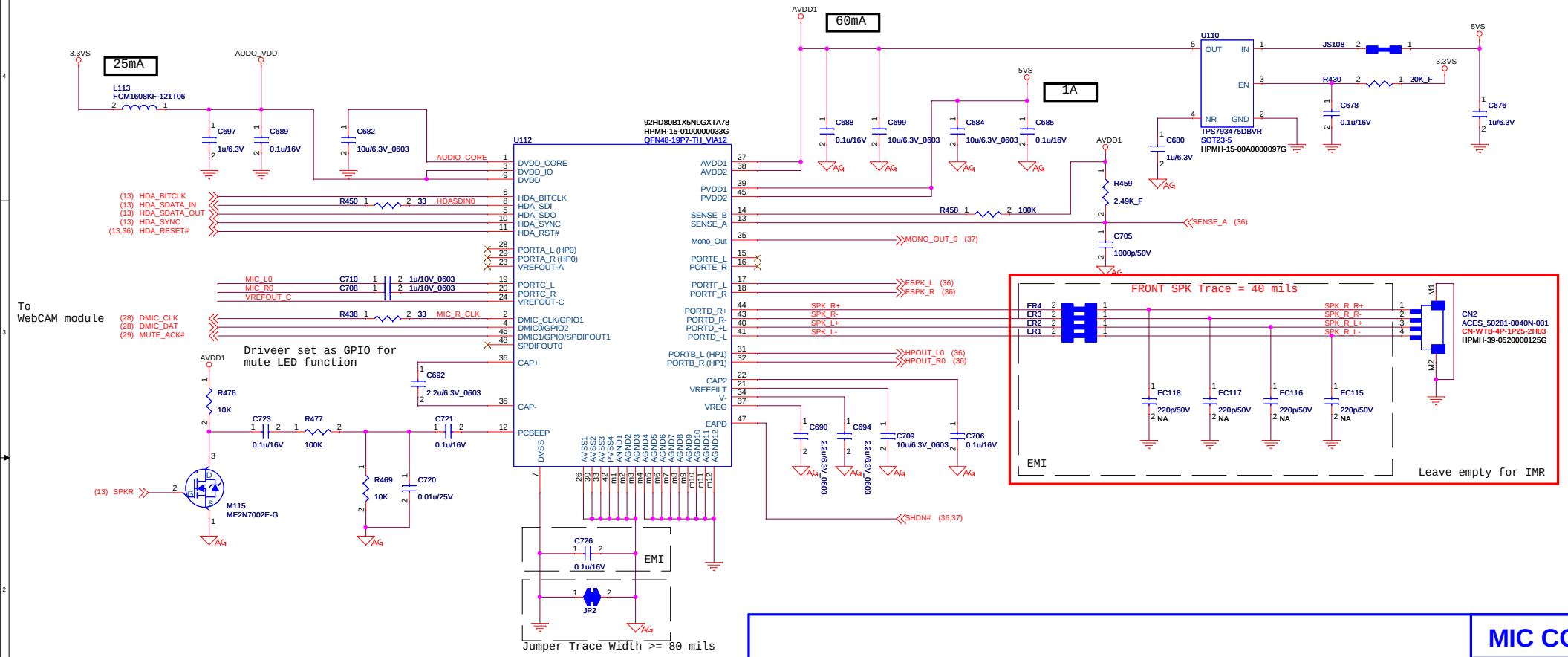
USB3.0 Conn:
- HPMH-38-00400000065G -- CONN USB 3.0 9P 2UB4014-000101 SINGATRON
- HPMH-38-00400000067G -- CONN USB 3.0 9PIN TARA7-9Y5391 ACON
- HPMH-38-00400000068G -- CONN USB 3.0 9P USBF-D9F1-ANR1-00 E-CONN
- HPMH-38-00400000088G -- CONN USB3.0 1-1932354-1 9P H:7.4mm

USB2.0 Conn:
- HPMH-38-00400000066G -- CONN USB 2.0 4P 2UB4015-000111 SINGATRON
- HPMH-38-00400000070G -- CONN USB 2.0 4PIN UARBS-4K5986 ACON
- HPMH-38-00400000071G -- CONN USB 2.0 4P USBF-D4F1-ANR1-CA E-CONN

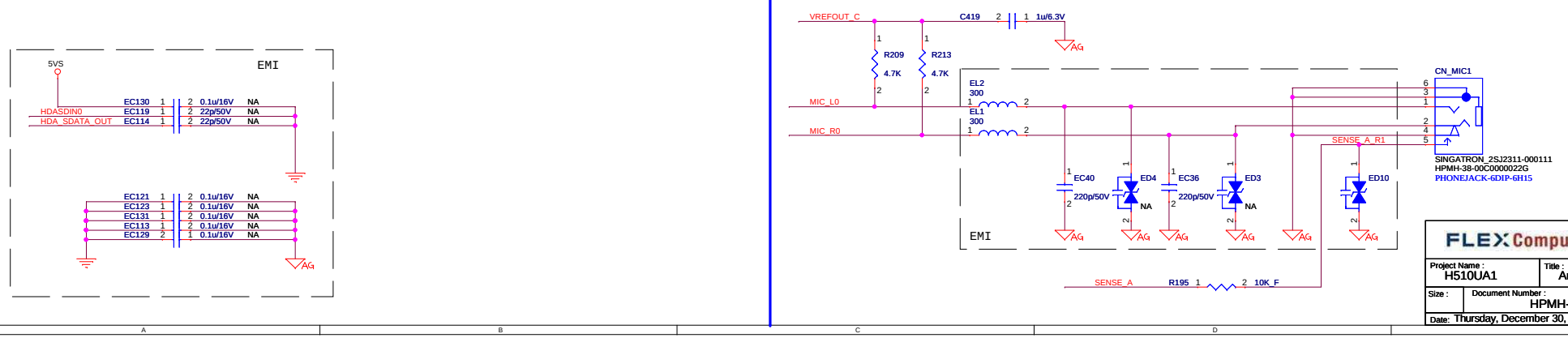
FLEXComputing

Project Name: H510UA1	Title: USB3.0 PWR/ USB I/F	
Size:	Document Number: HPMH-40GAB6300-D	Rev: D
Date: Thursday, December 30, 2010	Sheet: 34 of 51	

Audio CODEC



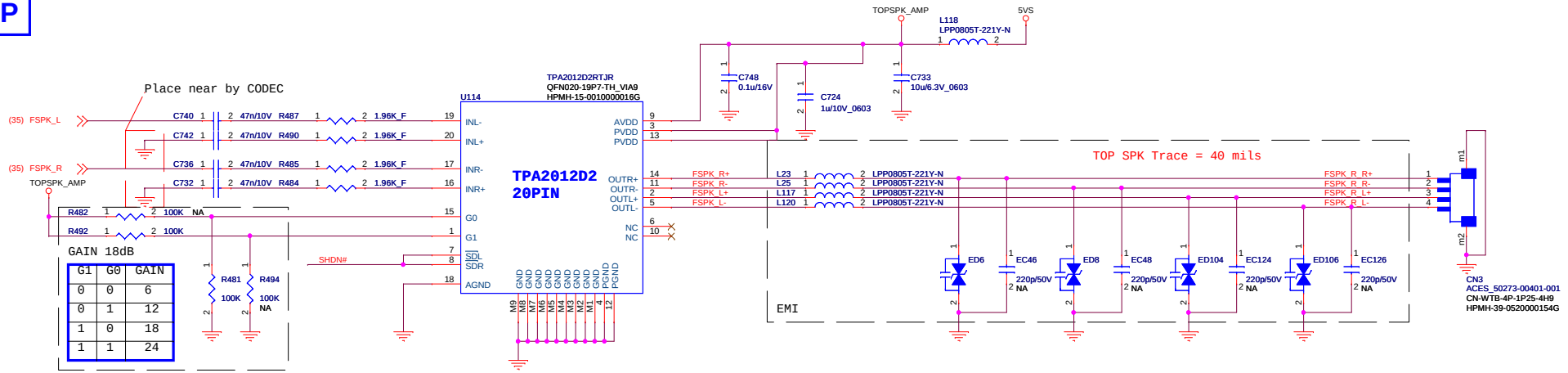
MIC CONN



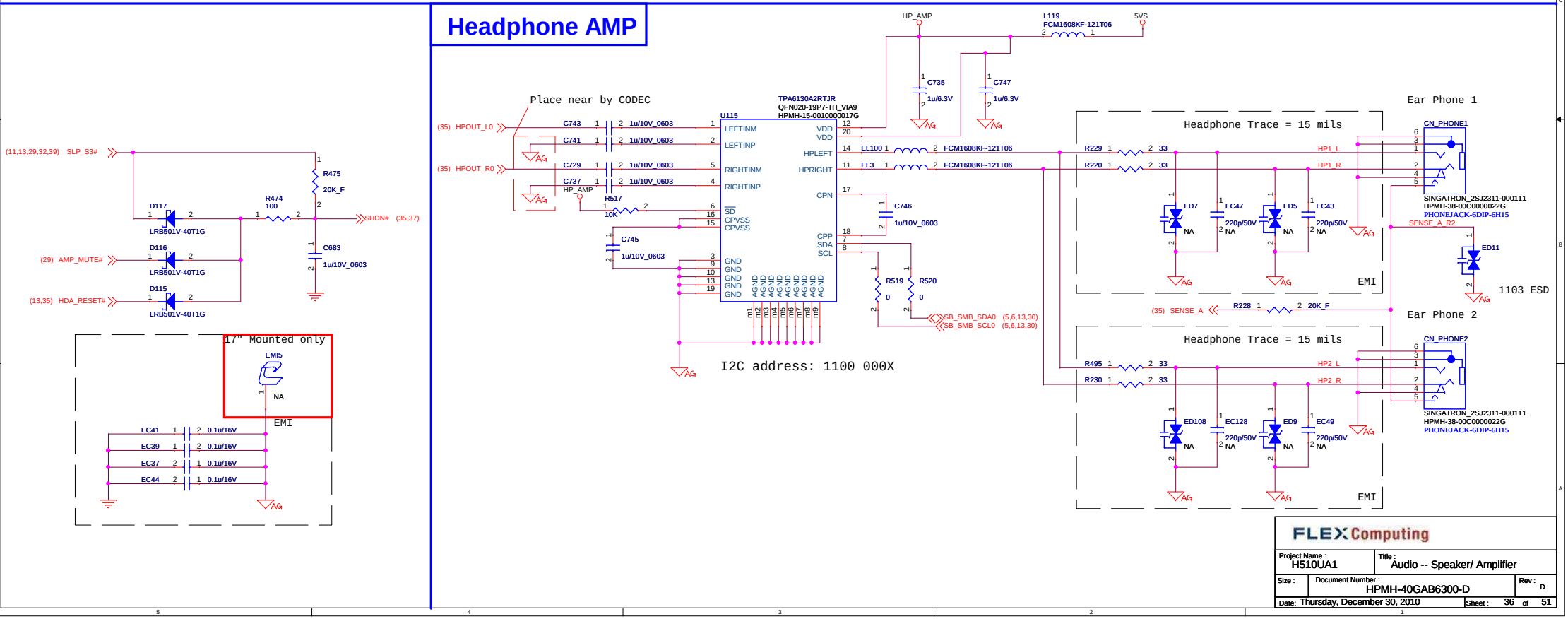
FLEX Computing

Project Name : H510UA1	Title : Audio -- IDT92HD80TA
Size :	Document Number : HPMH-40GAB6300-D
Rev : D	
Date: Thursday, December 30, 2010	Sheet : 35 of 51

FRONT SPK AMP



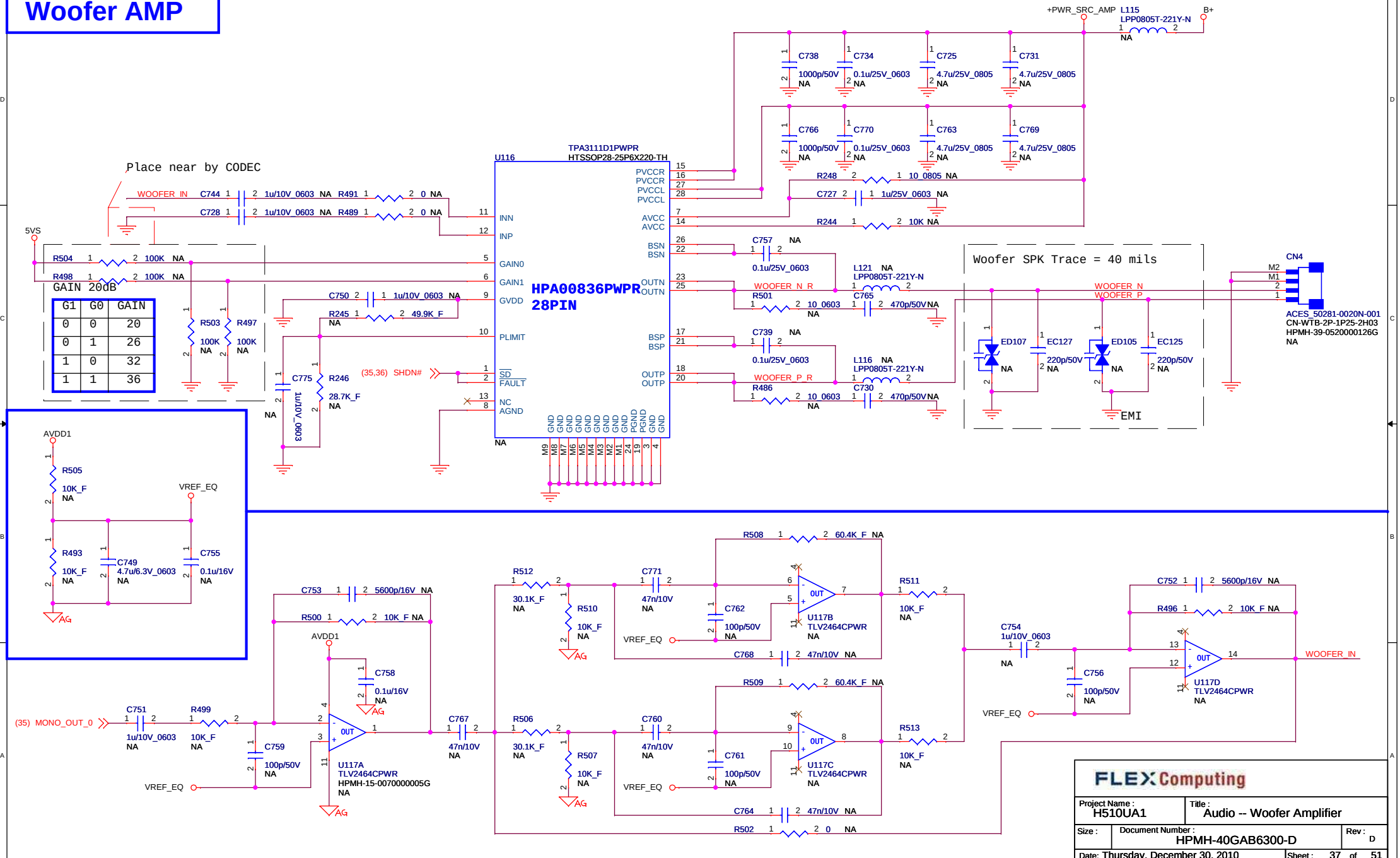
Headphone AMP



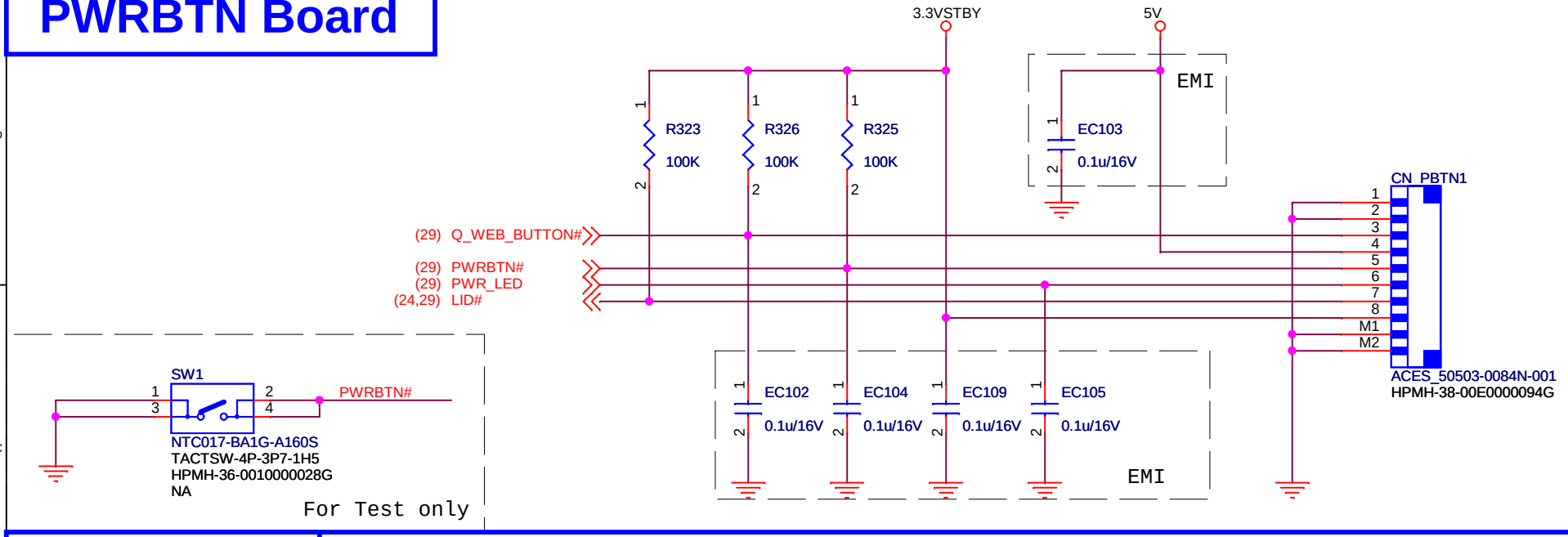
FLEX Computing

Project Name : H510UA1	Title : Audio -- Speaker/ Amplifier
Size :	Document Number : HPMH-40GAB6300-D
Rev : D	
Date: Thursday, December 30, 2010	Sheet : 36 of 51

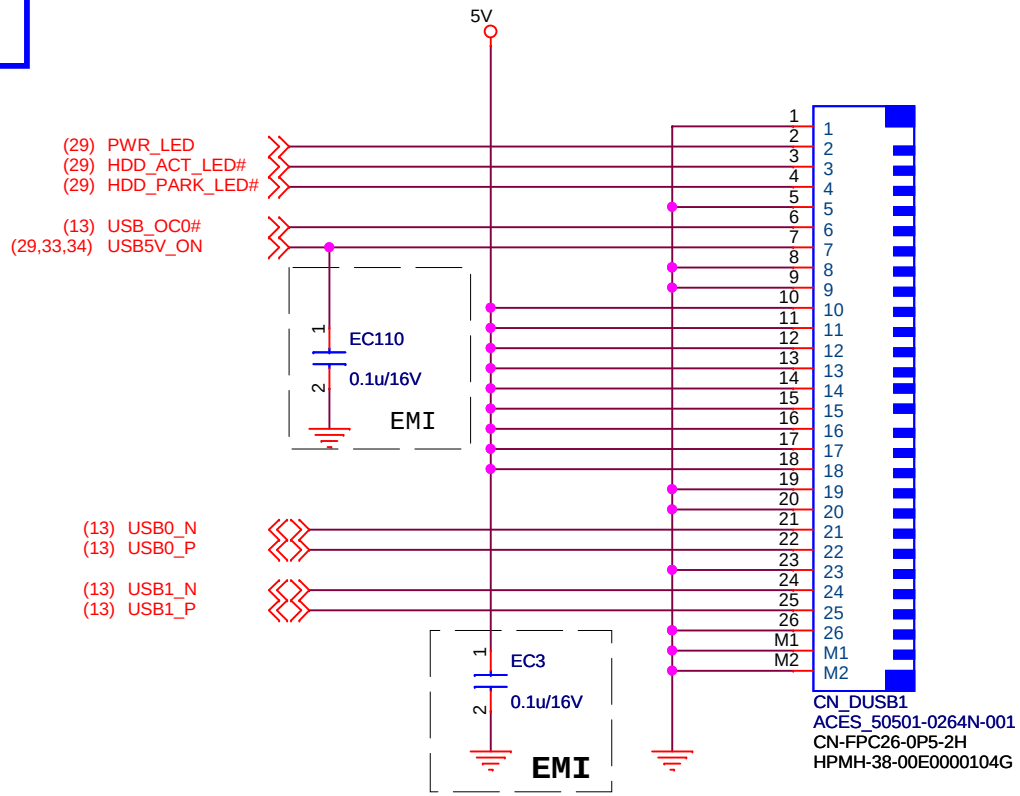
Woofer AMP


+PWR_SRC_AMP
L115
LPP0805T-221Y-N
B+
NA
C738 1000p/50V NA
C734 0.1u/25V_0603 NA
C725 4.7u/25V_0805 NA
C731 4.7u/25V_0805 NA
C766 1000p/50V NA
C770 0.1u/25V_0603 NA
C763 4.7u/25V_0805 NA
C769 4.7u/25V_0805 NA
R248 10_0805 NA
C727 1u/25V_0603 NA
R244 10K NA
Place near by CODEC
WOOFER_IN
C744 1u/10V_0603 NA
R491 0 NA
C728 1u/10V_0603 NA
R489 0 NA
5VS
R504 100K NA
R498 100K NA
GAIN 20dB
G1 G0 GAIN
0 0 20
0 1 26
1 0 32
1 1 36
R503 100K NA
R497 100K NA
C750 1u/10V_0603 NA
R245 49.9K_F NA
C775 1u/10V_0603 NA
R246 28.7K_F NA
(35,36) SHDN#
U116
TPA3111D1PWPR
HTSSOP28-25P6X220-TH
HPA00836PWPR
28PIN
INN
INP
GAIN0
GAIN1
GVDD
PLIMIT
SD
FAULT
NC
AGND
PVCCR
PVCCL
AVCC
BSN
OUTN
BSP
OUTP
GND
PGND
C757 0.1u/25V_0603 NA
C739 0.1u/25V_0603 NA
L121 LPP0805T-221Y-N NA
L116 LPP0805T-221Y-N NA
WOOFER_N_R
WOOFER_P_R
R501 10_0603 NA
R486 10_0603 NA
C765 470p/50V NA
C730 470p/50V NA
Woofer SPK Trace = 40 mils
ED107 NA
ED105 NA
EC127 220p/50V NA
EC125 220p/50V NA
EMI
WOOFER_N
WOOFER_P
CN4
ACES_50281-0020N-001
CN-WTB-2P-1P25-2H03
HPMH-39-0520000126G
NA
AVDD1
R505 10K_F NA
VREF_EQ
R493 10K_F NA
C749 4.7u/6.3V_0603 NA
C755 0.1u/16V NA
AG
C753 5600p/16V NA
R500 10K_F NA
C758 0.1u/16V NA
(35) MONO_OUT_0
C751 1u/10V_0603 NA
R499 10K_F NA
C759 100p/50V NA
U117A
TLV2464CPWR
HPMH-15-0070000005G
NA
C767 47n/10V NA
R512 30.1K_F NA
R510 10K_F NA
C771 47n/10V NA
C762 100p/50V NA
R508 60.4K_F NA
U117B
TLV2464CPWR
NA
C768 47n/10V NA
R511 10K_F NA
R506 30.1K_F NA
R507 10K_F NA
C760 47n/10V NA
C761 100p/50V NA
R509 60.4K_F NA
U117C
TLV2464CPWR
NA
C764 47n/10V NA
R513 10K_F NA
R502 0 NA
C754 1u/10V_0603 NA
C756 100p/50V NA
C752 5600p/16V NA
R496 10K_F NA
U117D
TLV2464CPWR
NA
WOOFER_IN
FLEXComputing
Project Name : H510UA1
Title : Audio -- Woofer Amplifier
Size :
Document Number : HPMH-40GAB6300-D
Rev : D
Date: Thursday, December 30, 2010
Sheet : 37 of 51

PWRBTN Board



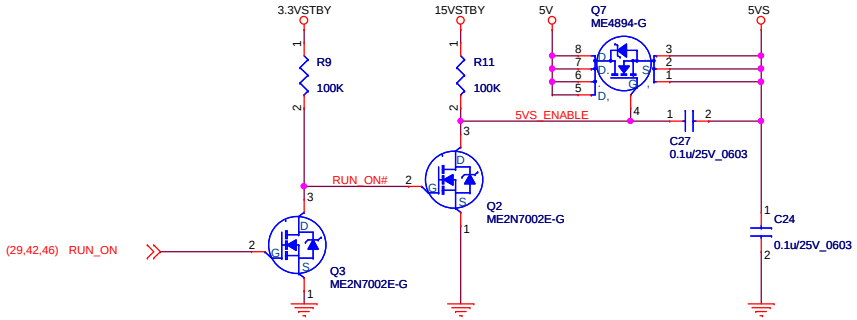
USB Board

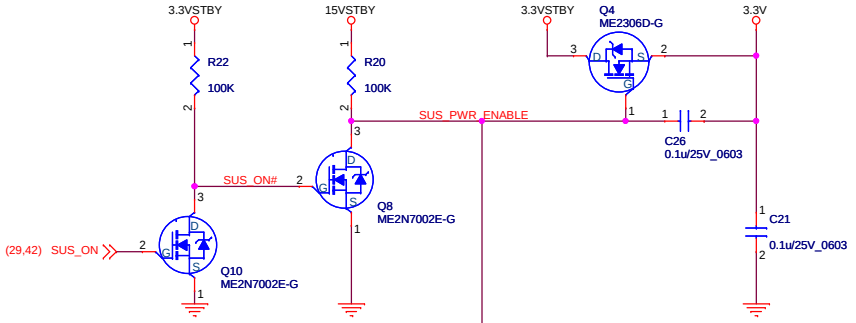


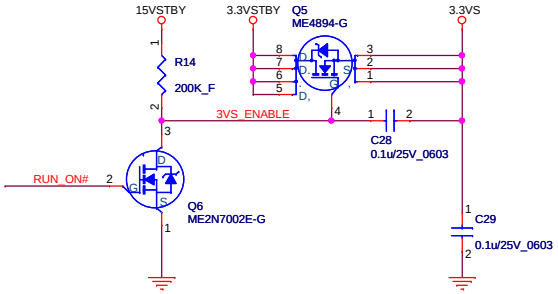
FLEXComputing

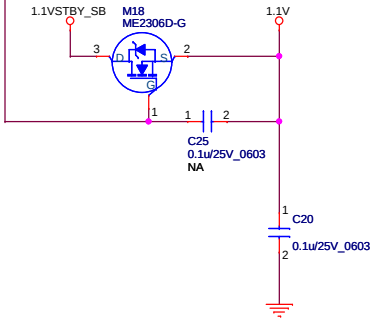
Project Name : H510UA1	Title : Daughter Board Connector	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 38 of 51	

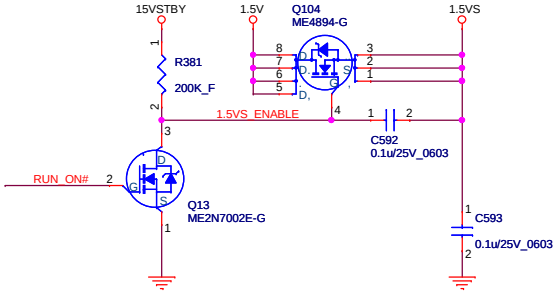
RUN/ SUS PWR

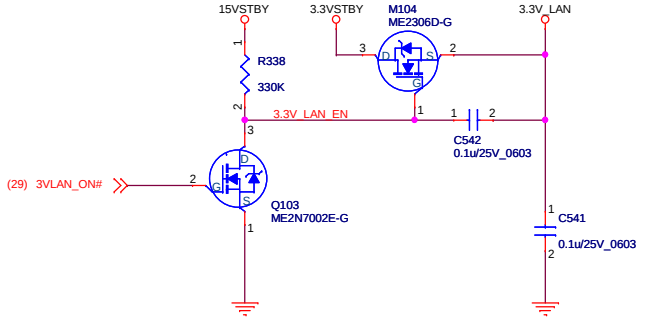


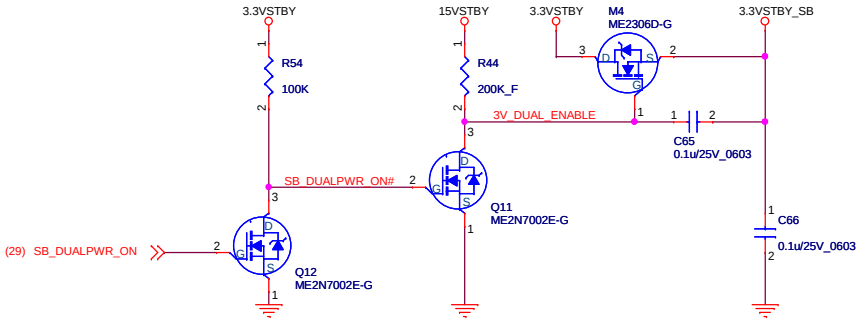




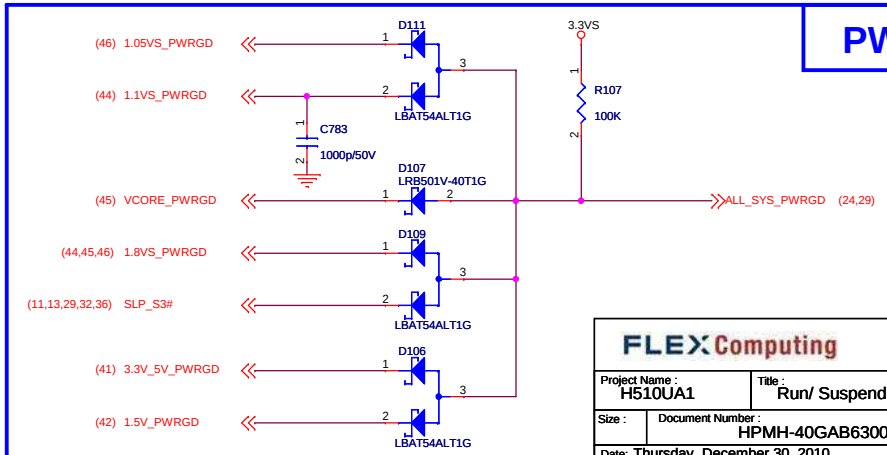








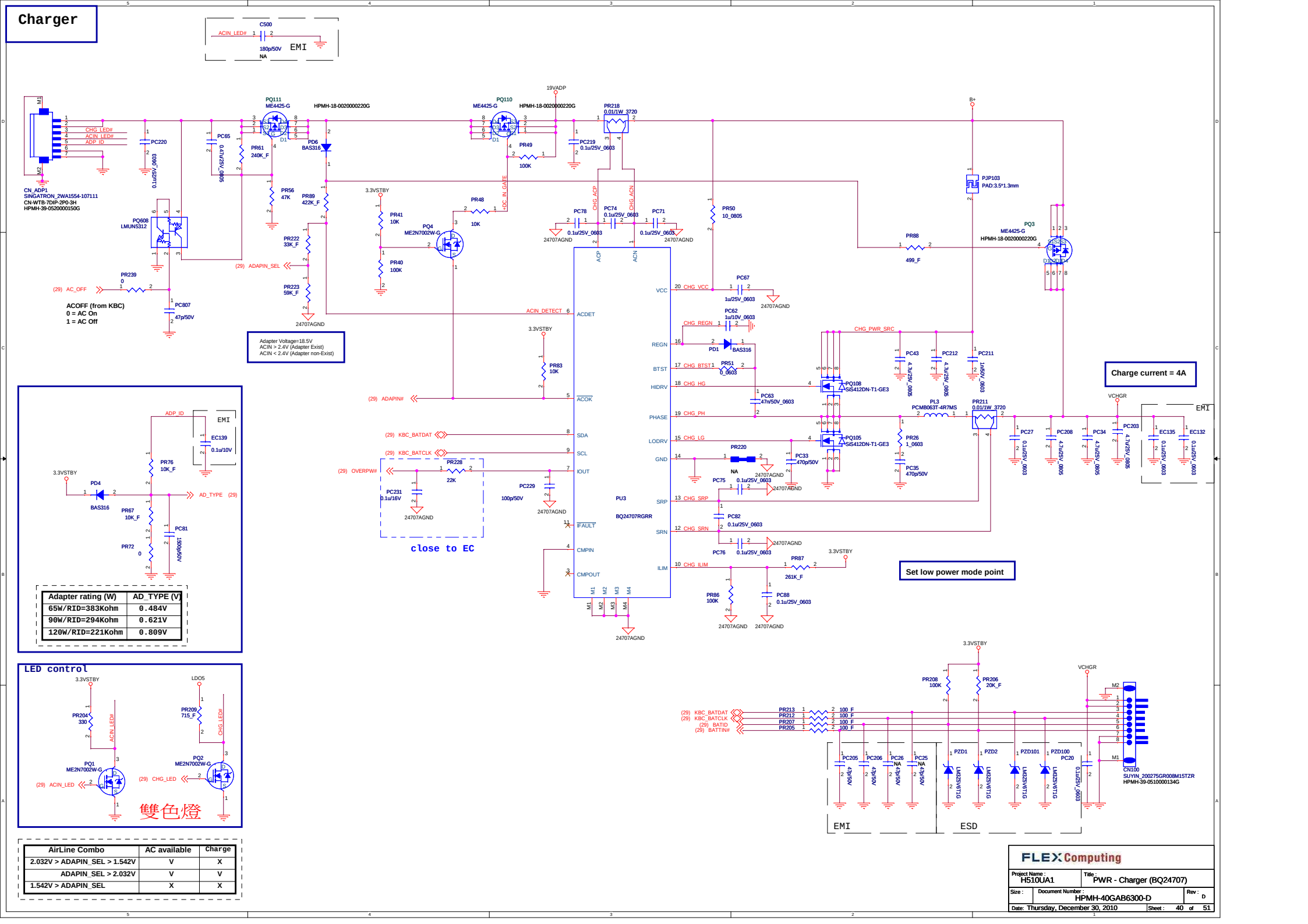
PWRGD



FLEX Computing

Project Name : H510UA1	Title : Run/ Suspend PWR switch
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 39 of 51

Charger



FLEX Computing

Project Name : H510UA1	Title : PWR - Charger (BQ24707)
Size :	Document Number : HPMH-40GAB6300-D
Rev : D	
Date: Thursday, December 30, 2010	Sheet : 40 of 51

5V / 3.3VSTBY

Freq= 365KHz
TDC = 6 A
OCP = 10 A

Freq = 460KHz
TDC = 4 A
OCP = 5.7A

PU4
TPS51125RGER

5V/3.3VSTBY ON

TRIP 3V

TRIP 5V

ENTrip floating active

Vo=(1+R1/R2)*2
(1+34.8K/22K)*2= 5..164V

Vo=(1+R1/R2)*2
= (1+13/20)*2 = 3.3V

NA by 0730

VREG5 : 5V -> 365KHz , 3.3V -> 460KHz
VREG3: 5V -> 300KHz , 3.3V -> 375KHz

QFN024-19P7-TH_VIA4

PU4-m1
For layout request, no connect anything.

+15V Charge pump

0910 Neo

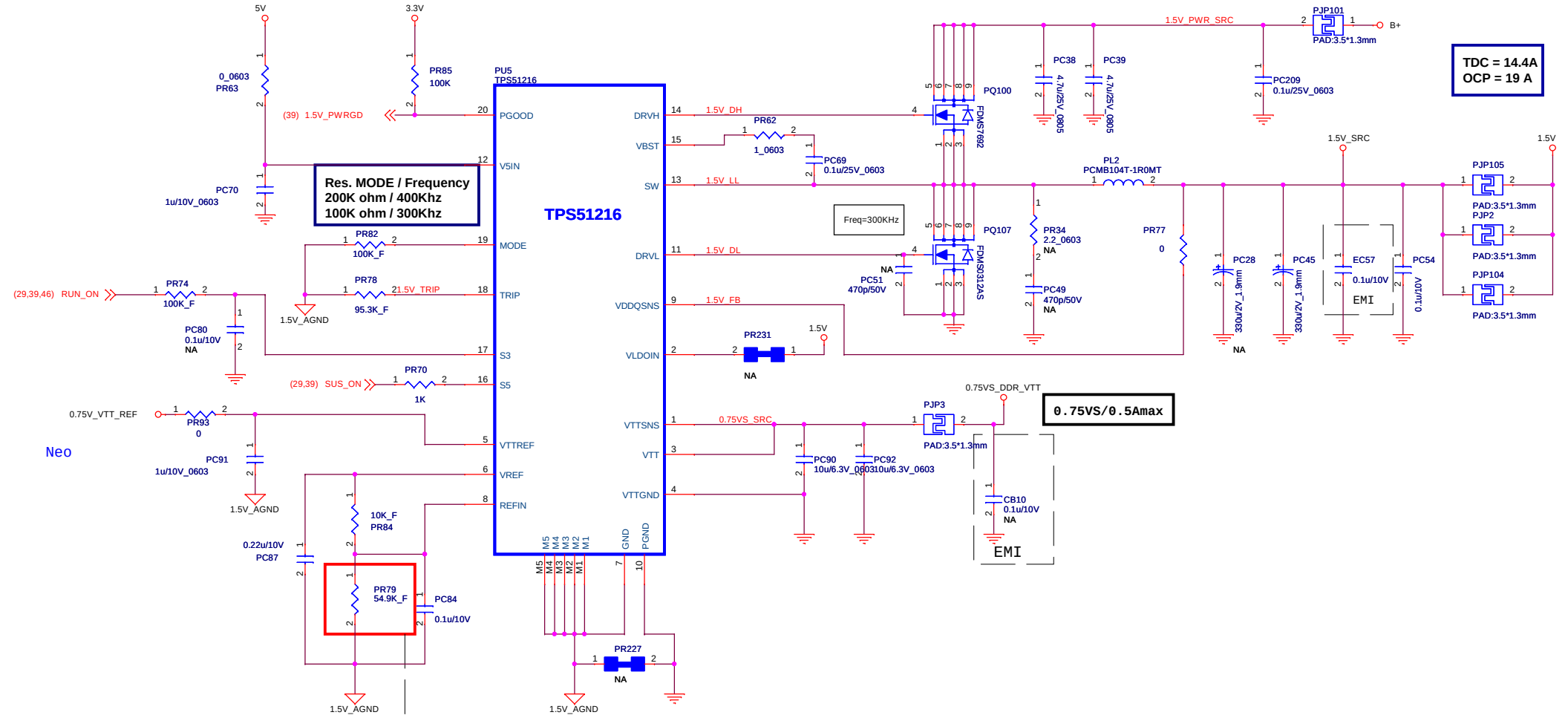
Table 3. Enabling State

EN0	ENTRIP1	ENTRIP2	VREF	VREG5	VREG3	CH1	CH2	VCLK
GND	Don't Care	Don't Care	Off	Off	Off	Off	Off	Off
R to GND	Off	Off	On	On	On	Off	Off	Off
R to GND	On	Off	On	On	On	Off	Off	Off
R to GND	Off	On	On	On	On	Off	On	Off
R to GND	On	On	On	On	On	On	On	Off
Open	Off	Off	On	On	On	Off	Off	Off
Open	On	Off	On	On	On	On	Off	On
Open	Off	On	On	On	On	Off	On	Off
Open	On	On	On	On	On	On	On	On

FLEX Computing

Project Name : H510UA1	Title : PWR -- 3V/ 5V (TPS51125)
Size :	Document Number : HPMH-40GAB6300-D — Rev : D
Date: Thursday, December 30, 2010	Sheet : 41 of 51

1.5V



	UMA	Discret
PR79	49.9K ohm 1% HPMH-30-149921-990G	54.9K ohm 1% HPMH-30-154921-990G

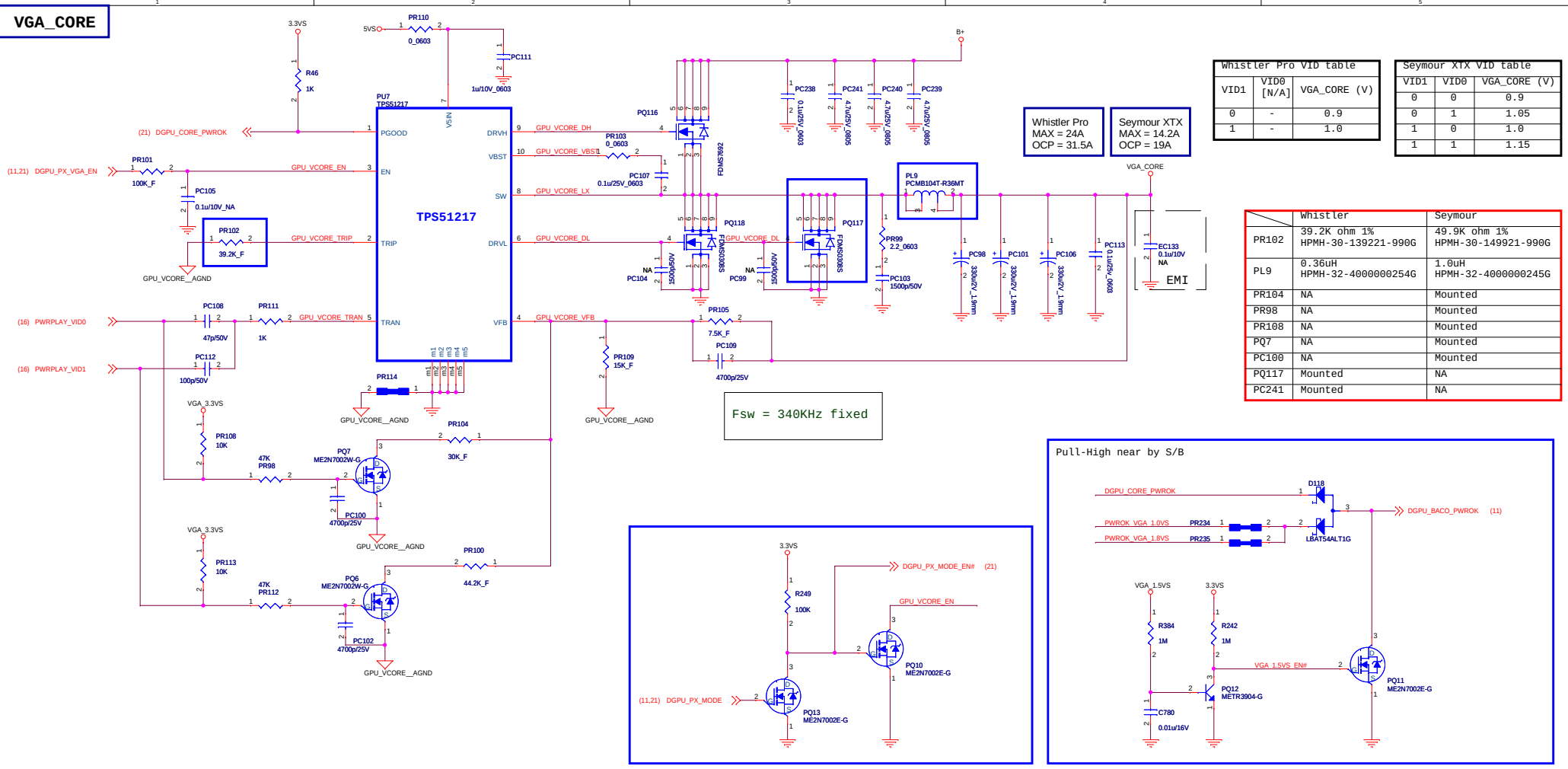
Table 1. S3 and S5 Control Table

STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3	L	H	1	0 (high~Z)
S4/S5	L	L	0 (discharge)	0 (discharge)

FLEXComputing

Project Name : H510UA1	Title : PWR -- DDR PWR (TPS51216)
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 42 of 51

VGA_CORE



Fsw = 340KHz fixed

Whistler Pro
MAX = 24A
OCP = 31.5A

Seymour XTX
MAX = 14.2A
OCP = 19A

Whistler Pro VID table

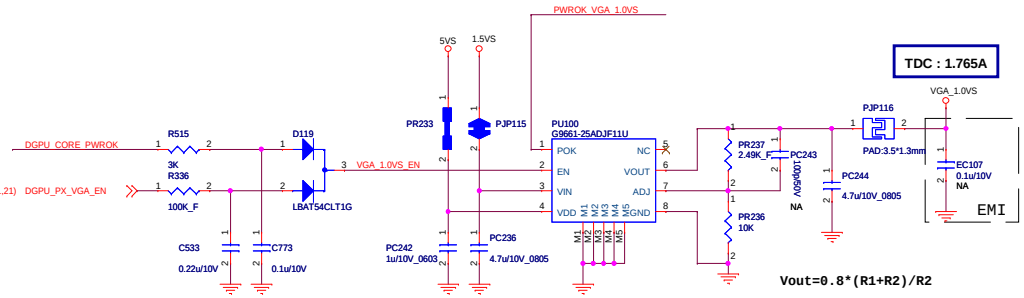
VID1	VID0 [N/A]	VGA_CORE (V)
0	-	0.9
1	-	1.0

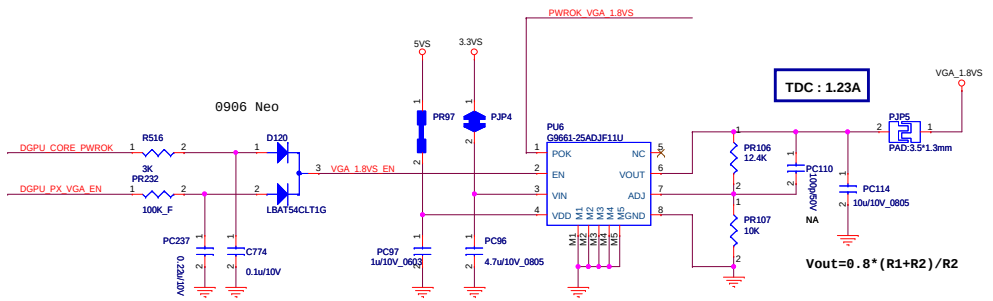
Seymour XTX VID table

VID1	VID0	VGA_CORE (V)
0	0	0.9
0	1	1.05
1	0	1.0
1	1	1.15

	Whistler	Seymour
PR102	39.2K ohm 1% HPMH-30-139221-990G	49.9K ohm 1% HPMH-30-149921-990G
PL9	0.36uH HPMH-32-4000000254G	1.0uH HPMH-32-4000000245G
PR104	NA	Mounted
PR98	NA	Mounted
PR108	NA	Mounted
PQ7	NA	Mounted
PC100	NA	Mounted
PQ117	Mounted	NA
PC241	Mounted	NA

Pull-High near by S/B

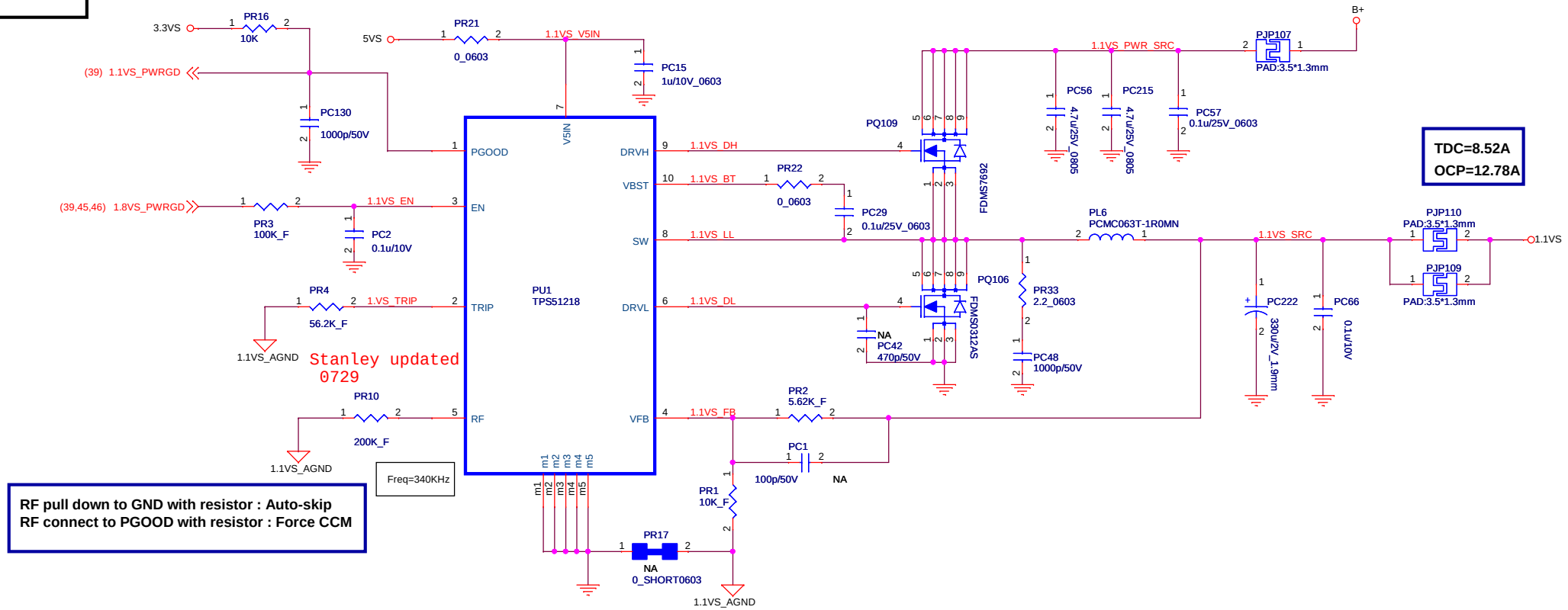




FLEX Computing

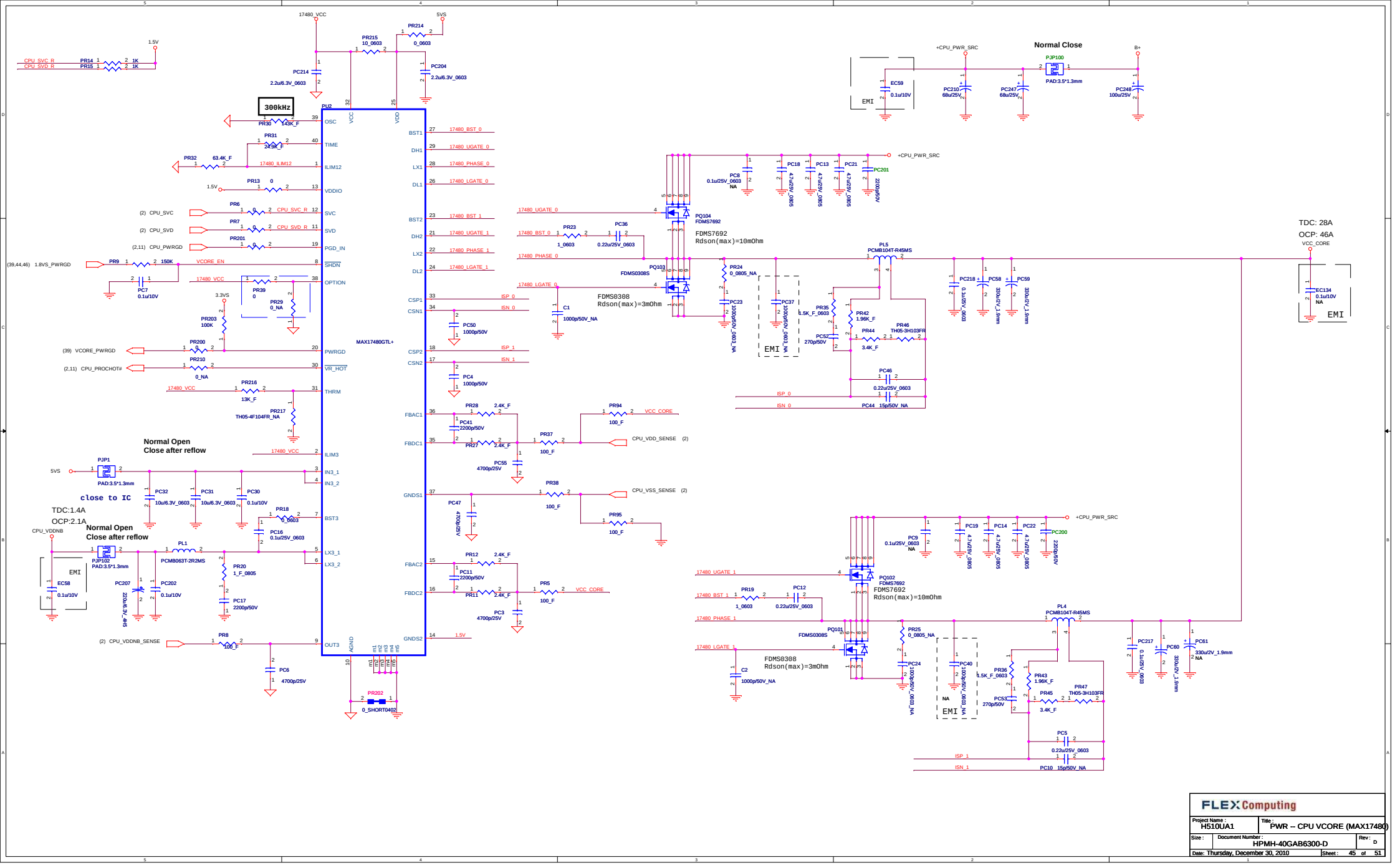
Project Name : H510UA1	Title : PWR - GPU Core (TPS51217)
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Tuesday, January 11, 2011	Sheet : 43 of 51

1.1VS



FLEX Computing

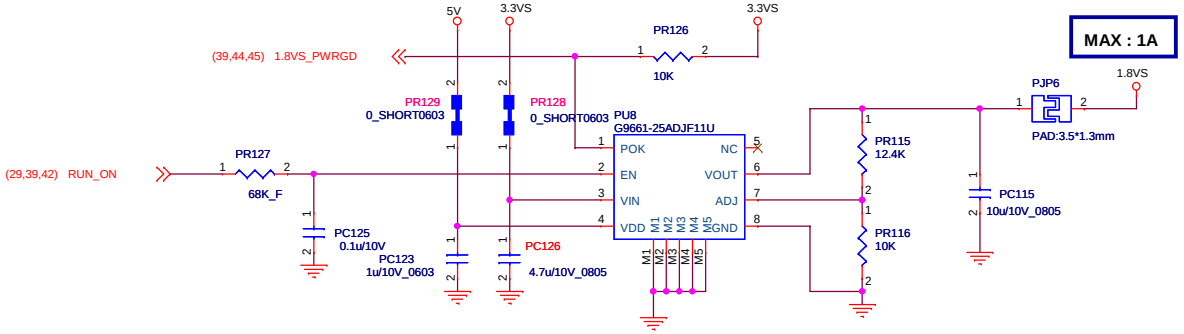
Project Name : H510UA1	Title : PWR -- 1.1VS (TPS51218)	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 44 of 51	



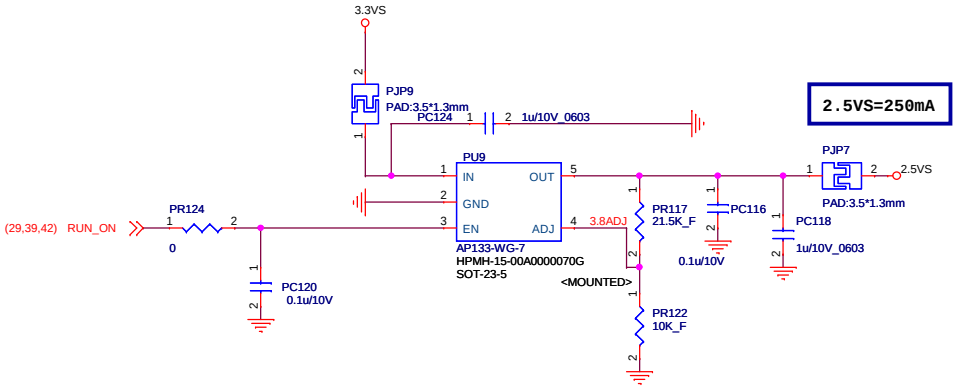
FLEX Computing

Project Name : H510UA1	Title : PWR -- CPU VCORE (MAX17480)
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 45 of 51

1.8VS

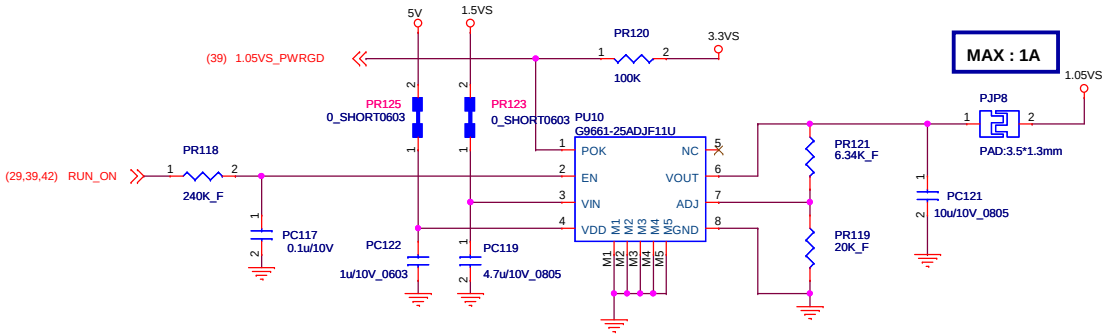


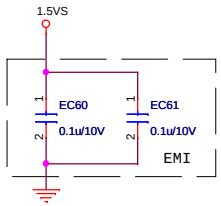
2.5VS



AP133:
Low dropout: 350mV at 300mA
EN logic low: <0.4V
EN logic high: >1.4V
Thermal shutdown: 145'C

1.05VS



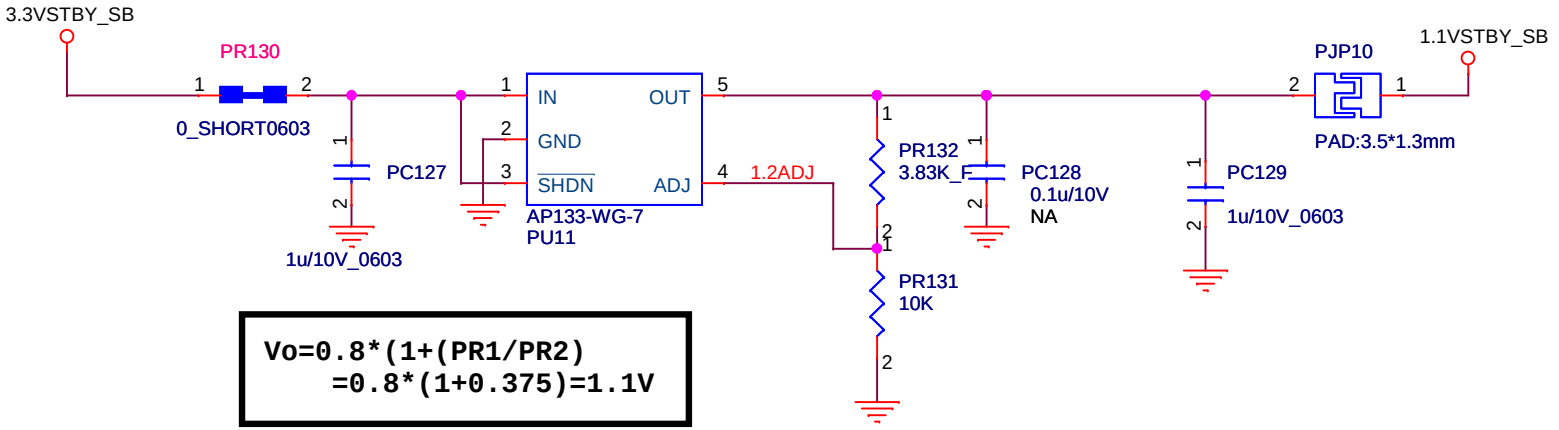


FLEX Computing

Project Name : H510UA1	Title : PWR -- 1.8VS/ 1.05VS/ 2.5VS
Size :	Document Number : HPMH-40GAB6300-D Rev : D
Date: Thursday, December 30, 2010	Sheet : 46 of 51

1.1VSTBY

1.1V_DUAL=250mA



Vo=0.8*(1+(PR1/PR2)
=0.8*(1+0.375)=1.1V

FLEX Computing

Project Name : H510UA1	Title : PWR -- 1.1VSTBY_SB (AP133)
Size :	Document Number : HPMH-40GAB6300-D / Rev : D
Date: Thursday, December 30, 2010	Sheet : 47 of 51

Screw Hole

H9 PTH6B7_2.8 THR236B276_110	H17 PTH7B8_2.8 THR276B315_110	H21 PTH7B8_2.8 THR276B315_110	H10 PTH7B4.8_3.8 THR276B189_150	H11 PTH7B4.8_3.8 THR276B189_150
H15 PTH7B4.8_3.8 THR276B189_150	H16 PTH7B4.8_3.8 THR276B189_150	H18 PTH3.1B7_2.1 THR122B276_083	H19 PTH3.1B7_2.1 THR122B276_083	H20 PTH8B7_2.8 THR315B276_110
H7 PTH3.1B7_2.1 THR122B276_083	H2 PTH8B7_2.8 THR315B276_110	H1 PTH8B7_2.8 THR315B276_110	H5 PTH7B4.8_3.8 THR276B189_150	H6 PTH7B4.8_3.8 THR276B189_150
H12 PTH7B4.8_3.8 THR276B189_150	H13 PTH7B4.8_3.8 THR276B189_150	H14 PTH7B8_2.8 THR276B315_110	H3 PTH6.8_2.8 THR268_110	H8 NPTH2.7_2.2 NPTH106X087
H22 NPTH2.2 NPTH087	H4 NPTH2.7_2.2 NPTH106X087			

EMI/ Moat CAP

B+ — EC1 1 2 0.1u/25V_0603 NA — 5V

3.3VS — EC8 1 2 0.1u/10V NA; EC13 1 2 0.1u/10V NA — 5V

3.3VS — EC101 1 2 0.1u/10V NA; EC100 1 2 0.1u/10V NA — 3.3VSTBY

1.1VS — EC112 1 2 0.1u/10V NA — VGA_1.5VS

3.3VS — EC15 1 2 0.1u/10V; EC21 1 2 0.1u/10V; EC65 1 2 0.1u/10V; EC66 1 2 0.1u/10V

3.3VS — EC4 1 2 0.1u/25V_0603 NA; EC2 1 2 0.1u/25V_0603 — B+

1.1VS — EC16 1 2 0.1u/10V; EC17 1 2 0.1u/10V; EC108 1 2 0.1u/10V

3.3VS — EC20 1 2 0.1u/10V NA; EC19 1 2 0.1u/10V NA — 1.1VS

1.1VS — C17 1 2 0.1u/10V; C22 1 2 0.1u/10V; C178 1 2 0.1u/10V

1.1VS — EC32 1 2 0.1u/10V NA; EC27 1 2 0.1u/10V NA — VGA_1.5VS

1.5V — EC12 1 2 0.1u/10V; EC6 1 2 0.1u/10V; EC11 1 2 0.1u/10V; EC5 1 2 0.1u/10V; EC10 1 2 0.1u/10V; EC7 1 2 0.1u/10V

5V — EC142 1 2 0.1u/10V; EC122 1 2 0.1u/10V; EC120 1 2 0.1u/10V NA; EC143 1 2 0.1u/10V; EC144 1 2 0.1u/10V; EC146 1 2 0.1u/10V; EC147 1 2 0.1u/10V; EC18 1 2 0.1u/10V

1.1VS — EC34 1 2 0.1u/10V NA

3.3VSTBY — EC56 1 2 0.1u/10V NA

B+ — EC22 1 2 0.1u/25V_0603; EC42 1 2 0.1u/25V_0603; EC50 1 2 0.1u/25V_0603; EC51 1 2 0.1u/25V_0603; EC55 1 2 0.1u/25V_0603; EC52 1 2 0.1u/25V_0603; EC53 1 2 0.1u/25V_0603; EC54 1 2 0.1u/25V_0603; EC62 1 2 0.1u/25V_0603; EC64 1 2 0.1u/25V_0603; EC63 1 2 0.1u/25V_0603

+CPU_PWR_SRC — EC140 1 2 0.1u/25V_0603; EC141 1 2 0.1u/25V_0603

5V_USB — EC35 1 2 0.1u/10V NA

1.5V_SRC — EC38 1 2 0.1u/10V NA

FID

FID1	FIDUCIAL	CAD-016
FID2	FIDUCIAL	CAD-016
FID3	FIDUCIAL	CAD-016
FID4	FIDUCIAL	CAD-016
FID5	FIDUCIAL	CAD-016
FID6	FIDUCIAL	CAD-016
FID7	FIDUCIAL	CAD-016
FID8	FIDUCIAL	CAD-016

NC, NO CONNECT TO ANY.

FLEXComputing

Project Name : H510UA1	Title : Screw Hole/ EMI/ Unused	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 48 of 51	

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phase
1	Rev. A Schematic released	Rev. A Schematic released	A			A0	DB
2	Modify F1 to smaller package	Modify F1 to smaller package	B	26	Modify F1 package to "FUSE-3L4X1W8X1H".	B0	SI
3	Add resistor for CPU test point resistor.	Add resistor for CPU test point resistor.	B	2	Add R514 for 80.6 ohm.	B0	SI
4	Add thermal sensor for NB thermal diode	Prevent N/B thermal break down	B	8, 30	Add RJ105, RJ106 and C772 to seperate DGPU& NB thermal signal.	B0	SI
5	Add DGPU CRT DDC source	Add DGPU CRT DDC channel for DDC6	B	16	Add U104 DDC channel test PAD (P27, P26) of pin AJ30, AJ31 (DDC6)	B0	SI
6	Modify CRT damping components.	Improve re-work performance	B	26	Modify JS102, JS103, JS104, JS7, JS9, JS10, JS11 to R233, R234, R235, R236, R237, R238, R239	B0	SI
7	Shift LAN transformer pin signal	Correct LAN transformer pin-out	B	32	Shift U107 pin-out to meet transformer spec	B0	SI
8	Update LAN 25M net-name	Correct LAN 25M for reserved signal.	B	32	Modify LAN 25M clock from S/B and named "LAN_25M_IN_SB"	B0	SI
9	Modify USB3.0 clock request signal	Modify USB3.0 clock request signal	B	33	Delete D7 for USB 3.0 clock request work properly	B0	SI
10	Reduce CPU/ DGPU screw hole size	To meet BGA& Screw hole keeping 3mm.	B	48	Reduce H5, H6, H12, H3 (CPU), H10, H11, H15, H16 (DGPU) to 7B4.8_3.8 mm	B0	SI
11	Prevent leakage current& fine-tune PWR seq	Prevent leakage current& fine-tune PWR seq	B	34, 39, 44, 45, 46	1. Modify R423 pin 1 to 3.3VSTBY 2. Leave C25 as empty for 1.1V seq 3. Modify R44 to 200K ohm 1% for 3.3VSTBY_SB seq. 4. Add R240, R241 for waveform improve 5. Add R519, R520 to Audio SM bus reserved. 6. Modify PR118 to 240Kohm 1% for 1.05VS seq. 7. Modify PR126 to 10Kohm for 1.8VS seq. 8. Modify PR9 to 150Kohm 1% for VCORE seq. 9. Modify PR3 to 100Kohm 1% for 1.1VS seq. 10. Del R82	B0	SI
12	Remove un-used circuit	Remove function by HP requirement	B		Remove Blue tooth& Keyboard bakclight circuit	B0	SI
13	Add KBC External Wake up event	Add KBC External Wake up event	B	13, 29	Add D6 and make link "SIO_EXT_WAKE#" from U5 pin 117 to U111 pin H3.	B0	SI
14	Modify components by ME/ height limitation	Modify components by ME/ height limitation	B	11, 28, 35, 37	1. Modify CN_RTC1 to ACES - "50273-0020N", CN2 to ACES - "50273-0020N", CN4 to ACES - "50281-00201", CN_LVDS1 to ACES "50398-04001" 2. Add M119, M120 for TP EN LED& TP Sidelight LED sinker.	B0	SI
15	Modify DGPU power sequence& BACO circuit	To meet DGPU power sequence& BACO required.	B	11, 21, 43	1. Modify U111 pin AH6 as "DGPU_PX_VGA_EN" 2. Modify PR238 to 620K ohm 1%. 3. Add R243, Q14, PQ121, PC246 for VGA_3.3VS gating circuit. 4. Modify VGA_1.5VS enable signal from DGPU_PX_EN to DGPU_PX_VGA_EN. 5. Delete D6 and connect DPGU_PX_MODE to BACO circuit as enable 6. Add D118, D119, D120, PR240, R249, R515, R516, C773, C774, PC130, PQ10, PQ11, PQ12, PQ13 for VGA PWR Seq. 7. Add JP3, JP4 for BACO mode reserved. 8. Add D121, R250, PQ9, PQ11, PQ12, R242 for DGPU_BACO PWROK seq. 9. Modify DGPU_PERST# from DGPU_PX_GPIO0 and PCIE_RST# combined. Or shorted by RJ100B from DGPU_GPIO0. 10. Modify entire 3.3VS of DGPU to VGA_3.3VS. 11. Update PCIE_RST#0 reset source.	B0	SI
16	DFB update	DFB update improvement (Factory)	B	26	Modify D101 to 1N5819HW-7-F.	B0	SI
17	X'tal accuracy modify	X'tal accuracy modify	B	11	1. Modify C704, C719 to 27pF for 32.768M Hz	B0	SI
18	Seperate PCI_WAKE# from different power source	Seperate PCI_WAKE# from different power source	B	11	Add D123, R200 and pull-high to 3.3V_LAN	B0	SI
19	Add transistor for LED sinker	Add transistor for LED sinker	B	28	Add M119& M120 for LED power sinker.	B0	SI
20	Update thermal circuit	Update thermal circuit	B	30	1. Add RJ105, RJ106, R247 for DGPU& NB thermal diode switch circuit. 2. Delete R23, R25, R30, R37, R38, R42, R43, C94, D1, D2, M5, M6, Q9.	B0	SI
21	Update USB3.0 solution to NEC	Update USB3.0 solution to NEC by HP required.	B	33	Modify USB3.0 soultion to NEC uDP720200	B0	SI
22	Audio circuit modify (Kevin.Yeh)	Audio circuit modify	B	36, 37	1. Modify R484, R485, R487& R490 to 1.96K ohm 1% 2. Add R517 (10K ohm) and pull-high to "HP_AMP". 3. Add R244, R245, R246, R248, C727, C775 for B+ break down issue.	B0	SI
23	Power circuit modify (Eva.Chao)	Power circuit modify	B	40, 42, 44, 45	1. Modify PR50, PC67 from 1206 to 0805& 0603 package. 2. Modify PC45, PC207 to 220uF/ 6.3V. 3. Leave PC22, PC45& PC61 empty. 4. Add PQ608, PR239 for AC-off funtion. 5. Modify PL8 to PCMC063T-3R3MN 6. Leave PR64 empty and PR53 mouted for charge-pump states. 7. Modify PR102 to 30.1K ohm 1%. 8. Modify PR16 to 10K ohm and Add PC130 for 1.1VS_PWRGD signal quality 9. Modify PC222 for double pulse issue.	B0	SI

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phase
24	Prevent GPU ACAVIN leakage current	Prevent GPU ACAVIN leakage current	C	16	Add R352& D7 to prevent GPU ACAVIN leakage current.	C0	PV
25	Update USB3.0 circuit	Update USB3.0 circuit	C	33, 34	1. Add R263, R264& M125 for USB3.0 Wake up event. 2. Add R262& D123 for USB3.0 reset timing issue. 3. Modify L26 to package 0603 for parts lead time issue. 4. Correct Analog& Digital power source 5. Add R261 for SMI BOM option 6. Delete M17 and update power switch circuit. 7. Update U16 footprint	C0	PV
26	KBC SLP_S5# signal setting	KBC SLP_S5# signal setting	C	29	Add R165 to setting SLP_S5# GND level	C0	PV
27	Logo LED broken issue	Logo LED module didn't have current limit resistor	C	24	Add R335 for Logo LED current limit	C0	PV
28	Zero power ODD function removal	Zero power ODD function removal	C	27	Leave C652, M108, M109, Q105, Q106, R419, R424& R452 empty for Zero Power ODD function removal.	C0	PV
29	EEPROM WP#	Add EEPROM WP# from EC	C	29	Add EC pin 81 as EEPROM WP# signal for EEPROM Write Protection.	C0	PV
30	NEC USB3.0 device dispear issue	Fine-tune NEC USB3.0 power up seq	C	33	1. Add C94 for NEC uPD700200A global reset timing fine-tune 2. Add R259 as empty for CLKREQ external pull-high	C0	PV
31	GPU thermal trip normal operation status	Set GPU thermal trip normal operation status	C	2, 29	1. Add R423 for GPU thermal trip normal operation status 2. Add Q108 for CPU processor hot	C0	PV
32	Hall sensor sense issue	Hall sensor can't work fine	C	28, 38	Modify SW100, C510 to D/B and modify CN_PBTN1 to 8 pin to meet M.E. modify	C0	PV
33	PX mode GPU thermal sensor fail	EC can't check GPU thermal status	C	2, 21, 29 30	1. Remove Q101, R303 remove CPU thermal alert. 2. Add R268 pull-high at alert of thermal sensor. 3. Connect DGPU_PX_VGA_EN to EC for PX mode indicates. 4.Add Q109, R181 for thermal sensor leakage issue	C0	PV
34	Stage ID indicate	Indicate SI/ PV stage for SW	C	12	Add R461 for Stage ID (Deflaut internal PU: H-SI, L-PV)	C0	PV
35	Power seq fine-tune	Power seq fine-tune	C	33, 43	1. Modify PR801 to 100K_F for USB3.0 chip power seq 2. Modify R336, PR232 to 100K_F for VGA power seq	C0	PV
36	Power circuit modify (Staley Chiu)	Power circuit modify	C	41, 43, 44, 45, 46	1. PL8 change to 4R7 2. Leave PR66 as empty 3. PR81/ PR81 change to 22K/ 34.8K for USB port load issue 4. PR79 change to 54.9k for VRAM load issue 5. PR104 change to 30K for AMD VID Updated 6. PR100 change to 44.2k for AMD VID Updated 7. Modify MAX/OCP current text 8. Update VID table 9. PC114 change to 10u/10v0805 for Phase/Gain 10. PC222 change to 330u/2v for double purse 11. PC60 change to Panasonic source (use the same source with others) 12. Add PC247, PC248/ 68uF/25V for closing acoustic noise 13. PC115 change to 10u/10v0805 for Phase/Gain 14. PC121 change to 10u/10v0805 for Phase/Gain 15. Delete PJP114	C0	PV
37	RFI solution (Hank Tsai)	RFI solution	C	11	Modify C442, C448 to 10pF as mounted.	C0	PV
38	EMI solution (PV - Benson Ni)	Update EMI solution	C	30, 37, 38, 39, 40, 41, 42, 45, 46, 48	1. Modify CB15,CB16 as mounted. 2. Modify EC37,EC39,EC41,EC44 as mounted. 3. Modfy EC102,EC104,EC105 as mounted. 4. Add EC110/ 0.1uF bypass caps. Between USB conn pin7 (USB5V_ON) and GND. 5. Add EC139/ 0.1uF bypass caps.Between CN_ADP1 pin 5 and GND. Modify C500 as mounted. 6. Add EC138/ 0.1uF bypass caps. between 5VSTBY_SRC and GND. 7. Add EC57/ 0.1uF bypass caps. between 1.5V_SRC and GND. 8. Add EC45/ 0.1uF bypass caps. between CPU_VDDNB and GND. Add EC59/ 0.1uF bypass caps. between +CPU_PWR_SRC and GND. 9. Add EC60, EC61/ 0.1uF bypass caps. between 1.5VS and GND. 10. Modify EC5,EC6,EC7,EC10,EC11,EC12,EC108,EC122 as mounted. Add EC62, EC63, EC64/ 0.1uF bypass caps. between B+ and GND. Add EC65/ 0.1uF bypass caps. between 3.3VS and GND. Delete EC111,EC25,EC23,EC24,EC26,EC33,EC35,EC109,EC110,EC45,EC38.	C0	PV
39	ESD solution (PV - Stone Wang)	Update ESD solution	C	35, 36	1. EL1, EL2 from Bead 120ohm change to the Resistor 300ohm. 2. EC36, EC40 change to mounted. 3. Add a Varistor ED10 between CN_MIC1 pin5 and Net AGND. 4. ED3, ED4 change to 0603 Varistors. 5. Add a Varistor ED11 between CN_PHONE1 pin5 and Net AGND. 6. ED6, ED8, ED104, ED106 change to 0603 Varistors. 7. ED5, ED7, ED9, ED108 change to 0603 Varistors and keep them as empty	C0	PV

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phase
40	RTC accurcy update (BOM)	RTC accurcy update	D	11	Modify C704& C719 to 22pF and 18pF.	D0	MV
41	Prevent adaptor level fail (Power)	Prevent adaptor level fail	D	40	Modify PR89 to 422Kohm 1%	D0	MV
42	Prevent leakage current from CRT	Prevent leakage current from CRT	D	26	Add R23 as 10Kohm to prevent leakage cuurent from CRT	D0	MV
43	Fine-tune LED brightness (BOM)	Fine-tune LED brightness by HP ID	D	29	1. Modify R399 to 590ohm 1% for RF on LED 2. Modify R401 to 240ohm 1% for RF off LED 3. Modify R404 to 1.27Kohm 1% for CAP lock LED 4. Modify R405 to 240ohm 1% for MUTE LED 5. Modify PR209 to 715ohm 1% for Charger LED	D0	MV
44	S5 wake-up event leakage issue (BOM)	Prevent leakage current from pull-high resistor	D	29	Leave R356, R361 as empty to prevent it.	D0	MV
45	DFX report improvement	Meet Factory DFX checking	D	45	Modify PJP100 to Normal close footprint	D0	MV
46	EMI solution improvement	EMI solution improvement	D	48	1. Modify EC15 from between 3.3VS& 5V to 3.3VS& GND 2. Modify EC18 from between 3.3VS& 5V to 5V& GND 3. Modify EC2 from between 3.3VS& B+ to B+& GND 4. Add EC35, EC38, EC66, EC140, EC141, EC142, EC143, EC144, EC146, EC147, EC148	D0	MV