PROJECT NAME : Tulip 14",15", 17" / Van Gogh 14", 15"
PCB NO : LA-C142PR04

Dell / Compal Confidential

Schematic Document

AMD Carrizo / Carizo-L
AMD EXO XT S3(23 X 23mm)+DDR3L x4

2015-02-12 Rev: 1.0

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

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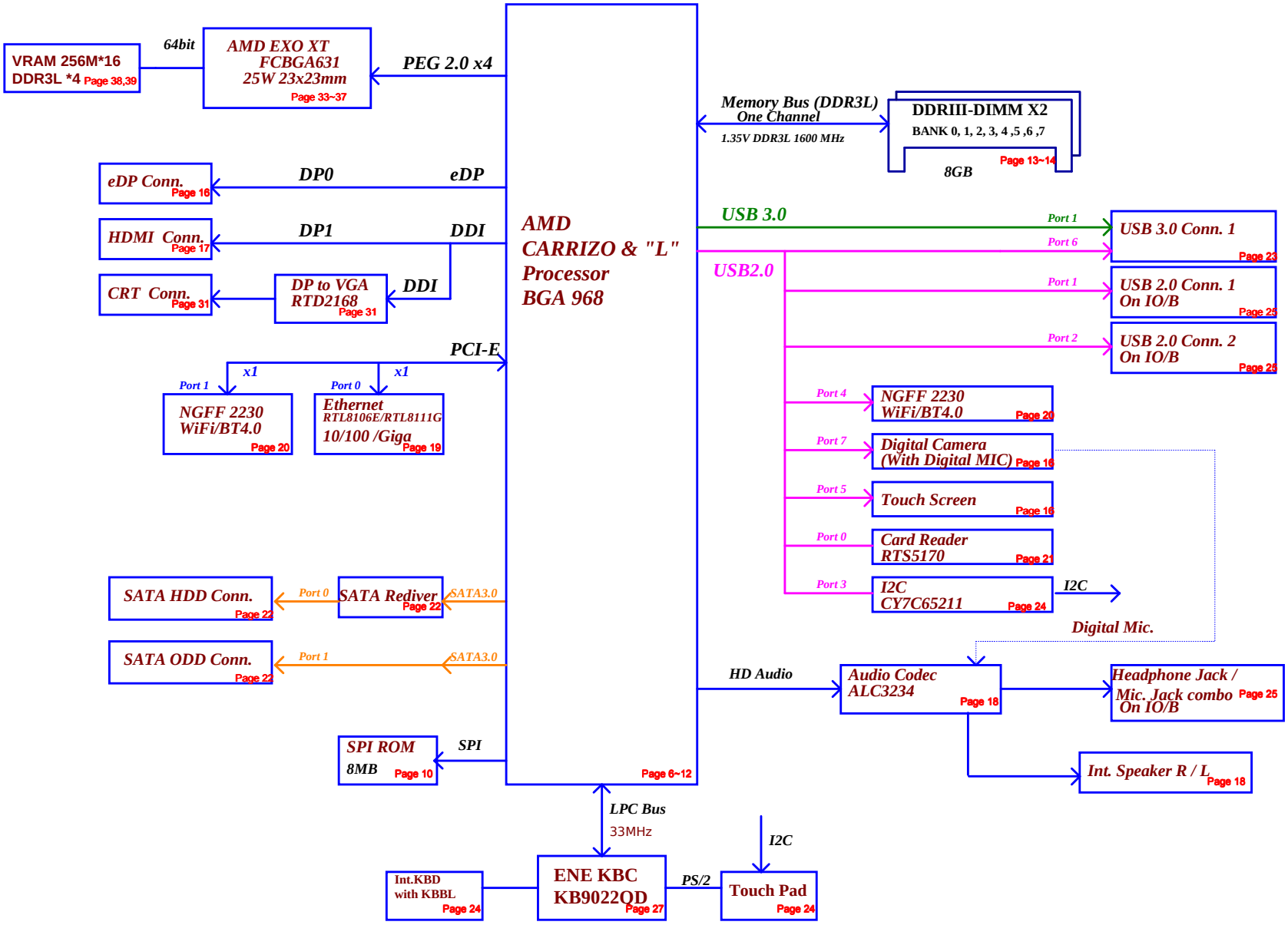
Title: *Cover Page*

Size | Document Number: *Tulip AAL12 LA-C142P* | Rev: 0.3

Date: Friday, February 13, 2015 | Sheet 1 of 56



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

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Title: Block diagram

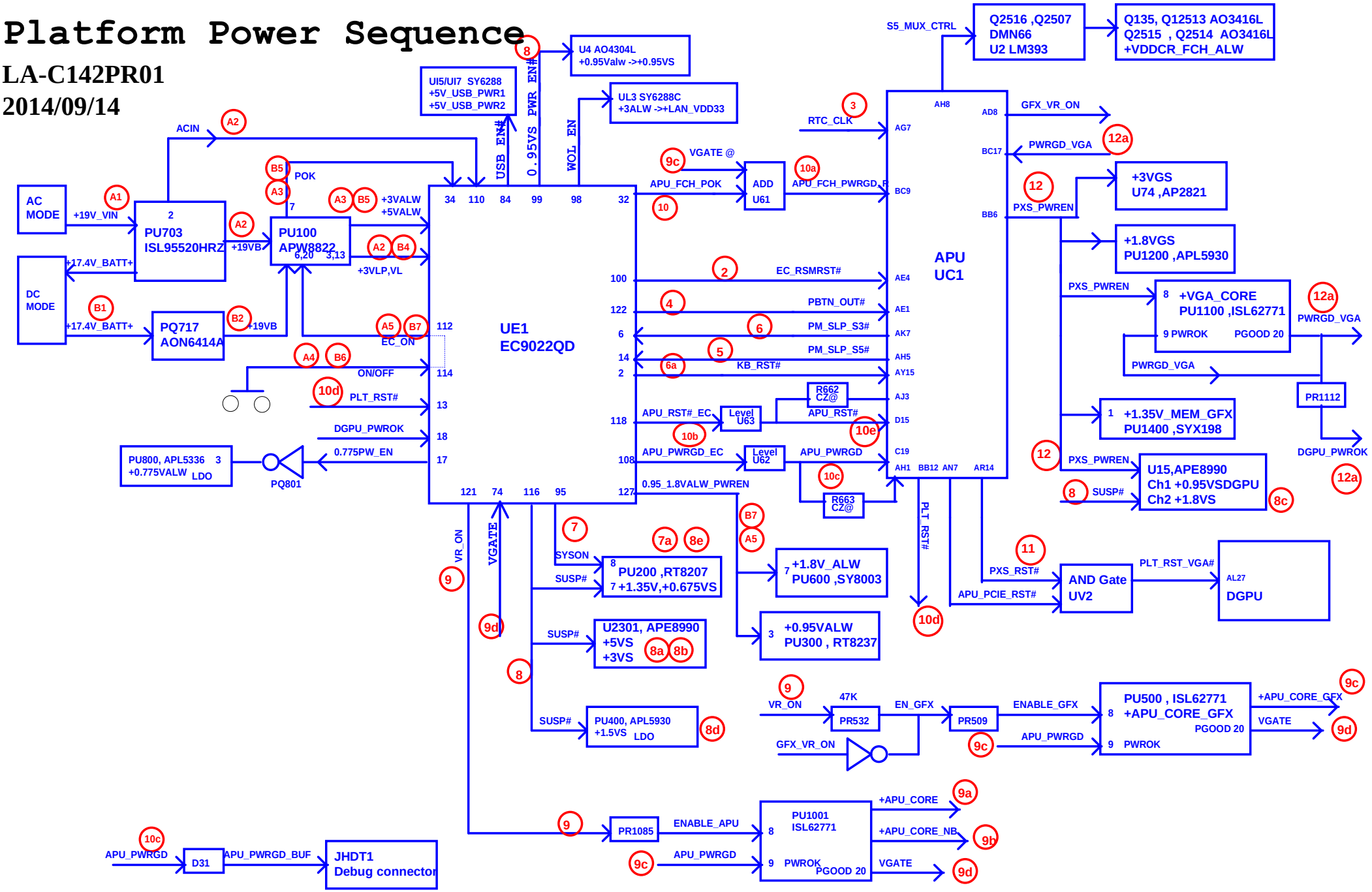
Size	Document Number	Rev
	Tulip AAL12 LA-C142P	0.3

Date: Friday, February 13, 2015 Sheet 2 of 56

Platform Power Sequence

LA-C142PR01

2014/09/14



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Issued Date	2014/06/10	Deciphered Date	2015/06/30

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Title: **Power Sequence diagram**

Size | Document Number: **Tulip AAL12 LA-C142P** | Rev: 0.3

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Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

BOARD ID Table

Board ID	
0	Tulip EVT UMA
1	Tulip EVT DIS
2	Tulip CZL DVT1
3	Tulip CZ DVT1
4	Tulip CZL DVT2
5	Tulip CZ DVT2
6	Tulip CZL pilot
7	Tulip CZ pilot
8	
9	
10	VG EVT
11	VG DVT1
12	VG DVT2
13	VG pre-MP
14	VG MP
15	
16	
17	
18	
19	

SMBUS Control Table

	SOURCE	BATT	Charger	VGA	DIMM	USB -> I2C	Thermal Sensor	eDP Touch Sensor	Touch PAD
EC_SMB_CK1 EC_SMB_DA1	KB9022Q	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9022Q			V			V		
EC_I2C_TPCLK EC_I2C_TPDAT	KB9022Q								
APU_SCLK0 APU_SDATA0	APU				V				
APU_SCLK1 APU_SDATA1	APU					V		V	V
APU_SIC APU_SID	APU			V			V		

Link

Symbol Note :

: means Digital Ground

: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	10/100 LAN
CLKOUT_PCIE1	NGFF Card (WLAN)
CLKOUT_PCIE2	
CLKOUT_PCIE3	
GFX CLK	dGPU

ULT		
	USB3.0	
	Port1	USB3 connector 1
	Port2	NA
	Port3	
	Port4	
	USB2.0	
	Port0	Card Reader
	Port1	USB connector 2 (D/B)
	Port2	USB connector 3 (D/B)
	Port3	IIC Converter CY7C65211
	Port4	NGFF Card (WLAN)
	Port5	Touch Screen Panel
	Port6	USB3 connector 1
	Port7	Camera
	PCI EXPRESS	
	Lane 1	10/100 LAN
	Lane 2	NGFF Card (WLAN)
	Lane 3	
	Lane 4	
	Lane 5	PEG (AMD)EXO UL
	Lane 6	PEG (AMD)EXO UL
	Lane 7	PEG (AMD)EXO UL
	Lane 8	PEG (AMD)EXO UL
	SATA	
	SATA0	HDD
	SATA1	ODD

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Title: Notes List

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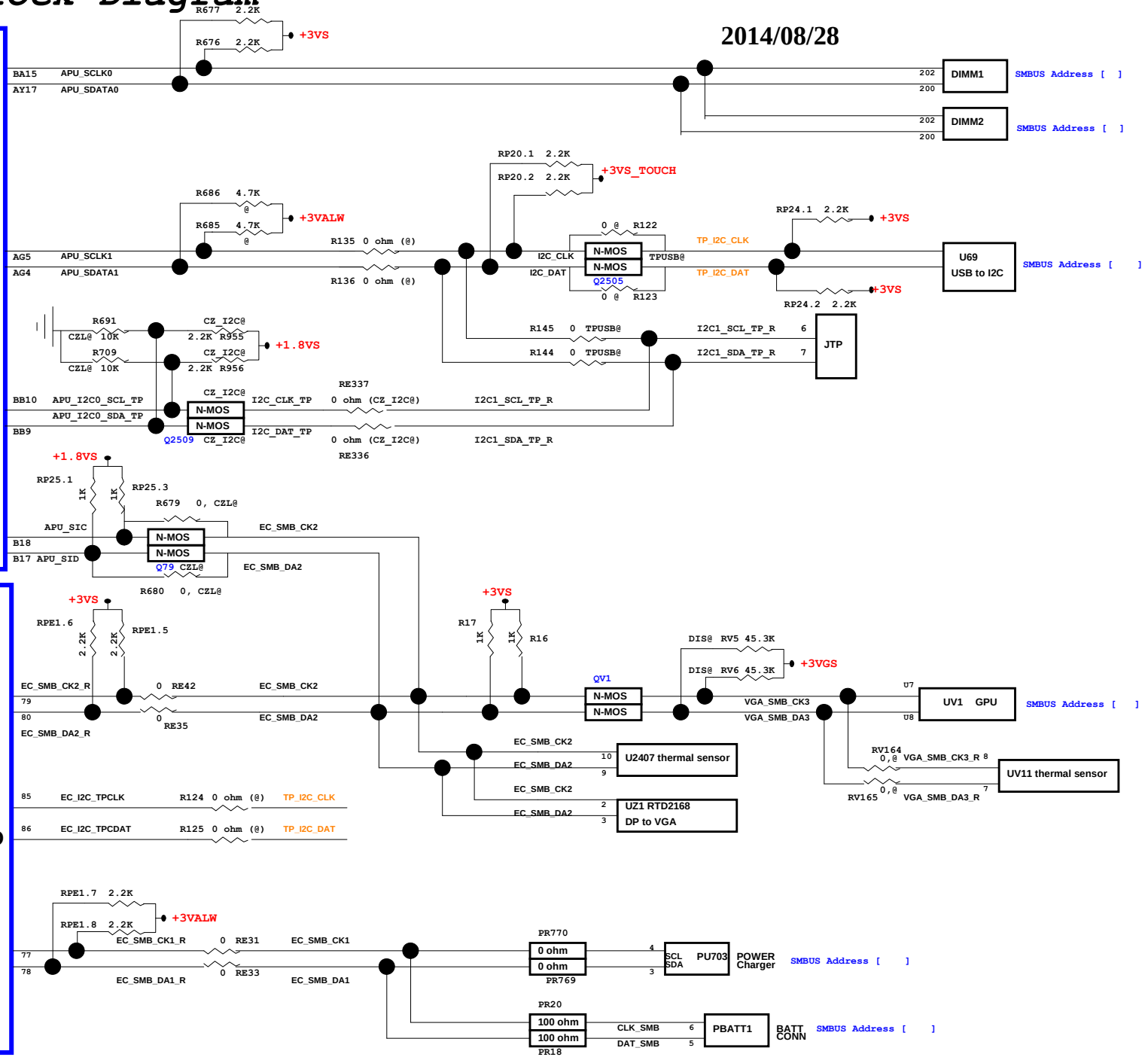
SMBus Block Diagram

2014/08/28

Carrizo

KBC
KB9022QD



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Title: SMBus block diagram

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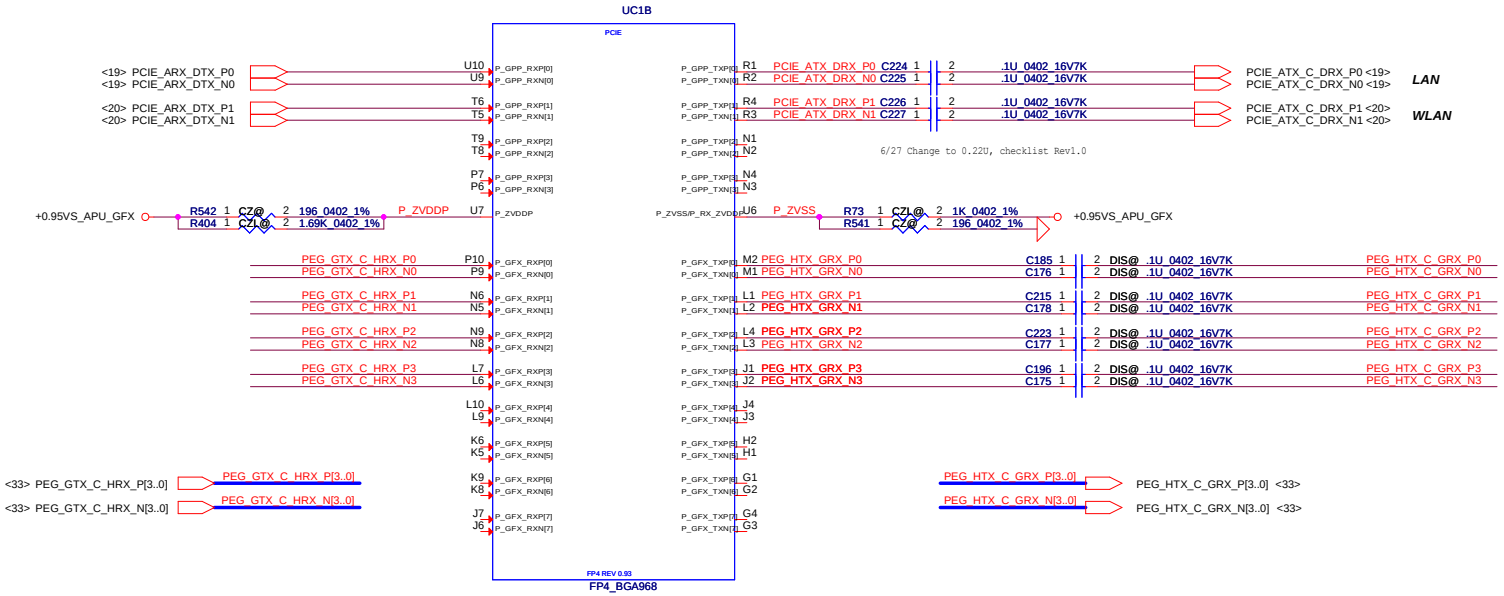
Main Func = CPU



UC1 CZL_2P2G@

S IC A8 SERIES AM7410JBY44JBA 2.2G BGA

SA00008PS1L

UC1 CZ_2P1G@

S IC FX-8800P FM880PAAY43KA 2.1G BGA 968P APU

SA00008T30L

UC1 CZL_2G@

S IC CARRIZO-L AM7310JBY44JBA 2G BGA

SA00008KX0L

UC1 CZ_1P8G@

S IC A10-8700P AM870PAAY43KA 1.8G BGA 968P APU

SA00008T40L

UC1 CZL_1P8G_A4@

CARRIZO-L AM7210JBY44JB 1.8G BGA 968P

SA00008J51L

UC1 CZL_1P8G_E2@

S IC CARRIZO-L EM7110JBY44JBA 1.8G BGA

SA00008KW0L

UC1 CZL_1P5G@

S IC CARRIZO-L EM7010JCY23JBA 1.5G BGA

SA00008KY0L

Carrizo-L:
PCIe GPP: Four x1 Gen2
PCIe Discrete Graphics Port: PCI Gen2 x4

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Title: FP3 PCIE/UMI

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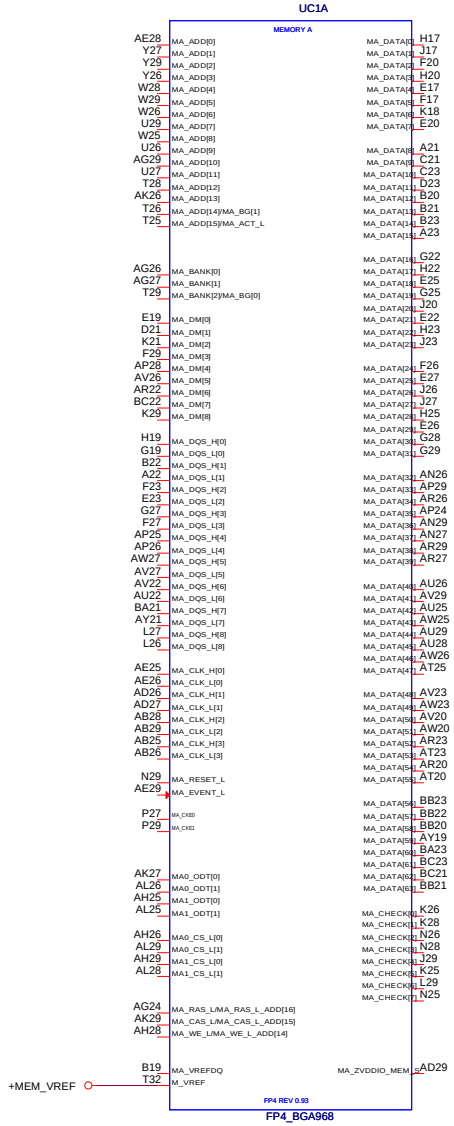
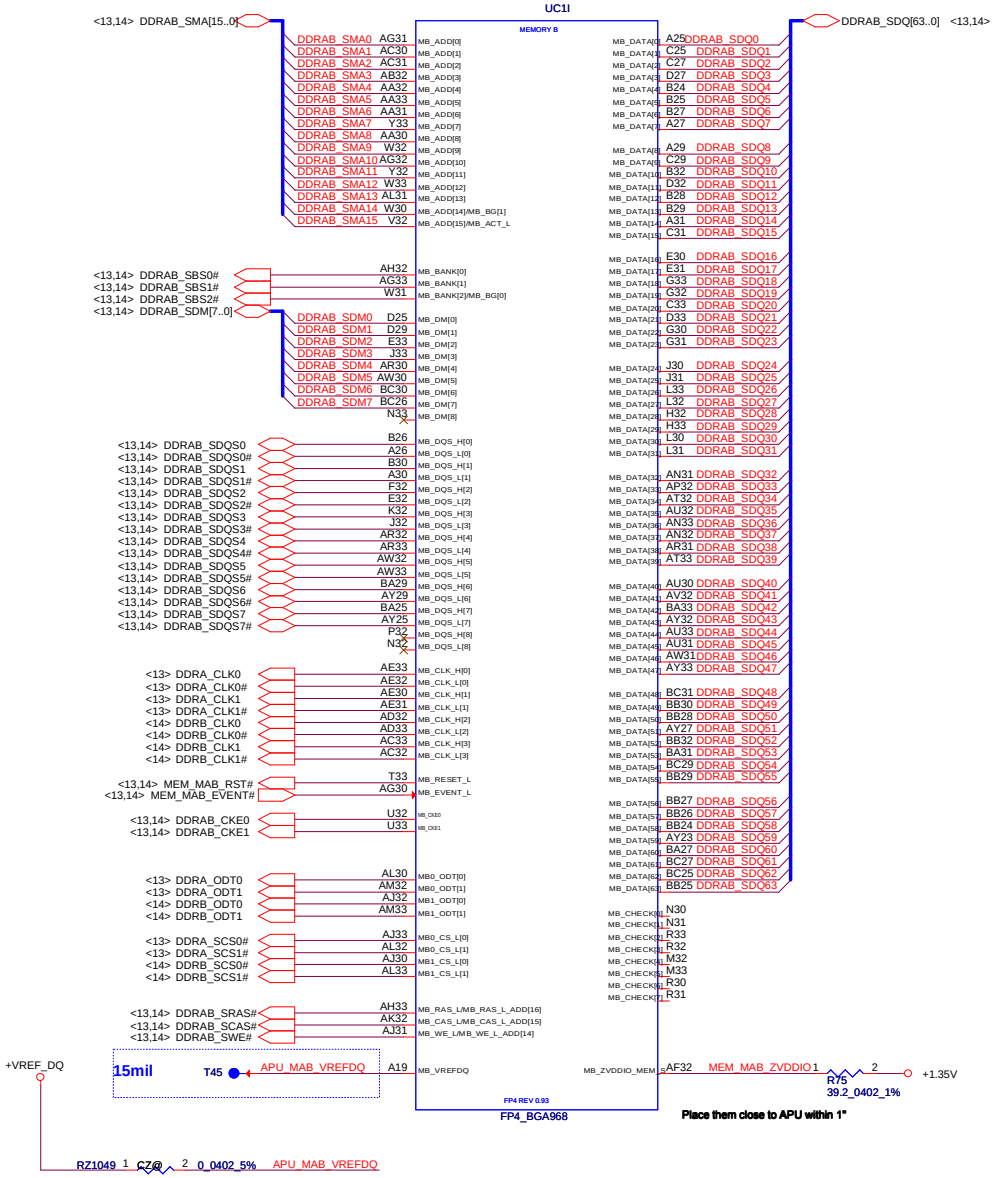
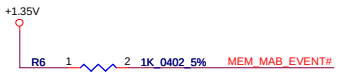
Main Func = CPU

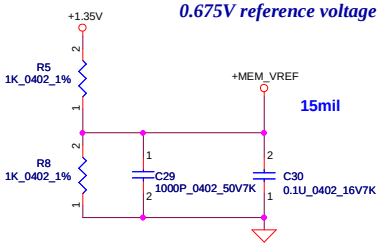




EVENT# pull high



0.675V reference voltage



Carrizo:
DDR3 - Dual Channel
- Up to 2133
- Up to 2 DIMMs/Channel
- uDIMM and SO-DIMM/DRAM down
- 1.35V and 1.5V

Carrizo-L(CHANNEL B ONLY):
DDR3 - Single Channel
- Up to 1866
- Up to 2 DIMMs/Channel
- uDIMM and SO-DIMM/DRAM down
- 1.35V and 1.5V

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Title: FP3 DDRIII MEMORY I/F

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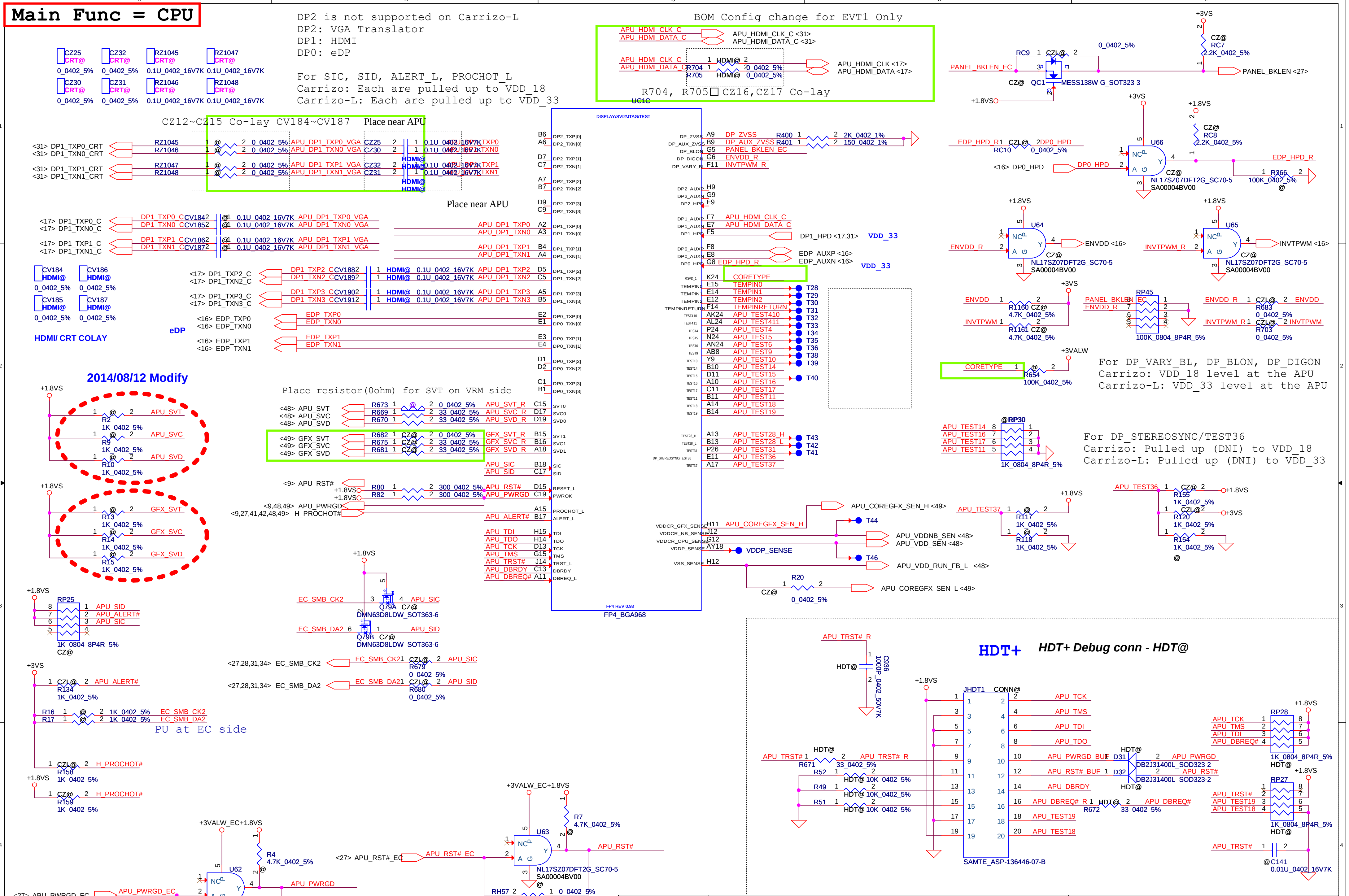

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: FP4 DISP/MISC/HDT

Size: Custom | Document Number: Tulip AAL12 LA-C142P | Rev: 0.3

Date: Friday, February 13, 2015 |

Main Func = CPU

UC1D
ACPI/SDA/ZJGPIO/RTC/I2C/UART/MISC
FP4_BGA968

I2C0 and I2C1 for CZ only
1.8V_S0 level, need LS
I2C Not Implemented:
Used as EGPIO or configured with one of the following options:
1.PH 2.2K
2.PD 10K

32.768KMHz CRYSTAL

RSMRST#
1.8V /EC program to 1.8V OUTPUT
Check RSMRST delay 10ms

SYS_PWRGD:
CZ->3.3V /EC program to 3.3V OUTPUT
CZL->1.8V /EC program to 1.8V OUTPUT

UMA: LOW
DIS: HIGH

SD no used can NC

UART no used can NC

For PCIE device reset on FS1
(GFX,GLAN,WLAN,LVDS Travis)
APU_PCIE_RST #: Reset PCIE device on APU

QCL10 LAN-APU,WLAN&ExCARD-FCH 20110803

	LPC_CLK0_EC	LPC_CLK1	LPC_FRAME#	GEVENT2_L ???? <INT PU>		RTC_CLK <INT PU>	BLINK/GPIO11 <INT PU>	SYS_RST# <INT PU>
				CZL	CZ		LD2_RST#/PG	
H	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	SPI ROM (DEFAULT)	1.8V SPI ROM (Default)	ENHANCED RESET (AOAC)	COIN BATT ON BOARD (DEFAULT)	OUTPUT TO APU (DEFAULT)	NORMAL RESET MODE (DEFAULT)
L	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM	TRADITION RESET (DEFAULT)	COIN BATT NOT ON BOARD	OUTPUT TO PADS	SHORT RST MODE

Security Classification	Compal Secret Data
Issued Date	2014/06/10
Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: FP4 GPIO/AZ/MISC/STRAPS

Size: Custom | Document Number: Tulip AAL12 LA-C142P | Rev: 0.3

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Main Func = CPU

UC1E
CLK/SATA/USB/SPI/LPC
FP4 REV 0.93
FP4_BGA968

HDD
ODD
VGA
LAN
WLAN

<22> SATA_ATX_DRX_P0
<22> SATA_ATX_DRX_N0
<22> SATA_ARX_DTX_N0
<22> SATA_ARX_DTX_P0
<22> SATA_ATX_DRX_P1
<22> SATA_ARX_DRX_N1
<22> SATA_ARX_DTX_N1
<22> SATA_ARX_DTX_P1
R90 2 1 1K_0402_1% SATA_ZVSS
R96 2 1 1K_0402_1% SATA_ZVDD
+0.95VS
<22> DEVSLP0_HDD
<20> WL_OFF#
<27,29> SATA_ACT#
DEVSLP0_HDD
WL_OFF#
SATA_ACT#
+3VS
10K_0402_5% RH40
10K_0402_5% RH42
10K_0402_5% RH43
<33> CLK_PEG_VGA
<33> CLK_PEG_VGA#
<19> CLK_PCIE_LAN
<19> CLK_PCIE_LAN#
<20> CLK_PCIE_WLAN
<20> CLK_PCIE_WLAN#
48M_X1
48M_X2
<9,27> LPC_CLK0_EC
<9> LPC_CLK1
R449 33_0402_5%
R450 0_0402_5%
<27> LPC_AD0
<27> LPC_AD1
<27> LPC_AD2
<27> LPC_AD3
<9,27> LPC_FRAME#
<27> SERIRQ
R106 0_0402_5%
<27> EC_SPI_CLK
<27> EC_SPI_CS1#
<27> EC_SPI_MISO
<27> EC_SPI_MOSI
R1691 0_0402_5% APU_SPI_CLK
R1693 0_0402_5% APU_SPI_CS1#
R1692 0_0402_5% APU_SPI_MISO
R1694 0_0402_5% APU_SPI_MOSI
APU_SPI_CLK_R
APU_SPI_CS1#_R
APU_SPI_WP#
APU_SPI_HOLD#
APU_SPI_TPMCS#
CRT_EMI@
APU_SPI_CLK C27 10P_0402_50V8J
7/25 Add, EMI request
APU_SPI_CS1# R107 0_0402_5% APU_SPI_CS1#_R

USBCLK/25M_48M_OSC
USB_ZVSS R641 11.8K_0402_1%
USB20_CR_P0 <21>
USB20_CR_N0 <21>
USB20_JUSB2_P1 <25>
USB20_JUSB2_N1 <25>
USB20_JUSB3_P2 <25>
USB20_JUSB3_N2 <25>
USB20_P3 <24>
USB20_N3 <24>
USB20_MINI1_P4 <20>
USB20_MINI1_N4 <20>
USB20_TOUCH_P5 <16>
USB20_TOUCH_N5 <16>
USB20_JUSB1_P6 <23>
USB20_JUSB1_N6 <23>
USB20_CAM_P7 <16>
USB20_CAM_N7 <16>
Card Reader
USB Conn JUSB2 (DB)
USB Conn JUSB3 (DB)
For I2C
Mini Card (WLAN)
Touch screen panel
USB Conn JUSB1
Camera
USB 3.0

USBSS_ZVSS R644 1K_0402_1%
USBSS_ZVDD R645 1K_0402_1%
+0.95VALW
USB3TP1_JUSB1 <23>
USB3TN1_JUSB1 <23>
USB3RP1_JUSB1 <23>
USB3RN1_JUSB1 <23>
USB Conn JUSB1

48MHz CRYSTAL

48M_X2
48M_X1
R939 1M_0402_5%
Y2
48MHZ_8PF_X3S048000D81H-W
Part Number = SJ10000AF00
C796 5.6P_0402_50V8D
C797 5.6P_0402_50V8D

8MB SPI ROM

+SPI_VCC
R634 CZL@ APU_SPI_HOLD# 10K_0402_5%
R635 CZL@ APU_SPI_WP# 10K_0402_5%
R636 CZL@ APU_SPI_CS1# 10K_0402_5%
R637 @ APU_SPI_CS1# 10K_0402_5%
R638 @ APU_SPI_TPMCS# 10K_0402_5%
+1.8VS
+1.8V_ALW
+3VALW
R1673 CZL@ 0_0603_5%
R1672 @ 0_0603_5%
R1675 CZ@ 0_0603_5%
C635 @ 1U_0402_16V7K
U56 CZ@
CS# VCC
DO(IO1) HOLD#(IO3)
WP#(IO2) CLK
GND DI(IO0)
W25Q64FWSSIQ_SO8
APU_SPI_CS1#
APU_SPI_MISO
APU_SPI_WP#
+SPI_VCC
APU_SPI_HOLD#
APU_SPI_CLK
APU_SPI_MOSI
APU_SPI_CLK R617 NEMI@ 10_0402_5% C636 NEMI@ 10P_0402_50V8J
R642 CZ@ APU_SPI_HOLD# 10K_0402_5%
R640 CZ@ APU_SPI_WP# 10K_0402_5%
R639 CZ@ APU_SPI_CS1# 10K_0402_5%

U56 CZL@
SPI ROM
Part Number = SA00008IP00
EN25QH64A-104HIP_SO8

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: FT3 SATA/CLK/USB/SPI

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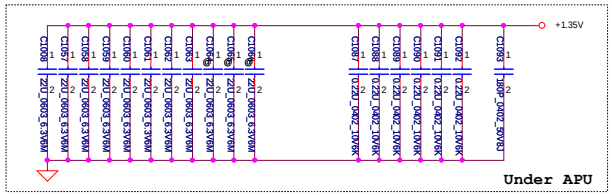
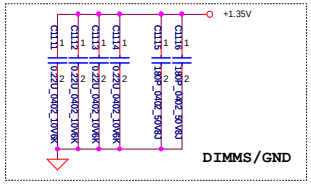
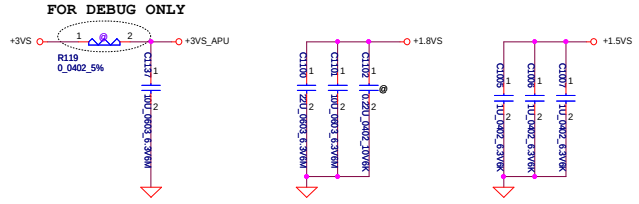
Main Func = CPU

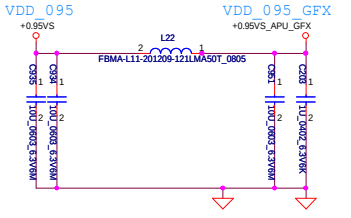


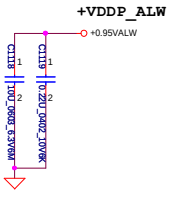


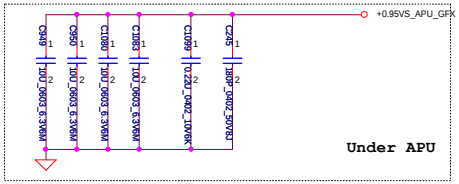
FOR DEBUG ONLY

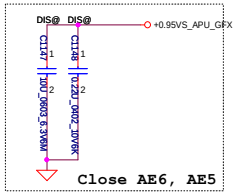


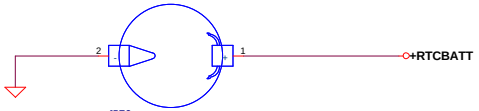
+0.95VALW/+0.95VS OF APU +VDDP_VS

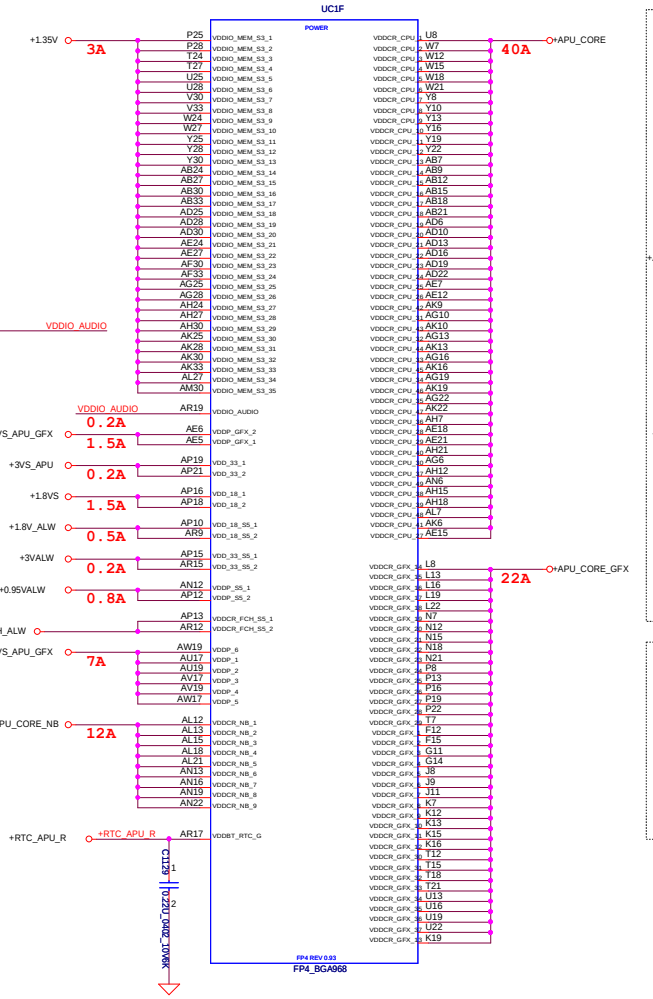


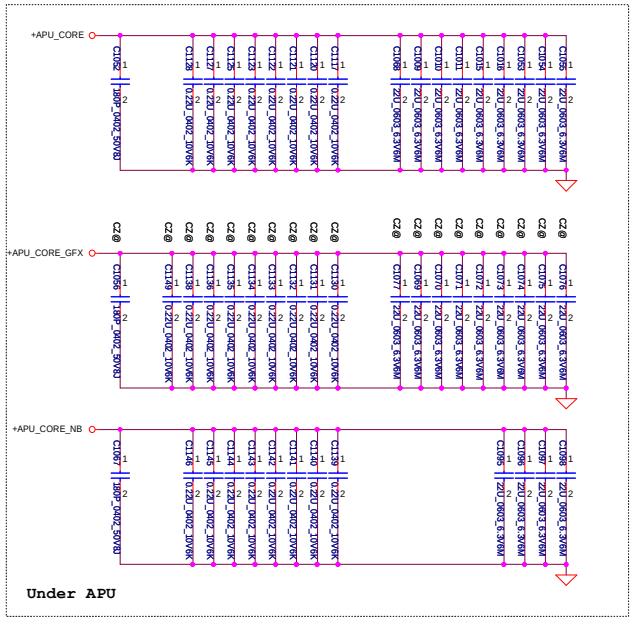


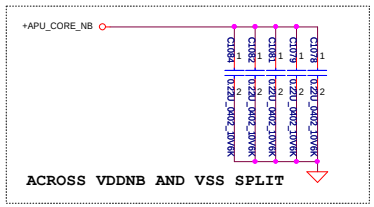


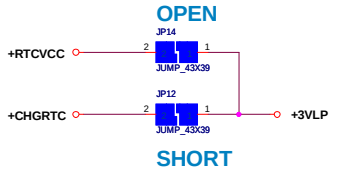




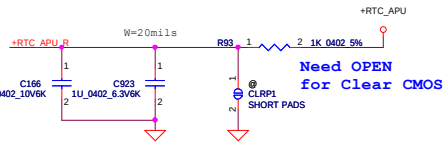


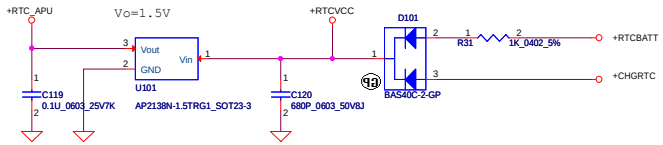






RTC OF APU





Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

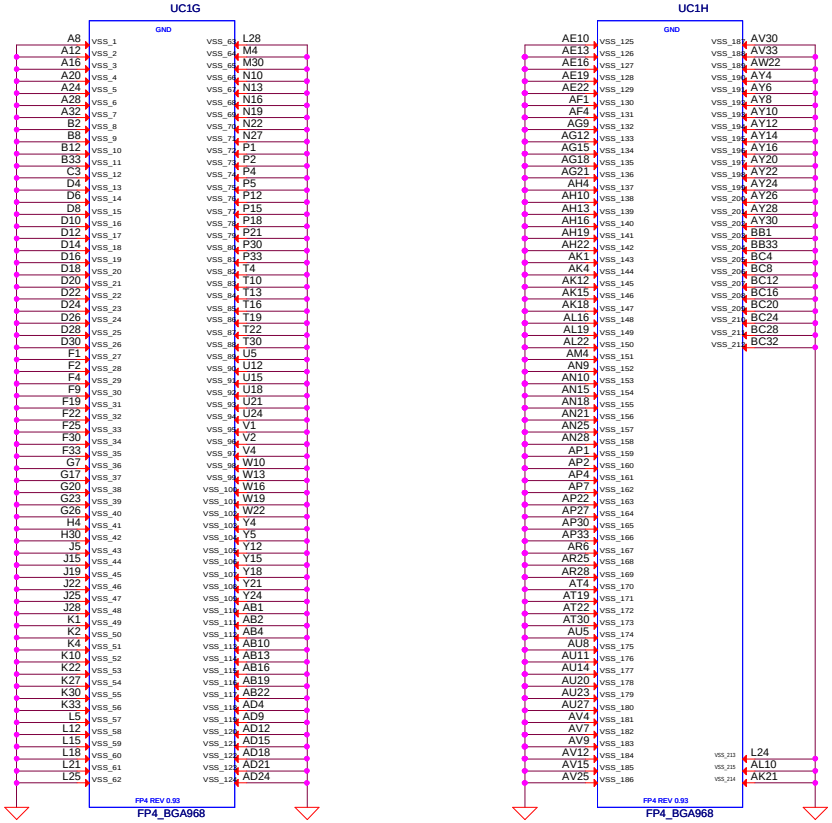
Compal Electronics, Inc.

Title: FP4 PWR

Size	Document Number	Rev
C	Tulip AAL12 LA-C142P	0.3

Date: Friday, February 13, 2015 | Sheet 11 of 56

Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

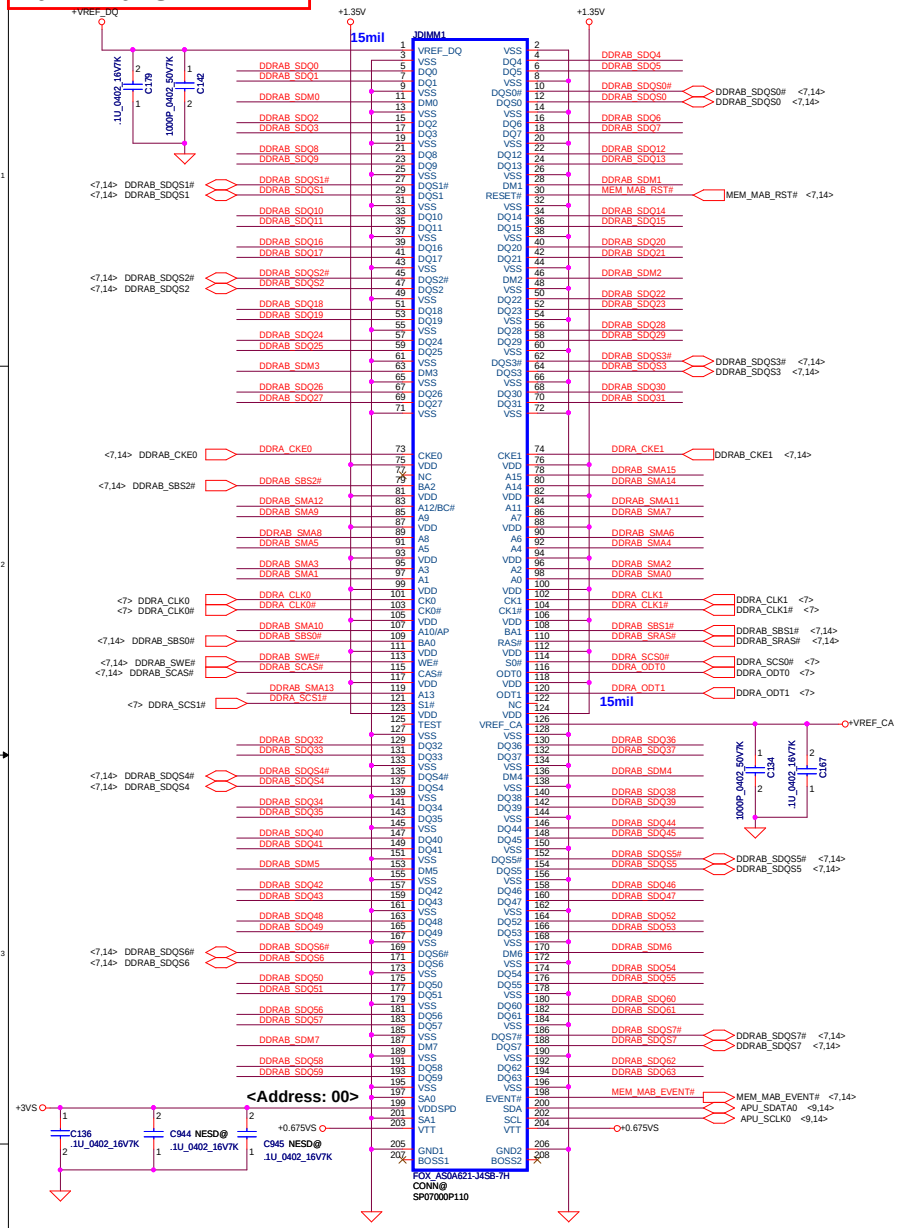
Compal Electronics, Inc.

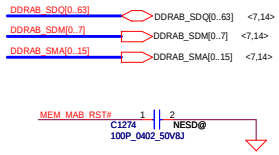
Title: FP3 GND

Size: Custom | Document Number: Tulip AAL12 LA-C142P | Rev: 0.3

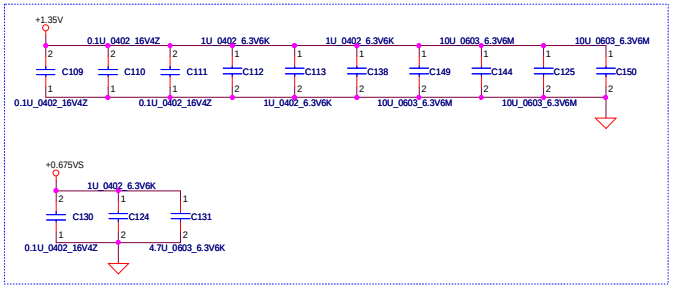
Date: Friday, February 13, 2015 | Sheet 12 of 56

Main Func = DIMM1

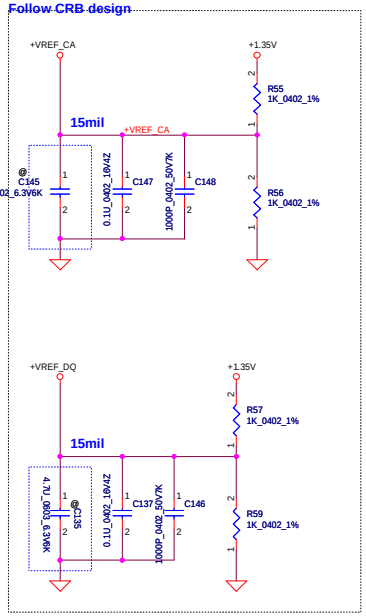


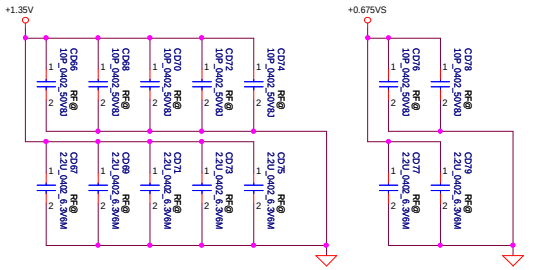


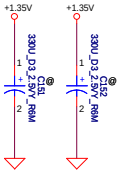
Place near DIMM1



Follow CRB design







Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

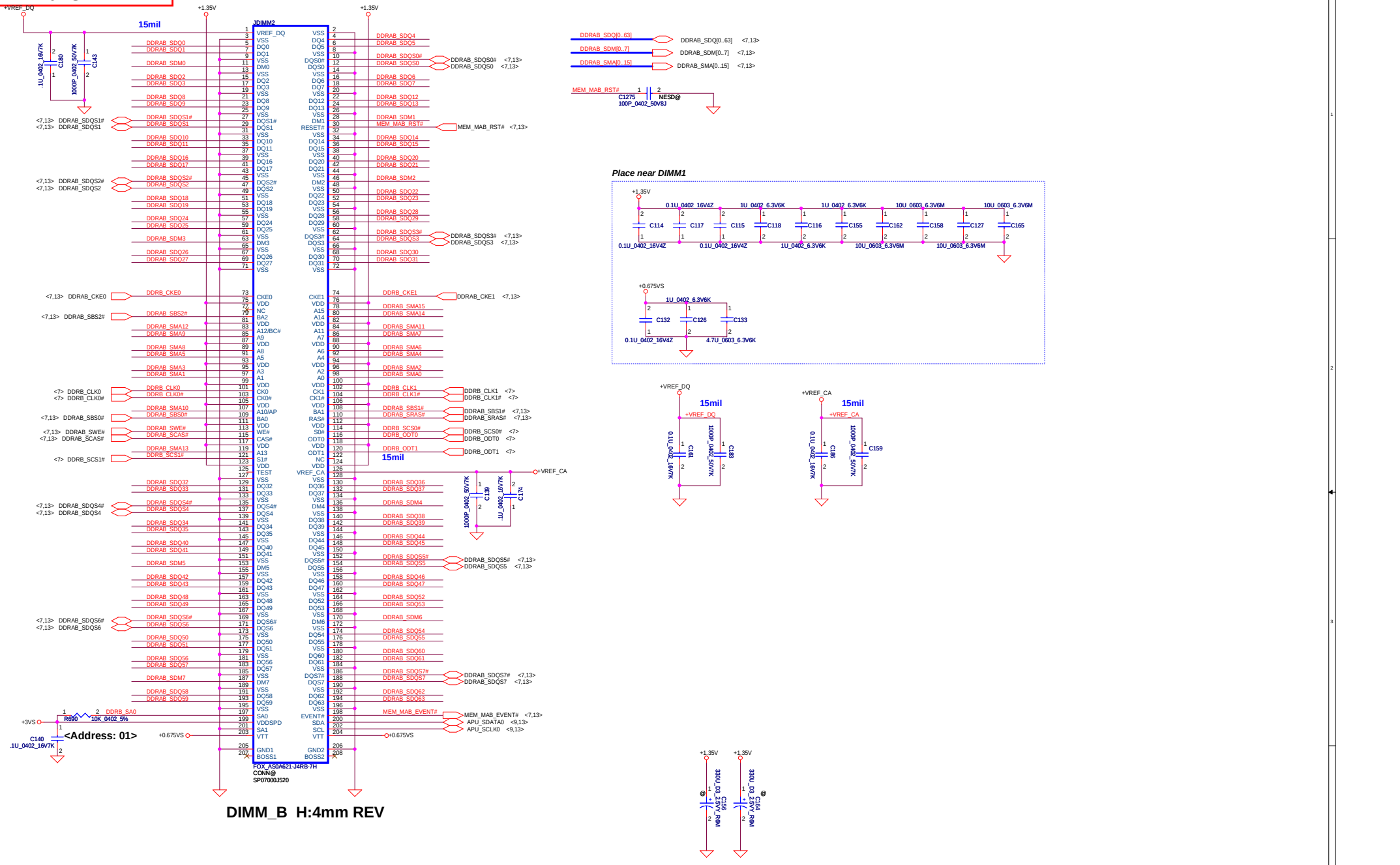
Compal Electronics, Inc.

Title: DDR3 SODIMM-I Socket

Size	Document Number	Rev
C	Tulip_AAL12 LA-C142P	0.3

Date: Friday, February 13, 2015 Sheet 13 of 56

Main Func = DIMM2



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: DDR3 SODIMM-II Socket

Size	Document Number	Rev
C	Tulip AAL12 LA-C142P	0.3

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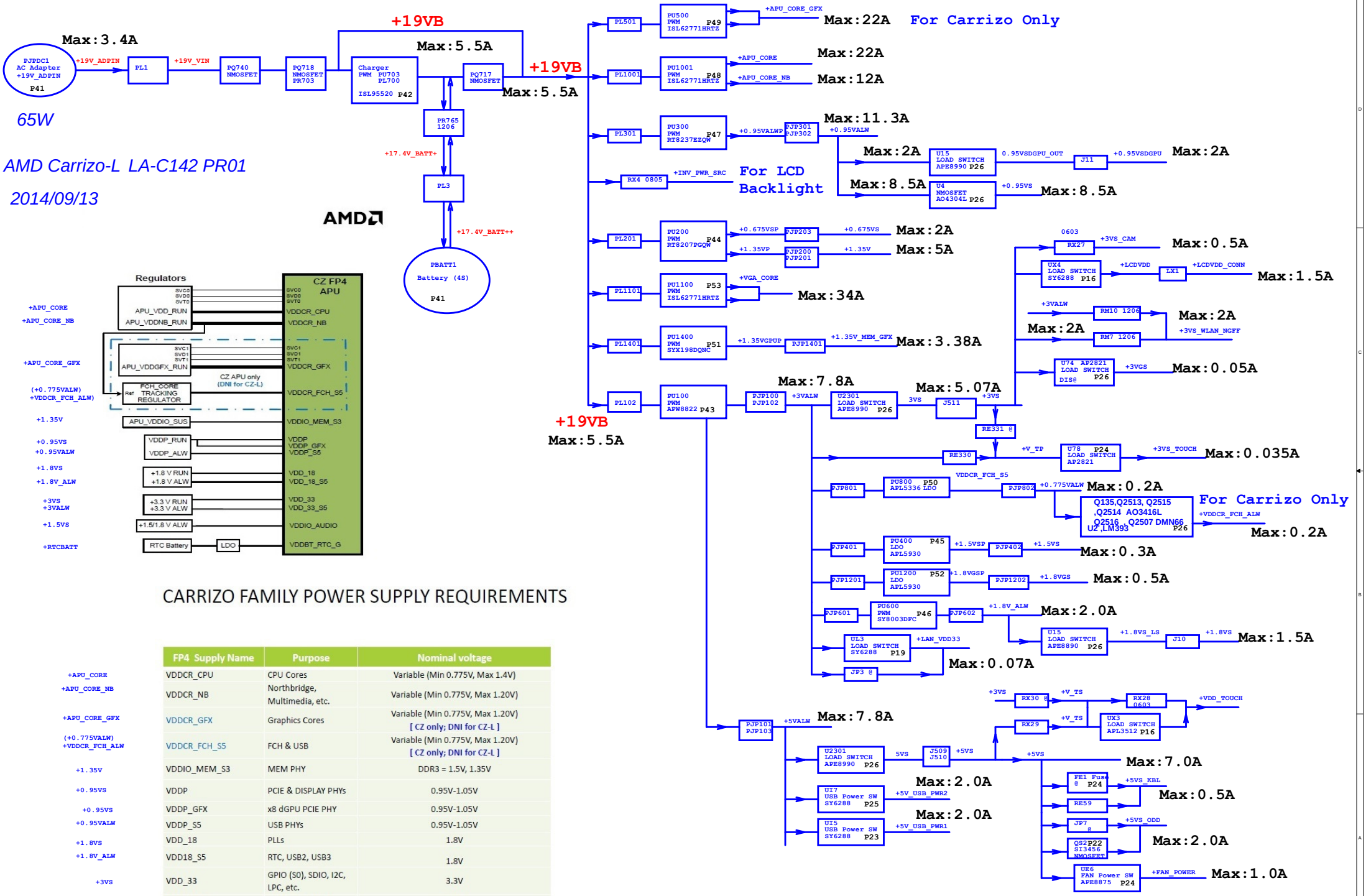

CARRIZO FAMILY POWER SUPPLY REQUIREMENTS

	FP4 Supply Name	Purpose	Nominal voltage
+APU_CORE	VDDCR_CPU	CPU Cores	Variable (Min 0.775V, Max 1.4V)
+APU_CORE_NB	VDDCR_NB	Northbridge, Multimedia, etc.	Variable (Min 0.775V, Max 1.20V)
+APU_CORE_GFX	VDDCR_GFX	Graphics Cores	Variable (Min 0.775V, Max 1.20V) [CZ only; DNI for CZ-L]
(+0.775VALW) +VDDCR_FCH_ALW	VDDCR_FCH_S5	FCH & USB	Variable (Min 0.775V, Max 1.20V) [CZ only; DNI for CZ-L]
+1.35V	VDDIO_MEM_S3	MEM PHY	DDR3 = 1.5V, 1.35V
+0.95VS	VDDP	PCIE & DISPLAY PHYs	0.95V-1.05V
+0.95VS	VDDP_GFX	x8 dGPU PCIE PHY	0.95V-1.05V
+0.95VALW	VDDP_S5	USB PHYs	0.95V-1.05V
+1.8VS	VDD_18	PLLs	1.8V
+1.8V_ALW	VDD18_S5	RTC, USB2, USB3	1.8V
+3VS	VDD_33	GPIO (S0), SDIO, I2C, LPC, etc.	3.3V
+3VALW	VDD_33_S5	GPIO (S5), USB2	3.3V
+1.5VS	VDDIO_AUDIO	AZ, I2S	1.5V (AZ)/1.8V (I2S)
+RTCBATT	VDDBT_RTC_G	RTC	1.5V

Compal Electronics, Inc.

Title: Green CLK

Size | Document Number: Tulip AAL12 LA-C142P | Rev: 0.3

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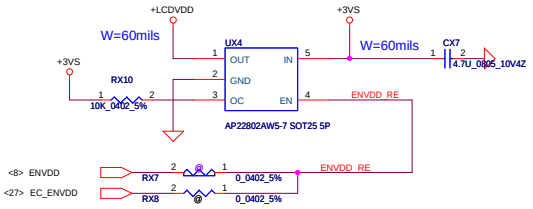
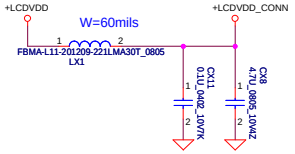
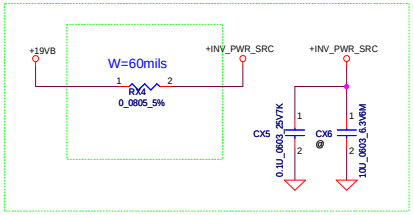
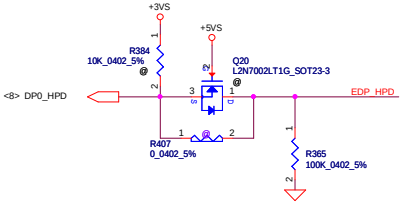
Main Func = LCD

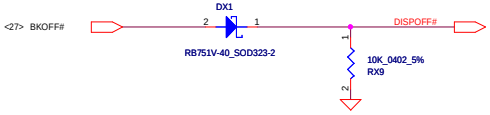
LCD PWR CTRL

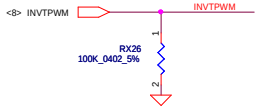


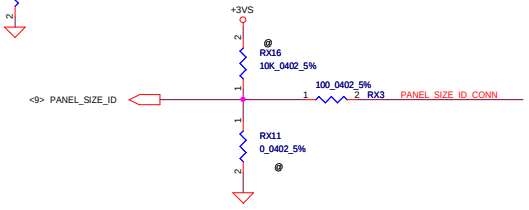


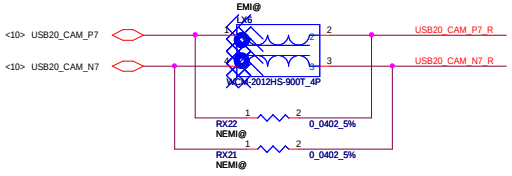


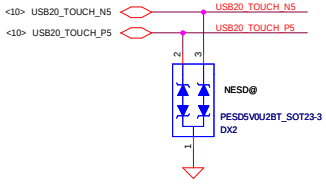




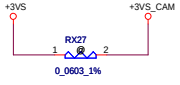




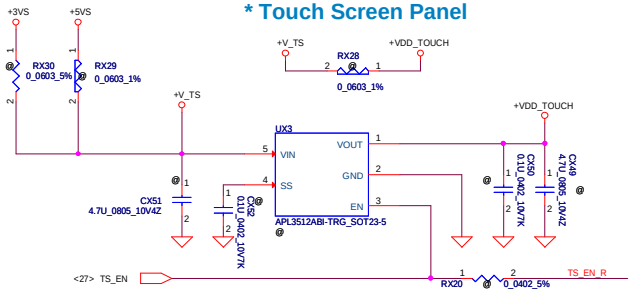




Webcam PWR CTRL

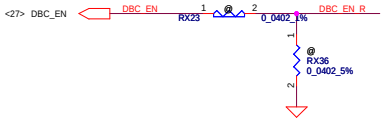


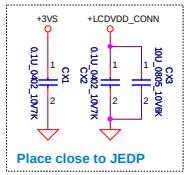
* Touch Screen Panel



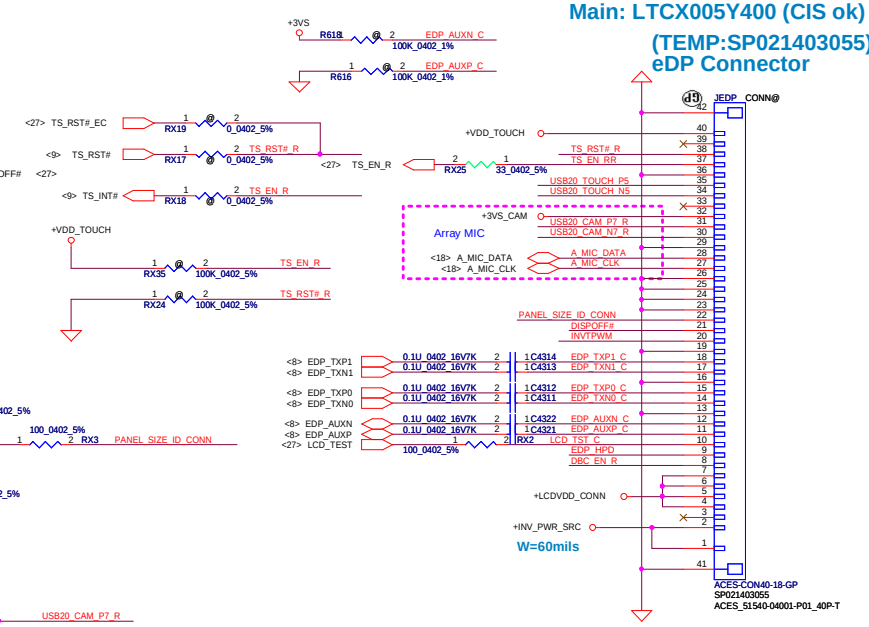
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

SS table





Main: LTCX005Y400 (CIS ok)
(TEMP:SP021403055)
eDP Connector



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

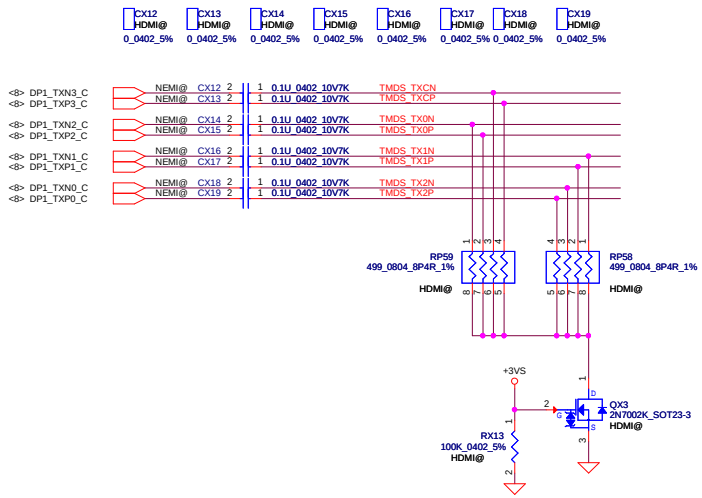
Compal Electronics, Inc.

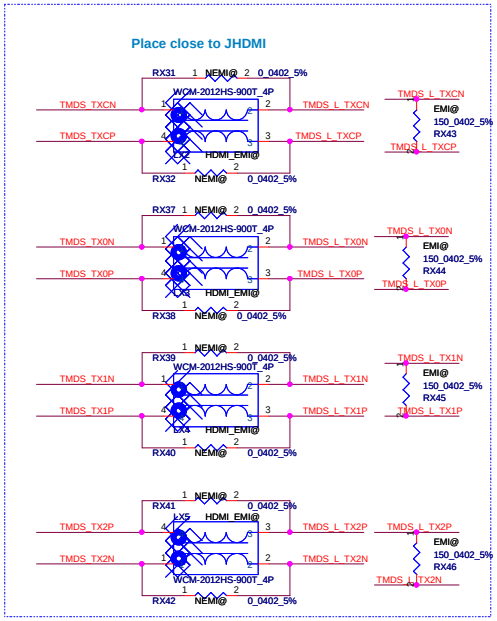
Title: eDP / webcam / TouchScreen

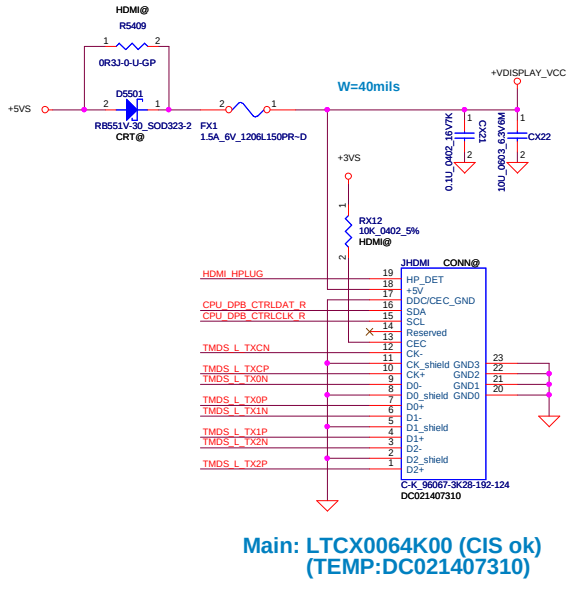
Size	Document Number	Rev
	Tulip AAL12 LA-C142P	0.3

Date: Friday, February 13, 2015 Sheet 16 of 56

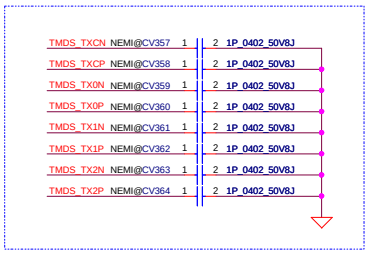
Main Func = HDMI

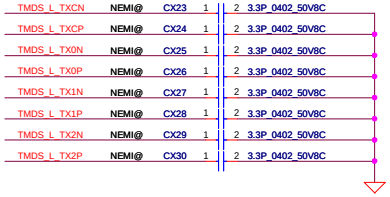






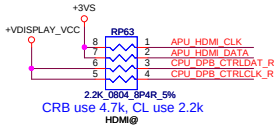
Main: LTCX0064K00 (CIS ok)
(TEMP:DC021407310)



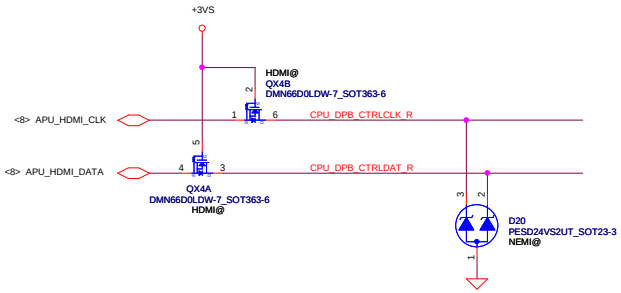


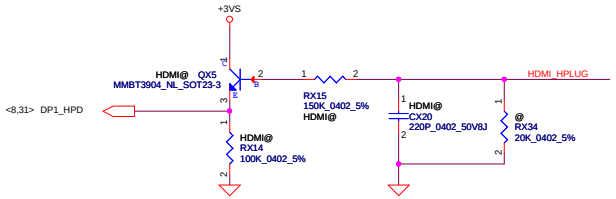
46@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM



CRB use 4.7k, CL use 2.2k





Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: **HDMI**

Size | Document Number: **Tulip AAL12 LA-C142P** | Rev: 0.3

Date: Friday, February 13, 2015 | Sheet 17 of 56

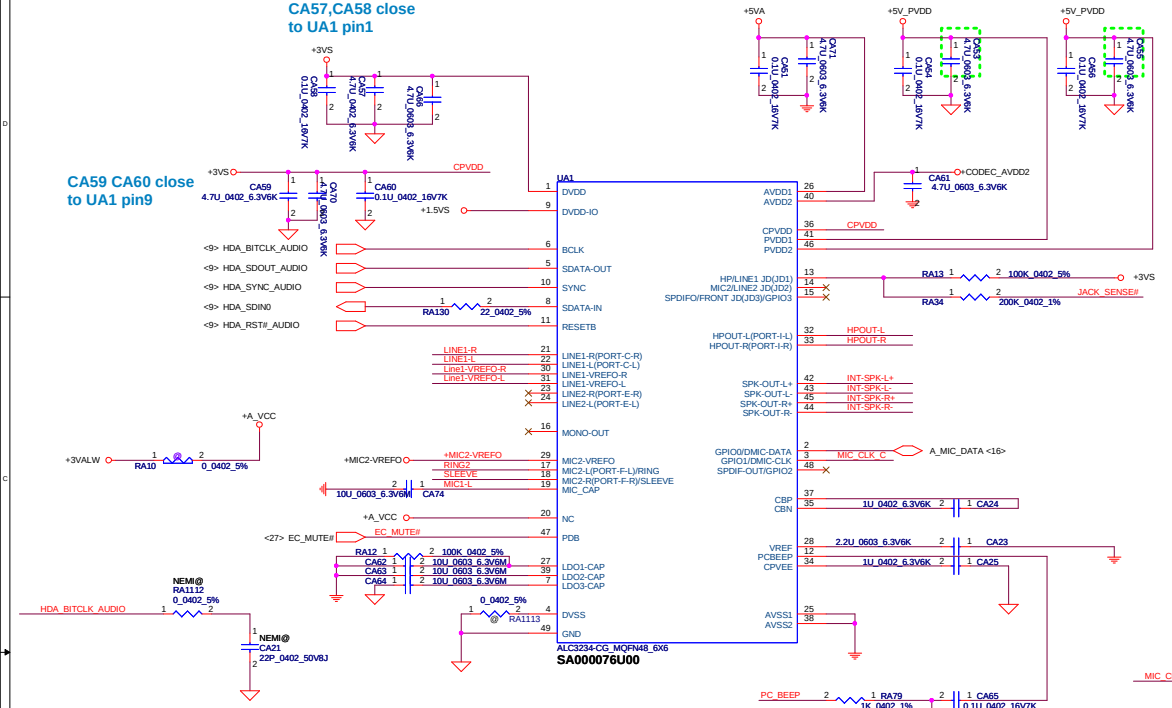
Main Func = Audio

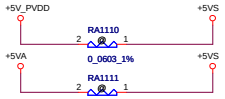
CA71, CA51 place close to Pin 26

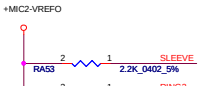
CA53, CA55 change Value from 10U_0603_6.3V6M~D to 4.7U_0603_6.3V6K

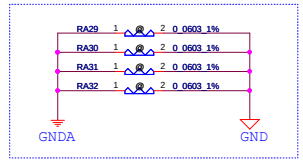
CA57,CA58 close to UA1 pin1

CA59 CA60 close to UA1 pin9

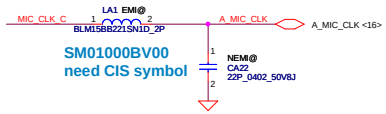




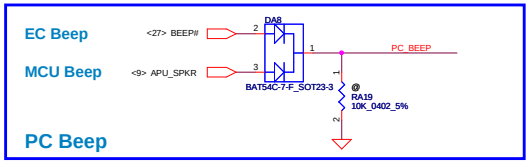


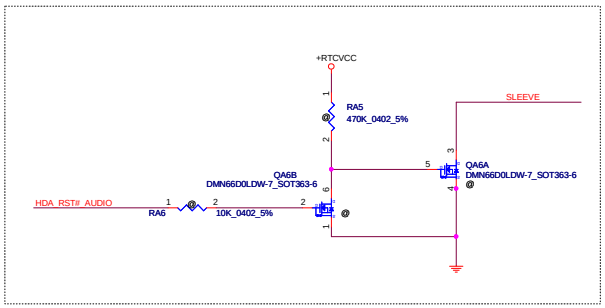


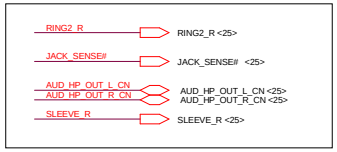
Place on the moat between GND & GNDA.



SM01000BV00
need CIS symbol

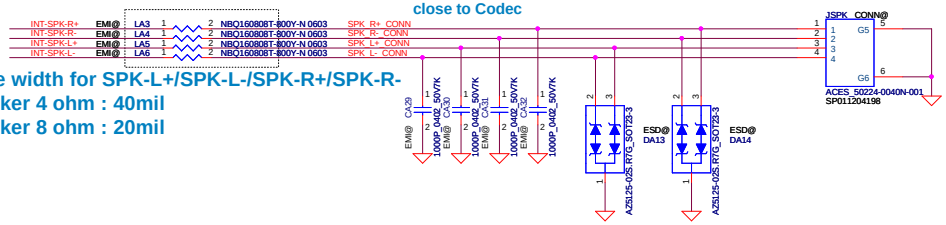




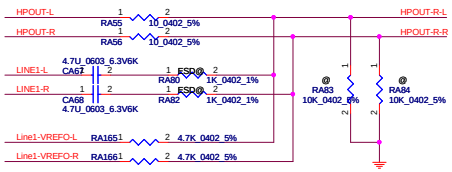


Close to UA1 Pin11,13,14,16

close to Codec



Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil



iPhone and Nokia type Combo Jack

Place CAP and ESD Diode on D/B

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

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Compal Electronics, Inc.

Title: Audio Codec ALC3234

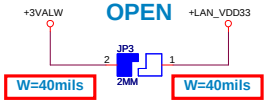
Size: A3 | Document Number: Tulip AAL12 LA-C142P | Rev: 0.3

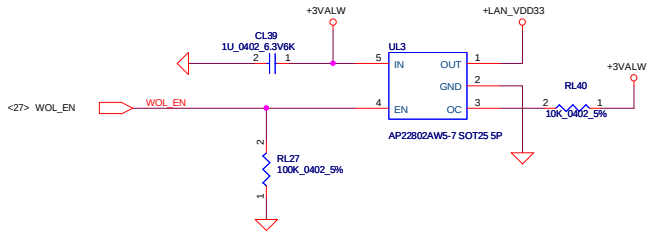
Date: Friday, February 13, 2015 | Sheet 18 of 56

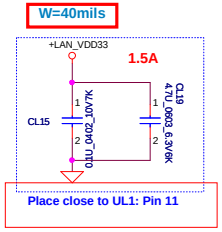
Main Func = LAN

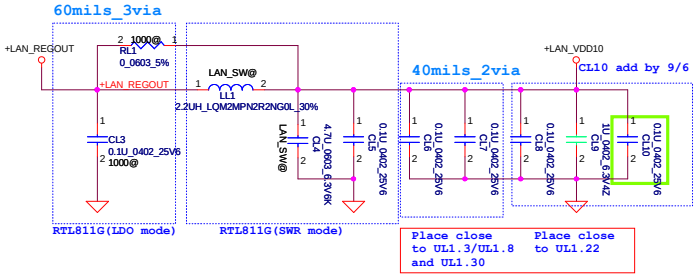
OPEN

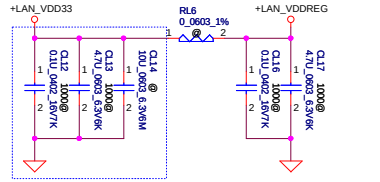
+LAN_IO rising time : >1ms and <100ms



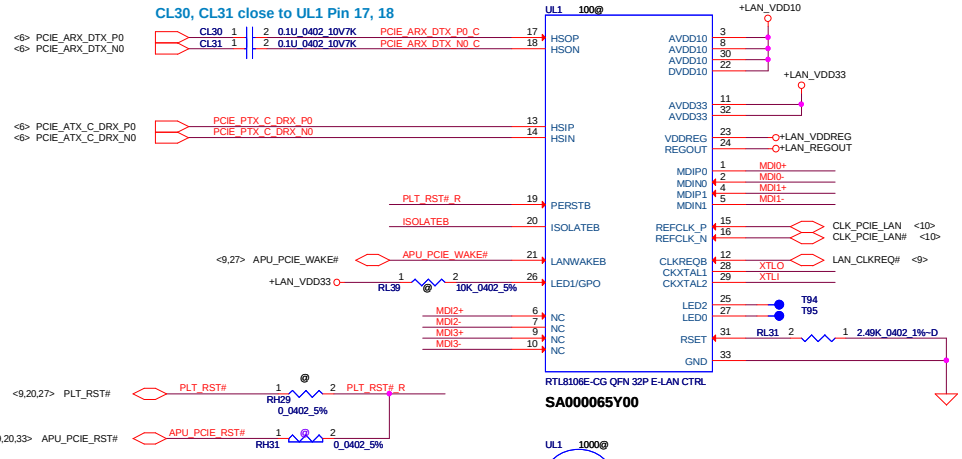








CL30, CL31 close to UL1 Pin 17, 18



TL1

S X'FORM_ NS0015 LF LAN

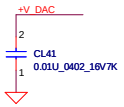
SP050005Y00

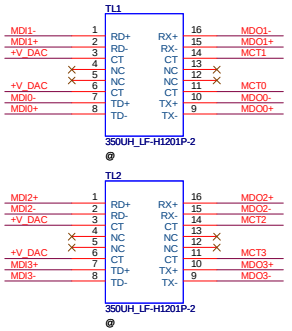
TL2

S X'FORM_ NS0015 LF LAN

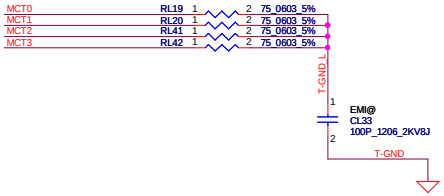
SP050005Y00

1000@

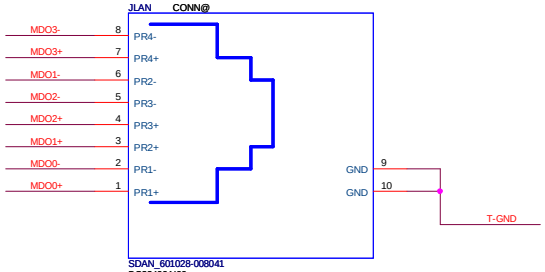


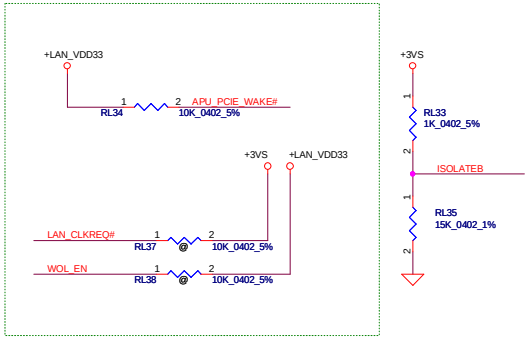


Place close to TCT pin

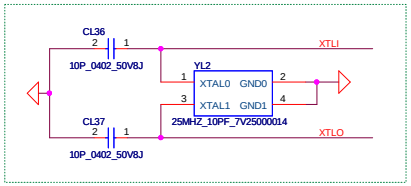


Main: DC23400AI00 (CIS ok)





Reserve 10K pull LAN_IO



XTAL

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

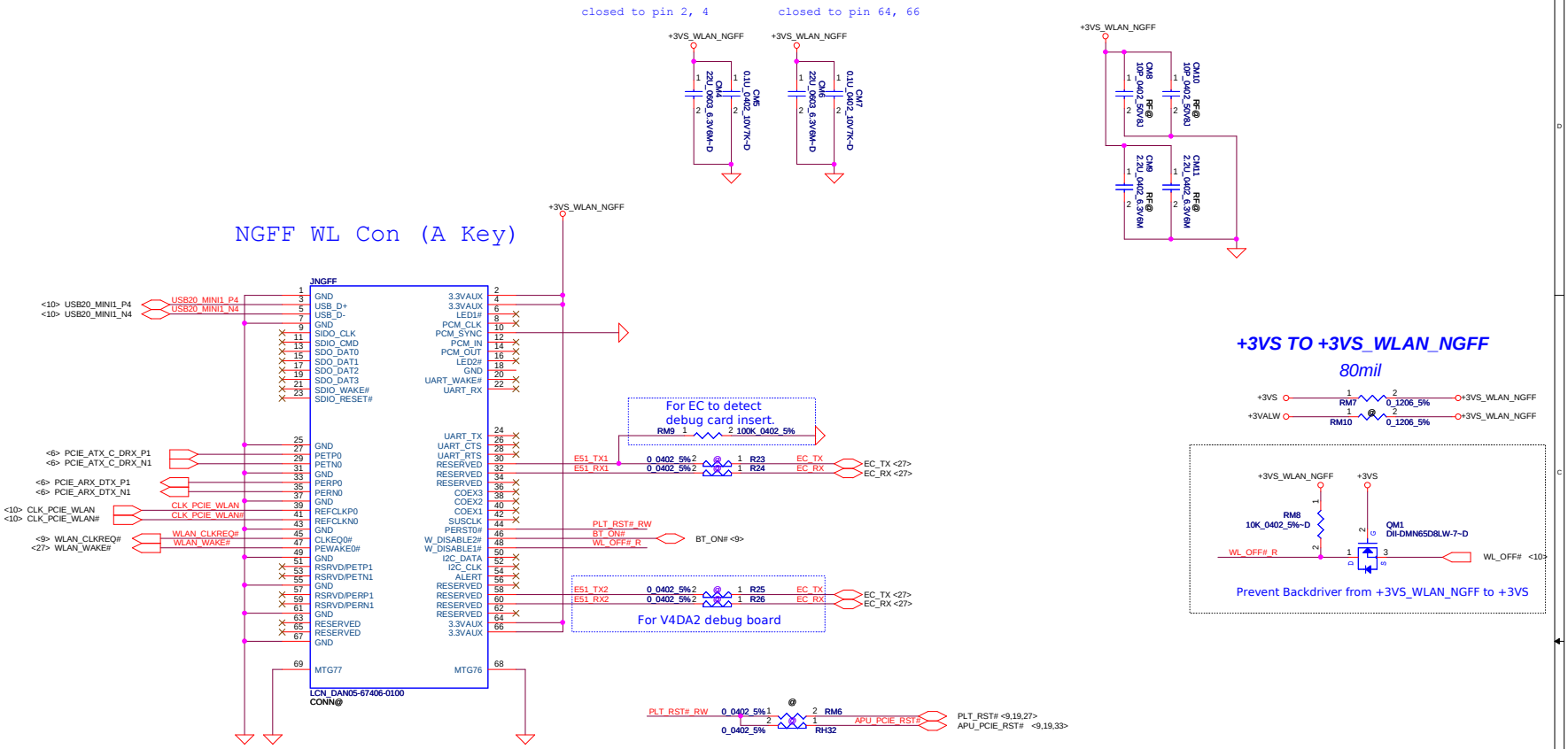
Compal Electronics, Inc.

Title: **LAN RTL8106EUS**

Size: Custom | Document Number: Tulip AAL12 LA-C142P | Rev: 1.0

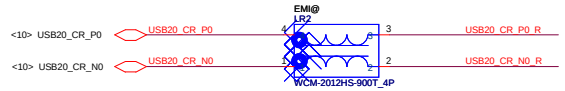
Date: Friday, February 13, 2015 | Sheet 19 of 56

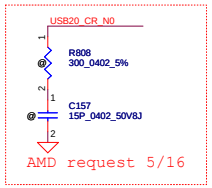
Main Func = WLAN

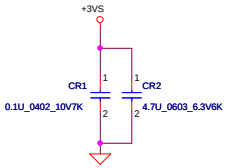


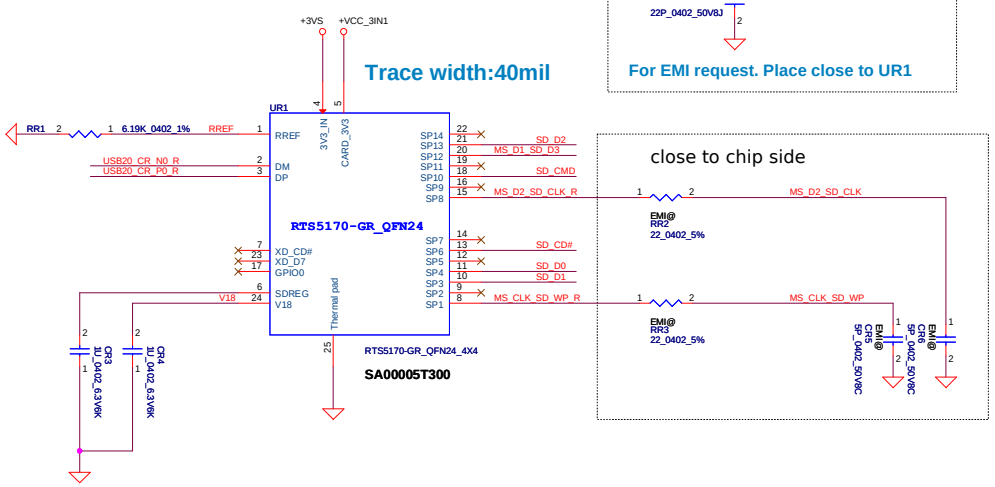
Compal Electronics, Inc.	
Title	NGFF WLAN
Size	Document Number: Tulip AAL12 LA-C142P
Rev	0.3
Date: Friday, February 13, 2015	Sheet 20 of 56

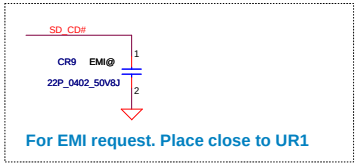
Main Func = Card Reader

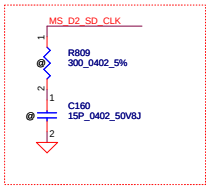


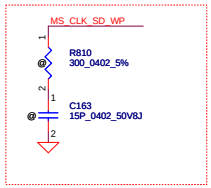


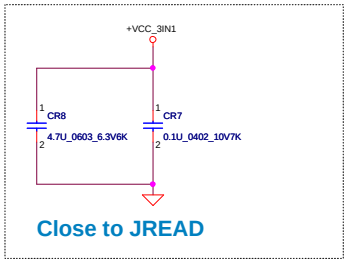


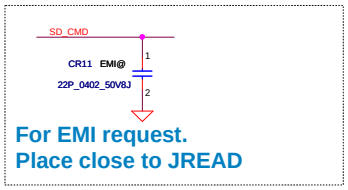


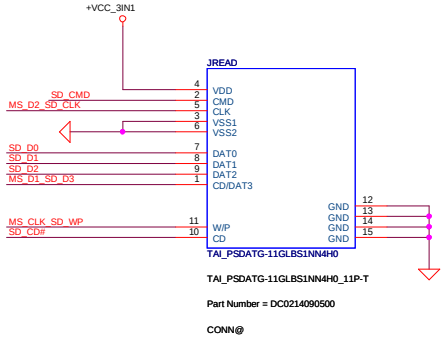












Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

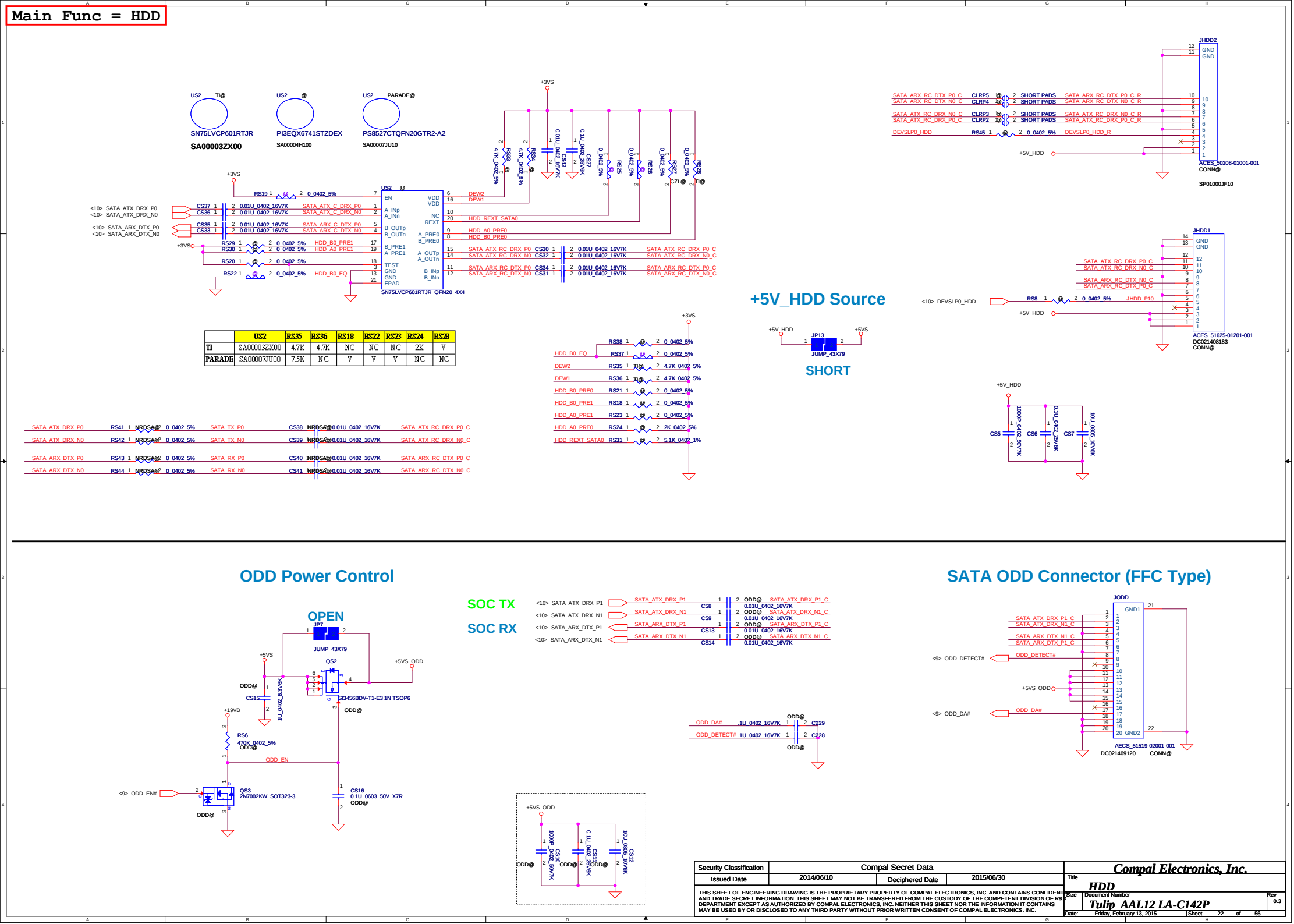
Compal Electronics, Inc.

Title: **Card Reader RTS5179**

Size | Document Number: **Tulip AAL12 LA-C142P** | Rev: 0.3

Date: Friday, February 13, 2015 | Sheet 21 of 56

Main Func = HDD



	US2	RS35	RS36	RS18	RS22	RS23	RS24	RS28
TI	SA00003ZX00	4.7K	4.7K	NC	NC	NC	2K	V
PARADE	SA00007JU00	7.5K	NC	V	V	V	NC	NC

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

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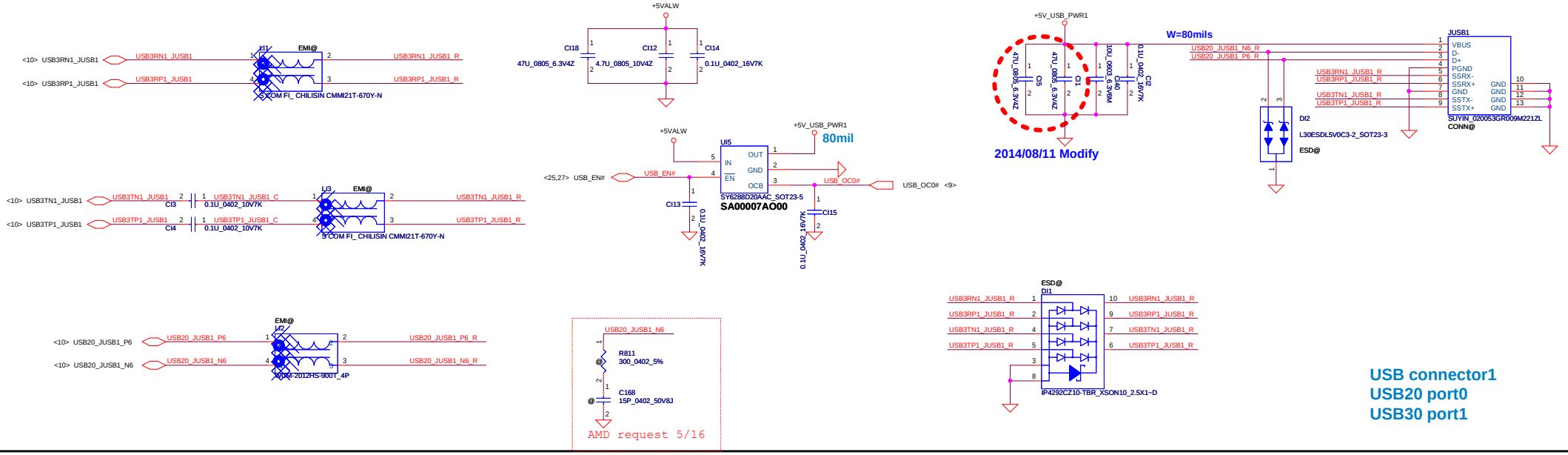
Compal Electronics, Inc.

Title: HDD

Size | Document Number: Tulip AAL12 LA-C142P | Rev: 0.3

Date: Friday, February 13, 2015 | Sheet 22 of 56

Main Func = USB3.0 Port1



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: USB3.0

Size | Document Number: Tulip AAL12 LA-C142P | Rev: 0.3

Date: Friday, February 13, 2015 | Sheet 23 of 56

Main Func = Touch Pad

Touch pad

From APU

FAN Control circuit

INT_KBD Connector

Main: SP01001H600 (CIS ok)

CZ: CZ_I2C@+TP_I2C@+PTP@
CZ-L: TPUSB@+TP_I2C@+PTP@

* Key Board Back Light

Main: SP01001UE00 (CIS ok)

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

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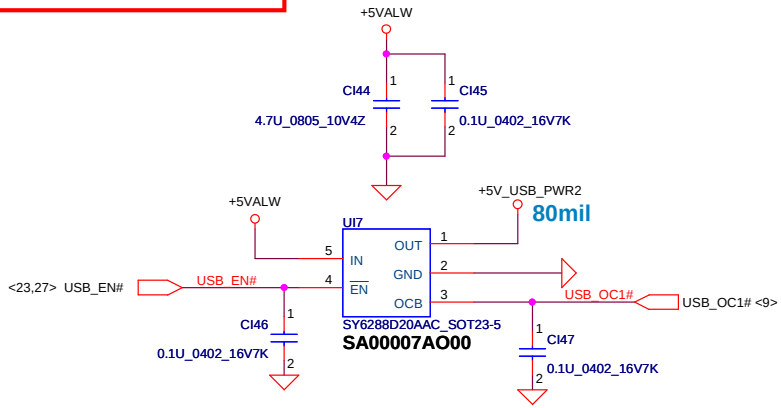
Compal Electronics, Inc.

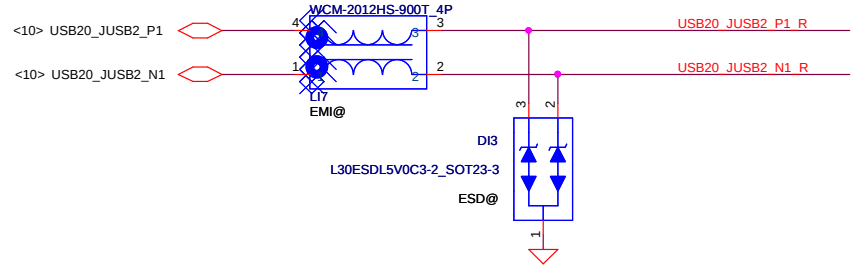
Title: FAN / TP / PWR SW / KBBL

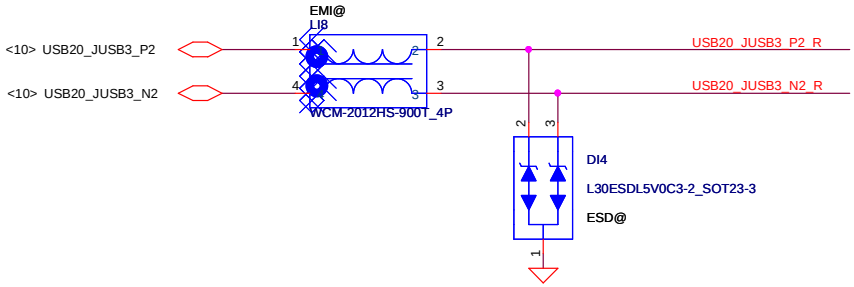
Size | Document Number: Tulip AAL12 LA-C142P | Rev: 0.3

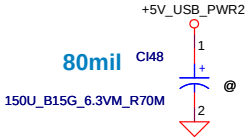
Date: Friday, February 13, 2015 | Sheet 24 of 56

Main Func = IO Connector



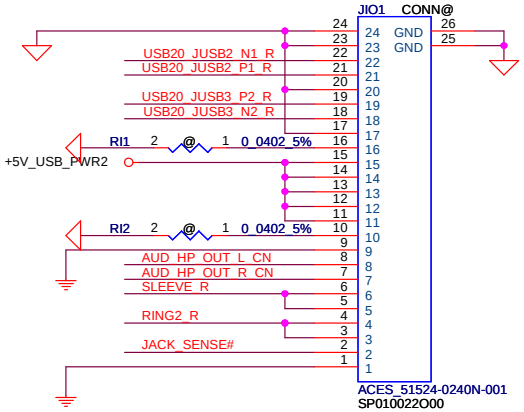


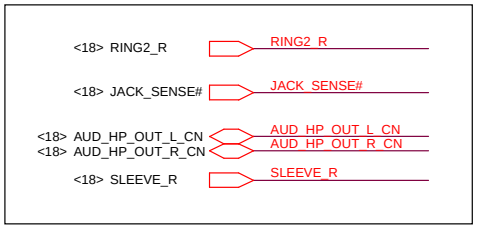




IO to MB CONN

Main: SP010022O00 (CIS ok)





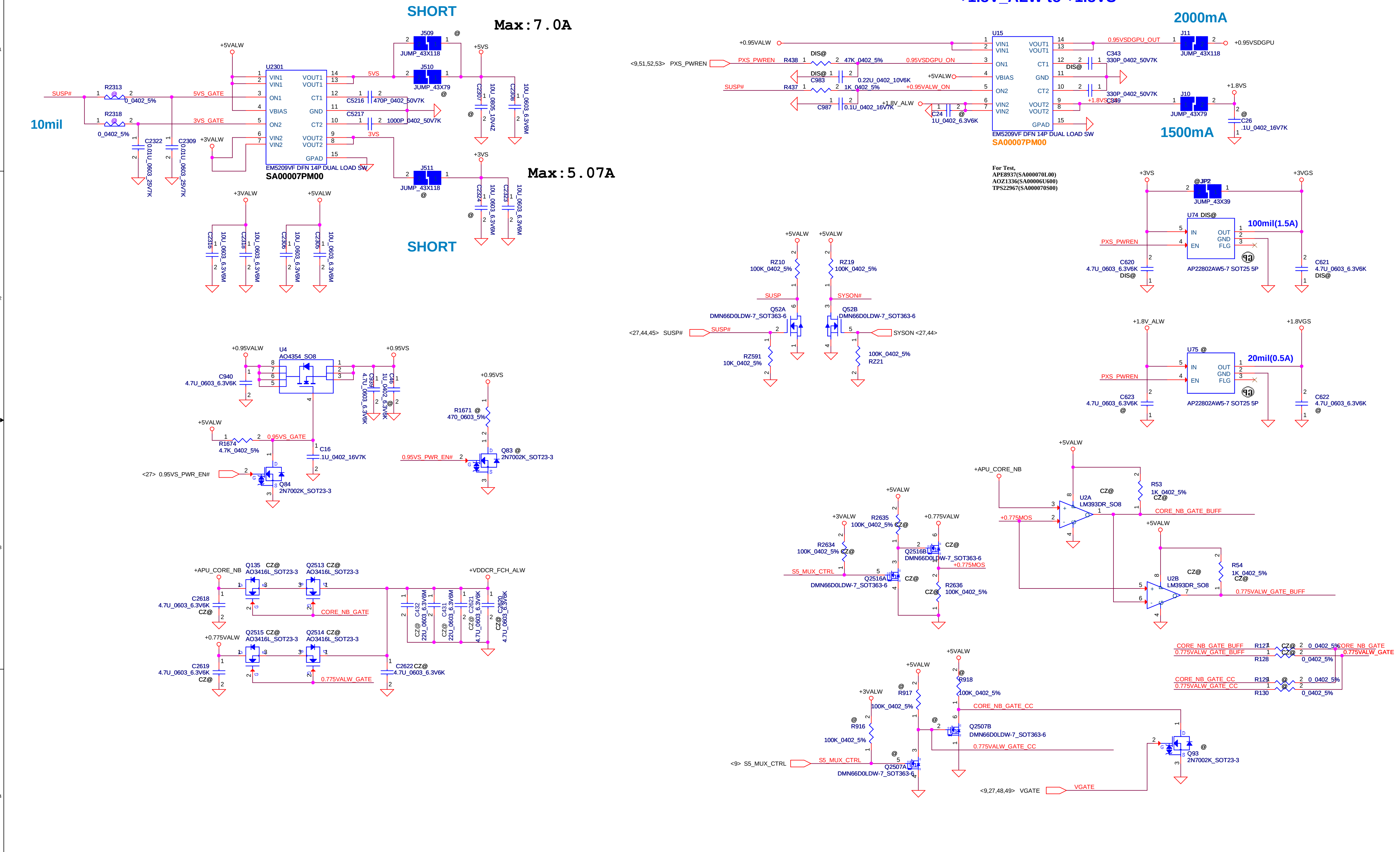
AUDIO Jack

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Title	IO-DB		
Size: B	Document Number: Tulip AAL12 LA-C142P		Rev: 0.3
Date: Friday, February 13, 2015	Sheet 25 of 56		

Main Func = DC Interface

+5VS and +3VS switch



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/06/10	Deciphered Date 2015/06/30	Title: DC/DC Interface
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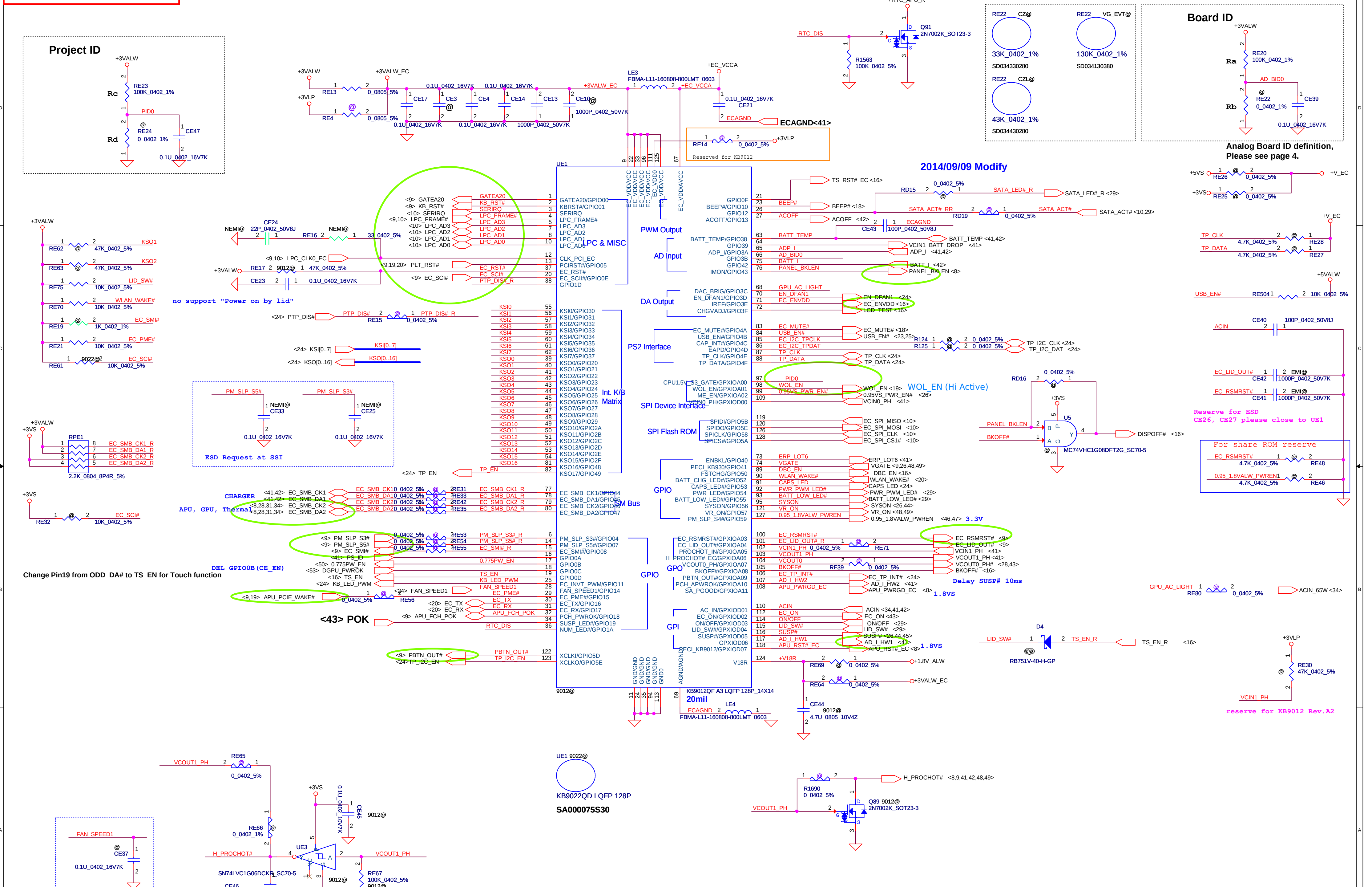
			Date: Friday, February 13, 2015 / Sheet 26 of 56

Main Func = KBC



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/06/10	Deciphered Date 2015/06/30	Title: EC ENE-KB9012A4/KB9022QC

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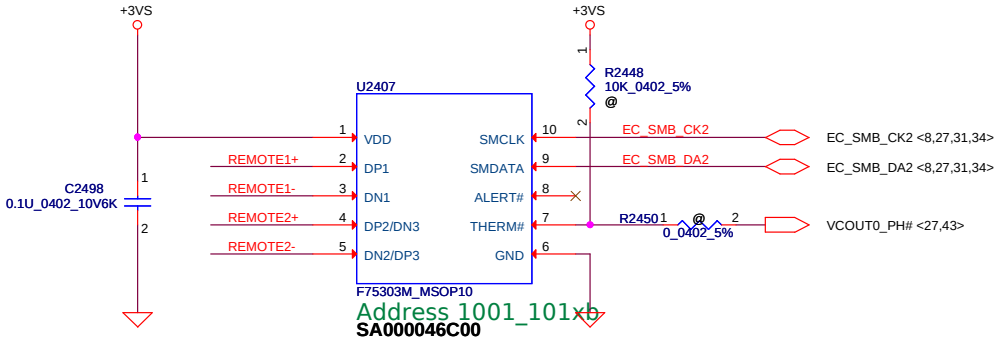
Size: Document Number: Tulip AAL12 LA-C142P — Rev 0.3

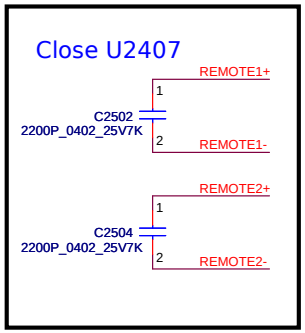
Date: Friday, February 13, 2015 — Sheet 27 of 56

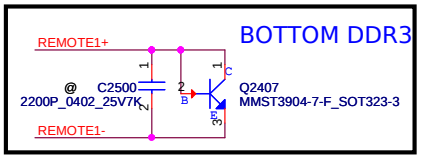
Main Func = Thermal Sensor

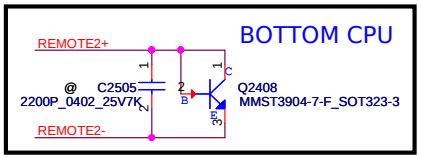
Fintek thermal sensor
placed near by TOP DDR3



2nd source
SA000029210-->EMC1403-2-AIZL-TR







REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: **Thermal Sensor**

Size: R&D | Document Number: **Tulip AAL12 LA-C142P** | Rev: 0.3

Date: Friday, February 13, 2015 | Sheet 28 of 56

Main Func = Power BTN

Battery LED1 (AMBER_LED)

Low actived from KBC GPIO

<27> BATT_LOW_LED#

BATT_LOW_LED# — R6105 0R2J-2-GP — BATT_LOW_LED_R#

Q6101 DDTA144VCA-7-F-GP

+5VALW

BATT_LOW_LED

R6103 470R2J-2-GP — BAT_AMBER

R6107 390R2J-3-GP — BAT_WHITE

LED1 LTW-327ZDSKS-5A 3X1 YELLOW/WHITE

Battery LED2 (WHITE_LED)

Low actived from KBC GPIO

<27> PWR_PWM_LED#

PWR_PWM_LED# — R6104 0R2J-2-GP — PWR_PWM_LED_R#

Q6102 DDTA144VCA-7-F-GP

+5VALW

PWR_PWM_LED

+3VS

R6110 10KR2J-3-GP

SATA_LED#_R

APU-->EC and LED

<10,27> SATA_ACT#

Q6103 2N7002KW_SOT323-3

SATA_LED#_B

Q6104 DDTA144VCA-7-F-GP

+5VS

SATA_LED

R6108 330R2J-3-GP

SATA_LED_R

HDLED1 LED-W-27-GP-U

2nd = 83.00110.R70

3rd = 083.11204.0070

R6106 0R2J-2-GP

SATA HDD LED

LOW actived from PCH GPIO

From EC

<27> SATA_LED#_R

Q6105 2N7002KW_SOT323-3

SATA_ACT#

PWR_PWM_LED_R#

For EMI Reserved

SATA_LED — EC6104 SCD1U16V2KX-3GP

ON/OFF switch

TOP Side

SW1 SMT1-05-A_4P

Pop only before MP

+3VLP

RE49 100K_0402_5%

ON/OFF <27>

CE20 0.1U_0402_16V7K

PWR/B TO M/B

<27> LID_SW#

LID_SW#

ON/OFF

+3VALW

JPWR CONN@ JXT_FP202DH-004M10M

C34 0.1U_0402_16V7K

C33 0.1U_0402_16V7K

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: Reserved Page

Size: C — Document Number: Tulip AAL12 LA-C142P — Rev: 0.3

Date: Friday, February 13, 2015 — Sheet 29 of 56

Main Func = Screw Hole

ZZZ

Part Number	Description
DA6001AL000	PCB 1AO LA-C142P REV0 M/B 3

PCB@

@ CLIP1
1 1
EMIST-SQ-26G_1P

@ CLIP2
1 1
EMIST-SQ-26G_1P

@ CLIP4
1 1
EMIST-SQ-26G_1P

Screw Hole

CPU bracket

Upper

H31 H_3P4 @ 1
H32 H_3P7 @ 1
H33 H_3P7 @ 1

GPU stand-off

H21 H_3P3 @ 1
H22 H_3P3 @ 1
H23 H_3P3 @ 1

FAN stand-off

H14 H_3P0 @ 1

FD1 @FIDUCAL
FD2 @FIDUCIAL
FD3 @FIDUCAL
FD4 @FIDUCIAL
FD5 @FIDUCAL
FD6 @FIDUCIAL

RJ45

H1 H_3P0 @ 1

HDMI

H2 H_3P0 @ 1
H3 H_3P0X3P8N @ 1

DDR RIGHT (TOP View)

H4 H_3P0 @ 1

APU RIGHT down (TOP View)

H5 H_3P0 @ 1

IO Conn Upper (TOP View)

H6 H_3P2 @ 1

VRAM Left Side (TOP View)

H7 H_3P2 @ 1
H8 H_4P0N @ 1

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

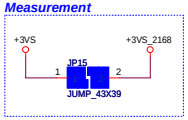
Title: Screw Hole

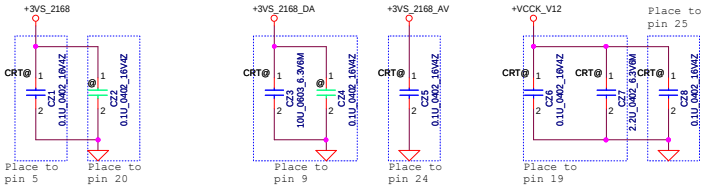
Size | Document Number: Tulip AAL12 LA-C142P | Rev: 0.3

Date: Friday, February 13, 2015 | Sheet 30 of 56

Main Func = VGA Translator

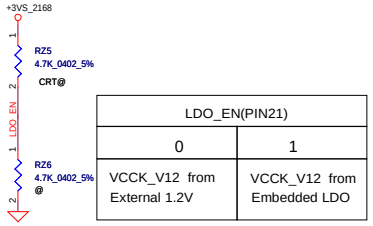
For Power consumption Measurement



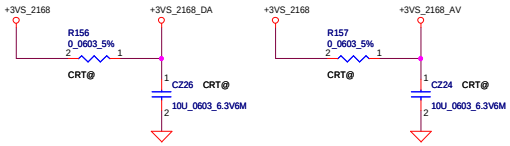


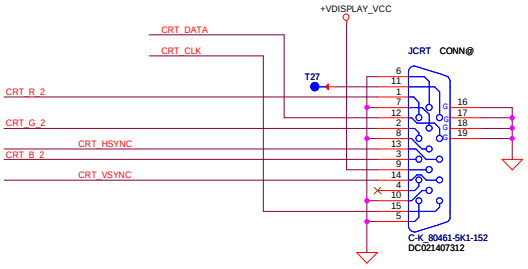
Embedded LDO

Select VCCK_V12 source from external 1.2V or embedded LDO

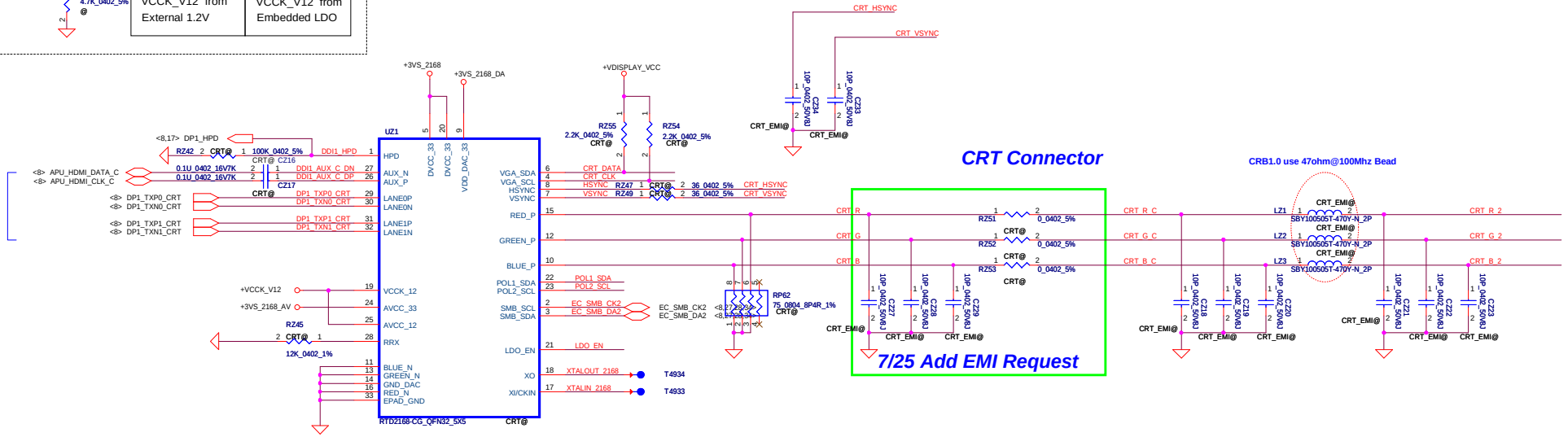


LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO



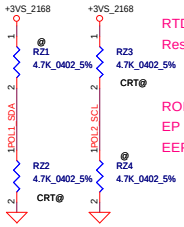


CRT Connector



Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE



RTD2168 Supports three operation mode for system design.
Reserve 4.7K resistor pull high/low for mode selection

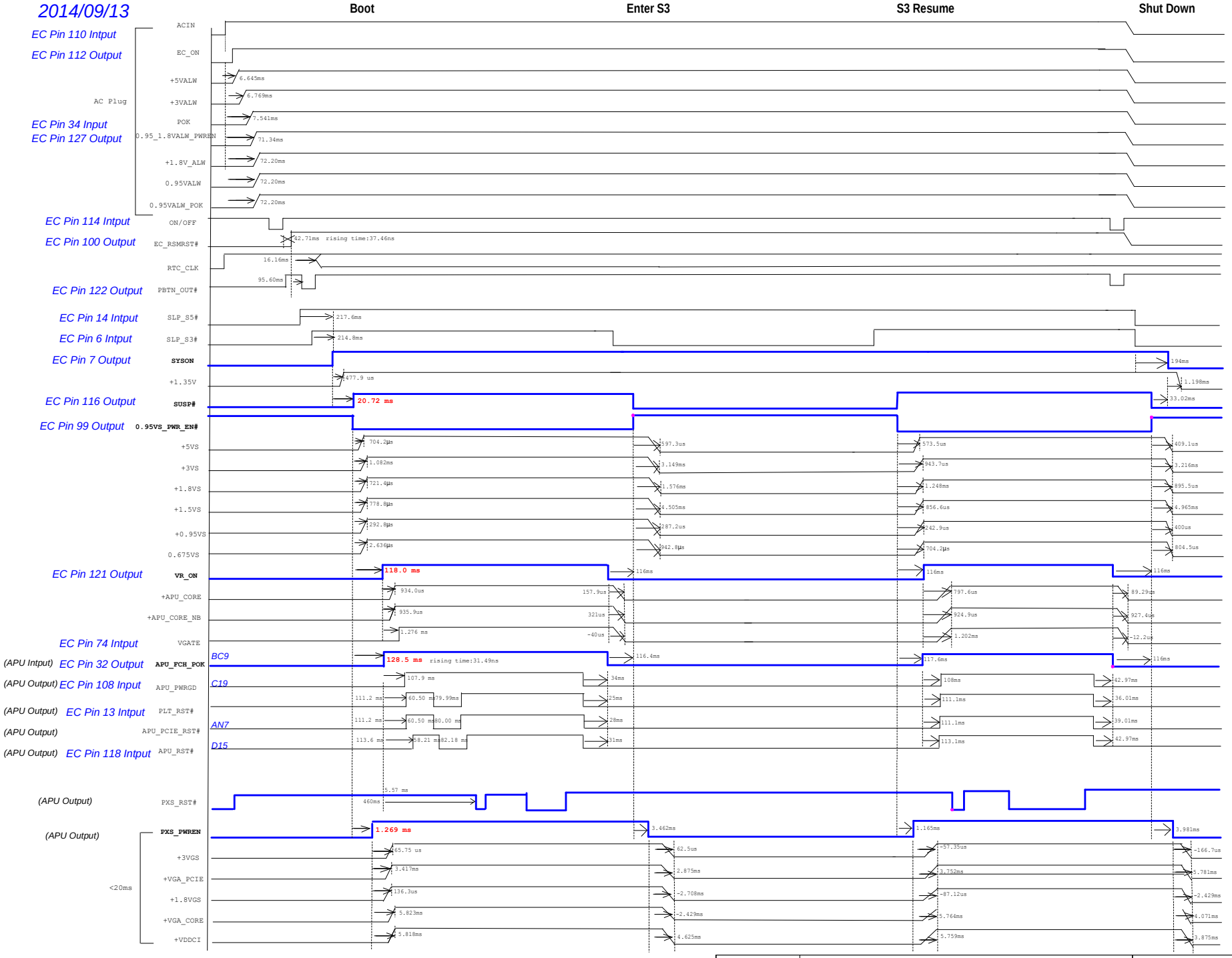
ROM ONLY Mode : PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title	VGA Translator-IT6513	
Size	Document Number: Tulip AAL12 LA-C142P	Rev 0.3
Date: Friday, February 13, 2015	Sheet 31 of 56	

2014/09/13



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

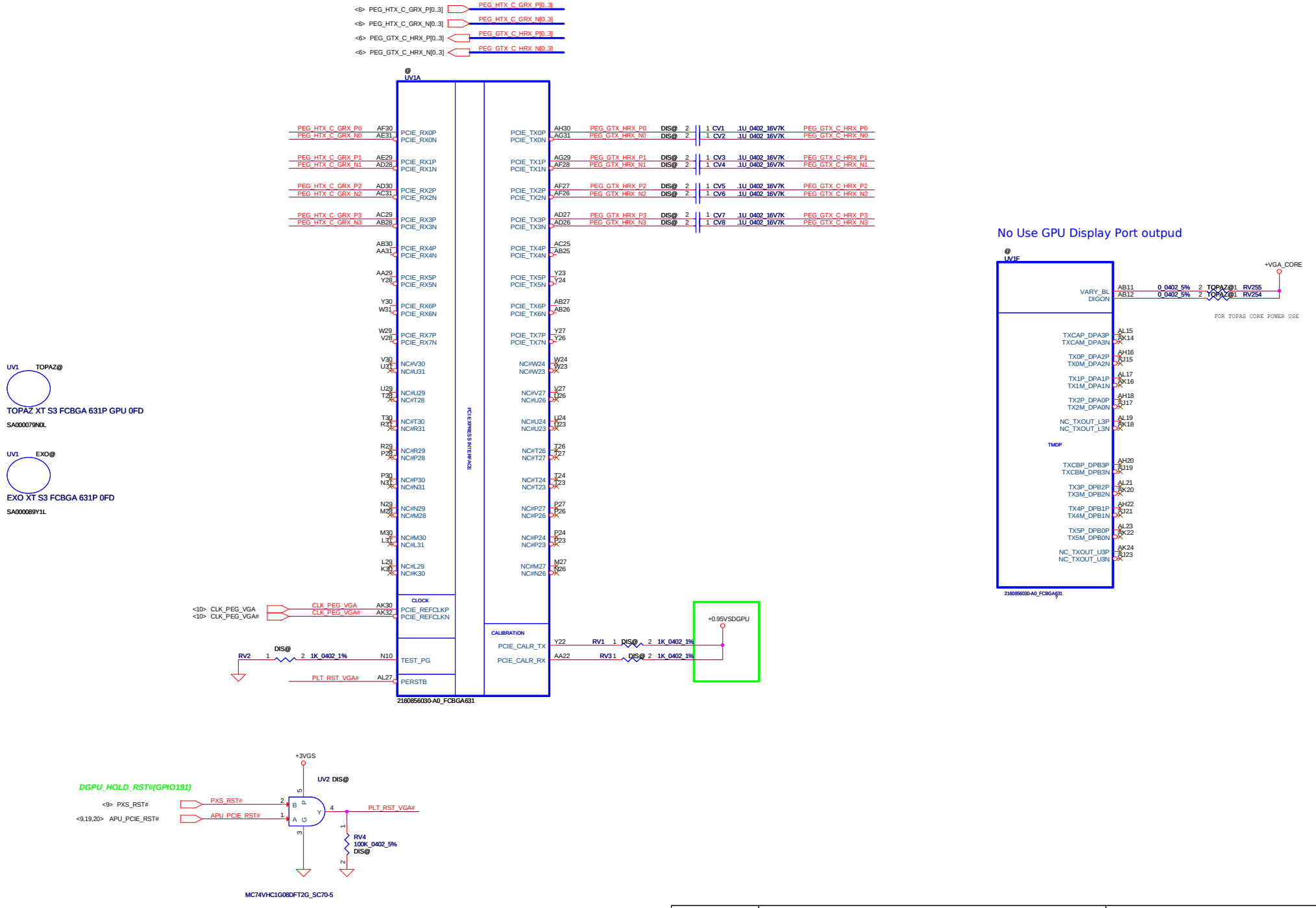
Compal Electronics, Inc.

Title: S5_MUX_CTRL

Size	Document Number	Rev
	Tulip AAL12 LA-C142P	0.3

Date: Friday, February 13, 2015 Sheet 32 of 56

Main Func = dGPU



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: TOPAZ_PCIE/DP

Size: Custom | Document Number: Tulip_AAL12 LA-C142P | Rev: 1.0

Date: Friday, February 13, 2015 | Sheet 33 of 56

Main Func = dGPU

Resistor Divider Lookup Lable		
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

PS_0[3:1]=001
PS_0[5:4]=11

PS_1[3:1]=000
PS_1[5:4]=11

PS_2[3:1]=000
PS_2[5:4]=01

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :

PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A

PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

2G_H@ -->Hynix
2G_S@ -->Samsung
2G_M@ -->Micron
2G_M2@-->Micron

SA010320110 (S IC ADM1032ARMZ MSOP 8P TEMP SENSOR)

Address:100_1101

For 2nd
SA000017Z710 (S IC EMC1402-2-ACZL-TR MSOP 8P SENSOR)
SA00003PU00 (S IC W83L771AWG-2 TSSOP 8P SENSOR)

U1 CPN is phase out

3.3V TO 1.8V LEVEL SHIF
For JET/SUN to support SVI2 reaulator
DNI for TOPAZ

Topaz SVI2

TOPAZ Thermal Address-->0x82

13mA

Enable MLPS

Enable --> Low
Disenable --> High

Peak Current Control (PCC) CKT Reversed

Memory ID	P/N	Vendor	Configuration	Size
SSI (default) 000	SA000076P2L	SAMSUNG	K4W4G1646E-BC1A	2GB
001	SA00008DN1L	HYNIX	H5TC4G63CFR-N0C	2GB
010	SA000065D1L	Micron	MT41K256M16HA-107G	2GB
011	SA000077K1L	Micron	MT41J256M16HA-093G:E	2GB
100	NA	NA	NA	NA
101	NA	NA	NA	NA

Tulip AMD 2G VRAM Only

Short_pad
RV158
RV159
RV60

Security Classification:	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

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Compal Electronics, Inc.

Title: TOPAZ_MSIC

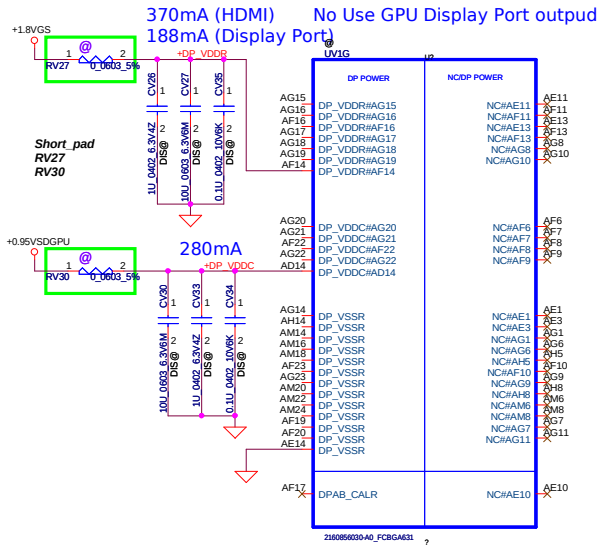
Size: Custom | Document Number: Tulip_AAL12 LA-C142P | Rev: 0.3

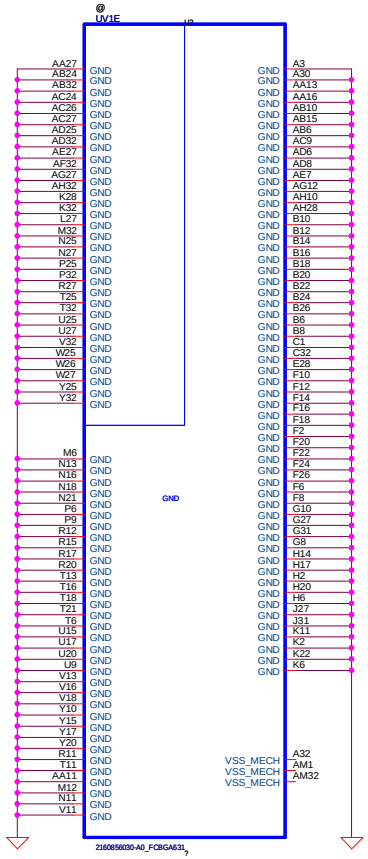
Date: Friday, February 13, 2015 | Sheet 34 of 56

Main Func = dGPU

+1.35VS_VGA TO +1.35V_MEM_GFX

JP9 DEFAULT SHORT





Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: TOPAZ_Power/GND

Size: Custom | Document Number: Tulip_AAL12 LA-C142P | Rev: 1.0

Date: Friday, February 13, 2015 | Sheet 35 of 56

Main Func = dGPU

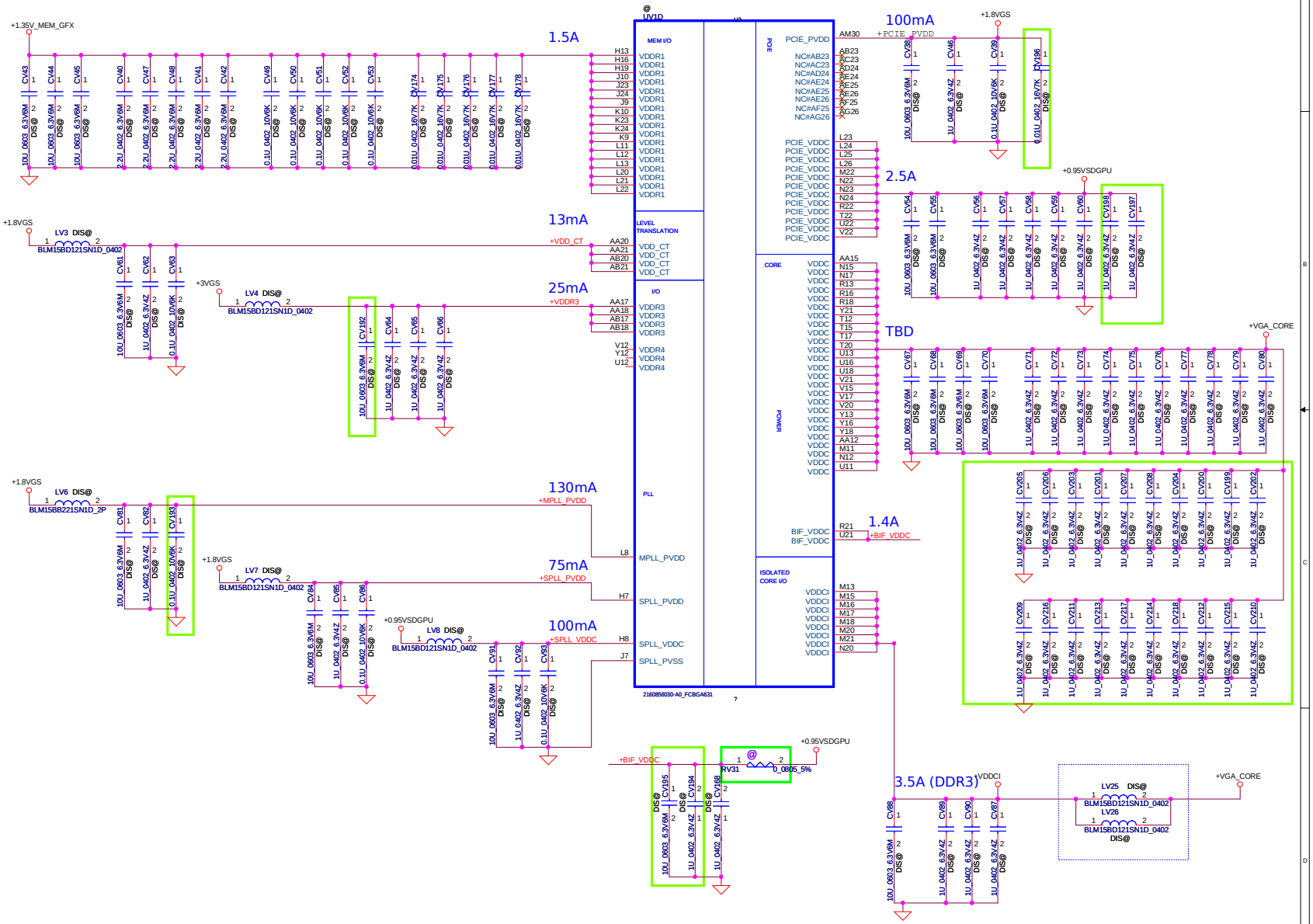
+VGA_CORE	10uF	1uF	0.1uF
VDDC TBD	5 (1@)	10 (2@)	0
VDDCI 3.5A	1	3	0

+0.95VSDGPU	10uF	1uF	0.1uF
PCIE_VDDC 2.5A	2 (1@)	5 (1@)	0
BIF_VDDC 1.4A	0	1	0
SPLL_VDDC 100mA	1	1	1

+1.35V_MEM_GFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1 1.5A	3	5	5	5

+1.8VGS	10uF	1uF	0.1uF
PCIE_PVDD 100mA	1	1	1
MPLL_PVDD 130mA	1	1	1
SPLL_PVDD 75mA	1	1	1
VDDR4 (300mA)	0	0	0
VDD_CT 13mA	1	1	1
+TSVDD 13mA	1	1	1
+DP_VDDR	0	0	0
+DP_VDDC	0	0	0

+3VGS	10uF	1uF	0.1uF
VDDR3 25mA	0	2 (1@)	1



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

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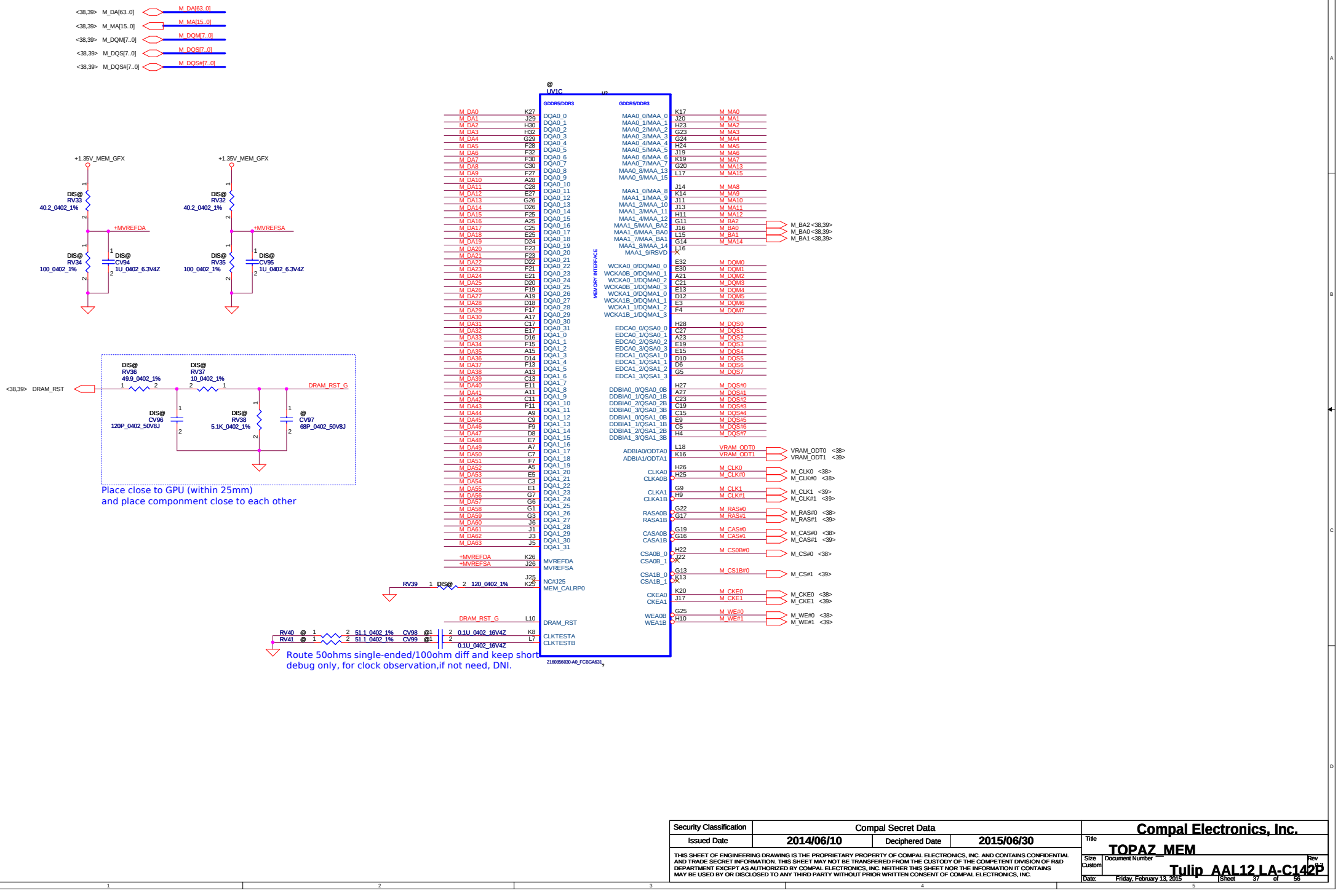
Compal Electronics, Inc.

Title: **TOPAZ_Power**

Size: Custom | Document Number: **Tulip_AAL12 LA-C142P** | Rev: 1.0

Date: Friday, February 13, 2015 | Sheet 36 of 56

Main Func = dGPU



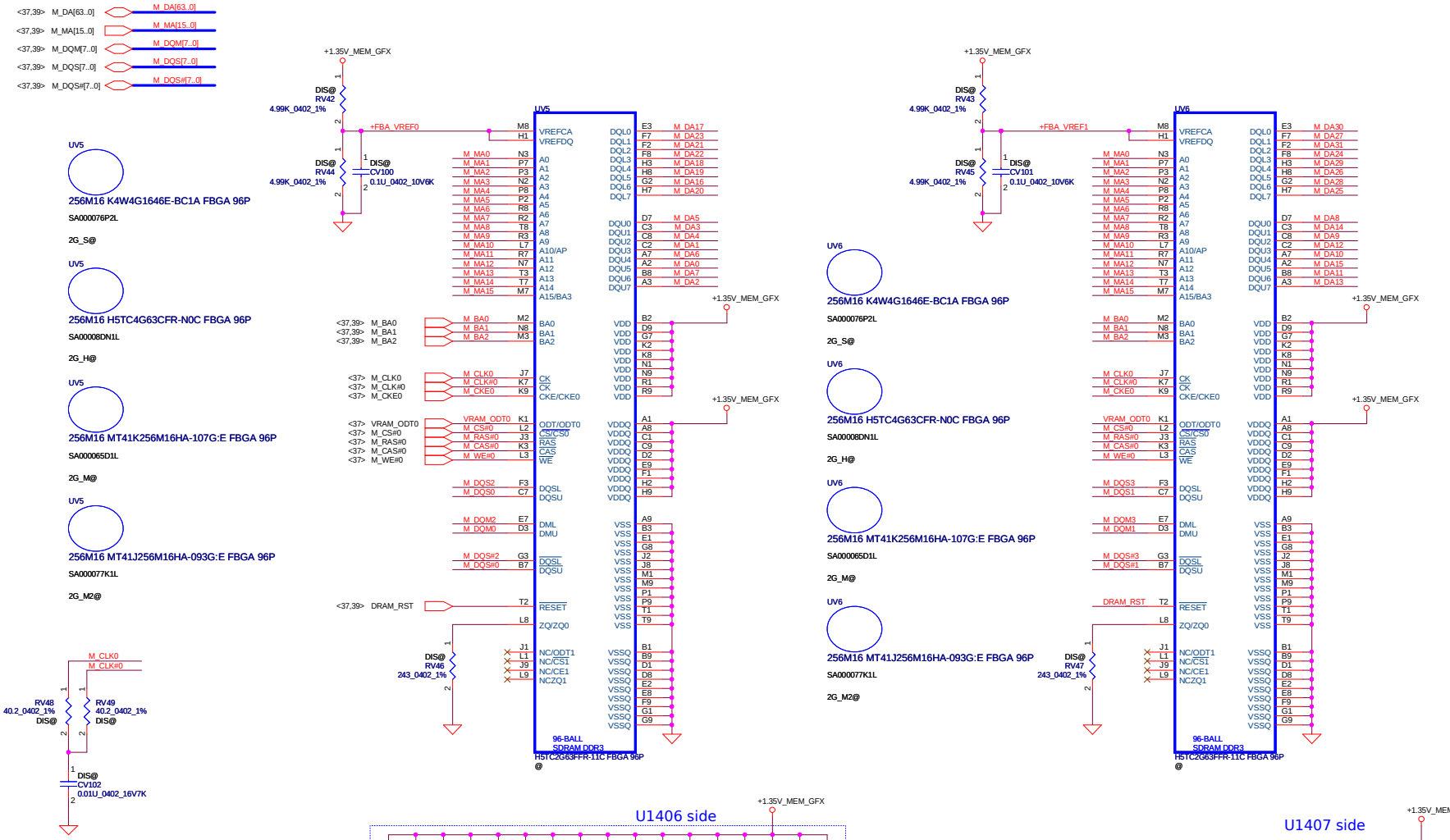
Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title	TOPAZ_MEM	
Size: Custom	Document Number: Tulip_AAL12 LA-C142P	Rev: 1.0
Date: Friday, February 13, 2015	Sheet 37 of 56	

Main Func = dGPU

Memory Partition A - Lower 32 bits



X7655131L04, ALT. GROUP PARTS VRAM 2G HYNIX ZAVC0, A.2 (Design)			
	SA00006E80L, S IC D3 256MX16 H5TC4G63AFR-11C FBGA 96P, A.1 (Design)		
	SD034453180, S RES 1/16W 4.53K +-1% 0402, A.1 (Design)		
	SD034499180, S RES 1/16W 4.99K +-1% 0402, A.2 (Design)		
X7655131L05, ALT. GROUP PARTS VRAM 2G SAMSUNG ZAVC0, A.2 (Design)			
	SA000076P0L, S IC D3 256MX16 K4W4G1646D-BC1A FBGA 96P, A.2 (Design)		
	SD000002680, S RES 1/16W 6.98K +-1% 0402, A.1 (Design)		
	SD034499180, S RES 1/16W 4.99K +-1% 0402, A.2 (Design)		
X7655131L06, ALT. GROUP PARTS VRAM 2G MICRON ZAVC0, A.2 (Design)			
	SA000077K0L, S IC D3 256M16 MT41J256M16HA-093G:E FBGA, A.4 (Design)		
	SD034324180, S RES 1/16W 3.24K +-1% 0402, A.1 (Design)		
	SD034562180, S RES 1/16W 5.62K +-1% 0402, A.1 (Design)		

Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

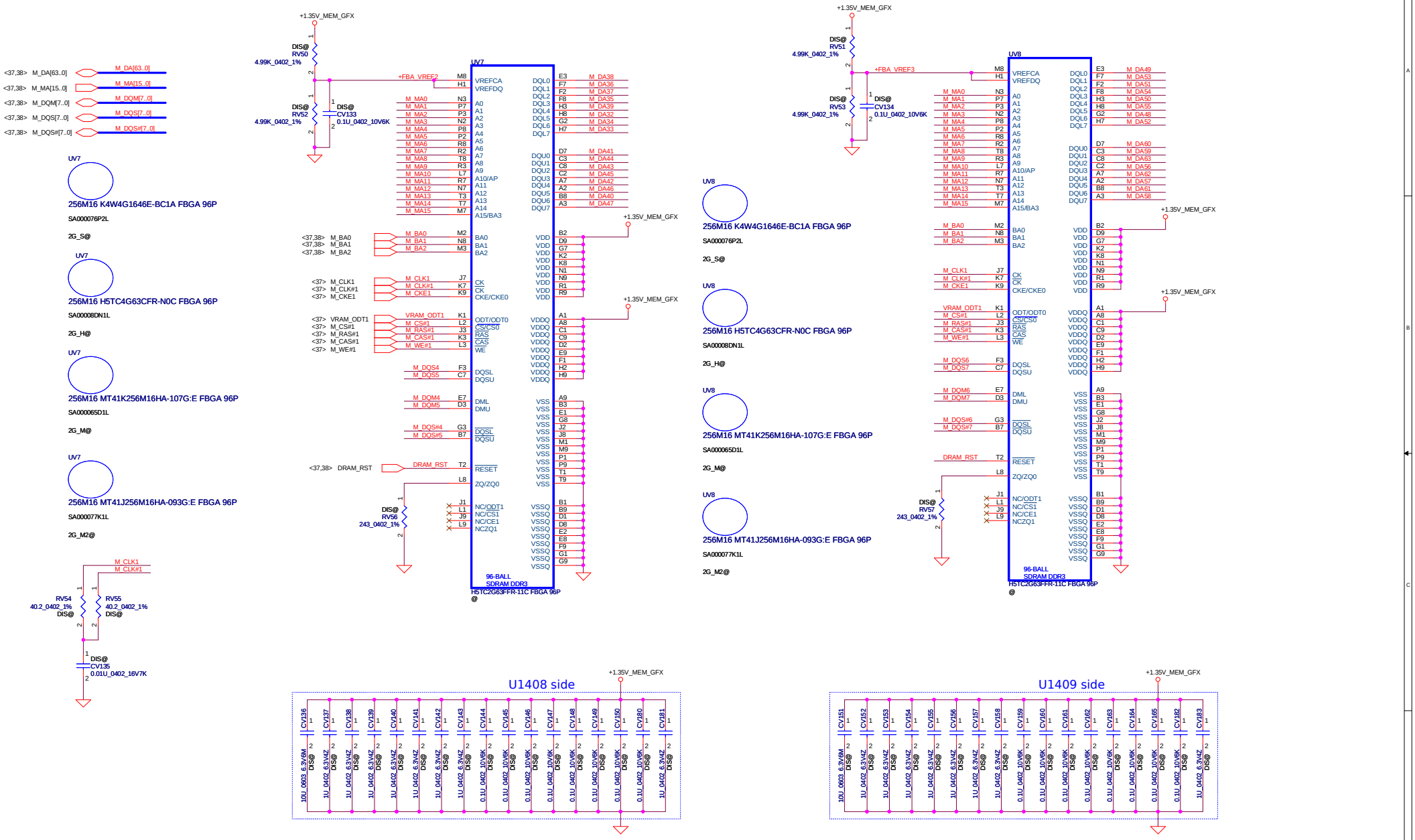
Title: TOPAZ_VRAM A Lower

Size: Custom | Document Number: Tulip_AAL12 LA-C142P | Rev: 0.3

Date: Friday, February 13, 2015 | Sheet 38 of 56

Main Func = dGPU

Memory Partition A - Upper 32 bits



Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: TOPAZ_VRAM A Upper

Size: Custom | Document Number: Tulip_AAL12 LA-C142P | Rev: 0.3

Date: Friday, February 13, 2015 | Sheet 39 of 56

Main Func = dGPU

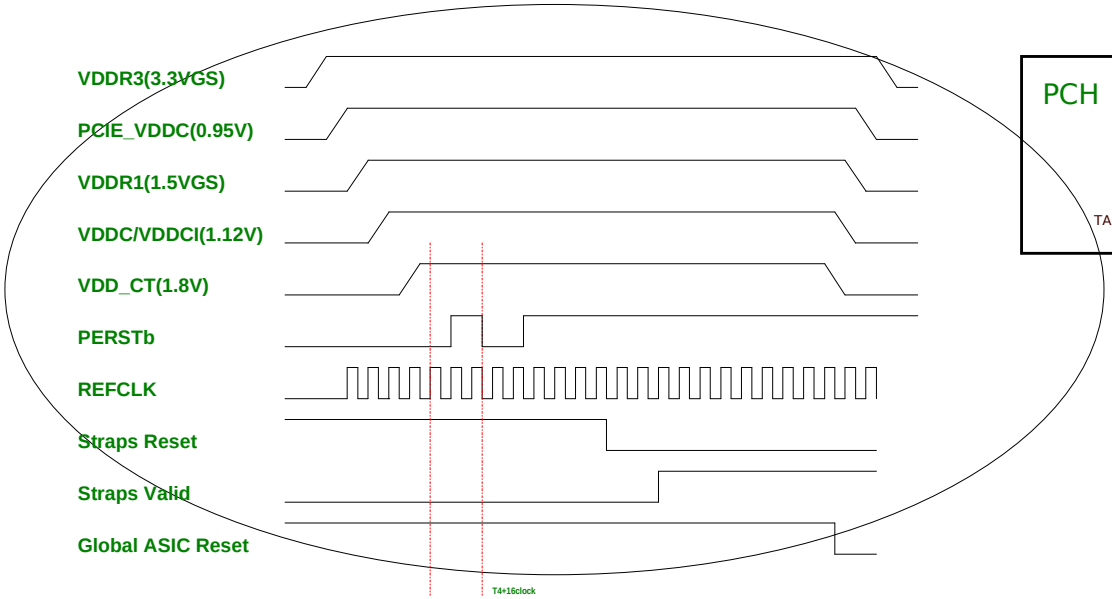
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

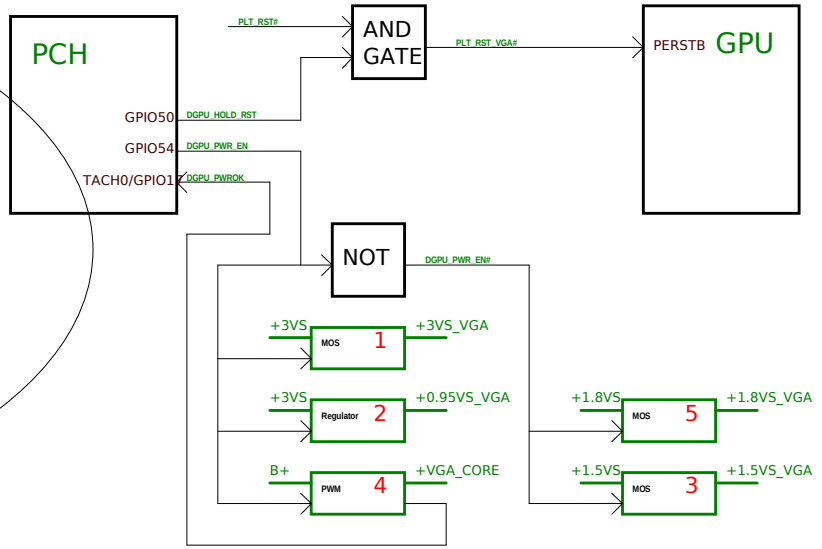
2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.

3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).

4. For power down, reversing the ramp-up sequence is recommended.



CPU part



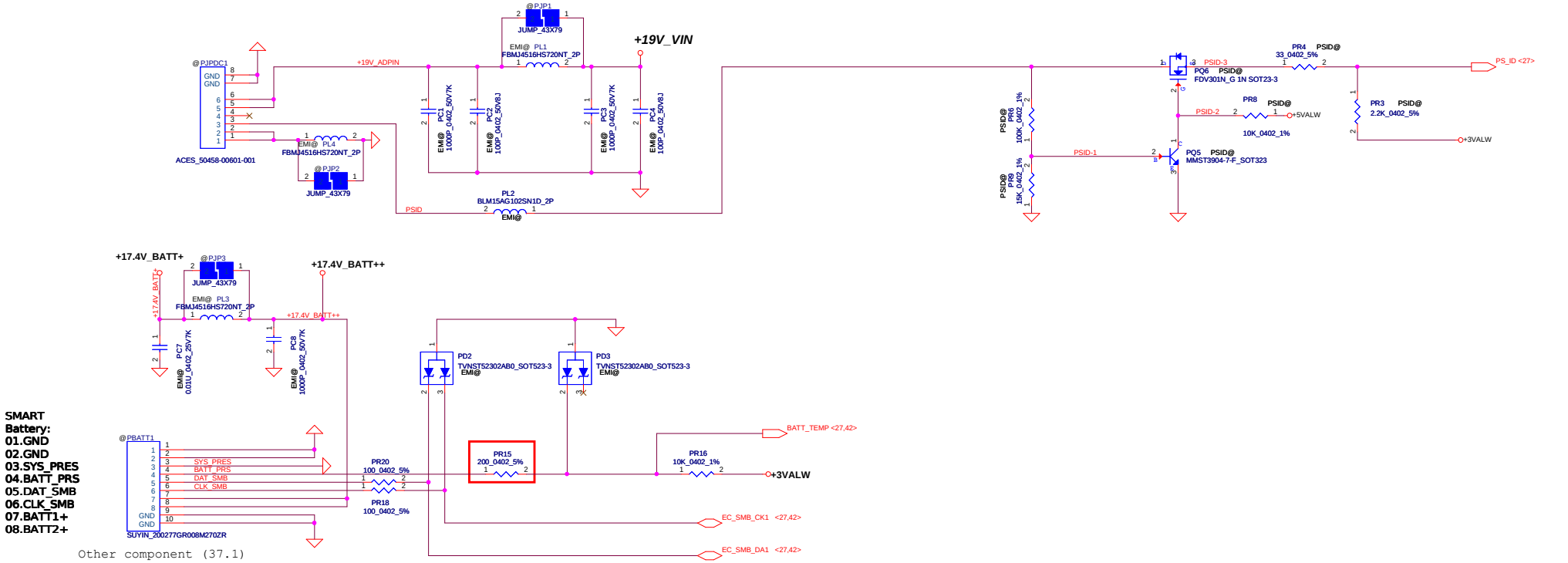
Security Classification	Compal Secret Data		
Issued Date	2014/06/10	Deciphered Date	2015/06/30

Compal Electronics, Inc.

Title: TOPAZ_NOTE

Size	Document Number	Rev
	Tulip AAL12 LA-C142P	0.3

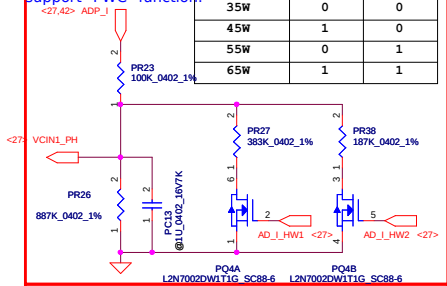
Date: Friday, February 13, 2015 Sheet 40 of 56



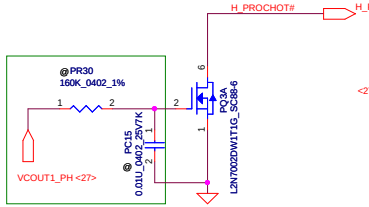
Other component (37.1)

ADP_I(with selector) to support "PWC" function.

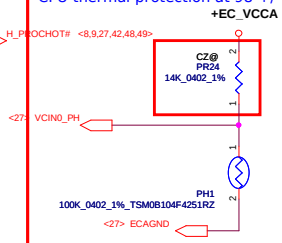
H_PROCHOT#	AD_I_HW1	AD_I_HW2
35W	0	0
45W	1	0
55W	0	1
65W	1	1



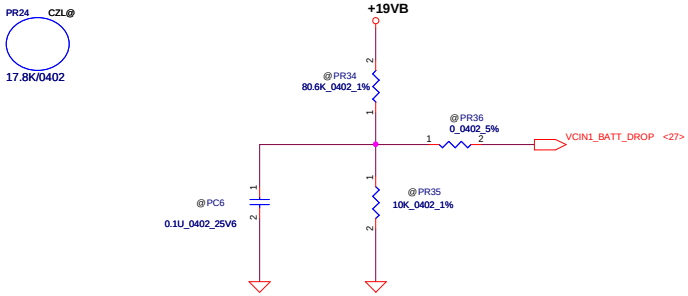
Delay adaptor OC H_PROCHOT# 2ms while hybrid power transition



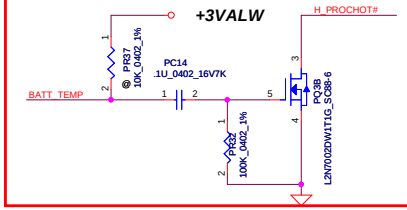
PH1 under CPU bottem side :(Carrizo)
CPU thermal protection at 98 +/- 3 degree C



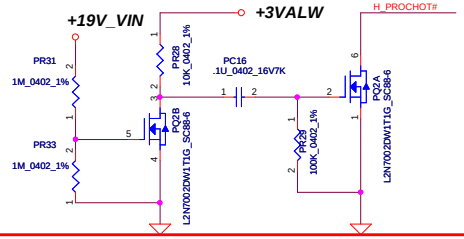
PH1 under CPU bottem side :(Carrizo-L)
CPU thermal protection at 90 +/- 3 degree C



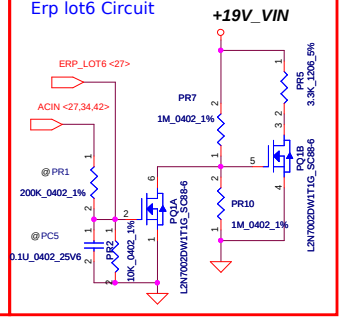
Adapter protection:
if battery removed, adaptor only, then trigger the H_PROCHOT#, keep @ in BOM since battery can not be removed by end user



Battery protection:
asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC



Erp lot6 Circuit



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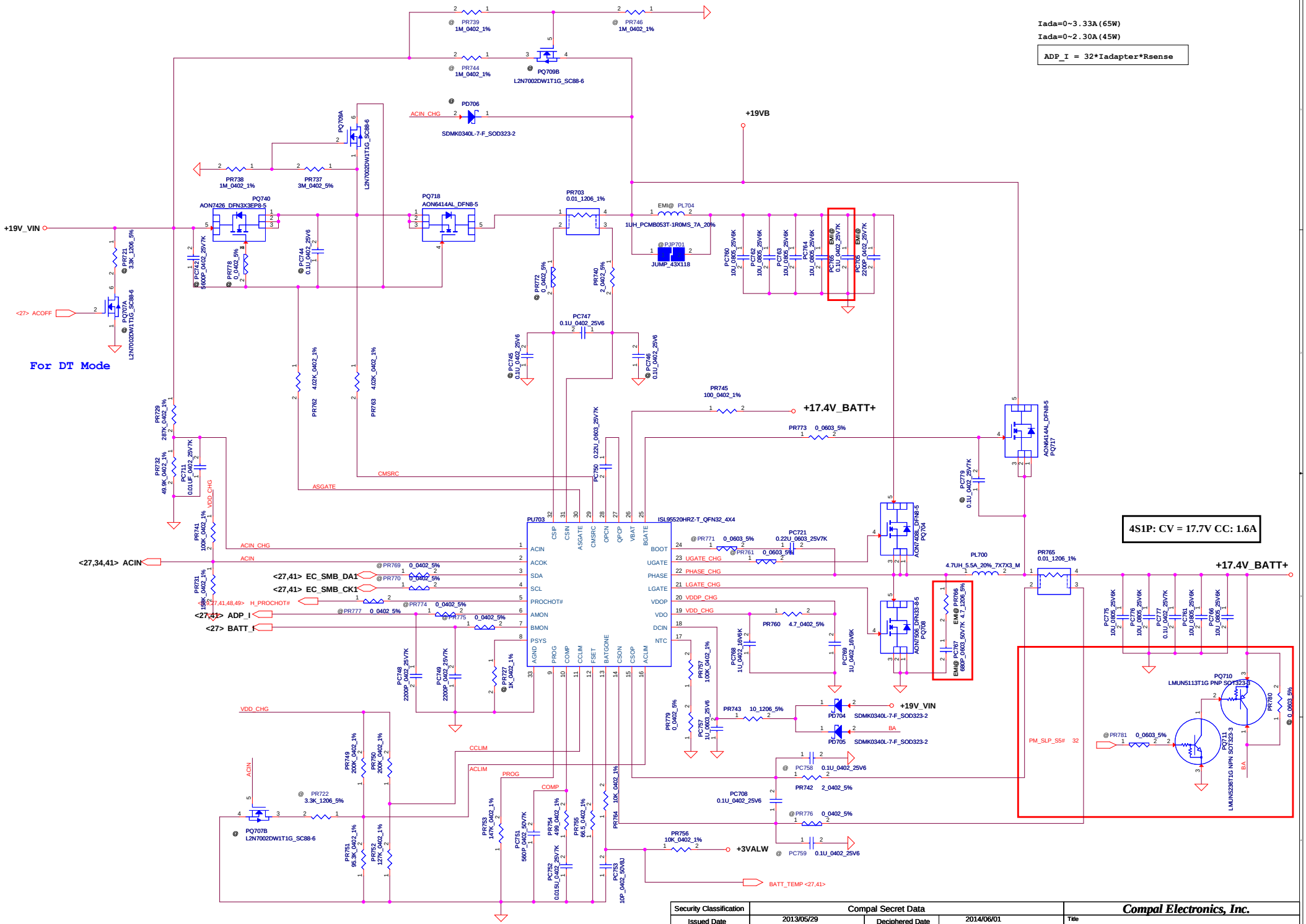
Issued Date	2013/10/01	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: PWR_DCIN/BATT CONN/OTP

Size: | Document Number: LA-C142P | Rev: 0.1

Date: Friday, February 13, 2015 | Sheet 41 of 56



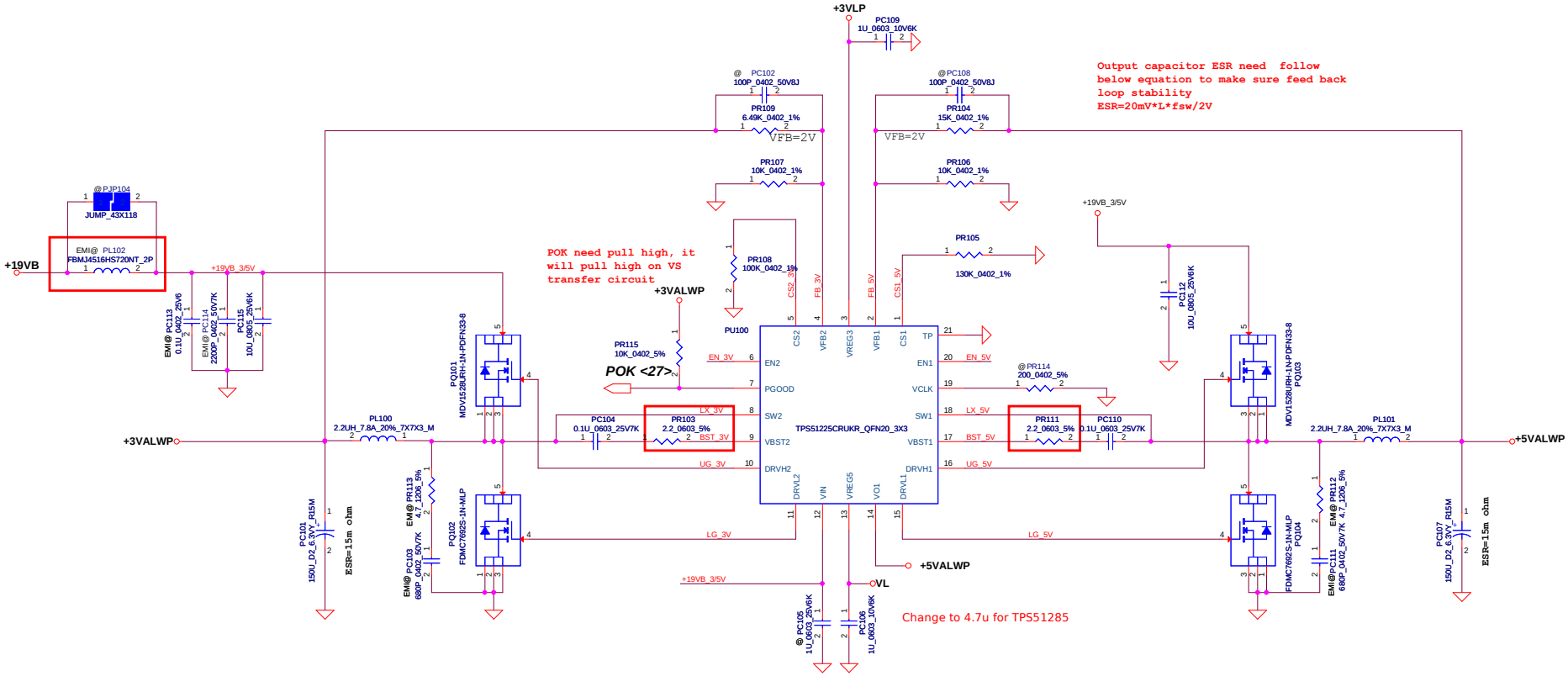
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: **PWR_CHARGER**

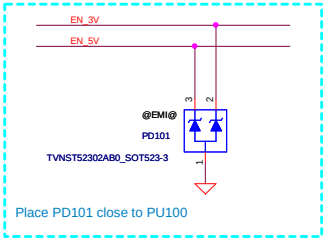
Size	Document Number	Rev
	LA-C142P	0.1

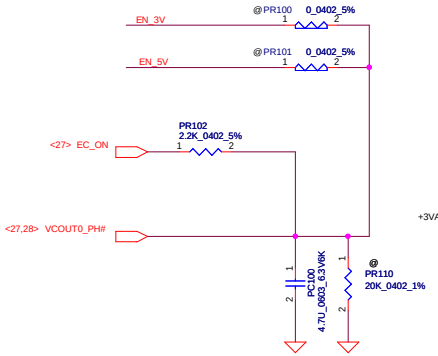
Date: Friday, February 13, 2015 | Sheet 42 of 56



3VALWP
TDC 4.9A
Peak Current 7A
OCP current 9.1A

	TYP	MAX
H/S Rds(on)	23.2mohm	27.8mohm
L/S Rds(on)	10.8mohm	13.6mohm





5VALWP
TDC 6A
Peak Current 10A
OCP current 12A

	TYP	MAX
H/S Rds(on)	23.2mohm	27.8mohm
L/S Rds(on)	10.8mohm	13.6mohm

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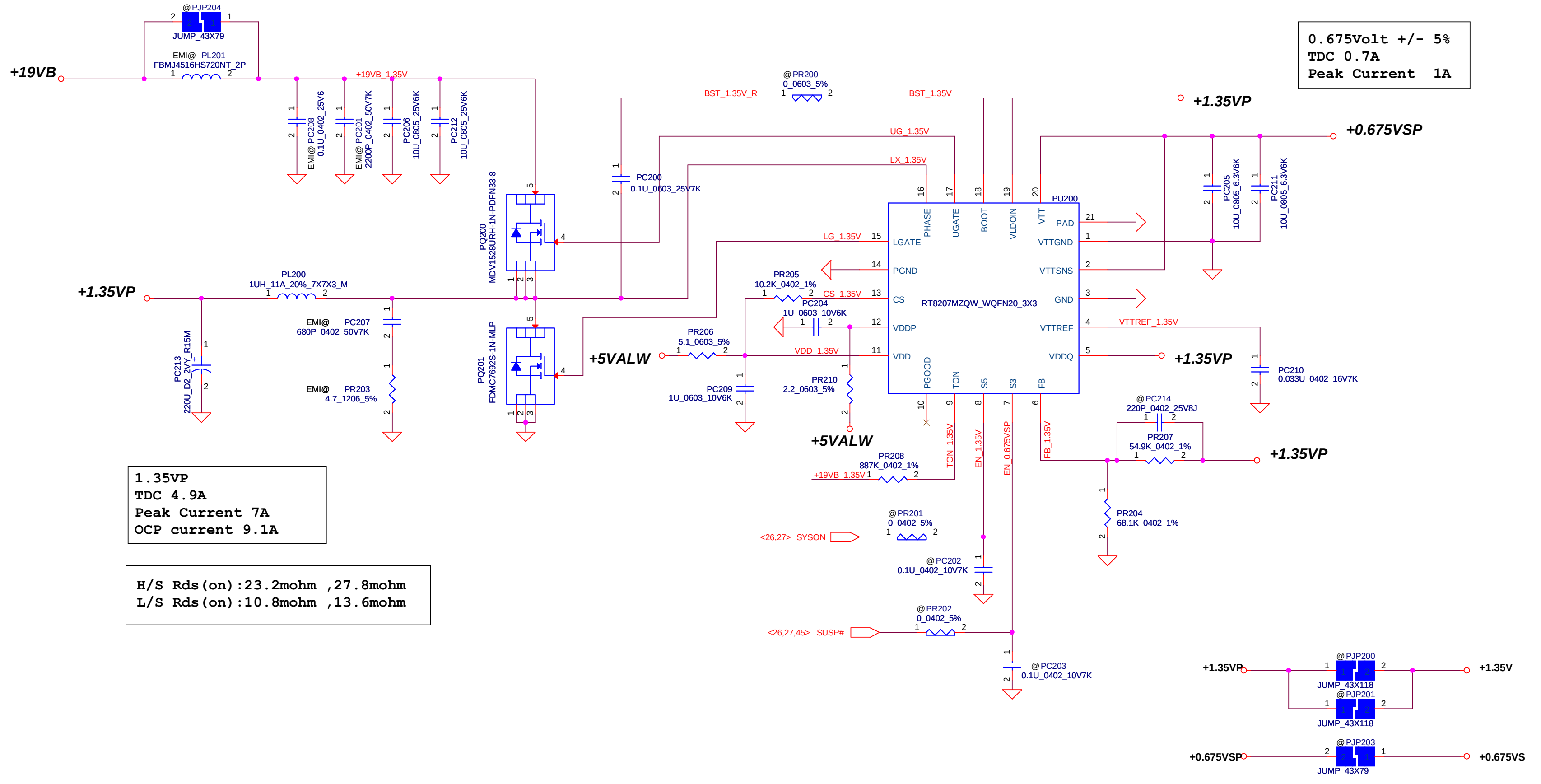
Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

Size | Document Number: LA-C142P | Rev: 0.1

Date: Friday, February 13, 2015 | Sheet 43 of 56



0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

1.35VP
TDC 4.9A
Peak Current 7A
OCP current 9.1A

H/S Rds(on):23.2mohm ,27.8mohm
L/S Rds(on):10.8mohm ,13.6mohm

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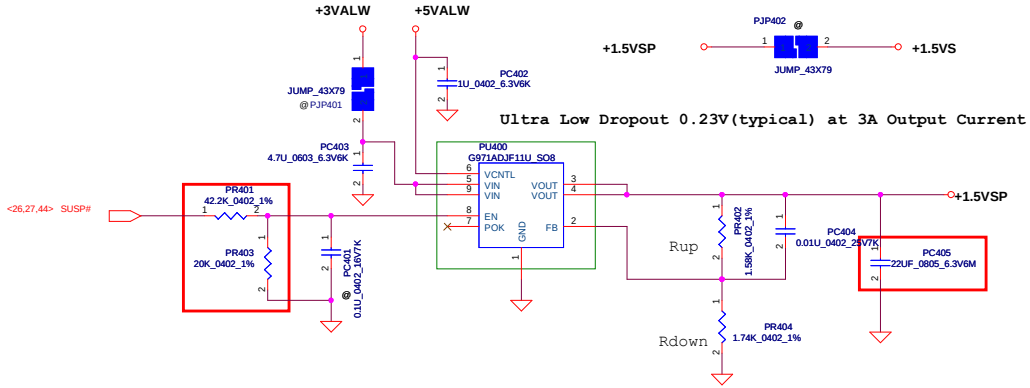
Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: *PWR_+1.35VP/0.675VSP*

Size | Document Number: LA-C142P | Rev: 0.1



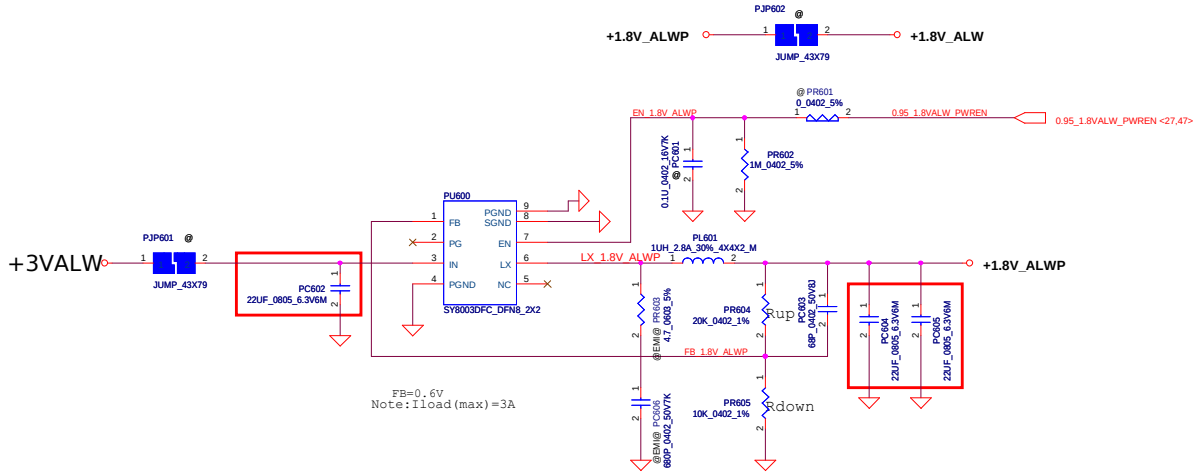
Security Classification	Compal Secret Data		
Issued Date	2014/03/31	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: **PWR_1.5VSP**

Size	Document Number	Rev
	LA-C142P	0.1

Date: Friday, February 13, 2015 | Sheet 45 of 56



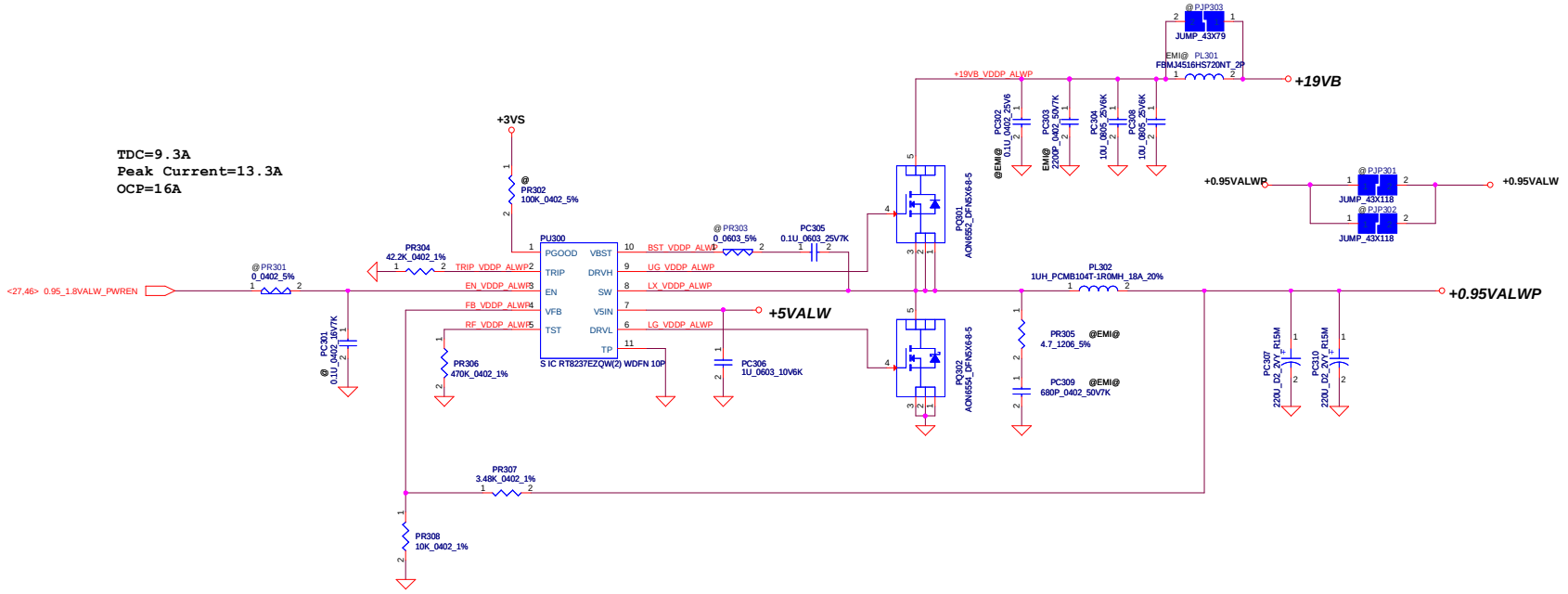
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: PWR_+1.8V_ALWP

Size	Document Number	Rev
C	LA-C142P	1.0

Date: Friday, February 13, 2015 Sheet 46 of 56



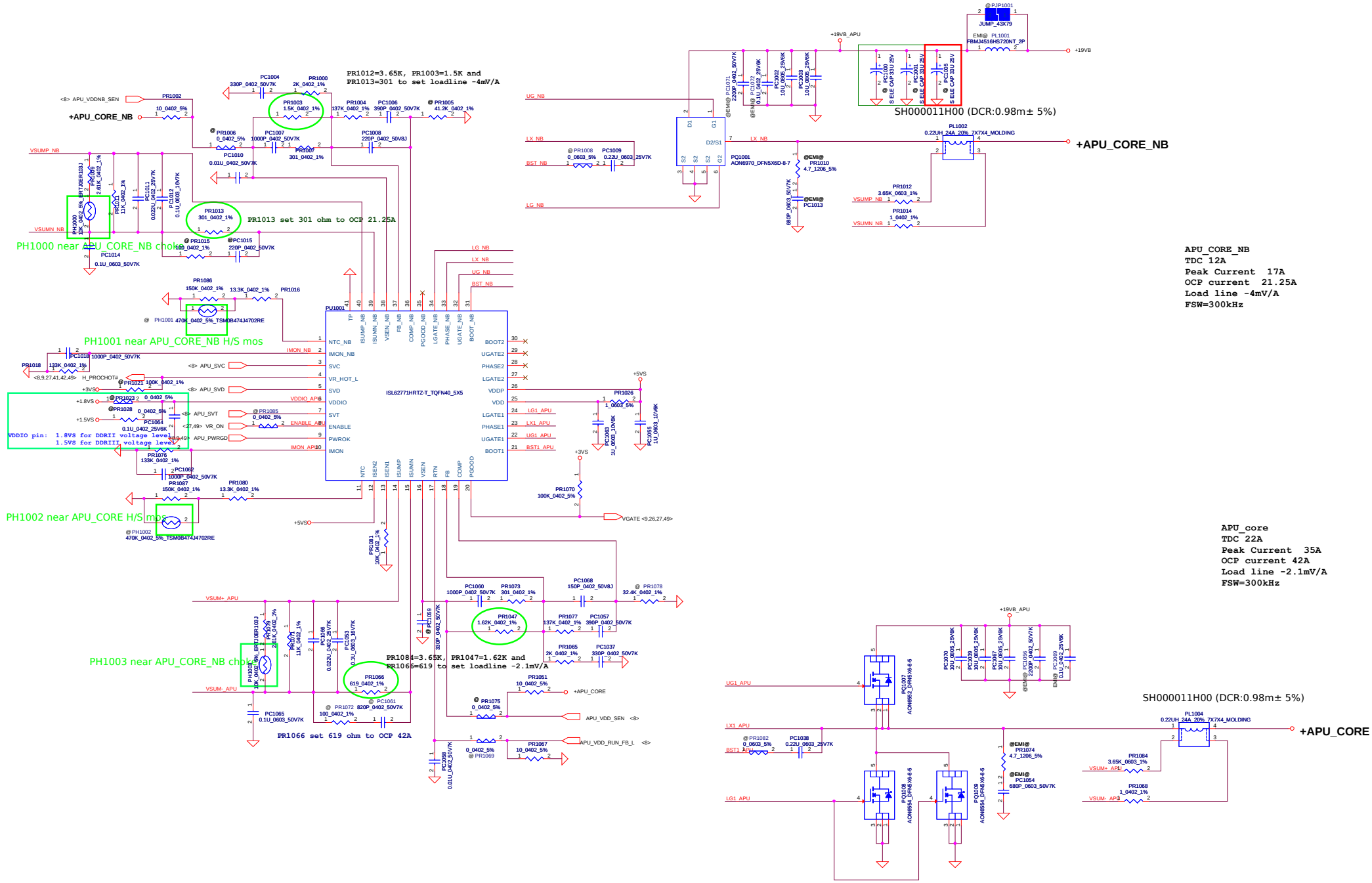
Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.

Title: P45-PWR_VDDP_ALWP(+0.95V)

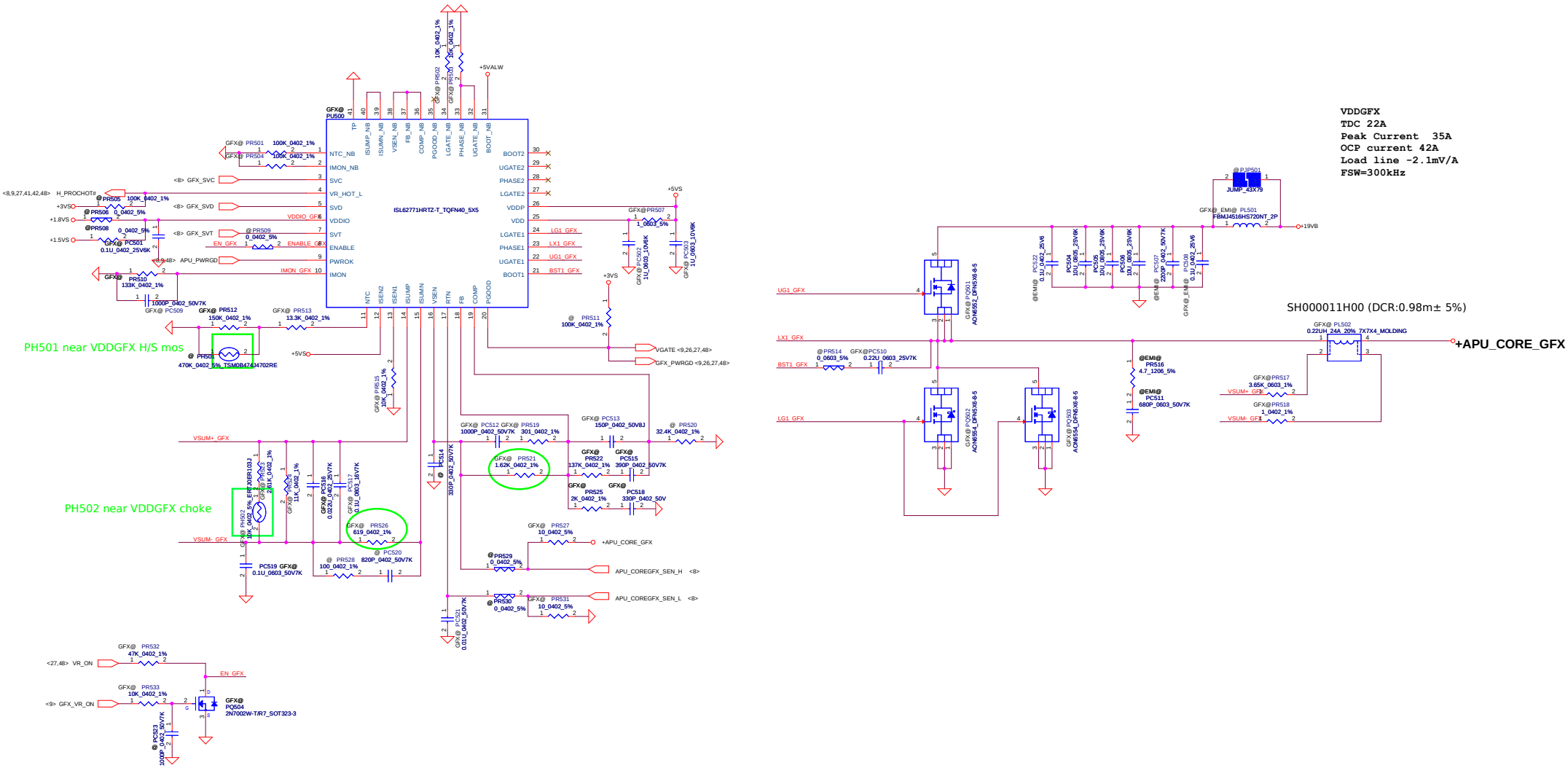
Size	Document Number	Rev
C	LA-C142P	1.0

Date: Friday, February 13, 2015 Sheet 47 of 56



Security Classification	Compal Secret Data		
Issued Date	2013/01/04	Deciphered Date	2015/01/04

Compal Electronics, Inc.	
Title	PWR_APU_CORE/APU_CORE_NB
Size: Custom	Document Number: LA-C142P
Rev	0.1
Date: Friday, February 13, 2015	Sheet 48 of 56



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Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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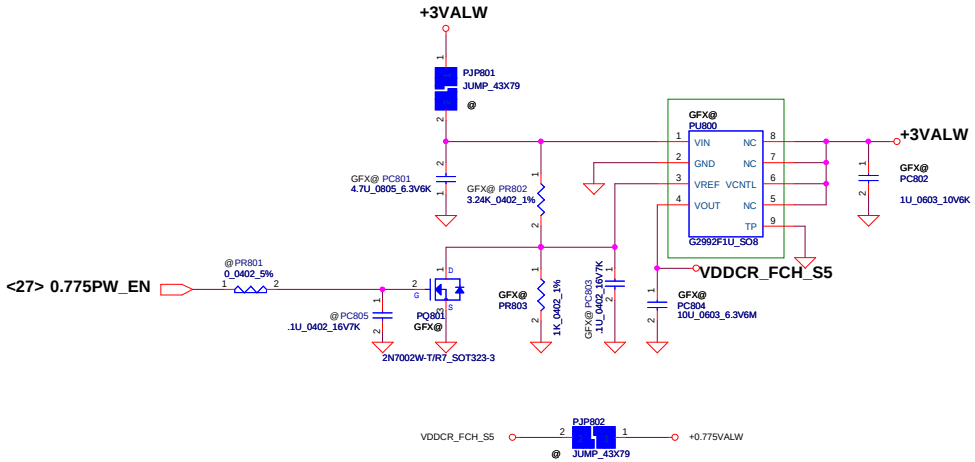
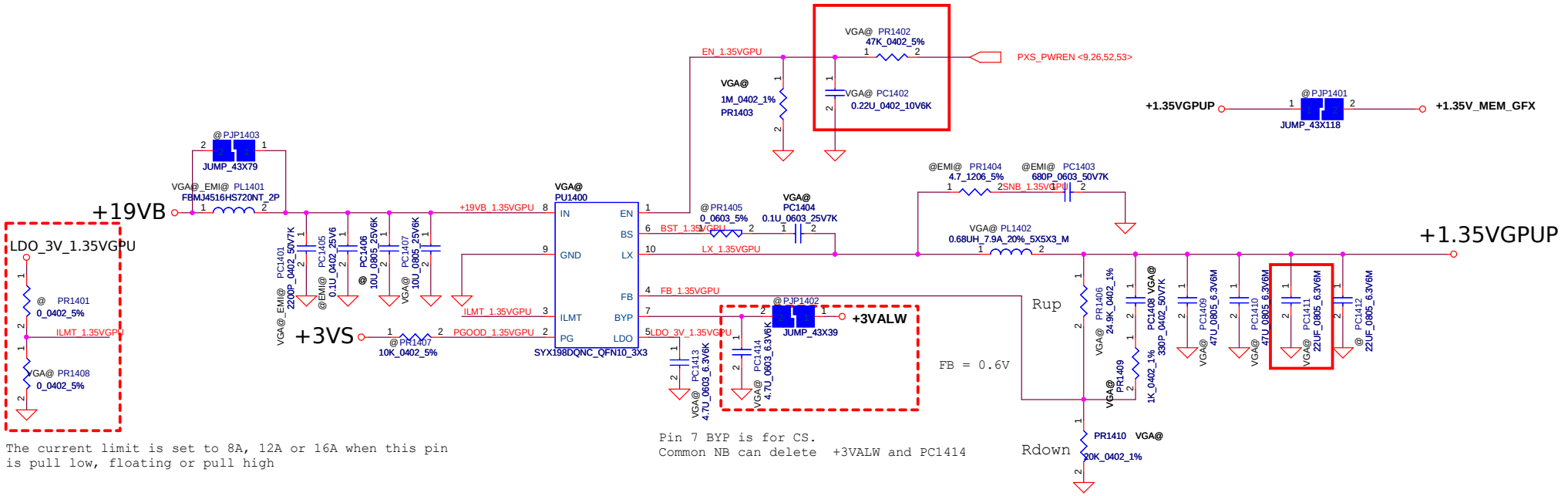
Compal Electronics, Inc.			
Title: PWR_VDDGFX			
Size: Custom	Document Number: LA-C142P		Rev: 0.1
Date: Friday, February 13, 2015	Sheet 49 of 56		



Security Classification	Compal Secret Data		
Issued Date	2014/03/31	Deciphered Date	2015/04/30

Compal Electronics, Inc.		
Title: PWR_1.5V/VDDCR_FCH_S5		
Size	Document Number: LA-C142P	Rev: 0.1
Date: Friday, February 13, 2015	Sheet 50 of 56	

EN pin don't floating
If have pull down resistor at HW side, pls delete PR1403



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

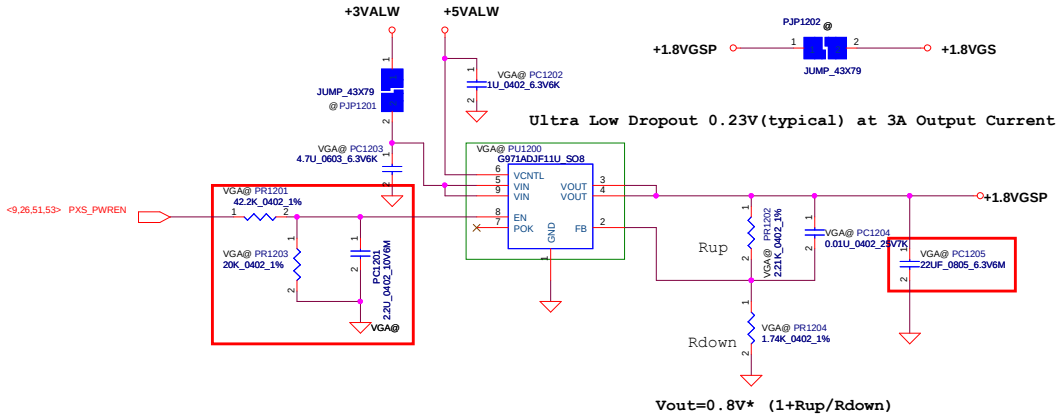
Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC1414

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=1.35V

+1.35VGPU
TDC 3.5A
Peak Current 5A
OCP current 8A

Security Classification	Compal Secret Data		
Issued Date	2014/03/31	Deciphered Date	2015/04/30

Compal Electronics, Inc.			
Title: PWR_+1.35VGPU			
Size	Document Number: LA-C142P		Rev: 0.1
Date: Friday, February 13, 2015	Sheet 51 of 56		

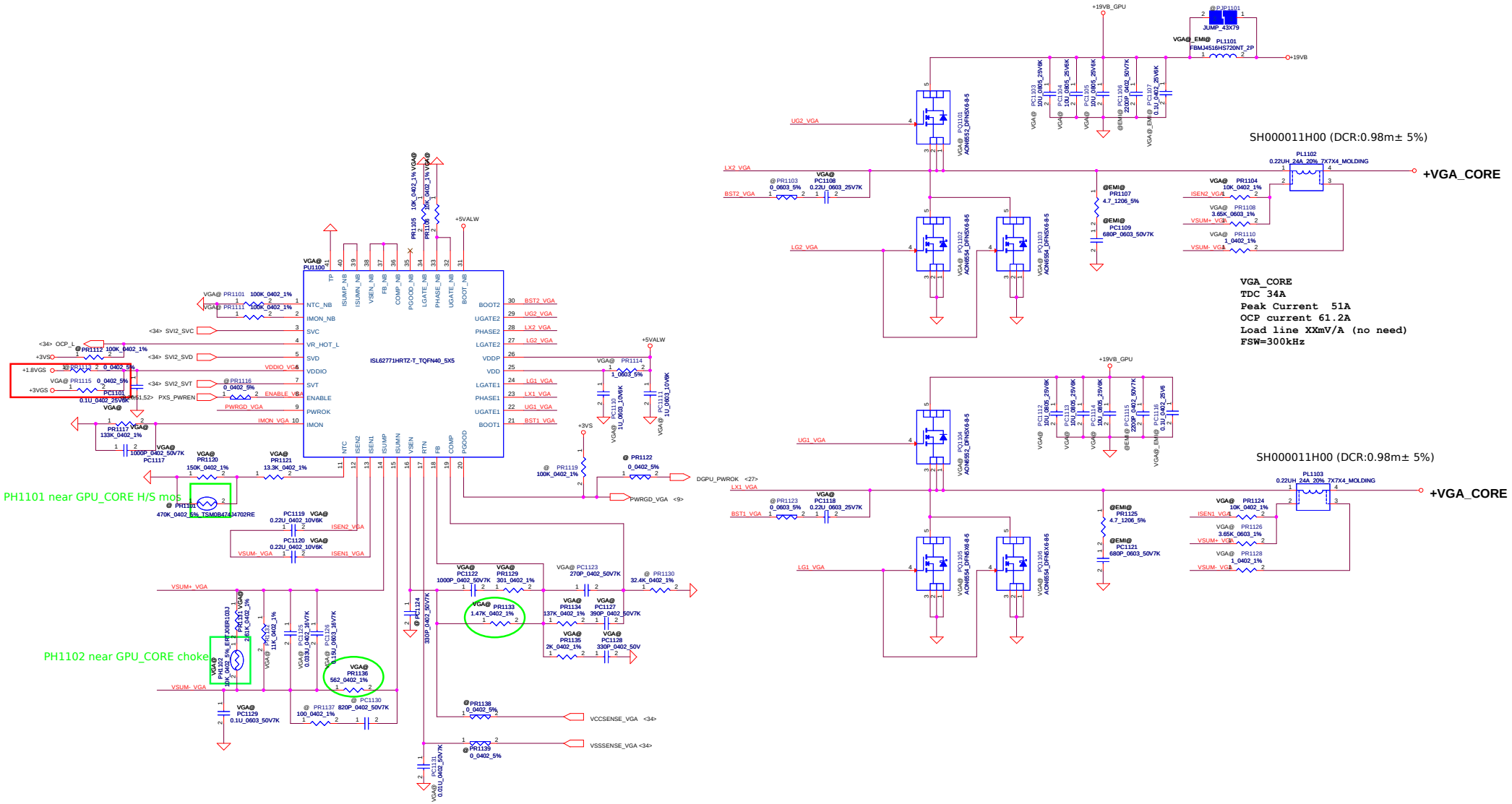


Compal Electronics, Inc.

Title: PWR_1.8VGS

Size | Document Number: LA-C142P | Rev: 0.1

Date: Friday, February 13, 2015 | Sheet 52 of 56



DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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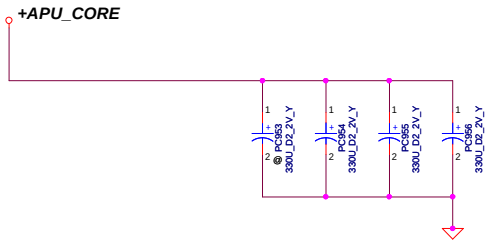
Compal Electronics, Inc.		
Title: PWR_VGA_CORE		
Size: Custom	Document Number: LA-C142P	Rev: 0.1
Date: Friday, February 13, 2015	Sheet 53 of 56	

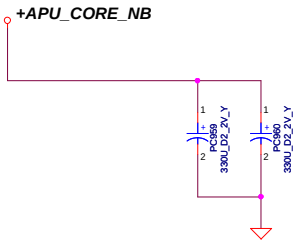
+APU_CORE

APU_CORE
330uF*3+1(reserve)



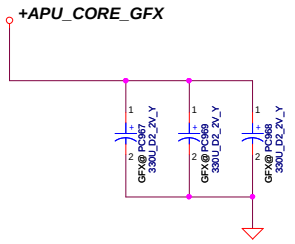
+APU_CORE_NB

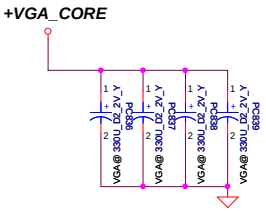
APU_CORE_NB
330uF*2



+VDDGFX

+VDDGFX
330uF*3





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Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

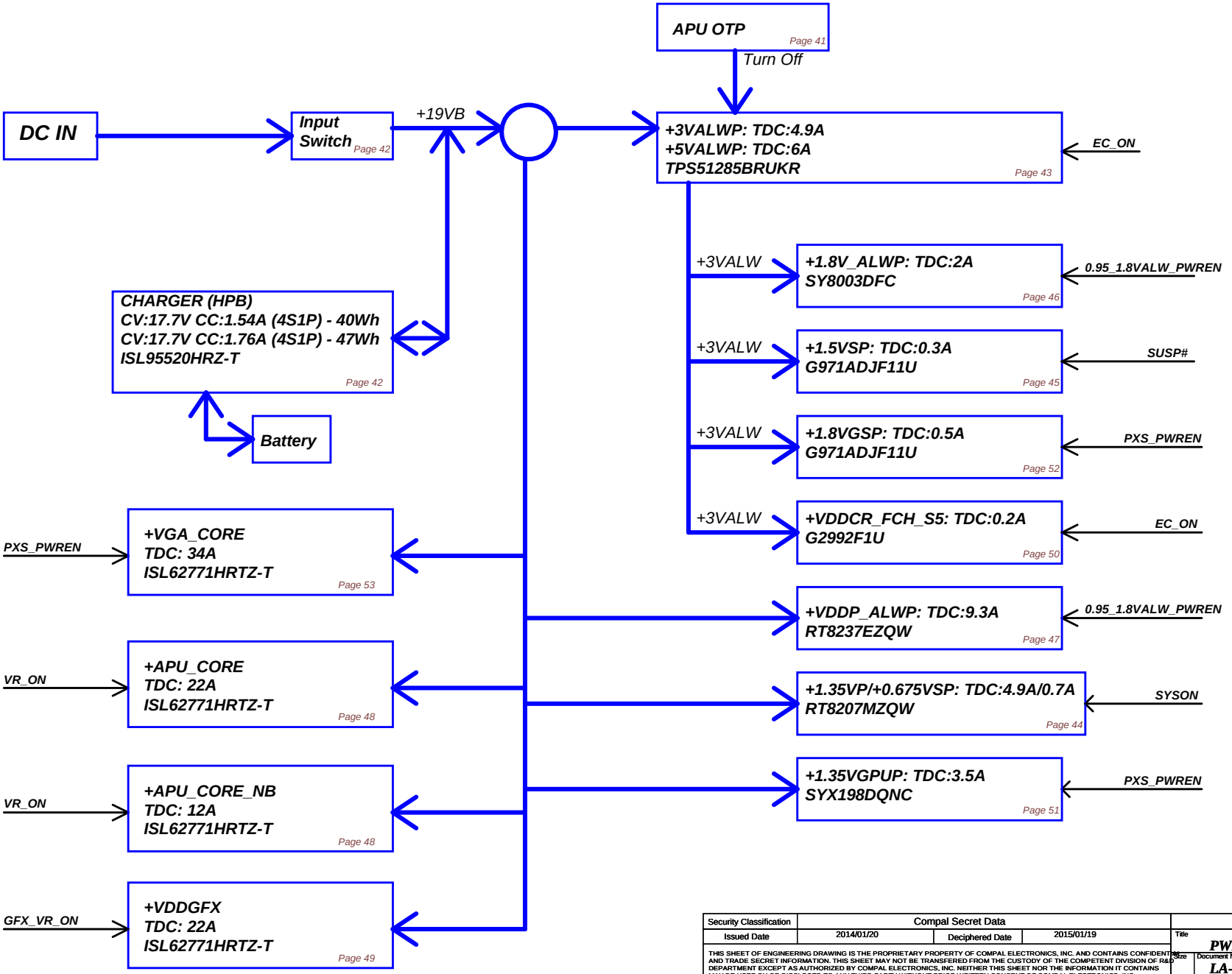
Compal Electronics, Inc.

Title: PWR_PROCESSOR DECOUPLING

Size | Document Number: LA-C142P | Rev: 0.1

Date: Friday, February 13, 2015 | Sheet 54 of 56

Power block



Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2015/01/19

Compal Electronics, Inc.			
Title	PWR_POWER BLOCK DIAGRAM		
Size	Document Number		Rev
	LA-C142P		1.0
Date:	Friday, February 13, 2015	Sheet	55 of 56

Version Change List (P . I. R . List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	45	+1.5VSP	14/12/04	Morris	design change	change PR401 from 47K to 42.2K change PR403 from 47K to 20K	0.2
2	52	1.8VGSP	14/12/04	Morris	revise sequence from EE requirement	change PR1201 from 47K to 42.2K change PR1203 from 47K to 20K add PC1201 2.2uF	0.2
3	51	+1.35VGPUP	14/12/04	Morris	revise sequence from EE requirement	change PR1402 from 0 to 47K	0.2
4	42	CHARGER	14/12/04	Morris	from EMI requirement	add PC765 0.1uF add PR766 4.7 add PC767 680P	0.2
5	43	+3.3VALWP/+5VALWP	14/12/04	Morris	from EMI requirement	change PR103 and PR111 from 0 to 2.2 change PL102 from SH00000Z200 to SM010009C80	0.2
6	42	CHARGER	14/12/04	Morris	improve S5 power consumption	delete PR780 add PQ710,PQ711,PR781	0.2
7	41	DCIN/BATT CONN/OTP	14/12/04	Morris	improve PWC function	change PQ4 from SB000009Q80 to SB00000PV00 change PR23 from 150K to 100K change PR26 from 499K to 887K change PR27 from 392K to 383K add PR38 187K	0.2
8	41	DCIN/BATT CONN/OTP	15/01/14	Morris	adjust OTP setting point from thermal requirement	change PR24 from 14K to 17.8K only for CZL	0.3
9	41	DCIN/BATT CONN/OTP	15/01/14	Morris	from ESD requirement	change PR15 from 100 to 200	1.0

Compal Electronics, Inc.

Title: PWR-PIR

Size | Document Number: LA-C142P | Rev: 1.0

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