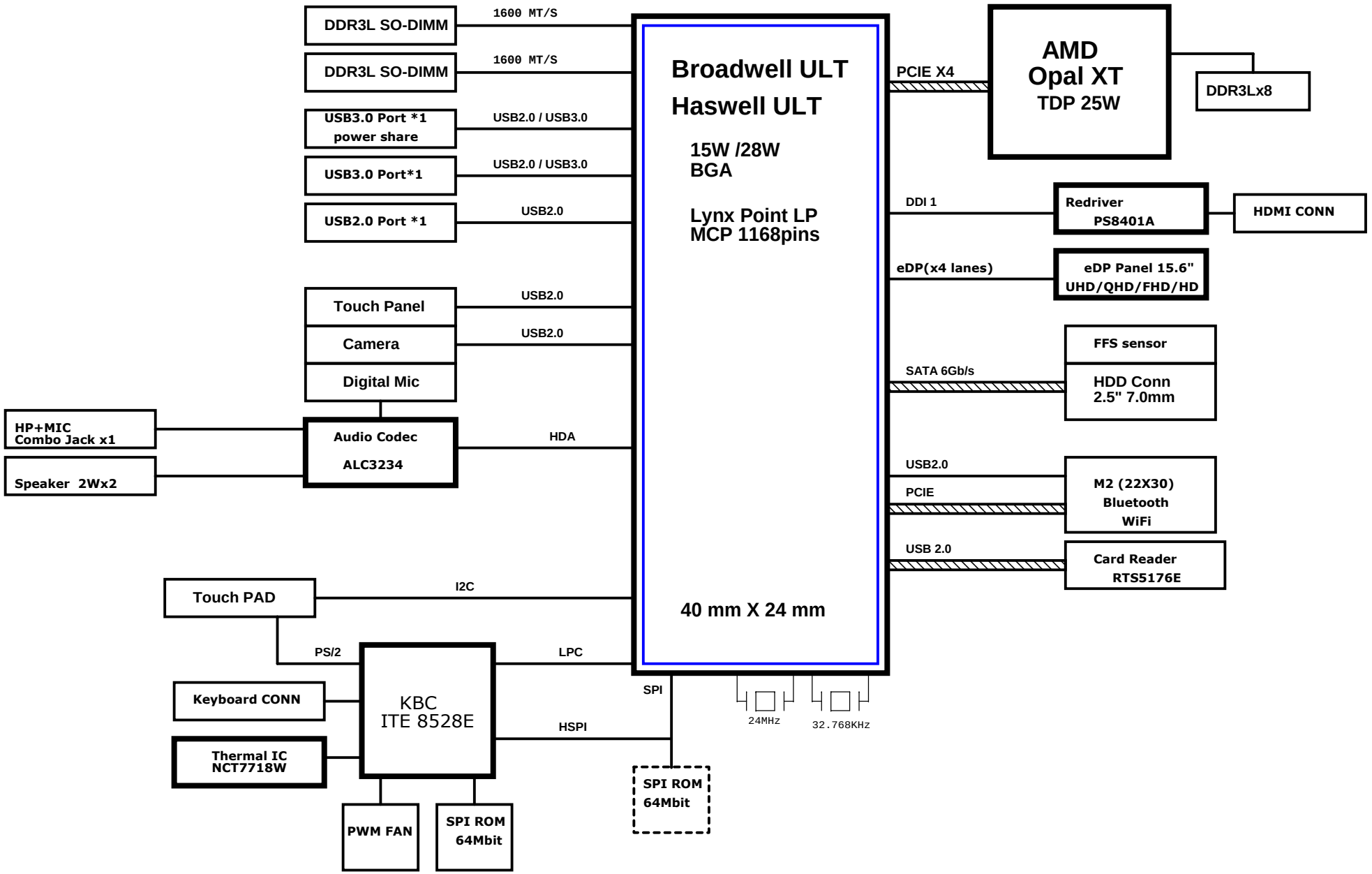
AM6 BLOCK DIAGRAM



Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	Block Diagram	A

Date: Monday, May 05, 2014 Sheet 1 of 58

HSIO Port	USB3.0	PCIE	SATA
1	USB3.0_1 Left Power Share		
2	USB3.0_2 Right		
3	USB3.0_3 X	PCIE1 X	
4	USB3.0_4 X	PCIE2 X	
5		PCIE3 X	
6		PCIE4 WIFI	
7		PCIE5 GPU 4X	
8		PCIE5 GPU 4X	
9		PCIE5 GPU 4X	
10		PCIE5 GPU 4X	
11		PCIE6 X	SATA3 X
12		PCIE6 X	SATA2 X
13		PCIE6 X	SATA1 HDD
14		PCIE6 X	SATA0 X

PCIE CLK
CLK0 X
CLK1 X
CLK2 X
CLK3 WIFI
CLK4 GPU 4X
CLK5 X

USB2.0
USB2.0_0 Left Power Share
USB2.0_1 Right /w 3.0
USB2.0_2 Right
USB2.0_3 Card Reader
USB2.0_4 Camera
USB2.0_5 eTP
USB2.0_6 Blue Tooth
USB2.0_7 X

Quanta Computer Inc.
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Size	Document Number	Rev
	PORT ASSIGNMENT	A

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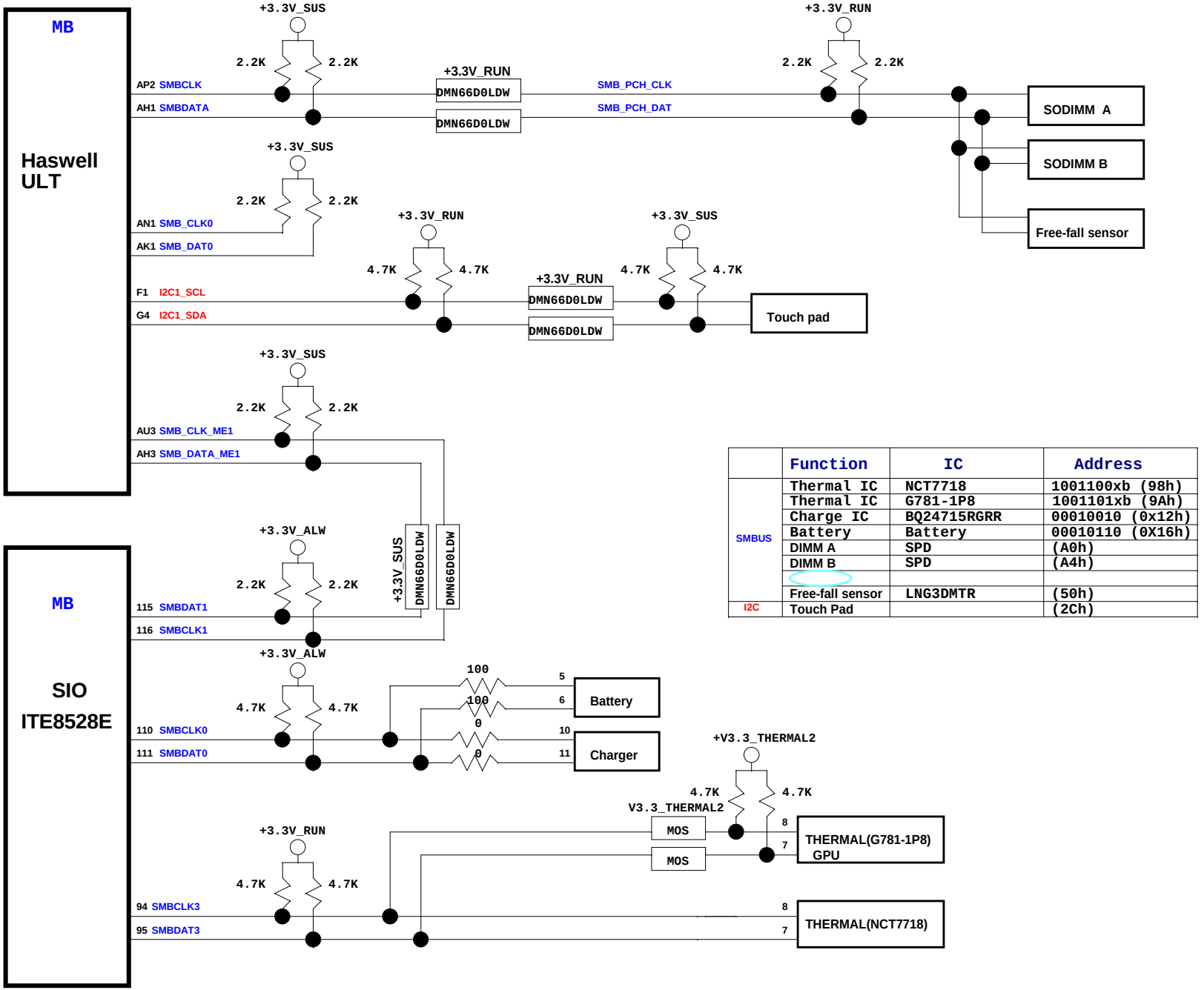

	Function	IC	Address
SMBUS	Thermal IC	NCT7718	1001100xb (98h)
	Thermal IC	G781-1P8	1001101xb (9Ah)
	Charge IC	BQ24715RGRR	00010010 (0x12h)
	Battery	Battery	00010110 (0X16h)
	DIMM A	SPD	(A0h)
	DIMM B	SPD	(A4h)
	Free-fall sensor	LNG3DMTR	(50h)
I2C	Touch Pad		(2Ch)

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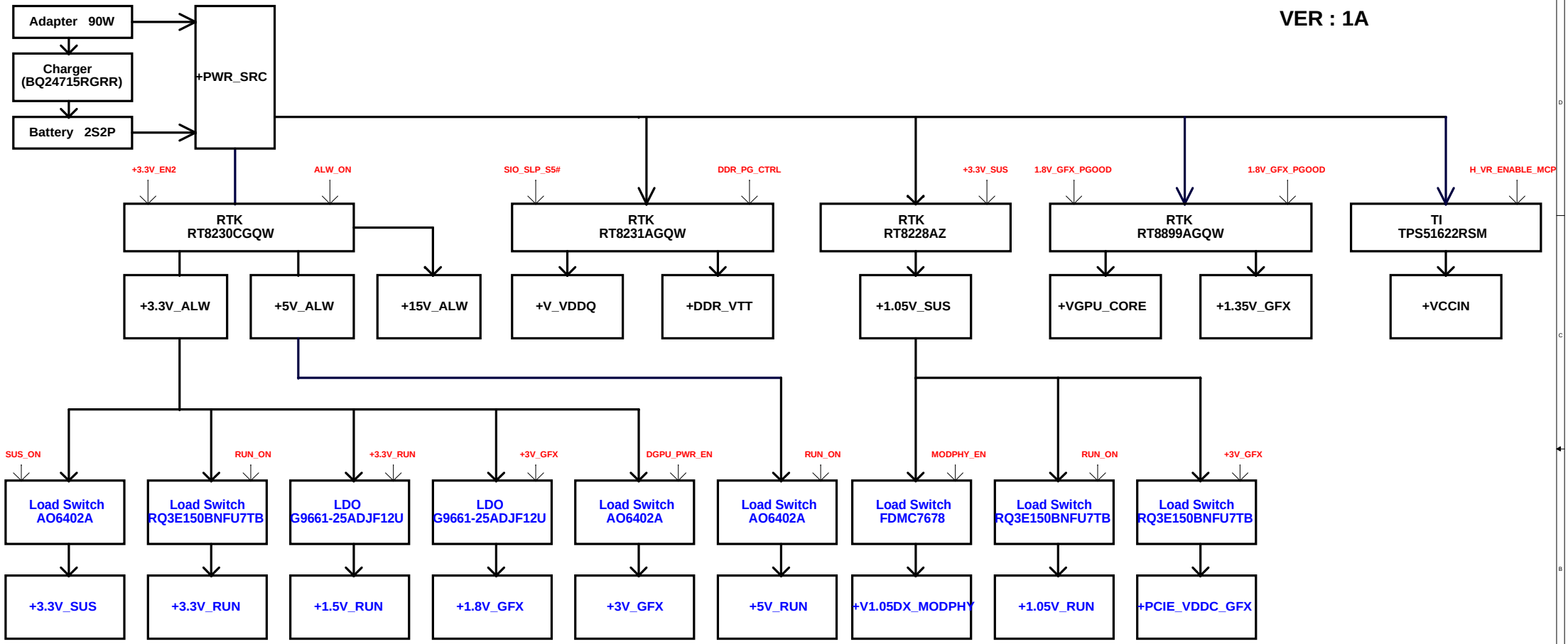
Size | Document Number: SMBUS | Rev A
Date: Monday, May 05, 2014 | Sheet 3 of 58

VER : 1A



Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	Power Block Diagram	A

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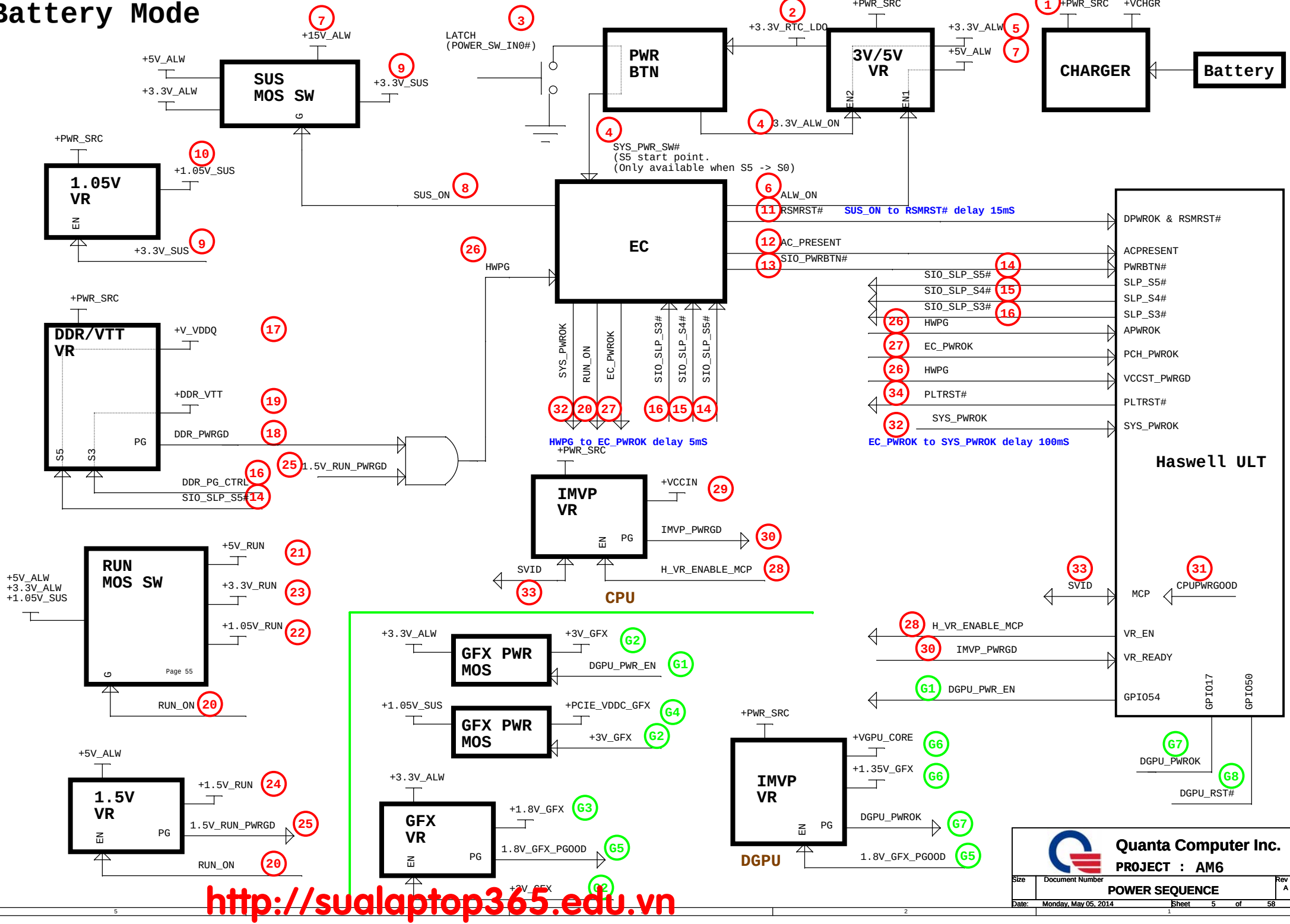
Battery Mode



Quanta Computer Inc.
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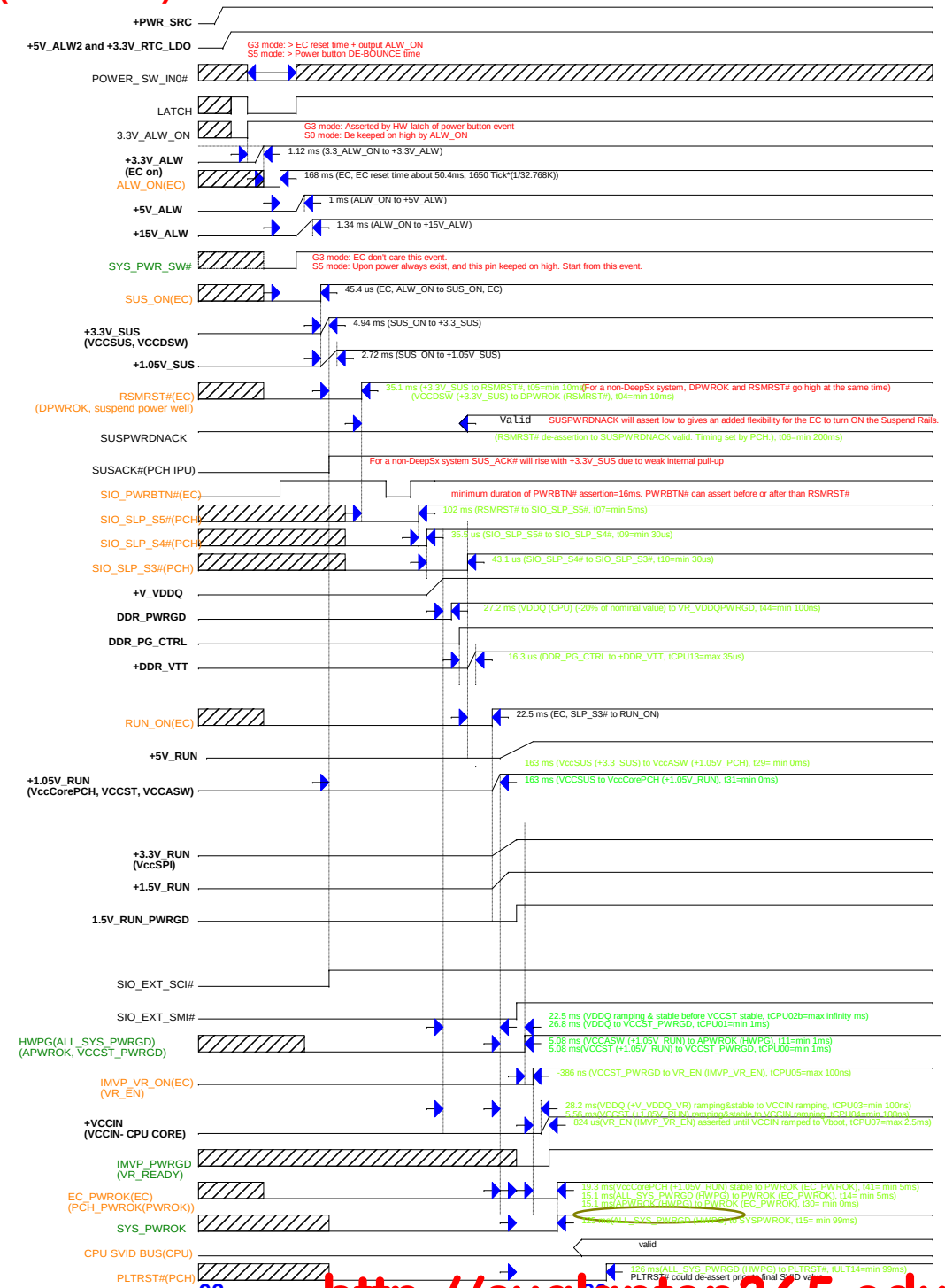
Size	Document Number	Rev
	POWER SEQUENCE	A
Date: Monday, May 05, 2014	Sheet 5 of 58	

Power Sequence (G3 to S0)

Shark Bay ULT PSS, 490828, Rev1.1



Quanta Computer Inc.	PROJECT : AM6	
Size	Document Number	Rev A
	G3 to S0	
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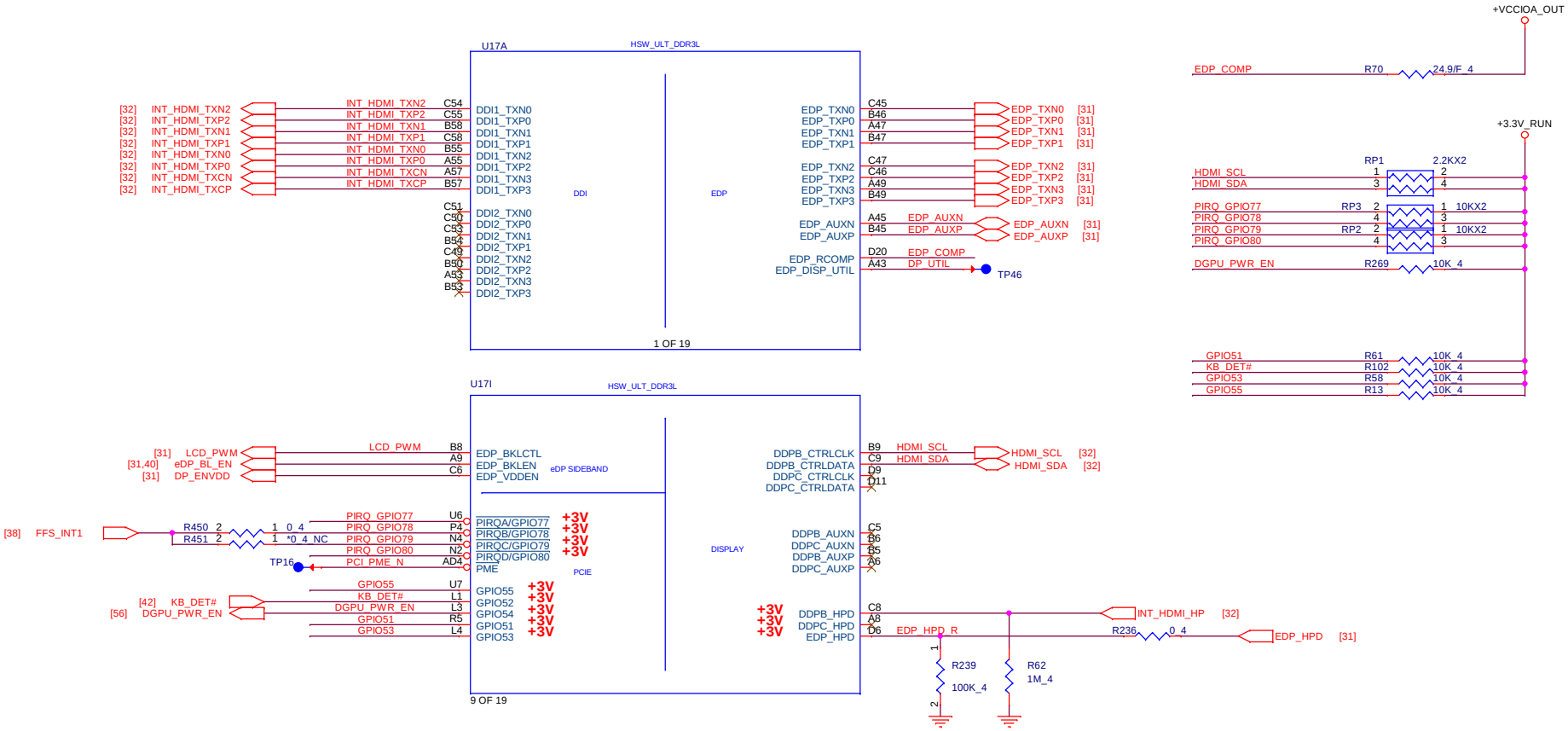
Haswell ULT (DISPLAY)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
DDPB_CTRLDATA	Port B Detected	PCH_PWROK	0 = Port B is not detected. 1 = Port B is detected.	This signal has a weak internal pull-down. IPD 20K is disabled when PLTRST# is de-asserted. PU 2.2K to +3.3V_RUN
DDPC_CTRLDATA	Port C Detected	PCH_PWROK	0 = Port C is not detected. 1 = Port C is detected.	This signal has a weak internal pull-down. IPD 20K is disabled when PLTRST# is de-asserted. NC

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	Haswell ULT 1/12	A

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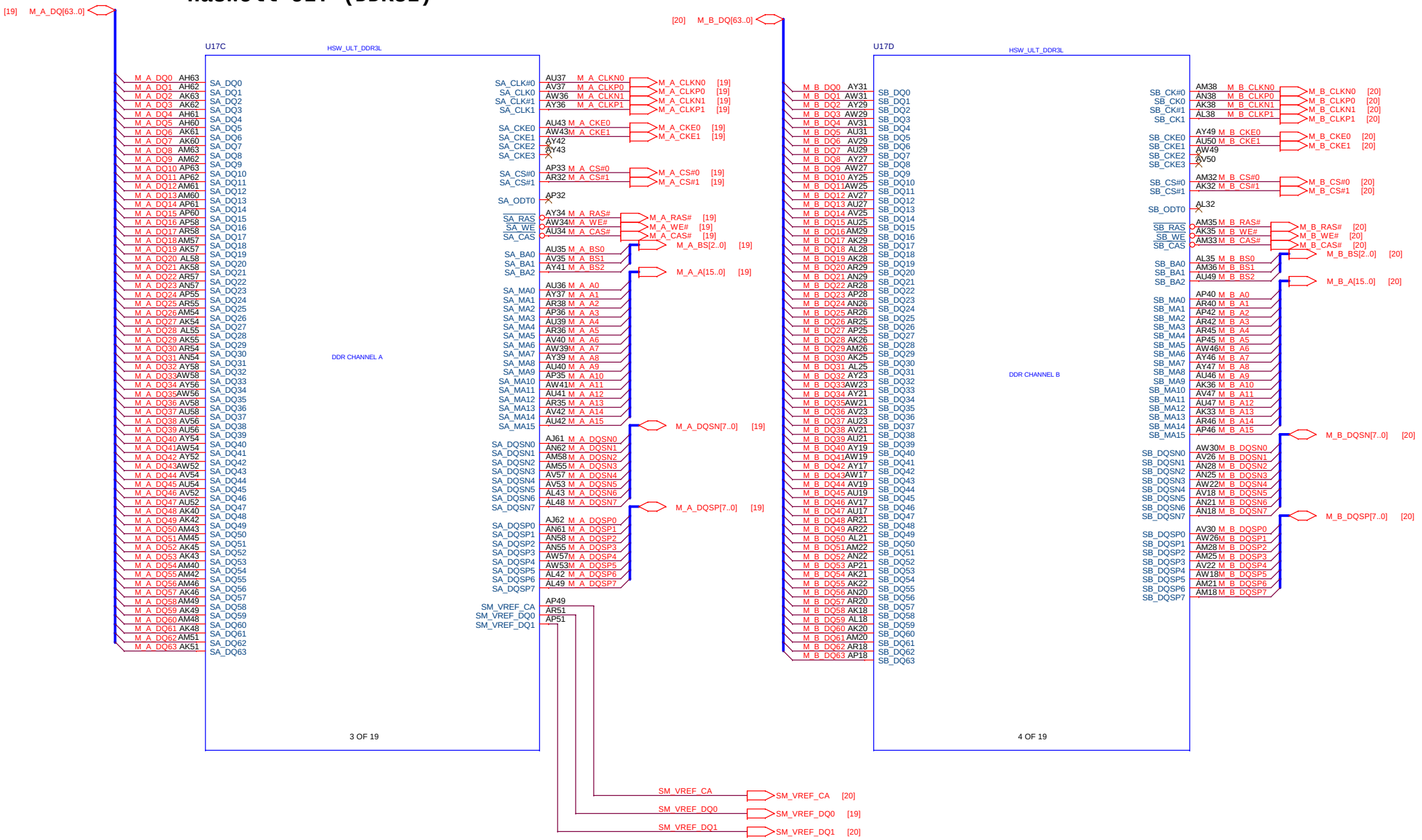
Haswell ULT (DDR3L)



Quanta Computer Inc.

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Size	Document Number	Rev
	Haswell ULT 2/12	A

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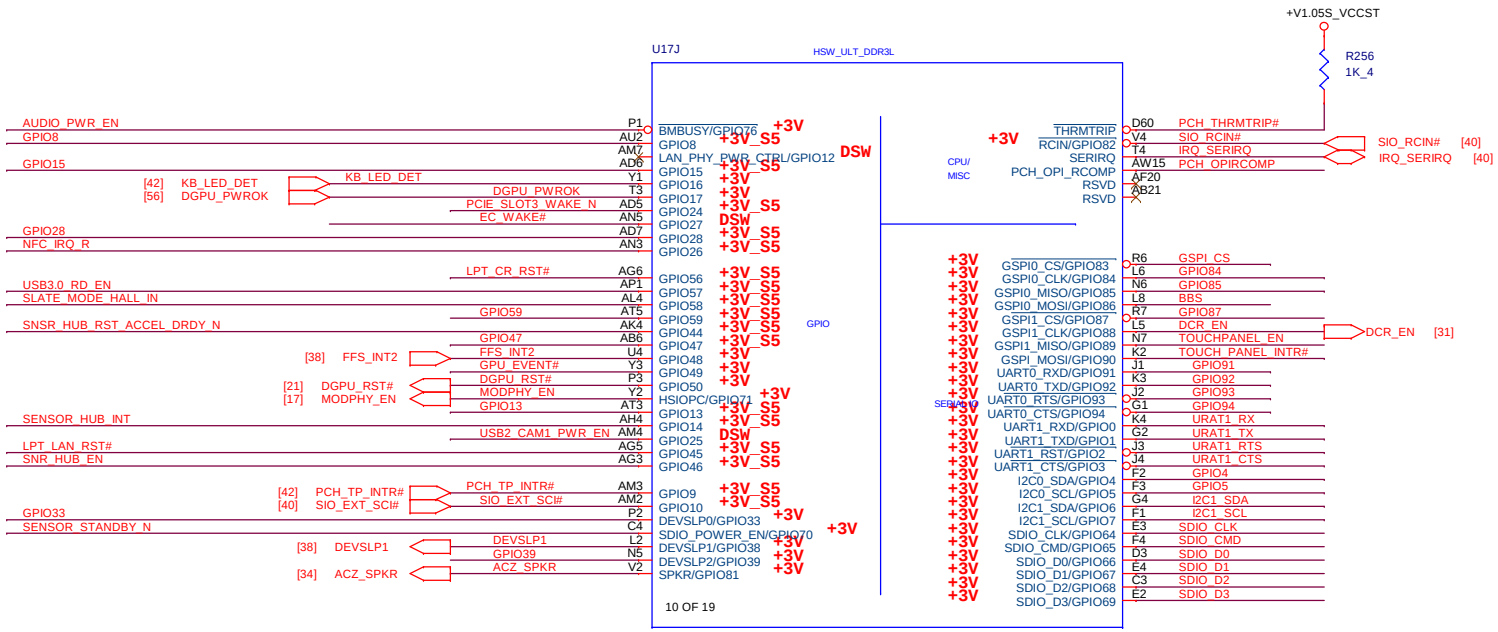
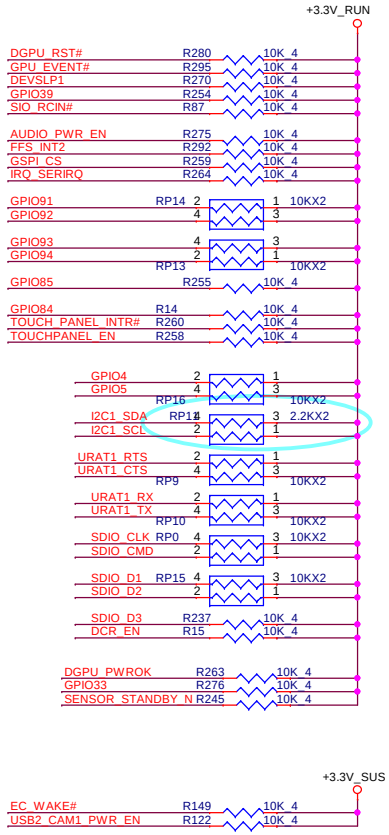
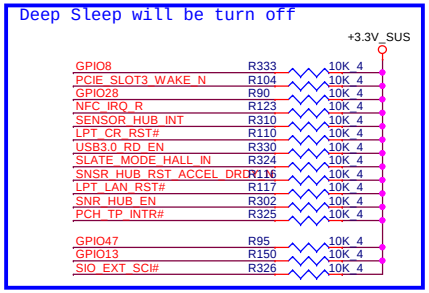
Hasswell ULT(GPIO,LPIO,MISC)

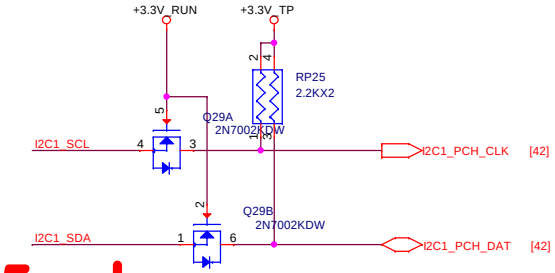


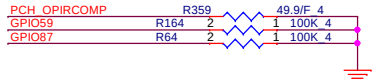


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
GPIO15	TLS Confidentiality	RSMRST#	0 = Disable 1 = Enable	This signal has a weak internal pull-down.
SPKR/GPIO81	No Reboot mode	PCH_PWROK	0 = Disable 1 = Enable	This signal has a weak internal pull-down. NA
GSPI0_MOSI/GPIO86	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = SPI 1 = LPC	This signal has a weak internal pull-down.
SDIO_D0/GPIO66	Top Swap Override	PCH_PWROK	0 = Disable 1 = Enable	This signal has a weak internal pull-down.







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	Haswell ULT 3/12	A

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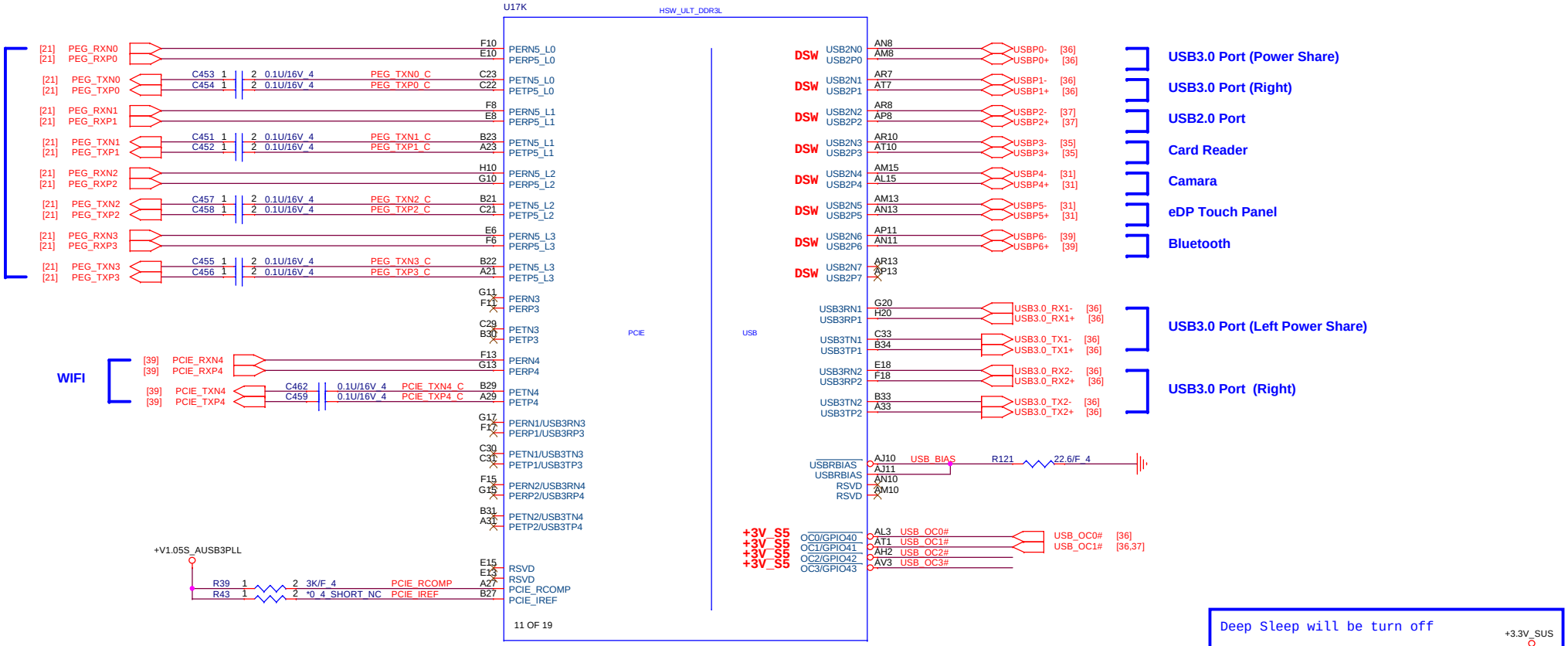
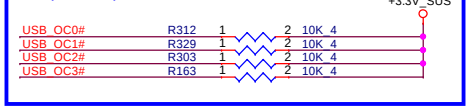
Haswell ULT (PCIE,USB)



Deep Sleep will be turn off



Overcurrent Pin Setting

Pin	Default Port Mapping	AM6 setting
OC0#	Port 0, Port 1	Port 0
OC1#	Port 2, Port 3	Port 1, Port 2
OC2#	Port 4, Port 5	no use
OC3#	Port 6, Port 7	no use

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	Haswell ULT 4/12	A

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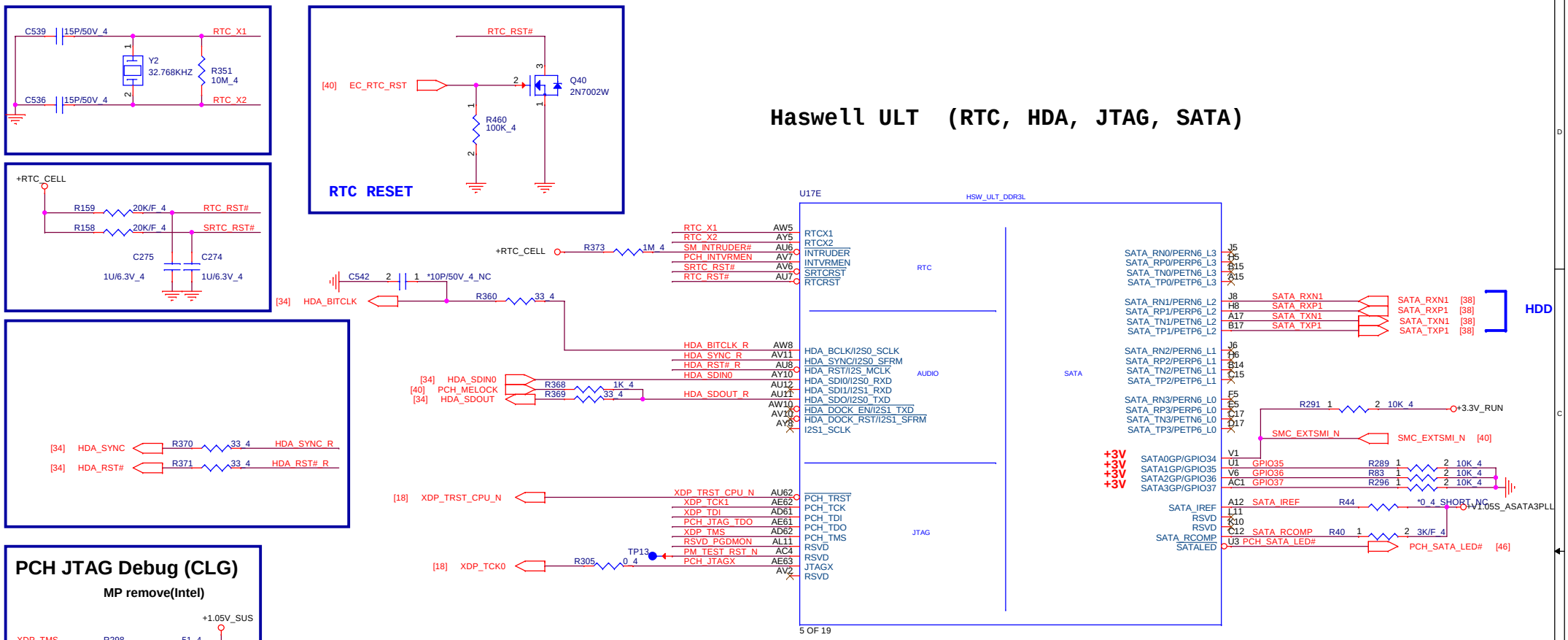
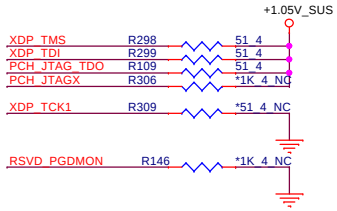
Haswell ULT (RTC, HDA, JTAG, SATA)



PCH JTAG Debug (CLG)

MP remove(Intel)



DFXTESTMODE
HIGH - DFXTESTMODE DISABLED(DEFAULT)
LOW - DFXTESTMODE ENABLED

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = Security Effect (Int PD) 1 = Can be Override	This signal has a weak internal pull-down. The internal pull-down is disabled after PLTRST# deasserts
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Integrated VRMs disabled. 1 = Integrated VRMs enabled.	+RTC_CELL R157 *330K_4_NC PCH_INTVRMEN R147 330K_4 **An external resistor is required**

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	Haswell ULT 5/12	A

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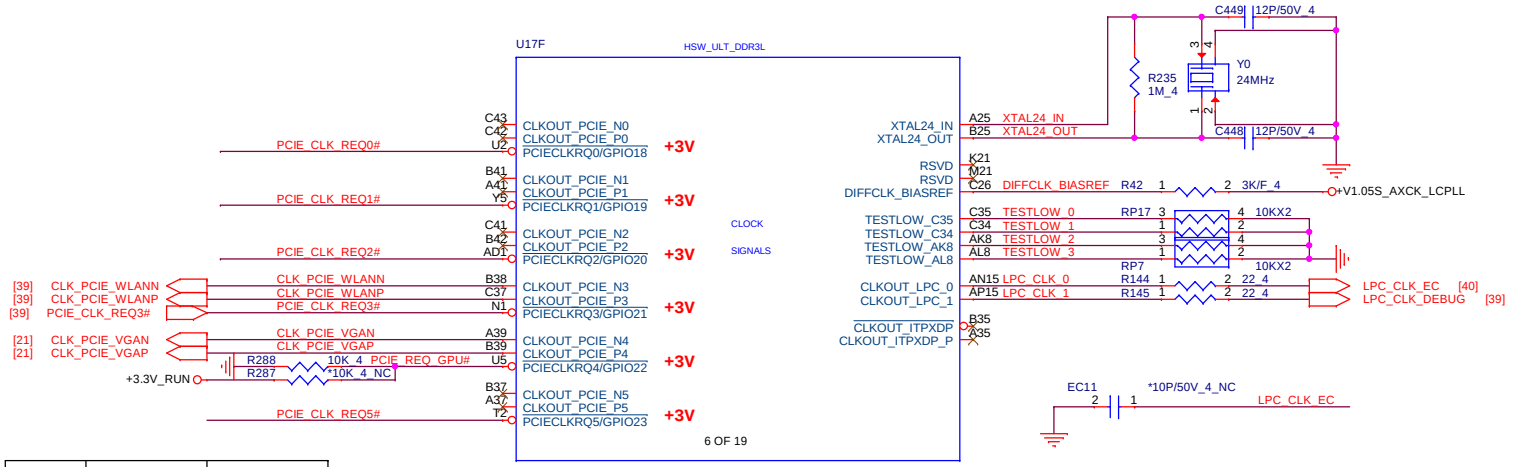
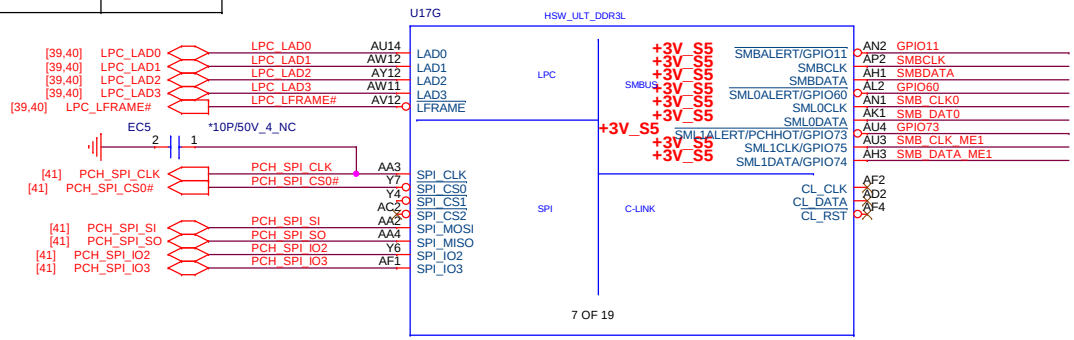
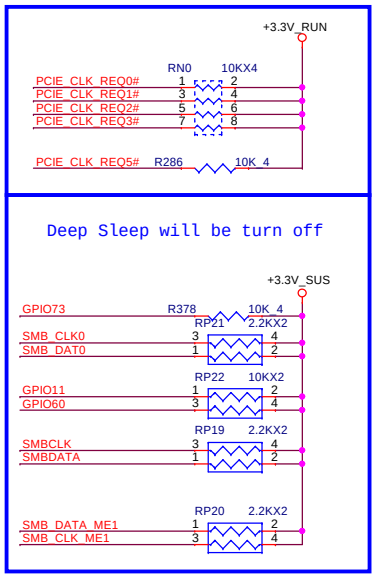
Haswell ULT (CLK)

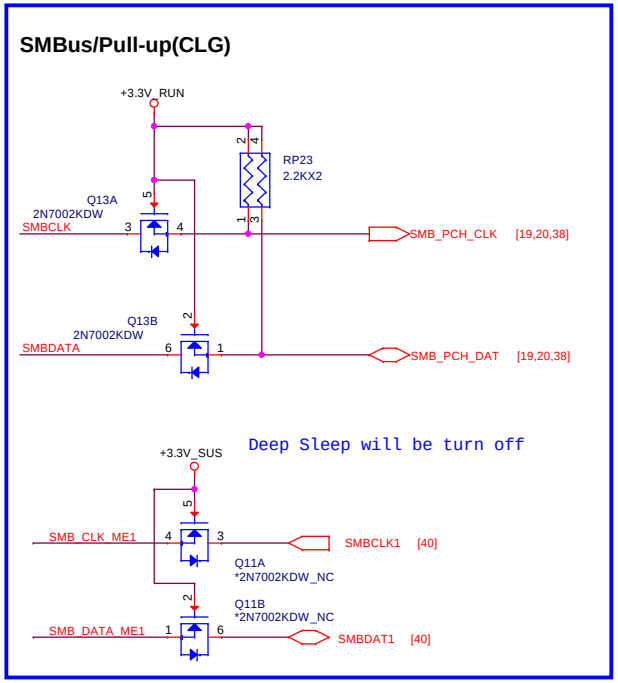


	UMA	Discrete
R288	*10K_4_NC	10K_4
R287	10K_4	*10K_4_NC

Haswell ULT (LPC/SPI/SMB/CLINK)







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	Haswell ULT 6/12	A

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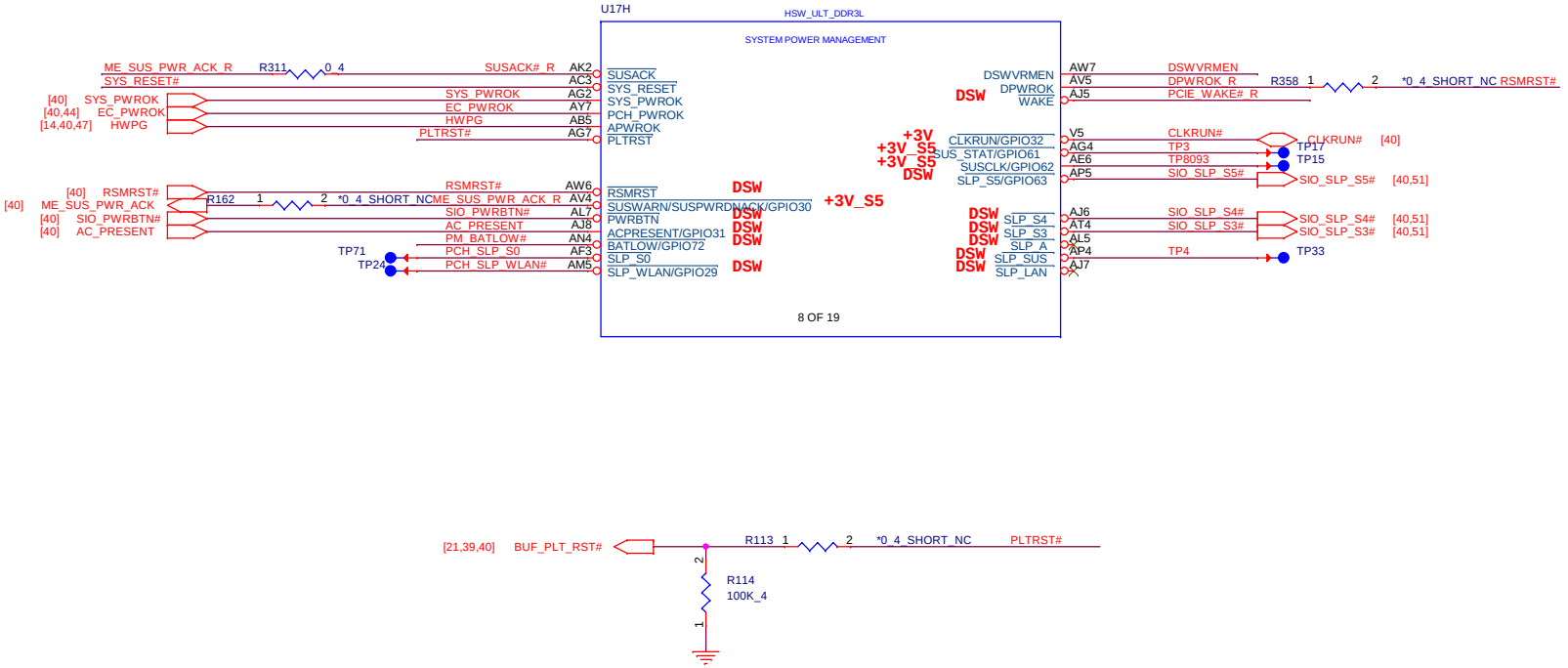
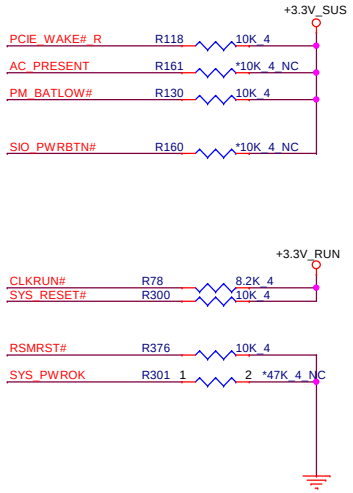
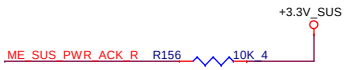
Haswell ULT (SYSTEM POWER MANAGEMENT)



PCH Pull-high/low(CLG)



Deep Sleep will be turn off



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
DSWVRMEN	DeepSx Well On-Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	1. This signal is always sampled. 2. This signal is in the RTC well.

+RTC_CELL 330K_4 R372 DSWVRMEN

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Haswell ULT MCP(POWER)

CPU VDDQ

Haswell ULT 15W & 28W: 1.4A

6X10UF MLCC
4X2.2UF MLCC

+V_VDDQ
C284 10U/4V_6
C283 10U/4V_6
C279 10U/4V_6
C278 10U/4V_6
C286 10U/4V_6
C280 10U/4V_6
C270 1U/6.3V_4
C273 1U/6.3V_4
C271 0.1U/16V_4
C272 0.1U/16V_4

+V1.05S_VCCST
R243 10K_4
[13,40,47] HWPG
SDM10K45-7-F 1 2 D2
VCCST_PWRGD

+VCCIOA_OUT
VCOMP_OUT(+VCCIOA_OUT) only be used to connect eDP_RCOMP.

[54] H_VR_ENABLE_MCP
R242 1 2 10K_4
H_VR_ENABLE_MCP

[54] IMVP_PWRGD
IMVP_PWRGD

C464 0.1U/16_4

+V1.05S_VCCST
R6 *10K_4_NC IMVP_PWRGD

+V1.05S_VCCST
R94 1 2 *0_8_SHORT_NC
+1.05V_RUN

U17L HSW_ULT_DDR3L

L59	RSVD	
J58	RSVD	
AH26	VDDQ	
AJ31	VDDQ	
AJ33	VDDQ	
AJ37	VDDQ	
AN33	VDDQ	1.4A
AP43	VDDQ	
AR48	VDDQ	
AY35	VDDQ	
AY40	VDDQ	
AY44	VDDQ	
AY50	VDDQ	
F59	VCC	
N58	RSVD	
AC58	RSVD	
E63	VCC_SENSE	VCCSENSE
AB23	RSVD	
A59	VCCIO_OUT	+VCCIO_OUT
E20	VCCIOA_OUT	VCOMP_OUT
AD23	RSVD	
AA23	RSVD	
AE58	RSVD	
L62	VIDALERT	H_CPU_SVIDALRT#
N63	VIDSCLK	VR_SVID_CLK
L63	VIDSOUT	VR_SVID_DATA
B59	VCCST_PWRGD	
F60	VR_EN	H_VR_ENABLE_MCP
C59	VR_READY	IMVP_PWRGD
D63	VSS	
H59	PWR_DEBUG	FIVR_EN_BUF
P62	VSS	
P60	RSVD_TP	MCP_RSVD_69
P61	RSVD_TP	MCP_RSVD_70
N59	RSVD_TP	MCP_RSVD_71
N61	RSVD_TP	MCP_RSVD_72
T59	RSVD	
AD60	RSVD	
AD59	RSVD	
AA59	RSVD	
AE60	RSVD	
AC59	RSVD	
AG58	RSVD	
U58	RSVD	
V59	RSVD	
AC22	VCCST	
AE22	VCCST	
AE23	VCCST	
AB57	VCC	
AD57	VCC	
AG57	VCC	
C24	VCC	
C28	VCC	
C32	VCC	

HSW ULT POWER

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CPU VCC

Haswell ULT 15W : 32A
28W : 40A

24 X 10UF(0603 MLCC)

+VCCIN
C210 10U/4V_6
C199 10U/4V_6
C181 10U/4V_6
C182 10U/4V_6
C219 10U/4V_6
C214 10U/4V_6
C168 10U/4V_6
C201 10U/4V_6
C169 10U/4V_6
C170 10U/4V_6
C185 10U/4V_6
C200 10U/4V_6
C166 10U/4V_6
C167 10U/4V_6
C203 10U/4V_6
C183 10U/4V_6
C202 10U/4V_6
C226 10U/4V_6
C186 10U/4V_6
C209 10U/4V_6
C213 10U/4V_6
C204 10U/4V_6
C171 10U/4V_6
C184 10U/4V_6

C36	VCC	
C40	VCC	
C44	VCC	
C48	VCC	
C52	VCC	
C56	VCC	
E23	VCC	
E25	VCC	
E27	VCC	
E29	VCC	
E31	VCC	
E33	VCC	
E35	VCC	
E37	VCC	
E39	VCC	
E41	VCC	
E43	VCC	
E45	VCC	
E47	VCC	
E49	VCC	
E51	VCC	
E53	VCC	
E55	VCC	
E57	VCC	
F24	VCC	
F28	VCC	
F32	VCC	
F36	VCC	
F40	VCC	
F44	VCC	
F48	VCC	
F52	VCC	
F56	VCC	
G23	VCC	
G25	VCC	
G27	VCC	
G29	VCC	
G31	VCC	
G33	VCC	
G35	VCC	
G37	VCC	
G39	VCC	
G41	VCC	
G43	VCC	
G45	VCC	
G47	VCC	
G49	VCC	
G51	VCC	
G53	VCC	
G55	VCC	
G57	VCC	
H23	VCC	
J23	VCC	
K23	VCC	
K57	VCC	
L22	VCC	
M23	VCC	
M57	VCC	
P57	VCC	
U57	VCC	
W57	VCC	

C218 1 2 100P/50V_4
C224 1 2 100P/50V_4
C229 1 2 100P/50V_4
C162 1 2 100P/50V_4

R262 100/F_4 +VCCIN
VCCSENSE VCCSENSE [54]
FIVR_EN_BUF R77 150_6 +V1.05S_VCCST

+V1.05S_VCCST

SVID ALERT

+V1.05S_VCCST
CLOSE TO CPU
R283 75_4
C485 0.1U/16V_4
H_CPU_SVIDALRT# R285 43_4 VR_SVID_ALERT# [54]

SVID DATA

+V1.05S_VCCST
CLOSE TO CPU
R284 130_4
C488 0.1U/16V_4
+V1.05S_VCCST
CLOSE TO VR
R7 130_4
C47 0.1U/16V_4
VR_SVID_DATA VR_SVID_DATA [54]

SVID CLK

+V1.05S_VCCST
CLOSE TO VR
R8 54.9/F_4
C49 0.1U/16V_4
VR_SVID_CLK VR_SVID_CLK [54]

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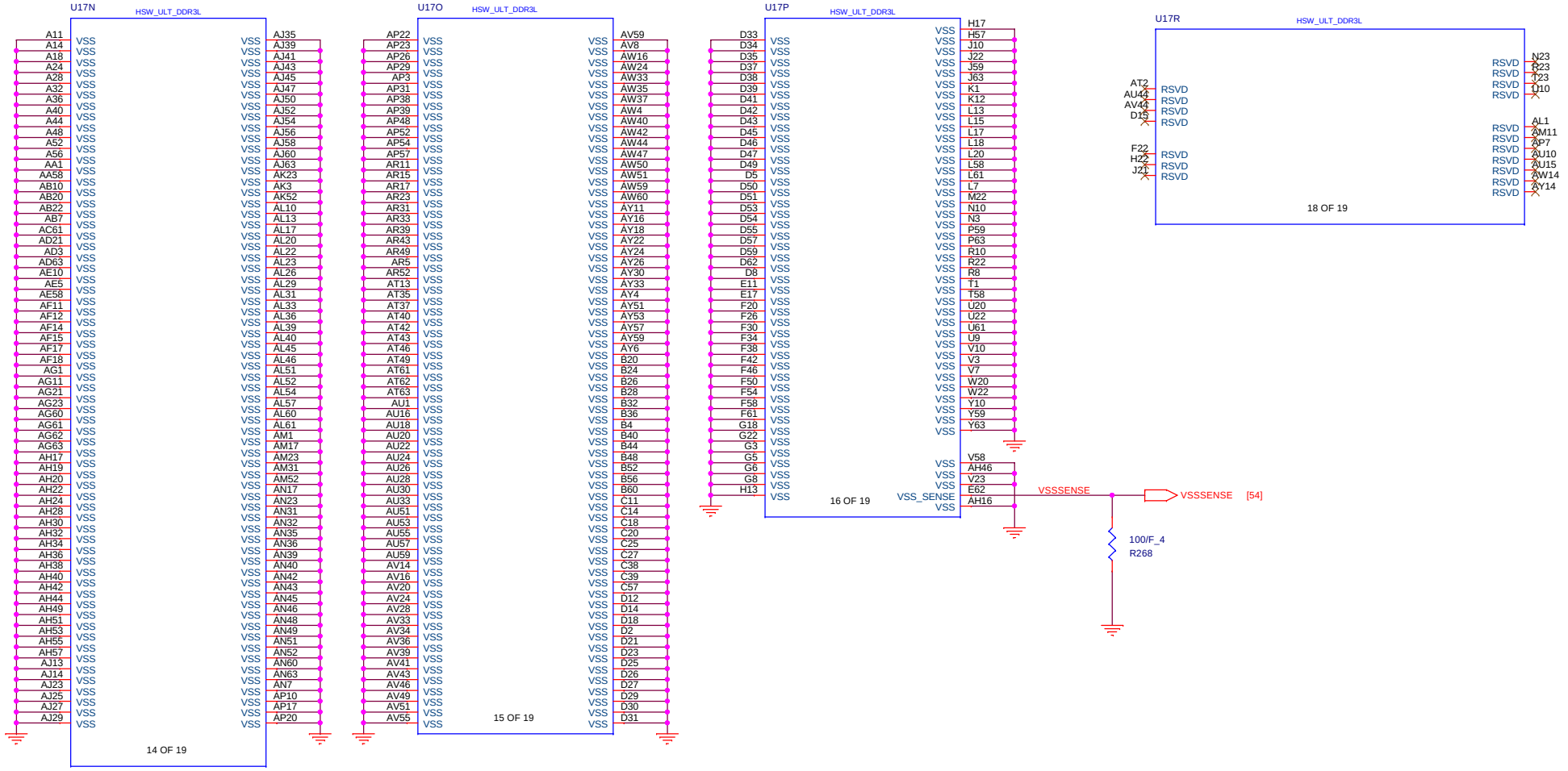
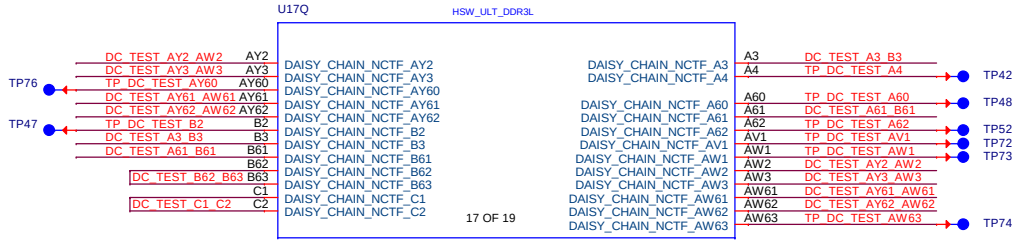
Haswell ULT (GND)





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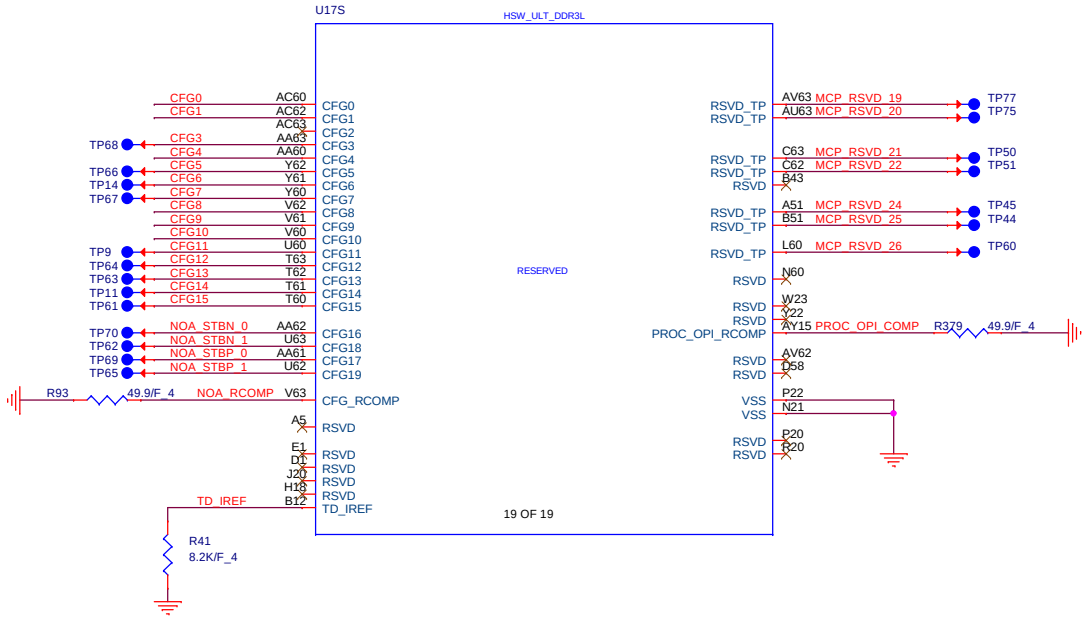

Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	
CFG0 Reserved	(DEFAULT) NORMAL OPERATION		CFG0 R108 *1K_4_NC
CFG1 Reserved	(DEFAULT) NORMAL OPERATION		CFG1 R297 *1K_4_NC
CFG2 Reserved	(DEFAULT) NORMAL OPERATION		
CFG3 MSR Privacy Bit Feature	Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting	IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden	CFG3 R293 *1K_4_NC
CFG4 eDP enable	Disabled	Enabled	CFG4 R107 1K_4
CFG[19:5] Reserved	(DEFAULT) NORMAL OPERATION		CFG8 R92 *1K_4_NC
			CFG9 R294 *1K_4_NC
			CFG10 R100 *1K_4_NC

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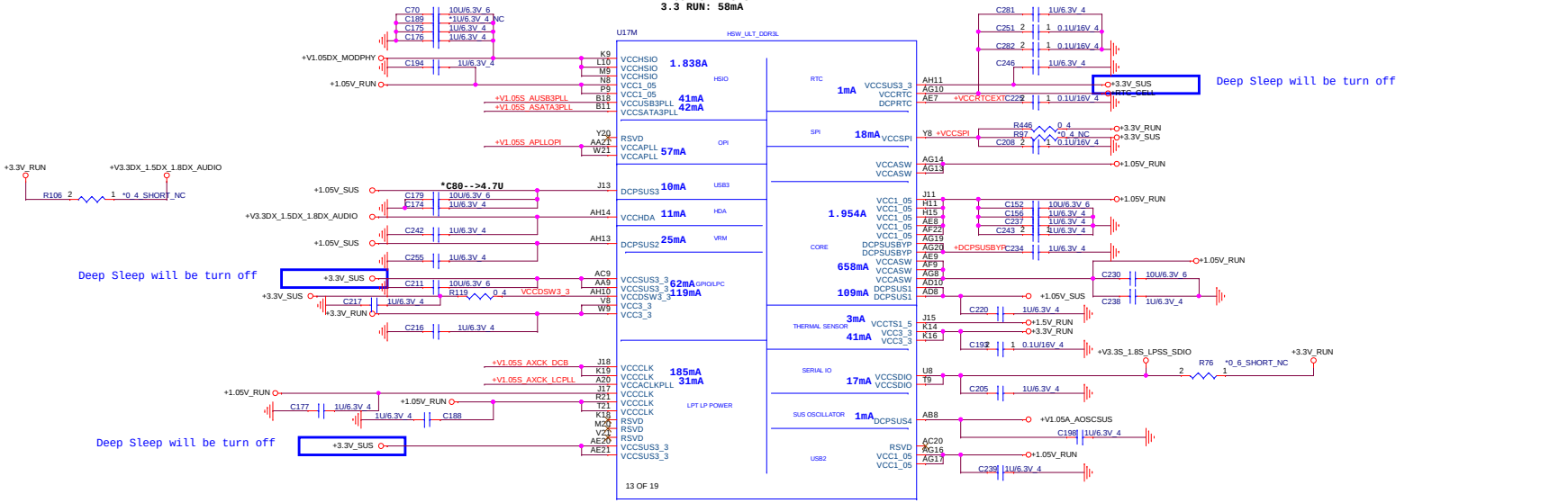
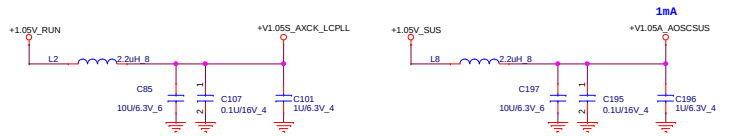
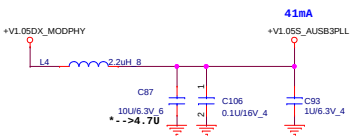
Haswell ULT PCH(POWER)

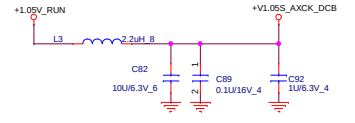
3.3 SUS: 205mA
1.05 SUS: 2066mA
1.05 RUN: 2578mA
3.3 RUN: 58mA

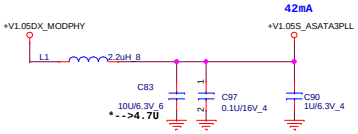


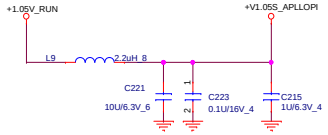
boot strap capacitor	VCCDSW3_3 C233 0.47U/6.3V_4 +DCPSUSBYP

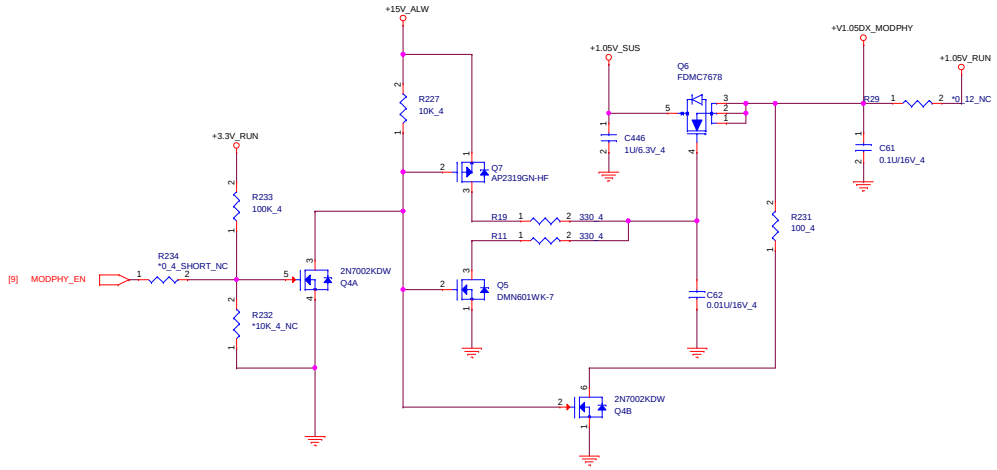












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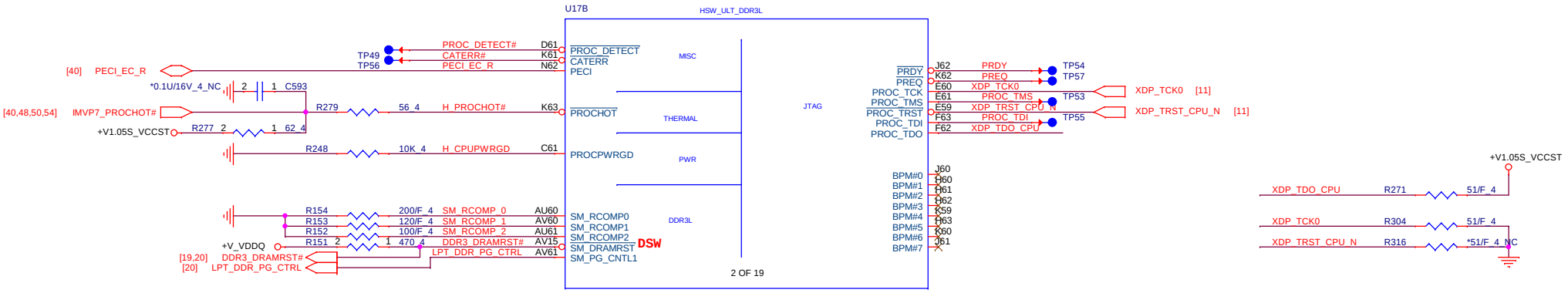

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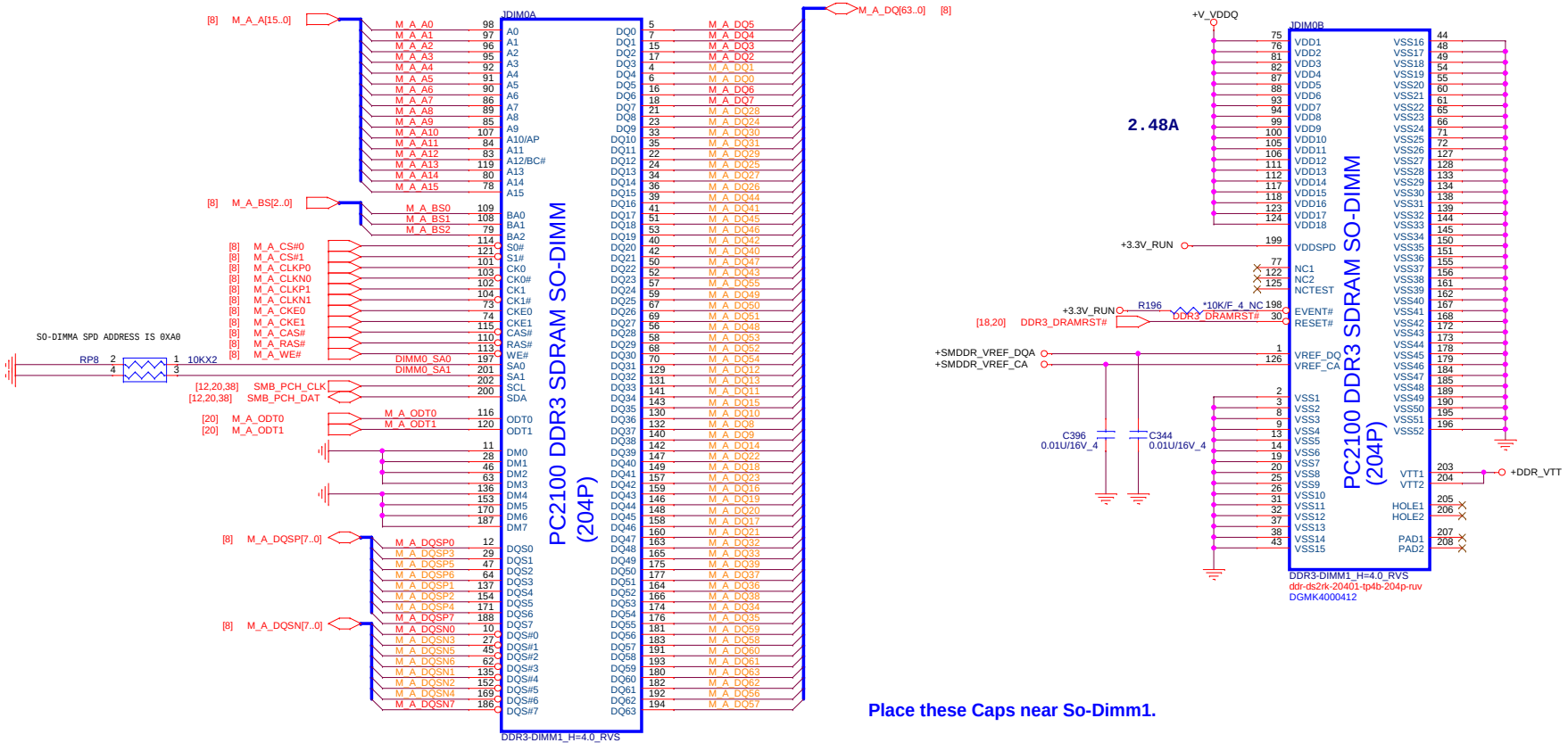
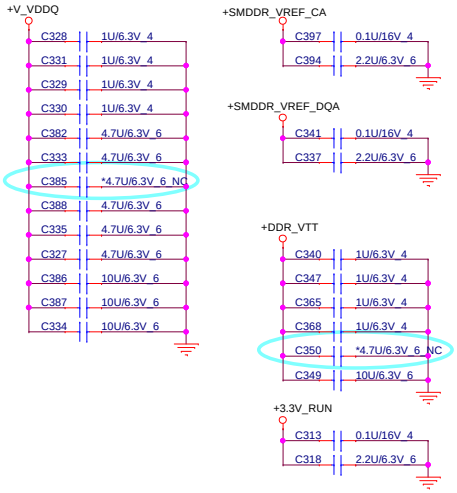
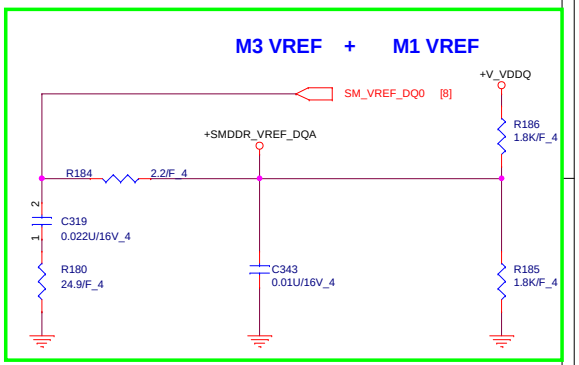
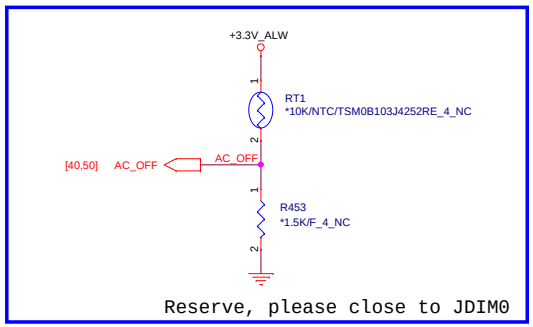


Place these Caps near So-Dimm1.







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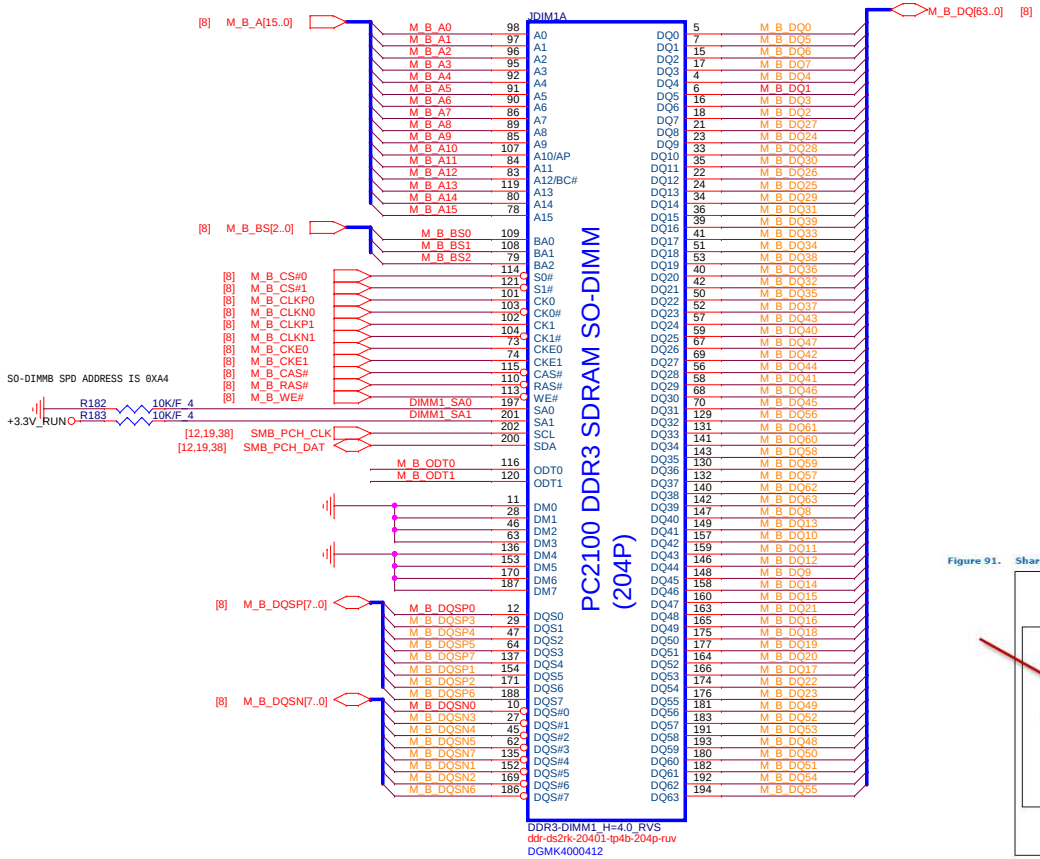


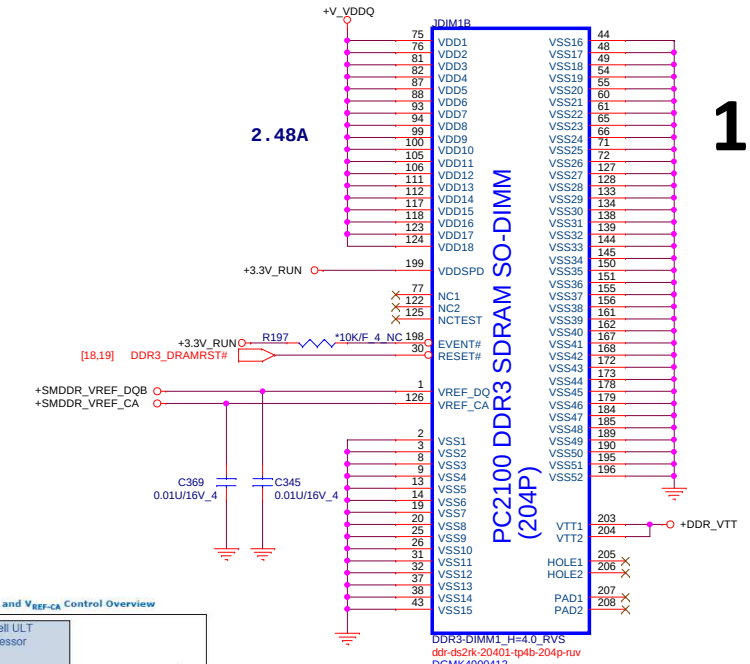
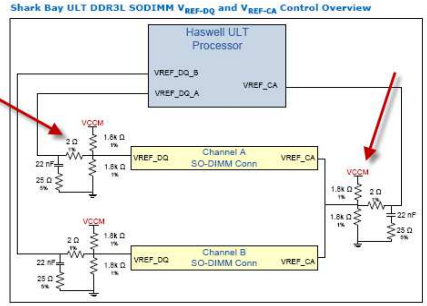
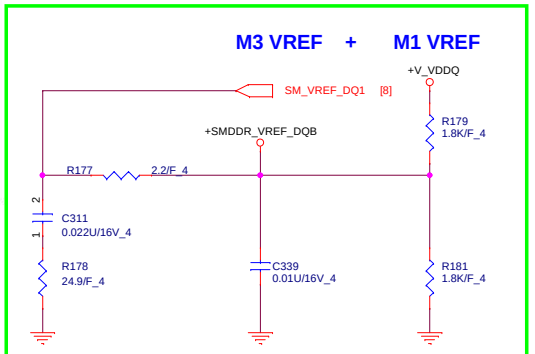
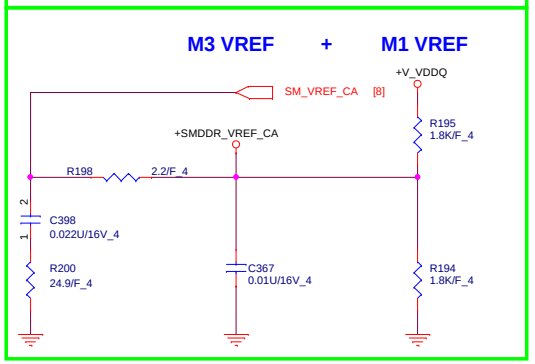


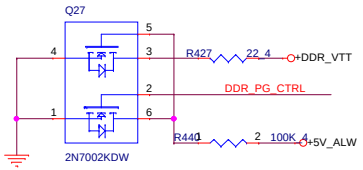
Figure 91. Shark Bay ULT DDR3L SODIMM V_{REF-DQ} and V_{REF-CA} Control Overview



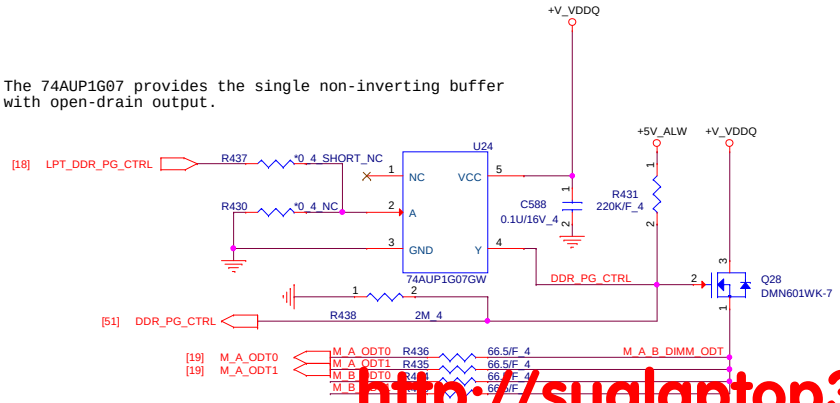




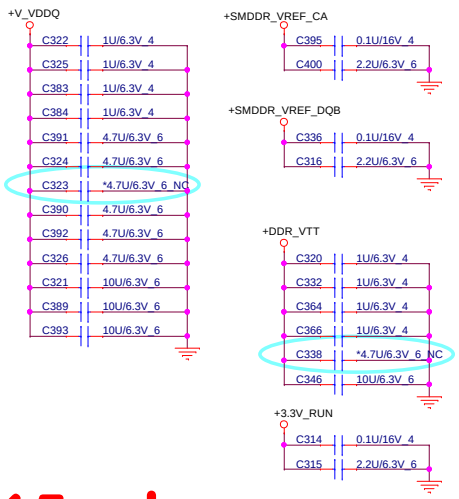
DDR3L SODIMM ODT GENERATION



The 74AUP1G07 provides the single non-inverting buffer with open-drain output.



Place these Caps near So-Dimm2.



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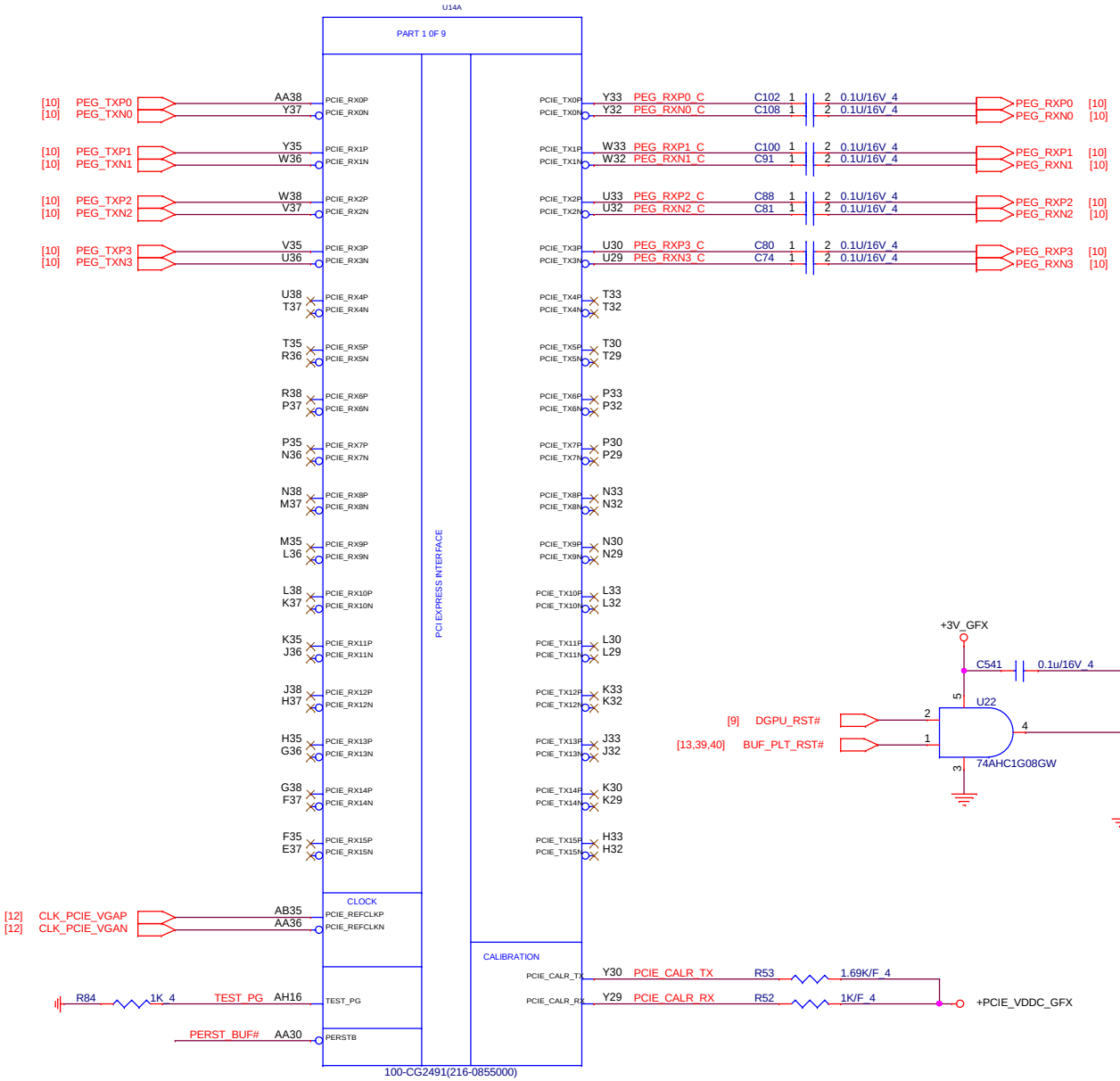
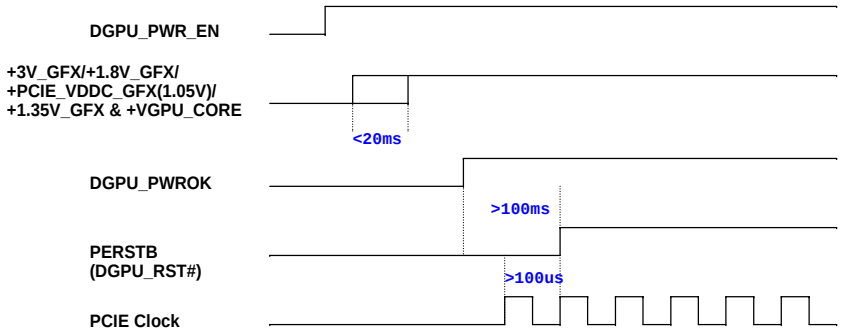
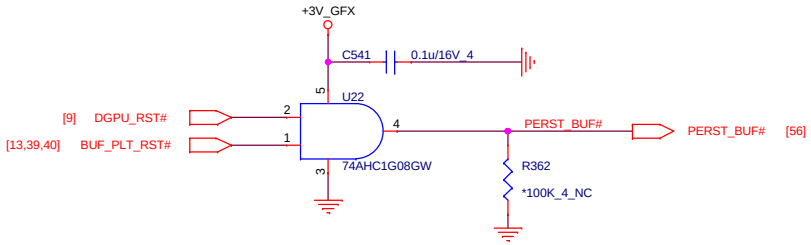


Opal XT Power-on sequence





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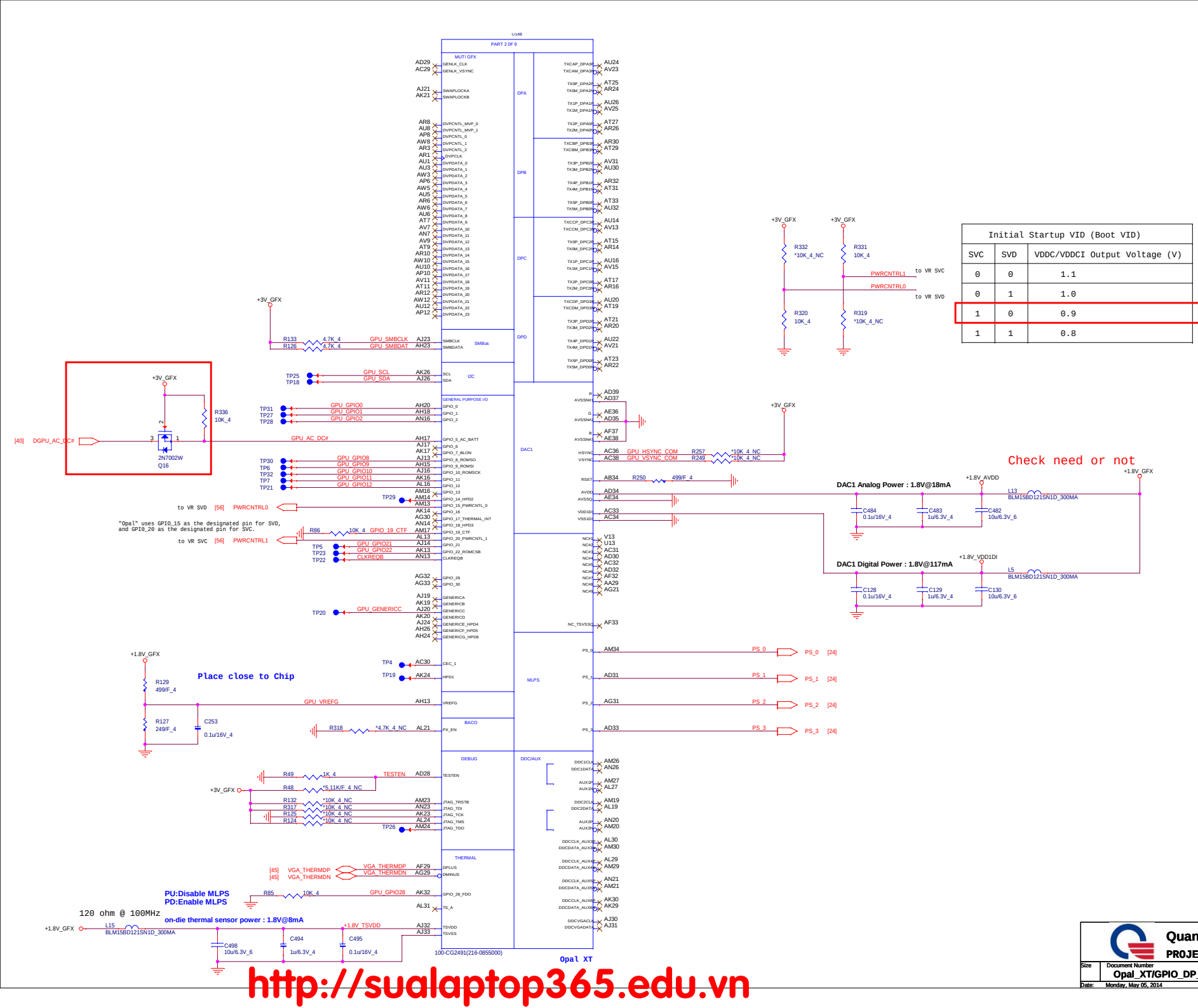

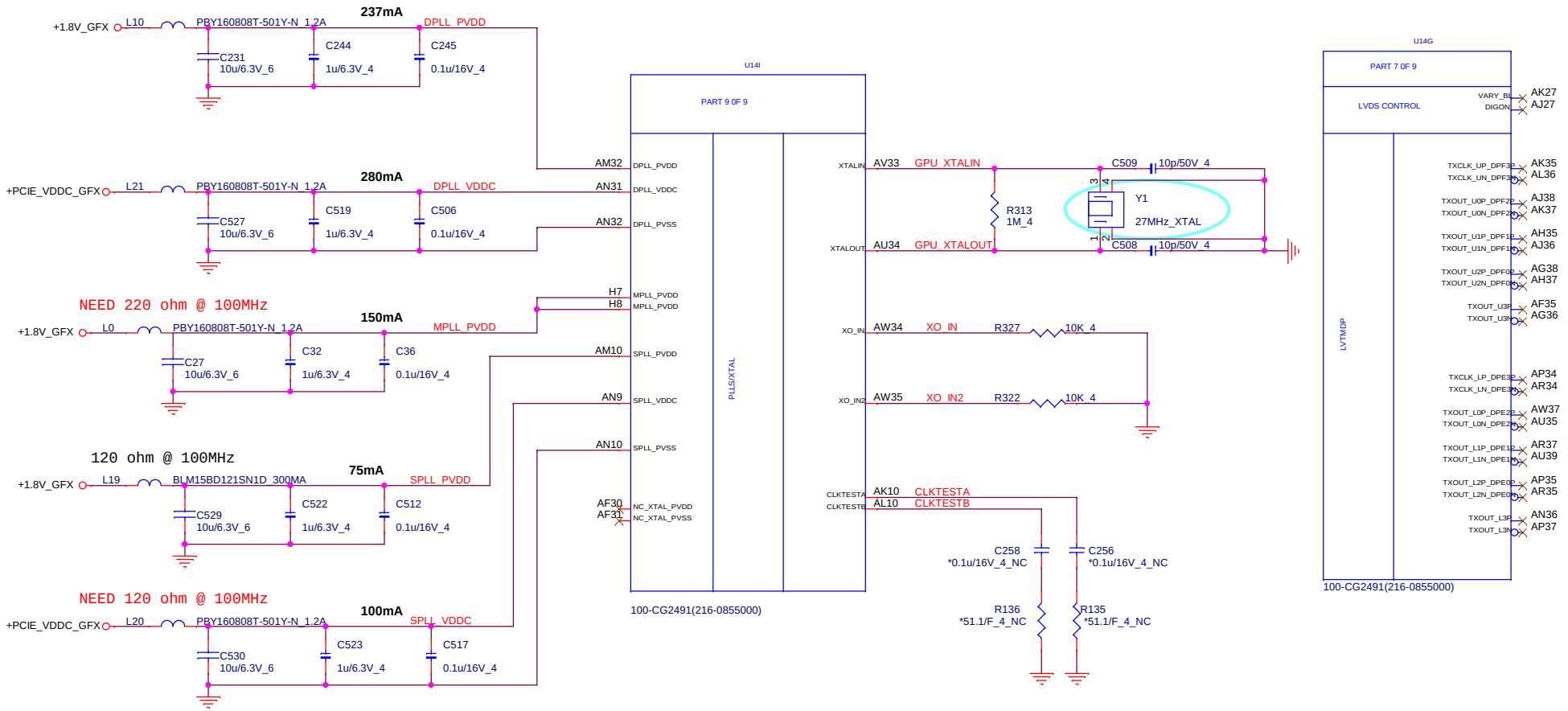

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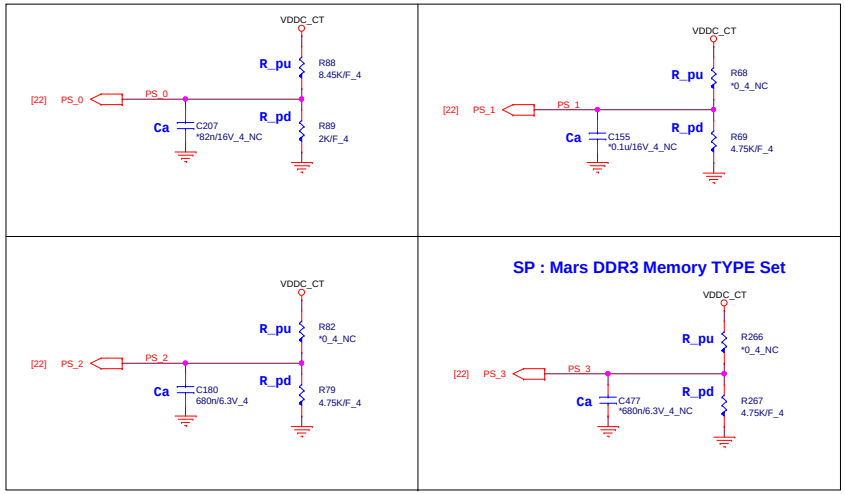

MLPS Bit	Bits [5:1]
PS_0	11001
PS_1	11000
PS_2	00000
PS_3	11XXX

MLPS

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	NA

R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

R_pu/R_pd	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
10K	CS31002FB26

MLPS Bit	Strap Name	AM6 Settings	AM6 Settings	Description	AMD Recommended Settings
PS_0[1]	ROM_CONFIG[0]	1	Memory Aperture Size Select : 256MB	Serial ROM type or Memory Aperture Size Select If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size.	Design dependent, SIZE ROM_CONFIG[2:0] 128MB 000 256MB 001 64MB 010 Reserved 011
PS_0[2]	ROM_CONFIG[1]	0			
PS_0[3]	ROM_CONFIG[2]	0			
PS_0[4]	N/A	1	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	1	All endpoints are usable.	the strap option indicates the number of audio-capable display outputs.	Design dependent
PS_1[1]	STRAP_BIF_GEN3_EN_A	0	PCIe GEN3 is not supported. (use GEN2)	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent
PS_1[2]	STRAP_BIF_CLK_PM_EN	0	The CLKREQB power management capability is disabled	Determines whether or not the PCIe reference clock power management capability 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	0	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1	The transmitter full-swing is enabled	Control the transmitter full-/ half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	1	Tx deemphasis enabled.	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent
PS_2[1]	N/A	0	Reserved.	Reserved.	N/A
PS_2[2]	N/A	0	Reserved.	Reserved.	N/A
PS_2[3]	STRAP_BIOS_ROM_EN	0	Disable the external BIOS ROM device.	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent
PS_2[4]	STRAP_BIF_VGA_DIS	0	Standalone dGPU design	VGA disable determines whether or not the card will be recognized as the system's VGA controller 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	Standalone dGPU design = 0 AMD PowerXpress design = 1
PS_2[5]	N/A	0	Reserved.	Reserved.	N/A
PS_3[1]	BOARD_CONFIG[0]	X	VRAM vendor BOARD_CONFIG[2:0] Hynix 000 default Micron 001 Samsung 010	Board configuration related strapping, such as for memory ID	Design dependent
PS_3[2]	BOARD_CONFIG[1]	X			
PS_3[3]	BOARD_CONFIG[2]	X			
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	1	No usable endpoints.	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	Design dependent
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]	1			

System Memory Aperture size

GPIO9 BIOSROM	SIZE	GPIO13 ROM_CONFIG2	GPIO12 ROM_CONFIG1	GPIO11 ROM_CONFIG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	Reserved	0	1	1

Vendor	Vendor P/N	STN B/S P/N	Size	Opal USE MLPS
Hynix	H5TC4G63AFR-11C (256M*16)	AKD5PGWTW11 * 8	4GB	000
Micron	MT41J256M16HA-093G:E (256M*16)	AKD5PZSTL02 * 8	4GB	001
Samsung	K4W4G1646D-BC1A (256M*16)	AKD5PGWT500 * 8	4GB	010

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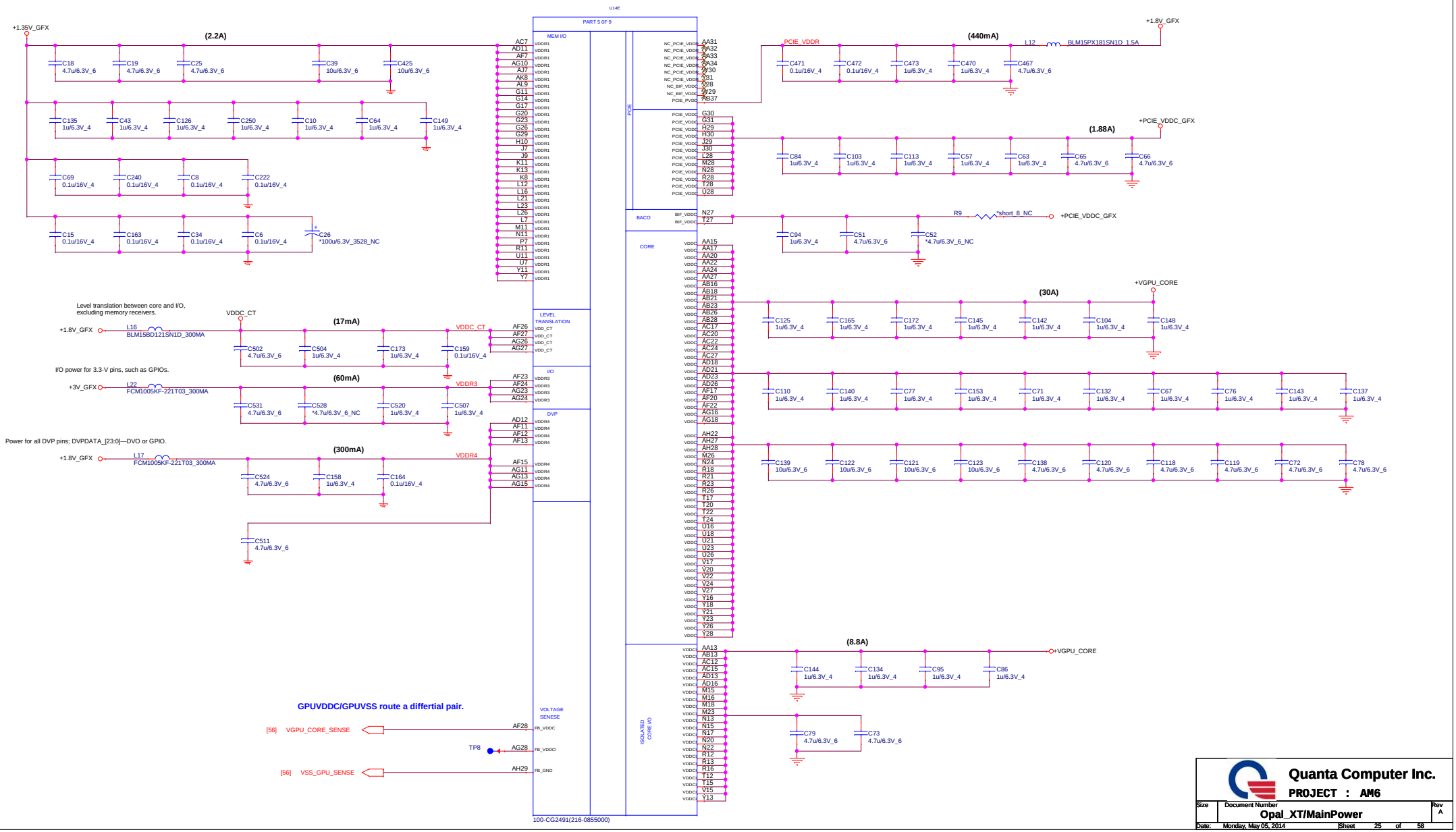

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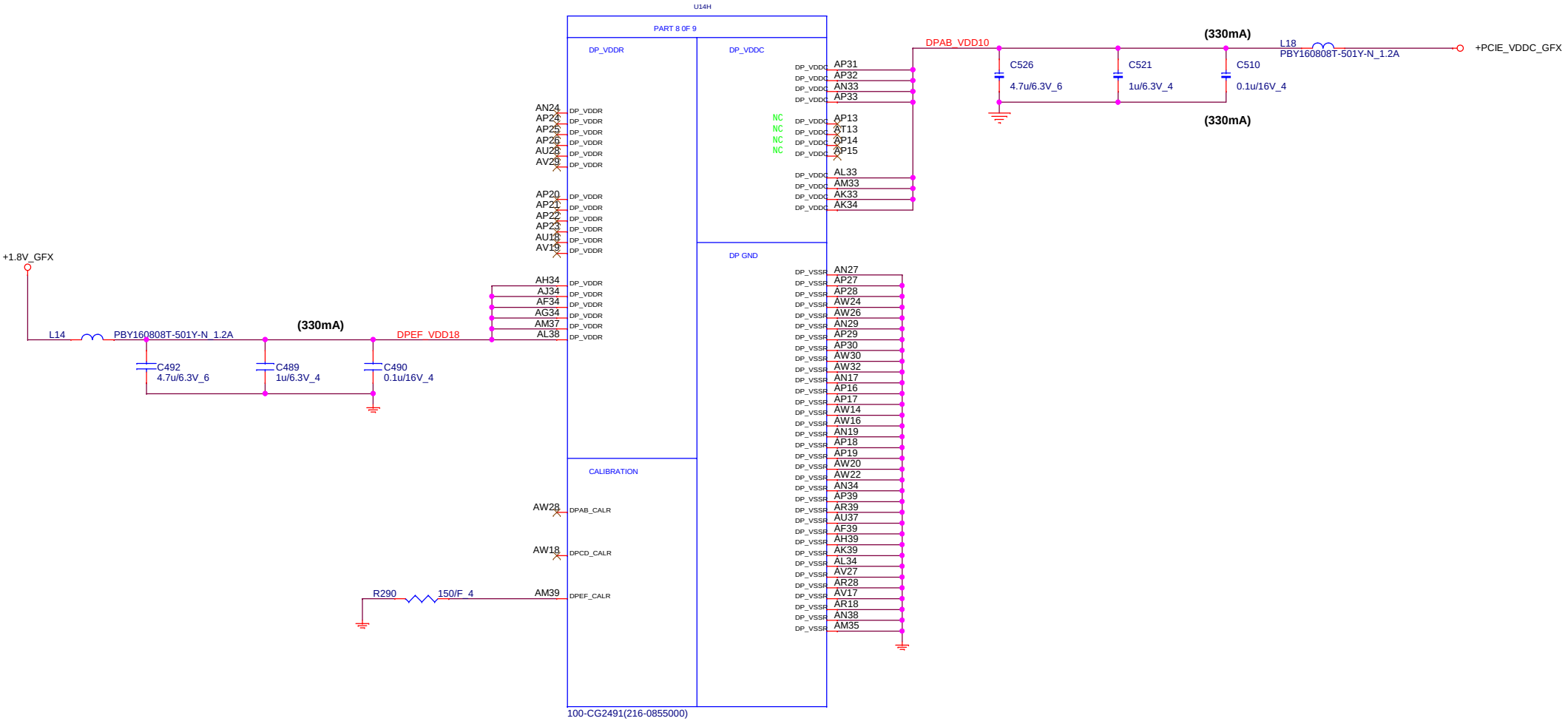

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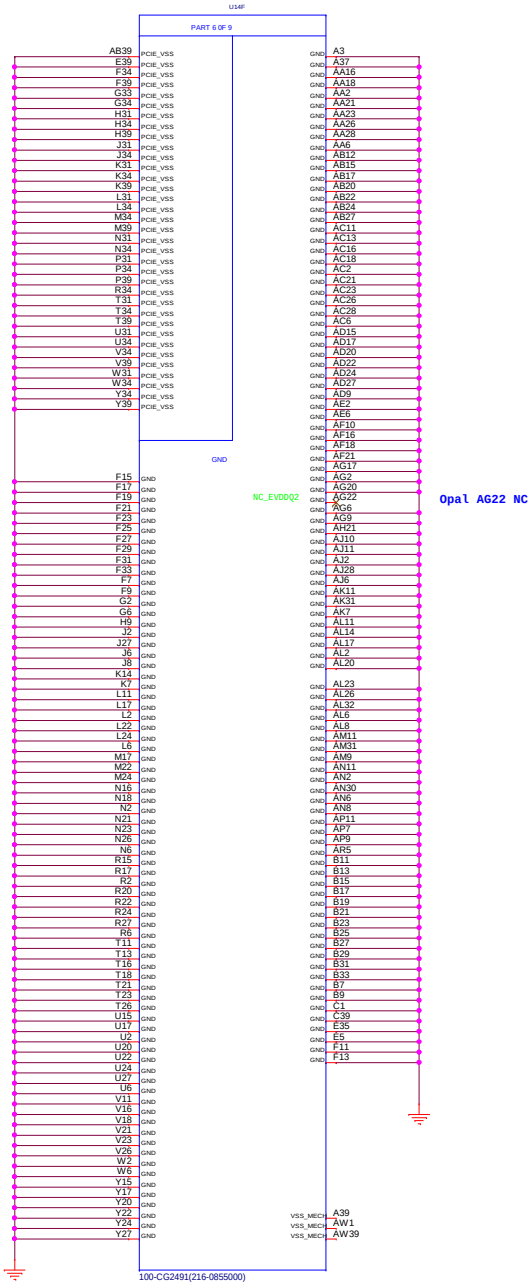
<VGA>



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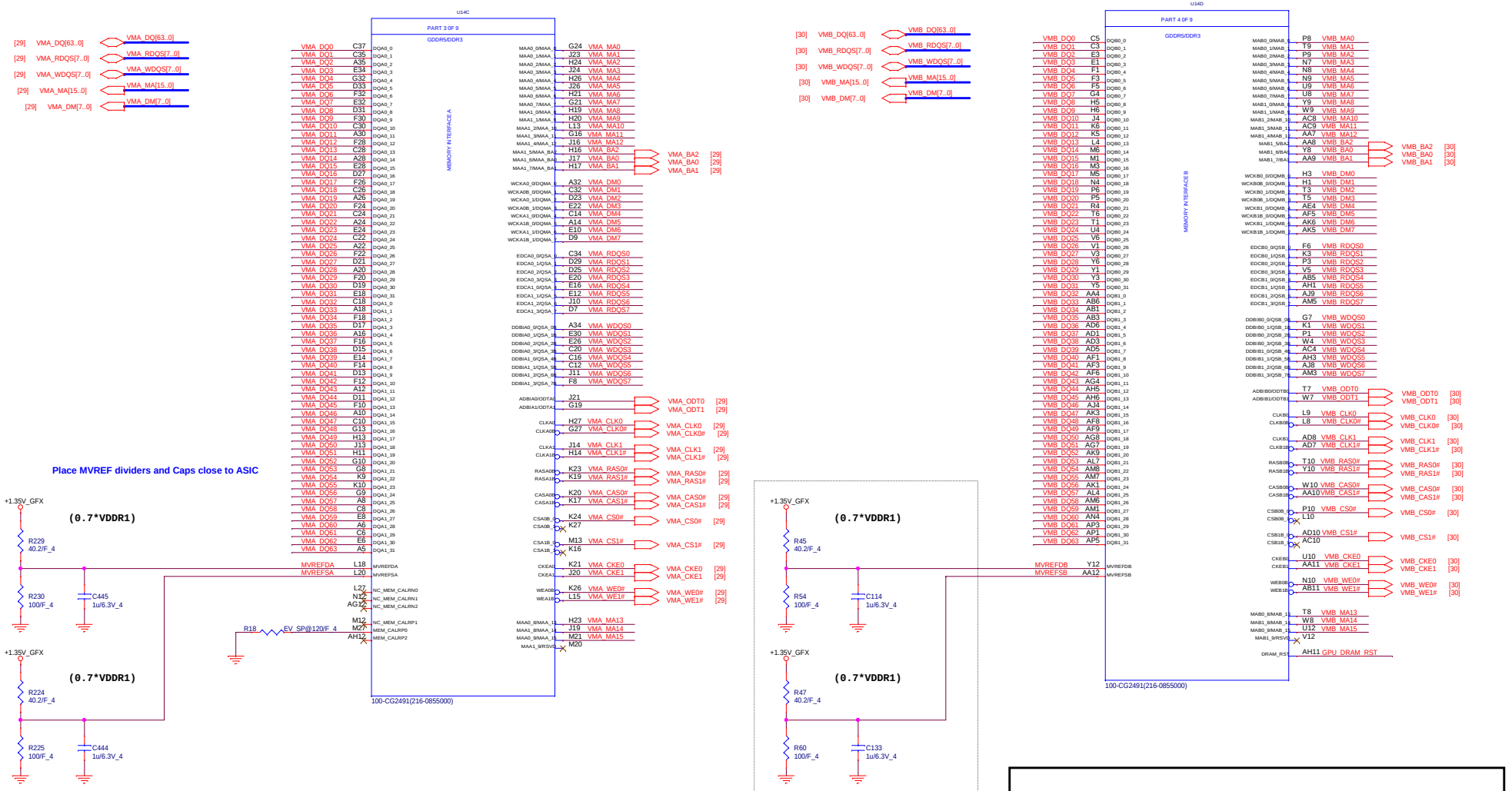

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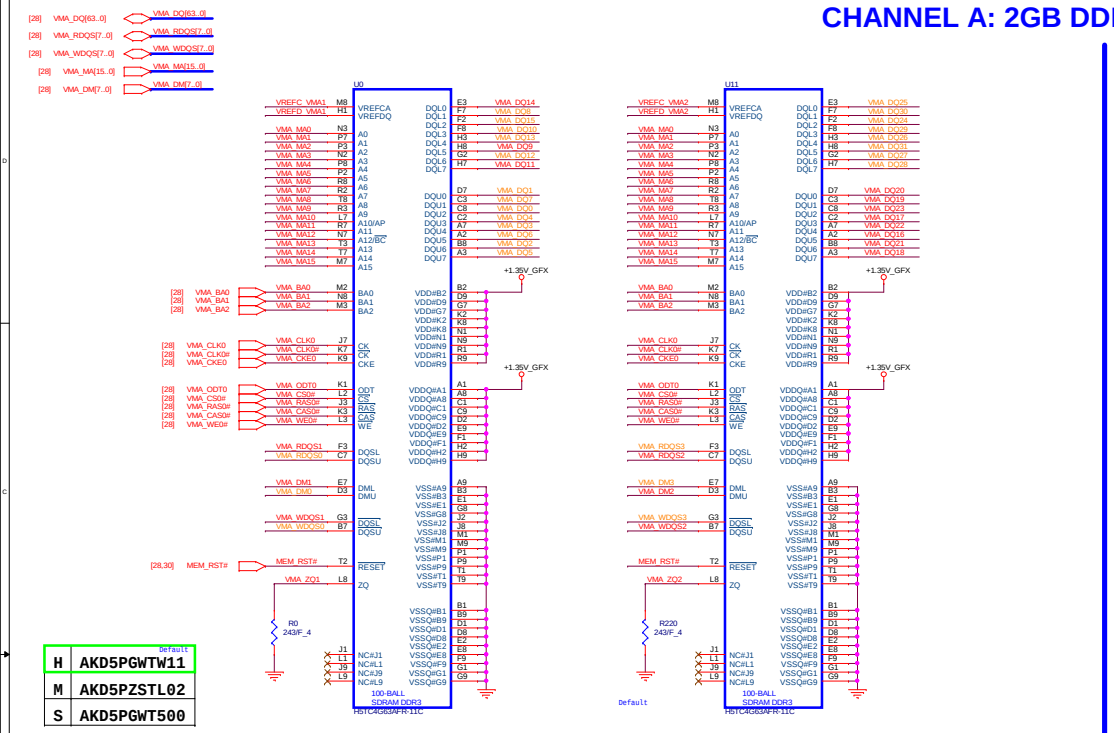
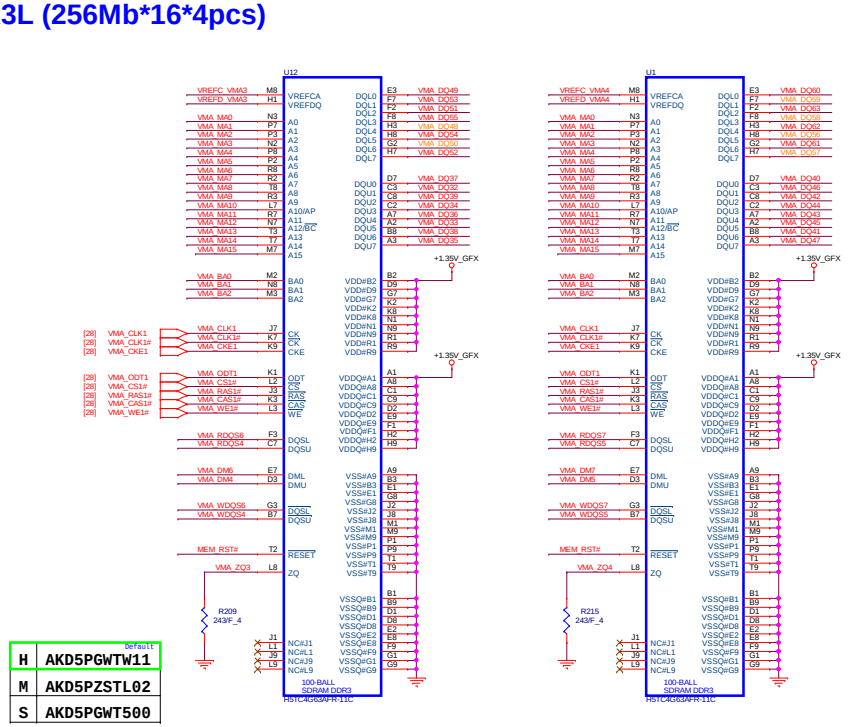
CHANNEL A: 2GB DDR3L (256Mb*16*4pcs)

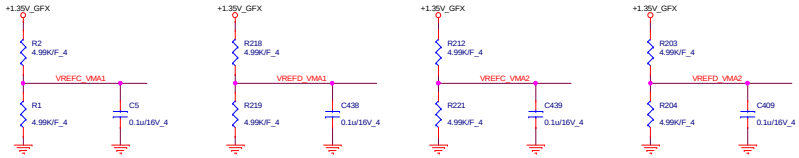


H	AKD5PGWTW11
M	AKD5PZSTL02
S	AKD5PGWT500

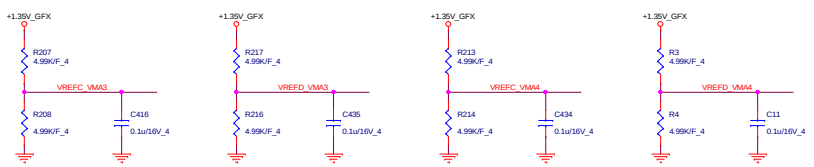


H	AKD5PGWTW11
M	AKD5PZSTL02
S	AKD5PGWT500

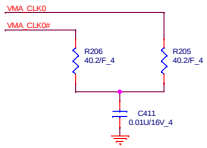
Group-A0 VREF



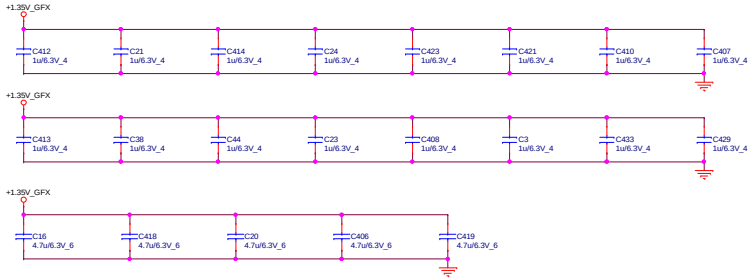
Group-A1 VREF



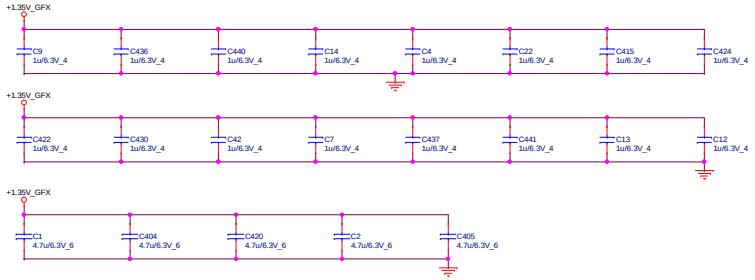
MEM_A0 CLK



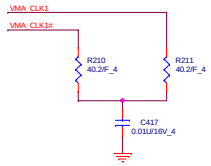
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



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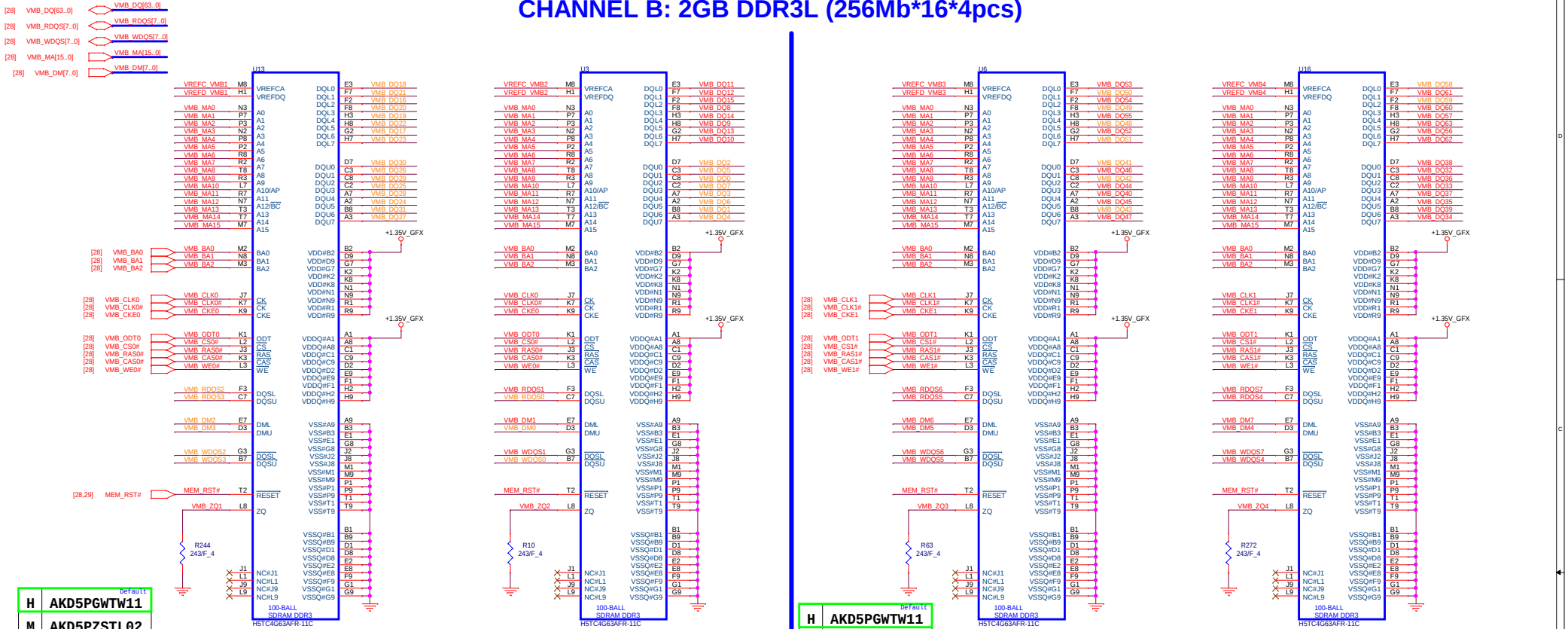
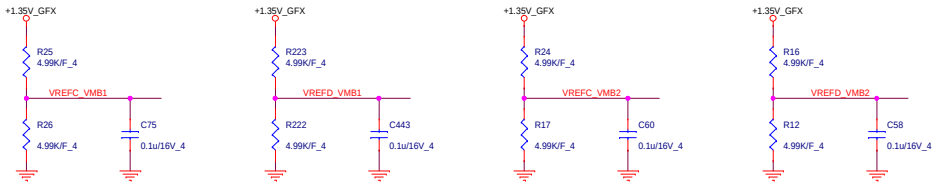
CHANNEL B: 2GB DDR3L (256Mb*16*4pcs)

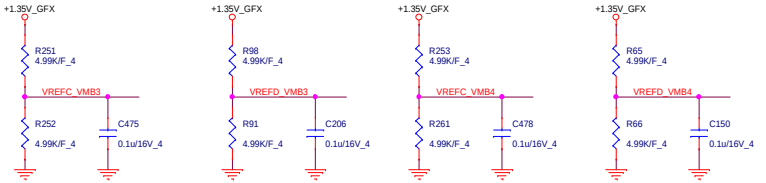


	Default
H	AKD5PGWTW11
M	AKD5PZSTL02
S	AKD5PGWT500

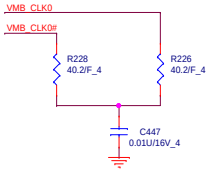
Group-B0 VREF



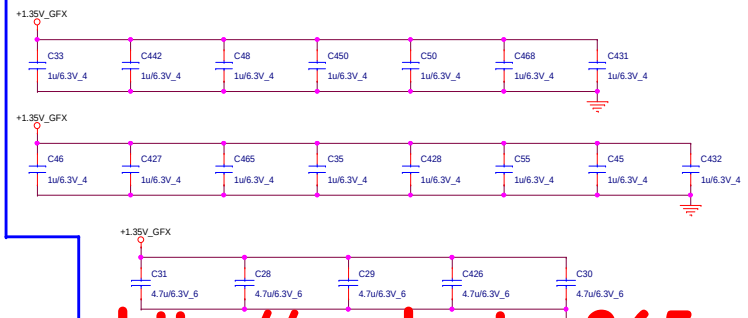
Group-B1 VREF



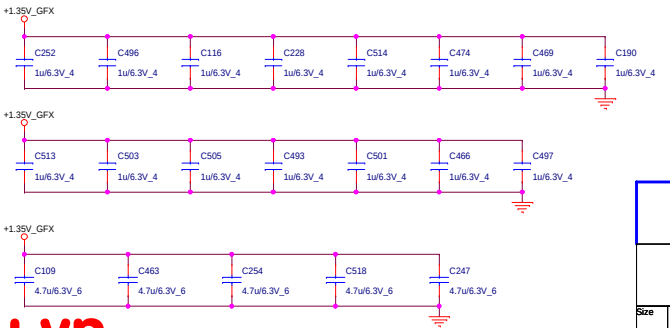
MEM_B0 CLK



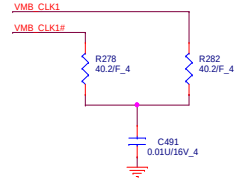
Group-B0 decoupling CAP



Group-B1 decoupling CAP



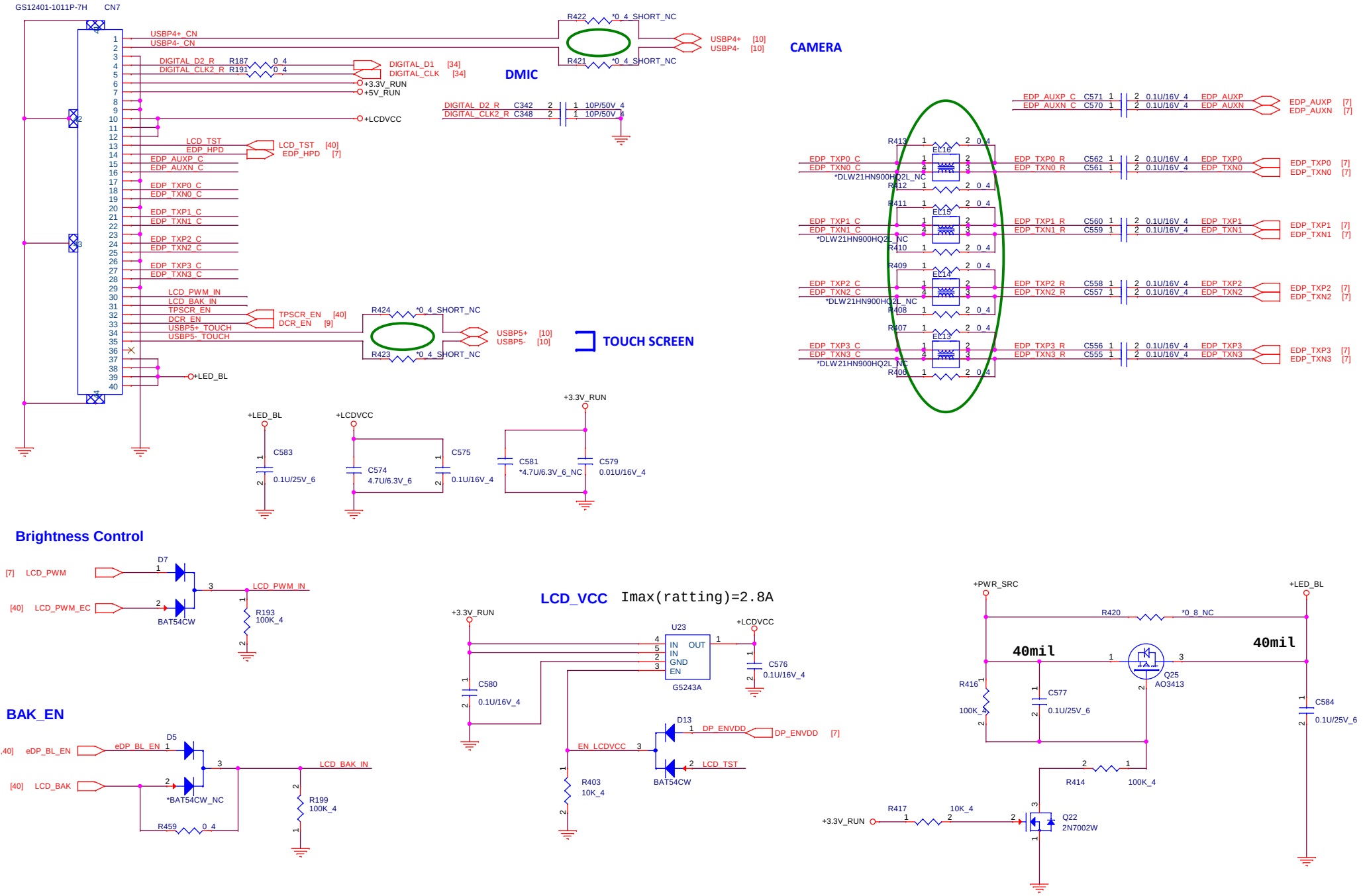
MEM_B1 CLK



Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	Opal_XT/VRAM_B	A

Date: Monday, May 05, 2014 Sheet 30 of 58

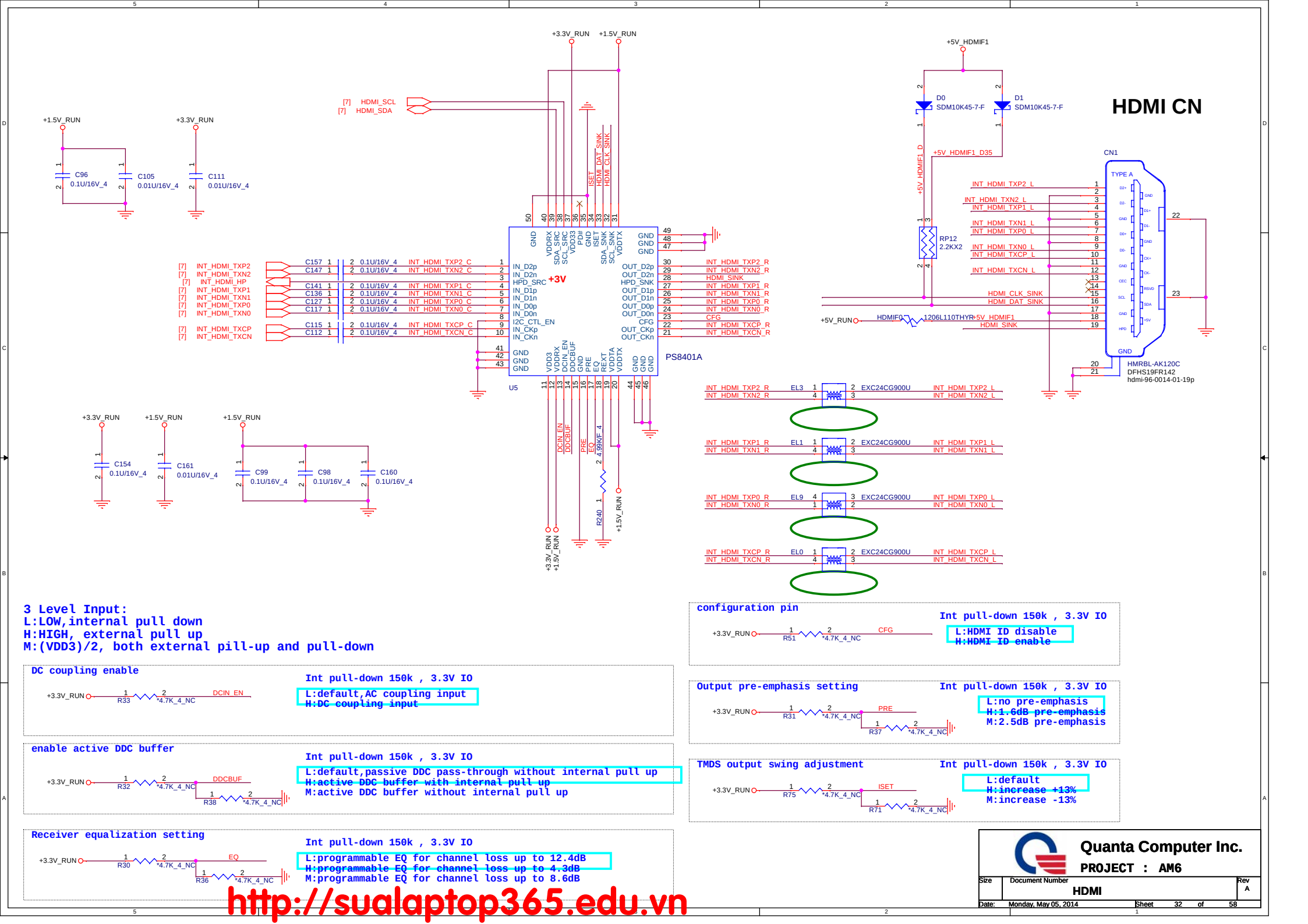


Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	eDP CONN	A

Date: Monday, May 05, 2014 Sheet 31 of 58



H8
*H-C158D158N_NC

H6
*H-C158D158N_NC

H20
*h-o114x98d114x98n_NC

H1
*H-TC236BC197D98P2_NC

H0
*H-TC236BC197D98P2_NC

H7
*H-TC236BC197D98P2_NC

H4
*H-TC236BC197D98P2_NC

H9
*O-AM6-2_NC

H10
*h-c236i158d118p2_NC

H11
*h-c236i158d118p2_NC

H3
*h-c236i158d118p2_NC

H14
*h-c236i158d118p2_NC

H2
*H-TC236BC197D98P2_NC

H13
*O-AM6-1_NC

H12
*H-C118X98D118X98N_NC

H5
*H-C118X98D118X98N_NC

Bracket

HOLE0

*intel-CPU-bracket_NC

H17
H-TC217BC141D141PT

NGFF NUT

NUT

H15
H-TC217BC141D141PT

H16
H-TC217BC141D141PT

H18
H-TC217BC141D141PT

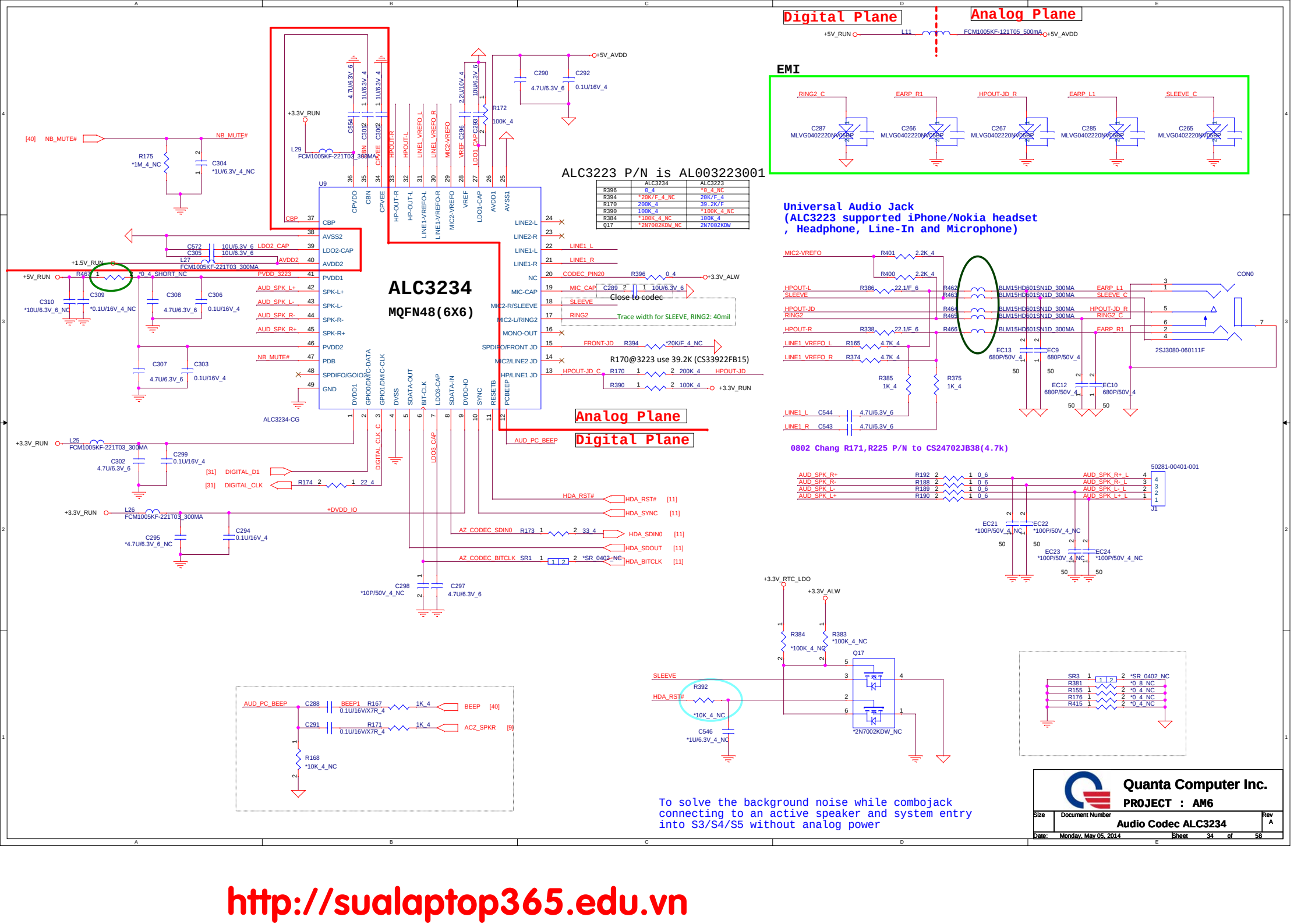
H19
H-TC217BC141D141PT

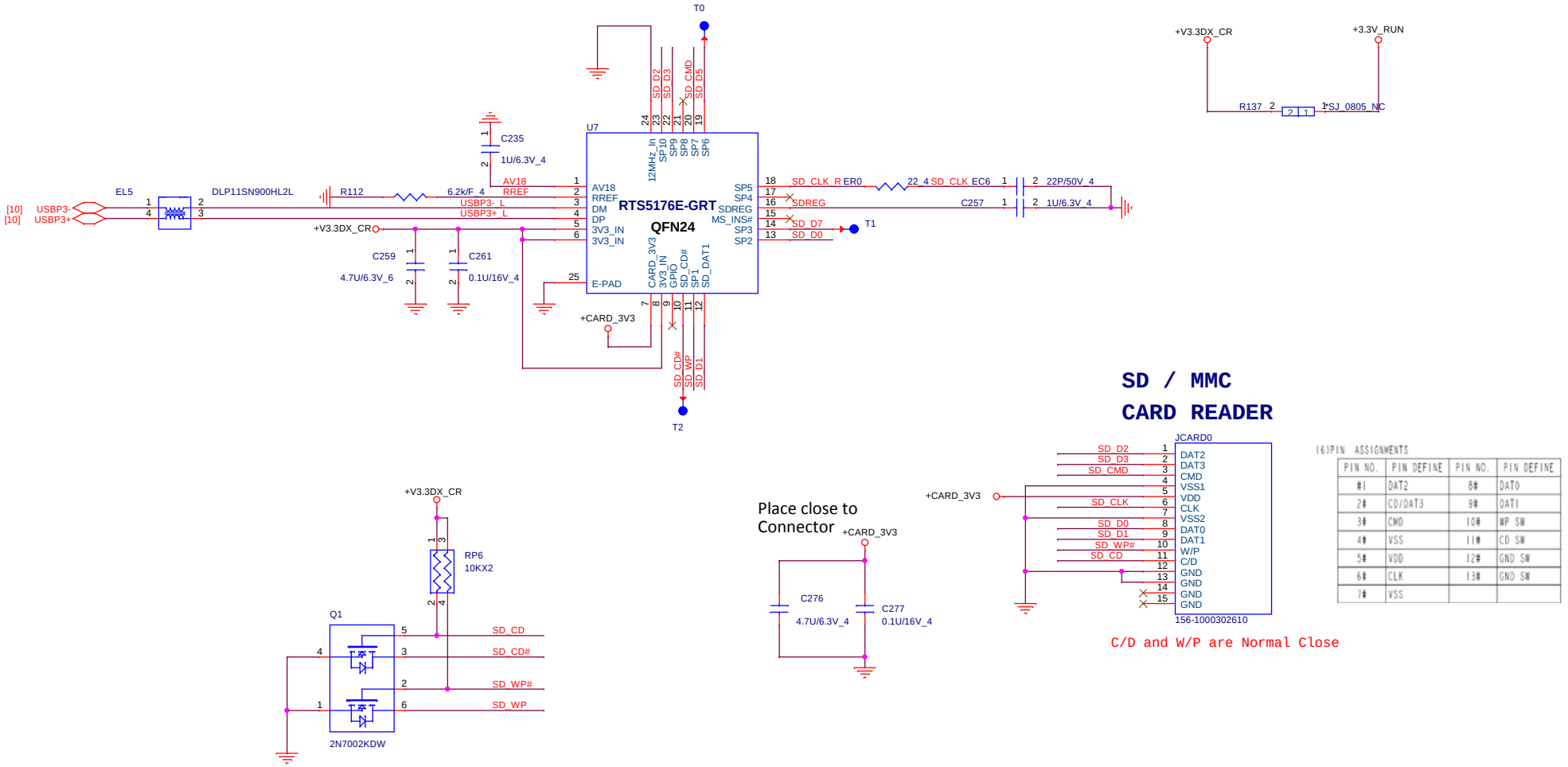
Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	Hole	A

Date: Monday, May 05, 2014 Sheet 33 of 58





Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: Card Reader RTS5176E	Rev: A
Date: Monday, May 05, 2014	Sheet 35 of 58	

USB3.0 Power Share

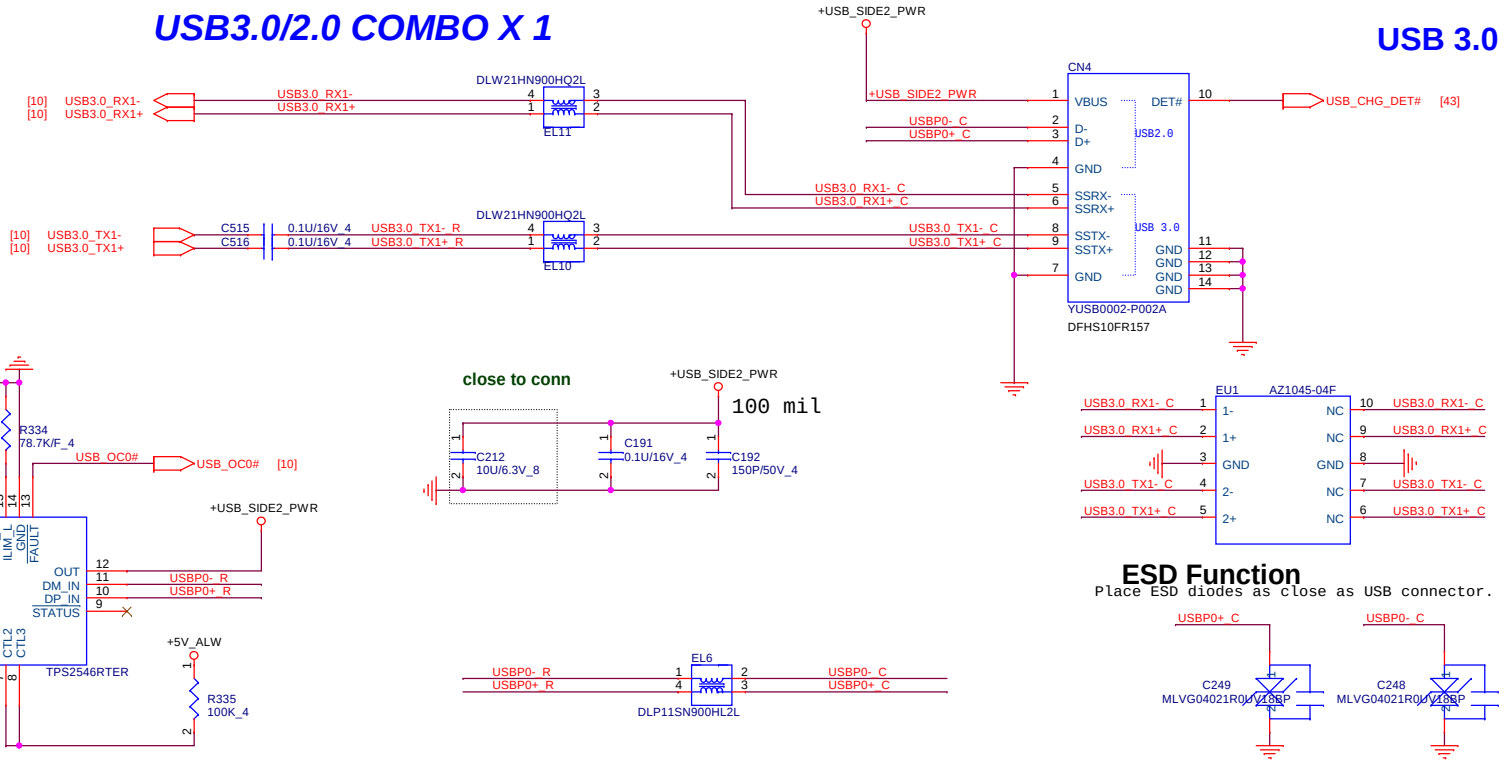
USB Power share

USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.2

	R337	mA	
OC limitation	100k ohm	504	
	22.1k ohm	2274	Applied Now

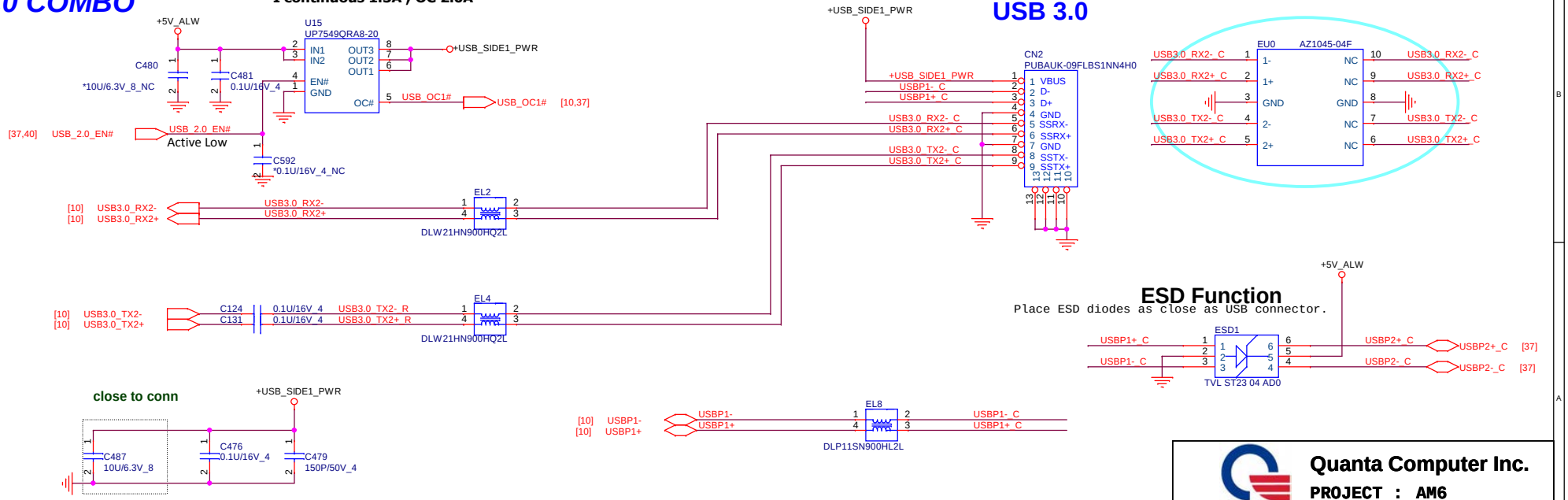
Current limit = 50250/(R337)

USB3.0/2.0 COMBO X 1



USB3.0/2.0 COMBO

M15 Design Requirement:
I continuous 1.5A ; OC 2.0A



Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	USB3/USB Charger	A

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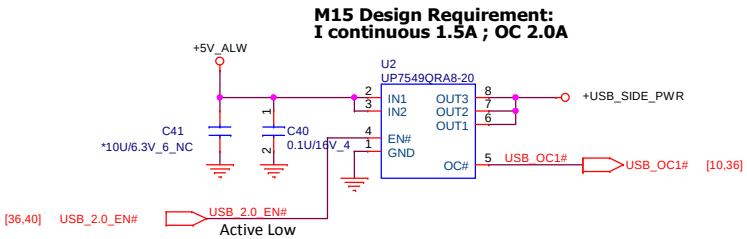
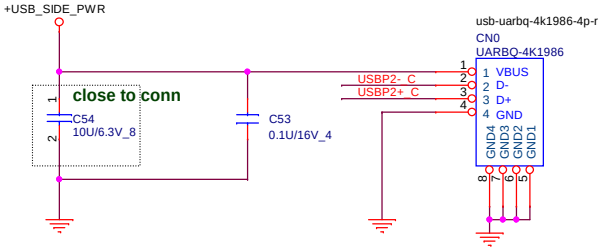
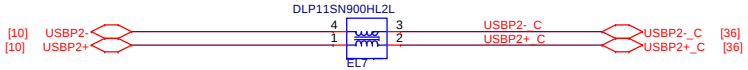
USB2.0 X1







Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	USB2*1	A

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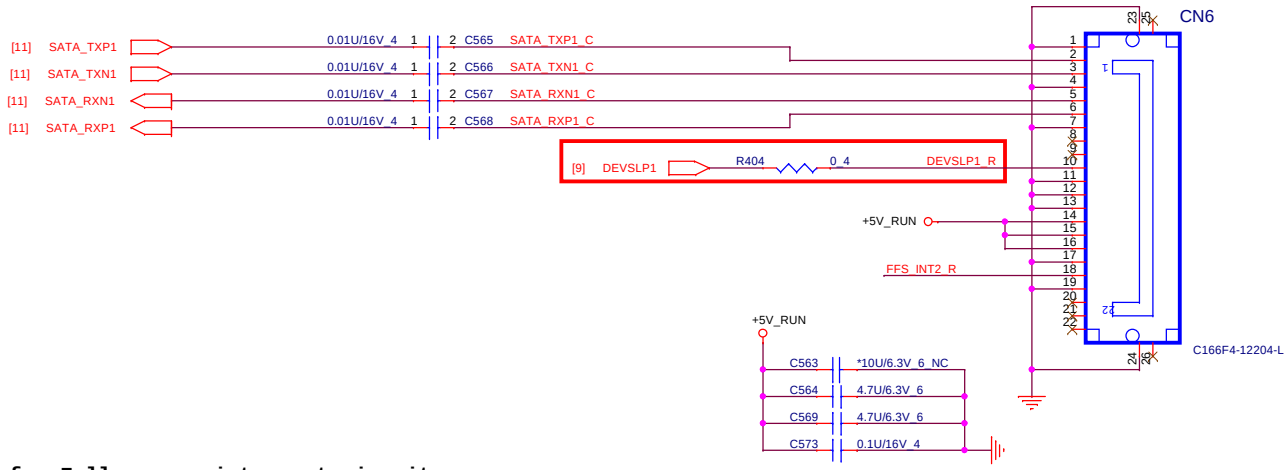
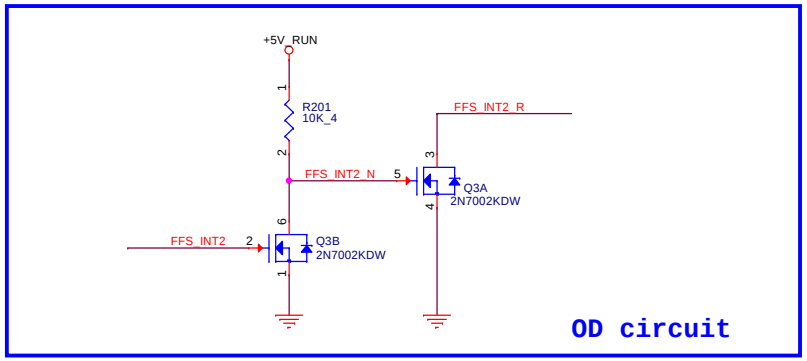
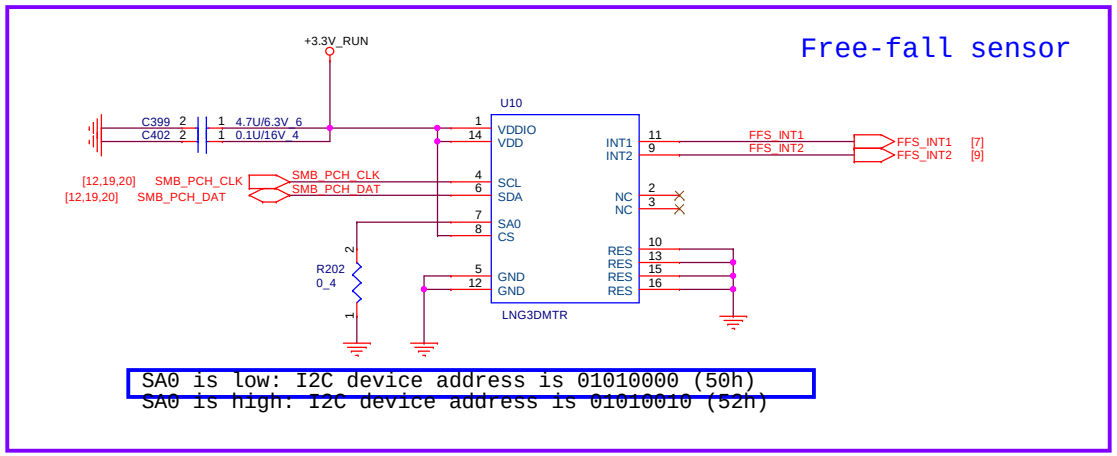
SATA HDD Connector



If you have two HDD,need add two OD circuit for Fall sensor interrupt circuit

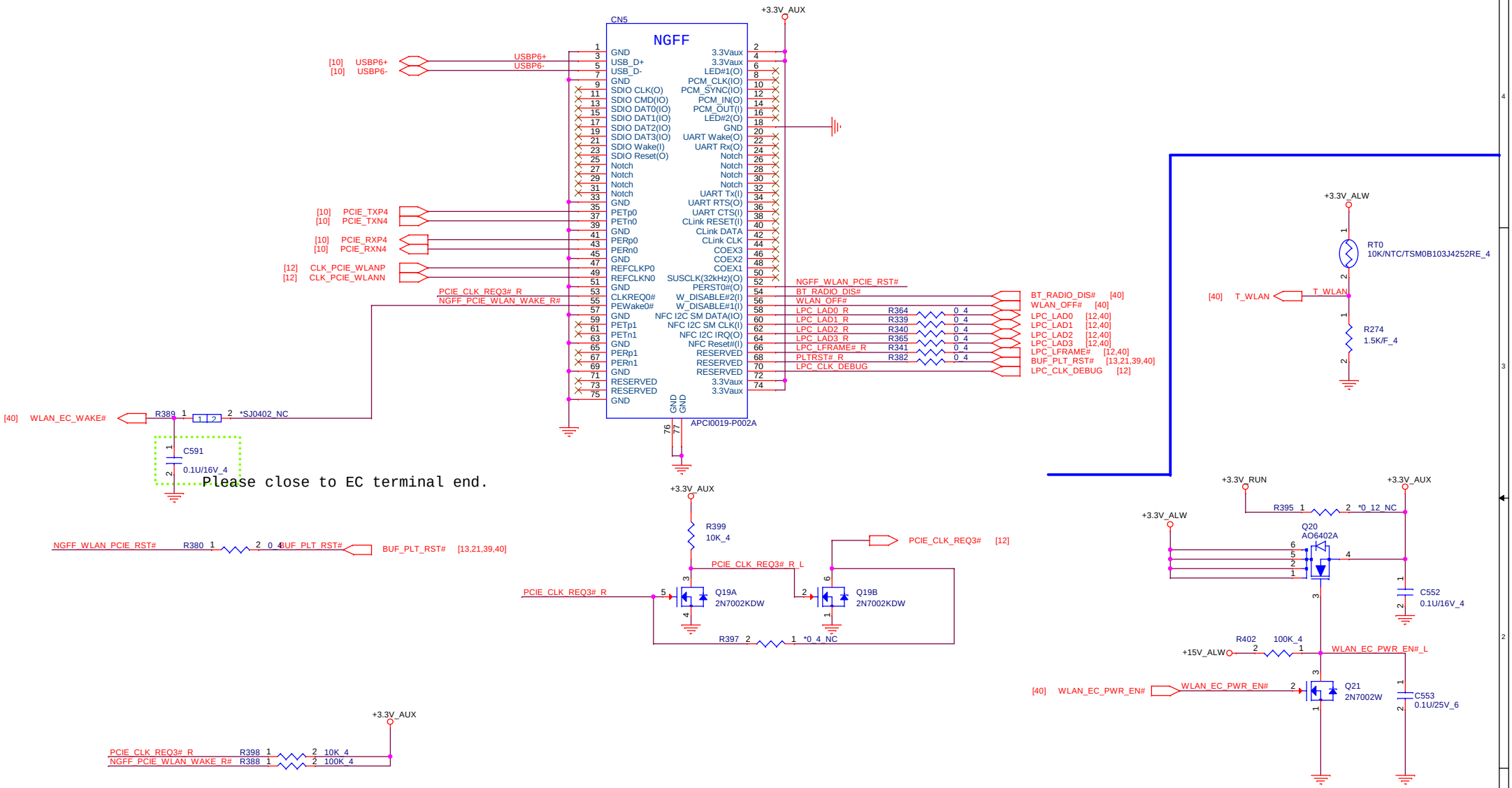




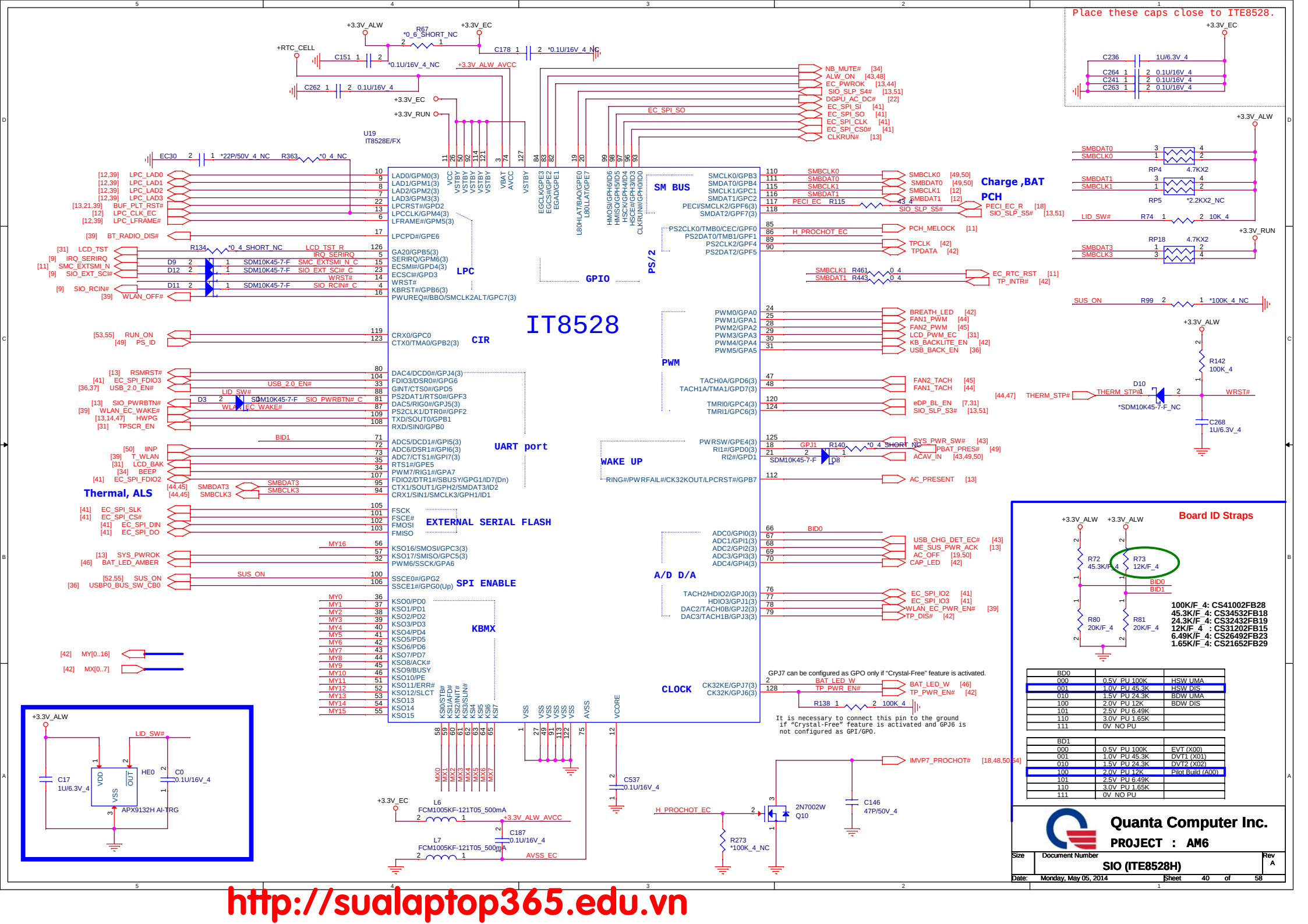
Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	SATA HDD/Accelerometer	A
Date: Monday, May 05, 2014	Sheet 38 of 58	

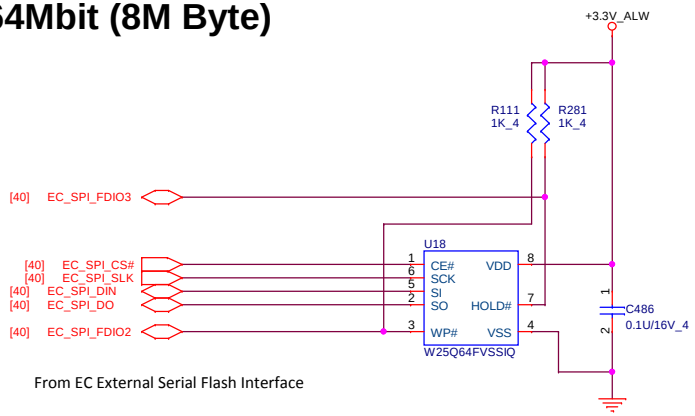
NGFF Wifi/BT connector



Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: Wifi/BT NGFF	Rev: A
Date: Monday, May 05, 2014	Sheet 39 of 58	

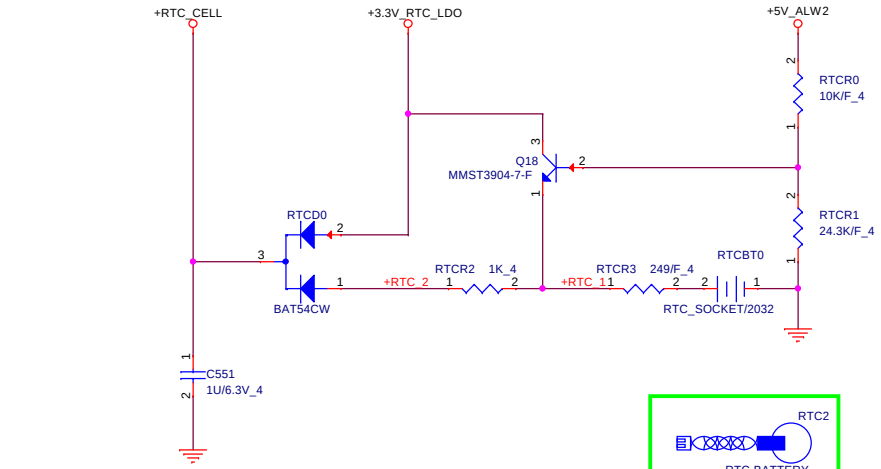

Place these caps close to ITE8528.
IT8528
U19
IT8528E/FX
LPC
GPIO
PS/2
SM BUS
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Charge ,BAT
PCH
Thermal, ALS
Board ID Straps
100K/F_4: CS41002FB28
45.3K/F_4: CS34532FB18
24.3K/F_4: CS32432FB19
12K/F_4 : CS31202FB15
6.49K/F_4: CS26492FB23
1.65K/F_4: CS21652FB29
GPJ7 can be configured as GPO only if "Crystal-Free" feature is activated.
It is necessary to connect this pin to the ground if "Crystal-Free" feature is activated and GPJ6 is not configured as GPI/GPO.
Quanta Computer Inc.
PROJECT : AM6
SIO (ITE8528H)
Monday, May 05, 2014
http://sualaptop365.edu.vn

For EC 64Mbit (8M Byte)



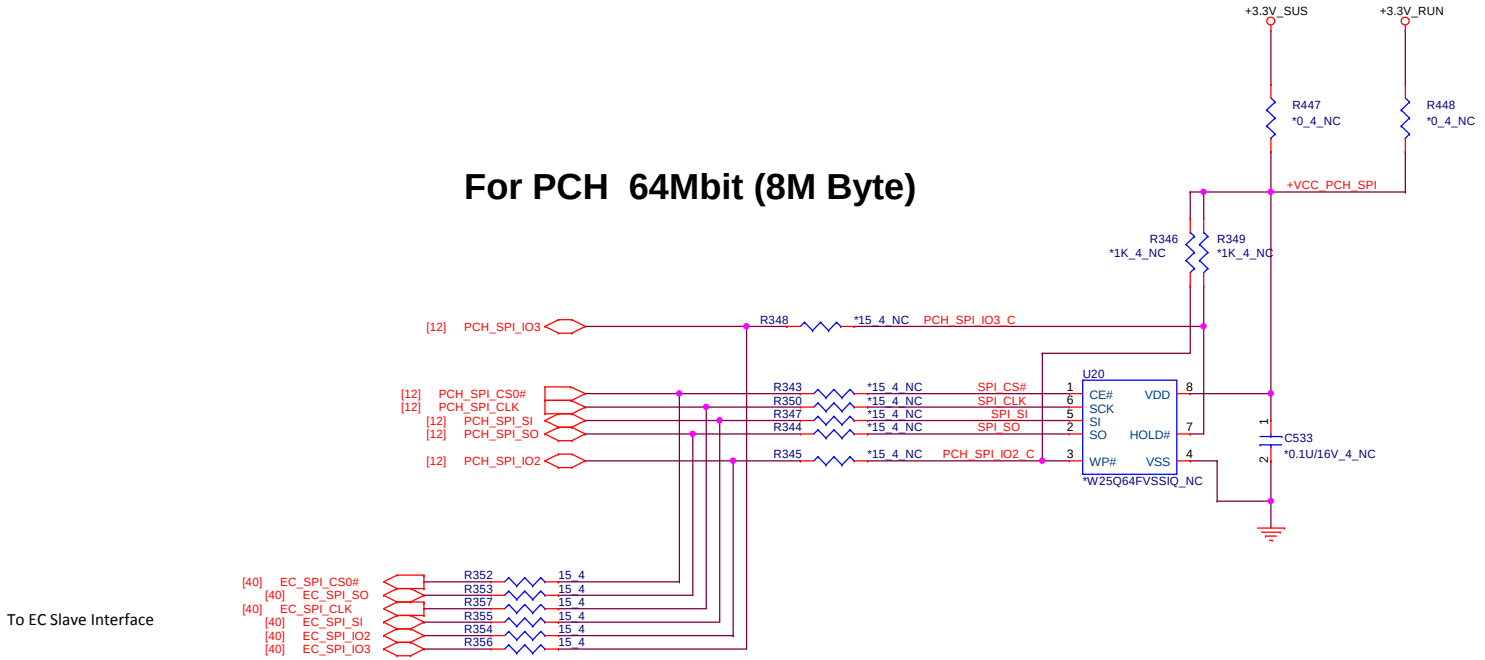
From EC External Serial Flash Interface

RTC BATTERY



5*[24.3/(24.3+10)]-0.8=2.74V
RTC Battery Charger when lower than 2.74V

For PCH 64Mbit (8M Byte)



To EC Slave Interface

Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	FLASH / RTC	A
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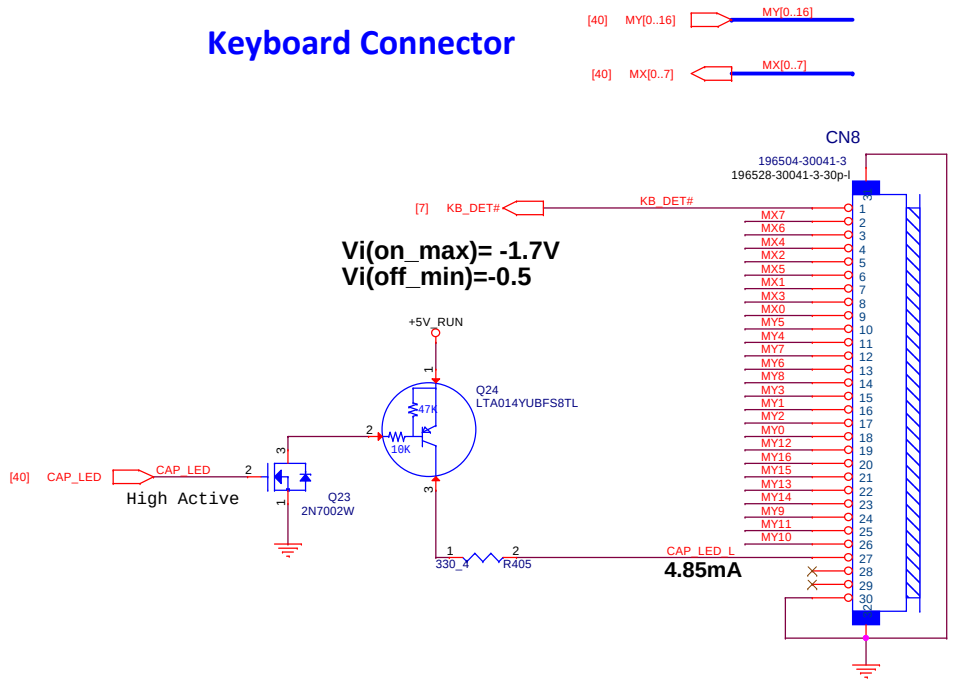
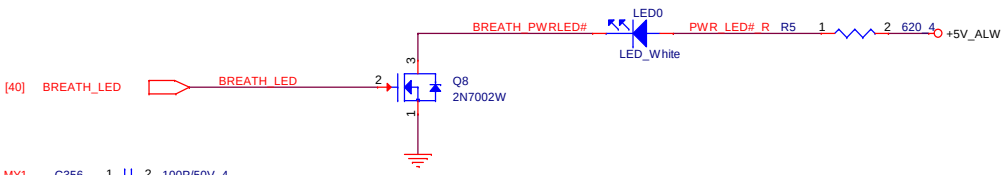
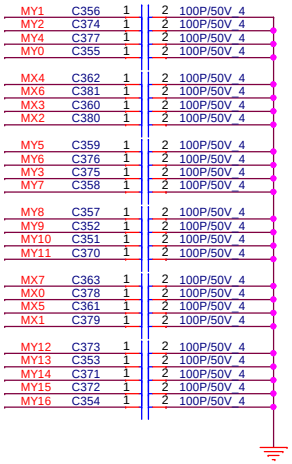
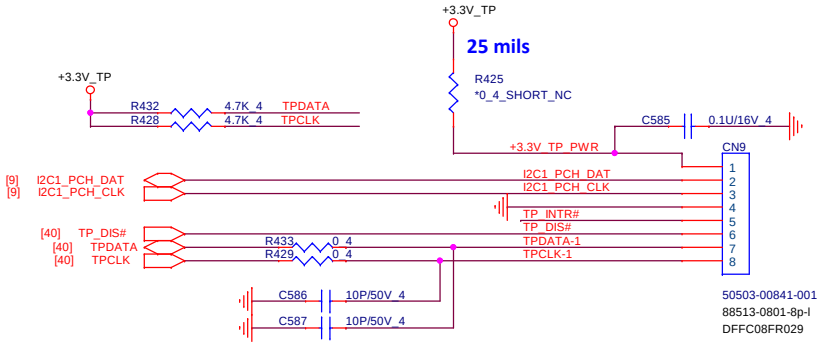
Keyboard Connector



BREATH_LED

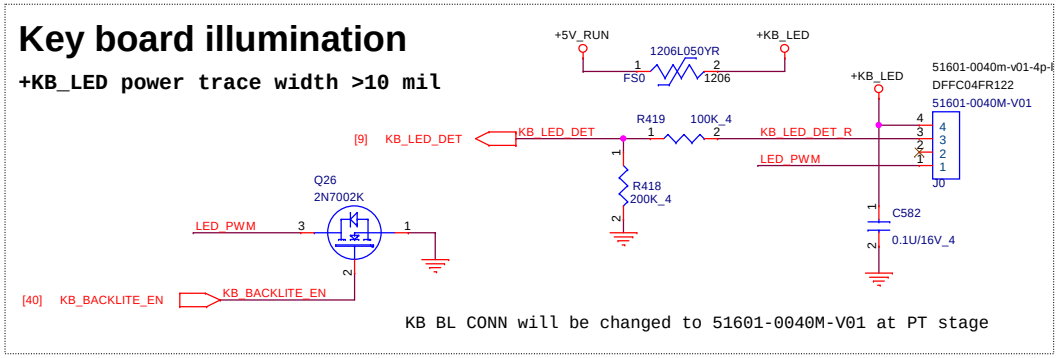




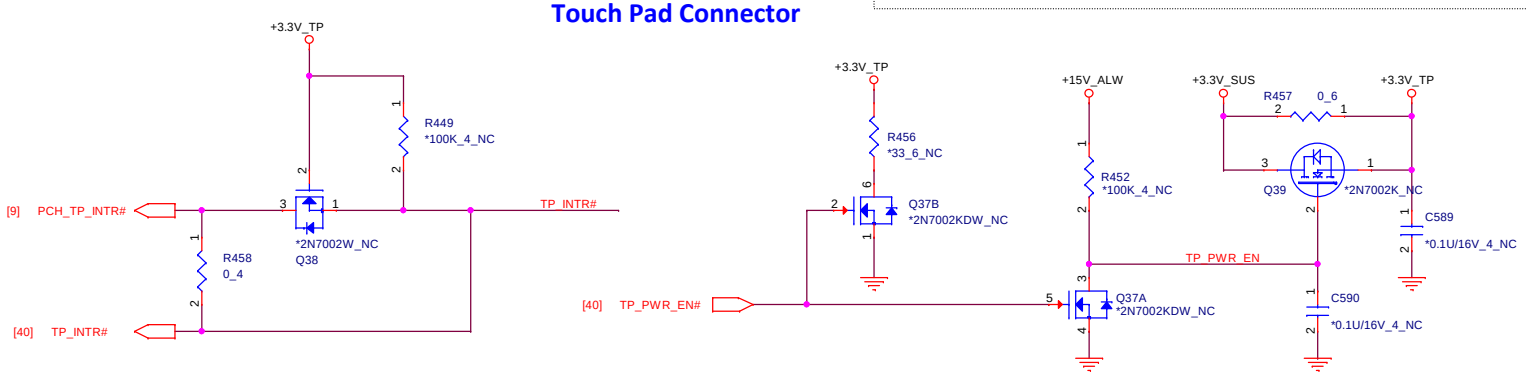


Key board illumination

+KB_LED power trace width >10 mil



Touch Pad Connector



Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	KB/CLK Gen/FAN/TP	A

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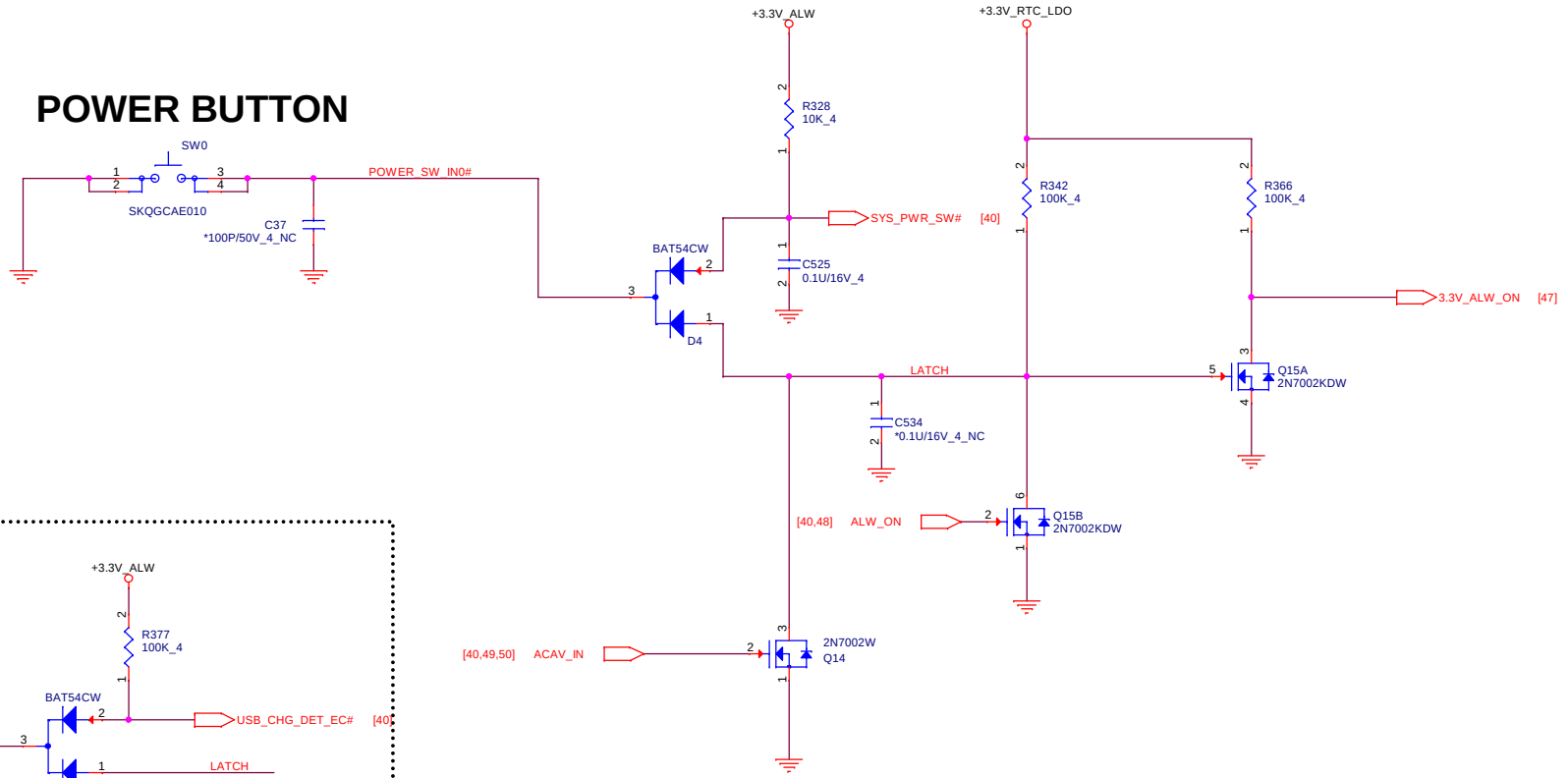
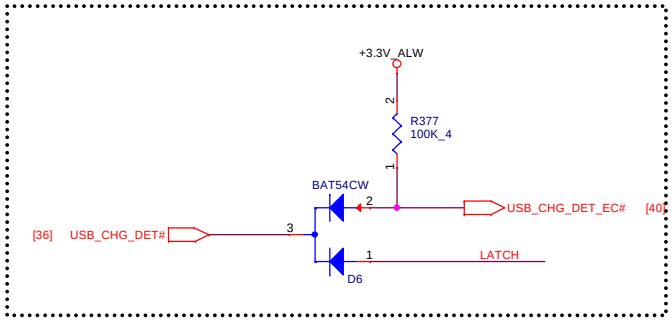
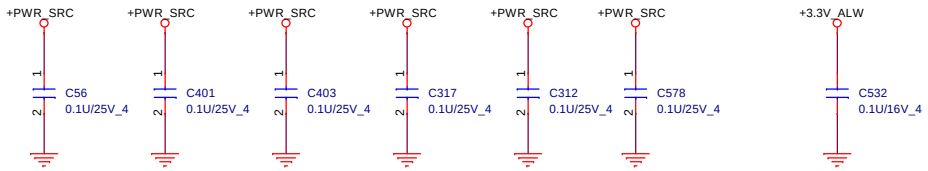
3VALW ON POWER LOGIC

POWER BUTTON





Stitching Capacitors



Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	3VALW ON POWER LOGIC	A
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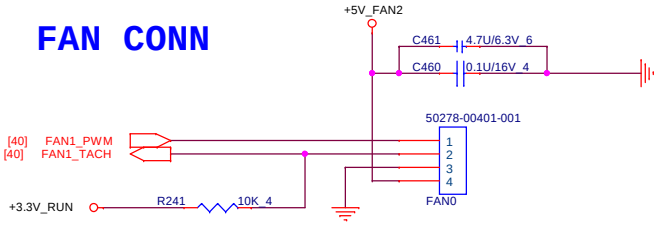
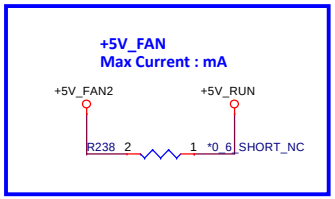
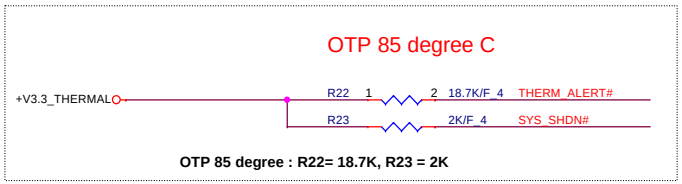
FAN CONN



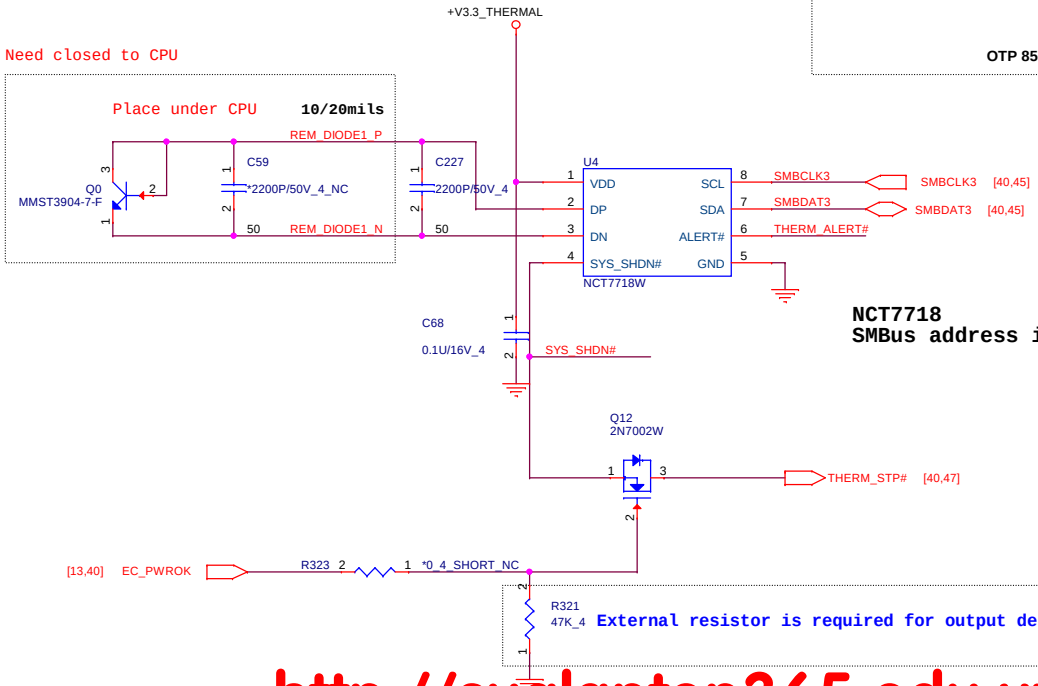


THERMAL IC

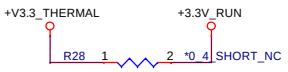


OTP 85 degree : R22= 18.7K, R23 = 2K

SYS_SHD# / ALERT#	2K	7.5K	10.5K	14K	18.7K
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C



NCT7718
SMBus address is 1001100xb (98h) (x is R/W bit).



+V3.3_THERMAL
Max Current :mA

Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	FAN & THERMAL	A

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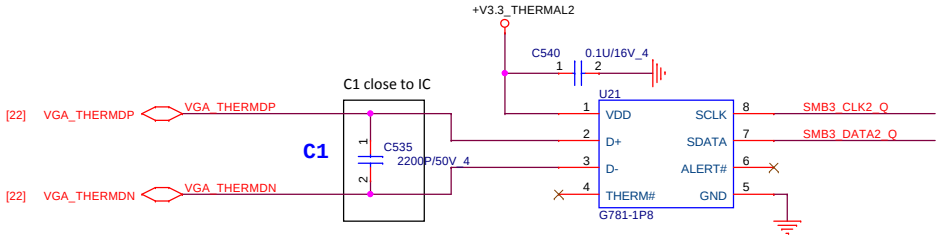
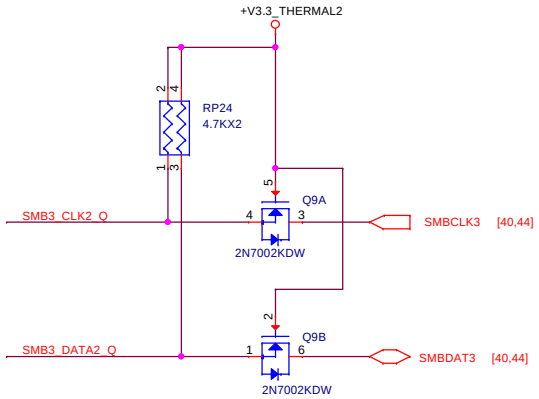
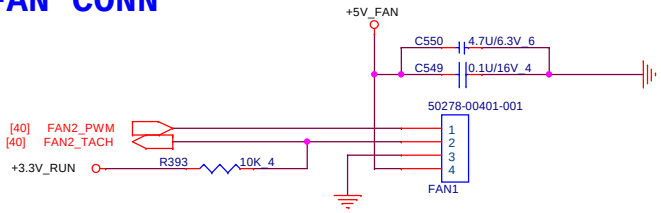
For GPU use

G781-1P8
SMBus address is 1001101xb (9Ah) (x is R/W bit).

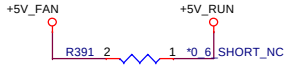


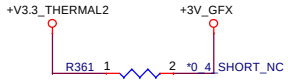


FAN CONN



+5V_FAN
Max Current : mA



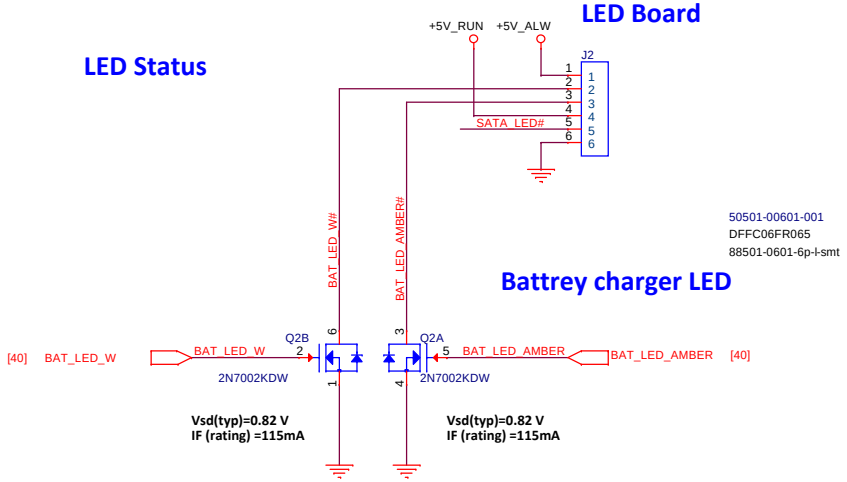


+V3.3_THERMAL
Max Current :mA

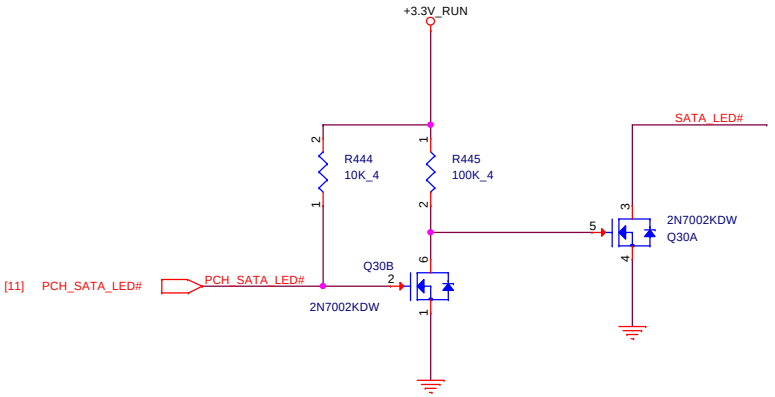
Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: Thermal GPU	Rev: A
Date: Monday, May 05, 2014	Sheet 45 of 58	

LED Board

LED Status



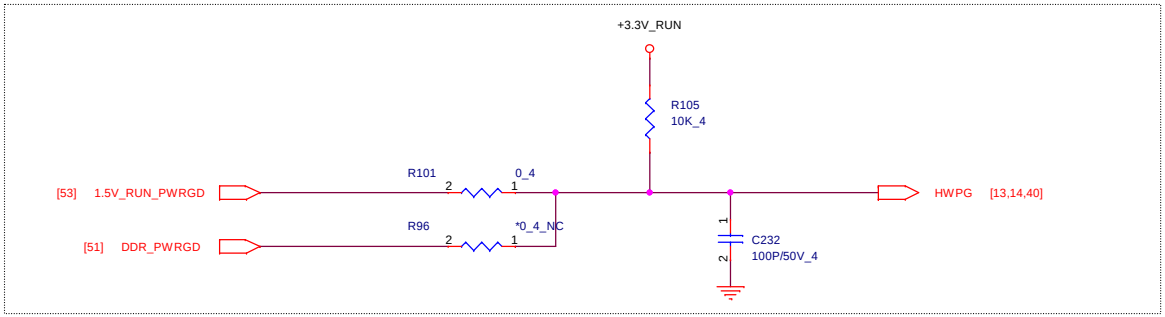
HDD activity LED.

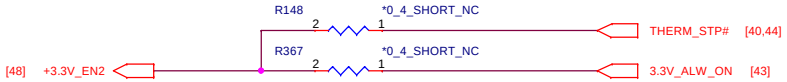


Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	LED	A
Date: Monday, May 05, 2014	Sheet 46 of 58	





Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	System Reset Circuit	A

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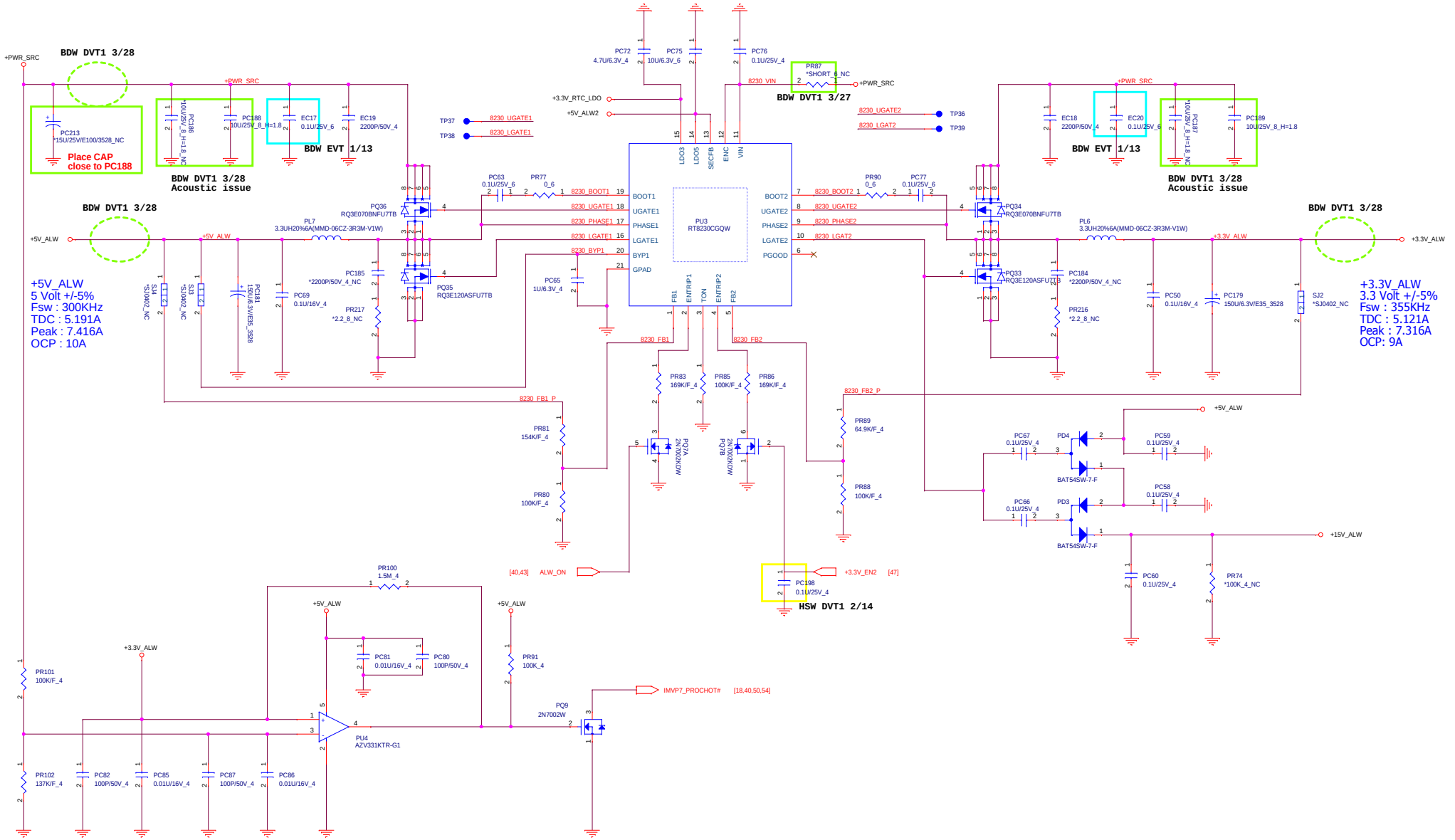
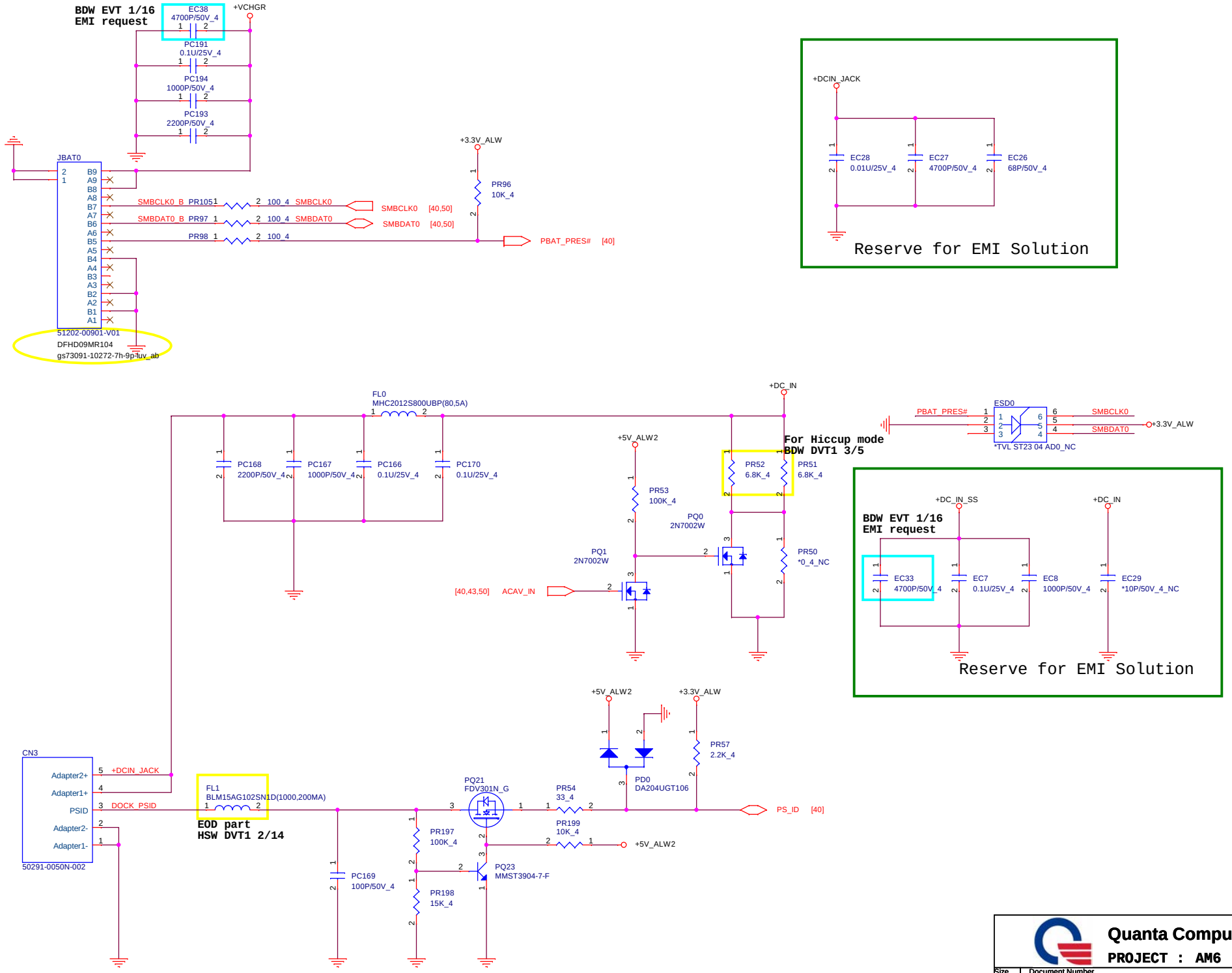


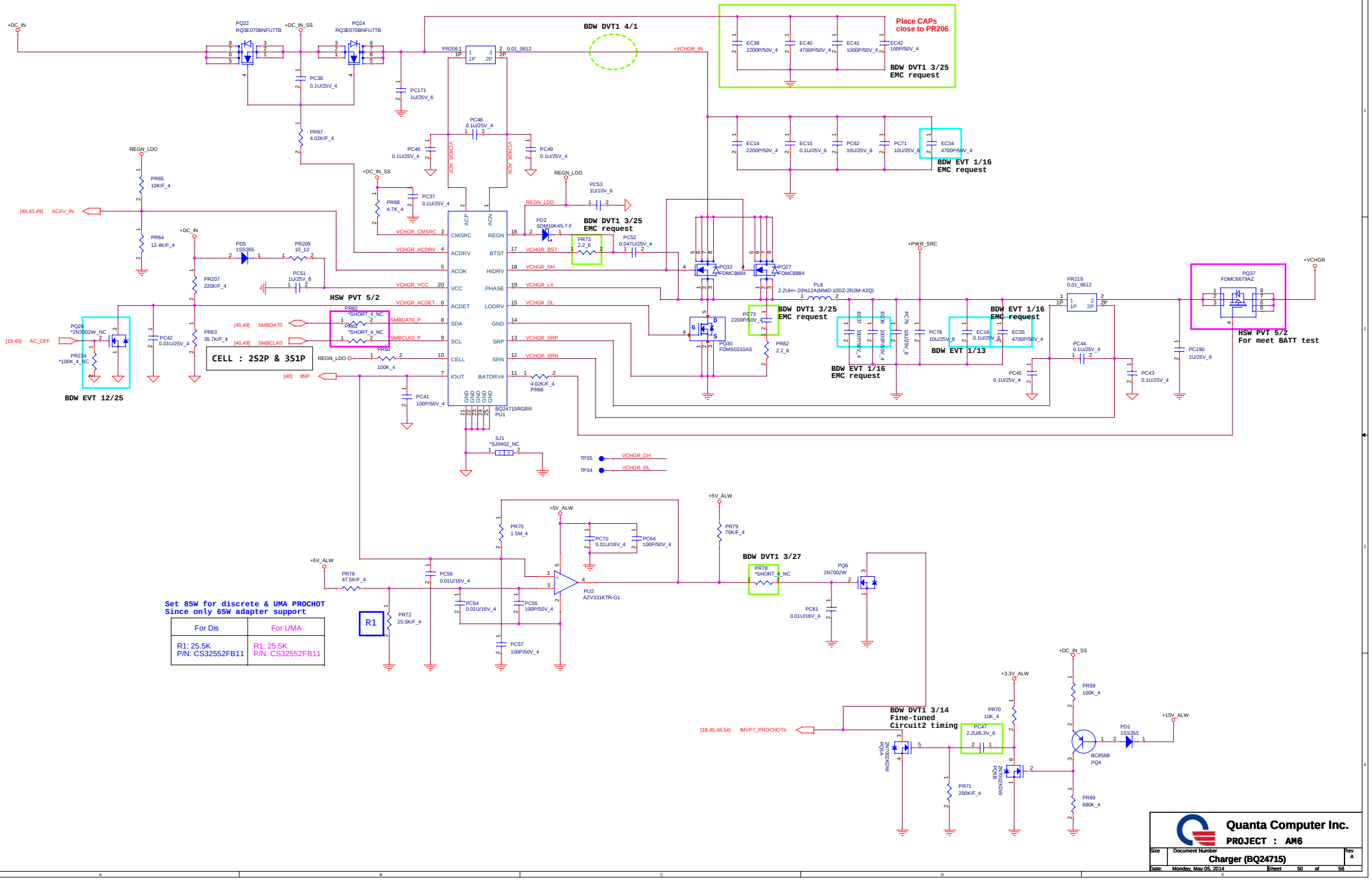
Quanta Computer Inc.
PROJECT : AM6

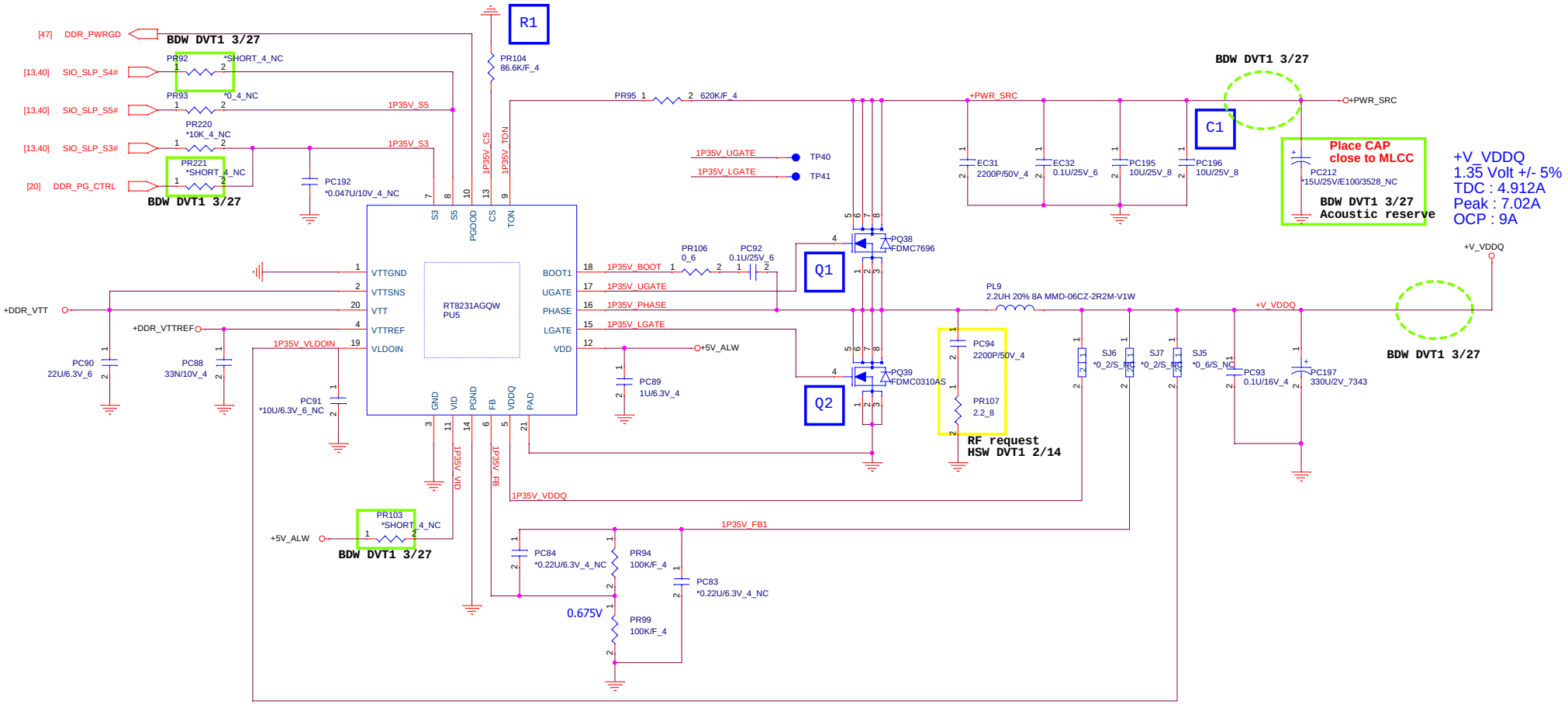
Size	Document Number	Rev
	3V/5V (RT8230CGQW)	A
Date: Monday, May 05, 2014	Sheet 48 of 58	



Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	DCin & Bat	A
Date: Monday, May 05, 2014	Sheet 49 of 58	





Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	1.35_DDR/0.675(RT8231)	A

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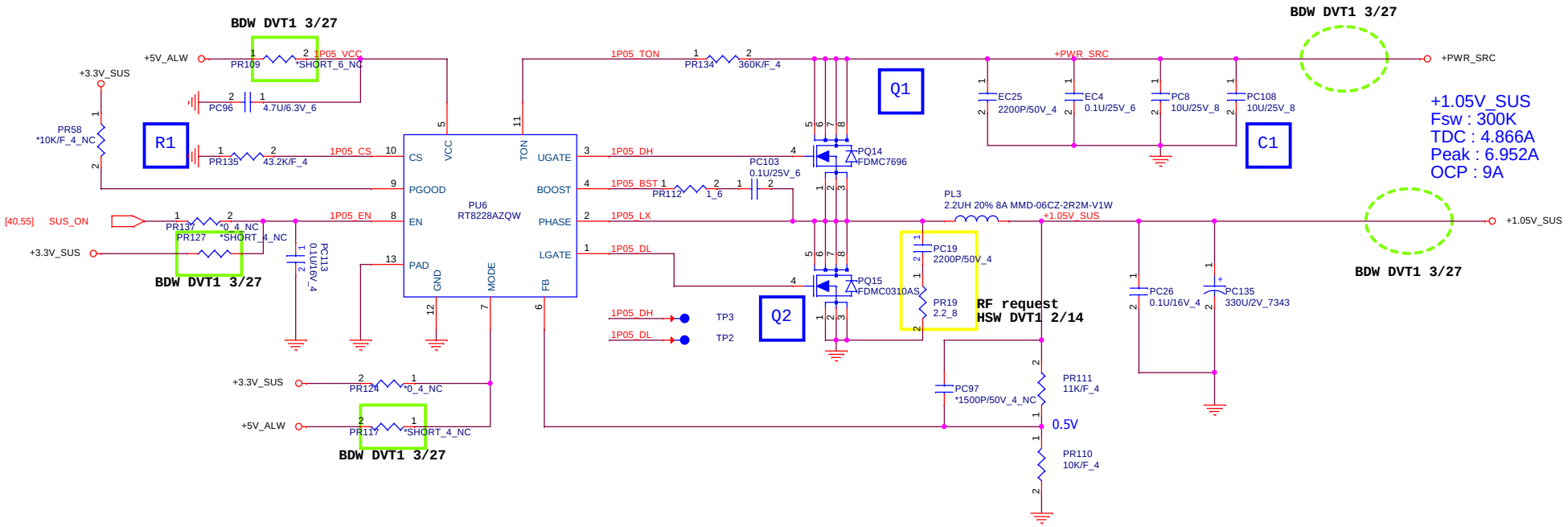

Quanta Computer Inc.

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Size	Document Number	Rev
	1.05V_SUS (RT8228AZ)	A

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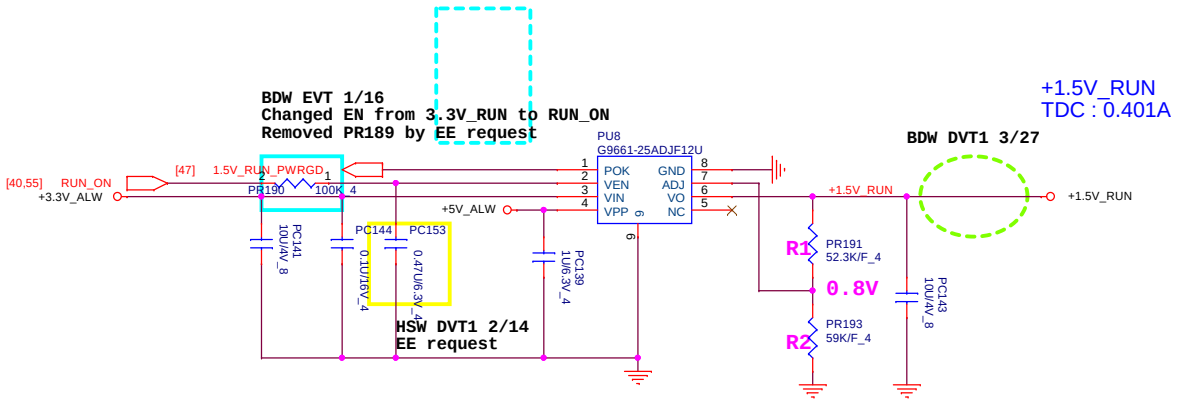

Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	+1.5V_RUN (G9661-25ADJF12U)	A

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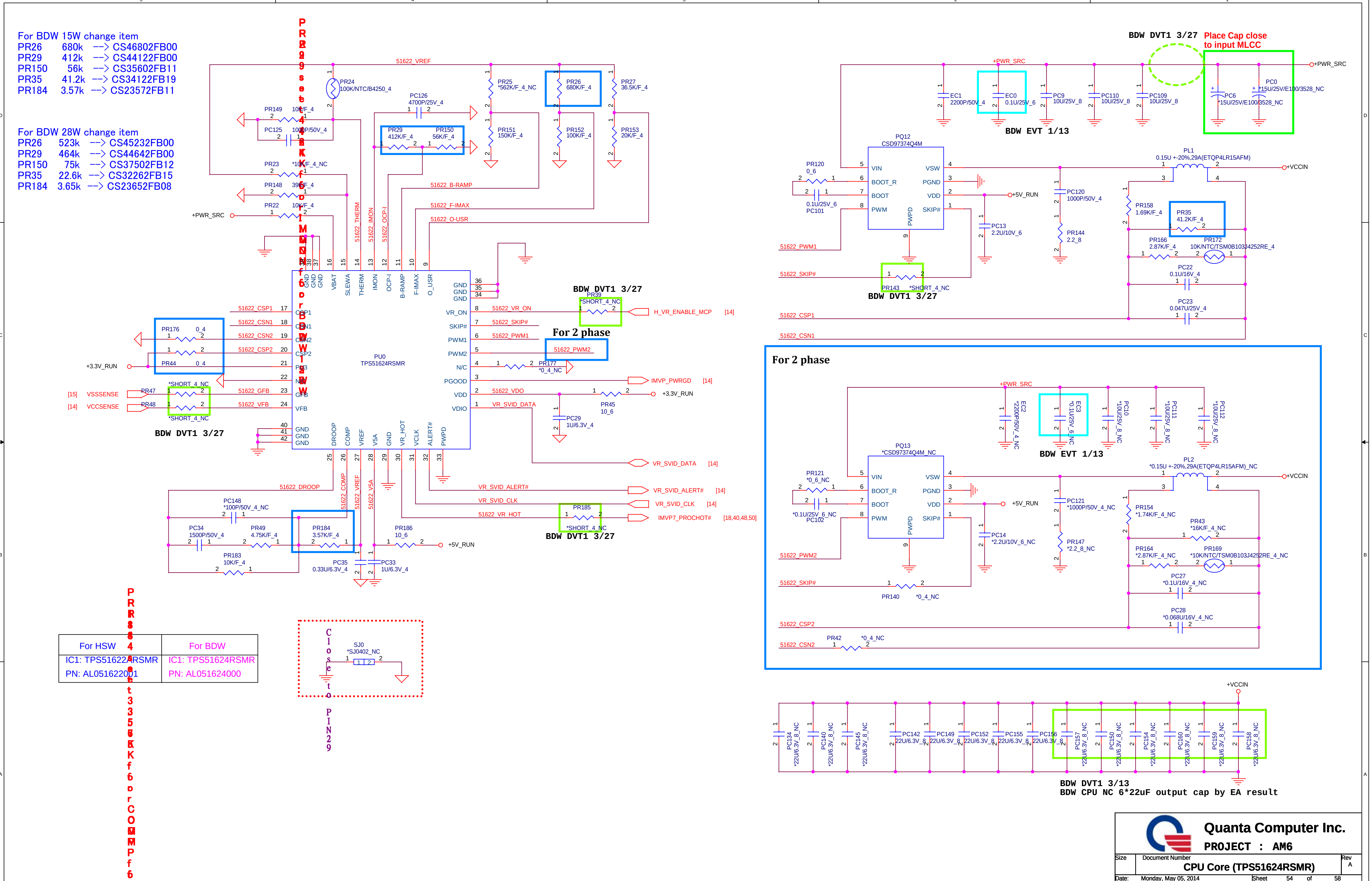
For BDW 15W change item

PR26	680k	-->	CS46802FB00
PR29	412k	-->	CS44122FB00
PR150	56k	-->	CS35602FB11
PR35	41.2k	-->	CS34122FB19
PR184	3.57k	-->	CS23572FB11

For BDW 28W change item

PR26	523k	-->	CS45232FB00
PR29	464k	-->	CS44642FB00
PR150	75k	-->	CS37502FB12
PR35	22.6k	-->	CS32262FB15
PR184	3.65k	-->	CS23652FB08



For HSW	For BDW
IC1: TPS51622ARSMR	IC1: TPS51624RSMR
PN: AL051622001	PN: AL051624000

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Size	Document Number	Rev
	CPU Core (TPS51624RSMR)	A

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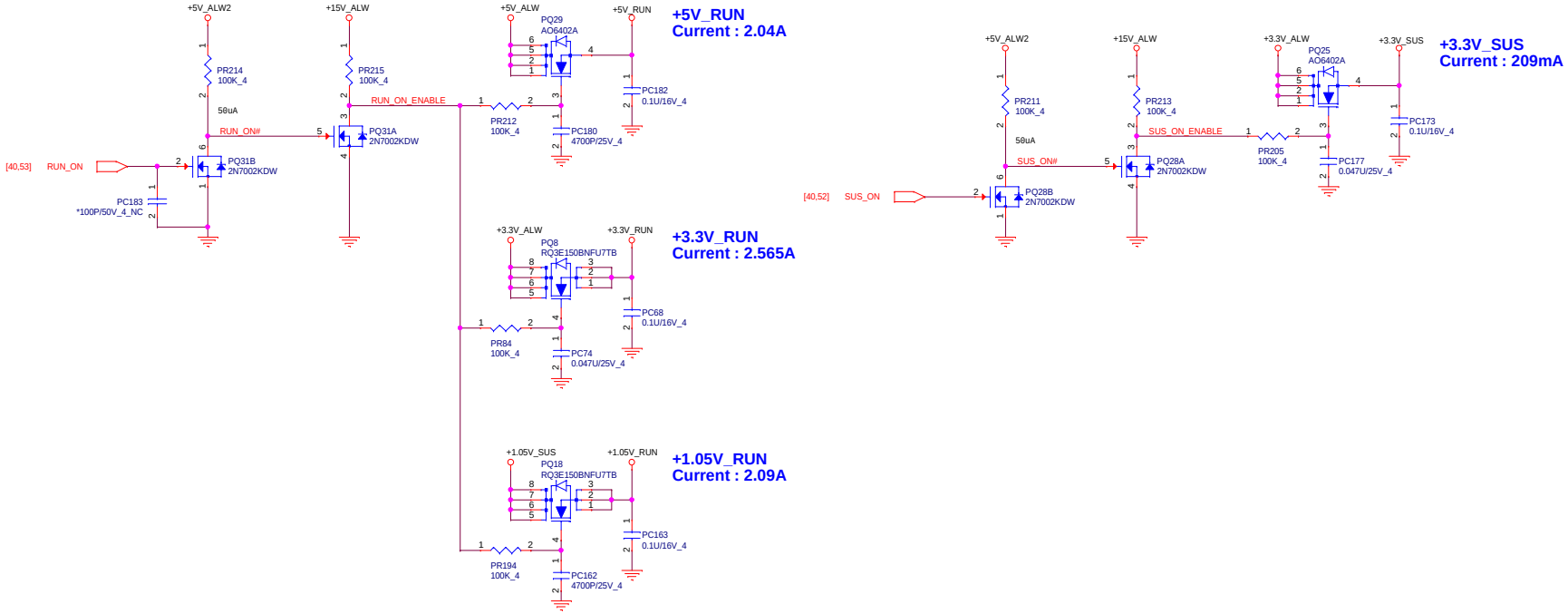

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Size	Document Number	Rev
	SUS_RUN Power Switch	A

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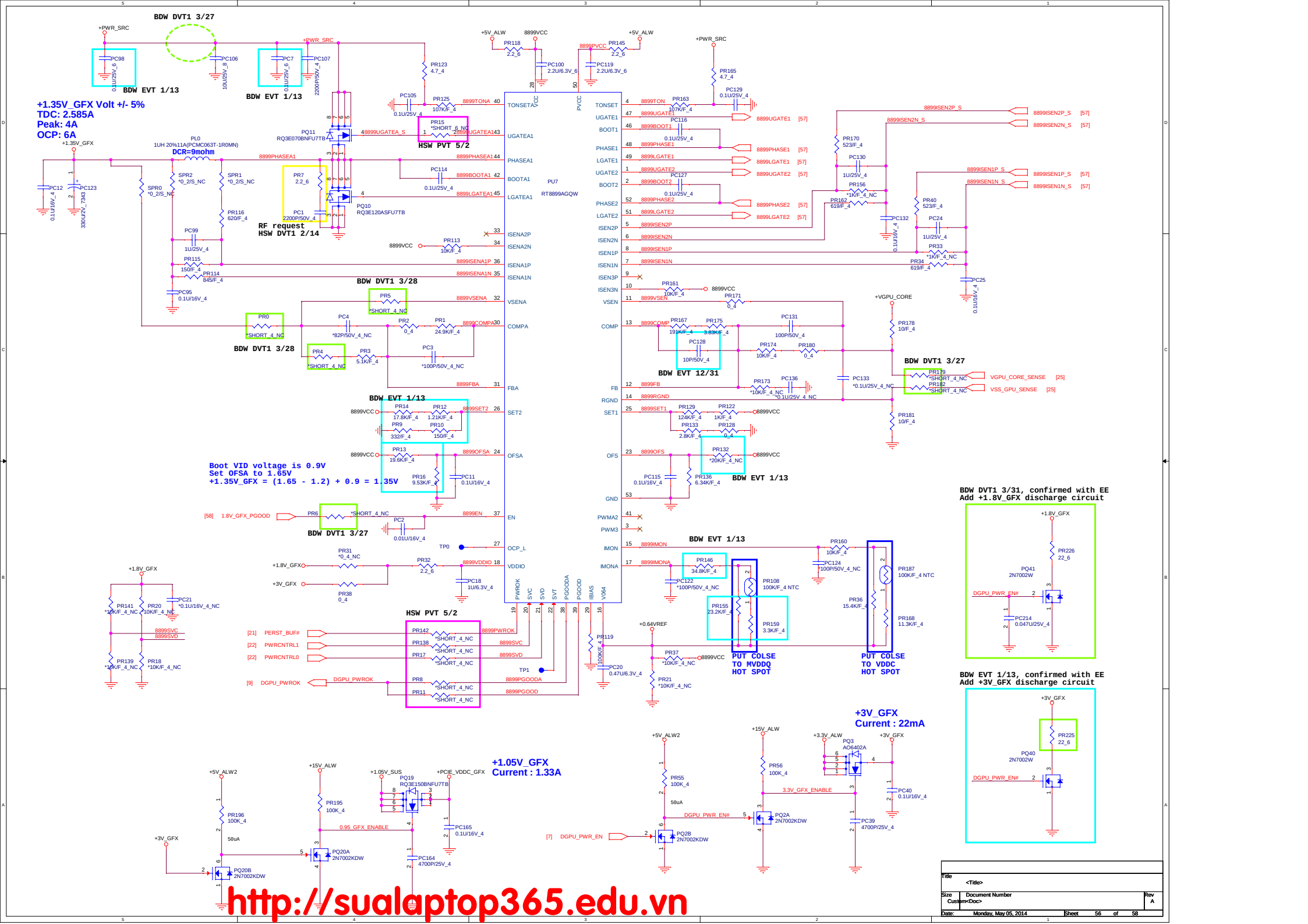
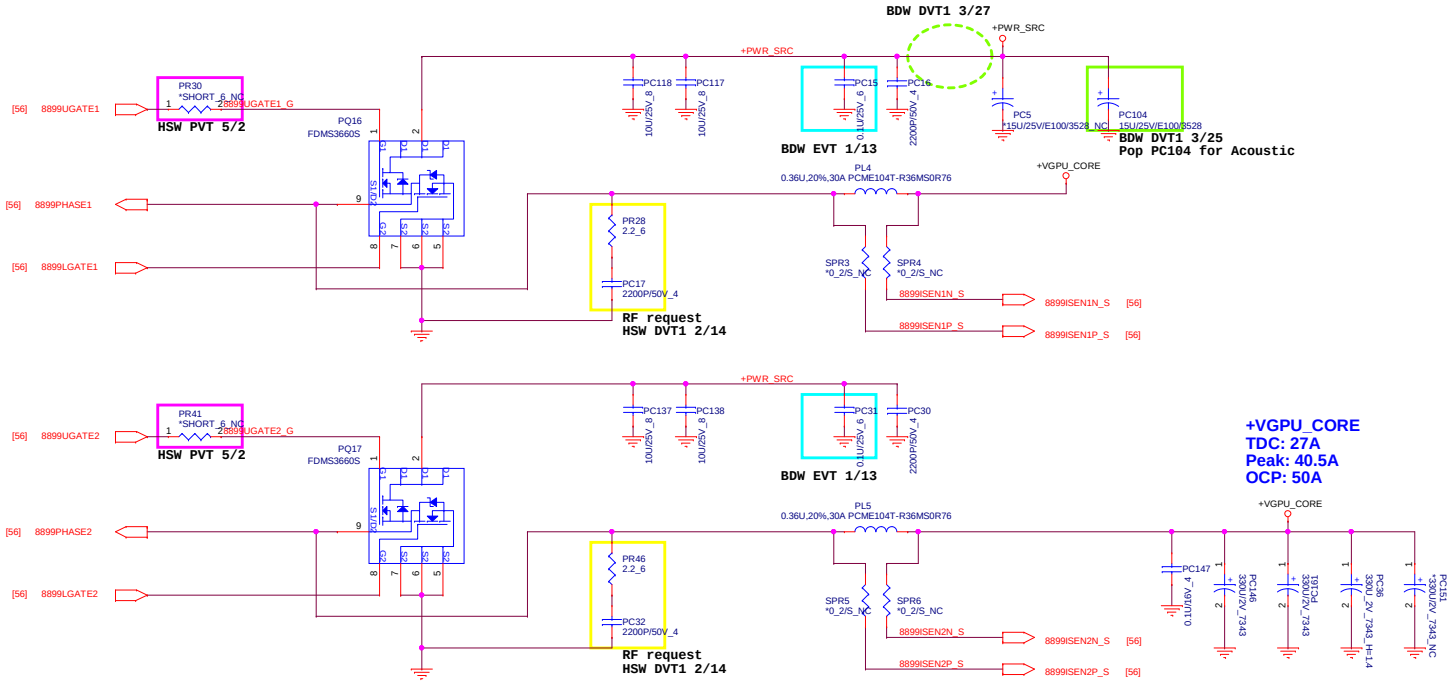

BDW DVT1 3/27
BDW EVT 1/13
+1.35V_GFX Volt +/- 5%
TDC: 2.585A
Peak: 4A
OCP: 6A
DCR=9mohm
RF request
HSW DVT1 2/14
HSW PVT 5/2
BDW DVT1 3/28
BDW EVT 12/31
Boot VID voltage is 0.9V
Set OFSA to 1.65V
+1.35V_GFX = (1.65 - 1.2) + 0.9 = 1.35V
PUT COLSE TO MVDDQ HOT SPOT
PUT COLSE TO VDDC HOT SPOT
BDW DVT1 3/31, confirmed with EE
Add +1.8V_GFX discharge circuit
BDW EVT 1/13, confirmed with EE
Add +3V_GFX discharge circuit
+3V_GFX Current : 22mA
+1.05V_GFX Current : 1.33A
http://sualaptop365.edu.vn



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Size	Document Number <Doc>	Rev A
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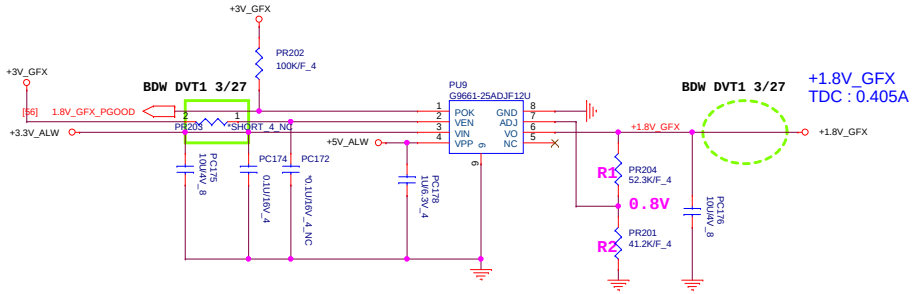

Title	<Title>	
Size	Document Number Custom<Doc>	Rev A
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