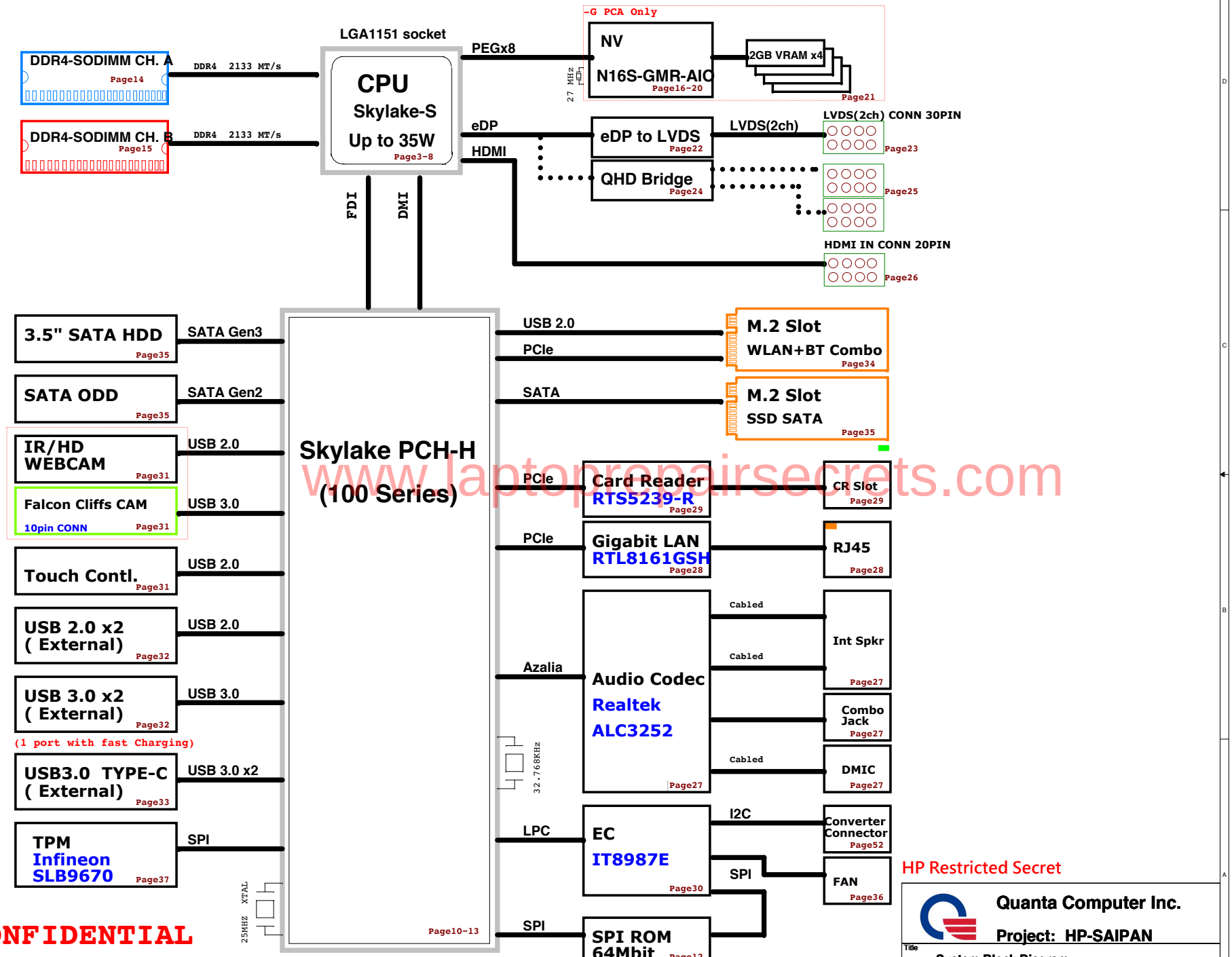
HP Saipan System Block Diagram

01



CONFIDENTIAL

HP Restricted Secret

Quanta Computer Inc.

Project: HP-SAIPAN

Title: System Block Diagram		
Size	Document Number: –	Rev: A
Page Modified: Thursday, December 17, 2015	Sheet 1 of 61	

Voltage Rails

Power Rail	Voltage	S0	S3	S4	S5	PCU	G3	Ctl Signal	
+RTC_VCC	3V	ON	ON	ON	ON	ON	ON		RTC Batt, PCH , EC
+VIN	19V	ON	ON	ON	ON	ON	ON	Adapter in	
+5V_ALW	5V	ON	ON	ON	ON	ON	ON	Int. LDO	LED
+3V_ALW	3.3V	ON	ON	ON	ON	ON	ON	Int. LDO	EC
+3V_AUX	3.3V	ON	ON	ON	ON	ON	OFF	LDO	System
+5V_S5	5V	ON	ON	ON	ON	OFF	OFF	S5_ON	PCH, USB, 3D WebCAM, Touch Panel, USB Charger
+3V_S5	3.3V	ON	ON	ON	ON	OFF	OFF	S5_ON	PCH, XDP, SPI flash ROM,NGFF LAN
+1.8V_S5	1.8V	ON	ON	ON	ON	OFF	OFF	S5_ON	PCH, XDP, NGFF LAN
+1V_S5	1.0V	ON	ON	ON	ON	OFF	OFF	PG_+1.8V_S5	PCH
+VCCST_VCCPLL	1.0V	ON	ON	OFF	OFF	OFF	OFF	S3_ON	CPU, PCH, XDP
+VDDQ	1.35V	ON	ON	OFF	OFF	OFF	OFF	S3_ON	DDR4, CPU DDR4 I/O
SMDDR_VTERM	0.75V	ON	ON	OFF	OFF	OFF	OFF	DDR_VTT_CNTL	DDR4
+5V	5V	ON	OFF	OFF	OFF	OFF	OFF	MAIN_ON1	HDD, ODD,Audio AMP,Panel VCC,FAN
+3V	3V	ON	OFF	OFF	OFF	OFF	OFF	MAIN_ON1	PCH, Audio, Card Reader, TPM, FHD CAM
+12V	12V	ON	OFF	OFF	OFF	OFF	OFF	MAIN_ON1	3.5" HDD
+VCCIO	0.95V	ON	OFF	OFF	OFF	OFF	OFF	PG_MAIN	CPU
+VCCSA	1.05V	ON	OFF	OFF	OFF	OFF	OFF	PG_+VCCIO	CPU
+VCCGT	0.65~1.3V	ON	OFF	OFF	OFF	OFF	OFF	VR_ON	CPU
+3.3V_VGA	3.3V	ON	OFF	OFF	OFF	OFF	OFF	EN_+3.3V_VGA	dGPU
+1.05V_VGA	1.05V	ON	OFF	OFF	OFF	OFF	OFF	PG_+3.3V_MAIN	dCPU
+VGA_CORE	0.8~1.15V	ON	OFF	OFF	OFF	OFF	OFF	PG_+3.3V_MAIN	dGPU
+1.35V_VGA	1.35V	ON	OFF	OFF	OFF	OFF	OFF	EN_+1.35V_VGA	dGPU, VRAM
+VCCCORE	0.65~1.3V	ON	OFF	OFF	OFF	OFF	OFF	VR_ON	CPU

Schematic "Value" Definition

Intel Platform Saipan-G and Saipan-U			DB/SI/PV Stage		MP		ALL STAGE	
By Value format	Description	Auto BOM Control	UMA	Discrete N16S GPU	UMA	Discrete N16S GPU	QHD PANEL	FHD PANEL
XX	Install	V	V	V	V	V		
*XX	Non-Install	V						
PROTO@XX	Install in Pre-production only	V	V	V				
MP@XX	Install in MP only	V			V	V		
DIS@xx	Install Discrete (DGPU) only	V		V		V		
UMA@xx	Install UMA	V	V		V			
QHD@xx	QHD panel	V	V	V	V	V	V	
FHD@xx	FHD panel	V	V	V	V	V		V

* Board ID and VRAM ID by manual control

HP Restricted Secret

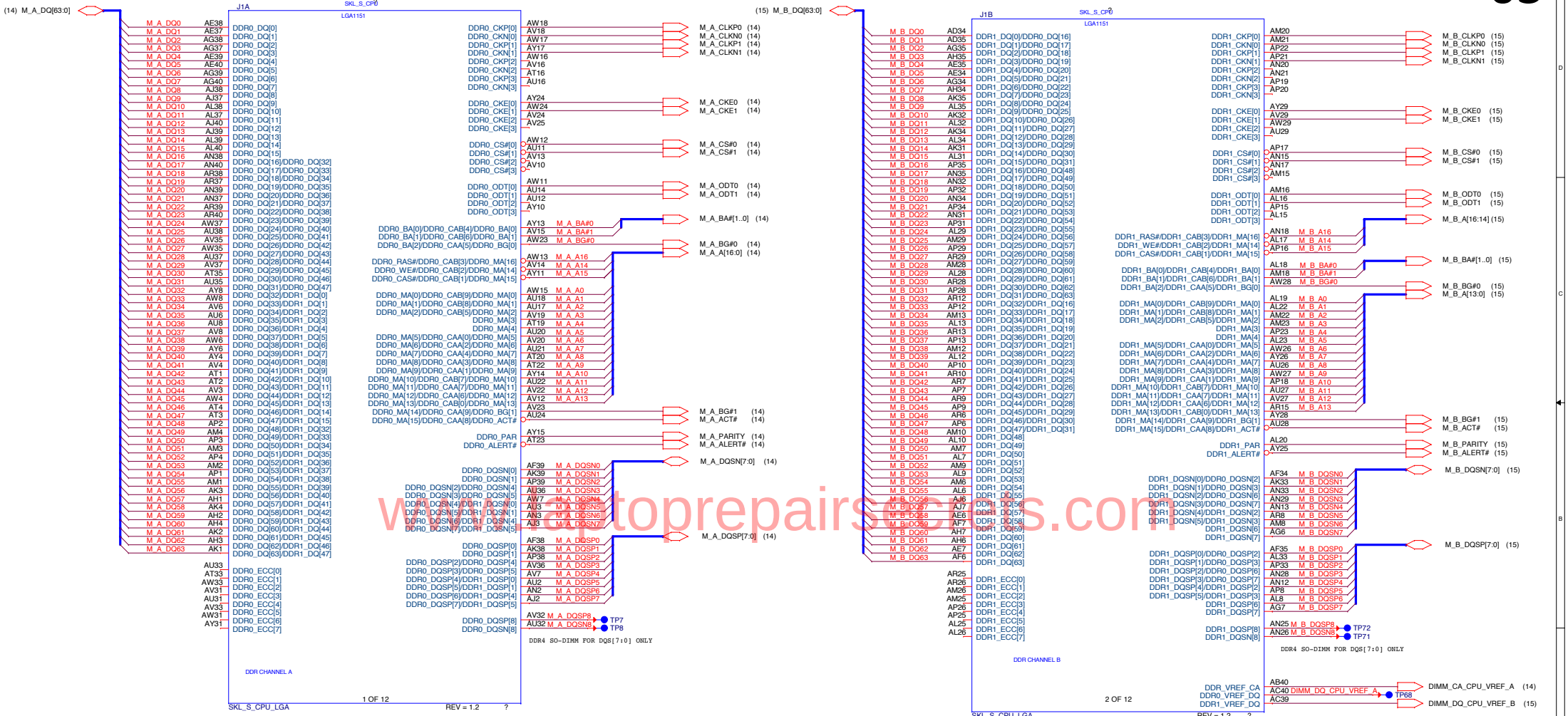
Quanta Computer Inc.

Project: HP-SAIPAN

Title: Power States & Value Definition

Size: | Document Number: -- | Rev: A

Page Modified: Thursday, December 17, 2015 | Sheet 2 of 61



HP Restricted Secret

Quanta Computer Inc.

Project: HP-SAIPAN

Title		
CPU_PEG/DISPLAY		
Size	Document Number	Rev
–		A
Page Modified: Thursday, December 17, 2015		Sheet 3 of 61

(7,38,42,47) +VCCIO

J1C SKL_S_CPU ?
LGA1151

(16) PEG_RXP0 B8 PEG_RXP[0] PEG_TXP[0] A5 PEG_TXP0 (16)
(16) PEG_RXN0 B7 PEG_RXN[0] PEG_TXN[0] A6 PEG_TXN0 (16)
(16) PEG_RXP1 C7 PEG_RXP[1] PEG_TXP[1] B4 PEG_TXP1 (16)
(16) PEG_RXN1 C6 PEG_RXN[1] PEG_TXN[1] B5 PEG_TXN1 (16)
(16) PEG_RXP2 D6 PEG_RXP[2] PEG_TXP[2] C3 PEG_TXP2 (16)
(16) PEG_RXN2 D5 PEG_RXN[2] PEG_TXN[2] C4 PEG_TXN2 (16)
(16) PEG_RXP3 E5 PEG_RXP[3] PEG_TXP[3] D2 PEG_TXP3 (16)
(16) PEG_RXN3 E4 PEG_RXN[3] PEG_TXN[3] D3 PEG_TXN3 (16)
F6 PEG_RXP[4] PEG_TXP[4] E1
F5 PEG_RXN[4] PEG_TXN[4] E2
G5 PEG_RXP[5] PEG_TXP[5] F2
G4 PEG_RXN[5] PEG_TXN[5] F3
H6 PEG_RXP[6] PEG_TXP[6] G1
H5 PEG_RXN[6] PEG_TXN[6] G2
J5 PEG_RXP[7] PEG_TXP[7] H2
J4 PEG_RXN[7] PEG_TXN[7] H3
K6 PEG_RXP[8] PEG_TXP[8] J1
K5 PEG_RXN[8] PEG_TXN[8] J2
L5 PEG_RXP[9] PEG_TXP[9] K2
L4 PEG_RXN[9] PEG_TXN[9] K3
M6 PEG_RXP[10] PEG_TXP[10] L1
M5 PEG_RXN[10] PEG_TXN[10] L2
N5 PEG_RXP[11] PEG_TXP[11] M2
N4 PEG_RXN[11] PEG_TXN[11] M3
P6 PEG_RXP[12] PEG_TXP[12] N1
P5 PEG_RXN[12] PEG_TXN[12] N2
R5 PEG_RXP[13] PEG_TXP[13] P2
R4 PEG_RXN[13] PEG_TXN[13] P3
T6 PEG_RXP[14] PEG_TXP[14] R2
T5 PEG_RXN[14] PEG_TXN[14] R1
U5 PEG_RXP[15] PEG_TXP[15] T2
U4 PEG_RXN[15] PEG_TXN[15] T3
L7 PEG_RCOMP

EC-DB-E02

EC-DB-E02

PEG_RCOMP
Trace length < 400 mils
Trace width = 12 mils
Trace spacing = 15 mils

+VCCIO
R57 24.9/F_4 PEG_RCOMP
PLACE INSIDE CPU CAVITY

(10) DMI_PCH_CPU_RXP0 Y3 DMI_RXP[0] DMI_TXP[0] AC2 DMI_CPU_PCH_TXP0 (10)
(10) DMI_PCH_CPU_RXN0 Y4 DMI_RXN[0] DMI_TXN[0] AC1 DMI_CPU_PCH_TXN0 (10)
(10) DMI_PCH_CPU_RXP1 AA4 DMI_RXP[1] DMI_TXP[1] AD3 DMI_CPU_PCH_TXP1 (10)
(10) DMI_PCH_CPU_RXN1 AA5 DMI_RXN[1] DMI_TXN[1] AD2 DMI_CPU_PCH_TXN1 (10)
(10) DMI_PCH_CPU_RXP2 AB4 DMI_RXP[2] DMI_TXP[2] AE2 DMI_CPU_PCH_TXP2 (10)
(10) DMI_PCH_CPU_RXN2 AB3 DMI_RXN[2] DMI_TXN[2] AE1 DMI_CPU_PCH_TXN2 (10)
(10) DMI_PCH_CPU_RXP3 AC4 DMI_RXP[3] DMI_TXP[3] AF2 DMI_CPU_PCH_TXP3 (10)
(10) DMI_PCH_CPU_RXN3 AC5 DMI_RXN[3] DMI_TXN[3] AF3 DMI_CPU_PCH_TXN3 (10)

3 OF 12
SKL_S_CPU_LGA REV = 1.2 ?

HDMI

(26) HDMI_TX2P C21 DDI1_TXP[0]
(26) HDMI_TX2N D21 DDI1_TXN[0]
(26) HDMI_TX1P D22 DDI1_TXP[1]
(26) HDMI_TX1N E22 DDI1_TXN[1]
(26) HDMI_TX0P B23 DDI1_TXP[2]
(26) HDMI_TX0N A23 DDI1_TXN[2]
(26) HDMI_CLKP C23 DDI1_TXP[3]
(26) HDMI_CLKN D23 DDI1_TXN[3]
B13 DDI1_AUXP
C13 DDI1_AUXN
B18 DDI2_TXP[0]
A18 DDI2_TXN[0]
D18 DDI2_TXP[1]
E18 DDI2_TXN[1]
C19 DDI2_TXP[2]
D19 DDI2_TXN[2]
D20 DDI2_TXP[3]
E20 DDI2_TXN[3]
A12 DDI2_AUXP
B12 DDI2_AUXN
B14 DDI3_TXP[0]
A14 DDI3_TXN[0]
C15 DDI3_TXP[1]
B15 DDI3_TXN[1]
B16 DDI3_TXP[2]
A16 DDI3_TXN[2]
C17 DDI3_TXP[3]
B17 DDI3_TXN[3]
B11 DDI3_AUXP
C11 DDI3_AUXN

J1D SKL_S_CPU ?
LGA1151

EDP_TXP[0] E10 DDID_TXDP0 (22)
EDP_TXN[0] D10 DDID_TXDN0 (22)
EDP_TXP[1] D9 DDID_TXDP1 (22)
EDP_TXN[1] C9 DDID_TXDN1 (22)
EDP_TXP[2] H10 DDID_TXDN2 (24)
EDP_TXN[2] G10 DDID_TXDP2 (24)
EDP_TXP[3] G9 DDID_TXDN3 (24)
EDP_TXN[3] F9 DDID_TXDP3 (24)
EDP_AUXP D12 EDP_AUXP (22)
EDP_AUXN E12 EDP_AUXN (22)
EDP_DISP_UTIL D14
EDP_RCOMP M9 EDP_COMP R59 24.9/F_4 +VCCIO
Place inside CPU cavity
PROC_AUDIO_CLK V3 AUD_CPU_BCLK AUD_CPU_BCLK (9)
PROC_AUDIO_SDI V2 AUD_CPU_SDO (9)
PROC_AUDIO_SDO U1 AUD_CPU_SDI_R

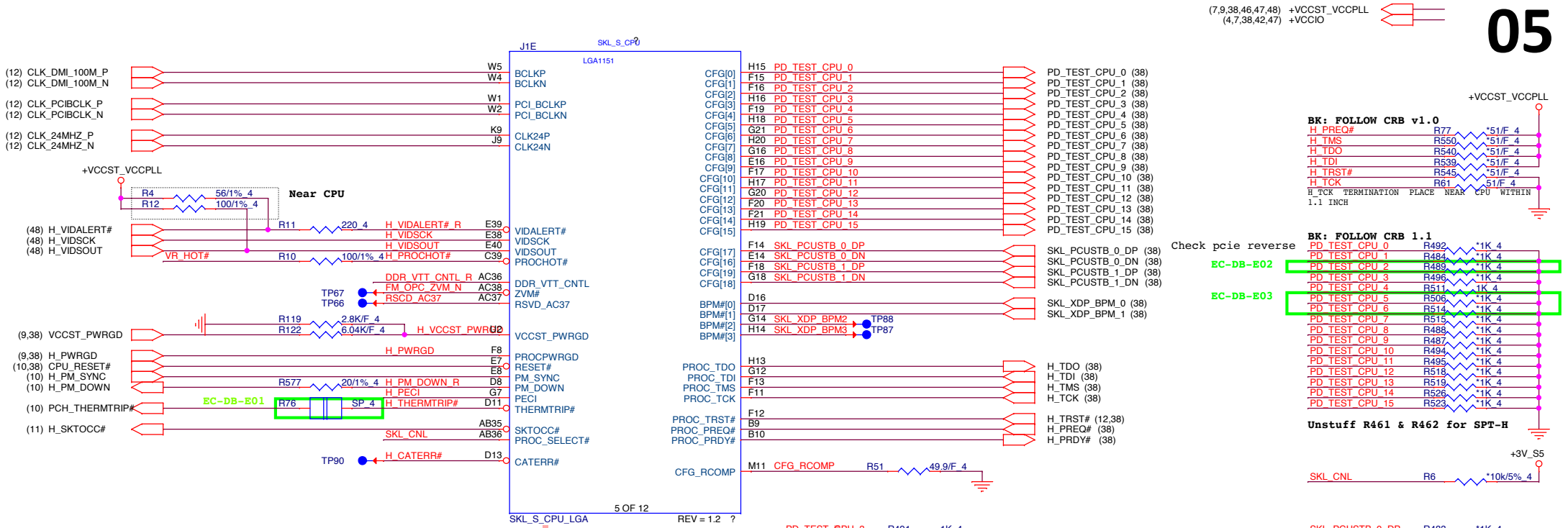
4 OF 12
SKL_S_CPU_LGA REV = 1.2 ?

AUD_CPU_SDI_R R121 20/1%_4 AUD_CPU_SDI (9)

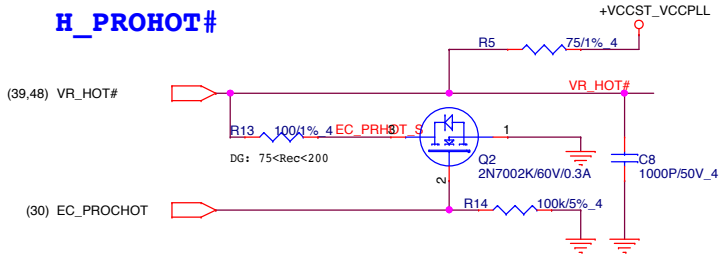
EMI reserved
AUD_CPU_BCLK C96 *10p/50V/NPO_4

Quanta Computer Inc.
Project: HP-SAIPAN

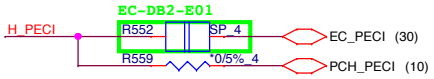
Title: CPU_PEG/DISPLAY
Size: Document Number: -- Rev: A
Page Modified: Thursday, December 17, 2015 Sheet 4 of 61



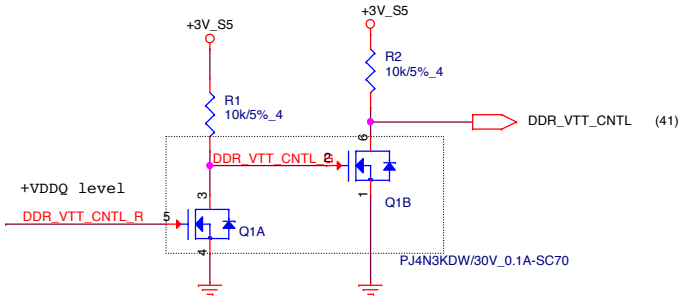
H_PROHOT#

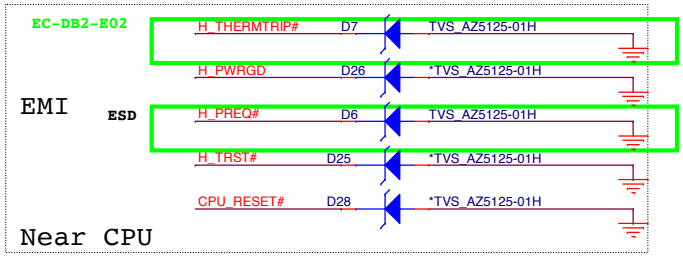


H_PECI



DDR_VTT_CNTL





HP Restricted Secret

Quanta Computer Inc.

Project: HP-SAIPAN

Title		
CPU MISC		
Size	Document Number	Rev
	--	A
Page Modified: Thursday, December 17, 2015	Sheet 5 of 61	

+VCCCPRE:
Icc (max) : 66A
Icc (PS2) : 35A

Decoupling Capacitors

+VCCCORE

EC-DB2-E03

PC329 DIS@330u/2V_7343
PC330 *DIS@330u/2V_7343

Place caps at top socket edge

+VCCCORE

C45 22U 6.3V X5R 0603
C323 22U 6.3V X5R 0603
C50 22U 6.3V X5R 0603
C329 22U 6.3V X5R 0603
C51 22U 6.3V X5R 0603
C360 22U 6.3V X5R 0603
C44 22U 6.3V X5R 0603
C362 22U 6.3V X5R 0603
C56 22U 6.3V X5R 0603
C42 22U 6.3V X5R 0603
C61 22U 6.3V X5R 0603
C58 22U 6.3V X5R 0603

Place all above caps on top side of CPU cavity

+VCCCORE

C43 22U 6.3V X5R 0603
C68 22U 6.3V X5R 0603
C57 22U 6.3V X5R 0603
C63 22U 6.3V X5R 0603
C59 22U 6.3V X5R 0603
C350 22U 6.3V X5R 0603
C46 22U 6.3V X5R 0603
C341 22U 6.3V X5R 0603
C60 22U 6.3V X5R 0603
C371 22U 6.3V X5R 0603

Place all below caps on bottom side near CPU socket

+VCCCORE

J1G SKL_S_CPU LGA1151

A25 A26 A27 A28 A29 A30 B25 B27 B29 B31 B32 B33 B34 B35 B36 B37 C25 C26 C27 C28 C29 C30 C32 C34 C36 D25 D27 D29 D31 D32 D33 D34 D35 D36 E24 E25 E26 E27 E28 E29 E30 E32 E34 E36 F23 F24 F25 F27 F29 F31 G30 G32 H22 H23 H25 H27 H29 H31 AJ11 AJ13 AJ15 AJ17 AJ19 AJ21 — VCC

H32 J21 F32 F33 F34 G23 G24 G25 G26 G27 G28 G29 J22 J23 J24 J25 J26 J27 J28 J29 J30 J31 K16 K18 K20 K21 K23 K25 K27 K29 K31 L14 L15 L16 L17 L18 L19 L20 L21 L22 L23 L24 L25 L26 L27 L28 L29 L30 M13 M14 M16 M18 M20 M22 M24 M26 M28 M30 AJ12 AJ14 AJ16 AJ18 AJ20 AJ22 — VCC

VCC_SENSE C38
VSS_SENSE D38

VCCCORE_SENSE (48)
VSSCORE_SENSE (48)

7 OF 12
SKL_S_CPU_LGA REV = 1.2 ?

+VCCCORE

+VCCCPRE:
Icc (max) : 40A
Icc (PS2) : 32A

+VCCGT

J1H SKL_S_CPU LGA1151

AA34 AA35 AA36 AA37 AA38 AB33 AB34 G36 G37 G38 G39 G40 H36 H38 H40 J36 J37 J38 J39 J40 K36 K38 K40 L34 L35 L36 L37 L38 L39 L40 M33 M34 M36 M38 M40 N34 N35 N36 N37 N38 N39 N40 P33 P34 P36 P38 P40 R34 R35 R36 R37 R38 R39 R40 T33 T34 T36 T38 T40 U34 U35 U36 U37 U38 U39 U40 V33 V34 V36 V38 V40 W34 W35 W36 W37 W38 Y33 Y34 Y36 Y38 — VCCGT

VCCGTX F35 G34 G35 H33 H34 J33 J35 K32 K34 L31 L33 M32 — VCCGTX

VCCGT_SENSE F39
VSSGT_SENSE F38

VCCGT_SENSE (48)
VSSGT_SENSE (48)

VCCGTX_SENSE F37
VSSGTX_SENSE F36

8 OF 12
SKL_S_CPU_LGA REV = 1.2 ?

VCCCORE_SENSE R8 *0/5%_4 VSSCORE_SENSE

+VCCCORE

VCCCORE_SENSE R7 100/1%_4
VSSCORE_SENSE R9 100/1%_4

DG: Near CPU

(7,47,48,49) +VCCCORE
(47,48,50) +VCCGT

Decoupling Capacitors

+VCCGT

C327 47u/6.3V_8
C26 47u/6.3V_8
C36 47u/6.3V_8
C347 47u/6.3V_8
C318 47u/6.3V_8
C35 47u/6.3V_8
C336 47u/6.3V_8

Place caps on top side socket cavity

+VCCGT

C335 47u/6.3V_8
C348 47u/6.3V_8
C32 47u/6.3V_8
C337 47u/6.3V_8
C326 47u/6.3V_8
C325 47u/6.3V_8
C27 47u/6.3V_8
C28 47u/6.3V_8
C37 47u/6.3V_8

Place caps on backside under socket cavity

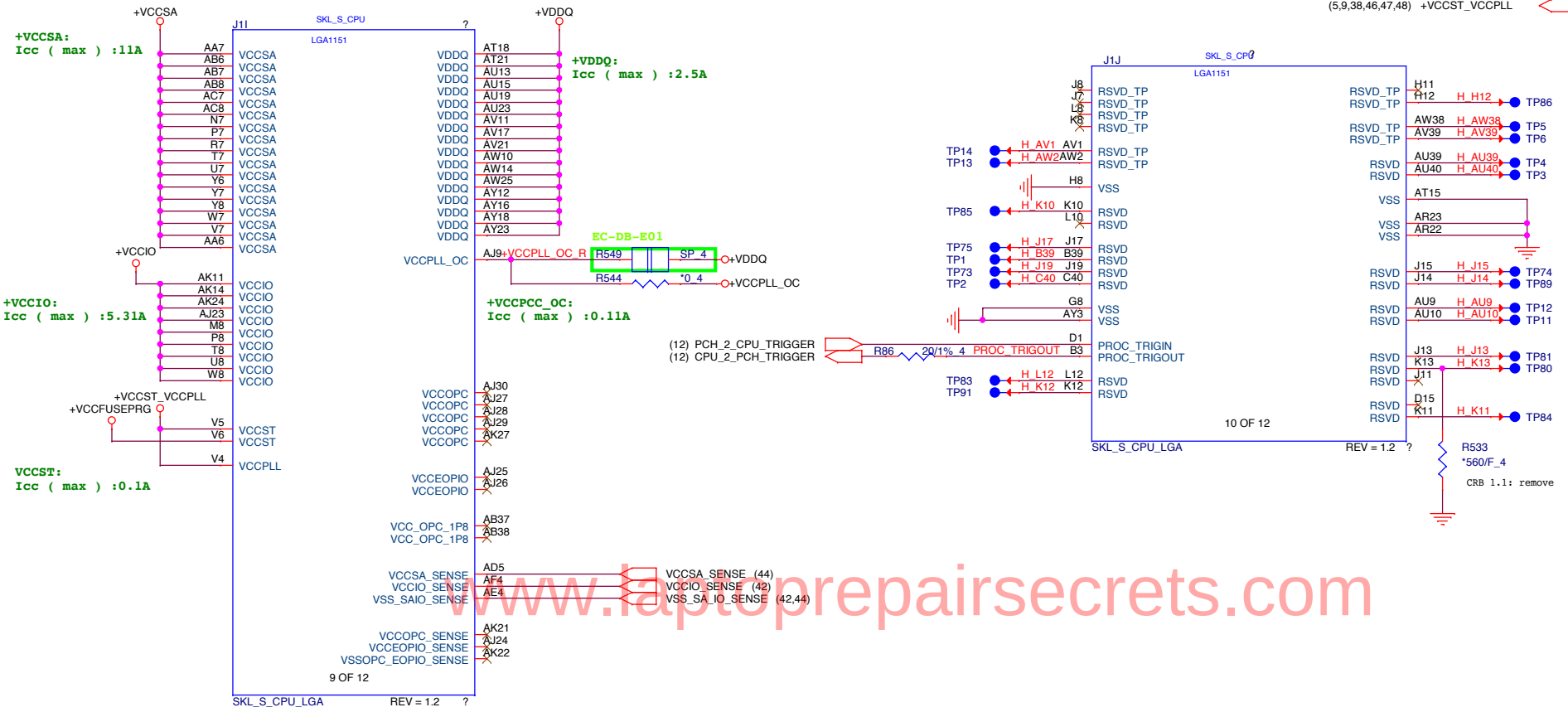
+VCCGT

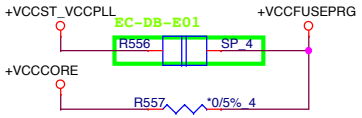
C30 47u/6.3V_8
C31 47u/6.3V_8
C320 47u/6.3V_8
C319 47u/6.3V_8

Quanta Computer Inc.
Project: HP-SAIPAN

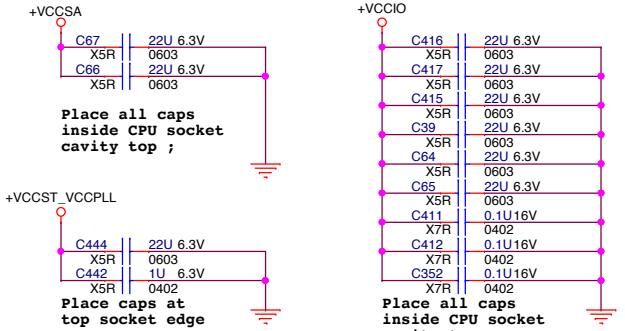
Title: CPU POWER
Size: Document Number: -- Rev: A
Page Modified: Thursday, December 17, 2015 Sheet 6 of 61

(44,47) +VCCSA
(9,14,15,41,46,47,55) +VDDQ
(4,38,42,47) +VCCIO
(5,9,38,46,47,48) +VCCST_VCCPLL

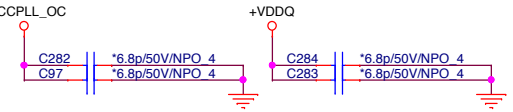




Decoupling Capacitors



RF

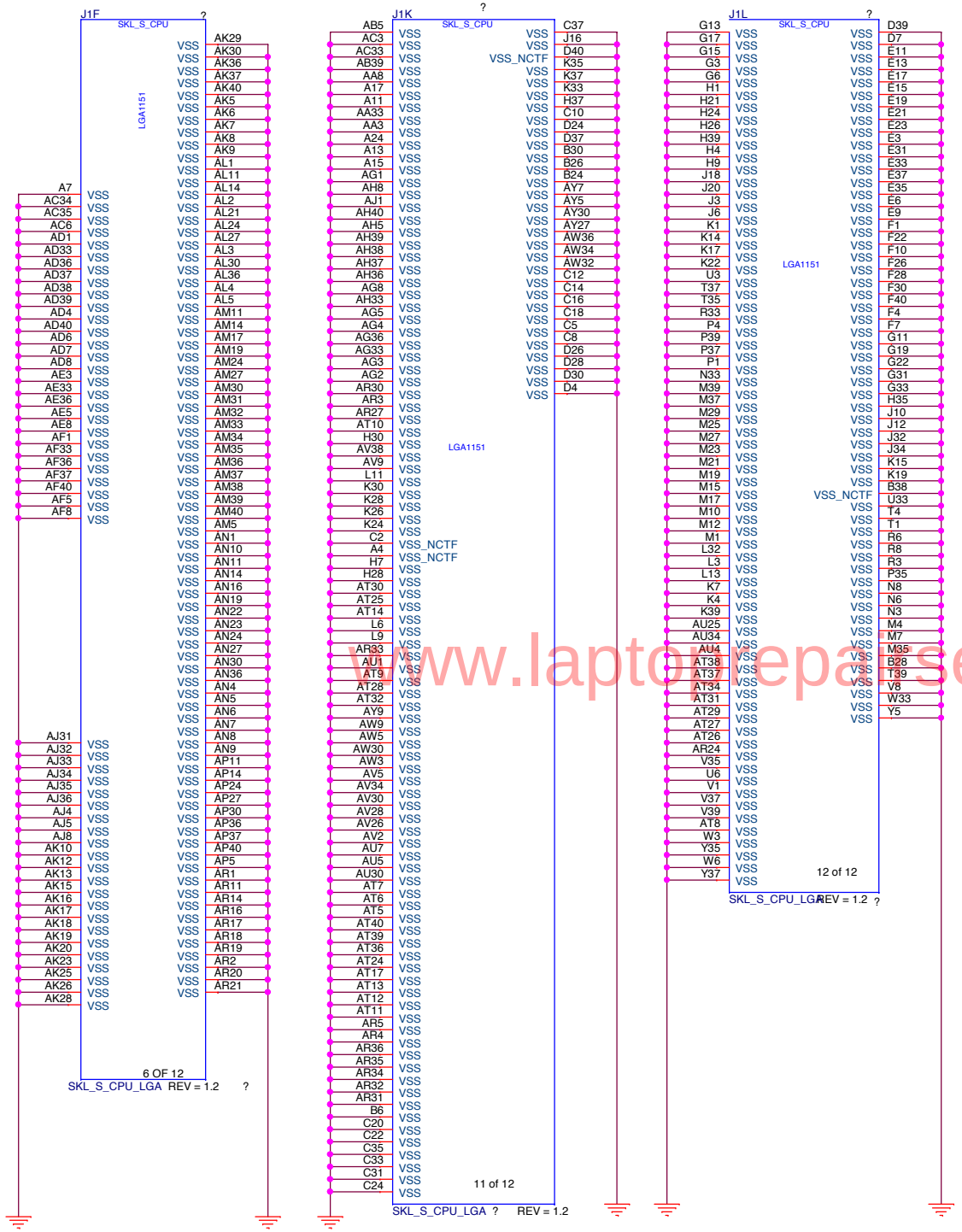


HP Restricted Secret

Quanta Computer Inc.

Project: HP-SAIPAN

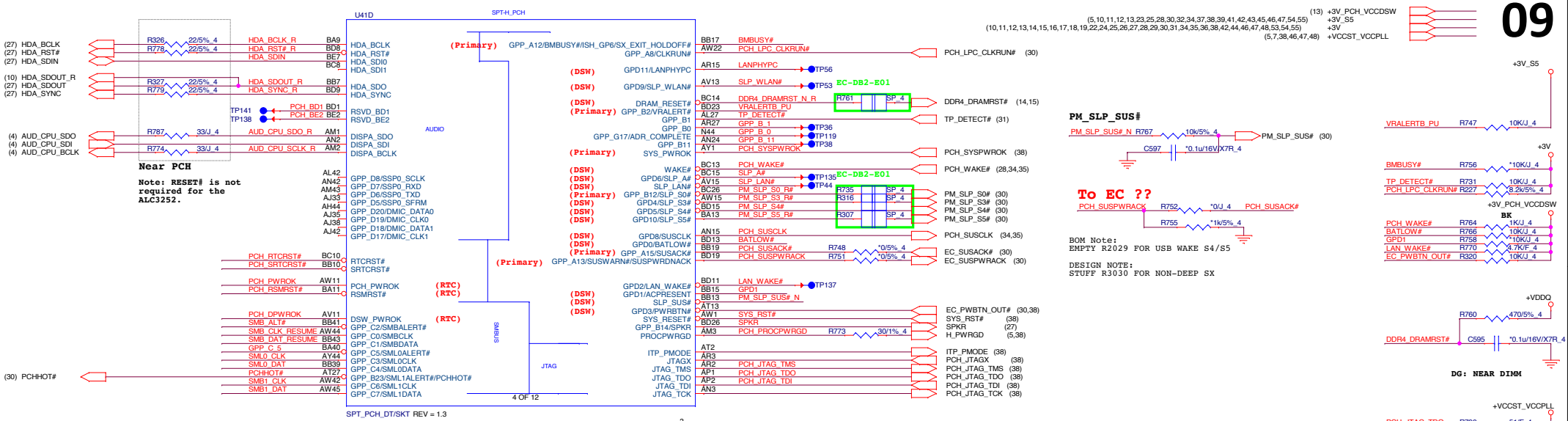
Title		
CPU POWER/RSVD		
Size	Document Number	Rev
	--	A
Page Modified: Thursday, December 17, 2015	Sheet 7 of 61	



Quanta Computer Inc.

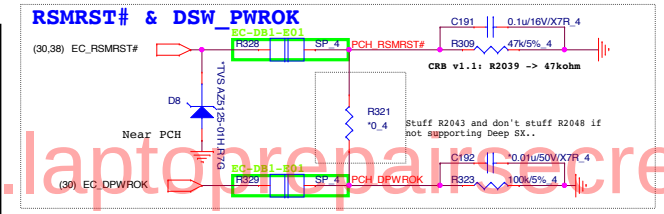
Project: HP-SAIPAN

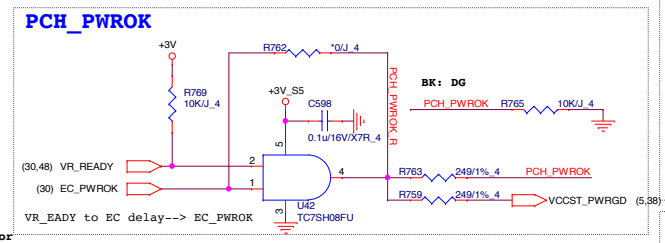
Title: CPU GND		
Size	Document Number: --	Rev: A
Page Modified: Thursday, December 17, 2015		Sheet 8 of 61

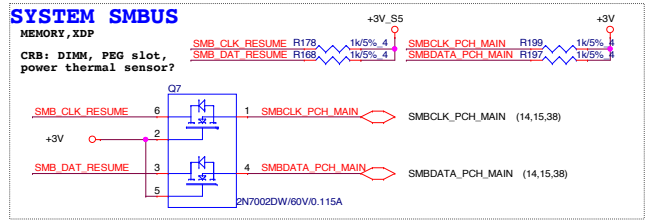


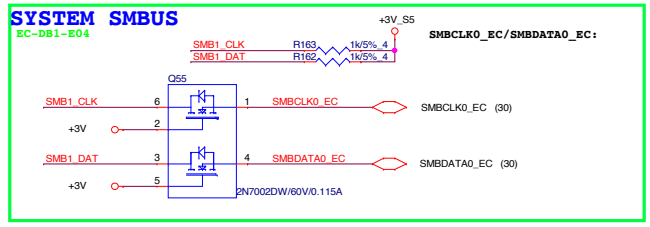
Strap Pin Table

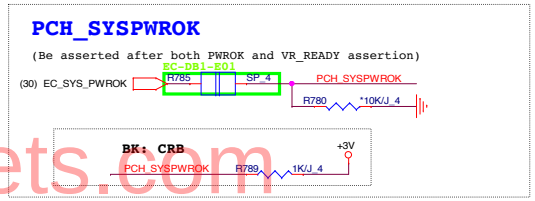
Configuration	Note
"Top swap" mode 0 = Disable, Default (Internal pull-down) 1 = Enable	
"No-Reboot" mode 0 = Disable, Default (Internal pull-down) 1 = Enable	CRB 1.0
Intel ME Crypto TLS cipher suite. 0 = Disable, Default (Internal pull-down) 1 = Enable	
BOOT SELECT STRAP 0 = SPI, Default (Internal pull-down) 1 = LPC	
ESPI/LPC SELECT STRAP (for EC) 0 = LPC (Default, int. pull-down) 1 = ESPI	
BOOT HALT 0 = Enable 1 = PCH has Internal weak pull-up	
JTAG ODT 0 = Enable 1 = PCH has Internal weak pull-up	
CONSENT STRAP 0 = Consent strap is enabled 1 = PCH has Internal weak pull-up	
PERSONALITY STRAP 0 = Enable 1 = PCH has Internal weak pull-up	pull down is needed for pre-ES1/ES1 samples
0 = PCH has Internal weak pull-down 1 = EXI boot stall bypass is enabled	150K PU NEEDED TO DISABLE EXI BOOT STALL BYPASS
SECRUITY MEASURES. 0 = Enable, Defualt (Internal weak pull-down) 1 = Disable. Flash Descriptor Security overrided, pull up for debug only.	
ESPI FLASH SHARING MODE 0 = Master (Internal weak pull-down) 1 = Slave	
DFX TEST MODE XTAL input is single ended if sampled low else differential	
TEST SETUP MENU 0 = Test setup menu enabled 1 = Disabled (Default)	
SV ADVANCE MENU TABLE 0 = SV ADVANCE MENU 1 = Normal Menu (Default)	

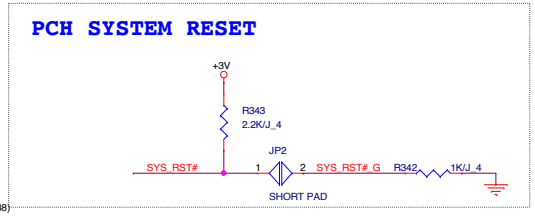


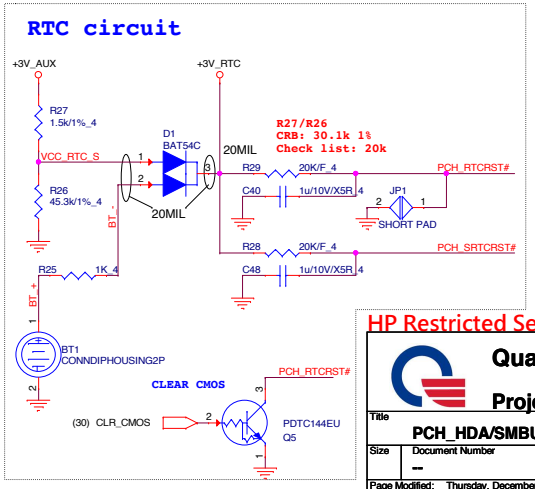


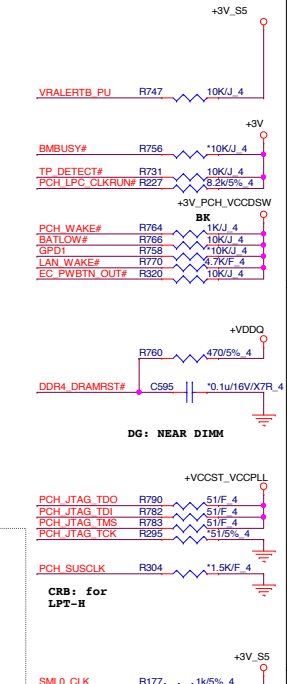












HP Restricted Secret

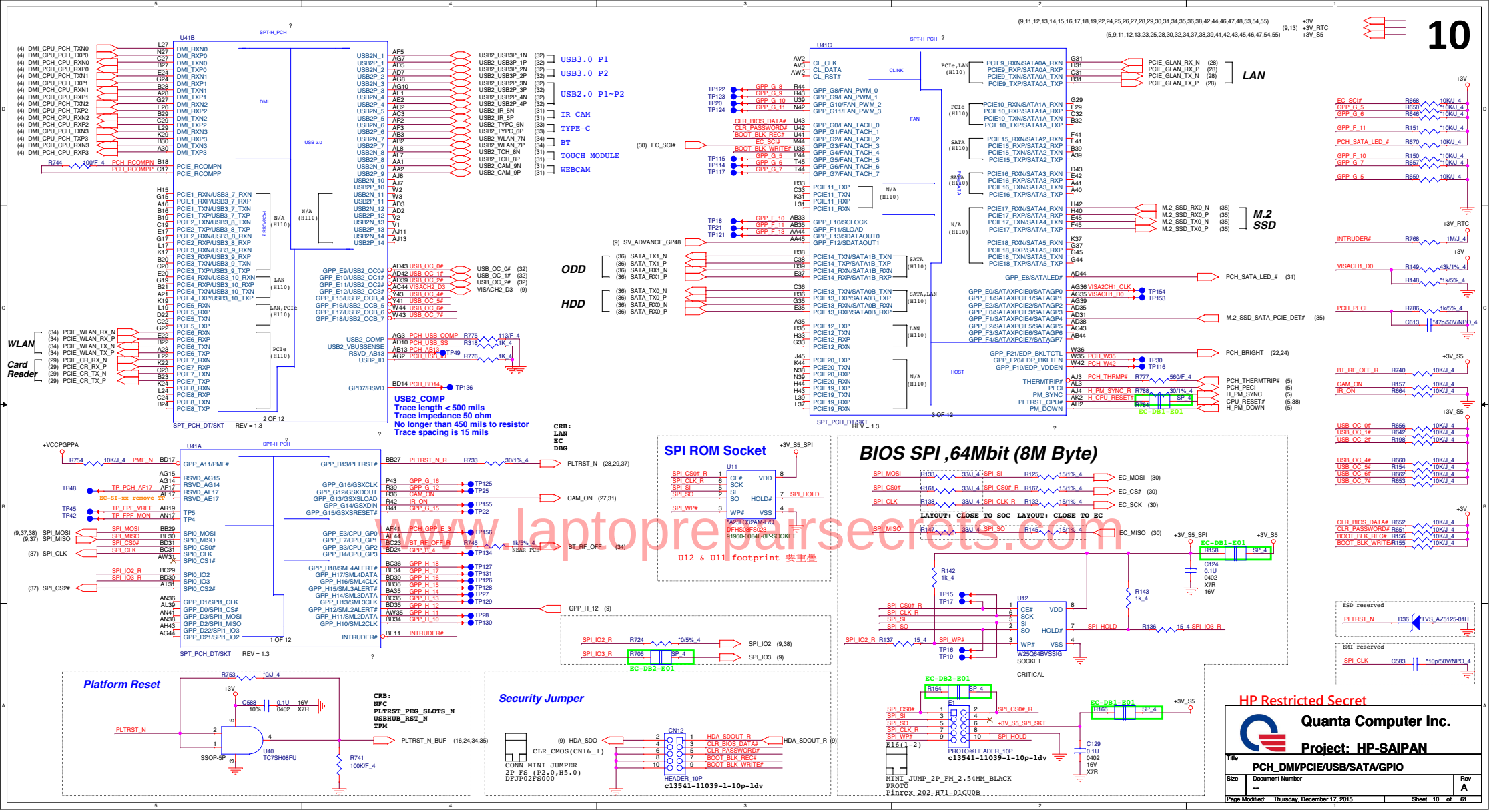
Quanta Computer Inc.

Project: HP-SAIPAN

Title: PCH_HDA/SMBUS/MISC

Size	Document Number	Rev
	--	A

Page Modified: Thursday, December 17, 2015 | Sheet 9 of 61



HP Restricted Secret

Quanta Computer Inc.

Project: HP-SAIPAN

Title	PCH_DMI/PCIE/USB/SATA/GPIO	
Size	Document Number	Rev
	--	A
Page Modified: Thursday, December 17, 2015	Sheet 10 of 61	

(9,10,12,13,14,15,16,17,18,19,22,24,25,26,27,28,29,30,31,34,35,36,38,42,44,46,47,48,53,54,55) +3V
(5,9,10,12,13,23,25,28,30,32,34,37,38,39,41,42,43,45,46,47,54,55) +3V_S5

USB PORT
(32) USB3_TXN1
(32) USB3_TXP1
(32) USB3_RXN1
(32) USB3_RXP1

USB PORT
(32) USB3_TXN2
(32) USB3_TXP2
(32) USB3_RXN2
(32) USB3_RXP2

TYPE-C_1
(33) USB3_TYPC_TX5N
(33) USB3_TYPC_TX5P
(33) USB3_TYPC_RX5N
(33) USB3_TYPC_RX5P

TYPE-C_2
(33) USB3_TYPC_TX3P
(33) USB3_TYPC_TX3N
(33) USB3_TYPC_RX3P
(33) USB3_TYPC_RX3N

3D CAM
(31) USB3_CAM_TX4P
(31) USB3_CAM_TX4N
(31) USB3_CAM_RX4P
(31) USB3_CAM_RX4N

U41F — SPT-H_PCH

C11	USB3_1_TXN	
B11	USB3_1_TXP	
B7	USB3_1_RXN	
A7	USB3_1_RXP	
B12	USB3_2_TXN/SSIC_1_TXN	
A12	USB3_2_TXP/SSIC_1_TXP	
C8	USB3_2_RXN/SSIC_1_RXN	
B8	USB3_2_RXP/SSIC_1_RXP	
B15	USB3_6_TXN	N/A (H110)
C15	USB3_6_TXP	
K15	USB3_6_RXN	
K13	USB3_6_RXP	
B14	USB3_5_TXN	
C14	USB3_5_TXP	
G13	USB3_5_RXN	
H13	USB3_5_RXP	
D13	USB3_3_TXP/SSIC_2_TXP	
C13	USB3_3_TXN/SSIC_2_TXN	
A9	USB3_3_RXP/SSIC_2_RXP	
B10	USB3_3_RXN/SSIC_2_RXN	
B13	USB3_4_TXP	USB3 (H110)
A14	USB3_4_TXN	
G11	USB3_4_RXP	
E11	USB3_4_RXN	

LPC/eSPI · USB3 · SATA

AT22	GPP_A1/LAD0/ESPI_IO0	F_LAD0 (30,34,37)	
AV22	GPP_A2/LAD1/ESPI_IO1	F_LAD1 (30,34,37)	
AT19	GPP_A3/LAD2/ESPI_IO2	F_LAD2 (30,34,37)	
BD16	GPP_A4/LAD3/ESPI_IO3	F_LAD3 (30,34,37)	
BE16	GPP_A5/LFRAME#/ESPI_CS#	L_FRAME# (30,34,37)	
BA17	GPP_A6/SERIRQ	SERIRQ (30,37)	
AW17	GPP_A7/PIRQA#/ESPI_ALERT0#	LPC_PIRQ → TP47	
AT17	GPP_A0/RCIN#/ESPI_ALERT1#	EC_KBRST# (30)	
BC18	GPP_A14/SUS_STAT#/ESPI_RESET#	EC_LPCPD# (30)	
BC17	GPP_A9/CLKOUT_LPC0/ESPI_CLK	CLKOUT_LPC0 R757 22_4	CK_24M_EC (30)
AV19	GPP_A10/CLKOUT_LPC1	CLKOUT_LPC1 R228 22_4	CK_24M_LPC (37)
		R226 22_4	CK_24M_DEBUG (34)
M45	GPP_G19/SMI#		PCH_SMI# (37)
N43	GPP_G18/NMI#	2X4_PWRDET → TP120	EC-DB2-E04
AE45	GPP_E6/DEVSLP2		
AG43	GPP_E5/DEVSLP1		
AG42	GPP_E4/DEVSLP0	PCH_GPP_E_4 → TP157	
AB39	GPP_F9/DEVSLP7	HD_3D_DET	
AB36	GPP_F8/DEVSLP6		DGPU_EVENT# (19)
AB43	GPP_F7/DEVSLP5		DGPU_PWROK (16,18)
AB42	GPP_F6/DEVSLP4	SSD_SATA_DEVSLP	SSD_SATA_DEVSLP (35)
AB41	GPP_F5/DEVSLP3	PCH_CODEC_IRQ → TP24	

6 OF 12
SPT_PCH_DT/SKT REV = 1.3

3D camera	1
HD camera	0

+3V
2X4_PWRDET R661 *10K/J_4
CAM_DET# R140 10K/J_4
DMIC_DET# R678 10K/J_4

+3V
EC_KBRST# R294 10K/J_4
SERIRQ R286 10K/J_4
PCH_SMI# R672 10K/J_4
R671 *10K/J_4

+3V
HD_3D_DET R128 *10K/J_4
R127 10K/J_4

+3V_S5
LPC_PIRQ R293 10K/J_4

CRB: Connect to +3V_S5 directly

SERIRQ & LPC_PIRQ
Note: An external pull-up is required

+3V_S5
SPI_TPM_PIRQ R153 8.2k/5% 4

+3V
DGPU_PLTRST_N R152 10K/J_4
EC_SMI# R341 10K/J_4

U41E — SPT-H_PCH

(26) HDMI_HPD
(30) EC_SMI#
R336 SP_4 EC_SMI#_PCH
EC_DB2_E01
(22,24) DDPD_HPD

AW4	GPP_I0/DDPB_HPD0	GPP_I7/DDPC_CTRLCLK	BB3
AY2	GPP_I1/DDPC_HPD1	GPP_I8/DDPC_CTRLDATA	BD6
AV4	GPP_I2/DDPD_HPD2	GPP_I5/DDPB_CTRLCLK	BA5 DDPB_CTRLCLK
BA4	GPP_I3/DDPE_HPD3	GPP_I6/DDPB_CTRLDATA	BC4 DDPB_CTRLDATA
BD7	GPP_I4/EDP_HPD	GPP_I9/DDPD_CTRLCLK	BE5
	Active high	GPP_I10/DDPD_CTRLDATA	BE6
		GPP_F14	Y44 CAM_DET#
		GPP_F23	V44 DGPU_PLTRST_N
		GPP_F22	W39
		GPP_G23	L43
		GPP_G22	L44
		GPP_G21	U35
		GPP_G20	R35
		GPP_H23	BD36 DMIC_DET#

5 OF 12
SPT_PCH_DT/SKT REV = 1.3

DDPB_CTRLCLK (26)
DDPB_CTRLDATA (26)
H_SKTOCC# (5)
CAM_DET# (31)
DGPU_PLTRST_N (16)
CAM_FW_UPDATE# (31)
EN_DGPU_PWR# (54)
SPI_TPM_PIRQ (37)
TEST_SETUP_MENU (9)
DMIC_DET# (31)

H/W STRAPS:
DDPB_CTRLDATA: (pull up at HDMI page)
0= Port B is not detected. Default, Internal PD
1= Port B is detected.

DGPU_HOLD_RST#
0 = Keep dGPU in reset
1 = Reset is released. This action taken 100 ms after DGPU_PWROK to ensure clock is stable.

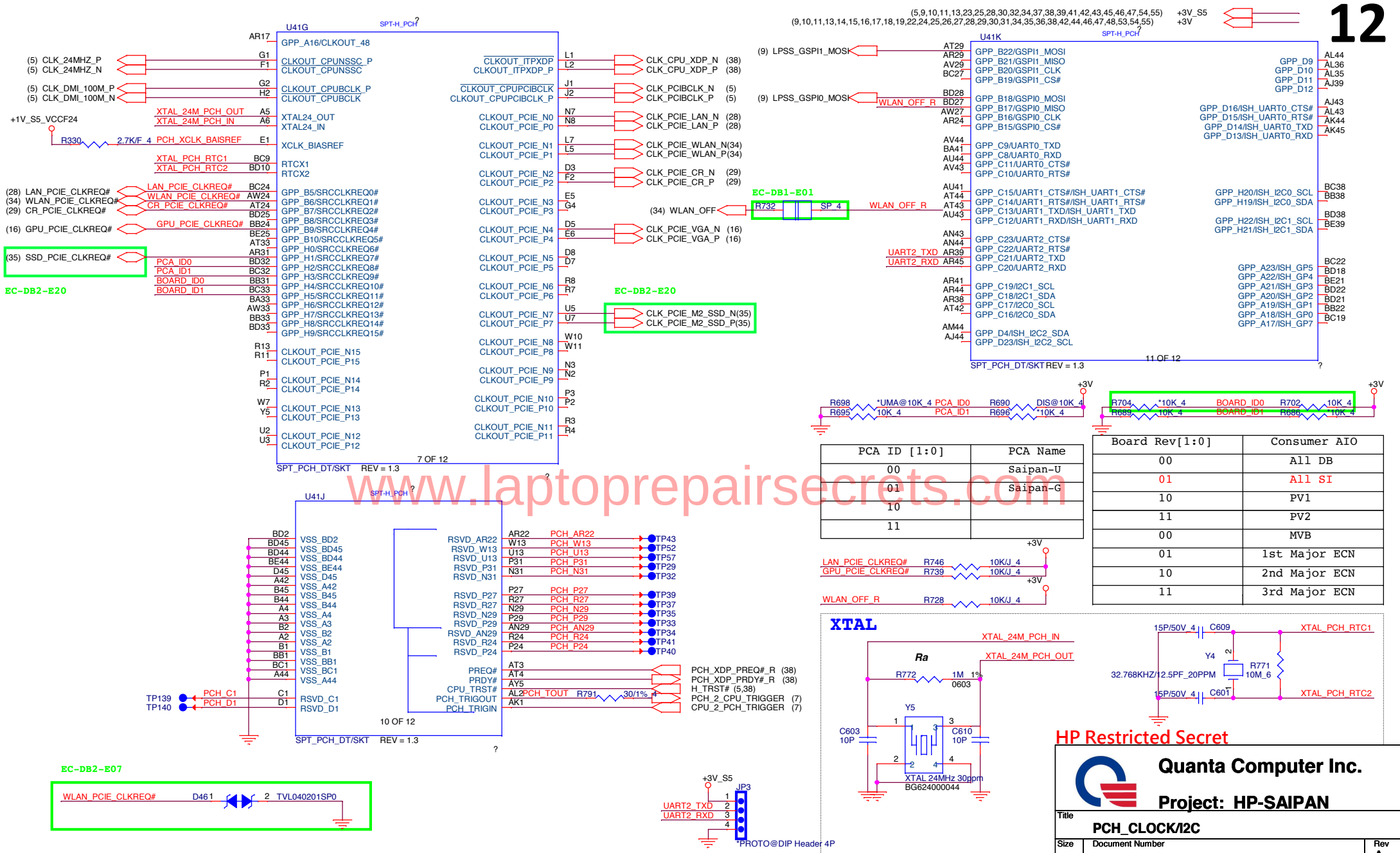
EN_DGPU_PWR
1 = dGPU power switch turned on
0 = Power switch turned off

EC-DB2-E05

EMI reserved
CK_24M_EC C594 10p/50V/NPO_4
CK_24M_LPC C153 *10p/50V/NPO_4

Quanta Computer Inc.
Project: HP-SAIPAN

Title: PCH_USB3/LPC
Size: Document Number: -- Rev: A
Page Modified: Thursday, December 17, 2015 Sheet 11 of 61



PCA ID [1:0]	PCA Name
00	Saipan-U
01	Saipan-G
10	
11	

Board Rev[1:0]	Consumer AIO
00	All DB
01	All SI
10	PV1
11	PV2
00	MVB
01	1st Major ECN
10	2nd Major ECN
11	3rd Major ECN

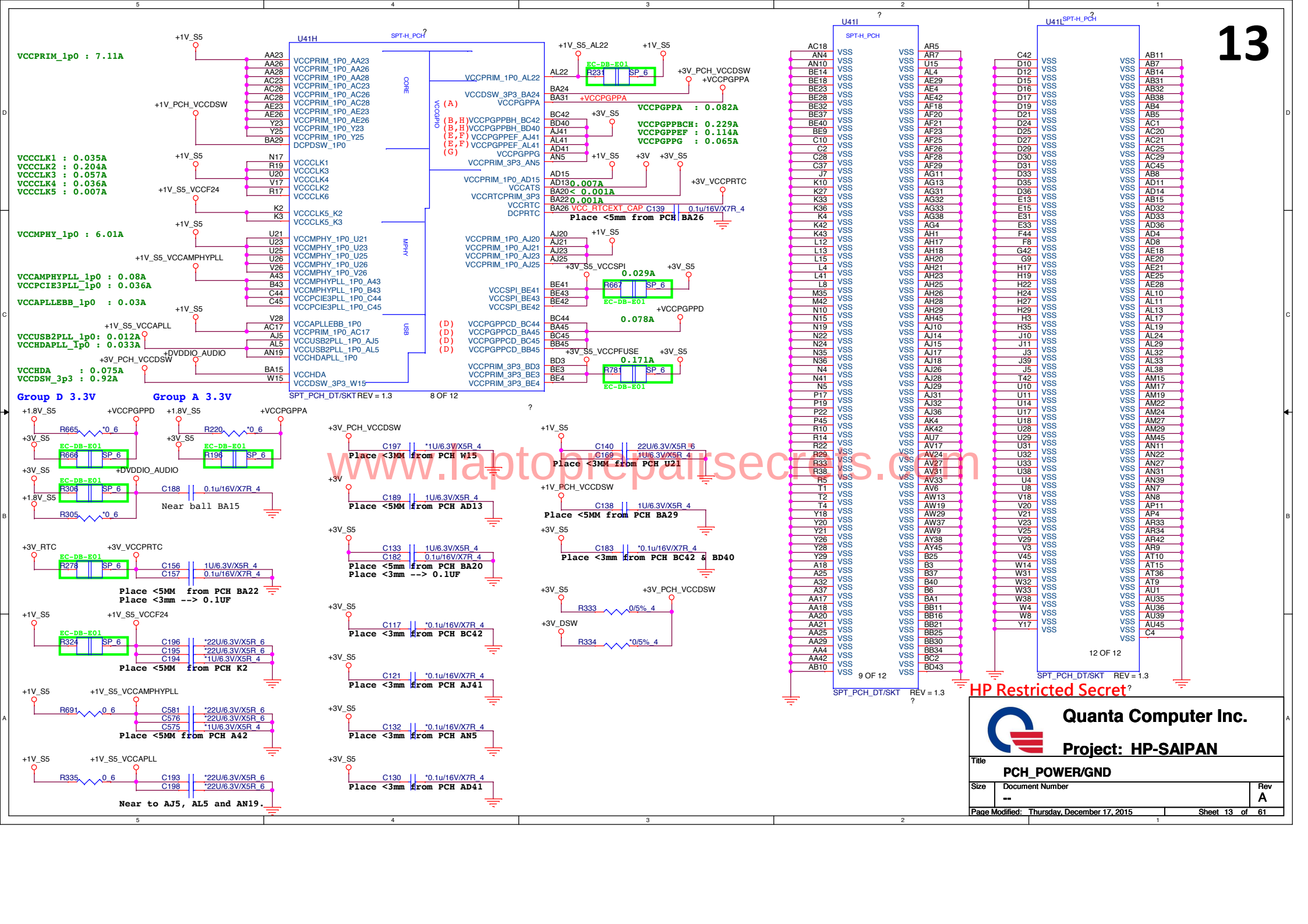
Quanta Computer Inc.

Project: HP-SAIPAN

Title: PCH_CLOCK/I2C

Size: | Document Number: -- | Rev: A

Page Modified: Thursday, December 17, 2015 | Sheet 12 of 61



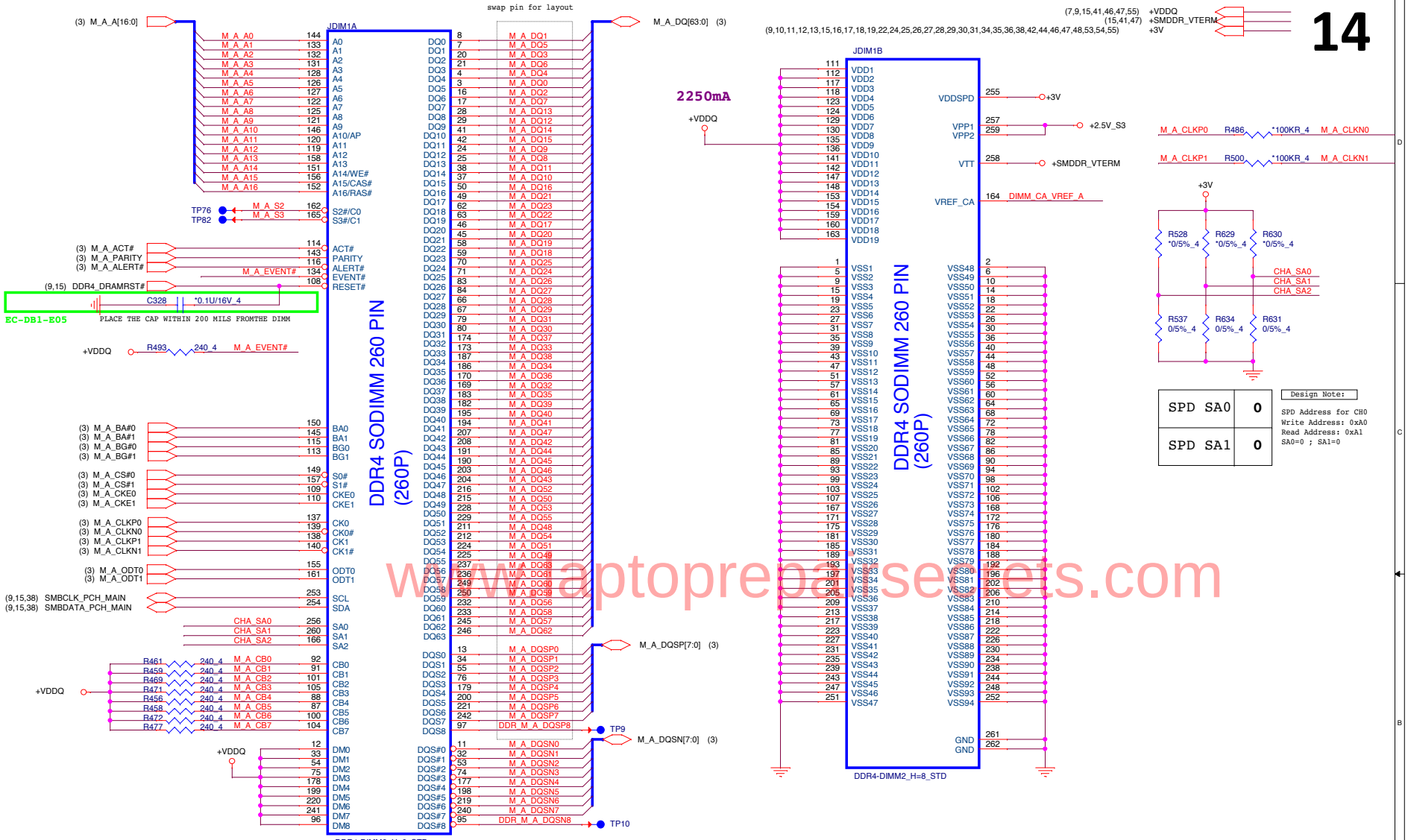
Quanta Computer Inc.

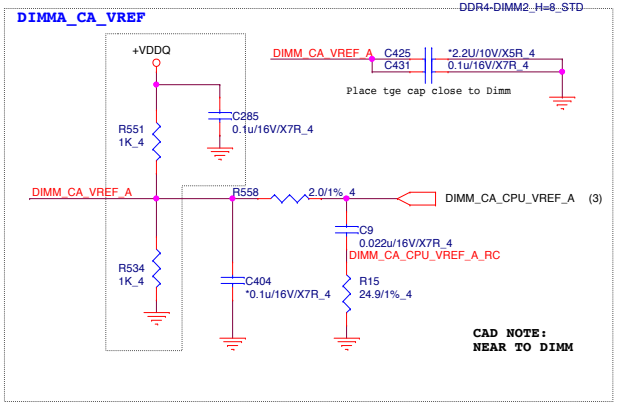
Project: HP-SAIPAN

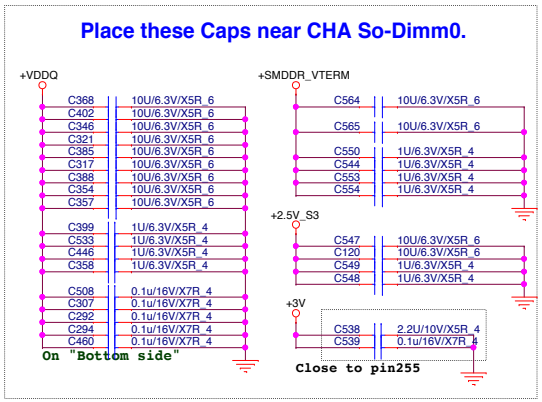
Title: PCH_POWER/GND

Size: | Document Number: -- | Rev: A

Page Modified: Thursday, December 17, 2015 | Sheet 13 of 61



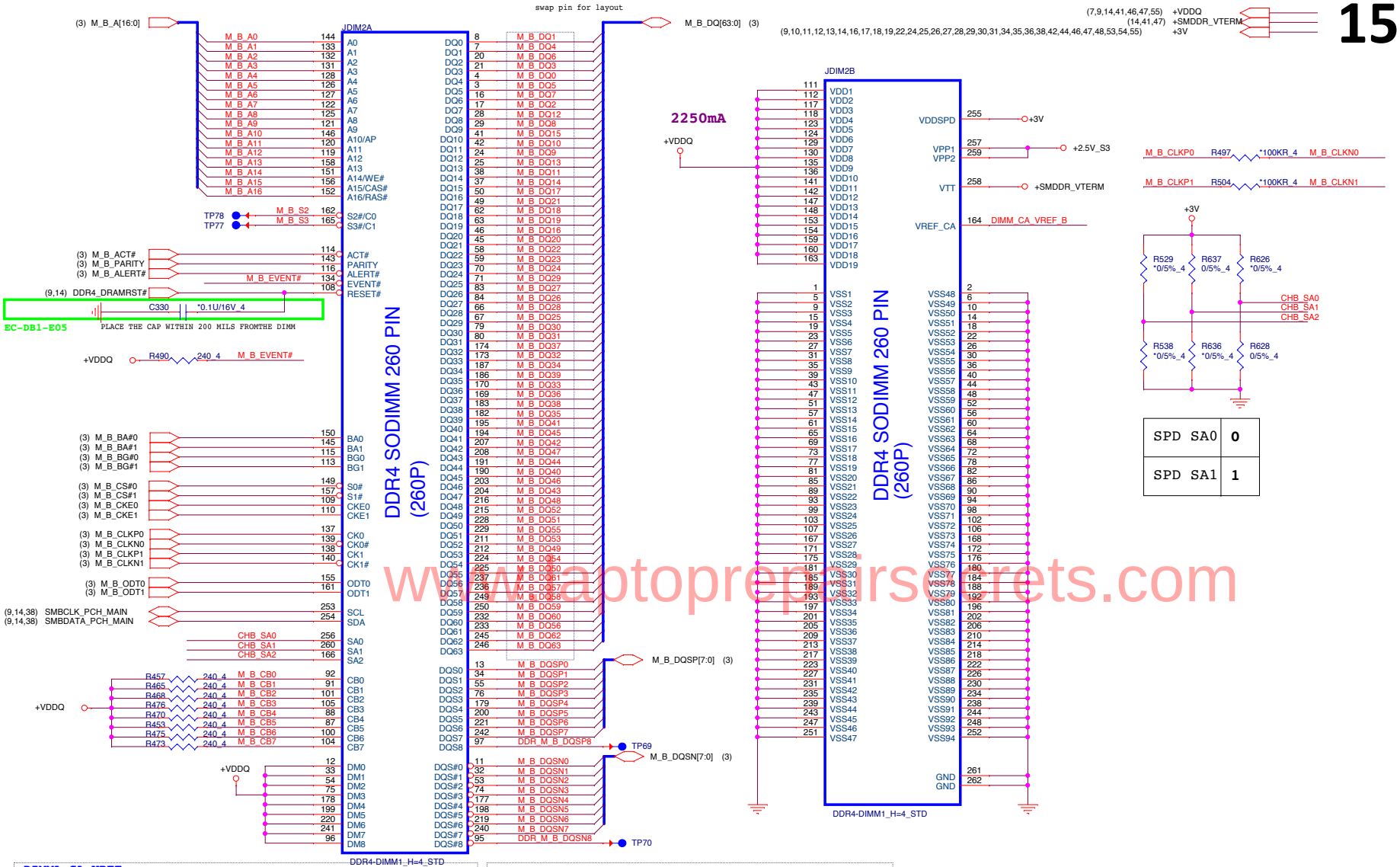


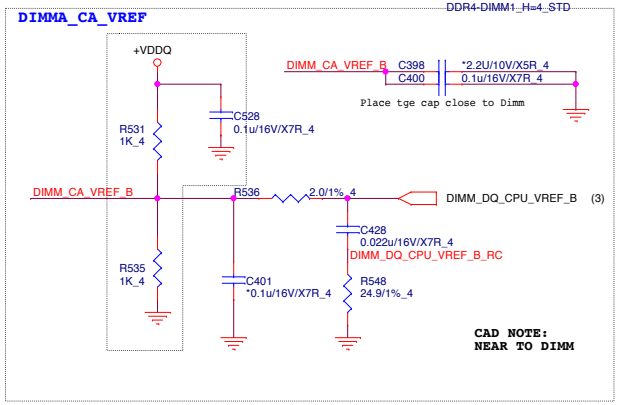


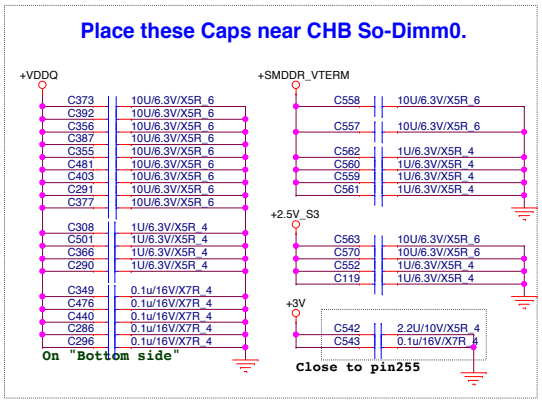
Quanta Computer Inc.

Project: HP-SAIPAN

Title	DDR4 CHA DIMM 0	
Size	Document Number	Rev
	–	A
Page Modified: Thursday, December 17, 2015	Sheet 14 of 61	







Quanta Computer Inc.

Project: HP-SAIPAN

Title: DDR4 CHB DIMM 1

Size	Document Number	Rev
	--	A

Page Modified: Thursday, December 17, 2015 | Sheet 15 of 61

(17,18,54) +1.05V_VGA
(18,19,20,53,54) +3.3V_VGA
(9,10,11,12,13,14,15,17,18,19,22,24,25,26,27,28,29,30,31,34,35,36,38,42,44,46,47,48,53,54,55) +3V
(20,53,54) +VGA_CORE

PEX_IOVDD + PEX_IOVDDQ = 1.042A

+1.05V_VGA

Near GPU
C393 DIS@22u/6.3V/X5R_6
C375 *DIS@22u/6.3V/X5R_6
C376 DIS@10u/6.3V/X5R_6
C433 *DIS@10u/6.3V/X5R_6
C474 DIS@4.7u/6.3V/X5R_4

Under GPU
C408 DIS@1u/6.3V/X5R_4
C462 *DIS@1u/6.3V/X5R_4

U7A
1/14 PCI_EXPRESS

AA22 PEX_IOVDD
AB23 PEX_IOVDD
AC24 PEX_IOVDD
AD25 PEX_IOVDD
AE26 PEX_IOVDD
AE27 PEX_IOVDD

+1.05V_VGA

Near GPU
C396 DIS@22u/6.3V/X5R_6
C374 *DIS@22u/6.3V/X5R_6
C395 DIS@10u/6.3V/X5R_6
C386 *DIS@10u/6.3V/X5R_6
C432 DIS@4.7u/6.3V/X5R_6

Under GPU
C438 DIS@1u/6.3V/X5R_4
C427 *DIS@1u/6.3V/X5R_4

AA10 PEX_IOVDDQ
AA12 PEX_IOVDDQ
AA13 PEX_IOVDDQ
AA16 PEX_IOVDDQ
AA18 PEX_IOVDDQ
AA19 PEX_IOVDDQ
AA20 PEX_IOVDDQ
AA21 PEX_IOVDDQ
AB22 PEX_IOVDDQ
AC23 PEX_IOVDDQ
AD24 PEX_IOVDDQ
AE25 PEX_IOVDDQ
AF26 PEX_IOVDDQ
AF27 PEX_IOVDDQ

PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA

Place all above caps on top side of CPU cavity

+3.3V_VGA

Near GPU
C519 DIS@4.7u/6.3V/X5R_6
C510 DIS@4.7u/6.3V/X5R_6
C493 DIS@0.1u/16V/X7R_4

AA8 PEX_PLL_HVDD
AA9 PEX_PLL_HVDD
AB8 PEX_SVDD_3V3

(53) VGA_VDD_SEN F2 VDD_SENSE
(53) VGA_GND_SEN F1 GND_SENSE

PEX_PLLVDD = 130mA

+1.05V_VGA
R527 *DIS@200/1% PEX_TSTCLK AF22 PEX_TSTCLK_OUT
PEX_TSTCLK# AE22 PEX_TSTCLK_OUT
CX300730001 Change to 0ohm
R543 DIS@0/5%_6

Near GPU
C441 DIS@4.7u/6.3V/X5R_6
C447 DIS@1u/6.3V/X5R_4
PEX_PLLVDD AA14 PEX_PLLVDD
AA15 PEX_PLLVDD

Under GPU
C456 DIS@0.1u/16V/X7R_4

R579 DIS@10k/5%_4 TESTMODE AD9 TESTMODE

R49 DIS@2.49k/1%_4 PEX_TERMP AF25 PEX_TERMP

bga595-nvidia-n13p-gv2-s-a2

PEX_WAKE AB6
PEX_RST AC7 VGA_RST# R611 DIS@0/5%_4 PEGX_RST# (19)
PEX_CLKREQ AC6 PEG_CLKREQ# R590 DIS@10k/5%_4 +3.3V_VGA
PEX_REFCLK AE8 PEG_REFCLK R589 DIS@0/5%_4 CLK_PCIE_VGA_P (12)
PEX_REFCLK# AD8 PEG_REFCLK# R587 DIS@0/5%_4 CLK_PCIE_VGA_N (12)

C513 *DIS@0.1u/16V/X7R_4

PEX_TX0	AC9	C_PEG_RXP0	C541	DIS@0.22u/10V/X5R_4	PEG_RXP0 (4)
PEX_TX0#	AB9	C_PEG_RXN0	C536	DIS@0.22u/10V/X5R_4	PEG_RXN0 (4)
PEX_RX0	AG6	C_PEG_TXP0	C89	DIS@0.22u/10V/X5R_4	PEG_TXP0 (4)
PEX_RX0#	AG7	C_PEG_TXN0	C88	DIS@0.22u/10V/X5R_4	PEG_TXN0 (4)
PEX_TX1	AB10	C_PEG_RXP1	C531	DIS@0.22u/10V/X5R_4	PEG_RXP1 (4)
PEX_TX1#	AC10	C_PEG_RXN1	C534	DIS@0.22u/10V/X5R_4	PEG_RXN1 (4)
PEX_RX1	AF7	C_PEG_TXP1	C87	DIS@0.22u/10V/X5R_4	PEG_TXP1 (4)
PEX_RX1#	AE7	C_PEG_TXN1	C85	DIS@0.22u/10V/X5R_4	PEG_TXN1 (4)
PEX_TX2	AD11	C_PEG_RXP2	C525	DIS@0.22u/10V/X5R_4	PEG_RXP2 (4)
PEX_TX2#	AC11	C_PEG_RXN2	C529	DIS@0.22u/10V/X5R_4	PEG_RXN2 (4)
PEX_RX2	AE9	C_PEG_TXP2	C84	DIS@0.22u/10V/X5R_4	PEG_TXP2 (4)
PEX_RX2#	AF9	C_PEG_TXN2	C83	DIS@0.22u/10V/X5R_4	PEG_TXN2 (4)
PEX_TX3	AC12	C_PEG_RXP3	C516	DIS@0.22u/10V/X5R_4	PEG_RXP3 (4)
PEX_TX3#	AB12	C_PEG_RXN3	C522	DIS@0.22u/10V/X5R_4	PEG_RXN3 (4)
PEX_RX3	AG9	C_PEG_TXP3	C82	DIS@0.22u/10V/X5R_4	PEG_TXP3 (4)
PEX_RX3#	AG10	C_PEG_TXN3	C81	DIS@0.22u/10V/X5R_4	PEG_TXN3 (4)

PEX_TX4 AB13
PEX_TX4# AC13
PEX_RX4 AF10
PEX_RX4# AE10
PEX_TX5 AD14
PEX_TX5# AC14
PEX_RX5 AE12
PEX_RX5# AF12
PEX_TX6 AC15
PEX_TX6# AB15
PEX_RX6 AG12
PEX_RX6# AG13
PEX_TX7 AB16
PEX_TX7# AC16
PEX_RX7 AF13
PEX_RX7# AE13

EC-DB-E03

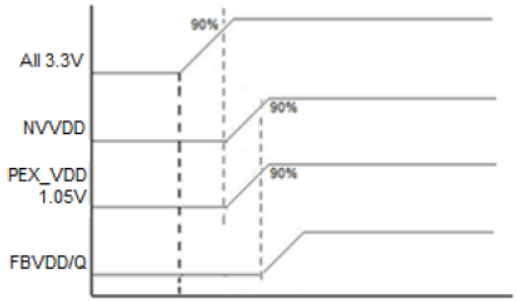
PEX_TX8 AD17
PEX_TX8# AC17
PEX_RX8 AE15
PEX_RX8# AF15
PEX_TX9 AC18
PEX_TX9# AB18
PEX_RX9 AG15
PEX_RX9# AG16
PEX_TX10 AB19
PEX_TX10# AC19
PEX_RX10 AF16
PEX_RX10# AE16
PEX_TX11 AD20
PEX_TX11# AC20
PEX_RX11 AE18
PEX_RX11# AF18
PEX_TX12 AC21
PEX_TX12# AB21
PEX_RX12 AG18
PEX_RX12# AG19
PEX_TX13 AD23
PEX_TX13# AE23
PEX_RX13 AF19
PEX_RX13# AE19
PEX_TX14 AF24
PEX_TX14# AE24
PEX_RX14 AE21
PEX_RX14# AF21
PEX_TX15 AG24
PEX_TX15# AG25
PEX_RX15 AG21
PEX_RX15# AG22

NC

GF117 GF119

COMMON

swap pin for layout



PEG_RST#

NV SUGGEST (for ADP only)
No stuff: U62,
stuff:R614

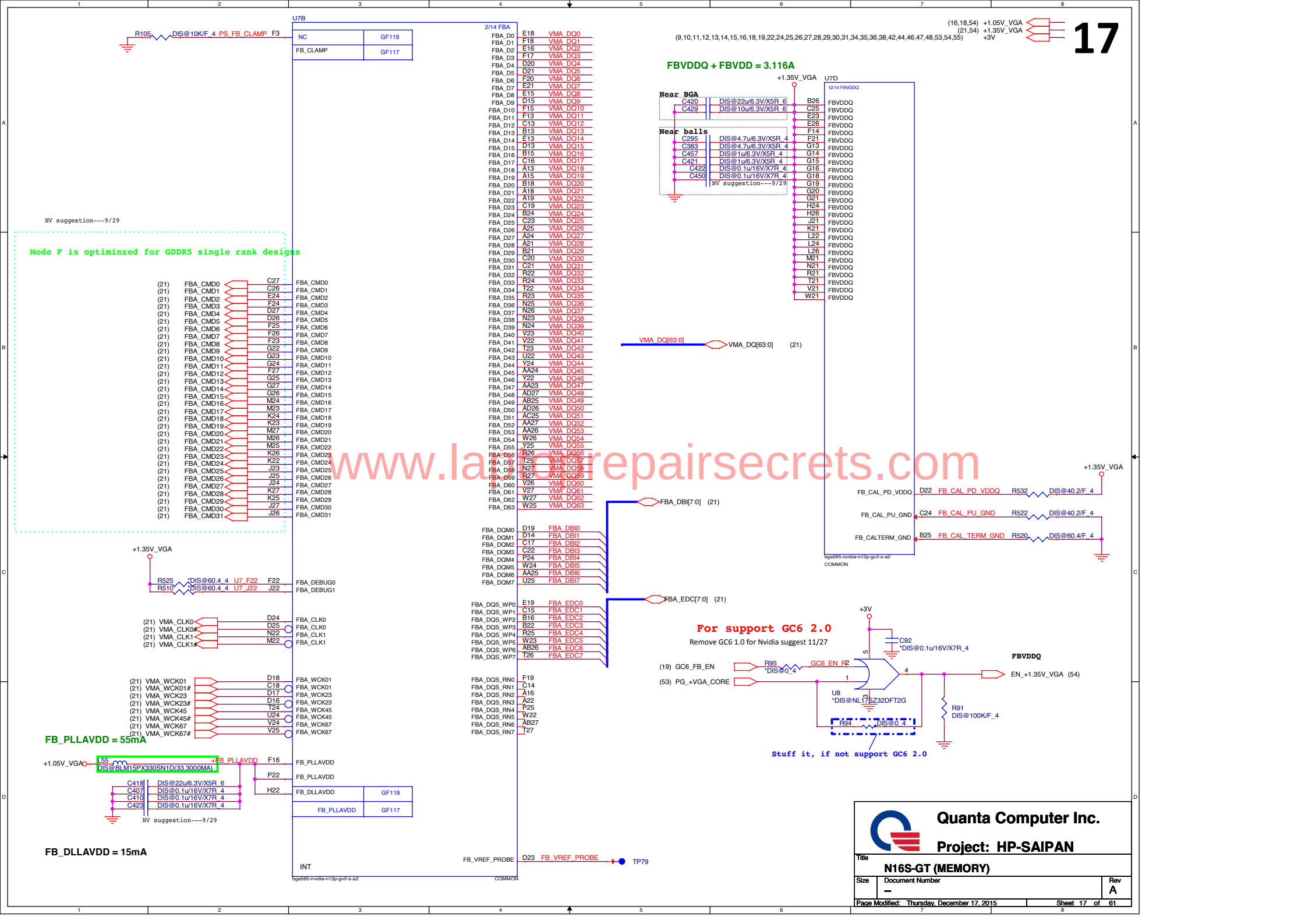
+3V
C535 DIS@0.1u/16V/X5R_4
(10,24,34,35) PLTRST_N_BUF
(11) DGPU_PLTRST_N
R618 SP_4 DGPU_PLTRST#
EC-DB1-E01
U35 DIS@TC7SH08FU
SYS_PEX_RST
EC-DB1-E02
R612 *DIS@0/5%_4
(19) GPU_PEX_RST_HOLD#
SYS_PEX_RST_MON# (19)
C546 DIS@0.1u/16V/X5R_4
PEGX_RST#
U36 *DIS@TC7SH08FU
R624 DIS@100K/F_4
SYS_PEX_RST_MON# R604 *DIS@100K/F_4
R614 DIS@0/5%_4

PEG_RST#

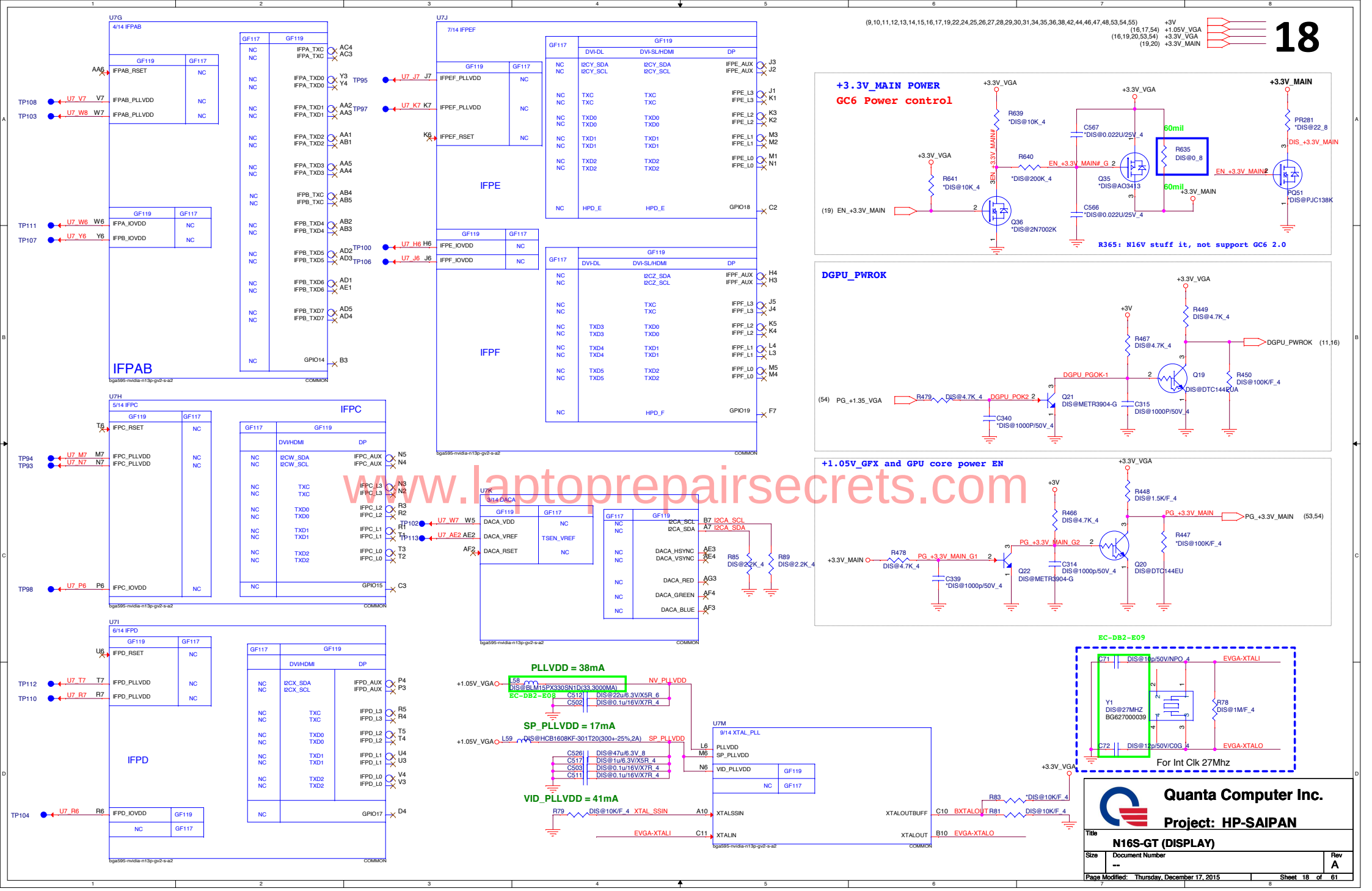
(11,18) DGPU_PWROK
+3.3V_VGA
EC-DB1-E07
R126 *DIS@10k/5%_4
+3V
EC-DB1-E07
R118 *DIS@10k/5%_4
PEG_CLKREQ#
Q6 DIS@PJA138K/50V_0.5A
GPU_PCIE_CLKREQ# (12)

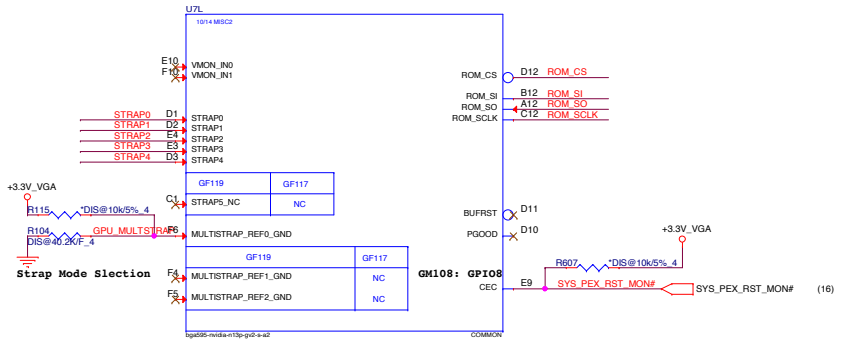
Quanta Computer Inc.
Project: HP-SAIPAN

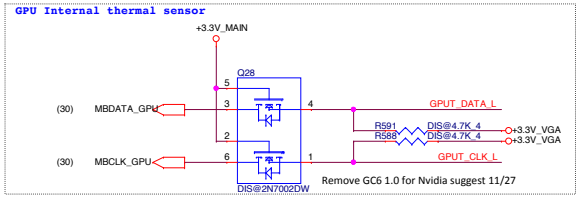
Title: N16S-GM_PCIE_Interface
Size: Document Number: -- Rev: A
Page Modified: Thursday, December 17, 2015 Sheet 16 of 61

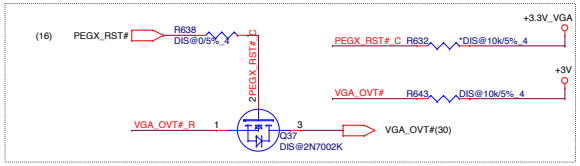


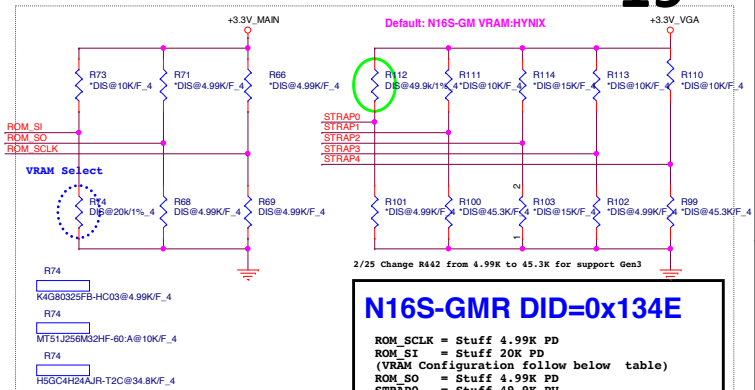
Quanta Computer Inc.	
Project: HP-SAIPAN	
Title: N16S-GT (MEMORY)	
Size:	Document Number: – Rev: A
Page Modified: Thursday, December 17, 2015	Sheet 17 of 61







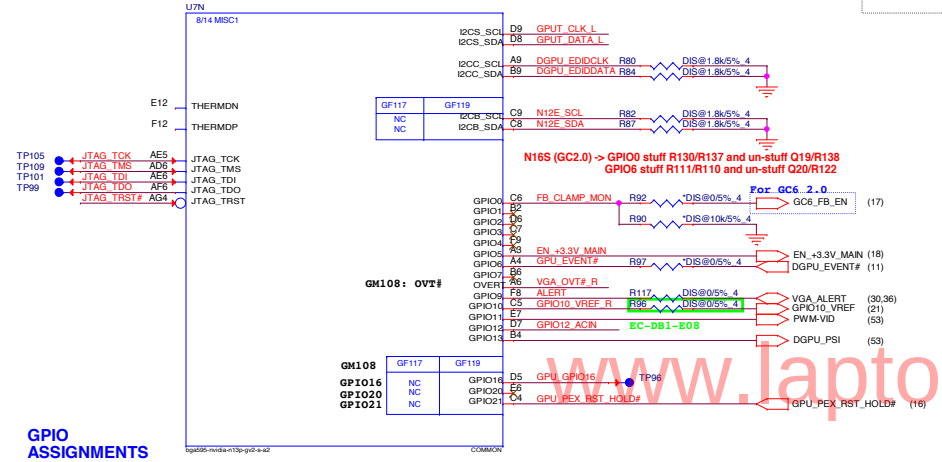




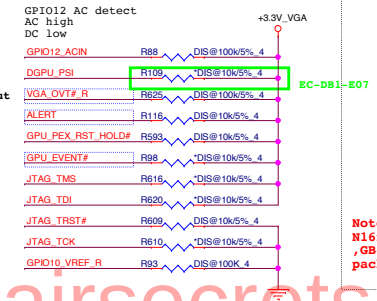
N16S-GMR DID=0x134E

```
ROM_SCLK = Stuff 4.99K PD
ROM_SI   = Stuff 20K PD
(VRAM Configuration follow below  table)
ROM_SO   = Stuff 4.99K PD
STRAP0   = Stuff 49.9K PU
STRAP1   = NC
STRAP2   = NC
STRAP3   = NC
STRAP4   = NC
```

GB2B-64



HW STRAPS:



OVT: Active low OD output

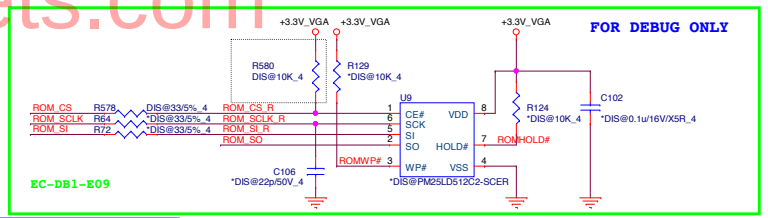
Alert: OD Input

For GC6 2.0

Note: GC6 2.0 is supported by N16x GPU in the GB2B ,GB4B-128,and GB3B-256 packages.

Logical Strap Bit Mapping

	PU-VDD	PD	QCI P/N
4.99K	1000	0000	CS24992FB26
10K	1001	0001	CS31002FB26
15K	1010	0010	CS31502FB24
20K	1011	0011	CS32002FB29
24.9K	1100	0100	CS32492FB16
30.1K	1101	0101	CS33012FB18
34.8K	1110	0110	CS33482FB06
45.3K	1111	0111	CS34532FB18



GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor (GC6 1.0)
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	OUT	FB_CLAMP_REQ#	Active low FB Clamp toggle request (GC6 1.0)
6	IN	DGPU_EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVT#	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

N16S-GM/-GT/-LP VRAM Configuration Table

ROM_SI

RAMCFG [3:0]	DESCRIPTION 1.35V gDDR5	Vendor	Vendor P/N	ROM_SI (R74)	STN B/S	Configuration
0000 0001	512Mx16	SAMSUNG Micron	K4G80325FB-HC03 MT51J256M32HF-60:A	PD 4.99K ohm PD 10K ohm		
0011 0110	256Mx16	SAMSUNG HYNIX	K4G41325FC-HC03 H5GC4H24AJR-T2C	PD 20K ohm PD 34.8K ohm		

HP Restricted Secret

Quanta Computer Inc.

Project: HP-SAIPAN

Title: N16S-GT (GPIO/STRAPS)

Size: | Document Number: -- | Rev: A

Page Modified: Thursday, December 17, 2015 | Sheet 19 of 61

(18,19) +3.3V_MAIN
(16,18,19,53,54) +3.3V_VGA
(53,54) +VGA_CORE

NVDD = 32.22 ~ 26.66 A

VDD33 = 56mA

+VGA_CORE

Under GPU

C473 DIS@1u/6.3V/X5R_4
C461 DIS@1u/6.3V/X5R_4
C430 DIS@1u/6.3V/X5R_4
C439 DIS@1u/6.3V/X5R_4
C453 DIS@4.7u/6.3V/X5R_6
C454 DIS@4.7u/6.3V/X5R_6
C464 DIS@4.7u/6.3V/X5R_6
C435 DIS@4.7u/6.3V/X5R_6
C490 DIS@4.7u/6.3V/X5R_6
C437 DIS@4.7u/6.3V/X5R_6
C463 DIS@4.7u/6.3V/X5R_6
C455 DIS@4.7u/6.3V/X5R_6
C434 DIS@4.7u/6.3V/X5R_6
C452 DIS@4.7u/6.3V/X5R_6

Near GPU

C545 *DIS@330u_2.5V_3528
C105 DIS@390U/2.5V/ELEC
C491 DIS@22u/6.3V/X5R_6
C94 DIS@47u/6.3V_8
C465 DIS@4.7u/6.3V/X5R_6
C436 DIS@4.7u/6.3V/X5R_6
C492 DIS@4.7u/6.3V/X5R_6
C466 DIS@4.7u/6.3V/X5R_6
C451 DIS@4.7u/6.3V/X5R_6

330uf : ESR <=6m ohm

U7E
11/14 NVVDD
K10 K12 K14 K16 K18 L11 L13 L15 L17 M10 M12 M14 M16 M18 N11 N13 N15 N17 P10 P12 P14 P16 P18 R11 R13 R15 R17 T10 T12 T14 T16 T18 U11 U13 U15 U17 V10 V12 V14 V16 V18 — VDD
bga595-nvidia-n13p-gv2-s-a2
COMMON

TP92
U7_F11 R11 3V3AUX_NC

U7C
14/14 XVDD/VDD33
AD10 NC
AD7 NC
B19 NC
V5 FERMI_RSVD1_NC
V6 FERMI_RSVD2_NC
VDD33 G10
VDD33 G12
VDD33 G8
VDD33 G9
CONFIGURABLE POWER CHANNELS
* nc on substrate
G1 XPWR_G1
G2 XPWR_G2
G3 XPWR_G3
G4 XPWR_G4
G5 XPWR_G5
G6 XPWR_G6
G7 XPWR_G7
V1 XPWR_V1
V2 XPWR_V2
W1 XPWR_W1
W2 XPWR_W2
W3 XPWR_W3
W4 XPWR_W4
bga595-nvidia-n13p-gv2-s-a2 COMMON

+3.3V_VGA
C555 DIS@4.7u/6.3V/X5R_6
C458 DIS@1u/6.3V/X5R_4
Near BGA
C467 DIS@0.1u/16V/X7R_4
Near balls

+3.3V_MAIN
C540 DIS@4.7u/6.3V/X5R_6
C484 DIS@1u/6.3V/X5R_4
Near BGA
C485 DIS@0.1u/16V/X7R_4
C486 DIS@0.1u/16V/X7R_4
Near balls

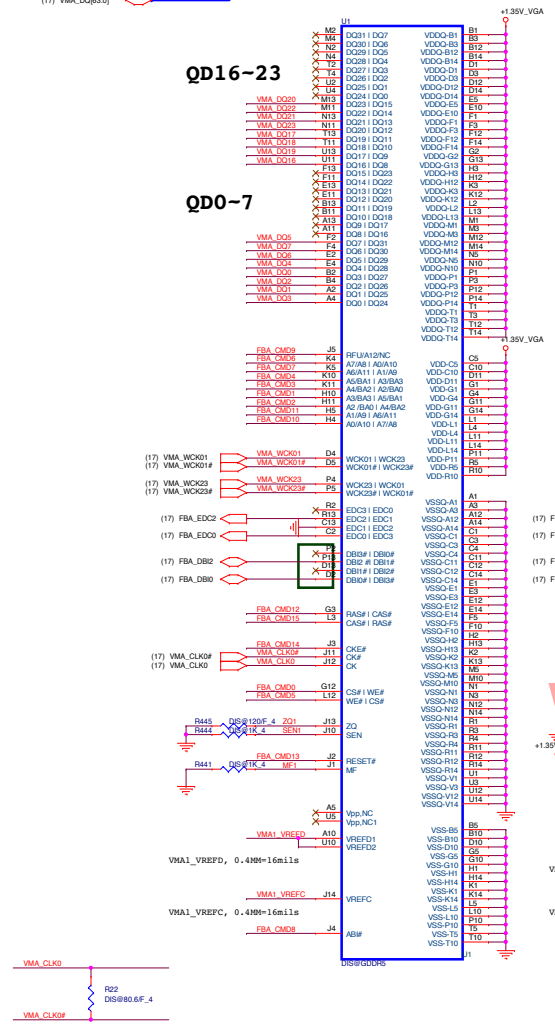
U7F
13/14 GND
A2 AB17 AB20 AB24 AC2 AC22 AC26 AC5 AC8 AD12 AD13 A26 AD15 AD16 AD18 AD19 AD21 AD22 AE11 AE14 AE17 AE20 AB11 AF1 AF11 AF14 AF17 AF20 AF23 AF5 AF8 AG2 AG26 AB14 B1 B11 B14 B17 B20 B23 B27 B5 B8 E11 E14 E17 E2 E20 E22 E25 E5 E8 H2 H23 H25 H5 K11 K13 K15 K17 L10 L12 L14 L16 L18 L2 L23 L25 L5 M11 — GND
M13 M15 M17 N10 N12 N14 N16 N18 P11 P13 P15 P17 P2 P23 P26 P5 R10 R12 R14 R16 R18 T11 T13 T15 T17 U10 U12 U14 U16 U18 U2 U23 U26 U5 V11 V13 V15 V17 Y2 Y23 Y26 Y5 — GND
AA7 AB7 — GND
bga595-nvidia-n13p-gv2-s-a2 COMMON

Quanta Computer Inc.
Project: HP-SAIPAN

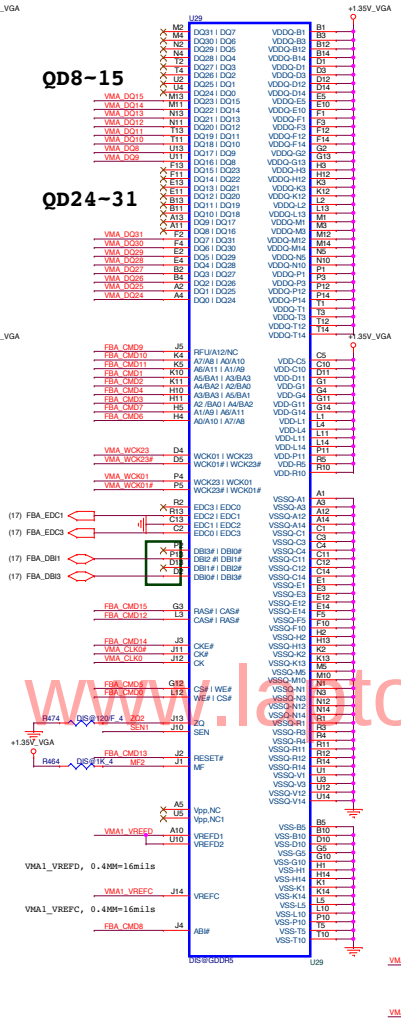
Title		
NV16S-GM_Power/GND		
Size	Document Number	Rev
	--	A
Page Modified: Thursday, December 17, 2015		Sheet 20 of 61

2GB gDDR5

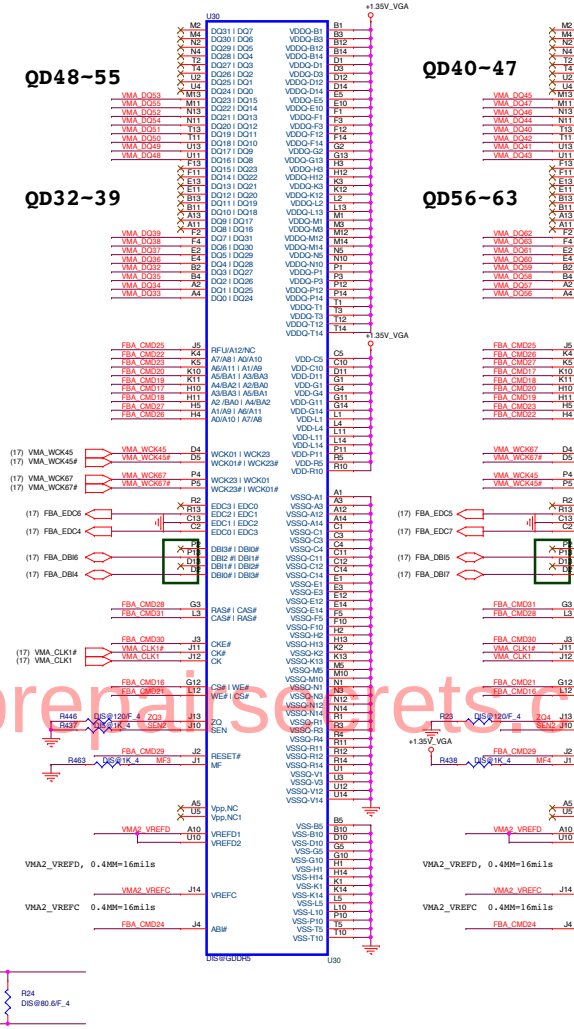
Channel A0
MF=0 Non-mirrored



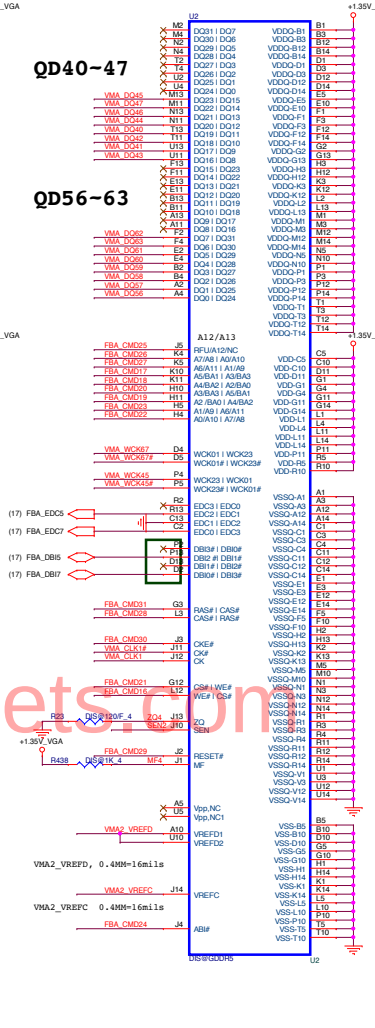
MF=1 Mirrored



Channel A1
MF=0 Non-mirrored



MF=1 Mirrored



NV suggestion---9/29
Place near memory side

GDDR5 Mode H Mapping

< 0-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

CKE* is strap pin to set ODT value of memory chip

RST PD place @ the end of daisy-chain.

Layout:
0.1uf to close memory device
Larger caps slightly farther away

Quanta Computer Inc.	
Project: HP-SAIPAN	
Title: VRAM_DDR3 BGA96	
Size:	Document Number: -- Rev: A
Page Modified: Thursday, December 17, 2015	Sheet 21 of 61

eDP to LVDS (RTD2136N-CG)

(9,10,11,12,13,14,15,16,17,18,19,24,25,26,27,28,29,30,31,34,35,36,38,42,44,46,47,48,53,54,55) +3V

DP input signals

(11,24) DDPD_HPD — R693 FHD@1K/F_4 — R688 FHD@100K/F_4

eDP_HPD with pull down 100K-ohm on PCH side.

qHD / FHD co-lay

3 PAD
(4) EDP_AUXN — C573 FHD@0.1u/16V/X7R_4 2136_AUXN — C93 *QHD@0.1u/16V/X7R_4 7515_AUXN (24)
(4) EDP_AUXP — C572 FHD@0.1u/16V/X7R_4 2136_AUXP — C95 *QHD@0.1u/16V/X7R_4 7515_AUXP (24)
(4) DDID_TXDP0 — C571 FHD@0.1u/16V/X7R_4 DPD_TXP0_R — C112 *QHD@0.1u/16V/X7R_4 7515_TXP0 (24)
(4) DDID_TXDN0 — C568 FHD@0.1u/16V/X7R_4 DPD_TXN0_R — C111 *QHD@0.1u/16V/X7R_4 7515_TXN0 (24)
(4) DDID_TXDP1 — C556 FHD@0.1u/16V/X7R_4 DPD_TXP1_R — C103 *QHD@0.1u/16V/X7R_4 7515_TXP1 (24)
(4) DDID_TXDN1 — C551 FHD@0.1u/16V/X7R_4 DPD_TXN1_R — C100 *QHD@0.1u/16V/X7R_4 7515_TXN1 (24)

+SWR_V12 — C134 FHD@0.1u/16V/X5R_4

2136_BKLT_EN
EDID_DAT
EDID_CLK
2136_CFG0
2136_CFG1

U37 RTD2136N FHD@RTD2136N-CG(QFN)

1	eDP_HPD_R	DP_HPD	
2	TEST_MODE	TEST_MODE	
3	2136_AUXN	AUX-CH_N	
4	2136_AUXP	AUX-CH_P	
5		DP_V33	
6	+3.3V_2136_AVCC33	DP_GND	
7	DPD_TXP0_R	LANE0P	
8	DPD_TXN0_R	LANE0N	
9	DPD_TXP1_R	LANE1P	
10	DPD_TXN1_R	LANE1N	
11		DP_V12	
12	DP_REXT	DP_REXT	
13	LVDS_SCL	CIICSCL1	
14	LVDS_SDA	CIICSDA1	
15	+SWR_V12	SWR_VCCK	
16	+3.3V_2136_DVCC33	GND	
17	+SWR_LX	SWR_LX	
18		SWR_VDD	
19	PCH_BRIGHT	GPIO/PWMOUT	
20	2136_LVDS_PWREN	GPIO/PWM1	
21	2136_VADJ	GPIO/PWMIN	
22		PVCC	
23		TXE3+	
24		TXE3-	

49	EPD		
48	MIICSCL0		
47	MIICSDA0		
46	MIICSCL1		
45	MIICSDA1		
44	GPIO/PWM0/PWMOUT		
43	VCCK		
42	TXO0-		
41	TXO0+		
40	TXO1-		
39	TXO1+		
38	TXO2-		
37	TXO2+		

36	TXOC-		
35	TXOC+		
34	TXO3-		
33	TXO3+		
32	TXE0-		
31	TXE0+		
30	TXE1-		
29	TXE1+		
28	TXE2-		
27	TXE2+		
26	TXEC-		
25	TXEC+		

ODD_CH

LVDS_TX_ON0 (23)
LVDS_TX_OP0 (23)
LVDS_TX_ON1 (23)
LVDS_TX_OP1 (23)
LVDS_TX_ON2 (23)
LVDS_TX_OP2 (23)
LVDS_TXCLK_ON (23)
LVDS_TXCLK_OP (23)
LVDS_TX_ON3 (23)
LVDS_TX_OP3 (23)

EVEN_CH

LVDS_TX_EN0 (23)
LVDS_TX_EP0 (23)
LVDS_TX_EN1 (23)
LVDS_TX_EP1 (23)
LVDS_TX_EN2 (23)
LVDS_TX_EP2 (23)
LVDS_TXCLK_EN (23)
LVDS_TXCLK_EP (23)
LVDS_TX_EN3 (23)
LVDS_TX_EP3 (23)

C125 FHD@0.1u/16V/X5R_4 — R663 FHD@12K/F_6

C731 close to Pin22 — C113 FHD@0.1u/16V/X7R_4

RTD2136N Power

+3V — L10 FHD@HCB1608KF-600T30 — +3.3V_2136_DVCC33
C118 FHD@10U/6.3V/X5R_6
C127 FHD@0.1u/16V/X5R_4
C108 FHD@10U/6.3V/X5R_6
C115 FHD@0.1u/16V/X5R_4
EC-DB2-E13
Trace width >40mils
>80mils Near to Pin18 within 200mils

+3V — L11 FHD@HCB1608KF-600T30 — +3.3V_2136_AVCC33
C126 FHD@10U/6.3V/X5R_6
C128 FHD@0.1u/16V/X5R_4
C131 FHD@0.1u/16V/X5R_4

+SWR_LX — L60 FHD@0.8 — +SWR_V12
C569 FHD@22U/6.3V/X5R_6
C109 FHD@0.1u/16V/X7R_4
Trace width >30mils Near to Pin17 within 400mils

SWR MODE /LDO MODE

L9	2.2-uH	0 Olm
SWR	Connect	NC
LDO	NC	Connect

EDID

EDID_CLK — R180 FHD@4.7K/F_4
EDID_DAT — R181 *FHD@4.7K/F_4
R822 FHD@4.7K/F_4
+3.3V_2136_DVCC33
EC-DB2-E12

Intel CRB

2136_AUXN — R683 *FHD@100k/1%_4
2136_AUXP — R677 *FHD@100k/1%_4
+3V

GPIO & TESTing signals

(52) 2136_VADJ
(23) 2136_LVDS_PWREN
(23) 2136_BKLT_EN
(10,24) PCH_BRIGHT
TEST_MODE
2136_VADJ
2136_LVDS_PWREN
2136_BKLT_EN
PCH_BRIGHT
R687 FHD@100K/F_4
R658 100K/F_4

NEED STUFF FOR FHD/QHD

Mode select

2136_CFG1 — R707 *FHD@4.7K/F_4 FHD@4.7K/F_4
2136_CFG0 — R710
R700 *FHD@4.7K_4 FHD@4.7K_4
R699
+3.3V_2136_DVCC33

2136_CFG1 (PIN48)	2136_CFG0 (PIN47) = 0	2136_CFG0 (PIN47) = 1
0	X	EP MODE
1	ROM ONLY MODE	EEPROM MODE

EEPROM

EC-DB2-E11
+3.3V_2136_DVCC33
C116 *FHD@0.1u/16V/X7R_4
U13 *FHD@M24C64
EDID_DAT
EDID_CLK
VCC SDA SCL GND WP A2 A1 A0

1- EEPROM with a size 8K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

In System Programing slave address=0xA8

+3.3V_2136_DVCC33
R647 FHD@4.7K/F_4
R649 FHD@4.7K/F_4

EC

(30) LVDS_SCL — LVDS_SCL
(30) LVDS_SDA — LVDS_SDA

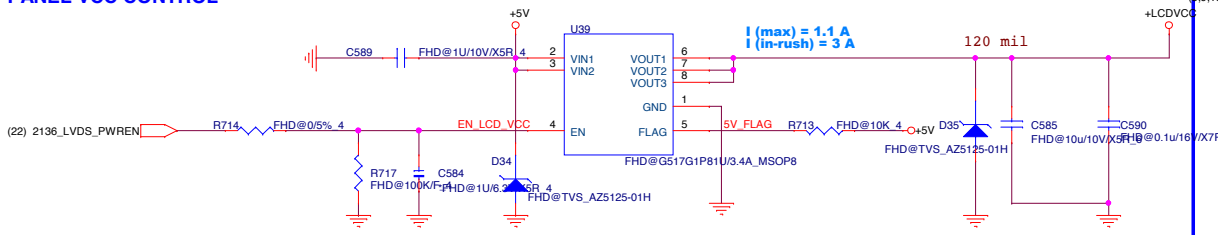
HP Restricted Secret

Quanta Computer Inc.
Project: HP-SAIPAN

Title		
eDP-LVDS_RTD2136N		
Size	Document Number	Rev
	--	A
Page Modified: Thursday, December 17, 2015		Sheet 22 of 61

LED PANEL

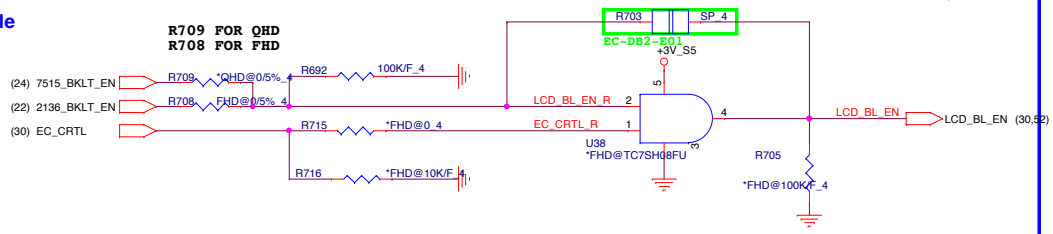
PANEL VCC CONTROL



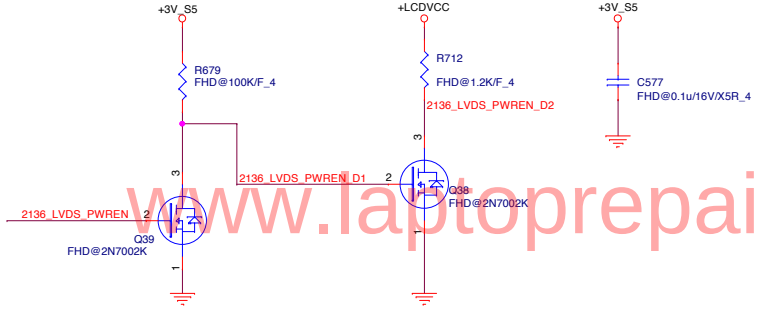
(31,39,40,41,42,43,44,46,47,49,50,51,52,53,54,55) +VIN
(5,9,10,11,12,13,25,28,30,32,34,37,38,39,41,42,43,45,46,47,54,55) +3V_S5
(26,27,31,36,39,46,47,48,49,50,53,55) +5V

23

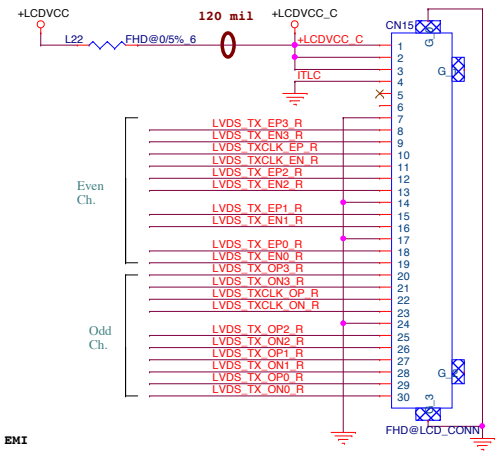
BackLight Enable



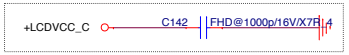
LCDVCC Discharge Circuit



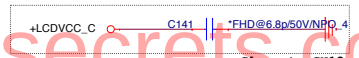
LVDS Conn



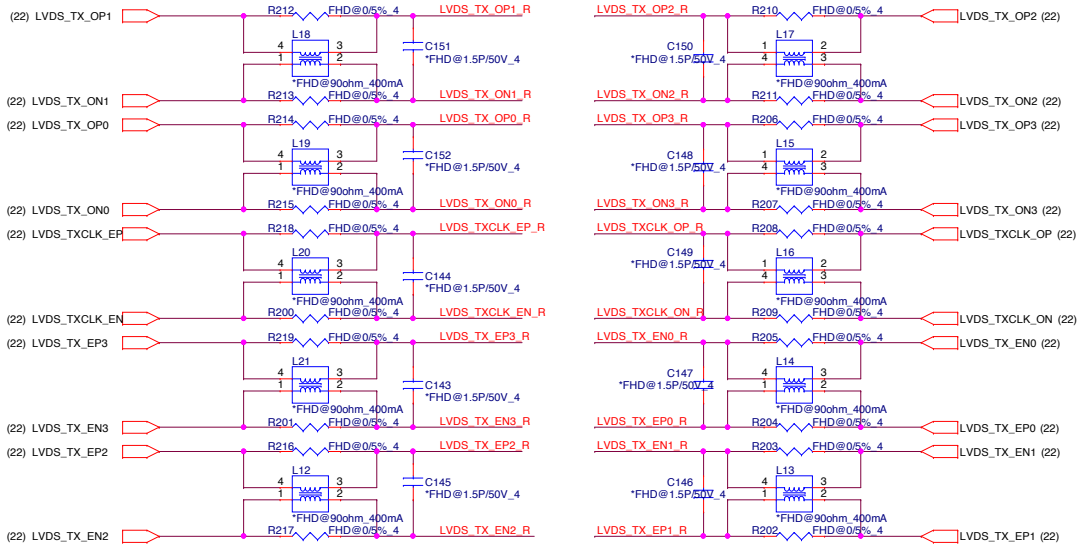
EMI



RF



EMI

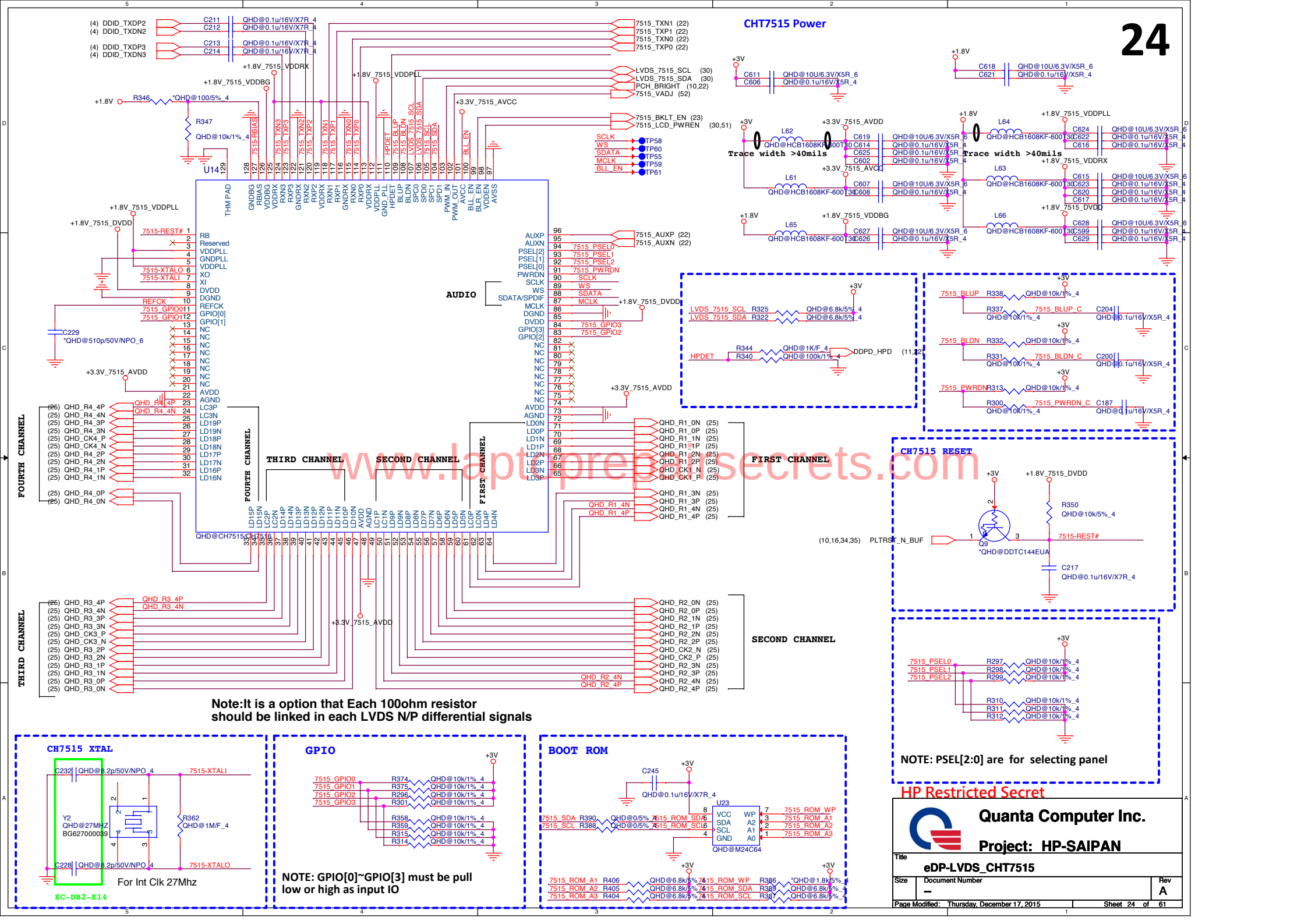


HP Restricted Secret

Quanta Computer Inc.

Project: HP-SAIPAN

Title: Panel (Control).LCD-Conn.		
Size	Document Number: --	Rev: A
Page Modified: Thursday, December 17, 2015	Sheet 23 of 61	



Quanta Computer Inc.

Project: HP-SAIPAN

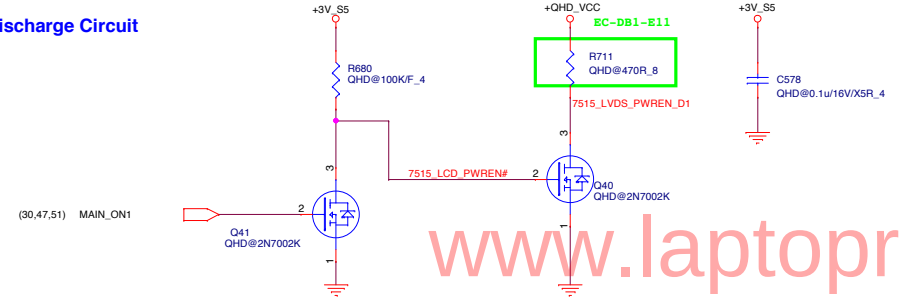
Title		
eDP-LVDS_CHT7515		
Size	Document Number	Rev
–		A
Page Modified: Thursday, December 17, 2015		Sheet 24 of 61

LED PANEL

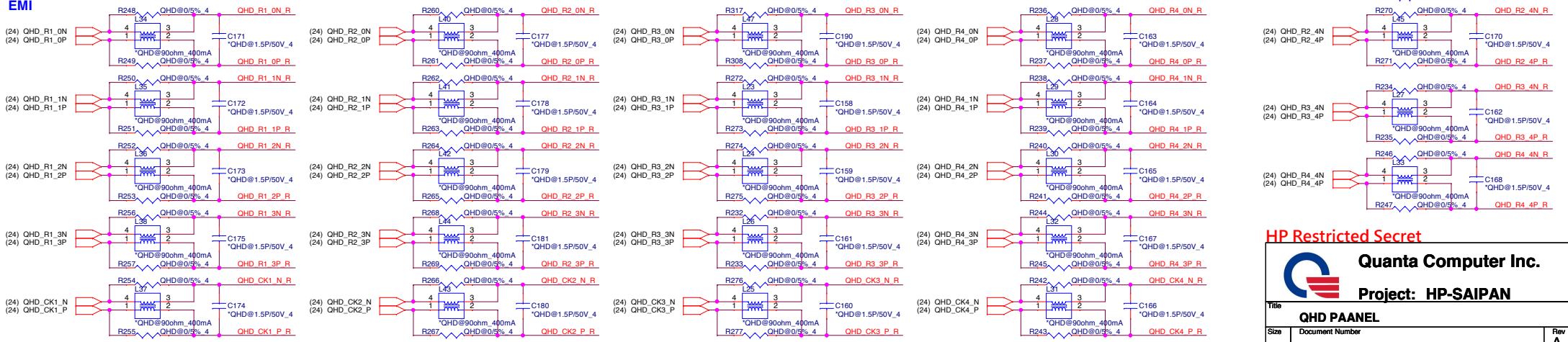
PANEL VCC CONTROL

EC-DB1-E10

LCDVCC Discharge Circuit



EMI

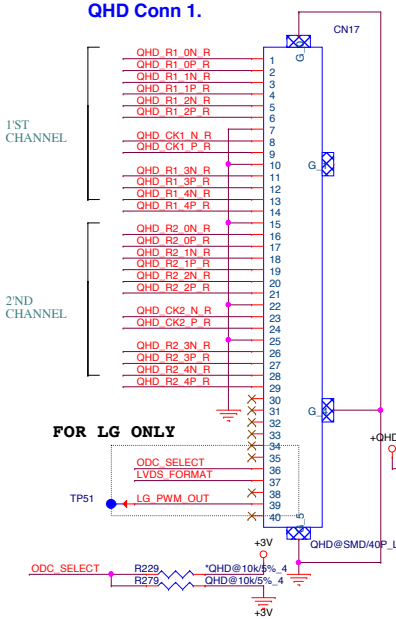


(31,39,40,41,42,43,44,46,47,49,50,51,52,53,54,55) +VIN
(5,9,10,11,12,13,23,28,30,32,34,37,38,39,41,42,43,45,46,47,54,55) +3V_S5
(23,26,27,31,36,39,46,47,48,49,50,53,55) +5V

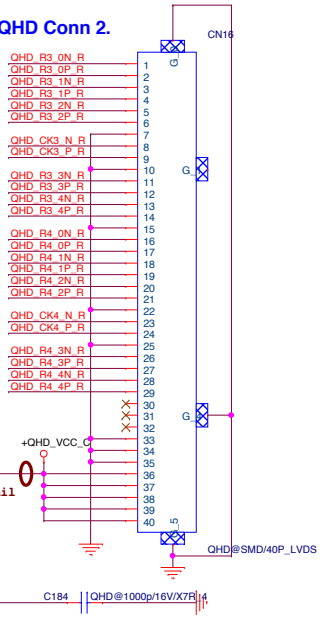
25

AUO (default pin to pin)

QHD Conn 1.



QHD Conn 2.



FOR LG ONLY

HP Restricted Secret

Quanta Computer Inc.

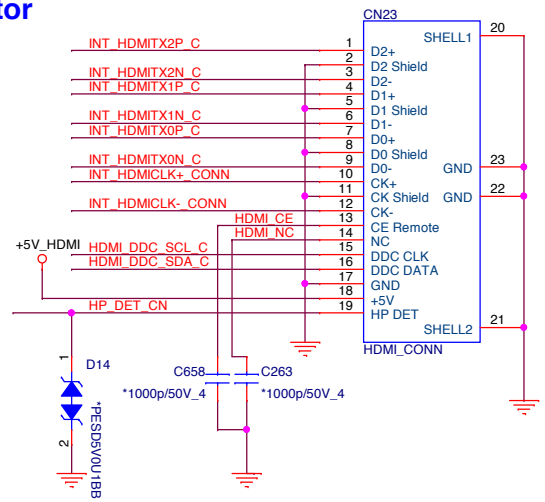
Project: HP-SAIPAN

Title	QHD PAANEL	
Size	Document Number	Rev
	–	A
Page Modified: Thursday, December 17, 2015		Sheet 25 of 61

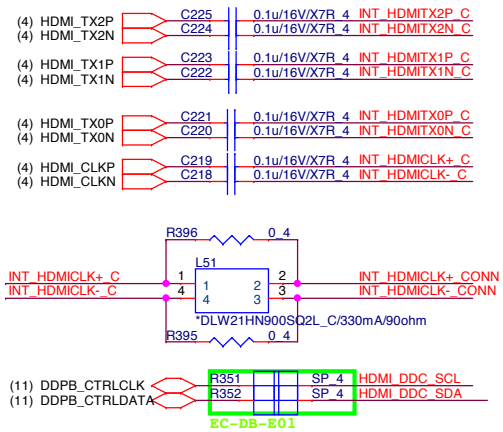
HDMI

(9,10,11,12,13,14,15,16,17,18,19,22,24,25,27,28,29,30,31,34,35,36,38,42,44,46,47,48,53,54,55) +3V
(23,27,31,36,39,46,47,48,49,50,53,55) +5V

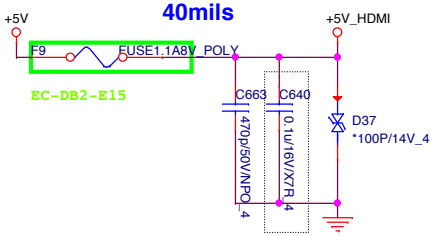
HDMI connector



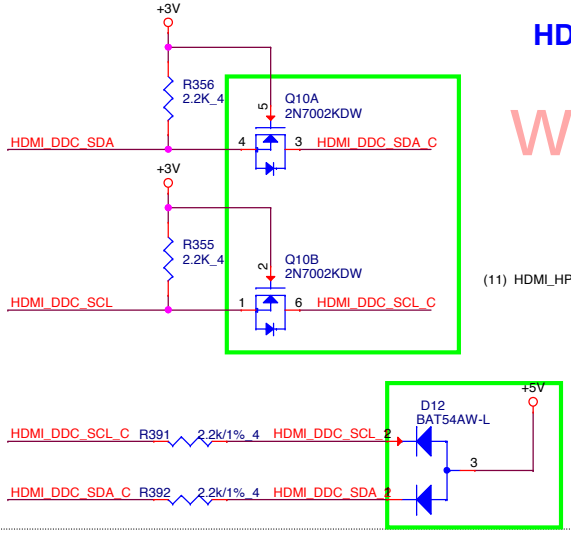
HDMI INTERFACE



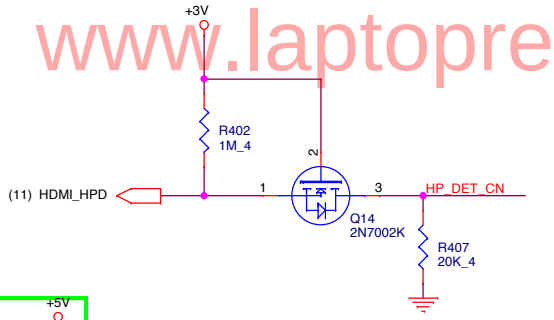
HDMI POWER SUPPLY



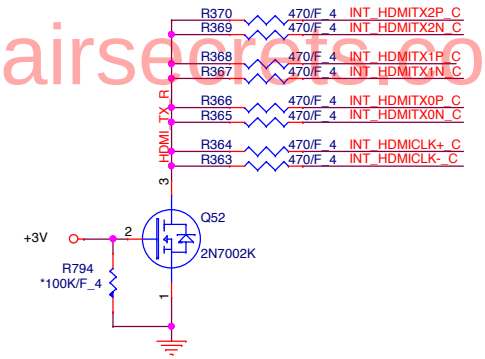
HDMI DDC



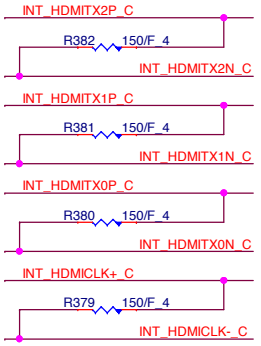
HDMI-detect



HDMI LEVEL SHIFT

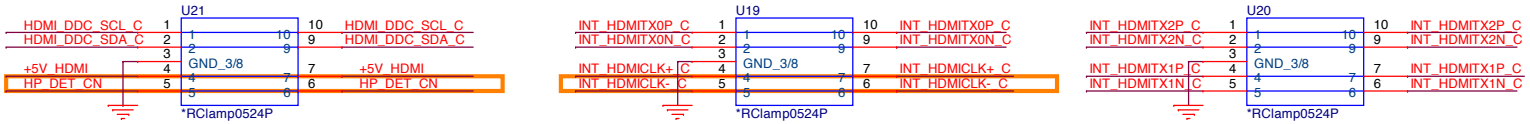


HDMI EMI (EMC)



ESD reserve for HDMI

Layout Notes:
Place decoupling CAPs close to Connector



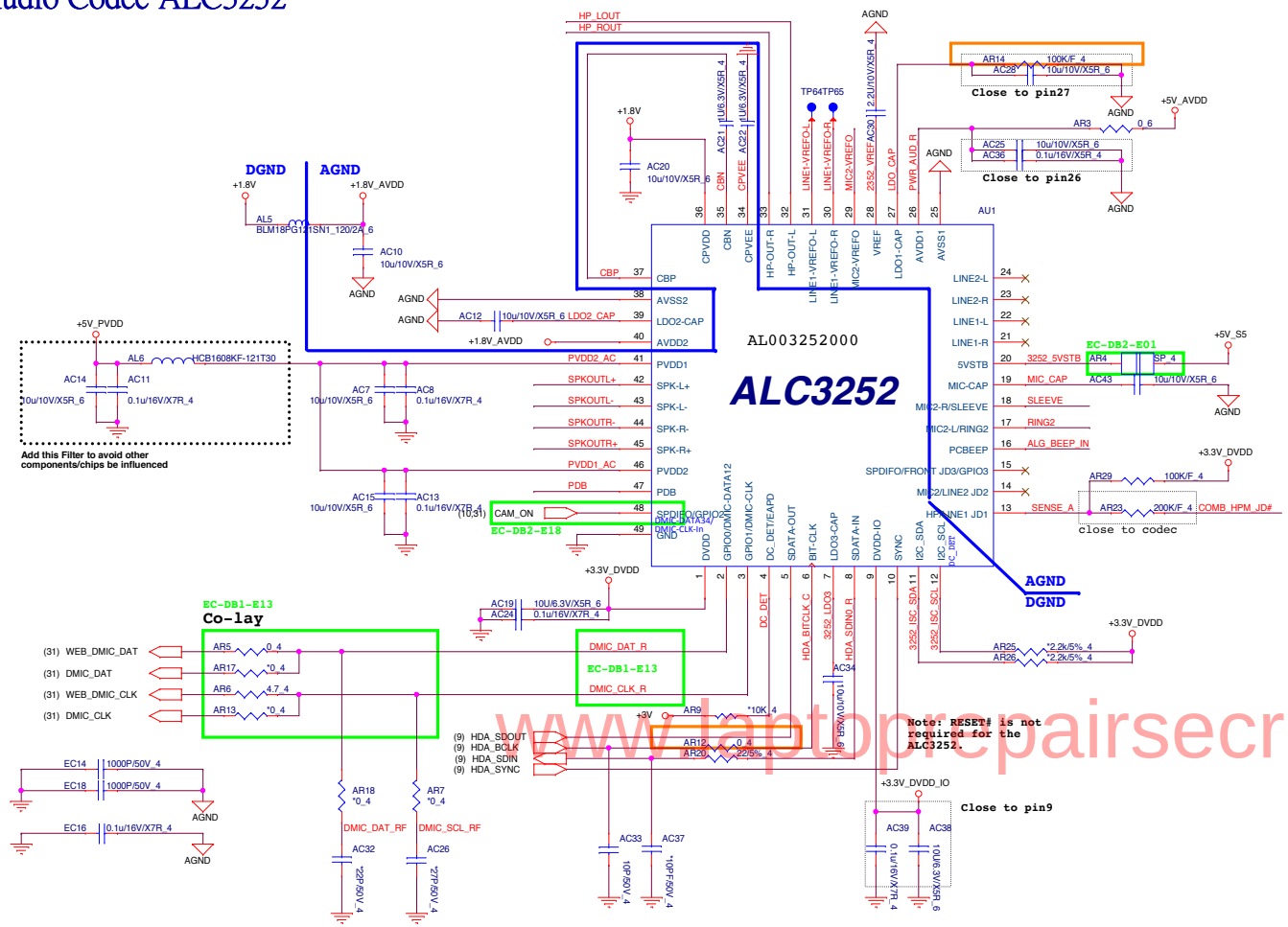
HP Restricted Secret

Quanta Computer Inc.

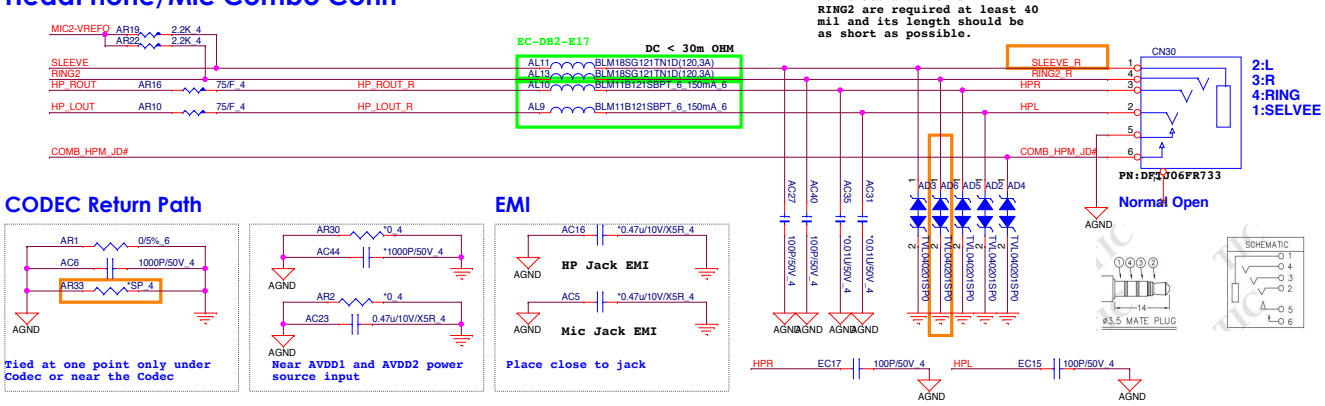
Project: HP-SAIPAN

Title		
HDMI		
Size	Document Number	Rev
	--	A
Page Modified: Thursday, December 17, 2015		Sheet 26 of 61

Audio Codec ALC3252



HeadPhone/Mic Combo Conn

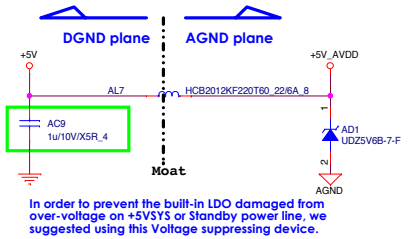


CODEC Return Path

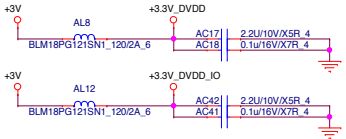
EMI

(23,26,31,36,39,46,47,48,49,50,53,55) +5V
(5,9,10,11,12,13,23,25,28,30,32,34,37,38,39,41,42,43,45,46,47,54,55) +3V_S5
(9,10,11,12,13,14,15,16,17,18,19,22,24,25,26,28,29,30,31,34,35,36,38,42,44,46,47,48,53,54,55) +3V

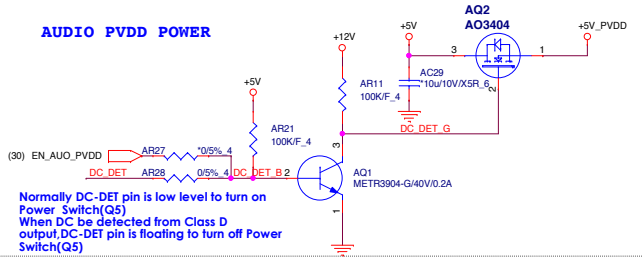
AUDIO AVDD POWER



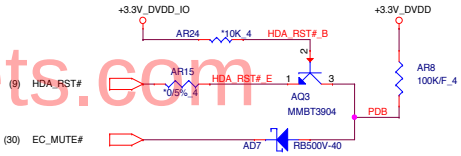
AUDIO DVDD/DVDD_IO POWER



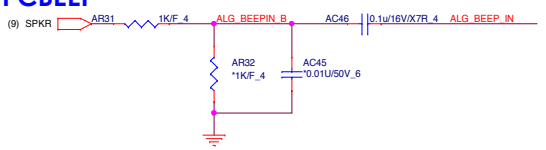
AUDIO PVDD POWER



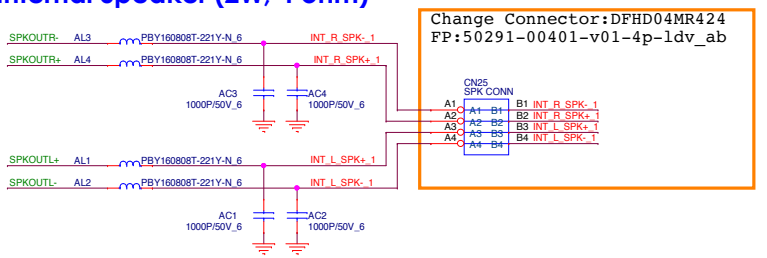
EC MUTE



PCBEEP



Internal Speaker (2W, 4 ohm)



Quanta Computer Inc.	
Project: HP-SAIPAN	
Title: Audio ALC3228-CG	
Size:	Document Number: -- Rev: A
Page Modified: Thursday, December 17, 2015	Sheet 27 of 61

LAN (RTL8161GSH) 10/100/1000

R412 value should be 2.49K (1%) for all application.

RTL8161GSH-CG

3V_LAN

EVDD10/AVDD33_REG trace width >40mils

Close to Pin32

Close to Pin11

Close to Pin23

EVDD10/N780946/REGOUT trace width >60mils

Close to PIN3, 8, 22, 30

C367,C368 Close to PIN22

X'tal 25MHz

LAN Conn

EC-DB2-E19

EC-DB2-E21

BK: reserve

HP Restricted Secret

Quanta Computer Inc.

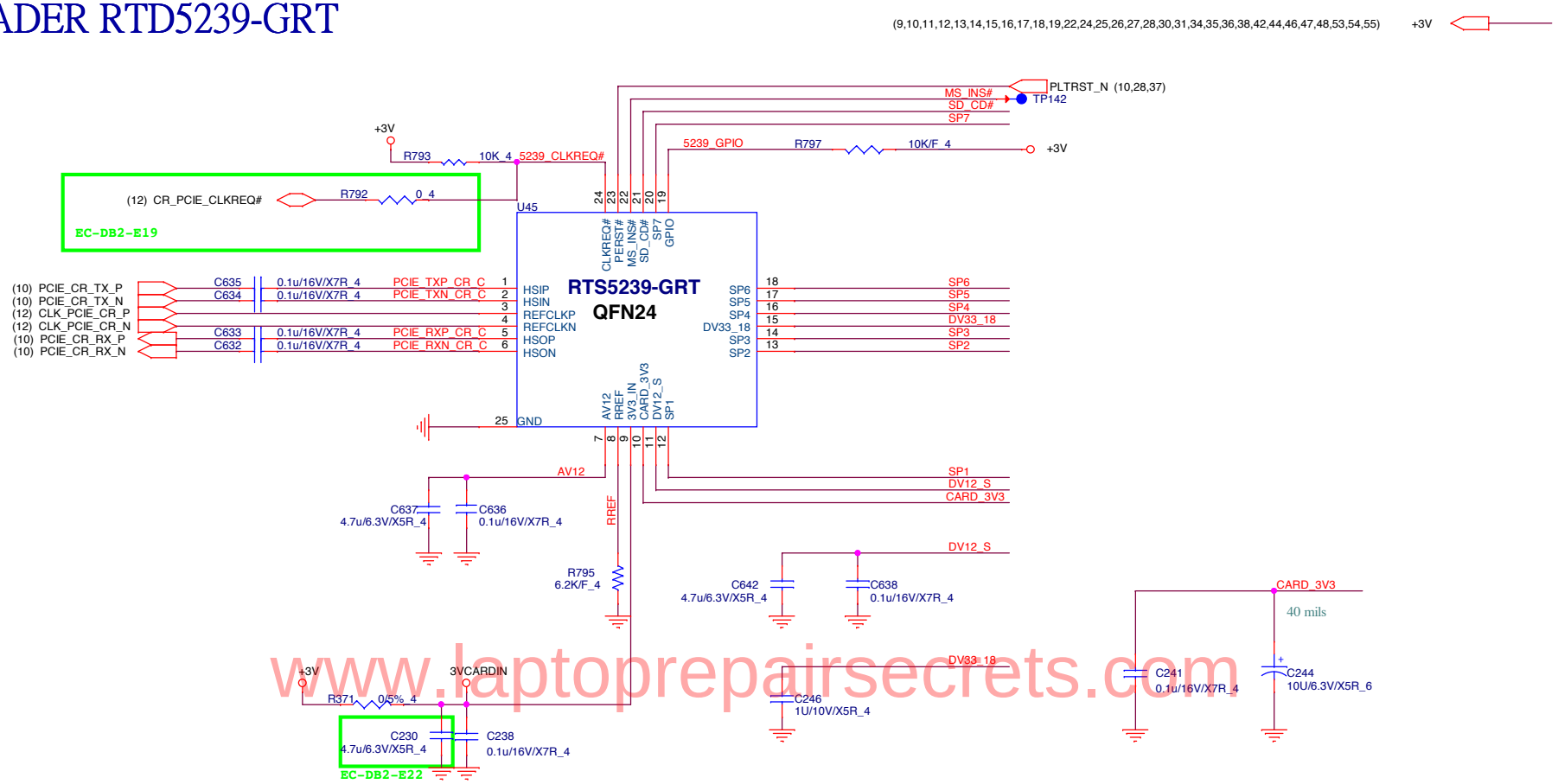
Project: HP-SAIPAN

Title: RTL8161/RJ45

Size: Document Number: — Rev: A

Page Modified: Thursday, December 17, 2015 Sheet 28 of 61

CARD READER RTD5239-GRT



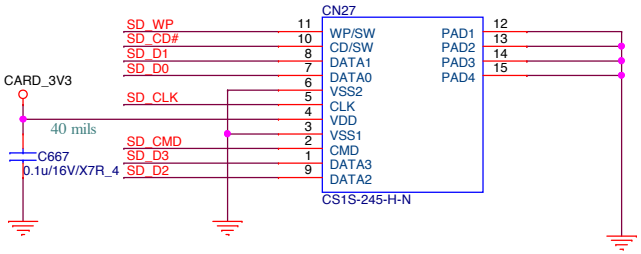
EMI EC-DB2-E23

SD_D1	C664	*5.6P/16V_4
SD_D0	C665	*5.6P/16V_4
SD_CLK	C666	4.7P/50V_4
SD_D3	C668	*5.6P/16V_4
SD_D2	C669	*5.6P/16V_4

SD damping resistor

SP1	R805	33_4	SD_D1
SP2	R806	33_4	SD_D0
SP3	R807	33_4	SD_CLK
SP4	R810	33_4	SD_CMD
SP5	R808	33_4	SD_D3
SP6	R809	33_4	SD_D2
SP7	R796	33_4	SD_WP

SD connector



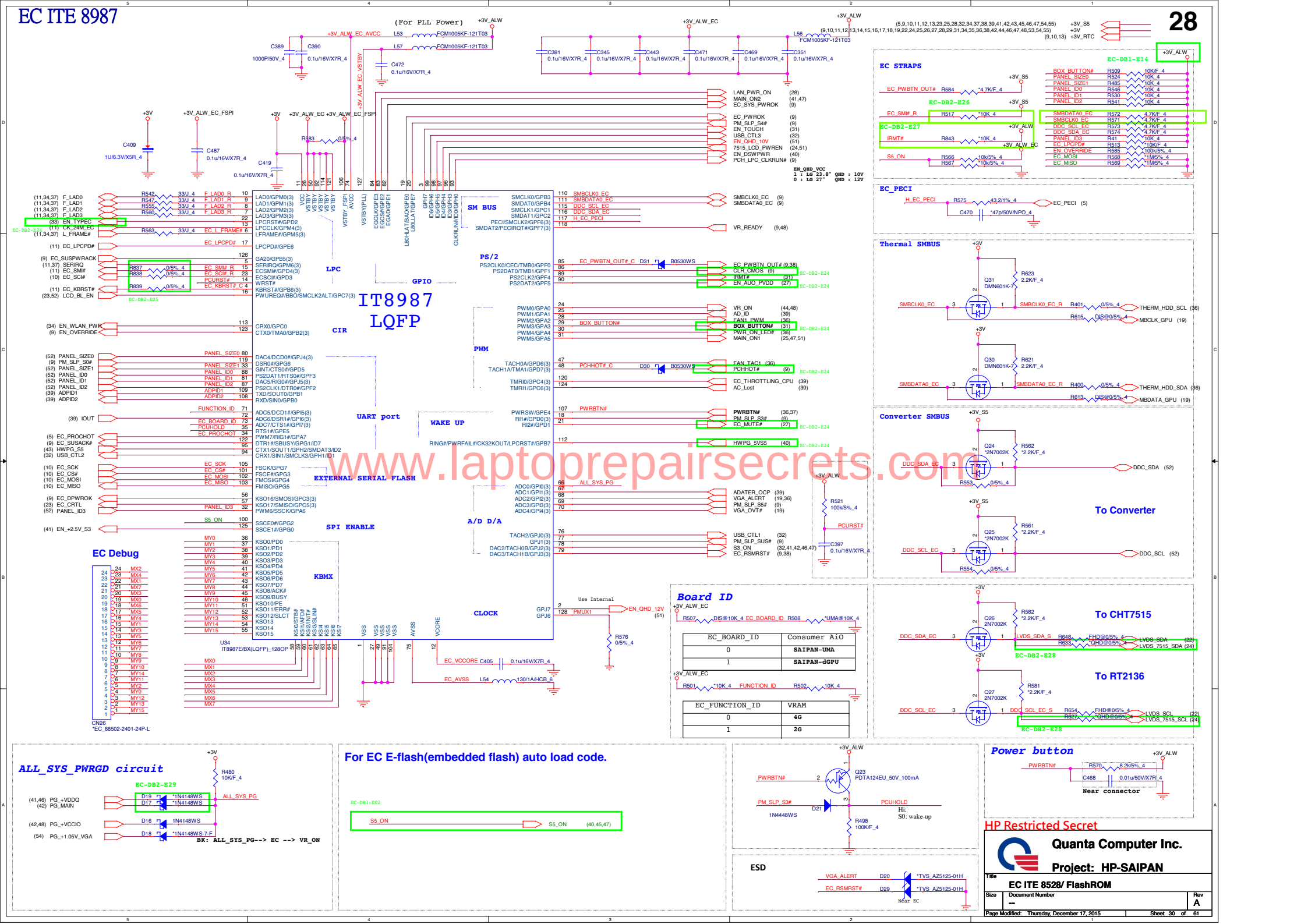
HP Restricted Secret

Quanta Computer Inc.

Project: HP-SAIPAN

Title: Card Reader (RTS5239)		
Size	Document Number: --	Rev: A
Page Modified: Thursday, December 17, 2015		Sheet 29 of 61

EC ITE 8987



(Optional 1: 3DCAM+DMIC)

3D CAM

3D CAM Module	
#	Description
1	GND
2	USB3_TX-
3	USB3_TX+
4	GND
5	USB3_RX-
6	USB3_RX+
7	GND
8	FW_UPDATE
9	5V +/- 5%
10	5V +/- 5%

EC-DB2-E34

Depth + Color = 0.366A
Design = 0.4A

(10,27) CAM_ON — CAM_ON — U32 (EN, OC#, GND, IN, OUT) G524B1T11U — +5V_S5 — C370 1U/6.3V/X5R_4 — C380 10u/6.3V_6 — 20 mil — +5V_CAM

Follow CRB IVCAM

+5V_CAM — D44 *TVL040201SP0 — C53 0.1u/16V/X7R_4 — CAM_DET#

(11) USB3_CAM_RX4N — USB3_CAM_RX4N_C — CN5
(11) USB3_CAM_RX4P — USB3_CAM_RX4P_C

(11) USB3_CAM_TX4N — C70 0.1u/16V/X7R_4 — USB3_CAM_TX4N_R — R55 0/5%_4 — *90ohm_400mA — CML1 — USB3_CAM_TX4N_C
(11) USB3_CAM_TX4P — C69 0.1u/16V/X7R_4 — USB3_CAM_TX4P_R — R54 0/5%_4 — USB3_CAM_TX4P_C

(11) CAM_FW_UPDATE# — CAM_FW_UPDATE#

+3V — R45 *10K/J_4 — R46 *10K/J_4 — CAM_FW_UPDATE#
CAM_DET# — R47 *0_4 — EC-DB1-E17 — +3.3V_CCD — CN4

3D_CAM DFHS10FR068 50463-0104a-001-10pin

DMIC

(27) DMIC_DAT — L2 BLM15AG121SN1D — DMIC_DAT_C — C38 4.7U/10V_6
(27) DMIC_CLK — L3 BLM15AG121SN1D — DMIC_CLK_C
(11) DMIC_DET# — DMIC_DET#

DMIC_DAT_C — C41 100p/50V/NPO_4
DMIC_CLK_C — C52 100p/50V/NPO_4
DMIC_DET# — C49 220p/50V/X7R_4

SMD/Wire/6P_AIO

ESD for DMIC

EC-DB1-E17

U3 (CH1, CH4, Vn, Vp, CH2, CH3) TVL ST23 04 AD0
DMIC_DAT_C — +3.3V_CCD
DMIC_DET# — DMIC_CLK_C

ESD for 3D CAM

U5 TVW DF10 04 AD0
USB3_CAM_RX4N — USB3_CAM_RX4N
USB3_CAM_RX4P — USB3_CAM_RX4P
GND_3/8
USB3_CAM_TX4N_C — USB3_CAM_TX4N_C
USB3_CAM_TX4P_C — USB3_CAM_TX4P_C

EC-DB2-E31

USB protection diodes for ESD.
as close as possible to USB connector pins.

(Optional 2: WEBCAM+DMIC)

+3V — F3 *POLY_SW 6V/1.1A — +3.3V_CCD — D15 TVL040201SP0

20 mil
Normal = 0.135A
Design = 0.3A

CAM_ON — U31 (EN, OC#, GND, IN, OUT) G524B1T11U Energy star — EC-DB2-E34
C342 1U/6.3V/X5R_4
C333 10u/6.3V_6 — C334 *1000P/50V/4 — +3.3V_CCD

HD

Connector1: ACES 50376-00601-001

Pin	Definition
1	VCC_3.3V
2	D-
3	D+
4	MDATA
5	MCLK
6	GND

IR (Reverse for safety)

Connector2: ACES 50376-00601-001

Pin	Definition	MB
1	VCC_3.3V	16
2	D-	15
3	D+	14
4	IR_3.3V	13
5	IR_GND	11
6	DGND	10

+3.3V_CCD — CN2

(10) USB2_CAM_9N — L7 — USB2_CAM_9N_C
(10) USB2_CAM_9P — USB2_CAM_9P_C — 90ohm_400mA

EC-DB2-E30

(27) WEB_DMIC_DAT — L6 BLM15AG121SN1D — WEB_DMIC-DATA_C
(27) WEB_DMIC_CLK — L5 4.7_4 — WEB_DMIC-CLK_C
(11) CAM_DET# — R48 1K_4 — CAM_DET#_C
(30) BOX_BUTTON# — R512 1K_4 — BOX_BUTTON#_C
(10) USB2_IR_5P — L1 — USB2_IR_5P_C
(10) USB2_IR_5N — USB2_IR_5N_C — 90ohm_400mA

HD CAM
IR CAM

HEADER_16P_P0.8

ESD IR CAM

USB2_IR_5P_C — D3 TVUFB0201AC0
USB2_IR_5N_C — D2 TVUFB0201AC0
CAM_DET#_C — D5 *TVL040201SP0
BOX_BUTTON#_C — D43 *TVL040201SP0

ESD HD CAM

EC-DB2-E31

U4 (CH1, CH4, Vn, Vp, CH2, CH3) TVL ST23 04 AD0
WEB_DMIC-CLK_C — WEB_DMIC-DATA_C — +3.3V_CCD
USB2_CAM_9N_C — USB2_CAM_9P_C

Touch Panel

(27,32,33,36,39,40,41,43,44,45,46,47,54)
(9,10,11,12,13,14,15,16,17,18,19,22,24,25,26,27,28,29,30,34,35,36,38,42,44,46,47,48,53,54,55)
(23,26,27,36,39,46,47,48,49,50,53,55)
+5V_S5 +3V +5V

+5V_S5 — F1 POLY_8V/1.1A — +5V_TOUCH — D4 TVS_AZ5125-01H

(30) EN_TOUCH — U33 (EN, OC#, GND, IN, OUT) *G524B1T11U Energy star — EC-DB2-E34
C372 *1U/6.3V/X5R_4 — C365 *10u/6.3V_6 — +5V_TOUCH

60 mil
Normal = 1A
Design = 1.5A

+5V_TOUCH — CN7

(10) USB2_TCH_8N — L4 90ohm_400mA — USB2_TCH_8N_C
(10) USB2_TCH_8P — USB2_TCH_8P_C

(9) TP_DETECT# — R56 1K/F_4 — TP_DETECT#_R — TOUCH_MODULE

C369 2.2U/10V/X5R_4 — C47 0.1u/16V/X7R_4

U6 (CH1, CH4, Vn, Vp, CH2, CH3) TVL ST23 04 AD0
TP_DETECT#_R — +5V_TOUCH
USB2_TCH_8N_C — USB2_TCH_8P_C
+5V_TOUCH — EC1 *2200P/50V_4

LEDs

DC_IN LED

White
R841 0/5%_4 — LED1 — LED_SMD(2P)WHI — POWER_LED — R383 *1k/5%_4 — +VIN — R377 750/1%_4 — +5V_ALW

IRMT# — R842 1K/F_4 — Q58 *MMBT3906
EC-DB2-E32

POWER_LED — D45 *TVL040201SP0
EC-DB2-E33

SATA LED

White
LED2 — LED_SMD(2P)WHI
HDD_LED#-D2 — HD_LED — R422 300_6 — +5V

(10) PCH_SATA_LED_# — R412 1K/F_4 — HDD_ON_LED#_B — Q16 MMBT3906
(30) IRMT# — R840 *1K/F_4
EC-DB2-E32

EA

WEB_DMIC-CLK_C — C674 22P/50V_4

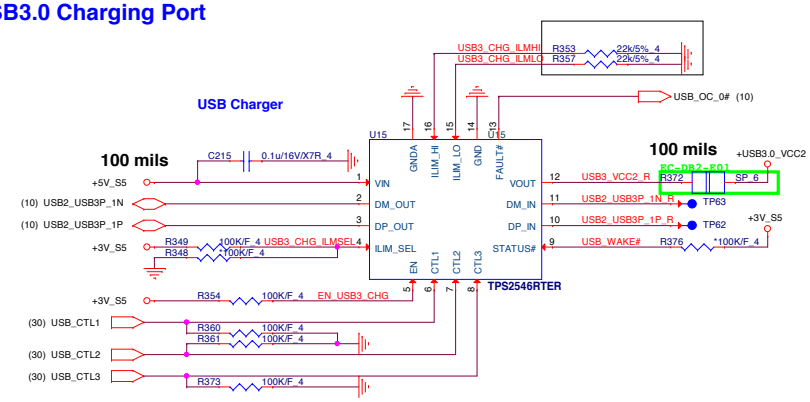
HP Restricted Secret

Quanta Computer Inc.
Project: HP-SAIPAN

Title: eDP-LVDS_RTD2136N		
Size	Document Number: –	Rev: A
Page Modified: Thursday, December 17, 2015		Sheet 31 of 61

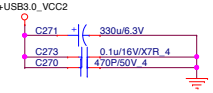
USB PORT

USB3.0 Charging Port



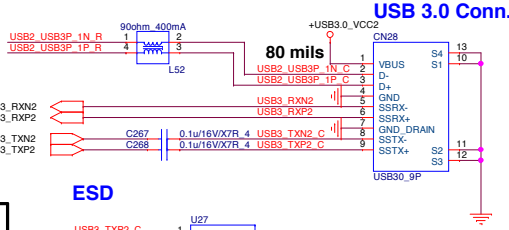
SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by BIOS

POWER STATE	TPS2546 CHARGING MODE	CTRL1	CTRL2	CTRL3	ILIM
S0	CDP LOAD DETECTION WITH ILIM_LO +60MA THRESHOLDS OR IF A BC1.2 PRIMARY DETECTION OCCURS	1	1	1	1
S3	AUTO MODE, LOAD DETECTION WITH POWER WAKE THRESHOLDS	0	1	1	1
S4/S5	AUTO MODE, KEYBOARD/ MOUSE WAKE-UP, LOAD DETECTION WITH ILIM_LO +60MA THRESHOLDS	0	0	1	1

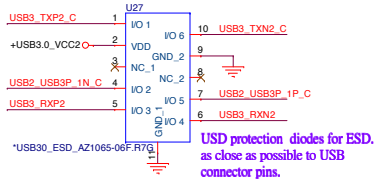


(5,9,10,11,12,13,23,25,28,30,34,37,38,39,41,42,43,45,46,47,54,55) +3V_S5
(27,31,33,36,39,40,41,43,44,45,46,47,54) +5V_S5

USB 3.0 Conn.



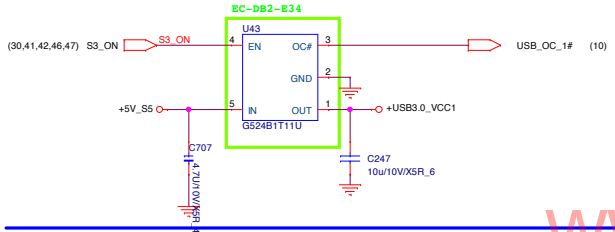
ESD



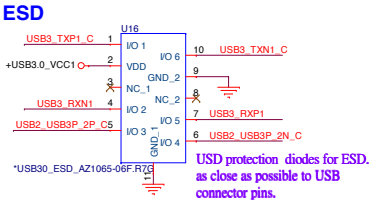
USD protection diodes for ESD. as close as possible to USB connector pins.

USB3.0 PORT

USB3.0 Power Switch

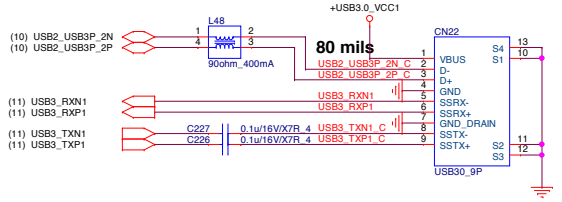


ESD



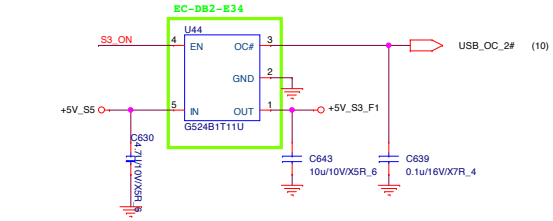
USD protection diodes for ESD. as close as possible to USB connector pins.

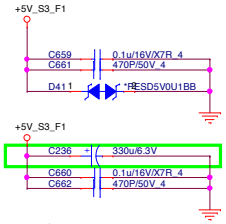
USB3.0 Conn



USB2.0 X 2

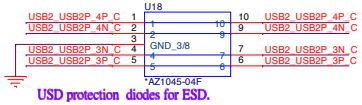
USB3.0 Power Switch





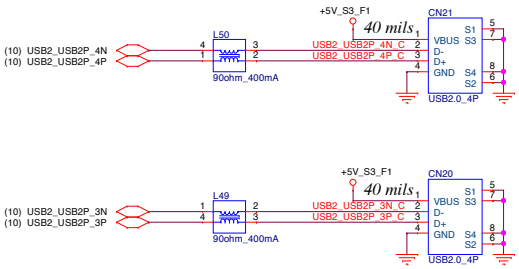
Layout:
1. All caps Near to Connector
2. Place D40 near CN21 and CN22

ESD



USD protection diodes for ESD.
as close as possible to USB connector pins.

USB2.0 Conn



HP Restricted Secret

Quanta Computer Inc.

Project: HP-SAIPAN

Title: USB2.0/USB3.0 Conn

Size: | Document Number: -- | Rev: A

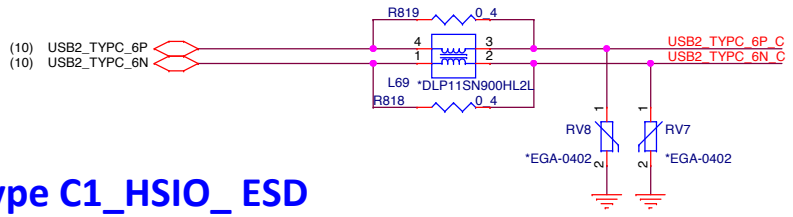
Page Modified: Thursday, December 17, 2015 | Sheet 32 of 61

USB TYPE-C

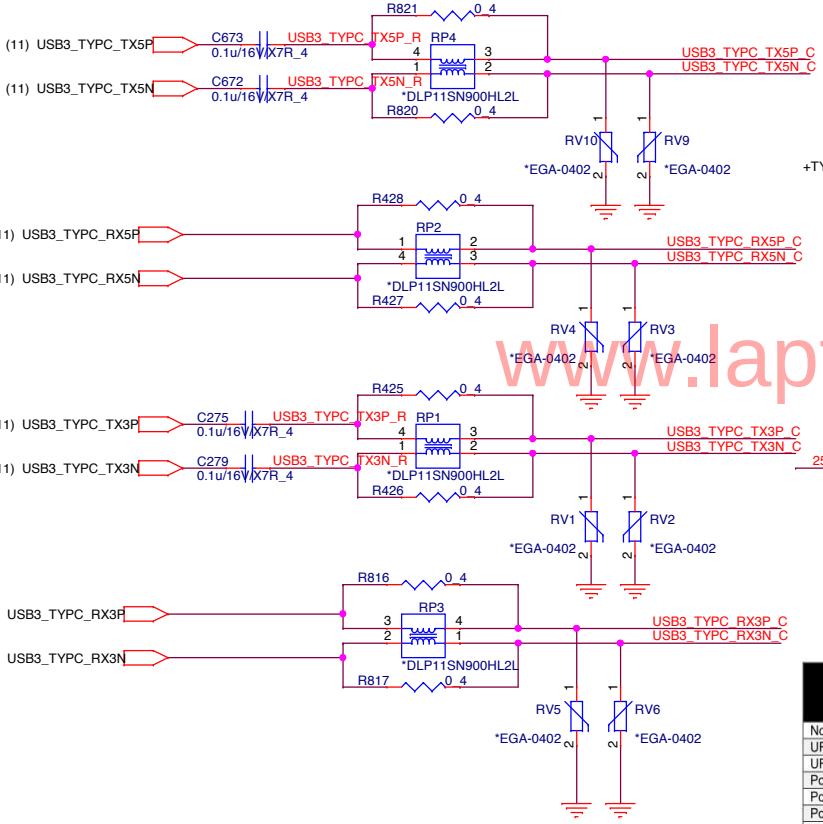
(5,9,10,11,12,13,23,25,28,30,32,34,37,38,39,41,42,43,45,46,47,54,55) +3V_S5
(27,31,32,36,39,40,41,43,44,45,46,47,54) +5V_S5

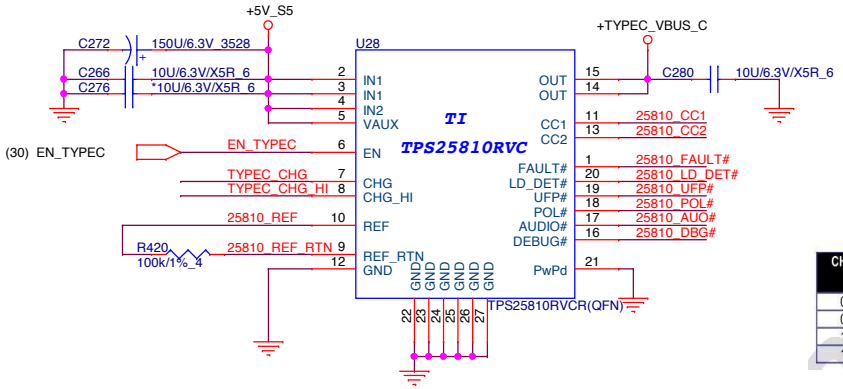
33

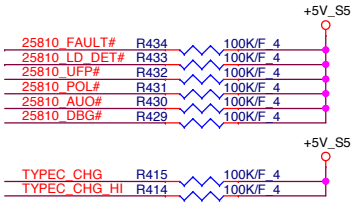
USB2.0 ESD



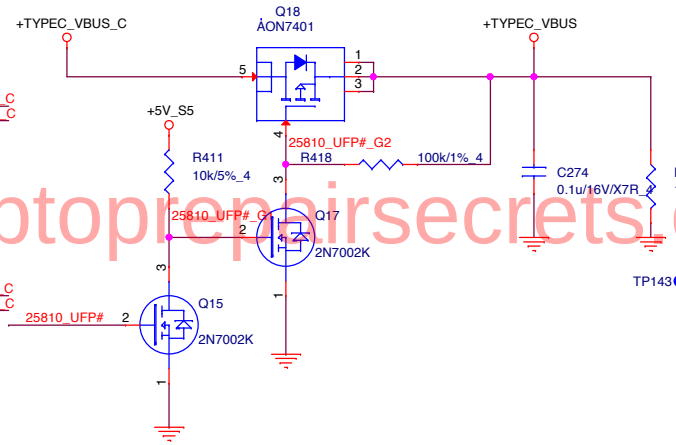
Type C1_HSIO_ ESD

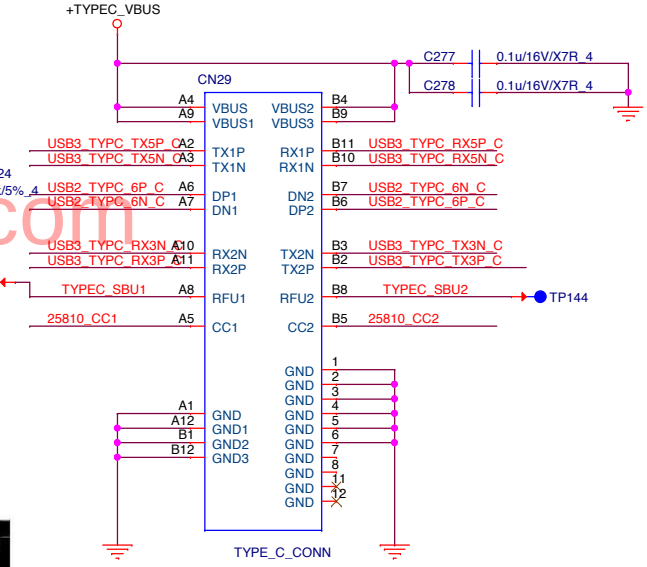






CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A





TPS25810 Port	CC1	CC2	TPS25810 Response					
			OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

HP Restricted Secret

Quanta Computer Inc.

Project: HP-SAIPAN

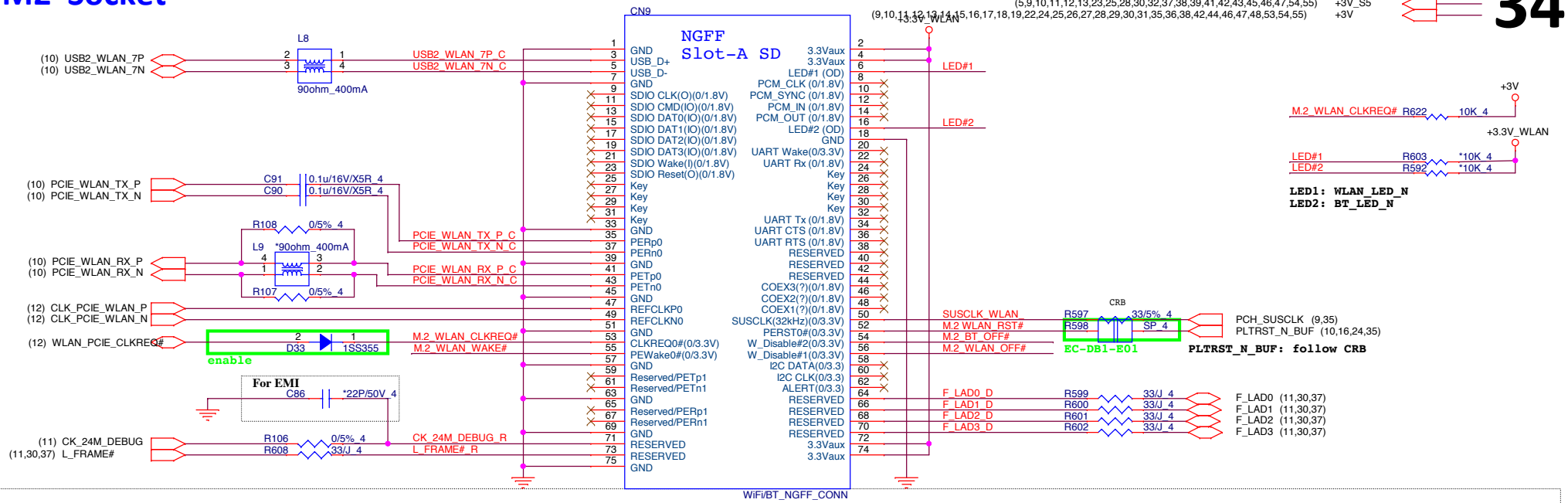
Title: USB TYPE-C

Size | Document Number -- | Rev A

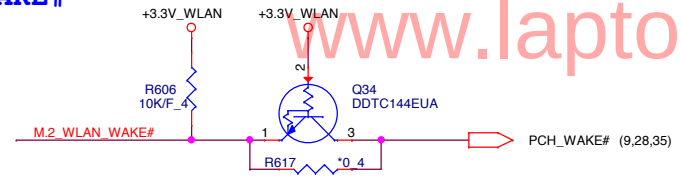
Page Modified: Thursday, December 17, 2015 | Sheet 33 of 61

NGFF M2 Socket

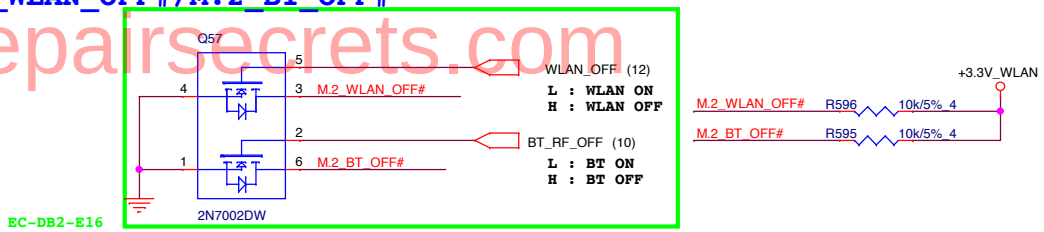
H=9.0



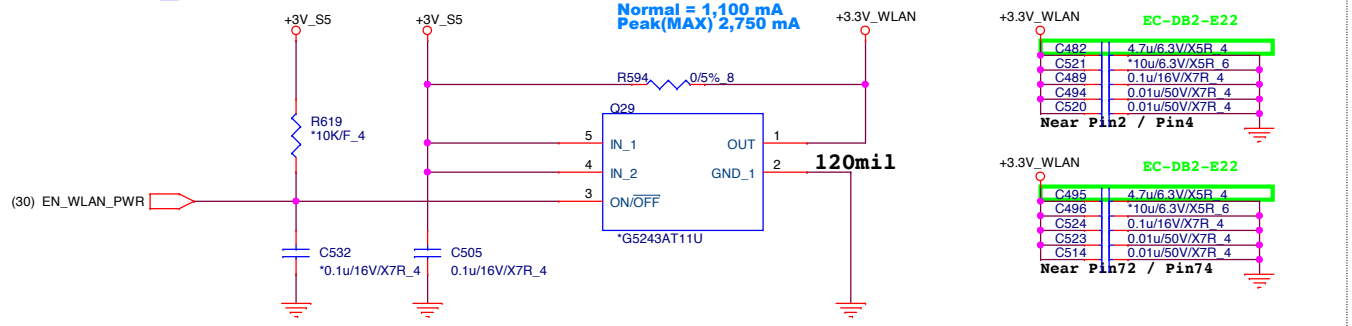
M.2 WLAN WAKE#



M.2_WLAN_OFF#/M.2_BT_OFF#



NGFF M2_power(S5)



HP Restricted Secret

Quanta Computer Inc.

Project: HP-SAIPAN

Title		
NGFF M.2 WLAN		
Size	Document Number	Rev
	--	B
Page Modified: Thursday, December 17, 2015		Sheet 34 of 61

NGFF M2 Socket

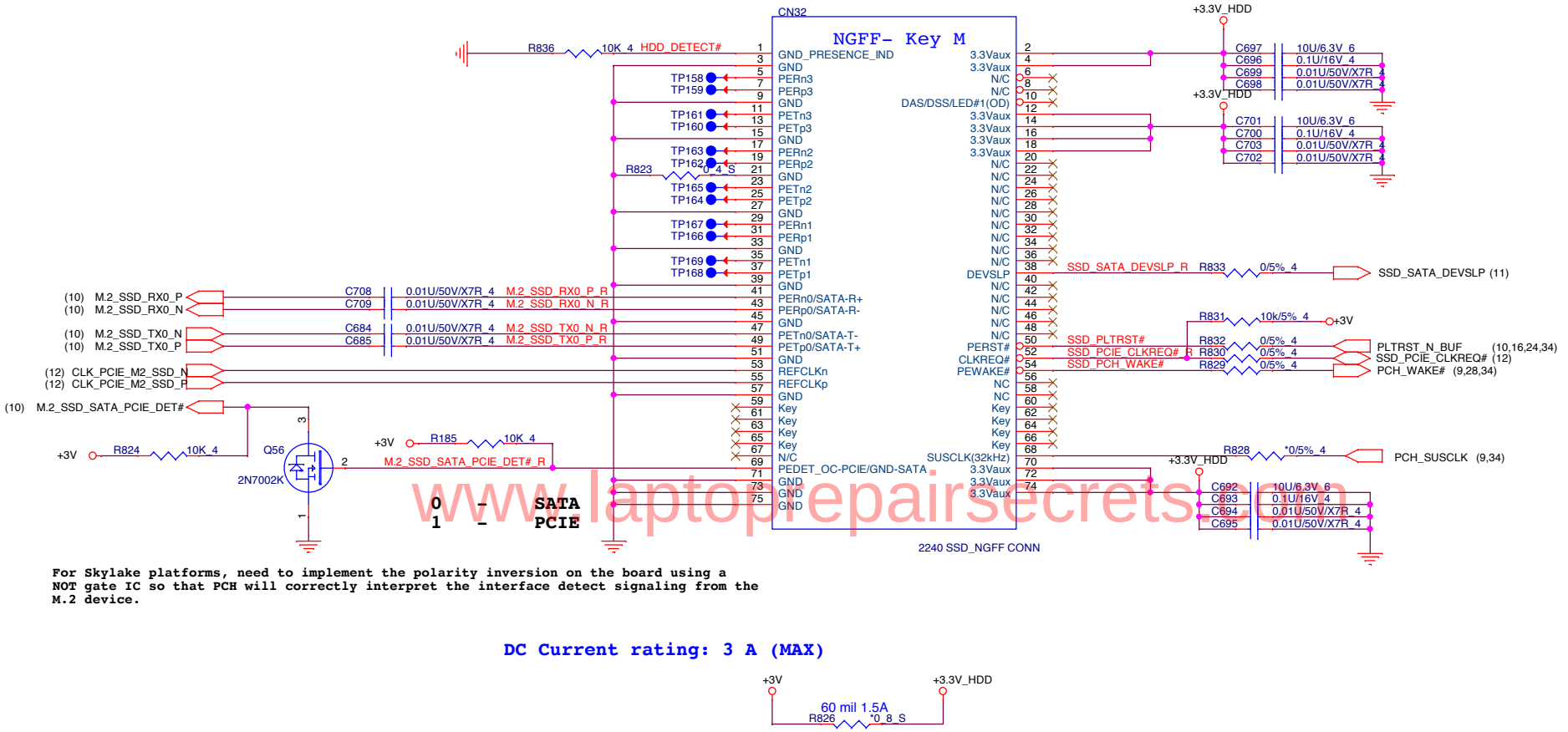
(5,9,10,11,12,13,23,25,28,30,32,34,37,38,39,41,42,43,45,46,47,54,55) +3V_S5
(9,10,11,12,13,14,15,16,17,18,19,22,24,25,26,27,28,29,30,31,34,36,38,42,44,46,47,48,53,54,55) +3V

35

60 mil 1.5A

EC-DB2-E36

H=9.0



For Skylake platforms, need to implement the polarity inversion on the board using a NOT gate IC so that PCH will correctly interpret the interface detect signaling from the M.2 device.

DC Current rating: 3 A (MAX)

HP Restricted Secret

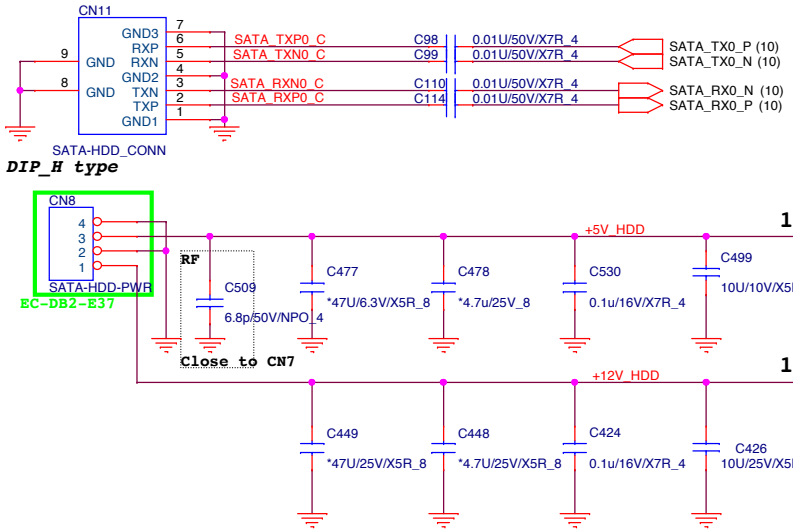
Quanta Computer Inc.

Project: HP-SAIPAN

Title		
NGFF M.2 WLAN		
Size	Document Number	Rev
	--	B
Page Modified: Thursday, December 17, 2015		Sheet 35 of 61

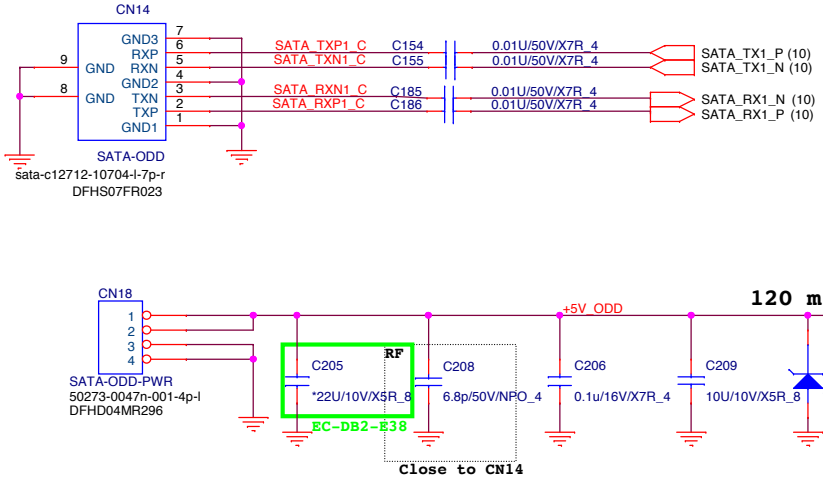
SATA HDD

HDD SATA Conn.



SATA ODD

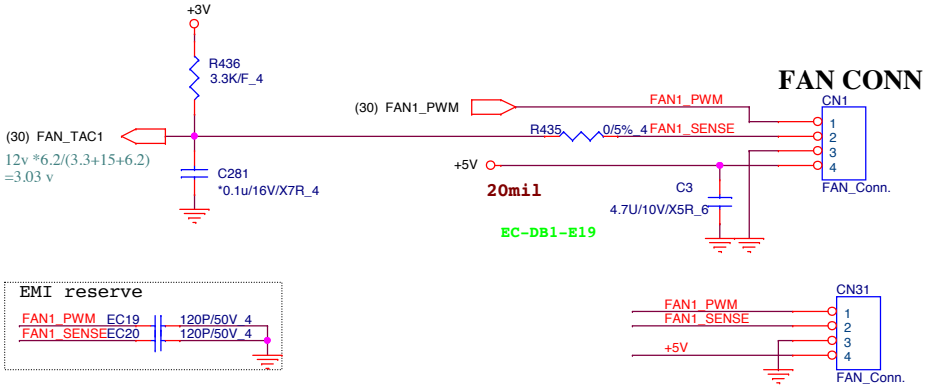
ODD SATA Conn.



SYSTEM FAN

(9,10,11,12,13,14,15,16,17,18,19,22,24,25,26,27,28,29,30,31,34,35,38,42,44,46,47,48,53,54,55) +3V
(27,31,32,33,39,40,41,43,44,45,46,47,54) +5V_S5
(23,26,27,31,39,46,47,48,49,50,53,55) +5V
(27,47,51,55) +12V

36

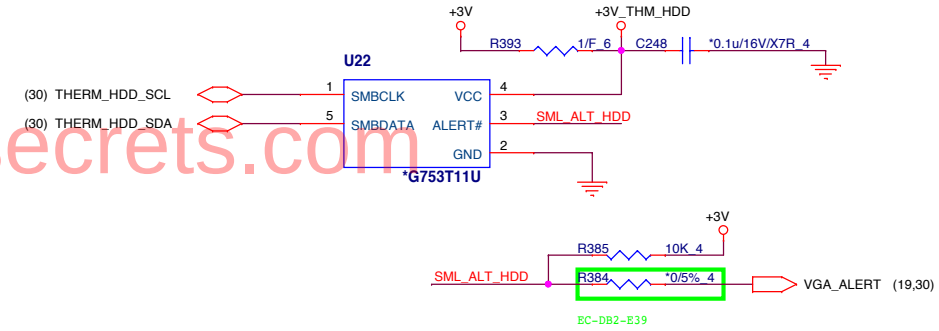


Ambient SENSOR

Reserved

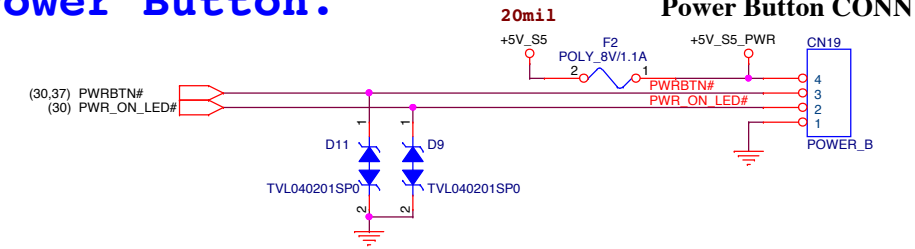
Slave Adress

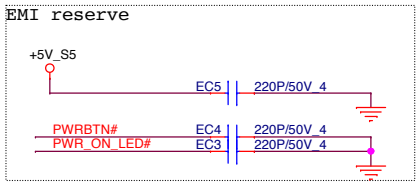
A6	A5	A4	A3	A2	A1	A0
1	0	0	1	0	0	0



Power Button.

Power Button CONN





HP Restricted Secret

Quanta Computer Inc.

Project: HP-SAIPAN

Title: FAN/HDD/ODD/HDD CONN.

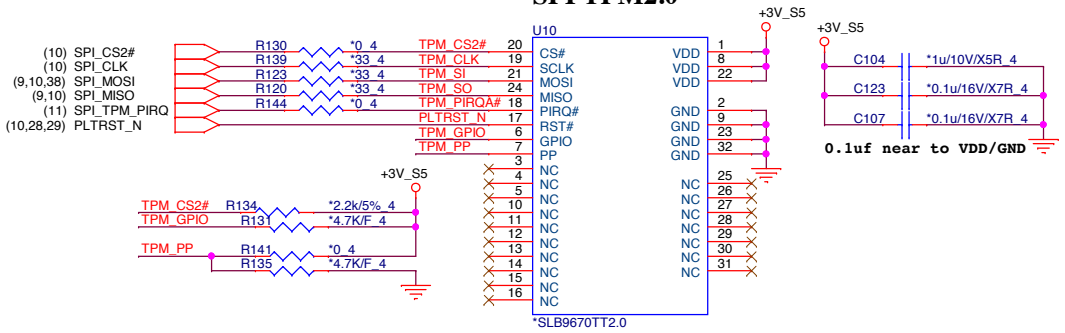
Size: | Document Number: -- | Rev: A

Page Modified: Thursday, December 17, 2015 | Sheet 36 of 61

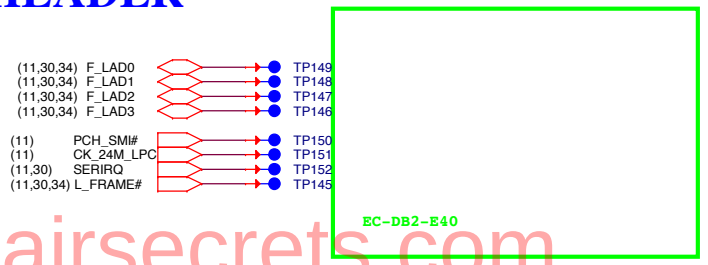
TPM2.0

(5,9,10,11,12,13,23,25,28,30,32,34,38,39,41,42,43,45,46,47,54,55) +3V_S5
(9,10,11,12,13,14,15,16,17,18,19,22,24,25,26,27,28,29,30,31,34,35,36,38,42,44,46,47,48,53,54,55) +3V
(23,26,27,31,36,39,46,47,48,49,50,53,55) +5V
(5,7,9,38,46,47,48) +VCCST_VCCPLL

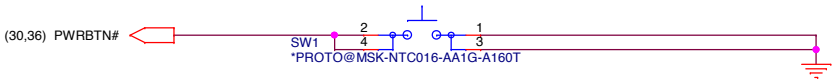
SPI TPM2.0



LPC HEADER



SW1 For Debug.MP will remove it.



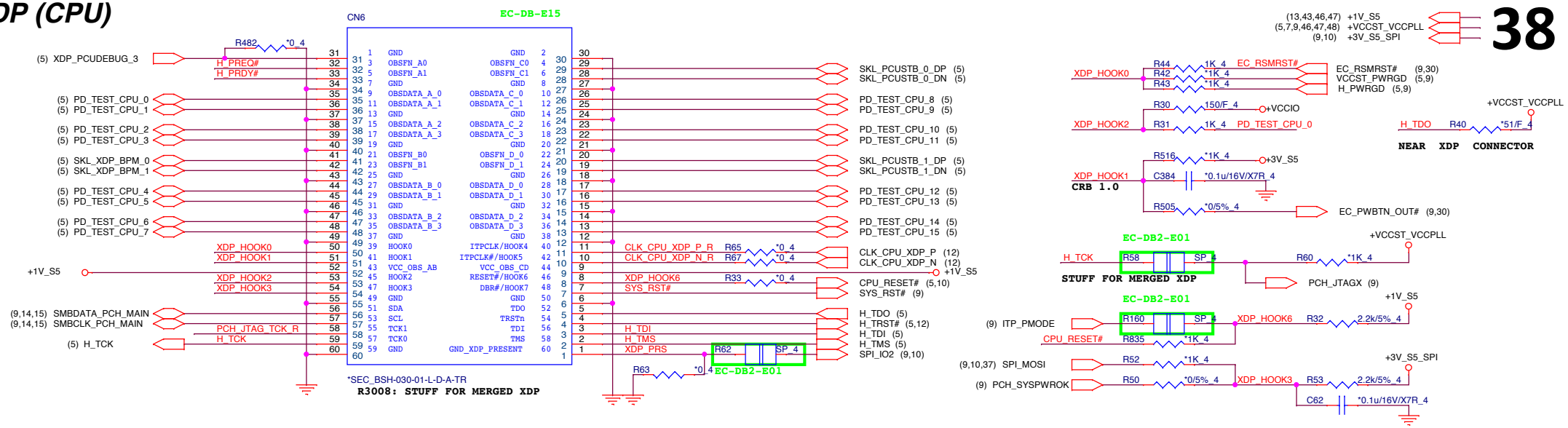
HP Restricted Secret

Quanta Computer Inc.

Project: HP-SAIPAN

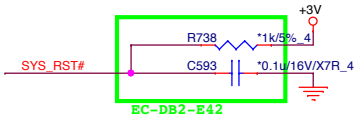
Title: Debug /LPC Header/TPM		
Size	Document Number: --	Rev: A
Page Modified: Thursday, December 17, 2015		Sheet 37 of 61

XDP (CPU)

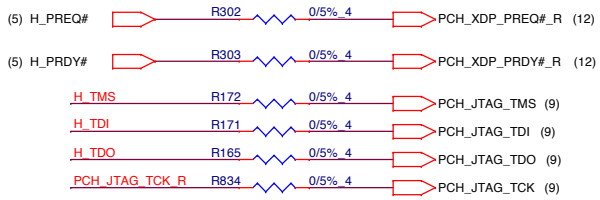


XDP (PCH)

EC-DB2-E41



MERGED XDP



stuff for merged XDP

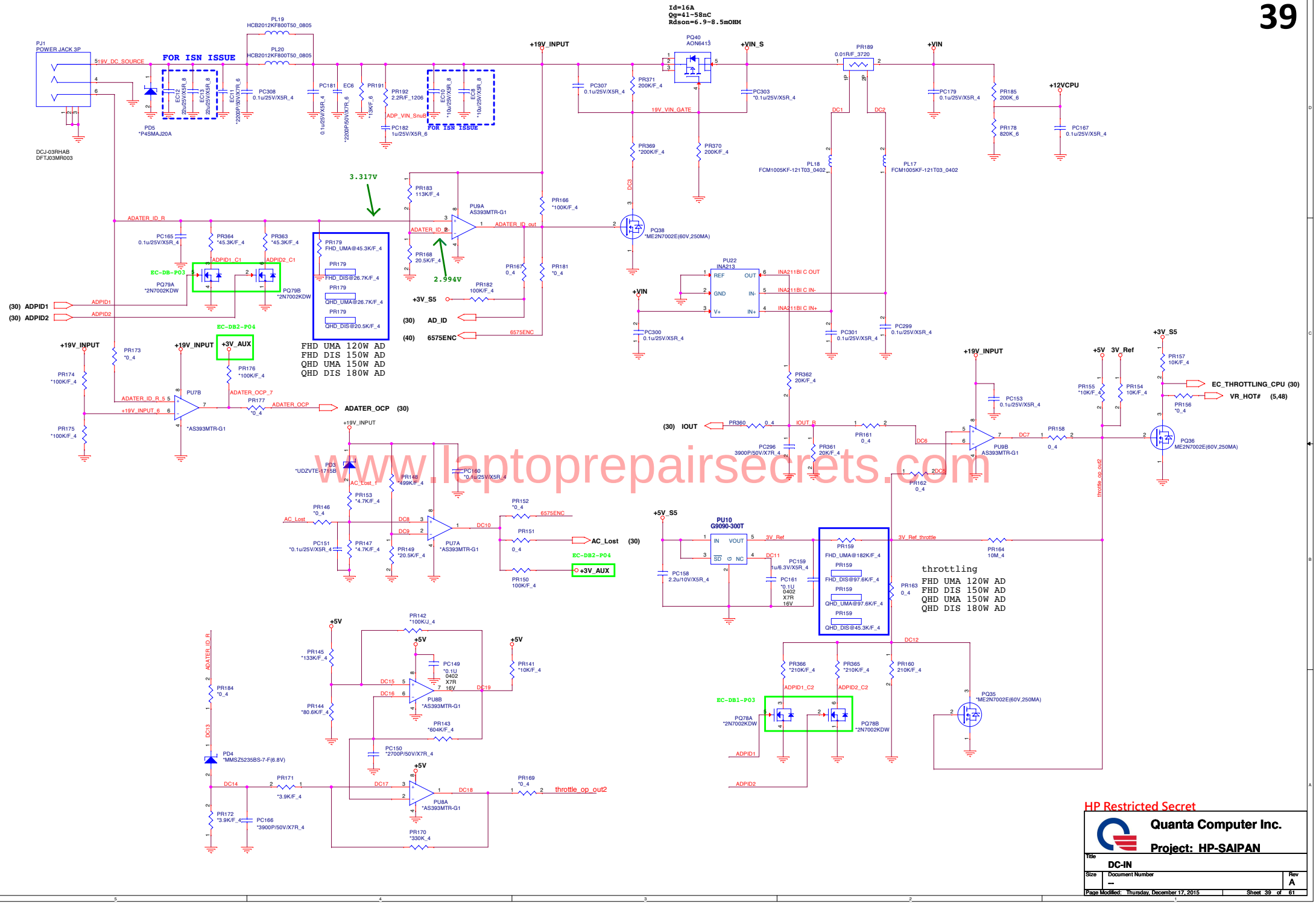
Quanta Computer Inc.

Project: HP-SAIPAN

Title: XDP DEBUG

Size: | Document Number: -- | Rev: A

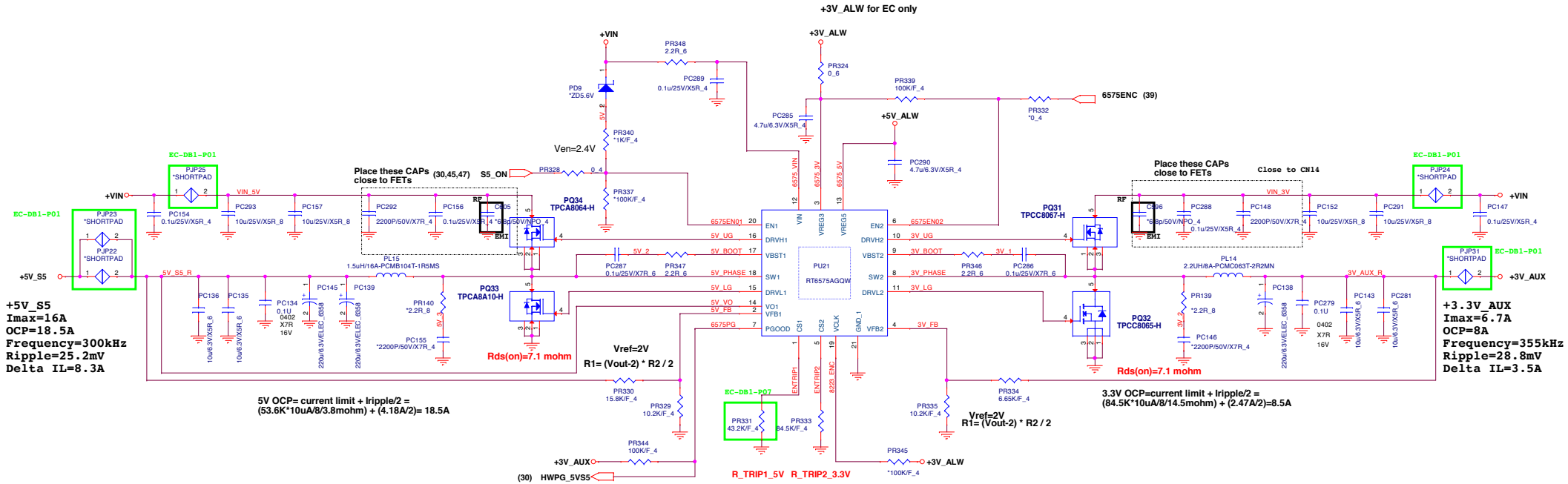
Page Modified: Thursday, December 17, 2015 | Sheet 38 of 61



Quanta Computer Inc.

Project: HP-SAIPAN

Title	DC-IN	
Size	Document Number	Rev
	--	A
Page Modified: Thursday, December 17, 2015		Sheet 39 of 61



L/S Mosfet parameter

MOSFET	Package	ID (Ta=25C)	Rds_on_max
TPCC8065-H	DFN3x3	13A	14.5m
TPCA8A10-H	DFN5x6	40A	3.8m

Power On sequencing

EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON

Quanta Computer Inc.

Project: HP-SAIPAN

Title: 3V_AUX/5V_S5(RT6575AGQW)

Size: | Document Number: -- | Rev: A

Page Modified: Thursday, December 17, 2015 | Sheet 40 of 61

(31,39,40,42,43,44,46,47,49,50,51,52,53,54,55) +VIN
(7,9,14,15,46,47,55) +VDDQ
(5,9,10,11,12,13,23,25,28,30,32,34,37,38,39,42,43,45,46,47,54,55) +3V_S5
(27,31,32,33,36,39,40,43,44,45,46,47,54) +5V_S5
(14,15,47) +SMDDR_VTERM

+3V_S5 PR29 100K/F_4

(30,46) PG_+VDDQ

+VDDQ asserted after +VCCST_PLL asserted

(30,32,42,46,47) S3_ON

PR23 10k/1%_4
PC22 1u/10V/X5R_4

+0.6V_DDR_VTT
PEAK :0.9A

(5) DDR_VTT_CNTL PR207 0_4
(30,47) MAIN_ON2 PR206 *0_4
PC23 *1u/6.3V/X5R_4
PR205 0_4
(47) DIS_SMDDR_VTERM

TPCA8059-H Rdson = 4.8m Ohms
OCP=Current limit + Iripple/2=(105K*5uA/10/4.8mohm)+ (4.18A/2)=13A

PR50 105K/F_4
PR26 620K/F_4
1P35V_TON

Place these CAPs close to FETs

VIN_8231
EC-DB1-P01 PJP2 *SHORTPAD
+VIN
PC19 2200P/50V/X7R_4
PC190 0.1u/25V/X5R_4
PC13 10u/25V/X5R_8
PC186 10u/25V/X5R_8
PC5 0.1u/25V/X5R_4

EC-DB1-P01 PJP5 *SHORTPAD
VTT
+SMDDR_VTERM
PC49 10u/6.3V/X5R_6

PU1 RT8231BGQW
S3 S5 PGOOD CS TON
VTT VTTSNS VTTGND VTTREF VLDOIN
UGATE BOOT1 PHASE LGATE VDD
LPMB VID PGND FB VDDQ PAD

PQ4 TPCA8064-H
1P35V_UGATE
1P35V_BOOT
PR59 0_6
DDR1
PC47 0.1u/25V/X7R_6
1P35V_PHASE
1P35V_LGATE
1P35V_VDD
+5V_S5
PR41 0_4
PC39 1u/6.3V/X5R_4
PQ8 TPCA8059-H

PL5 1.0uH/18A-PCMC104T-1R0MN
1.35V_S3_R
PJP8 *SHORTPAD
+VDDQ
PJP7 *SHORTPAD
EC-DB1-P01

PR49 *2.2R_8
DDR2
PC30 *2200P/50V/X7R_4
PC53 *390U/2.5V/ELEC_6358
PC54 390U/2.5V/ELEC_6358
PC60 10u/6.3V/X5R_6
PC64 0.1U 0402 X7R 16V

DDR_VTTREF
PR39 100/F_4
1P35V_VTTREF
PC29 0.1U 0402 X7R 16V
PC38 0.033u/50V/X7R_6
1.35V_S3_R
PC48 10u/6.3V/X5R_6
PR51 0_4
+5V_S5
PR38 0_4
1P35V_VDDQ
PR30 7.68K/F_4
PR25 0_4
PR24 10K/F_4

+VDDQ
Imax=9A
OCP=11A
Frequency=400kHz
Ripple=21mV
Delta IL=2.8A

Imax= 0.5A
Pd: 0.4W

+3V_S5 PR304 10K_4
+5V_S5
PC277 1u/6.3V/X5R_4
PU19 G9661-25ADJF12U
VPP PGOOD VEN VO VIN GND GND ADJ NC
PG_+2.5V_S3
+2.5V_S3_P
EC-DB1-P01 PJP20 *SHORTPAD
+2.5V_S3

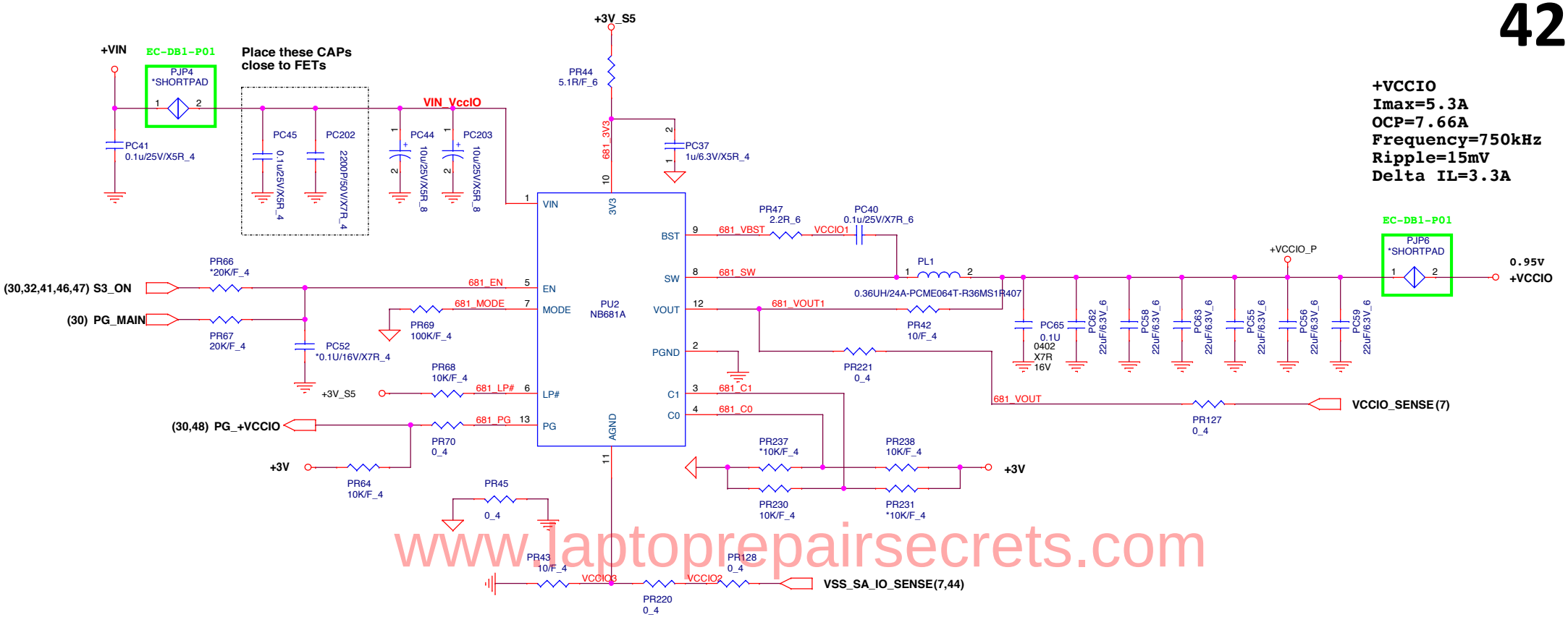
EC-DB1-P01 PJP30 *SHORTPAD
+3V_S5
+2.5V_VIN
PC272 10u/6.3V/X5R_6
(30) EN_+2.5V_S3
PC273 0.1U 0402 X7R 16V
R1 PR307 21.5K/F_4
+2.5V_ADJ
R2 PR305 10K/F_4
PC275 0.1U 0402 X7R 16V
PC269 10U/6.3V/X5R_6
PC271 10U/6.3V/X5R_6

Vout =0.8(1+R1/R2)

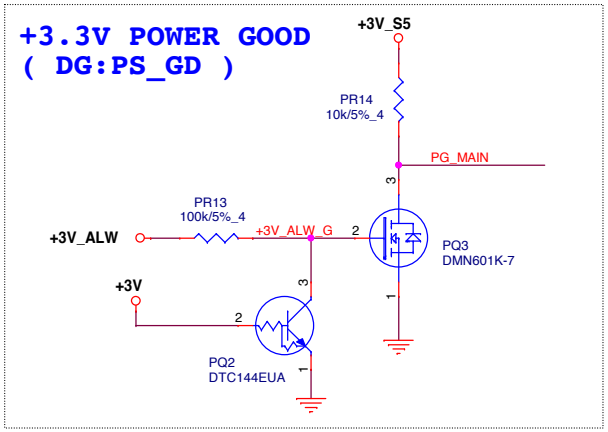
Quanta Computer Inc.
Project: HP-SAIPAN

Title: +VDDQ /SMDDR_VTERM (RT8231BGQW)
Size: Document Number: – Rev: A
Page Modified: Thursday, December 17, 2015 Sheet 41 of 61

+VCCIO
Imax=5.3A
OCP=7.66A
Frequency=750kHz
Ripple=15mV
Delta IL=3.3A



+3.3V POWER GOOD (DG:PS_GD)



MODE M2 (100K to GND)

LP#	C1	C0	Vout
0	X	X	0V
1	0	0	0.8V
1	0	1	0.95V
1	1	0	1V
1	1	1	1.05V

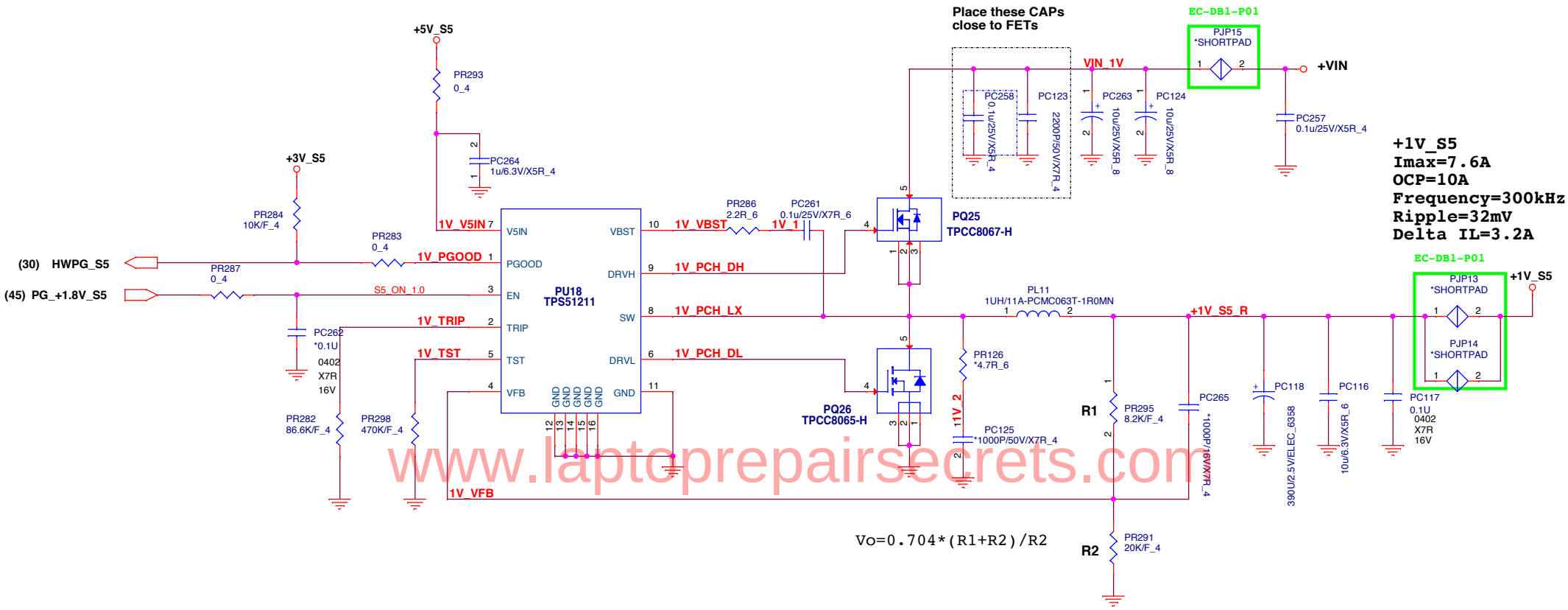
Quanta Computer Inc.

Project: HP-SAIPAN

Title: +VCCIO(NB681)

Size | Document Number: -- | Rev: A

Page Modified: Thursday, December 17, 2015 | Sheet 42 of 61

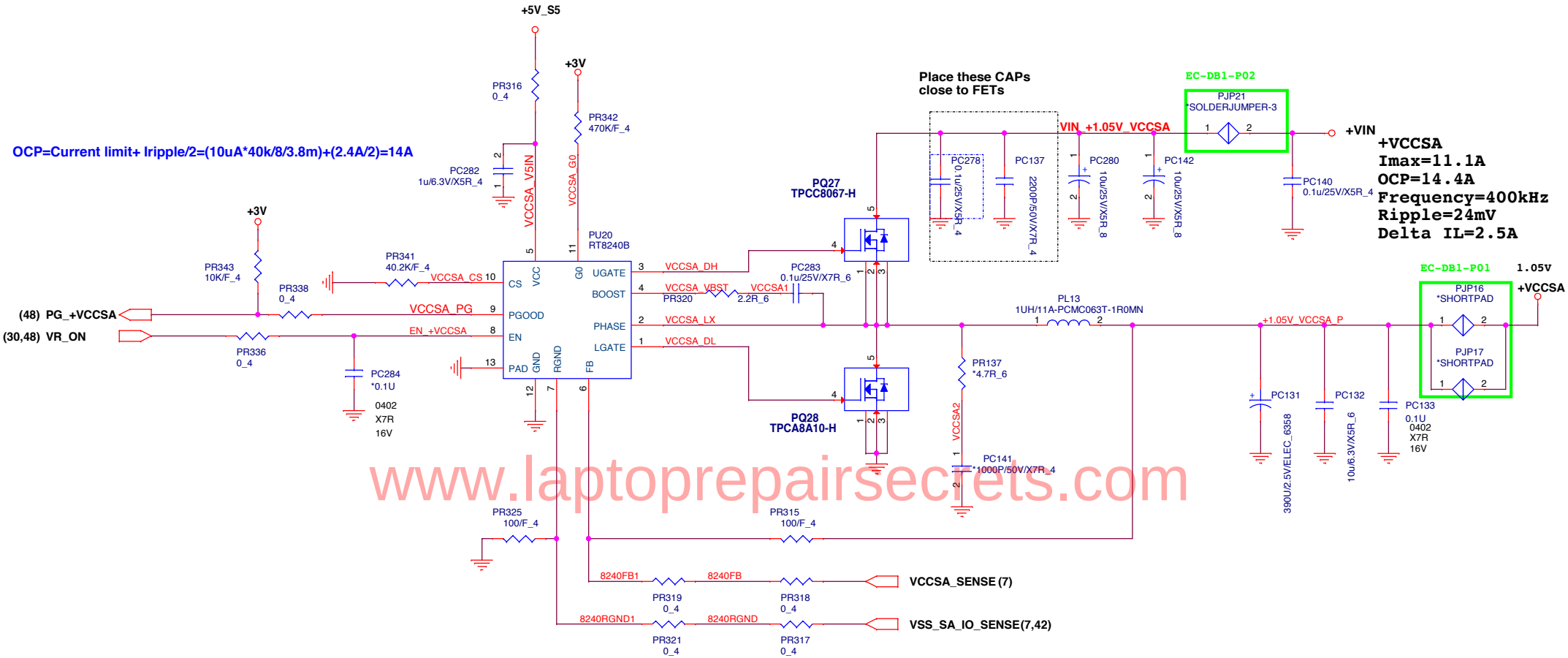


+1V_S5
Imax=7.6A
OCP=10A
Frequency=300kHz
Ripple=32mV
Delta IL=3.2A

Quanta Computer Inc.

Project: HP-SAIPAN

Title		
+1V_S5(TPS51211)		
Size	Document Number	Rev
	--	A
Page Modified: Thursday, December 17, 2015		Sheet 43 of 61



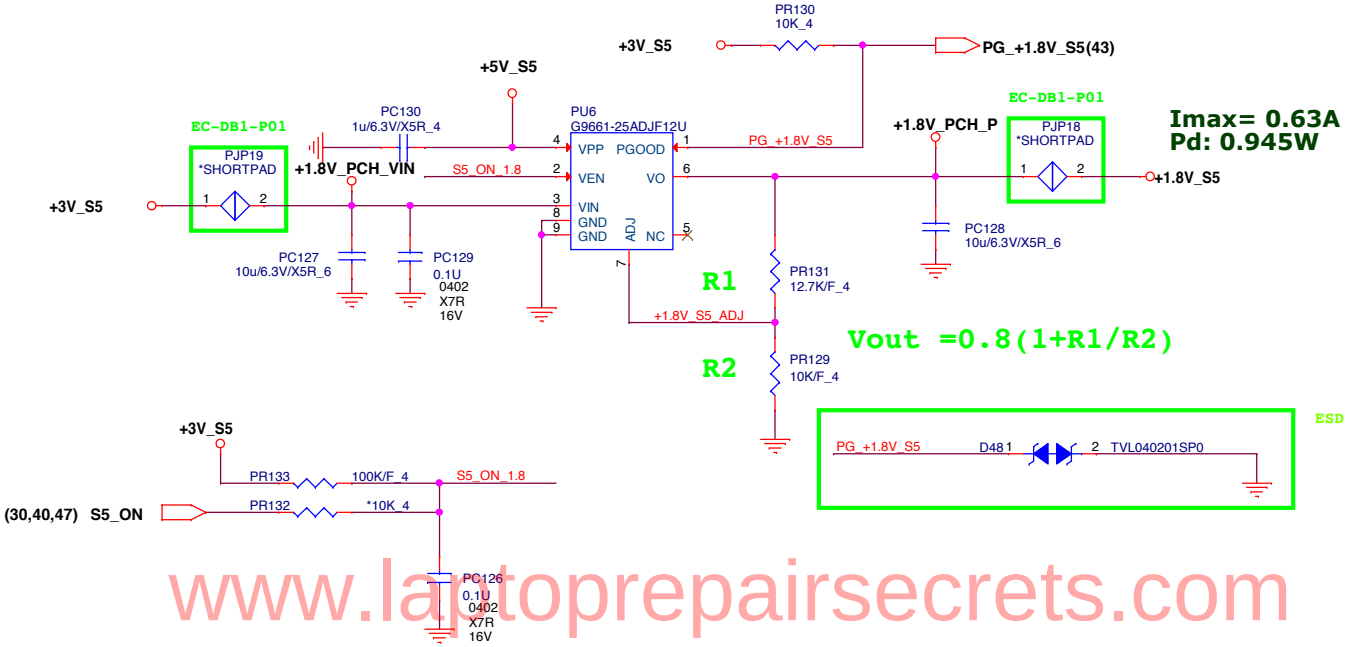
Quanta Computer Inc.

Project: HP-SAIPAN

Title: +VCCSA(RT8240B)

Size | Document Number -- | Rev A

Page Modified: Thursday, December 17, 2015 | Sheet 44 of 61



Quanta Computer Inc.

Project: HP-SAIPAN

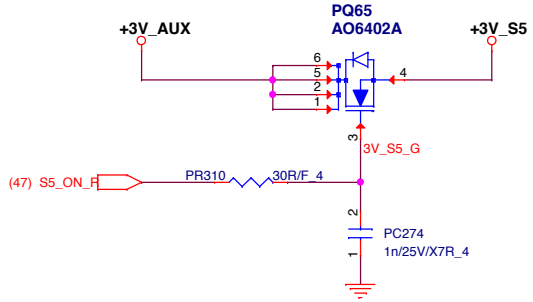
Title: +1.8V_S5 (G9661)

Size	Document Number	Rev
	--	A

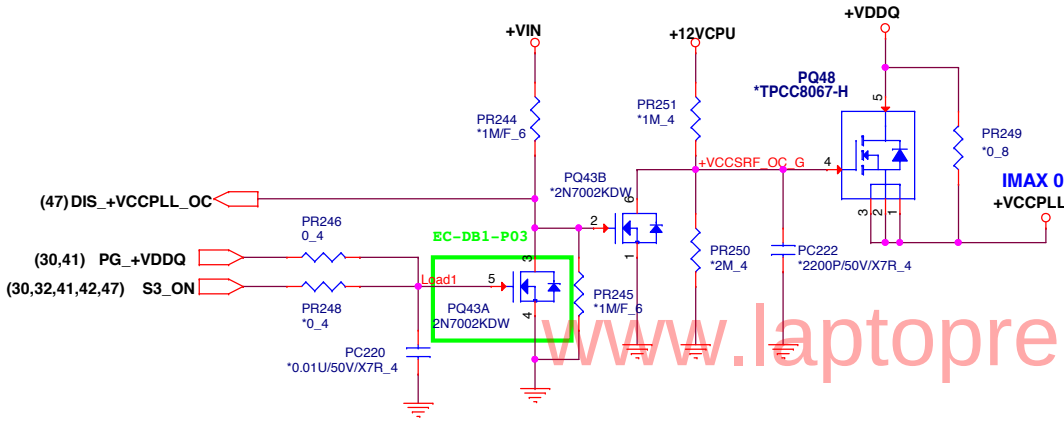
Page Modified: Thursday, December 17, 2015 | Sheet 45 of 61

S5 ON Load SW

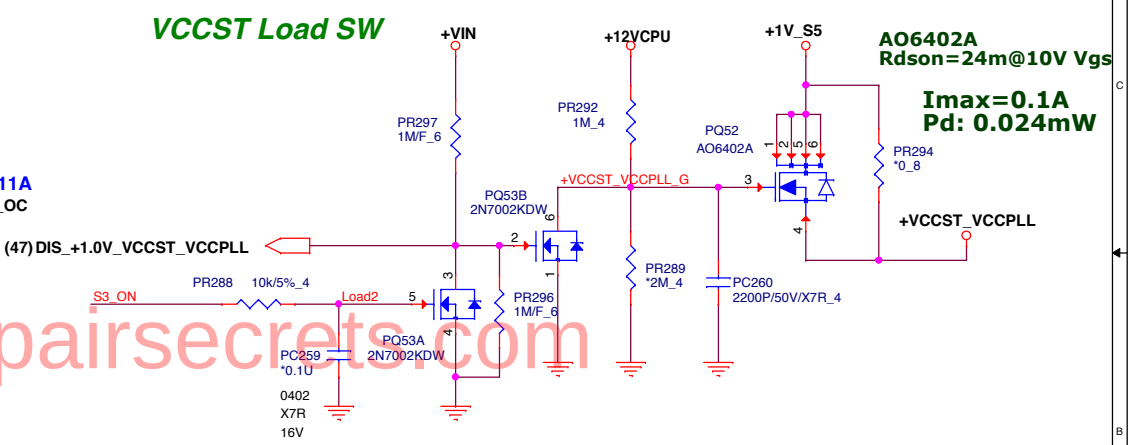
AO6402A
Rdson=24m@10V Vgs
Imax=5.5A
Pd: 0.726W



VCCST Load SW

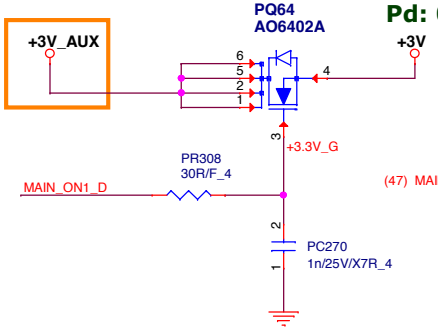


VCCST Load SW

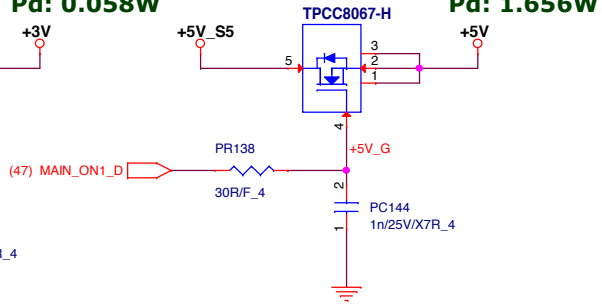


MAIN ON_1 Load SW

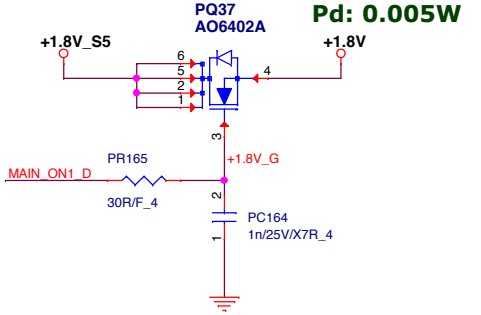
AO6402A
Rdson=24m@10V Vgs
Imax=1.2A
Pd: 0.058W



TPCC8067-H
Rdson=20m@10V Vgs
Imax=9.1A
Pd: 1.656W



AO6402A
Rdson=24m@10V Vgs
Imax=0.45A
Pd: 0.005W



Mosfet parameter

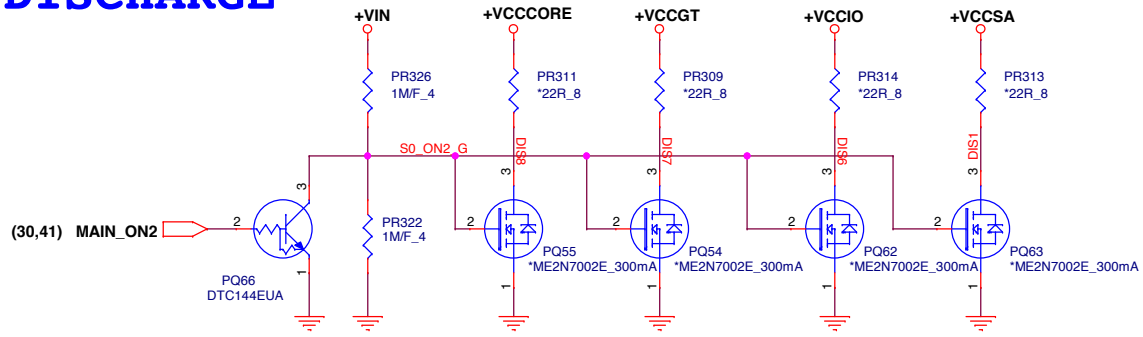
Mosfet	Package	ID(Ta=25C)	Rds_on_max	Vgs_max
ME3424D-G	TSOP-6	5.0A/6.7A	42m	+/- 20V
TPCC8067-H	3x3	9A	26m	+/- 20V
TPCA8064-H	SO-8	20A	7.9m	+/- 20V

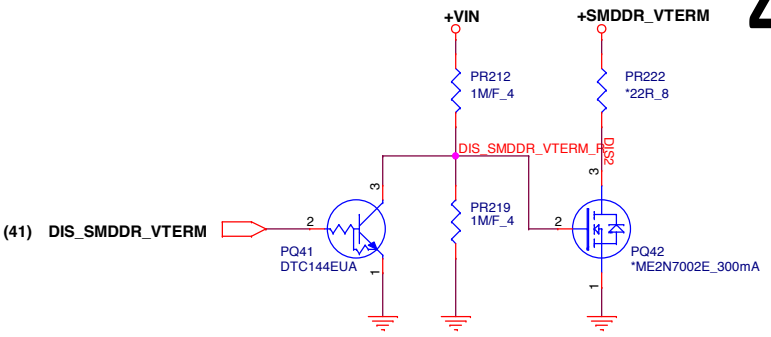
HP Restricted Secret

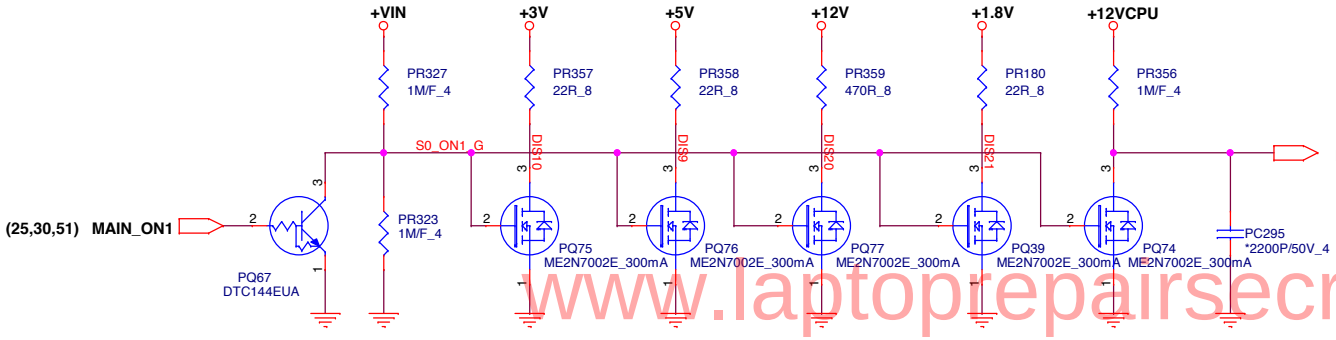
Quanta Computer Inc.
Project: HP-SAIPAN

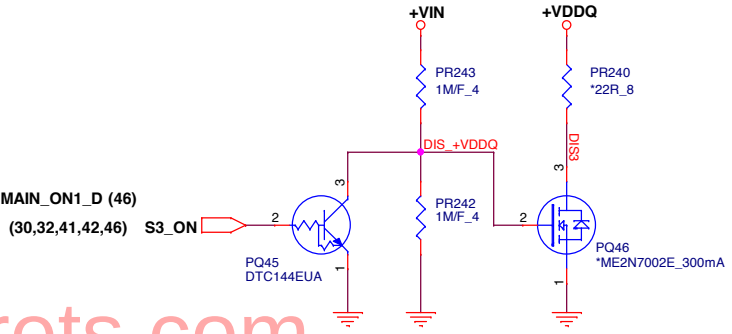
Title: Load Switch
Size: | Document Number: -- | Rev: A
Page Modified: Thursday, December 17, 2015 | Sheet 46 of 61

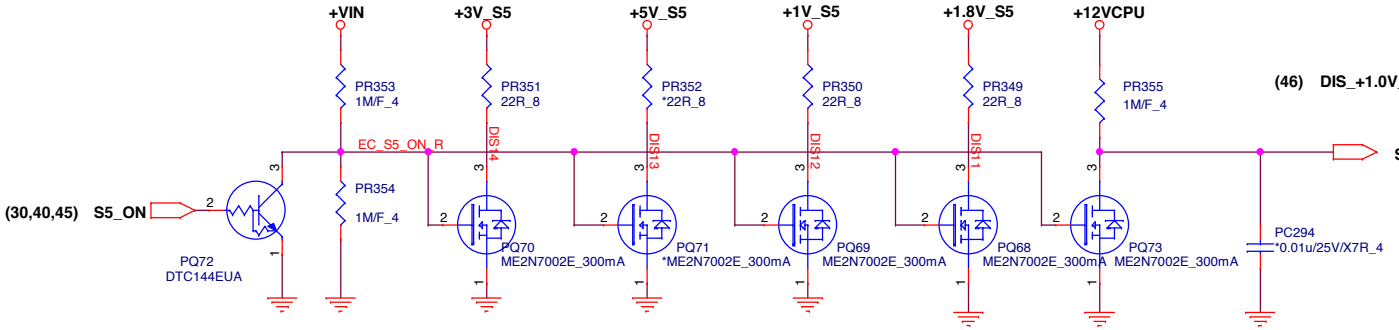
DISCHARGE

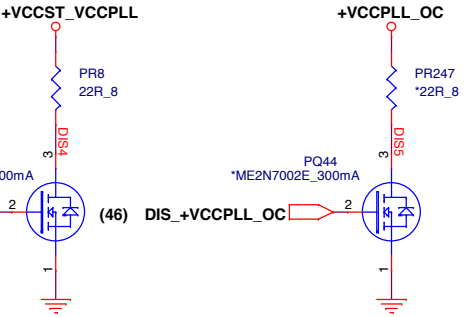










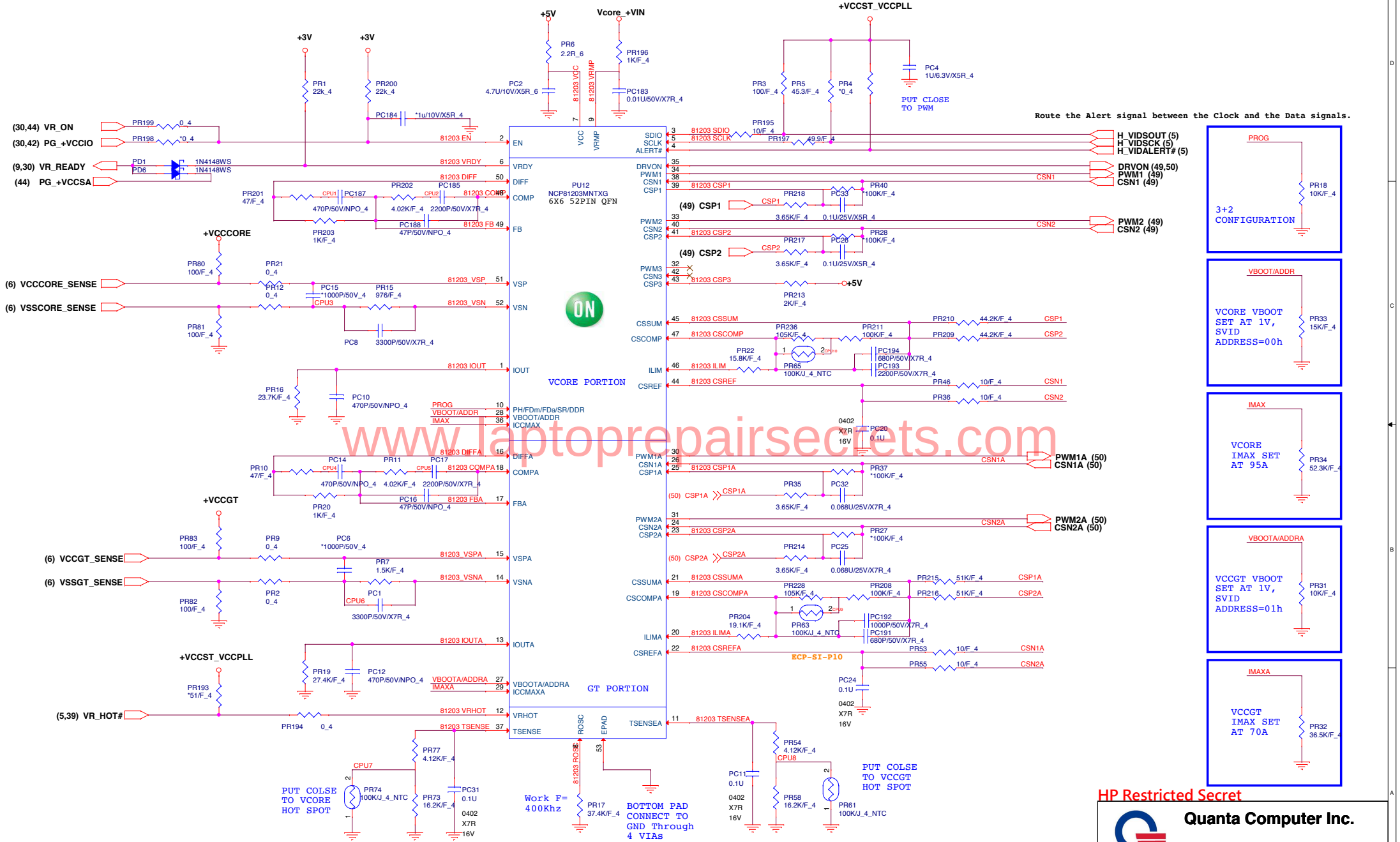


Quanta Computer Inc.

Project: HP-SAIPAN

Title		
Discharge		
Size	Document Number	Rev
	--	A
Page Modified: Thursday, December 17, 2015		Sheet 47 of 61

Intel SKYLAKE IMVP8 POWER CKT - 3+2 PHASE

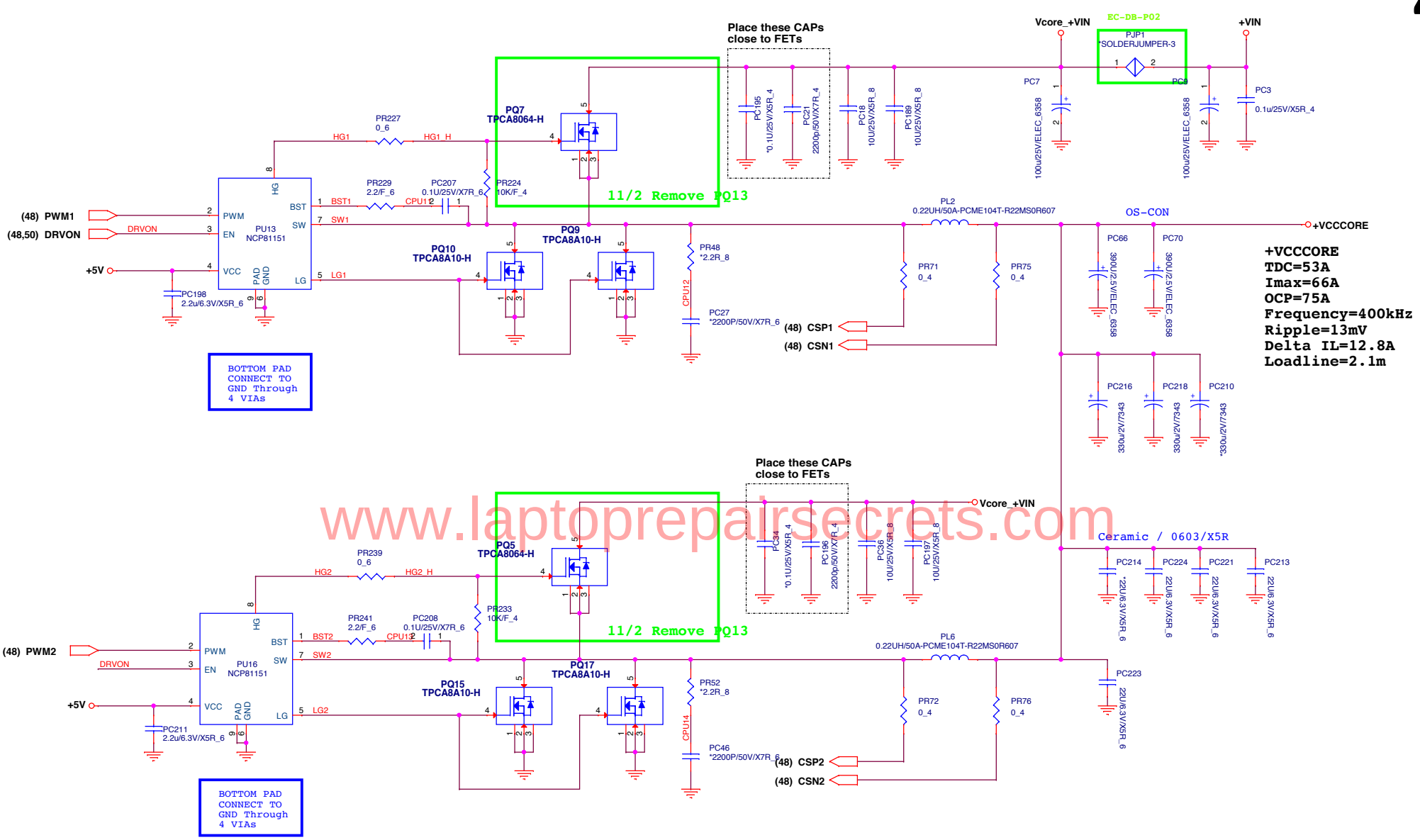


HP Restricted Secret

Quanta Computer Inc.

Project: HP-SAIPAN

Title: VCC_CORE & VCC_GT		
Size	Document Number: --	Rev: A
Page Modified: Thursday, December 17, 2015		Sheet 48 of 61



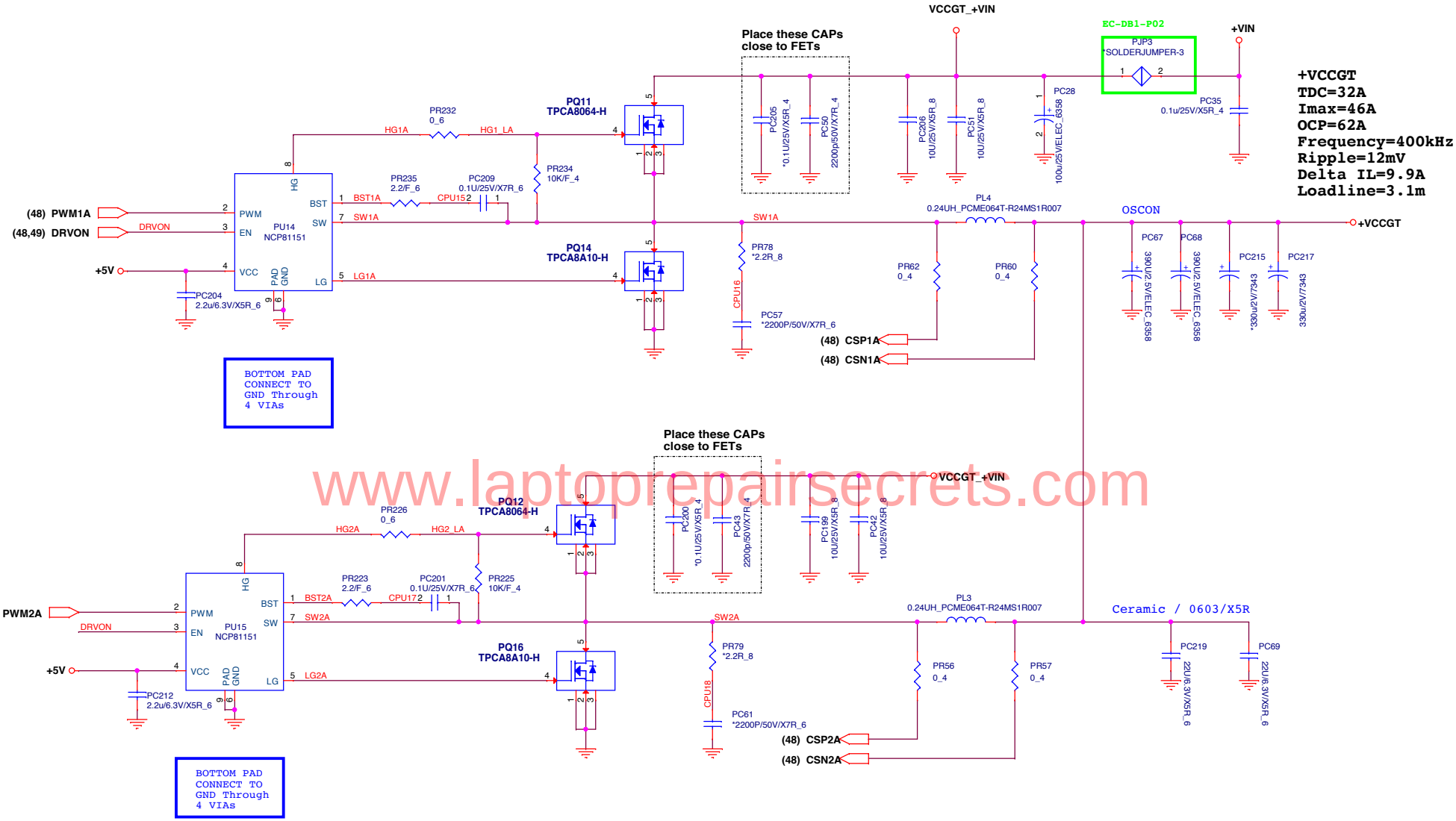
Quanta Computer Inc.

Project: HP-SAIPAN

Title: VCORE OUT STAGE

Size: Document Number: -- Rev: A

Page Modified: Thursday, December 17, 2015 Sheet 49 of 61



Quanta Computer Inc.

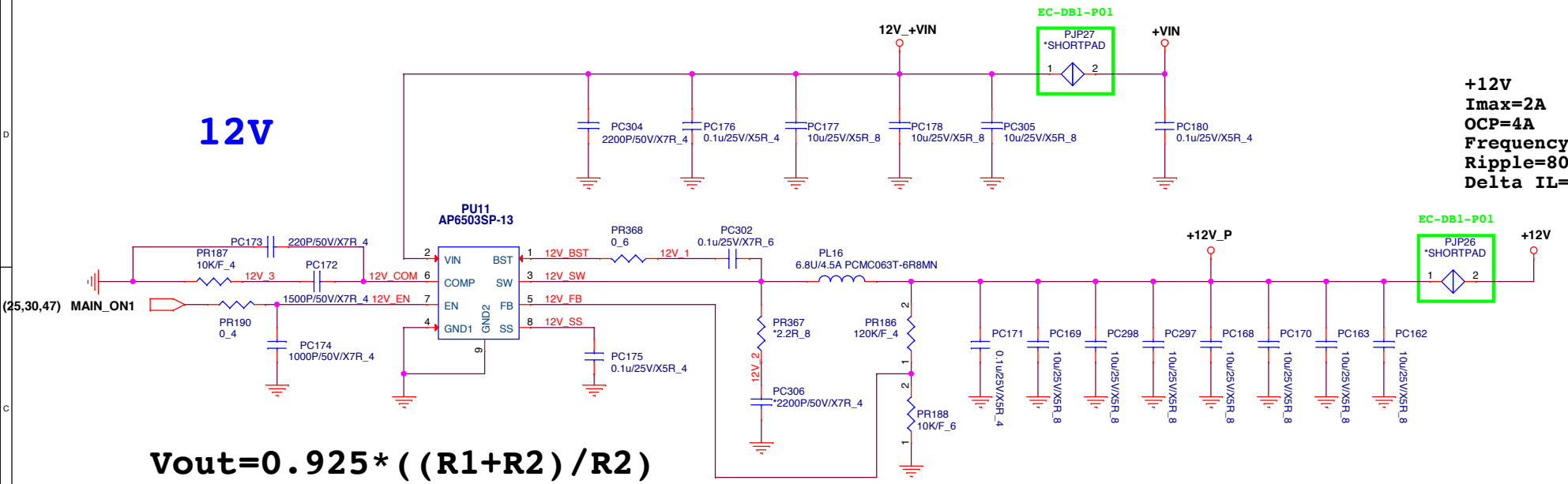
Project: HP-SAIPAN

Title: VCCGT OUTPUT STAGE

Size: | Document Number: -- | Rev: A

Page Modified: Thursday, December 17, 2015 | Sheet 50 of 61

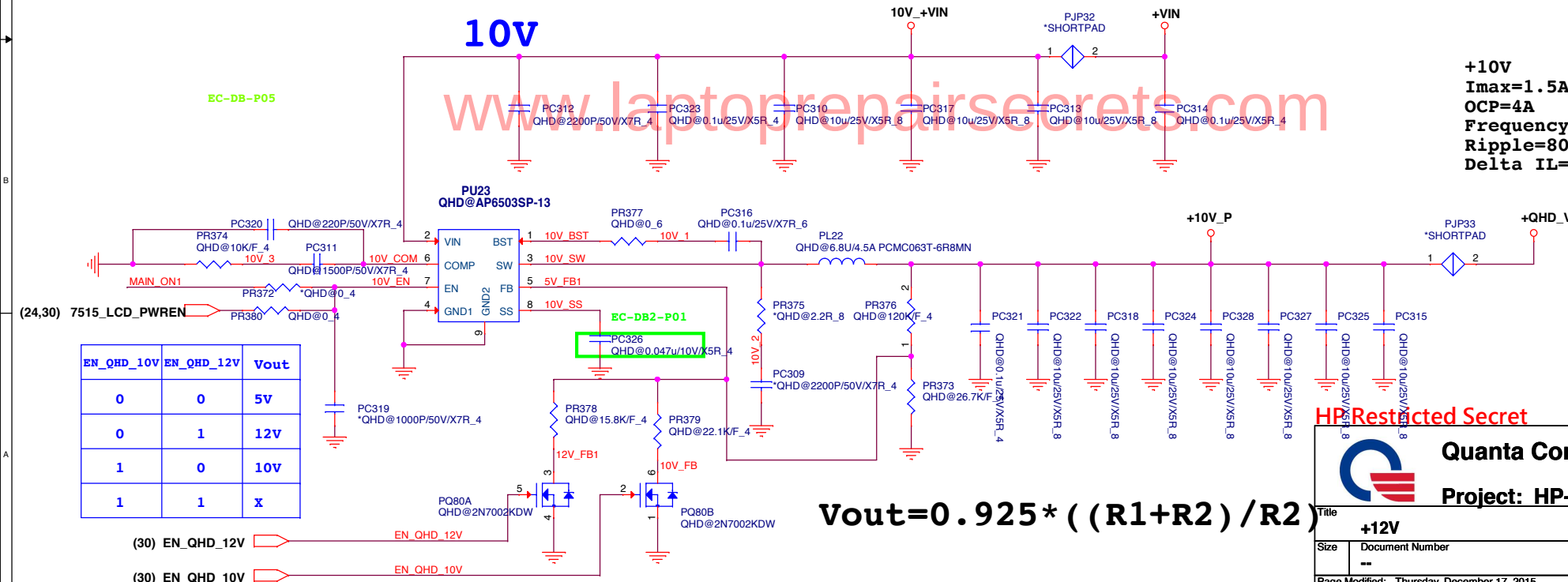
12V



+12V
Imax=2A
OCP=4A
Frequency=340kHz
Ripple=80mV
Delta IL=2A

Vout=0.925*((R1+R2)/R2)

10V



EN_QHD_10V	EN_QHD_12V	Vout
0	0	5V
0	1	12V
1	0	10V
1	1	X

+10V
Imax=1.5A
OCP=4A
Frequency=340kHz
Ripple=80mV
Delta IL=2A

Vout=0.925*((R1+R2)/R2)

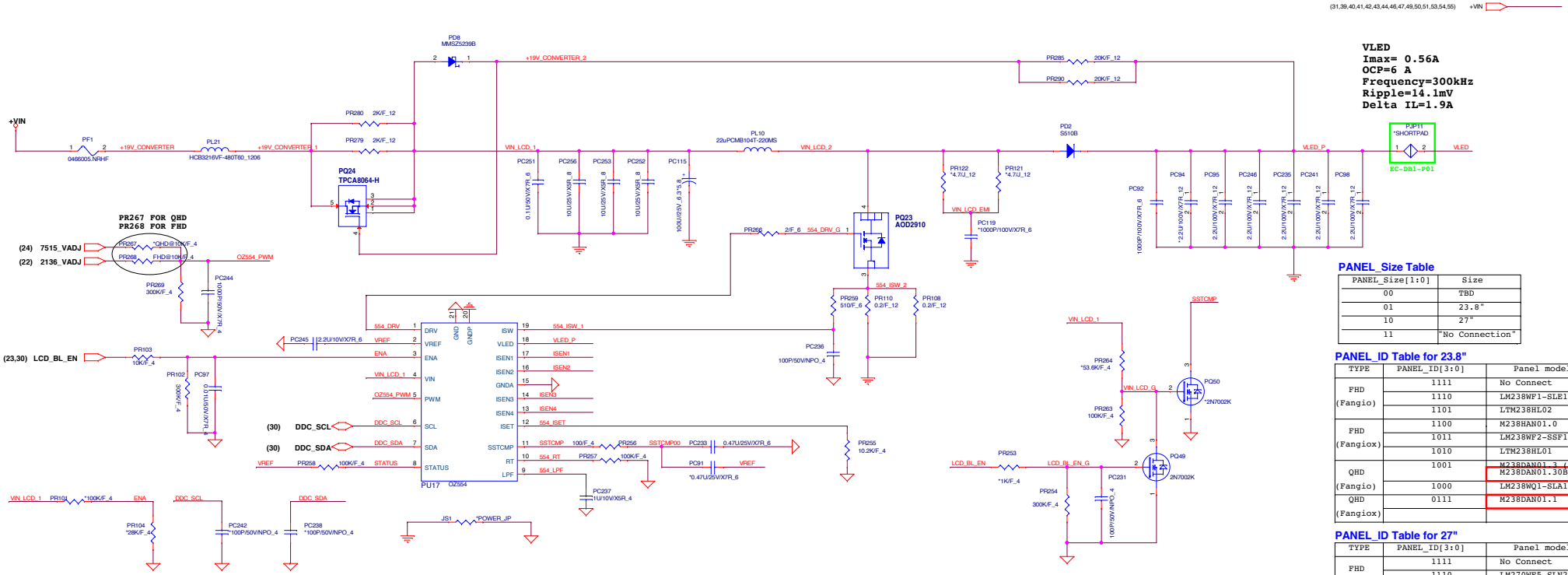
Quanta Computer Inc.

Project: HP-SAIPAN

Title: +12V

Size: | Document Number: -- | Rev: A

Page Modified: Thursday, December 17, 2015 | Sheet 51 of 61



PANEL_Size Table

PANEL_Size[1:0]	Size
00	TBD
01	23.8"
10	27"
11	"No Connection"

PANEL_ID Table for 23.8"

TYPE	PANEL_ID[3:0]	Panel model
FHD (Fangio)	1111	No Connect
	1110	LM238WF1-SLE1
	1101	LTM238HL02
FHD (Fangiox)	1100	M238HAN01.0
	1011	LM238WF2-SSF1
	1010	LTM238HL01
QHD (Fangio)	1001	M238DAN01.3 (DB)
		M238DAN01.30B (PV)
	1000	LM238WQ1-SLA1
QHD (Fangiox)	0111	M238DAN01.1

PANEL_ID Table for 27"

TYPE	PANEL_ID[3:0]	Panel model
FHD (Fangio)	1111	No Connect
	1110	LM270WF5-SLN2
	1101	LTM270HL02
QHD	1100	LM270WQ1-SLC2
	1011	LTM270DL05
	1010	AVL5
	1001	Reserve
	1000	Reserve

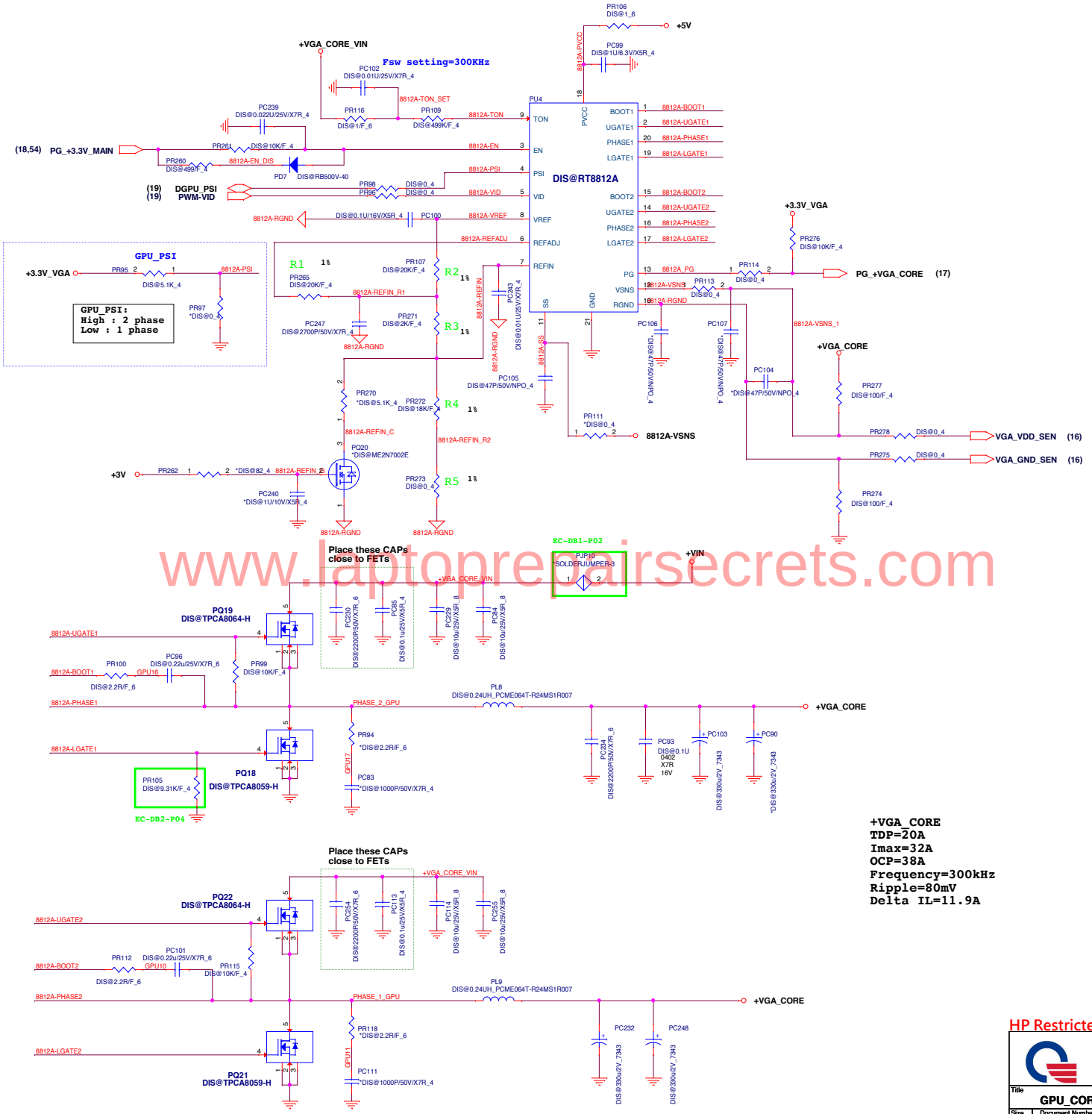
Quanta Computer Inc.

Project: HP-SAIPAN

Title: CONVERTER

Size: Document Number: — Rev: A

Page Modified: Thursday, December 17, 2015 Sheet 52 of 61



+VGA_CORE
TDP=20A
Imax=32A
OCP=38A
Frequency=300kHz
Ripple=80mV
Delta IL=11.9A

Quanta Computer Inc.

Project: HP-SAIPAN

Title: GPU_CORE (ISL62771)

Size: | Document Number: -- | Rev: A

Page Modified: Thursday, December 17, 2015 | Sheet 53 of 61

VGA POWER

(17,21) +1.35V_VGA
(16,18,19,20,53) +3.3V_VGA
(16,17,18) +1.05V_VGA

54

3.3V VGA

+3.3V_VGA +VGA_CORE +1.05V_VGA +1.35V_VGA +12VCPU +3V

PR306 *DIS@0_6

AO6402A
Rdson=24m@10V Vgs
Imax=0.06A
Pd: 0.086mW

PQ56 DIS@AO6402A
PC276 DIS@0.1U 0402 X7R 16V
3VGFX_OND
PQ58
PC266 DIS@1000P/10V/X7R_4
PC268 DIS@0.1U 0402 X7R 16V
PC267 DIS@10u/6.3V/X5R_6
+3.3V_VGA

+3V_S5
R221 DIS@10k/5%_4
R674 DIS@10k/5%_4
PR134 DIS@1M_4
PR135 *DIS@1M_4
PR299 DIS@22R_8
PR303 DIS@22R_8
PR300 DIS@22R_8
PR302 DIS@22R_8
PR301 DIS@1M_4
PQ59 PQ61 PQ57 PQ60
DIS@2N7002K_300MA
PR312 DIS@0_4
(11) EN_DGPU_PWR#
EN_+3.3V_VGA#_G1
3EN_+3.3V_VGA#_G2
PQ29B *2N7002KDW
PQ29A *2N7002KDW
EC-DB1-P04

3VGFX_ONG
D491 TVL040201SP0
ESD

EC-DB1-P01
PJP28 *SHORTPAD
1.35VGFX_VIN
+VIN

PC77 DIS@2200p/50V_6
PC226 DIS@0.1u/50V_6
PC78 DIS@10u/25V_8
PC227 DIS@10u/25V_8
PC76 DIS@0.1u/50V_6

VCC
PR88 *DIS@499K/F_4
PR85 DIS@1F_6
1.35VGFX_BST
1.35VGFX_BST1
PC71 DIS@0.1u/50V_6
PL7 DIS@1UH/11A-PCMC063T-1R0MN
PR91 DIS@100K/F_4
PR90 DIS@0_4
(18) PG_+1.35_VGA
PR92 DIS@200K/F_4
(17) EN_+1.35V_VGA
PR84 DIS@0_4
PC72 *DIS@0.1U/16V/X5R_4
PR89 DIS@0_4
PR252 DIS@0_6
1.35VGFX_EN
1.35VGFX_PG
1.35VGFX_LP#
PU3 DIS@NB671GQ-Z
VIN BST SW1 SW2 SW3 SW4 VOUT PGND EN PG LP# NC1 NC2 AGND VCC FB
1.35VGFX_SW
PR93 *DIS@4.7_6
1.35VGFX_SW_EMI
PC81 *DIS@680p/50V_6
PC80 DIS@0.1u/16V_4
VCC
PC73 DIS@1u/6.3V_4
1.35VGFX_FB
PR86 DIS@68.1K/F_4
PR87 DIS@54.9K/F_4
VREF=0.604V

EC-DB1-P01
PJP9 *SHORTPAD
+1.35V_VGA
+1.35V_VGA_P
PC74 PC228 PC225 PC79 PC75
PC82 *DIS@390U/2.5V/ELEC_6358

+1.35V_VGA
Imax=4.5A
OCP=8A
Frequency=500kHz
Ripple=20mV
Delta IL=2.5A

+1.05V VGA

+3.3V_VGA
PR125 DIS@100K_4
PR124 DIS@0_4
(30) PG_+1.05V_VGA
40mil
EC-DB1-P01
+5V_S5
PJP29 *SHORTPAD
PR117 DIS@10_6
PC250 DIS@0.01U/50V/X7R_4
PC249 DIS@10U/6.3V/X5R_6
PC110 DIS@1U/6.3V/X5R_4

EC2 *DIS@1000P/50V/X7R_4
ER1 *DIS@4.7_6
PU5 DIS@RT8068A
PG PVIN PVIN SVIN GND NC LX LX NC FB EN
8060_1.0V
8060PVIN_1.0V
8060SVIN_1.0V
8060LX_1.0V
8060NC_1.0V
8060FB_1.0V
8060EN_1.0V
PC108 *DIS@68P/50V/COG_4
PR123 DIS@10K/F_4
PC112 DIS@0.22u/10V/X5R_4
EC-DB1-P06

PL12 DIS@1UH/11A-PCMC063T-1R0MN
+1.05V_VGA_P
PR119 DIS@11.3K/F_4
R1
PR120 DIS@15K/F_4
R2
PC109 *DIS@22P/50V/NPO_4
PC122 DIS@0.1U 0402 X7R 16V
PC121 DIS@22u/6.3V/X5R_6

EC-DB1-P01
PJP12 *SHORTPAD
+1.05V_VGA
PC120 *DIS@390U/2.5V/ELEC_6358

+1.05V_VGA
Imax=2.1A
OCP=4A
Frequency=1MHz
Ripple=12mV
Delta IL=0.8A

PG_+3.3V_MAIN (18,53)

V0=0.6*(R1+R2)/R2

Quanta Computer Inc.
Project: HP-SAIPAN

Title		
GPU-1.05V / 1.35V		
Size	Document Number	Rev
	--	A
Page Modified: Thursday, December 17, 2015		Sheet 54 of 61

CPU HOLE

H7 H-C197D150P2 *Hole
H8 H-C197D150P2 *Hole
H11 H-C197D150P2 *Hole

H17 *Hole — HG-SAIPAN-1-N83
H4 *Hole — HG-SAIPAN-33-N83
H10 *Hole — HG-SAIPAN-11-N83
H18 *Hole — hg-saipan-1-N83
H20 *Hole — hg-saipan-3-N83
H19 *Hole — hg-c315d185p2-N83

H16 *Hole — hg-saipan-9-N83
H3 *Hole — hg-c315d138p2-N83
H15 *Hole — hg-saipan-1-N83

H13 *Hole — hg-c276d197p2
H6 *Hole — hg-c276d197p2
H12 *Hole — hg-c276d197p2
H5 *Hole — hg-c276d197p2

EC-DB2-E41

EMI PAD

H22 SPAD-RE158X1181NP PAD
H14 SPAD-RE495X98NP PAD
H21 SPAD-RE197X197NP PAD
H1 SPAD-RE236X79NP PAD
H2 SPAD-RE236X118NP PAD

VGA HOLE

HOLE1 H-C146D146N
HOLE3 H-C146D146N

WLAN HOLE

HOLE2 H-TC236IC126BC126D126PT Hole

EC-DB2-E42

SSD HOLE

HOLE4 H-TC236IC126BC126D126PT Hole

EC-DB2-E42

RF

+VDDQ C287 *15p/50V/C0G_4
+VDDQ C359 100p/50V/NPO_4
+VDDQ C363 100p/50V/NPO_4
+VDDQ C445 *15p/50V/C0G_4
+VDDQ C391 *15p/50V/C0G_4
+VDDQ C361 *15p/50V/C0G_4
RF
+VDDQ C449 100p/50V/NPO_4

RF
+VDDQ C496 100p/50V/NPO_4
+VDDQ C313 *15p/50V/C0G_4
RF
+VDDQ C55 100p/50V/NPO_4
+VDDQ C498 100p/50V/NPO_4
+VDDQ C364 100p/50V/NPO_4
+VDDQ C382 100p/50V/NPO_4

+VIN C604 *15p/50V/C0G_4
+VIN C600 *15p/50V/C0G_4
+VIN C239 *15p/50V/C0G_4
+VIN C136 *15p/50V/C0G_4
+VIN C201 *15p/50V/C0G_4
+VIN C7 *15p/50V/C0G_4
+VIN C203 *15p/50V/C0G_4
+VIN C592 *15p/50V/C0G_4

+12V C475 *15p/50V/C0G_4
+12V C612 *15p/50V/C0G_4
+12V C480 *15p/50V/C0G_4

+3V_S5 C122 *15p/50V/C0G_4
+3V_S5 C243 *15p/50V/C0G_4
+3V_S5 C574 *15p/50V/C0G_4

+3V C537 *15p/50V/C0G_4

+5V C582 *15p/50V/C0G_4
+5V C518 *15p/50V/C0G_4
+5V C202 *15p/50V/C0G_4

+3V C101 1000p/16V/X7R_4 For SPI_CLK
+3V C504 1000p/16V/X7R_4

Place around +VIN trace

+VIN C240 *0.1U/25V_4_X7R
+VIN C33 *0.1U/25V_4_X7R
+VIN C4 *0.1U/25V_4_X7R
+VIN C5 *0.1U/25V_4_X7R
+VIN C1 *0.1U/25V_4_X7R

+VIN C527 *0.1U/25V_4_X7R
+VIN C135 *0.1U/25V_4_X7R
+VIN C2 *0.1U/25V_4_X7R
+VIN C34 *0.1U/25V_4_X7R
+VIN C199 *0.1U/25V_4_X7R

+VIN C6 *0.1U/25V_4_X7R
+VIN C289 *0.1U/25V_4_X7R
+VIN C288 *0.1U/25V_4_X7R
+VIN C216 *0.1U/25V_4_X7R

Quanta Computer Inc.

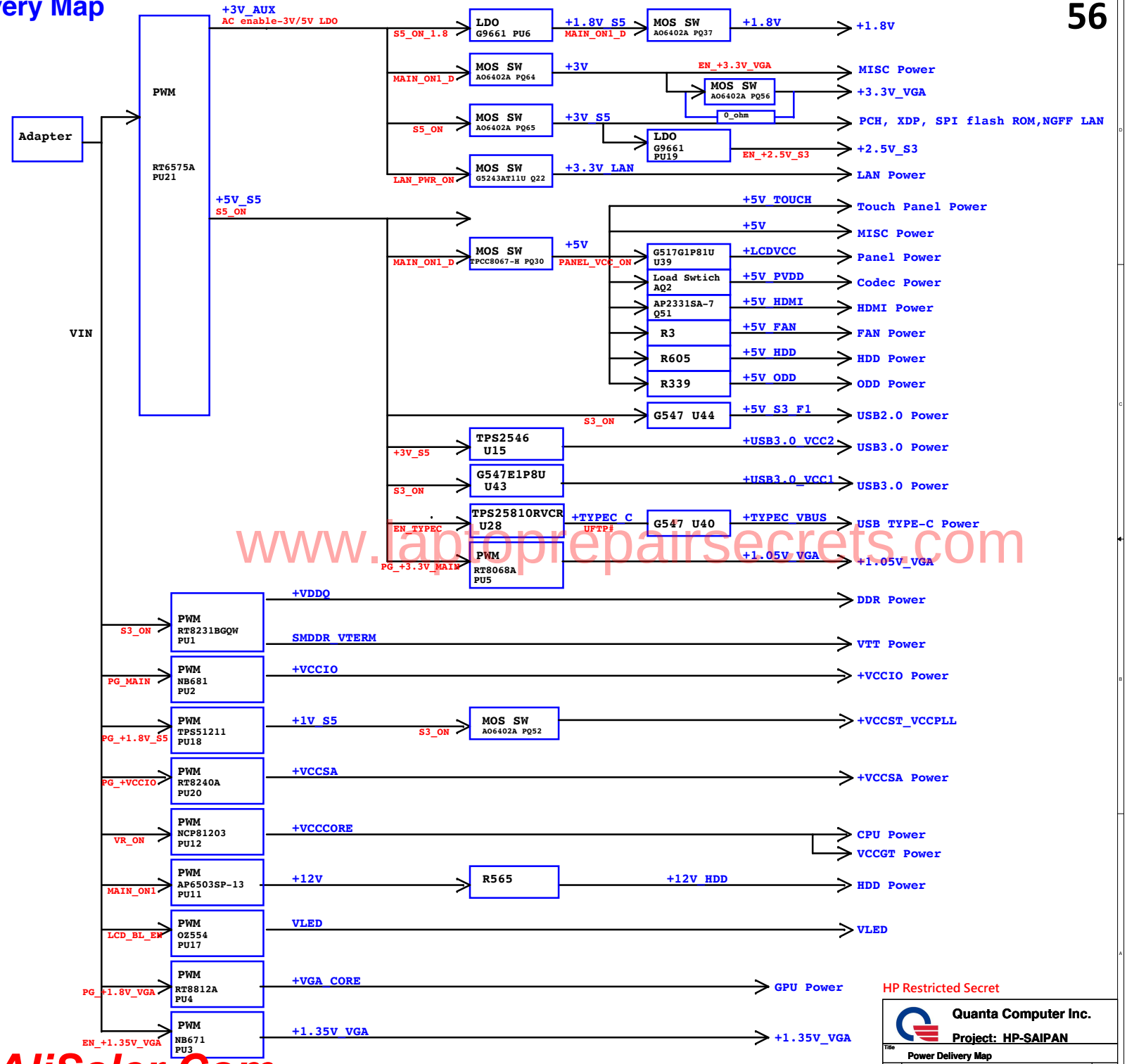
Project: HP-SAIPAN

Title: HOLE/VIN CAP/RF CAP

Size: | Document Number: -- | Rev: B

Page Modified: Thursday, December 17, 2015 | Sheet 55 of 61

Power Delivery Map



Quanta Computer Inc.

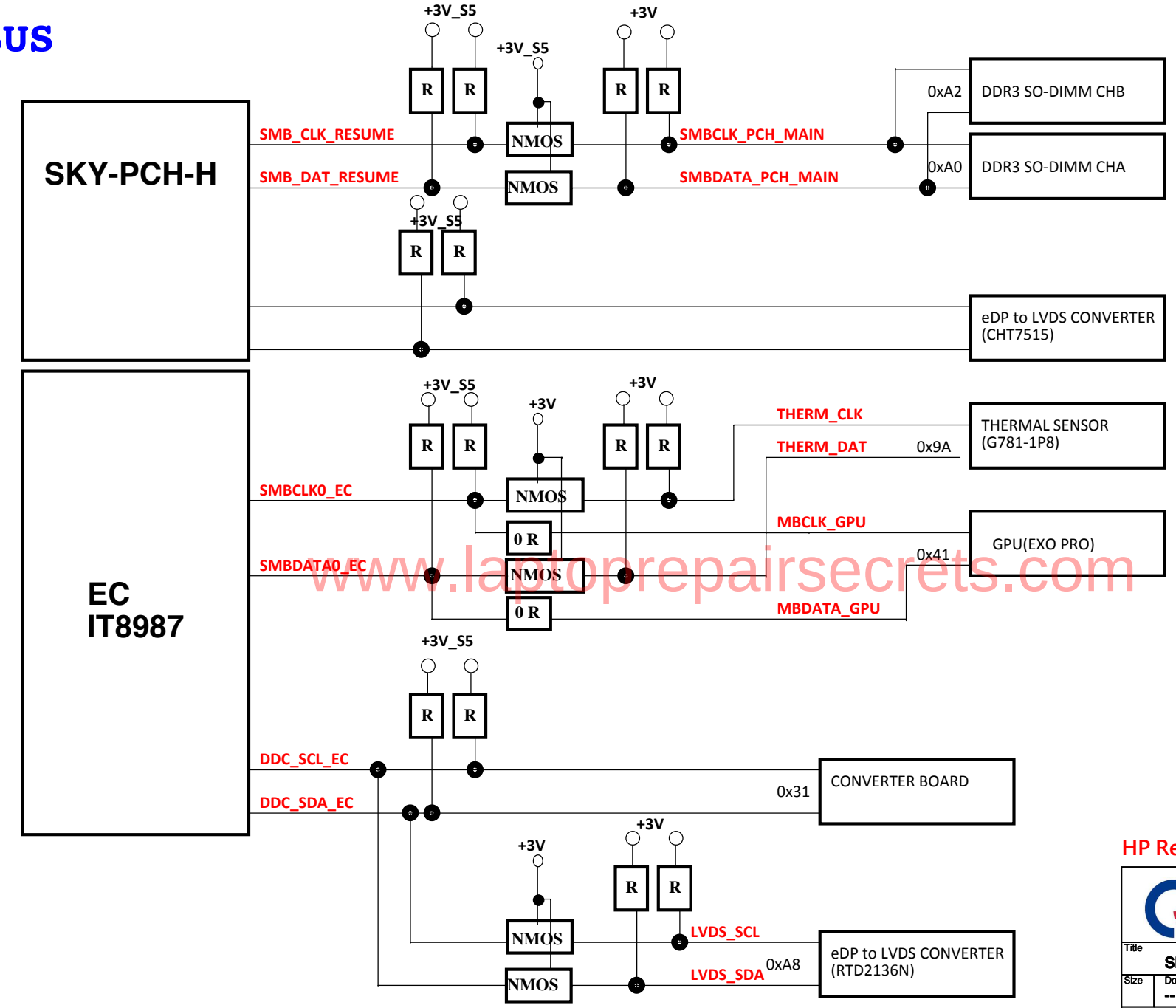
Project: HP-SAIPAN

Title: Power Delivery Map

Size: — Document Number: — Rev: A

Page Modified: Thursday, December 17, 2015 Sheet 56 of 61

SMBUS



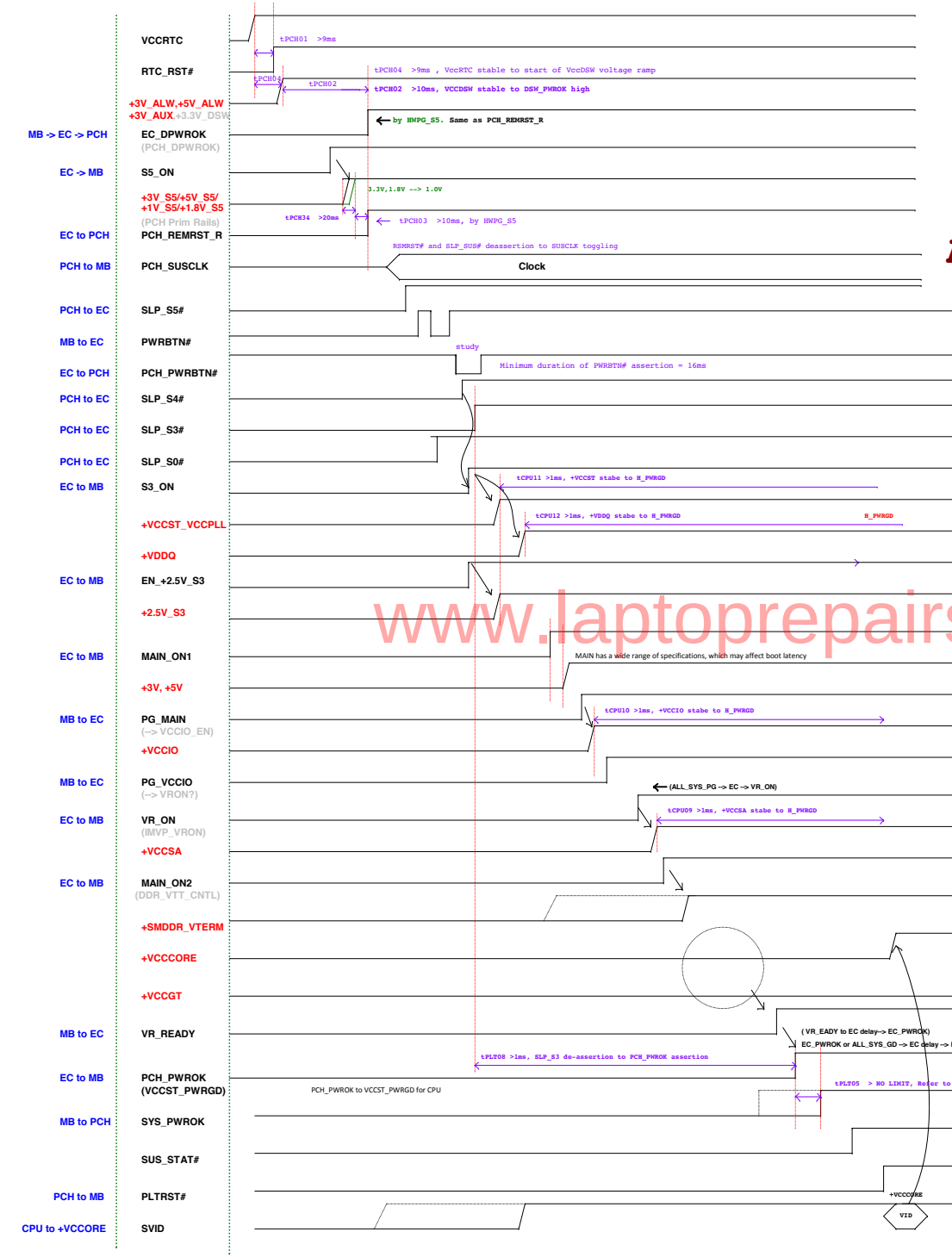
HP Restricted Secret

Quanta Computer Inc.

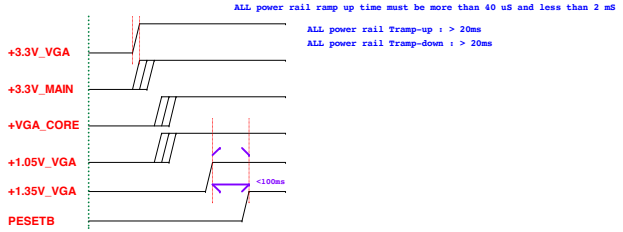
Project: HP-SAIPAN

Title		
SMBus		
Size	Document Number	Rev
	--	A
Page Modified: Thursday, December 17, 2015		Sheet 57 of 61

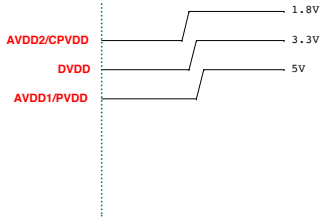
SKY-S POWER SEQUENCE



Nvidia dGPU POWER SEQUENCE



AUDIO POWER SEQUENCE



Quanta Computer Inc.

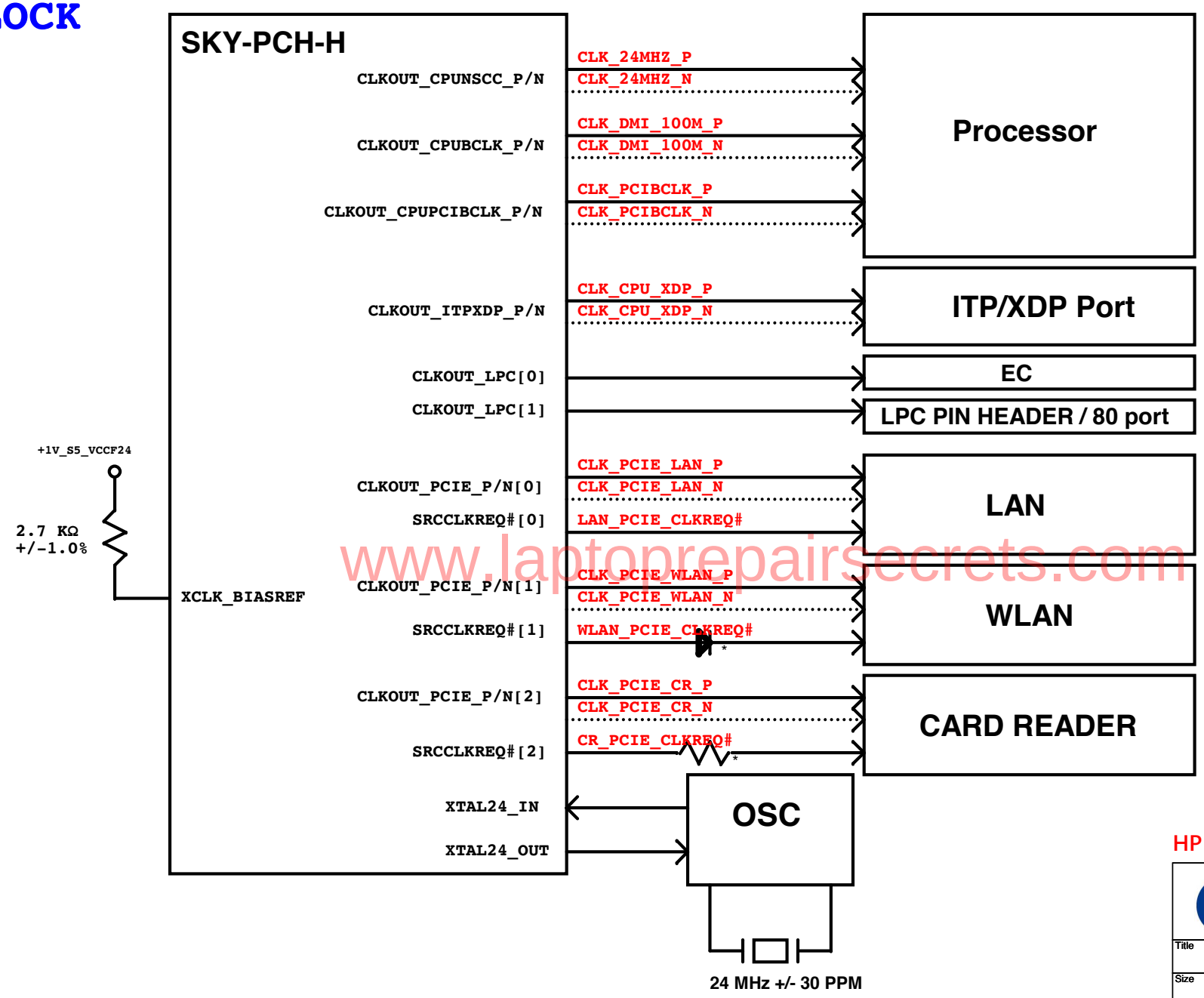
Project: HP-SAIPAN

Title: Power Sequence

Size: — Document Number: — Rev: A

Page Modified: Thursday, December 17, 2015 Sheet 58 of 61

CLOCK

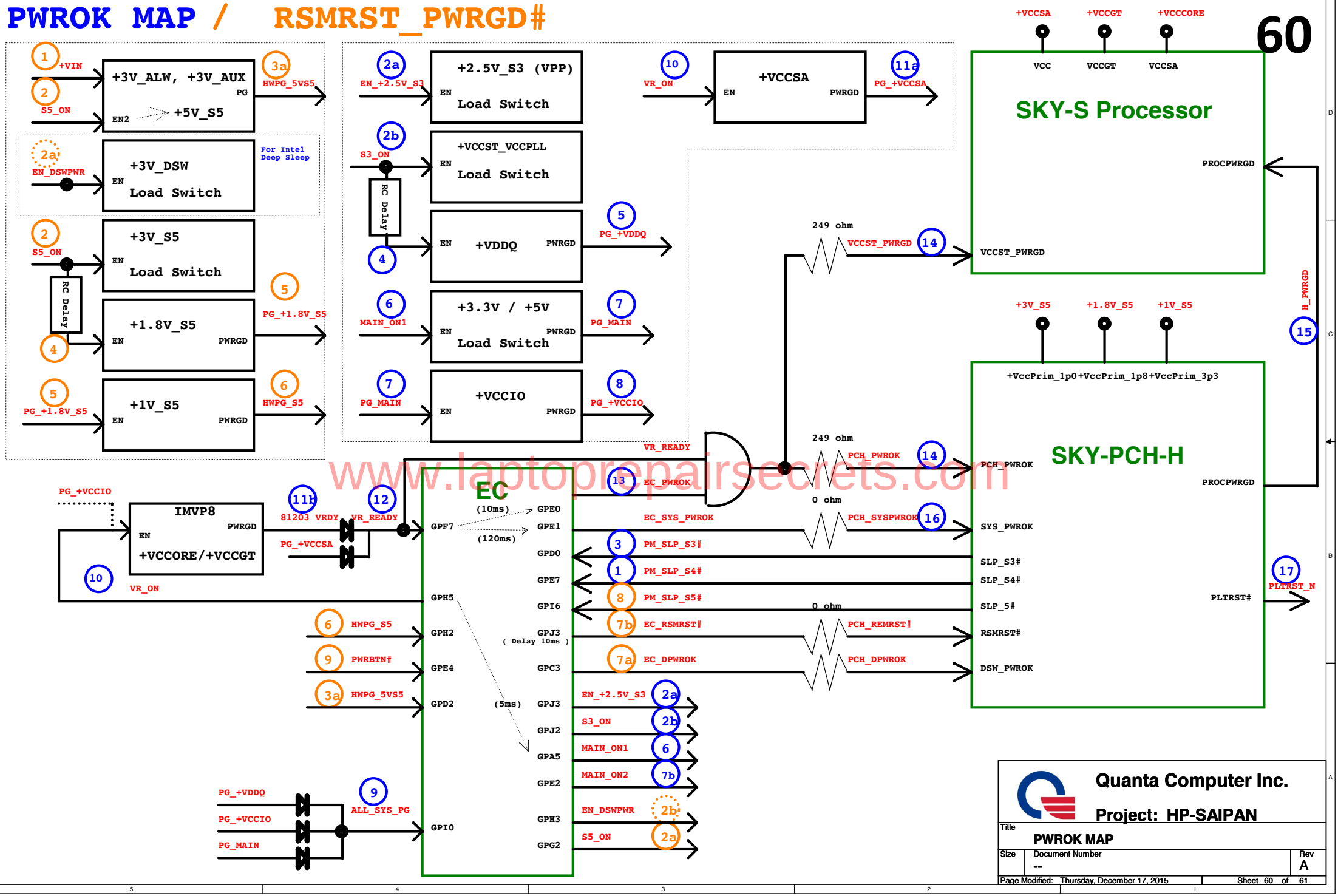


Quanta Computer Inc.

Project: HP-SAIPAN

Title: CLOCK MAP		
Size	Document Number: --	Rev: A
Page Modified: Thursday, December 17, 2015		Sheet 59 of 61

PWROK MAP / RSMRST_PWRGD#



DB1 Change List

No.	Change details	Location/Description	Page	Change Reason
EC-DB1-E01	Change 0 ohm to shortpad	R76,R328,R329,R785,R166,R158,R732,R618,R351, R352,R598	5,9,10,12,16,26,34	Reduce 0 ohm usage for SMT.
EC-DB1-E02	Modify PEG HW straps	R489,R5106,R514	5	For PEG PCIe x4 Gen3 setting.
EC-DB1-E03	Remove AC caps on PEG [4:7] for N16S	C74,C73,C483,C479,C75,C76,C488,C497,C77,C78,C500 ,C506,C79,C80,C507,C515	16	N16S-GMR support PEG x3 only.
EC-DB1-E04	Add dual mosfet on SMBl_CLK/DAT	Q55	9	I2C power domain.
EC-DB1-E05	Remove C328	C328,C330	14,15	for DDR4 reset timing
EC-DB1-E06	Remove R612	R612	16	Don't support GC6.0
EC-DB1-E07	Remove R126,R118,R109	R126,R118,109	16,19	unnecessary
EC-DB1-E08	stuff R96	R96	9	NV suggest
EC-DB1-E09	De-populate SPI ROM	R64,R72,R129,U9,R124C102	19	De-populate SPI ROM
EC-DB1-E10	Change QHD panel circuit	all page	25	Chage QHD VCC control circuit
EC-DB1-E11	Chage R711 to 470 ohm	R711	25	QHD VCC discharge resistor
EC-DB1-E12	Change part	F9	26	common part
EC-DB1-E13	DMIC I2C circuit wrong	AR5/AR17/AR6/AR13	27	DMIC I2C circuit wrong
EC-DB1-E14	Change EC HW straps power domain to +3V_ALW	'--	30	timing issue
EC-DB1-E15	Stuff R571/R572	R571/R572	30	I2C power domain.
EC-DB1-E16	Remove R70	R70	30	Reduce 0 ohm usage for SMT.
EC-DB1-E17	Change +3.3V to +3.3V_CCD on CN4.1 & U3.5	CN4.1 & U3.5	31	To disable DMIC device in Fangio-x
EC-DB1-E18	Stuff U5,U4	U5,U4	31	ESD
EC-DB1-E19	Remove R3	R3	30	unnecessary

EC-DB-P01	change footprint to short pad.	PJP2,4~9,11~20,22~31	50~54	change footprint to short pad.
EC-DB-P02	change footprint to short pad.	PJP1,3,10,21	50~54	change footprint to short pad.
EC-DB-P03	change part reference for schematic error	PQ43A,PQ78A,PQ78B,PQ79A,PQ79B	50~55	change part reference for schematic error
EC-DB-P04	For Common parts	PQ29A,PQ29B		For Common parts

DB2 Change List

No.	Change details	Location/Description	Page	Change Reason
EC-DB2-E01	Change 0 ohm to shortpad	R552,R761,R735,R316,R307,R706,R164,R336 ,R666,R306,R278,R324,196,R781,R667,R231,R703,R372	5,9,10,11,12, 13,14,32	Reduce 0 ohm usage for SMT.
EC-DB2-E02	Adding TVS DIODE	D6,D7	5	ESD request
EC-DB2-E03	Change location C378/C379 to PC329/PC330	C378,C379	6	power parts.
EC-DB2-E04	Remove R673	R673	11	simple circuit
EC-DB2-E05	Stuff C594 10pf	C594	11	for CK_24M_EC timing
EC-DB2-E06	Change Board ID to SI (STUFF R702)	R702	12	BOARD ID
EC-DB2-E07	ADD TVS on WLAN_PCIE_CLKREQ#	D46	12	ESD request
EC-DB2-E08	Change part	L58	18	For common part
EC-DB2-E09	Chage c71 to 10pf and C72 to 12pf	C71,C72	18	Xtal accuracy
EC-DB2-E10	Don't stuff R18/R20	R18,R20	21	unnecessary
EC-DB2-E11	Don't stuff C116	C116	22	unnecessary
EC-DB2-E12	Don't stuff R181 and add R822 pull down	R181,R822	22	Realek recommand
EC-DB2-E13	Chage caps power rating from 16v to 10v	C108,AC9	22	Chage caps power rating
EC-DB2-E14	Chage c232 to and C228 to 8.2pf	C232/C228	24	Xtal accuracy
EC-DB2-E15	Change part	F9	26	For common part
EC-DB2-E16	Change Q10 to dual MOSFET. Q32/33 to Q57	Q10/Q11/Q10, Q32/Q33/Q57	26,34	Simple layout
EC-DB2-E17	Change part	AL9,AL10,AL11,AL13	27	For common part
EC-DB2-E18	adding disable DMIC icon	Au1.48	28	HP request
EC-DB2-E19	Stuff R803/R792/D33, don't stuff R802	R803,R802,R792,D33	12,28,29,34	enable PCie clock request function
EC-DB2-E20	Adding M.2 SSD function	All page	35	HP request
EC-DB2-E21	Change RJ45 part	CN24	28	SMT request
EC-DB2-E22	Chage caps power rating from 10v to 6.3v	C230,C482,C495	29,34	Chage caps power rating
EC-DB2-E23	Stuff C666	C666	29	EMI request
EC-DB2-E24	Change GPIO table in EC	EN_TYPEC,CLR_CMOS,EN_AUO_PVDD,BOX_BUTTON #,PCHHOT#,EC_MUTE#,HWPG_5VS5	30	common design
EC-DB2-E25	Change diode to 0 ohm	R837,R838,R839	30	common design
EC-DB2-E26	Change SMI circuit	R517	30	unnecessary
EC-DB2-E27	Adding iRMT control pin	R843	30	iRMT
EC-DB2-E28	Change QHD I2C control circuit	R627/R633	30	Leakage.
EC-DB2-E29	Remove D17/D19	D17/D19	30	unnecessary
EC-DB2-E30	Change L5 to 4.7ohm. Adding C674	L58,C674	31	DMIC EA timing
EC-DB2-E31	Stuff U5,U4	U5,U4	31	ESD
EC-DB2-E32	Add iRMT control circuit	R842,Q58,R840	31	iRMT
EC-DB2-E33	Reserve D45	D45	31	ESD
EC-DB2-E34	Change USB power switch	U43,U44,U33,U32,C342,C372	31,32	For common part
EC-DB2-E35	Change C235/C236 from 150uf to one 390uf (C236)	C235,C236	32	simple layout
EC-DB2-E36	Add M.2 SSD function	'--	35	HP request
EC-DB2-E37	Change Part	CN8	36	common design
EC-DB2-E38	Reserve C205	C205	36	Reserve only
EC-DB2-E39	Don't populate R384	R384	36	Leakage.
EC-DB2-E40	Remove LPC pin header	CN10	37	no enough layout space.

EC-DB-P01	change footprint to short pad.	PJP2,4~9,11~20,22~31	50~54	change footprint to short pad.
EC-DB-P02	change footprint to short pad.	PJP1,3,10,21	50~54	change footprint to short pad.
EC-DB-P03	change part reference for schematic error	PQ43A,PQ78A,PQ78B,PQ79A,PQ79B	50~55	change part reference for schematic error
EC-DB-P04	For Common parts	PQ29A,PQ29B		For Common parts

Quanta Computer Inc.

Project: HP-SAIPAN

Title: Cange List

Size: | Document Number: -- | Rev: A

Page Modified: Thursday, December 17, 2015 | Sheet 61 of 61