LCFC Confidential

FS441/FS540(NMC121) MB Schematics Document

WHL U42 with DDR4 + Nvidia N16V-GM

2018-01

REV:0.1

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Title: *Cover Page*

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Custom	*FS441/FS540*	0.1

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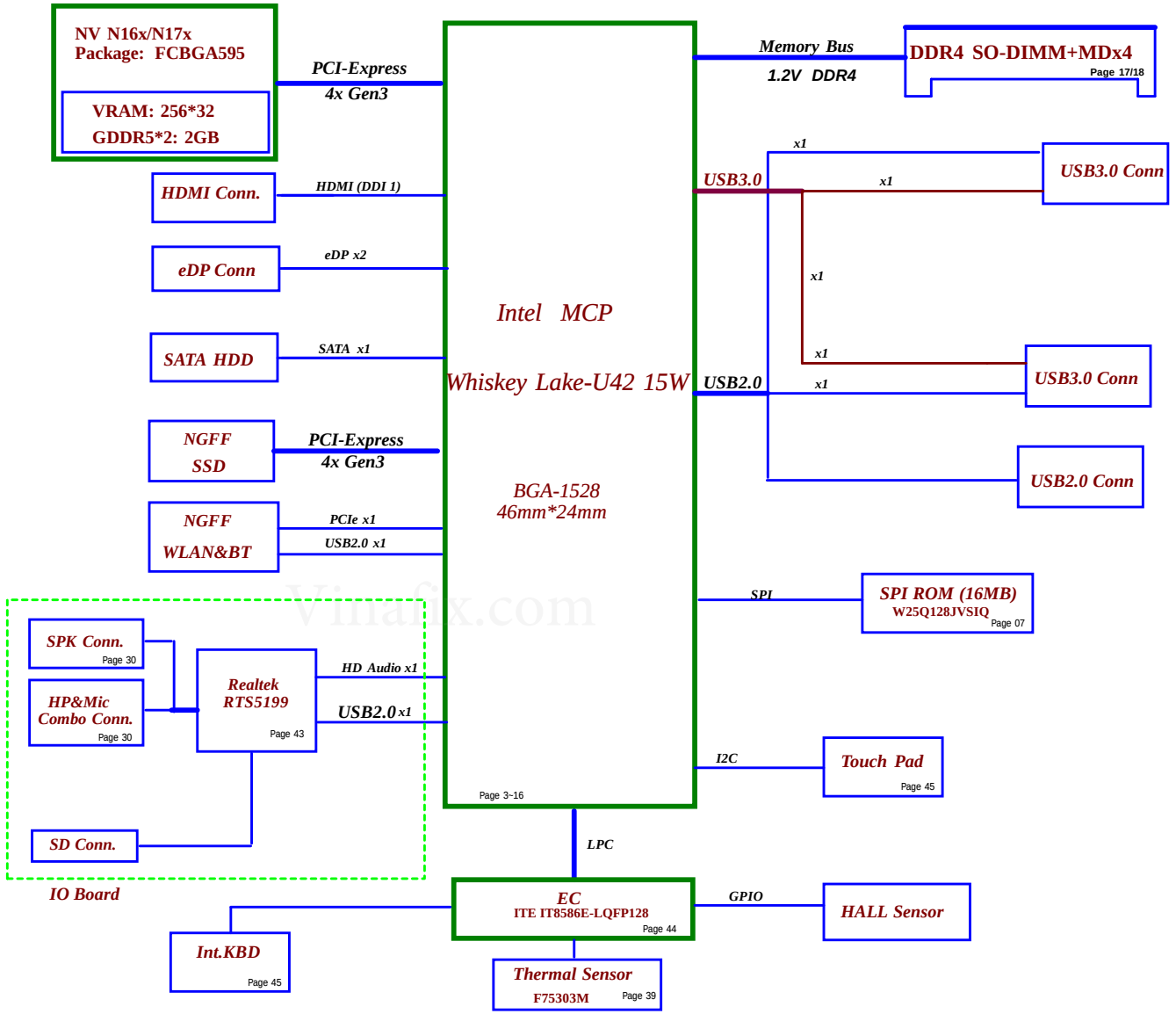

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Title: Block Diagram

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.05VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE / SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT		Function
USB3.0	1	USB3.0 Conn
	2	USB3.0 Conn
	3	NC
	4	NC
	5	NC
	6	NC
USB2.0	1	USB3.0 Conn
	2	NC
	3	USB3.0 Conn
	4	USB2.0 conn
	5	Card reader
	6	Touch Screen
	7	Camera
	8	NC
	9	NC
	10	Bluetooth
PCIE	5~8 X4	DGPU
	9	WLAN
	10	NC
	11	SATA HDD
	12	NC
	13~16 X4	PCIE/SATA SSD

BOM Structure	BTO Item
@	Un-stuff
14@	For 14" part
15@	For 15" part
YOGA@	For YOGA530 part
530@	For 530S part
CD@	For C cost down
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC un-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ME@	For ME part
OPT@	For NV GPU part
OPTN16@	For NV N16S-GTR GPU part
OPTN17@	For NV N17S-G1 GPU part
TS@	For touch screen part
TP@	For TOuch Pad Part
UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

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Title: **Notes List**

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HDMI D2
HDMI D1
HDMI D0
HDMI CLK

34 CPU_HDMI_TXN2 / CPU_HDMI_TXP2 / CPU_HDMI_TXN1 / CPU_HDMI_TXP1 / CPU_HDMI_TXN0 / CPU_HDMI_TXP0 / CPU_HDMI_CLKN / CPU_HDMI_CLKP

DDP*_CTRLDATA strapping sampled on the rising edge of PCH_PWROK

Port	Strap	Enable	Disable
Port 1	GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Pull up to 3.3 V with 2.2Kohm *	NC
Port 2	GPP_E21 / DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC *
Port 3	GPP_E23 / DDPD_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC *
Reserve	GPP_H17/ DPPF_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC *

100Ohm for CNL

+VCCIO&EDP_COMP :
Trace Width: 20mil
Isolation Spacing: 25mil
Max length: 100mil

+VCCIO — RC406 2 — 1 24.9_0402_1% — DP_COMP_OBS_DP — AM6 DISP_RCOMP

34 PCH_HDMI_DDC_CLK — PCH_HDMI_DDC_CLK — CC8 GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
34 PCH_HDMI_DDC_DATA — PCH_HDMI_DDC_DATA — CC9 GPP_E19/DPPB_CTRLDATA

CH4 GPP_E20/DPPC_CTRLCLK
CH3 GPP_E21/DPPC_CTRLDATA

CP4 GPP_E22/DPPD_CTRLCLK
CN4 GPP_E23/DPPD_CTRLDATA

CR26 GPP_H16/DDPF_CTRLCLK
CP26 GPP_H17/DDPF_CTRLDATA

+3VS — RPC401 1 2 4 3 — PCH_HDMI_DDC_CLK / PCH_HDMI_DDC_DATA — 2.2K_0404_4P2R_5%

UC1A — 1 of 20 — WHISKEYLAKE-U_BGA1528 @

DDI1_TXN_0 AL5 / DDI1_TXP_0 AL6 / DDI1_TXN_1 AJ5 / DDI1_TXP_1 AJ6 / DDI1_TXN_2 AF6 / DDI1_TXP_2 AF5 / DDI1_TXN_3 AE5 / DDI1_TXP_3 AE6
DDI2_TXN_0 AC4 / DDI2_TXP_0 AC3 / DDI2_TXN_1 AC1 / DDI2_TXP_1 AC2 / DDI2_TXN_2 AB3 / DDI2_TXP_2 AB2 / DDI2_TXN_3 AB1 / DDI2_TXP_3 AB5

EDP_TXN_0 AG4 / EDP_TXP_0 AG3 / EDP_TXN_1 AG2 / EDP_TXP_1 AG1 / EDP_TXN_2 AJ4 / EDP_TXP_2 AJ3 / EDP_TXN_3 AJ2 / EDP_TXP_3 AJ1
CPU_EDP_TX0- / CPU_EDP_TX0+ / CPU_EDP_TX1- / CPU_EDP_TX1+ — 33 — CPU_EDP_TX0- / CPU_EDP_TX0+ / CPU_EDP_TX1- / CPU_EDP_TX1+

EDP_AUX_N AH4 / EDP_AUX_P AH3
CPU_EDP_AUX# / CPU_EDP_AUX — 33 — CPU_EDP_AUX# / CPU_EDP_AUX

DISP_UTILS AM7

DDI1_AUX_N AC7 / DDI1_AUX_P AC6 / DDI2_AUX_N AD4 / DDI2_AUX_P AD3 / DDI3_AUX_N AG7 / DDI3_AUX_P AG6

GPP_E13/DDPB_HPD0/DISP_MISC0 — CN6 CPU_HDMI_HPD — CPU_HDMI_HPD 34
GPP_E14/DDPC_HPD1/DISP_MISC1 — CM6
GPP_E15/DPPD_HPD2/DISP_MISC2 — CP7 CNVI_EN# — CNVI_EN# 40
GPP_E16/DPPE_HPD3/DISP_MISC3 — CP6 GPP_E16 — RC4321 2 0_0402_5% — EC_SCI# — EC_SCI# 44
GPP_E17/EDP_HPD/DISP_MISC4 — CM7 CPU_EDP_HPD — CPU_EDP_HPD 33

Change EC_SCI# to GPP_E16 based on CRB

EDP_BKLTEN CK11 PCH_ENBKL — PCH_ENBKL 33,44
EDP_VDDEN CG11 PCH_ENVDD — PCH_ENVDD 33
EDP_BKLTCTL CH11 PCH_EDP_PWM — PCH_EDP_PWM 33

CPU_EDP_HPD / PCH_ENVDD — RPC806 1 2 4 3 — 100K_0404_4P2R_5%

GPP_E16 — RC404 1 — 2 10K_0402_5%

+3VS

+VCCSTG — RC408 1K_0402_5%
44,55 H_PROCHOT# — 44 H_PECI — RC4091 2 499 +-1% 0402
CATERR# AA4 / H_PECI AR1 / H_PROCHOT#_R Y4 / H_THRMTRIP# BJ1

+VCCST_CPU — RC407 49.9_0402_1% @

RC410 1K_0402_5%
+VCCST_CPU

XDP_BPM0# U1 / XDP_BPM1# U2 / XDP_BPM2# U3 / XDP_BPM3# U4
PAD @ TC403 / TC404 / TC405 / TC406

PAD @ TC407 — GPP_E3 — CE9 GPP_E3/CPU_GP0 / CN3 GPP_E7/CPU_GP1 / CB33 GPP_B3/CPU_GP2 / CC33 GPP_B4/CPU_GP3

Need to confirm stuff or not?

RC413 1 — 2 49.9_0402_1%
RC414 1 — 2 49.9_0402_1%
PROC_OPI_RCOMP — PCH_OPI_RCOMP — BP27 PROC_POPIRCOMP / BW25 PCH_OPIRCOMP / L5 RSVD35 / N5 RSVD36

UC1D — WHISKEYLAKE-U_BGA1528 @

CATERR# AA4 / PECI AR1 / PROCHOT# Y4 / THRMTRIP# BJ1
BPM#_0 U1 / BPM#_1 U2 / BPM#_2 U3 / BPM#_3 U4
PCH_TCK U5 / PCH_TDI W5 / PCH_TDO P5 / PCH_TMS Y6 / PCH_TRST# P6 / PCH_JTAGX P8
PROC_POPIRCOMP / PCH_OPIRCOMP / RSVD35 / RSVD36

PROC_TCK T6 — PROC_TCK — 1 — IT13
PROC_TDI U6 — PROC_TDI — 1 — IT10
PROC_TDO Y5 — PROC_TDO — 1 — IT9
PROC_TMS T5 — PROC_TMS — 1 — IT11
PROC_TRST# AB6 — PROC_TRST# — 1 — IT20

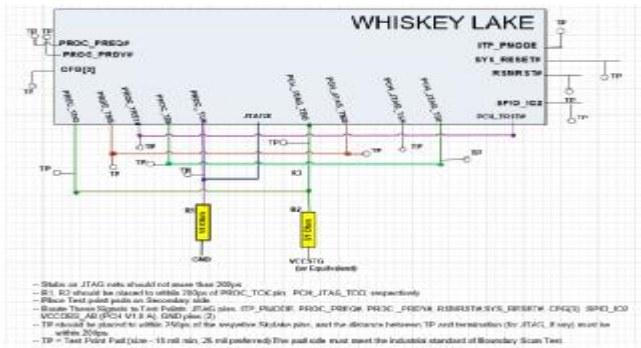
PCH_TCK W6 — PCH_TCK — 1 — IT12
PCH_TDI U5 — PROC_TDI
PCH_TDO W5 — PROC_TDO
PCH_TMS P5 — PROC_TMS
PCH_TRST# Y6 — PROC_TRST#
PCH_JTAGX P8 — PROC_TCK

PROC_PREQ# W2 — PROC_PREQ# — 1 — IT22
PROC_PRDY# W1 — PROC_PRDY# — 1 — IT21

+VCCSTG — RC408 1K_0402_5%

PROC_TDO — R95 51_0402_1%
PROC_TCK — RC176 51_0402_1%

Mount RC176 to enable DCI function



– Stubs on JTAG rails should not exceed 6mil 200ps
– R1, R2 should be placed to within 280ps of PROC_TCK pin. PCH_JTAG_TDO, respectively
– Place Test point pads on Secondary side
– Route These Signals to Test Points: JTAG pins: ITP_PMODE, PROC_PREQ#, PROC_PRDY#, RSMRST#,SYS_RESET#, CFG[3], SPI0_IO2
VCCDSW_AB (PCH V1.8 A), GND pins (2)
– TP should be placed to within 250ps of the respective Skylake pins, and the distance between TP and termination (for JTAG, if req'd) must be within 200ps
– TP = Test Point Pad (size – 15 mil min, 25 mil preferred) the pad side must meet the industrial standard of Boundary Scan Test

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Title: **MCP (DDI,EDP)**

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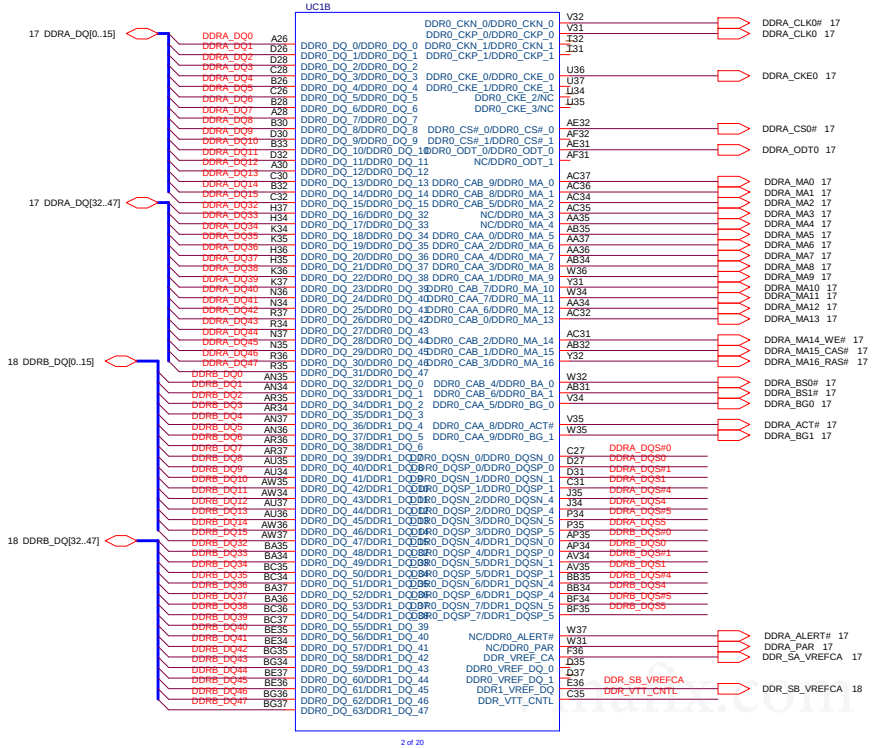

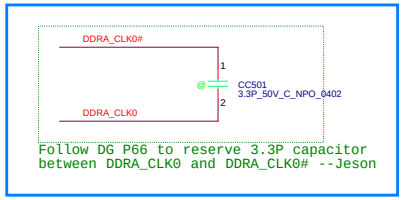

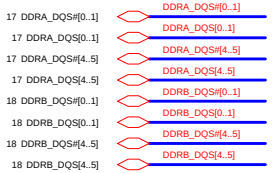

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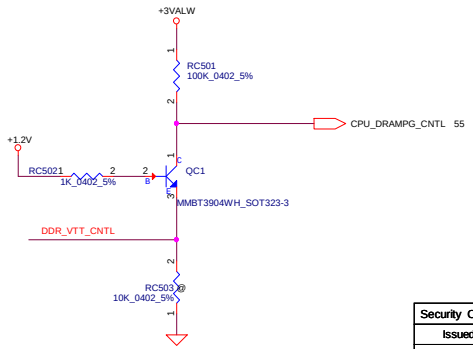

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Title: **MCP (DDR4)**

Size	Document Number	Rev
Custom	FS441/FS540	0.1
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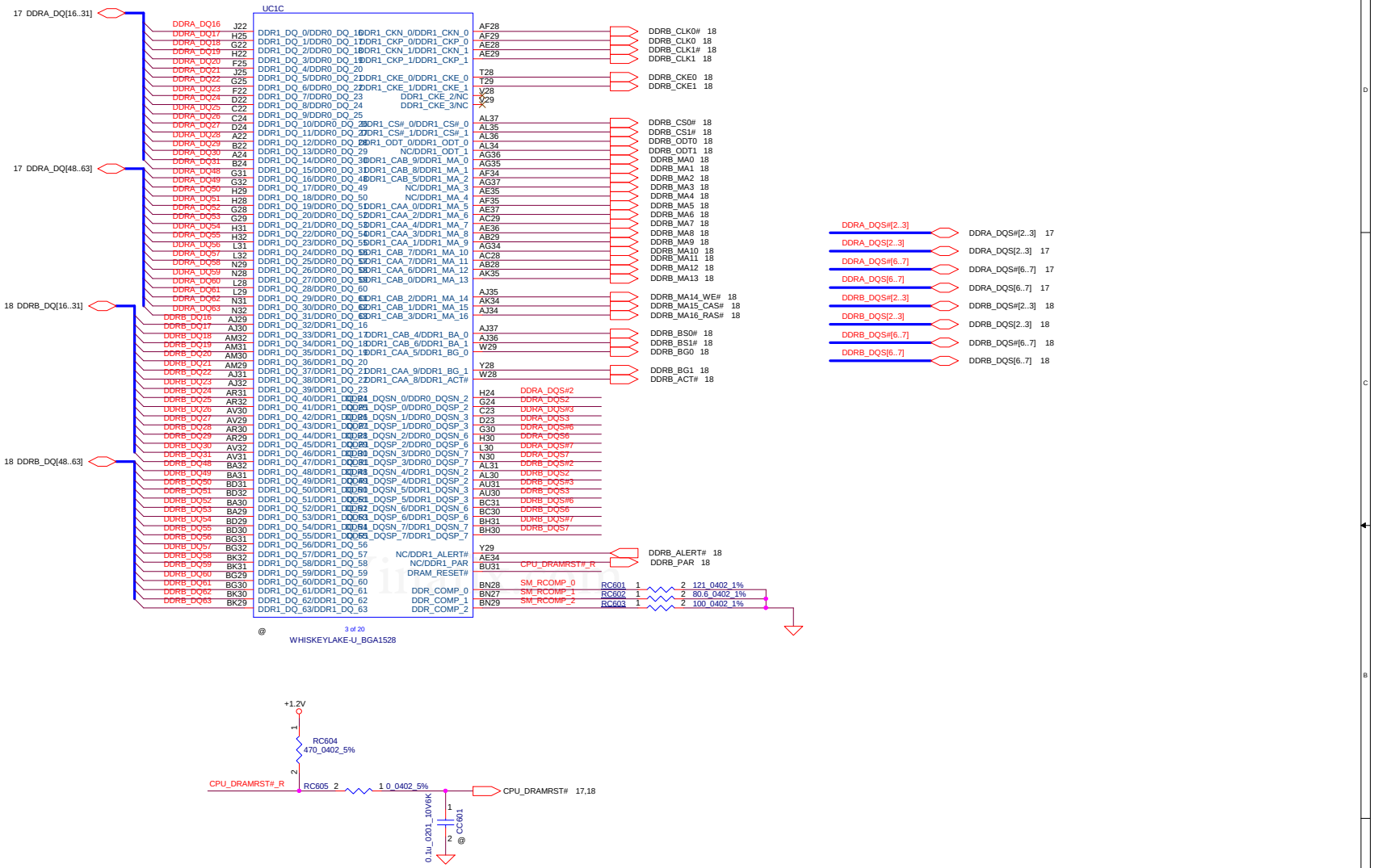

Security Classification	LC Future Center Secret Data		
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Title: **MCP (DDR4)**

Size	Document Number	Rev
Custom	**FS441/FS540**	0.1

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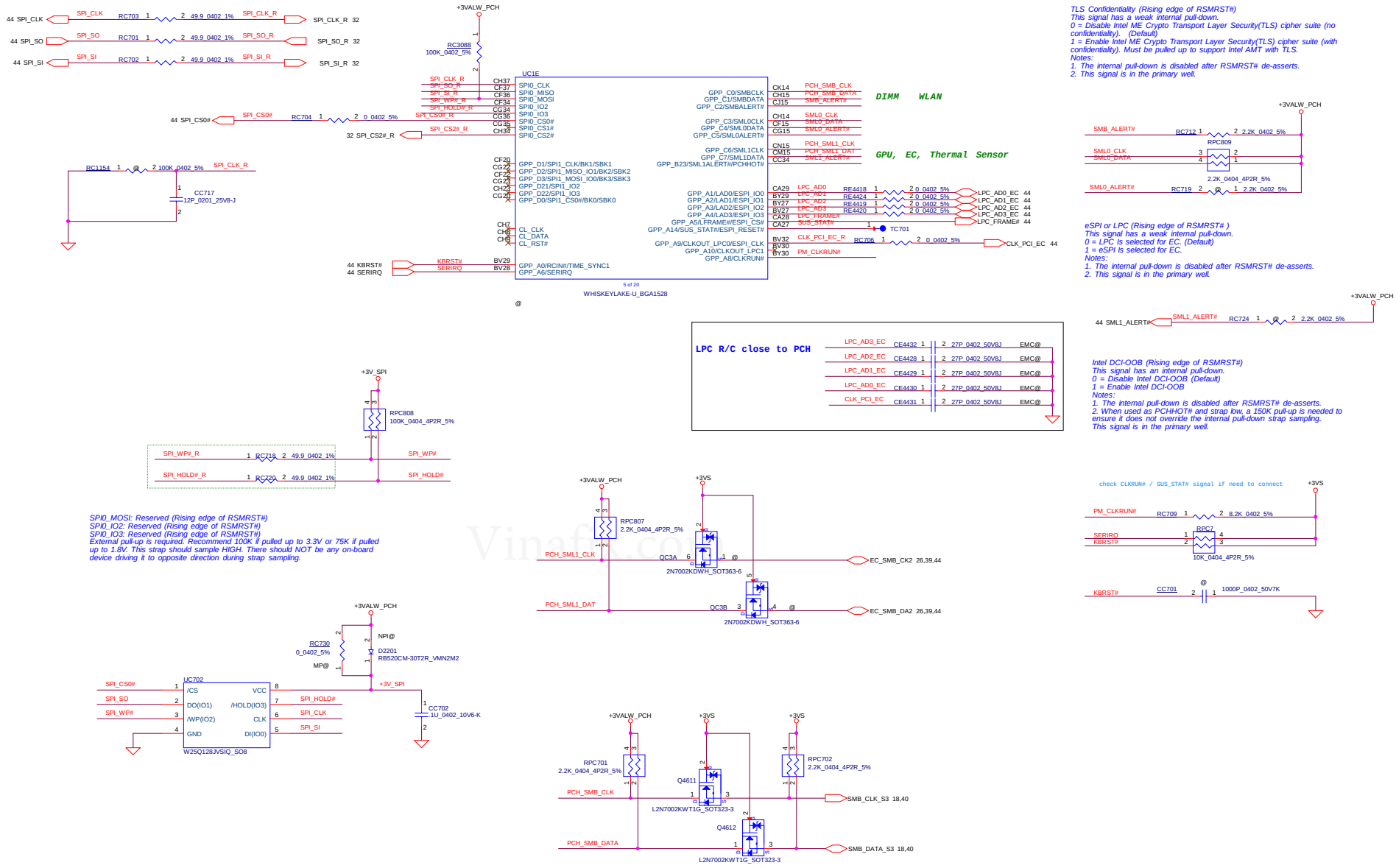

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Title: MCP (JTAG,SPI,LPC,SMB)

Size	Document Number	Rev
C	FS441/FS540	0.1
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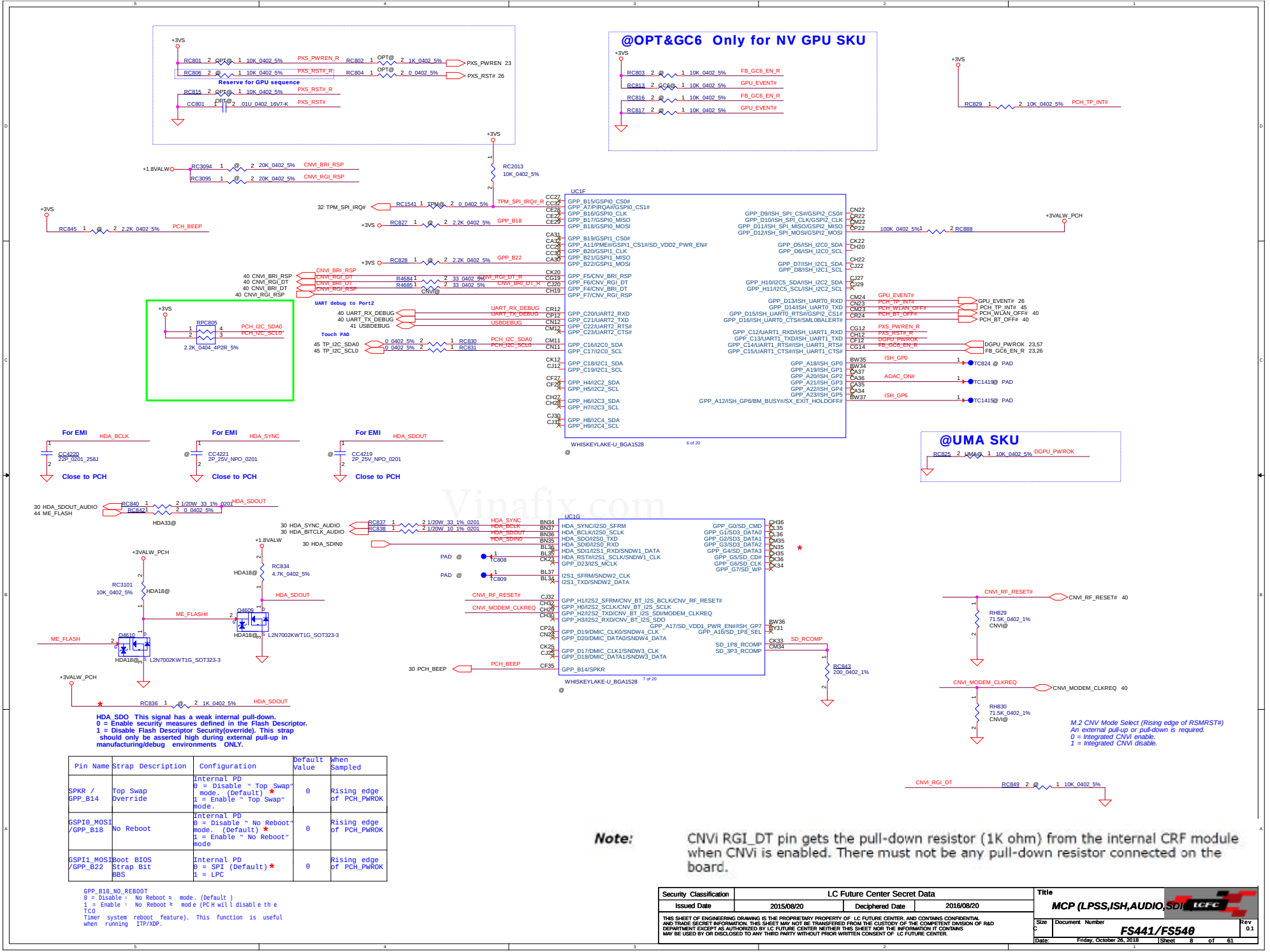

Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable " Top Swap" mode. (Default) * 1 = Enable " Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPI0_MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable " No Reboot" mode. (Default) * 1 = Enable " No Reboot" mode	0	Rising edge of PCH_PWROK
GSPI1_MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) * 1 = LPC	0	Rising edge of PCH_PWROK

GPP_B18_NO_REBOOT
0 = Disable : No Reboot ≈ mode. (Default)
1 = Enable : No Reboot ≈ mode (PCH will disable the TCO
Timer system reboot feature). This function is useful when running ITP/XDP.

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Title: MCP (LPSS,ISH,AUDIO,SDI

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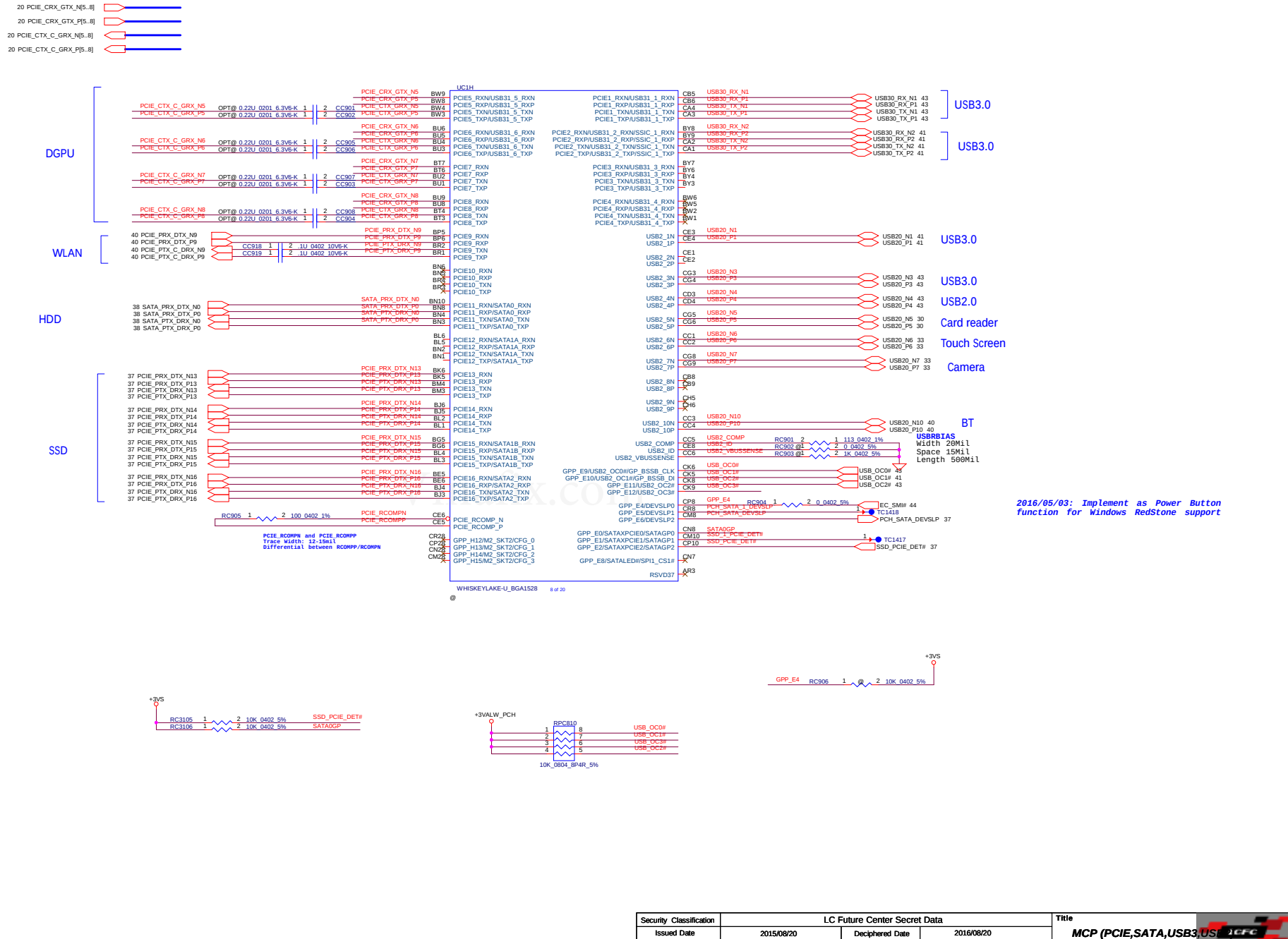

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Title: MCP (PCIE,SATA,USB3.USB2)

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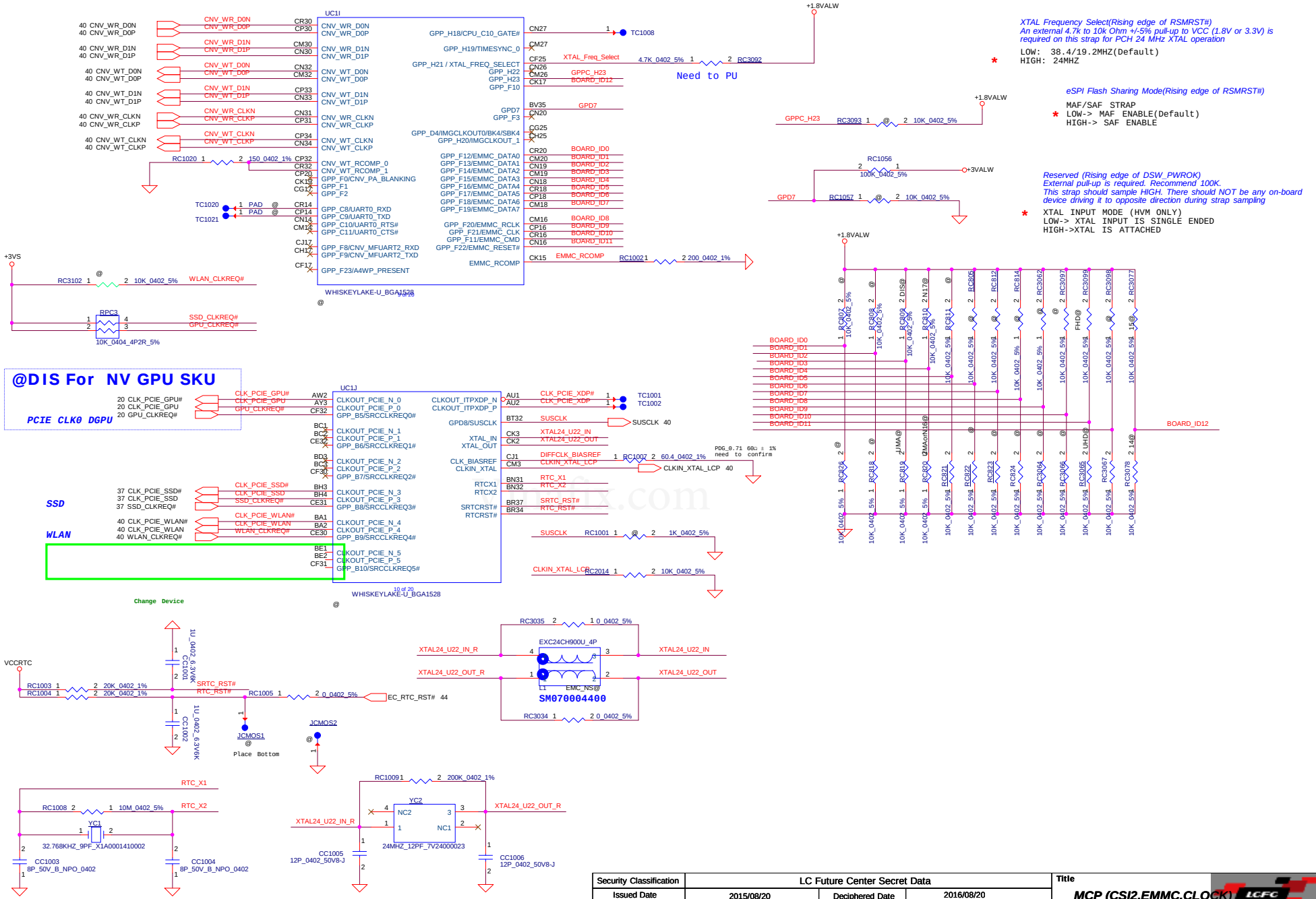

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Title: MCP (CSI2,EMMC,CLOCK)

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- **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]**: Reserved configuration lane.
- **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]**: Reserved configuration lane.
- **CFG[4]**: eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]**: PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]**: PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]**: Reserved configuration lanes.

UC1K

CC1101 0.1U_0402_25V6 EMC_NS@

32 PLT_RST# — RC1101 0_0402_5% — PLT_RST#_R — SYS_RESET# — PCH_RSMRST#_R — BJ35 CN10 BR36

44 EC_RSMRST# — RC1102 0_0402_5%

VCCST_PWRGD_R — TC1101 — RC1103 60.4_0402_1% — CPU_PROCPWRGD — VCCST_PWRGD — AR2 BJ2

44 SYS_PWROK — RC1106 0_0402_5% — SYS_PWROK_R — CR10

44 PCH_PWROK — RC1107 0_0402_5% — PCH_PWROK_R — BP31

EC_RSMRST# — RC1119 0_0402_5% — PCH_DPWROK_R — BP30

SUSWARN# — RC1189 @ 10K_0402_5% — SUSACK# — BV34 BY32

40 PCIE_WAKE# — PCIE_WAKE# — PCH_LAN_WAKE# — BU30 BU32

TC1408 — LANPHYPC — BU34

GPP_B13/PLTRST# SYS_RESET# RSMRST#

PROCPWRGD VCCST_PWRGOOD

SYS_PWROK PCH_PWROK DSW_PWROK

GPP_A13/SUSWARN#/SUSPWRDACK GPP_A15/SUSACK#

WAKE# GPD2/LAN_WAKE# GPD11/LANPHYPC

GPP_B12/SLP_S0# GPD4/SLP_S3# GPD5/SLP_S4# GPD10/SLP_S5#

SLP_SUS# SLP_LAN# GPD9/SLP_WLAN# GPD6/SLP_A#

GPD3/PWRBTN# GPD1/ACPRESENT GPD0/BATLOW#

INTRUDER#

GPP_B11/EXT_PWR_GATE# GPP_B2/VRALERT#

INPUT3VSEL

BJ37 — TC1110 — PM_SLP_S3# 44

BU36 BU27 BT29 — TC1109 — PM_SLP_S4# 44

BU29 — TC1407

BT31 BT30 BU37 — PM_SLP_WLAN# 40

BU28 — PBTN_OUT#_R — RC1108 0_0402_5% — PBTN_OUT# 44

BU35 — AC_PRESENT_R

BV36 — BATLOW#

BR35 — INTVRMEN — RC1109 1M_0402_5% — VCCRTC — +3VALW_PCH

CC37 — 100K_0402_5% — RC3100

CC36

BT27 — RC1188 4.7K_0402_5%

3.0V Select (Input pin must always be driven to a valid logic level)
External pull-up or pull-down is required
0 = 3.3V supply is 3.3V +/- 5%
1 = 3.3V supply is 3.0V +/- 5%
Note: This strap should only be used for specific targeted 1S battery systems

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WHISKEYLAKE-U_BGA1528

+3VALW

RC1112 8.2K_0402_5% — BATLOW#

RC1113 1K_0402_5% — PCIE_WAKE#

RPC6 — AC_PRESENT_R — PCH_LAN_WAKE#

10K_0404_4P2R_5%

+3VALW_PCH

RC1117 @ 10K_0402_5% — SUSWARN#

+3VS

RC1118 10K_0402_5% — SYS_RESET#

44 AC_PRESENT — RC1110 0_0402_5% — AC_PRESENT_R

+VCCST_CPU

RC1115 1K_0402_5%

44 EC_VCCST_PWRGD — RC1116 22_0402_5% — VCCST_PWRGD_R

CC1102 1000P_0402_50V7K @

RC3083 100K_0402_5% — PCH_RSMRST#_R

RC3103 10K_0402_5% — PCH_PWROK

RC3104 10K_0402_5% — SYS_PWROK

330P_0402_50V7K — CC1108

100K_0402_5% — RC1124 — PLT_RST#_R

10K_0402_5% — RC3069 @ — AC_PRESENT_R

RPC811 — PM_SLP_S3# — PM_SLP_S4#

100K_0404_4P2R_5%

1000P_0402_50V7K @ — CC1103 — PCH_RSMRST#_R

Stuff to fix Reset&PWRGD test fail issue

1000P_50V_K_X7R_0201 — CC1104 — PCH_PWROK

1000P_0402_50V7K @ — CC1105 — +3VALW_PG

0.01U_0201_10V6K — CC4234 @ — SYS_PWROK

0.01U_0201_10V6K — CC1107 @ — EC_RSMRST#

Add to fix Reset&PWRGD test fail issue

54 +3VALW_PG — RC1122 0_0402_5% @ — +3V_PWRGD_R

54,55 ALW_PWRGD — RC1123 0_0402_5%

D5101 — RB521CM-30T2R_VMN2M-2 — EC_RSMRST#

U4404 — SN74LVC1G17DCKR_SC70-5

+3VALW

PLT_RST# — PLT_RST#_B 26,37,40,44

PLT_RST# — RC3107 0_0402_5% — PLT_RST#_B

V0.2 add PLT_RST# buffer

UC1Q

TC1103 — CPU_CFG0 — CFG_0

TC1126 — CPU_CFG1 — CFG_1

TC1409 — CPU_CFG2 — CFG_2

IT19 — CPU_CFG3 — CFG_3

CPU_CFG4 — CFG_4

TC1410 — CPU_CFG5 — CFG_5

TC1411 — CPU_CFG6 — CFG_6

TC1412 — CPU_CFG7 — CFG_7

CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_18 CFG_17 CFG_19

RC1172 1K_0402_5%

RC1163 49.9_0402_1% — CFG_RCOMP

IT16 — ITP_PMODE

RSVD_TP5 RSVD_TP4 IST_TRIG RSVD_TP3 RSVD72 RSVD73 TP1 TP3 RSVD74 RSVD75 RSVD76 RSVD77 RSVD29 RSVD26 RSVD27 RSVD25 RSVD24 RSVD78 RSVD79 RSVD34 RSVD33 RSVD8 RSVD9 RSVD22 RSVD23 RSVD11 RSVD10 RSVD80 RSVD81 RSVD69 RSVD70 RSVD82 RSVD83 RSVD17 RSVD16 RSVD35 RSVD7 RSVD68 RSVD71 RSVD_TP1 RSVD67 RSVD84 RSVD1 RSVD30 RSVD66 RSVD85 RSVD32 RSVD31 SKTOCC#

TP2 VSS_392 TP5

CR35 — TC1414

G3,G4,C34,AJ27,AH26 are reserved Pin on WHL

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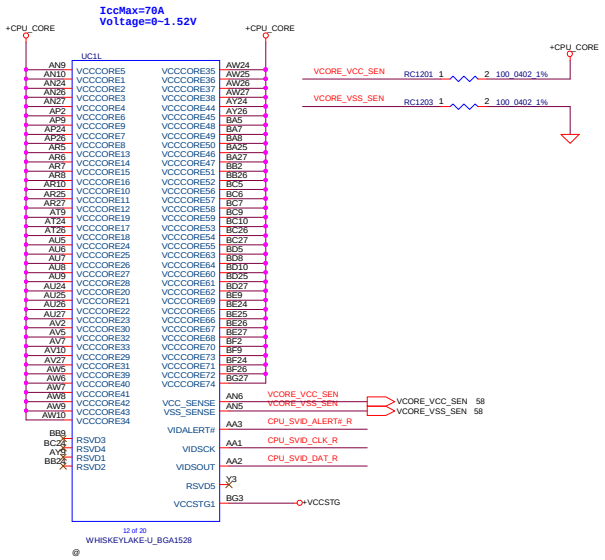
WHISKEYLAKE-U_BGA1528

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

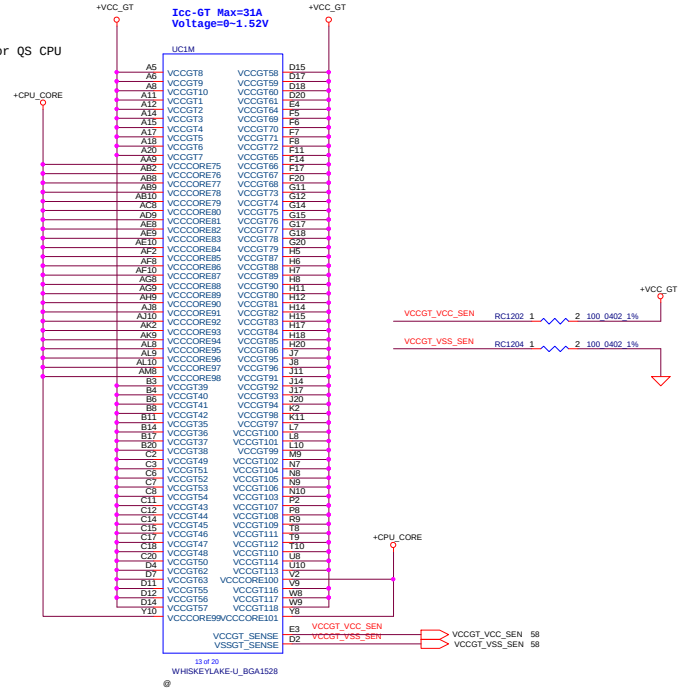
Title: MCP (SYSTEM PWR MANA[illegible])

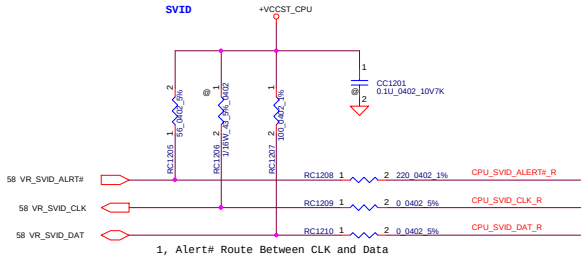
Size	Document Number	Rev
Custom	FS441/FS540	0.1

Date: Friday, October 26, 2018 | Sheet 11 of 61



Rename to +CPU_CORE for QS CPU





1, Alert# Route Between CLK and Data

Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

Title: MCP (CPU PWR1)

Size	Document Number	Rev
Custom	FS441/FS540	0.1
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WHL ES1 will be a CFL-U43e fused down to CFL-U42

* Pins marked RSVD must be left as NC

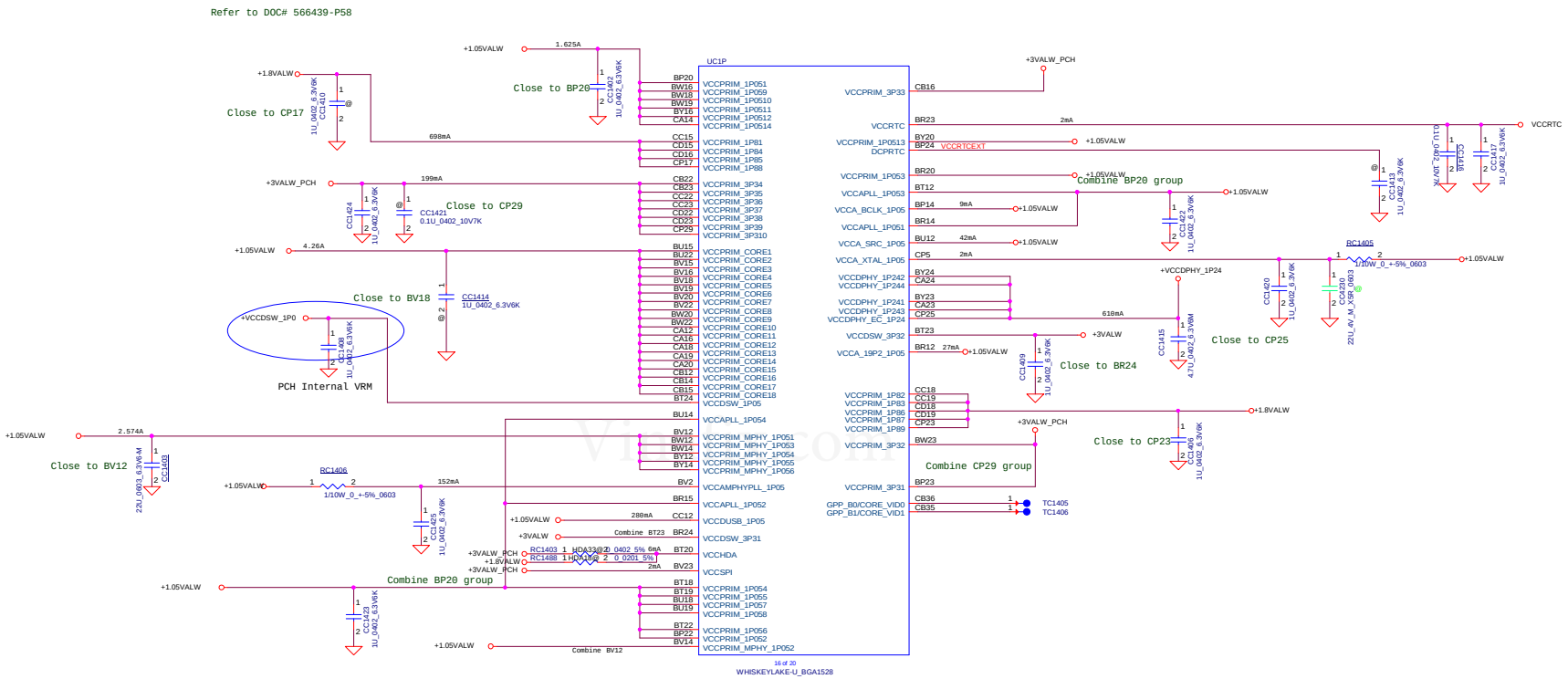
V_{DDQ}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603 6x 10uF 0402		
V_{CCIO}	4x 1uF 0201		Place underneath the package
	4x 1uF 0402/0201		Place as close to the package as possible
	6x 10uF 0402		
	4x 0402		*Placeholder Only*
V_{CCPLL_OC}	1x 1uF 0402		Do not merge V_{CCPLL}, V_{CCPLL_OC} and V_{CCST} to any noisy and high current power rail and do not route them close/adjacent to and reference to, any noisy and high current rail on top and bottmm layers - as this may impact to PLL failing to phase lock.
V_{CCPLL}	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		*Placeholder Only.* Can be placed on as either Primary or back side cap.
V_{CCST}	1x 1uF 0402		
V_{CCSTG}	1x 1uF 0402		
$V_{CCEOPIO}$		6x 1uF 0201	Place under BGA.
		2x 22uF 0603	$V_{CCEOPIO}$ and V_{CCOPC} rails are merged on board. VT to be placed as close as possible to BGA and a wide plane routing to meet DC_R <= 7mOhm.
V_{CCOPC}		4x 10uF 0402	
		2x 22uF 0603	$V_{CCEOPIO}$ and V_{CCOPC} is required for CFL-U43e SKUs only.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (CPU PWR2)

Size: Custom | Document Number: FS441/FS540 | Rev: 0.1

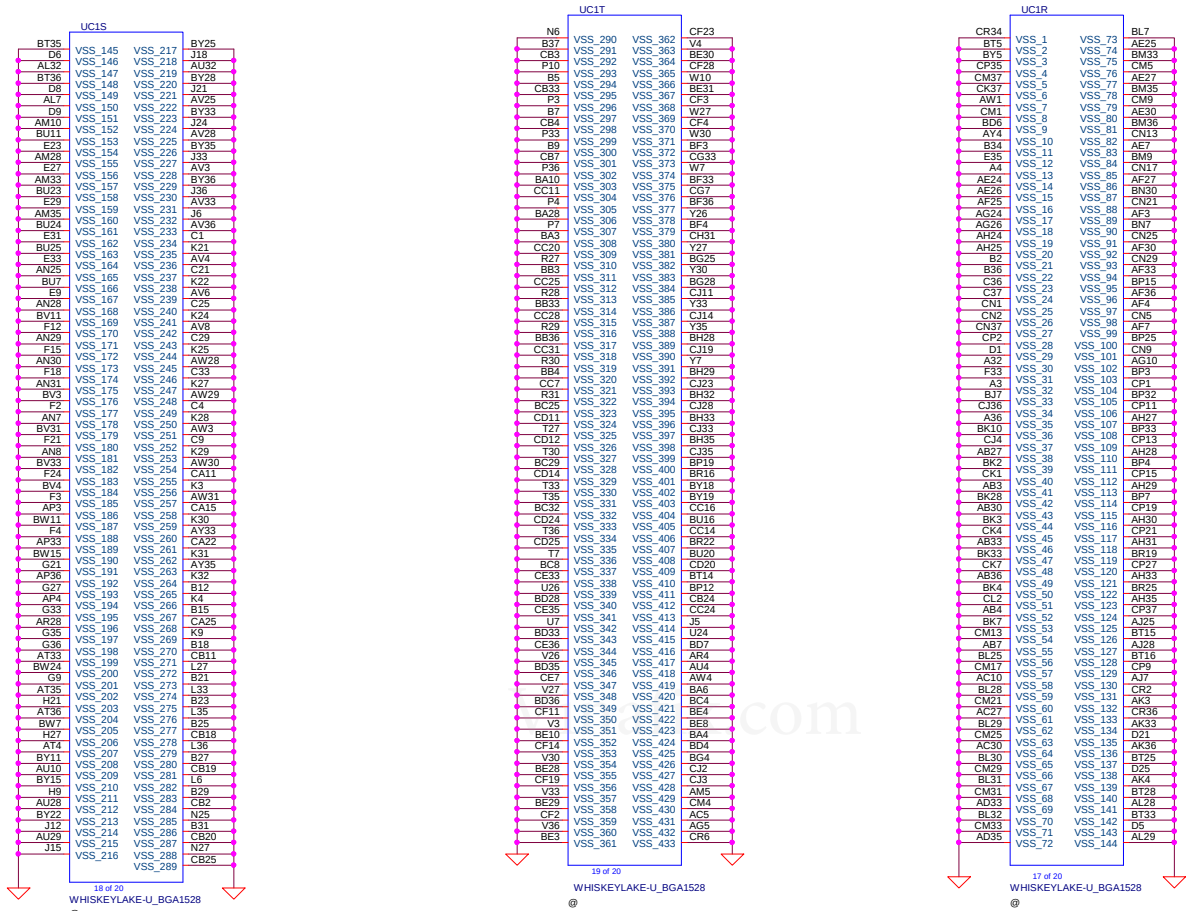
Date: Friday, October 26, 2018 | Sheet 13 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **MCP (PCH PWR)**

Size	Document Number	Rev
Custom	FS441/FS540	0.1
Date: Friday, October 26, 2018	Sheet 14 of 61	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (VSS)

Size	Document Number	Rev
Custom	FS441/FS540	0.1

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Place test points close to CPU

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

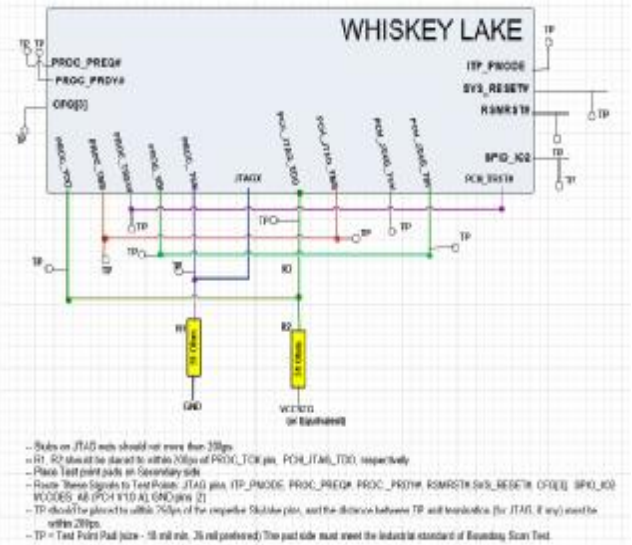
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC



- Stubs on JTAG nets should not exceed than 200ps.
- R1, R2 should be placed to within 200ps of PROC_TCK pin, PCH_JTAG_TDO, respectively
- Place Test point pads on Secondary side
- Route these Signals to Test Points: JTAG pins ITP_PMODE, PROC_PREQ#, PROC_PRDY#, RSMRST#,SYS_RESET#, CFG[0], SPKR_IO2, VCCDIES_AB (PCH Y10,AL6),GND pins (2)
- TP should be placed to within 750ps of the respective Stub/via pins, and the distance between TP and test probe (for JTAG, if any) must be within 200ps.
- TP = Test Point Pad (size - 18 mil min, 35 mil preferred) The pad side must meet the Industrial standard of Boundary Scan Test.

Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

Title: XDP

Size	Document Number	Rev
Custom	FS441/FS540	0.1

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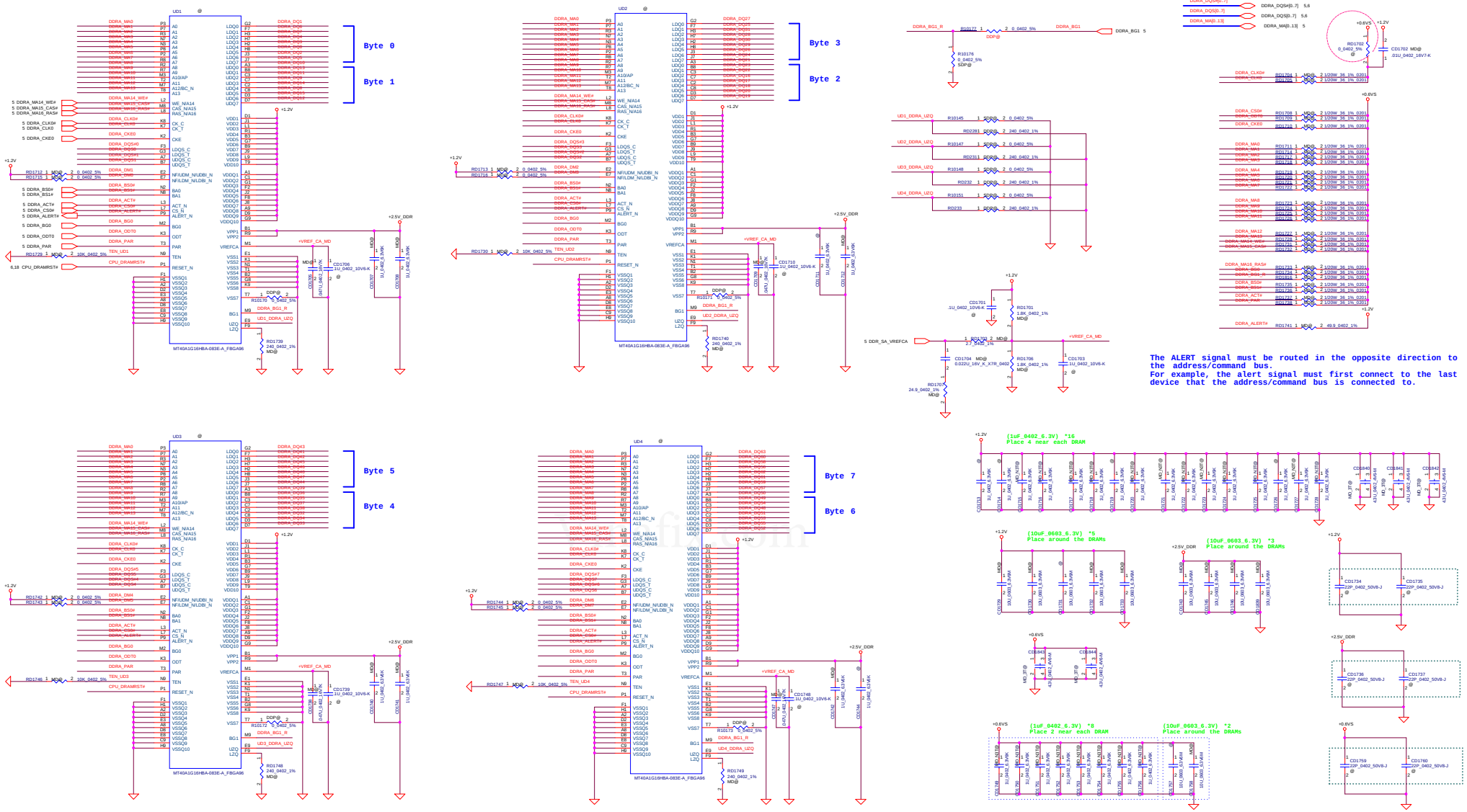
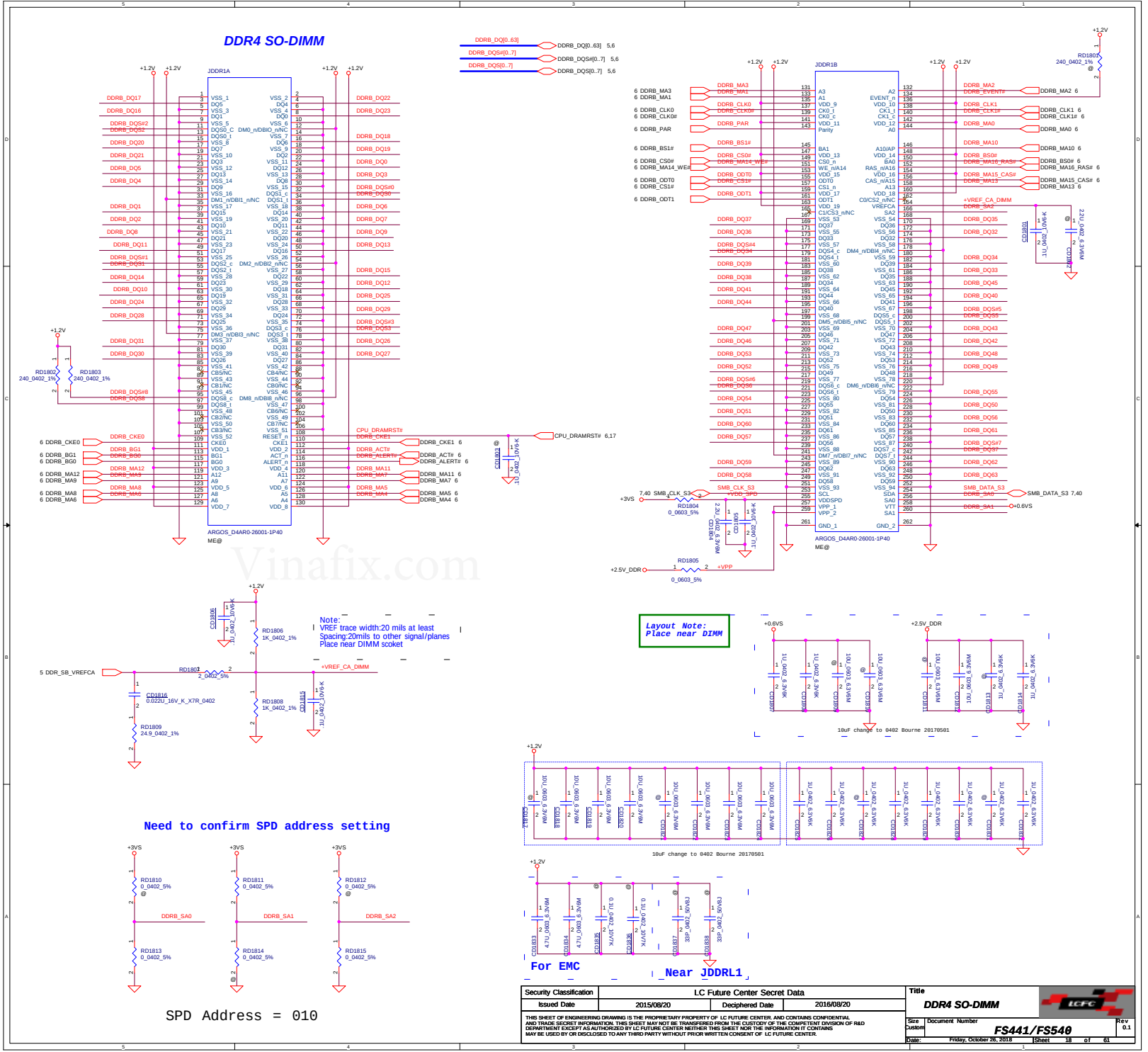
Apply X76 BOM to control DDP Memory Down stuff components!



Security Classification	LC Future Center Secret Data		
Issued Date	2017/06/24	Deciphered Date	2018/06/23

Title	DDR4 Memory Down		
Size	Document Number		Rev
Custom	FS441/FS540		0.1
Date:	Friday, October 26, 2018	Sheet 17 of 81	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title	DDR4 SO-DIMM		
Size: Custom	Document Number: FS441/FS540		Rev: 0.1
Date: Friday, October 26, 2018	Sheet 18 of 61		

N16x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU Core VDD PWM control signal
GPIO1	OUT	N/A	FB Enable for GC6 2.0
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

	GPU	Mem	Min Core Clk	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		(1.05V) (6)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

N16x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

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Title: *VGA Notes List*

Size	Document Number	Rev
C	FS441/FS540	0.1

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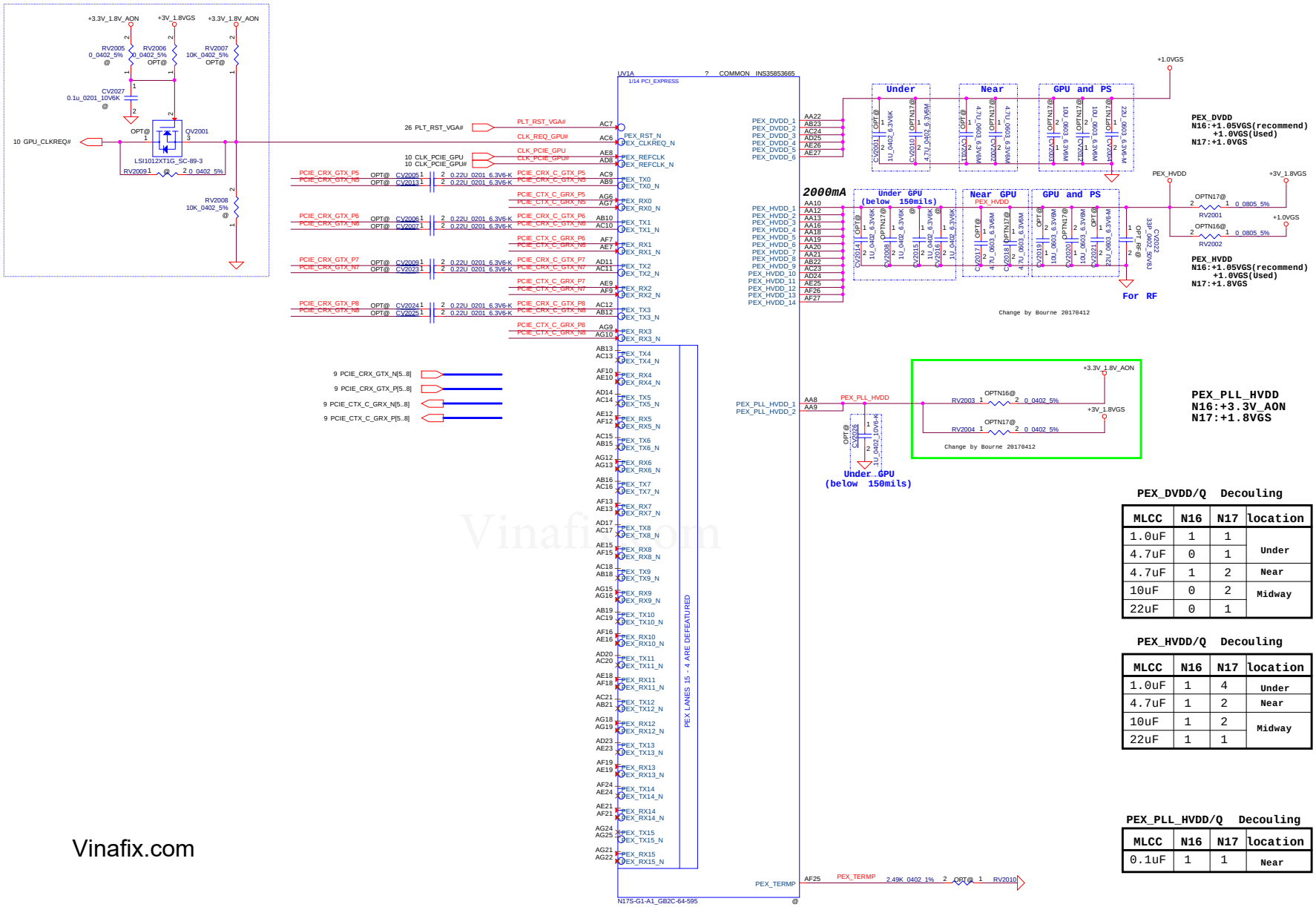

PEX_DVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	1	Under
4.7uF	0	1	
4.7uF	1	2	Near
10uF	0	2	Midway
22uF	0	1	

PEX_HVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	4	Under
4.7uF	1	2	Near
10uF	1	2	Midway
22uF	1	1	

PEX_PLL_HVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	1	1	Near

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **GPU_PCIE Interface**

Size	Document Number	Rev
C	FS441/FS540	0.1

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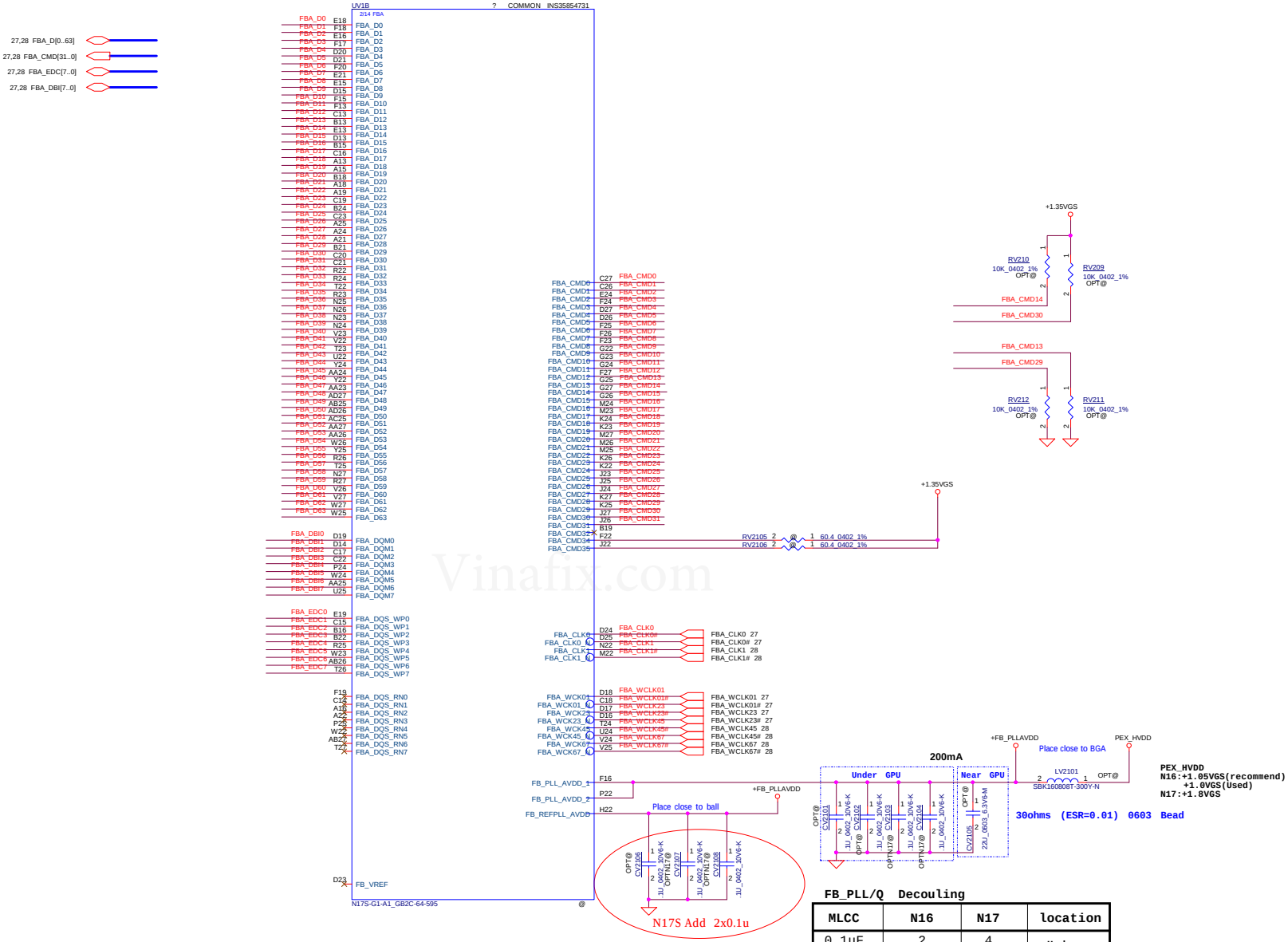

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_MEM Interface

Size	Document Number	Rev
C	FS441/FS540	0.1

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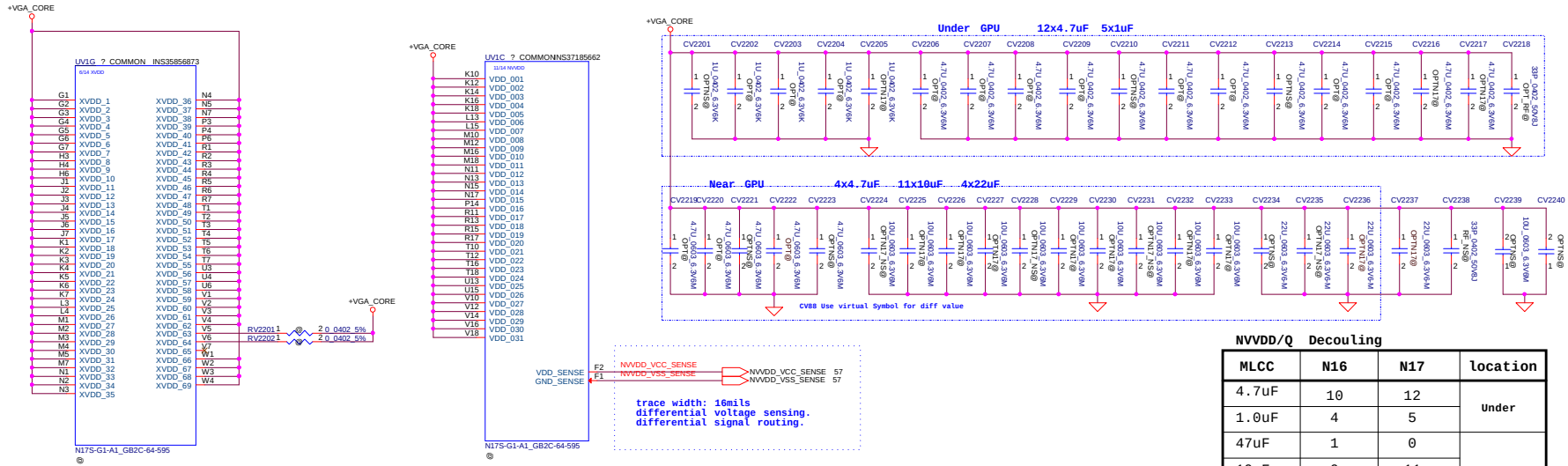
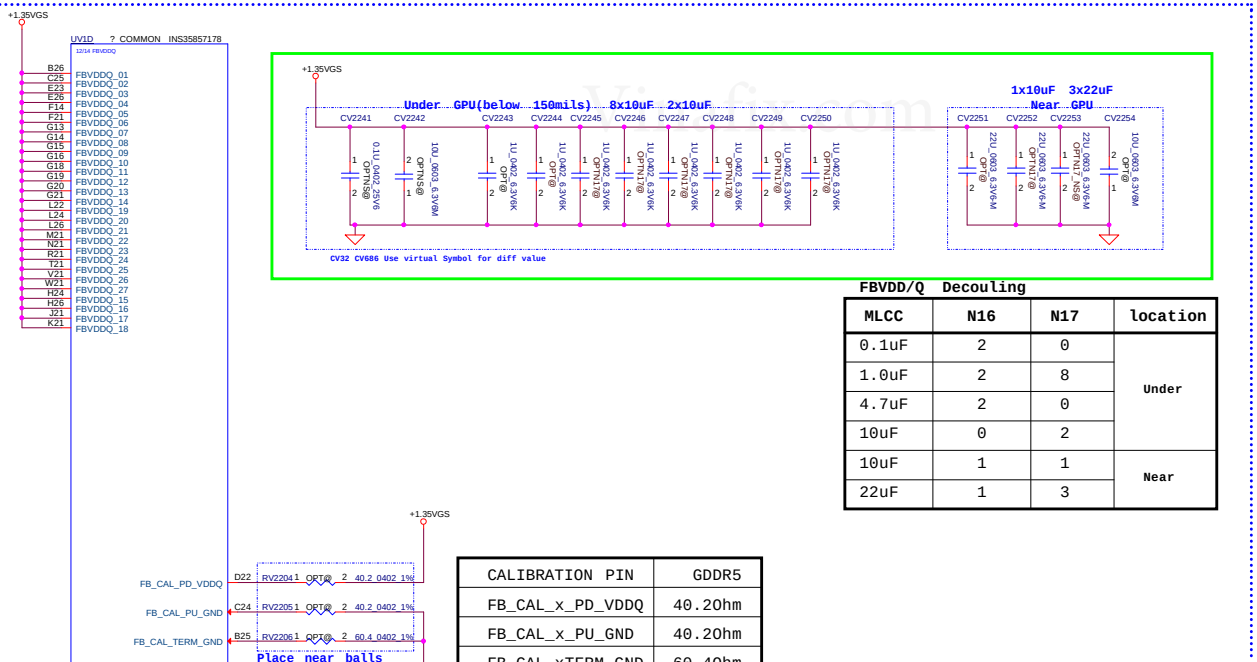


NVVDD/Q Decoupling

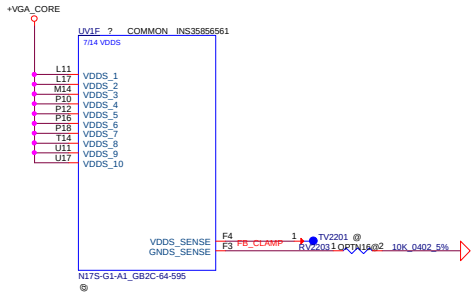
MLCC	N16	N17	location
4.7uF	10	12	Under
1.0uF	4	5	
47uF	1	0	Near
10uF	0	11	
22uF	1	4	
4.7uF	5	4	
330uF	1	2	



FBVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	0	Under
1.0uF	2	8	
4.7uF	2	0	
10uF	0	2	
10uF	1	1	Near
22uF	1	3	

CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm



Title: GPU_+VGA_CORE,FBVDDQ

Size	Document Number	Rev
C	FS441/FS540	0.1

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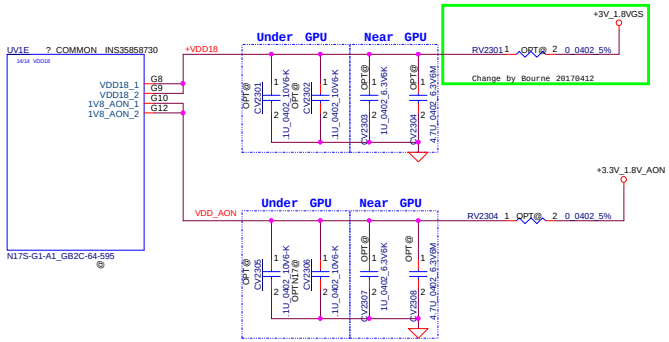


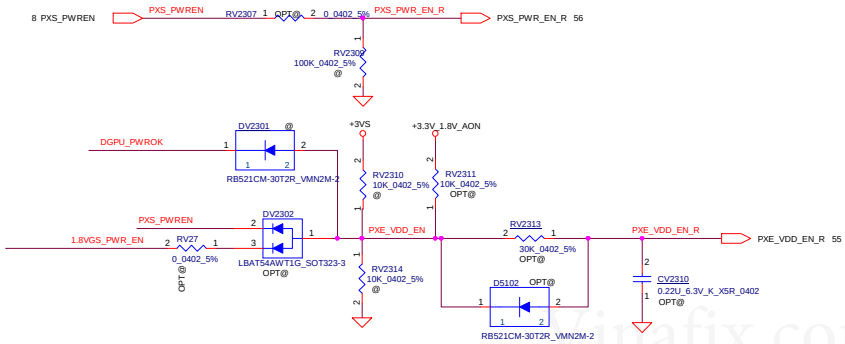
N16 3V3_MAIN(N17 VDD_18) Decouling

MLCC	N16	N17	location
0.1uF	2	2	Under
1.0uF	1	1	Near
4.7uF	1	1	

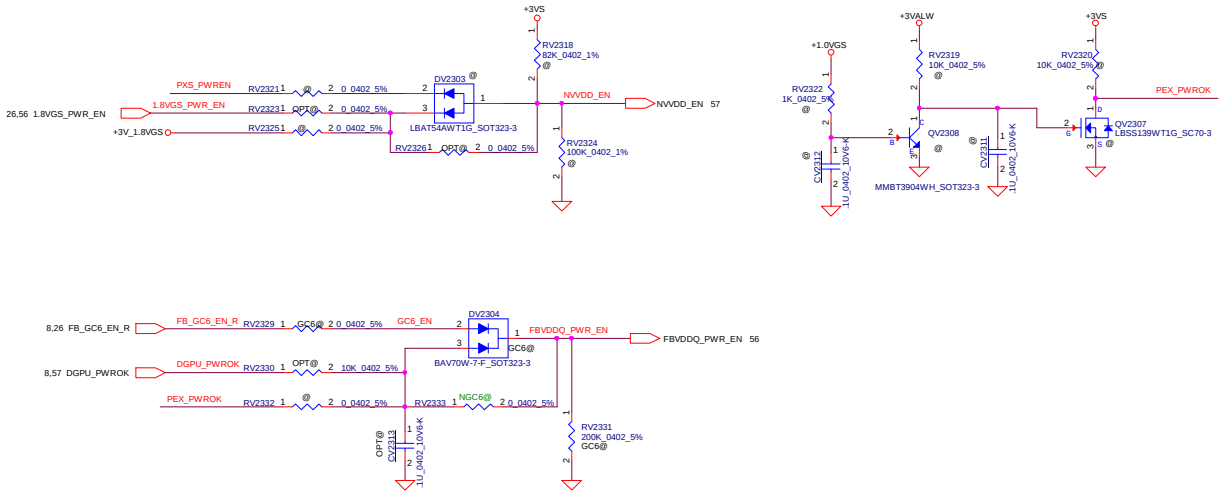
N16 3V3_AON(N17 1V8_AON) Decouling

MLCC	N16	N17	location
0.1uF	1	2	Under
1.0uF	1	1	Near
4.7uF	1	1	

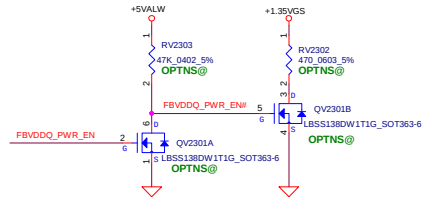
PXE_VDD & 1V8_AON

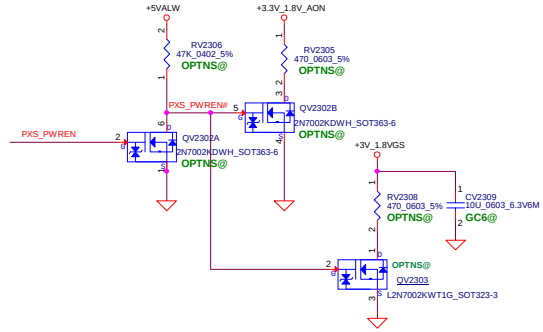


+1.8VG_AON TO +1.8VGS

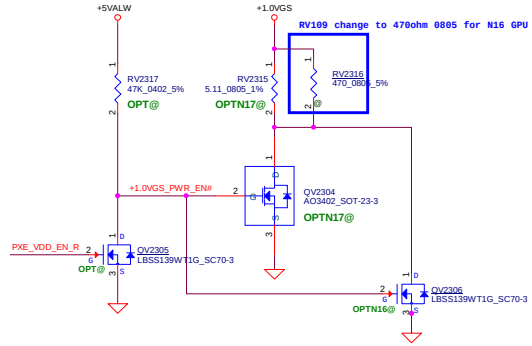


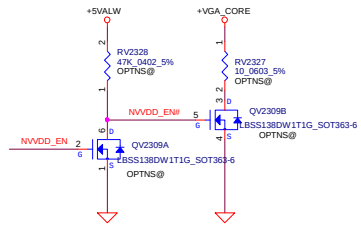
Discharge





RV2316 [illegible],N16 =470 ohm,N17= 5.11k





Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_AON/MAIN PWR/SEQ

Size	Document Number	Rev
C	FS441/FS540	0.1

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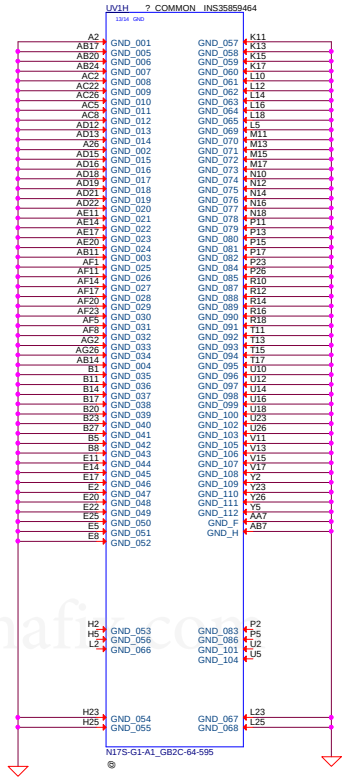

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **GPU_GND**

Size	Document Number	Rev
C	FS441/FS540	0.1

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PEX_PLLVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	NA	Under
1uF	1	NA	Near
4.7uF	1	NA	

PEX_PLLVDD
N16:+1.0VGS(recommend)
N17:NC

PEX_SVDD_3V3
N16:+3.3V_AON(recommend)
N17:NC

PEX_SVDD/Q Decoupling

MLCC	N16	N17	location
4.7uF	2	NA	Near

PEX_HVDD
N16:+1.05VGS(recommend)
+1.0VGS(Used)
N17:+1.8VGS

XS_PLLVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	1	1	Under
22uF	1	0	Near

SP_PLLVDD & VID_PLLVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	2	Under
10uF	1	0	Near
47uF	1	0	

GPCPLL_AVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	NA	1	Under
4.7uF	NA	1	Near
22uF	NA	1	

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_STRAP/DP/HDMI

Size: C | Document Number: FS441/FS540 | Rev: 0.1

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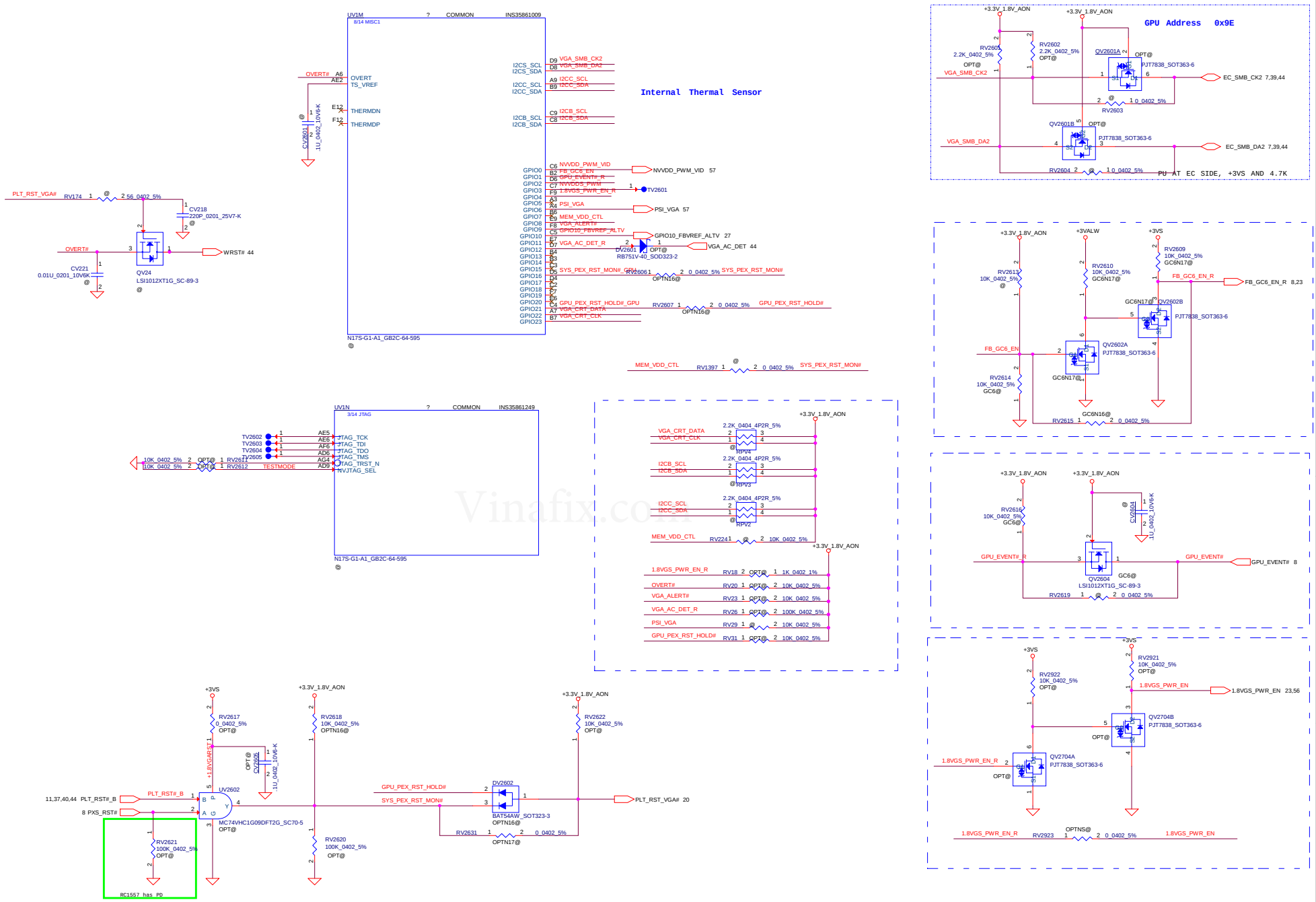

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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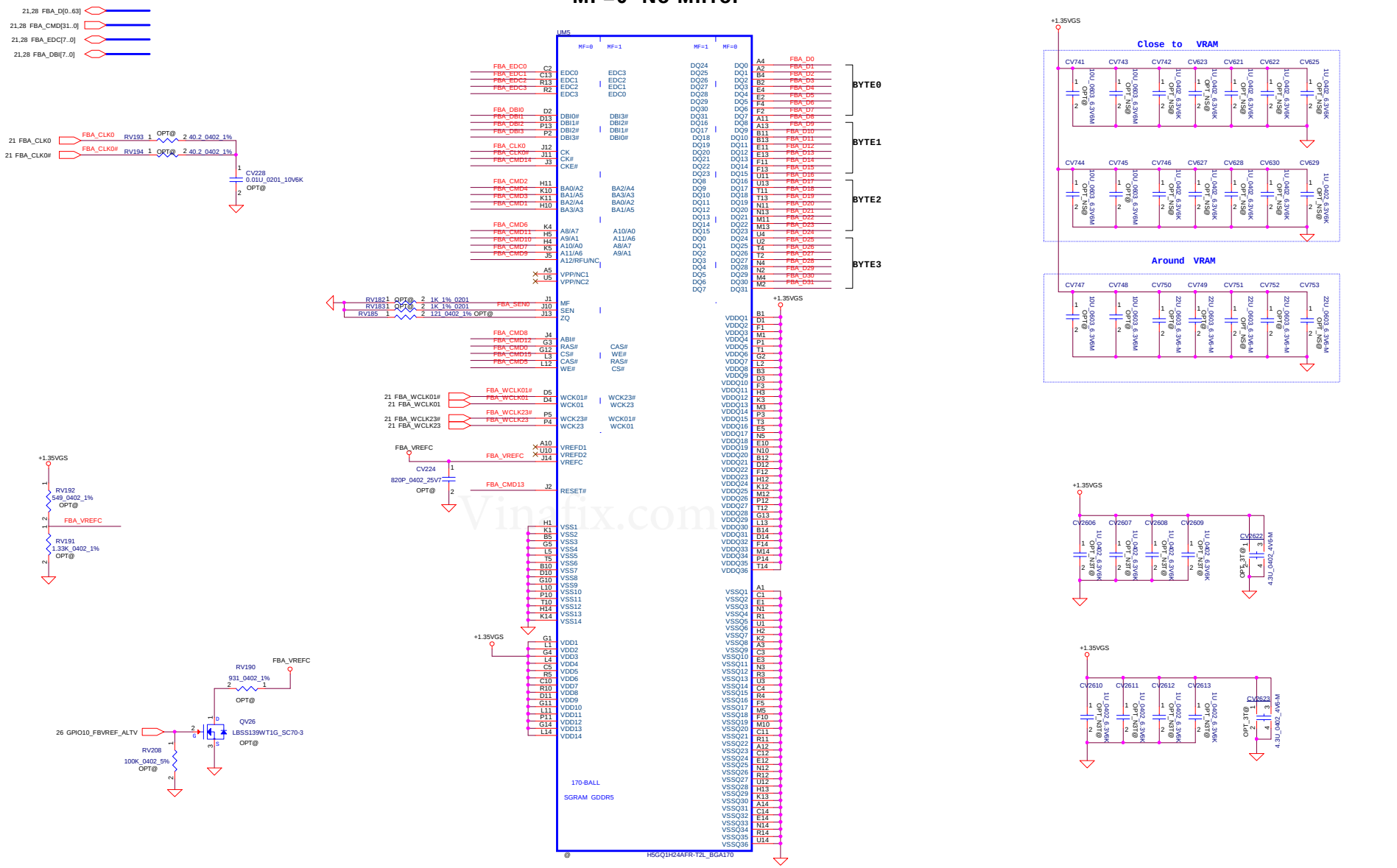
Title: GPU_GPIO/JTAG

Size	Document Number	Rev
C	FS441/FS540	0.1

Date: Friday, October 26, 2018 Sheet 26 of 61

Lower 32 bits

MF=0 No Mirror



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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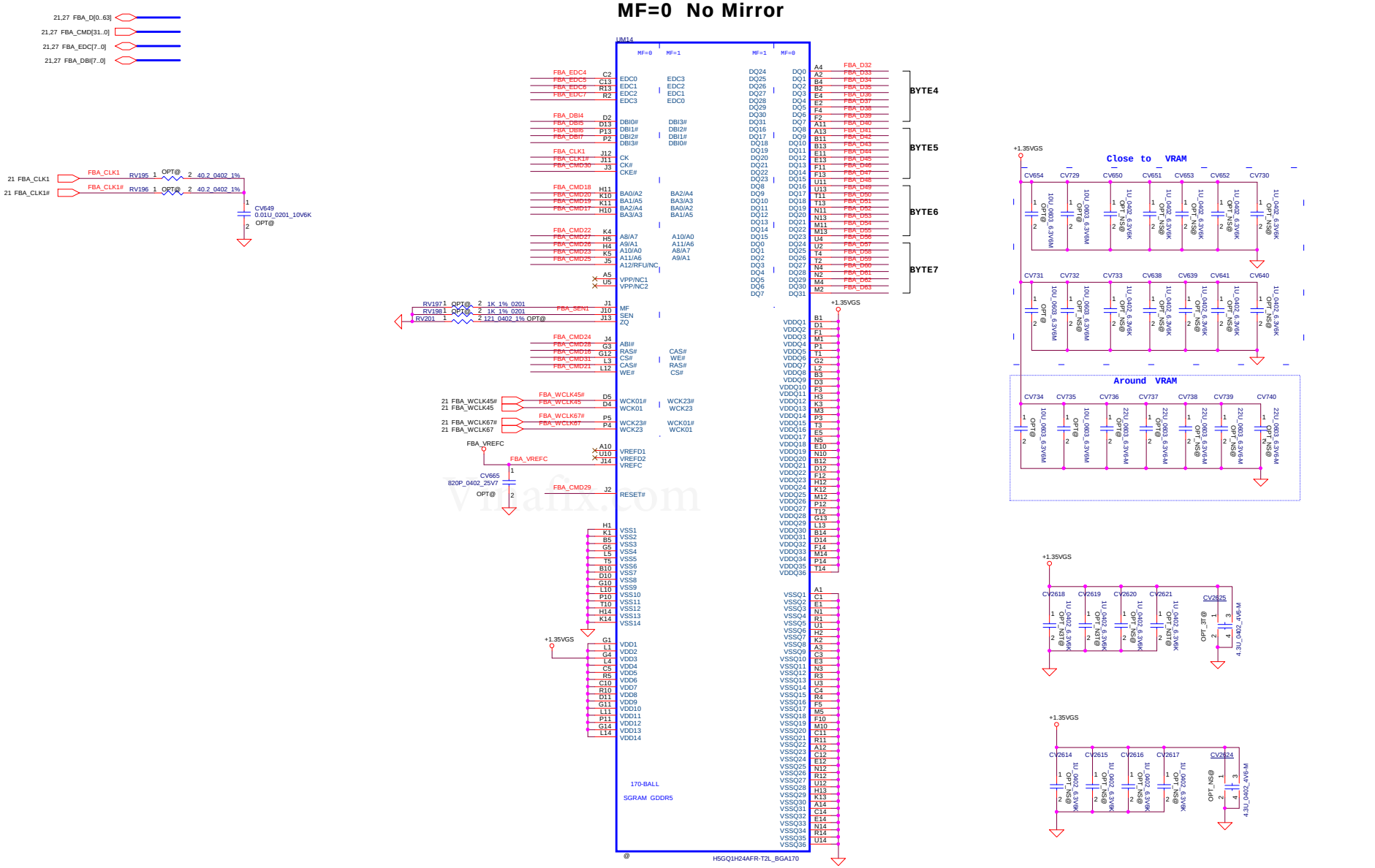
Title: GPU_GDDR5_Rank0_[31:0]

Size	Document Number	Rev
C	FS441/FS540	0.1

Date: Friday, October 26, 2018 Sheet 27 of 61

upper 32 bits

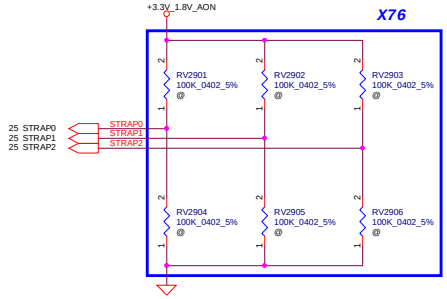
MF=0 No Mirror



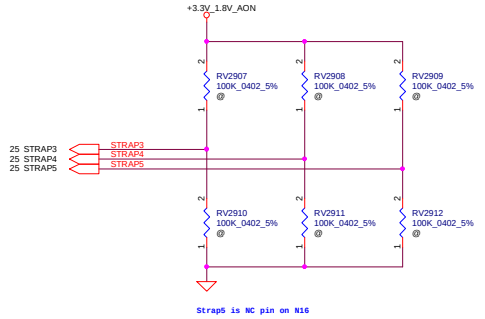
Title: GPU_GDDR5_Rank0_[64:32]

Size: C | Document Number: FS441/FS540 | Rev: 0.1

Date: Friday, October 26, 2018 | Sheet 28 of 61



GPU	FB Memory (GDDR5)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	K4G80325FB-HC28	0(0x0000)	L	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1(0x0001)	L	L	H
	Hynix 8Gb	H5GC8H24MJR-R0C	2(0x0010)	L	H	L



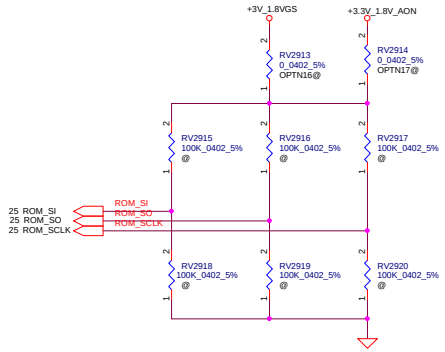
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE



	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N17S-G1	H	H	M	0000
N16S-GTR				

1:ENABLE 0:DISABLE

SOR0/1/2/3 DISABLE

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_MISC

Size	Document Number	Rev
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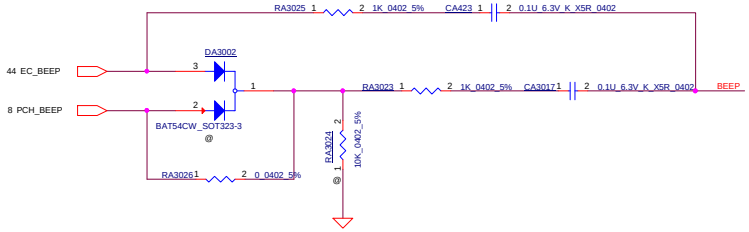

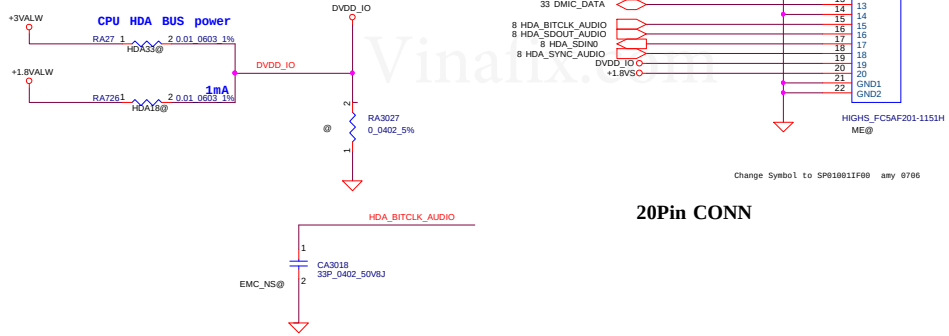

20Pin CONN

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: CODEC_RTS5199

Size	Document Number	Rev
C	FS441/FS540	0.1

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Title <Title>		
Size A	Document Number FS441/FS540	Rev 0.1
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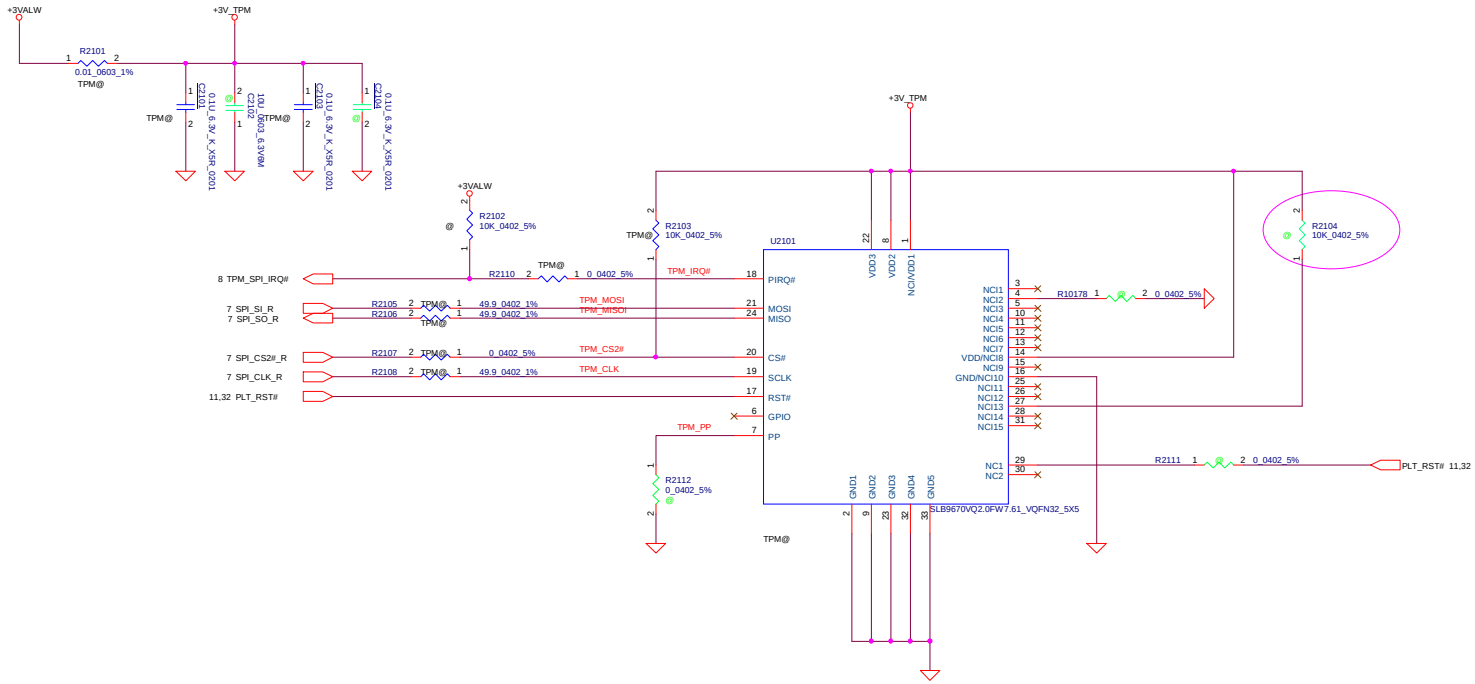

TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ2.0 FW 7.61	ST Micro ST33HTPH2E32AHB4	Nuvoton NPCT750LABYX	NATIONZ Z32H330TC
1	VDD	NC/VDD	NC	VSB	VDD
2	GND	GND	GND	NC	GND
3	GPIO	NC	NC	NC	NC
4	GPIO	NC	NC	PP/GPIO6	NC
5	NC	NC	NC	NC	NC
6	VNC/GPIO	GPIO	GPIO	GPIO3	NC
7	GPIO/VDD	PP	PP	NC	PP
8	VDD	VDD	NC	VHIO	VDD
9	GND	GND	NC	NC	GND
10	VNC	NC	NC	NC	NC
11	NC	NC	NC	NC	NC
12	NC	NC	NC	NC	NC
13	VNC/GPIO	NC	NC	GPIO4	NC
14	VDD	NC/VDD	NC	NC	VDD
15	NC	NC	NC	NC	NC
16	GND	NC/GND	NC	GND	GND
17	SPI_RST#	RST#	SPI_RST#	PLTRST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VDD	VPS	VHIO	VDD
23	GND	GND	NC	GND	GND
24	MISO	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC	NC
26	NC	NC	NC	NC	NC
27	NC	NC	NC	NC	NC
28	NC	NC	NC	NC	NC
29	VNC/GPIO	NC	NC	SDA/GPIO0	NC
30	VNC/GPIO	NC	NC	SCL/GPIO1	NC
31	VNC	NC	NC	NC	NC
32	GND	GND	NC	NC	GND

Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	TPM		
Size C	Document Number	FS441/FS540	Rev 0.1
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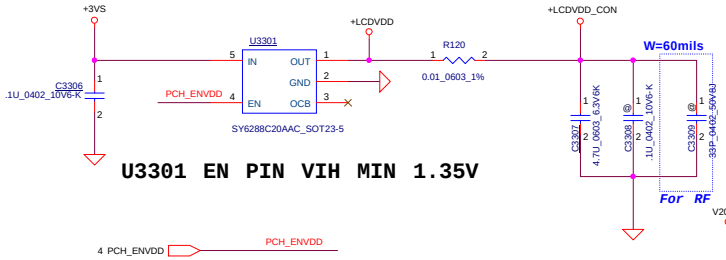
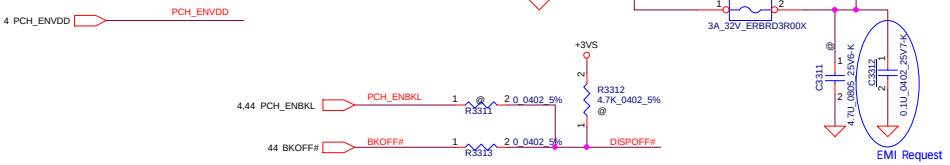
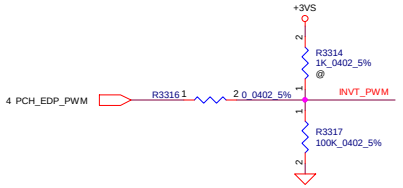
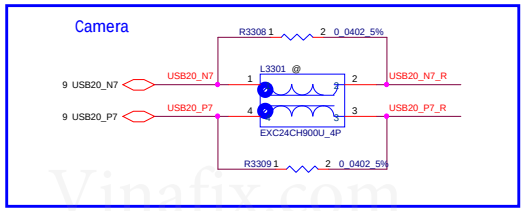
LCD POWER CIRCUIT

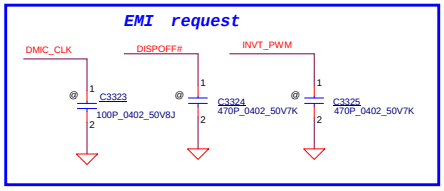


U3301 EN PIN VIH MIN 1.35V

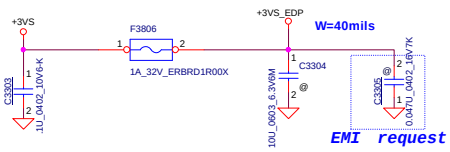


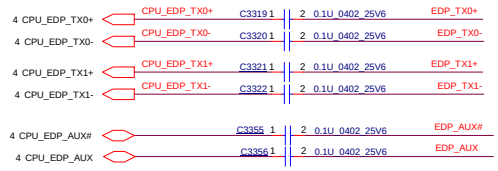


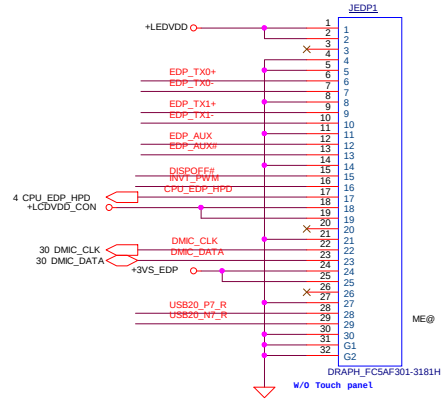




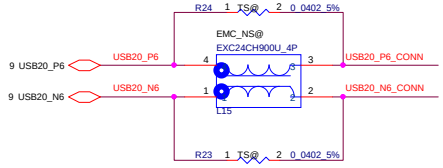
CMOS Camera

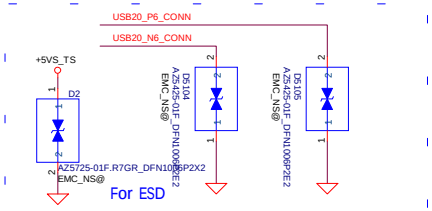


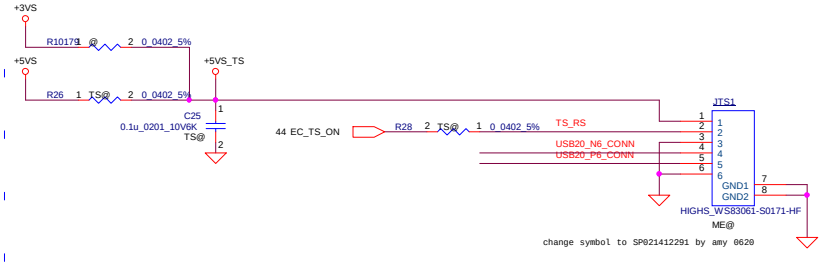




Touch Screen







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Title			
eDP/CAMERA.			
Size: Custom	Document Number: FS441/FS540		Rev: 0.1
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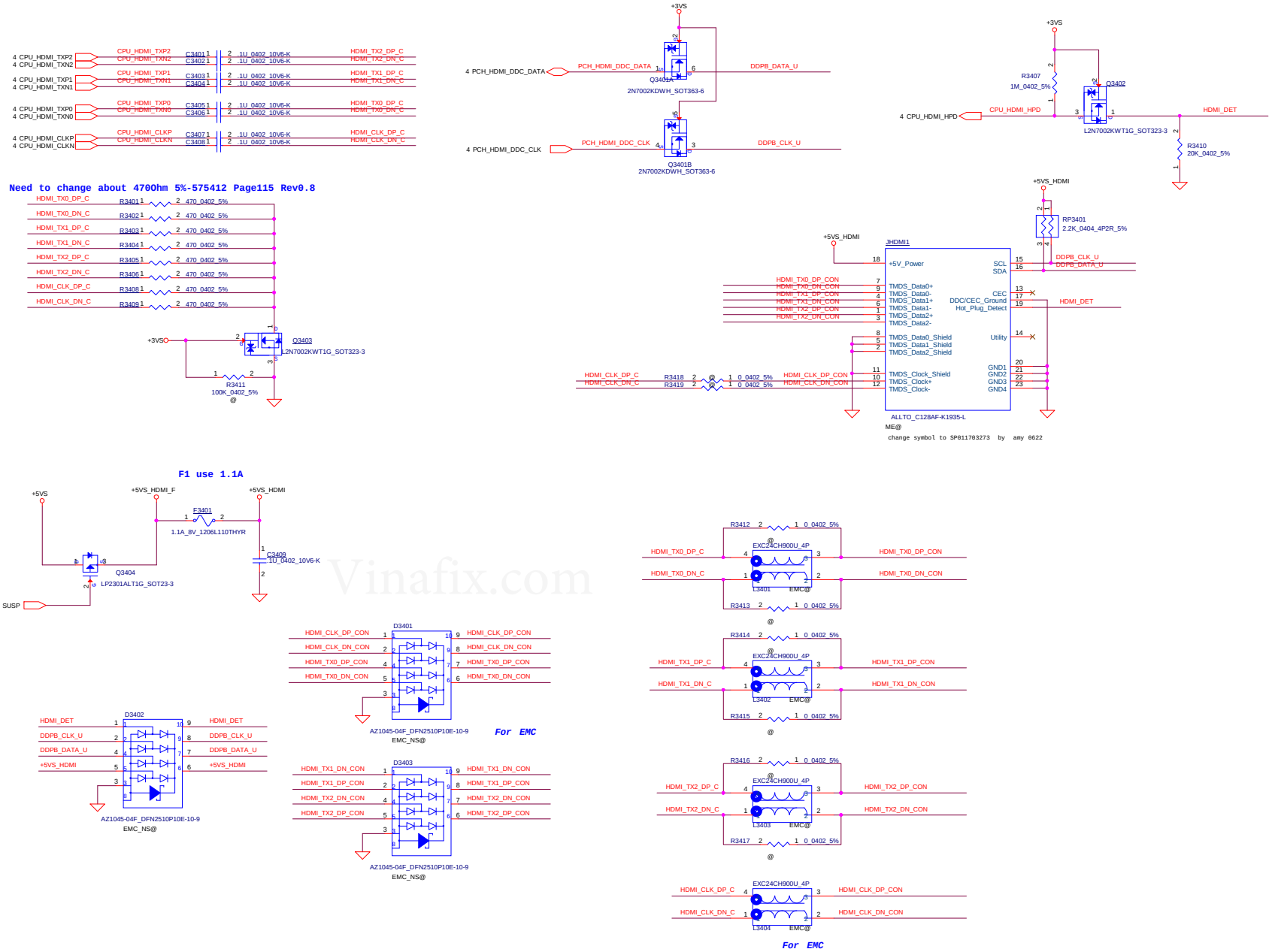

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Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title	HDMI_CONN		
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1.1.8VGS_PWR_EN_R pull high RV18----P26

2.ON/OFFBTN# add diode D25-----P36

3.del

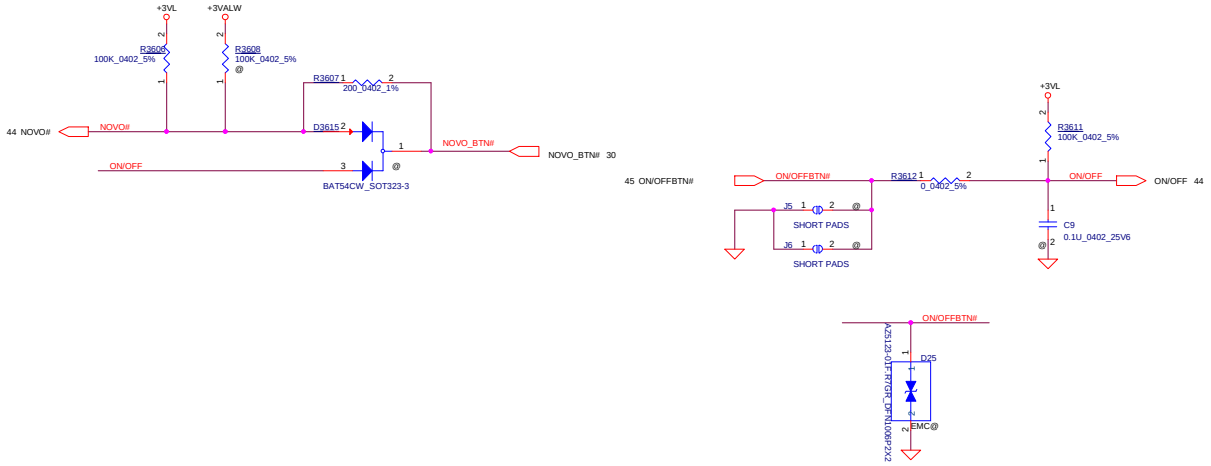
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title

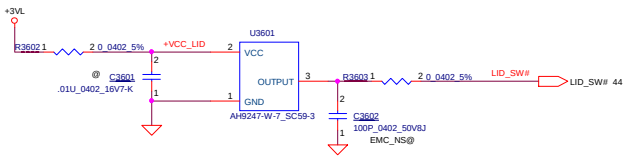
Blank

Size: B	Document Number: FS441/FS540	Rev: 0.1
Date: Friday, October 26, 2018	Sheet 35 of 61	

ON/OFF switch



LID switch



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **HALL Sensor**

Size	Document Number	Rev
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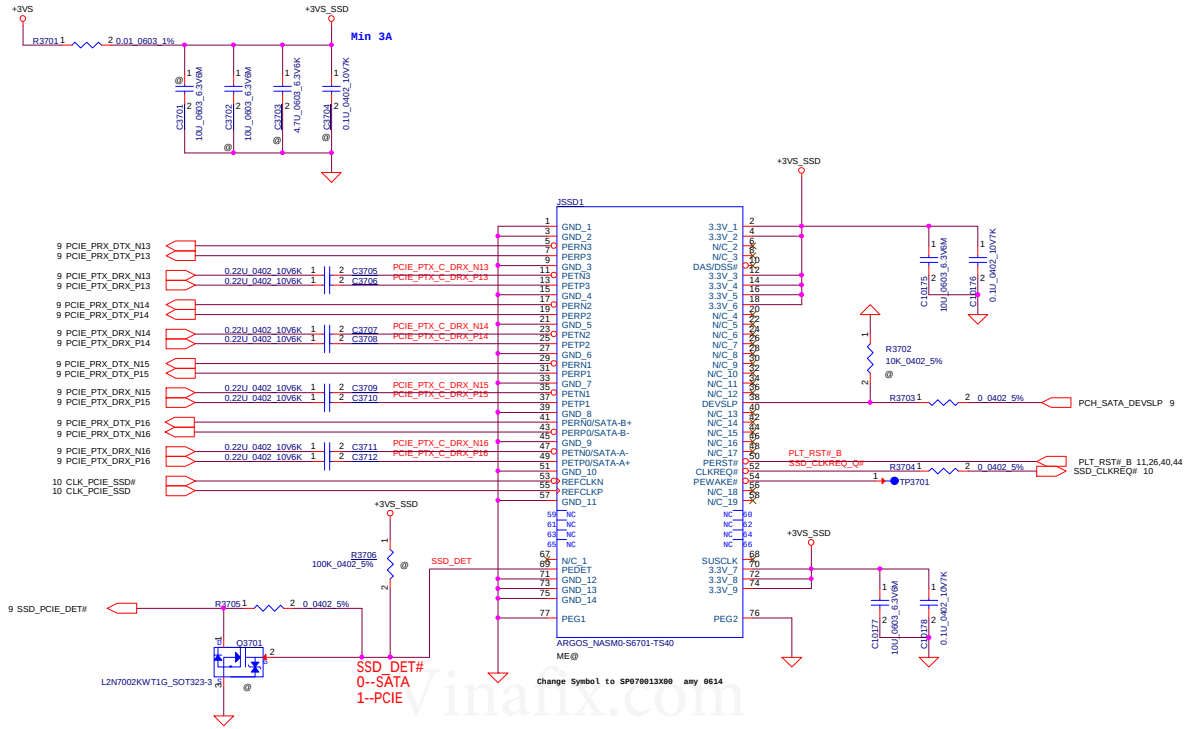

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	NGFF_SSD_1		
Size	Document Number		Rev
C	FS441/FS540		0.1
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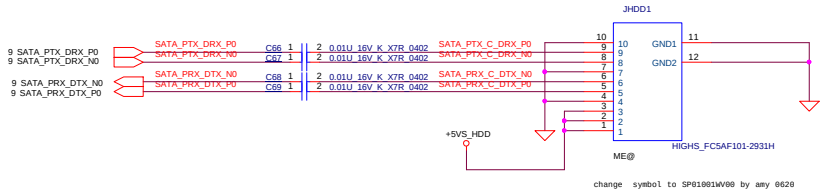

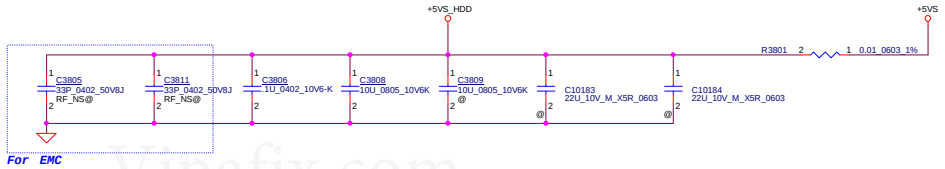

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **SATA HDD CONN**

Size	Document Number	Rev
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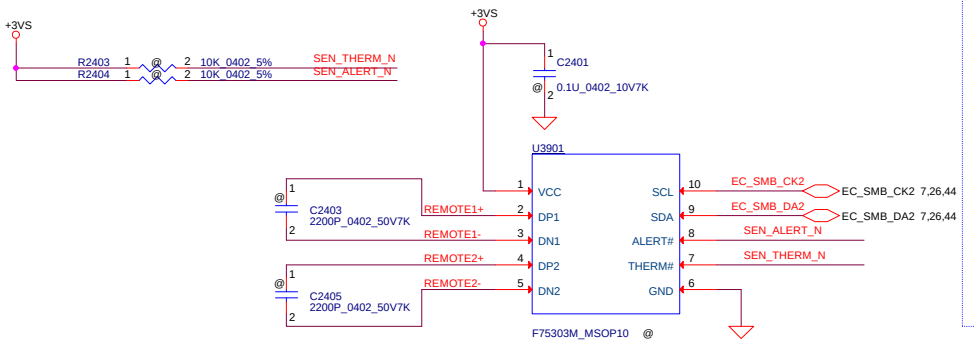
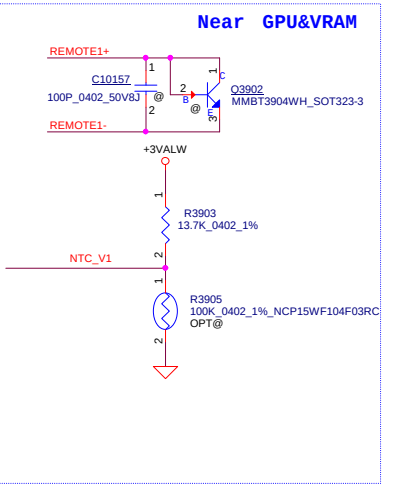
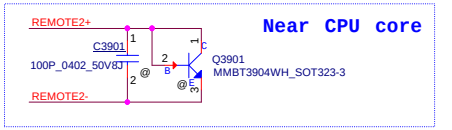
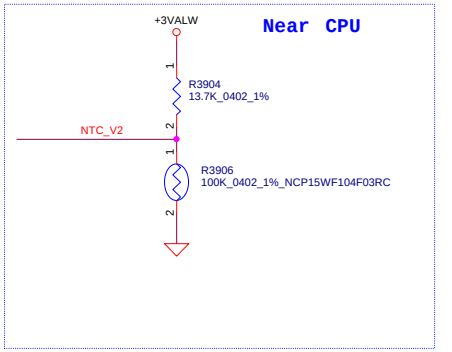
SMSC thermal sensor placed near DIMM

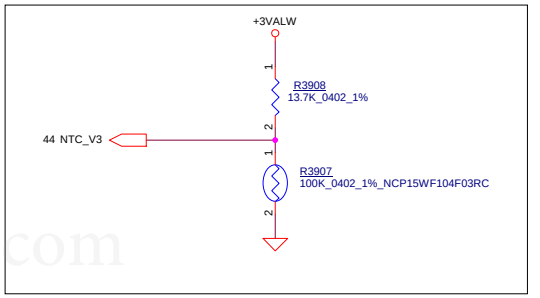
REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



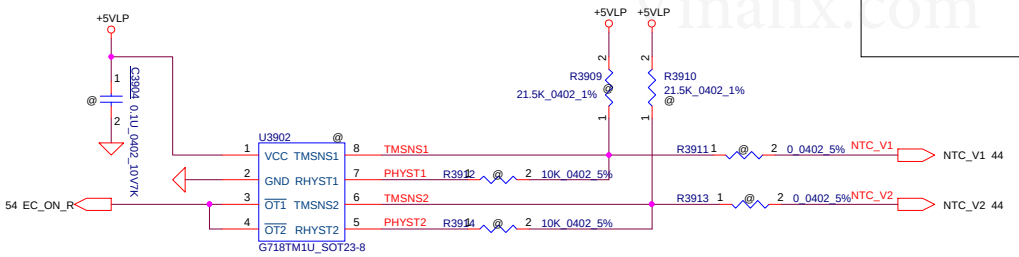




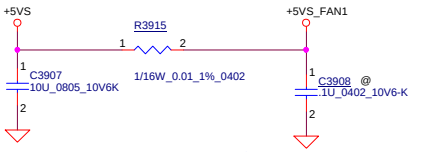




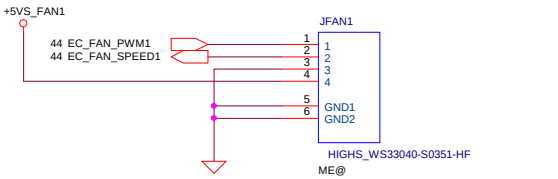
HW thermal sensor



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C



FAN Conn



Change Symbol to SP021410082 amy 0614

Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title: **Thermal sensor/FAN CONN**

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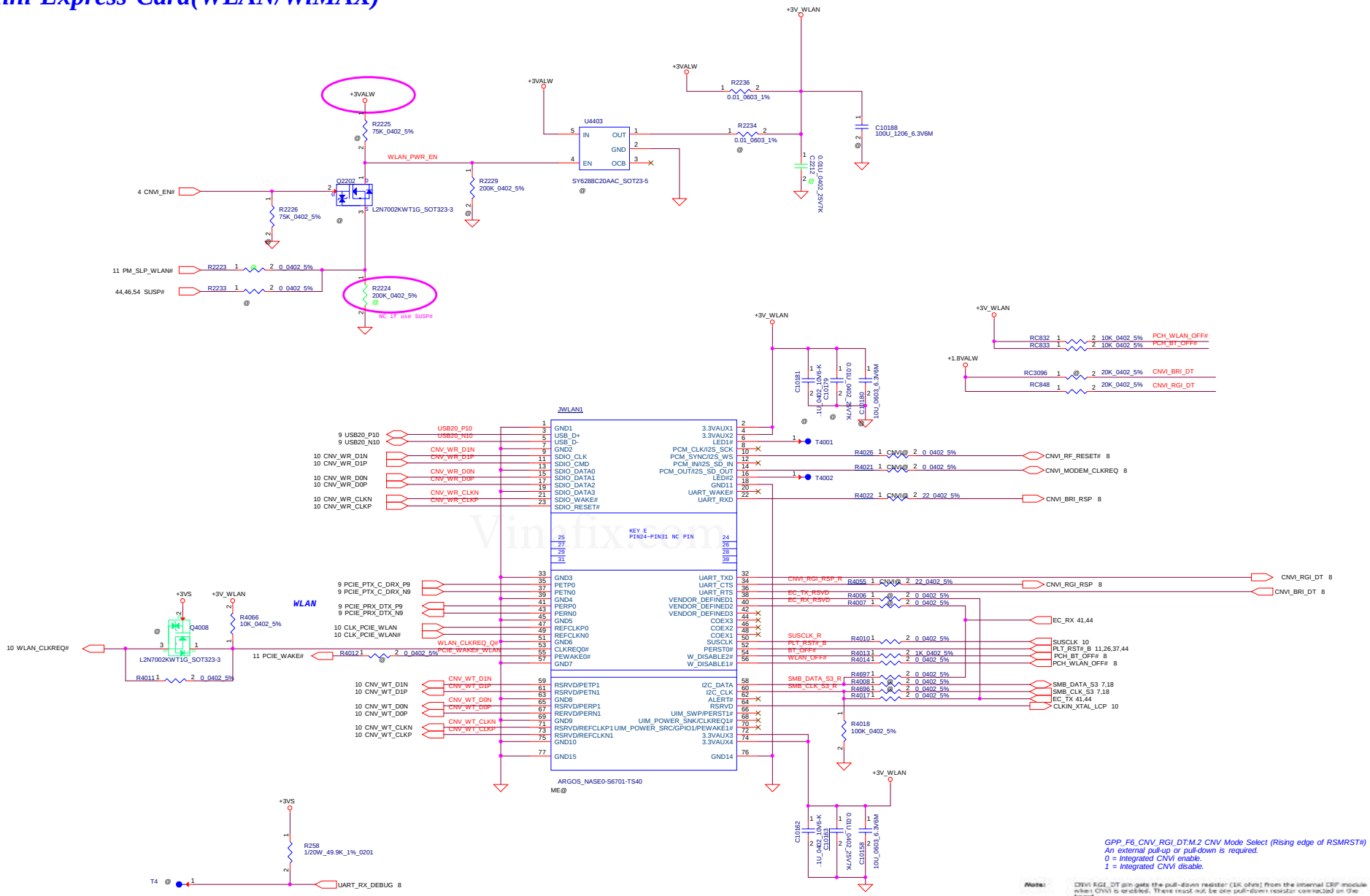
Mini-Express Card(WLAN/WiMAX)



GPP_F6_CNV_RGI_DT:M.2 CNV Mode Select (Rising edge of RSMRST#)
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

Note: CNVi RGI_DT pin gets the pull-down resistor (1K ohm) from the internal CRF module when CNVi is enabled. There must not be one pull-down resistor connected on the board.

Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

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Title: **NGFF_WLAN**

Size	Document Number	Rev
C	FS441/FS540	0.1

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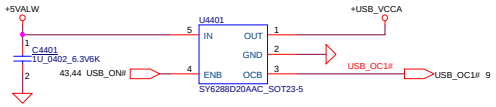
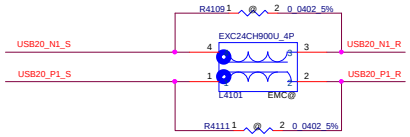
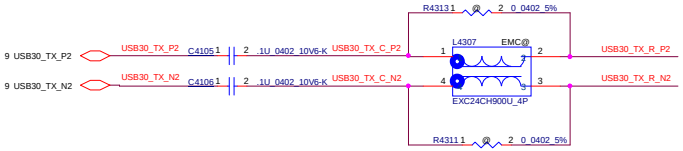
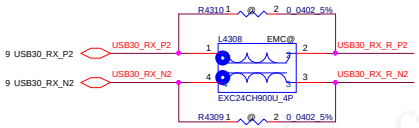
RIGHT SIDE USB3.0 PORT x1

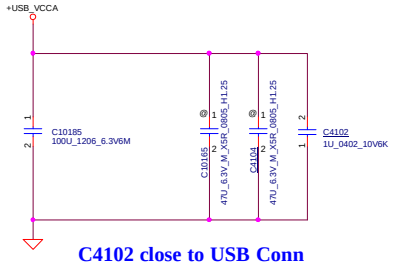


Low Active 2A

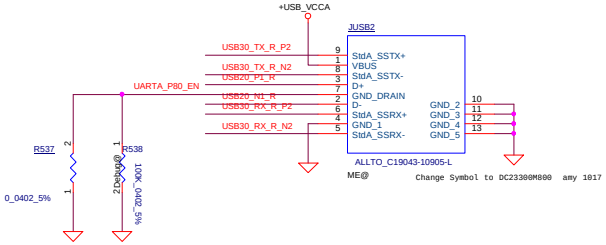


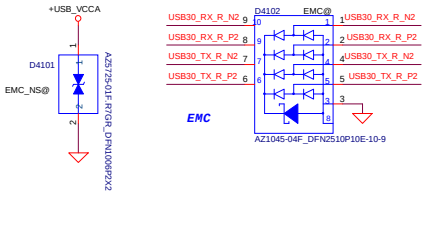




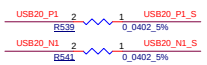


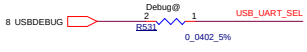
C4102 close to USB Conn

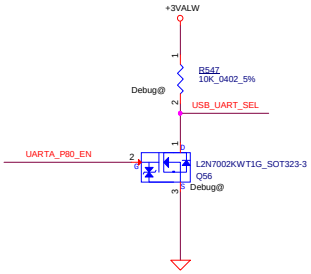




For USB Debug Function



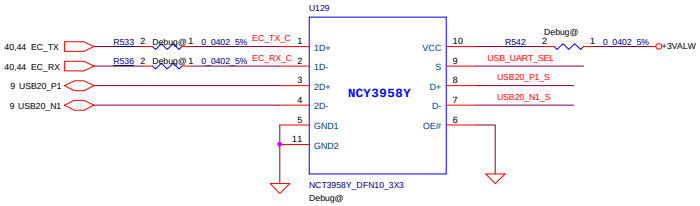




USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

UARTA_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)



07/06 add USB debug function Amy

Security Classification	LC Future Center Secret Data		
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Title: USB3 PORT_LEFT

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Title

Blank

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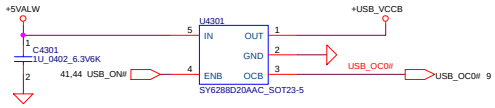
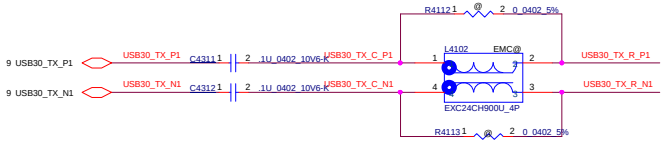
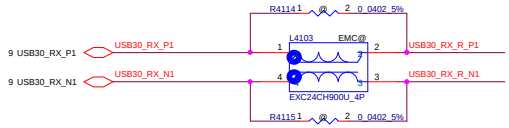
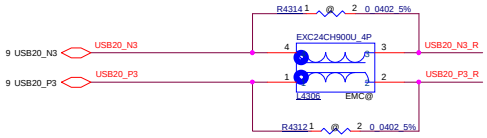
Right SIDE USB3.0 PORT

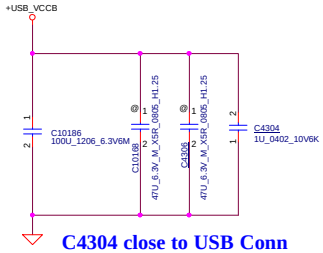


Low Active 2A



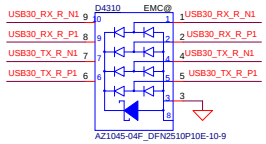




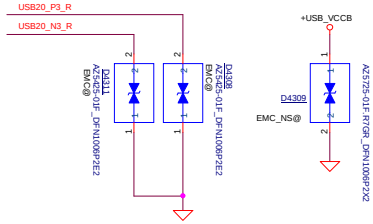


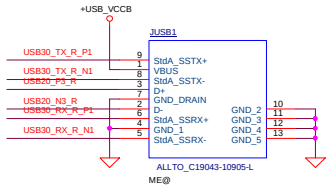
C4304 close to USB Conn

04/02 add USB debug function bron



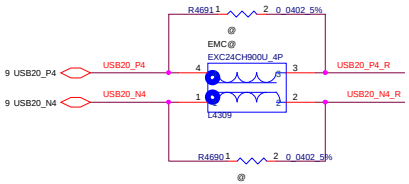
EMC

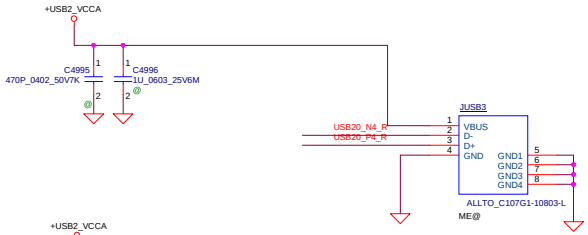




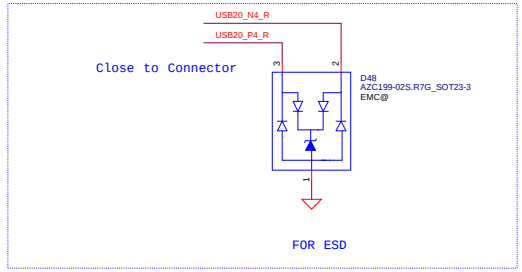
Change Symbol to SP011703284 amy 0614

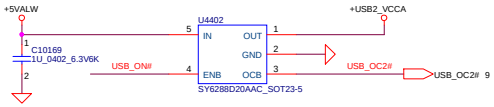
USB2.0 PORT x1



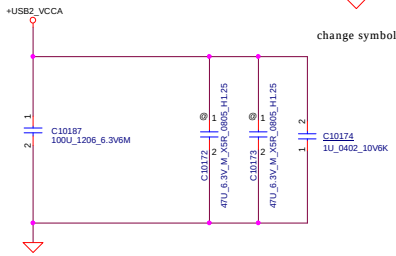


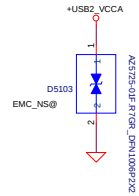
change symbol to SP011807041 amy 0710





Low Active 2A





Security Classification	LC Future Center Secret Data		
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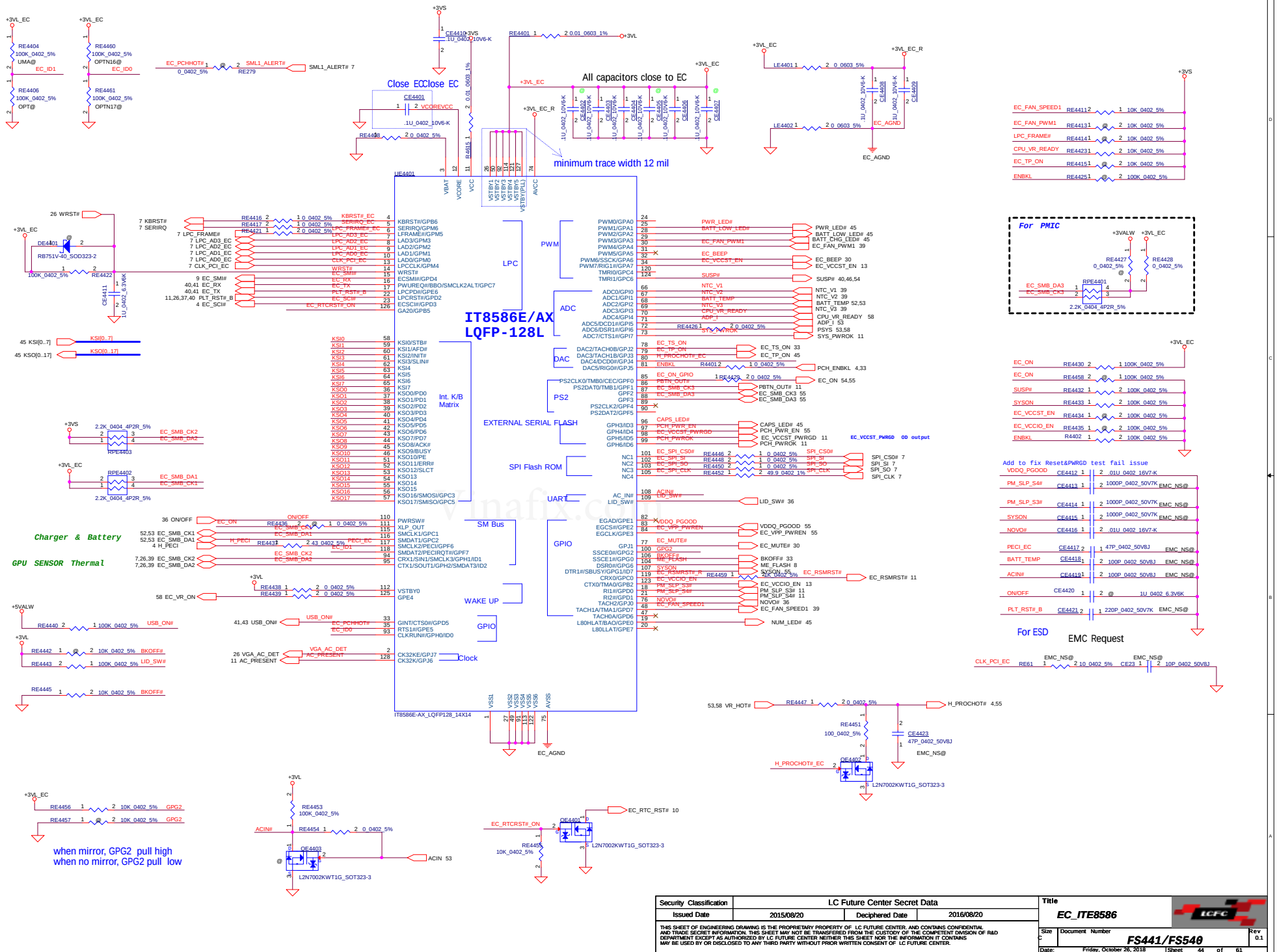
IT8586E/AX
LQFP-128L
LPC
PWM
ADC
DAC
PS2
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
GPIO
WAKE UP
SM Bus
Int. K/B Matrix
Clock
Close ECClose EC
All capacitors close to EC
minimum trace width 12 mil
For PMIC
Add to fix Reset&PWRGD test fail issue
For ESD
EMC Request
Charger & Battery
GPU SENSOR Thermal
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
EC_AGND
L2N7002KWT1G_SOT323-3
Security Classification
LC Future Center Secret Data
Issued Date
2015/08/20
Deciphered Date
2016/08/20
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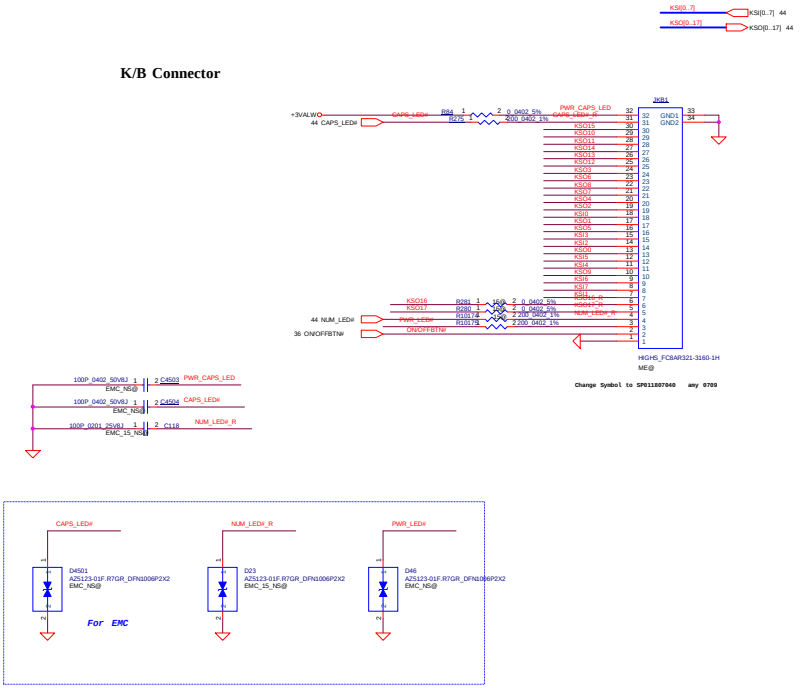
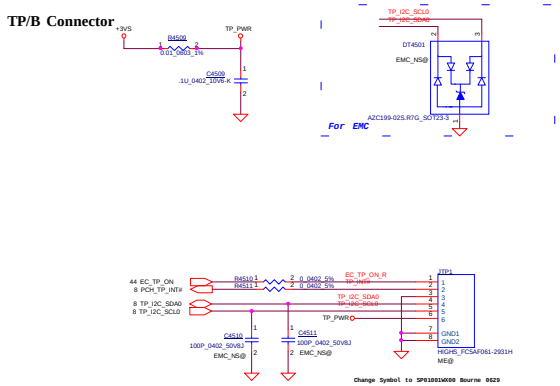
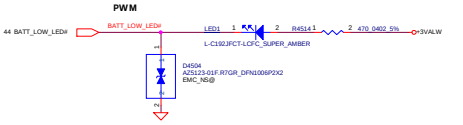
K/B Connector



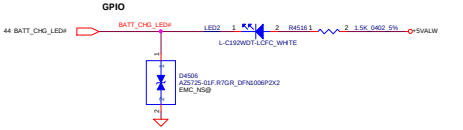
TP/B Connector

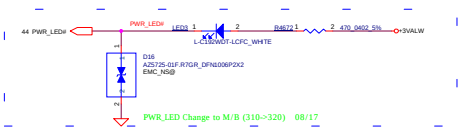


PWM



GPIO





LED	Stute	LED Behavior
Power Button	System on	White_on(battery≥21%-100%)
		Amber_on(battery≥5%-20%)
	Standby LID closed	White_on(battery≥21%-100%)
		Amber_Blink_3S(battery≥5%-20%)
	System off	OFF
Charging	Battery only	OFF
	Charging	Amber_on(battery≥1%-90%)
		White_on(battery≥91%-100%)

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Title	KB/TP_CONN.		
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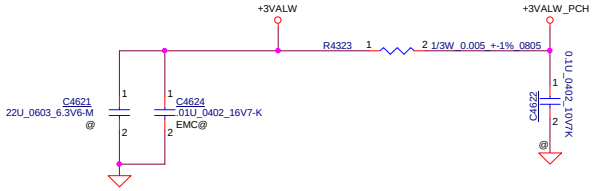
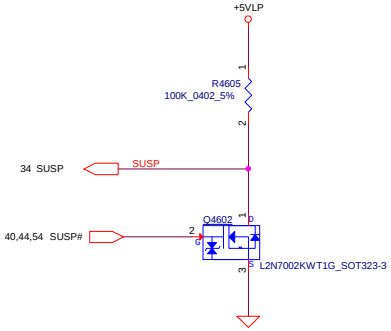
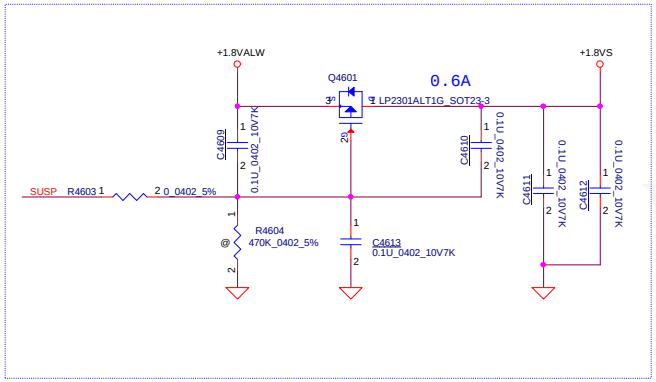
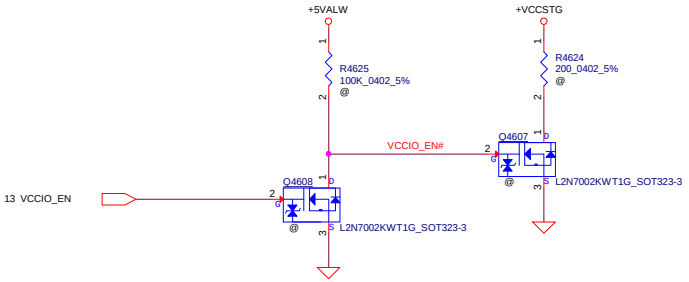
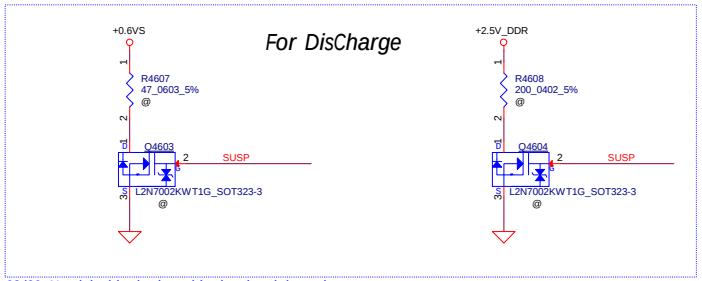






Reserve for VCCSGT discharge





08/29: Need double check enable signal and the resistance

12.1.4 VccSTG Rail Discharge Requirements

As long as VccST and VccSTG are power gated separately, the following requirements are critical to prevent system failure on Whiskey Lake:

1. VccSTG should have a discharge circuit, either integrated into its load switch or externally on the motherboard. The recommended nominal $R_{discharge}$ <= 300Ω to GND. The discharge circuit should be activated when the VccSTG load switch is disabled.
2. If VccST/VccPLL has a discharge circuit, either integrated into its load switch or externally on the motherboard, then VccSTG nominal $R_{discharge}$ <= VccST/VccPLL $R_{discharge}$.
3. The total capacitance on VccSTG <= total capacitance on VccST/VccPLL.

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Title: **DC V TO VS INTERFACE**

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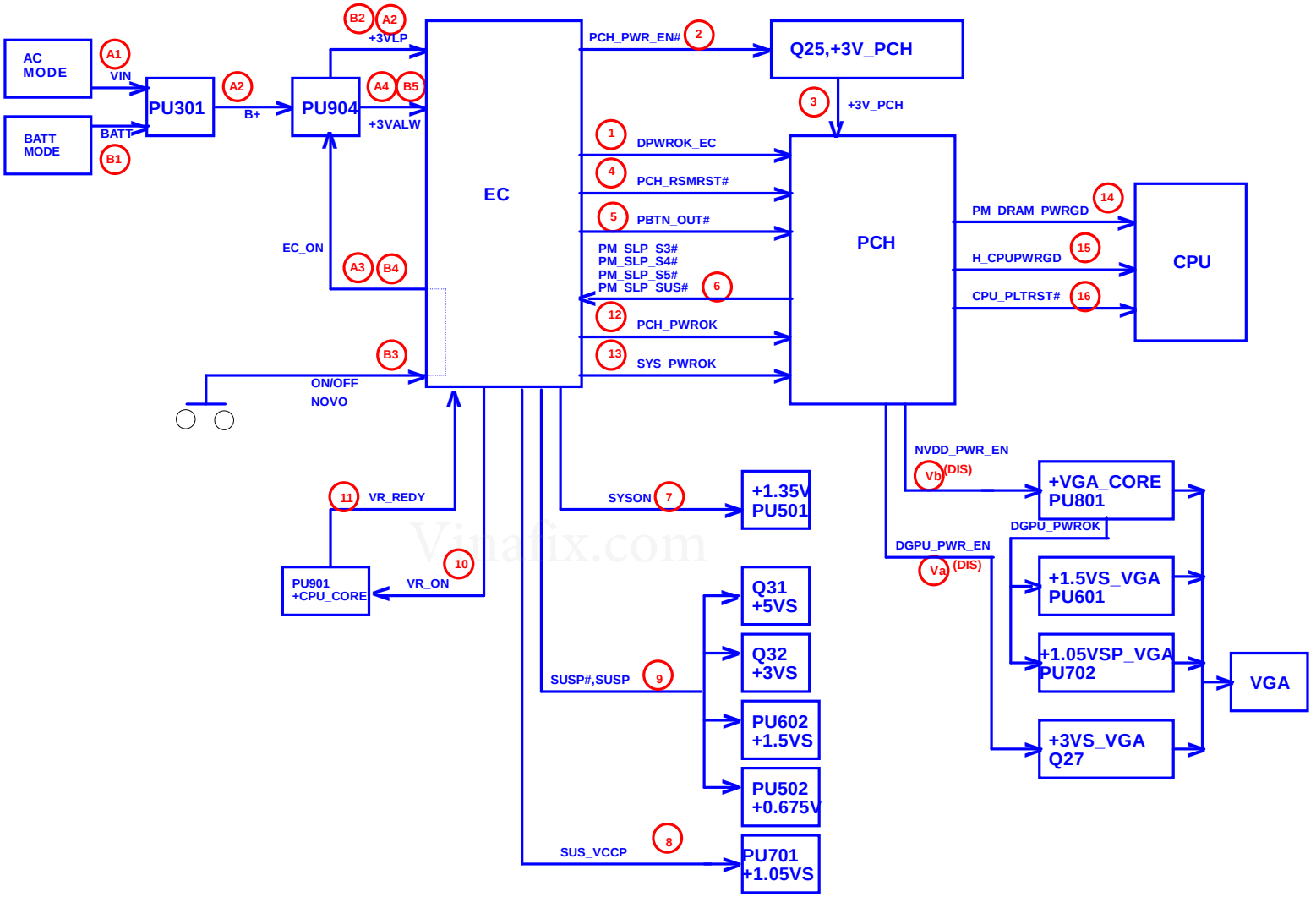

Security Classification	LC Future Center Secret Data		
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Title: **Power sequence block**

Size	Document Number	Rev
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CPU

UC1 8565U@
Intel i7-8565U 1.8G/4C/8M
SA00009GY00

UC1 8265U@
Intel i5-8265U 1.6G/4C/6M
SA00009GZ00

UC1 8145U@
Intel i3-8145U 2.1G/2C/4M
SA00009H000

UC1 5405U@
Intel Pentium-5405U 2.3G/2C/2M
SA00009T100

UC1 4205U@
Intel Celeron-4205U 1.8G/2C/2M
SA00009T200

GPU

UV1 OPTN16@
N16V-GMR1 GPU
SA00007QX00

RV2316 OPTN17@
5.11_0805_1%
SD00001NQ00

RV2316 OPTN16@
470_0805_5%
SD00247008J

PCB_MB

ZZZ1 FS540@
NM-C121
DA600014P00

ZZZ6 SAM_VR_N16@
V2G SAM N16
X7646612001
VRAM_Samsung

ZZZ5 Hyn_VR_N16@
HYNIX V2G N16S
X7646612002
VRAM_Hynix

ZZZ4 Mic_VR_N16@
V2G MIC N16
X7646512001
VRAM_Micron

ZZZ9 SAM_DRAM@
D4G SAM
X7646512004
DRAM_Samsung

ZZZ8 Hyn_DRAM@
HYNIX D4G
X7646512003
DRAM_Hynix

ZZZ7 Mic_DRAM@
D4G MIC
X7646512002
DRAM_Micron

SO_DIMM only

RC805 NMD@
SO_DIMM
SD02810028J

RC812 NMD@
SO_DIMM
SD02810028J

RC814 NMD@
SO_DIMM
SD02810028J

Security Classification	LC Future Center Secret Data		
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Title: *Virtual symbol*

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Hole

H2
HOLEA
PAD_C10P0D8P0

PCB Fedical Mark PAD

FD4901 FD4902 FD4903 FD4904 FD4905 FD4906

MD Shielding

SH1 SPRING_FINGER_6.2X1.64
SH2 SPRING_FINGER_6.2X1.64
SH3 SPRING_FINGER_6.2X1.64
SH4 SPRING_FINGER_6.2X1.64
SH5 SPRING_FINGER_6.2X1.64
SH6 SPRING_FINGER_6.2X1.64

H3 HOLEA PAD_CT7P0B6P0D3P2
H4 HOLEA PAD_CT7P0B6P0D3P2
H5 HOLEA PAD_CT7P0B6P0D3P2
H6 HOLEA PAD_CT7P0B6P0D3P2
H7 HOLEA PAD_CT7P0B6P0D3P2
H8 HOLEA PAD_CT7P0B6P0D3P2

H9 HOLEA PAD_C7P0D4P0
H10 HOLEA PAD_C7P0D4P0

H17 HOLEA PAD_O2P5X3P0D2P5X3P0N
H18 HOLEA PAD_O2P5X3P0D2P5X3P0N

H11 HOLEA PAD_C7P0D2P8
H12 HOLEA PAD_C7P0D2P8
H13 HOLEA PAD_C7P0D2P8

H19 HOLEA PAD_C2P5D2P5N

H14 HOLEA PAD_C7P0D2P4

H15 HOLEA PAD_CT7P0B10P0D4P0
H16 HOLEA PAD_CT7P0B10P0D4P0

SODIMM Shielding

SH10 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH11 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH12 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH13 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH14 SHIELDING_SUL-35A2M_9P2X3P3_1P

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	Hole	
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B	FS441/FS540	0.1
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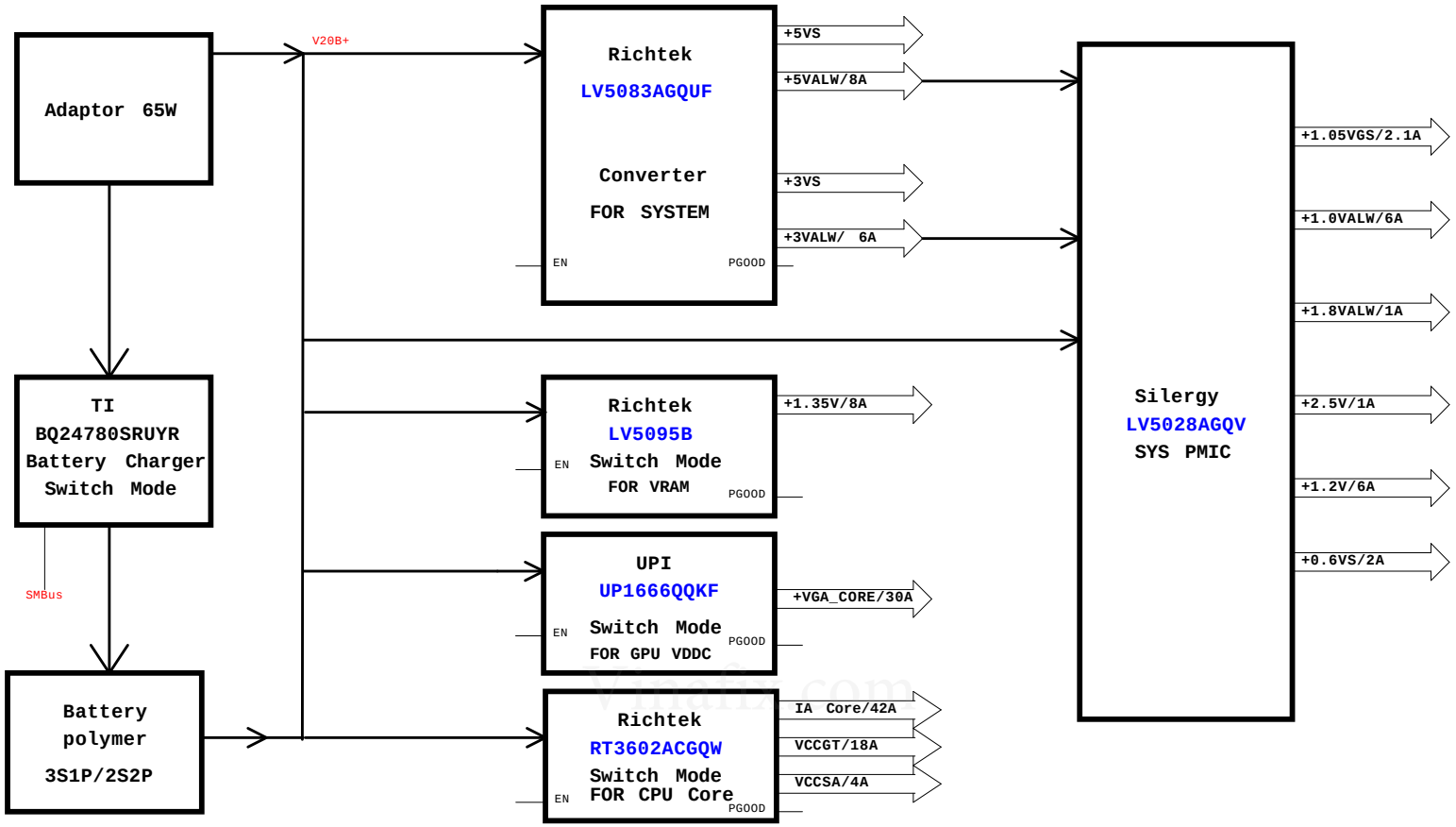
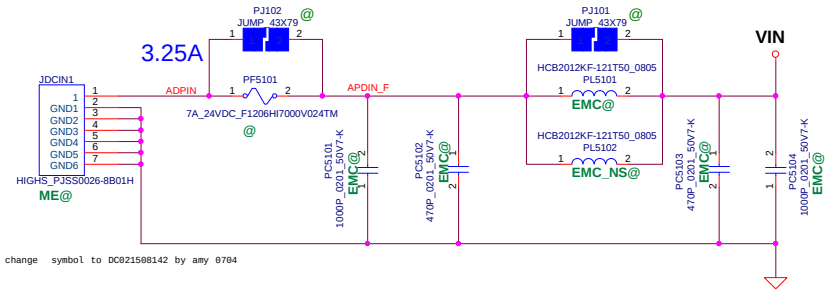


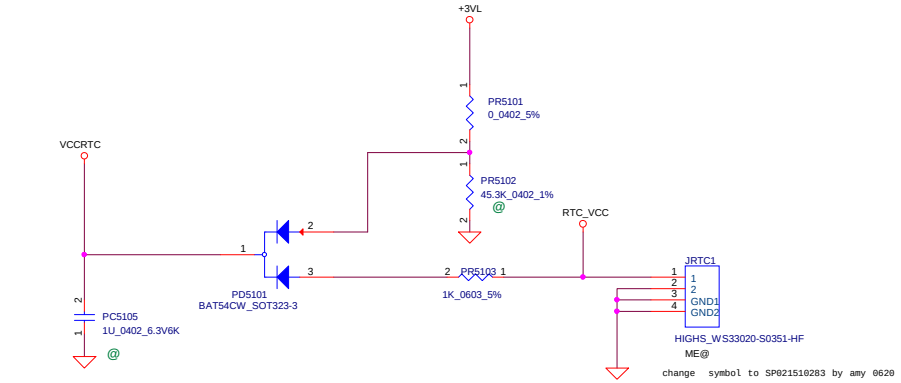
Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-Power Diagram

Size	Document Number	Rev
C	140S-WHL	0.3

Date: Friday, October 26, 2018 Sheet 50 of 61





RTC_VCC 20MIL
+3VL 20MIL
VCCRTC 20MIL

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-DCIN / RTC charger

Size	Document Number	Rev
Custom	140S-WHL	0.3

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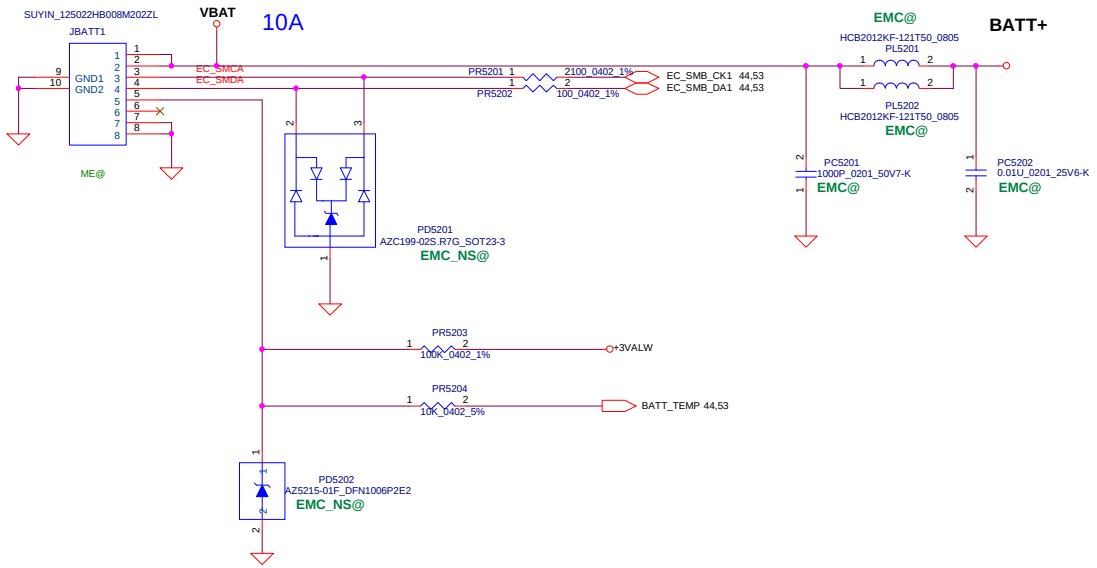


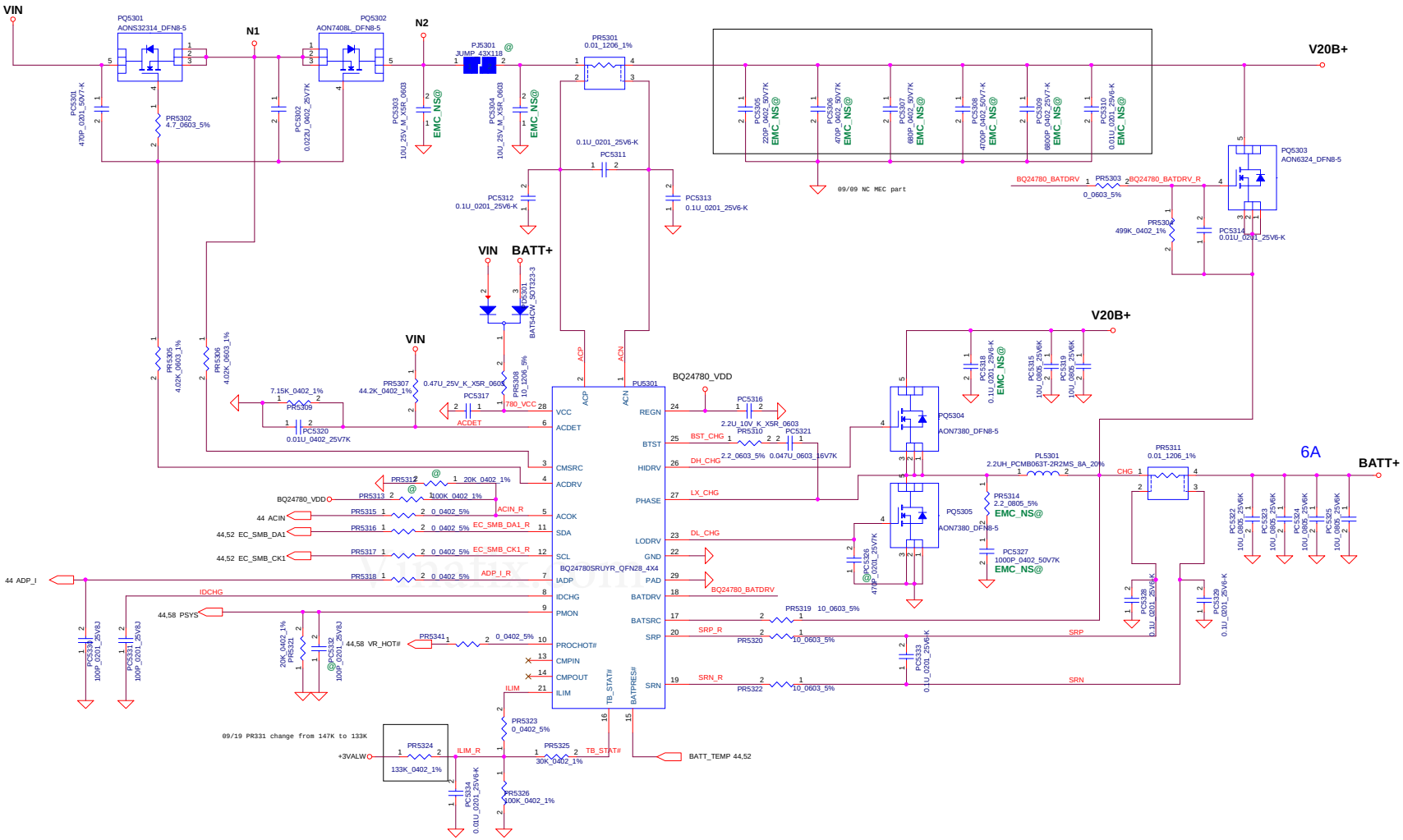
2S1P polymer battery voltage level: +5.5V ~ 8.8 V

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-BATTERY CONN/OTP

Size	Document Number	Rev
Custom	140S-WHL	0.3

Date: Friday, October 26, 2018 Sheet 52 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-CHARGER

Size	Document Number	Rev
C	140S-WHL	0.3
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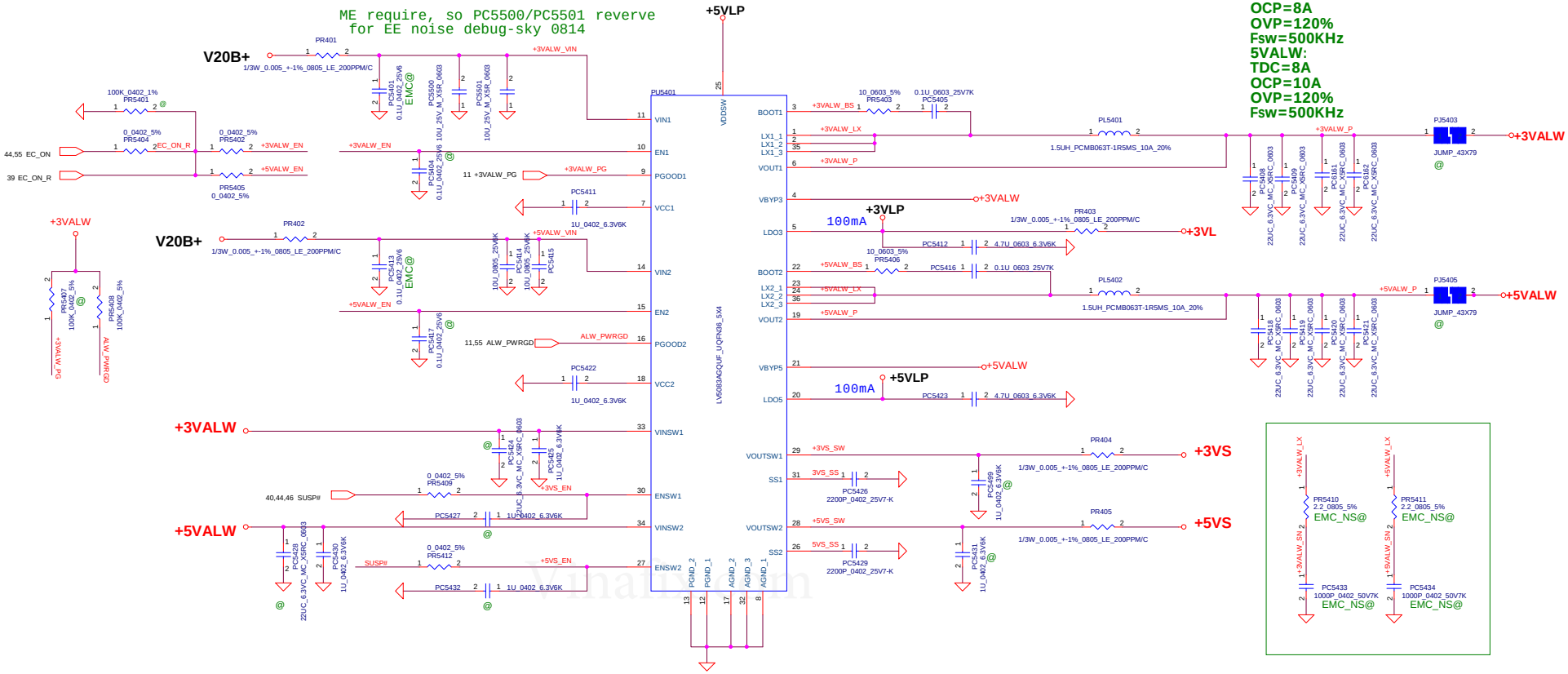
EC_ON pull high reserve at EC,
no need USM enable=1.57V USM

ME require, so PC5500/PC5501 reverve
for EE noise debug-sky 0814

3VALW:
TDC=6A
OCP=8A
OVP=120%
Fsw=500KHz
5VALW:
TDC=8A
OCP=10A
OVP=120%
Fsw=500KHz

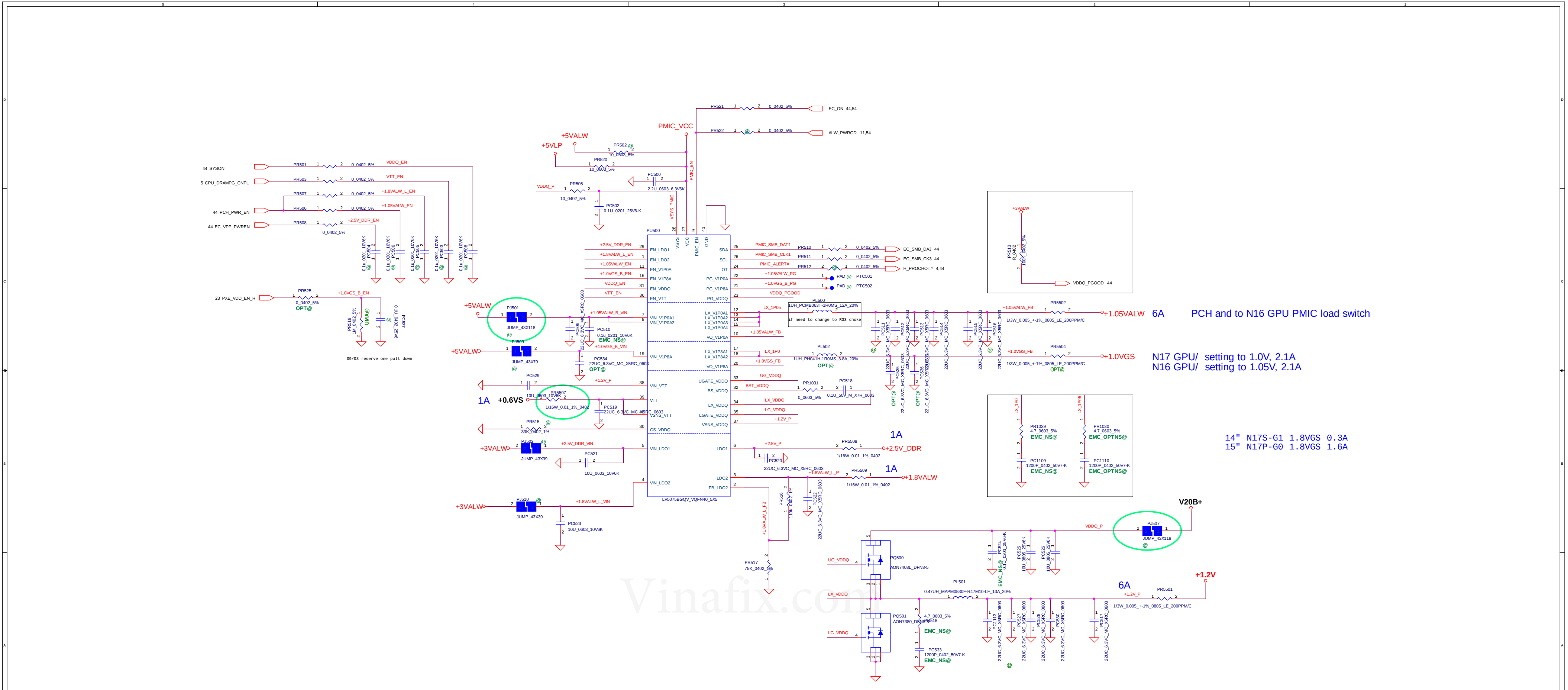


Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR_3VALW/5VALW

Size: C | Document Number: 140S-WHL | Rev: 0.2

Date: Friday, October 26, 2018 | Sheet 54 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

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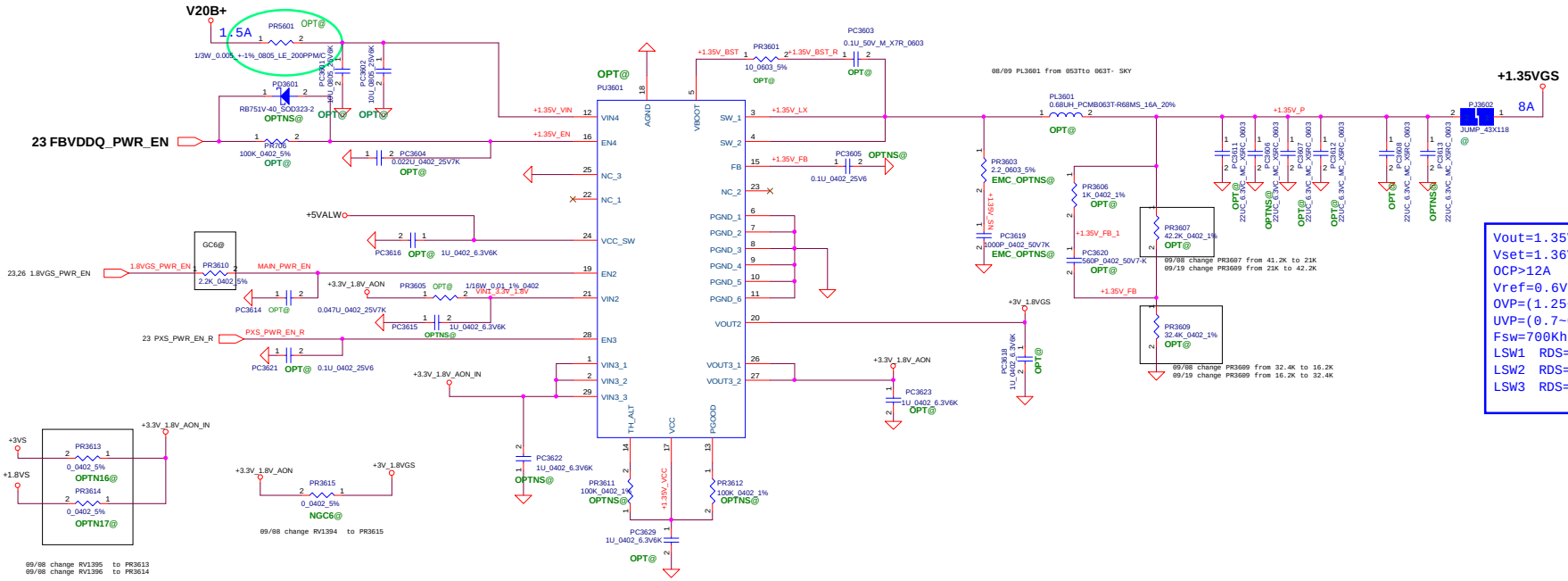
Title: PWR PMIC-DDR4/1.0ALW/1.8ALW

Size: Custom | Document Number: 140S-WHL | Rev: 0.3

Date: Friday, October 26, 2018 | Sheet 55 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

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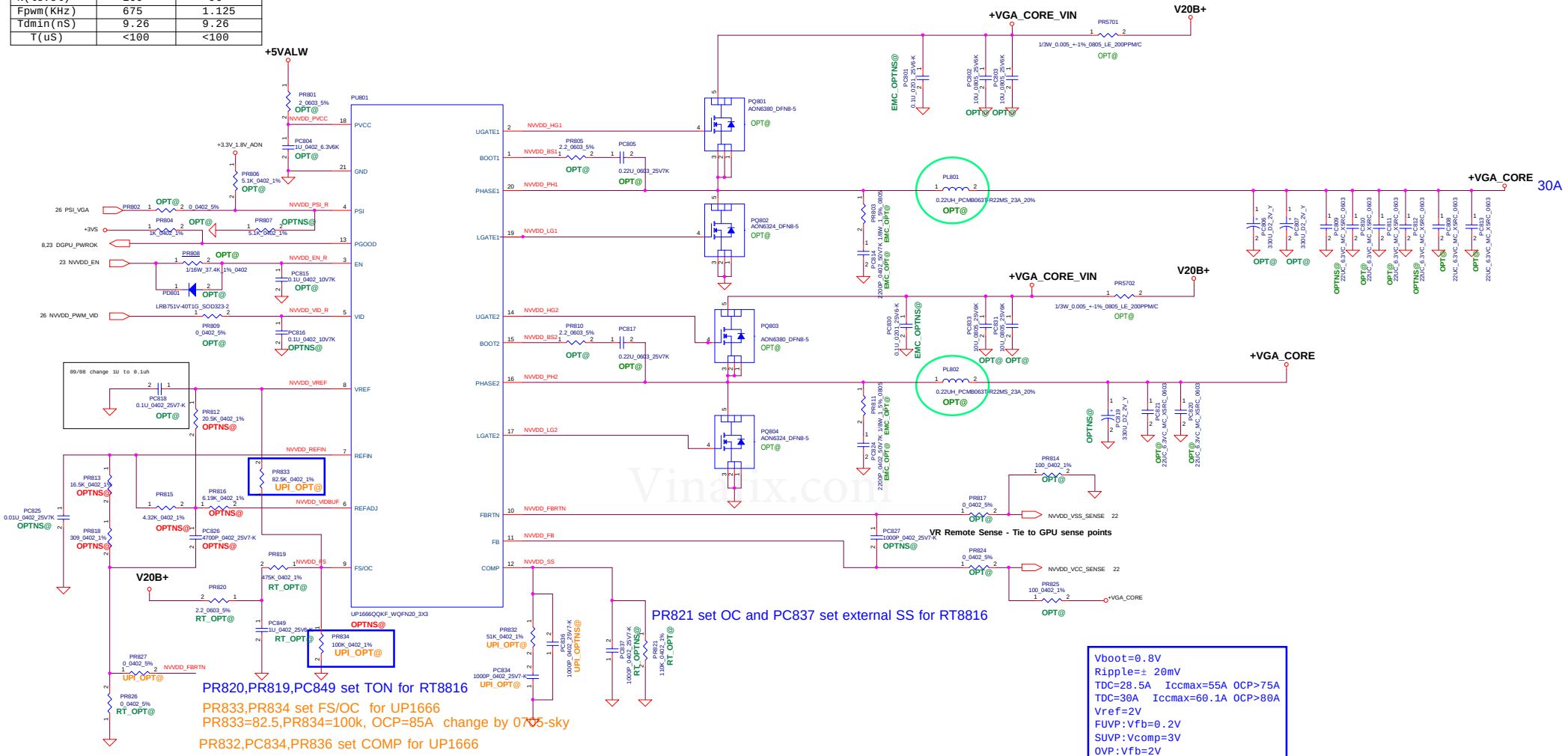
Title	PWR-VGA-PMIC		
Size	Document Number		Rev
Custom	149S-WHL		0.3
Date:	Friday, October 26, 2018	Sheet 56 of 61	

PWM-VID Specification		
	N17 Config	N16 Config B
Vmin(V)	0.3	0.6
Vmax(V)	1.3	1.2
Vboot(V)	0.8	0.9
Vstep(mV)	6.25	6.25
N(level)	160	96
Fpwm(KHz)	675	1.125
Tdmin(nS)	9.26	9.26
T(uS)	<100	<100

RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM



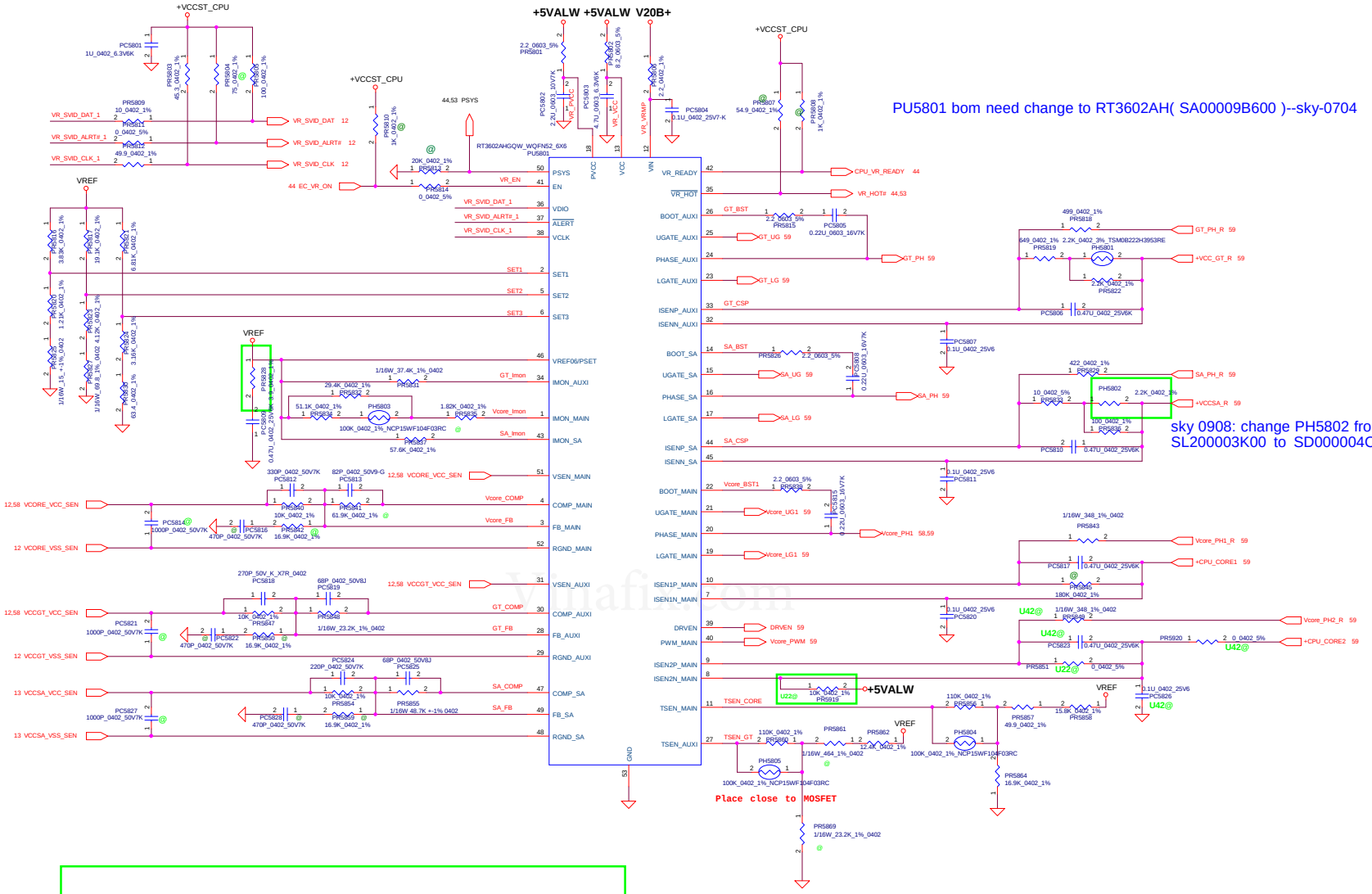
PR816,PR812,PR815,PR813,PR818,PC826 BOM structure control for N16 or N17

Component	Value	N17	N16
R1(KΩ)	PR816	6.19	20
R2(KΩ)	PR812	20.5	20
R3(KΩ)	PR815	4.32	2
R4(KΩ)	PR813	16.5	18
R5(KΩ)	PR818	0.309	0
C(nF)	PC826	4.7	2.7

UPI_OPT@ : for UP1666
RT_OPT@ : for RT8816A

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-VGA_CORE
Size: Custom | Document Number: 140S-WHL | Rev: 0.3
Date: Friday, October 26, 2018 | Sheet 57 of 60



Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Decipered Date	2018/07/10

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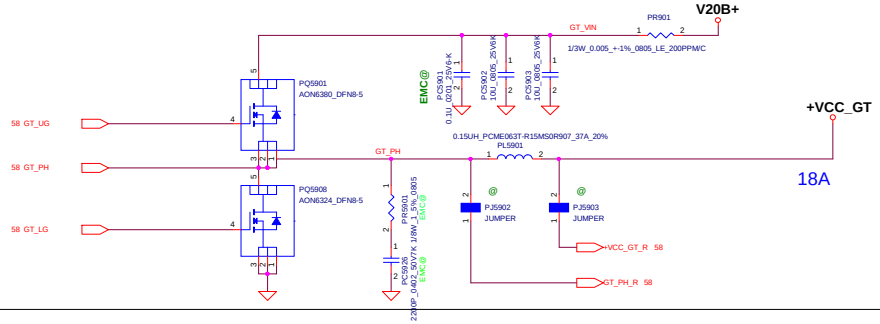
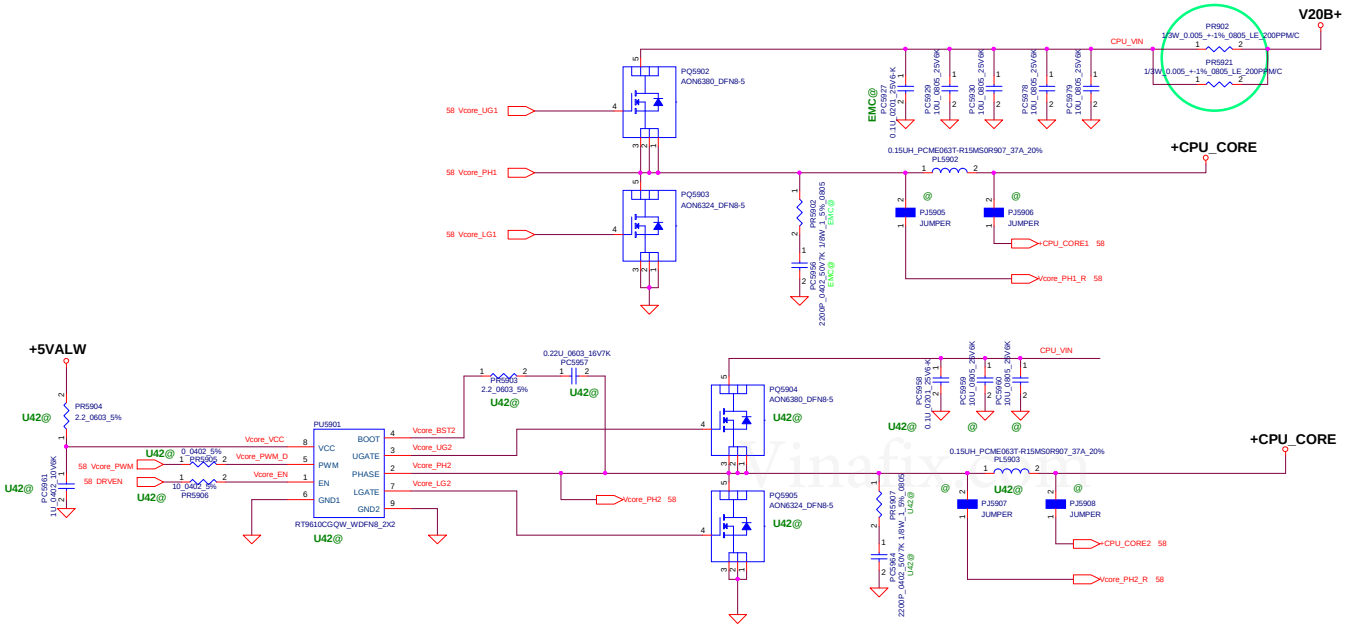
Title	PWR-CPU-CORE-1		
Size: b2	Document Number: 140S-WHL		Rev: 0.3
Date: Friday, October 26, 2018	Sheet 58 of 61		




```
Vboot=0V        Loadline=3.1mΩ
Ripple=+30mV/-10mV(0A~0.5A)
Ripple=± 10mV(0.5A~TDC)
Ripple=± 15mV(TDC~Iccmax)
TDC=18A  Iccmax=31A  OCP=37A
OVP=VID+370mV~VID+430mV
Max  Overshoot:70mv/10us
UVP=VID-370mV~VID-225mV
Fsw=550Khz
```

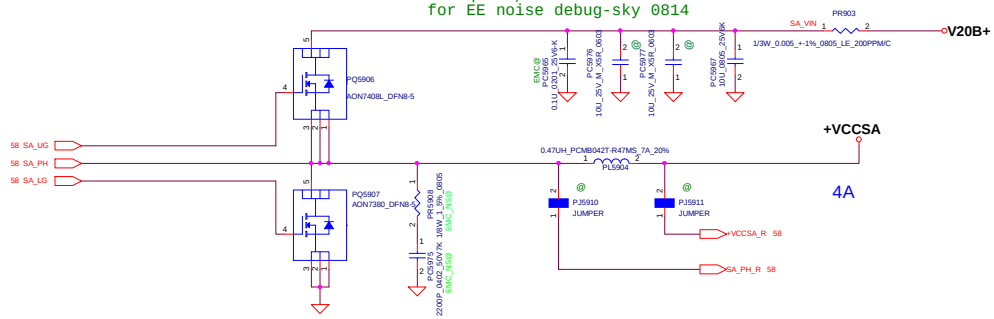



```
U22 :21A
U42: 48A
```

```
Vboot=0V        Loadline=1.8mΩ
Ripple=+30mV/-10mV(0A~0.5A)
Ripple=± 10mV(0.5A~TDC)
Ripple=± 15mV(TDC~Iccmax)
TDC=21A/48A  Iccmax=32A/70A
OCP=37A / 74A
Max  Overshoot:70mv/10us
OVP=VID+370mV~VID+430mV
UVP=VID-370mV~VID-225mV
Fsw=550Khz
```



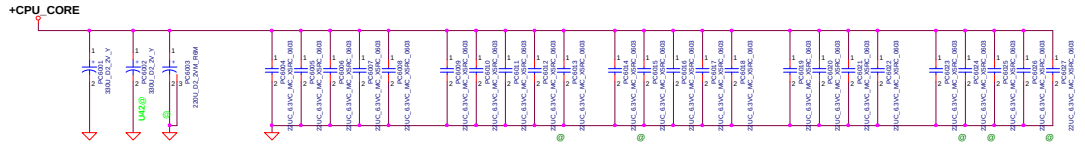
```
ME require, so PC5500/PC5501 reverve
 for EE noise debug-sky 0814
```




```
Vboot=0V        Loadline=10.3Ω
Ripple=+30mV/-10mV(0A~0.5A)
Ripple=± 10mV(0.5A~TDC)
Ripple=± 15mV(TDC~Iccmax)
TDC=4A  Iccmax=4.5A  OCP=7A
Max  Overshoot:70mv/10us
OVP=VID+370mV~VID+430mV
UVP=VID-370mV~VID-225mV
Fsw=550Khz
```

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title	PWR-CPU-CORE-2		
Size: A2	Document Number: 140S-WHL		Rev: 0.3
Date: Friday, October 26, 2018	Sheet 59 of 61		

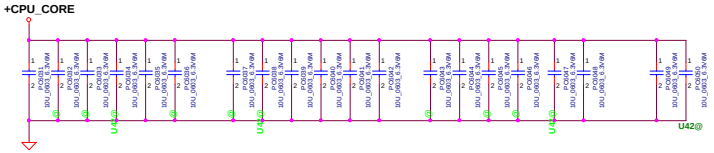


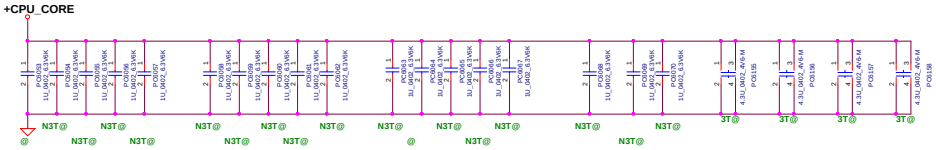
CPU_CORE: 2PCS_330U_D2_2V+1PCS_220U_D2_2V
+13PCS_22U_0603_6V+18PCS_10U_0402_6V
+16PCS_1U_0201_6V=

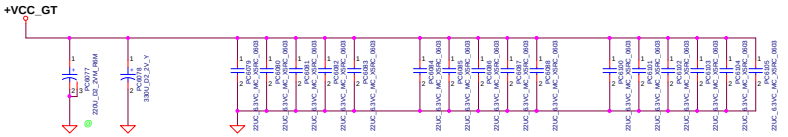
Vender modify_20180705
PC6003 @ and stuff 6 pcs 22U/0603

sky modify_20180709
change 10U/0402 to 10U/0603, 1U/0201 to 1U/0402

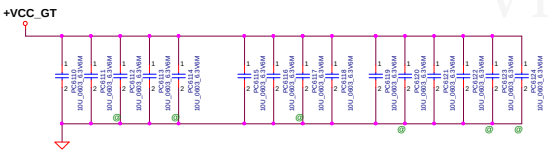
sky modify_20180925
layout change PC6024/PC6025 to PC6036/PC6046

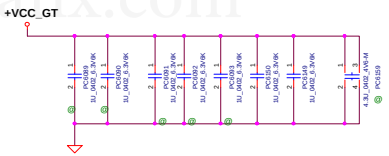




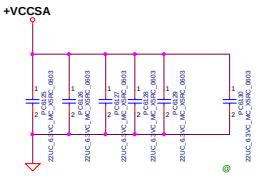


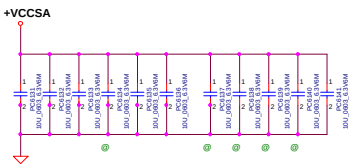
VCCGT: 1PCS_330U_D2_2V+1PCS_220U_D2_2V
+10PCS_22U_0603_6V+9PCS_9U_0603_6V
+2PCS_1U_0402_6V= sky_07_09

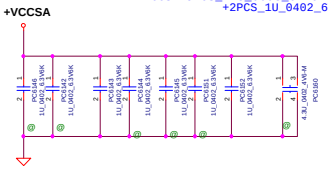




VCCSA:5PCS_22U_0603_6V+6PCS_10U_0603_6V
+2PCS_1U_0402_6V=07-09 sky







Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-CPU Decoupling Cap

Size	Document Number	Rev
Custom	14GS-WHL	0.3

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PU801 RT_OPT@

RT8816AGQW_WQFN20_3X3
SA000081U00

PU801 UPI_OPT@

UP1666QQKF WQFN 20P CONTROLLER
SA00008G000

GPU solution

OPTN17@	OPTN17@	OPTN17@	OPTN17@	OPTN17@	OPTN17@
PR816	PR812	PR815	PR813	PR818	PC826
6.19K_0402_1%	20.5K_0402_1%	4.32K_0402_1%	16.5K_0402_1%	309_0402_1%	4700P_0402_25V
SD000015G00	SD034205283J	SD00000J28J	SD034165283J	SD00001XX00	SE075472K8J

N17 solution

OPTN16@	OPTN16@	OPTN16@	OPTN16@	OPTN16@	OPTN16@
PR816	PR812	PR815	PR813	PR818	PC826
20K_0402_1%	20K_0402_1%	2K_0402_5%	18K_0402_1%	0_0402_5%	2700P_0402_50V
SD034200283J	SD034200283J	SD034200183J	SD00000058J	SD02800008j	SE00000ZJ00

N16 solution

U42@	U42@	U42@	U42@
PR5835	PR5841	PR5861	PR5869
1.8K +-1% 0402	61.9K +-1% 0402	464 +-1% 0402	23.2K +-1% 0402
SD00000R58J	SD034619283J	SD00001CP00	SD00001NZ00

U42 solution

U22@	U22@	U22@	U22@
PR5835	PR5841	PR5861	PR5869
2.32K +-1% 0402	47.5K +-1% 0402	1.8K +-1% 0402	19.6K +-1% 0402
SD000016300	SD034475283J	SD00000R58J	SD00000358J

U22 solution

Component	Value	N17	N16S-GTR
R1(KΩ)	PR816	6.19	20
R2(KΩ)	PR812	20.5	20
R3(KΩ)	PR815	4.32	2
R4(KΩ)	PR813	16.5	18
R5(KΩ)	PR818	0.309	0
C(nF)	PC826	4.7	2.7

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: ***NGFF_SSD_1***

Size	Document Number	Rev
C	***EYG10***	0.2

Date: Friday, October 26, 2018 Sheet 61 of 60