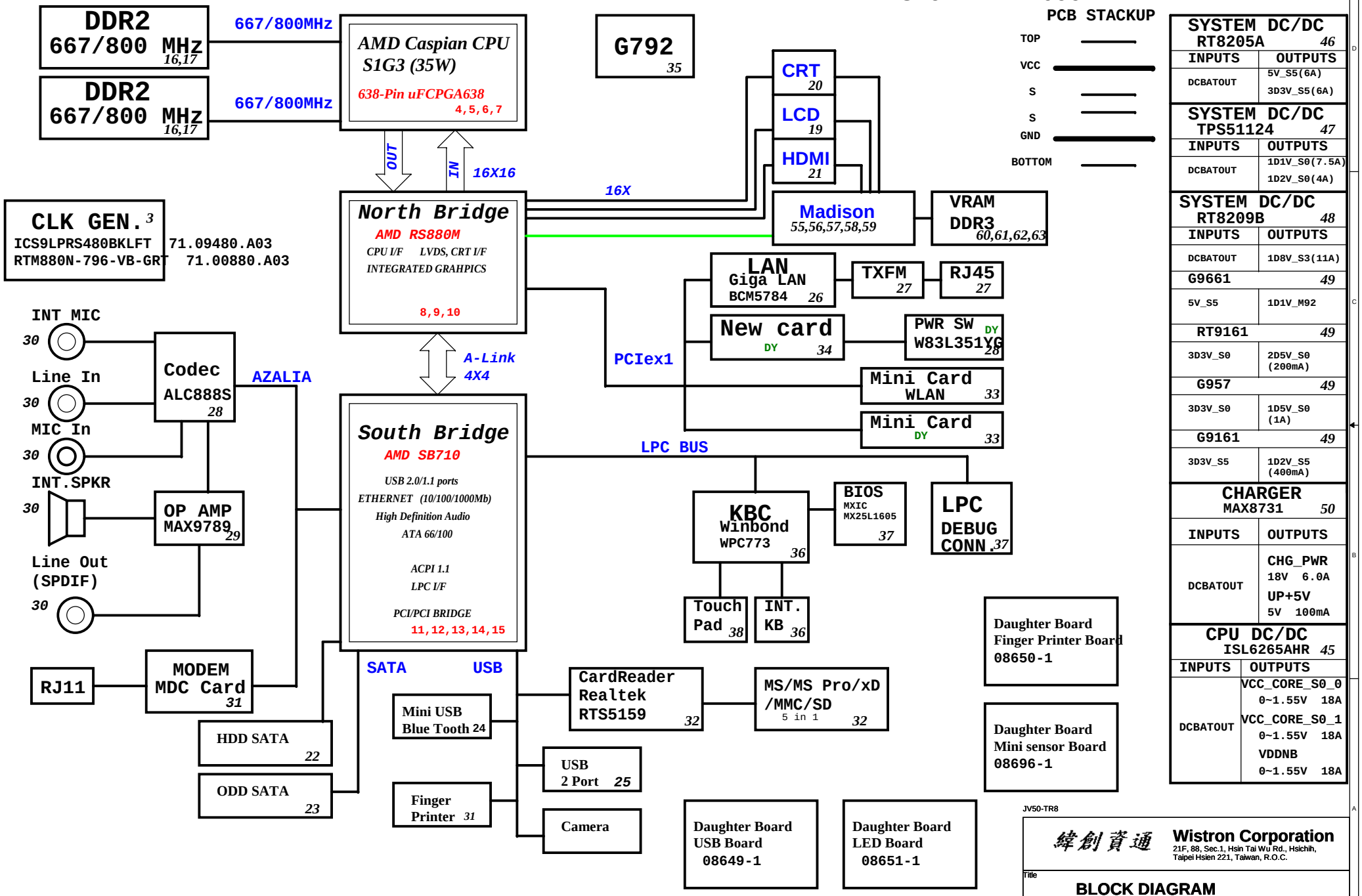
JV50-TR_8VRAM Block Diagram

Project code: 91.4FN01.001
PCB P/N : 48.4FN02.001
REVISION : 09927-1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC RT8205A 46

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC TPS51124 47

INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A) 1D2V_S0(4A)

SYSTEM DC/DC RT8209B 48

INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)
G9661 49	
5V_S5	1D1V_M92
RT9161 49	
3D3V_S0	2D5V_S0 (200mA)
G957 49	
3D3V_S0	1D5V_S0 (1A)
G9161 49	
3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731 50

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265AHR 45

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 05, 2009 Sheet 1 of 63

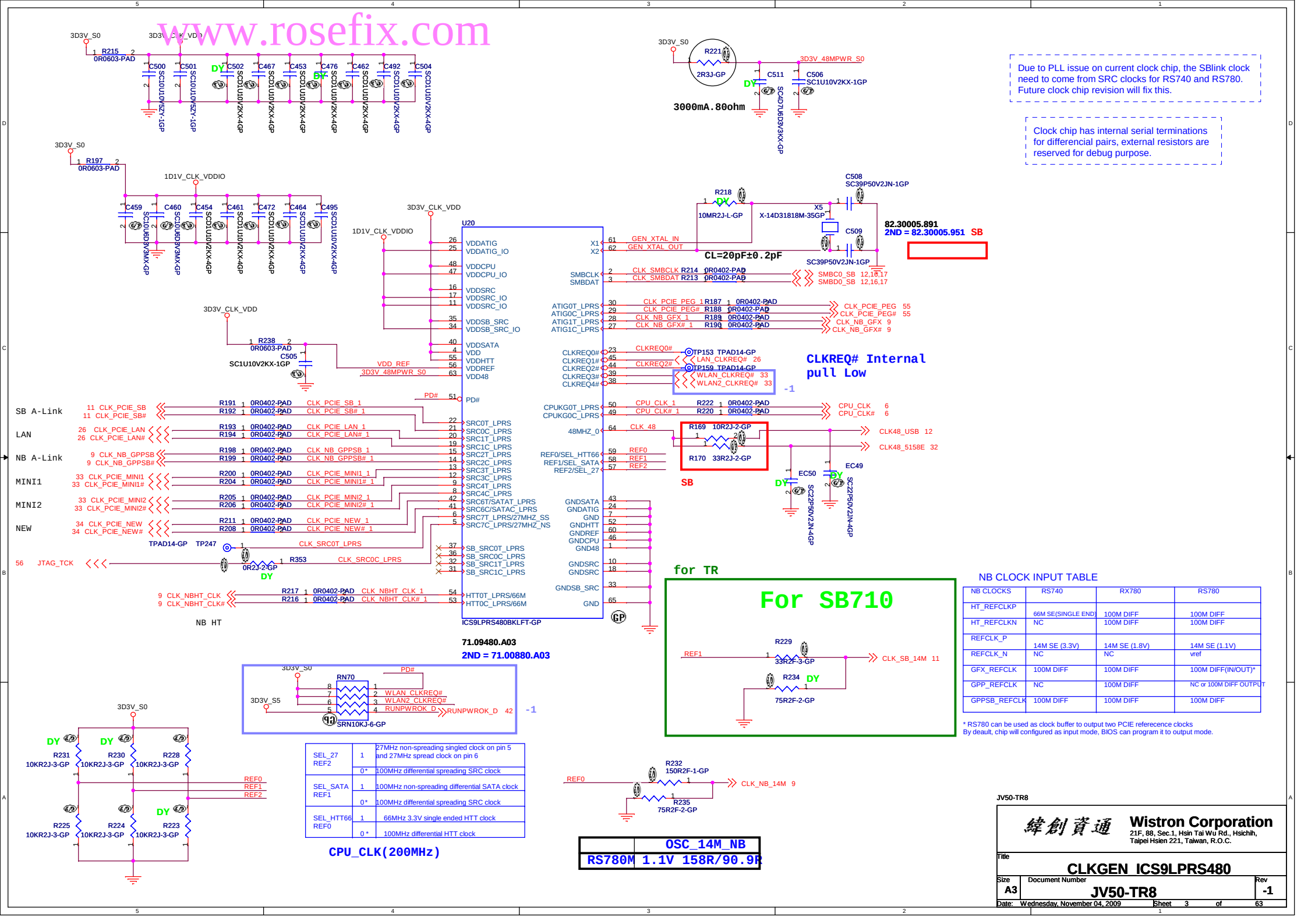
JV50-TR8

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB/PCIE Routing**

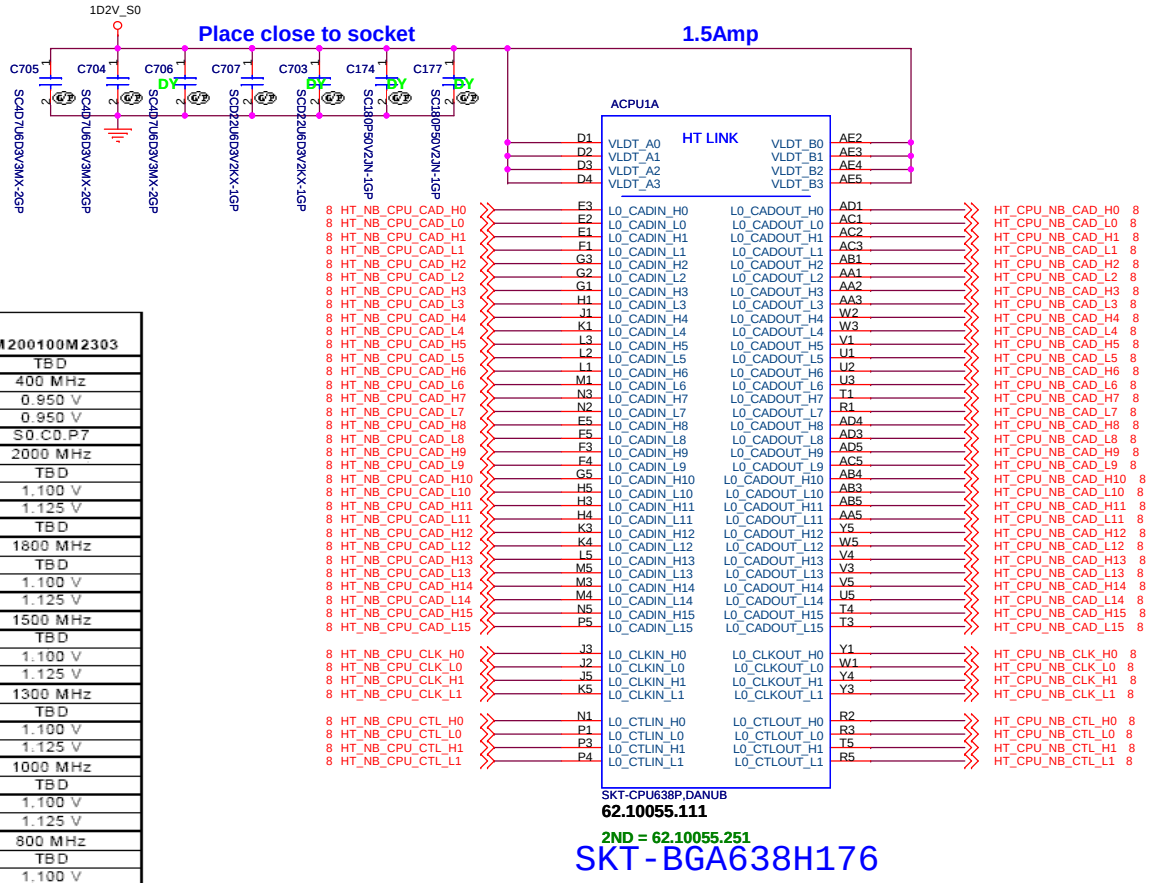
Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 05, 2009 Sheet 2 of 63



NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

SEL_27 REF2	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0 *	100MHz differential spreading SRC clock
SEL_SATA REF1	1	100MHz non-spreading differential SATA clock
	0 *	100MHz differential spreading SRC clock
SEL_HTT66 REF0	1	66MHz 3.3V single ended HTT clock
	0 *	100MHz differential HTT clock



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

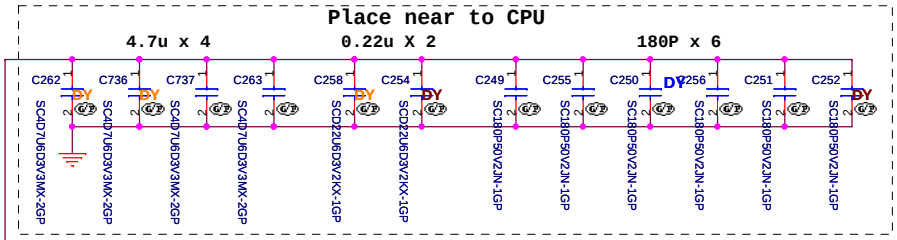
JV50-TR8

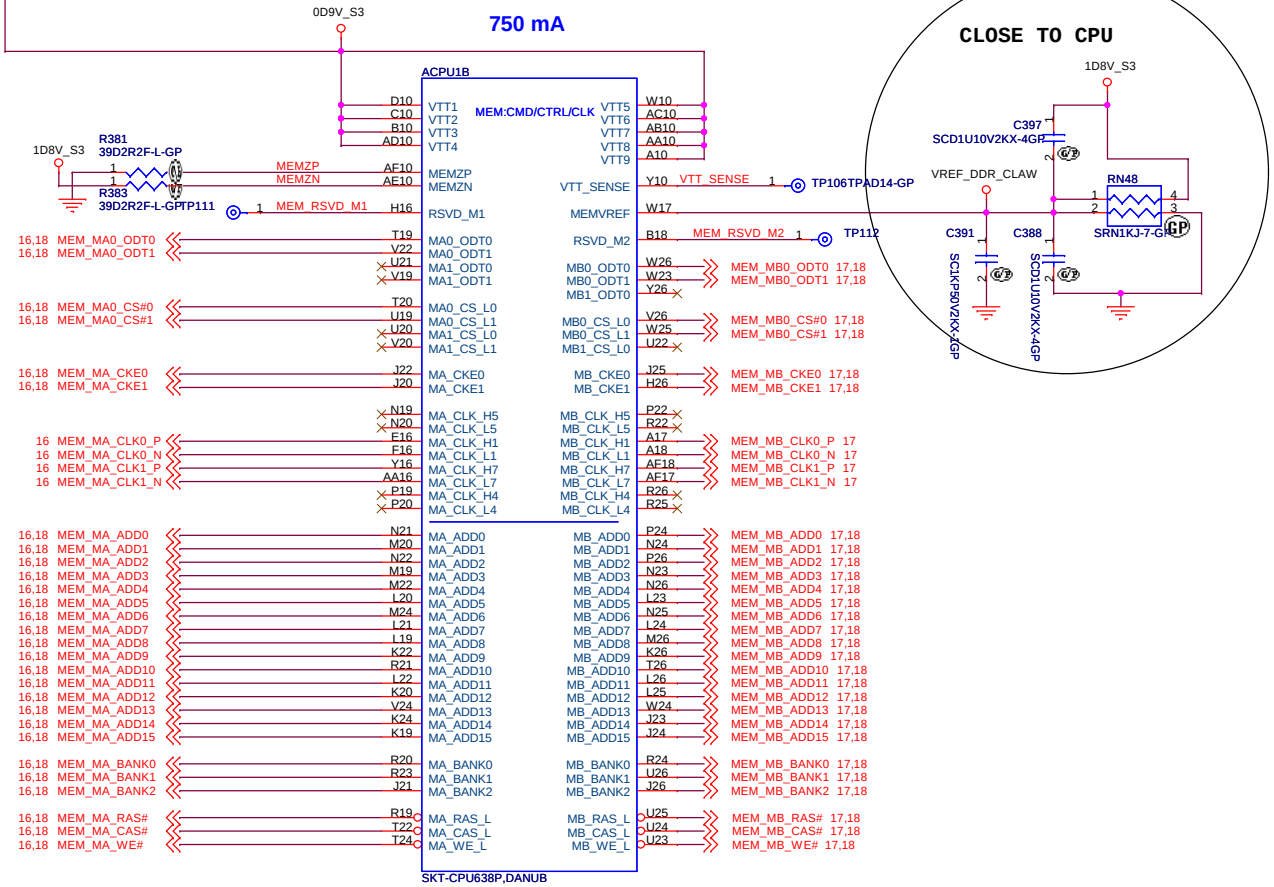
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

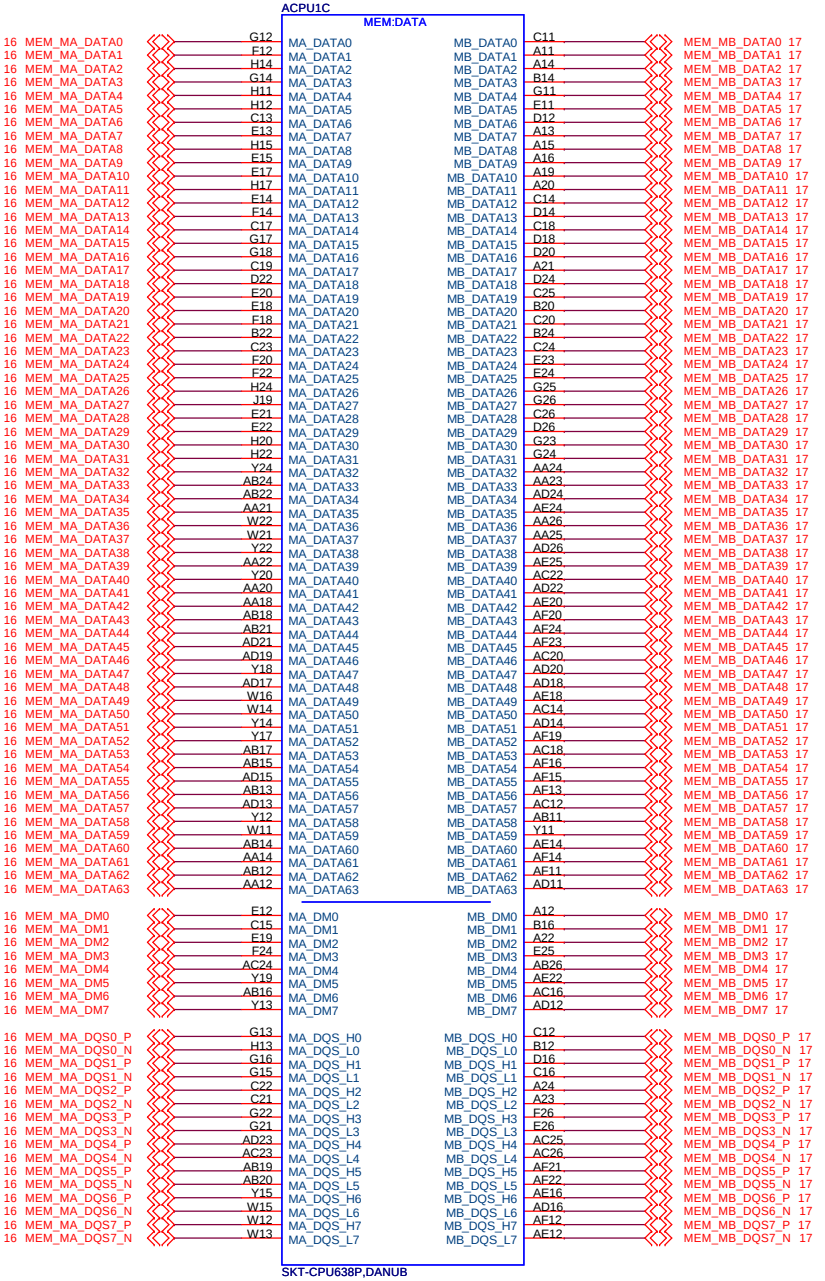
Title: CPU_HT_LINK I/F (1/4)

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 26, 2009 Sheet 4 of 63







JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR_(2/4)

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 26, 2009 Sheet 5 of 63

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

Cloce To CPU

for TR

for TR

Near CPU PIN

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

-1_20091021

CPU exceeds to 125℃

84.T3904.C11
2ND = 84.03904.L06

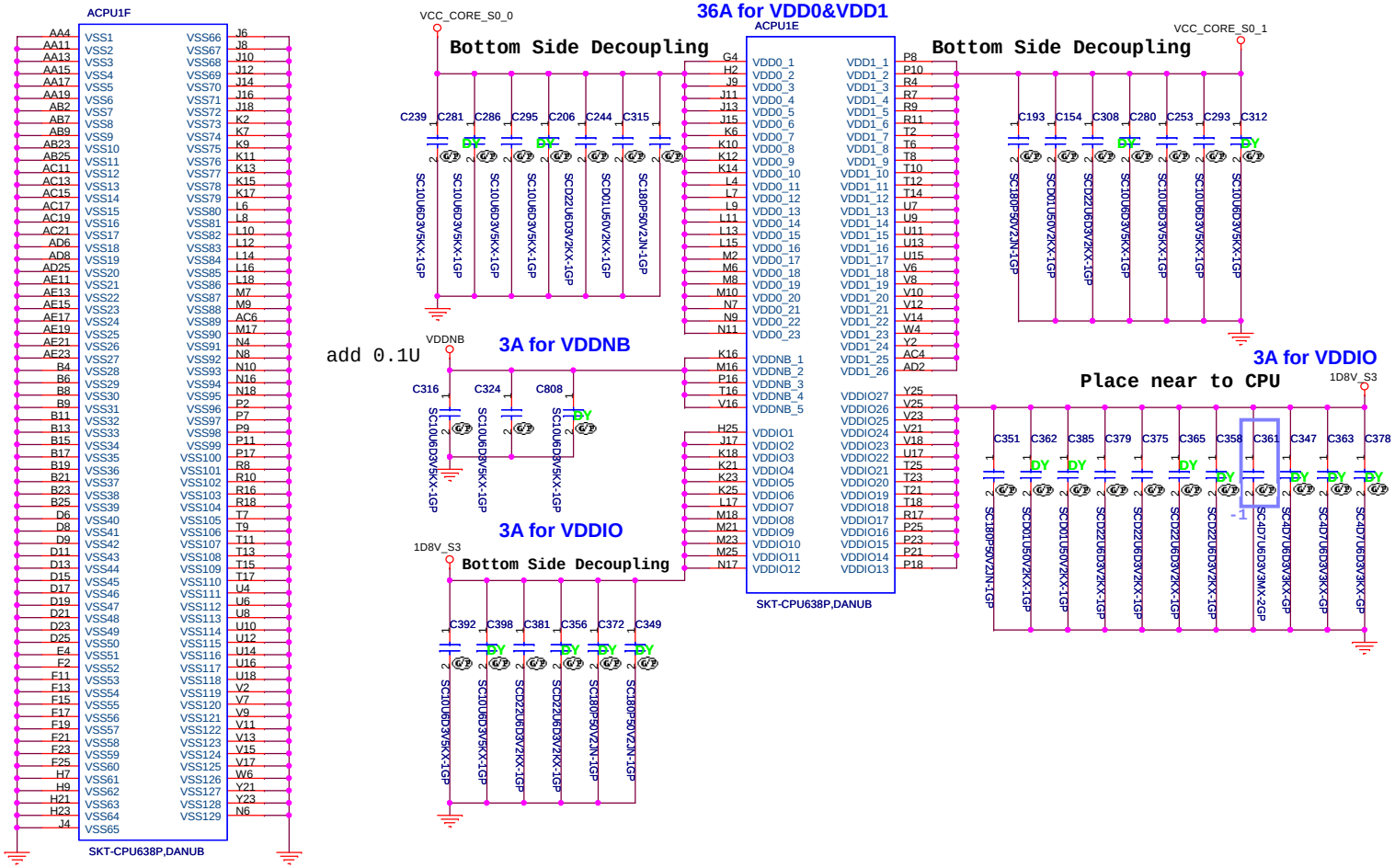
SKT-CPU638P,DANUBU

HDT Connectors

SMC-CONN26A-FP

JV50-TR8

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU_Control&Debug_(3/4)		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 6 of 63	



JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_Power_(4/4)	
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 05, 2009	Sheet 7 of 63	

ANB1A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

RS780M-GP-U2

HT_CPU_NB_CAD_H0 Y25 … HT_CPU_NB_CAD_L7 N25 — HT_RXCAD0P … HT_RXCAD7N

HT_CPU_NB_CAD_H8 AC24 … HT_CPU_NB_CAD_L15 U18 — HT_RXCAD8P … HT_RXCAD15N

HT_CPU_NB_CLK_H0 T22, HT_CPU_NB_CLK_L0 T23, HT_CPU_NB_CLK_H1 AB23, HT_CPU_NB_CLK_L1 AA22 — HT_RXCLK0P, HT_RXCLK0N, HT_RXCLK1P, HT_RXCLK1N

HT_CPU_NB_CTL_H0 M22, HT_CPU_NB_CTL_L0 M23, HT_CPU_NB_CTL_H1 R21, HT_CPU_NB_CTL_L1 R20 — HT_RXCTL0P, HT_RXCTL0N, HT_RXCTL1P, HT_RXCTL1N

R344 301R2F-GP: HT_RXCALP C23 — HT_RXCALN A24

Place < 100mils from pin C23 and A24

HT_TXCAD0P D24 … HT_TXCAD7N K22 — HT_NB_CPU_CAD_H0 … HT_NB_CPU_CAD_L7

HT_TXCAD8P F21 … HT_TXCAD15N M18 — HT_NB_CPU_CAD_H8 … HT_NB_CPU_CAD_L15

HT_TXCLK0P H24, HT_TXCLK0N H25, HT_TXCLK1P L21, HT_TXCLK1N L20 — HT_NB_CPU_CLK_H0, HT_NB_CPU_CLK_L0, HT_NB_CPU_CLK_H1, HT_NB_CPU_CLK_L1

HT_TXCTL0P M24, HT_TXCTL0N M25, HT_TXCTL1P P19, HT_TXCTL1N R18 — HT_NB_CPU_CTL_H0, HT_NB_CPU_CTL_L0, HT_NB_CPU_CTL_H1, HT_NB_CPU_CTL_L1

HT_TXCALP B24, HT_TXCALN B25 — R343 301R2F-GP: HT_TXCALP, HT_TXCALN

Place < 100mils from pin B25 and B24

Placement: close RS780

Placement: close RS780

ANB1B

PART 2 OF 6

PCIE I/F GFX

PEG_RXP0 D4 … PEG_RXP15 T3 — GFX_RX0P … GFX_RX15N

PEG_TXP0 A5 … PEG_TXP15 P2 — GFX_TX0P … GFX_TX15N

55 PEG_RXN[15..0]

55 PEG_RXP[15..0]

PEG_TXP[15..0] 55

PEG_TXN[15..0] 55

DIS 1 — C617 SCD1U16V2KX-3GP PEG_TXP0 … C578 SCD1U16V2KX-3GP PEG_TXP15

PEG_TXN0 … PEG_TXN15

for TR

RS780M Display Port Support(muxed on GFX)

DP0	GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1	GFX_TX4,TX5,TX6,TX7,AUX1,HPD1

GTXP0 UMA C30 1 — SCD1U16V2KX-3GP — HDMI_DATA2+ 21

GTXN0 UMA C29 1 — SCD1U16V2KX-3GP — HDMI_DATA2- 21

GTXP1 UMA C27 1 — SCD1U16V2KX-3GP — HDMI_DATA1+ 21

GTXN1 UMA C26 1 — SCD1U16V2KX-3GP — HDMI_DATA1- 21

GTXP2 UMA C25 1 — SCD1U16V2KX-3GP — HDMI_DATA0+ 21

GTXN2 UMA C22 1 — SCD1U16V2KX-3GP — HDMI_DATA0- 21

GTXP3 UMA C21 1 — SCD1U16V2KX-3GP — HDMI_CLK+ 21

GTXN3 UMA C19 1 — SCD1U16V2KX-3GP — HDMI_CLK- 21

PCIE I/F GPP

LAN 26 PCIE_RXP1 — AF3 GPP_RX0P

MINICARD1 26 PCIE_RXN1 — AD4 GPP_RX0N; 33 PCIE_RXP2 — AE2 GPP_RX1P

MINICARD2 33 PCIE_RXN2 — AD3 GPP_RX1N; 33 PCIE_RXP3 — AD1 GPP_RX2P

NEW CARD 33 PCIE_RXN3 — AD2 GPP_RX2N; 34 PCIE_RXP5 — V5 GPP_RX3P; 34 PCIE_RXN5 — W6 GPP_RX3N

U5 GPP_RX4P; U6 GPP_RX4N; U8 GPP_RX5P; U7 GPP_RX5N

TPAD14-GP TP21 — GPP_RX5P; TPAD14-GP TP20 — GPP_RX5N

GPP_TX0P … GPP_TX5N

AC1 TXP0 C621 1 — SCD1U16V2KX-3GP — PCIE_TXP1 26 (LAN)

AC2 TXN0 C622 1 — SCD1U16V2KX-3GP — PCIE_TXN1 26 (LAN)

AB4 TXP1 C597 1 — SCD1U16V2KX-3GP — PCIE_TXP2 33 (MINICARD1)

AB3 TXN1 C596 1 — SCD1U16V2KX-3GP — PCIE_TXN2 33 (MINICARD1)

AA2 TXP3 C599 1 — SCD1U16V2KX-3GP — PCIE_TXP3 33 (MINICARD2)

AA1 TXN3 C598 1 — SCD1U16V2KX-3GP — PCIE_TXN3 33 (MINICARD2)

Y1 TXP5 C600 1 — SCD1U16V2KX-3GP — PCIE_TXP5 34 (NEW CARD)

Y2 TXN5 C601 1 — SCD1U16V2KX-3GP — PCIE_TXN5 34 (NEW CARD)

Y4, Y3

V1 GPP_TX5P — TP16 TPAD14-GP

V2 GPP_TX5N — TP17 TPAD14-GP

A-LINK

PCIE I/F SB

11 ALINK_NBRX_SBTX_P0 … 11 ALINK_NBRX_SBTX_N3 — AA8 SB_RX0P … Y5 SB_RX3N

AD7 ALINK_NBTX_SBRX_P0 C642 1 — SCD1U16V2KX-3GP — ALINK_NBTX_C_SBRX_P0 11

AE7 ALINK_NBTX_SBRX_N0 C640 1 — SCD1U16V2KX-3GP — ALINK_NBTX_C_SBRX_N0 11

AE6 ALINK_NBTX_SBRX_P1 C632 1 — SCD1U16V2KX-3GP — ALINK_NBTX_C_SBRX_P1 11

AD6 ALINK_NBTX_SBRX_N1 C637 1 — SCD1U16V2KX-3GP — ALINK_NBTX_C_SBRX_N1 11

AB6 ALINK_NBTX_SBRX_P2 C627 1 — SCD1U16V2KX-3GP — ALINK_NBTX_C_SBRX_P2 11

AC6 ALINK_NBTX_SBRX_N2 C629 1 — SCD1U16V2KX-3GP — ALINK_NBTX_C_SBRX_N2 11

AD5 ALINK_NBTX_SBRX_P3 C624 1 — SCD1U16V2KX-3GP — ALINK_NBTX_C_SBRX_P3 11

AE5 ALINK_NBTX_SBRX_N3 C625 1 — SCD1U16V2KX-3GP — ALINK_NBTX_C_SBRX_N3 11

AC8 PCE_PCAL, AB8 PCE_NCAL — R315 1K27R2F-L-GP, R16 2KR2F-3-GP — 1D1V_S0

Place < 100mils from pin AC8 and AB8

JV50-TR8

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS880M_HT LINK&PCIe(1/3)

Size: A3 | Document Number: JV50-TR8 | Rev: -1

Date: Monday, October 26, 2009 | Sheet 8 of 63

STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable

SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

Close to NB ball

R69 BOM Option

for TR

ENABLE External CLK GEN
UMA-->L4-->2R 0603
C82-->47U/6.3V
DIS-->L4-->Bead
C82-->DY

	GPIO MODE	
STRP_DATA	0	*1
VCC_NB	1.1V	1.0V

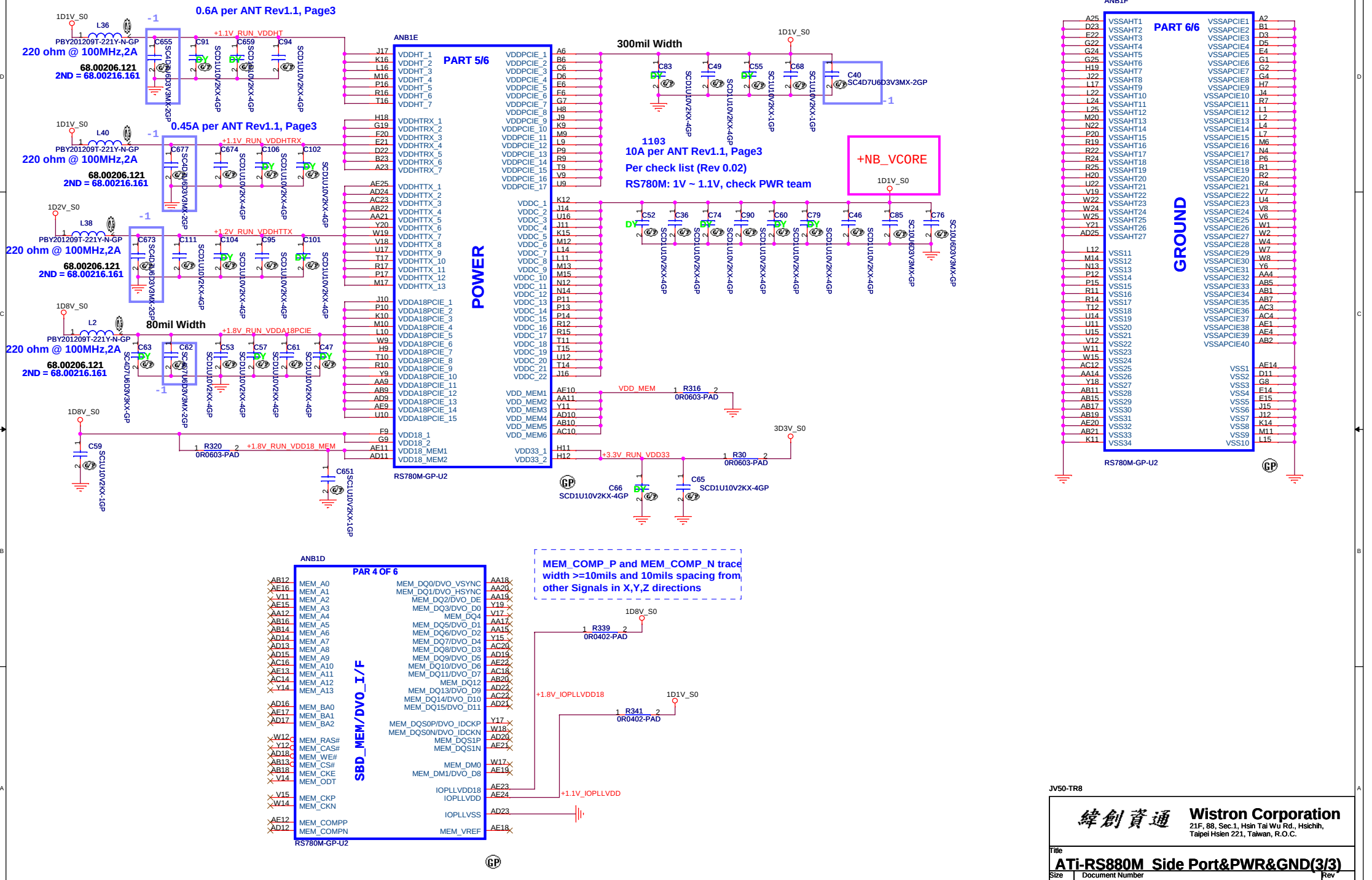
ANB1C
PART 3 OF 6
RS780M-GP-U2
CRT/TVOUT
LVTM
PLL/PWR
CLOCKs
PM
MIS.

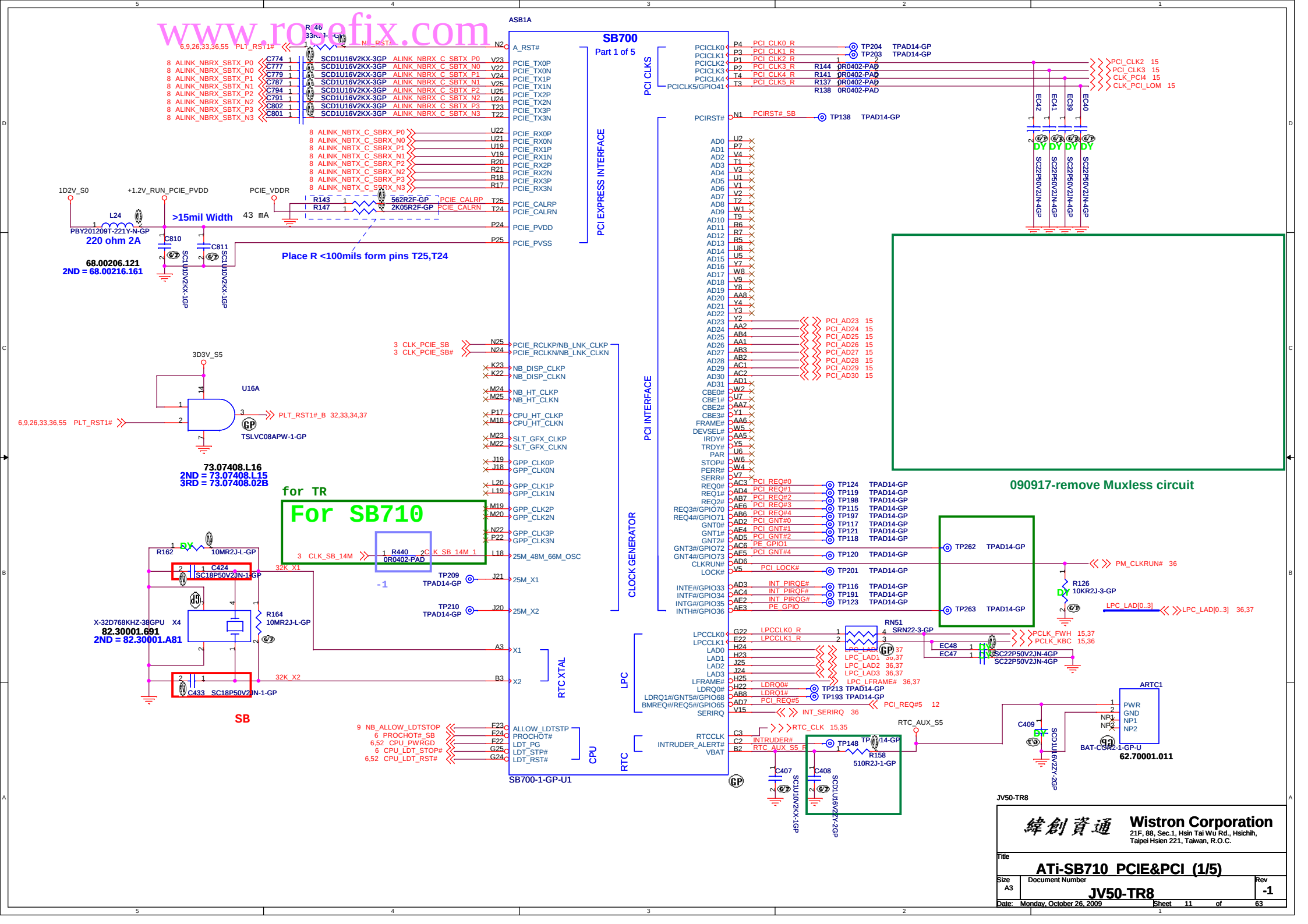
for TR
UMA

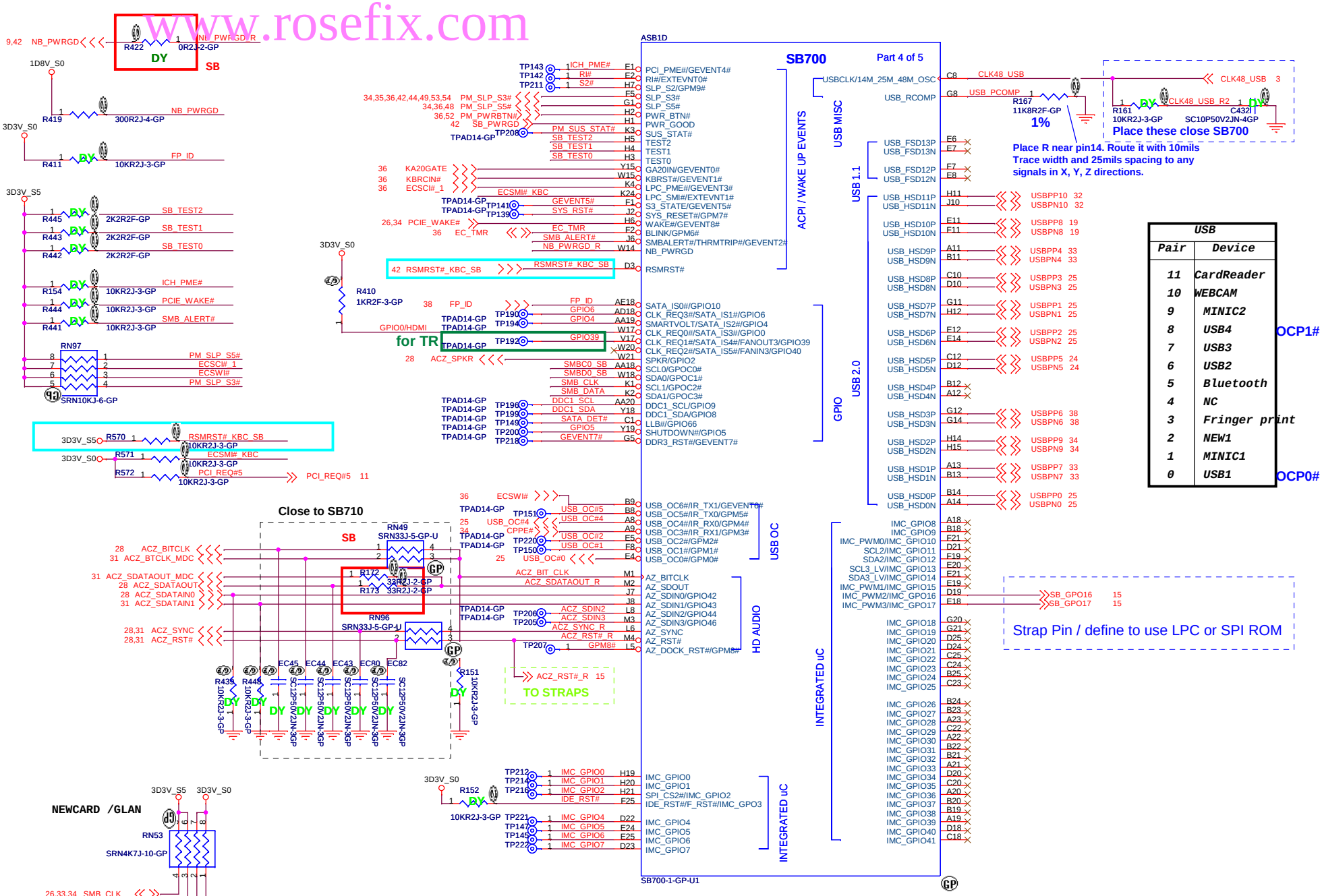
JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS880M LVDS&CRT (2/3)
Size: A3 | Document Number: JV50-TR8 | Rev: -1
Date: Monday, October 26, 2009 | Sheet 9 of 63







USB	
Pair	Device
11	CardReader
10	WEBCAM
9	MINIC2
8	USB4
7	USB3
6	USB2
5	Bluetooth
4	NC
3	Fringer print
2	NEW1
1	MINIC1
0	USB1

JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 USB&GPIO (2/5)

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Wednesday, November 11, 2009 Sheet 12 of 63

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB710

SATA HDD
SATA ODD

SB700
Part 2 of 5

ASB1B

SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR

Very Close to SB710

1ST 82.30020.851
2ND = 82.30020.791
SB

93 mA

>15mil Width

Dummy CKG select

CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0

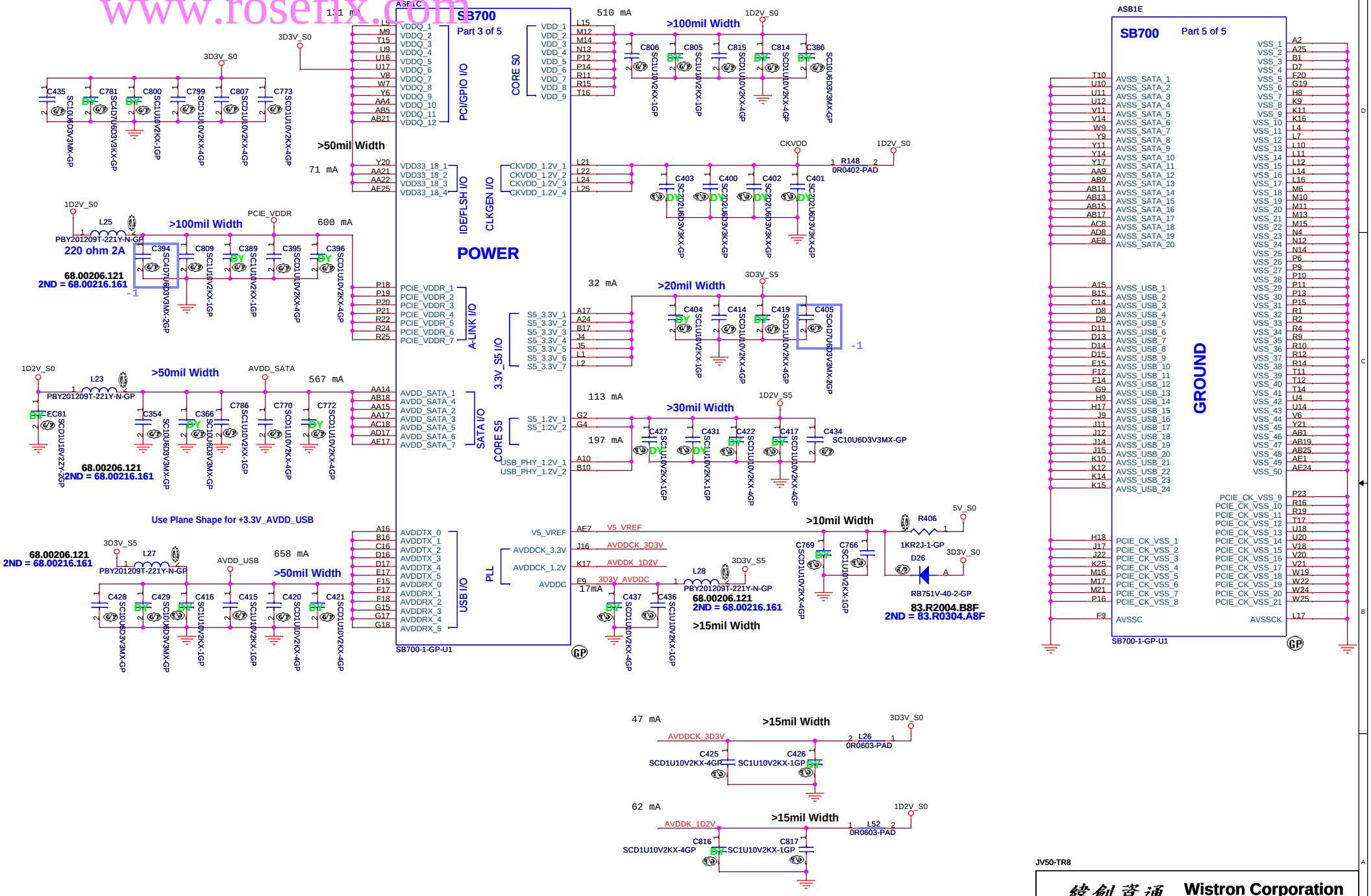
Layout connect to Cap then GND

SB700-1-GP-U1

JV50-TR8

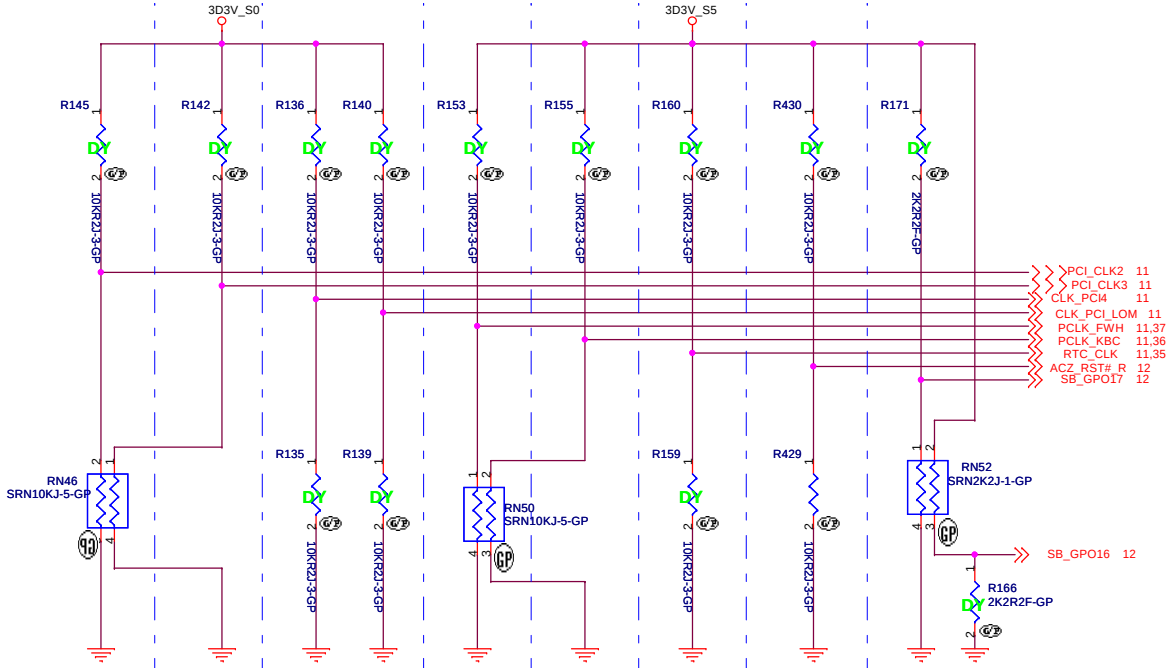
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 SATA-IDE (3/5)
Size: A3
Document Number: JV50-TR8
Rev: -1
Date: Monday, October 26, 2009
Sheet 13 of 63



REQUIRED STRAPS

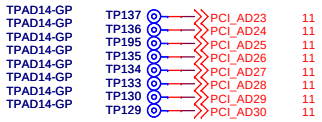
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved
								H, L = SPI ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM DEFAULT
								L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

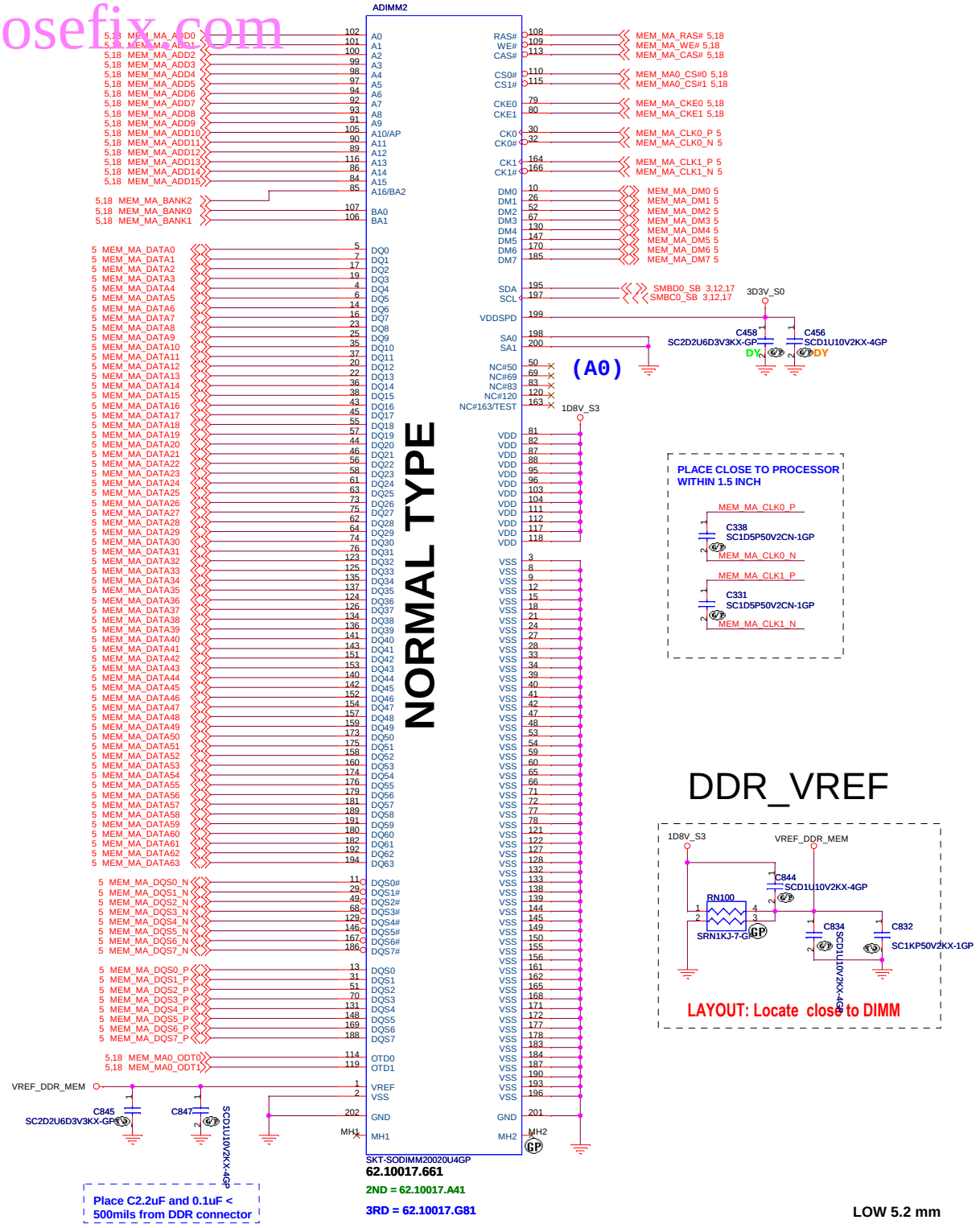
JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 STRAPPING (5/5)

Size	Document Number	Rev
A3	JV50-TR8	-1

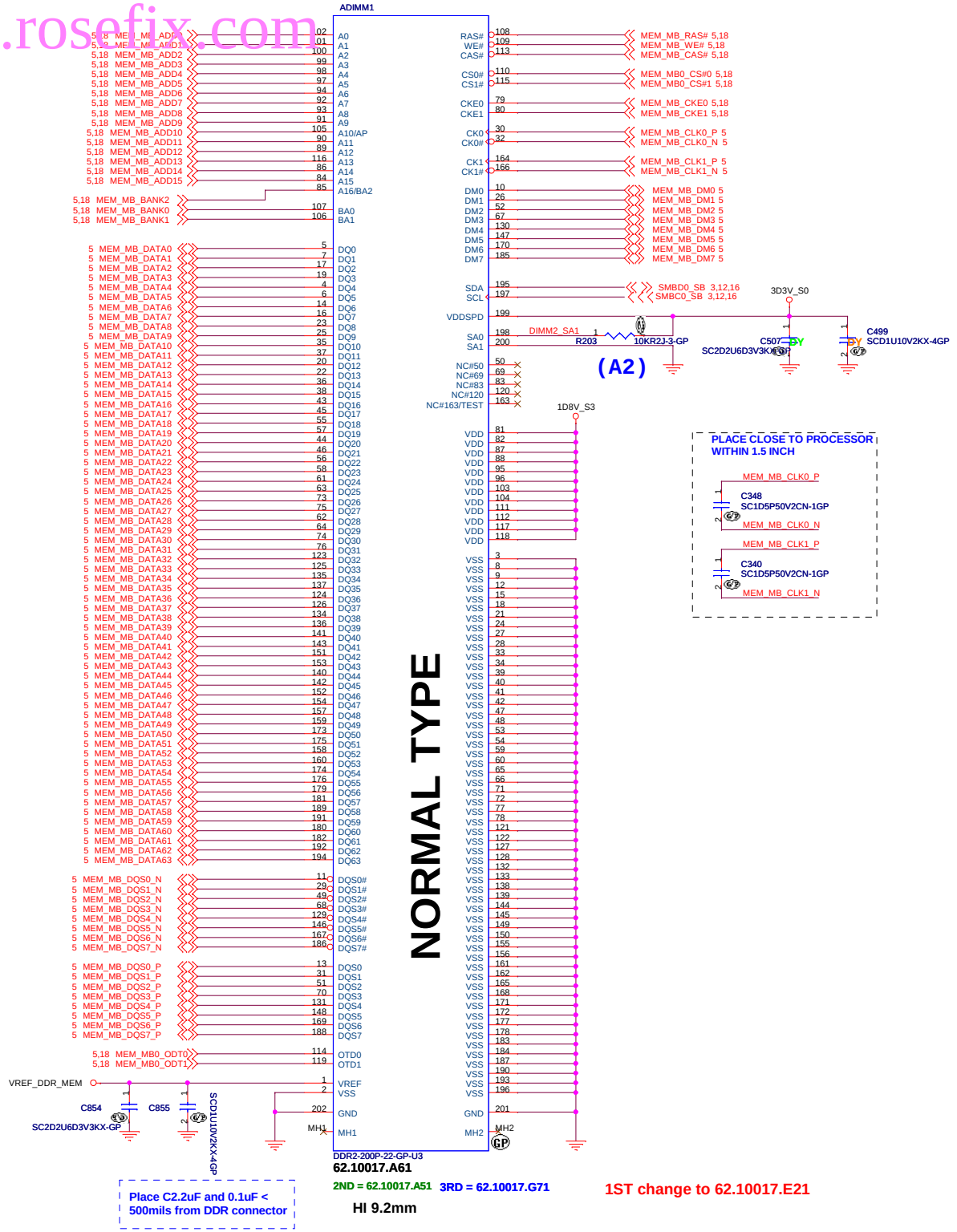
Date: Monday, October 26, 2009 Sheet 15 of 63



JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR_SO-DIMM SKT_1	
Size: Custom	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 16 of 63	



62.10017.A61

2ND = 62.10017.A51 3RD = 62.10017.G71

HI 9.2mm

1ST change to 62.10017.E21

JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

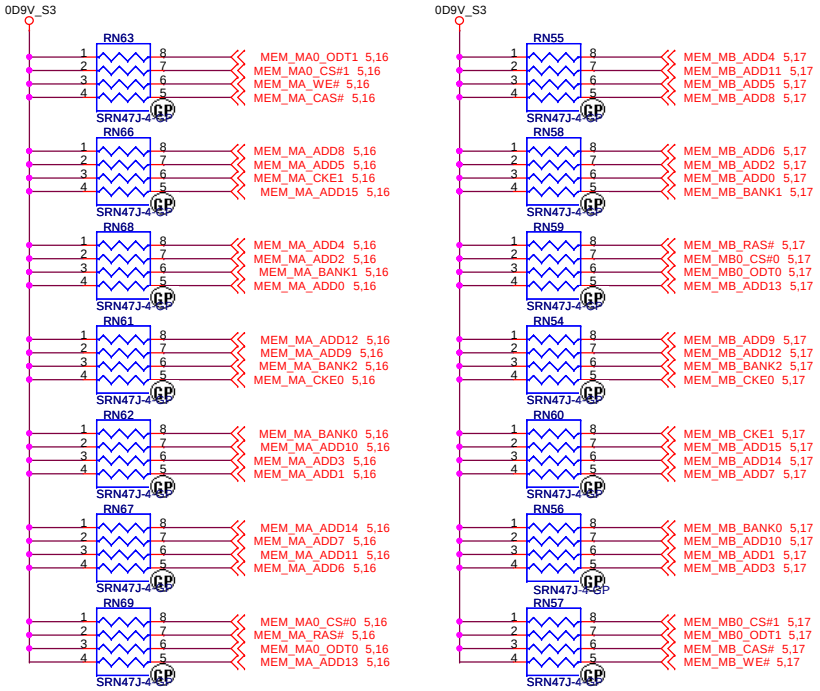
Title: DDR_SO-DIMM SKT_2

Size: Custom | Document Number: JV50-TR8 | Rev: -1

Date: Monday, October 26, 2009 | Sheet 17 of 63

PARALLEL TERMINATION

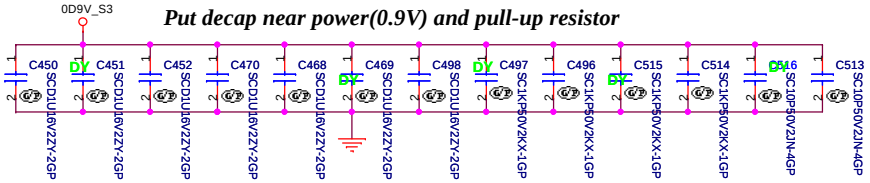
Put decap near power(0.9V) and pull-up resistor



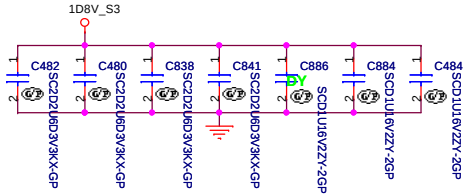
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

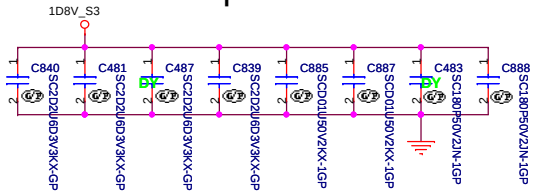


Place these Caps near DM1



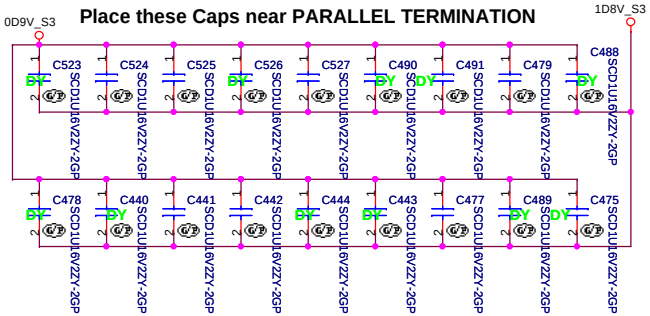
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



JV50-TR8

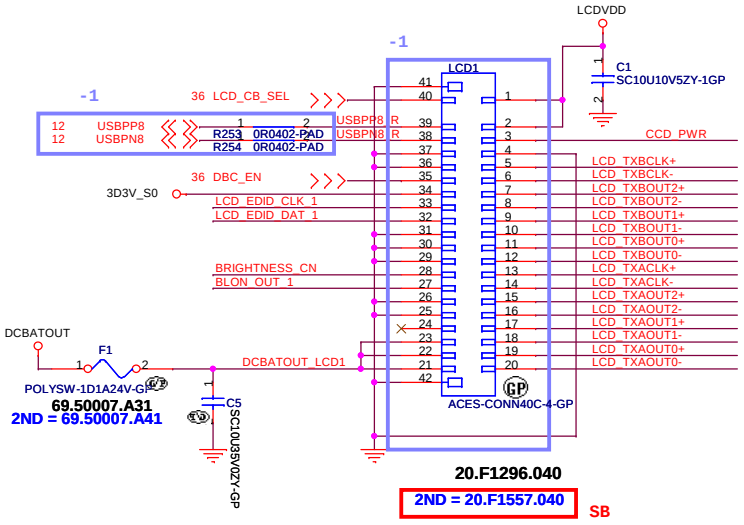
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

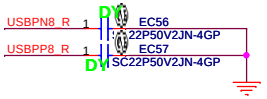
Title: **DDR_DAMPING & TERMINATION**

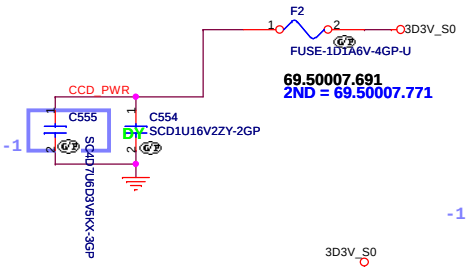
Size	Document Number	Rev
A3	JV50-TR8	-1

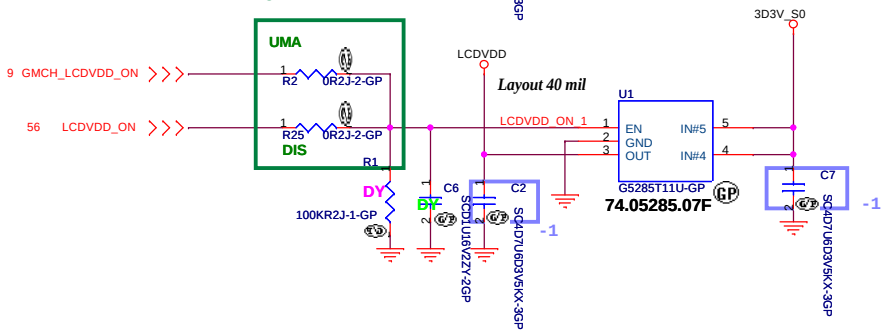
Date: Monday, October 26, 2009 Sheet 18 of 63

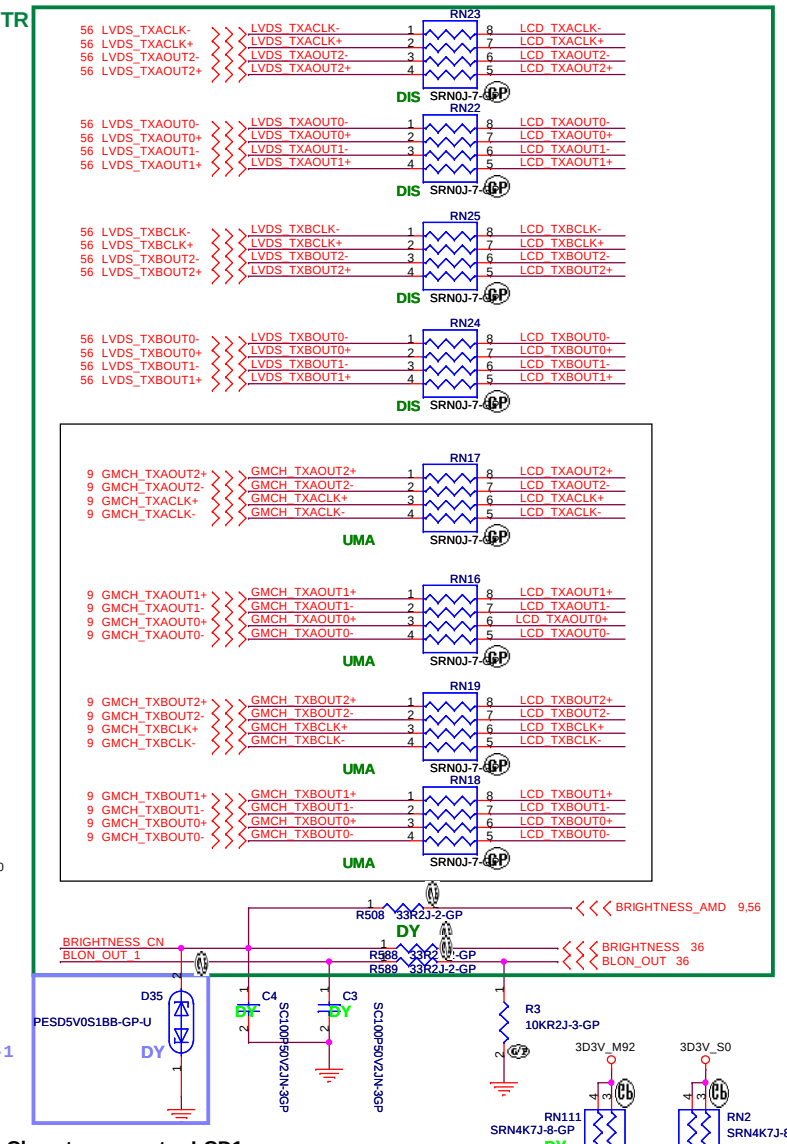
LCD/INVERTER/CCD CONN











Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

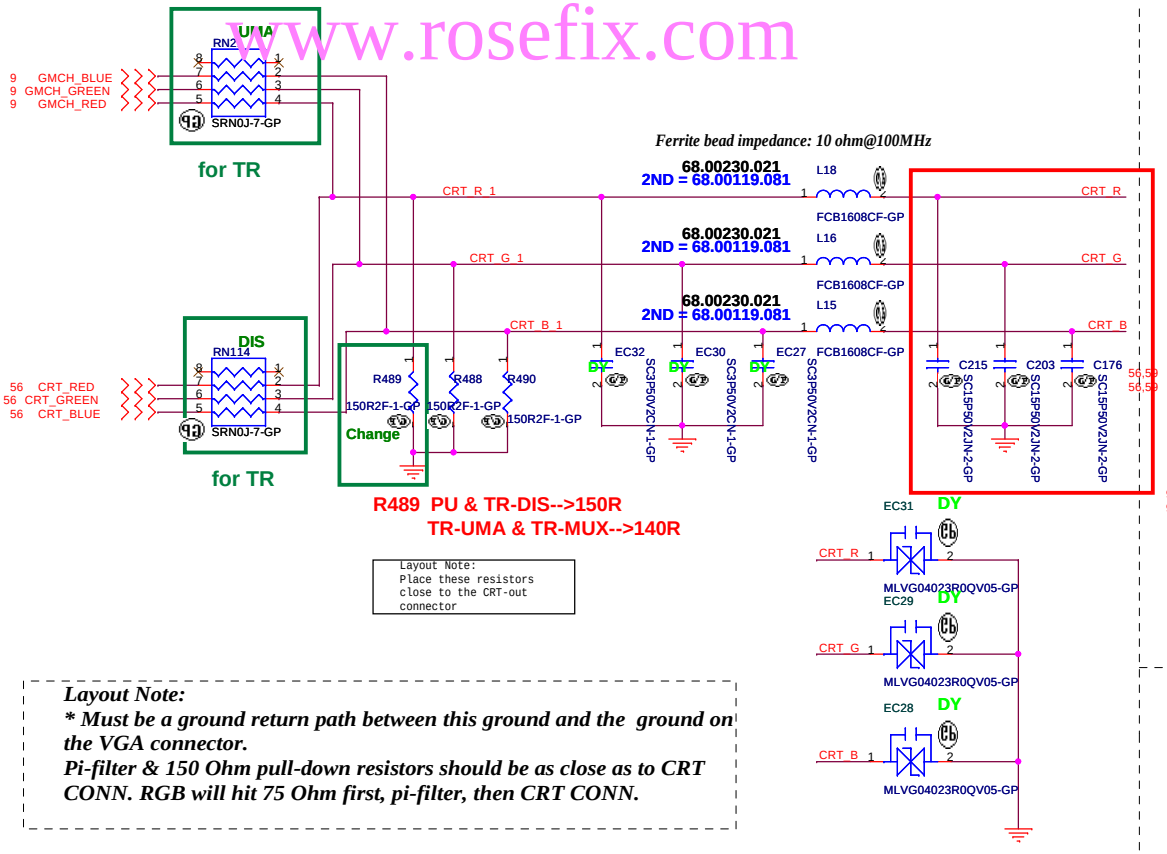
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

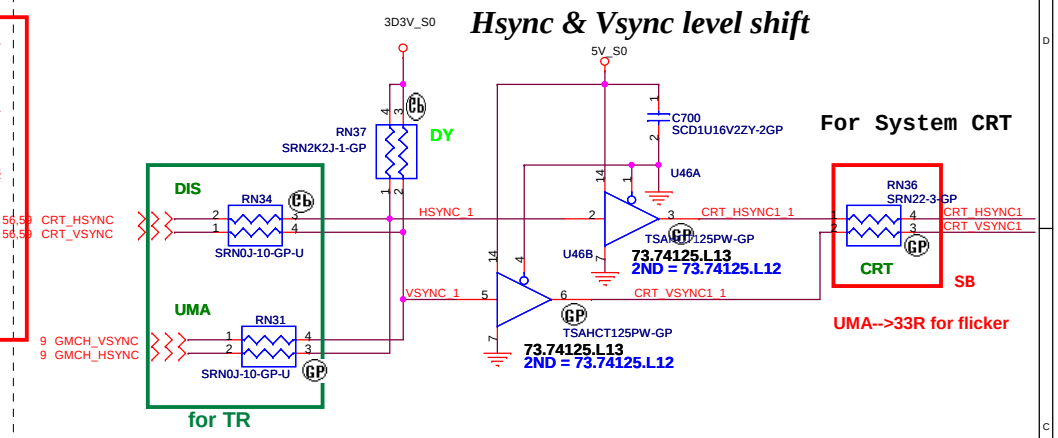
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

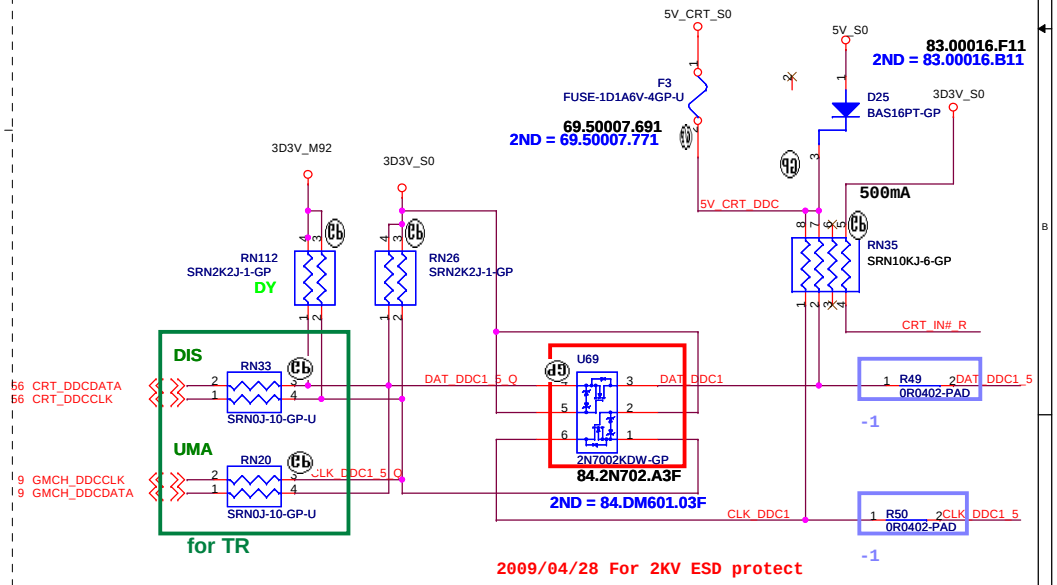
Title: LCD CONN

Size: A3 | Document Number: JV50-TR8 | Rev: -1

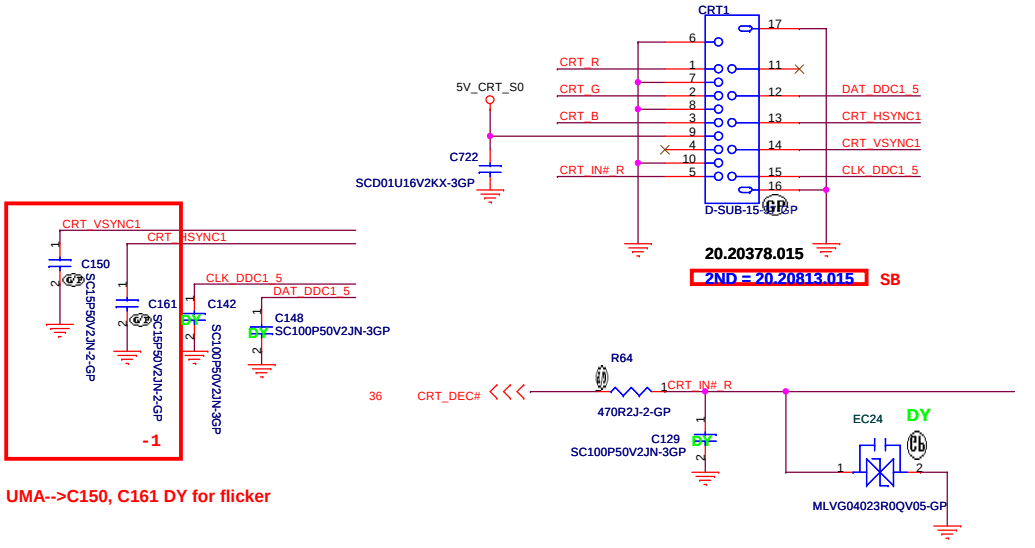
Date: Monday, October 26, 2009 | Sheet 19 of 63







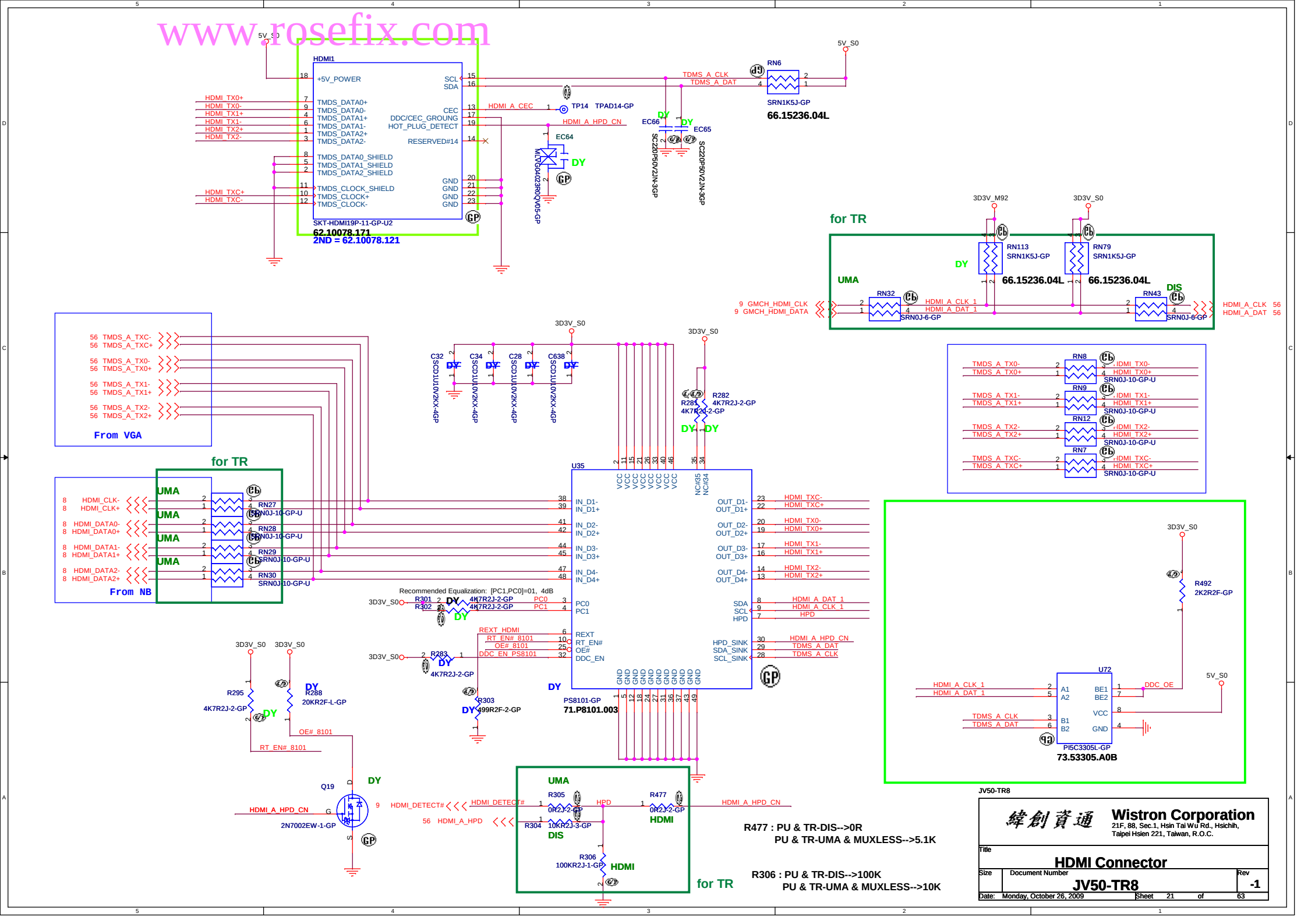
CRT I/F & CONNECTOR



JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

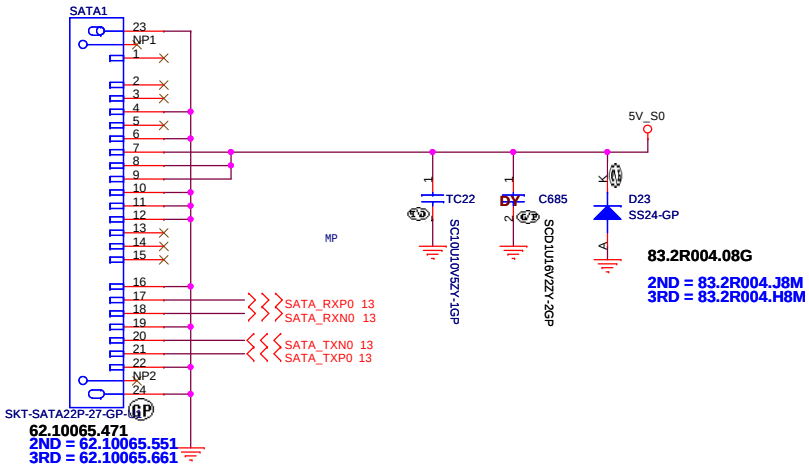
Title: CRT Connector
Size | Document Number: JV50-TR8 | Rev: -1
Date: Monday, October 26, 2009 | Sheet 20 of 63

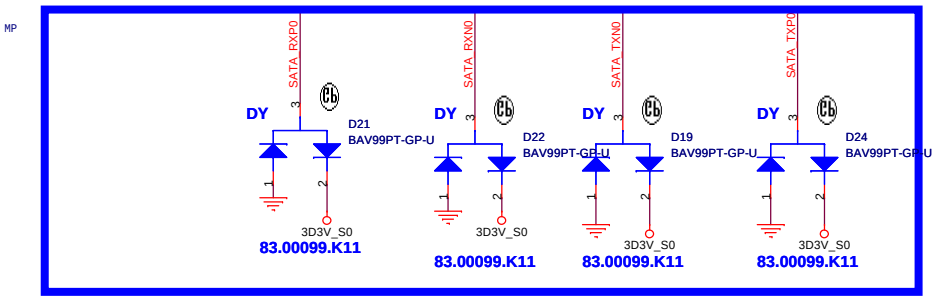


JV50-TR8

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**HDMI Connector**	
Size	Document Number **JV50-TR8**	Rev **-1**
Date: Monday, October 26, 2009	Sheet 21 of 63	

SATA Connector

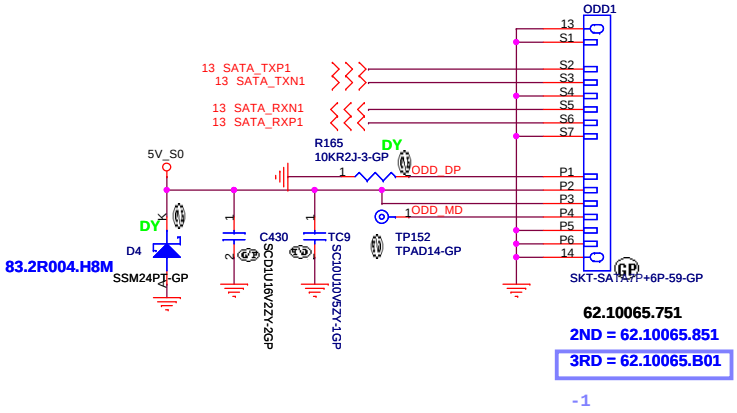


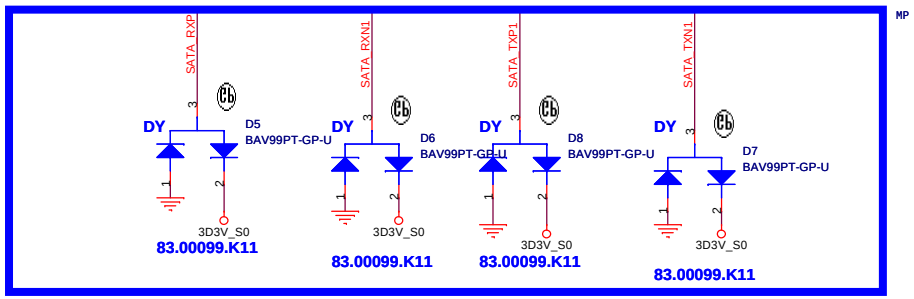


JV50-TR8

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD		
Size	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 22 of 63	

SATA ODD Connector



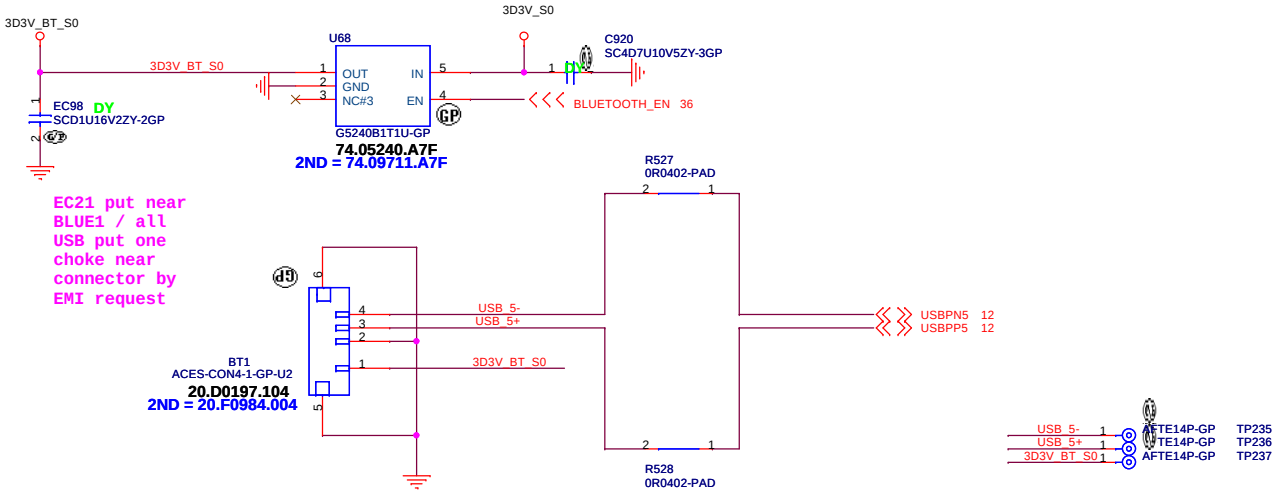


JV50-TR8

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ODD		
Size	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 23 of 63	

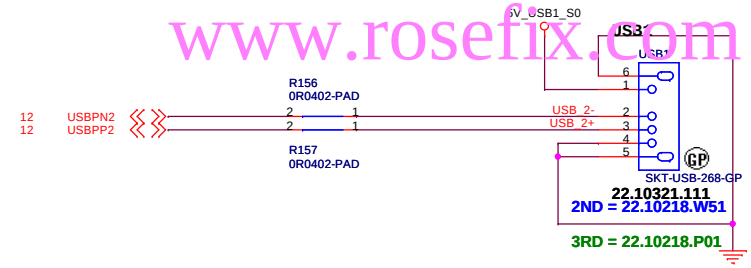
BLUETOOTH MODULE

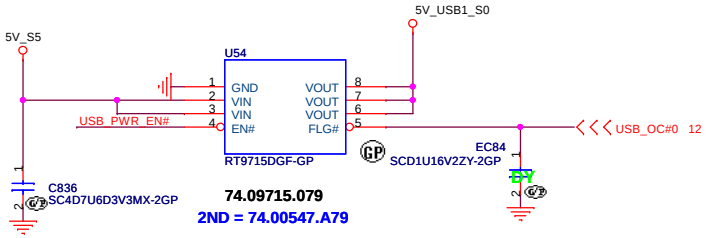
1.5A / High Active Voltage 2V

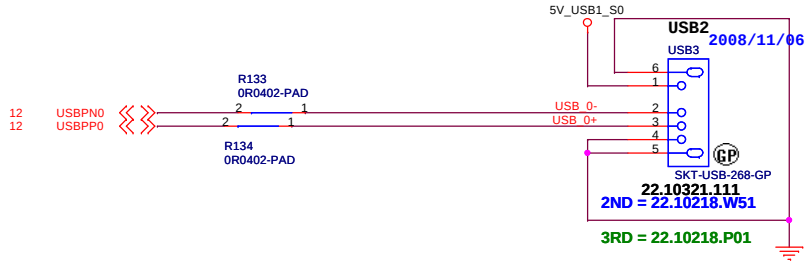


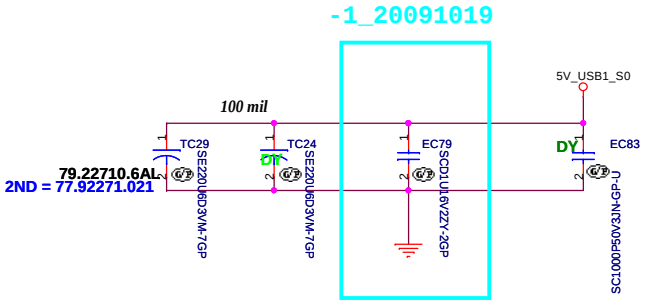
JV50-TR8

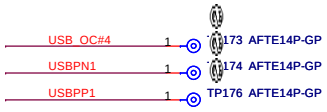
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	BLUETOOTH
Size	Document Number: JV50-TR8 — Rev: -1
Date: Thursday, November 12, 2009	Sheet 24 of 63

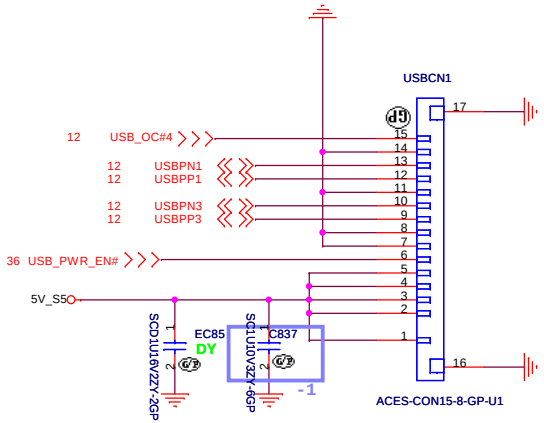


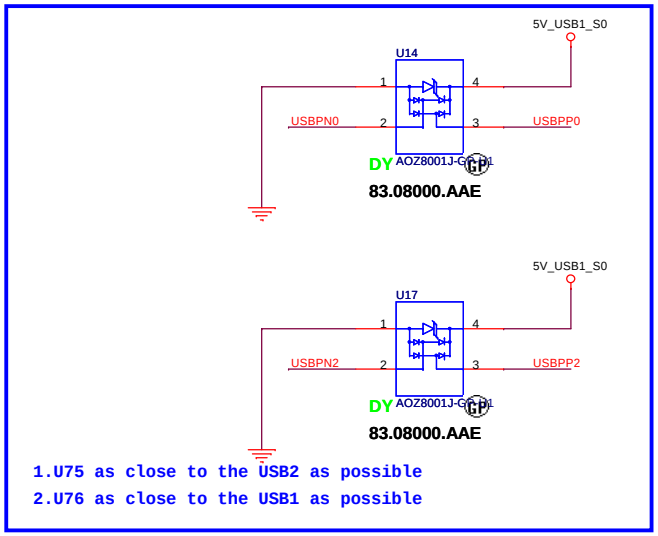












JV50-TR8

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB**		
Size	Document Number: **JV50-TR8**	Rev: **-1**
Date: Monday, October 26, 2009	Sheet 25 of 63	

CO-Layout BCM5764 and BCM5784
modify BOM :71.05784.M03

U4
BCM5784MKMLG-GP
71.05784.M03

U3
AT24C02BN-SH-T-GP
72.24C02.R01
2ND = 72.24C02.M01

82.30020.851
2ND = 82.30020.791

1ST 84.DCP69.01B
2ND = 84.00069.B1B

Place PLLVDD/AVDDL
CKT as close to chip as
possible

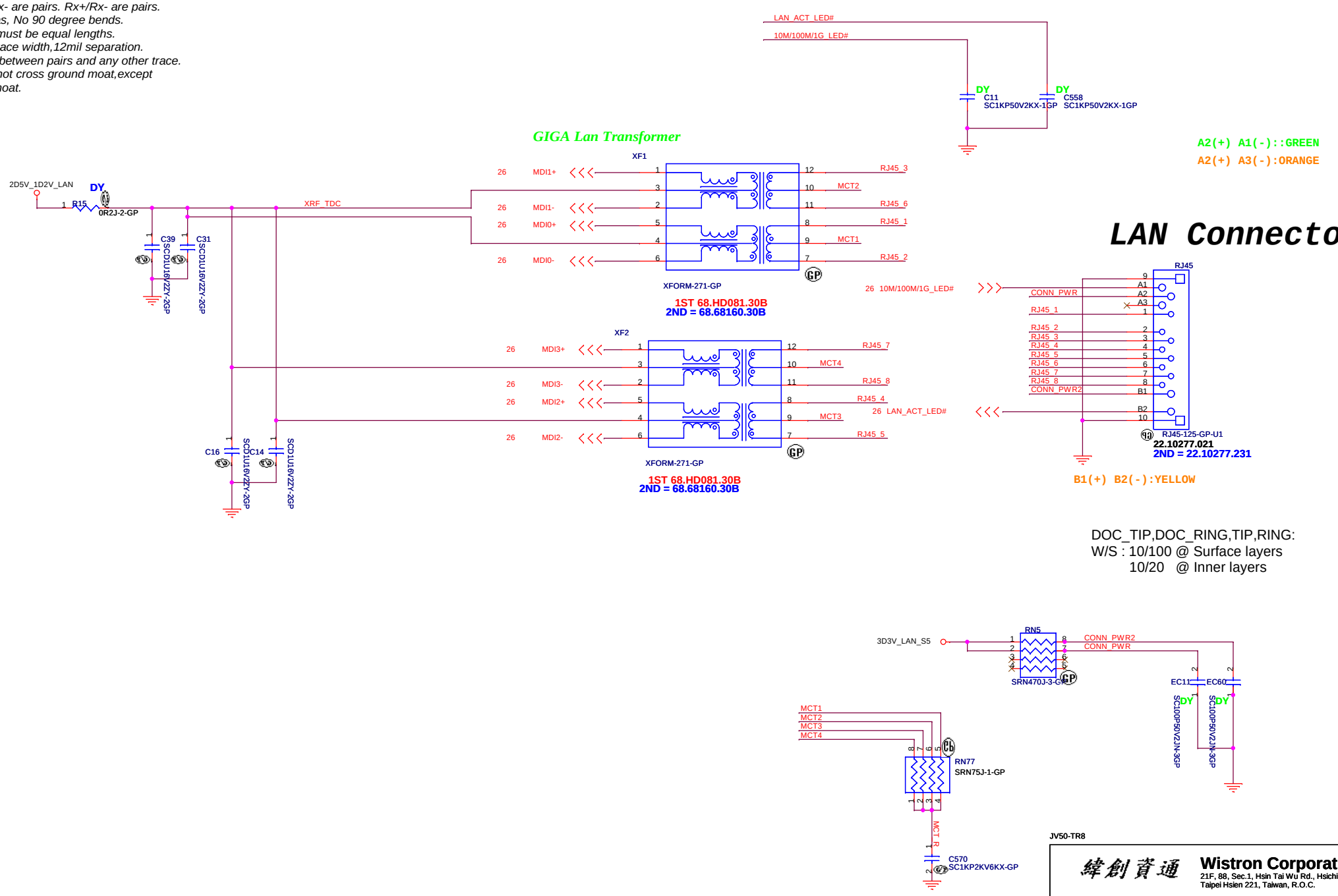
JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BCM5784MKMLG
Size: Custom | Document Number: JV50-TR8 | Rev: -1
Date: Monday, October 26, 2009 | Sheet 26 of 63

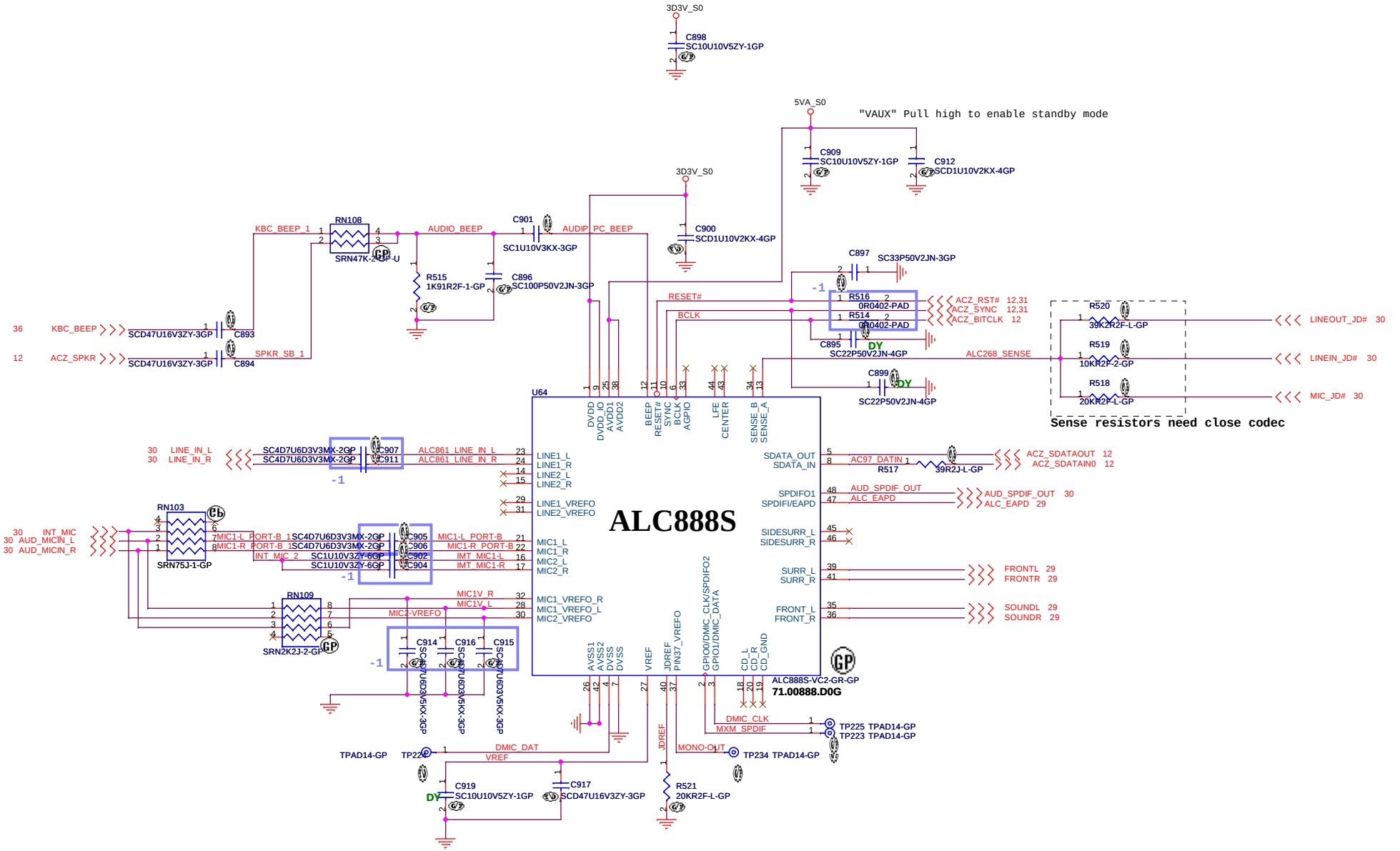
LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.



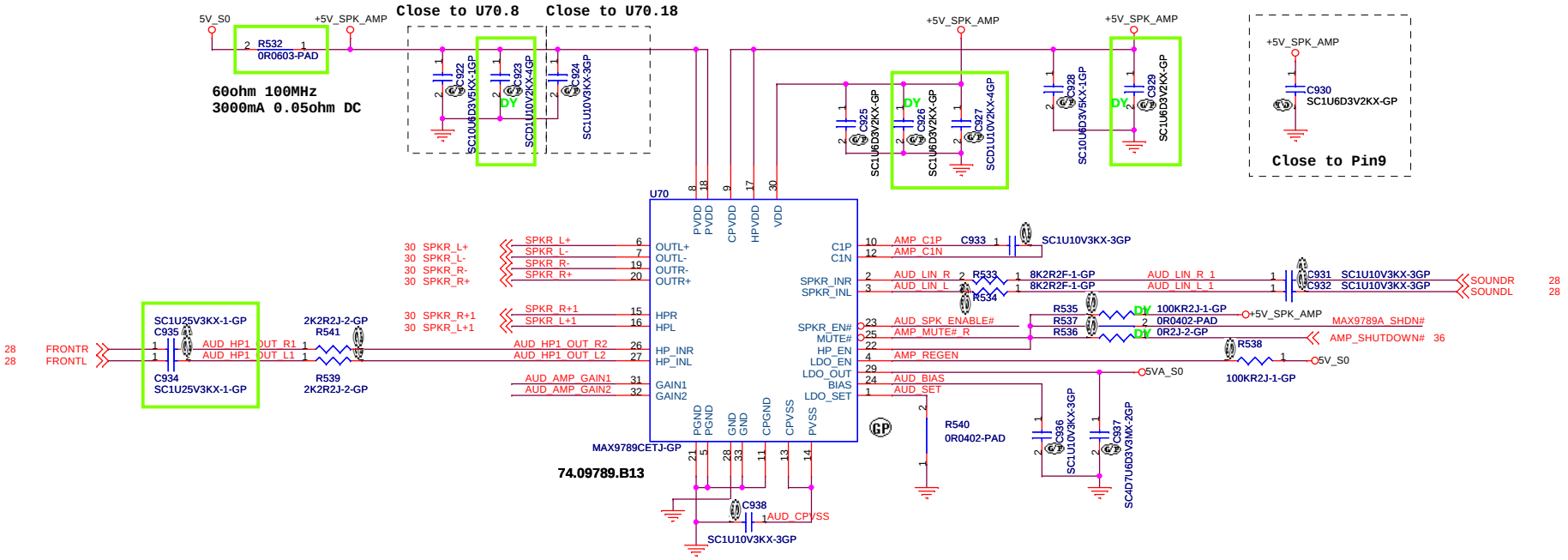
JV50-TR8

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAN CONN		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 27 of 63	

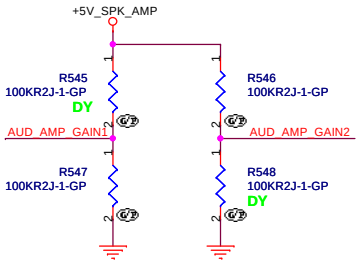


JV50-TR8

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Azalia codec ALC888**	
Size A3	Document Number **JV50-TR8**	Rev **-1**
Date: Monday, October 26, 2009	Sheet 28 of 63	

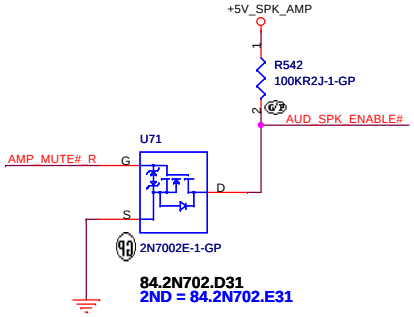


GAIN SETTING

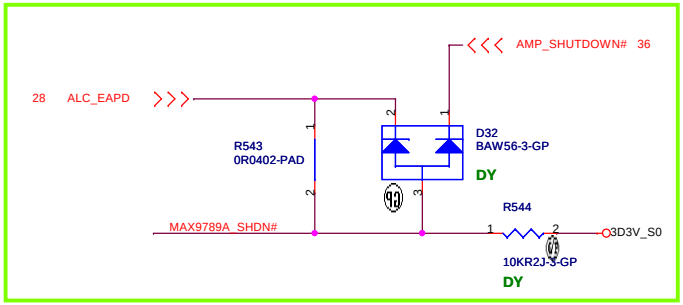


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Signal inverter for speaker shutdown



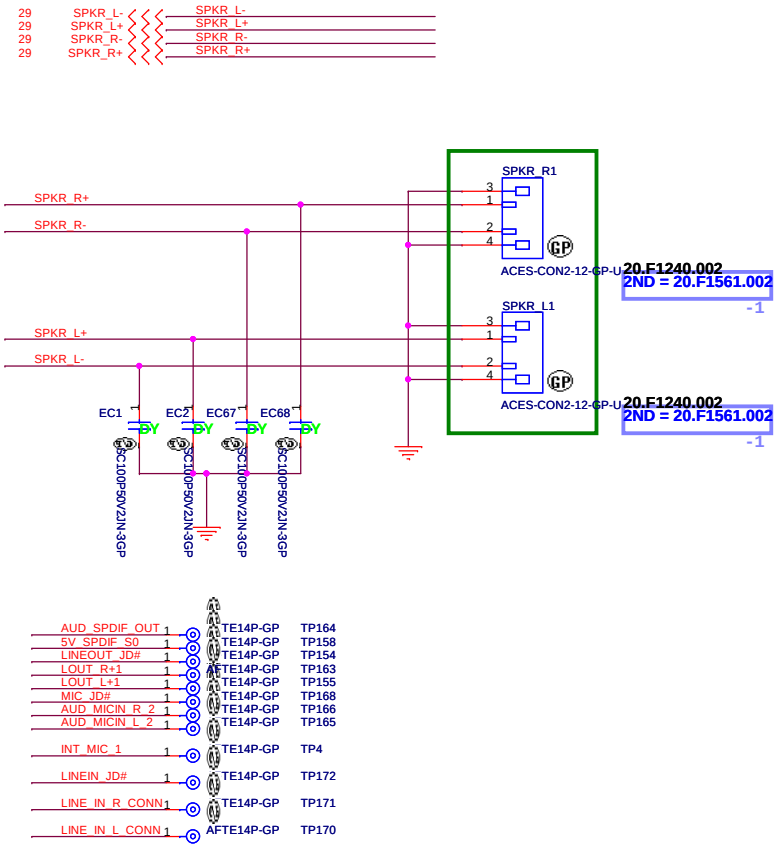
84.2N702.D31
2ND = 84.2N702.E31



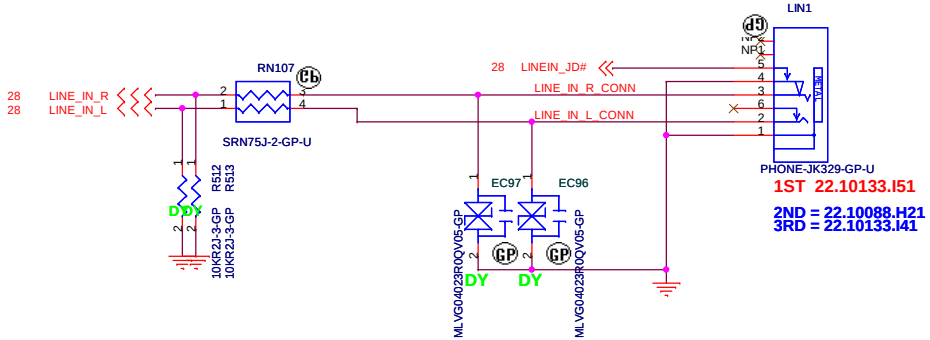
JV50-TR8

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO AMP		
Size	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 29 of 63	

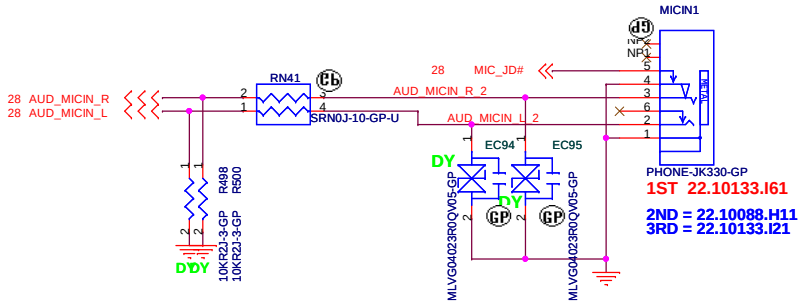
Internal Speaker



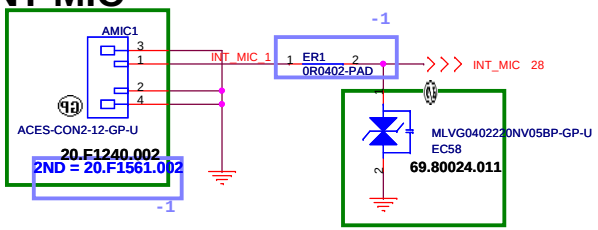
LINE IN



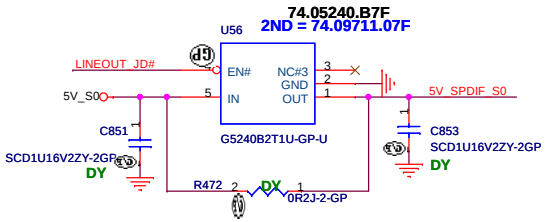
MIC IN

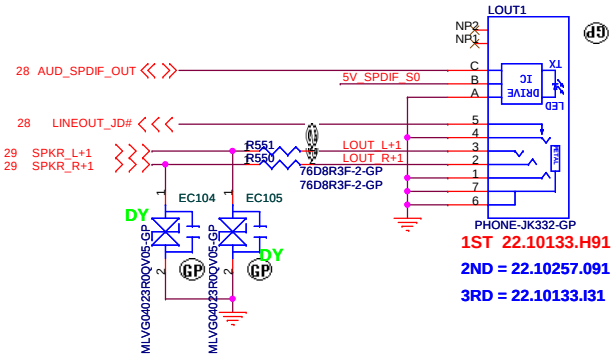


INT MIC



LINE OUT

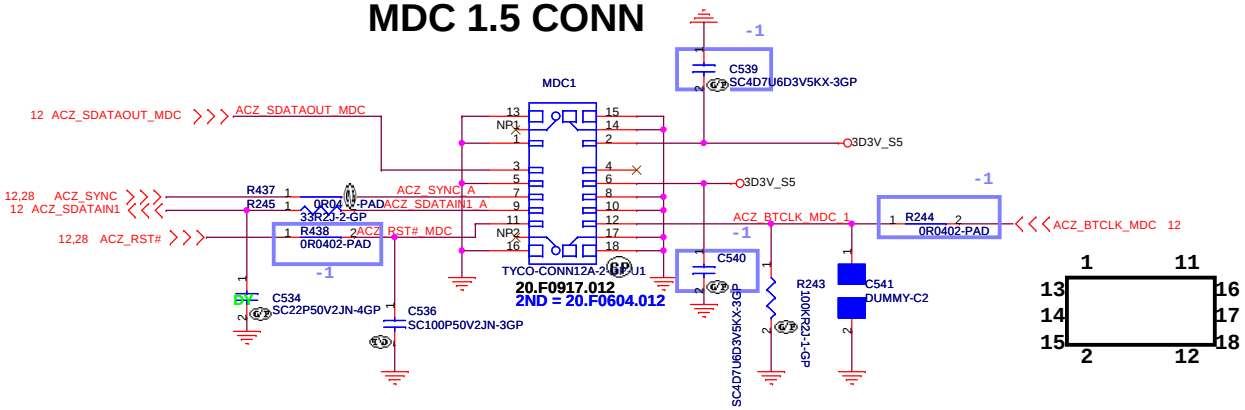




JV50-TR8

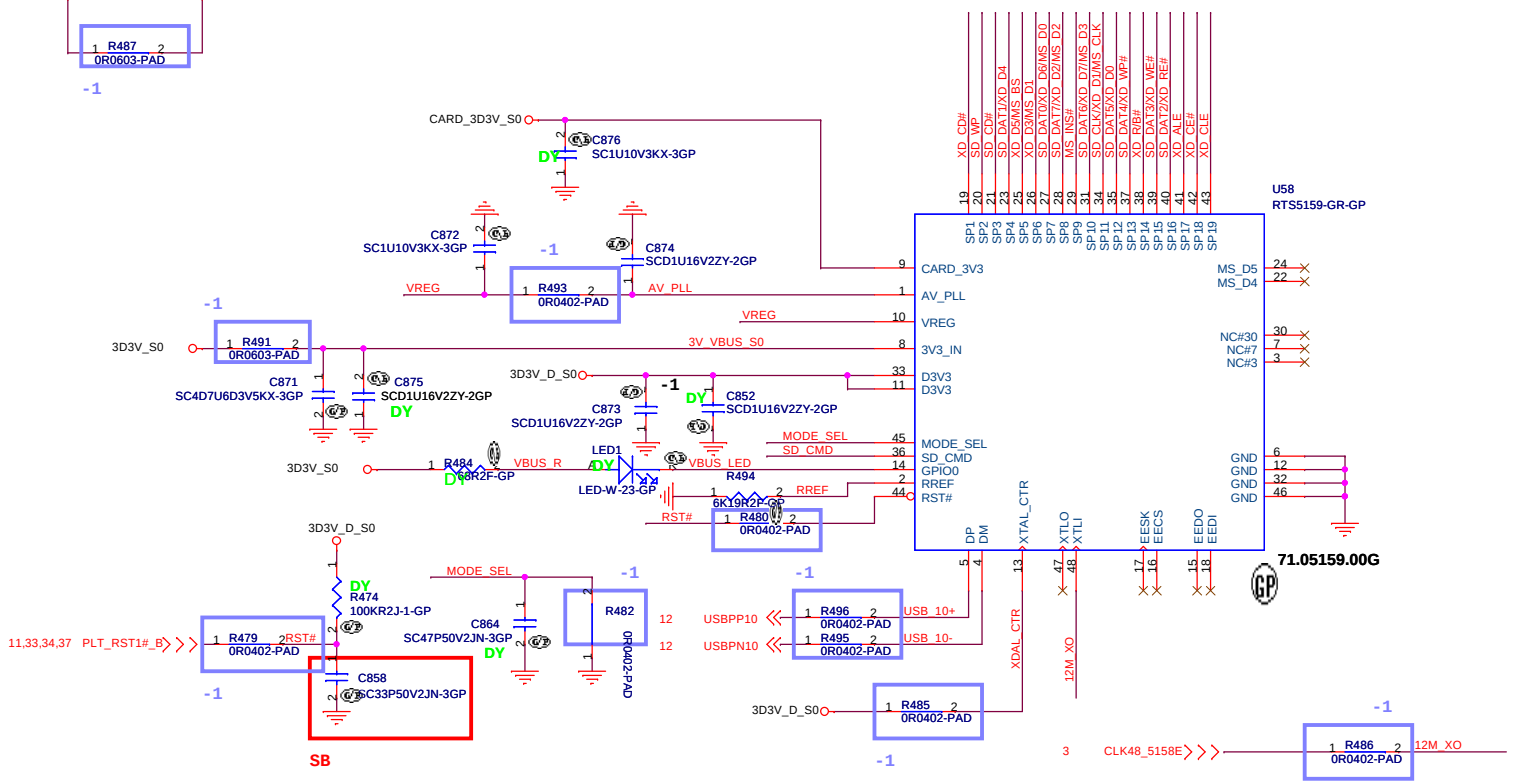
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO JACK		
Size	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 30 of 63	

MDC 1.5 CONN

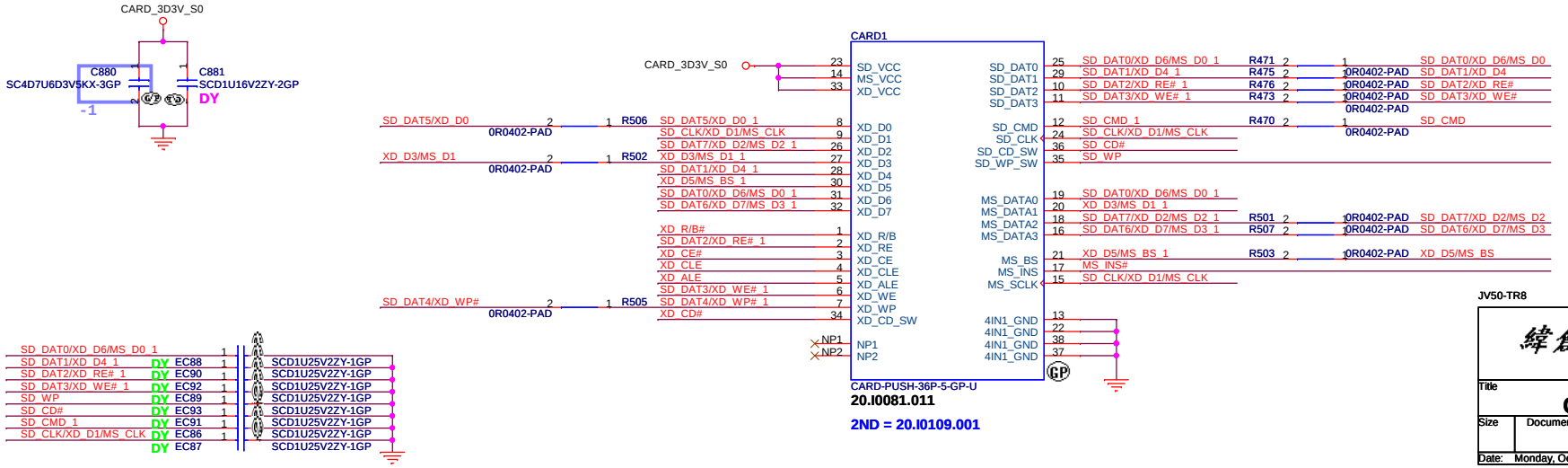


JV50-TR8

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MDC		
Size	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 31 of 63	



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



JV50-TR8

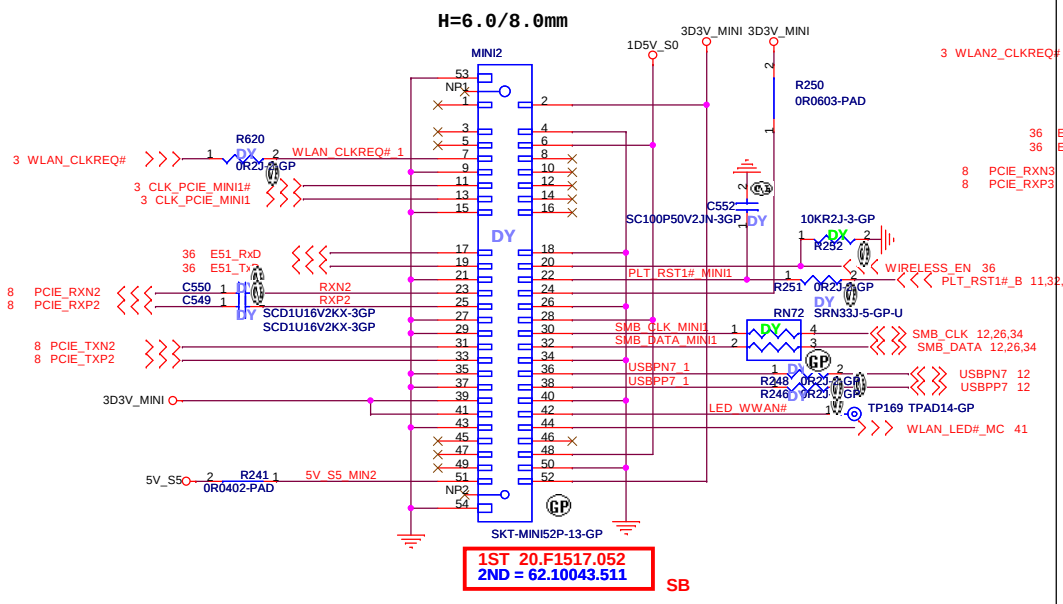
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

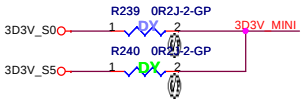
Title: **CARDREADER- RTS5159**

Size	Document Number	Rev
	JV50-TR8	-1

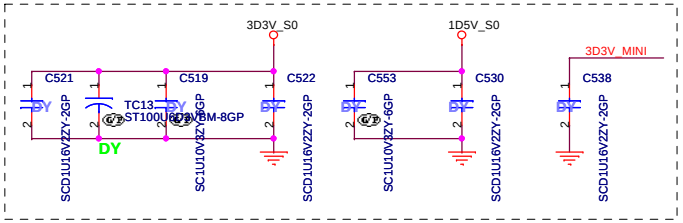
Date: Monday, October 26, 2009 Sheet 32 of 63

Mini Card Connector(WLAN)

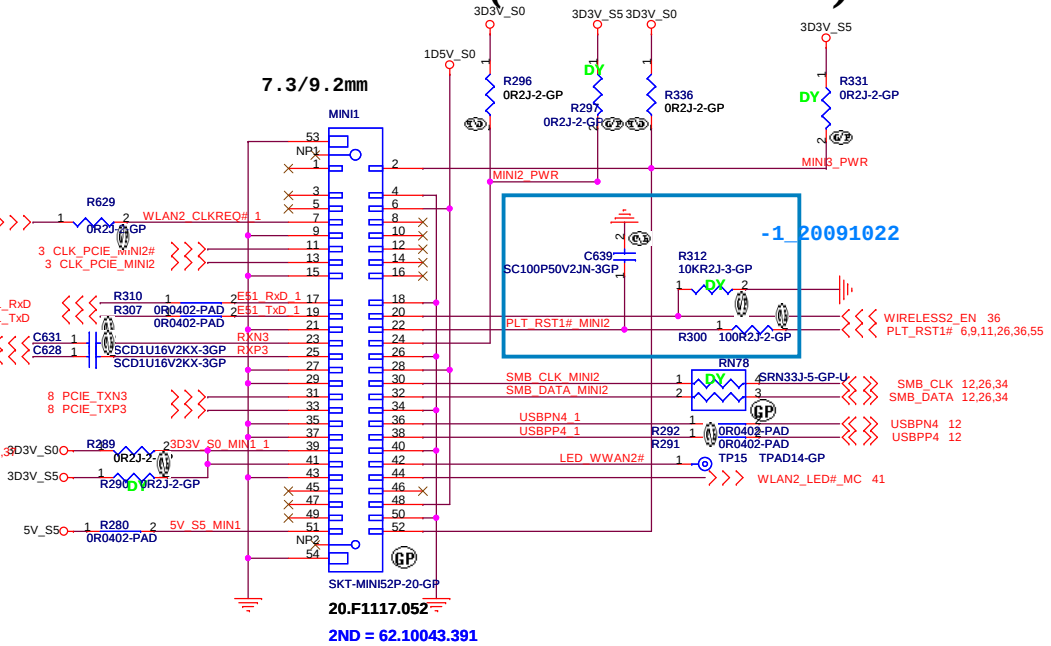




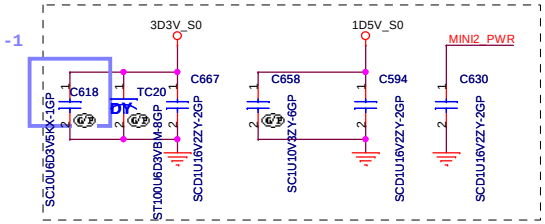
Place near MINI2



Mini Card Connector(Robson2 and 3G)



Place near MINI1

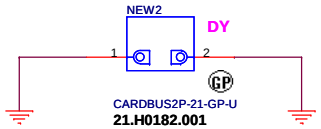


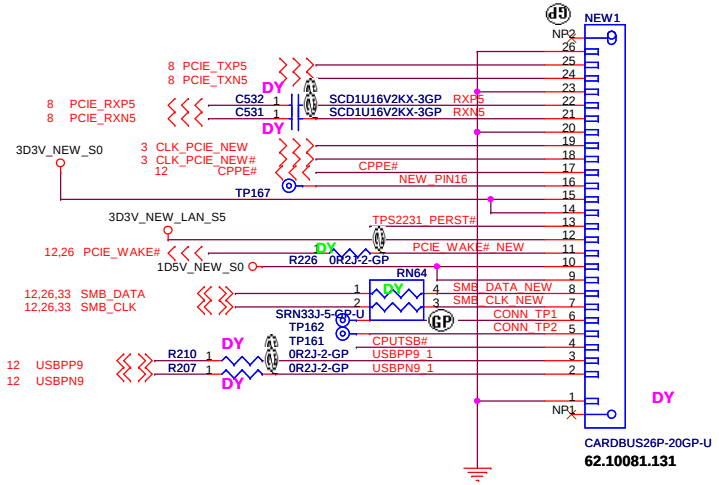
JV50-TR8

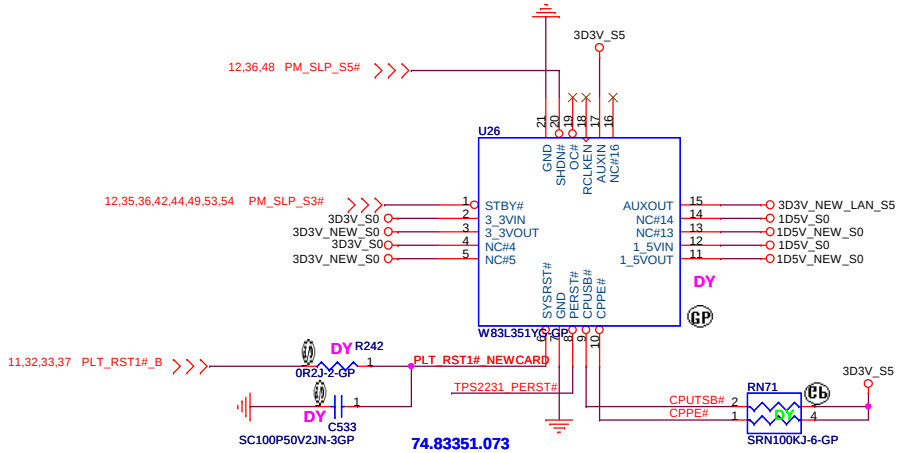
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MINI CARD	
Size	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 33 of 63	

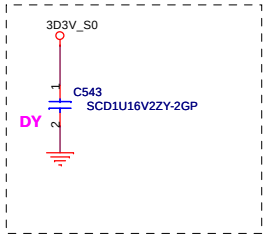
NEWCARD Connector



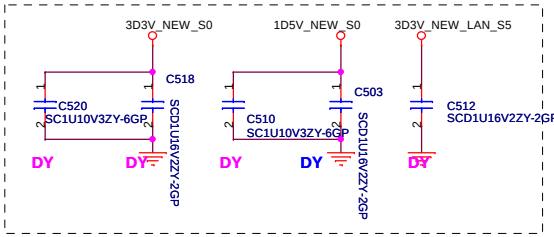




Place them Near to Chip



Place them Near to Connector



JV50-TR8

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: NEW CARD		
Size	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 34 of 63	

Layout 15 mil

C669 SCD1U16V2ZY-2GP DY
C679 SC4D7U6D3V5KX-3GP
FAN1_VCC
D20 BAS16PT-GP
C670 SC2200P50V2KX-2GP DY

83.00016.F11
2ND = 83.00016.B11

5V_S0
R9 10KR2J-3-GP
FAN1_VCC
FAN1_FG1
AFAN1
C18 SC1KP50V2KX-1GP
Layout 15 mil
ACES-CON3-GP-U1
20.F0714.003
2ND = 20.D0246.103

5V_S0
Layout 30 mil
R12 10R2J-2-GP
C24 SC1U10V3ZY-6GP
R11 21KR2F-GP
R10 49K9R2F-L-GP
T8=90

5V_S0
C12 SC4D7U6D3V3MX-2GP
C9 DY
C10 SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP

U2
5V_G792_S0
VCC DVCC
DXP1 DXP2 DXP3
ALERT# THERM# THERM_SET RESET#
DGND DGND
SGND1 SGND2 SGND3
FAN1 FG1 CLK SDA SCL NC#19
G792_32K
SMBD_Therm 36,56
SMBC_Therm 36,56
ALERT#
T8_HW_SHUT#
V_DEGREE
RUNPWROK
G792SFUF-GP
74.00792.A79

3.System Sensor, Put Plamrest.
G792_DXP2
G792_DXP3
G792_DXN2
G792_DXN3
C17
C8
C551 SC470P50V3JN-2GP
Q11 MMBT3904-4-GP
SC2200P50V2KX-2GP
84.T3904.C11
2ND = 84.03904.L06
C702 SC470P50V3JN-2GP
Q23 MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.L06
2.H/W Shutdown
GAP-CLOSE G1
GAP-CLOSE G2
SC2200P50V2KX-2GP
H_THERMDA 6
H_THERMDC 6
1.For CPU Sensor

DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

Place near chip as close as possible

C20 SC2200P50V2KX-2GP

3D3V_S5
U16B
12,34,36,42,44,49,53,54 PM_SLP_S3#
11,15 RTC_CLK
32KHZ
R7 10R2J-2-GP
G792_32K
TSLVC08APW-1-GP
32K suspend clock output

73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B

BL3#

HW Thermal Throttling

5V_AUX_S5
C656 SCD1U16V2ZY-2GP DY
U43
VCC DY RESET#/RESET
HTH GND LTH
G680LT1UF-GP
DCBATOUT
R330 1MR2F-GP DY
R338 6K04R2F-GP DY
R337 174KR2F-GP DY
HTH
LTH
T8_HW_SHUT#
LOW3_OFF

3D3V_AUX_S5
-1
R322 0R0402-PAD
D18 BAW56-7-F-GP DY
R311 10KR2J-3-GP
D17 BAT54-4-GP DY
C646 SCD1U16V2ZY-2GP

RSMRST# 6,36
36,52 S5_ENABLE
U39
A B GND DY VCC Y
NC7S08M5X-NL-GP
3D3V_AUX_S5
S5PWR_ENABLE 46
R298 1KR2J-1-GP

6,36 RSMRST#
D34
3V5V_ENABLE 46
KBC_THERMTRIP# 36
BAT54C-7-F-GP
1ST 83.R2003.E81
2ND = 83.BAT54.081
3RD = 83.00054.X81

HW thermal shut down tempature setting 95 degree . Put Near SB.

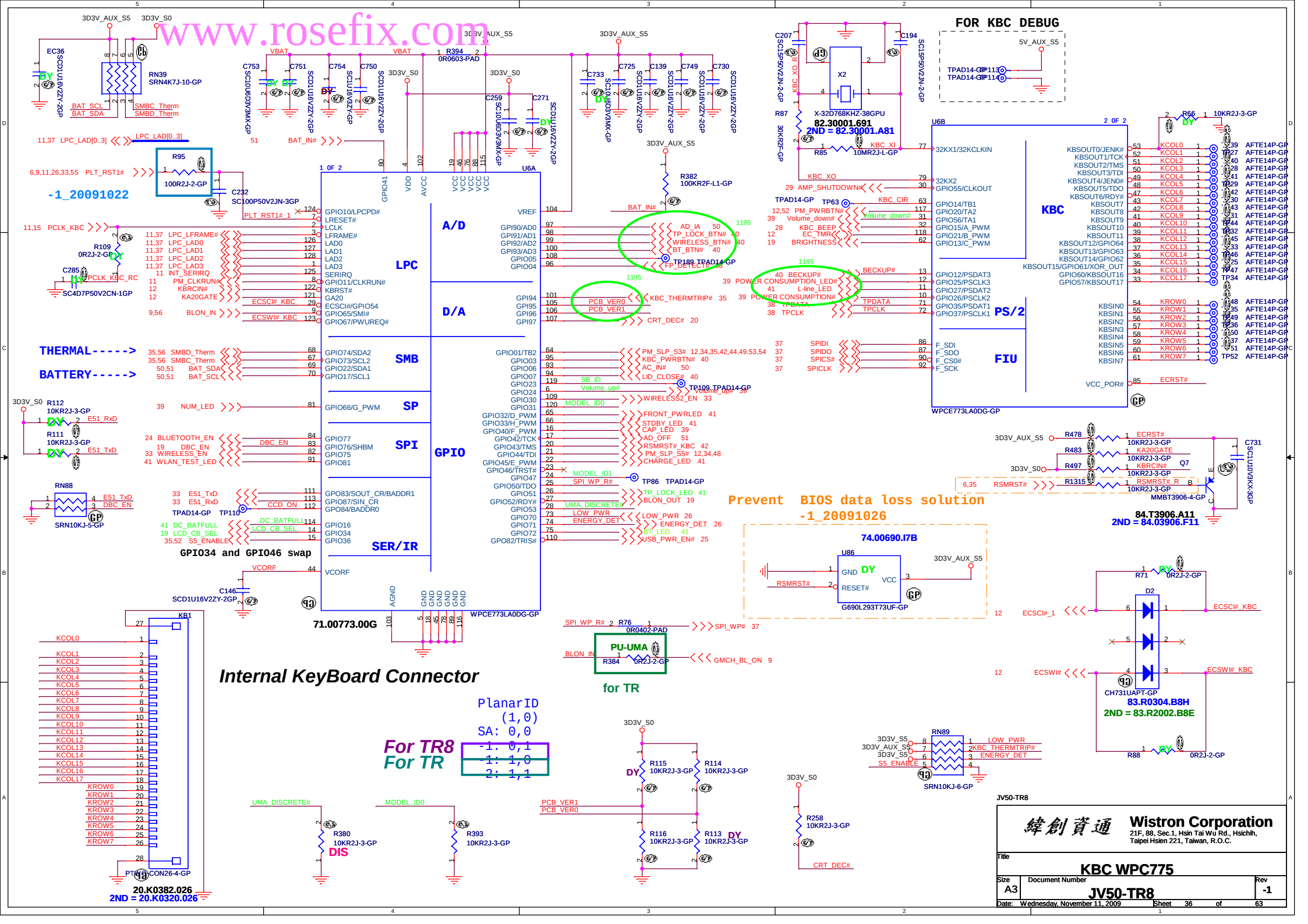
5V_AUX_S5
R308 150R2J-L1-GP-U
C645 SCD01U16V2KX-3GP DY
R321 DY
SB_THSET
18KR2F-GP
T8_HW_SHUT#
U38
SET GND OUT# DY VCC HYST
G709_VCC
SB_TH_HYST
G709T1UF-GP
R309 0R2J-2-GP DY
R314 0R2J-2-GP DY

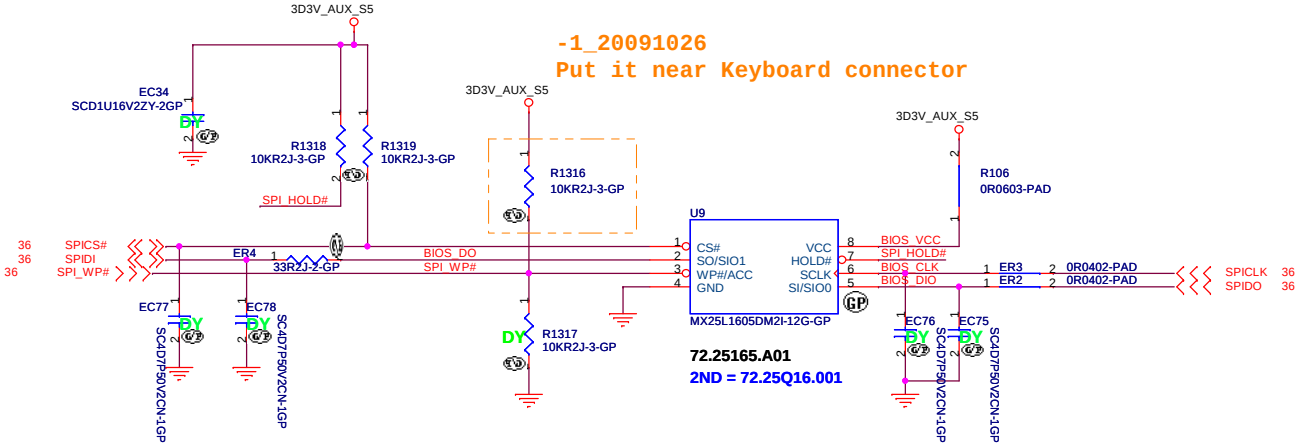
OUT#: Hi active / mount R1110
Low active / mount R1108

JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

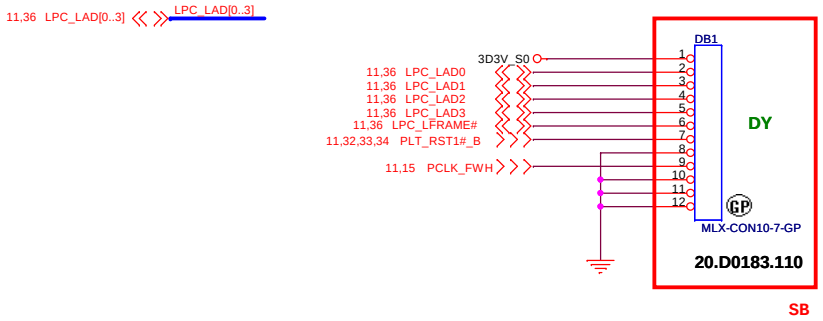
Title: G792
Size: A3
Document Number: JV50-TR8
Rev: -1
Date: Monday, October 26, 2009
Sheet 35 of 63





16M Bits
SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD

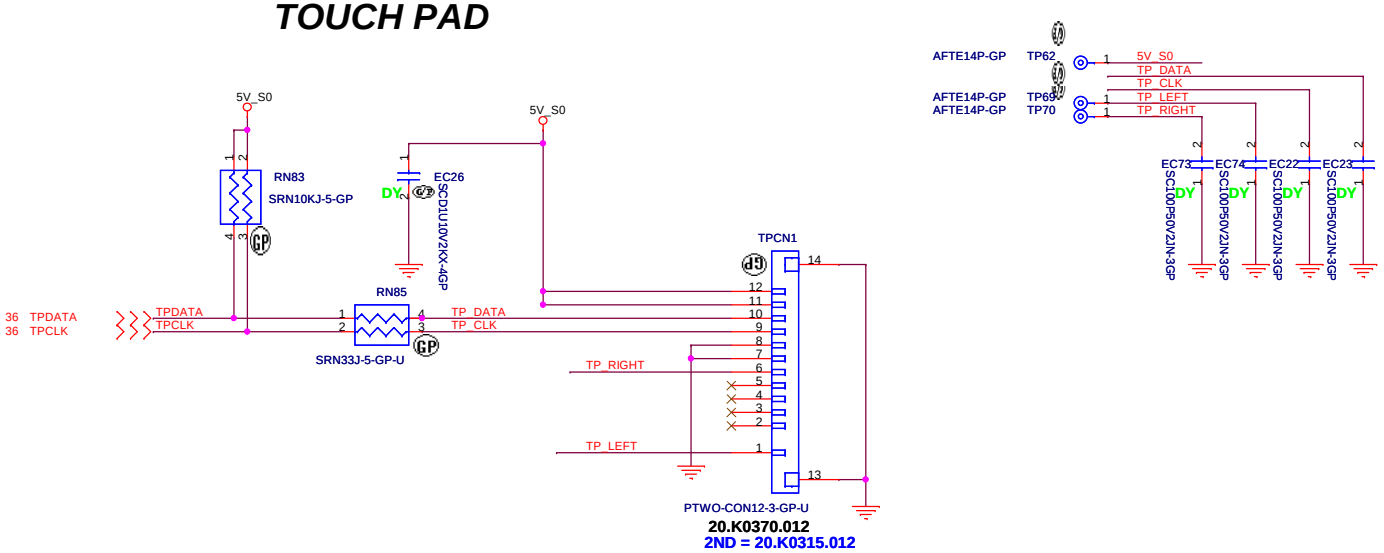


JV50-TR8

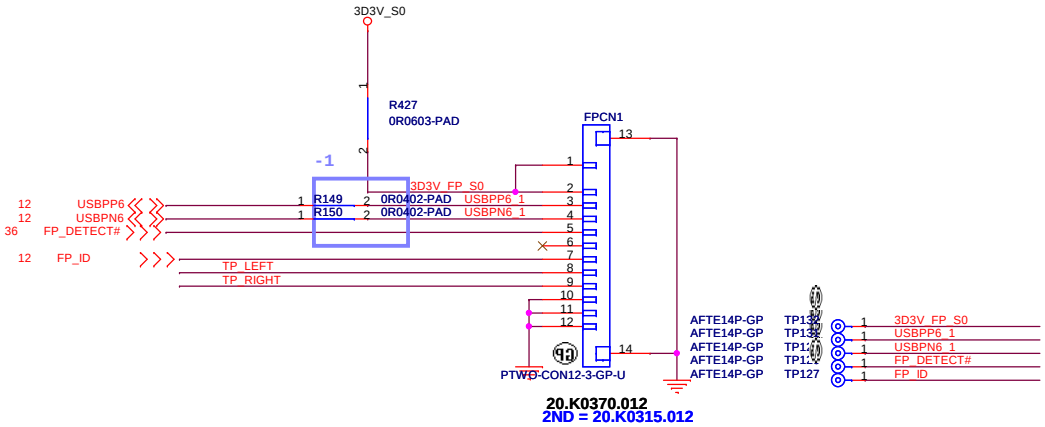
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BIOS		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Wednesday, November 11, 2009	Sheet 37 of 63	

TOUCH PAD



Finger printer



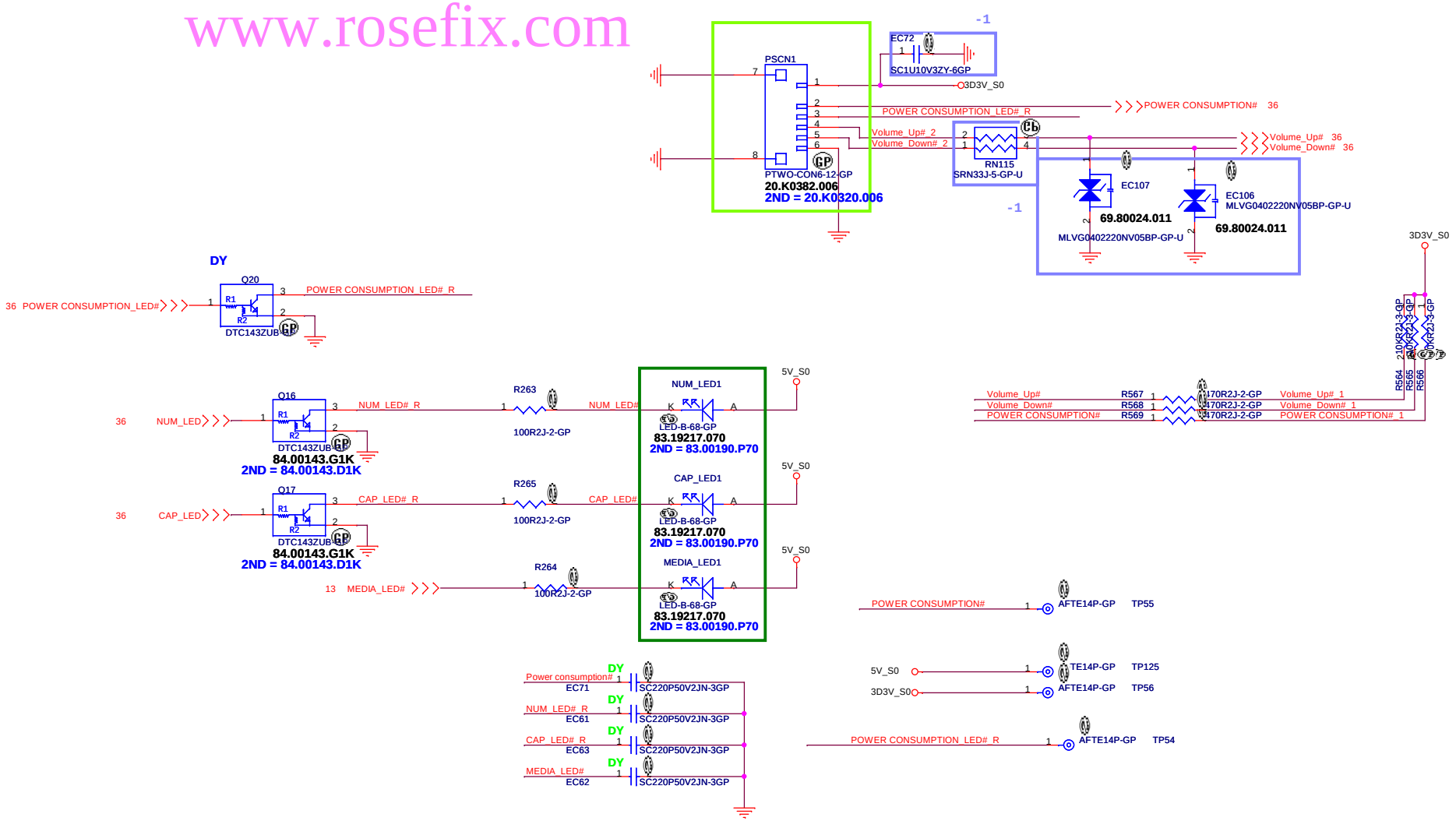
JV50-TR8

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Touch PAD/Finger printer**

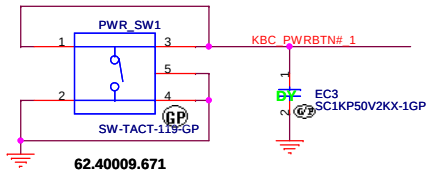
Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 26, 2009 Sheet 38 of 63

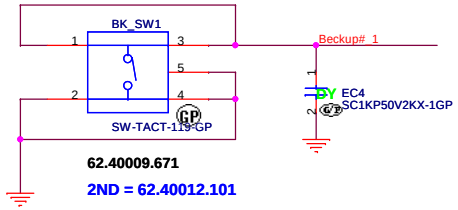


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LAUNCH BOARD**	
Size: A3	Document Number: **JV50-TR8**	Rev: -1
Date: Monday, October 26, 2009	Sheet 39 of 63	

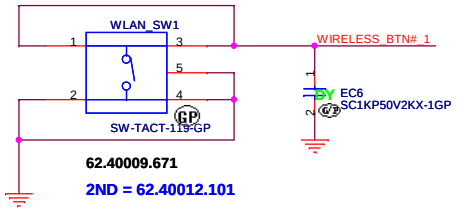
Power Button



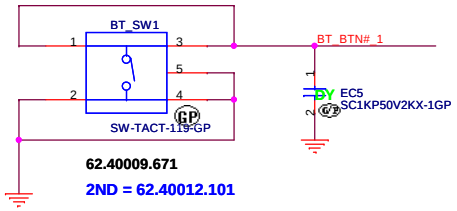
Beckup Button



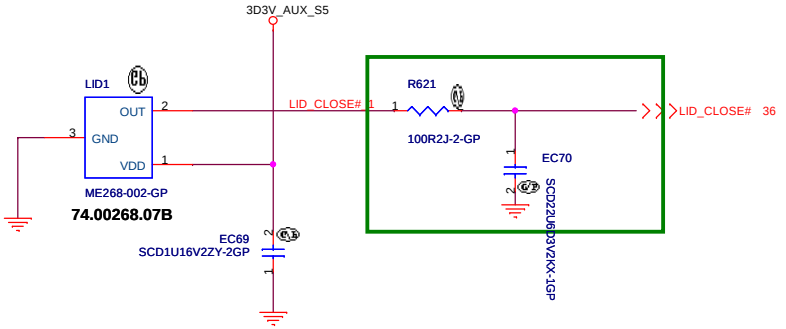
WIRELESS Button

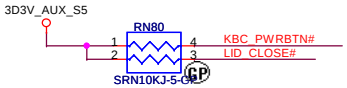


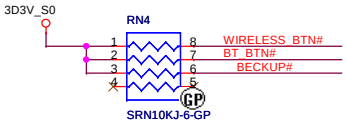
BT/3G Button

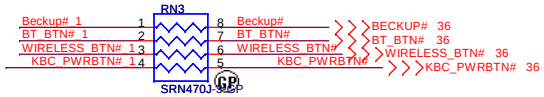


Cover Up Switch

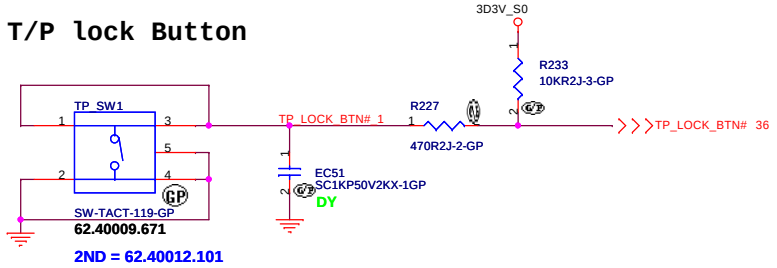






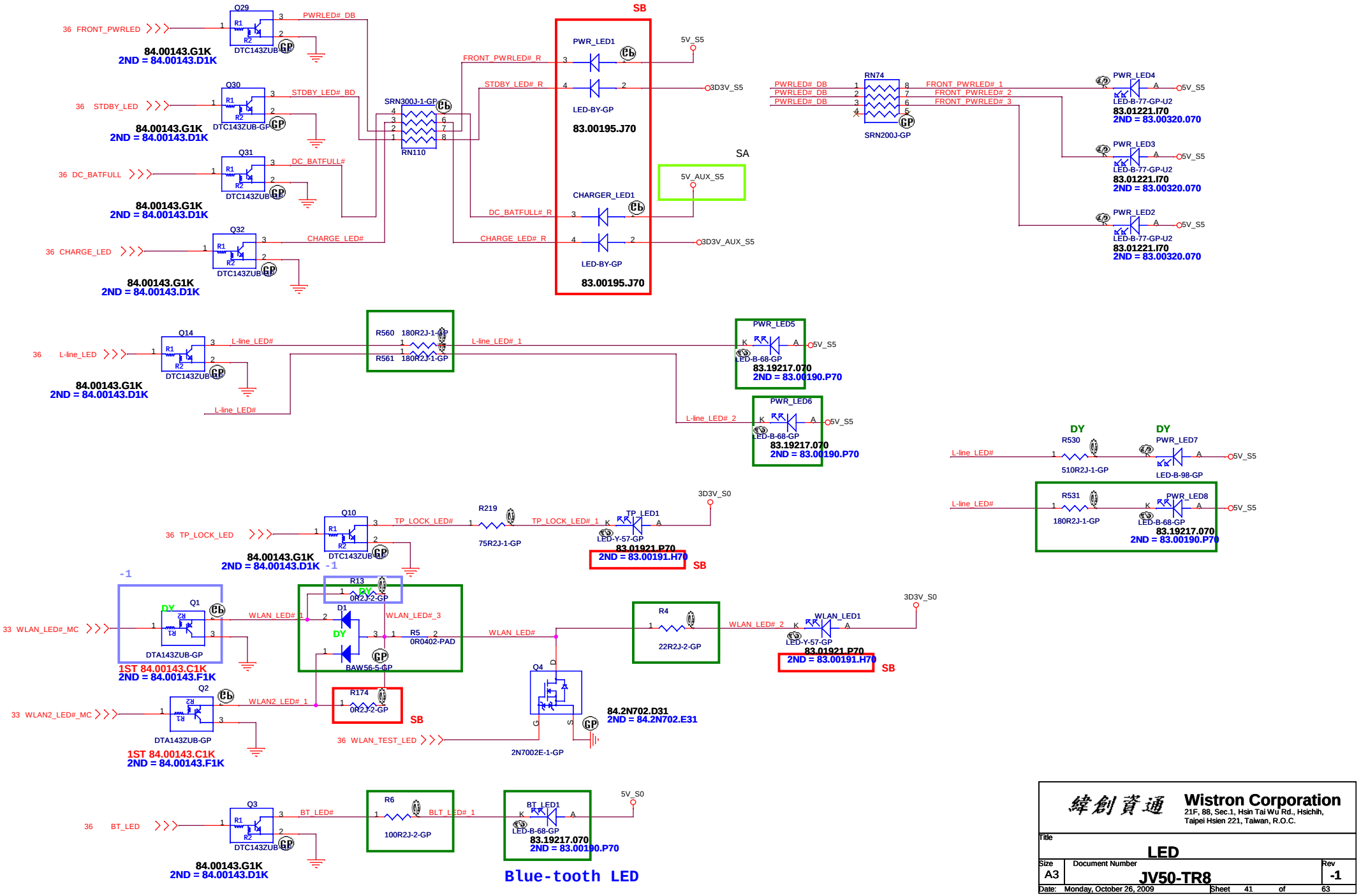


T/P lock Button

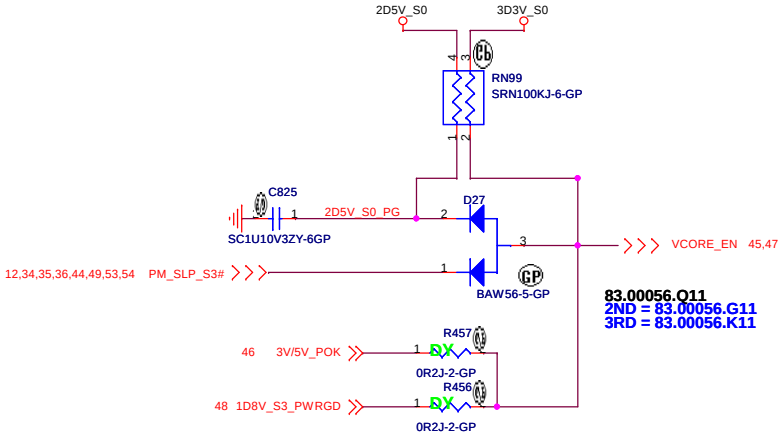


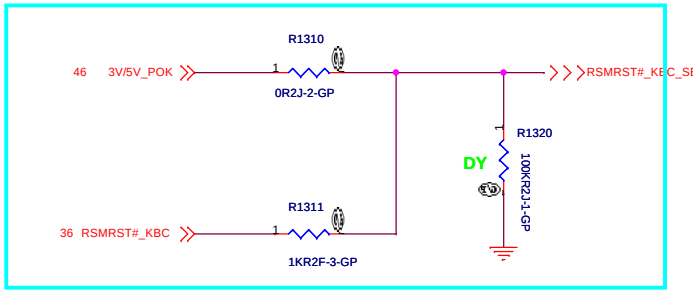
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
SWITCH		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 40 of 63	



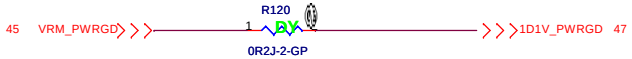
緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LED	
Size A3	Document Number JV50-TR8	Rev -1
Date: Monday, October 26, 2009	Sheet 41 of 63	

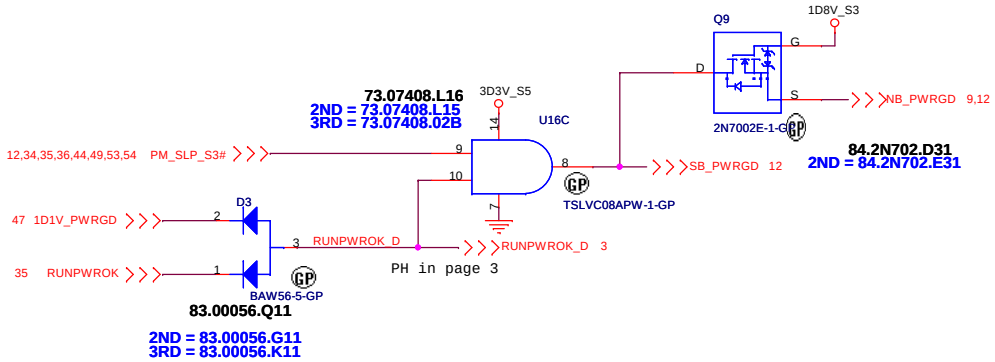




-1_20091026

P/H @ 1D8V_S3 PAGE





JV50-TR8

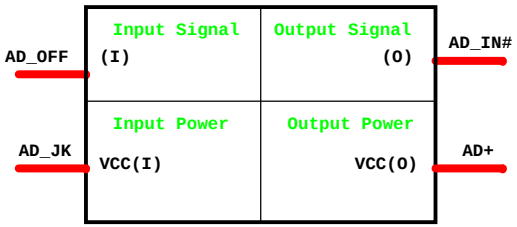
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER ON LOGIC

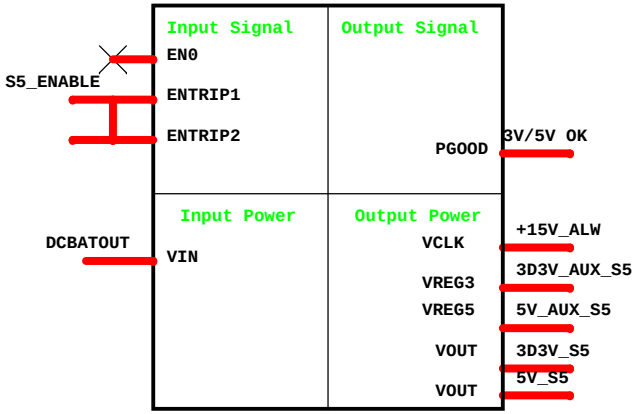
Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Wednesday, November 11, 2009 Sheet 42 of 63

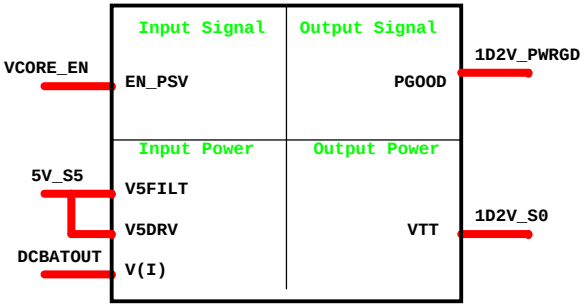
Adapter



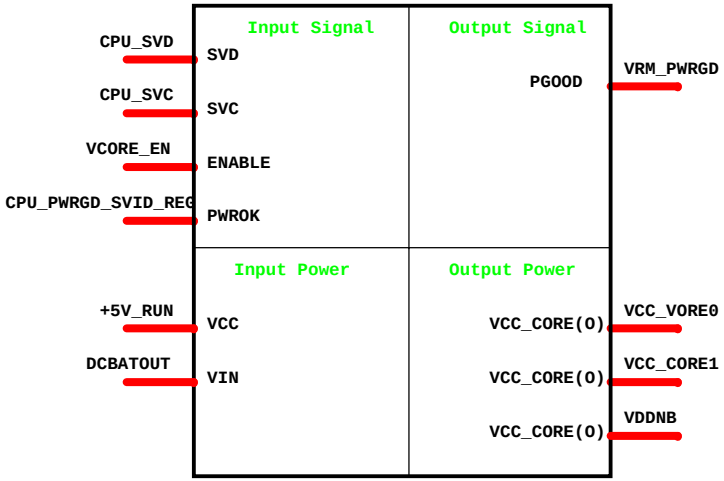
DCDC 5V/3D3V(RT8205A)



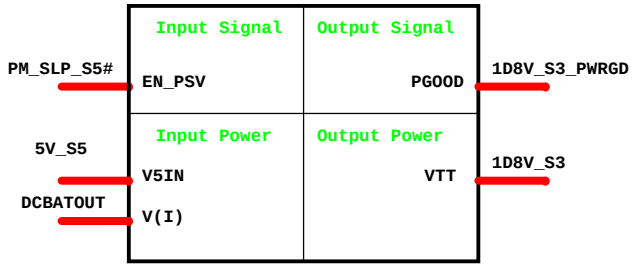
DCDC 1D2V(TPS51124)



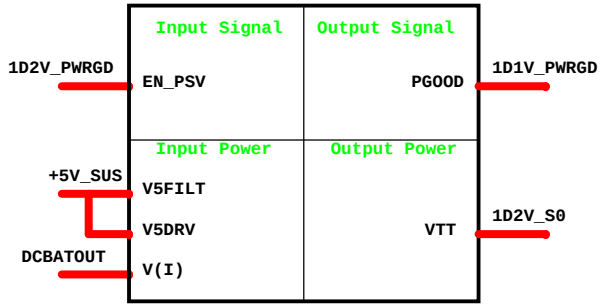
CPU_CORE
ISL6265HRTZ



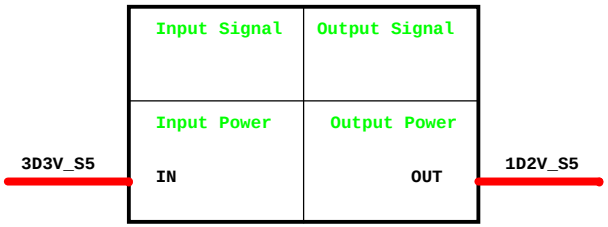
DCDC 1D8V(RT8209B)



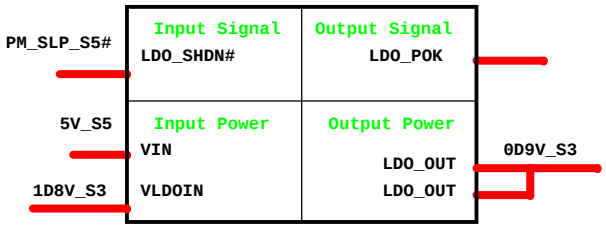
DCDC 1D1V(TPS51124)



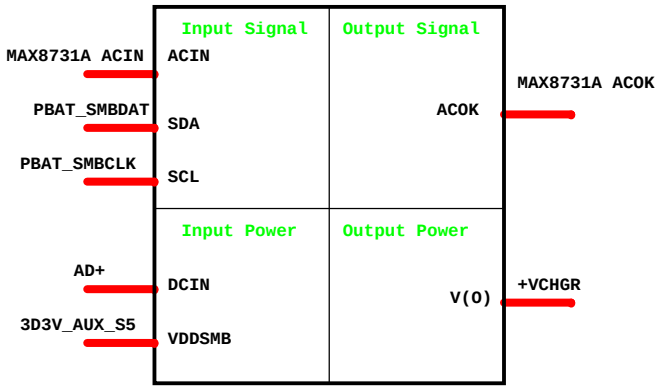
1D2V LDO G9161



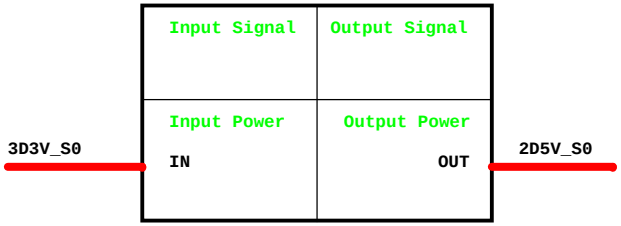
0D9V LDO RT9026



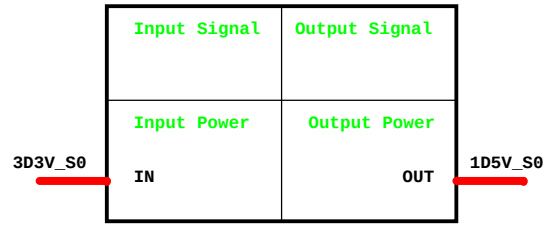
CHARGER MAX8731



2D5V LDO R9161



1D5V LDO G9571



JV50-TR8

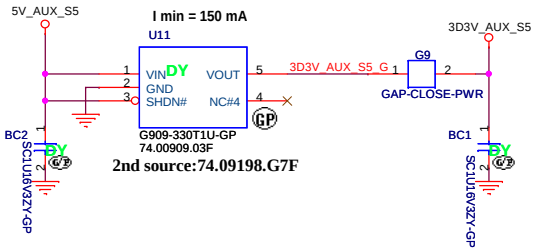
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

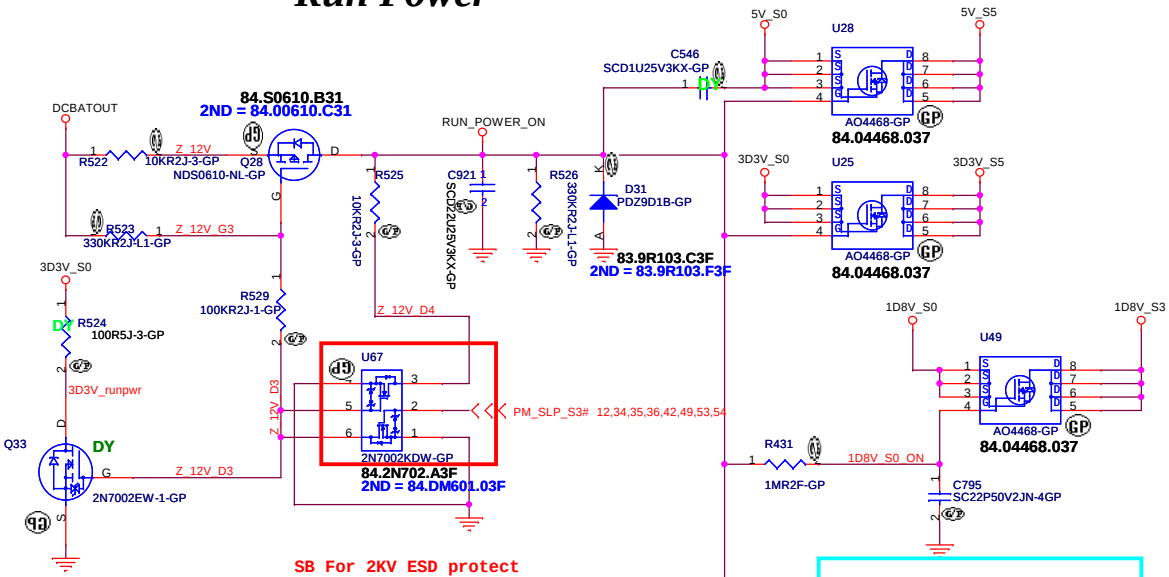
Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 05, 2009 Sheet 43 of 63

Aux Power 3D3V_AUX_S5



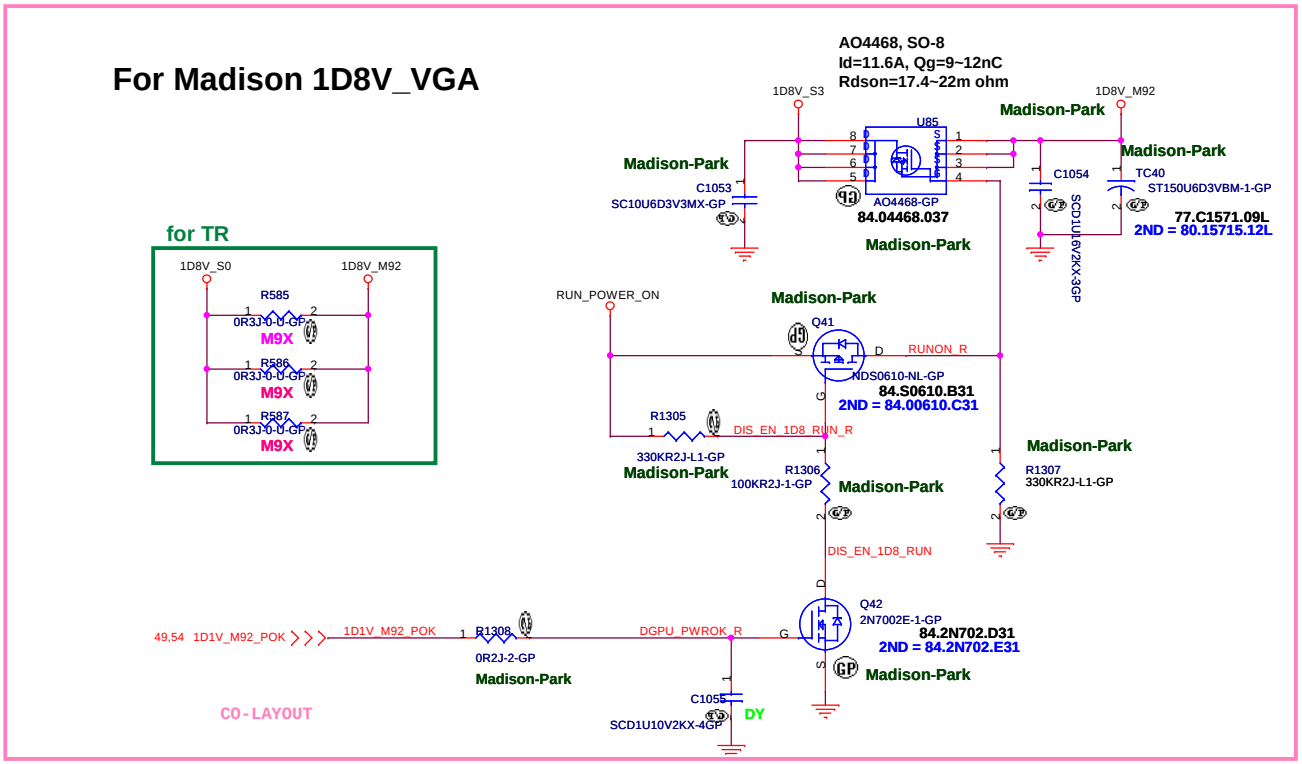
Run Power



SB For 2KV ESD protect

-1_20091023

For Madison 1D8V_VGA



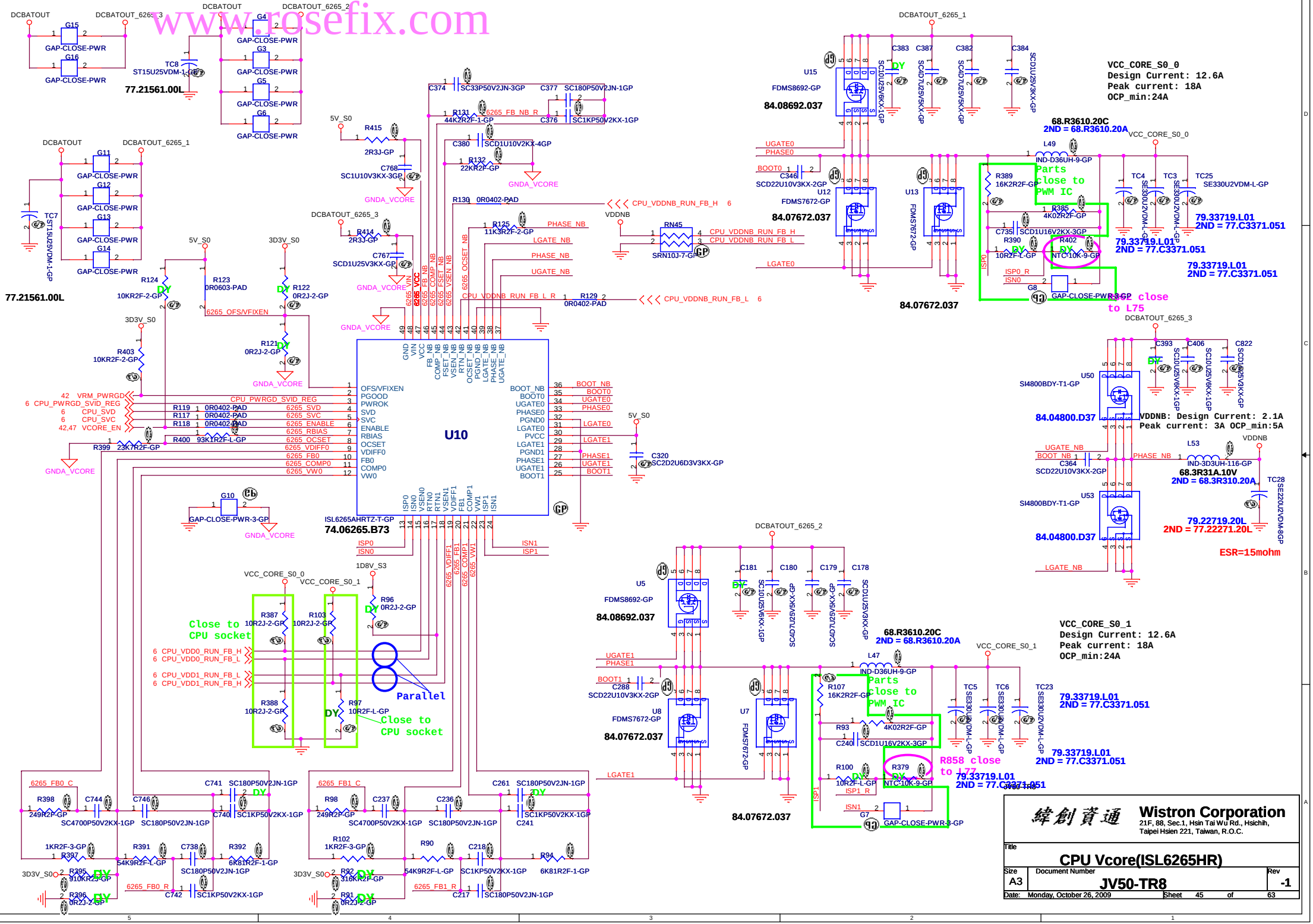
JV50-TR8

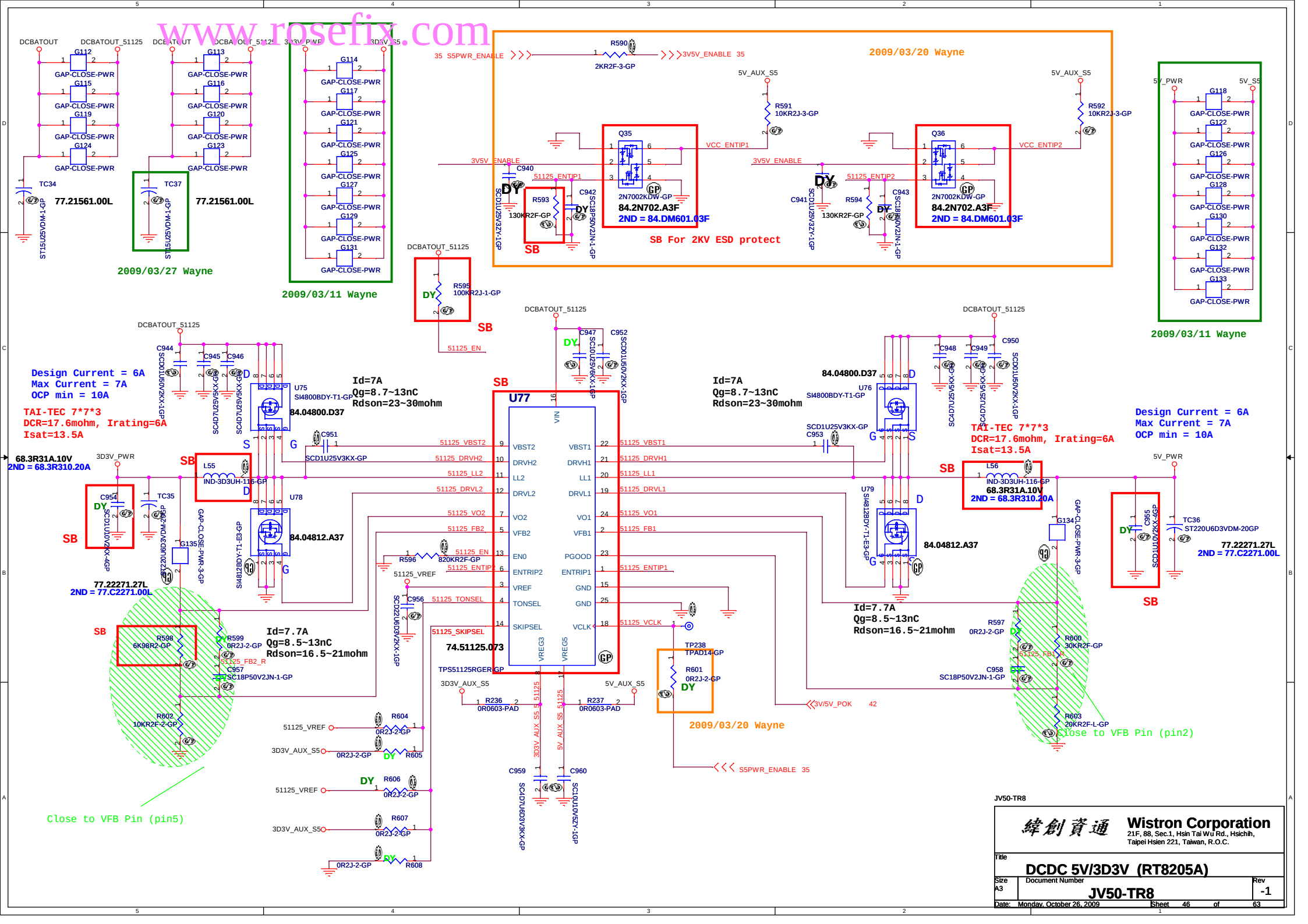
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

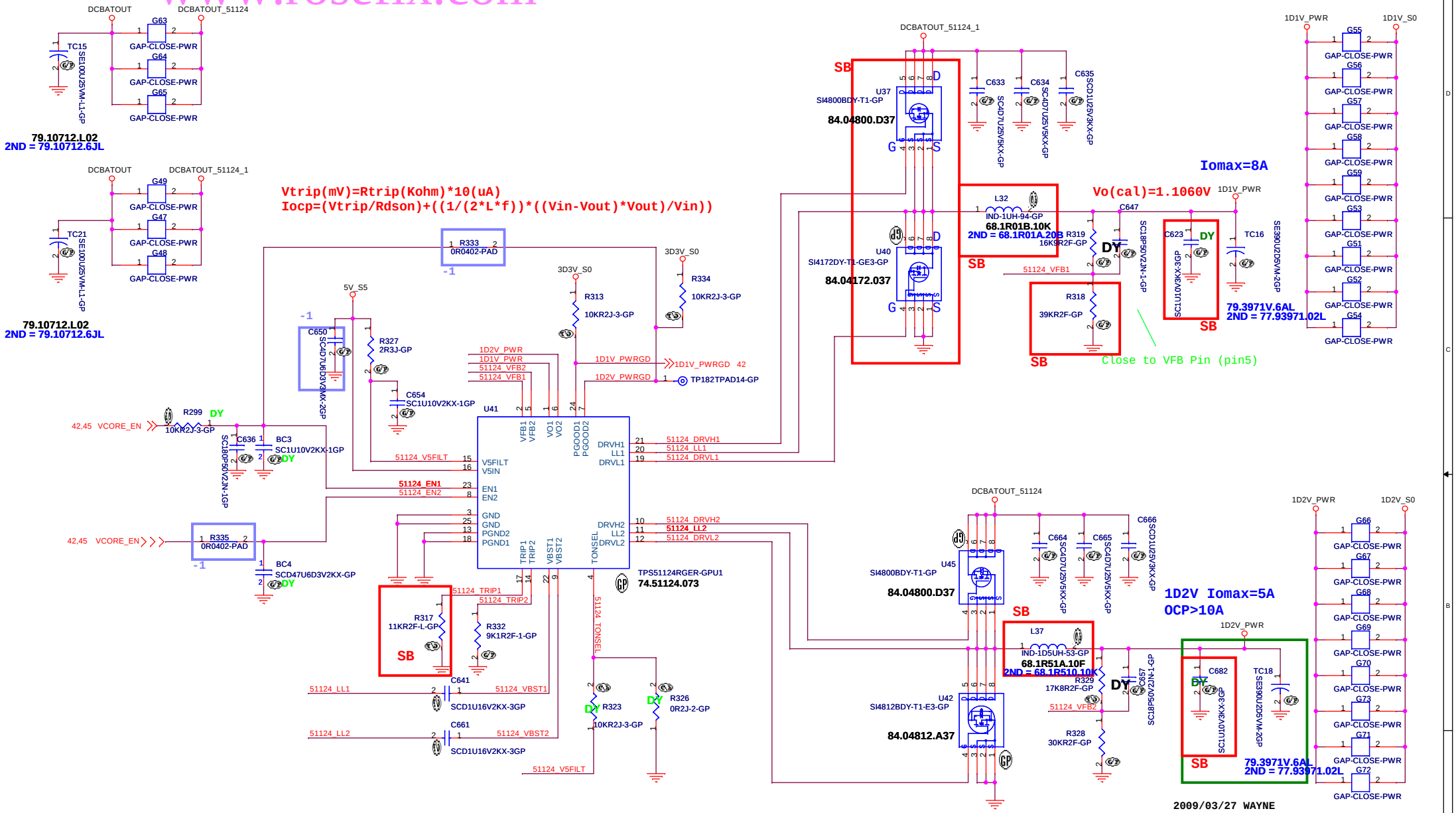
Title: RUN AND AUX POWER

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Wednesday, November 11, 2009 Sheet 44 of 63







	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

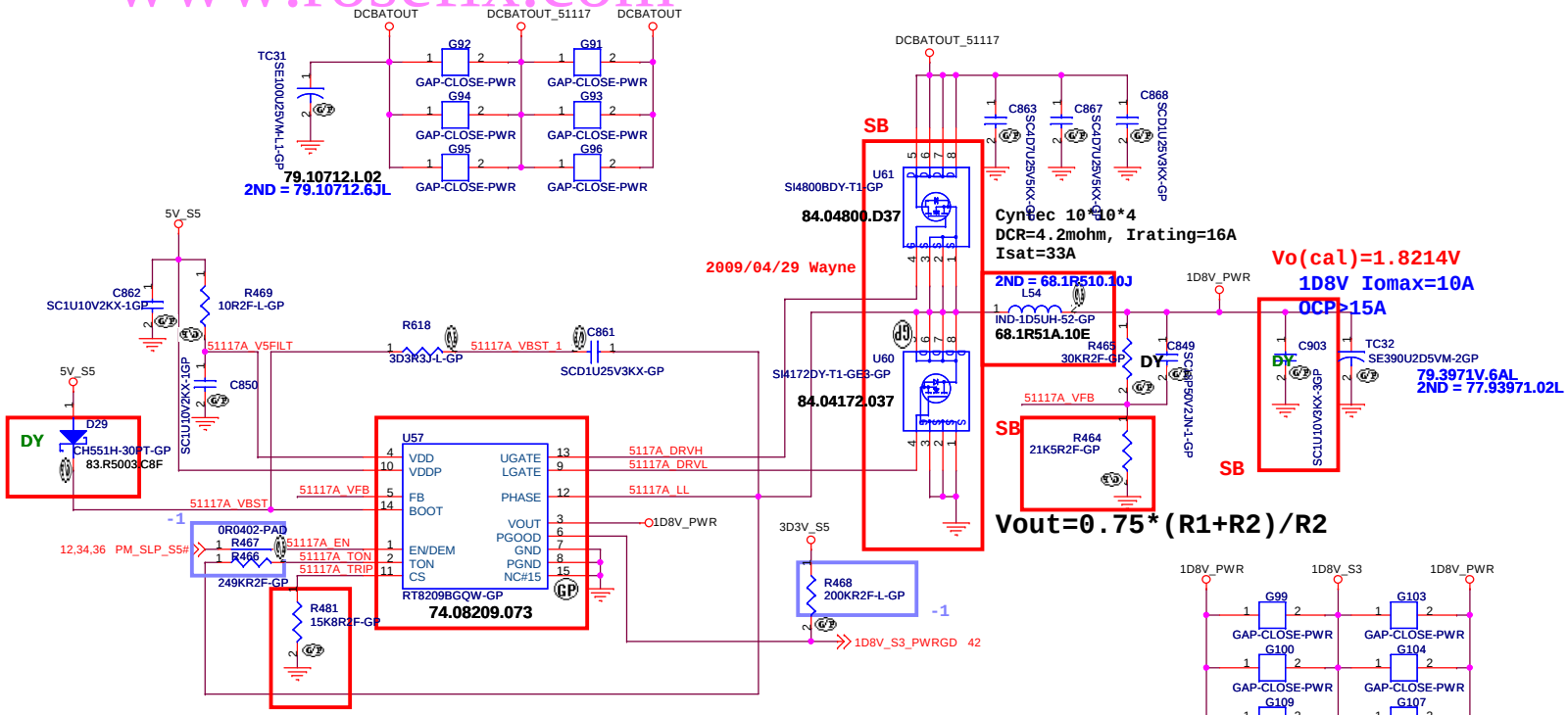
JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D1V_1D2V

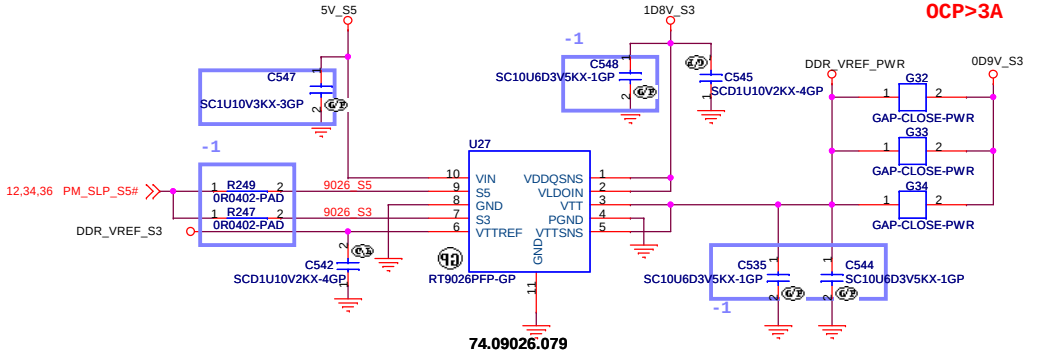
Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 26, 2009 Sheet 47 of 63



DDR_0.9V

Iomax=1.5A
OCP>3A

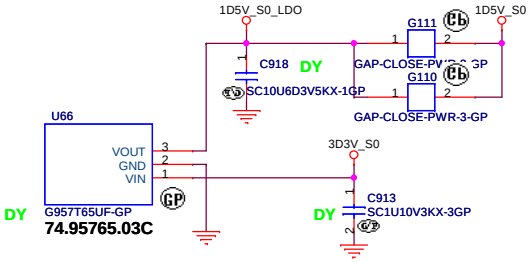


JV50-TR8

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DCDC_1D8V_RT8209B/LDO 0D9V
Size: A3	Document Number: JV50-TR8 — Rev: -1
Date: Monday, October 26, 2009	Sheet 48 of 63

G957

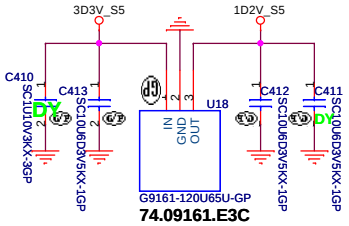
1D5V_S0
Iomax=1A



For MINI Card.NEW Card power SW

G9161

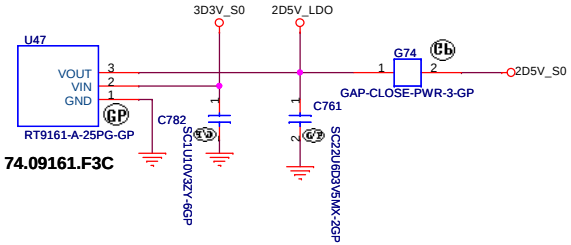
1D2V_S5
Iomax=400mA



Place near to SB710

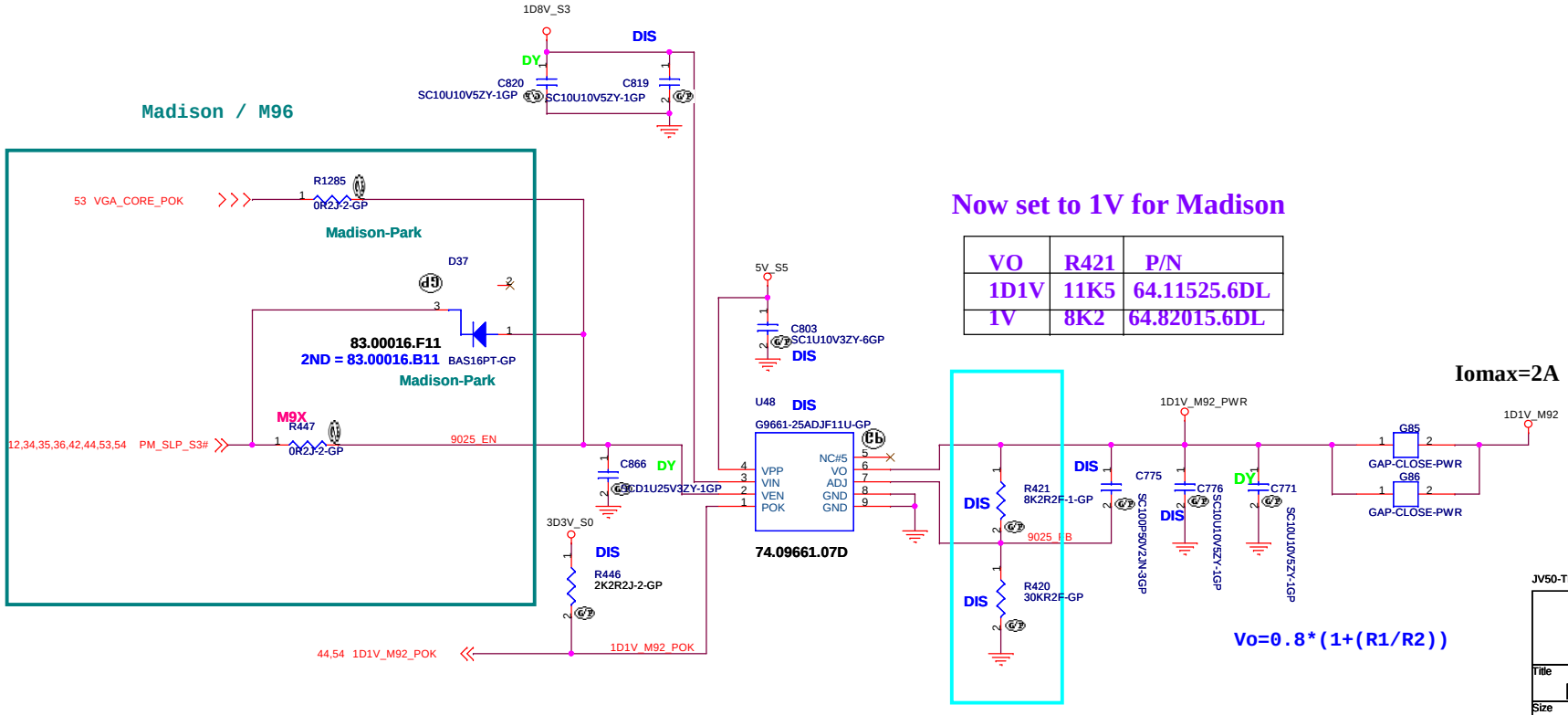
RT9161A

2D5V
Iomax=0.2A



Place near to CPU

Madison / M96



Now set to 1V for Madison

VO	R421	P/N
1D1V	11K5	64.11525.6DL
1V	8K2	64.82015.6DL

Iomax=2A

Vo=0.8*(1+(R1/R2))

-1_20091019

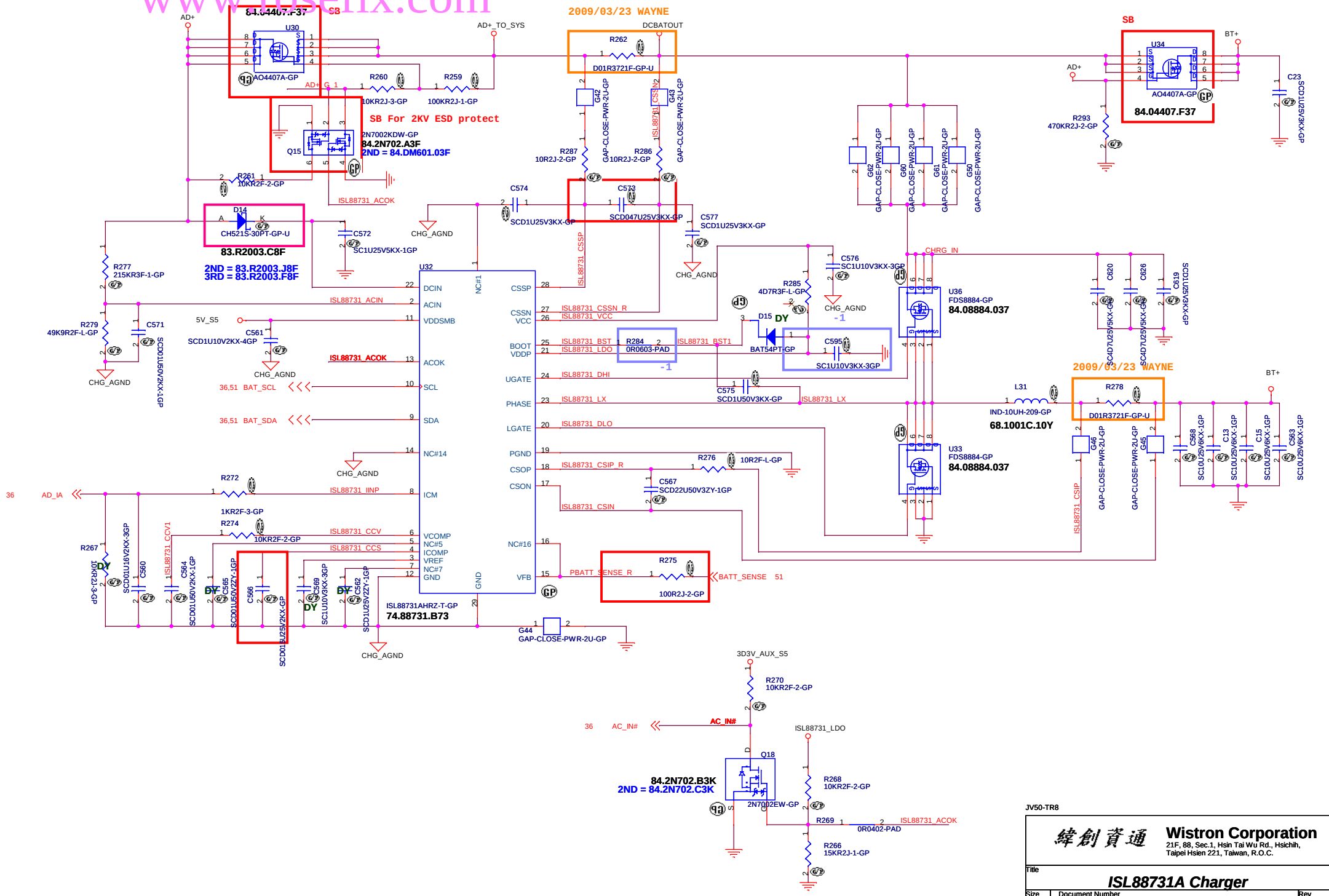
JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO 2D5V/1D5V/1D2V S5/1V VGA

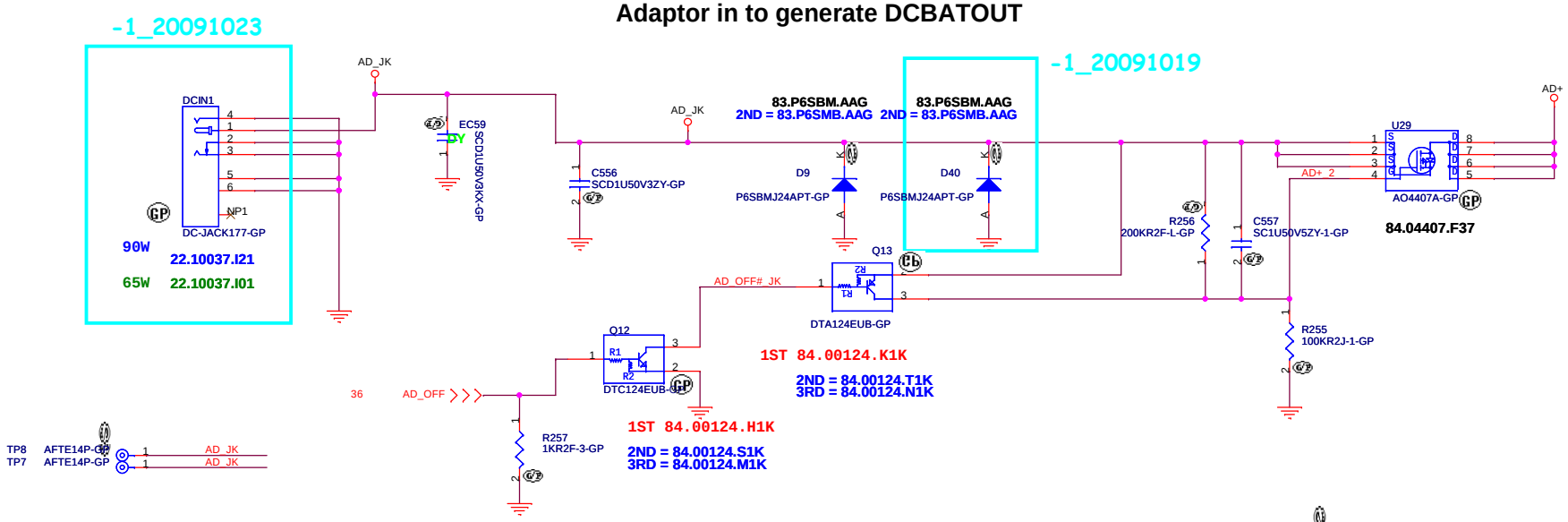
Size: A3 | Document Number: JV50-TR8 | Rev: -1

Date: Wednesday, November 11, 2009 | Sheet 49 of 63

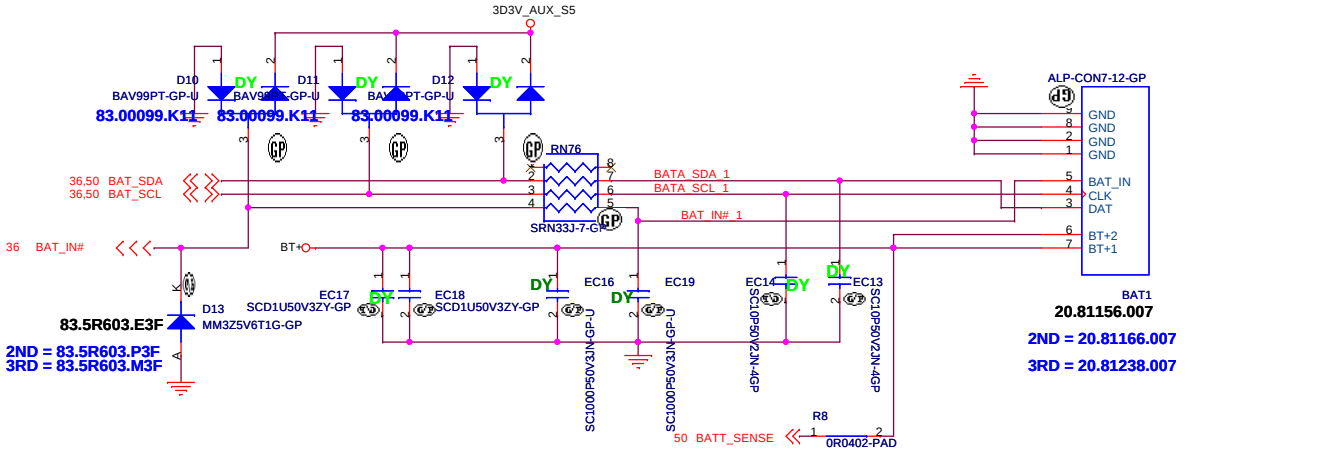


JV50-TR8			
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	ISL88731A Charger		
Size A3	Document Number JV50-TR8		Rev -1
Date: Thursday, November 12, 2009	Sheet 50 of 63		

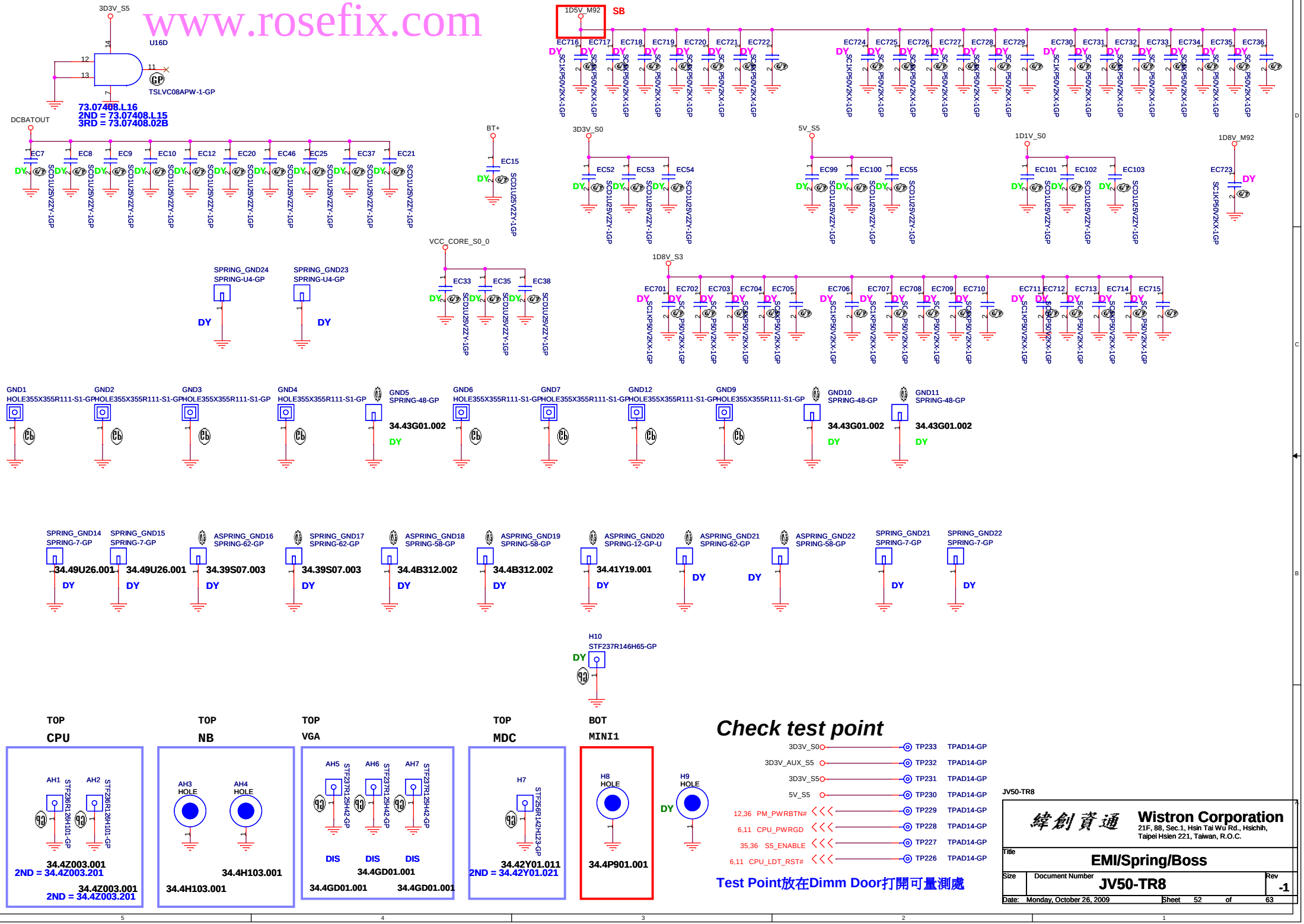
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AD/BATT CONN	
Size	Document Number JV50-TR8	Rev -1
Date: Monday, October 26, 2009	Sheet 51 of 63	



JV50-TR8

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	EMI/Spring/Boss	
Size	Document Number JV50-TR8	Rev -1
Date: Monday, October 26, 2009	Sheet 52 of 63	

Iomax=23A, OCP>40A

RT8209E for VGA

DCBATOUT
DCBATOUT_8209E_VGA
G136 GAP-CLOSE-PWR
G138 GAP-CLOSE-PWR
G140 GAP-CLOSE-PWR
G142 GAP-CLOSE-PWR
5V_S5
C1037 SC1U10V2KX-1GP
R1286 10R2F-L-GP
C1041 SC1U10V2KX-1GP
D36 B0530WS-7-F-GP
R1287 3D3K3J-L-GP
8209A_R_BOOT_VGA
C1038 SCD1U16V2KX-3GP
U81
8209A_VDD_VGA
RT8209_FB_VGA
8209A_BOOT
8209A_EN/DEM_VGA
8209A_TON_VGA
8209A_CS_VGA
VDD VDDP FB BOOT EN/DEM TON CS
UGATE LGATE PHASE VOUT PGOOD GND PGND NC#15
RT8209EGQW-GP
8209A_HGATE_VGA
8209A_LGATE_VGA
8209A_PHASE_VGA
8209A_PGOOD_VGA
VGA_CORE_PWR
R1288 8K2R2F-1-GP
R1290 220KR2F-GP
R1289 10KR2J-3-GP M9X
12,34,35,36,42,44,49,54 PM_SLP_S3#
D38 BAS16PT-GP
83.00016.F11
2ND = 83.00016.B11
Madison-Park
R1293 10KR2J-3-GP Madison-Park
3D3V_M92
C1043 16KR3F-GP
3D3V_S0
R1291 10KR2J-3-GP
R1292 0R0402-PAD-1-GP
VGA_CORE_POK 49
C1042 SC100P50V2JN-3GP
-1_20091021
U80 SIR474DP-T1-GE3-GP
U82 SIR460DP-T1-GE3-GP
U83 SIR460DP-T1-GE3-GP
C1039 C1040 C1056 SC1U25V5KX-GP
L62 IND-D45UH-14-GP
TC38 TC39 SE330U2VDM-L-GP
79.33719.L01
Vout=0.75*(1+Rh/Rl)
C1044 SC47P50V2JN-3GP
R1294 10KR2F-2-GP
RT8209_FB_VGA
R1295 49K9R2F-L-GP
R1296 110KR2F-L-GP
NV_VID1_Q
Q39 84.2N702.B3K 2ND = 84.2N702.C3K 2N7002EW-GP
R1298 10KR2J-3-GP
PWRCNTL_1 56
C1046 SCD1U10V2KX-4GP
R1297 73K2R2F-GP
NV_VID0_Q
Q40 2N7002EW-GP 84.2N702.B3K 2ND = 84.2N702.C3K
-1_20091019
R1309 100KR2J-1-GP
NV_VID0_R
Q45 MMBT2222A-3-GP
R1299 10KR2J-3-GP
PWRCNTL_0 56
C1045 SCD1U10V2KX-4GP
VCC_GFX_CORE
G137 G139 G141 G143 G144 G145 G146 G147 G148 G149 G150 G151 G152 G153 G154 G155 G156 G157 G158 G159 G160 G161 GAP-CLOSE-PWR

M92 XT			
R1295	37.4K	R1297	30K
VGA_CORE	1.20V		

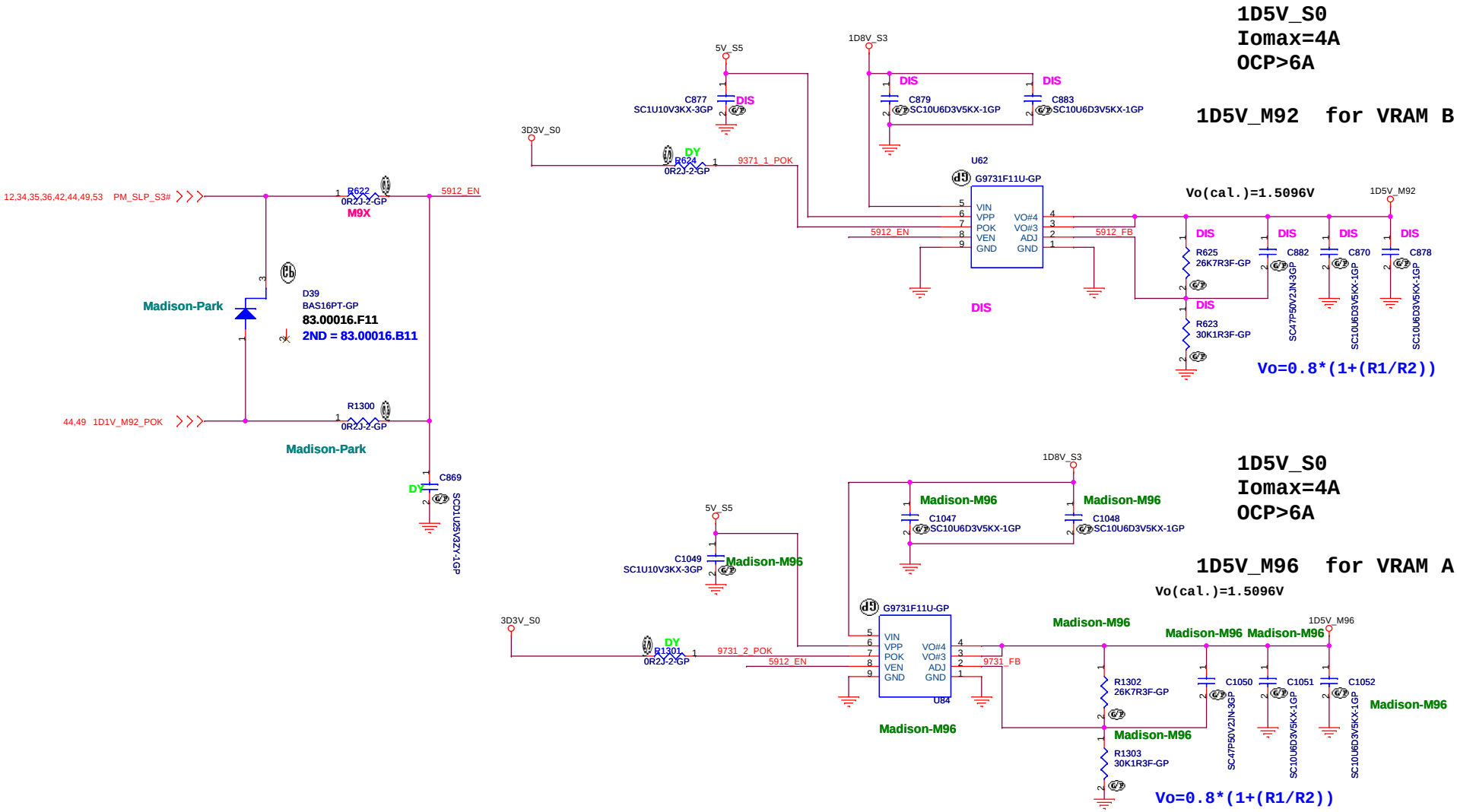
30k(64.30025.6DL)
73.2k(64.73225.6DL)
37.4k (64.37425.6DL)

	Madison Pro	Park XT	M96 Pro
R1297	73.2K	36.5K	30K
VGA_CORE	1.00V	1.12V	1.15V

	Madison Pro	Park XT	M96 Pro	M92-XT
PWRCNTL_0				
0	1.00V	1.12V	1.15V	1.20V
1	0.90V	0.90V	0.90V	0.95V

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E VGA CORE
Size: A3
Document Number: JV50-TR8
Rev: -1
Date: Thursday, November 12, 2009
Sheet 53 of 63



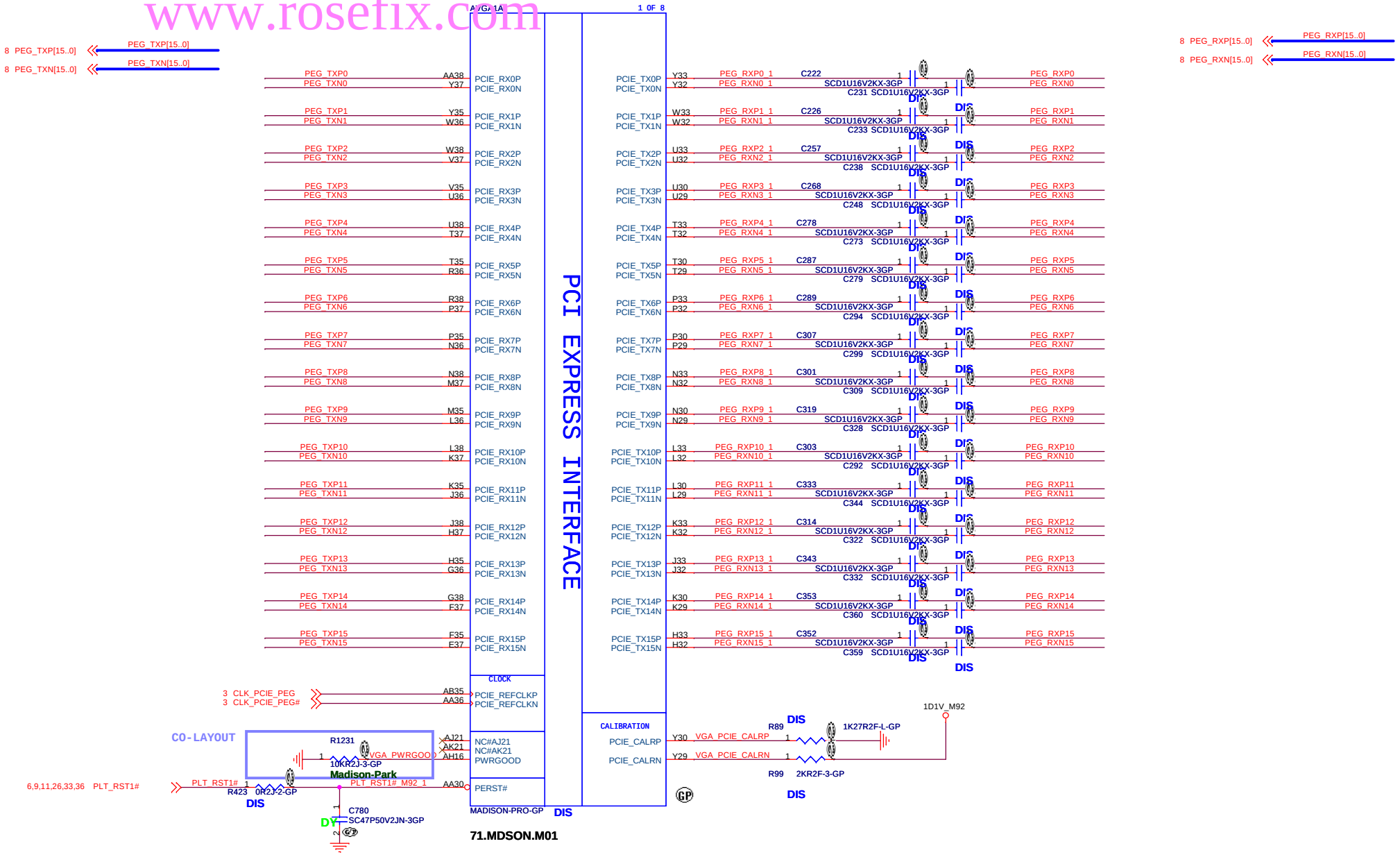
JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G9731_1D5V_VRAM POWER

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Wednesday, November 11, 2009 Sheet 54 of 63



DIS / UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Madison PCIE		
Size: A3	Document Number: JV71-TR	Rev: -1
Date: Monday, October 26, 2009	Sheet 55 of 63	

Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type
selection H/W strap
Should provide VRAM Table for VBios
request

DVPDATA [3:0]
0100 1GB GDDR3 Hynix-H5TQ1G63BFR-12C (800MHz)
1000 1GB GDDR3 Samsung-K4W1G1646E-HC12 (800MHz)
1100 1GB GDDR3 ATI (800MHz)

It's strap for GDDR3-136ball
Need to Clarify

Back Bias (body bias) which minimizes
power consumption in battery modes.
PD = Disable
PU = Enable

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

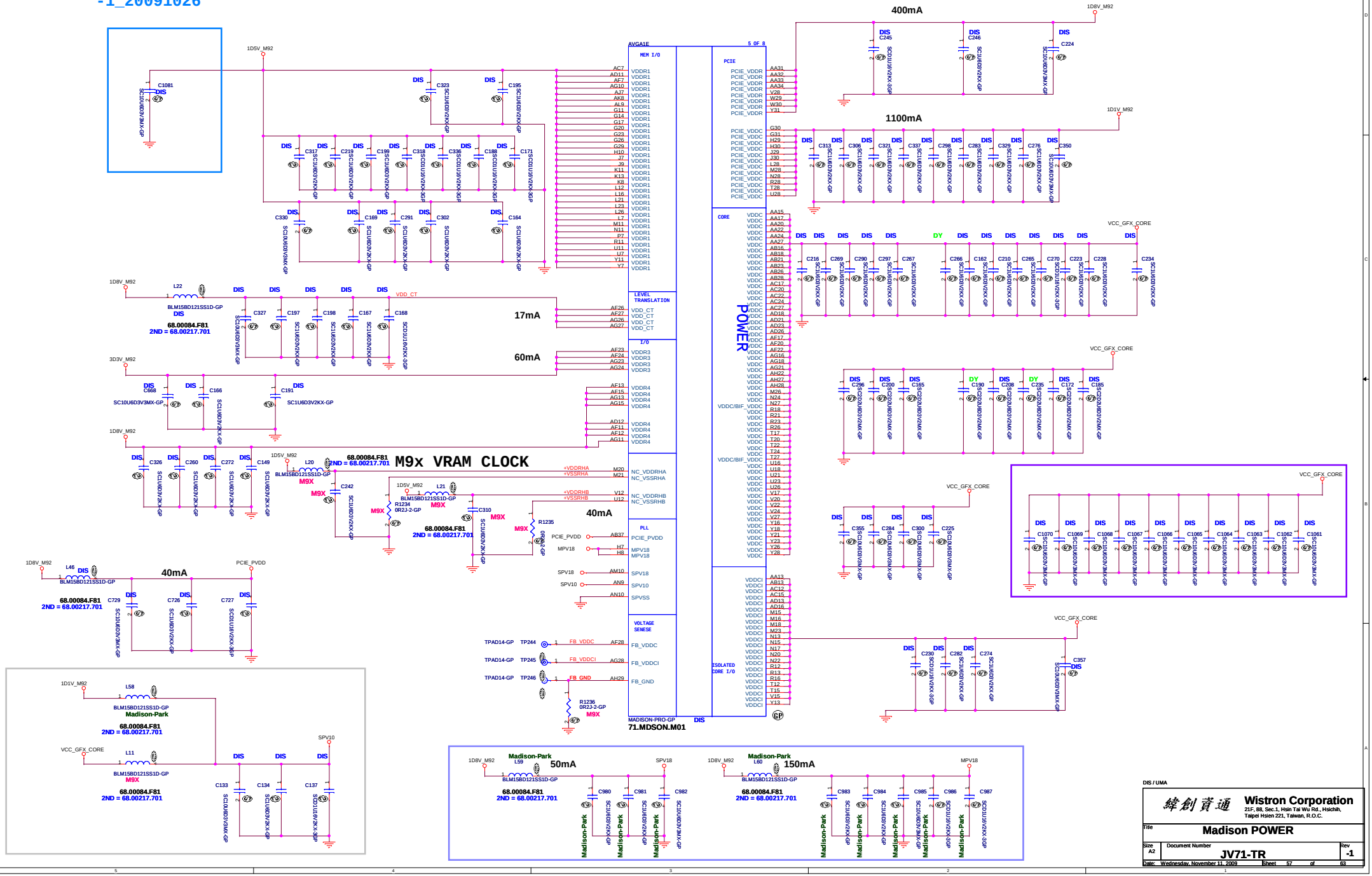
For Thermal sensor

for TR

71.MDSON.M01

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Madison IO
Size A2	Document Number JV71-TR Rev -1
Date: Wednesday, November 11, 2009	Sheet 56 of 63

-1_20091026



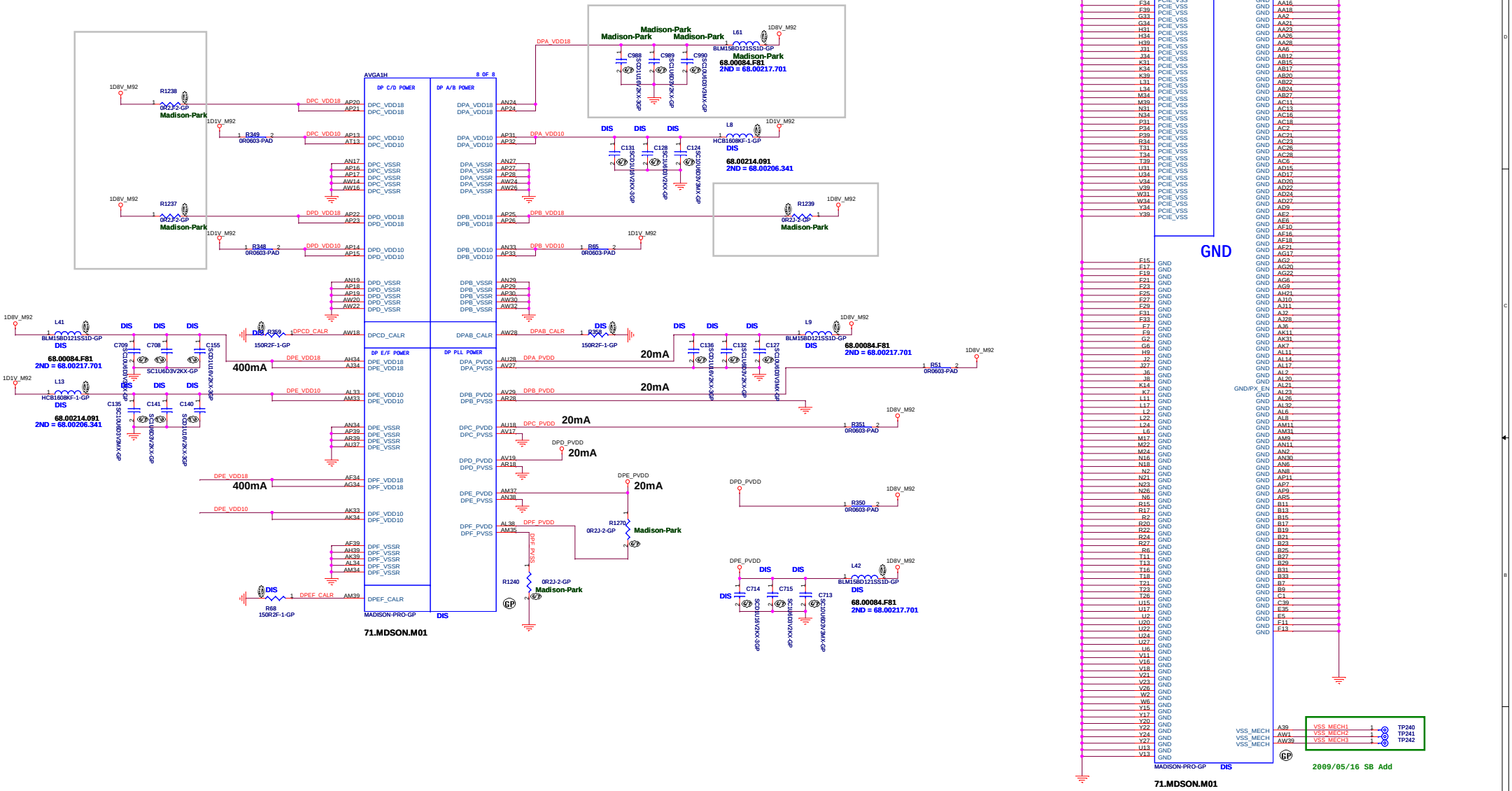
DIS / UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison POWER

Size: A2 | Document Number: JV71-TR | Rev: -1

Date: Wednesday, November 11, 2009 | Sheet 57 of 63



DIS / UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

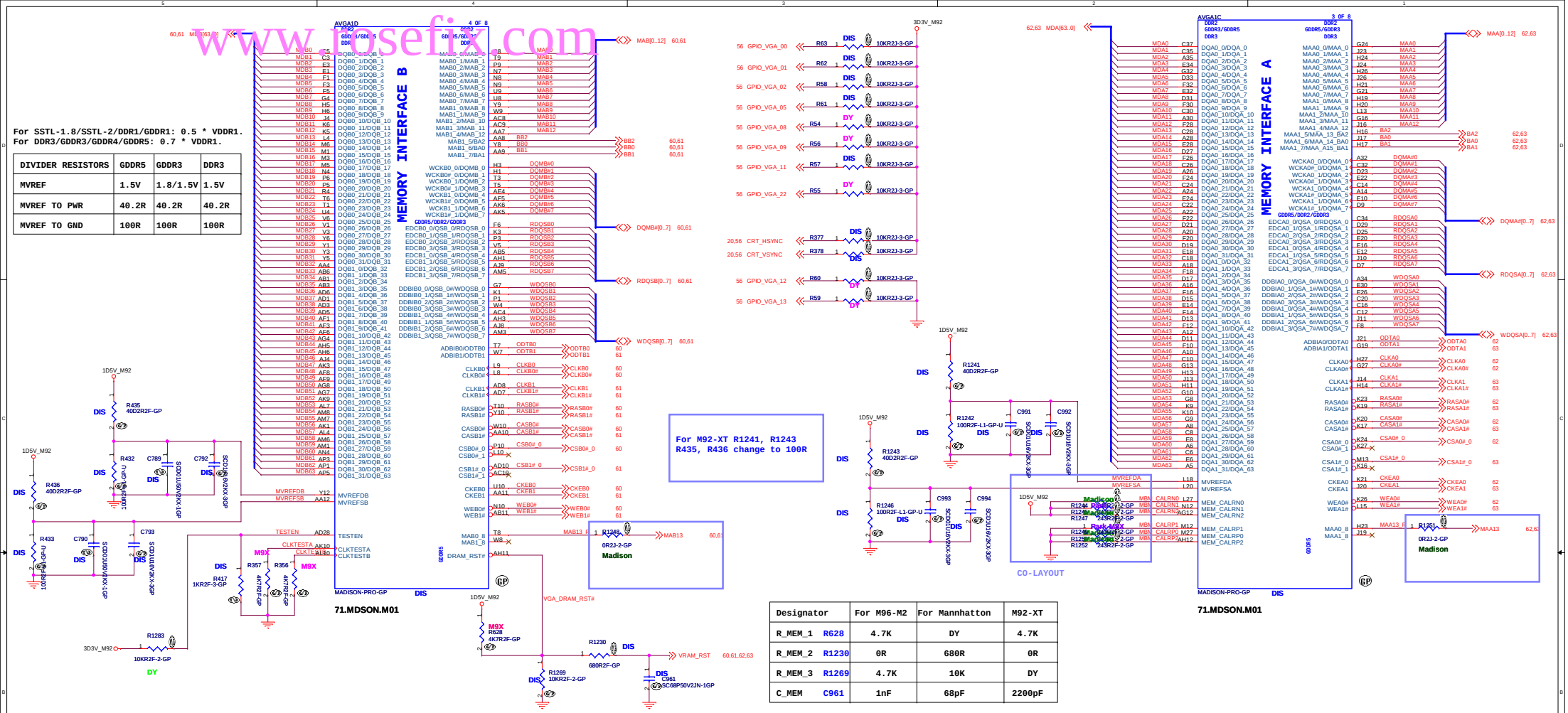
Title: **DP POWER_GND**

Size	Document Number	Rev
A2	JV71-TR	-1

Date: Monday, October 05, 2009 Sheet 58 of 63

For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



Designator		For M96-M2	For Mannhatton	M92-XT
R_MEM_1	R628	4.7K	DY	4.7K
R_MEM_2	R1230	0R	680R	0R
R_MEM_3	R1269	4.7K	10K	DY
C_MEM	C961	1nF	68pF	2200pF

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000			
V 256MB	x001			
64MB	x010	ST Microelectronics	M25P05A	0100
32MB	x		M25P10A	0101
512MB	x		M25P20	0101
1GB	x		M25P40	0101
2GB	x		M25P80	0101
4GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
			Pm25LV010A	0101

DIS / UMA

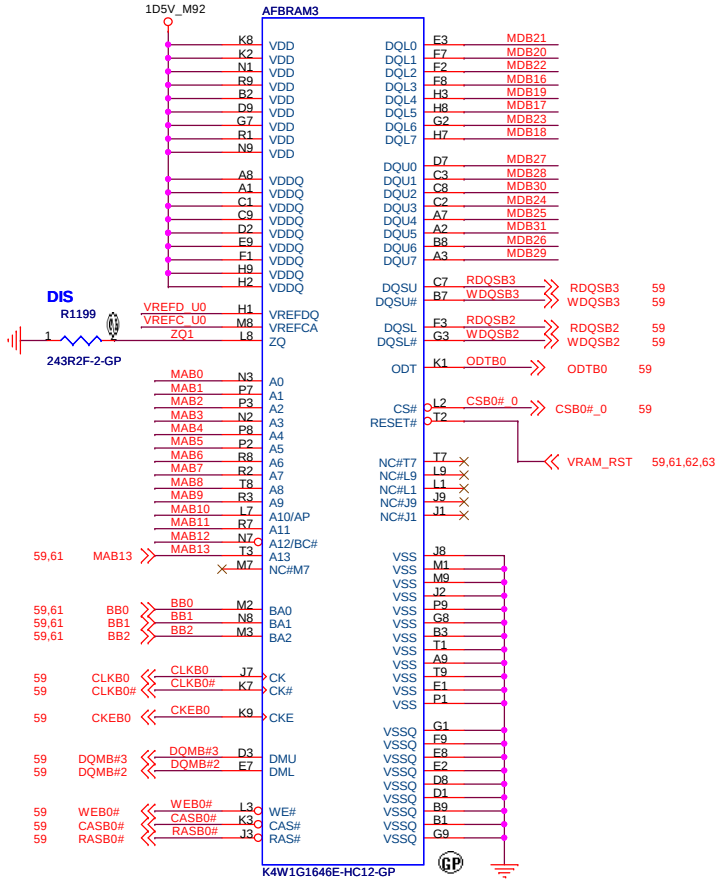
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

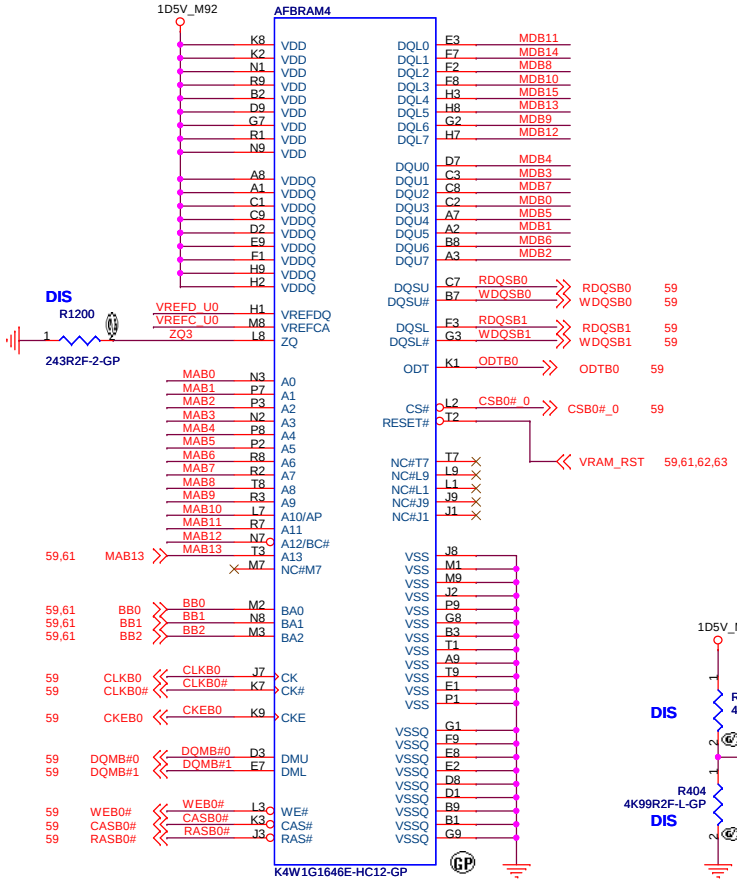
Title: Madison Memory / Straps

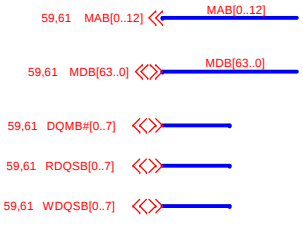
Size: A2 | Document Number: JV71-TR | Rev: -1

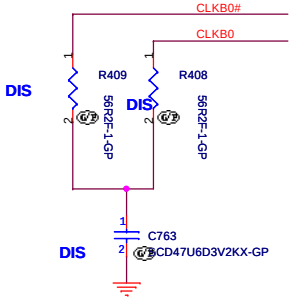
Date: Wednesday, November 11, 2009 | Sheet 59 of 63

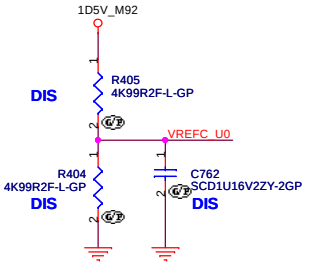
GDDR3

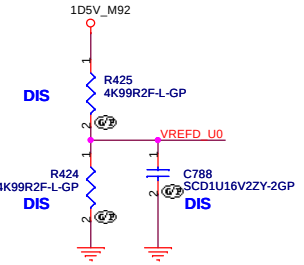












DIS

72.41164.H0U

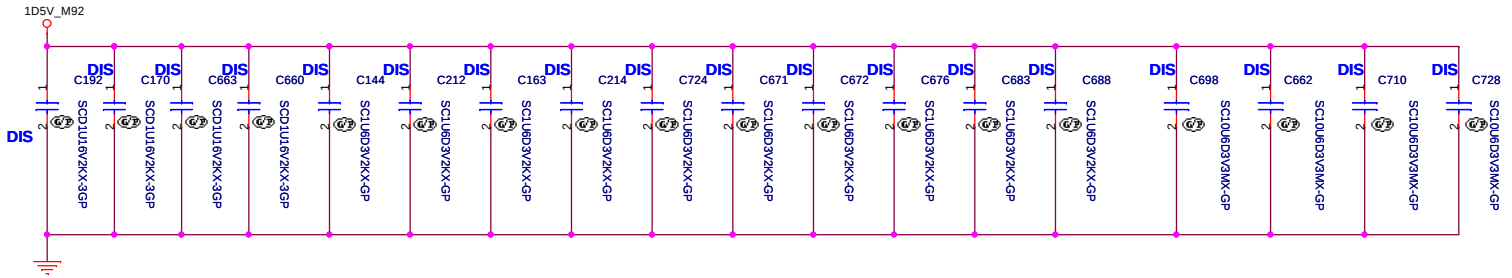
2ND = 72.51G63.C0U

SAMSUNG 1ST=72.41164.H0U
HYUNIX 2ND=72.51G63.C0U

DIS

72.41164.H0U

2ND = 72.51G63.C0U

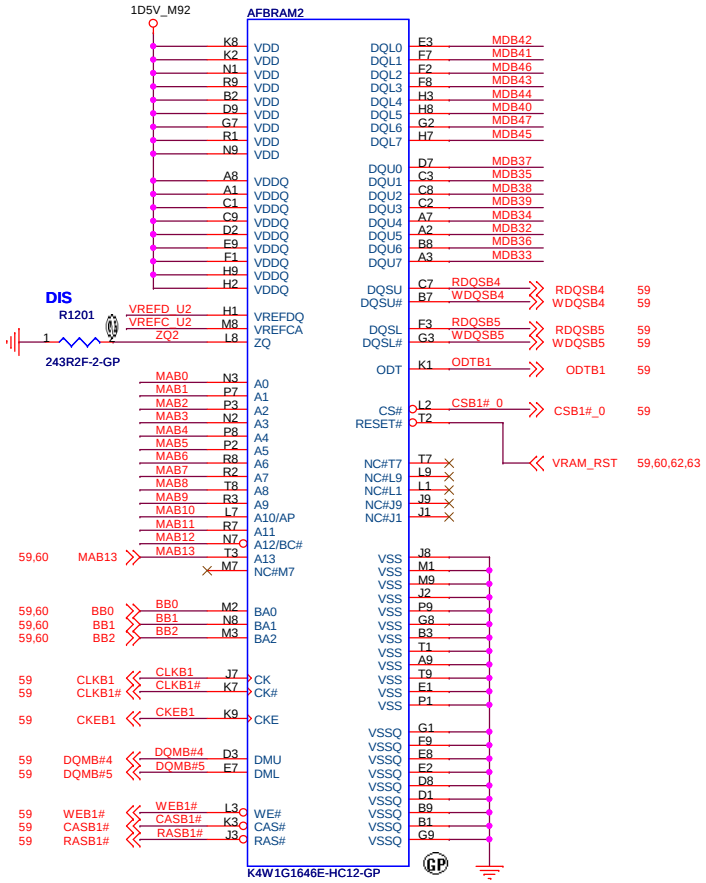


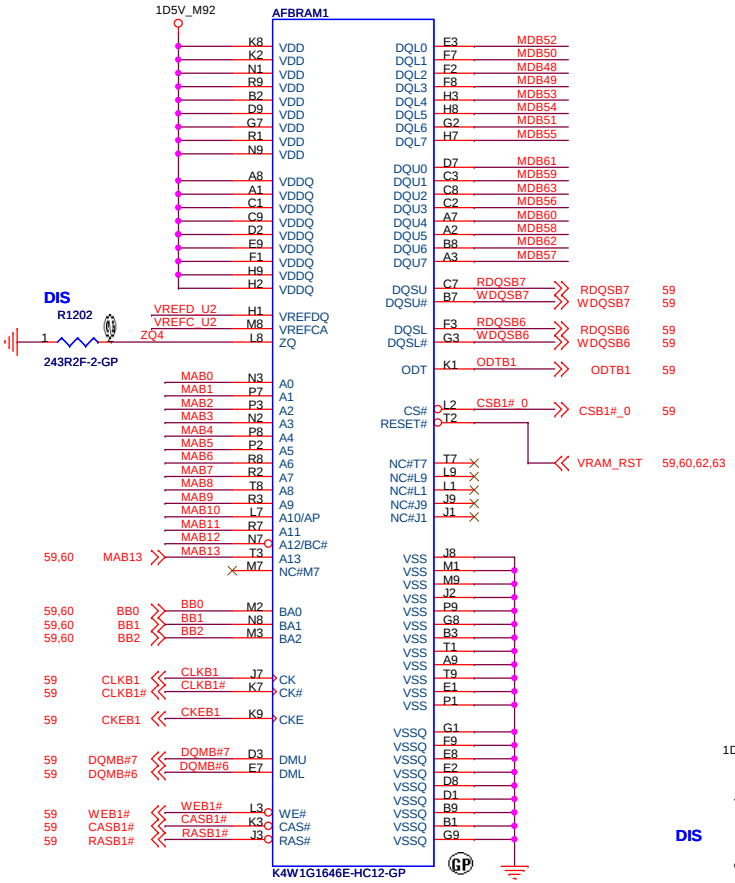
JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	M92 DDR3 B0	
Size A3	Document Number JV50-TR8	Rev -1
Date: Monday, October 26, 2009	Sheet 60 of 63	

DDR3





DIS

72.41164.H0U

2ND = 72.51G63.C0U

SAMSUNG 1ST=72.41164.H0U
HYUNIX 2ND=72.51G63.C0U

DIS

72.41164.H0U

2ND = 72.51G63.C0U

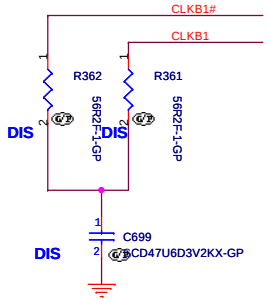
59,60 MAB[0..12] → MAB[0..12]

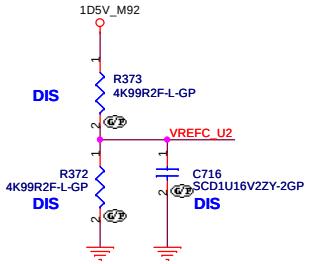
59,60 MDB[63..0] → MDB[63..0]

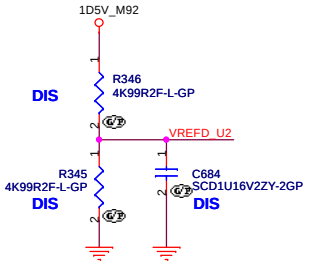
59,60 DQMB#[0..7]

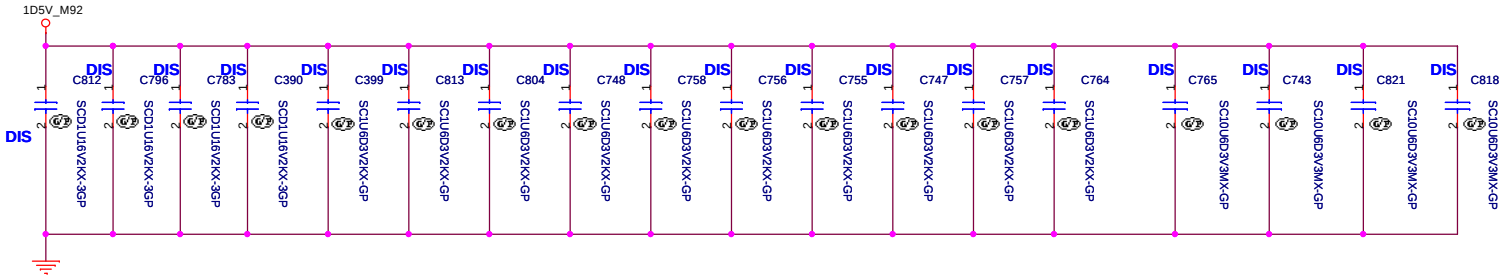
59,60 RDQSB[0..7]

59,60 WDQSB[0..7]







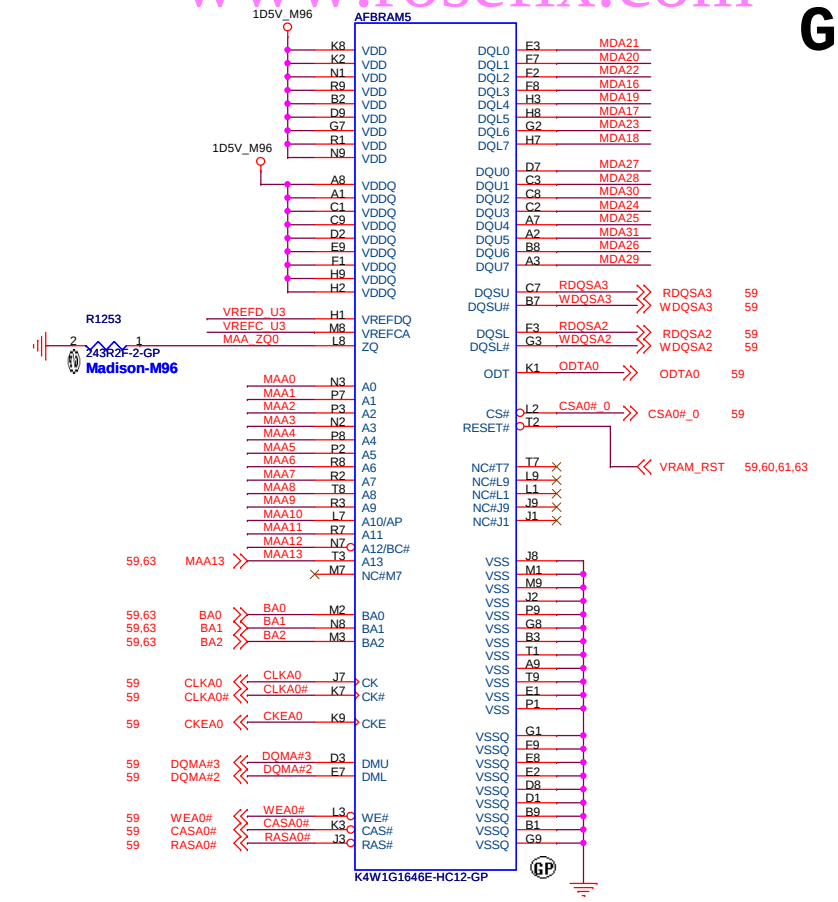


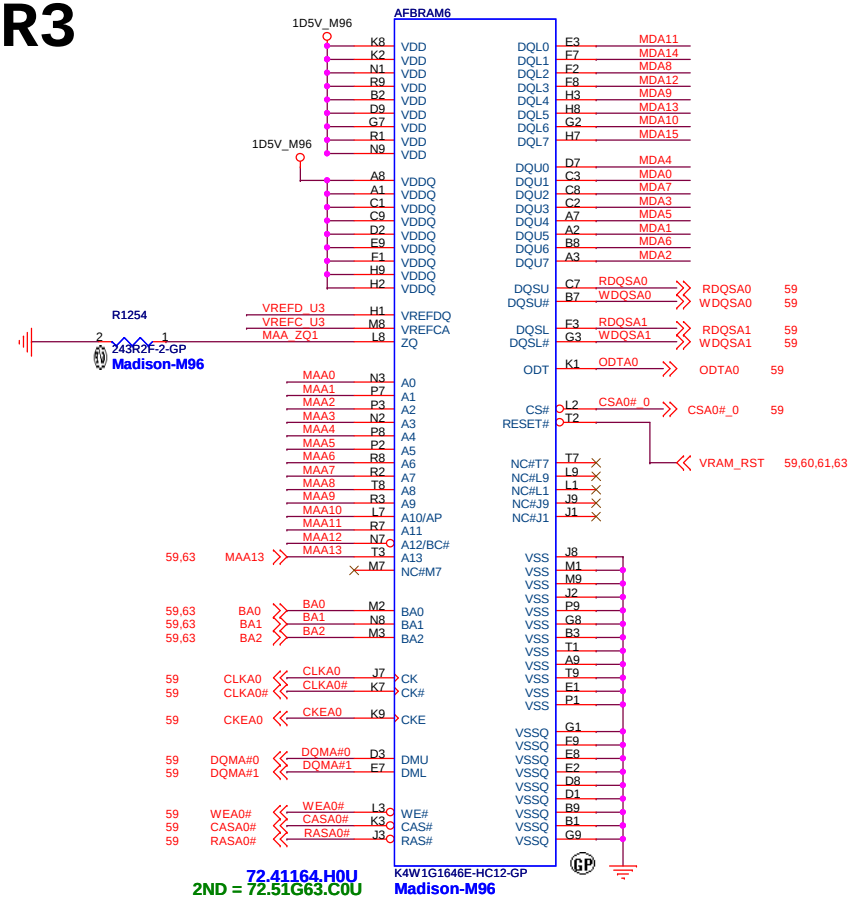
JV50-TR8

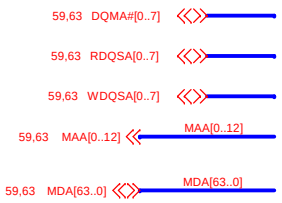
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

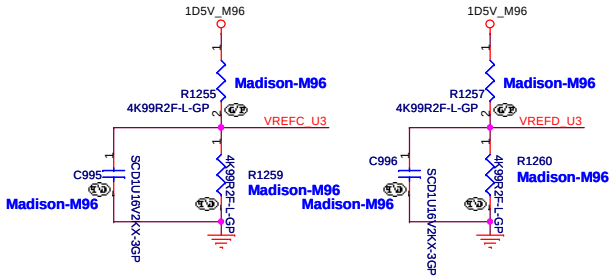
Title	M92 DDR3 B1	
Size A3	Document Number JV50-TR8	Rev -1
Date: Monday, October 26, 2009	Sheet 61 of 63	

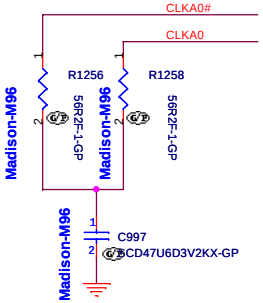
GDDR3

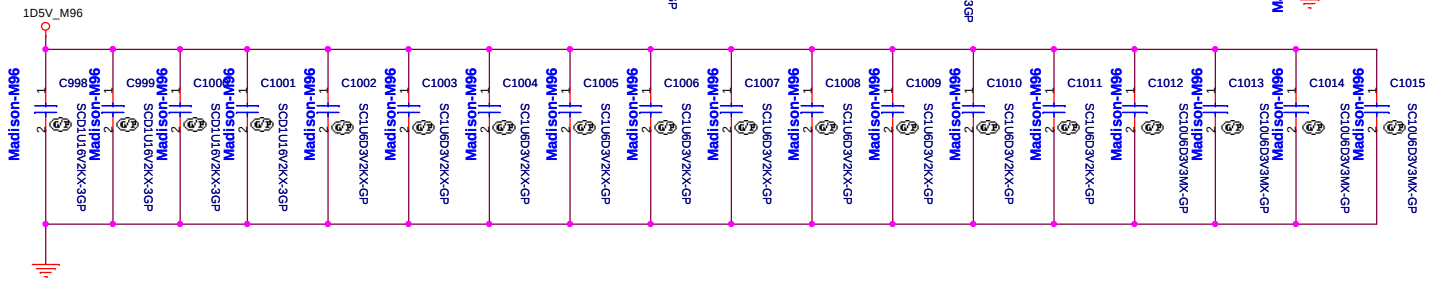








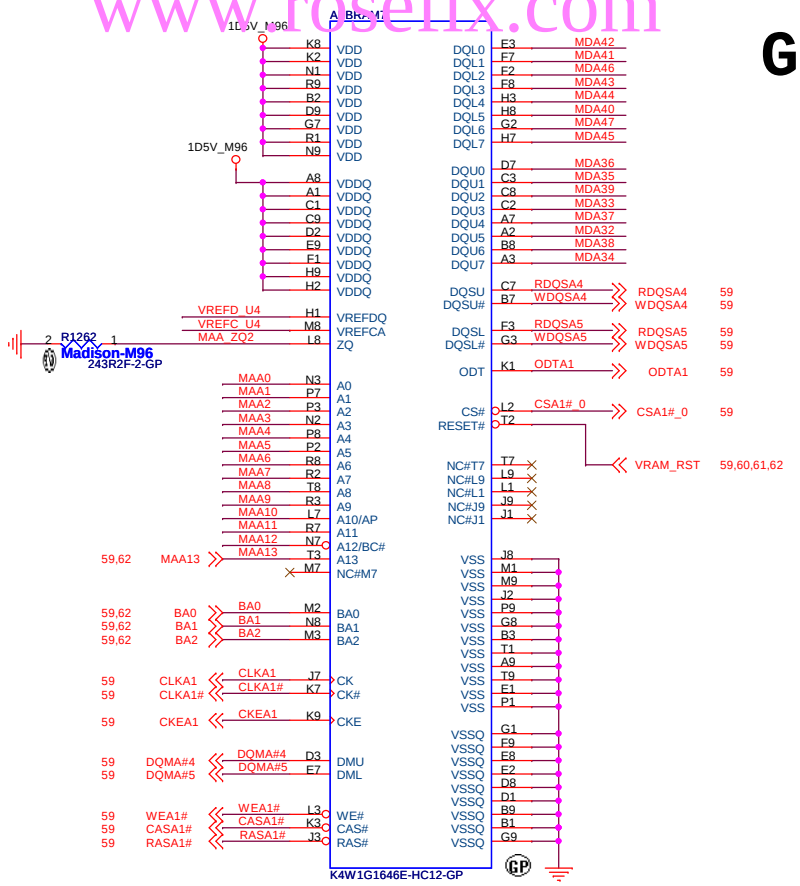


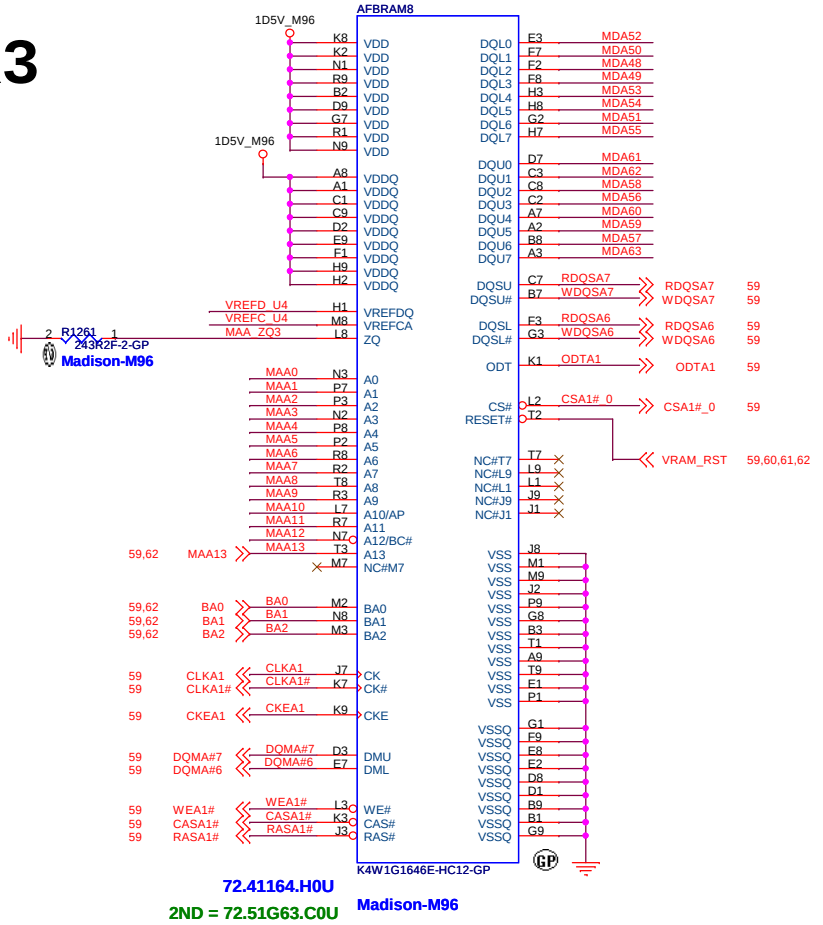


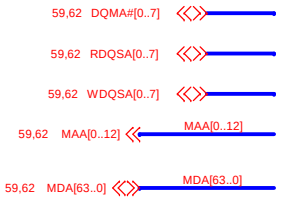
JV50-TR8

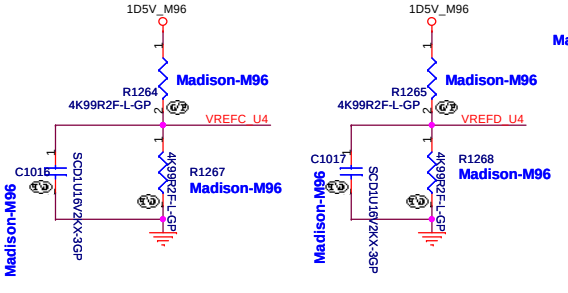
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: M92 DDR3 A0		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 62 of 63	

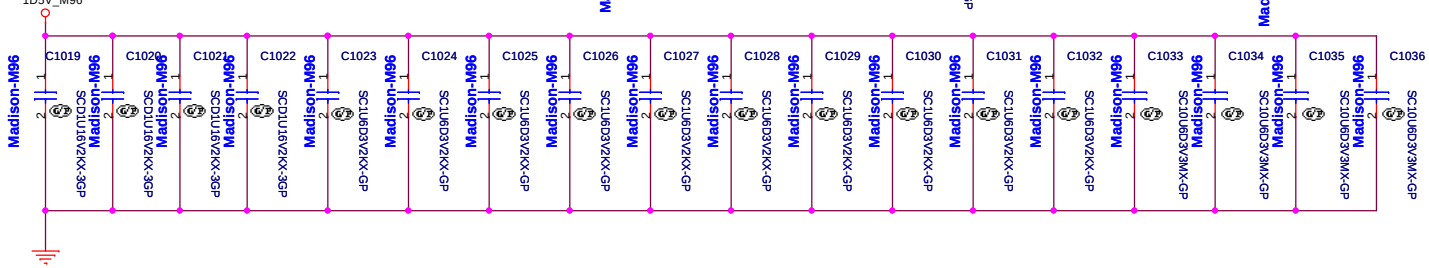
GDDR3











JV50-TR8

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: M92 DDR3 A1		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 63 of 63	