Quanta Project Name: XM1

Dell Project Name: Nike

G94 VGA

2008-03-17

REV : A1A

X01 Stage

QUANTA COMPUTER

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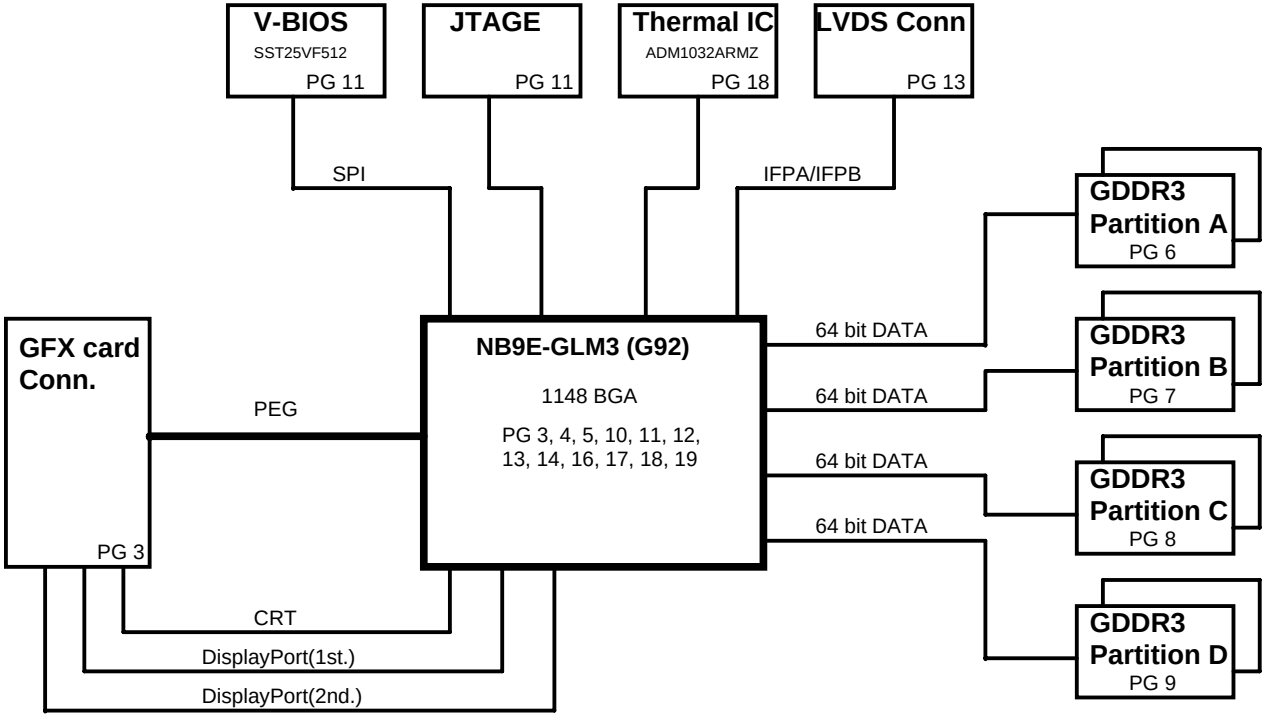
System Block Diagram for Nike G94 VGA

02

XM1 G94 PCB



POWER

DC/DC 1.1V_GFX PCIE and 1.8V_MEM	PG 20
VCORE NV_VCORE	PG 21

QUANTA COMPUTER

Title: System Block Diagram		
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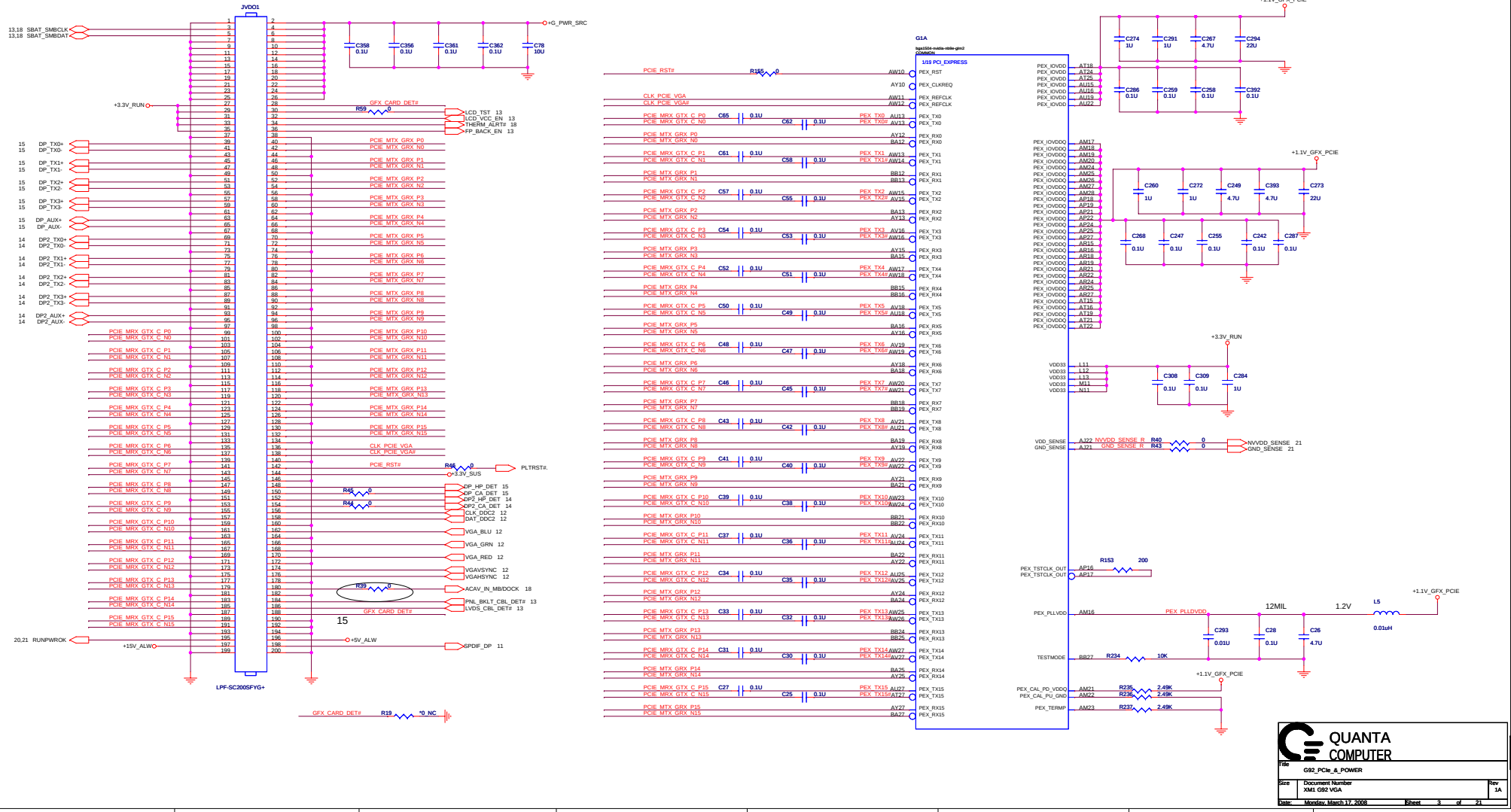
PEX Conn + GPU PEX

03



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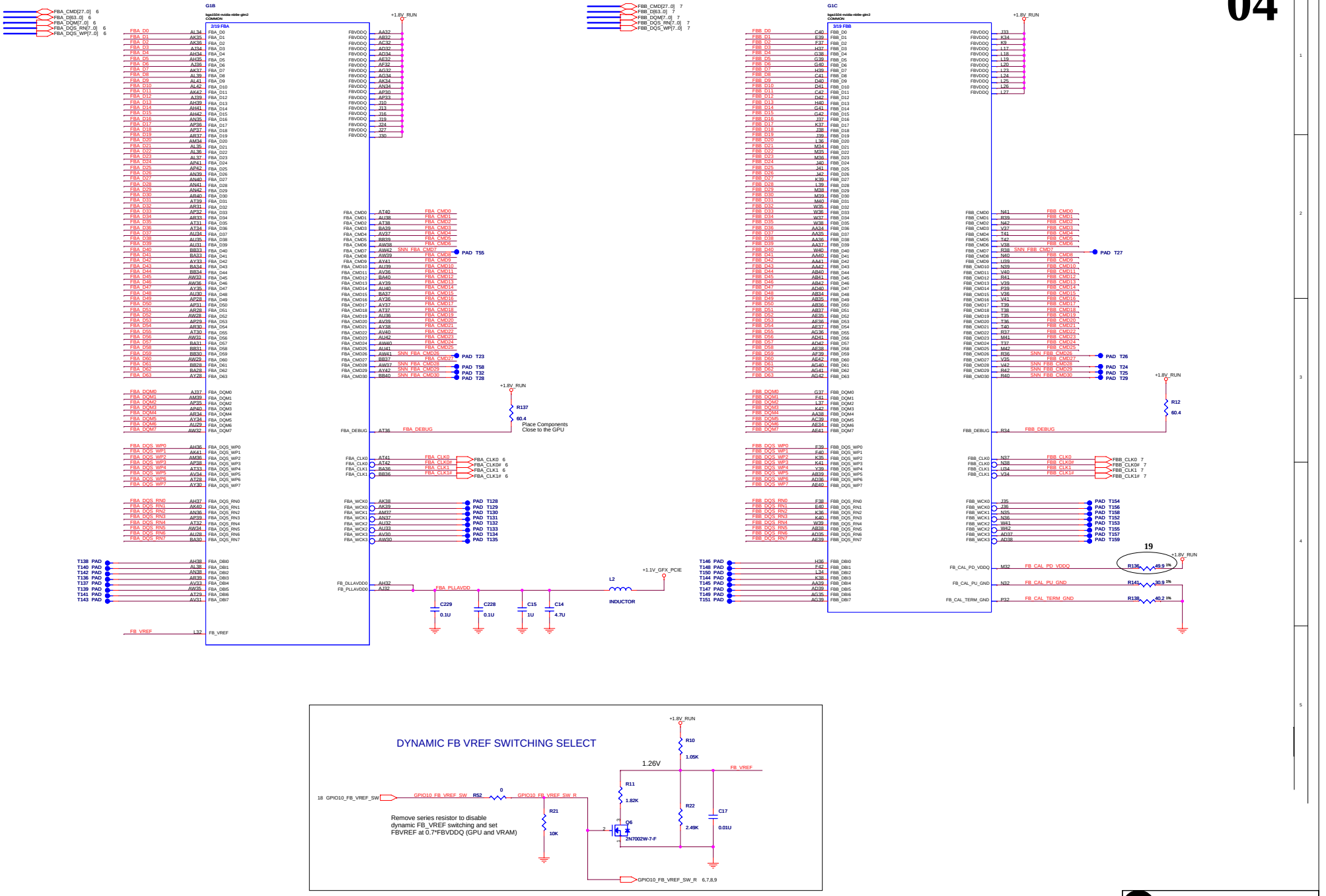
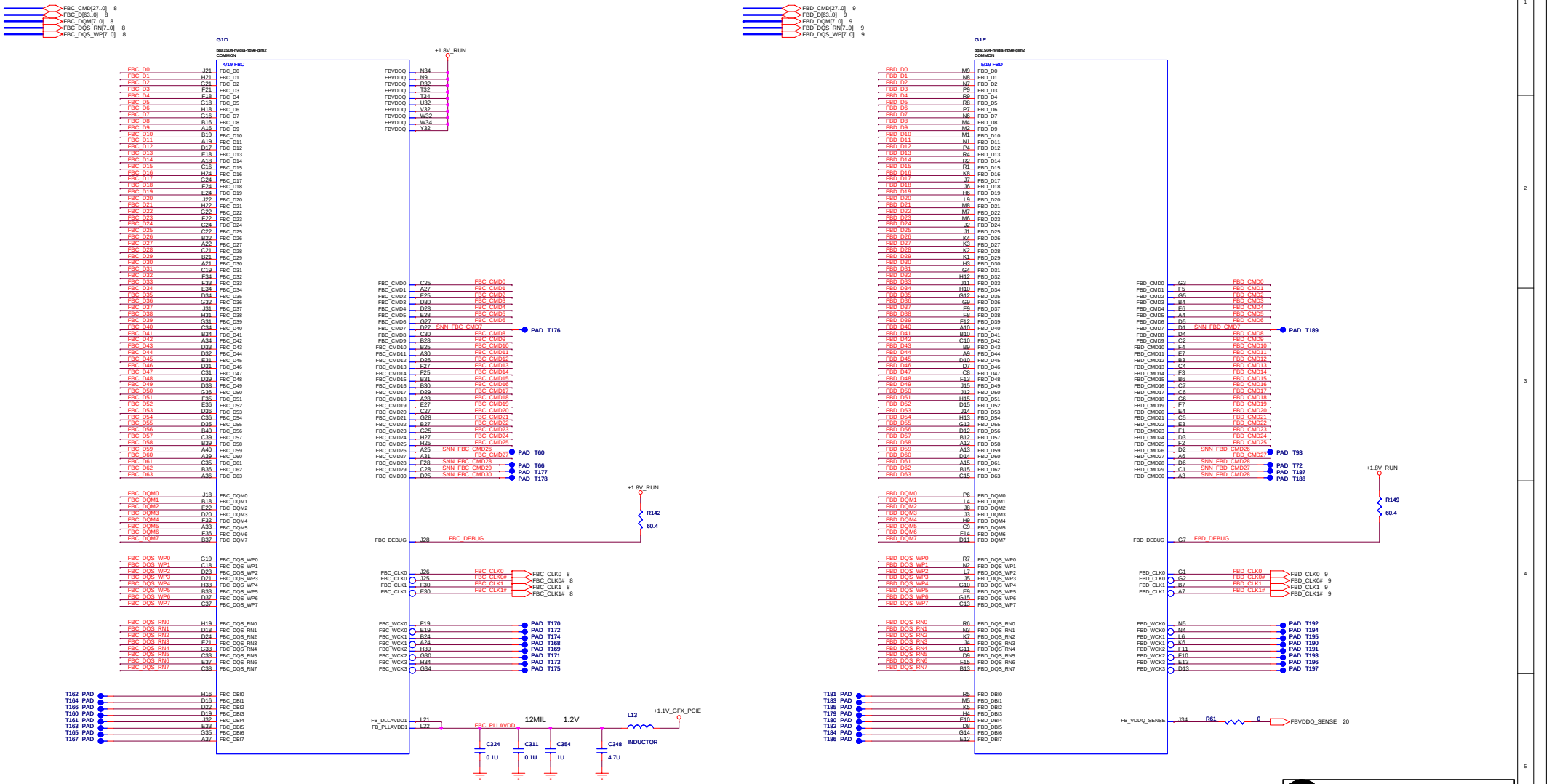
FrameBuffer - GPU Partition A/B

04



FrameBuffer - GPU Partition C/D

05



QUANTA COMPUTER

Title	G92_FB_Partition_C/D	
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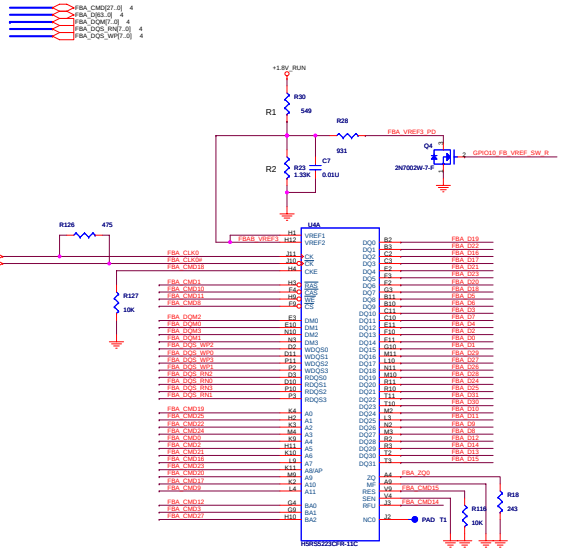
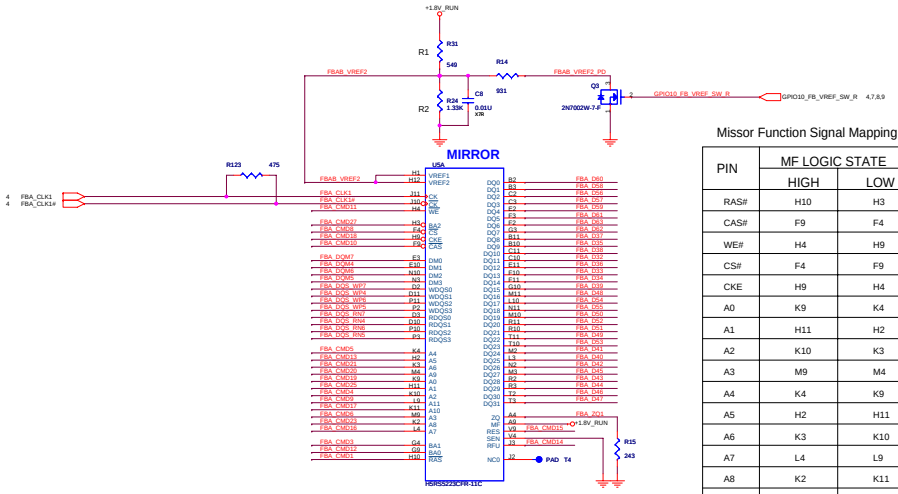
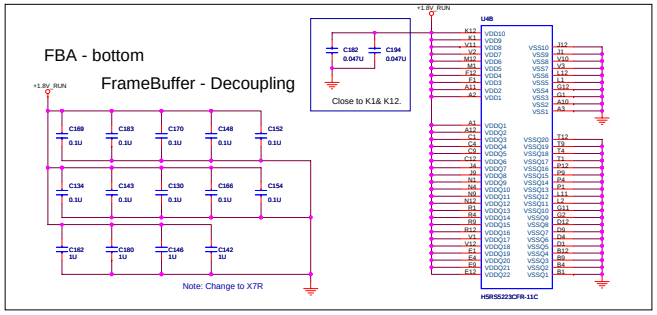
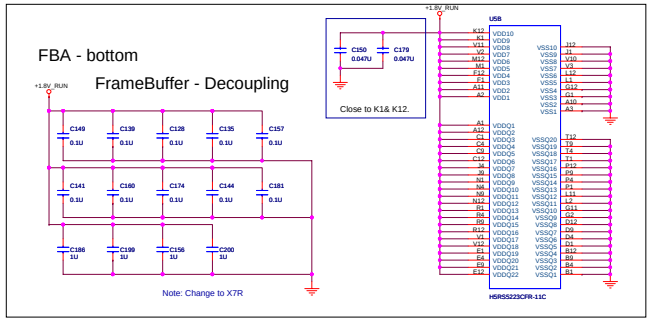


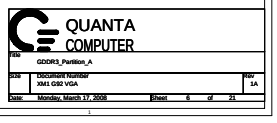


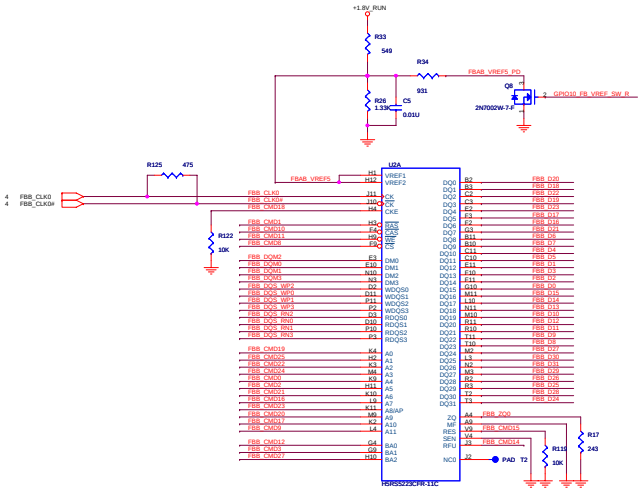
Missor Function Signal Mapping

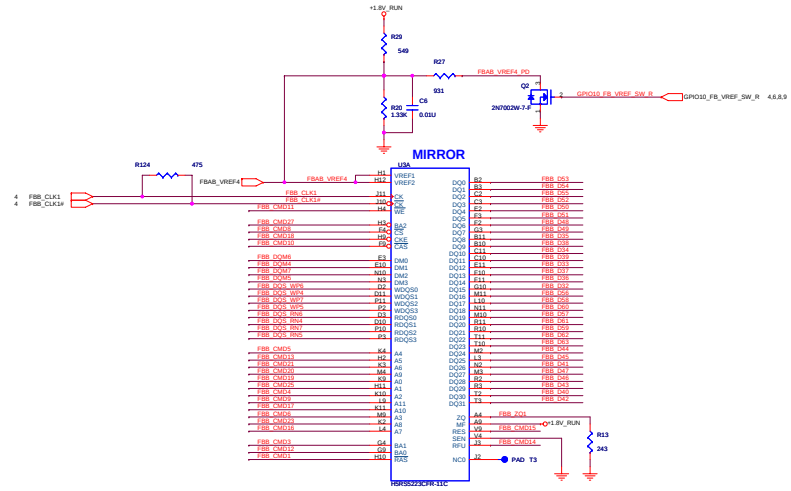
PIN	MF LOGIC STATE	
	HIGH	LOW
RAS#	H10	H3
CAS#	F9	F4
WE#	H4	H9
CS#	F4	F9
CKE	H9	H4
A0	K9	K4
A1	H11	H2
A2	K10	K3
A3	M9	M4
A4	K4	K9
A5	H2	H11
A6	K3	K10
A7	L4	L9
A8	K2	K11
A9	M4	M9
A10	K11	K2
A11	L9	L4
BA0	G9	G4
BA1	G4	G9
BA2	H3	H10

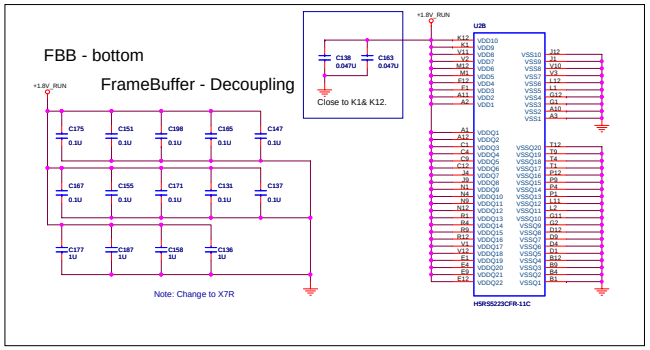


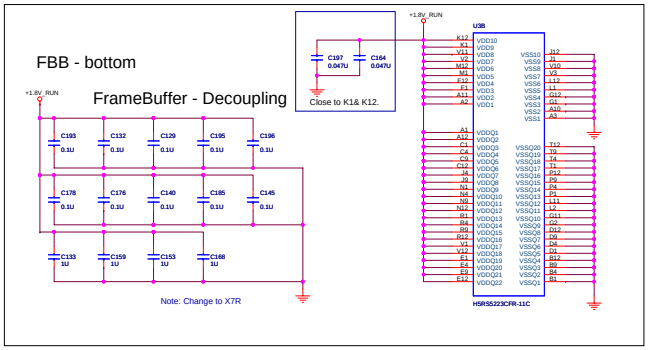












QUANTA COMPUTER

Title	GDDR3_Partition_B	
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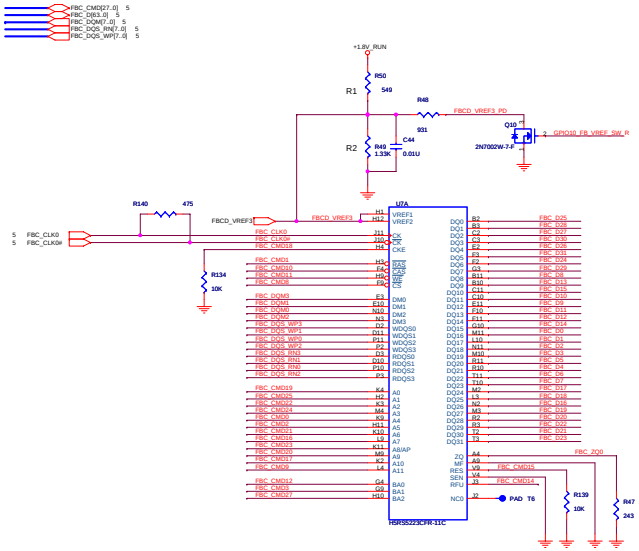

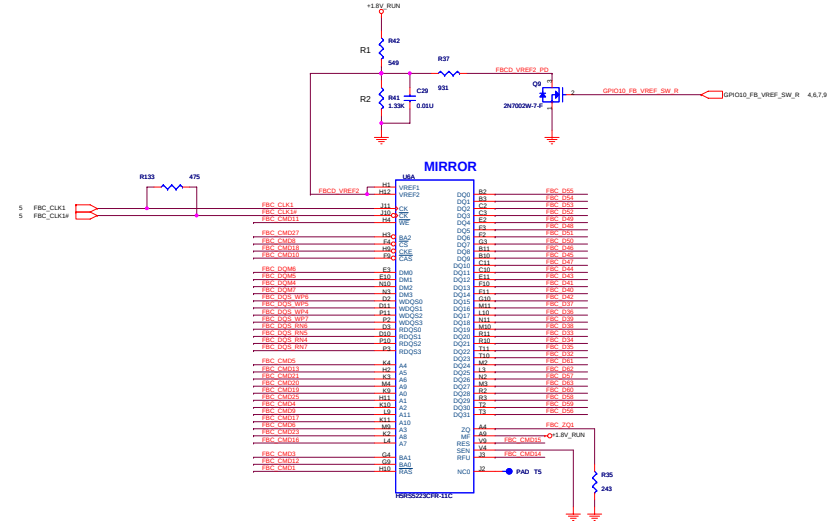

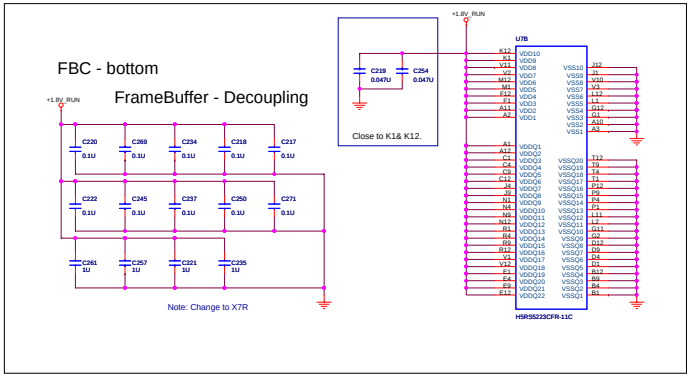

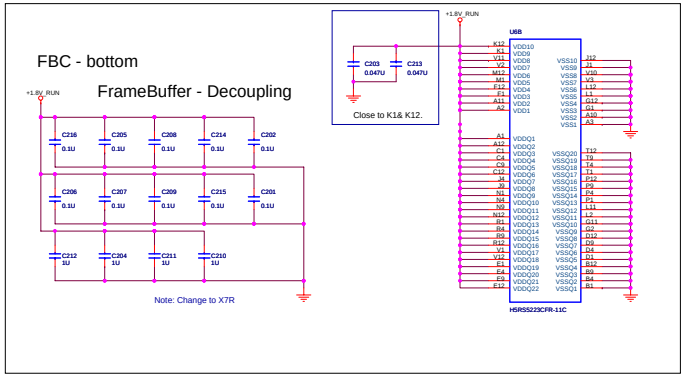

QUANTA COMPUTER

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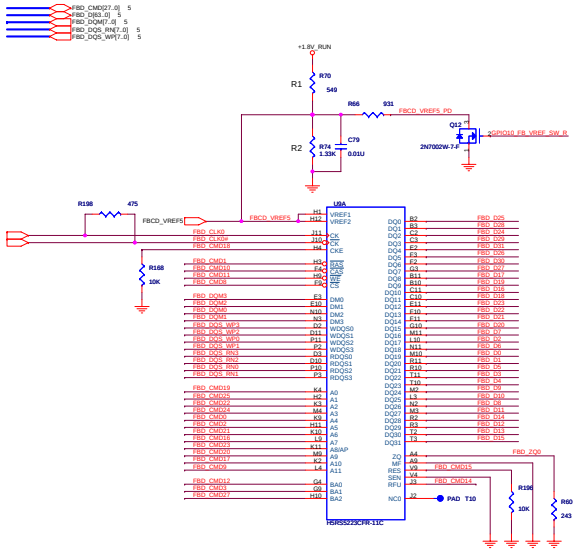

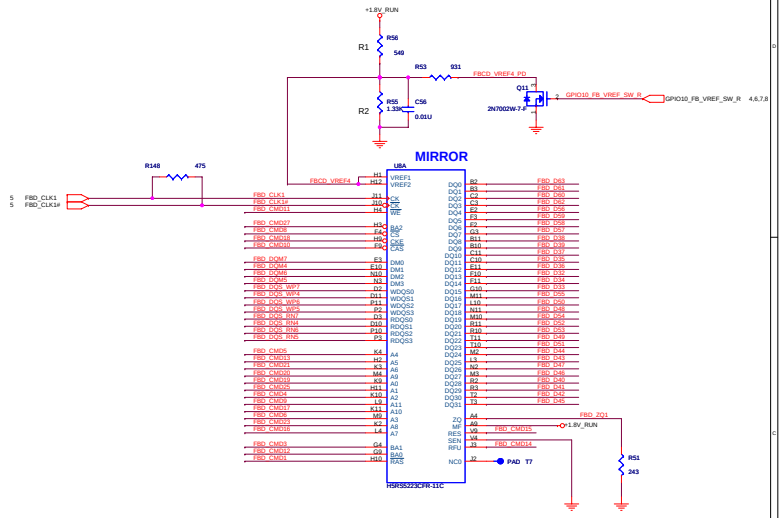

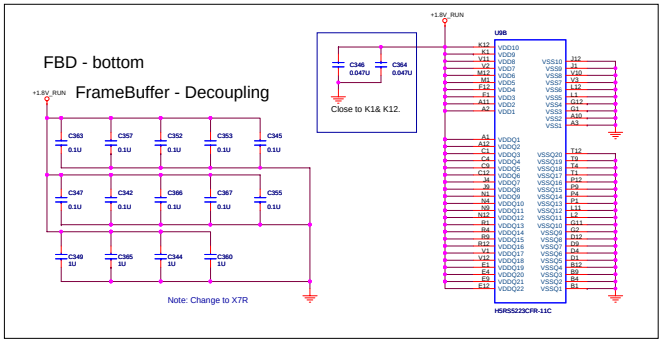

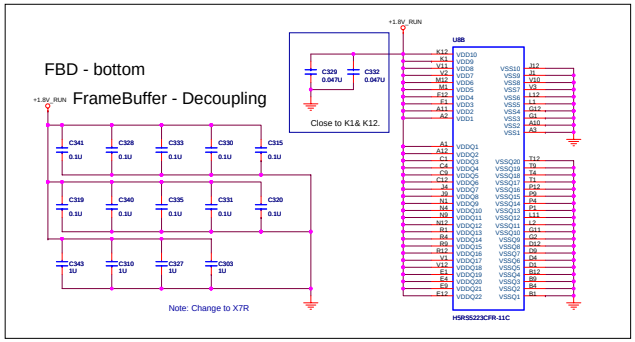

QUANTA COMPUTER			
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Power Decoupling and GND

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FBVDDQ

Under GPU

+1.8V_RUN

C244 0.1U, C256 0.1U, C288 0.1U, C226 0.1U

C280 0.1U, C241 0.1U, C224 0.1U, C225 0.1U

C227 .47U/6.3V, C236 .47U/6.3V, C240 .47U/6.3V, C232 .47U/6.3V, C230 .47U/6.3V, C231 .47U/6.3V

C266 .47U/6.3V, C297 .47U/6.3V, C248 .47U/6.3V, C243 .47U/6.3V, C233 .47U/6.3V, C279 .47U/6.3V

C239 1U, C246 1U, C321 1U, C275 1U

C238 4.7U, C300 4.7U, C406 4.7U, C407 4.7U

NVVDD

+VCC_GFX_CORE

Place under the GPU.

C252 0.1U, C262 0.1U, C251 0.1U, C263 0.1U, C282 0.1U, C289 0.1U, C265 0.1U, C402 0.1U

C264 0.1U, C292 0.1U, C283 0.1U, C295 0.1U, C281 0.1U, C290 0.1U, C296 0.1U

C276 .47U/6.3V/0402, C253 .47U/6.3V/0402, C270 .47U/6.3V/0402, C278 .47U/6.3V/0402, C277 .47U/6.3V/0402, C285 .47U/6.3V/0402, C301 .47U/6.3V/0402

C399 .47U/6.3V/0402, C395 .47U/6.3V/0402, C396 .47U/6.3V/0402, C397 .47U/6.3V/0402, C398 .47U/6.3V/0402, C400 .47U/6.3V/0402, C401 .47U/6.3V/0402

C403 4.7U, C404 4.7U, C405 4.7U

G1H

bga1504-nvidia-nbbe-gbn2

COMMON

G1F

bga1504-nvidia-nbbe-gbn2

COMMON

+VCC_GFX_CORE

G1G

bga1504-nvidia-nbbe-gbn2

COMMON

QUANTA COMPUTER

Title: G92_PWRDecoupling_&_GND

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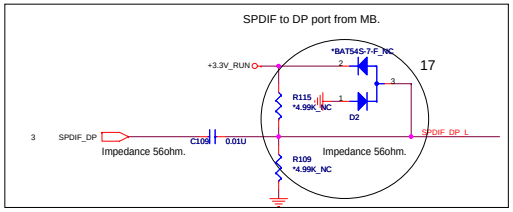
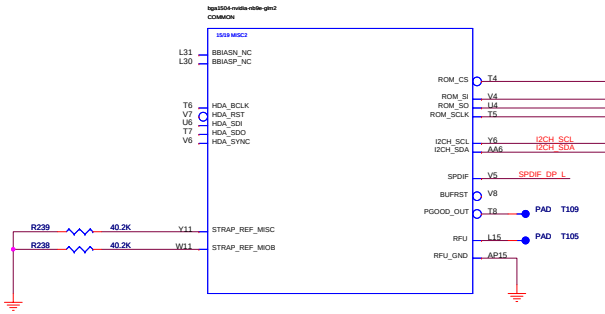
VBIOS MECHANICAL COMPONENTS-SCREW HOLES

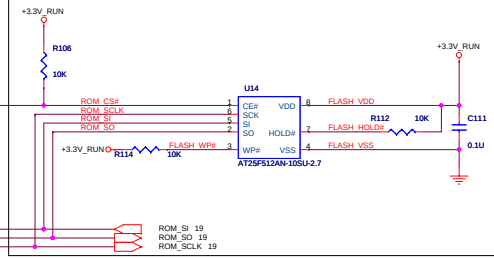
SPDIF to DP port from MB.



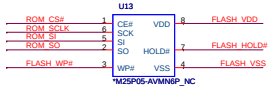


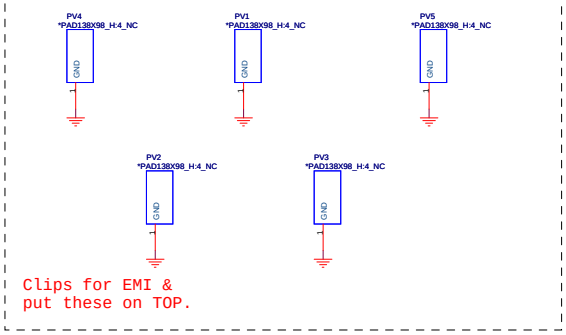
BIOS ROM

SPI ROM for V-BIOS

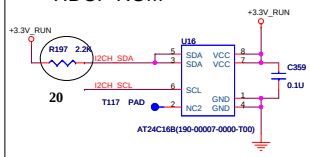


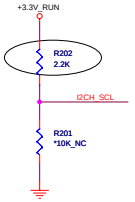
U33 dual layout for SST with SGT (U37).





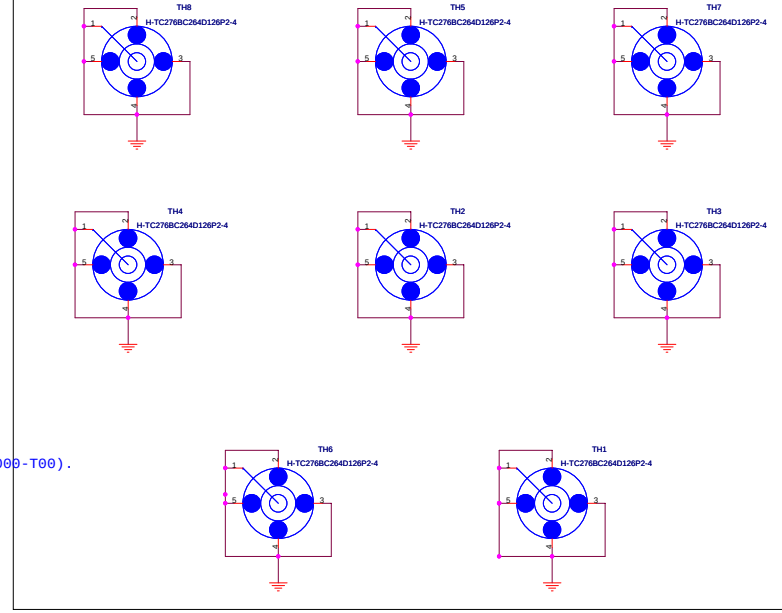
HDCP ROM





Stuff R202 for
standard I2C ROM(AT24C16B(190-00007-0000-T00).
Stuff R201 for
crypto ROM(AT88SC0808C-SU)

MECHANICAL COMPONENTS-Screw Holes



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Title	G92_V-BIOS_JTAG_Screw	
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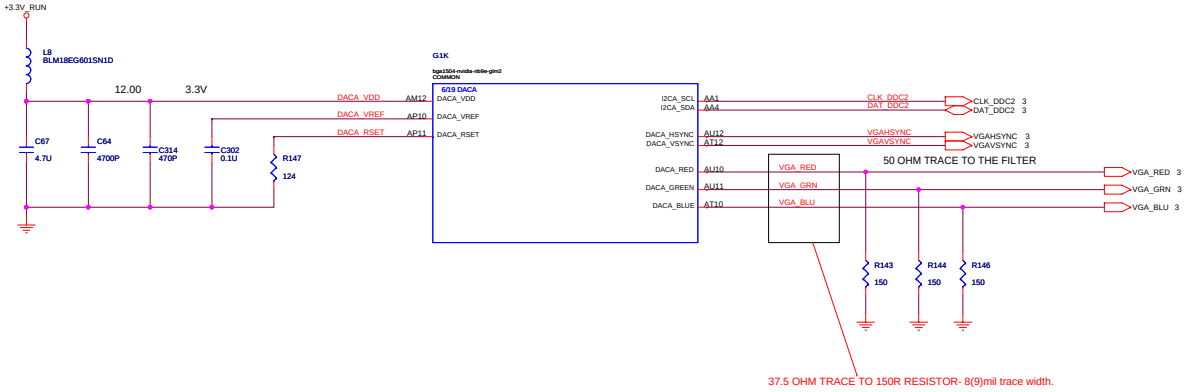
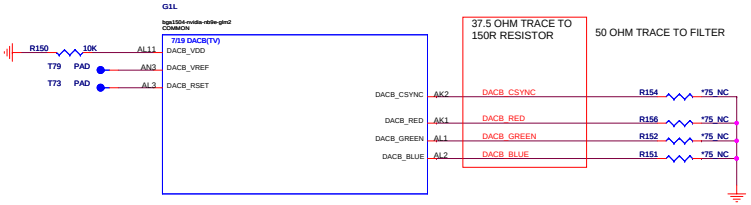
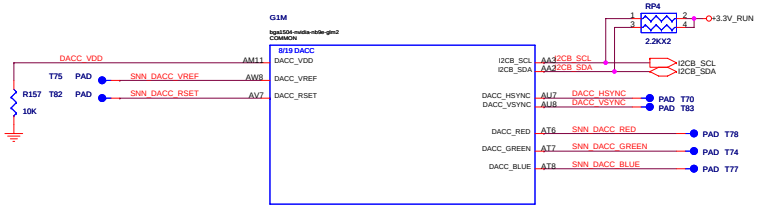
PRIMARY VGA (DAC A)



TV OUT (DAC B)



SECONDARY VGA (DAC C)--NO USING on Nike



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Title	G92_VGA_&_TV OUT	
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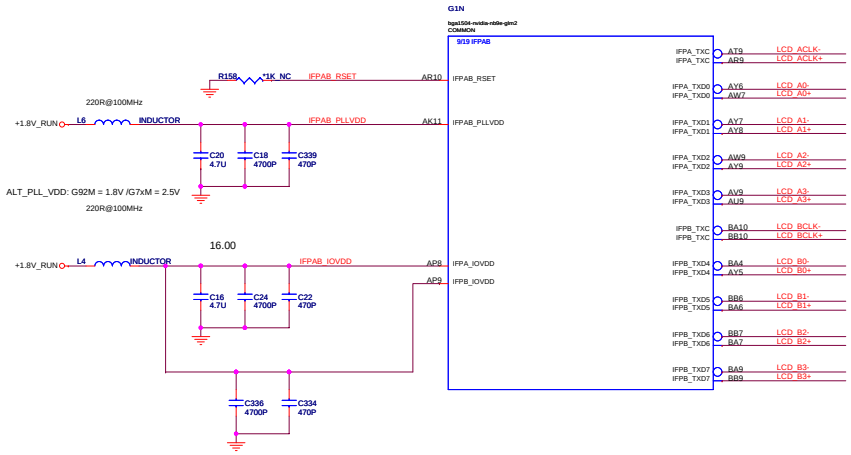
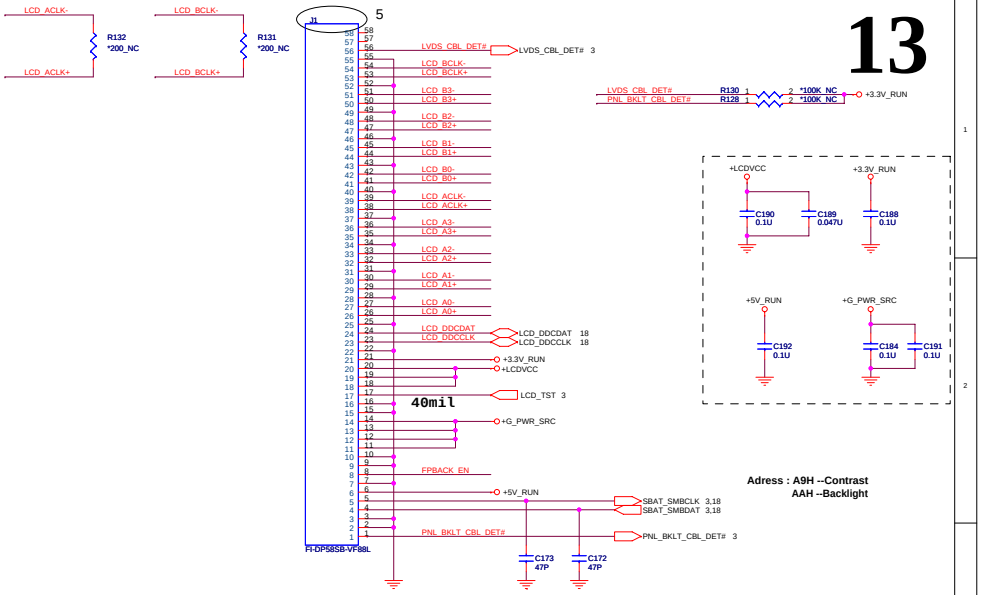
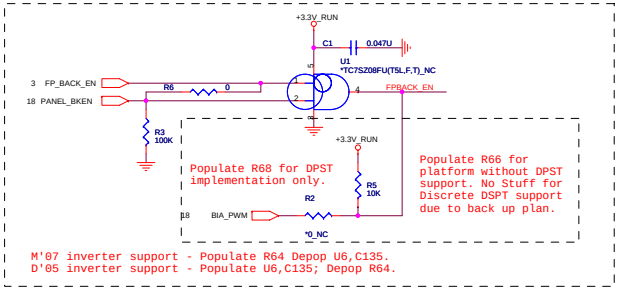
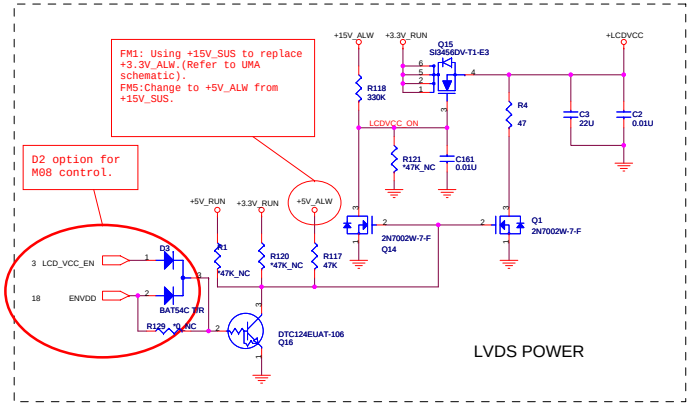
LVDS (LINK A/B) AND BACKLIGHT CONTROL





Adress : A9H --Contrast
AAH --Backlight





QUANTA COMPUTER

Title	G92_VGA_&_TV OUT	
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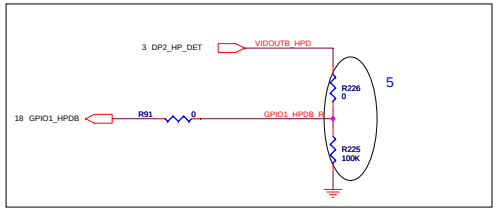

DP2

No using on G94.

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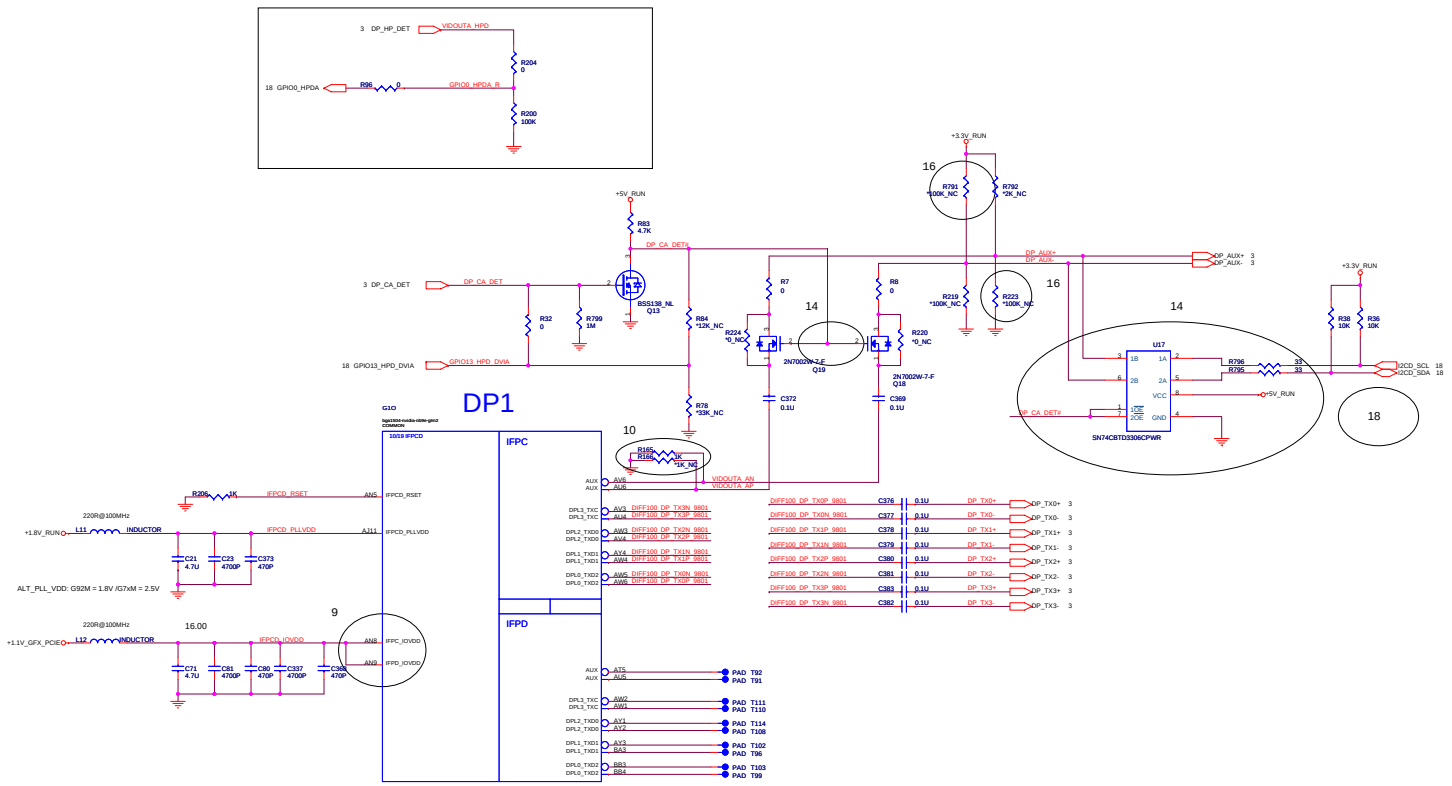

Title	9805_DP_Port_Txr		
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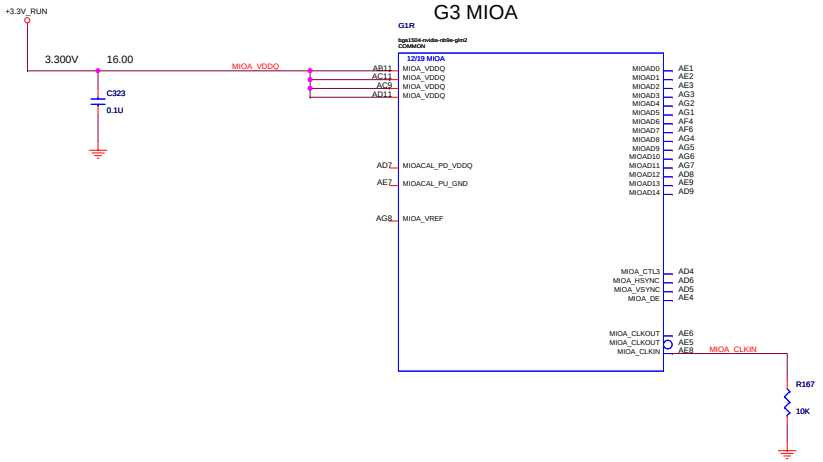
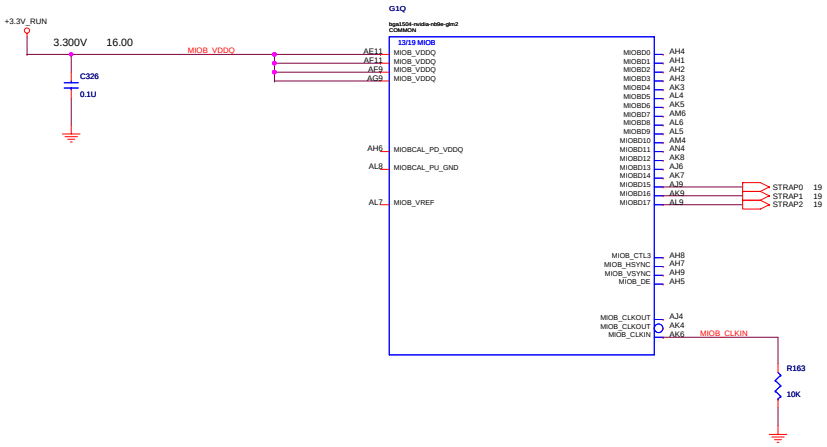
MIOA AND MIOB

G3 MIOA



G3 MIOB



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Title	G92_MIOA_&_MIOB	
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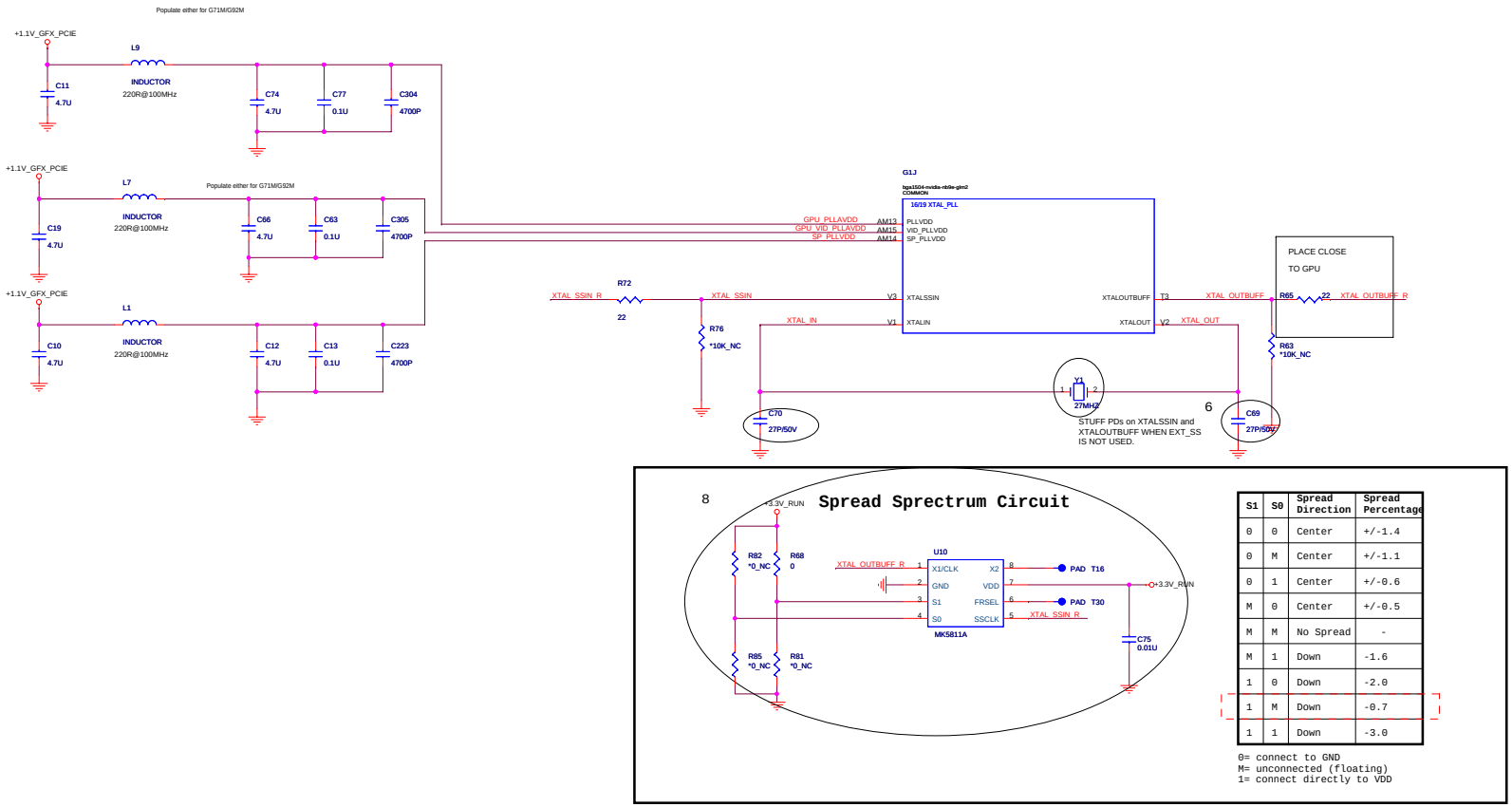
PLL VDD



8

Spread Sprectrum Circuit

S1	S0	Spread Direction	Spread Percentage
0	0	Center	+/-1.4
0	M	Center	+/-1.1
0	1	Center	+/-0.6
M	0	Center	+/-0.5
M	M	No Spread	-
M	1	Down	-1.6
1	0	Down	-2.0
1	M	Down	-0.7
1	1	Down	-3.0

0= connect to GND
M= unconnected (floating)
1= connect directly to VDD

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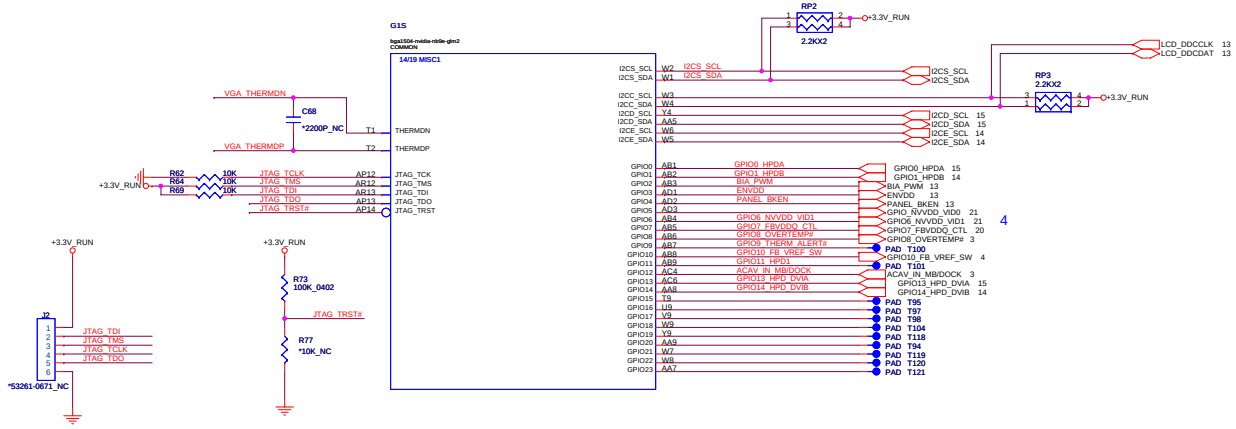
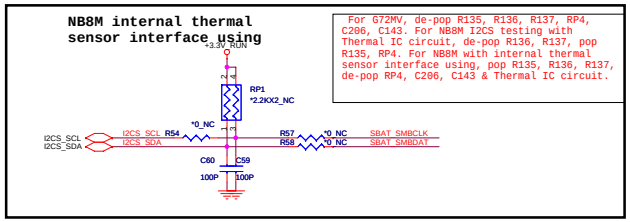
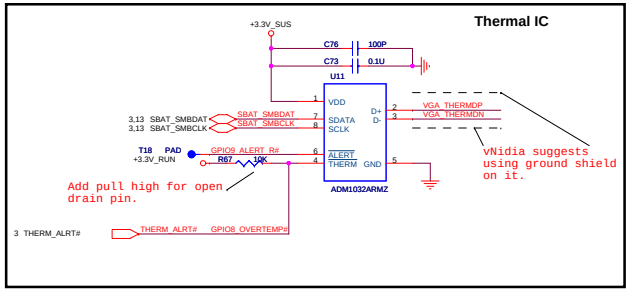
GPIOS, JTAG, TEMP SENSOR, FAN CONTROL, SPDIF, STATUS LED(S)







LOW VREF

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	OUT	LOW	OVER TEMP/GPU SHUTDOWN
9	OUT	LOW	THERMAL ALERT/FAM PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

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STRAPS

BIT

ROM_SI	0	RAMCFG_0	RAMCFG[3:0] 512MB (16Mx32) 1024MB (32Mx32) 0001 --- 256-bit Qimonda 0101 --- 256-bit Qimonda 0010 --- 256-bit Hynix 0110 --- 256-bit Hynix 0011 --- 256-bit Samsung 0111 --- 256-bit Samsung NOTE: See table 1 for the correct value/location of the ROM_SI resistor for the memory used
	1	RAMCFG_1	
	2	RAMCFG_2	
	3	RAMCFG_3	
ROM_SO	0	TVMODE_0	TVMODE[2:0] 000 --- DEFAULT XCLK_277 1 --- DEFAULT ROM_SO not required can be set in VBIOS See NOTE 2
	1	TVMODE_1	
	2	TVMODE_2	
	3	XCLK_277	
ROM_SCLK	0	PEX_PLL_EN_TERM100	PEX_PLL_EN_TERM100 0 --- DEFAULT SLOT_CLK_CFG 1 --- DEFAULT SUB_VENDOR 1 --- DEFAULT PCI_DEVID_EXT 0 --- DEFAULT See NOTE 2 See NOTE 3
	1	SLOT_CLK_CFG	
	2	SUB_VENDOR	
	3	PCI_DEVID_EXT	
STRAP0	0	USER_0	USER[3:0] (LVDS RESOLUTION OR EDID SELECT SWITCH) See Table 3 shown on the LVDS DISPLAY page which outlines the proper switch setting for the panel in use. NOTE: IF the LVDS panel is not in use the EDID MODE must be used else SW may prohibit other display outputs
	1	USER_1	
	2	USER_2	
	3	USER_3	
STRAP1	0	3GIO_PADCFG_LUT_ADR_0	3GIO_PADCFG_LUT_ADR[3:0] 0001 --- DEFAULT See NOTE 2
	1	3GIO_PADCFG_LUT_ADR_1	
	2	3GIO_PADCFG_LUT_ADR_2	
	3	3GIO_PADCFG_LUT_ADR_3	
STRAP2	0	PCI_DEVID_0	PCI_DEVID[3:0] BRING-UP SKU: Set the PCDEVID for the specifc GPU DEVID according to table 2 CUSTOMER SKU: Select the value/location of the strap 2 resistor for a specific GPU PCDEVID according to Table 1
	1	PCI_DEVID_1	
	2	PCI_DEVID_2	
	3	PCI_DEVID_3	

NOTE 2: See table 1 for the correct value/location of the strap resistor for the desired modes

NOTE 3: Bring-up SKU(s) have jumper configurable subvendor and DEVID_4 settings see the ROM_SCLK STRAP

TABLE 2: PCDEVID SWITCH SETTING DECODE
Switches are from left to right with the first switch being *

DVID # * 0 1 2 3 DEC	DVID # * 0 1 2 3 DEC
0 0 0 0 0	0 0 0 0 1 8
0 1 0 0 0 1	0 1 0 0 1 9
0 0 1 0 0 2	0 0 1 0 1 10
0 1 1 0 0 3	0 1 1 0 1 11
0 0 0 1 0 4	0 0 0 1 1 12
0 1 0 1 0 5	0 1 0 1 1 13
0 0 1 1 0 6	0 0 1 1 1 14
1 1 1 1 0 7	1 1 1 1 1 15

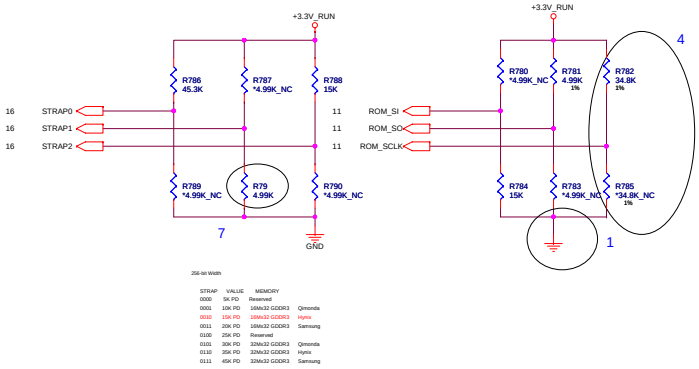
PCDEVID SWITCH LOGIC:
ON (closed / Switch down) = 0
OFF(OPEN / Switch Up) = 1

Note 1: DVID * always = 0 except for decimal 7 and 15 where it is set to 1 as shown.

Note 2: If PCDEVID[4]=0 needs to be 1 for a particular GPU DEVID, it is done by jumpering J21 1-2 (see below).

SEE the latest documentation for more details on G9x Straps!
For multi-level stuff the appropriate resistance to grnd or VDD as required
For Binary stuff the appropriate PU or PD as required,
Note: The correct refernce value must be used..
Don't use strap 0 or 2 options below if switches are used, Reserved for binary mode or no switch only

PCI_DEVID[4]/SUBVENDOR
Strap selectable



256-bit Width

STRAP	VALUE	MEMORY		
0000	5K PD	Reserved		
0001	10K PD	16Mx32 GDDR3	Qimonda	
0010	15K PD	16Mx32 GDDR3	Hynix	
0011	20K PD	16Mx32 GDDR3	Samsung	
0100	25K PD	Reserved		
0101	30K PD	32Mx32 GDDR3	Qimonda	
0110	35K PD	32Mx32 GDDR3	Hynix	
0111	45K PD	32Mx32 GDDR3	Samsung	

TABLE 1: STRAP DECODE ACCORDING TO
TERMINATION RESISTANCE/VOLTAGE

TERMINATION RESISTANCE	TERMINATION VOLTAGE 3V3 [3:0]	GND [3:0]
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110

EXAMPLE: 3GIO_PADCFG_LUT_ADR[3:0] is desired to be set to 0001
TABLE 1 shows that 0001 = a 10K resistance to GRND
so it is populated in the PD STRAP 1 position

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FBVDDQ

Thermal PAD is ground pin
It has to connect to ground

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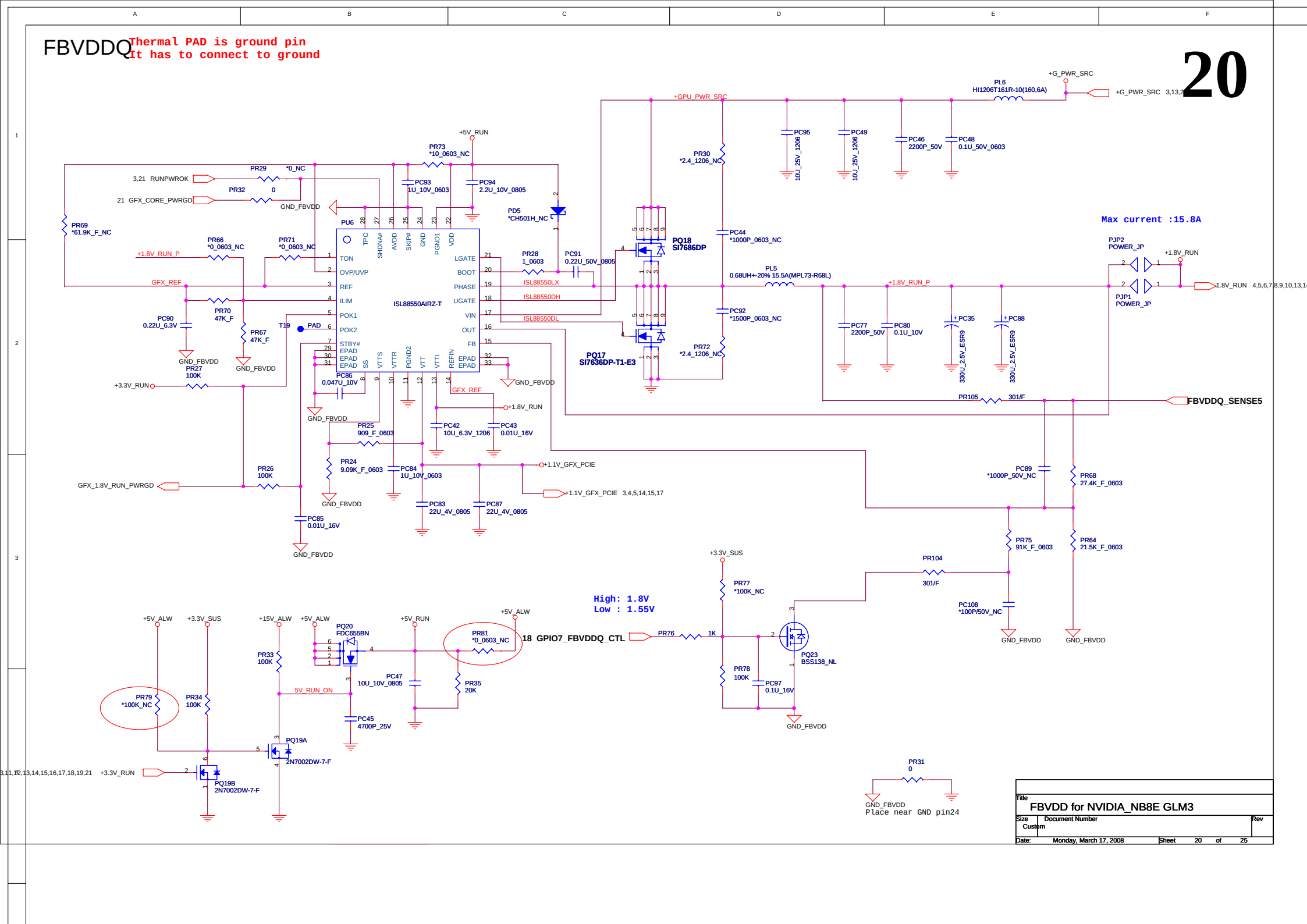

Title	FBVDD for NVIDIA_NB8E GLM3	
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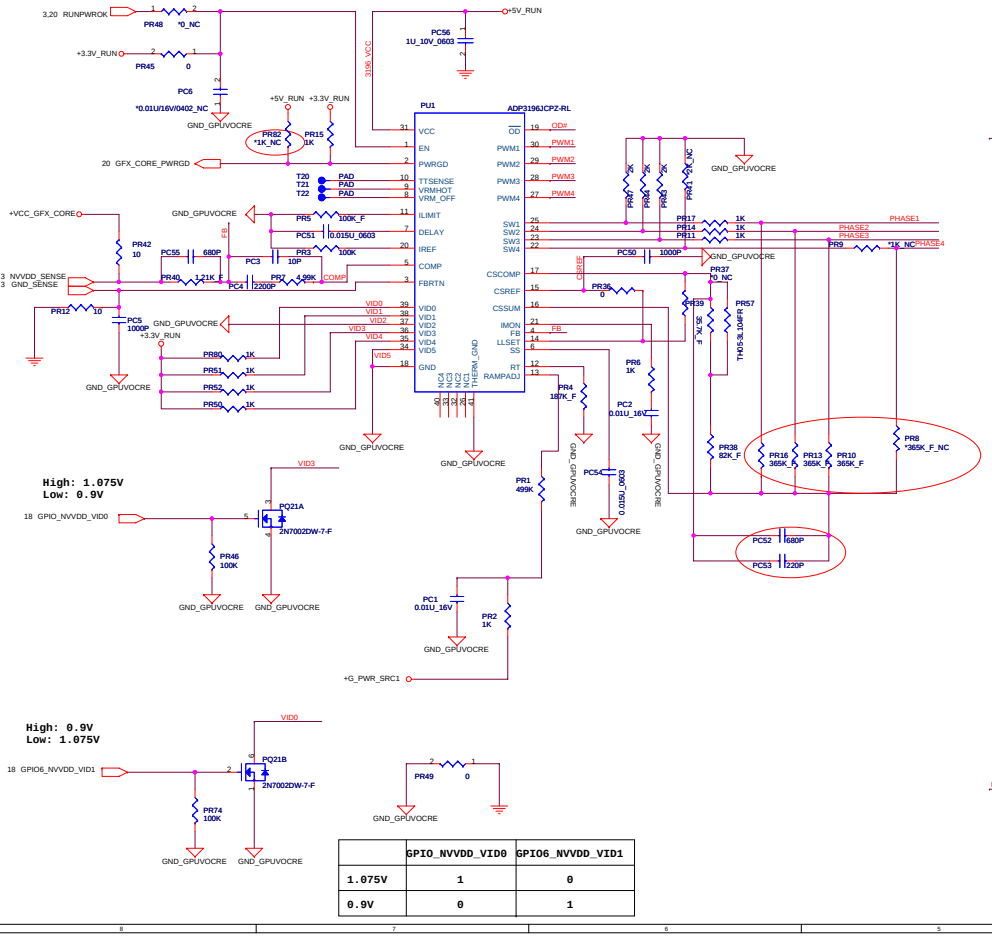
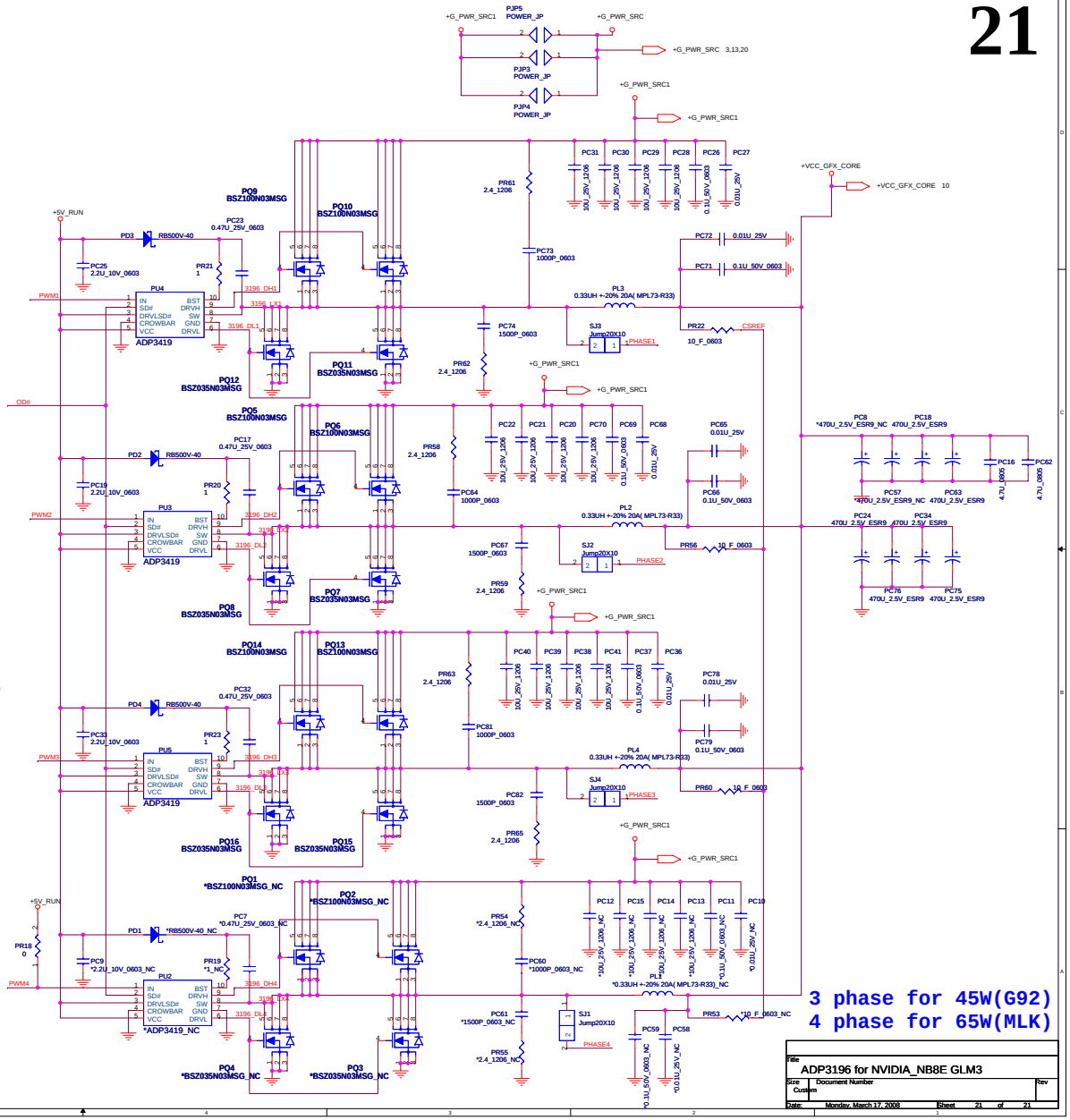
VID	5	4	3	2	1	0
1.55V	0	0	0	0	0	0
1.075V	0	1	0	0	1	1
1.05V	0	1	0	1	0	0
0.975V	0	1	0	1	1	1
0.95V	0	1	1	0	0	0
0.9V	0	1	1	0	1	0
0.85V	0	1	1	1	0	0



	GPIO_NVVDD_VID0	GPIO6_NVVDD_VID1
1.075V	1	0
0.9V	0	1



3 phase for 45W(G92)
4 phase for 65W(MLK)

Title	ADP3196 for NVIDIA_NB8E GLM3
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Model	Item	Page	Date	Rev.	Description
XM1 MB	1	P.19	0124	1A	Modify VRAM strapping circuit lose GND.
	2	6~9	0129	1A	The 16x32 pn used on NIke G94 is Nova die and will be EOL before Nike RTS.Change QCI PN from AKD5FWHTW00 to AKD5FWHTW03 and Mfr PN from HY5RS123235BFP-14 to H5RS5223CFR-11C.
	3	P.15	0129	1A	Aux+ pull down, Aux- pull up issue on DP1. Pop R223, R791 with 100K per Nvidia.
	4	P.19	0129	1A	Wrong Device ID setting: Depop R785. Pop R782 35K
	5	P.13	0225	1A	Change J1 footprint from LVDS-FI-DP58SB-VF100-58P-L to LVDS-FI-DP58SB-VF88L-58P-L.
	6	P.17	0304	1A	Per crystal test report, change C69 and C70 from 18p to 27p.
	7	P.19	0304	1A	Because Nike use desktop chipset.Change R79 from 10K to 5K for PCI-E interface high swing setting.
	8	P.17	0305	1A	Update SSC from P1819GF to MK5811A.
	9	P.14,15	0306	1A	DP workaround:need connect GPU ball AN9 and AN7 to +1.1V_GFX_PCIE also to slove DP can not display issue.
	10	P.14,15	0306	1A	Per PUN: Displayport aux channel workaround.
	11	P.20	0313	1A	Add PR79 (100K_NC), PR81(0_0603_NC)
	12	P.21	0313	1A	Add PR82 (1K_NC), PR16, PR13, PR10 and PR8 change from 93.1K to 365K, PC52 change to 680P, PC53 change to 220P
	13	NA	0313	1A	Update T23,T32,T55,T110,T111,T17 as TP3050.
	14	14,15	0314	1A	Update SW circuit.
	15	3	0314	1A	Per DPstatus report: Pop R39 to enable AVAC_IN_MB/DOCK.
	16	14,15	0314	1A	Per DPstatus report: Depop R223&R791 for DP1, R218&R793 for DP2
	17	11	0314	1A	Per DPstatus report: SPDIF voltage divider: Depop R109, R115, BAT54S-7-F, D2
	18	14,15	0317	1A	Update AUX SW schematic and remove RP5 and RP6.
	19	4	0317	1A	As PUN suggest .R136 should be change to 49.9ohm.
	20	14,15	0317	1A	As PUN suggest .Please change R197 and R202 to 2.2k ohm

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