# Topstar Digital technologies Co.,LTD

Board name: Mother Board Schematic
Project name: S42G
Version: VerD
Release Date: Jan.08, 2008

1. System Block Diagram & Schematic page description;
2. Power Block Diagram & Discription;
3. Annotations & information;
4. Schematic modify Item and history;
5. Power on & off Sequence;
6. ACPI Mode Switch Timings;
7. Power On Sequence Map;
8. CLOCK Distribution;
9. Power Distribution;

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Hardware drawing by: | Hardware check by: | EMI Check by:

Power drawing by: | Power check by:

Manager Sign by:

| | | | |
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| Page Name | Title | | |
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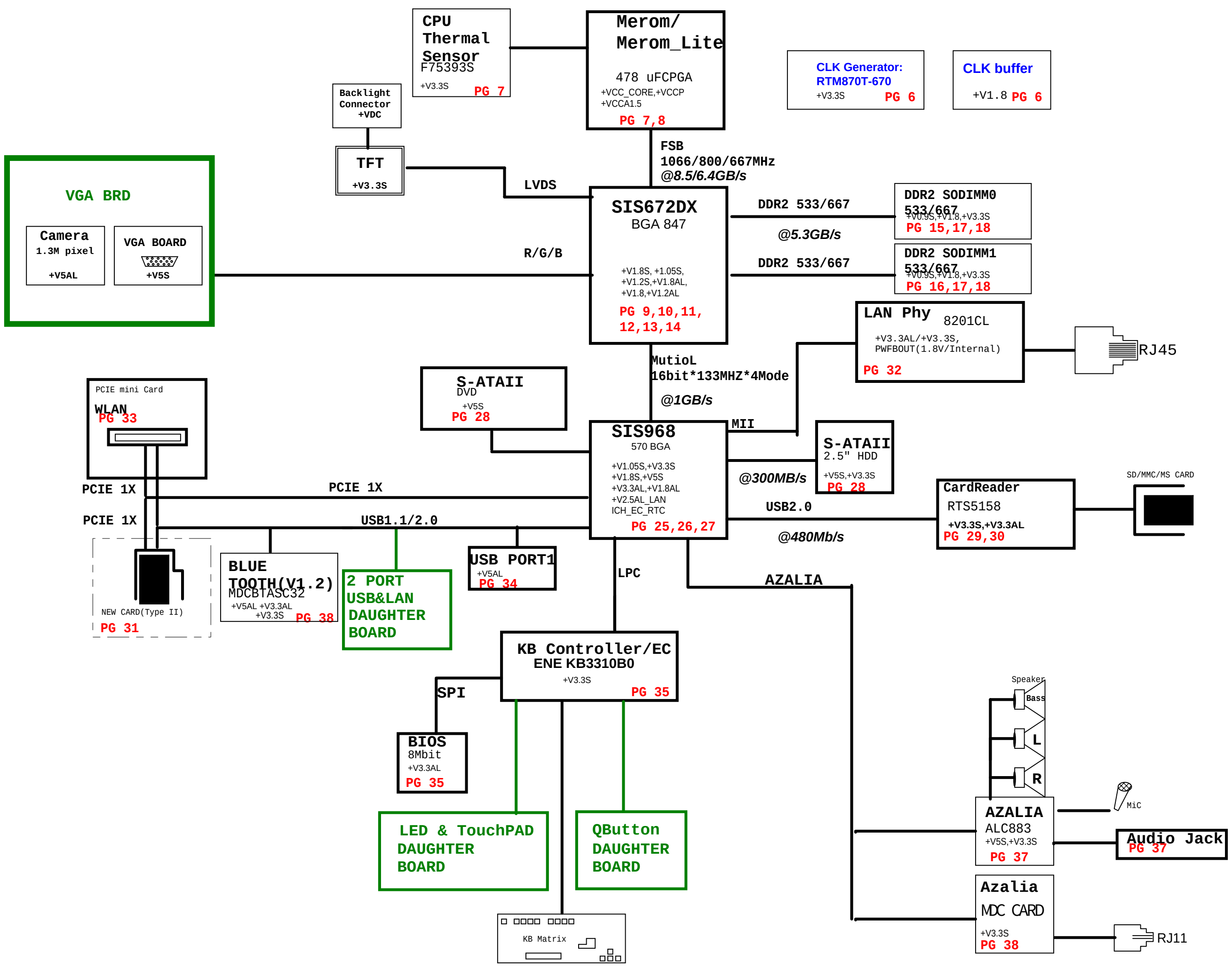
### S42C SYSTEM BLOCK Ver:A

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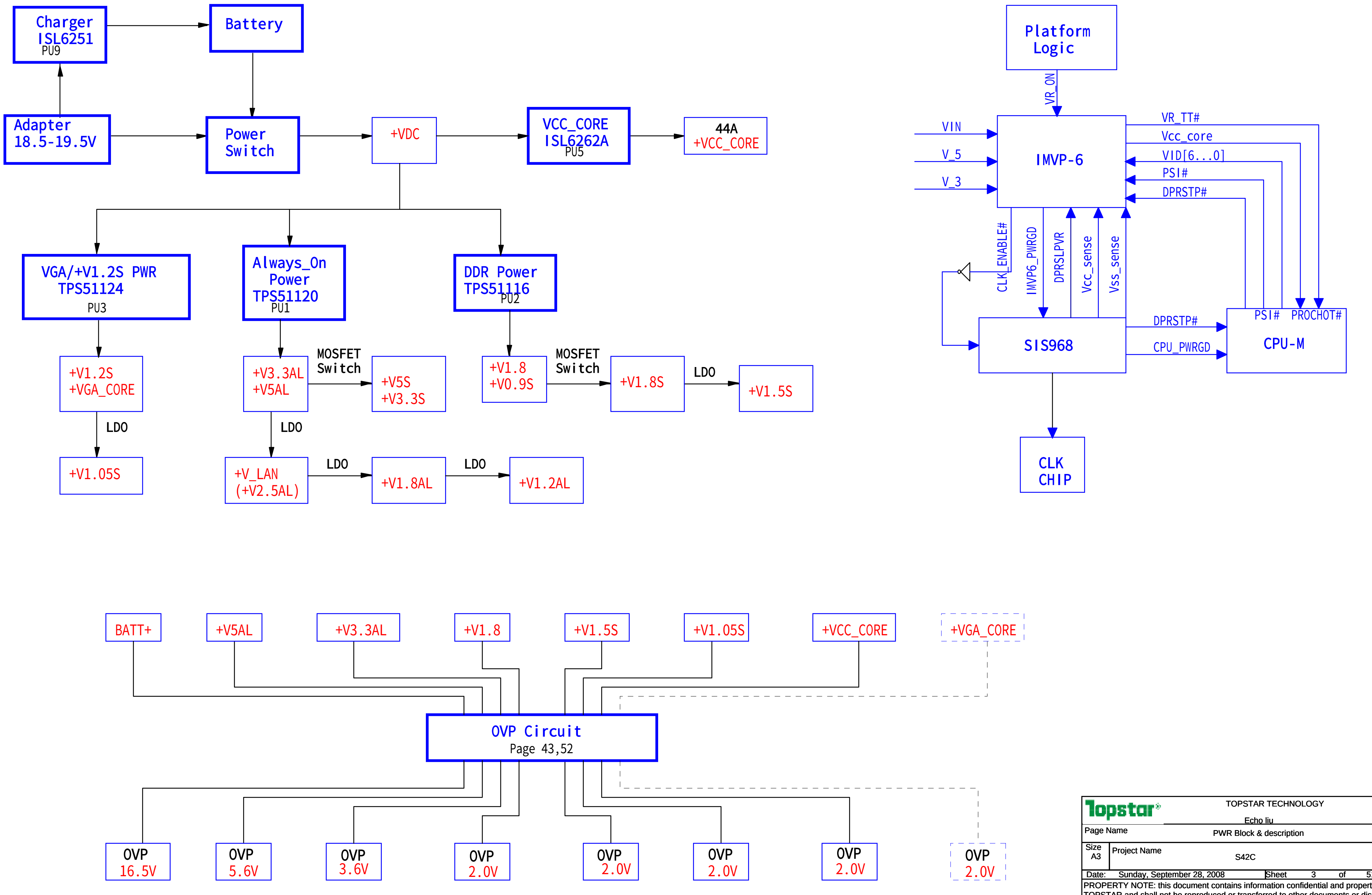
# S42C POWER BLOCK Ver:A

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## Voltage Rails

| | |
|---|---|
| +VDC | Primary DC system power supply(9V-19V) |
| +VCC_CORE | Core voltage for processor |
| +V1.5S | 1.5V for CPU PLL |
| +V1.05S | 1.05V for FSB VTT |
| +V0.9S | 0.9V DDR2 Termination voltage |
| +V1.8 | 1.8V power rail for DDR2 |
| +V3.3AL | 3.3V always on power rail |
| +V3.3S | 3.3V main power rail |
| +V5AL | 5V for USB Device |
| +V5S | 5V main power rail |
| +V1.2S | 1.2V PCIE IO,PLL,SIS671DX Core |
| +V1.8S | 1.8V SIS672/SIS968 Core/SATA/USB/PCIE |

## Board stack up description

| PCB Layers | Trace Impedence:55ohm +/-15%(Default) |
|---|---|
| TOP | |
| VCC | |
| IN1 | |
| IN2 | |
| GND | |
| Bottom | |

## USB Table

| USB Port# | Function Description |
|---|---|
| 0 | USB Port(on Main Board) |
| 1 | Mini PCIE Card(WLAN & ROBSON) |
| 2 | Express Card |
| 3 | USB CAMERA(On VGA Board) |
| 4 | Bluetooth |
| 5 | UB6232 CARD Reader |
| 6 | USB Port(on I/O Board) |
| 7 | USB Port(on I/O Board) |

## I2C SMB Address

| Device | Address | Hex | Bus | Master |
|---|---|---|---|---|
| Clock Generator | 1101 111x | D2 | SMB_ICH_S | SIS968 |
| SO-DIMM0 | 1010 000x | A0 | SMB_ICH_S | SIS968 |
| SO-DIMM1 | 1010 001x | A2 | SMB_ICH_S | SIS968 |
| NEW CARD | Variable | Variable | SMB_ICH_S | SIS968 |
| PCIE Mini CARD | Variable | Variable | SMB_ICH_S | SIS968 |
| Smart Battery | 0001 011x | 16 | I2C_591 | Embeded Controller(EC) Pin169/170 |
| CPU Thermal Sensor(F75383S) | 1001 100x | 98 | I2C_591 | Embeded Controller(EC) Pin163/164 |

## PCI Devices

```
Bus # Device # Function # Device ID IDSEL INTX Device Function
SIS968:
Bus 0 Device 2 Function 0 0008h AD13 N/A LPC
Bus 0 Device 2 Function 5 5513h/1180h/1181h AD13 INTA IDE
Bus 0 Device 3 Function 0 7001h AD14 INTE USB 1.1 #0
Bus 0 Device 3 Function 1 7001h AD14 INTF USB 1.1 #1
Bus 0 Device 3 Function 3 7002h AD14 INTG USB 2.0
Bus 0 Device 4 Function 0 0191h AD15 INTD LAN
Bus 0 Device 5 Function 0 1183h/1184h/1185h AD16 INTB SATA
Bus 0 Device 6 Function 0 000Ah AD17 INTA/B/C/D PCI Express 0
Bus 0 Device 7 Function 0 000Ah AD18 INTA/B/C/D PCI Express 1
Bus 0 Device F Function 0 7502h AD26 INTC HD Audio
SIS672:
Bus 0 Device 0 Function 0 0671h AD11 North Bridge
Bus 0 Device 31 Function 0 0004h AD31 Virtual PCI-to-PCI Bridge for
PCI-Express device
Onboard Devide:NON
```

## Power States/AC mode

| Signal | SLP_S3# | SLP_S4# | SLP_S5# | +V*AL | +V* | +V*S | Clock |
|---|---|---|---|---|---|---|---|
| S0(Full On) | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S3(STM) | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4(STD) | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5(SoftOff) | LOW | LOW | LOW | ON | OFF | OFF | OFF |

## Wake up Events

Wake up by LAN/968GMAC Internal
LID switch from EC
Power switch from EC

**ns: Component marked "ns" is not stuff**

**This is a lead free project,all component must be LF**

| | | |
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# Schematic modify Item and history:

## 2007-08-31 Ver A initial release

## 2007-02-09 Ver B Change List

1.PG6 C218,C212,C331,C341 footprint from 1206 to 0805.Add C622,C623,C119,C120,C128 for EMI reserved.

2.PG6 Clock Enable : change R156 from 10K to 51K,ns C344,install C142

3.PG6 FSB : Add R673 and R674, ns R148,R151 ,R145,install R155 and R147.

4.PG11 : Change C573 and C574 net from DACAVDD2 to DACAVDD1

5.PG15 Add DIMM2 and surrounding Capacitor

6.PG21 : Add clear_cmos point.

7.PG22 : Change R421 value from 127 to 130 Ohm

8.PG26 Power Switch: Add Power Switch and surrounding circuit.

9.PG29 USB: Delete CHK3, and R331 and R329

10.PG30: PCB version from A to B

## 2007-03-09 Ver C Change List

1.PG19: Change VGA Connector

2.PG30: PCB version from B to C

## 2007-04-29 Ver D Change List

1. PG32 & PG21:Add modem and surrounding circuit
2. PG30: PCB version from C to D,Reserved R691
3. PG44:Change H3,H7 and H9 footprint from TH_315_112 to TH_315_118
4. PG33:Co-lay PD5 and PD8
5. PG36:Co-lay PC164

## 2007-05-28 Ver E Change List

1.改了板边,升级PCB的料号从VerD到VerE.

## 2008-09-11 Ver F Change List

1.改了板边,升级PCB的料号从VerD到VerE.

## 2008-09-22 S42C Ver A Change List,主要换了realtek clock和新EC（KB3310B）

1. Delete CLKGEN_PWRGD circuit, NS R124,pull high PECLK2/3/5_REQ# and STOP_PCI_L#.
2. pull high CPU_STOP# because of no C3 and C4 function to realtek clock,change 56 ohm parallel resistor to 0 ohm paraller resistor.
3. R24,R26 footprint from 0603 to 0402
4. Delete paraller DVD net,and pull down or up according to SIS FAE suggest.
5. Reserved SPI BIOS ROM for SIS968, add R170
6. Delete LDRQ# off connector and R148,Delete reserved power on/S3/S4 control circuit.
7. Delete parallel DVD net add pull down or up according to SIS FAE suggest
8. Add reserved SPI ROM
9. Add SATA ODD,NS Q40 and R481,NS PQ58 and R489
10. 添加SATA DVD的Connector
11. Delete Co-layout card reader connector.
12. Delete Co-layout Newcard powerswitch circuit
13. Change minipcie according to minipcie 1.2 spec
14. change EC form 87541 to KB3310B
15. Delete CD_IN circuit.
16. 删掉BAT_TEM circuit
17. 根据采购以及CE的意见，更改F75383 to F75393, U16 from ATMEL to SEIKO,U15 from RICHON to ENE,PU5 from KIA to APEC.
18. 根据采购意见，更换CPU Vcore的Mosfet。

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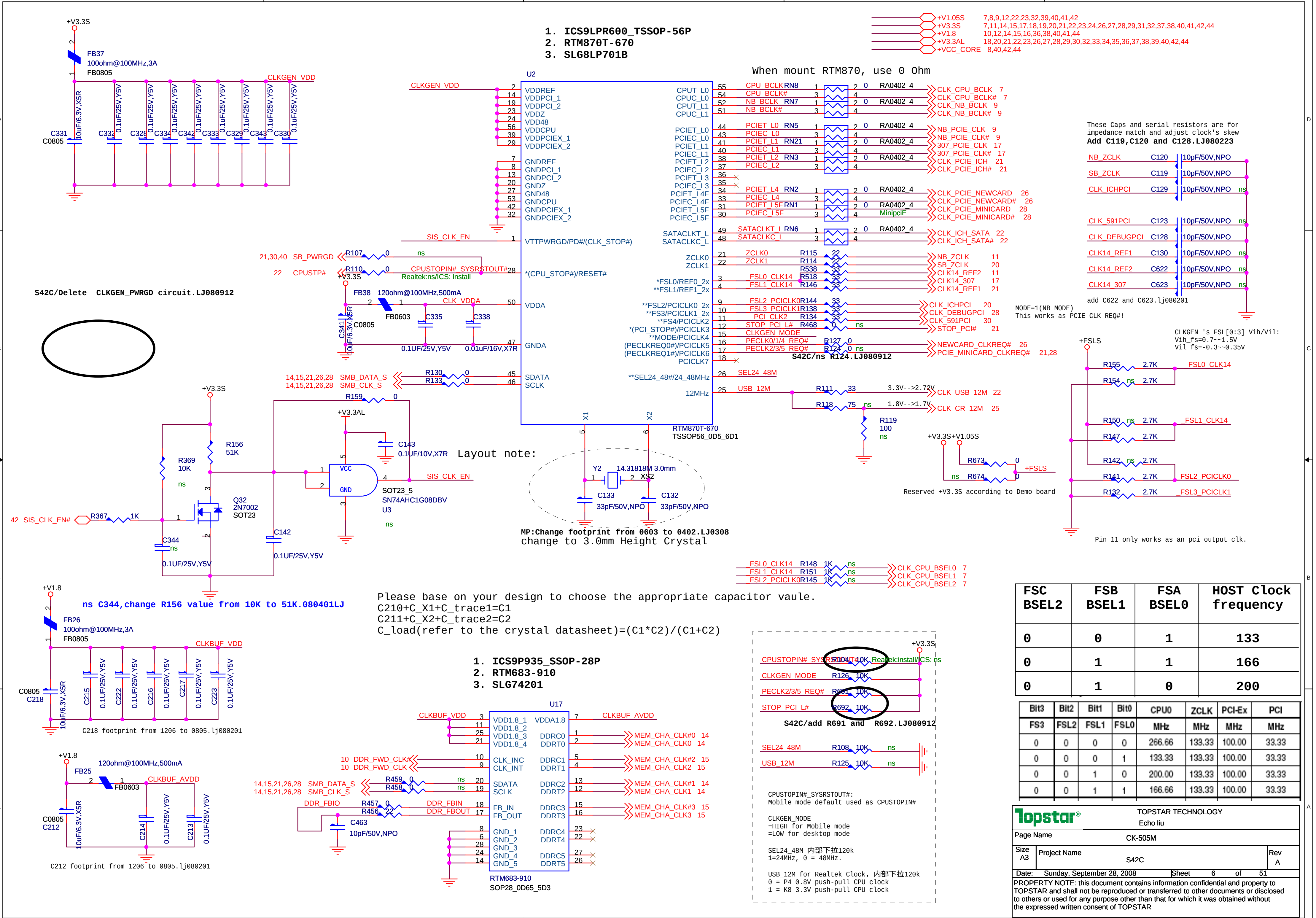


| FSC BSEL2 | FSB BSEL1 | FSA BSEL0 | HOST Clock frequency |
|---|---|---|---|
| 0 | 0 | 1 | 133 |
| 0 | 1 | 1 | 166 |
| 0 | 1 | 0 | 200 |

| Bit3 | Bit2 | Bit1 | Bit0 | CPU0 | ZCLK | PCI-Ex | PCI |
|---|---|---|---|---|---|---|---|
| FS3 | FSL2 | FSL1 | FSL0 | MHz | MHz | MHz | MHz |
| 0 | 0 | 0 | 0 | 266.66 | 133.33 | 100.00 | 33.33 |
| 0 | 0 | 0 | 1 | 133.33 | 133.33 | 100.00 | 33.33 |
| 0 | 0 | 1 | 0 | 200.00 | 133.33 | 100.00 | 33.33 |
| 0 | 0 | 1 | 1 | 166.66 | 133.33 | 100.00 | 33.33 |

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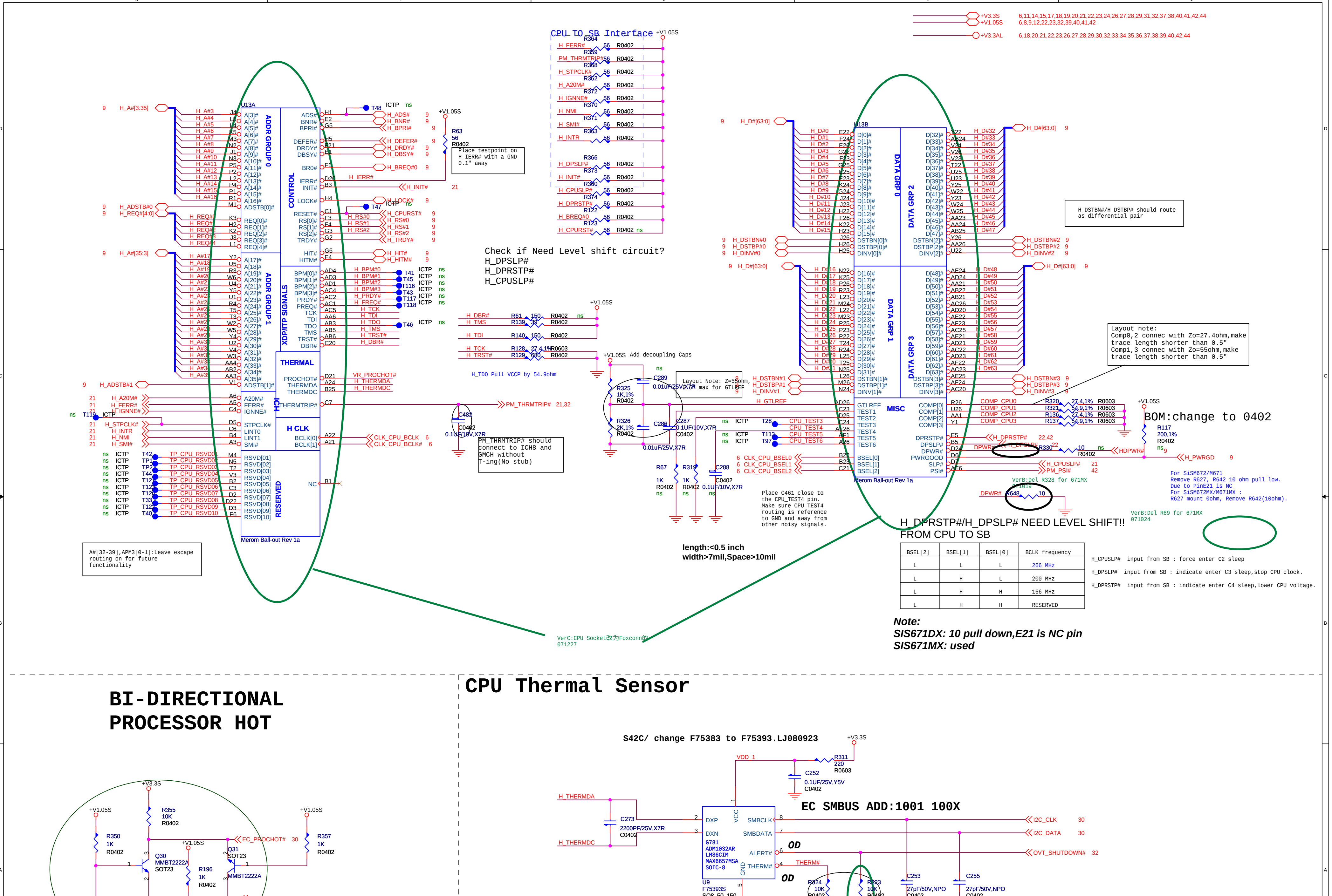


| BSEL[2] | BSEL[1] | BSEL[0] | BCLK frequency |
|---|---|---|---|
| L | L | L | 266 MHz |
| L | H | L | 200 MHz |
| L | H | H | 166 MHz |
| L | H | H | RESERVED |

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| | | |
|---|---|---|
| Page Name | Merom CPU(1of2)(Host BUS) | |
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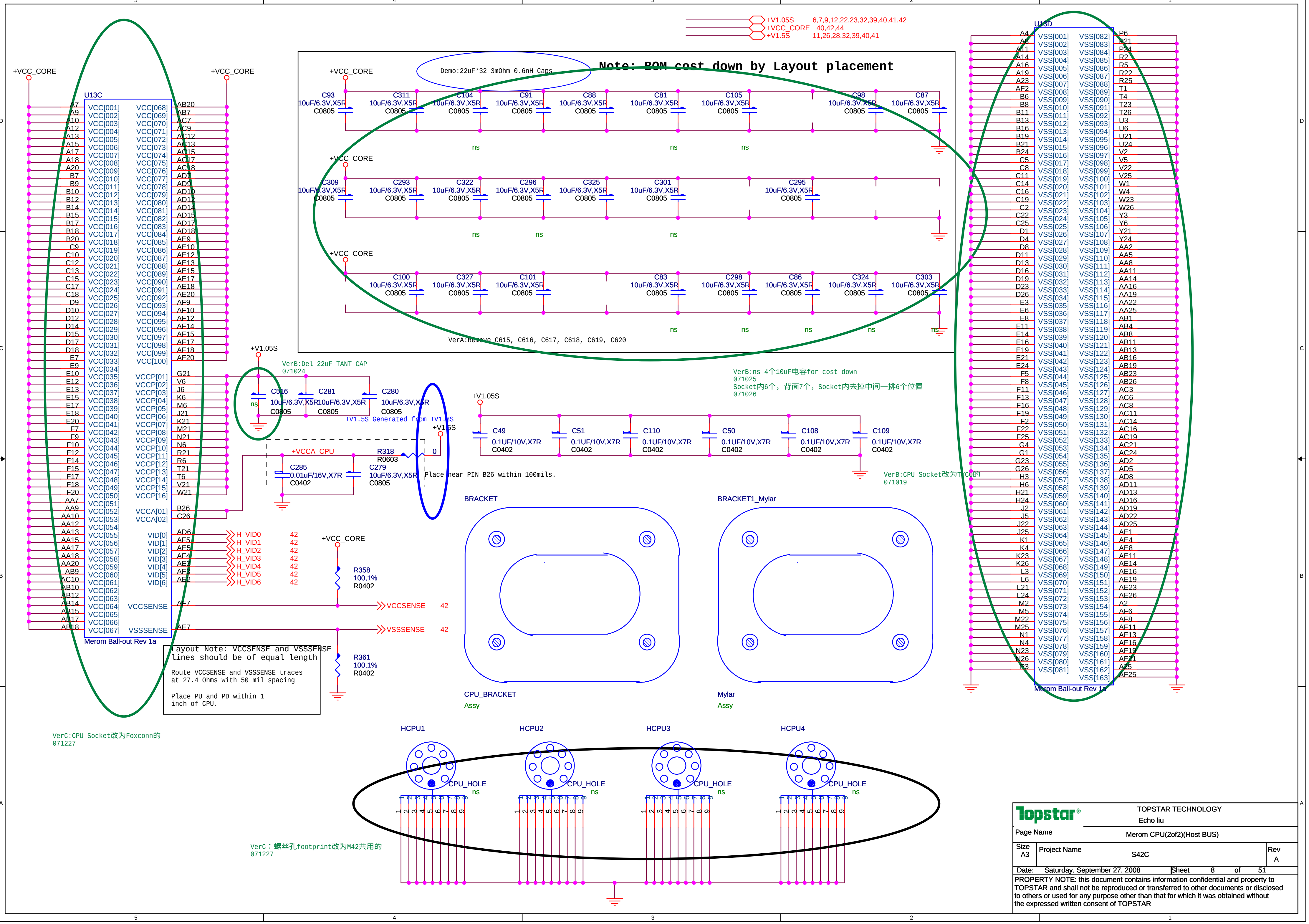

+V1.05S 6,7,9,12,22,23,32,39,40,41,42
+VCC_CORE 40,42,44
+V1.5S 11,26,28,32,39,40,41
Note: BOM cost down by Layout placement
Demo:22uF*32 3mOhm 0.6nH Caps
+VCC_CORE
U13C
Merom Ball-out Rev 1a
U13D
Merom Ball-out Rev 1a
C93 C311 C104 C91 C88 C81 C105 C98 C87
C309 C293 C322 C296 C325 C301 C295
C100 C327 C101 C83 C298 C86 C324 C303
10uF/6.3V,X5R
C0805
ns
VerA:Remove C615, C616, C617, C618, C619, C620
+V1.05S
VerB:Del 22uF TANT CAP
071024
C516 C281 C280
+V1.5S Generated from +V1.5S
+VCCA_CPU
R318
R0603
0
C285
0.01uF/16V,X7R
C0402
C279
Place near PIN B26 within 100mils.
C49 C51 C110 C50 C108 C109
0.1UF/10V,X7R
C0402
VerB:ns 4个10uF电容for cost down
071025
Socket内6个，背面7个，Socket内去掉中间一排6个位置
071026
VerB:CPU Socket改为TYCO的
071019
H_VID0 H_VID1 H_VID2 H_VID3 H_VID4 H_VID5 H_VID6 42
R358
100,1%
R0402
VCCSENSE 42
VSSSENSE 42
R361
100,1%
R0402
Layout Note: VCCSENSE and VSSSENSE lines should be of equal length
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing
Place PU and PD within 1 inch of CPU.
BRACKET
CPU_BRACKET
Assy
BRACKET1_Mylar
Mylar
Assy
VerC:CPU Socket改为Foxconn的
071227
HCPU1 HCPU2 HCPU3 HCPU4
CPU_HOLE
VerC：螺丝孔footprint改为M42共用的
071227
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Merom CPU(2of2)(Host BUS)
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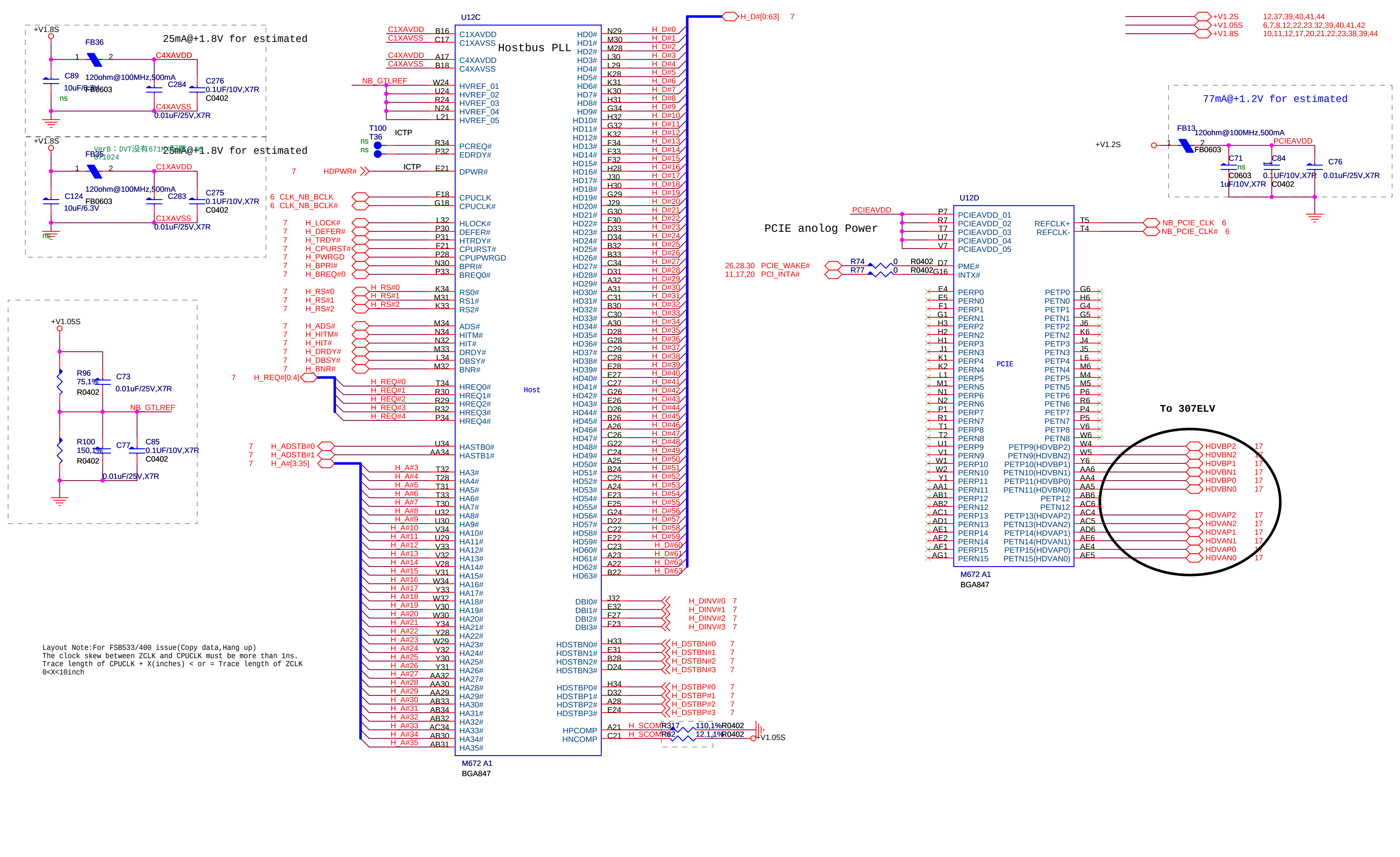


Layout Note:For FSB533/400 issue(Copy data,Hang up)
The clock skew between ZCLK and CPUCLK must be more than 1ns.
Trace length of CPUCLK + X(inches) < or = Trace length of ZCLK
0<X<10inch

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| | | |
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| Page Name | Crestline(HOST) | |
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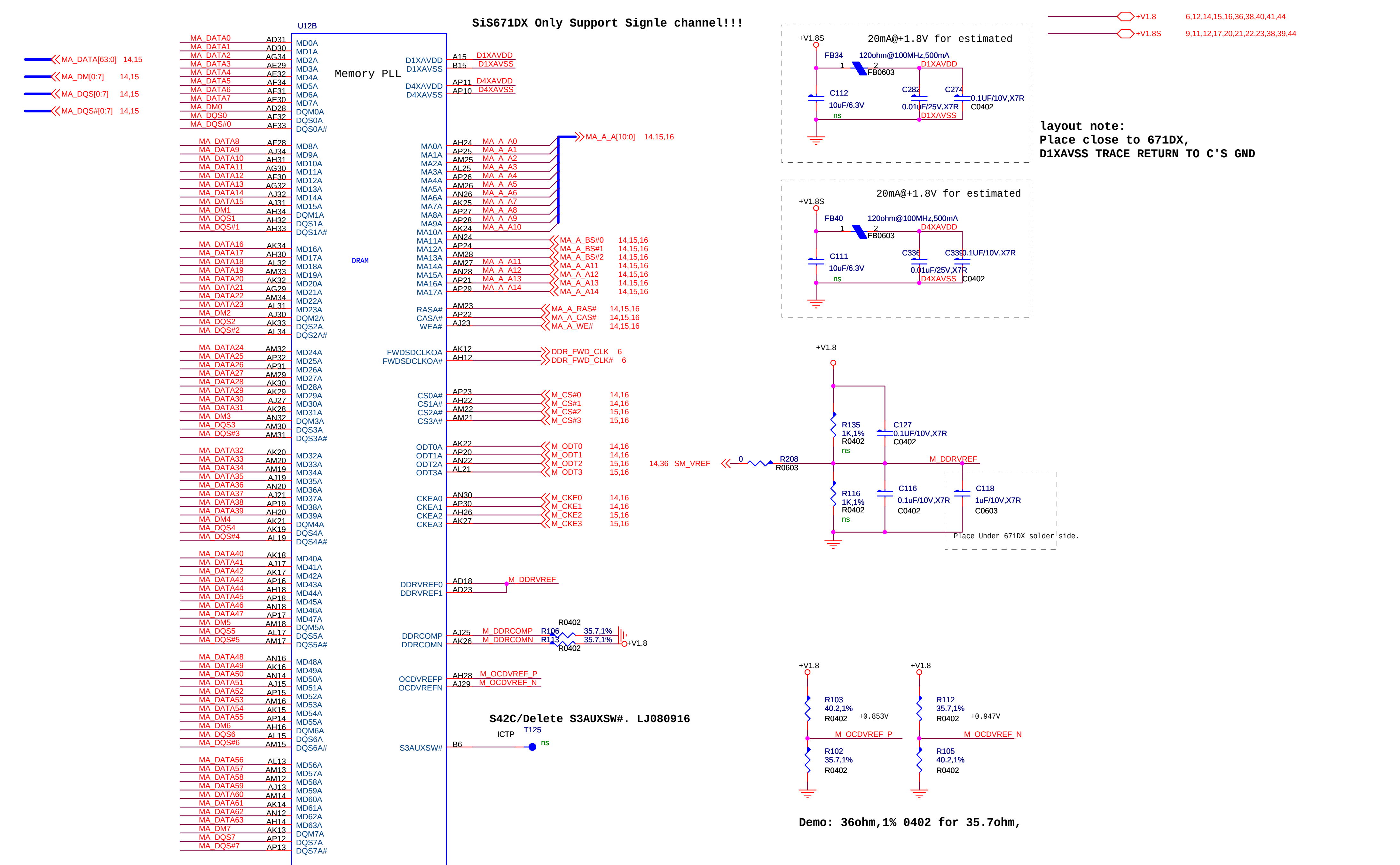


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Page Name: Crestline(DDRII)

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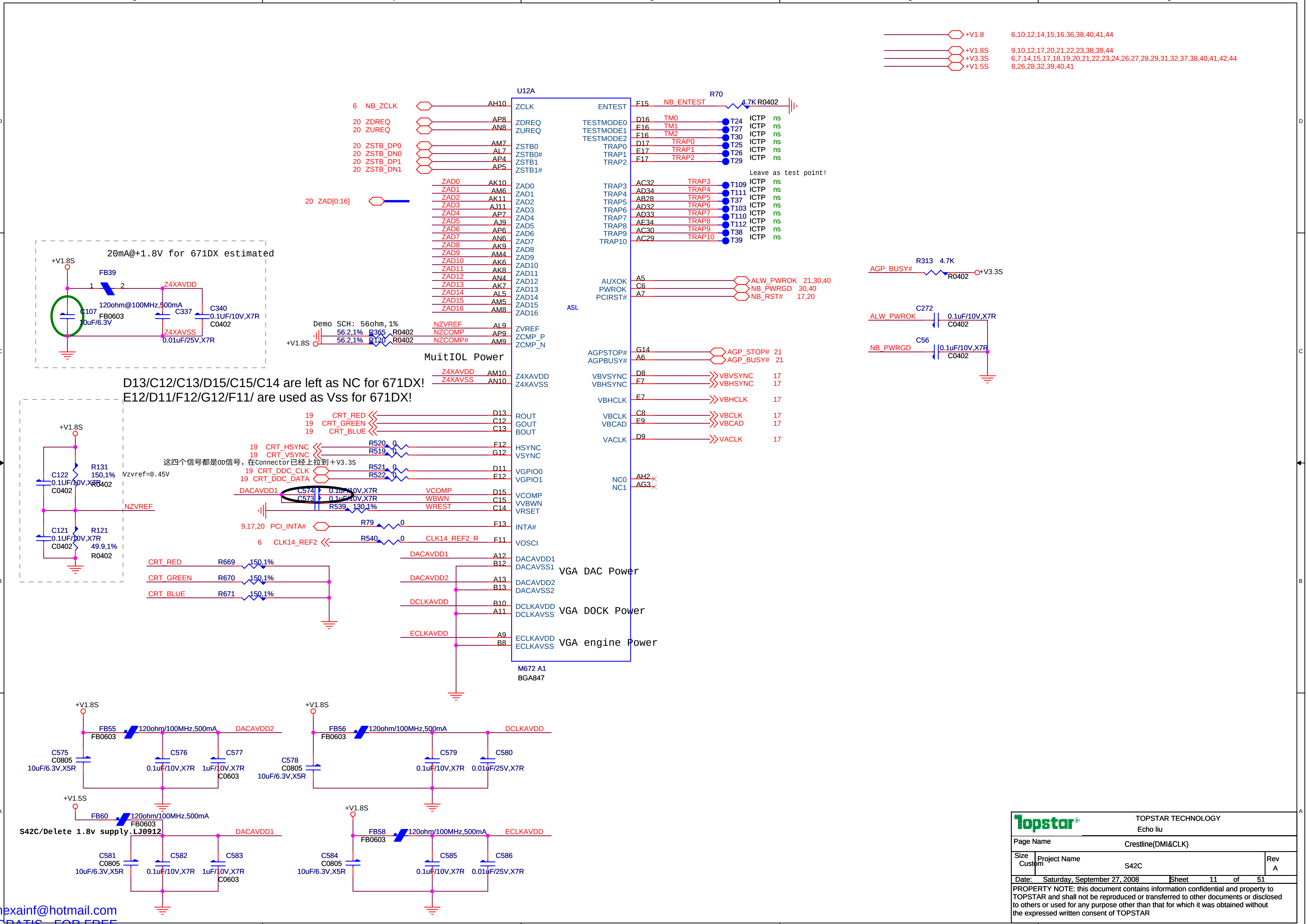

+V1.8 6,10,12,14,15,16,36,38,40,41,44
+V1.8S 9,10,12,17,20,21,22,23,38,39,44
+V3.3S 6,7,14,15,17,18,19,20,21,22,23,24,26,27,28,29,31,32,37,38,40,41,42,44
+V1.5S 8,26,28,32,39,40,41
U12A
M672 A1
BGA847
6 NB_ZCLK AH10 ZCLK
20 ZDREQ AP8 ZDREQ
20 ZUREQ AN8 ZUREQ
20 ZSTB_DP0 AM7 ZSTB0
20 ZSTB_DN0 AL7 ZSTB0#
20 ZSTB_DP1 AP4 ZSTB1
20 ZSTB_DN1 AP5 ZSTB1#
20 ZAD[0:16]
ZAD0 AK10 ZAD0
ZAD1 AM6 ZAD1
ZAD2 AK11 ZAD2
ZAD3 AJ11 ZAD3
ZAD4 AP7 ZAD4
ZAD5 AJ9 ZAD5
ZAD6 AP6 ZAD6
ZAD7 AN6 ZAD7
ZAD8 AK9 ZAD8
ZAD9 AM4 ZAD9
ZAD10 AK6 ZAD10
ZAD11 AK8 ZAD11
ZAD12 AN4 ZAD12
ZAD13 AK7 ZAD13
ZAD14 AL5 ZAD14
ZAD15 AM5 ZAD15
ZAD16 AM8 ZAD16
Demo SCH: 56ohm,1%
NZVREF AL9 ZVREF
NZCOMP AP9 ZCMP_P
NZCOMP# AM9 ZCMP_N
R365 56.2,1% R0402
R120 56.2,1% R0402
+V1.8S
MuitIOL Power
Z4XAVDD AM10 Z4XAVDD
Z4XAVSS AN10 Z4XAVSS
ENTEST F15 NB_ENTEST R70 4.7K R0402
TESTMODE0 D16 TM0 T24 ICTP ns
TESTMODE1 E16 TM1 T27 ICTP ns
TESTMODE2 F16 TM2 T30 ICTP ns
TRAP0 D17 TRAP0 T25 ICTP ns
TRAP1 E17 TRAP1 T26 ICTP ns
TRAP2 F17 TRAP2 T29 ICTP ns
Leave as test point!
TRAP3 AC32 TRAP3 T109 ICTP ns
TRAP4 AD34 TRAP4 T111 ICTP ns
TRAP5 AB28 TRAP5 T37 ICTP ns
TRAP6 AD32 TRAP6 T103 ICTP ns
TRAP7 AD33 TRAP7 T110 ICTP ns
TRAP8 AE34 TRAP8 T112 ICTP ns
TRAP9 AC30 TRAP9 T38 ICTP ns
TRAP10 AC29 TRAP10 T39 ICTP ns
AUXOK A5 ALW_PWROK 21,30,40
PWROK C6 NB_PWRGD 30,40
PCIRST# A7 NB_RST# 17,20
ASL
AGPSTOP# G14 AGP_STOP# 21
AGPBUSY# A6 AGP_BUSY# 21
VBVSYNC D8 VBVSYNC 17
VBHSYNC F7 VBHSYNC 17
VBHCLK E7 VBHCLK 17
VBCLK C8 VBCLK 17
VBCAD E9 VBCAD 17
VACLK D9 VACLK 17
NC0 AH2
NC1 AG3
AGP_BUSY# R313 4.7K R0402 +V3.3S
ALW_PWROK C272 0.1UF/10V,X7R C0402
NB_PWRGD C56 0.1UF/10V,X7R C0402
20mA@+1.8V for 671DX estimated
+V1.8S FB39 1 2 120ohm@100MHz,500mA FB0603
Z4XAVDD C107 10uF/6.3V C337 C340 0.1UF/10V,X7R C0402
Z4XAVSS 0.01uF/25V,X7R
D13/C12/C13/D15/C15/C14 are left as NC for 671DX!
E12/D11/F12/G12/F11/ are used as Vss for 671DX!
19 CRT_RED D13 ROUT
19 CRT_GREEN C12 GOUT
19 CRT_BLUE C13 BOUT
19 CRT_HSYNC R520 0 F12 HSYNC
19 CRT_VSYNC R519 0 G12 VSYNC
这四个信号都是OD信号，在Connector已经上拉到+V3.3S
19 CRT_DDC_CLK R521 0 D11 VGPIO0
19 CRT_DDC_DATA R522 0 E12 VGPIO1
DACAVDD1 C574 0.1uF/10V,X7R VCOMP D15 VCOMP
C573 0.1uF/10V,X7R WBWN C15 VVBWN
R539 130,1% WREST C14 VRSET
9,17,20 PCI_INTA# R79 0 F13 INTA#
6 CLK14_REF2 R540 0 CLK14_REF2_R F11 VOSCI
DACAVDD1 A12 DACAVDD1
B12 DACAVSS1
VGA DAC Power
DACAVDD2 A13 DACAVDD2
B13 DACAVSS2
DCLKAVDD B10 DCLKAVDD
A11 DCLKAVSS
VGA DOCK Power
ECLKAVDD A9 ECLKAVDD
B8 ECLKAVSS
VGA engine Power
+V1.8S
C122 0.1UF/10V,X7R C0402
R131 150,1% R0402
Vzvref=0.45V
NZVREF
C121 0.1UF/10V,X7R C0402
R121 49.9,1% R0402
CRT_RED R669 150,1%
CRT_GREEN R670 150,1%
CRT_BLUE R671 150,1%
+V1.8S FB55 FB0603 120ohm/100MHz,500mA DACAVDD2
C575 C0805 10uF/6.3V,X5R
C576 0.1uF/10V,X7R
C577 1uF/10V,X7R C0603
+V1.8S FB56 FB0603 120ohm/100MHz,500mA DCLKAVDD
C578 C0805 10uF/6.3V,X5R
C579 0.1uF/10V,X7R
C580 0.01uF/25V,X7R
+V1.5S FB60 120ohm/100MHz,500mA FB0603
S42C/Delete 1.8v supply.LJ0912
DACAVDD1
C581 C0805 10uF/6.3V,X5R
C582 0.1uF/10V,X7R
C583 1uF/10V,X7R C0603
+V1.8S FB58 FB0603 120ohm/100MHz,500mA ECLKAVDD
C584 C0805 10uF/6.3V,X5R
C585 0.1uF/10V,X7R
C586 0.01uF/25V,X7R
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Page Name Crestline(DMI&CLK)
Size Custom Project Name S42C Rev A
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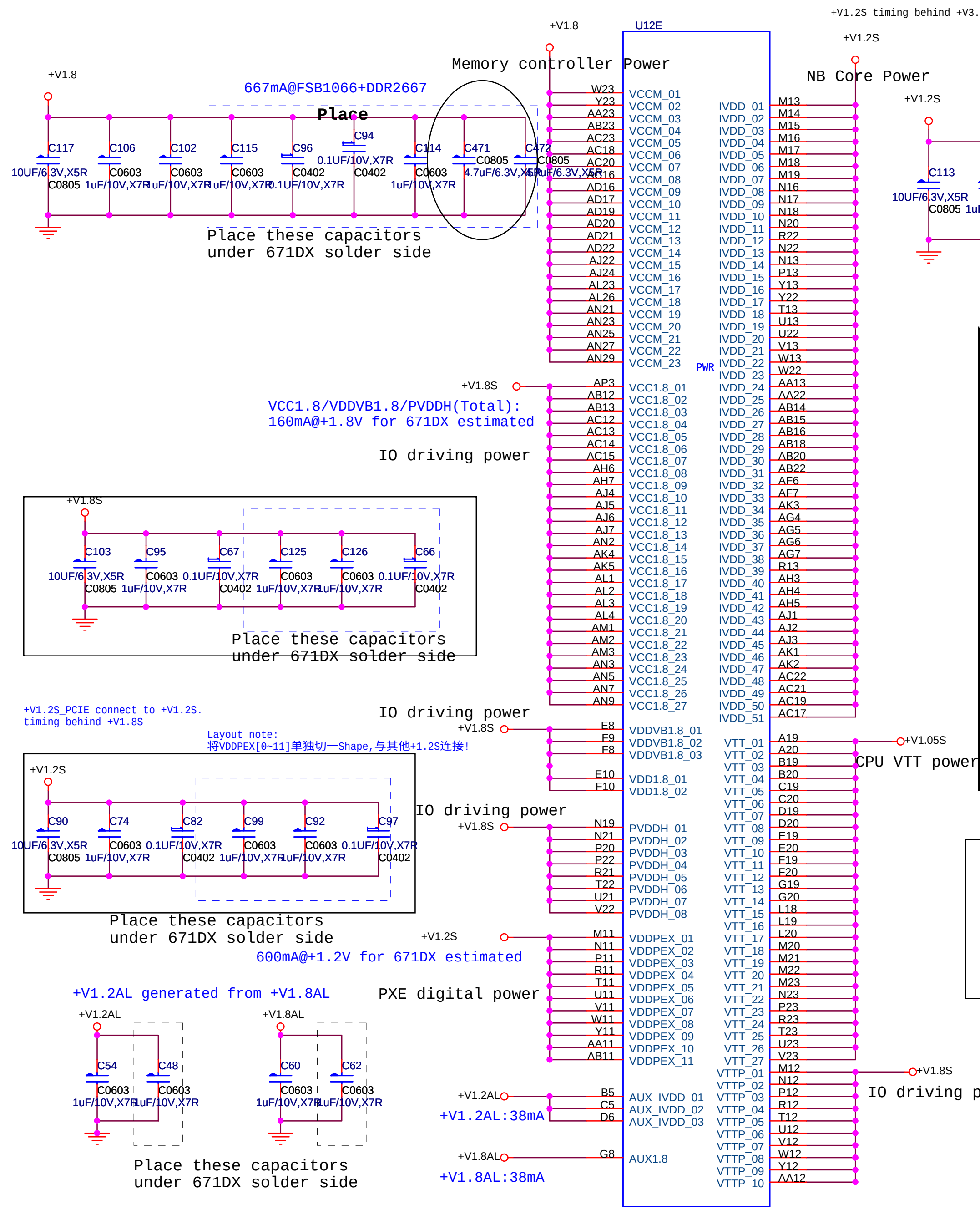
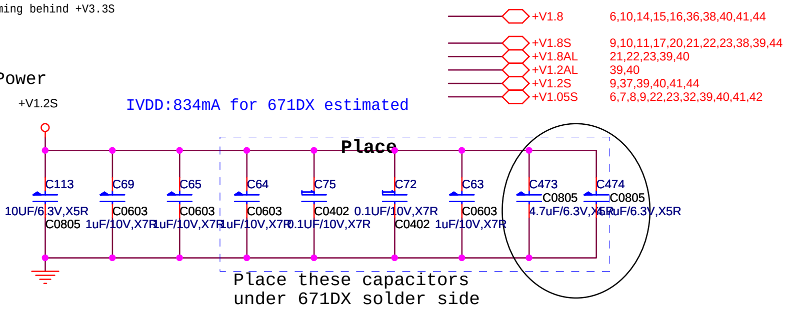
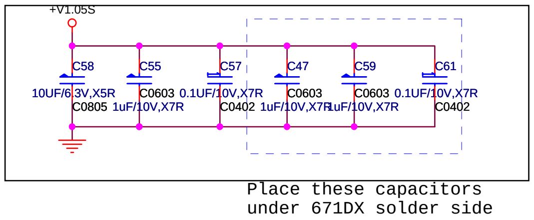


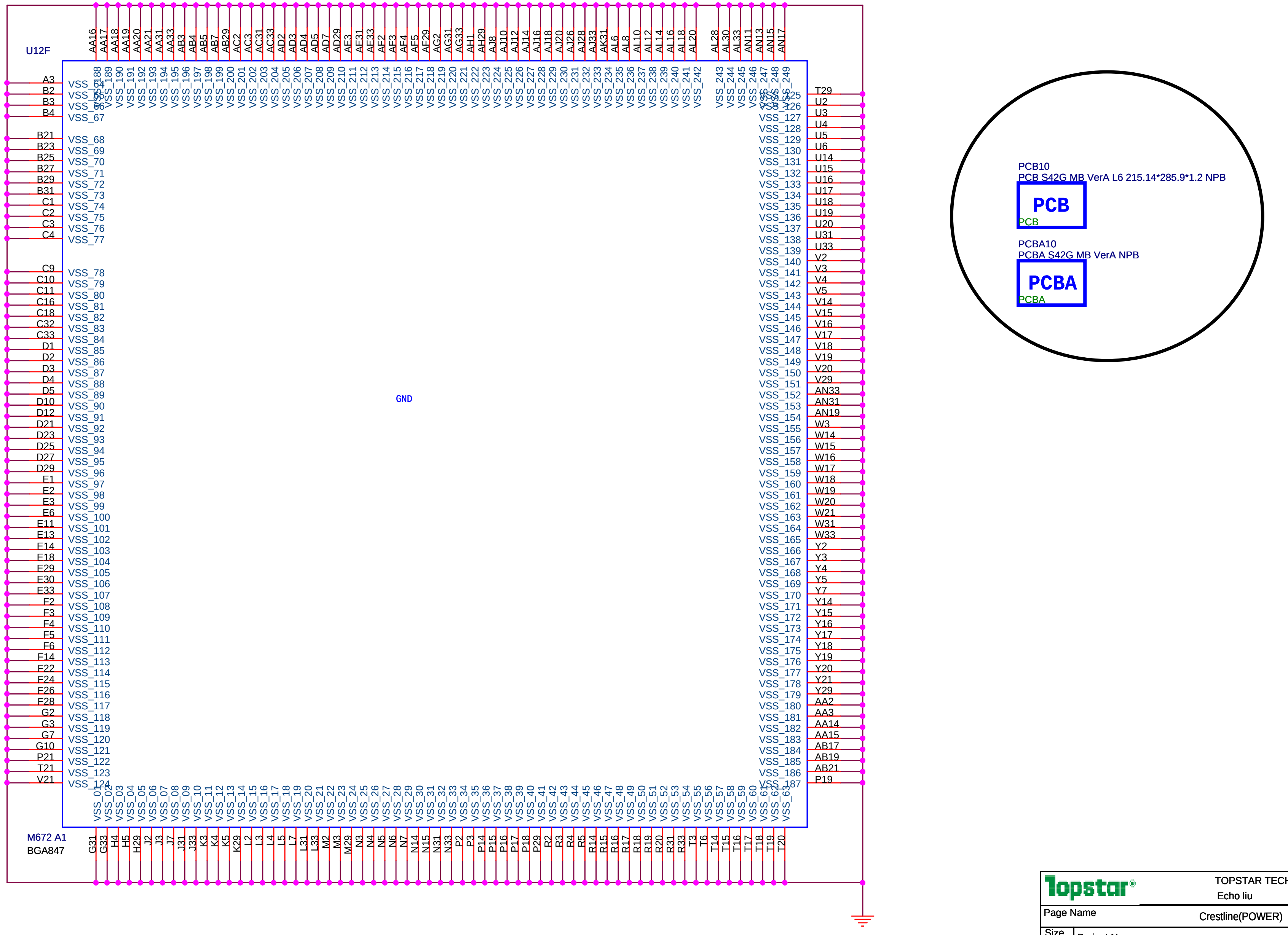




## Subject: SiS671DX Estimated Power Consumption

| Board Power | Chipset Power Plane | Vol | SiS671DX | |
|---|---|---|---|---|
| | | | Current (mA) | Power (mW) |
| V_N_1.8V | C1XAVDD | 1.8 | 25 | 45 |
| V_N_1.8V | C4XAVDD | 1.8 | 25 | 45 |
| V_N_1.8V | D1XAVDD | 1.8 | 20 | 36 |
| V_N_1.8V | DACAVDD1 | 1.8 | 65 | 117 |
| V_N_1.8V | DACAVDD2 | 1.8 | 20 | 36 |
| V_N_1.8V | DCLKAVDD | 1.8 | 20 | 36 |
| V_N_1.8V | ECLKAVDD | 1.8 | 20 | 36 |
| V_S_1.8V | D4XAVDD | 1.8 | 20 | 36 |
| V_S_1.8V | Z4XAVDD | 1.8 | 20 | 36 |
| V_S_1.8V | VCC1.8/VDDVB1.8/VDD1.8/PVDDH | 1.8 | 160 | 288 |
| V_S_1.8V | VTTP | 1.8 | 250 | 450 |
| V_CPU_VTT | VTT | 1.2 | 70 | 84 |
| VMEM_1.8V_DUAL | VCCM | 1.8 | 667 | 1200 |
| V_PCIE_1.2V | VDDPEX | 1.2 | 600 | 720 |
| V_IVDD_1.2V | IVDD | 1.2 | 834 | 1000 |
| V_1.2V_Dual | AUX_IVDD | 1.2 | 47 | 56.4 |
| V_1.8V_Dual | AUX1.8 | 1.8 | 38 | 68.4 |
| SiS671DX FSB1066+DDR2-667+External VGA | | | | 4.29(W) |




| | | |
|---|---|---|
| Topstar | TOPSTAR TECHNOLOGY<br>Echo liu | |
| Page Name | Crestline(VSS&NCTF) | |
| Size A3 | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 12 of 51 | |

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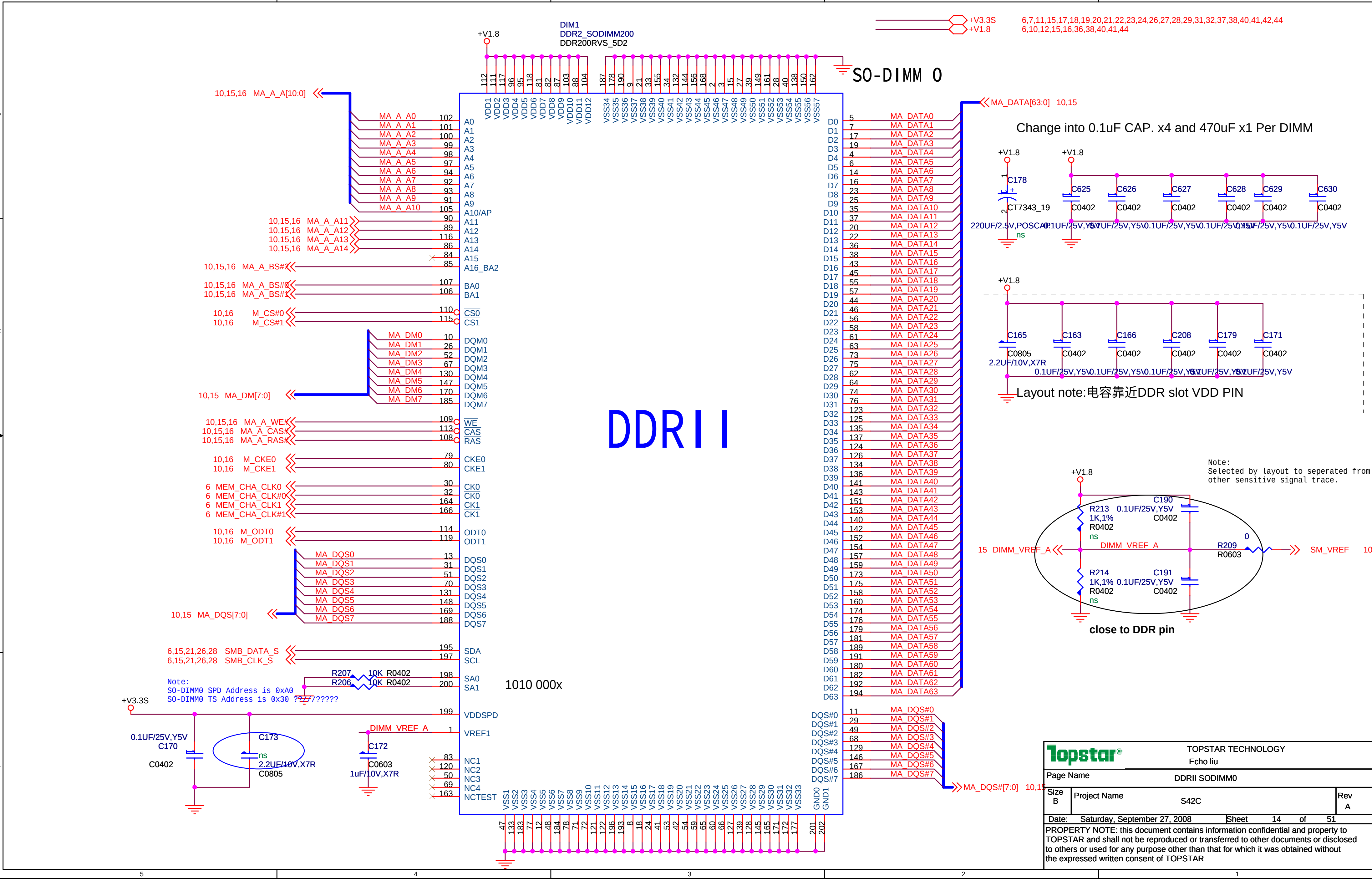
|---|---|---|---|
| Topstar | TOPSTAR TECHNOLOGY<br>Echo liu | | |
| Page Name | Crestline(POWER) | | |
| Size B | Project Name S42C | | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 13 of 51 | | |

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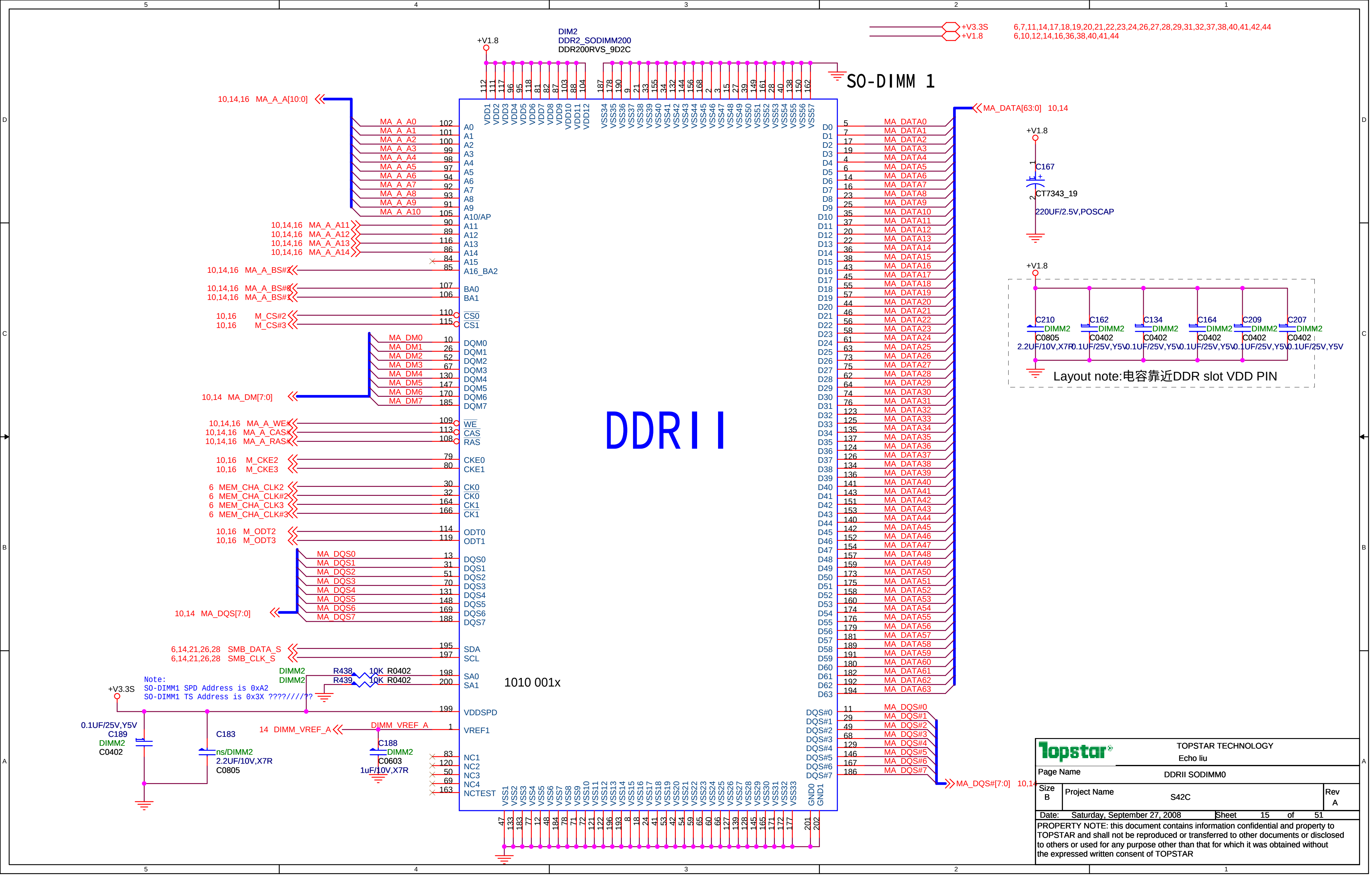
Echo liu

| | | | |
|---|---|---|---|
| Page Name | DDRII SODIMM0 | | |
| Size B | Project Name | S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 14 of 51 | | |

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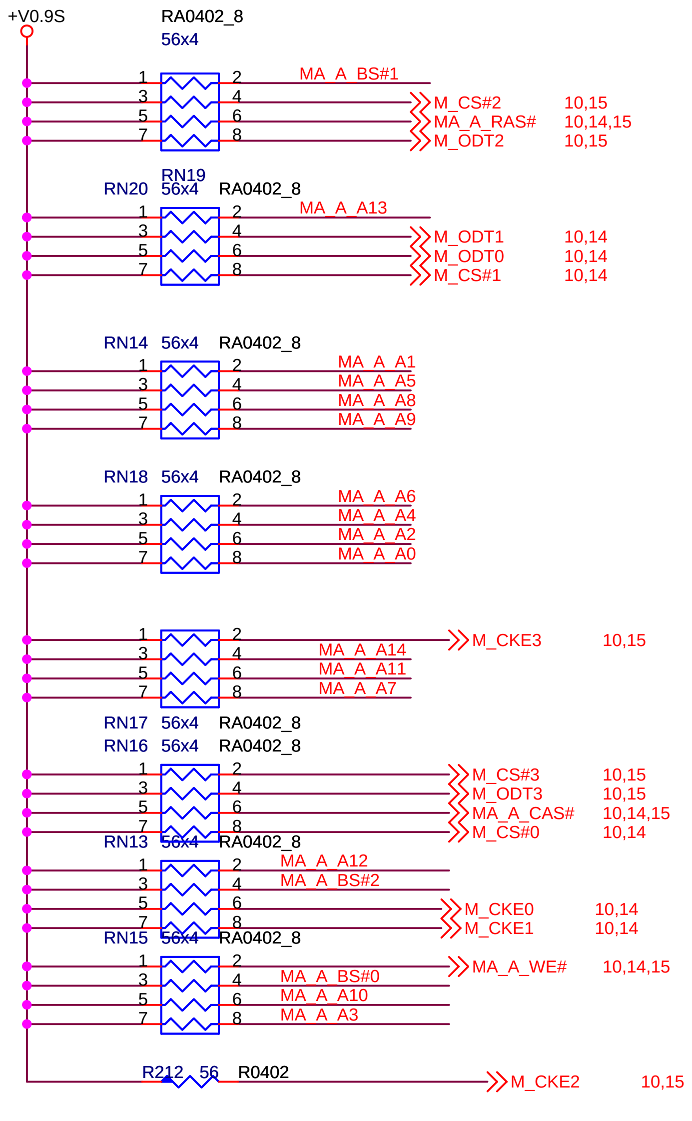
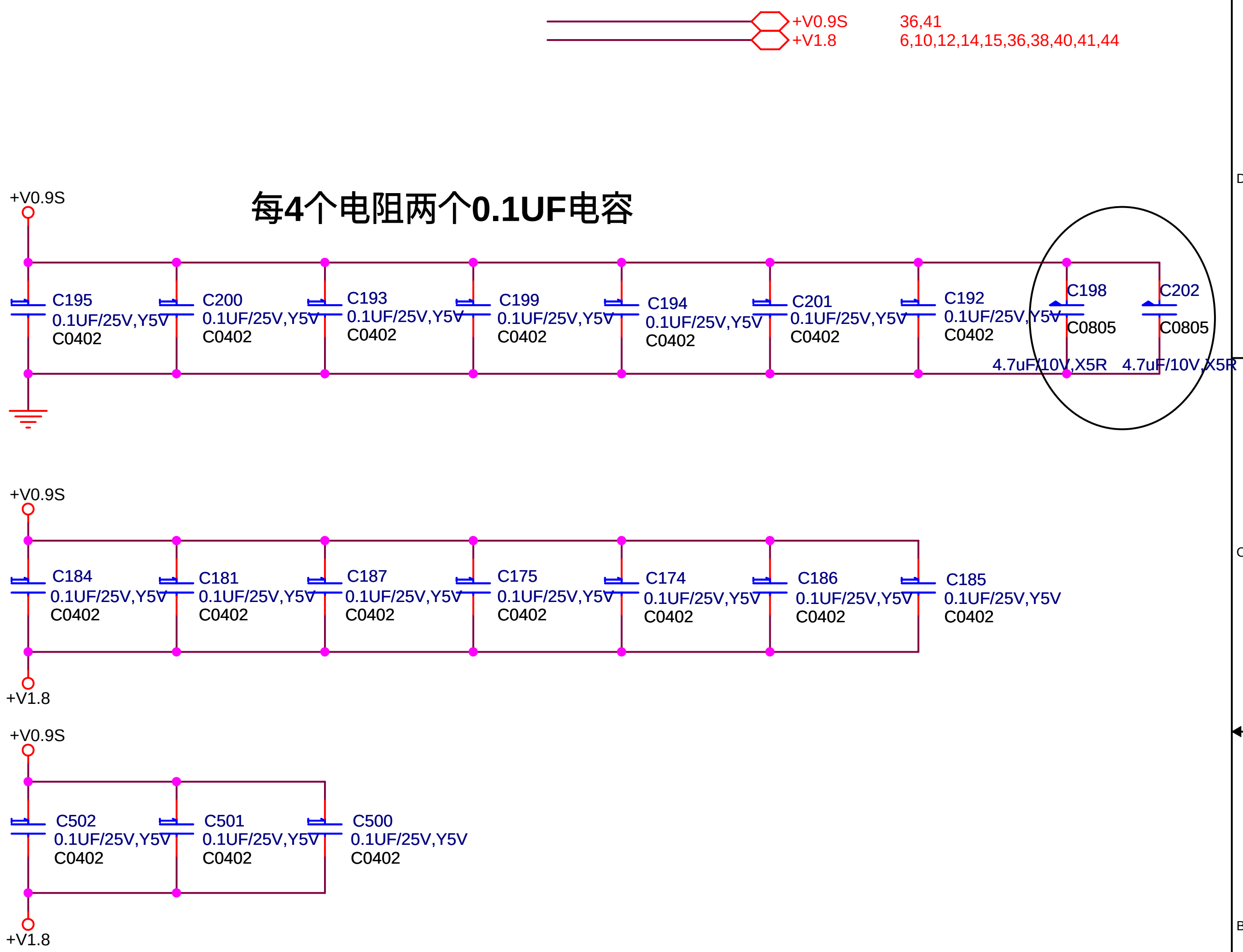
Echo liu

| | | |
|---|---|---|
| Page Name | DDRII SODIMM0 | |
| Size B | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 15 of 51 | |

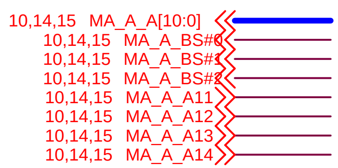


DIMM2




Layout note:
1.Place one cap every 2 terminated resistors;
2.Place +V1.8 to +V0.9 Caps by their power shape;
3.BOM costdown by layout or by test.

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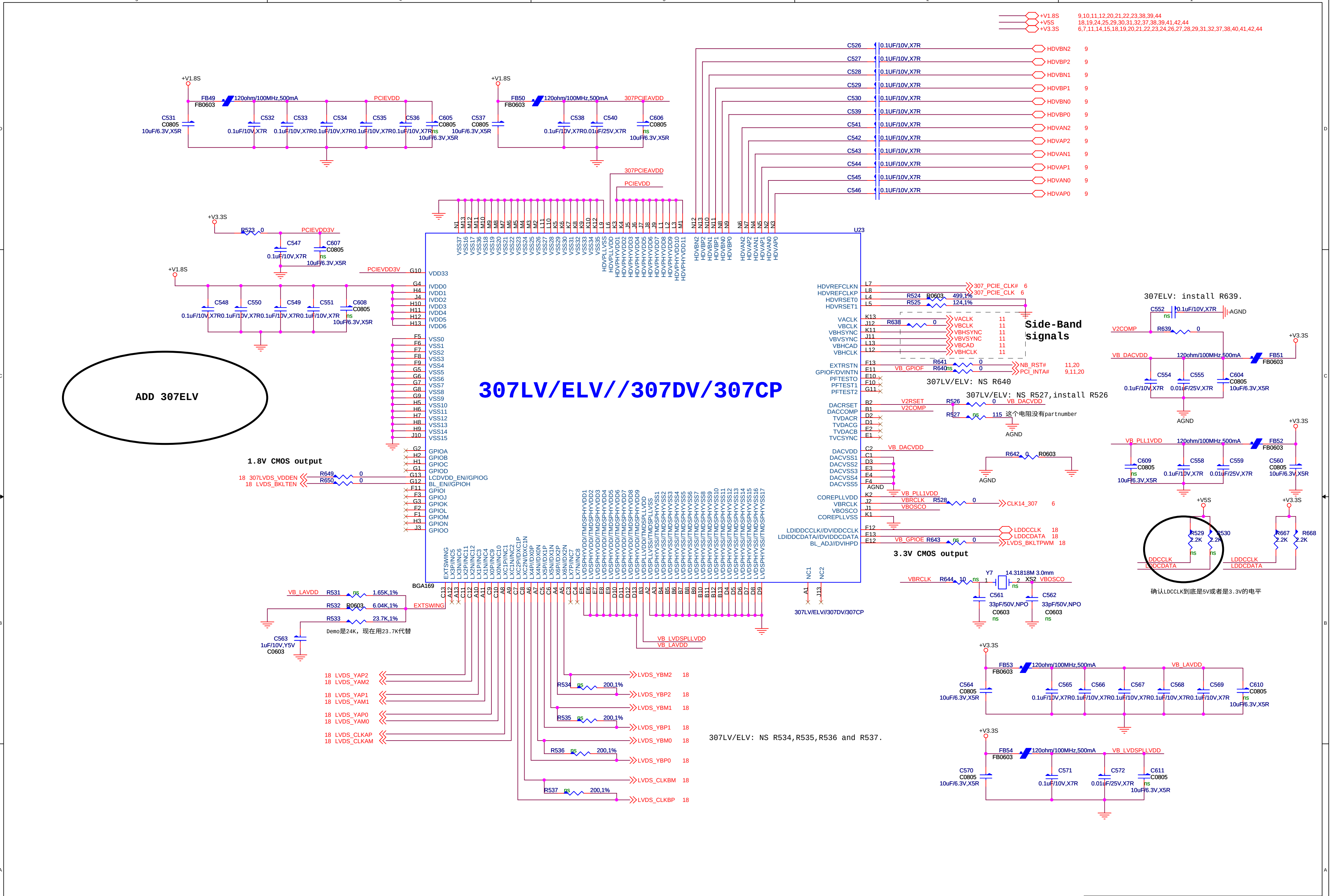
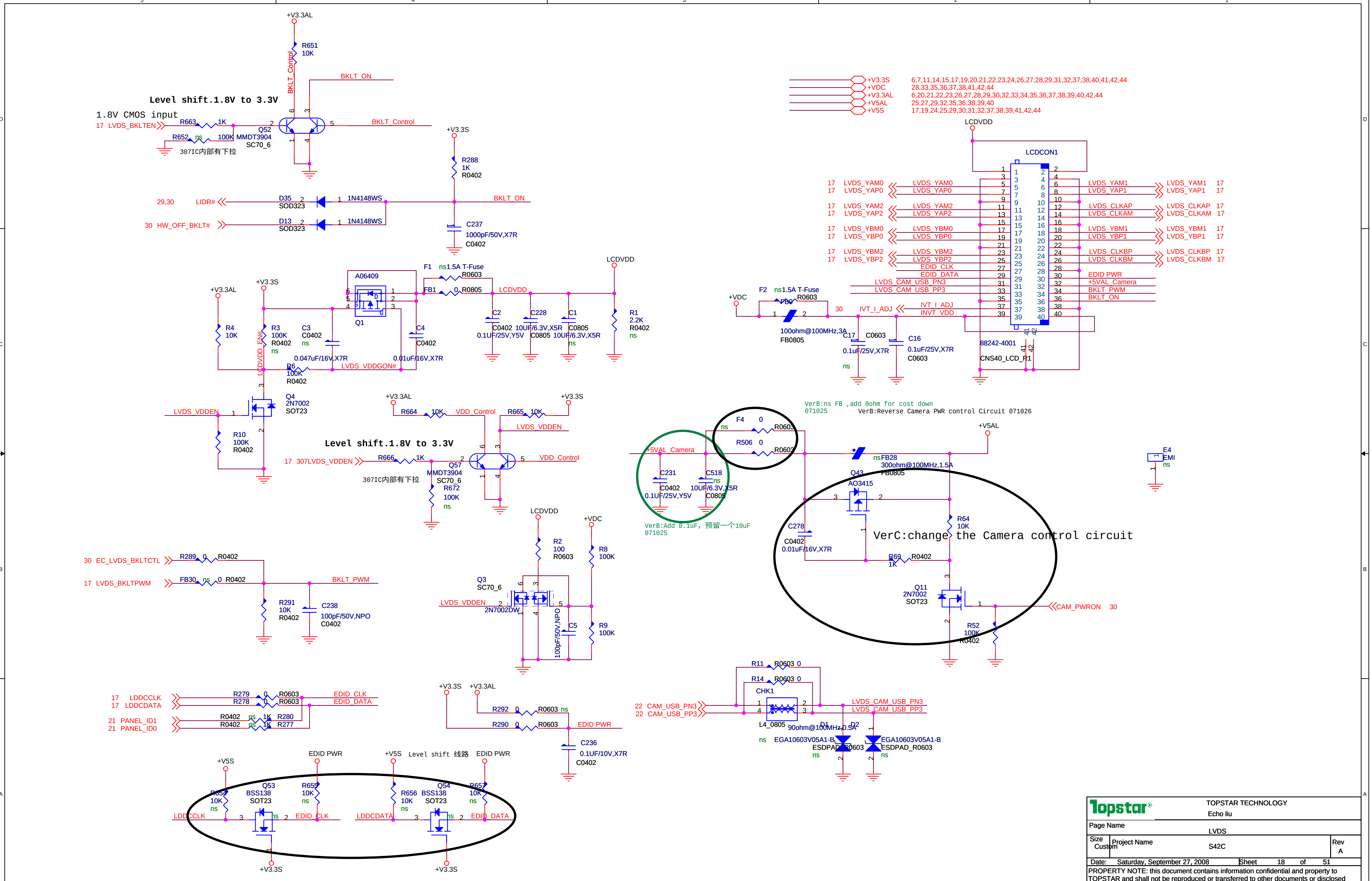
Echo liu

| | | |
|---|---|---|
| Page Name | DDRII Series Termination | |
| Size A4 | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 16 of 51 | |

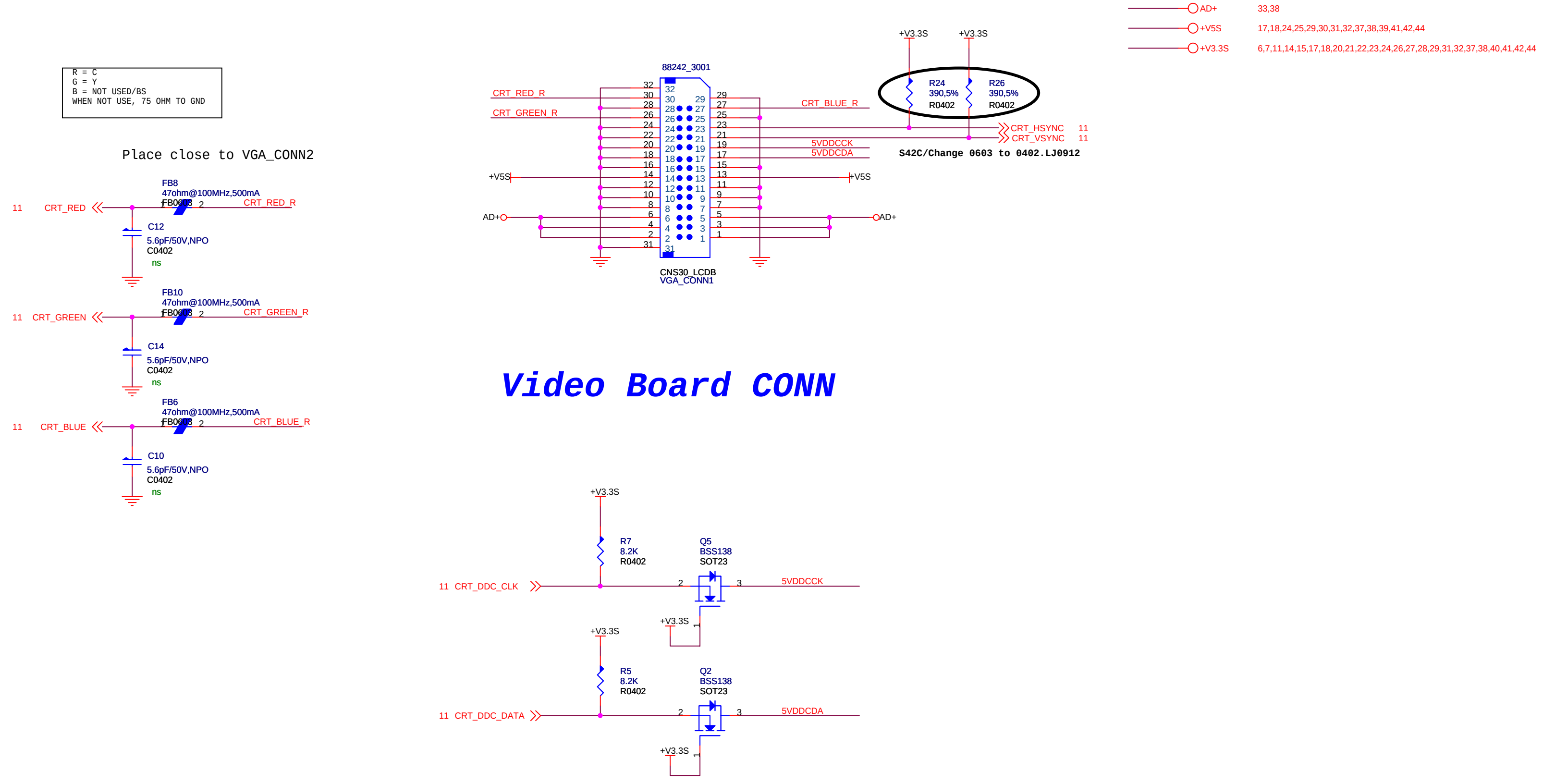



TOPSTAR TECHNOLOGY
Echo liu

| | | |
|---|---|---|
| Page Name | 307LVDS | |
| Size C | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 17 of 51 | |




Topstar
TOPSTAR TECHNOLOGY
Echo liu
Page Name: LVDS
Size: Custom | Project Name: S42C | Rev: A
Date: Saturday, September 27, 2008 | Sheet 18 of 51

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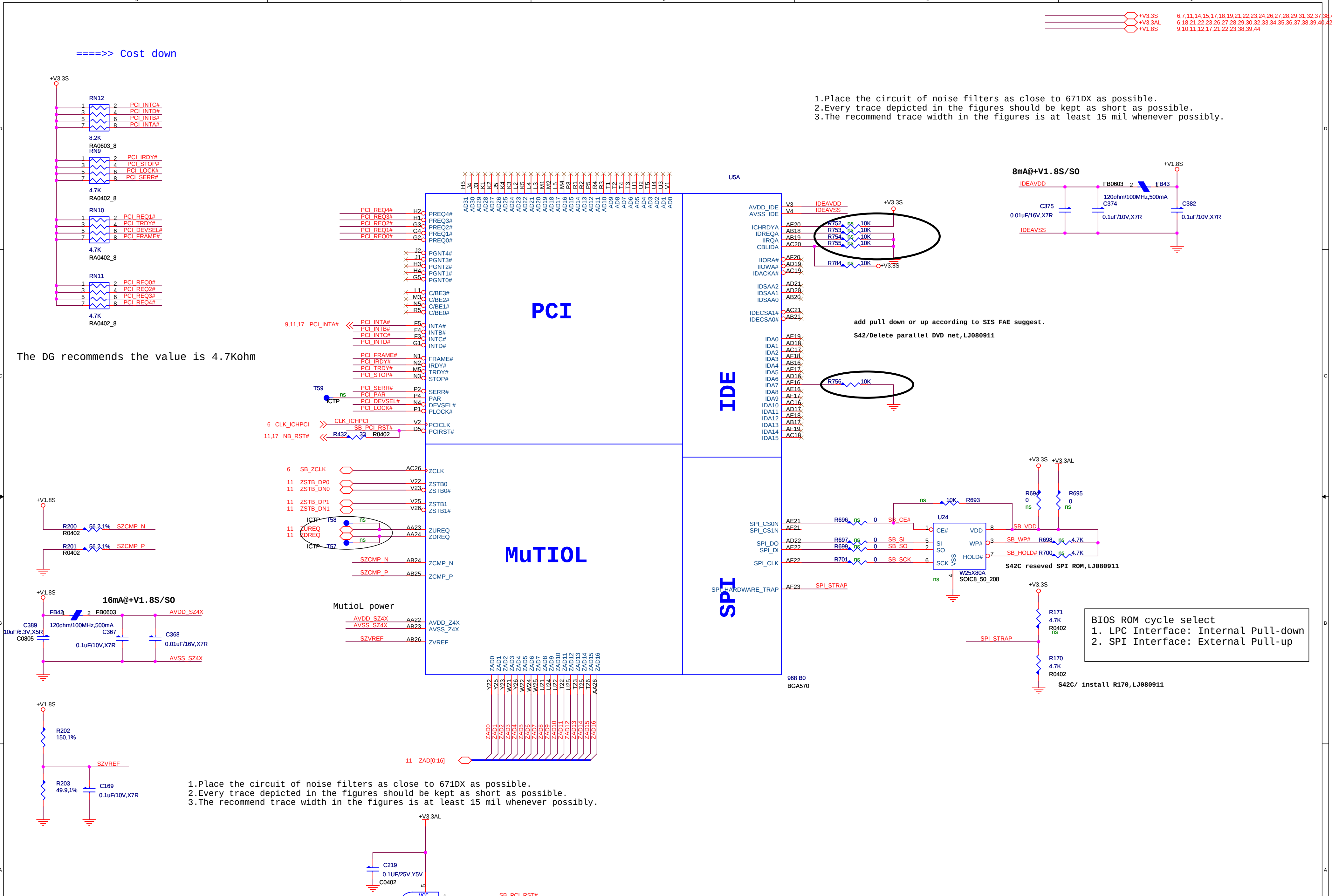
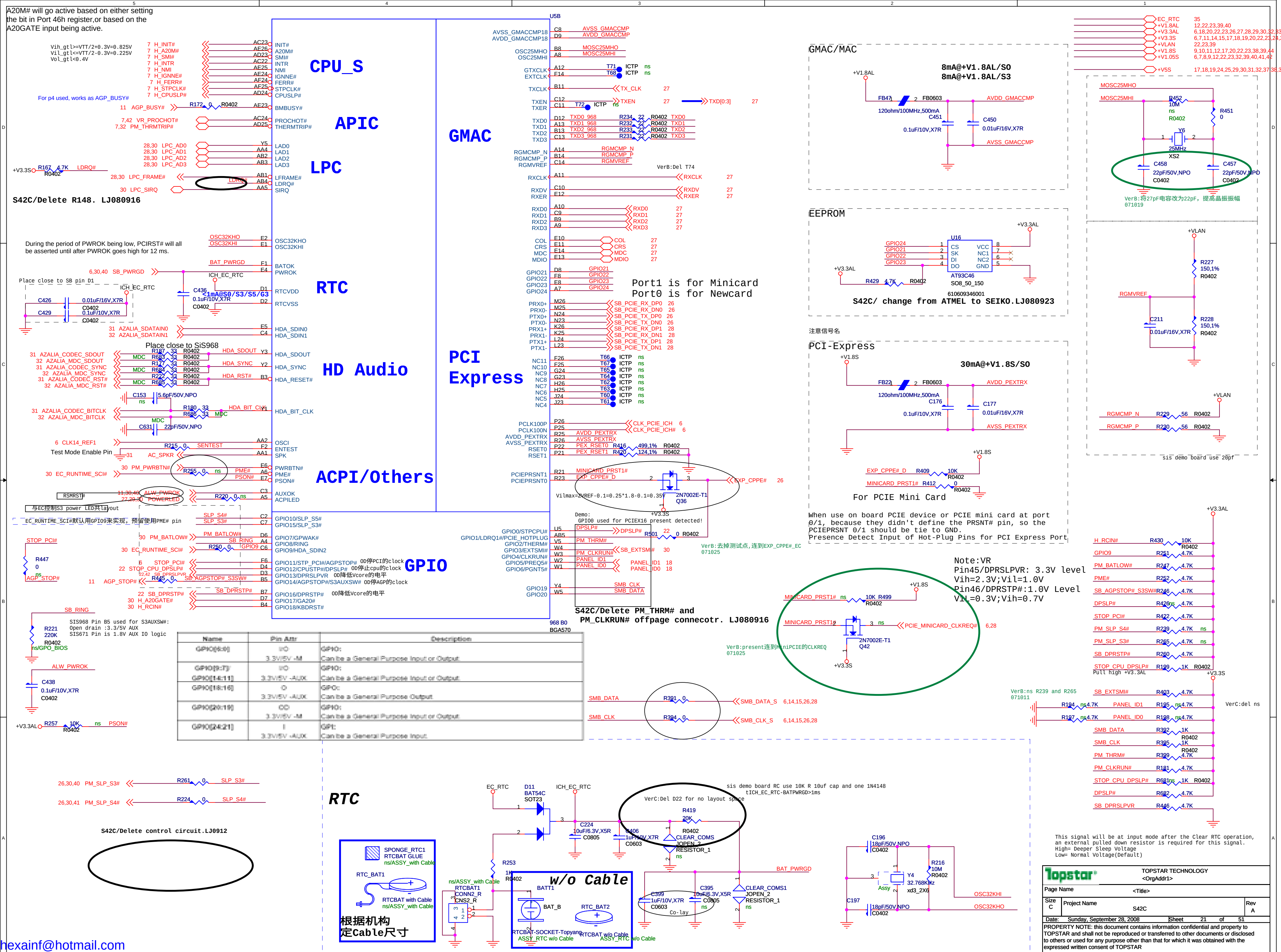
|---|---|
| Topstar | TOPSTAR TECHNOLOGY<br>Echo liu |
| Page Name | CRT CONN & S TV OUT & LIDR SWITCH |
| Size C | Project Name S42C — Rev A |
| Date: Saturday, September 27, 2008 | Sheet 19 of 51 |



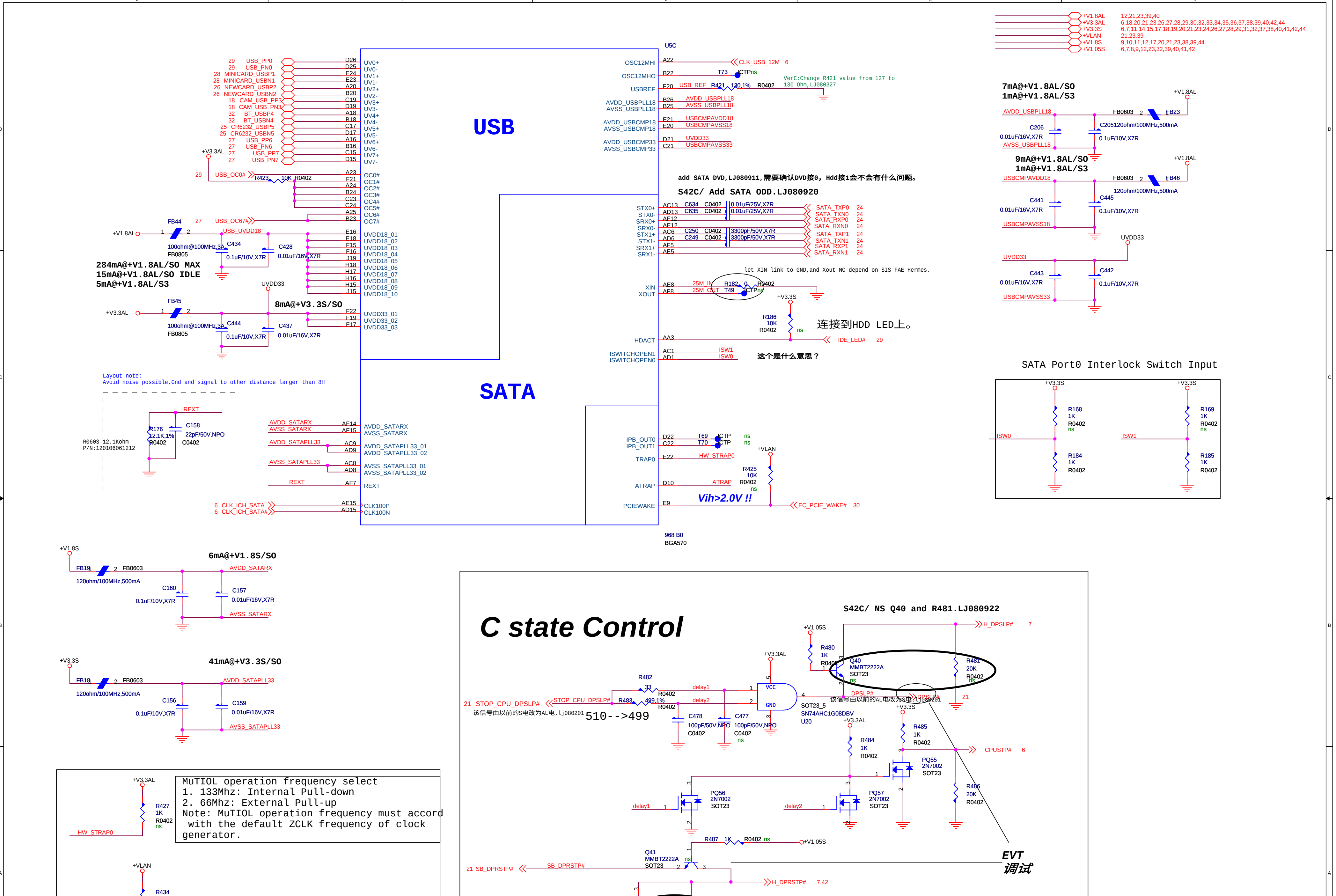

TOPSTAR TECHNOLOGY
<OrgAddr1>

| | | |
|---|---|---|
| Page Name | <Title> | |
| Size C | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 20 of 51 | |




| Name | Pin Attr | Description |
|---|---|---|
| GPIO[6:0] | I/O 3.3V/5V -M | GPIO: Can be a General Purpose Input or Output |
| GPIO[9:7] GPIO[14:11] | I/O 3.3V/5V -AUX | GPIO: Can be a General Purpose Input or Output |
| GPIO[18:16] | O 3.3V/5V -AUX | GPO: Can be a General Purpose Output |
| GPIO[20:19] | OD 3.3V/5V -M | GPIO: Can be a General Purpose Input or Output |
| GPIO[24:21] | I 3.3V/5V -AUX | GPI: Can be a General Purpose Input |

TOPSTAR TECHNOLOGY
Project Name: S42C
Size: C | Rev: A
Date: Sunday, September 28, 2008 | Sheet 21 of 51

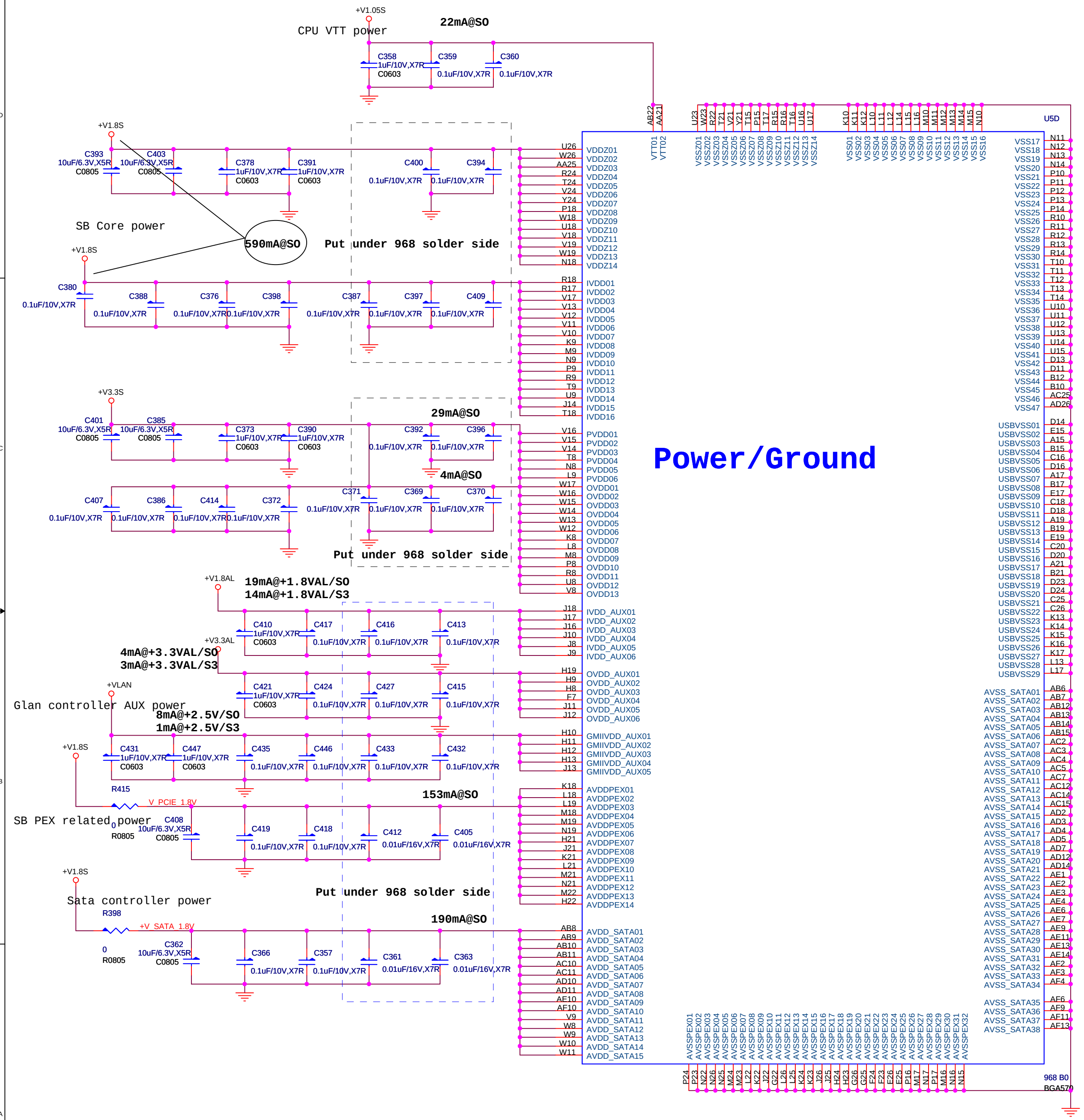



Topstar TOPSTAR TECHNOLOGY <OrgAddr1>

Page Name: <Title>

| Size | Project Name | Rev |
|---|---|---|
| C | S42C | A |

Date: Saturday, September 27, 2008 Sheet 22 of 51




| | | |
|---|---|---|
| +V1.8S | | 9,10,11,12,17,20,21,22,38,39,44 |
| +V1.8AL | | 12,21,22,39,40 |
| +V3.3AL | | 6,18,20,21,22,26,27,28,29,30,32,33,34,35,36,37,38,39,40,42,44 |
| +V1.05S | | 6,7,8,9,12,22,32,39,40,41,42 |
| +VLAN | | 21,22,39 |
| +V3.3S | | 6,7,11,14,15,17,18,19,20,21,22,24,26,27,28,29,31,32,37,38,40,41,42,44 |

## Subject: SiS968 B0 Stepping Measured Power Consumption

| Chipset Power plane | Vol | SiS968 | | | SiS968 | | |
|---|---|---|---|---|---|---|---|
| | | Max. | Idle | S3 | Max. | Idle | S3 |
| | | Current (mA) | | | Power (mW) | | |
| PVDD | 3.3 | 29 | 29 | - | 96 | 96 | - |
| OVDD | 3.3 | 4 | 4 | - | 13 | 15 | - |
| AVDD_SATAPLL33 | 3.3 | 41 | 41 | - | 135 | 135 | - |
| AVDD_SATA | 1.8 | 190 | 162 | - | 342 | 291 | - |
| AVDD_SATARX | 1.8 | 6 | 6 | - | 11 | 11 | - |
| AVDDPEX | 1.8 | 153 | 124 | - | 275 | 224 | - |
| AVDD_PEXTRX | 1.8 | 30 | 30 | - | 54 | 55 | - |
| IVDD/VDDZ | 1.8 | 522 | 485 | - | 940 | 873 | - |
| AVDD_IDE | 1.8 | 8 | 8 | - | 14 | 14 | - |
| AVDDZ4X | 1.8 | 16 | 16 | - | 29 | 29 | - |
| VTT | 1.2/1.05 | 22 | 22 | - | 26/23 | 26/23 | - |
| GMIIVDD_AUX | 2.5 | 8 | 7 | 1 | 20 | 18 | 2 |
| OVDD_AUX | 3.3 | 4 | 4 | 3 | 13 | 14 | 10 |
| UVDD33/AVDD_USBCMP33 | 3.3 | 8 | 8 | - | 26 | 27 | - |
| RTCVDD | 3.3 | <1 | <1 | <1 | <1 | <1 | <1 |
| IVDD_AUX | 1.8 | 19 | 13 | 14 | 34 | 24 | 25 |
| AVDD_GMACCMP18 | 1.8 | 8 | 8 | 8 | 14 | 14 | 14 |
| UVDD18 | 1.8 | 284 | 15 | 5 | 511 | 27 | 9 |
| AVDD_USBPLL18 | 1.8 | 7 | 7 | <1 | 13 | 13 | 1 |
| AVDD_USBCMP18 | 1.8 | 9 | 9 | <1 | 16 | 16 | <1 |
| **SiS968 B0 Stepping Total Power Consumption on DT** | | | | | **2584** | **1921** | **61** |
| **SiS968 B0 Stepping Total Power Consumption on NB** | | | | | **2581** | **1918** | **61** |



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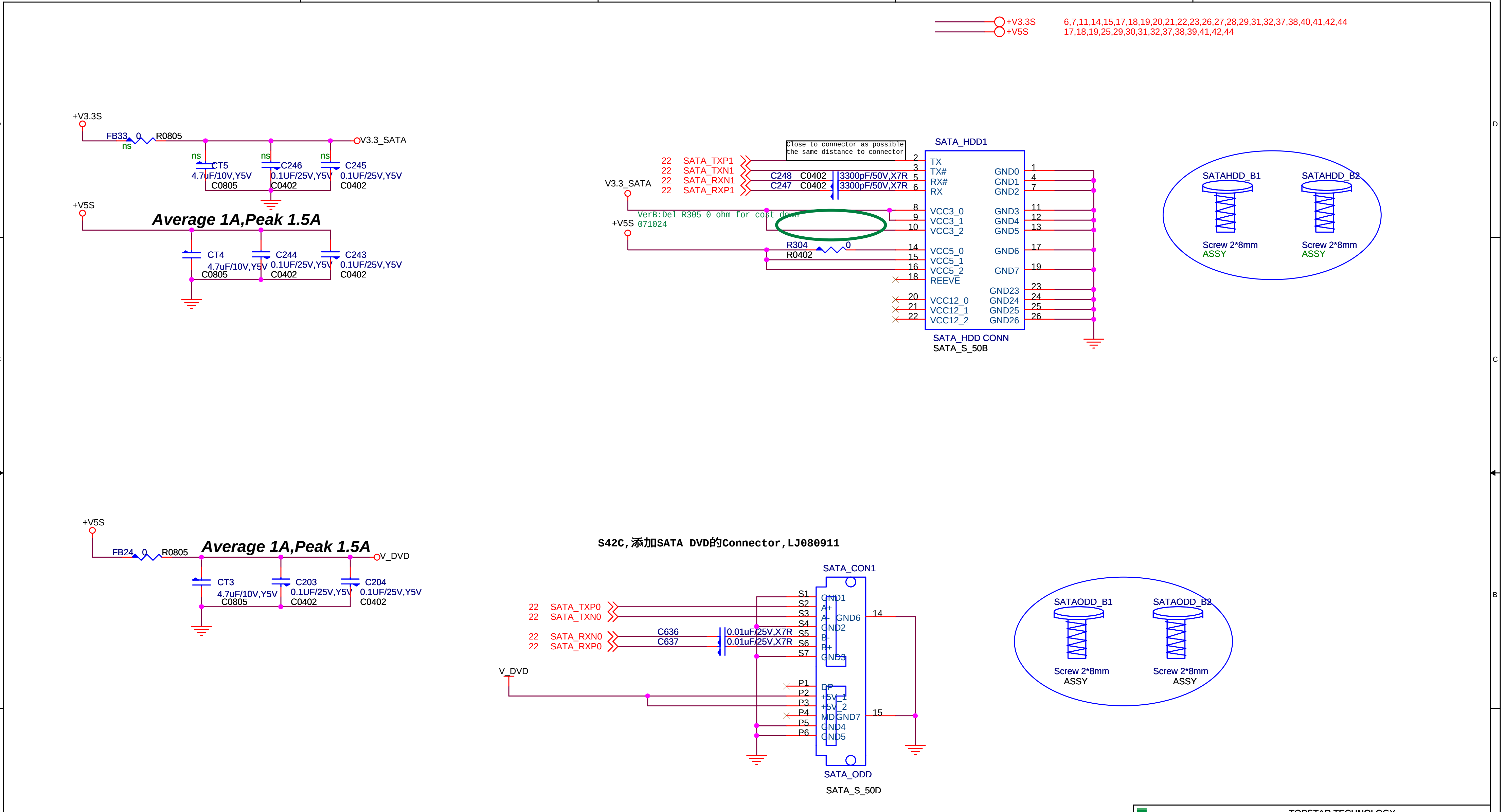
<OrgAddr1>

Page Name: <Title>

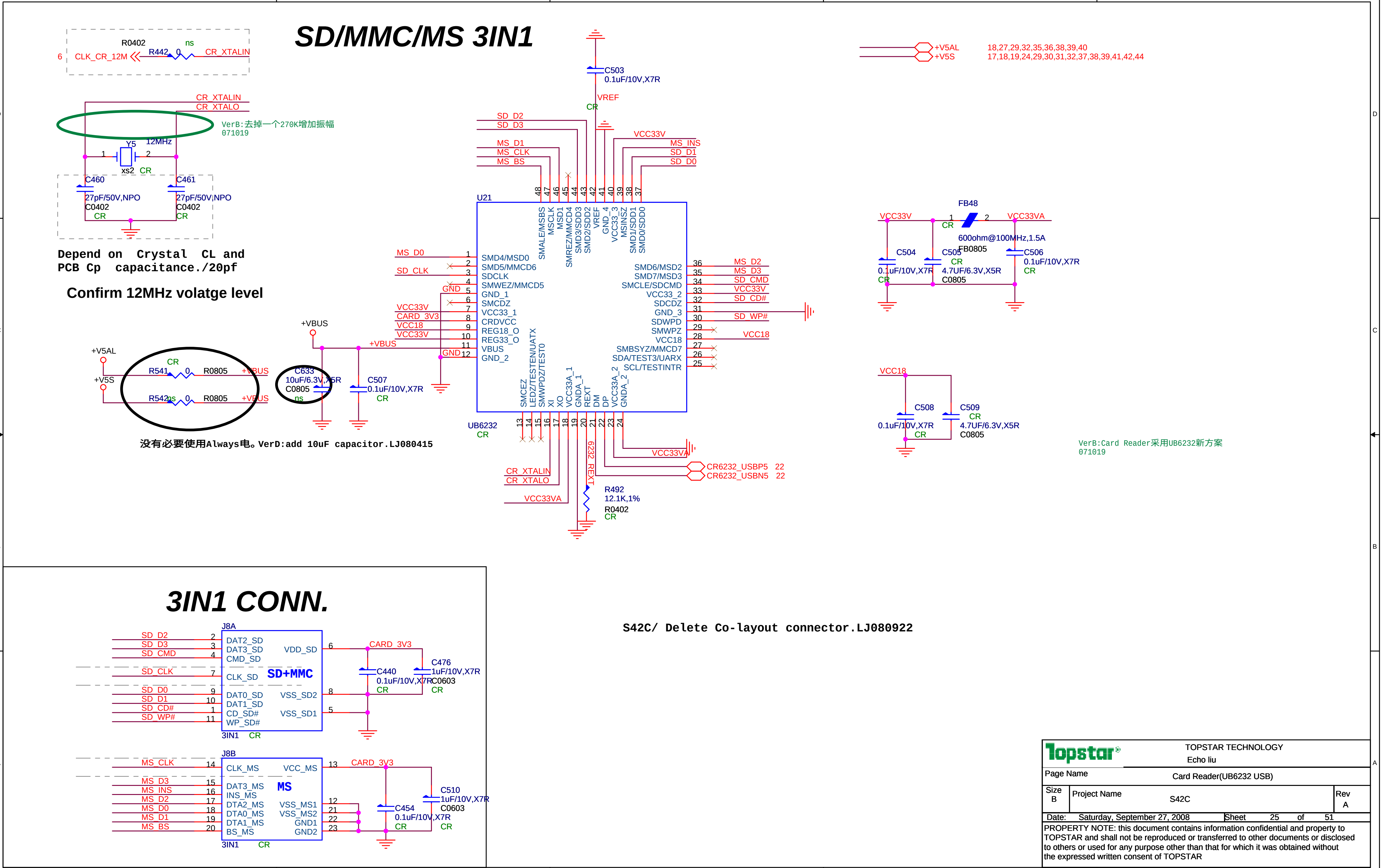
Size: C | Project Name: S42C | Rev: A

Date: Saturday, September 27, 2008 | Sheet 23 of 51

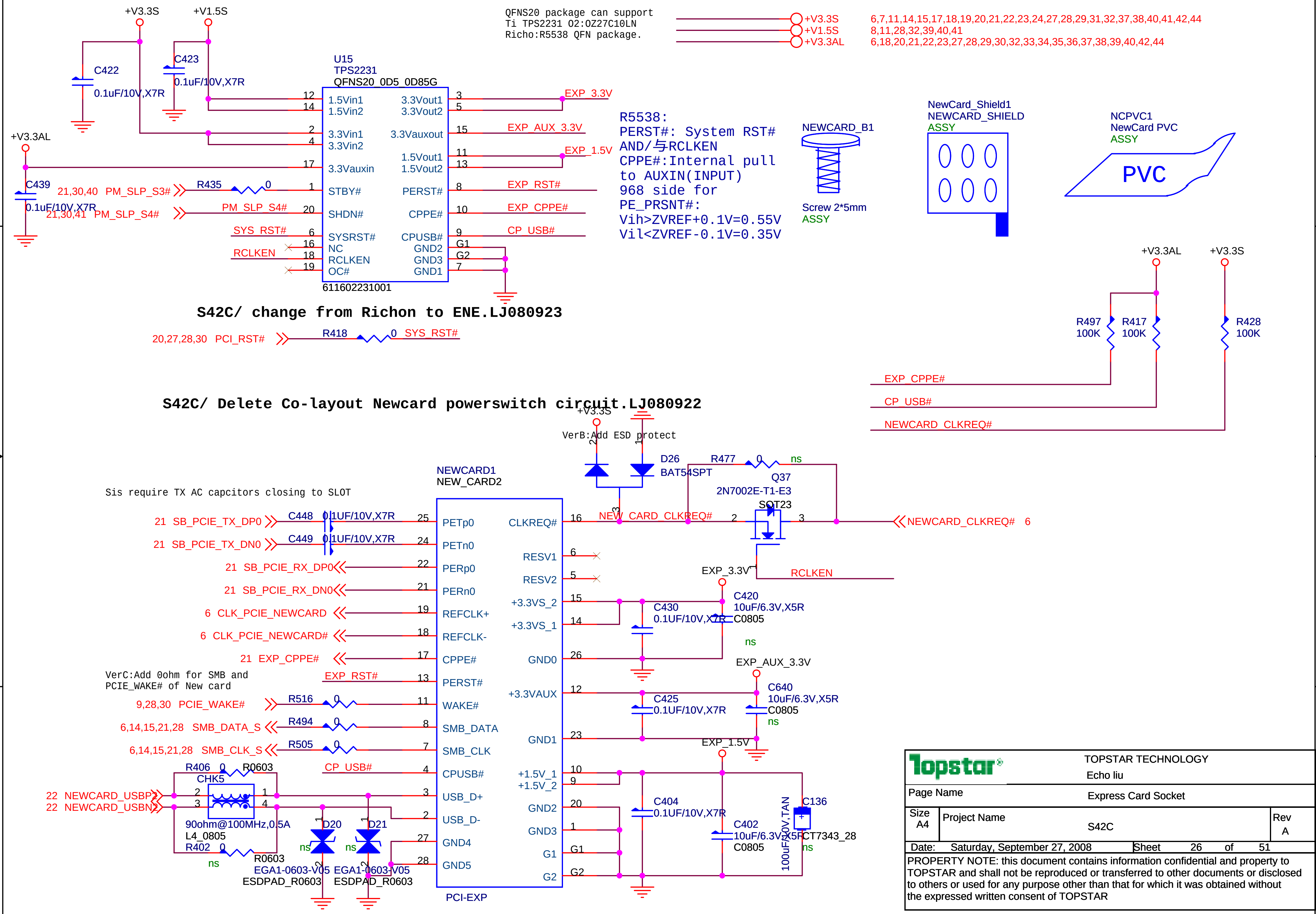



| | |
|---|---|
| Topstar | TOPSTAR TECHNOLOGY<br>Echo liu |
| Page Name | IDE/SATA CONN(SATA&DVD) |
| Size B | Project Name S42C — Rev A |
| Date: Saturday, September 27, 2008 | Sheet 24 of 51 |

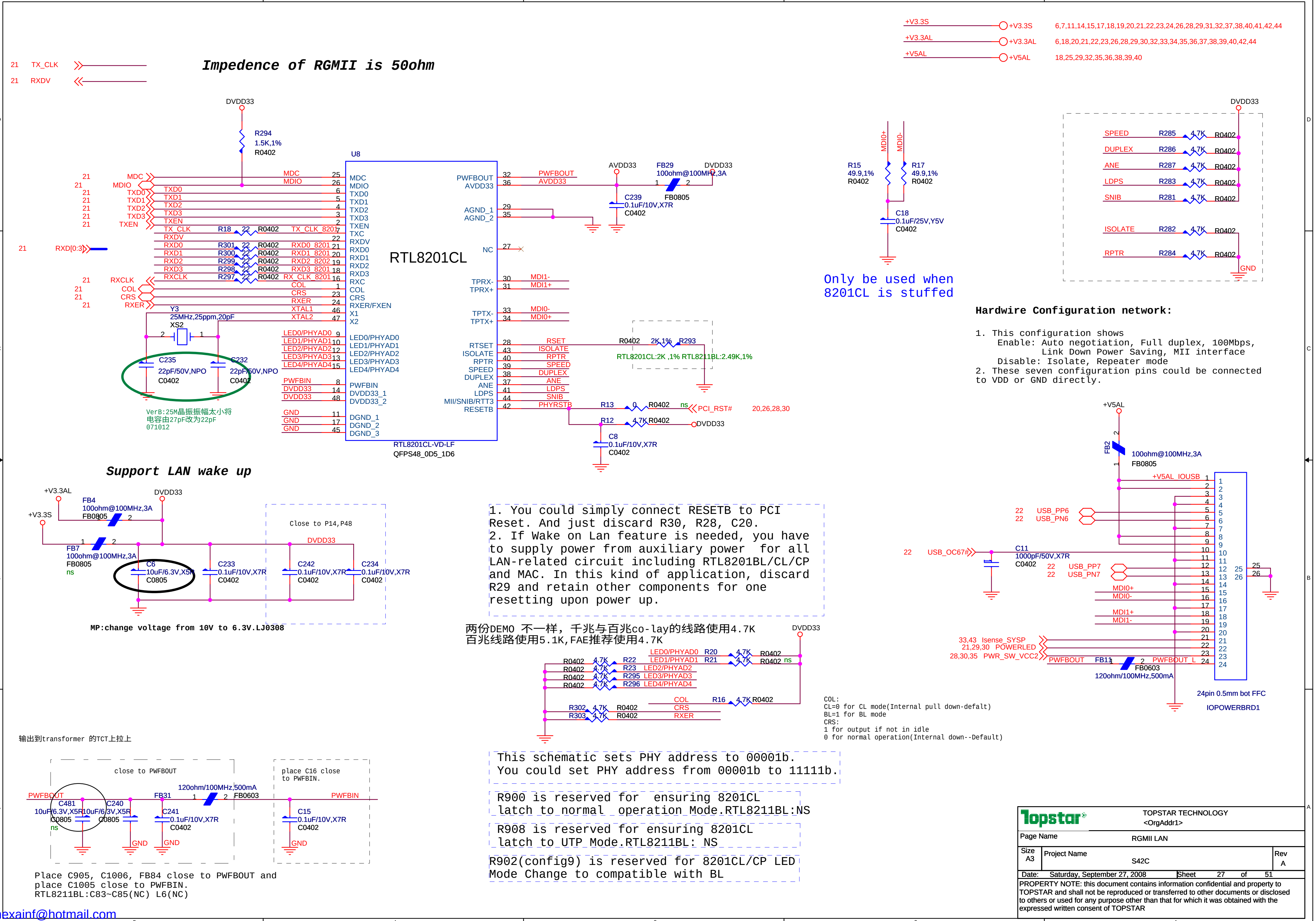
# SD/MMC/MS 3IN1




| | |
|---|---|
| TOPSTAR TECHNOLOGY | Echo liu |
| Page Name | Card Reader(UB6232 USB) |
| Size B | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 25 of 51 |




| | |
|---|---|
| Topstar | TOPSTAR TECHNOLOGY<br>Echo liu |
| Page Name | Express Card Socket |
| Size A4 | Project Name S42C — Rev A |
| Date: Saturday, September 27, 2008 | Sheet 26 of 51 |




**Hardwire Configuration network:**

1. This configuration shows
   Enable: Auto negotiation, Full duplex, 100Mbps, Link Down Power Saving, MII interface
   Disable: Isolate, Repeater mode
2. These seven configuration pins could be connected to VDD or GND directly.

1. You could simply connect RESETB to PCI Reset. And just discard R30, R28, C20.
2. If Wake on Lan feature is needed, you have to supply power from auxiliary power for all LAN-related circuit including RTL8201BL/CL/CP and MAC. In this kind of application, discard R29 and retain other components for one resetting upon power up.

两份DEMO 不一样，千兆与百兆co-lay的线路使用4.7K
百兆线路使用5.1K,FAE推荐使用4.7K

COL:
CL=0 for CL mode(Internal pull down-defalt)
BL=1 for BL mode
CRS:
1 for output if not in idle
0 for normal operation(Internal down--Default)

This schematic sets PHY address to 00001b.
You could set PHY address from 00001b to 11111b.

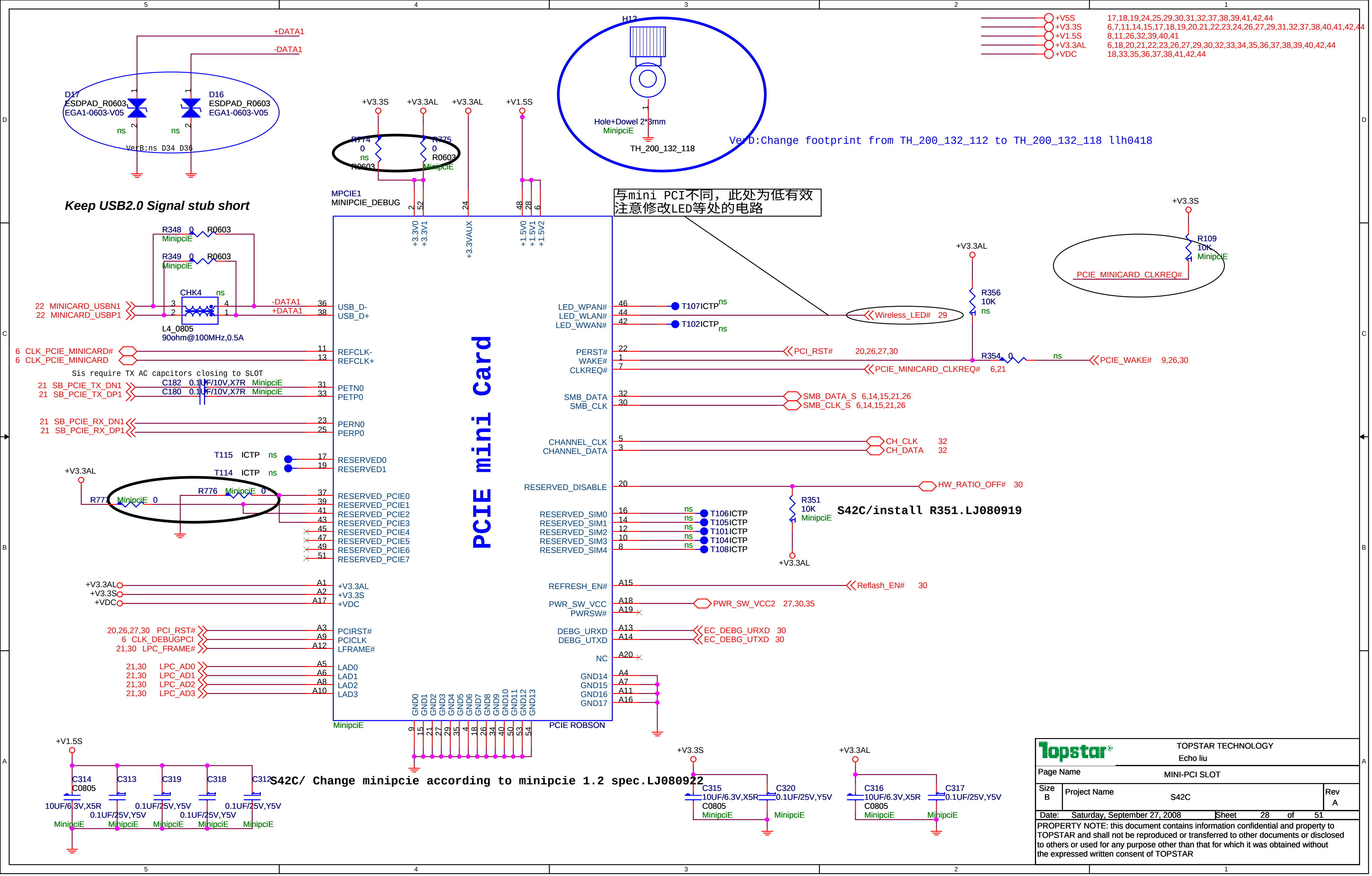
R900 is reserved for ensuring 8201CL latch to normal operation Mode.RTL8211BL:NS

R908 is reserved for ensuring 8201CL latch to UTP Mode.RTL8211BL: NS

R902(config9) is reserved for 8201CL/CP LED Mode Change to compatible with BL

Place C905, C1006, FB84 close to PWFBOUT and place C1005 close to PWFBIN.
RTL8211BL:C83~C85(NC) L6(NC)

| | |
|---|---|
| Topstar | TOPSTAR TECHNOLOGY <OrgAddr1> |
| Page Name | RGMII LAN |
| Size A3 | Project Name S42C, Rev A |
| Date: Saturday, September 27, 2008 | Sheet 27 of 51 |

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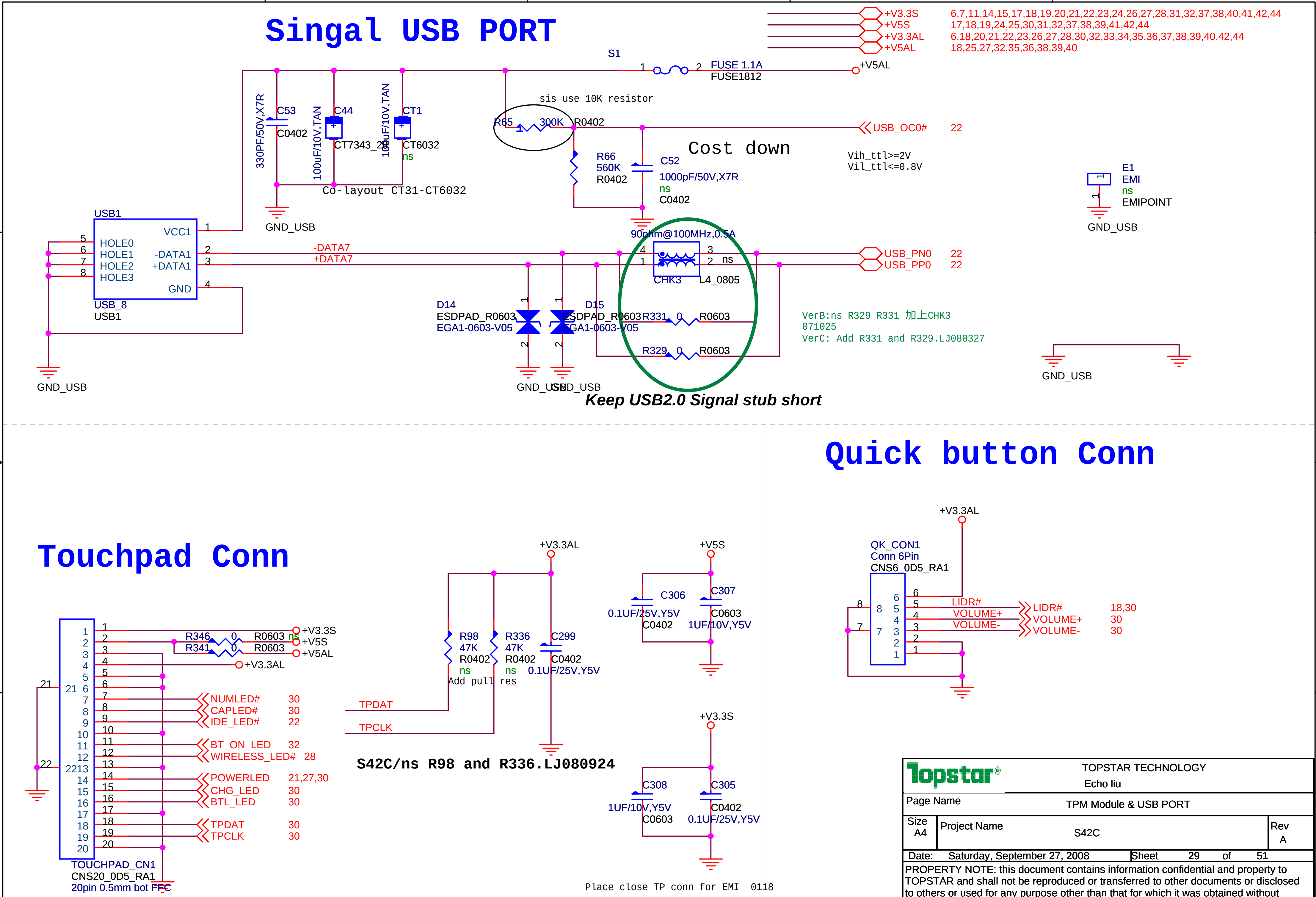
Page Name: MINI-PCI SLOT

Size: B | Project Name: S42C | Rev: A

Date: Saturday, September 27, 2008 | Sheet 28 of 51

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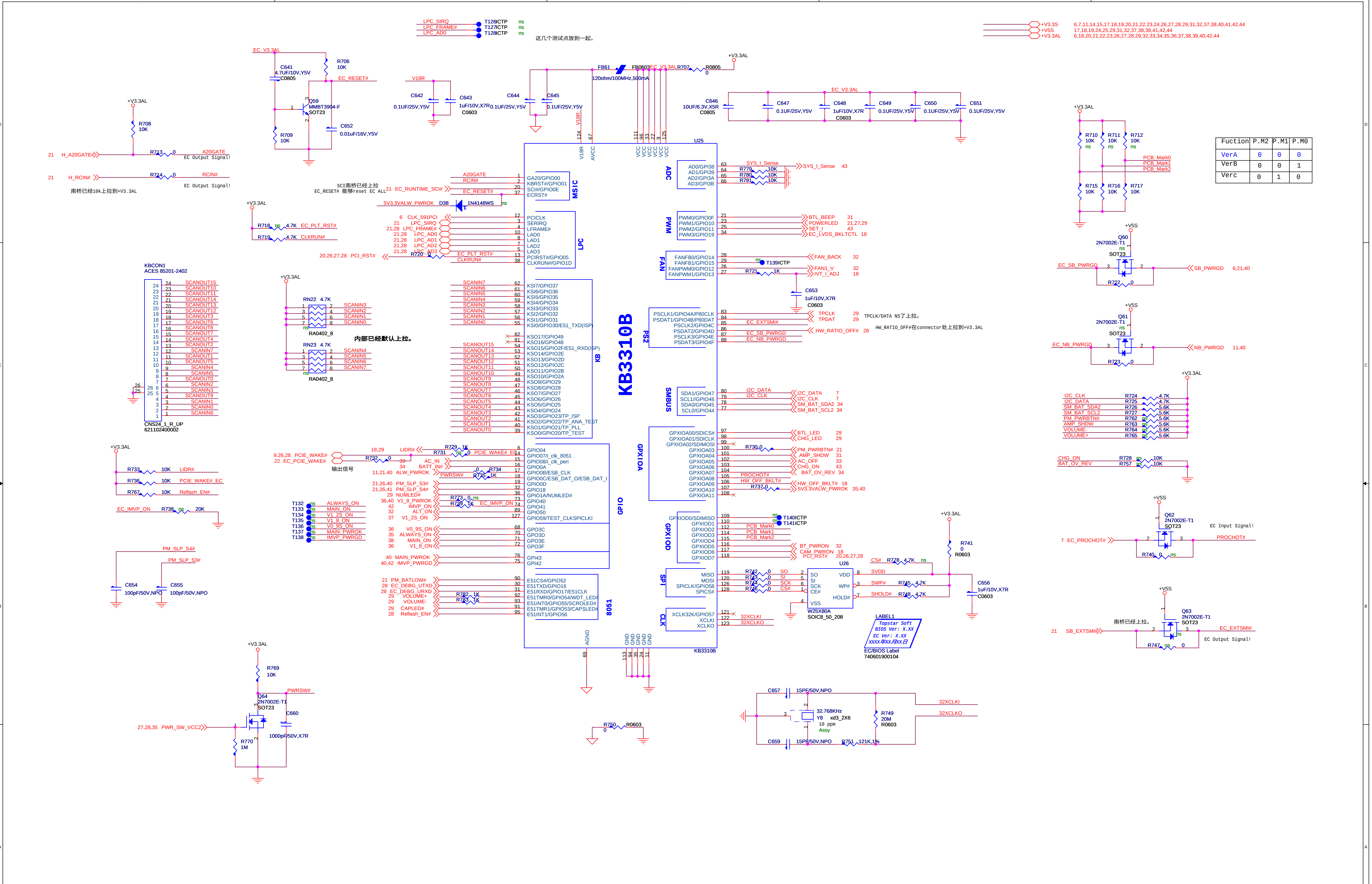
|---|---|
| Topstar | TOPSTAR TECHNOLOGY<br>Echo liu |
| Page Name | TPM Module & USB PORT |
| Size A4 | Project Name S42C — Rev A |
| Date: Saturday, September 27, 2008 | Sheet 29 of 51 |




| Fuction | P.M2 | P.M1 | P.M0 |
|---|---|---|---|
| VerA | 0 | 0 | 0 |
| VerB | 0 | 0 | 1 |
| Verc | 0 | 1 | 0 |

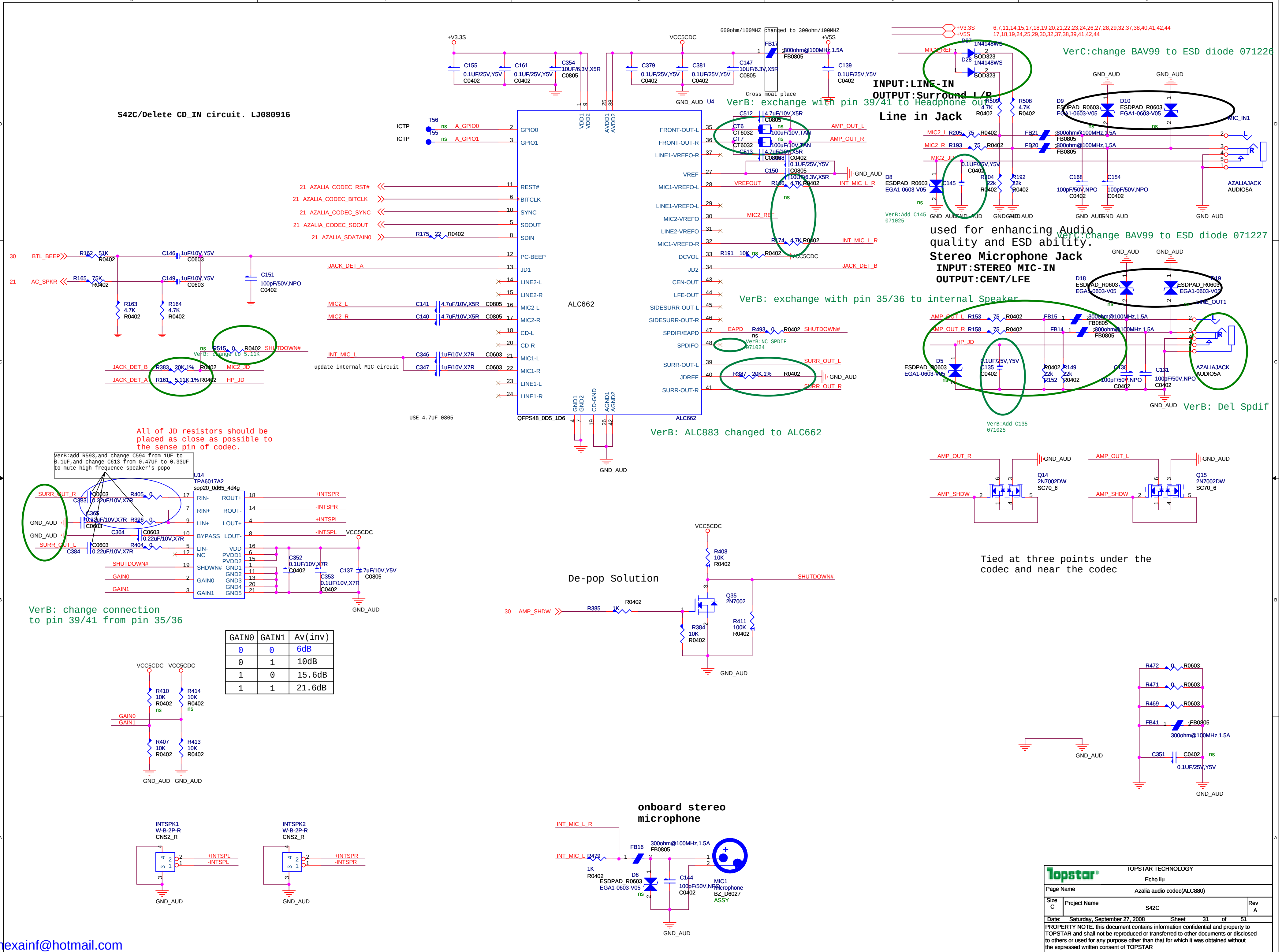
TOPSTAR TECHNOLOGY

Echo liu

Page Name: KBC(KB3310B)

Size: Custom | Project Name: S42C | Rev: A

Date: Saturday, September 27, 2008 | Sheet 30 of 51




| GAIN0 | GAIN1 | Av(inv) |
|---|---|---|
| 0 | 0 | 6dB |
| 0 | 1 | 10dB |
| 1 | 0 | 15.6dB |
| 1 | 1 | 21.6dB |

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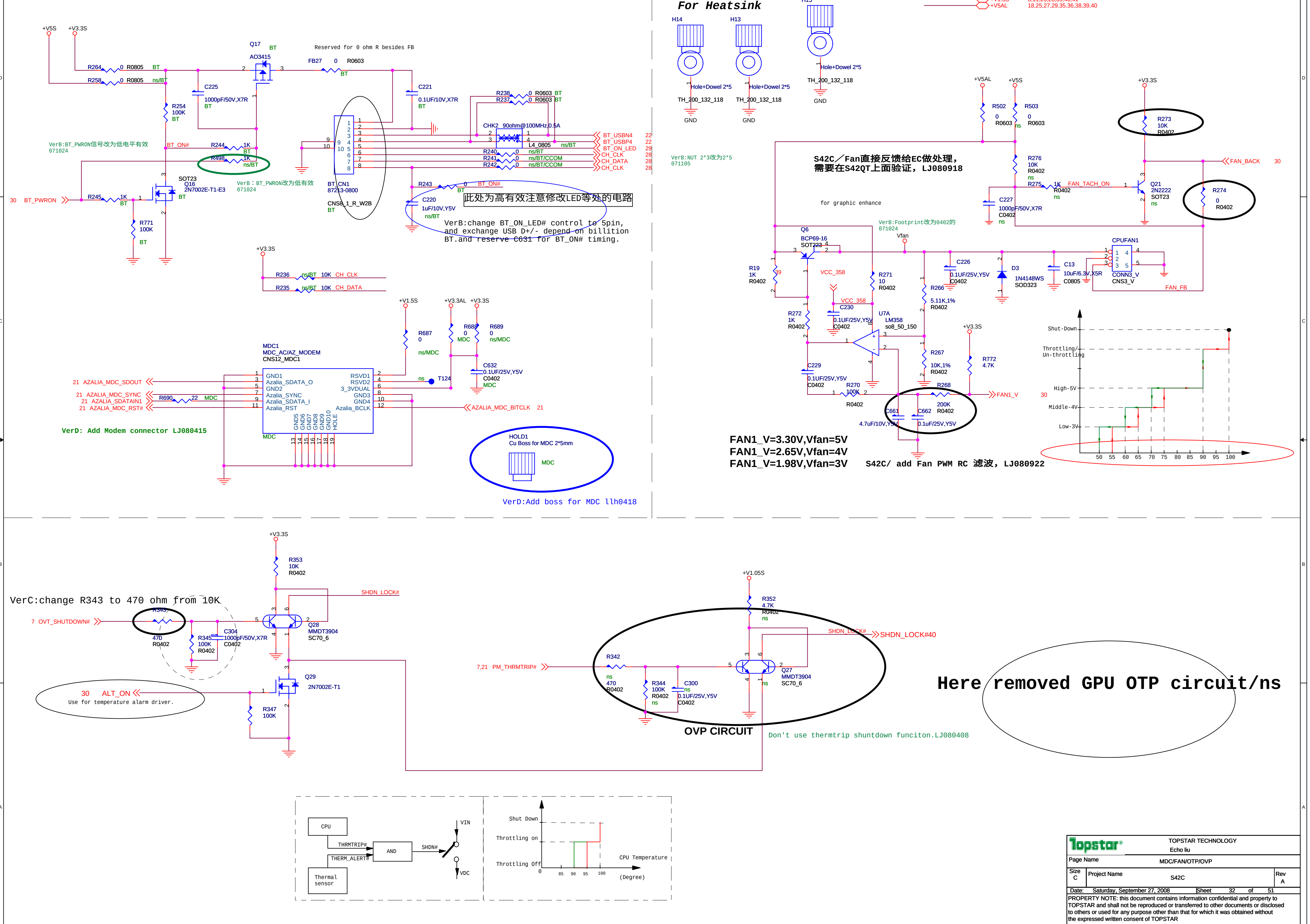
Echo liu

Page Name: Azalia audio codec(ALC880)

Size: C | Project Name: S42C | Rev: A

Date: Saturday, September 27, 2008 | Sheet 31 of 51

# FAN Controller Circuit

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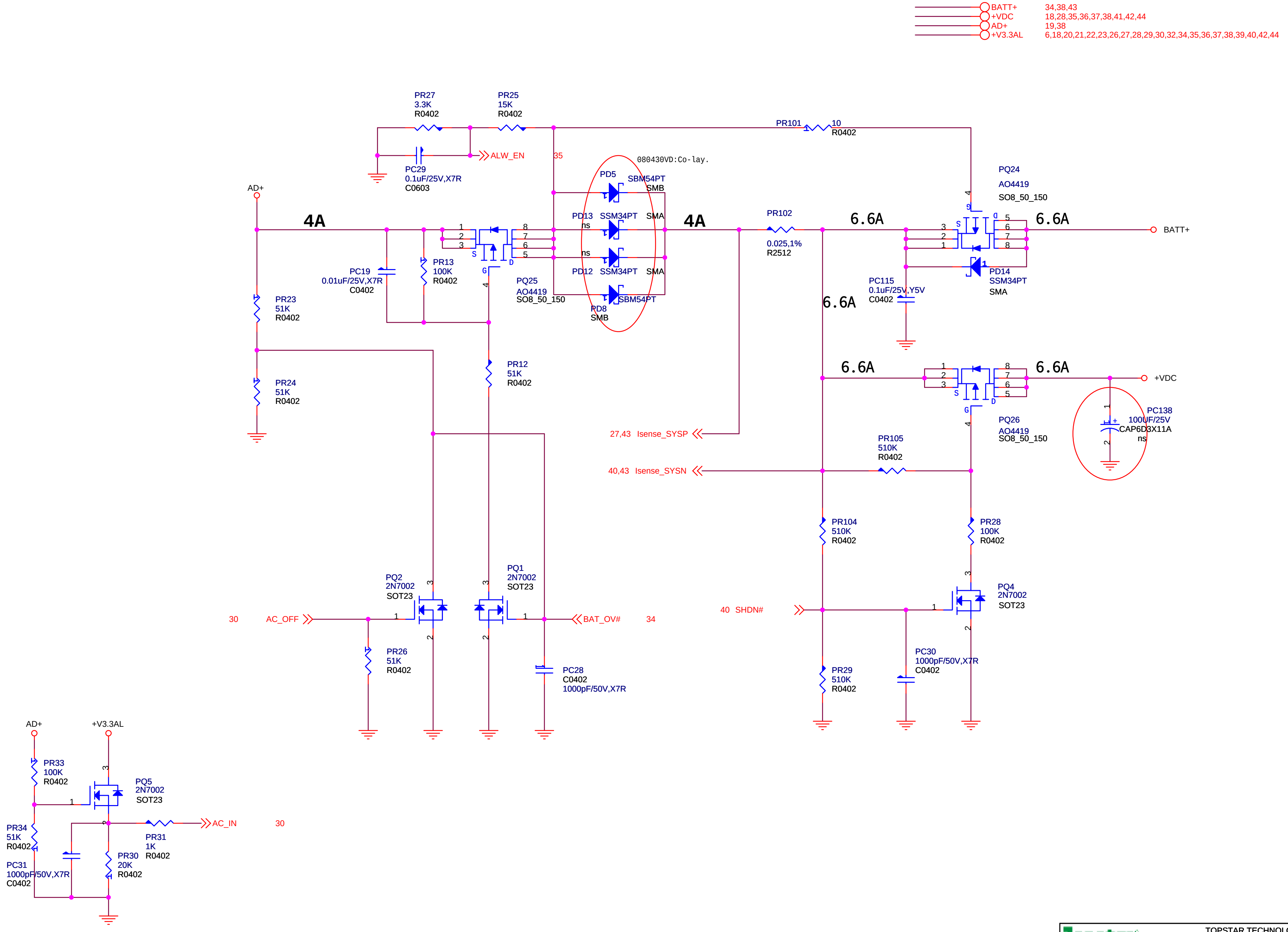
| Topstar | TOPSTAR TECHNOLOGY | | |
| | Echo liu | | |
| Page Name | MDC/FAN/OTP/OVP | | |
| Size C | Project Name | S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 32 of 51 | | |

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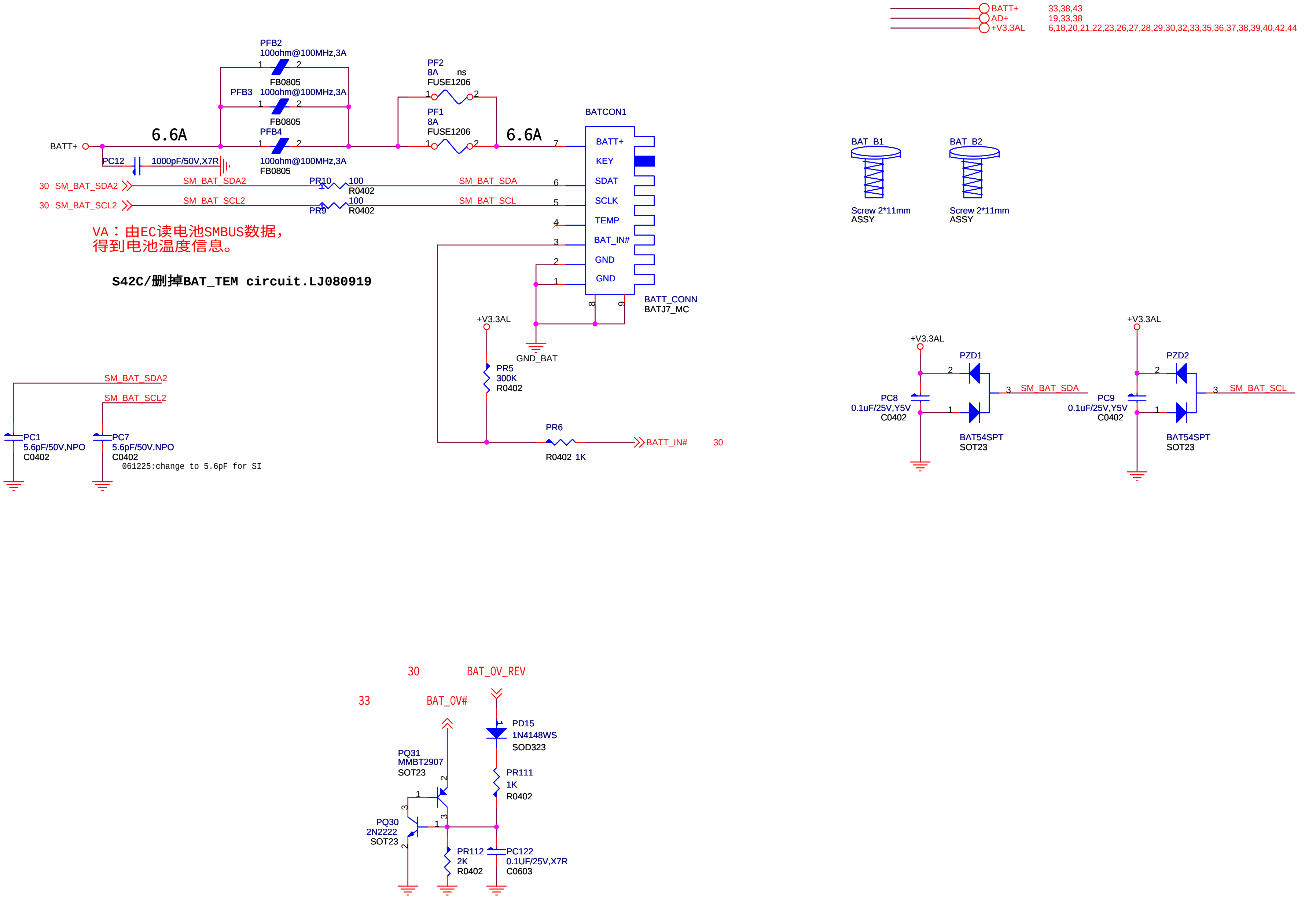
Echo liu

| Page Name | ADAPTER IN | |
|---|---|---|
| Size A3 | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 33 of 51 | |

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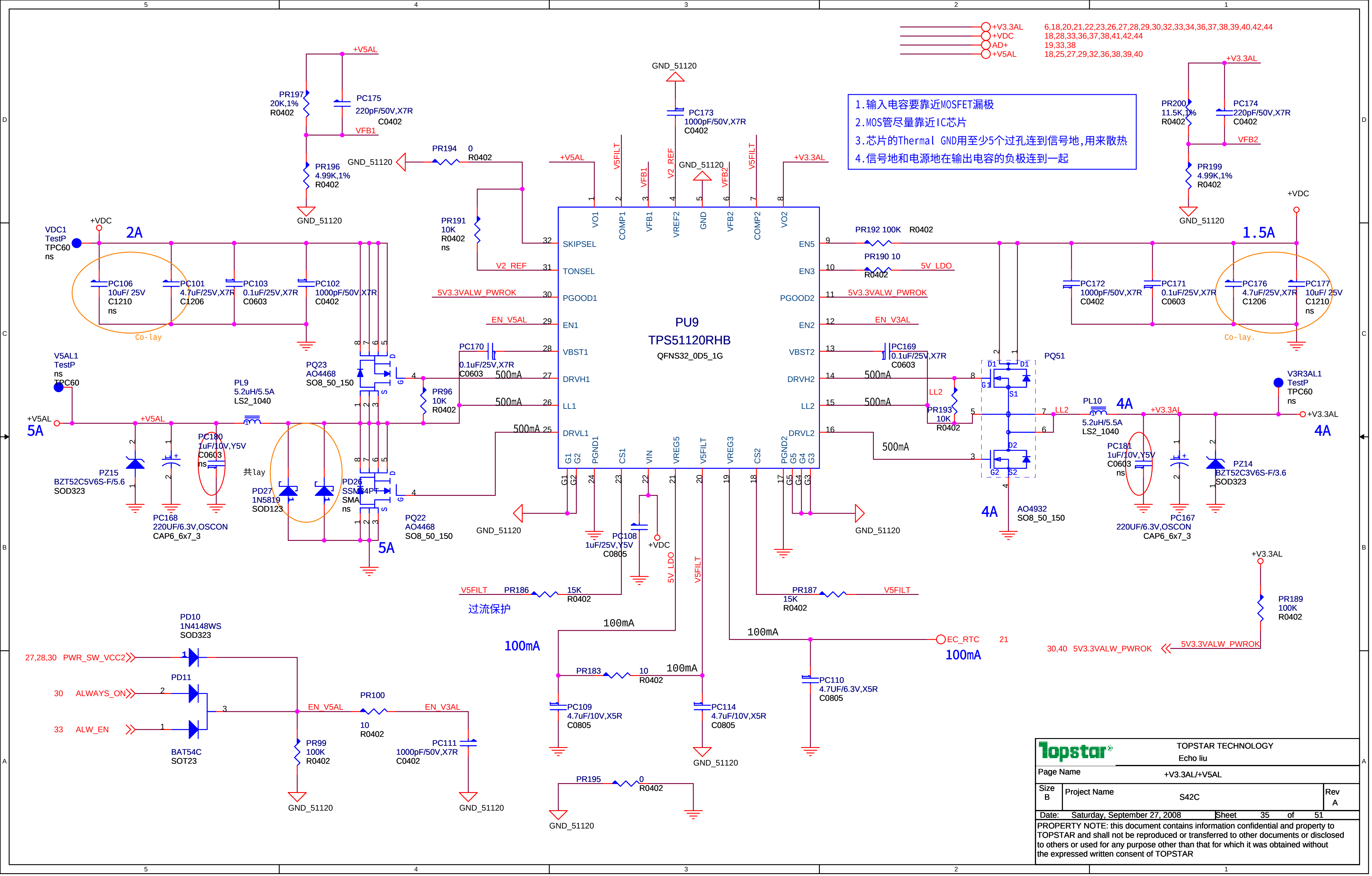
|---|---|---|
| Topstar | TOPSTAR TECHNOLOGY<br>Echo liu | |
| Page Name | BATTERY IN/OVP | |
| Size A3 | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 34 of 51 | |



1.输入电容要靠近MOSFET漏极
2.MOS管尽量靠近IC芯片
3.芯片的Thermal GND用至少5个过孔连到信号地,用来散热
4.信号地和电源地在输出电容的负极连到一起
+V3.3AL 6,18,20,21,22,23,26,27,28,29,30,32,33,34,36,37,38,39,40,42,44
+VDC 18,28,33,36,37,38,41,42,44
AD+ 19,33,38
+V5AL 18,25,27,29,32,36,38,39,40
PU9
TPS51120RHB
QFNS32_0D5_1G
SKIPSEL
TONSEL
PGOOD1
EN1
VBST1
DRVH1
LL1
DRVL1
EN5
EN3
PGOOD2
EN2
VBST2
DRVH2
LL2
DRVL2
VO1
COMP1
VFB1
VREF2
GND
VFB2
COMP2
VO2
G1
G2
PGND1
CS1
VIN
VREG5
V5FILT
VREG3
CS2
PGND2
G5
G4
G3
2A
1.5A
5A
4A
500mA
100mA
Co-lay
共lay
过流保护
PR197 20K,1% R0402
PC175 220pF/50V,X7R C0402
PR196 4.99K,1% R0402
PR194 0 R0402
PR191 10K R0402 ns
PC173 1000pF/50V,X7R C0402
PR200 11.5K,1% R0402
PC174 220pF/50V,X7R C0402
PR199 4.99K,1% R0402
PR192 100K R0402
PR190 10 R0402
VDC1 TestP TPC60 ns
PC106 10uF/ 25V C1210 ns
PC101 4.7uF/25V,X7R C1206
PC103 0.1uF/25V,X7R C0603
PC102 1000pF/50V,X7R C0402
PC172 1000pF/50V,X7R C0402
PC171 0.1uF/25V,X7R C0603
PC176 4.7uF/25V,X7R C1206
PC177 10uF/ 25V C1210 ns
V5AL1 TestP ns TPC60
PL9 5.2uH/5.5A LS2_1040
PQ23 AO4468 SO8_50_150
PC170 0.1uF/25V,X7R C0603
PR96 10K R0402
PC169 0.1uF/25V,X7R C0603
PQ51 AO4932 SO8_50_150
PR193 10K R0402
PL10 5.2uH/5.5A LS2_1040
V3R3AL1 TestP TPC60 ns
PZ15 BZT52C5V6S-F/5.6 SOD323
PC180 1uF/10V,Y5V C0603 ns
PC168 220UF/6.3V,OSCON CAP6_6x7_3
PD27 1N5819 SOD123
PD26 SSM34PT SMA ns
PQ22 AO4468 SO8_50_150
PC108 1uF/25V,Y5V C0805
PC181 1uF/10V,Y5V C0603 ns
PZ14 BZT52C3V6S-F/3.6 SOD323
PC167 220UF/6.3V,OSCON CAP6_6x7_3
PR186 15K R0402
PR187 15K R0402
PR189 100K R0402
PD10 1N4148WS SOD323
27,28,30 PWR_SW_VCC2
PD11
30 ALWAYS_ON
33 ALW_EN
BAT54C SOT23
EN_V5AL
PR100 10 R0402
EN_V3AL
PR99 100K R0402
PC111 1000pF/50V,X7R C0402
PR183 10 R0402
PC109 4.7uF/10V,X5R C0805
PC114 4.7uF/10V,X5R C0805
PC110 4.7UF/6.3V,X5R C0805
EC_RTC 21
30,40 5V3.3VALW_PWROK
PR195 0 R0402
GND_51120
Topstar
TOPSTAR TECHNOLOGY
Echo liu
Page Name +V3.3AL/+V5AL
Size B
Project Name S42C
Rev A
Date: Saturday, September 27, 2008
Sheet 35 of 51
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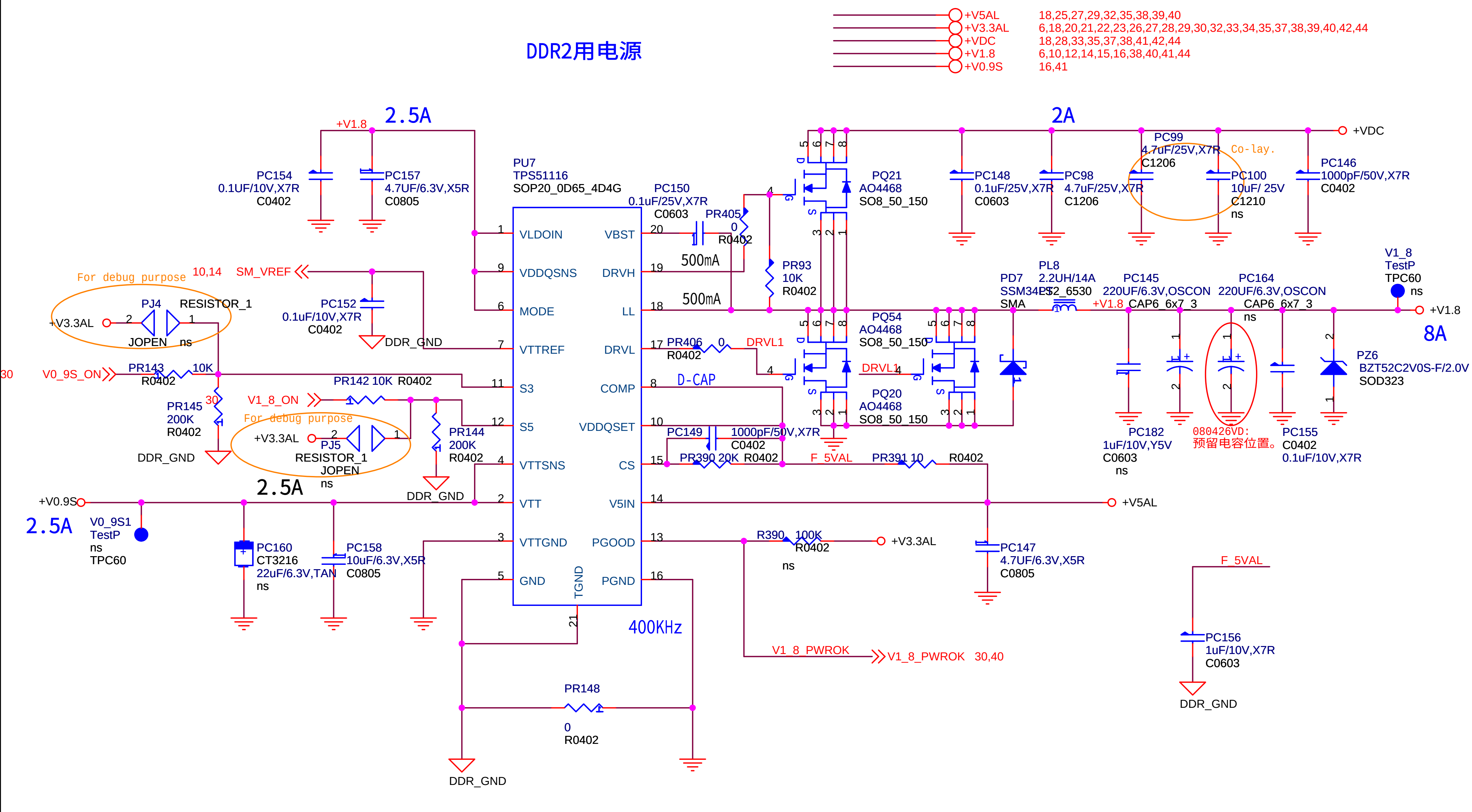
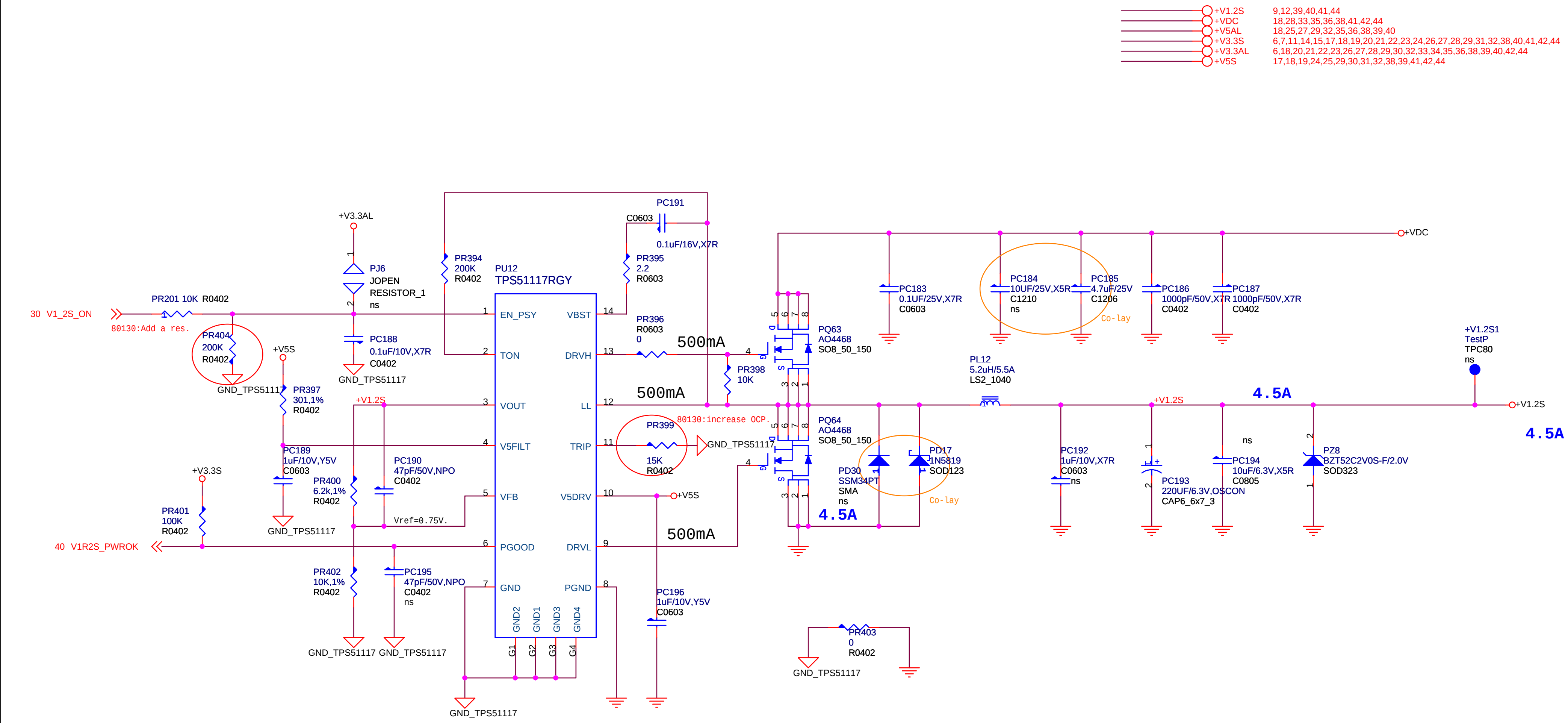
# DDR2用电源



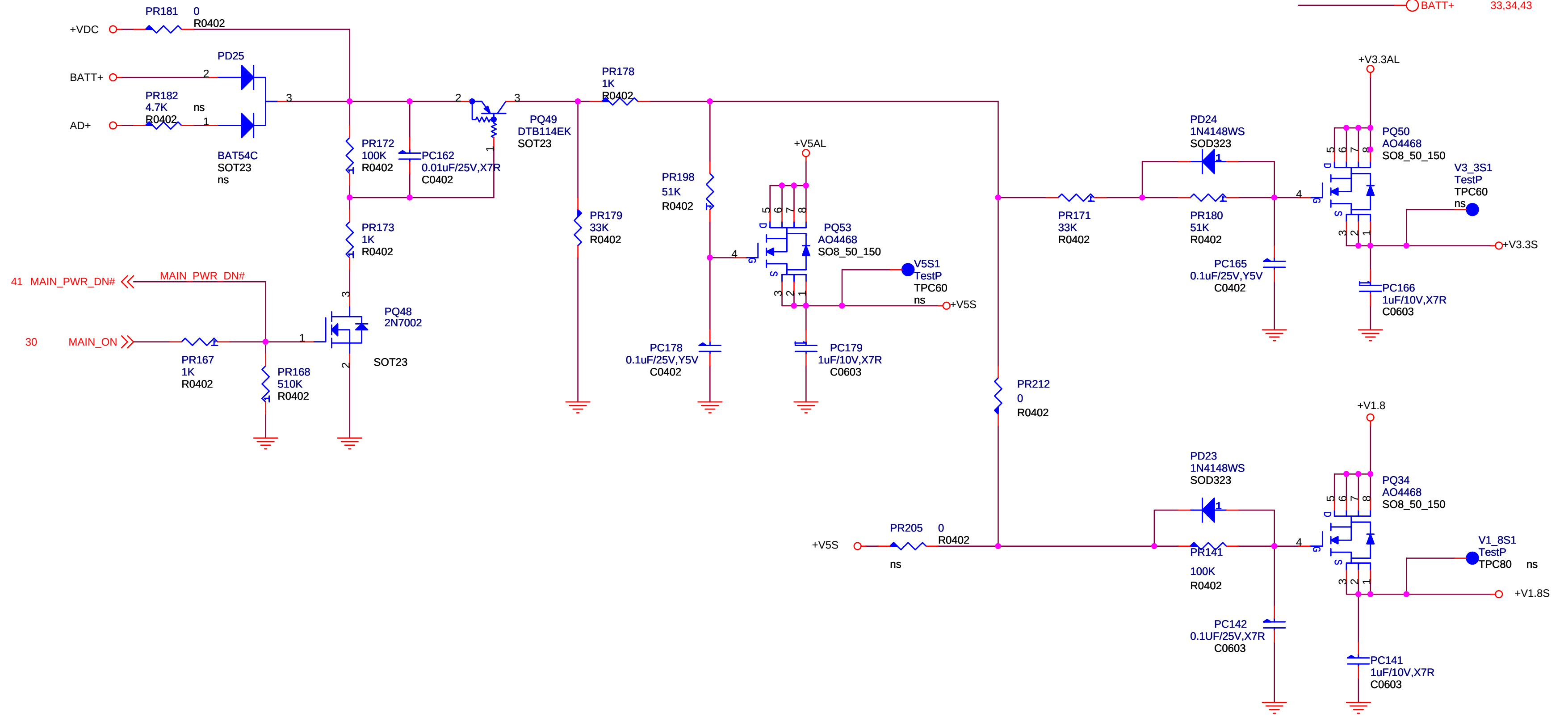

1.输入电容要靠近MOSFET漏极
2.MOS管尽量靠近IC芯片
3.芯片的Thermal GND用至少5个过孔连到信号地,用来散热
4.信号地和电源地在输出电容的负极连到一起

| | |
|---|---|
| Topstar | TOPSTAR TECHNOLOGY<br>Echo liu |
| Page Name | +V1.8/+V0.9S POWER |
| Size A4 | Project Name S42C — Rev A |
| Date: Saturday, September 27, 2008 | Sheet 36 of 51 |

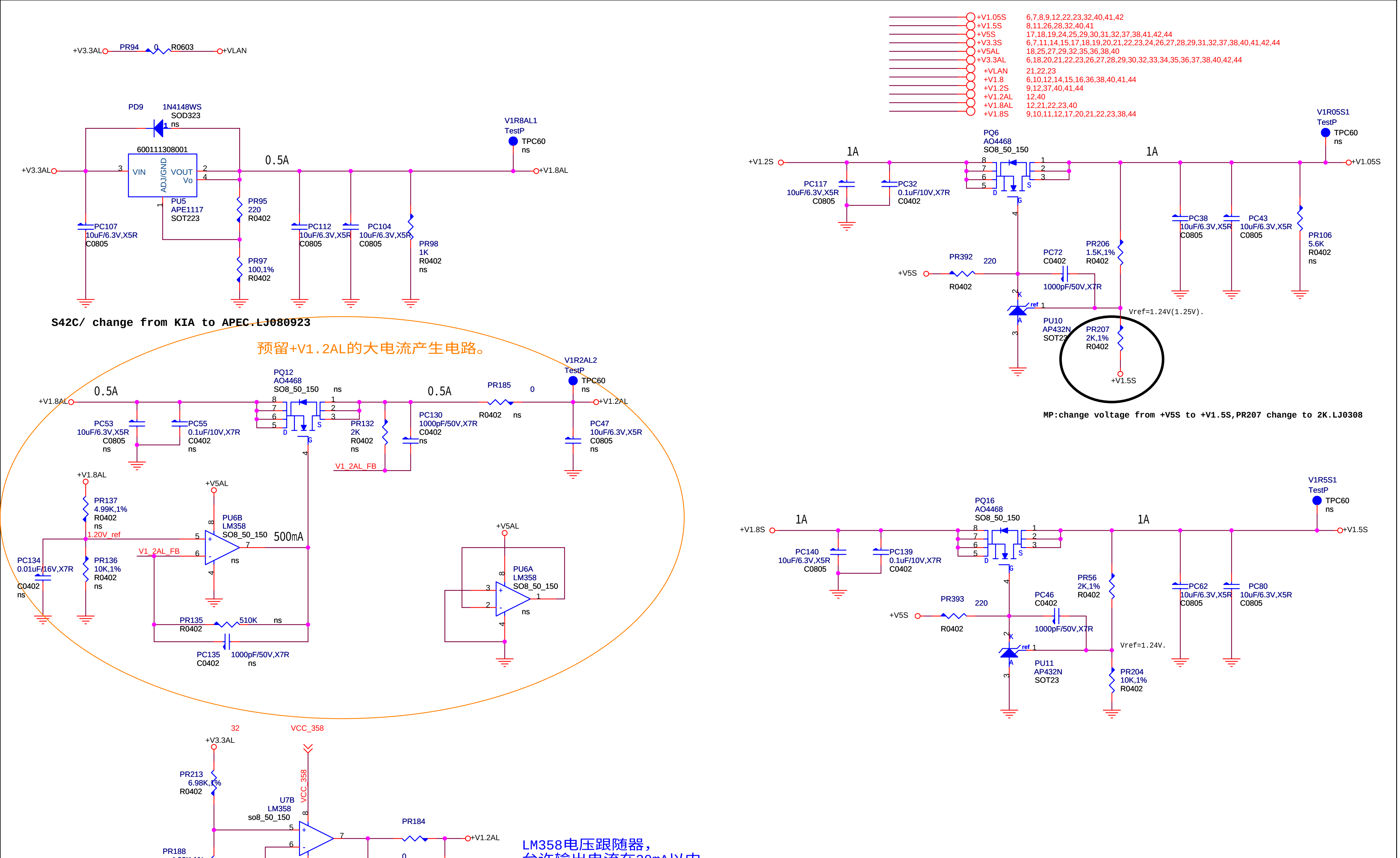



| Topstar | TOPSTAR TECHNOLOGY<br>Echo liu | |
|---|---|---|
| Page Name | +V1.2S | |
| Size A3 | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 37 of 51 | |

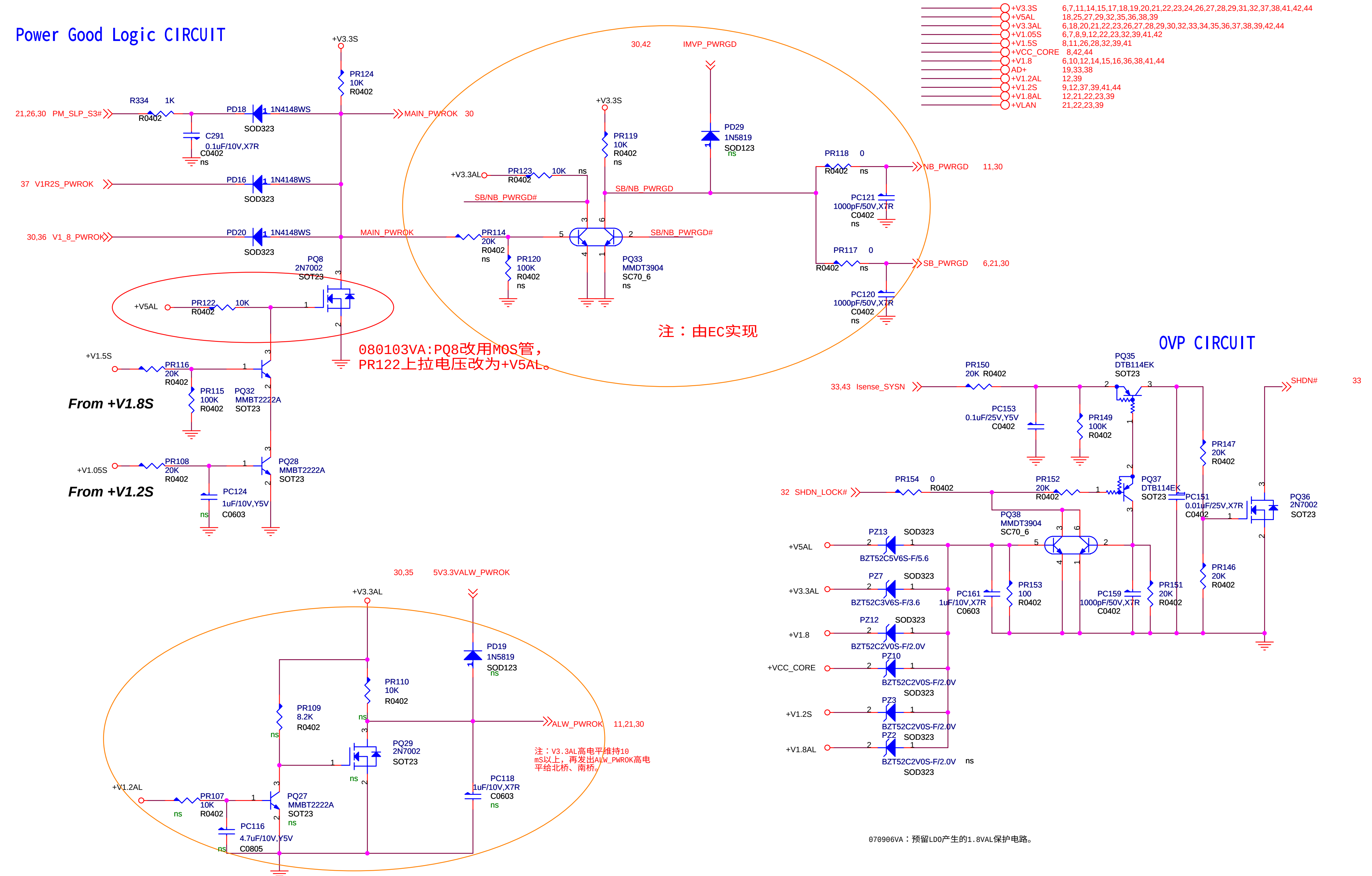
| | |
|---|---|
| +VDC | 18,28,33,35,36,37,41,42,44 |
| +V5S | 17,18,19,24,25,29,30,31,32,37,39,41,42,44 |
| +V3.3S | 6,7,11,14,15,17,18,19,20,21,22,23,24,26,27,28,29,31,32,37,40,41,42,44 |
| +V5AL | 18,25,27,29,32,35,36,39,40 |
| +V3.3AL | 6,18,20,21,22,23,26,27,28,29,30,32,33,34,35,36,37,39,40,42,44 |
| +V1.5S | 8,11,26,28,32,39,40,41 |
| +V1.8S | 9,10,11,12,17,20,21,22,23,39,44 |
| +V1.8 | 6,10,12,14,15,16,36,40,41,44 |
| AD+ | 19,33 |
| BATT+ | 33,34,43 |




| | | |
|---|---|---|
| Topstar | TOPSTAR TECHNOLOGY<br>Echo liu | |
| Page Name | V5S/ V3.3S/ V1.8S Power | |
| Size A3 | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 38 of 51 | |




| | | |
|---|---|---|
| Topstar | TOPSTAR TECHNOLOGY<br>Echo liu | |
| Page Name | 2.5AL/1.8AL/1.5S/1.05S LDO | |
| Size A3 | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 39 of 51 | |

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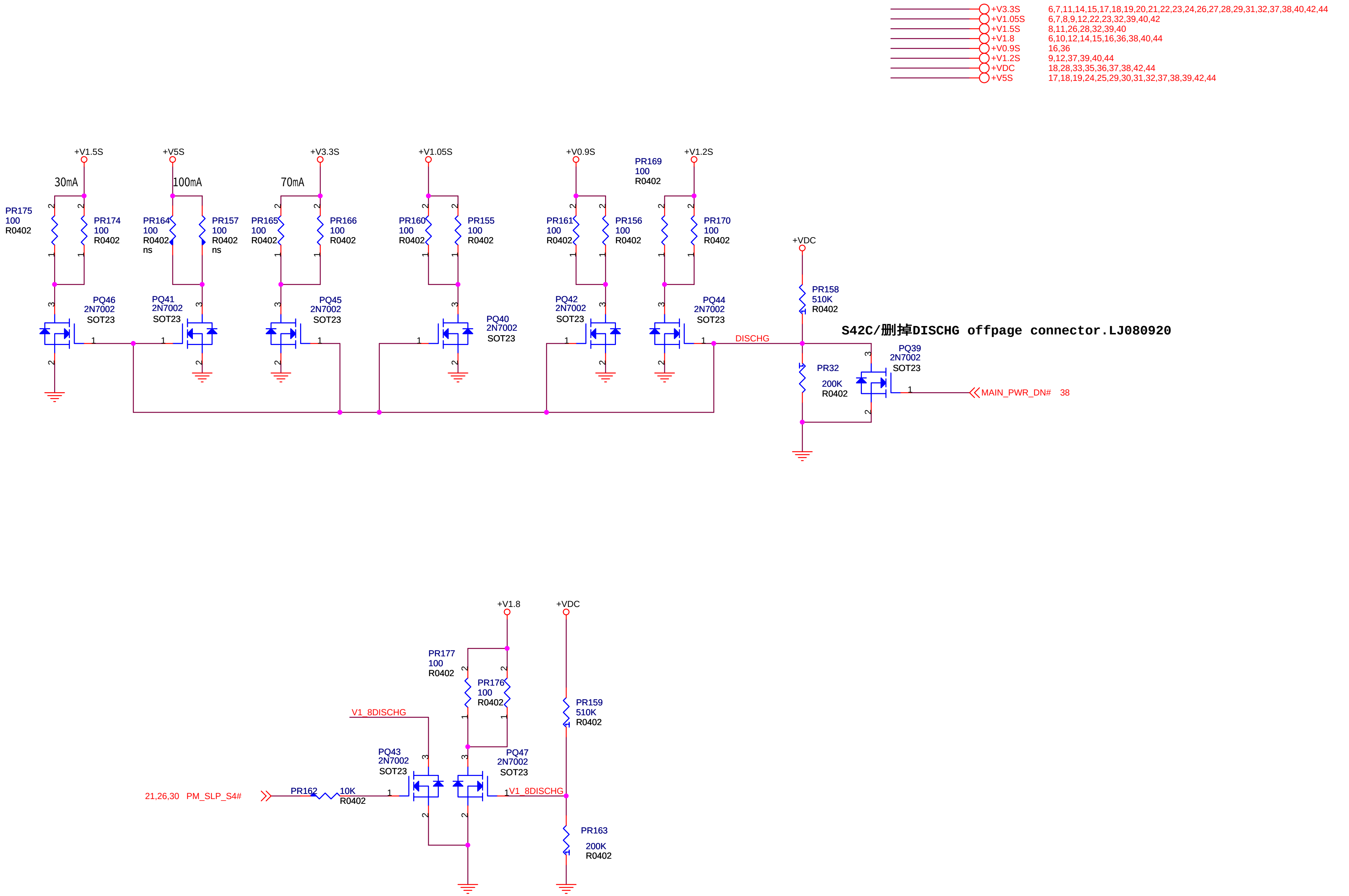
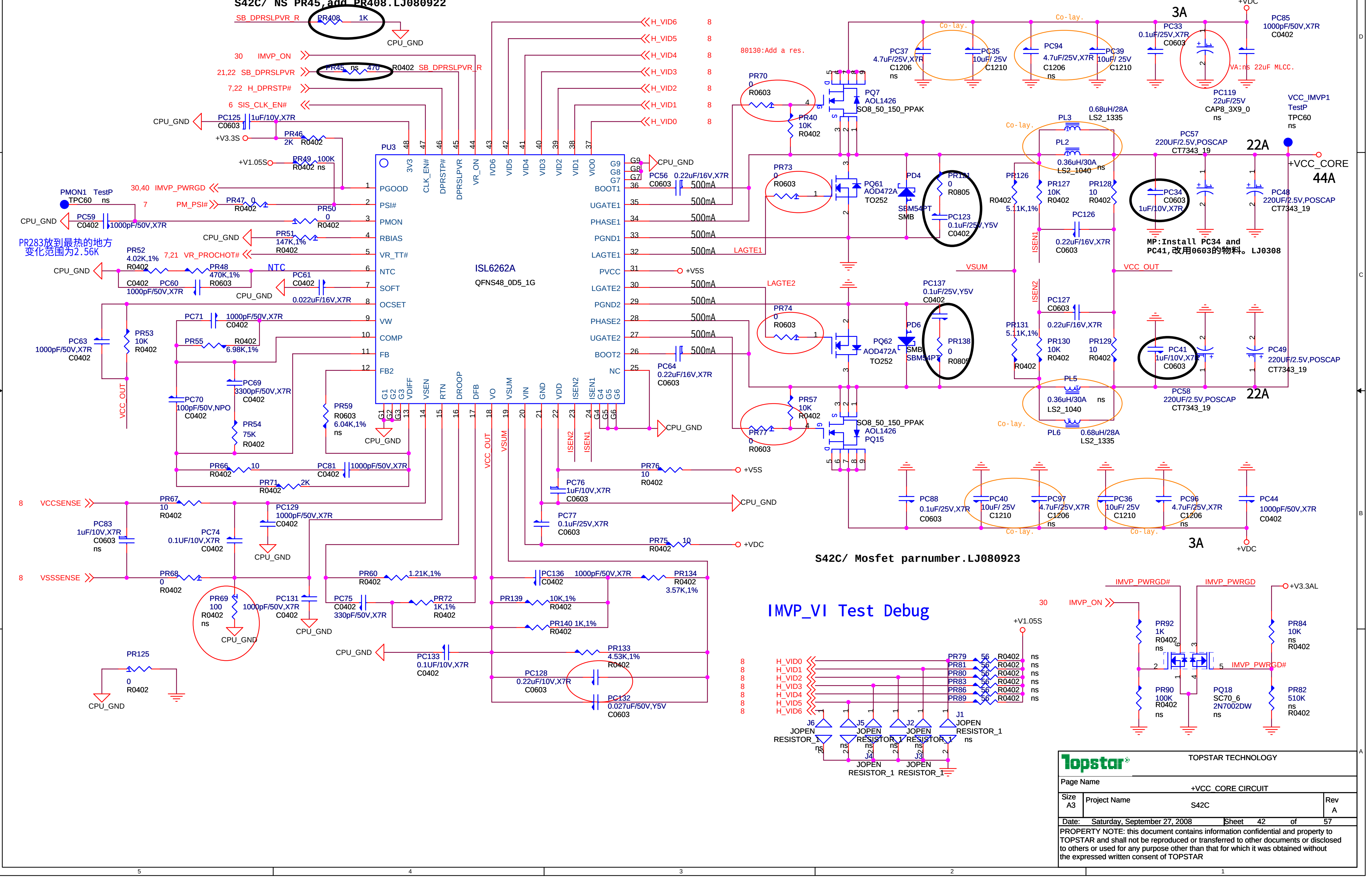
| | |
|---|---|
| Page Name | Power Good Logic / OVP |
| Size A3 | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 40 of 51 |



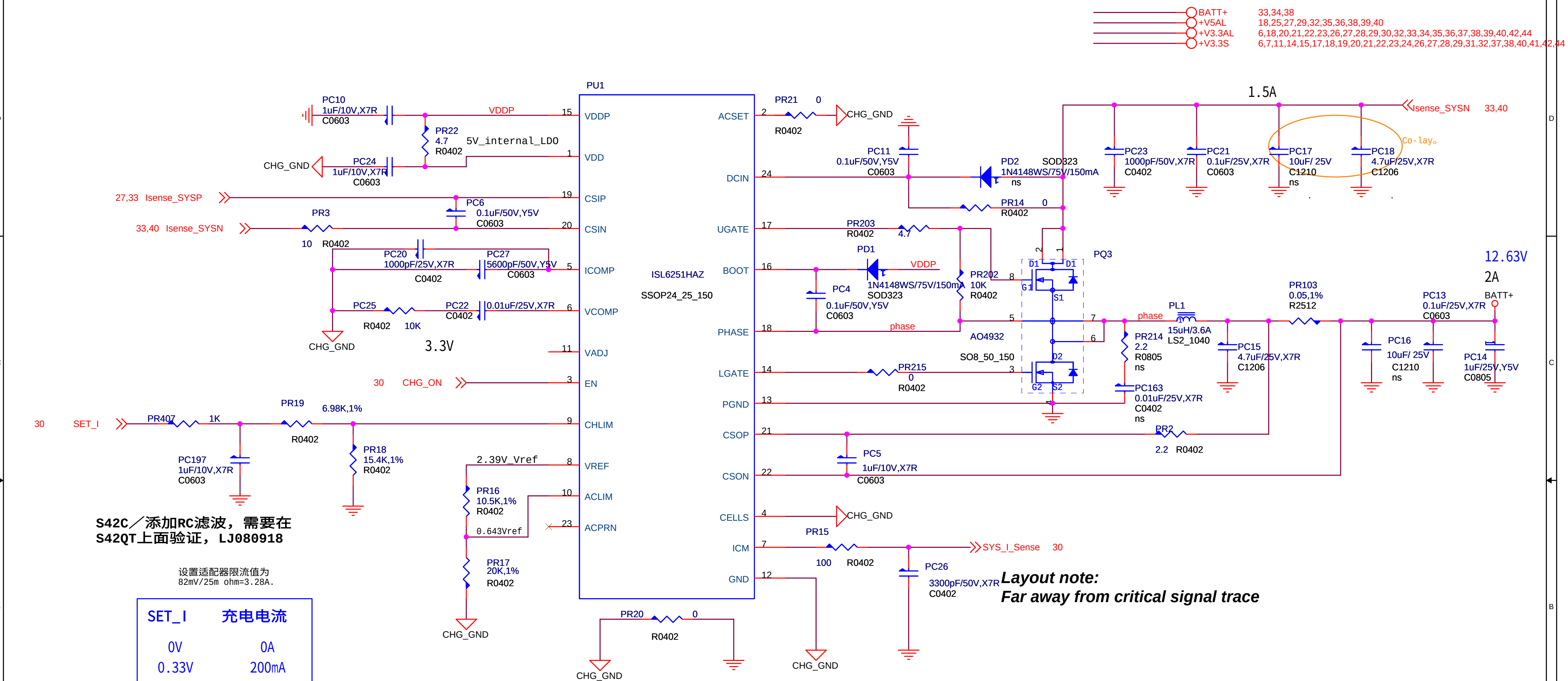

| | | | |
|---|---|---|---|
| Topstar | TOPSTAR TECHNOLOGY<br>Echo liu | | |
| Page Name | Discharge Circuit | | |
| Size A3 | Project Name | S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 41 of 51 | | |

Note:
Pin45/DPRSLPVR: 3.3V level
Vih=2.3V;Vil=1.0V
Pin46/DPRSTP#:1.0V Level
Vih=0.3V;Vil=0.7V

S42C/ NS PR45,add PR408.LJ080922




| | | | |
|---|---|---|---|
| Topstar | TOPSTAR TECHNOLOGY | | |
| Page Name | +VCC_CORE CIRCUIT | | |
| Size A3 | Project Name S42C | | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 42 | of 57 | |




*Layout note:*
*Far away from critical signal trace*

**S42C／添加RC滤波，需要在S42QT上面验证，LJ080918**

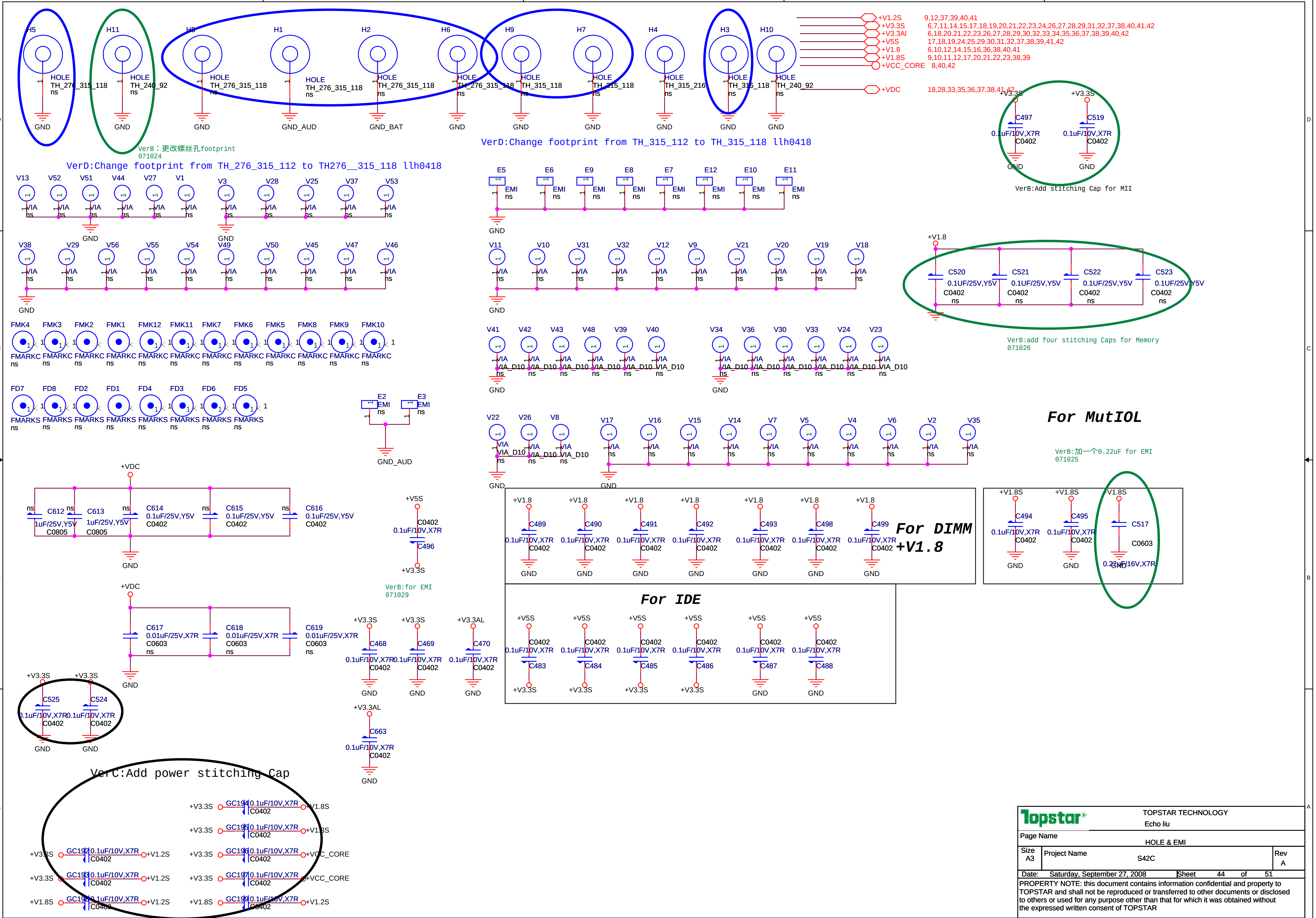
设置适配器限流值为
82mV/25m ohm=3.28A.

| SET_I | 充电电流 |
|---|---|
| 0V | 0A |
| 0.33V | 200mA |
| 2V | 1.2A |
| 3.3V | 2A |

| SYS_I_Sense | SYS_CURRENT |
|---|---|
| | 1A |
| 500mV | 3A |
| 1.5V | 3.33A |
| 1.67V | |

| SYS_CURRENT | SYS_I_Sense |
|---|---|
| >3.6A | >1.8V |
| <3A | <1.5V |

| | | |
|---|---|---|
| Topstar | TOPSTAR TECHNOLOGY<br>Echo liu | |
| Page Name | CHARGER(ISL6251) | |
| Size B | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 43 of 51 | |

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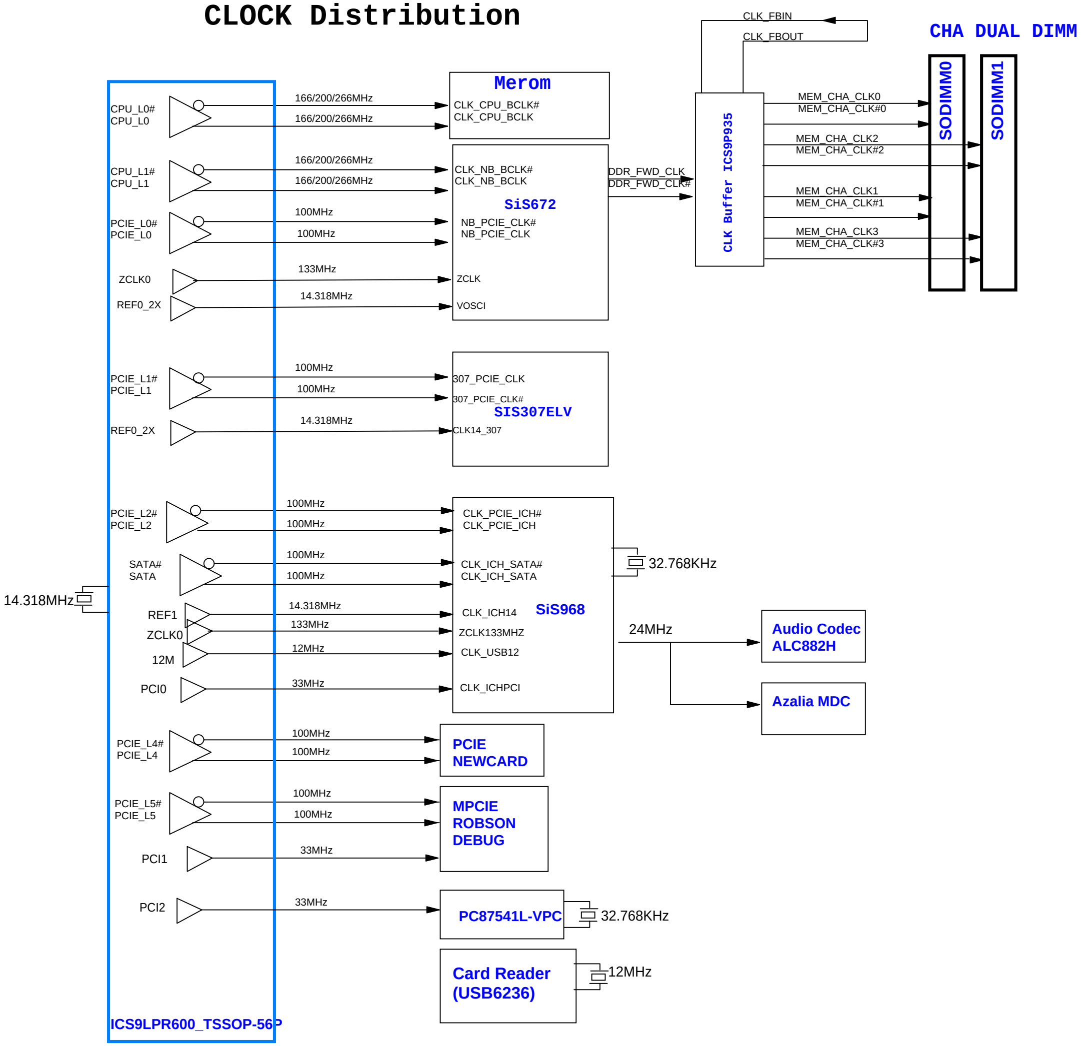
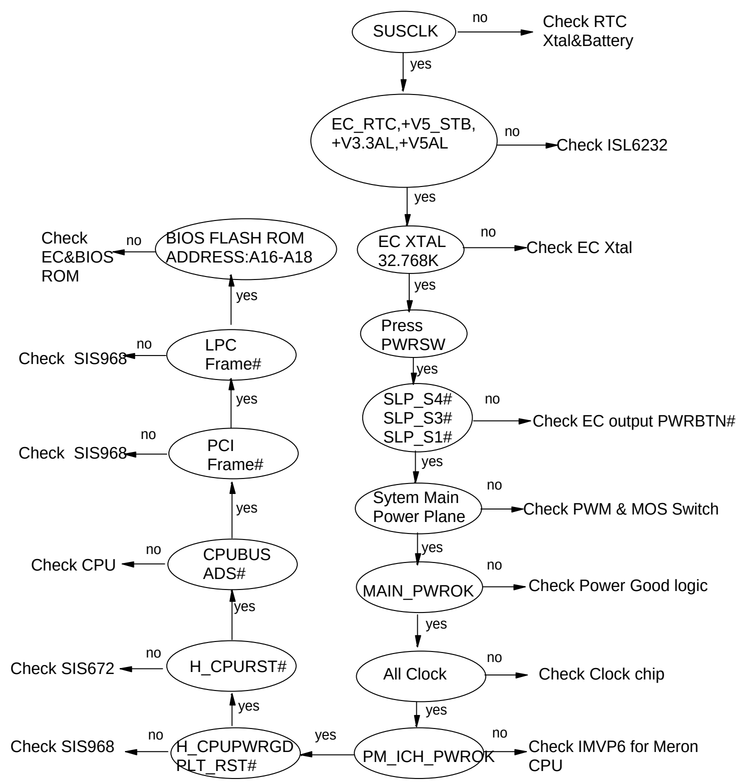
Echo liu

| | | |
|---|---|---|
| Page Name | HOLE & EMI | |
| Size A3 | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 44 of 51 | |

# CLOCK Distribution

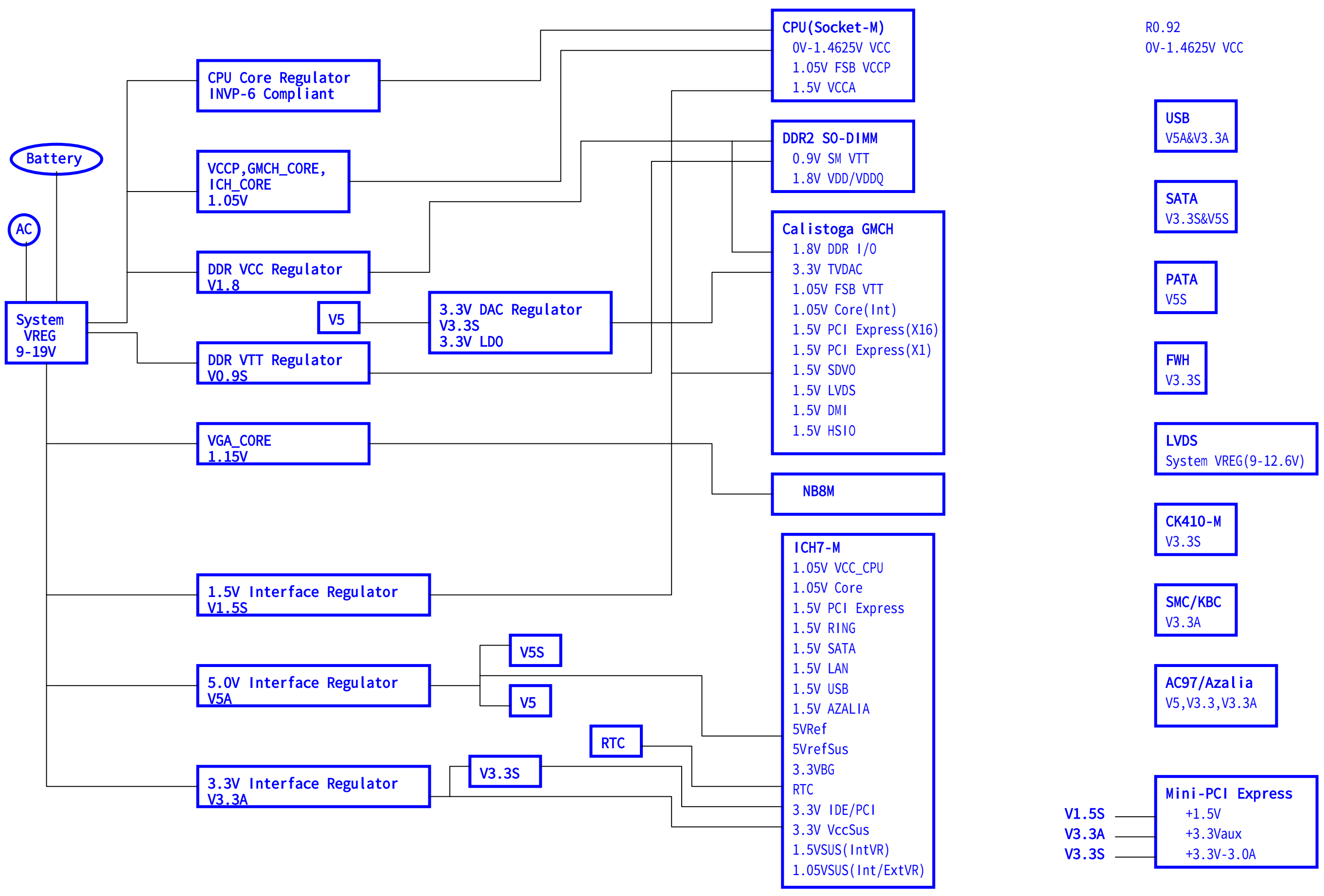



## ADAPTER MODE

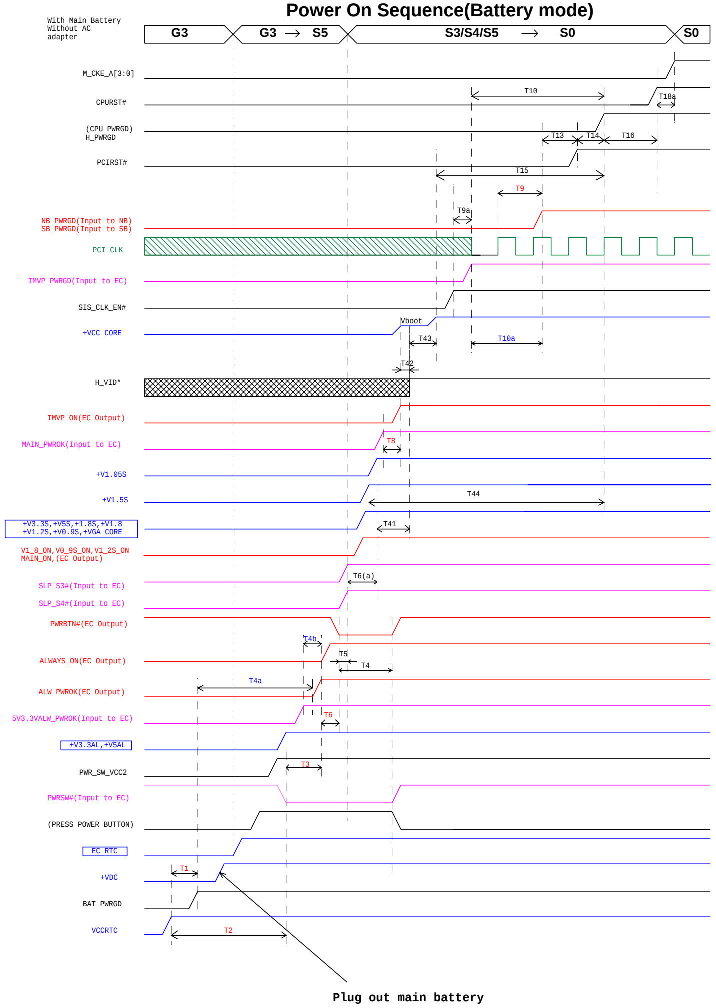



| | | |
|---|---|---|
| Topstar | TOPSTAR TECHNOLOGY | Echo liu |
| Page Name | Clock Distribution | |
| Size C | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 45 of 51 | |

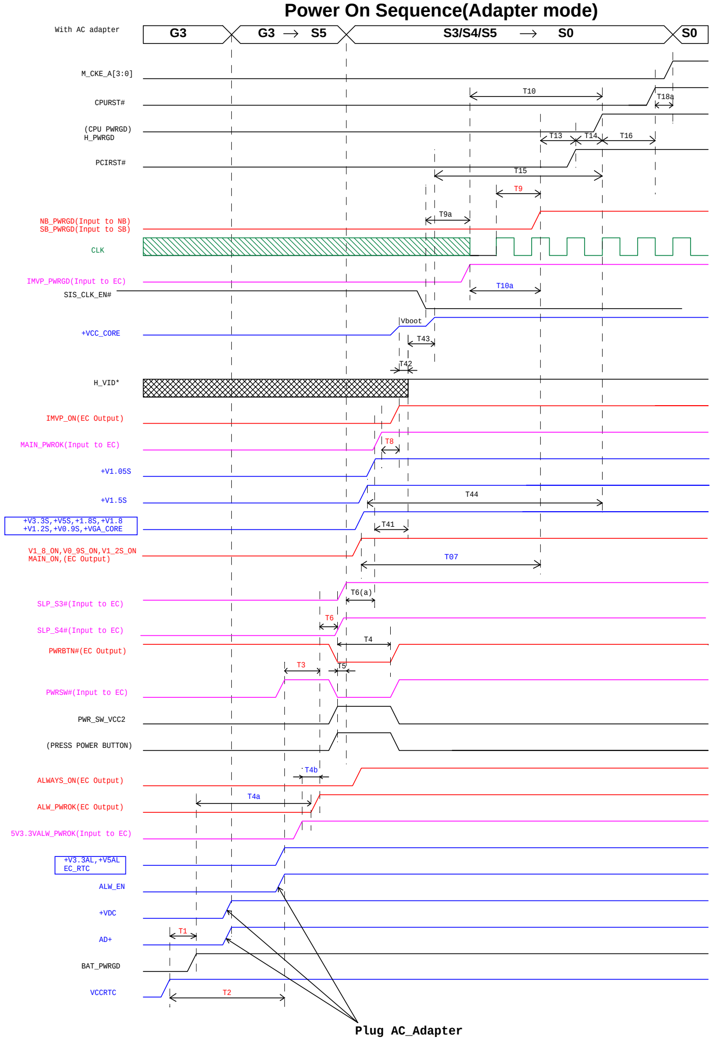
# POWER Distribution



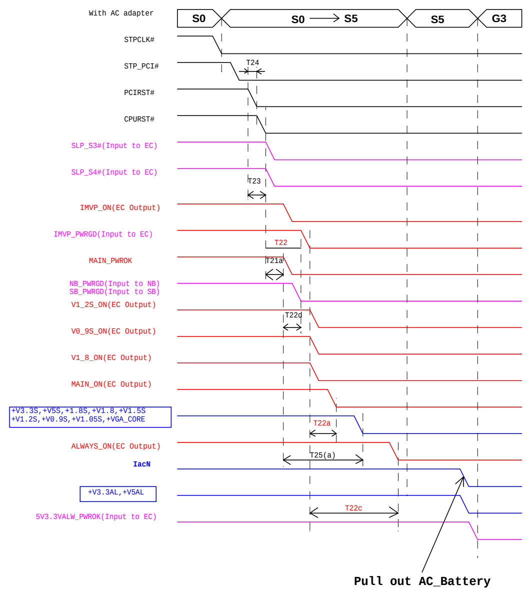
## Power On Sequence(Battery mode)



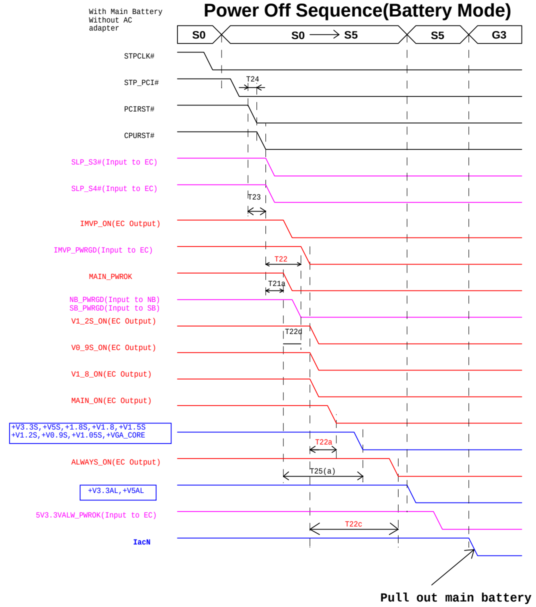

## Power On Sequence(Adapter mode)




## Power Off Sequence(Adapter Mode)

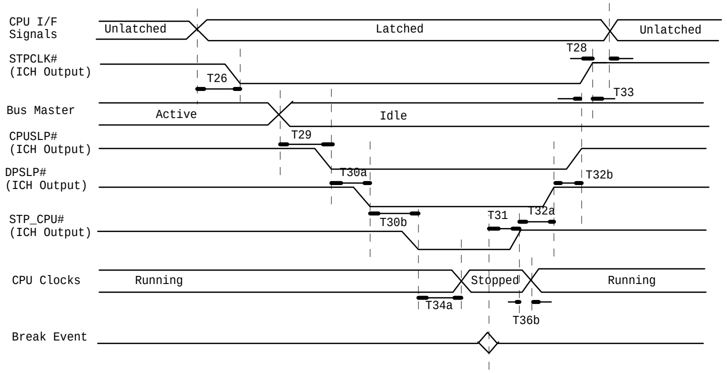



## Power Off Sequence(Battery Mode)

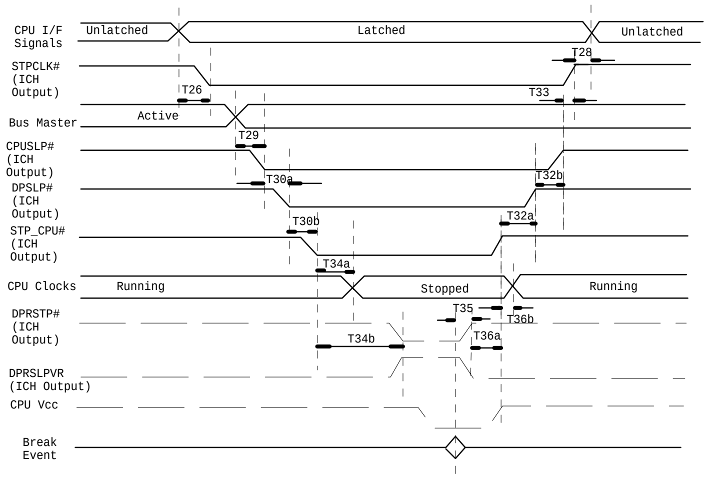



| | |
|---|---|
| Topstar | TOPSTAR TECHNOLOGY |
| Page Name | Power ON/OFF Timing |
| Size: Custom | Project Name: S42C — Rev: A |
| Date: Saturday, September 27, 2008 | Sheet 47 of 51 |

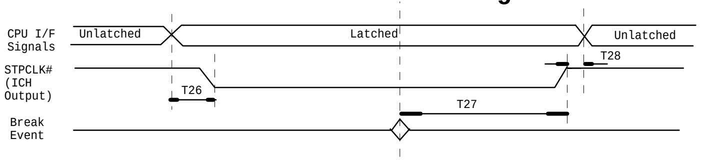
# C0 to C3 to C0 Timings



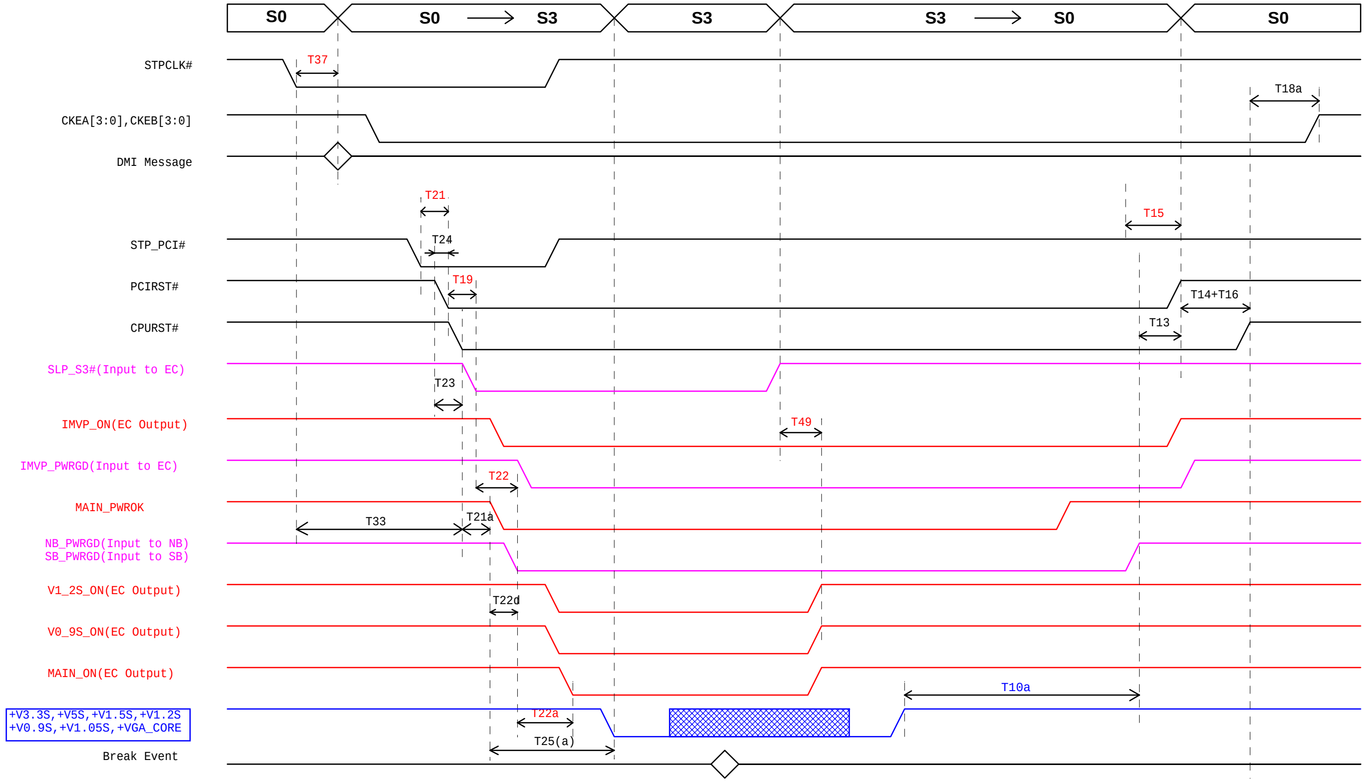

# C0 to C4 to C0 Timings




# C0 to C2 to C0 Timings




# S0 to S3 to S0 Timing




| | | |
|---|---|---|
| Topstar | TOPSTAR TECHNOLOGY | |
| Page Name | ACPI mode switch timings | |
| Size Custom | Project Name S42C | Rev A |
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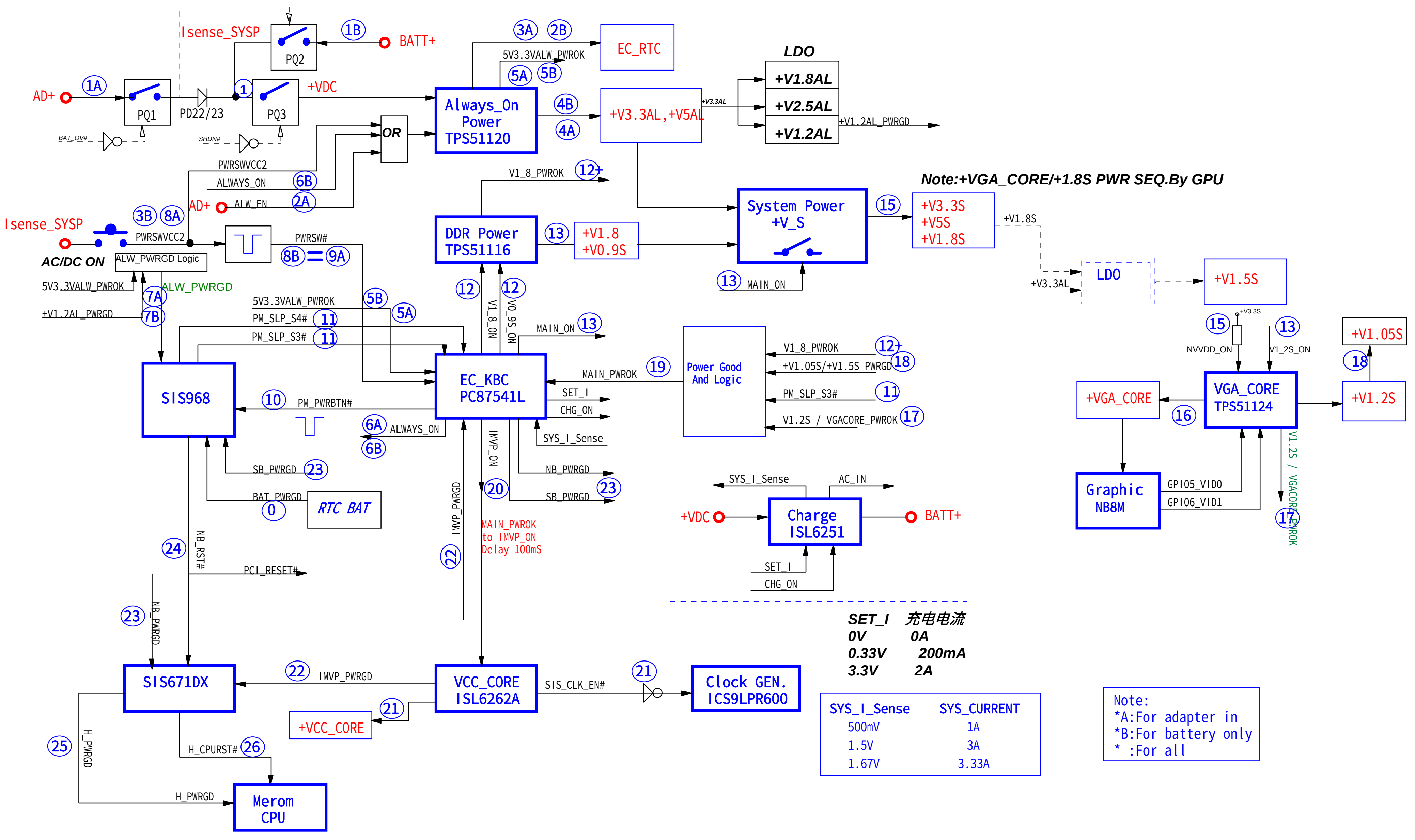


| SET_I | 充电电流 |
|---|---|
| 0V | 0A |
| 0.33V | 200mA |
| 3.3V | 2A |

| SYS_I_Sense | SYS_CURRENT |
|---|---|
| 500mV | 1A |
| 1.5V | 3A |
| 1.67V | 3.33A |

Note:
*A:For adapter in
*B:For battery only
* :For all

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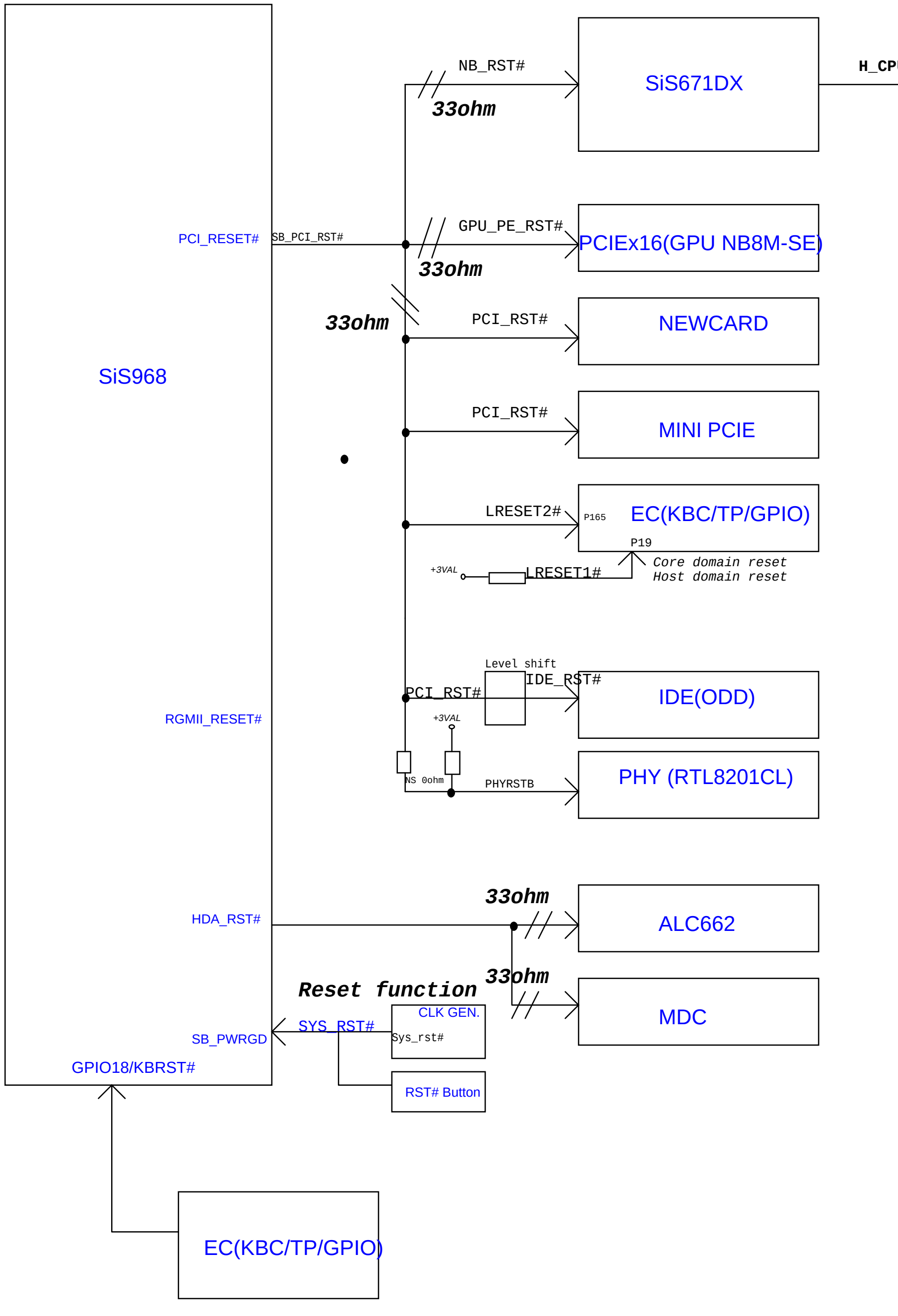
Page Name: PowerOnSequence & Reset Map

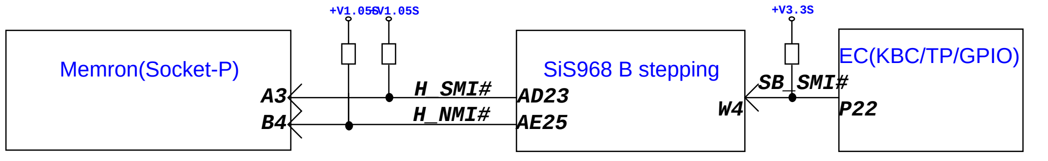
Size A3 | Project Name: S42C | Rev A

Date: Saturday, September 27, 2008 | Sheet 49 of 51

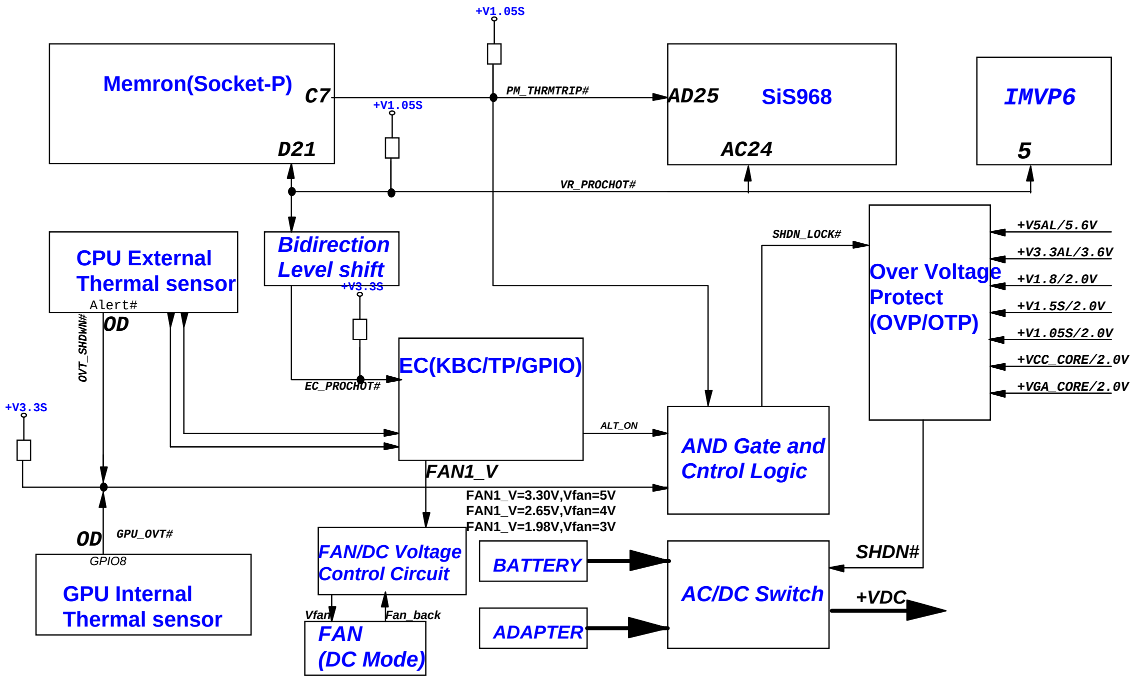
# RESET Mapping




# SMI#/NMI# Toplogy




# Thermal/FAN/OVP/OTP Control Logic Mapping

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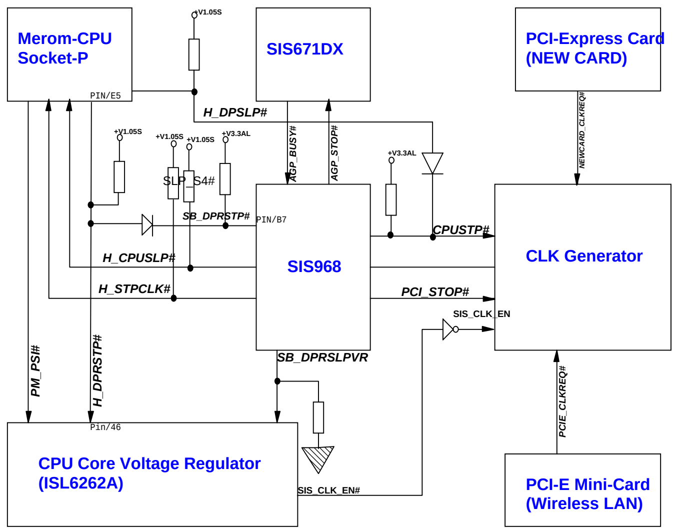
| | | | |
|---|---|---|---|
| Page Name | RESET/NMI/SMI/THERMAL/OV(T)P | | |
| Size A3 | Project Name S42C | | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 50 of 51 | | |

# SIS968 GPIO Routing

| Pin Name | Type | Power | Net Name | Description | Default Used |
|---|---|---|---|---|---|
| GPIO0 | I/O | +V3.3S | CPUSTP# | For CPU C State Control,Output toCLK IC stop CPU clk | CPUSTP# |
| GPIO1 | I/O | +V3.3S | N/A | BIOS Configuration for output | NC/output |
| GPIO2 | I/O | +V3.3S | PM_THRM# | Thermal information from EC | PM_THRM#/Input |
| GPIO3 | I/O | +V3.3S | SB_EXTSMI# | SMI From EC not used | NC/output |
| GPIO4 | I/O | +V3.3S | PM_CLKRUN# | CLKRUN# From EC | PM_CLKRUN#/Input |
| GPIO5 | I/O | +V3.3S | PANEL_ID1 | Not used | NC/output |
| GPIO6 | I/O | +V3.3S | PANEL_ID0 | Not used | NC/output |
| GPIO7 | I | +V3.3AL | PM_BATLOW# | EC Ouput Low When Detected BAT Voltage too lower?? | PM_BATLOW# |
| GPIO8 | I/O | +V3.3AL | SB_RING | Ring up wakeup function(Pulse >4ms) | NC/output |
| GPIO9 | I/O | +V3.3AL | EC_RUNTIME_SCI# | Embedded controller SCI Interrupt to SIS968 | EC_RUNTIME_SCI#/Input |
| GPIO10 | O/PU | +V3.3AL | SLP_S4# | SIS968 Only as SLP_S5# function | SLP_S4# |
| GPIO11 | I/O/OD | +V3.3AL | PCI_STOP# | For STOP PCI CLKS with S/W setup by I2C | PCI_STOP#/Output |
| GPIO12 | I/O/OD | +V3.3AL | DPSLP# | For CPU C State Control | DPSLP# |
| GPIO13 | I/O | +V3.3AL | SB_DPRSLPVR | CPU Deep Sleep control for VR | SB_DPRSLPVR/Output |
| GPIO14 | I/O/OD | +V3.3AL | AGP_STOP# | STOP AGP CLKs For 671DX Not used | AGP_STOP#/Output |
| GPIO15 | O/PU | +V3.3AL | SLP_S3# | SIS968 Only as SLP_S3# function | SLP_S3# |
| GPIO16 | I/O/OD | +V3.3AL | SB_DPRSTP# | For CPU C State Control /Ouput | SB_DPRSTP#/Output |
| GPIO17 | I/O | +V3.3AL | H_A20GATE# | A20GATE# from KBC,when active, use to force A20M# signal active/ | H_A20GATE# |
| GPIO18 | I/O | +V3.3AL | H_RCIN# | Keyboard Reset input from KBC | H_RCIN#/Input |
| GPIO19 | O/PU | +V3.3S | SMBCLK | SIS968 SMBUS Master Controller CLK | SMBCLK |
| GPIO20 | I/O/PU | +V3.3S | SMBDATA | SIS968 SMBUS Master Controller DATA | SMBDATA |
| GPIO21 | O | +V3.3AL | EESK | GMAC EEPROM CLK | EESK |
| GPIO22 | O | +V3.3AL | EEDI | GMAC EEPROM DATA OUTPUT FROM SIS968 | EEDI |
| GPIO23 | I | +V3.3AL | EEDO | GMAC EEPROM DATA INPUT TO SIS968 | EEDO |
| GPIO24 | O | +V3.3AL | EECS | GMAC EEPROM CHIP SELECT | EECS |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

# CPU C State CONTROL TOPLOGY




# Embeded Controller GPIO Routing After updating from R18P VC

| | | | | |
|---|---|---|---|---|
| Pin165 | I | Digital | EC_LPC_RST# | Host domain reset(LPC/Host controlled/Shared memory host) |
| Pin5 | O | Digital | A20GATE | HIGH LEVEL AFTER PCI RESET# SO DOUBLE CHECK AGAIN?? |
| Pin110 | I | Digital | ALW_PWROK | Used for EC detected AlW_PWRGD |
| Pin63 | O | Digital | V1_2S_ON | |
| Pin156 | I | Digital | 5V3.3VALW_PWROK | |
| Pin90 | I | Analog | AD7 | |
| Pin102 | O | Digital | NB_PWRGD | |
| Pin32 | O | Digital | SB_PWRGD | |
| Pin43 | I | Digital | Media | HW pull high/NOT USED |
| Pin176 | I | Digital | FAN_BACK | HW pull high/NOT USED |
| Pin44 | I | Digital | CPPE#_GPU_OVT# | HW pull high/NOT USED |
| Pin24 | I | Digital | EC_PMSUSStat# | Platform don't have PM_SUS_SATA# |
| Pin30 | I | Digital | PCIE_WAKE# | HW pull high/NOT USED |
| Pin23 | O | Digital | PWUREQ# | HW pull high/NOT USED |
| Pin43 | I | Digital | RY/BY# | Bios Flsah Ready or Busy,default NC |
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|---|---|---|
| Page Name | RESET/NMI/SMI/THERMAL/OV(T)P | |
| Size C | Project Name S42C | Rev A |
| Date: Saturday, September 27, 2008 | Sheet 51 of 51 | |