Topstar Digital technologies Co.,LTD

Board name: MotherBoard Schematic
Project name: M42P
Version: VerB
Initial Date: Sep.22, 2007

Topstar Confidential

Hardware drawing by:

Hardware check by:

EMI Check by:

Power drawing by:

Power check by:

Manager Sign by:

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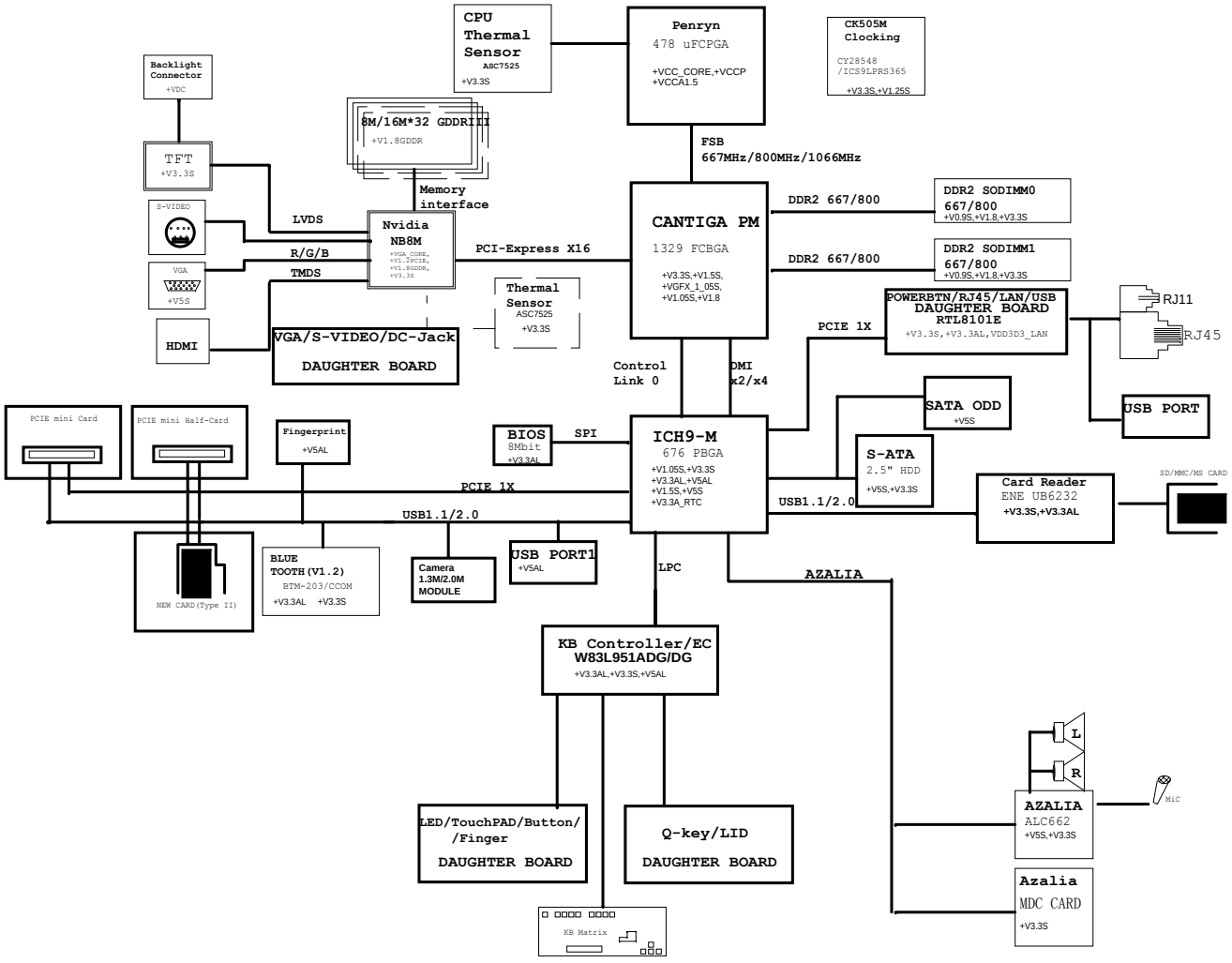
ShenZhen Topstar Industry Co.,LTD

M42 SYSTEM BLOCK Ver:A



CONTENT

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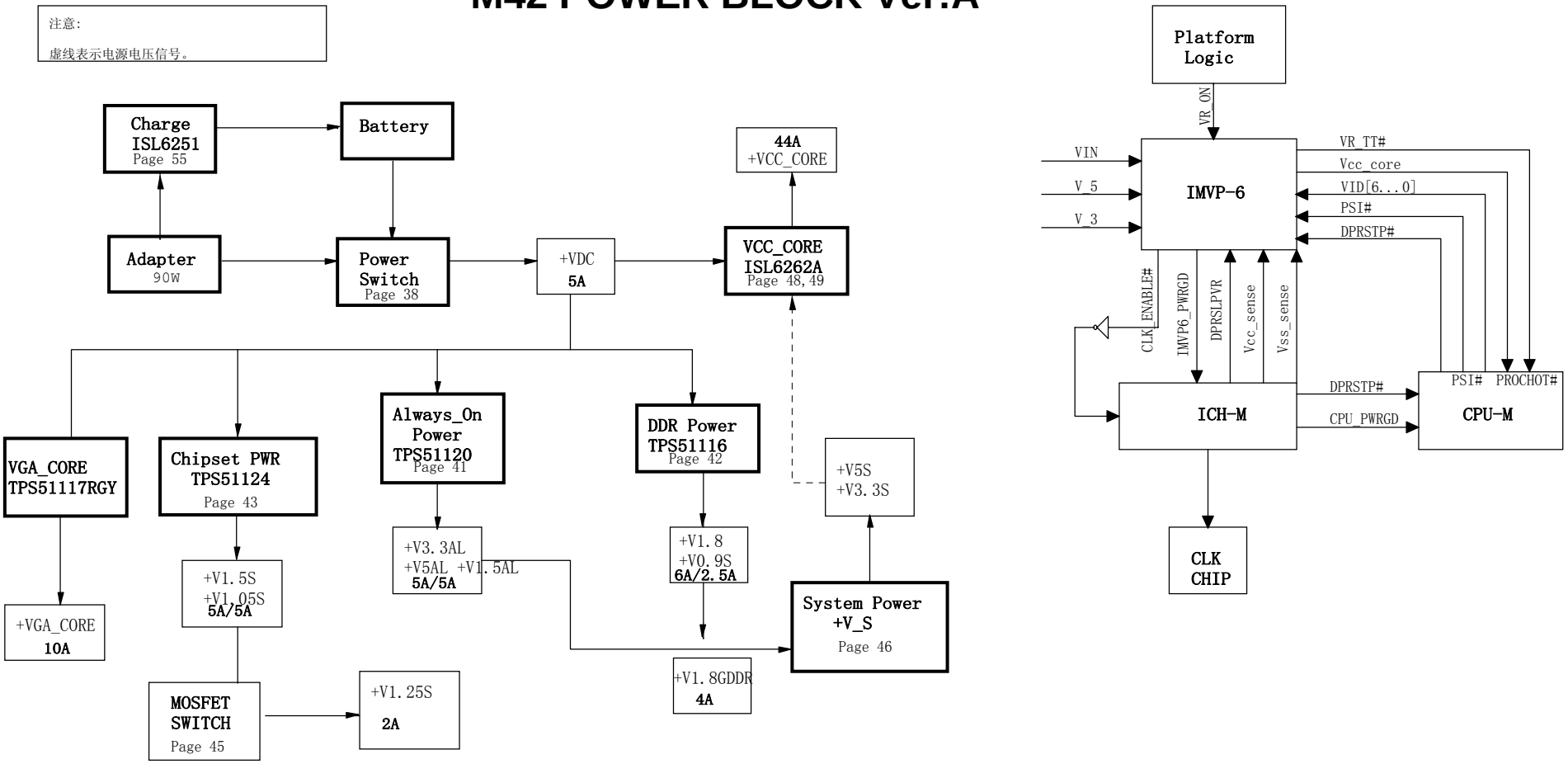
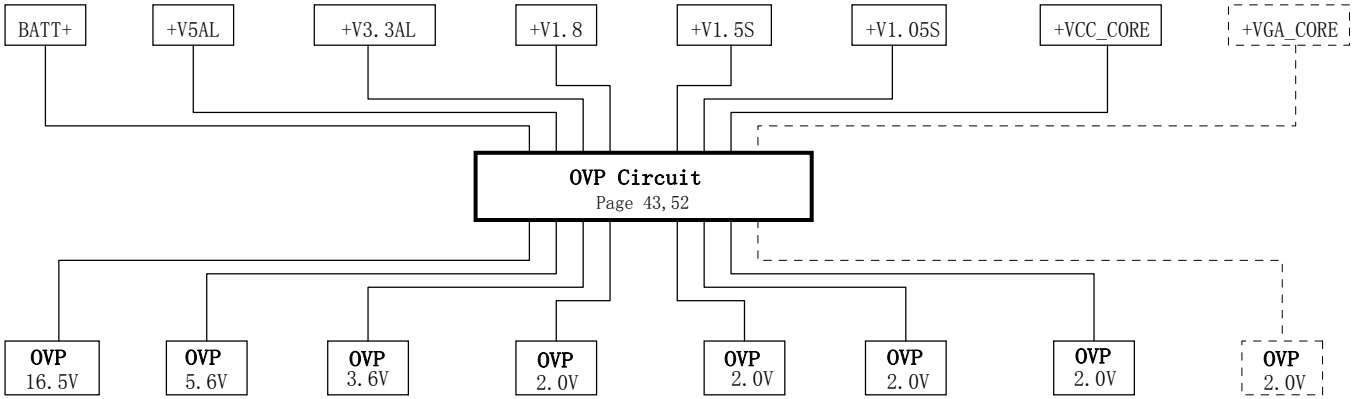
M42 POWER BLOCK Ver:A

注意:

虚线表示电源电压信号。





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Voltage Rails

+VDC	Primary DC system power supply(9V-19V)
+VCC_CORE	Core voltage for processor
+V1.5S	1.5V for CPU PLL
+V1.05S	1.05V for FSB VTT
+V0.9S	0.9V DDR2 Termination voltage
+V1.8	1.8V power rail for DDR2
+V3.3AL	3.3V always on power rail
+V3.3S	3.3V main power rail
+V5AL	5V for USB Device
+V5S	5V main power rail
+VGA_CORE	1.15V for GPU NB8M core voltage
+V1.25S	1.25V NB8M PCIE IO
+V1.8GDDR	1.8V GMEM

Board stack up description

PCB Layers	Trace Impedence:55ohm +/-15%(Default)
TOP	
GND	
IN1	
IN2	
VCC	
IN3	
GND	
Bottom	

USB Table

USB Port#	Function Description
0	Express Card
1	Finger
2	USB Port(on Main Board)
3	Mini PCIE Card(WLAN & ROBSON)
4	Mini PCIE Card(WLAN & ROBSON)
5	Bluetooth
6	USB CAMERA(On VGA Board)
7	USB Port(on I/O Board)
8	CARD Reader
9	USB Port(on I/O Board)

I2C SMB Address

Device	Address	Hex	Bus	Master
Clock Generator	1101 001x	D2	SMB_ICH_S	ICH9M
SO-DIMM0	1010 000x	A0	SMB_ICH_S	ICH9M
SO-DIMM1	1010 010x	A4	SMB_ICH_S	ICH9M
NEW CARD	Variable	Variable	SMB_ICH_S	ICH9M
PCIE Mini CARD	Variable	Variable	SMB_ICH_S	ICH9M
Smart Battery	0001 011x	16	I2C	W83L951ADG
CPU Thermal Sensor(ASC7525)	1001 100x	98	I2C	W83L951ADG

Power States/AC mode

Signal	SLP_S3#	SLP_S4#	SLP_S5#	+V*AL	+V*	+V*S	Clock
S0(Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(STM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(STD)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(SoftOff)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Wake up Events

LID switch from EC
Power switch from EC

ns: Component marked "ns" is not stuff

This is a lead free project,all component must be LF

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Schematic modify Item and history:

2007-10-26 Ver A initial release

2007-12-28 Ver B release

1 P6 CLK C112 ns change to 18pf stuff for EMC issue
2 P7 Host clk CLK_CPU_BCLK (#) add far end diff termination as DG and intel FAE advised
3 P7 Thermal sensor7525 change to 75393
4 P8 BRACKET1_Mylarchange to bi-side sticky malyer
5 P9 CPU bracket holesupport hold change to esd protection type
6 P22 IFPCD_IOVDD_FBIFPCD_IOVDD_FB add circuit for voltage leakage issue
7 P23 CameraAdd camera_on control circuit
8 P24 CRTC8 C9 C10 ns change to 22p stuff for vga emc issue
9 P25 HDMI EMCAdd common choke for HDMI emc issue
10 P27 spi bootR497 ns to stuff for boot from spi
11 P28 V1.5ALdelete for cost down
12 P32 EP_MYLAR1change as S42
13 P36 MIC1_JDMIC1_JD connect to sense B , reserved route to sense A
14 P36 Audio Jack esdD40 D41 D42 D43 change from bat54s to ESDPAD
15 P39 KBCADG change to DG
16 P39 CrystalDelete 32.768 crystal for no using
17 P39 KBC flashpull down reset# and test# for flash KBC
18 P39 "MCH_TSATN# EC_BKLT_PWM"swap these two pins for association with other cases

Cost Down list

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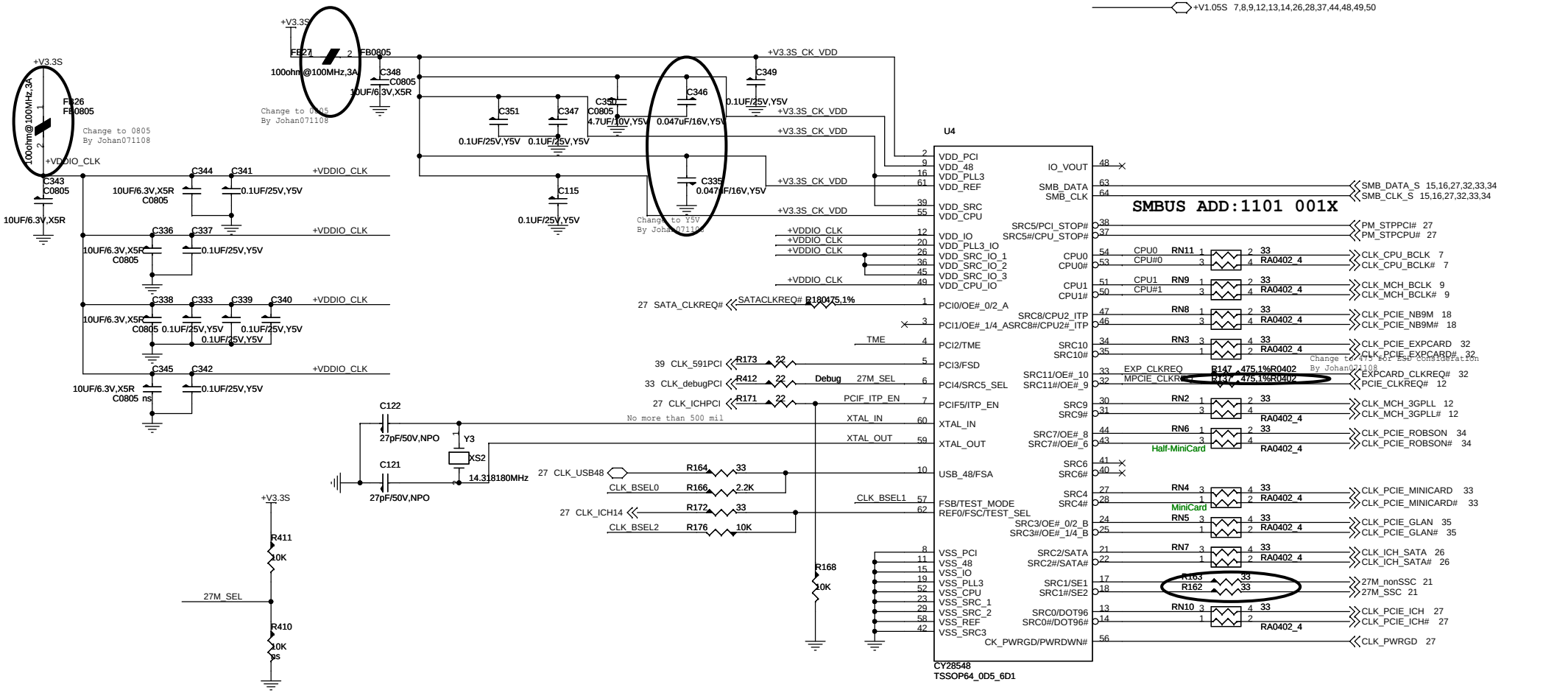
+V3.3S 7,12,14,15,16,18,21,22,23,25,26,27,28,29,32,33,34,35,36,37,38,39,44,45,47,48,49,50

+V1.05S 7,8,9,12,13,14,26,28,37,44,48,49,50



BUS FREQUENCE SELECT

FSC BSEL2	FSB BSEL1	FSA BSEL0	HOST Clock frequency
0	0	0	266
0	1	0	200
0	1	1	166

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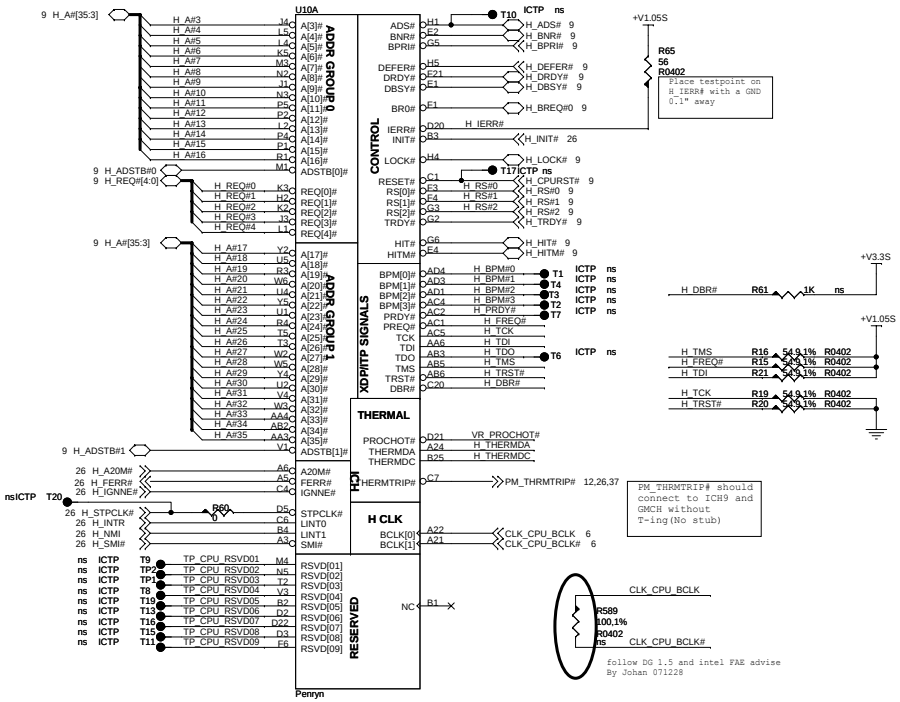

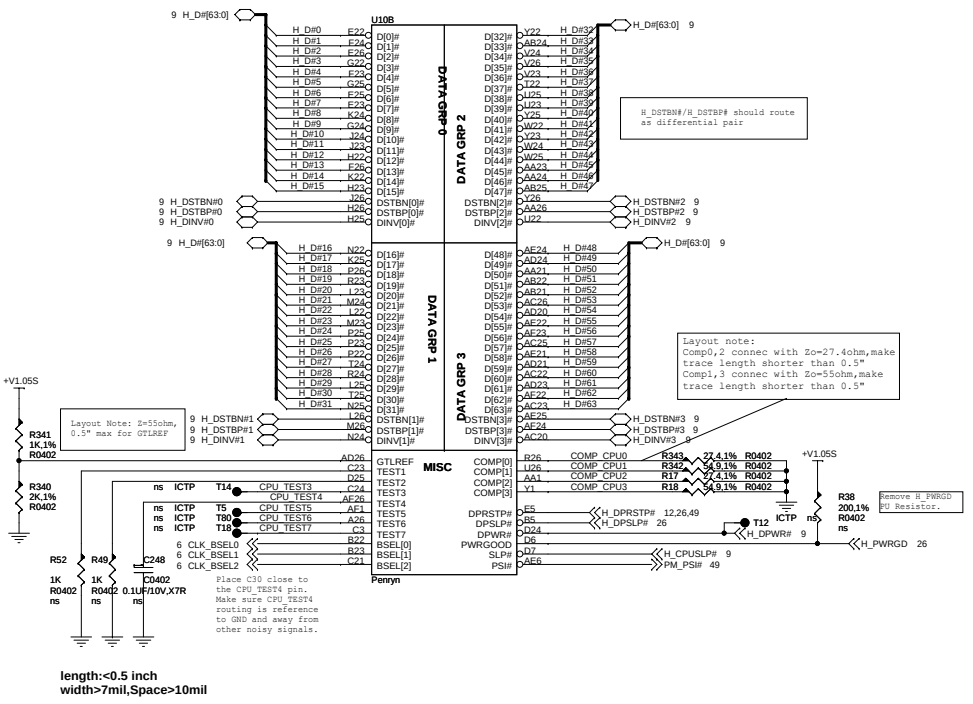

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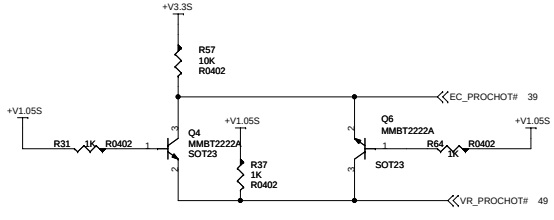
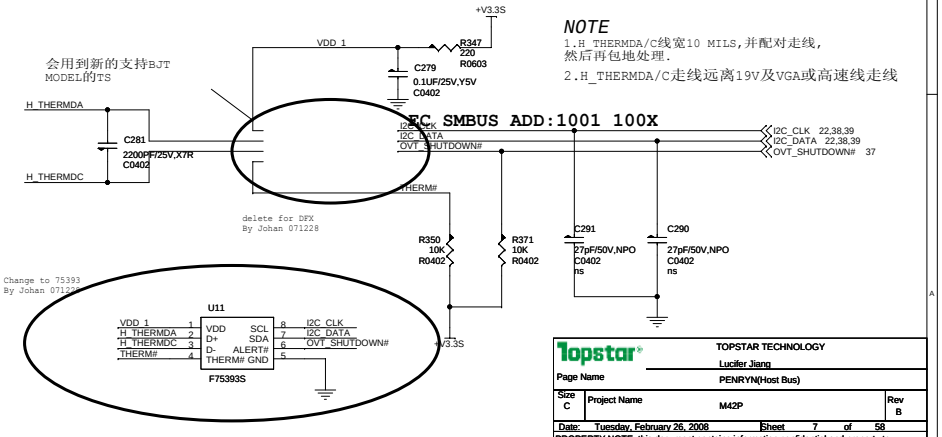
BI-DIRECTIONAL PROCESSOR HOT





NOTE

1.H_THERMDA/C线宽10 MILS,并配对走线,然后再包地处理.

2.H_THERMDA/C走线远离19V及VGA或高速线走线

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	PENRYN(Host Bus)
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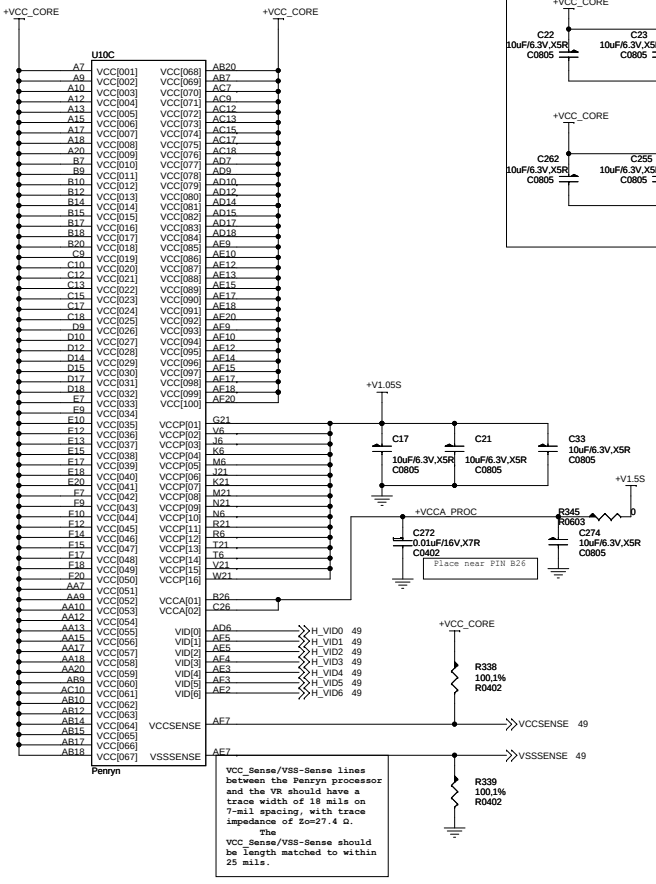

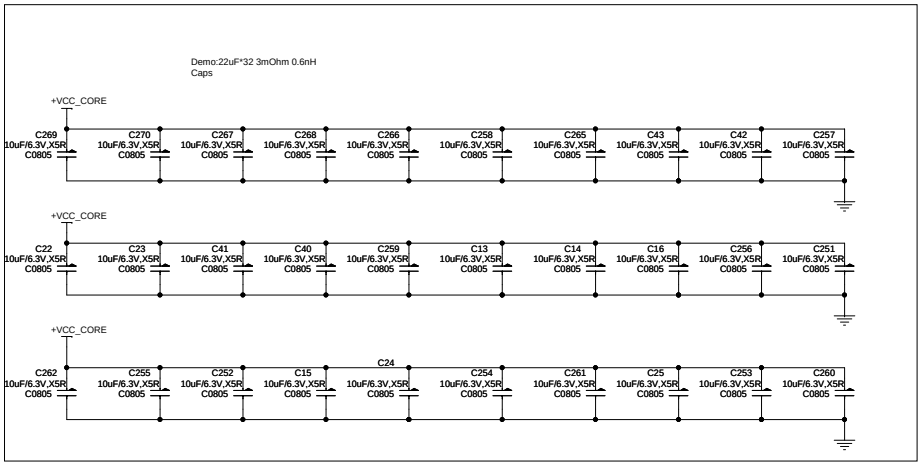

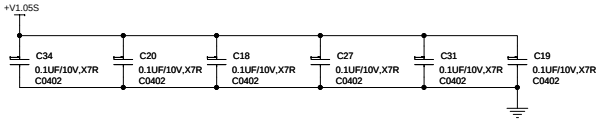

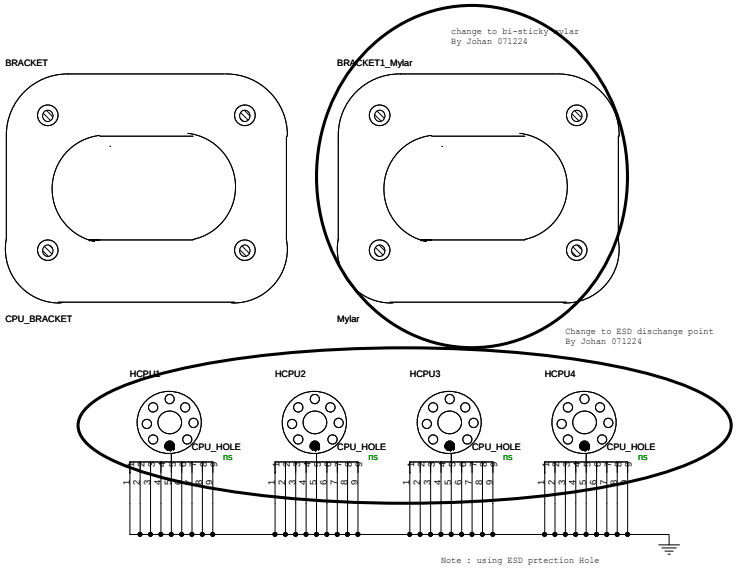

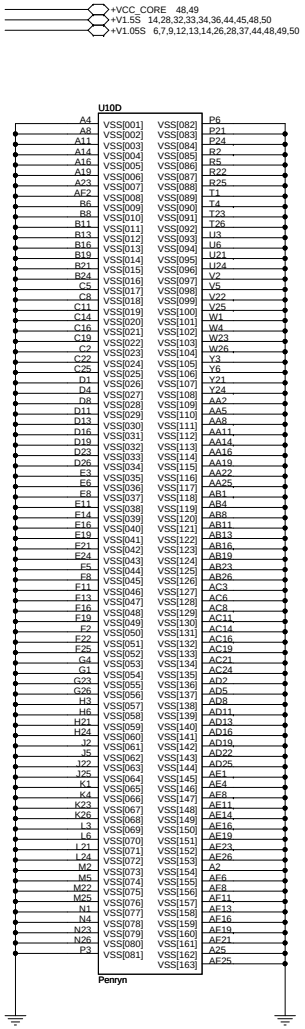

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Page Name	PENRYN(POWER&GND)
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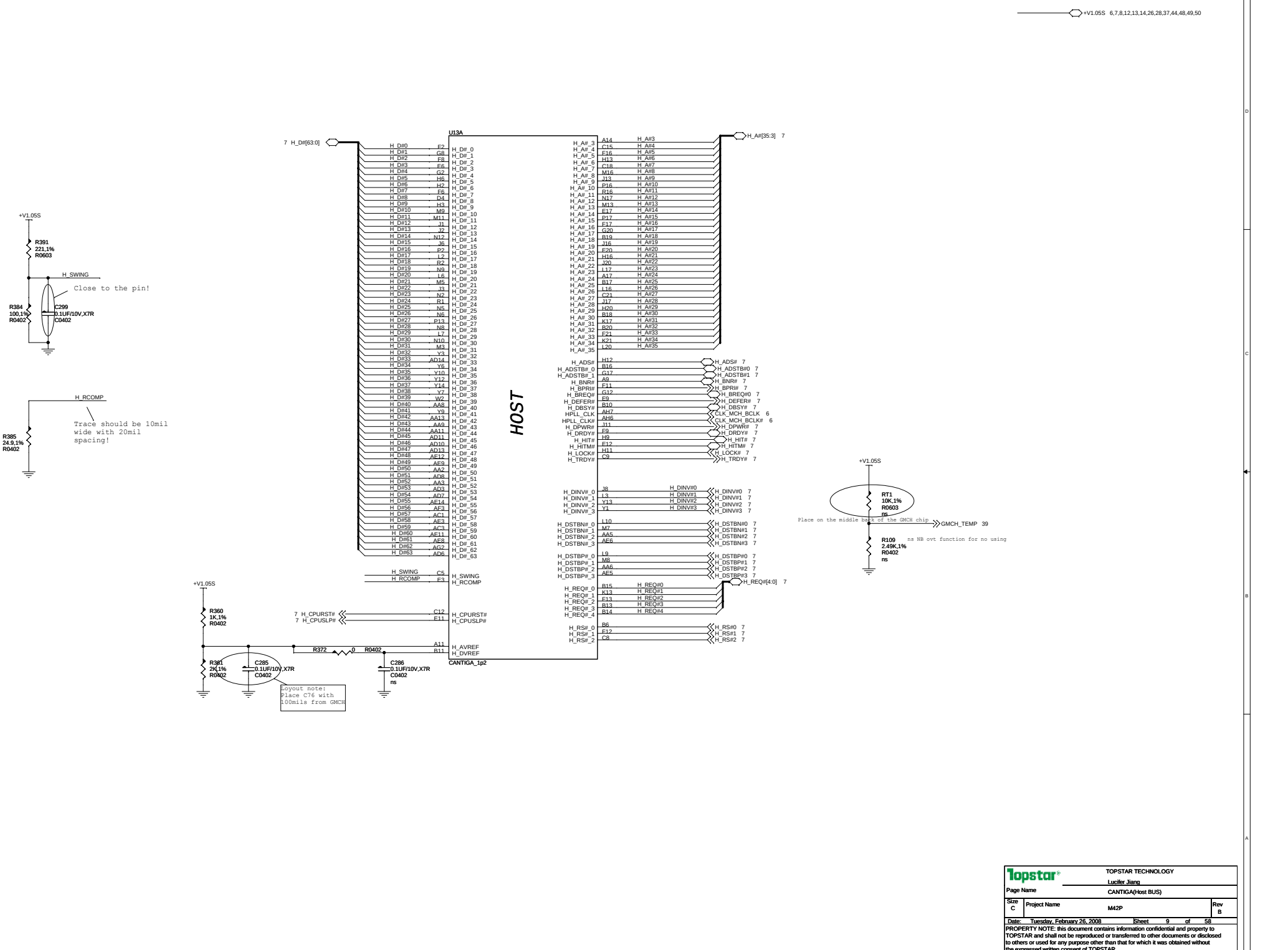

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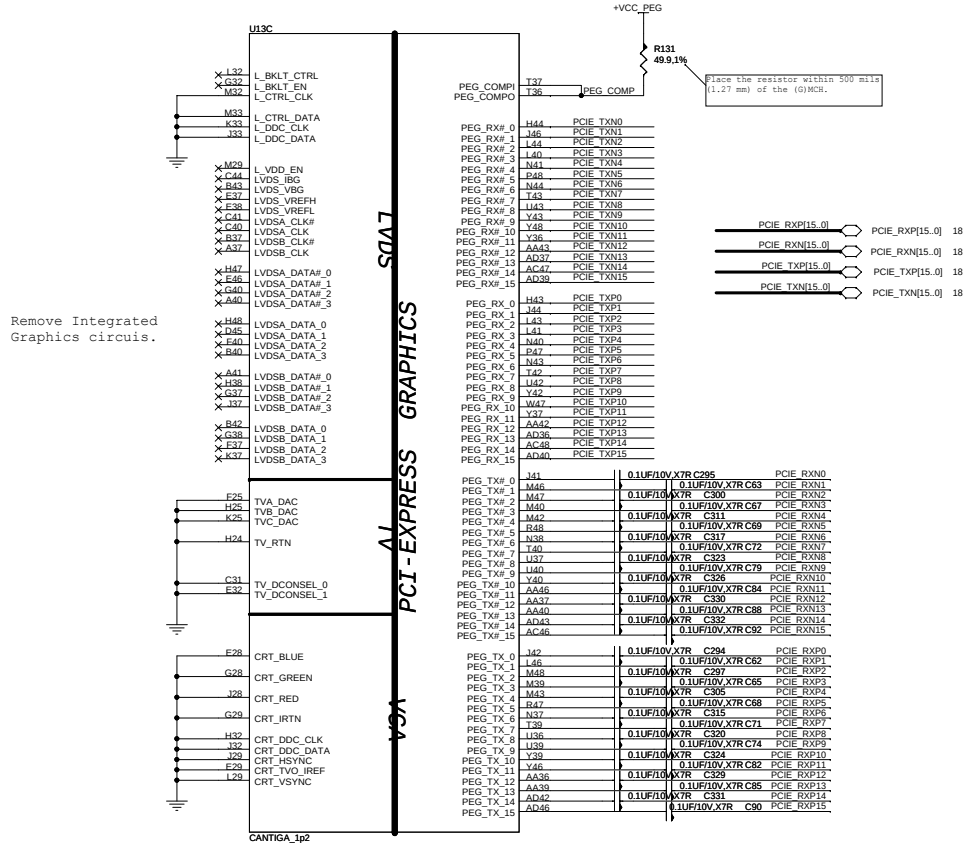

Remove Integrated Graphics circuis.

+VCC_PEG 14

topstar	TOPSTAR TECHNOLOGY		
Page Name	Lucifer Jiang		
	CANTIGA(GRAPHIC)		
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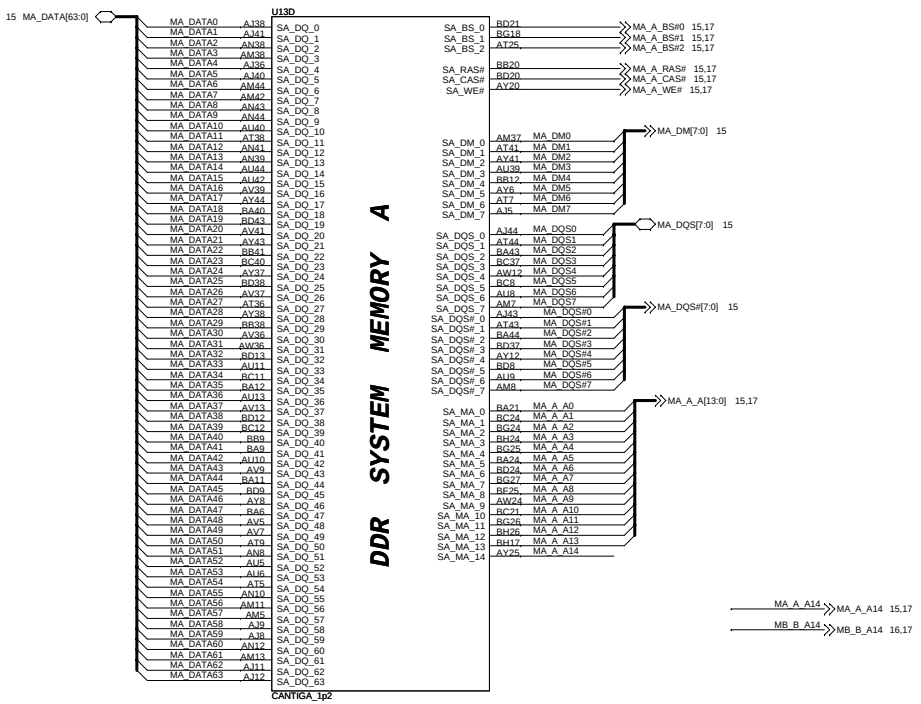

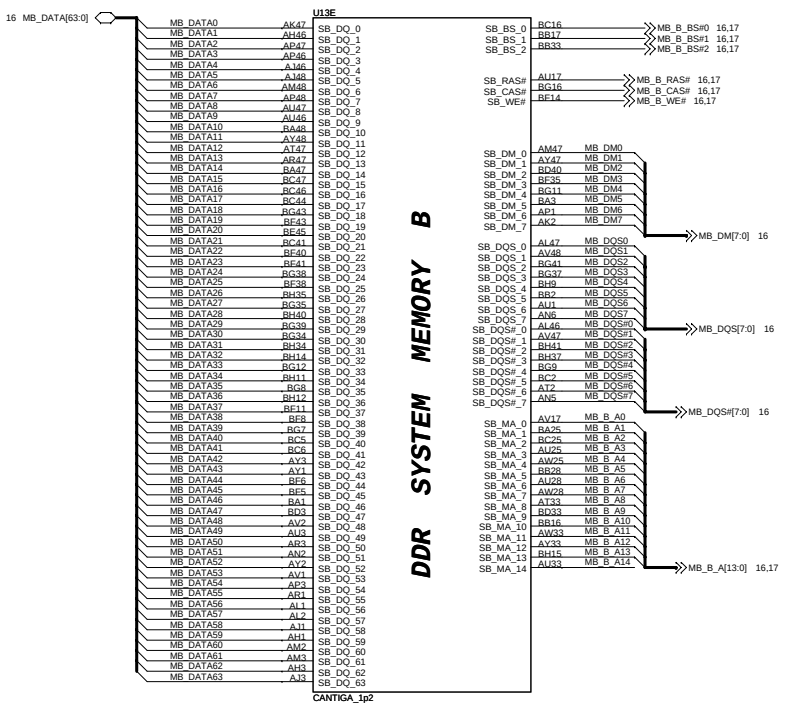

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Page Name	CANTIGA(DDRII)		
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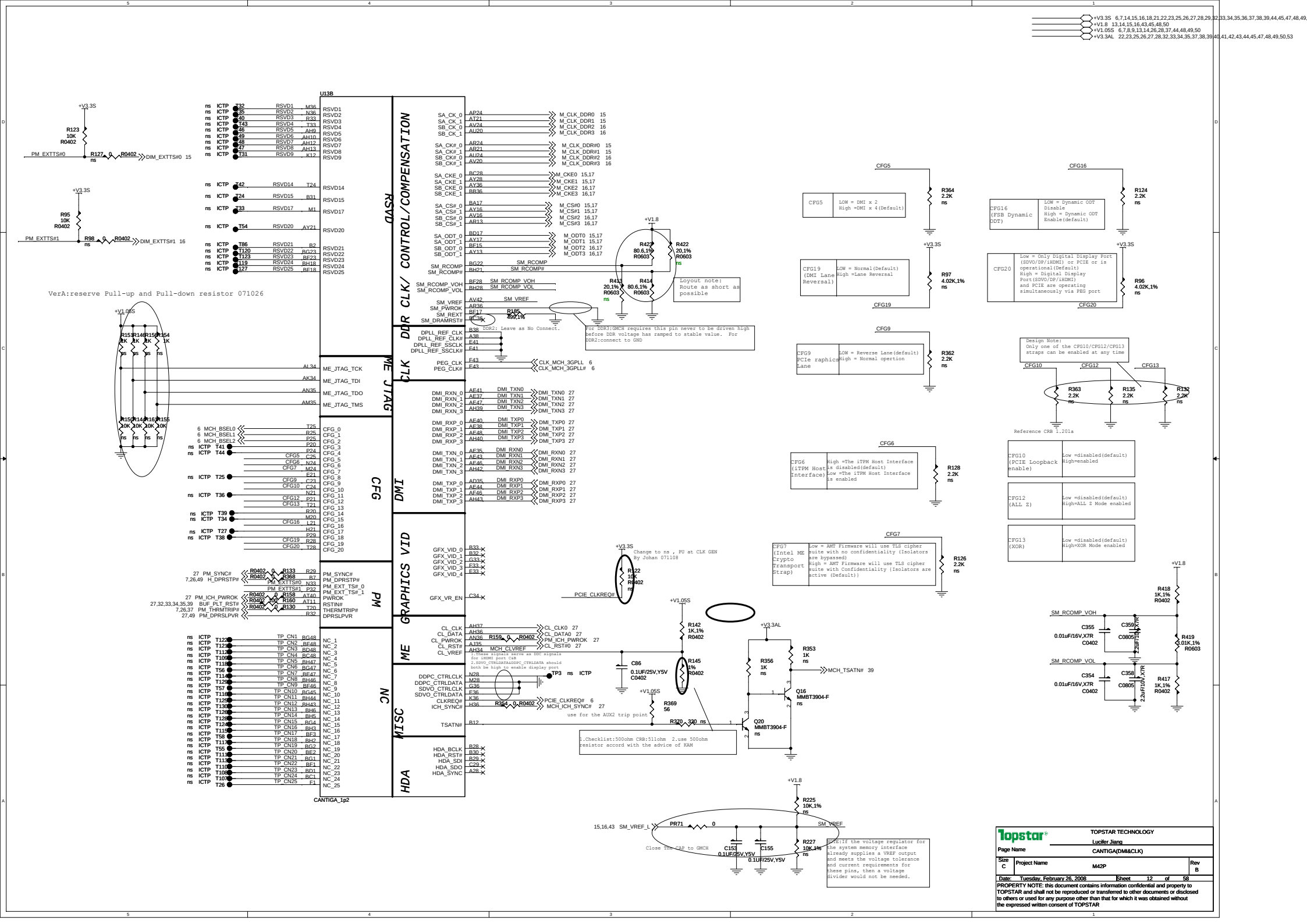
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+V1.8 13,14,15,16,43,45,48,50
+V1.05S 6,7,8,9,13,14,26,28,37,44,48,49,50
+V3.3AL 22,23,25,26,27,28,32,33,34,35,37,38,39,40,41,42,43,44,45,47,48,49,50,53
U13B
RSVD
DDR CLK/ CONTROL/COMPENSATION
ME JTAG
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
HDA
CANTIGA_1p2
VerA:reserve Pull-up and Pull-down resistor 071026
Design Note:
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time
Reference CRB 1.201a
Change to ns , PU at CLK GEN By Johan 071108
1.Checklist:500ohm CRB:511ohm 2.use 500ohm resistor accord with the advice of KAM
Close the CAP to GMCH
Note:If the voltage regulator for the system memory interface already supplies a VREF output and meets the voltage tolerance and current requirements for these pins, then a voltage divider would not be needed.
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Page Name CANTIGA(DMI&CLK)
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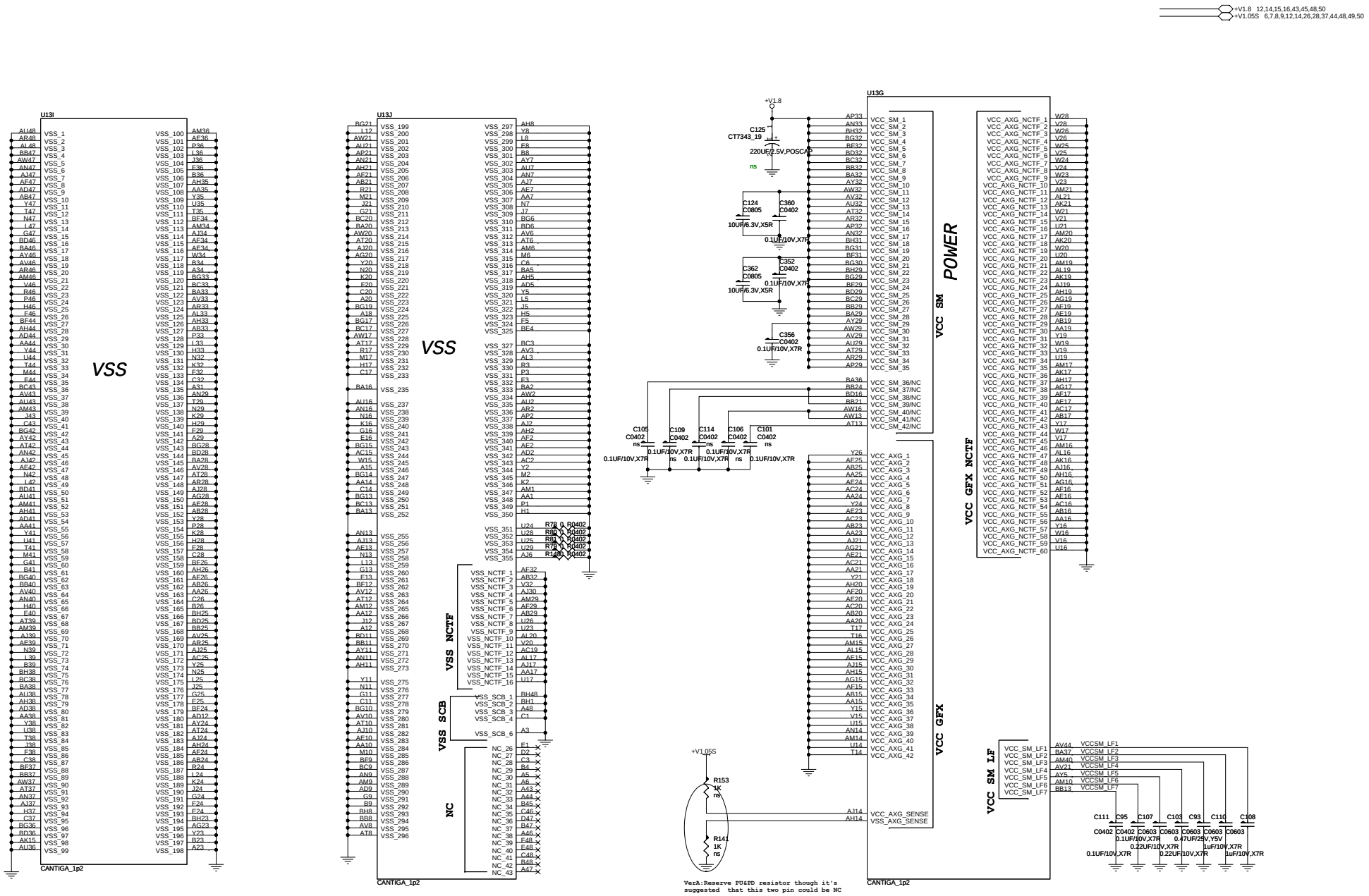

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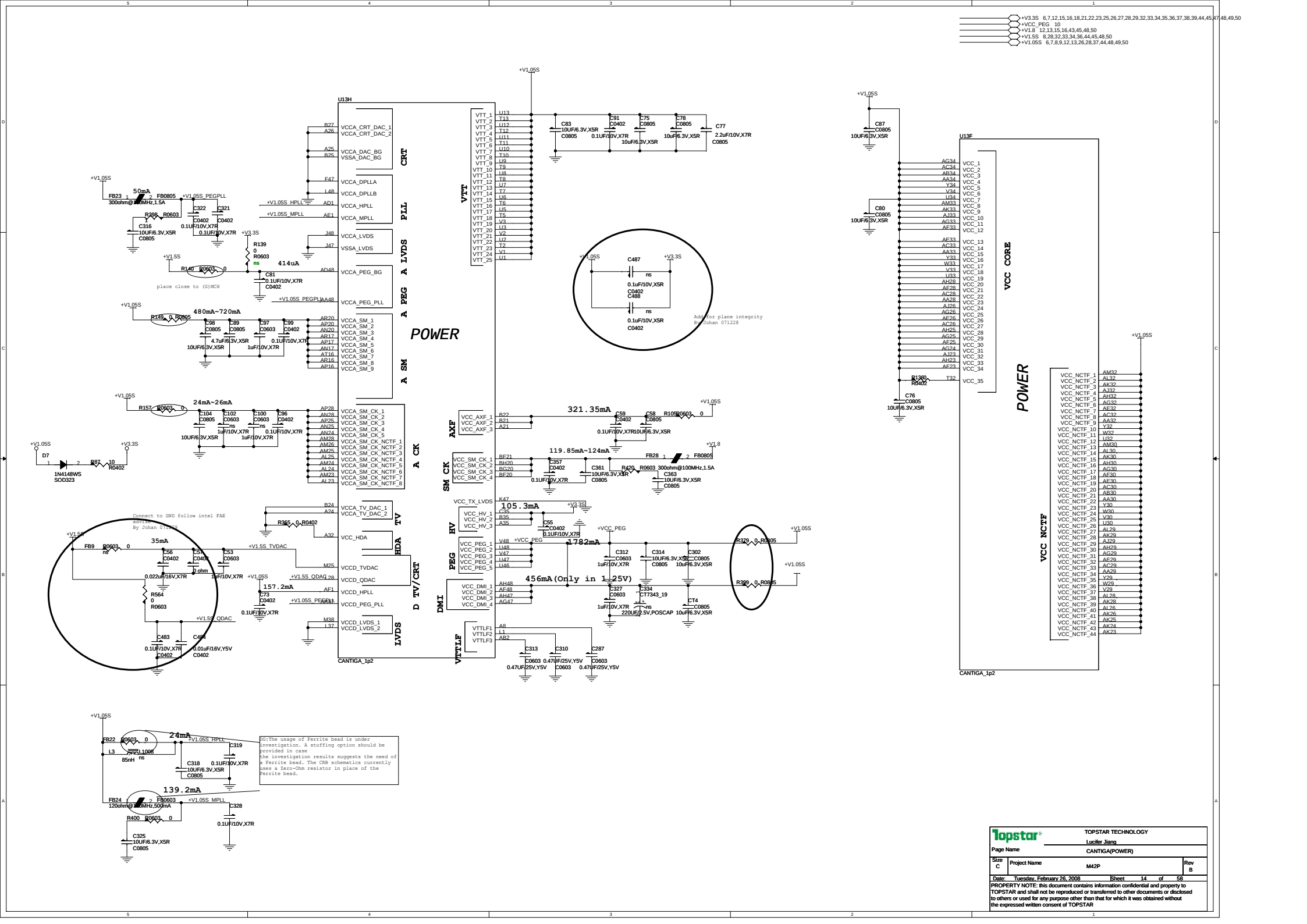
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+VCC_PEG 10
+V1.8 12,13,15,16,43,45,48,50
+V1.5S 8,28,32,33,34,36,44,45,48,50
+V1.05S 6,7,8,9,12,13,26,28,37,44,48,49,50
U13H
CRT
PLL
LVDS
POWER
SM
PEG
AXF
SM CK
HV
PEG
DMI
TV
HDA
LVDS
TV/CRT
VTT
VTTLF
CANTIGA_1p2
U13F
VCC CORE
POWER
VCC NCTF
CANTIGA_1p2
50mA
480mA~720mA
414uA
24mA~26mA
321.35mA
119.85mA~124mA
105.3mA
1782mA
456mA(Only in 1.25V)
35mA
157.2mA
24mA
139.2mA
place close to (G)MCH
Add for plane integrity By Johan 071228
Connect to GND follow intel FAE advise By Johan 071228
DG:The usage of Ferrite bead is under investigation. A stuffing option should be provided in case the investigation results suggests the need of a Ferrite bead. The CRB schematics currently uses a Zero-Ohm resistor in place of the Ferrite bead.
1N4148WS SOD323
topstar
TOPSTAR TECHNOLOGY
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+V3.3S 6,7,12,14,16,18,21,22,23,25,26,27,28,29,32,33,34,35,36,37,38,39,44,45,47,48,49,50
+V1.8 12,13,14,16,43,45,48,50

DIM1
DDR2_SODIMM200
DDR200RVS_5D2

SO-DIMM 0

DDRII

1010 000x

Note:
SO-DIMM0 SPD Address is 0xA0
SO-DIMM0 TS Address is 0x30

close to DDR pin

1, A minimum of 9 high frequency capacitors are recommended to be placed near each SO-DIMM of DDR2.
2, 2.2uF*5 per DIMM,0.1uF*4 per DIMM,330uF*1 per DIMM

Layout note:电容靠近DDR slot VDD PIN

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Page Name	DDR2 SODIMM0
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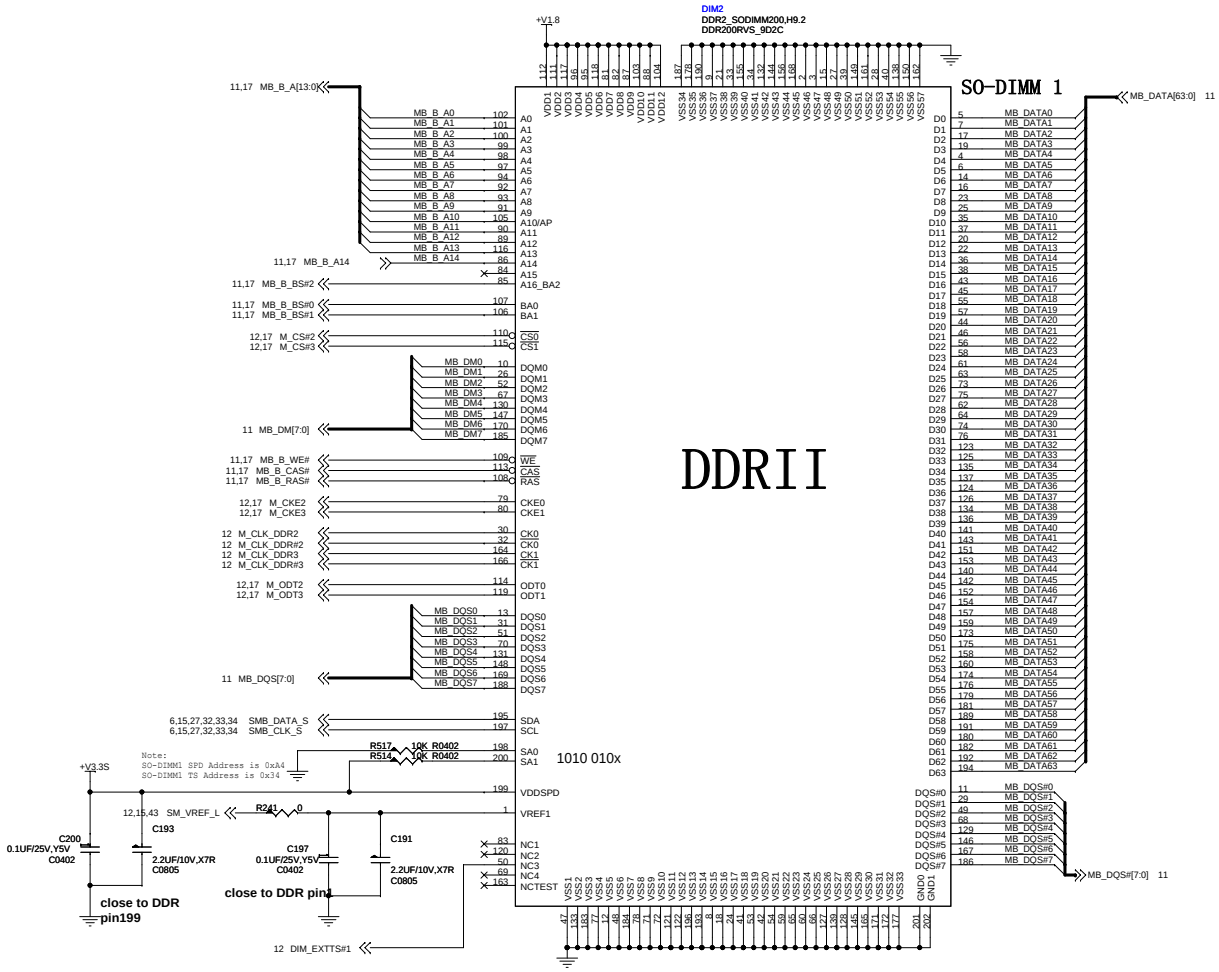
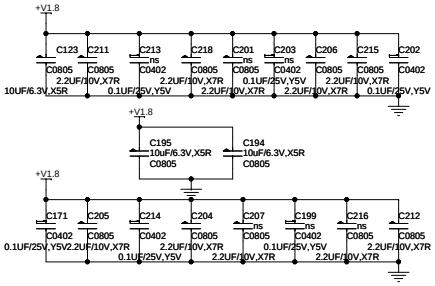
+V3.3S 6,7,12,14,15,18,21,22,23,25,26,27,28,29,32,33,34,35,36,37,38,39,44,45,47,48,49,50
+V1.8 12,13,14,15,43,45,48,50





Layout note:电容靠近DDR slot VDD PIN

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Page Name	DDR2 SODIMM1	
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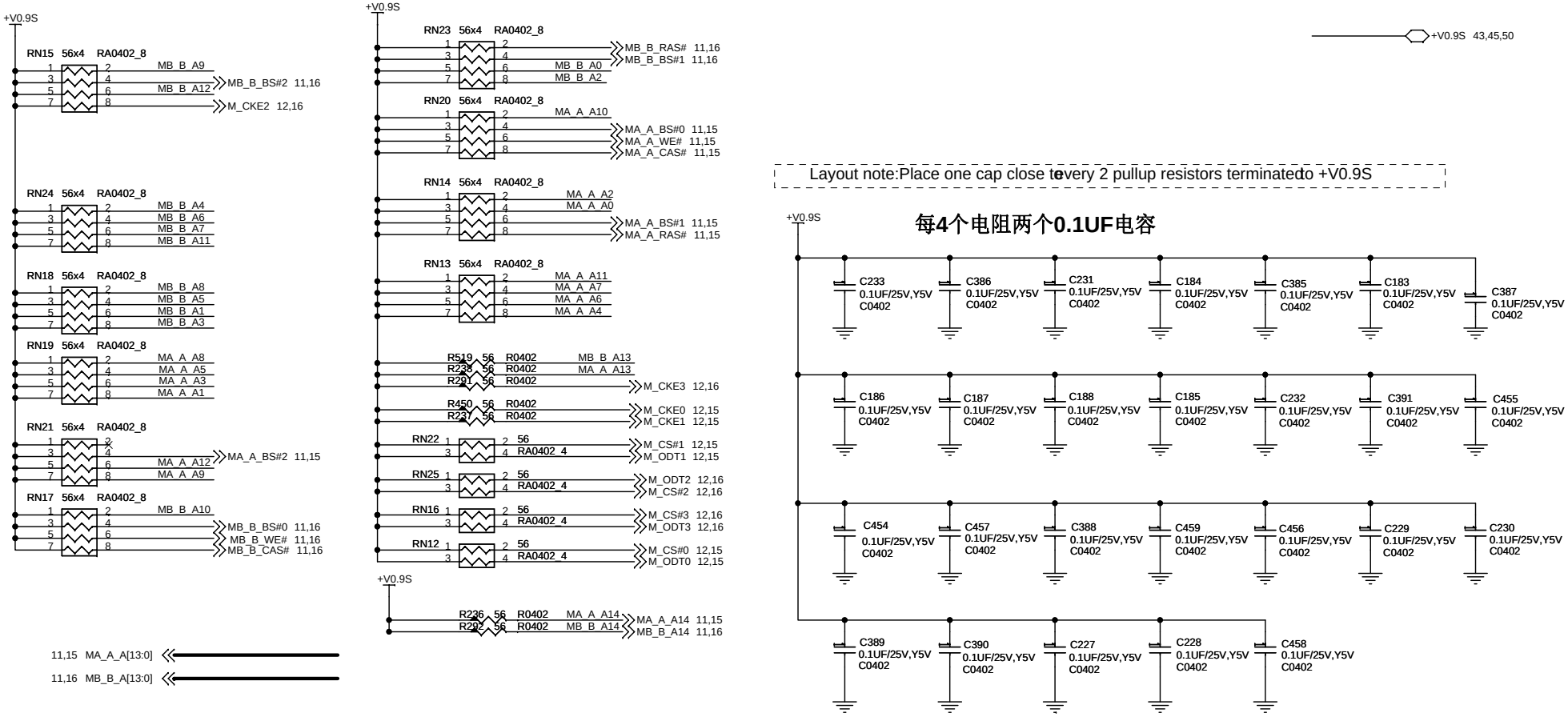

+V0.9S 43,45,50

Layout note:Place one cap close to every 2 pullup resistors terminated to +V0.9S

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Page Name	DDR2 TERM and Decoupling	
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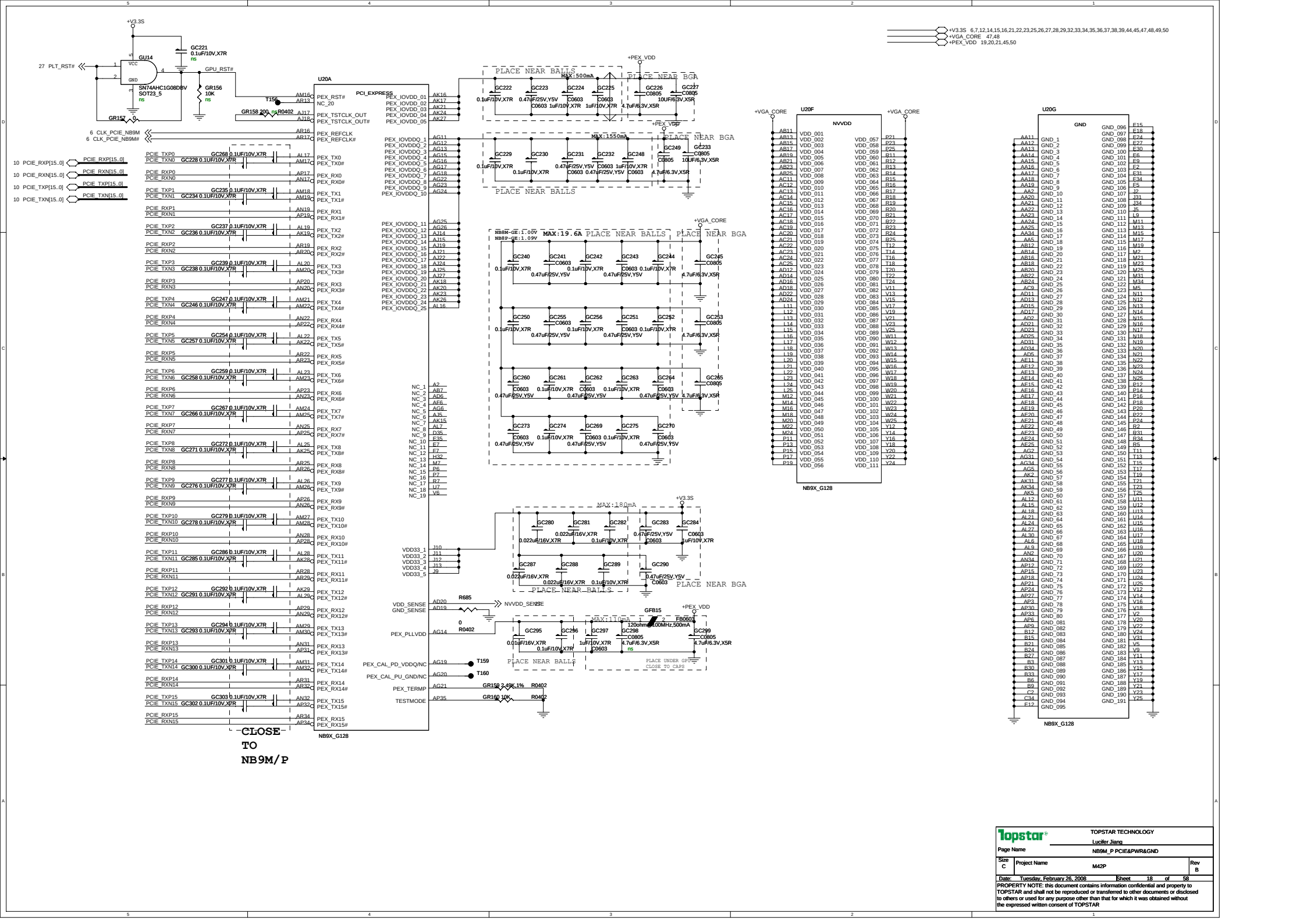

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Page Name	NB9M_P PCIE&PWR&GND		
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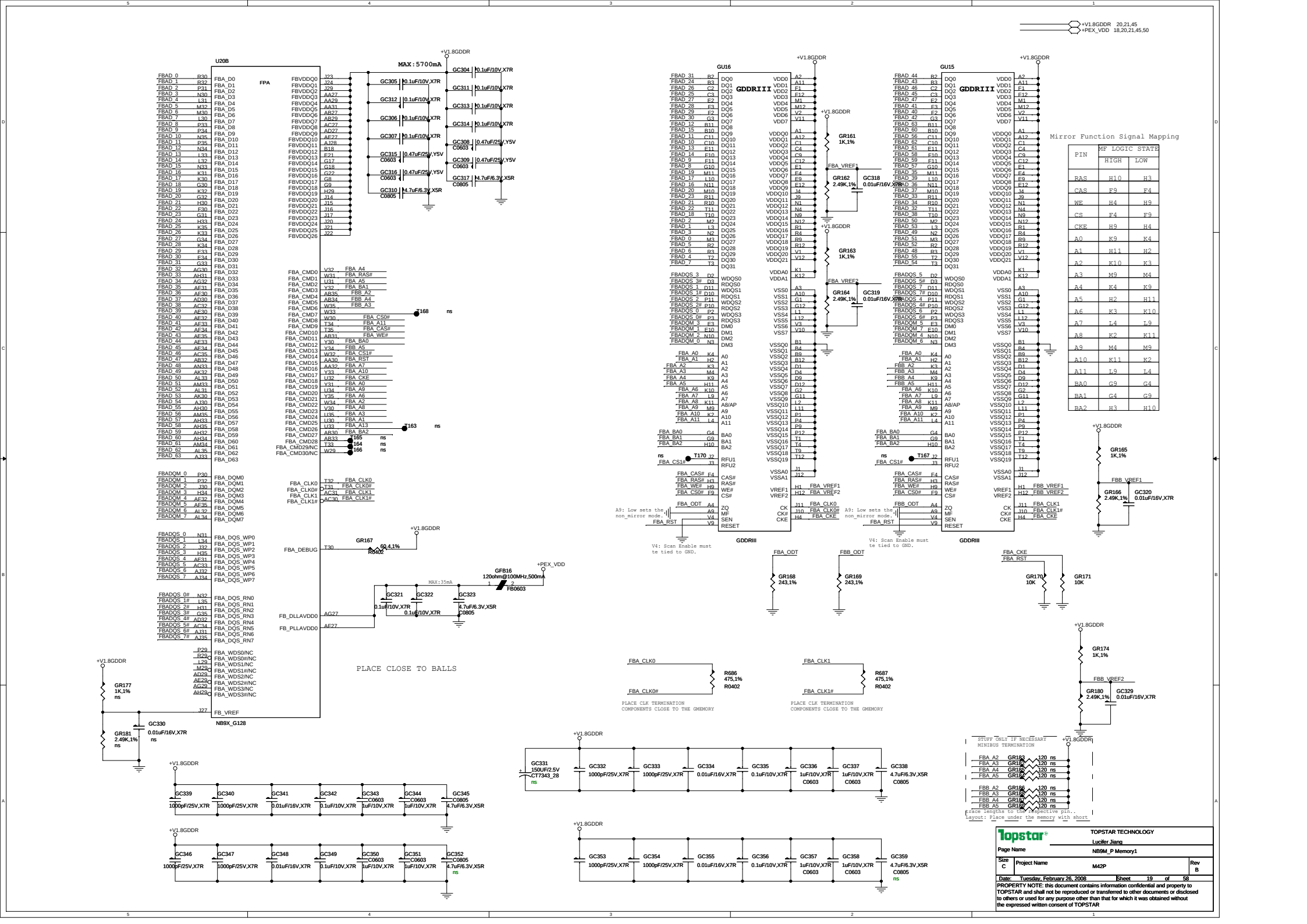
+V1.8GDDR 20,21,45
+PEX_VDD 18,20,21,45,50
U20B
NB9X_G128
FPA
MAX:5700mA
GC304 0.1uF/10V_X7R
GC305 0.1uF/10V_X7R
GC311 0.1uF/10V_X7R
GC312 0.1uF/10V_X7R
GC313 0.1uF/10V_X7R
GC306 0.1uF/10V_X7R
GC314 0.1uF/10V_X7R
GC307 0.1uF/10V_X7R
GC308 0.47uF/25V_Y5V C0603
GC315 0.47uF/25V_Y5V C0603
GC309 0.47uF/25V_Y5V C0603
GC316 0.47uF/25V_Y5V C0603
GC310 4.7uF/6.3V_X5R C0805
GC317 4.7uF/6.3V_X5R C0805
T168 ns
T163 ns
T170 ns
T167 ns
GR167 60.4,1% R0402
GFB16 120ohm@100MHz,500mA FB0603
GC321 0.1uF/10V_X7R
GC322 0.1uF/10V_X7R
GC323 4.7uF/6.3V_X5R C0805
PLACE CLOSE TO BALLS
GR177 1K,1% ns
GC330 0.01uF/16V,X7R ns
GR181 2.49K,1% ns
GC339 1000pF/25V,X7R
GC340 1000pF/25V,X7R
GC341 0.01uF/16V,X7R
GC342 0.1uF/10V,X7R
GC343 C0603 1uF/10V,X7R
GC344 C0603 1uF/10V,X7R
GC345 C0805 4.7uF/6.3V,X5R
GC346 1000pF/25V,X7R
GC347 1000pF/25V,X7R
GC348 0.01uF/16V,X7R
GC349 0.1uF/10V,X7R
GC350 C0603 1uF/10V,X7R
GC351 C0603 1uF/10V,X7R
GC352 C0805 4.7uF/6.3V,X5R ns
GU16
GU15
GDDRIII
GR161 1K,1%
GR162 2.49K,1%
GC318 0.01uF/16V,X7R
GR163 1K,1%
GR164 2.49K,1%
GC319 0.01uF/16V,X7R
FBA_VREF1
FBA_VREF2
A9: Low sets the non_mirror mode.
V4: Scan Enable must te tied to GND.
GR165 1K,1%
GR166 2.49K,1%
GC320 0.01uF/16V,X7R
FBB_VREF1
FBB_VREF2
GR168 243,1%
GR169 243,1%
GR170 10K
GR171 10K
FBA_ODT
FBB_ODT
FBA_CKE
FBA_RST
GR174 1K,1%
GR180 2.49K,1%
GC329 0.01uF/16V,X7R
R686 475,1% R0402
R687 475,1% R0402
FBA_CLK0
FBA_CLK0#
FBA_CLK1
FBA_CLK1#
PLACE CLK TERMINATION COMPONENTS CLOSE TO THE GMEMORY
GC331 150UF/2.5V CT7343_28 ns
GC332 1000pF/25V,X7R
GC333 1000pF/25V,X7R
GC334 0.01uF/16V,X7R
GC335 0.1uF/10V,X7R
GC336 1uF/10V,X7R C0603
GC337 1uF/10V,X7R C0603
GC338 4.7uF/6.3V,X5R C0805
GC353 1000pF/25V,X7R
GC354 1000pF/25V,X7R
GC355 0.01uF/16V,X7R
GC356 0.1uF/10V,X7R
GC357 1uF/10V,X7R C0603
GC358 1uF/10V,X7R C0603
GC359 4.7uF/6.3V,X5R C0805 ns
STUFF ONLY IF NECESSARY MINIBUS TERMINATION
Trace lengths to the respective pin..
Layout: Place under the memory with short
Mirror Function Signal Mapping
PIN | MF LOGIC STATE HIGH | LOW
RAS H10 H3
CAS F9 F4
WE H4 H9
CS F4 F9
CKE H9 H4
A0 K9 K4
A1 H11 H2
A2 K10 K3
A3 M9 M4
A4 K4 K9
A5 H2 H11
A6 K3 K10
A7 L4 L9
A8 K2 K11
A9 M4 M9
A10 K11 K2
A11 L9 L4
BA0 G9 G4
BA1 G4 G9
BA2 H3 H10
TOPSTAR TECHNOLOGY
Lucifer Jiang
Page Name NB9M_P Memory1
Size C
Project Name M42P
Rev B
Date: Tuesday, February 26, 2008 Sheet 19 of 58
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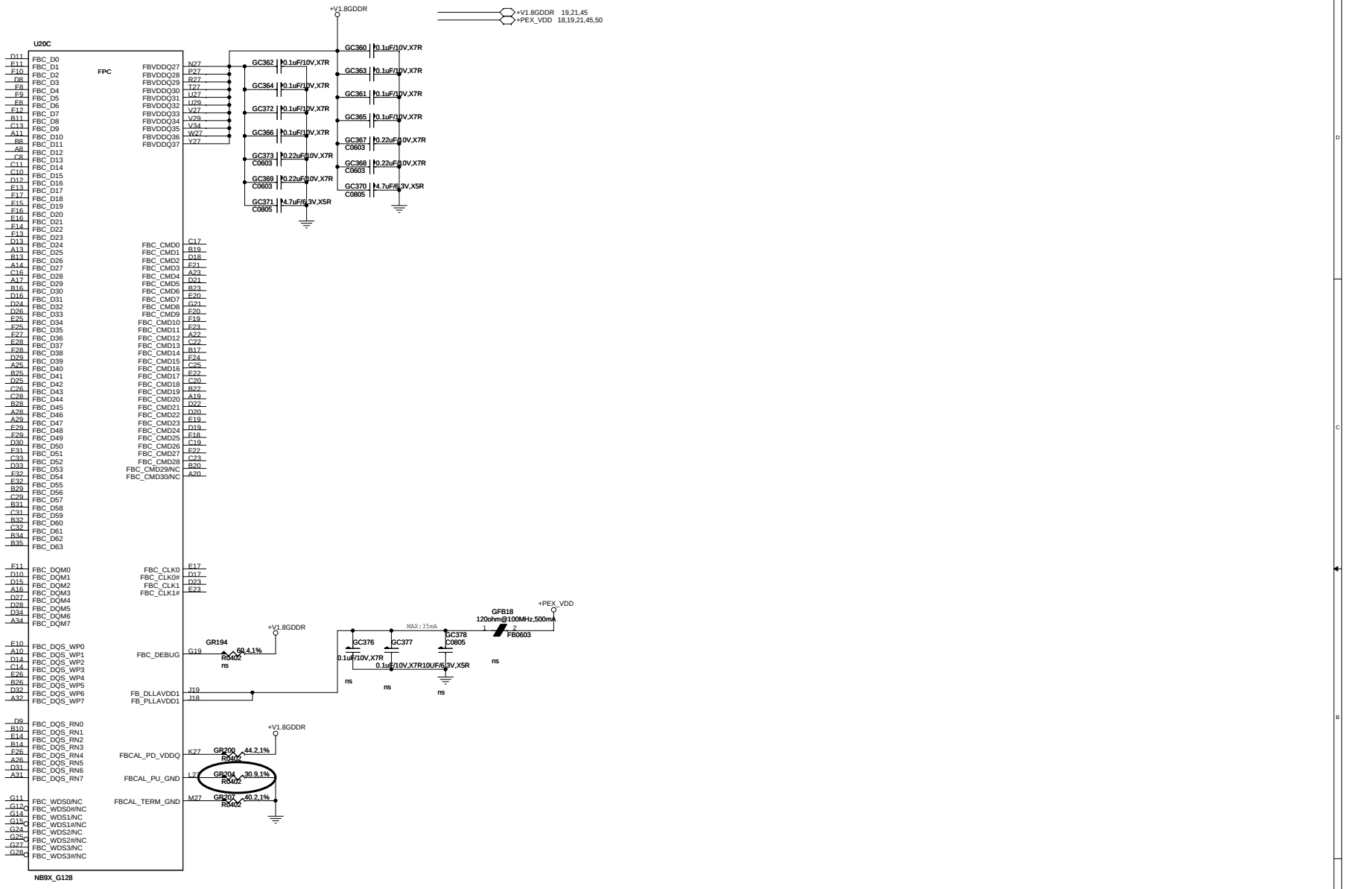

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	Lucifer Jiang		
Page Name	NB9M_P Memory2		
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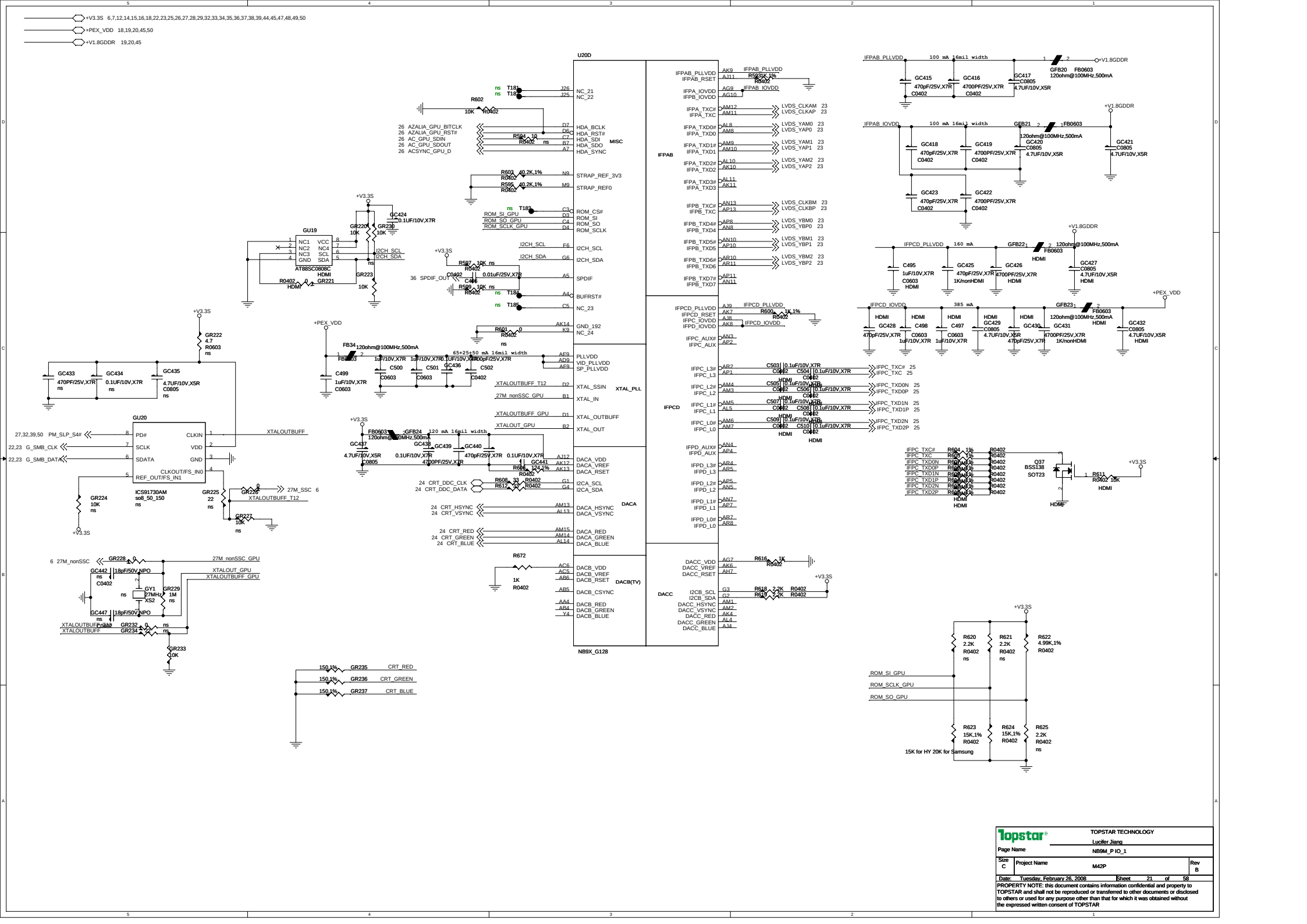

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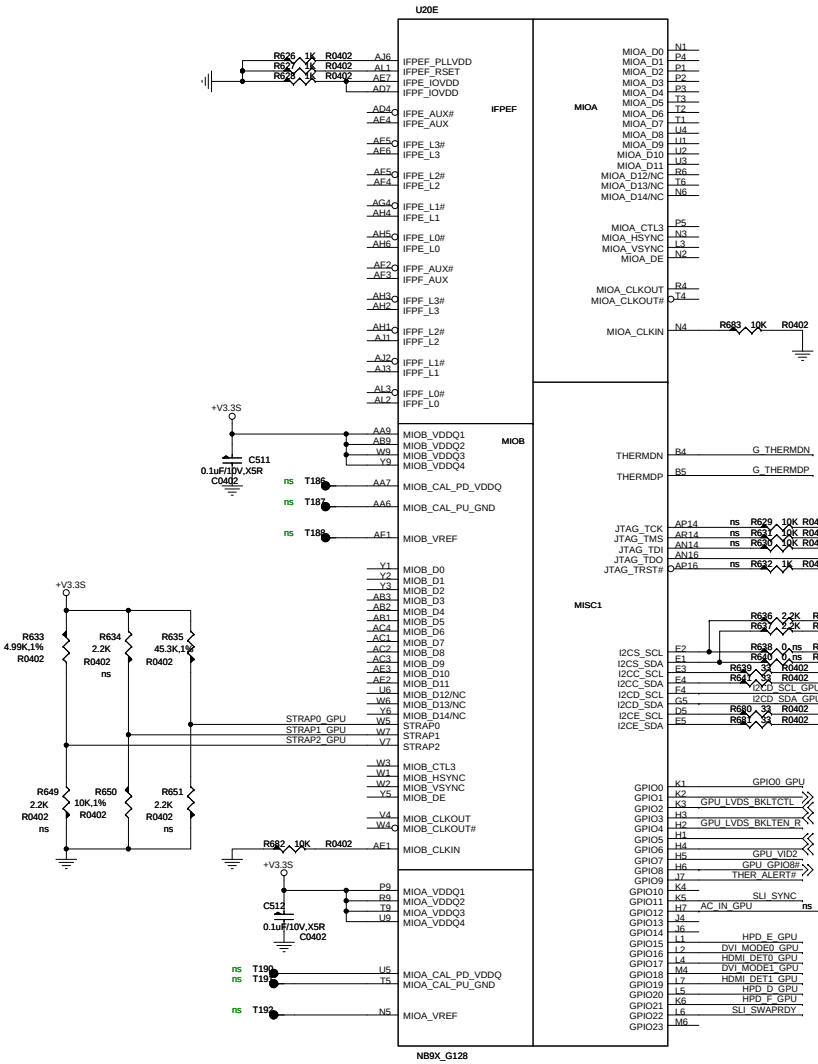
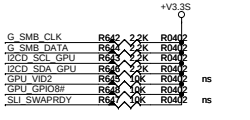
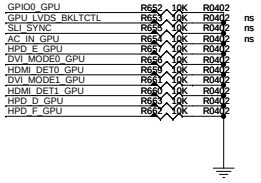
+V3.3S 6,7,12,14,15,16,18,21,23,25,26,27,28,29,32,33,34,35,36,37,38,39,44,45,47,48,49,50

+V3.3AL 12,23,25,26,27,28,32,33,34,35,37,38,39,40,41,42,43,44,45,47,48,49,50,53



ITEM	FUNC	Action
GPIO0	GPIO	no using , PD 2.2K
GPIO1	HPD-C	connect to HDMI conn with level shifter
GPIO2	Panel backlight brightness	reserved associated with EC PWM , then connect to LVDS conn , reserved PD 2.2K
GPIO3	Panel Power enable , active high	connect LCDVDD_ON
GPIO4	Panel backlight On , active high	connect LCDVDD backlight on
GPIO5	GPU vid0	Reserved routing to GPU power controller
GPIO6	GPU vid1	Reserved routing to GPU power controller
GPIO7	GPU vid2	no using , reserved 2.2K PU V3.3S
GPIO8	Thermal trip of GPU , active low	Connect to Hardware shut down circuit , parallel with CPU thermaltrip , 2.2K PU V3.3S
GPIO9	Thermal alert input	connect to thermal sensor IC alert with 2.2K PU V3.3S
GPIO10	Memory Vref switch	no using , follow CRB
GPIO11	SLI_SYNC , host GPU output , slave input	PD 10K
GPIO12	AC detect	no using , 2.2K PU V3.3S
GPIO13	Dynamic NVVDD control 0	no using , NC
GPIO14	Dynamic NVVDD control 0	no using , NC
GPIO15	HPD-E	no using , PD 2.2K
GPIO16	DVI-Mode0	no using , PD 2.2K
GPIO17	HDMI-detect0	no using , PD 2.2K
GPIO18	DVI-Mode1	no using , PD 2.2K
GPIO19	HDMI-detect1	no using , PD 2.2K
GPIO20	HPD-D	no using , PD 2.2K
GPIO21	HPD-F	no using , PD 2.2K
GPIO22	SLI_swapy	10K PU V3.3S
GPIO23	GPIO	no using , NC

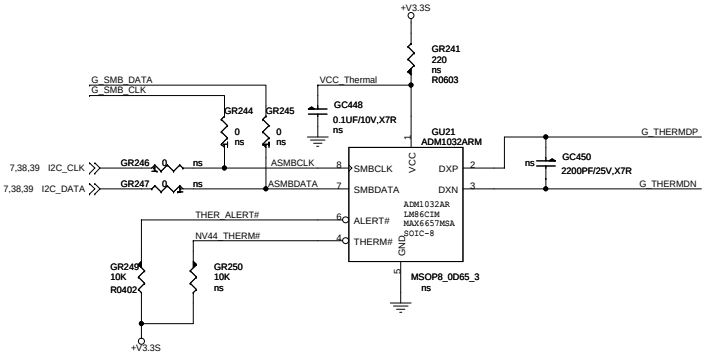


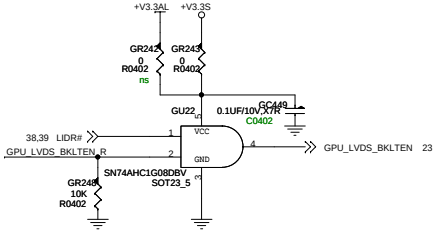


strap pin	Power rail	bit 3	bit 2	bit 1	bit 0	Action
		XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]	
ROM_SO	Vdd33	1	0	0	0	PU 5K
		PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100	
ROM_SCLK	Vdd33	0	0	1	0	PD 15K
ROM_SI	Vdd33	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	TBD
		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	
STRAP2	MIOB_VDDQ	1	0	0	0	PU 5K
		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	
STRAP1	MIOB_VDDQ	0	0	0	1	PD 10K
		USER[3]	USER[2]	USER[1]	USER[0]	
STRAP0	MIOB_VDDQ	1	1	1	1	PU 45K

Res value	PU VDD	PD GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

NOTE:
1, XCLK_277 set 1 , using 27MHz clock
2, TVMODE[2:0] set 000 , using NTSC M
3, PCI_DEVID[4:0] NB9M-GE set 0x06E8 NB9P-GE(65nm) set 0x0648 , using last five bit , PCI_DEVID[4:0] set 01000 for both
4, USER[3:0] set 1111 , using EDID method to detect panel
5, 3GIO_PADCFG[3:0] set 0001 , using NOTEBOOK configuration
6, RAMCFG[3:0] need follow latest PUN
7, PEX_PLL_EN_TERM100 set 0 , using PEX PLL termination disable configuration
8, SLOT_CLK_CFG set 1 , GPU MCH using the same clk chip
9, SUB_VENDOR set 0 , no VIDEO BIOS ROM





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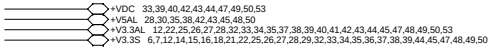
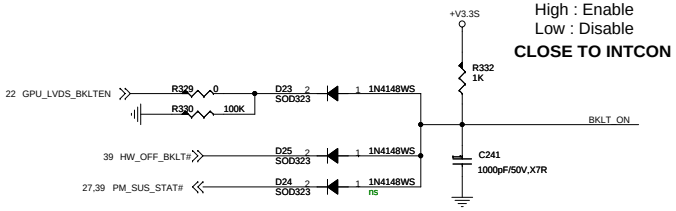
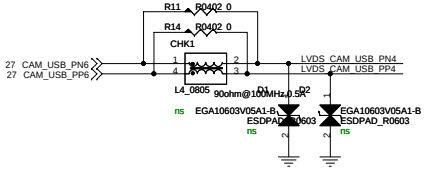
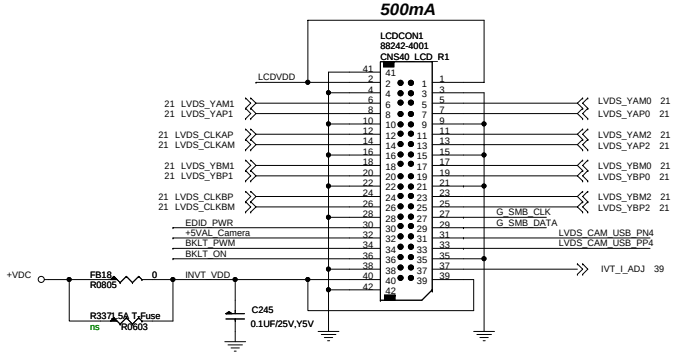
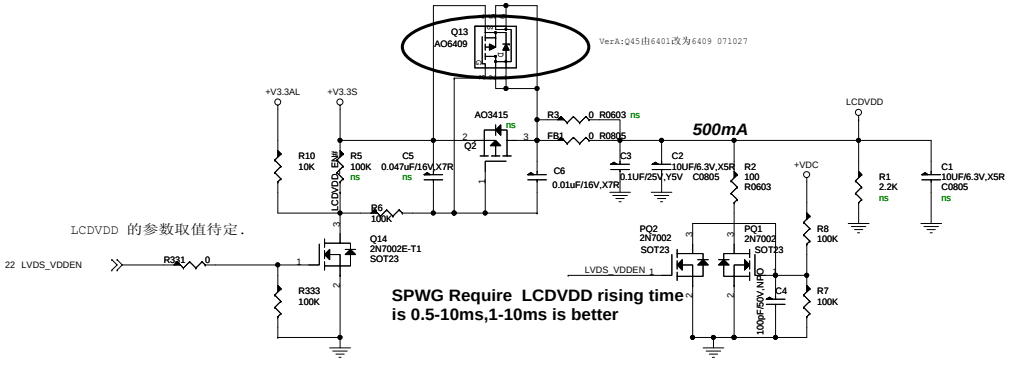
PANEL INTERFACE

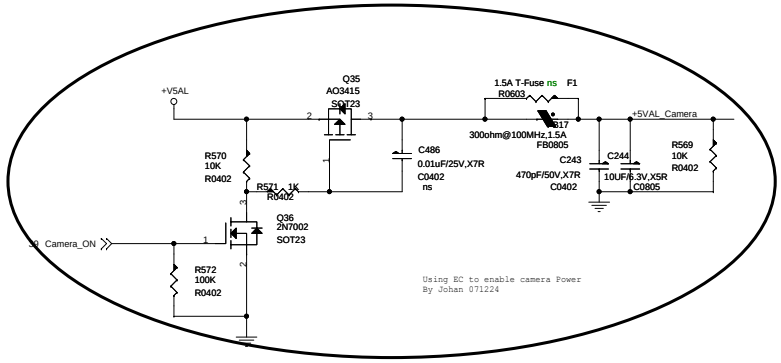


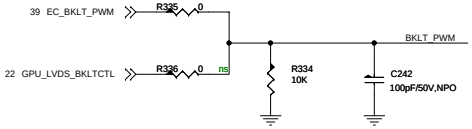


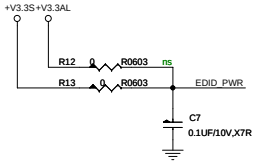


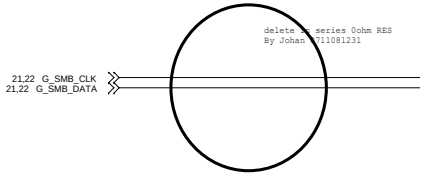












topstar®	TOPSTAR TECHNOLOGY	
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Page Name	LVDS&Inverter CONN	
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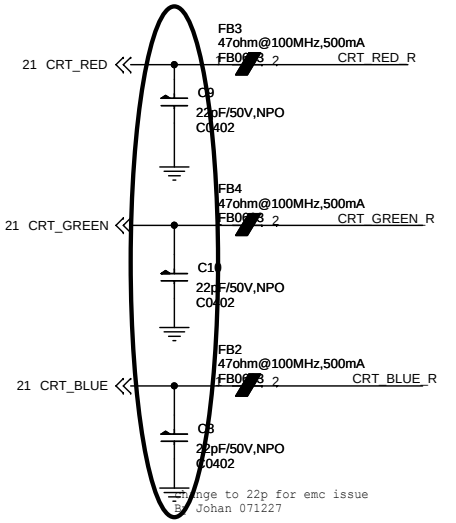
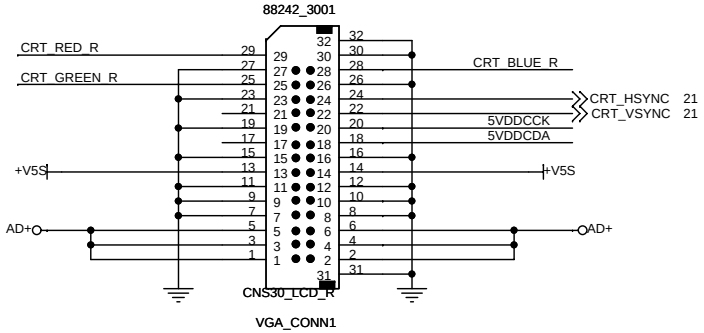
AD+ 40,41
+V5S 25,27,28,29,30,36,37,38,39,44,45,47,49,50
+V3.3S 6,7,12,14,15,16,18,21,22,23,25,26,27,28,29,32,33,34,35,36,37,38,39,44,45,47,48,49,50

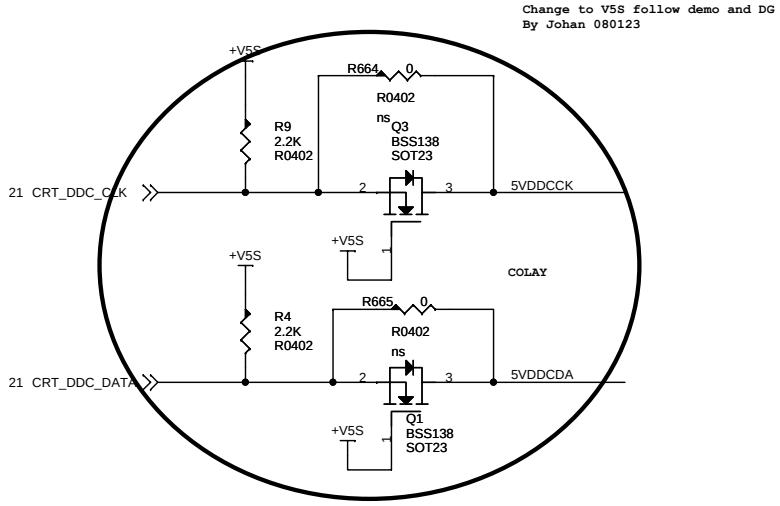
R = C
G = Y
B = NOT USED/BS
WHEN NOT USE, 75 OHM TO GND

Place close to VGA_CONN1





Video Board CONN



Topstar	TOPSTAR TECHNOLOGY		
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Page Name	VGA &SVIDEO &DCIN		
Size B	Project Name	M42P	Rev B
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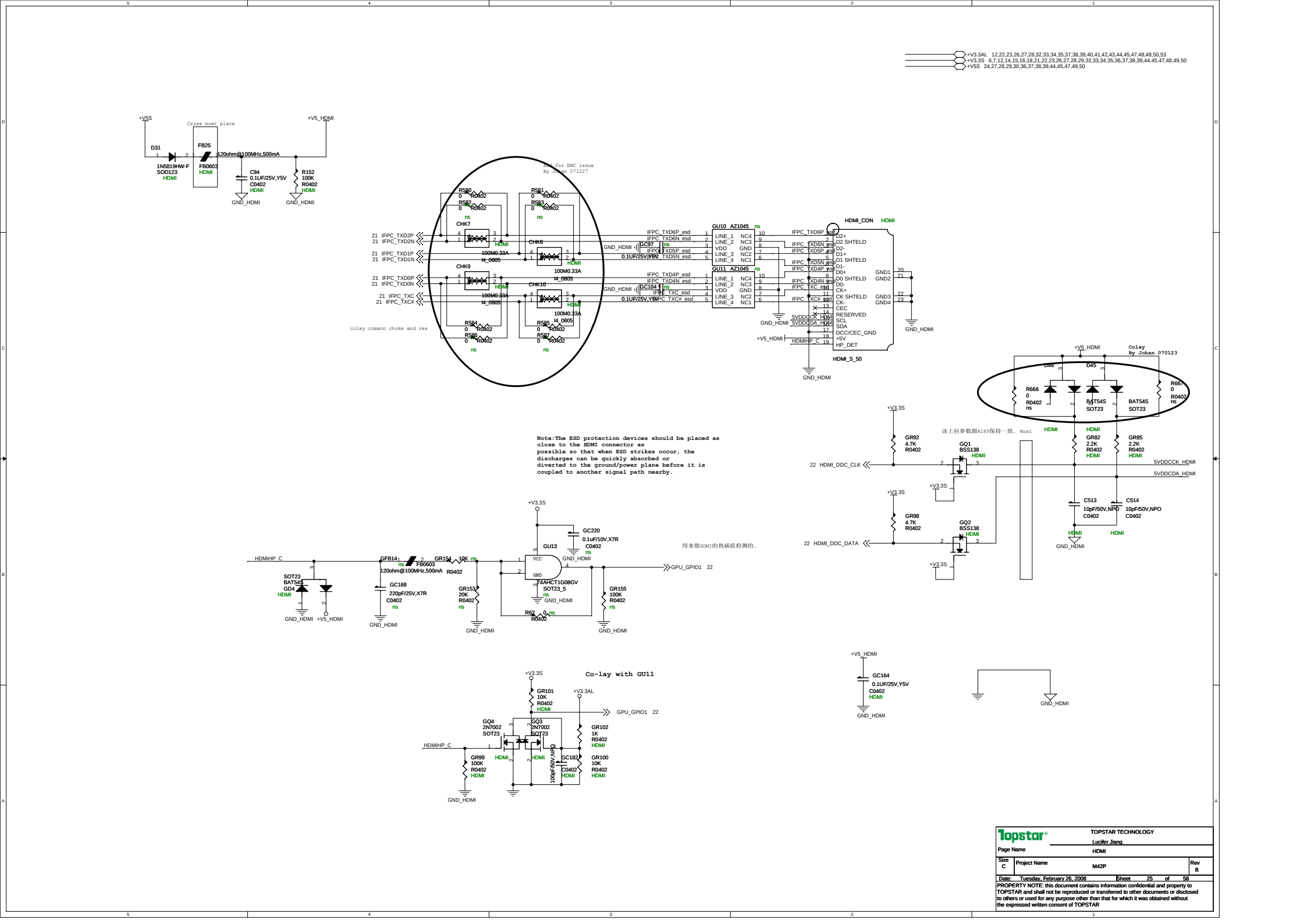
+V3.3AL 12,22,23,26,27,28,32,33,34,35,37,38,39,40,41,42,43,44,45,47,48,49,50,53
+V3.3S 6,7,12,14,15,16,18,21,22,23,26,27,28,29,32,33,34,35,36,37,38,39,44,45,47,48,49,50
+V5S 24,27,28,29,30,36,37,38,39,44,45,47,49,50
+VSS
Cross moat place
+V5_HDMI
D31
1N5819HW-F
SOD123
HDMI
FB25
FB0603
HDMI
120ohm@100MHz,500mA
C94
0.1UF/25V,Y5V
C0402
HDMI
R152
100K
R0402
HDMI
GND_HDMI
Add for EMC issue
By Johan 071227
R580
R581
R582
R583
R584
R585
R586
R587
0
R0402
ns
CHK7
CHK8
CHK9
CHK10
100M0.33A
I4_0805
HDMI
21 IFPC_TXD2P
21 IFPC_TXD2N
21 IFPC_TXD1P
21 IFPC_TXD1N
21 IFPC_TXD0P
21 IFPC_TXD0N
21 IFPC_TXC
21 IFPC_TXC#
colay common choke and res
GU10 AZ1045
GU11 AZ1045
LINE_1
LINE_2
LINE_3
LINE_4
NC1
NC2
NC3
NC4
VDD
GND
IFPC_TXD6P_esd
IFPC_TXD6N_esd
IFPC_TXD5P_esd
IFPC_TXD5N_esd
IFPC_TXD4P_esd
IFPC_TXD4N_esd
IFPC_TXC_esd
IFPC_TXC#_esd
GC97
GC104
0.1UF/25V,Y5V
GND_HDMI
HDMI_CON
HDMI_S_50
D2+
D2 SHTELD
D2-
D1+
D1 SHTELD
D1-
D0+
D0 SHTELD
D0-
CK+
CK SHTELD
CK-
CEC
RESERVED
SCL
SDA
DCC/CEC_GND
+5V
HP_DET
GND1
GND2
GND3
GND4
5VDDCCK_HDM
5VDDCDA_HDM
HDMIHP_C
Note:The ESD protection devices should be placed as close to the HDMI connector as possible so that when ESD strikes occur, the discharges can be quickly absorbed or diverted to the ground/power plane before it is coupled to another signal path nearby.
Colay
By Johan 070123
D44
D45
R666
R667
BAT54S
SOT23
该上拉参数跟R18F保持一致. Moat
+V3.3S
GR92
4.7K
R0402
GQ1
BSS138
22 HDMI_DDC_CLK
5VDDCCK_HDMI
5VDDCDA_HDMI
GR82
2.2K
GR85
GR98
GQ2
22 HDMI_DDC_DATA
C513
10pF/50V,NPO
C0402
C514
HDMIHP_C
GFB14
FB0603
120ohm@100MHz,500mA
GR154
10K
GC168
220pF/25V,X7R
GD4
SOT23
BAT54S
GR153
20K
GR155
100K
GU13
74AHCT1G08GV
SOT23_5
GC220
0.1uF/10V,X7R
R62
GPU_GPIO1 22
用来做HDMI的热插拔检测的.
Co-lay with GU11
GR101
10K
GQ4
2N7002
SOT23
GQ3
GR102
1K
GR99
100K
GC182
100pF/50V,NPO
GR100
10K
GC164
0.1UF/25V,Y5V
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Lucifer Jiang
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HDMI
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+V3.3S 6,7,12,14,15,16,18,21,22,23,25,27,28,29,32,33,34,35,36,37,38,39,44,45,47,48,49,50
ICH_EC_RTC 28
EC_RTC 42
+V1.05S 6,7,8,9,12,13,14,28,37,44,48,49,50
+V1.5S_PCIE_ICH 27,28
+V3.3AL 12,22,23,25,27,28,32,33,34,35,37,38,39,40,41,42,43,44,45,47,48,49,50,53

Note:The new SRTCRST# signal is used to reset the RTC registers used for the Intel Management Engine when the on-board battery is changed. The external capacitor and the external resistor between SRTCRST# and VccRTC were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid.
The RC time delay should be in the range of 18 ms to 25 ms. There must not be a jumper for SRTCRST# pin. The SRTCRST# does not impact the implementation of CMOS clearing.

Voltage Swing on RTCX1 pin should not exceed 1.0V.

ICH_EC_RTC
R269 332K,1% R0402
332K 1% PULL HIGH TO VBAT_RTC FOR ICH8M INTRNAL VR ENABLE(PULL LOW DISABLE)
ICH_INTVRMEN
R293 0 ns R0402

EC_RTC
D22 BAT54C SOT23
ICH_EC_RTC
C235 1uF/10V,X7R C0603
R309 1K R0402
R261 20K
R268 R0402 20K
R262 R0402 1M R0402
C430 1uF/10V,X7R C0603
C223 1uF/10V,X7R C0603
J9 JOPEN RESISTOR_1 ns
CMOS Settings J1
Clear CMOS Short
Keep CMOS Open
Y4 32.768KHz XS4_8038
C463 15PF/50V,NPO C0402
C462 15PF/50V,NPO C0402
R523 10M R0402
RTCBAT1 CONN2_R CNS2_R
Delete RTCBat socket for mechanical conflict

SPONGE_RTC1 RTCBAT GLUE
RTC_BAT1
RTCBAT with Cable
根据机构定Cable尺寸

U6A
RTCX1 C23
RTCX2 C24
RTC_RST# A25
SRTC_RST# F20
SM_INTRUDER# C22
ICH_INTVRMEN B22
INTVRMEN A22
LAN100_SLP
RTC

If LAN interface is not used, this signal can be left as No Connect.
R282 0 R0402 ns
GLAN_CLK E25
LAN_RSTSYNC C13
+V1.5S_PCIE_ICH
R487 24.9,1% R0402
LAN_RXD0 E14
LAN_RXD1 G13
LAN_RXD2 D14
LAN_TXD0 D13
LAN_TXD1 D12
LAN_TXD2 E13
GPIO56 B10
GLAN_COMPI B28
GLAN_COMPO B27
LAN / GLAN

C373 ns 5.6pF/50V,NPO C0402
C368 ns 5.6pF/50V,NPO C0402
36 AZALIA_CODEC_BITCLK R428 33 R0402
37 AZALIA_MDC_BITCLK R428 33 R0402 MDC
36 AZALIA_CODEC_SYNC R428 33 R0402
37 AZALIA_MDC_SYNC R428 33 R0402 MDC
36 AZALIA_CODEC_RST# R428 33 R0402
37 AZALIA_MDC_RST# R428 33 R0402 MDC
AZALIA_BITCLK AF6
ACSYNC_D AH4
AZALIA_RST_ AE7
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0 AE4
HDA_SDIN1 AG4
HDA_SDIN2 AH3
HDA_SDIN3 AE5
HDA_SDOUT AG5
HDA_DOCK_EN# AG7
HDA_DOCK_EN#/GPIO33 AF8
HDA_DOCK_RST#/GPIO34
IHDA

Reserved for GPU codec application By Johan 070123
ns ICTP T135
36 AZALIA_CODEC_SDOUT R189 22 R0402 AC_SDOUT
37 AZALIA_MDC_SDOUT R185 22 R0402 MDC
ns ICTP T136

38 IDE_LED# AG8 SATALED#

SATA HDD
29 SATA_RXN0 AJ16 SATA0RXN
29 SATA_RXP0 AH16 SATA0RXP
29 SATA_TXN0 AE17 SATA0TXN
29 SATA_TXP0 AG17 SATA0TXP
C0402 C370 0.01uF/25V,X7R
C0402 C369 0.01uF/25V,X7R

SATA ODD
29 SATA_RXN1 AH13 SATA1RXN
29 SATA_RXP1 AJ13 SATA1RXP
29 SATA_TXN1 AG14 SATA1TXN
29 SATA_TXP1 AF14 SATA1TXP
C0402 C135 0.01uF/25V,X7R
C0402 C134 0.01uF/25V,X7R
SATA

Same distance to the ICH
Close the ICH as possible

ICH9M REV 1.0

FWH0/LAD0 K5 LPC_AD0 33,39
FWH1/LAD1 K4 LPC_AD1 33,39
FWH2/LAD2 L6 LPC_AD2 33,39
FWH3/LAD3 K2 LPC_AD3 33,39
FWH4/LFRAME# K3 LPC_FRAME# 33,39
LDRQ0# J3
LDRQ1#/GPIO23 J1
LPC

+3.3S
R239 10K R0402
R242 10K R0402 ns

A20GATE N7 H_A20GATE 39
A20M# AJ27 H_A20M# 7
DPRSTP# A25 H_DPRSTP# 7,12,49
DPSLP# AE23 H_DPSLP# 7
FERR# A26 R207 56 R0402 H_FERR# 7
CPUPWRGD AD22 H_PWRGD 7
IGNNE# AF25 H_IGNNE# 7
INIT# AE22 H_INIT# 7
INTR AG25 H_INTR 7
RCIN# L3 H_RCIN# 39
NMI AF23 R435 R0402 H_NMI 7
SMI# AF24 H_SMI# 7
STPCLK# AH27 H_STPCLK# 7
THRMTRIP# AG26 R216 54.9,1% PM_THRMTRIP# 7,12,37
TP12 AG27 T67 ICTP ns R0402
CPU

+V1.05S
R213 56 R0402
R454 56 ns R0402
R214 56 R0402
R208 R0402
R444 R0402
R215 56 R0402
R177 NEEDS BE PLACE WITHIN 2" OF ICH9, R173 NEEDS BE PLACED WITHIN 2" OF R177 WITHOUT STUB

Checklist:the series termination RES of FERR#/IERR#/THERMTRIP are 56/56/55ohm。

SATA4RXN AH11 SATA4_RXN R192 1K R0402 ns
SATA4RXP AJ11 SATA4_RXP R191 1K R0402 ns
SATA4TXN AG12
SATA4TXP AF12
SATA5RXN AH9 SATA5_RXN R194 1K R0402 ns
SATA5RXP AJ9 SATA5_RXP R193 1K R0402 ns
SATA5TXN AE10
SATA5TXP AE10
SATA_CLKN AH18 CLK_ICH_SATA# 6
SATA_CLKP AJ18 CLK_ICH_SATA 6
SATARBIAS# AJ7 R0402 24.9,1% R427
SATARBIAS AH7
within 500 mils of the ICH9-M
No stuff for SATA function

+V3.3AL
R275 10K R0402
GPIO56
HDA_DOCK_EN#
R437 1K ns R0402

C515 5.6pF/50V,NPO C0402
21 AZALIA_GPU_BITCLK R569 22 R0402 AZALIA_CODEC_BITCLK
21 ACSYNC_GPU_D R569 22 R0402 AZALIA_CODEC_SYNC
21 AZALIA_GPU_RST# R570 22 R0402 AZALIA_CODEC_RST#
21 AC_GPU_SDOUT R571 22 R0402 AZALIA_CODEC_SDOUT
ns
Reserved for GPU codec application By Johan 070123

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	Lucifer Jiang	
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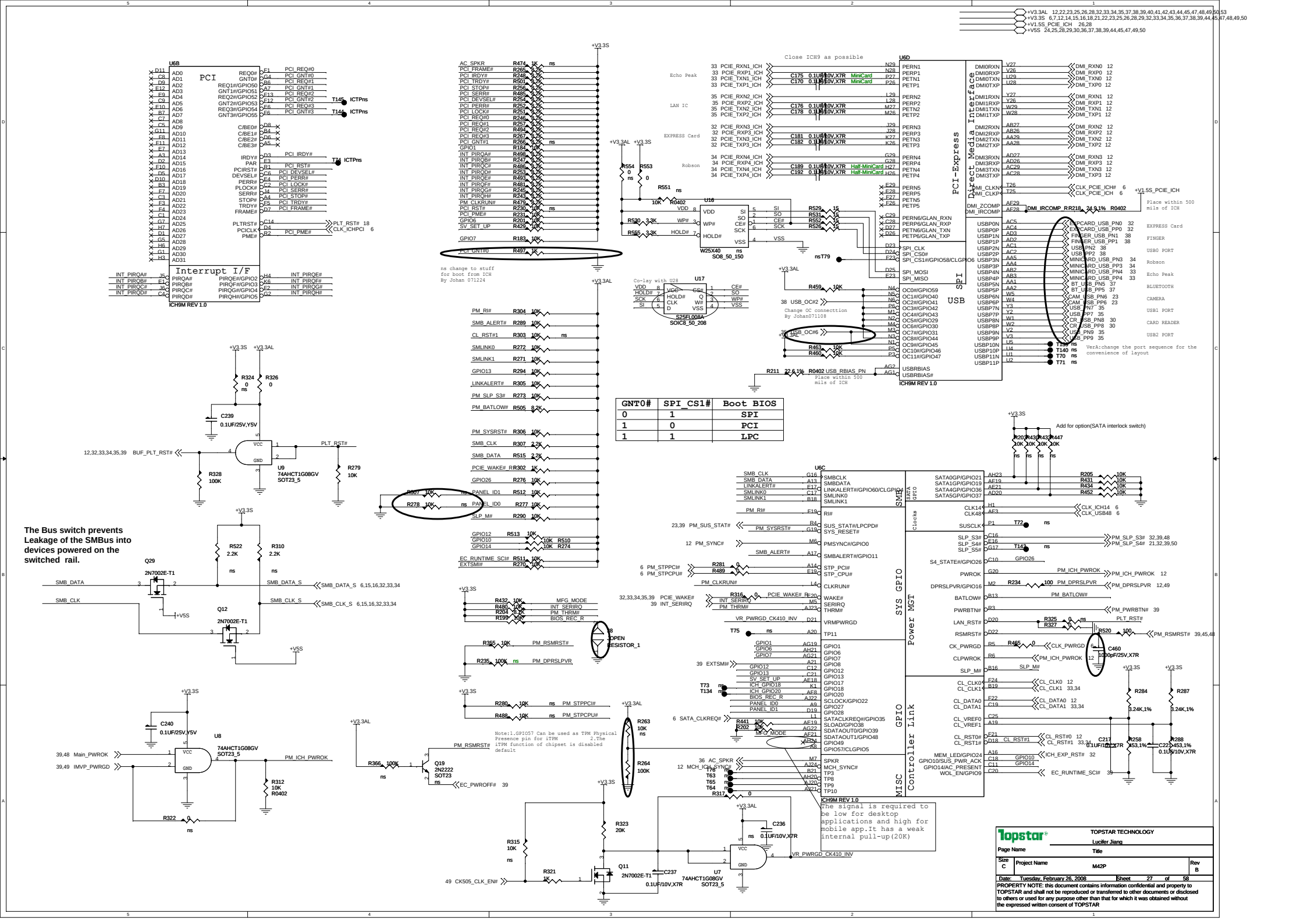
+V3.3AL 12,22,23,25,26,28,32,33,34,35,37,38,39,40,41,42,43,44,45,47,48,49,50,53
+V3.3S 6,7,12,14,15,16,18,21,22,23,25,26,28,29,32,33,34,35,36,37,38,39,44,45,47,48,49,50
+V1.5S_PCIE_ICH 26,28
+V5S 24,25,28,29,30,36,37,38,39,44,45,47,49,50
U6B
PCI
Interrupt I/F
ICH9M REV 1.0
U6D
PCI-Express
Direct Media Interface
SPI
USB
ICH9M REV 1.0
Close ICH9 as possible
Echo Peak
LAN IC
EXPRESS Card
Robson
Co-lay with U28
U17
S25FL008A
SOIC8_50_208
W25X40
SO8_50_150
Change OC connecttion
By Johan071108
Place within 500 mils of ICH
Add for option(SATA interlock switch)
U6C
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
The signal is required to be low for desktop applications and high for mobile app.It has a weak internal pull-up(20K)
ns change to stuff for boot from ICH By Johan 071224
The Bus switch prevents Leakage of the SMBus into devices powered on the switched rail.
Note:1.GPIO57 Can be used as TPM Physical Presence pin for iTPM 2.The iTPM function of chipset is disabled default
U9 74AHCT1G08GV SOT23_5
U8 74AHCT1G08GV SOT23_5
U7 74AHCT1G08GV SOT23_5
Q29 2N7002E-T1
Q12 2N7002E-T1
Q19 2N2222 SOT23
Q11 2N7002E-T1
OPEN RESISTOR_1
GNT0# SPI_CS1# Boot BIOS
0 1 SPI
1 0 PCI
1 1 LPC
TOPSTAR TECHNOLOGY
Lucifer Jiang
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Title
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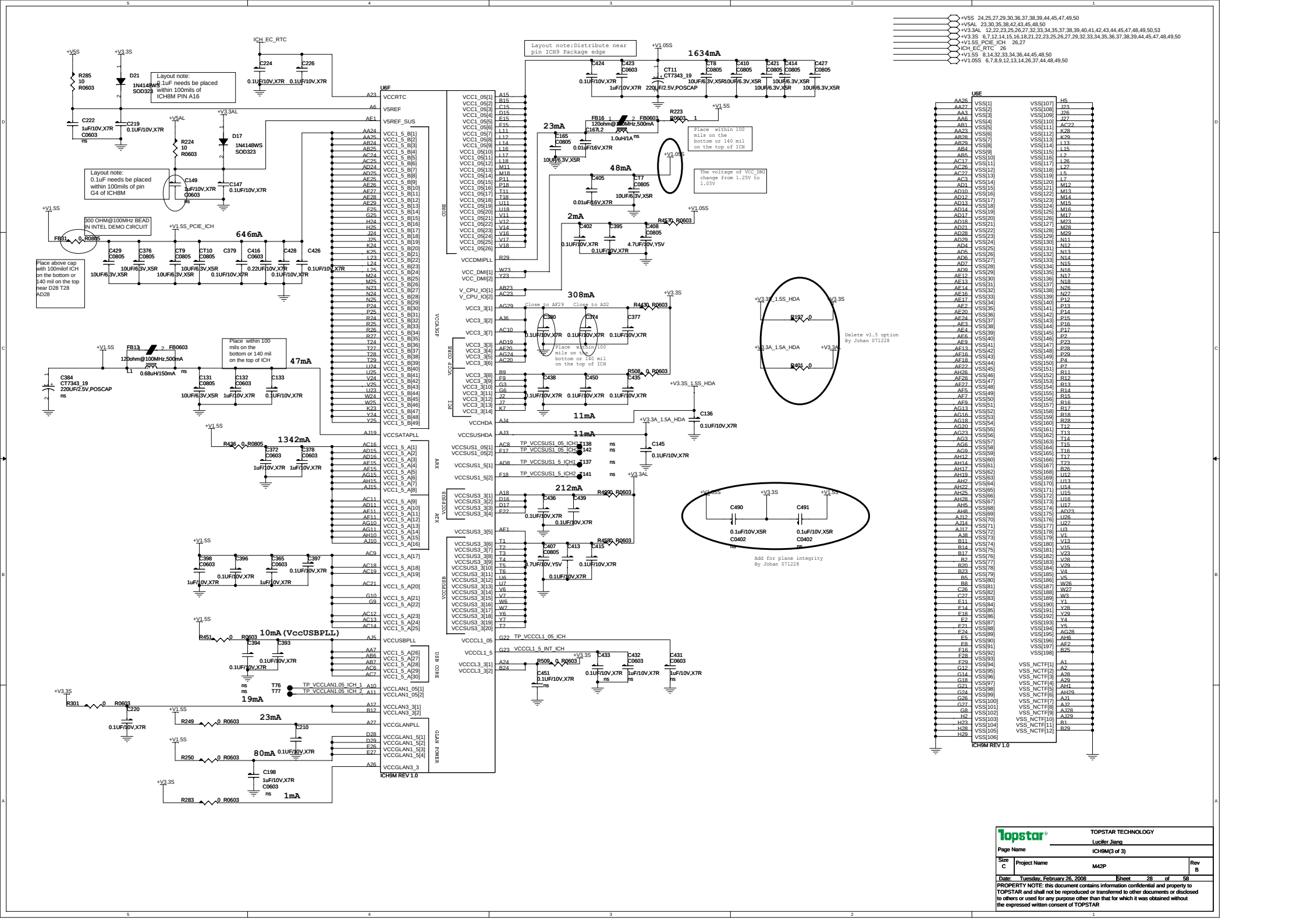
+V5S 24,25,27,29,30,36,37,38,39,44,45,47,49,50
+V5AL 23,30,35,38,42,43,45,48,50
+V3.3AL 12,22,23,25,26,27,32,33,34,35,37,38,39,40,41,42,43,44,45,47,48,49,50,53
+V3.3S 6,7,12,14,15,16,18,21,22,23,25,26,27,29,32,33,34,35,36,37,38,39,44,45,47,48,49,50
+V1.5S_PCIE_ICH 26,27
ICH_EC_RTC 26
+V1.5S 8,14,32,33,34,36,44,45,48,50
+V1.05S 6,7,8,9,12,13,14,26,37,44,48,49,50
U6F
U6E
ICH9M REV 1.0
Layout note:Distribute near pin ICH9 Package edge
Layout note: 0.1uF needs be placed within 100mils of ICH8M PIN A16
Layout note: 0.1uF needs be placed within 100mils of pin G4 of ICH8M
Place above cap with 100milof ICH on the bottom or 140 mil on the top near D28 T28 AD28
300 OHM@100MHz BEAD IN INTEL DEMO CIRCUIT
Place within 100 mils on the bottom or 140 mil on the top of ICH
Place within 100 mils on the bottom or 140 mil on the top of ICH
The voltage of VCC_DMI change from 1.25V to 1.05V
Delete v1.5 option By Johan 071228
Add for plane integrity By Johan 071228
1634mA
646mA
47mA
1342mA
10mA(VccUSBPLL)
19mA
23mA
80mA
1mA
2mA
48mA
308mA
11mA
212mA
TOPSTAR TECHNOLOGY
Lucifer Jiang
Page Name ICH9M(3 of 3)
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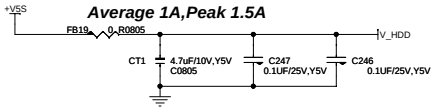
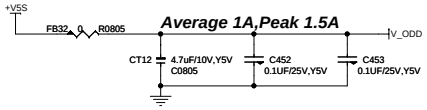
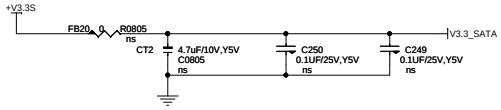
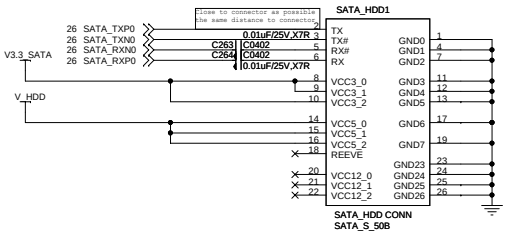
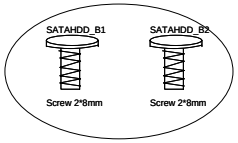
+V5S 24,25,27,28,30,36,37,38,39,44,45,47,49,50
+V3.3S 6,7,12,14,15,16,18,21,22,23,25,26,27,28,32,33,34,35,36,37,38,39,44,45,47,48,49,50

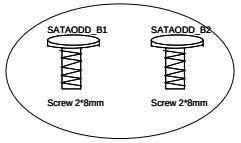


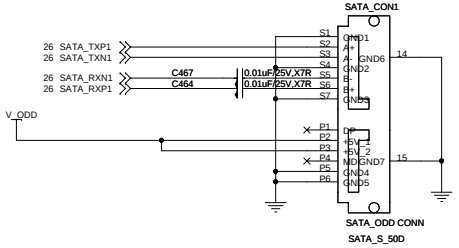












TOPSTAR TECHNOLOGY		
Lucifer Jiang		
Page Name	SATA HDD&ODD	
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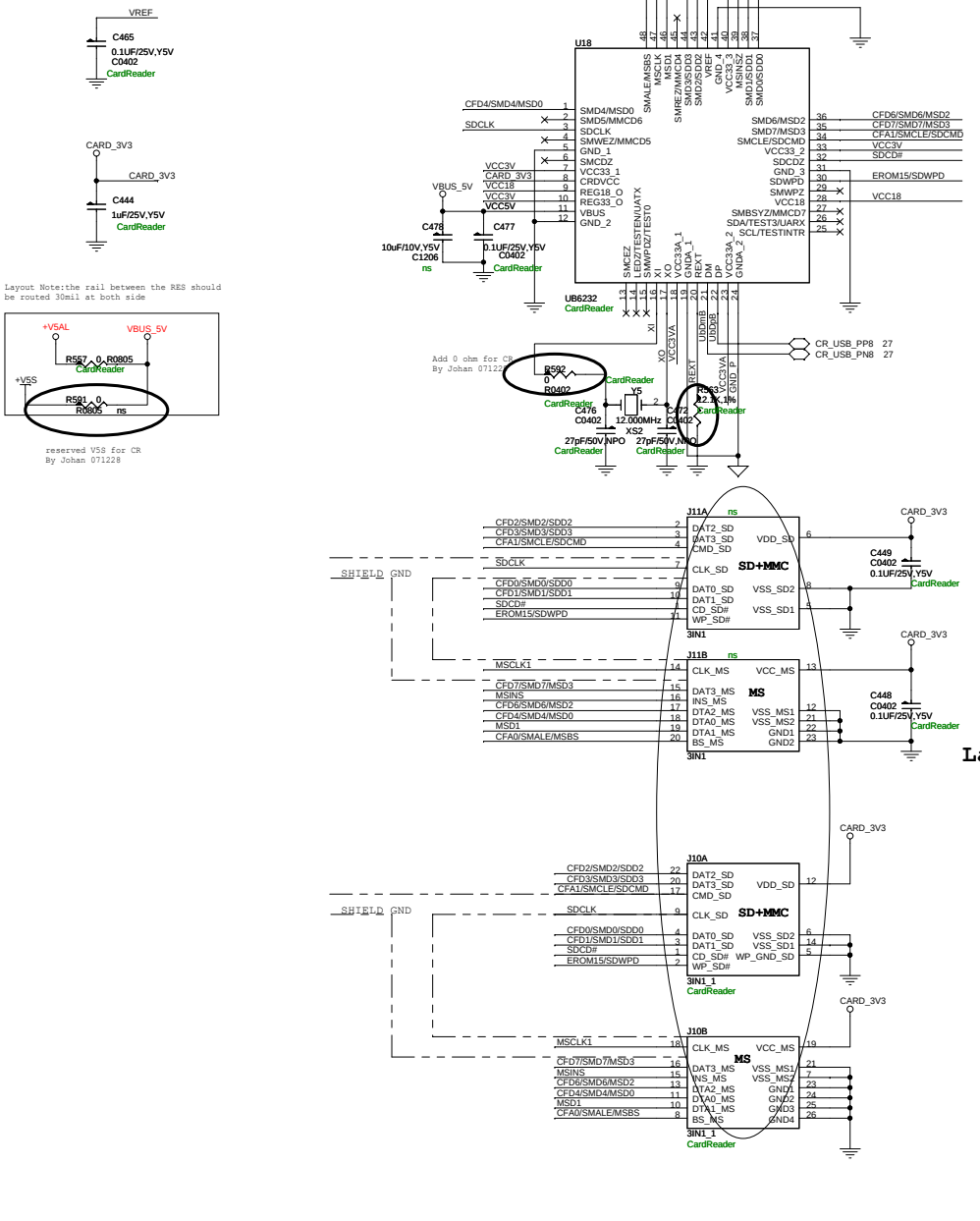
+V5AL 23,28,35,38,42,43,45,48,50
+V5S 24,25,27,28,29,36,37,38,39,44,45,47,49,50



Layout:COLAY J11 and J12

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	Lucifer Jiang	
Page Name	Card Reader(UB6232 USB)	
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	Lucifer Jiang	
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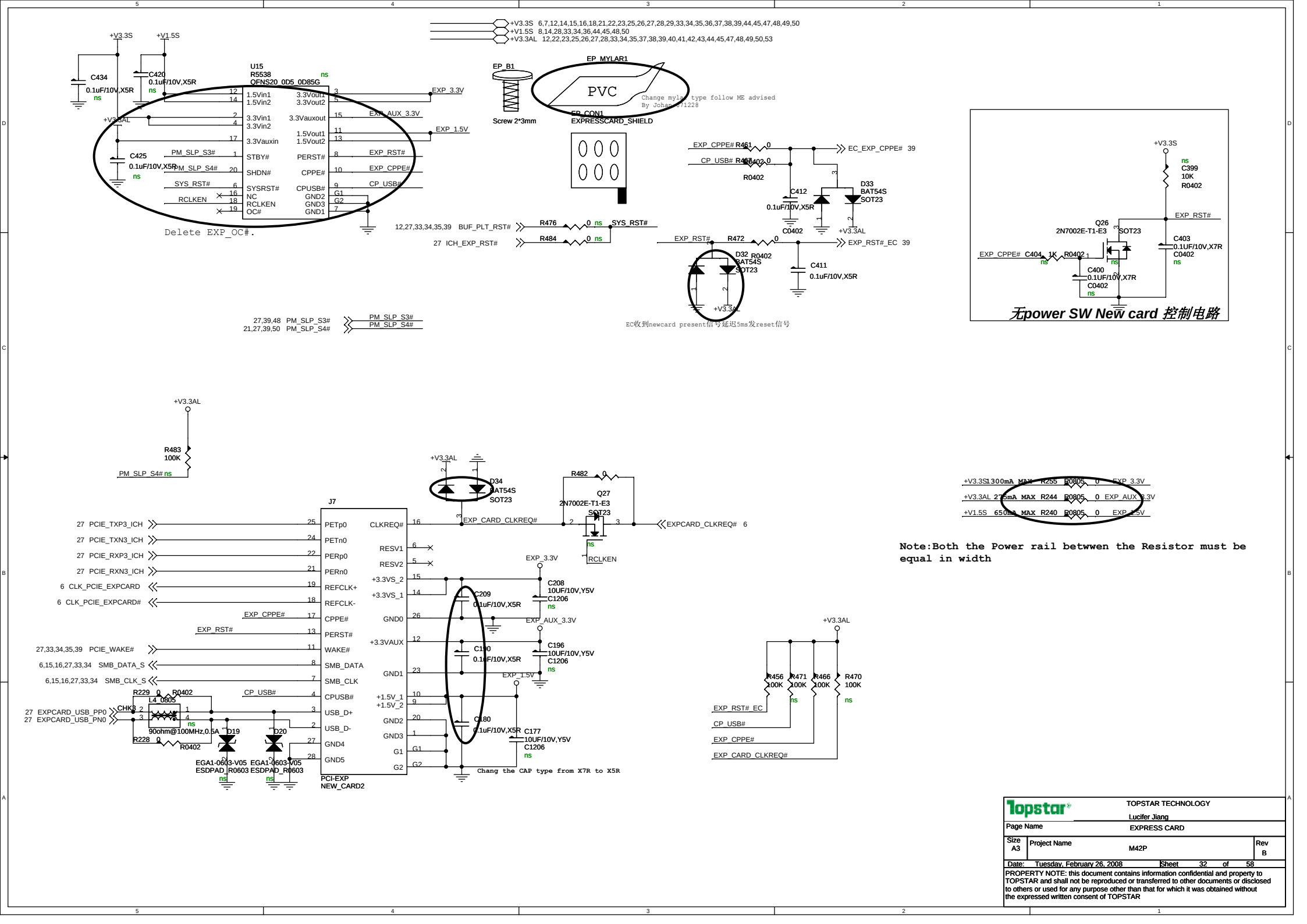

Topstar	TOPSTAR TECHNOLOGY	Lucifer Jiang
Page Name	EXPRESS CARD	
Size A3	Project Name M42P	Rev B
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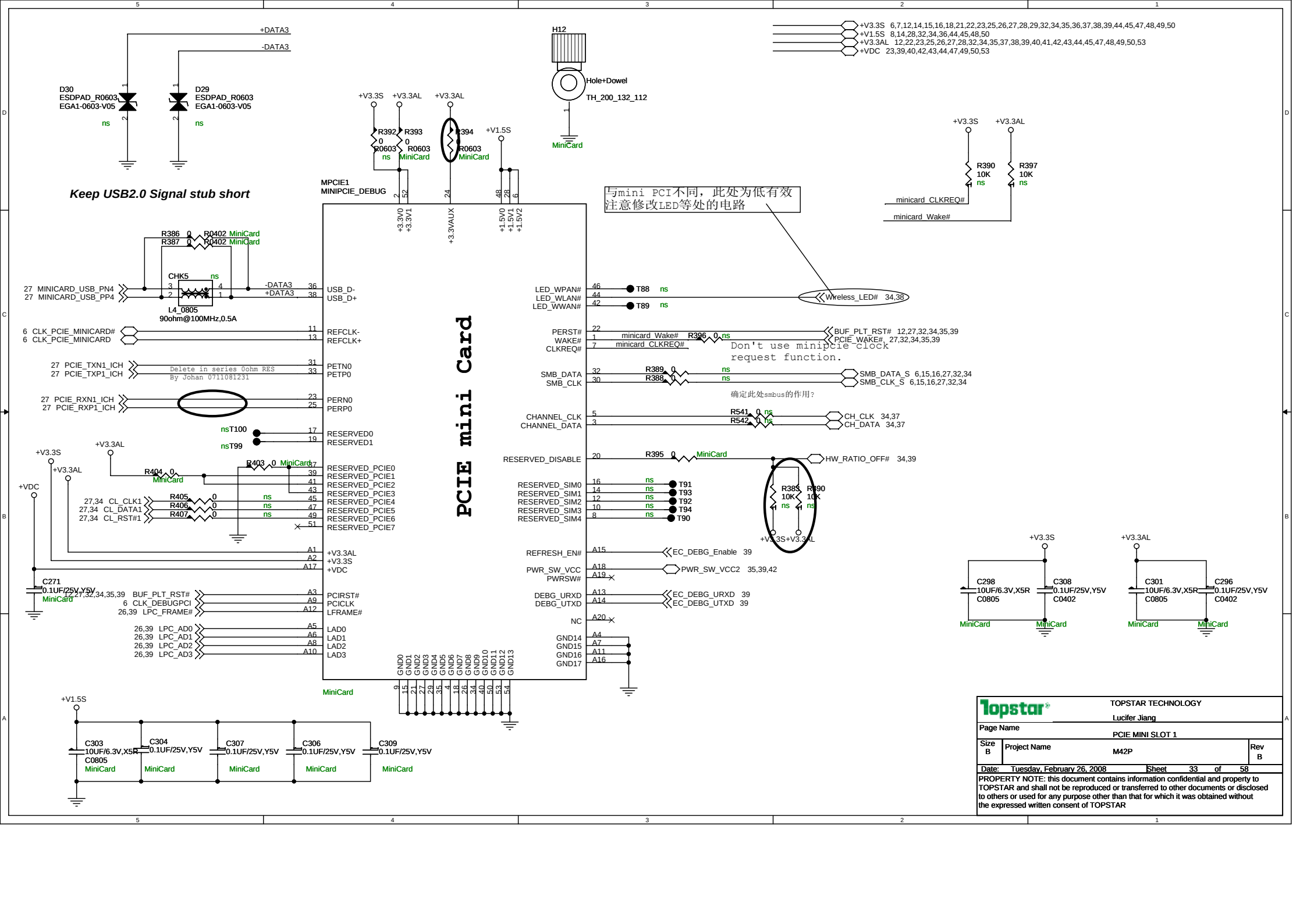

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Page Name	PCIE MINI SLOT 1
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+V3.3S 6,7,12,14,15,16,18,21,22,23,25,26,27,28,29,32,33,35,36,37,38,39,44,45,47,48,49,50
+V1.5S 8,14,28,32,33,36,44,45,48,50
+V3.3AL 12,22,23,25,26,27,28,32,33,35,37,38,39,40,41,42,43,44,45,47,48,49,50,53

H17
Hole+Dowel
TH_200_132_112
Half-MiniCard

+DATA8
-DATA8
D36 EGA10603V05A1-B ESDPAD_R0603 ns
D35 EGA10603V05A1-B ESDPAD_R0603 ns

Keep USB2.0 Signal stub short

+V3.3S +V3.3AL +V3.3AL
R500 0 R0603 ns Half-MiniCard
R506 0 R0603 Half-MiniCard
R504 0 R0603 Half-MiniCard
+V1.5S

MPCIE2
MINIPCIE_HALF

+3.3V0 +3.3V1 +3.3VAUX +1.5V0 +1.5V1 +1.5V2

R495 0 Half-MiniCard
R496 0 Half-MiniCard
CHK6 90ohm@100MHz,0.5A L4_0805 ns

27 MINICARD_USB_PN3
27 MINICARD_USB_PP3
-DATA8
+DATA8
USB_D-
USB_D+

6 CLK_PCIE_ROBSON#
6 CLK_PCIE_ROBSON
REFCLK-
REFCLK+

27 PCIE_TXN4_ICH
27 PCIE_TXP4_ICH
PETN0
PETP0

27 PCIE_RXN4_ICH
27 PCIE_RXP4_ICH
PERN0
PERP0

ns ICTP T150
ns ICTP T146
RESERVED0
RESERVED1

+V3.3AL
R523 0 Half-MiniCard
R532 0 Half-MiniCard
R0603
RESERVED_PCIE0
RESERVED_PCIE1
RESERVED_PCIE2
RESERVED_PCIE3
RESERVED_PCIE4
RESERVED_PCIE5
RESERVED_PCIE6
RESERVED_PCIE7

27,33 CL_CLK1 R534 0 ns
27,33 CL_DATA1 R535 0 ns
27,33 CL_RST#1 R536 0 ns

LED_WPAN#
LED_WLAN#
LED_WWAN#
T148 ns
T147 ns
Wireless_LED# 33,38

PERST#
WAKE#
CLKREQ#
WAKE# R538 0 ns
MiniPCIE_REQ#
BUF_PLT_RST# 12,27,32,33,35,39
PCIE_WAKE# 27,32,33,35,39

SMB_DATA R382 0 ns
SMB_CLK R381 0 ns
SMB_DATA_S 6,15,16,27,32,33
SMB_CLK_S 6,15,16,27,32,33

CHANNEL_CLK R537 0 ns
CHANNEL_DATA R543 0 ns
CH_CLK 33,37
CH_DATA 33,37

RESERVED_DISABLE R503 0 Half-MiniCard
HW_RATIO_OFF# 33,39

RESERVED_SIM0 T152 ICTP ns
RESERVED_SIM1 T151 ICTP ns
RESERVED_SIM2 T149 ICTP ns
RESERVED_SIM3 T154 ICTP ns
RESERVED_SIM4 T153 ICTP ns

R491 10K ns
R492 10K ns
+V3.3S +V3.3AL

GND0 GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13

Half-MiniCard
PCIE MINI CARD

+V3.3S +V3.3AL
R540 10K ns
R502 10K ns
R539 10K ns
MiniPCIE_REQ#
HW_RATIO_OFF#
WAKE#

+V1.5S
C441 10UF/6.3V,X5R C0805
C447 0.1UF/25V,Y5V C0402
C446 0.1UF/25V,Y5V C0402
C442 0.1UF/25V,Y5V C0402
C440 0.1UF/25V,Y5V C0402
Half-MiniCard

+V3.3S
C437 10UF/6.3V,X5R C0805
C468 0.1UF/25V,Y5V C0402
Half-MiniCard

+V3.3AL
C445 10UF/6.3V,X5R C0805
C443 0.1UF/25V,Y5V C0402
Half-MiniCard

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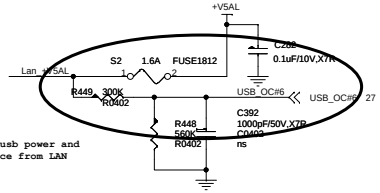
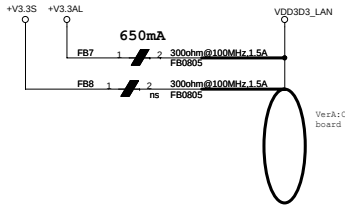
+VDC 23,33,39,40,42,43,44,47,49,50,53
+V5AL 23,28,30,38,42,43,45,48,50
+V3.3AL 12,22,23,25,26,27,28,32,33,34,37,38,39,40,41,42,43,44,45,47,48,49,50,53
+V3.3S 6,7,12,14,15,16,18,21,22,23,25,26,27,28,29,32,33,34,36,37,38,39,44,45,47,48,49,50
Isense_SYSP 40,52

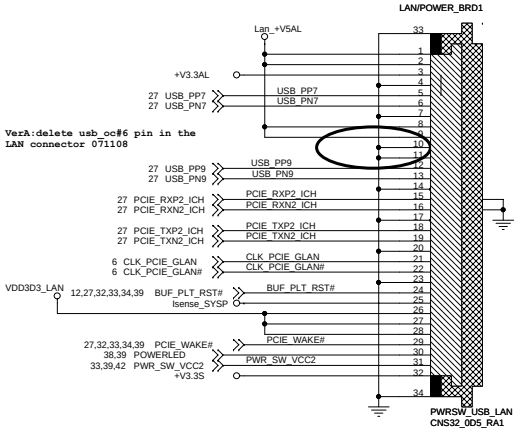
PWR LED/USB/Lan Connector



VerA:Change usb power and usb_oc#6 place from LAN board to MB.



VerA:Change the power decoupling CAP from MB board to daughter board.



topstar®	TOPSTAR TECHNOLOGY	
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Page Name	Power/USB/LAN CONN	
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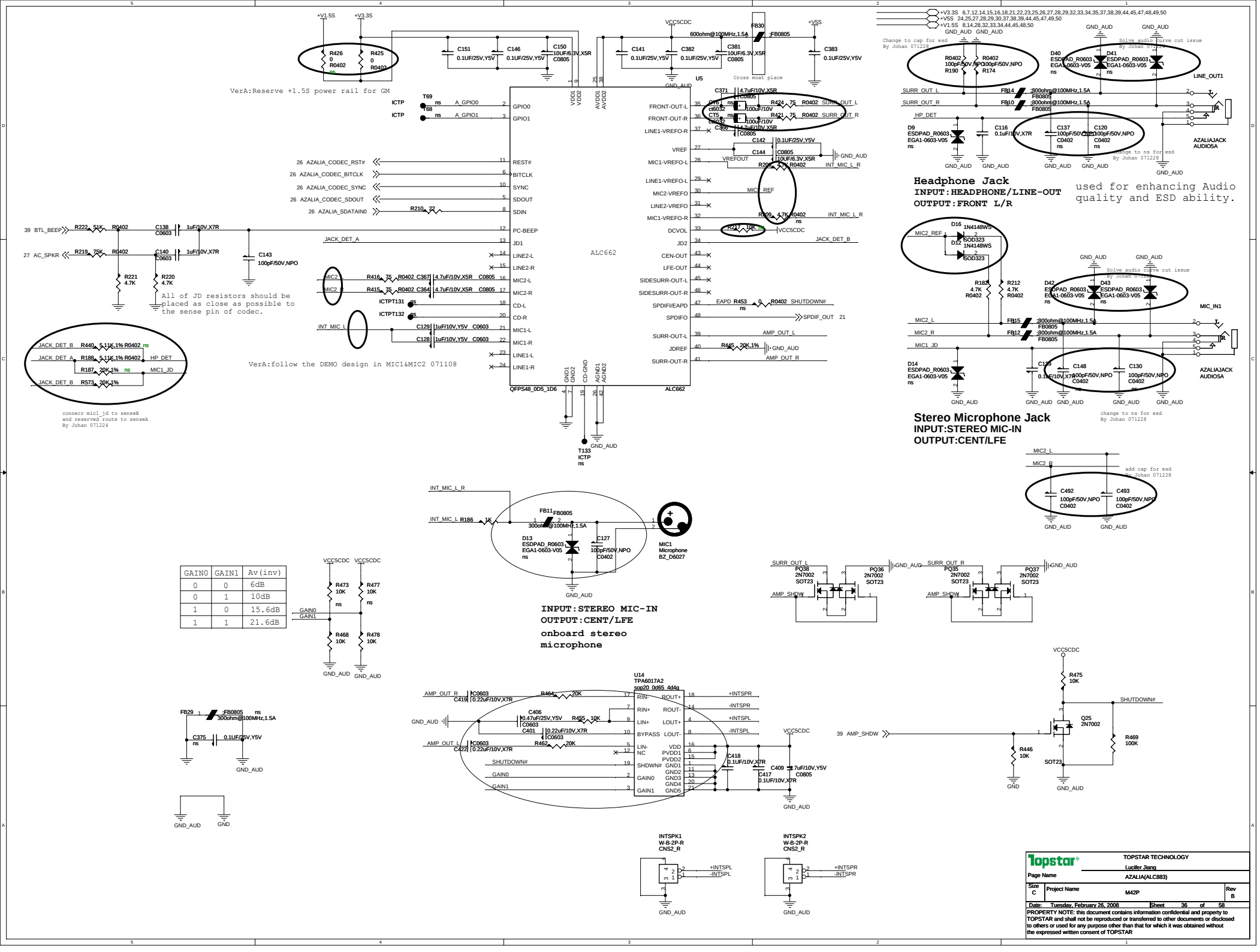
ALC662
QFPS48_0D5_1D6
U5
VerA:Reserve +1.5S power rail for GM
VerA:follow the DEMO design in MIC1&MIC2 071108
All of JD resistors should be placed as close as possible to the sense pin of codec.
connecr mic1_jd to senseB and reserved route to senseA By Johan 071224
Cross moat place
Change to cap for esd By Johan 071228
Solve audio curve cut issue By Johan 071228
change to ns for esd By Johan 071228
Headphone Jack
INPUT:HEADPHONE/LINE-OUT
OUTPUT:FRONT L/R
used for enhancing Audio quality and ESD ability.
Stereo Microphone Jack
INPUT:STEREO MIC-IN
OUTPUT:CENT/LFE
INPUT:STEREO MIC-IN
OUTPUT:CENT/LFE
onboard stereo microphone
GAIN0 GAIN1 Av(inv)
0 0 6dB
0 1 10dB
1 0 15.6dB
1 1 21.6dB
U14
TPA6017A2
sop20_0d65_4d4q
INTSPK1
W-B-2P-R
CNS2_R
INTSPK2
W-B-2P-R
CNS2_R
TOPSTAR TECHNOLOGY
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Page Name AZALIA(ALC883)
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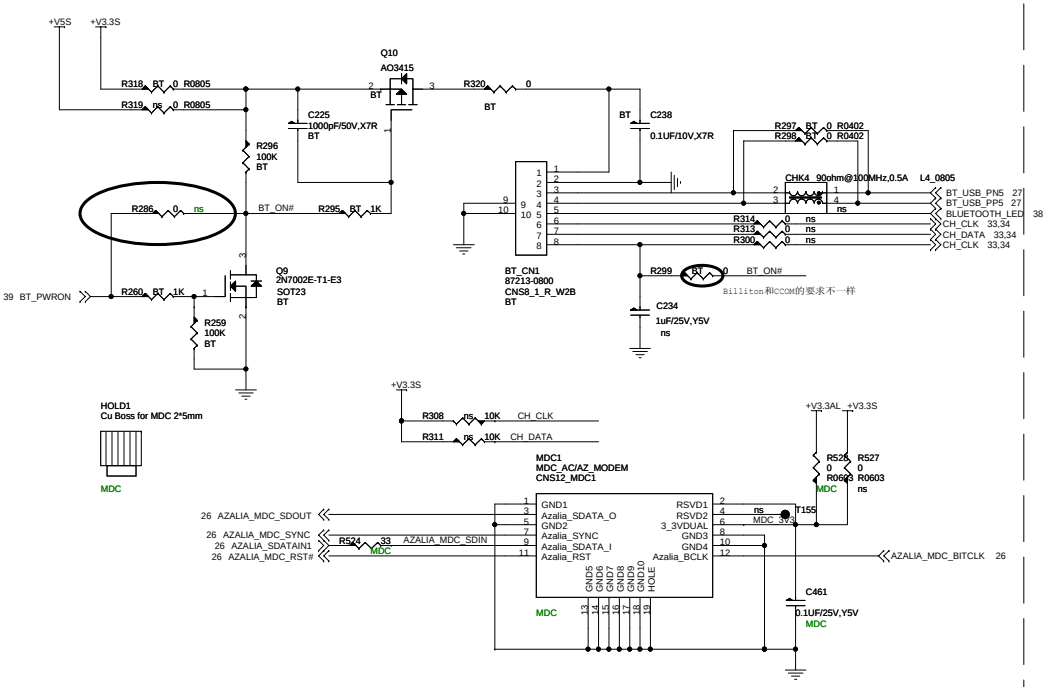
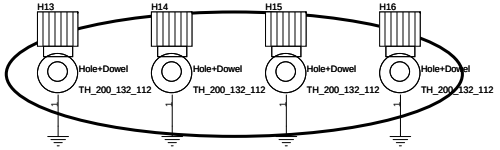
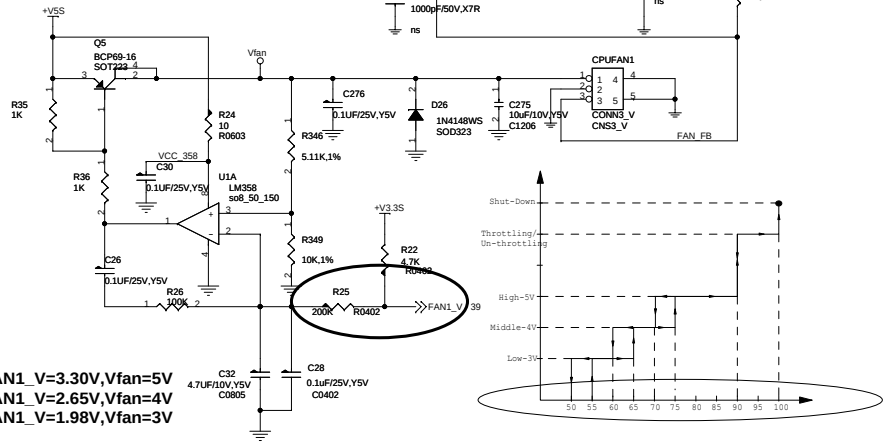
FAN Controller Circuit

MDC (Software MODEM)

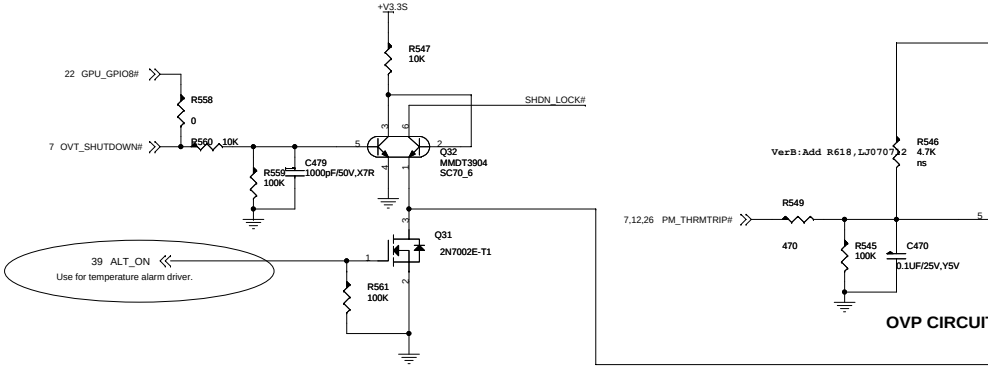




For FAN&Heatsink use

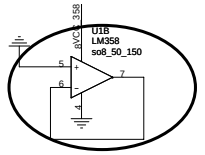


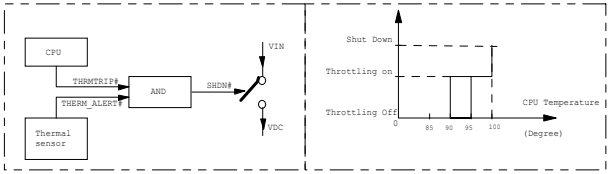
FAN1_V=3.30V,Vfan=5V
FAN1_V=2.65V,Vfan=4V
FAN1_V=1.98V,Vfan=3V



OVP CIRCUIT

VerA:Delete GMCH_TEMP signal and components 071026





PCB1
R20 MB
PCB

PCBA1
R20 PCBA
PCBA

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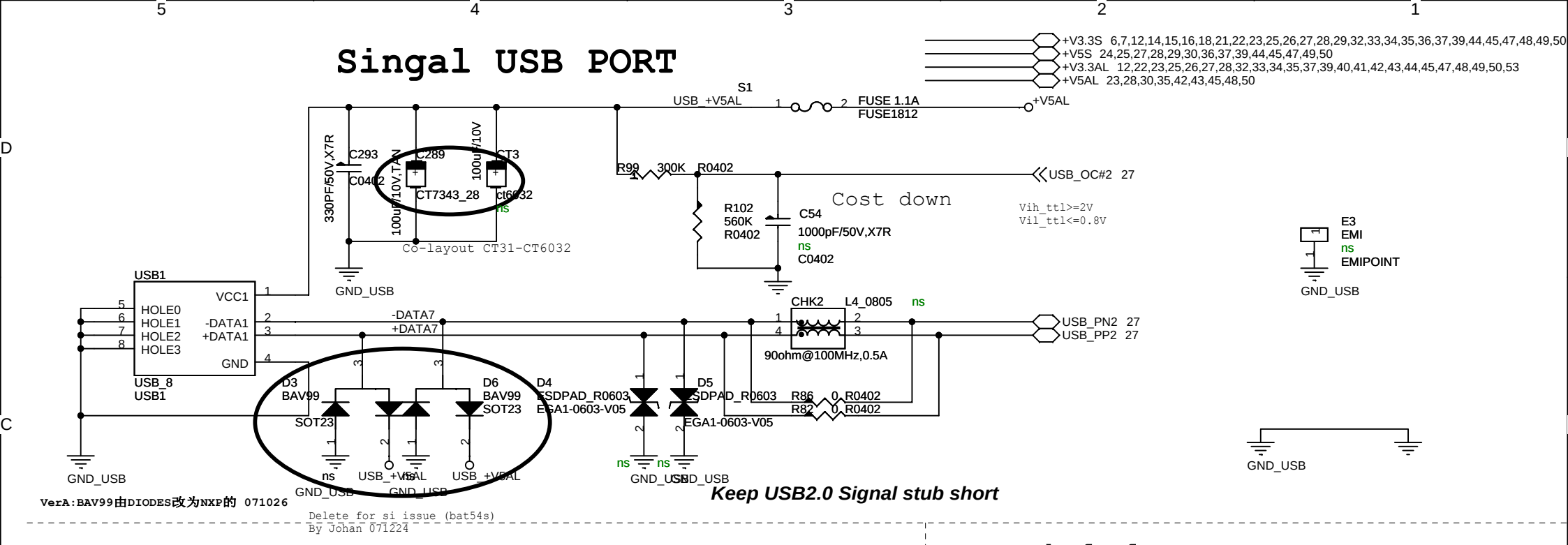
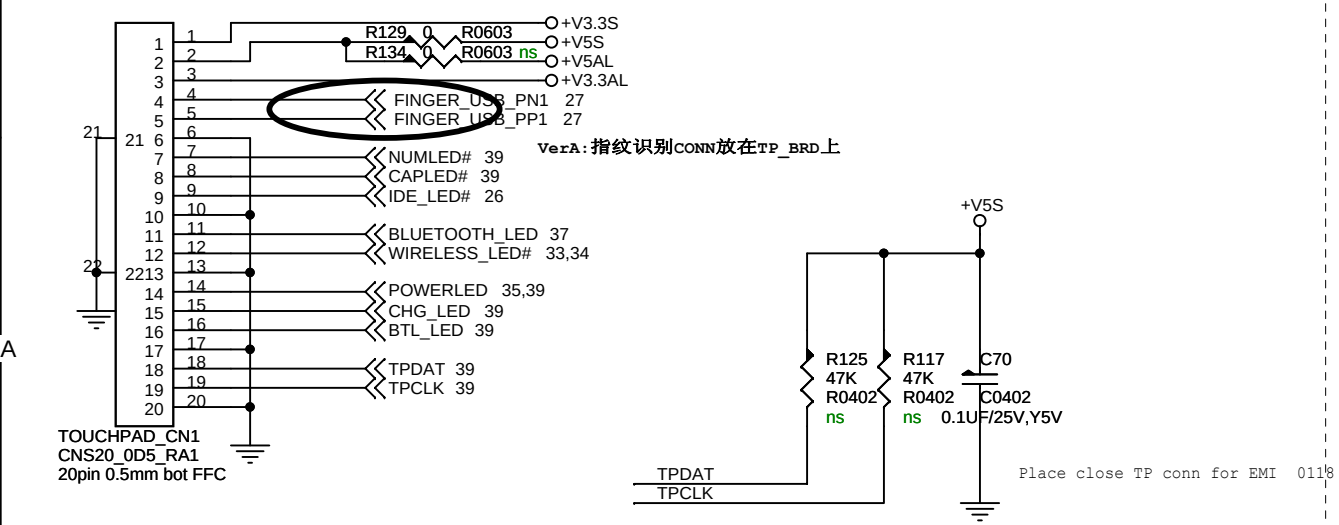
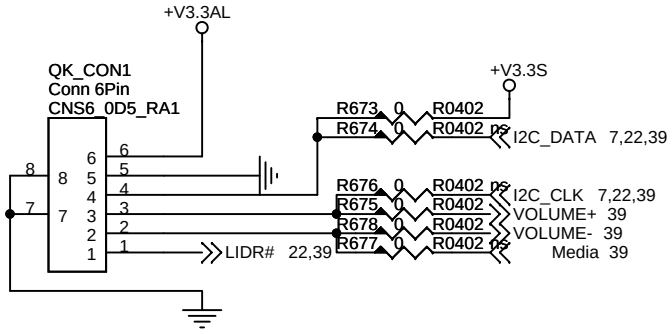
Singal USB PORT



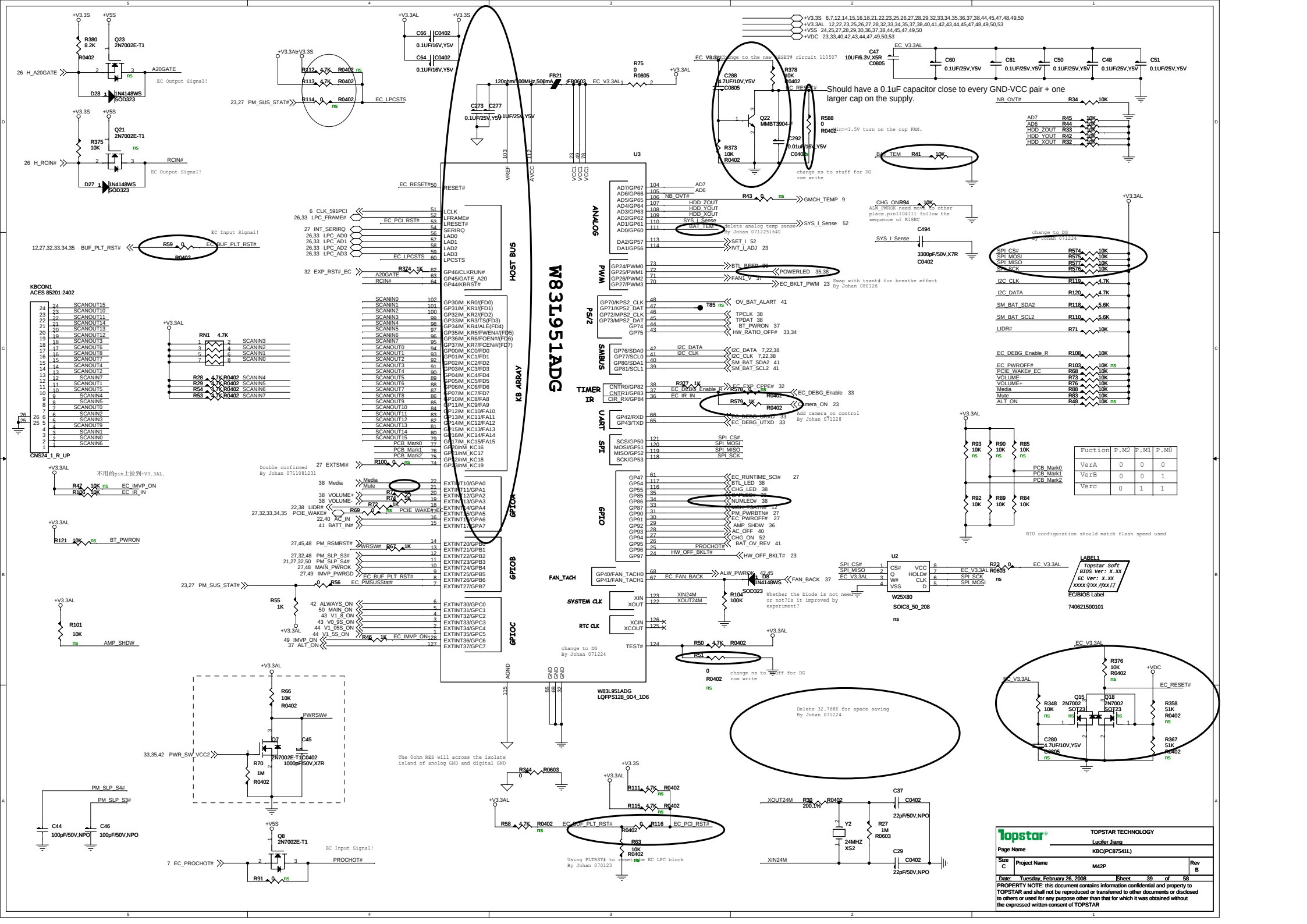
Touchpad Conn



Quick button Conn



Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	USB2.0&&LED CONN&Qkey CONN	
Size A4	Project Name M42P	Rev B
Date: Tuesday, February 26, 2008	Sheet 38 of 58	


W83L951ADG
LQFPS128_0D4_1D6
+V3.3S 6,7,12,14,15,16,18,21,22,23,25,26,27,28,29,32,33,34,35,36,37,38,44,45,47,48,49,50
+V3.3AL 12,22,23,25,26,27,28,32,33,34,35,37,38,40,41,42,43,44,45,47,48,49,50,53
+VSS 24,25,27,28,29,30,36,37,38,44,45,47,49,50
+VDC 23,33,40,42,43,44,47,49,50,53
Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.
HOST BUS
KB ARRAY
GPIOK
GPIOB
GPIOC
ANALOG
PWM
PS/2
SMBUS
TIMER IR
UART
SPI
GPIO
FAN_TACH
SYSTEM CLK
RTC CLK
KBCON1
ACES 85201-2402
CNS24_1_R_UP
U2
W25X80
SOIC8_50_208
LABEL1
EC/BIOS Label
740621500101
Fuction P.M2 P.M1 P.M0
VerA 0 0 0
VerB 0 0 1
Verc 0 1 1
BIU configuration should match flash speed used
Delete 32.768K for space saving By Johan 071224
Using PLTRST# to reset the EC LPC block By Johan 070123
The 0ohm RES will across the isolate island of anolog GND and digital GND
TOPSTAR TECHNOLOGY
Lucifer Jiang
Page Name KBC(PC87541L)
Size C
Project Name M42P
Rev B
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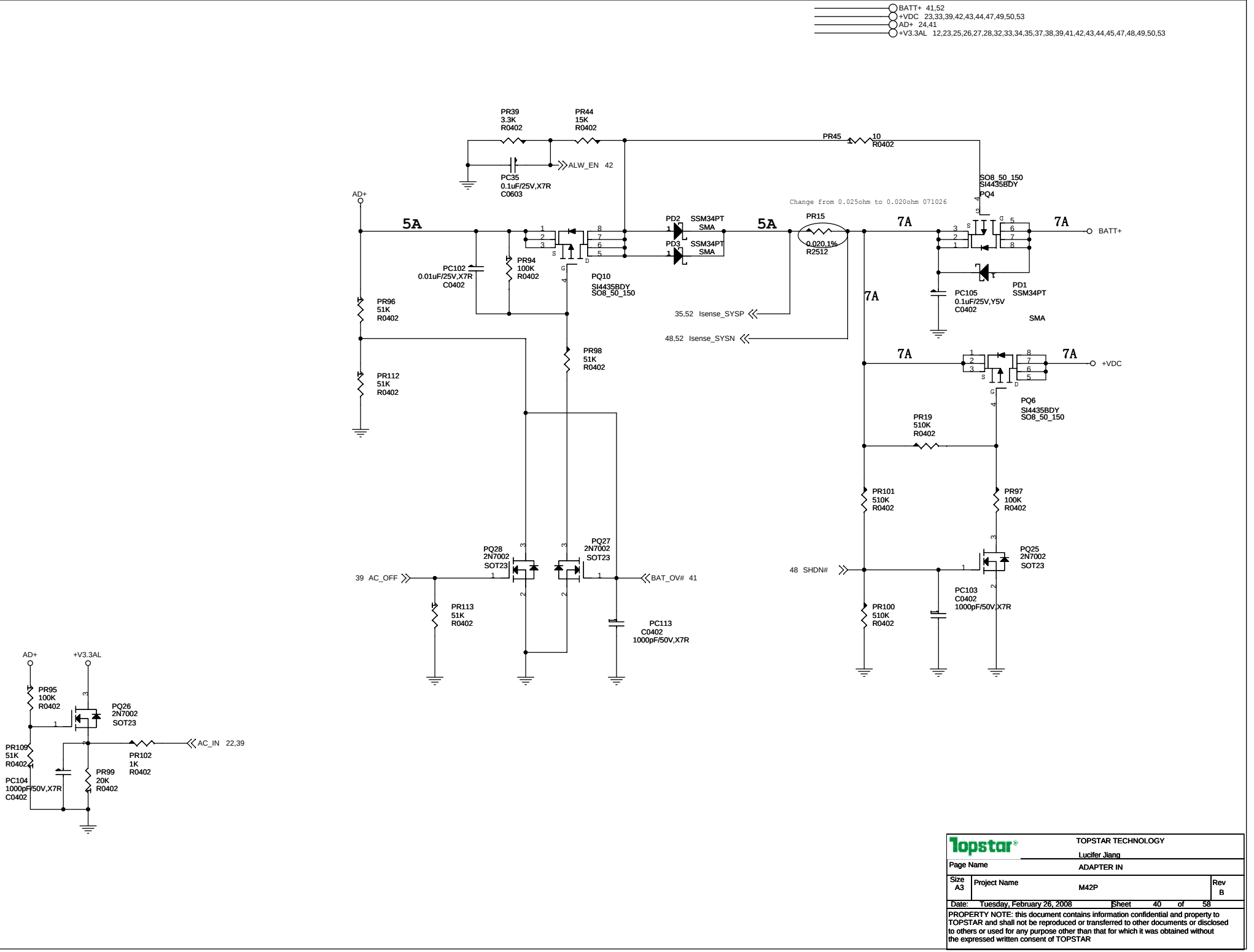
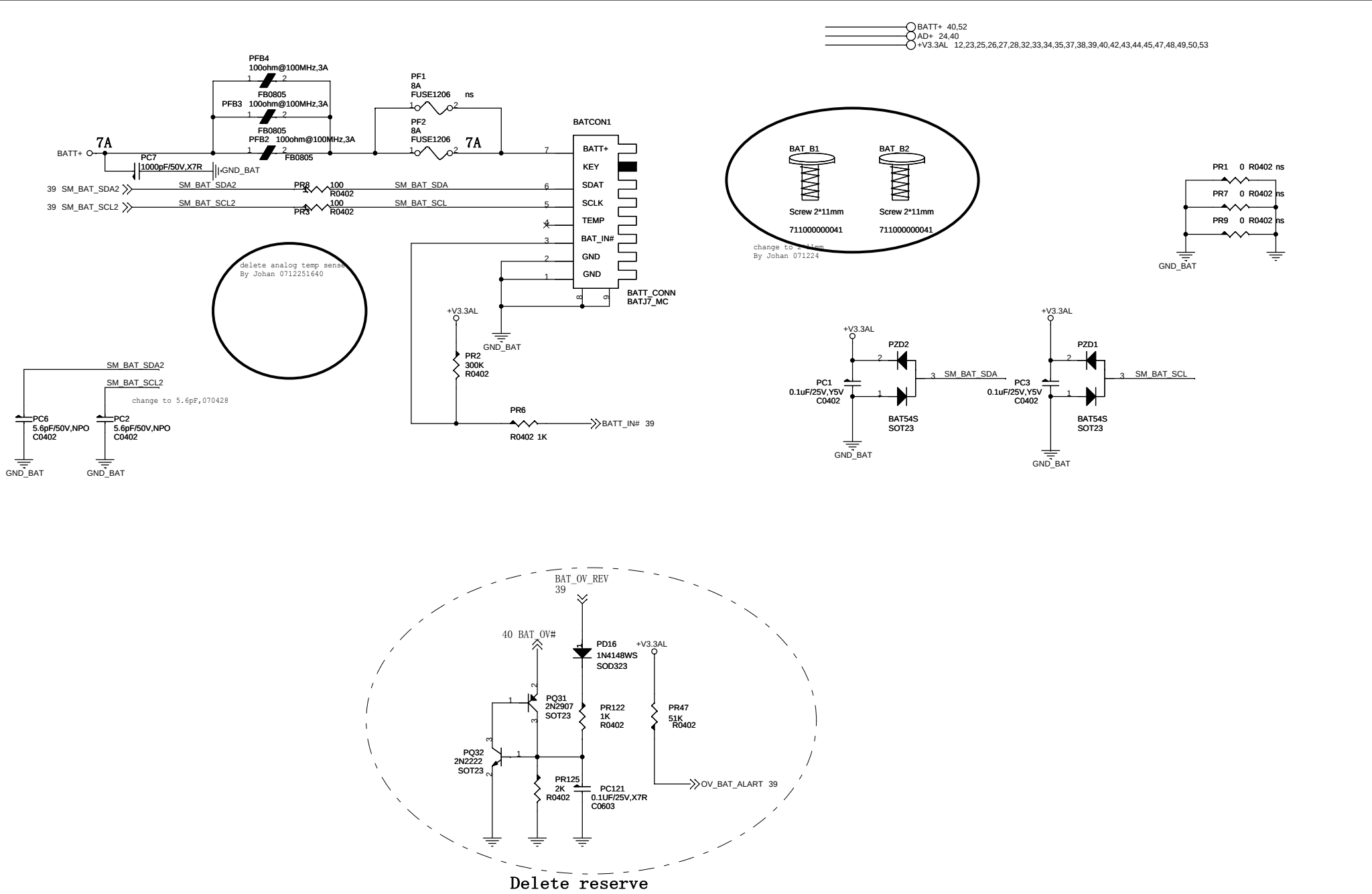
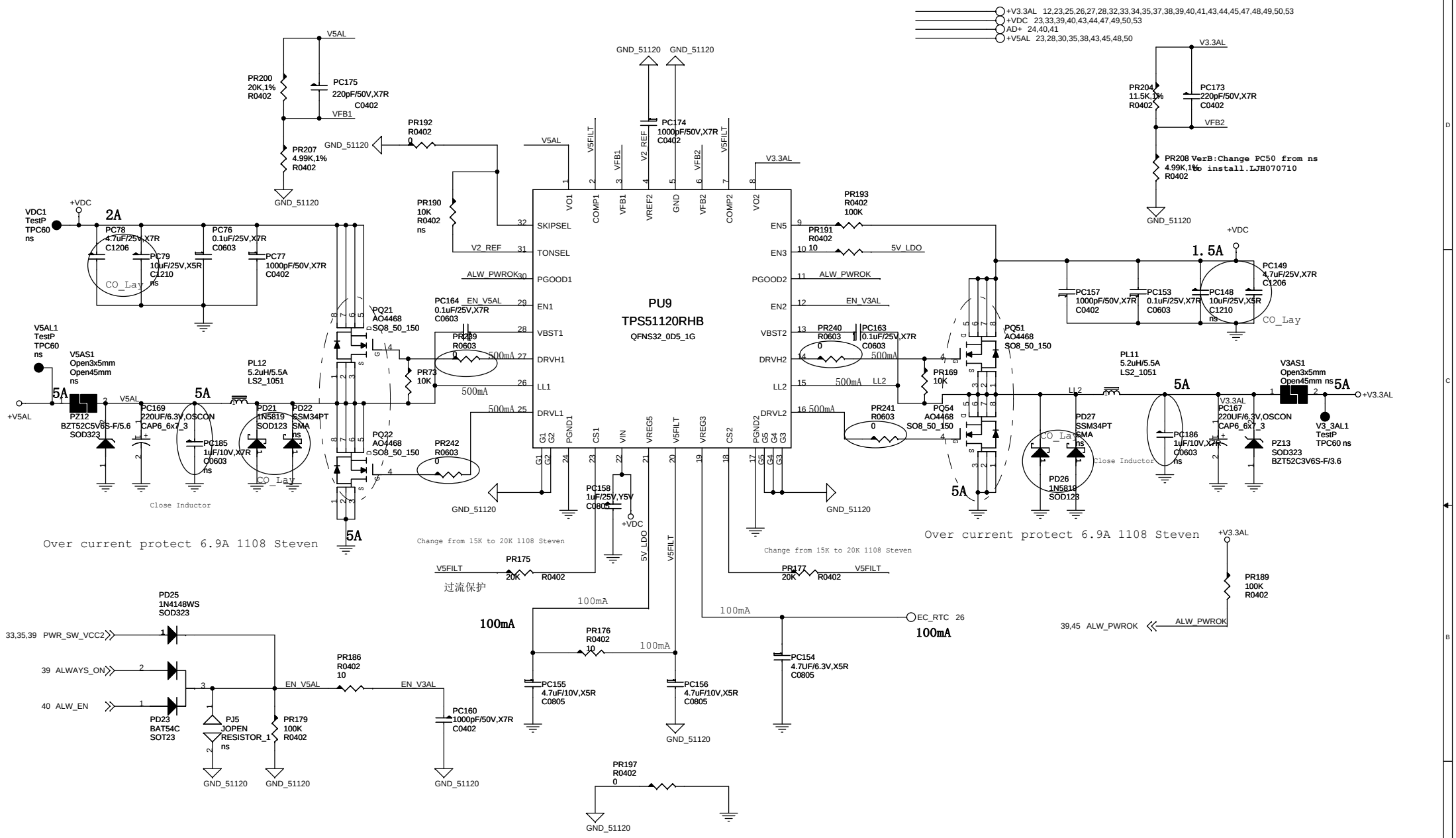


Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	ADAPTER IN	
Size A3	Project Name M42P	Rev B
Date: Tuesday, February 26, 2008	Sheet 40 of 58	



Delete reserve

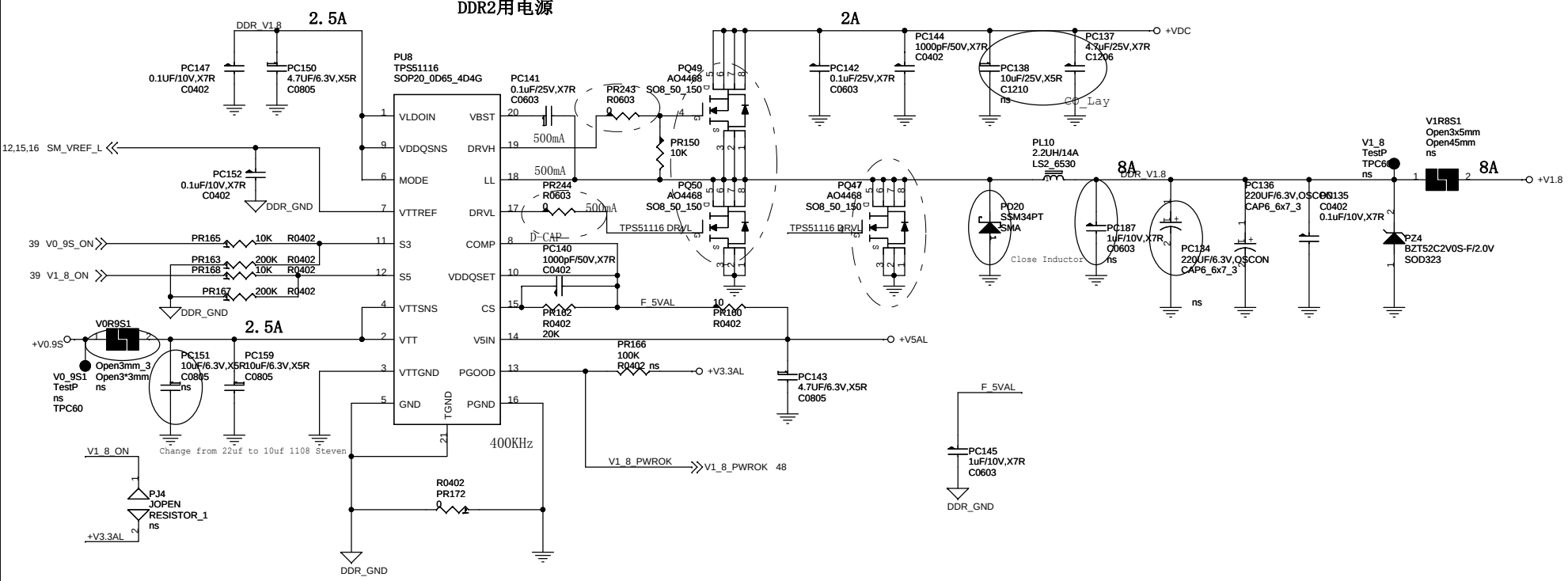
Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	BATTERY IN	
Size A3	Project Name M42P	Rev B
Date: Tuesday, February 26, 2008	Sheet 41 of 58	



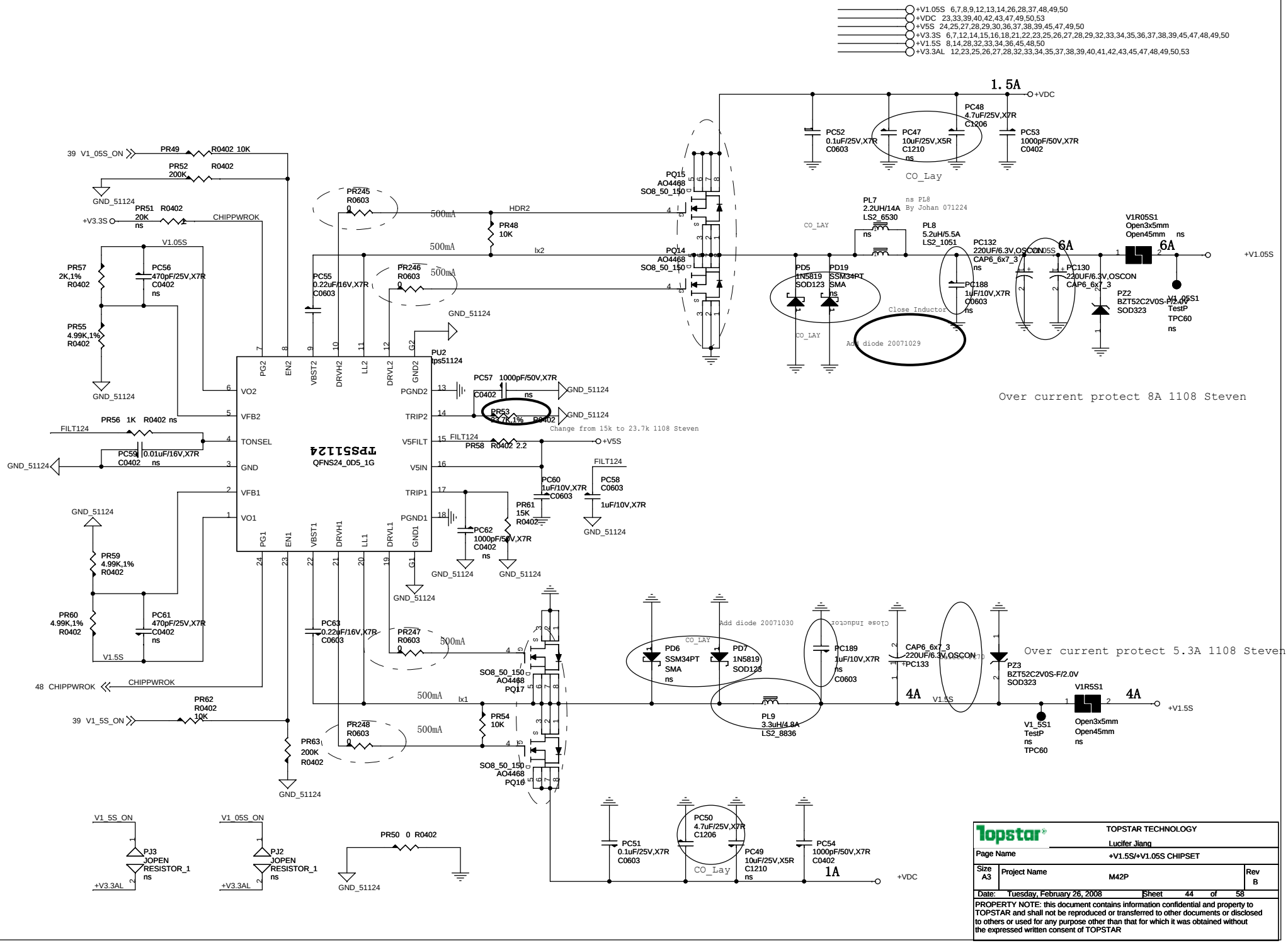
Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	+V3.3AL/+V5AL/+V1.5AL	
Size A3	Project Name M42P	Rev B
Date: Tuesday, February 26, 2008	Sheet 42 of 58	

+V0.9S 17,45,50
+V5AL 23,28,30,35,38,42,45,48,50
+V3.3AL 12,23,25,26,27,28,32,33,34,35,37,38,39,40,41,42,44,45,47,48,49,50,53
+VDC 23,33,39,40,42,44,47,49,50,53
+V1.8 12,13,14,15,16,45,48,50

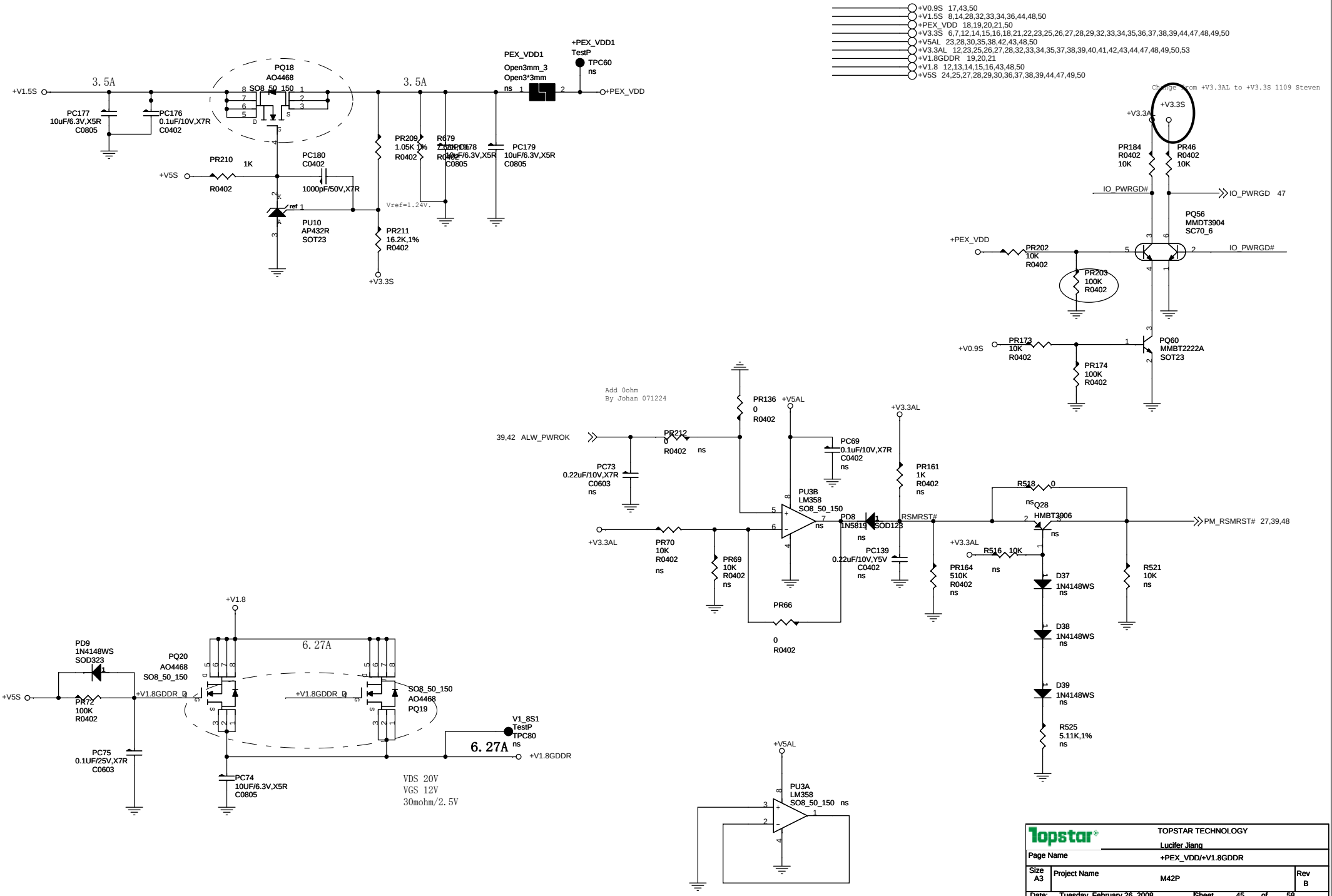
DDR2用电源



Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	+V1.8/+V0.9S DDR	
Size A3	Project Name M42P	Rev B
Date: Tuesday, February 26, 2008	Sheet 43 of 58	



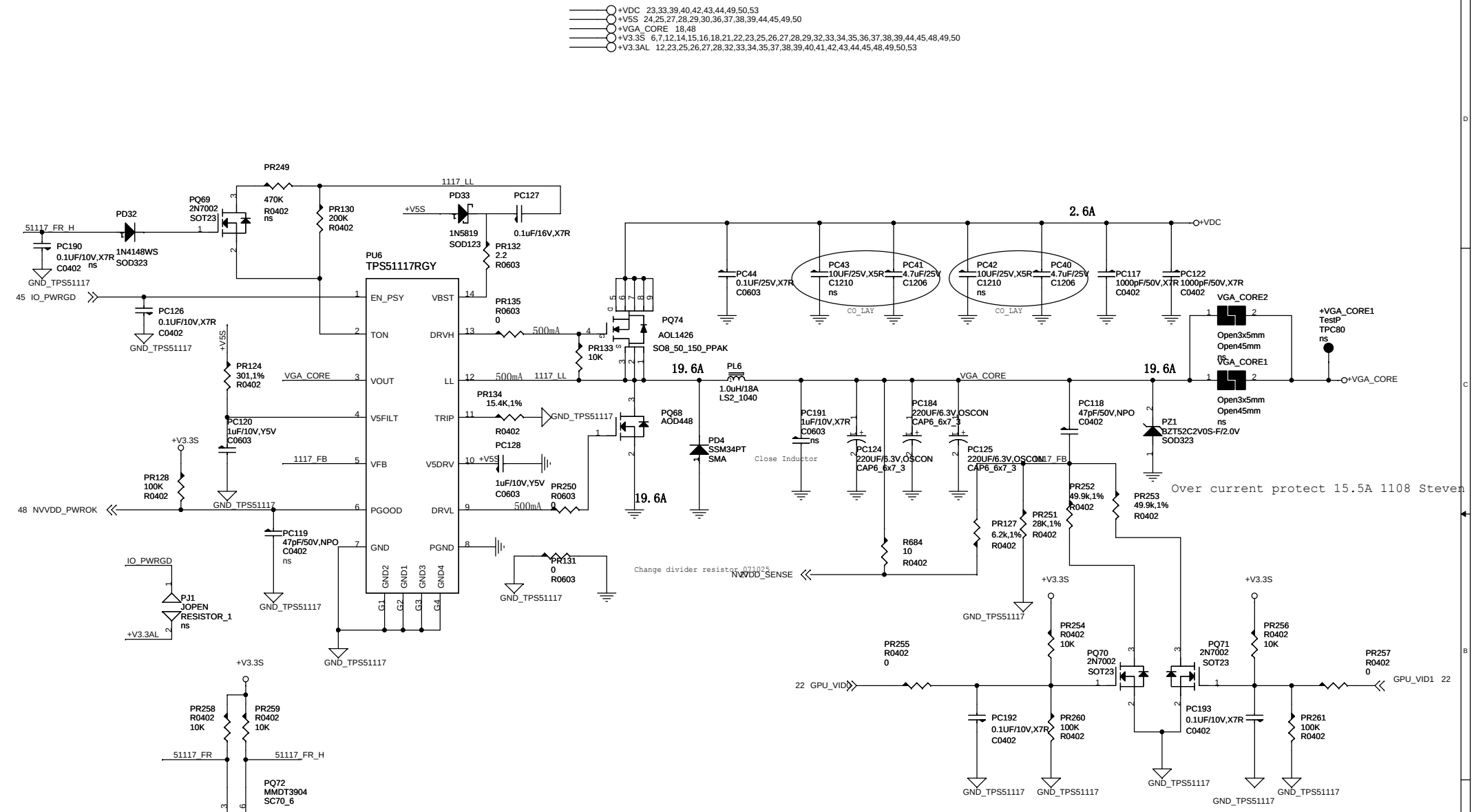
Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	+V1.5S/+V1.05S CHIPSET	
Size A3	Project Name M42P	Rev B
Date: Tuesday, February 26, 2008	Sheet 44 of 58	



Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	+PEX_VDD/+V1.8GDDR	
Size A3	Project Name M42P	Rev B
Date: Tuesday, February 26, 2008	Sheet 45 of 58	

del 6263 circuit,070428

Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	BLANK	
Size B	Project Name M42P	Rev B
Date: Tuesday, February 26, 2008	Sheet 46 of 58	

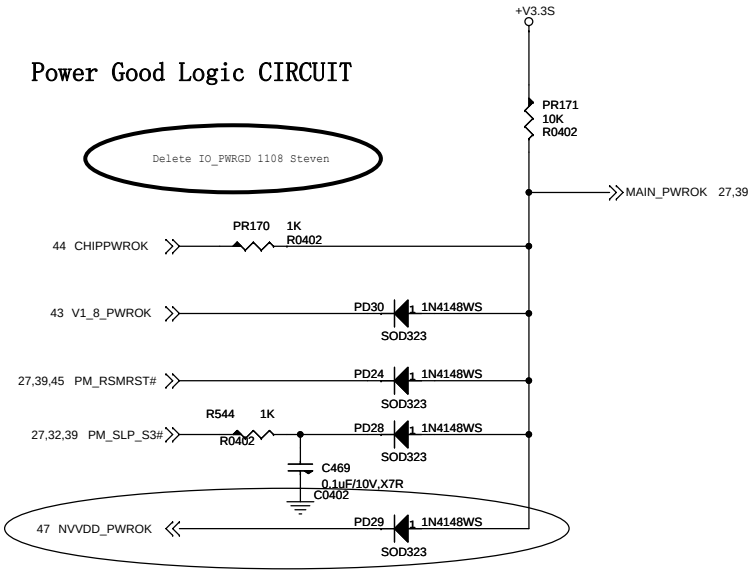


GPI05	GPI06	Frequency	P_STATE	+VGA_CORE
LOW	LOW	350K	MAX BATTERY	0.920V
LOW	HIGH	350K	SD DVD	1.015V
HIGH	LOW	350K	HD DVD	1.015V
HIGH	HIGH	500K	MAX PERF	1.110V

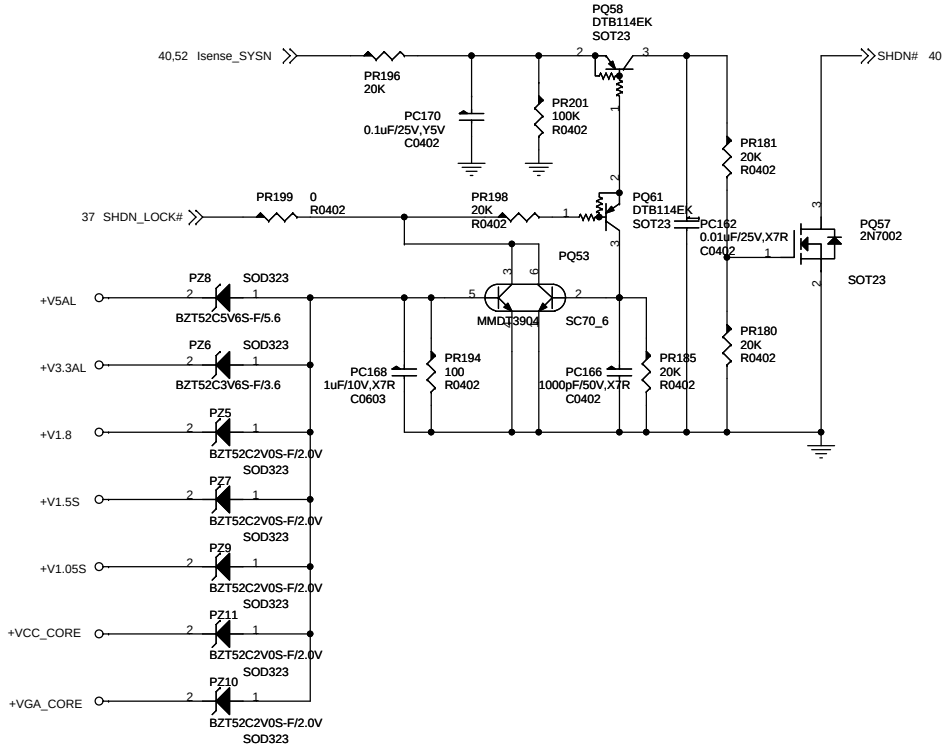
Topstar	TOPSTAR TECHNOLOGY
	Lucifer Jiang
Page Name	NB8M GRAPHICS VCORE POWER
Size A3 / Project Name	M42P / Rev B
Date: Tuesday, February 26, 2008	Sheet 47 of 58

+V3.3S 6,7,12,14,15,16,18,21,22,23,25,26,27,28,29,32,33,34,35,36,37,38,39,44,45,47,49,50
+V5AL 23,28,30,35,38,42,43,45,50
+V3.3AL 12,23,25,26,27,28,32,33,34,35,37,38,39,40,41,42,43,44,45,47,49,50,53
+V1.05S 6,7,8,9,12,13,14,26,28,37,44,49,50
+V1.5S 8,14,28,32,33,34,36,44,45,50
+VCC_CORE 8,49
+V1.8 12,13,14,15,16,43,45,50
AD+ 24,40,41
+VGA_CORE 18,47

Power Good Logic CIRCUIT



OVP CIRCUIT



Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	Power Good Logic/OVP	
Size A3	Project Name M42P	Rev B
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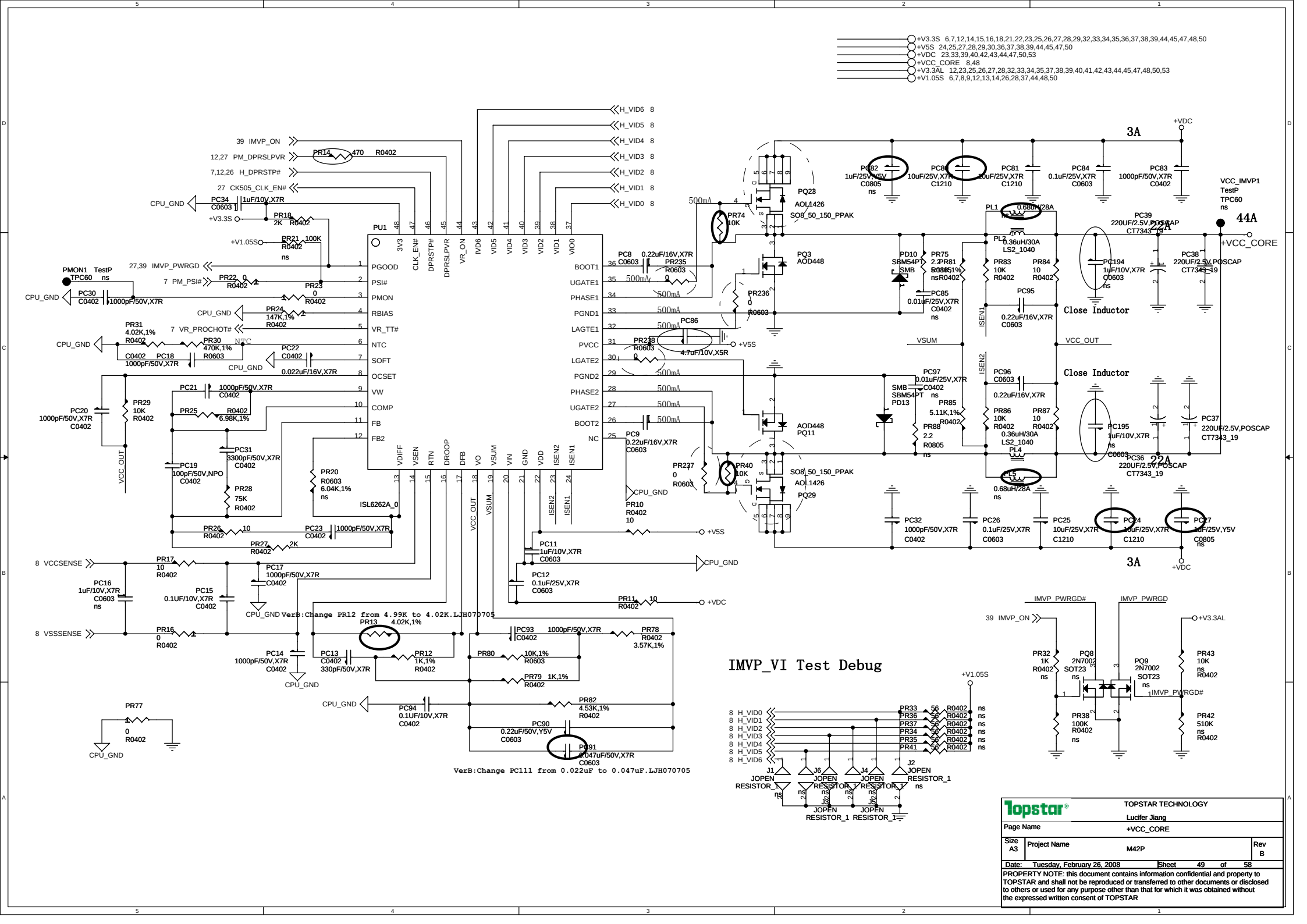
+V3.3S 6,7,12,14,15,16,18,21,22,23,25,26,27,28,29,32,33,34,35,36,37,38,39,44,45,47,48,50
+V5S 24,25,27,28,29,30,36,37,38,39,44,45,47,50
+VDC 23,33,39,40,42,43,44,47,50,53
+VCC_CORE 8,48
+V3.3AL 12,23,25,26,27,28,32,33,34,35,37,38,39,40,41,42,43,44,45,47,48,50,53
+V1.05S 6,7,8,9,12,13,14,26,28,37,44,48,50
PU1
ISL6262A_0
VerB:Change PR12 from 4.99K to 4.02K.LJH070705
VerB:Change PC111 from 0.022uF to 0.047uF.LJH070705
IMVP_VI Test Debug
Close Inductor
TOPSTAR TECHNOLOGY
Lucifer Jiang
Page Name +VCC_CORE
Size A3
Project Name M42P
Rev B
Date: Tuesday, February 26, 2008
Sheet 49 of 58
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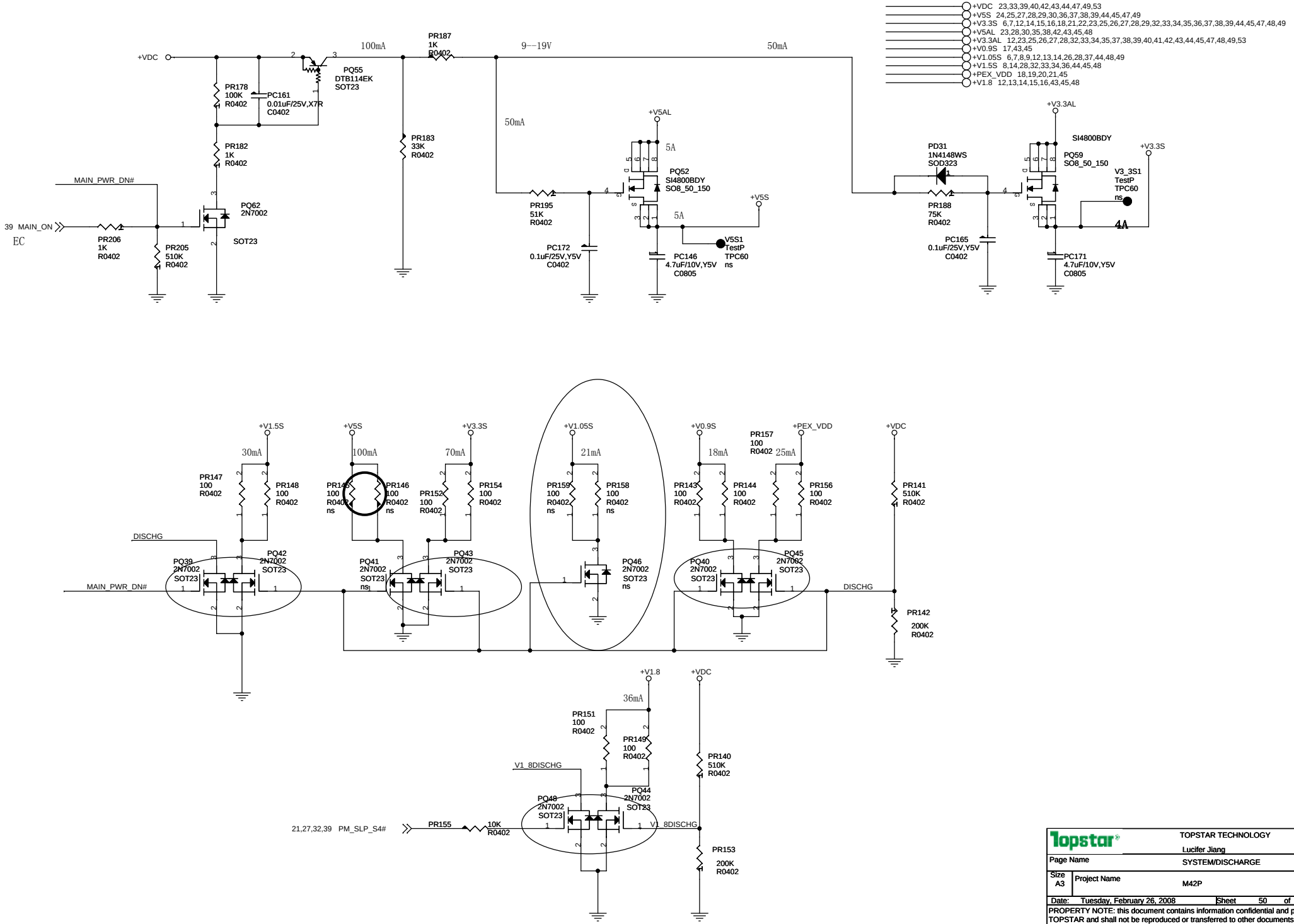

Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	SYSTEM/DISCHARGE	
Size A3	Project Name M42P	Rev B
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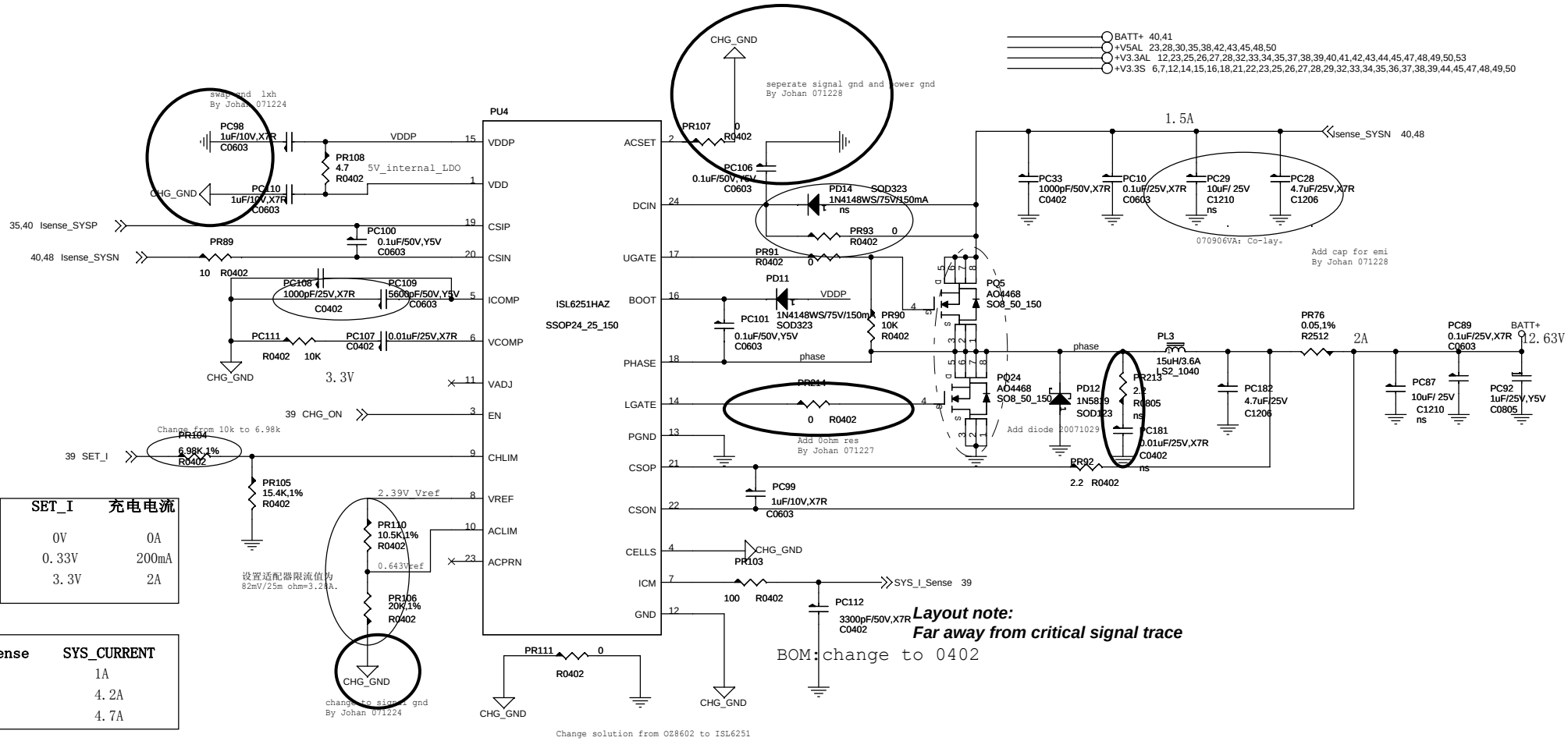
Topstar	TOPSTAR TECHNOLOGY Lucifer Jiang		
Page Name	SYS_I_Sense		
Size A3	Project Name	M42P	Rev B
Date: Tuesday, February 26, 2008	Sheet 51 of 58		

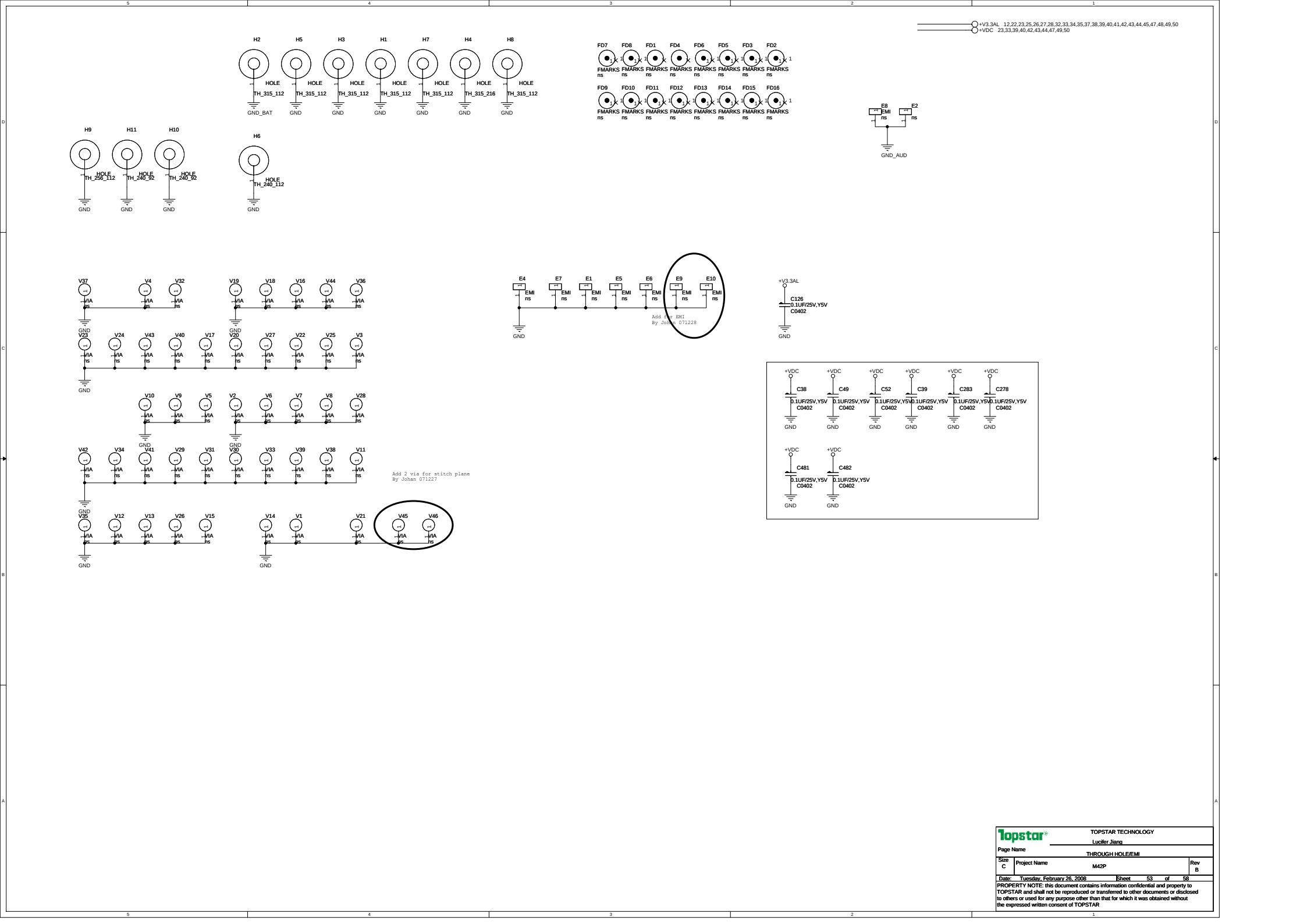


SET_I	充电电流
0V	0A
0.33V	200mA
3.3V	2A

SYS_I_Sense	SYS_CURRENT
400mV	1A
1.67V	4.2A
1.87V	4.7A

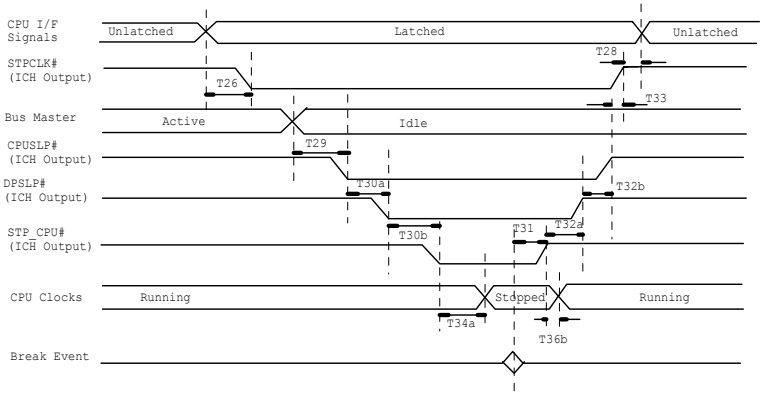
SYS_CURRENT	SYS_I_Sense	SYS_I_Trip
>3.6A	>1.8V	High
<3A	<1.5V	Low

Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	CHARGER	
Size A3	Project Name M42P	Rev B
Date: Tuesday, February 26, 2008	Sheet 52 of 58	

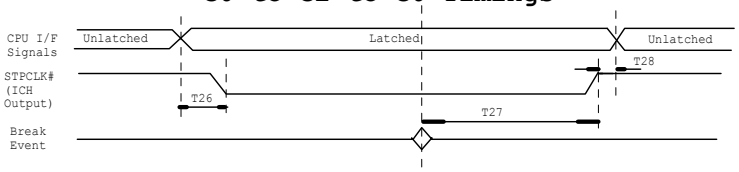


topstar®	TOPSTAR TECHNOLOGY	
Page Name	Lucifer Jiang	
	THROUGH HOLE/EMI	
Size C	Project Name M42P	Rev B
Date: Tuesday, February 26, 2008	Sheet 53 of 58	

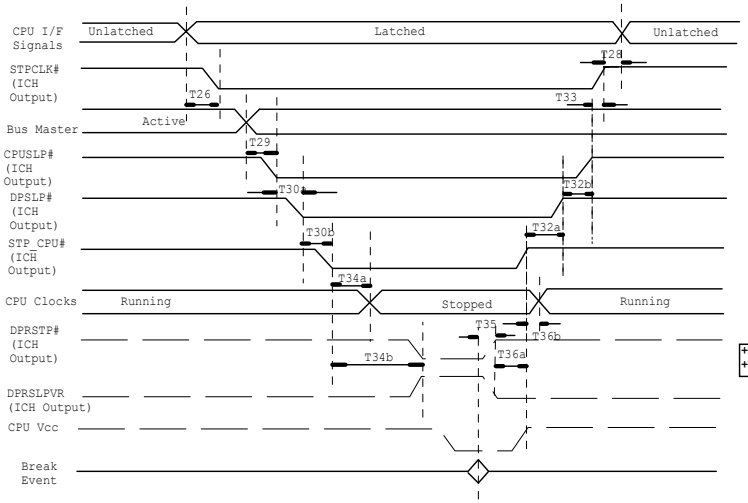
C0 to C3 to C0 Timings



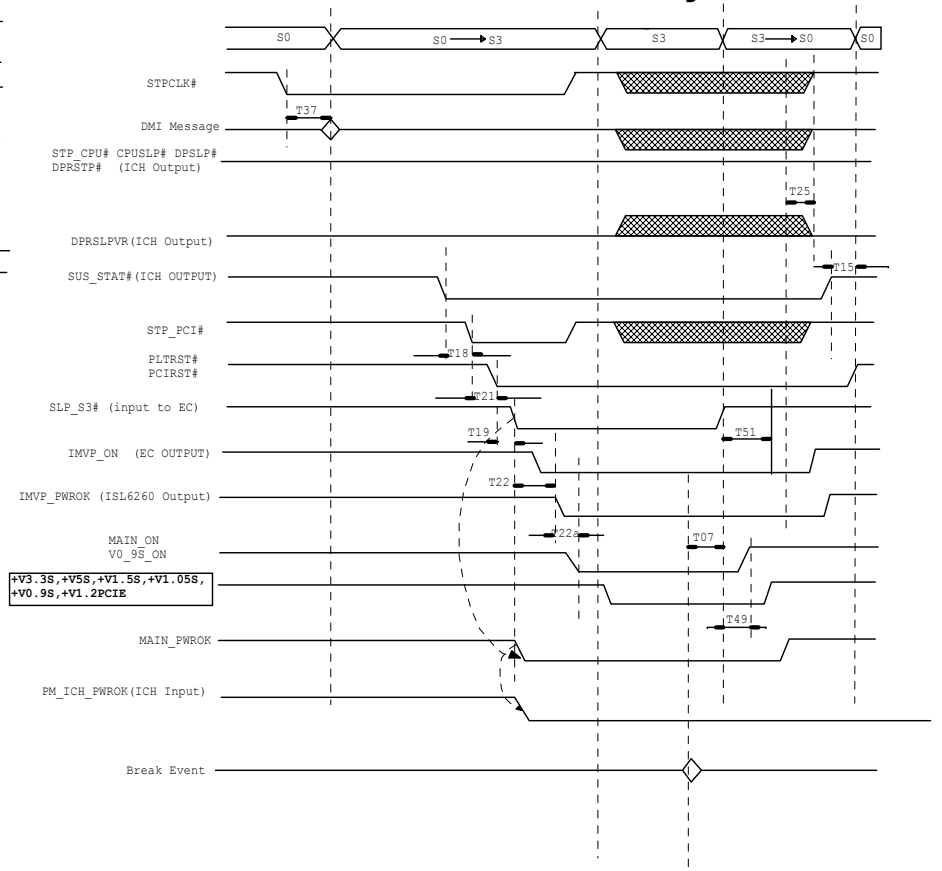
C0 to C2 to C0 Timings



C0 to C4 to C0 Timings

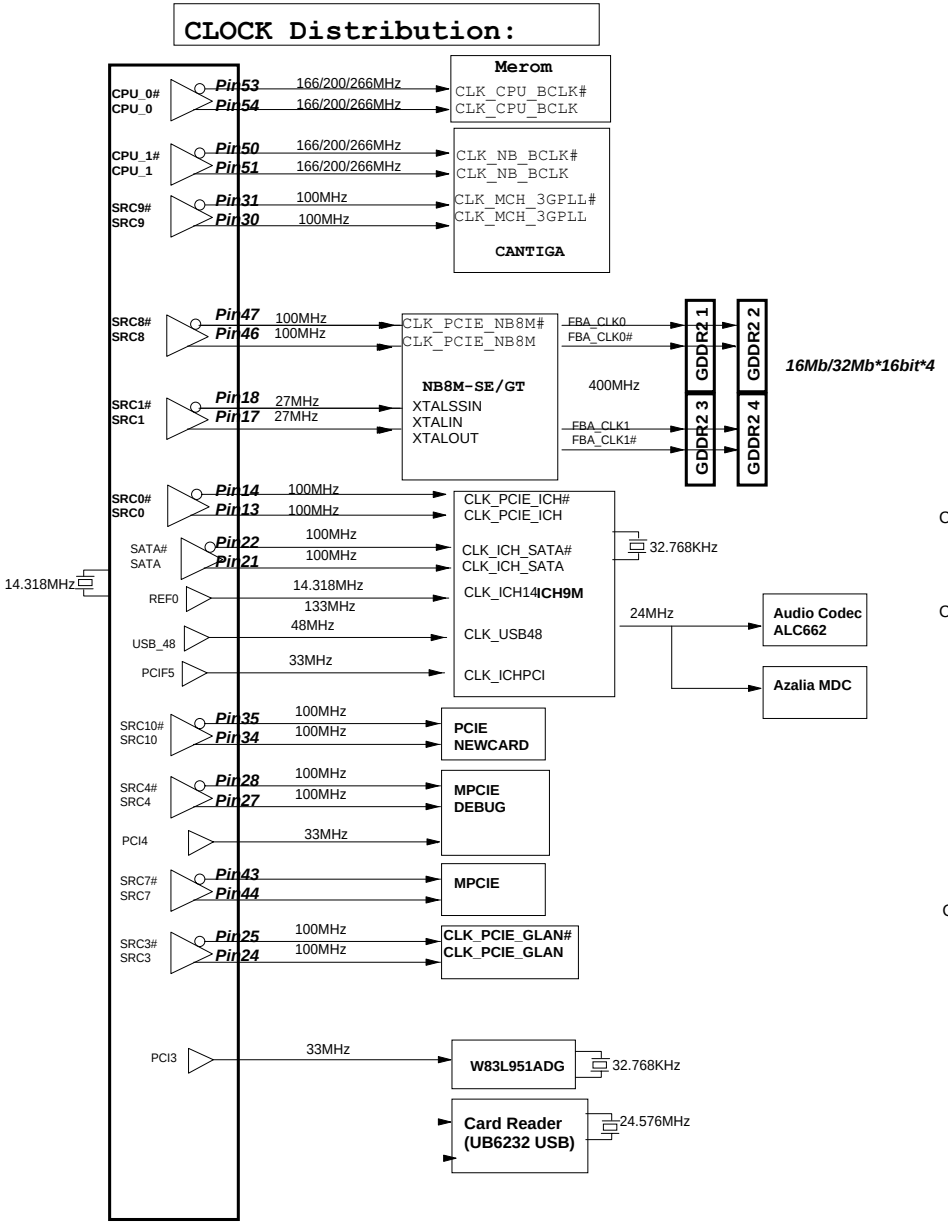


S0 to S3 to S0 Timings

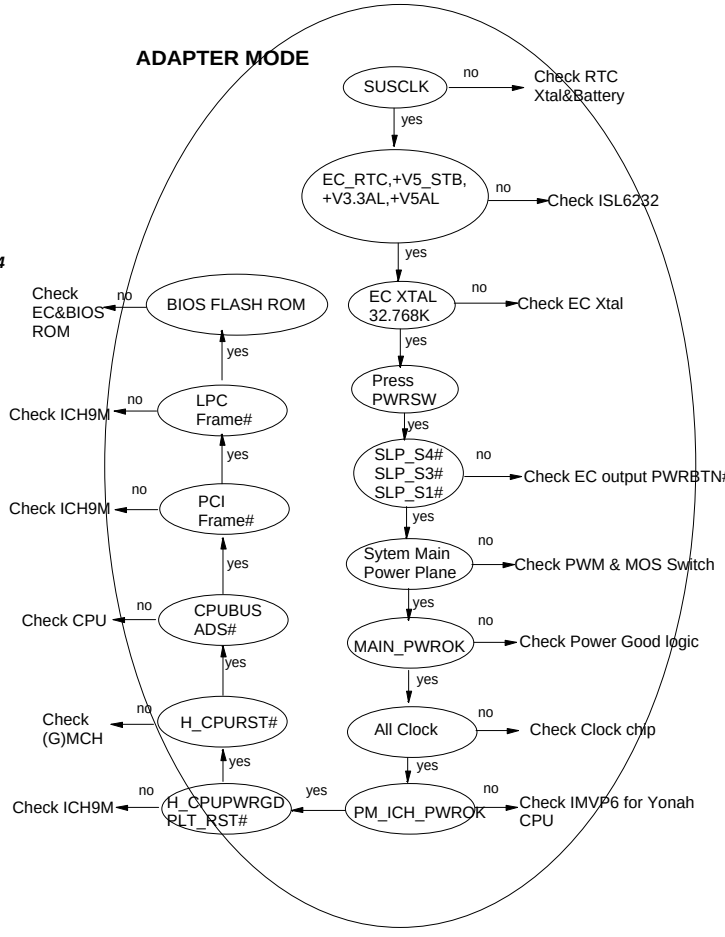


Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	ACPI Mode Switch Timings	
Size B	Project Name M42P	Rev B
Date: Tuesday, February 26, 2008	Sheet 54 of 58	

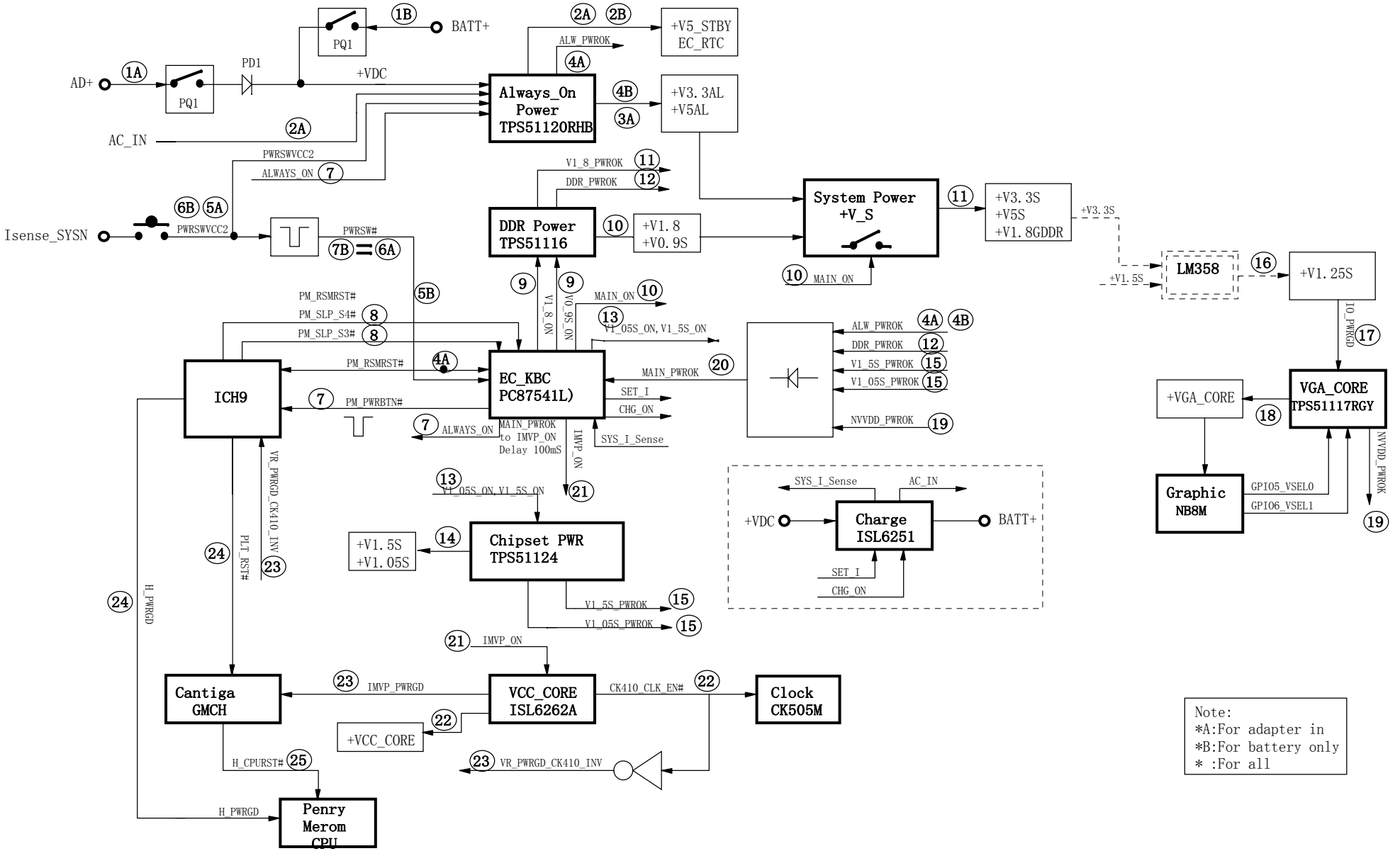
CLOCK Distribution:



CY28548_TSSOP-56P



topstar®	TOPSTAR TECHNOLOGY		
	Lucifer Jiang		
Page Name	Clock Distribution		
Size C	Project Name M42P		Rev B
Date: Tuesday, February 26, 2008	Sheet 55 of 58		



Note:
*A:For adapter in
*B:For battery only
* :For all

Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	THROUGH HOLE/EMI	
Size A3	Project Name M42P	Rev B
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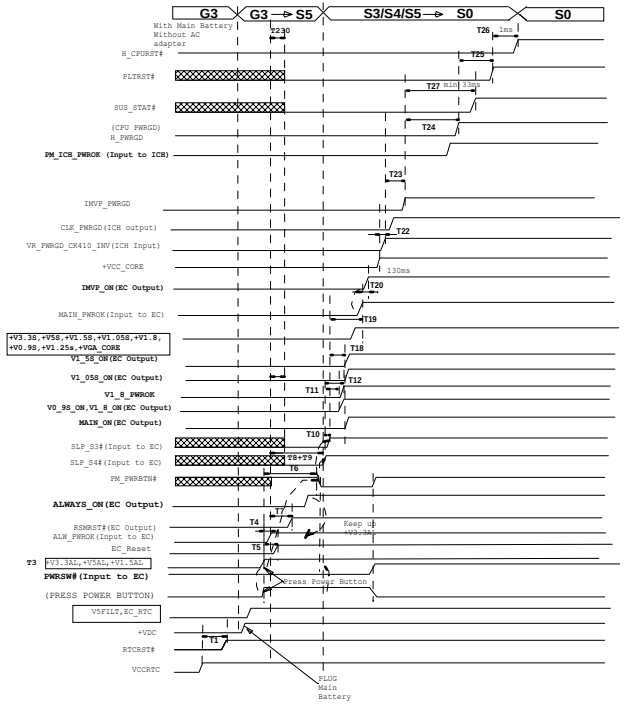
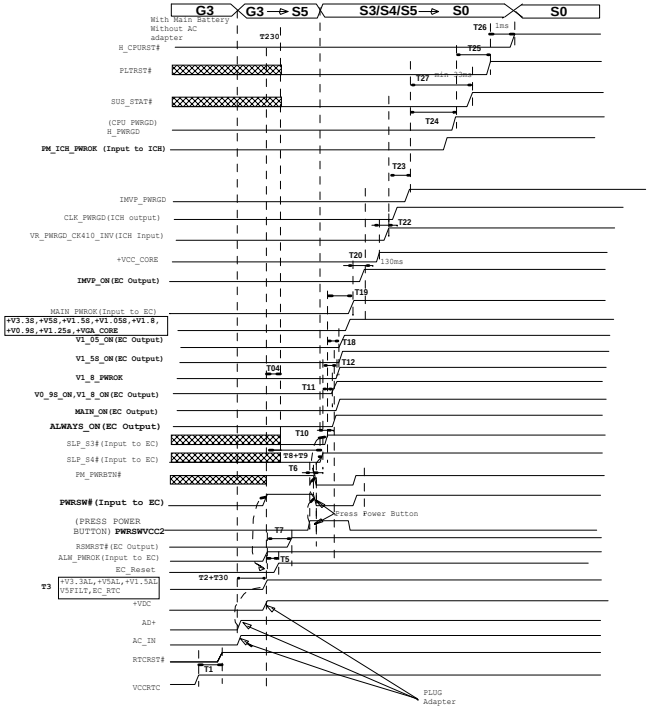
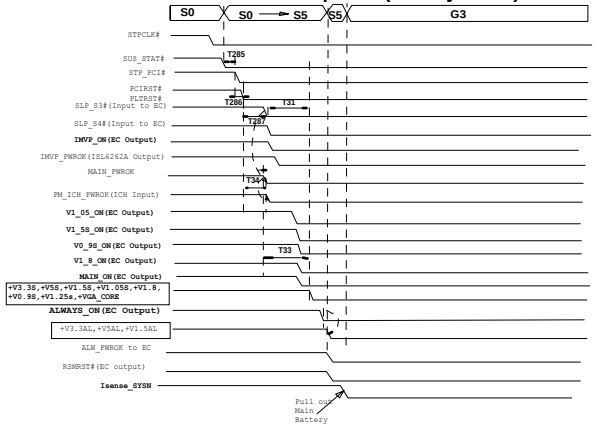
Power On Sequence(Battery mode)



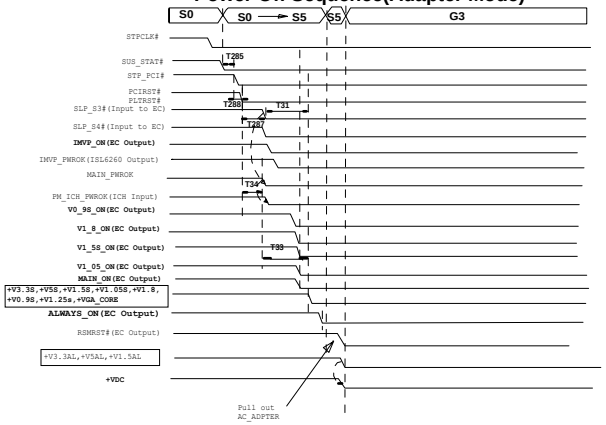
Power On Sequence(Adapter mode)



Power Off Sequence(Battery Mode)



Power Off Sequence(Adapter Mode)



T3 V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0.7 V

Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	Power On/Off Sequence	
Size A2	Project Name M42P	Rev B
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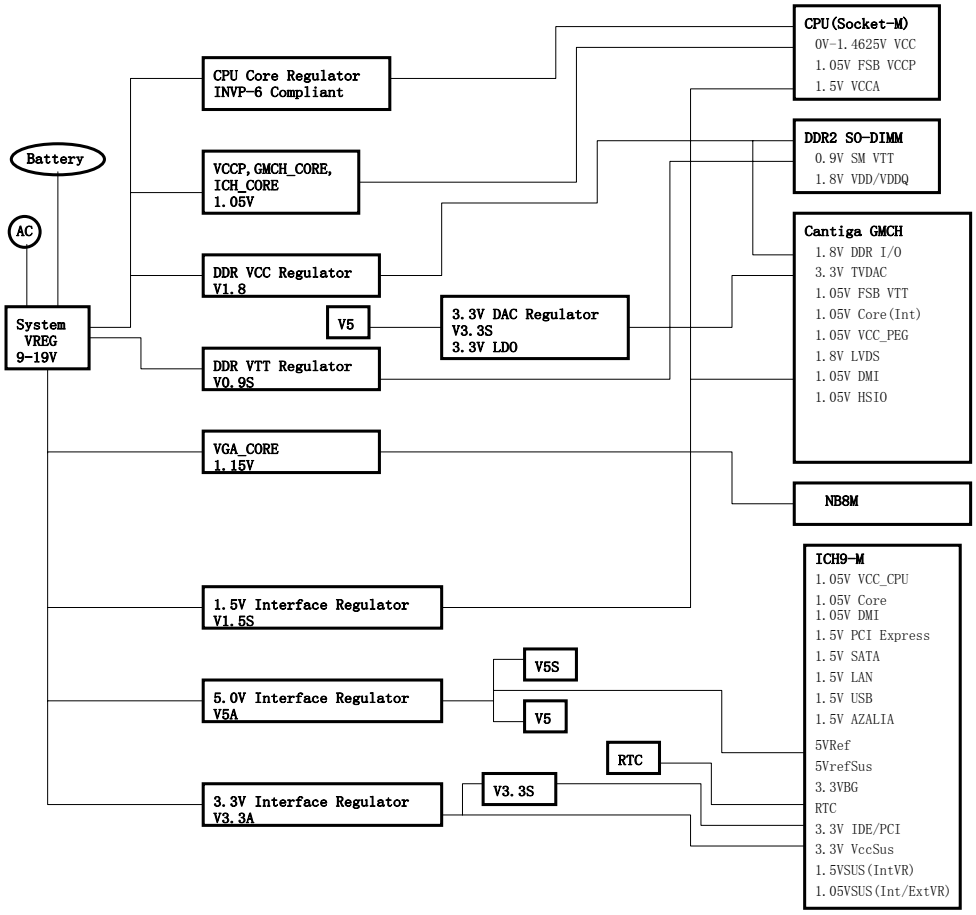
POWER Distribution



R0.92
0V-1.4625V VCC

USB
V5A&V3.3A

SATA
V3.3S&V5S

BLUETOOTH
V3.3S

SPI
V3.3S

LVDS
System VREG(9-12.6V)

CK505-M
V3.3S

SMC/KBC
V3.3A

Azalia
V5,V3.3S

Mini-PCI Express
V1.5S +1.5V
V3.3A +3.3Vaux
V3.3S +3.3V-3.0A

topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	POWER Distribution	
Size C	Project Name M42P	Rev B
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