Topstar Digital technologies Co.,LTD

Board name: MotherBoard Schematic
Project name: M42
Version: VerA
Initial Date: Sep.22, 2007

Topstar Confidential

Hardware drawing by:

Hardware check by:

EMI Check by:

Power drawing by:

Power check by:

Manager Sign by:

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	Lucifer Jiang	
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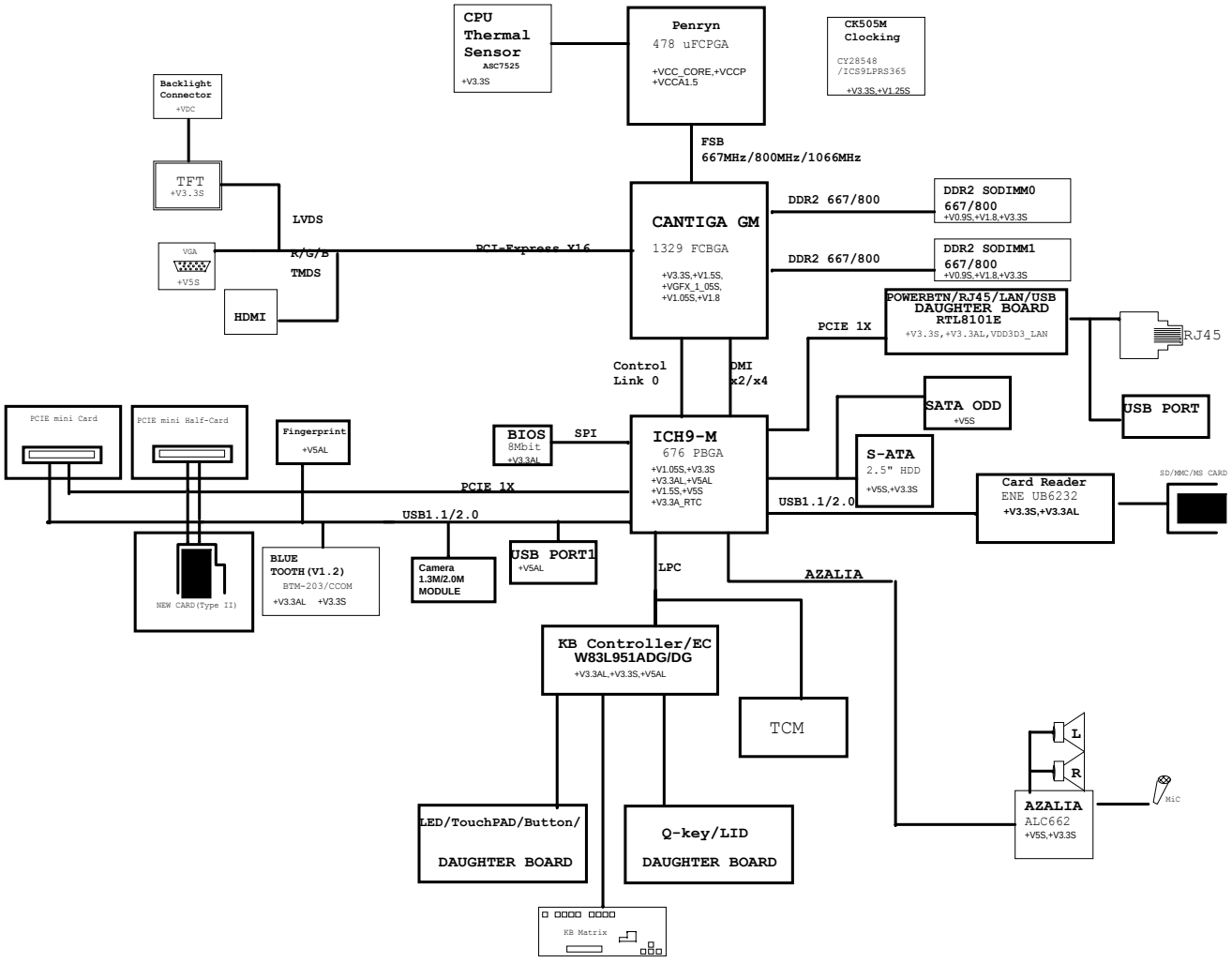
ShenZhen Topstar Industry Co.,LTD

M42G SYSTEM BLOCK Ver:A



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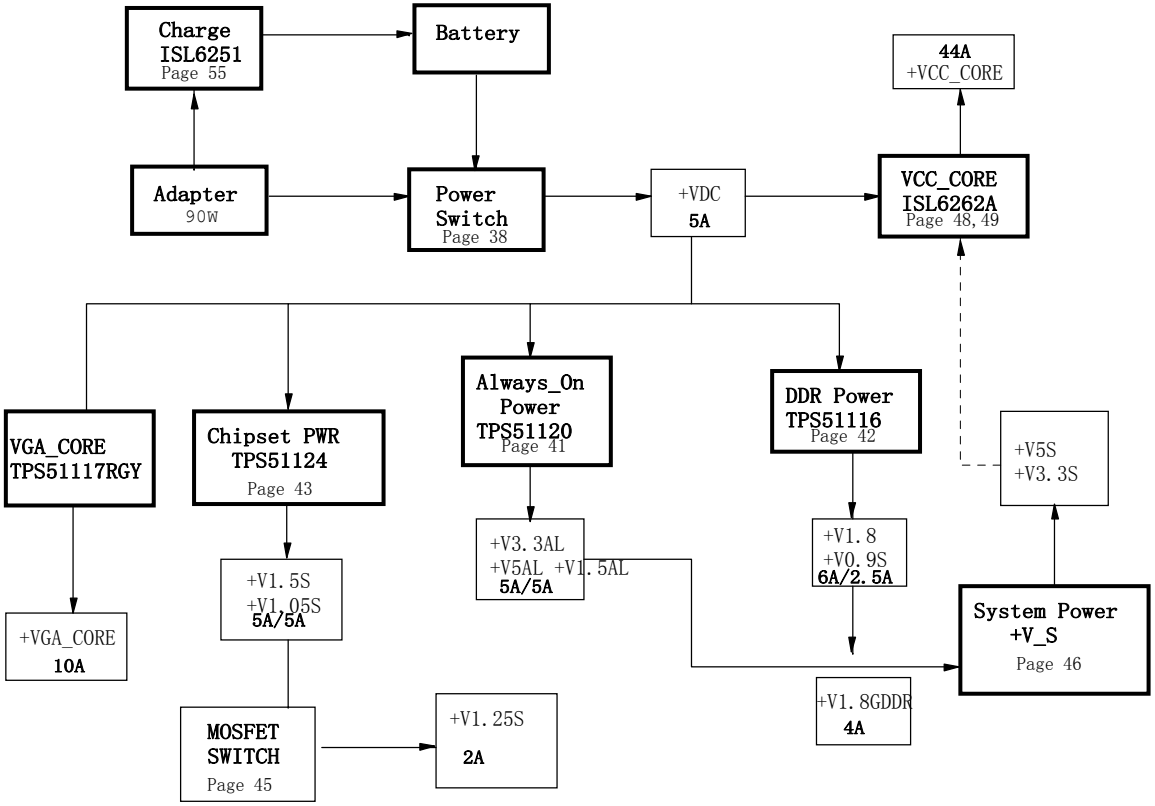
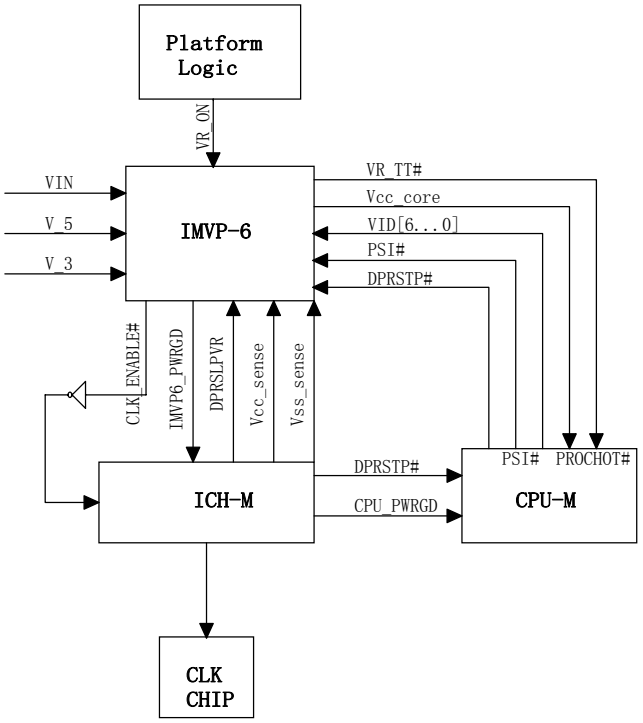
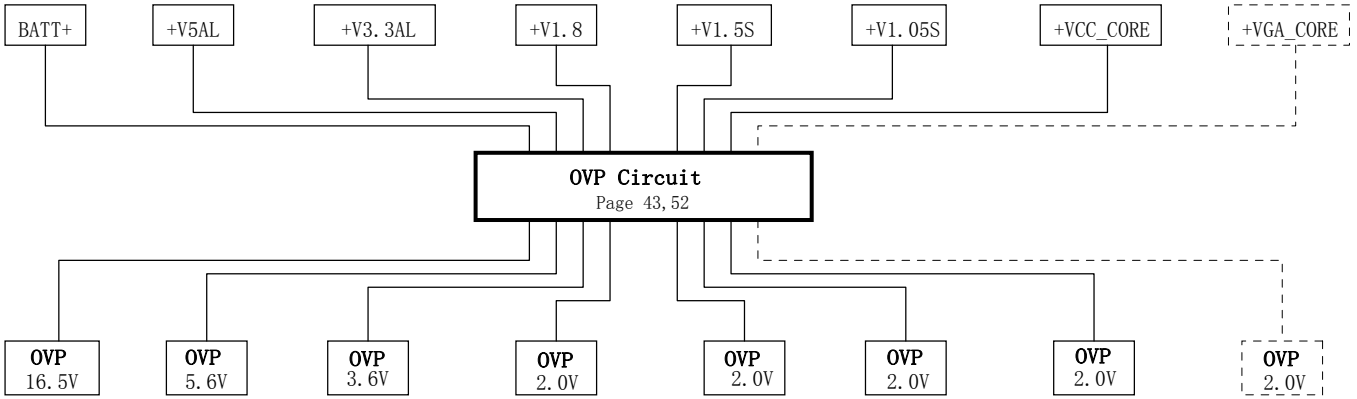
M42 POWER BLOCK Ver:A

注意:

虚线表示电源电压信号。







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Voltage Rails

+VDC	Primary DC system power supply(9V-19V)
+VCC_CORE	Core voltage for processor
+V1.5S	1.5V for CPU PLL
+V1.05S	1.05V for FSB VTT
+V0.9S	0.9V DDR2 Termination voltage
+V1.8	1.8V power rail for DDR2
+V3.3AL	3.3V always on power rail
+V3.3S	3.3V main power rail
+V5AL	5V for USB Device
+V5S	5V main power rail
+VGA_CORE	1.15V for GPU NB8M core voltage
+V1.5AL	1.5AL for HDMI
+V1.8DDR	1.8V for DDR

Board stack up description

PCB Layers	Trace Impedence:55ohm +/-15%(Default)
TOP	
GND	
IN1	
IN2	
VCC	
IN3	
GND	
Bottom	

USB Table

USB Port#	Function Description
0	Express Card
1	RESERVED
2	USB Port(on Main Board)
3	Mini PCIE Card(WLAN & ROBSON)
4	Mini PCIE Card(WLAN & ROBSON)
5	Bluetooth
6	USB Port(on I/O Board)
7	USB CAMERA(On VGA Board)
8	CARD Reader
9	USB Port(on I/O Board)

I2C SMB Address

Device	Address	Hex	Bus	Master
Clock Generator	1101 001x	D2	SMB_ICH_S	ICH9M
SO-DIMM0	1010 000x	A0	SMB_ICH_S	ICH9M
SO-DIMM1	1010 010x	A4	SMB_ICH_S	ICH9M
NEW CARD	Variable	Variable	SMB_ICH_S	ICH9M
PCIE Mini CARD	Variable	Variable	SMB_ICH_S	ICH9M
Smart Battery	0001 011x	16	I2C	W83L951ADG
CPU Thermal Sensor(ASC7525)	1001 100x	98	I2C	W83L951ADG

Power States/AC mode

Signal	SLP_S3#	SLP_S4#	SLP_S5#	+V*AL	+V*	+V*S	Clock
S0(Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(STM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(STD)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(SoftOff)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Wake up Events

LID switch from EC
Power switch from EC

ns: Component marked "ns" is not stuff

This is a lead free project,all component must be LF

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Schematic modify Item and history:

2007-10-26 Ver A initial release

2007-12-28 Ver B release

1 P6 CLK C112 ns change to 18pf stuff for EMC issue
2 P7 Host clk CLK_CPU_BCLK (#) add far end diff termination as DG and intel FAE advised
3 P7 Thermal sensor7525 change to 75393
4 P8 BRACKET1_Mylarchange to bi-side sticky malyer
5 P9 CPU bracket holesupport hold change to esd protection type
6 P22 IFPCD_IOVDD_FBIFPCD_IOVDD_FB add circuit for voltage leakage issue
7 P23 CameraAdd camera_on control circuit
8 P24 CRTC8 C9 C10 ns change to 22p stuff for vga emc issue
9 P25 HDMI EMCAdd common choke for HDMI emc issue
10 P27 spi bootR497 ns to stuff for boot from spi
11 P28 V1.5ALdelete for cost down
12 P32 EP_MYLAR1change as S42
13 P36 MIC1_JDMIC1_JD connect to sense B , reserved route to sense A
14 P36 Audio Jack esdD40 D41 D42 D43 change from bat54s to ESDPAD
15 P39 KBCADG change to DG
16 P39 CrystalDelete 32.768 crystal for no using
17 P39 KBC flashpull down reset# and test# for flash KBC
18 P39 "MCH_TSATN# EC_BKLT_PWM"swap these two pins for association with other cases

Cost Down list

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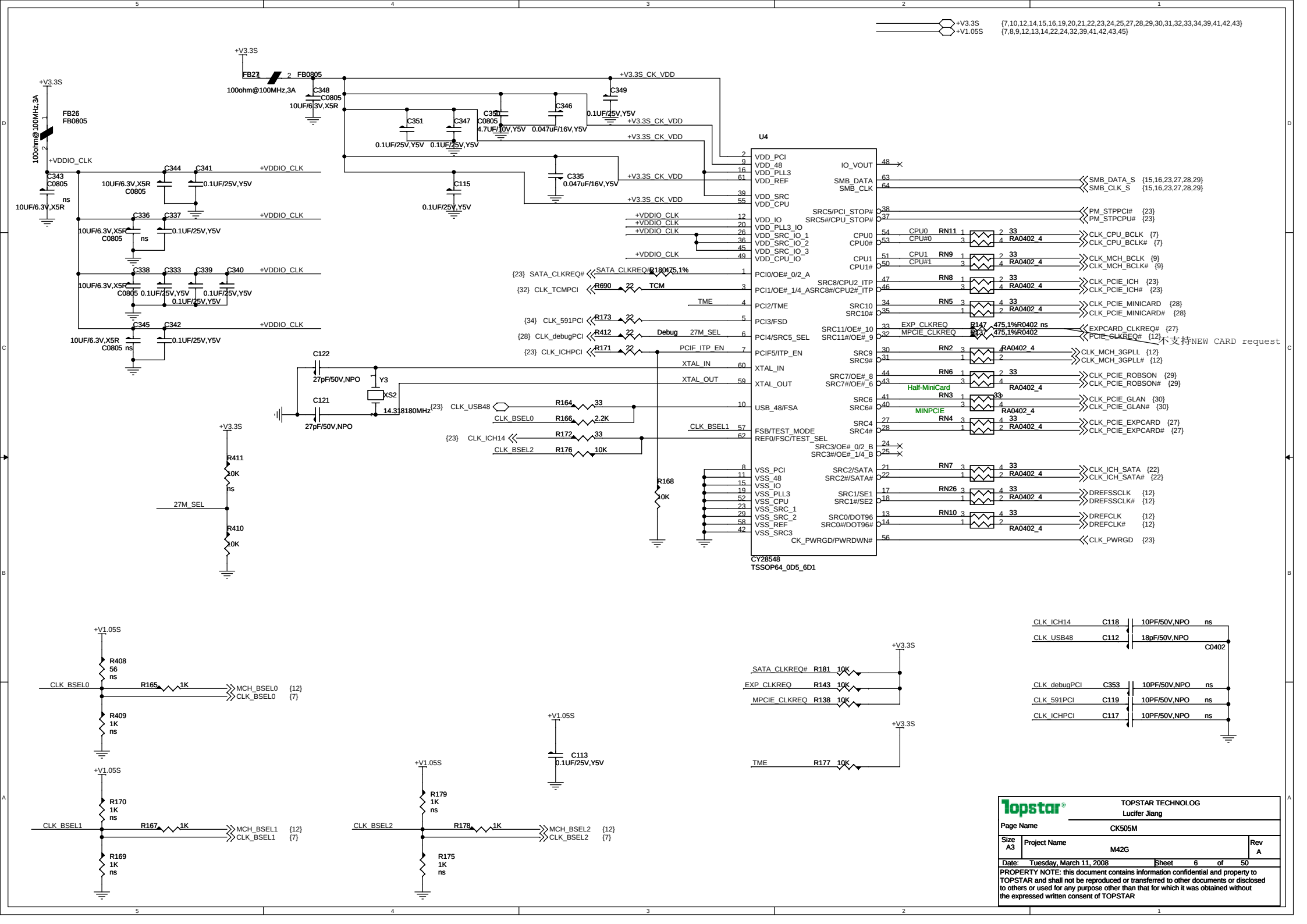
+V3.3S {7,10,12,14,15,16,19,20,21,22,23,24,25,27,28,29,30,31,32,33,34,39,41,42,43}
+V1.05S {7,8,9,12,13,14,22,24,32,39,41,42,43,45}
U4
CY28548
TSSOP64_0D5_6D1
Half-MiniCard
MINPCIE
不支持NEW CARD request
TOPSTAR TECHNOLOG
Lucifer Jiang
Page Name CK505M
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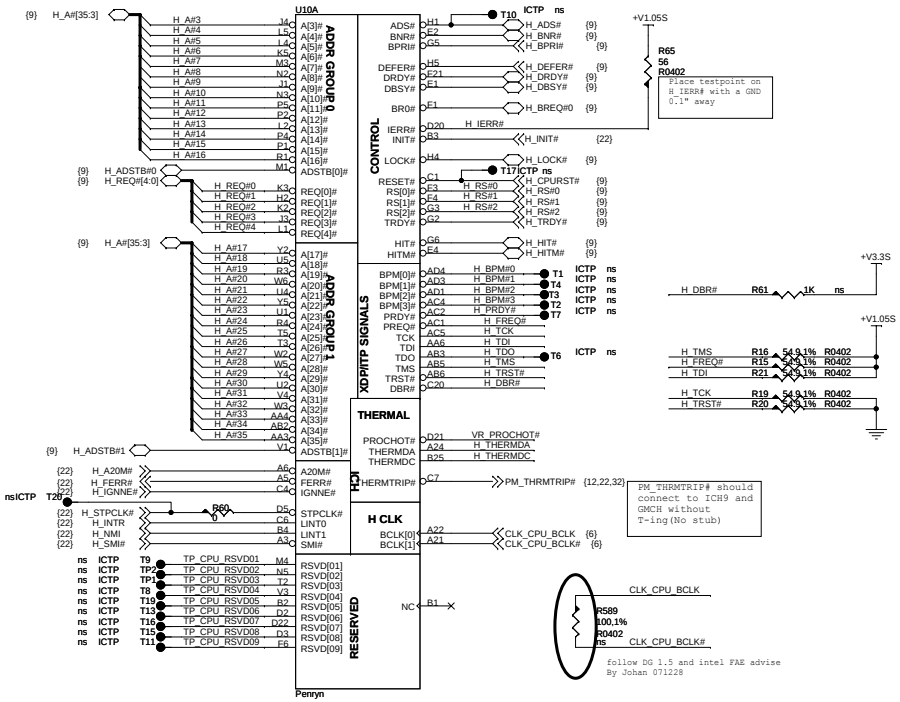

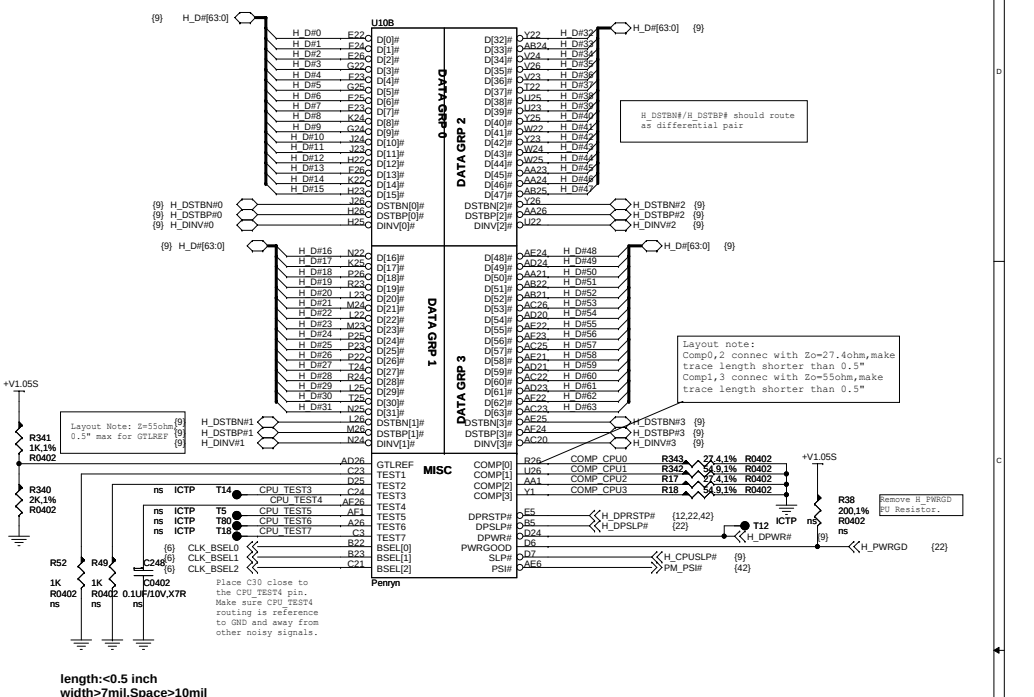

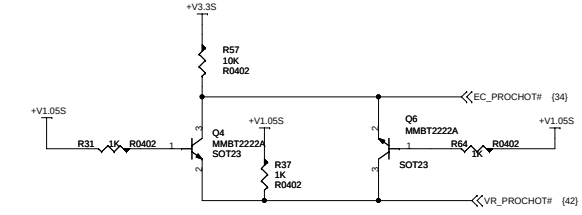

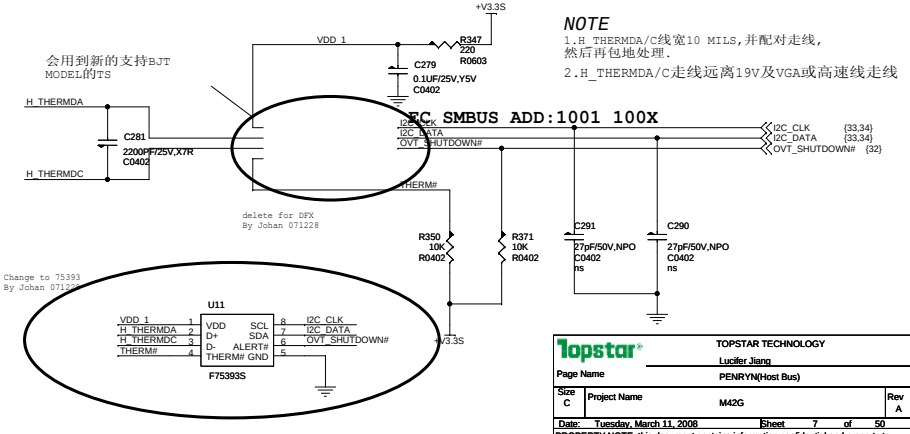

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+VCC_CORE {41,42}
+V1.5S {14,22,24,27,28,29,31,39,41,43}
+V1.05S {6,7,9,12,13,14,22,24,32,39,41,42,43,45}

Demo:22uF*32 3mOhm 0.6nH
Caps

+VCC_CORE
C269 10uF/6.3V,X5R C0805 ns
C270 10uF/6.3V,X5R C0805
C267 10uF/6.3V,X5R C0805
C268 10uF/6.3V,X5R C0805 ns
C266 10uF/6.3V,X5R C0805
C258 10uF/6.3V,X5R C0805 ns
C265 10uF/6.3V,X5R C0805
C43 10uF/6.3V,X5R C0805
C42 10uF/6.3V,X5R C0805
C257 10uF/6.3V,X5R C0805

+VCC_CORE
C22 10uF/6.3V,X5R C0805 ns
C23 10uF/6.3V,X5R C0805
C41 10uF/6.3V,X5R C0805 ns
C40 10uF/6.3V,X5R C0805
C259 10uF/6.3V,X5R C0805 ns
C13 10uF/6.3V,X5R C0805
C14 10uF/6.3V,X5R C0805
C16 10uF/6.3V,X5R C0805
C256 10uF/6.3V,X5R C0805
C251 10uF/6.3V,X5R C0805

+VCC_CORE
C24
C262 10uF/6.3V,X5R C0805
C255 10uF/6.3V,X5R C0805 ns
C252 10uF/6.3V,X5R C0805 ns
C15 10uF/6.3V,X5R C0805
C254 10uF/6.3V,X5R C0805 ns
C261 10uF/6.3V,X5R C0805 ns
C25 10uF/6.3V,X5R C0805 ns
C253 10uF/6.3V,X5R C0805 ns
C260 10uF/6.3V,X5R C0805 ns

+VCC_CORE +VCC_CORE

U10C

A7	VCC[001]	VCC[068]	AB20
A9	VCC[002]	VCC[069]	AB7
A10	VCC[003]	VCC[070]	AC7
A12	VCC[004]	VCC[071]	AC9
A13	VCC[005]	VCC[072]	AC12
A15	VCC[006]	VCC[073]	AC13
A17	VCC[007]	VCC[074]	AC15
A18	VCC[008]	VCC[075]	AC17
A20	VCC[009]	VCC[076]	AC18
B7	VCC[010]	VCC[077]	AD7
B9	VCC[011]	VCC[078]	AD9
B10	VCC[012]	VCC[079]	AD10
B12	VCC[013]	VCC[080]	AD12
B14	VCC[014]	VCC[081]	AD14
B15	VCC[015]	VCC[082]	AD15
B17	VCC[016]	VCC[083]	AD17
B18	VCC[017]	VCC[084]	AD18
B20	VCC[018]	VCC[085]	AE9
C9	VCC[019]	VCC[086]	AE10
C10	VCC[020]	VCC[087]	AE12
C12	VCC[021]	VCC[088]	AE13
C13	VCC[022]	VCC[089]	AE15
C15	VCC[023]	VCC[090]	AE17
C17	VCC[024]	VCC[091]	AE18
C18	VCC[025]	VCC[092]	AE20
D9	VCC[026]	VCC[093]	AF9
D10	VCC[027]	VCC[094]	AF10
D12	VCC[028]	VCC[095]	AF12
D14	VCC[029]	VCC[096]	AF14
D15	VCC[030]	VCC[097]	AF15
D17	VCC[031]	VCC[098]	AF17
D18	VCC[032]	VCC[099]	AF18
E7	VCC[033]	VCC[100]	AF20
E9	VCC[034]		
E10	VCC[035]	VCCP[01]	G21
E12	VCC[036]	VCCP[02]	V6
E13	VCC[037]	VCCP[03]	J6
E15	VCC[038]	VCCP[04]	K6
E17	VCC[039]	VCCP[05]	M6
E18	VCC[040]	VCCP[06]	J21
E20	VCC[041]	VCCP[07]	K21
F7	VCC[042]	VCCP[08]	M21
F9	VCC[043]	VCCP[09]	N21
F10	VCC[044]	VCCP[10]	N6
F12	VCC[045]	VCCP[11]	R21
F14	VCC[046]	VCCP[12]	R6
F15	VCC[047]	VCCP[13]	T21
F17	VCC[048]	VCCP[14]	T6
F18	VCC[049]	VCCP[15]	V21
F20	VCC[050]	VCCP[16]	W21
AA7	VCC[051]		
AA9	VCC[052]	VCCA[01]	B26
AA10	VCC[053]	VCCA[02]	C26
AA12	VCC[054]		
AA13	VCC[055]	VID[0]	AD6
AA15	VCC[056]	VID[1]	AE5
AA17	VCC[057]	VID[2]	AE5
AA18	VCC[058]	VID[3]	AE4
AA20	VCC[059]	VID[4]	AE3
AB9	VCC[060]	VID[5]	AE3
AC10	VCC[061]	VID[6]	AE2
AB10	VCC[062]		
AB12	VCC[063]		
AB14	VCC[064]	VCCSENSE	AF7
AB15	VCC[065]		
AB17	VCC[066]		
AB18	VCC[067]	VSSSENSE	AF7

Penryn

+V1.05S
C17 10uF/6.3V,X5R C0805
C21 10uF/6.3V,X5R C0805
C33 10uF/6.3V,X5R C0805
+V1.5S
+VCCA_PROC
C272 0.01uF/16V,X7R C0402
Place near PIN B26
R345 0 R0603
C274 10uF/6.3V,X5R C0805

H_VID0 {42}
H_VID1 {42}
H_VID2 {42}
H_VID3 {42}
H_VID4 {42}
H_VID5 {42}
H_VID6 {42}

+VCC_CORE
R338 100,1% R0402
VCCSENSE {42}
VSSSENSE {42}
R339 100,1% R0402

VCC_Sense/VSS-Sense lines between the Penryn processor and the VR should have a trace width of 18 mils on 7-mil spacing, with trace impedance of Zo=27.4 Ω. The VCC_Sense/VSS-Sense should be length matched to within 25 mils.

+V1.05S
C34 0.1UF/10V,X7R C0402
C20 0.1UF/10V,X7R C0402
C18 0.1UF/10V,X7R C0402
C27 0.1UF/10V,X7R C0402
C31 0.1UF/10V,X7R C0402
C19 0.1UF/10V,X7R C0402

BRACKET
CPU_BRACKET
BRACKET1_Mylar
Mylar
change to bi-sticky Mylar
By Johan 071224
Change to ESD discharge point
By Johan 071224

HCPU1 HCPU2 HCPU3 HCPU4
CPU_HOLE ns

Note : using ESD prtection Hole

U10D

A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AE2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE11
K26	VSS[068]	VSS[149]	AE14
L3	VSS[069]	VSS[150]	AE16
L6	VSS[070]	VSS[151]	AE19
L21	VSS[071]	VSS[152]	AF23
L24	VSS[072]	VSS[153]	AF26
M2	VSS[073]	VSS[154]	A2
M5	VSS[074]	VSS[155]	AF6
M22	VSS[075]	VSS[156]	AF8
M25	VSS[076]	VSS[157]	AF11
N1	VSS[077]	VSS[158]	AF13
N4	VSS[078]	VSS[159]	AF16
N23	VSS[079]	VSS[160]	AF19
N26	VSS[080]	VSS[161]	AF21
P3	VSS[081]	VSS[162]	A25
		VSS[163]	AF25

Penryn

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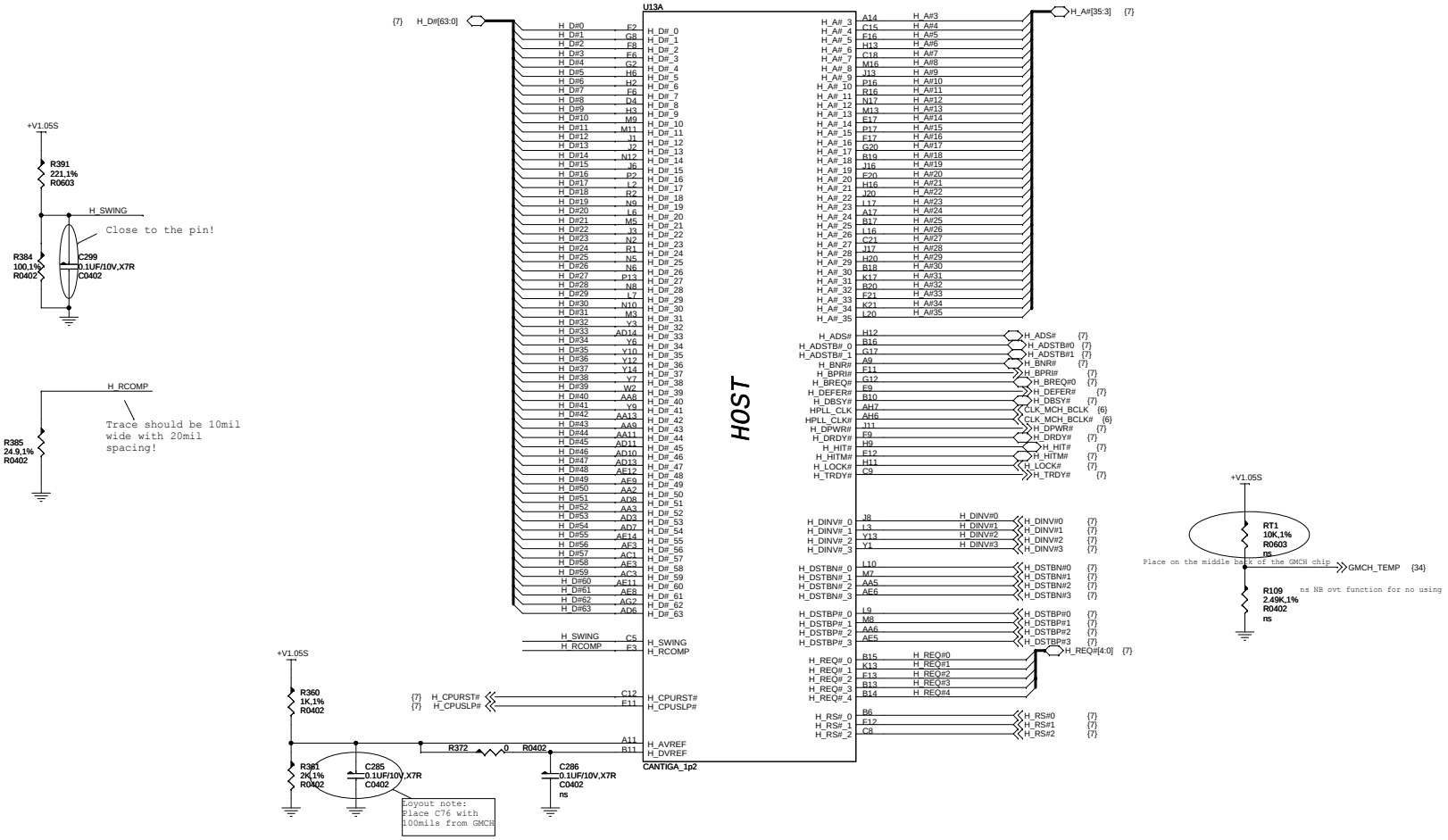

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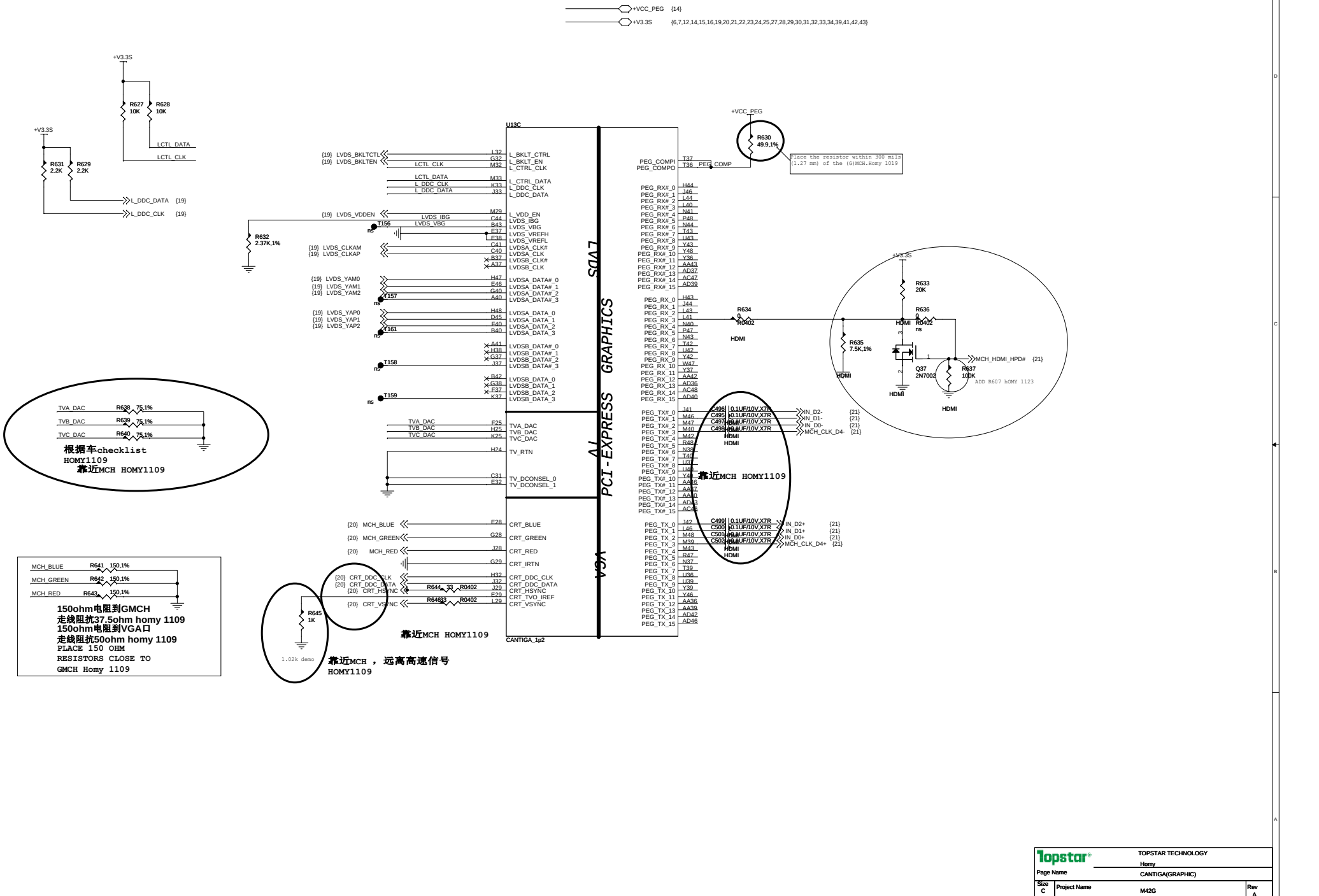

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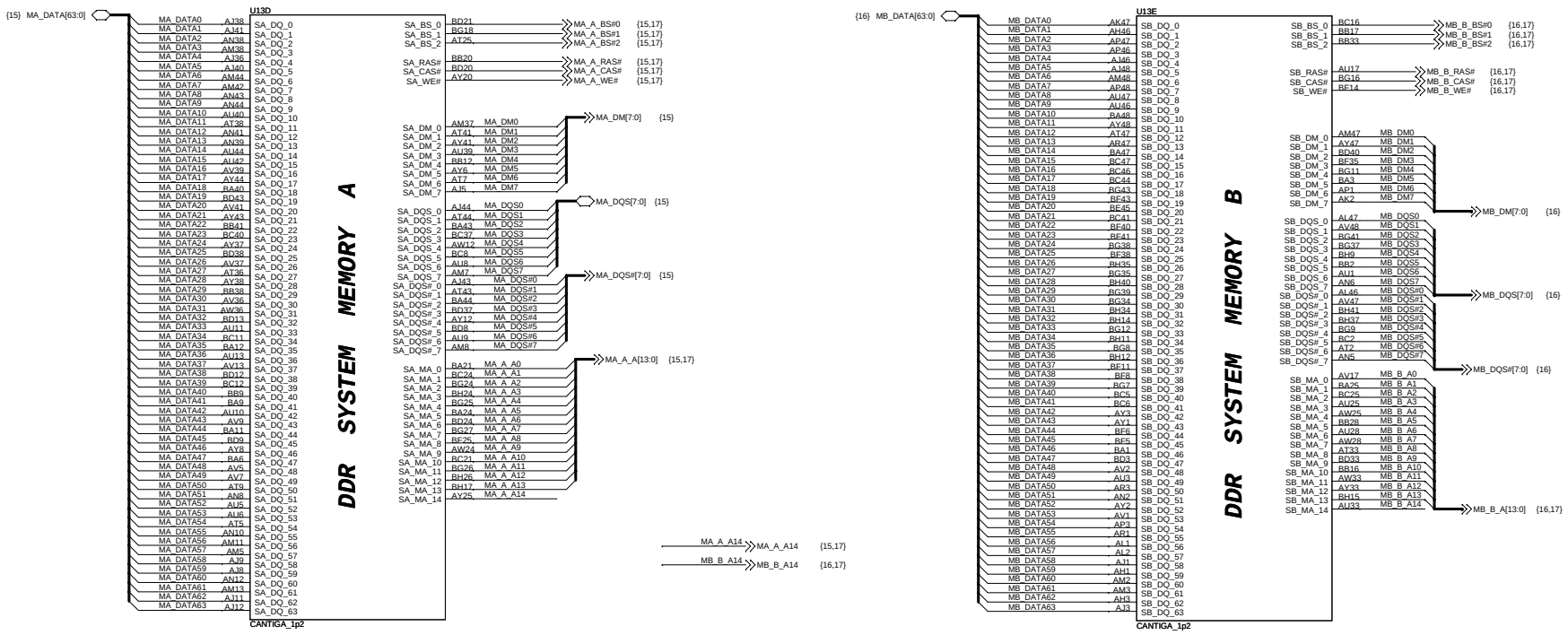

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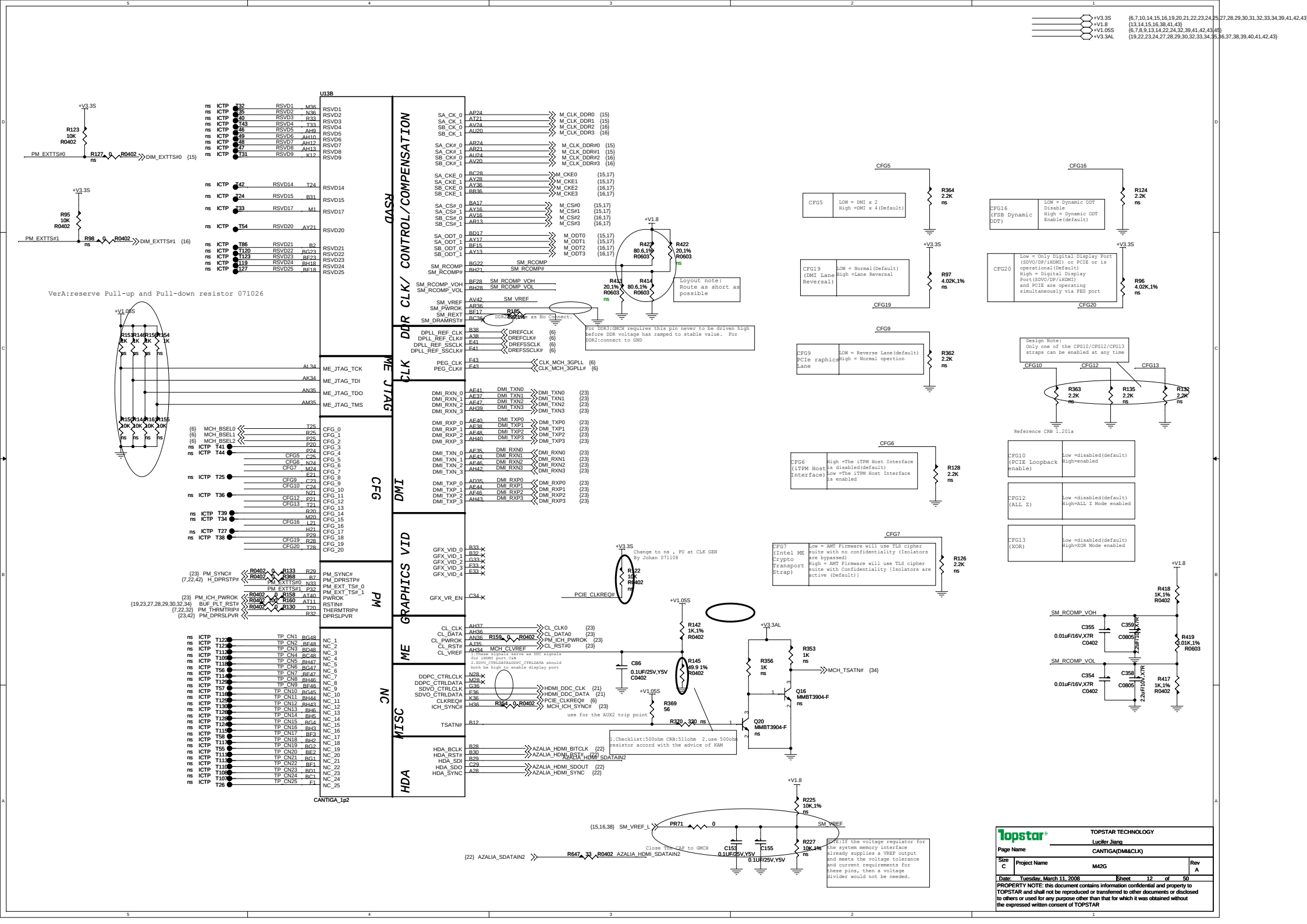
+V3.3S {6,7,10,14,15,16,19,20,21,22,23,24,25,27,28,29,30,31,32,33,34,39,41,42,43}
+V1.8 {13,14,15,16,38,41,43}
+V1.05S {6,7,8,9,13,14,22,24,32,39,41,42,43,45}
+V3.3AL {19,22,23,24,27,28,29,30,32,33,34,35,36,37,38,39,40,41,42,43}
U13B
RSVD
DDR CLK/ CONTROL/COMPENSATION
ME JTAG
CLK
DMI
CFG
GRAPHICS VID
PM
ME
MISC
NC
HDA
CANTIGA_1p2
VerA:reserve Pull-up and Pull-down resistor 071026
Layout note: Route as short as possible
For DDR3:GMCH requires this pin never to be driven high before DDR voltage has ramped to stable value. For DDR2:connect to GND
Change to ns , PU at CLK GEN By Johan 071108
1.Checklist:500ohm CRB:511ohm 2.use 500ohm resistor accord with the advice of KAM
Close the CAP to GMCH
Note:If the voltage regulator for the system memory interface already supplies a VREF output and meets the voltage tolerance and current requirements for these pins, then a voltage divider would not be needed.
Design Note: Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time
Reference CRB 1.201a
CFG5 LOW = DMI x 2 High =DMI x 4(Default)
CFG16 (FSB Dynamic ODT) LOW = Dynamic ODT Disable High = Dynamic ODT Enable(default)
CFG19 (DMI Lane Reversal) LOW = Normal(Default) High =Lane Reversal
CFG20 Low = Only Digital Display Port (SDVO/DP/iHDMI) or PCIE or is operational(Default) High = Digital Display Port(SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
CFG9 PCIe raphics Lane LOW = Reverse Lane(default) High = Normal opertion
CFG6 (iTPM Host Interface) High =The iTPM Host Interface is disabled(default) Low =The iTPM Host Interface is enabled
CFG7 (Intel ME Crypto Transport Strap) Low = AMT Firmware will use TLS cipher suite with no confidentiality (Isolators are bypassed) High = AMT Firmware will use TLS cipher suite with Confidentiality (Isolators are active (Default))
CFG10 (PCIE Loopback enable) Low =disabled(default) High=enabled
CFG12 (ALL Z) Low =disabled(default) High=ALL Z Mode enabled
CFG13 (XOR) Low =disabled(default) High=XOR Mode enabled
TOPSTAR TECHNOLOGY
Lucifer Jiang
Page Name CANTIGA(DMI&CLK)
Size C Project Name M42G Rev A
Date: Tuesday, March 11, 2008 Sheet 12 of 50
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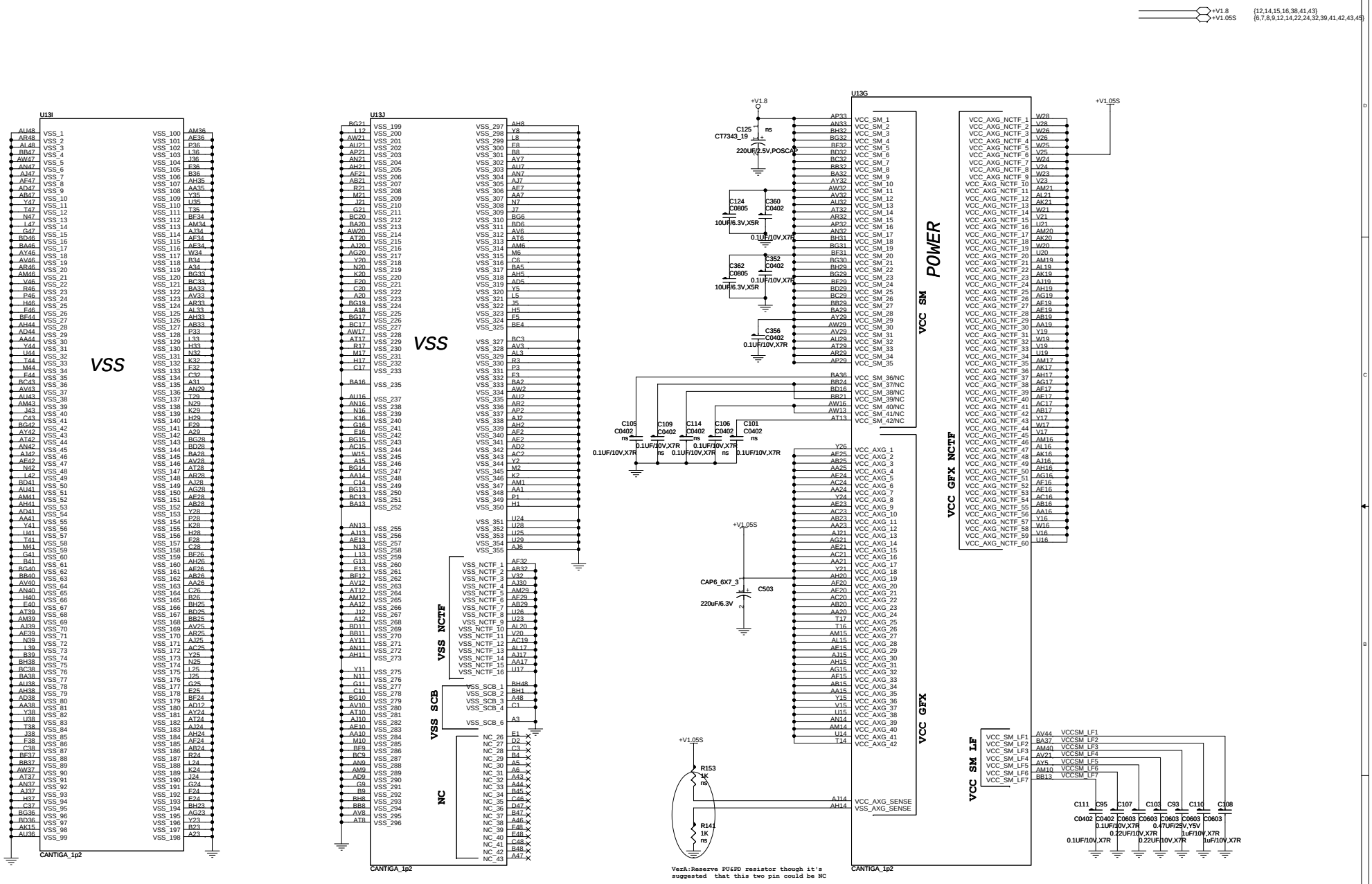

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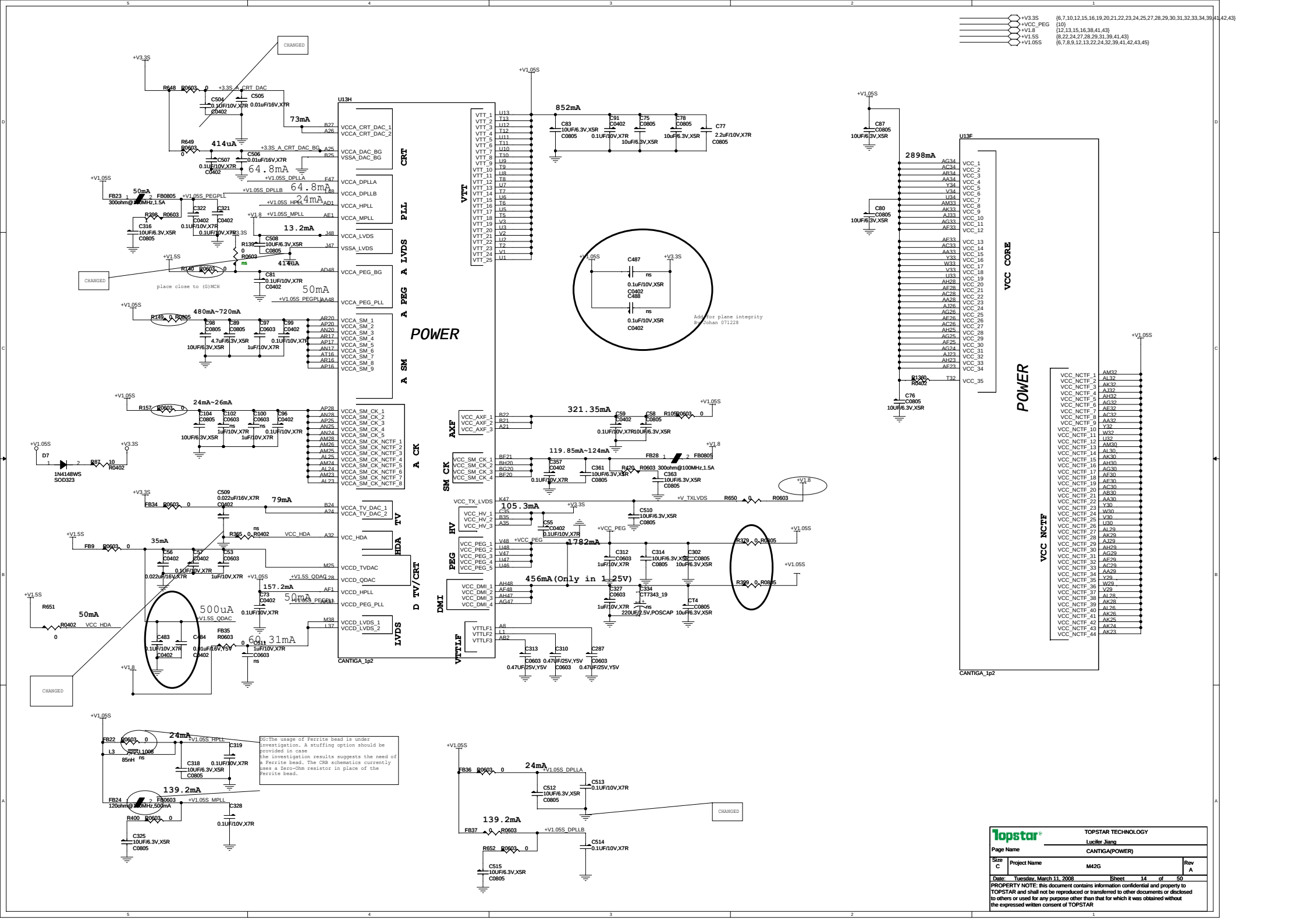
	Lucifer Jiang	
Page Name	CANTIGA(VSS&NCTF)	
Size C	Project Name M42G	Rev A
Date: Tuesday, March 11, 2008	Sheet 13 of 50	


+V3.3S {6,7,10,12,15,16,19,20,21,22,23,24,25,27,28,29,30,31,32,33,34,39,41,42,43}
+VCC_PEG {10}
+V1.8 {12,13,15,16,38,41,43}
+V1.5S {8,22,24,27,28,29,31,39,41,43}
+V1.05S {6,7,8,9,12,13,22,24,32,39,41,42,43,45}
U13H
U13F
POWER
CRT
PLL
LVDS
PEG
SM CK
AXF
HV
PEG
DMI
TV/CRT
TV
HDA
LVDS
VTTLF
VTT
VCC CORE
VCC NCTF
CANTIGA_1p2
852mA
321.35mA
119.85mA~124mA
105.3mA
1782mA
456mA(Only in 1.25V)
2898mA
73mA
414uA
64.8mA
50mA
24mA
13.2mA
480mA~720mA
24mA~26mA
79mA
35mA
157.2mA
500uA
60.31mA
139.2mA
CHANGED
place close to (G)MCH
Add for plane integrity By Johan 071228
DG:The usage of Ferrite bead is under investigation. A stuffing option should be provided in case the investigation results suggests the need of a Ferrite bead. The CRB schematics currently uses a Zero-Ohm resistor in place of the Ferrite bead.
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Lucifer Jiang
Page Name CANTIGA(POWER)
Size C
Project Name M42G
Rev A
Date: Tuesday, March 11, 2008
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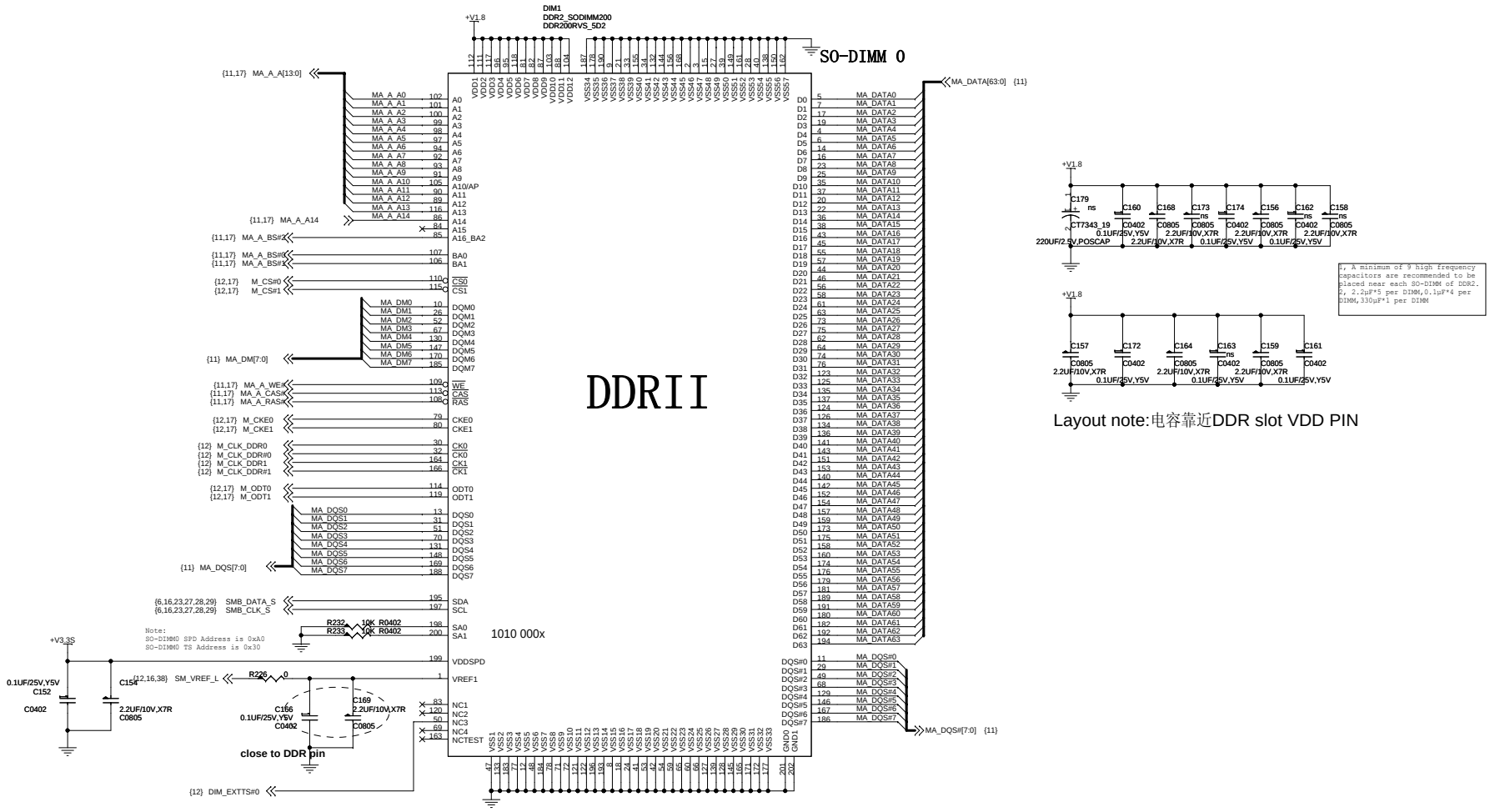
+V3.3S {6,7,10,12,14,16,19,20,21,22,23,24,25,27,28,29,30,31,32,33,34,39,41,42,43}
+V1.8 {12,13,14,16,38,41,43}



Layout note:电容靠近DDR slot VDD PIN

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Page Name	Lucifer Jiang	
	DDR2 SODIMM0	
Size C	Project Name M42G	Rev A
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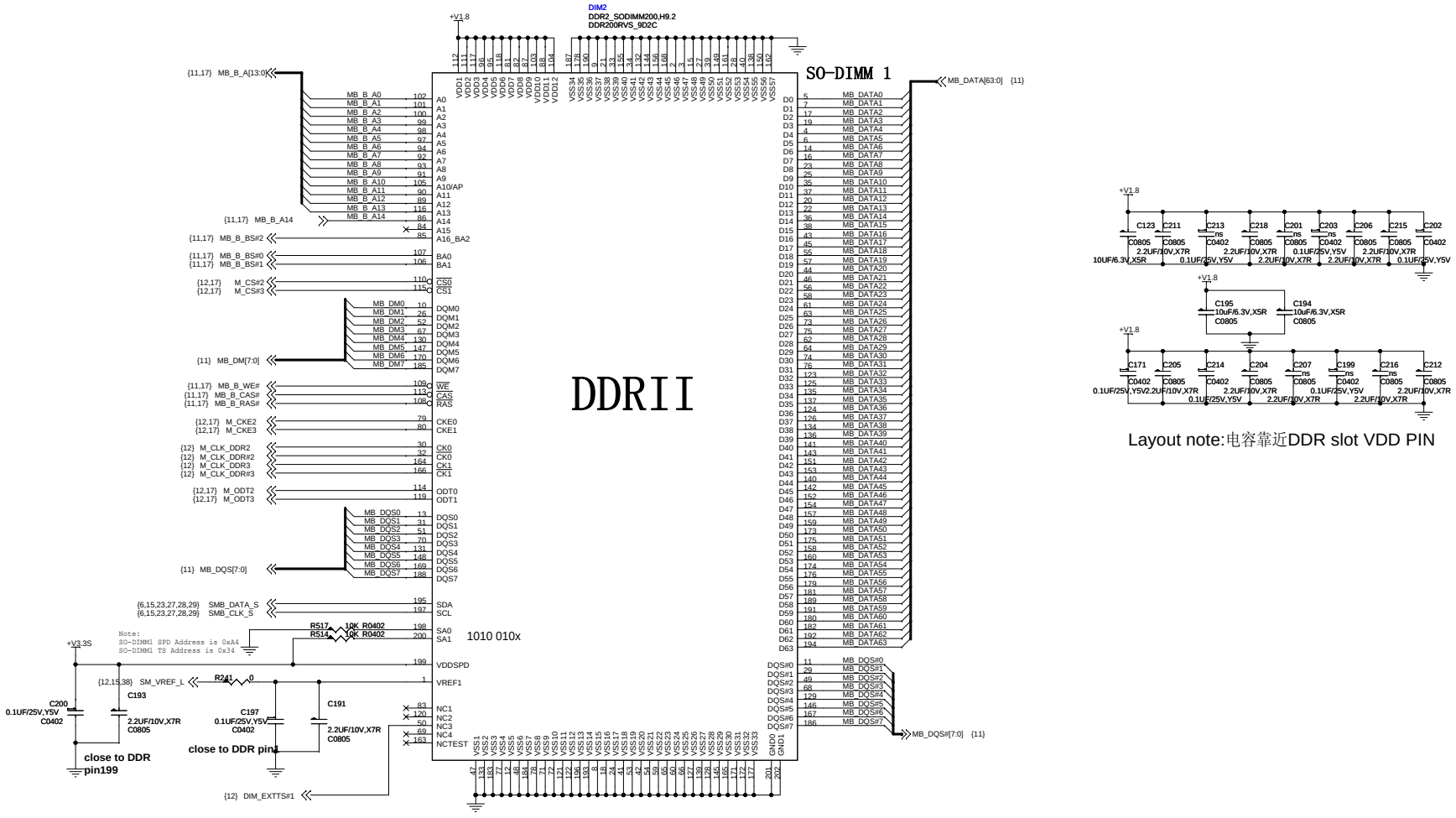

Layout note:电容靠近DDR slot VDD PIN

topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	DDR2 SODIMM1	
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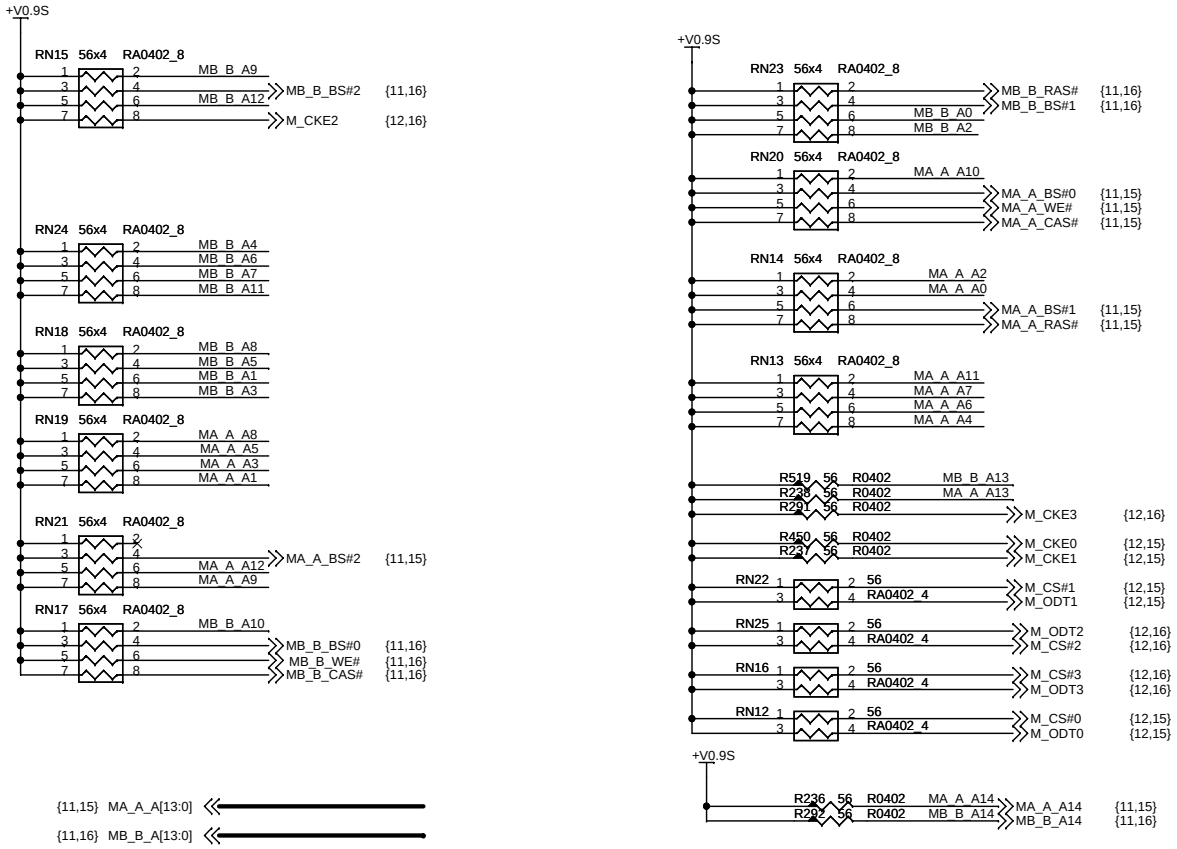
+V0.9S {18,38,43}



Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	DDR2 Series Termination	
Size B	Project Name M42G	Rev A
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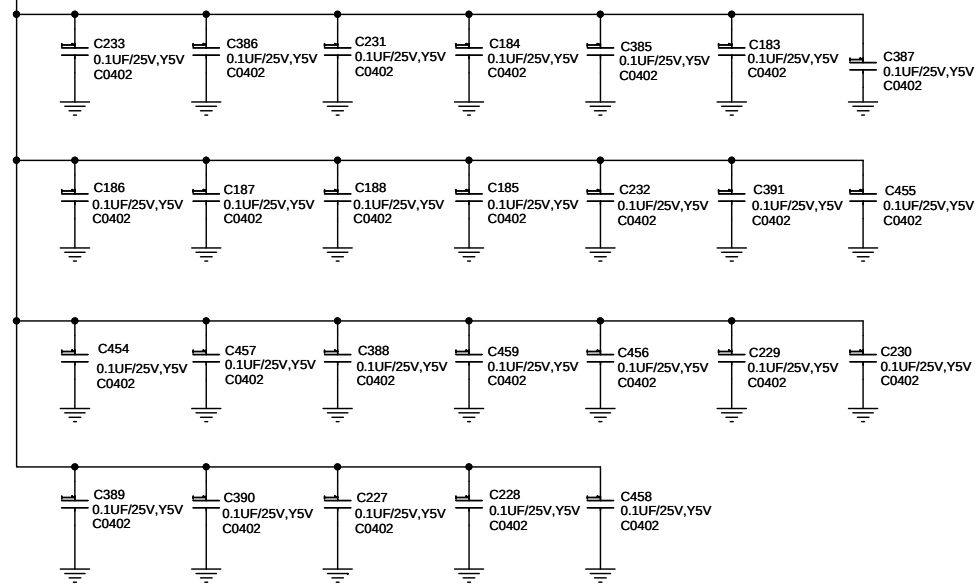
+V0.9S {17,38,43}

Layout note:Place one cap close to every 2 pullup resistors terminated to +V0.9S

+V0.9S

每4个电阻两个0.1UF电容



Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	DDR2 Decoupling	
Size B	Project Name M42G	Rev A
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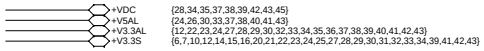
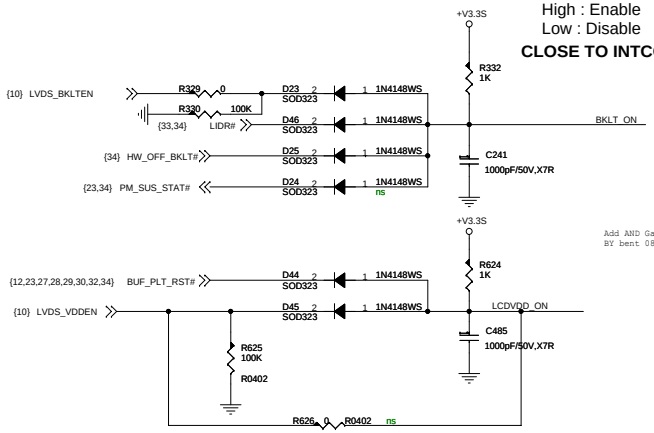
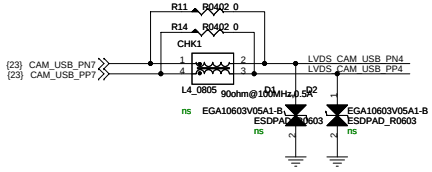
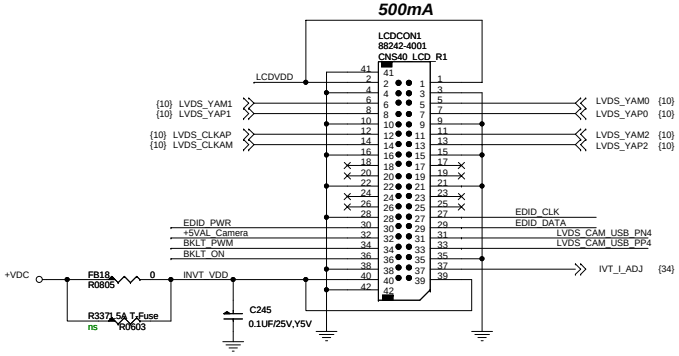
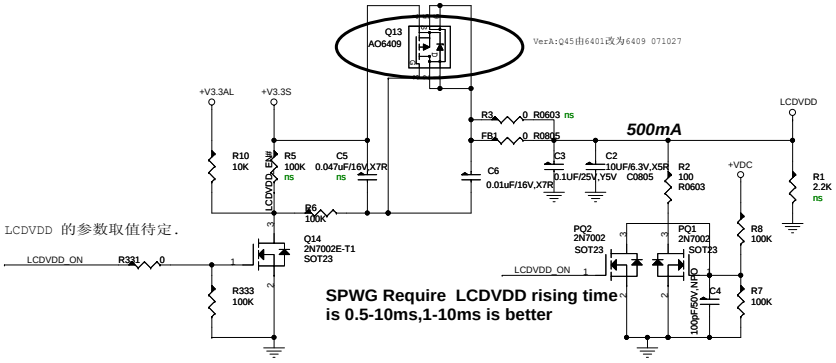
PANEL INTERFACE

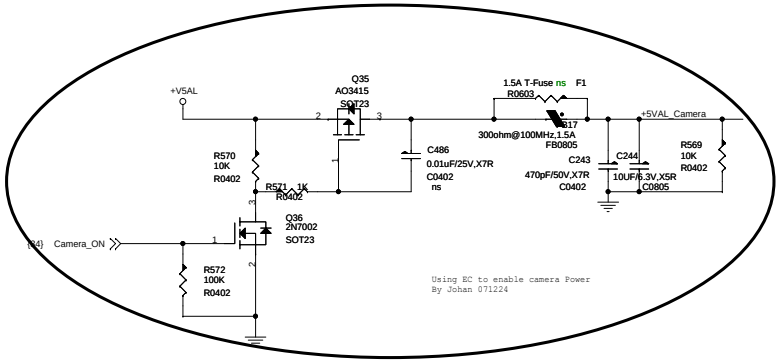


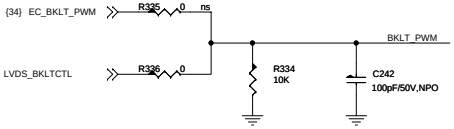


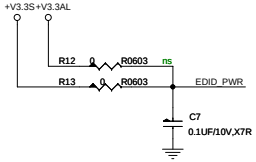


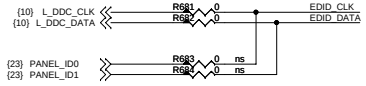












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	Lucifer Jiang	
Page Name	LVDS&Inverter CONN	
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AD+ {35}
+V5S {21,23,24,25,26,31,32,33,34,39,42,43}
+V3.3S {6,7,10,12,14,15,16,19,21,22,23,24,25,27,28,29,30,31,32,33,34,39,41,42,43}

R = C
G = Y
B = NOT USED/BS
WHEN NOT USE, 75 OHM TO GND

Place close to VGA_CONN1

{10} MCH_RED — FB3 47ohm@100MHz,500mA FB0402 — CRT_RED_R
C9 22pF/50V,NPO C0402

{10} MCH_GREEN — FB4 47ohm@100MHz,500mA FB0402 — CRT_GREEN_R
C10 22pF/50V,NPO C0402

{10} MCH_BLUE — FB2 47ohm@100MHz,500mA FB0402 — CRT_BLUE_R
C8 22pF/50V,NPO C0402

change to 22p for emc issue
by Johan 071227

88242_3001

CRT_RED_R
CRT_GREEN_R
CRT_BLUE_R
CRT_HSYNC {10}
CRT_VSYNC {10}
5VDDCCK
5VDDCDA
+V5S
AD+
CNS30_LCDB
VGA_CONN1

Video Board CONN

+V3.3S
R9 8.2K R0402
Q3 BSS138 SOT23
{10} CRT_DDC_CLK
5VDDCCK

+V3.3S
R4 8.2K R0402
Q1 BSS138 SOT23
{10} CRT_DDC_DATA
5VDDCDA

TOPSTAR TECHNOLOGY	Lucifer Jiang	
Page Name	VGA &SVIDEO &DCIN	
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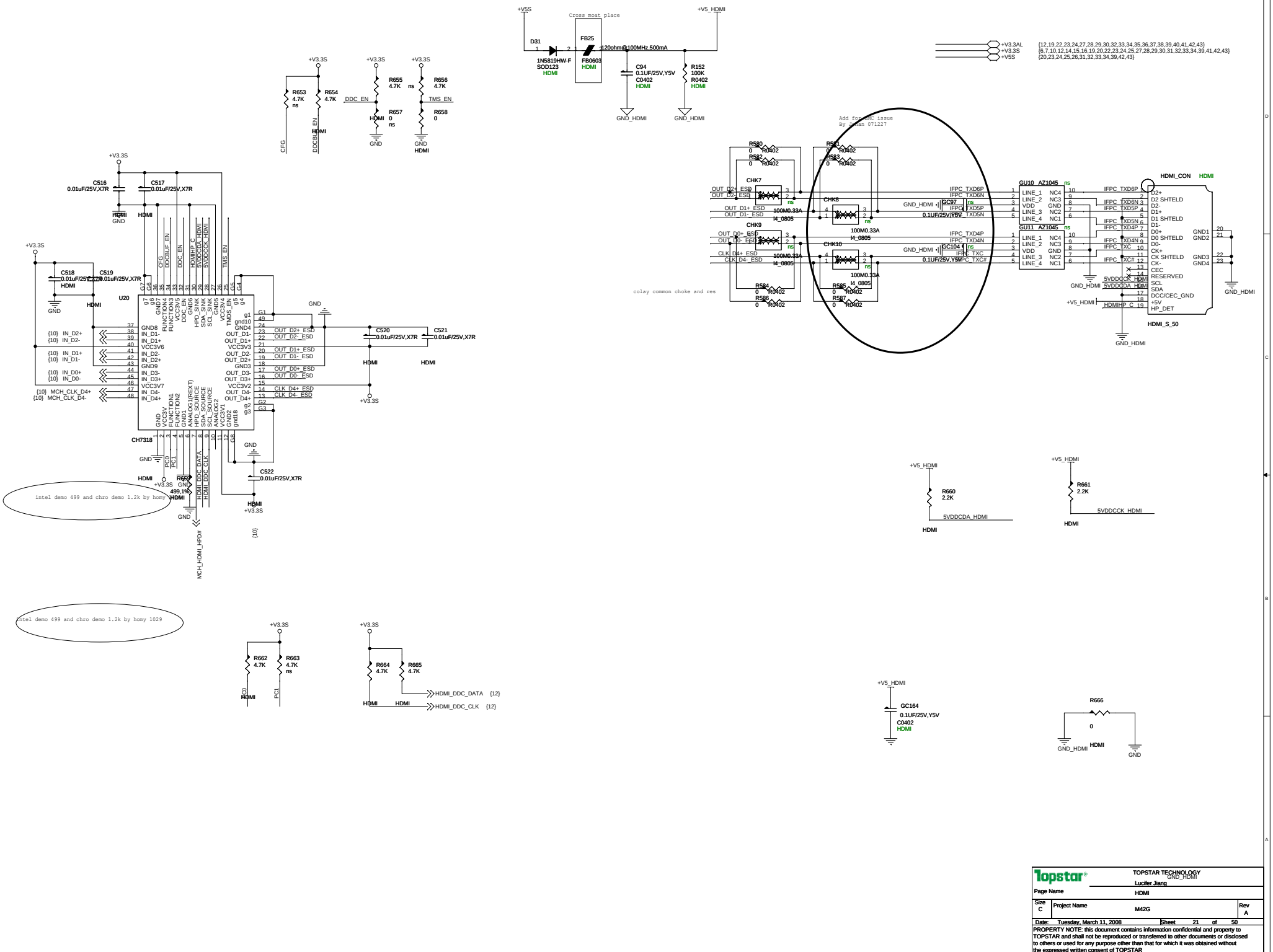

topstar®	TOPSTAR TECHNOLOGY	
Page Name	HDMI	
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+V3.3S {6,7,10,12,14,15,16,19,20,21,23,24,25,27,28,29,30,31,32,33,34,39,41,42,43}
ICH_EC_RTC {24}
EC_RTC {37}
+V1.05S {6,7,8,9,12,13,14,24,32,39,41,42,43,45}
+V1.5S_PCIE_ICH {23,24}
+V3.3AL {12,19,23,24,27,28,29,30,32,33,34,35,36,37,38,39,40,41,42,43}
+V1.5S {8,14,24,27,28,29,31,39,41,43}

Note:The new SRTCRST# signal is used to reset the RTC registers used for the Intel Management Engine when the on-board battery is changed. The external capacitor and the external resistor between SRTCRST# and VccRTC were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid.
The RC time delay should be in the range of 18 ms to 25 ms. There must not be a jumper for SRTCRST# pin. The SRTCRST# does not impact the implementation of CMOS clearing.

Voltage Swing on RTCX1 pin should not exceed 1.0V.

ICH_EC_RTC
R269 332K,1% R0402
332K 1% PULL HIGH TO VBAT_RTC FOR ICH8M INTRNAL VR ENABLE(PULL LOW DISABLE)
ICH_INTVRMEN
R293 0 ns R0402

EC_RTC
D22 BAT54C SOT23
ICH_EC_RTC
C235 1uF/10V,X7R C0603
R309 1K R0402
RTCBAT1 CONN2_R CNS2_R
Delete RTCBat socket for mechanical conflict
R261 20K
R268 R0402 20K
R262 R0402 1M R0402
C430 1uF/10V,X7R C0603
C223 1uF/10V,X7R C0603
CMOS Settings J1
Clear CMOS Short
Keep CMOS Open
J9 JOPEN RESISTOR_1 ns
Y4 32.768KHz XS4_8038
C463 15PF/50V,NPO C0402
C462 15PF/50V,NPO C0402
R523 10M R0402

SPONGE_RTC1 RTCBAT GLUE
RTC_BAT1
RTCBAT with Cable
根据机构定Cable尺寸

U6A
RTCX1 C23
RTCX2 C24
RTCRST# A25 RTC_RST#
SRTCRST# F20 SRTC_RST#
INTRUDER# C22 SM_INTRUDER#
INTVRMEN B22 ICH_INTVRMEN
LAN100_SLP A22
RTC

FWH0/LAD0 K5 LPC_AD0 {28,32,34}
FWH1/LAD1 K4 LPC_AD1 {28,32,34}
FWH2/LAD2 L6 LPC_AD2 {28,32,34}
FWH3/LAD3 K2 LPC_AD3 {28,32,34}
FWH4/LFRAME# K3 LPC_FRAME# {28,32,34}
LDRQ0# J3
LDRQ1#/GPIO23 J1
LPC
+V3.3S
R239 10K R0402
R242 10K R0402 ns

GLAN_CLK E25
LAN_RSTSYNC C13
LAN_RXD0 E14
LAN_RXD1 G13
LAN_RXD2 D14
LAN_TXD0 D13
LAN_TXD1 D12
LAN_TXD2 E13
If LAN interface is not used, this signal can be left as No Connect.
R282 0 R0402 ns
+V1.5S_PCIE_ICH
R487 24.9,1% R0402
C373 ns 5.6pF/50V,NPO C0402
R428 33 R0402 {31} AZALIA_CODEC_BITCLK
GPIO56 B10
GLAN_COMPI B28
GLAN_COMPO B27
LAN / GLAN

A20GATE N7 H_A20GATE {34}
A20M# J27 H_A20M# {7}
DPRSTP# A25 H_DPRSTP# {7,12,42}
DPSLP# AE23 H_DPSLP# {7}
FERR# A26 H_FERR# {7}
R207 56 R0402
R208 R0402
R444 R0402
R213 56 R0402
R454 56 ns R0402
R214 56 R0402
+V1.05S
CPUPWRGD AD22 H_PWRGD {7}
IGNNE# AE25 H_IGNNE# {7}
INIT# AE22 H_INIT# {7}
INTR AG25 H_INTR {7}
RCIN# L3 H_RCIN# {34}
NMI AF23 H_NMI {7}
SMI# AF24 H_SMI# {7}
R435 R0402
STPCLK# AH27 H_STPCLK# {7}
THRMTRIP# AG26 R216 54.9,1% PM_THRMTRIP# {7,12,32}
TP12 AG27 T67 ICTP ns R0402
CPU

Checklist:the series termination RES of FERR#/IERR#/THERMTRIP are 56/56/55ohm。
+V1.05S
R215 56 R0402
R177 NEEDS BE PLACE WITHIN 2" OF ICH9, R173 NEEDS BE PLACED WITHIN 2" OF R177 WITHOUT STUB

HDA_BIT_CLK AF6
HDA_SYNC AH4
HDA_RST# AE7
HDA_SDIN0 AF4
HDA_SDIN1 AG4
HDA_SDIN2 AH3
HDA_SDIN3 AE5
HDA_SDOUT AG5
HDA_DOCK_EN#/GPIO33 AG7
HDA_DOCK_RST#/GPIO34 AF8
SATALED# AG8
IHDA
{31} AZALIA_CODEC_SYNC R200 33 R0402
{31} AZALIA_CODEC_RST# R442 33 R0402
{31} AZALIA_SDATAIN0
{12} AZALIA_SDATAIN2
{31} AZALIA_CODEC_SDOUT R189 33 R0402
bitclk ACSYNC_D RST# AC_SDOUT
ns ICTP T160
ns ICTP T135
ns ICTP T136
HDA_DOCK_EN#
{33} IDE_LED#

SATA4RXN AH11 SATA4_RXN R192 1K R0402 ns
SATA4RXP AJ11 SATA4_RXP R191 1K R0402 ns
SATA4TXN AG12
SATA4TXP AF12
SATA5RXN AH9 SATA5_RXN R194 1K R0402 ns
SATA5RXP AJ9 SATA5_RXP R193 1K R0402 ns
SATA5TXN AE10
SATA5TXP AE10
SATA_CLKN AH18 CLK_ICH_SATA# {6}
SATA_CLKP AJ18 CLK_ICH_SATA {6}
SATARBIAS# AJ7 R427 24.9,1%
SATARBIAS AH7
R0402
No stuff for SATA function
within 500 mils of the ICH9-M

SATA HDD
{25} SATA_RXN0 AJ16
{25} SATA_RXP0 AH16
{25} SATA_TXN0 AF17
{25} SATA_TXP0 AG17
C0402 C370 0.01uF/25V,X7R
C0402 C369 0.01uF/25V,X7R
SATA ODD
{25} SATA_RXN1 AH13
{25} SATA_RXP1 AJ13
{25} SATA_TXN1 AG14
{25} SATA_TXP1 AF14
C0402 C135 0.01uF/25V,X7R
C0402 C134 0.01uF/25V,X7R
SATA
Same distance to the ICH
Close the ICH as possible
ICH9M REV 1.0

+V3.3AL
R275 10K R0402
GPIO56
+V1.5S
+V3.3S
R685 8.2K R0402 ns
R686 8.2K R0402 ns
HDA_DOCK_EN#
R687 1K R0402 ns
HDCP JOPEN RESISTOR_1 ns
后盖打开就能看到。

+V3.3S
C526 0.01uF/25V,X7R C0402
加两个缝合电容

C523 C0402 5.6pF/50V,NPO ns
HDMR0402
{12} AZALIA_HDMI_BITCLK R667 33 bitclk
{12} AZALIA_HDMI_SYNC R668 HDMI 33 R0402 ACSYNC_D
{12} AZALIA_HDMI_RST# R669 HDMI 33 R0402 RST#
{12} AZALIA_HDMI_SDOUT R670 <Designator> HDMI 33 R0402 AC_SDOUT

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Close ICH9 as possible

+V3.3AL {12,19,22,24,27,28,29,30,32,33,34,35,36,37,38,39,40,41,42,43}
+V3.3S {6,7,10,12,14,15,16,19,20,21,22,24,25,27,28,29,30,31,32,33,34,39,41,42,43}
+V1.5S_PCIE_ICH {22,24}
+V5S {20,21,24,25,26,31,32,33,34,39,42,43}

U6B
PCI
Interrupt I/F
ICH9M REV 1.0

U6D
PCI-Express
Direct Media Interface
SPI
USB
ICH9M REV 1.0

GNT0#	SPI_CS1#	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC

U6C
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC

U8 74AHCT1G08GV SOT23_5
U7 74AHCT1G08GV SOT23_5
U9 74AHCT1G08GV SOT23_5
U16 W25X40 SO8_50_150
U17 S25FL008A SOIC8_50_208

The Bus switch prevents Leakage of the SMBus into devices powered on the switched rail.

Add for option(SATA interlock switch)

Place within 500 mils of ICH

EXPRESS Card
Robson
Echo Peak
BLUETOOTH
USB0 PORT
USB1 PORT
CAMERA
CARD READER
USB2 PORT

VerA:change the port sequence for the convenience of layout

Note:1.GPIO57 Can be used as TPM Physical Presence pin for iTPM 2.The iTPM function of chipset is disabled default

The signal is required to be low for desktop applications and high for mobile app.It has a weak internal pull-up(20K)

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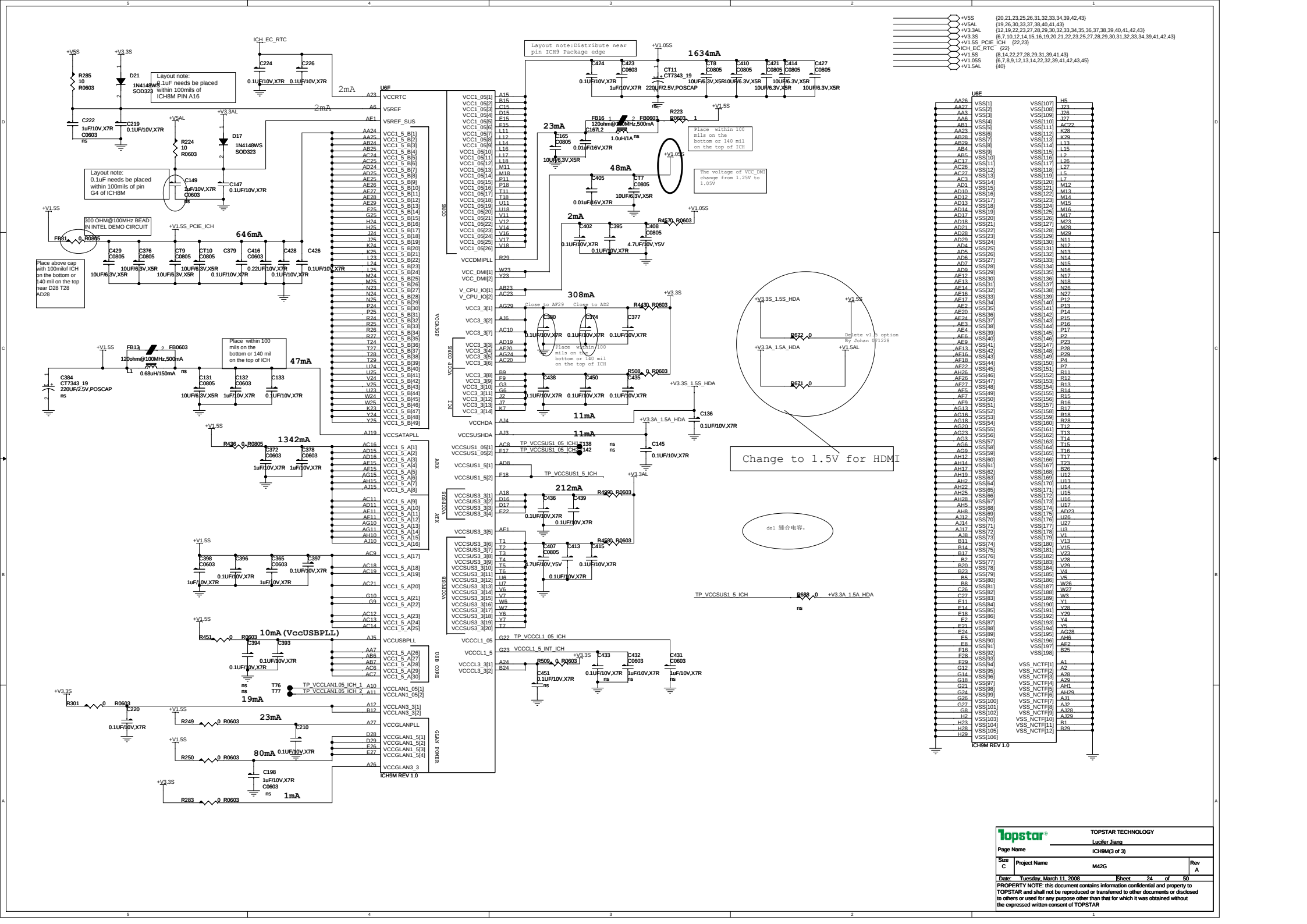

Company	TOPSTAR TECHNOLOGY
Designer	Lucifer Jiang
Page Name	ICH9M(3 of 3)
Size	C
Project Name	M42G
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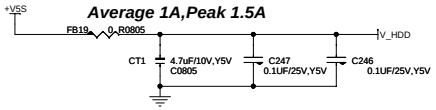
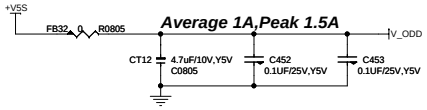
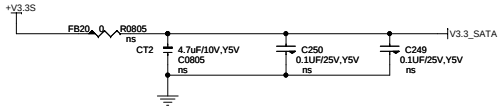
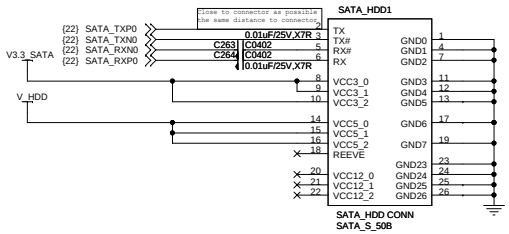
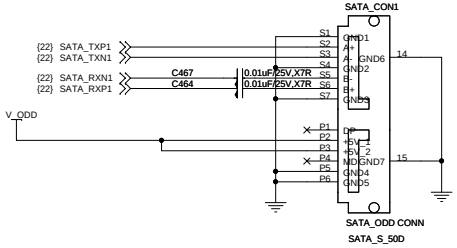
+V5S {20,21,23,24,26,31,32,33,34,39,42,43}
+V3.3S {6,7,10,12,14,15,16,19,20,21,22,23,24,27,28,29,30,31,32,33,34,39,41,42,43}

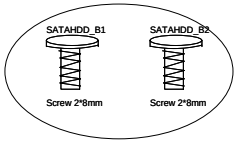


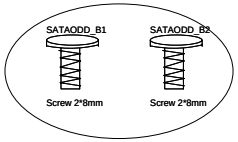






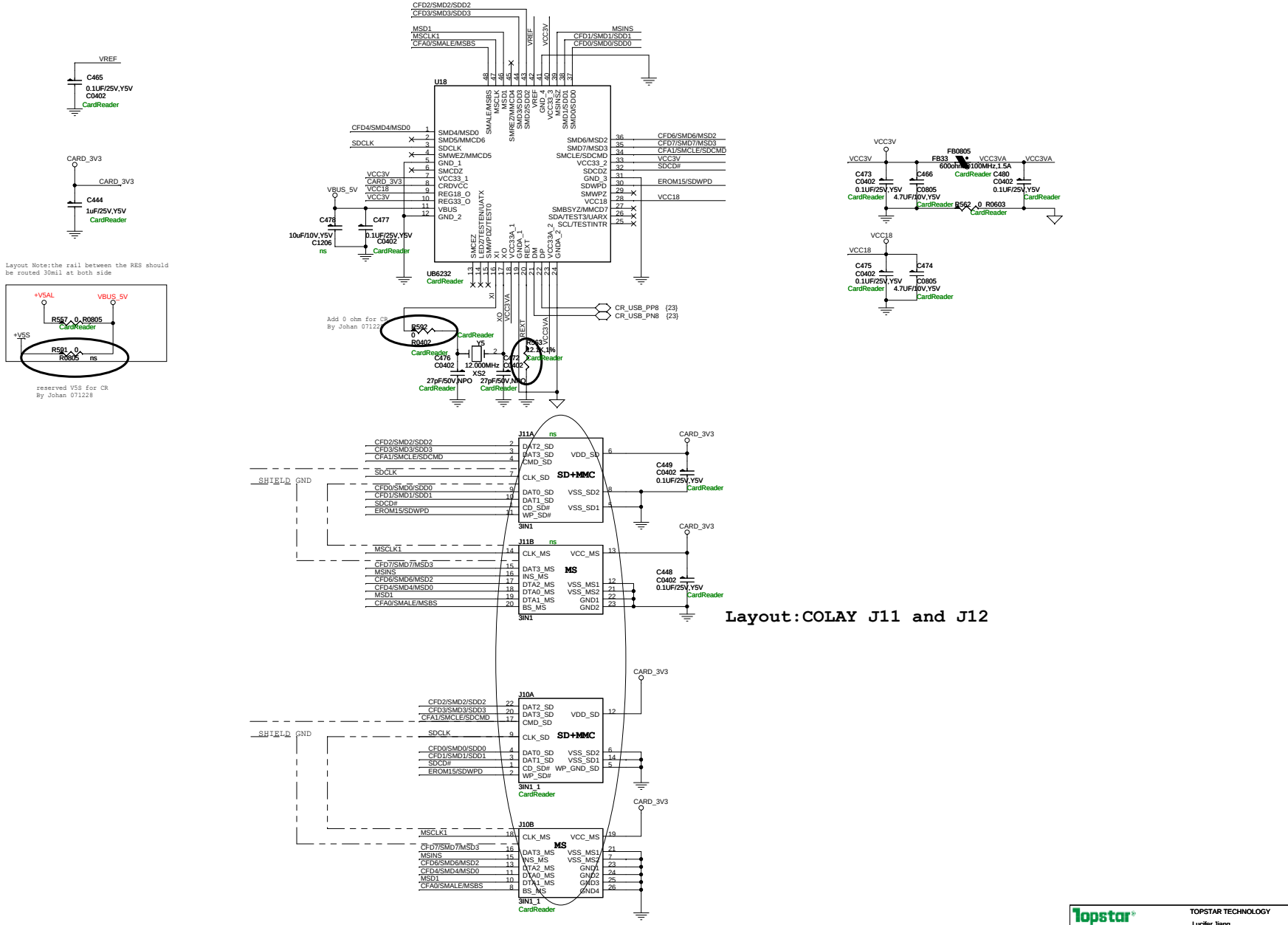






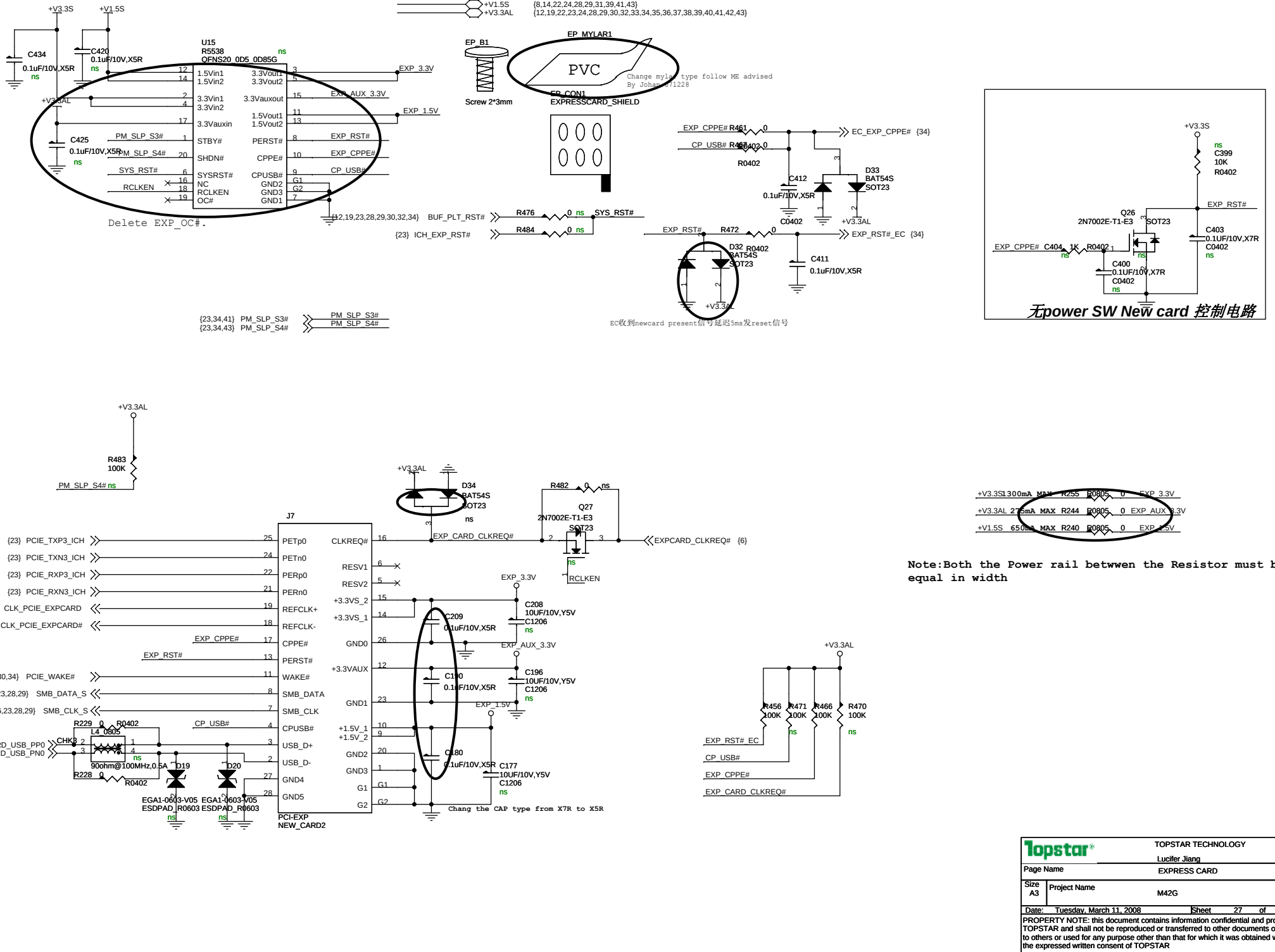
topstar®	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	SATA HDD&ODD	
Size C	Project Name M42G	Rev A
Date: Tuesday, March 11, 2008	Sheet 25 of 50	

+V5AL {19,24,30,33,37,38,40,41,43}
+V5S {20,21,23,24,25,31,32,33,34,39,42,43}

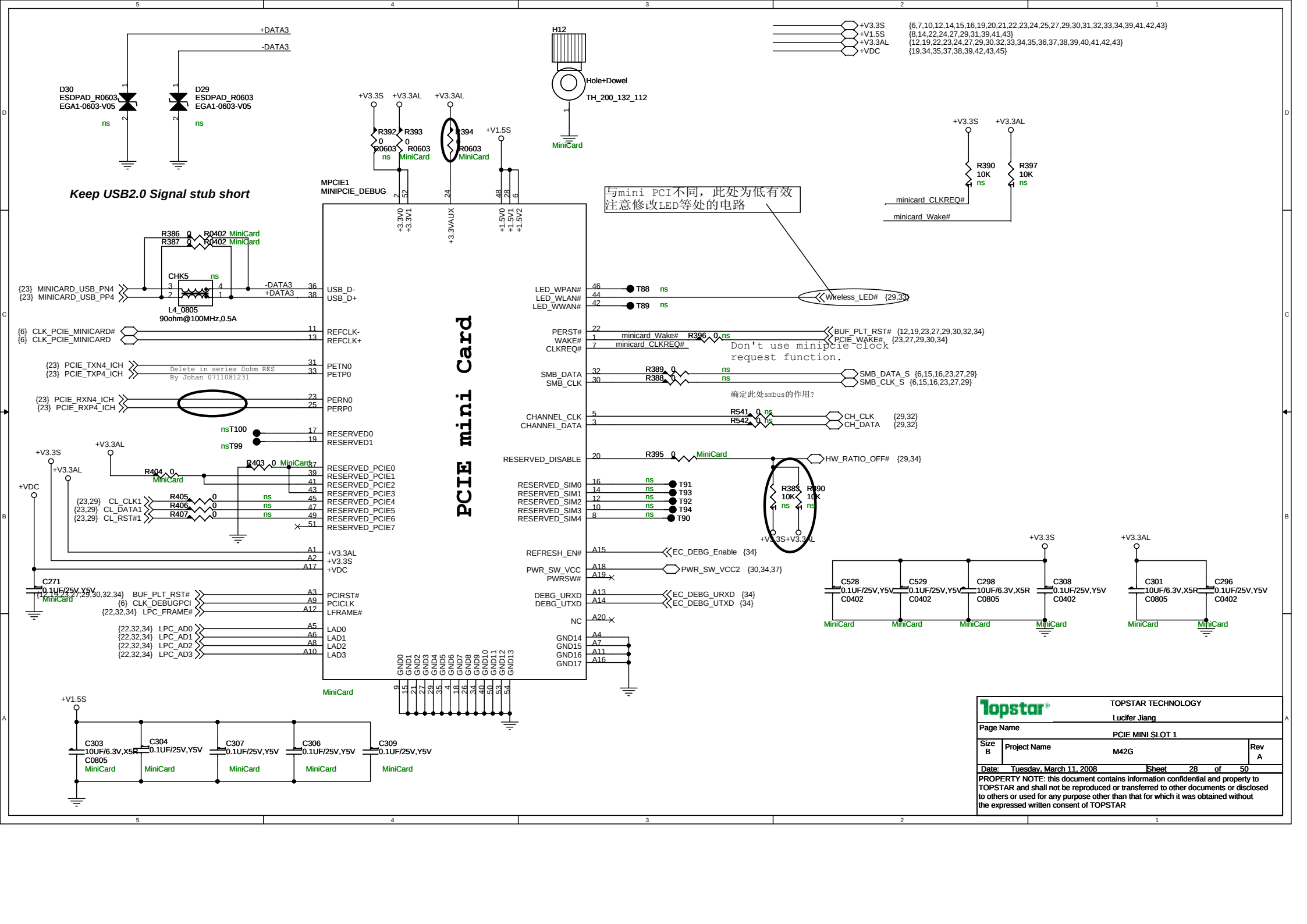


Layout:COLAY J11 and J12

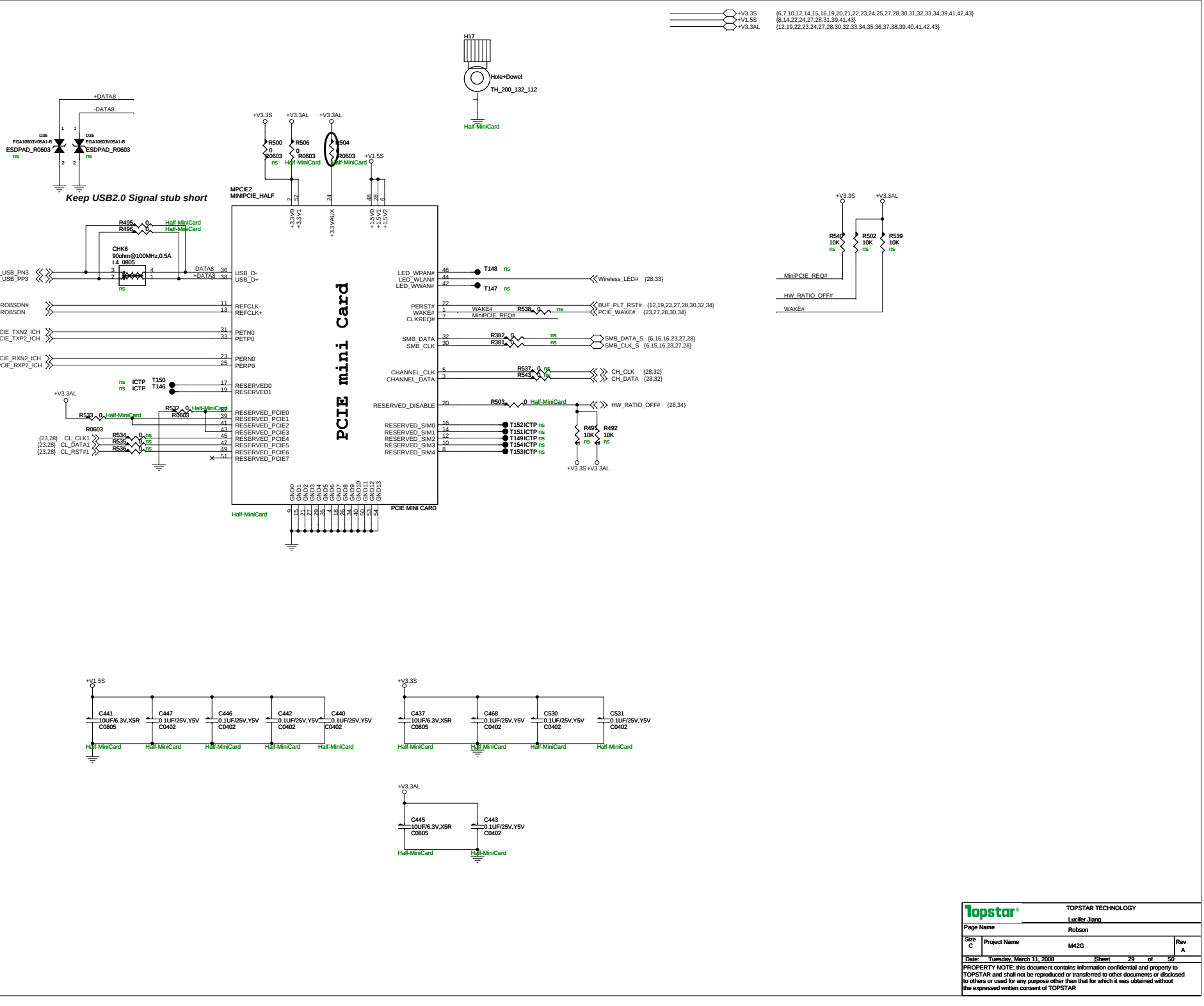
topstar	TOPSTAR TECHNOLOGY	
Page Name	Lucifer Jiang	
	Card Reader(UB6232 USB)	
Size C	Project Name M42G	Rev A
Date: Tuesday, March 11, 2008	Sheet 26 of 50	



Topstar	TOPSTAR TECHNOLOGY		
	Lucifer Jiang		
Page Name	EXPRESS CARD		
Size A3	Project Name M42G		Rev A
Date: Tuesday, March 11, 2008	Sheet 27 of 50		



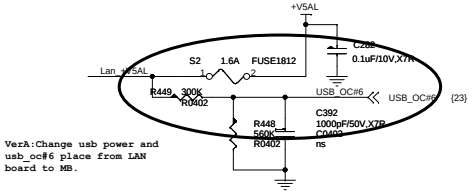
Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	PCIE MINI SLOT 1	
Size B	Project Name M42G	Rev A
Date: Tuesday, March 11, 2008	Sheet 28 of 50	



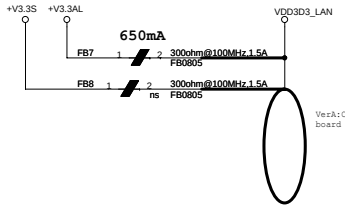
topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	Robson	
Size C	Project Name M42G	Rev A
Date: Tuesday, March 11, 2008	Sheet 29 of 50	

+VDC {19,28,34,35,37,38,39,42,43,45}
+V5AL {19,24,26,33,37,38,40,41,43}
+V3.3AL {12,19,22,23,24,27,28,29,32,33,34,35,36,37,38,39,40,41,42,43}
+V3.3S {6,7,10,12,14,15,16,19,20,21,22,23,24,25,27,28,29,31,32,33,34,39,41,42,43}
Isense_SYSP {35,44}

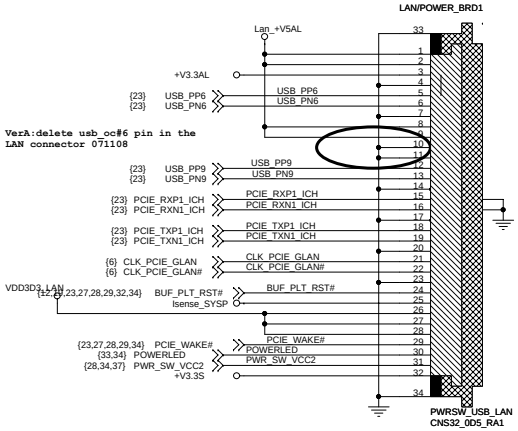
PWR LED/USB/Lan Connector



VerA:Change usb power and usb_oc#6 place from LAN board to MB.



VerA:Change the power decoupling CAP from MB board to daughter board.



topstar®	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	Power/USB/LAN CONN	
Size C	Project Name M42G	Rev A
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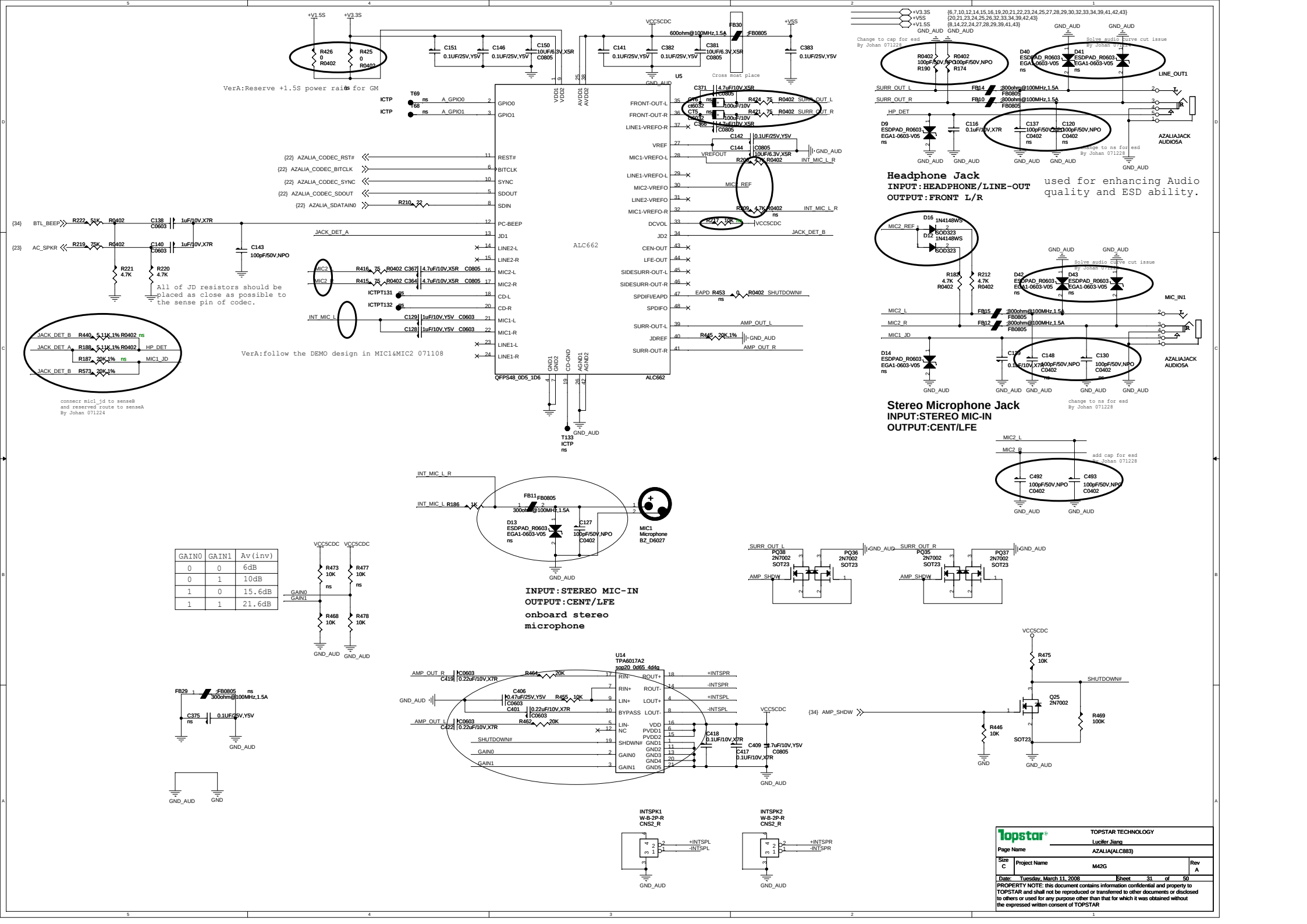
ALC662
QFPS48_0D5_1D6
VerA:Reserve +1.5S power rail is for GM
VerA:follow the DEMO design in MIC1&MIC2 071108
All of JD resistors should be placed as close as possible to the sense pin of codec.
connecr mic1_jd to senseB and reserved route to senseA By Johan 071224
Headphone Jack
INPUT:HEADPHONE/LINE-OUT
OUTPUT:FRONT L/R
used for enhancing Audio quality and ESD ability.
Stereo Microphone Jack
INPUT:STEREO MIC-IN
OUTPUT:CENT/LFE
INPUT:STEREO MIC-IN
OUTPUT:CENT/LFE
onboard stereo microphone
GAIN0 GAIN1 Av(inv)
0 0 6dB
0 1 10dB
1 0 15.6dB
1 1 21.6dB
U14 TPA6017A2 sop20_0d65_4d4q
INTSPK1 W-B-2P-R CNS2_R
INTSPK2 W-B-2P-R CNS2_R
TOPSTAR TECHNOLOGY
Lucifer Jiang
Page Name AZALIA(ALC883)
Size C Project Name M42G Rev A
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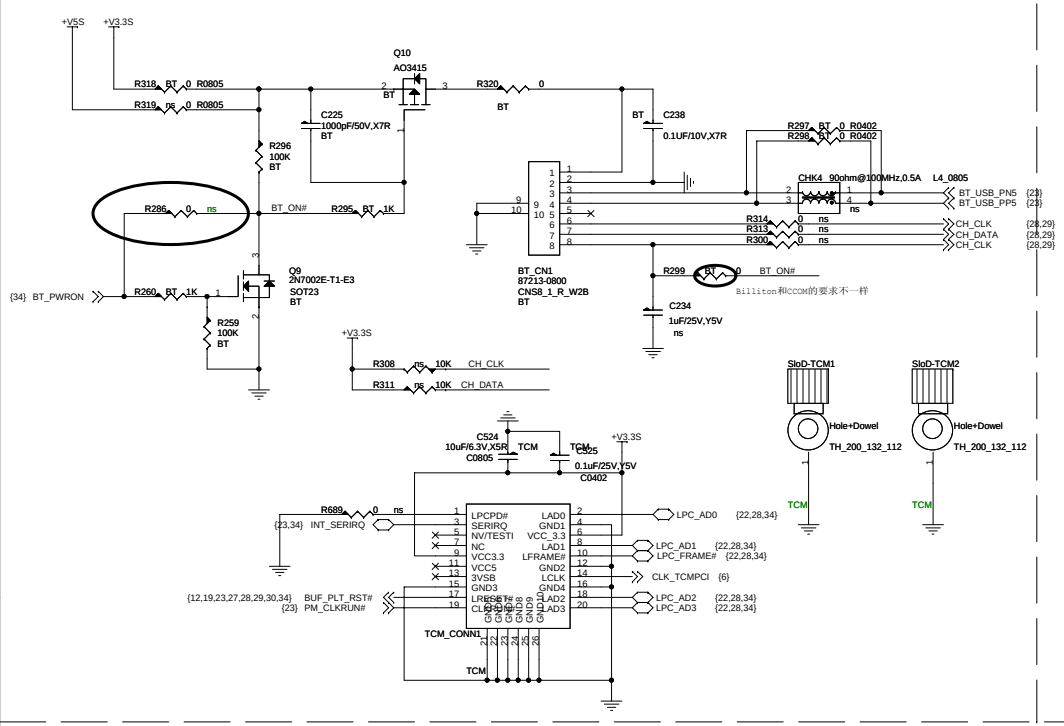
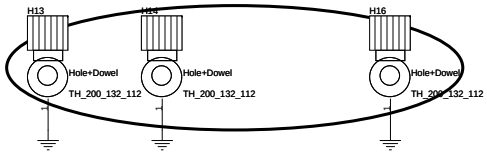
FAN Controller Circuit

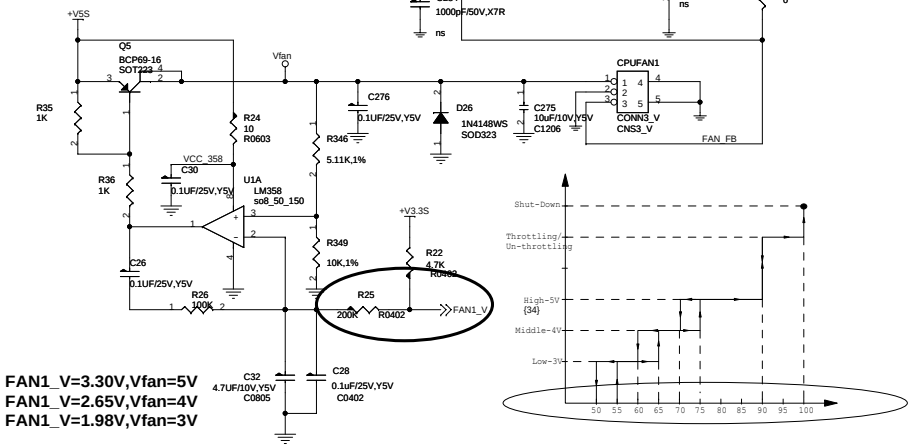
+V1.05S {6,7,8,9,12,13,14,22,24,39,41,42,43,45}
+V3.3S {6,7,10,12,14,15,16,19,20,21,22,23,24,25,27,28,29,30,31,33,34,39,41,42,43}
+V5S {20,21,23,24,25,26,31,33,34,39,42,43}
+V3.3AL {12,19,22,23,24,27,28,29,30,33,34,35,36,37,38,39,40,41,42,43}

MDC (Software MODEM)

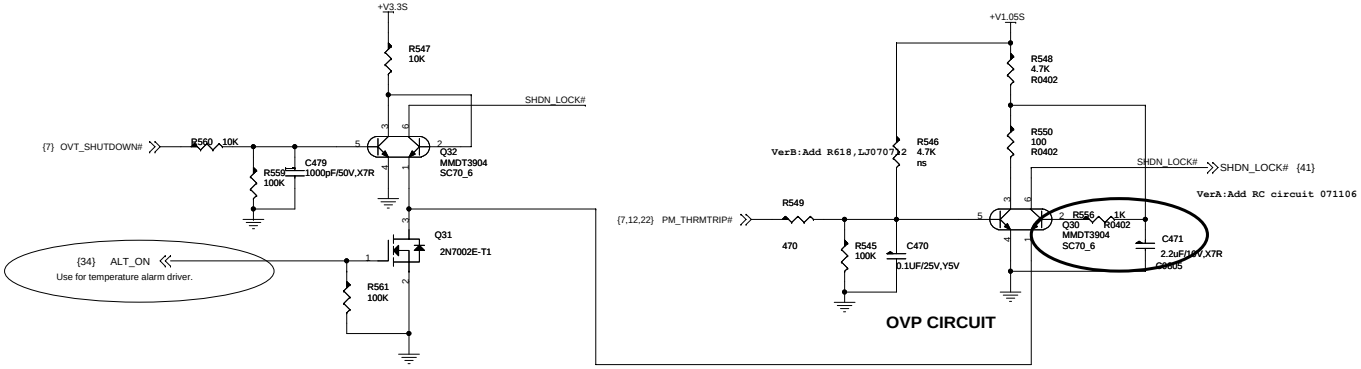




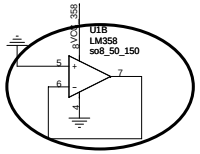
For FAN&Heatsink use

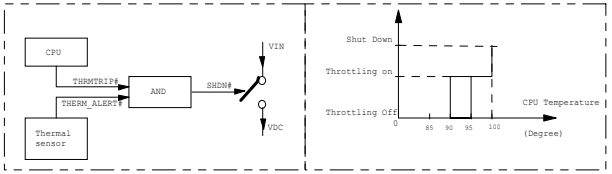


FAN1_V=3.30V,Vfan=5V
FAN1_V=2.65V,Vfan=4V
FAN1_V=1.98V,Vfan=3V



VerA:Delete GMCH_TEMP signal and components 071026





PCB1 R20 MB **PCB**

PCBA1 R20 PCBA **PCBA**

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	Lucifer Jiang	
Page Name	MDC&BT/FAN/OTP	
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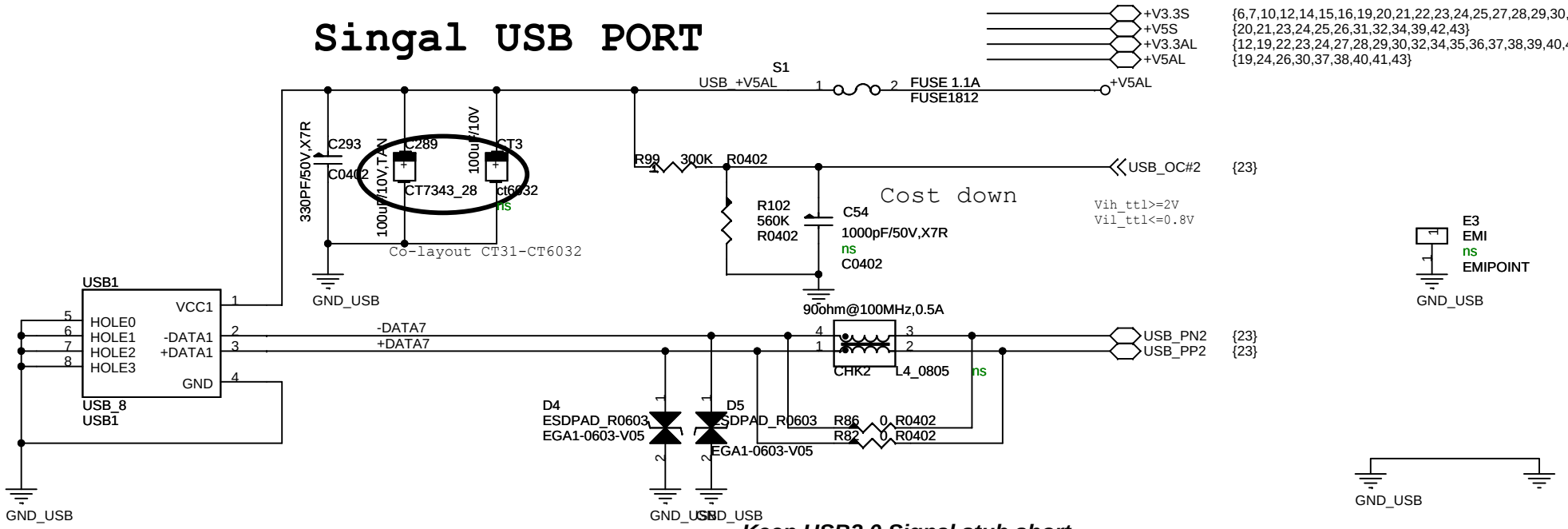
Singal USB PORT

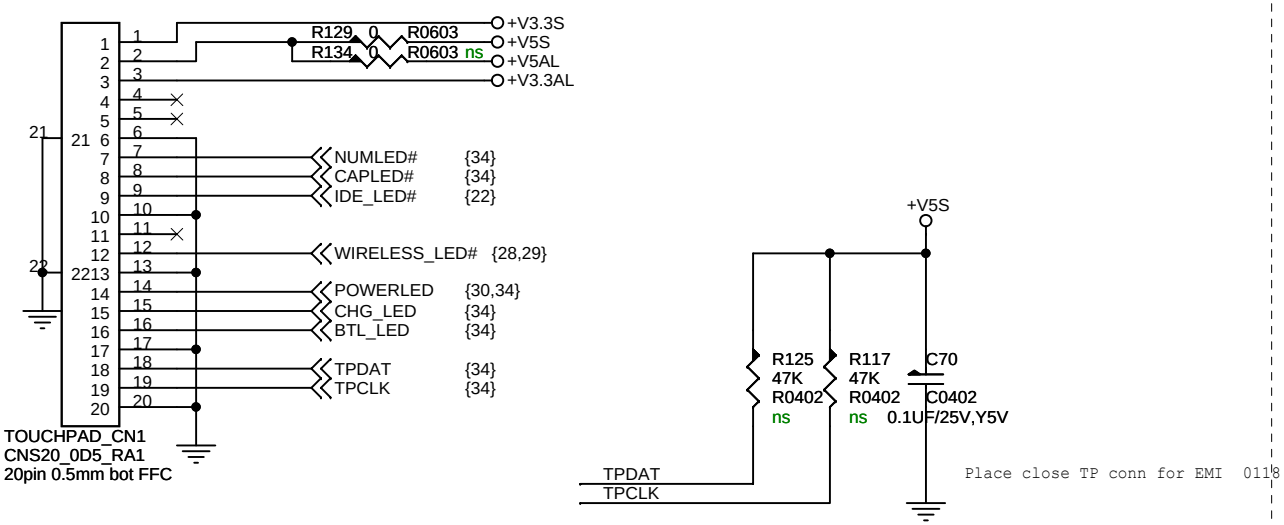


Keep USB2.0 Signal stub short

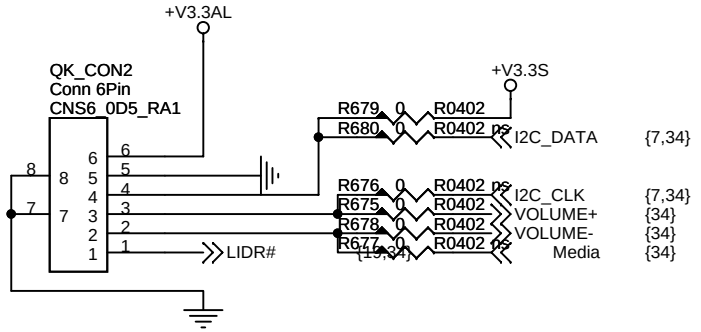
VerA:BAV99由DIODES改为NXP的 071026

Delete for si issue (bat54s)
By Johan 071224

Touchpad Conn



Quick button Conn



Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	USB2.0&&LED CONN&Qkey CONN	
Size A4	Project Name M42G	Rev A
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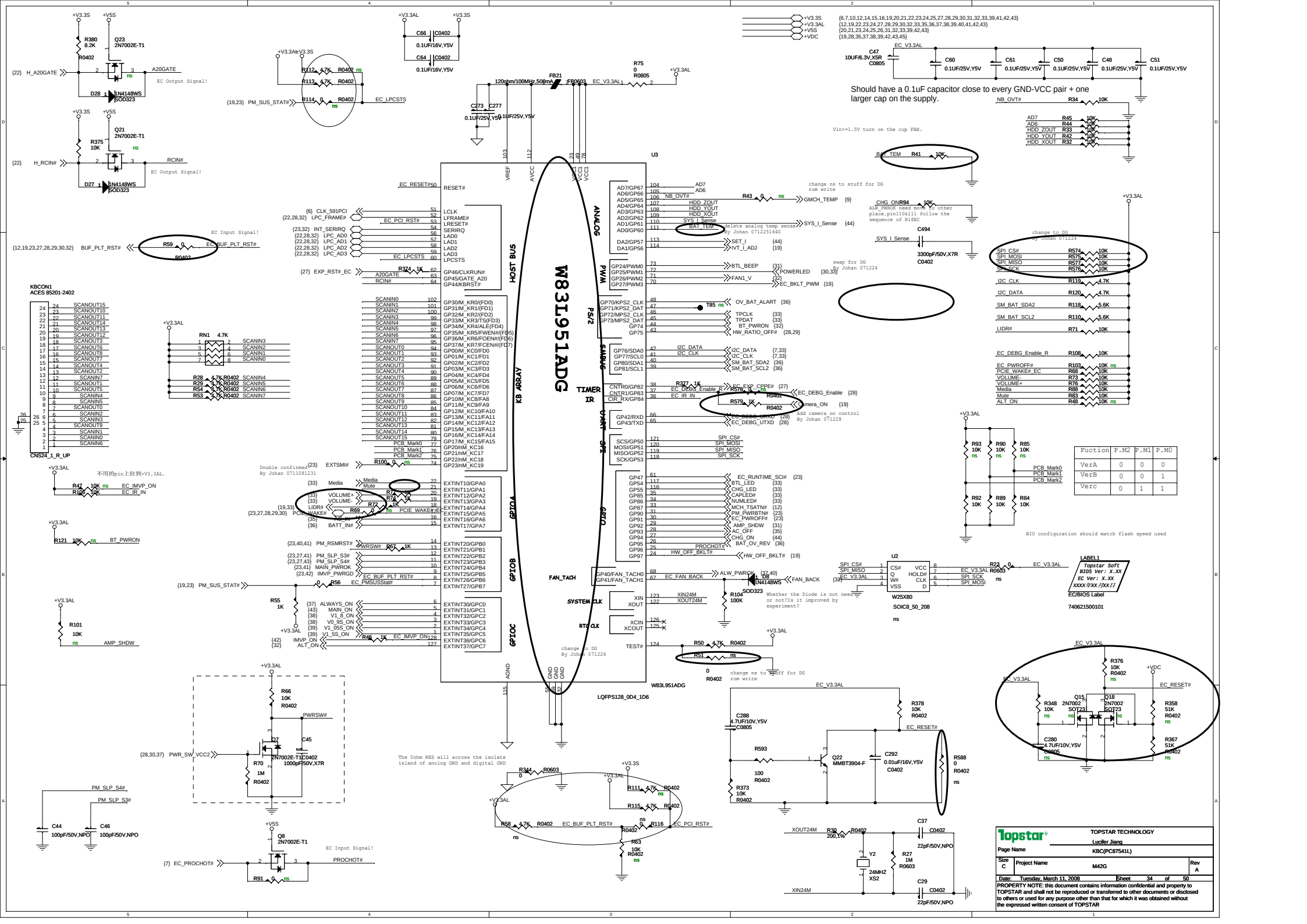
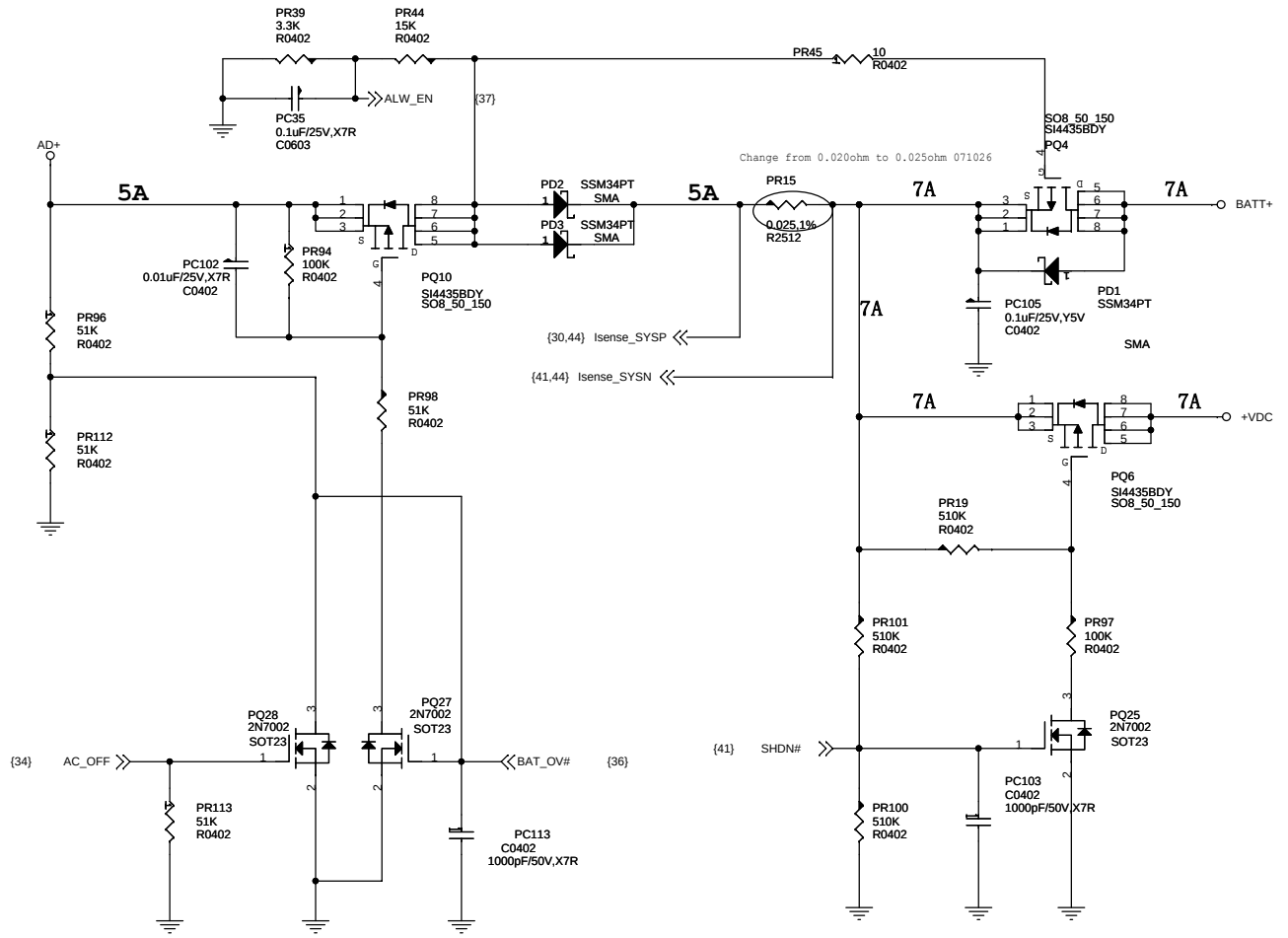
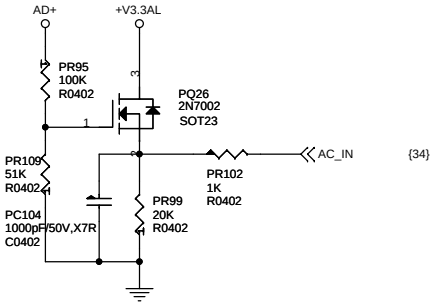


Fuction	P.M2	P.M1	P.M0
VerA	0	0	0
VerB	0	0	1
Verc	0	1	1

BATT+ {36,44}
+VDC {19,28,34,37,38,39,42,43,45}
AD+ {20}
+V3.3AL {12,19,22,23,24,27,28,29,30,32,33,34,36,37,38,39,40,41,42,43}





Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	ADAPTER IN	
Size A3	Project Name M42G	Rev A
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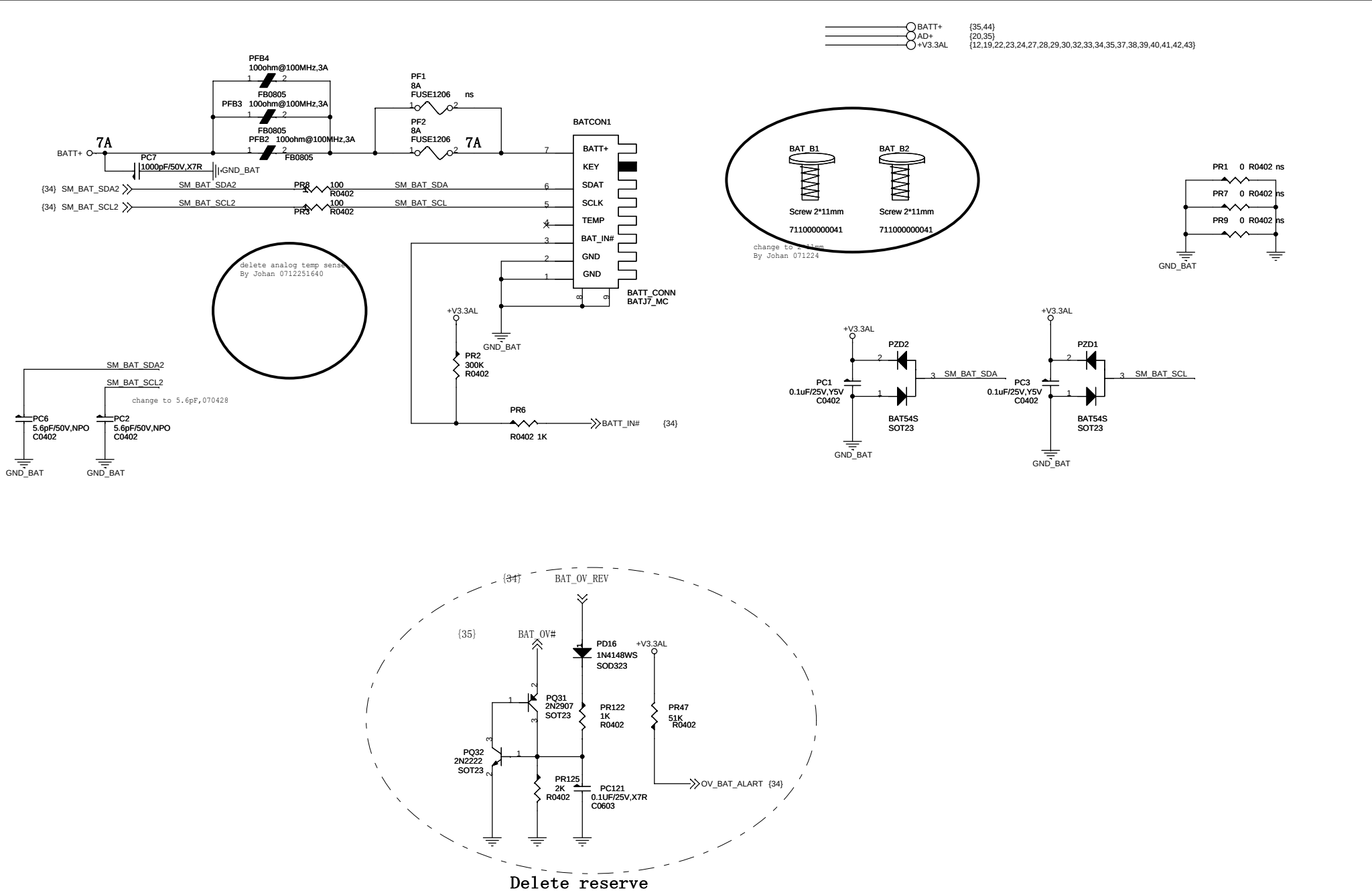

Delete reserve

Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	BATTERY IN	
Size A3	Project Name M42G	Rev A
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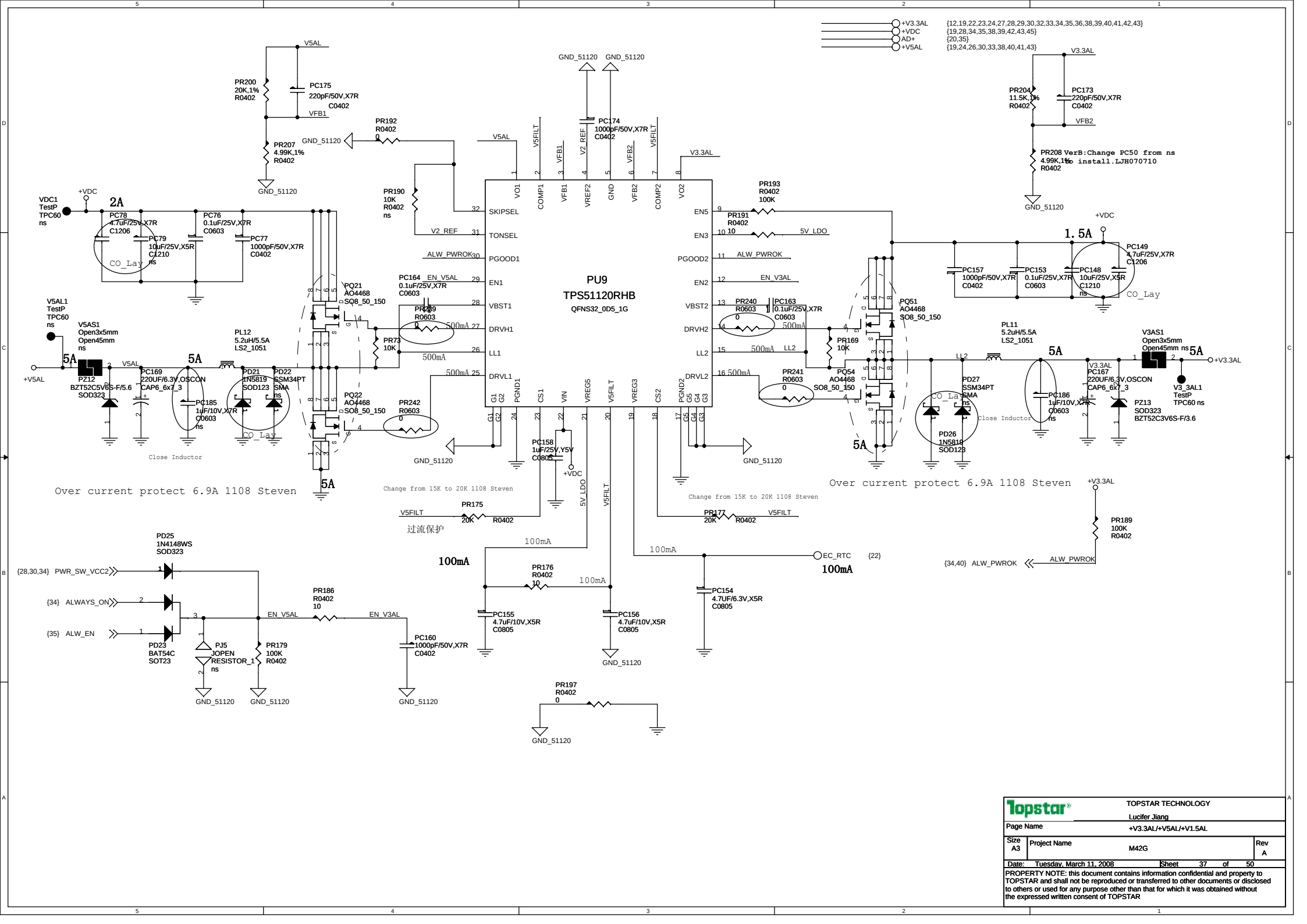
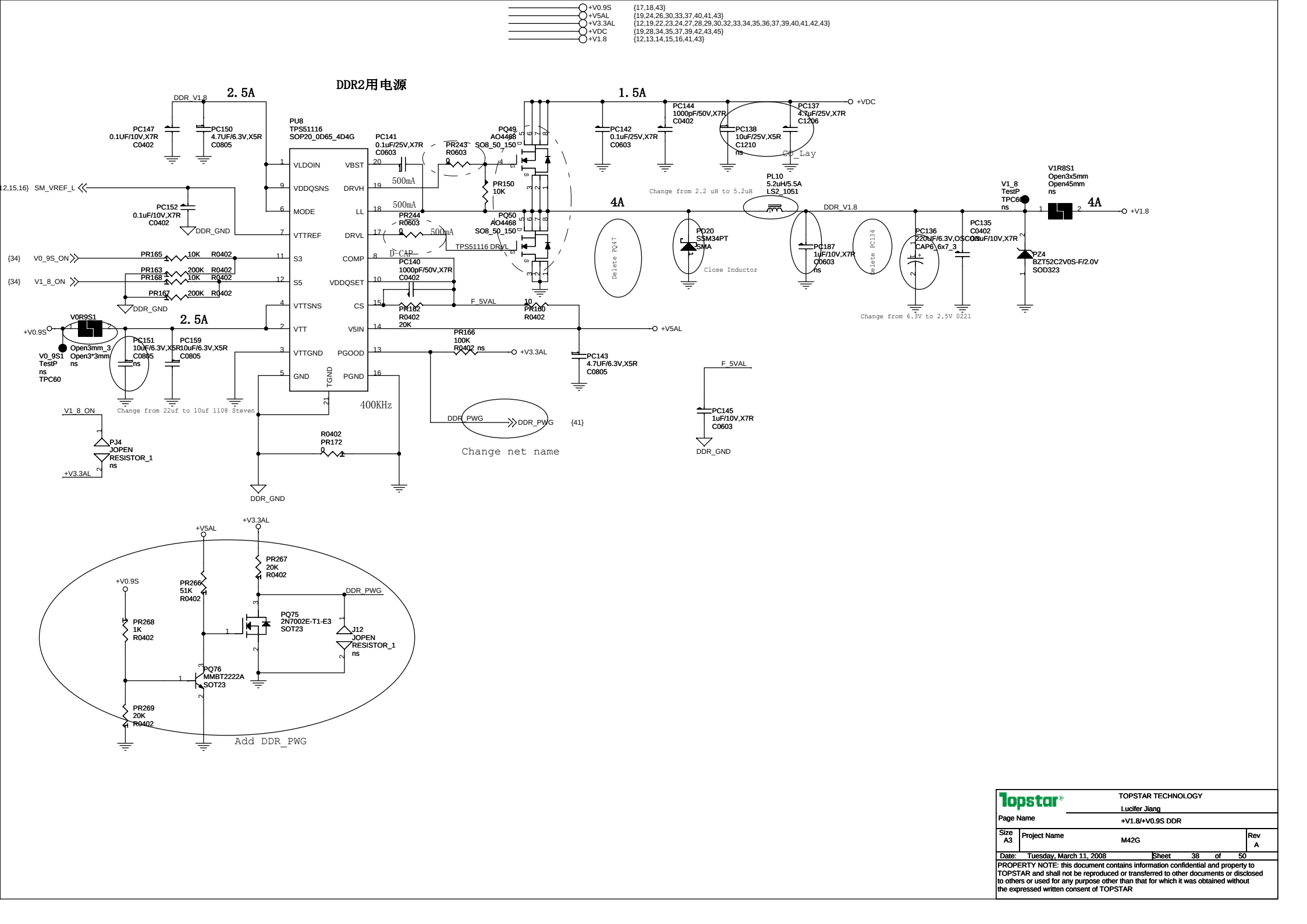


Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	+V3.3AL/+V5AL/+V1.5AL	
Size A3	Project Name M42G	Rev A
Date: Tuesday, March 11, 2008	Sheet 37 of 50	



Topstar	TOPSTAR TECHNOLOGY
	Lucifer Jiang
Page Name	+V1.8/+V0.9S DDR
Size A3 / Project Name	M42G / Rev A
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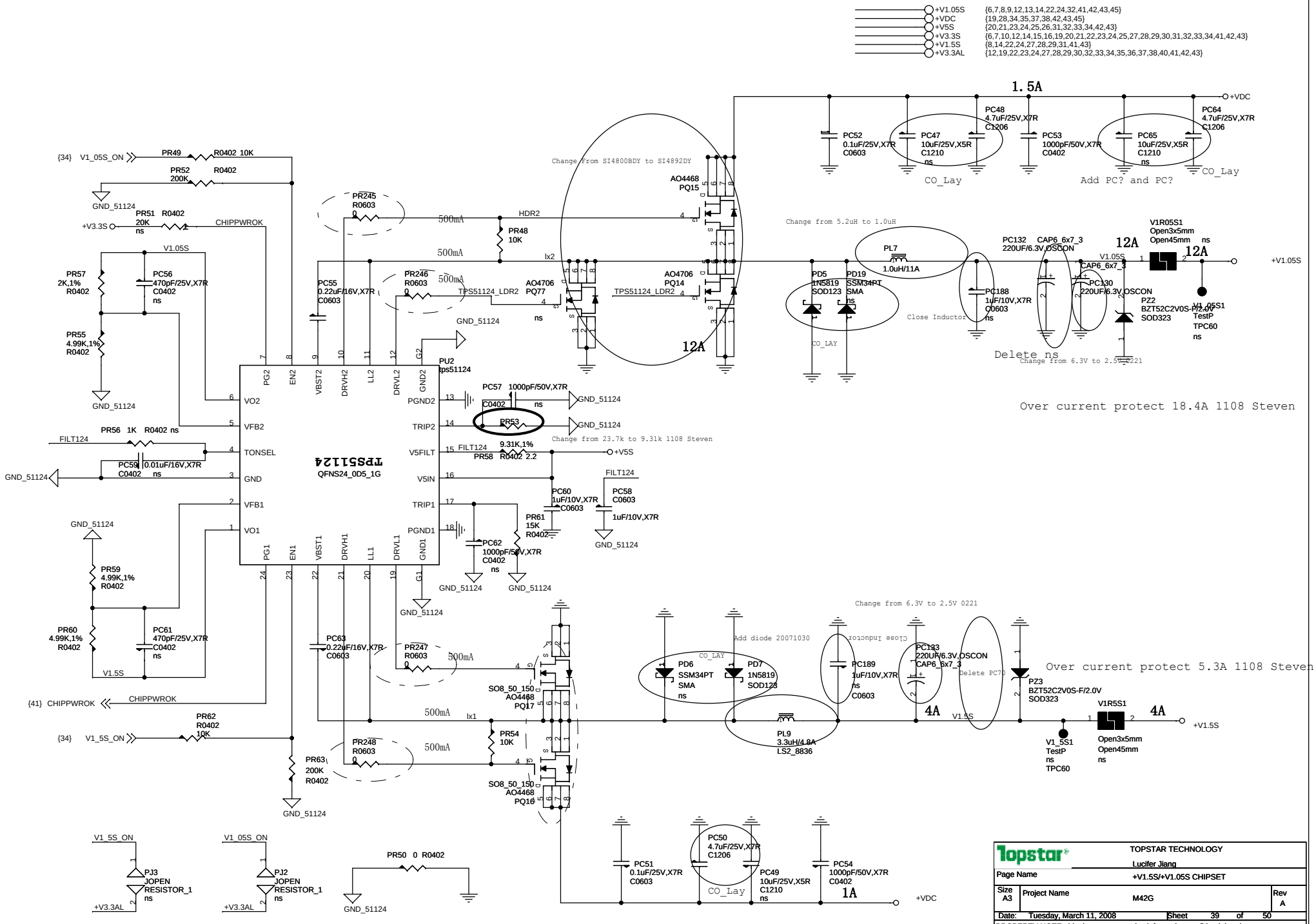
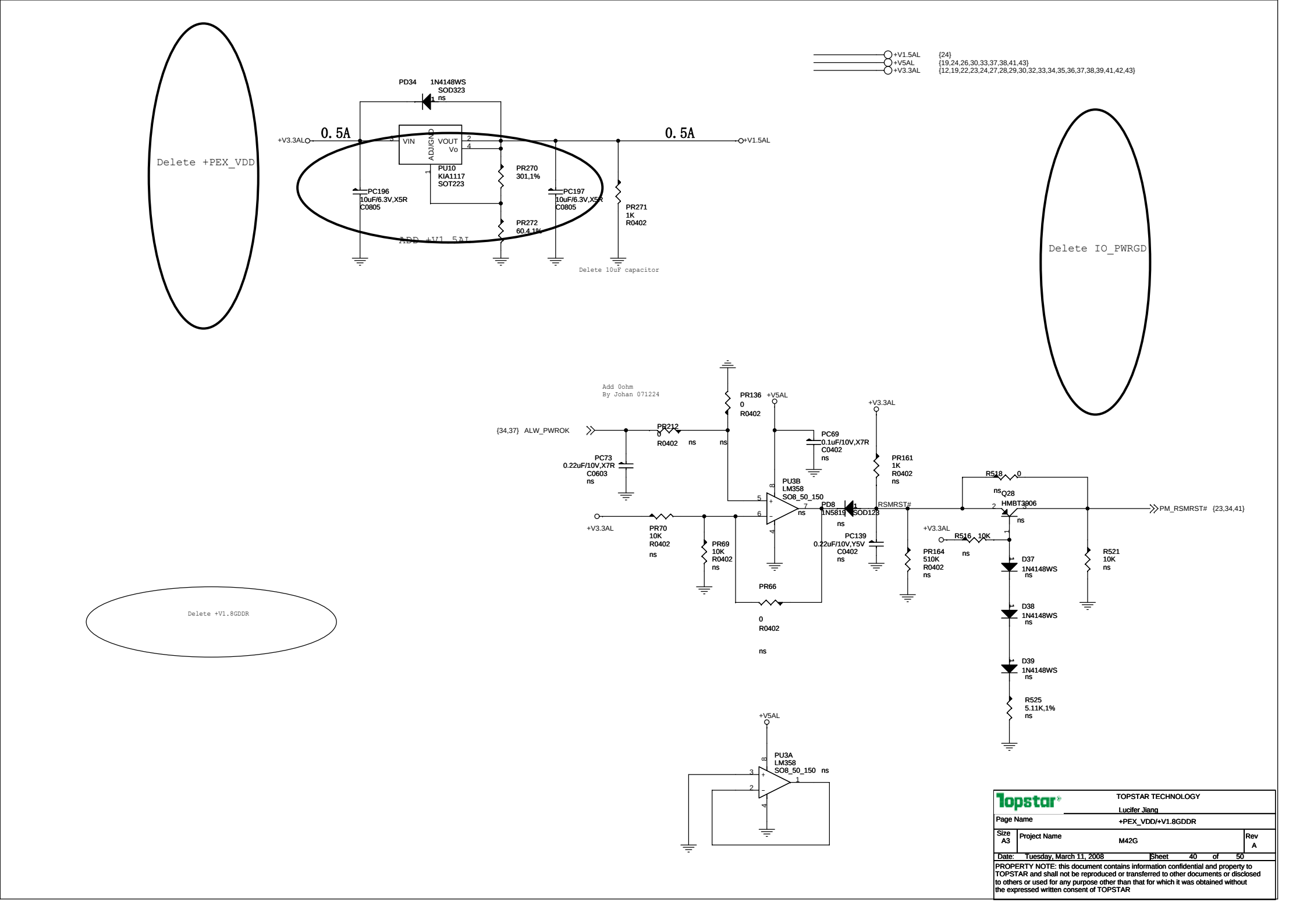


Topstar	TOPSTAR TECHNOLOGY
	Lucifer Jiang
Page Name	+V1.5S/+V1.05S CHIPSET
Size A3 / Project Name	M42G / Rev A
Date: Tuesday, March 11, 2008	Sheet 39 of 50


+V1.5AL {24}
+V5AL {19,24,26,30,33,37,38,41,43}
+V3.3AL {12,19,22,23,24,27,28,29,30,32,33,34,35,36,37,38,39,41,42,43}
Delete +PEX_VDD
PD34 1N4148WS SOD323 ns
0.5A
+V3.3AL
VIN
VOUT
Vo
ADJ/GND
PU10 KIA1117 SOT223
PR270 301,1%
PR272 60.4,1%
PC196 10uF/6.3V,X5R C0805
PC197 10uF/6.3V,X5R C0805
PR271 1K R0402
0.5A
+V1.5AL
ADD +V1.5AL
Delete 10uF capacitor
Delete IO_PWRGD
Add 0ohm By Johan 071224
PR136 0 R0402
+V5AL
+V3.3AL
{34,37} ALW_PWROK
PR212 0 R0402 ns
PC69 0.1uF/10V,X7R C0402 ns
PC73 0.22uF/10V,X7R C0603 ns
PR161 1K R0402 ns
PU3B LM358 SO8_50_150 ns
PD8 1N5819 SOD123 ns
RSMRST#
R518 0 ns
Q28 HMBT3906 ns
PM_RSMRST# {23,34,41}
+V3.3AL
PR70 10K R0402 ns
PR69 10K R0402 ns
PC139 0.22uF/10V,Y5V C0402 ns
R516 10K ns
PR164 510K R0402 ns
D37 1N4148WS ns
D38 1N4148WS ns
D39 1N4148WS ns
R521 10K ns
R525 5.11K,1% ns
PR66 0 R0402 ns
Delete +V1.8GDDR
+V5AL
PU3A LM358 SO8_50_150 ns
TOPSTAR TECHNOLOGY
Lucifer Jiang
Page Name +PEX_VDD/+V1.8GDDR
Size A3
Project Name M42G
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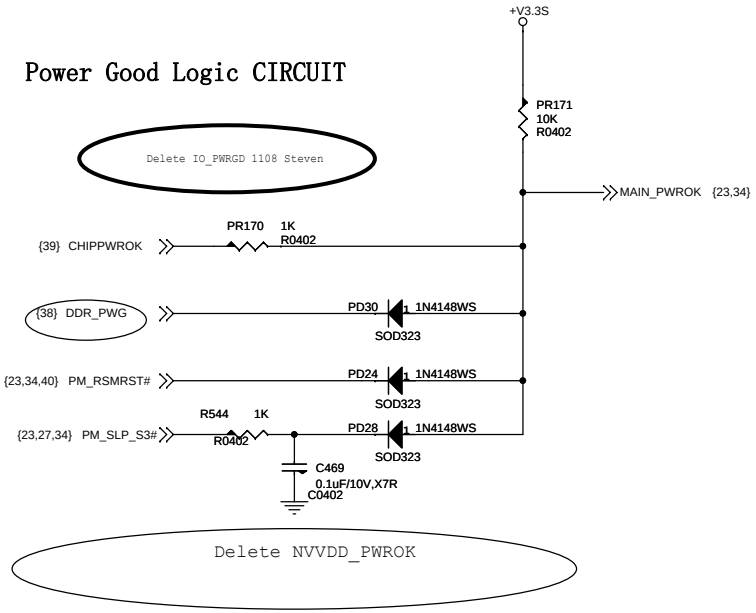
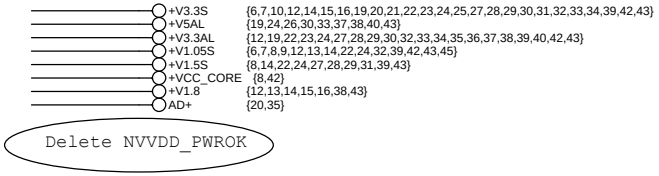
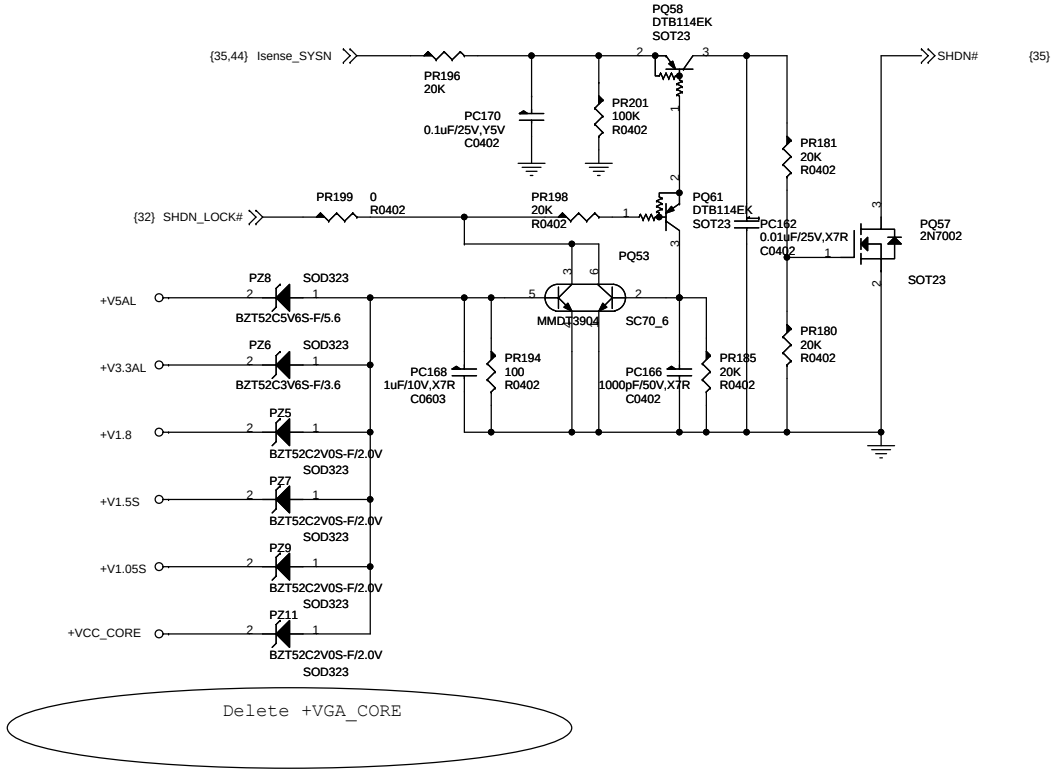
Power Good Logic CIRCUIT

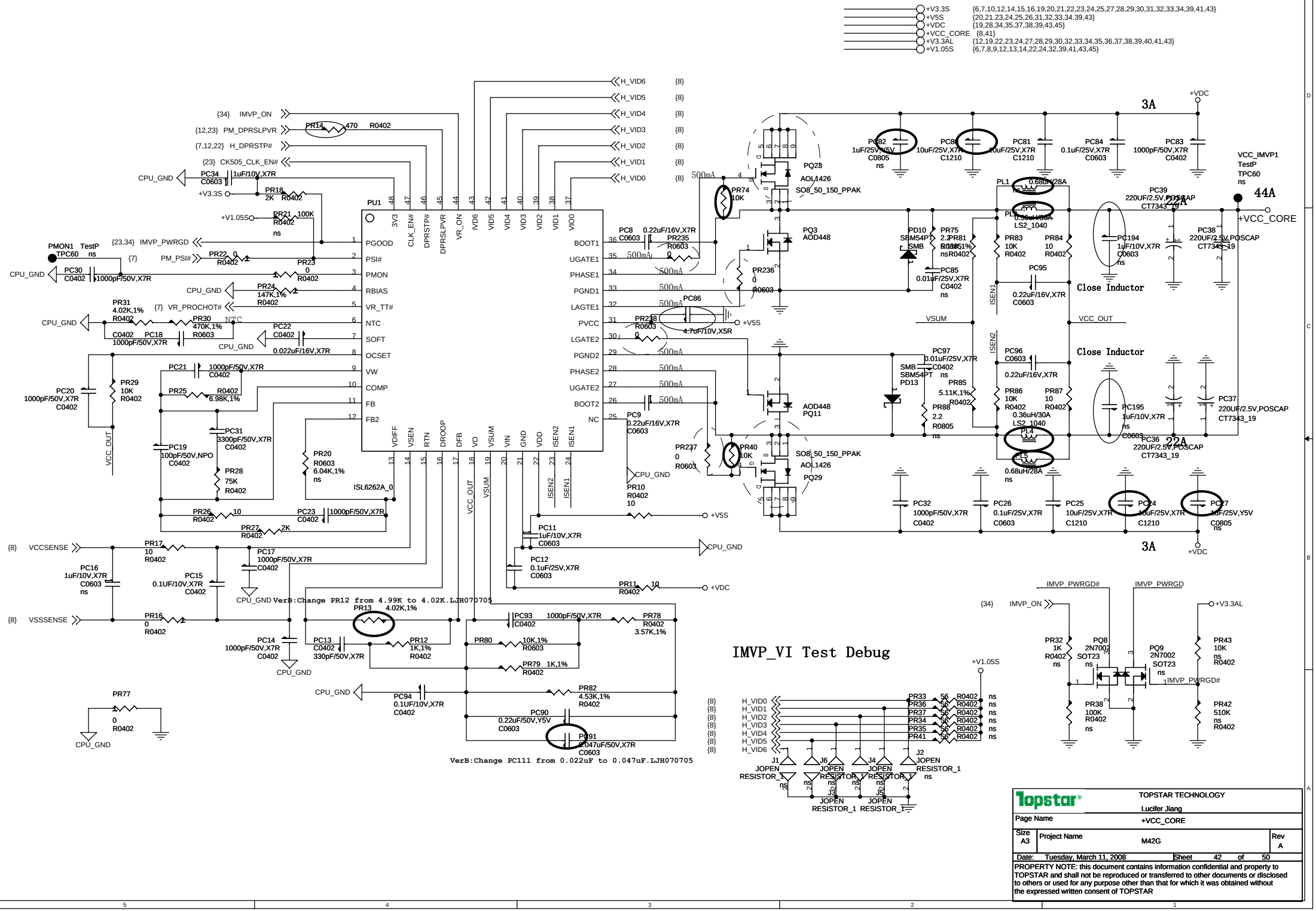




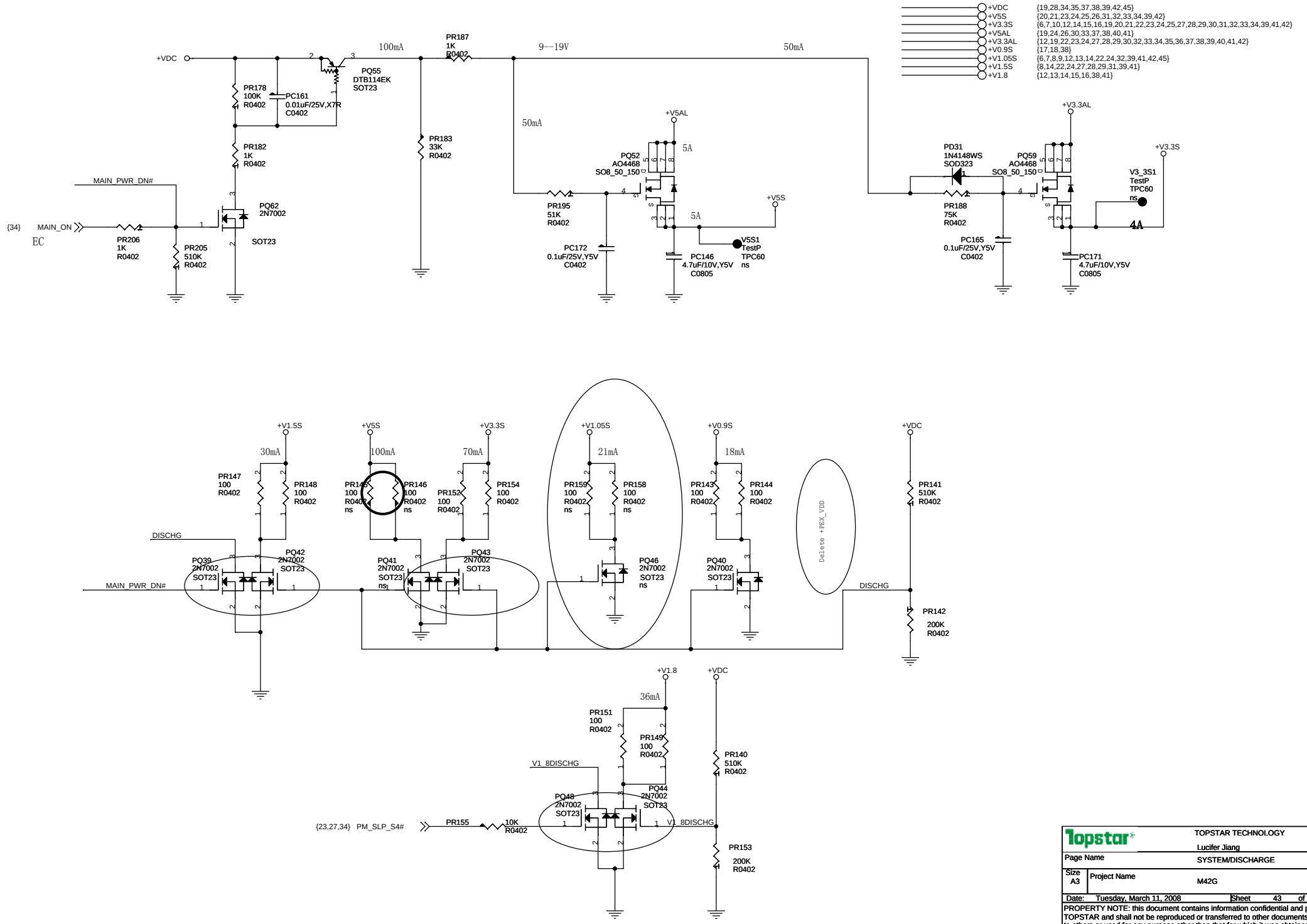
OVP CIRCUIT



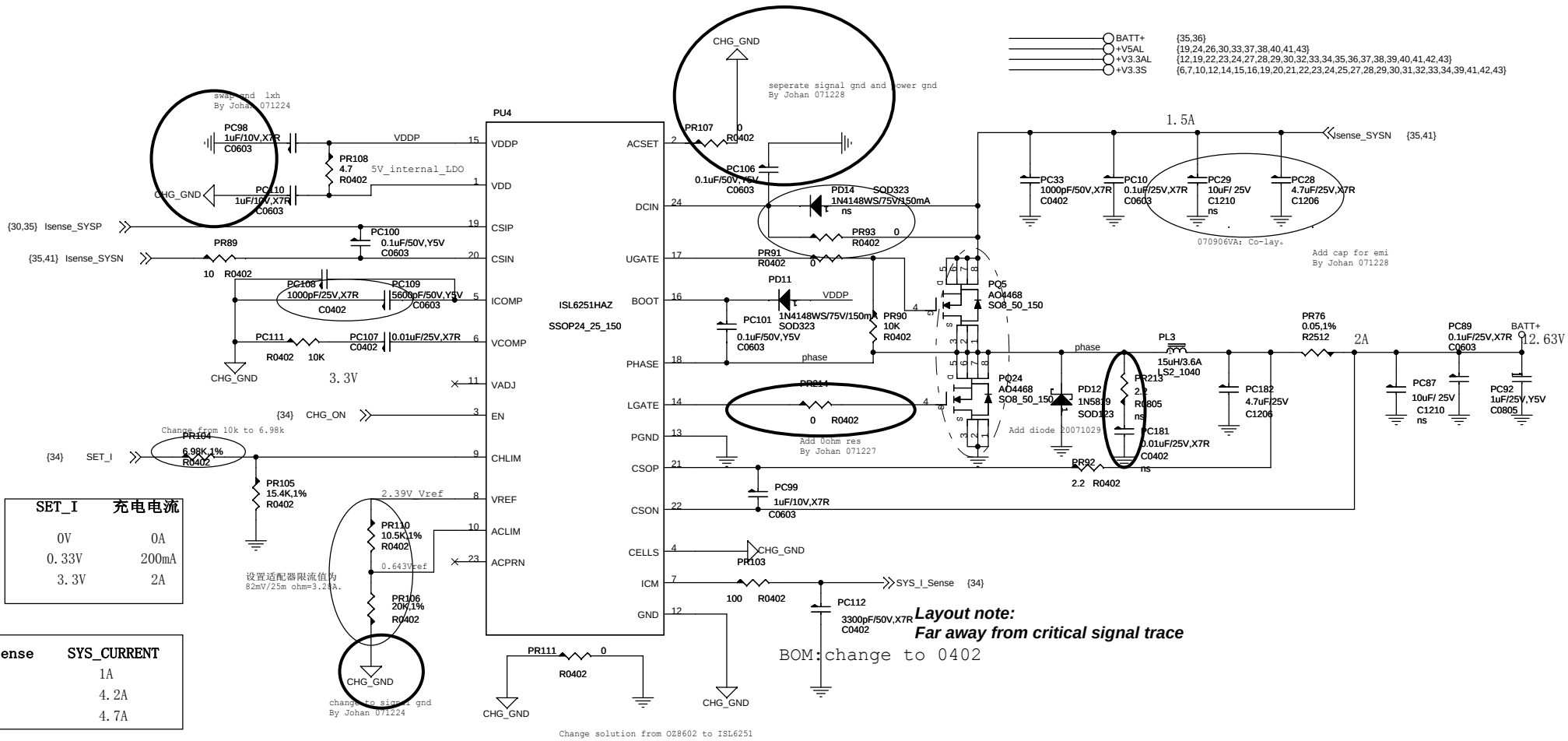
Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	Power Good Logic/OVP	
Size A3	Project Name M42G	Rev A
Date: Tuesday, March 11, 2008	Sheet 41 of 50	



Topstar	TOPSTAR TECHNOLOGY
	Lucifer Jiang
Page Name	+VCC_CORE
Size A3 / Project Name	M42G / Rev A
Date: Tuesday, March 11, 2008	Sheet 42 of 50



Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	SYSTEM/DISCHARGE	
Size A3	Project Name M42G	Rev A
Date: Tuesday, March 11, 2008	Sheet 43 of 50	

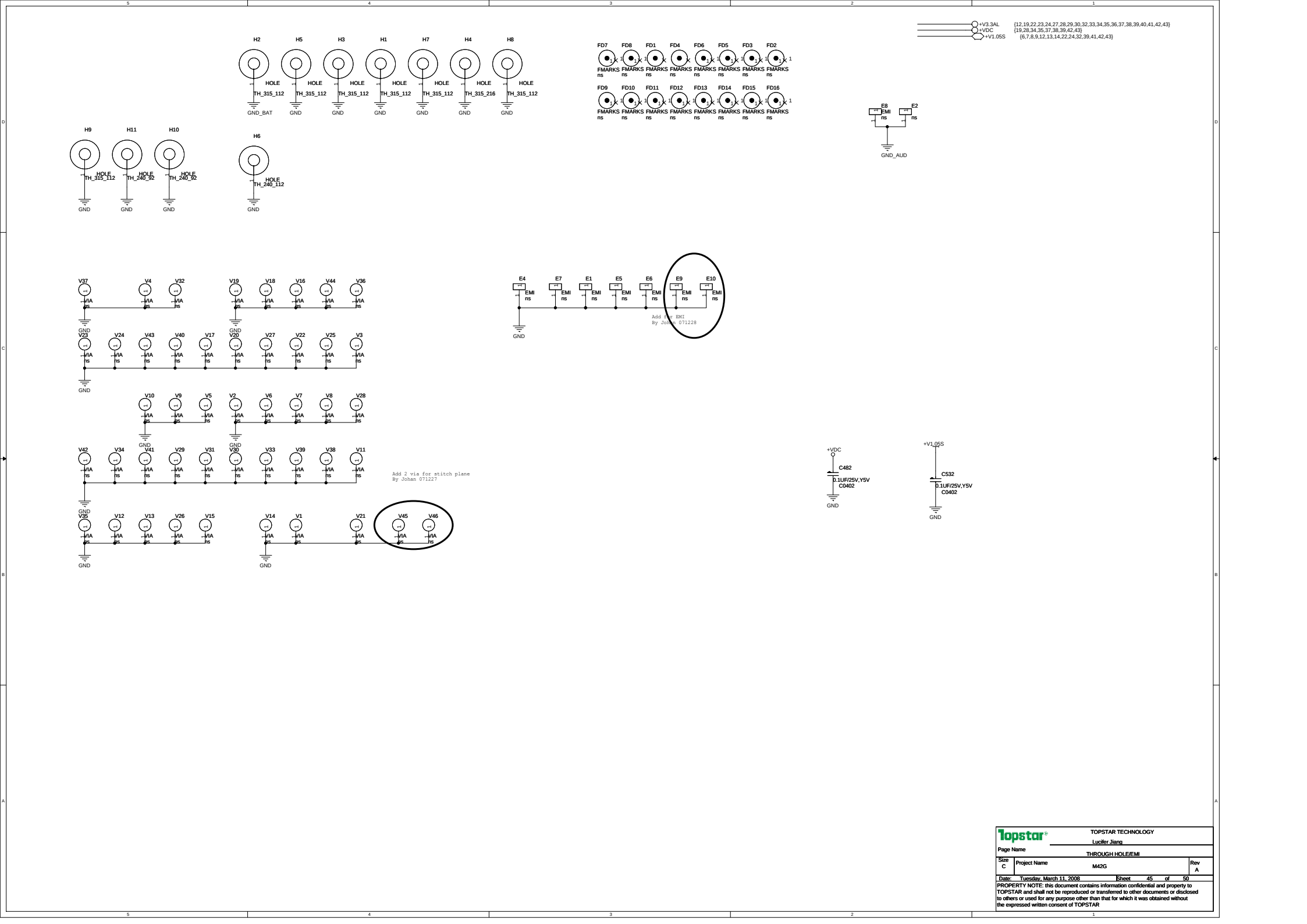


SET_I	充电电流
0V	0A
0.33V	200mA
3.3V	2A

SYS_I_Sense	SYS_CURRENT
400mV	1A
1.67V	4.2A
1.87V	4.7A

SYS_CURRENT	SYS_I_Sense	SYS_I_Trip
>3.6A	>1.8V	High
<3A	<1.5V	Low

Topstar	TOPSTAR TECHNOLOGY	
	Lucifer Jiang	
Page Name	CHARGER	
Size A3	Project Name M42G	Rev A
Date: Tuesday, March 11, 2008	Sheet 44 of 50	



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Page Name	Lucifer Jiang	
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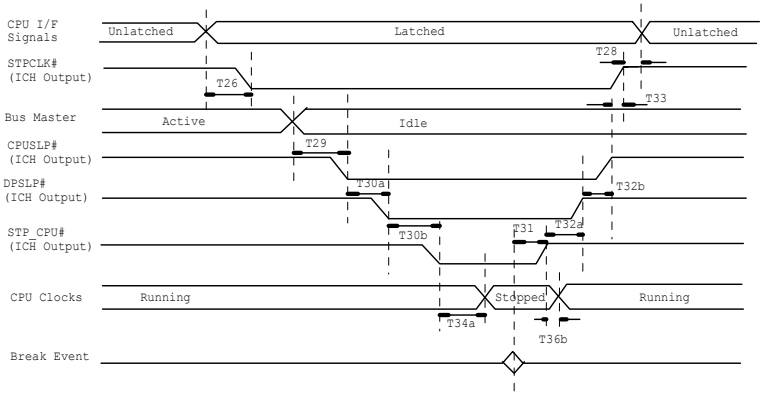
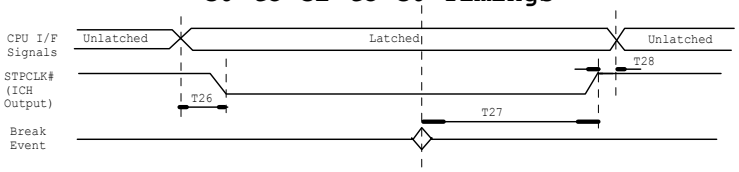
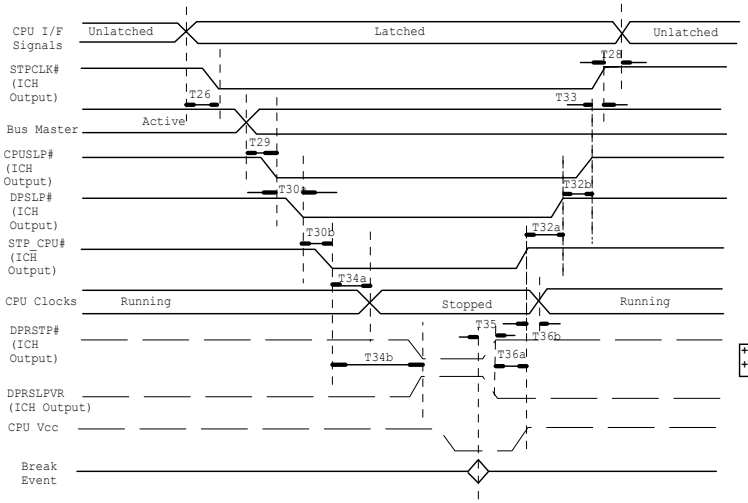
C0 to C3 to C0 Timings



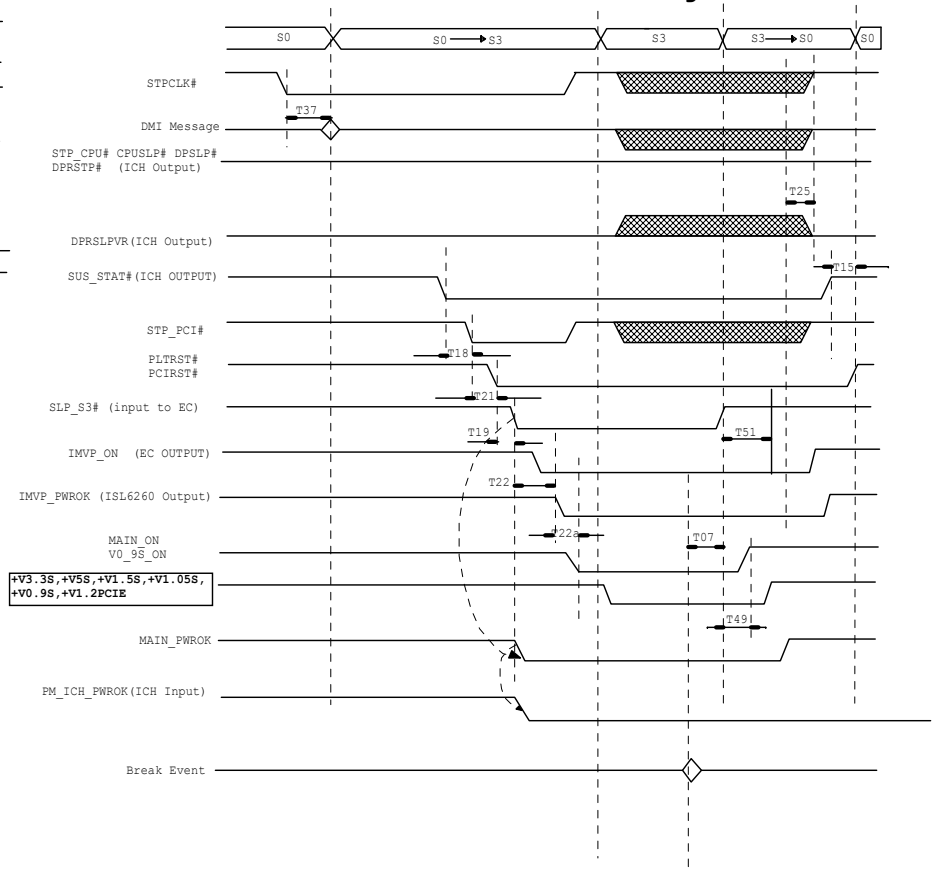
C0 to C2 to C0 Timings



C0 to C4 to C0 Timings



S0 to S3 to S0 Timings



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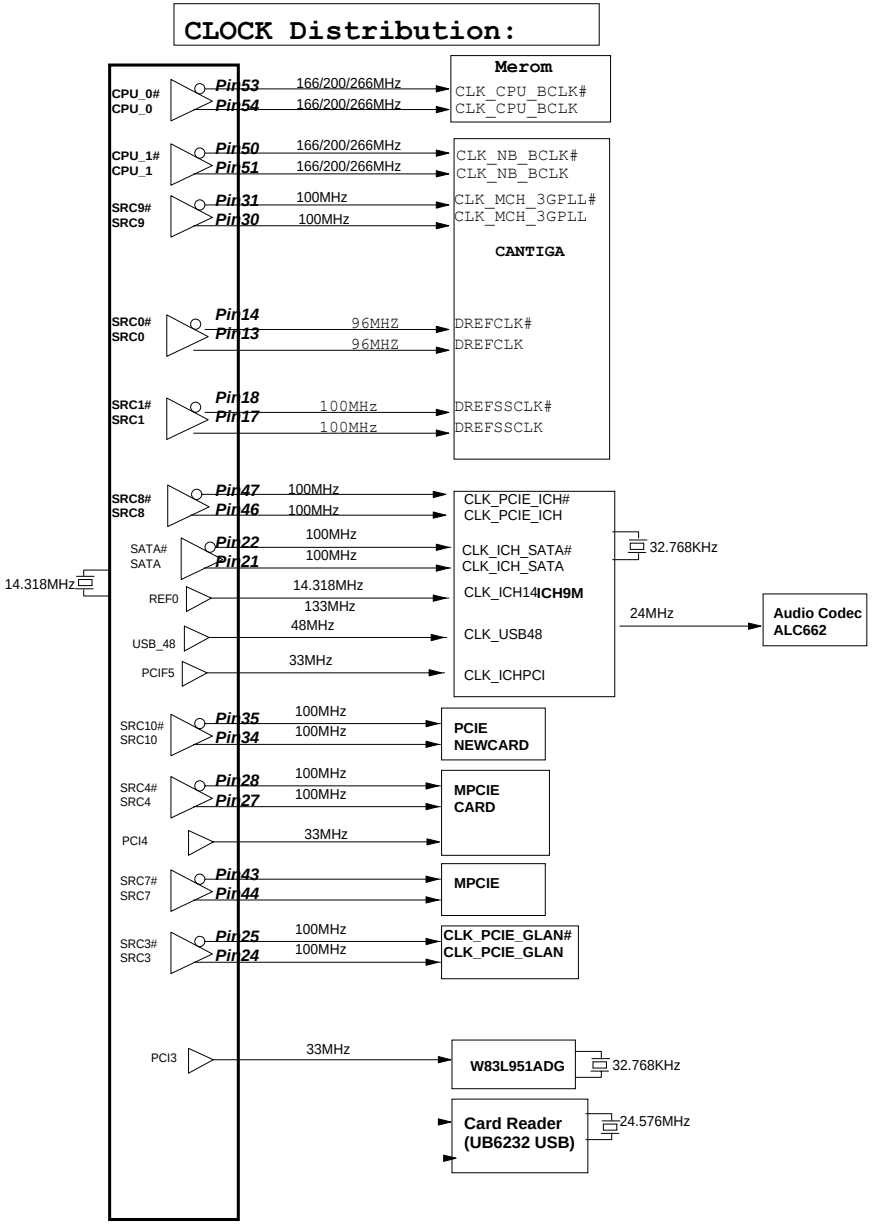
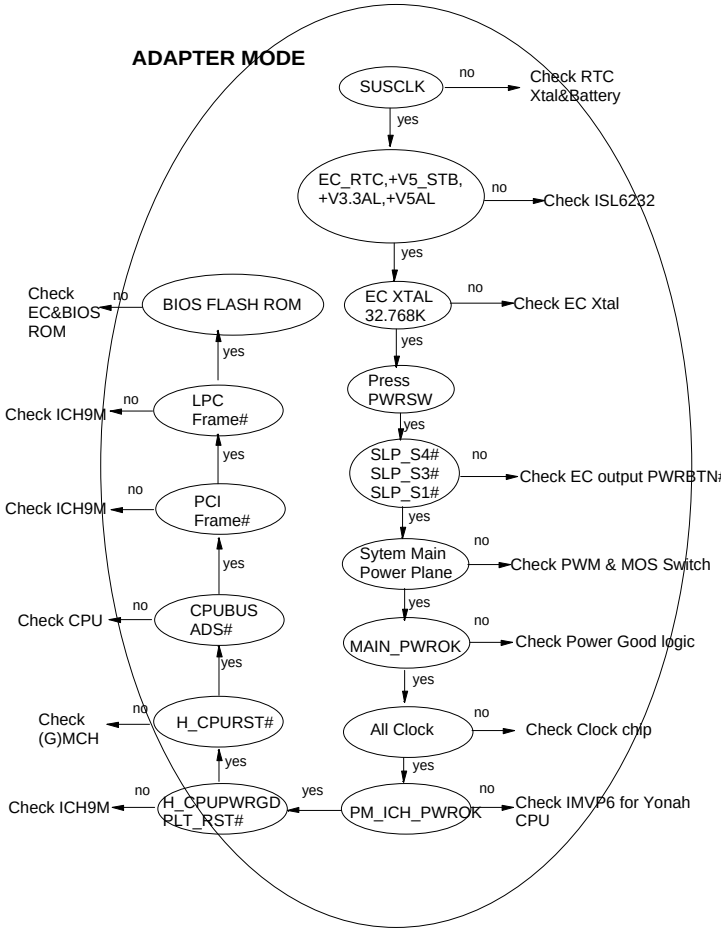
CLOCK Distribution:



CY28548_TSSOP-56P



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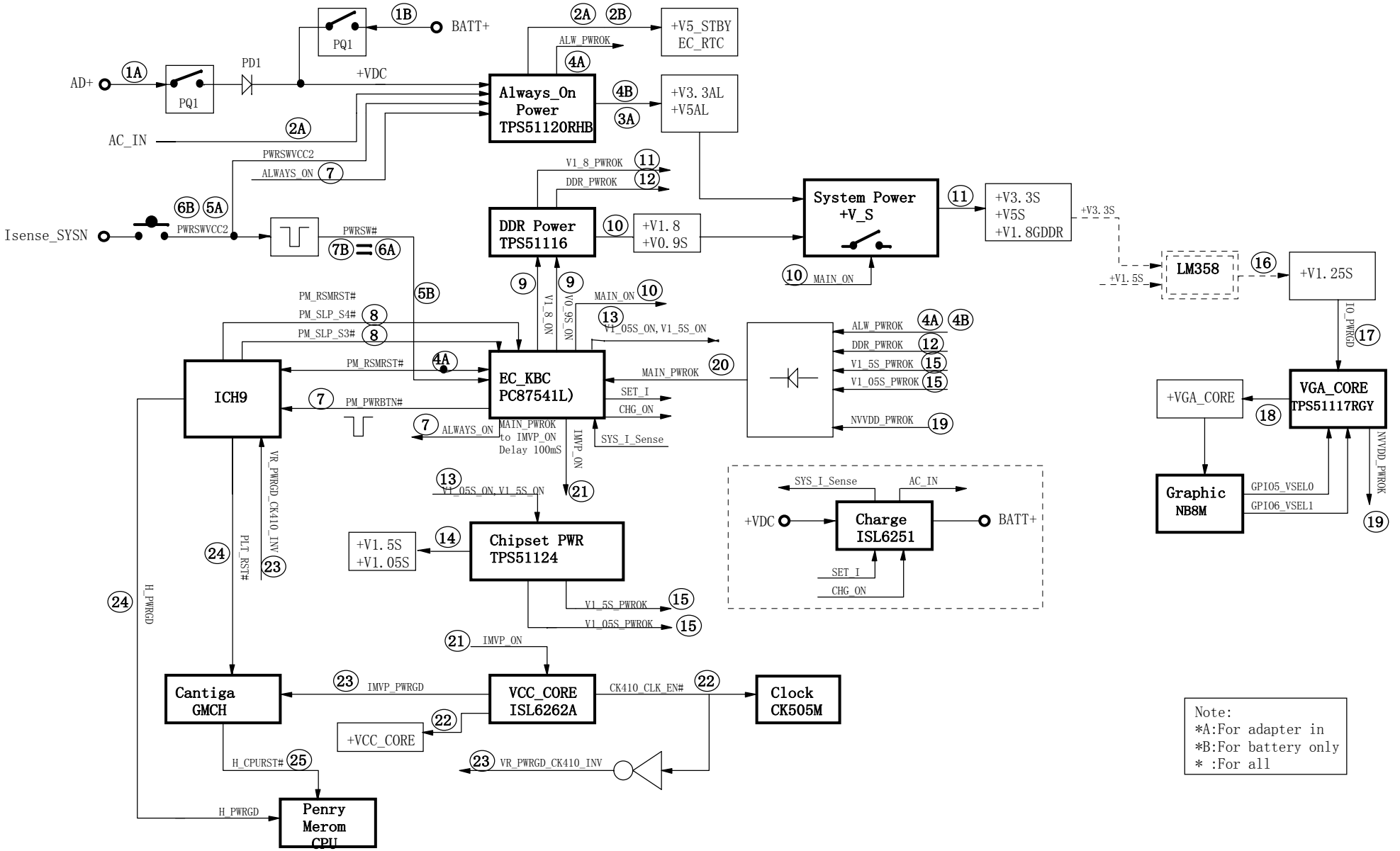

Note:
*A:For adapter in
*B:For battery only
* :For all

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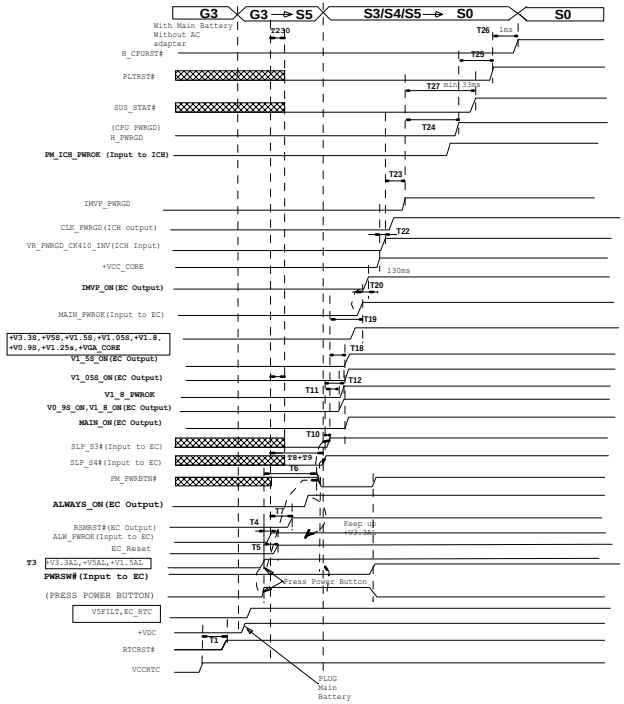
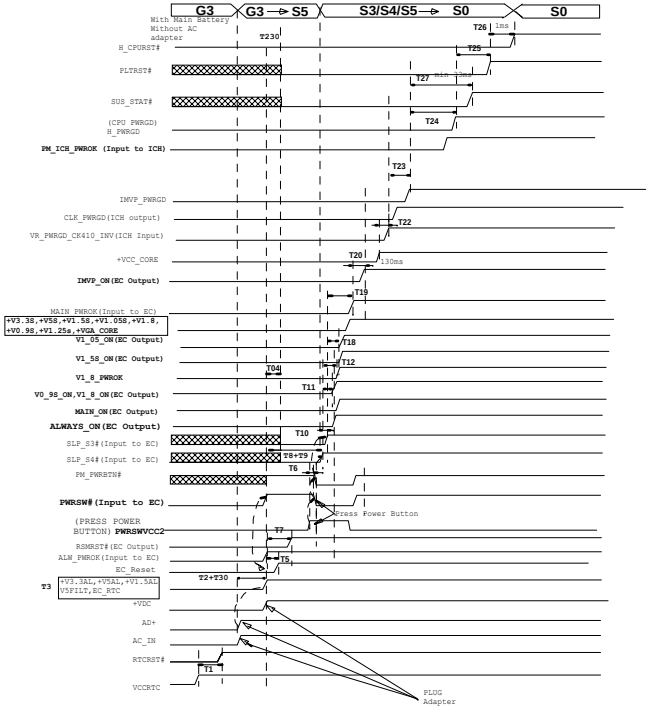
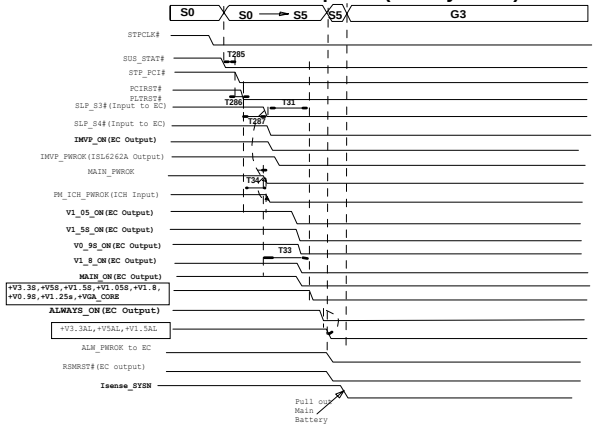
Power On Sequence(Battery mode)



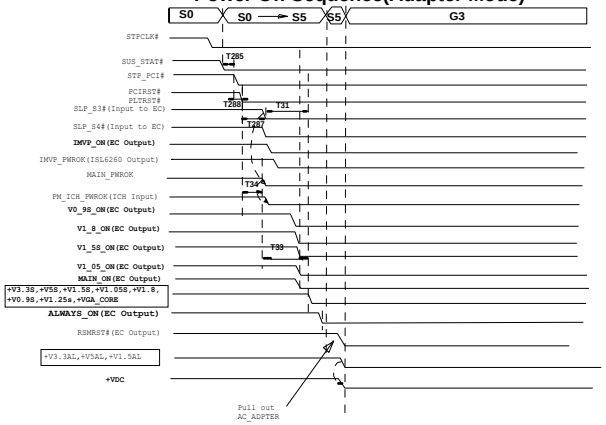
Power On Sequence(Adapter mode)



Power Off Sequence(Battery Mode)



Power Off Sequence(Adapter Mode)



T3 V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0.7 V

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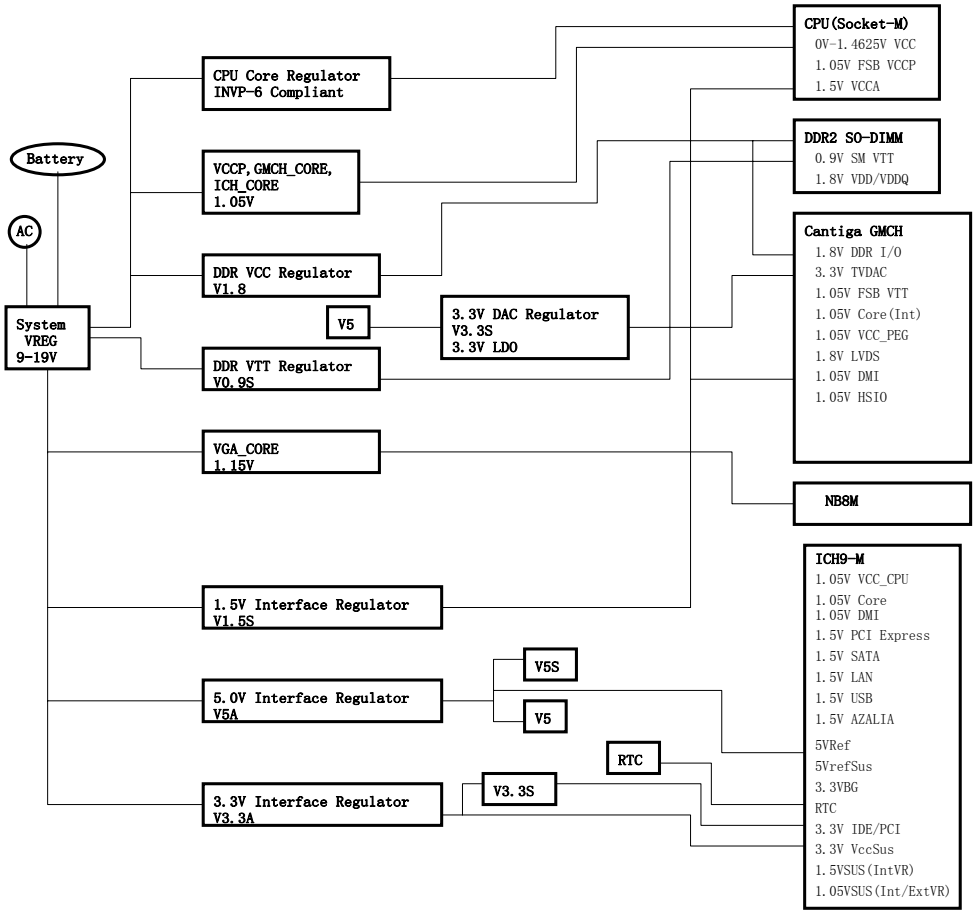
POWER Distribution



R0.92

0V-1.4625V VCC

USB
V5A&V3.3A

SATA
V3.3S&V5S

BLUETOOTH
V3.3S

SPI
V3.3S

LVDS
System VREG(9-12.6V)

CK505-M
V3.3S

SMC/KBC
V3.3A

Azalia
V5,V3.3S

Mini-PCI Express
V1.5S +1.5V
V3.3A +3.3Vaux
V3.3S +3.3V-3.0A

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