ZZZ PCB@

PCB EH5A1 LA-H441P LS-G521P 02
DAZ2KJ00101

ZZZ LOGO@

ROYALTY HDMI W/LOGO+HDCP
RO0000003HM

ZZZ X4E@

SMT EMC AH441 EH5A1
X4EAGHBOL01

**MP**

UC1 U42_SR3W0@

S IC FJ8067703282227 SR3W0 Y0 2.2G ABO!
SA0000BKN60

**QS**

UC1 U22_QNZU@

S IC FJ8067702739769 QNZU H0 2.3G BGA
SA0000BLH20

UC1 U23e_QNMU@

S IC FH8067703037315 QNMU J1 2.3G BGA
SA0000BVB00

# Compal Confidential

# Raticate_KL MB Schematic Document

## LA-H441P

## Rev: 1A

## 2018.11.28



| | | | |
|---|---|---|---|
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| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



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Title: Cover Sheet

Size: Custom | Document Number: Raticate_KL M/B LA-H441P | Rev: 0.1

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HDMI Conn.


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DDI1
HDMI x 4 lanes

eDP

page 28

eDP

DDI

Intel Kabylake U

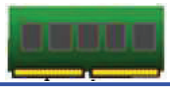
Kabylake U
Kabylake PCH-LP(MCP)
(KBL-U_2+2)
(KBL-RU_4+2)
(KBL-U_2+3e)
Processor

Quad Core + GT2
Dual Core + GT2

5W
528pin BGA
page 07~18

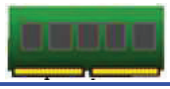
Memory BUS
Dual Channel
1.2V DDR4 2133/2400

260pin DDR4-SO-DIMM X1



page 19

260pin DDR4-SO-DIMM X1



page 20

Nvidia N16S-GTR /
N17S-G0
with GDDR5 x2
page 21~27

page 31

PCIe 3.0 x 4
8GT/s
port 1-4

PCIE 3.0 x4
8GT/s
Port 9-12

Flexible IO
Base-U PCIE2.0
Premium-U PCIE3.0

USB 3.0
conn x1
USB3 port 1
USB2 port 1

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USB 2.0
conn x2
USB2 port3,4
on Sub/B

page 35

CMOS
Camera
USB2 port 7

page 28

USB TypeC
conn x1
USB3 port 2,3
USB2 port2



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USBx8 48MHz

HD Audio 3.3V 24MHz

NGFF
WLAN
USB2 port 10

PCIe 1.0
2.5GT/s
port 6
page 31

PCIe 1.0
2.5GT/s
port 5

LAN(GbE)
Realtek 8411B
page 30

SD conn.

RJ45 conn.

SATA3.0
6.0 Gb/s
port 7
(SATA0)

SATA HDD
Conn.

page 33

VINAFIX.COM

SPI

SPI ROM
64Mb page 9

HDA Codec
ALC255 page 32

Touch
Screen
9USB2 port 6
page 28

LPC/eSPI BUS
CLK=24MHz

ENE
KB9022
page 36

Int. Speaker
page 32

Int. DMIC
on Camera
page 28

UAJ
on Sub/B
page 35

Int.KBD

page 37

Touch Pad
PS2 (from EC) / I2C (from SOC)
USB2 port 5 (FP)

page 37

RTC CKT.
page 15

Power On/Off CKT.
page 38

DC/DC Interface CKT.
page 40

Power Circuit DC/DC
page 41~54

Fan Control
page 39

Sub Board
LS-G521
IO/B
page 35

| | | | |
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| | |
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| Title | Block Diagrams |
| Size: Custom | Document Number: Raticate KL M/B LA-H441P |
| Rev | 0.1 |
| Date: Friday, November 30, 2018 | Sheet 2 of 57 |

## Board ID Table for AD channel

| | |
|---|---|
| Vcc | 3.3V +/- 5% |
| Ra | 100K +/- 1% |

| Board ID | Rb | $V_{BID}$ min | $V_{BID}$ typ | $V_{BID}$ max | EC AD3 | PCB Revision |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 V | 0 V | 0.300 V | 0x00 - 0x13 | 0.1(EVT) |
| 1 | 12K +/- 1% | 0.347 V | 0.345 V | 0.360 V | 0x14 - 0x1E | 0.2(DVT) |
| 2 | 15K +/- 1% | 0.423 V | 0.430 V | 0.438 V | 0x1F - 0x25 | 1.0(PVT) |
| 3 | 20K +/- 1% | 0.541 V | 0.550 V | 0.559 V | 0x26 - 0x30 | 1.A(MP) |
| 4 | 27K +/- 1% | 0.691 V | 0.702 V | 0.713 V | 0x31 - 0x3A | |
| 5 | 33K +/- 1% | 0.807 V | 0.819 V | 0.831 V | 0x3B - 0x45 | |
| 6 | 43K +/- 1% | 0.978 V | 0.992 V | 1.006 V | 0x46 - 0x54 | |
| 7 | 56K +/- 1% | 1.169 V | 1.185 V | 1.200 V | 0x55 - 0x64 | |

## Power State

| STATE \ SIGNAL | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|---|---|---|---|---|---|---|---|
| S0 (Full ON) | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S3 (Suspend to RAM) | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | ON | OFF | OFF | OFF |

## BOM Structure Table

### BOM Option Table

| Item | BOM Structure |
|---|---|
| Unpop | @ |
| Connector | CONN@ |
| Acer BYOC | BYOC@ / NBYOC@ |
| CODEC | 255@/256@ |
| EC Mode Select | LPC@ / ESPI@ |
| For Intel CMC | CMC@ |
| LAN Mode Select | SWR@ / LDO@ |
| EMI requirement | EMI@ / @EMI@ |
| ESD requirement | ESD@ / @ESD@ |
| RF requirement | @RF@ |
| CPU Selection | U42@/U22@ |
| DGPU Serial Select | N16X@/N17S@ |
| TPM/Only BIOS ROM | TPM@/SPI@ |
| Finger Print | FP@/FPEMC@/ETU@ |
| Finger print power | FP3V@/FP5V@ |
| UMA or DGPU | UMA@/VGA@ |
| | |

### BOM Option Table

| Item | BOM Structure |
|---|---|
| MB Stage | EVT@/DVT@/PVT@/MP@ |
| N16SGTR or N17SG1/G0 | N16SGTR@/N17SG1@/N17SG0@ |
| G Sensor | GSEN@ |
| For over 3 cell battery | 3S@ |
| BOM Select | X76@ |
| VRAM BOM Select | X76793BOL01@~04@/X7605@/X7608@ |
| VPRO SKU | VPRO@ |
| RTC | RTC@/RTC_CHG@ |
| X'tal 24MHz | U22@/U42@ |
| | |
| | |
| | |
| | |
| CPU Code | U42_SR3W0@<br>U22_QNZU@<br>U23e_QNMU@ |

## Voltage Rails

| Power Plane | Description | S0 | S3 | S4/S5 |
|---|---|---|---|---|
| +19V_VIN | Adapter power supply | N/A | N/A | N/A |
| +12.6V_BATT | Battery power supply | N/A | N/A | N/A |
| +19VB | AC or battery power rail for power circuit. | N/A | N/A | N/A |
| +VCC_CORE | Processor IA Cores Power Rail | ON | OFF | OFF |
| +VCC_GT | Processor Graphics Power Rails | ON | OFF | OFF |
| +VCC_SA | System Agent power rail | ON | OFF | OFF |
| +0.6VS_VTT | DDR +0.6VS power rail for DDR terminator . | ON | OFF | OFF |
| +1.05VALW_PRIM | +1.05V Always power rail | ON | ON | ON*1 |
| +1.05V_VCCSTU | Sustain voltage for processor in Standby modes | ON | ON | OFF |
| +VCCIO | CPU IO power rail | ON | OFF | OFF |
| +1.05VS_VCCSTG | +1.0VALW_PRIM Gated version of VCCST | ON | OFF | OFF |
| +1.2V_VDDQ | DDR4 +1.2V Power Rail | ON | ON | OFF |
| +1.8VALW_PRIM | +1.8V Always power rail | ON | ON | ON*1 |
| +1.8VS | System +1.8V power rail | ON | OFF | OFF |
| +3VLP | +19VB to +3VLP power rail for suspend power | ON | ON | ON |
| +3VALW | System +3VALW always on power rail | ON | ON | ON*1 |
| +3VS | System +3V power rail | ON | OFF | OFF |
| +5VALW | +5V Always power rail | ON | ON | ON |
| +5VS | System +5V power rail | ON | OFF | OFF |
| +RTCVCC | RTC Battery Power | ON | ON | ON |
| +1.05VS_1.0VSDGPU | +1.05VS power rail for N16X/ +1.0VS power rail for N17S | ON*2 | OFF | OFF |
| +1.35VSDGPU | +1.35VS power rail for GPU | ON*2 | OFF | OFF |
| +3VS_1.8VSDGPU_AON | +3VS power rail for N16X/ +1.8VS power rail for N17S(AON) | ON*2 | OFF | OFF |
| +3VS_1.8VSDGPU_MAIN | +3VS power rail for N16X/ +1.8VS power rail for N17S(MAIN) | ON*2 | OFF | OFF |
| +VGA_CORE | Core power for descrete GPU | ON*2 | OFF | OFF |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.
ON*2 power plane is ON when DGPU turn on

## 43 level BOM table

| 43 Level | Description | BOM Structure |
|---|---|---|
| 431AGHBOL01 | SMT MB AH441 EH5A1 I38130U UMA HDMI | DA@/U42_QP8K@/U42@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/UMA@/EVT@/X4E@/RTC@/FP@/FP3V@ |
| 431AGHBOL02 | SMT MB AH441 EH5A1 I37020UF N17SG0 HDMI | DA@/U22_QNZU@/U22@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/VGA@/N17S@/N17SG0@/X7608@/EVT@/X4E@/RTC@/FP@/FP3V@ |
| 431AGHBOL03 | SMT MB AH441 EH5A1 QNMU N17SG0 HDMI | DA@/U23e_QNMU@/U22@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/VGA@/N17S@/N17SG0@/X76793BOL01@/EVT@/X4E@/RTC@/FP@/FP3V@ |
| 431AGHBOL04 | SMT MB AH441 EH5A1 I38130U N17SG0 HDMI | DA@/U42_QP8K@/U42@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/VGA@/N17S@/N17SG0@/X76793BOL02@/EVT@/X4E@/RTC@/FP@/FP3V@ |
| 431AGHBOL05 | SMT MB AH441 EH5A1 QNZU UMA FP HDMI | PCB@/U22_QNZU@/U22@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/UMA@/PVT@/X4E@/RTC@/FP@/FP3V@/SPI@ |
| 431AGHBOL06 | SMT MB AH441 EH5A1 QNMU UMA FP HDMI | PCB@/U23e_QNMU@/U22@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/UMA@/PVT@/X4E@/RTC@/FP@/FP3V@/SPI@ |
| 431AGHBOL07 | SMT MB AH441 EH5A1 I38130 UMA FP HDMI | PCB@/U42_SR3W0@/U42@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/UMA@/PVT@/X4E@/RTC@/FP@/FP3V@/SPI@ |
| 431AGHBOL08 | SMT MB AH441 EH5A1 QNZU N17G0 FP HDMI | PCB@/U22_QNZU@/U22@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/VGA@/N17S@/N17SG0@/X76793BOL02@/PVT@/X4E@/RTC@/FP@/FP3V@/SPI@ |
| 431AGHBOL09 | SMT MB AH441 EH5A1 QNMU N17G0 FP HDMI | PCB@/U23e_QNMU@/U22@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/VGA@/N17S@/N17SG0@/X76793BOL02@/PVT@/X4E@/RTC@/FP@/FP3V@/SPI@ |
| 431AGHBOL10 | SMT MB AH441 EH5A1 I38130 N17G0 FP HDMI | PCB@/U42_SR3W0@/U42@/CHG@/3S@/LPC@/CMC@/255@/BYOC@/LDO@/VGA@/N17S@/N17SG0@/X76793BOL01@/PVT@/X4E@/RTC@/FP@/FP3V@/SPI@ |
| | | |



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Title: Notes List

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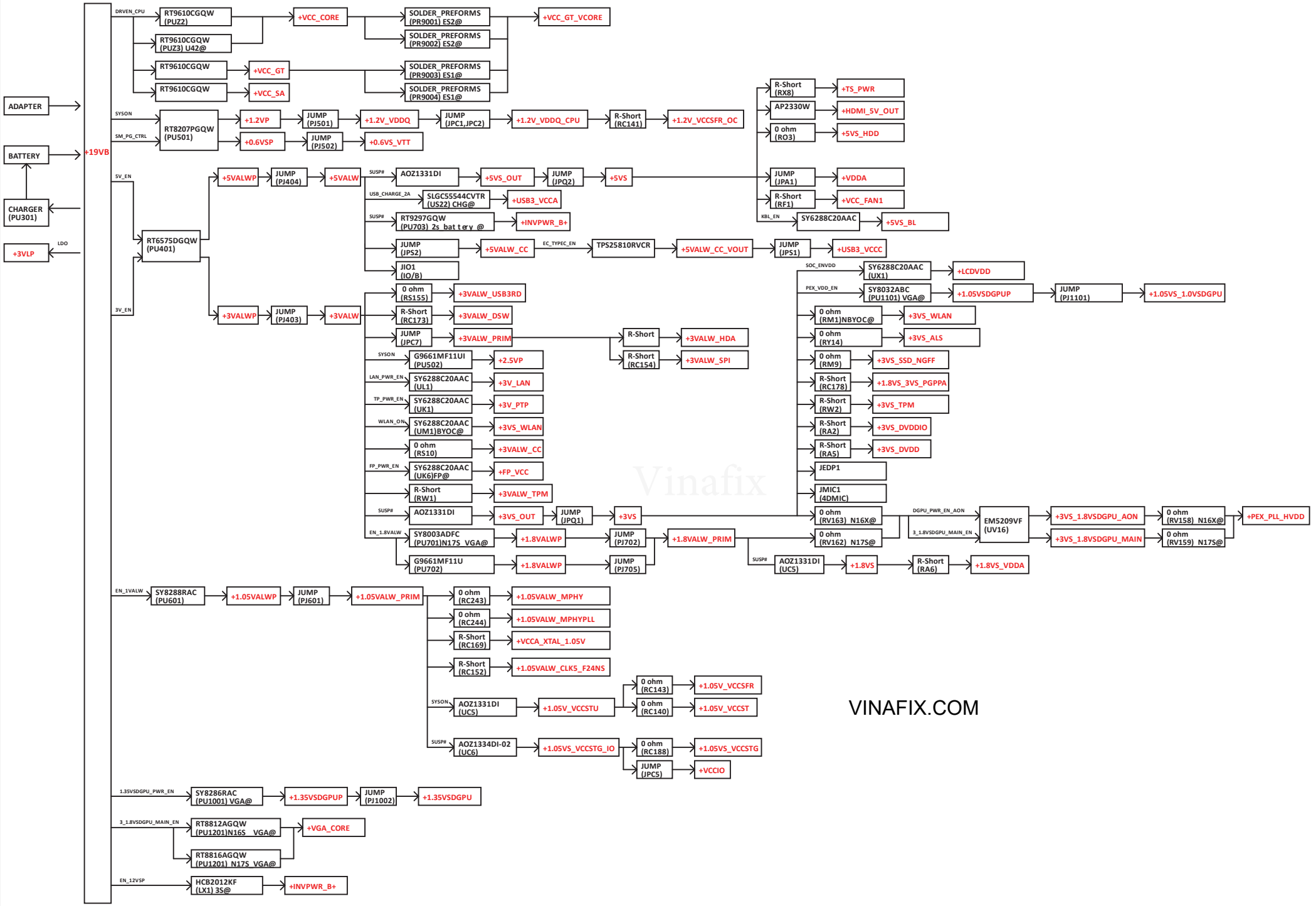




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|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2018/08/24 | Deciphered Date 2018/08/24 | Title: Power Rail |
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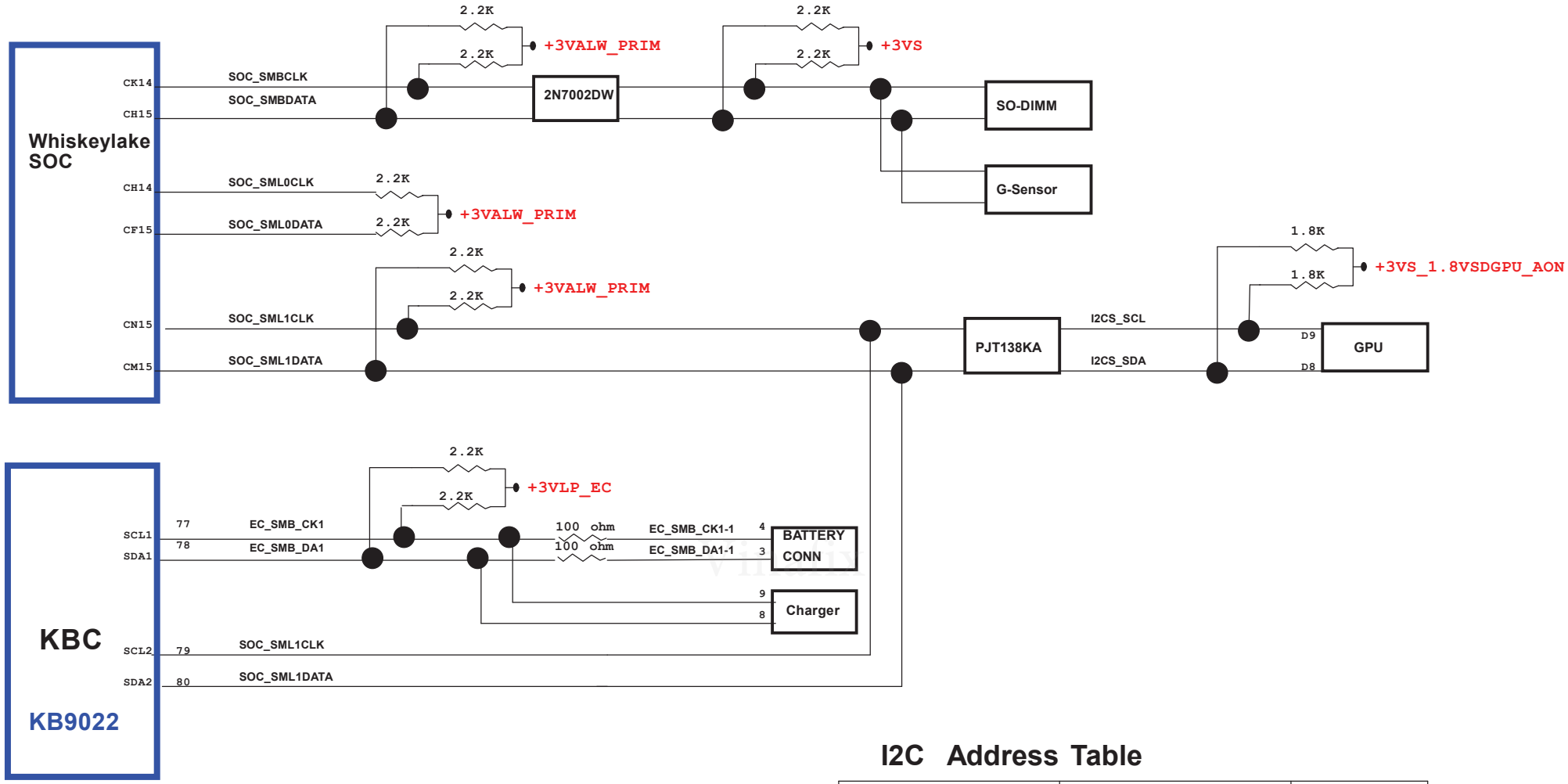
| Date: Friday, November 30, 2018 | Sheet 4 of 57 | | |




## I2C Address Table

| BUS | Device | Address (8 bit) |
|---|---|---|
| I2C_0 (+3VS) | Reserved | |
| I2C_1 (+3VALW_PRIM) | TM-P2969-001 (TP) | 0x2C |
| | SB8787-1200 (TP-ELAN) | 0x15 |
| SOC_SMBCLK (+3VS) | SO-DIMM1 | 0xA0 |
| | SO-DIMM2 | 0xA4 |
| | G-Sensor | 0x30 |
| SOC_SML1CLK (+3VALW_PRIM) | GPU | 0x9E |
| | EC | |
| EC_SMB_CK1 (+3VLP) | ISL88739 (Charger IC) | 0x12 |
| | BATTERY PACK | 0x16 |

| | | | |
|---|---|---|---|
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Title: SMBUS Routing Table

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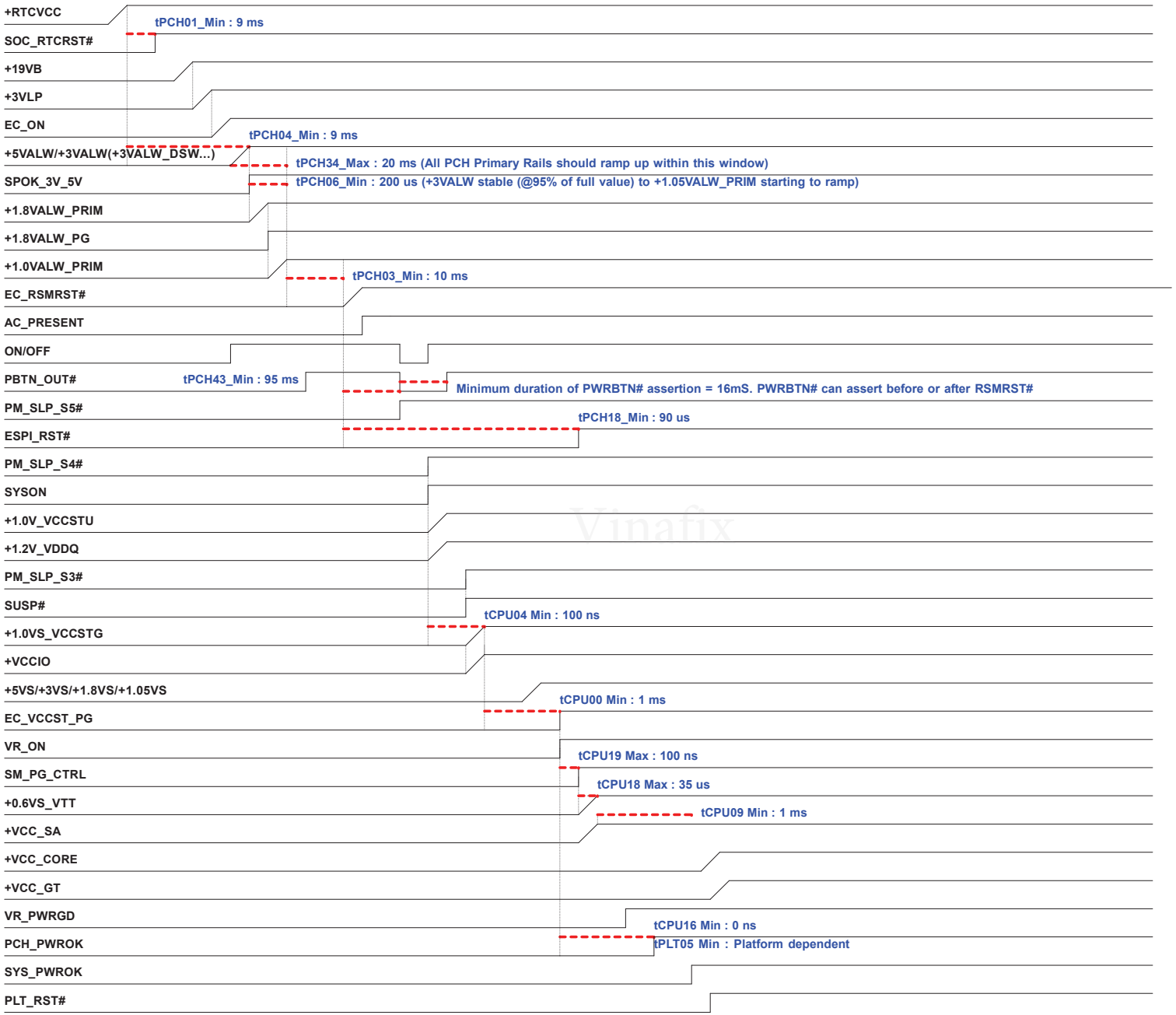
# PWR Sequence_KBL-U_DDR4_Value_NON CS






| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



**Compal Electronics, Inc.**

Title: **Power Sequence**

| Size | Document Number | Rev |
|---|---|---|
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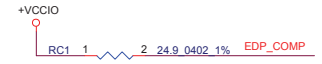
Date: Friday, November 30, 2018 Sheet 6 of 57

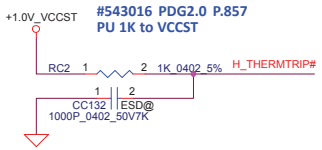
## Functional Strap Definitions

**#543016 PDG2.0 P.844**

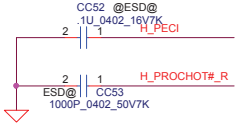
**DDPB_CTRLDATA**
**DDPC_CTRLDATA**
**Display Port B/C Detected**
**NC =Port is not detected.**
**PU =Port is detected.**

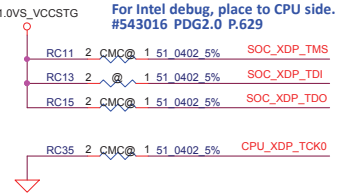



**#543016 PDG2.0 P.225**
**COMPENSATION PU for eDP**
**Trace width=5 mils,Spacing=25mil,Max length=600mils**

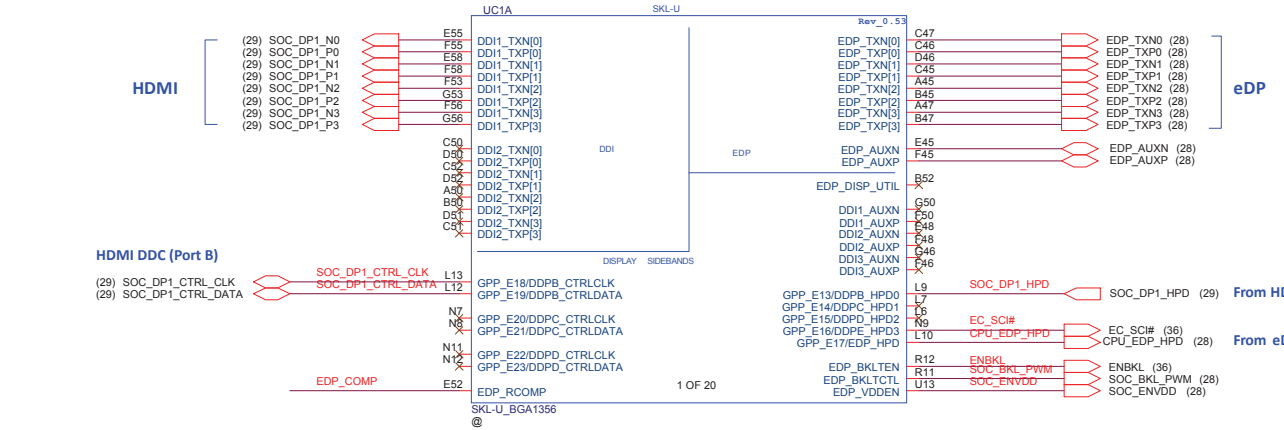


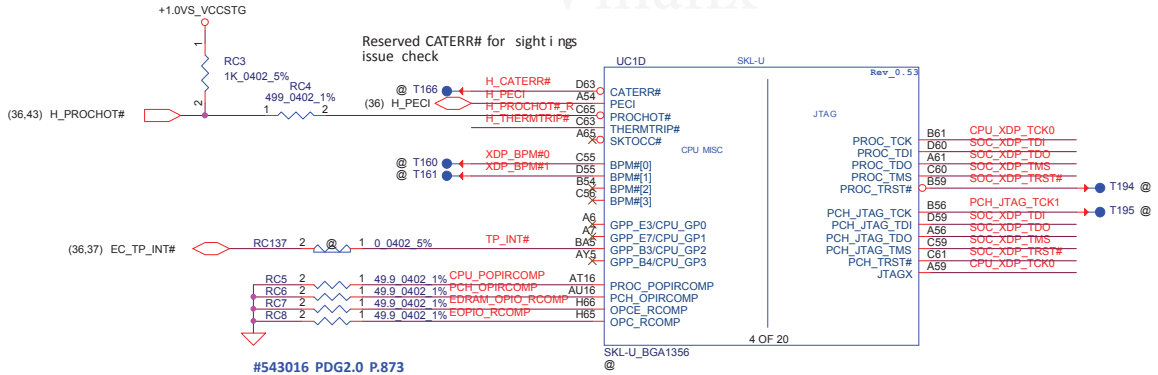

**#543016 PDG2.0 P.857**
**PU 1K to VCCST**




**For Intel debug, place to CPU side.**
**#543016 PDG2.0 P.629**




**#543016 PDG2.0 P.873**
**PROC_POPIRCOMP/PCH_OPIRCOMP**
**PD 50ohm**

**#544669 CRB1.1 P.52**
**EDRAM_OPIO_RCOMP/EOPIO_RCOMP**
**PD 50ohm**


**#545659 PCH EDS1.51 P.131**
**SCI capability is available on all GPIOs, while NMI and SMI capability is available on only select GPIOs.**
**Below are the PCH GPIOs that can be routed to generate SMI# or NMI:**
- **GPP_B14 GPP_B20 GPP_B23**
- **GPP_C [23 : 22 ]**
- **GPP_D [4 : 0 ]**
- **GPP_E [8: 0], GPP_E [16: 13 ]**

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|---|---|---|---|
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|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: KBL-R U(1/12)DDI,MSIC,XDP,EDP | | | |
| Size: Custom | Document Number: Raticate_KL M/B LA-H441P | | Rev: 0.1 |
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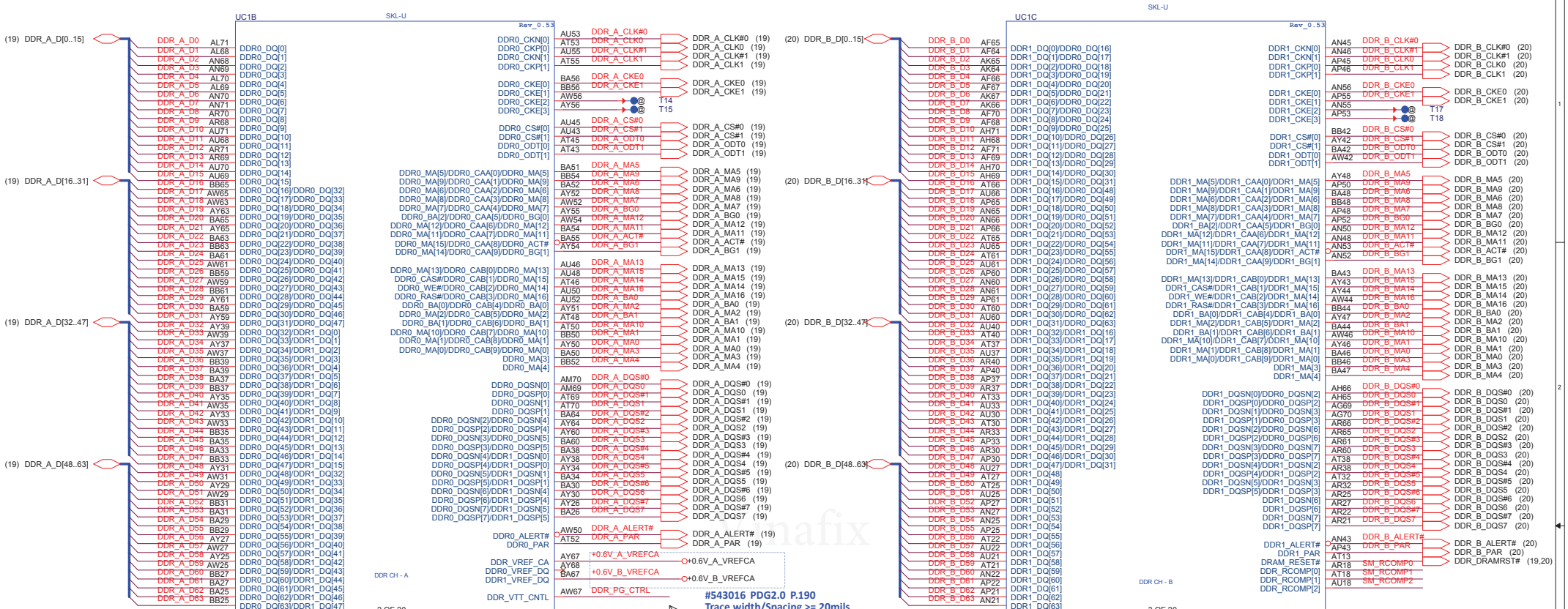
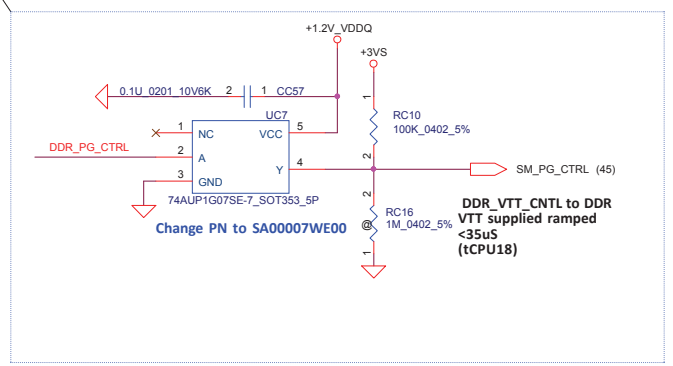
# Interleaved Memory

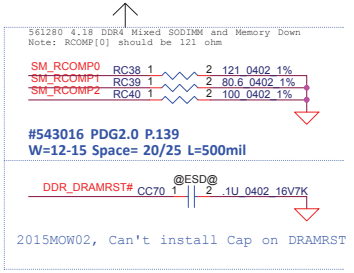



#543016 PDG2.0 P.190
Trace width/Spacing >= 20mils
Place compponment near SODIMM




Change PN to SA00007WE00

DDR_VTT_CNTL to DDR VTT supplied ramped <35uS (tCPU18)




#543016 PDG2.0 P.139
W=12-15 Space= 20/25 L=500mil

2015MOW02, Can't install Cap on DRAMRST

Intel DOC: 549352

3. RCOMP[0] value for SDP is 200+/-1% ohm, and for DDP is 121+/- 1% ohm

| | | | |
|---|---|---|---|
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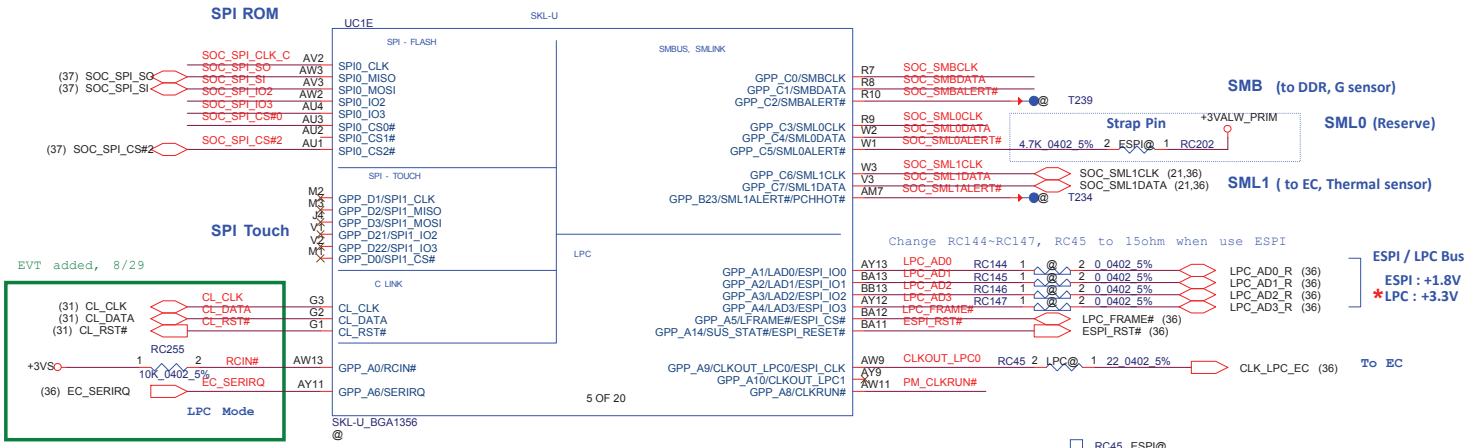
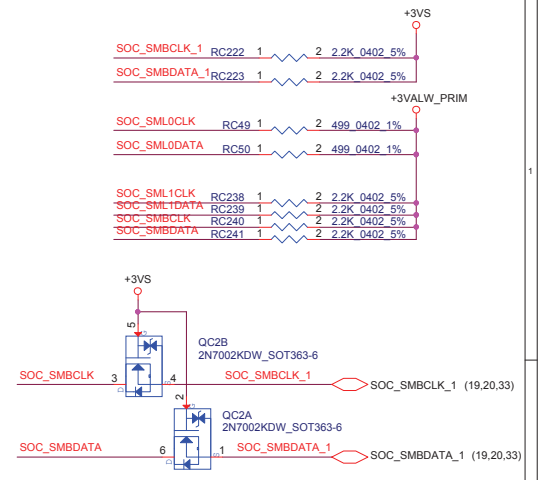
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | KBL-R U(2/12)DDR4 | | |
| Size | Document Number | | Rev |
| Custom | Raticate_KL M/B LA-H441P | | 0.1 |
| Date: | Friday, November 30, 2018 | Sheet | 8 of 57 |



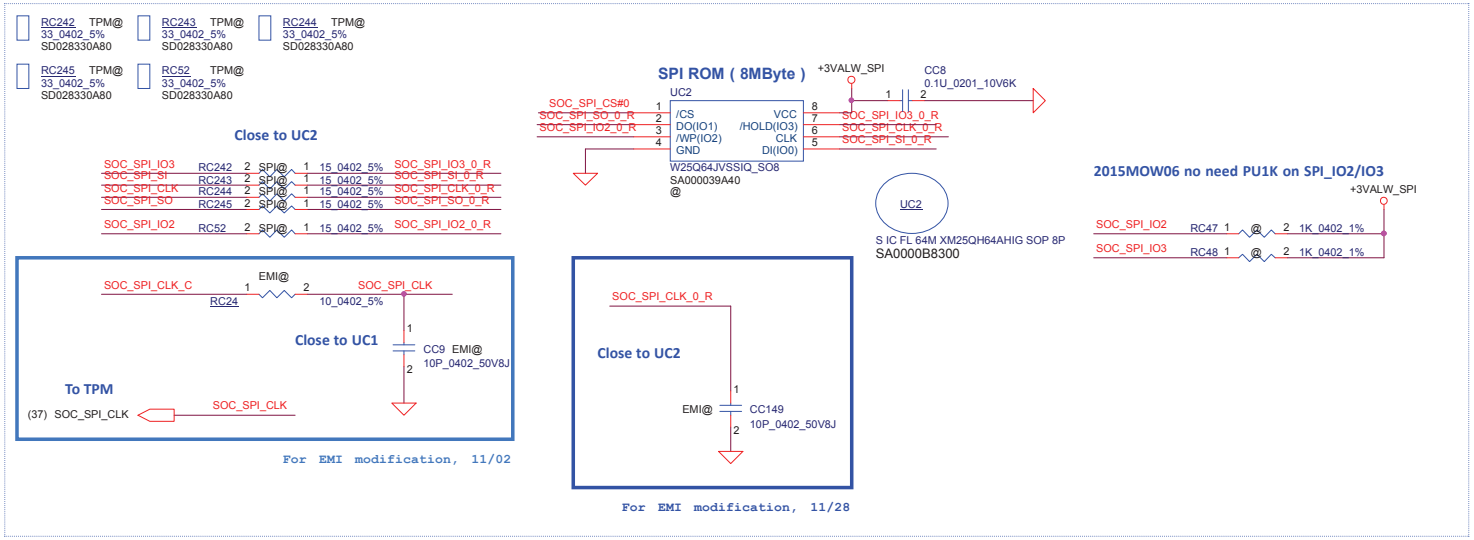


**SML0ALERT# / GPP_C5 (Internal Pull Down):**
**(Sampled: Rising edge of RSMRST# )**

**eSPI or LPC**
***0 = LPC is selected for EC --> For KB9022/9032 Use**
**1 = eSPI is selected for EC --> For KB9032 Only.**

**SMBALERT# / GPP_C2 (Internal Pull Down):**
**(Sampled: Rising edge of RSMRST# )**

**TLS Confidentiality**
***0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality) .**
**1 = Enable Intel ME Crypto (TLS) (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.**



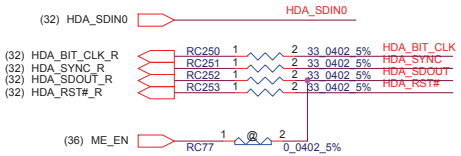



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | KBL-R U(3/12)SPI,ESPI,SMB,LPC | | |
| Size: Custom | Document Number: Raticate_KL M/B LA-H441P | | Rev: 0.1 |
| Date: Friday, November 30, 2018 | Sheet 9 of 57 | | |

## HDA for AUDIO



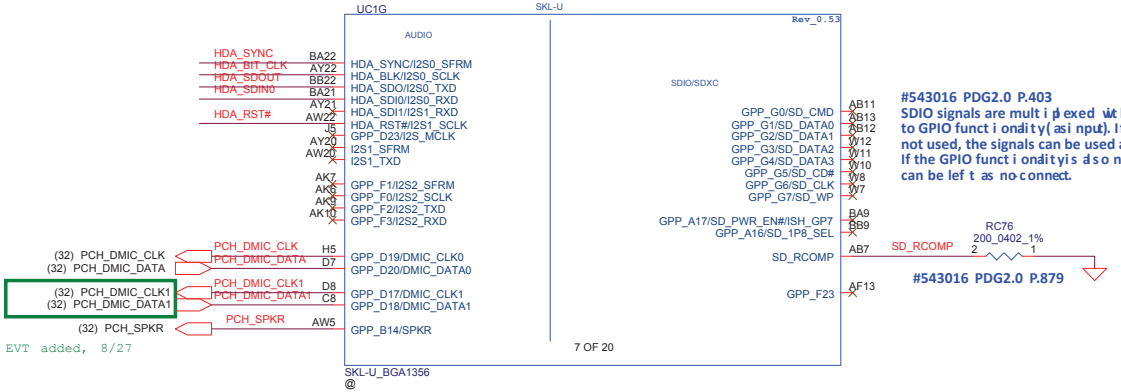

HDA_SDO / I2S_TXD0 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK )
Flash Descriptor Security Override
0 = Enable security measures defined in the flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external

pull-up in manufacturing/debug environments ONLY.

**SPKR / GPP_B14 (Internal Pull Down):**
**(Sampled:Rising edge of PCH_PWROK)**

**TOP Swap Override**
*** 0 = Disable TOP Swap mode.**
**1 = Enable TOP Swap Mode.**

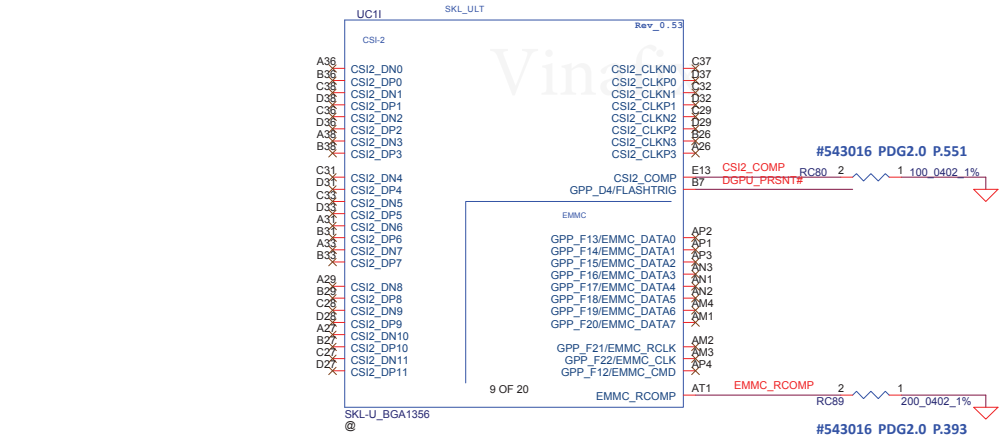
Intel HD Audio link capabilities
> Two SDI signals to support two external codecs.
> Drivers variable requency (5MHz to 24MHz) BCLK to support:
-- SDO double pumped up to 48 Mb/s
-- SDI's single pumped up to 24 Mb/s
> Provides cadence for 44.1 kHz based sample rate output.
> Support 1.5V, 1.8V, and 3.3V modes.




EVT added, 8/27

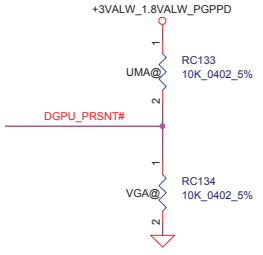
#543016 PDG2.0 P.403
SDIO signals are multiplexed with GPIOs and default to GPIO functionality(as input). If SDIO interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, these signals can be left as no-connect.

#543016 PDG2.0 P.879




#543016 PDG2.0 P.551

#543016 PDG2.0 P.393




| | DGPU_PRSNT# |
|---|---|
| DIS,Optimus | 0 |
| UMA | 1 |



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |

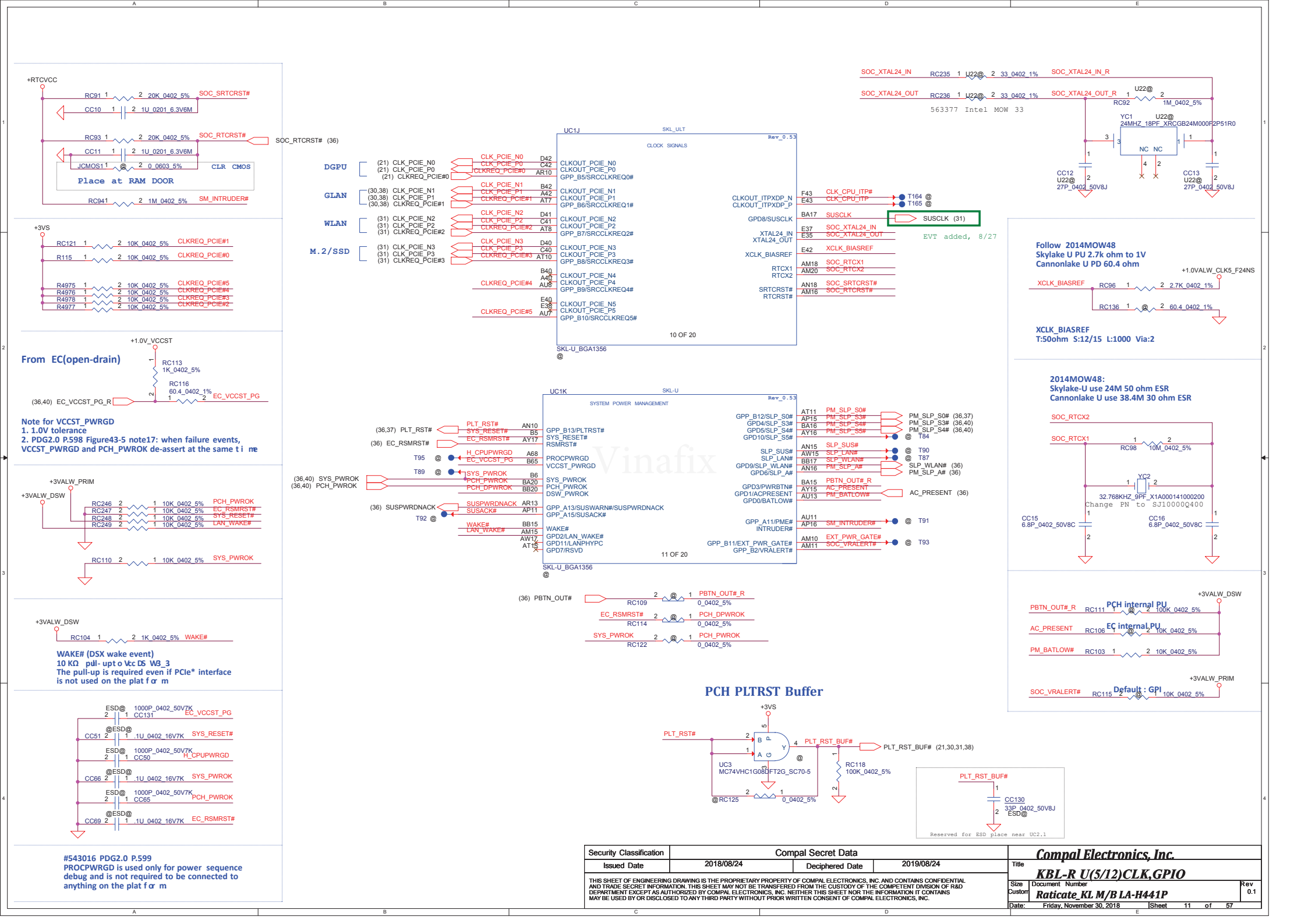


Compal Electronics, Inc.

Title: KBL-R U(4/12)HDA,EMMC,SDIO,CSI2

| Size | Document Number | Rev |
|---|---|---|
| Custom | Raticate_KL M/B LA-H441P | 0.1 |

Date: Friday, November 30, 2018 Sheet 10 of 57

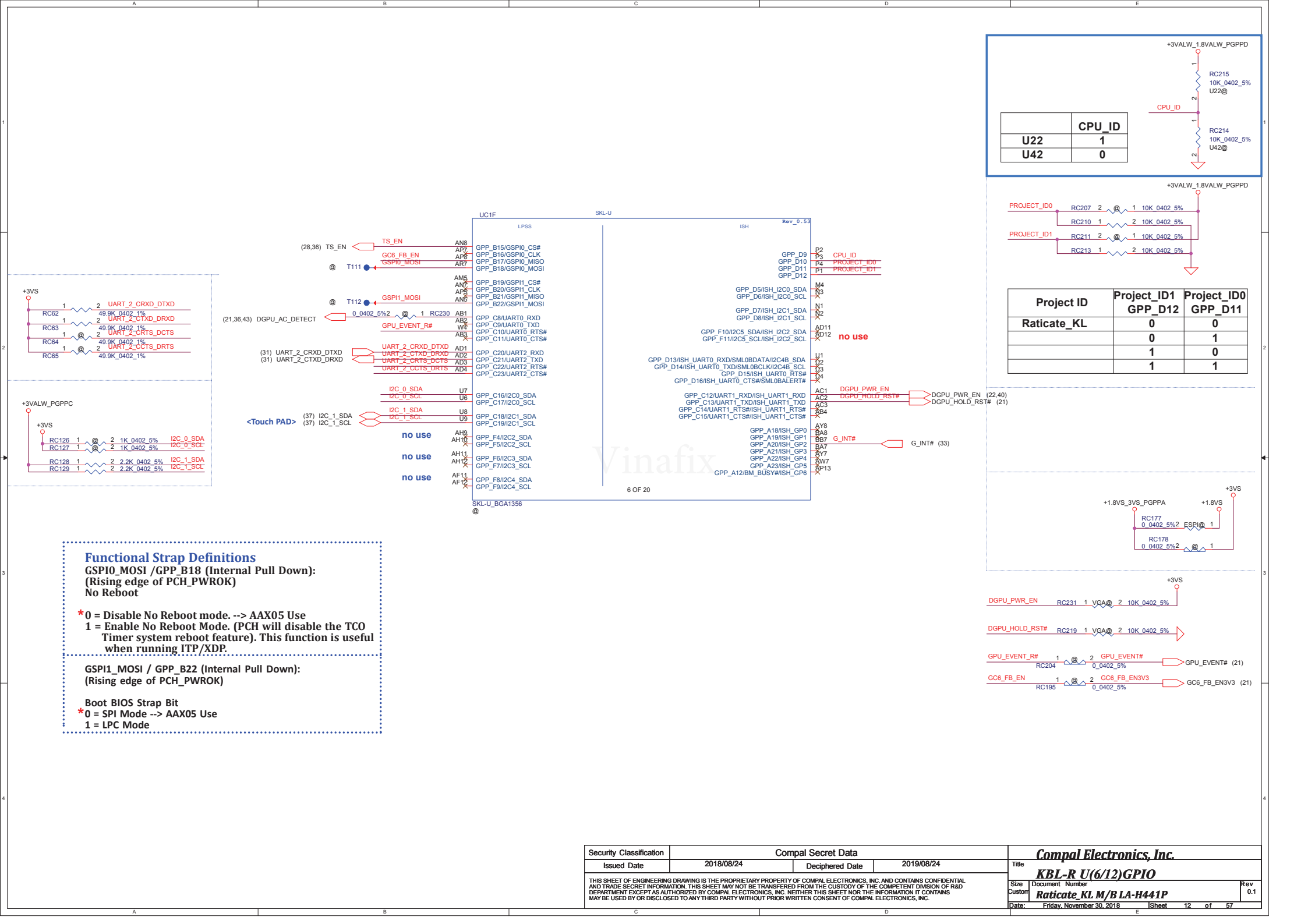





| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: KBL-R U(5/12)CLK,GPIO | | | |
| Size: Custom | Document Number: Raticate_KL M/B LA-H441P | | Rev: 0.1 |
| Date: Friday, November 30, 2018 | | Sheet 11 of 57 | |




## Functional Strap Definitions

**GSPI0_MOSI /GPP_B18 (Internal Pull Down):**
**(Rising edge of PCH_PWROK)**
**No Reboot**

***0 = Disable No Reboot mode. --> AAX05 Use**
**1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.**

**GSPI1_MOSI / GPP_B22 (Internal Pull Down):**
**(Rising edge of PCH_PWROK)**

**Boot BIOS Strap Bit**
***0 = SPI Mode --> AAX05 Use**
**1 = LPC Mode**



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | KBL-R U(6/12)GPIO |
| Size: Custom | Document Number: Raticate_KL M/B LA-H441P |
| Rev | 0.1 |
| Date: Friday, November 30, 2018 | Sheet 12 of 57 |

for RTS5227

(38) PCIE_CTX_DRX_P5 → PCIE_CTX_DRX_P5
(38) PCIE_CTX_DRX_N5 → PCIE_CTX_DRX_N5

EVT added, 8/27

UC1H — SKL-U — Rev_0.53

PCIE/USB3/SATA

DGPU

(21) PCIE_CRX_GTX_N1 → PCIE_CRX_GTX_N1 → H13 → PCIE1_RXN/USB3_5_RXN
(21) PCIE_CRX_GTX_P1 → PCIE_CRX_GTX_P1 → G13 → PCIE1_RXP/USB3_5_RXP
(21) PCIE_CTX_C_GRX_N1 → CC17 VGA@1 0.22U 0402 16V7K → PCIE_CTX_GRX_N1 → B17 → PCIE1_TXN/USB3_5_TXN
(21) PCIE_CTX_C_GRX_P1 → CC21 VGA@1 0.22U 0402 16V7K → PCIE_CTX_GRX_P1 → A17 → PCIE1_TXP/USB3_5_TXP

(21) PCIE_CRX_GTX_N2 → PCIE_CRX_GTX_N2 → G11 → PCIE2_RXN/USB3_6_RXN
(21) PCIE_CRX_GTX_P2 → PCIE_CRX_GTX_P2 → F11 → PCIE2_RXP/USB3_6_RXP
(21) PCIE_CTX_C_GRX_N2 → CC18 VGA@1 0.22U 0402 16V7K → PCIE_CTX_GRX_N2 → D16 → PCIE2_TXN/USB3_6_TXN
(21) PCIE_CTX_C_GRX_P2 → CC19 VGA@1 0.22U 0402 16V7K → PCIE_CTX_GRX_P2 → C16 → PCIE2_TXP/USB3_6_TXP

(21) PCIE_CRX_GTX_N3 → PCIE_CRX_GTX_N3 → H16 → PCIE3_RXN
(21) PCIE_CRX_GTX_P3 → PCIE_CRX_GTX_P3 → G16 → PCIE3_RXP
(21) PCIE_CTX_C_GRX_N3 → CC20 VGA@1 0.22U 0402 16V7K → PCIE_CTX_GRX_N3 → D17 → PCIE3_TXN
(21) PCIE_CTX_C_GRX_P3 → CC22 VGA@1 0.22U 0402 16V7K → PCIE_CTX_GRX_P3 → C17 → PCIE3_TXP

(21) PCIE_CRX_GTX_N4 → PCIE_CRX_GTX_N4 → G15 → PCIE4_RXN
(21) PCIE_CRX_GTX_P4 → PCIE_CRX_GTX_P4 → F15 → PCIE4_RXP
(21) PCIE_CTX_C_GRX_N4 → CC23 VGA@1 0.22U 0402 16V7K → PCIE_CTX_GRX_N4 → B19 → PCIE4_TXN
(21) PCIE_CTX_C_GRX_P4 → CC24 VGA@1 0.22U 0402 16V7K → PCIE_CTX_GRX_P4 → A19 → PCIE4_TXP

GLAN

(30,38) PCIE_CRX_DTX_N5 → PCIE_CRX_DTX_N5 → F16 → PCIE5_RXN
(30,38) PCIE_CRX_DTX_P5 → CC25 .1U 0402 16V7K → PCIE_CRX_DTX_P5 → E16 → PCIE5_RXP
(30) PCIE_CTX_C_DRX_N5 → CC26 .1U 0402 16V7K → PCIE_CTX_DRX_N5 → C19 → PCIE5_TXN
(30) PCIE_CTX_C_DRX_P5 → PCIE_CTX_DRX_P5 → D19 → PCIE5_TXP

NGFF WLAN+BT(Key E)

(31) PCIE_CRX_DTX_N6 → PCIE_CRX_DTX_N6 → G18 → PCIE6_RXN
(31) PCIE_CRX_DTX_P6 → PCIE_CRX_DTX_P6 → F18 → PCIE6_RXP
(31) PCIE_CTX_C_DRX_N6 → CC60 .1U 0402 16V7K → PCIE_CTX_DRX_N6 → D20 → PCIE6_TXN
(31) PCIE_CTX_C_DRX_P6 → CC62 .1U 0402 16V7K → PCIE_CTX_DRX_P6 → C20 → PCIE6_TXP

HDD

(33) SATA_CRX_DTX_N0 → F20 → PCIE7_RXN/SATA0_RXN
(33) SATA_CRX_DTX_P0 → E20 → PCIE7_RXP/SATA0_RXP
(33) SATA_CTX_DRX_N0 → B21 → PCIE7_TXN/SATA0_TXN
(33) SATA_CTX_DRX_P0 → A21 → PCIE7_TXP/SATA0_TXP

G21 → PCIE8_RXN/SATA1A_RXN
F21 → PCIE8_RXP/SATA1A_RXP
D21 → PCIE8_TXN/SATA1A_TXN
C21 → PCIE8_TXP/SATA1A_TXP

(31) PCIE_CRX_DTX_N9 → E22 → PCIE9_RXN
(31) PCIE_CRX_DTX_P9 → E23 → PCIE9_RXP
(31) PCIE_CTX_DRX_N9 → B23 → PCIE9_TXN
(31) PCIE_CTX_DRX_P9 → A23 → PCIE9_TXP

(31) PCIE_CRX_DTX_N10 → F25 → PCIE10_RXN
(31) PCIE_CRX_DTX_P10 → E25 → PCIE10_RXP
(31) PCIE_CTX_DRX_N10 → D23 → PCIE10_TXN
(31) PCIE_CTX_DRX_P10 → C23 → PCIE10_TXP

NGFF SSD(Key M)
(Need Lane Reversal)

#543016 PDG2.0 P.285
PCIE_RCOMPN/PCIE_RCOMPP
BO=4 W=12 S=12 R=100ohm

RC1201 100_0402_1% → PCIE_RCOMPN → F5 → PCIE_RCOMPN
PCIE_RCOMPP → E5 → PCIE_RCOMPP

+3VALW_PRIM
RC135 @ T196 @ T197 10K_0402_5%
XDP_PRDY# → D56 → PROC_PRDY#
XDP_PREQ# → D61 → PROC_PREQ#
TPM_PIRQ# → BB11 → GPP_A7/PIRQA#

EVT added, 9/4
(37) TPM_PIRQ#

(31) PCIE_CRX_DTX_N11 → E28 → PCIE11_RXN/SATA1B_RXN
(31) PCIE_CRX_DTX_P11 → E27 → PCIE11_RXP/SATA1B_RXP
(31) PCIE_CTX_DRX_N11 → D24 → PCIE11_TXN/SATA1B_TXN
(31) PCIE_CTX_DRX_P11 → C24 → PCIE11_TXP/SATA1B_TXP
(31) PCIE_CRX_DTX_N12 → E30 → PCIE12_RXN/SATA2_RXN
(31) PCIE_CRX_DTX_P12 → F30 → PCIE12_RXP/SATA2_RXP
(31) PCIE_CTX_DRX_N12 → A25 → PCIE12_TXN/SATA2_TXN
(31) PCIE_CTX_DRX_P12 → B25 → PCIE12_TXP/SATA2_TXP

SKL-U_BGA1356
@
8 OF 20

SSIC / USB3

USB3_1_RXN → H8 → USB3_CRX_DTX_N1 (35)
USB3_1_RXP → G8 → USB3_CRX_DTX_P1 (35)
USB3_1_TXN → C13 → USB3_CTX_DRX_N1 (35)
USB3_1_TXP → D13 → USB3_CTX_DRX_P1 (35)

USB3 MB

J6
USB3_2_RXN/SSIC_1_RXN → H6 → USB3_CRX_DTX_N2 (34)
USB3_2_RXP/SSIC_1_RXP → B13 → USB3_CRX_DTX_P2 (34)
USB3_2_TXN/SSIC_1_TXN → A13 → USB3_CTX_DRX_N2 (34)
USB3_2_TXP/SSIC_1_TXP → USB3_CTX_DRX_P2 (34)

J10
USB3_3_RXN/SSIC_2_RXN → H10 → USB3_CRX_DTX_N3 (34)
USB3_3_RXP/SSIC_2_RXP → B15 → USB3_CRX_DTX_P3 (34)
USB3_3_TXN/SSIC_2_TXN → A15 → USB3_CTX_DRX_N3 (34)
USB3_3_TXP/SSIC_2_TXP → USB3_CTX_DRX_P3 (34)

USB TypeC

USB3_4_RXN → E10
USB3_4_RXP → F10
USB3_4_TXN → C15
USB3_4_TXP → D15

USB2

USB2N_1 → AB9 → USB20_N1 → USB20_N1 (35)
USB2P_1 → AB10 → USB20_P1 → USB20_P1 (35)

USB3 MB

USB2N_2 → AD6 → USB20_N2 → USB20_N2 (34)
USB2P_2 → AD7 → USB20_P2 → USB20_P2 (34)

USB TypeC

USB2N_3 → AH3 → USB20_N3 → USB20_N3 (35)
USB2P_3 → AJ3 → USB20_P3 → USB20_P3 (35)

TO D/B USB2

USB2N_4 → AD9 → USB20_N4 → USB20_N4 (35)
USB2P_4 → AD10 → USB20_P4 → USB20_P4 (35)

USB2N_5 → AJ1 → USB20_N5 → USB20_N5 (37)
USB2P_5 → AJ2 → USB20_P5 → USB20_P5 (37)

FP

EVT added, 8/27

USB2N_6 → AF6
USB2P_6 → AF7

USB2N_7 → AH1 → USB20_N7 → USB20_N7 (28)
USB2P_7 → AH2 → USB20_P7 → USB20_P7 (28)

Camera

USB2N_8 → AF8
USB2P_8 → AF9

USB2N_9 → AG1 → USB20_N9 → USB20_N9 (28)
USB2P_9 → AG2 → USB20_P9 → USB20_P9 (28)

TS
BT

EVT added, 8/27

USB2N_10 → AH7 → USB20_N10 → USB20_N10 (31)
USB2P_10 → AH8 → USB20_P10 → USB20_P10 (31)

USB2_COMP → AB6 → USB2_COMP → RC119 1 2 113_0402_1%
USB2_ID → AG3 → USB2_ID → RC130 1 2 0_0402_5%
USB2_VBUSSENSE → AG4 → USB2_VBUSSENSE → RC131 1 2 0_0402_5%

2015MOW10, USB2_ID Connected to GND Directly

A9 → USB_OC0# → USB_OC0# (35)
C9
D9
E9

Unused OC pin need set to GPI.

GPP_E9/USB2_OC0#
GPP_E10/USB2_OC1#
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#

J1
J2
J3
GPP_E4/DEVSLP0
GPP_E5/DEVSLP1
GPP_E6/DEVSLP2
SSD_DEVSLP2 → SSD_DEVSLP2 (31)

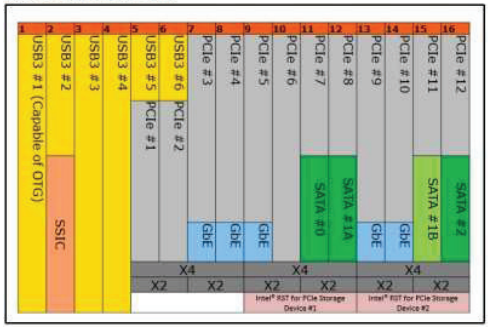
H2
G3
G4
GPP_E0/SATAXPCIE0/SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E2/SATAXPCIE2/SATAGP2
SATAXPCIE2 → SATAXPCIE2 (31)

H1
GPP_E8/SATALED#
RH16 1 2 +3VS 10K_0402_5%
M.2 SSD PCIE/SATA select pin

SSD_DET# (SATA_GP0)
SATA Device 0
PCIE Device 1

+3VALW_PRIM
USB_OC0# RC132 1 2 10K_0402_5%
ESD@ CC135 0.1U_0201_10V6K
For MB field lesson learnt

HSIO Multiplexing on PCH-U




| PCH-LP Details | | PCIe* Controller #1 | | | | PCIe* Controller #2 | | | | PCIe* Controller #3 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Flex I/O Lane # | | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| PCIe* Lane # | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| Base-U | 1x4 | RP1 | | | | | | | | RP9 | | | |
| | 2x2 | RP1 | | RP3 | | RP5 | | | | RP9 | | RP11 | |
| | 1x2+2x1 | RP1 | | RP3 | RP4 | RP5 | | | | RP9 | | RP11 | RP12 |
| | 2x1+1x2 | RP4 | RP3 | RP1 | | RP8 | RP7 | | | RP12 | RP11 | RP9 | |
| | 4x1 | RP1 | RP2 | RP3 | RP4 | RP5 | RP6 | | | RP9 | RP10 | RP11 | RP12 |
| Premium-U | 1x4 | RP1 | | | | RP5 | | | | RP9 | | | |
| | 2x2 | RP1 | | RP3 | | RP5 | | RP7 | | RP9 | | RP11 | |
| | 1x2+2x1 | RP1 | | RP3 | RP4 | RP5 | | RP7 | RP8 | RP9 | | RP11 | RP12 |
| | 2x1+1x2 | RP4 | RP3 | RP1 | | RP8 | RP7 | RP5 | | RP12 | RP11 | RP9 | |
| | 4x1 | RP1 | RP2 | RP3 | RP4 | RP5 | RP6 | RP7 | RP8 | RP9 | RP10 | RP11 | RP12 |

| GPIO | DEVICE CONTROL |
|---|---|
| USB_OC0# | USB2 Port 1 |
| USB_OC1# | NA |
| USB_OC2# | NA |
| USB_OC3# | NA |
| DEVSLP0 | NA |
| DEVSLP1 | NA |
| DEVSLP2 | NA |
| SATA_GP0 | NA |
| SATA_GP1 | NA |
| SATA_GP2 | NA |

**DEVSLP[2:0] Implementation**
DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.
The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL U.
• When high, DEVSLP requests the SATA device to enter into the DEVSLP power state
• When low, DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

**SATA General Purpose (SATAGP[2:0]) Signals**
•The processor provides three SATA general purpose input signals, SATAGP[2:0] for SKL U. These signals can be configured as interlock switch inputs corresponding to a given SATA port.
• When used as an interlock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.
If mechanical presence switches will not be used on the platform, SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.



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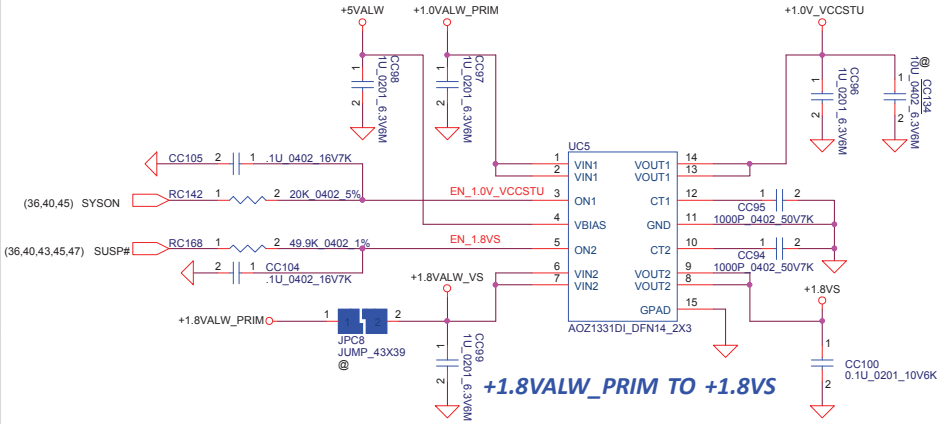
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |

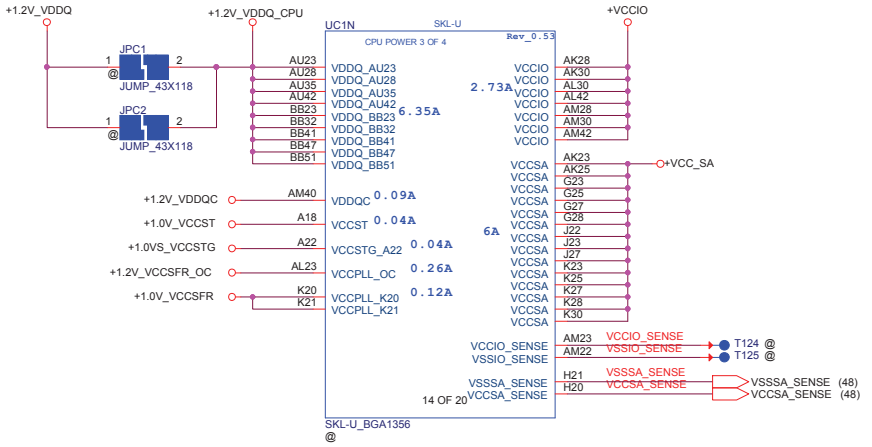


Compal Electronics, Inc.
Title: KBL-R U(7/12)PCIE,USB,SATA
Size: Custom | Document Number: Raticate_KL M/B LA-H441P | Rev: 0.1
Date: Friday, November 30, 2018 | Sheet 13 of 57

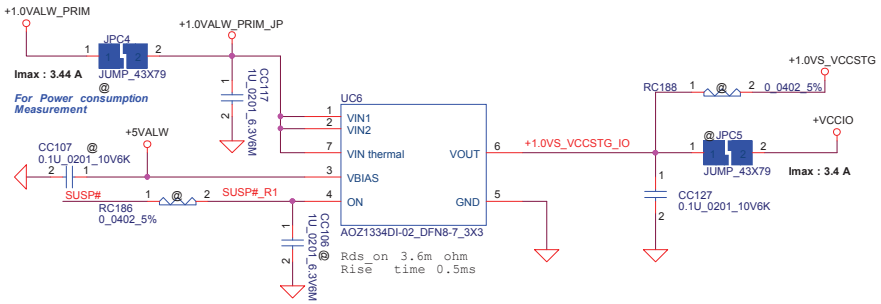
## +1.0VALW_PRIM TO +1.0V_VCCSTU / +1.0VCCST

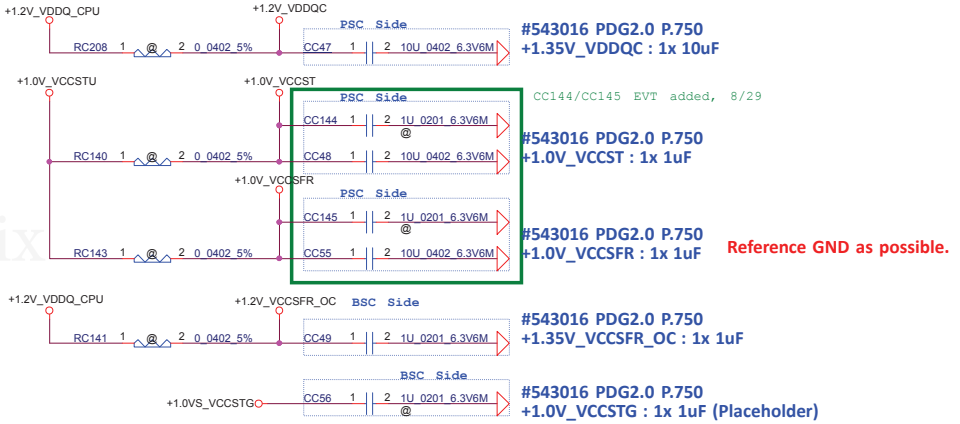


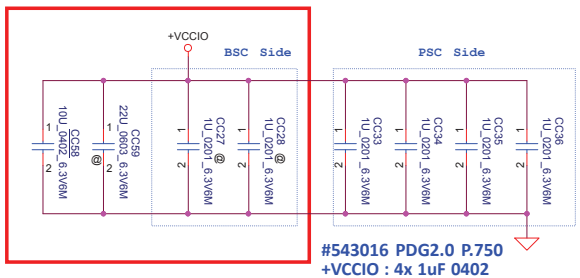

## +1.8VALW_PRIM TO +1.8VS

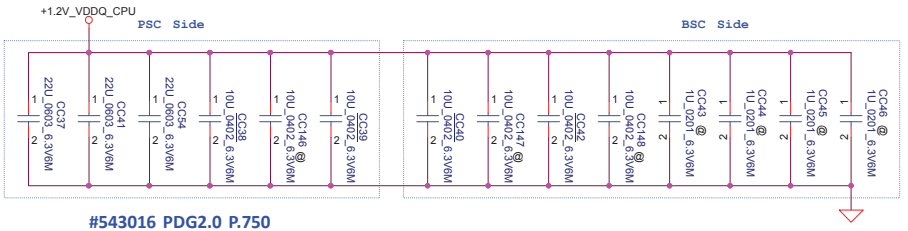



## +1.0VALW_PRIM TO +1.0VS_VCCSTG



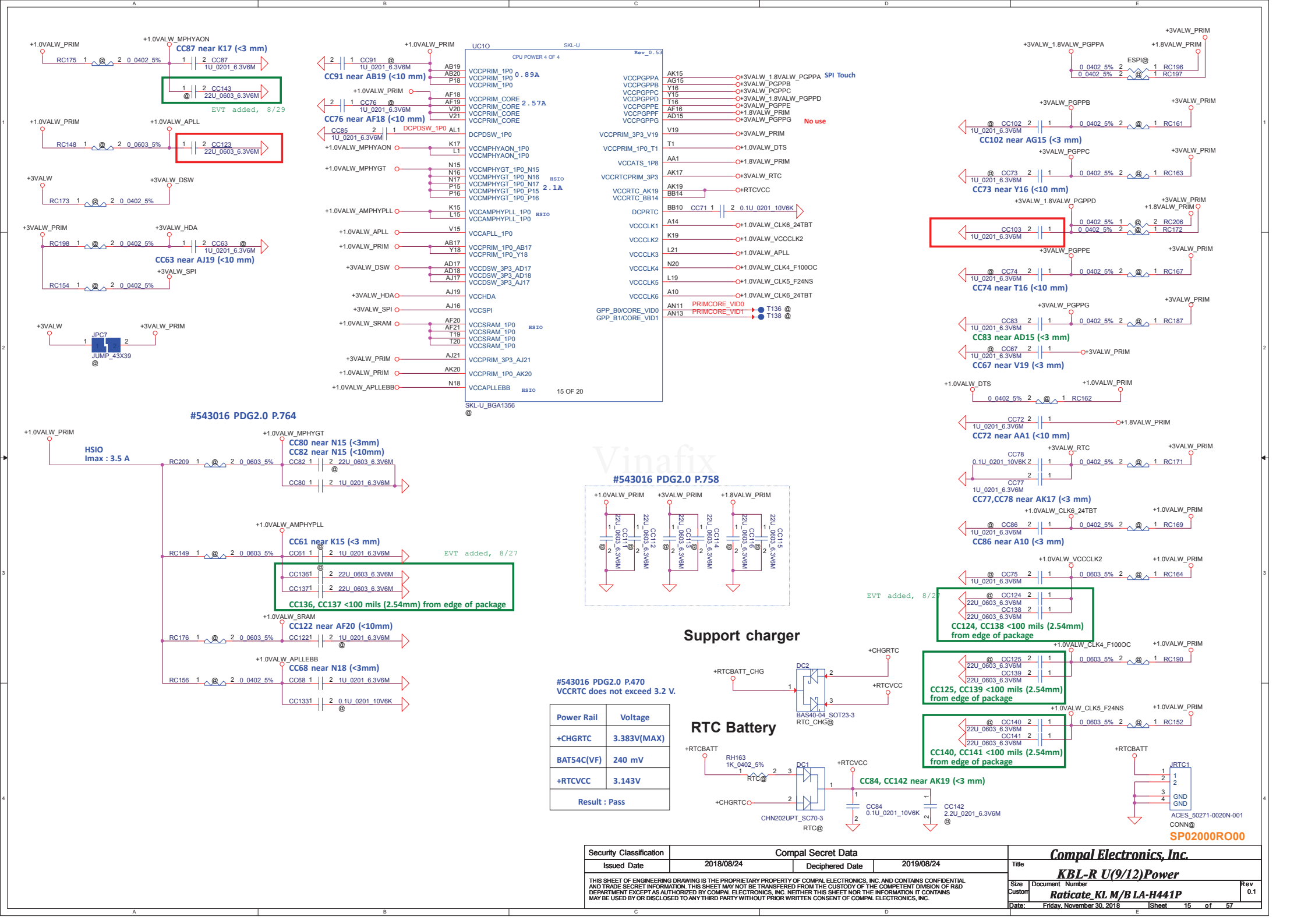






| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | KBL-R U(8/12)Power |
| Size / Custom | Document Number: Raticate_KL M/B LA-H441P |
| Rev | 0.1 |
| Date: | Friday, November 30, 2018 |
| Sheet | 14 of 57 |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |

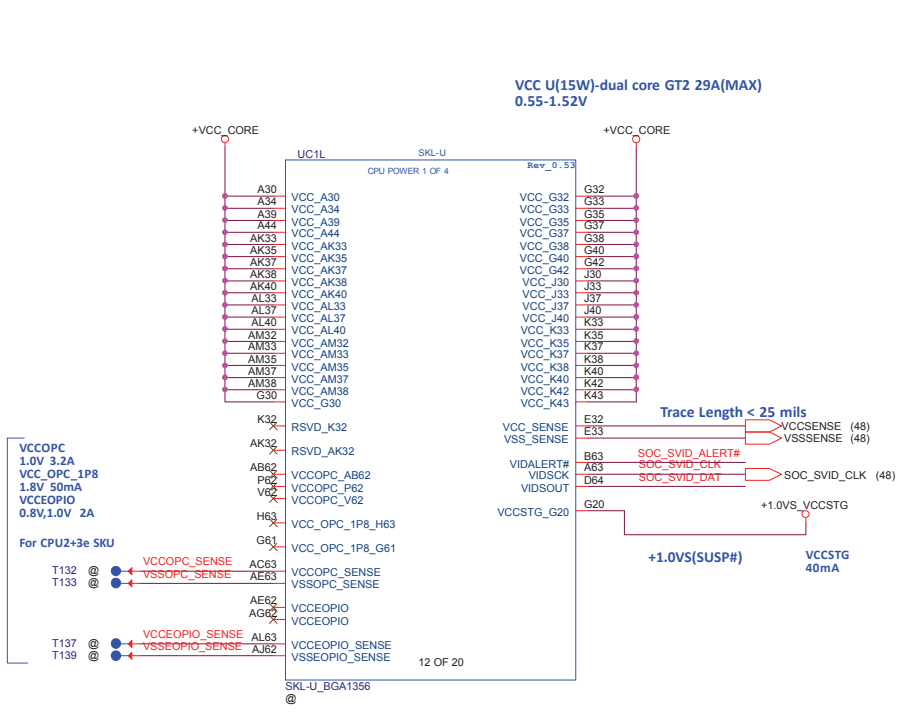


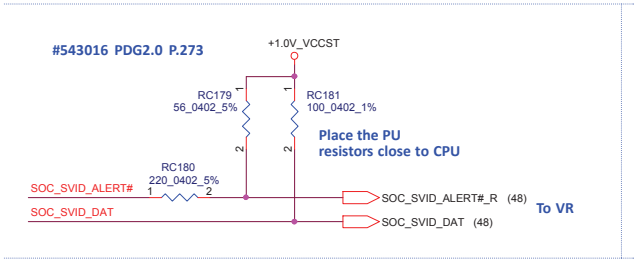
Compal Electronics, Inc.

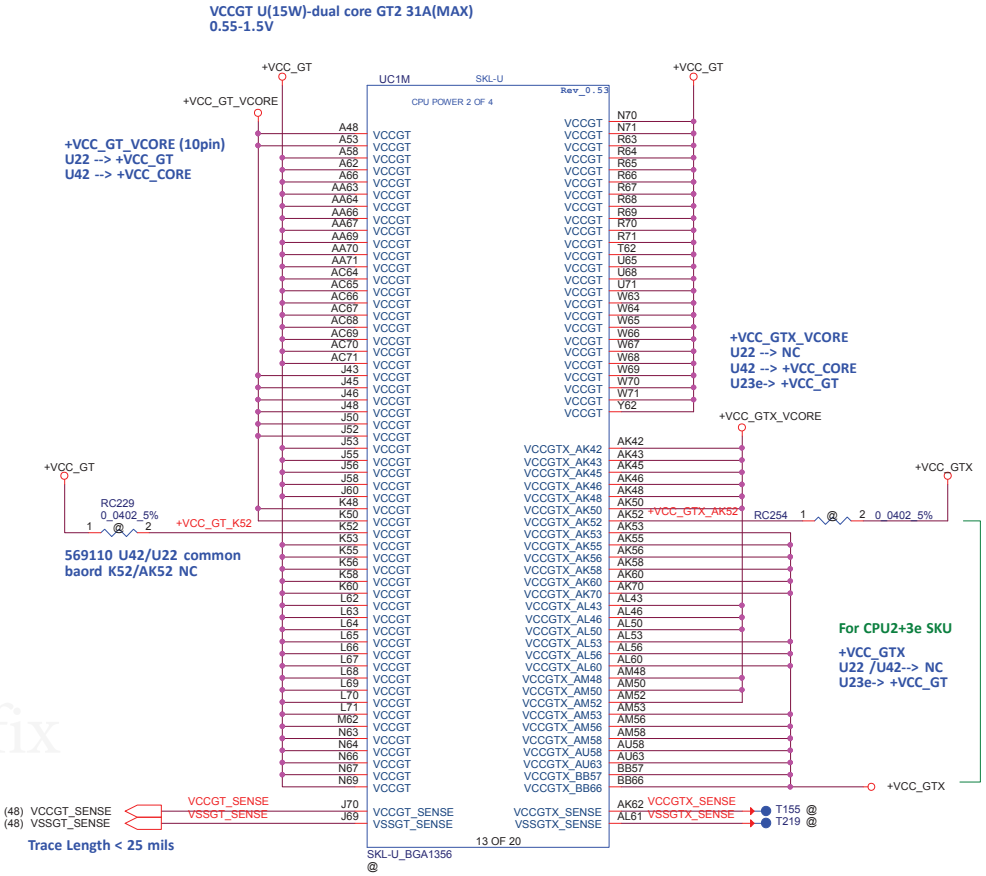
Title: KBL-R U(9/12)Power

Size: Custom | Document Number: Raticate_KL M/B LA-H441P | Rev: 0.1

Date: Friday, November 30, 2018 | Sheet 15 of 57




## Processor Power Rails

| Power Rail | Description | Control |
|---|---|---|
| $V_{CC}$ | Processor IA Cores Power Rail | SVID |
| $Vcc_{GT}$ | Processor Graphics Power Rails | SVID |
| $Vcc_{GTX}$ | Processor Graphics Extended Power Rail<br>Available only for GT3/GT4 processor SKUs | SVID |
| $Vcc_{SA}$ | System Agent Power Rail | SVID/Fixed (SKU dependent) |
| $Vcc_{IO}$ | IO Power Rail | Fixed |
| $Vcc_{ST}$ | Sustain Power Rail | Fixed |
| $Vcc_{PLL}$ | Processor PLLs power rail | Fixed |
| $V_{DDQ}$ | Integrated Memory Controller Power Rail | Fixed (Memory technology dependent) |
| $Vcc_{OPC}$ | Processor OPC power rail (available only in SKU's with OPC) | Fixed |
| $Vcc_{OPC\_1P8}$ | Processor OPC power rail (available only in SKU's with OPC) | Fixed |
| $Vcc_{EOPIO}$ | Processor EOPIO power rail (available only in SKU's with OPC) | Fixed |



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



Compal Electronics, Inc.

Title: KBL-R U(10/12)Power,SVID

Size: Custom | Document Number: Raticate_KL M/B LA-H441P | Rev: 0.1

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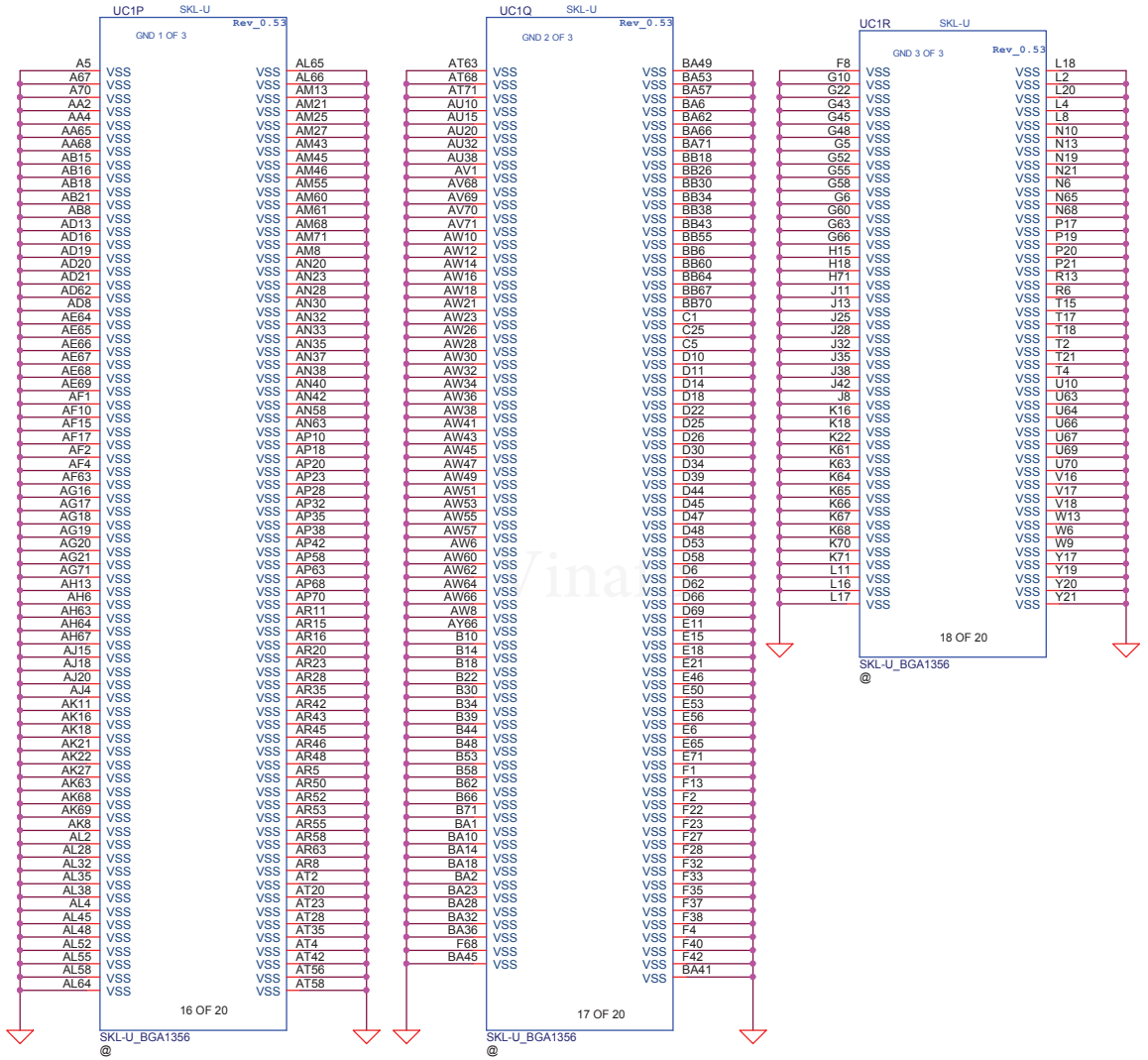



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |

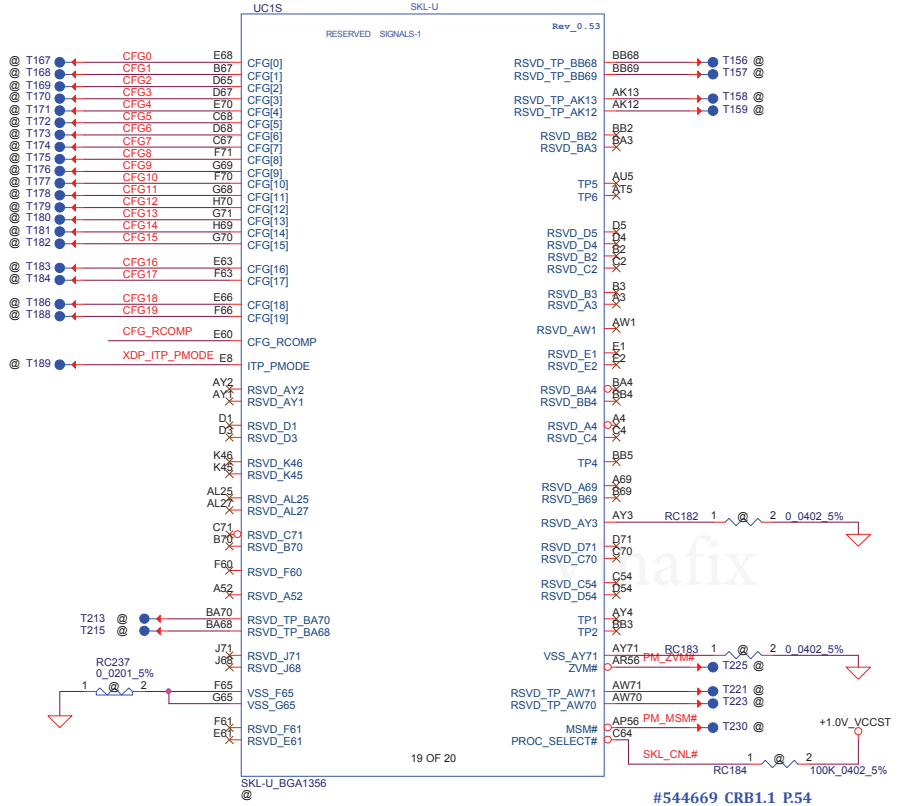


**Compal Electronics, Inc.**

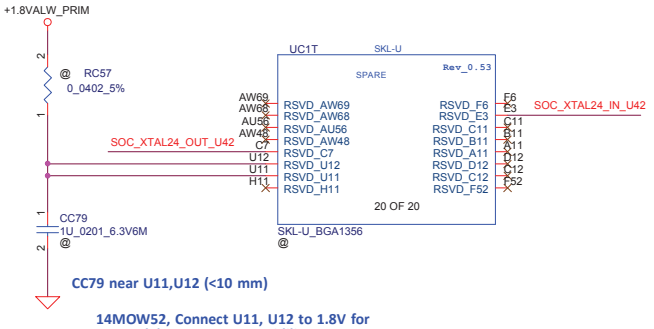
Title: **KBL-R U(11/12)GND**

| Size | Document Number | Rev |
|---|---|---|
| Custom | Raticate_KL M/B LA-H441P | 0.1 |

Date: Friday, November 30, 2018 Sheet 17 of 57




#544669 CRB1.1 P.54
#544924 SKL EDS1.2 P.125
PROC_SELECT#
This pin is for compatibility with future platforms. It should be unconnected for the processor.




CC79 near U11,U12 (<10 mm)

14MOW52, Connect U11, U12 to 1.8V for Cannonlake-U PCH compatibility

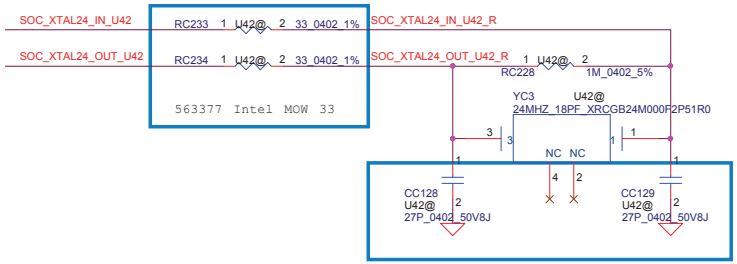
For 2+3e Solution

PM_ZVM#
Zero Voltage Mode: Control Signal to OPC VR, when low OPC VR output is 0V.

PM_MSM#
Minimum Speed Mode: Control signal to VccEOPIO VR (connected only in 2 VR solution for OPC).

| Display Port Presence Strap | |
|---|---|
| CFG4 | 1 : Disabled; No Physical Display Port attached to Embedded Display Port<br>0 : Enabled; An external Display Port device is connected to the Embedded Display Port |

568813_KBL_U42 Rev0.5




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



Compal Electronics, Inc.

Title: KBL-R U(12/12)RSVD

Size: Custom | Document Number: Raticate_KL M/B LA-H441P | Rev: 0.1

Date: Friday, November 30, 2018 | Sheet 18 of 57

# REVERSE TYPE

2-3A to 1 DIMMs/channel

(8) DDR_A_DQS#[0..7]
(8) DDR_A_D[0..63]
(8) DDR_A_DQS[0..7]

(8) DDR_A_MA[0..16]
(8) DDR_A_BA0 — DDR_A_BA0
(8) DDR_A_BA1 — DDR_A_BA1
(8) DDR_A_BG0 — DDR_A_BG0
(8) DDR_A_BG1 — DDR_A_BG1
(8) DDR_A_ACT# — DDR_A_ACT#
(8) DDR_A_ALERT# — DDR_A_ALERT#
(8) DDR_A_PAR — DDR_A_PAR

(8) DDR_A_CLK0 — DDR_A_CLK0
(8) DDR_A_CLK#0 — DDR_A_CLK#0
(8) DDR_A_CLK1 — DDR_A_CLK1
(8) DDR_A_CLK#1 — DDR_A_CLK#1

(8) DDR_A_CKE0 — DDR_A_CKE0
(8) DDR_A_CKE1 — DDR_A_CKE1
(8) DDR_A_CS#0 — DDR_A_CS#0
(8) DDR_A_CS#1 — DDR_A_CS#1

(9,20,33) SOC_SMBDATA_1 — SOC_SMBDATA_1
(9,20,33) SOC_SMBCLK_1 — SOC_SMBCLK_1

(8) DDR_A_ODT0 — DDR_A_ODT0
(8) DDR_A_ODT1 — DDR_A_ODT1

DDR_A_SA2
DDR_A_SA1
DDR_A_SA0
RD66 0_0402_5% @
RD64 0_0402_5% @
RD67 0_0402_5% @

**Layout Note:**
**Place near JDIMM1**

+1.2V_VDDQ
CD74 1U_0201_6.3V6M
CD72 1U_0201_6.3V6M
CD76 1U_0201_6.3V6M
CD77 1U_0201_6.3V6M
CD78 1U_0201_6.3V6M
CD79 1U_0201_6.3V6M
CD80 1U_0201_6.3V6M
CD81 1U_0201_6.3V6M

+1.2V_VDDQ
CD82 10U_0402_6.3V6M
CD83 10U_0402_6.3V6M
CD84 10U_0402_6.3V6M
CD85 10U_0402_6.3V6M
CD86 10U_0402_6.3V6M
CD87 10U_0402_6.3V6M
CD88 10U_0402_6.3V6M
CD89 10U_0402_6.3V6M

JDIMM1A
REVERSE

| | | | | | |
|---|---|---|---|---|---|
| DDR_A_CLK0 | 137 | CK0(T) | DQ0 | 8 | DDR_A_D4 |
| DDR_A_CLK#0 | 139 | CK0#(C) | DQ1 | 7 | DDR_A_D5 |
| DDR_A_CLK1 | 138 | CK1(T) | DQ2 | 20 | DDR_A_D2 |
| DDR_A_CLK#1 | 140 | CK1#(C) | DQ3 | 21 | DDR_A_D7 |
| | | | DQ4 | 4 | DDR_A_D0 |
| DDR_A_CKE0 | 109 | CKE0 | DQ5 | 3 | DDR_A_D1 |
| DDR_A_CKE1 | 110 | CKE1 | DQ6 | 16 | DDR_A_D6 |
| | | | DQ7 | 17 | DDR_A_D3 |
| DDR_A_CS#0 | 149 | S0# | DQS0(T) | 13 | DDR_A_DQS0 |
| DDR_A_CS#1 | 157 | S1# | DQS0#(C) | 11 | DDR_A_DQS#0 |
| | 162 | S2#/C0 | | | |
| | 165 | S3#/C1 | | | |
| | | | DQ8 | 28 | DDR_A_D9 |
| DDR_A_ODT0 | 155 | ODT0 | DQ9 | 29 | DDR_A_D12 |
| DDR_A_ODT1 | 161 | ODT1 | DQ10 | 41 | DDR_A_D10 |
| | | | DQ11 | 42 | DDR_A_D15 |
| DDR_A_BG0 | 115 | BG0 | DQ12 | 24 | DDR_A_D13 |
| DDR_A_BG1 | 113 | BG1 | DQ13 | 25 | DDR_A_D8 |
| DDR_A_BA0 | 150 | BA0 | DQ14 | 38 | DDR_A_D11 |
| DDR_A_BA1 | 145 | BA1 | DQ15 | 37 | DDR_A_D14 |
| | | | DQS1(T) | 34 | DDR_A_DQS1 |
| | | | DQS1#(C) | 32 | DDR_A_DQS#1 |
| DDR_A_MA0 | 144 | A0 | | | |
| DDR_A_MA1 | 133 | A1 | DQ16 | 50 | DDR_A_D21 |
| DDR_A_MA2 | 132 | A2 | DQ17 | 49 | DDR_A_D20 |
| DDR_A_MA3 | 131 | A3 | DQ18 | 62 | DDR_A_D19 |
| DDR_A_MA4 | 128 | A4 | DQ19 | 63 | DDR_A_D22 |
| DDR_A_MA5 | 126 | A5 | DQ20 | 46 | DDR_A_D17 |
| DDR_A_MA6 | 127 | A6 | DQ21 | 45 | DDR_A_D16 |
| DDR_A_MA7 | 122 | A7 | DQ22 | 58 | DDR_A_D18 |
| DDR_A_MA8 | 125 | A8 | DQ23 | 59 | DDR_A_D23 |
| DDR_A_MA9 | 121 | A9 | DQS2(T) | 55 | DDR_A_DQS2 |
| DDR_A_MA10 | 146 | A10_AP | DQS2#(C) | 53 | DDR_A_DQS#2 |
| DDR_A_MA11 | 120 | A11 | | | |
| DDR_A_MA12 | 119 | A12 | DQ24 | 70 | DDR_A_D24 |
| DDR_A_MA13 | 158 | A13 | DQ25 | 71 | DDR_A_D29 |
| DDR_A_MA14 | 151 | A14_WE# | DQ26 | 83 | DDR_A_D25 |
| DDR_A_MA15 | 156 | A15_CAS# | DQ27 | 84 | DDR_A_D26 |
| DDR_A_MA16 | 152 | A16_RAS# | DQ28 | 66 | DDR_A_D28 |
| | | | DQ29 | 67 | DDR_A_D27 |
| DDR_A_ACT# | 114 | ACT# | DQ30 | 79 | DDR_A_D31 |
| | | | DQ31 | 80 | DDR_A_D30 |
| DDR_A_PAR | 143 | PARITY | DQS3(T) | 76 | DDR_A_DQS3 |
| DDR_A_ALERT# | 116 | ALERT# | DQS3#(C) | 74 | DDR_A_DQS#3 |
| DDR_A_EVENT# | 134 | EVENT# | | | |
| DDR_DRAMRST# | 108 | RESET# | | | |
| | | | DQ32 | 174 | DDR_A_D32 |
| | | | DQ33 | 173 | DDR_A_D37 |
| | | | DQ34 | 187 | DDR_A_D39 |
| | | | DQ35 | 186 | DDR_A_D34 |
| SOC_SMBDATA_1 | 254 | SDA | DQ36 | 170 | DDR_A_D35 |
| SOC_SMBCLK_1 | 253 | SCL | DQ37 | 169 | DDR_A_D36 |
| | | | DQ38 | 183 | DDR_A_D38 |
| DDR_A_SA2 | 166 | SA2 | DQ39 | 182 | DDR_A_D33 |
| DDR_A_SA1 | 260 | SA1 | DQS4(T) | 179 | DDR_A_DQS4 |
| DDR_A_SA0 | 256 | SA0 | DQS4#(C) | 177 | DDR_A_DQS#4 |
| | | | | | |
| | 92 | CB0_NC | DQ40 | 195 | DDR_A_D44 |
| | 91 | CB1_NC | DQ41 | 194 | DDR_A_D45 |
| | 101 | CB2_NC | DQ42 | 207 | DDR_A_D43 |
| | 105 | CB3_NC | DQ43 | 208 | DDR_A_D47 |
| | 88 | CB4_NC | DQ44 | 191 | DDR_A_D40 |
| | 87 | CB5_NC | DQ45 | 190 | DDR_A_D41 |
| | 100 | CB6_NC | DQ46 | 203 | DDR_A_D42 |
| | 104 | CB7_NC | DQ47 | 204 | DDR_A_D46 |
| DDR_A_DQS8 | 97 | DQS8(T) | DQS5(T) | 200 | DDR_A_DQS5 |
| DDR_A_DQS#8 | 95 | DQS8#(C) | DQS5#(C) | 198 | DDR_A_DQS#5 |
| | | | | | |
| | 12 | DM0#/DBI0# | DQ48 | 216 | DDR_A_D53 |
| | 33 | DM1#/DBI1# | DQ49 | 215 | DDR_A_D51 |
| | 54 | DM2#/DBI2# | DQ50 | 228 | DDR_A_D54 |
| | 75 | DM3#/DBI3# | DQ51 | 229 | DDR_A_D49 |
| | 178 | DM4#/DBI4# | DQ52 | 211 | DDR_A_D52 |
| | 199 | DM5#/DBI5# | DQ53 | 212 | DDR_A_D48 |
| | 220 | DM6#/DBI6# | DQ54 | 224 | DDR_A_D55 |
| | 241 | DM7#/DBI7# | DQ55 | 225 | DDR_A_D50 |
| | 96 | DM8#/DBI8# | DQS6(T) | 221 | DDR_A_DQS6 |
| | | | DQS6#(C) | 219 | DDR_A_DQS#6 |
| | | | | | |
| | | | DQ56 | 237 | DDR_A_D60 |
| | | | DQ57 | 236 | DDR_A_D56 |
| | | | DQ58 | 249 | DDR_A_D58 |
| | | | DQ59 | 250 | DDR_A_D63 |
| | | | DQ60 | 232 | DDR_A_D61 |
| | | | DQ61 | 233 | DDR_A_D57 |
| | | | DQ62 | 245 | DDR_A_D62 |
| | | | DQ63 | 246 | DDR_A_D59 |
| | | | DQS7(T) | 242 | DDR_A_DQS7 |
| | | | DQS7#(C) | 240 | DDR_A_DQS#7 |

DEREN_40-42271-26001RHF
CONN@
SP07001EZ00

**Symbol:SP07001EGA0(H=5.2)**

+1.2V_VDDQ
RD71 2 — 1 240_0402_1%
(8,20) DDR_DRAMRST#
+1.2V_VDDQ
RD72 1 — @ — 2 470_0402_5%
CD73 2 — 1 .1U_0402_16V7K
@ESD@

+1.2V_VDDQ
RD73 2 — 1 240_0402_1%
RD74 2 — 1 240_0402_1%

+0.6V_A_VREFCA
RD65 1K_0402_1%
RD68 2_0402_1%
RD69 1K_0402_1%
RD70 24.9_0402_1%
CD71 0.022U_0402_16V7K
+0.6V_DDRA_VREFCA
10mils
CD72 0.1U_0201_10V6K

**Place near to SO-DIMM connector.**

JDIMM1B
REVERSE

| | | | | | |
|---|---|---|---|---|---|
| | 111 | VDD1 | VDD11 | 141 | |
| | 112 | VDD2 | VDD12 | 142 | |
| | 117 | VDD3 | VDD13 | 147 | |
| | 118 | VDD4 | VDD14 | 148 | |
| | 123 | VDD5 | VDD15 | 153 | |
| | 124 | VDD6 | VDD16 | 154 | |
| | 129 | VDD7 | VDD17 | 159 | |
| | 130 | VDD8 | VDD18 | 160 | |
| | 135 | VDD9 | VDD19 | 163 | |
| | 136 | VDD10 | | | |
| +3VS | 255 | VDDSPD | VTT | 258 | +0.6VS_VTT |
| | 164 | VREFCA | VPP1 | 257 | +2.5V |
| | | | VPP2 | 259 | |
| | 1 | VSS | VSS | 99 | |
| | 2 | VSS | VSS | 102 | |
| | 5 | VSS | VSS | 103 | |
| | 6 | VSS | VSS | 106 | |
| | 9 | VSS | VSS | 107 | |
| | 10 | VSS | VSS | 167 | |
| | 14 | VSS | VSS | 168 | |
| | 15 | VSS | VSS | 171 | |
| | 18 | VSS | VSS | 172 | |
| | 19 | VSS | VSS | 175 | |
| | 22 | VSS | VSS | 176 | |
| | 23 | VSS | VSS | 180 | |
| | 26 | VSS | VSS | 181 | |
| | 27 | VSS | VSS | 184 | |
| | 30 | VSS | VSS | 185 | |
| | 31 | VSS | VSS | 188 | |
| | 35 | VSS | VSS | 189 | |
| | 36 | VSS | VSS | 192 | |
| | 39 | VSS | VSS | 193 | |
| | 40 | VSS | VSS | 196 | |
| | 43 | VSS | VSS | 197 | |
| | 44 | VSS | VSS | 201 | |
| | 47 | VSS | VSS | 202 | |
| | 48 | VSS | VSS | 205 | |
| | 51 | VSS | VSS | 206 | |
| | 52 | VSS | VSS | 209 | |
| | 56 | VSS | VSS | 210 | |
| | 57 | VSS | VSS | 213 | |
| | 60 | VSS | VSS | 214 | |
| | 61 | VSS | VSS | 217 | |
| | 64 | VSS | VSS | 218 | |
| | 65 | VSS | VSS | 222 | |
| | 68 | VSS | VSS | 223 | |
| | 69 | VSS | VSS | 226 | |
| | 72 | VSS | VSS | 227 | |
| | 73 | VSS | VSS | 230 | |
| | 77 | VSS | VSS | 231 | |
| | 78 | VSS | VSS | 234 | |
| | 81 | VSS | VSS | 235 | |
| | 82 | VSS | VSS | 238 | |
| | 85 | VSS | VSS | 239 | |
| | 86 | VSS | VSS | 243 | |
| | 89 | VSS | VSS | 244 | |
| | 90 | VSS | VSS | 247 | |
| | 93 | VSS | VSS | 248 | |
| | 94 | VSS | VSS | 251 | |
| | 98 | VSS | VSS | 252 | |
| | 262 | GND | GND | 261 | |

DEREN_40-42271-26001RHF
CONN@

**Layout Note:**
**Place near JDIMM1.258**

+0.6VS_VTT
CD90 10U_0402_6.3V6M
CD91 1U_0201_6.3V6M
CD92 1U_0201_6.3V6M

**Layout Note:**
**Place near JDIMM1.257,259**

+2.5V
CD241
CD93
CD94 1U_0201_6.3V6M
10U_0402_6.3V6M
10U_0402_6.3V6M
add 1 cap for MLCC downsize

**Layout Note:**
**Place near JDIMM1.255**

#575412 WHL-U PDG R0.7 Table 4-23
add 0.1UF

+3VS
CD243 2.2U_0201_6.3V6M
CD95 2.2U_0201_6.3V6M
CD238 1U_0402_16V7K
add 1 cap for MLCC downsize

+1.2V_VDDQ
**Follow MA51**
CD237 330U_D2_2V_Y
**SGA00009S00**
**330U 2V H1.9**
**9mohm POLY**

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



Compal Electronics, Inc.

Title: DDR4 DIMMA

| Size | Document Number | Rev |
|---|---|---|
| Custom | Raticate_KL M/B LA-H441P | 0.1 |

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# Standard Type

2-3A to 1 DIMMs/channel

(8) DDR_B_DQS#[0..7]
(8) DDR_B_D[0..63]
(8) DDR_B_DQS[0..7]

(8) DDR_B_MA[0..16]
(8) DDR_B_BA0 — DDR_B_BA0
(8) DDR_B_BA1 — DDR_B_BA1
(8) DDR_B_BG0 — DDR_B_BG0
(8) DDR_B_BG1 — DDR_B_BG1
(8) DDR_B_ACT# — DDR_B_ACT#
(8) DDR_B_ALERT# — DDR_B_ALERT#
(8) DDR_B_PAR — DDR_B_PAR

(8) DDR_B_CLK0 — DDR_B_CLK0
(8) DDR_B_CLK#0 — DDR_B_CLK#0
(8) DDR_B_CLK1 — DDR_B_CLK1
(8) DDR_B_CLK#1 — DDR_B_CLK#1

(8) DDR_B_CKE0 — DDR_B_CKE0
(8) DDR_B_CKE1 — DDR_B_CKE1
(8) DDR_B_CS#0 — DDR_B_CS#0
(8) DDR_B_CS#1 — DDR_B_CS#1

(9,19,33) SOC_SMBDATA_1 — SOC_SMBDATA_1
(9,19,33) SOC_SMBCLK_1 — SOC_SMBCLK_1

(8) DDR_B_ODT0 — DDR_B_ODT0
(8) DDR_B_ODT1 — DDR_B_ODT1

+3VS
RD52 0_0402_5% @
DDR_B_SA2
DDR_B_SA1
DDR_B_SA0
RD54 0_0402_5% @
RD56 0_0402_5% @

**Layout Note:**
**Place near JDIMM2**

+1.2V_VDDQ
CD32 1U_0201_6.3V6M
CD33 1U_0201_6.3V6M
CD34 1U_0201_6.3V6M
CD35 1U_0201_6.3V6M
CD36 1U_0201_6.3V6M
CD37 1U_0201_6.3V6M
CD69 1U_0201_6.3V6M
CD70 1U_0201_6.3V6M

+1.2V_VDDQ
CD38 10U_0402_6.3V6M
CD39 10U_0402_6.3V6M
CD40 10U_0402_6.3V6M
CD41 10U_0402_6.3V6M
CD42 10U_0402_6.3V6M
CD43 10U_0402_6.3V6M
CD44 10U_0402_6.3V6M
CD45 10U_0402_6.3V6M

JDIMM2A (STD)

| | | | | | |
|---|---|---|---|---|---|
| DDR_B_CLK0 | 137 | CK0(T) | DQ0 | 8 | DDR_B_D11 |
| DDR_B_CLK#0 | 139 | CK0#(C) | DQ1 | 7 | DDR_B_D14 |
| DDR_B_CLK1 | 138 | CK1(T) | DQ2 | 20 | DDR_B_D8 |
| DDR_B_CLK#1 | 140 | CK1#(C) | DQ3 | 21 | DDR_B_D13 |
| | | | DQ4 | 4 | DDR_B_D10 |
| DDR_B_CKE0 | 109 | CKE0 | DQ5 | 3 | DDR_B_D15 |
| DDR_B_CKE1 | 110 | CKE1 | DQ6 | 16 | DDR_B_D9 |
| | | | DQ7 | 17 | DDR_B_D12 |
| DDR_B_CS#0 | 149 | S0# | DQS0(T) | 13 | DDR_B_DQS1 |
| DDR_B_CS#1 | 157 | S1# | DQS0#(C) | 11 | DDR_B_DQS#1 |
| | 162 | S2#/C0 | | | |
| | 165 | S3#/C1 | | 28 | DDR_B_D0 |
| DDR_B_ODT0 | 155 | | DQ8 | 29 | DDR_B_D4 |
| DDR_B_ODT1 | 161 | ODT0 | DQ9 | 41 | DDR_B_D2 |
| | | ODT1 | DQ10 | 42 | DDR_B_D3 |
| DDR_B_BG0 | 115 | | DQ11 | 24 | DDR_B_D1 |
| DDR_B_BG1 | 113 | BG0 | DQ12 | 25 | DDR_B_D5 |
| DDR_B_BA0 | 150 | BG1 | DQ13 | 38 | DDR_B_D6 |
| DDR_B_BA1 | 145 | BA0 | DQ14 | 37 | DDR_B_D7 |
| | | BA1 | DQ15 | 34 | DDR_B_DQS0 |
| DDR_B_MA0 | 144 | | DQS1(T) | 32 | DDR_B_DQS#0 |
| DDR_B_MA1 | 133 | A0 | DQS1#(C) | | |
| DDR_B_MA2 | 132 | A1 | DQ16 | 50 | DDR_B_D17 |
| DDR_B_MA3 | 131 | A2 | DQ17 | 49 | DDR_B_D21 |
| DDR_B_MA4 | 128 | A3 | DQ18 | 62 | DDR_B_D22 |
| DDR_B_MA5 | 126 | A4 | DQ19 | 63 | DDR_B_D19 |
| DDR_B_MA6 | 127 | A5 | DQ20 | 46 | DDR_B_D20 |
| DDR_B_MA7 | 122 | A6 | DQ21 | 45 | DDR_B_D16 |
| DDR_B_MA8 | 125 | A7 | DQ22 | 58 | DDR_B_D23 |
| DDR_B_MA9 | 121 | A8 | DQ23 | 59 | DDR_B_D18 |
| DDR_B_MA10 | 146 | A9 | DQS2(T) | 55 | DDR_B_DQS2 |
| DDR_B_MA11 | 120 | A10_AP | DQS2#(C) | 53 | DDR_B_DQS#2 |
| DDR_B_MA12 | 119 | A11 | | | |
| DDR_B_MA13 | 158 | A12 | DQ24 | 70 | DDR_B_D25 |
| DDR_B_MA14 | 151 | A13 | DQ25 | 71 | DDR_B_D29 |
| DDR_B_MA15 | 156 | A14_WE# | DQ26 | 83 | DDR_B_D30 |
| DDR_B_MA16 | 152 | A15_CAS# | DQ27 | 84 | DDR_B_D27 |
| | | A16_RAS# | DQ28 | 66 | DDR_B_D28 |
| DDR_B_ACT# | 114 | | DQ29 | 67 | DDR_B_D24 |
| | | ACT# | DQ30 | 79 | DDR_B_D31 |
| DDR_B_PAR | 143 | | DQ31 | 80 | DDR_B_D26 |
| DDR_B_ALERT# | 116 | PARITY | DQS3(T) | 76 | DDR_B_DQS3 |
| DDR_B_EVENT# | 134 | ALERT# | DQS3#(C) | 74 | DDR_B_DQS#3 |
| DDR_DRAMRST# | 108 | EVENT# | | | |
| | | RESET# | DQ32 | 174 | DDR_B_D32 |
| | | | DQ33 | 173 | DDR_B_D37 |
| SOC_SMBDATA_1 | 254 | | DQ34 | 187 | DDR_B_D39 |
| SOC_SMBCLK_1 | 253 | SDA | DQ35 | 186 | DDR_B_D35 |
| | | SCL | DQ36 | 170 | DDR_B_D33 |
| DDR_B_SA2 | 166 | | DQ37 | 169 | DDR_B_D36 |
| DDR_B_SA1 | 260 | SA2 | DQ38 | 183 | DDR_B_D38 |
| DDR_B_SA0 | 256 | SA1 | DQ39 | 182 | DDR_B_D34 |
| | | SA0 | DQS4(T) | 179 | DDR_B_DQS4 |
| | | | DQS4#(C) | 177 | DDR_B_DQS#4 |
| | 92 | | | | |
| | 91 | CB0_NC | DQ40 | 195 | DDR_B_D44 |
| | 101 | CB1_NC | DQ41 | 194 | DDR_B_D40 |
| | 105 | CB2_NC | DQ42 | 207 | DDR_B_D47 |
| | 88 | CB3_NC | DQ43 | 208 | DDR_B_D42 |
| | 87 | CB4_NC | DQ44 | 191 | DDR_B_D45 |
| | 100 | CB5_NC | DQ45 | 190 | DDR_B_D41 |
| | 104 | CB6_NC | DQ46 | 203 | DDR_B_D46 |
| | 97 | CB7_NC | DQ47 | 204 | DDR_B_D43 |
| DDR_B_DQS8 | 95 | DQS8(T) | DQS5(T) | 200 | DDR_B_DQS5 |
| DDR_B_DQS#8 | | DQS8#(C) | DQS5#(C) | 198 | DDR_B_DQS#5 |
| | | | | 216 | DDR_B_D48 |
| | 12 | | DQ48 | 215 | DDR_B_D53 |
| | 33 | DM0#/DBI0# | DQ49 | 228 | DDR_B_D54 |
| | 54 | DM1#/DBI1# | DQ50 | 229 | DDR_B_D50 |
| | 75 | DM2#/DBI2# | DQ51 | 211 | DDR_B_D52 |
| | 178 | DM3#/DBI3# | DQ52 | 212 | DDR_B_D49 |
| | 199 | DM4#/DBI4# | DQ53 | 224 | DDR_B_D55 |
| | 220 | DM5#/DBI5# | DQ54 | 225 | DDR_B_D51 |
| | 241 | DM6#/DBI6# | DQ55 | 221 | DDR_B_DQS6 |
| | 96 | DM7#/DBI7# | DQS6(T) | 219 | DDR_B_DQS#6 |
| | | DM8#/DBI8# | DQS6#(C) | | |
| | | | | 237 | DDR_B_D60 |
| | | | DQ56 | 236 | DDR_B_D56 |
| | | | DQ57 | 249 | DDR_B_D58 |
| | | | DQ58 | 250 | DDR_B_D63 |
| | | | DQ59 | 232 | DDR_B_D57 |
| | | | DQ60 | 233 | DDR_B_D61 |
| | | | DQ61 | 245 | DDR_B_D59 |
| | | | DQ62 | 246 | DDR_B_D62 |
| | | | DQ63 | 242 | DDR_B_DQS7 |
| | | | DQS7(T) | 240 | DDR_B_DQS#7 |
| | | | DQS7#(C) | | |

FOX_AS0A821-H4SB-7H
CONN@
SP07001GA00

+1.2V_VDDQ
RD63 2 — 1 240_0402_1%
(8,19) DDR_DRAMRST#
RD1 1 — 2 470_0402_5%
CD30 2 — 1 .1U_0402_16V7K
@ESD@

+1.2V_VDDQ
RD61 2 — 1 240_0402_1%
RD62 2 — 1 240_0402_1%

+1.2V_VDDQ

+0.6V_B_VREFCA
RD46 1K_0402_1%
RD49 2_0402_1%
RD47 1K_0402_1%
RD50 24.9_0402_1%
CD66 0.022U_0402_16V7K
+0.6V_DDRB_VREFCA
10mils
CD65 0.1U_0201_10V6K

Place near to SO-DIMM connector.

JDIMM2B (STD)

| | | | | | |
|---|---|---|---|---|---|
| | 111 | VDD1 | VDD11 | 141 | |
| | 112 | VDD2 | VDD12 | 147 | |
| | 117 | VDD3 | VDD13 | 148 | |
| | 118 | VDD4 | VDD14 | 153 | |
| | 123 | VDD5 | VDD15 | 154 | |
| | 124 | VDD6 | VDD16 | 159 | |
| | 129 | VDD7 | VDD17 | 160 | |
| | 130 | VDD8 | VDD18 | 163 | |
| | 135 | VDD9 | VDD19 | | |
| | 136 | VDD10 | | | |
| +3VS | 255 | VDDSPD | VTT | 258 | +0.6VS_VTT |
| | 164 | VREFCA | VPP1 | 257 | +2.5V |
| | | | VPP2 | 259 | |
| | 1 | VSS | VSS | 99 | |
| | 2 | VSS | VSS | 102 | |
| | 5 | VSS | VSS | 103 | |
| | 6 | VSS | VSS | 106 | |
| | 9 | VSS | VSS | 107 | |
| | 10 | VSS | VSS | 167 | |
| | 14 | VSS | VSS | 168 | |
| | 15 | VSS | VSS | 171 | |
| | 18 | VSS | VSS | 172 | |
| | 19 | VSS | VSS | 175 | |
| | 22 | VSS | VSS | 176 | |
| | 23 | VSS | VSS | 180 | |
| | 26 | VSS | VSS | 181 | |
| | 27 | VSS | VSS | 184 | |
| | 30 | VSS | VSS | 185 | |
| | 31 | VSS | VSS | 188 | |
| | 35 | VSS | VSS | 189 | |
| | 36 | VSS | VSS | 192 | |
| | 39 | VSS | VSS | 193 | |
| | 40 | VSS | VSS | 196 | |
| | 43 | VSS | VSS | 197 | |
| | 44 | VSS | VSS | 201 | |
| | 47 | VSS | VSS | 202 | |
| | 48 | VSS | VSS | 205 | |
| | 51 | VSS | VSS | 206 | |
| | 52 | VSS | VSS | 209 | |
| | 56 | VSS | VSS | 210 | |
| | 57 | VSS | VSS | 213 | |
| | 60 | VSS | VSS | 214 | |
| | 61 | VSS | VSS | 217 | |
| | 64 | VSS | VSS | 218 | |
| | 65 | VSS | VSS | 222 | |
| | 68 | VSS | VSS | 223 | |
| | 69 | VSS | VSS | 226 | |
| | 72 | VSS | VSS | 227 | |
| | 73 | VSS | VSS | 230 | |
| | 77 | VSS | VSS | 231 | |
| | 78 | VSS | VSS | 234 | |
| | 81 | VSS | VSS | 235 | |
| | 82 | VSS | VSS | 238 | |
| | 85 | VSS | VSS | 239 | |
| | 86 | VSS | VSS | 243 | |
| | 89 | VSS | VSS | 244 | |
| | 90 | VSS | VSS | 247 | |
| | 93 | VSS | VSS | 248 | |
| | 94 | VSS | VSS | 251 | |
| | 98 | VSS | VSS | 252 | |
| | 262 | GND | GND | 261 | |

FOX_AS0A821-H4SB-7H
CONN@
SP07001GA00

**Layout Note:**
**Place near JDIMM1.258**

+0.6VS_VTT
CD64 10U_0402_6.3V6M
CD62 1U_0201_6.3V6M
CD63 1U_0201_6.3V6M

**Layout Note:**
**Place near JDIMM1.257,259**

+2.5V
CD240 10U_0402_6.3V6M
CD68 10U_0402_6.3V6M
CD67 1U_0201_6.3V6M
add 1 cap for MLCC downsize

**Layout Note:**
**Place near JDIMM2.255**

#575412 WHL-U PDG R0.7 Table 4-23
add 0.1UF

+3VS
CD242 2.2U_0201_6.3V6M
CD55 2.2U_0201_6.3V6M
CD239 .1U_0402_16V7K
add 1 cap for MLCC downsize

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



Compal Electronics, Inc.

Title: DDR4 DIMMB

| Size | Document Number | Rev |
|---|---|---|
| Custom | Raticate_KL M/B LA-H441P | 0.1 |

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## N16 GPU

| GPIO | I/O | USAGE |
|---|---|---|
| GPIO0 | O | GC6_FB_EN |
| GPIO1 | O | MEM_VDD_CTL |
| GPIO2 | O | LCD_BL_PWM |
| GPIO3 | O | LCD_VCC |
| GPIO4 | O | LCD_BLEN |
| GPIO5 | O | 3V3_MAIN_EN |
| GPIO6 | I | GPU_EVENT# |
| GPIO7 | O | 3D Vision |
| GPIO8 | I | SYS_PEX_RST_MON# |
| GPIO9 | I/O | THERM_ALERT |
| GPIO10 | O | MEM_VREF_CTL |
| GPIO11 | O | PWM_VID |
| GPIO12 | I | PWR_LEVEL |
| GPIO13 | O | PSI |
| GPIO14 | I | HPD_A |
| GPIO15 | I | HPD_C |
| GPIO16 | I | FRAME_LOCK# |
| GPIO17 | I | HPD_D |
| GPIO18 | I | HPD_E |
| GPIO19 | I | HPD_F or HPD_B |
| GPIO20 | | Reserved |
| GPIO21 | O | GPU_PEX_RST_HOLD# |
| GPIO22 | | |
| GPIO23 | | |

## N17 GPU

| GPIO | I/O | USAGE |
|---|---|---|
| GPIO0 | O | PWM_VID |
| GPIO1 | O | GC6_FB_EN |
| GPIO2 | I | GPU_EVENT# |
| GPIO3 | I/O | NVVDDS_PWM |
| GPIO4 | O | 1V8_MAIN_EN |
| GPIO5 | I | FRAME_LOCK# |
| GPIO6 | O | PSI |
| GPIO7 | O | LCD_BL_PWM |
| GPIO8 | O | MEM_VDD_CTL |
| GPIO9 | I/O | THERM_ALERT |
| GPIO10 | O | MEM_VREF_CTL |
| GPIO11 | O | LCD_VDD |
| GPIO12 | I | PWR_LEVEL |
| GPIO13 | O | LCD_BLEN |
| GPIO14 | I | HPD_IFPA |
| GPIO15 | I | HPD_IFPB |
| GPIO16 | | Reserved |
| GPIO17 | I | HPD_IFPD |
| GPIO18 | I | HPD_IFPE |
| GPIO19 | O | 3D_VISION |
| GPIO20 | | Reserved |
| GPIO21 | | Reserved (OC_WARN) |
| GPIO22 | | Reserved |
| GPIO23 | | Reserved |

## DA-08329-001_V02

Table 8. Other PLLs Power Decoupling and Filtering

| GPU | Type | Footprint | Population N16 | Population N17 | Location |
|---|---|---|---|---|---|
| **PLLVDD (N17: XS_PLLVDD) Supply Rail** | | | | | |
| GB2B-64, GB2C-64 | 0.1 µF X7R | 0402 | 1 | 1 | Under GPU |
| | 22 µF X5R | 0805 | 1 | 0 | Near GPU |
| | **Bead Type** | | | | |
| | L2=30 Ω (ESR=0.05 Ω) | 0402 | 1 | 0 | Near GPU |
| **SP_PLLVDD and VID_PLLVDD Combined Supply Rails** | | | | | |
| GB2B-64, GB2C-64 | 0.1 µF X7R | 0402 | 2 | 2 | Under GPU |
| | 10 µF X5R | 0603 | 1 | 0 | Near GPU |
| | 47 µF X5R | 0805 | 1 | 0 | Near GPU |
| | **Bead Type** | | | | |
| | L2=300 Ω (ESR=0.2 Ω) | 0603 | 1 | 0 | Near GPU |

## GC6 2.0 function

Table 15-8. I2CS Slave Address

| SMBUS_ALT_ADDR | Description |
|---|---|
| 0 | 0x9E (Default) |
| 1 | 0x9C (multi-GPU usage) |

### 10.2.2 I²CS Slave Address

N16x GPUs use I²CS slave address 0x96h for NVIDIA internal testing. I²C address 0x96h must not be used by other I²C devices on the same bus as the GPU to avoid address conflict. The SMB_ALT_ADDR strap does not affect this 0x96h address. Refer to Chapter

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



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|---|---|---|---|
| Title: N16X PEG 1/9 | | | |
| Size: Custom | Document Number: Raticate KL M/B LA-H441P | | Rev: 0.1 |
| Date: Friday, November 30, 2018 | Sheet 21 of 57 | | |

# VRAM Interface

(26) MDA[15..0] MDA[15..0]
(26) MDA[31..16] MDA[31..16]
(27) MDA[47..32] MDA[47..32]
(27) MDA[63..48] MDA[63..48]

UGPU1
S IC N16S-GTR-S-A2 BGA 595P GPU ABO !
N16SGTR@
SA00009FP40

UGPU1
S IC N17S-G1-A1 BGA 595P GPU ABO !
N17SG1@
SA0000ANV10

UGPU1
S IC N17S-G0-A1 BGA 595P GPU ABO !
N17SG0@
SA0000CC920

UGPU1B
Part 2 of 6
MEMORY INTERFACE A
GM108-ES-S-A1_FCBGA595
@

CMDA[31..0] (26,27)

+1.35VSDGPU

CMDA14 2 VGA@ 1 RV87 10K_0402_5%
CMDA30 2 VGA@ 1 RV88 10K_0402_5%
CMDA13 2 VGA@ 1 RV89 10K_0402_5%
CMDA29 2 VGA@ 1 RV90 10K_0402_5%

+3VS

Power Side PU to +3VS_1.8VSDGPU_AON

RV106 10K_0402_5% @
RV108 10K_0402_5% @
QV7A @
QV7B PJT138KA 2N SOT363-6 @
PJT138KA 2N SOT363-6
RV188 0_0402_5% 1 VGA@ 2 VGA_CORE_PG
DV10 N17S@ RB751S40T1G_SOD523-2
RV103 10K_0402_1% 2 @ 1
DGPU_MAIN_EN
CV231 @ .1U_0402_16V7K
(21,40) 3_1.8VSDGPU_MAIN_EN

UV10 N16X@ MC74VHC1G08DFT2G_SC70-5 SA00000OH00
VCC: 2.0 ~ 5.5V
Push Pull Output

+3VS_1.8VSDGPU_AON
VCC: 1.65 ~ 5.5V
Push Pull Output
IN B VCC IN A GND OUT Y
PEX_VDD_EN
PEX_VDD_EN (40,52)
UV10 N17S@ NL17SZ08DFT2G_SC70-5
DGPU_PWR_EN (12,40)

DV7 N17S@ RB751S40T1G_SOD523-2
(21,36) GPU_OVERT#
RV189 N17S@ 2.2K_0402_5% SD028220180
PVT 03/09
RV189 1 N16X@ 2 1K_0402_1% NVVDD_EN (53)
DV11 RB751S40T1G_SOD523-2
CV263 .1U_0402_16V7K VGA@

+3VS_1.8VSDGPU_AON
CV230 0.1U_0201_10V6K @
(21) PLTRST_VGA#
PLTRST_VGA#
RV102 10K_0402_5%
(21) GC6_FB_EN1V8
QV6A PJT138KA 2N SOT363-6 @
QV6B PJT138KA 2N SOT363-6 @
UV9 NL17SZ08DFT2G_SC70-5
VCC: 1.65 ~ 5.5V
Push Pull Output
VGA_CORE_PG
VGA_CORE_PG (53)
Near Power PWM IC
DV11 change to @ for wavefrom glitch
Thermal shutdown protection
change to @ for wavefrom glitch

UV9 N16X@ MC74VHC1G08DFT2G_SC70-5 SA00000OH00
QV6 N16X@ 2N7002KDW_SOT363-6 SB00000EO00
VCC: 2.0 ~ 5.5V
Push Pull Output

+PEX_IOVDDQ
15+55mA
Place Under F16 P22
+FB_PLLAVDD
L2002 PBY160808T-300Y-N_2P
C2008 VGA@ 22U_0603_6.3V6M
C2011 VGA@ .1U_0402_16V7K
C2010 VGA@ .1U_0402_16V7K
C2009 N17S@ 0.1U_0201_10V6K
C2736 N17S@ 0.1U_0201_10V6K
Place Near GPU
Place Under H22
SM010008A00 3000ma 30ohm@100mhz DCR 0.03

## DA-08329-001_V01

Table 5. Frame Buffer PLLs Decoupling and Filtering

| GPU | Capacitor Type | | Footprint | Population N16 | Population N17 | Location |
|---|---|---|---|---|---|---|
| **FB PLL Supply Rail for GDDR5** | | | | | | |
| GB2B-64, GB2C-64 | 0.1 µF | X7R | 0402 | 2 | 4 | Under GPU |
| | 22 µF | X6S | 0805 | 1 | 1 | Near GPU |
| | **Bead Type** | | | | | |
| | 30 Ω (ESR=0.010 Ω) | | 0603 | 1 | 1 | Near GPU |

## NV 15x DG-06803-V03
## NV 16x DG-07158-V04

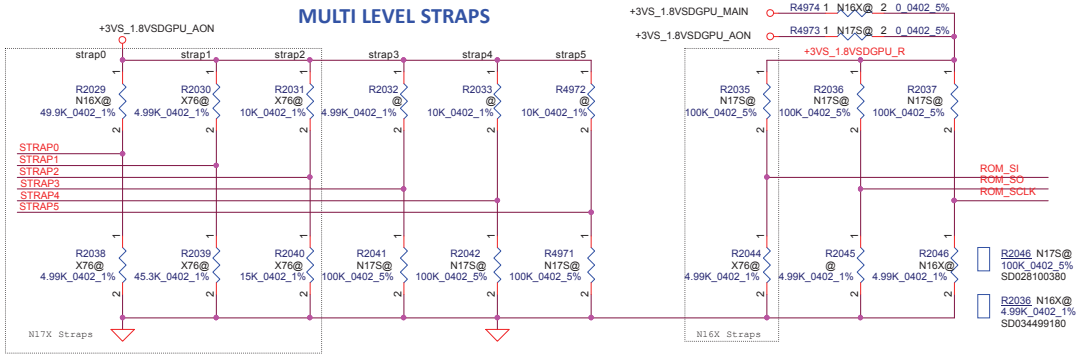
| GPU Package | Rail | Capacitor Type | | Footprint | Population | Location |
|---|---|---|---|---|---|---|
| GB2B-64 | FBx_PLL_AVDD and FB_DLL_AVDD Combined | 0.1 µF | X7R | 0402 | 2 | Under GPU |
| | | 22 µF | X5R | 0805 | 1 | Near GPU |
| | | **Bead Type** | | | | |
| | | 30 Ω (ESR=0.010 Ω) | | 0603 | 1 | Near GPU |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



Compal Electronics, Inc.
Title: N16X VRAM 2/9
Size: Custom | Document Number: Raticate KL M/B LA-H441P | Rev: 0.1
Date: Friday, November 30, 2018 | Sheet 22 of 57

## MULTI LEVEL STRAPS




## Multi strap table

MX110 Decive ID : N16V-GMR1 0x174E
MX130 Decive ID : N16S-GTR 0x174D

| GPU | VRAM Voltage | RANK | X76 | Freq | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | strap5 | ROM_SI | ROM_SO | ROM_SCLK |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N16V-GMR1 N16S-GTR | +1.35V | | X76793BOL03 | 2.5GHz | 256Mx32x2 2G | 0x8 (SA00009TV50) Micron MT51J256M32HF-70:B | PU 49.9K | NC | NC | NC | NC | NC | PU 4.99K | PU 4.99K | PD 4.99K |
| | | | X76793BOL04 | | | 0x9 (SA00009U160) Hynix H5GC8H24AJR-R0C | | | | | | | PU 10K | | |
| | | | | | | | | | | | | | | | |
| | | | X76739BOL04 | | | 0x0 (SA000094R30) Samsung K4G80325FB-HC03 | | | | | | | PD 4.99K | | |
| | | | X76739BOL05 | | | 0x5(SA00009ZG20) Hynix H5GC8H24MJR-T2C | | | | | | | PD 30.1K | | |
| | | | X76739BOL06 | | | 0x1 (SA000096K30) Micron MT51J256M32HF-60:A | | | | | | | PD 10K | | |

## Multi strap table

MX230 Decive ID : N17S-G0-A1 0x1D10
MX150 Decive ID : N17S-G1-A1 0x1D10

| GPU | VRAM Voltage | RANK | X76 | Freq | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | strap5 | ROM_SI | ROM_SO | ROM_SCLK |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N17S- G1 | +1.35V | | X76793BOL01 | 3.0GHz | 256Mx32x2 2G | 0x4 (SA00009TV50) Micron MT51J256M32HF-70:B | PD 100K | PD 100K | PU 100K | PD 100K | | | PU 100K | PU 100K | PU 100K |
| | | | X76793BOL02 | | | 0x5 (SA00009U160) Hynix H5GC8H24AJR-R0C | PU 100K | PD 100K | PU 100K | | | | | | PD 100K |
| | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | |
| | | | X76739BOL07 | | | 0x0 (SA000092D00) Samsung K4G80325FB-HC28 | PD 100K | PD 100K | PD 100K | | | | | | |
| | | | X76739BOL08 | | | 0x2 (SA00009U110) Hynix H5GC8H24MJR-R0C | PD 100K | PU 100K | PD 100K | | | | | | |
| | | | X76739BOL09 | | | 0x1 (SA00009TV10) Micron MT51J256M32HF-70:A | PU 100K | PD 100K | PD 100K | | | | | | |

## NV16x Straps set t i g (ROM_SI => follow RVL)

| Physical Strapping pin | Bit3 | | Bit2 | | Bit1 | | Bit0 | | Result |
|---|---|---|---|---|---|---|---|---|---|
| ROM_SO | DEVID_SEL | *0 / 1 | PCIE_CFG | *0 / 1 | SMB_ALT_ADDR | 0: 0x9Eh * / 1: 0x9C (GPUs) | VGA_DEVICE | 0: 3D device (Optimus)* / 1: VGA device | PH 4.99K |
| ROM_SCLK | SOR3_EXPOSED (FP E/F) | 0 / 1 | SOR2_EXPOSED (FP D) | 0 / 1 | SOR1_EXPOSED (FP C) | 0 / 1 | SOR0_EXPOSED (FP A/B) | 0 / 1 | PL 4.99K |
| ROM_SI | RAMCFG[3] | 0 / 1 | RAMCFG[2] | 0 / 1 | RAMCFG[1] | 0 / 1 | RAMCFG[0] | 0 / 1 | PL 4.99K |
| STRAP4 | Reserve PH on 3V3_AON /PL foot print for further usage | | | | | | | | NA |
| STRAP3 | | | | | | | | | NA |
| STRAP2 | | | | | | | | | NA |
| STRAP1 | | | | | | | | | NA |
| STRAP0 | Pull up 49.9 KΩ to 3V3_AON and reserve Pull down resister foot print. | | | | | | | | PH49.9K |

## NV 16x DG-07158-V05

Table 3-4. GPU Core Sensing Line Routing Constrains

| Constraint Parameter | Requirement |
|---|---|
| Single-ended impedance | 25 Ω ± 10% |
| Differential Trace Impedance | 50 Ω ± 15% |
| Reference Plane | GND Reference |
| Routing Type | Stripline[1] or Microstrip |
| Dielectric spacing | Stripline: ≥ 3.0x dielectric<br>Microstrip: ≥ 4.0x dielectric |
| Intrapair skew | ≤ 5 ps |
| Via stub | |
| Trace length | GPU to $R_S/R_S$ ≤ 250 mm (9842.5 mil)<br>$R_S/R_S$ to VR ≤ 50 mm (1968.5 mil) |

Note:
1. Stripline is recommended to minimize EMI. Do not route over any voids.

Table 15-2. Resistance Mapping to Hex Values

| Resistor Values | Pull-Up to 3V3_MAIN | Pull-Down to GND |
|---|---|---|
| 4.99 kΩ | 1000 | 0000 |
| 10.0 kΩ | 1001 | 0001 |
| 15.0 kΩ | 1010 | 0010 |
| 20.0 kΩ | 1011 | 0011 |
| 24.9 kΩ | 1100 | 0100 |
| 30.1 kΩ | 1101 | 0101 |
| 34.8 kΩ | 1110 | 0110 |
| 45.3 kΩ | 1111 | 0111 |

## NV 17S DG-07785-001_V07

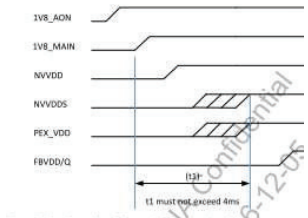



Figure 7.5 Example of Power-Up Sequencing Order

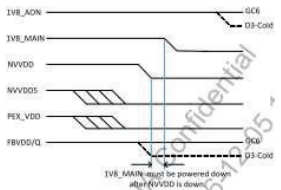
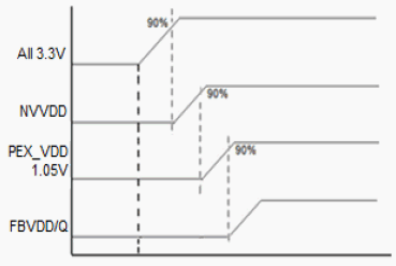



Figure 7.6 Example of Power-Down Sequencing Order

## VGA Power Sequence (N16X)




**Notes:** - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

## DA-08329-001_V02

Table 8. Other PLLs Power Decoupling and Filtering

| GPU | Type | Footprint | N16 | N17 | Location |
|---|---|---|---|---|---|
| **PLLVDD (N17: XS_PLLVDD) Supply Rail** | | | | | |
| GB2B-64, GB2C-64 | 0.1 µF X7R | 0402 | 1 | 1 | Under GPU |
| | 22 µF X5R | 0805 | 1 | 0 | Near GPU |
| | Bead Type | | | | |
| | L=30 Ω (ESR=0.05 Ω) | 0402 | 1 | 0 | Near GPU |
| **SP_PLLVDD and VID_PLLVDD Combined Supply Rails** | | | | | |
| GB2B-64, GB2C-64 | 0.1 µF X7R | 0402 | 2 | 2 | Under GPU |
| | 10 µF X5R | 0603 | 1 | 0 | Near GPU |
| | 47 µF X5R | 0805 | 1 | 0 | Near GPU |
| | Bead Type | | | | |
| | L=300 Ω (ESR=0.2 Ω) | 0603 | 1 | 0 | Near GPU |
| **NC (N17: GPCPLL_AVDD) Supply Rail** | | | | | |
| GB2C-64 | 0.1 µF X7R | 0402 | N/A | 1 | Under GPU |
| | 4.7 µF X6S | 0603 | N/A | 1 | Near GPU |
| | 22 µF X6S | 0805 | N/A | 1 | Near GPU |
| | Bead Type | | | | |
| | L=30 Ω (ESR=0.010 Ω) | 0603 | N/A | 1 | Near GPU |



Compal Electronics, Inc.

Title: N16X LVDS 3/9

Size: Custom | Document Number: Raticate KL M/B LA-H441P | Rev: 0.1

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## NV 16x DG-07158-V05

Table 3-9. DDR3 GPU-Side FBVDD and FBVDDQ Combined Decoupling

| GPU Package Type | Capacitor Type | Footprint | Population | Location |
|---|---|---|---|---|
| GB2B-64/GB2-64 DDR3 | 0.1µF X7R | 0402 | 2 | Under GPU |
| | 1 µF X7R | 0603 | 2 | Under GPU |
| | 4.7 µF X6S | 0603 | 2 | Under GPU |
| | 10 µF X5R | 0805 | 1 | Near GPU |
| | 22 µF X5R | 0805 | 1 | Near GPU |

## DA-08329-001_V02

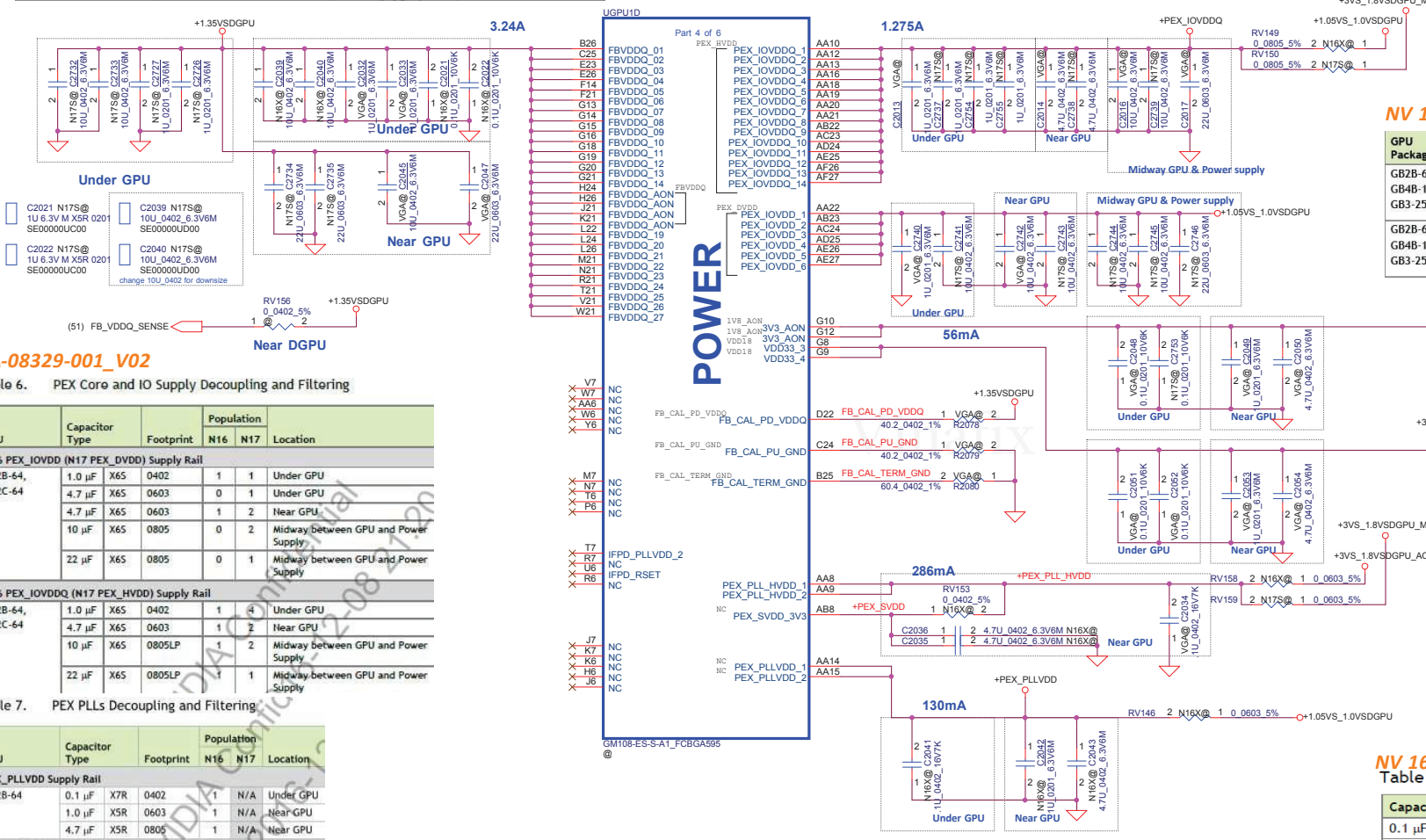
Table 4. Frame Buffer Core and IO Decoupling and Filtering

| GPU | Capacitor Type | Footprint | Population N16 | Population N17 | Location |
|---|---|---|---|---|---|
| FBVDD/Q Supply Rail for GDDR5 | | | | | |
| GB2B-64, GB2C-64 | 0.1 µF X7R | 0402 | 2 | 0 | Under GPU |
| | 1 µF X7R | 0603 | 2 | 8 | Under GPU |
| | 4.7 µF X6S | 0603 | 2 | 0 | Under GPU |
| | 10 µF X6S | 0603 | 0 | 2 | Under GPU |
| | 10 µF X6S | 0603 | 1 | 1 | Near GPU |
| | 22 µF X6S | 0603W | 1 | 3 | Near GPU |

## NV 16x DG-07158-V05

Table 3-16. PEX_IOVDD/Q Power Rail Combined

| GPU Package Type | Capacitor Type | | Footprint | Population | Location |
|---|---|---|---|---|---|
| GB2B-64/ GB2-64 | 1.0 µF | X6S | 0402 | 1 | Under GPU |
| | 4.7 µF | X6S | 0603 | 1 | Near GPU |
| | 10 µF | X5R | 0805 | 1 | Midway between GPU and Power Supply |
| | 22 µF | X5R | 0805 | 1 | Midway between GPU and Power Supply |




## NV 16x DG-07158-V05

Table 7-13. Default GPU Drive Calibration for Frame Buffer Interface

| Memory/PKG | FBVDDQ | FBCAL_PU_GND | FBCAL_PD_VDDQ | FBCAL_TERM_GND |
|---|---|---|---|---|
| GDDR5 / BGA-170 | 1.35 V or 1.50 V | 40.2 Ω | 40.2 Ω | 60.4 Ω |

## NV 16x DG-07158-V05

| GPU Package | Rail | Capacitor Type | | Footprint | | Population | Location |
|---|---|---|---|---|---|---|---|
| GB2B-64 GB4B-128 GB3-256 | 3V3_MAIN | 0.1µF | X6S | 0402 | 2 | 2 | Under GPU |
| | | 1 µF | X5R | 0603 | 1 | 1 | Near GPU |
| | | 4.7 µF | X5R | 0603 | 1 | 1 | Near GPU |
| GB2B-64 GB4B-128 GB3-256 | 3V3_AON | 0.1µF | X6S | 0402 | 1 | 1 | Under GPU |
| | | 1 µF | X5R | 0603 | 1 | 1 | Near GPU |
| | | 4.7 µF | X5R | 0603 | 1 | 1 | Near GPU |

## DA-08329-001_V02

Table 6. PEX Core and IO Supply Decoupling and Filtering

| GPU | Capacitor Type | Footprint | Population N16 | Population N17 | Location |
|---|---|---|---|---|---|
| N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail | | | | | |
| GB2B-64, GB2C-64 | 1.0 µF X6S | 0402 | 1 | 1 | Under GPU |
| | 4.7 µF X6S | 0603 | 0 | 1 | Under GPU |
| | 4.7 µF X6S | 0603 | 1 | 2 | Near GPU |
| | 10 µF X6S | 0805 | 0 | 2 | Midway between GPU and Power Supply |
| | 22 µF X6S | 0805 | 0 | 1 | Midway between GPU and Power Supply |
| N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail | | | | | |
| GB2B-64, GB2C-64 | 1.0 µF X6S | 0402 | 1 | 4 | Under GPU |
| | 4.7 µF X6S | 0603 | 1 | 2 | Near GPU |
| | 10 µF X6S | 0805LP | 1 | 2 | Midway between GPU and Power Supply |
| | 22 µF X6S | 0805LP | 1 | 1 | Midway between GPU and Power Supply |

Table 7. PEX PLLs Decoupling and Filtering

| GPU | Capacitor Type | Footprint | Population N16 | Population N17 | Location |
|---|---|---|---|---|---|
| PEX_PLLVDD Supply Rail | | | | | |
| GB2B-64 | 0.1 µF X7R | 0402 | 1 | N/A | Under GPU |
| | 1.0 µF X5R | 0603 | 1 | N/A | Near GPU |
| | 4.7 µF X5R | 0805 | 1 | N/A | Near GPU |
| PEX_SVDD_3V3 Supply Rail | | | | | |
| GB2B-64 | 4.7 µF X5R | 0603 | 2 | N/A | Near GPU |
| PEX_PLL_HVDD Supply Rail | | | | | |
| GB2B-64, GB2C-64 | 0.1 µF X7R | 0402 | 1 | 1 | Near GPU |

## DA-08329-001_V01

Table 9. VDD AON and VDD_MAIN Decoupling

| GPU | Capacitor Type | Footprint | Population N16 | Population N17 | Location |
|---|---|---|---|---|---|
| N16 3V3_MAIN (N17 VDD18) Supply Rail | | | | | |
| GB2B-64, GB2C-64 | 0.1 µF X7R | 0402 | 2 | 2 | Under GPU |
| | 1.0 µF X6S | 0603 | 1 | 1 | Near GPU |
| | 4.7 µF X6S | 0603 | 1 | 1 | Near GPU |
| N16 3V3_AON (N17 1V8_AON) Supply Rail | | | | | |
| GB2B-64, GB2C-64 | 0.1 µF X7R | 0402 | 1 | 1 | Under GPU |
| | 1.0 µF X6S | 0603 | 1 | 1 | Near GPU |
| | 4.7 µF X6S | 0603 | 1 | 1 | Near GPU |

## NV 16x DG-07158-V05

Table 3-18. PEX_SVDD_3V3 and PEX_PLL_HVDD Decoupling

| Capacitor Type | | Footprint | Population | Location |
|---|---|---|---|---|
| 0.1 µF | X7R | 0402 | 1 | Near GPU |
| 4.7 µF | X5R | 0603 | 2 | Near GPU |

## NV 16x DG-07158-V05

Table 3-17. PEX_PLLVDD Decoupling

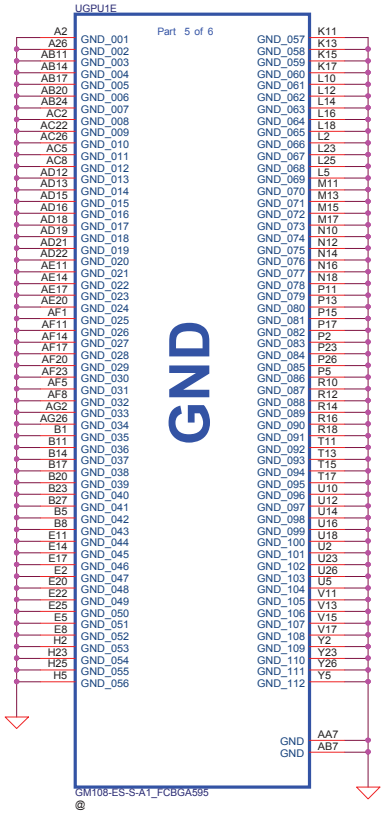
| Capacitor Type | | Footprint | Population | Location |
|---|---|---|---|---|
| 0.1 µF | X7R | 0402 | 1 | Under GPU |
| 1.0 µF | X5R | 0603 | 1 | Near GPU |
| 4.7 µF | X5R | 0805 | 1 | Near GPU |

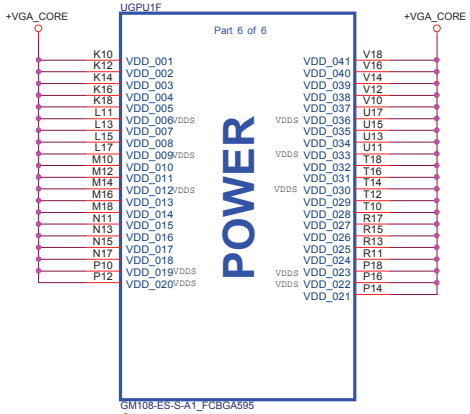


| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: N16X POWER & GND 4/9 | | | |
| Size: Custom | Document Number: Raticate KL M/B LA-H441P | | Rev: 0.1 |
| Date: Friday, November 30, 2018 | Sheet 24 of 57 | | |




## NV 16x DG-07158-V05

Table 3-6. NVVDD Decoupling Footprint and Population

| GPU Package Type | Capacitor Type | | Footprint | | Population | Location | Comments |
|---|---|---|---|---|---|---|---|
| GB2B-64 / GB2-64 | 4.7 µF | X6S | 0603 | 10 | 10 | Under GPU | |
| | 1 µF | X6S | 0402 | 4 | 4 | Under GPU | |
| | 47 µF | X5R | 0805 | 1 | 1 | Near GPU | |
| | 22 µF | X5R | 0805 | 1 | 1 | Near GPU | |
| | 4.7 µF | X5R | 0805 | 5 | 5 | Near GPU | |
| | 330 µF | POS | 7343 | 1 | 1 | Near GPU | ESR ≤ 6 mΩ |

## DA-08329-001_V01

Table 3. NVVDD and NVVDDS Decoupling and Filtering

| GPU | Capacitor Type | | Footprint | Population N16 | Population N17 | Location |
|---|---|---|---|---|---|---|
| **NVVDD Supply Net** | | | | | | |
| GB2B-64, GB2C-64 | 4.7 µF | X6S | 0603 | 10 | 8 | Under GPU |
| | 1 µF | X6S | 0402 | 4 | 3 | Under GPU |
| | 47 µF | X5R | 0805 | 1 | - | Near GPU |
| | 10 µF | X7R | 0805 | - | 4 | Near GPU |
| | 22 µF | X5R | 0805 | 1 | 3 | Near GPU |
| | 4.7 µF | X5R | 0805 | 1 | 4 | Near GPU |
| | 330 µF | POS | 7343 | 1 | 1 | Near GPU |
| **NVVDDS Supply Net** | | | | | | |
| GB2C-64 Only | 4.7 µF | X6S | 0603 | N/A | 4 | Under GPU |
| | 1 µF | X6S | 0402 | N/A | 2 | Under GPU |
| | 10 µF | X6S | 0805 | N/A | 7 | Near GPU |
| | 22 µF | X6S | 0805LP | N/A | 1 | Near GPU |
| | 330 µF | POS | 7343 | N/A | 1 | Near GPU |

## DA-07750-000-V02

Table 6. EDP-Continuous [3]

| Products | VRAM Type | GPU Core – (A) | GPU FBIO 1.5V [4] (A) | GPU FBIO 1.35V [4] (A) | FB Total [1,5] 1.5V [4] (A) | FB Total [1,5] 1.35V [4] (A) | 1.05V Total [2] 1.05V [4] (A) | 3.3V Total 3.3V [4] (A) |
|---|---|---|---|---|---|---|---|---|
| N16S-GMR | GDDR5 | 19.0 | – | 2.0 | – | 4.2 | 0.80 | 0.06 |
| | DDR3/L | 21.0 | 1.4 | 1.4 | 2.4 | 2.3 | 0.80 | 0.06 |
| N16S-GTR | GDDR5 @ 2.0 GHz | 26.5 | – | 2.0 | – | 4.2 | 0.80 | 0.06 |
| | GDDR5 @ 2.5 GHz | 26.5 | – | 2.0 | – | 4.7 | 0.80 | 0.06 |
| | DDR3/L | 26.0 | 1.4 | 1.4 | 2.4 | 2.3 | 0.80 | 0.06 |

Table 7. EDP-Peak [3]

| Products | VRAM Type | GPU Core – (A) | GPU FBIO 1.5V [4] (A) | GPU FBIO 1.35V [4] (A) | FB Total [1,5] 1.5V [4] (A) | FB Total [1,5] 1.35V [4] (A) | 1.05V Total [2] 1.05V [4] (A) |
|---|---|---|---|---|---|---|---|
| N16S-GMR | GDDR5 | 34.0 | – | 2.9 | – | 6.8 | 2.1 |
| | DDR3/L | 39.5 | 2.6 | 2.3 | 4.1 | 3.9 | 2.1 |
| N16S-GTR | GDDR5 @ 2.0 GHz | 53.0 | – | 2.9 | – | 6.8 | 2.1 |
| | GDDR5 @ 2.5 GHz | 53.0 | – | 3.1 | – | 7.2 | 2.1 |
| | DDR3/L | 51.0 | 2.6 | 2.3 | 4.1 | 3.9 | 2.1 |

## DA-07751-000-V02

Table 5. EDP-Continuous [3]

| Product | VRAM Type | GPU Core – (A) | GPU FBIO 1.5V [4] (A) | GPU FBIO 1.35V [4] (A) | FB Total [1,5] 1.5V [4] (A) | FB Total [1,5] 1.35V [4] (A) | 1.05V Total [2] 1.05V [4] (A) | 3.3V Total 3.3V [4] (A) |
|---|---|---|---|---|---|---|---|---|
| N16V-GMR1 | GDDR5 @ 2.0 GHz | 18.5 | – | 2.0 | – | 4.2 | 0.8 | 0.06 |
| | GDDR5 @ 2.5 GHz | 18.5 | – | 2.0 | – | 4.7 | 0.8 | 0.06 |
| | DDR3/L | 19.0 | 1.4 | 1.4 | 2.4 | 2.3 | 0.8 | 0.06 |

Table 6. EDP-Peak [3]

| Products | VRAM Type | GPU Core – (A) | GPU FBIO 1.5V [4] (A) | GPU FBIO 1.35V [4] (A) | FB Total [1,5] 1.5V [4] (A) | FB Total [1,5] 1.35V [4] (A) | 1.05V Total [2] 1.05V [4] (A) |
|---|---|---|---|---|---|---|---|
| N16V-GMR1 | GDDR5 @ 2.0 GHz | 30.0 | – | 2.9 | – | 6.8 | 2.1 |
| | GDDR5 @ 2.5 GHz | 31.0 | – | 3.1 | 7.2 | | 2.1 |
| | DDR3/L | 28.5 | 2.6 | 2.3 | 4.1 | 3.9 | 2.1 |

## SP-08318-001_V03

Table 7. Output EDP-Continuous

| Product | NVVDD – (A) | GPU FBIO 1.35V[4] (A) | FB Total[5] 1.35V[4] (A) | 1.0V Total[1] 1.0V[4] (A) | 1.8V Total[2] 1.8V[4] (A) |
|---|---|---|---|---|---|
| N17S-G1 | 30.0 | 2.0 | 3.4 | 0.1 | 0.3 |

Table 8. Output EDP-Peak

| Product | NVVDD – (A) | GPU FBIO 1.35V[3] (A) | FB TOTAL[4] 1.35V[3] (A) | 1.0V Total[1] 1.0V[3] (A) |
|---|---|---|---|---|
| N17S-G1 | 60.1 | 3.2 | 6.6 | 0.2 |

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



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|---|---|---|
| Custom | Raticate KL M/B LA-H441P | 0.1 |

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# VRAM GDDR5 chips

## X76 for N16X 2G VRAM

- X7604@ — Samsung_256Mx32x2 — X76739BOL04
- X7605@ — Hynix_256Mx32x2 — X76739BOL05
- X7606@ — Micron_256Mx32x2 — X76739BOL06
- X76793BOL03@ — Micron_MT51J256M32HF-70:B
- X76793BOL04@ — Hynix_H5GC8H24AJR-R0C — New

## X76 for N17S 2G VRAM

- X7607@ — Samsung_256Mx32x2 — X76739BOL07
- X7608@ — Hynix_256Mx32x2 — X76739BOL08
- X7609@ — Micron_256Mx32x2 — X76739BOL09
- X76793BOL01@ — Micron_MT51J256M32HF-70:B
- X76793BOL02@ — Hynix_H5GC8H24AJR-R0C — New

## GDDR5 Mode H Mapping

| | DATA Bus | |
|---|---|---|
| Address | 0..31 | 32..63 |
| CMD0 | CS# | |
| CMD1 | A3_BA3 | |
| CMD2 | A2_BA0 | |
| CMD3 | A4_BA2 | |
| CMD4 | A5_BA1 | |
| CMD5 | WE# | |
| CMD6 | A7_A8 | |
| CMD7 | A6_A11 | |
| CMD8 | ABI# | |
| CMD9 | A12_RFU | |
| CMD10 | A0_A10 | |
| CMD11 | A1_A9 | |
| CMD12 | RAS# | |
| CMD13 | RST# | |
| CMD14 | CKE# | |
| CMD15 | CAS# | |
| CMD16 | | CS# |
| CMD17 | | A3_BA3 |
| CMD18 | | A2_BA0 |
| CMD19 | | A4_BA2 |
| CMD20 | | A5_BA1 |
| CMD21 | | WE# |
| CMD22 | | A7_A8 |
| CMD23 | | A6_A11 |
| CMD24 | | ABI# |
| CMD25 | | A12_RFU |
| CMD26 | | A0_A10 |
| CMD27 | | A1_A9 |
| CMD28 | | RAS# |
| CMD29 | | RST# |
| CMD30 | | CKE# |
| CMD31 | | CAS# |

# Channel 0 BOT SIDE

(22,27) MDA[63..0] — MDA[63..0]
(22,27) CMDA[31..0] — CMDA[31..0]

UV13 — MF=0

BYTE0 / BYTE1 / BYTE2 / BYTE3

+1.35VSDGPU

FBA_CLK0 / FBA_CLK0# — RV63 40.2_0402_1% VGA@ — RV95 40.2_0402_1% VGA@ — CV190 0.01U_0402_16V7K VGA@

RV136 549_0402_1% VGA@ — RV135 931_0402_1% VGA@ — RV56 1.33K_0402_1% VGA@ — CV195 820PF_0402_50V7K VGA@ — QV3 BSS138W-7-F_SOT323-3 VGA@ — (21) VRAM_VREF_CTL — FBA_VREFC_L — +FBA_VREFC0 (27)

170-BALL SGRAM GDDR5 — H5GC4H24AJR-R0C_BGA170

DA8335 Cap Q'ty
22U x2
10U x 6
1U x 10
22U x 3 (unPOP)

N16X Cap Q'ty
10U x2
1U x 8
0.1U x 6

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



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Title: N16X Lower Rank0 6/9

Size: Custom | Document Number: Raticate KL M/B LA-H441P | Rev: 0.1

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# VRAM GDDR5 chips

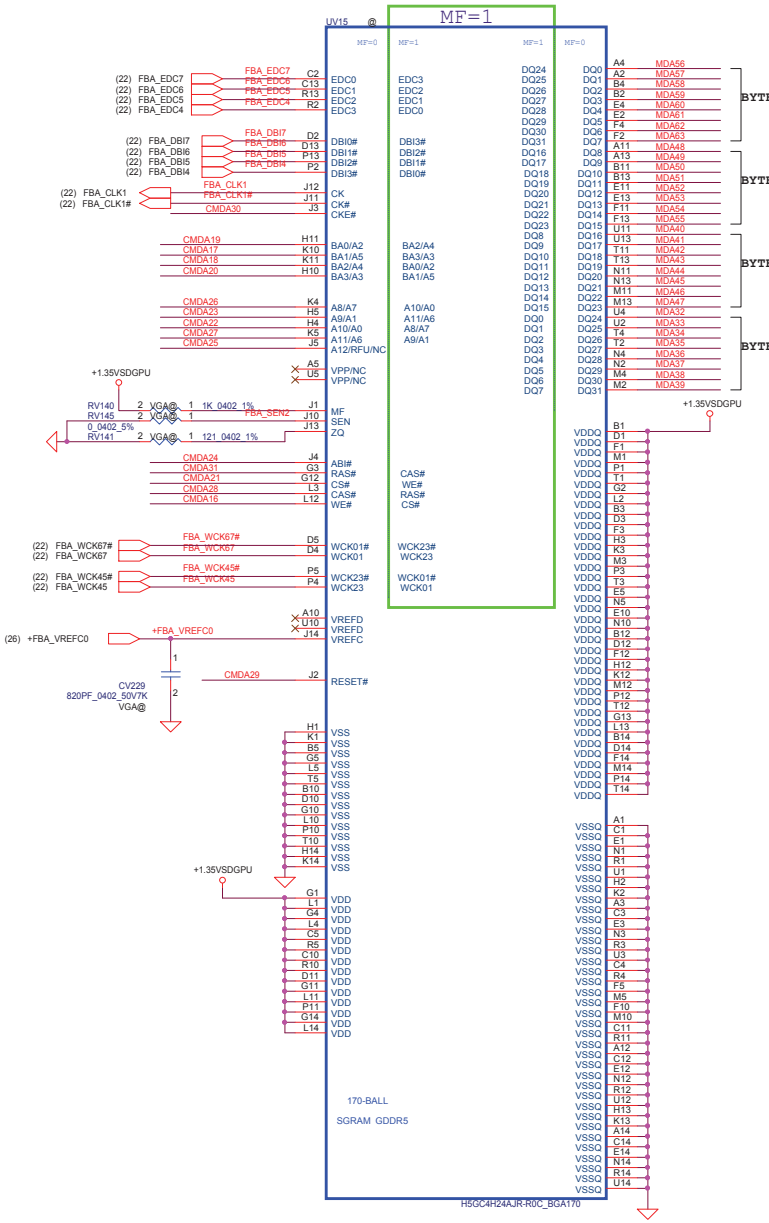
(22,26) MDA[63..0] → MDA[63..0]

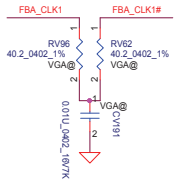
(22,26) CMDA[31..0] → CMDA[31..0]

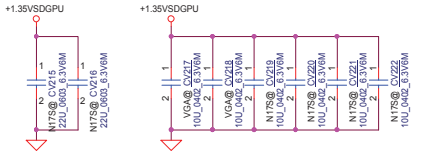
## GDDR5 Mode H Mapping

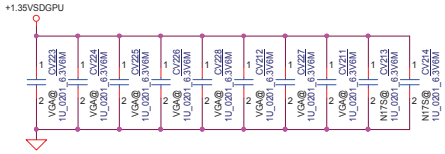
| | DATA Bus | |
|---|---|---|
| Address | 0..31 | 32..63 |
| CMD0 | CS# | |
| CMD1 | A3_BA3 | |
| CMD2 | A2_BA0 | |
| CMD3 | A4_BA2 | |
| CMD4 | A5_BA1 | |
| CMD5 | WE# | |
| CMD6 | A7_A8 | |
| CMD7 | A6_A11 | |
| CMD8 | ABI# | |
| CMD9 | A12_RFU | |
| CMD10 | A0_A10 | |
| CMD11 | A1_A9 | |
| CMD12 | RAS# | |
| CMD13 | RST# | |
| CMD14 | CKE# | |
| CMD15 | CAS# | |
| CMD16 | | CS# |
| CMD17 | | A3_BA3 |
| CMD18 | | A2_BA0 |
| CMD19 | | A4_BA2 |
| CMD20 | | A5_BA1 |
| CMD21 | | WE# |
| CMD22 | | A7_A8 |
| CMD23 | | A6_A11 |
| CMD24 | | ABI# |
| CMD25 | | A12_RFU |
| CMD26 | | A0_A10 |
| CMD27 | | A1_A9 |
| CMD28 | | RAS# |
| CMD29 | | RST# |
| CMD30 | | CKE# |
| CMD31 | | CAS# |

# Channel 1 BOT SIDE



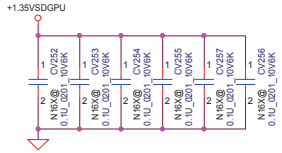




DA8335 Cap Q'ty
22U x2
10U x 6
1U x 10
22U x 3 (unPOP)

N16X Cap Q'ty
10U x2
1U x 8
0.1U x 6




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



Compal Electronics, Inc.

Title: N16X Lower Rank1 7/9

| Size | Document Number | Rev |
|---|---|---|
| Custom | Raticate KL M/B LA-H441P | 0.1 |

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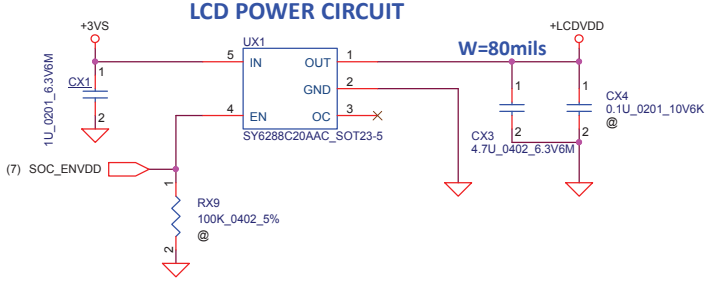
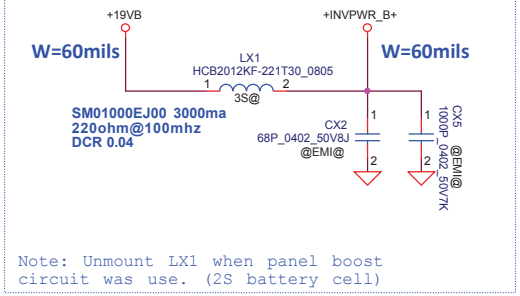
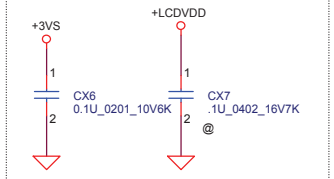
## LCD POWER CIRCUIT

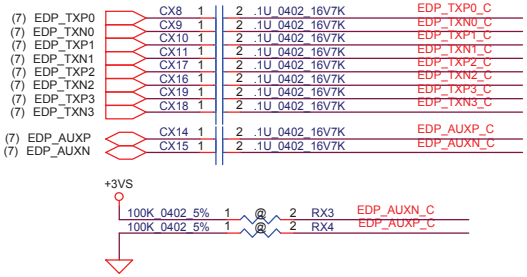


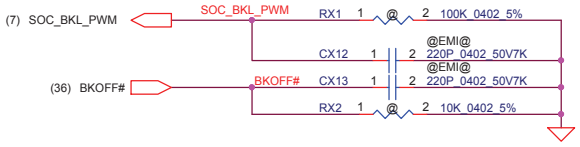



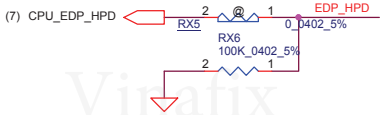

Note: Unmount LX1 when panel boost circuit was use. (2S battery cell)

## Place closed to JEDP1

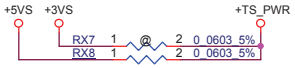


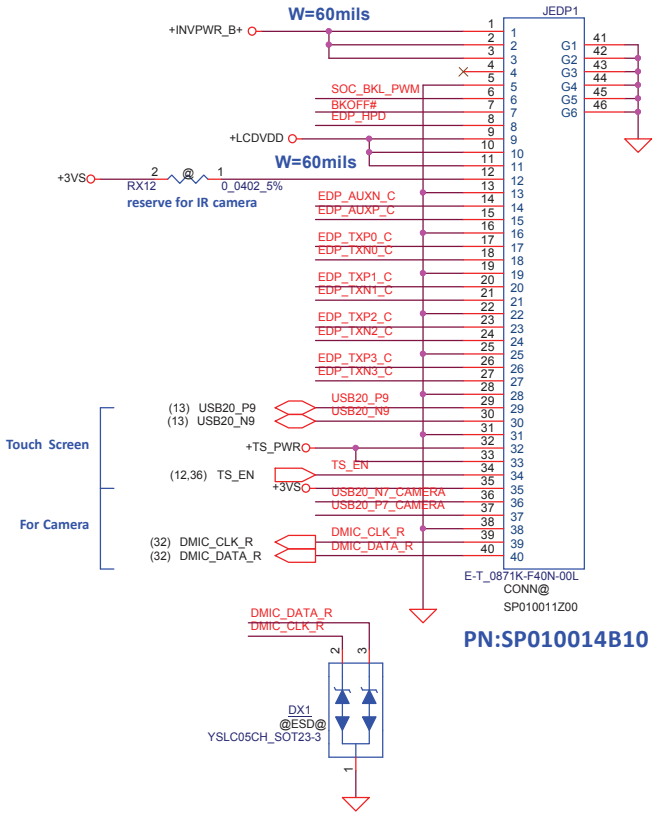




## Touch Screen




## Camera


## LED PANEL Conn.




PN:SP010014B10



| | | | |
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| | | | |
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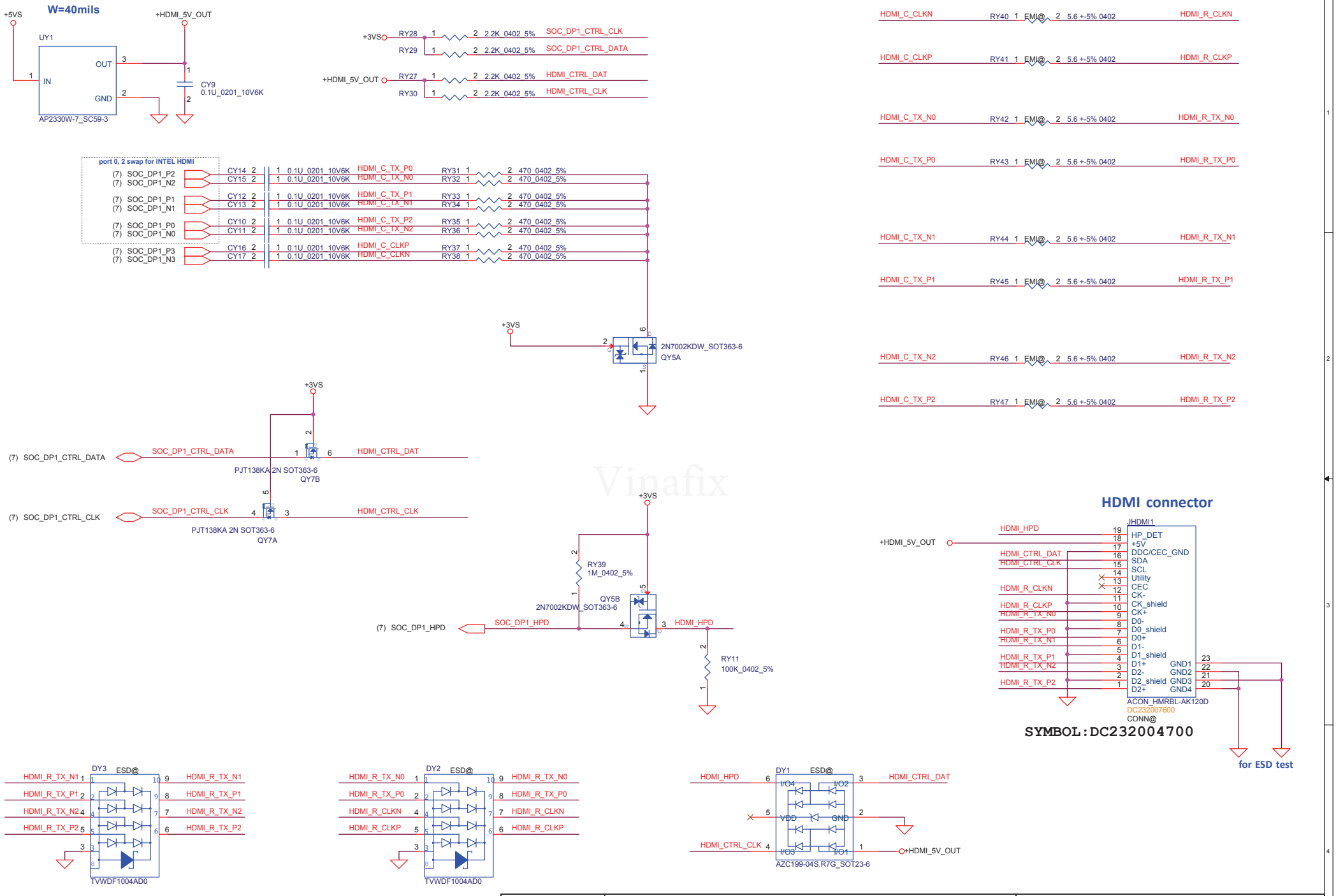




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



| | | |
|---|---|---|
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| Size: Custom | Document Number: Raticate KL M/B LA-H441P | Rev: 0.1 |
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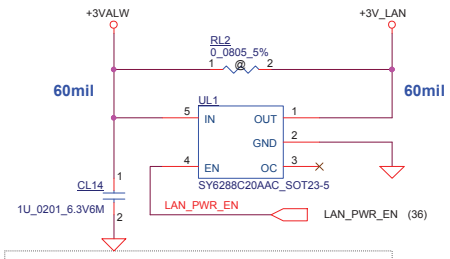
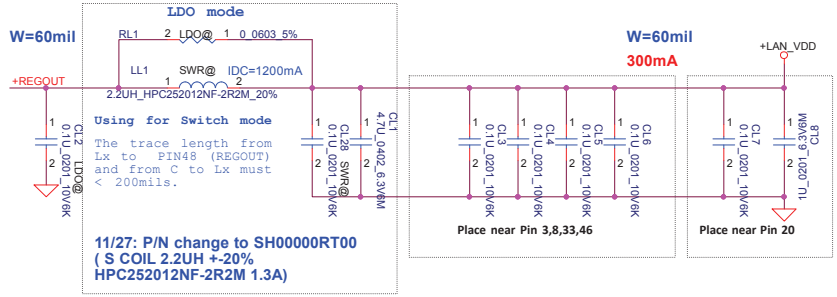
# LAN-RTL8411B




From EC

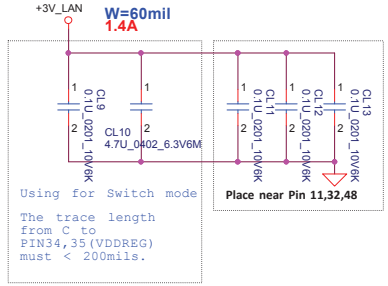
High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A

+3V_LAN Rising time must >0.5ms and <100ms



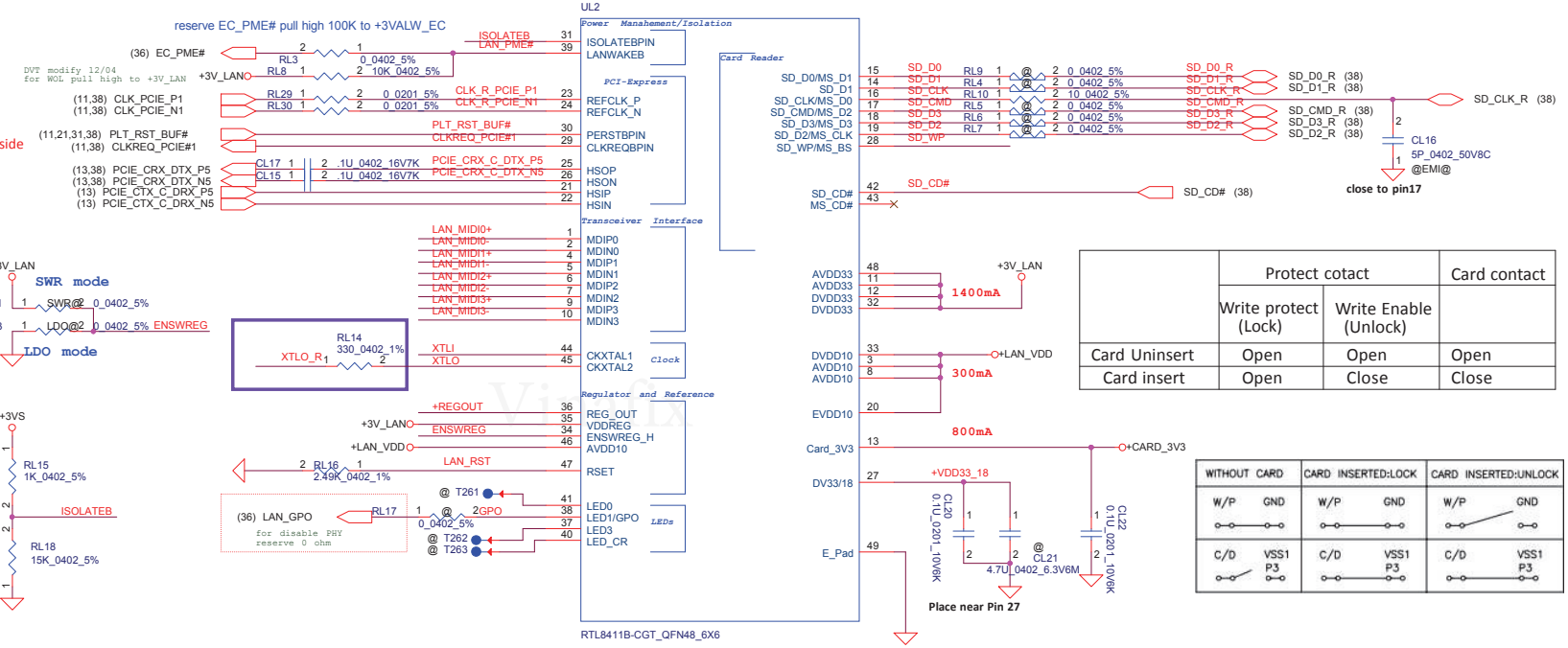






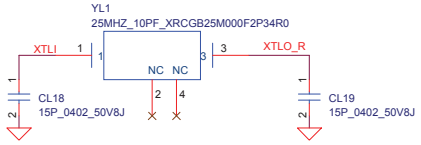

reserve EC_PME# pull high 100K to +3VALW_EC

PU at PCH side



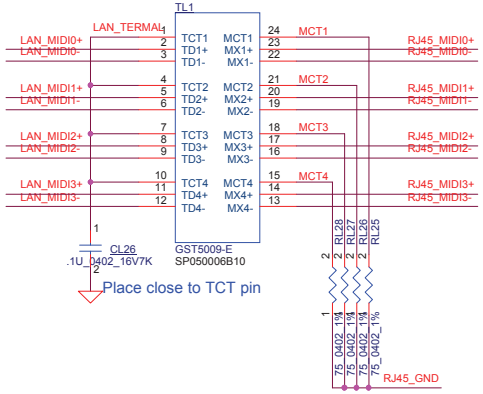

| | Protect cotact | | Card contact |
|---|---|---|---|
| | Write protect (Lock) | Write Enable (Unlock) | |
| Card Uninsert | Open | Open | Open |
| Card insert | Open | Close | Close |

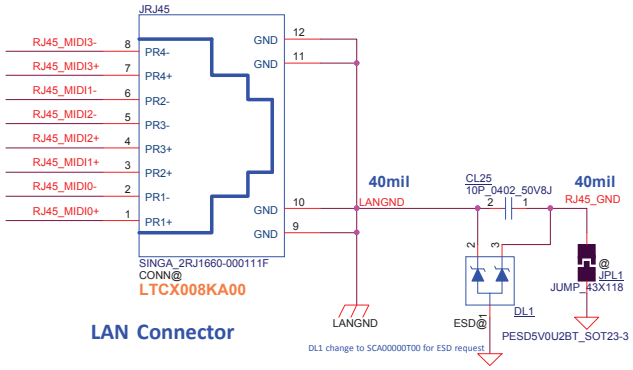


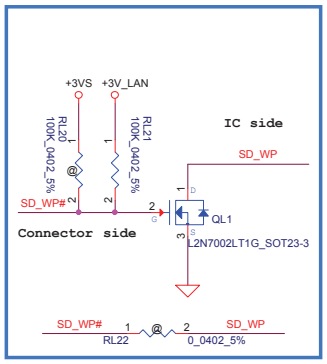




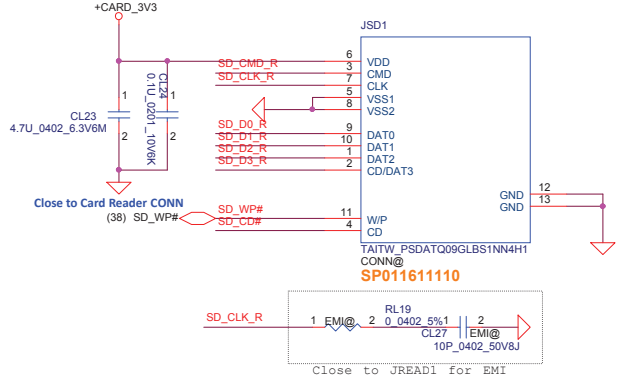



LAN Connector




Card Reader Connector

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Title: LAN RTL8411B-CG/Card Reader

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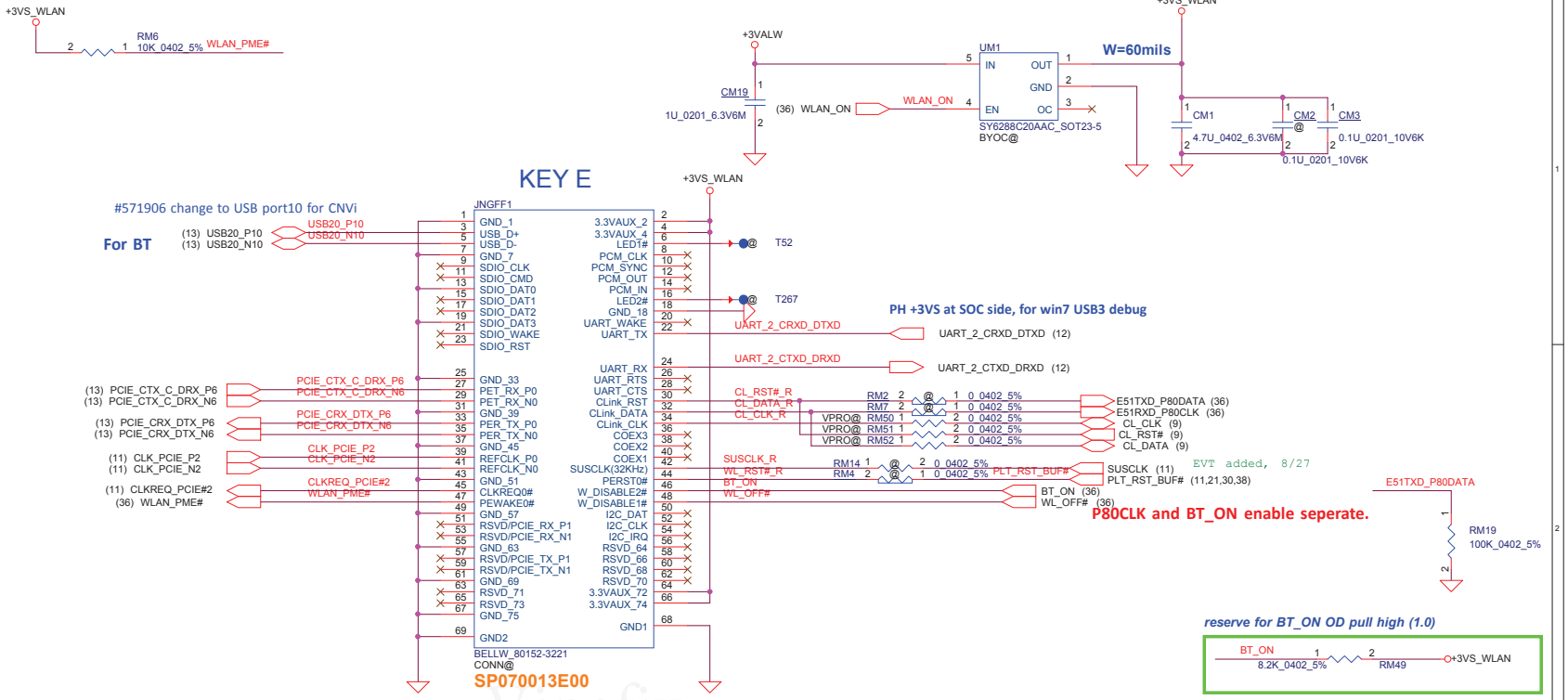
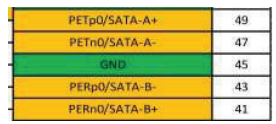
# Wireless LAN

## NGFF WL+BT (KEY E)


# mSATA/SSD



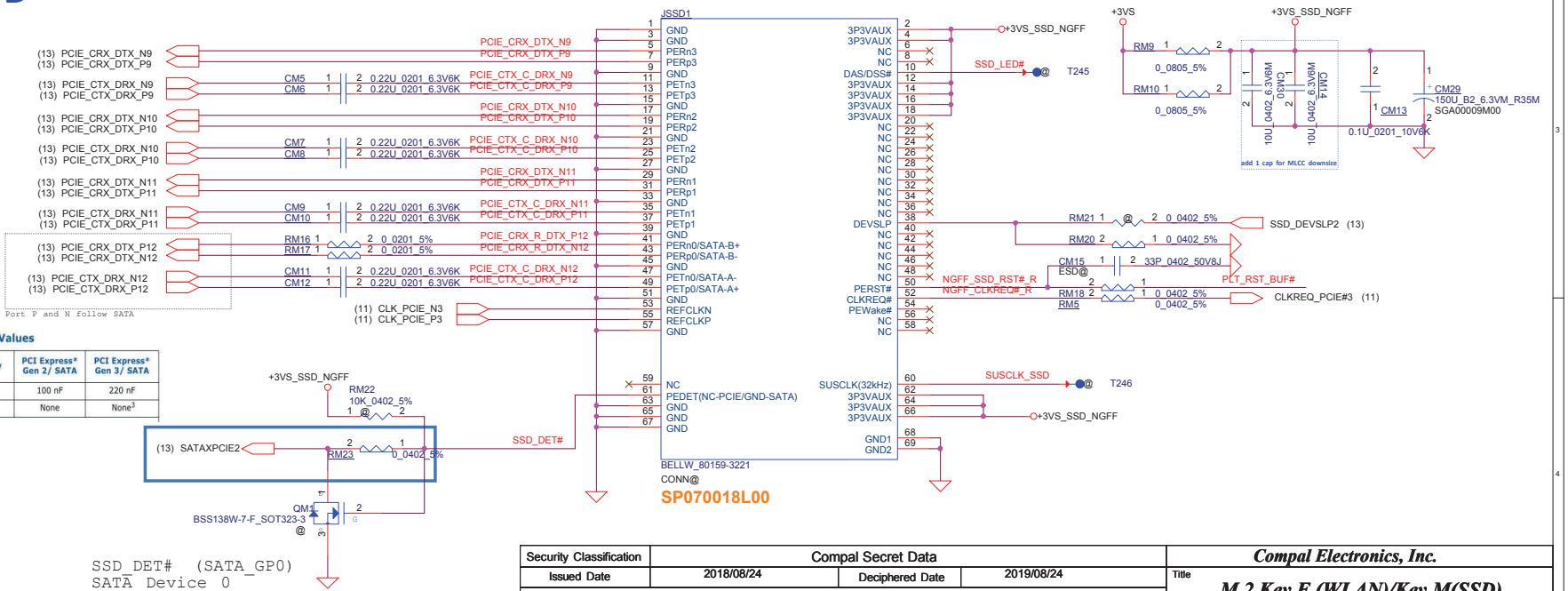




Table 35-7. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

| Condition | PCI Express* Gen 2 Only | PCI Express* Gen 3 Only | SATA Only | PCI Express* Gen 2/ SATA | PCI Express* Gen 3/ SATA |
|---|---|---|---|---|---|
| Processor Tx | 100 nF | 220 nF | 10 nF | 100 nF | 220 nF |
| Processor Rx | None | None | 10 nF[2] | None | None[3] |

SSD_DET# (SATA_GP0)
SATA Device 0
PCIE Device 1

| | | | |
|---|---|---|---|
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Compal Electronics, Inc.

Title: M.2 Key E (WLAN)/Key M(SSD)

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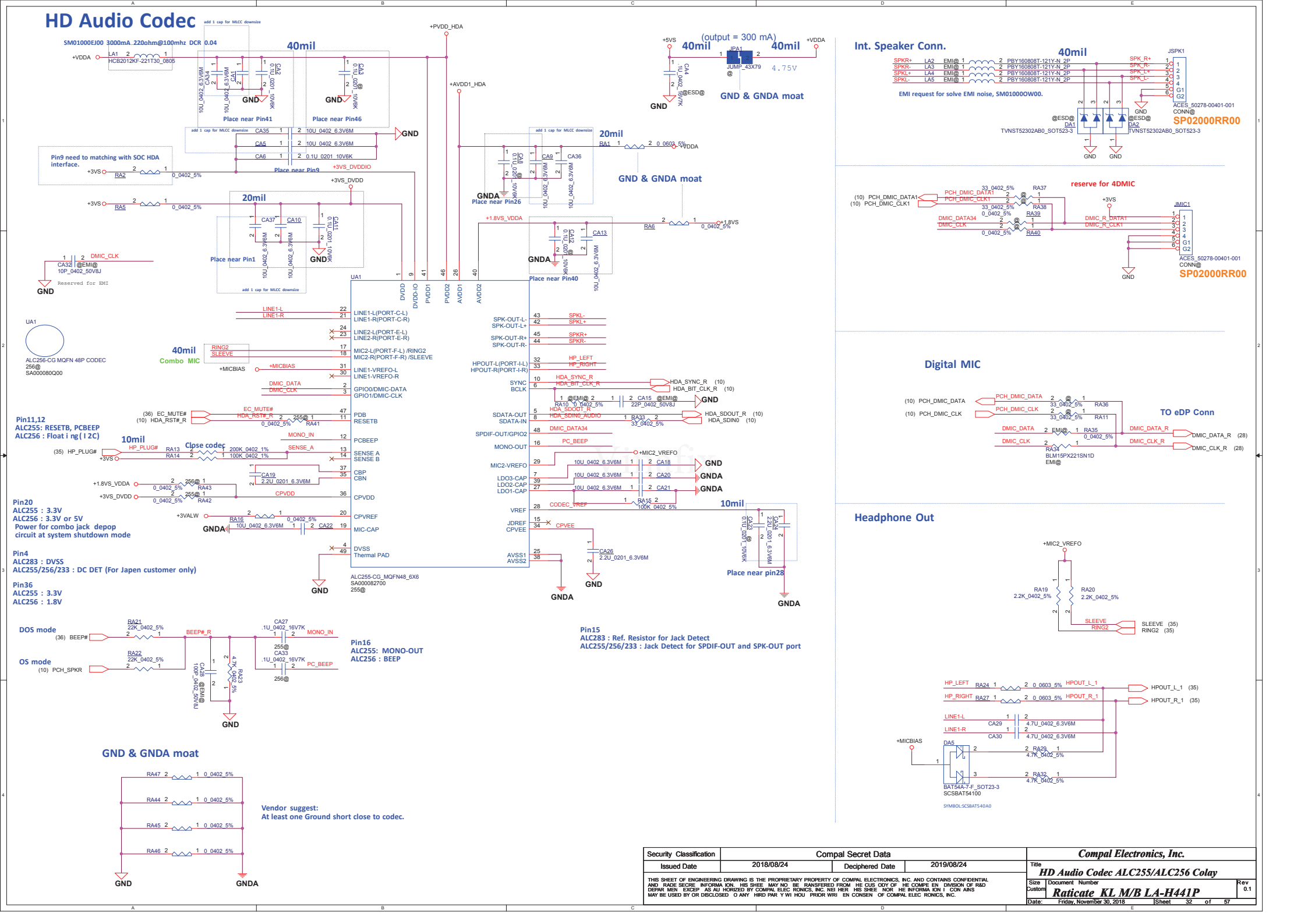
# HD Audio Codec




| | | | |
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| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | HD Audio Codec ALC255/ALC256 Colay |
| Size / Custom | Document Number: Raticate KL M/B LA-H441P |
| Rev | 0.1 |
| Date: | Friday, November 30, 2018 |
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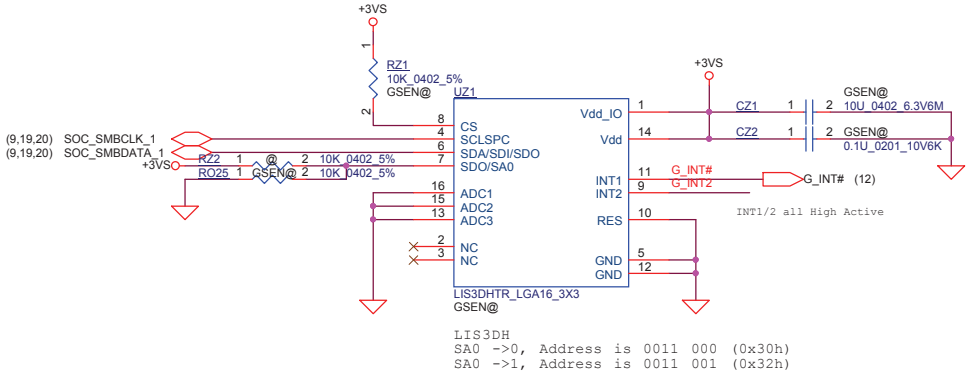
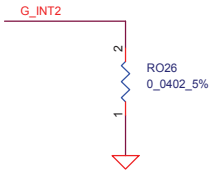
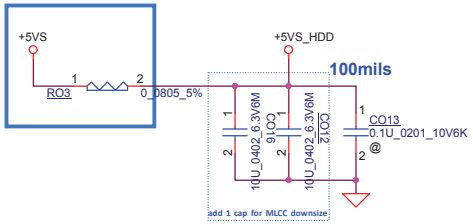
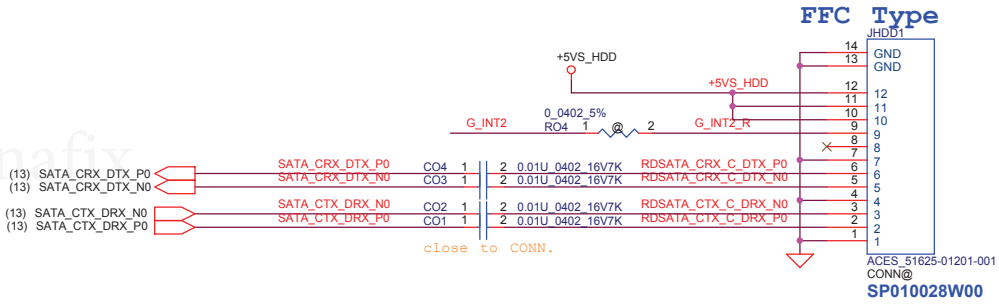
# G-Sensor reserved for BA serial




```
LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)
```






| | | | |
|---|---|---|---|
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Compal Electronics, Inc.

Title: HDD/ HDD Re-Driver

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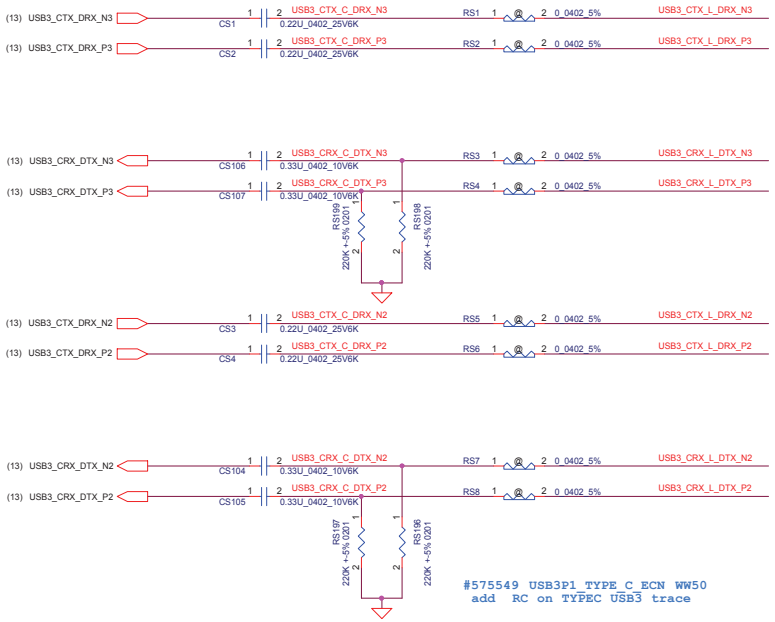
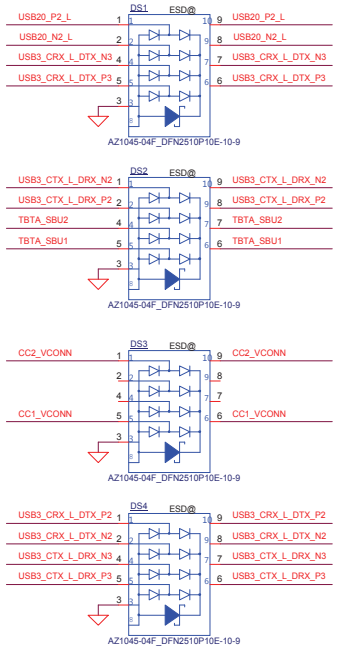
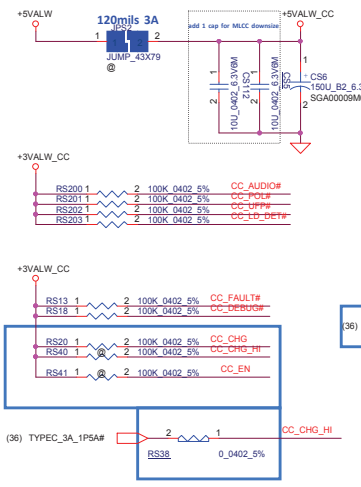
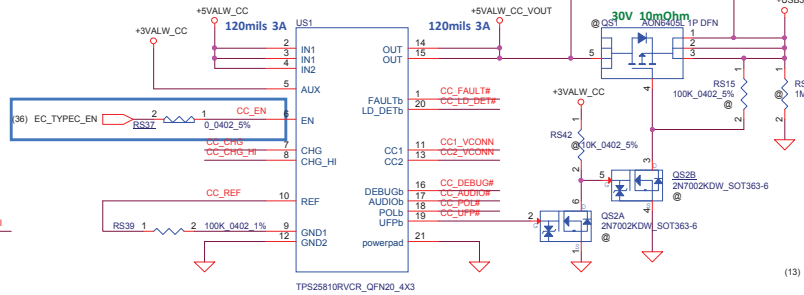
# TypeC USB3.0 Gen1

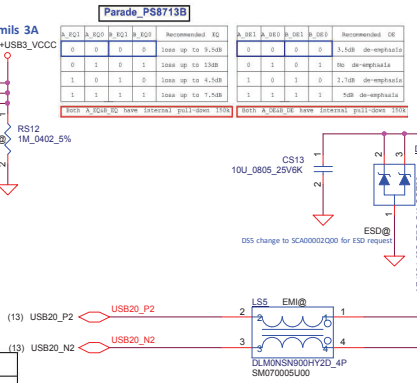



DS1~4 change to SC300001Y00 For ESD request



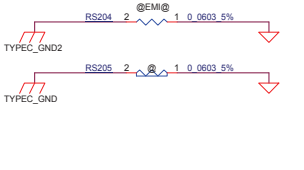













Vinafix

**Table 3. USB Type-C Current Advertisement**

| CHG | CHG_HI | CC CAPABILITY BROADCAST | CURRENT LIMIT (typ) | LOAD DETECT THRESHOLD (typ) |
|---|---|---|---|---|
| 0 | 0 | STD | 1.7 A | NA |
| 0 | 1 | STD | 1.7 A | NA |
| 1 | 0 | 1.5 A | 1.7 A | NA |
| 1 | 1 | 3 A | 3.4 A | 1.95 A |

| EC_TYPEC_EN | S0 | S3 | S5 |
|---|---|---|---|
| AC Mode (Adapter In) | On | On | Off |
| DC Mode (Battery Only) | On | On[1] | Off |

Note 1: Stop charge current when the battery capacity is below a specified percentage.

Note : 2017 BIOS SPEC define DC mode 30% stop charge

| | | | |
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Title: CC+USB TYPE C

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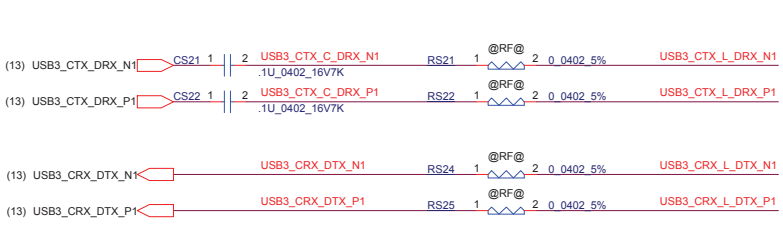
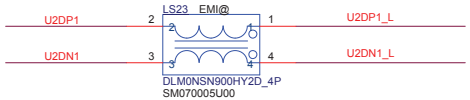
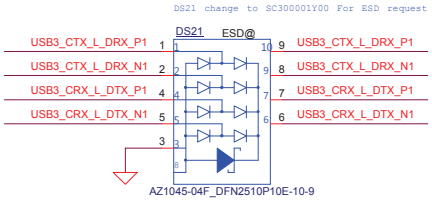
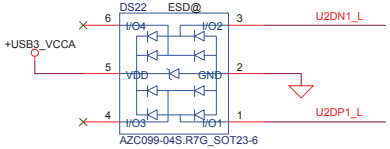
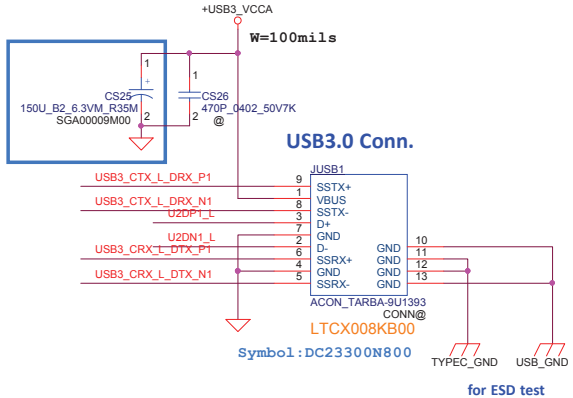
# USB3.0 (Port 1)

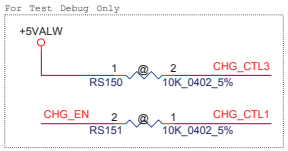


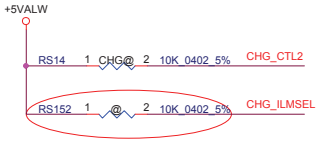



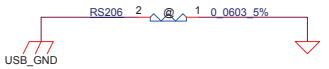



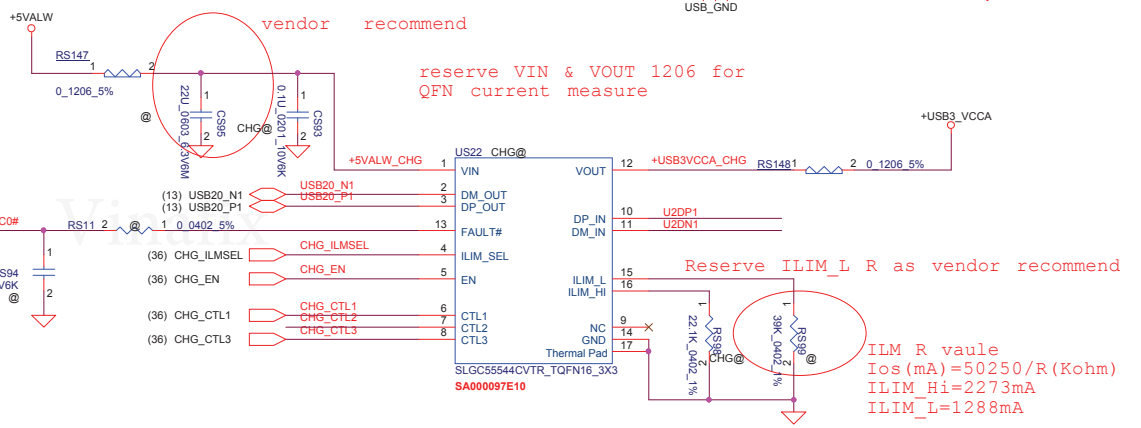




Rerserve PU, vendor suggest to EC control if future need support SDP2

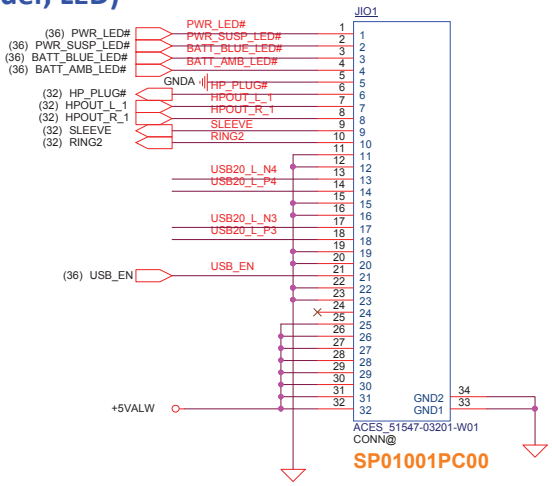


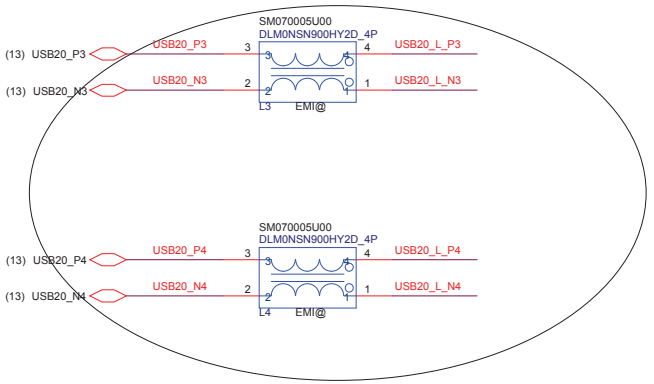




## USB Host Charger Truth Table

| CHG_EN | CTL1 | CTL2 | CTL3 | ILIM_SEL | MODE | Current Limit Setting | Note |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | SDP1-OFF | ILIM_H | Port power off |
| 1 | 0 | 1 | 0 | 1 | SDP1 | ILIM_H | Data Lines Connected |
| 1 | 0 | 1 | 1 | 1 | DCP Auto | ILIM_H | Data Lines Disconnected |
| 1 | 1 | 1 | 1 | 1 | CDP | ILIM_H | Data Lines Connected |

# IO/B (USBx2, Card reader, LED)




| | | | |
|---|---|---|---|
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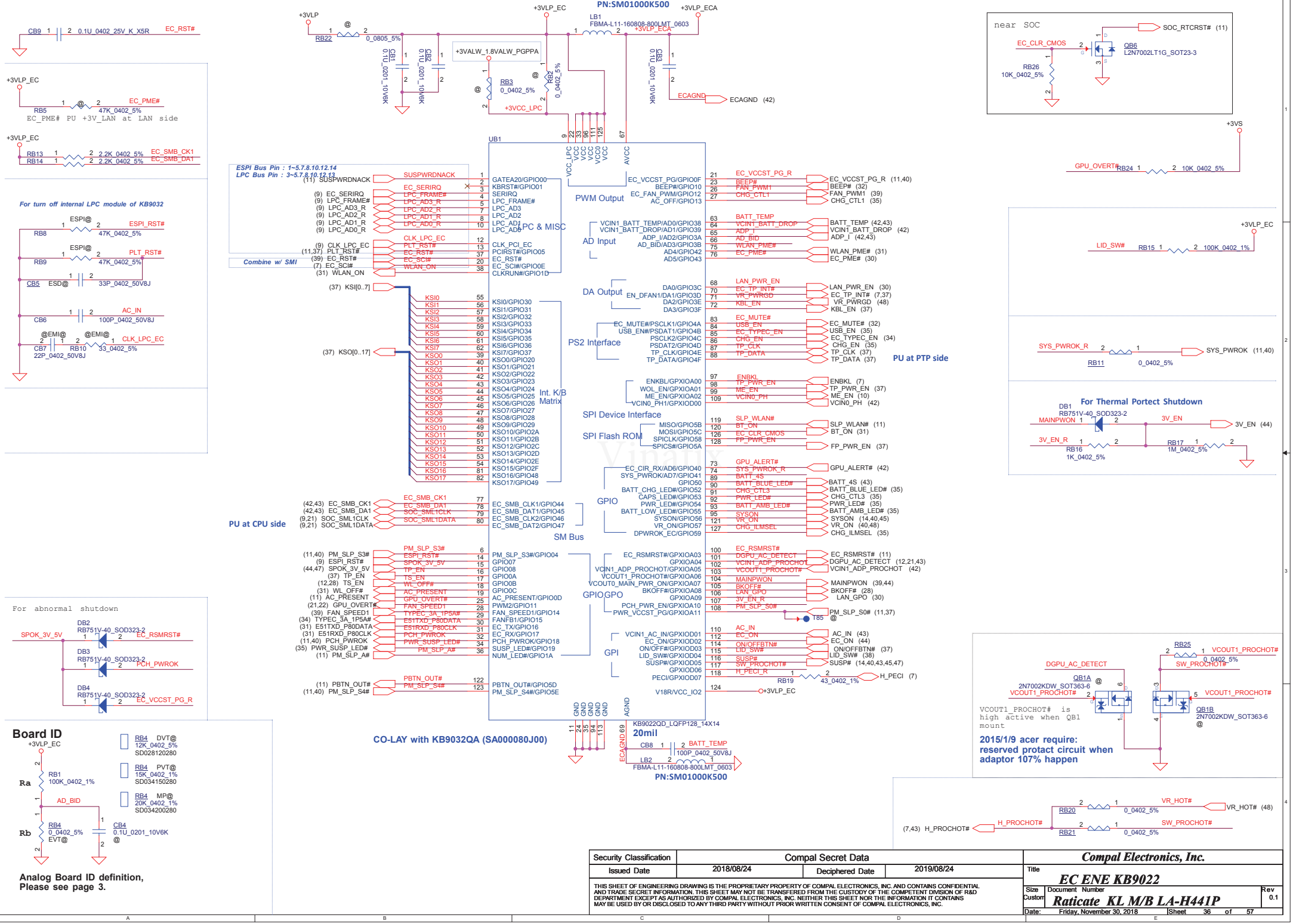
PN:SM01000K500
UB1
KB9022QD_LQFP128_14X14
20mil
CO-LAY with KB9032QA (SA000080J00)
ESPI Bus Pin : 1~5,7,8,10,12,14
LPC Bus Pin : 3~5,7,8,10,12,13
Combine w/ SMI
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPI
PC & MISC
Int. K/B Matrix
PU at CPU side
PU at PTP side
For turn off internal LPC module of KB9032
For abnormal shutdown
near SOC
For Thermal Portect Shutdown
VCOUT1_PROCHOT# is high active when QB1 mount
2015/1/9 acer require: reserved protact circuit when adaptor 107% happen
Board ID
Analog Board ID definition, Please see page 3.
Compal Secret Data
Issued Date 2018/08/24
Deciphered Date 2019/08/24
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EC ENE KB9022
Raticate KL M/B LA-H441P
Friday, November 30, 2018
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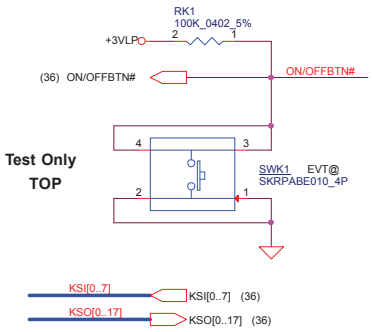
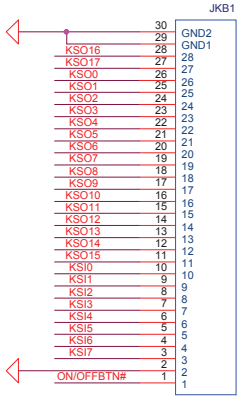
# KB Conn.

## ON/OFF BTN

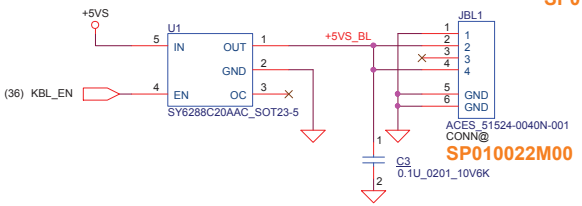



KSI[0..7] KSI[0..7] (36)
KSO[0..17] KSO[0..17] (36)

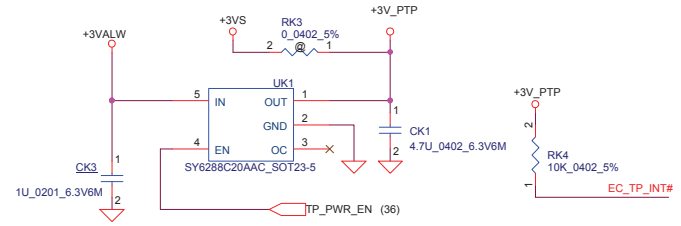



ACES_85201-2805
CONN@
SP01000GO00

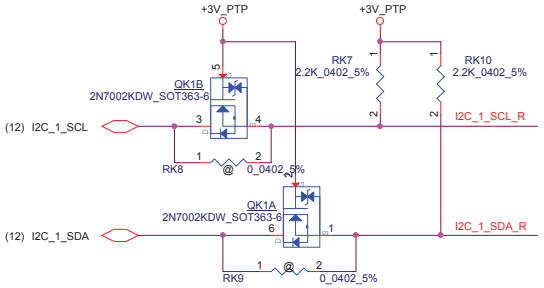
# KB BackLight

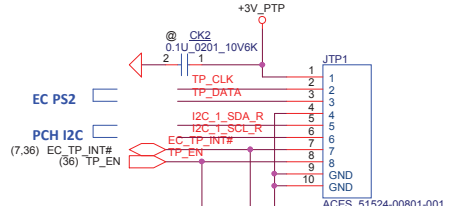


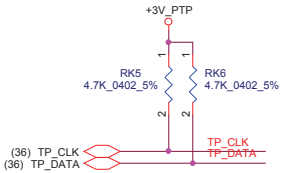

# TP/B Conn.



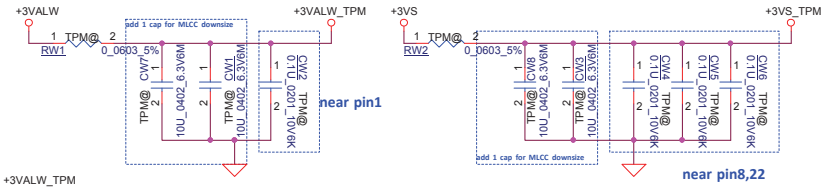

TP_PWR_EN follow SYSON behavior

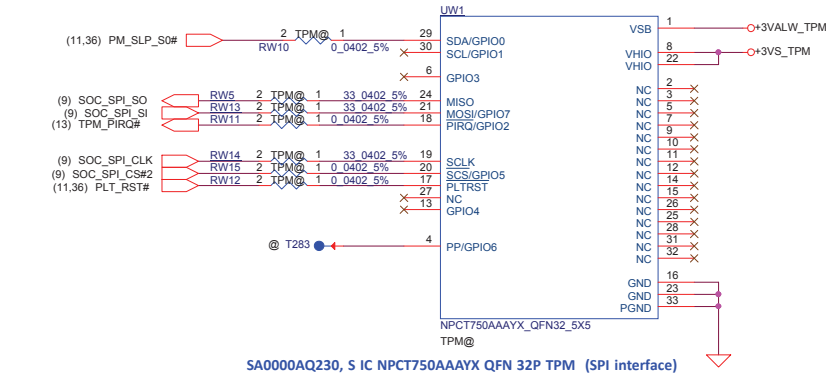



# TPM 2.0

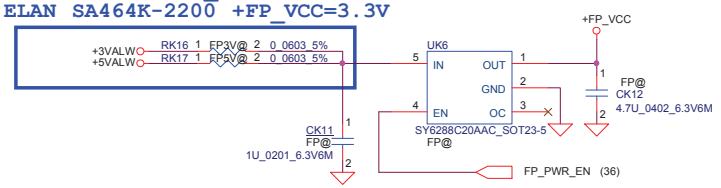


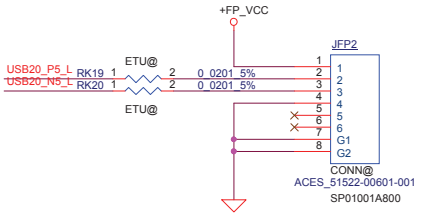



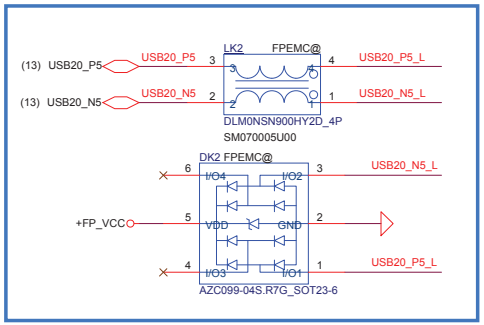

SA0000AQ230, S IC NPCT750AAAYX QFN 32P TPM (SPI interface)

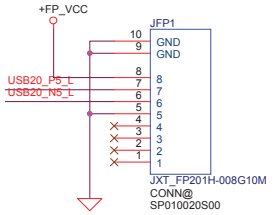
# Finger Print

Power Souce Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V




JFP2 JFP1

| PIN | ETU801 | SA464K-2200 |
|---|---|---|
| 1 | +FP_VCC(5V) | +FP_VCC(3V) |
| 2 | USBP | D+ |
| 3 | USBN | D- |
| 4 | GND | GND |
| 5 | NC | NC |
| 6 | NC | NC |
| 7 | | NC |
| 8 | | NC |



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|---|---|---|---|
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



Compal Electronics, Inc.

Title: KB & TP & TPM & FP

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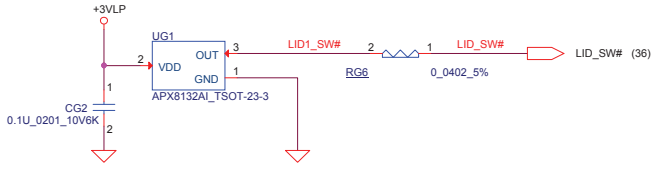
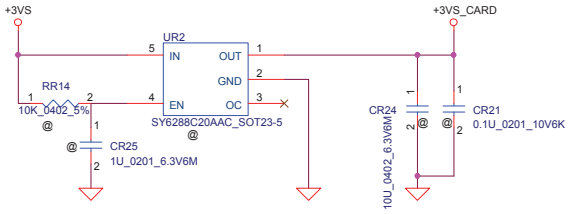
Date: Friday, November 30, 2018 | Sheet 37 of 57

# LID




SA00008K800, S IC APX8132AI-TRG SOT-23 3P HALL SENSOR

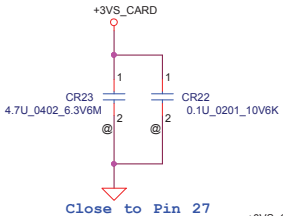
# reserve RTS5227 for VPRO



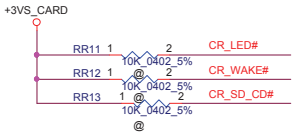


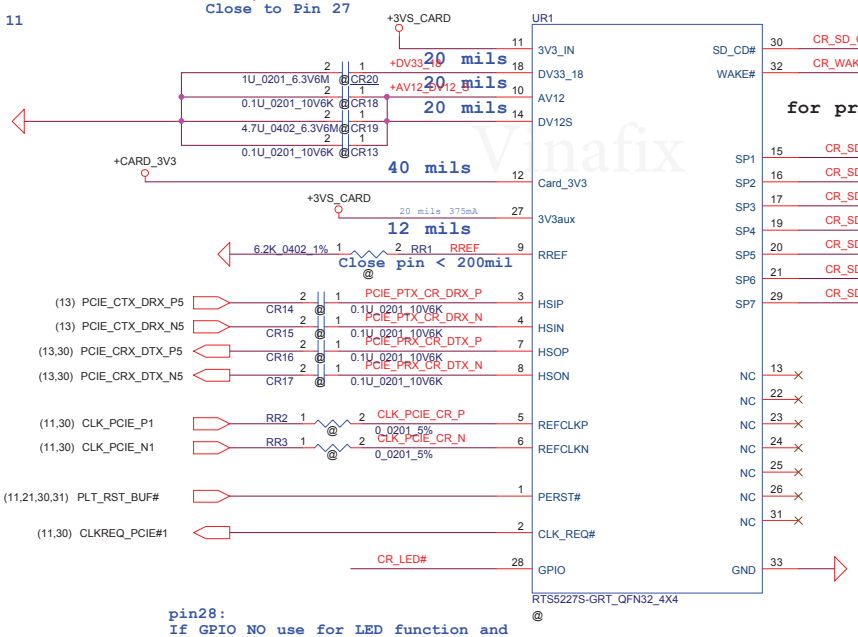


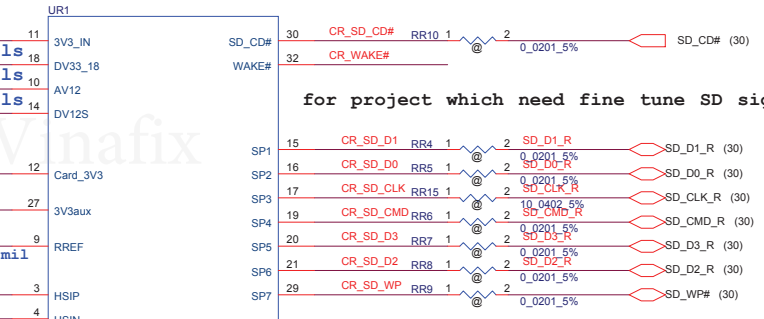
Close to Pin 11




Close to Pin 27




for project which need fine tune SD signal can change to R

pin28:
If GPIO NO use for LED function and
GPIO must pull high

| | | | |
|---|---|---|---|
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Title: LID/RTS5227

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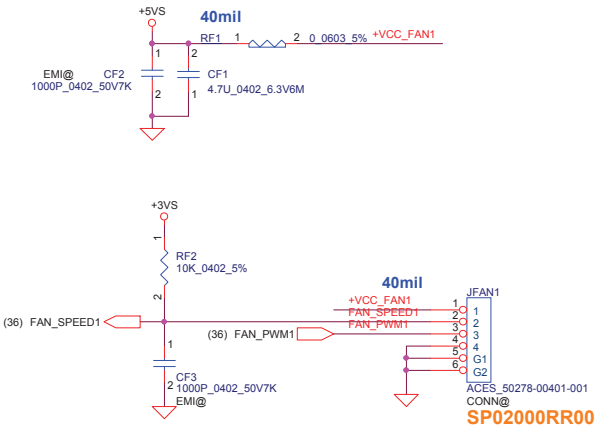
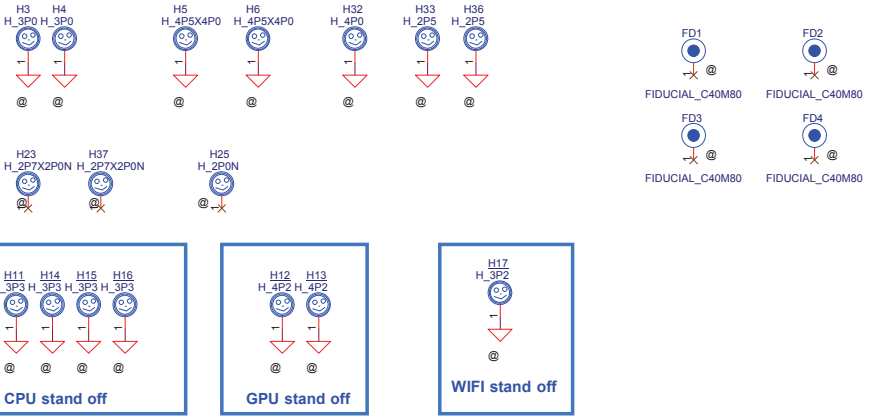
Date: Friday, November 30, 2018 | Sheet 38 of 57

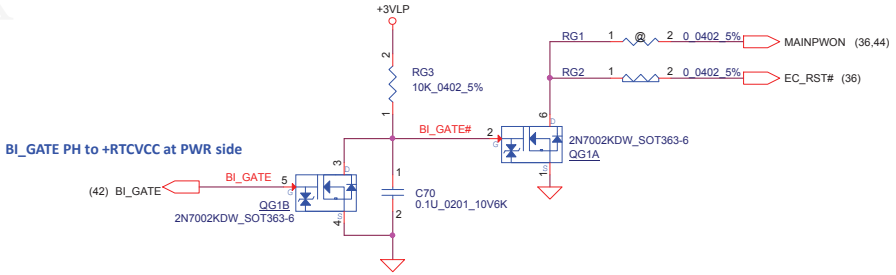
# FAN1 Conn



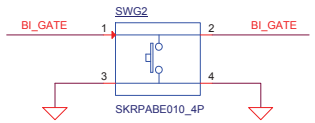

# Screw Hole




# Reset Circuit




## Reset Button






| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



Compal Electronics, Inc.

Title: FAN & Screw Hole & Reset

| Size | Document Number | Rev |
|---|---|---|
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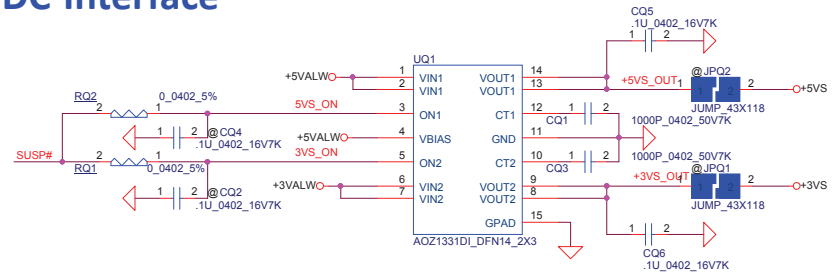
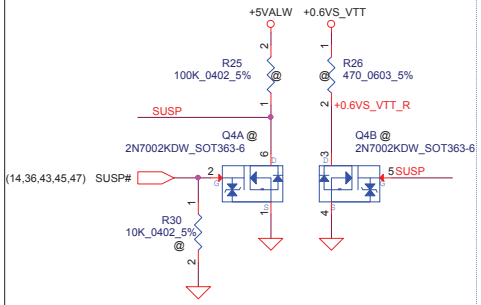
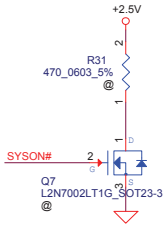
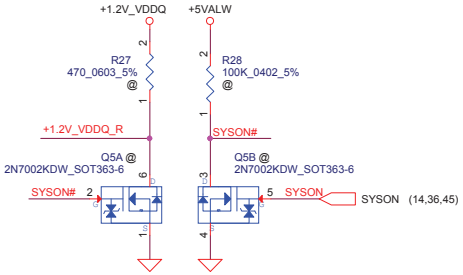
# DC Interface

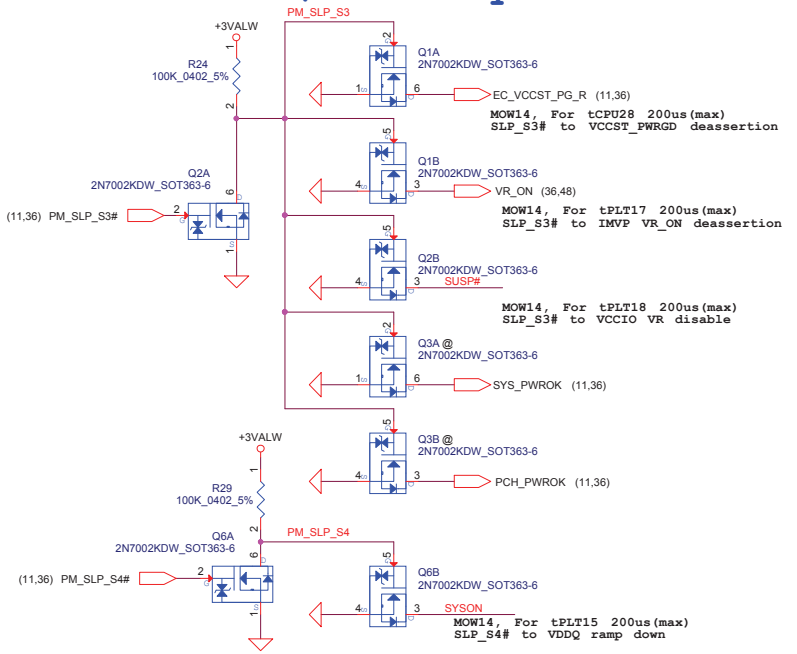


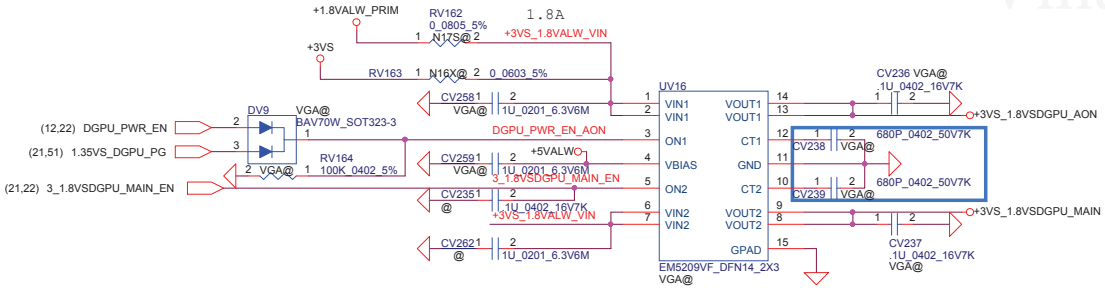



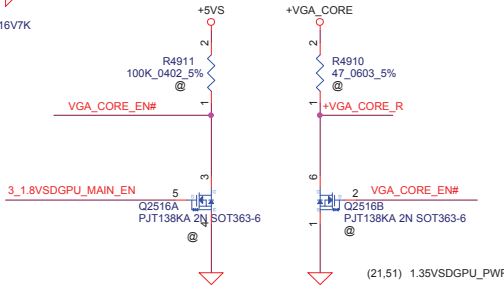



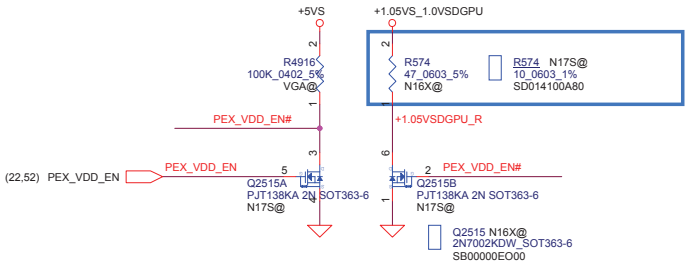



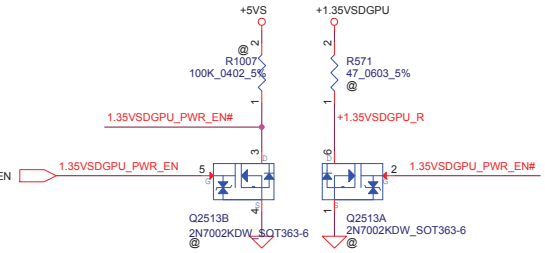

# For Power ON/Off Sequence




**+3VS to +3VSDGPU_AON for GPU**



| | | | |
|---|---|---|---|
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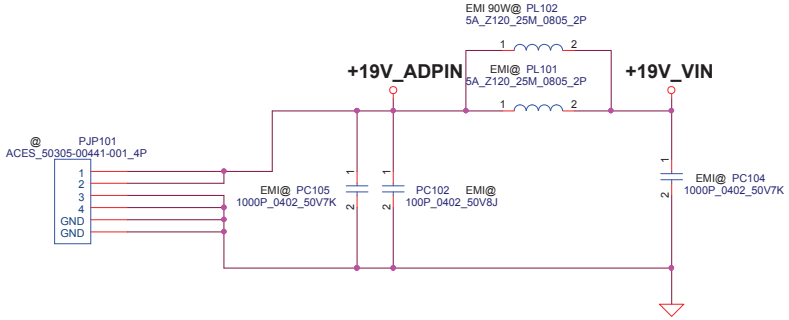
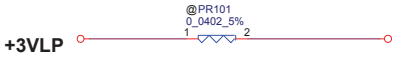
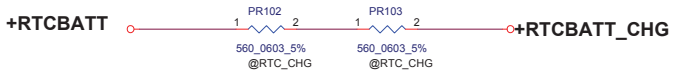
| Issued Date | 2018/08/24 | Deciphered Date | 2019/08/24 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: DC Interface | | | |
| Size: Custom | Document Number: Raticate KL M/B LA-H441P | | Rev: 0.1 |
| Date: Friday, November 30, 2018 | Sheet 40 of 57 | | |



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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/01/10 | Deciphered Date | 2018/11/04 |



**Compal Electronics, Inc.**

Title: **PWR DCIN / Pre-charge**

| Size | Document Number | Rev |
|---|---|---|
| Custom | EH5AW M/B LA-G521P | 0.1 |

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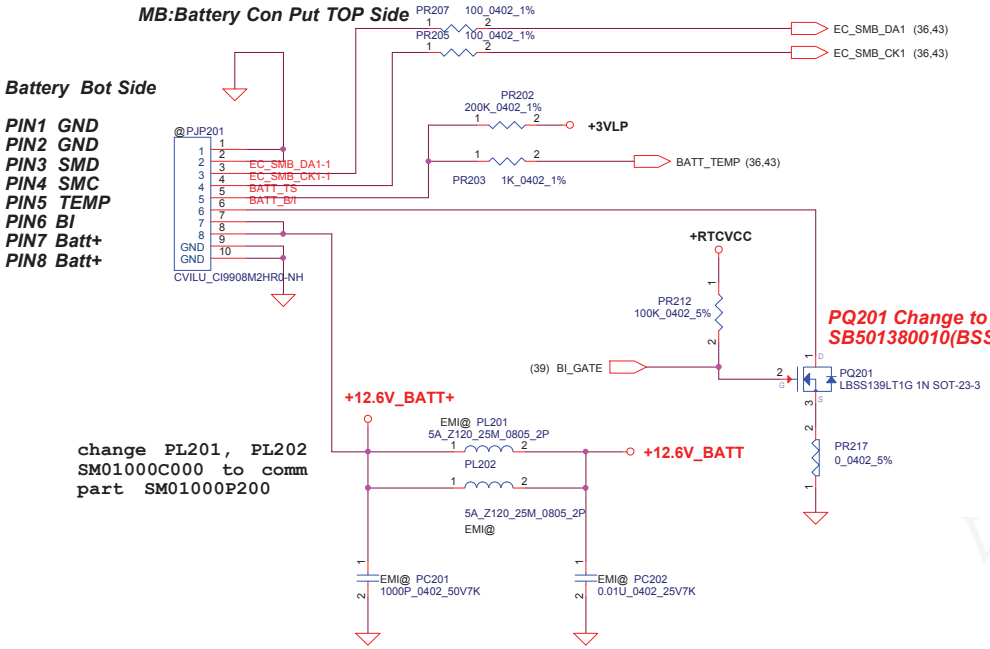
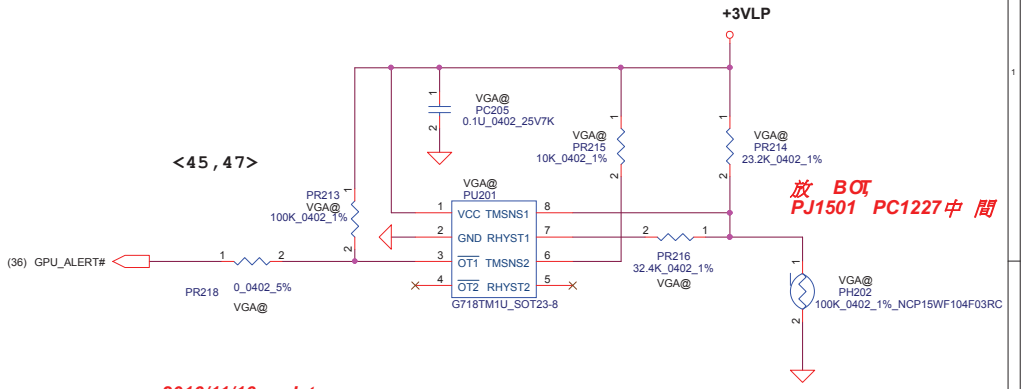
*2013/07/23*
*change PC5 and PC6 function field from 37.1 to 47.1*




*PQ201 Change to SB00000QO00, SB501380010(BSS138LT1G Del)*

change PL201, PL202 SM01000C000 to comm part SM01000P200




*放 BOT, PJ1501 PC1227中 間*

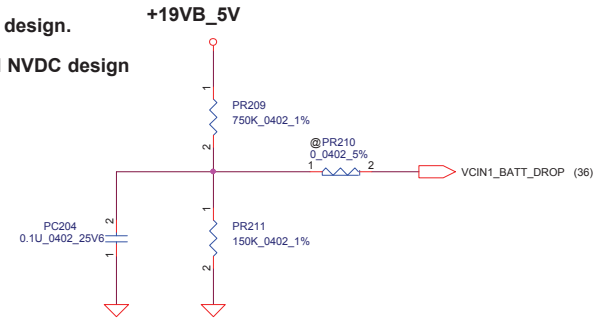
*2016/11/16 update*

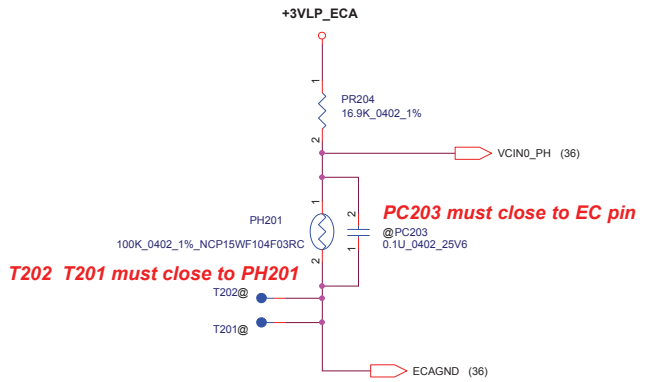
| For KB9022 sense 20mΩ | Active | Recovery |
|---|---|---|
| 45W PR206 10K ohm | 58.5W,0.61V | Active=recovery |
| 65W PR206 19.1K ohm | 84.5W,0.61V | Active=recovery |
| 90W PR206 30.1K ohm | 117W,0.61V | Active=recovery |
| PH1 | 2V | 1V |

*PH1 under CPU botten side :*
*CPU thermal protection at 89 +-3 degree C*
*Recovery at 56 +-3 degree C*

*2013/06/07*
*Add for ENE9022 Battery Voltage drop detection.*
*Connect to ENE9022 pin64 AD1.*

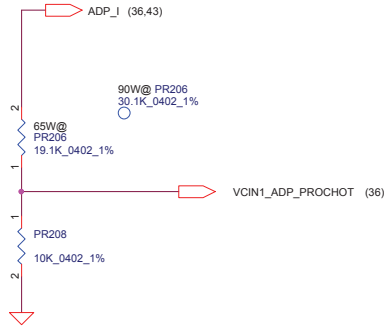
**VAL50/ZAL20 Battery is 3-cell NVDC design.**
**B+=9V**
**Change PR12=50k if Battery is 2-cell NVDC design**
**B+=6V**




*PC203 must close to EC pin*

*T202 T201 must close to PH201*




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/01/10 | Deciphered Date | 2018/11/04 |



Compal Electronics, Inc.
Title: PWR-BATTERY CONN/OTP
Size: Custom | Document Number: EH5AW M/B LA-G521P | Rev: 0.1
Date: Friday, November 30, 2018 | Sheet 42 of 57

Module model information

ISL95520_Hybrid_Boost_V2.mdd

Protection for reverse input

Vgs = 20V
Vds = 60V
Id = 250mA

PQ301 L2N7002WT1G_SC70-3
PR301 1M_0402_1%
PR302 3M_0402_5%

Need check the SOA for inrush

+19V_VIN
PQ310 AON6406 1N DFN5X6-8
+19V_P1
PQ311 AON7506_DFN33-8-5
+19V_P2
PR303 0.01_1206_1%
@PC322 1000P_0402_25V

max Power loss 0.22W for 90W;0.12W for 65W system;0.05W for 45W
CSR rating: 1W
VCSIP-VCSIN spec < 81mV

+19VB
@EMI@ PL302 FBMA-L11-201209-800LMA50T
Isat: 10A
DCR: 14mohm
@PJP1 JUMP_43X118
+19VB_CHG
PC302 10U_0603_25V6M
PC303 10U_0603_25V6M
PC305 @EMI@ 0.1U_0402_25V6
PC304 @EMI@ 2200P_0402_25V7K
PC324 @EMI@ 0.1U_0402_25V6

Co-lay jump and ISN choke.

CSIP_CHG_R
CSIN_CHG_R
PR304 0_0402_5%
PR305 2_0402_5%
PC306 0.1U_0402_25V6

PR306 499K_0402_1%
PR307 4.02K_0402_1%
PR308 4.02K_0402_1%

L->H
2. 4 vin min w/o 2M =17.41

H->L
2. 2 vin min w 2M =17.77

PR309 100_0402_1%
+12.6V_BATT
PQ312 AON7506_DFN33-8-5
@PC308 0.1U_0402_25V7K

CMSRC_CHG
ASGATE_CHG
PR310 66.5K_0402_1%
PC301 2200P_0402_50V7K

support Turbo boost : 2200P
no support Turbo boost : 0.1u

0x3CH <BIT9> PSYS current gain
Rs1 = 1 mΩ nd Rs2 = 5mΩ or Rs1 = 10mΩ and Rs2 = 10mΩ
BIT = 1.14 A/W
BIT1 = .285 A/W
Rs1 = 2 mΩ nd Rs2 = 1 mΩ or Rs1 = 2 mΩ nd Rs2 = 2mΩ
BIT = 2.28 A/W
BIT1 = .57 A/W

Ipsys = KPSYS x ( VAD P x IAD P + VBA T x IBA T )
R_Psys = 1.2V / Ipsys
KPSYS = 1.14uA/W
adapter wattage = 45W
Battery wattage = 40Wh
Ipsys = 1.14 x (45+40) = 96.9uA
R_Psys = 1.2V / 96.9uA = 12.3K-ohm.

adapter wattage = 65W
Battery wattage = 40Wh
Ipsys = 1.14 x (65+40) = 119.7uA
R_Psys = 1.2V / 96.9uA = 10K-ohm.

**Design Notes**
For 45W/65W /90W system, 2S/3S/4S battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W
#Register Setting
1. 0X3DH bit10 set 0 (default 1) to enable turbo boost function
2. Disable turbo when AC only
#Circuit Design
1. ACLIM and CCLIM are devider voltage control.
2. Use 7X7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=0.227W,L/S=1.2738W,Choke=0.297W)
Power density : 0.61 (23X16)
#Protect function
1. ACOVP : VCC voltage > 24V
2. SMBus timeout : 0X3DH bit15 set 0 (default 0) to enable 175s(default).
3. ACOC : OX3CH bit4 set1 release adapter limit function (default:Enable).
4. CHGOCP : based on charge current setting
5. BATOVP : 4.6V/Cell
6. BATLOWV : No.
7. TSHUT : 150C

PR311 100K_0402_1%
PR313 158K_0402_1%
(36) AC_IN
(36,42) EC_SMB_DA1
(36,42) EC_SMB_CK1
(7,36) H_PROCHOT#
(36,42) ADP_I
PR314 0_0402_5%
PR316 0_0402_5%
PR317 0_0402_5%
PR318 1K_0402_1%
PR321 1K_0402_1%
EC_SMB_DA1_R
EC_SMB_CK1_R
AMON_ISL95520
BMON_ISL95520
Close to EC.

PU301 ISL88739AHRZ-T_QFN32_4X4
ACIN ACOK SDA SCL PROCHOT# AMON BMON NC AGND
CSIP CSIN ASGATE CMSRC OPCN QPCP VBAT BGATE
BOOT UGATE PHASE LGATE VDDP VDD DCIN NTC
PROG COMP CCLIM FSET BATGONE CSON CSOP ACLIM

PR312 0_0603_5%
BST_CHG
UG_CHG
LX_CHG
LG_CHG
VDDP_CHG
VDD_CHG

PD301 RB751V-40_SOD323-2
PC309 0.47U_0402_25V6K
PQ305 AON7506_DFN33-8-5
PQ306 AON7506_DFN33-8-5
PL301 4.7UH_PCMB063T-4R7MS_8A_20%
17.4V_BATT_CHG
PR315 0.01_1206_1%
+12.6V_BATT
PC310 10U_0603_25V6M
PC311 10U_0603_25V6M
PC312 10U_0603_25V6M

Choke 4.7uH SH00000YC00 (Common Part)
(Size:6.6 x 7.3 x 3 mm)
(DCR:28m~33m)

Support max charge 3.5A
Power loss: 0.245W
CSR rating: 1W
VCSPP-VCSON spec < 81mV

PC313 1U_0201_6.3V6M
PC314 1U_0201_6.3V6M
PC315 1U_0201_6.3V6M
PR319 4.7_0402_5%
PR320 4.7_1206_5%
@EMI@ PC325 680P_0402_50V7K

PC316 0.1U_0402_25V6
PC317 0.1U_0402_25V6
PR322 0_0402_5%
Follow adapter and b ttery c rrent so rce ase on CPU Core VR design.
The resistor will pop on CPU VR schematic.

PR323 100K_0402_1%
PC318 1U_0603_25V6
PR324 10_1206_5%
VF = 0.38V
PD1 S SCH DIO BAS40CW SOT-323
+19V_VIN
@PR326 0_0603_5%
+12.6V_BATT

PR325 10K_0402_1%

VDD=5V
VDD_CHG
PR328 200K_0402_1%
PR329 200K_0402_1%
ACLIM_CHG
CCLIM_CHG
PROG_CHG
COMP_CHG
FSET_CHG
CSOP_CHG
CSOP_CHG_R
PR330 2_0402_5%
PC319 0.1U_0402_25V6
CSON_CHG
CSON_CHG_R
PR334 0_0402_5%

PR333=0 ohm, Fs=500KHZ ~ +/- 15%

+3VS
@VGA@ PR340 10K_0402_1%
@VGA@ PR341 10K_0402_1%
(12,21,36) DGPU_AC_DETECT
@VGA@ PQ314 RUM001L02_VMT3
@VGA@ PQ313B 2N7002KDW_SOT363-6
@VGA@ PQ313A 2N7002KDW_SOT363-6
H_PROCHOT#
AC_IN

Pull high on HW side
@ PR331 76.8K_0402_1%
@ PQ309 L2N7002WT1G_SC70-3
PR336 79K_0402_1%
PR337 100K_0402_1%
PR335 150K_0402_1%
@ PC320 560P_0402_50V7K
PR332 100_0402_1%
PC321 0.015U_0402_25V7K
OCCP setting
Hybrid boost power mode
Cell = 4s

BATT_TEMP (36,42)
BATGONE(BATT_TEMP)
logic high: above 2.4V
logic low: under 0.8V

ICClimit : 7.73A
Delta I : 1.44A
IC charge current :6.48A

Battery current limimed by CCLIm ~ 3.89A.
Ad ter c rrent limimed by ACLIm ~ 4.33A.
(PR779 nd PQ741 re for ch n e ACLIm when AC in)
(Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 20mΩ and Rs2 = 10mΩ)
CC_LIM = VccLIM / 64 x Rs2
(Rs1 = 1 mΩ nd Rs2 = 1 mΩ or Rs1 = 2 mΩ nd Rs2 = 2 mΩ).
CC_LIM = VccLIM / 32 x Rs2
AC_LIM = Vac_LIM / 32 x Rs1

For 4S per cell 4.35V battery

ACIN_CHG
4S_BATT@PR342 2M_0402_1%
4S_BATT@PQ308 LTC015EUBFS8TL_UMT3F
4S_BATT@ PR343 100K_0402_1%
(36) BATT_4S
4S_BATT@ PQ315 2N7002KW_SOT323-3
(14,35,40,45,47) SUSP#

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/01/10 | Deciphered Date | 2014/12/15 |

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Compal Electronics, Inc.

Title: PWR_CHARGER

Size | Document Number | Rev 1.0

Date: Friday, November 30, 2018 | Sheet 43 of 57

Module model information

RT6575D_DMOS_single_V1.mdd
RT6575D_DMOS_dual_V1.mdd

H/S Rds(on):typ:12.4mOhm, max:15.8mOhm
Idsm(TA=25)=13A, Idsm(TA=70)=7.8A
Ploss=0.42W

L/S Rds(on):typ:9.1mOhm, max:11.6mOhm
Idsm(TA=25)=15A, Idsm(TA=70)=9A
Ploss=0.14W

CHOKE:4.7uH, DCR 35mOhm
Ploss=1.77W



Output capacitor ESR need follow below equation to make sure feed back loop stability
ESR=20mV*L*fsw/2V

POK need pull high, it will pull high on VS transfer circuit

5V-OCP=13.5A
3V-OCP=8.9A

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/01/10 | Deciphered Date | 2018/11/04 |

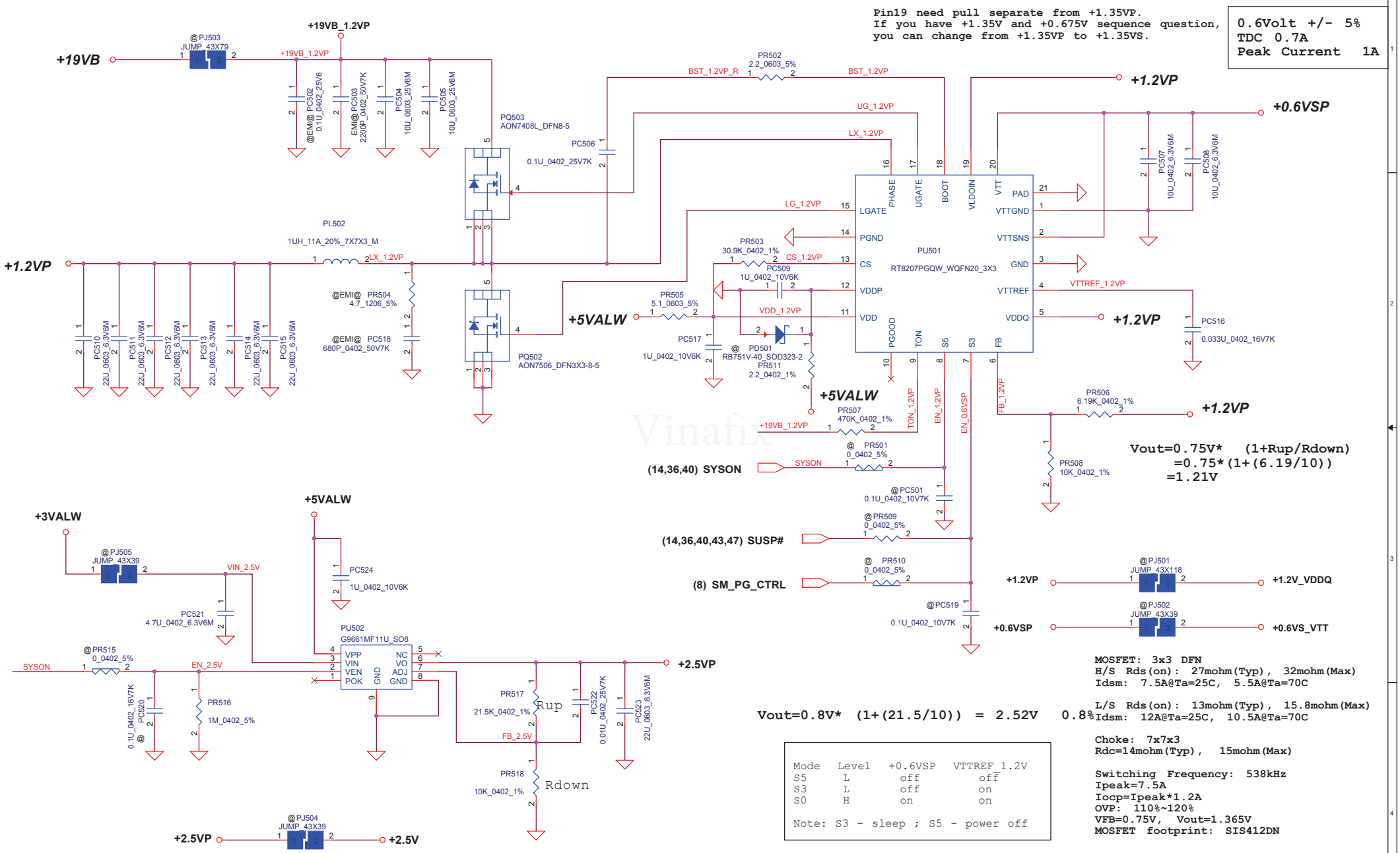


Compal Electronics, Inc.

Title: PWR-3.3VALWP/5VALWP

| Size | Document Number | Rev |
|---|---|---|
| Custom | EH5AW M/B LA-G521P | 0.1 |

Date: Friday, November 30, 2018 Sheet 44 of 57






| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/01/10 | Deciphered Date | 2018/11/04 |



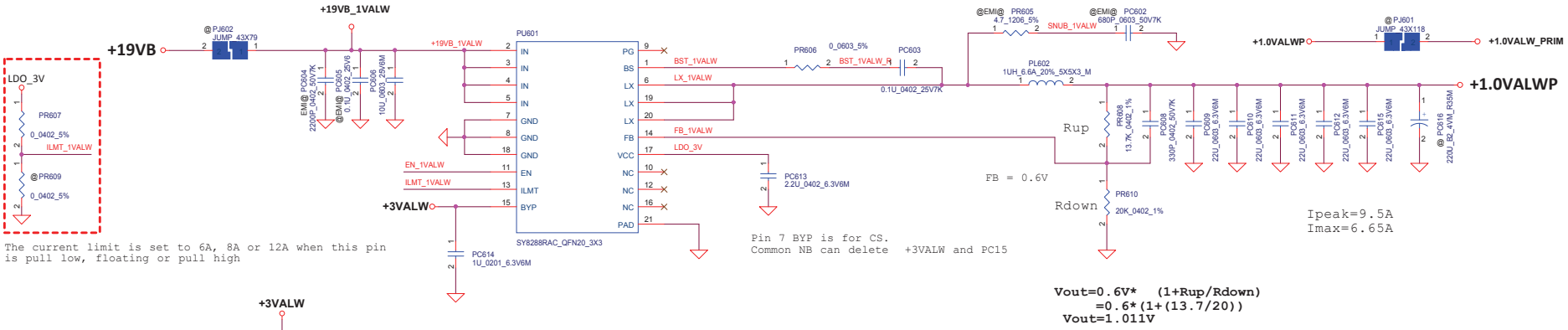
Compal Electronics, Inc.

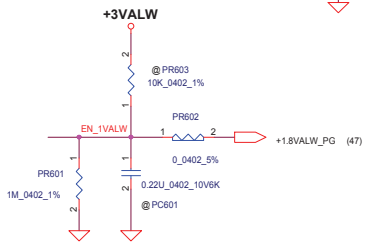
Title: RT8207P

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 0.1

Date: Friday, November 30, 2018 | Sheet 45 of 57

EN pin don't floating
If have pull down resistor at HW side, pls delete PR702






| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/01/10 | Deciphered Date | 2018/11/04 |



Compal Electronics, Inc.

Title: VCCP

| Size | Document Number | Rev |
|---|---|---|
| C | EH5AW M/B LA-G521P | 0.1 |

Date: Friday, November 30, 2018 Sheet 46 of 57

Current limit = 4.7A(min)
0.4%

@N17S_VGA@ PR705 10K_0402_5% +3VALW

(46) +1.8VALW_PG

@N17S_VGA@ PU701 SY8003ADFC_DFN8_2X2

(Common Part) SH00000YG00
4*4*2

@N17S_VGA@ PR701 0_0402_5% EN_1.8VALWP → SPOK_3V_5V (36,44)

@N17S_VGA@ PR703 1M_0402_5%

@N17S_VGA@ PC703 0.1U_0402_16V7K

@ PJ702 JUMP_43X39 +1.8VALWP → +1.8VALW_PRIM

+3VALW

VIN_1.8V

@ PJ701 JUMP_43X79

@N17S_VGA@ PC702 22U_0603_6.3V6M

LX_1.8V

@N17S_VGA@ PL703 1UH_2.8A_30%_4X4X2_F

Rup

@N17S_VGA_EMI@ PR717 4.7_0603_5%

@N17S_VGA@ PR702 20.5K_0402_1%

@N17S_VGA@ PC704 68P_0402_50V8J

@N17S_VGA@ PC705 22U_0603_6.3V6M

@N17S_VGA@ PC727 22U_0603_6.3V6M

+1.8VALWP

FB_1.8V

@N17S_VGA_EMI@ PC726 68P_0402_50V7K

Rdown

@N17S_VGA@ PR704 10K_0402_1%

FB=0.6V
Note:Iload(max)=3A

Function Field :
PWR.Plane.Regulator_1.8V - 35.15
Rest of support elements - 35.16

+3VALW

@ PJ704 JUMP_43X39

VIN_1.8VALW

PC730 4.7U_0402_6.3V6M

+5VALW

PC701 1U_0402_10V6K

PU702 G9661MF11U_SO8

SPOK_3V_5V

PR718 0_0402_5%

EN_1.8VALW

PR719 1M_0402_1%

@ PC728 0.1U_0402_16V7K

+3VALW

PR722 10K_0402_1%

+1.8VALW_PG

@ PJ705 JUMP_43X39 +1.8VALWP → +1.8VALW_PRIM

+1.8VALWP

PR721 12.7K_0402_1%

Rup

FB_1.8VS

PC729 0.01U_0402_25V7K

PC731 22U_0603_6.3V6M

Rdown

PR720 10K_0402_1%

Vout=0.8V* (1+Rup/Rdown)
Vout=0.8V* (1+(12.7/10)) = 1.816V

5*5*H1.5
Idc: 3A
Isat: 4A

+5VS

@ PJ703 JUMP_43X79

@2s_battery_EMI@ PC711 680P_0603_50V7K

@2s_battery_EMI@ PR710 4.7_1206_5%

2s_battery@ PQ701 AON7403L_DFN8-5 P-MOS

2s_battery@ PL702 4.7UH_PCME051E-4R7MS_3A_20% SH00000OG00

2s_battery@ PD701 SS1P4-M3-84A_DO-220AA2

+5VALW

2s_battery@ PR711 100K_0402_1%

2s_battery@ PC712 0.022U_0402_25V7K

2s_battery@ PC713 1500P_0402_50V7K

2s_battery@ PC714 10U_0603_25V6M

2s_battery@ PC715 10U_0603_25V6M

LX_12VSP

FB_12VSP

SS_12VSP

COMP_12VSP

EN_12VSP

2s_battery@ PU703 RT9297GQW_WDFN10_3X3 SA00004JV00

2s_battery@ PR712 88.7K_0402_1%

+12VSP

+INVPWR_B+

@2s_battery bead@ PL701 5A_Z120_25M_0805_2P

2s_battery@ PC716 100P_0402_25V8K

2s_battery@ PC717 10U_0603_25V6M

2s_battery@ PC719 10U_0603_25V6M

2s_battery@ PC718 10U_0603_25V6M

@2s_battery_EMI@ PC720 0.1U_0402_25V6

@2s_battery_EMI@ PC721 2200P_0402_50V7K

2s_battery@ PR715 10K_0402_1%

Vout=1.24*(1+88.7/10)=12.2V

(14,36,40,43,45) SUSP#

@2s_battery@ PR714 0_0402_5%

2s_battery@ PQ702 2N7002KW_SOT323-3

@2s_battery@ PC723 0.1U_0402_10V7K

2s_battery@ PR716 10K_0402_1%

2s_battery@ PC724 4700P_0402_25V7K

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2018/01/10 | Deciphered Date | 2018/11/04 |



Compal Electronics, Inc.

Title: SY8032

Size: C | Document Number: EH5AW M/B LA-G521P | Rev: 0.1

Date: Friday, November 30, 2018 | Sheet 47 of 57

Module model information

RT3602AE_U22_RU42_colay_V1A.mdd for IC portion

RT3602AE_U22_RU42_colay_V1B.mdd for SW portion

Close IC

PRZ1 and PRZ22 are for debug only.
VCCSSA_SENSE and VSSSA_SENSE need other resistor at HW side.

RT3602_VREF Vref=0.6V

+VCC_SA

(14) VCCSA_SENSE

(14) VSSSA_SENSE

Close IC

Close CORE1 choke

(16) VSSSENSE

Close IC

+VCC_CORE

(16) VCCSENSE

Close IC

PRZ41 and PRZ21 are for debug only.
VCCCORE_SENSE and VSSCORE_SENSE need other resistor at HW side.

| | Ra | Rb/Rc |
|---|---|---|
| U22 | N/A | Stuff |
| U42 | Stuff | N/A |

Close CORE1 MOSFET

Set DRVEN output function at PS4. Set to 5V DRVEN is floating, and set to GND DRVEN is low at PS4.

Close GT MOSFET

EN
High: > 0.7V
Low: < 0.3V

+1.0V_VCCST

+3VS

+5VALW

+19VB_CPU

PRZ59 and PRZ60 are for debug only.
VCCGT_SENSE and VSSGT_SENSE need other resistor at HW side.

Close IC

Close IC

Close IC

Close IC



| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2018/01/10 | Deciphered Date | 2019/09/01 |

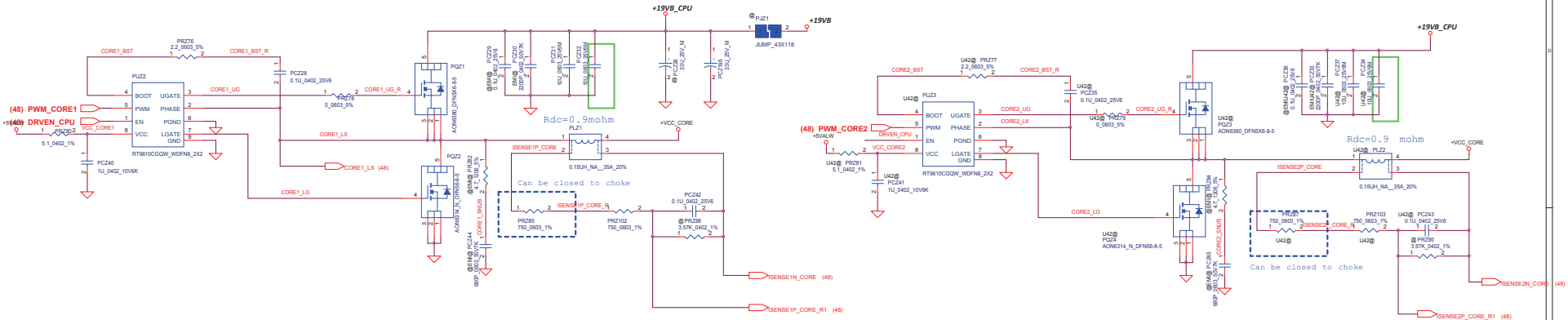


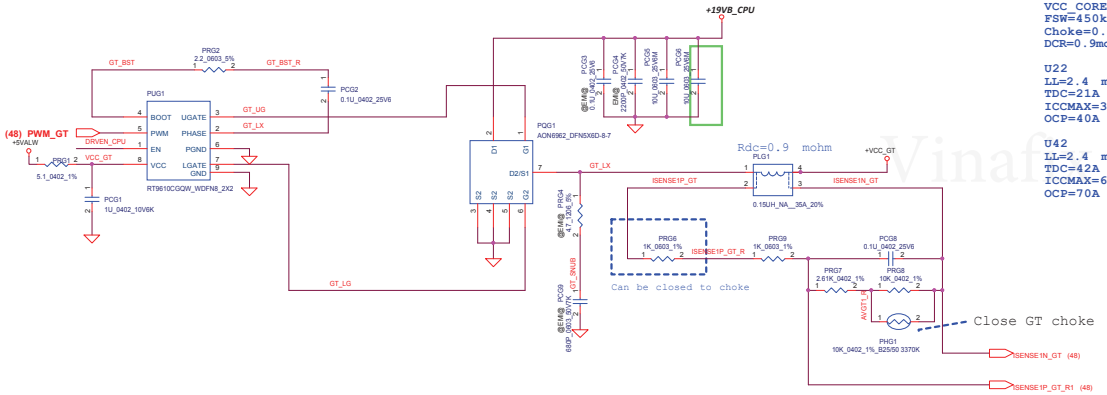
Compal Electronics, Inc.

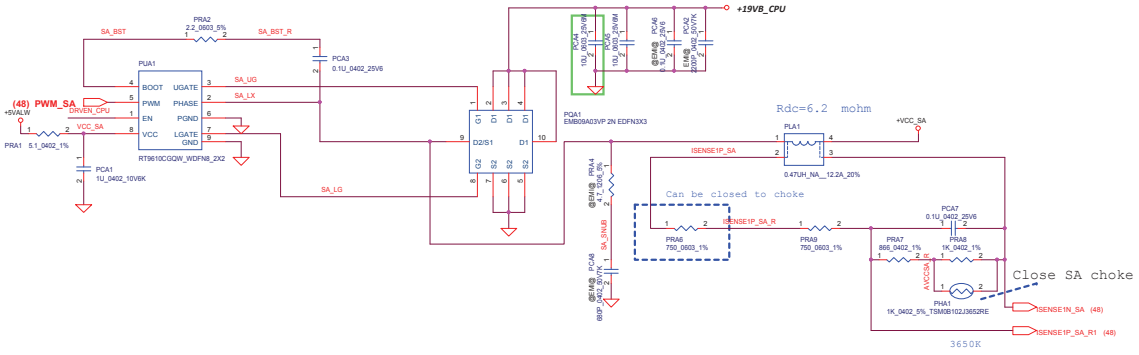
Title: CPU_CORE

Size: Document Number: EH5AW M/B LA-G521P Rev: 0.1

Date: Friday, November 30, 2018 Sheet 48 of 57




**VCC_CORE**
FSW=450kHz
Choke=0.15uH
DCR=0.9mohm +/- 5%

U22
LL=2.4 mohm
TDC=21A
ICCMAX=32A
OCP=40A

U42
LL=2.4 mohm
TDC=42A
ICCMAX=64A
OCP=70A

**VCC_GT**
FSW=450kHz
Choke=0.15uH
DCR=0.9 mohm +/- 5%

U22
LL=3.1 mohm
TDC=18A
ICCMAX=31A
OCP=39A

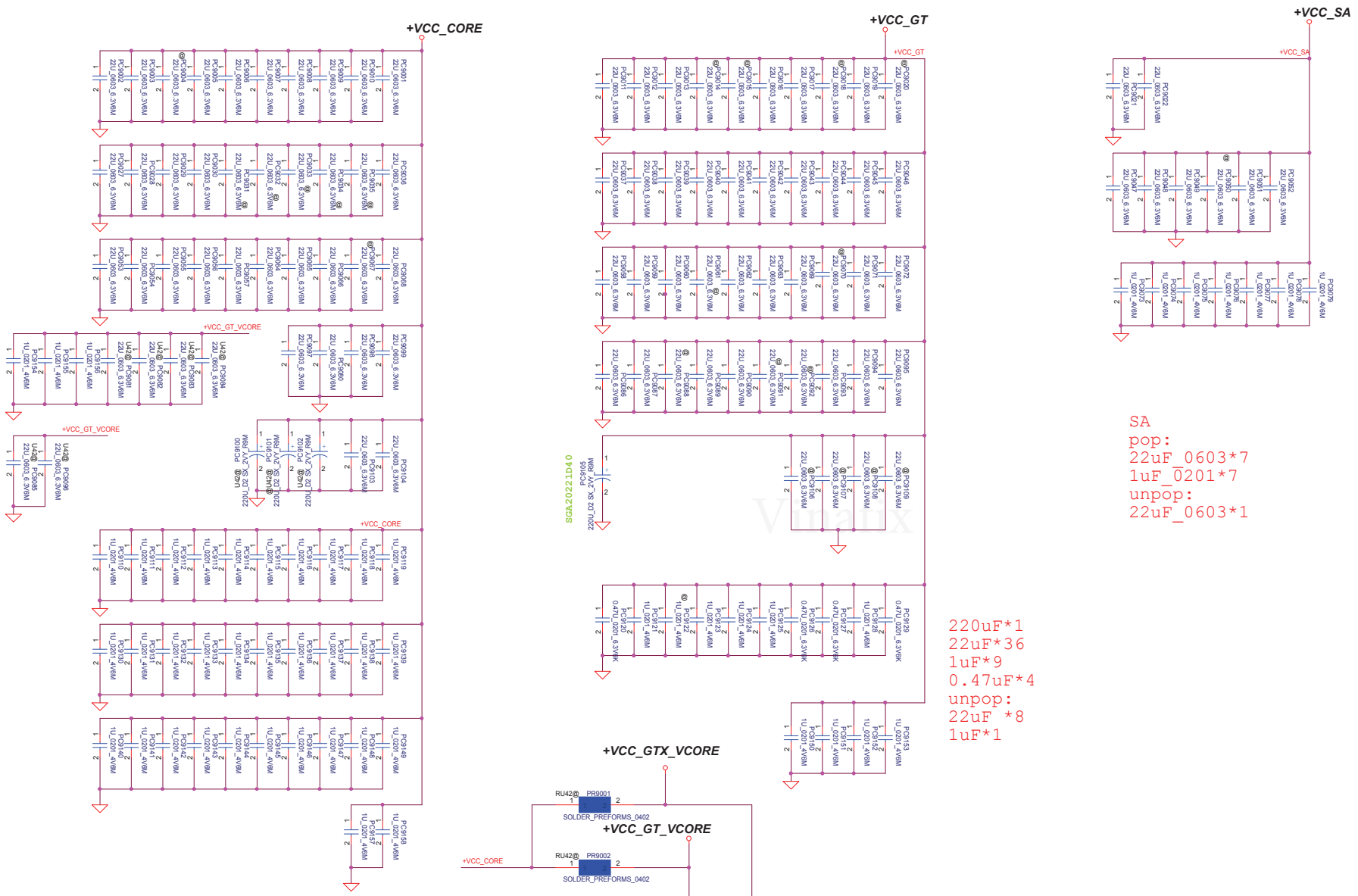
U42
LL=3.1 mohm
TDC=12A
ICCMAX=31A
OCP=39A

**VCC_SA**
FSW=600kHz
DCR=6.2 mohm +/- 5%

U22
LL=10.3 mohm
TDC=4A
ICCMAX=4.5A
OCP=9.5A

U42
LL=10.3 mohm
TDC=
ICCMAX=6A
OCP=9.5A

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2018/01/10 | Deciphered Date | 2019/09/01 | Title: CPU Power stage |
| Size | Document Number | Rev |
| | EH5AW M/B LA-G521P | 0.1 |
| Date: Friday, November 30, 2018 | Sheet 49 of 57 | |




2017/07/03
VCORE Output Capacitor:
U42
22uF_0603*35
1uF_0201*35
220uF *2
UNPOP
22_0603*7

2017/07/03
VCORE Output Capacitor:
U22
22uF_0603*29
1uF_0201*35
UNPOP
22_0603*7
220uF *3

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/10/10 | Deciphered Date | 2018/11/04 |

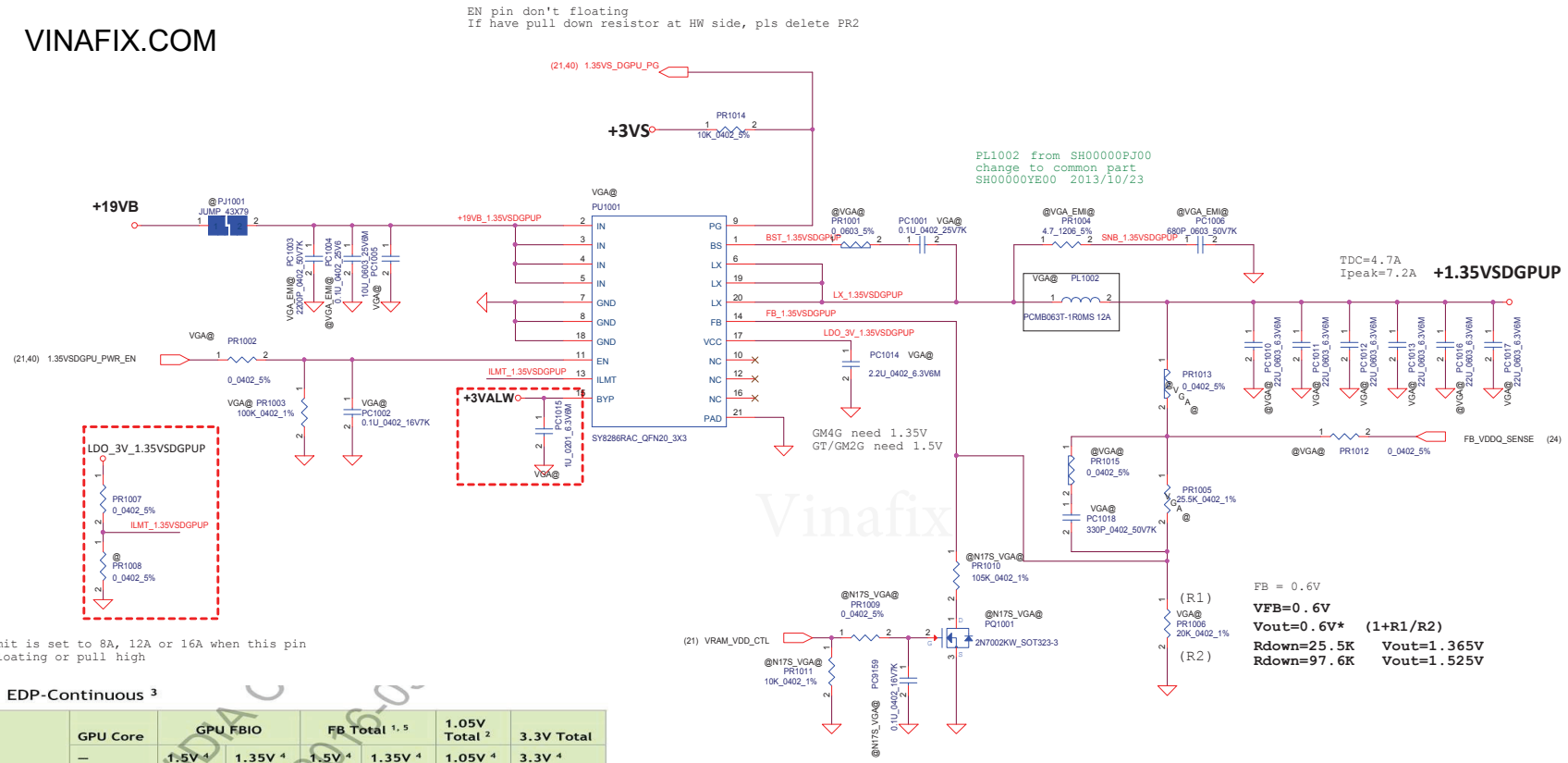


Compal Electronics, Inc.

Title: Power Train

| Size | Document Number | Rev |
|---|---|---|
| C | EH5AW M/B LA-G521P | 0.1 |

Date: Friday, November 30, 2018 Sheet 50 of 57




The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Table 6. EDP-Continuous [3]

| Products | VRAM Type | GPU Core | GPU FBIO | | FB Total [1, 5] | | 1.05V Total [2] | 3.3V Total |
|---|---|---|---|---|---|---|---|---|
| | | — | 1.5V [4] | 1.35V [4] | 1.5V [4] | 1.35V [4] | 1.05V [4] | 3.3V [4] |
| | | (A) | (A) | (A) | (A) | (A) | (A) | (A) |
| N16S-GMR | GDDR5 | 19.0 | — | 2.0 | — | 4.2 | 0.80 | 0.06 |
| | DDR3/L | 21.0 | 1.4 | 1.4 | 2.4 | 2.3 | 0.80 | 0.06 |
| N16S-GTR | GDDR5 @ 2.0 GHz | 26.5 | — | 2.0 | — | 4.2 | 0.80 | 0.06 |
| | GDDR5 @ 2.5 GHz | 26.5 | — | 2.0 | — | 4.7 | 0.80 | 0.06 |
| | DDR3/L | 26.0 | 1.4 | 1.4 | 2.4 | 2.3 | 0.80 | 0.06 |
| N16S-GXR | GDDR5 | 35.4 | — | 2.4 | — | 4.9 | 2.6 | 0.40 |

Table 7. EDP-Peak [3]

| Products | VRAM Type | GPU Core | GPU FBIO | | FB Total [1, 5] | | 1.05V Total [2] |
|---|---|---|---|---|---|---|---|
| | | — | 1.5V [4] | 1.35V [4] | 1.5V [4] | 1.35V [4] | 1.05V [4] |
| | | (A) | (A) | (A) | (A) | (A) | (A) |
| N16S-GMR | GDDR5 | 34.0 | — | 2.9 | — | 6.8 | 2.1 |
| | DDR3/L | 39.5 | 2.6 | 2.3 | 4.1 | 3.9 | 2.1 |
| N16S-GTR | GDDR5 @ 2.0 GHz | 53.0 | — | 2.9 | — | 6.8 | 2.1 |
| | GDDR5 @ 2.5 GHz | 53.0 | — | 3.1 | — | 7.2 | 2.1 |
| | DDR3/L | 51.0 | 2.6 | 2.3 | 4.1 | 3.9 | 2.1 |
| N16S-GXR | GDDR5 | 54.0 | — | 4.6 | — | 9.5 | 2.9 |

Table 7. Output EDP-Continuous

| Product | NVVDD | GPU FBIO | FB Total[5] | 1.0V Total[1] | 1.8V Total[2] |
|---|---|---|---|---|---|
| | — | 1.35V[4] | 1.35V[4] | 1.0V[4] | 1.8V[4] |
| | (A) | (A) | (A) | (A) | (A) |
| N17S-G1 | 29.7 | 2.0 | 3.4 | 0.1 | 0.3 |
| N17S-LG | 15.4 | 1.6 | 2.8 | 0.1 | 0.2 |

Table 8. Output EDP-Peak

| Product | NVVDD | GPU FBIO | FB TOTAL[4] | 1.0V Total[1] |
|---|---|---|---|---|
| | — | 1.35V[3] | 1.35V[3] | 1.0V[3] |
| | (A) | (A) | (A) | (A) |
| N17S-G1 | 59.2 | 3.2 | 6.6 | 0.2 |
| N17S-LG | 49.6 | 3.2 | 6.6 | 0.2 |




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2018/01/10 | Deciphered Date | 2018/11/04 |



Compal Electronics, Inc.

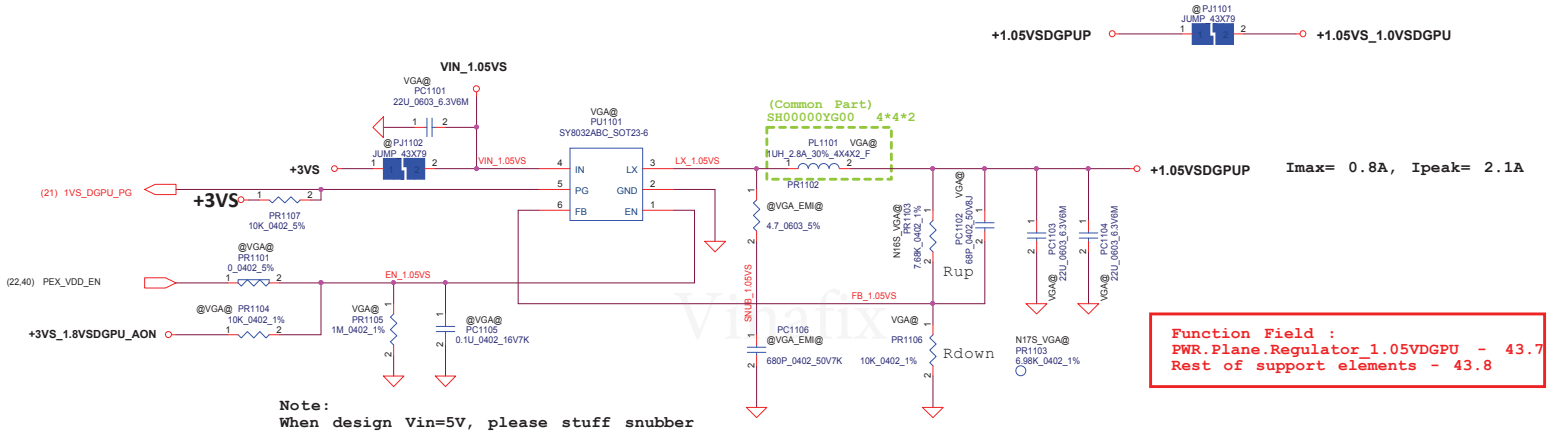
Title: Power Train

| Size | Document Number | Rev |
|---|---|---|
| C | EH5AW M/B LA-G521P | 0.1 |

Date: Friday, November 30, 2018 Sheet 51 of 57

Module model information

SY8032_V2.mdd




Function Field :
PWR.Plane.Regulator_1.05VDGPU - 43.7
Rest of support elements - 43.8

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)
N16=>1.05V
=>0.6V*(1+(7.68/10)=1.061 (1.01%)
=>0.6V*(1+(7.32/10)=1.039 (-1%)

N17=>1.0V
Vout=0.6V*(1+(6.98/10)=1.019V (1.02%)



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/01/10 | Deciphered Date | 2018/11/04 |



Compal Electronics, Inc.

Title: Power Train

| Size | Document Number | Rev |
|---|---|---|
| C | EH5AW M/B LA-G521P | 0.1 |

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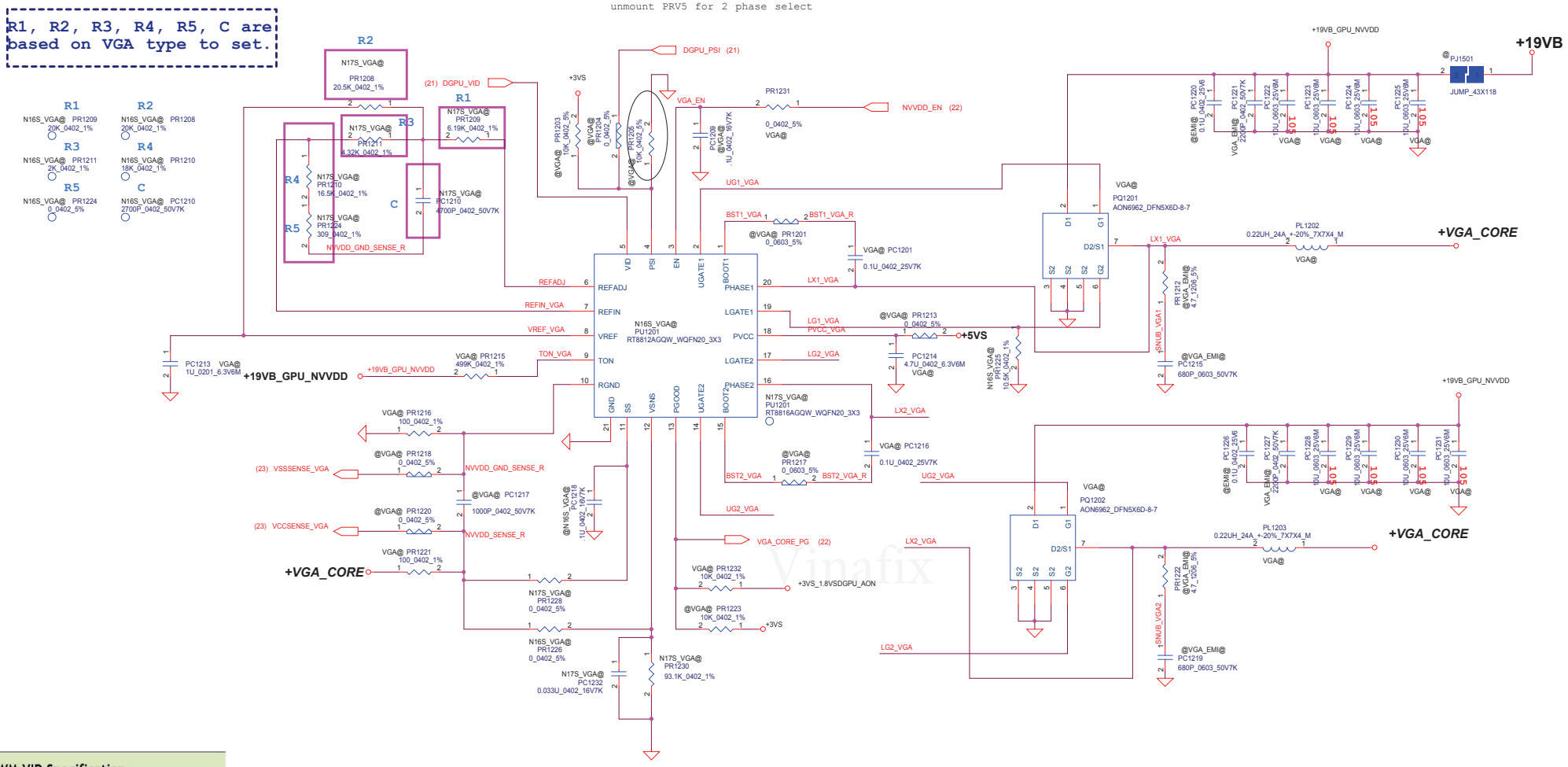
R1, R2, R3, R4, R5, C are based on VGA type to set.




| PWM-VID Specification | | |
|---|---|---|
| | | Config B |
| Vmin | V | 0.6 |
| Vmax | V | 1.2 |
| Vboot | V | 0.9 |
| Voltage Step Vstep | mV | 6.25 |
| Number of Voltage Levels N | level | 96 |
| PWM Frequency $F_{PWM}$ | MHz | 1.125 |
| PWM Minimum Pulse Width $T_{DMIN}$ | ns | 9.26 |
| VID Transient Time T | us | <100 |
| **Component Value** | | |
| R1 (1%) | KΩ | 20 |
| R2 (1%) | KΩ | 20 |
| R3 (1%) | KΩ | 2 |
| R4 (1%) | KΩ | 18 |
| R5 (1%) | KΩ | 0 |
| C | nF | 2.7 |

N17x DG-07875-001_v08.pdf:

Table 7.8 PWM-VID Spec and Component Values

| PWM-VID Specification | Unit | Config |
|---|---|---|
| Vmin | V | 0.3 |
| Vmax | V | 1.3 |
| Vboot | V | 0.8 |
| Voltage Step Vstep | mV | 6.25 |

Table 7.8 PWM-VID Spec and Component Values

| PWM-VID Specification | Unit | Config |
|---|---|---|
| Number of Voltage Levels N | level | 160 |
| PWM Frequency $F_{PWM}$ | kHz | 675 |
| PWM Minimum Pulse Width $T_{DMIN}$ | ns | 9.26 |
| VID Transient Time T | us | <100 |
| **Component Value** | | |
| R1 (1%) | KΩ | 6.19 |
| R2 (1%) | KΩ | 20.5 |
| R3 (1%) | KΩ | 4.32 |
| R4 (1%) | KΩ | 16.5 |
| R5 (1%) | KΩ | 0.309 |
| C | nF | 4.7 |

Table 6. EDP-Continuous [3]

| Products | VRAM Type | GPU Core – (A) |
|---|---|---|
| N16S-GMR | GDDR5 | 19.0 |
| | DDR3/L | 21.0 |
| N16S-GTR | GDDR5 @ 2.0 GHz | 26.5 |
| | GDDR5 @ 2.5 GHz | 26.5 |
| | DDR3/L | 26.0 |
| N16S-GXR | GDDR5 | 35.4 |

Table 7. EDP-Peak [3]

| Products | VRAM Type | GPU Core – (A) |
|---|---|---|
| N16S-GMR | GDDR5 | 34.0 |
| | DDR3/L | 39.5 |
| N16S-GTR | GDDR5 @ 2.0 GHz | 53.0 |
| | GDDR5 @ 2.5 GHz | 53.0 |
| | DDR3/L | 51.0 |
| N16S-GXR | GDDR5 | 54.0 |

Table 7. Output EDP-Continuous

| Product | NVVDD – (A) | GPU FBIO 1.35V[4] (A) | FB Total[5] 1.35V[4] (A) | 1.0V Total[1] 1.0V[4] (A) | 1.8V Total[2] 1.8V[4] (A) |
|---|---|---|---|---|---|
| N17S-G1 | 29.7 | 2.0 | 3.4 | 0.1 | 0.3 |
| N17S-LG | 15.4 | 1.6 | 2.8 | 0.1 | 0.2 |

Table 8. Output EDP-Peak

| Product | NVVDD – (A) | GPU FBIO 1.35V[3] (A) | FB TOTAL[4] 1.35V[3] (A) | 1.0V Total[1] 1.0V[3] (A) |
|---|---|---|---|---|
| N17S-G1 | 59.2 | 3.2 | 6.6 | 0.2 |
| N17S-LG | 49.6 | 3.2 | 6.6 | 0.2 |



| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2018/01/10 | Deciphered Date | 2018/11/04 |



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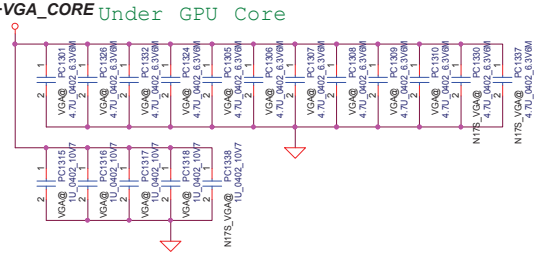
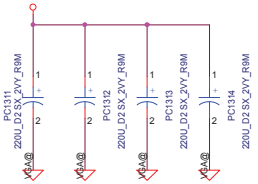
## GB4-128 package

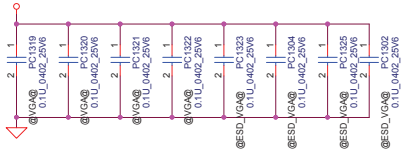
+VGA_CORE Under GPU Core



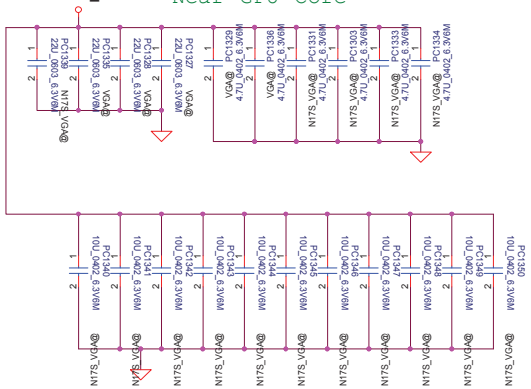

+VGA_CORE




+VGA_CORE




+VGA_CORE Near GPU Core






| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2018/01/10 | Deciphered Date | 2018/11/04 |



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