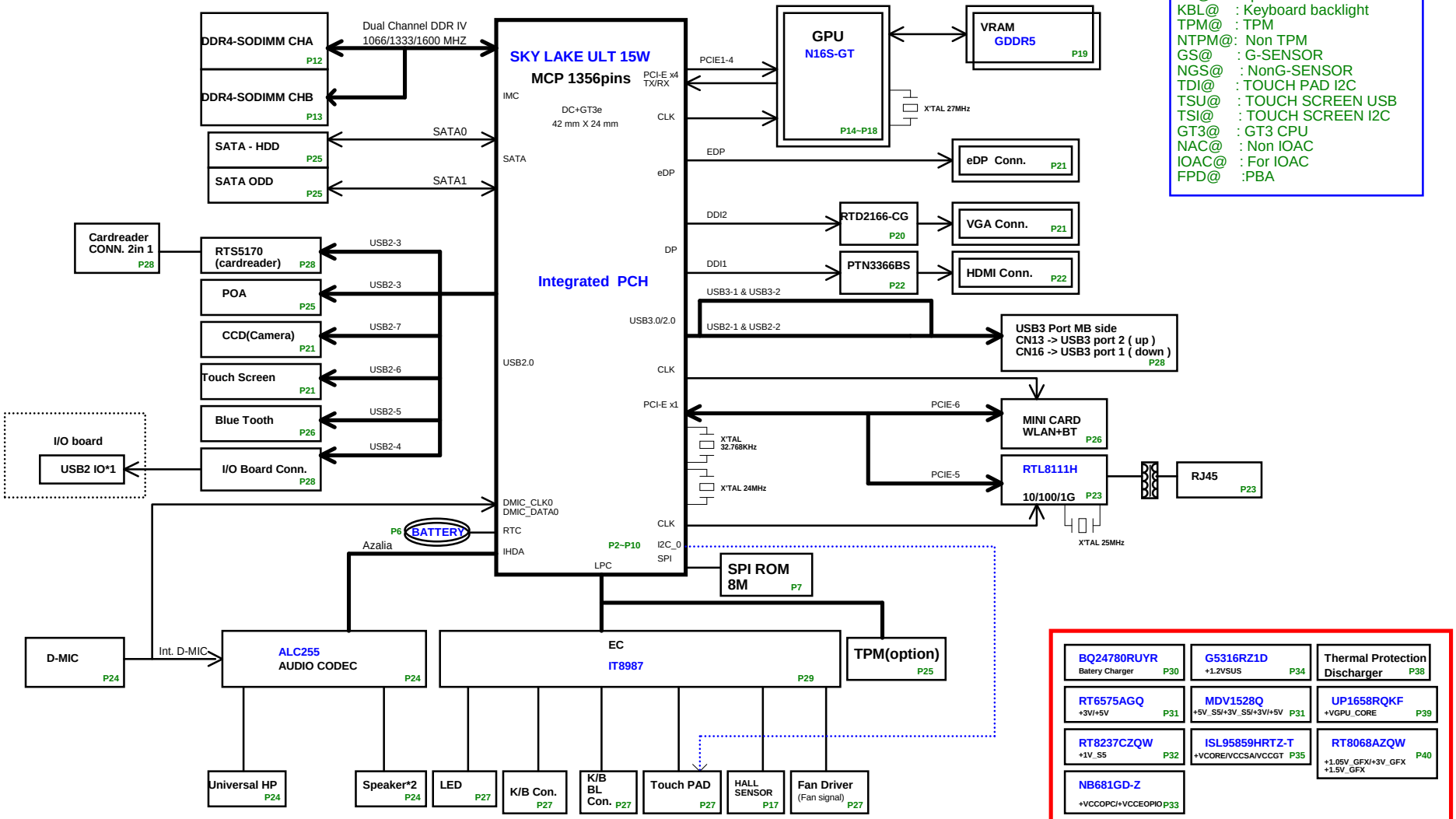
Z8VR Serials SKL ULT SYSTEM BLOCK DIAGRAM

BOM

IV@ : iGPU
EV@ : Optimus
KBL@ : Keyboard backlight
TPM@ : TPM
NTPM@: Non TPM
GS@ : G-SENSOR
NGS@ : NonG-SENSOR
TDI@ : TOUCH PAD I2C
TSU@ : TOUCH SCREEN USB
TSI@ : TOUCH SCREEN I2C
GT3@ : GT3 CPU
NAC@ : Non IOAC
IOAC@ : For IOAC
FPD@ :PBA

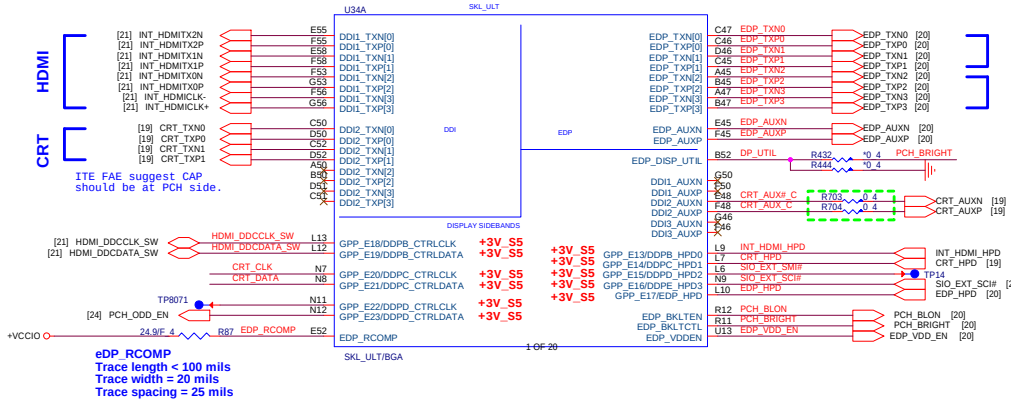


BQ24780RUYR Batery Charger P30	G5316RZ1D +1.2VSUS P34	Thermal Protection Discharger P38
RT6575AGQ +3V/+5V P31	MDV1528Q +5V_S5/+3V_S5/+3V/+5V P31	UP1658RQKF +VGPU_CORE P39
RT8237CZQW +1V_S5 P32	ISL95859HRTZ-T +VCORE/VCCSA/VCCGT P35	RT8068AZQW +1.05V_GFX/+3V_GFX +1.5V_GFX P40
NB681GD-Z +VCCOPC/+VCCEOPIO P33		

Quanta Computer Inc.
PROJECT : Z8VR
Size | Document Number | Block Diagram | Rev 1A
Date: Thursday, June 22, 2017 | Sheet 1 of 46

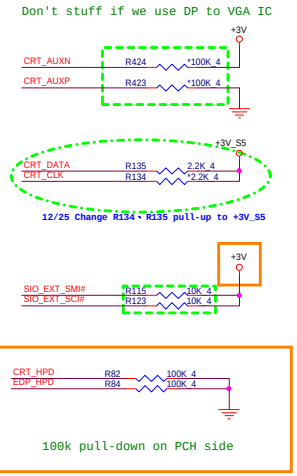
Skylake ULT (DISPLAY,eDP)

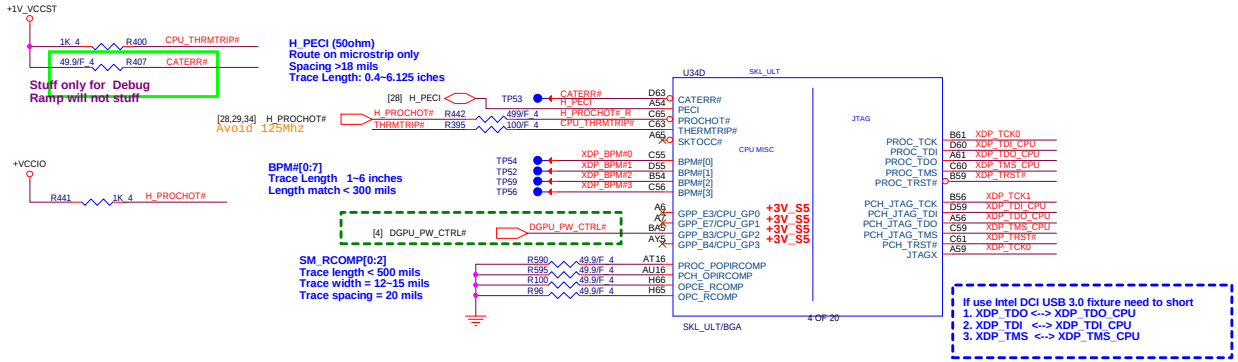
02



eDP Panel

Reserve 2 Lane for 4K x 2K





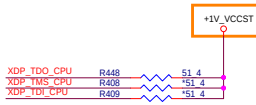
If use Intel DCI USB 3.0 fixture need to short
1. XDP_TDO <--> XDP_TDO_CPU
2. XDP_TDI <--> XDP_TDI_CPU
3. XDP_TMS <--> XDP_TMS_CPU

PCH JTAG

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

TCK,TMS
Trace Length < 9000mils

MP remove(Intel)

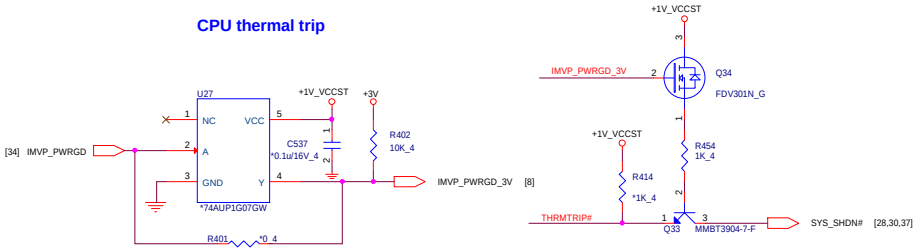


H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

,XDP_TCK1,XDP_TMS
don't need pull up or pull down

XDP_TCK0 R558 Stuff

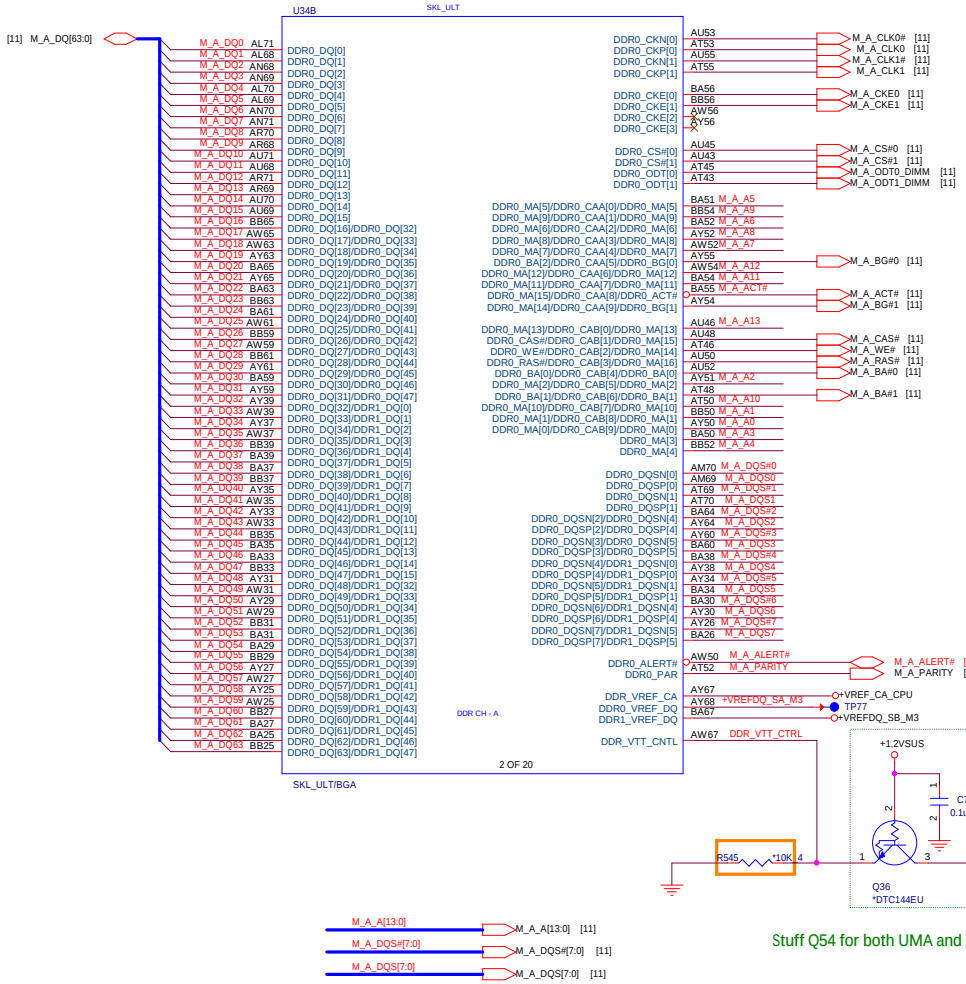
CPU thermal trip



Quanta Computer Inc.			
PROJECT : Z8VR			
Size	Document Number		Rev
	Skylake 1/4 (DDI/eDP)		1A
Date: Thursday, June 22, 2017		Sheet 2 of 46	

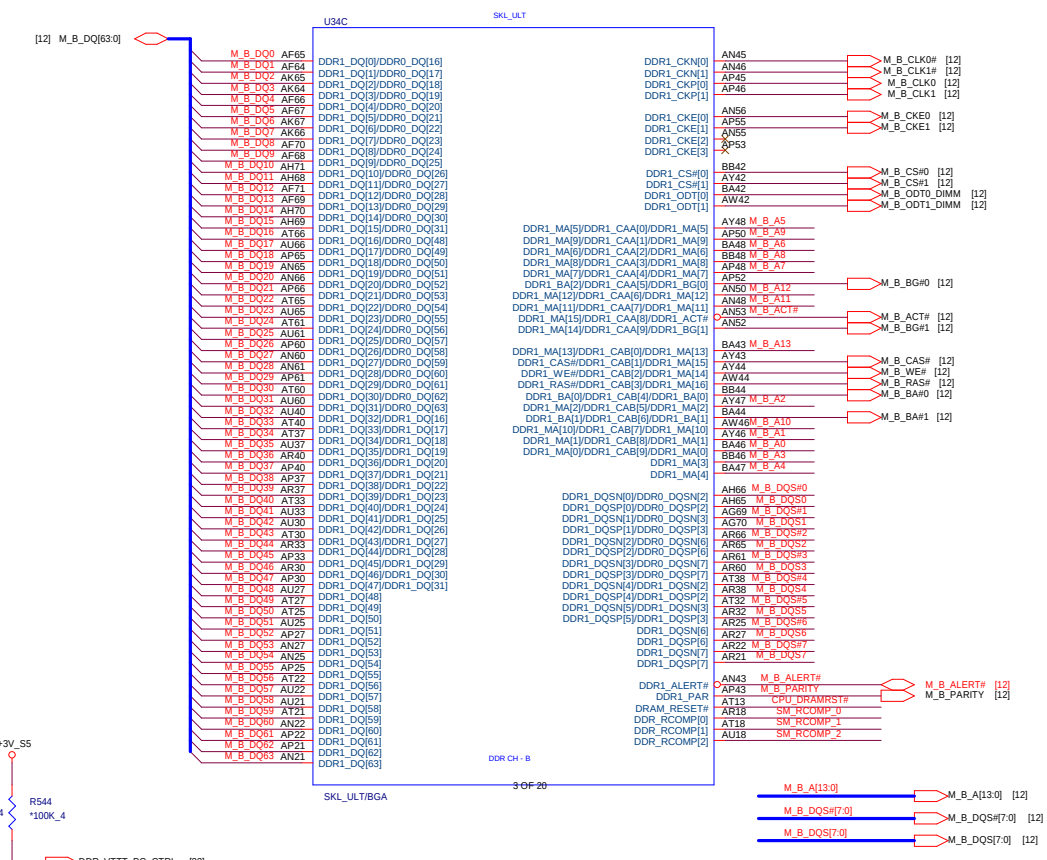
Change Data and DQS to interleave.

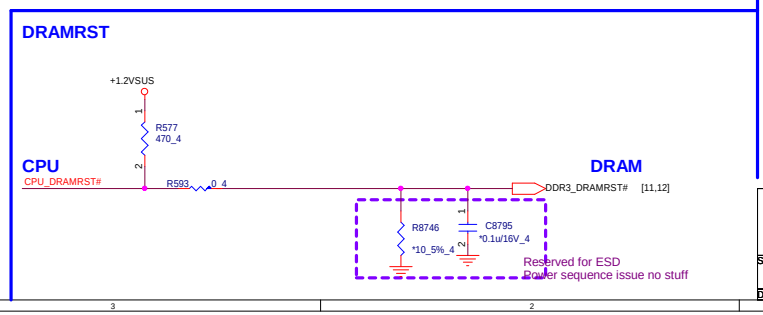
SKL ULT (DDR4)



Stuff Q54 for both UMA and GPU in DDR_VTT_CNTL

SKL ULT (DDR4)

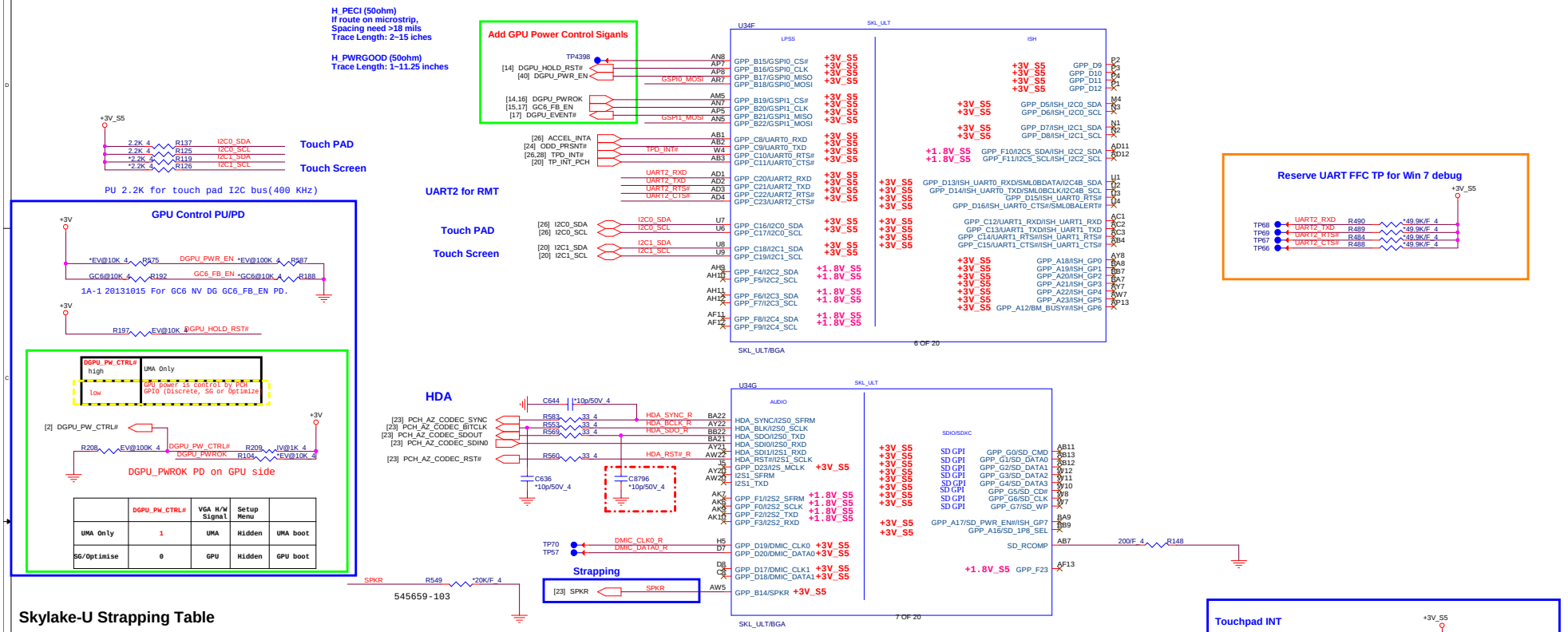




Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	Skylake 2/3 (DDR3 I/F)	1A
Date: Thursday, June 22, 2017	Sheet 3 of 46	

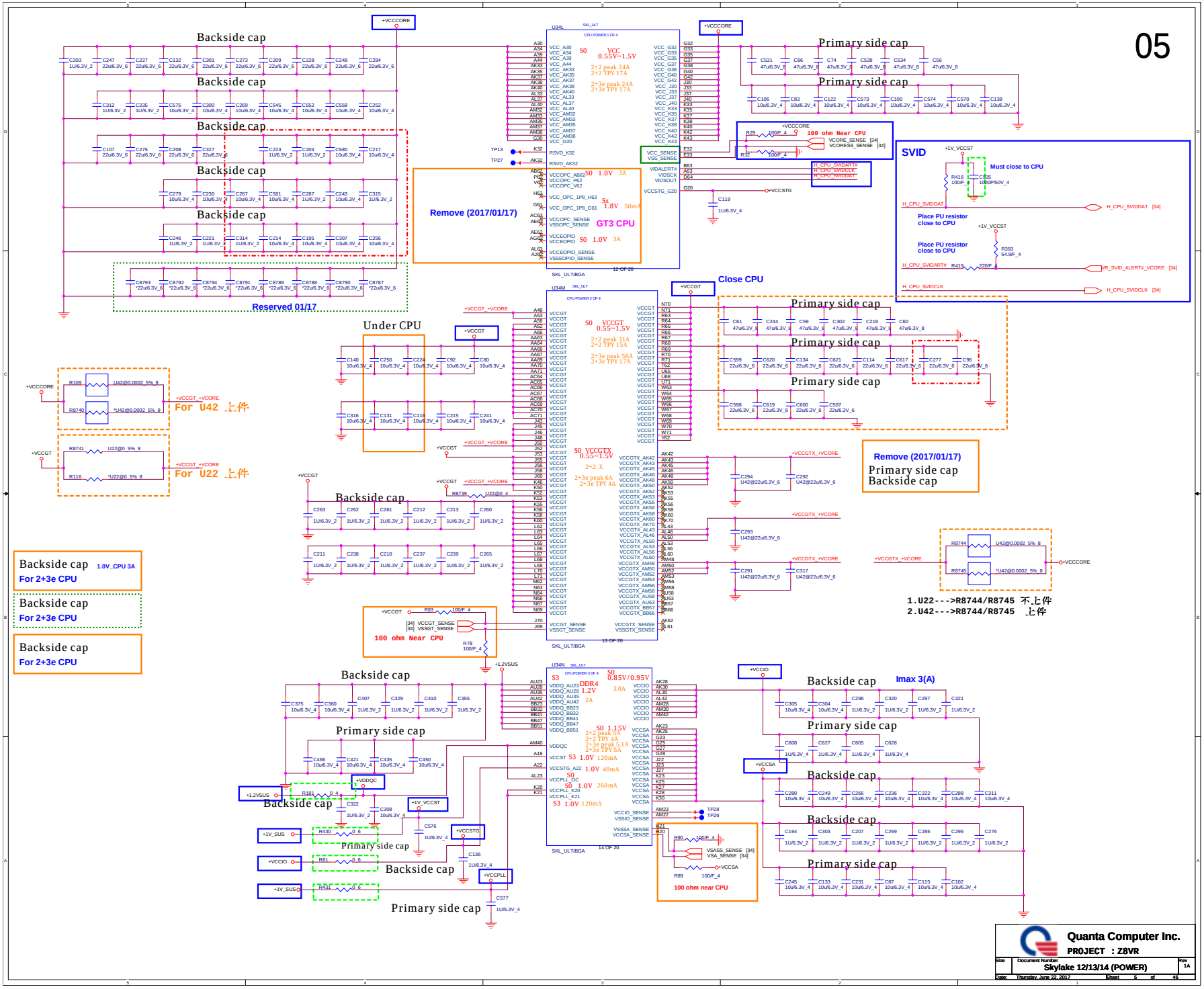
SKL ULT (SIDEBAND) GPIO



Skylake-U Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = *Disable Top Swap (iPD 20K) 1 = Enable Top Swap Mode	+3V R550 *1K_4 SPKR
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	+3V R543 *1K_4 GSPI0_MOSI
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Cryp to TLS(iPD 20K) 1 = Enable Intel ME Cryp to TLS	+3V_S5 R144 *10K_4 SMBALERT# [7]
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (iPD 20K) 1 = LPC	+3V R191 *1K_4 GSPI1_MOSI
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (iPD 20K) 1 = eSPI selected for EC	+3V_S5 R481 *1K_4 SML0ALERT# [7]
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_MISO	Reserved	RSMRST#	(iPU 15 ~ 40K)	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K)	
SPI0_IO2	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 ~ 40K)	
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (iPD 20K) 1 = Disable Flash Descriptor Security (Override)	change location to near CPU to prevent impact HDA_SDO signal HDA_SDO_R R570 *1K_4 ME_WR# [28]
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (iPD 20K) 1 =Port B is detected	
GPP_E21 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (iPD 20K) 1 =Port C is detected	

Quanta Computer Inc.		
PROJECT : Z8VR		
Size	Document Number: Skylake 6/7 (PEG/DMI/FDI)	Rev 1A
Date: Thursday, June 22, 2017	Sheet 4 of 46	


Backside cap
Primary side cap
Reserved 01/17
Remove (2017/01/17)
GT3 CPU
Under CPU
Close CPU
SVID
Must close to CPU
Place PU resistor close to CPU
For U42 上件
For U22 上件
Remove (2017/01/17)
Primary side cap
Backside cap
100 ohm Near CPU
100 ohm near CPU
Imax 3(A)
1.U22--->R8744/R8745 不上件
2.U42--->R8744/R8745 上件
Backside cap 1.0V_CPU 3A
For 2+3e CPU
Backside cap
For 2+3e CPU
Backside cap
For 2+3e CPU
Quanta Computer Inc.
PROJECT : Z8VR
Skylake 12/13/14 (POWER)
Thursday, June 22, 2017

Skylake ULT (GPU, SATA , ODD, CLK ,USB2&3)

06

dGPU PEG*4 / HDD / ODD / LAN / WIFI

MB USB3.0 CN16 (Charger IC) Down

MB USB3.0 CN13 -> Up

MB USB3.0 CN16 (Charger IC) Down

MB USB3.0 CN13 -> Up

DB USB2.0

POA (Reserved)

BT

Touch Screen

CCD

Card reader

USBCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

MB U3
MB U3
DB U2

Near CPU
01/17

SKL_ULT_BGA

8 OF 20

M.2 SSD N16S VGA / LAN / WLAN

1V power plane
0.71 checklist p14

SKL_ULT_BGA

10 OF 20

add for EC reset RTC

PCH PU/PD

Add SSD ID 1/14

Hight is SSD , Low is ODD

Skylake-U userd 24 MHz (50 Ohm ESR) XTAL

BG624000078 -> HHE(1st)
BG624000044 -> TXC(2nd)

01/17

Note: Change Y4 to 38.4 MHz(ESR 30 ohm) for Cannonlake U

RTC Clock 32.768KHz (RTC)

CH01006JB08 -> 10p
CH01506JB06 -> 15p
CH-6806TB01 -> 6.8p

Trace length < 1000 mils

BG3327680C6 -> HHE(1st)

BG332768099 -> TXC(2nd)--EOD
Change to BG332768104

RTC Circuitry (RTC)

On SKL voltage at VCCRTC does not exceed 3.2V

+3V_RTC
Trace width = 30 mils

+3V_RTC_[0:2]
Trace width = 20 mils

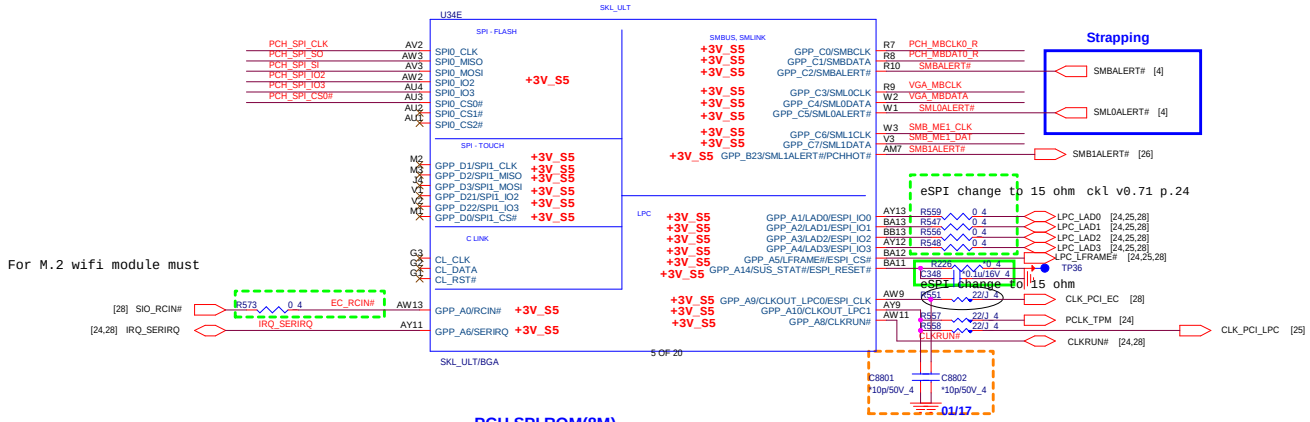
1A-22013/10/16 Chage +3V_RTC_0 to VCCTC_2.

1. AHL03003057 DBV CR2032
2. AHL03003003 VDE CR2032

Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	Skylake 9/10 (PEG/USB/CLK)	1A

Date: Thursday, June 22, 2017 Sheet 6 of 46



Strapping

SMBALERT# [4]
SML0ALERT# [4]
SML1ALERT# [26]

eSPI change to 15 ohm ckl v0.71 p.24

eSPI change to 15 ohm

For M.2 wifi module must

[28] SIO_RCIN#
[24,28] IRQ_SERIRQ
R573 0_4
EC_RCIN#
IRQ_SERIRQ

SMBus

Termination Resistor Requirement for PCH PCHHOT# Pin
Reserve PU 150K resistor

PCH SPI ROM(8M)
15ohm CS01502JB12
33ohm CS03302JB29

01/17

SP@ socket P/N: DFHS08FS023 only for A-TEST

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
	GGD	8M	AKE2EZN0Q00	GD25B64CSIGR
	WND	16M	AKE3DZN0N01	W25Q128FVSIQ
	GGD	16M	AKE3DZN0Q02	GD25B127DSIGR

3.3K is original and for no support fast read function

reserve for SPI fast read

only 0ohm option

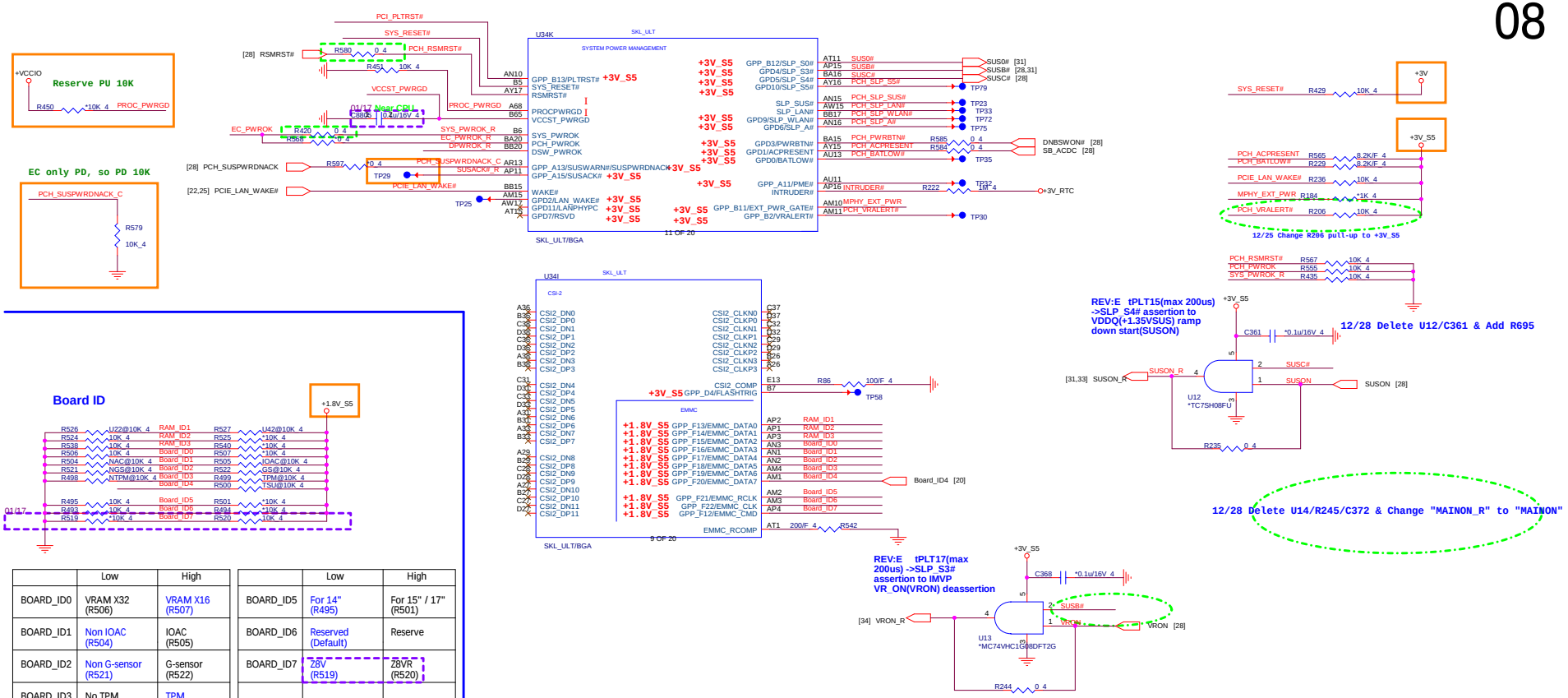
S5 SMBus(PCH) S0

Change to 2.2k

PCH_XDP_WLAN/S5 DDR_TP/S0

SMBus(EC)

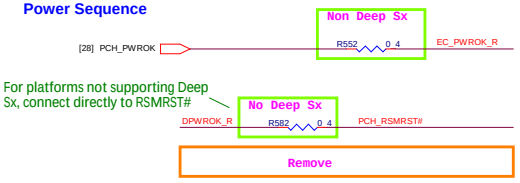
EC/S5



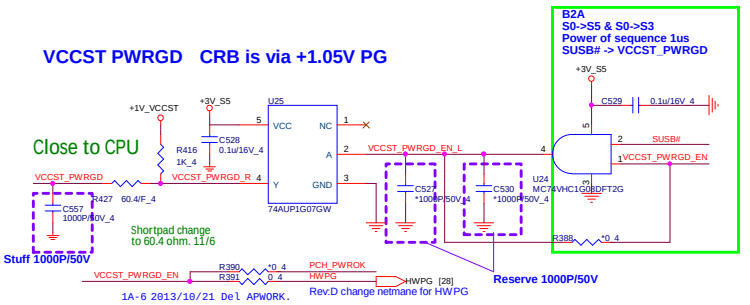
	Low	High
BOARD_ID0	VRAM X32 (R506)	VRAM X16 (R507)
BOARD_ID1	Non IOAC (R504)	IOAC (R505)
BOARD_ID2	Non G-sensor (R521)	G-sensor (R522)
BOARD_ID3	No TPM (R498)	TPM (R499)
BOARD_ID4	No-Touch panel	Touch panel (R500)

	Low	High
BOARD_ID5	For 14" (R495)	For 15" / 17" (R501)
BOARD_ID6	Reserved (Default)	Reserve
BOARD_ID7	Z8V (R519)	Z8VR (R520)

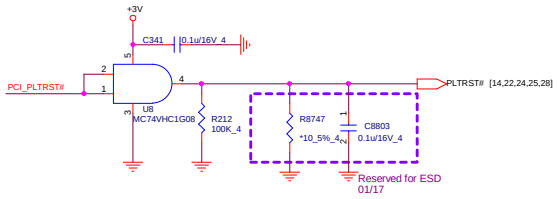
Power Sequence



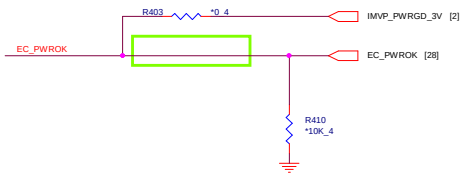
VCCST PWRGD CRB is via +1.05V PG



PLTRST# Buffer

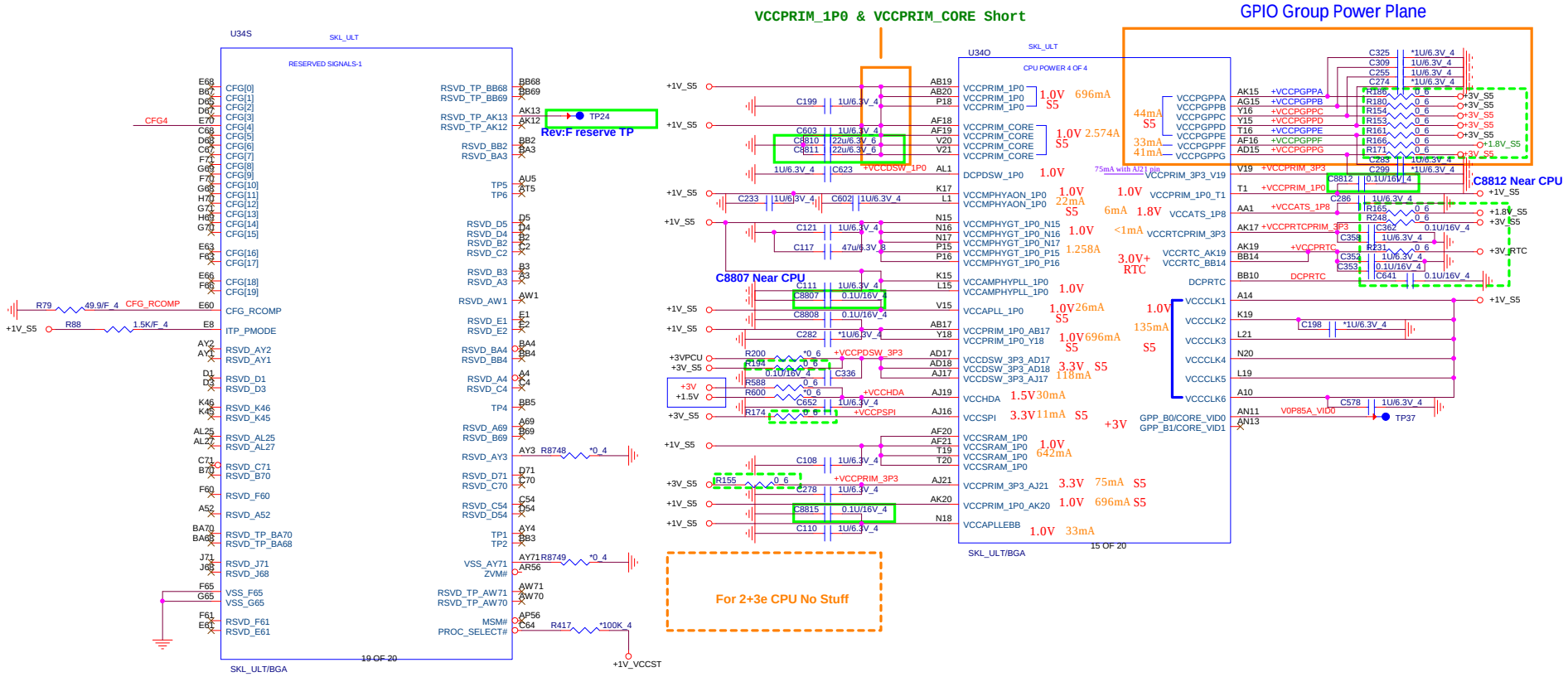


SYSPWOK



Quanta Computer Inc.
PROJECT : Z8VR

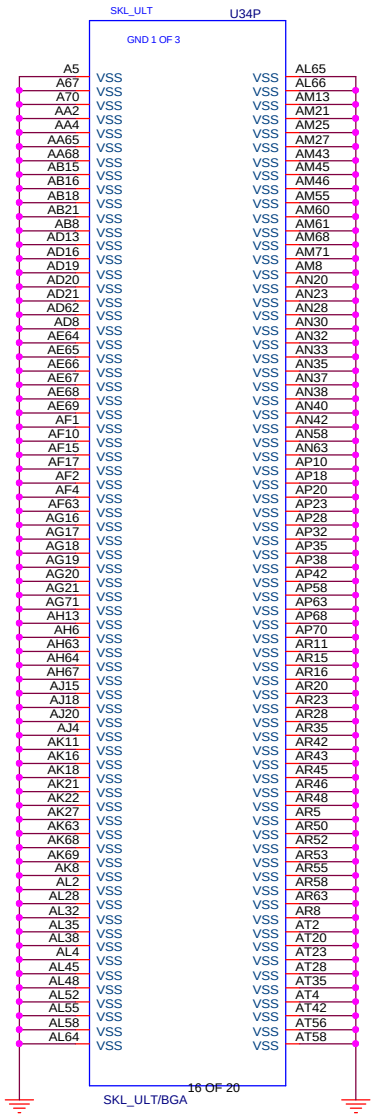
Size	Document Number	Rev
	Skylake 9/11 (PWROK/Board_ID)	1A
Date: Thursday, June 22, 2017	Sheet 8 of 46	

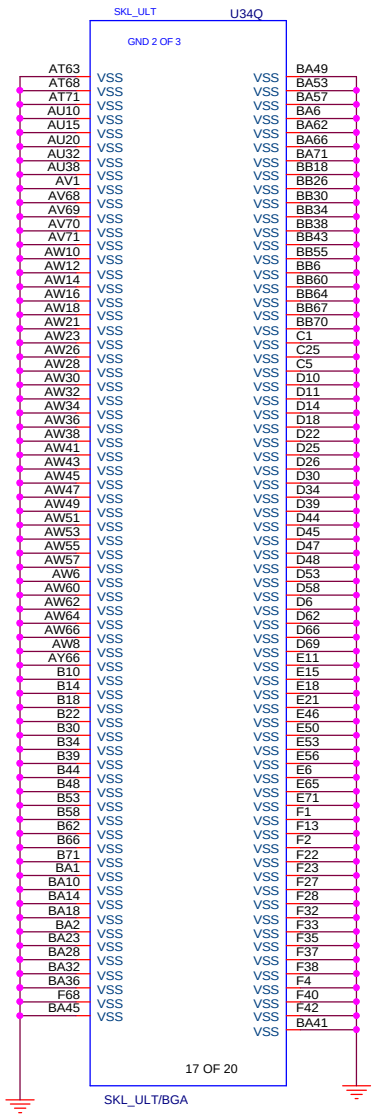


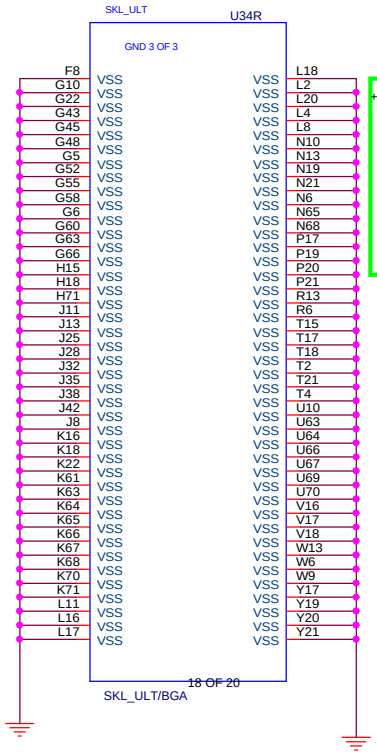
Pin Name	Strap description	Configuration	Note
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	**1 = *Normal Operation; No stall (iPU 3K)** 0 = Stall	
CFG[1]	Reserved Configuration lane		
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal	**1 = *Normal Operation(iPU 3K)** 0 = Lan number reversed	**H & S processor used only**
CFG[3]	Reserved Configuration lane		
CFG[4]	eDP enable	1 = Disabled (iPU 3K) **0 = *Enabled**	CFG4 R455 1K_4
CFG[6:5]	PCI Express* Bifunction	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*	**H & S processor used only**
CFG[7]	PEG Training	**1 = *PEG Train immediatedly follow RESET# de-assertion (iPU 3K)** 0 = PEG wait for BIOS for training	**H & S processor used only**
CFG[19:8]	Reserved Configuration lane		

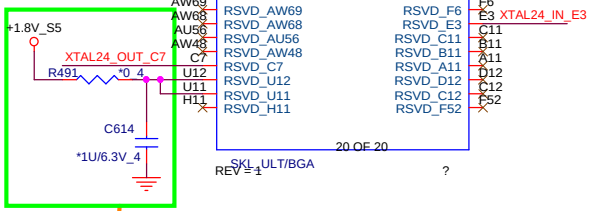
Quanta Computer Inc.			
PROJECT : Z8VR			
Size	Document Number		Rev
	Skylake PCH-LP 15/19 (POWER)		1A
Date: Thursday, June 22, 2017		Sheet 9 of 46	

Skylake ULT (GND)



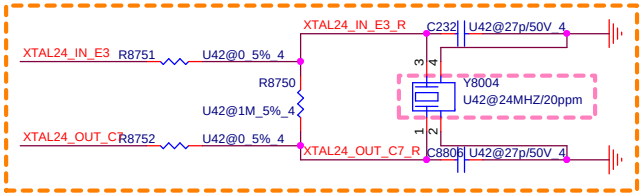






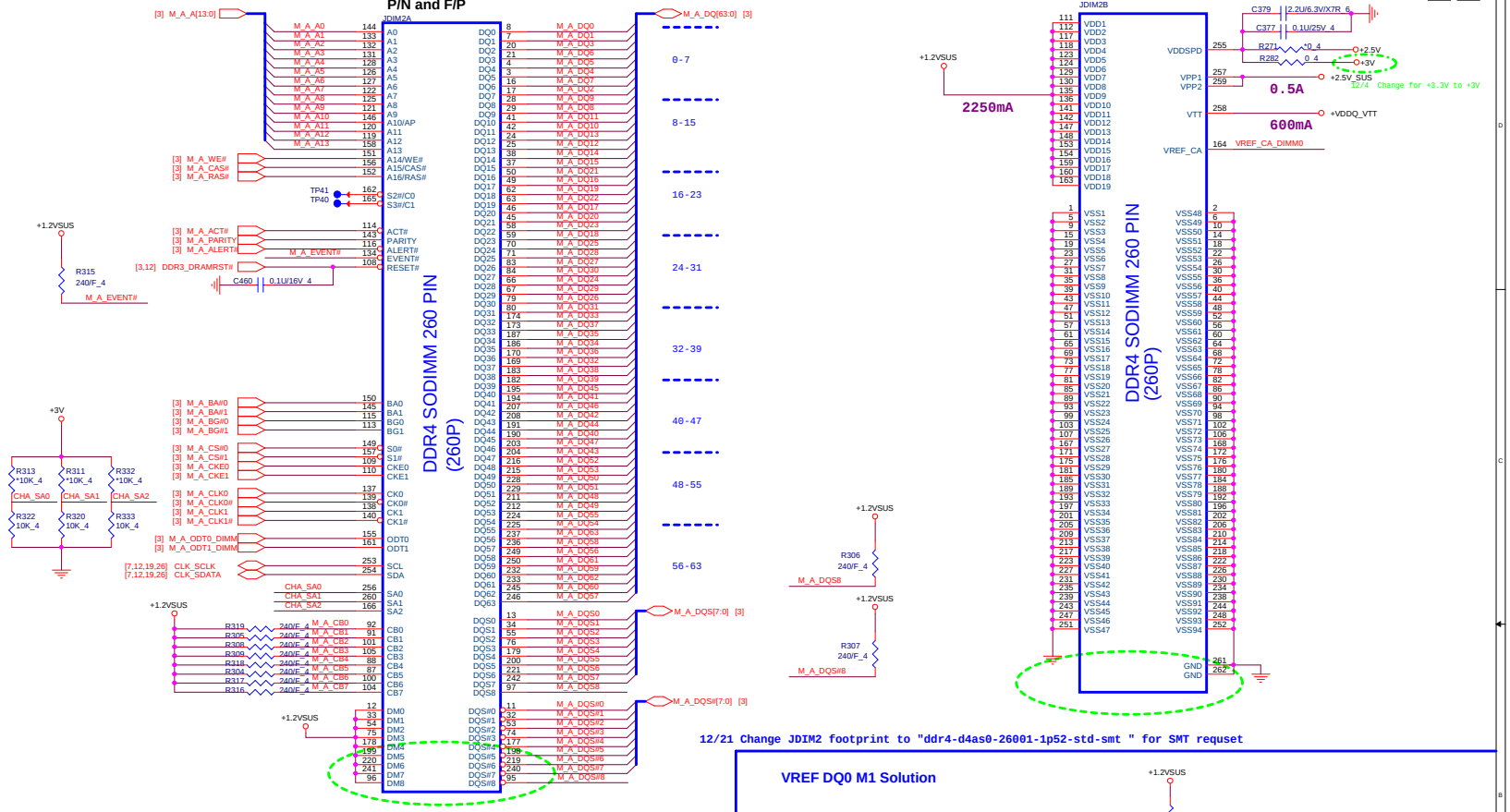
Reserve 1uF no stuff in CPU U11,U12 ball support Cannonlake-U PCH

For KBL R U42
(i)Non-stuff on KBL-U

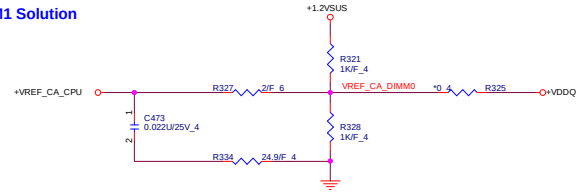


Quanta Computer Inc.		
PROJECT : Z8VR		
Size	Document Number: Skylake 10/17/18 (GND)	Rev: 1A
Date: Thursday, June 22, 2017	Sheet 10 of 46	

P/N and F/P

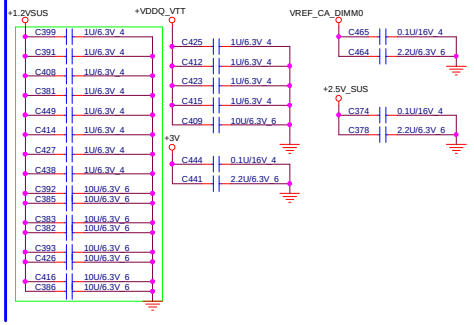


VREF DQ0 M1 Solution



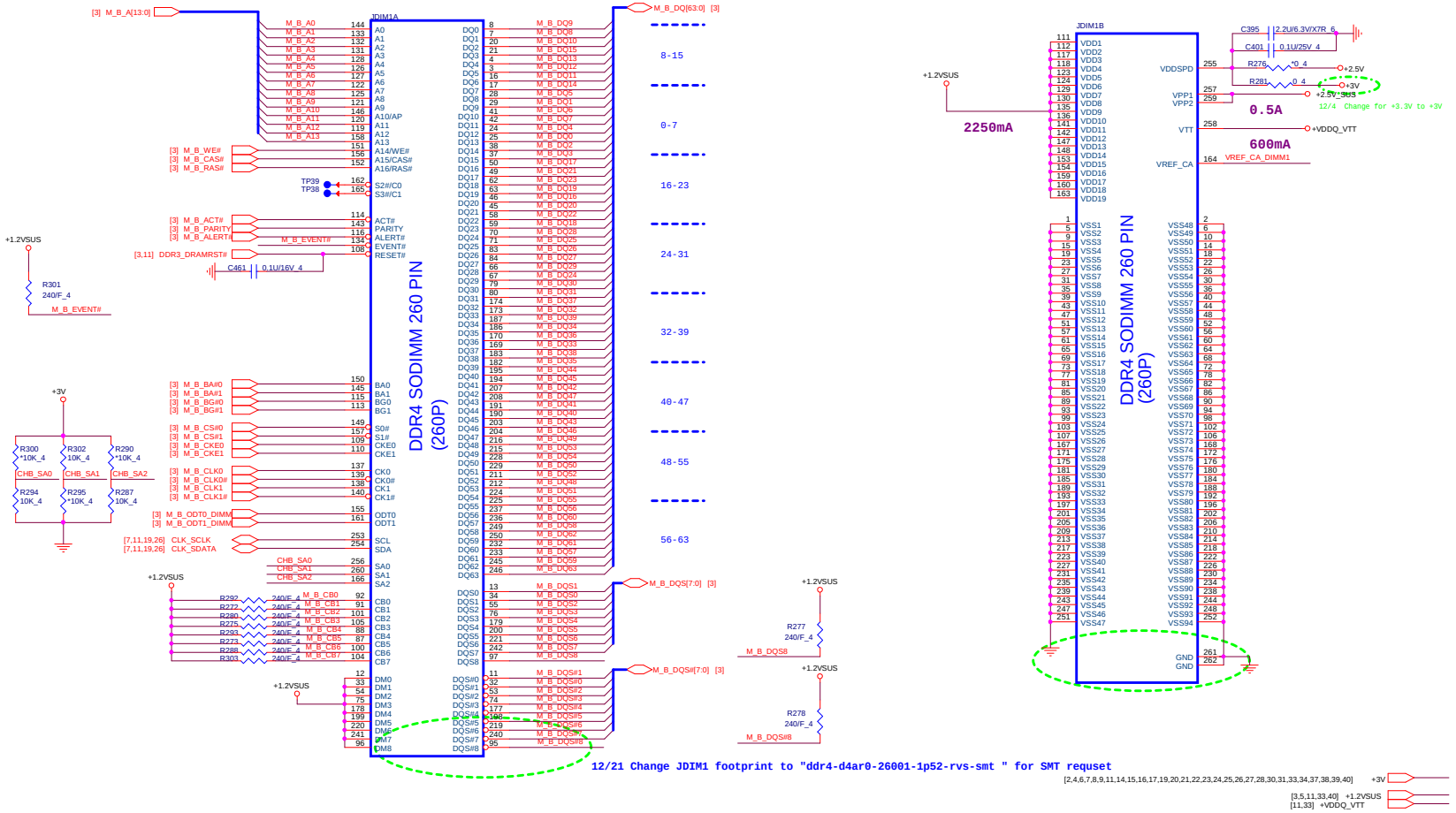
Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector

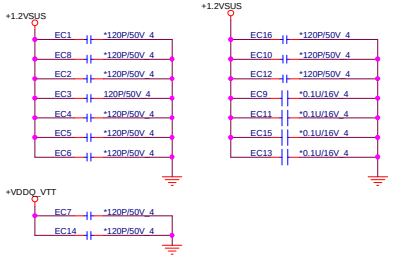


[3,5,12,33,40] +1.2VSUS
[12,33] +VDDQ_VTT
[2,4,6,7,8,9,12,14,15,16,17,19,20,21,22,23,24,25,26,27,28,30,31,33,34,37,38,39,40] +3V

Quanta Computer Inc. PROJECT : Z8VR		
Size	Document Number: DDR4 DIMM-RVS(5.2H) CHA	Rev 1A
Date: Thursday, June 22, 2017	Sheet 11 of 46	

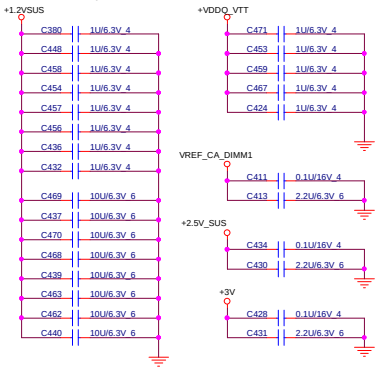


For EMI RESERVE

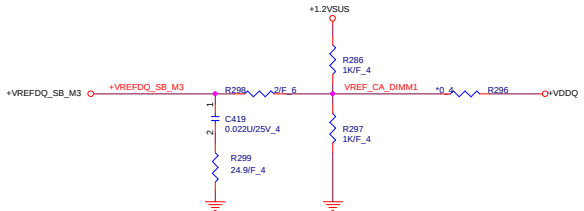


Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector



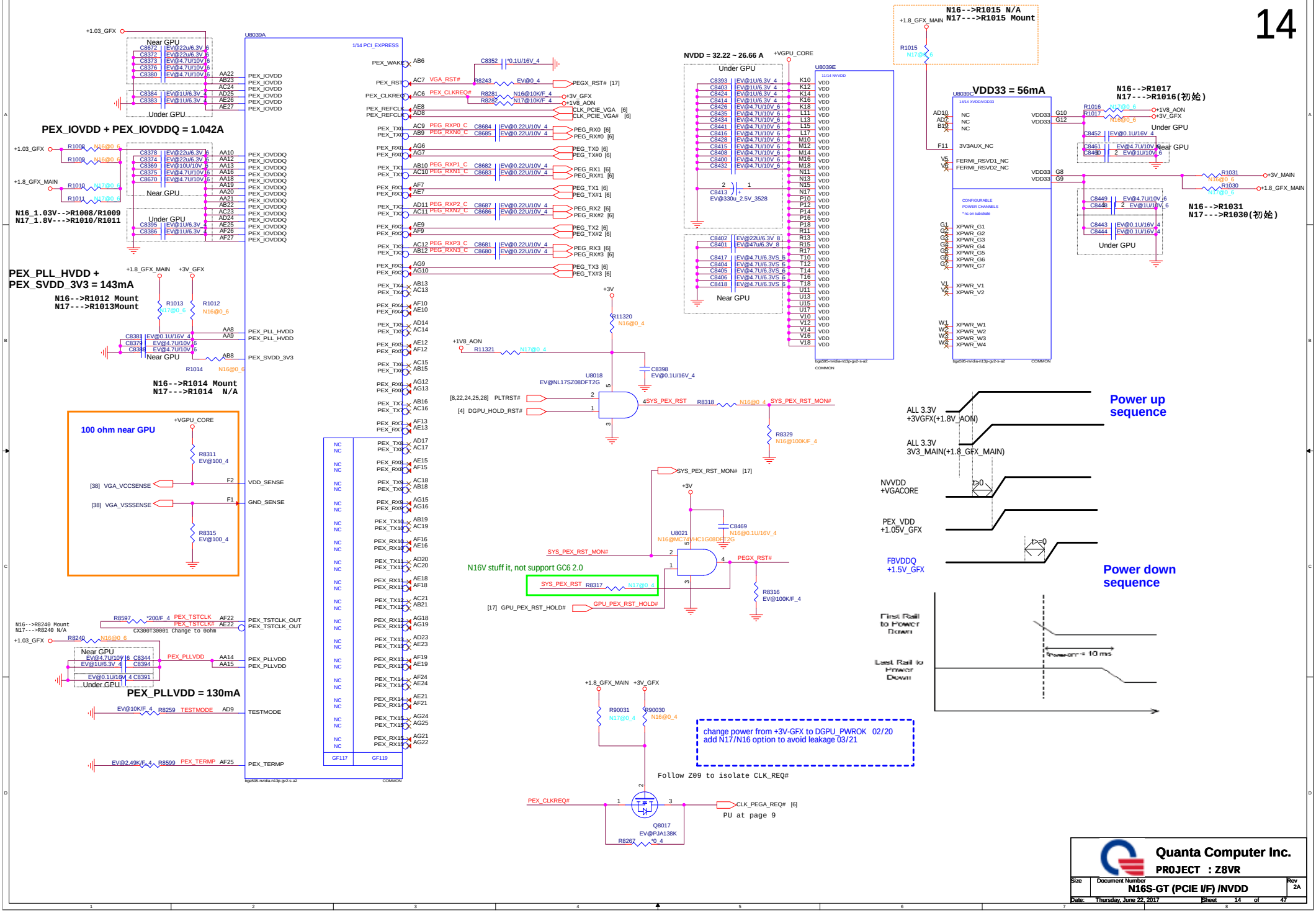
VREF DQ1 M1 Solution

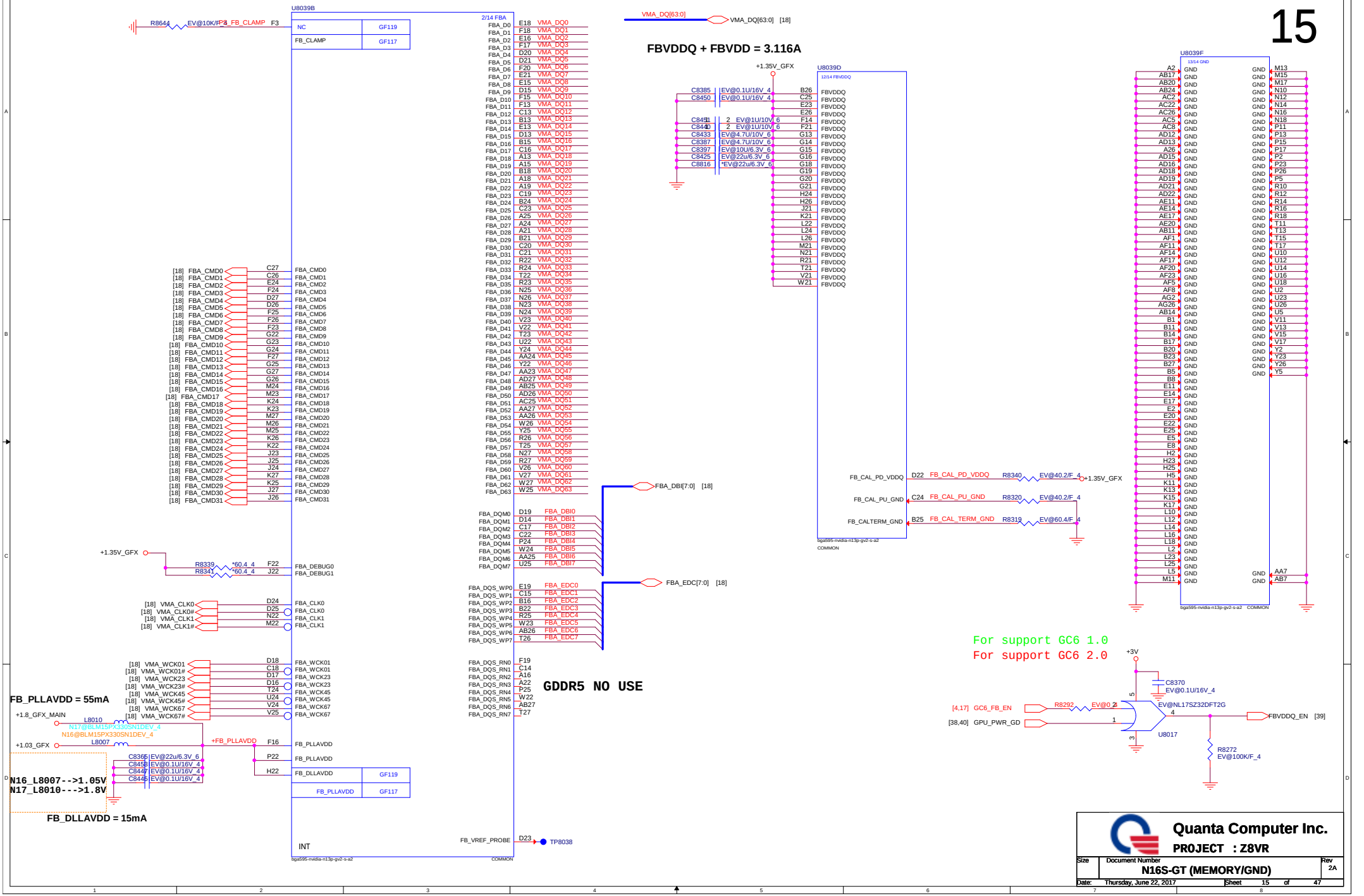


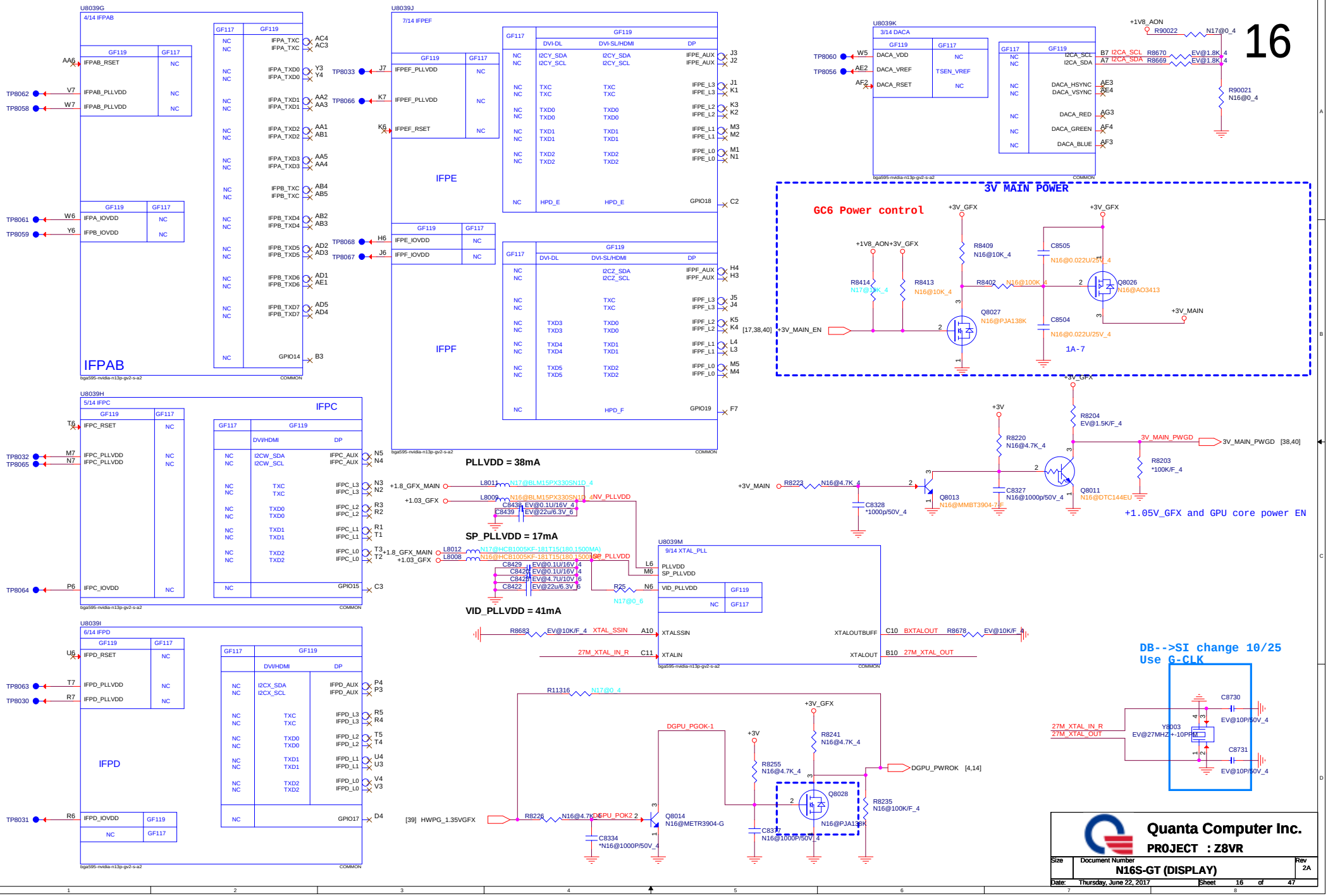
Quanta Computer Inc.

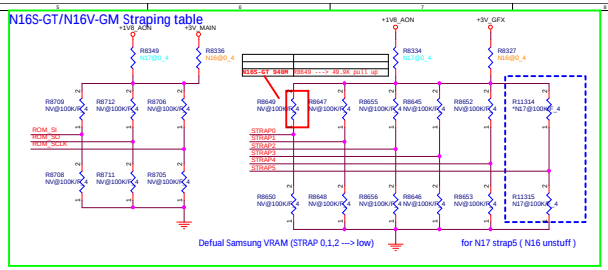
PROJECT : Z8VR

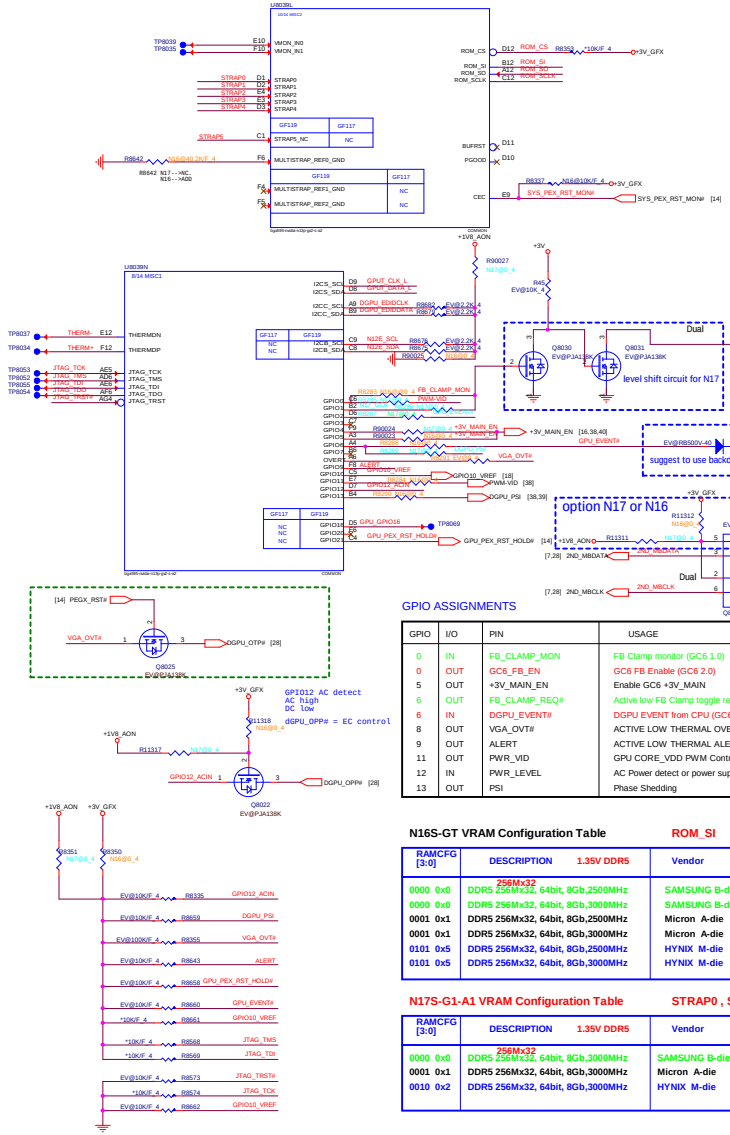
Size	Document Number	Rev
	DDR4 DIMM-STD(5.2H) CHB	1A
Date: Thursday, June 22, 2017	Sheet 12 of 46	


PEX_IOVDD + PEX_IOVDDQ = 1.042A
N16_1.03V-->R1008/R1009
N17_1.8V--->R1010/R1011
PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA
N16-->R1012 Mount
N17--->R1013Mount
N16-->R1014 Mount
N17--->R1014 N/A
100 ohm near GPU
PEX_PLLVDD = 130mA
N16-->R1015 N/A
N17--->R1015 Mount
VDD33 = 56mA
N16-->R1017
N17--->R1016(初始)
N16-->R1031
N17--->R1030(初始)
NVDD = 32.22 ~ 26.66 A
N16V stuff it, not support GC6 2.0
change power from +3V-GFX to DGPU_PWROK 02/20
add N17/N16 option to avoid leakage 03/21
Follow Z09 to isolate CLK_REQ#
PU at page 9
Power up sequence
Power down sequence
ALL 3.3V
+3VGFX(+1.8V_AON)
ALL 3.3V
3V3_MAIN(+1.8_GFX_MAIN)
NVVDD
+VGACORE
PEX_VDD
+1.05V_GFX
FBVDDQ
+1.5V_GFX
First Rail to Power Down
Last Rail to Power Down
Tpower-off <= 10 ms
Quanta Computer Inc.
PROJECT : Z8VR
N16S-GT (PCIE I/F) /NVDD
Thursday, June 22, 2017


15
U8039B
R8644 EV@10K/F_4 FB_CLAMP F3
NC GF119
FB_CLAMP GF117
2/14 FBA
FBA_D0 E18 VMA_DQ0
FBA_D1 F18 VMA_DQ1
FBA_D2 E16 VMA_DQ2
FBA_D3 F17 VMA_DQ3
FBA_D4 D20 VMA_DQ4
FBA_D5 D21 VMA_DQ5
FBA_D6 F20 VMA_DQ6
FBA_D7 E21 VMA_DQ7
FBA_D8 E15 VMA_DQ8
FBA_D9 D15 VMA_DQ9
FBA_D10 F15 VMA_DQ10
FBA_D11 F13 VMA_DQ11
FBA_D12 C13 VMA_DQ12
FBA_D13 B13 VMA_DQ13
FBA_D14 E13 VMA_DQ14
FBA_D15 D13 VMA_DQ15
FBA_D16 B15 VMA_DQ16
FBA_D17 C16 VMA_DQ17
FBA_D18 A13 VMA_DQ18
FBA_D19 A15 VMA_DQ19
FBA_D20 B18 VMA_DQ20
FBA_D21 A18 VMA_DQ21
FBA_D22 A19 VMA_DQ22
FBA_D23 C19 VMA_DQ23
FBA_D24 B24 VMA_DQ24
FBA_D25 C23 VMA_DQ25
FBA_D26 A25 VMA_DQ26
FBA_D27 A24 VMA_DQ27
FBA_D28 A21 VMA_DQ28
FBA_D29 B21 VMA_DQ29
FBA_D30 C20 VMA_DQ30
FBA_D31 C21 VMA_DQ31
FBA_D32 R22 VMA_DQ32
FBA_D33 R24 VMA_DQ33
FBA_D34 T22 VMA_DQ34
FBA_D35 R23 VMA_DQ35
FBA_D36 N25 VMA_DQ36
FBA_D37 N26 VMA_DQ37
FBA_D38 N23 VMA_DQ38
FBA_D39 N24 VMA_DQ39
FBA_D40 V23 VMA_DQ40
FBA_D41 V22 VMA_DQ41
FBA_D42 T23 VMA_DQ42
FBA_D43 U22 VMA_DQ43
FBA_D44 Y24 VMA_DQ44
FBA_D45 AA24 VMA_DQ45
FBA_D46 Y22 VMA_DQ46
FBA_D47 AA23 VMA_DQ47
FBA_D48 AD27 VMA_DQ48
FBA_D49 AB25 VMA_DQ49
FBA_D50 AD26 VMA_DQ50
FBA_D51 AC25 VMA_DQ51
FBA_D52 AA27 VMA_DQ52
FBA_D53 AA26 VMA_DQ53
FBA_D54 W26 VMA_DQ54
FBA_D55 Y25 VMA_DQ55
FBA_D56 R26 VMA_DQ56
FBA_D57 T25 VMA_DQ57
FBA_D58 N27 VMA_DQ58
FBA_D59 R27 VMA_DQ59
FBA_D60 V26 VMA_DQ60
FBA_D61 V27 VMA_DQ61
FBA_D62 W27 VMA_DQ62
FBA_D63 W25 VMA_DQ63
[18] FBA_CMD0 C27 FBA_CMD0
[18] FBA_CMD1 C26 FBA_CMD1
[18] FBA_CMD2 E24 FBA_CMD2
[18] FBA_CMD3 F24 FBA_CMD3
[18] FBA_CMD4 D27 FBA_CMD4
[18] FBA_CMD5 D26 FBA_CMD5
[18] FBA_CMD6 F25 FBA_CMD6
[18] FBA_CMD7 F26 FBA_CMD7
[18] FBA_CMD8 F23 FBA_CMD8
[18] FBA_CMD9 G22 FBA_CMD9
[18] FBA_CMD10 G23 FBA_CMD10
[18] FBA_CMD11 G24 FBA_CMD11
[18] FBA_CMD12 F27 FBA_CMD12
[18] FBA_CMD13 G25 FBA_CMD13
[18] FBA_CMD14 G27 FBA_CMD14
[18] FBA_CMD15 G26 FBA_CMD15
[18] FBA_CMD16 M24 FBA_CMD16
[18] FBA_CMD17 M23 FBA_CMD17
[18] FBA_CMD18 K24 FBA_CMD18
[18] FBA_CMD19 K23 FBA_CMD19
[18] FBA_CMD20 M27 FBA_CMD20
[18] FBA_CMD21 M26 FBA_CMD21
[18] FBA_CMD22 M25 FBA_CMD22
[18] FBA_CMD23 K26 FBA_CMD23
[18] FBA_CMD24 K22 FBA_CMD24
[18] FBA_CMD25 J23 FBA_CMD25
[18] FBA_CMD26 J25 FBA_CMD26
[18] FBA_CMD27 J24 FBA_CMD27
[18] FBA_CMD28 K27 FBA_CMD28
[18] FBA_CMD29 K25 FBA_CMD29
[18] FBA_CMD30 J27 FBA_CMD30
[18] FBA_CMD31 J26 FBA_CMD31
+1.35V_GFX
R8339 *60.4_4 F22 FBA_DEBUG0
R8341 *60.4_4 J22 FBA_DEBUG1
[18] VMA_CLK0 D24 FBA_CLK0
[18] VMA_CLK0# D25 FBA_CLK0
[18] VMA_CLK1 N22 FBA_CLK1
[18] VMA_CLK1# M22 FBA_CLK1
[18] VMA_WCK01 D18 FBA_WCK01
[18] VMA_WCK01# C18 FBA_WCK01
[18] VMA_WCK23 D17 FBA_WCK23
[18] VMA_WCK23# D16 FBA_WCK23
[18] VMA_WCK45 T24 FBA_WCK45
[18] VMA_WCK45# U24 FBA_WCK45
[18] VMA_WCK67 V24 FBA_WCK67
[18] VMA_WCK67# V25 FBA_WCK67
FB_PLLAVDD = 55mA
+1.8_GFX_MAIN
L8010
N17@BLM15PX330SN1DEV_4
N16@BLM15PX330SN1DEV_4
+1.03_GFX
L8007
+FB_PLLAVDD F16 FB_PLLAVDD
P22 FB_PLLAVDD
H22
C8365 EV@22u/6.3V_6
C8458 EV@0.1U/16V_4
C8447 EV@0.1U/16V_4
C8445 EV@0.1U/16V_4
N16_L8007-->1.05V
N17_L8010--->1.8V
FB_DLLAVDD = 15mA
FB_DLLAVDD GF119
FB_PLLAVDD GF117
INT
bga595-nvidia-n13p-gv2-s-a2 COMMON
FBA_DBI[7:0] [18]
FBA_DQM0 D19 FBA_DBI0
FBA_DQM1 D14 FBA_DBI1
FBA_DQM2 C17 FBA_DBI2
FBA_DQM3 C22 FBA_DBI3
FBA_DQM4 P24 FBA_DBI4
FBA_DQM5 W24 FBA_DBI5
FBA_DQM6 AA25 FBA_DBI6
FBA_DQM7 U25 FBA_DBI7
FBA_EDC[7:0] [18]
FBA_DQS_WP0 E19 FBA_EDC0
FBA_DQS_WP1 C15 FBA_EDC1
FBA_DQS_WP2 B16 FBA_EDC2
FBA_DQS_WP3 B22 FBA_EDC3
FBA_DQS_WP4 R25 FBA_EDC4
FBA_DQS_WP5 W23 FBA_EDC5
FBA_DQS_WP6 AB26 FBA_EDC6
FBA_DQS_WP7 T26 FBA_EDC7
FBA_DQS_RN0 F19
FBA_DQS_RN1 C14
FBA_DQS_RN2 A16
FBA_DQS_RN3 A22
FBA_DQS_RN4 P25
FBA_DQS_RN5 W22
FBA_DQS_RN6 AB27
FBA_DQS_RN7 T27
GDDR5 NO USE
FB_VREF_PROBE D23 TP8038
VMA_DQ[63:0]
VMA_DQ[63:0] [18]
FBVDDQ + FBVDD = 3.116A
+1.35V_GFX
C8385 EV@0.1U/16V_4
C8450 EV@0.1U/16V_4
C8451 2 EV@1U/10V_6
C8440 2 EV@1U/10V_6
C8433 EV@4.7U/10V_6
C8387 EV@4.7U/10V_6
C8397 EV@10U/6.3V_6
C8425 EV@22u/6.3V_6
C8816 *EV@22u/6.3V_6
U8039D
12/14 FBVDDQ
B26 C25 E23 E26 F14 F21 G13 G14 G15 G16 G18 G19 G20 G21 H24 H26 J21 K21 L22 L24 L26 M21 N21 R21 T21 V21 W21 FBVDDQ
FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R8340 EV@40.2/F_4 +1.35V_GFX
FB_CAL_PU_GND C24 FB_CAL_PU_GND R8320 EV@40.2/F_4
FB_CALTERM_GND B25 FB_CAL_TERM_GND R8319 EV@60.4/F_4
bga595-nvidia-n13p-gv2-s-a2 COMMON
U8039F
13/14 GND
A2 AB17 AB20 AB24 AC2 AC22 AC26 AC5 AC8 AD12 AD13 A26 AD15 AD16 AD18 AD19 AD21 AD22 AE11 AE14 AE17 AE20 AB11 AF1 AF11 AF14 AF17 AF20 AF23 AF5 AF8 AG2 AG26 AB14 B1 B11 B14 B17 B20 B23 B27 B5 B8 E11 E14 E17 E2 E20 E22 E25 E5 E8 H2 H23 H25 H5 K11 K13 K15 K17 L10 L12 L14 L16 L18 L2 L23 L25 L5 M11 GND
M13 M15 M17 N10 N12 N14 N16 N18 P11 P13 P15 P17 P2 P23 P26 P5 R10 R12 R14 R16 R18 T11 T13 T15 T17 U10 U12 U14 U16 U18 U2 U23 U26 U5 V11 V13 V15 V17 Y2 Y23 Y26 Y5 GND
AA7 AB7 GND
bga595-nvidia-n13p-gv2-s-a2 COMMON
For support GC6 1.0
For support GC6 2.0
+3V
C8370 EV@0.1U/16V_4
[4,17] GC6_FB_EN
R8292 EV@0
[38,40] GPU_PWR_GD
U8017
EV@NL17SZ32DFT2G
FBVDDQ_EN [39]
R8272 EV@100K/F_4
Quanta Computer Inc.
PROJECT : Z8VR
Size
Document Number
N16S-GT (MEMORY/GND)
Rev 2A
Date: Thursday, June 22, 2017
Sheet 15 of 47


16
U8039G
4/14 IFPAB
IFPAB
U8039J
7/14 IFPEF
IFPE
IFPF
U8039K
3/14 DACA
U8039H
5/14 IFPC
IFPC
U8039I
6/14 IFPD
IFPD
U8039M
9/14 XTAL_PLL
3V MAIN POWER
GC6 Power control
1A-7
PLLVDD = 38mA
SP_PLLVDD = 17mA
VID_PLLVDD = 41mA
+1.05V_GFX and GPU core power EN
DB-->SI change 10/25
Use G-CLK
Quanta Computer Inc.
PROJECT : Z8VR
N16S-GT (DISPLAY)
Thursday, June 22, 2017
Sheet 16 of 47





N16S-GT DID=0x1347 [940M]

ROM_SCLK	=	Stuff 4.99K pull down
ROM_SO	=	Stuff 4.99K pull down
STRAP0	=	Stuff 49.9K pull up
STRAP1	=	NC
STRAP2	=	NC
STRAP3	=	NC
STRAP4	=	NC
ROM_SI	=	VRAM Configuration follow below table

N17S-G1-A1 DID=0x1D10 [1040]

ROM_SI	=	Stuff 100K pull up
ROM_SO	=	Stuff 100K pull up
ROM_SCLK	=	Stuff 100K pull up and Stuff 100K pull down
STRAP0	=	VRAM Configuration follow below table
STRAP1	=	VRAM Configuration follow below table
STRAP2	=	VRAM Configuration follow below table
STRAP3	=	Stuff 100K pull down
STRAP4	=	Stuff 100K pull down
STRAP5	=	Stuff 100K pull down

Note: GC6 2.0 is supported by N16x GPU in the GB2B ,GB4B-128,and GB3B-256 packages.

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor (GC6 1.0)
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	OUT	FB_CLAMP_REQ#	Active low FB Clamp toggle request (GC6 1.0)
6	IN	DGPU_EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVT#	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

N16S-GT/N16V-GM Straping table

ROM_SI N16S-GT [940M]		
2G Hynix 128Mx16	-->	34.8K PD
2G Micron 128Mx16	-->	45.3K PD
2G Samsumg 128Mx16	-->	4.99K PU
4G Hynix 256Mx16	-->	30.1K PU Single Rank
4G Hynix 256Mx16	-->	24.9K PU Dual Rank
4G Micron 256Mx16	-->	10K PD
4G Samsumg 256Mx16	-->	15K PD

ROM_SO
N16S-GT --> 4.99K PD

ROM_SCLK
N16S-GT --> 4.99K PD

STRAP0
N16S-GT --> 49.9K PU

Resistor P/N

4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K --->CS32492FB16
30.1K --->CS33012FB18
34.8K---> CS33482FB22
45.3K ---> CS34532FB18
49.9K ---> CS34992FB10

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

N16S-GTR-S-A2 PN : AJ0N16S0T44

N17S-G1-A1 PN : AJ0N17S0T00

N16S-GT VRAM Configuration Table ROM_SI

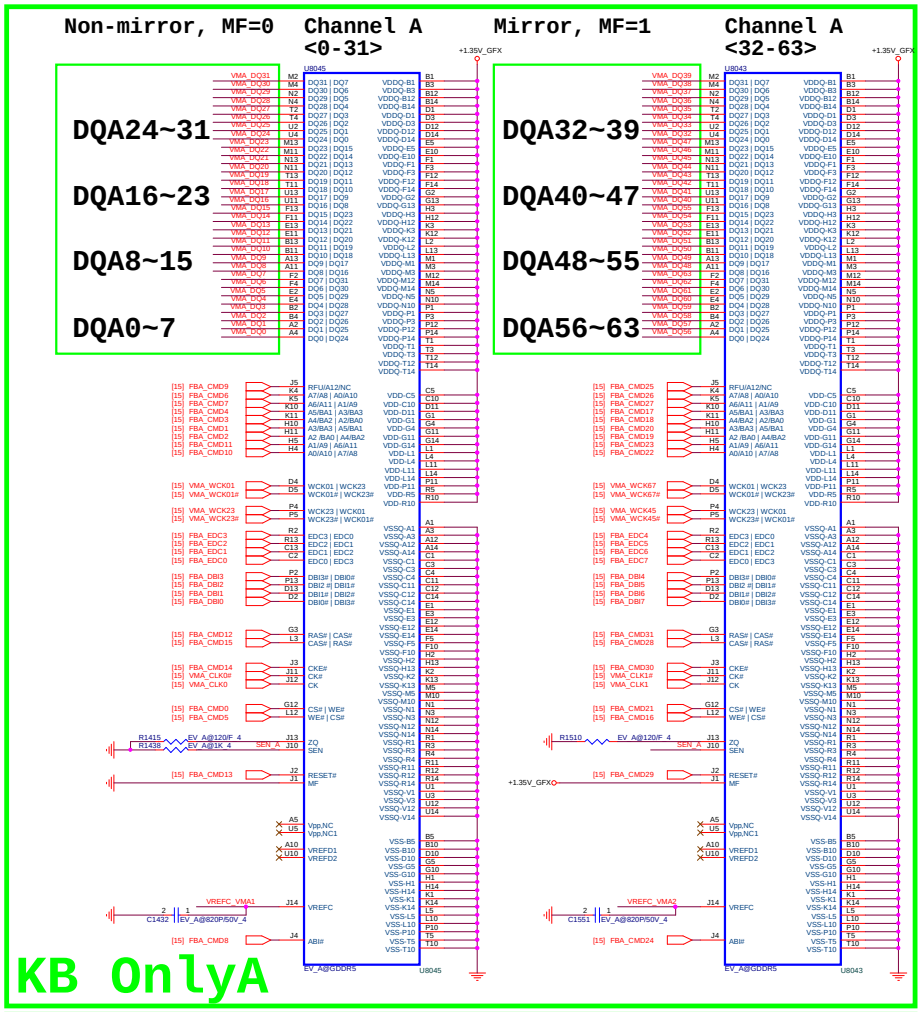
RAMCFG [3:0]	DESCRIPTION 1.35V DDR5	Vendor	Vendor P/N	ROM_SI	STN B/S	
0000 0x0	DDR5 256Mx32, 64bit, 8Gb,2500MHz	SAMSUNG B-die	K4G80325FB-HC03	PD 4.99K ohm	AKG5QGDT502	
0000 0x0	DDR5 256Mx32, 64bit, 8Gb,3000MHz	SAMSUNG B-die	K4G80325FB-HC28	PD 4.99K ohm	AKG5QGDT518	
0001 0x1	DDR5 256Mx32, 64bit, 8Gb,2500MHz	Micron A-die	MT51J256M32HF-60:A	PD 10K ohm	AKG5LGUTL04	
0001 0x1	DDR5 256Mx32, 64bit, 8Gb,3000MHz	Micron A-die	MT51J256M32HF-70:A	PD 10K ohm	AKG5QGUTL15	
0101 0x5	DDR5 256Mx32, 64bit, 8Gb,2500MHz	HYNIX M-die	H5GC8H24MJR-T2C	PD 30.1K ohm	AKG5QFUTW04	
0101 0x5	DDR5 256Mx32, 64bit, 8Gb,3000MHz	HYNIX M-die	H5GC8H24MJR-R0C	PD 30.1K ohm	AKG5QGUTW06	

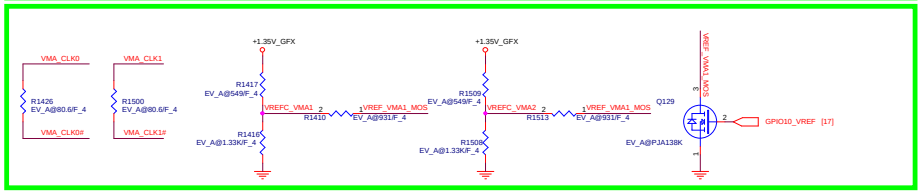
N17S-G1-A1 VRAM Configuration Table STRAP0 , STRAP1 , STRAP2

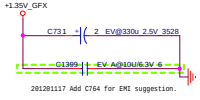
RAMCFG [3:0]	DESCRIPTION 1.35V DDR5	Vendor	Vendor P/N	STRAP0	STRAP1	STRAP2	STN B/S	
0000 0x0	DDR5 256Mx32, 64bit, 8Gb,3000MHz	SAMSUNG B-die	K4G80325FB-HC28	PD 100K ohm	PD 100K ohm	PD 100K ohm	AKG5QGDT518	
0001 0x1	DDR5 256Mx32, 64bit, 8Gb,3000MHz	Micron A-die	MT51J256M32HF-70:A	PU 100K ohm	PD 100K ohm	PD 100K ohm	AKG5QGUTL15	
0010 0x2	DDR5 256Mx32, 64bit, 8Gb,3000MHz	HYNIX M-die	H5GC8H24MJR-R0C	PD 100K ohm	PU 100K ohm	PD 100K ohm	AKG5QGUTW06	

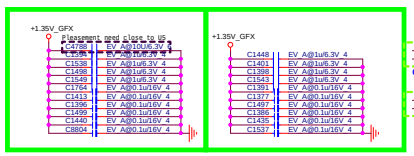
Quanta Computer Inc.
PROJECT : Z8VR
Size | Document Number: N16S-GT (GPIO/STRAPS) | Rev: 2A
Date: Thursday, June 22, 2017 | Sheet 17 of 47

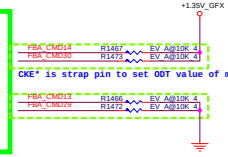
CHANNEL A: 1024MB GDDR5x32











RST PD place @ the end of daisy-chain.

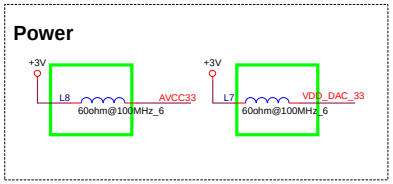
GDDR5 Mode H Mapping

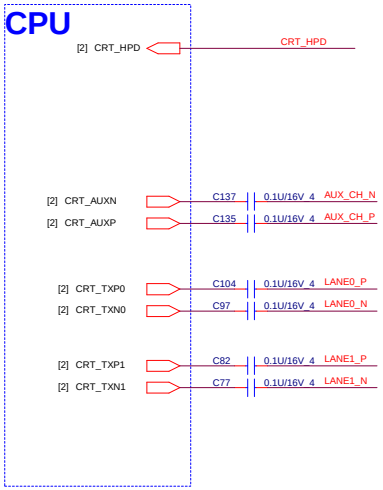
< 0-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A8_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

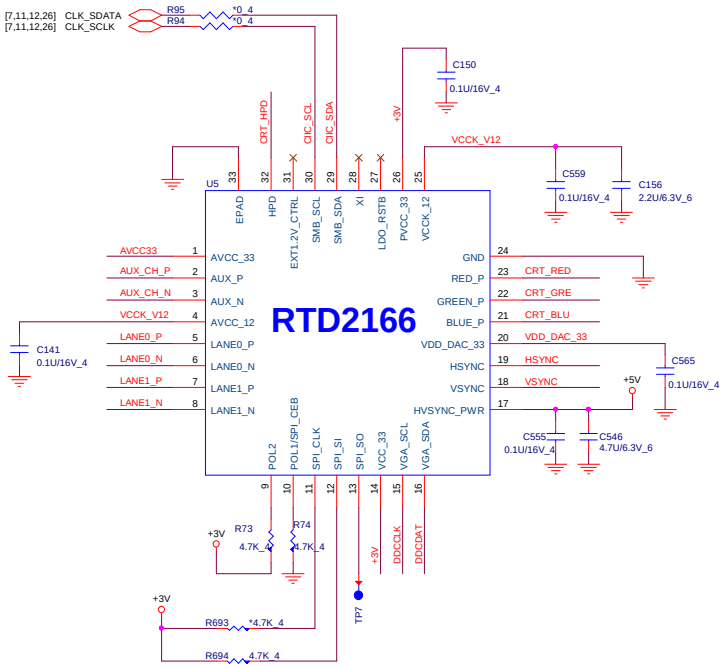
Quanta Computer Inc.
PROJECT : Z8VR

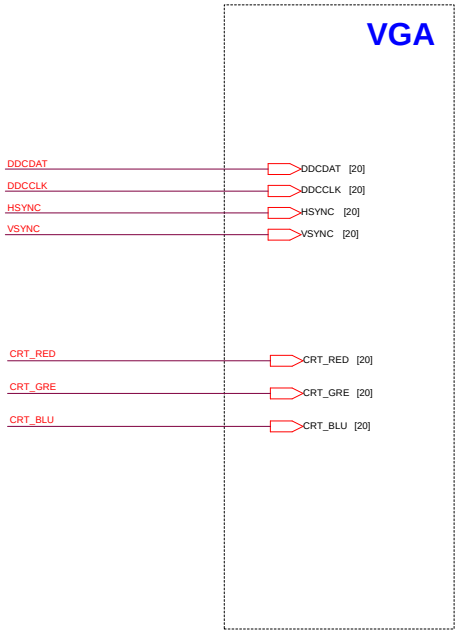
Size	Document Number	Rev
	N16x - 6/6 (GDDR5x32)	3A
Date: Thursday, June 22, 2017	Sheet 18 of 47	

DP TO VGA









Note:

1- C1,C3,C4,C5,C11,C16, C21 should be placed close to chip
2- C5 shold be X5R material
3- R6, R7, R8 should be 75 ohm with +/-1%
4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.
5- This configuration is for internal ROM mode and using embedded LDO mode.

[2,4,6,7,8,9,11,12,14,15,16,17,20,21,22,23,24,25,26,27,28,30,31,33,34,37,38,39,40] +3V
[20,21,23,24,26,30,37] +5V

Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	DP to VGA iT6165	1A
Date: Thursday, June 22, 2017	Sheet 19 of 46	

CRT

RTD2166 integrate 5V HSYNC/VSYNC buffer inside IC

12/24 Delete R449

12/18 Change R412 to 47ohm for vendor requset

12/24 Delete R396

12/18 Change R399 to 47ohm for vendor requset

Co-Layout

Realtek FAE suggest close to connector

Close to RTD2166 IC

12/18 Change to BLM15BB220SN1D (CX5BB220005) for vendor requset

12/18 Un-Stuff C95/C128/C148 for vendor requset

12/21 Change CN5 footprint to "dsub-95-0005-01-15p" for layout requset

Realtek FAE suggest close to connector

12/18 Un-Stuff C539/C551 for vendor requset

Power trace tracking

LCD CONNECTOR

ESD

2013/12/12 change eDP pin define
colayout FHD Panel for A2 stage

MAX 1.5A

eDP FHD

Touch Panel-I2C

Touch Panel-USB

eDP 4k*2k

CCD-USB

Prevent ESD/EOS Layout near device

1C1-2 2014/03/11 Add R698 for TS_EN short TP_INT, for issue debug.

Touch Panel interrupt

LCD Power

1st : AL005245000---GMT
2nd : AL007553000---UPI

Touch screen level shift I2C(reserve)

S5

S0

TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.

LID591#,EC intrnal PU

1B-3 2013/12/10 change Q3.3 from +3V to +3VPCU.

Hall Sensor (HSR)

1st:AL009249000 -- BCD
2nd:AL009132001 -- ANC

Quanta Computer Inc.	
PROJECT : Z8VR	
Size	Document Number: CRT/LVDS/CAMERA/LID — Rev 1A
Date: Thursday, June 22, 2017	Sheet 20 of 46

HDMI

<HDM>

OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode: DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V_{DC}	2 dB
short to V_{DD}	short to GND	4 dB
short to V_{DD}	short to V_{DC}	6 dB

From PCH

U15 PTN3366BS

HDMI-detect

S5 input high

S0

Close connector

DDS AL002331000

HDMI connector

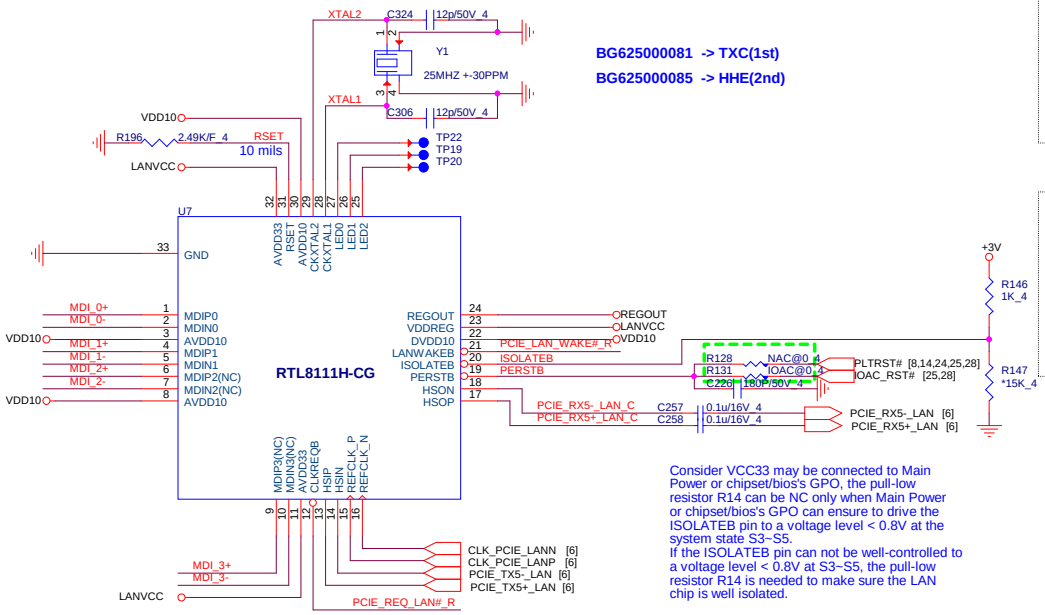
EMI

Power trace tracking

[2,4,6,7,8,9,11,12,14,15,16,17,19,20,22,23,24,25,26,27,28,30,31,33,34,37,38,39,40] +3V
[19,20,23,24,26,30,37] +5V

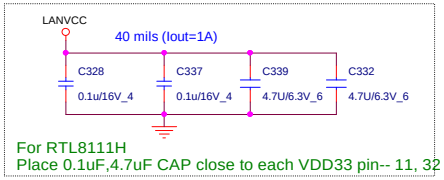
Quanta Computer Inc.
PROJECT : Z8VR
HDMI (PS8407 4k*2k)
Size | Document Number | Rev 1A
Date: Thursday, June 22, 2017 | Sheet 21 of 46

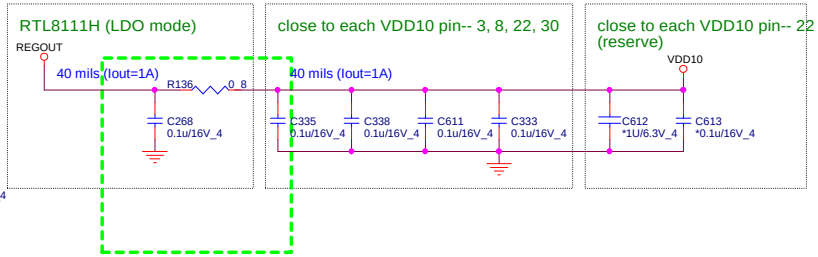
Giga LAN (LAN)



BG625000081 -> TXC(1st)

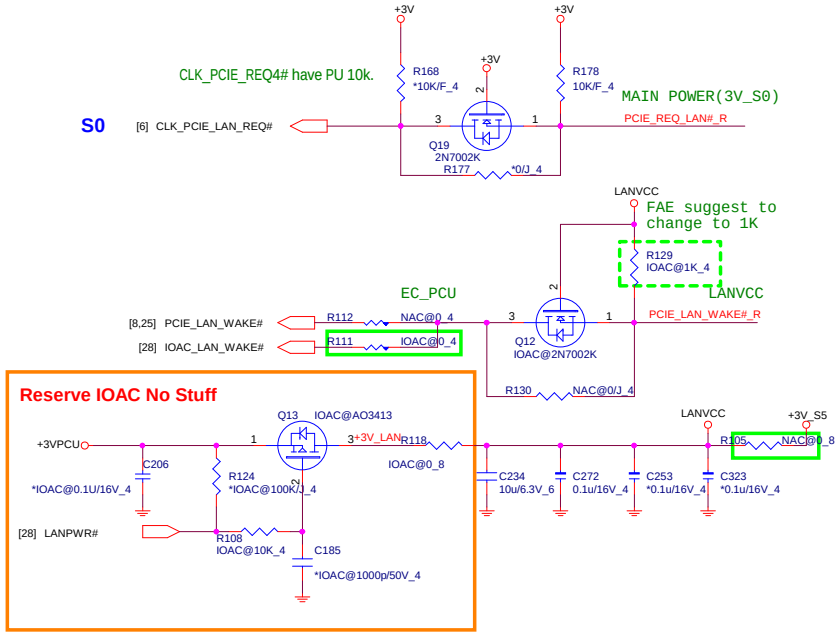
BG625000085 -> HHE(2nd)





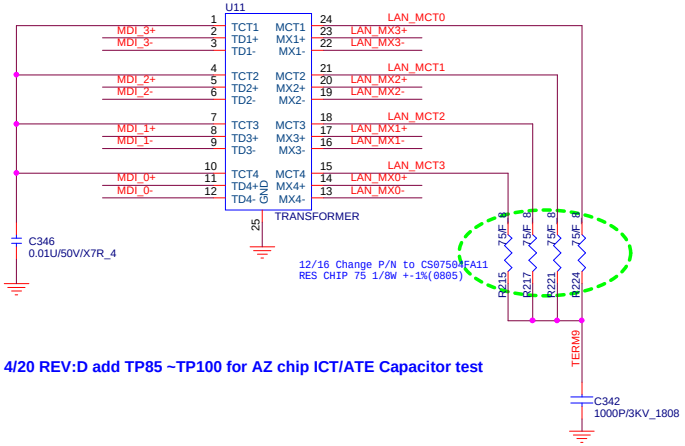
Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S3~S5.
If the ISOLATEB pin can not be well-controlled to a voltage level < 0.8V at S3~S5, the pull-low resistor R14 is needed to make sure the LAN chip is well isolated.

Leakage circuit (MPC)



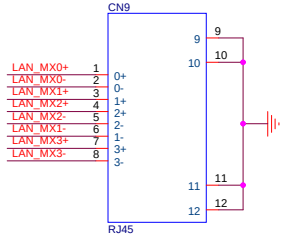
Tramsformer

Layout:All termination signal should have 30 mil trace



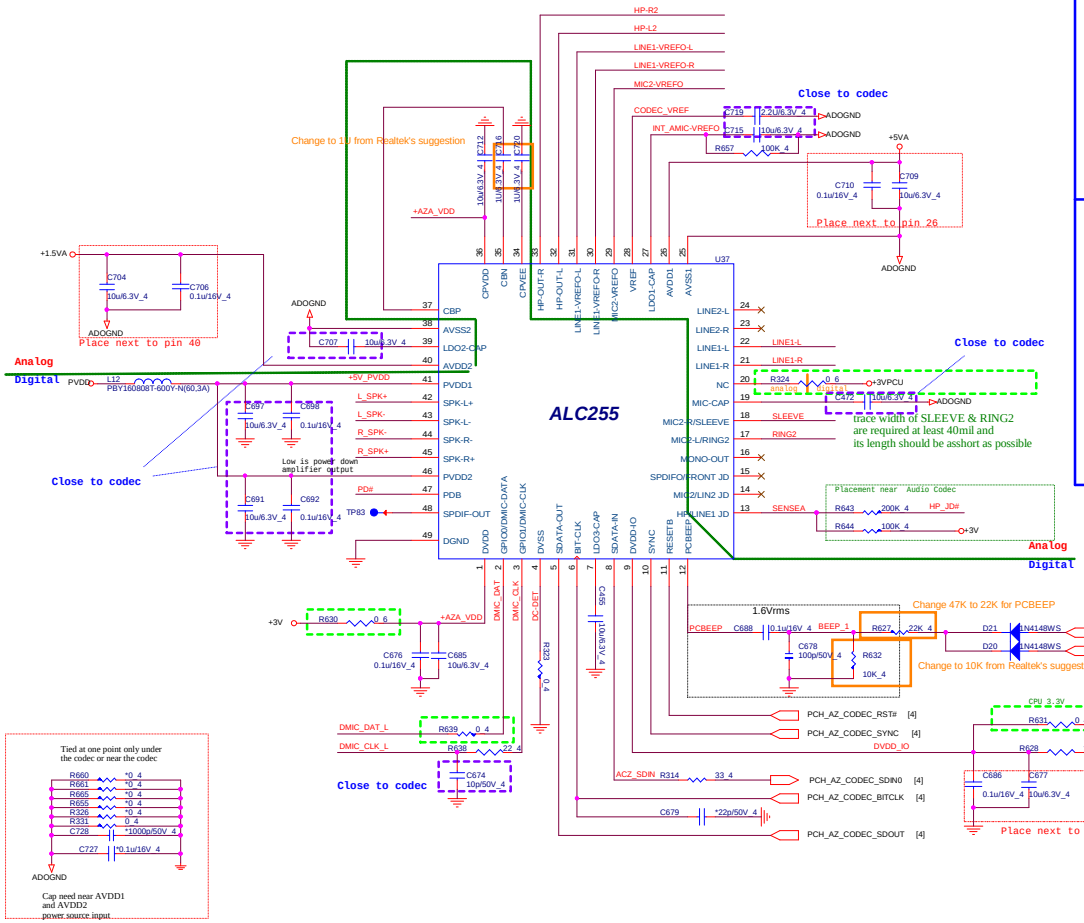
4/20 REV:D add TP85 ~TP100 for AZ chip ICT/ATE Capacitor test

RJ45 Connector



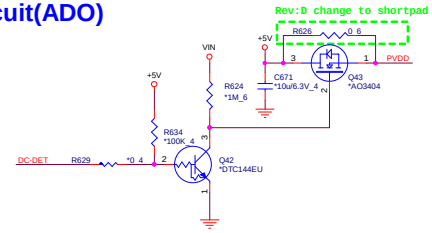
Quanta Computer Inc.		
PROJECT : Z8VR		
Size	Document Number: LAN(RTL8111H)	Rev: 1A
Date: Thursday, June 22, 2017	Sheet 22 of 46	

Codec(ADO)



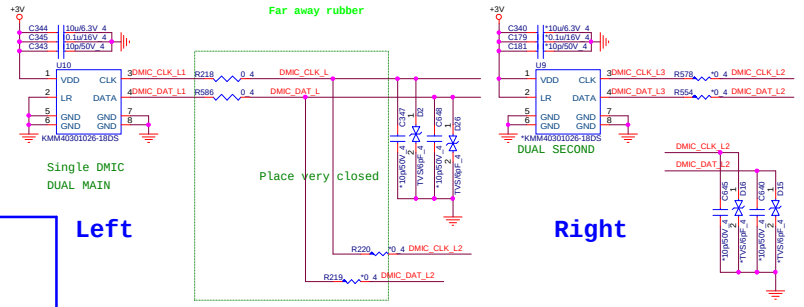
DC-DET circuit(ADO)

Rev:D change to shortpad



D-Mic (MIC)

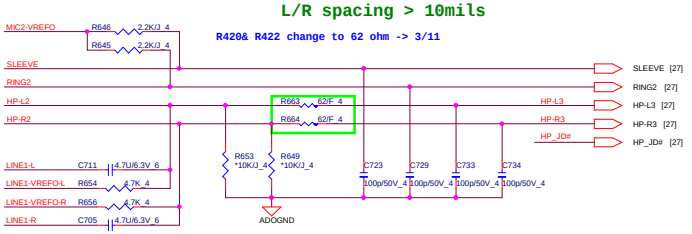
Single DMIC and Dual DIMC same PN: AL403010A00



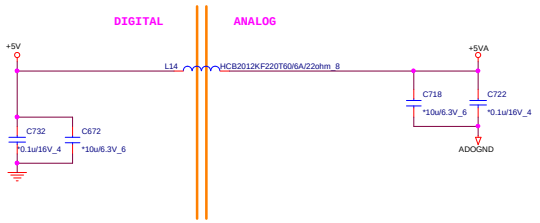
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)

SLEEVE/RING2 trace > 40mils
HP/LINE trace > 10mils
L/R spacing > 10mils

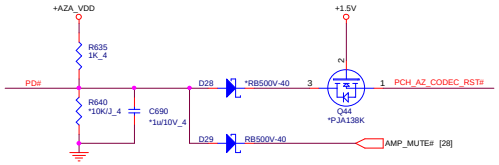
R420& R422 change to 62 ohm -> 3/11



Codec PWR 5V(ADO)



Mute(ADO)

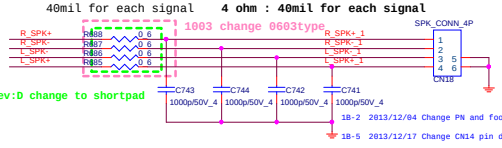


Internal Speaker

40mil for each signal **4 ohm : 40mil for each signal**

1003 change 0603type

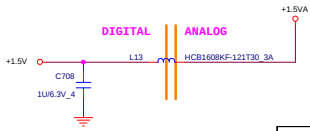
Rev:D change to shortpad



1B-2 2013/12/04 Change PN and footprint.

1B-5 2013/12/17 Change CN14 pin define

Codec PWR 1.5V(ADO)

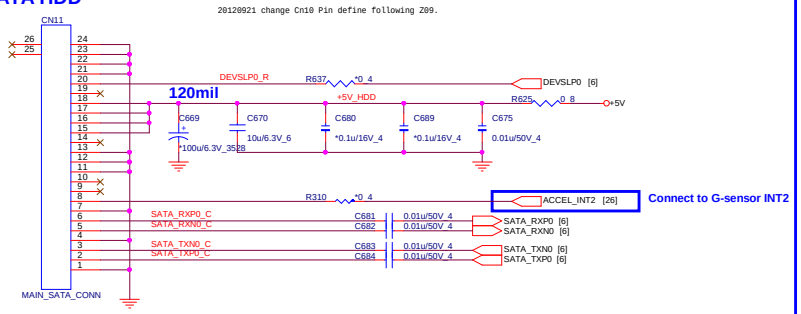


Quanta Computer Inc.

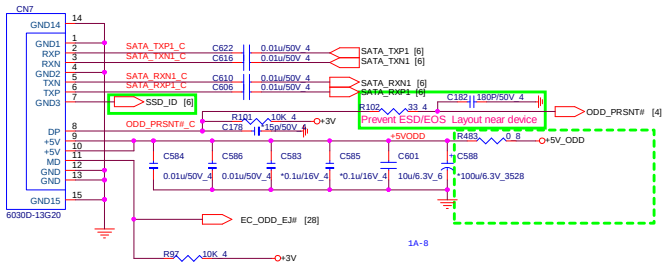
PROJECT : Z8VR

Size	Document Number	Rev
	ALC255/HP/SPK	1A
Date: Thursday, June 22, 2017	Sheet 23 of 46	

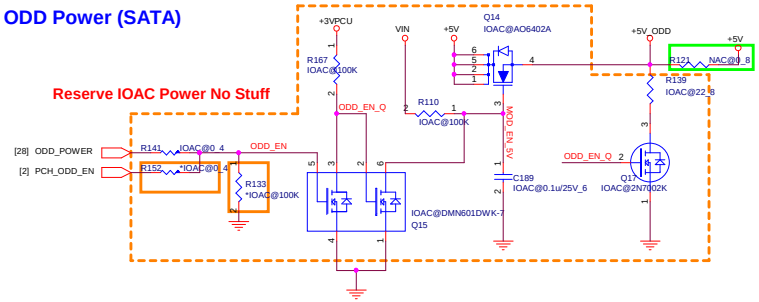
SATA HDD



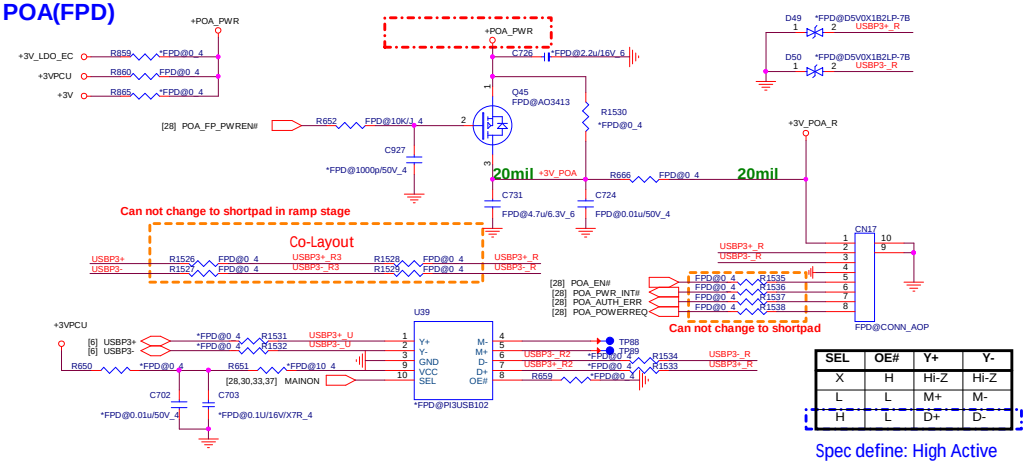
SATA ODD Connector



ODD Power (SATA)



POA(FPD)



SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

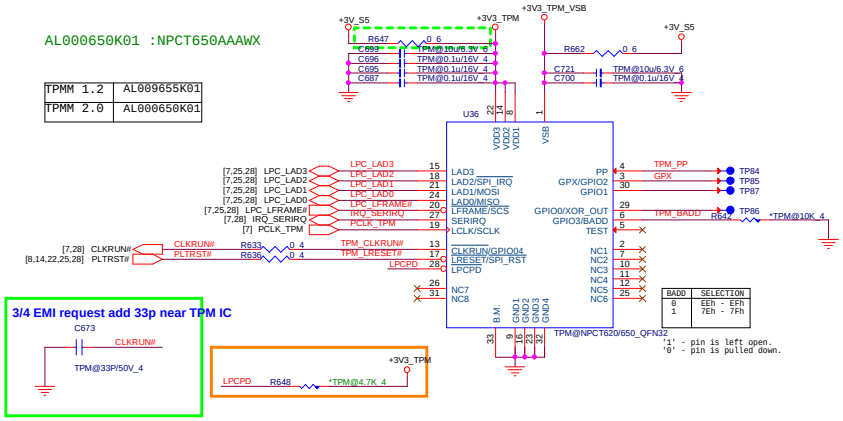
Spec define: High Active

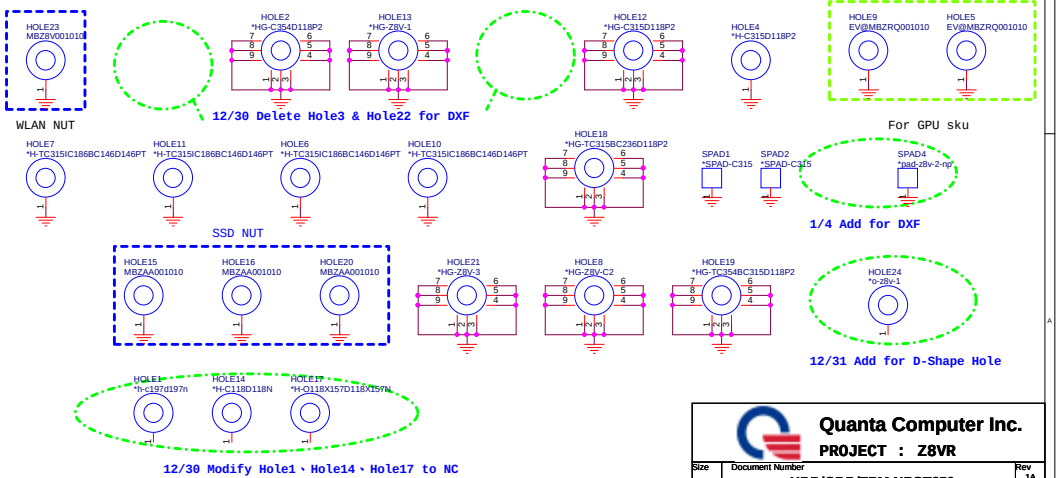
TPM NPCT650 (TPM)

SP@ BOM周邊上NPCT650
A,B,C P/N:AL009655K01(SLB9655TT1.2- FW4.31)
RAMP P/N: AL000650K01 (NPCT650AAAWX)

AL000650K01 :NPCT650AAAWX

TPMM 1.2	AL009655K01
TPMM 2.0	AL000650K01





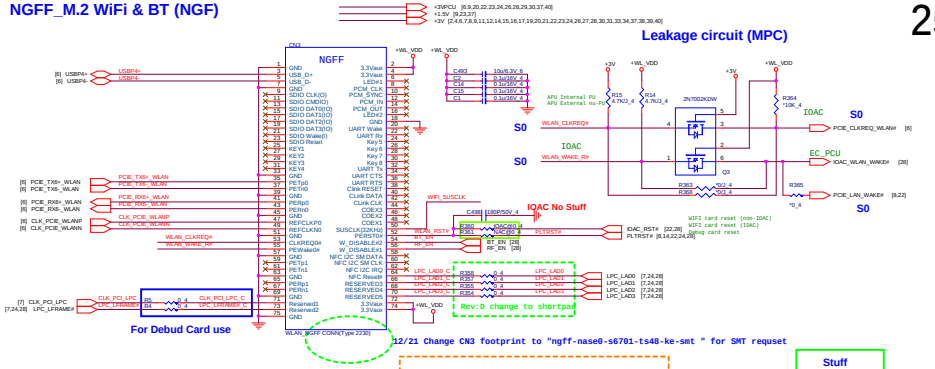
Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	HDD/ODD/TPM NPCT650	1A

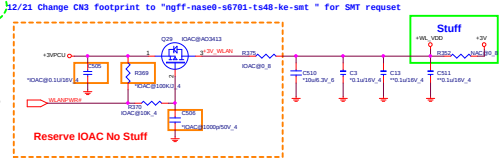
Date: Thursday, June 22, 2017 Sheet 24 of 46

NGFF_M.2 WiFi & BT (NGF)

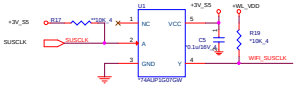
Leakage circuit (MPC)

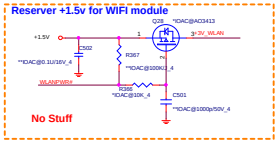


Low	Mini card +3V power enable
High	Mini card +3V power disable

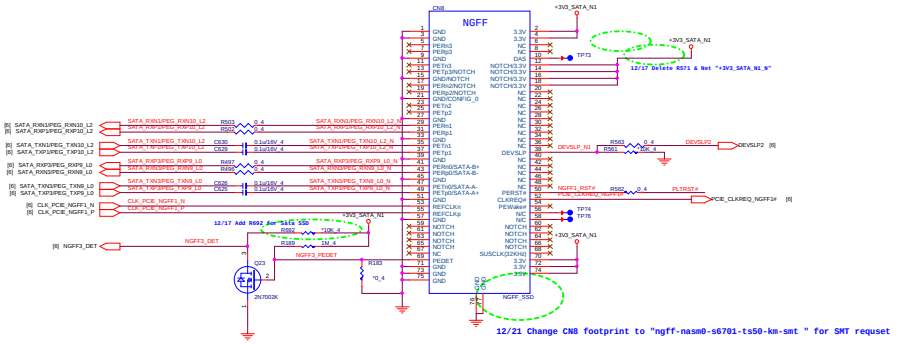


Reserve only for Intel module no need to stuff by default 11/24



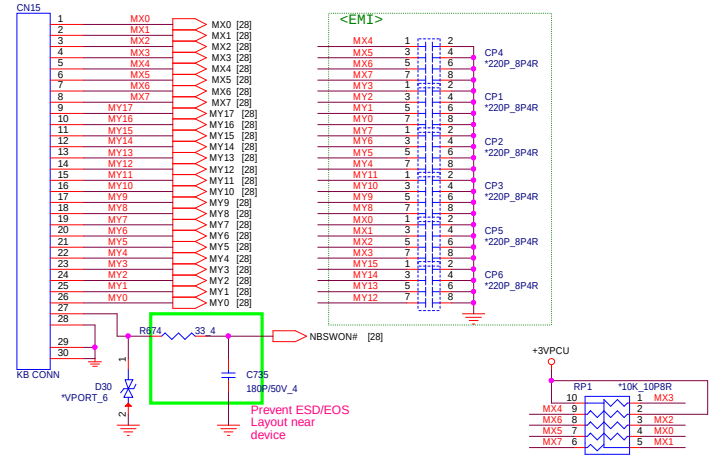


NGFF_M.2 SSD (NGF)

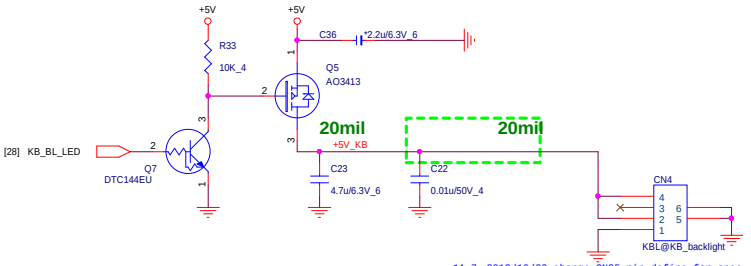


Quanta Computer Inc.			
PROJECT : Z8VR			
Size	Document Number		Rev
	NGFF WiFi & BT & SSD		1A
Date: Thursday, June 22, 2017	Sheet 25 of 45		

KEYBOARD (KBC)



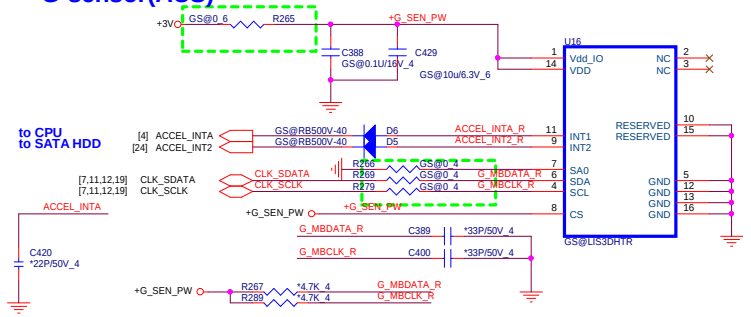
KB_BL LED (KBC)



1A-7 2013/10/22 change CN25 pin define for spec.

1A-8 2013/10/23 change CN25 footprint.

G-sensor(ACS)



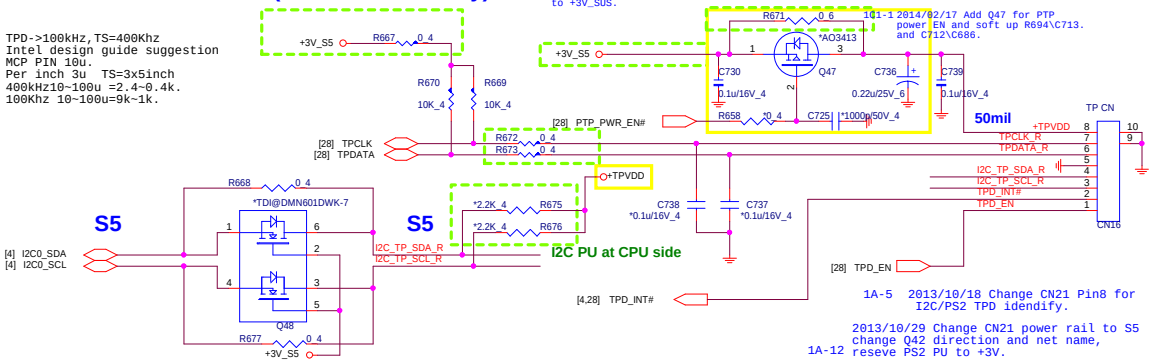
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

1C-2 2014/01/13 Change TP power rail from +3V_S5 to +3V_SUS.

1C-4 2014/01/15 reserve TP power rail +3V_S5.

1C1-1 2014/02/17 Add Q47 for PTP power EN and soft up R694\C713. and C712\C686.

TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.



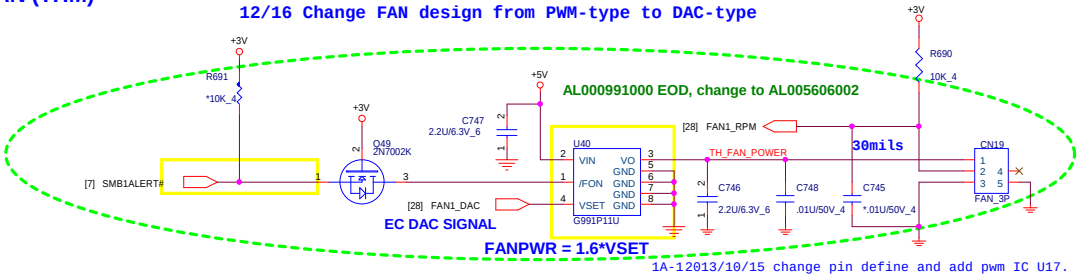
1A-5 2013/10/18 Change CN21 Pin8 for I2C/PS2 TPD idendify.

2013/10/29 Change CN21 power rail to S5 change Q42 direction and net name,

1A-12 reseve PS2 PU to +3V.

CPU FAN (THM)

12/16 Change FAN design from PWM-type to DAC-type



1A-12013/10/15 change pin define and add pwm IC U17.

1A-42013/10/17 Change U17 to G991P11U and PU U17 pin1.

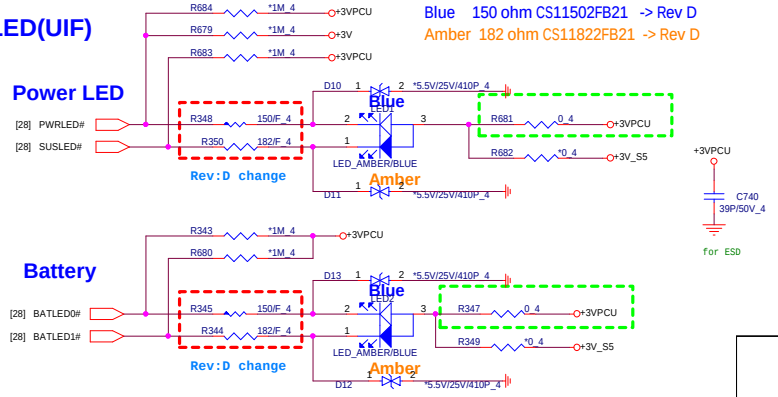
1A-92013/10/24 Add alert on U17.1 for CPU themal tempture.

1A-13 2013/10/31CN15 Pin2/3 swap.

POWER LED(UIF)

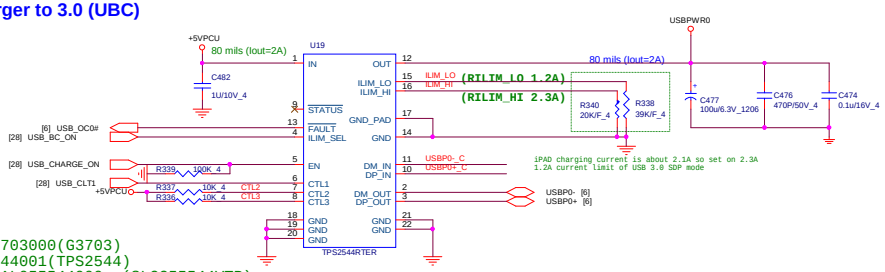
Blue 150 ohm CS11502FB21 -> Rev D

Amber 182 ohm CS11822FB21 -> Rev D



Quanta Computer Inc.		
PROJECT : Z8VR		
Size	Document Number	Rev
	KB/TP/FAN	1A
Date: Thursday, June 22, 2017	Sheet 26 of 46	

USB Charger to 3.0 (UBC)



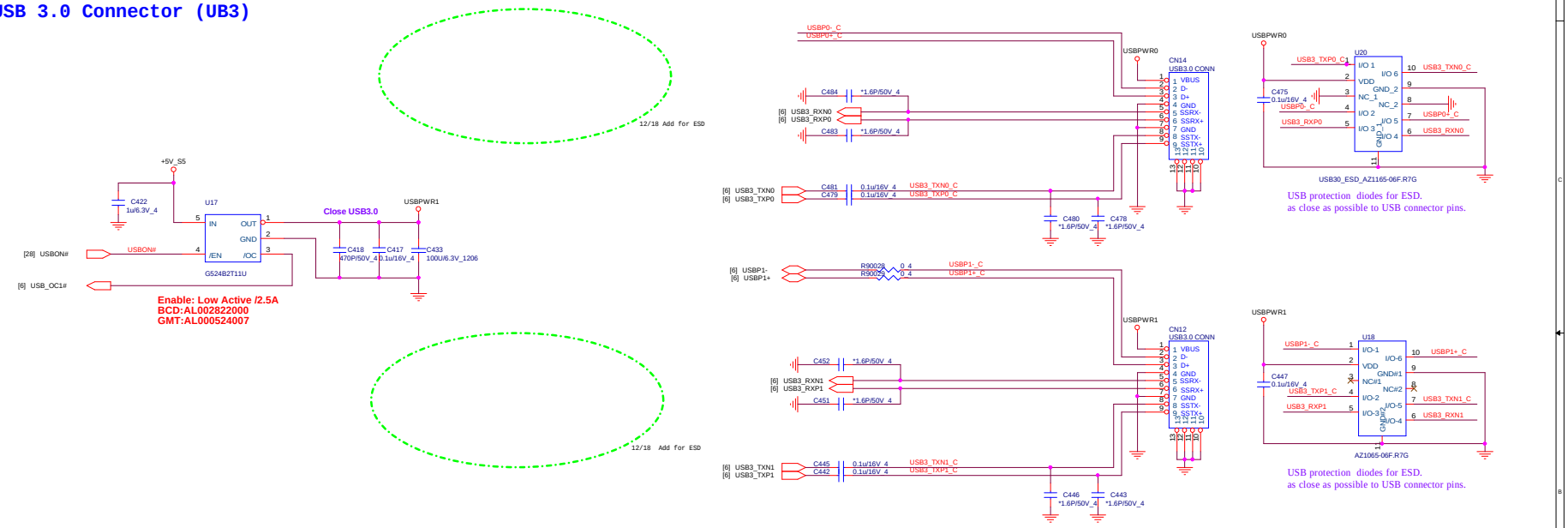
	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

GMT:AL003703000(G3703)
TI:AL002544001(TPS2544)
Silergy: AL055544000 (SLGC55544VTR)

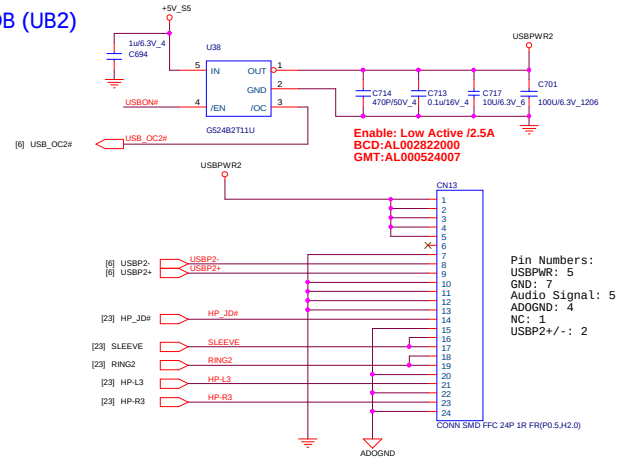
RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$IOS\_typ(mA) = 50{,}250 / \{RILIM\_XX(K\Omega)+0.1\}$$

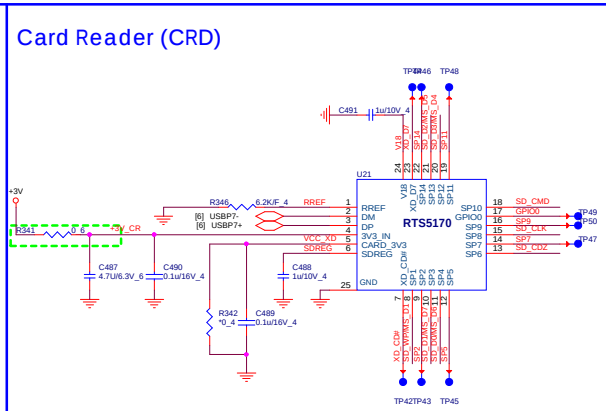
USB 3.0 Connector (UB3)

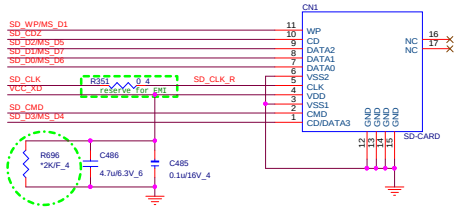


USB2.0 DB (UB2)

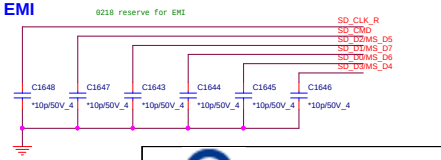


Card Reader (CRD)





EMI



Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	USB3/Charger/CR/USB2 DB	1A
Date: Thursday, June 22, 2017	Sheet 27 of 46	

EC(KBC)

IT8987E/CX
LQFP

AJ089870F02 IT8987E/CX

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

SM BUS PU(KBC)

Battery module

UMA& VGA SKU
Need Stuff

HWPG(KBC)

DDR=1.5V, D1 DNP and D2 POP
DDR=1.35V, D1 POP and D2 DNP

Reset SW (FSW)

Battery Detect Switch

Reserve no stuff

Reserve switch for test
(MP remove)

Quanta Computer Inc.	
PROJECT : Z8VR	
Size	Document Number: KBC IT8587
Rev	1A
Date: Thursday, June 22, 2017	Sheet 28 of 46

Double Check ADP-In Type

12/22 Change PJ2 footprint to "50320-0040n-001-4p-l-smt"
& reverse Pin1~4 for SMT request

PJ2 Power conn

VA PD1 SV1040 VA1 PQ1 AON6414AL VA2 PR3 0.01/F_0612 VIN PQ2 AON6414AL

PC14 0.1u/50V_6 PC13 2200p/50V_4 PD2 P4SMAFJ28A PC5 0.1u/50V_6 PC1 1n/50V_4 PC2 47n/50V_6

PR29 4.02K/F_4 PR28 4.02K/F_4 PR2 0_4 24780_ACN PR1 0_4 24780_ACP

PC12 0.1u/50V_6 PC7 2200p/50V_4 PC17 *0.01u/50V_4 PR4 0_6

24780_ACP 24780_ACN PR72 10/F_6

PC36 0.1u/50V_6 PC25 0.1u/50V_6 PC35 0.1u/50V_6 24780_CMSRC

PR16 20_1206

PR31 866K/F_4 PR211 137K/F_4

REGN6V PR39 100K/F_4 PR40 100K/F_4

[28] ACIN

PC16 0.47u/25V_6

24780_ACDRV 24780_VCC 24780_ACDET

PR30 0_4 PR19 0_4 PR17 0_4 PR32 0_4 PR26 0_4 PR25 0_4

MBDATA MBCLK ICMNT

[28] ICMNT TP1 D/C# [34] PMON PMON

PR23 SP@12.7K/F

UMA-> PR342 CS31542FB14 15.4K 1/16W +-1% (0402) For 78W
Dis -> PR342 CS31272FB17 12.7K 1/16W +-1% (0402) For 95W

no stuff PC18 *100P/50V_4 PC36 100P/50V_4 PC37 100P/50V_4

+3VPCU PR9 10K_4 PR15 *10K_4 PR204 316K/F_4

24780_BM# 24780_CMPOUT 24780_ILIM 24780_CMPIN

PR206 100K/F_4 PR207 100K_4 PC8 0.01u/50V_4

PU1 BQ24780SRUYR

CMSRC ACP ACN BATDRV BATSRC ACDRV VCC REGN BTST HIDRV PHASE LDODRV SRP SRN ACDET ACOK SDA SCL IADP IDCHG PMON TB_STAT CMPOUT ILIM CMPIN PROCHOT BATPRES GND#1 GND#2 GND#3 GND#4 GND#5 PAD GND#6 GND#7 GND#8 GND#9 GND#10

24780_BATDRV 24780_BATSRC 24780_REGN 24780_BST 24780_DH 24780_LX 24780_DL

REGN6V PR11 0_6 PC9 2.2u/10V_6 PC15 47n/50V_6

PQ30 AON7410 PQ29 AON7410 PL5 6.8uH_7X7X3

VIN PC172 2200p/50V_4 PC170 10u/25V_8

PR33 *4.7_6 PC19 *680p/50V_6

PR209 0.01/F_0612 BAT-V PR210 0_4 PR208 0_4

24780_SRP 24780_SRN PC165 2200p/50V_4 PC164 10U/25V_8 PC166 10U/25V_8

PR52 0_6 PR62 0_6 PC6 0.1u/25V_4 PC3 0.1u/25V_4 PC4 0.1u/25V_4

PC167 0.1u/50V_6 PC168 *100p/50V_4

BAT-V BI [28] PR10 *0_4 PR14 100_4 TEMP_MBAT# TEMP_MBAT# [28] PR18 1M_4 +3VPCU

SM06B-GHS-TB PJ1

PR13 100_4 PR12 100_4

Double Check BATT-In Type

MBCLK [28] MBDATA [28]

PC10 *47p/50V_4 PC11 *47p/50V_4 PD3 PDZ5.6B PD4 PDZ5.6B

PR8 0_4 PR35 *10_4 TEMP_MBAT#

H_PROCHOT# H_PROCHOT# [2,28,34]

C756 0.1u/16V_4 PR22 *100K_4 +VCCIO

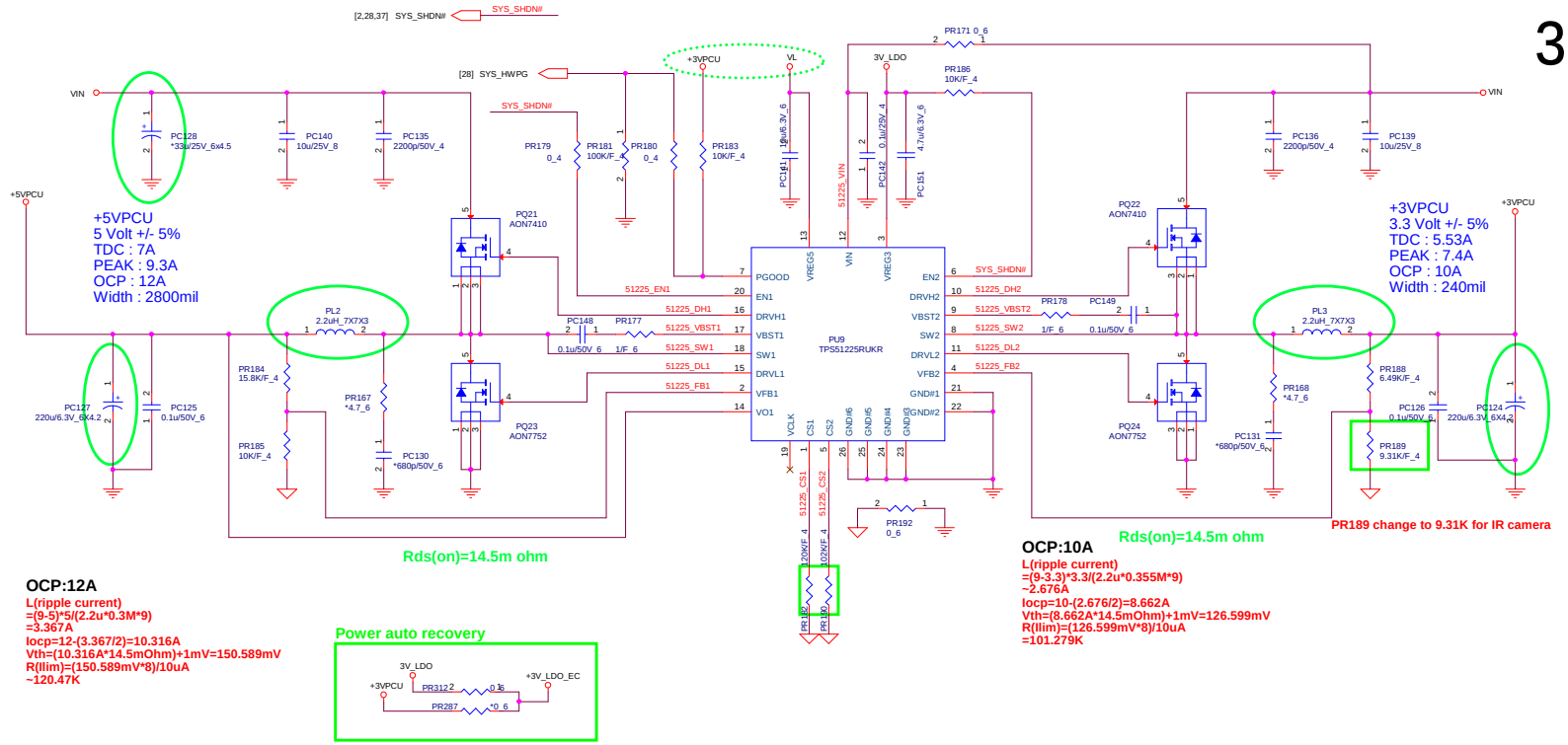
Check PU high with HW side

REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit

ILIM=0.793V
Rsr = 0.01ohm

Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	Charger (BQ24780S)	1A
Date: Thursday, June 22, 2017	Sheet 29 of 46	



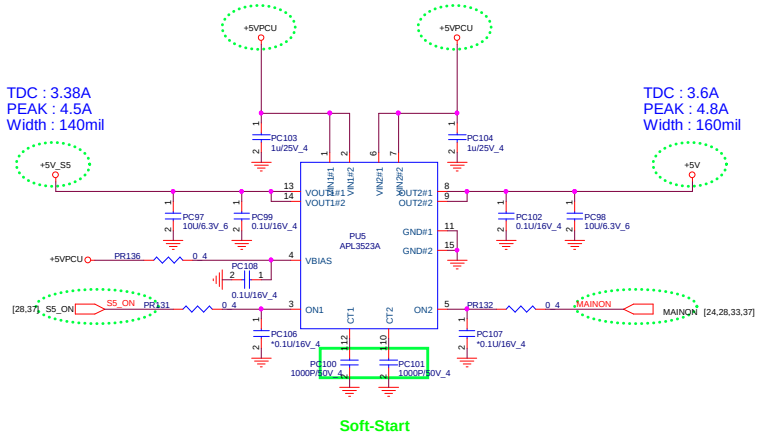
OCP:12A

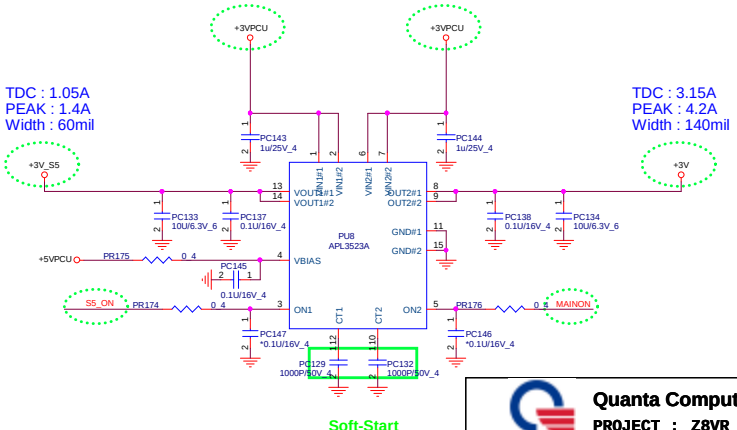
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=12-(3.367/2)=10.316A
Vth=(10.316A*14.5mOhm)+1mV=150.589mV
R(Ilim)=(150.589mV*8)/10uA
~120.47K

OCP:10A

L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=10-(2.676/2)=8.662A
Vth=(8.662A*14.5mOhm)+1mV=126.599mV
R(Ilim)=(126.599mV*8)/10uA
=101.279K

Power auto recovery

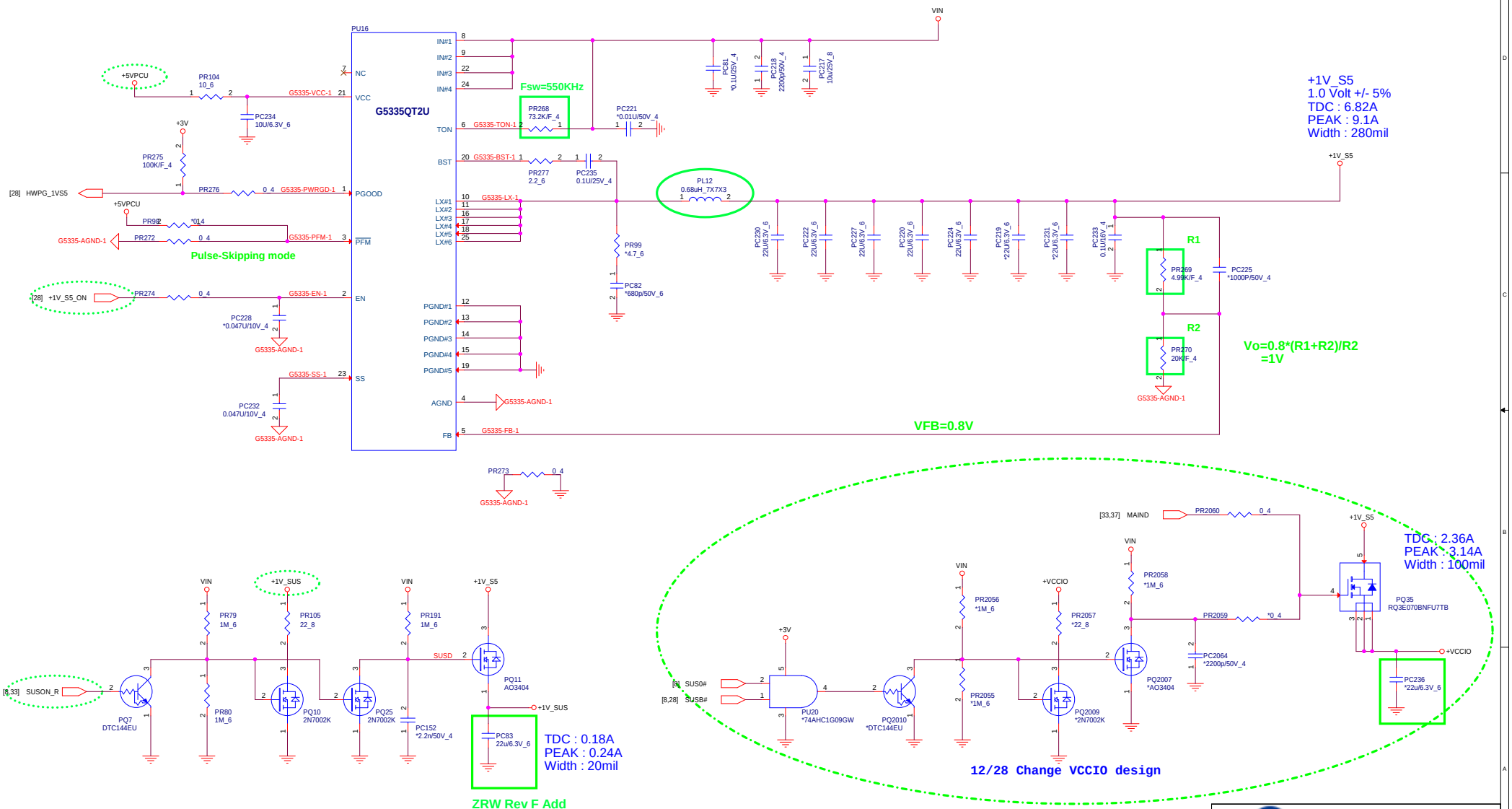




Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	SYSTEM 5V/3V (TPS51225R)	1A

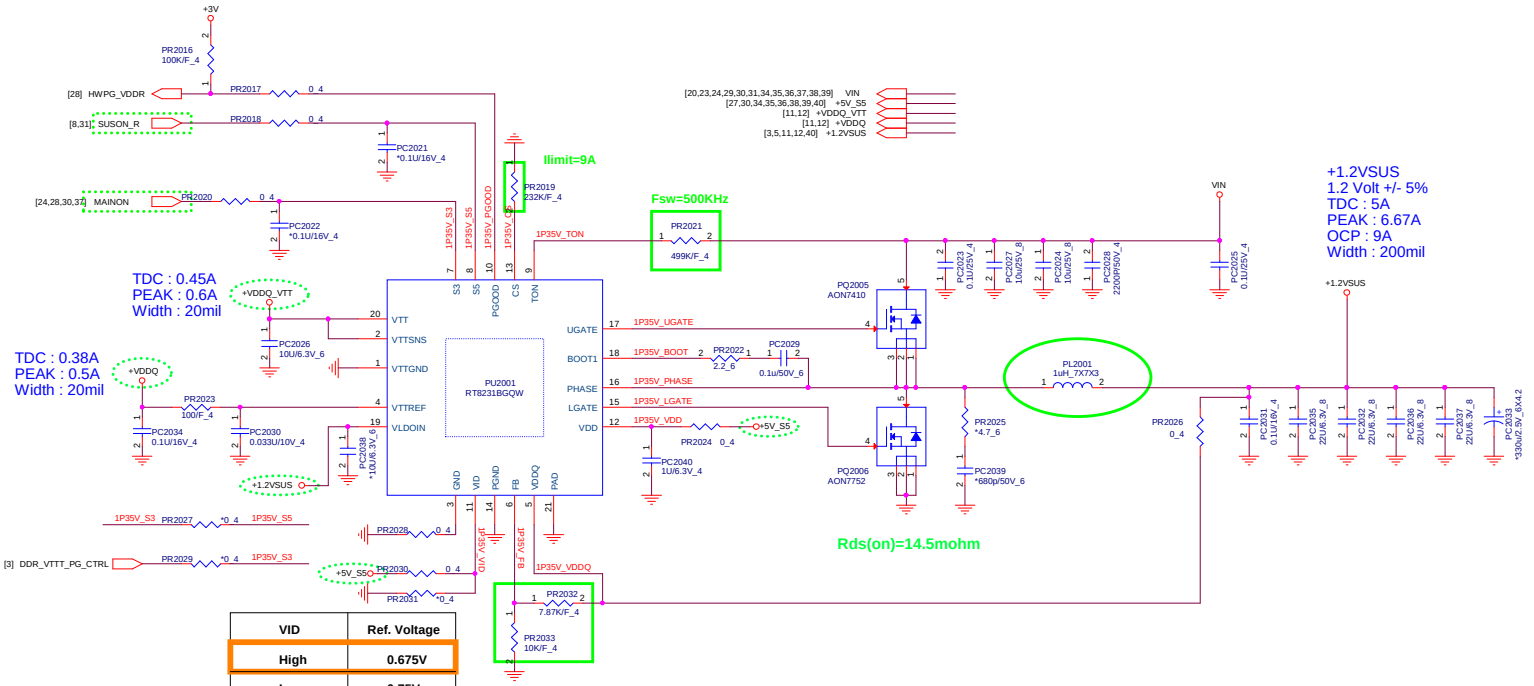
Date: Thursday, June 22, 2017 Sheet 30 of 46



Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	+1V_S5 (G5335QT2U)	1A

Date: Thursday, June 22, 2017 Sheet 31 of 46



TDC : 0.45A
PEAK : 0.6A
Width : 20mil

TDC : 0.38A
PEAK : 0.5A
Width : 20mil

+1.2VSUS
1.2 Volt +/- 5%
TDC : 5A
PEAK : 6.67A
OCP : 9A
Width : 200mil

Rds(on)=14.5mohm

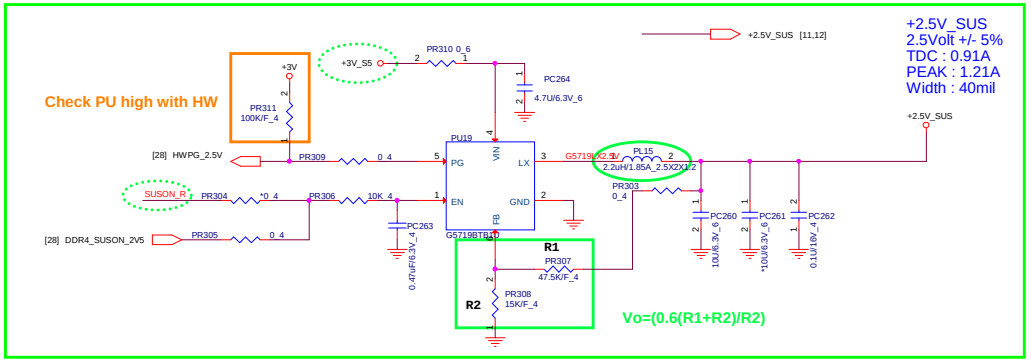
VID	Ref. Voltage
High	0.675V
Low	0.75V

OCP=9A
L ripple current
=(19-1.2)*1.2/(1u*500k*19)
=2.248A
Vtrip=9-(2.248/2)*14.5mohm
=114.202mV
Rlimit=114.202mV/5uA*10=228.4Kohm

DDR=1.2V
PR2032=7.87K/F_4
PR2033=10K/F_4

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

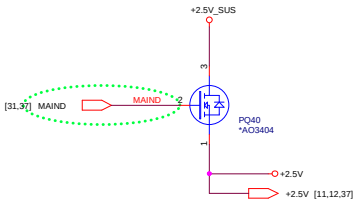
+2.5VSUS Power Rail For DDR4



+2.5V_SUS
2.5Volt +/- 5%
TDC : 0.91A
PEAK : 1.21A
Width : 40mil

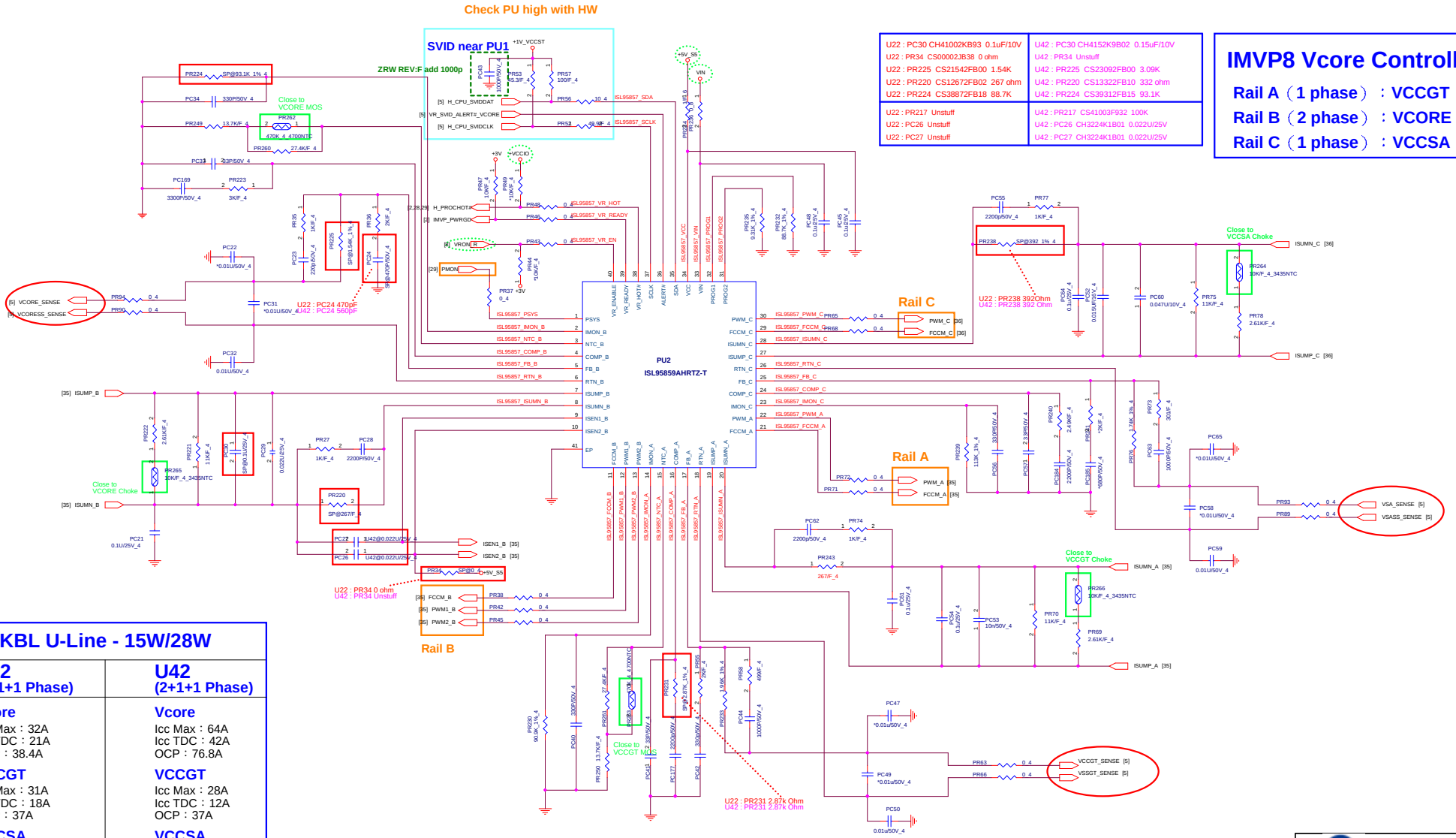
Vo=(0.6(R1+R2)/R2)

10/26 Reserve +2.5V for DDR4 VDDSPD



TDC : 0.16A
PEAK : 0.21A
Width : 20mil

Quanta Computer Inc.
PROJECT : Z8VR
Size
Document Number
DDR4_+1.2VSUS (G5316RZ1D)
Rev 1A
Date: Thursday, June 22, 2017
Sheet 33 of 46



U22	U42
U22 : PC30 CH41002KB93 0.1uF/10V	U42 : PC30 CH4152K9B02 0.15uF/10V
U22 : PR34 CS00002JB38 0 ohm	U42 : PR34 Unstuff
U22 : PR225 CS21542FB00 1.54K	U42 : PR225 CS23092FB00 3.09K
U22 : PR220 CS12672FB02 267 ohm	U42 : PR220 CS13322FB10 332 ohm
U22 : PR224 CS38872FB18 88.7K	U42 : PR224 CS39312FB15 93.1K
U22 : PR217 Unstuff	U42 : PR217 CS41003F932 100K
U22 : PC26 Unstuff	U42 : PC26 CH3224K1B01 0.022U/25V
U22 : PC27 Unstuff	U42 : PC27 CH3224K1B01 0.022U/25V

IMVP8 Vcore Controller

- Rail A（1 phase）：VCCGT
- Rail B（2 phase）：VCORE
- Rail C（1 phase）：VCCSA

KBL U-Line - 15W/28W

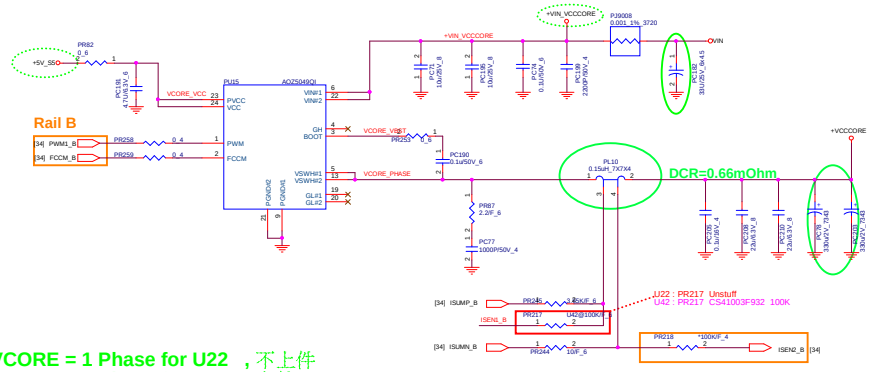
U22 (1+1+1 Phase)	U42 (2+1+1 Phase)
Vcore	**Vcore**
Icc Max：32A	Icc Max：64A
Icc TDC：21A	Icc TDC：42A
OCP：38.4A	OCP：76.8A
VCCGT	**VCCGT**
Icc Max：31A	Icc Max：28A
Icc TDC：18A	Icc TDC：12A
OCP：37A	OCP：37A
VCCSA	**VCCSA**
Icc Max：4.5A	Icc Max：5A
OCP：10A	OCP：10A

Quanta Computer Inc.
PROJECT : Z8VR
Size | Document Number: CPU_CORE (ISL95859HRTZ-T) | Rev: 1A
Date: Thursday, June 22, 2017 | Sheet 34 of 46

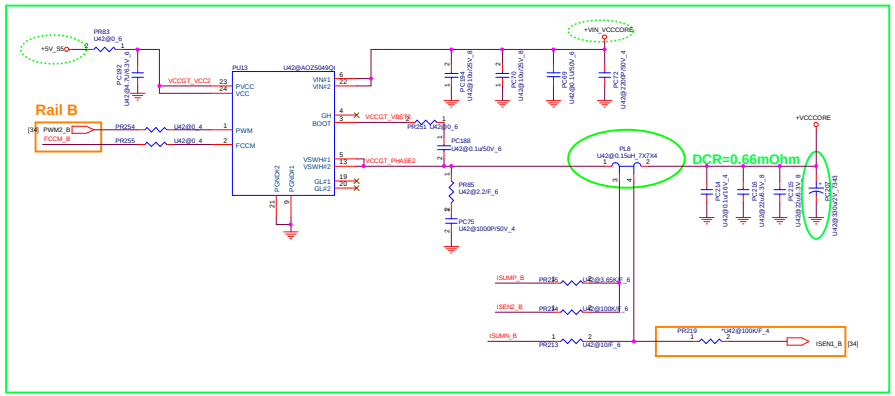
[20,23,24,29,30,31,33,34,36,37,38,39] VIN
[5] +VCCCORE
[5] +VCCGT
[27,30,33,34,36,38,39,40] +5V_S5

U22 : PR217 Unstuff	U42 : PR217 CS41003F932 100K

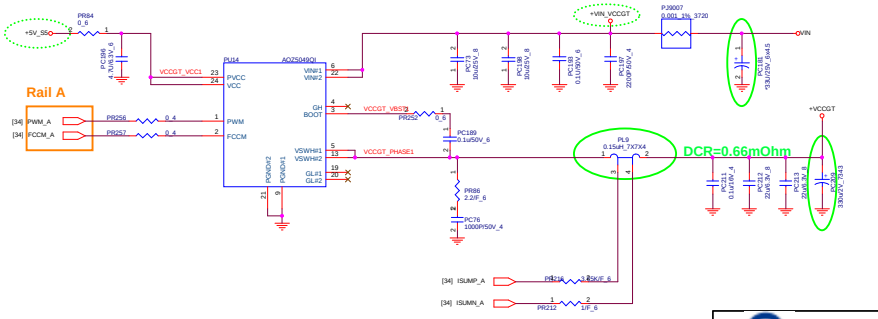
VCORE



VCORE = 1 Phase for U22 ，不上件
VCORE = 2 Phase for U42 ，上件



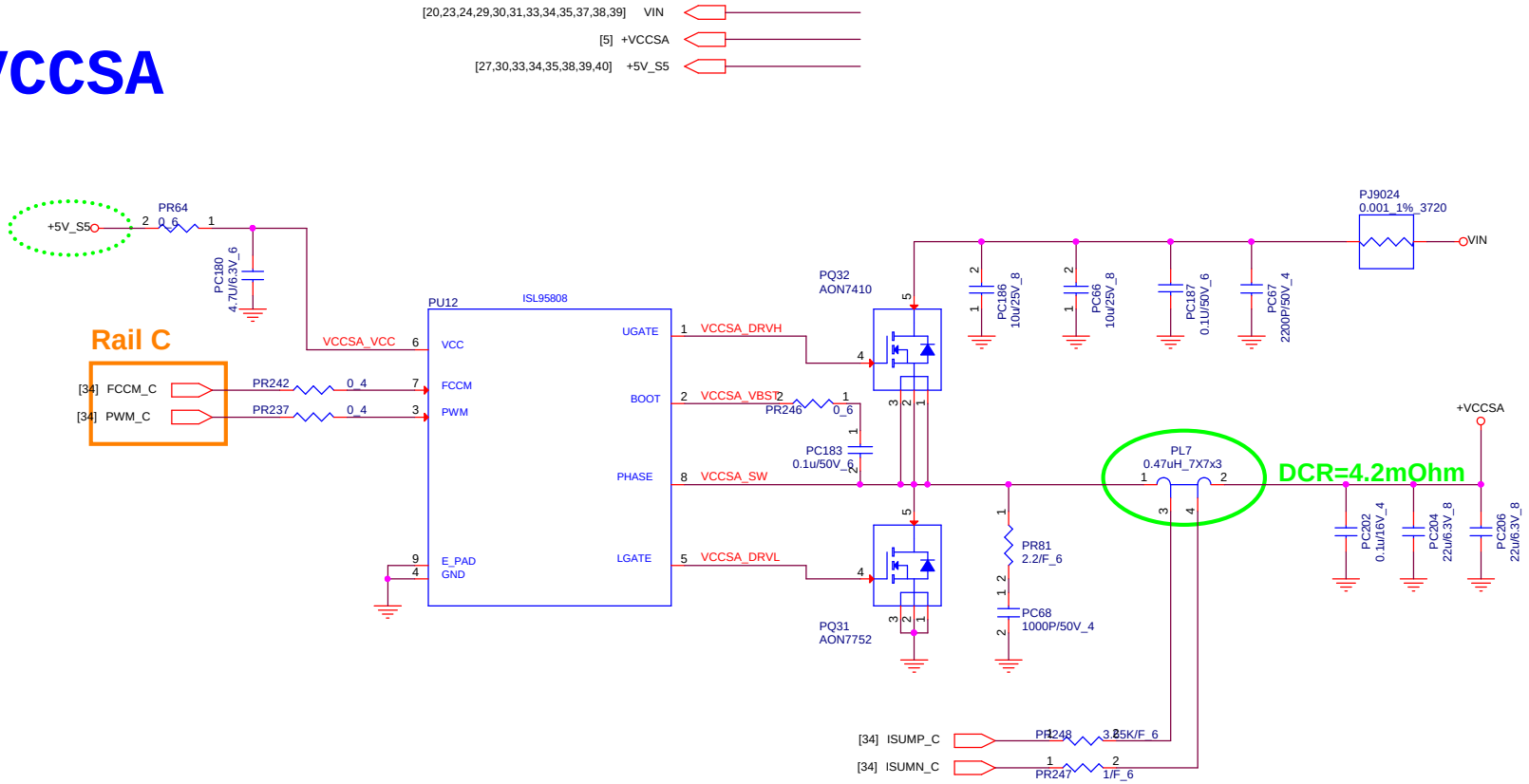
VCCGT



Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	VCORE/VCCGT (ISL95808HRZ-T)	1A
Date: Thursday, June 22, 2017	Sheet 35 of 46	

VCCSA



VCCSA

Icc TDC PL2：5A

Icc Max：5A

OCP：6A

Fsw：800KHz

VCCSA L/L：

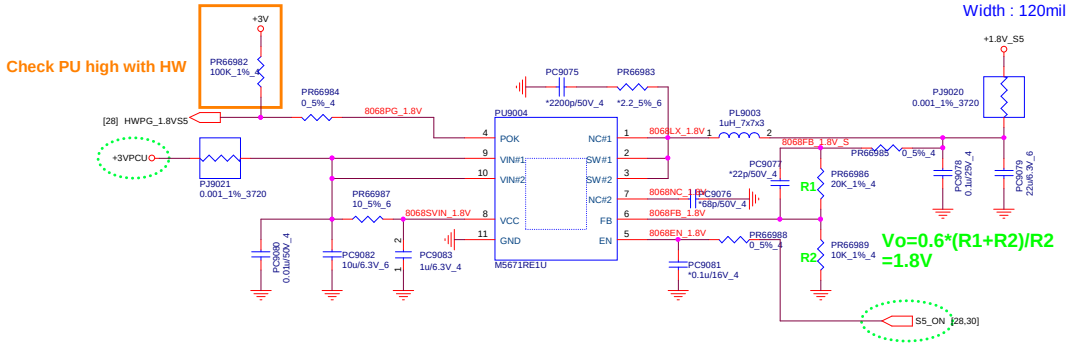
R_DC_LL：10.3mV/A

R_AC_LL：10.3mV/A

Quanta Computer Inc.		
PROJECT : Z8VR		
Size	Document Number: VCCSA (ISL95808HRZ-T)	Rev 1A
Date: Thursday, June 22, 2017	Sheet 36 of 46	

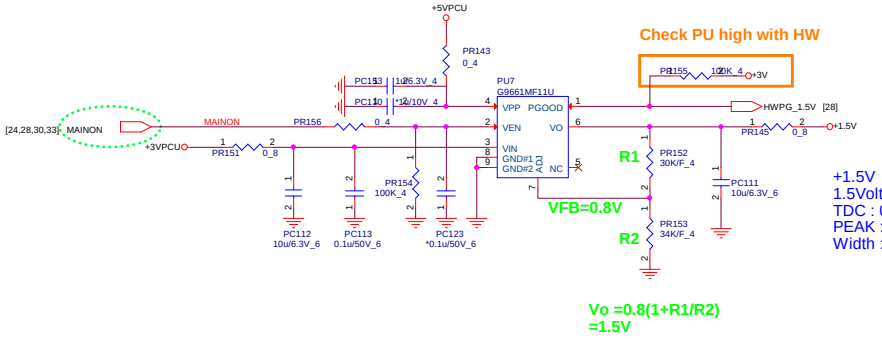
+1.8V_S5
1.8Volt +/- 5%
TDC : 2.61A
PEAK : 3.48A
Width : 120mil

Check PU high with HW



+1.5V
1.5Volt +/- 5%
TDC : 0.49A
PEAK : 0.66A
Width : 20mil

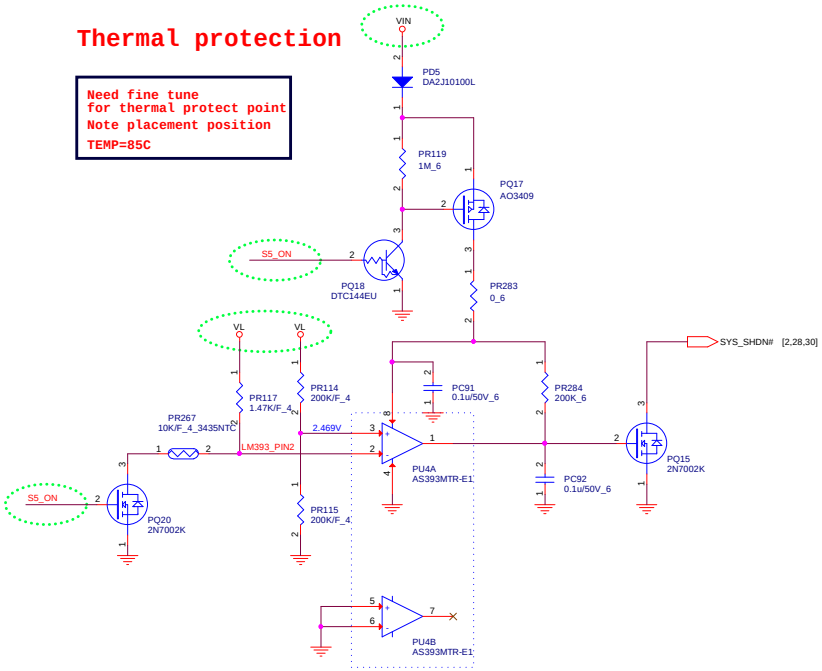
Check PU high with HW



Vo =0.8(1+R1/R2)
=1.5V

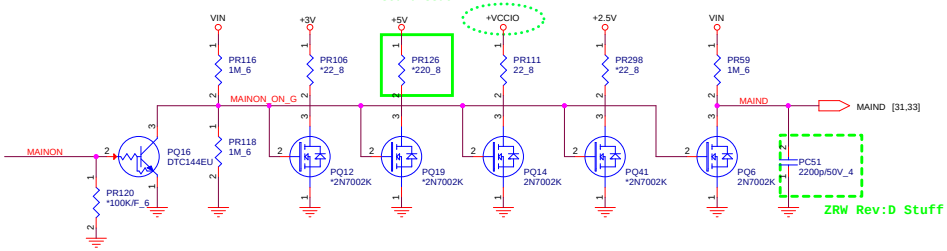
Thermal protection

Need fine tune
for thermal protect point
Note placement position
TEMP=85C



For EC control thermal protection (output 3.3V)

PR153 Change to
220 ohm for bo bo
sound issue.

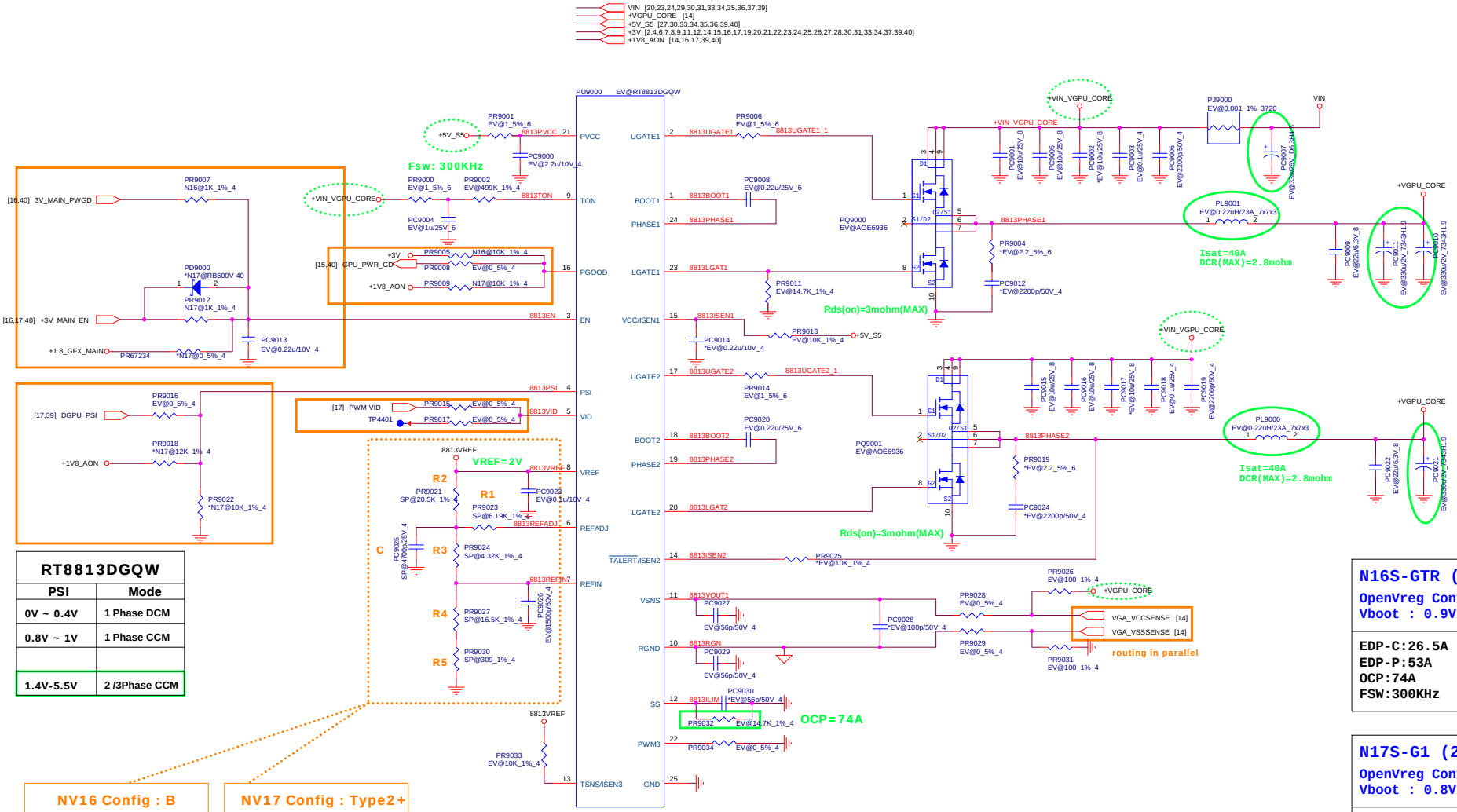


ZRW Rev:D Stuff

Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	+1.8V/+1.5V/Thermal Protect	1A
Date: Thursday, June 22, 2017	Sheet 37 of 46	

VGPU_CORE



RT8813DGQW	
PSI	Mode
0V ~ 0.4V	1 Phase DCM
0.8V ~ 1V	1 Phase CCM
1.4V-5.5V	2 /3Phase CCM

NV16 Config : B	
R1	20K
R2	20K
R3	2K
R4	18K
R5	0 ohm
C	2.7nF

NV17 Config : Type2+	
R1	6.19K
R2	20.5K
R3	4.32K
R4	16.5K
R5	0.309K
C	4.7nF

N16S-GTR (23W/GDDR5)
OpenVreg Config : B
Vboot : 0.9V

EDP-C:26.5A
EDP-P:53A
OCP:74A
FSW:300KHz

N17S-G1 (23W/GDDR5)
OpenVreg Config : Type2+
Vboot : 0.8V

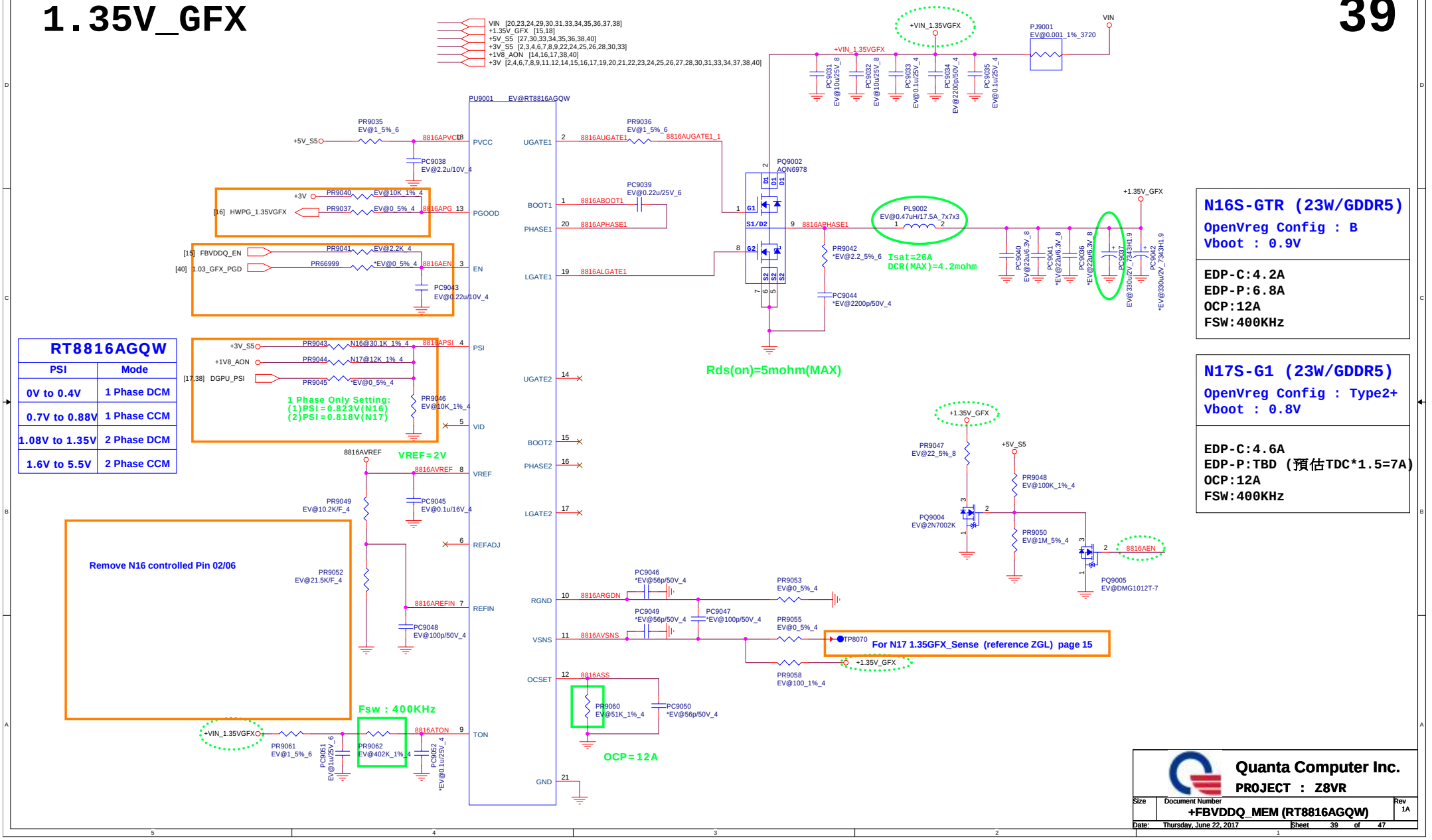
EDP-C:27.9A
EDP-P:62.2A
OCP:74A
FSW:300KHz

Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	+NVVDD (RT8813DGQW)	1A

Date: Thursday, June 22, 2017 Sheet 38 of 47

1.35V_GFX



RT8816AGQW	
PSI	Mode
0V to 0.4V	1 Phase DCM
0.7V to 0.88V	1 Phase CCM
1.08V to 1.35V	2 Phase DCM
1.6V to 5.5V	2 Phase CCM

N16S-GTR (23W/GDDR5)

OpenVreg Config : B
Vboot : 0.9V

EDP-C:4.2A
EDP-P:6.8A
OCP:12A
FSW:400KHz

N17S-G1 (23W/GDDR5)

OpenVreg Config : Type2+
Vboot : 0.8V

EDP-C:4.6A
EDP-P:TBD (預估TDC*1.5=7A)
OCP:12A
FSW:400KHz

Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	+FBVDDQ_MEM (RT8816AGQW)	1A
Date: Thursday, June 22, 2017	Sheet 39 of 47	

+1.8V_S5 [8,9,10,37]
+1.8_GFX_MAIN [14,15,16]
+1V8_AON [14,16,17,38,39]

+5VPCU [27,30,31,37]
+1.2VSUS [3,5,11,12,33]
+1.03_GFX [14,15,16]
+5V_S5 [27,30,33,34,35,36,38,39]
+3V [2,4,6,7,8,9,11,12,14,15,16,17,19,20,21,22,23,24,25,26,27,28,30,31,33,34,37,38,39]

N16S-GTR
+3V_GFX TDC : 0.06A Width : 20mil

N17S-G1
+1.8V_MAIN TDC : 1.13A PEAK : 1.5A Width : 60mil

PR9084 For N17 use only

+3V_GFX
PR9066 N16@0_5%_8
PR9084 N17@0_5%_8
+1.8_GFX_MAIN
PR9067 N17@0_5%_8

+3VPCU
+1.8V_S5
PR9063 N16@0_5%_8
PR9064 N17@0_5%_8
PR9065 N17@0_5%_8
PC9053 EV@1u/25V_4
PC9054 N17@1u/25V_4

PU9002 EV@AOZ1331DI
VIN1#1 VIN1#2 VIN2#1 VIN2#2
VOUT1#1 VOUT1#2
OUT2#1 OUT2#2
VBIAS
GND#1 GND#2
ON1 ON2 CT1 CT2

PC9055 EV@10u/6.3V_6
PC9056 EV@0.1u/16V_4
PC9057 N17@0.1u/16V_4
PC9058 N17@10u/6.3V_6
1V8_AON_S
PR9068 N17@0_5%_8
+1V8_AON

+5VPCU
PR9069 EV@0_5%_4
PC9059 EV@0.1u/16V_4
PR9070 N17@0_5%_4
DGPU_PWR_EN
PC9060 *N17@0.1u/16V_4

[4] DGPU_PWR_EN
PR9071 N16@0_5%_4
PC9061 *N16@0.1u/16V_4
[16,17,38] +3V_MAIN_EN
PR9072 N17@0_5%_4
PC9062 EV@1000p/50V_4
PC9063 N17@1000p/50V_4
PC9064 *N17@820p/50V_4

N17S-G1
+1.8V_AON TDC : 1.13A PEAK : 1.5A Width : 60mil

A2

VIN
+1.8_GFX_MAIN
PR67230 N17@1M_5%_6
PR67231 N17@22_5%_8
+3V_MAIN_EN_G
PQ9083 N17@LTC044EUBFS8TL
+3V_MAIN_EN
PR67232 N17@1M_5%_6
PQ9084 N17@2N7002KW
PR67233 *N17@100K_1%_6

N16S-GTR	N17S-G1
+1.05V TDC : 0.8A PEAK : 2.1A Width : 80mil	+1V TDC : 0.9A PEAK : 1.1A Width : 40mil

+1.2VSUS
PJ9002 EV@0.001_1%_3720
PQ9008 EV@AON7408
PEX_VDD_S
PC9065 EV@0.1u/16V_4
PC9066 EV@10u/6.3V_6
PC9067 EV@10u/6.3V_6
PC9068 EV@10u/6.3V_6
PC9069 EV@0.1u/16V_4
9336DRV

+1.03_GFX
PJ9003 EV@0.001_1%_3720
PC9070 *EV@220u/2V_7343H1.9

PR9073 EV@5.6_5%_8
+5V_S5
PR9074 EV@100K_1%_4
PQ9009 EV@2N7002K
PQ9010 EV@DMG1012T-7
PR9077 EV@1M_5%_4

+3V
PR9075 EV@10K_1%_4
PD9001 EV@1SS355
PQ9011 EV@2N7002K

Check N16 Power Good

+1V8_AON
Check PU high with HW
PR9076 N17@10K_1%_4

PU9003 EV@G9336ADJTP1U
PR9078 N17@0_5%_4
[39] 1.03_GFX_PGD
PGD EN VCC GND DRV ADJ
PR9080 EV@47_1%_4
PC9071 EV@0.01u/50V_4
[15,38] GPU_PWR_GD
PR9079 N17@0_5%_4
PC9073 *N17@0.1u/16V_4
+5VPCU
PC9072 EV@0.1u/16V_4
9336ADJ
PR9081 EV@133_1%_4
PEX_VDD_S
R1
R2
PR9082 EV@124/F_4

N16S:Vo=(1+R1/R2)*0.5=1.03V
N17S:Vo=(1+R1/R2)*0.5=1.03V

[16,38] 3V_MAIN_PWGD
PR9083 N16@1K_1%_4
PC9074 N16@0.22u/10V_4

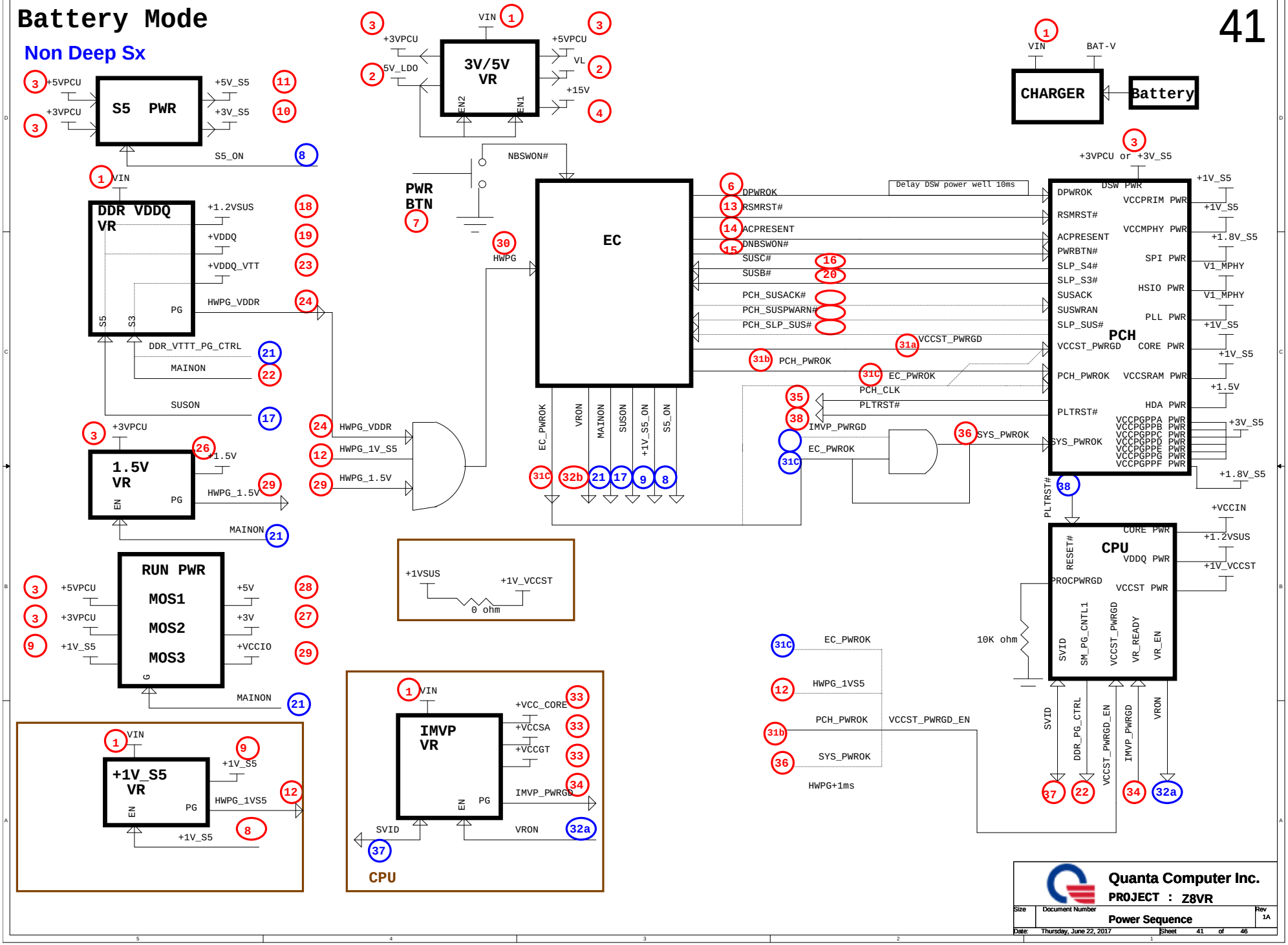
	R1	R2
N16S	133 ohm	124 ohm
N17S	133 ohm	124 ohm

Quanta Computer Inc.
PROJECT : Z8VR

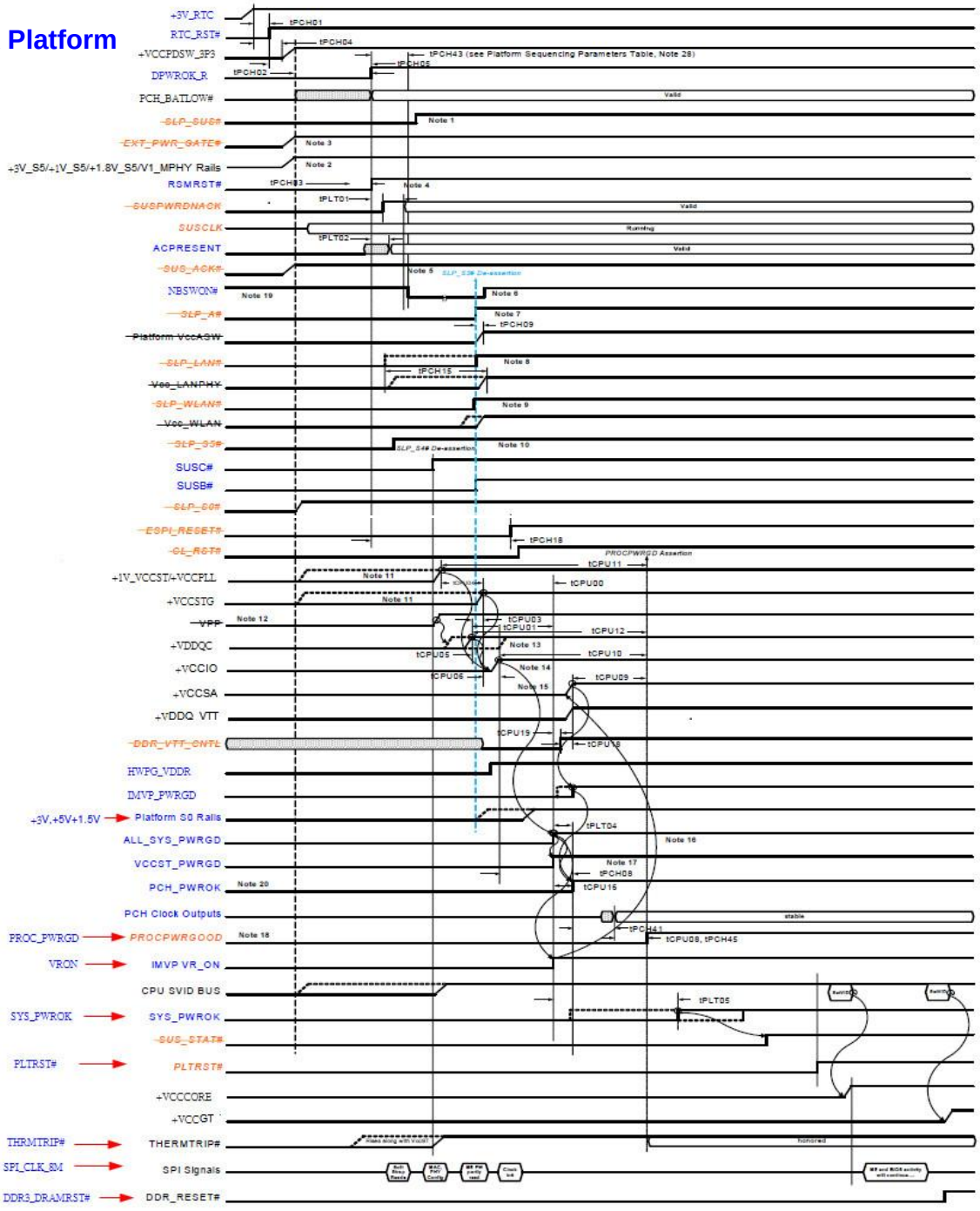
Size	Document Number	Rev
	+1.8V_AON (AOZ1331DI)	1A
Date: Thursday, June 22, 2017	Sheet 40 of 47	

Battery Mode

Non Deep Sx

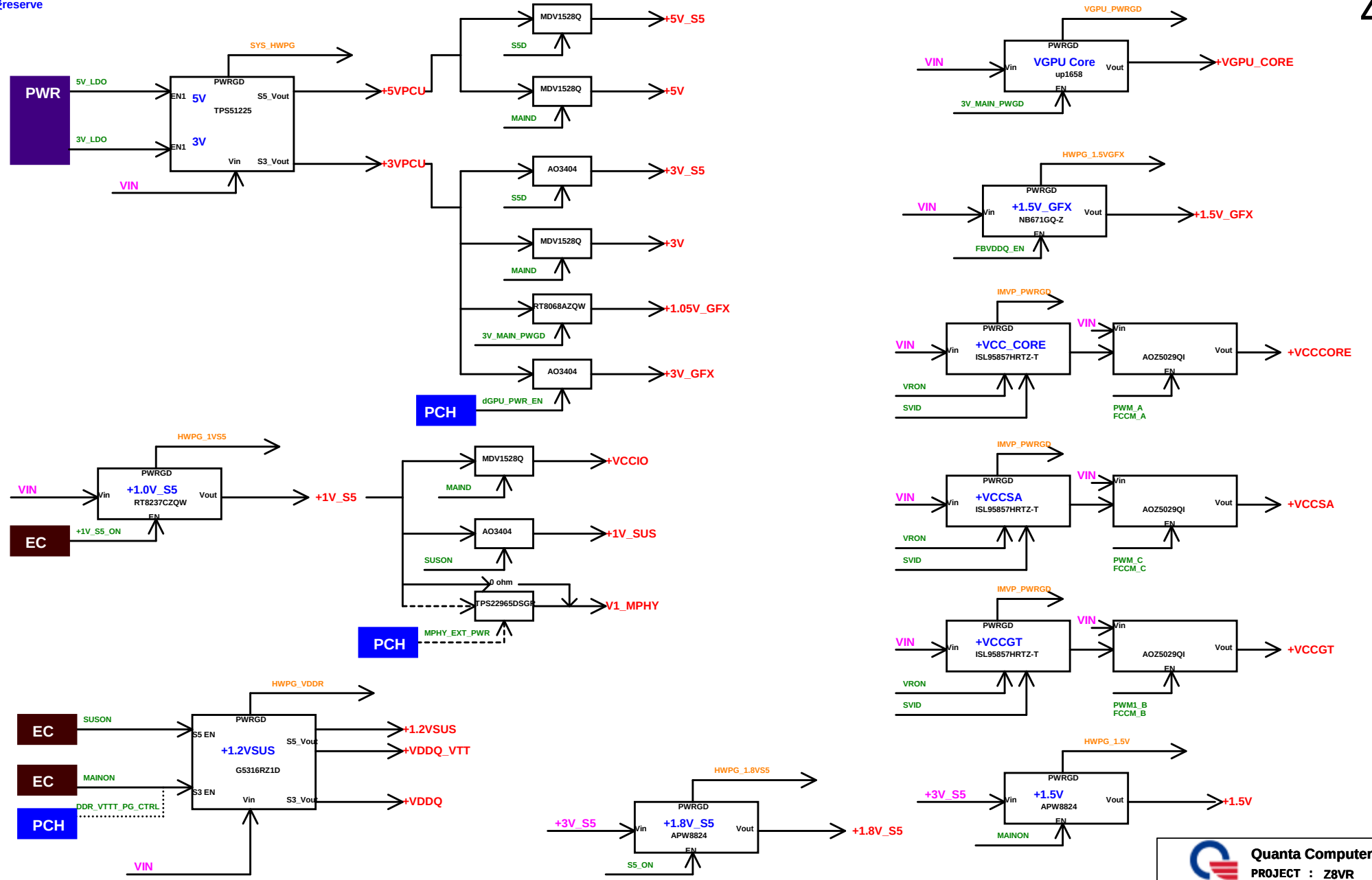


Skylake U Non-Deep Sx Platform Power on sequence



Quanta Computer Inc.		
PROJECT : Z8VR		
Size	Document Number: Power on Sequence	Rev: 1A
Date: Thursday, June 22, 2017	Sheet 42 of 46	

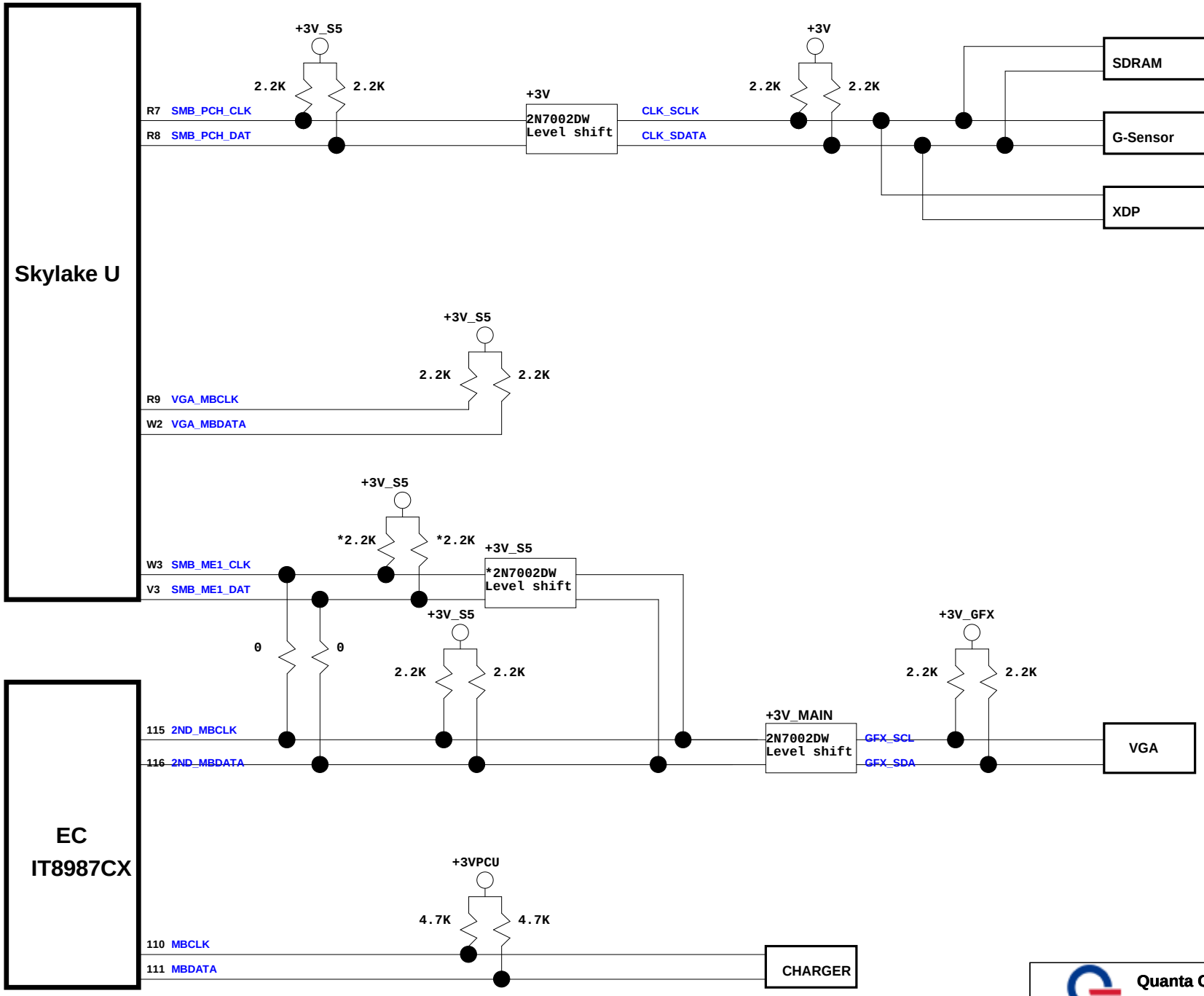
實線表defult
虛線表reserve



Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	SKL PCH PWR CONTROL	1A

Date: Thursday, June 22, 2017 Sheet 43 of 46



Quanta Computer Inc.
PROJECT : Z8VR

Size	Document Number	Rev
	SMBUS Block Diagram	1A
Date: Thursday, June 22, 2017	Sheet 44 of 46	

Model	Date	CHANGE LIST
Z8VR REV:A	03/14	First release
Z8VR REV:B	03/16	Change SW3 Footprint to Sw-ds-a40e-4p-smt for SMT issue Remove C460/C461 for 16G memory module can't power on issue Change SPI ROM GGD 16M P/N to GD25B127DSIGR, original PN is EOL
	03/28	according to Intel DG to unstuff R8748,R8749 and R417.
	04/28	label PR23 as sp@(UMA and DIS value are different)
Z8VR REV:C	05/15	Change 0 Ohm to shortpad add EV@ for PQ9002 value that no need to stuff on UMA SKU
	06/01	Change for Power Noise issue 1.Add PC181 with 33uF in +VIN_VCCGT net 2.Change PC210,PC216 from 22 uF to 47 uF 3.Change PC208,PC212 from 22uF to no stuff

Quanta Computer Inc. PROJECT : Z8VR Size: Document Number: Change list; Rev: 1A Date: Thursday, June 22, 2017; Sheet 45 of 46	DOC NO.	PROJECT MODEL :	Z8VR	APPROVED BY:	DATE:
		PART NUMBER:		DRAWING BY:	REVISON:

Model	Date	CHANGE LIST

Quanta Computer Inc. PROJECT : Z8VR Size: Document Number: Change list Rev: 1A Date: Thursday, June 22, 2017 Sheet 46 of 46	DOC NO.	PROJECT MODEL :	Z8VR	APPROVED BY:	DATE:
		PART NUMBER:		DRAWING BY:	REVISON: