LCFC Confidential

BE560 Rev1.0 Schematic

Intel SkyLake Processor with DDRIIIL + PCH-LP

AMD Litho XT GDDR5 2GB

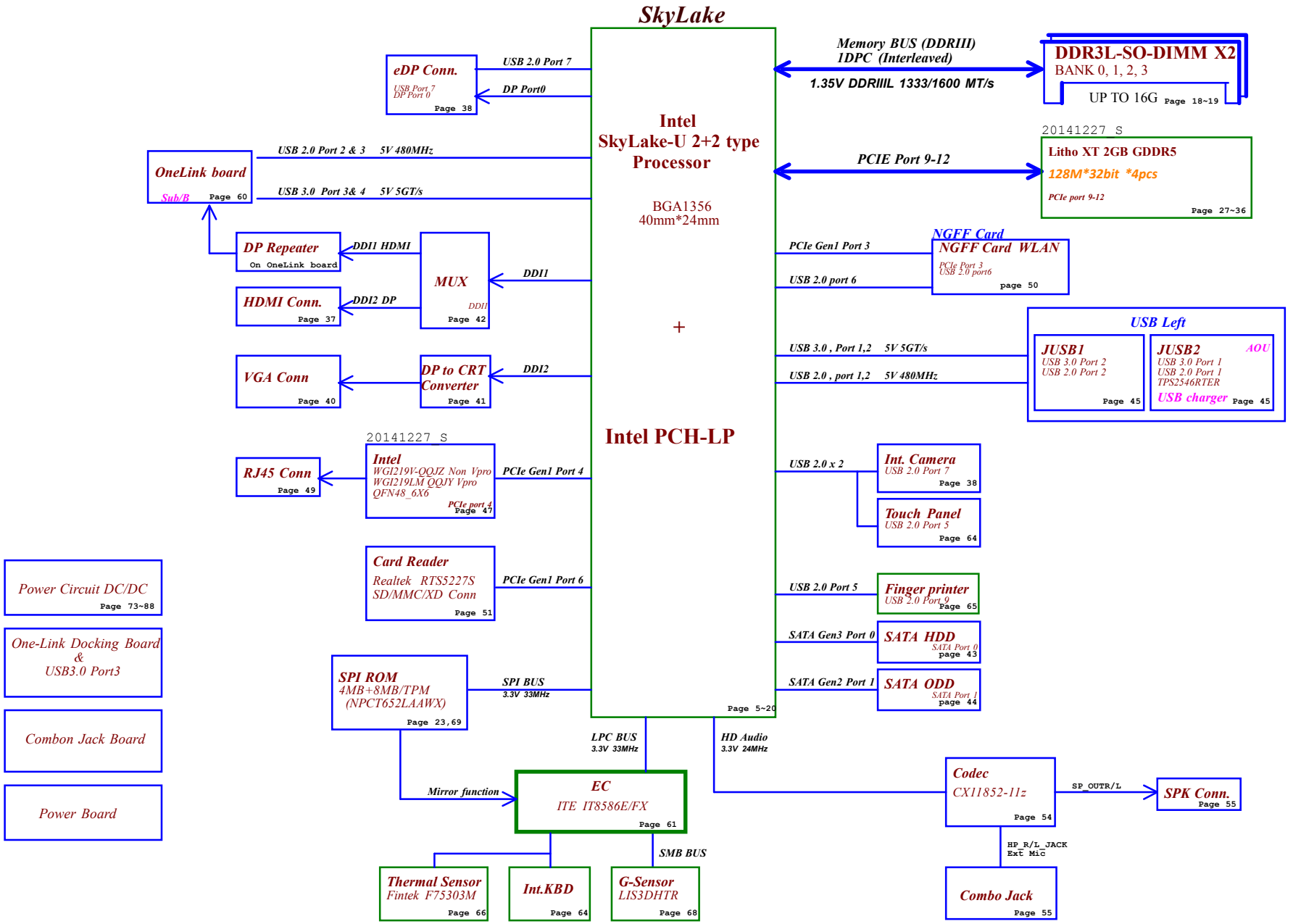
2015-07-28 Rev1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: COVER PAGE

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 1 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A2	BE560	0.1

Date: Wednesday, September 23, 2015 Sheet 2 of 99

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW +1.8VALW +1VALW	+1.35V	+5VS +3VS +VCC_CORE +VCC_IO +VCC_SA +VCC_ST +VCC_STG +VGA_CORE +3VS_VGA +1.8VS_VGA +1.35VS_VGA +0.675VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	EC_ON2	EC_ON	SUSP#
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF

SMBUS Control Table

	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	Security ROM	LAN PHY	G sensor
EC_SMB_CK1 EC_SMB_DA1	IT8580F +3VL	X	V +3VALW	X	X	X	X	X	X	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8580F +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3V_PCH	X	X	X	V +3VALW_GS
PCH_SMB_CLK PCH_SMB_DATA	PCH +3V_PCH	X	X	V +3VS	X	X	X	V +5VS	V +3VS	X	X
PCH_SML0_CLK PCH_SML0_DAT	PCH +3V_PCH	X	X	X	X	X	X	X	X	V +3VALW	X

USB2 Port

Port	Device
1	JUSB2
2	JUSB3
3	Sub Board
4	Docking
5	Touch Panel
6	BT
7	CMOS
8	FP/Smart

USB3 Port

Port	Device
1	JUSB2
2	JUSB3
3	Sub Board
4	Docking
5	3D CCD(PCIE1)

PCIE Port

Port	Device
1	3D CCD(USB3)
2	X
3	WLAN
4	LAN
5	X
6	CardReader
7	X
8	X
9	GPU
10	GPU
11	GPU
12	GPU

SATA Port

Port	Device
1	HDD
2	ODD
3	X
4	X

Title: NOTE LIST

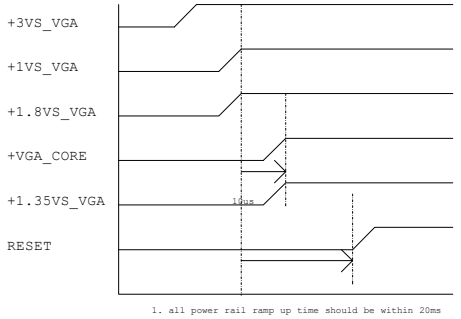
Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 3 of 99

VGA and DDR3 Voltage Rails (Litho XT 2GB DDR3)

20141227_S

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	N/A	
GPIO5	IN	-	GPIO5_AC_BATT
GPIO6	IN	-	GPIO6
GPIO7	OUT	N/A	
GPIO8	OUT	-	GPIO8_ROMSO
GPIO9	OUT	-	GPIO9_ROMSI
GPIO10	OUT	-	GPIO10_ROMSCK
GPIO11	OUT	N/A	
GPIO12	OUT	N/A	
GPIO13	OUT	N/A	
GPIO15	IN	N/A	SVI2_SVD
GPIO16	OUT	N/A	
GPIO17	OUT	N/A	
GPIO19	OUT	N/A	GPIO19_CTF
GPIO20	IN	IN	GPIO20
GPIO21	OUT	N/A	
GPIO22	OUT	N/A	GPIO22_ROMCSB
GPIO29	OUT	N/A	
GPIO30	OUT	N/A	



1. all power rail ramp up time should be within 20ms

	Device ID
JET-XT	0xFFFF

	setting	I2C Slave addrees ID
SMB_ALT_ADDR (ROM_SO Bit 1)	0	0xFF
	1	0xFF

BOM Structure Table

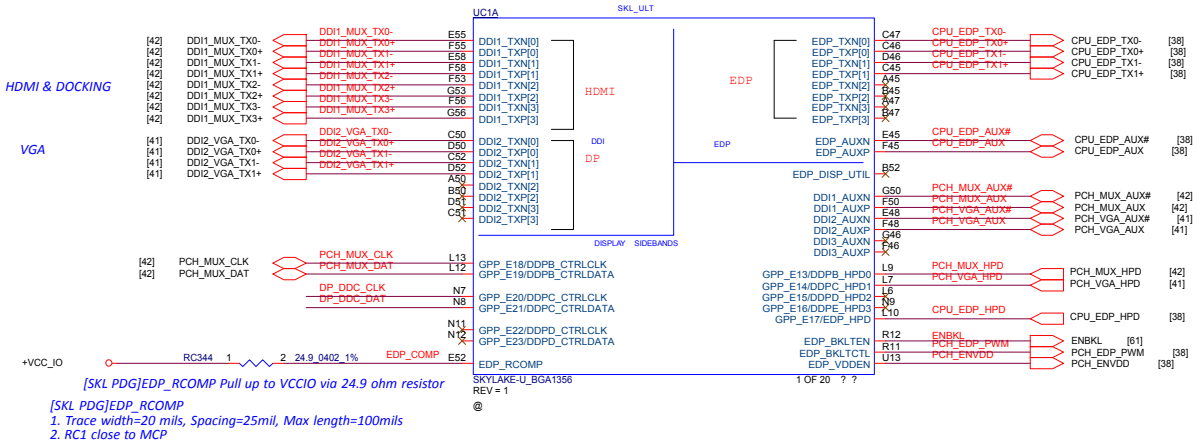
BOM Structure	NOTE
PCB@	For PCB load BOM
XDP@	Debug port
UMA@	UMA SKU ID
DIS@	Optimus SKU ID
DIMM2@	For DIMM2 function
DIMM1@	For DIMM1 function
VPRO@	For VPRO function
ME@	ME Connector
EMC@	For EMC function
EMC_2D@	For EMC function
EMC_NS@	For EMC function
RF_NS@	For RF function
S2G@	For VRAM Strap
CHA@	For VRAMA function
CHB@	For VRAMB function
RANKA@	GPU DDR5 Setting
X76@	GPU VRAM Setting
3DCCD@	3D Camera Setting
VGA@	VGA Setting
MUX@	MUX Setting
ODD@	ODD Setting
TPM@	Trusted Platform Module (TPM)
NVPRO@	For Non-VPRO function
MIRROR@	For mirror function

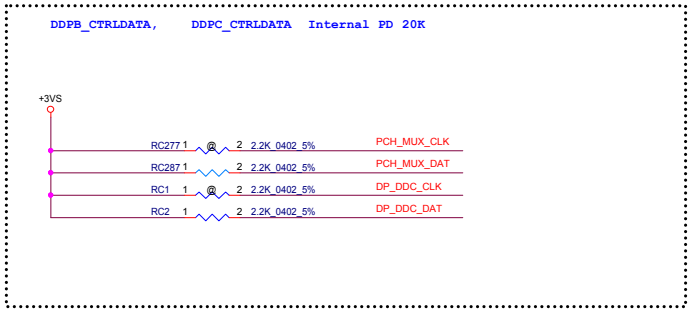
GPU		Litho XT 2GB DDR3	
FB Memory (DDR3L)		PS_3 (RV114)	PS_3 (RV117)
Samsung 1000MHz	K4W4G1646D-BC1A		
	256Mx16	PH 3.4K	PD 10K
Hynix 1000MHz	H5TC4G63AFR-11C		
	256Mx16	PH 4.75K	NC
Micro 1000MHz	MT41J256M16HA-093G		
	256Mx16	PH 3.24K	PD 5.62K

Title: VGA NOTE

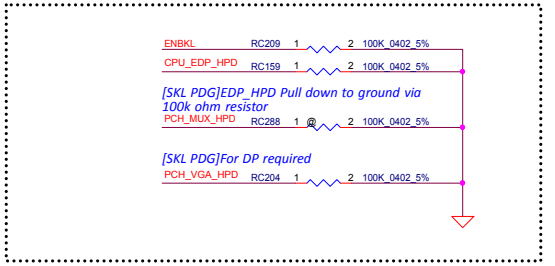
Size: Custom | Document Number: BE560 | Rev: 0.1

Date: Wednesday, September 23, 2015 | Sheet 4 of 99





DDPB_CTRLDATA	Port B Detected	This signal has an integrated weak pull-down (20 KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port B will be detected.
DDPC_CTRLDATA	Port C Detected	This signal has an integrated weak pull-down (20 KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port C will be detected.

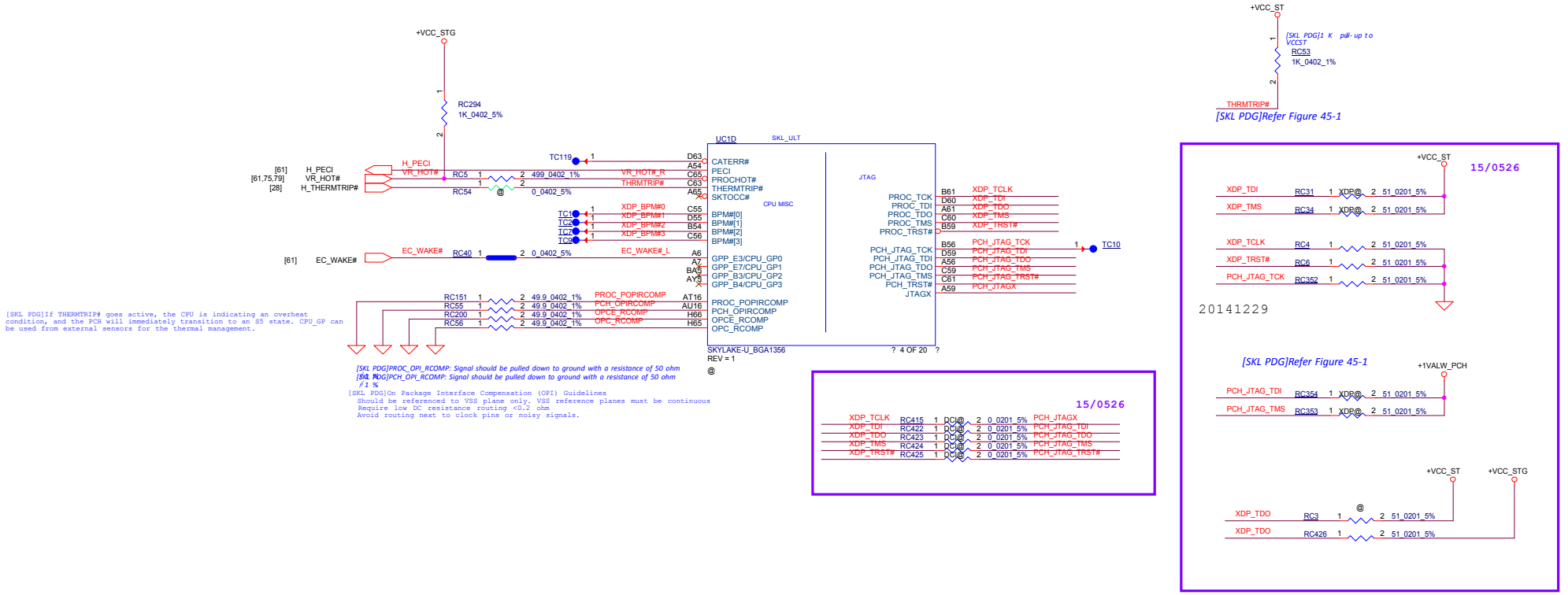


Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: SKL(1/16):DDI/EDP

Size: Custom | Document Number: BE560 | Rev: 0.1

Date: Wednesday, September 23, 2015 | Sheet 5 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: SKL(2/16):MISC/JTAG

Size	Document Number	Rev
Custom	AIVL2 NM-A351	0.1

Date: Wednesday, September 23, 2015 Sheet 6 of 99

[25] DDR_A_D[0..63]
[25] DDR_A_DQS#[0..7]
[25] DDR_A_DQS[0..7]
[25] DDR_A_MA[0..15]

UC1B

SKL_ULT

DDR_A_D0 AL71
DDR_A_D1 AL68
DDR_A_D2 AN68
DDR_A_D3 AN69
DDR_A_D4 AL70
DDR_A_D5 AL69
DDR_A_D6 AN70
DDR_A_D7 AN71
DDR_A_D8 AR70
DDR_A_D9 AR68
DDR_A_D10 AU71
DDR_A_D11 AU68
DDR_A_D12 AR71
DDR_A_D13 AR69
DDR_A_D14 AU70
DDR_A_D15 AU69
DDR_A_D16 BB65
DDR_A_D17 AW65
DDR_A_D18 AW63
DDR_A_D19 AY63
DDR_A_D20 BA65
DDR_A_D21 AY65
DDR_A_D22 BA63
DDR_A_D23 BB63
DDR_A_D24 BA61
DDR_A_D25 AW61
DDR_A_D26 BB59
DDR_A_D27 AW59
DDR_A_D28 BB61
DDR_A_D29 AY61
DDR_A_D30 BA59
DDR_A_D31 AY59
DDR_A_D32 AY39
DDR_A_D33 AW39
DDR_A_D34 AY37
DDR_A_D35 AW37
DDR_A_D36 BB39
DDR_A_D37 BA39
DDR_A_D38 BA37
DDR_A_D39 BB37
DDR_A_D40 AY35
DDR_A_D41 AW35
DDR_A_D42 AY33
DDR_A_D43 AW33
DDR_A_D44 BB35
DDR_A_D45 BA35
DDR_A_D46 BA33
DDR_A_D47 BB33
DDR_A_D48 AY31
DDR_A_D49 AW31
DDR_A_D50 AY29
DDR_A_D51 AW29
DDR_A_D52 BB31
DDR_A_D53 BA31
DDR_A_D54 BA29
DDR_A_D55 BB29
DDR_A_D56 AY27
DDR_A_D57 AW27
DDR_A_D58 AY25
DDR_A_D59 AW25
DDR_A_D60 BB27
DDR_A_D61 BA27
DDR_A_D62 BA25
DDR_A_D63 BB25

DDR0_DQ[0]
DDR0_DQ[1]
DDR0_DQ[2]
DDR0_DQ[3]
DDR0_DQ[4]
DDR0_DQ[5]
DDR0_DQ[6]
DDR0_DQ[7]
DDR0_DQ[8]
DDR0_DQ[9]
DDR0_DQ[10]
DDR0_DQ[11]
DDR0_DQ[12]
DDR0_DQ[13]
DDR0_DQ[14]
DDR0_DQ[15]
DDR0_DQ[16]/DDR0_DQ[32]
DDR0_DQ[17]/DDR0_DQ[33]
DDR0_DQ[18]/DDR0_DQ[34]
DDR0_DQ[19]/DDR0_DQ[35]
DDR0_DQ[20]/DDR0_DQ[36]
DDR0_DQ[21]/DDR0_DQ[37]
DDR0_DQ[22]/DDR0_DQ[38]
DDR0_DQ[23]/DDR0_DQ[39]
DDR0_DQ[24]/DDR0_DQ[40]
DDR0_DQ[25]/DDR0_DQ[41]
DDR0_DQ[26]/DDR0_DQ[42]
DDR0_DQ[27]/DDR0_DQ[43]
DDR0_DQ[28]/DDR0_DQ[44]
DDR0_DQ[29]/DDR0_DQ[45]
DDR0_DQ[30]/DDR0_DQ[46]
DDR0_DQ[31]/DDR0_DQ[47]
DDR0_DQ[32]/DDR1_DQ[0]
DDR0_DQ[33]/DDR1_DQ[1]
DDR0_DQ[34]/DDR1_DQ[2]
DDR0_DQ[35]/DDR1_DQ[3]
DDR0_DQ[36]/DDR1_DQ[4]
DDR0_DQ[37]/DDR1_DQ[5]
DDR0_DQ[38]/DDR1_DQ[6]
DDR0_DQ[39]/DDR1_DQ[7]
DDR0_DQ[40]/DDR1_DQ[8]
DDR0_DQ[41]/DDR1_DQ[9]
DDR0_DQ[42]/DDR1_DQ[10]
DDR0_DQ[43]/DDR1_DQ[11]
DDR0_DQ[44]/DDR1_DQ[12]
DDR0_DQ[45]/DDR1_DQ[13]
DDR0_DQ[46]/DDR1_DQ[14]
DDR0_DQ[47]/DDR1_DQ[15]
DDR0_DQ[48]/DDR1_DQ[32]
DDR0_DQ[49]/DDR1_DQ[33]
DDR0_DQ[50]/DDR1_DQ[34]
DDR0_DQ[51]/DDR1_DQ[35]
DDR0_DQ[52]/DDR1_DQ[36]
DDR0_DQ[53]/DDR1_DQ[37]
DDR0_DQ[54]/DDR1_DQ[38]
DDR0_DQ[55]/DDR1_DQ[39]
DDR0_DQ[56]/DDR1_DQ[40]
DDR0_DQ[57]/DDR1_DQ[41]
DDR0_DQ[58]/DDR1_DQ[42]
DDR0_DQ[59]/DDR1_DQ[43]
DDR0_DQ[60]/DDR1_DQ[44]
DDR0_DQ[61]/DDR1_DQ[45]
DDR0_DQ[62]/DDR1_DQ[46]
DDR0_DQ[63]/DDR1_DQ[47]

DDR0_CKN[0] AU53 SA_CLK_DDR#0 → SA_CLK_DDR#0 [25]
DDR0_CKP[0] AT53 SA_CLK_DDR0 → SA_CLK_DDR0 [25]
DDR0_CKN[1] AU55 SA_CLK_DDR#1 → SA_CLK_DDR#1 [25]
DDR0_CKP[1] AT55 SA_CLK_DDR1 → SA_CLK_DDR1 [25]

DDR0_CKE[0] BA56 DDRA_CKE0_DIMMA → DDRA_CKE0_DIMMA [25]
DDR0_CKE[1] BB56 DDRA_CKE1_DIMMA → DDRA_CKE1_DIMMA [25]
DDR0_CKE[2] AW56 X
DDR0_CKE[3] AY56 X

DDR0_CS#[0] AU45 DDRA_CS0_DIMMA# → DDRA_CS0_DIMMA# [25]
DDR0_CS#[1] AU43 DDRA_CS1_DIMMA# → DDRA_CS1_DIMMA# [25]
DDR0_ODT[0] AT45 DDRA_ODT0_DIMMA# → DDRA_ODT0_DIMMA# [25]
DDR0_ODT[1] AT43 DDRA_ODT1_DIMMA# → DDRA_ODT1_DIMMA# [25]

DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5] BA51 DDR_A_MA5
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9] BB54 DDR_A_MA9
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6] BA52 DDR_A_MA6
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8] AY52 DDR_A_MA8
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7] AW52 DDR_A_MA7
DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0] AY55 DDR_A_BS2 → DDR_A_BS2 [25]
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12] AW54 DDR_A_MA12
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11] BA54 DDR_A_MA11
DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT# BA55 DDR_A_MA15
DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1] AY54 DDR_A_MA14

DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13] AU46 DDR_A_MA13
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15] AU48 DDR_A_CAS# → DDR_A_CAS# [25]
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14] AT46 DDR_A_WE# → DDR_A_WE# [25]
DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16] AU50 DDR_A_RAS# → DDR_A_RAS# [25]
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0] AU52 DDR_A_BS0 → DDR_A_BS0 [25]
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2] AY51 DDR_A_MA2
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1] AT48 DDR_A_BS1 → DDR_A_BS1 [25]
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10] AT50 DDR_A_MA10
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1] BB50 DDR_A_MA1
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0] AY50 DDR_A_MA0
DDR0_MA[3] BA50 DDR_A_MA3
DDR0_MA[4] BB52 DDR_A_MA4

DDR0_DQSN[0] AM70 DDR_A_DQS#0
DDR0_DQSP[0] AM69 DDR_A_DQS0
DDR0_DQSN[1] AT69 DDR_A_DQS#1
DDR0_DQSP[1] AT70 DDR_A_DQS1
DDR0_DQSN[2]/DDR0_DQSN[4] BA64 DDR_A_DQS#2
DDR0_DQSP[2]/DDR0_DQSP[4] AY64 DDR_A_DQS2
DDR0_DQSN[3]/DDR0_DQSN[5] AY60 DDR_A_DQS#3
DDR0_DQSP[3]/DDR0_DQSP[5] BA60 DDR_A_DQS3
DDR0_DQSN[4]/DDR1_DQSN[0] BA38 DDR_A_DQS#4
DDR0_DQSP[4]/DDR1_DQSP[0] AY38 DDR_A_DQS4
DDR0_DQSN[5]/DDR1_DQSN[1] AY34 DDR_A_DQS#5
DDR0_DQSP[5]/DDR1_DQSP[1] BA34 DDR_A_DQS5
DDR0_DQSN[6]/DDR1_DQSN[4] BA30 DDR_A_DQS#6
DDR0_DQSP[6]/DDR1_DQSP[4] AY30 DDR_A_DQS6
DDR0_DQSN[7]/DDR1_DQSN[5] AY26 DDR_A_DQS#7
DDR0_DQSP[7]/DDR1_DQSP[5] BA26 DDR_A_DQS7

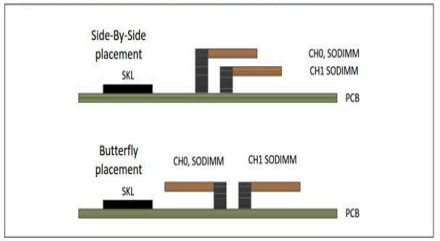
DDR0_ALERT# AW50 → 20141201
DDR0_PAR AT52 X

DDR_VREF_CA AY67 SM_DIMM_VREFCA → SM_DIMM_VREFCA [25]
DDR0_VREF_DQ AY68 SA_DIMM_VREFDQ → SA_DIMM_VREFDQ [25]
DDR1_VREF_DQ BA67 SB_DIMM_VREFDQ → SB_DIMM_VREFDQ [26]
DDR_VTT_CNTL AW67 DDR_PG_CTRL → DDR_PG_CTRL [25]

DDR CH - A

SKYLAKE-U_BGA1356
REV = 1
@
2 OF 20 ?

Figure 4-14. SKL U DDR3L/-RS SODIMM T3/8L 1L Placement Options

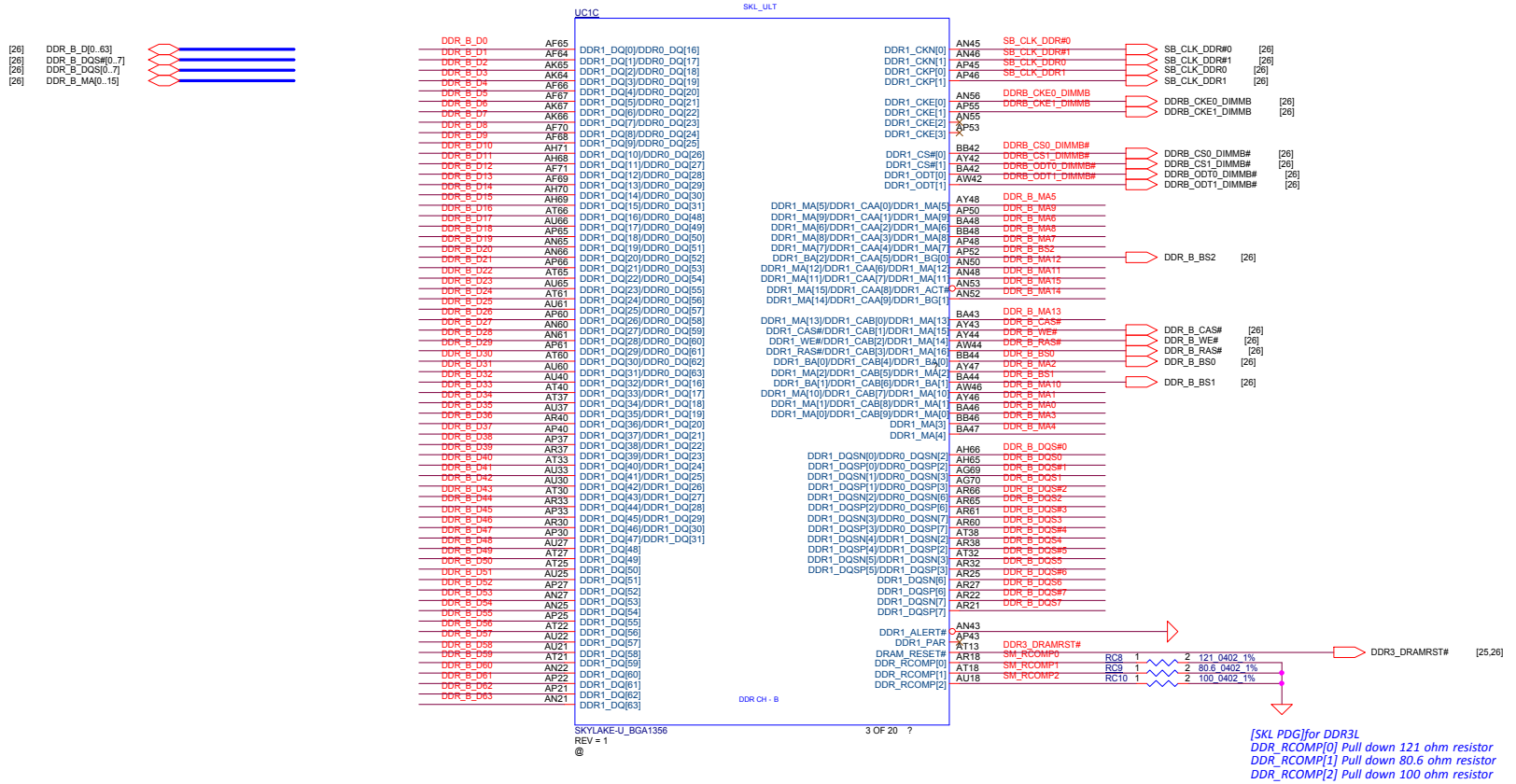


Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: SKL(3/16):DDR3L CH.A

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 7 of 99



[SKL PDG]for DDR3L
DDR_RCOMP[0] Pull down 121 ohm resistor
DDR_RCOMP[1] Pull down 80.6 ohm resistor
DDR_RCOMP[2] Pull down 100 ohm resistor

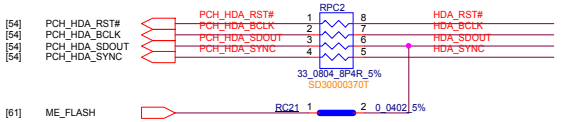
Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: **SKL(4/16):DDR3L CH.B**

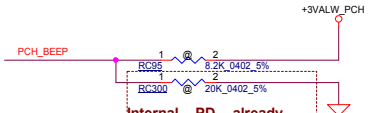
Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 Sheet 8 of 99

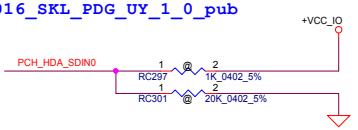
[SKL PDG]Manufacturing Mode Jumper
1. If strap is sampled low, the security measures defined in the flash Descriptor will be in effect (default)
2. If sampled high, the Flash Descriptor Security will be overridden.

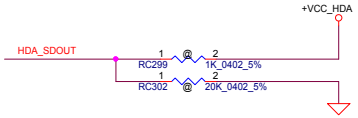


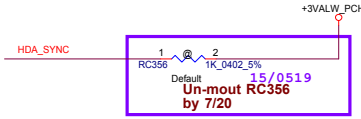
GPP_B14, Internal PD 20K
No Reboot on TCO
Timer expiration
pull-up to VCC3_3 through a 18.2K ±5% resistor to disable this capability



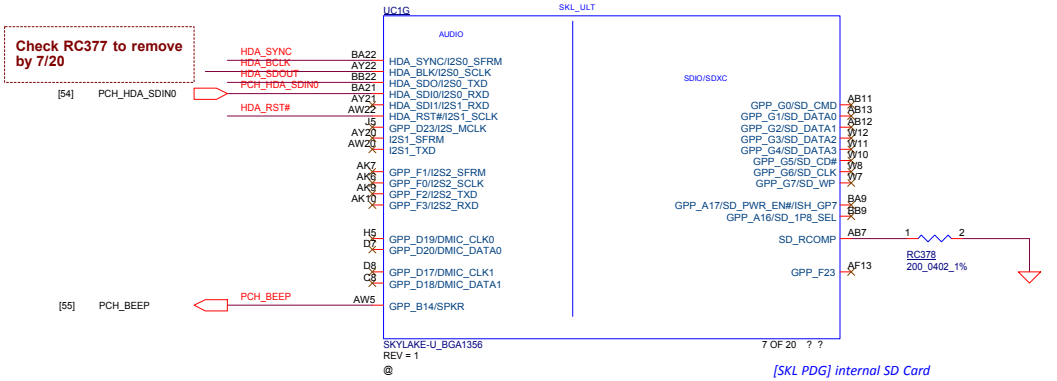
Processor Strapping
543016_543016_SKL_PDG_UY_1_0_pub
P780







Check RC377 to remove by 7/20



[SKL PDG] internal SD Card

Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: **SKL(5/16):HDA/SDIO**

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 9 of 99

20150514

RTC External Circuit

+RTCBATT

+RTCVCC

RC11 1 2 0_0402_5%

CC2 1U_0402_10V6-K

C8542 0.1U_0402_10V6-K

+RTCBATT, +RTCVCC
Trace width = 20mils

JCMOS, JME Setting, Need Under DDR Door

+RTCVCC

RC12 20K_0402_5% PCH_RTCRST# JCMOS1 @ CC1 1U_0402_10V6K

RC14 20K_0402_5% PCH_SRTCRST# JME1 @ CC5 1U_0402_10V6K

+3VS

RC165 UMA@ 10K_0402_5% CLKREQ_PCIE4_VGA#

RC166 DIS@ 10K_0402_5%

20141220

+3VS

RPC200 10K_0804_8P4R_5%

CLKREQ_PCIE2_WLAN#
CLKREQ_PCIE3_LAN#
CLKREQ_PCIE5_CR#

15/0519

+3VS

RC29 1 DIS@ 2 10K_0402_5%

RC32 1 UMA@ 2 10K_0402_5%

DISCRETE_PRESENCE

UC1J SKL_ULT

CLOCK SIGNALS

CLKOUT_PCIE_N0 D42
CLKOUT_PCIE_P0 C42
GPP_B5/SRCCLKREQ0# AR10

CLKOUT_PCIE_N1 B42
CLKOUT_PCIE_P1 A42
GPP_B6/SRCCLKREQ1# AT7

CLKOUT_PCIE_N2 D41
CLKOUT_PCIE_P2 C41
GPP_B7/SRCCLKREQ2# AT8

CLKOUT_PCIE_N3 D40
CLKOUT_PCIE_P3 C40
GPP_B8/SRCCLKREQ3# AT10

CLKOUT_PCIE_N4 B40
CLKOUT_PCIE_P4 A40
GPP_B9/SRCCLKREQ4# AU8

CLKOUT_PCIE_N5 E40
CLKOUT_PCIE_P5 E38
GPP_B10/SRCCLKREQ5# AU7

CLKOUT_ITPXDP_N F43
CLKOUT_ITPXDP_P E43

GPD8/SUSCLK BA17 SUSCLK_32K → SUSCLK_32K [50]

XTAL24_IN E37 PCH_XTAL24_IN
XTAL24_OUT E35 PCH_XTAL24_OUT

XCLK_BIASREF E42 DIFFCLK_BIASREF → RC379 2.7K_0402_1% → +1VALW

RTCX1 AM18 PCH_RTCX1
RTCX2 AM20 PCH_RTCX2

SRTCRST# AN18 PCH_SRTCRST#
RTCRST# AM16 PCH_RTCRST#

SKYLAKE-U_BGA1356
REV = 1
@
10 OF 20 ? ?

WLAN
[50] CLK_PCIE_WLAN# → CLK_PCIE_WLAN#
[50] CLK_PCIE_WLAN → CLK_PCIE_WLAN
[50] CLKREQ_PCIE2_WLAN# → CLKREQ_PCIE2_WLAN#

LAN
[47] CLK_PCIE_LAN# → CLK_PCIE_LAN#
[47] CLK_PCIE_LAN → CLK_PCIE_LAN
[47] CLKREQ_PCIE3_LAN# → CLKREQ_PCIE3_LAN#

VGA
[27] CLK_PCIE_VGA# → CLK_PCIE_VGA#
[27] CLK_PCIE_VGA → CLK_PCIE_VGA
[27] CLKREQ_PCIE4_VGA# → CLKREQ_PCIE4_VGA#

CR
[51] CLK_PCIE_CR# → CLK_PCIE_CR#
[51] CLK_PCIE_CR → CLK_PCIE_CR
[51] CLKREQ_PCIE5_CR# → CLKREQ_PCIE5_CR#

[SKL PDG]External pull-up resistor required if used for CLKREQ# functionality.

[SKL PDG]Used to set BIAS reference for differential clocks. Connect to a [RC379] 2.71K ∮ 0.5% precision resistor to 1.0v.

[SKL PDG]
1.Space > 15mils
2.No trace under crystal
3.Place on oppsosit side of MCP for temp inf l uence
4.The exact capacitor values forC1 and C2 must be based on the crystal maker recommendat i ons. Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.

RTC Crystal

PCH_RTCX1
RC13 10M_0402_5%
PCH_RTCX2
YC1 32.768KHZ_12.5PF_9H03200042
[SKL PDG]Max Crystal ESR = 50k Ohm.
CC3 5.6P_0402_50V8-D
CC4 5.6P_0402_50V8-D

[SKL PDG]
1.A 24 MHz crystal with crystal frequency tolerance and stability of +/-30 ppm
2.Two External Load Capacitors (Ce1 and Ce2)
3.A 1-Mohm bias resistor (Rf)

PCH_XTAL24_IN
PCH_XTAL24_OUT
RC30 1M_0402_5%
YC2 GND1 GND2
CC6 12P_0402_50V8-J
CC7 12P_0402_50V8-J
24MHZ_10PF_8Y24000011

Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

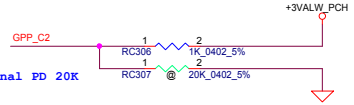
Title: **SKL(6/16):CLOCK SIGNALS**

Size: Custom | Document Number: **BE560** | Rev: 0.1

Date: Wednesday, September 23, 2015 | Sheet 10 of 99

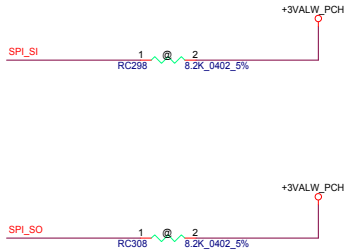
Functional Strap Definitions

L:Disable Intel ME Crypto TLS cipher suite (no confidentiality).
*H:Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).Support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



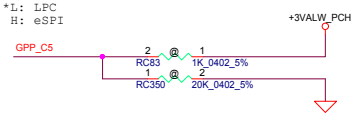
GPP_C2, Internal PD 20K

JTAG ODT

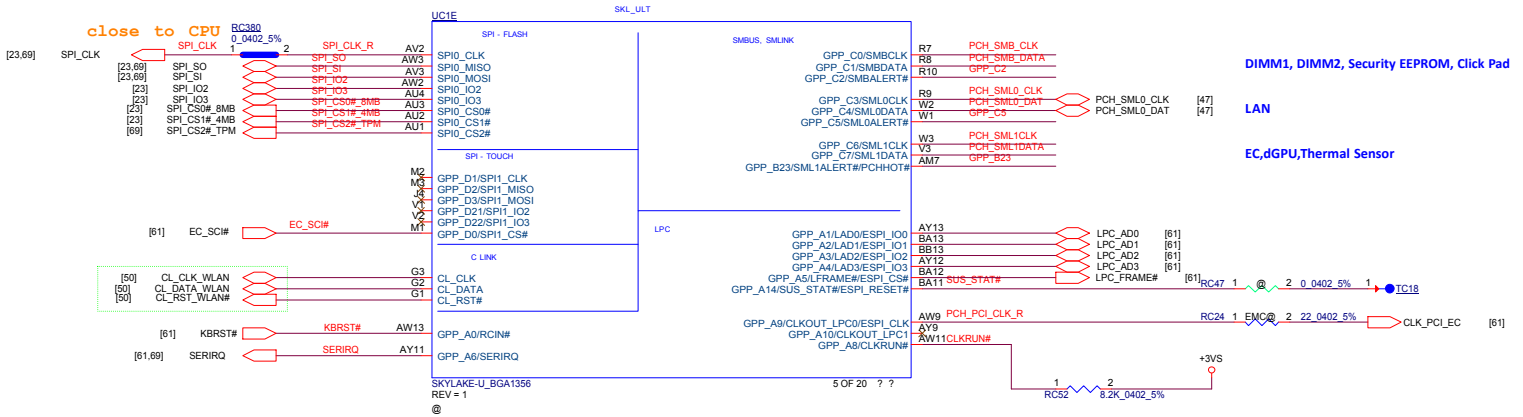


GPP_C5, Internal PD 20K

*L: LPC
H: eSPI



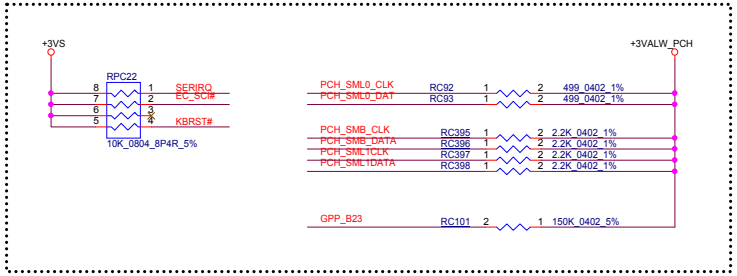
close to CPU

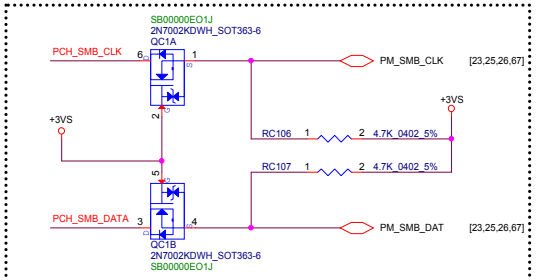


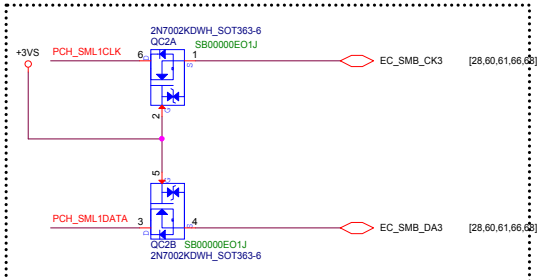
DIMM1, DIMM2, Security EEPROM, Click Pad

LAN

EC,dGPU,Thermal Sensor

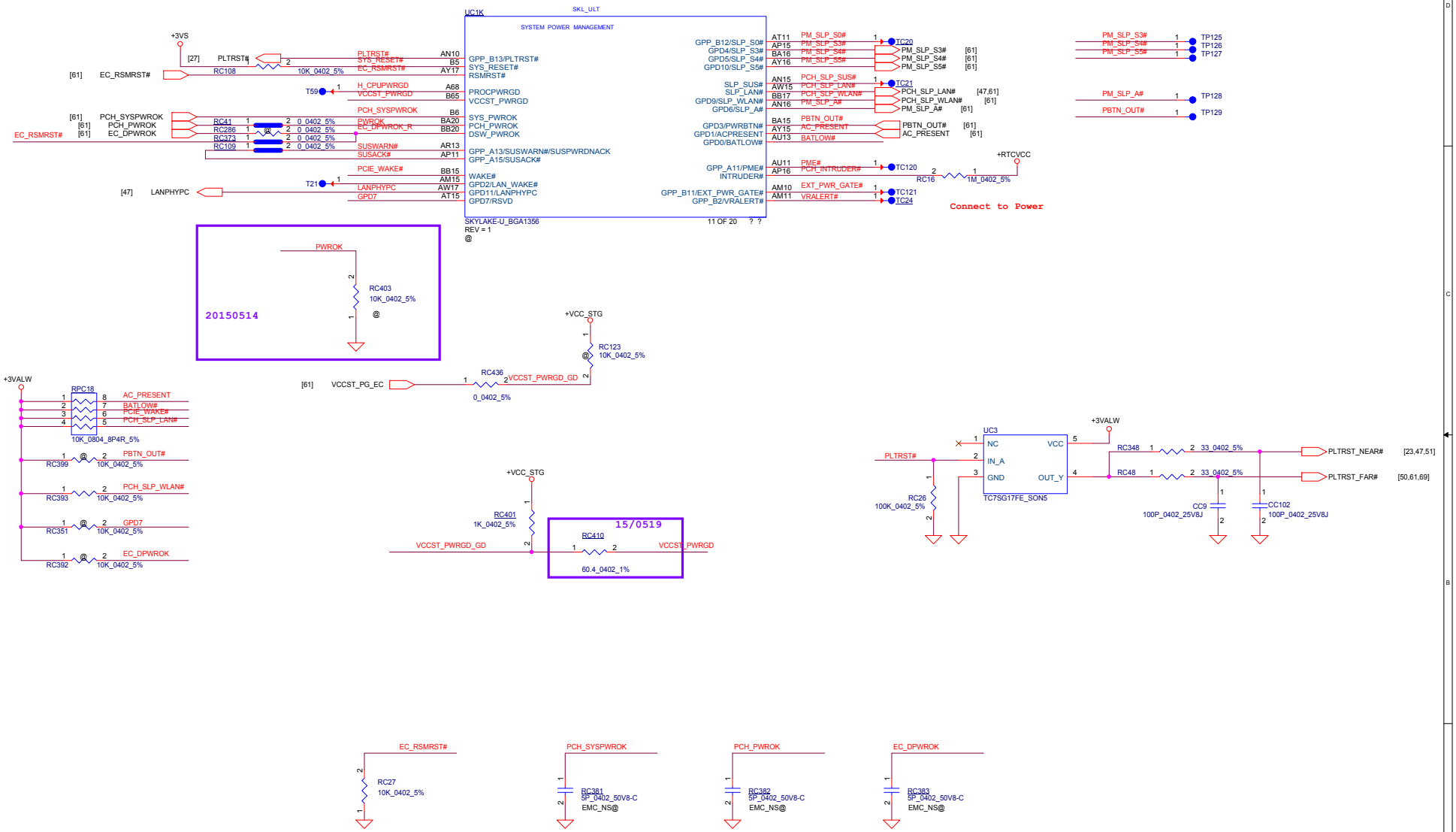






Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

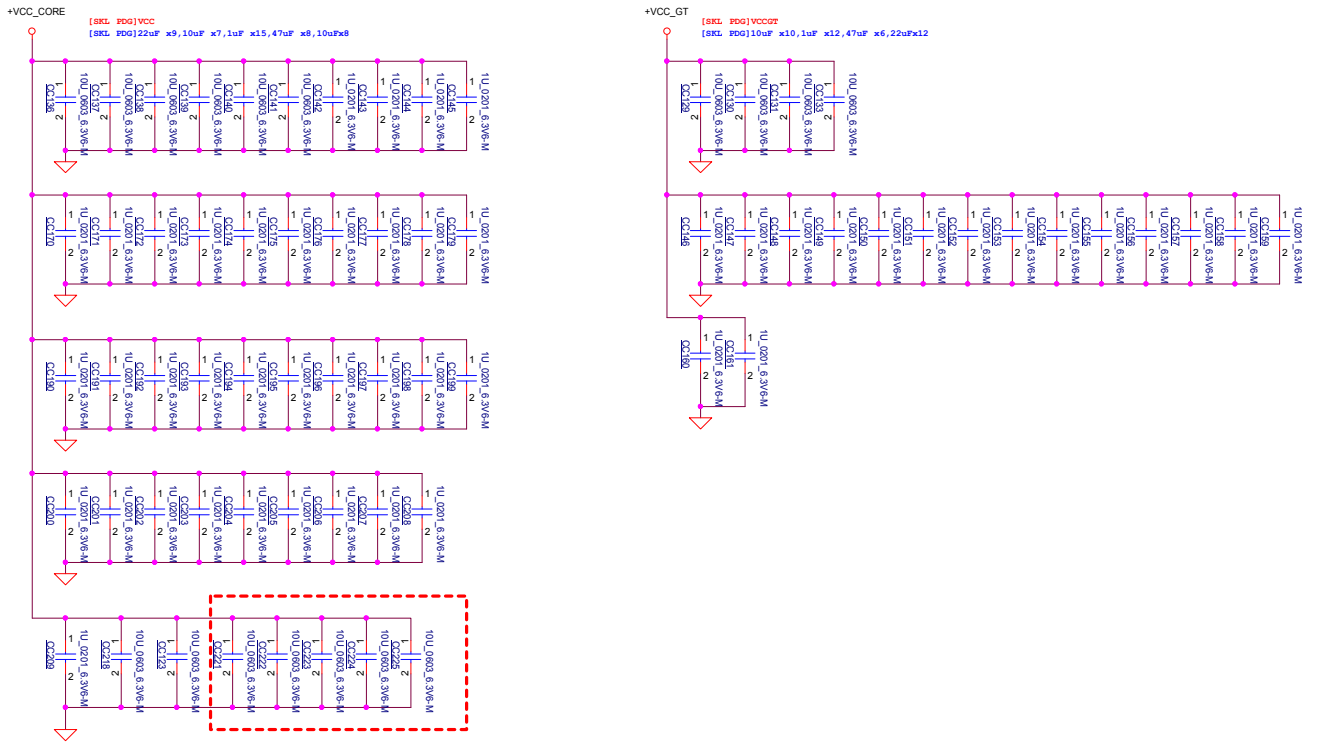
Title	SKL(7/16):LPC/SPI/SMBUS/CL	
Size: Custom	Document Number: BE560	Rev: 0.1
Date: Wednesday, September 23, 2015	Sheet 11 of 99	



Title: **SKL(8/16):SYSTEM PM**

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 12 of 99

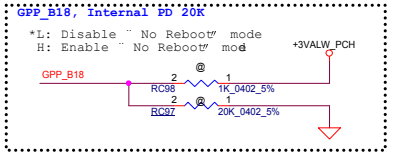


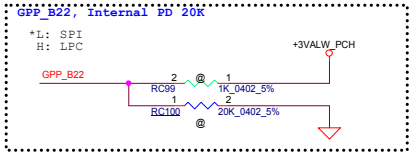
Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

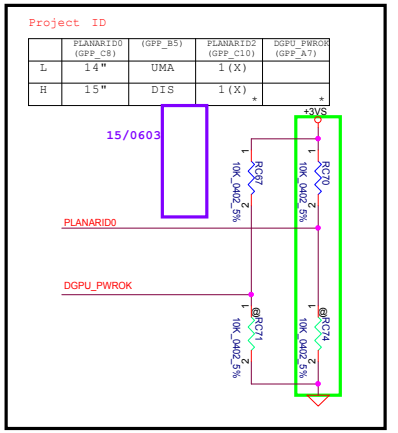
Title: **SKL(9/16):Decoupling**

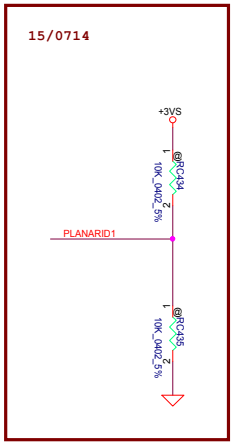
Size	Document Number	Rev
Custom	BE560	0.1

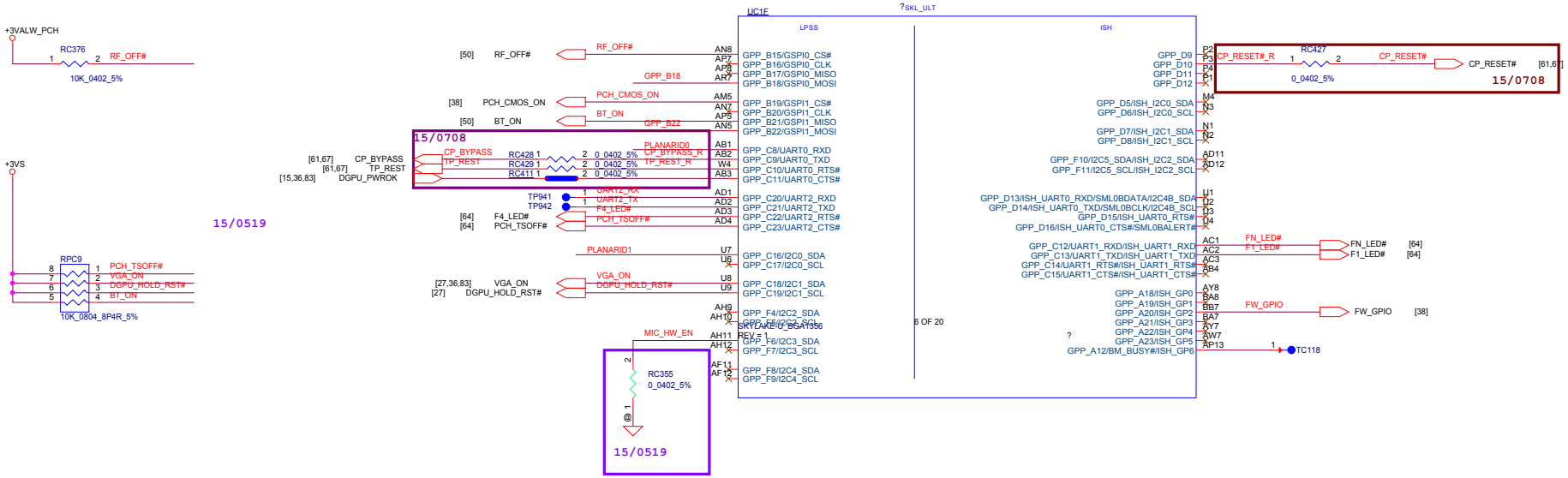
Date: Wednesday, September 23, 2015 | Sheet 13 of 99









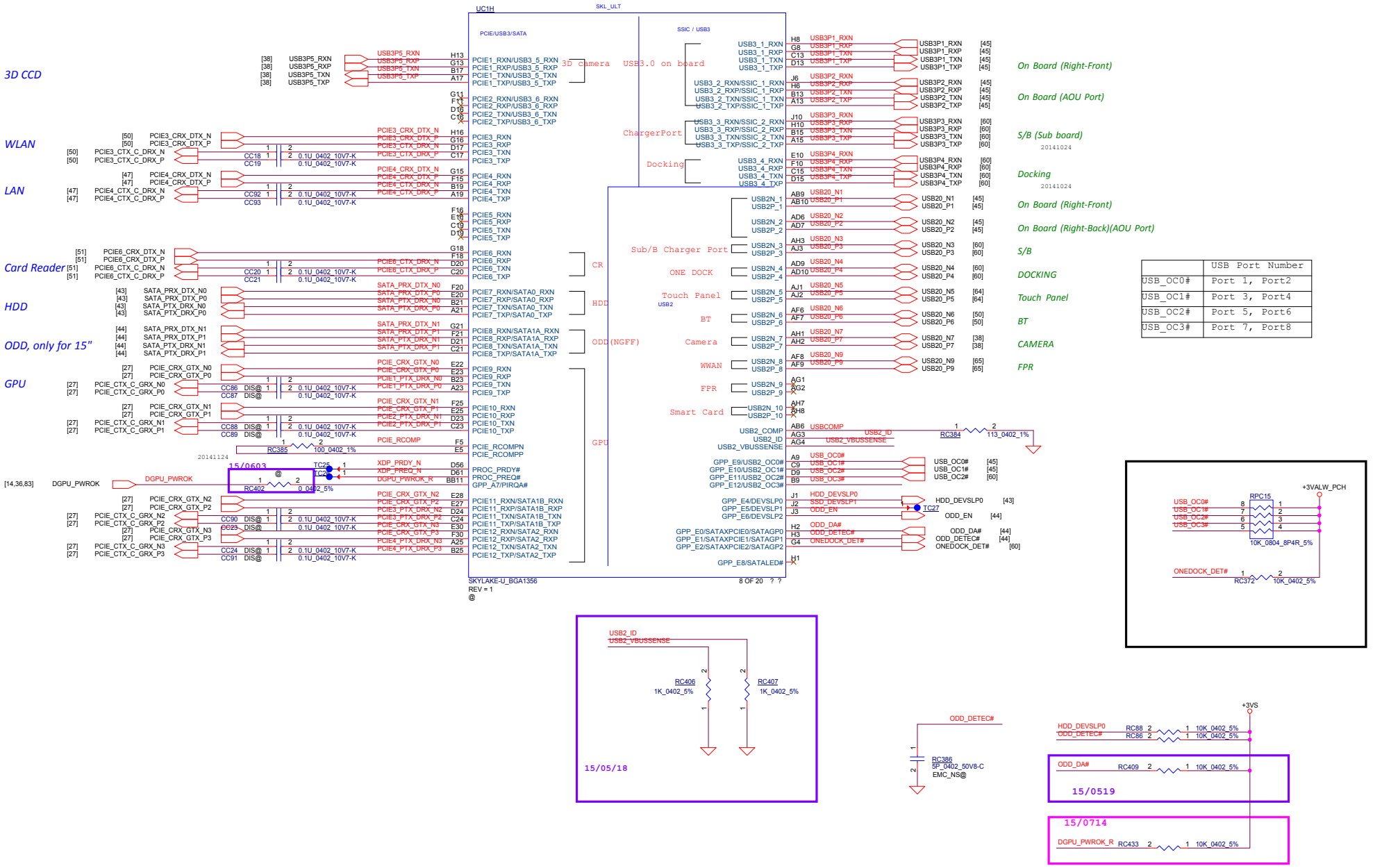


Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: SKL(10/16):GPIO/CPU/MISC

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 14 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

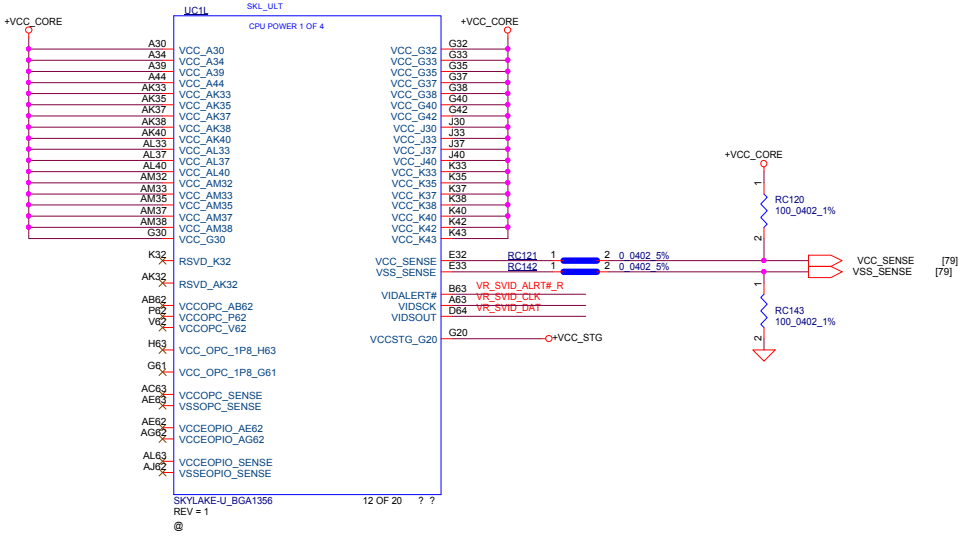
Title: SKL(11/16):PCIE/USB/SATA

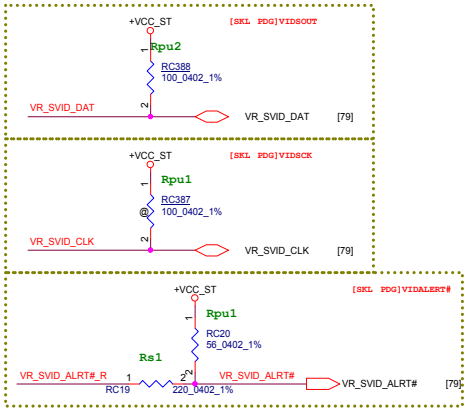
Size: Custom | Document Number: BE560 | Rev: 0.1

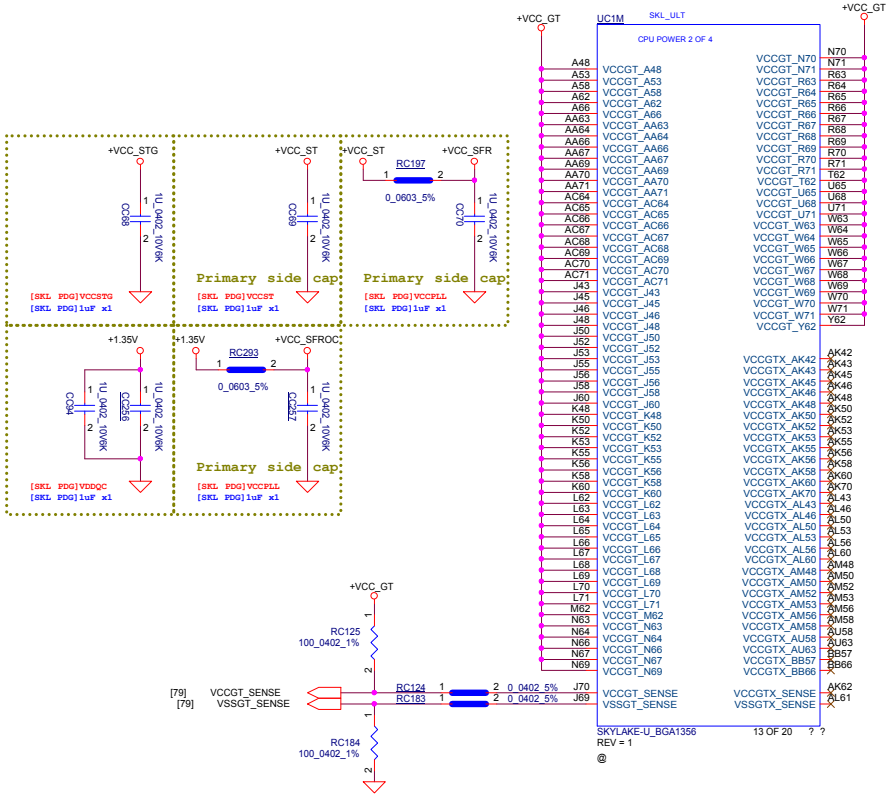
Date: Wednesday, September 23, 2015 | Sheet 15 of 99

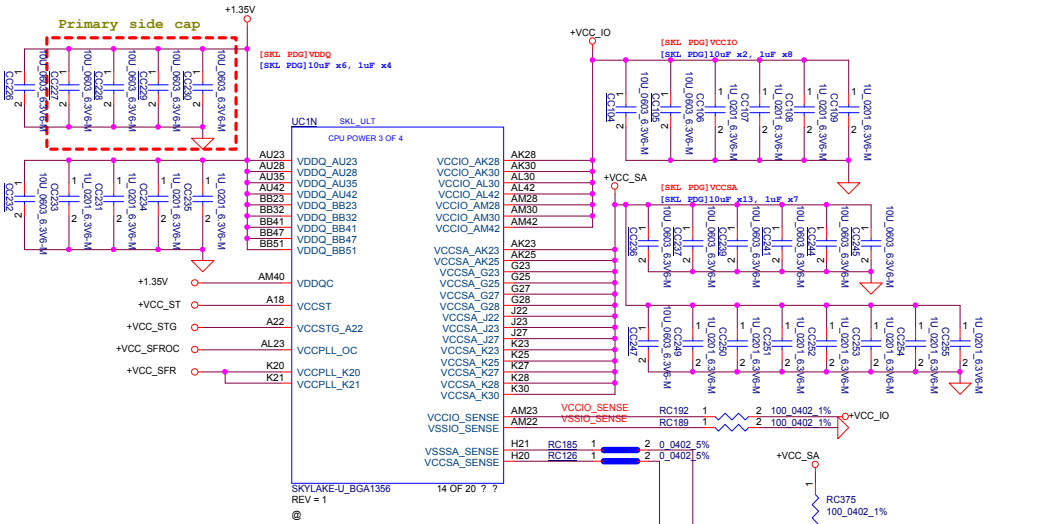
Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	







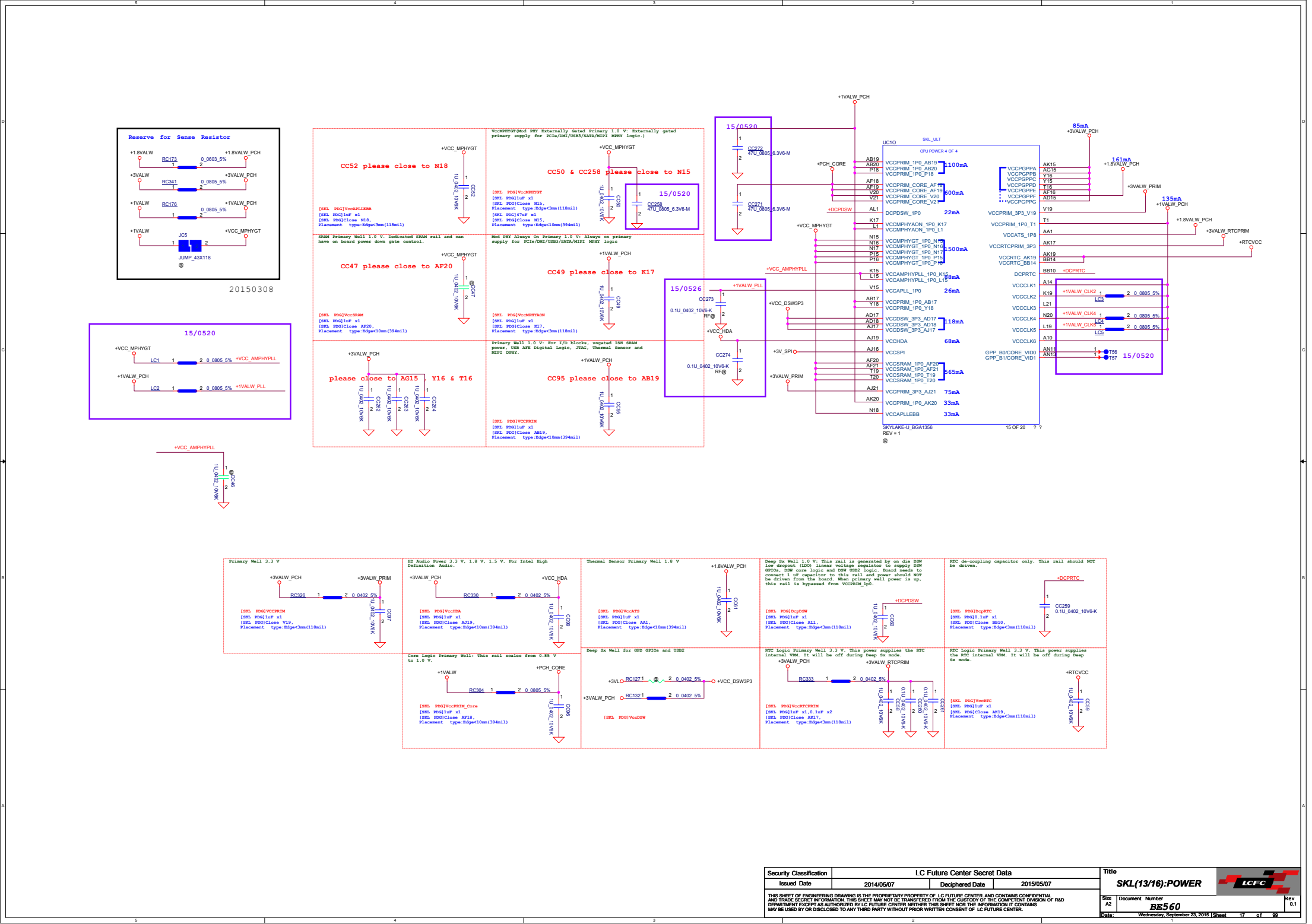


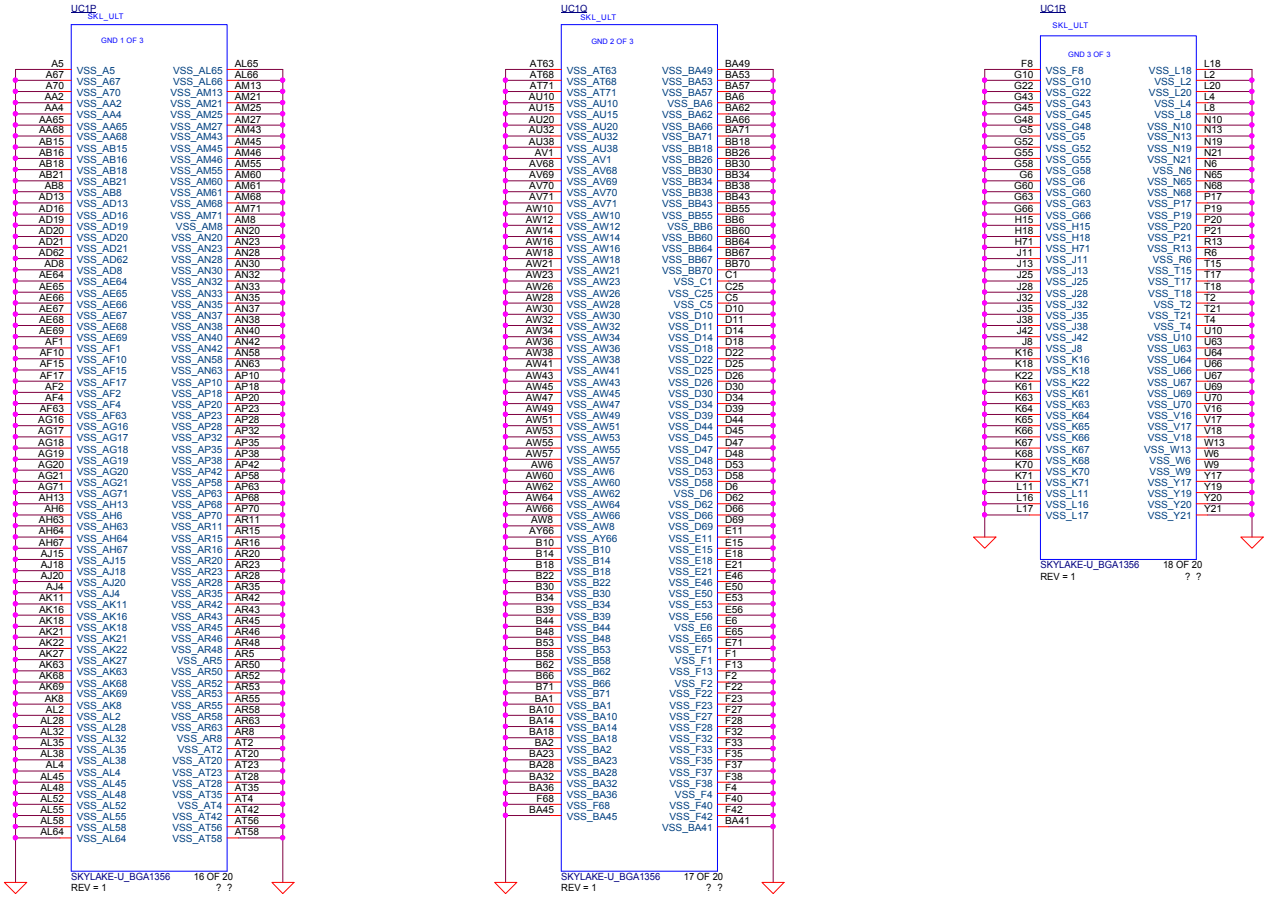
Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: **SKL(12/16):POWER**

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 16 of 99


Reserve for Sense Resistor
RC173 0_0603_5%
RC341 0_0805_5%
RC176 0_0805_5%
JC5 JUMP_43X118
20150308
15/0520
LC1 0_0805_5% +VCC_AMPHYPLL
LC2 0_0805_5% +1VALW_PLL
CC52 please close to N18
CC47 please close to AF20
CC50 & CC258 please close to N15
CC49 please close to K17
please close to AG15 Y16 & T16
CC95 please close to AB19
15/0526
UC1O SKL_ULT
CPU POWER 4 OF 4
SKYLAKE-U_BGA1356
REV = 1
15 OF 20
Primary Well 3.3 V
HD Audio Power 3.3 V, 1.8 V, 1.5 V. For Intel High Definition Audio.
Thermal Sensor Primary Well 1.8 V
Deep Sx Well 1.0 V: This rail is generated by on die DSW low dropout (LDO) linear voltage regulator to supply DSW GPIOs, DSW core logic and DSW USB2 logic. Board needs to connect 1 uF capacitor to this rail and power should NOT be driven from the board. When primary well power is up, this rail is bypassed from VCCPRIM_1p0.
RTC de-coupling capacitor only. This rail should NOT be driven.
Core Logic Primary Well: This rail scales from 0.85 V to 1.0 V.
Deep Sx Well for GPD GPIOs and USB2
RTC Logic Primary Well 3.3 V. This power supplies the RTC internal VRM. It will be off during Deep Sx mode.
RTC Logic Primary Well 3.3 V. This power supplies the RTC internal VRM. It will be off during Deep Sx mode.
Security Classification
LC Future Center Secret Data
Issued Date
2014/05/07
Deciphered Date
2015/05/07
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.
Title
SKL(13/16):POWER
Size A2
Document Number
BE560
Rev 0.1
Date: Wednesday, September 23, 2015
Sheet 17 of 99

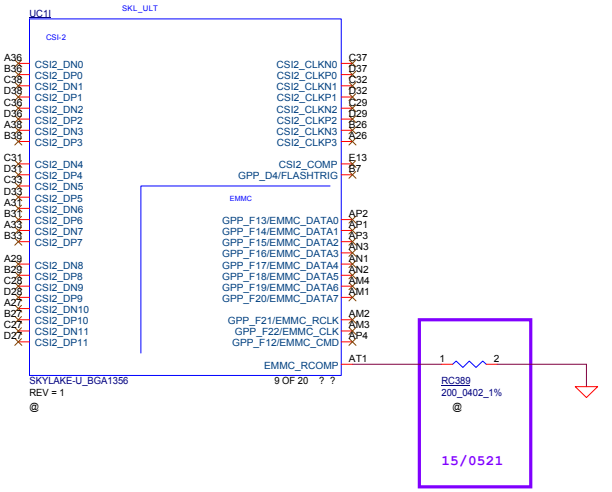


Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: **SKL(14/16):GND**

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 18 of 99

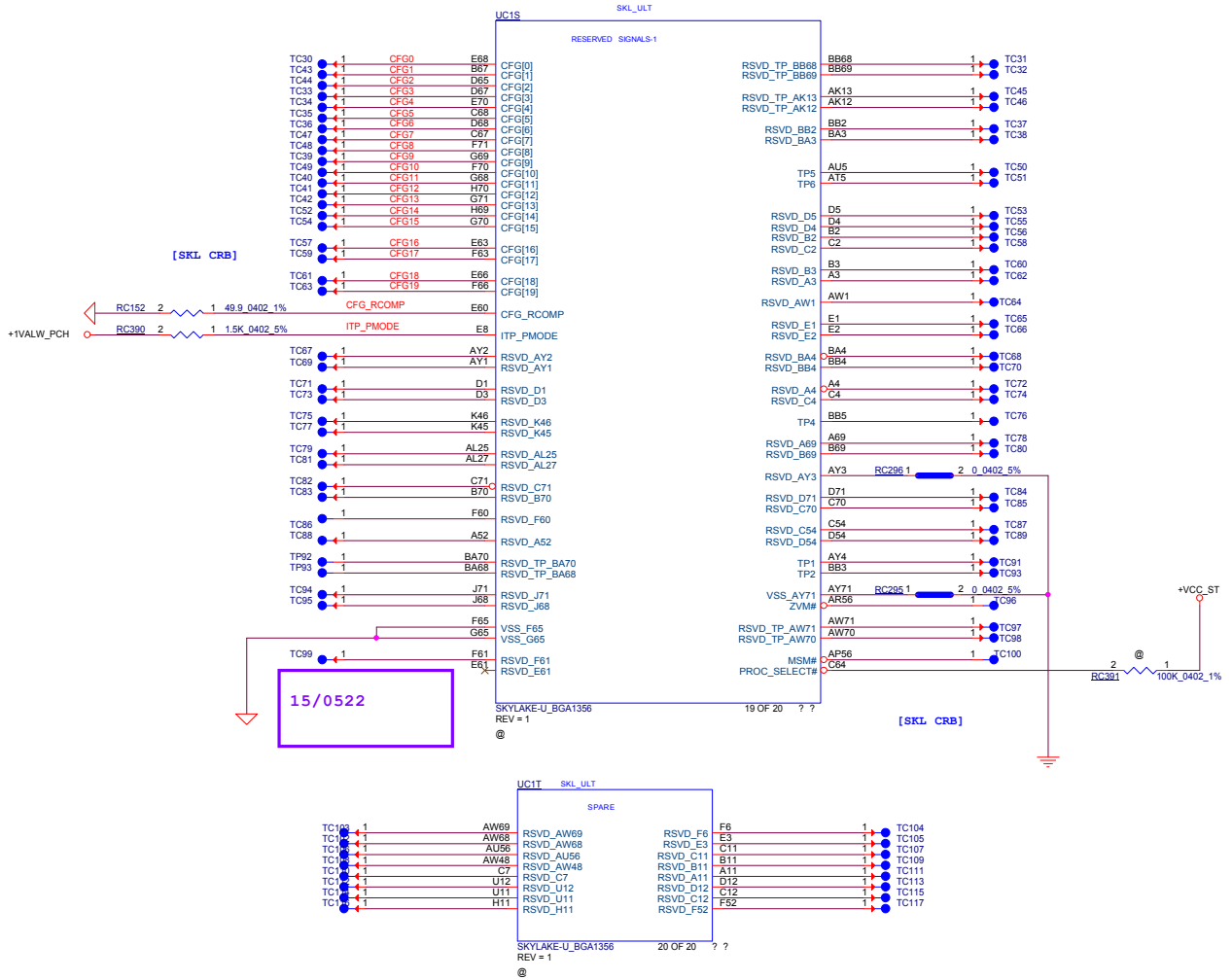


Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

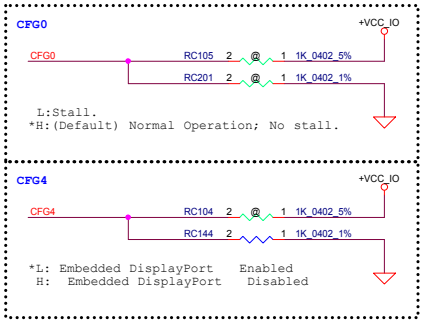
Title
SKL(15/16):CSI-2/EMMC

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 Sheet 19 of 99



[SKL EDS]



TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted **1 : No Stall** **0 : Stall**
CFG4 : eDP Enable **1 : Disabled** **0 : Enabled**
CFG9 : SVID Bus Communication **1 : Enabled** **0 : Disabled**

ZVM# state	VCCOPC
0V	0V
1V	1V

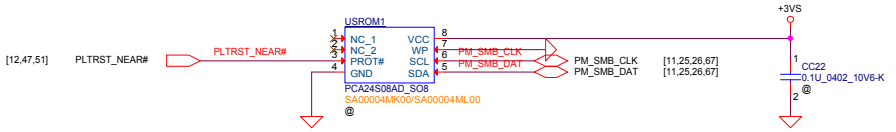
ZVM# state	MSM# state	VCCEOPIO
0V	X	0V
1V	0V	0.8V
1V	1V	1V

Title: SKL(16/16):CFG/RESERVED

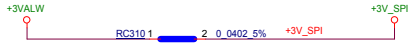
Size: Custom | Document Number: BE560 | Rev: 0.1

Date: Wednesday, September 23, 2015 | Sheet 20 of 99

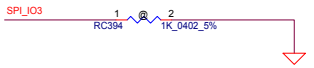
Security ROM



M3 Support + Intel LAN PHY / Wireless LAN Solut i on

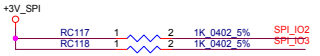


20141220

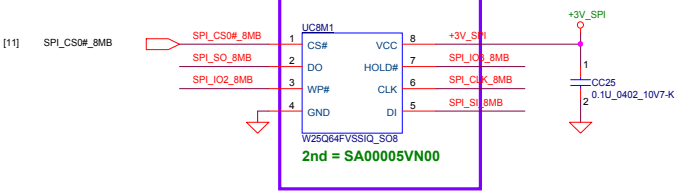


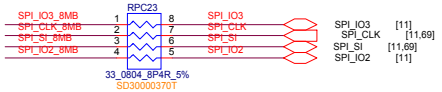
[SKL]SPI0_CS0#: SPI FLASH
SPI0_CS1#: SPI FLASH
SPI0_CS2#: SPI TPM

8MB(64Mb)



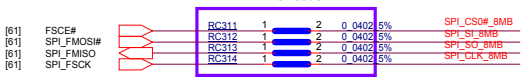
feedback to SDV rev..
15/0522





Near SPI ROM

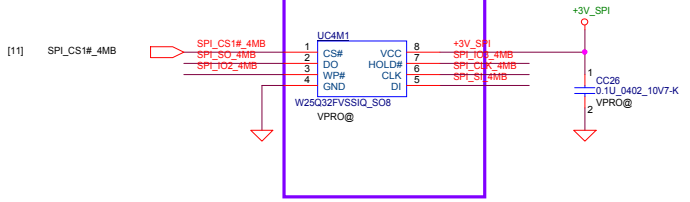
Mirror Code

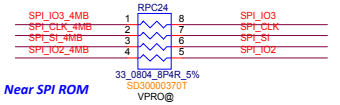


Close to SPI ROM (UC8M1).

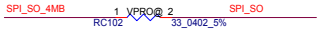
4MB(32Mb) for VPRO SKU

15/0525





Near SPI ROM

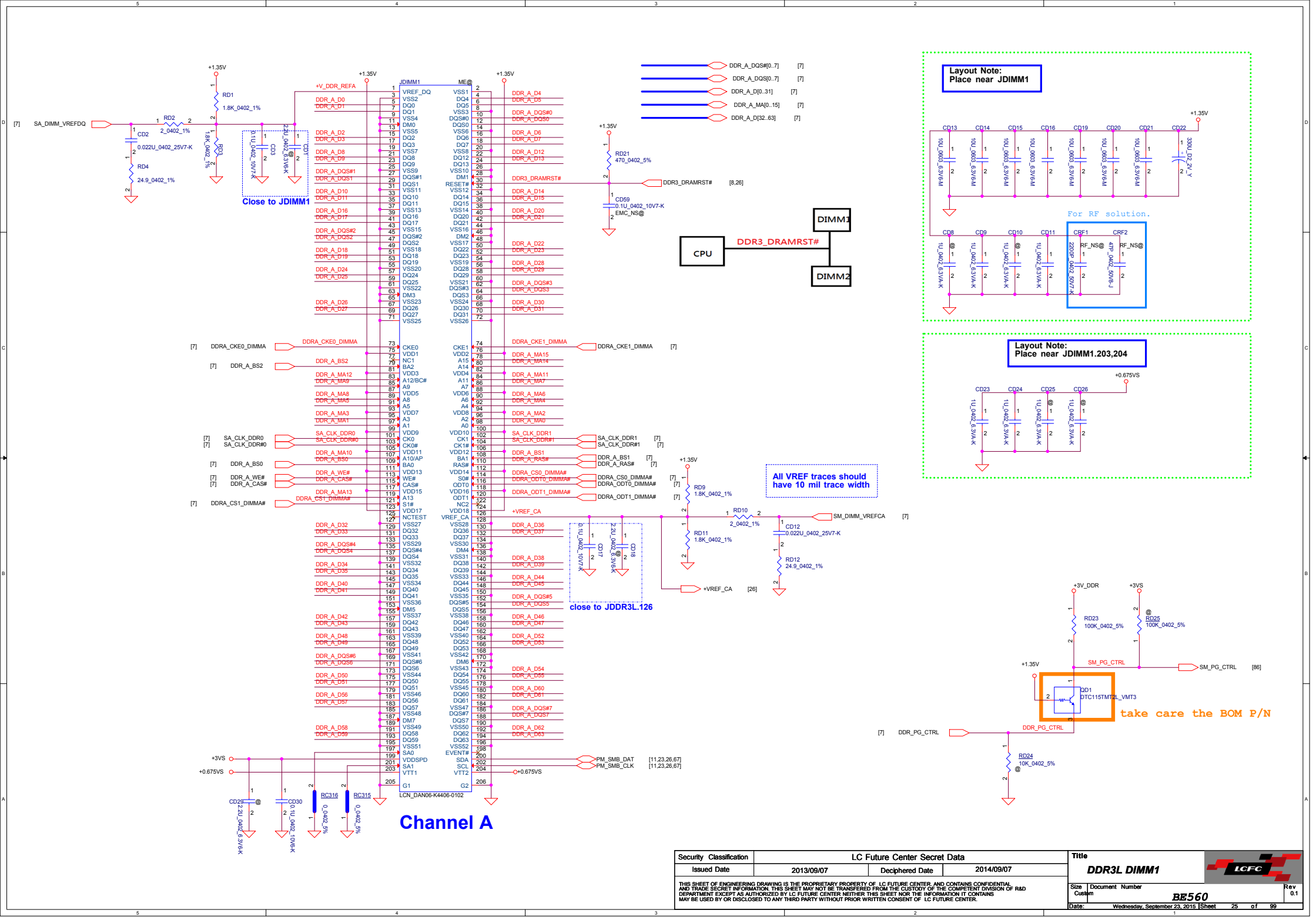


Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **SPI ROM**

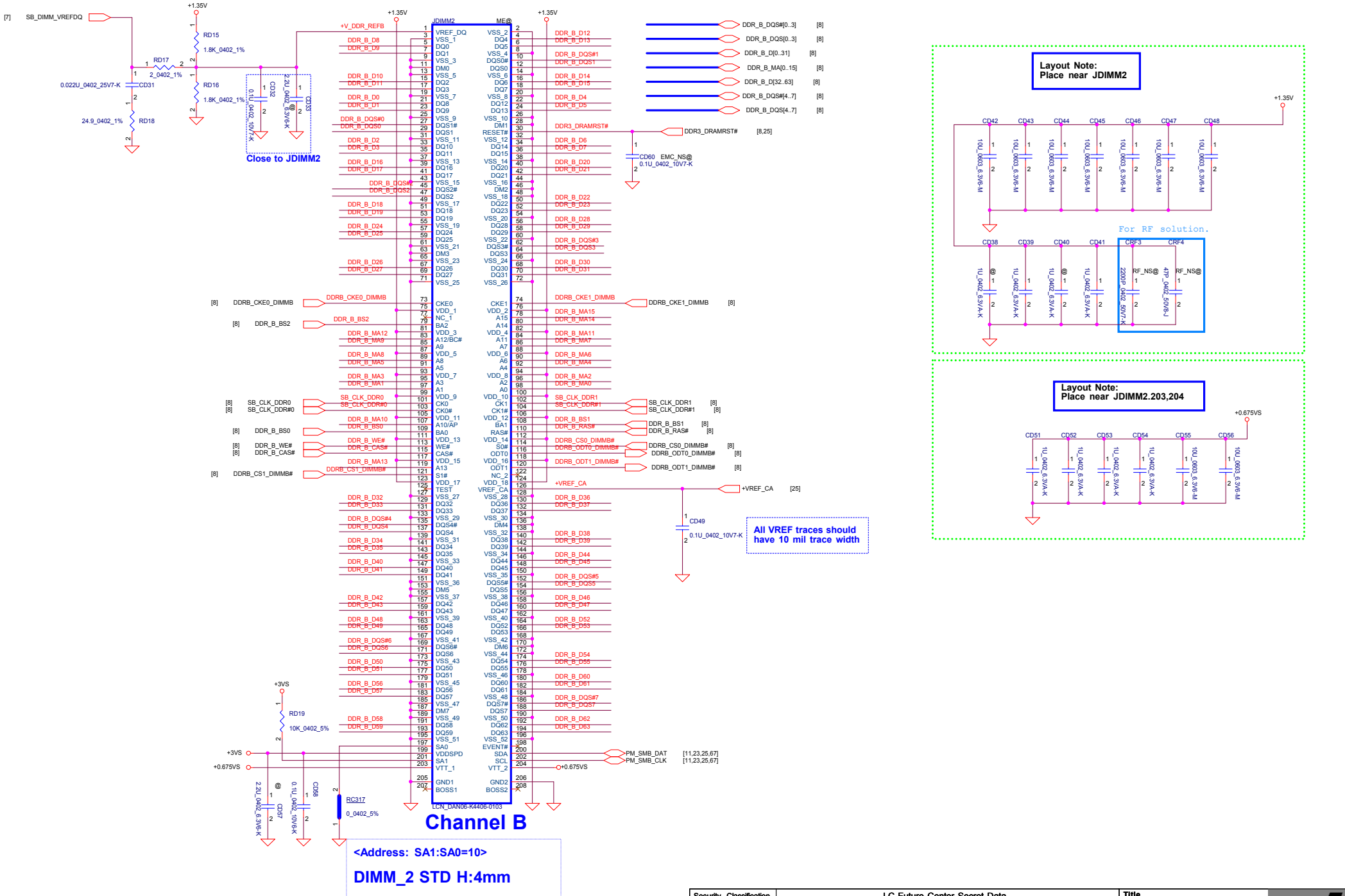
Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 23 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title	DDR3L DIMM1		
Size	Document Number		Rev
Custom	BE560		0.1
Date:	Wednesday, September 23, 2015	Sheet	25 of 99

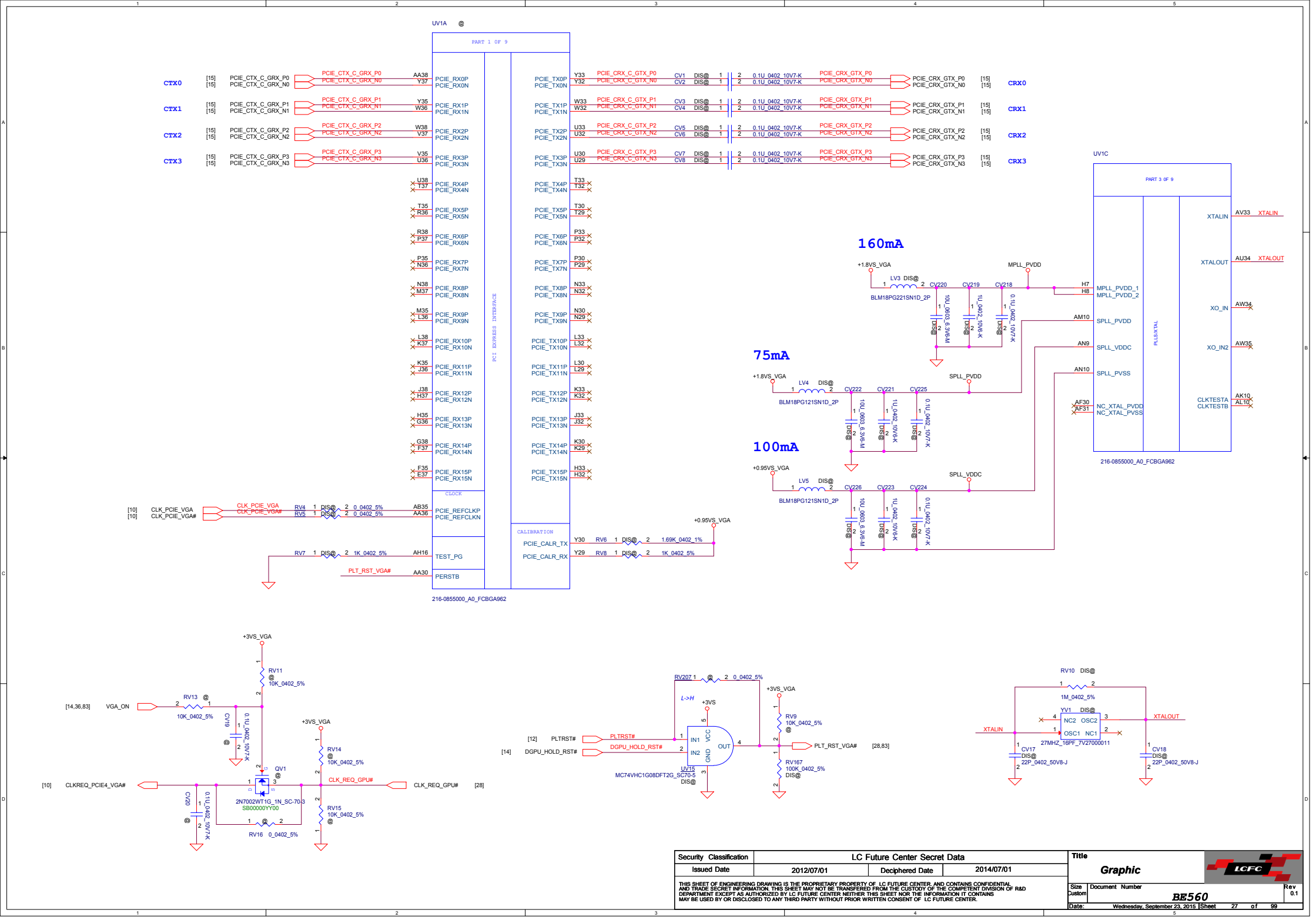


Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: DDR3L DIMM2

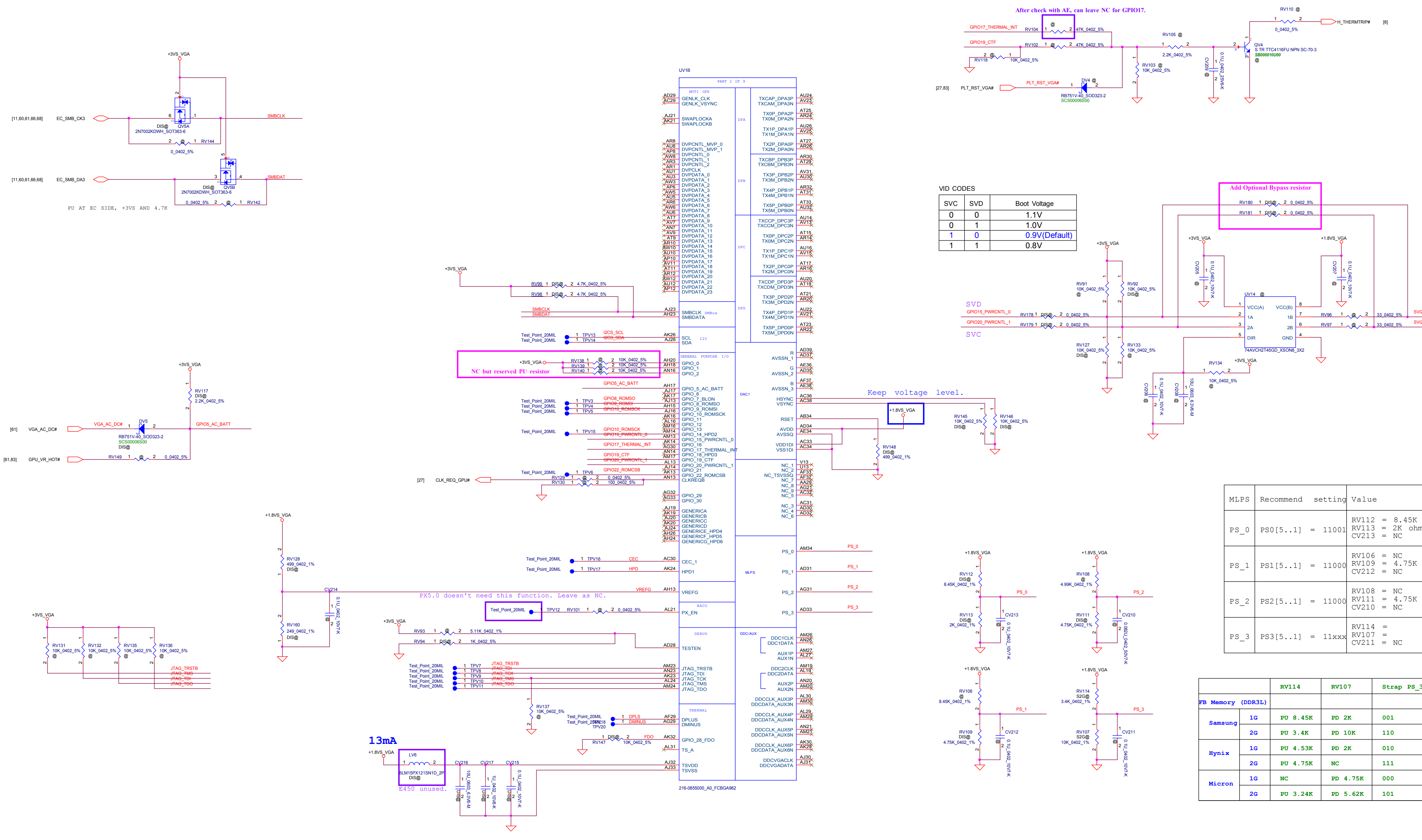
Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 Sheet 26 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	Graphic		
Size Custom	Document Number	BE560	Rev 0.1
Date:	Wednesday, September 23, 2015	Sheet 27 of 99	



VID CODES

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V

MLPS	Recommend setting	Value
PS_0	PS0[5..1] = 11001	RV112 = 8.45K ohm RV113 = 2K ohm CV213 = NC
PS_1	PS1[5..1] = 11000	RV106 = NC RV109 = 4.75K ohm CV212 = NC
PS_2	PS2[5..1] = 11000	RV108 = NC RV111 = 4.75K ohm CV210 = NC
PS_3	PS3[5..1] = 11xxx	RV114 = RV107 = CV211 = NC

		RV114	RV107	Strap PS_3[3..1]
FB Memory (DDR3L)				
Samsung	1G	PU 8.45K	PD 2K	001
	2G	PU 3.4K	PD 10K	110
Hynix	1G	PU 4.53K	PD 2K	010
	2G	PU 4.75K	NC	111
Micron	1G	NC	PD 4.75K	000
	2G	PU 3.24K	PD 5.62K	101

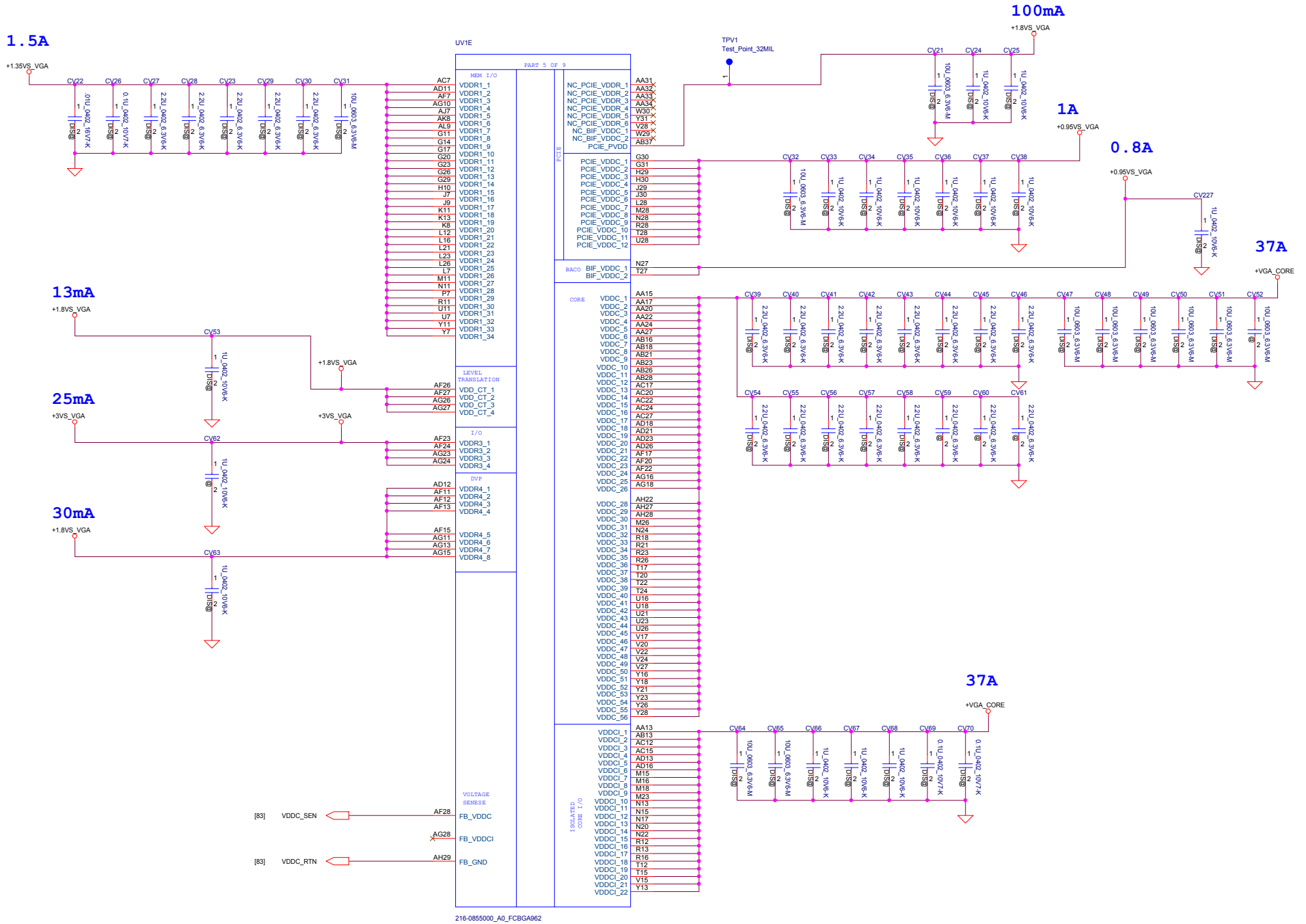
Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: Graphic

LCFC

Size: D | Document Number: BE560 | Rev: 0.1

Date: Wednesday, September 23, 2015 | Sheet 28 of 99

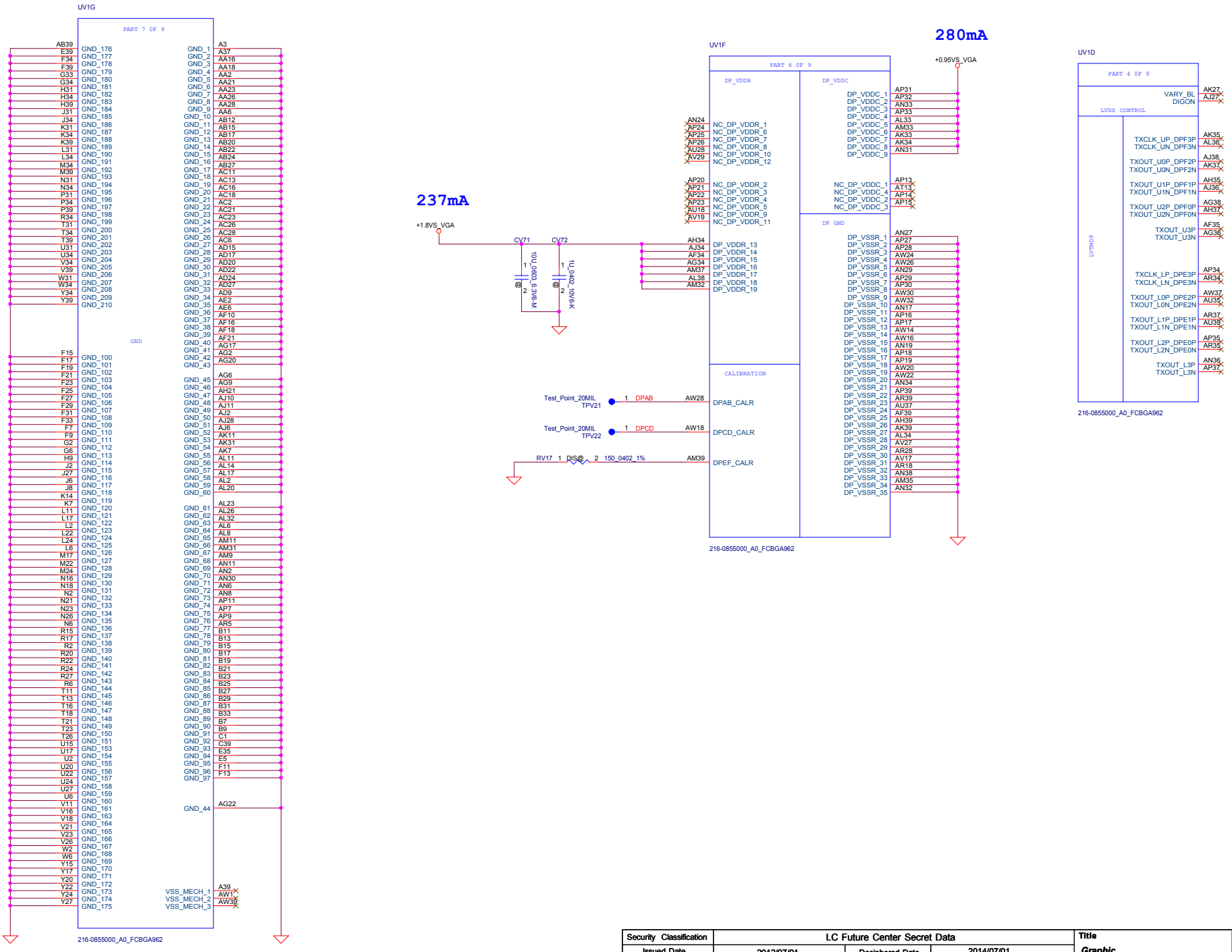


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: Graphic

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 29 of 99

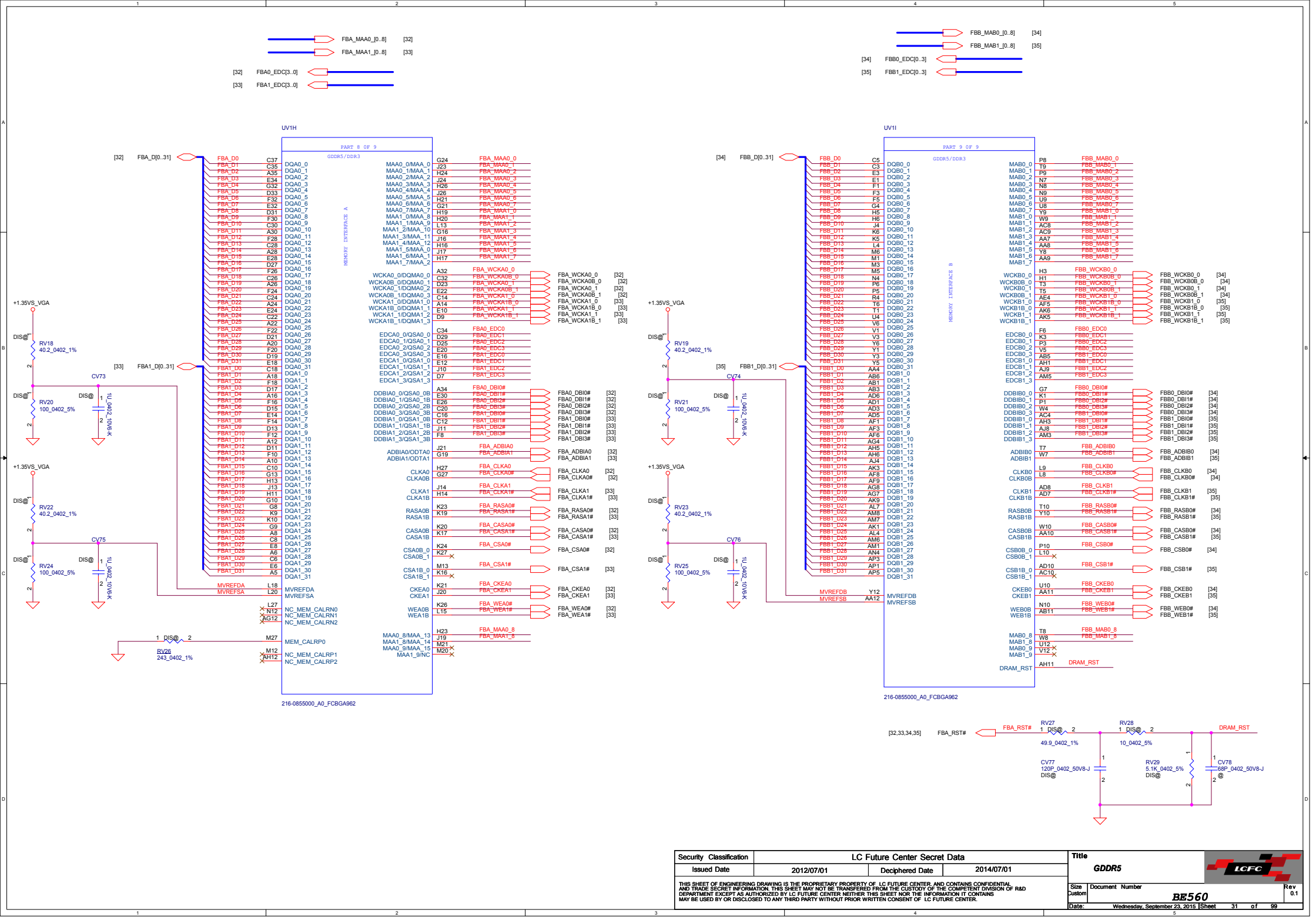


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

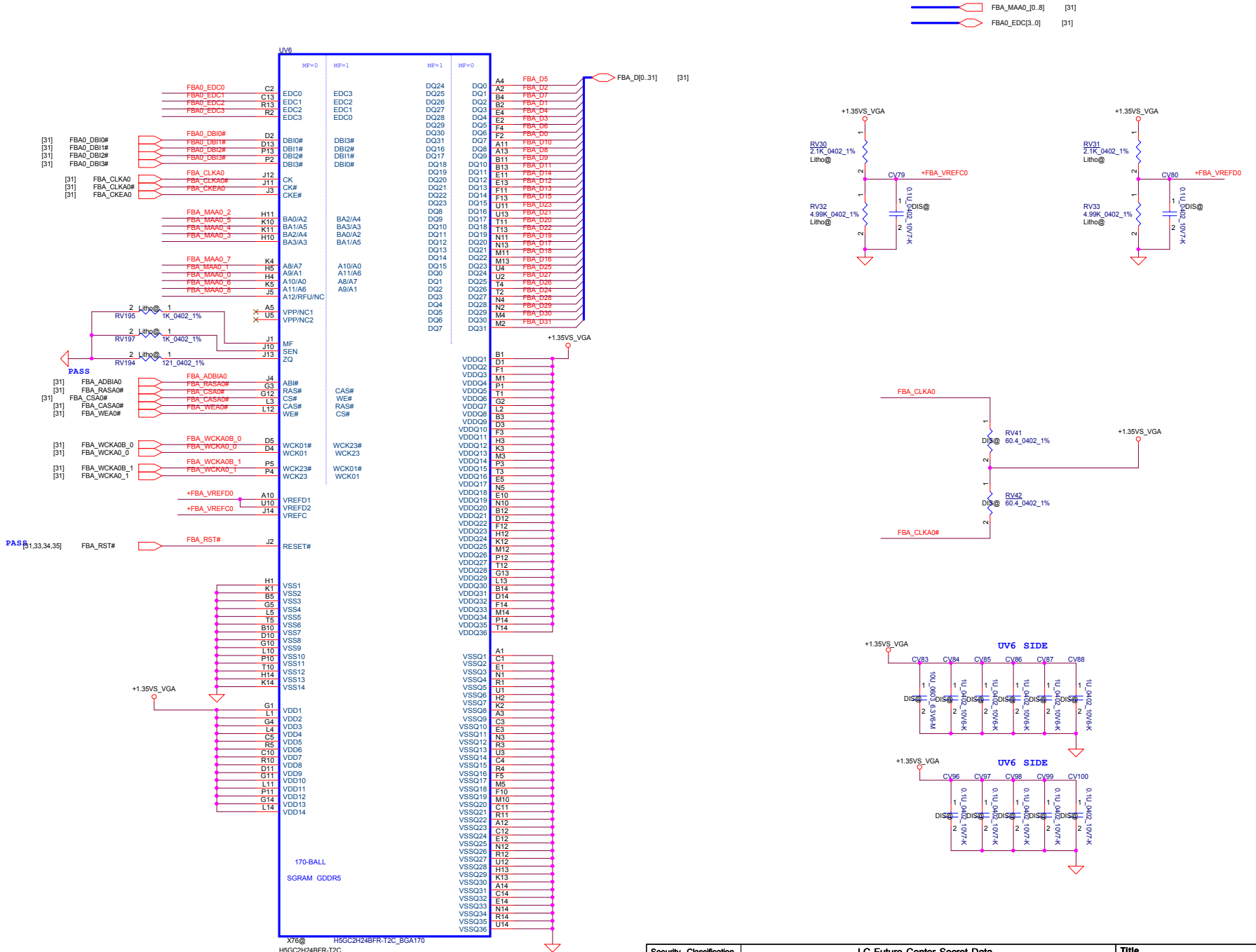
Title: Graphic

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 30 of 99


FBA_MAA0_[0..8] [32]
FBA_MAA1_[0..8] [33]
[32] FBA0_EDC[3..0]
[33] FBA1_EDC[3..0]
FBB_MAB0_[0..8] [34]
FBB_MAB1_[0..8] [35]
[34] FBB0_EDC[0..3]
[35] FBB1_EDC[0..3]
UV1H
PART 8 OF 9
GDDR5/DDR3
MEMORY INTERFACE A
[32] FBA_D[0..31]
[33] FBA1_D[0..31]
FBA_D0 C37
FBA_D1 C35
FBA_D2 A35
FBA_D3 E34
FBA_D4 G32
FBA_D5 D33
FBA_D6 F32
FBA_D7 E32
FBA_D8 D31
FBA_D9 F30
FBA_D10 C30
FBA_D11 A30
FBA_D12 F28
FBA_D13 C28
FBA_D14 A28
FBA_D15 E28
FBA_D16 D27
FBA_D17 F26
FBA_D18 C26
FBA_D19 A26
FBA_D20 F24
FBA_D21 C24
FBA_D22 A24
FBA_D23 E24
FBA_D24 C22
FBA_D25 A22
FBA_D26 F22
FBA_D27 D21
FBA_D28 A20
FBA_D29 F20
FBA_D30 D19
FBA_D31 E18
FBA1_D0 C18
FBA1_D1 A18
FBA1_D2 F18
FBA1_D3 D17
FBA1_D4 A16
FBA1_D5 F16
FBA1_D6 D15
FBA1_D7 E14
FBA1_D8 F14
FBA1_D9 D13
FBA1_D10 F12
FBA1_D11 A12
FBA1_D12 D11
FBA1_D13 F10
FBA1_D14 A10
FBA1_D15 C10
FBA1_D16 G13
FBA1_D17 H13
FBA1_D18 J13
FBA1_D19 H11
FBA1_D20 G10
FBA1_D21 G8
FBA1_D22 K9
FBA1_D23 K10
FBA1_D24 G9
FBA1_D25 A8
FBA1_D26 C8
FBA1_D27 E8
FBA1_D28 A6
FBA1_D29 C6
FBA1_D30 E6
FBA1_D31 A5
DQA0_0 DQA0_1 DQA0_2 DQA0_3 DQA0_4 DQA0_5 DQA0_6 DQA0_7 DQA0_8 DQA0_9 DQA0_10 DQA0_11 DQA0_12 DQA0_13 DQA0_14 DQA0_15 DQA0_16 DQA0_17 DQA0_18 DQA0_19 DQA0_20 DQA0_21 DQA0_22 DQA0_23 DQA0_24 DQA0_25 DQA0_26 DQA0_27 DQA0_28 DQA0_29 DQA0_30 DQA0_31
DQA1_0 DQA1_1 DQA1_2 DQA1_3 DQA1_4 DQA1_5 DQA1_6 DQA1_7 DQA1_8 DQA1_9 DQA1_10 DQA1_11 DQA1_12 DQA1_13 DQA1_14 DQA1_15 DQA1_16 DQA1_17 DQA1_18 DQA1_19 DQA1_20 DQA1_21 DQA1_22 DQA1_23 DQA1_24 DQA1_25 DQA1_26 DQA1_27 DQA1_28 DQA1_29 DQA1_30 DQA1_31
MAA0_0/MAA_0 G24
MAA0_1/MAA_1 J23
MAA0_2/MAA_2 H24
MAA0_3/MAA_3 J24
MAA0_4/MAA_4 H26
MAA0_5/MAA_5 J26
MAA0_6/MAA_6 H21
MAA0_7/MAA_7 G21
MAA1_0/MAA_8 H19
MAA1_1/MAA_9 H20
MAA1_2/MAA_10 L13
MAA1_3/MAA_11 G16
MAA1_4/MAA_12 J16
MAA1_5/MAA_0 H16
MAA1_6/MAA_1 J17
MAA1_7/MAA_2 H17
FBA_MAA0_0 FBA_MAA0_1 FBA_MAA0_2 FBA_MAA0_3 FBA_MAA0_4 FBA_MAA0_5 FBA_MAA0_6 FBA_MAA0_7 FBA_MAA1_0 FBA_MAA1_1 FBA_MAA1_2 FBA_MAA1_3 FBA_MAA1_4 FBA_MAA1_5 FBA_MAA1_6 FBA_MAA1_7
WCKA0_0/DQMA0_0 C32
WCKA0B_0/DQMA0_1 D23
WCKA0_1/DQMA0_2 E22
WCKA0B_1/DQMA0_3 C14
WCKA1_0/DQMA1_0 A14
WCKA1B_0/DQMA1_1 E10
WCKA1_1/DQMA1_2 D9
WCKA1B_1/DQMA1_3 A32
FBA_WCKA0_0 FBA_WCKA0B_0 FBA_WCKA0_1 FBA_WCKA0B_1 FBA_WCKA1_0 FBA_WCKA1B_0 FBA_WCKA1_1 FBA_WCKA1B_1
FBA_WCKA0_0 [32]
FBA_WCKA0B_0 [32]
FBA_WCKA0_1 [32]
FBA_WCKA0B_1 [32]
FBA_WCKA1_0 [33]
FBA_WCKA1B_0 [33]
FBA_WCKA1_1 [33]
FBA_WCKA1B_1 [33]
EDCA0_0/QSA0_0 C34
EDCA0_1/QSA0_1 D29
EDCA0_2/QSA0_2 D25
EDCA0_3/QSA0_3 E20
EDCA1_0/QSA1_0 E16
EDCA1_1/QSA1_1 E12
EDCA1_2/QSA1_2 J10
EDCA1_3/QSA1_3 D7
FBA0_EDC0 FBA0_EDC1 FBA0_EDC2 FBA0_EDC3 FBA1_EDC0 FBA1_EDC1 FBA1_EDC2 FBA1_EDC3
DDBIA0_0/QSA0_0B A34
DDBIA0_1/QSA0_1B E30
DDBIA0_2/QSA0_2B E26
DDBIA0_3/QSA0_3B C20
DDBIA1_0/QSA1_0B C16
DDBIA1_1/QSA1_1B C12
DDBIA1_2/QSA1_2B J11
DDBIA1_3/QSA1_3B F8
FBA0_DBI0# FBA0_DBI1# FBA0_DBI2# FBA0_DBI3# FBA1_DBI0# FBA1_DBI1# FBA1_DBI2# FBA1_DBI3#
FBA0_DBI0# [32]
FBA0_DBI1# [32]
FBA0_DBI2# [32]
FBA0_DBI3# [32]
FBA1_DBI0# [33]
FBA1_DBI1# [33]
FBA1_DBI2# [33]
FBA1_DBI3# [33]
ADBIA0/ODTA0 J21
ADBIA1/ODTA1 G19
FBA_ADBIA0 FBA_ADBIA1
FBA_ADBIA0 [32]
FBA_ADBIA1 [33]
CLKA0 H27
CLKA0B G27
CLKA1 J14
CLKA1B H14
FBA_CLKA0 FBA_CLKA0# FBA_CLKA1 FBA_CLKA1#
FBA_CLKA0 [32]
FBA_CLKA0# [32]
FBA_CLKA1 [33]
FBA_CLKA1# [33]
RASA0B K23
RASA1B K19
FBA_RASA0# FBA_RASA1#
FBA_RASA0# [32]
FBA_RASA1# [33]
CASA0B K20
CASA1B K17
FBA_CASA0# FBA_CASA1#
FBA_CASA0# [32]
FBA_CASA1# [33]
CSA0B_0 K24
CSA0B_1 K27
FBA_CSA0#
FBA_CSA0# [32]
CSA1B_0 M13
CSA1B_1 K16
FBA_CSA1#
FBA_CSA1# [33]
CKEA0 K21
CKEA1 J20
FBA_CKEA0 FBA_CKEA1
FBA_CKEA0 [32]
FBA_CKEA1 [33]
WEA0B K26
WEA1B L15
FBA_WEA0# FBA_WEA1#
FBA_WEA0# [32]
FBA_WEA1# [33]
MAA0_8/MAA_13 H23
MAA1_8/MAA_14 J19
MAA0_9/MAA_15 M21
MAA1_9/NC M20
FBA_MAA0_8 FBA_MAA1_8
MVREFDA L18
MVREFSA L20
MVREFDA
MVREFSA
NC_MEM_CALRN0 L27
NC_MEM_CALRN1 N12
NC_MEM_CALRN2 AG12
MEM_CALRP0 M27
NC_MEM_CALRP1 M12
NC_MEM_CALRP2 AH12
+1.35VS_VGA
RV18 40.2_0402_1%
RV20 100_0402_5%
CV73 1U_0402_10V6-K
RV22 40.2_0402_1%
RV24 100_0402_5%
CV75 1U_0402_10V6-K
RV26 243_0402_1%
DIS@
UV1I
PART 9 OF 9
GDDR5/DDR3
MEMORY INTERFACE B
[34] FBB_D[0..31]
[35] FBB1_D[0..31]
FBB_D0 C5
FBB_D1 C3
FBB_D2 E3
FBB_D3 E1
FBB_D4 F1
FBB_D5 F3
FBB_D6 F5
FBB_D7 G4
FBB_D8 H5
FBB_D9 H6
FBB_D10 J4
FBB_D11 K6
FBB_D12 K5
FBB_D13 L4
FBB_D14 M6
FBB_D15 M1
FBB_D16 M3
FBB_D17 M5
FBB_D18 N4
FBB_D19 P6
FBB_D20 P5
FBB_D21 R4
FBB_D22 T6
FBB_D23 T1
FBB_D24 U4
FBB_D25 V6
FBB_D26 V1
FBB_D27 V3
FBB_D28 Y6
FBB_D29 Y1
FBB_D30 Y3
FBB_D31 Y5
FBB1_D0 AA4
FBB1_D1 AB6
FBB1_D2 AB1
FBB1_D3 AB3
FBB1_D4 AD6
FBB1_D5 AD1
FBB1_D6 AD3
FBB1_D7 AD5
FBB1_D8 AF1
FBB1_D9 AF3
FBB1_D10 AF6
FBB1_D11 AG4
FBB1_D12 AH5
FBB1_D13 AH6
FBB1_D14 AJ4
FBB1_D15 AK3
FBB1_D16 AF8
FBB1_D17 AF9
FBB1_D18 AG8
FBB1_D19 AG7
FBB1_D20 AK9
FBB1_D21 AL7
FBB1_D22 AM8
FBB1_D23 AM7
FBB1_D24 AK1
FBB1_D25 AL4
FBB1_D26 AM6
FBB1_D27 AM1
FBB1_D28 AN4
FBB1_D29 AP3
FBB1_D30 AP1
FBB1_D31 AP5
DQB0_0 DQB0_1 DQB0_2 DQB0_3 DQB0_4 DQB0_5 DQB0_6 DQB0_7 DQB0_8 DQB0_9 DQB0_10 DQB0_11 DQB0_12 DQB0_13 DQB0_14 DQB0_15 DQB0_16 DQB0_17 DQB0_18 DQB0_19 DQB0_20 DQB0_21 DQB0_22 DQB0_23 DQB0_24 DQB0_25 DQB0_26 DQB0_27 DQB0_28 DQB0_29 DQB0_30 DQB0_31
DQB1_0 DQB1_1 DQB1_2 DQB1_3 DQB1_4 DQB1_5 DQB1_6 DQB1_7 DQB1_8 DQB1_9 DQB1_10 DQB1_11 DQB1_12 DQB1_13 DQB1_14 DQB1_15 DQB1_16 DQB1_17 DQB1_18 DQB1_19 DQB1_20 DQB1_21 DQB1_22 DQB1_23 DQB1_24 DQB1_25 DQB1_26 DQB1_27 DQB1_28 DQB1_29 DQB1_30 DQB1_31
MAB0_0 P8
MAB0_1 T9
MAB0_2 P9
MAB0_3 N7
MAB0_4 N8
MAB0_5 N9
MAB0_6 U9
MAB0_7 U8
MAB1_0 Y9
MAB1_1 W9
MAB1_2 AC8
MAB1_3 AC9
MAB1_4 AA7
MAB1_5 AA8
MAB1_6 Y8
MAB1_7 AA9
FBB_MAB0_0 FBB_MAB0_1 FBB_MAB0_2 FBB_MAB0_3 FBB_MAB0_4 FBB_MAB0_5 FBB_MAB0_6 FBB_MAB0_7 FBB_MAB1_0 FBB_MAB1_1 FBB_MAB1_2 FBB_MAB1_3 FBB_MAB1_4 FBB_MAB1_5 FBB_MAB1_6 FBB_MAB1_7
WCKB0_0 H3
WCKB0B_0 H1
WCKB0_1 T3
WCKB0B_1 T5
WCKB1_0 AE4
WCKB1B_0 AF5
WCKB1_1 AK6
WCKB1B_1 AK5
FBB_WCKB0_0 FBB_WCKB0B_0 FBB_WCKB0_1 FBB_WCKB0B_1 FBB_WCKB1_0 FBB_WCKB1B_0 FBB_WCKB1_1 FBB_WCKB1B_1
FBB_WCKB0_0 [34]
FBB_WCKB0B_0 [34]
FBB_WCKB0_1 [34]
FBB_WCKB0B_1 [34]
FBB_WCKB1_0 [35]
FBB_WCKB1B_0 [35]
FBB_WCKB1_1 [35]
FBB_WCKB1B_1 [35]
EDCB0_0 F6
EDCB0_1 K3
EDCB0_2 P3
EDCB0_3 V5
EDCB1_0 AB5
EDCB1_1 AH1
EDCB1_2 AJ9
EDCB1_3 AM5
FBB0_EDC0 FBB0_EDC1 FBB0_EDC2 FBB0_EDC3 FBB1_EDC0 FBB1_EDC1 FBB1_EDC2 FBB1_EDC3
DDBIB0_0 G7
DDBIB0_1 K1
DDBIB0_2 P1
DDBIB0_3 W4
DDBIB1_0 AC4
DDBIB1_1 AH3
DDBIB1_2 AJ8
DDBIB1_3 AM3
FBB0_DBI0# FBB0_DBI1# FBB0_DBI2# FBB0_DBI3# FBB1_DBI0# FBB1_DBI1# FBB1_DBI2# FBB1_DBI3#
FBB0_DBI0# [34]
FBB0_DBI1# [34]
FBB0_DBI2# [34]
FBB0_DBI3# [34]
FBB1_DBI0# [35]
FBB1_DBI1# [35]
FBB1_DBI2# [35]
FBB1_DBI3# [35]
ADBIB0 T7
ADBIB1 W7
FBB_ADBIB0 FBB_ADBIB1
FBB_ADBIB0 [34]
FBB_ADBIB1 [35]
CLKB0 L9
CLKB0B L8
CLKB1 AD8
CLKB1B AD7
FBB_CLKB0 FBB_CLKB0# FBB_CLKB1 FBB_CLKB1#
FBB_CLKB0 [34]
FBB_CLKB0# [34]
FBB_CLKB1 [35]
FBB_CLKB1# [35]
RASB0B T10
RASB1B Y10
FBB_RASB0# FBB_RASB1#
FBB_RASB0# [34]
FBB_RASB1# [35]
CASB0B W10
CASB1B AA10
FBB_CASB0# FBB_CASB1#
FBB_CASB0# [34]
FBB_CASB1# [35]
CSB0B_0 P10
CSB0B_1 L10
FBB_CSB0#
FBB_CSB0# [34]
CSB1B_0 AD10
CSB1B_1 AC10
FBB_CSB1#
FBB_CSB1# [35]
CKEB0 U10
CKEB1 AA11
FBB_CKEB0 FBB_CKEB1
FBB_CKEB0 [34]
FBB_CKEB1 [35]
WEB0B N10
WEB1B AB11
FBB_WEB0# FBB_WEB1#
FBB_WEB0# [34]
FBB_WEB1# [35]
MAB0_8 T8
MAB1_8 W8
MAB0_9 U12
MAB1_9 V12
FBB_MAB0_8 FBB_MAB1_8
DRAM_RST AH11
DRAM_RST
MVREFDB Y12
MVREFSB AA12
MVREFDB
MVREFSB
+1.35VS_VGA
RV19 40.2_0402_1%
RV21 100_0402_5%
CV74 1U_0402_10V6-K
RV23 40.2_0402_1%
RV25 100_0402_5%
CV76 1U_0402_10V6-K
DIS@
[32,33,34,35] FBA_RST#
FBA_RST#
RV27 49.9_0402_1%
RV28 10_0402_5%
DRAM_RST
CV77 120P_0402_50V8-J
RV29 5.1K_0402_5%
CV78 68P_0402_50V8-J
@
216-0855000_A0_FCBGA962
Security Classification
LC Future Center Secret Data
Issued Date
2012/07/01
Deciphered Date
2014/07/01
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.
Title
GDDR5
Size Custom
Document Number
BE560
Rev 0.1
Date: Wednesday, September 23, 2015 Sheet 31 of 99

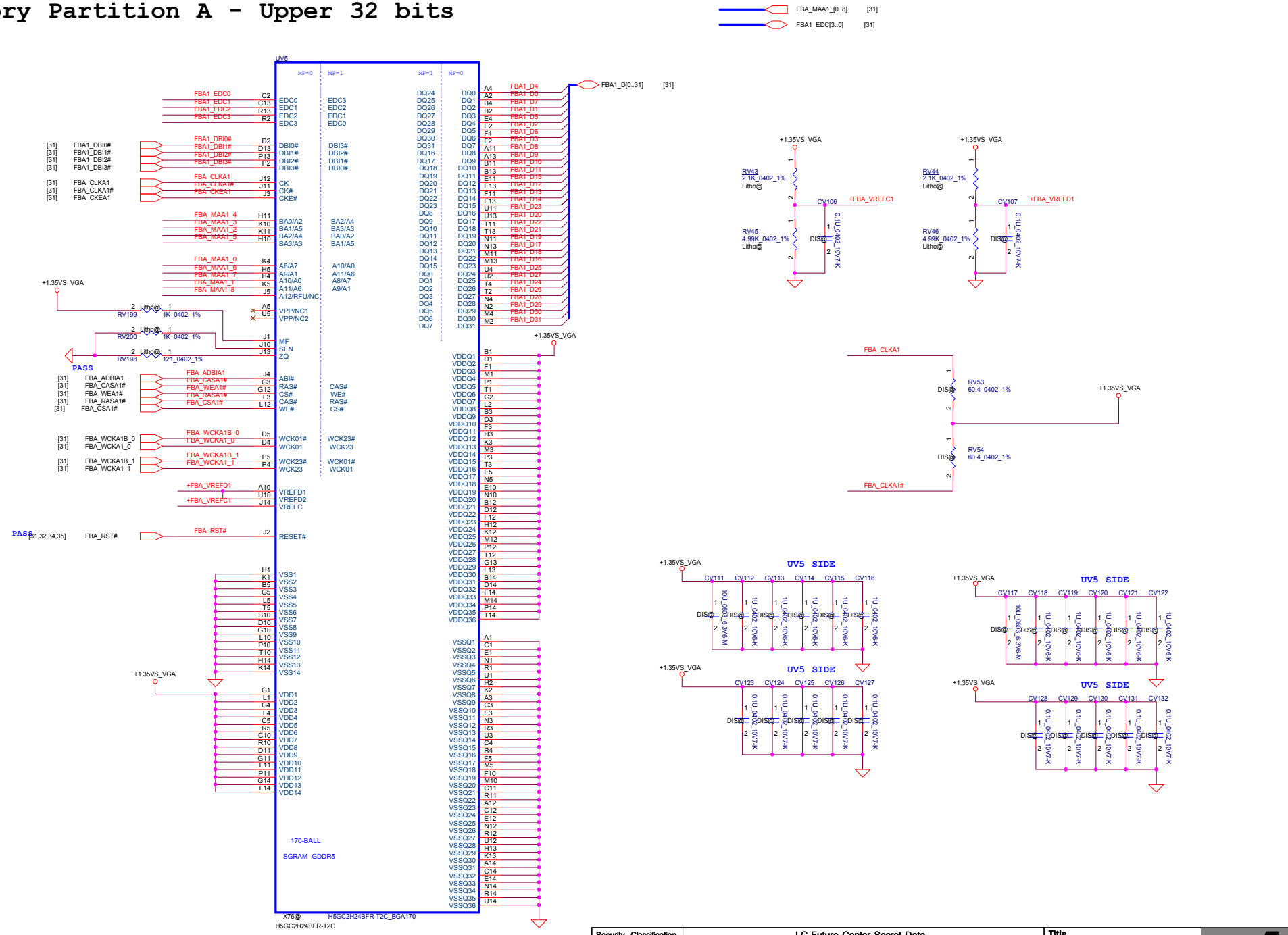
Memory Partition A - Lower 32 bits



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	GDDR5		
Size Custom	Document Number	BE560	Rev 0.1
Date:	Wednesday, September 23, 2015	Sheet 32 of 99	

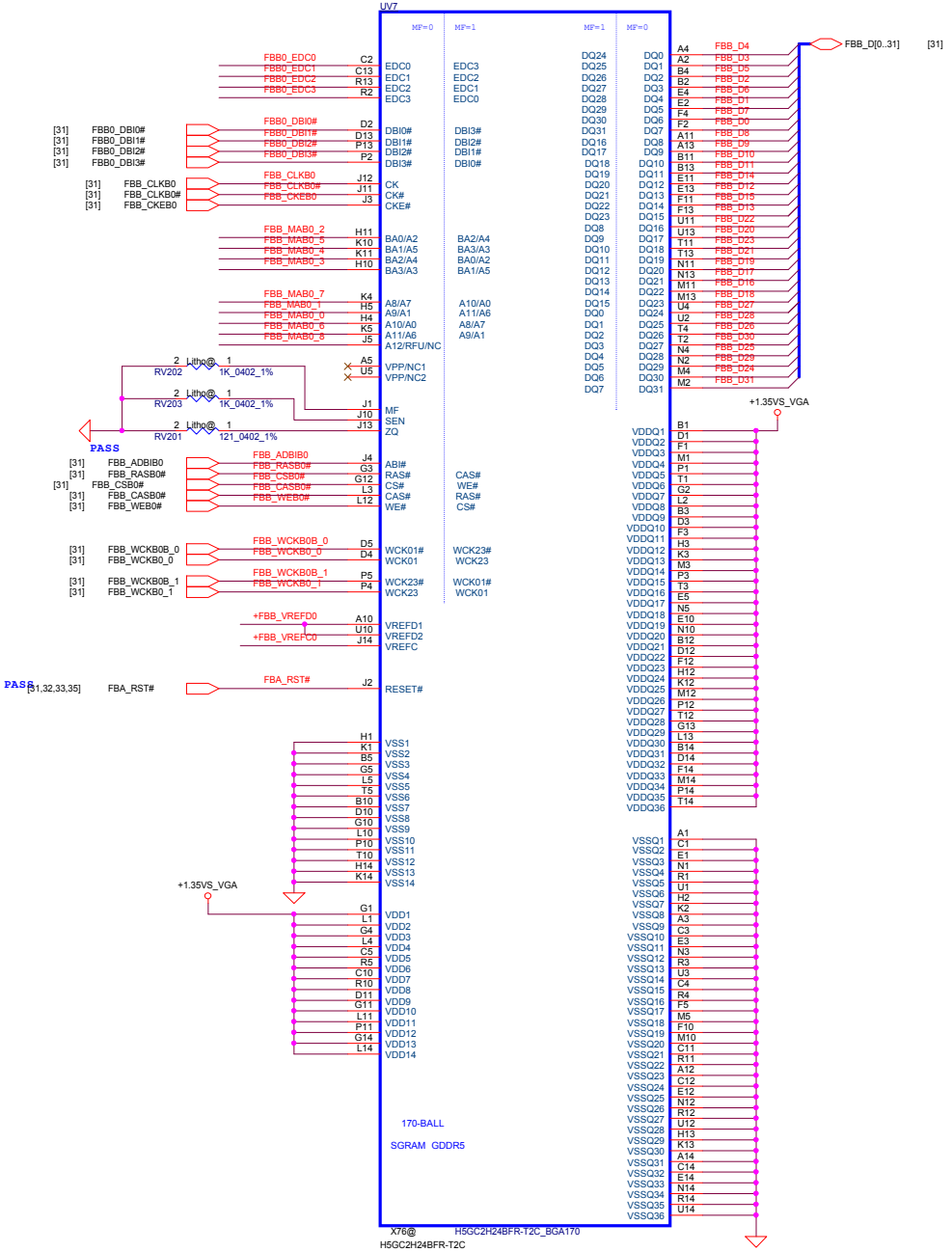
Memory Partition A - Upper 32 bits

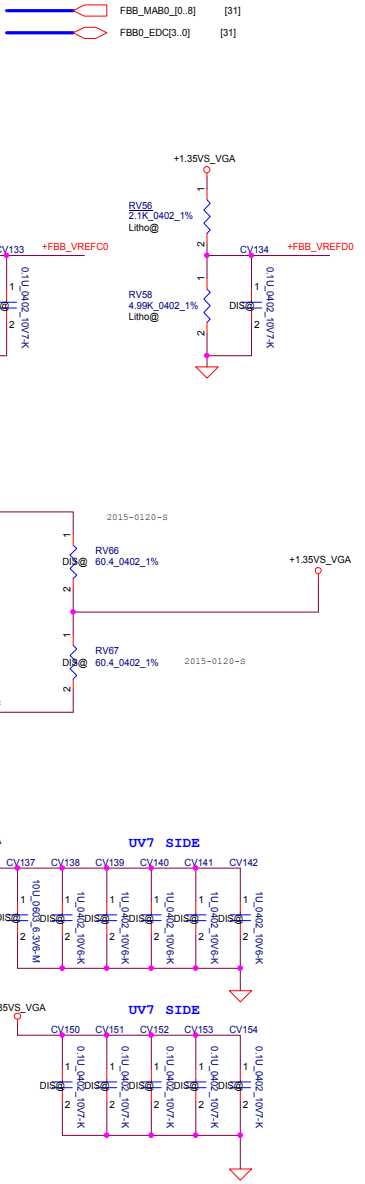


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	GDDR5	
Size Custom	Document Number BE560	Rev 0.1
Date: Wednesday, September 23, 2015	Sheet 33 of 99	

Memory Partition A - Lower 32 bits

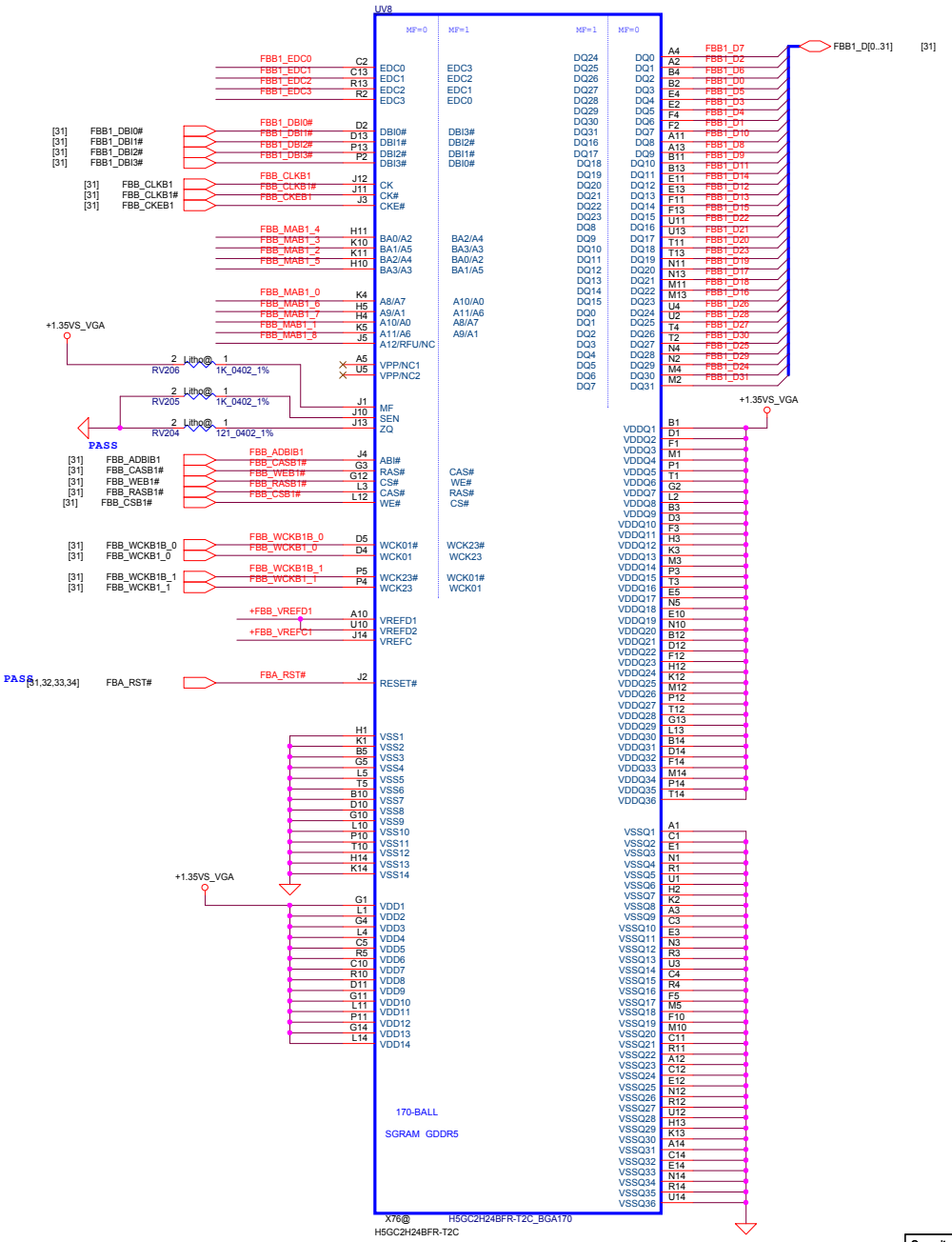


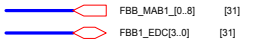


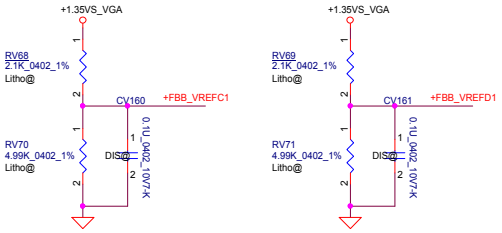
Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

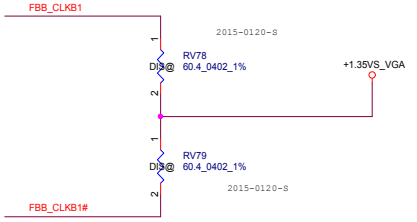
Title	GDDR5		
Size Custom	Document Number BE560		Rev 0.1
Date: Wednesday, September 23, 2015	Sheet 34 of 99		

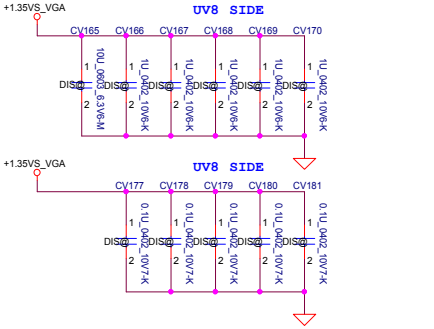
Memory Partition A - Upper 32 bits







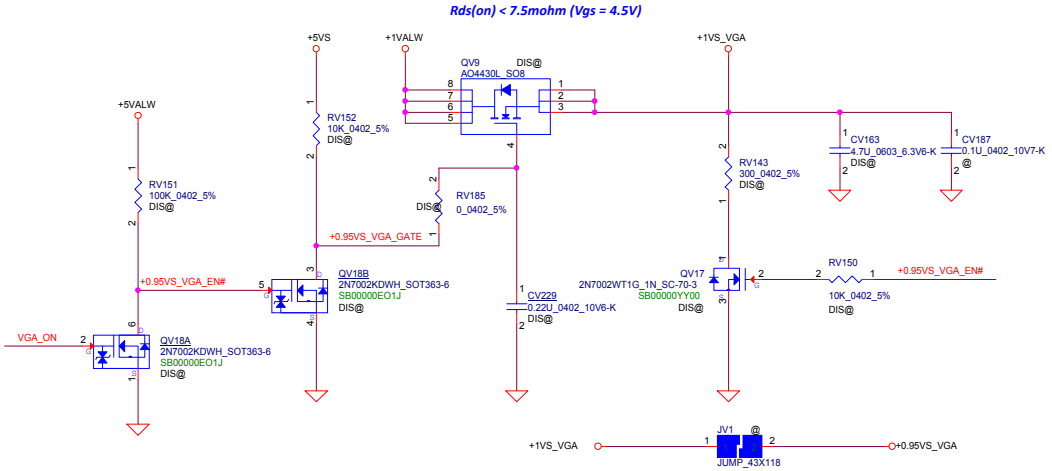




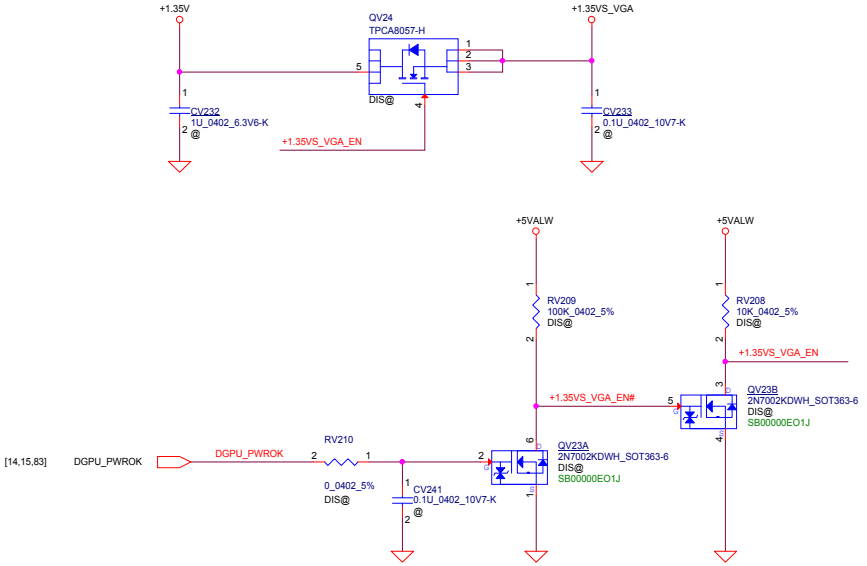
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title	GDDR5	
Size: Custom	Document Number: BE560	Rev: 0.1
Date: Wednesday, September 23, 2015	Sheet 35 of 99	

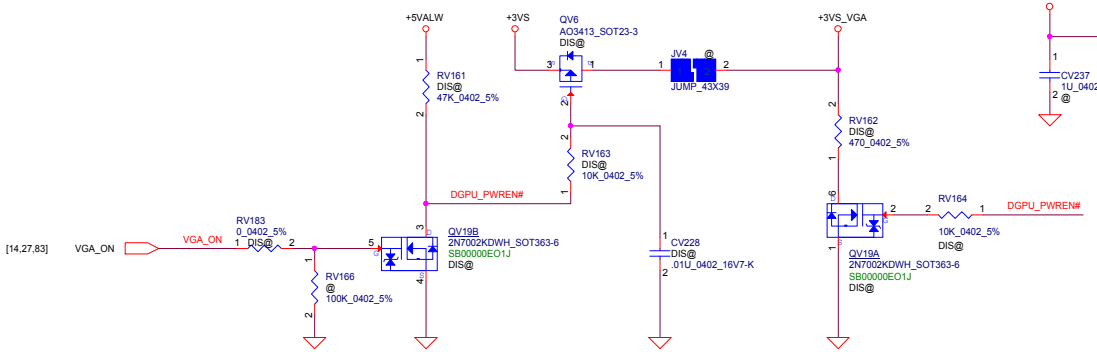
+1.0VALW to +0.95VS_VGA



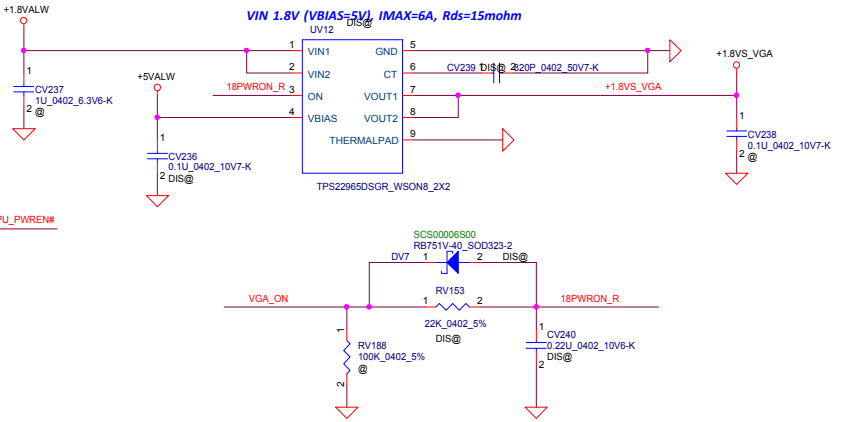
+1.35V to +1.35VS_VGA



+3VS to +3VS_VGA



+1.8VALW to +1.8VS_VGA



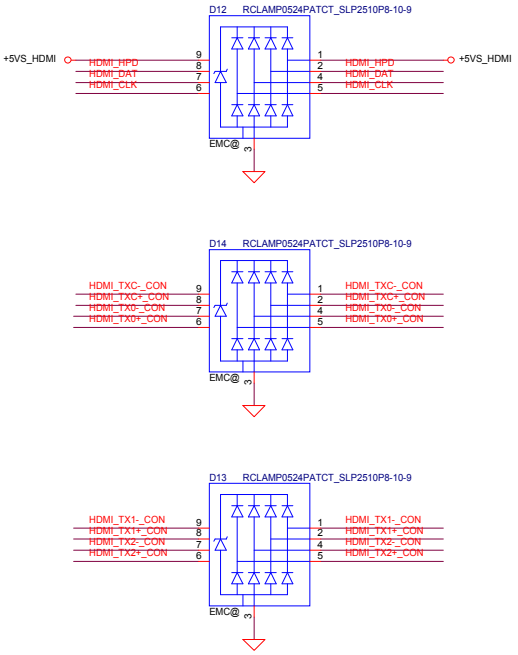
MLPS	Bit				
	5	4	3	2	1
PS_0[5:1]	1	1	0	0	1
PS_1[5:1]	1	1	0	0	0
PS_2[5:1]	1	1	0	0	0
PS_3[5:1]	1	1	X	X	X

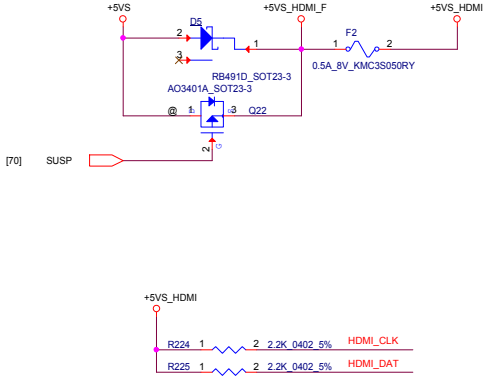
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

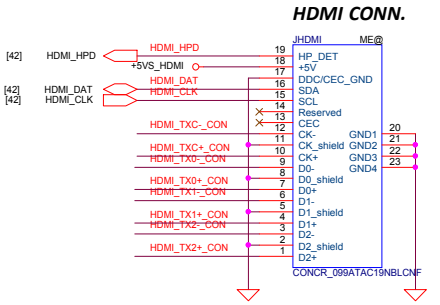
Title: *Litho swich power*

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 36 of 99







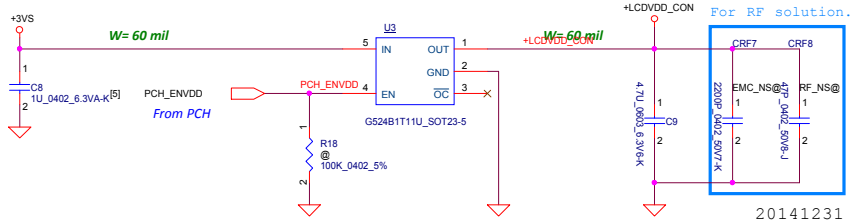
Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **HDMI CONN**

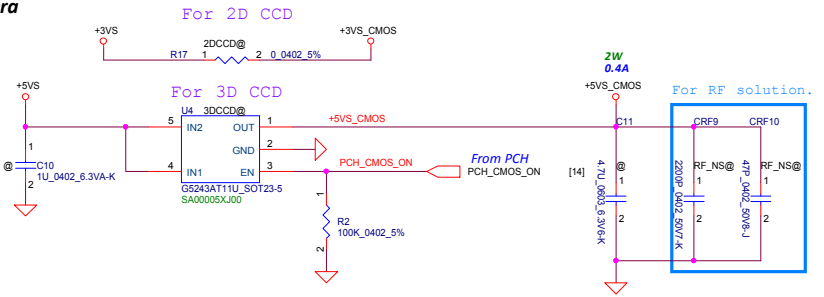
Size	Document Number	Rev
Custom	BE560	0.1

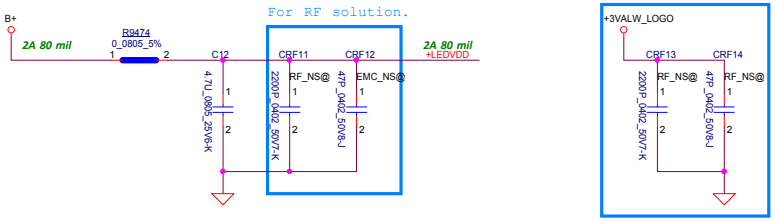
Date: Wednesday, September 23, 2015 Sheet 37 of 99

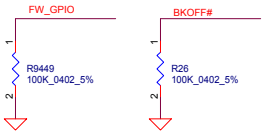
LCDVDD Circuit



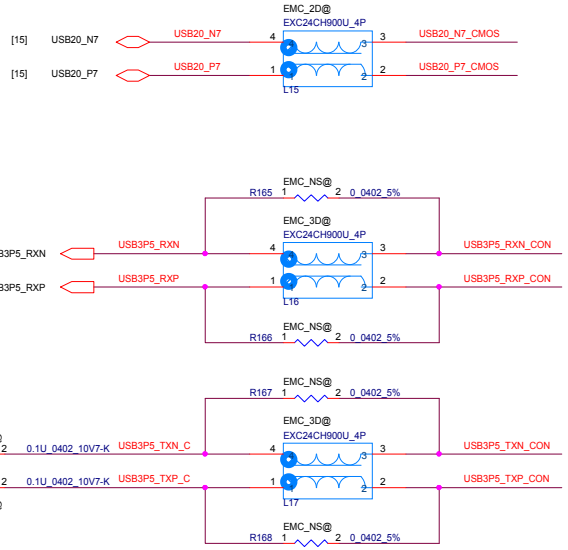
CMOS Camera



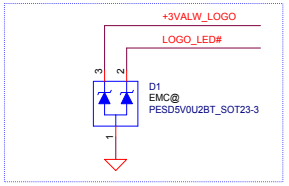




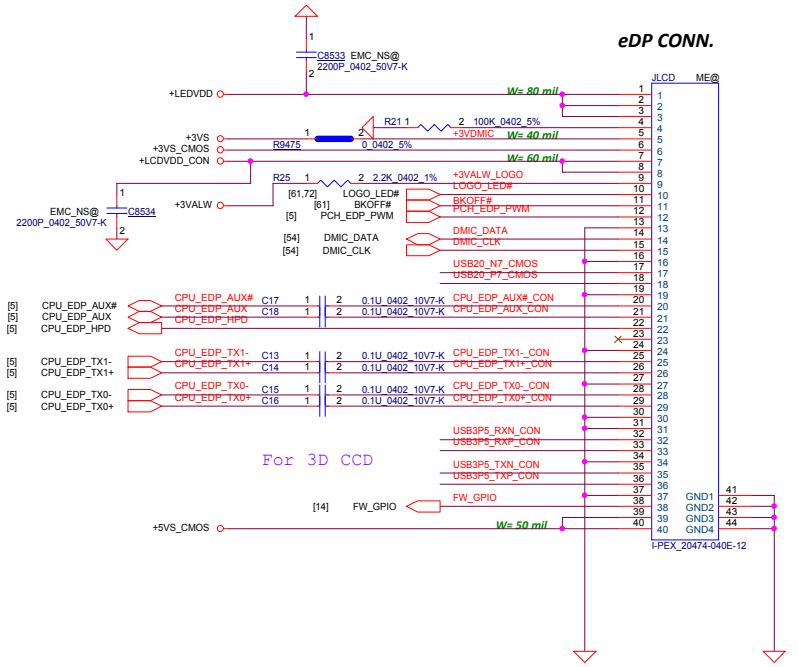
CMOS USB Port 2



ESD request



eDP CONN.

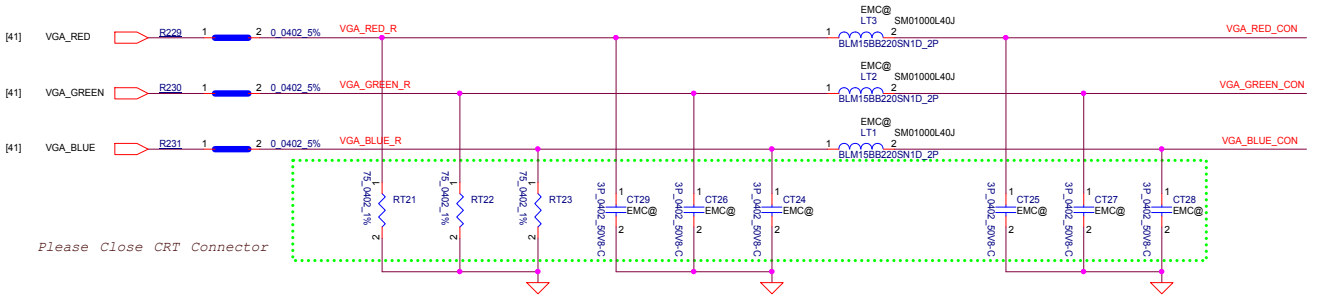


Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

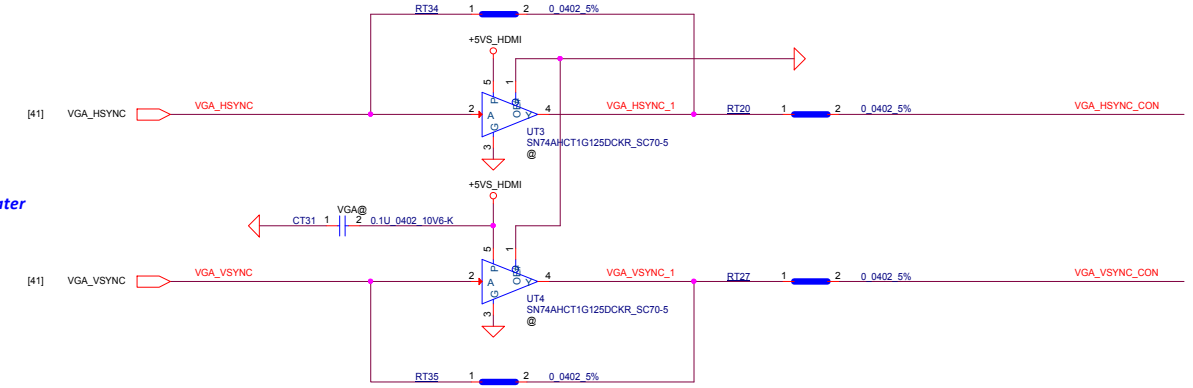
Title: eDP CONN

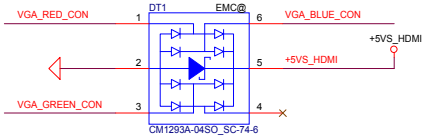
Size: Custom | Document Number: BE560 | Rev: 0.1

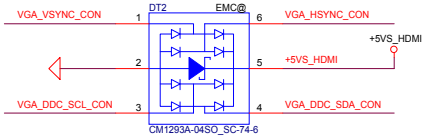
Date: Wednesday, September 23, 2015 | Sheet 38 of 99

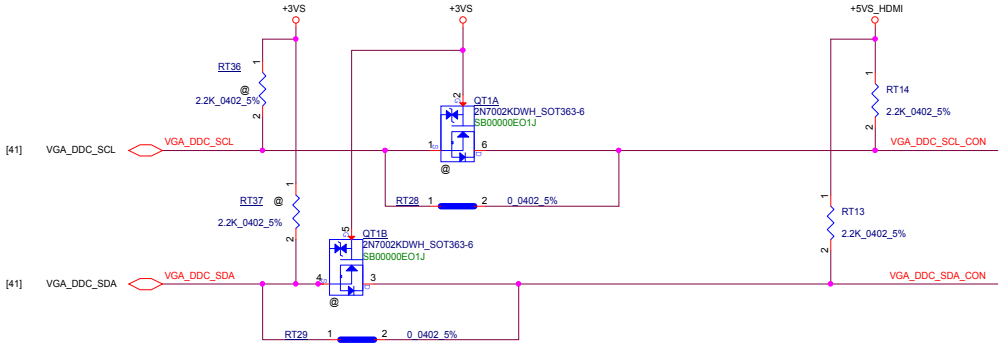


Traslater



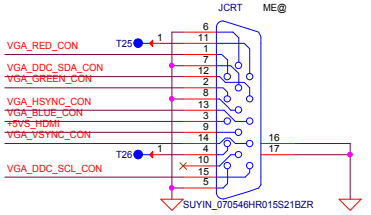






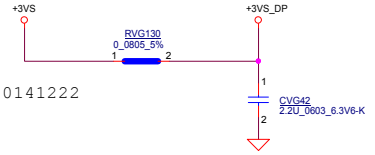
Only for 15'

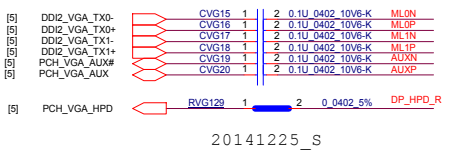
CRT Connector

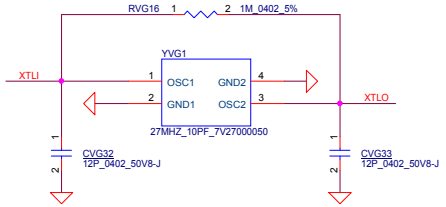


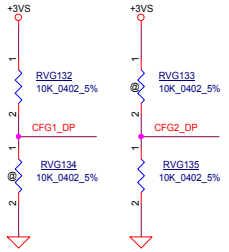
Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title		
CRT CONN		
Size: Custom	Document Number: BE560	Rev: 0.1
Date: Wednesday, September 23, 2015	Sheet 40 of 99	









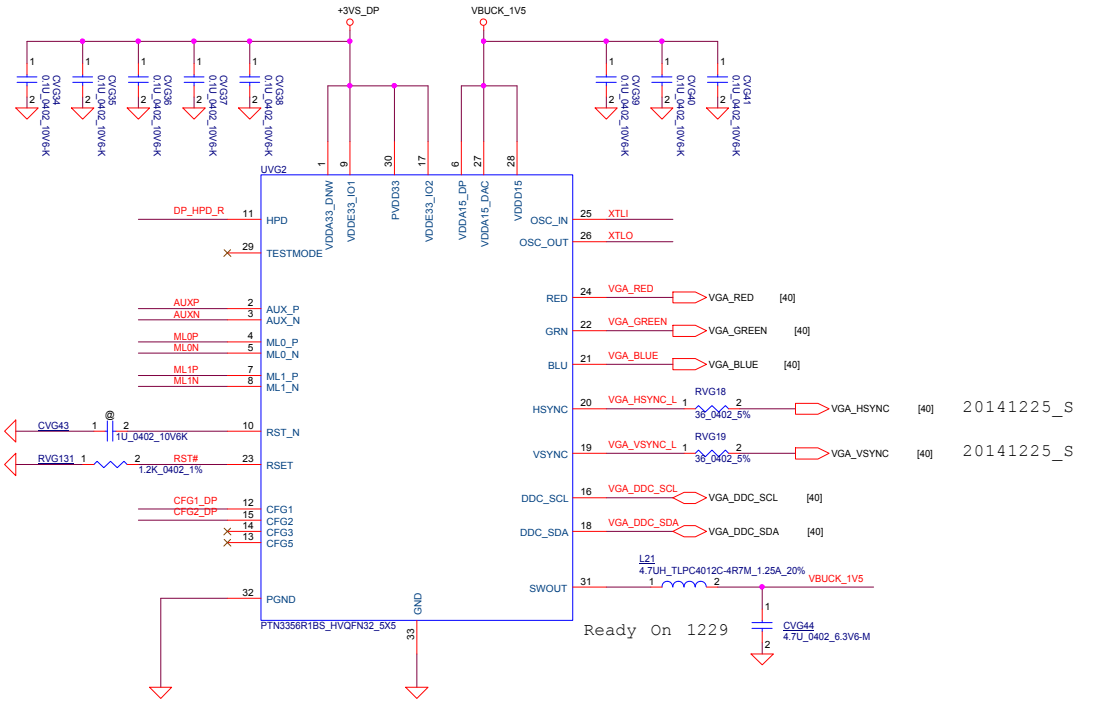


Table 7. CFG1/CFG2 pin definitions

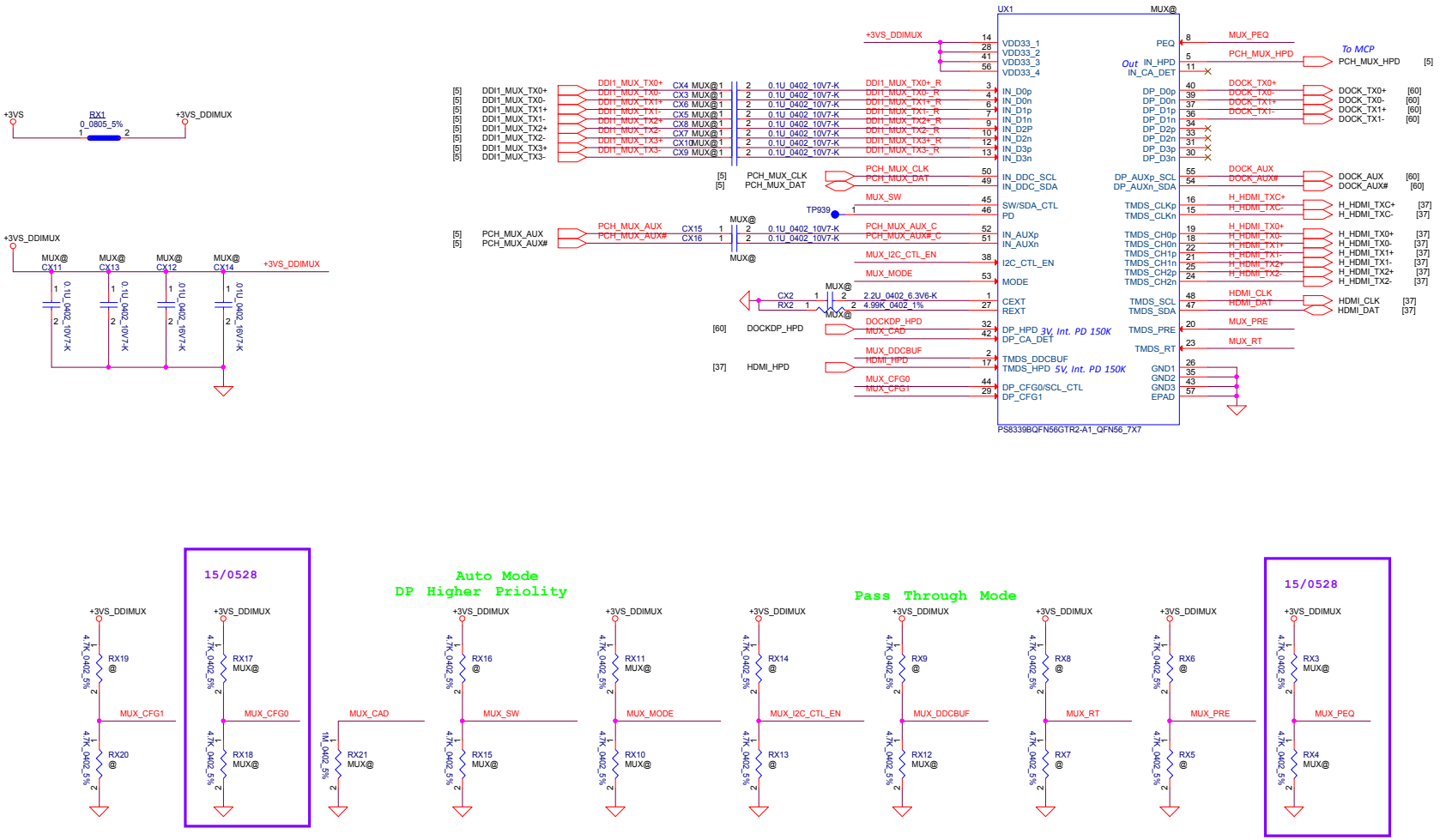
Pin value	System behavior
00	Compliant HPD behavior
01	Most interoperable (non-compliant) HPD behavior
10	Most interoperable (non-compliant) HPD behavior
11	(Default) Compliant behavior

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: DP to VGA

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 41 of 99



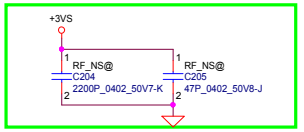
Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

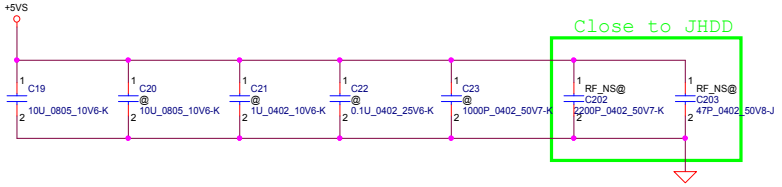
Title: **Mux IC**

Size	Document Number	Rev
Custom	BE560	0.1
Date: Wednesday, September 23, 2015	Sheet 42 of 99	

SATA HDD CONN.

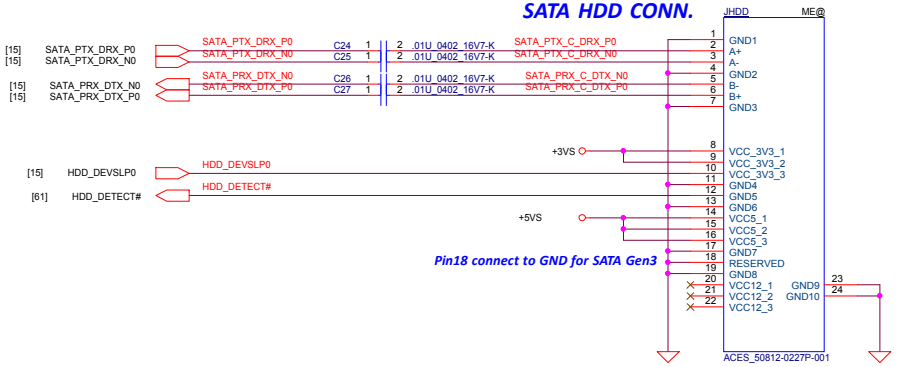
Close to JHDD





Close to JHDD

SATA HDD CONN.



Pin18 connect to GND for SATA Gen3

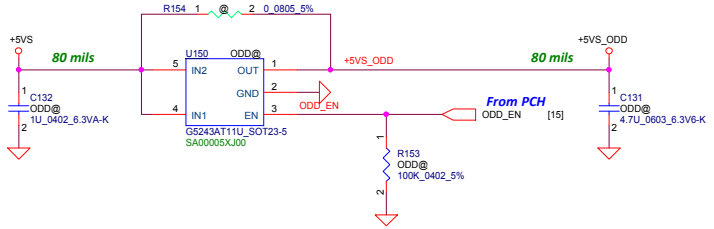
Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

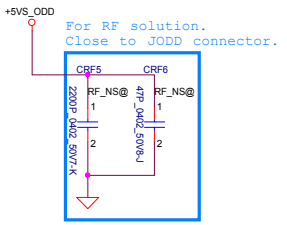
Title: **SATA HDD**

Size	Document Number	Rev
Custom	BE560	0.1

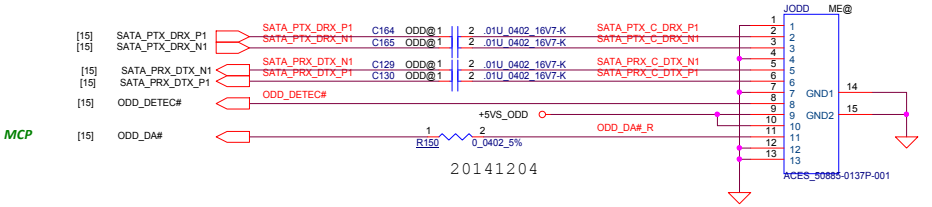
Date: Wednesday, September 23, 2015 | Sheet 43 of 99

+5VS TO +5VS_ODD





SATA ODD CONN



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

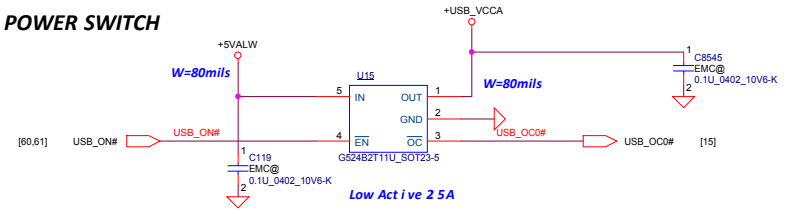
Title: ODD

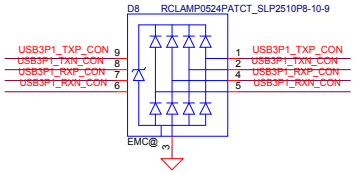
Size	Document Number	Rev
Custom	BE560	0.1

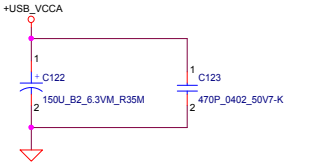
Date: Wednesday, September 23, 2015 | Sheet 44 of 99

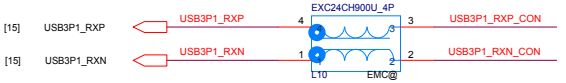
USB3 PORT1

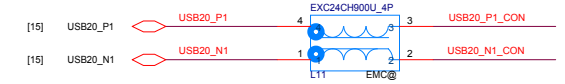
POWER SWITCH

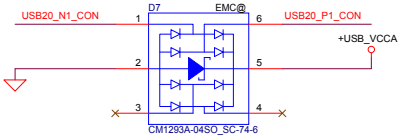


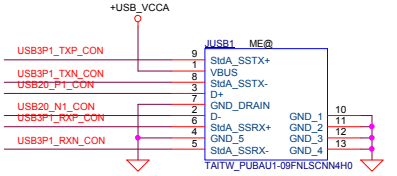




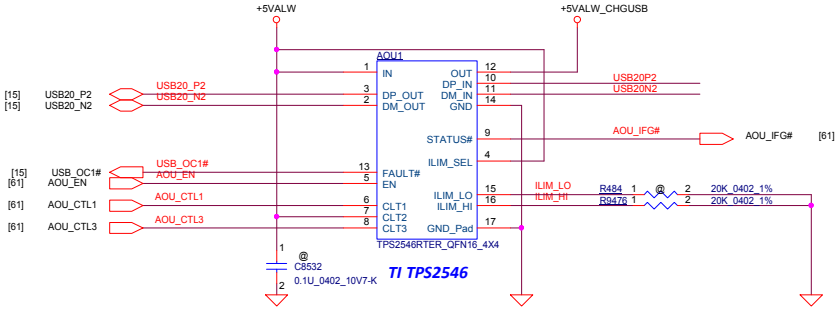




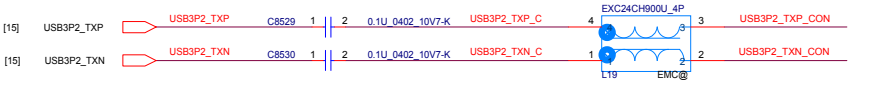


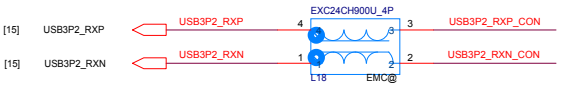


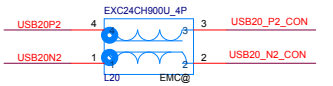
PORT2 (AOU)

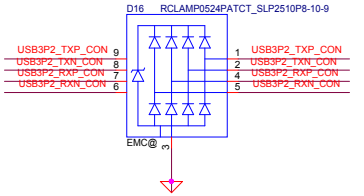


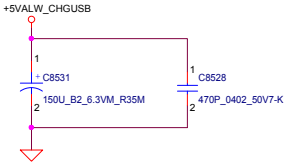
CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCH	OUT held low
1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

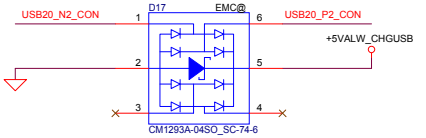


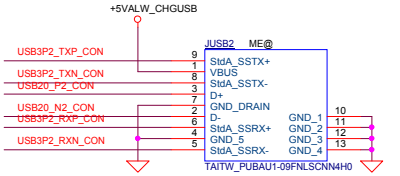










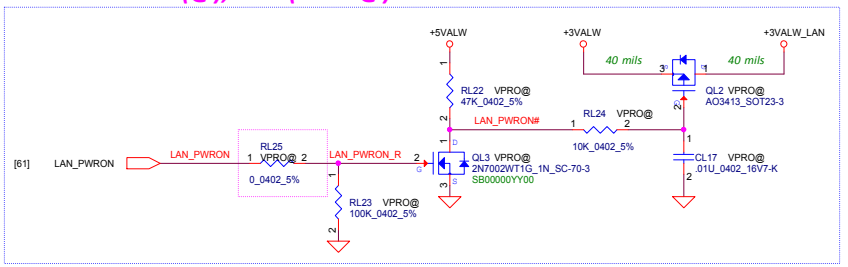


Title: USB3 PORT1/PORT2(AOU)

Size: Custom | Document Number: BE560 | Rev: 0.1

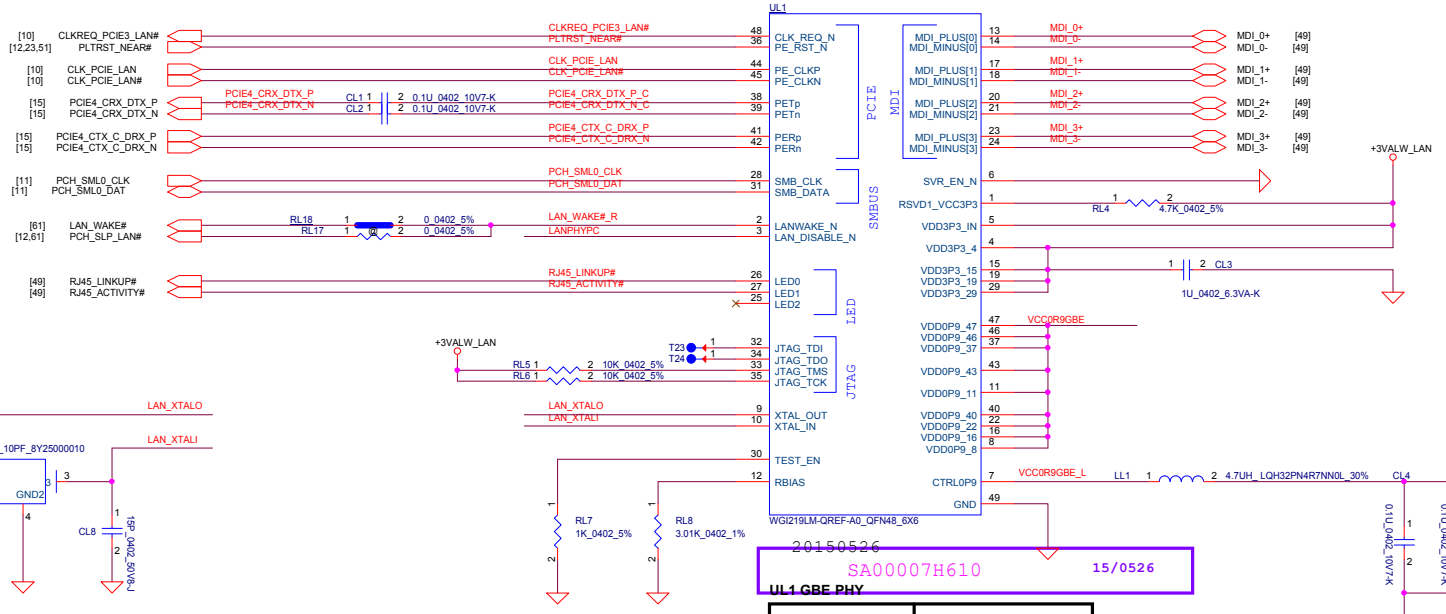
Date: Wednesday, September 23, 2015 | Sheet 45 of 99

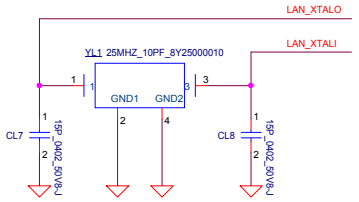
VPRO SKU : RL2 (@), RL25(VPRO@)



For Non-Vpro

20141209





20150526

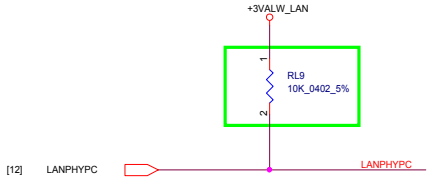
SA00007H610

15/0526

UL1 GBE PHY

vPro Model	Non-vPro Model
I219LM	I219V

ST-1_SWG_SDV-SWG_EC062
Add vPro/Non-vPro table.



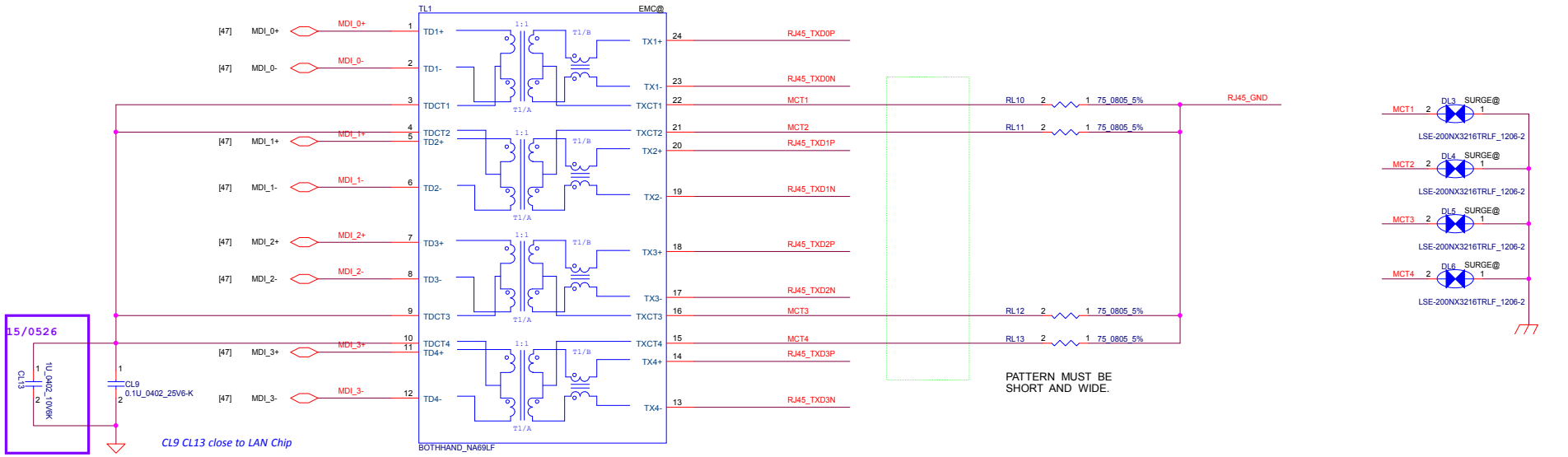
When use Native function, intel recommend pull high 10K ohm
This part is un-mount in Sting.

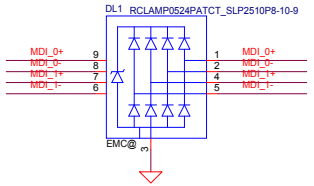
Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

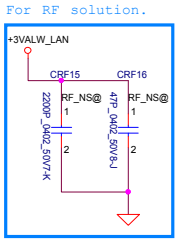
Title: **LAN**

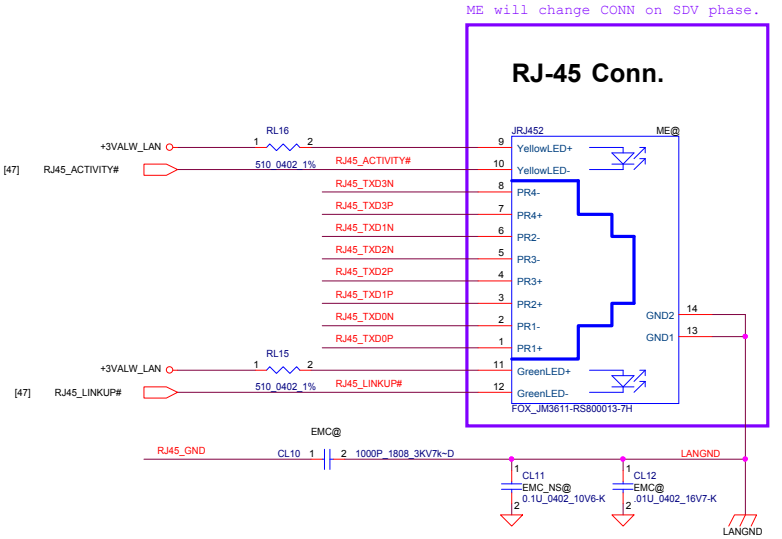
Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 47 of 99









20141231

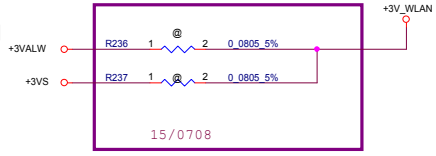
Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: RJ45 CONN

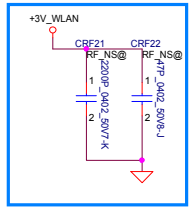
Size	Document Number	Rev
Custom	BE560	0.1

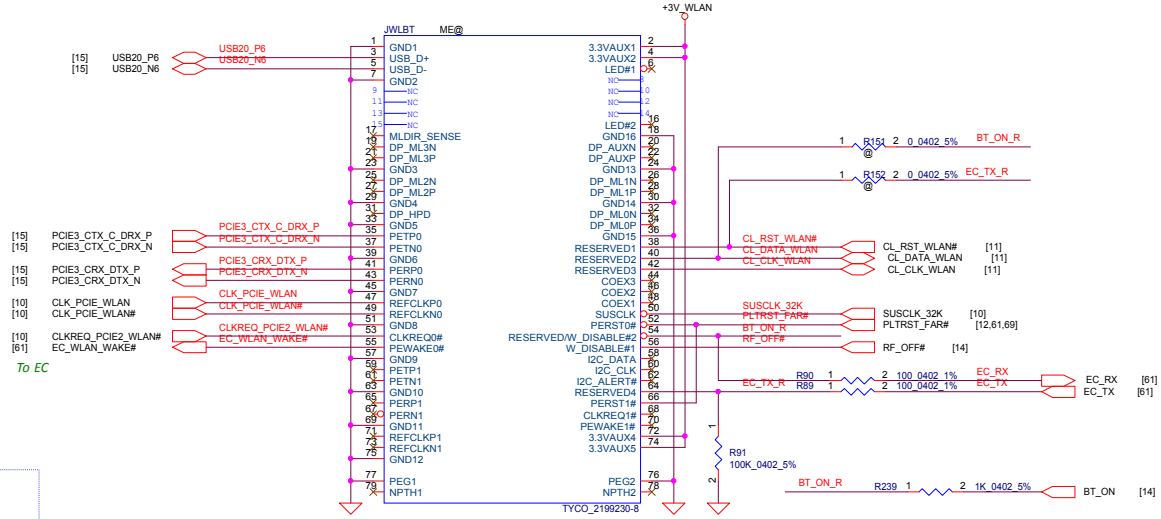
Date: Wednesday, September 23, 2015 | Sheet 49 of 99

TYPE-A NGFF SLOT FOR WLAN
3.2H CONNECTOR

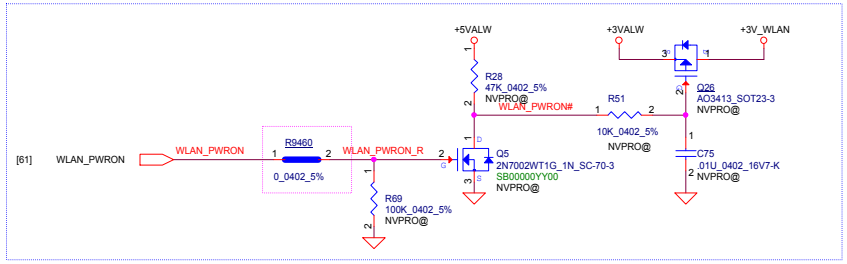


For RF solution.





VPRO SKU : R48(@), R70(VPRO@)

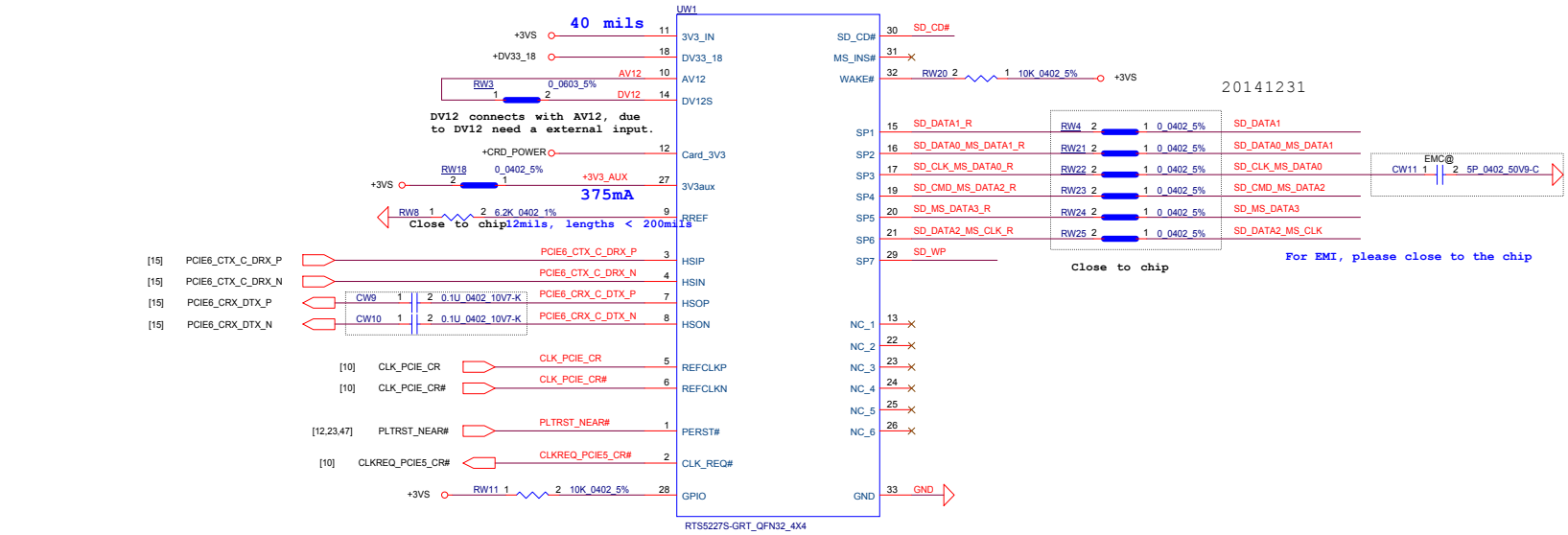


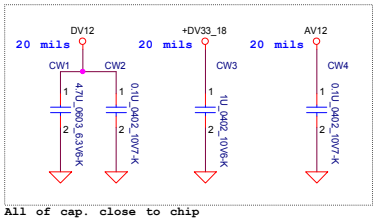
Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

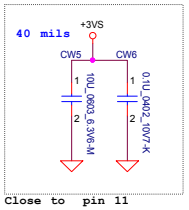
Title: *WWAN/WLAN NGFF CONN.*

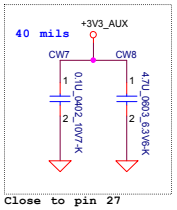
Size	Document Number	Rev
Custom	BE560	0.1

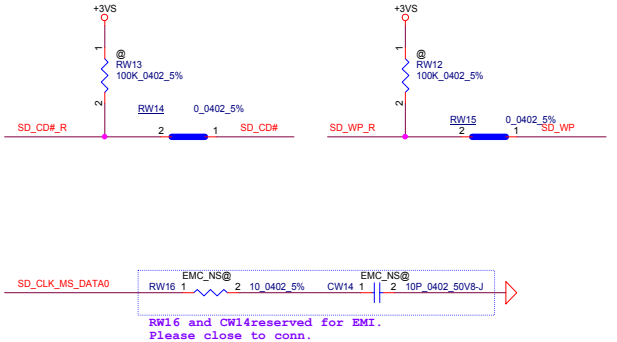
Date: Wednesday, September 23, 2015 Sheet 50 of 99

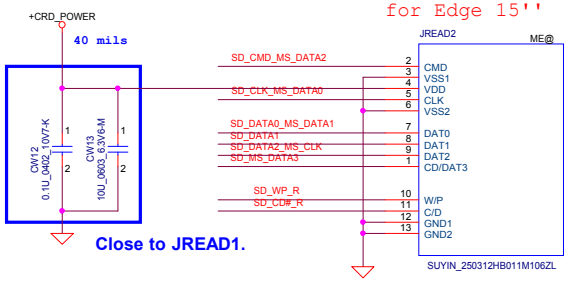










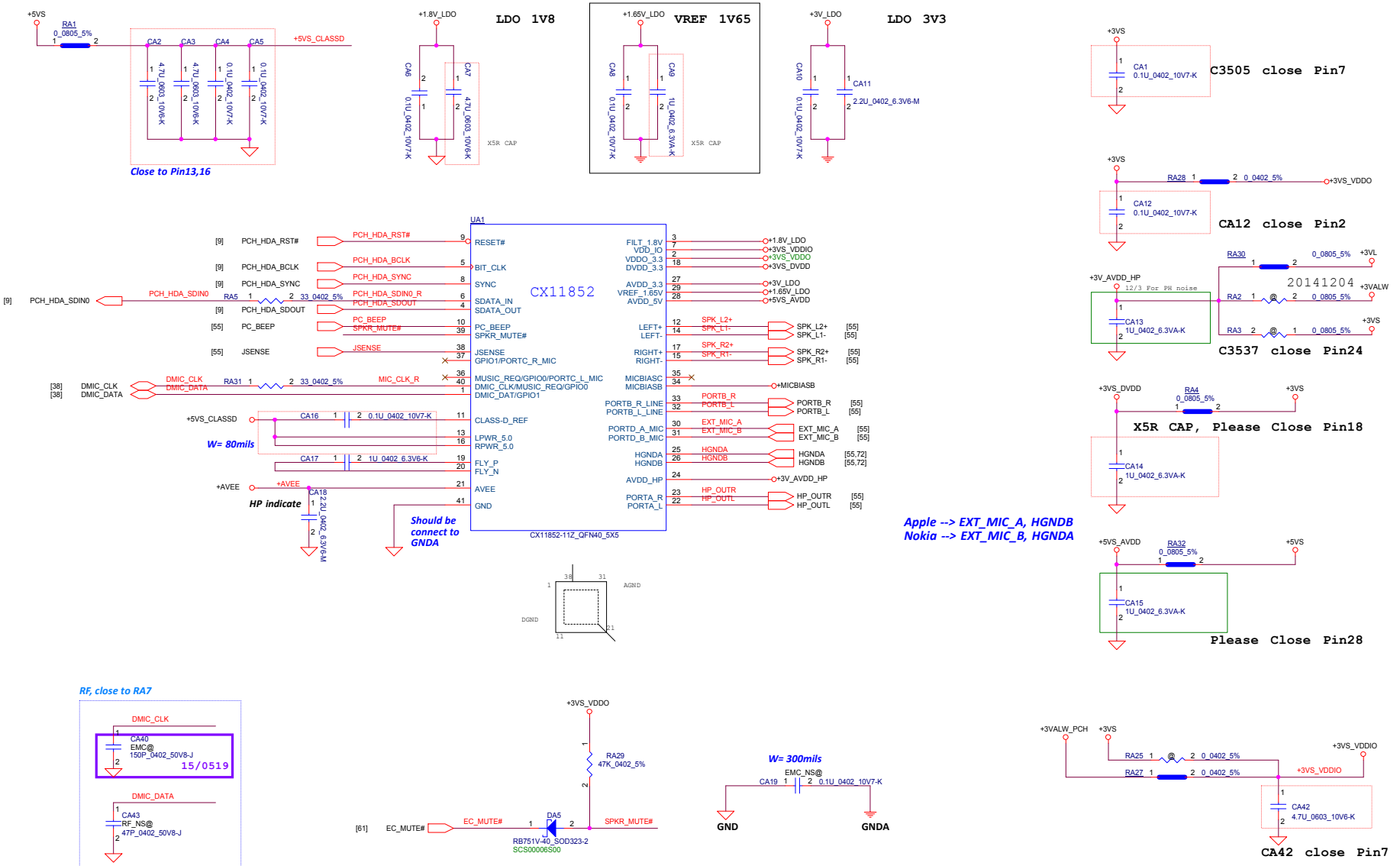


Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **Card Reader**

Size	Document Number	Rev
Custom	BE560	0.1

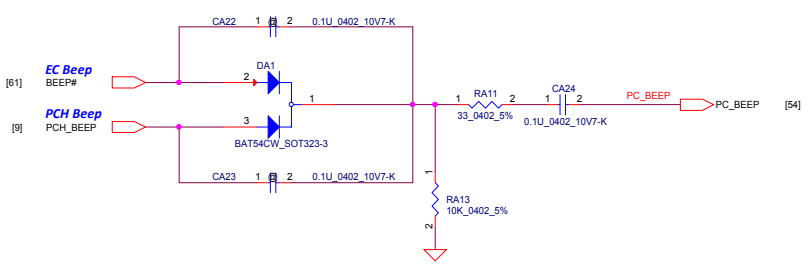
Date: Wednesday, September 23, 2015 | Sheet 51 of 99

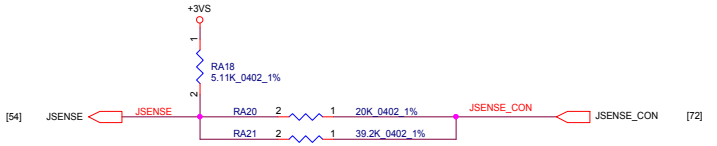


Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title	Audio Codec		
Size	Document Number		Rev
Custom	BE560		0.1
Date:	Wednesday, September 23, 2015	Sheet	54 of 99

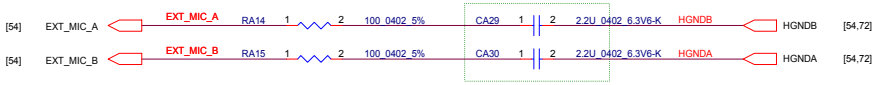
PC Beep





EXT. MIC/LINE IN

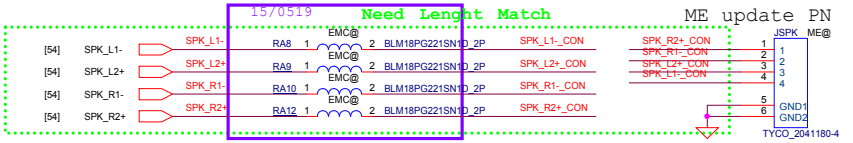
Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA

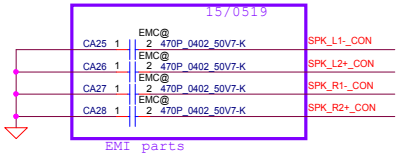


Changed CA29 & CA30 from 1uF to 2.2uF/X5R
to meet Port-D(headset-Mic) THD+N <= -65 dB

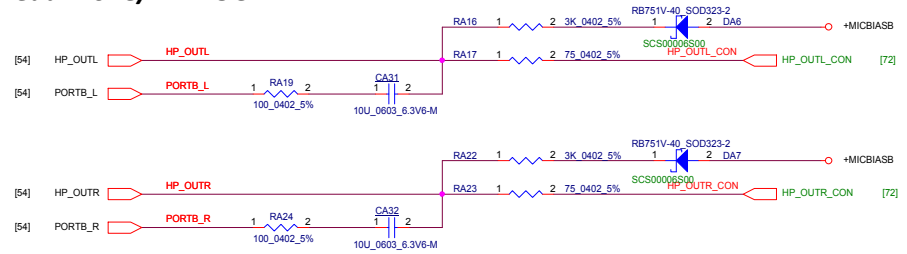
Speaker OUT

SPK CONN.





HeadPhone/LINE OUT



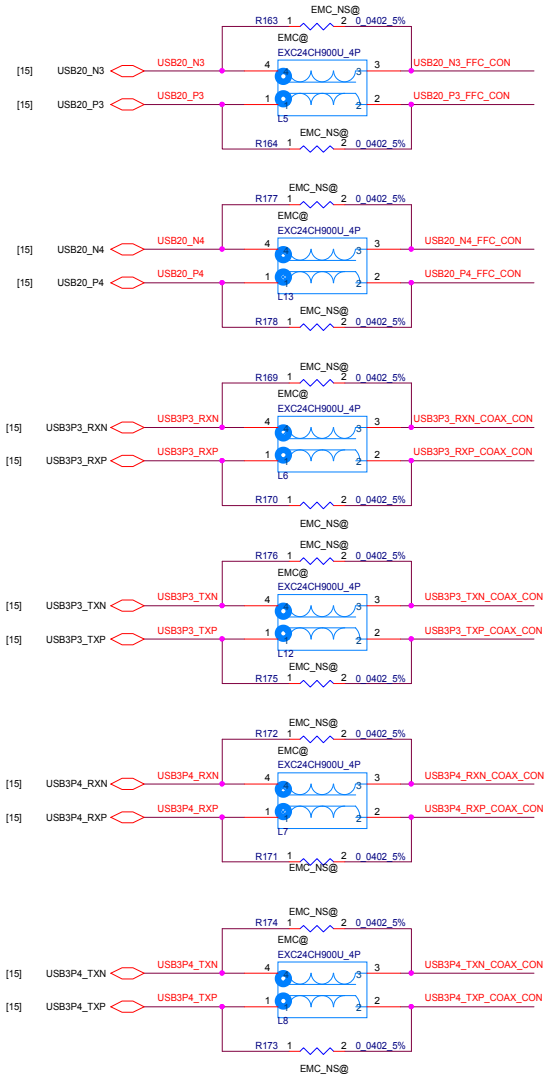
CA31, CA32 change to 4.7U for Quality requirement

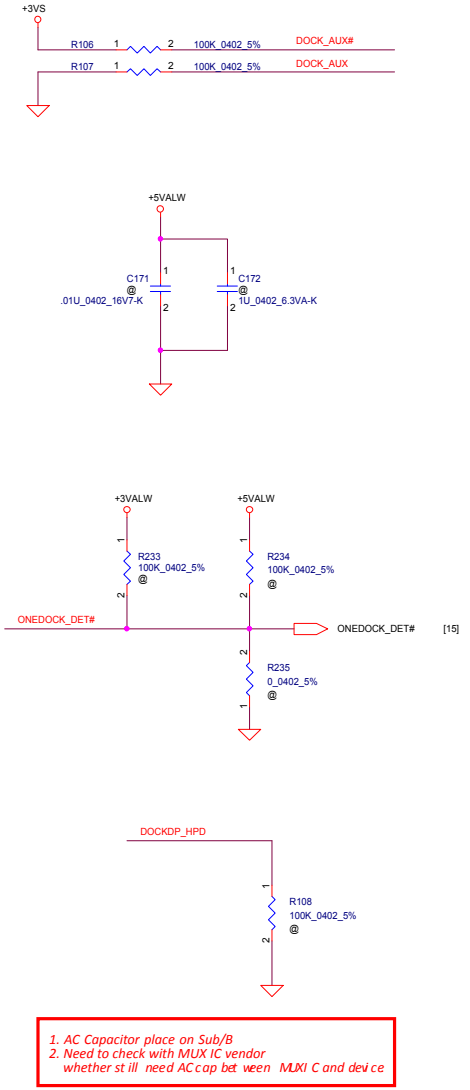
Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **HP/MIC JACK/Speaker**

Size	Document Number	Rev
Custom	BE560	0.1

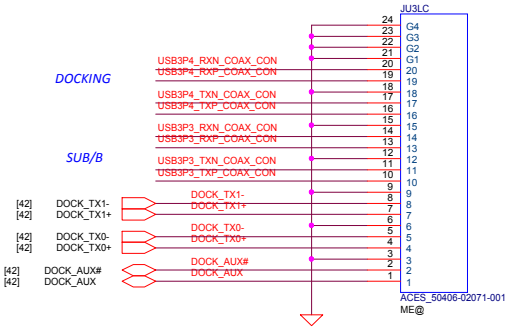
Date: Wednesday, September 23, 2015 | Sheet 55 of 99



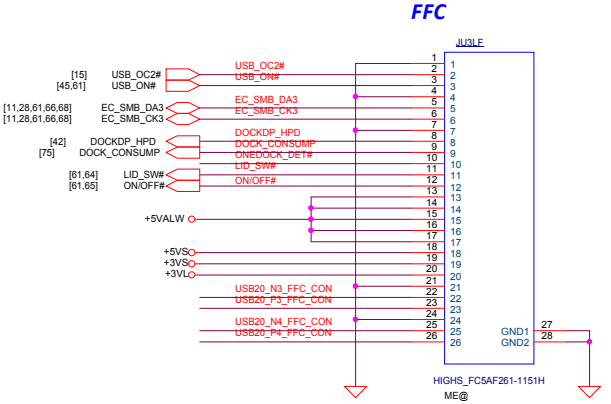


1. AC Capacitor place on Sub/B
2. Need to check with MUX IC vendor whether still need AC cap between MUX IC and device

CABLE



FFC

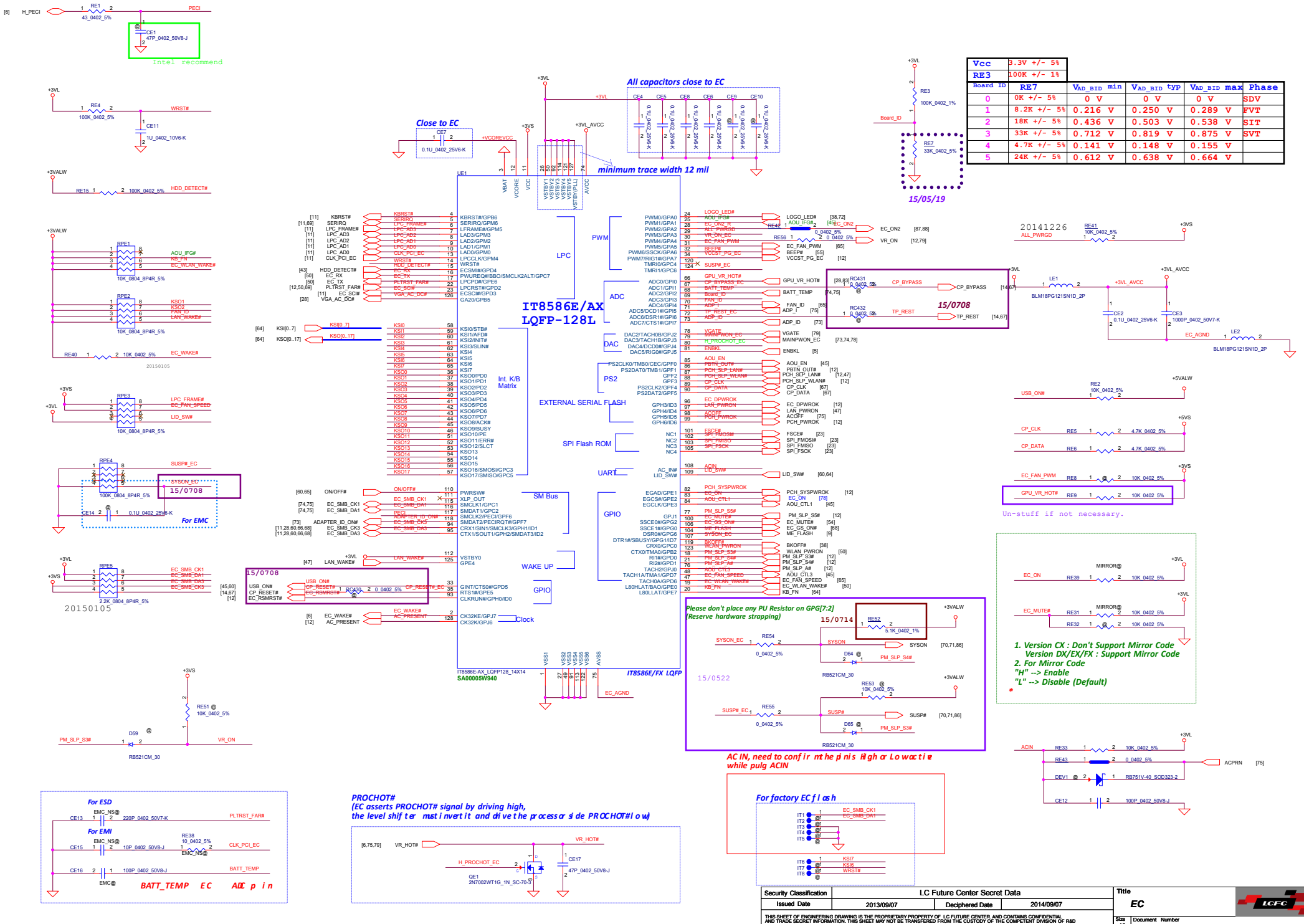


Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: DOCKING/ DCIN CONN

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 60 of 99



Vcc	3.3V +/- 5%			
RE3	100K +/- 1%			

Board ID	RE7	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	FVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	SIT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SVT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

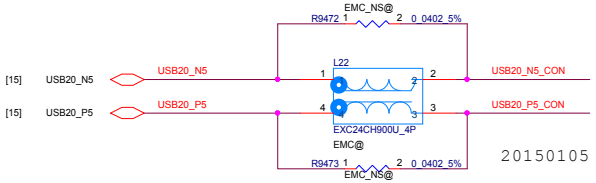
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: EC

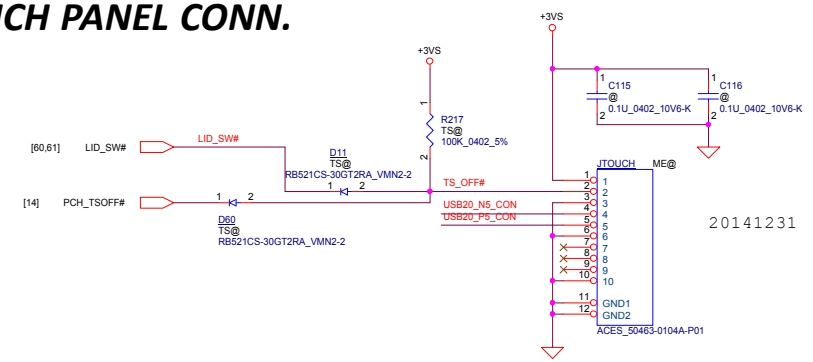
Size: A2 | Document Number: BE560 | Rev: 0.1

Date: Wednesday, September 23, 2015 | Sheet 61 of 99

TOUCH PANEL CONN.

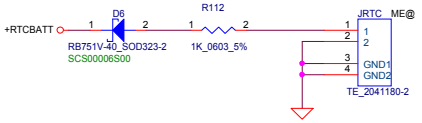


20150105

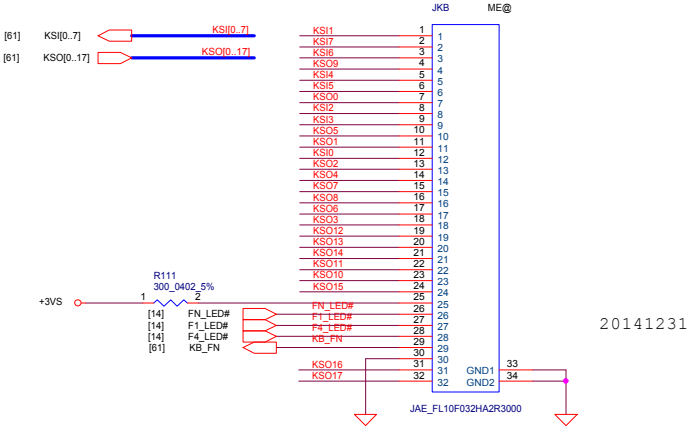


20141231

RTC CONN.



KB CONN



20141231

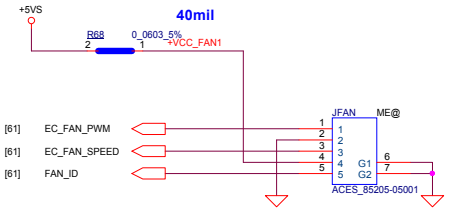
Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

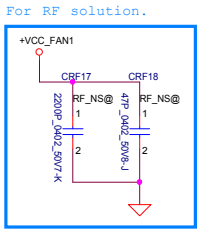
Title: KB/RTC/TOUCH PAN CONN.

Size	Document Number	Rev
Custom	BE560	0.1

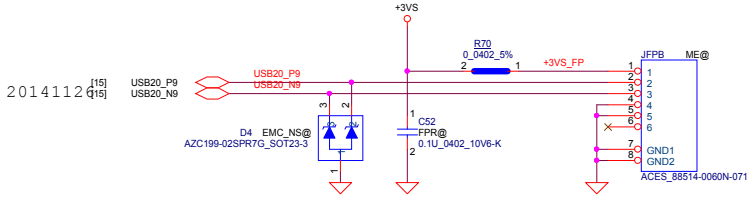
Date: Wednesday, September 23, 2015 | Sheet 64 of 99

FAN CONN.





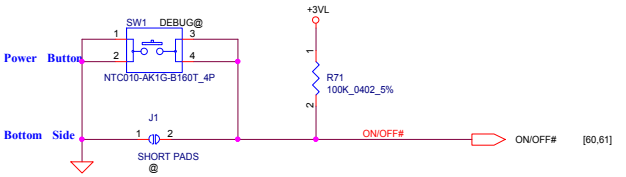
FingerPrint CONN.



PWR BTN/LID SW CONN.

For 14" on board
For 15" on Sub/B

ON/OFF Switch --> Sub/B



Lid Switch --> Sub/B

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

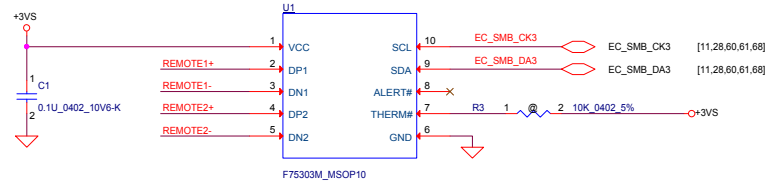
Title: PBTN/LID/FP/FAN CONN.

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 Sheet 65 of 99

Thermal Sensor

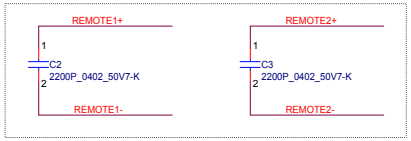
Thermal Sensor
placed near by VRAM



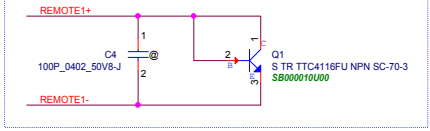
Address 1001_101xb

Internal pull up 1.2K to 1.5V
R for init i d ther mal shut do wn t e mp

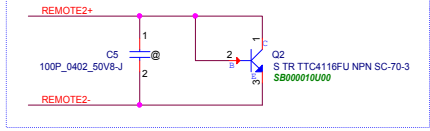
Close to U1



Close to +VCC_CORE



Close JDIMM1&JDIMM2



REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

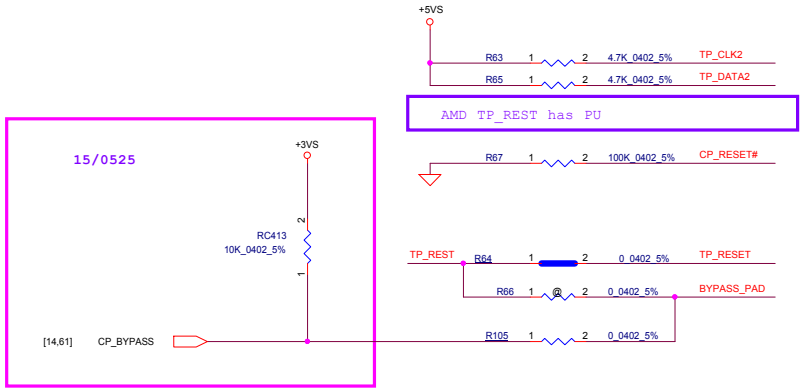
Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: *Thermal Sensor*

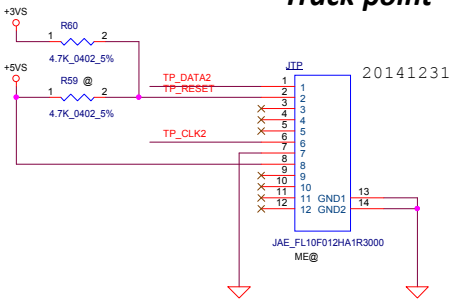
Size	Document Number	Rev
Custom	*BE560*	0.1

Date: Wednesday, September 23, 2015 Sheet 66 of 99

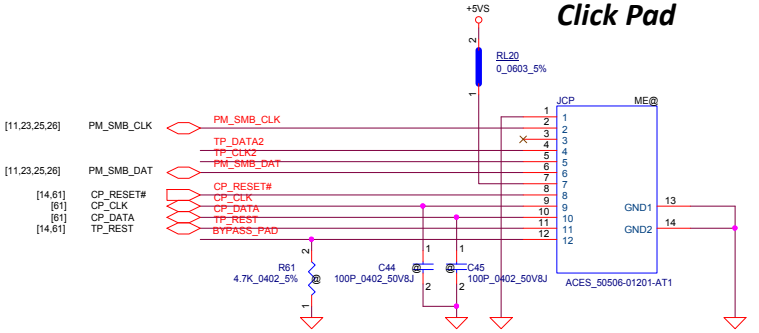
15/0525



Track point



Click Pad

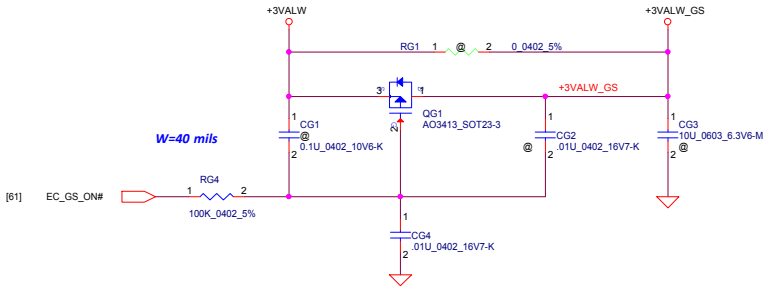


Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: CP/TPOINTCONN.

Size	Document Number	Rev
Custom	BE560	0.1

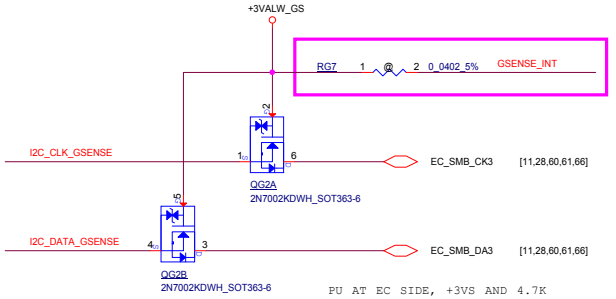
Date: Wednesday, September 23, 2015 | Sheet 67 of 99



APS G-Sensor

TABLE

P/N	ADDR_SEL	Address
LIS3DH	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX023-1025	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

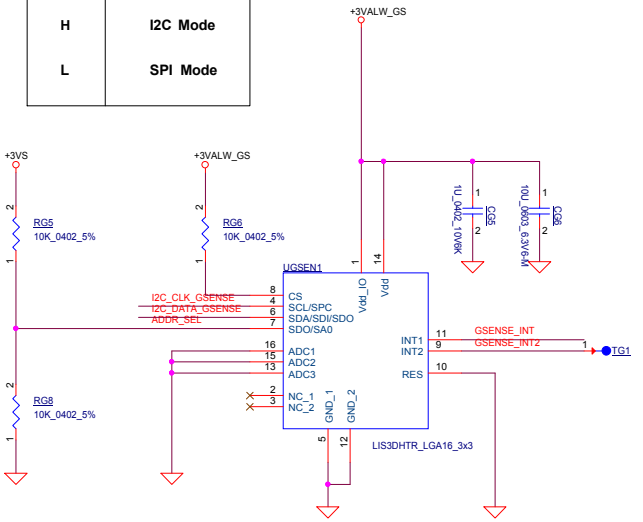


PU AT EC SIDE, +3VS AND 4.7K

20141204

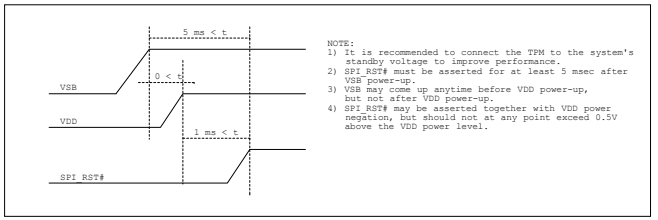
TABLE

P/N	Mode Selection
H	I2C Mode
L	SPI Mode

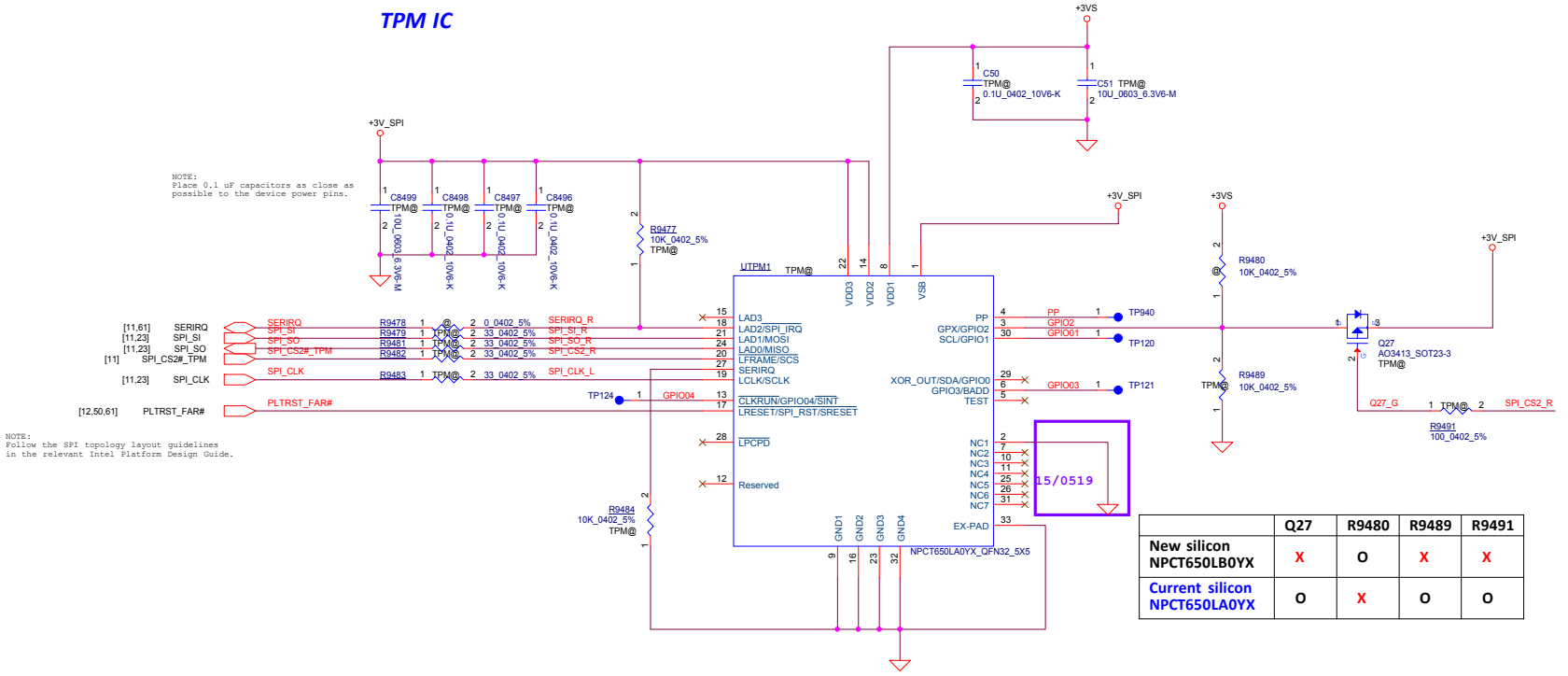


Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title	G SENSOR		
Size	Document Number		Rev
Custom	BE560		0.1
Date:	Wednesday, September 23, 2015	Sheet	68 of 99



TPM IC



	Q27	R9480	R9489	R9491
New silicon NPCT650LB0YX	X	O	X	X
Current silicon NPCT650LA0YX	O	X	O	O

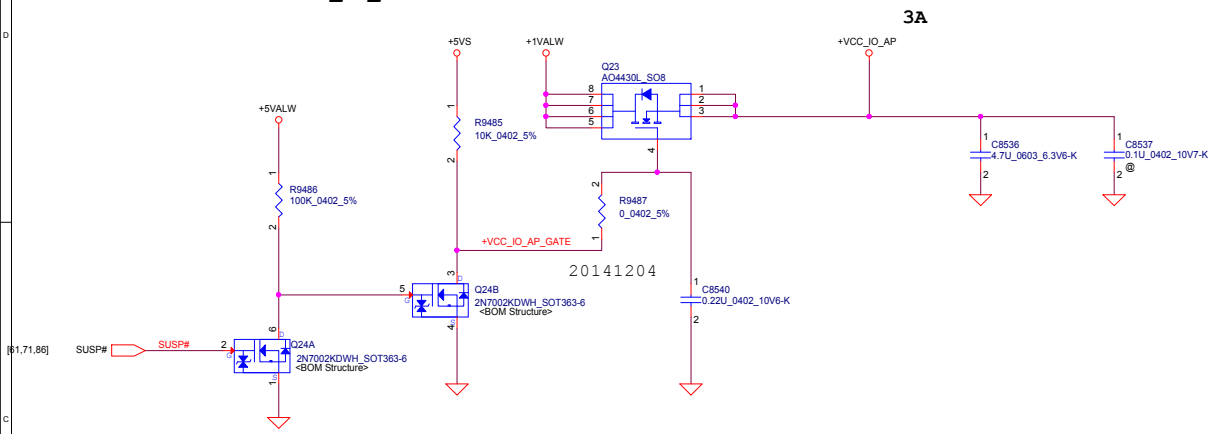
Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

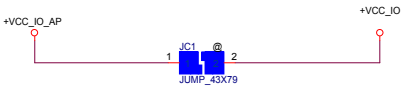
Title: TPM

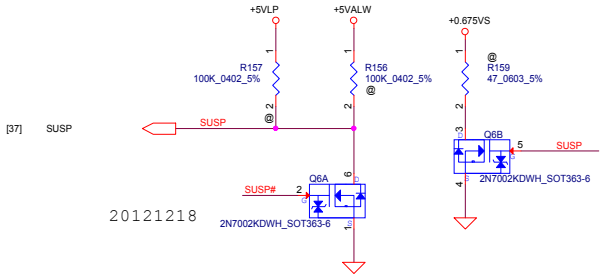
Size: Custom | Document Number: BE560 | Rev: 0.1

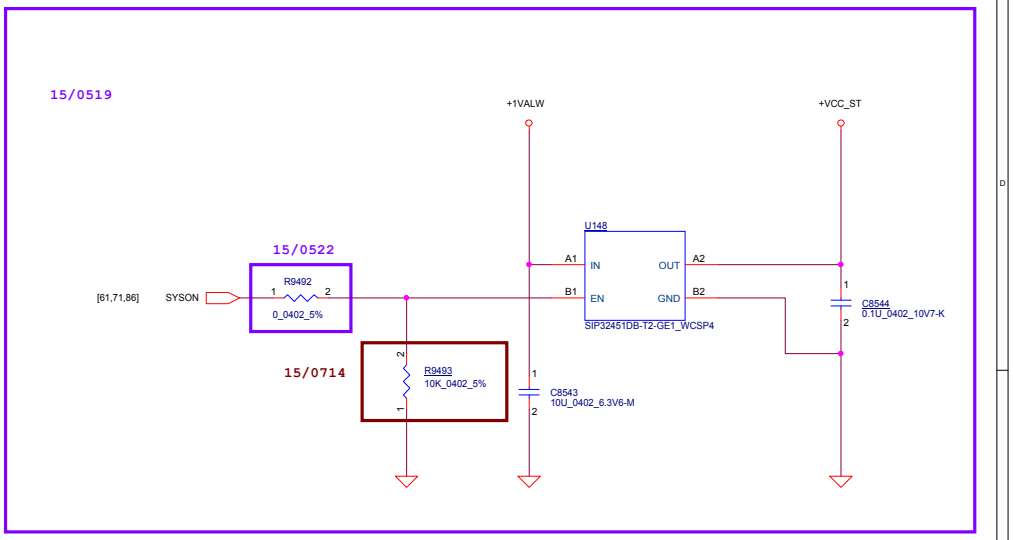
Date: Wednesday, September 23, 2015 | Sheet 69 of 99

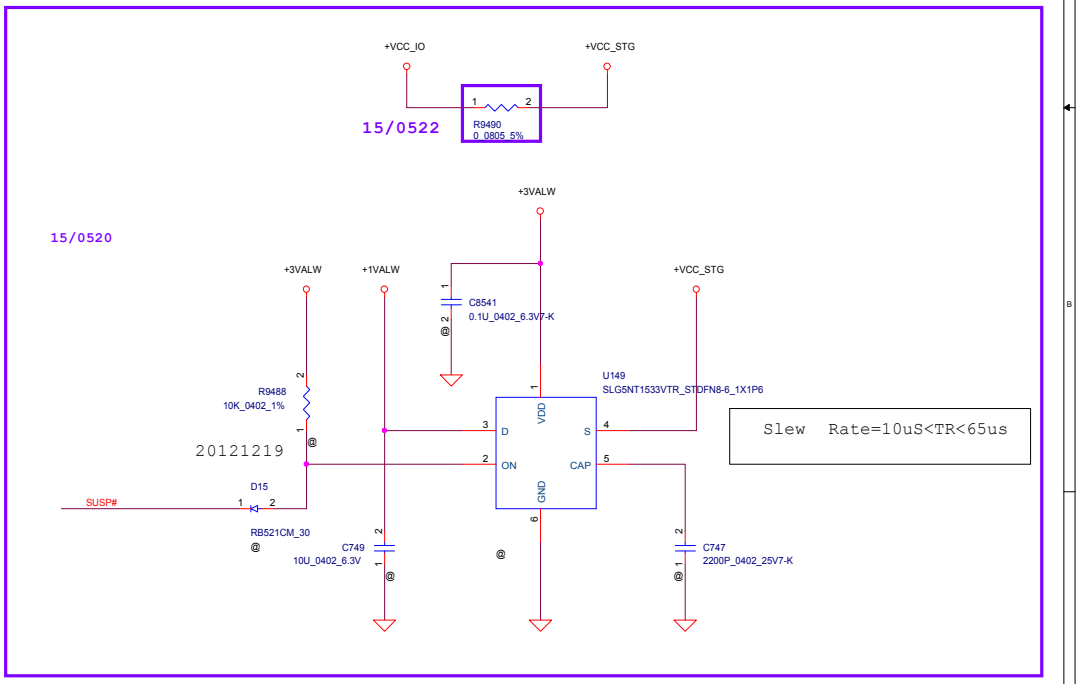
+1VALW to +VCC_IO_AP











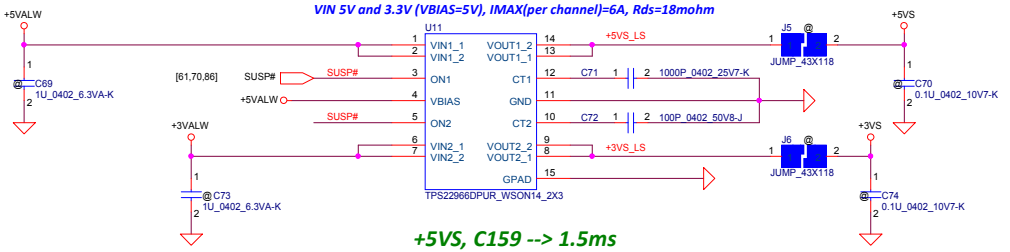
Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: VCC_IO and VCC_ST LSW

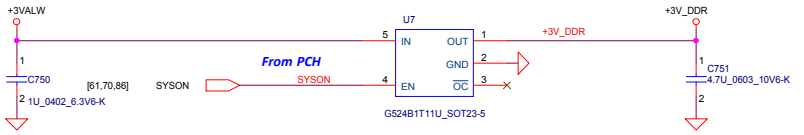
Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 70 of 99

Load Switch
+5VALW To +5VS
+3VALW To +3VS



+3VALW to +3V_DDR



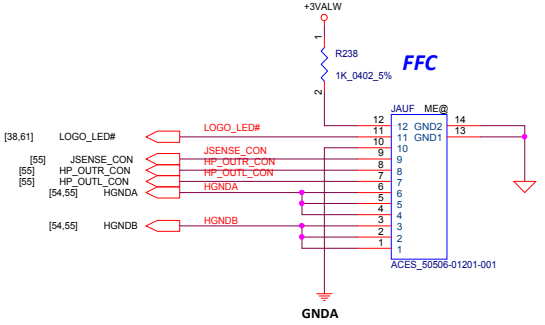
Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **DC V TO VS/ V-PCH/VM**

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 71 of 99

For Edge 15'' Audio board CONNECTOR

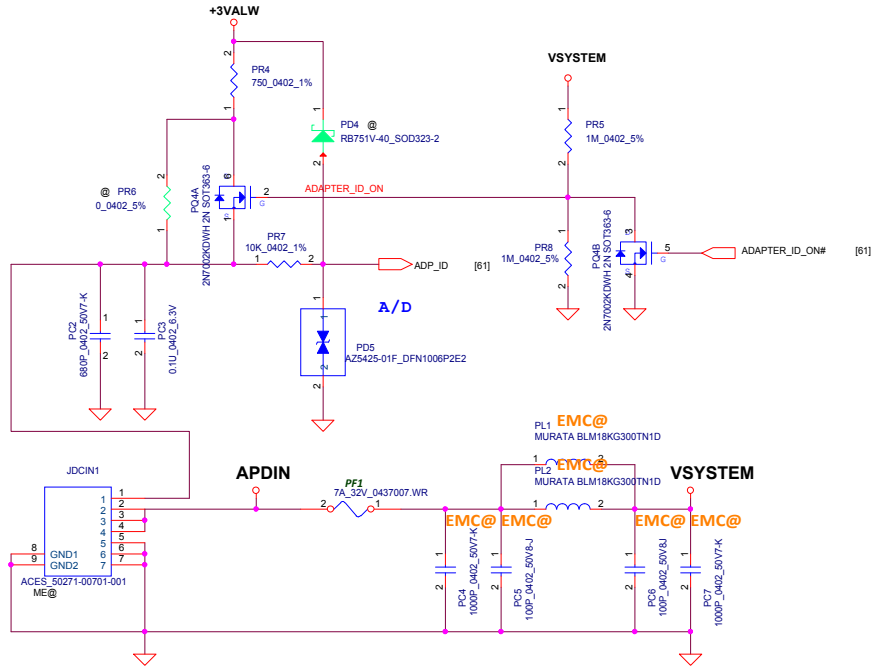


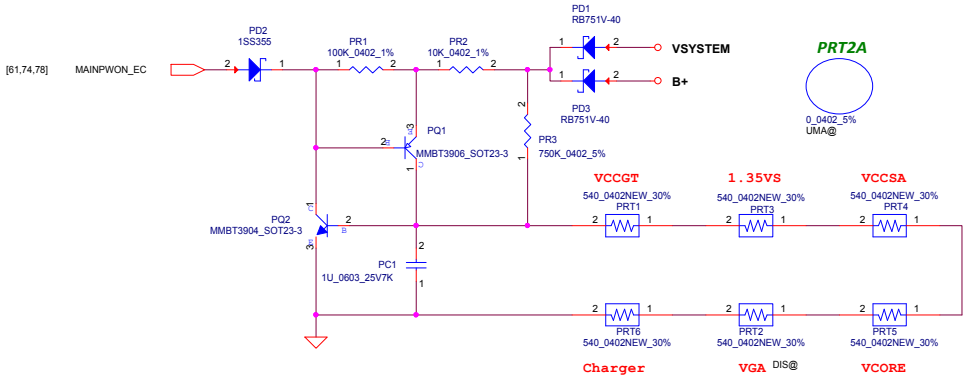
Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

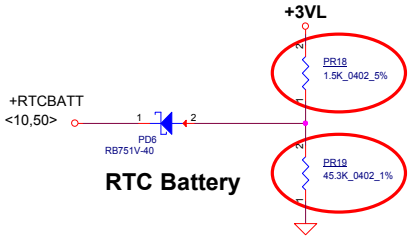
Title: **SUB-AUDIO JACK CONN.**

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 72 of 99





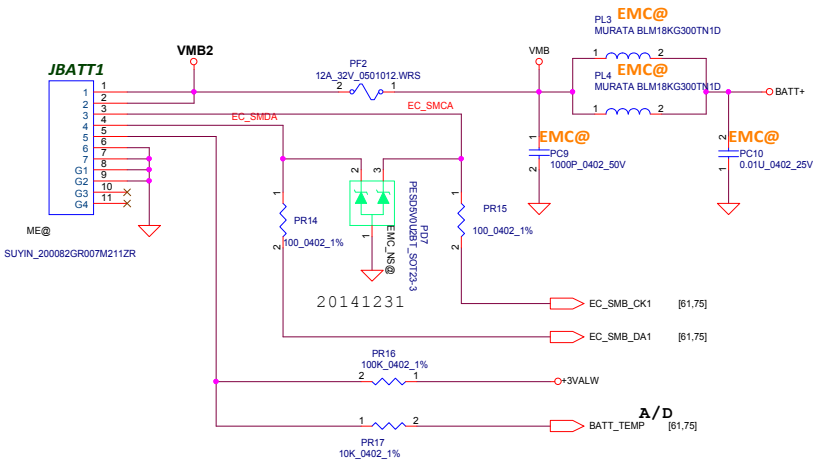


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

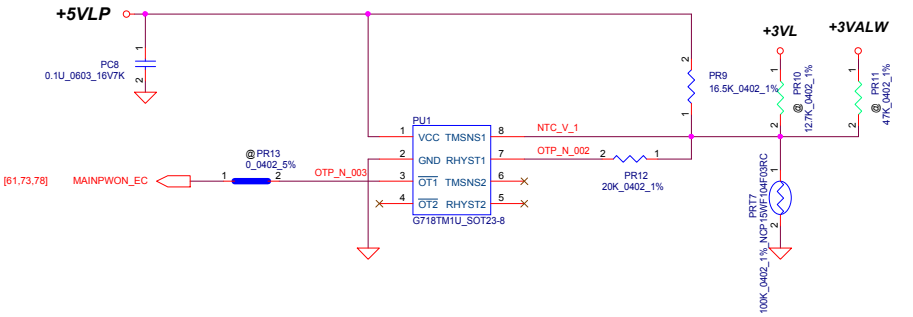
Title: DCIN / Vin Detector

Size	Document Number	Rev
Custom	AIVL2 NM-A351	0.1

Date: Wednesday, September 23, 2015 | Sheet 73 of 99



PRT7 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

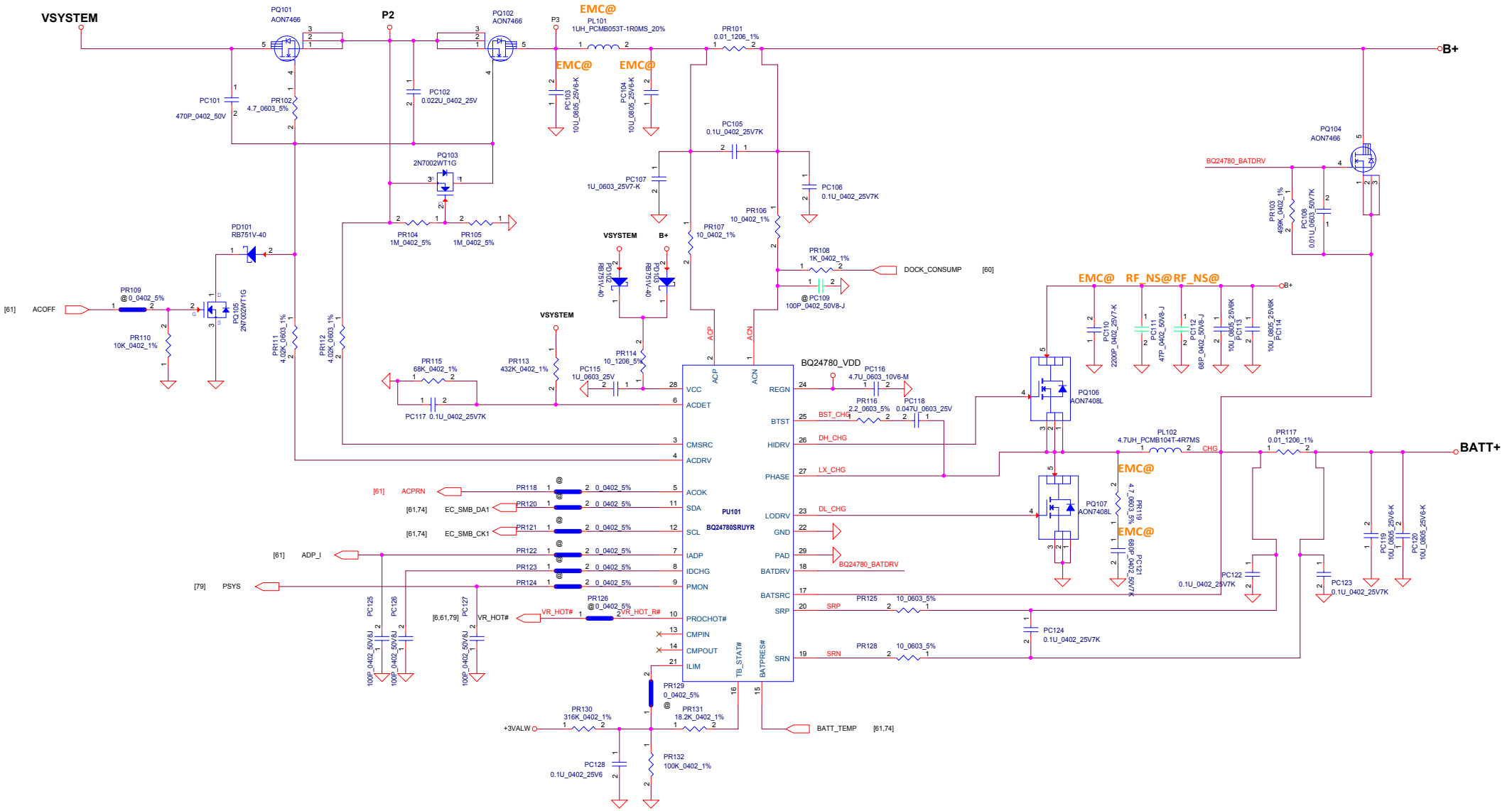


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	AIVL2 NM-A351	0.1

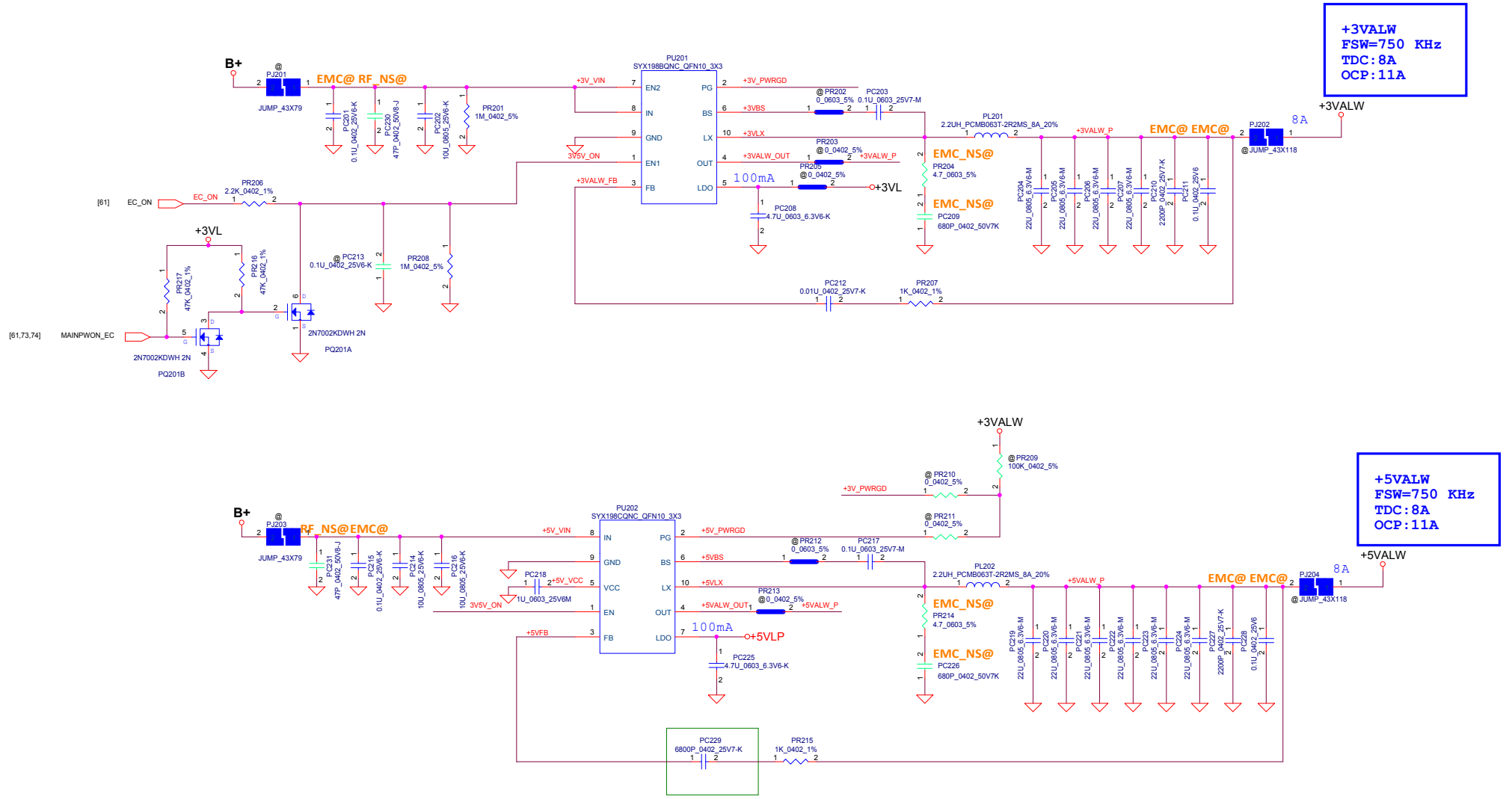
Date: Wednesday, September 23, 2015 | Sheet 74 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	CHARGER		
Size	Document Number		Rev
Custom	AIVL2 NM-A351		0.1
Date:	Wednesday, September 23, 2015	Sheet	75 of 99

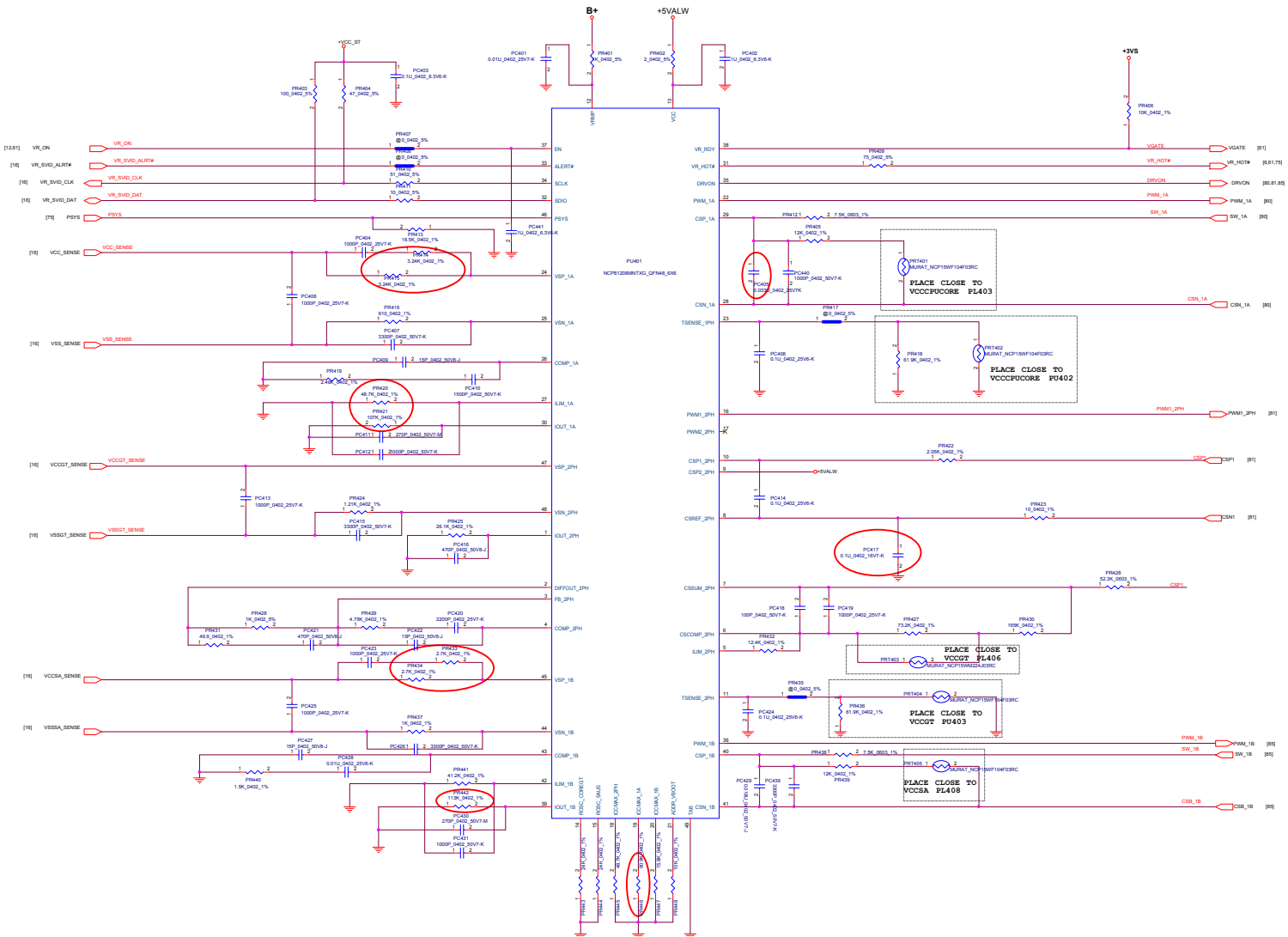


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	AIVL2 NM-A351	0.1

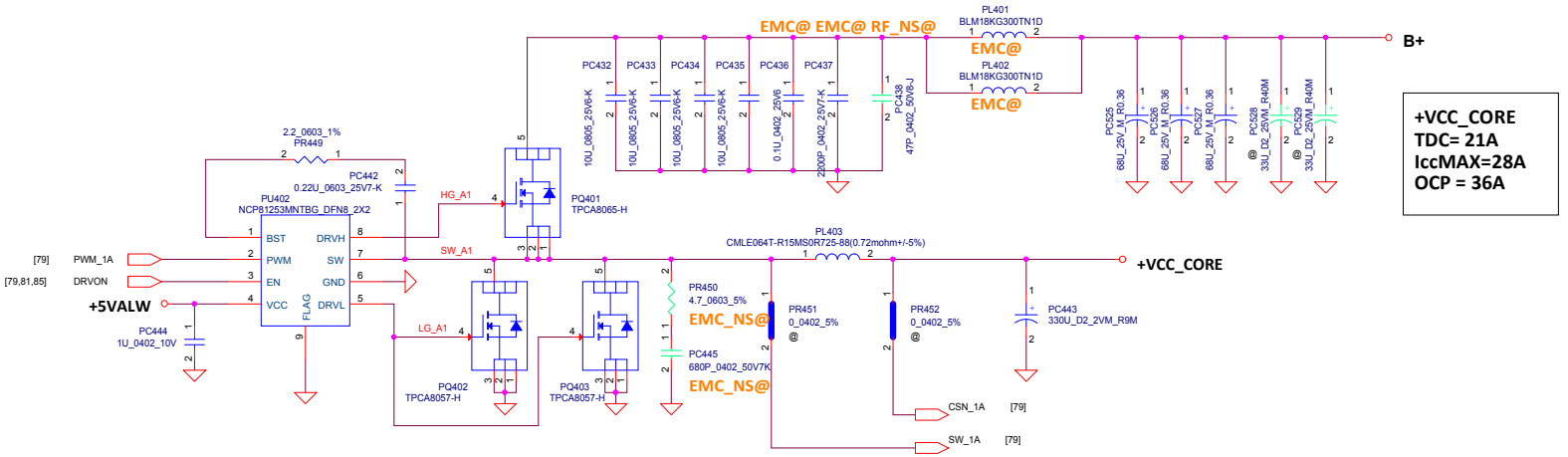
Date: Wednesday, September 23, 2015 | Sheet 78 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THE SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	MVP8		
Size: A1	Document Number: AIVL2 NM-A351		Rev: 0.1
Date: Wednesday, September 23, 2015	Sheet 29 of 50		

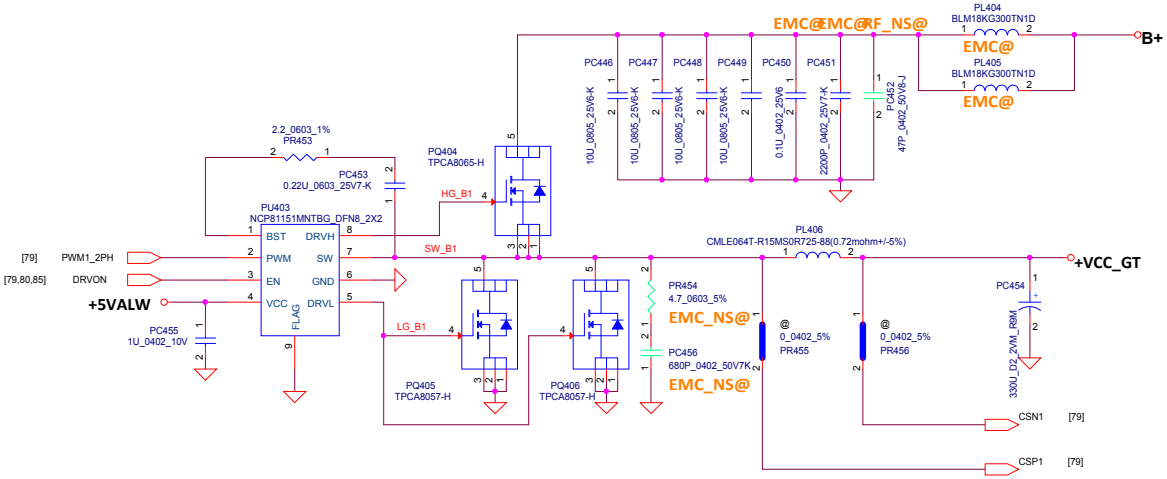


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +VCC_CORE

Size: Custom | Document Number: AIVL2 NM-A351 | Rev: 0.1

Date: Wednesday, September 23, 2015 | Sheet 80 of 99



+VCC_GT
TDC= 18A
IccMAX=31A
OCP min = 40A

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

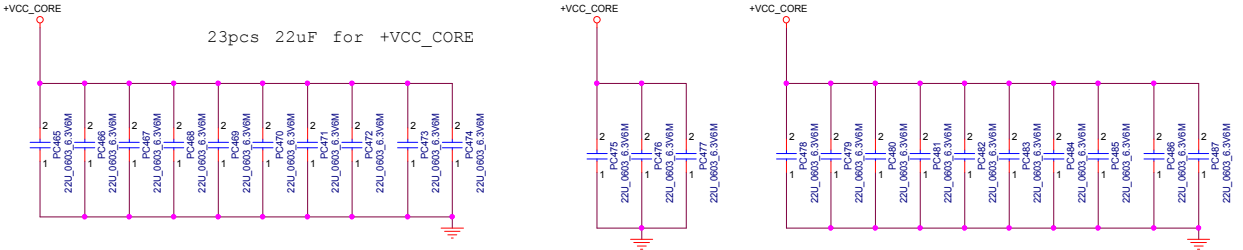
Title: +VCC_GT

Size	Document Number	Rev
Custom	AIVL2 NM-A351	0.1

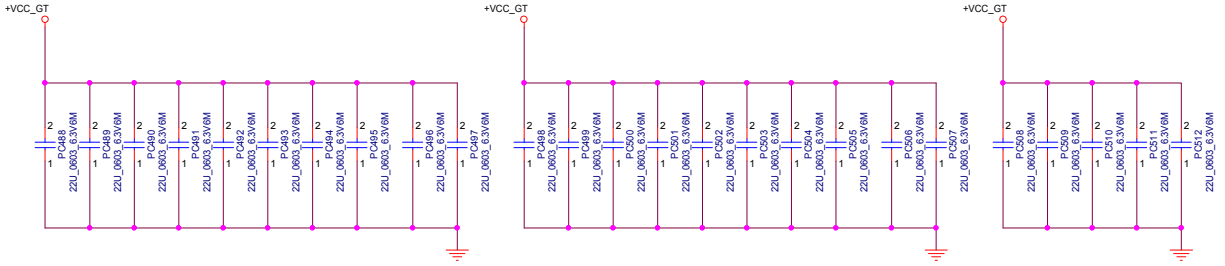
Date: Wednesday, September 23, 2015 Sheet 81 of 99

Based on PDDG rev 0.7 Table 5-1.

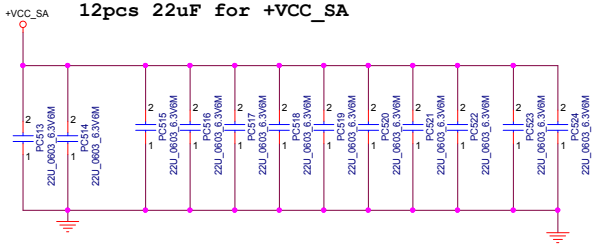
23pcs 22uF for +VCC_CORE



25pcs 22uF for +VCC_GT



12pcs 22uF for +VCC_SA



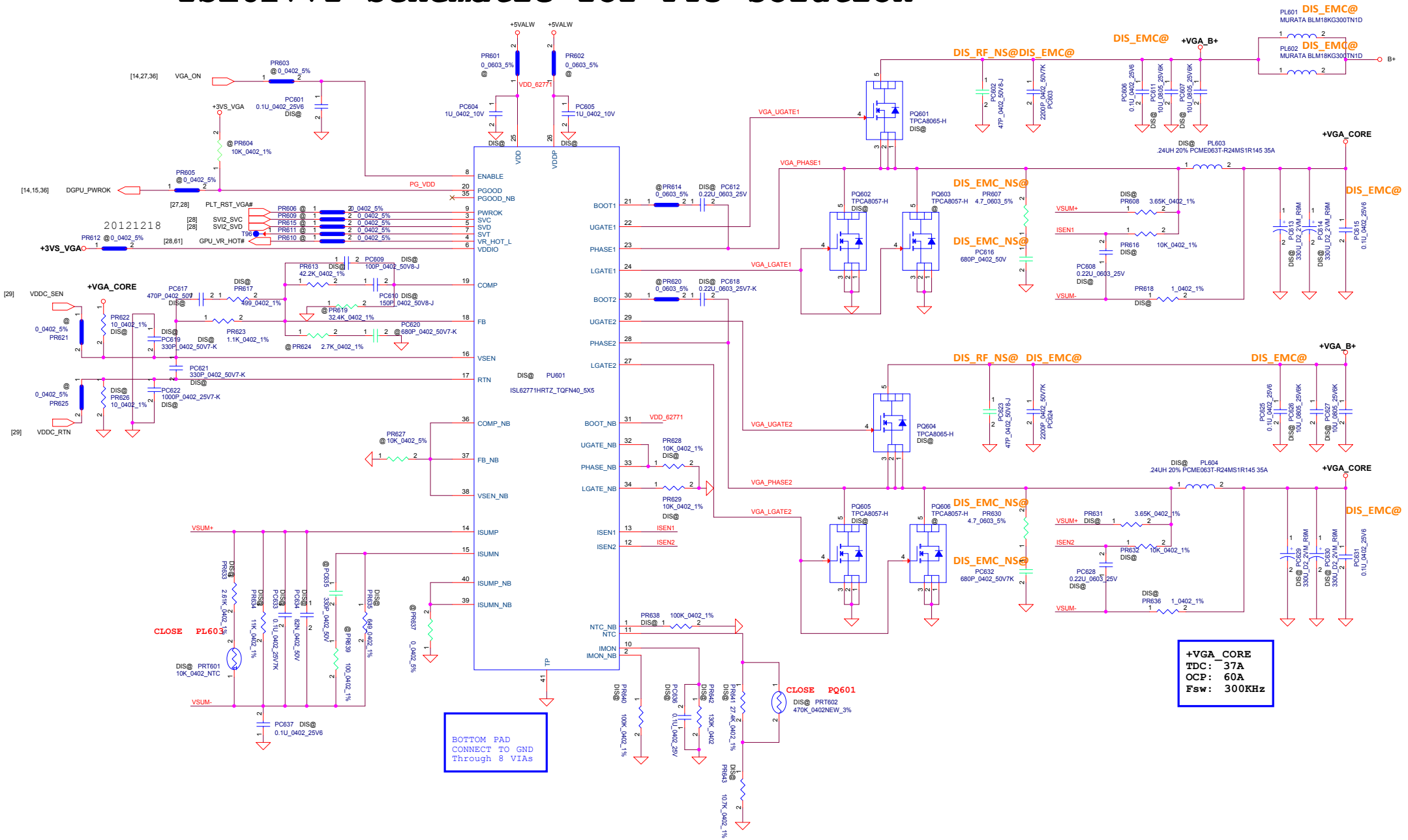
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **PROCESSOR DECOUPLING**

Size	Document Number	Rev
Custom	AIVL2 NM-A351	0.1

Date: Wednesday, September 23, 2015 Sheet 82 of 99

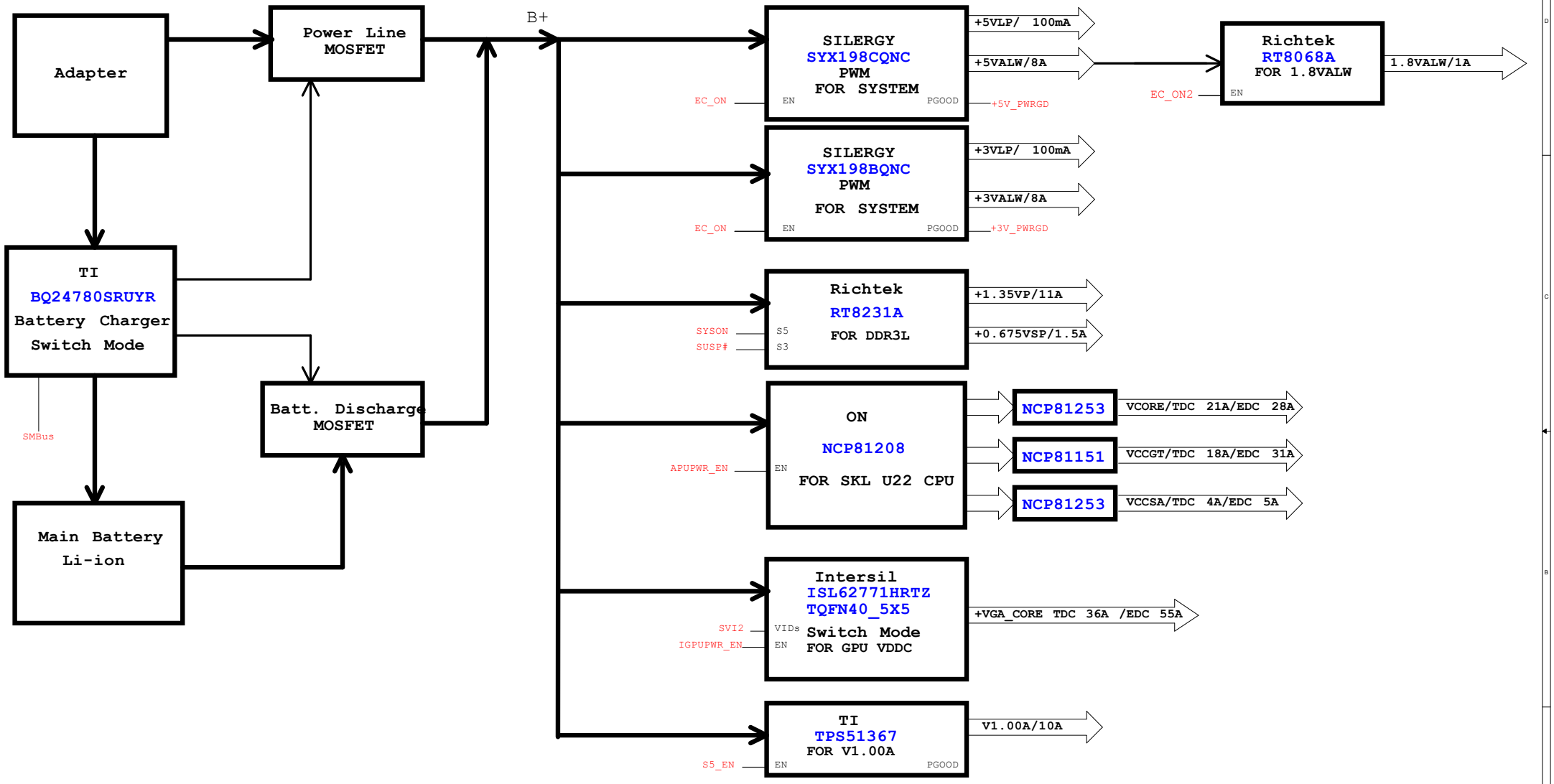
ISL62771 Schematic for FT3 solution



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	+VGA_CORE		
Size	Custom	Document Number	AIVL2 NM-A351
Rev	0.1		
Date:	Wednesday, September 23, 2015	Sheet	83 of 99

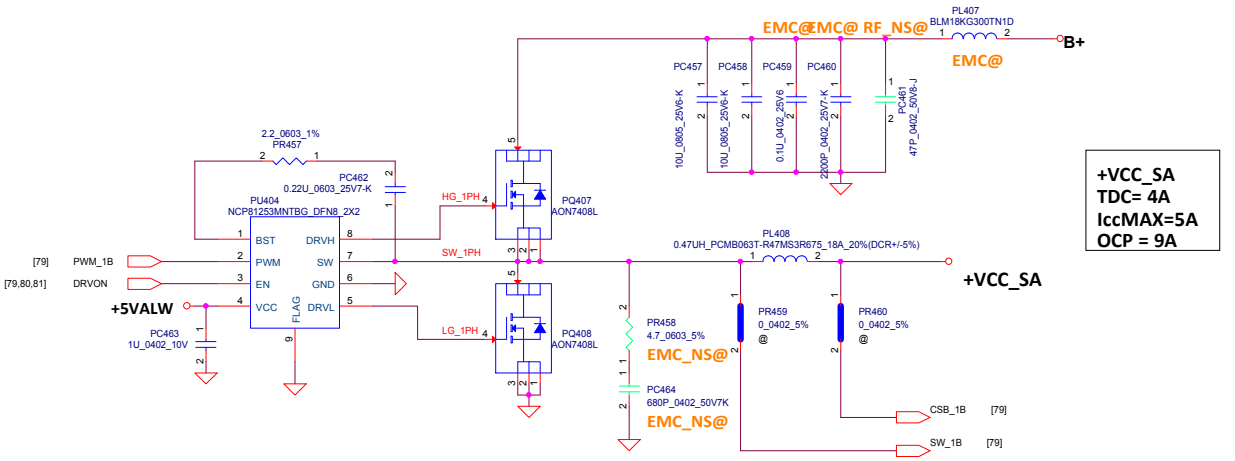


Security Classification	LC Future Center Secret Data		
Issued Date		Deciphered Date	

Title: *Block Diagram*

Size	Document Number	Rev
Custom	AIVL2_NM-A351	0.1

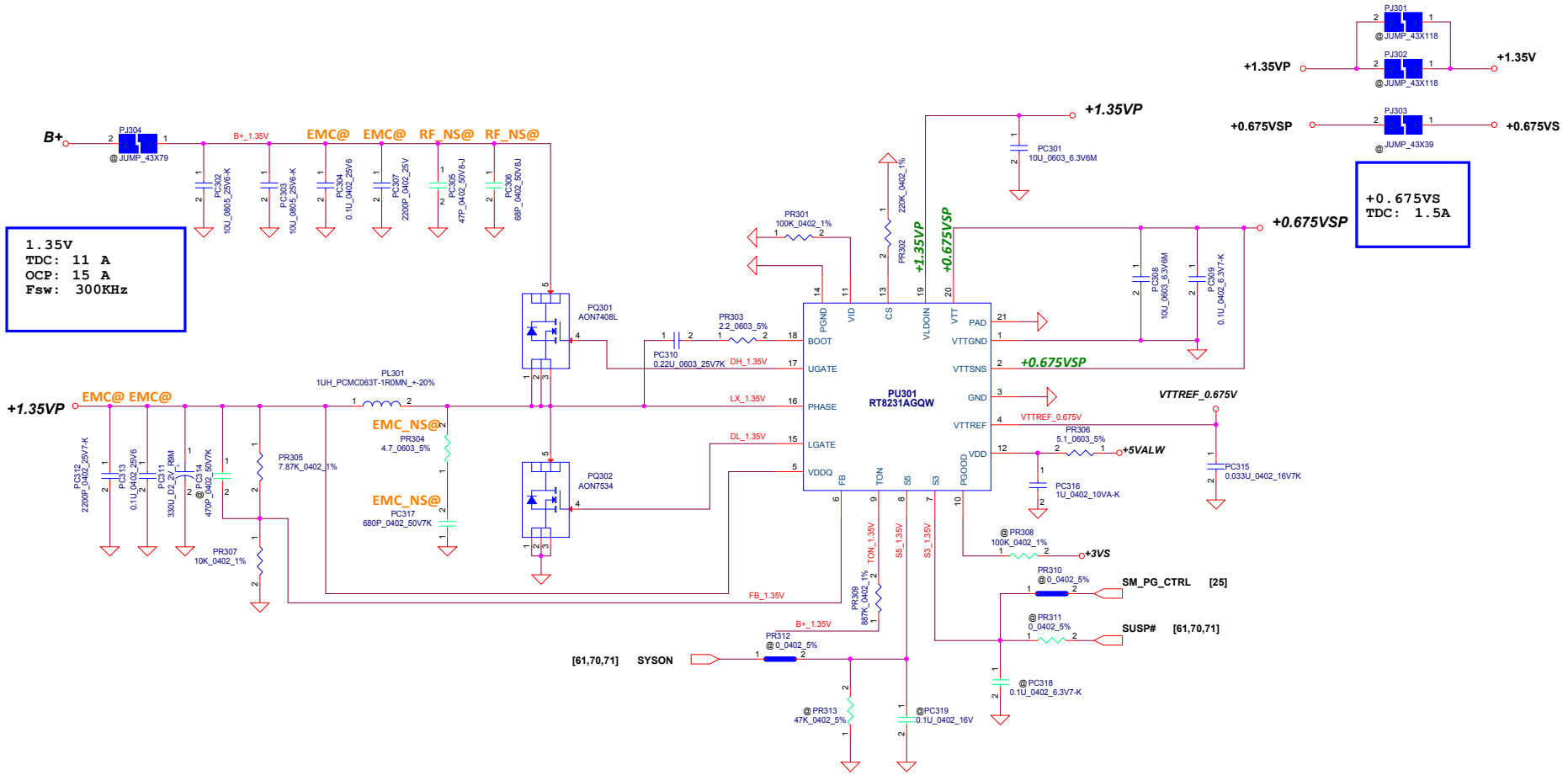
Date: Wednesday, September 23, 2015 | Sheet 84 of 99



Title: VCCSA

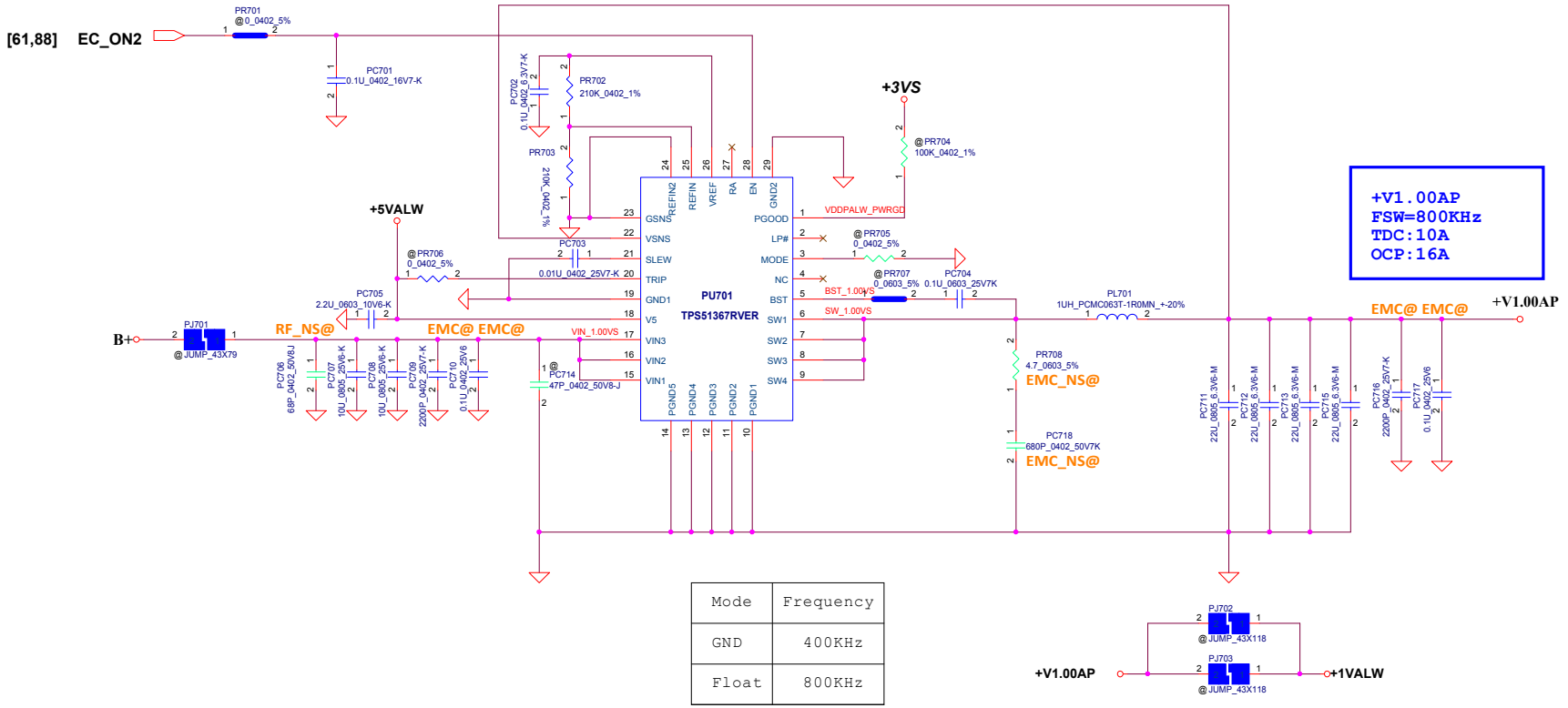
Size	Document Number	Rev
Custom	AIVL2 NM-A351	0.1

Date: Wednesday, September 23, 2015 | Sheet 85 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+1.35V/+0.675VS		
Size	Document Number		Rev
Custom	AIVL2 NM-A351		0.1
Date:	Wednesday, September 23, 2015	Sheet	86 of 99

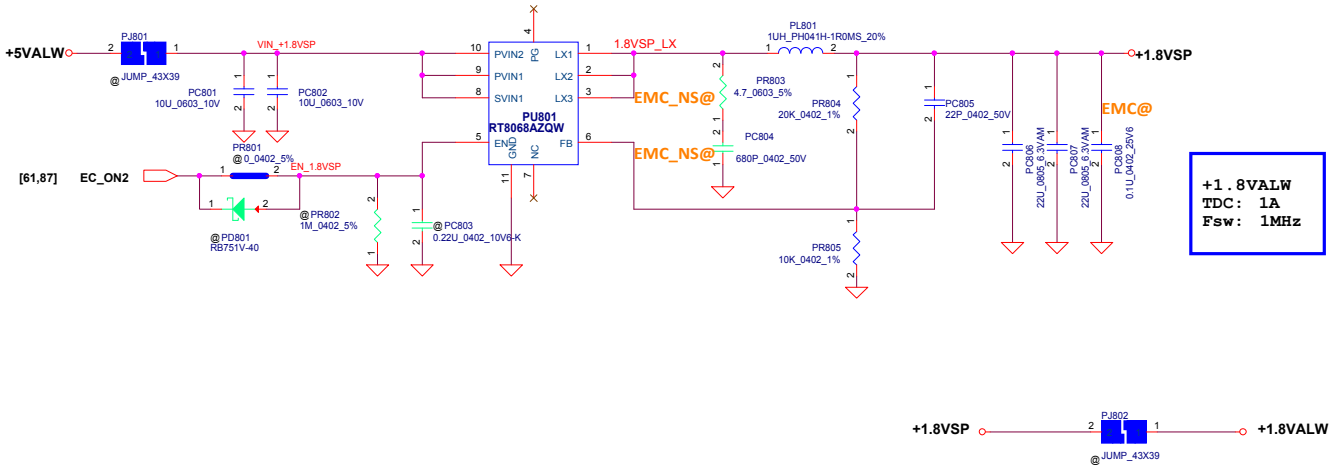


Mode	Frequency
GND	400KHz
Float	800KHz

Title: *+V1.00A*

Size	Document Number	Rev
Custom	AIVL2 NM-A351	0.1

Date: Wednesday, September 23, 2015 Sheet 87 of 99



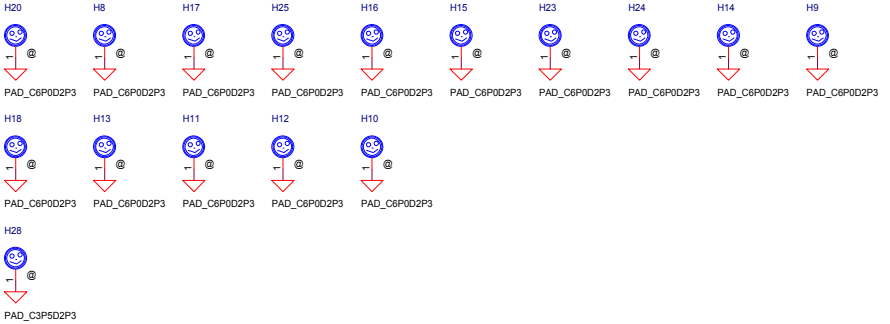
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: *+1.8VS_VGA*

Size	Document Number	Rev
Custom	*AIVL2 NM-A351*	0.1

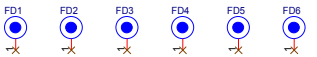
Date: Wednesday, September 23, 2015 | Sheet 88 of 99

Screw Hole



Center Zero

PCB Fedical Mark PAD



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: XXXX

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 99 of 99