BUCKY_WHL Schematic

2018/04/10

REV : X01

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*

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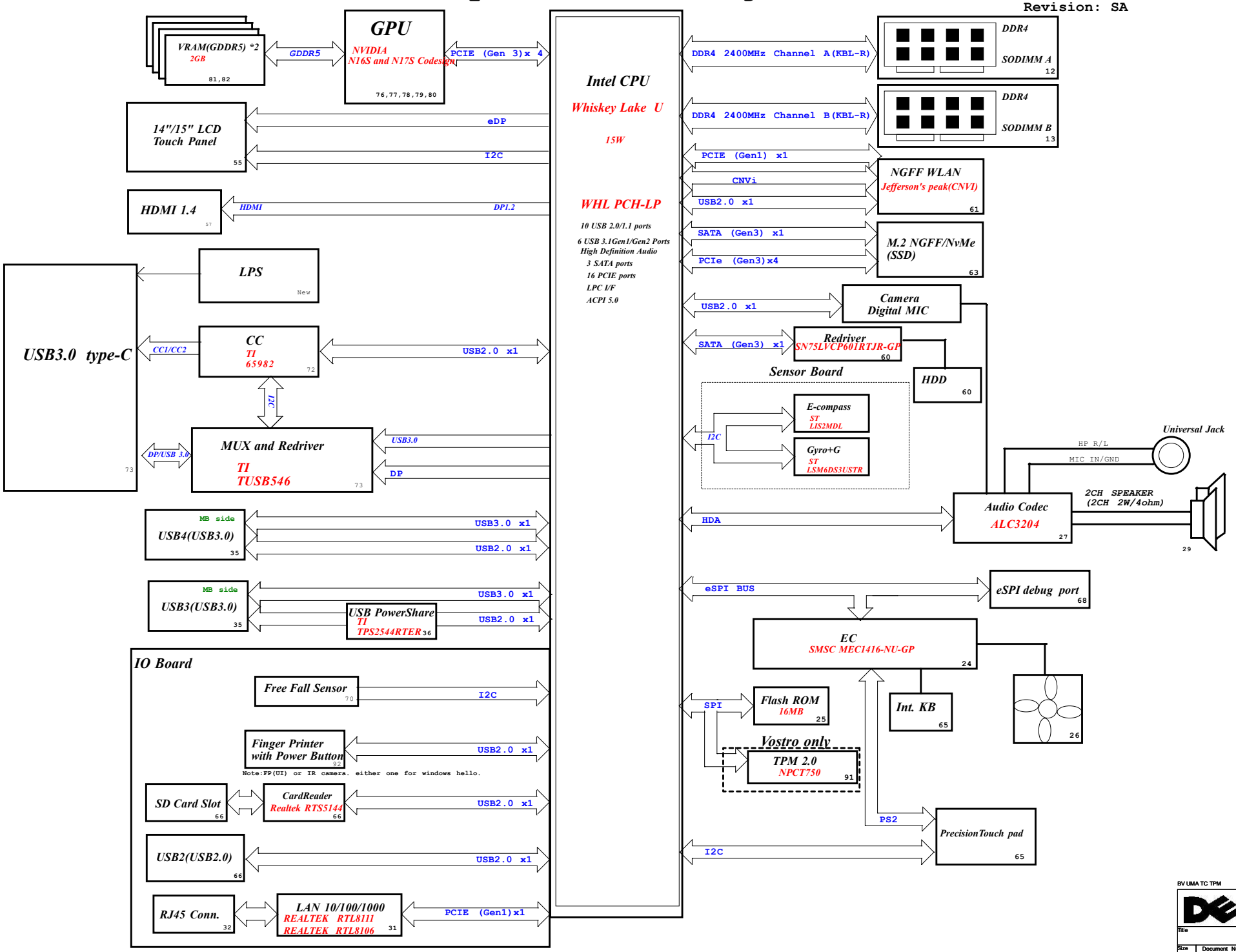
Bucky WHL Block Diagram

Project code:
PCB P/N: 17859
Revision: SA



CHARGER	
ISL88739	44
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	OUTPUTS
DCBATOUT	3D3V_PWR 3D3V_S5 5V_PWR 5V_S5

CPU Core Power	
NCP81208MNTXG	46~50
NCP81382MNTXG x 2	
NCP81382MNTXG (23e)	
NCP81253MNTBG	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCGT (23e)
DCBATOUT	+VCCSA

DDR4 SUS	
RT8231AGQW-GP APL5930KAI-TRG	51
INPUTS	OUTPUTS
DCBATOUT 3D3V_S5	1D2V_S3 0D6V_S0 2D5V_S3

CPU VCCPRIM_CORE 1v	
	11
INPUTS	OUTPUTS
1D0V_S5	+VCCPRIM_CORE

CPU DCDC-V1D00A	
AOZ2262QI-10-GP-U	53
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D8V	
APL5930KAI-TRG	54
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0	
TPS22966DPUR-GP	40
INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

EOPIO/EDRAM (23e)	
TPS22961DNYT	40
INPUTS	OUTPUTS
1D0V_S5 1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR

3D3V VGA	
AO3419L	86
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0

VGA_CORE	
ISL62771HRTZ-GP-U	85
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

1D5V_VGA_S0	
Y8288RAC-GP	86
INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0

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Title: Block Diagram

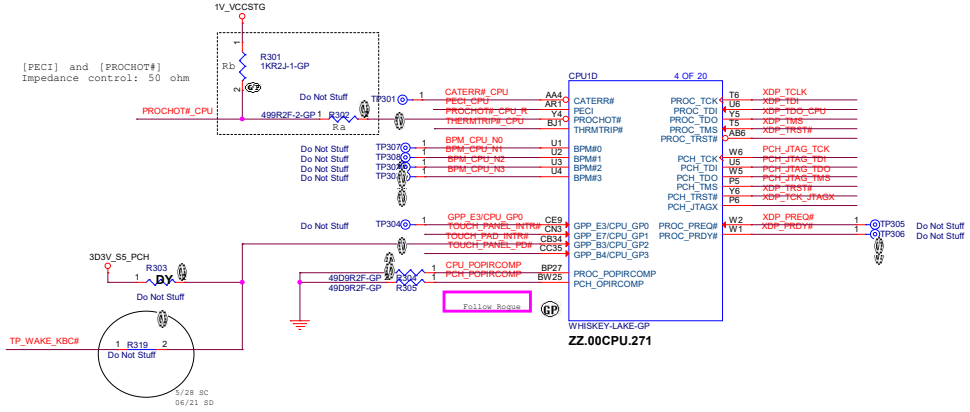
Size: A2 | Document Number: Bucky WHL | Rev: SA

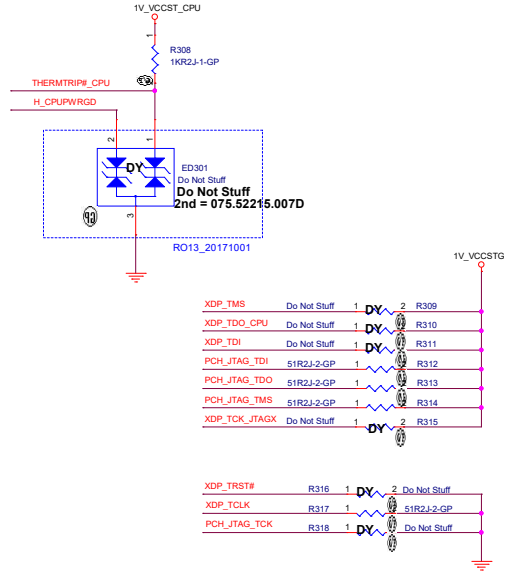
Date: Friday, July 13, 2018 | Sheet 2 of 105

SSID = CPU

24 PECI_CPU
24,44,46 PROCHOT#_CPU
55 TOUCH_PANEL_INTR#
24,65 TP_WAKE_KBC#
17 H_CPUPWRGD
55 TOUCH_PANEL_PD#

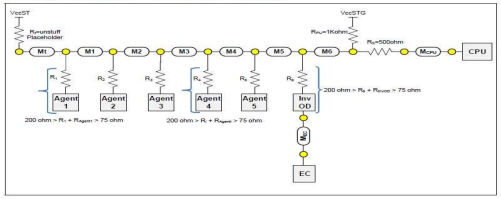
99 XDP_TCLK
99 XDP_TDO_CPU
99 XDP_TDI
99 XDP_TMS
99 XDP_TCK_JTAGX
99 PCH_JTAG_TDO
99 PCH_JTAG_TDI
99 PCH_JTAG_TMS





(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

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Title: CPU (THML/JTAG)

Size	Document Number	Rev
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SSID = CPU

DP to HDMI2.0

57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N3
57 HDMI_DDI_TX_P3

57 HDMI_HPD_CPU
57 HDMI_SDA_CPU
57 HDMI_SCL_CPU

DP for Type-C Mux

73 DP2_DDI_TX_N0
73 DP2_DDI_TX_P0
73 DP2_DDI_TX_N1
73 DP2_DDI_TX_P1
73 DP2_DDI_TX_N2
73 DP2_DDI_TX_P2
73 DP2_DDI_TX_N3
73 DP2_DDI_TX_P3
73 DP2_AUX_CPU_P
73 DP2_AUX_CPU_N

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1

55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
55 eDP_HPD_CPU
72,73 DP1_HPD_CPU

24 L_BKLT_EN
55 L_BKLT_CTRL
55 EDP_VDD_EN

15 GPP_H17_STRAP

2016/11/01modify

3D3V_S0
RN401
1 2 4 3
HDMI_SDA_CPU
HDMI_SCL_CPU
SRN2K2J-1-GP

3D3V_S0
SRN2K2J-1-GP
1 2 4 3
CPU_DP2_CTRL_DATA
CPU_DP2_CTRL_CLK
RN403

1.65GT Length 6.5" (3VIA)

DP to HDMI2.0

DP for Type-C Mux

CPU1A 1 OF 20

HDMI_DDI_TX_N2	AL5	DDI1_TXN0	EDP_TXN0 AG4
HDMI_DDI_TX_P2	AL6	DDI1_TXP0	EDP_TXP0 AG3
HDMI_DDI_TX_N1	AJ5	DDI1_TXN1	EDP_TXN1 AG2
HDMI_DDI_TX_P1	AJ6	DDI1_TXP1	EDP_TXP1 AG1
HDMI_DDI_TX_N0	AF6	DDI1_TXN2	EDP_TXN2 AJ4
HDMI_DDI_TX_P0	AF5	DDI1_TXP2	EDP_TXP2 AJ3
HDMI_DDI_TX_N3	AE5	DDI1_TXN3	EDP_TXN3 AJ2
HDMI_DDI_TX_P3	AE6	DDI1_TXP3	EDP_TXP3 AJ1
DP2_DDI_TX_N0	AC4	DDI2_TXN0	
DP2_DDI_TX_P0	AC3	DDI2_TXP0	
DP2_DDI_TX_N1	AC1	DDI2_TXN1	EDP_AUX_N AH4
DP2_DDI_TX_P1	AC2	DDI2_TXP1	EDP_AUX_P AH3
DP2_DDI_TX_N2	AE4	DDI2_TXN2	DISP_UTILS AM7
DP2_DDI_TX_P2	AE3	DDI2_TXP2	AC7
DP2_DDI_TX_N3	AE1	DDI2_TXN3	DDI1_AUX_N AC6
DP2_DDI_TX_P3	AE2	DDI2_TXP3	DDI1_AUX_P AD4
			DDI2_AUX_N AD3
			DDI2_AUX_P AG7
			DDI3_AUX_N AG6
			DDI3_AUX_P

eDP_TX_CPU_N0
eDP_TX_CPU_P0
eDP_TX_CPU_N1
eDP_TX_CPU_P1
eDP_AUX_CPU_N
eDP_AUX_CPU_P
DP2_AUX_CPU_N
DP2_AUX_CPU_P

Length 2"~10" (2VIA)
Cable Length 4"~15"
Length 10" (3VIA)

for HDMI2.0
TYPE-C MUX

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6 HDMI_HPD_CPU
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6 DP1_HPD_CPU_R
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7 SIO_EXT_SMI#
GPP_E16/DPPE_HPD3/DISP_MISC3 CP6 eDP_HPD_CPU
GPP_E17/EDP_HPD/DISP_MISC4 CM7

EDP_BKLTEN CK11 L_BKLT_EN
EDP_VDDEN CG11 EDP_VDD_EN
EDP_BKLTCTL CH11 L_BKLT_CTRL

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ± 1% Ω resistor

RO13_20170626

1V_VCCIO
R401
1 2
24D9R2F-L-GP
eDP_RCOMP_CPU AM6 DISP_RCOMP

HDMI_SCL_CPU CC8 GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
HDMI_SDA_CPU CC9 GPP_E19/DPPB_CTRLDATA

CPU_DP2_CTRL_CLK CH4 GPP_E20/DPPC_CTRLCLK
CPU_DP2_CTRL_DATA CH3 GPP_E21/DPPC_CTRLDATA

Do Not Stuff TP402 1 GPP_E23 CP4 CN4 GPP_E22/DPPD_CTRLCLK
GPP_E23/DPPD_CTRLDATA

GPP_H17_STRAP CR26 CP26 GPP_H16/DDPF_CTRLCLK
GPP_H17/DDPF_CTRLDATA

WHISKEY-LAKE-GP
ZZ.00CPU.271

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ± 1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ± 5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ± 5% resistor	NC

3D3V_S0
SIO_EXT_SMI# 1 R403 2
10KR2J-3-GP

Add RTC Gen 9 reset circuit_20170814
leakage issue

3D3V_S5_PCH
R406 10KR2J-3-GP
RTC_RST
3D3V_S5_PCH
R405 10KR2J-3-GP
RTC_RST
RO13_20171011
Q401
CPU_DP_HPD_P
DP1_HPD_CPU_R
DP1_HPD_CPU
RTC_RST
common part
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C

RTC Gen 9 reset circuit_20170814
DP1_HPD_CPU_R
R404 1 2 Do Not Stuff
DP1_HPD_CPU
NON_RTC_RST
R403
100KR2J-1-GP

DP for Type-C Mux

BV UMA TC TPM

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDI/EDP/TBT/TPC/)

Size	Document Number	Rev
A2	Bucky WHL	SA

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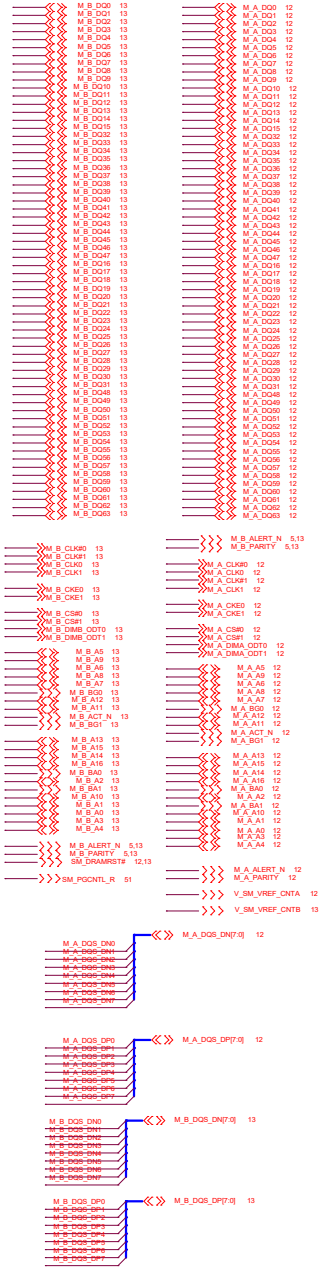
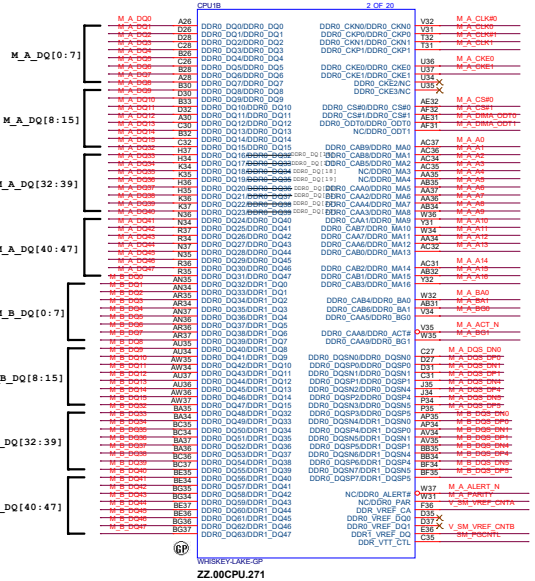
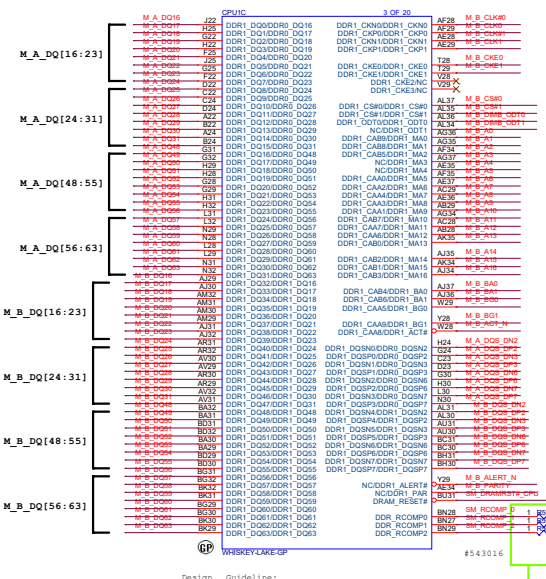
Main Func = CPU

DDR4 ball type: NON-Interleaved Type



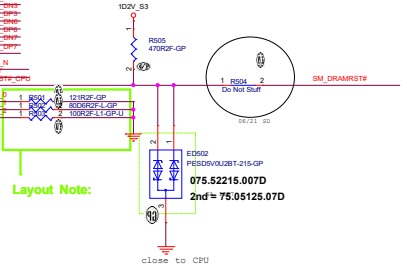


ZZ.00CPU.271



#543016

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.



Layout Note:

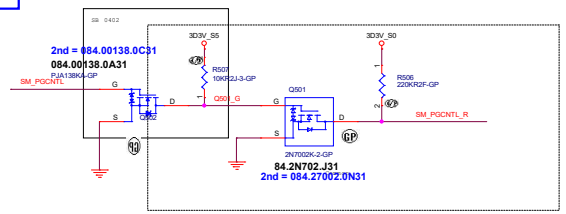
DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

PDG: DDR/ODT

ODT Signals Connectivity Table

Processor	Memory type	Side	Signal	Rule
WHL-U	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.
		DRAMs	ODT[1:0]	
	DDR4 SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.
		DIMMs	ODT[1:0]	

1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.



BV UMA TC TPM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(DDR)

Size: Custom | Document Number: Bucky WHL | Rev: SA

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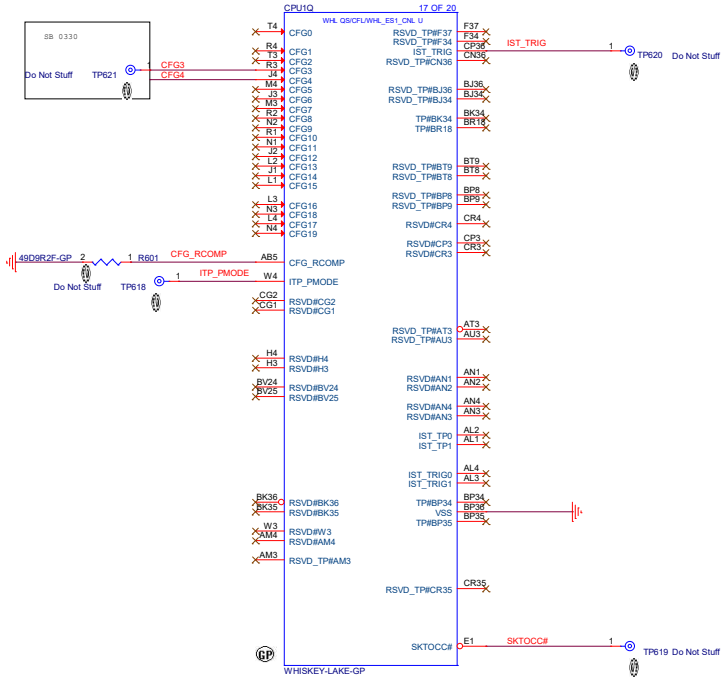
SSID = CPU

15 CFG3

15 CFG4



SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

BV UMA TC TPM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CFG/IST)

Size	Document Number	Rev
A2	Bucky WHL	SA

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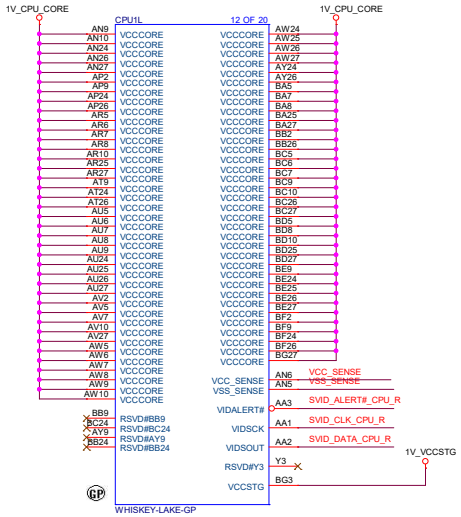
SSID = CPU

46 VCC_SENSE
46 VSS_SENSE

46 SVID_DATA_CPU
46 SVID_CLK_CPU
46 SVID_ALERT#_CPU

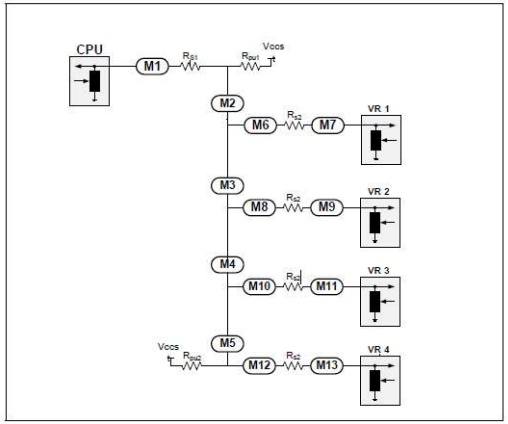


Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS		76	76	2992.13	2992.13

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381	432	15000	17007.9
M3	MS/SL/DSL	VSS		102		4015.75	
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11

Topology Guidelines	
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock
Length Matching Rules	
Length Matching between VIDSOUT and VIDSCK	± 100mils

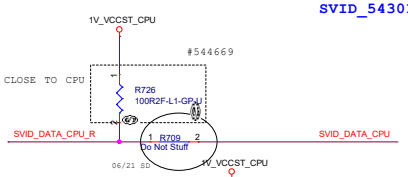
. Routing Illustration for SVID Topology



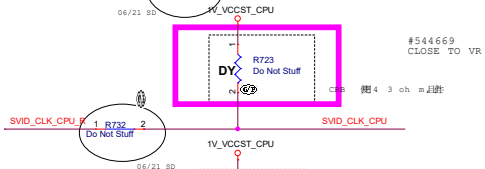
Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID_543016:

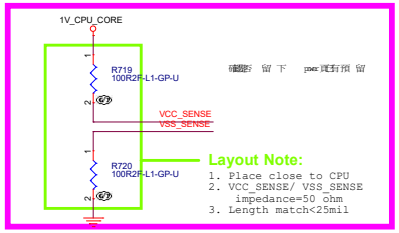
SVID DATA



SVID CLOCK



SVID ALERT



BV UMA TC TPM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCCIN/VID)

Size: A2 | Document Number: Bucky WHL | Rev: SA

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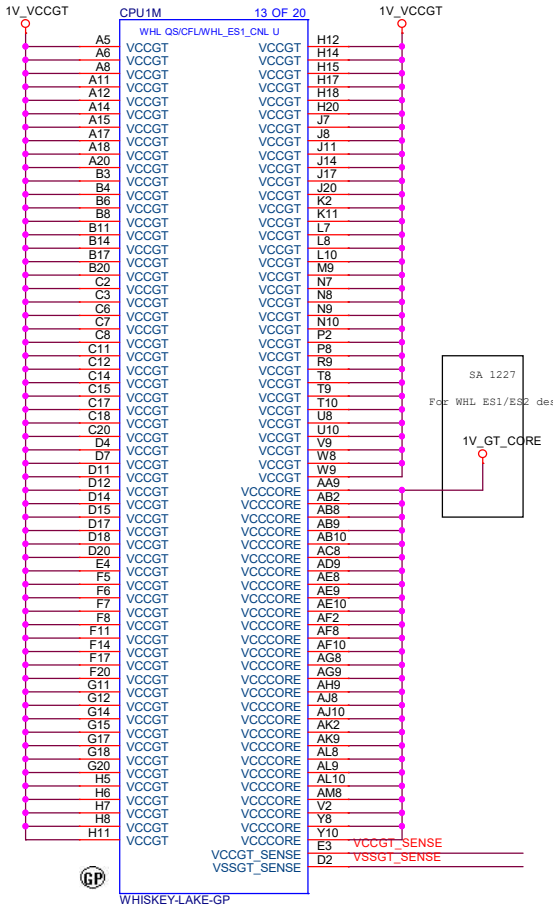
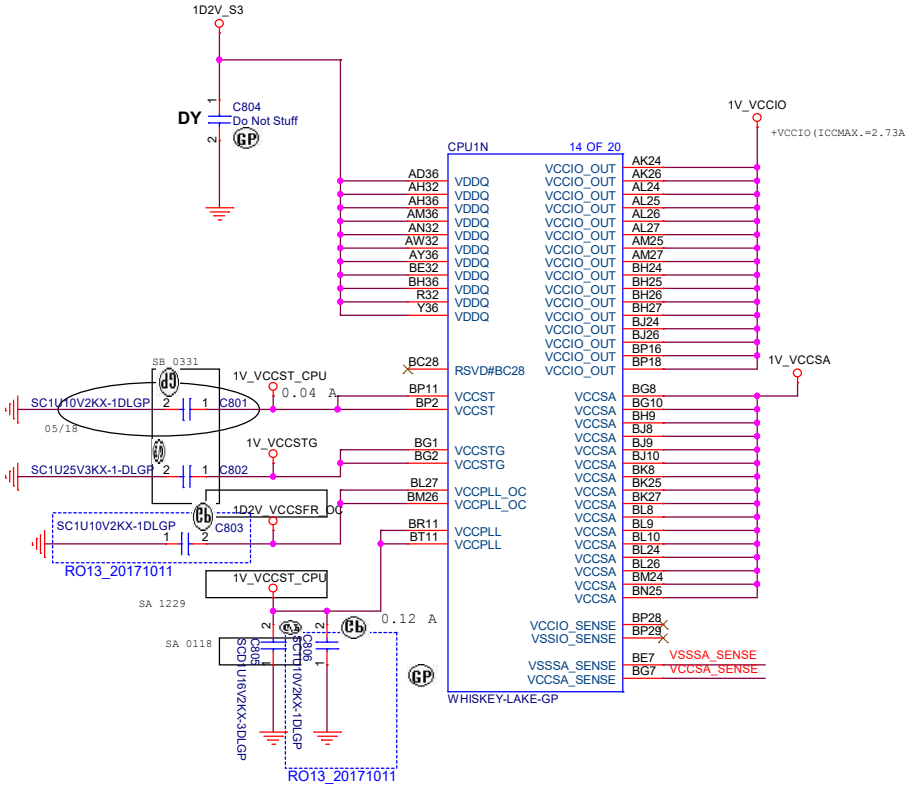
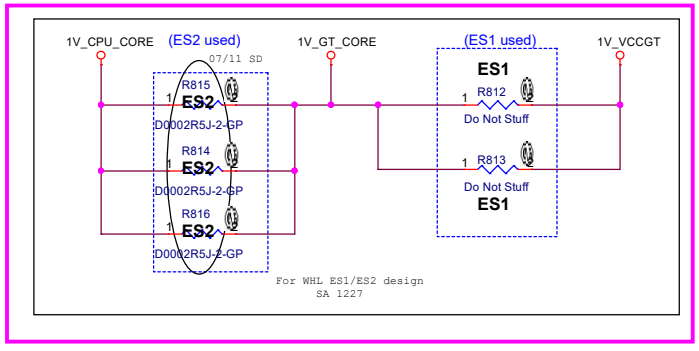
46 VSSSA_SENSE
46 VCCSA_SENSE

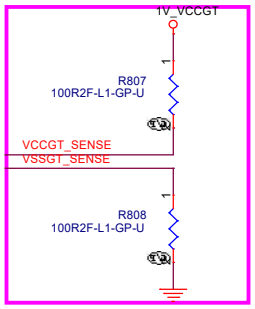
46 VCCGT_SENSE
46 VSSGT_SENSE

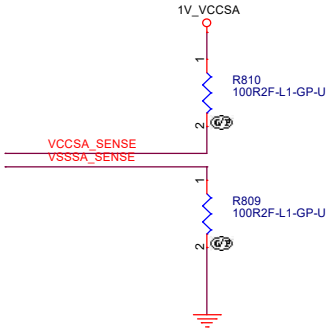
Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE











確認影 留下 per 更有預 留

BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VDDQ/VCC/VCCST/VCCSTG)

Size	Document Number	Rev
A3	Bucky WHL	SA

Date: Friday, July 13, 2018 Sheet 8 of 105

Main Func = CPU

(Blanking)

BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RSVD)

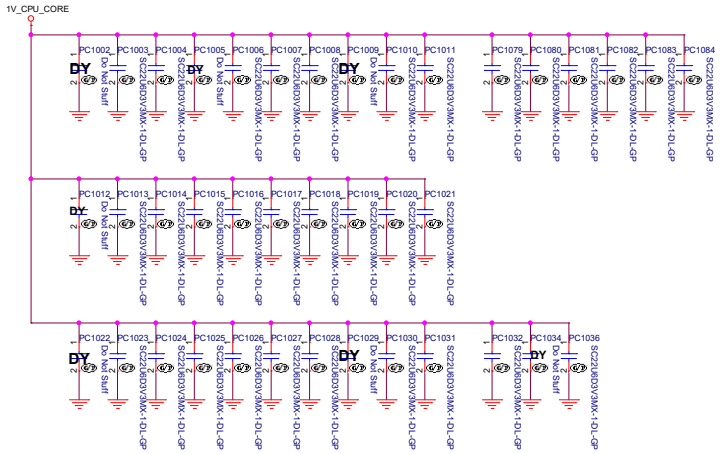
Size: A3 | Document Number: Bucky WHL | Rev: SA

Date: Friday, July 13, 2018 | Sheet 9 of 105

SSID = CPU

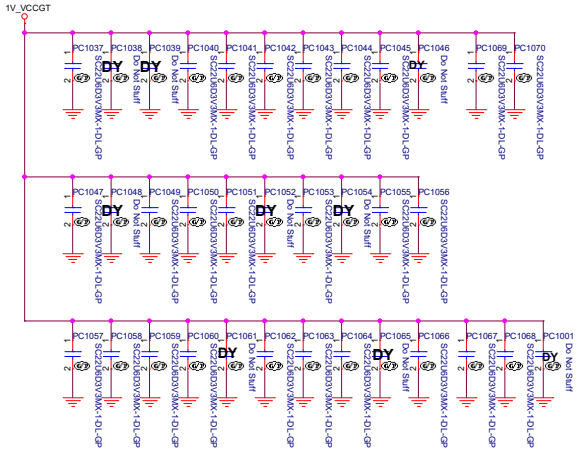
1V_CPU_CORE

22U 0603 x 39 (3DY)



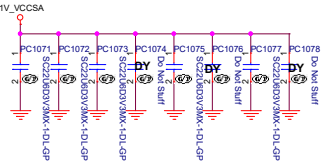
VCCGT

22U 0603 x 35 (3 DY)



VCCSA

22U 0603 x 8 (3DY)



Whiskey Lake U 4+2 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
Vcc_{CORE} Power Plane at VR output	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
Vcc_{GT} Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
Vcc_{CORE}		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
Vcc_{GT}	15x 22uF 0603		Place underneath the package
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	
Vcc_{SA}		*4x 0402*	*Placeholder only.*
		7x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
	2x 0805		*Placeholder Only*
V_{DDQ}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
Vcc_{IO}	4x 1uF 0201		Place underneath the package
	6x 10uF 0402		Place as close to the package as possible
	4x 0402		*Placeholder Only*
Vcc_{PLL_OC}	1x 1uF 0402		Do not merge Vcc_{PLL}, Vcc_{PLL_OC} and Vcc_{GT} to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
Vcc_{PLL}	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		*Placeholder Only.* Can be placed on as either Primary or back side cap.
Vcc_{ST}	1x 1uF 0402		
Vcc_{STG}	1x 1uF 0402		

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ' 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps >Power source.

BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

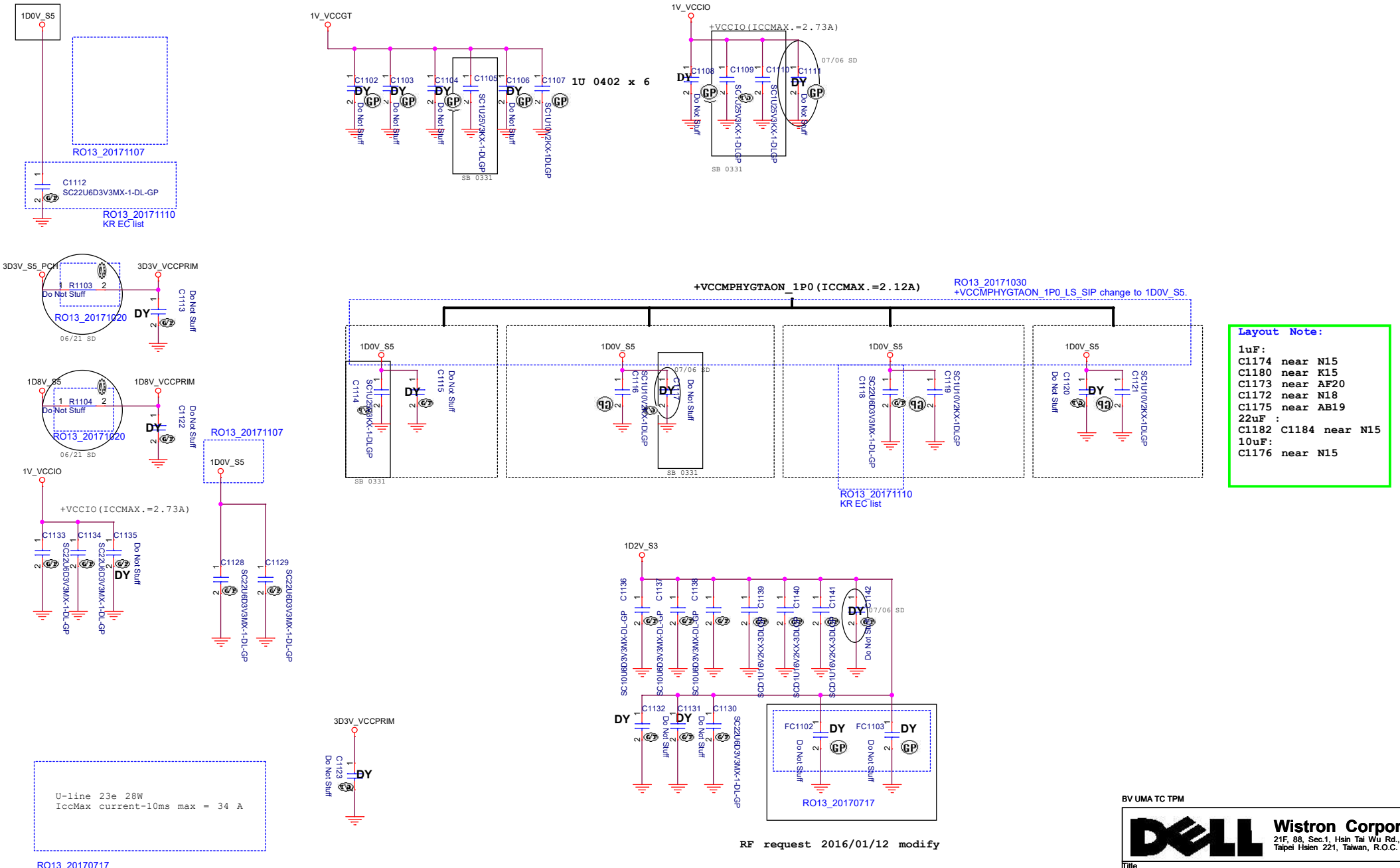
Title: CPU(CORE Power Cap1)

Size: A2 | Document Number: Bucky WHL | Rev: SA

Date: Friday, July 13, 2018 | Sheet 10 of 105

SSID = CPU

PCH DERIVED RAILS UNSLICED GT VCCIO



BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(Power CAP2)

Size	Document Number	Rev
A3	Bucky WHL	SA

Date: Friday, July 13, 2018 Sheet 11 of 105

Main Func = DDR4 SODIMM

DDR_DATA

M_A_A0 5
M_A_A1 5
M_A_A2 5
M_A_A3 5
M_A_A4 5
M_A_A5 5
M_A_A6 5
M_A_A7 5
M_A_A8 5
M_A_A9 5
M_A_A10 5
M_A_A11 5
M_A_A12 5
M_A_A13 5
M_A_A14 5
M_A_A15 5
M_A_A16 5

M_A_DQ0 5
M_A_DQ1 5
M_A_DQ2 5
M_A_DQ3 5
M_A_DQ4 5
M_A_DQ5 5
M_A_DQ6 5
M_A_DQ7 5
M_A_DQ8 5
M_A_DQ9 5
M_A_DQ10 5
M_A_DQ11 5
M_A_DQ12 5
M_A_DQ13 5
M_A_DQ14 5
M_A_DQ15 5
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M_A_DQ34 5
M_A_DQ35 5
M_A_DQ36 5
M_A_DQ37 5
M_A_DQ38 5
M_A_DQ39 5
M_A_DQ40 5
M_A_DQ41 5
M_A_DQ42 5
M_A_DQ43 5
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M_A_DQ45 5
M_A_DQ46 5
M_A_DQ47 5
M_A_DQ16 5
M_A_DQ17 5
M_A_DQ18 5
M_A_DQ19 5
M_A_DQ20 5
M_A_DQ21 5
M_A_DQ22 5
M_A_DQ23 5
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M_A_DQ25 5
M_A_DQ26 5
M_A_DQ27 5
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M_A_DQ30 5
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M_A_DQ52 5
M_A_DQ53 5
M_A_DQ54 5
M_A_DQ55 5
M_A_DQ56 5
M_A_DQ57 5
M_A_DQ58 5
M_A_DQ59 5
M_A_DQ60 5
M_A_DQ61 5
M_A_DQ62 5
M_A_DQ63 5

5 M_A_DQS_DN[7:0]
5 M_A_DQS_DP[7:0]

DDR CMD/ADD

5 M_A_ACT_N
5 M_A_ALERT_N
5 M_A_PARITY

5 V_SM_VREF_CNTA

5 M_A_BA0
5 M_A_BA1
5 M_A_BG0
5 M_A_BG1

DDR CTRL

5 M_A_CS#0
5 M_A_CS#1

5 M_A_CKE0
5 M_A_CKE1

5 M_A_DIMA_ODT0
5 M_A_DIMA_ODT1

DDR CLOCK

5 M_A_CLK0
5 M_A_CLK#0

5 M_A_CLK1
5 M_A_CLK#1

DDR_OTHERS

5,12,13 SM_DRAMRST# Edison 11/13 for STU
13,18,65 PCH_SMBDATA
13,18,65 PCH_SMBCLK
5,12,13 SM_DRAMRST# Edison 11/13 for STU

DM1A 1 OF 4
DDR4-260P-79-GP-U
062.10011.M003

DM1B 2 OF 4
SA 1225 SWAP
DDR4-260P-79-GP-U

DM1C 3 OF 4
DDR4-260P-79-GP-U

DM1D 4 OF 4
DDR4-260P-79-GP-U

DDR4 SWAP 0212

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R1215 DY Do Not Stuff
C1229 SCD025V2KX-1DLGP
20171011 Follow KR15.

RN1201 SRN1KJ-7-GP
R1206 2R2F-GP
C1222 SCD022U16V2KX-3DLGP
+V_VREF_PATH1
R1209 24D9R2F-L-GP

R1204 R1205 R1210 R1212 DY Do Not Stuff
DIMM1_SA0
DIMM1_SA1
DIMM1_SA2

05/10 SC
SM_DRAMRST#
ED1217 Do Not Stuff
Layout note: closed to Dimm

C1226 C1233 C1225 C1230 C1224 C1227
C1202 C1203 C1204 C1205 C1206 C1208 C1209 C1210
C1214 C1215 C1216 C1217 C1218 C1219 C1220 C1221 EC1201 EC1202
C1211 C1231 C1232 C1212 C1207 C1213

BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-CHA)
Size: A2
Document Number: Bucky WHL
Rev: SA
Date: Friday, July 13, 2018
Sheet 12 of 105

Main Func = DDR4 SODIMM

DDR_DATA

M_B_A0 5
M_B_A1 5
M_B_A2 5
M_B_A3 5
M_B_A4 5
M_B_A5 5
M_B_A6 5
M_B_A7 5
M_B_A8 5
M_B_A9 5
M_B_A10 5
M_B_A11 5

M_B_A12 5
M_B_A13 5
M_B_A14 5
M_B_A15 5
M_B_A16 5

M_B_DQ0 5
M_B_DQ1 5
M_B_DQ2 5
M_B_DQ3 5
M_B_DQ4 5
M_B_DQ5 5
M_B_DQ6 5
M_B_DQ7 5
M_B_DQ8 5
M_B_DQ9 5
M_B_DQ10 5
M_B_DQ11 5
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M_B_DQ15 5
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M_B_DQ59 5
M_B_DQ60 5
M_B_DQ61 5
M_B_DQ62 5
M_B_DQ63 5

5 M_B_DQS_DN[7:0]
5 M_B_DQS_DP[7:0]

DDR CMD/ADD

5 M_B_ACT_N
5 M_B_ALERT_N
5 M_B_PARITY

5 V_SM_VREF_CNTB

5 M_B_BA0
5 M_B_BA1
5 M_B_BG0
5 M_B_BG1

DDR CTRL

5 M_B_CS#0
5 M_B_CS#1

5 M_B_CKE0
5 M_B_CKE1

5 M_B_DIMB_ODT0
5 M_B_DIMB_ODT1

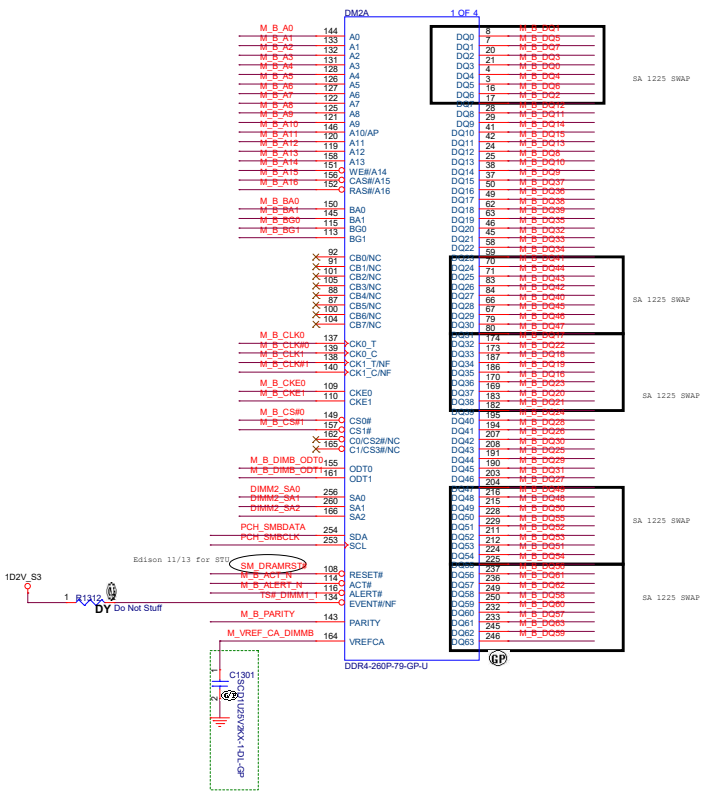
DDR CLOCK

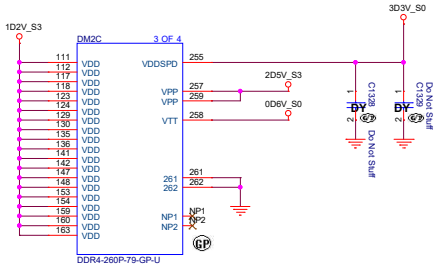
5 M_B_CLK0
5 M_B_CLK#0

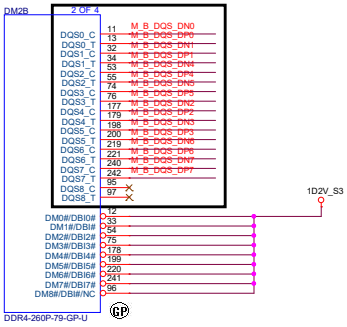
5 M_B_CLK1
5 M_B_CLK#1

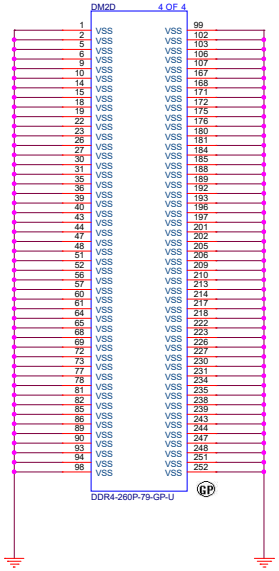
DDR OTHERS

5,12,13 SM_DRAMRST#
12,18,65 PCH_SMBDATA
12,18,65 PCH_SMBCLK
5,12,13 SM_DRAMRST#









DDR4 SWAP 0212
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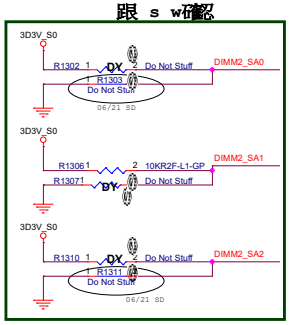

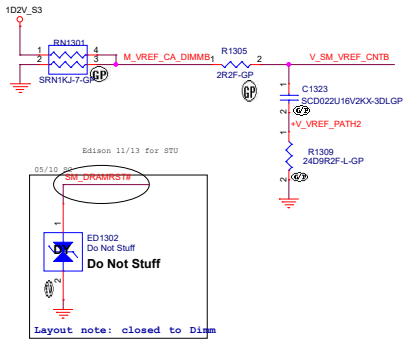

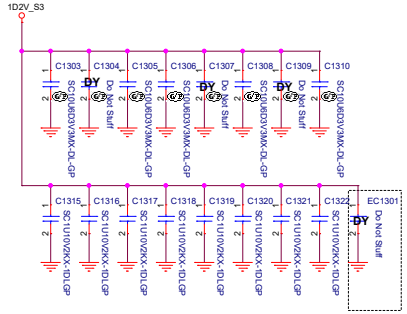

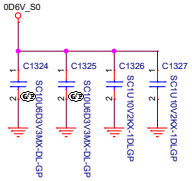

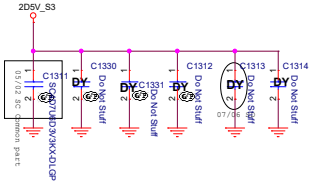

BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-CHB)
Size: A2
Document Number: Bucky WHL
Rev: SA
Date: Friday, July 13, 2018
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(Blanking)

BV UMA TC TPM

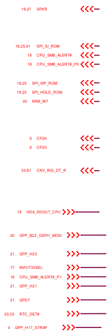
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
DDR (RSVD) (DDR4-CHA1)

Size	Document Number	Rev
A4	Bucky WHL	SA

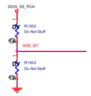
Date: Friday, July 13, 2018 Sheet 14 of 105

Main Func = PCH

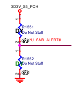


GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.

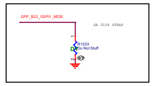
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.



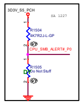
GPP_C2 / SMBALERT#	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.



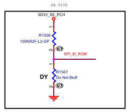
GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). **Bit 6** – **Boot BIOS Destination** 0 – SPI (Default) 1 – LPC ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.



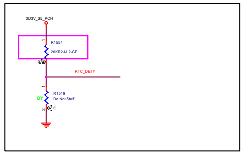
GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the *eSPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**



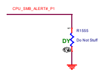
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



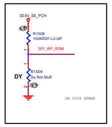
GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



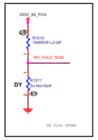
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.



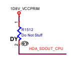
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

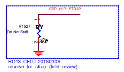


GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

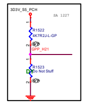
GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

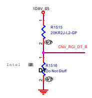
GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.



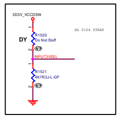
GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.



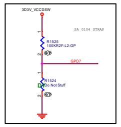
GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.



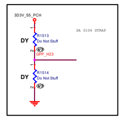
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% ***Note:*** This strap should only be used for specific targeted 1S battery systems.



GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

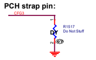


GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**



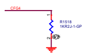
[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

PCH strap pin:



(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.



BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)		
Size: A0	Document Number: Bucky WHL	Rev: SA
Date: Friday, July 13, 2018	Sheet 15 of 105	

Main Func = PCH

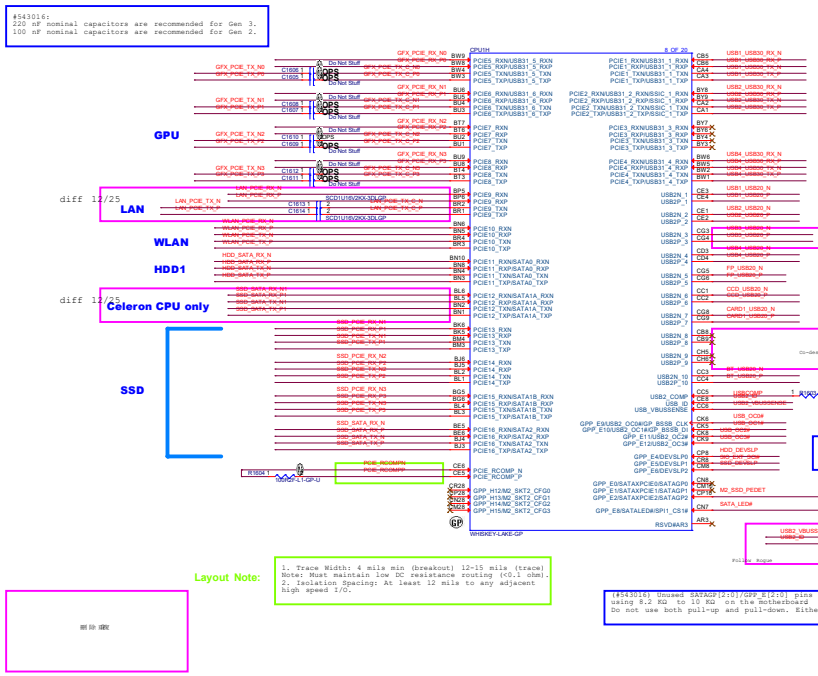
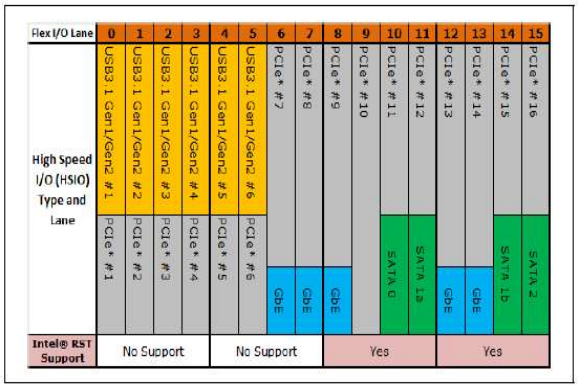


Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3				PCIe* Controller #4			
										Cycle Router #2				Cycle Router #3			
Flex I/O Lane		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	1x4	RP1				RP5				RP9				RP13			
	1x4 LR	RP1				RP5				RP9				RP13			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16
	2x1+1x2	RP4	RP3		RP1	RP6	RP7		RP5	RP12	RP11		RP9	RP16	RP15		RP13
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

CPU (PCIE/SATA/USB)

Size: A1 | Document Number: Bucky WHL | Rev: SA

Date: Friday, July 13, 2018 | Sheet 18 of 155

SSID = PCH

24 SYS_PWROK
24,26,40 RESET_OUT#
24,40 VCCST_PWRGD
24 PCH_RSMRST#
17,25,40,45 3V_5V_POK
24,40,68,91 PM_SLP_S0#
27,40,68 PM_SLP_S3#
40,51,66,68 PM_SLP_S4#
24,61 AUX_EN_WOWL
24 SIO_PWRBTN#
43,44 ACOK_IN_M
3 H_CPUPWRGD
24 LAN_WAKE#
17,25,40,45 3V_5V_POK
68 SIO_SLP_A#
68 XDP_DBRESET#
26,61,63,66,76,91 PLT_RST#
68 PM_SLP_S5#
15 INPUT3VSEL

RO13_20170822
remove 3D3V_S5 short +VCCPDSW_3P3 (R1711)
U2502 instead it.

RTC_RST
NON_RTC_RST
PCH_BATLOW#

#544669 (CRB): 330k.

#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.

RO13_20171001
move ED1702 TVS to dual TVS ED401

AOZ Power switch, P/N: 074.01334.0093
Low Rds(on)= 5m Ohm
Turn on rise time = 10us

remove R1724 R1735 C1704 EC1710 and
+VCCMPHYGTAON_1P0_LS_SIP change to 1D0V_S5.
RO13_20171030

Dis-wire with XDP_PM_RSMRST_PWRGD_XDP

R1722 & EC1708 modify to 100k and 0.01uF at DVT1

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

RO13_20171011
B3.R2003.A8M
2ND = 083.52030.008F
common part
2nd = 075.27002.F7C
Reserve by NON DS3 function 20150413
RO13_20170921
remove R1720 short pad

2017/03/09

Dummy C1710 by it's useless

EC1711 modify to 100k and 0.01uF at DVT1 20150203

External Pull-up requirement for SLP_S0# and EXT_PWR_GATE# signal pins

SLP_S0# and EXT_PWR_GATE# signal pins require External Pull-up and the details are given below:

Signal Name	Pull-up Resistor Value		Note
	3.3V Signaling Mode	1.8V Signaling Mode	
EXT_PWR_GATE#	100K	75K	Pull-up resistor is required
SLP_S0#	100K	75K	Pull-up resistor is required if a device is monitoring SLP_S0# before RSMRST# de- assertion

BATLOW#:
Pull-up required even if not implemented.

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

8V UMA TC TPM

PCH_(PMU)

Size: A1 | Document Number: Bucky WHL | Rev: SA

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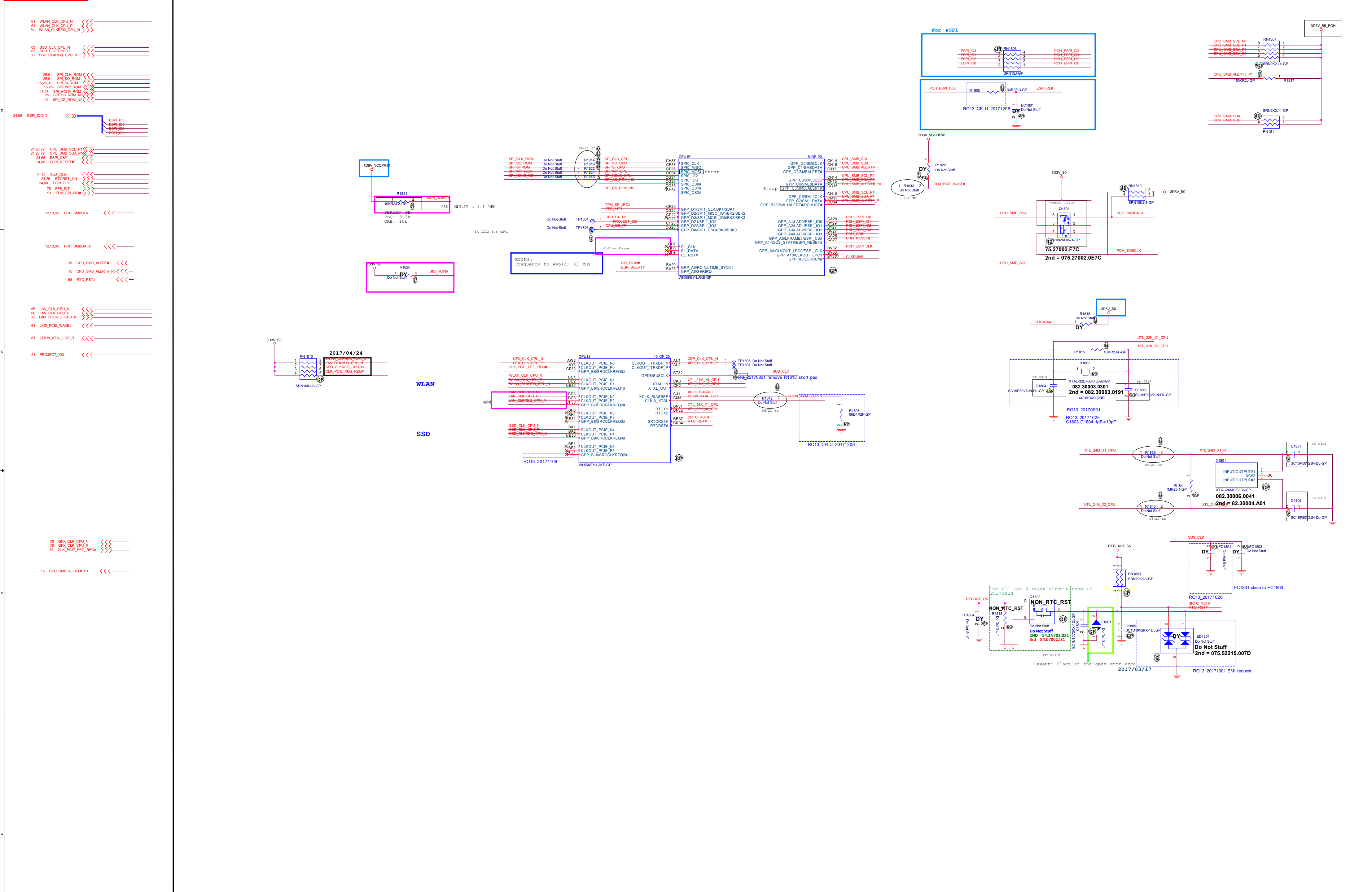
SSID = PCH



BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SPI/ESPI/SMBS/XTAL/CLK)

Size A1 | Document Number: Bucky WHL | Rev SA

Date: Friday, July 13, 2018 | Sheet 18 of 105

SSID = PCH

15,27 SPKR
27 HDA_SDIN0_CPU
27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
98 ME_FWP_SW
27 HDA_SDOUT_CODEC
65 KB_LED_BL_DET

24 GC6_THM_DIS#
15 HDA_SDOUT_CPU

55 DMIC_PCH_CLK
55 DMIC_PCH_DATA

24,85 DGPU_PWROK

61 BT_PCMFRM_CRF_RST_N
61 BT_PCMOUT_CLKREQ0

CPU1G 7 OF 20
WHISKEY-LAKE-GP

HDA_SYNC_CPU BN34 HDA_SYNC/I2S0_SFRM
HDA_BITCLK_CPU BN37 HDA_BCLK/I2S0_SCLK
HDA_SDOUT_CPU BN36 HDA_SDO/I2S0_TXD
HDA_SDIN0_CPU BN35 HDA_SDI0/I2S0_RXD
BL36 HDA_SDI1/I2S1_RXD/SNDW1_DATA
HDA_RST_N_CPU BL35 HDA_RST#/I2S1_SCLK/SNDW1_CLK
CK23 GPP_D23/I2S_MCLK
BL37 I2S1_SFRM/SNDW2_CLK
BL34 I2S1_TXD/SNDW2_DATA

Do Not Stuff TP1903

BT_PCMFRM_CRF_RST_N_1 R1923 33R2J-2-GP BT_PCMFRM_CRF_RST_N_R
BT_PCMOUT_CLKREQ0_1 R1922 33R2J-2-GP BT_PCMOUT_CLKREQ0_R
CJ32 GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#
CH32 GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK
CH29 GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ
CH30 GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO

DMIC_PCH_CLK CP24 GPP_D19/DMIC_CLK0/SNDW4_CLK
DMIC_PCH_DATA CN24 GPP_D20/DMIC_DATA0/SNDW4_DATA
PWM_LC CK25 GPP_D17/DMIC_CLK1/SNDW3_CLK
DGPU_PWROK CJ25 GPP_D18/DMIC_DATA1/SNDW3_DATA
SPKR CF35 GPP_B14/SPKR

GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
GPP_A16/SD_1P8_SEL
SD_1P8_RCOMP
SD_3P3_RCOMP

GPP_G0/SD_CMD CH36 GC6_THM_DIS#
GPP_G1/SD_DATA0 CL38
GPP_G2/SD_DATA1 CL36
GPP_G3/SD_DATA2 CM35
GPP_G4/SD_DATA3 CN33
GPP_G5/SD_CD# CH35 KB_LED_BL_DET
GPP_G6/SD_CLK CK36
GPP_G7/SD_WP CK34

BW36 SENSOR_DB_DET#
BY31
CK33 SD_RCOMP
CM34
R1901 1 2 200R2F-L-GP

RO13_CFLU_20171207

3D3V_S5
R1910 Not Stuff
fwTPM
TPM_ID
R1911 10KR2J-3-GP
TPM

diff 12/25 Bucky DMIC I2C from Codec TC

3D3V_S5
R1913 10KR2J-3-GP
CLAM
SENSOR_DB_DET#
R1912 Do Not Stuff
2IN1
CHECK

EC1901 DY
HDA_BITCLK_CODEC
Do Not Stuff

HDA_SYNC_CODEC
R1908 Do Not Stuff
HDA_SYNC_CPU
07/06 SD

RO13_20171027
delete ED1901

R1920~R1921 need to close for merge prepare
HDA_BITCLK_CODEC
HDA_SDOUT_CODEC
R1920 1
R1921 1
0R2J-1-GP
33R2J-2-GP
HDA_BITCLK_CPU
HDA_SDOUT_CPU
ME_FWP_SW
R1909 1 1KR2J-1-GP

R1907,R1912 merge to RN1902
2015/10/06 modify

HDA_SDOUT_CODEC
EC1903 DY
Do Not Stuff

BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HAD/I2S/SD/DMIC)
Size: A2
Document Number: Bucky WHL
Rev: SA
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SSID = PCH

79,86 GC6_FB_EN
55 CPU_I2C_SDA_P1
55 CPU_I2C_SCL_P1
65 CPU_I2C_SDA_P0
65 CPU_I2C_SCL_P0
55 DBC_PANEL_EN

68 UART_2_CRXD_DTXD
68 UART_2_CTXD_DRXD
24 SIO_EXT_WAKE#
65 KB_DET#

66 GSEN_INT1
66 GSEN_INT2
70 GSEN2_INT1_C
70 GSEN2_INT2_C
70 GYRO_INT_C
66 GYRO_DRDY
15,25 RTC_DET#
66,70 SENSOR_I2C_SDA
66,70 SENSOR_I2C_SCL
70 FFS_INT2

91 PIRQA#

21 BOARD_ID2

61 CNV_BRI_RSP
15,61 CNV_RGI_DT_R
61 CNV_BRI_DT_R
61 CNV_RGI_RSP

76 DGPU_HOLD_RST#
79 GPU_EVENT#
86 DGPU_PWR_EN
15 NRB_BIT
15 GPP_B22_GSPI1_MOSI

EC2002 DY DGPU_HOLD_RST#
Do Not Stuff
RN2009 OPS DGPU_HOLD_RST#
DGPU_PWR_EN
Do Not Stuff

1D8V_VCCPRM
R2053 DY Do Not Stuff PIRQA#

3D3V_S0
Do Not Stuff R2048 UART_2_CRXD_DTXD
Do Not Stuff R2049 UART_2_CTXD_DRXD
DEBUG
DEBUG

Do Not Stuff DY R2043 DBC_PANEL_EN
10KR2J-3-GP R2044 FFS_INT2
10KR2J-3-GP R2045 KB_DET#
10KR2J-3-GP R2046 IR_CAM_DET#
Do Not Stuff DY R2011 DGPU_PWR_EN

3D3V_S5_PCH
10KR2J-3-GP R2041 SIO_EXT_WAKE#

1D8V_S5
SB 0404
R2029 20KR2J-L2-GP CNV_RGI_RSP
R2030 20KR2J-L2-GP CNV_BRI_RSP

2016/11/07 modify

3D3V_S0
UMA
R2038 10KR2J-3-GP
VRAM_ID2
R2037 Do Not Stuff
OPS

	H(10K)	L(10K)
VRAM_ID2	UMA	OPS
BOARD_ID2	2IN1	CLAM
BOARD_ID1	CNL	WHL-U
NB_MODE#	2IN1	CLAM

3D3V_S0
2IN1
R2005 Do Not Stuff
BOARD_ID2
R2008 10KR2J-3-GP
CLAM

3D3V_S0
CNL
R2010 Do Not Stuff
BOARD_ID1
R2009 10KR2J-3-GP
WHL-U

GPU_EVENT# R2003 OPS Do Not Stuff
GC6_FB_EN R2004 OPS Do Not Stuff

SA 1212 For CNVi
diff 12/25

CNV_RGI_DT_R R2006 1 5R2J-1-GP
CNV_BRI_DT_R R2007 1 5R2J-1-GP

TPAD
Touch panel

CPU1F 6 OF 20
WHISKEY-LAKE-GP

GPU_EVENT_MCP#	CC27	GPP_B15/GSPI0_CS0#
PIRQA#	CC32	GPP_A7/PIRQA#/GSPI0_CS1#
GC6_FB_EN_MCP	CE28	GPP_B16/GSPI0_CLK
	CE27	GPP_B17/GSPI0_MISO
NRB_BIT	CE29	GPP_B18/GSPI0_MOSI
DBC_PANEL_EN	CA31	GPP_B19/GSPI1_CS0#
	CA32	GPP_A11/PME#/GSPI1_CS1#/SD_VDD2_PWR_EN#
	CC29	GPP_B20/GSPI1_CLK
GPP_B22_GSPI1_MOSI	CC30	GPP_B21/GSPI1_MISO
	CA30	GPP_B22/GSPI1_MOSI
CNV_BRI_RSP	CJ20	GPP_F5/CNV_BRI_RSP
CNV_RGI_DT	CG19	GPP_F6/CNV_RGI_DT
CNV_BRI_DT	CJ20	GPP_F4/CNV_BRI_DT
CNV_RGI_RSP	CH19	GPP_F7/CNV_RGI_RSP
UART_2_CRXD_DTXD	CR12	GPP_C20/UART2_RXD
UART_2_CTXD_DRXD	CP12	GPP_C21/UART2_TXD
SIO_EXT_WAKE#	CN12	GPP_C22/UART2_RTS#
KB_DET#	CM12	GPP_C23/UART2_CTS#
CPU_I2C_SDA_P0	CM11	GPP_C16/I2C0_SDA
CPU_I2C_SCL_P0	CN11	GPP_C17/I2C0_SCL
CPU_I2C_SDA_P1	CK12	GPP_C18/I2C1_SDA
CPU_I2C_SCL_P1	CJ12	GPP_C19/I2C1_SCL
	CF27	GPP_H4/I2C2_SDA
	EF29	GPP_H5/I2C2_SCL
	CH27	GPP_H6/I2C3_SDA
	EH28	GPP_H7/I2C3_SCL
	CJ30	GPP_H8/I2C4_SDA
	EJ31	GPP_H9/I2C4_SCL

Strap

CN22	DGPU_HOLD_RST#	GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
CR22	IR_CAM_DET#	GPP_D10/ISH_SPI_CLK/GSPI2_CLK
CP22	RTC_DET#	GPP_D11/ISH_SPI_MISO/GSPI2_MISO
		GPP_D12/ISH_SPI_MOSI/GSPI2_MOSI
CK22	CPU_I2C_SDA_ISH0	GPP_D5/ISH_I2C0_SDA
CH20	CPU_I2C_SCL_ISH0	GPP_D6/ISH_I2C0_SCL
CH22	CPU_I2C_SDA_ISH1	GPP_D7/ISH_I2C1_SDA
CJ22	CPU_I2C_SCL_ISH1	GPP_D8/ISH_I2C1_SCL
CJ27		GPP_H10/I2C5_SDA/ISH_I2C2_SDA
CJ28		GPP_H11/I2C5_SCL/ISH_I2C2_SCL
CM24	DGPU_PWR_EN	
CN23	VRAM_ID2	GPP_D13/ISH_UART0_RXD
CR24		GPP_D14/ISH_UART0_TXD
		GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#
CG12	BOARD_ID1	GPP_D16/ISH_UART0_CTS#/SML0ALERT#
CH12	FFS_INT2	
CF12	UART1_RTS#	GPP_C12/UART1_RXD/ISH_UART1_RXD
CG14	UART1_CTS#	GPP_C13/UART1_TXD/ISH_UART1_TXD
		GPP_C14/UART1_RTS#/ISH_UART1_RTS#
		GPP_C15/UART1_CTS#/ISH_UART1_CTS#
BW35	ISH_KB_DISABLE	
BW34		GPP_A18/ISH_GP0
CA37		GPP_A19/ISH_GP1
CA36		GPP_A20/ISH_GP2
CA35		GPP_A21/ISH_GP3
CA34		GPP_A22/ISH_GP4
BW37		GPP_A23/ISH_GP5
		GPP_A12/ISH_GP6/BM_BUSY#/SX_EXIT_HOLDOFF#

CPU_I2C_SDA_ISH0 R2021 Do Not Stuff SENSOR_I2C_SDA
CPU_I2C_SCL_ISH0 R2020 Do Not Stuff SENSOR_I2C_SCL
06/21 SD

KBLK:GPP_F10~F11: 1.8V only
CFLU:GPP_H10~H11: 3.3V
記 GPIO 腳位 準 位 轉 換 電 路

remove TP2012 TP2014 TP2016 TP2017 and net. 20131031
TP2001 Do Not Stuff
TP2002 Do Not Stuff
R2013_20170921 remove R2023 R2024 short pad
R2025 1 Do Not Stuff GSEN_INT1
R2026 1 Do Not Stuff GSEN2_INT1_C
R2027 1 Do Not Stuff GYRO_INT_C
R2028 1 DY Do Not Stuff GYRO_DRDY
06/21 SD

3D3V_S0
RN2007 SRN1KJ-7-GP
CPU_I2C_SDA_ISH0
CPU_I2C_SCL_ISH0
RN2008 Do Not Stuff DY
CPU_I2C_SDA_ISH1
CPU_I2C_SCL_ISH1

(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

3D3V_S5
R2001 Do Not Stuff
2IN1
KB_DISABLE_CPU_R
Vth(max)=1.1V
2IN1
Q2001
ISH_KB_DISABLE
NB_MODE# 24
Do Not Stuff
Do Not Stuff
2nd = 075.27002.0E7C

3D3V_S5
R2050 Do Not Stuff
2IN1
NB_MODE#
R2002 10KR2J-3-GP
CLAM

1D8V_S0
R2052 Do Not Stuff DY
GYRO_DRDY_ISH
R2051 Do Not Stuff DY
2017/03/17

(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.

BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)
Size: A2
Document Number: Bucky WHL
Rev: SA
Date: Friday, July 13, 2018
Sheet 20 of 105

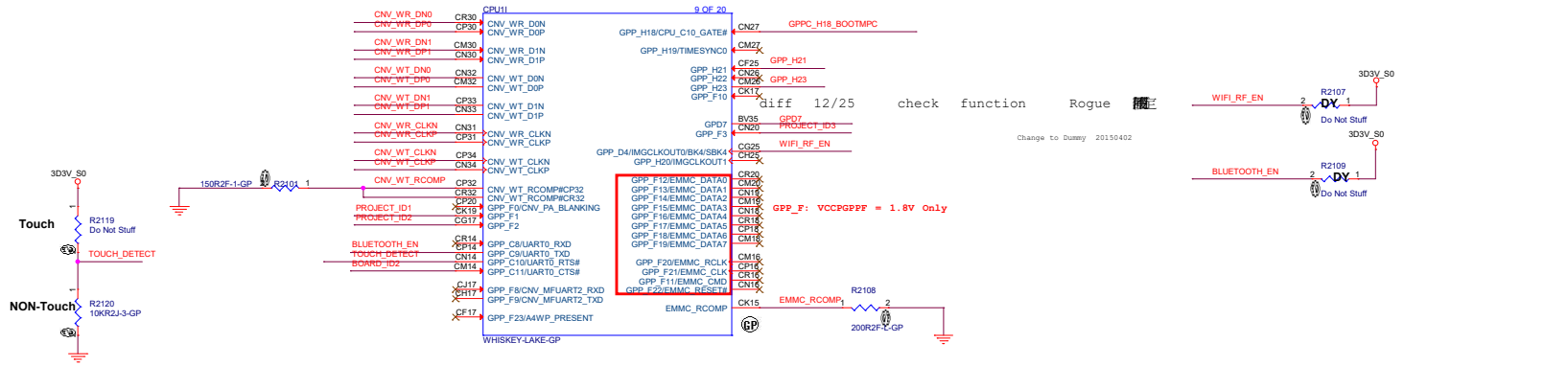
SSID = PCH

SSID = PCH

40 GPPC_H18_BOOTMPC
61 WIFI_RF_EN
61 BLUETOOTH_EN
20 BOARD_ID2
15 GPP_H23
15 GPP_H21

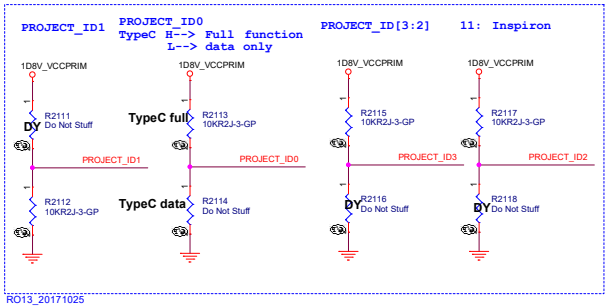
61 CNV_WT_CLKN
61 CNV_WT_CLKP
61 CNV_WT_DP0
61 CNV_WT_DN0
61 CNV_WT_DP1
61 CNV_WT_DN1
61 CNV_WR_CLKN
61 CNV_WR_CLKP
61 CNV_WR_DP0
61 CNV_WR_DN0
61 CNV_WR_DP1
61 CNV_WR_DN1

18 PROJECT_ID0
15 GPD7



diff 12/25 check function Rogue

Change to Dummy 20150402



RO13_20171025

	H(10K)	L(10K)	Note
PROJECT_ID0	TypeC full	TypeC data	TypeC function det
PROJECT_ID1	Non	Non	follow Rogue define
PROJECT_ID2	Non	Non	
PROJECT_ID3	Non	Non	

BV UMA TC TPM

Wistron Corporation
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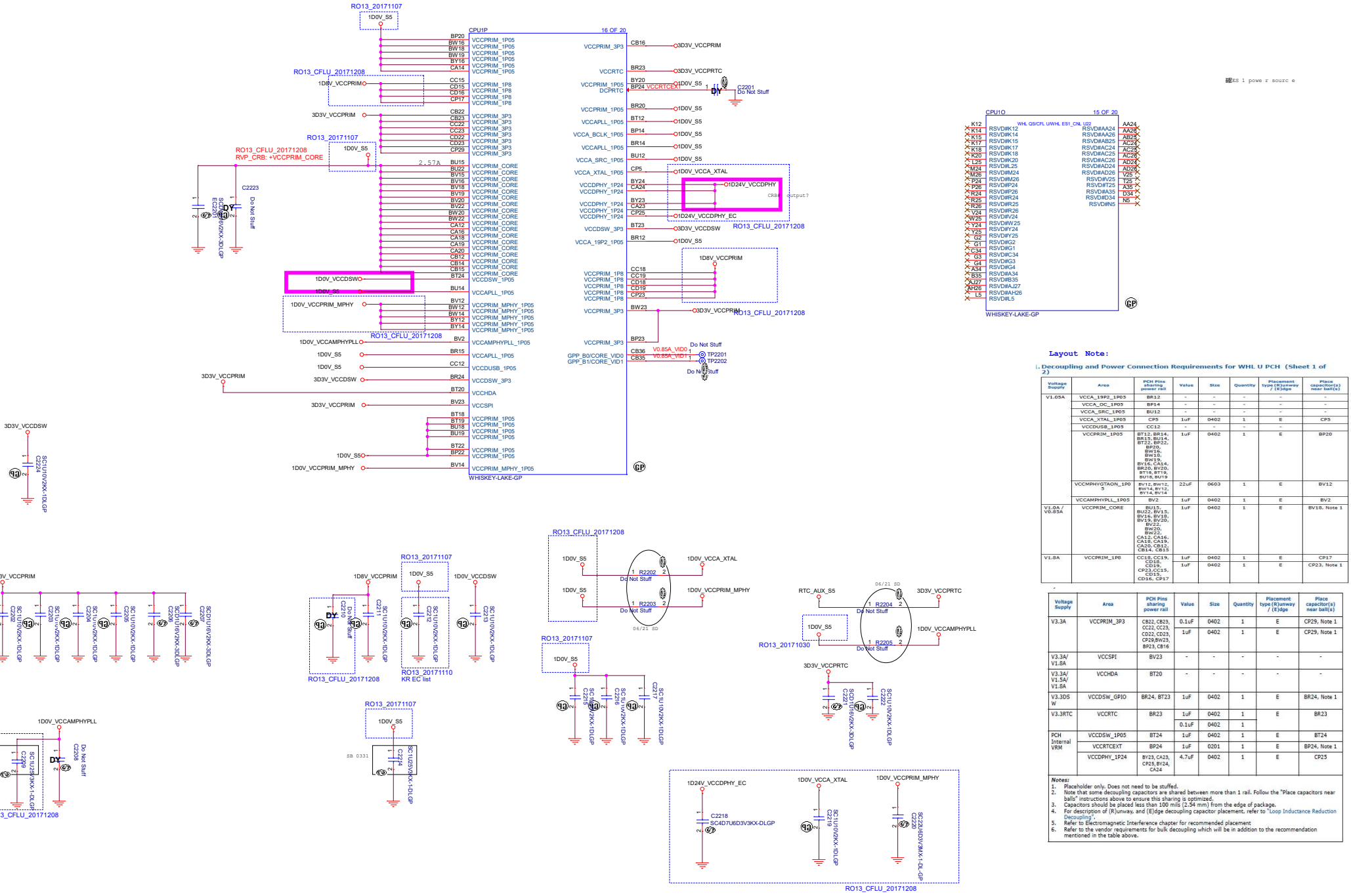
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CSI/EMMC/CNVi)

Size: A2 | Document Number: Bucky WHL | Rev: SA

Date: Friday, July 13, 2018 | Sheet 21 of 105

SSID = PCH



Layout Note:

1. Decoupling and Power Connection Requirements for WHL U PCH (Sheet 1 of 2)

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)unway / (E)dge	Place capacitor(s) near ball(s)
V1.05A	VCCA_19P2_1P05	BR12	-	-	-	-	-
	VCCA_DC_1P05	BP14	-	-	-	-	-
	VCCA_SRC_1P05	BU12	-	-	-	-	-
	VCCA_XTAL_1P05	CP5	1uF	0402	1	E	CP5
	VCCDUSB_1P05	CC12	-	-	-	-	-
	VCCPRIM_1P05	BT12, BR14, BR15, BU14, BT22, BP22, BP20, BW16, BW18, BW19, BV16, CA14, BR20, BV20, BT19, BT19, BU18, BU19	1uF	0402	1	E	BP20
	VCCMPHYGTAON_1P05	BV12, BW12, BW14, BV12, BV14, BV14	22uF	0603	1	E	BV12
	VCCAMPHYPLL_1P05	BV2	1uF	0402	1	E	BV2
V1.0A / V0.85A	VCCPRIM_CORE	BU15, BU22, BV15, BV16, BV18, BV19, BV20, BV22, BW20, BW22, CA12, CA16, CA18, CA19, CA20, CB12, CB14, CB15	1uF	0402	1	E	BV18, Note 1
V1.8A	VCCPRIM_1P8	CC18, CC19, CD18, CD19, CP23,CC15, CD19, CD16, CP17	1uF	0402	1	E	CP17
			1uF	0402	1	E	CP23, Note 1

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)unway / (E)dge	Place capacitor(s) near ball(s)
V3.3A	VCCPRIM_3P3	CB22, CB23, CC22, CC23, CD22, CD23, CP29,BW23, BP23, CB16	0.1uF	0402	1	E	CP29, Note 1
			1uF	0402	1	E	CP29, Note 1
V3.3A/ V1.8A	VCCSPI	BV23	-	-	-	-	-
V3.3A/ V1.5A/ V1.8A	VCCHDA	BT20	-	-	-	-	-
V3.3DSW	VCCDSW_GPIO	BR24, BT23	1uF	0402	1	E	BR24, Note 1
V3.3RTC	VCCRTC	BR23	1uF	0402	1	E	BR23
			0.1uF	0402	1		
PCH Internal VRM	VCCDSW_1P05	BT24	1uF	0402	1	E	BT24
	VCCRTCEXT	BP24	1uF	0201	1	E	BP24, Note 1
	VCCDPHY_1P24	BV23, CA23, CP25, BV24, CA24	4.7uF	0402	1	E	CP25

Notes:
1. Placeholder only. Does not need to be stuffed.
2. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
3. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
4. For description of (R)unway, and (E)dge decoupling capacitor placement, refer to "Loop Inductance Reduction Decoupling".
5. Refer to Electromagnetic Interference chapter for recommended placement
6. Refer to the vendor requirements for bulk decoupling which will be in addition to the recommendation mentioned in the table above.

BV UMA TC TPM

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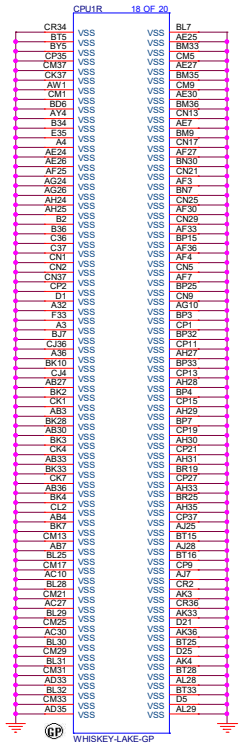
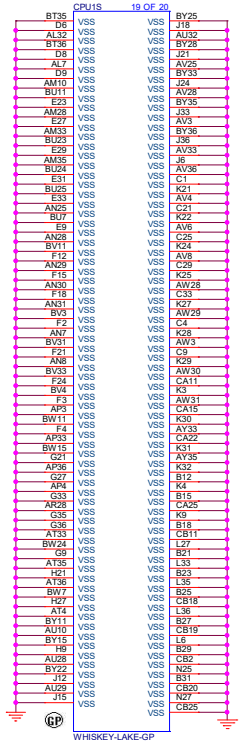
Title: CPU (PCH-LP PWR&Caps)

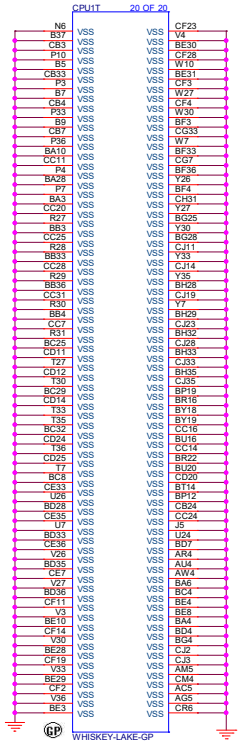
Size: A2 | Document Number: Bucky WHL | Rev: SA

Date: Friday, July 13, 2018 | Sheet 22 of 105

SSID = PCH







Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

BV UMA TC TPM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_(VSS)

Size: A2 | Document Number: Bucky WHL | Rev: SA

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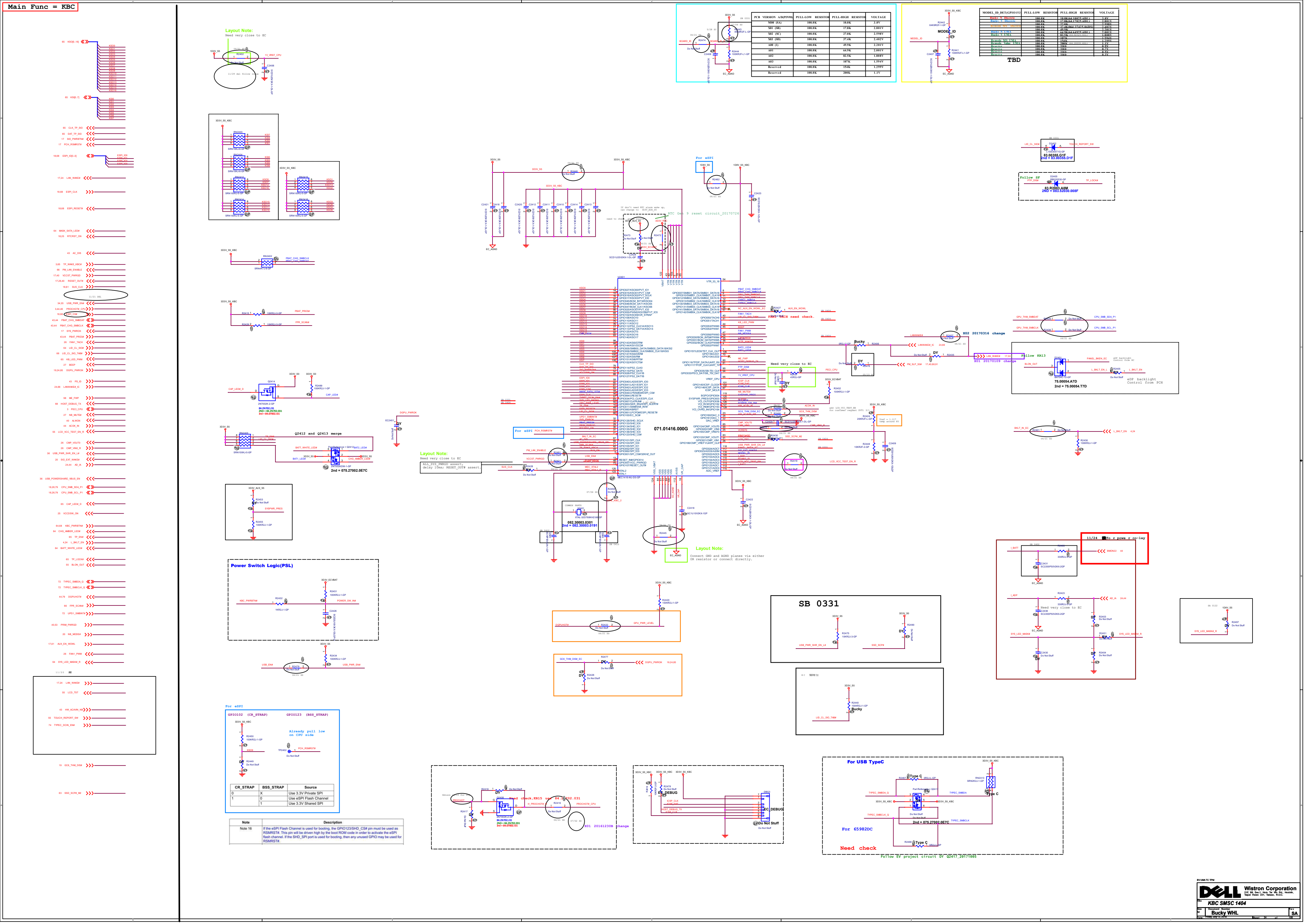
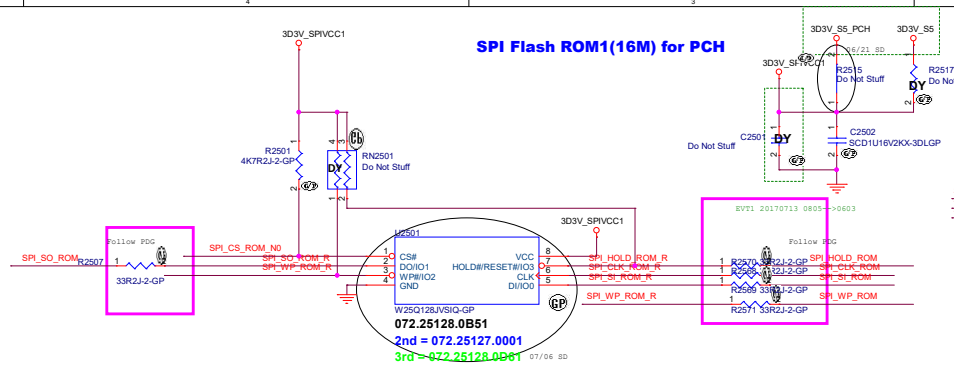


Main Func = KBC
Layout Note:
Need very close to EC
Power Switch Logic(PSL)
For eSPI
GPIO102 (CR_STRAP)
GPIO123 (BSS_STRAP)
Already pull low on CPU side
CR_STRAP
BSS_STRAP
Source
Use 3.3V Private SPI
Use eSPI Flash Channel
Use 3.3V Shared SPI
Note
Description
Note 16
If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.
G2412 and G2413 merge
071.01416.00GG
Layout Note:
Need very close to EC
ALL_SYS_PWRGD assert, delay 10ms; RESET_OUT# assert
Layout Note:
Connect GND and AGND planes via either 0R resistor or connect directly.
SB 0331
For USB TypeC
For 65982DC
Need check
Follow EV project circuit DY Q2417_20171005
TBD
X02 20170316 change
Follow XN13
eDP backlight Control from PCH
Need very close to EC
11/24
DELL
Wistron Corporation
KBC SMSC 1404
Bucky WHL
SA

Main Func = SPI Flash

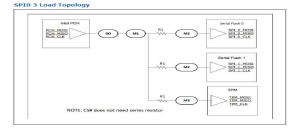
Edison 11/13 for STU

18 SPI_CS_ROM_N0
18,91 SPI_SO_ROM
18,91 SPI_CLK_ROM
15,18,91 SPI_SI_ROM
15,18 SPI_HOLD_ROM
15,18 SPI_WP_ROM



Dual SPI0 Devices + TPM Topology Guidelines

The CFL PCH supports TPM through SPI0 bus. The topology below was a full configuration which consist of 2 SPI0 Flash and 1 TPM device. The system can be configured with 1 SPI0 Flash and 1 TPM device.

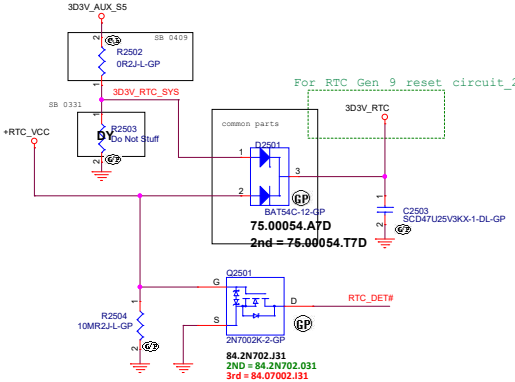


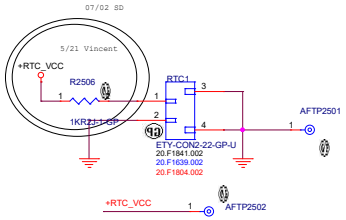
Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, mils	
				Segment	Total	Segment	Total

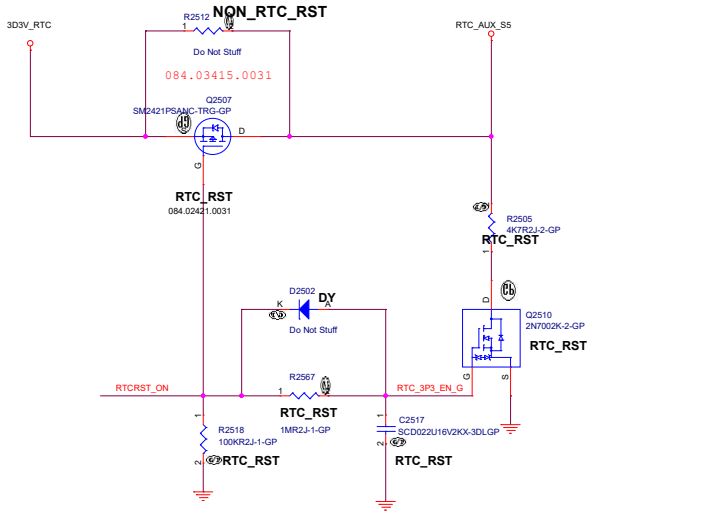
Notes:
1. R1 Resistor should be 15 ohm for 1.8V and 33 ohm for 3.3V. SPI0_1/O2 and SPI0_1/O3 connection to be pulled up with 1k ohm on R2 resistor.
2. 5 number of vias can be allowed.
3. Reference plane should be Continuous Ground Plane only allowed.
4. This topology relates to SPI0_IO_2 to 3, SPI0_MOSI, SPI0_MISO and SPI0_CLK
5. Design guideline support up to 50MHz.

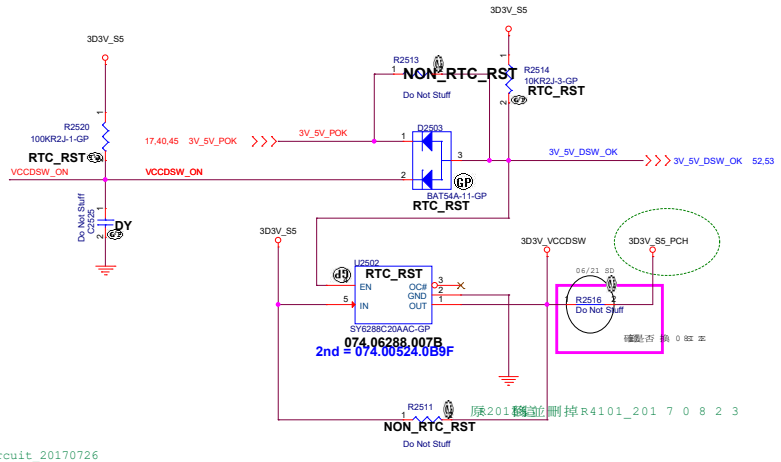
Main Func = RTC

15,20 RTC_DET#
24 VCCDSW_ON
18,24 RTCRST_ON









Add RTC Gen 9 reset circuit_20170726

BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash

Size	Document Number	Rev
A2	Bucky WHL	SA

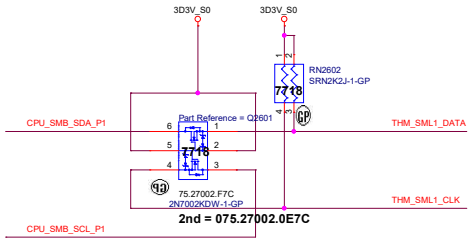
Date: Friday, July 13, 2018 Sheet 25 of 105

Main Func = Thermal Sensor

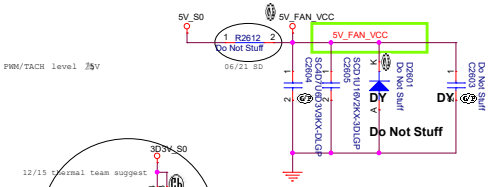
18,24,79 CPU_SMB_SDA_P1
18,24,79 CPU_SMB_SCL_P1
17,24,40 RESET_OUT#
40 PURE_HW_SHUTDOWN#
24 CMP_VOUT0
24 CMP_VIN0_R
24 FAN1_PWM
24 FAN1_TACH
17,61,63,66,76,91 PLT_RST#

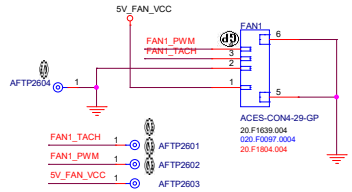
PWM FAN1

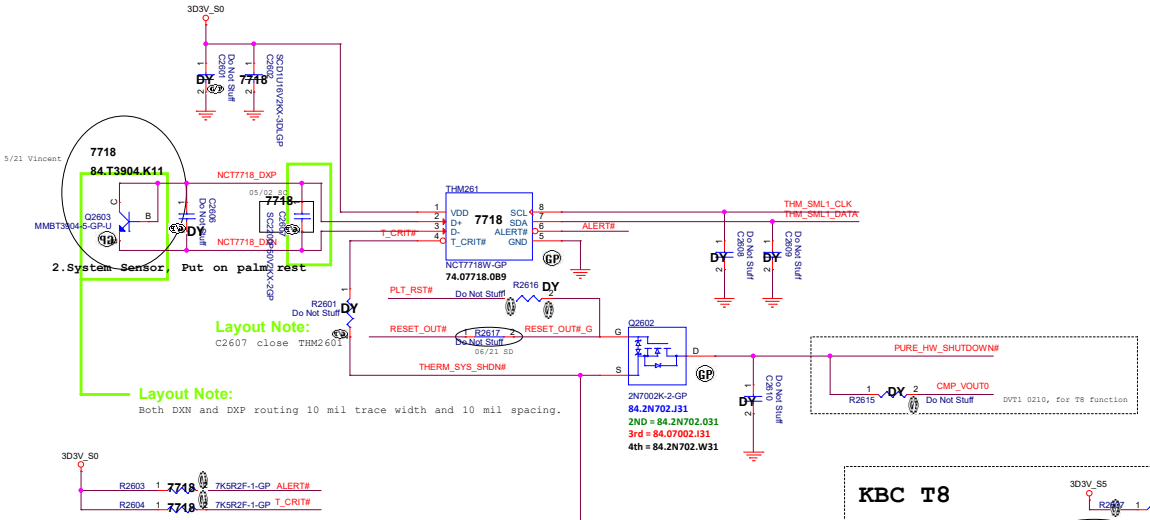
Layout Note:
Signal Routing Guideline:
Trace width = 15mil



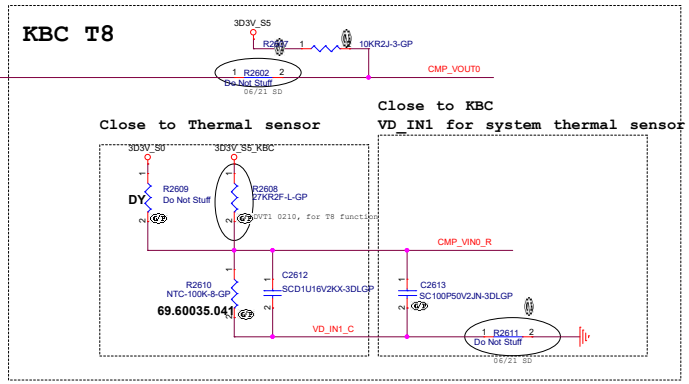
Need check







TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



BV UMA TC TPM

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan
Size: A2
Document Number: Bucky WHL
Rev: SA
Date: Friday, July 13, 2018
Sheet 26 of 105

Main Func = Audio

Audio Codec Chip ALC3204

19 HDA_SDIN0_CPU
19 HDA_SDOUT_CODEC
19 HDA_SYNC_CODEC
19 HDA_BITCLK_CODEC

29 AUD_SPK_R+
29 AUD_SPK_R-
29 AUD_SPK_L+
29 AUD_SPK_L-

55 DMIC_SDA_CODEC
55 DMIC_SCL_CODEC
17,40,68 PM_SLP_S3#
24 NB_Mute#
15,19 SPKR
24 BEEP
29 AUD_SENSE

29 LINE1_VREFO
29 MIC2_VREFO

29 AUD_HP1_JACK_L
29 AUD_HP1_JACK_R

29 LINE1_L
29 LINE1_R

29 AUD_SLEEVE
29 AUD_RING

Analog
Digital

1.8V power rail should be supplied by linear regulator, not switching regulator.if switch regulator is uvailable, please make sure that switch frequency operates at out-band(over 20KHz)

ALC3204
QFN40 (5X5)

ALC3204-CG-GR-U

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Layout Note:
Place close to Pin 20

Layout Note:
Tied at point only under Codec or near the Codec

DVDD must >= DVDD_IO

place close to pin8

place close to pin1

Close pin3

For RTC Gen9 reset circuit change power rail. 20070921

Azalia I/F EMI

150mA

SM2421PSANC-TRG-GP
084.02421.0031

75.00054.A7D

BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3204

Size: A2 | Document Number: Bucky WHL | Rev: SA

Date: Friday, July 13, 2018 | Sheet 27 of 105

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A4	*Bucky WHL*	*SA*

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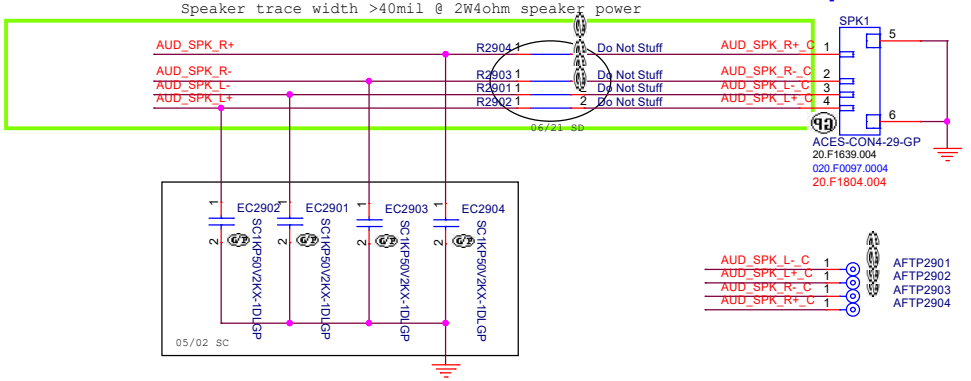
Main Func = Audio

27 AUD_SPK_R+
27 AUD_SPK_R-
27 AUD_SPK_L-
27 AUD_SPK_L+

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

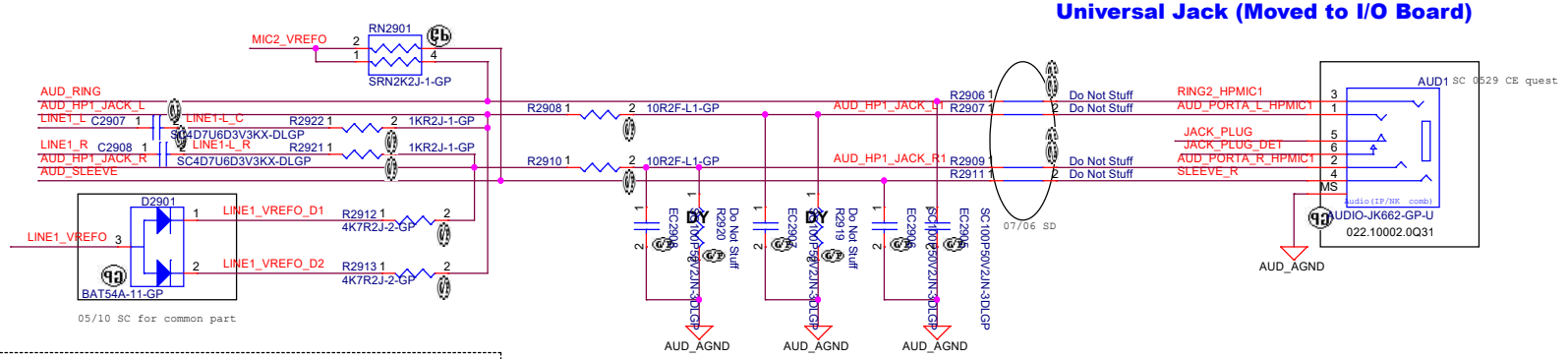
Speaker



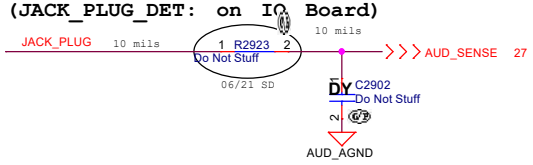
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L-
Pin4	SPK_L+

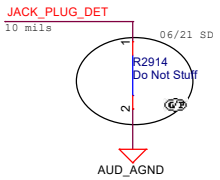
27 MIC2_VREFO
27 AUD_RING
27 AUD_HP1_JACK_L
27 LINE1_L
27 LINE1_R
27 AUD_HP1_JACK_R
27 AUD_SLEEVE
27 LINE1_VREFO

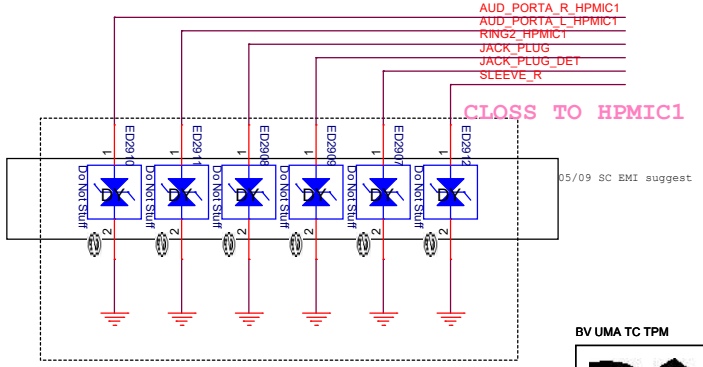
Universal Jack (Moved to I/O Board)



Delay circuit
(JACK_PLUG_DET: on IO Board)







BV UMA TC TPM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio IO**

Size	Document Number	Rev
A3	Bucky WHL	SA

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(Blanking)

BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	Bucky WHL	SA

Date: Friday, July 13, 2018 Sheet 30 of 105

Main Func = LAN

BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LAN RTL8106*

Size	Document Number	Rev
Custom	*Bucky WHL*	*SA*

Date: Friday, July 13, 2018 Sheet 31 of 105

Main Func = LAN

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Title: *XFOM&RJ45*

Size	Document Number	Rev
A3	*Bucky WHL*	*SA*

Date: Friday, July 13, 2018 Sheet 32 of 105

Main Func = Card Reader

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Title

Card Reader-RTS5170

Size	Document Number	Rev
A4	Bucky WHL	SA

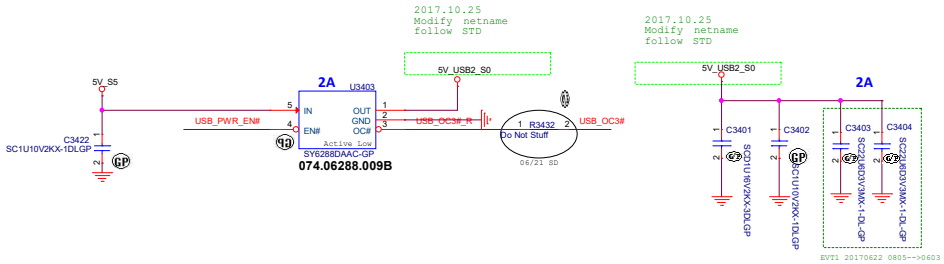
Date: Friday, July 13, 2018 Sheet 33 of 105

Main Func = USB2.0

16 USB_OC3#

24,35 USB_PWR_EN#

USB2.0 Port2 (IO Board)



Layout Note: Close IO2

BV UMA TC TPM

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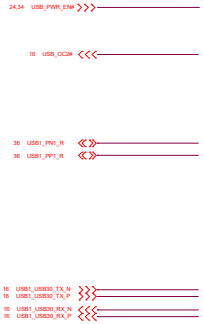
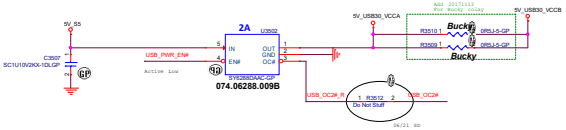
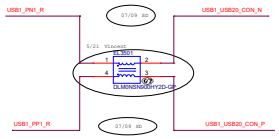
Title: USB2.0 CONN		
Size	Document Number: Bucky WHL	Rev: SA
Date: Friday, July 13, 2018	Sheet 34 of 105	

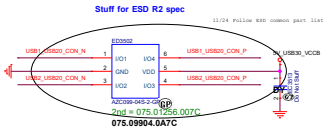
Main Func = USB3.0 Port2

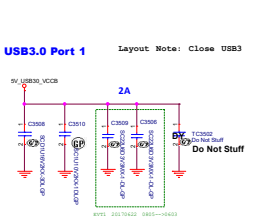
Main Func = USB3.0 Port1

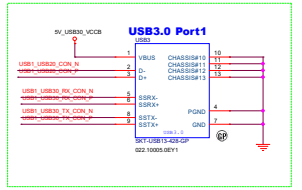


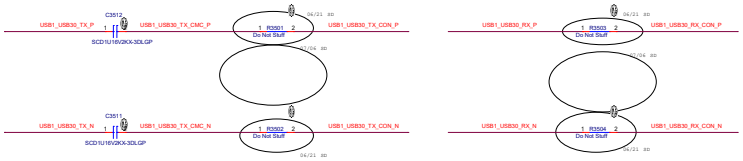


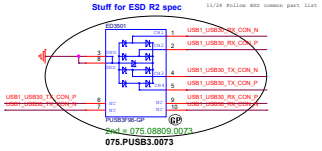




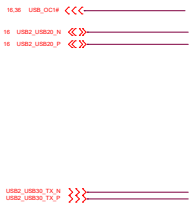


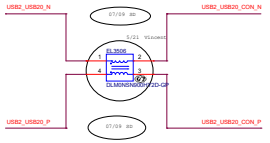


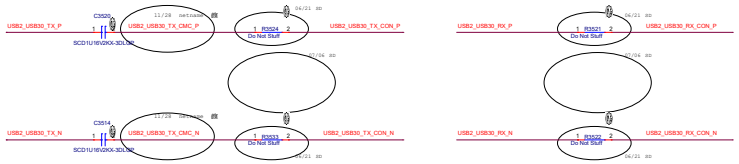


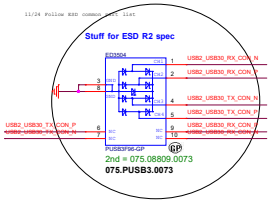


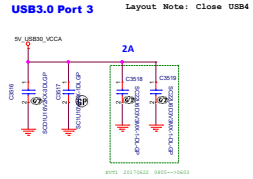
Main Func = USB3.0 Port3

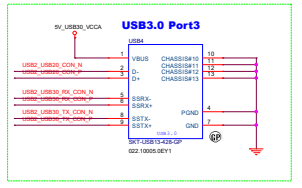












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Title: **USB3.0 CONN**

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Main Func = USB Charger

24,34,35 USB_PWR_EN#

24 USB_POWERSHARE_VBUS_EN

24 USB_PWR_SHR_EN_L#

16 USB_OC1#

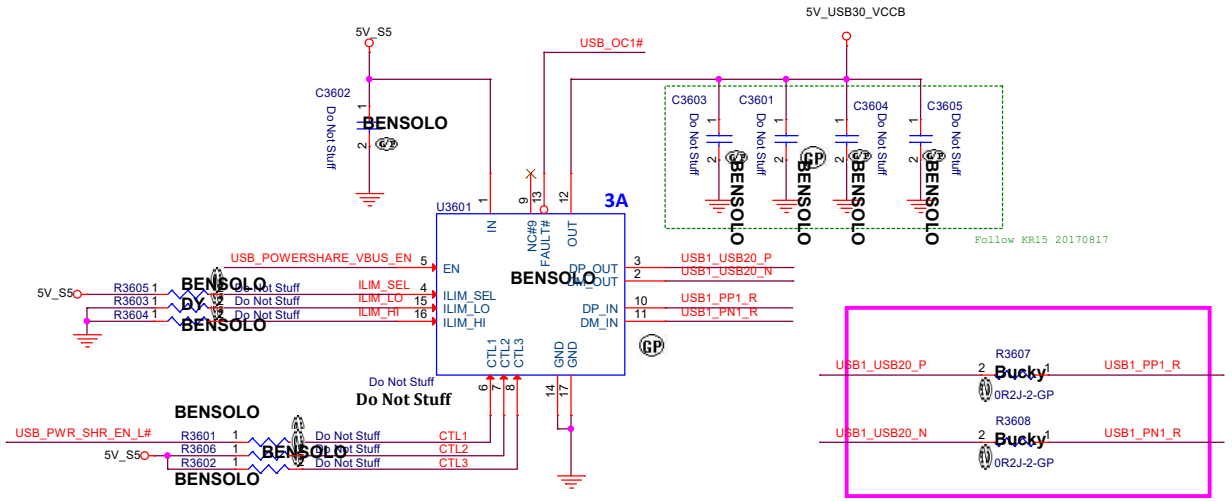
35 USB1_PN1_R

35 USB1_PP1_R

16 USB1_USB20_N

16 USB1_USB20_P

USB Charger Port1



Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

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Title: USB Charger

Size	Document Number	Rev
A3	Bucky WHL	SA

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(Blanking)

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Title

USB3.0 PORT

Size	Document Number	Rev
A4	Bucky WHL	SA

Date: Friday, July 13, 2018 Sheet 37 of 105

(Blanking)

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Title

Reserved

Size	Document Number	Rev
A4	***Bucky WHL***	***SA***

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Title

(RSVD)

Size	Document Number	Rev
A2	Bucky WHL	SA

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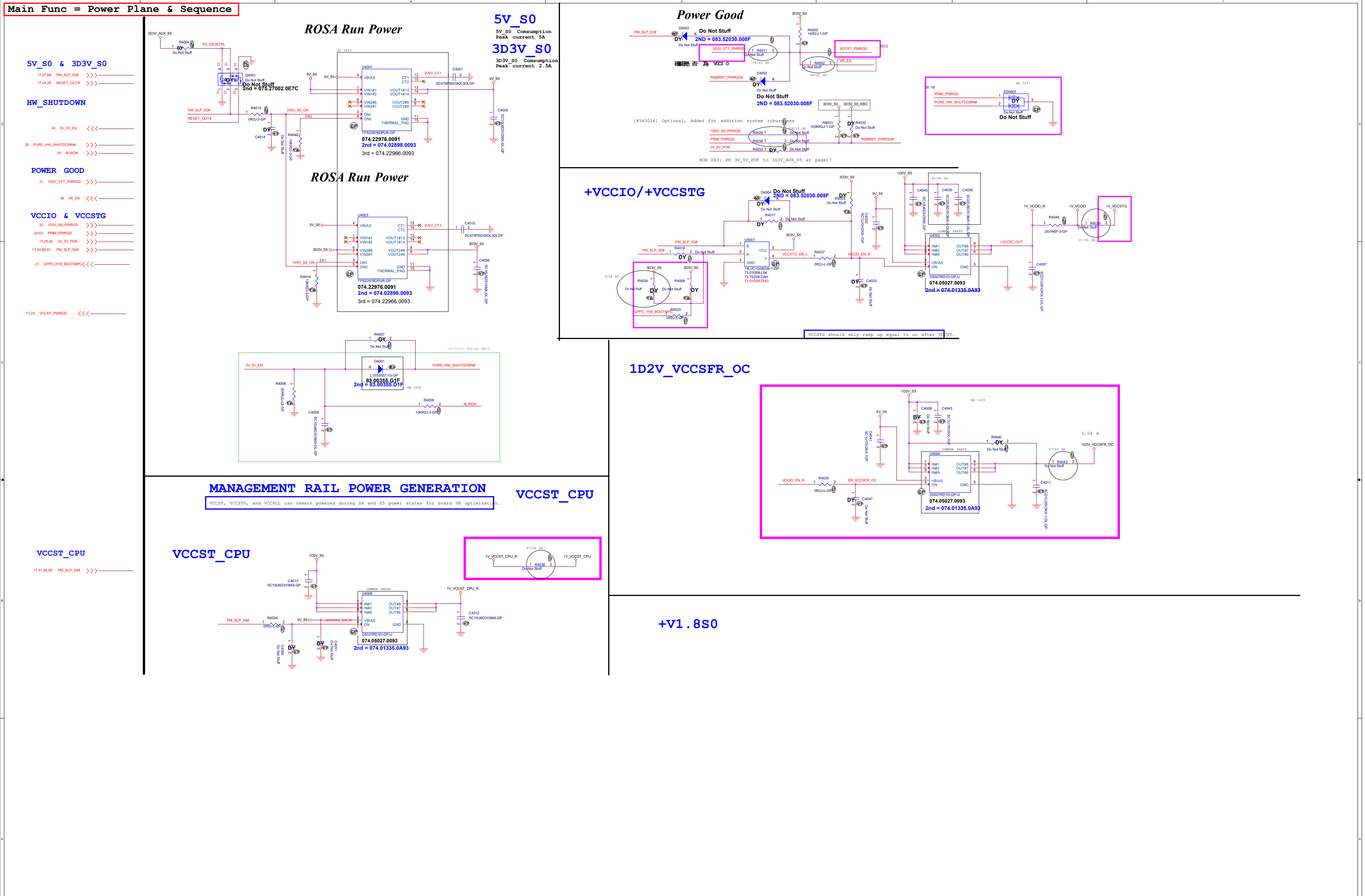

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Title: Power Plane Enable

Size: A1 | Document Number: Bucky WHL | Rev: SA

Date: Friday, July 13, 2018 | Sheet 40 of 105

Main Func = Power & Sequence

原410讓一用R2516_2017 0 82 3

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Title

Connected_Standby(1/2)+DS3

Size	Document Number	Rev
A4	Bucky WHL	SA

Date: Friday, July 13, 2018 Sheet 41 of 105

(Blanking)

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Title: *Connected_Standby(2/2)*

Size	Document Number	Rev
A4	Bucky WHL	SA

Date: Friday, July 13, 2018 Sheet 42 of 105

24 AC_DIS

17,44 ACOK_IN_M

24 PS_ID

24 HW_ACAVIN_NB

Main Func = ADT Input

Pin Definition: TBD

Layout Note:
PSID Layout width > 25mil

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

S1

S2

X01 20161230 change

X02 20170314 add

Barrel Adapter Piug-in Detect

TypeC full

074.01004.00BF

Main Func = M-BAT Input

Batt Connecter

Placement: Close to Batt Connector

2nd = 75.00099.K7D	2nd = 75.00099.K7D	2nd = 75.00099.K7D
3rd = 75.00099.Q7D	3rd = 75.00099.Q7D	3rd = 75.00099.Q7D
4th = 75.00099.D7D	4th = 75.00099.D7D	4th = 75.00099.D7D

24,44 PBAT_CHG_SMBCLK

24,44 PBAT_CHG_SMBDAT

24,44 PBAT_PRES#

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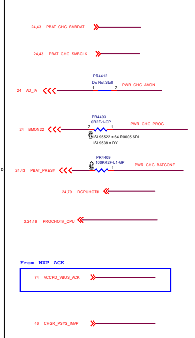
Title: DCIN

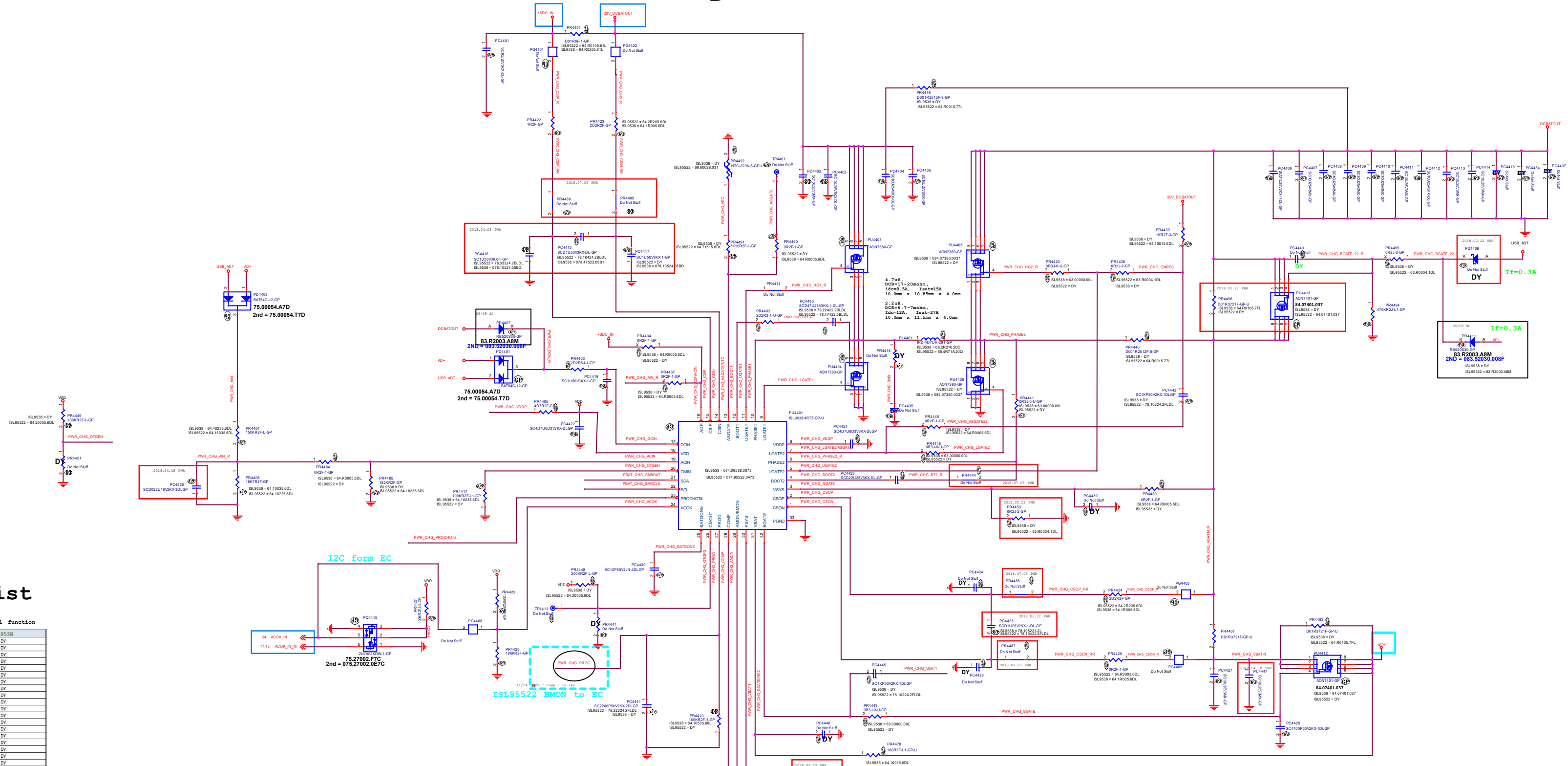
Size: A1 | Document Number: Bucky WHL | Rev: X02

Date: Friday, July 13, 2018 | Sheet 43 of 106

Main Func = Charger



ISL95522 Hybrid Charger
ISL9538 Buck-Boost Charger



BOM Change List

Data only and non -typeC — full function

Item	Location	ISL95522		ISL9538	
1	PR4437	0R	64.R0005.6DL	DY	
2	PR4491	7.15K	64.71515.6DL	DY	
3	PR4492	THERM 220K	69.60028.031	DY	
4	PR4440	0.001R	64.R0015.77L	DY	
5	PR4438	0R	63.R0034.1DL	DY	
6	PR4439	1K	64.10015.6DL	DY	
7	PR4453	0R	63.R0034.1DL	DY	
8	PC4445	1000p	78.10224.2FLDL	DY	
9	PR4483	0.01R	64.R0105.7FL	DY	
10	PR4493	0R	64.R0005.6DL	DY	
11	PR4448	200K	64.20035.6DL	DY	
12	PR4495	0R	63.R0034.1DL	DY	
13	PR4485	182K	64.18235.6DL	DY	
14	PR4449	200K	64.20035.6DL	DY	
15	PD4409	DY		DY	
16	PR4445	0R	64.R0005.6DL	DY	
17	PR4479	0.001R	64.R0015.77L	DY	
18	PD4411	DIODE	83.R2003.A8M	DY	
19	PC4442	1000p	78.10224.2FLDL	DY	
20	PC4433	470p	78.47124.2FLDL	DY	
21	PC4441	2200p	78.22224.2FLDL	DY	
22	PC4416	0.033u	78.33324.2BLDL	1u	078.10524.05BD
23	PR4434	DY		0R	64.R0005.6DL
24	PR4490	DY		0R	64.R0005.6DL
25	PU4406	DY		AON7380	084.07380.0037
26	PR4480	DY		0R	64.R0005.6DL
27	PR4446	DY		0R	63.00000.00L
28	PR4420	DY		0R	63.00000.00L
29	PU4412	DY		AON7401	84.07401.037
30	PR4443	DY		0R	63.00000.00L
31	PR4410	DY		105K	64.10535.60L
32	PR4417	DY		100K	64.10035.6DL
33	PR4441	DY		0R	63.00000.00L
34	PR4484	DY		0R	64.R0005.6DL
35	PU4405	DY		AON7380	084.07380.0037
36	PR4423	2.2R	64.2R205.6DL	1R	64.1R005.6DL
37	PC4415	0.1u	78.10424.2BLDL	4.7u	078.47522.05B1
38	PR4424	2.2R	64.2R205.6DL	1R	64.1R005.6DL
39	PR4425	0R	64.R0005.6DL	1R	64.1R005.6DL
40	PC4425	0.1u	78.10422.5FLDL	1u	78.10523.L2L
41	PR4411	100R	64.10005.6DL	499R	64.49905.6DL
42	PC4431	0.033u	78.33322.2FL	0.01u	78.10322.2FLDL
43	PR4404	150K	64.15035.6DL	402K	64.40235.6DL
44	PR4406	18.7K	64.18725.6DL	100K	64.10035.6DL
45	PU4401	ISL95522	074.95522.0A73	ISL9538	074.09538.0073
46	PR4401	0.01R	64.R0105.81L	0.02R	64.R0205.81L
47	PL4401	4.7uH	68.4R71A.20Q	2.2uH	68.2R210.20C
48	PR4478	100R	64.10005.6DL	1K	64.10015.6DL
49	PC4436	0.47u	78.47422.5BLDL	0.22u	78.22422.2BLDL
50	PU4413	AON7401-GP	84.07401.037	DY	
51	PR4496	DY		0.01R	64.R0105.7FL
52	PC4417	DY		1u	078.10524.05BD

ISL95522

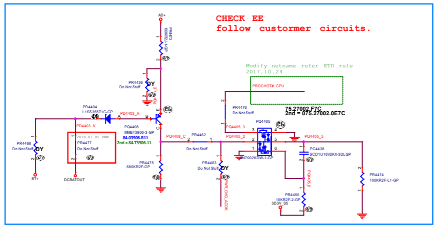
Table 17. Prog Pin Programming Options

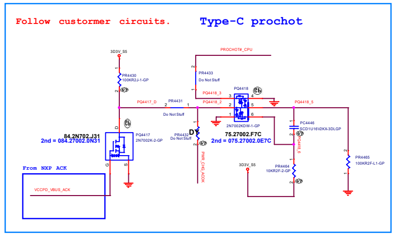
Prog-GND Resistance (kΩ) Typ (1% Standard Resistor)	Charger Type	Current Sense Resistor Value	Default # of Battery Cells in Series
0	NVDC	$R_{s1}:R_{s2} = 2:1$, $R_{s1} = 10m\Omega$, $R_{s2} = 5m\Omega$ or $R_{s1} = 20m\Omega$, $R_{s2} = 10m\Omega$	3
22.6			4
38.3			2
69.8		$R_{s1}:R_{s2} = 1:1$, $R_{s1} = 10m\Omega$, $R_{s2} = 10m\Omega$ or $R_{s1} = 20m\Omega$, $R_{s2} = 20m\Omega$	3
86.6			4
102			2
150	HPB		4
165			2
182			3
215		$R_{s1}:R_{s2} = 2:1$, $R_{s1} = 10m\Omega$, $R_{s2} = 5m\Omega$ or $R_{s1} = 20m\Omega$, $R_{s2} = 10m\Omega$	4
237			2
255			3

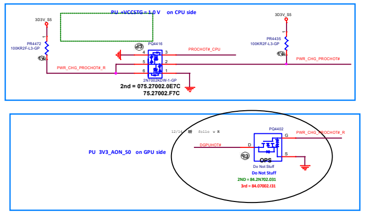
ISL9538

TABLE 22. PROG PIN PROGRAMMING OPTIONS

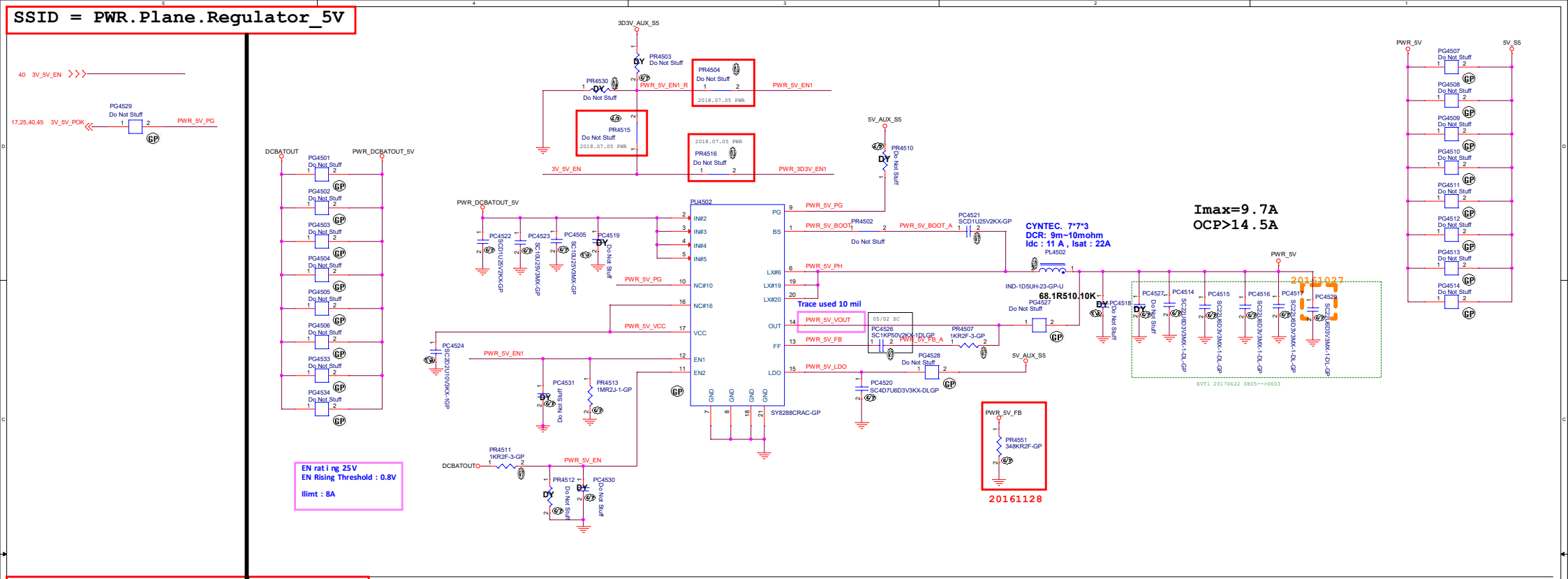
PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
	0		1	733kHz	No	0.476
	8.45			733kHz	No	1.5
	14.7			1MHz	No	1.5
	21.0			1MHz	No	0.476
	28.0			733kHz	Yes	0.476
	35.7			733kHz	Yes	1.5
	43.2		2	733kHz	Yes	1.5
	52.3			733kHz	Yes	0.476
	61.9			1MHz	No	0.476
	71.5			1MHz	No	1.5
	82.5			733kHz	No	1.5
	93.1			733kHz	No	0.476
	105		3	733kHz	No	0.476
	118			733kHz	No	1.5
	133			1MHz	No	1.5
	147			1MHz	No	0.476
	162			733kHz	Yes	0.476
	178			733kHz	Yes	1.5
	196		4	733kHz	Yes	1.5
	215			733kHz	Yes	0.476
	237			1MHz	No	0.476
	261			1MHz	No	1.5
	287			733kHz	No	1.5
	316			733kHz	No	0.476
	348		1	733kHz	No	0.476



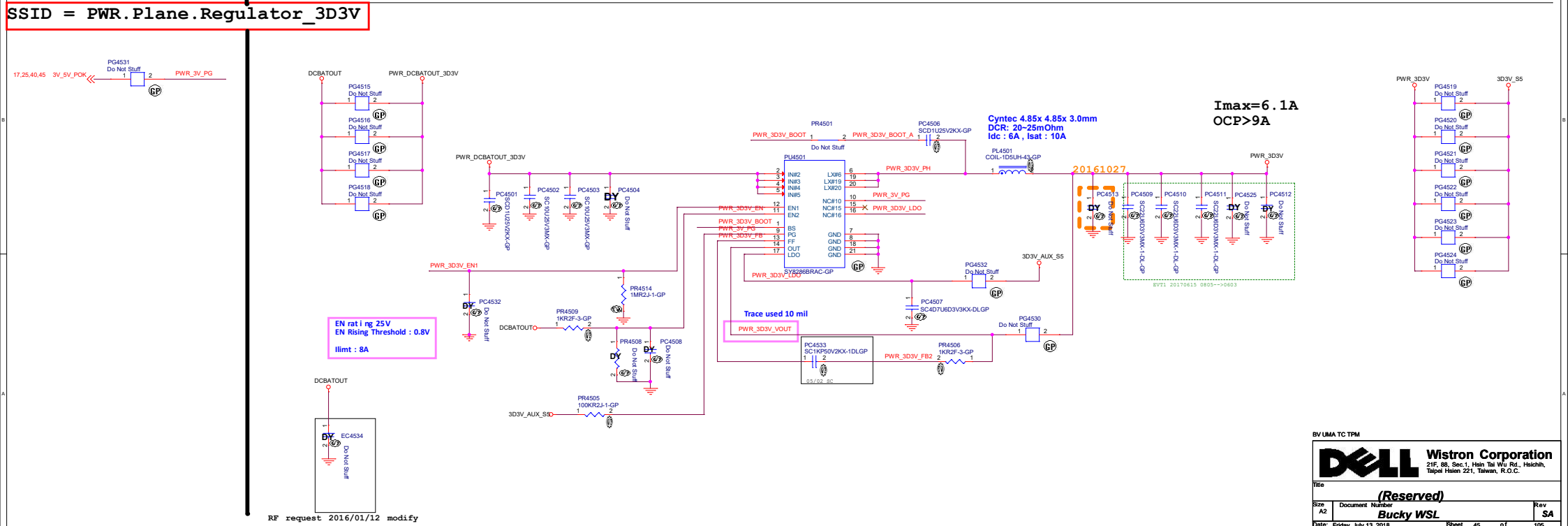




SSID = PWR.Plane.Regulator_5V



SSID = PWR.Plane.Regulator_3D3V



RF request 2016/01/12 modify

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Title: (Reserved)

Size	Document Number	Rev
A2	Bucky WSL	SA

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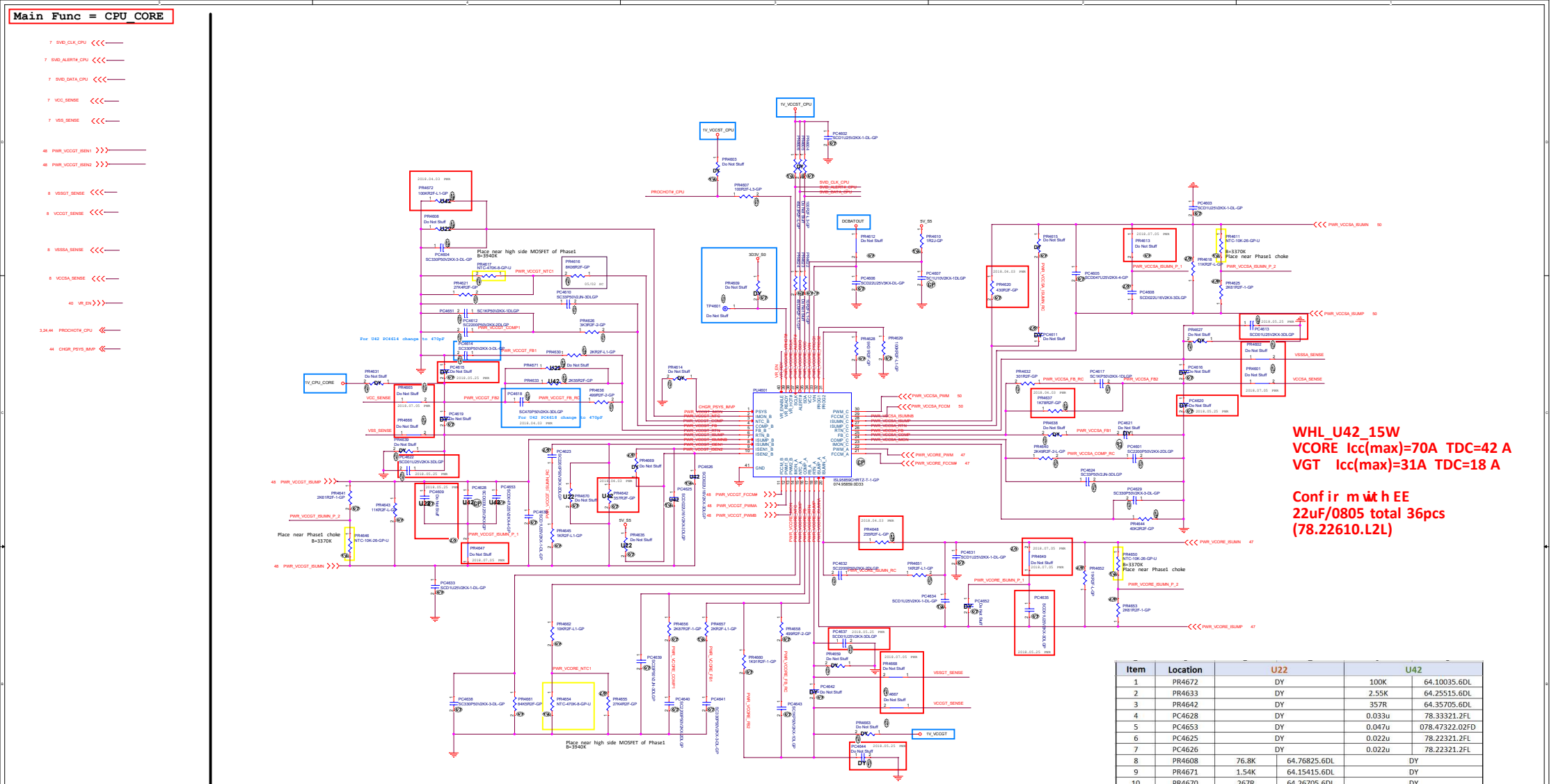
Main Func = CPU_CORE



Item	Location	U22		U42	
1	PR4672	DY		100K	64.10035.6DL
2	PR4633	DY		2.55K	64.25515.6DL
3	PR4642	DY		357R	64.35705.6DL
4	PC4628	DY		0.033u	78.33321.2FL
5	PC4653	DY		0.047u	078.47322.02FD
6	PC4625	DY		0.022u	78.22321.2FL
7	PC4626	DY		0.022u	78.22321.2FL
8	PR4608	76.8K	64.76825.6DL	DY	
9	PR4671	1.54K	64.15415.6DL	DY	
10	PR4670	267R	64.26705.6DL	DY	
11	PR4635	1K	64.10015.6DL	DY	
12	PC4609	0.01u	78.10322.2FLDL	DY	
11	PC4618	1000p	78.10224.2FLDL	470p	78.47124.2FLDL
13	PU4802	DY		AOZ5038	074.05038.0073
14	PC4816	DY		10u	78.10612.5BL
15	PC4817	DY		10u	78.10612.5BL
16	PC4814	DY		10u	78.10612.5BL
17	PC4815	DY		10u	78.10612.5BL
18	PR4813	DY		2R2	64.2R205.6DL
19	PC4812	DY		1u	78.10523.5FLDL
20	PC4866	DY		1u	78.10523.5FLDL
21	PR4810	DY		2R2	64.2R205.55L
22	PC4811	DY		0.022u	78.22422.2BLDL
23	PL4802	DY		0.15uH	68.R1510.20A
24	PR4823	DY		100K	64.10035.6DL
25	PR4816	DY		3.65K	64.36515.6DL
26	PR4815	DY		10R	64.10R05.L1L
27	PR4821	DY		100K	64.10035.6DL
28	PT4803	DY		330u	79.33719.20C

8V UMA TC TPM

Wistron Corporation
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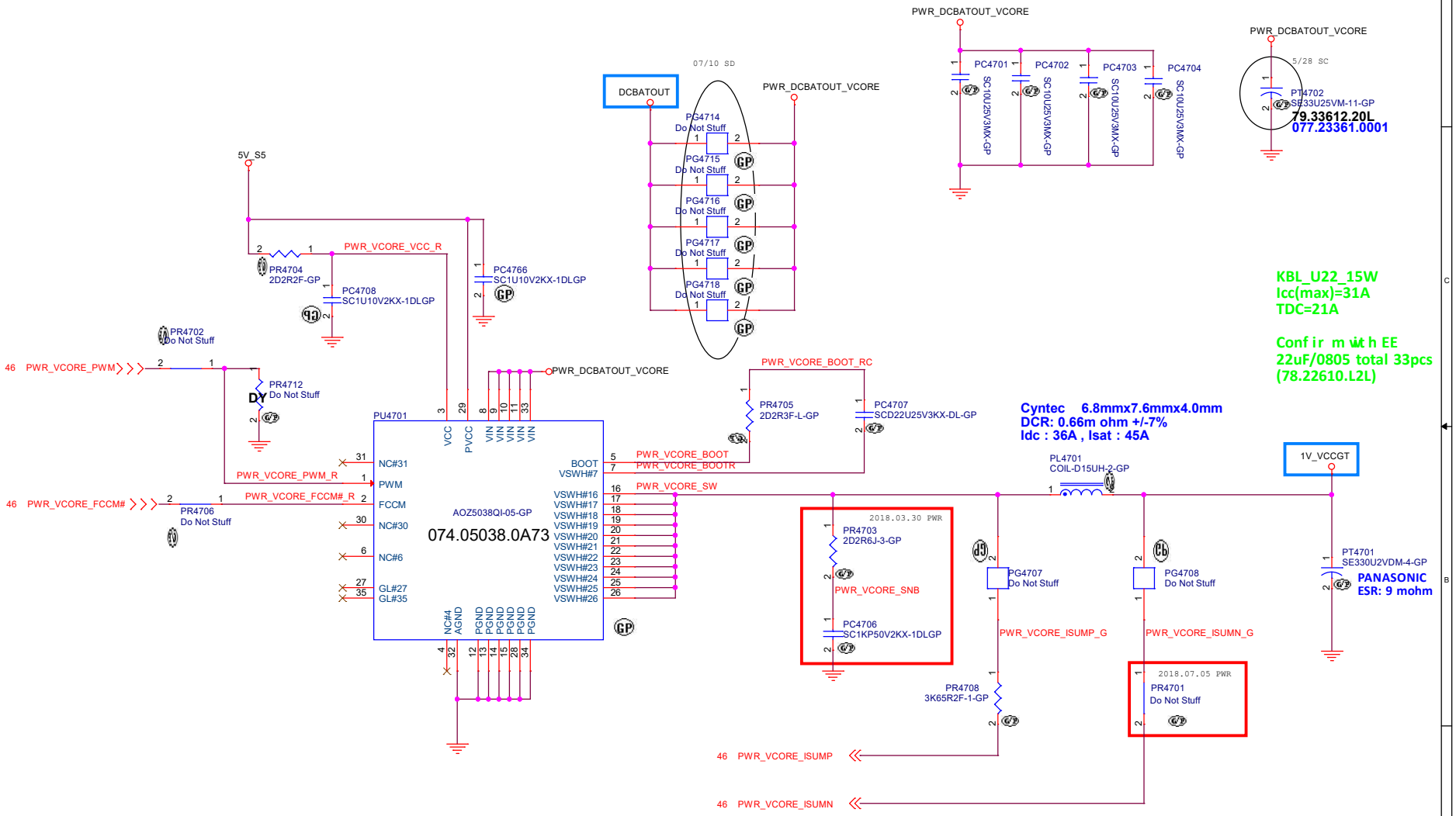
Taipei Hsien 221, Taiwan, R.O.C.

File: NCP81208MN_CPU_VCORE(1/3)

Size	Document Number	Rev
A1	Bucky WHL	SA

Date: Friday, July 13, 2018 Sheet 46 of 55

Main Func = CPU_CORE



BV UMA TC TPM

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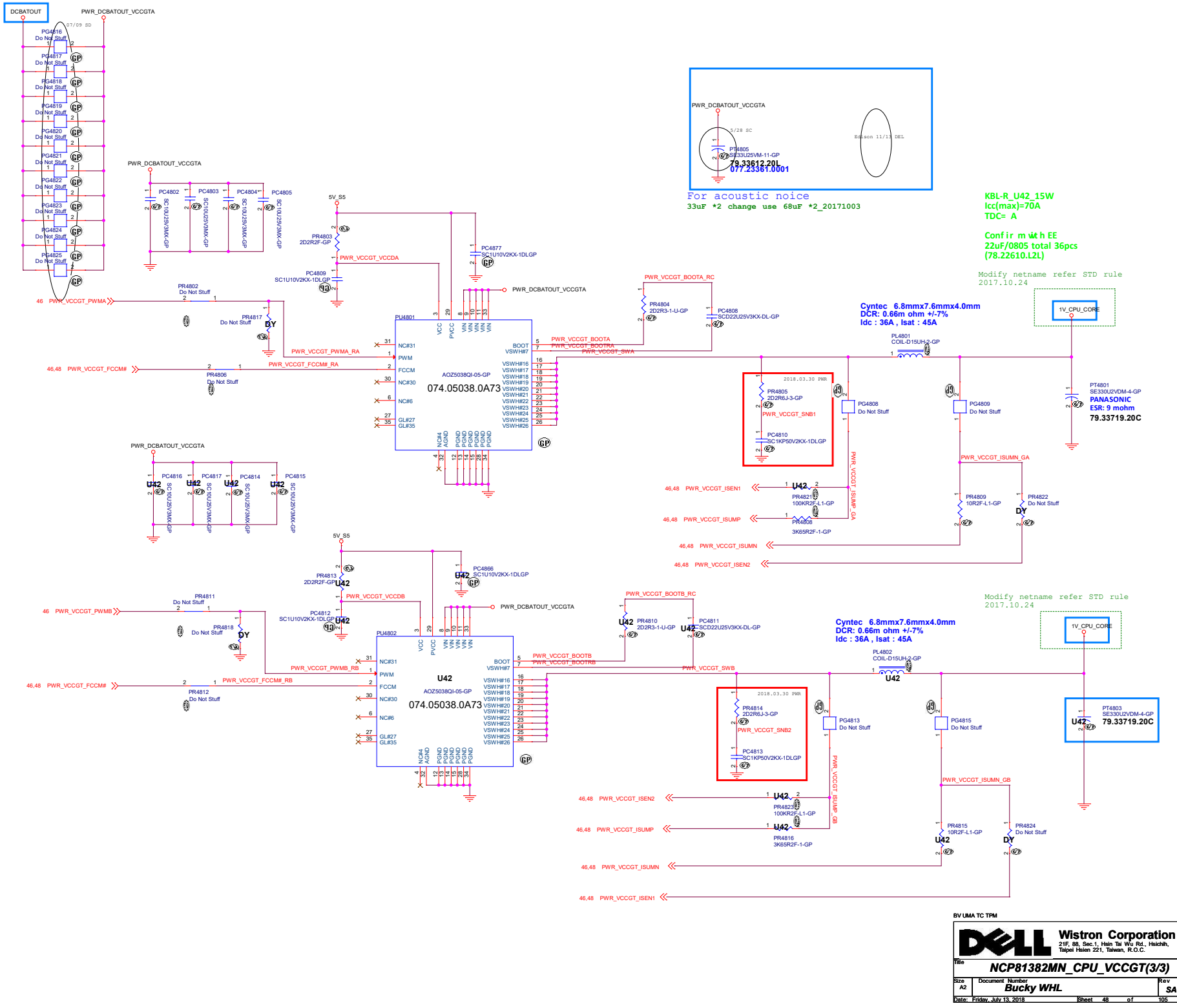
Taipei Hsien 221, Taiwan, R.O.C.

Title	NCP81382MN_CPU_VCORE(2/3)	
Size A3	Document Number Bucky WHL	Rev SA
Date: Friday, July 13, 2018	Sheet 47 of 105	

Main Func = CPU_CORE



BV UMA TC TPM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81382MN_CPU_VCCGT(3/3)

Size	Document Number	Rev
A2	Bucky WHL	SA

Date: Friday, July 13, 2018 Sheet 48 of 105

BV UMA TC TPM

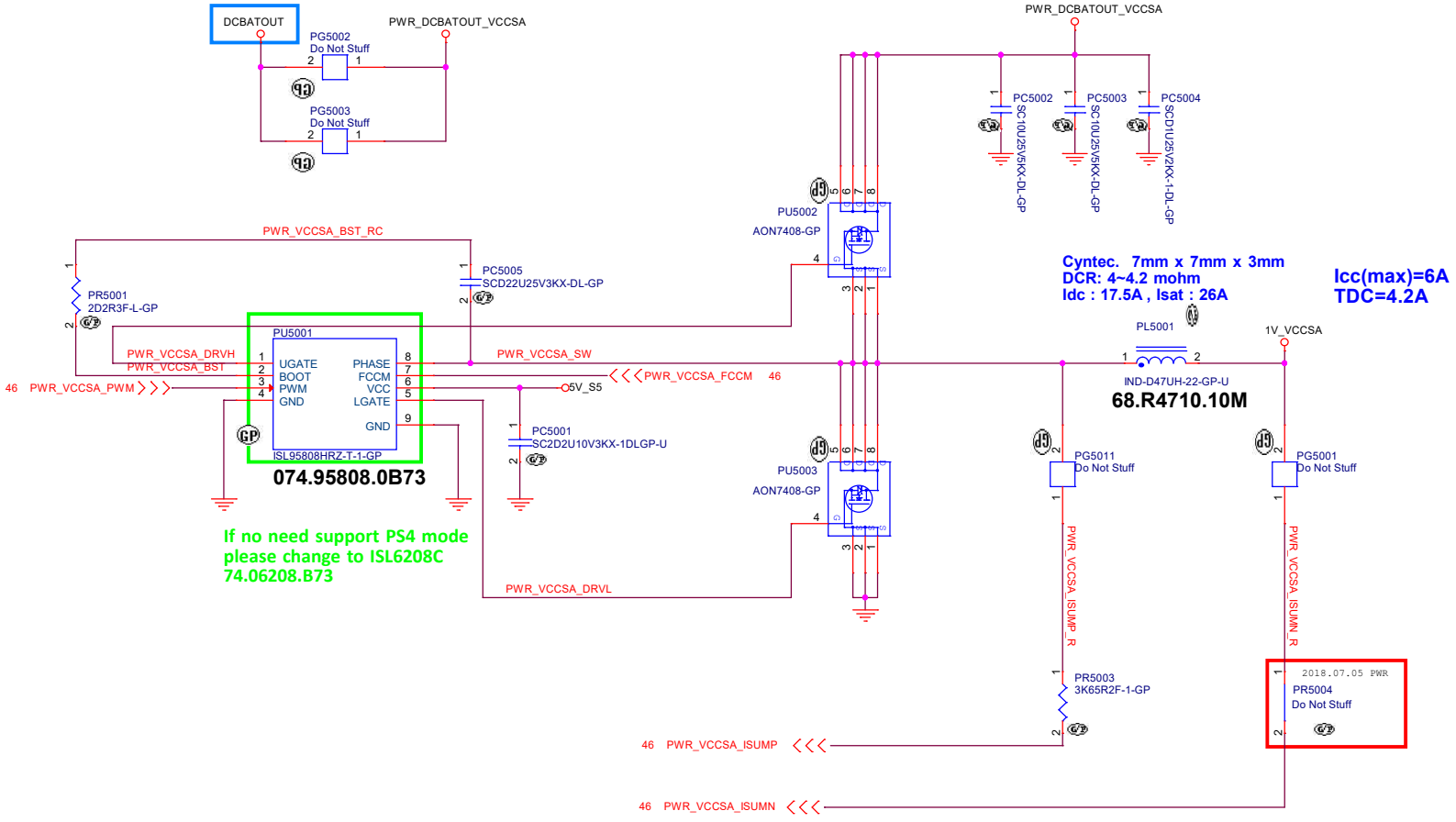
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81210MN_CPU_VCCGTUS

Size: A2 | Document Number: Bucky WHL | Rev: SA

Date: Friday, July 13, 2018 | Sheet 49 of 105

Main Func = VCCSA



BV UMA TC TPM

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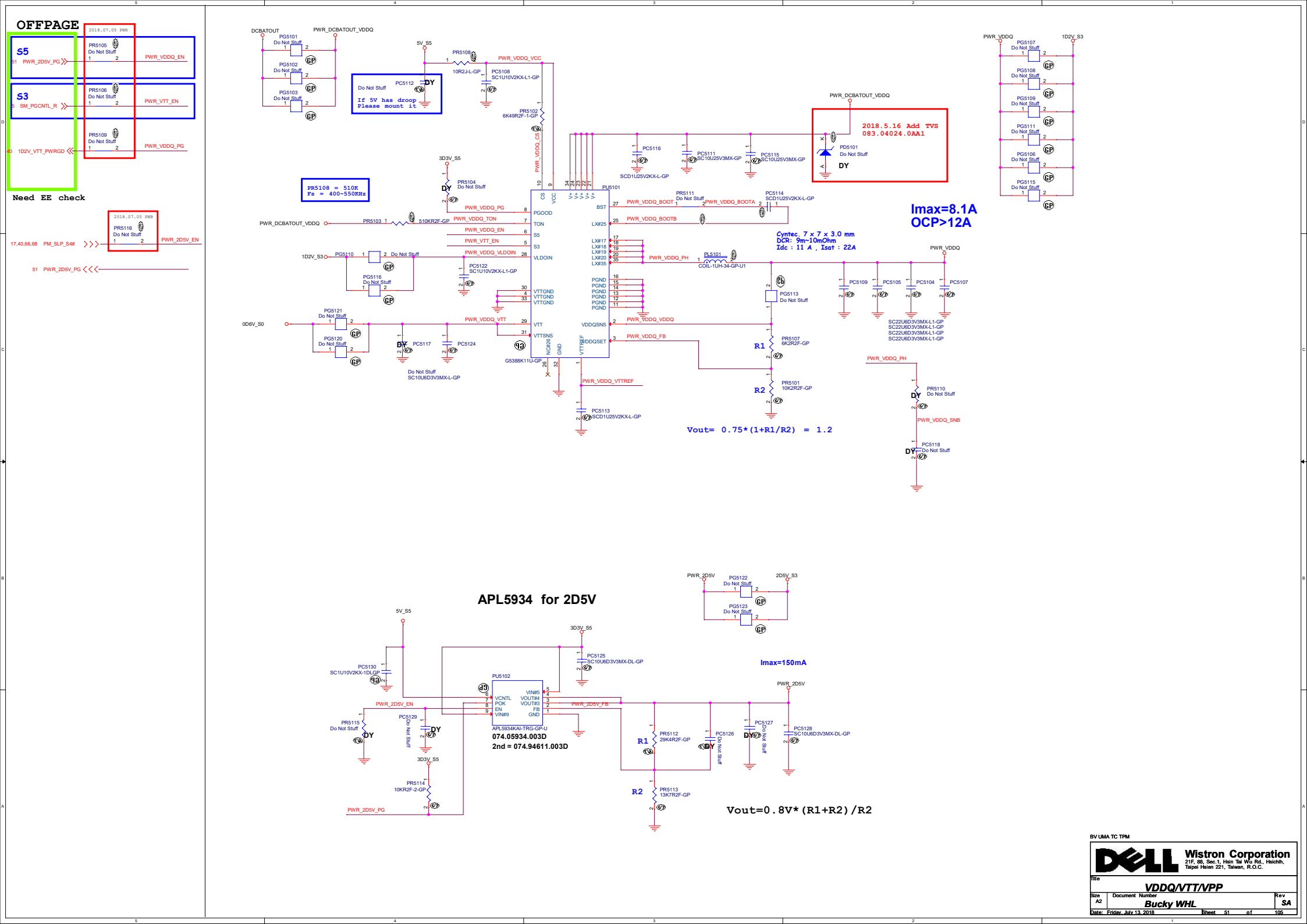
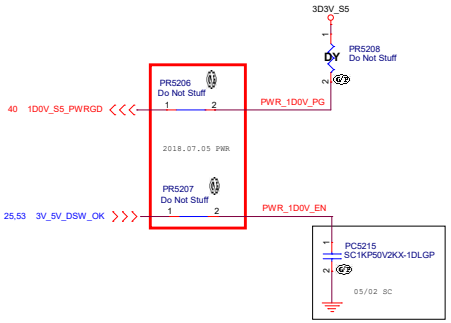
Taipei Hsien 221, Taiwan, R.O.C.

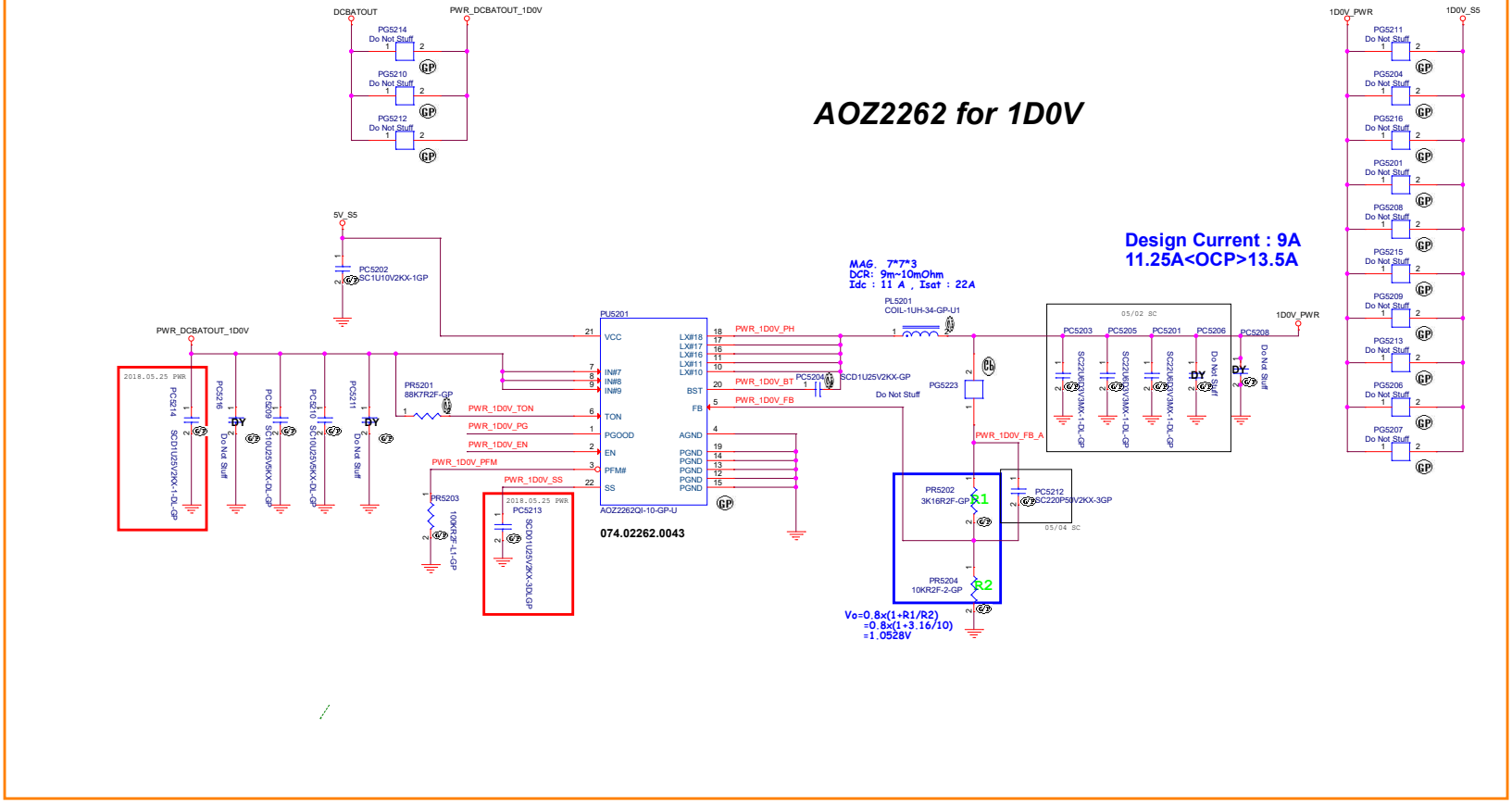
Title	VCCSA	
Size A3	Document Number: Bucky WHL	Rev SA
Date: Friday, July 13, 2018	Sheet 50 of 105	


OFFPAGE
S5
PWR_2D5V_PG
PWR_VDDQ_EN
S3
SM_PGCNTL_R
PWR_VTT_EN
1D2V_VTT_PWRGD
PWR_VDDQ_PG
Need EE check
2018.07.05 PWR
PR5116
Do Not Stuff
PWR_2D5V_EN
17,40,66,68 PM_SLP_S4#
51 PWR_2D5V_PG
DCBATOUT
PWR_DCBATOUT_VDDQ
PG5101
PG5102
PG5103
Do Not Stuff
5V_S5
PR5108
10R2J-L-GP
PWR_VDDQ_VCC
PC5108
SC1U10V2KX-L1-GP
PC5112
DY
If 5V has droop
Please mount it
PR5102
6K49R2F-1-GP
PWR_VDDQ_CS
PC5116
SCD1U25V2KX-L-GP
PC5111
SC10U25V3MX-GP
PC5115
SC10U25V3MX-GP
PWR_DCBATOUT_VDDQ
2018.5.16 Add TVS
083.04024.0AA1
PD5101
Do Not Stuff
DY
PWR_VDDQ
1D2V_S3
PG5107
PG5108
PG5109
PG5111
PG5106
PG5115
3D3V_S5
PR5104
Do Not Stuff
PR5108 = 510K
Fs = 400~550KHz
PR5103
510KR2F-GP
PWR_VDDQ_PG
PWR_VDDQ_TON
PWR_VDDQ_EN
PWR_VTT_EN
PWR_VDDQ_VLDOIN
PU5101
CS
VCC
PGOOD
TON
S5
S3
VLDOIN
VTTGND
VTTGND
VTTGND
VTT
VTTSNS
NC#26
GND
VTTREF
VDDQSET
VDDQSNS
BST
LX#25
LX#17
LX#18
LX#19
LX#20
LX#35
PGND
PWR_VDDQ_BOOT
PWR_VDDQ_BOOTA
PWR_VDDQ_BOOTB
PWR_VDDQ_PH
PWR_VDDQ_VDDQ
PWR_VDDQ_FB
PWR_VDDQ_VTTREF
G5388K11U-GP
PR5111
Do Not Stuff
PC5114
SCD1U25V2KX-L-GP
Imax=8.1A
OCP>12A
Cyntec, 7 x 7 x 3.0 mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A
PL5101
COIL-1UH-34-GP-U1
PG5110
PG5116
PC5122
SC1U10V2KX-L1-GP
PG5121
PG5120
PC5117
PC5124
Do Not Stuff
SC10U6D3V3MX-L-GP
0D6V_S0
PG5113
Do Not Stuff
PC5109
PC5105
PC5104
PC5107
SC22U6D3V3MX-L1-GP
SC22U6D3V3MX-L1-GP
SC22U6D3V3MX-L1-GP
SC22U6D3V3MX-L1-GP
R1
PR5107
6K2R2F-GP
R2
PR5101
10K2R2F-GP
PC5113
SCD1U25V2KX-L-GP
Vout= 0.75*(1+R1/R2) = 1.2
PWR_VDDQ_PH
PR5110
Do Not Stuff
PWR_VDDQ_SNB
PC5118
Do Not Stuff
APL5934 for 2D5V
PWR_2D5V
PG5122
PG5123
2D5V_S3
Imax=150mA
PC5130
SC1U10V2KX-1DLGP
PC5125
SC10U6D3V3MX-DL-GP
PU5102
VCNTL
POK
EN
VIN#9
VIN#5
VOUT#4
VOUT#3
FB
GND
APL5934KAI-TRG-GP-U
074.05934.003D
2nd = 074.94611.003D
PWR_2D5V_EN
PWR_2D5V_FB
PR5115
Do Not Stuff
PC5129
Do Not Stuff
PR5112
29K4R2F-GP
PC5126
Do Not Stuff
PC5127
Do Not Stuff
PC5128
SC10U6D3V3MX-DL-GP
PR5114
10KR2F-2-GP
PR5113
13K7R2F-GP
PWR_2D5V_PG
Vout=0.8V*(R1+R2)/R2
BV UMA TC TPM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VDDQ/VTT/VPP
Size
A2
Document Number
Bucky WHL
Rev
SA
Date: Friday, July 13, 2018
Sheet 51 of 105

SSID = PWR.Plane.Regulator_1D0V



AOZ2262 for 1D0V



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Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A2	*Bucky WHL*	*SA*

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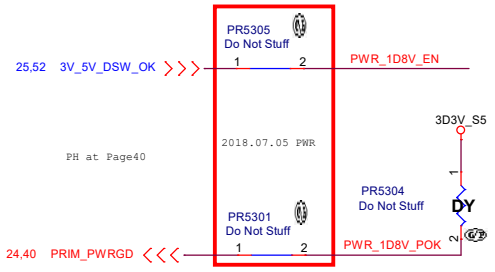
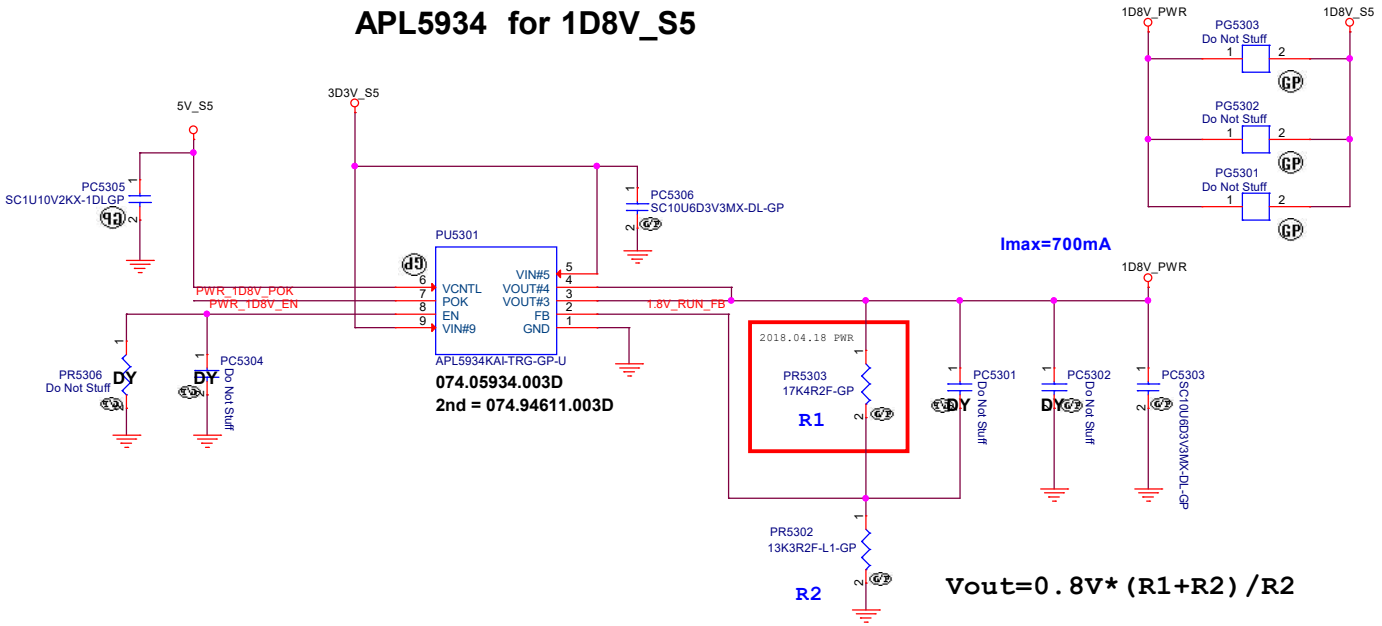
Main Func = 1D8V



APL5934 for 1D8V_S5



BV UMA TC TPM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: 053_LDO-V1D8V&2D5V

Size	Document Number	Rev
A3	Bucky WHL	SA

Date: Friday, July 13, 2018 Sheet 53 of 105

Main Func = 2D5V/ 1D8V

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Taipei Hsien 221, Taiwan, R.O.C.

Title: 054_LDO-V1D8V&2D5V

Size	Document Number	Rev
A3	Bucky WHL	SA

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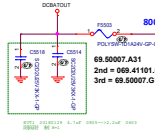
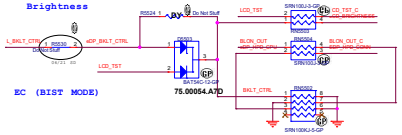
Main Func = LCD

INVERTER POWER

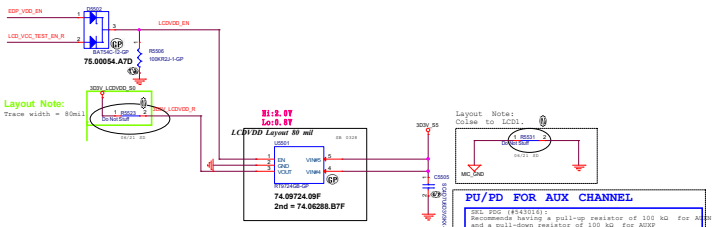


Brightness



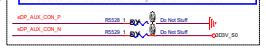
EC (BIST MODE)

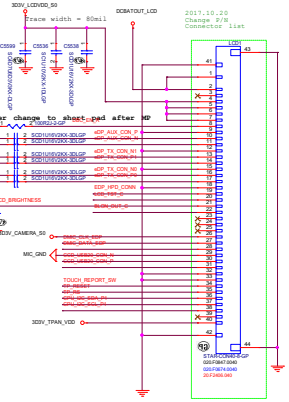
LCDVDD

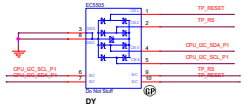


PU/PD FOR AUX CHANNEL

SKL 9DG (#543016):
Recommends having a pull-up resistor of 100 kΩ for AUX0 and a pull-down resistor of 100 kΩ for AUX0 between the AC capacitor and the connector, to assist source detection by the sink device.



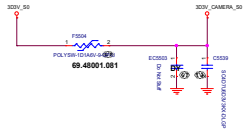


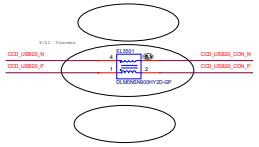


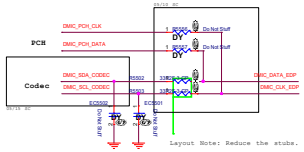
Main Func = CAMERA

Follow Santa Fe reserved for modern standby

CAMERA POWER

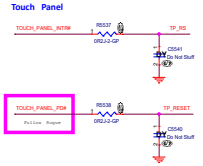


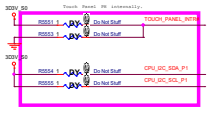




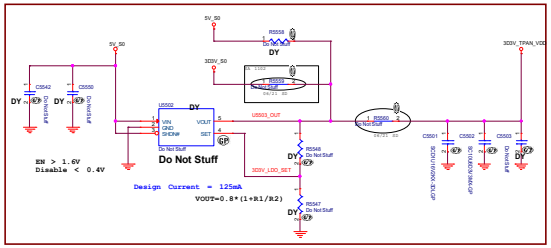
Main Func = Touch panel

Touch Panel





TOUCH PANEL POWER



8V LMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD&CAM&DMC&Touch

Size: Custom | Document Number: Bucky WHL | Rev: SA

Date: Friday, July 13, 2018 | Sheet 55 of 105

Main Func = CRT

BV UMA TC TPM

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title
CRT(Reserved)

Size A3 | Document Number: Bucky WHL | Rev: SA

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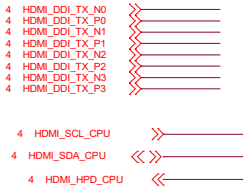
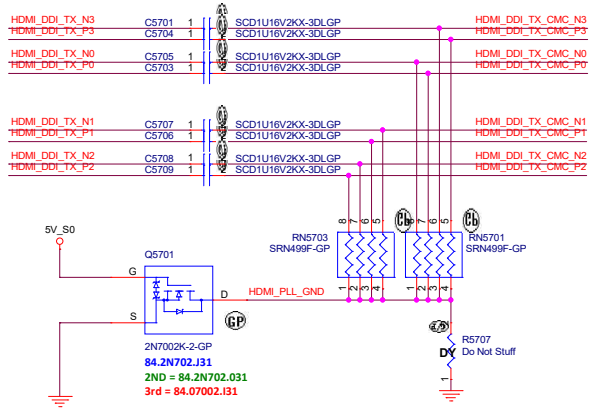
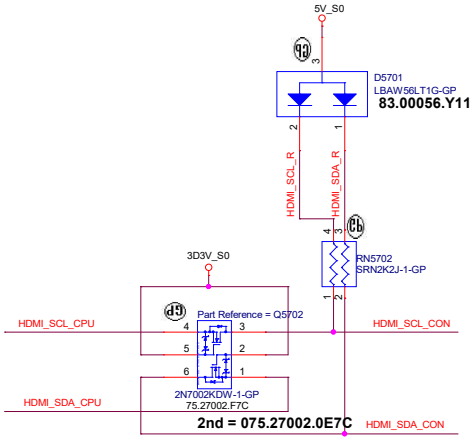
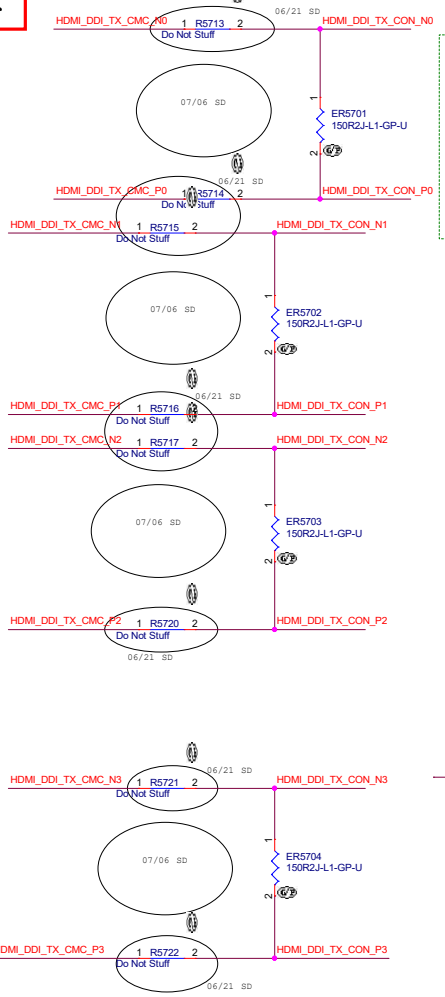
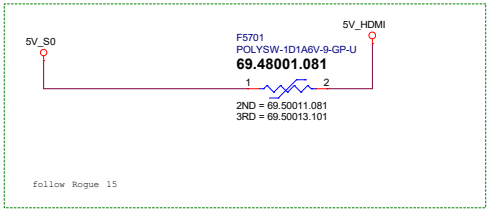
SSID = HDMI Level Shifter/Connector

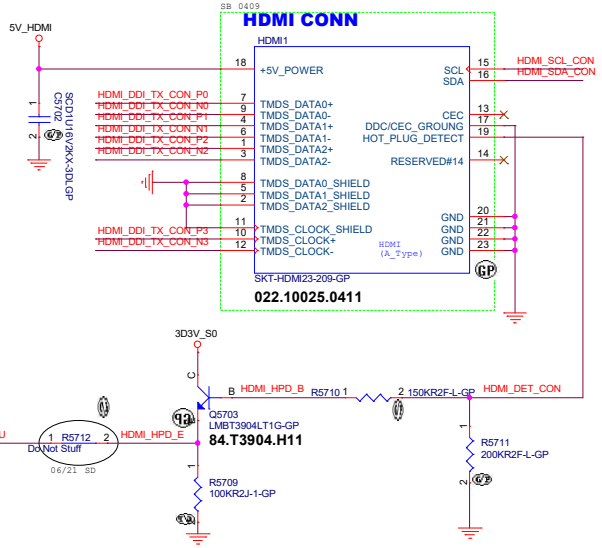




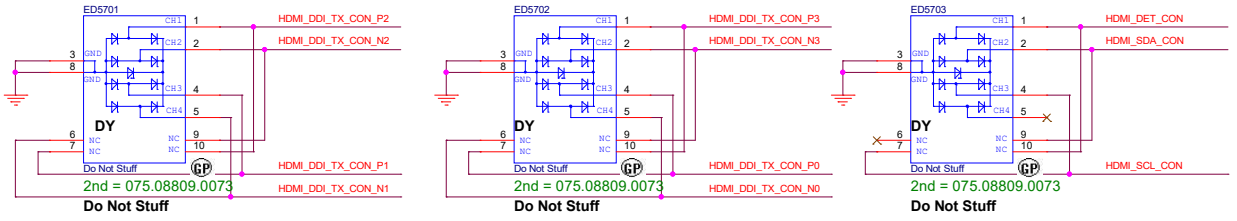








EMI Request:



BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HDMI	
Size: Custom	Document Number: Bucky WHL	Rev: SA
Date: Friday, July 13, 2018	Sheet 57 of 105	

(Blanking)

BV UMA TC TPM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A3	*Bucky WHL*	*SA*

Date: Friday, July 13, 2018 Sheet 58 of 105

(Blanking)

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Title
(Reserved)

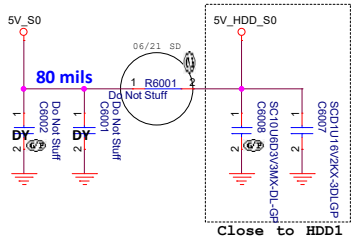
Size	Document Number	Rev
A3	*Bucky WHL*	*SA*

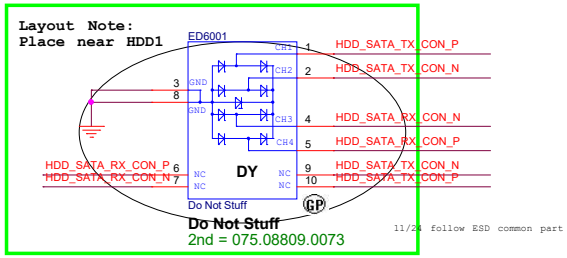
Date: Friday, July 13, 2018 Sheet 59 of 105

Main Func = HDD

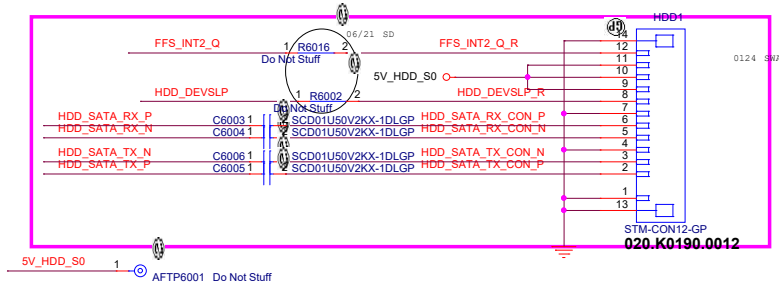
HDD

16 HDD_SATA_TX_P
16 HDD_SATA_TX_N
16 HDD_SATA_RX_P
16 HDD_SATA_RX_N
70 FFS_INT2_Q
16 HDD_DEVSLP

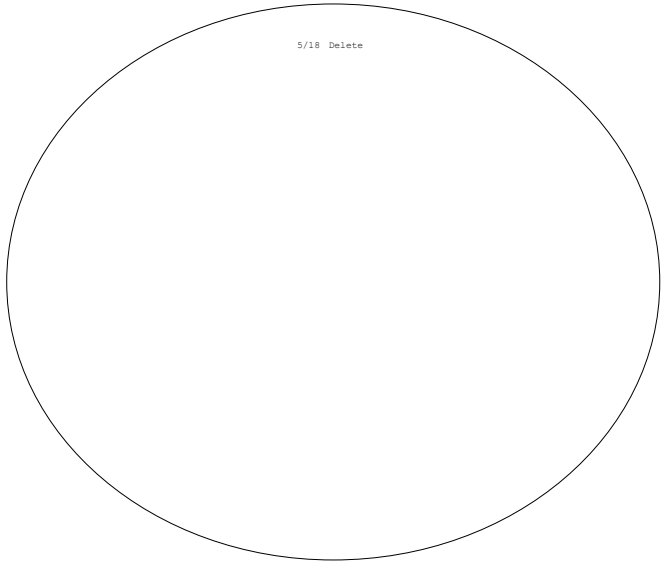




SATA HDD Connector



HDD Re- driver



BV UMA TC TPM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA IF HDD/ODD

Size	Document Number	Rev
Custom	Bucky WHL	SA

Date: Friday, July 13, 2018 Sheet 60 of 105

Main Func = WLAN

PCIE

16 WLAN_PCIE_TX_N
16 WLAN_PCIE_TX_P
16 WLAN_PCIE_RX_N
16 WLAN_PCIE_RX_P

PCIE_CLK

18 WLAN_CLK_CPU_N
18 WLAN_CLK_CPU_P
18,61 WLAN_CLKREQ_CPU_N

USB2.0

16 BT_USB20_P
16 BT_USB20_N

Single end

21 BLUETOOTH_EN
21 WIFI_RF_EN
17,26,63,66,76,91 PLT_RST#
18,24 SUS_CLK

Debug

24,68 HOST_DEBUG_TX

Power EN (Madesimo)

17,24 AUX_EN_WOWL

18,61 WLAN_CLKREQ_CPU_N

19 BT_PCMOUT_CLKREQ0
19 BT_PCMFRM_CRF_RST_N

21 CNV_WT_DN0
21 CNV_WT_DP0
21 CNV_WT_DN1
21 CNV_WT_DP1
21 CNV_WT_CLKN
21 CNV_WT_CLKP

21 CNV_WR_DN0
21 CNV_WR_DP0
21 CNV_WR_DN1
21 CNV_WR_DP1
21 CNV_WR_CLKN
21 CNV_WR_CLKP

15,20 CNV_RGI_DT_R
20 CNV_BRI_DT_R

20 CNV_BRI_RSP
20 CNV_RGI_RSP

18 JIO3_PCIE_WAKE#
18 CLKIN_XTAL_LCP_R

SC 0419

3D3V_S5
3D3V_S0
3D3V_WLAN
07/06 SD
R6140 1 2 Do Not Stuff
R6143 1 2 DY Do Not Stuff
1A
C6103 DY
R6137 Do Not Stuff
C6104 Do Not Stuff
Q6101 Do Not Stuff
Do Not Stuff
C6101 SCD1U16V2KX-3DLGP
FC6101 SC10P50V2JN-4DLGP
R6138 DY
WLAN_EN_R#
WLAN_EN#
R6136 3.3V_WLAN_EN Do Not Stuff DY
AUX_EN_WOWL
Q6102
Do Not Stuff
Do Not Stuff
2ND = 84.2N702.031
3rd = 84.07002.I31
DY

2017.10.25
Change Location
Connector list v8

Note:pin 76 and pin 77 need contact to GND

SB 0410

WLAN1
SKT-MINI67P-2-GP-U
62.10043.I91
NGFF_KEY_E_75P

76	76	77	77
74	3_3VAUX	GND	75
72	3_3VAUX	RESERVED#73	73
70	RESERVED#70	RESERVED#71	71
68	RESERVED#68	GND	69
66	RESERVED#66	RESERVED#67/2ND_LANE_PERN1	67
64	GPIO0_NFC_RESET#/MGPIO7	RESERVED#65/2ND_LANE_PERP1	65
62	NFC_I2C_IRQ/MGPIO5	GND	63
60	NFC_I2C_SM_CLK	RESERVED#61/2ND_LANE_PETN1	61
58	NFC_I2C_SM_DATA	RESERVED#59/2ND_LANE_PETP1	59
56	W_DISABLE#1	GND	57
54	RESERVED#54/W_DISABLE#2	PEWAKE0#	55
52	PERST0#	CLKREQ0#	53
50	SUSCLK_32KHZ	GND	51
48	COEX1	REFCLKN0	49
46	COEX2	REFCLKP0	47
44	COEX3	GND	45
42	CLINK_CLK	PERN0	43
40	CLINK_DATA	PERP0	41
38	CLINK_RESET	GND	39
36	UART_CTS	PETN0	37
34	UART_RTS	PETP0	35
32	UART_TX	GND	33
22	UART_RX	SDIO_RESET	23
20	UART_WAKE	SDIO_WAKE	21
18	GND	SDIO_DAT3	19
16	LED#2	SDIO_DAT2	17
14	PCM_OUT	SDIO_DAT1	15
12	PCM_IN	SDIO_DAT0	13
10	PCM_SYNC	SDIO_CMD	11
8	PCM_CLK	SDIO_CLK	9
6	LED#1	GND	7
4	3_3VAUX	USB_D-	5
2	3_3VAUX	USB_D+	3
		GND	1
NP2	NP2	NP1	NP1

3D3V_WLAN
3.3V
SUS_CLK R6135 33R2J-2-GP SUSCLK_WLAN
WIFI_RF_EN_R
BLUETOOTH_EN_R
PLT_RST#
CLKIN_XTAL_LCP_R
CNV_RGI_RSP R6109 22R2J-2-GP CNV_RGI_RSP_R CNV_RGI_DT_R
CNV_BRI_RSP R6118 22R2J-2-GP CNV_BRI_RSP_R
確認電阻 值
BT_PCMOUT_CLKREQ0
BT_PCMFRM_CRF_RST_N
R6134 75KR2F-GP 5/28 SC
R6133 DY Do Not Stuff

CNV_WT_CLKP_R R6130 Do Not Stuff CNV_WT_CLKP
CNV_WT_CLKN_R R6129 Do Not Stuff CNV_WT_CLKN
CNV_WT_DP0_R R6128 Do Not Stuff CNV_WT_DP0
CNV_WT_DN0_R R6127 Do Not Stuff CNV_WT_DN0
CNV_WT_DP1_R R6126 Do Not Stuff CNV_WT_DP1
CNV_WT_DN1_R R6125 Do Not Stuff CNV_WT_DN1
JIO3_PCIE_WAKE#_R R6105 Do Not Stuff JIO3_PCIE_WAKE#
WLAN_CLKREQ_CPU_N
06/21 SD
WLAN_CLK_CPU_N
WLAN_CLK_CPU_P
WLAN_PCIE_RX_N
WLAN_PCIE_RX_P
WLAN_PCIE_TX_CON_N C6107 SCD1U16V2KX-3DLGP WLAN_PCIE_TX_N
WLAN_PCIE_TX_CON_P C6108 SCD1U16V2KX-3DLGP WLAN_PCIE_TX_P
BT_USB20_CON_N
BT_USB20_CON_P

CNV_WR_CLKP_R R6124 Do Not Stuff CNV_WR_CLKP
CNV_WR_CLKN_R R6123 Do Not Stuff CNV_WR_CLKN
CNV_WR_DP0_R R6122 Do Not Stuff CNV_WR_DP0
CNV_WR_DN0_R R6121 Do Not Stuff CNV_WR_DN0
CNV_WR_DP1_R R6120 Do Not Stuff CNV_WR_DP1
CNV_WR_DN1_R R6119 Do Not Stuff CNV_WR_DN1
06/21 SD

BT_USB20_CON_P R6111 Do Not Stuff BT_USB20_P
5/21 Vincent
5/28 SC
BT_USB20_CON_N R6110 Do Not Stuff BT_USB20_N
06/21 SD

3D3V_WLAN
1.1A
C6110 SCD1U25V2KX-1-DL-GP
C6106 SC10U25V5KX-DL-GP
C6109 SCD1U25V2KX-1-DL-GP

Do Not Stuff AFTP6101 3D3V_WLAN
Do Not Stuff AFTP6105 WLAN_CLKREQ_CPU_N
Do Not Stuff AFTP6106 WIFI_RF_EN_R
Do Not Stuff AFTP6107 BLUETOOTH_EN_R
Do Not Stuff AFTP6108 PLT_RST#
Do Not Stuff AFTP6109 BT_USB20_CON_N
Do Not Stuff AFTP6110 BT_USB20_CON_P
Do Not Stuff AFTP6608 JIO3_PCIE_WAKE#

3D3V_WLAN
R6114 DY Do Not Stuff
WIFI_RF_EN
WIFI_RF_EN_R
R6142 DY Do Not Stuff
D6102 Do Not Stuff A
DY Do Not Stuff
2ND = 083.52030.008F

3D3V_WLAN
R6113 DY Do Not Stuff
BLUETOOTH_EN
BLUETOOTH_EN_R
R6102 DY Do Not Stuff
D6101 Do Not Stuff A
DY Do Not Stuff
2ND = 083.52030.008F

1D8V_S5
SB 0331
R6115 20KR2J-L2-GP CNV_BRI_DT_R

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Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF_WLAN CONN
Size: A3
Document Number: Bucky WHL
Rev: SA
Date: Friday, July 13, 2018
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(Blanking)

BV UMA TC TPM

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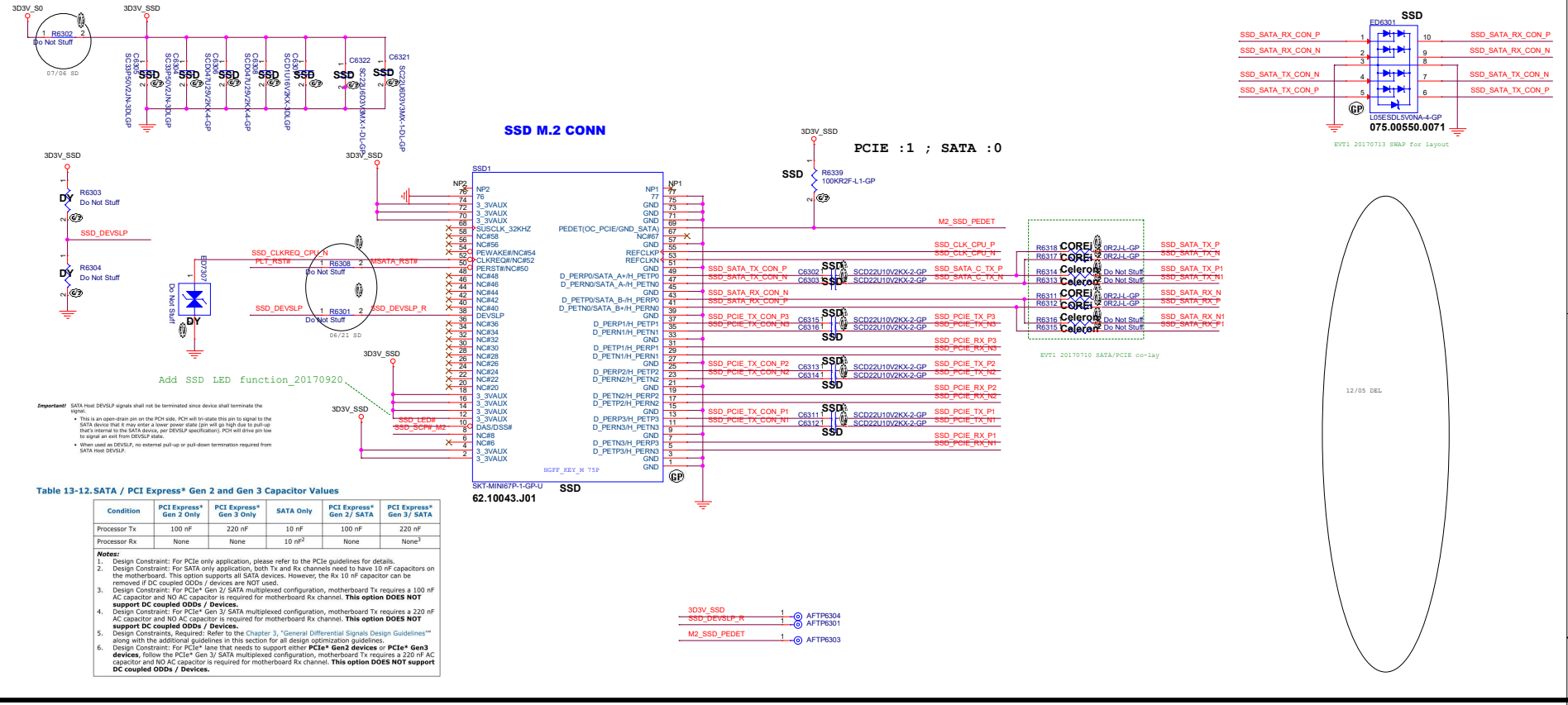
Title

Reserved

Size	Document Number	Rev
A4	***Bucky WHL***	***SA***

Date: Friday, July 13, 2018 Sheet 62 of 105

Main Func = M.2 SSD



Important! SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
- When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

Table 13-12. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

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Title	mSATA		
Size A2	Document Number Bucky WHL		Rev SA
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Main Func = Power BTN

24 LID_CL_SIO#
24,68 KBC_PWRBTN#
66 LID_CLOSE#_C
66 KBC_PWRBTN#_C

Low actived from KBC GPIO

For EMI Reserved
LID_CLOSE#_C EC6401 DY 2 Do Not Stuff

Power button

Layout note:
G6401 place to buttom
G6402 place to top

RN6401 SRN100J-3-GP
LID_CL_SIO# KBC_PWRBTN#
LID_CLOSE#_C KBC_PWRBTN#_C
EC6403 Do Not Stuff
ED6401
G6401 Do Not Stuff
G6402 Do Not Stuff
3D3V_S5
C6401 Do Not Stuff

Main Func = Battery LED

24 CHG_AMBER_LED#
24 SYS_LED_MASK#_R
24 BATT_WHITE_LED#

Low actived from KBC GPIO

CHG_AMBER_LED# R6405 Do Not Stuff CHG_AMBER_LED_R#
Q6403 RN2418-GP 084.02418.0011
5V_S5
AMBER_LED_BAT
R6407 499R2F-GP 07/06 SD
BAT_AMBER
EC6402 DY Do Not Stuff
5/25 SC
LED1 LED-YW-5-GP 083.1212A.0070
2ND = 083.00327.0070

MASK_BASE_LEDS#
Q6402 Do Not Stuff
Do Not Stuff
2nd = 075.00138.0F7C

BATT_WHITE_LED# R6404 Do Not Stuff BATT_WHITE_LED_R#
Q6404 RN2418-GP 084.02418.0011
WHITE_LED_BAT
R6406 549R2F-GP 07/09 SD
BAT_WHITE
EC6404 DY Do Not Stuff

Low actived from KBC GPIO

Battery LED1 (AMBER_LED)

Battery LED2 (WHITE_LED)

1D8V_S5
Q6402 Do Not Stuff
U6402
LID_CL_SIO#
SYS_LED_MASK#_R
MASK_BASE_LEDS#
Do Not Stuff
Do Not Stuff
73.7SZ08.DAH
73.01G08.DHG
R6419 Do Not Stuff

Main Func = HDD LED

24 MASK_SATA_LED#
16 SATA_LED#
63 SSD_LED#

SATA HDD LED
LOW actived from PCH GPIO

3D3V_S0
R6408 Do Not Stuff
R6402 Do Not Stuff
SATA_LED#
SSD_LED#
D6401 HWHDLED BAT54A-11-GP 75.BAT54.07D
Add SSD LED function_20170920

1D8V_S0
R6401 10KR2J-3-GP
HWHDLED
MASK_SATA_LED#
Q6401 HWHDLED PJA138KA-GP
SATA_LED#_D
BATT_WHITE_LED_R#
084.00138.0A31
2nd = 084.00138.0C31

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Board&Power Button
Size: A3
Document Number: Bucky WHL
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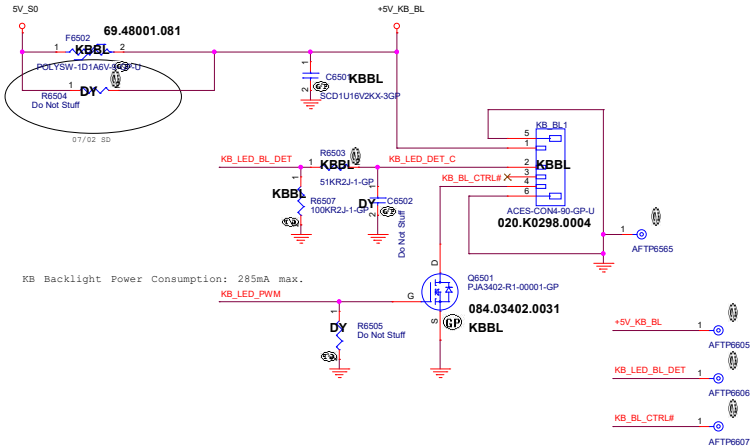
Date: Friday, July 13, 2018
Sheet 64 of 105

Main Func = KB

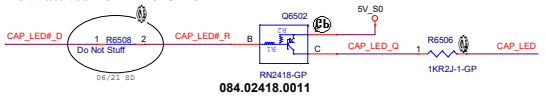
24 CAP_LED#_D
24 KSI[0..7]
24 KSO[0..16]
20 KB_DET#
19 KB_LED_BL_DET
24 KB_LED_PWM

Keyboard Backlight (Reserved)

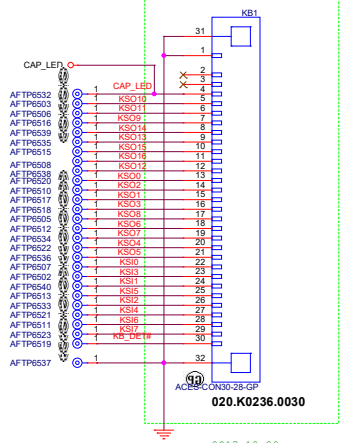


CAP LED Control

LOW actived from KBC GPIO



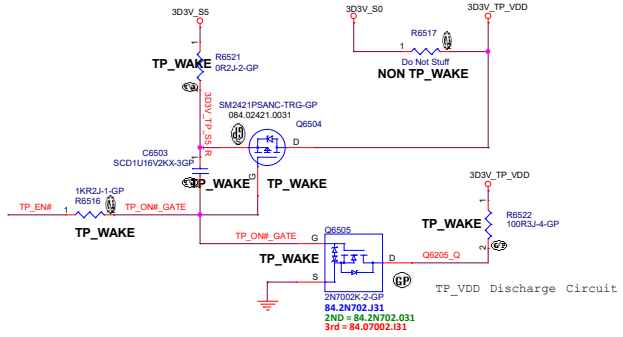
Internal Keyboard Connector



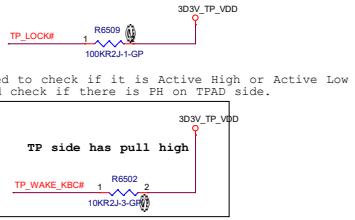
2017.10.20
Change P/N
Connector list

Main Func = TPAD

24 TP_EN#



TP_VDD Discharge Circuit



Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

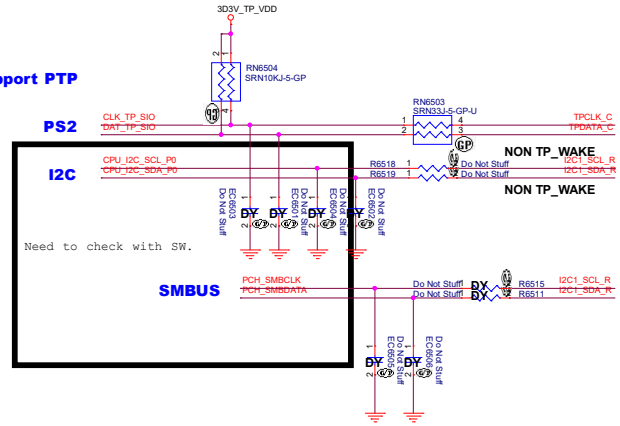
24 CLK_TP_SIO
24 DAT_TP_SIO
20 CPU_I2C_SCL_P0
20 CPU_I2C_SDA_P0
12,13,18 PCH_SMBCLK
12,13,18 PCH_SMBDATA
3,24 TP_WAKE_KBC#
24 TP_LOCK#

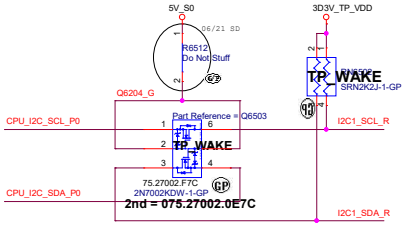
Support PTP

PS2

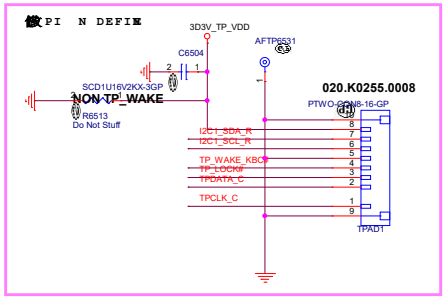
I2C

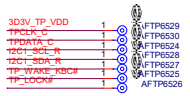
SMBUS





Precision Touch Pad Connector





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Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board&Touch Pad

Size: A2 | Document Number: Bucky WHL | Rev: SA

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Main Func = IO Connector

USB2.0

16 USB3_USB20_N
16 USB3_USB20_P

Card Reder

16 CARD1_USB20_N
16 CARD1_USB20_P

LAN

16 LAN_PCIE_RX_N
16 LAN_PCIE_RX_P
16 LAN_PCIE_TX_N
16 LAN_PCIE_TX_P
18 LAN_CLK_CPU_N
18 LAN_CLK_CPU_P
18 LAN_CLKREQ_CPU_N Edison 11/13 for STU
24 PM_LAN_ENABLE
24 LANWAKE#_IC

FP

16 FP_USB20_N
16 FP_USB20_P
24 FPR_SCAN#

Free Fall Sensor

20,66,70 SENSOR_I2C_SCL
20,66,70 SENSOR_I2C_SDA
70 SENSOR_I2C_SCL_2G
70 SENSOR_I2C_SDA_2G
20 GSEN_INT1
20 GSEN_INT2
70 GSEN2_INT1
70 GSEN2_INT2

17,26,61,63,76,91 PLT_RST#

20,66,70 SENSOR_I2C_SDA
20,66,70 SENSOR_I2C_SCL

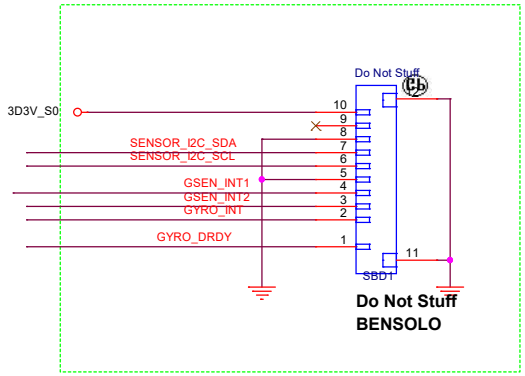
70 GYRO_INT
20 GYRO_DRDY

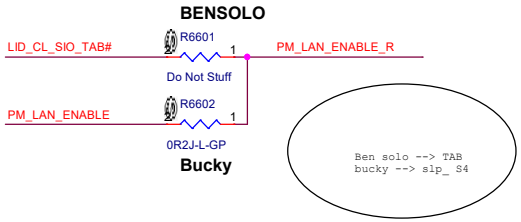
24 LID_CL_SIO_TAB#
64 LID_CLOSE#_C
64 KBC_PWRBTN#_C

17,40,51,68 PM_SLP_S4#

Sensor Board Connector

2017.10.20
Change P/N
Connector list





I/O Board Connector

Pitch: 1mm
Power:6 pins
GND: 5 pins

Wire

FP

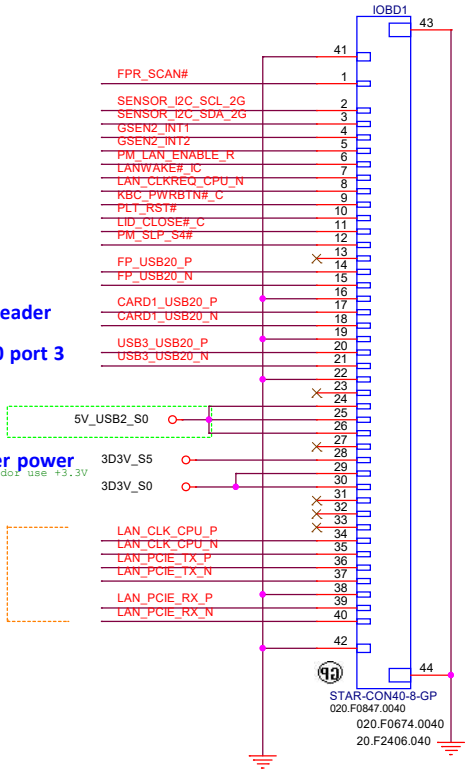
Card Reader

USB2.0 port 3

2017.10.25
Modify netname
follow STD

FP /Card Reder power
EVT1 20170628 FP vendor use +3.3V

Coaxial



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Title: IO Board Connector
Size: A3
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Title: Free Fall Sensor

Size: A3 | Document Number: Bucky WHL | Rev: SA

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Main Func = Debug

ESPI

18,24 ESPI_CLK
18,24 ESPI_RESET#
18,24 ESPI_CS#
18,24 ESPI_IO[3..0]
ESPI_IO3
ESPI_IO2
ESPI_IO1
ESPI_IO0

UART

24 HOST_DEBUG_TX
20 UART_2_CTXD_DRXD
20 UART_2_CRXD_DTXD

APS

18 RTC_RST#
24,64 KBC_PWRBTN#
17,27,40 PM_SLP_S3#
17 PM_SLP_S5#
17,40,51,66 PM_SLP_S4#
17 SIO_SLP_A#
17,24,40,91 PM_SLP_S0#
17 XDP_DBRESET#

ESPI Debug Connector

Modify_21070802

3D3V_S0

HOST_DEBUG_TX — R6801 1 — 2 Do Not Stuff — HOST_DEBUG_TX_CON
UART_2_CTXD_DRXD — R6802 1 — 2 Do Not Stuff — UART_2_CTXD_DRXD_CON
UART_2_CRXD_DTXD — R6803 1 — 2 Do Not Stuff — UART_2_CRXD_DTXD_CON
DY
DEBUG
DEBUG

DBG1
ESPI_CLK
ESPI_RESET#
ESPI_CS#
ESPI_IO3
ESPI_IO2
ESPI_IO1
ESPI_IO0
DEBUG
Do Not Stuff
Do Not Stuff

PM_SLP_S3# 1 TP9952 Do Not Stuff
PM_SLP_S5# 1 TP9949 Do Not Stuff
PM_SLP_S4# 1 TP9950 Do Not Stuff
SIO_SLP_A# 1 TP9951 Do Not Stuff
RTC_RST# 1 TP9953 Do Not Stuff
KBC_PWRBTN# 1 TP9954 Do Not Stuff
PM_SLP_S0# 1 TP9956 Do Not Stuff
XDP_DBRESET# 1 TP9955 Do Not Stuff

EC6801
1
2
DY
Do Not Stuff

BV UMA TC TPM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Dubug connector*

Size	Document Number	Rev
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Title

Reserved

Size	Document Number	Rev
A4	***Bucky WHL***	***SA***

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SSID = User.interface

Free Fall Sensor

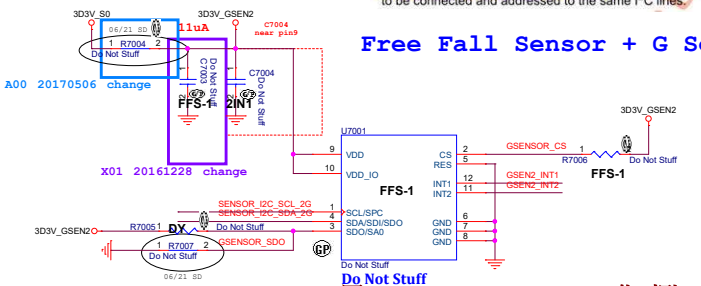
ref KR13_20170801

Reserve FFS-1

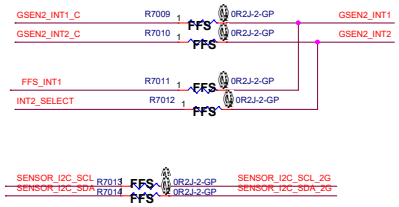
66 GSEN2_INT1
66 GSEN2_INT2
20 GSEN2_INT1_C
20 GSEN2_INT2_C
18 FFS_INT1
20,66 SENSOR_I2C_SCL
20,66 SENSOR_I2C_SDA
66 SENSOR_I2C_SCL_2G
66 SENSOR_I2C_SDA_2G
20 GYRO_INT_C
20 FFS_INT2
66 GYRO_INT
60 FFS_INT2_Q

The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

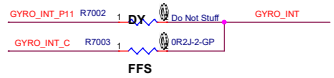
Free Fall Sensor + G Sensor

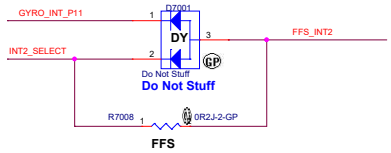


因free fall sesonr 在板上,所以 B -1在FFS 有在benso lo &2 i 會上件



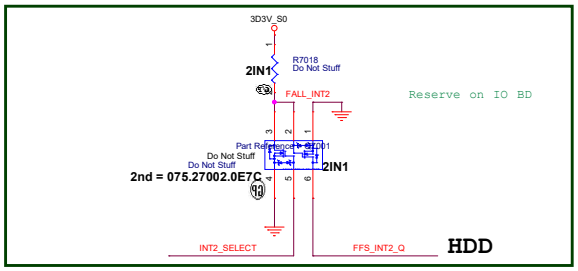
combine G





Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

BV UMA TC TPM

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Title: Free Fall Sensor

Size	Document Number	Rev
A2	Bucky WHL	SA

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BV UMA TC TPM

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Title

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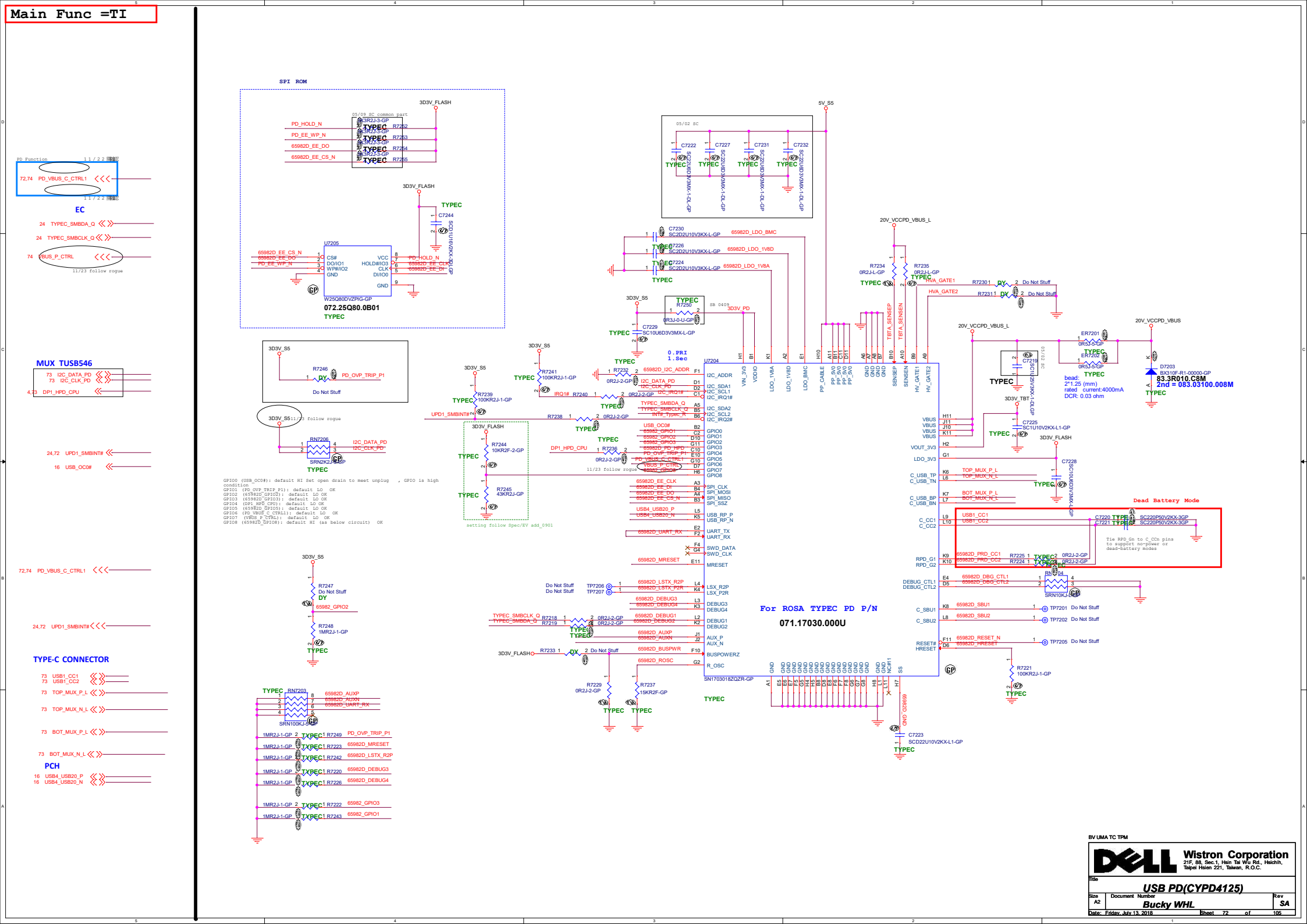
Size	Document Number	Rev
A4	Bucky WHL	SA

Date: Friday, July 13, 2018 Sheet 71 of 105

Main Func =TI


SPI ROM
3D3V_FLASH
PD_HOLD_N
PD_EE_WP_N
65982D_EE_DO
65982D_EE_CS_N
R7252
R7253
R7254
R7255
U7205
W25Q80DVZPIG-GP
072.25Q80.0B01
TYPEC
EC
24 TYPEC_SMBDA_Q
24 TYPEC_SMBCLK_Q
74 VBUS_P_CTRL
MUX TUSB546
73 I2C_DATA_PD
73 I2C_CLK_PD
4,73 DP1_HPD_CPU
24,72 UPD1_SMBINT#
16 USB_OC0#
72,74 PD_VBUS_C_CTRL1
TYPE-C CONNECTOR
73 USB1_CC1
73 USB1_CC2
73 TOP_MUX_P_L
73 TOP_MUX_N_L
73 BOT_MUX_P_L
73 BOT_MUX_N_L
PCH
16 USB4_USB20_P
16 USB4_USB20_N
5V_S5
20V_VCCPD_VBUS_L
20V_VCCPD_VBUS
U7204
SN170318ZQZR-GP
0.PRI
1.Sec
bead:
2*1.25 (mm)
rated current:4000mA
DCR: 0.03 ohm
83.3R010.C8M
2nd = 083.03100.008M
Dead Battery Mode
For ROSA TYPEC PD P/N
071.17030.000U
BV UMA TC TPM
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USB PD(CYPD4125)
Bucky WHL
Rev SA
Date: Friday, July 13, 2018
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Main Func = TYPEC MUX

DisplayPort Source

- 4 DP2_DDI_TX_P0
- 4 DP2_DDI_TX_N0
- 4 DP2_DDI_TX_P1
- 4 DP2_DDI_TX_N1
- 4 DP2_DDI_TX_P2
- 4 DP2_DDI_TX_N2
- 4 DP2_DDI_TX_P3
- 4 DP2_DDI_TX_N3

USB HOST

- 16 USB4_USB30_RX_P
- 16 USB4_USB30_RX_N
- 16 USB4_USB30_TX_P
- 16 USB4_USB30_TX_N

DisplayPort AUX

- 4 DP2_AUX_CPU_P
- 4 DP2_AUX_CPU_N

MUX I2C

- 72 I2C_CLK_PD
- 72 I2C_DATA_PD

DisplayPort HPD

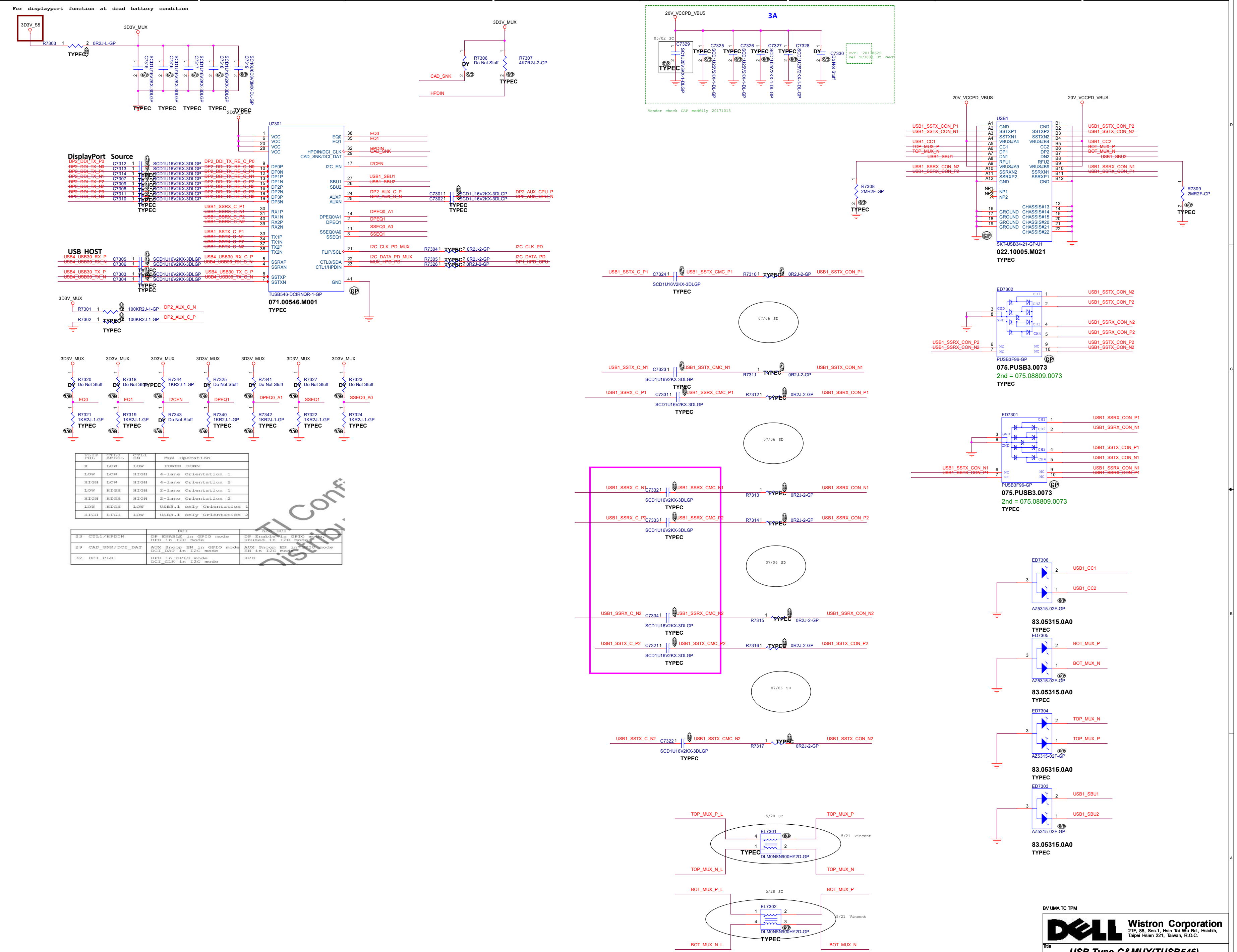
- 4,72 DP1_HPD_CPU

I2C/USB MUX

TypeC CC

- 72 USB1_CC1
- 72 USB1_CC2
- 72 TOP_MUX_P_L
- 72 TOP_MUX_N_L
- 72 BOT_MUX_P_L
- 72 BOT_MUX_N_L

For displayport function at dead battery condition



FLIP POL	CTL0 AMSEL	CTL1 EN	Mux Operation
X	LOW	LOW	POWER DOWN
LOW	LOW	HIGH	4-lane Orientation 1
HIGH	LOW	HIGH	4-lane Orientation 2
LOW	HIGH	HIGH	2-lane Orientation 1
HIGH	HIGH	HIGH	2-lane Orientation 2
LOW	HIGH	LOW	USB3.1 only Orientation 1
HIGH	HIGH	LOW	USB3.1 only Orientation 2

	DCI	non-DCI
23 CTL1/HPDIN	DP ENABLE in GPIO mode HPD in I2C mode	DP Enable in GPIO mode, Unused in I2C mode
29 CAD_SNK/DCI_DAT	AUX Snoop EN in GPIO mode DCI_DAT in I2C mode	AUX Snoop EN in GPIO mode EN in I2C mode
32 DCI_CLK	HPD in GPIO mode DCI_CLK in I2C mode	HPD

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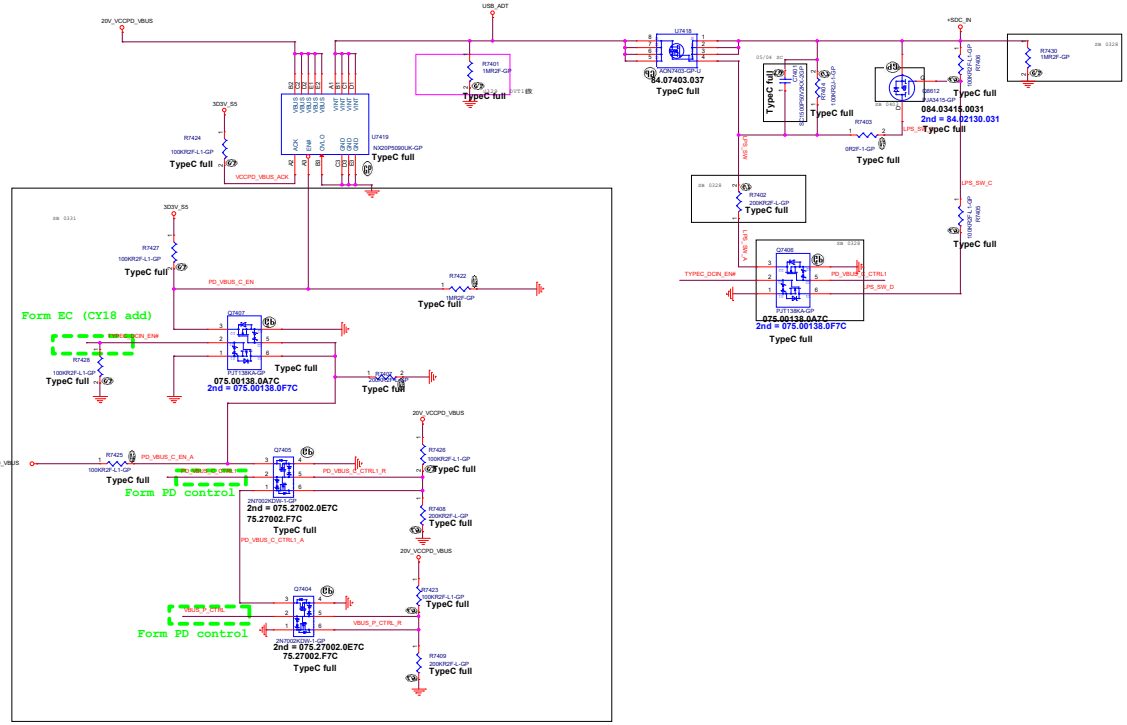
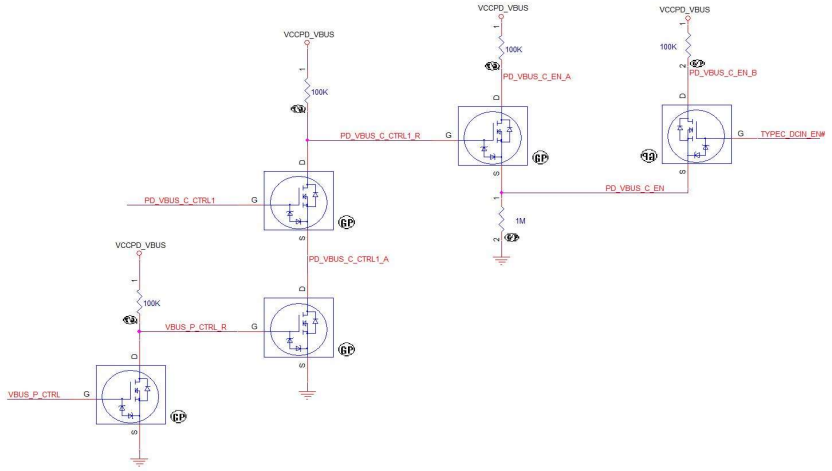
Title: USB Type-C&MUX(TUSB546)

Size: Custom | Document Number: Bucky WHL | Rev: SA

Date: Friday, July 13, 2018 |

72 PD_VBUS_C_CTRL1
72 VBUS_P_CTRL
24 TYPEC_DCIN_EN#
44 VCCPD_VBUS_ACK





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Title: GPU(2/5)DIGITALOUT

Size	Document Number	Rev
A1	Bucky WHL	SA

Date: Friday, July 13, 2018 Sheet 74 of 105

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Title: *Reserved*

Size: A3 | Document Number: *Bucky WHL* | Rev: *SA*

Date: Friday, July 13, 2018 | Sheet 75 of 105

Main Func = dGPU

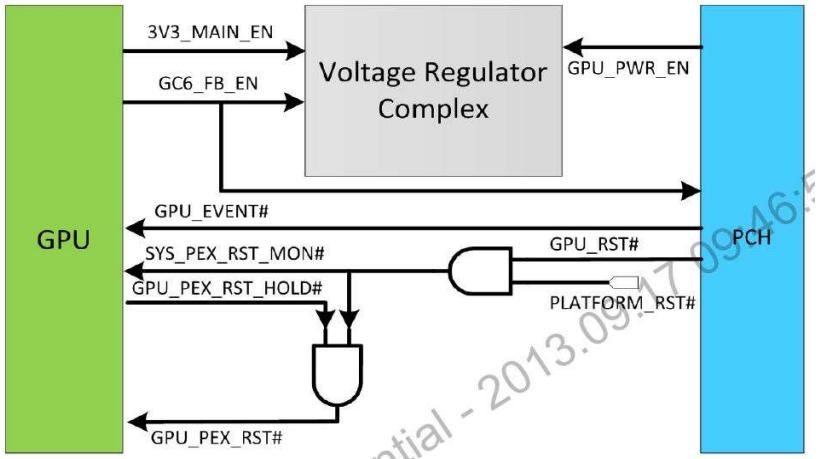

Figure 18-11. GC6 2.0 High-level Signal Connection Concept

dGPU Reset

POWER IC

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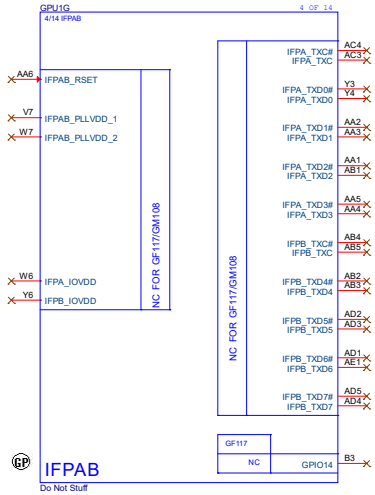
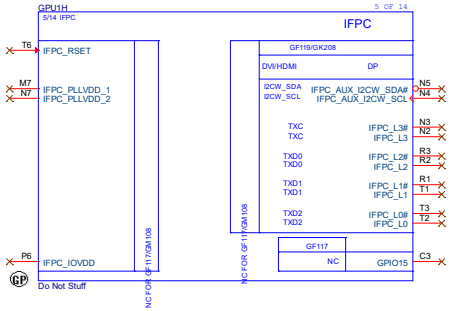
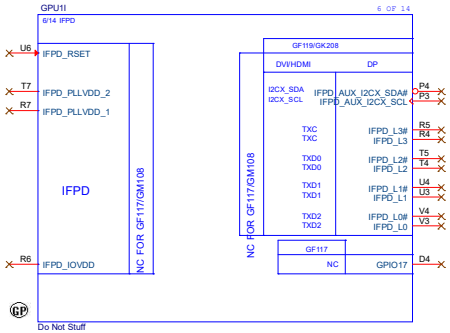
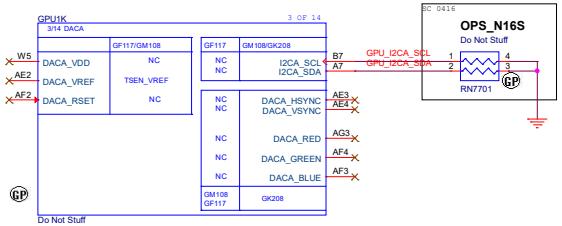
Title	GPU(1/5)PEG	
Size A2	Document Number: Bucky WHL	Rev SA
Date: Friday, July 13, 2018	Sheet 76 of 105	

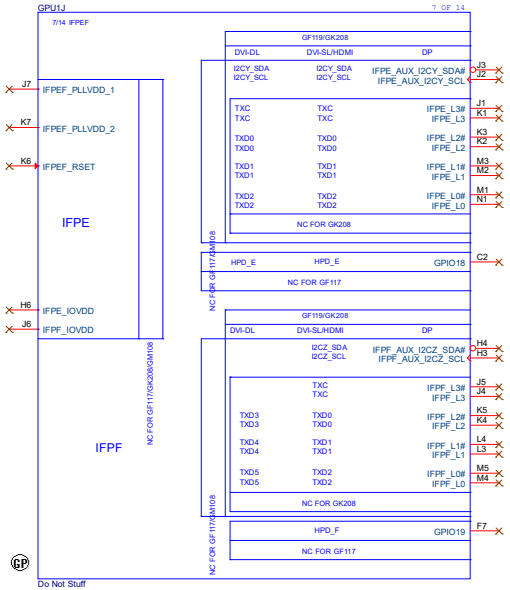
Main Func = dGPU











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Title: *GPU(2/5)DIGITALOUT*

Size: A2 | Document Number: Bucky WHL | Rev: SA

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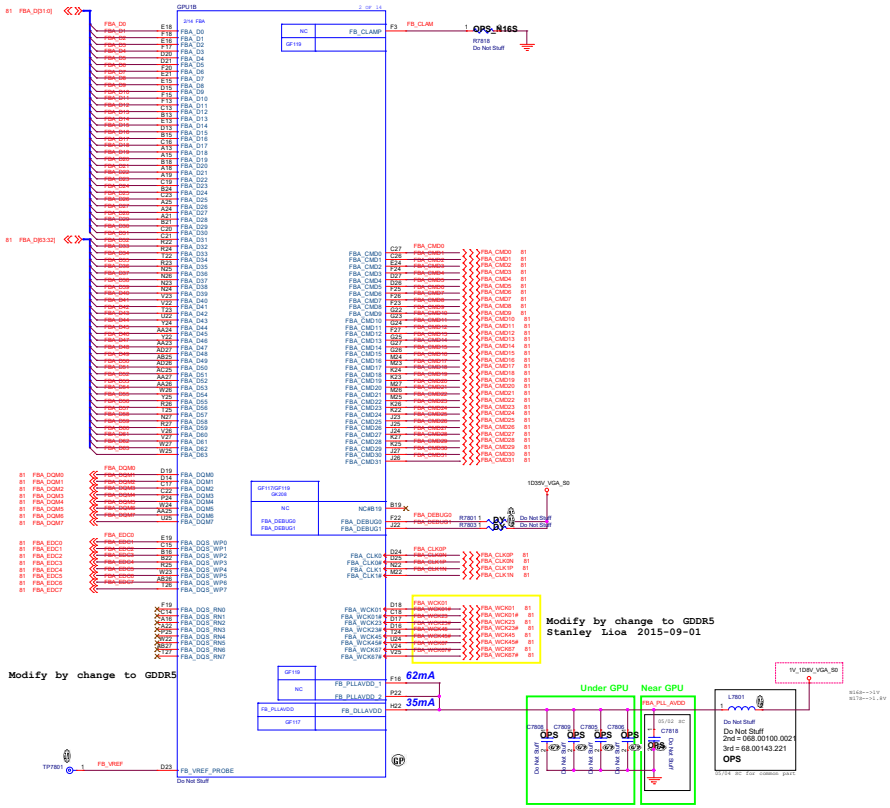
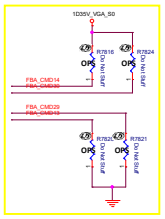
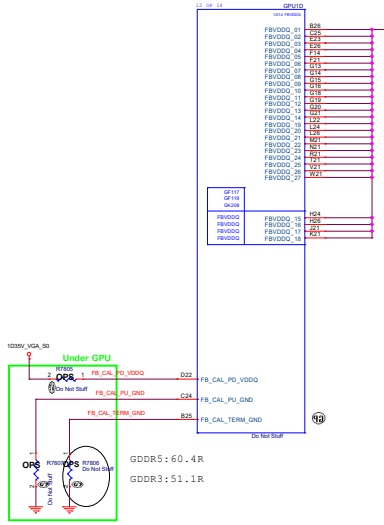
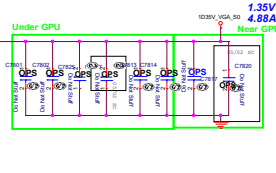
Main Func = dGPU





Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5





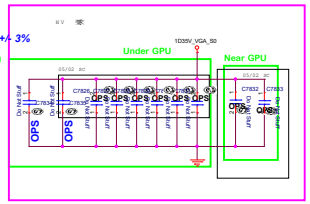


Table 3-10. GDDR5 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type	Footprint		Population	Location
GB2B-64/ GB2-64 GDDR5	0.1 µF	X7R	0402	2	Under GPU
	1 µF	X7R	0603	2	Under GPU
	4.7 µF	X6S	0603	2	Under GPU
	10 µF	X5R	0805	1	Near GPU
	22 µF	X5R	0805	1	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

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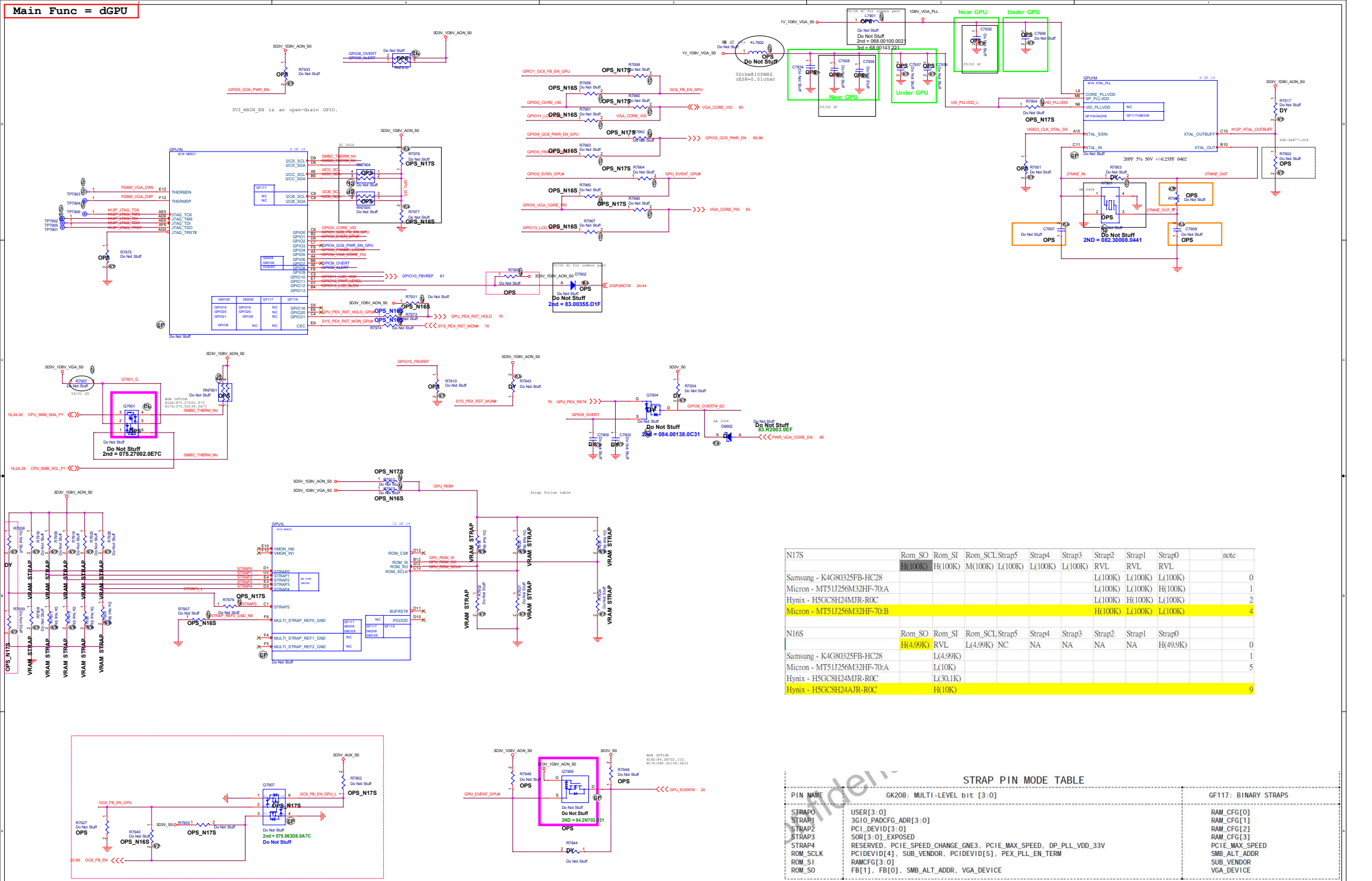
GPU(3/5)VRAM/F

Bucky WHL

Rev SA

Friday, July 13, 2018

Main Func = dGPU



N17S	Rom_SO	Rom_SI	Rom_SCL	Strap5	Strap4	Strap3	Strap2	Strap1	Strap0		note
	H(100K)	H(100K)	M(100K)	L(100K)	L(100K)	L(100K)	RVL	RVL	RVL		
Samsung - K4G80325FB-HC28							L(100K)	L(100K)	L(100K)		0
Micron - MT51J256M32HF-70:A							L(100K)	L(100K)	H(100K)		1
Hynix - H5GC8H24MJR-R0C							L(100K)	H(100K)	L(100K)		2
Micron - MT51J256M32HF-70:B							H(100K)	L(100K)	L(100K)		4
N16S	Rom_SO	Rom_SI	Rom_SCL	Strap5	Strap4	Strap3	Strap2	Strap1	Strap0		
	H(4.99K)	RVL	L(4.99K)	NC	NA	NA	NA	NA	H(49.9K)		0
Samsung - K4G80325FB-HC28		L(4.99K)									1
Micron - MT51J256M32HF-70:A		L(10K)									5
Hynix - H5GC8H24AJR-R0C		H(10K)									9

STRAP PIN MODE TABLE

PIN NAME	GK208: MULTI-LEVEL bit [3:0]	GF117: BINARY STRAPS
STRAP0	USER[3:0]	RAM_CFG[0]
STRAP1	3GIO_PADCFG_ADR[3:0]	RAM_CFG[1]
STRAP2	PCI_DEVID[3:0]	RAM_CFG[2]
STRAP3	SOR[3:0]_EXPOSED	RAM_CFG[3]
STRAP4	RESERVED, PCIE_SPEED_CHANGE_GNE3, PCIE_MAX_SPEED, DP_PLL_VDD_33V	PCIE_MAX_SPEED
ROM_SCLK	PCIDEVID[4], SUB_VENDOR, PCIDEVID[5], PEX_PLL_EN_TERM	SMB_ALT_ADDR
ROM_SI	RAMCFG[3:0]	SUB_VENDOR
ROM_SO	FB[1], FB[0], SMB_ALT_ADDR, VGA_DEVICE	VGA_DEVICE

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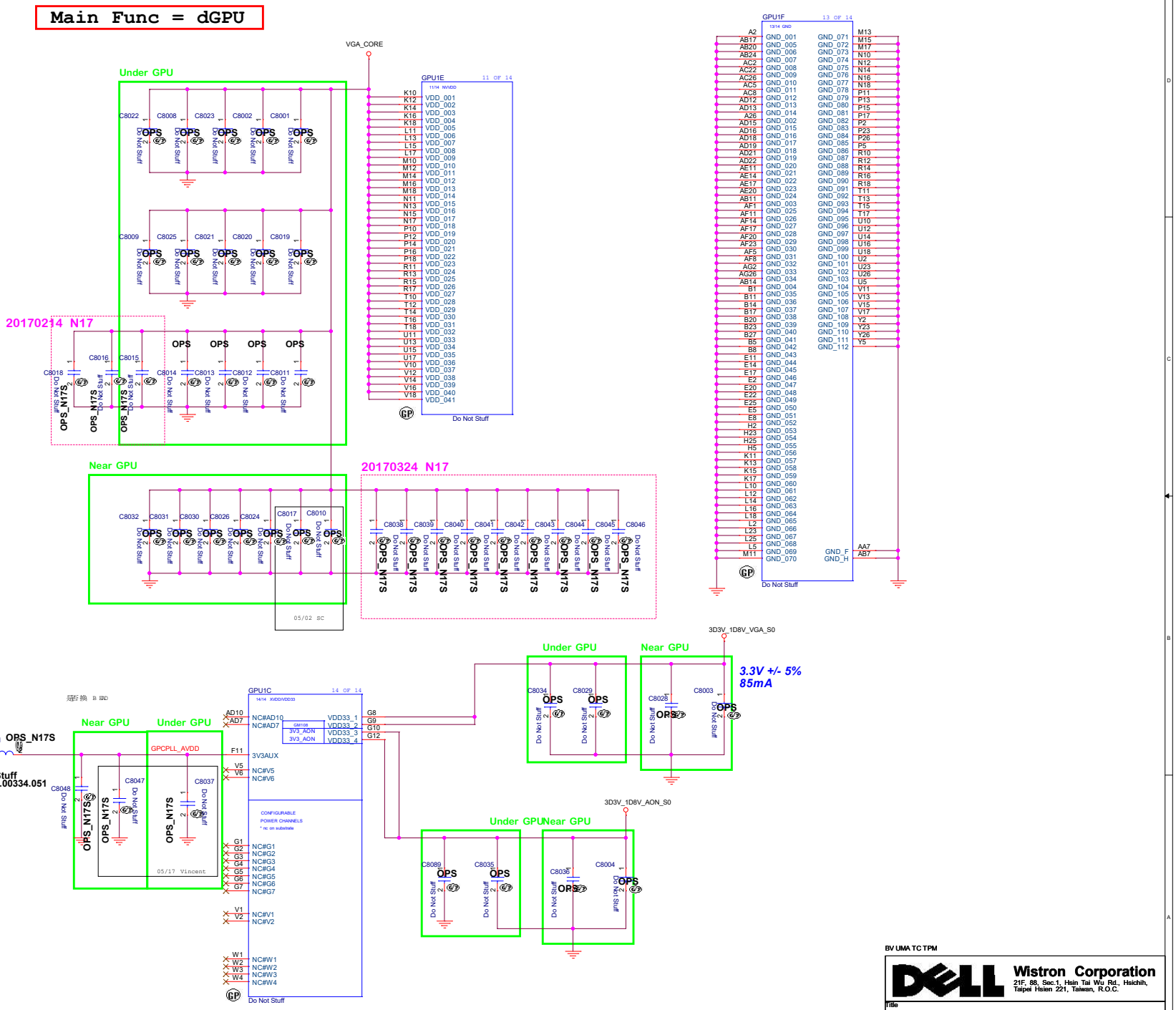
Title: GPU(4/5)GPIO/STRAP

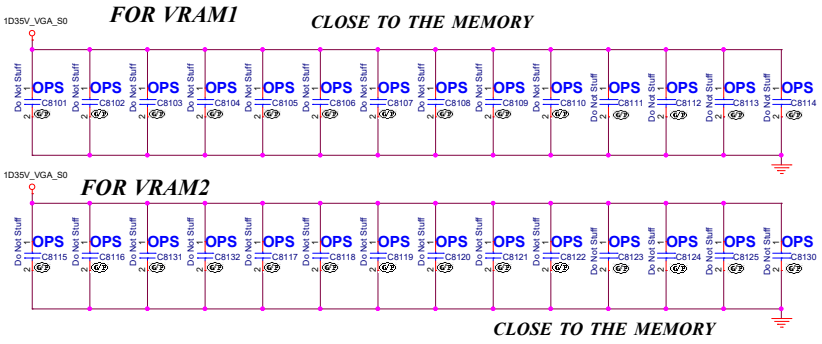
Size	Document Number	Rev
Custom	Bucky WHL	SA

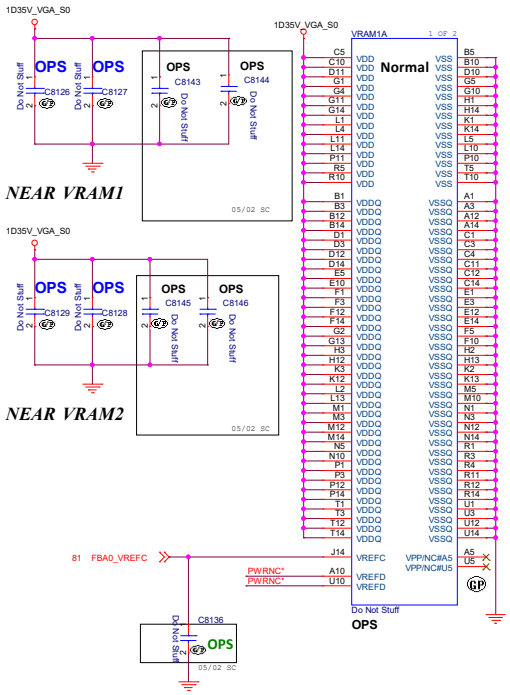
Date: Friday, July 13, 2012 Sheet 79 of 105

Main Func = dGPU



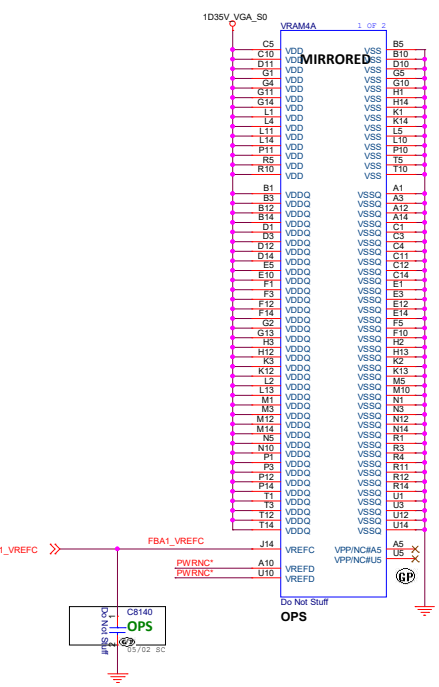
SSID = VRAM





Place close VDD ball

Place close VDD ball



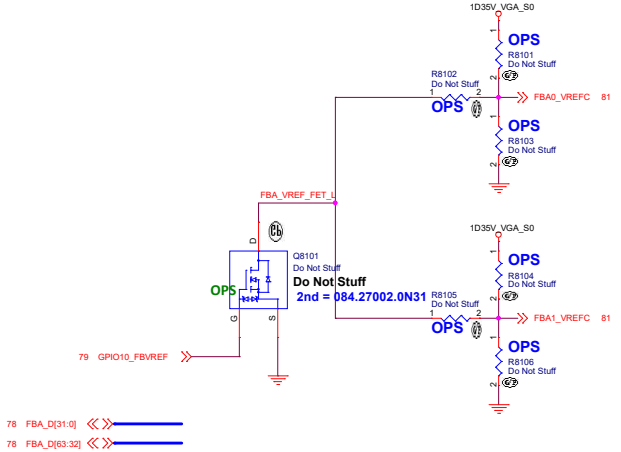
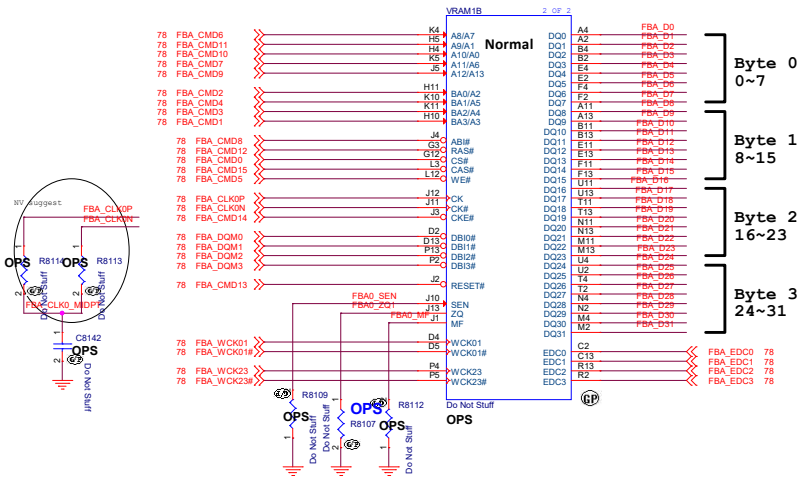
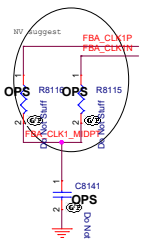
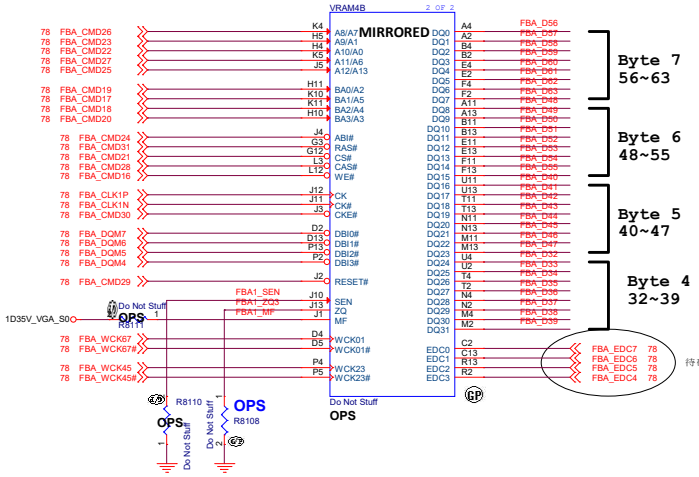


TABLE
GDDR5 VIDEO MEMORY 072.05424.0A0U 072.44132.000U 072.04032.000N

	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)	Micron 4GBITS (128Mx32)
VRAM1 VRAM2	H5GC4H24AJR-T2C	K4G41325FC-HC03	EDW4032BABG-60-F-D







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Title: GPU-VRAM1,2 (1/4)

Size: A2 | Document Number: Bucky WHL | Rev: SA

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SSID = VRAM

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Title: GPU-VRAM3,4 (2/4)

Size: A2 | Document Number: Bucky WHL | Rev: SA

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Main Func = dGPU

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Title: *GPU-VRAM5,6 (3/4)*

Size	Document Number	Rev
A3	Bucky WHL	SA

Date: Friday, July 13, 2018 Sheet 83 of 105

Main Func = dGPU

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Title: GPU-VRAM7,8 (4/4)

Size: A3 | Document Number: Bucky WHL | Rev: SA

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Main Func = dGFX_CORE

need EE Check

N16
EDP=27.2A Peak=53A

N17
EDP=30A Peak=60.1A

For tuning VGA_CORE sequence.

20161223 N17

Item	Location	N16		N17	
1	PU8514	RT8812AGQW	74.08812.073	RT8816AGQW	074.08816.0A73
2	PR8511	20K	64.20025.6DL	6.19K	64.61915.6DL
3	PR8510	20K	64.20025.6DL	20.5K	64.20525.6DL
4	PR8512	2K	64.20015.6DL	4.32k	64.43215.6DL
5	PR8514	18K	64.18025.6DL	16.5K	64.16525.6DL
6	PR8561	0R	63.R0034.1DL	309R	64.30905.6DL
7	PC8519	2700p	78.27224.2FLDL	4700p	078.47222.02FD
8	PR8525	0R	63.R0034.1DL	DY	
9	PR8526	0R	63.R0034.1DL	DY	
10	PR8527	DY		0R	63.R0034.1DL
11	PR8576	DY		0R	63.R0034.1DL
12	PR8577	DY		160K	64.16035.6DL
13	PR8508	15.4K	64.15425.6DL	DY	
14	PR8504	348K	64.34835.6DL	499K	64.49935.6DL

N17 OCP
OCP setting (current limit ~ 60.3A)

N16 OCP
OCP setting (current limit ~ 60.3A)

SoftStar

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Title: VGA_CORE
Size: M | Document Number: Bucky WSL | Rev: SA
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need EE Check

PARAMETER	MIN	MAX	UNITS
VIN1,2 Input voltage range	0.8	V_{BIAS}	V
VBIAS Bias voltage range	2.5	5.5	V
EN1,2 ON voltage range	0	5.5	V
VOUT1,2 Output voltage range	---	VIN1,2	V
VIH High-level input voltage, EN1, EN2	1.2	5.5	V
VIL Low-level input voltage, EN1, EN2	---	0.5	V
CT1,2 Input Capacitor	1	---	µF

Main Func = dGPU

G5516 for 1.8V_AON_S0

Main Func = dGPU

預留先擺位置

3D3V_S0 to 3V3_AON_S0 and 3D3V_VGA_S0

3D3V_VGA_S0

3V3_AON_S0

dGPU Power Discharge Circuit

1V_VGA_S0

VGA_CORE

1D35V_VGA_S0

1D8V_AON_S0

1D8V_VGA_S0

1D8V_AON_S0 to 1D8V_VGA_S0

RT5797 for 1V_VGA_S0

1V_VGA_S0

Imax=200mA

1D35V_VGA_S0

SY8288RAC for 1D35V

Imax=4.8A
OCP>7.2A

OCP setting	
High	10A
Float	12.4
Low	8A

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DISCRETE VGA POWER	
Bucky WH	-2

Main Func = dGPU

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Title: *Reserved*

Size	Document Number	Rev
A3	*Bucky WHL*	*SA*

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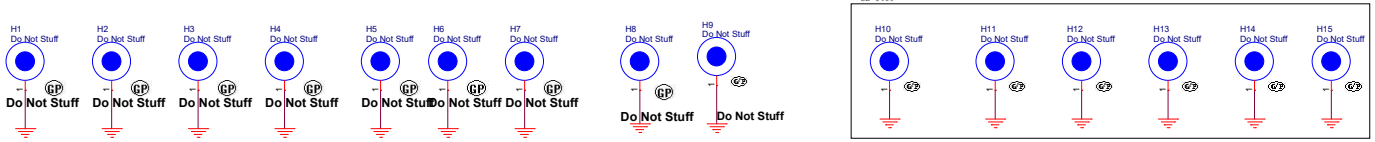
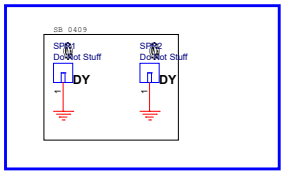
Title

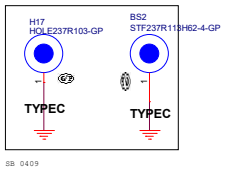
Reserved

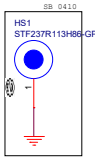
Size	Document Number	Rev
A4	Bucky WHL	SA

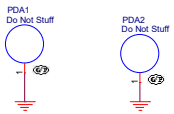
Main Func = UnusedParts







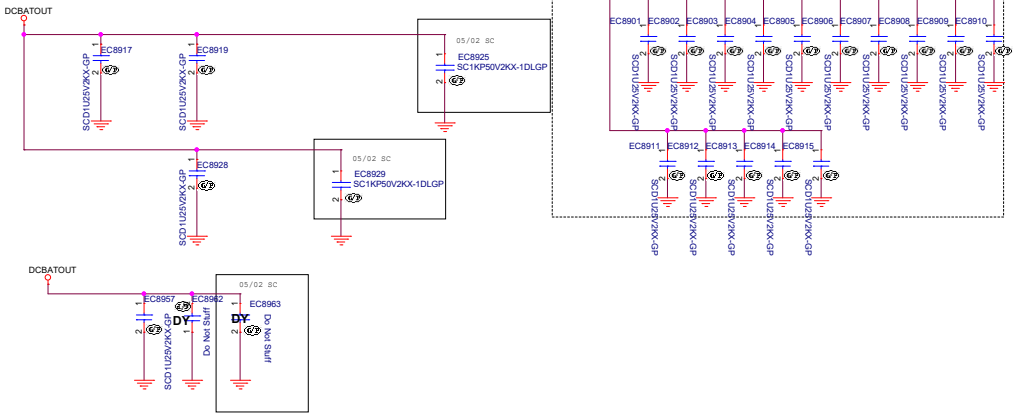


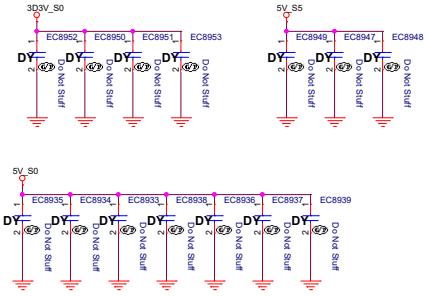


For acoustic noice

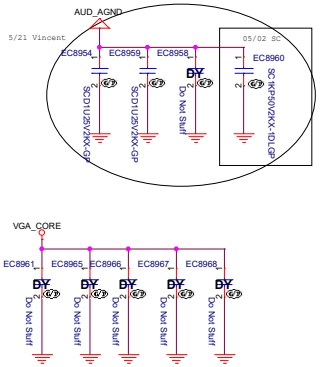
Main Func = EMI Capacitors

Mind the voltage rating of the caps.





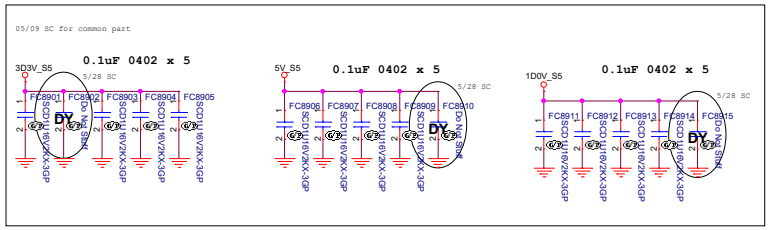
remove 1D5V_VGA_S0 EC CAP_21070719

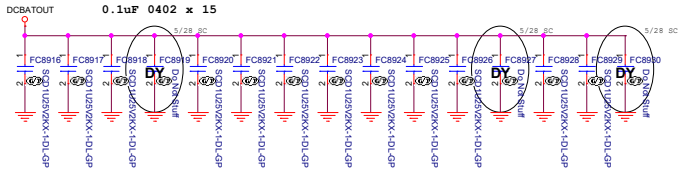


Main Func = RF Capacitors

For RF solution RFQ 2017/08/11

Mind the voltage rating of the caps.





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Title: UNUSED PARTS/EMI Capacitors

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A2	Bucky WHL	SA

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Title

Reserved

Size	Document Number	Rev
A4	Bucky WHL	SA

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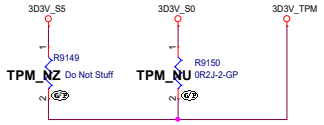
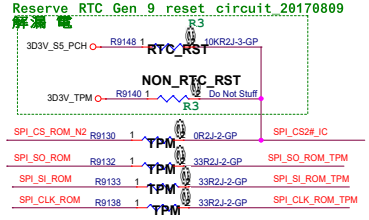
SSID = TPM

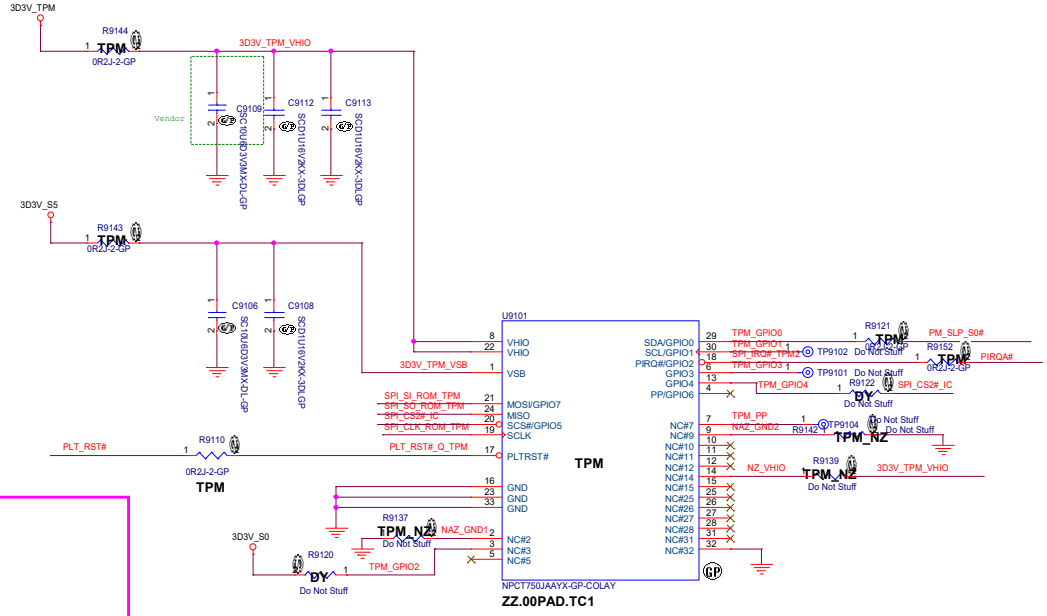
Change to use co-lay TP750X & Z32H330 follow DT porject_20170921

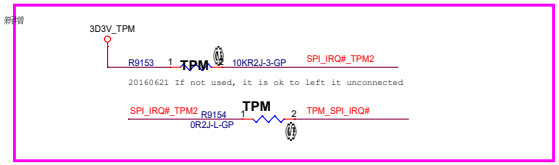
18,25 SPI_SO_ROM
15,18,25 SPI_SI_ROM
18,25 SPI_CLK_ROM
18 SPI_CS_ROM_N2
17,26,61,63,66,76 PLT_RST#
20 PIRQA#
18 TPM_SPI_IRQ#
17,24,40,68 PM_SLP_S0#



Reserve RTC Gen 9 reset circuit 20170809
保留電







NU: Nuvoton TPM :071.00750.0003

NZ: NationZ TPM :071.32330.0003

TPM _ID at P.19

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Title: TPM2.0

Size: Custom | Document Number: Bucky WHL | Rev: SA

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SSID = Finger Print

PWFPR(Botton side finger Print Sensor)

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Title: Finger Print

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Title: *LVDS_Switch*

Size	Document Number	Rev
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Main Func = Firmware SW

ME_FWP — 1 R9806 2 — ME_FWP_SW
Do Not Stuff
NON_MESW
INSTALL after MP
06/21 SD

add 0 ohm
20161122(X1)

Firmware SW

19 ME_FWP_SW >>>
24 ME_FWP <<<

Default setting:pull LOW
DY for MP

05/15 SC

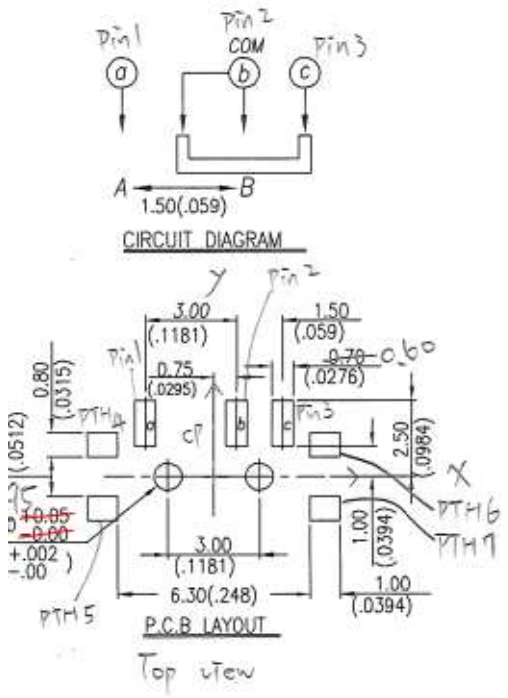
FSW1 change from 62.40018.691 to 62.40018.641
20160623(DVT1)

	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

modify 20161122(X1)

modify 20161122(X1)

*Symbol same as 62.40018.461.



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Title: *Firmware SW*

Size	Document Number	Rev
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Main Func = Debug

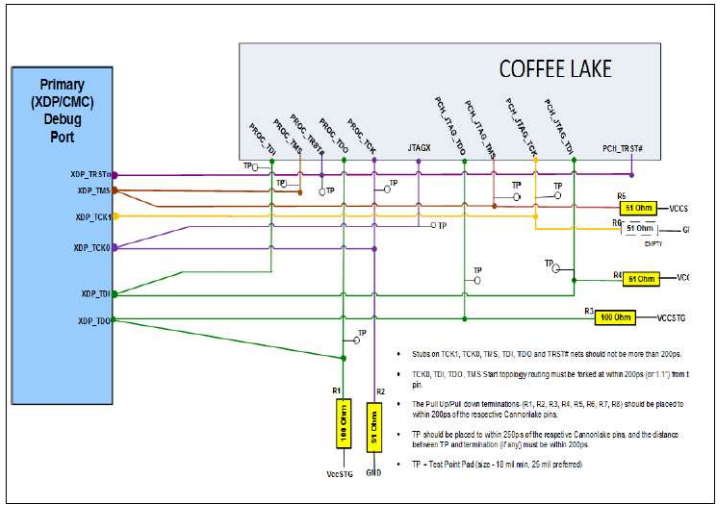
3 XDP_TCLK
3 XDP_TDO_CPU
3 XDP_TDI
3 XDP_TMS
3 XDP_TCK_JTAGX
3 PCH_JTAG_TDO
3 PCH_JTAG_TDI
3 PCH_JTAG_TMS

(#544669)

確認是否需要串接形成迴路

XDP_TCLK	R9996 1	XDP	Do Not Stuff	XDP_TCK_JTAGX
XDP_TDO_CPU	R9994 1	XDP	Do Not Stuff	PCH_JTAG_TDO
XDP_TDI	R9995 1	XDP	Do Not Stuff	PCH_JTAG_TDI
XDP_TMS	R9992 1	XDP	Do Not Stuff	PCH_JTAG_TMS

modify 20160628



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Title: CPU_XDP;PCH_XDP

Size	Document Number	Rev
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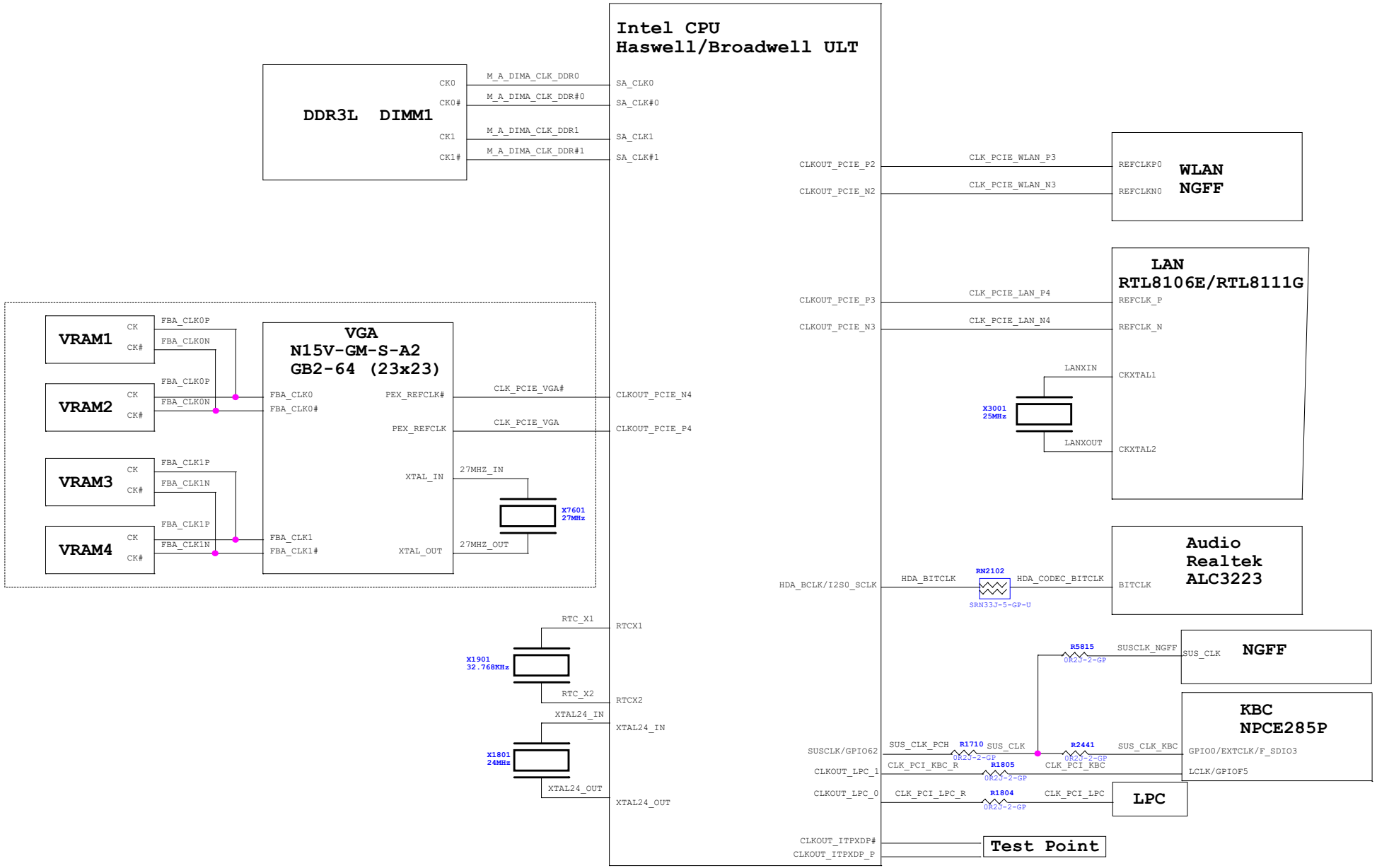
CLK Block Diagram



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Title: CLK Block Diagram

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Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER

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Title: ***Change History***

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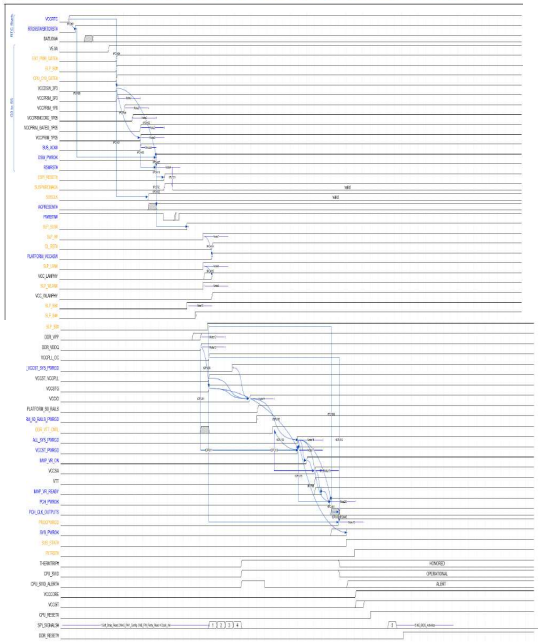
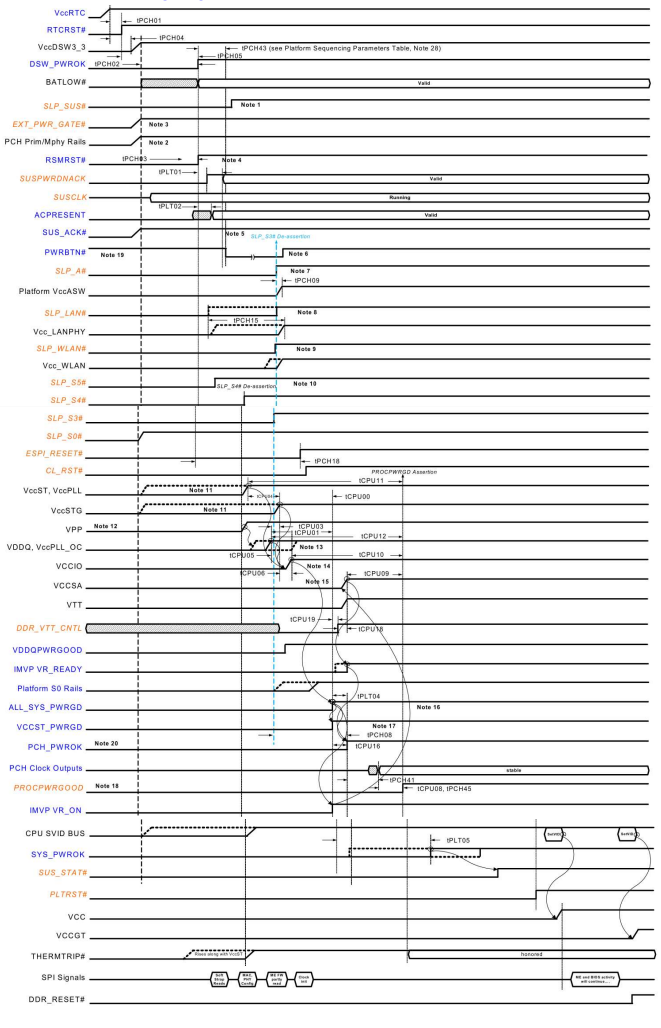
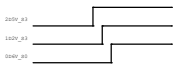
Figure 12-19.WHL-U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform]



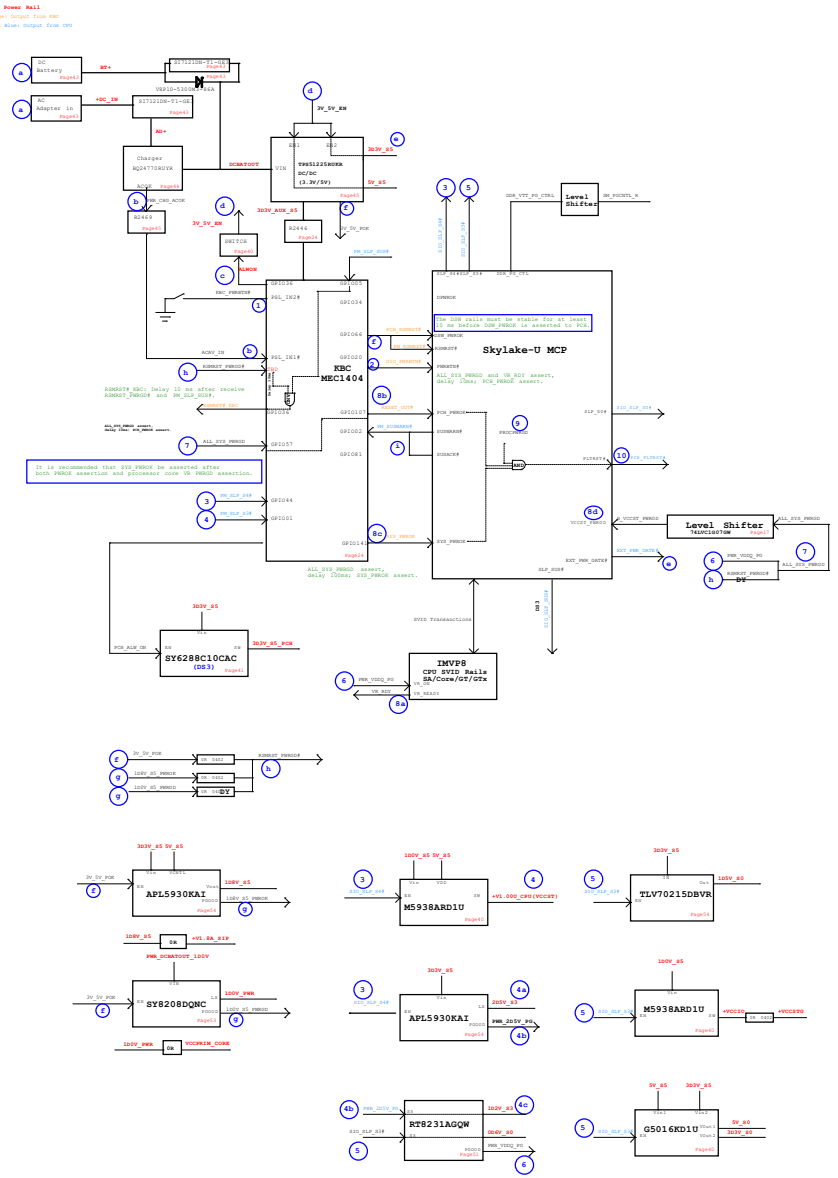
KBL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



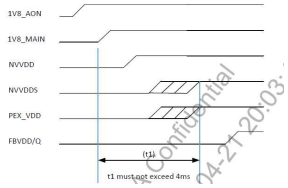
For DDR4 power sequence



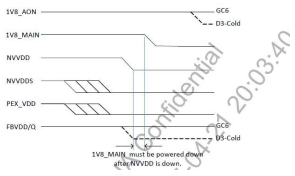
Tulip Skylake POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)

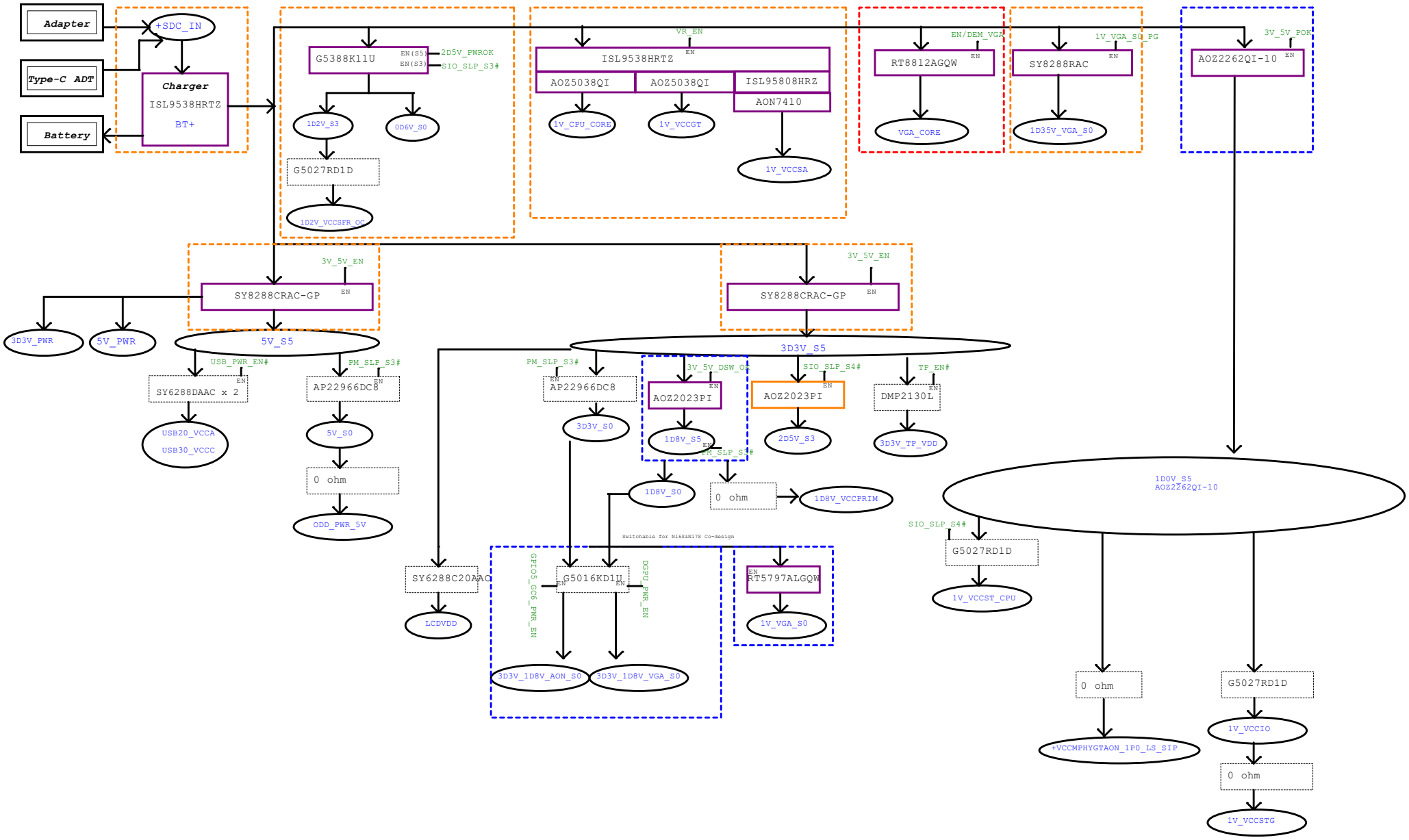


NV N17S GPU Power ON sequence



NV N17S GPU Power Down sequence





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Title: Power Block Diagram

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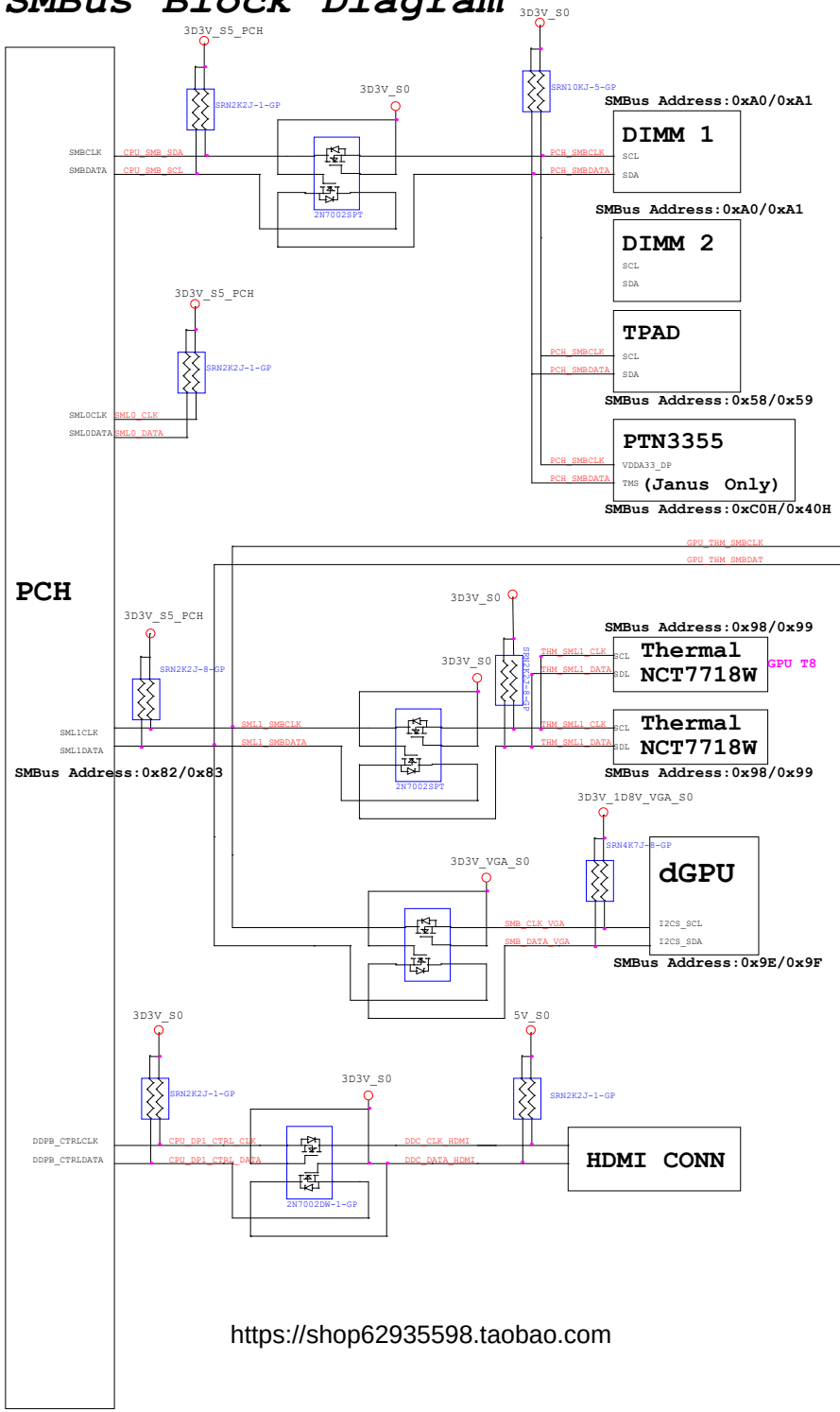
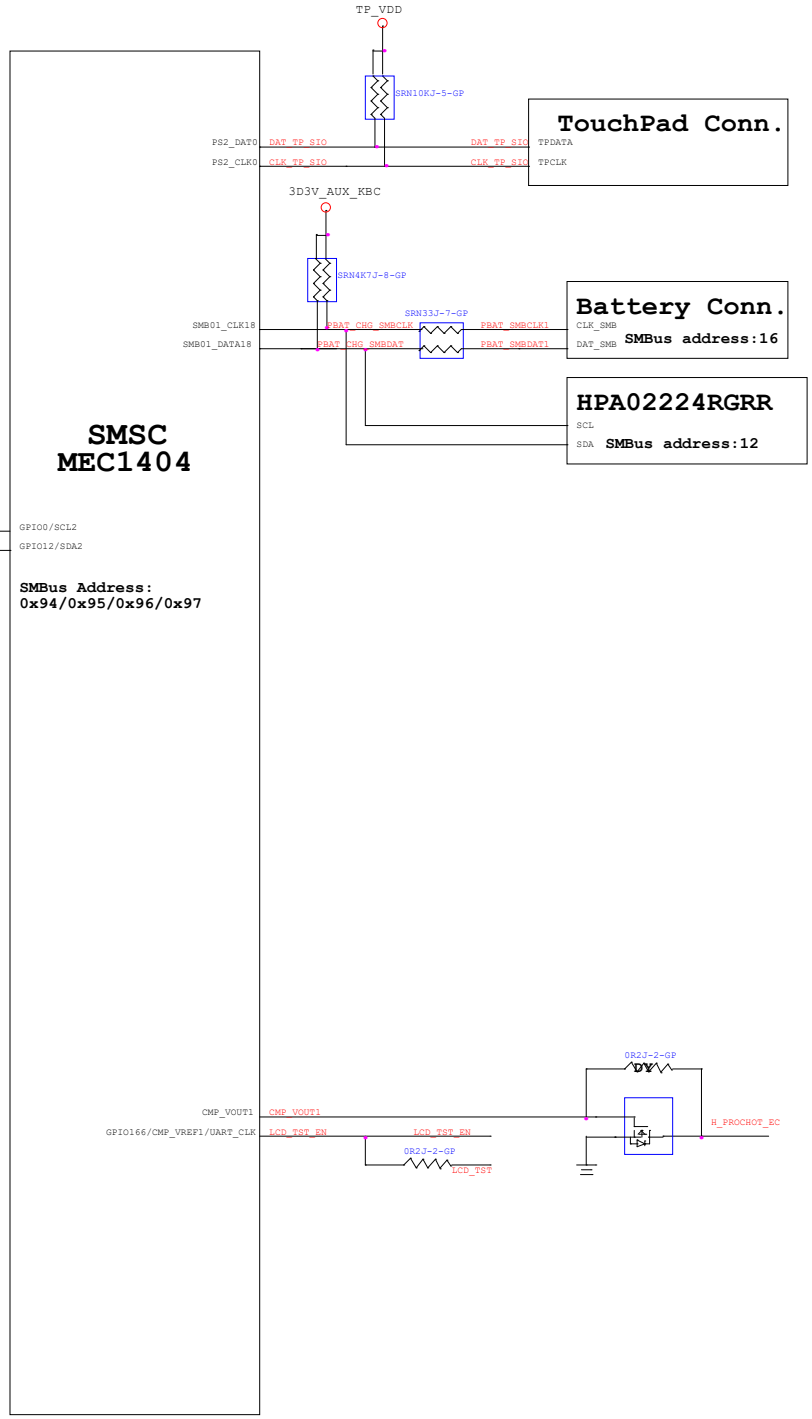
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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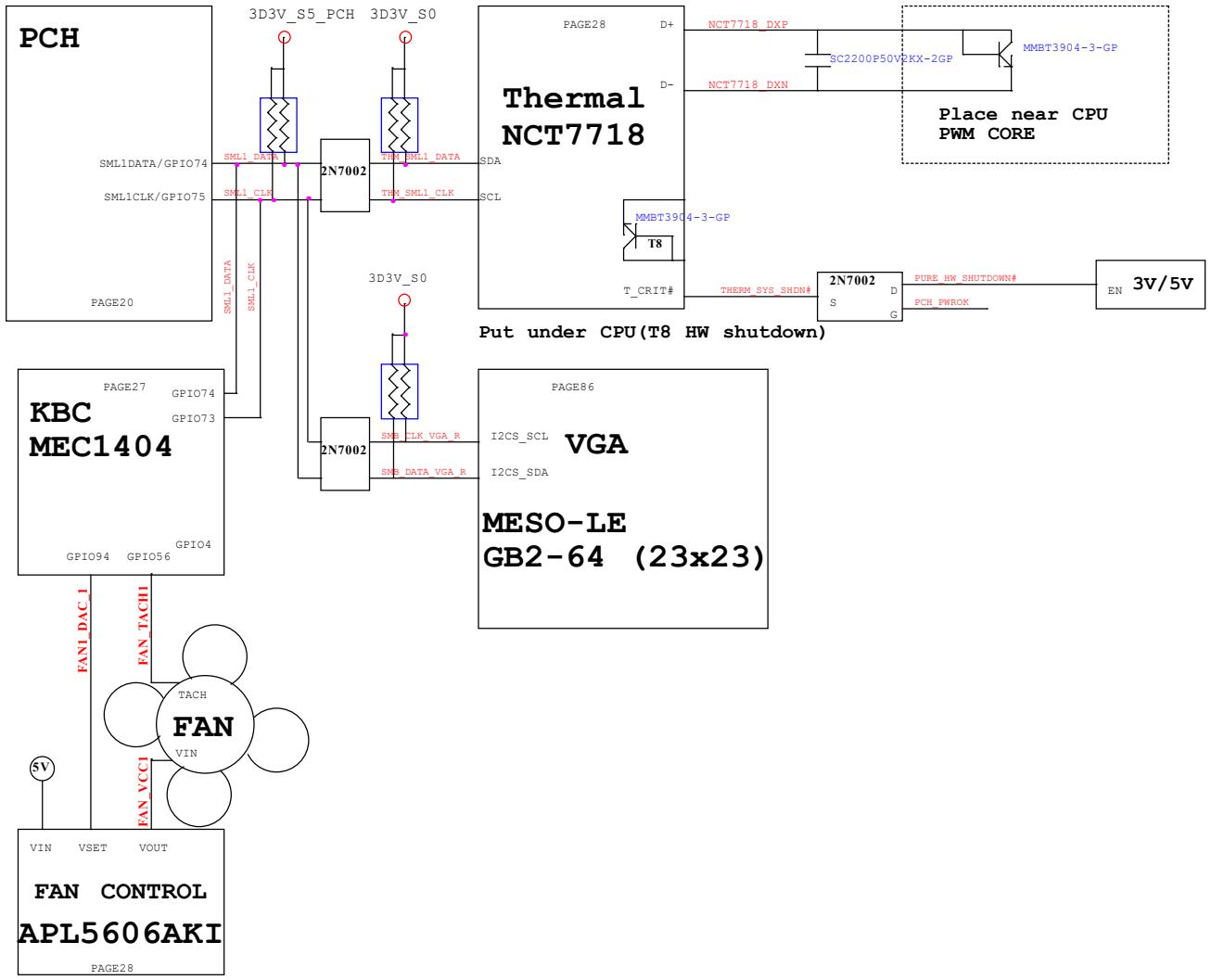
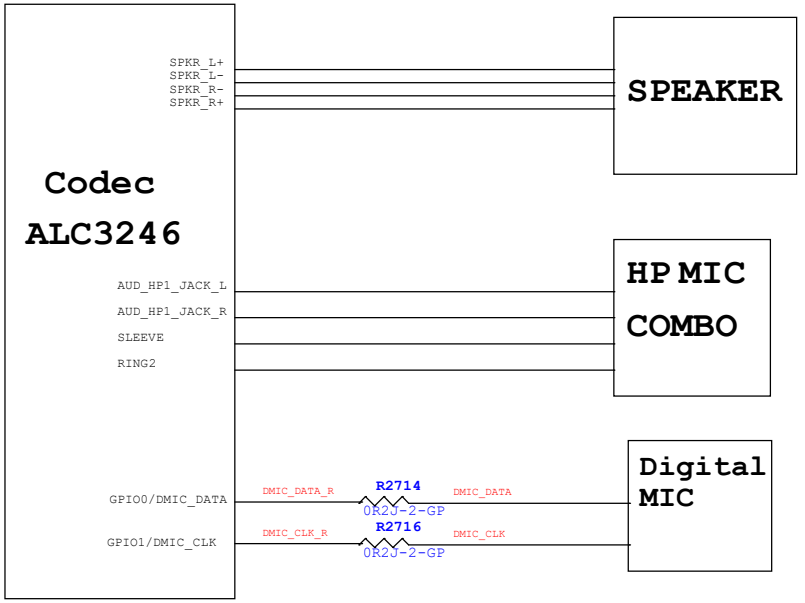
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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Custom	Bucky WHL	SA

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