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Intel M/B Schematics Document

Kabylake-U(2+2)-DDR4 SODIMMx2

nVidia N16 gDDR5-2GB

(N16S-GTR : GM108-670/770: GeForce MX130)
(N16V-GMR1 : GM108-626/726:GeForce MX110)

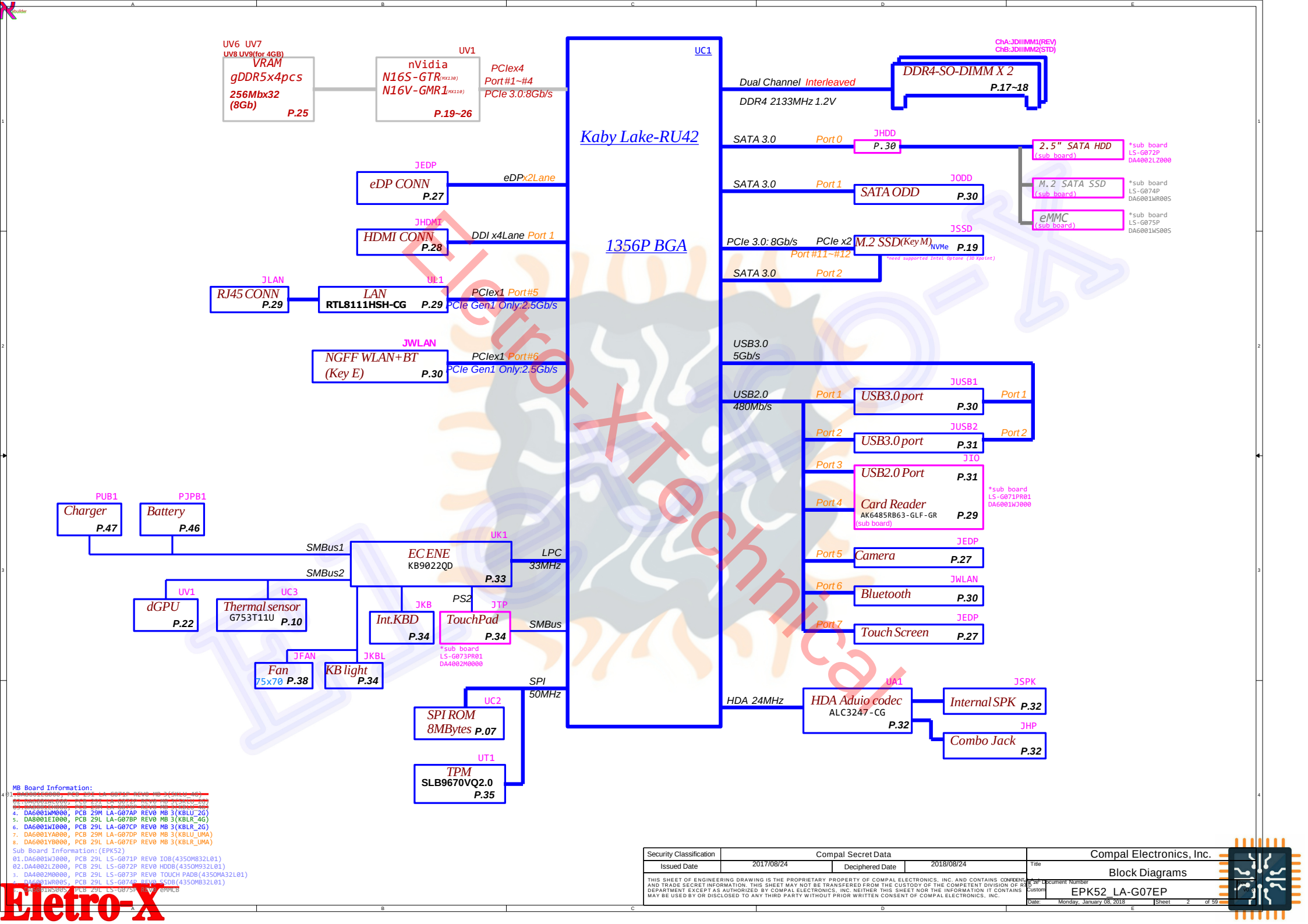
Project :2018OPP_Harry Potter(15.6")
EPK52 :LA-G07DP

Date : 2018-01-08
Version : 1.0

(Modified&Ref from:
01."NFLC_KBLR_LAE802PR10_MV_FINAL")
(02."Canadiens_LA-F035P-R10_KBL-UR_2017-06-23_CPU)
(02."CNL-U ORB_DDX02_LA-F152PR01_0822B")

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2017/10/22

Compal Electronics, Inc.			
Title: Cover Page			
Size: Custom	Document Number: EPK52_LA-G07EP		Rev: 1.0
Date: Monday, January 08, 2018	Sheet 1 of 59		



MB Board Information:

1. DA6001EG000, PCB 29L LA-G074P REV0 MB 3(5MKLU_4G)
2. DA6001WL000, PCB 29L LA-G072P REV0 MB 3(KBLU_2G)
3. DA6001WM000, PCB 29M LA-G07AP REV0 MB 3(KBLU_2G)
4. DA8001EI000, PCB 29L LA-G07BP REV0 MB 3(KBLR_4G)
5. DA6001WI000, PCB 29L LA-G07CP REV0 MB 3(KBLR_2G)
6. DA6001YA000, PCB 29M LA-G07DP REV0 MB 3(KBLU_UMA)
7. DA6001YB000, PCB 29L LA-G07EP REV0 MB 3(KBLR_UMA)

Sub Board Information:(EPK52)

1. DA6001WJ000, PCB 29L LS-G071P REV0 IOB(435OM832L01)
2. DA4002LZ000, PCB 29L LS-G072P REV0 HDDB(435OM932L01)
3. DA4002M0000, PCB 29L LS-G073P REV0 TOUCH PADB(435OMA32L01)
4. DA6001WR00S, PCB 29L LS-G074P REV0 SSDB(435OMB32L01)
5. DA6001WS00S, PCB 29L LS-G075P REV0 eMMCB

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

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Title: Block Diagrams

Size: Custom | Document Number: EPK52_LA-G07EP | Rev: 1.0

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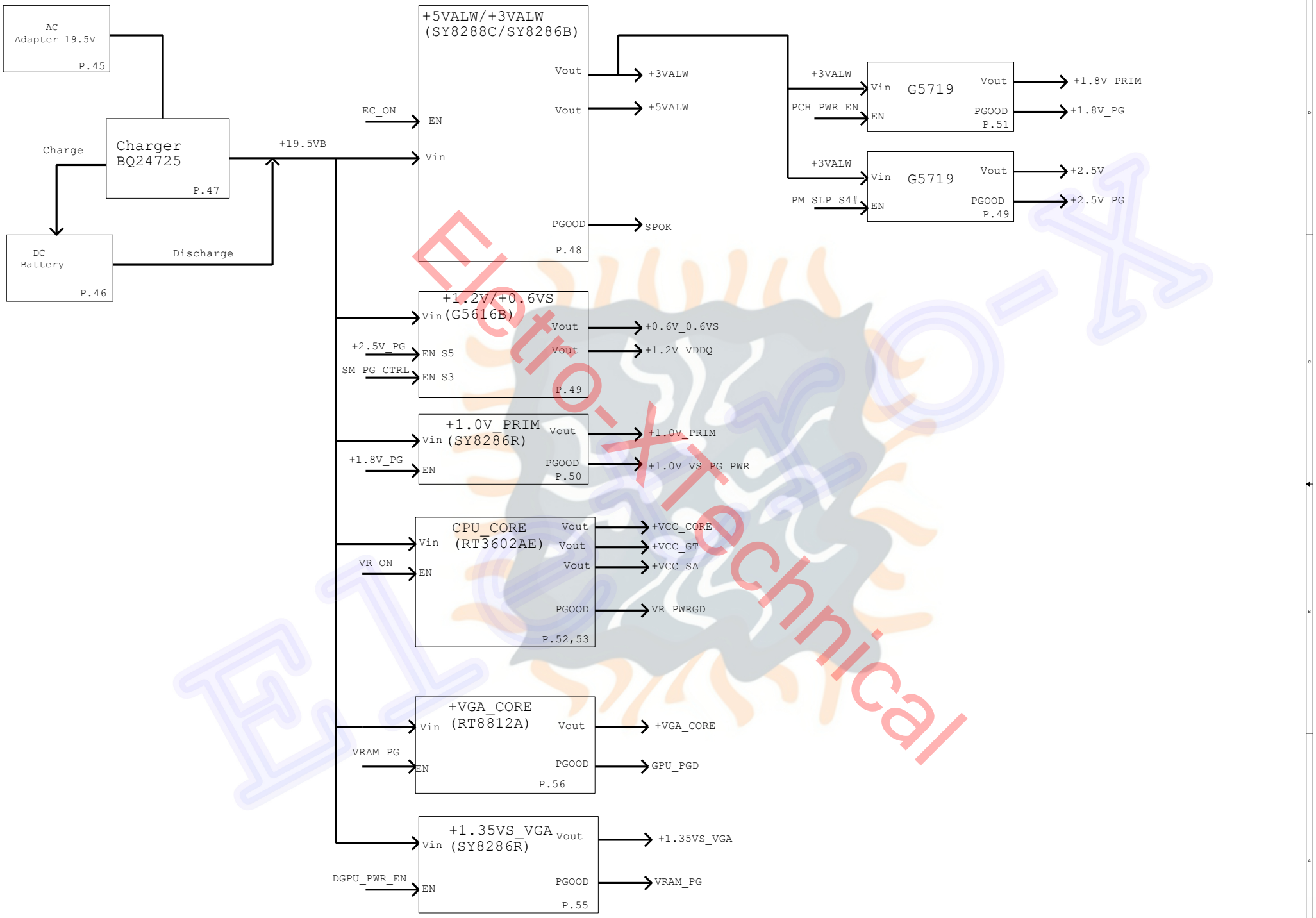

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Title	Power Block Diagram		
File Document Number	EPK52_LA-G07EP		Rev 0.3
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Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.2V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.6VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

BOM Structure Table (1/2)

Function	*Stuff*	*Un-Stuff*
DGPU SKU	PX@	
UMA SKU	UMA@	
TPM	TPM@	

SOC SMBUS Address Table

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBCLK SMBDATA	+3V_PRIM	DIMM1	0x50	0xA0	0xA1
		DIMM2	0x52	0xA4	0xA5
		Touch PAD	0x2C	0x58	0x59

EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
SMBUS Port 1	+3VL_EC	BAT	0x16
		CHGR	0x12
SMBUS Port 2	+3VS	dGPU	
		Thermal Sensor	0x90
		PCH	

Power State

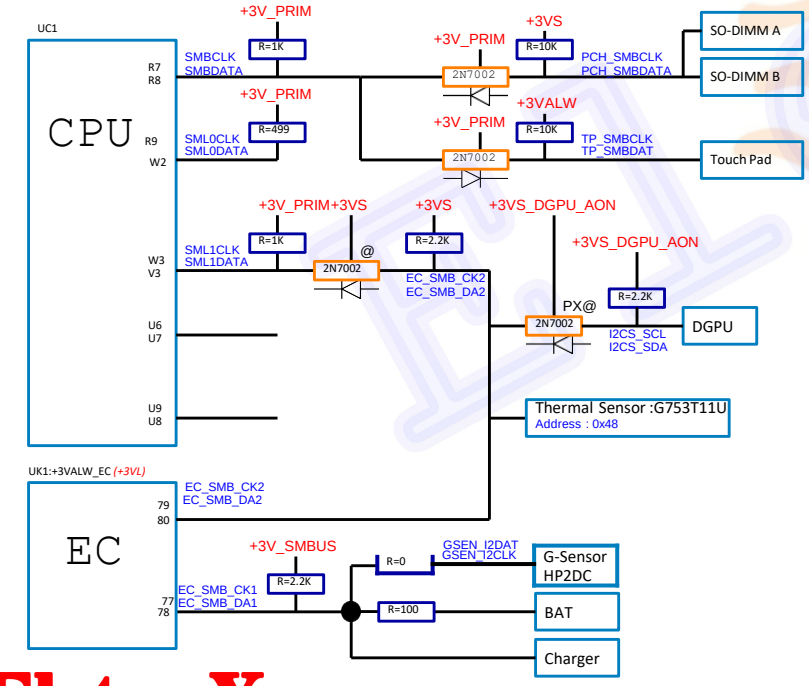
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

<USB2.0 port>

USB2.0 port	DESTINATION
1	USB3.0 Type-C
2	USB2.0/USB3.0
3	USB2.0/USB3.0
4	BT
5	HD/IR_1/IR_2 Camera
6	IR_2 Camera
7	Card Reader
8	X
9	X
10	X

<PCI-E,SATA,USB3.0/CLK>

Lane#	PCI-E	SATA	USB3.0		DESTINATION		CLK
1				1	USB3.0 Type-C		X
2				2	USB3.0 Type-C		X
3				3	USB2.0/USB3.0		X
4				4	USB2.0/USB3.0		X
5	1			5	GPU(DIS only)		CLK0
6	2			6	GPU(DIS only)		
7	3				GPU(DIS only)		
8	4				GPU(DIS only)		
9	5				LAN		CLK1
10	6				WLAN		CLK2
11	7		0		HDD		X
12	8		1a		ODD		CLK3
13	9				X		X
14	10				X		X
15	11		1b*		NVMe x2	X	CLK4
16	12		2			SATA SSD	X



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Title	Notes List		
Size	Document Number		LA-G07DP(KBL-U UMA) 6B
Custom			
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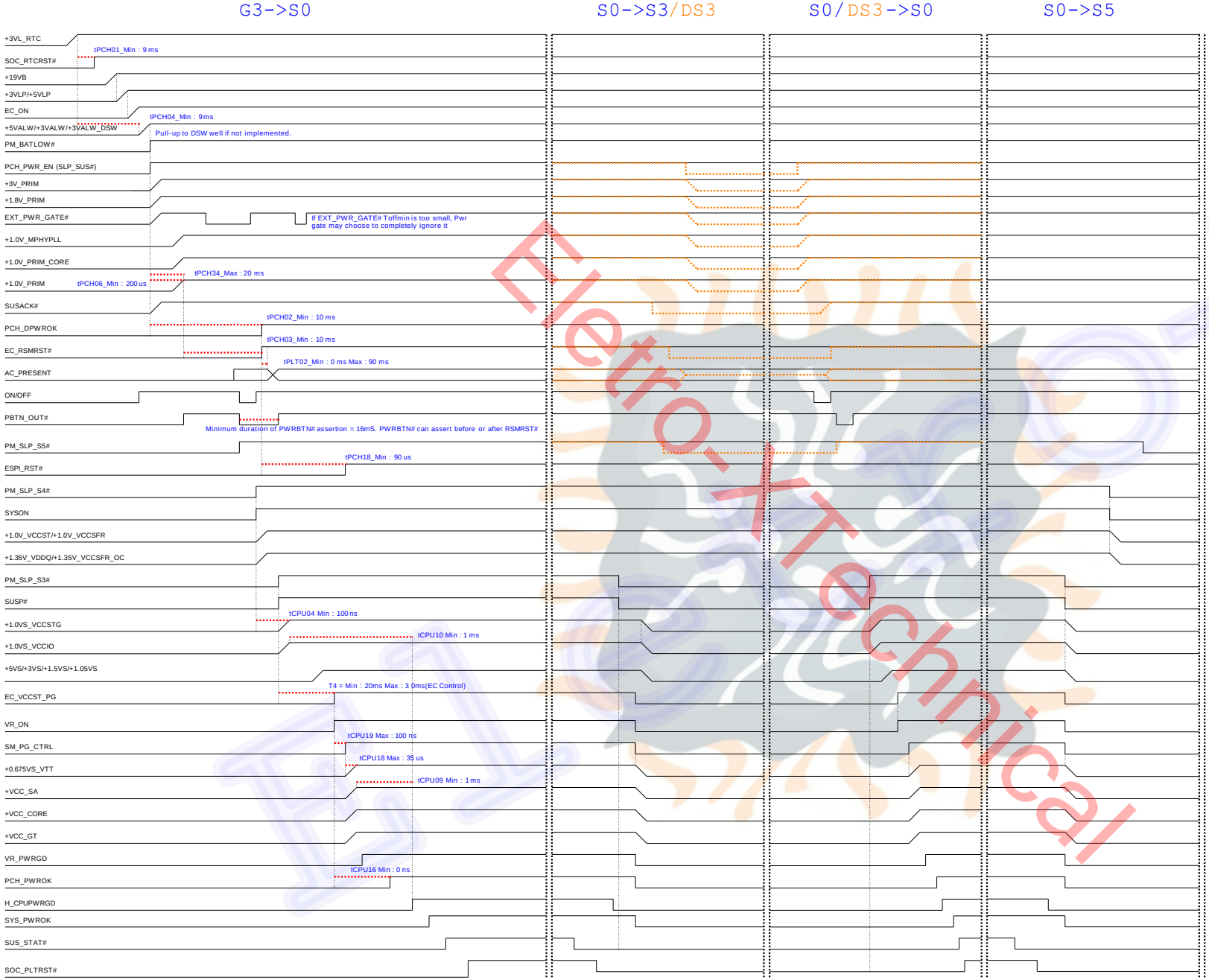
[Diner-PWR Sequence_SKL-U22_DDR3L_Volume_NON CS]



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SOC_DP1_CTRL_DATA(Internal Pull Down):

Display Port B Detected

0 = Port B is not detected.

1 = Port B is detected.

SOC_DP2_CTRL_DATA(Internal Pull Down):

Display Port C Detected

0 = Port C is not detected.

1 = Port C is detected.

<HDMI>

<eDP>

HDMI DDC (Port B)

UC1A SKL-U

SKL-U_BGA1356

UC1D SKL-U

SKL-U_BGA1356

COMPENSATION PU FOR eDP

CAD note:
Trace width=20 mils,Spacing=25mil,Max length=100mils

XDP CONN

Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: SKL-U(1/12)DDI,MSIC,XDP,EDP

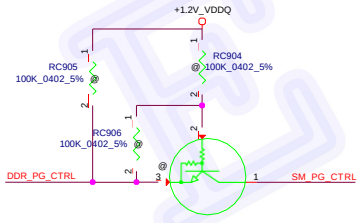
Size: Custom | Document Number: EPK52_LA-G07EP | Rev: 1.0

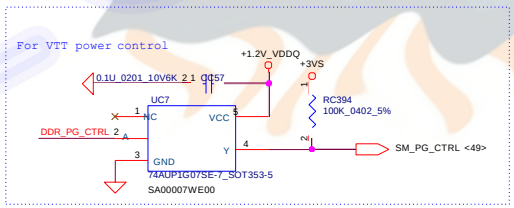
Date: Friday, January 05, 2018 | Sheet 5 of 5

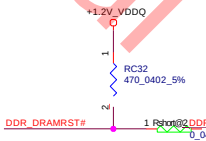
Interleaved Memory

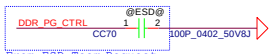
Interleaved Memory

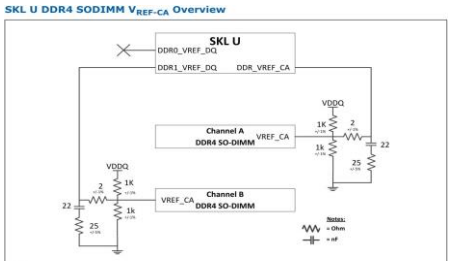
<Cocoa_1020>
PDG#543016, ODT: CPU side no connect, DRAM side connect to VDDQ(Memory down); FET+R(SO-DIMM)











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Compal Electronics, Inc.	
Title: SKL-U(2/12)DDRIII	
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SML0ALERT# (Internal Pull Down):
eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

UC1E SKL-U SPI-FLASH SMBUS, SMLINK LPC CLINK

<35> HOST_SPI_0_SO
<35> HOST_SPI_0_SI
HOST_SPI_0_CLK AV2
HOST_SPI_0_SO AW3
HOST_SPI_0_SI AY3
HOST_SPI_0_SIO2 AW2
HOST_SPI_0_SIO3 AU4
HOST_SPI_0_CS0# AU3
AU2
<35> HOST_SPI_0_CS2#
HOST_SPI_0_CS2# AU1
SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#

M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
M4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

G3 CL_CLK
G2 CL_DATA
G1 CL_RST#

<33> EC_KBRST# EC_KBRST# AW13 GPP_A0/RCIN#
To TPM <33,35> SERIRQ SERIRQ AY11 GPP_A6/SERIRQ
LPC Mode

SKL-U_BGA1356 5 OF 20

R7 SMBCLK
R8 SMBDATA
R10 SMBALERT# TP@ T239
R9 SML0CLK
W2 SML0DATA
W1 SML0ALERT#
W3 SML1CLK
V3 SML1DATA
AM7 GPP_B23 1 2 SML1ALERT#
RC902 @ 0_0201_5%
TP@ T234

GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#

SMB (Link to XDP, DDR, TP)
SML1 (Link to EC,DGPU, LAN, Thermal Sensor)

SML0ALERT# RC218 1K_0402_1%

+3V_PRIM
SML1ALERT# RC903 2 @ 1 150K_0402_1%
SML0ALERT# RC360 2 @ 1 10K_0402_5%
+3VS
SMBALERT#
EC_KBRST#
RPC19 10K_0804_8P4R_5%

AY13 LPC_AD0 LPC_AD0 <33>
BA13 LPC_AD1 LPC_AD1 <33>
BB13 LPC_AD2 LPC_AD2 <33>
AY12 LPC_AD3 LPC_AD3 <33>
BA12 LPC_FRAME# LPC_FRAME# <33>
BA11 SUS_STAT# TP@ T2402

GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A14/SUS_STAT#/ESPI_RESET#

AW9 CLK_PCI0 RC387 1 2 22_0402_5% CLK_PCI_LPC <33>
AY9
AW11 PM_CLKRUN# PM_CLKRUN# <33>
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A8/CLKRUN#

CC182 22P 50V J NPO 0402 EMI@

To EC

to SPI ROM UC2 Source From

RPH11
HOST_SPI_0_CS0#_R 1 8 EC_SPI_CS0#
HOST_SPI_0_CS0#_R 2 7 HOST_SPI_0_CS0#
HOST_SPI_0_SO_R 3 6 EC_SPI_SO
HOST_SPI_0_SO_R 4 5 HOST_SPI_0_SO
EC_SPI_CS0# <33>
EC_SPI_SO <33>
15_0804_8P4R_5%

RPH12
HOST_SPI_0_HOLD# 1 8 HOST_SPI_0_SIO3
HOST_SPI_0_SI_R 2 7 HOST_SPI_0_SI
HOST_SPI_0_SI_R 3 6 EC_SPI_SI
EC_SPI_SI <33>
15_0804_8P4R_5%

HOST_SPI_0_WP# 2 RC388 15_0402_5% 1 HOST_SPI_0_SIO2

SPI ROM (8MByte Only)
UC2
HOST_SPI_0_CS0#_R 1 CS# VCC 8 +3V_SPI
HOST_SPI_0_SO_R 2 DO(IO1) HOLD#(IO3) 7 HOST_SPI_0_HOLD#
HOST_SPI_0_WP# 3 WP#(IO2) CLK 6 HOST_SPI_0_CLK_R
4 GND DI(IO0) 5 HOST_SPI_0_SI_R
XM25QH64AHIG SOP 8P
SA0000B8300
ACES_91960-0084L_8P-T
Use socket footprint
CC8 1 2 0.1U_0201_10V6K

+3VS
RC216 10K_0402_5%
RC215 10K_0402_5%
QC1A
SMBCLK 6
L2N7002SDW1T1G 2N SC88-6
SB00001FF00
PCH_SMBCLK <17,18>
QC1B
SMBDATA
L2N7002SDW1T1G 2N SC88-6
SB00001FF00
PCH_SMBDATA <17,18>

+3VS
<DB> Un-pop QC2 for new 0x90 thermal sensor
SML1CLK 6
QC2A
L2N7002SDW1T1G 2N SC88-6
SB00001FF00
EC_SMB_CK2 <10,33>
SML1DATA
QC2B
L2N7002SDW1T1G 2N SC88-6
SB00001FF00
EC_SMB_DA2 <10,33>

+3V_PRIM
SML0CLK RC49 1 2 499_0402_1%
SML0DATA RC50 1 2 499_0402_1%
RPC7
SML1CLK 1 8
SML1DATA 2 7
SMBCLK 3 6
SMBDATA 4 5
1K_0804_8P4R_5%

+3V_SPI
HOST_SPI_0_SIO2 RC3901 @ 2 1K_0402_1%
HOST_SPI_0_SIO3 RC3911 @ 2 1K_0402_1%
HOST_SPI_0_CS0# R 1 @ 2 RC357 1K_0402_5%

+3V_PRIM +3VALW
RC81 10K_0402_5%
RC82 10K_0402_5%
SB00001FF00
SMBCLK 1
QC7A
L2N7002SDW1T1G 2N SC88-6
TP_SMBCLK <34>
SMBDATA
QC7B SB00001FF00
L2N7002SDW1T1G 2N SC88-6
TP_SMBDATA <34>

HOST_SPI_0_SIO3 RC51 1 ES@ 2 1K_0402_1%
From WW36 MOW for SKL-U ES sample

+3VS_PGPPA
PM_CLKRUN# RC107 1 2 8.2K_0402_5%
SERIRQ RC122 1 2 8.2K_0402_5%

Follow 543016_SKL_U_Y_PDG_0_9

CLK Source CPU to SPI ROM UC2&EC
HOST_SPI_0_CLK 2 RC368 15_0402_5% EMI@ 1 HOST_SPI_0_CLK_R HOST_SPI_0_CLK_R <33,35>
CC9 10P_0402_50V8J @EMI@

EON SA000046400 S IC FL 64M EN25Q64-104HIP SOP 8P MXIC
SA00006N100 S IC FL 64M MX25L6473EM2I-10G SOP 8P
WINBOND SA000039A30 S IC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM
Micron SA00005L100 S IC FL 64M M25Q064A13ESEC0F SO8W 8P

ENE Fixed Code Block Diagram
CPU SPI_CLK SPI_CS0# SPI_MOSI SPI_MISO SPI_IO2 SPI_IO3
PCH_SPI_CLK PCH_SPI_CS0# PCH_SPI_SI PCH_SPI_SO PCH_SPI_SIO2 PCH_SPI_SIO3
PCH_SPI_CLK_R PCH_SPI_CS0#_R PCH_SPI_SI_R PCH_SPI_SO_R PCH_SPI_SIO3
SPI_ROM 6_SPI_CLK 1_SPI_CS0# 5_SPI_MOSI 2_SPI_MISO 3_WP#_IO2 7_HOLD#_IO3
EC 126_SPI_CLK 128_SPI_CS0# 120_SPI_MOSI 119_SPI_MISO
EC_SPI_CLK EC_SPI_CS0# EC_SPI_SI EC_SPI_SO
M:Master S : Slave O : Output I : Input

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Compal Electronics, Inc.
Title: SKL-U(3/12)SPI,ESPI,SMB,LPC
Size: Custom
Document Number: EPK52_LA-G07EP
Date: Friday, January 05, 2018
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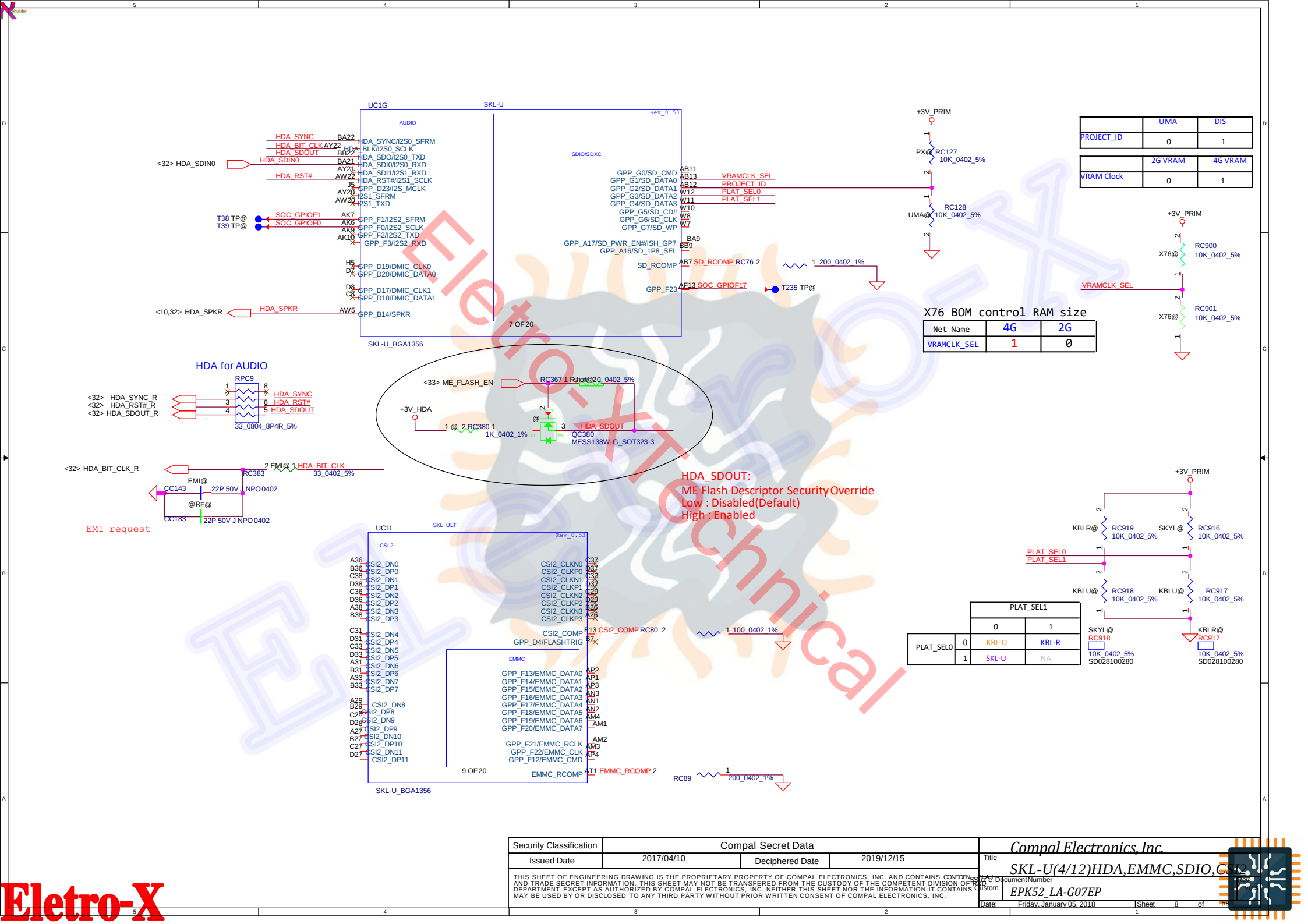

	UMA	DIS
PROJECT_ID	0	1

	2G VRAM	4G VRAM
VRAM Clock	0	1

X76 BOM control RAM size

Net Name	4G	2G
VRAMCLK_SEL	1	0

PLAT_SEL0	PLAT_SEL1 = 0	PLAT_SEL1 = 1
0	KBL-U	KBL-R
1	SKL-U	NA

Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

Size: Custom | Document Number: EPK52_LA-G07EP | Rev: 1.0

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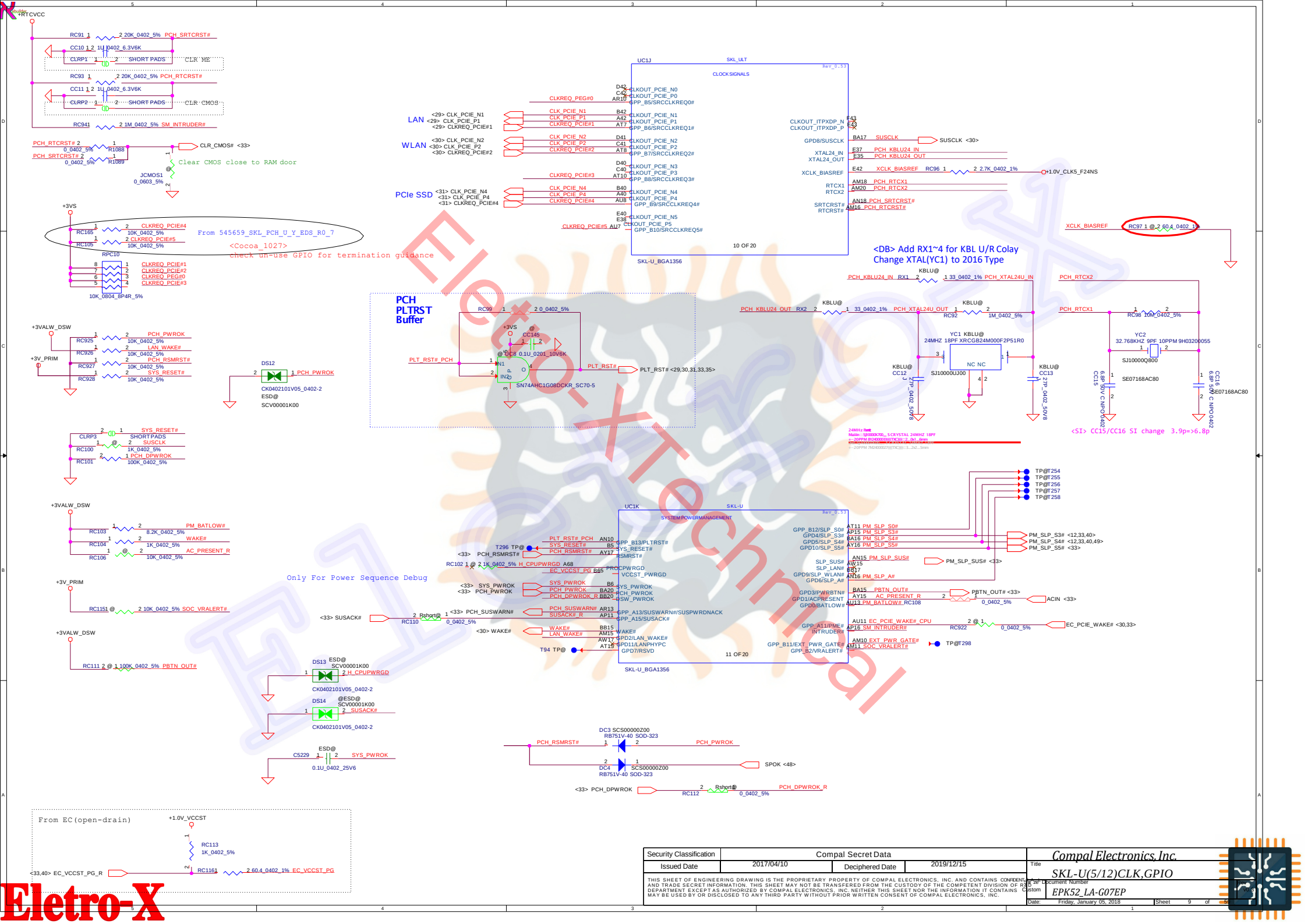

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Title	Compal Electronics, Inc.		
	SKL-U(5/12)CLK,GPIO		
Size: Custom	Document Number: EPK52_LA-G07EP		Rev: 0.3
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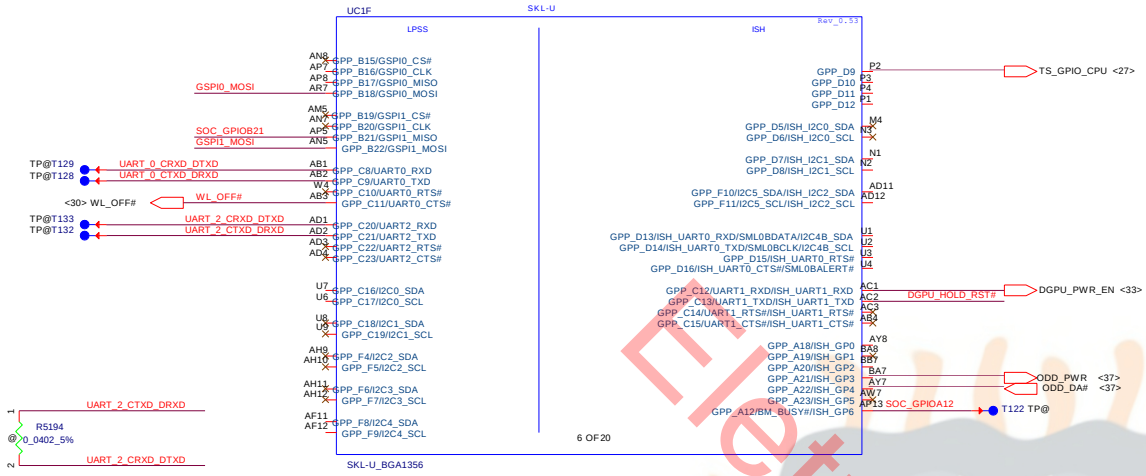
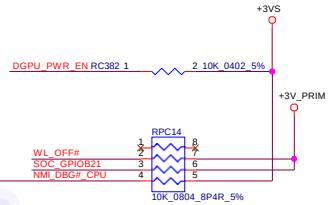
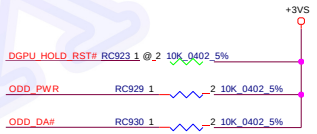






Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.---> AAX05 Use

1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

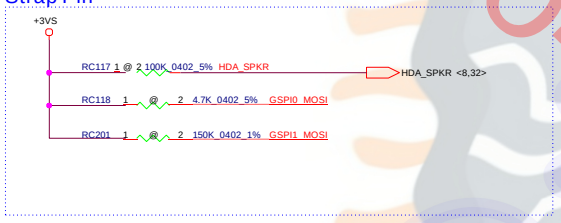
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode --> AAX05 Use

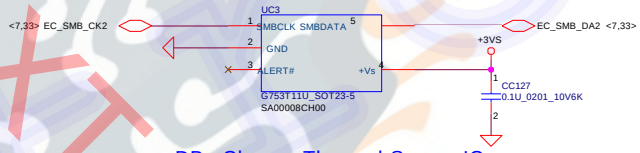
1 = LPC Mode

Strap Pin



CPU THERMAL SENSOR

Address : 0x48



<DB> Change Thermal Sensor IC

Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Title	Compal Electronics, Inc.
	SKL-U(6/12)GPIO
Size: Custom	Document Number: EPK52_LA-G07EP
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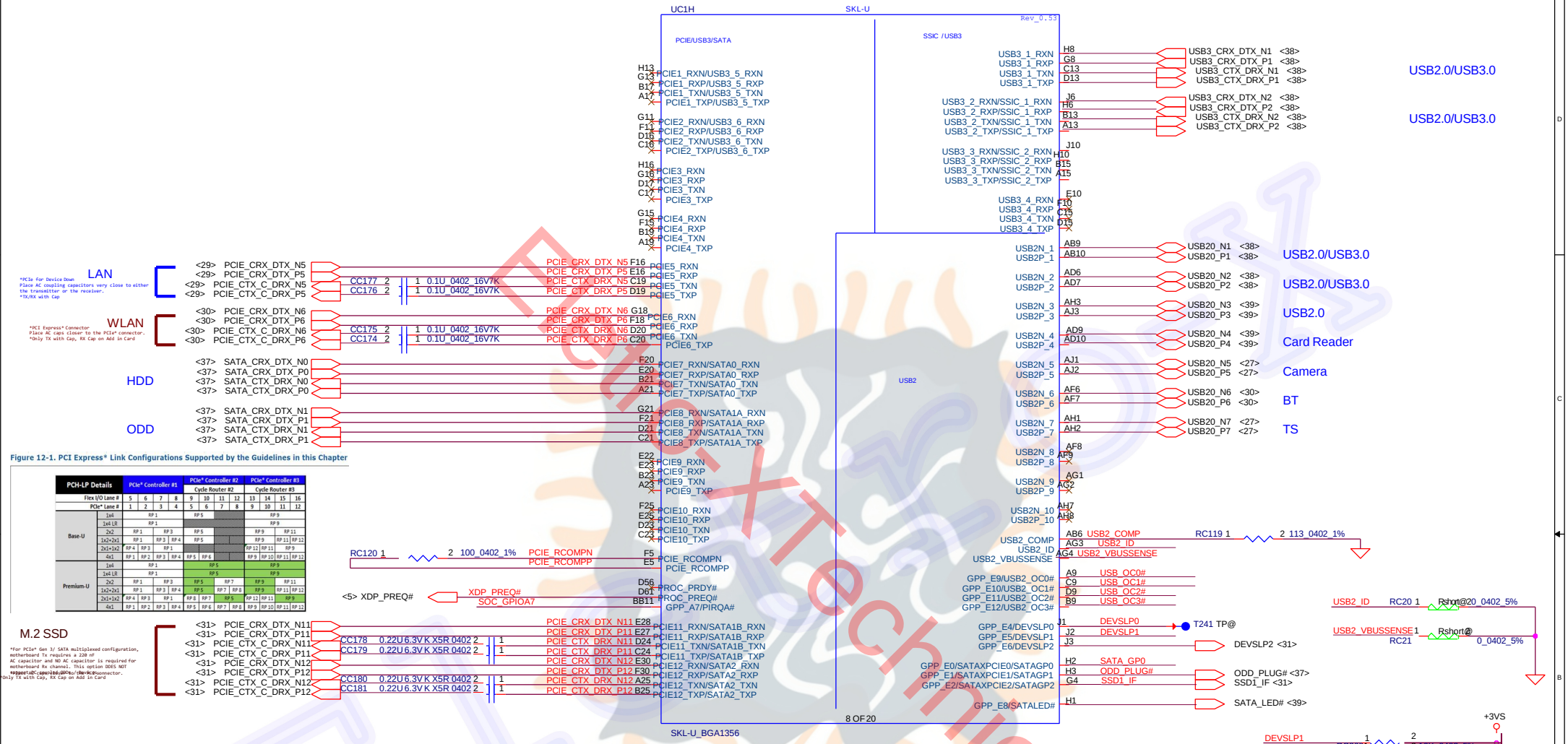
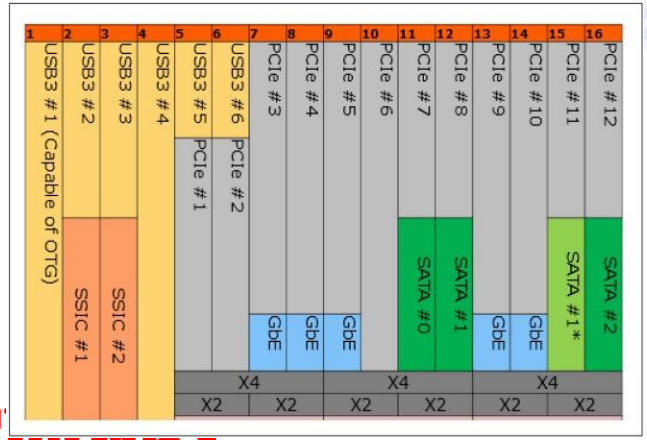


Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
						Cycle Router #2				Cycle Router #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP1				RP5				RP9			
	1x4 LR	RP1								RP9			
	2x2	RP1		RP3		RP5				RP9		RP11	
	1x2+2x1	RP1		RP3	RP4	RP5				RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1						RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6			RP9	RP10	RP11	RP12
Premium-U	1x4	RP1				RP5				RP9			
	1x4 LR	RP1				RP5				RP9			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12

High Speed I/O (HSIO) Lane Multiplexing in SKL U



When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1 and Port 2
USB_OC1#	USB2 Port 3
USB_OC2#	N/A
USB_OC3#	N/A
DEVSLP0	N/A
DEVSLP1	N/A
DEVSLP2	NGFF SSD KEY- M
SATA_GP0	N/A
SATA_GP1	ODD_PLUG#
SATA_GP2	PCIE/SATA

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Title: SKL-U(7/12)PCIE,USB,SATA

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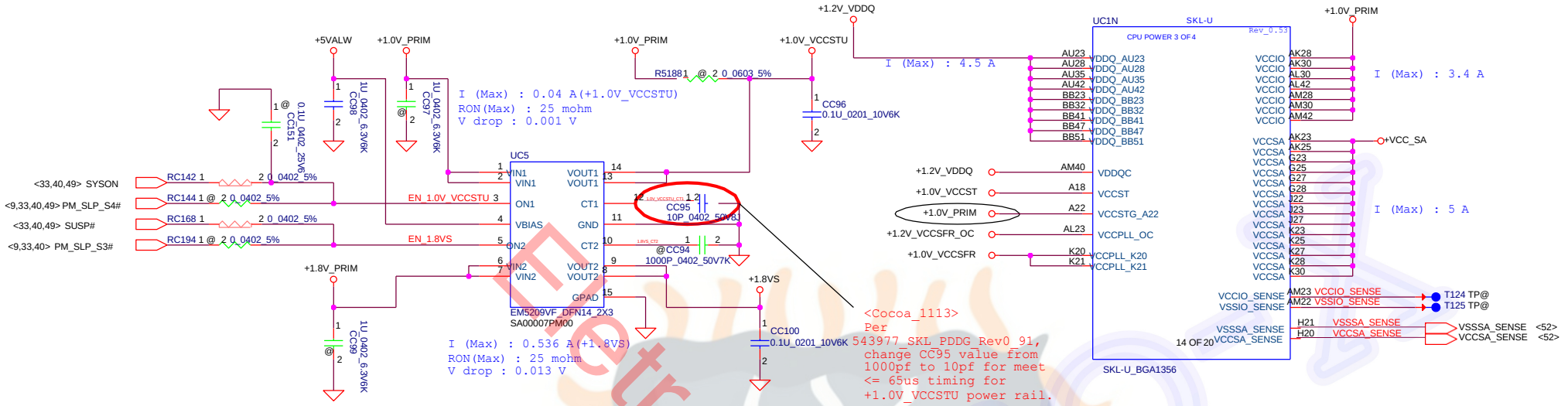
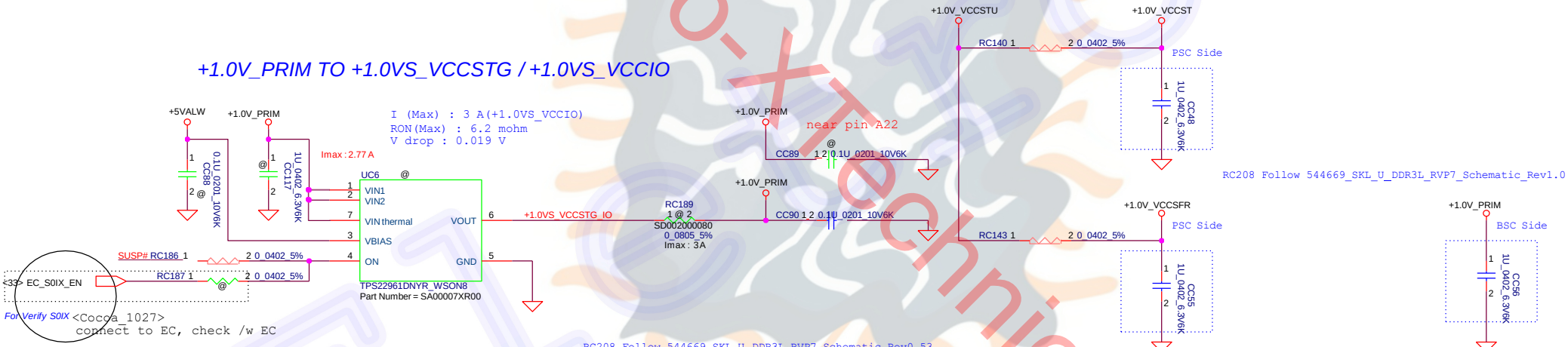
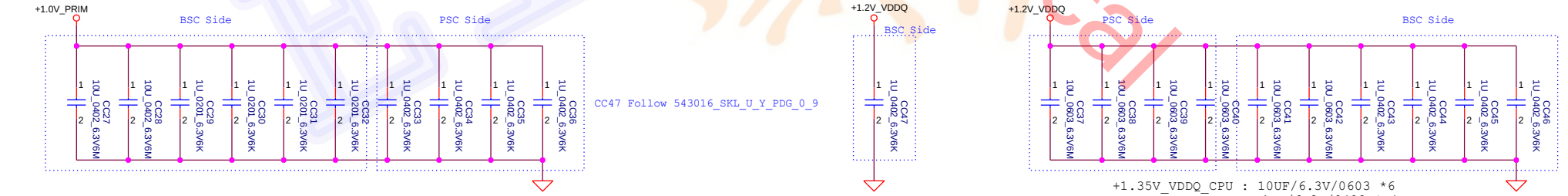
+1.0V_PRIM TO +1.0V_VCCSTU



<Cocoa_1113>
Per 543977_SKL_PDDG_Rev0_91, change CC95 value from 1000pf to 10pf for meet <= 65us timing for +1.0V_VCCSTU power rail.

+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO





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Title: SKL-U(8/12)Power

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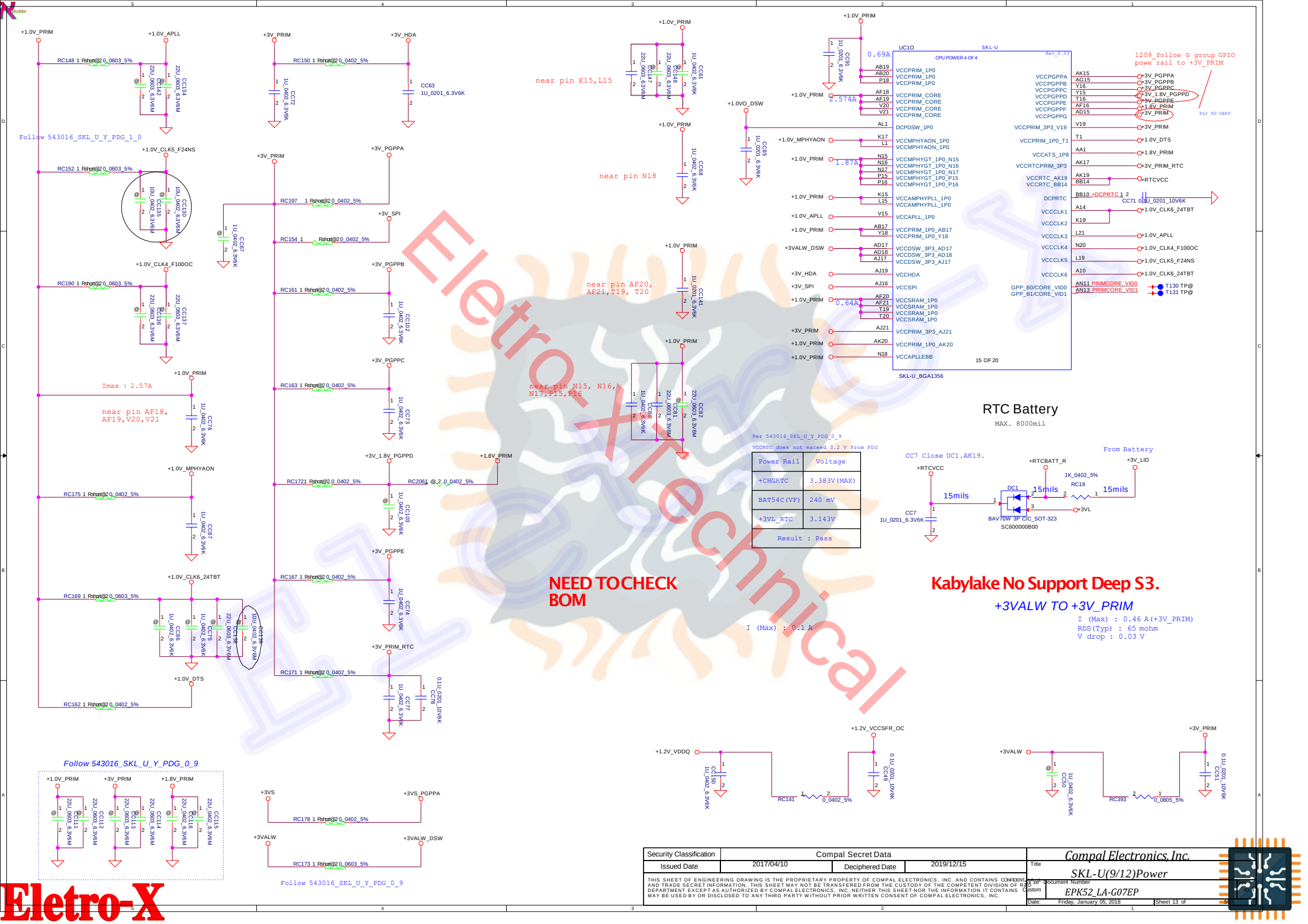
+1.0V_PRIM
+1.0V_APLL
+3V_PRIM
+3V_HDA
RC148 1 Rshort@20_0603_5%
RC150 1 Rshort@20_0402_5%
CC63 1U_0201_6.3V6K
Follow 543016_SKL_U_Y_PDG_1_0
+1.0V_CLK5_F24NS
RC152 1 Rshort@20_0603_5%
+3V_PGPPA
RC197 1 Rshort@20_0402_5%
+3V_SPI
RC154 1 Rshort@20_0402_5%
+1.0V_CLK4_F100OC
RC190 1 Rshort@20_0603_5%
+3V_PGPPB
RC161 1 Rshort@20_0402_5%
Imax : 2.57A
near pin AF18, AF19,V20,V21
+3V_PGPPC
RC163 1 Rshort@20_0402_5%
+1.0V_MPHYAON
RC175 1 Rshort@20_0402_5%
+3V_1.8V_PGPPD
+1.8V_PRIM
RC1721 Rshort@20_0402_5%
RC2061 @ 2_0_0402_5%
+1.0V_CLK6_24TBT
RC169 1 Rshort@20_0603_5%
+3V_PGPPE
RC167 1 Rshort@20_0402_5%
+3V_PRIM_RTC
RC171 1 Rshort@20_0402_5%
+1.0V_DTS
RC162 1 Rshort@20_0402_5%
Follow 543016_SKL_U_Y_PDG_0_9
+3VS
+3VS_PGPPA
RC178 1 Rshort@20_0402_5%
+3VALW
+3VALW_DSW
RC173 1 Rshort@20_0603_5%
Follow 543016_SKL_U_Y_PDG_0_9
near pin K15,L15
near pin N18
near pin AF20, AF21,T19, T20
near pin N15, N16, N17,P15,P16
UC1O
SKL-U
CPU POWER 4 OF 4
0.69A
2.574A
1.87A
0.64A
15 OF 20
SKL-U_BGA1356
1209_follow G group GPIO powe rail to +3V_PRIM
For SD CARD
+1.0V_DTS
+1.8V_PRIM
+3V_PRIM_RTC
+RTCVCC
+1.0V_APLL
+1.0V_CLK4_F100OC
+1.0V_CLK5_F24NS
+1.0V_CLK6_24TBT
T130 TP@
T131 TP@
RTC Battery
MAX. 8000mil
Per 543016_SKL_U_Y_PDG_0_9
VCCRTC does not exceed 3.2 V From PDG
Power Rail | Voltage
+CHGRTC | 3.383V(MAX)
BAT54C(VF) | 240 mV
+3VL_RTC | 3.143V
Result : Pass
CC7 Close UC1.AK19.
From Battery
15mils
1K_0402_5%
BAV70W 3P C/C_SOT-323
SC600000B00
NEED TOCHECK BOM
Kabylake No Support Deep S3.
+3VALW TO +3V_PRIM
I (Max) : 0.46 A(+3V_PRIM)
RDS(Typ) : 65 mohm
V drop : 0.03 V
I (Max) : 0.1 A
+1.2V_VDDQ
+1.2V_VCCSFR_OC
RC141 0_0402_5%
RC393 0_0805_5%
Security Classification | Compal Secret Data
Issued Date | 2017/04/10
Deciphered Date | 2019/12/15
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Document Number
EPK52_LA-G07EP
Friday, January 05, 2018
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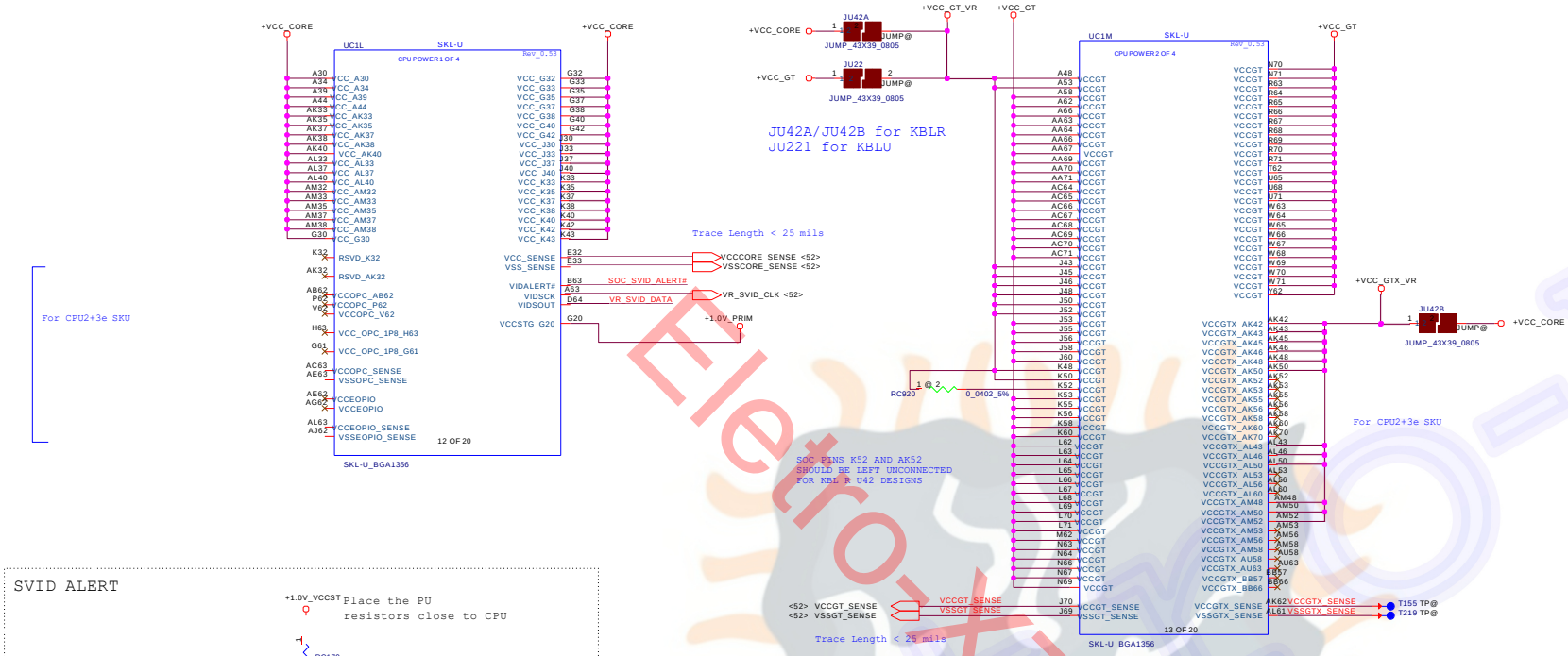
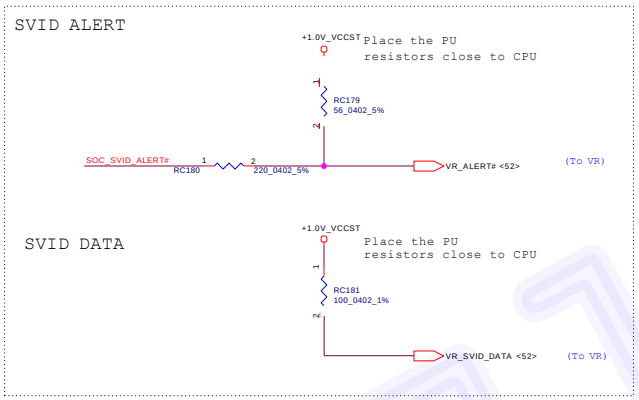
Eletro-X





Ball #	Ball Names R-U42	Ball Names U22	R-U42/U22 common board guidelines
C7	XTAL24_OUT	NC	connect to R-U42 XTAL24_OUT
E3	XTAL24_IN	NC	connect to R-U42 XTAL24_IN
E35	NC	XTAL24_OUT	connect to U22 XTAL24_OUT
E37	NC	XTAL24_IN	connect to U22 XTAL24_IN
AK42	VCCCORE	VccGTx	
AK43	VCCCORE	VccGTx	
AK45	VCCCORE	VccGTx	
AK46	VCCCORE	VccGTx	
AK48	VCCCORE	VccGTx	
AK50	VCCCORE	VccGTx	connect to VccGTx/VCCCORE
AL43	VCCCORE	VccGTx	power plane island
AL46	VCCCORE	VccGTx	
AL50	VCCCORE	VccGTx	
AM48	VCCCORE	VccGTx	
AM50	VCCCORE	VccGTx	
AM52	VCCCORE	VccGTx	
J43	VCCCORE	VCCGT	
J45	VCCCORE	VCCGT	
J46	VCCCORE	VCCGT	
J48	VCCCORE	VCCGT	
J50	VCCCORE	VCCGT	connect to VccGT/VCCCORE
J52	VCCCORE	VCCGT	power plane island
K48	VCCCORE	VCCGT	
K50	VCCCORE	VCCGT	
A48	VCCCORE	VCCGT	
A53	VCCCORE	VCCGT	
AK52	RSVD	VccGTx	**Must Not Be Connected**. RVP use this signal for debug and testing purpose only.
K52	RSVD	VCCGT	**Must Not Be Connected**. RVP use this signal for debug and testing purpose only.

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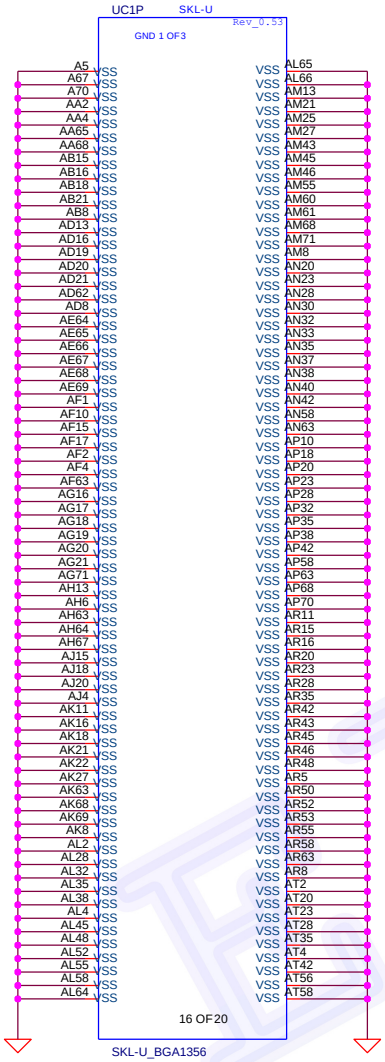
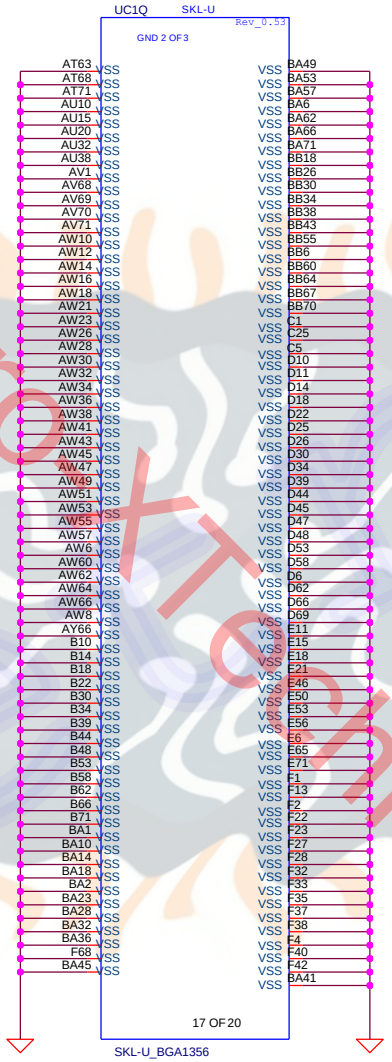
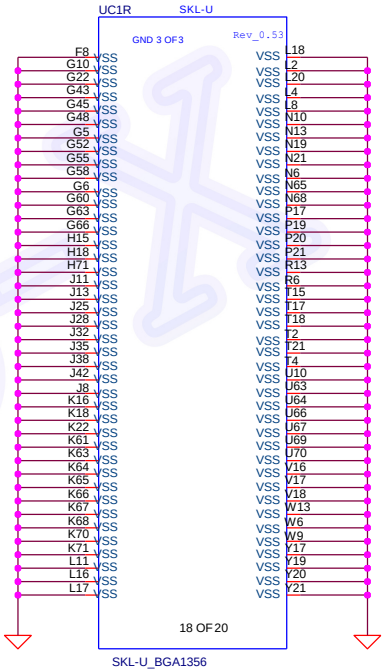
			Date: Friday, January 05, 2018; Sheet 14 of 59







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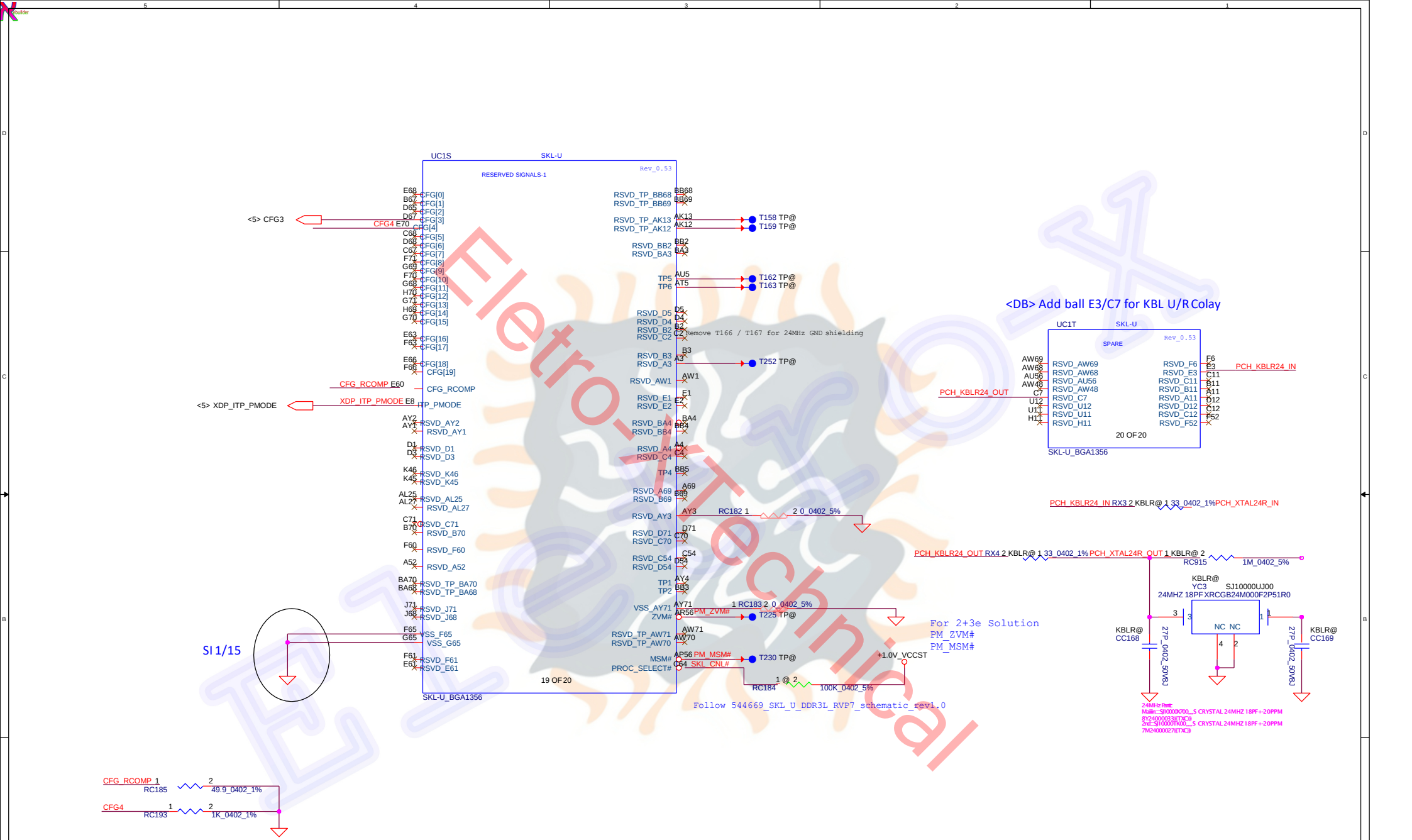

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Size: Custom | Document Number: EPK52_LA-G07EP | Rev: 0.3

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CHANNEL-A

REVERSE TYPE

Interleaved Memory

TOP: JDIMM1 CONN Non-ECC DIMM

PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

Layout Note:
PLACE THE CAP near JDIMM1. 164

Layout Note:
Place near JDIMM1

PLACE NEAR TO PIN

PLACE NEAR TO SODIMM

9/8 Modify

For ECC DIMM

DIMM Side

CPU Side

VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

Part Number:LTCX0069GA0
Part Value:S SOCKET FOX AS0A827-H2RB-7H 260P DDR4

FOX_AS0A827-H2RB-7H
CONN@

Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: P18-DDRIV_CHA: DMM0

Size: Document Number: EPK52_LA-G07EP

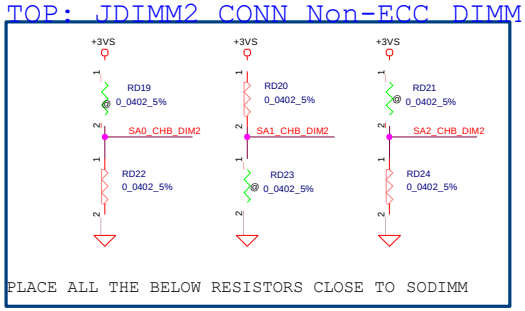
Date: Friday, January 05, 2018 Sheet 17 of 54

CHANNEL-B

Interleaved Memory

STD (5.2 mm)

TOP: JDIMM2 CONN Non-ECC DIMM

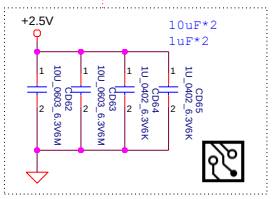


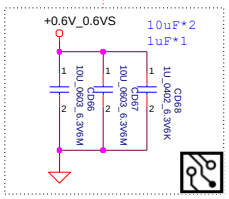
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

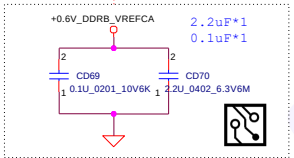
Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.258

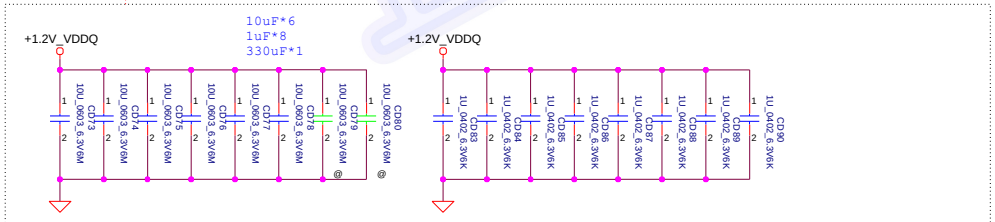


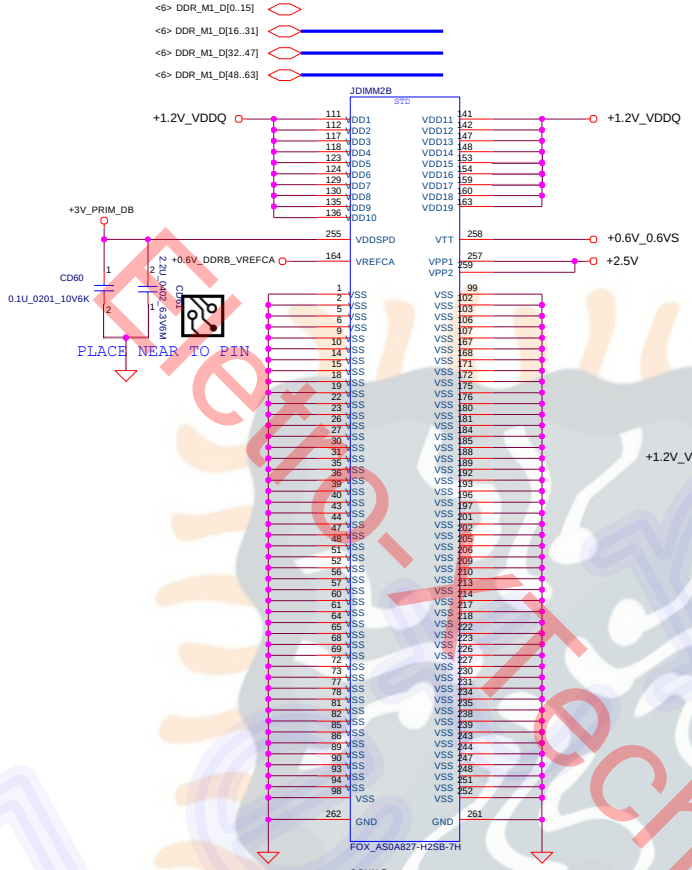


Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2

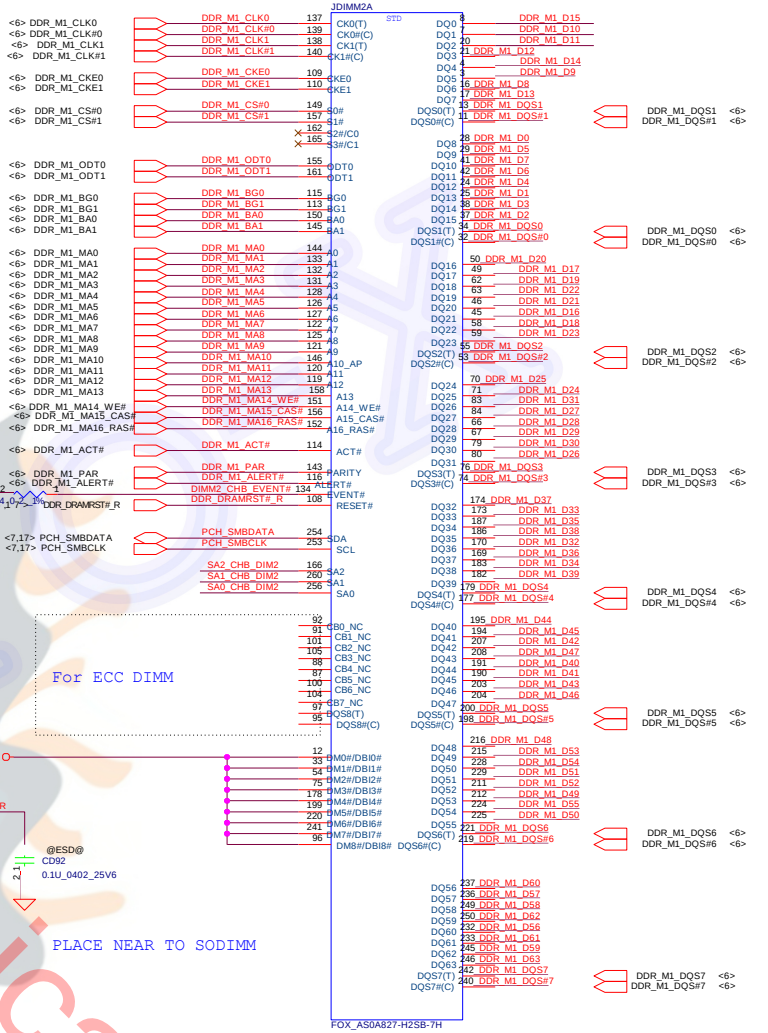


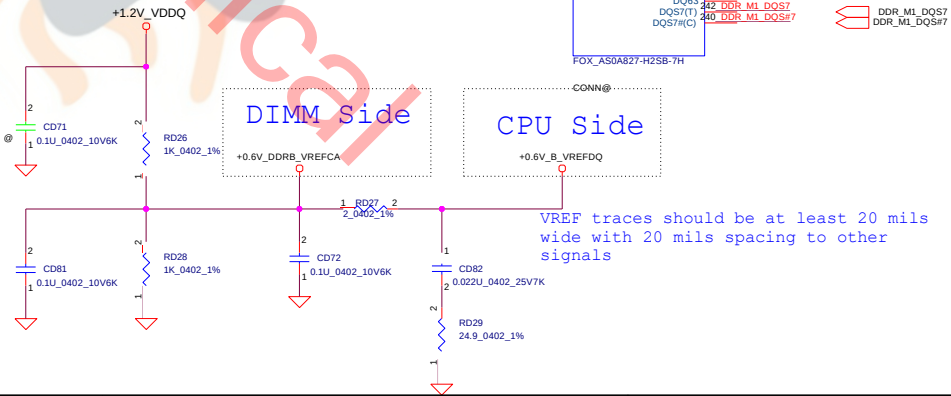
Layout Note:
Place near JDIMM2





Part Number:LTCX0069FA0
Part Value:S SOCKET FOX AS0A827-H2SB-7H 260P DDR4





VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

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Title: P19-DDRIV_CHB: DIMM0
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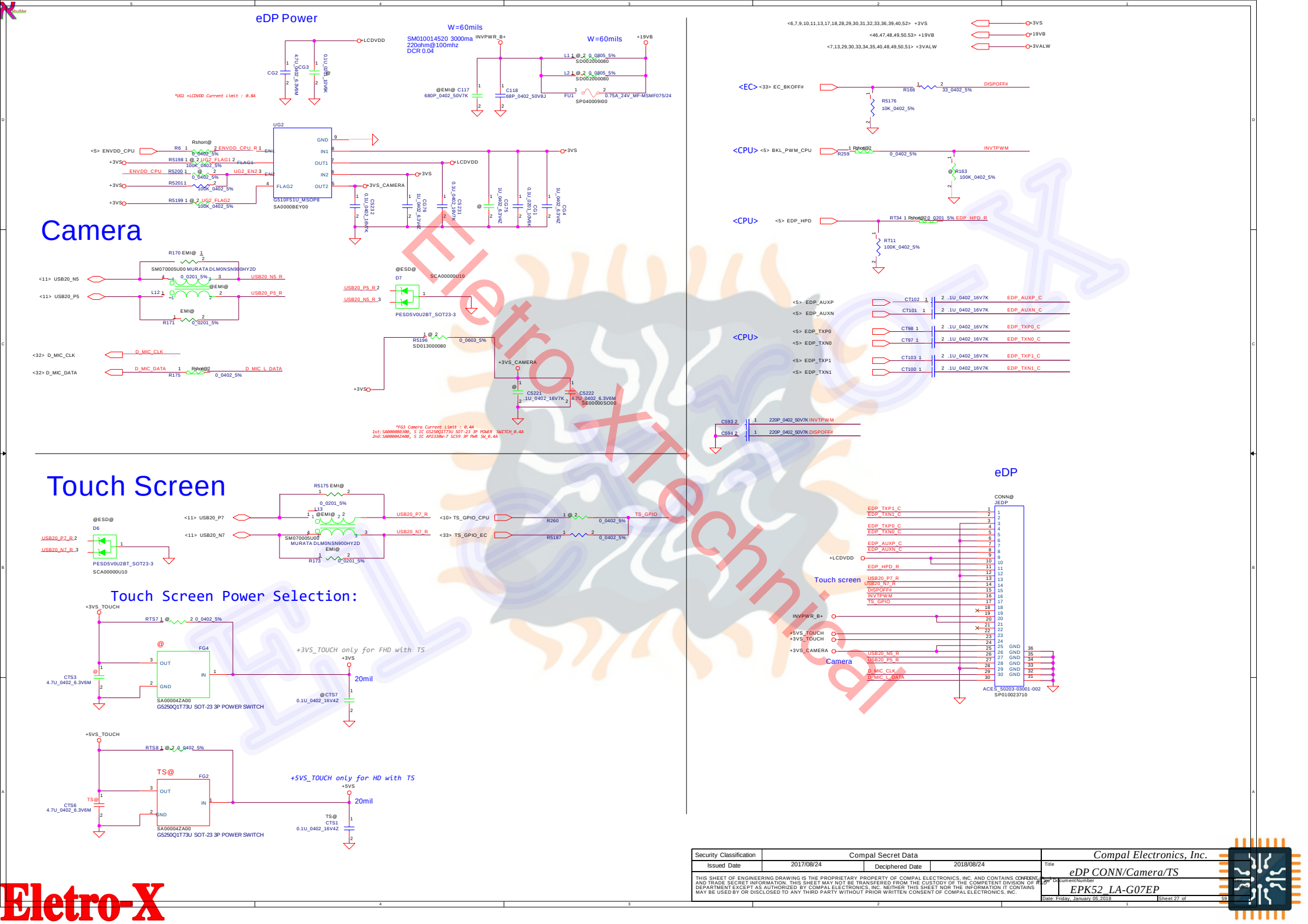

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.	
Title	eDP CONN/Camera/TS
Size	Document Number: EPK52_LA-G07EP
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<CPU>
<5> HOST_DP1_P0 — HOST_DP1_P0 0.1U_0402_16V7K 1 2 CG8 — HDMI_TX_P2
<5> HOST_DP1_N0 — HOST_DP1_N0 0.1U_0402_16V7K 1 2 CG9 — HDMI_TX_N2
<5> HOST_DP1_P1 — HOST_DP1_P1 0.1U_0402_16V7K 1 2 CG10 — HDMI_TX_P1
<5> HOST_DP1_N1 — HOST_DP1_N1 0.1U_0402_16V7K 1 2 CG11 — HDMI_TX_N1
<5> HOST_DP1_P2 — HOST_DP1_P2 0.1U_0402_16V7K 1 2 CG12 — HDMI_TX_P0
<5> HOST_DP1_N2 — HOST_DP1_N2 0.1U_0402_16V7K 1 2 CG13 — HDMI_TX_N0
<5> HOST_DP1_P3 — HOST_DP1_P3 0.1U_0402_16V7K 1 2 CG14 — HDMI_CLKP
<5> HOST_DP1_N3 — HOST_DP1_N3 0.1U_0402_16V7K 1 2 CG15 — HDMI_CLKN

RP1 470_0804_8P4R_5% RP2 470_0804_8P4R_5%

QG1B SB00001FF00
L2N7002SDW1T1G 2N SC88-6

+3VS

1.3.2 Digital Display Interface Signal Mapping

Table 1-4. Digital Display Interface Signal Mapping

Port	DDI PROCESSOR Pin Names	Display Port Mapping	HDMI* Mapping
Port 1	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIxC_TX2_DN
	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIxC_TX2_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIxC_TX1_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIxC_TX1_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIxC_TX0_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIxC_TX0_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIxC_CLK_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIxC_CLK_DP
	DDPB_HPD	DDI1_HPD_Q	DDI1_HPD_Q
	DDPB_CTRLCLK	NA	DDI1_CTRL_CK
	DDPB_CTRLDATA	NA	DDI1_CTRL_DATA

DDI_0 → HDMI_2; DDI_3 → HDMI_0 CLK

*DDA30_LA-F292PR02: RS_8.2ohm_RP_360ohm

HDMI_CLKP — RG59 1 EMI@ 2 15 +-1% 0402 — HDMI_R_CLKP
CG71 EMI@ 360 +-5% 0402 SD028360080
HDMI_CLKN — RG60 1 EMI@ 2 15 +-1% 0402 — HDMI_R_CLKN
HDMI_TX_N2 — RG63 1 EMI@ 2 15 +-1% 0402 — HDMI_R_TX_N2
CG72 EMI@ 360 +-5% 0402 SD028360080
HDMI_TX_P2 — RG61 1 EMI@ 2 15 +-1% 0402 — HDMI_R_TX_P2
HDMI_TX_P1 — RG65 1 EMI@ 2 15 +-1% 0402 — HDMI_R_TX_P1
CG73 EMI@ 360 +-5% 0402 SD028360080
HDMI_TX_N1 — RG10 1 EMI@ 2 15 +-1% 0402 — HDMI_R_TX_N1
HDMI_TX_P0 — RG12 1 EMI@ 2 15 +-1% 0402 — HDMI_R_TX_P0
CG74 EMI@ 360 +-5% 0402 SD028360080
HDMI_TX_N0 — RG13 1 EMI@ 2 15 +-1% 0402 — HDMI_R_TX_N0

@ESD@ D21
HDMI_R_TX_N0 1 — 10 9 HDMI_R_TX_N0
HDMI_R_TX_P0 2 — 9 8 HDMI_R_TX_P0
HDMI_R_CLKN 4 — 7 7 HDMI_R_CLKN
HDMI_R_CLKP 5 — 6 6 HDMI_R_CLKP
3
AZ1045-04F.R7G DFN2510P10E ESD
SC300001Y00

@ESD@ D22
HDMI_R_TX_N1 1 — 10 9 HDMI_R_TX_N1
HDMI_R_TX_P1 2 — 9 8 HDMI_R_TX_P1
HDMI_R_TX_N2 4 — 7 7 HDMI_R_TX_N2
HDMI_R_TX_P2 5 — 6 6 HDMI_R_TX_P2
3
AZ1045-04F.R7G DFN2510P10E ESD
SC300001Y00

@ESD@ DG1
HP_DETECT 1 — 10 9 HP_DETECT
HDMI_CTRL_DAT 2 — 9 8 HDMI_CTRL_DAT
HDMI_CTRL_CLK 4 — 7 7 HDMI_CTRL_CLK
5 6
3
AZ1045-04F.R7G DFN2510P10E ESD
SC300001Y00

W=40mils

FG1
+5VS — 1 IN; OUT 3 — +HDMI_CRT_5V
GND 2
AP2330W-7_SC59-3
SA00004ZA00
CG46 0.1U_0402_16V7K
CG47 4.7U_0402_6.3V6M

<6,7,9,10,11,13,17,18,27,29,30,31,32,33,36,39,40,52> +3VS
<27,32,33,34,36,37,40> +5VS

+3VS
RG47 1M_0402_5%
<5> HOST_DP1_HPD — QG1A L2N7002SDW1T1G 2N SC88-6 SB00001FF00 — HDMI_HPD
5V Level
RG108 10K_0402_5%
HP_DETECT
RG56 20K_0402_5%
@ CM17 220P_0402_50V7K

<5> HOST_DP1_CTRL_CLK — HOST_DP1_CTRL_CLK — QG2A SB00001FF00 L2N7002SDW1T1G 2N SC88-6 — HDMI_CTRL_CLK
+3VS
<5> HOST_DP1_CTRL_DATA — HOST_DP1_CTRL_DATA — QG2B SB00001FF00 L2N7002SDW1T1G 2N SC88-6 — HDMI_CTRL_DAT

+HDMI_CRT_5V
+3VS
RG105 2.2K_0804_8P4R_5%
HDMI_CTRL_CLK
HDMI_CTRL_DAT
HOST_DP1_CTRL_CLK
HOST_DP1_CTRL_DATA

HDMI Conn.

JHDMI_CONN@
HP_DETECT — 19 HP_DET
+HDMI_CRT_5V — 18 5V
HDMI_CTRL_DAT — 16 SDA
HDMI_CTRL_CLK — 15 SCL
14 Utility
13 CEC
HDMI_R_CLKN — 12 CK-
HDMI_R_CLKP — 11 CK_shield
HDMI_R_TX_N0 — 10 CK+
9 D0-
HDMI_R_TX_P0 — 8 D0_shield
HDMI_R_TX_N1 — 7 D0+
6 D1-
HDMI_R_TX_P1 — 5 D1_shield
HDMI_R_TX_N2 — 4 D1+
3 D2-
HDMI_R_TX_P2 — 2 D2_shield
1 D2+
GND1 23
GND2 22
GND3 21
GND4 20
ACON_HMRBL-AK120H
DC231709273

@ CM26 10P_0402_50V8J
@ CM27 10P_0402_50V8J

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Title: HDMI Conn/Level shift
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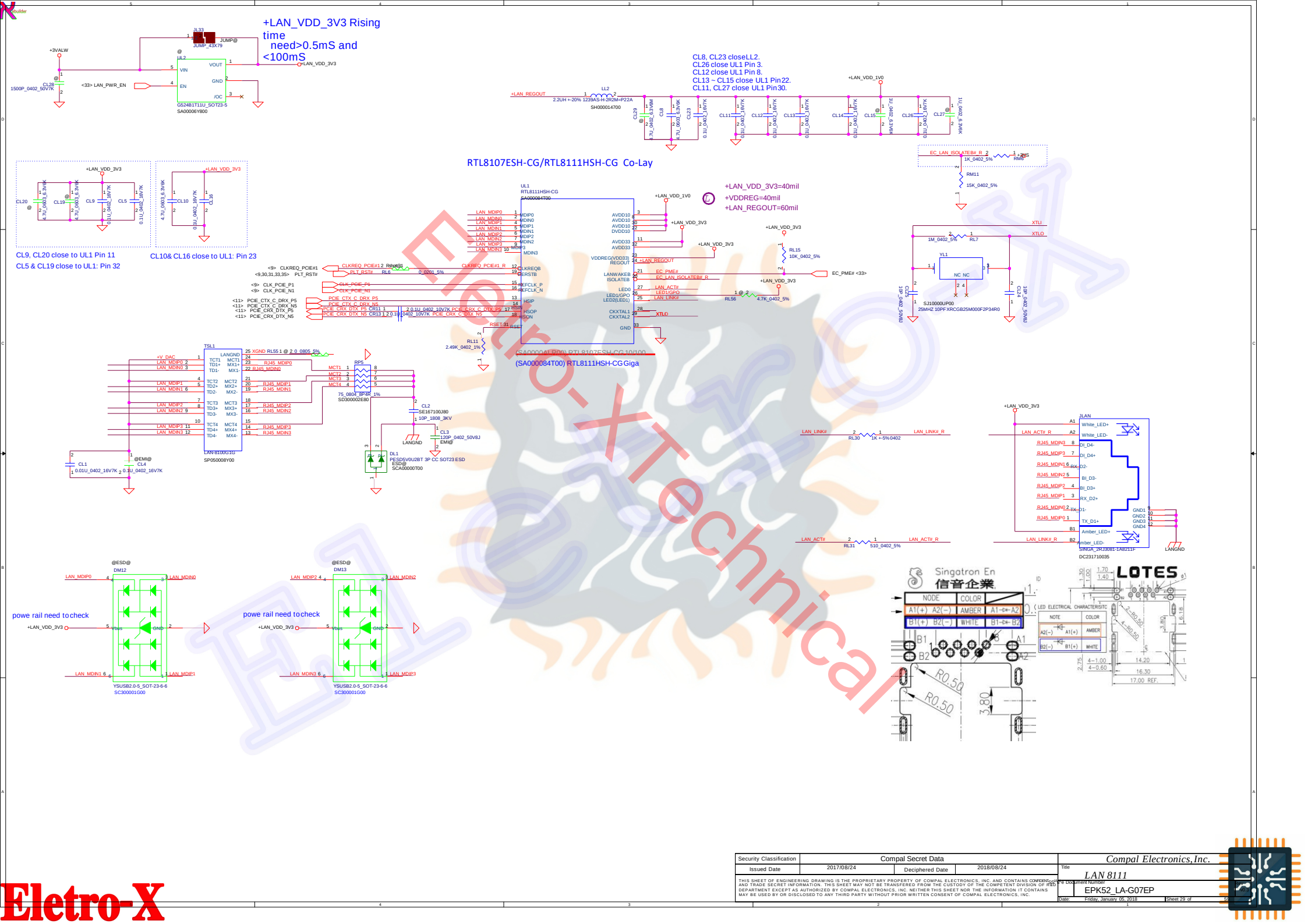
Date: Friday, January 05, 2018 Sheet 28 of 59


+LAN_VDD_3V3 Rising time need>0.5mS and <100mS
CL8, CL23 closeLL2.
CL26 close UL1 Pin 3.
CL12 close UL1 Pin 8.
CL13 ~ CL15 close UL1 Pin22.
CL11, CL27 close UL1 Pin30.
RTL8107ESH-CG/RTL8111HSH-CG Co-Lay
+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil
CL9, CL20 close to UL1 Pin 11
CL5 & CL19 close to UL1: Pin 32
CL10& CL16 close to UL1: Pin 23
(SA000084T00) RTL8111HSH-CG Giga
powe rail need to check
powe rail need to check
Singatron En
信音企業
LOTES
Compal Electronics, Inc.
LAN 8111
EPK52_LA-G07EP
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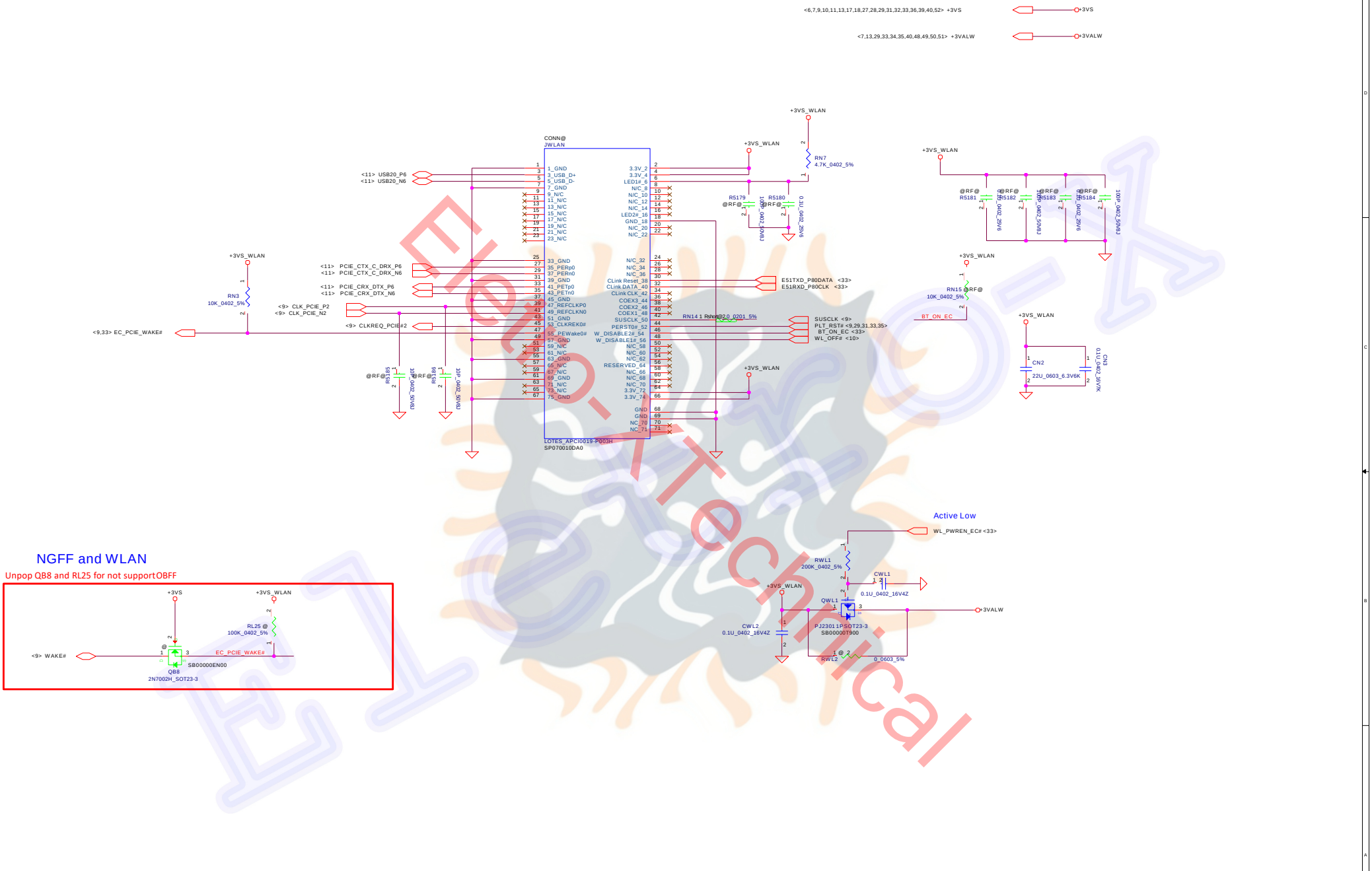

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Title: WLAN-BT

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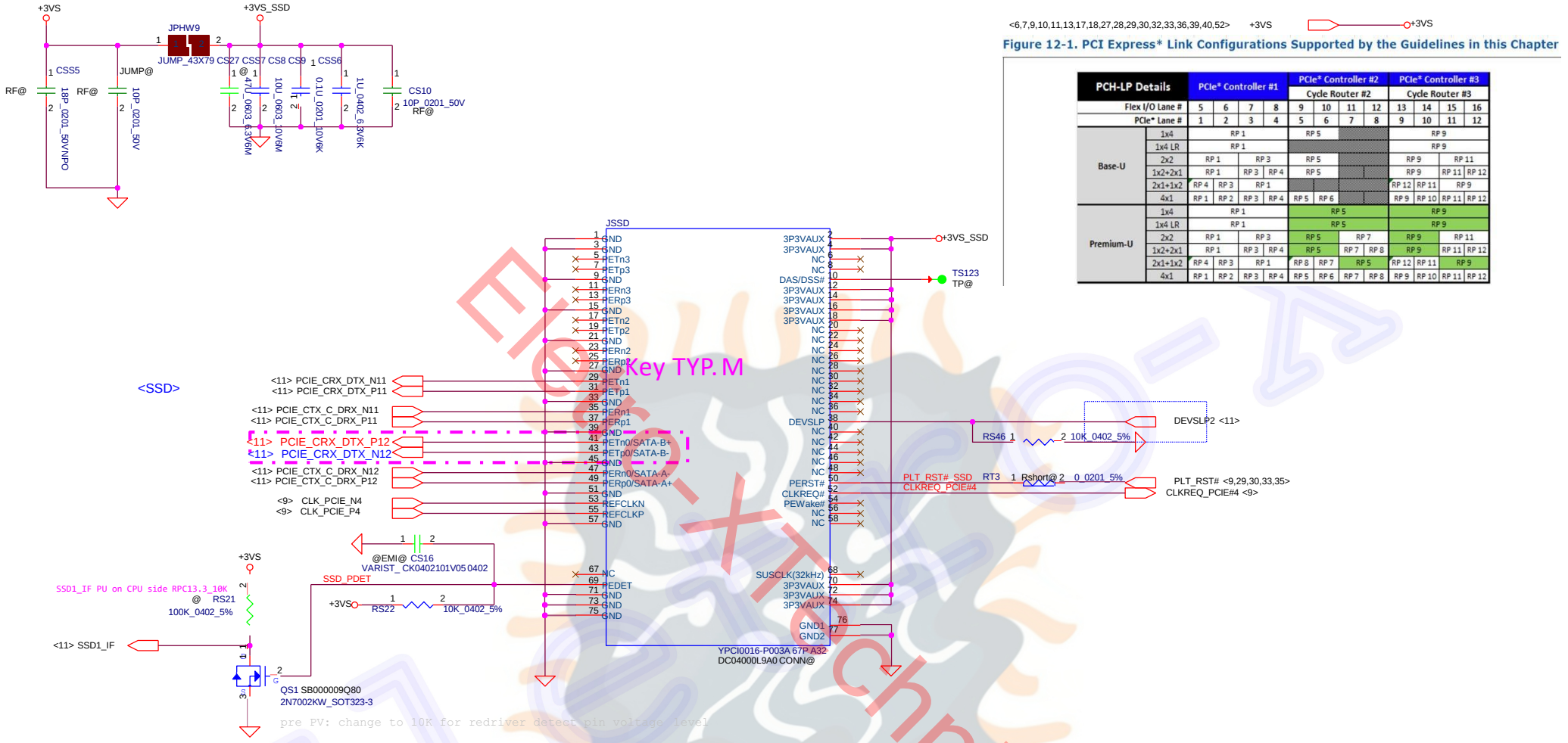

<6,7,9,10,11,13,17,18,27,28,29,30,32,33,36,39,40,52> +3VS +3VS

Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2 Cycle Router #2				PCIe* Controller #3 Cycle Router #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP 1				RP 5				RP 9			
	1x4 LR	RP 1								RP 9			
	2x2	RP 1		RP 3		RP 5				RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5				RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1						RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6			RP 9	RP 10	RP 11	RP 12
Premium-U	1x4	RP 1				RP 5				RP 9			
	1x4 LR	RP 1				RP 5				RP 9			
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12

39	GND	PCIeMVMe_DD90000NU90_MZVLW1T0HMLH-000H1 F73H1Q 0FH		
41	PETn0	PCIe TX	42	N/C
43	PETp0	PCIe TX	44	N/C
45	GND	Return current path	46	N/C
47	PERn0	PCIe Rx	48	N/C
49	PERp0	PCIe Rx	50	PERST#
51	GND	Return current path	52	CLKREQ#

39	GND	Return Current Path	40
41	+B TXP	Transmitter Differential Signal Pair	42
43	-B TXN	Transmitter Differential Signal Pair	44
45	GND	Return Current Path	46
47	+A RXN	Receiver Differential Signal Pair	48
49	+A RXP	Receiver Differential Signal Pair	50
51	GND	Return Current Path	52

36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

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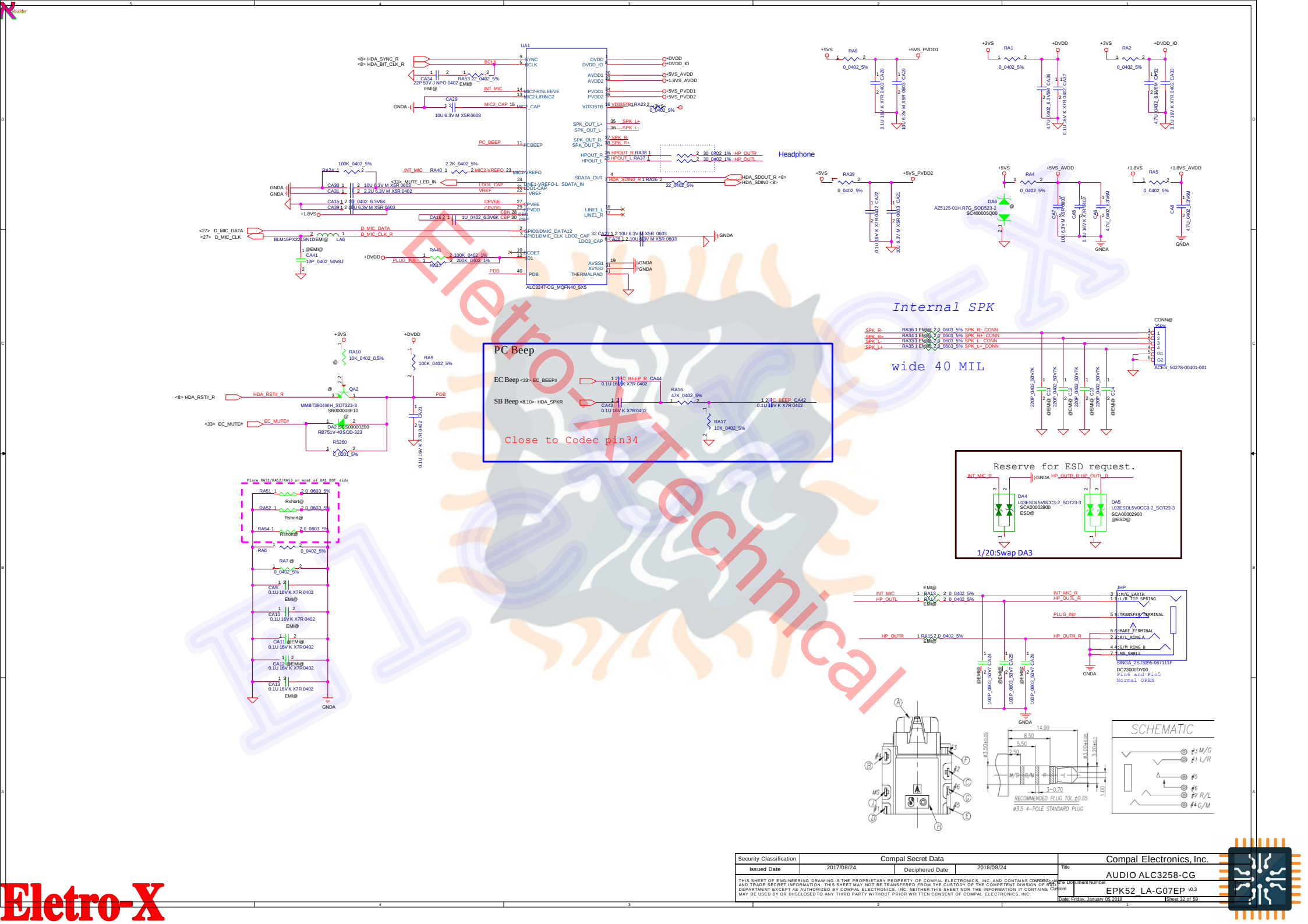

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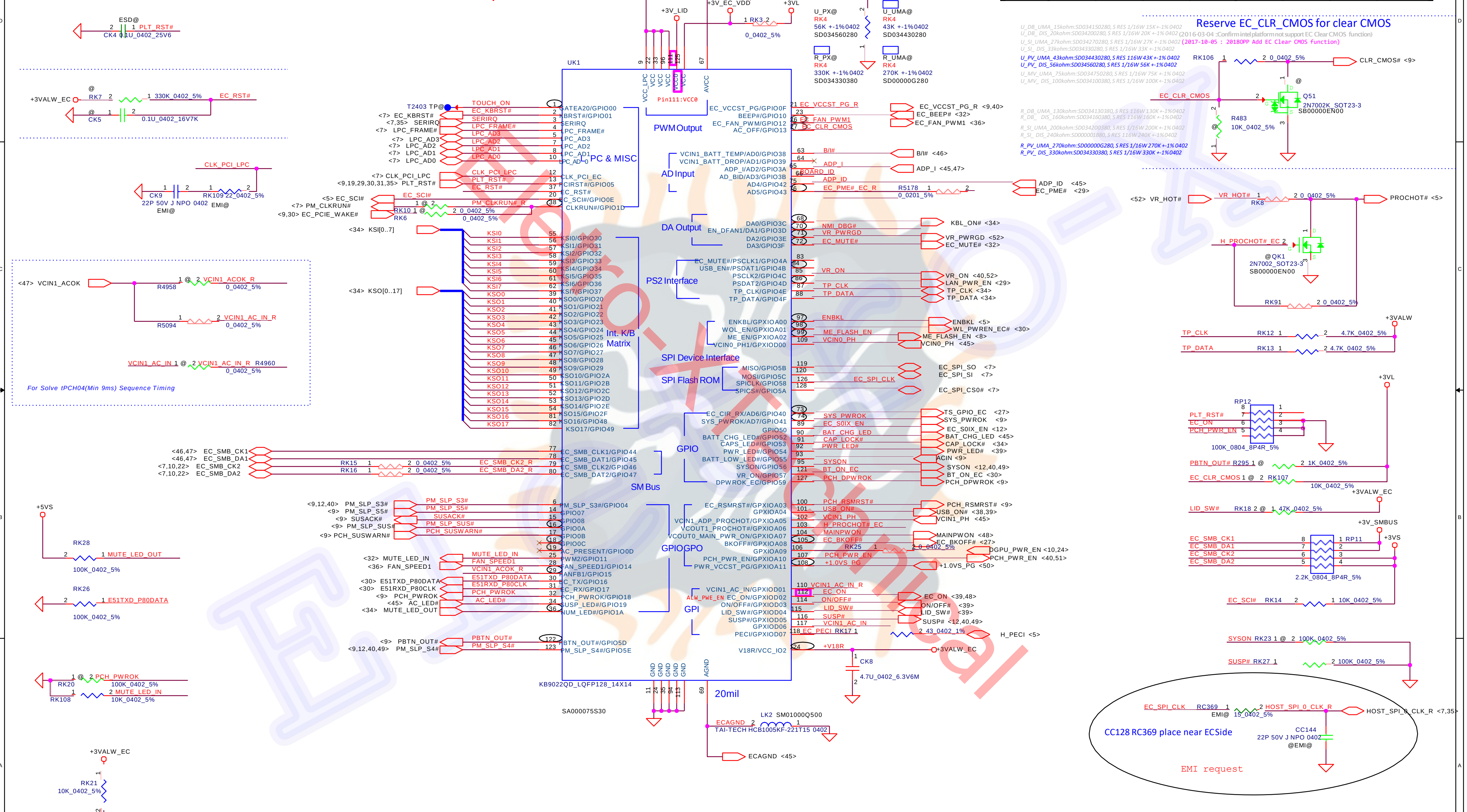
EC Board ID (UMA, DIS, phase) control table

RK4	KBL-U				KBL-R			
	DB	SI	PV	MV	DB	SI	PV	MV
UMA	15K	27K	43K	75K	130K	200K	270K	430K
DIS	20K	33K	56K	100K	160K	240K	330K	560K



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Title: EC ENE-KB9022

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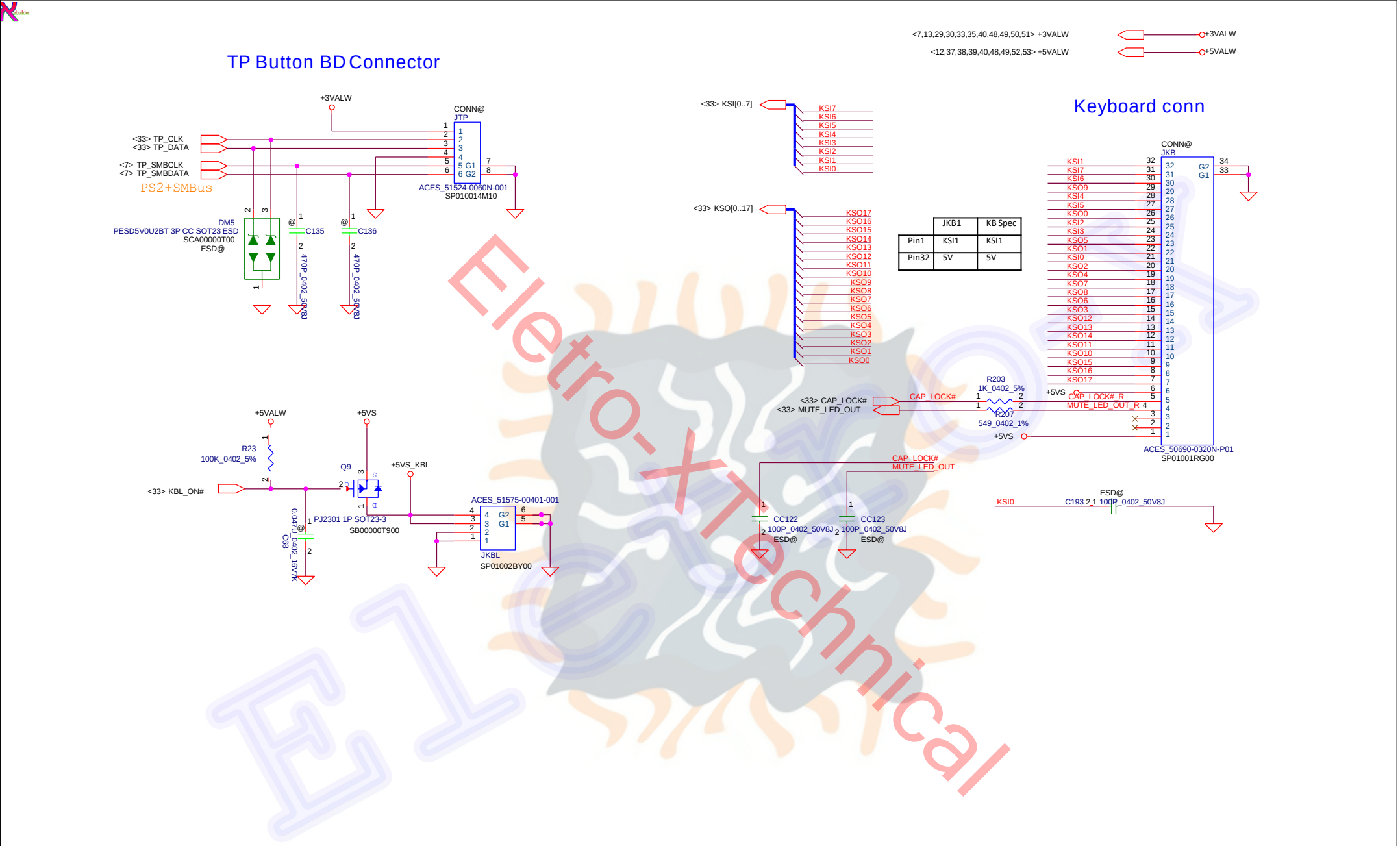

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Compal Electronics, Inc.

Title: KB/TP

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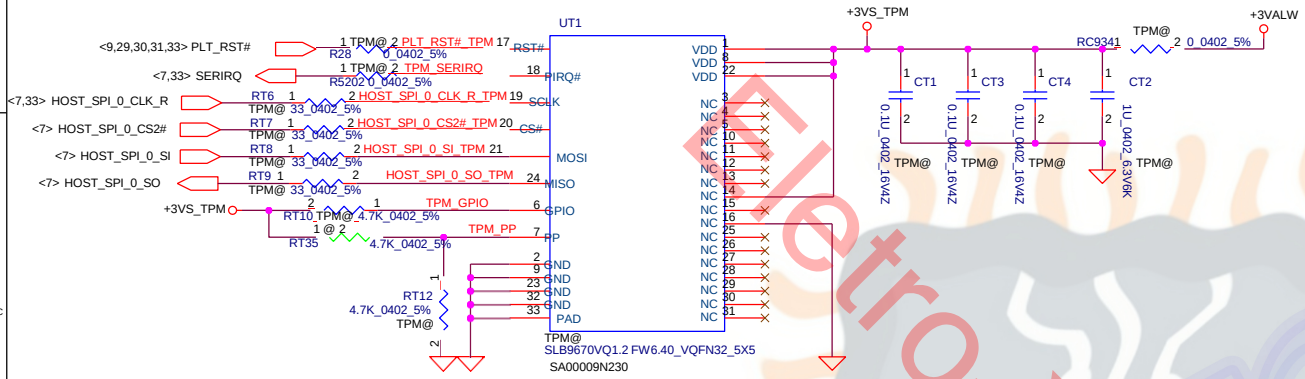
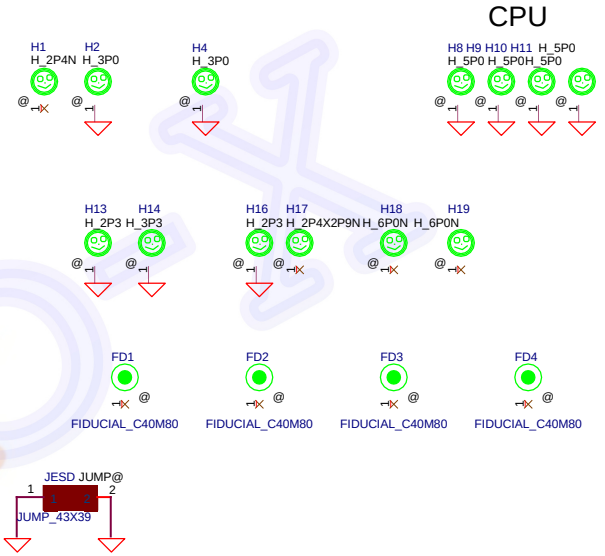
+3VALW +3VALW <7,13,29,30,33,34,40,48,49,50,51>

TPM2.0



Screw Hole



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Compal Electronics, Inc.

Title: TPM/Screw

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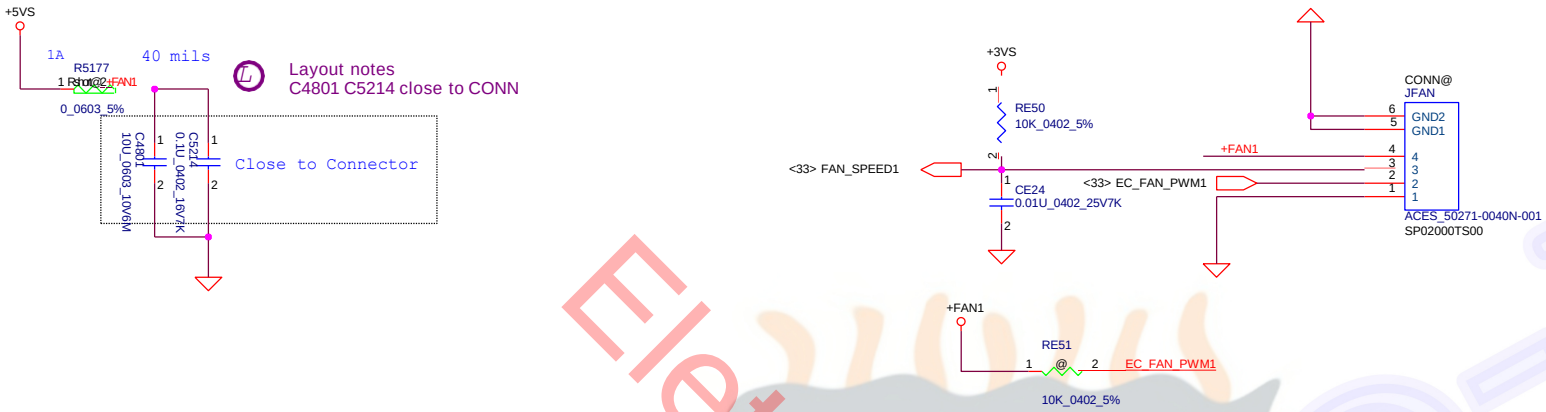

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Title: FAN

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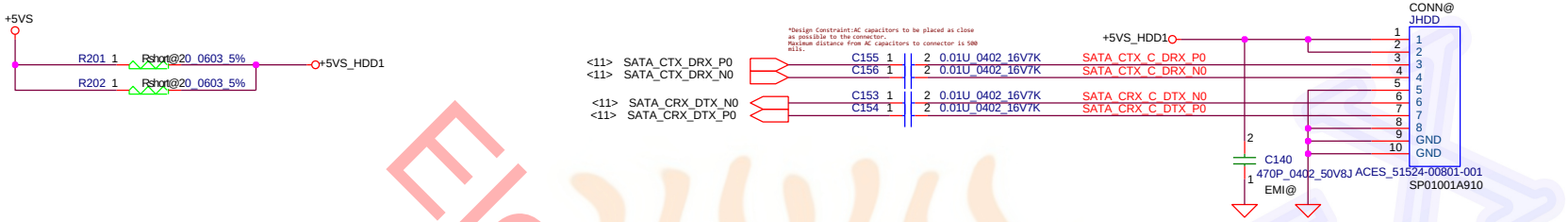
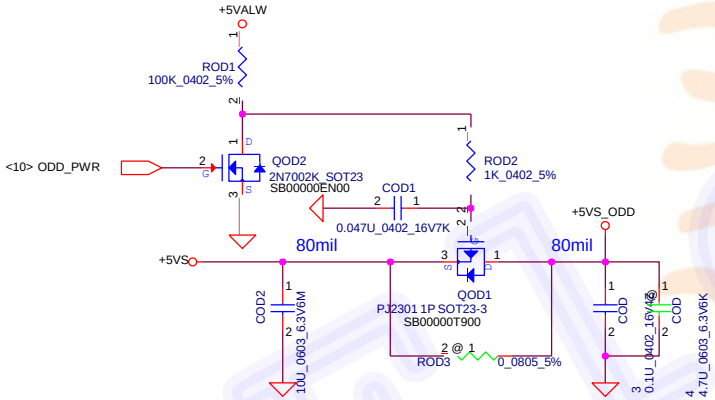
2.5" SATA HDD

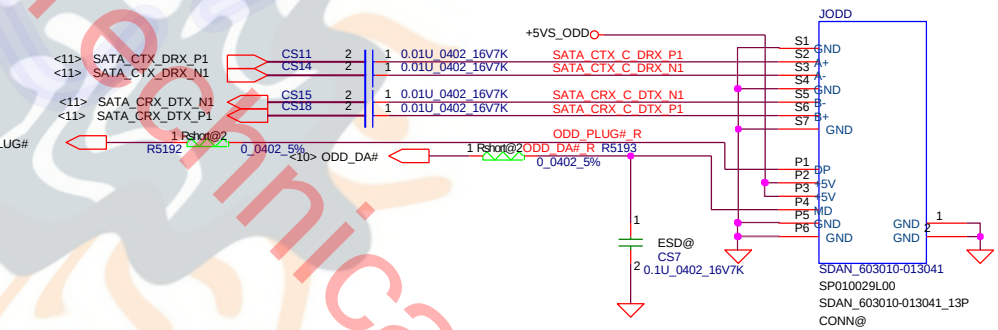
<27,28,32,33,34,36,40> +5VS
<12,34,38,39,40,48,49,52,53> +5VALW
<7,13,29,30,33,34,35,40,48,49,50,51> +3VALW

<PV> change short pad



SATA ODD





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Title: HDD/ODD Conn

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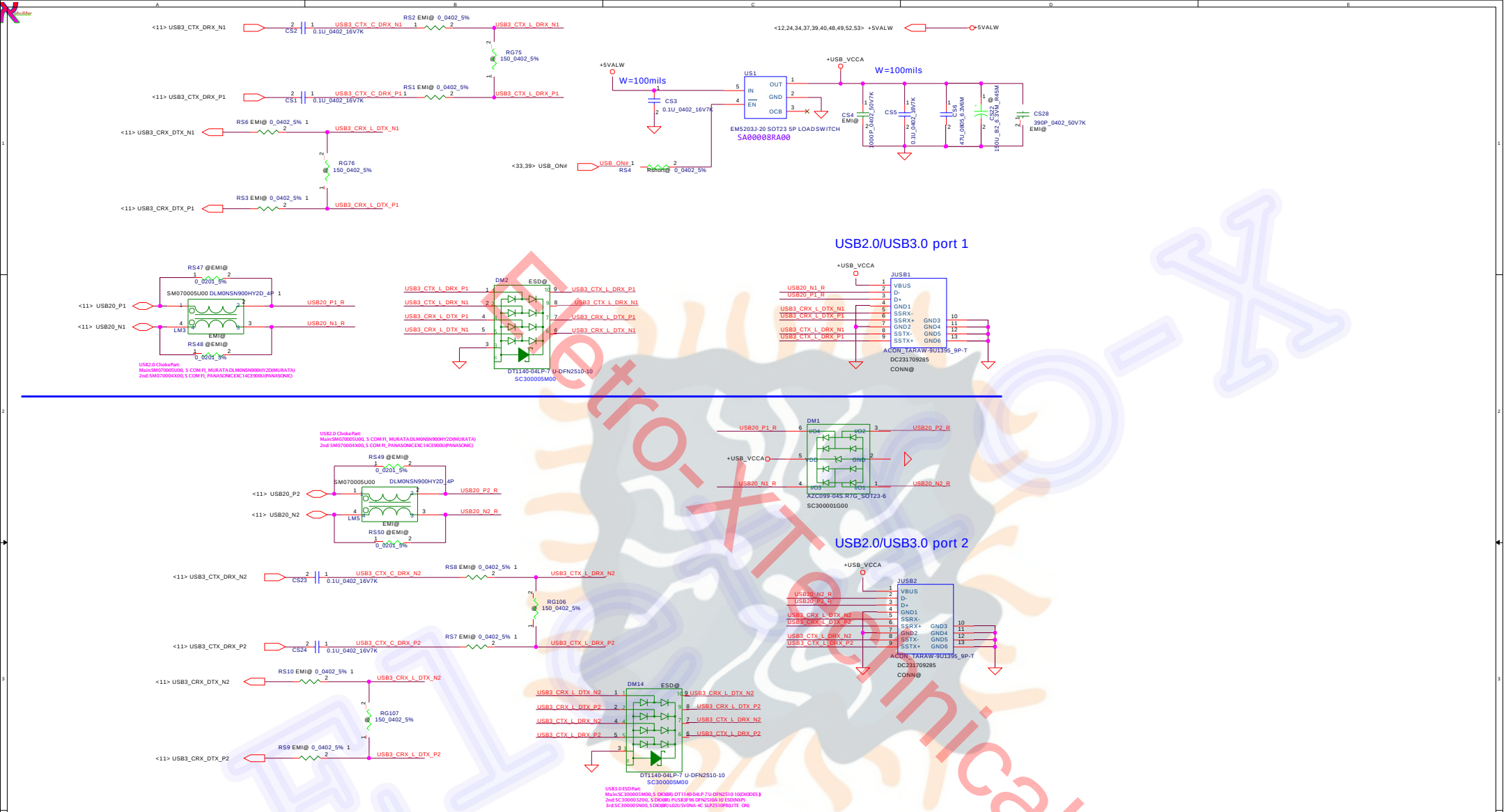

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Size	Custom	Document Number	EPK52_LA-G07EP
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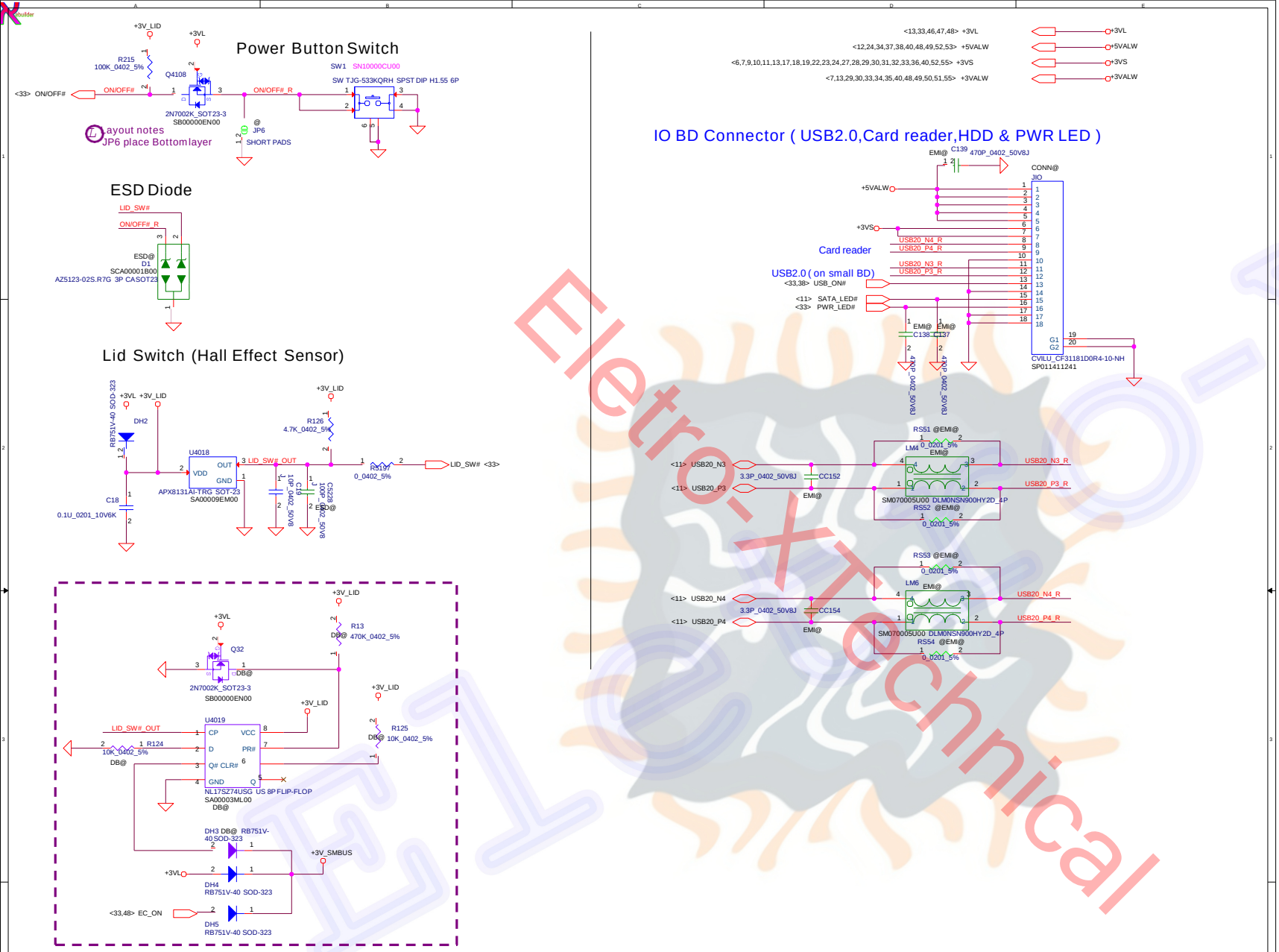

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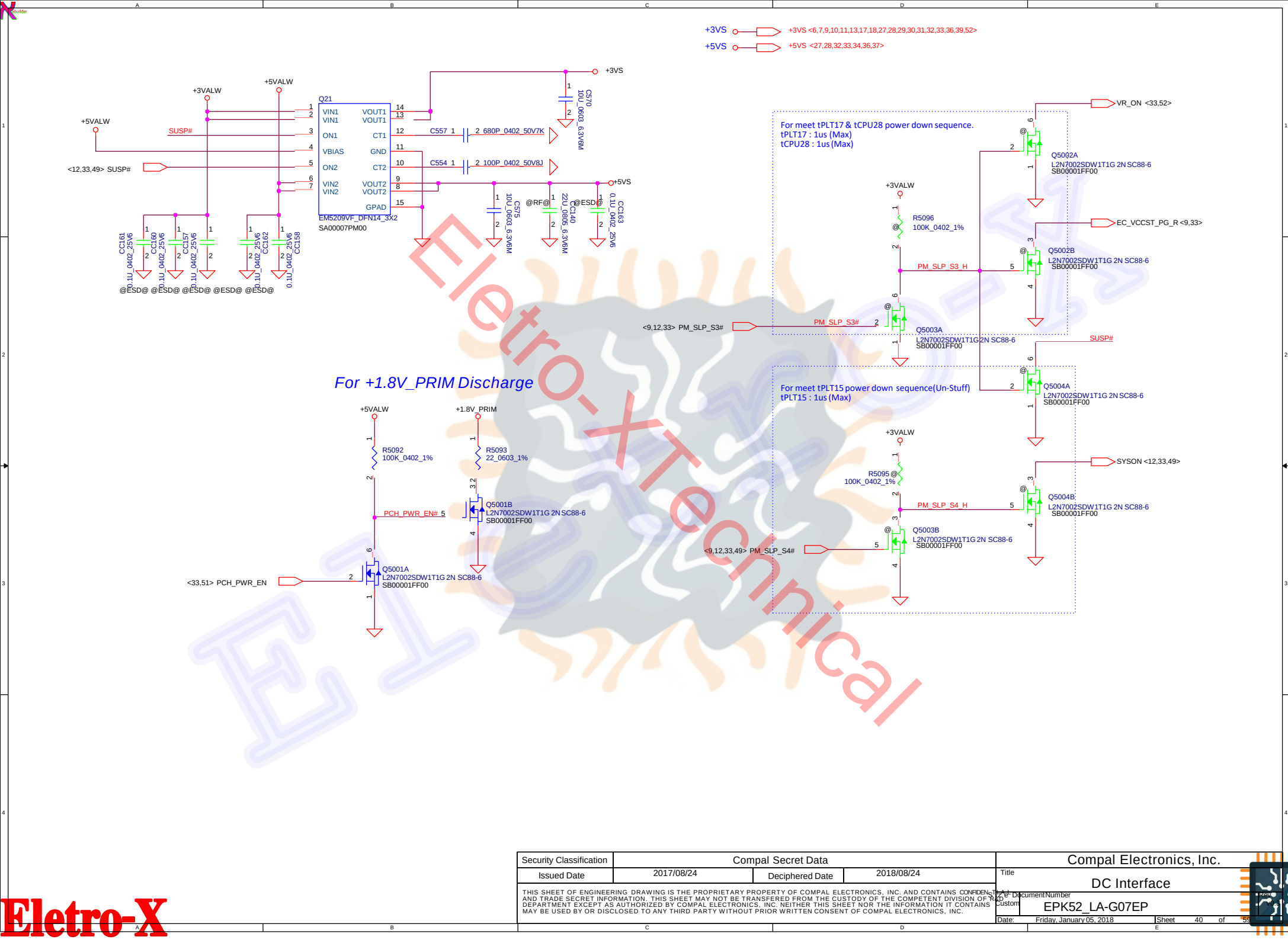

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Issued Date	2017/08/24	Deciphered Date	2018/08/24

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Title: DC Interface

Size: Custom | Document Number: EPK52_LA-G07EP | Rev: 1.0

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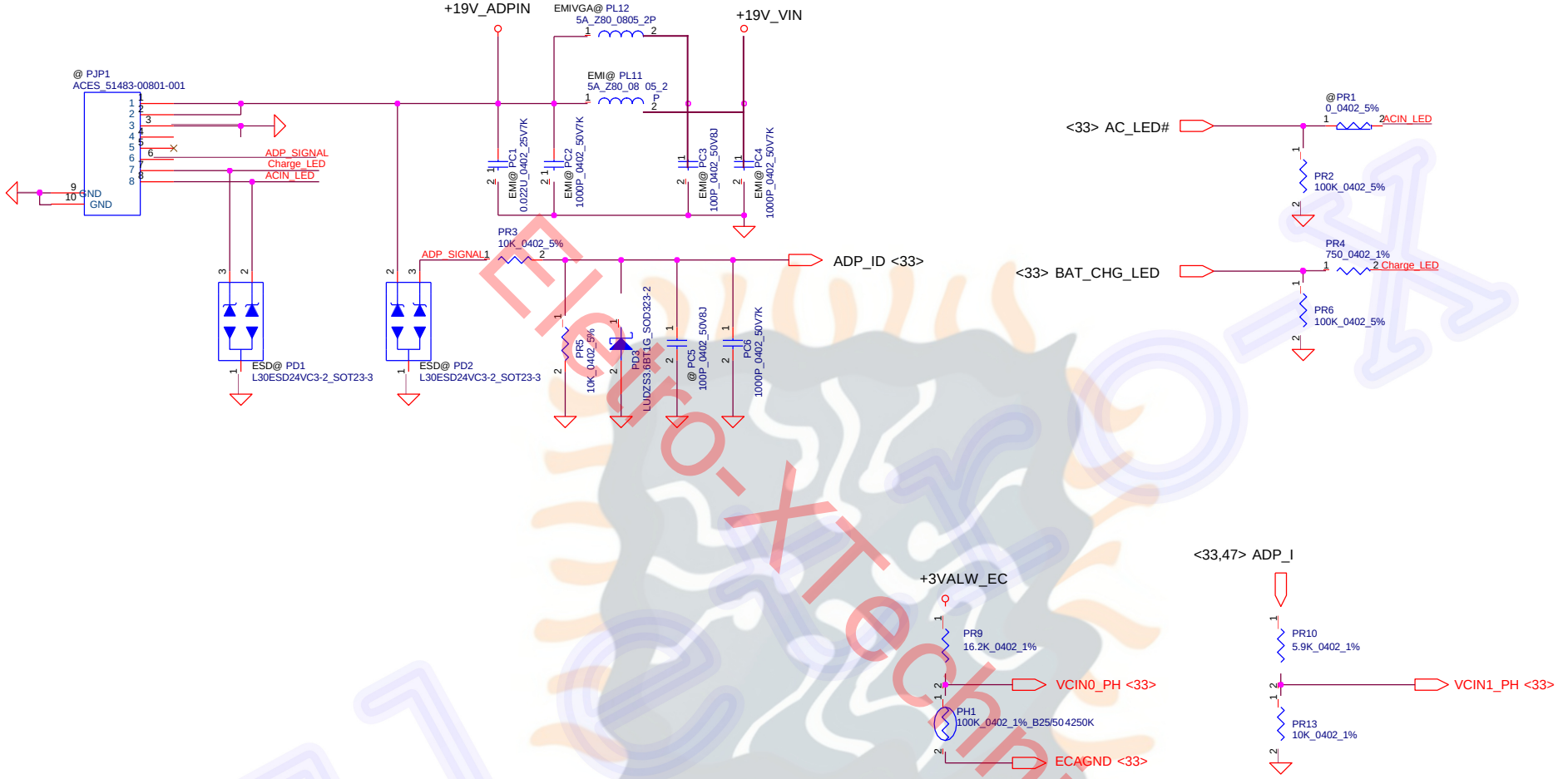

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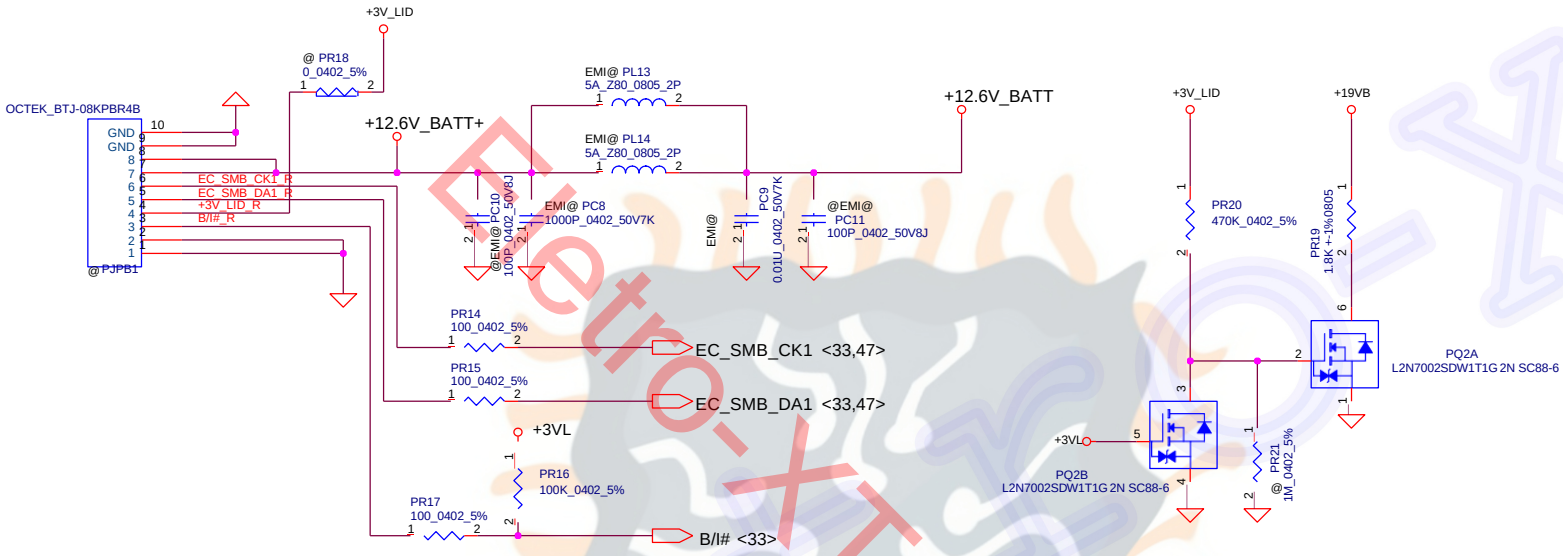

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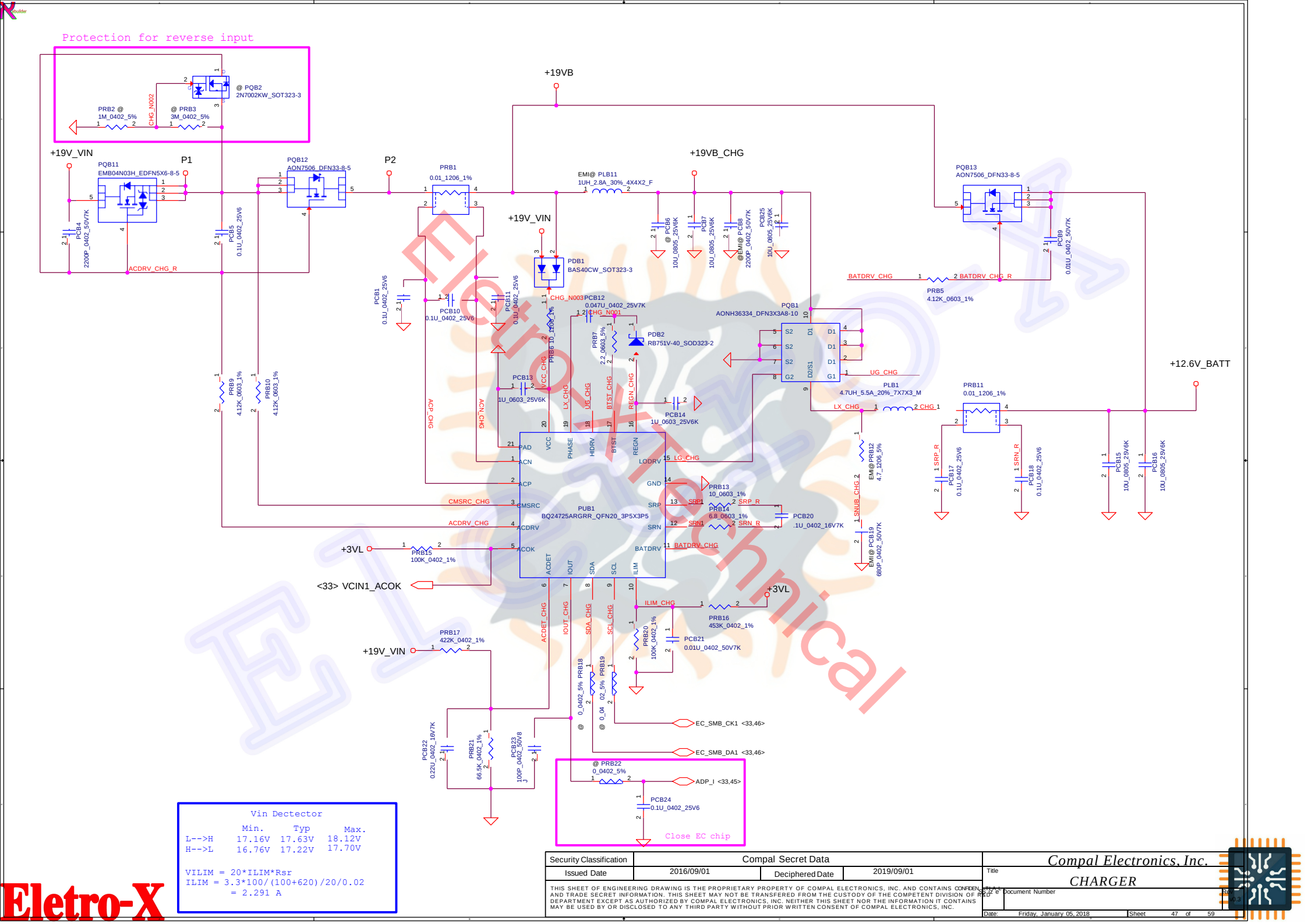
Protection for reverse input
@ PQB2
2N7002KW_SOT323-3
PRB2 @
1M_0402_5%
CHG_N002
@ PRB3
3M_0402_5%
+19V_VIN
PQB11
EMB04N03H_EDFN5X6-8-5
P1
PQB12
AON7506_DFN33-8-5
P2
PRB1
0.01_1206_1%
+19VB
EMI@ PLB11
1UH_2.8A_30%_4X4X2_F
+19VB_CHG
PQB13
AON7506_DFN33-8-5
PCB84
2200P_0402_50V7K
PCB85
0.1U_0402_25V6
ACDRV_CHG_R
PDB1
BAS40CW_SOT323-3
PCB86
10U_0805_25V6K
PCB87
10U_0805_25V6K
@EMI@ PCB88
2200P_0402_50V7K
PCB25
10U_0805_25V6K
PCB89
0.01U_0402_50V7K
BATDRV_CHG
PRB5
4.12K_0603_1%
BATDRV_CHG_R
PCB81
0.1U_0402_25V6
PCB810
0.1U_0402_25V6
PCB811
0.1U_0402_25V6
CHG_N003
PCB812
0.047U_0402_25V7K
CHG_N001
PQB1
AONH36334_DFN3X3A8-10
PRB9
4.12K_0603_1%
PRB10
4.12K_0603_1%
PRB7
2.2_0603_5%
PDB2
RB751V-40_SOD323-2
PCB13
1U_0603_25V6K
PCB14
1U_0603_25V6K
UG_CHG
PLB1
4.7UH_5.5A_20%_7X7X3_M
LX_CHG
CHG
+12.6V_BATT
PRB11
0.01_1206_1%
EM@PRB12
4.7_1206_5%
SNUB_CHG
EMI@ PCB19
680P_0402_50V7K
PCB15
10U_0805_25V6K
PCB16
10U_0805_25V6K
PRB17
422K_0402_1%
+19V_VIN
PCB22
0.22U_0402_16V7K
PRB21
66.5K_0402_1%
PCB23
100P_0402_50V8
PRB18
PRB19
@ PRB22
0_0402_5%
ADP_I <33,45>
PCB24
0.1U_0402_25V6
Close EC chip
+3VL
PRB15
100K_0402_1%
<33> VCIN1_ACOK
PRB16
453K_0402_1%
PRB20
100K_0402_1%
PCB21
0.01U_0402_50V7K
EC_SMB_CK1 <33,46>
EC_SMB_DA1 <33,46>
PUB1
BQ24725ARGRR_QFN20_3P5X3P5
PRB13
10_0603_1%
PRB14
6.8_0603_1%
PCB20
.1U_0402_16V7K
PCB17
0.1U_0402_25V6
PCB18
0.1U_0402_25V6
SRP_R
SRN_R
CMSRC_CHG
ACDRV_CHG
ACOK
ACDET
IOUT
SDA
SCL
ILIM
ACDET_CHG
IOUT_CHG
SDA_CHG
SCL_CHG
ILIM_CHG
LX_CHG
UG_CHG
BTST_CHG
REGN_CHG
LG_CHG
ACP_CHG
ACN_CHG
VCC_CHG
Vin Dectector
Min. Typ Max.
L-->H 17.16V 17.63V 18.12V
H-->L 16.76V 17.22V 17.70V
VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+620)/20/0.02
= 2.291 A
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2016/09/01
Deciphered Date
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Rev
0.3
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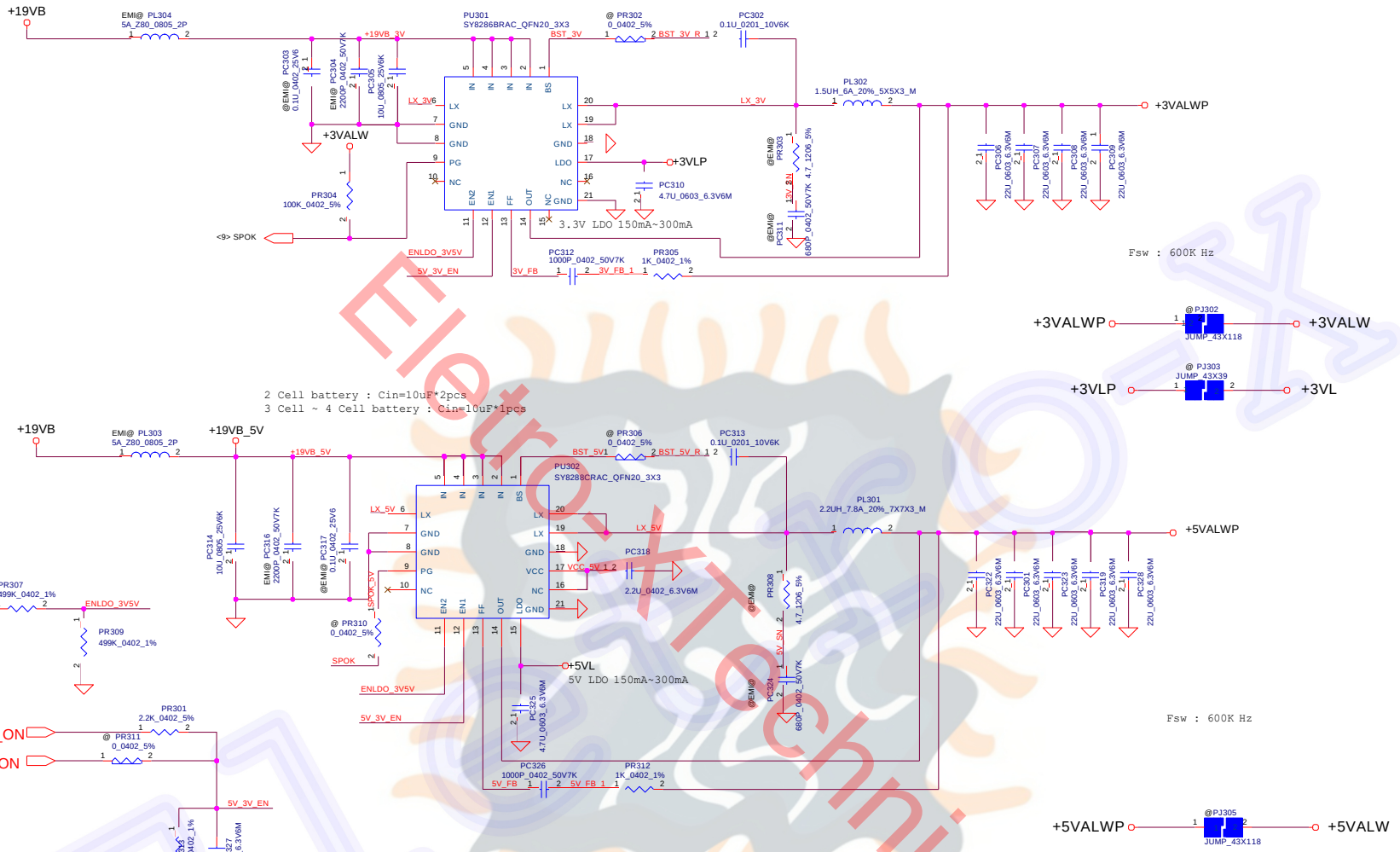
Eletro-X Technical



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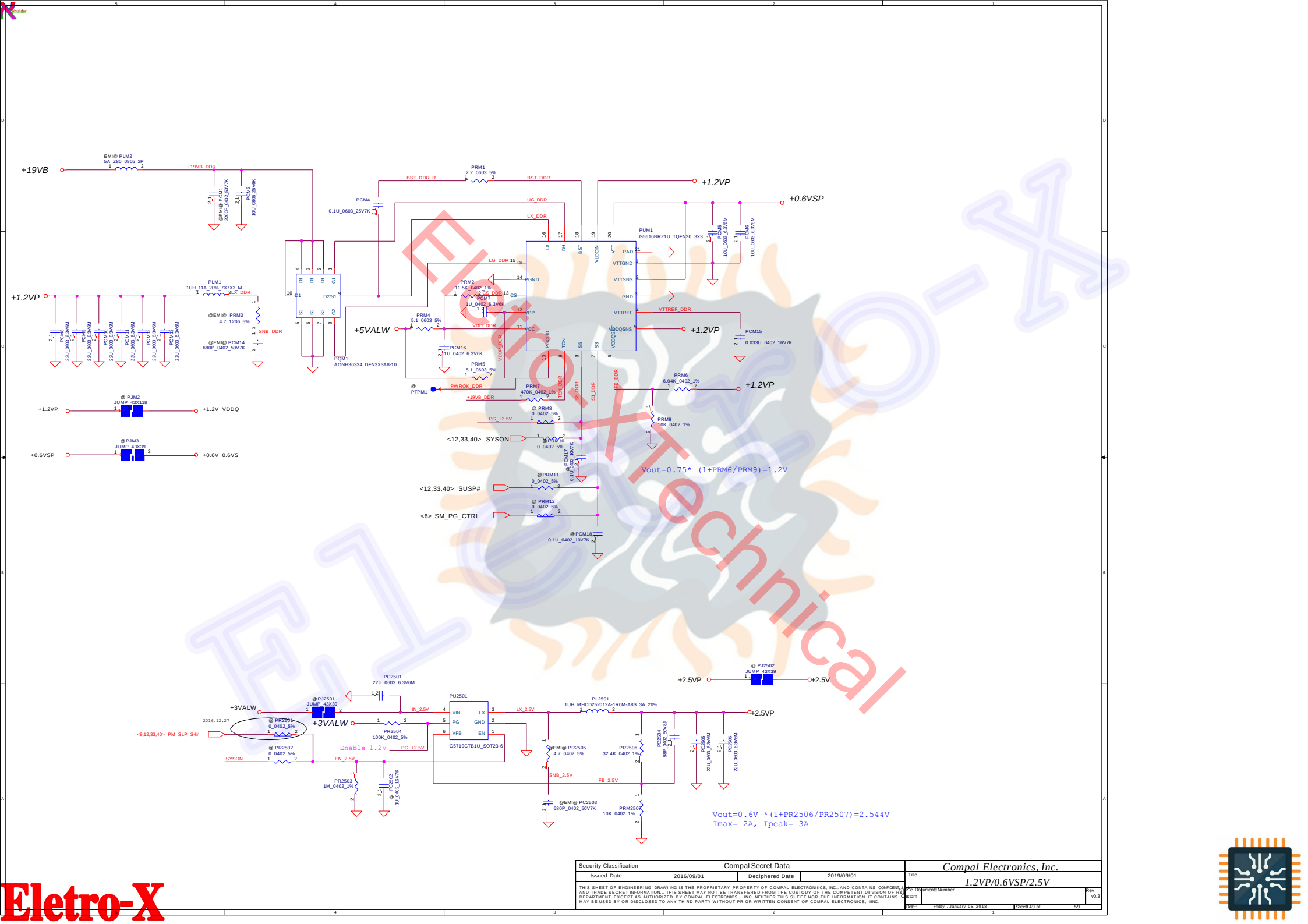
Date: Friday, January 05, 2018		Sheet: 48 of 59	



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Size: Custom	Document Number
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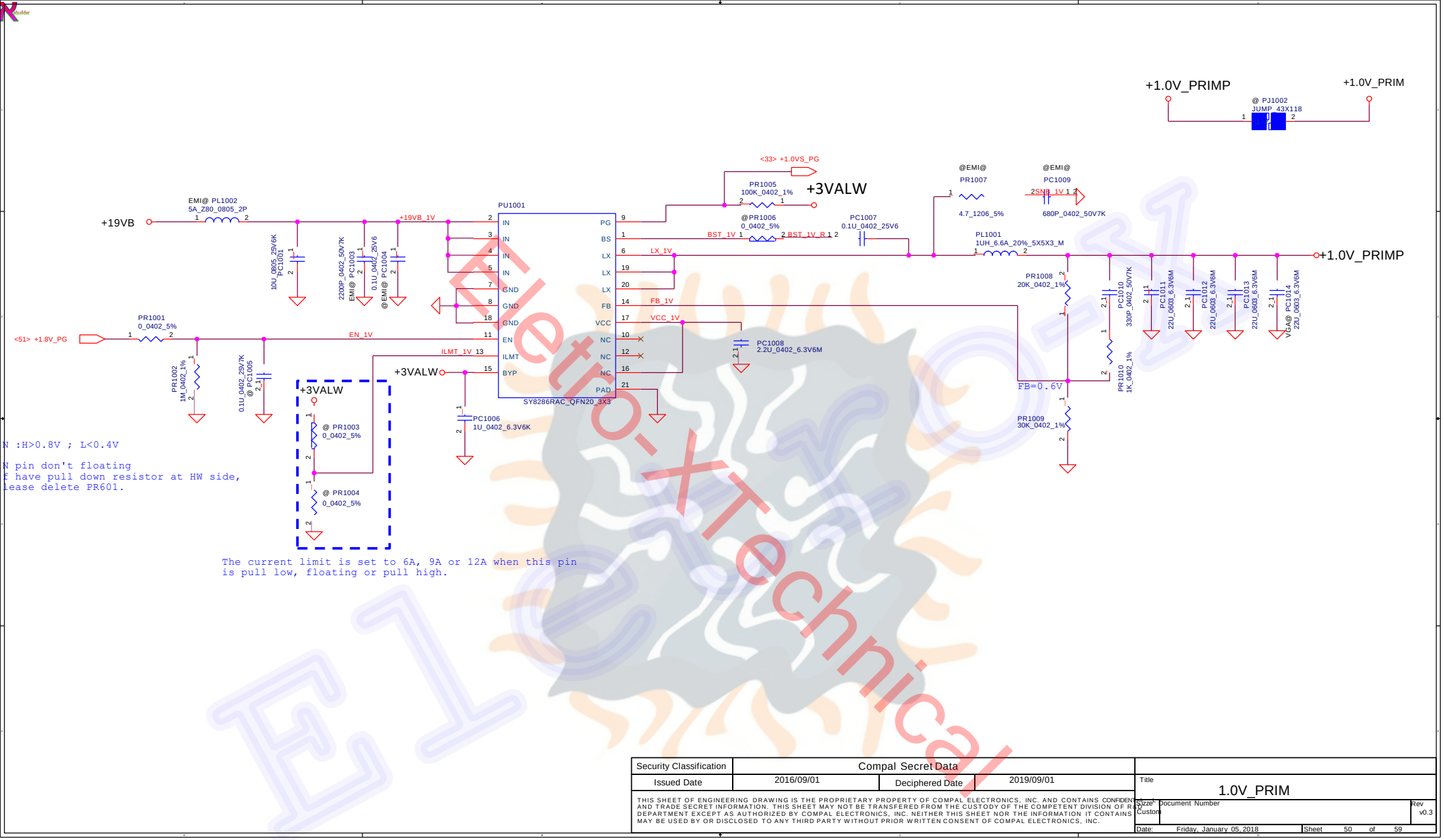

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Title: 1.0V_PRIM

Size: Custom | Document Number | Rev: v0.3

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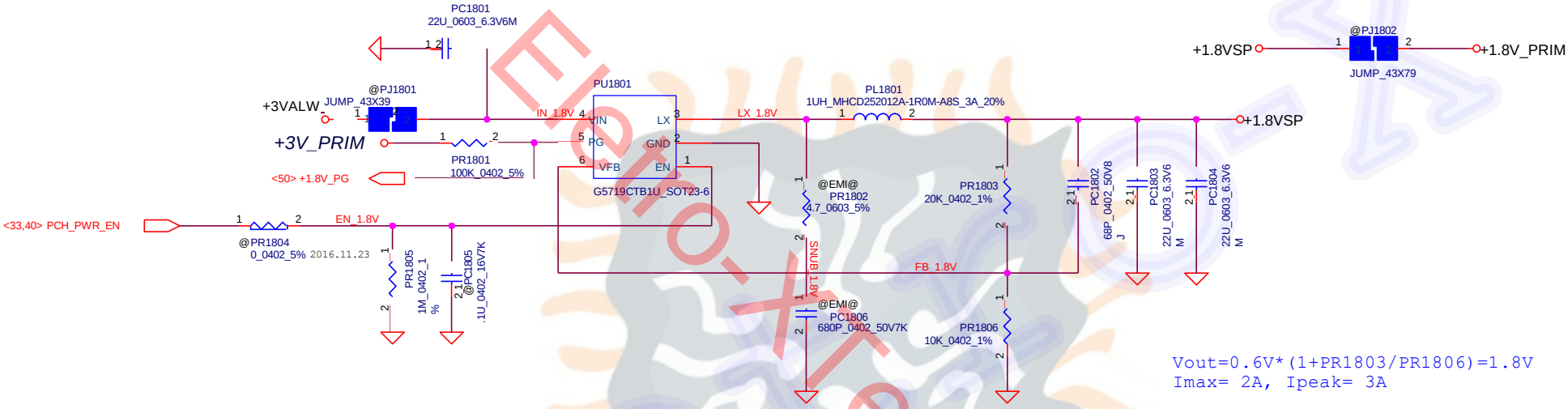

Vout=0.6V*(1+PR1803/PR1806)=1.8V
Imax= 2A, Ipeak= 3A

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

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Title: *1.8V_PRIM*

Size: B | Document Number: EPK52_LA-G07EP | Rev: v0.3

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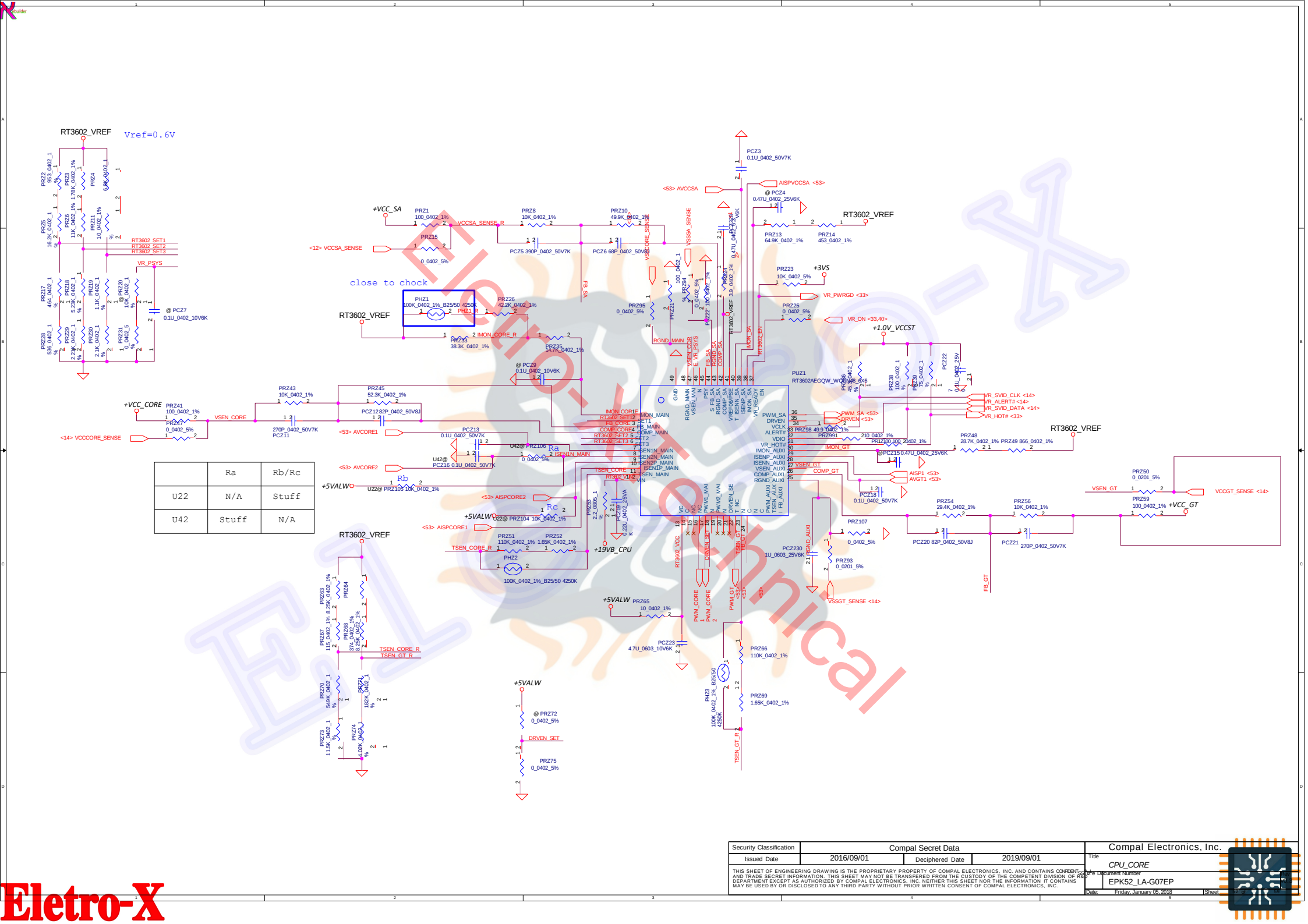

	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Title	CPU_CORE		
Size	Document Number		Rev
	EPK52_LA-G07EP		
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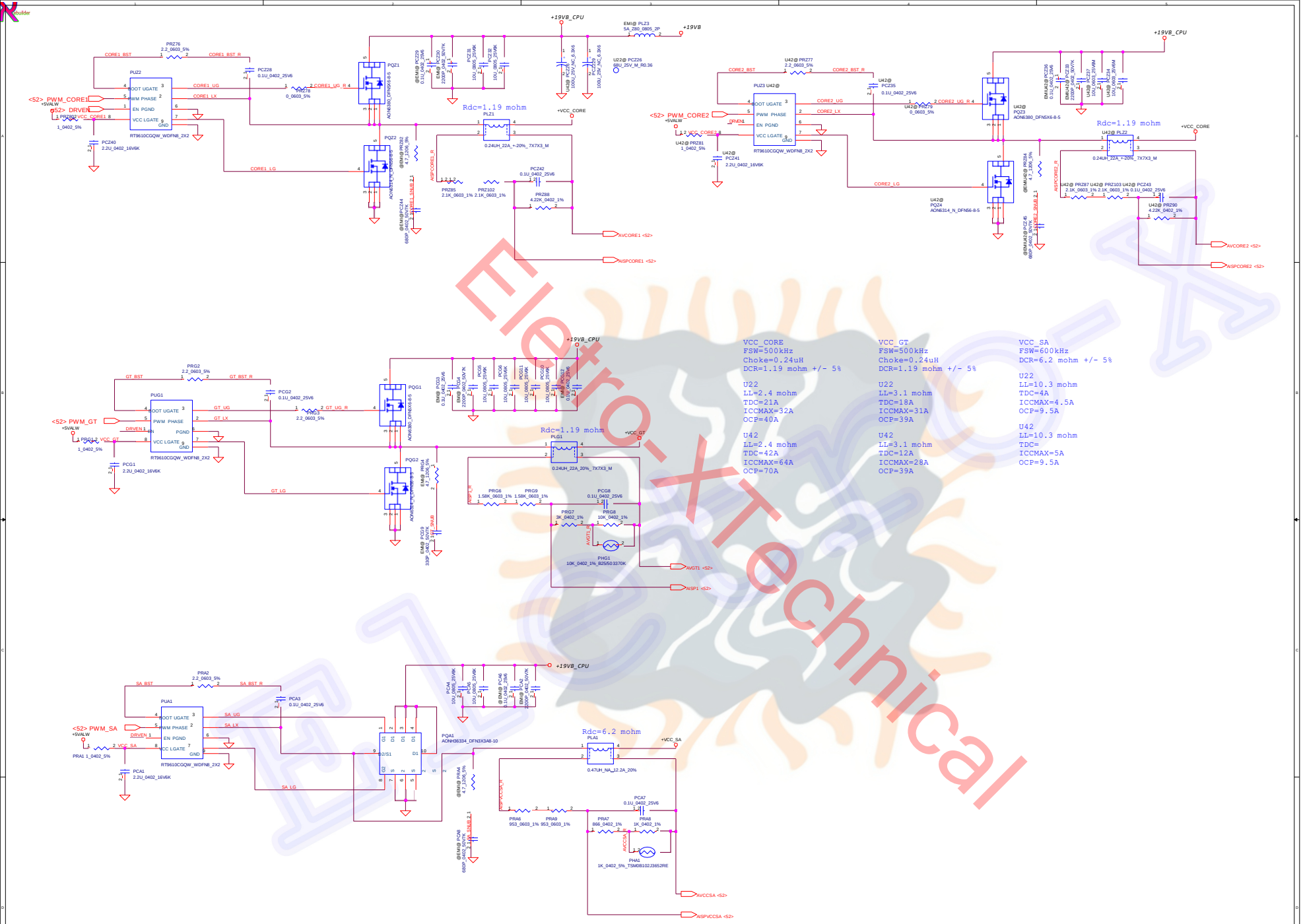

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01
Title	CPU Power stage		
Size	Document Number		Rev
	EPK52_LA-G07EP		X0.3
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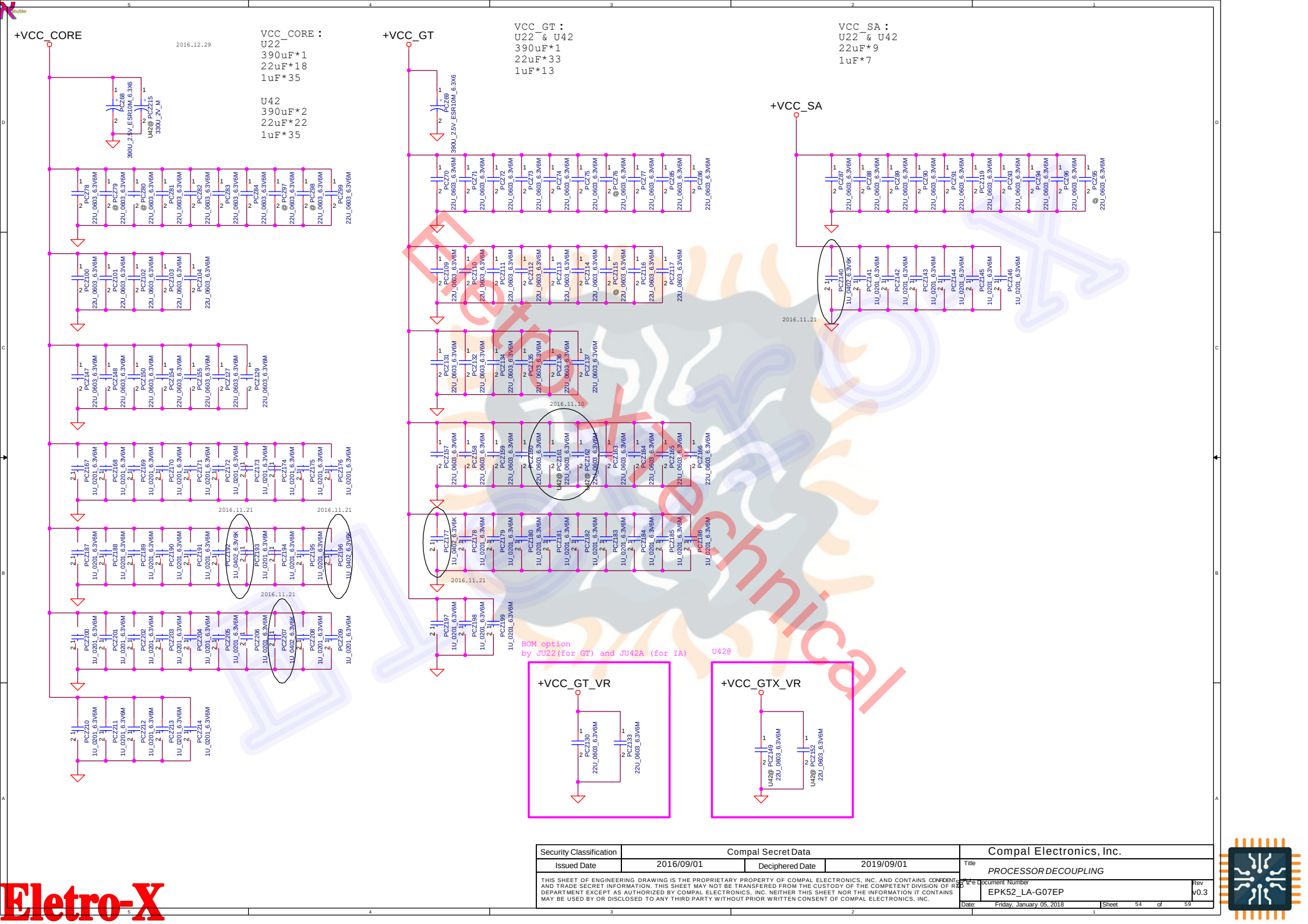

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Title	PROCESSOR DECOUPLING		
Size	Document Number		Rev
E	EPK52_LA-G07EP		v0.3
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