Compal Confidential

Intel M/B Schematics Document

Kabylake-U(2+2)-DDR4 SODIMMx2

nVidia N16 gDDR5-2GB

(N16S-GTR : GM108-670/770: GeForce MX130)
(N16V-GMR1 : GM108-626/726:GeForce MX110)

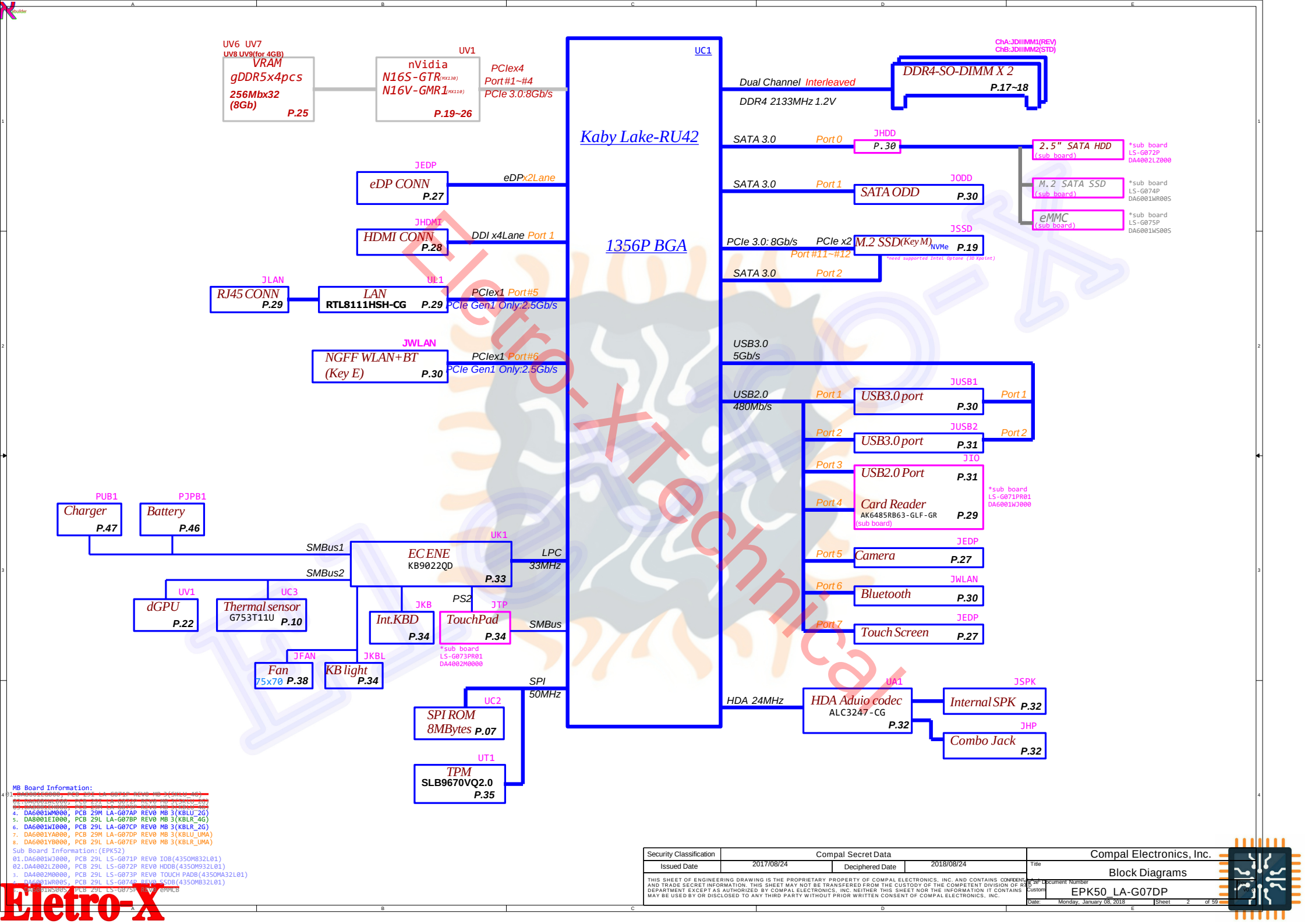
Project :2018OPP_Harry Potter(15.6")
EPK50 :LA-G07DP

Date : 2018-01-08
Version : 1.0

(Modified&Ref from:
01."NFLC_KBLR_LAE802PR10_MV_FINAL")
(02."Canadiens_LA-F035P-R10_KBL-UR_2017-06-23_CPU)
(02."CNL-U ORB_DDX02_LA-F152PR01_0822B")

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2017/10/22

Compal Electronics, Inc.			
Title: Cover Page			
Size: Custom	Document Number: EPK50_LA-G07DP		Rev: 1.0
Date: Monday, January 08, 2018	Sheet 1 of 59		



MB Board Information:

1. DA6001EG000, PCB 29L LA-G074P REV0 MB 3(5MKLU_4G)
2. DA6001WL000, PCB 29L LA-G072P REV0 MB 3(KBLU_2G)
3. DA6001WM000, PCB 29M LA-G07AP REV0 MB 3(KBLU_2G)
4. DA8001EI000, PCB 29L LA-G07BP REV0 MB 3(KBLR_4G)
5. DA6001WI000, PCB 29L LA-G07CP REV0 MB 3(KBLR_2G)
6. DA6001YA000, PCB 29M LA-G07DP REV0 MB 3(KBLU_UMA)
7. DA6001YB000, PCB 29L LA-G07EP REV0 MB 3(KBLR_UMA)

Sub Board Information:(EPK52)

1. DA6001WJ000, PCB 29L LS-G071P REV0 IOB(435OM832L01)
2. DA4002LZ000, PCB 29L LS-G072P REV0 HDDB(435OM932L01)
3. DA4002M0000, PCB 29L LS-G073P REV0 TOUCH PADB(435OMA32L01)
4. DA6001WR00S, PCB 29L LS-G074P REV0 SSDB(435OMB32L01)
5. DA6001WS00S, PCB 29L LS-G075P REV0 eMMCB

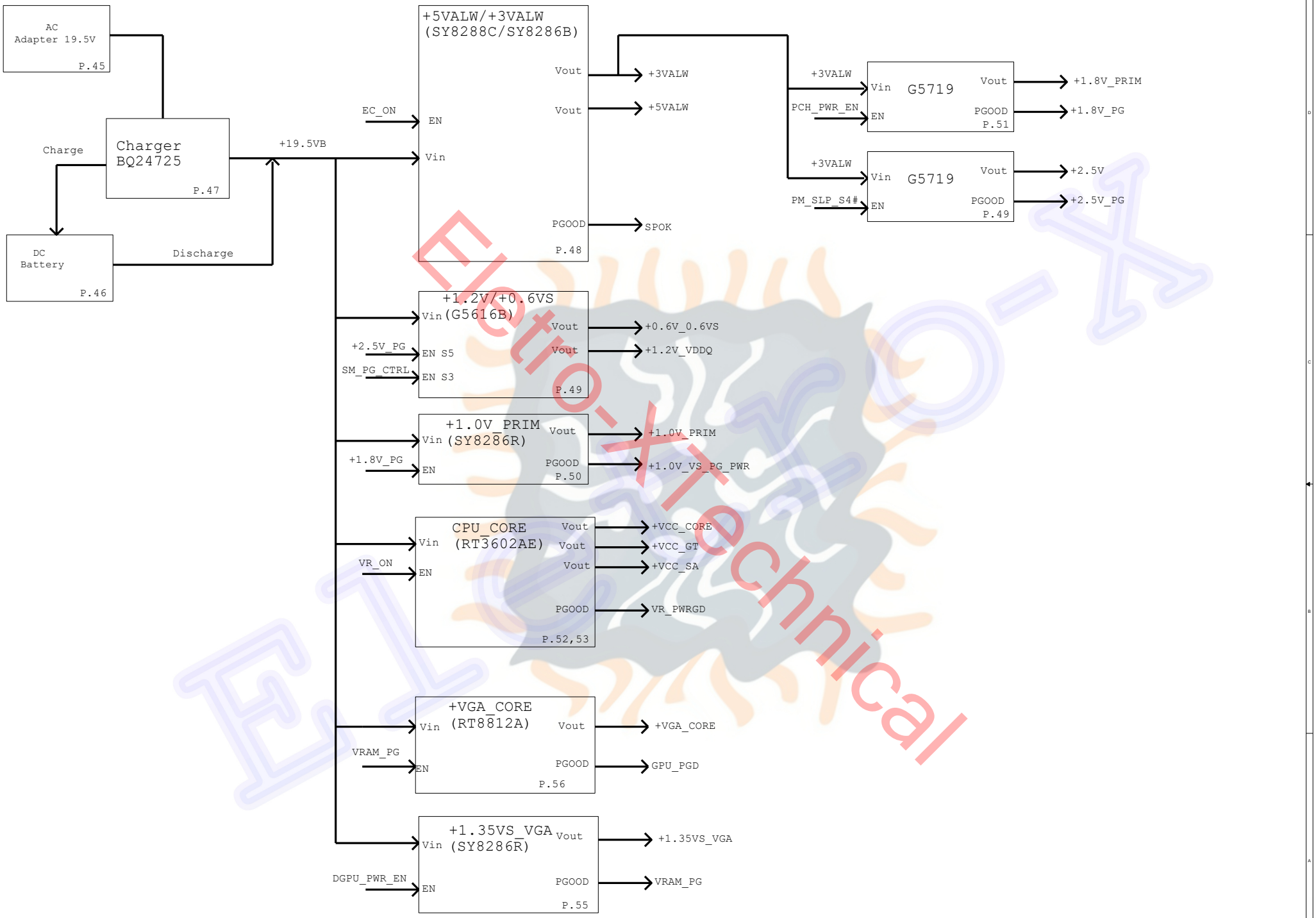
Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: Block Diagrams

Size: Custom | Document Number: EPK50_LA-G07DP | Rev: 1.0

Date: Monday, January 08, 2018 | Sheet 2 of 59



Security Classification	Compal Secret Data		Compal Electronics, Inc.
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Title	Power Block Diagram		
File Document Number	EPK50_LA-G07DP		Rev V0.3
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Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.2V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.6VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

BOM Structure Table (1/2)

Function	*Stuff*	*Un-Stuff*
DGPU SKU	PX@	
UMA SKU	UMA@	
TPM	TPM@	

SOC SMBUS Address Table

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBCLK SMBDATA	+3V_PRIM	DIMM1	0x50	0xA0	0xA1
		DIMM2	0x52	0xA4	0xA5
		Touch PAD	0x2C	0x58	0x59

EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
SMBUS Port 1	+3VL_EC	BAT	0x16
		CHGR	0x12
SMBUS Port 2	+3VS	dGPU	
		Thermal Sensor	0x90
		PCH	

Power State

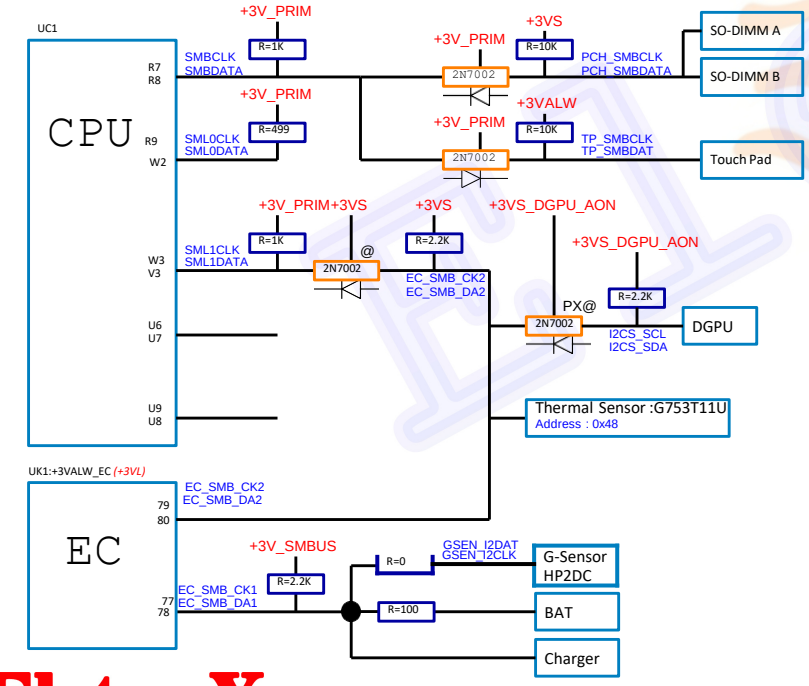
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

<USB2.0 port>

USB2.0 port	DESTINATION
1	USB3.0 Type-C
2	USB2.0/USB3.0
3	USB2.0/USB3.0
4	BT
5	HD/IR_1/IR_2 Camera
6	IR_2 Camera
7	Card Reader
8	X
9	X
10	X

<PCI-E,SATA,USB3.0/CLK>

Lane#	PCI-E	SATA	USB3.0		DESTINATION		CLK
1				1	USB3.0 Type-C		X
2				2	USB3.0 Type-C		X
3				3	USB2.0/USB3.0		X
4				4	USB2.0/USB3.0		X
5	1			5	GPU(DIS only)		CLK0
6	2			6	GPU(DIS only)		
7	3				GPU(DIS only)		
8	4				GPU(DIS only)		
9	5				LAN		CLK1
10	6				WLAN		CLK2
11	7		0		HDD		X
12	8		1a		ODD		CLK3
13	9				X		X
14	10				X		X
15	11		1b*		NVMe x2	X	CLK4
16	12		2			SATA SSD	X



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Size	Document Number		LA-G07DP(KBL-U UMA) 6B
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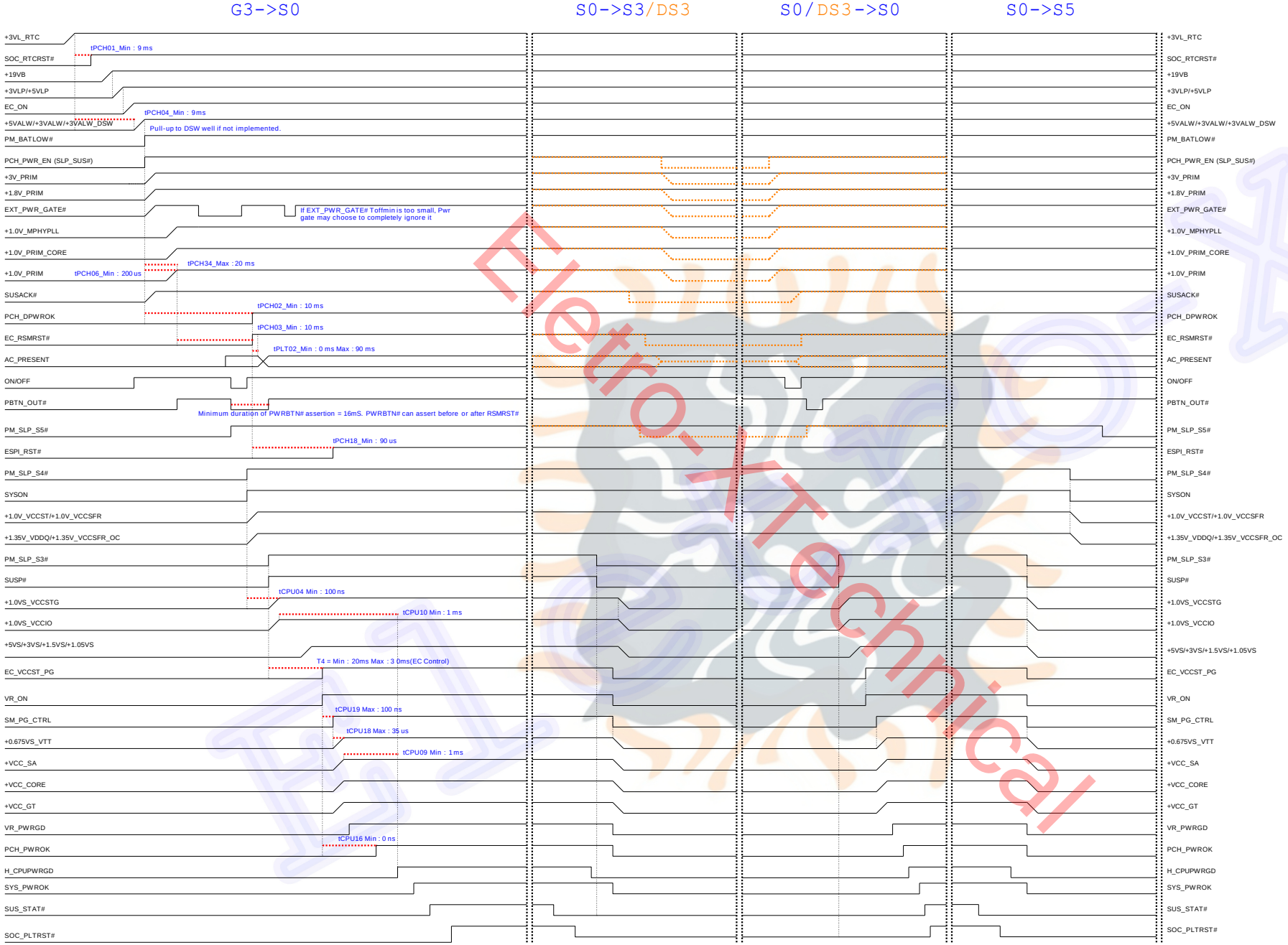

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Size: B	Document Number: EPK50_LA-G07DP		Rev: v0.3
Custom			
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SOC_DP1_CTRL_DATA(Internal Pull Down):

Display Port B Detected

0 = Port B is not detected.

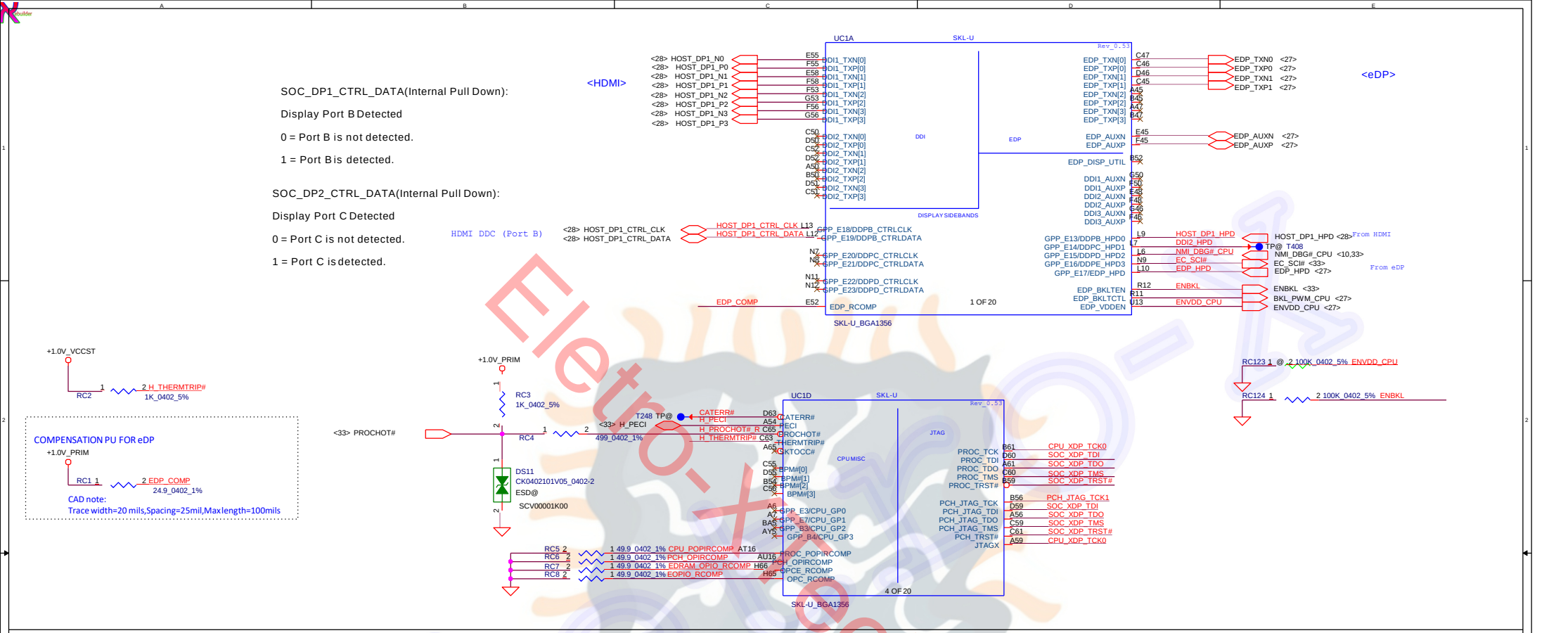
1 = Port B is detected.

SOC_DP2_CTRL_DATA(Internal Pull Down):

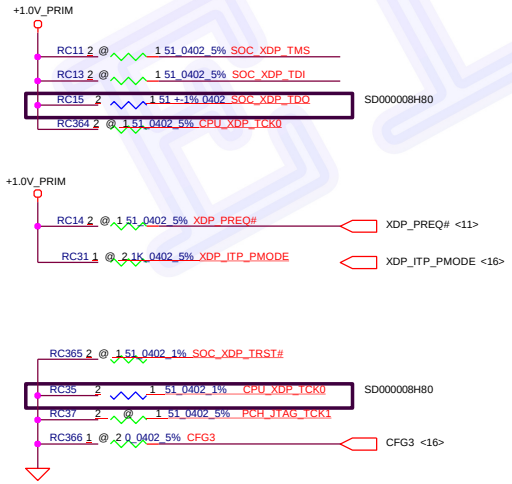
Display Port C Detected

0 = Port C is not detected.

1 = Port C is detected.



XDP CONN



Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: SKL-U(1/12)DDI,MISC,XDP,EDP

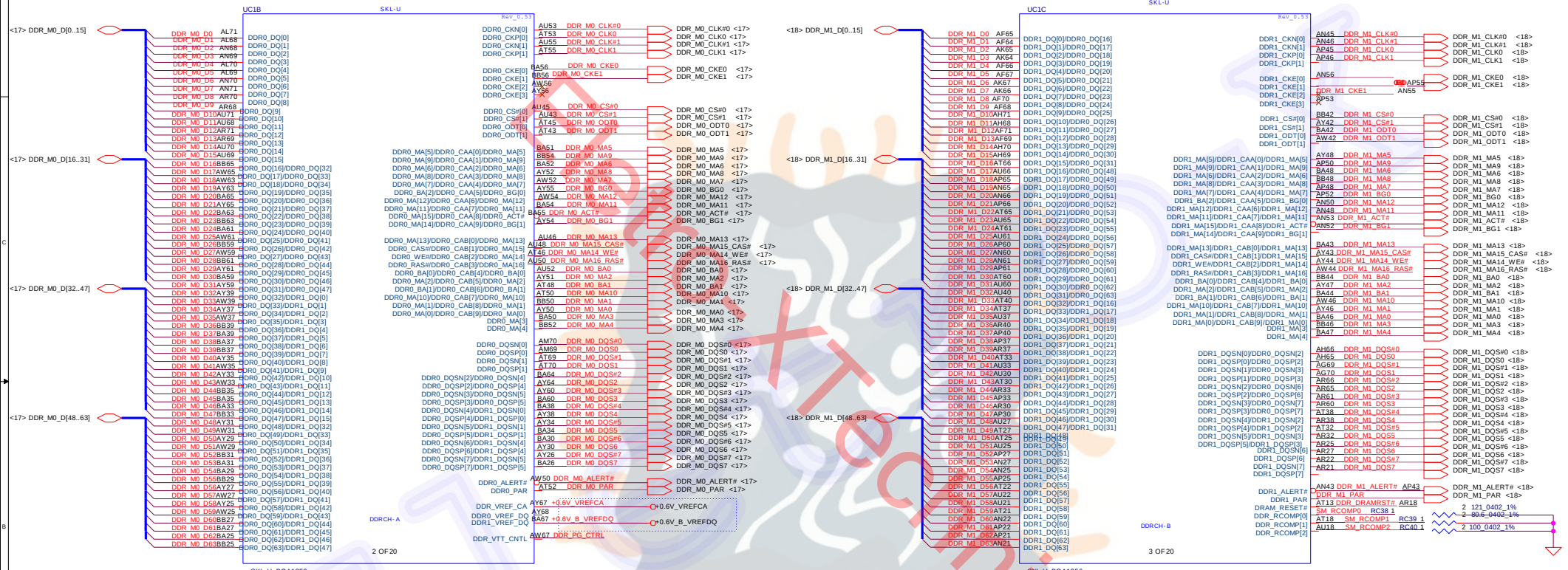
Size: Custom | Document Number: EPK50 LA-G07DP | Rev: 1.0

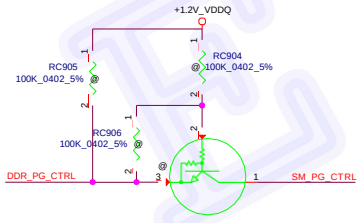
Date: Friday, January 05, 2018 | Sheet 5 of 5

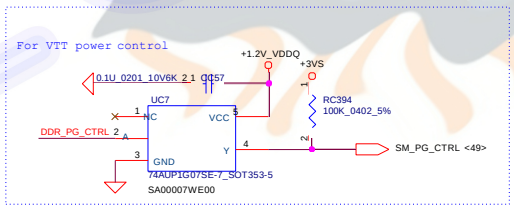
Interleaved Memory

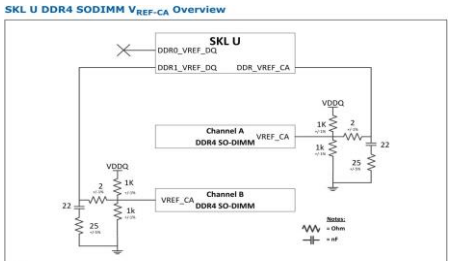
Interleaved Memory

<Cocoa_1020>
PDG#543016, ODT: CPU side no connect, DRAM side connect to VDDQ(Memory down); FET+R(SO-DIMM)









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Compal Electronics, Inc.	
Title	SKL-U(2/12)DDRIII
Size	Document Number: EPK50_LA-G07DP
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SML0ALERT# (Internal Pull Down):
eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

UC1E SKL-U SPI-FLASH SMBUS, SMLINK LPC CLINK SKL-U_BGA1356 5 OF 20

SMB (Link to XDP, DDR, TP)

SML1 (Link to EC,DGPU, LAN, Thermal Sensor)

To TPM

LPC Mode

To EC

Source From

SPI ROM (8MByte Only)

Use socket footprint

<DB> Un-pop QC2 for new 0x90 thermal sensor

From WW36 MOW for SKL-U ES sample

CLK Source CPU

EON SA000046400 S IC FL 64M EN25Q64-104HIP SOP 8P MXIC
SA00006N100 S IC FL 64M MX25L6473EM2I-10G SOP 8P
WINBOND SA000039A30 S IC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM
Micron SA00005L100 S IC FL 64M M25Q064A13ESEC0F SO8W 8P

ENE Fixed Code Block Diagram

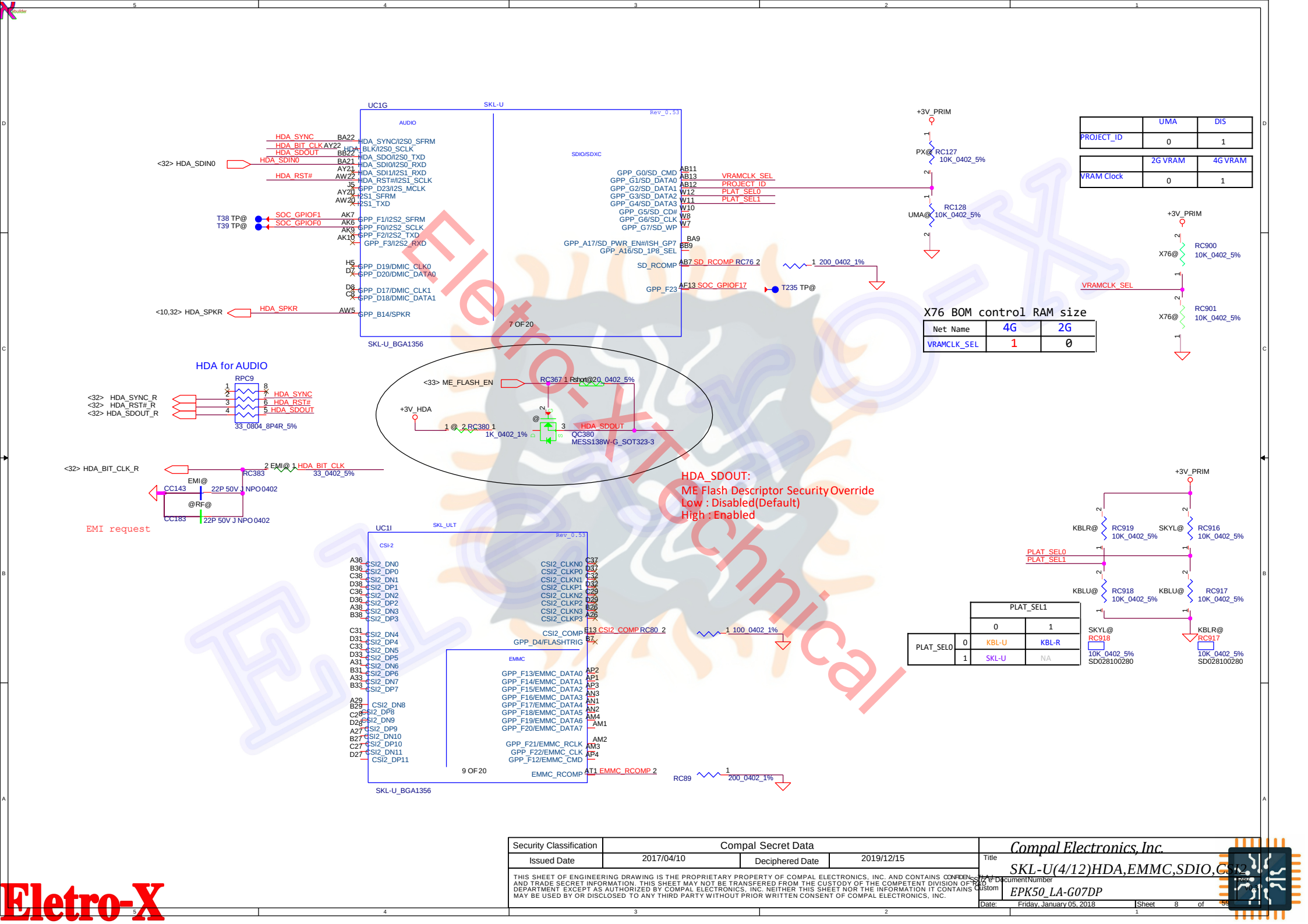
Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: SKL-U(3/12)SPI,ESPI,SMB,LPC

Size: Custom | Document Number: EPK50_LA-G07DP | Rev: 0.3

Date: Friday, January 05, 2018 | Sheet 7 of 9



	UMA	DIS
PROJECT_ID	0	1

	2G VRAM	4G VRAM
VRAM Clock	0	1

X76 BOM control RAM size

Net Name	4G	2G
VRAMCLK_SEL	1	0

PLAT_SEL0	PLAT_SEL1 = 0	PLAT_SEL1 = 1
0	KBL-U	KBL-R
1	SKL-U	NA

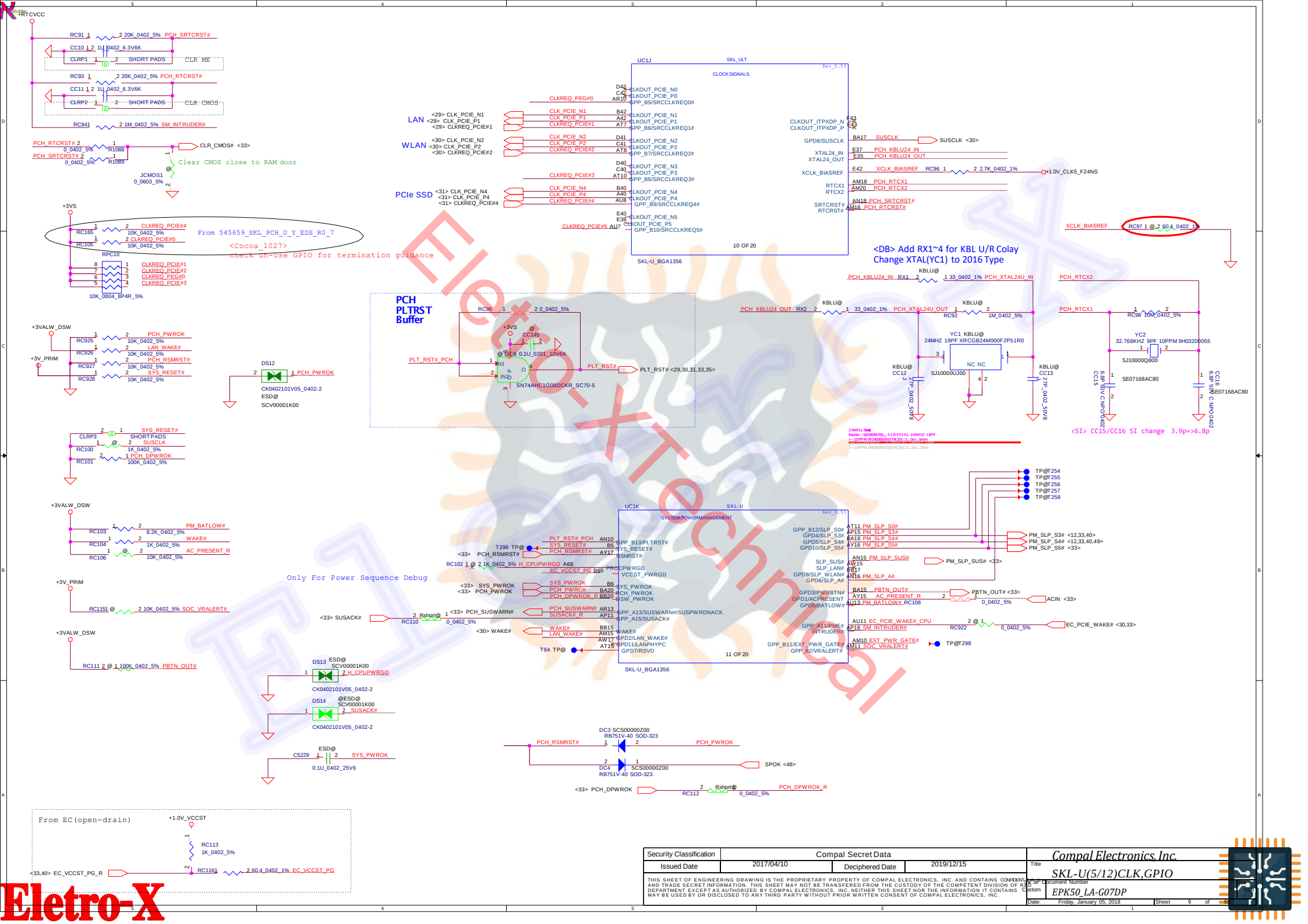
Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

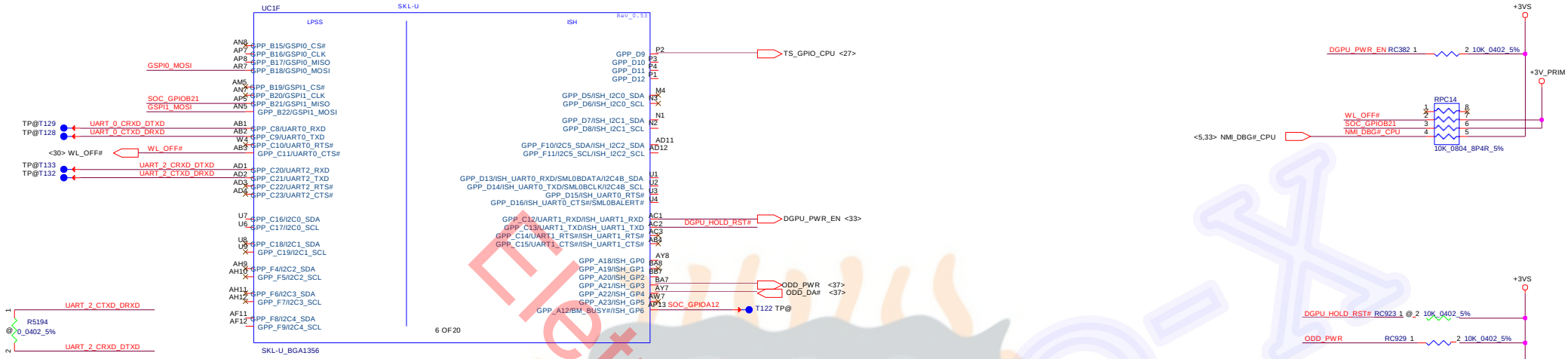
Size: Custom | Document Number: EPK50_LA-G07DP | Rev: 1.0

Date: Friday, January 05, 2018 | Sheet 8 of 55



Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.			
Title: SKL-U(5/12)CLK,GPIO			
Size: Custom	Document Number: EPK50_LA-G07DP		Rev: 0.3
Date: Friday, January 05, 2018	Sheet 9	of 54	



Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.---> AAX05 Use

1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

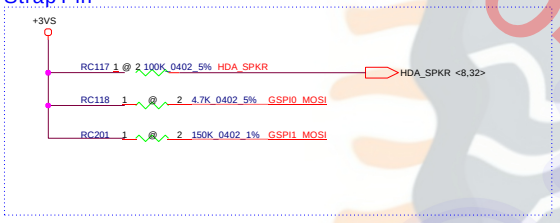
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode --> AAX05 Use

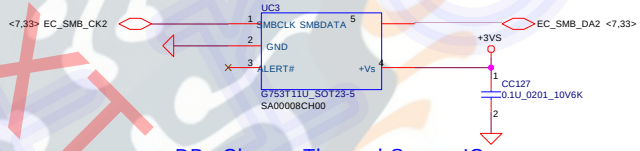
1 = LPC Mode

Strap Pin



CPU THERMAL SENSOR

Address : 0x48



<DB> Change Thermal Sensor IC

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Issued Date	2017/04/10	Deciphered Date	2019/12/15

Title	Compal Electronics, Inc.
	SKL-U(6/12)GPIO
Size: Custom	Document Number: EPK50_LA-G07DP
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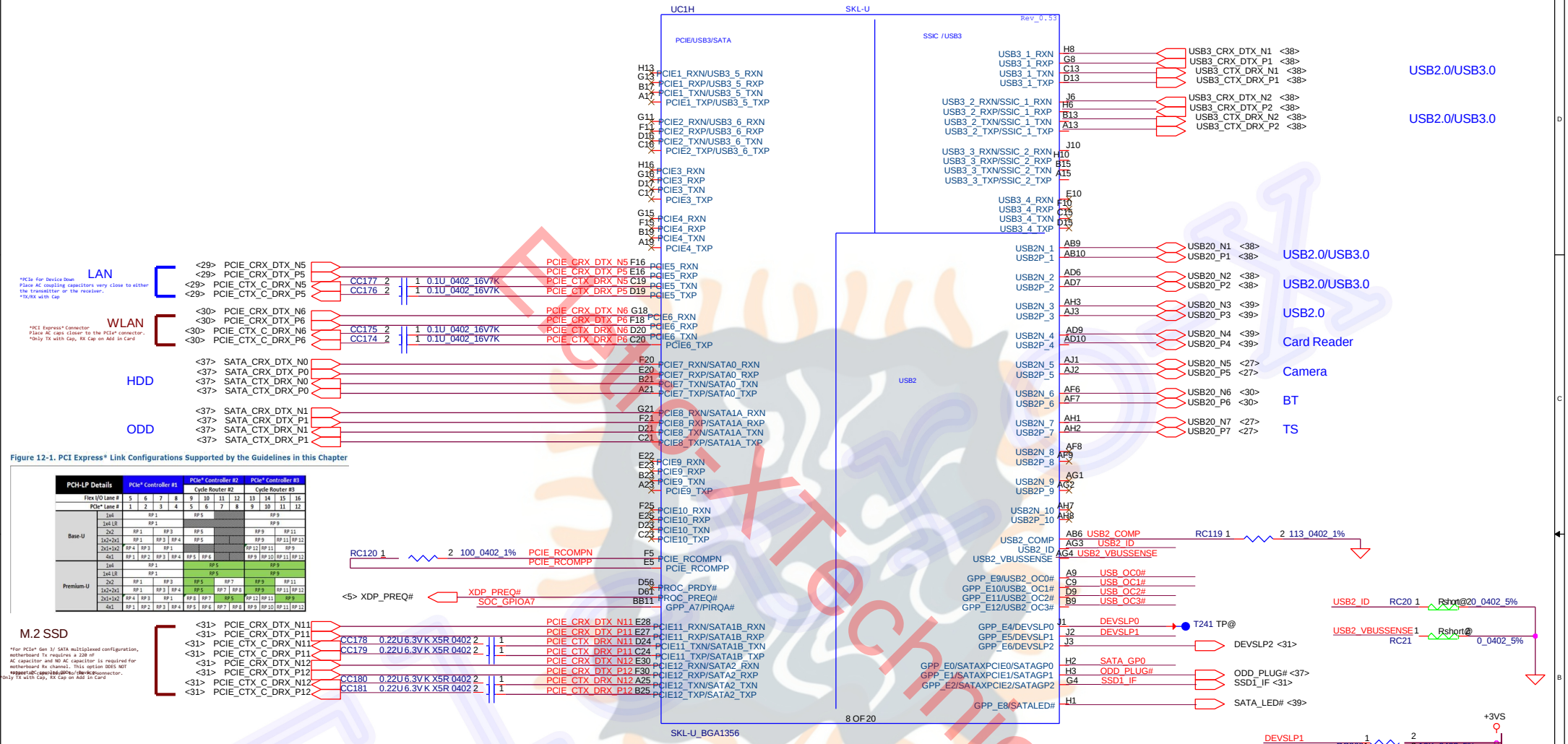
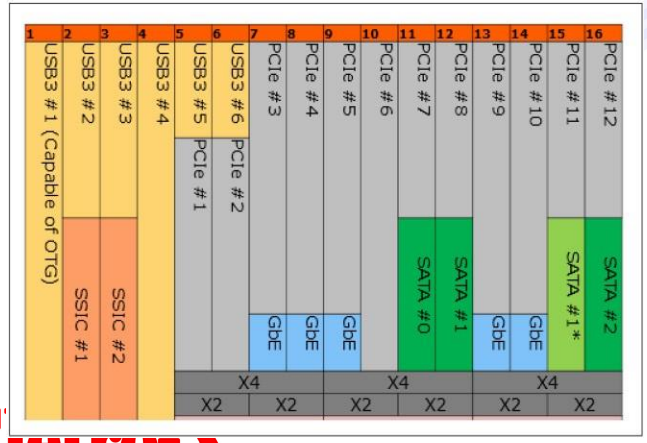


Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
						Cycle Router #2				Cycle Router #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP1				RP5				RP9			
	1x4 LR	RP1								RP9			
	2x2	RP1		RP3		RP5				RP9		RP11	
	1x2+2x1	RP1		RP3	RP4	RP5				RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1						RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6			RP9	RP10	RP11	RP12
Premium-U	1x4	RP1				RP5				RP9			
	1x4 LR	RP1				RP5				RP9			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12

High Speed I/O (HSIO) Lane Multiplexing in SKL U



When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1 and Port 2
USB_OC1#	USB2 Port 3
USB_OC2#	N/A
USB_OC3#	N/A
DEVSLP0	N/A
DEVSLP1	N/A
DEVSLP2	NGFF SSD KEY- M
SATA_GP0	N/A
SATA_GP1	ODD_PLUG#
SATA_GP2	PCIE/SATA

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Compal Electronics, Inc.

Title: SKL-U(7/12)PCIE,USB,SATA

Size: Custom | Document Number: EPK50_LA-G07DP | Rev: 0.3

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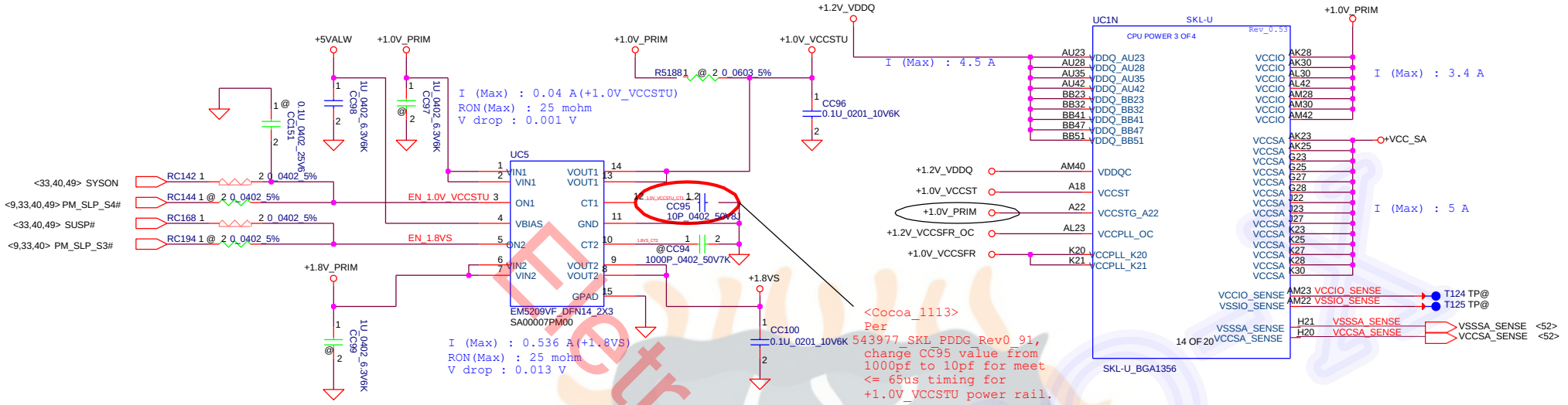
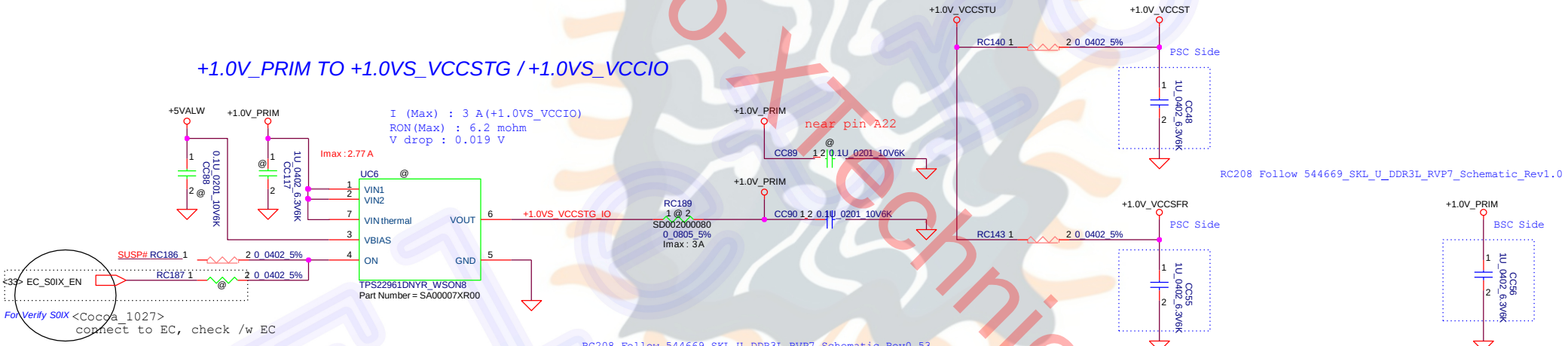
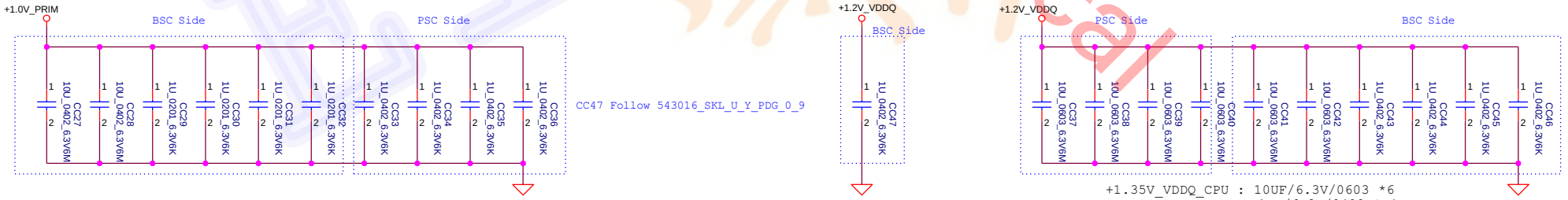
+1.0V_PRIM TO +1.0V_VCCSTU



<Cocoa_1113>
Per 543977_SKL_PDDG_Rev0_91, change CC95 value from 1000pf to 10pf for meet <= 65us timing for +1.0V_VCCSTU power rail.

+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO





Security Classification	Compal Secret Data		
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Title	SKL-U(8/12)Power		
Size	Document Number	EPK50_LA-G07DP	Rev
Custom			
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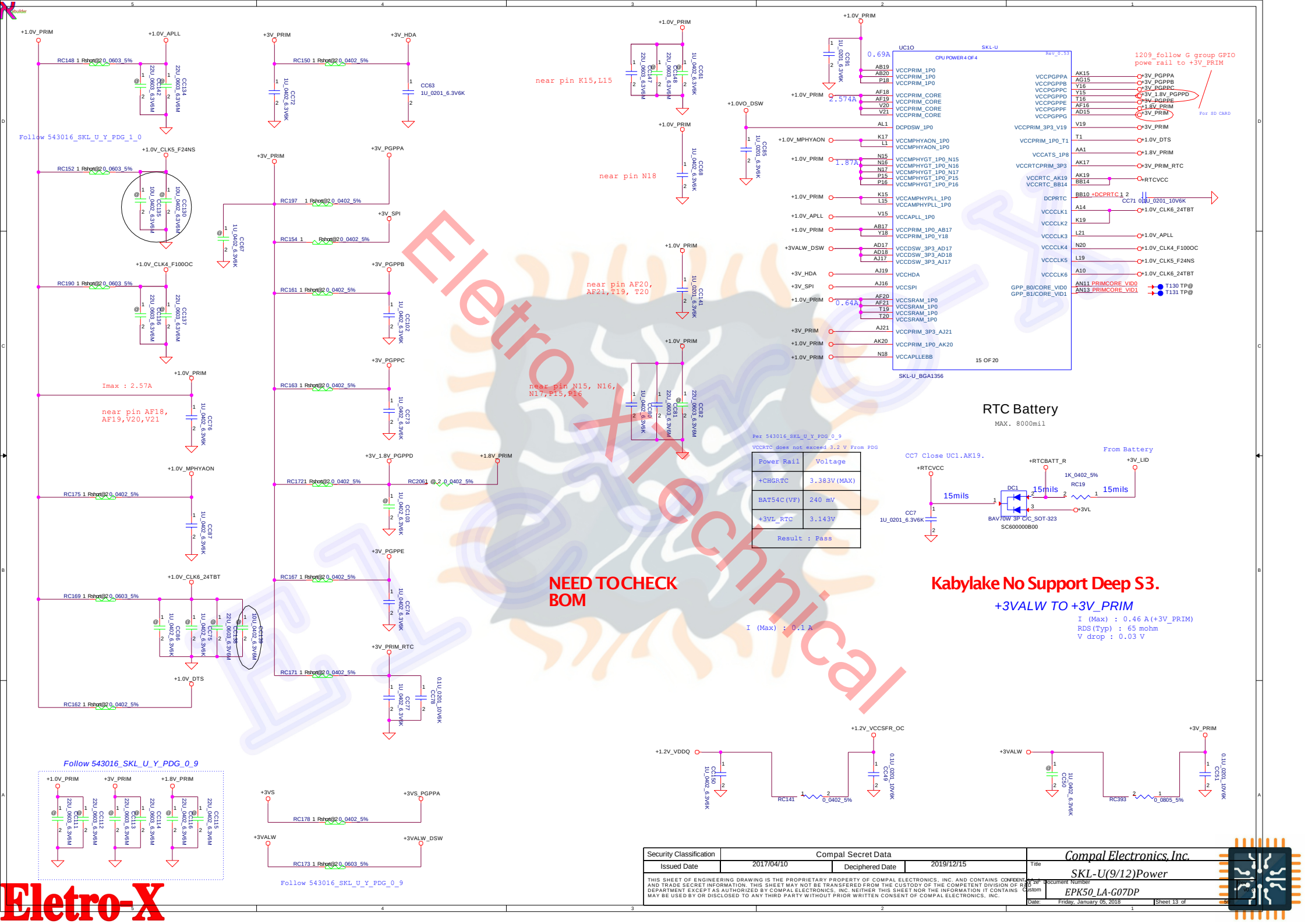
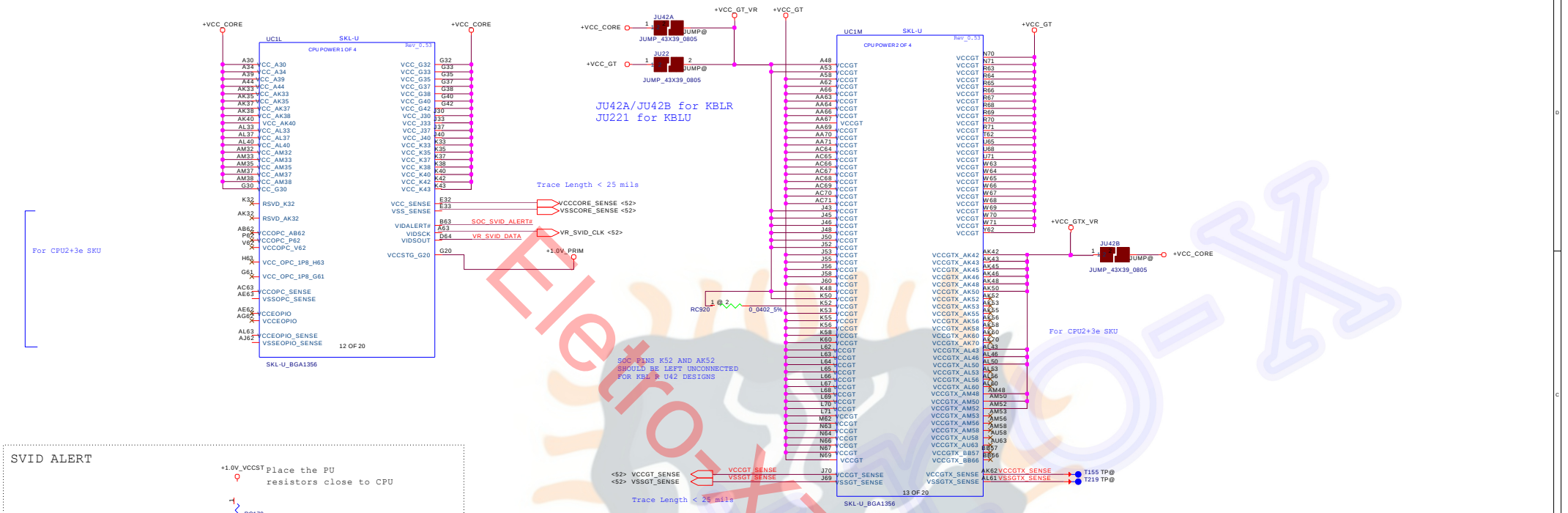
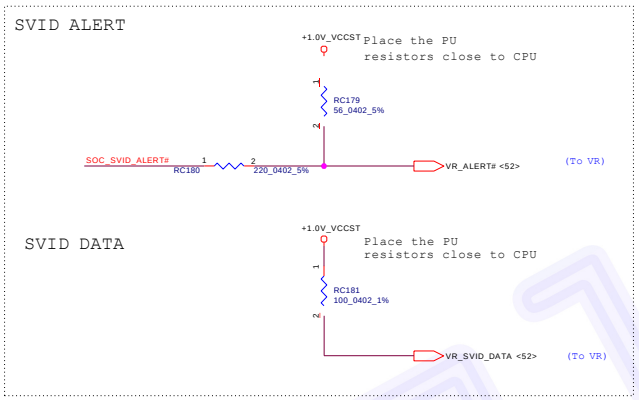


Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.			
Title: SKL-U(9/12)Power			
Size: Custom	Document Number: EPK50_LA-G07DP		Rev: 0.3
Date: Friday, January 05, 2018	Sheet 13 of		

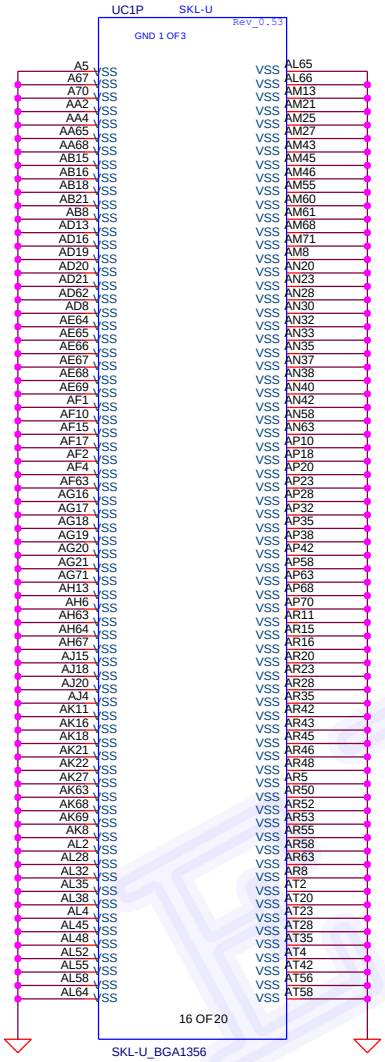


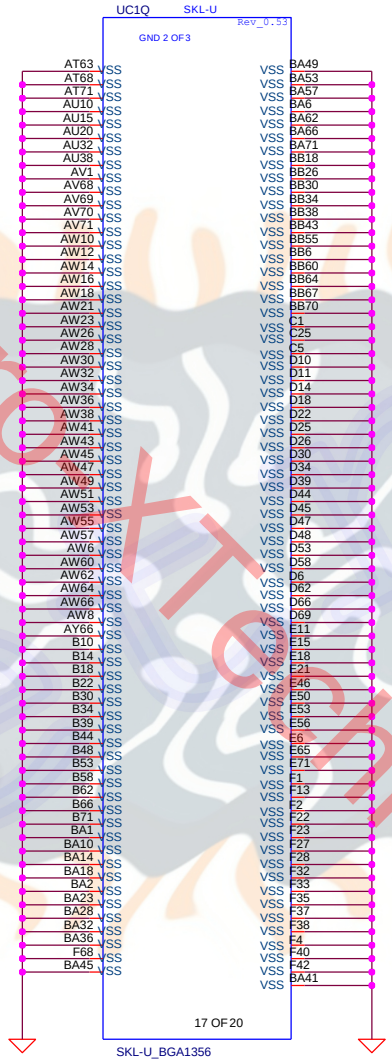


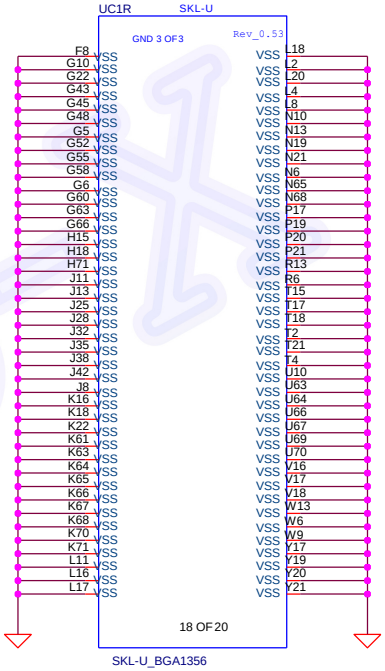
Ball #	Ball Names R-U42	Ball Names U22	R-U42/U22 common board guidelines
C7	XTAL24_OUT	NC	connect to R-U42 XTAL24_OUT
E3	XTAL24_IN	NC	connect to R-U42 XTAL24_IN
E35	NC	XTAL24_OUT	connect to U22 XTAL24_OUT
E37	NC	XTAL24_IN	connect to U22 XTAL24_IN
AK42	VCCCORE	VccGTx	
AK43	VCCCORE	VccGTx	
AK45	VCCCORE	VccGTx	
AK46	VCCCORE	VccGTx	
AK48	VCCCORE	VccGTx	
AK50	VCCCORE	VccGTx	connect to VccGTx/VCCCORE
AL43	VCCCORE	VccGTx	power plane island
AL46	VCCCORE	VccGTx	
AL50	VCCCORE	VccGTx	
AM48	VCCCORE	VccGTx	
AM50	VCCCORE	VccGTx	
AM52	VCCCORE	VccGTx	
J43	VCCCORE	VCCGT	
J45	VCCCORE	VCCGT	
J46	VCCCORE	VCCGT	
J48	VCCCORE	VCCGT	
J50	VCCCORE	VCCGT	connect to VccGT/VCCCORE
J52	VCCCORE	VCCGT	power plane island
K48	VCCCORE	VCCGT	
K50	VCCCORE	VCCGT	
A48	VCCCORE	VCCGT	
A53	VCCCORE	VCCGT	
AK52	RSVD	VccGTx	**Must Not Be Connected**. RVP use this signal for debug and testing purpose only.
K52	RSVD	VCCGT	**Must Not Be Connected**. RVP use this signal for debug and testing purpose only.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/04/10	Deciphered Date	2019/12/15
			Title: SKL-U(10/12)Power,SVID

Size: D	Custom	Document Number: EPK50_LA-G07DP	Rev: v0.3
Date: Friday, January 05, 2018		Sheet 14 of 59	







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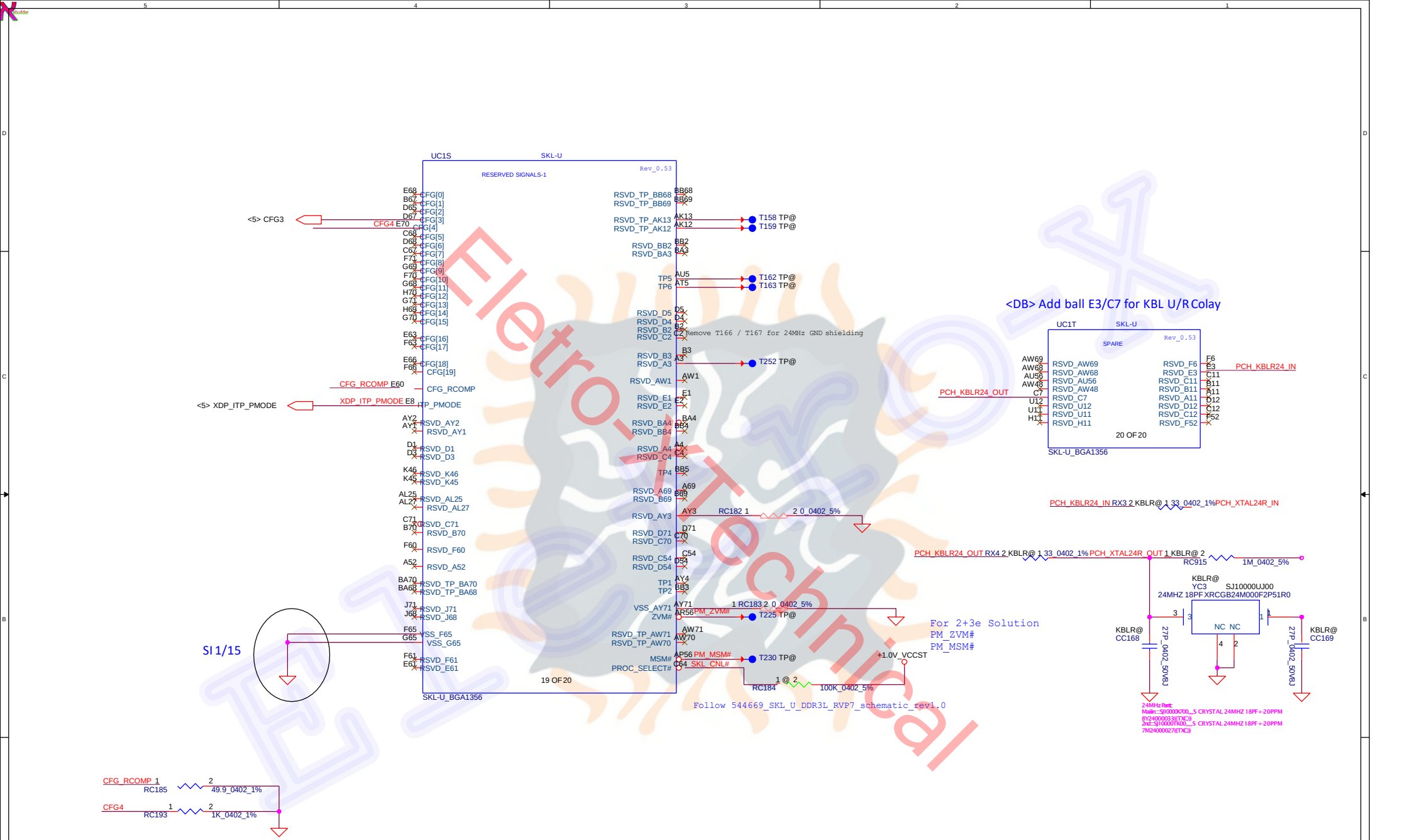
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: SKL-U(11/12)GND

Size: A3 | Document Number: EPK50_LA-G07DP | Rev: 1.0

Date: Friday, January 05, 2018 | Sheet 15 of 59



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: SKL-U(12/12)RSVD

Size: Custom | Document Number: EPK50_LA-G07DP | Rev: 0.3

Date: Friday, January 05, 2018 | Sheet 16 of 59

CHANNEL-A

REVERSE TYPE

Interleaved Memory

TOP: JDIMM1 CONN Non-ECC DIMM

PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

Layout Note:
PLACE THE CAP near JDIMM1. 164

Layout Note:
Place near JDIMM1

PLACE NEAR TO PIN

PLACE NEAR TO SODIMM

9/8 Modify

For ECC DIMM

DIMM Side

CPU Side

VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

Part Number:LTCX0069GA0
Part Value:S SOCKET FOX AS0A827-H2RB-7H 260P DDR4

Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: P18-DDRIV_CHA: DMM0

Size: Document Number: EPK50_LA-G07DP

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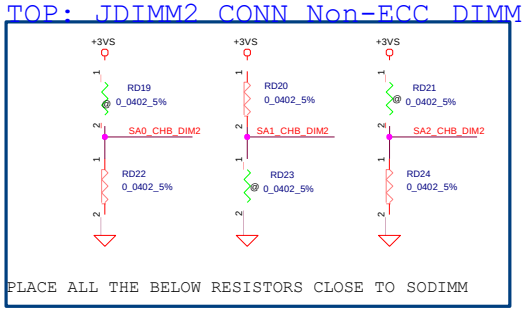
CHANNEL-B

Interleaved Memory

STD (5.2 mm)

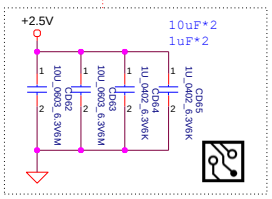
TOP: JDIMM2 CONN Non-ECC DIMM



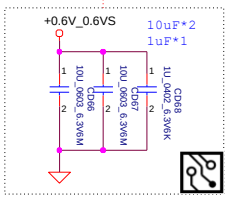
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

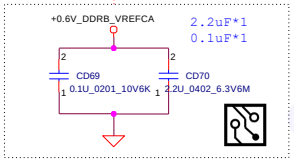
Layout Note:
Place near JDIMM2.257,259

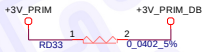


Layout Note:
Place near JDIMM2.258

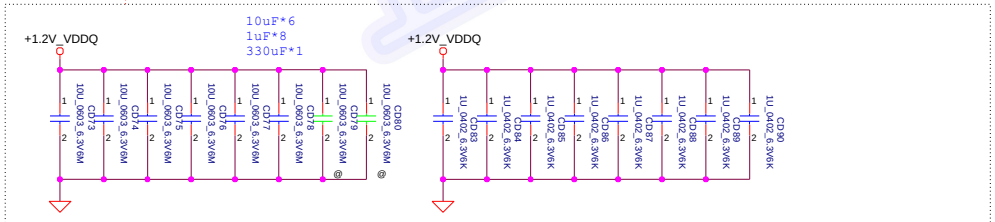


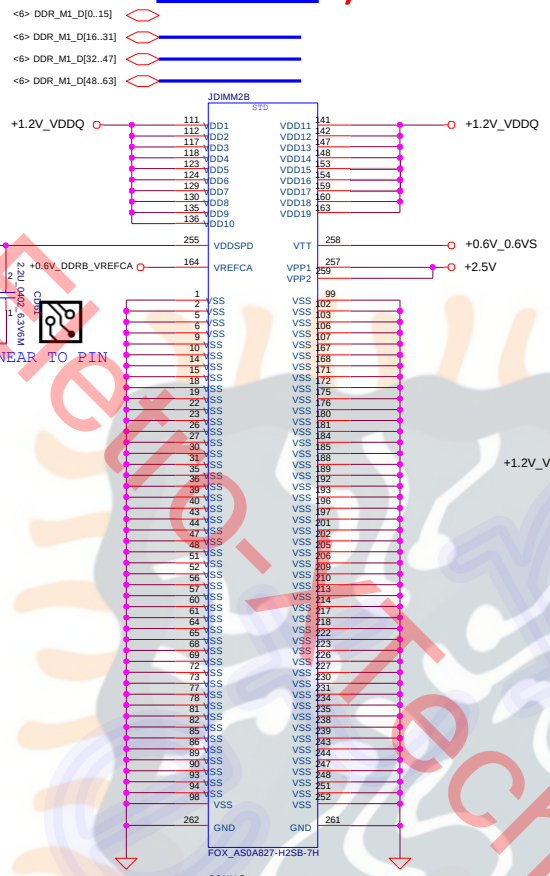
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2



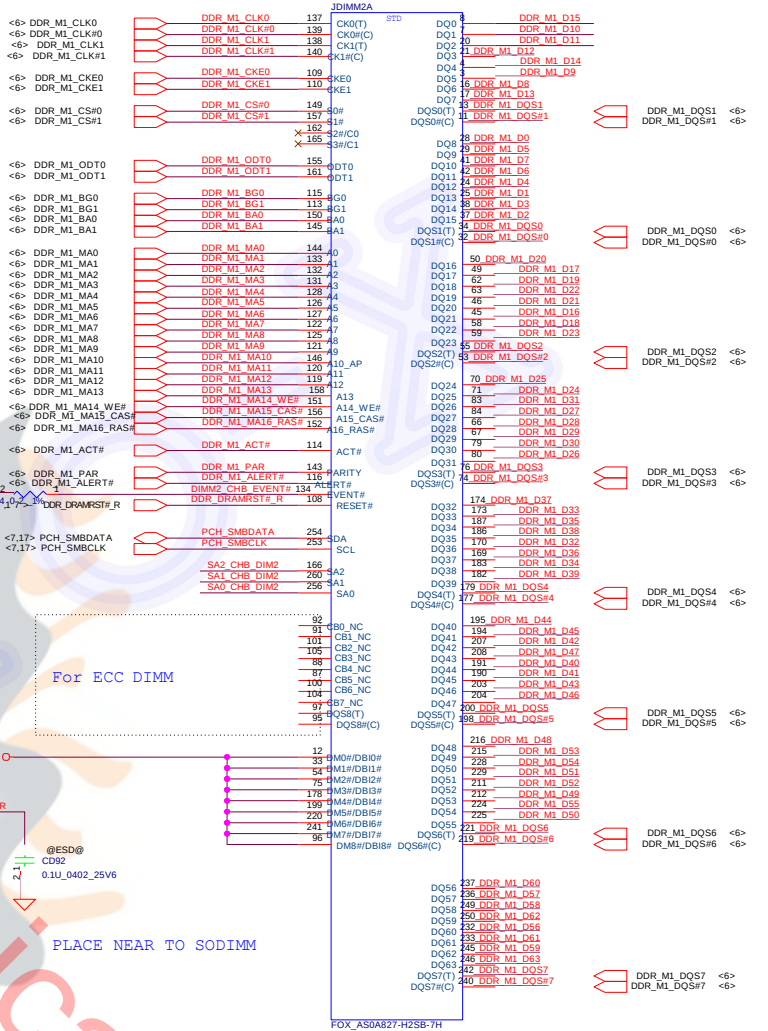


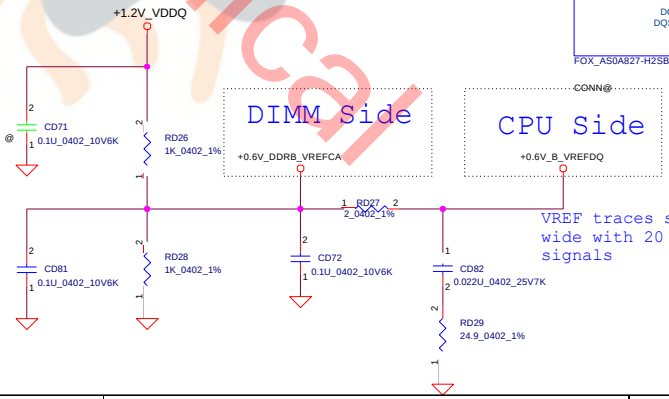
Layout Note:
Place near JDIMM2





Part Number:LTCX0069FA0
Part Value:S SOCKET FOX AS0A827-H2SB-7H 260P DDR4





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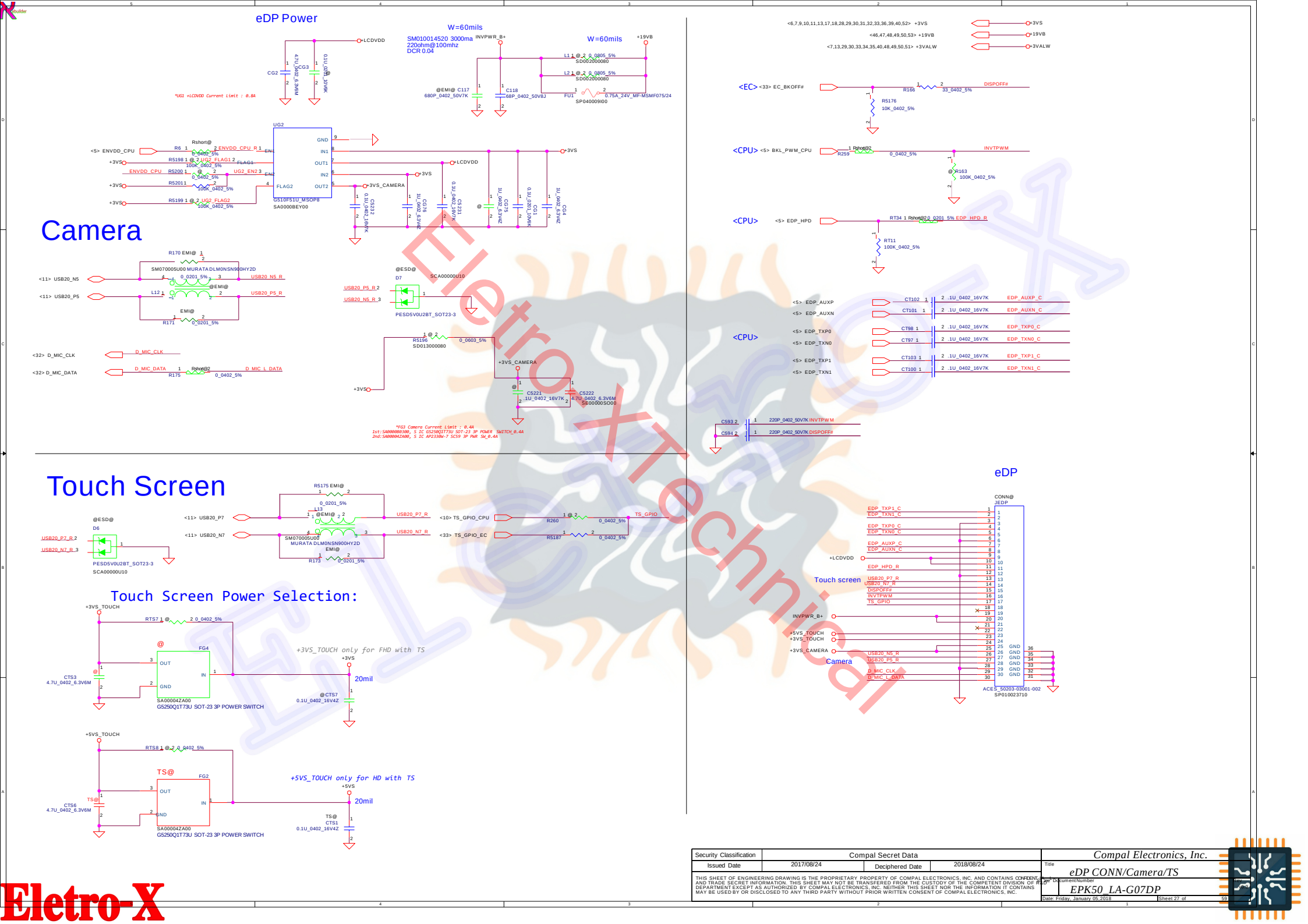
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: P19-DDRIV_CHB: DIMM0

Size: Document Number: EPK50_LA-G07DP

Date: Friday, January 05, 2018 Sheet 18 of 54



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Title: eDP CONN/Camera/TS

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<CPU>
<5> HOST_DP1_P0 — HOST_DP1_P0 0.1U_0402_16V7K 1 — 2 CG8 — HDMI_TX_P2
<5> HOST_DP1_N0 — HOST_DP1_N0 0.1U_0402_16V7K 1 — 2 CG9 — HDMI_TX_P2
<5> HOST_DP1_P1 — HOST_DP1_P1 0.1U_0402_16V7K 1 — 2 CG10 — HDMI_TX_P1
<5> HOST_DP1_N1 — HOST_DP1_N1 0.1U_0402_16V7K 1 — 2 CG11 — HDMI_TX_N1
<5> HOST_DP1_P2 — HOST_DP1_P2 0.1U_0402_16V7K 1 — 2 CG12 — HDMI_TX_P0
<5> HOST_DP1_N2 — HOST_DP1_N2 0.1U_0402_16V7K 1 — 2 CG13 — HDMI_TX_N0
<5> HOST_DP1_P3 — HOST_DP1_P3 0.1U_0402_16V7K 1 — 2 CG14 — HDMI_CLKP
<5> HOST_DP1_N3 — HOST_DP1_N3 0.1U_0402_16V7K 1 — 2 CG15 — HDMI_CLKN

RP1 470_0804_8P4R_5% RP2 470_0804_8P4R_5%

QG1B SB00001FF00
L2N7002SDW1T1G 2N SC88-6

+3VS

1.3.2 Digital Display Interface Signal Mapping

Table 1-4. Digital Display Interface Signal Mapping

Port	DDI PROCESSOR Pin Names	Display Port Mapping	HDMI* Mapping
Port 1	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIxC_TX2_DN
	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIxC_TX2_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIxC_TX1_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIxC_TX1_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIxC_TX0_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIxC_TX0_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIxC_CLK_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIxC_CLK_DP
	DDPB_HPD	DDI1_HPD_Q	DDI1_HPD_Q
	DDPB_CTRLCLK	NA	DDI1_CTRL_CK
	DDPB_CTRLDATA	NA	DDI1_CTRL_DATA

DDI_0 → HDMI_2; DDI_3 → HDMI_0 CLK

*DDA30_LA-F292PR02: RS_8.2ohm_RP_360ohm

HDMI_CLKP — RG59 1 EMI@ 2 15 +-1% 0402 — HDMI_R_CLKP
CG71 EMI@ 360 +-5%0402 SD028360080
HDMI_CLKN — RG60 1 EMI@ 2 15 +-1% 0402 — HDMI_R_CLKN
HDMI_TX_N2 — RG63 1 EMI@ 2 15 +-1% 0402 — HDMI_R_TX_N2
CG72 EMI@ 360 +-5%0402 SD028360080
HDMI_TX_P2 — RG61 1 EMI@ 2 15 +-1% 0402 — HDMI_R_TX_P2
HDMI_TX_P1 — RG65 1 EMI@ 2 15 +-1% 0402 — HDMI_R_TX_P1
CG73 EMI@ 360 +-5%0402 SD028360080
HDMI_TX_N1 — RG10 1 EMI@ 2 15 +-1% 0402 — HDMI_R_TX_N1
HDMI_TX_P0 — RG12 1 EMI@ 2 15 +-1% 0402 — HDMI_R_TX_P0
CG74 EMI@ 360 +-5%0402 SD028360080
HDMI_TX_N0 — RG13 1 EMI@ 2 15 +-1% 0402 — HDMI_R_TX_N0

W=40mils

FG1 (IN, OUT, GND) AP2330W-7_SC59-3 SA00004ZA00
+5VS → +HDMI_CRT_5V
CG46 0.1U_0402_16V7K
CG47 4.7U_0402_6.3V6M

<6,7,9,10,11,13,17,18,27,29,30,31,32,33,36,39,40,52> +3VS
<27,32,33,34,36,37,40> +5VS

+3VS
RG47 1M_0402_5%
<5> HOST_DP1_HPD
QG1A L2N7002SDW1T1G 2N SC88-6 SB00001FF00
HDMI_HPD — RG108 10K_0402_5% — HP_DETECT
RG56 20K_0402_5%
5V Level
@ CM17 220P_0402_50V7K

@ESD@ D21
HDMI_R_TX_N0 ↔ HDMI_R_TX_N0
HDMI_R_TX_P0 ↔ HDMI_R_TX_P0
HDMI_R_CLKN ↔ HDMI_R_CLKN
HDMI_R_CLKP ↔ HDMI_R_CLKP
AZ1045-04F.R7G DFN2510P10E ESD SC300001Y00

@ESD@ D22
HDMI_R_TX_N1 ↔ HDMI_R_TX_N1
HDMI_R_TX_P1 ↔ HDMI_R_TX_P1
HDMI_R_TX_N2 ↔ HDMI_R_TX_N2
HDMI_R_TX_P2 ↔ HDMI_R_TX_P2
AZ1045-04F.R7G DFN2510P10E ESD SC300001Y00

@ESD@ DG1
HP_DETECT ↔ HP_DETECT
HDMI_CTRL_DAT ↔ HDMI_CTRL_DAT
HDMI_CTRL_CLK ↔ HDMI_CTRL_CLK
AZ1045-04F.R7G DFN2510P10E ESD SC300001Y00

<5> HOST_DP1_CTRL_CLK — HOST_DP1_CTRL_CLK — QG2A SB00001FF00 L2N7002SDW1T1G 2N SC88-6 — HDMI_CTRL_CLK
<5> HOST_DP1_CTRL_DATA — HOST_DP1_CTRL_DATA — QG2B SB00001FF00 L2N7002SDW1T1G 2N SC88-6 — HDMI_CTRL_DAT
+3VS

+HDMI_CRT_5V
+3VS
RG105 2.2K_0804_8P4R_5%
HDMI_CTRL_CLK
HDMI_CTRL_DAT
HOST_DP1_CTRL_CLK
HOST_DP1_CTRL_DATA

HDMI Conn.

JHDMI CONN@ ACON_HMRBL-AK120H DC231709273
HP_DET, 5V, DDC/CEC_GND, SDA, SCL, Utility, CEC, CK-, CK_shield, CK+, D0-, D0_shield, D0+, D1-, D1_shield, D1+, D2-, D2_shield, D2+, GND1–GND4
HP_DETECT, +HDMI_CRT_5V, HDMI_CTRL_DAT, HDMI_CTRL_CLK, HDMI_R_CLKN, HDMI_R_CLKP, HDMI_R_TX_N0, HDMI_R_TX_P0, HDMI_R_TX_N1, HDMI_R_TX_P1, HDMI_R_TX_N2, HDMI_R_TX_P2
@ CM26 10P_0402_50V8J
@ CM27 10P_0402_50V8J

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Compal Electronics, Inc.
Title: HDMI Conn/Level shift
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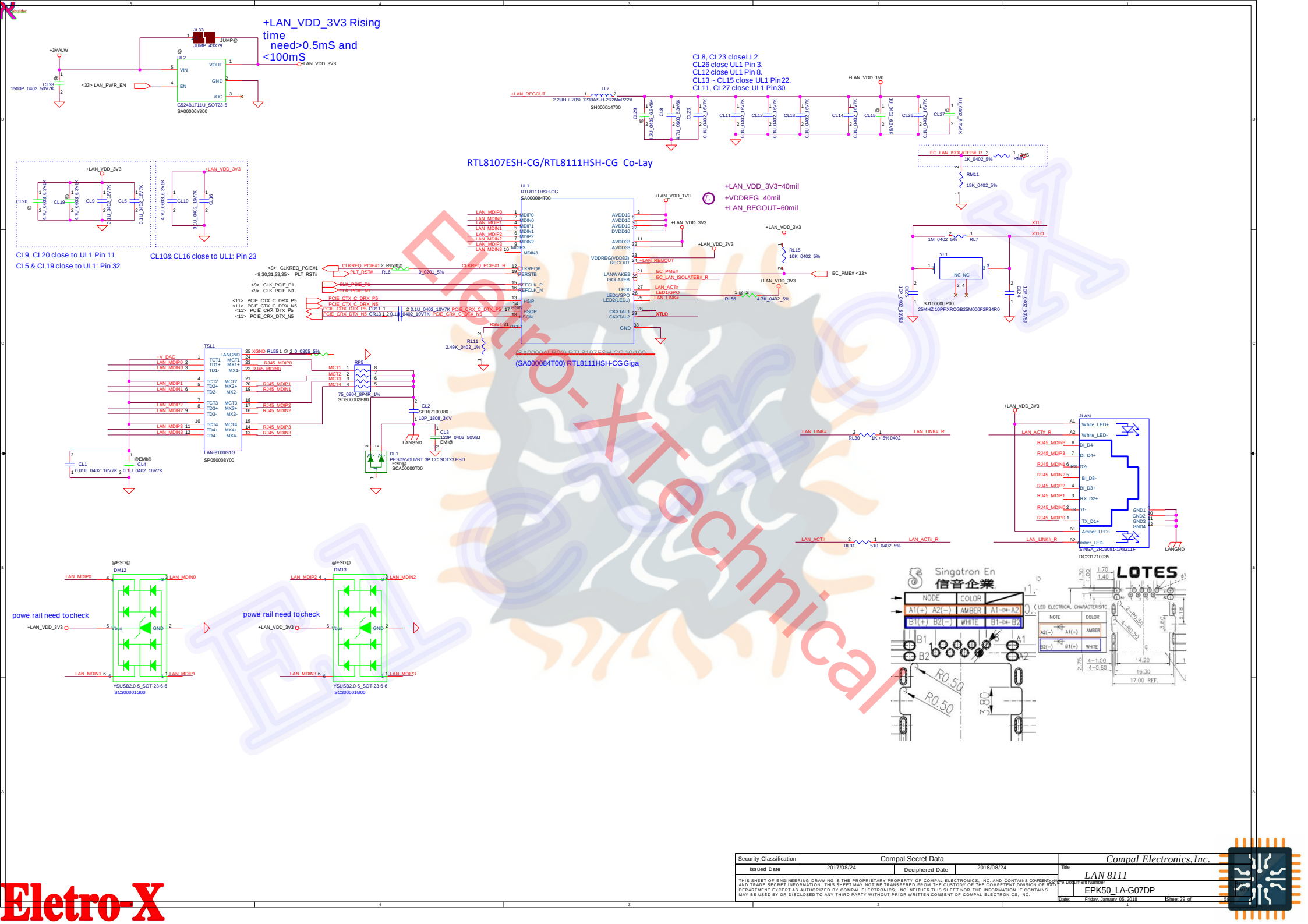

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Compal Electronics, Inc.

Title: LAN 8111

Size: C | Document Number: EPK50_LA-G07DP | Rev: 1.0

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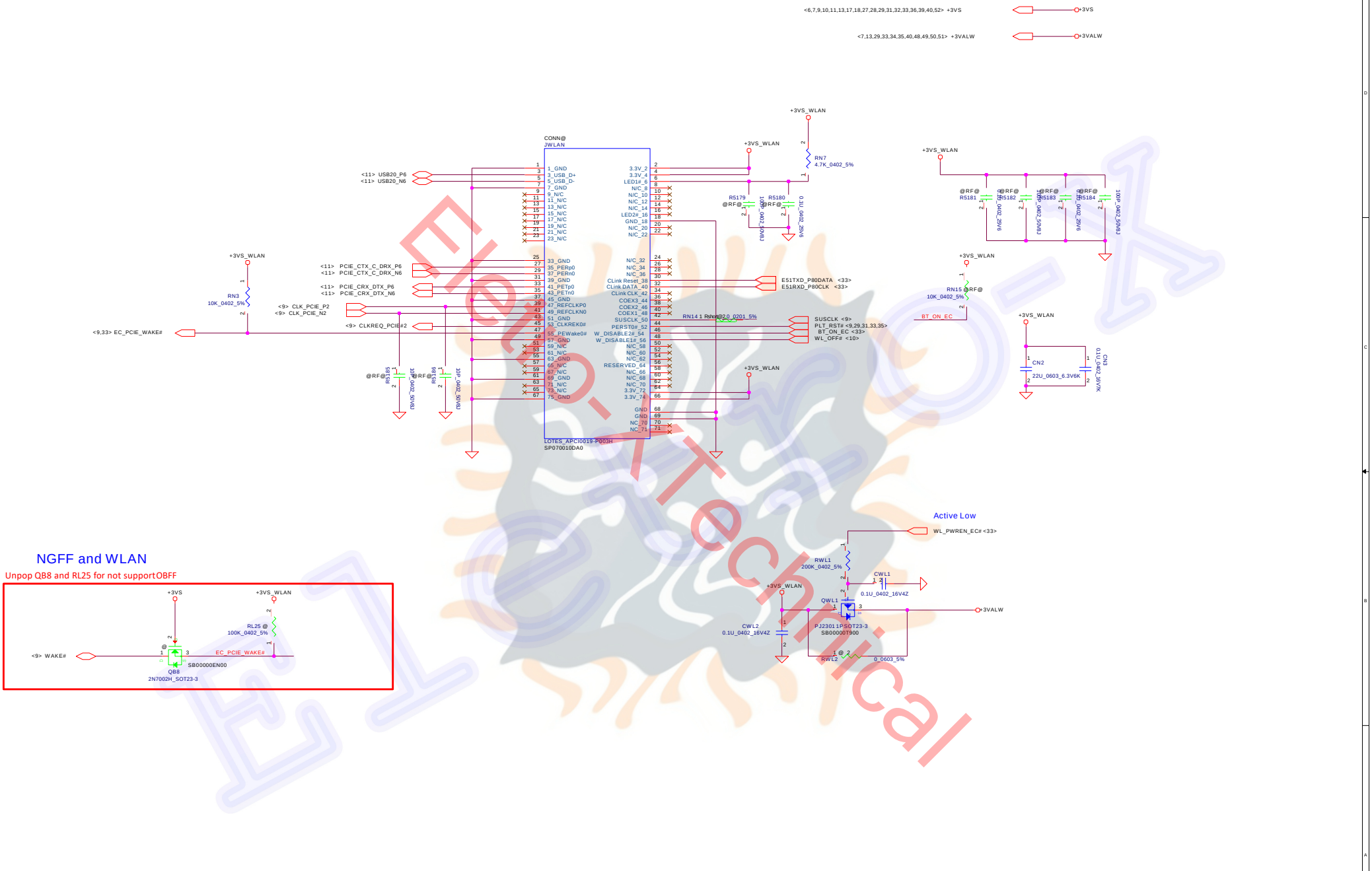

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: WLAN-BT

Size: C | Document Number: EPK50_LA-G07DP | Rev: 1.0

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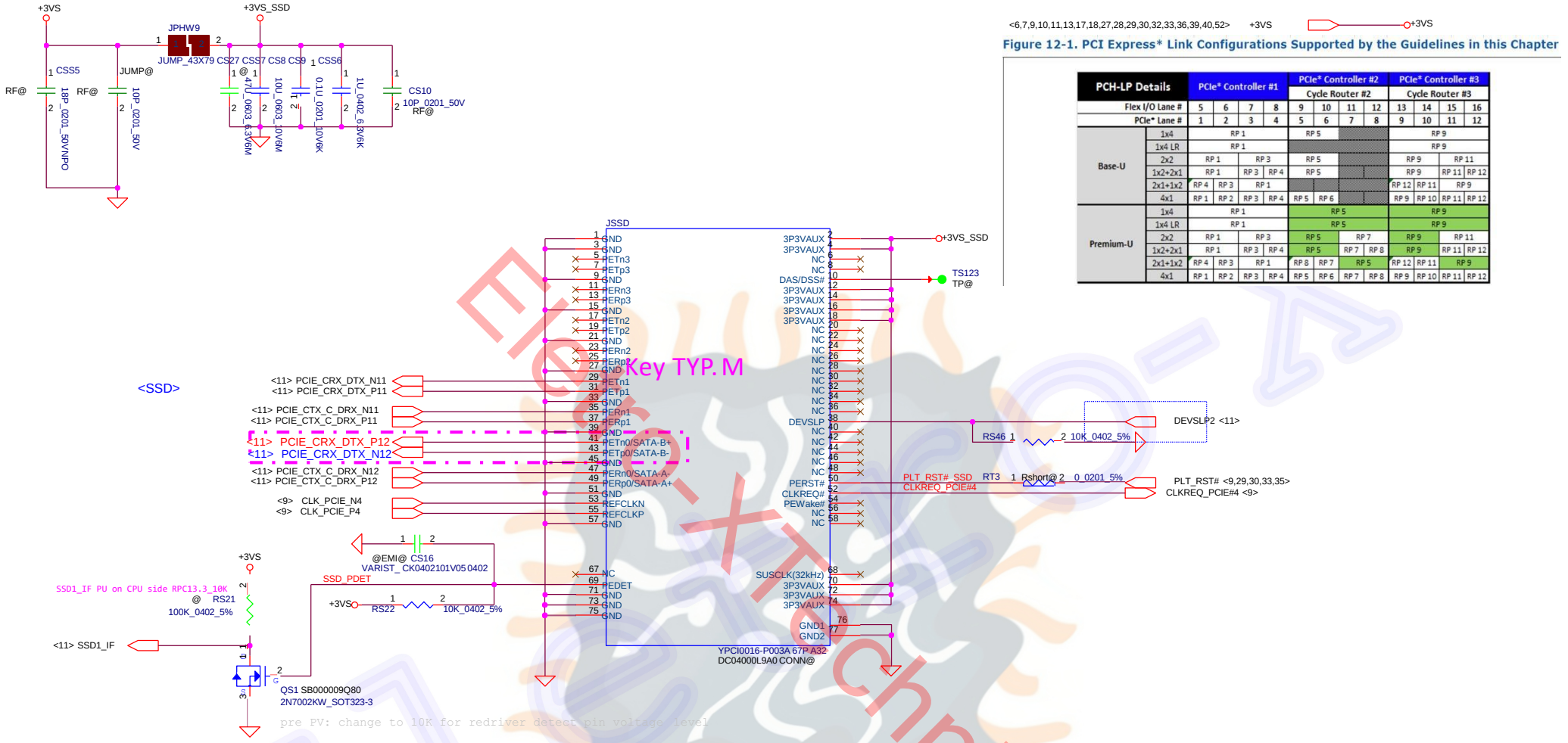

Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2 Cycle Router #2				PCIe* Controller #3 Cycle Router #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP 1				RP 5				RP 9			
	1x4 LR	RP 1								RP 9			
	2x2	RP 1		RP 3		RP 5				RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5				RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1						RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6			RP 9	RP 10	RP 11	RP 12
Premium-U	1x4	RP 1				RP 5				RP 9			
	1x4 LR	RP 1				RP 5				RP 9			
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12

39	GND	PCIeMVMe_DD90000NU90_MZVLW1T0HMLH-000H1 F73H1Q 0FH		
41	PETn0	PCIe TX	42	N/C
43	PETp0	PCIe TX	44	N/C
45	GND	Return current path	46	N/C
47	PERn0	PCIe Rx	48	N/C
49	PERp0	PCIe Rx	50	PERST#
51	GND	Return current path	52	CLKREQ#

39	GND	Return Current Path	40
41	+A TXP	Transmitter Differential Signal Pair	42
43	-A TXN	Transmitter Differential Signal Pair	44
45	GND	Return Current Path	46
47	-A RXN	Receiver Differential Signal Pair	48
49	+A RXP	Receiver Differential Signal Pair	50
51	GND	Return Current Path	52

36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

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Compal Electronics, Inc.

Title: *M.2 SSD*

Size: A4 | Document Number: EPK50_LA-G07DP | Rev: 1.0

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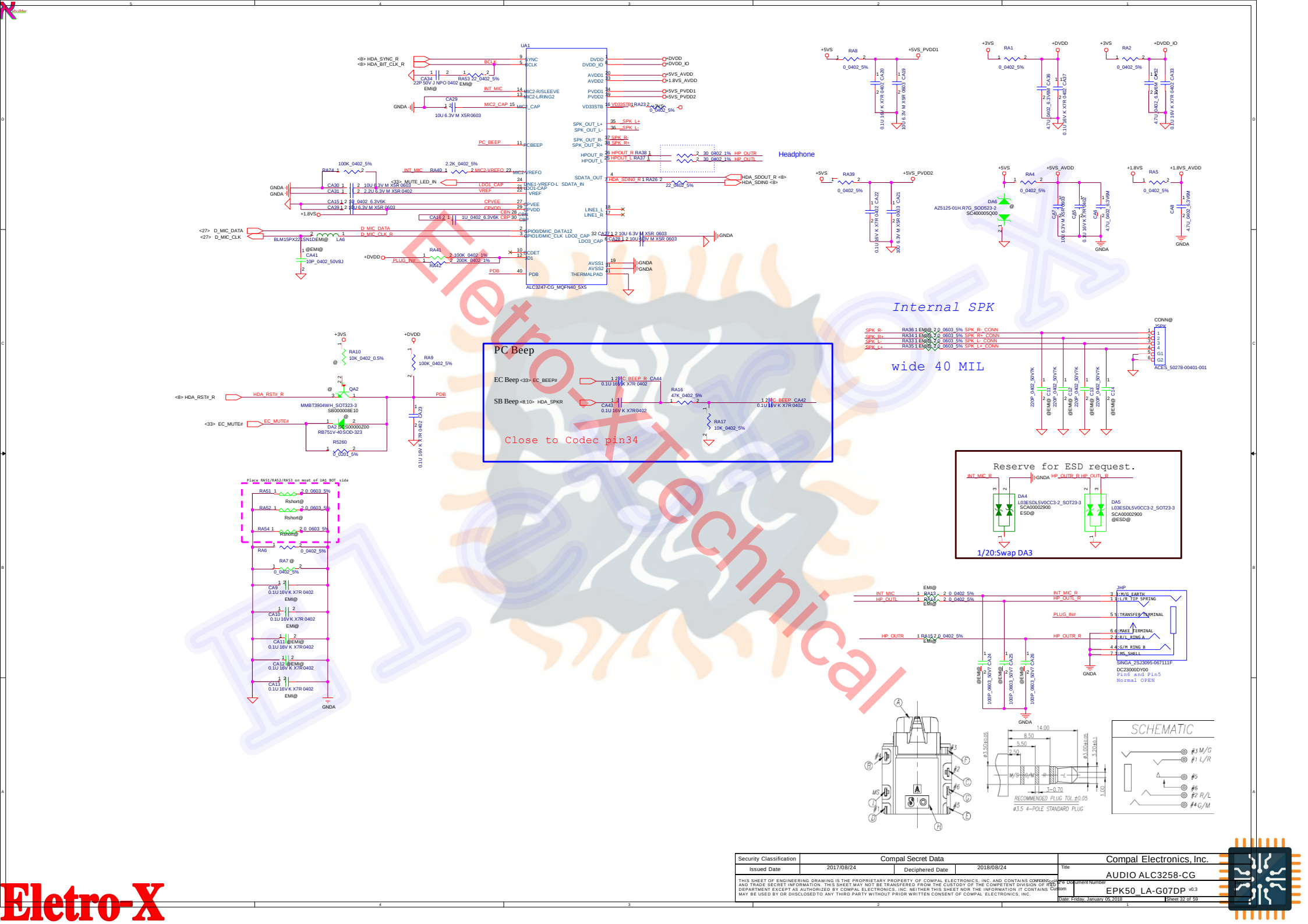

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			Date: Friday, January 05, 2018 Sheet 32 of 59

EC Board ID (UMA, DIS, phase) control table

RK4	KBL-U				KBL-R			
	DB	SI	PV	MV	DB	SI	PV	MV
UMA	15K	27K	43K	75K	130K	200K	270K	430K
DIS	20K	33K	56K	100K	160K	240K	330K	560K

Reserve EC_CLR_CMOS for clear CMOS

U_DB_UMA_15kohm:SD034150280_5 RES 1/16W 15K +-1% 0402
U_DB_DIS_20kohm:SD034200280_5 RES 1/16W 20K +-1% 0402 (2016-03-04 :Confirm intel platform not support EC Clear CMOS function)
U_SI_UMA_27kohm:SD034270280_5 RES 1/16W 27K +-1% 0402 (2017-10-05 : 2018OPP Add EC Clear CMOS function)
U_SI_DIS_33kohm:SD034330280_5 RES 1/16W 33K +-1% 0402
U_PV_UMA_43kohm:SD034430280_5 RES 1/16W 43K +-1% 0402
U_PV_DIS_56kohm:SD034560280_5 RES 1/16W 56K +-1% 0402
U_MV_UMA_75kohm:SD034750280_5 RES 1/16W 75K +-1% 0402
U_MV_DIS_100kohm:SD034100380_5 RES 1/16W 100K +-1% 0402
R_DB_UMA_130kohm:SD034130380_5 RES 1/16W 130K +-1% 0402
R_DB_DIS_160kohm:SD034160380_5 RES 1/16W 160K +-1% 0402
R_SI_UMA_200kohm:SD034200380_5 RES 1/16W 200K +-1% 0402
R_SI_DIS_240kohm:SD000001880_5 RES 1/16W 240K +-1% 0402
R_PV_UMA_270kohm:SD000000280_5 RES 1/16W 270K +-1% 0402
R_PV_DIS_330kohm:SD034330380_5 RES 1/16W 330K +-1% 0402

RK106 2 0_0402_5% CLR_CMOS# <9>
EC_CLR_CMOS → Q51 2N7002K_SOT23-3 SB00000EN00
R483 10K_0402_5%

Int. K/B Matrix

KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7
KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15 KSO16 KSO17

PC & MISC

T2403 TP@ TOUCH_ON
EC_KBRST# SERIRQ LPC_FRAME# LPC_AD3 LPC_AD2 LPC_AD1 LPC_AD0
CLK_PCI_LPC PLT_RST# EC_RST#
EC_SCI# PM_CLKRUN#

PWM Output

EC_VCCST_PG/GPIO0F
BEEP#/GPIO10
EC_FAN_PWM/GPIO12
AC_OFF/GPIO13
EC_VCCST_PG_R <9,40>
EC_BEEP# <32>
FAN_PWM1
CLR_CMOS
EC_FAN_PWM1 <36>

AD Input

VCIN1_BATT_TEMP/AD0/GPIO38
VCIN1_BATT_DROP/AD1/GPIO39
ADP_I/AD2/GPIO3A
AD_BID/AD3/GPIO3B
AD4/GPIO42
AD5/GPIO43
B/I# <46>
ADP_I <45,47>
BOARD_ID
ADP_ID
EC_PME# EC_R
R5178 1 2 0_0201_5%
ADP_ID <45>
EC_PME# <29>

DA Output

DA0/GPIO3C
EN_DFAN1/DA1/GPIO3D
DA2/GPIO3E
DA3/GPIO3F
NMI_DBG#
VR_PWRGD
EC_MUTE#
KBL_ON# <34>
VR_PWRGD <52>
EC_MUTE# <32>

PS2 Interface

EC_MUTE#/PSCLK1/GPIO4A
USB_EN#/PSDAT1/GPIO4B
PSCLK2/GPIO4C
PSDAT2/GPIO4D
TP_CLK/GPIO4E
TP_DATA/GPIO4F
VR_ON
TP_CLK
TP_DATA
VR_ON <40,52>
LAN_PWR_EN <29>
TP_CLK <34>
TP_DATA <34>

SPI Device Interface

SPI Flash ROM

MISO/GPIO5B
MOSI/GPIO5C
SPICLK/GPIO58
SPICS#/GPIO5A
EC_SPI_CLK
EC_SPI_SO <7>
EC_SPI_SI <7>
EC_SPI_CS0# <7>

GPIO

ENKBL/GPXIOA00
WOL_EN/GPXIOA01
ME_EN/GPXIOA02
VCIN0_PH1/GPXIOD00
ENBKL
ME_FLASH_EN
VCIN0_PH
ENBKL <5>
WL_PWREN_EC# <30>
ME_FLASH_EN <8>
VCIN0_PH <45>

EC_CIR_RX/AD6/GPIO40
SYS_PWROK/AD7/GPIO41
GPIO50
BATT_CHG_LED#/GPIO52
CAPS_LED#/GPIO53
PWR_LED#/GPIO54
BATT_LOW_LED#/GPIO55
SYSON/GPIO56
VR_ON/GPIO57
DPWROK_EC/GPIO59
SYS_PWROK
EC_S0IX_EN
BAT_CHG_LED
CAP_LOCK#
PWR_LED#
SYSON
BT_ON_EC
PCH_DPWROK
TS_GPIO_EC <27>
SYS_PWROK <9>
EC_S0IX_EN <12>
BAT_CHG_LED <45>
CAP_LOCK# <34>
PWR_LED# <39>
ACIN <9>
SYSON <12,40,49>
BT_ON <30>
PCH_DPWROK <9>

SM Bus

EC_SMB_CK1/GPIO44
EC_SMB_DAT1/GPIO45
EC_SMB_CLK2/GPIO46
EC_SMB_DAT2/GPIO47
EC_SMB_CK2_R
EC_SMB_DA2_R

GPIO GPO

EC_RSMRST#/GPXIOA03
GPXIOA04
VCIN1_ADP_PROCHOT/GPXIOA05
VCOUT1_PROCHOT#/GPXIOA06
VCOUT0_MAIN_PWR_ON/GPXIOA07
BKOFF#/GPXIOA08
GPXIOA09
PCH_PWR_EN/GPXIOA10
PWR_VCCST_PG/GPXIOA11
PCH_RSMRST#
USB_ON#
VCIN1_PH
H_PROCHOT#_EC
MAINPWON
EC_BKOFF#
+1.0VS_PG
PCH_PWR_EN
PCH_RSMRST# <9>
USB_ON# <38,39>
VCIN1_PH <45>
MAINPWON <48>
EC_BKOFF# <27>
DGPU_PWR_EN <10,24>
PCH_PWR_EN <40,51>
+1.0VS_PG <50>

GPI

VCIN1_AC_IN/GPXIOD01
ALW_PWR_EN EC_ON/GPXIOD02
ON/OFF#/GPXIOD03
LID_SW#/GPXIOD04
SUSP#/GPXIOD05
GPXIOD06
PEC/GPXIOD07
V18R/VCC_IO2
EC_ON
ON/OFF#
LID_SW#
SUSP#
VCIN1_AC_IN
EC_PECI
+V18R
EC_ON <39,48>
ON/OFF# <39>
LID_SW# <39>
SUSP# <12,40,49>
H_PECI <5>
+3VALW_EC

KB9022QD_LQFP128_14X14
SA000075S30
20mil

Power

+3VL
+3VALW_EC
+3V_EC_VDD
+3V_LID
+5VS
+3VS
+3VALW
+3V_SMBUS

LK1 SM01000Q500 S SUPPRE_ TAI-TECH HCB1005KF-221T15 0402
LK2 SM01000Q500 TAI-TECH HCB1005KF-221T15 0402
ECAGND
AGND
GND

For Solve tPCH04(Min 9ms) Sequence Timing

VCIN1_ACOK R4958 0_0402_5%
VCIN1_AC_IN_R R5094 0_0402_5%
VCIN1_AC_IN_R R4960 0_0402_5%

EMI request

CC128 RC369 place near ECSide
EC_SPI_CLK RC369 EMI@ 15_0402_5%
HOST_SPI_0_CLK_R <7,35>
CC144 22P 50V J NPO 0402 @EMI@

Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

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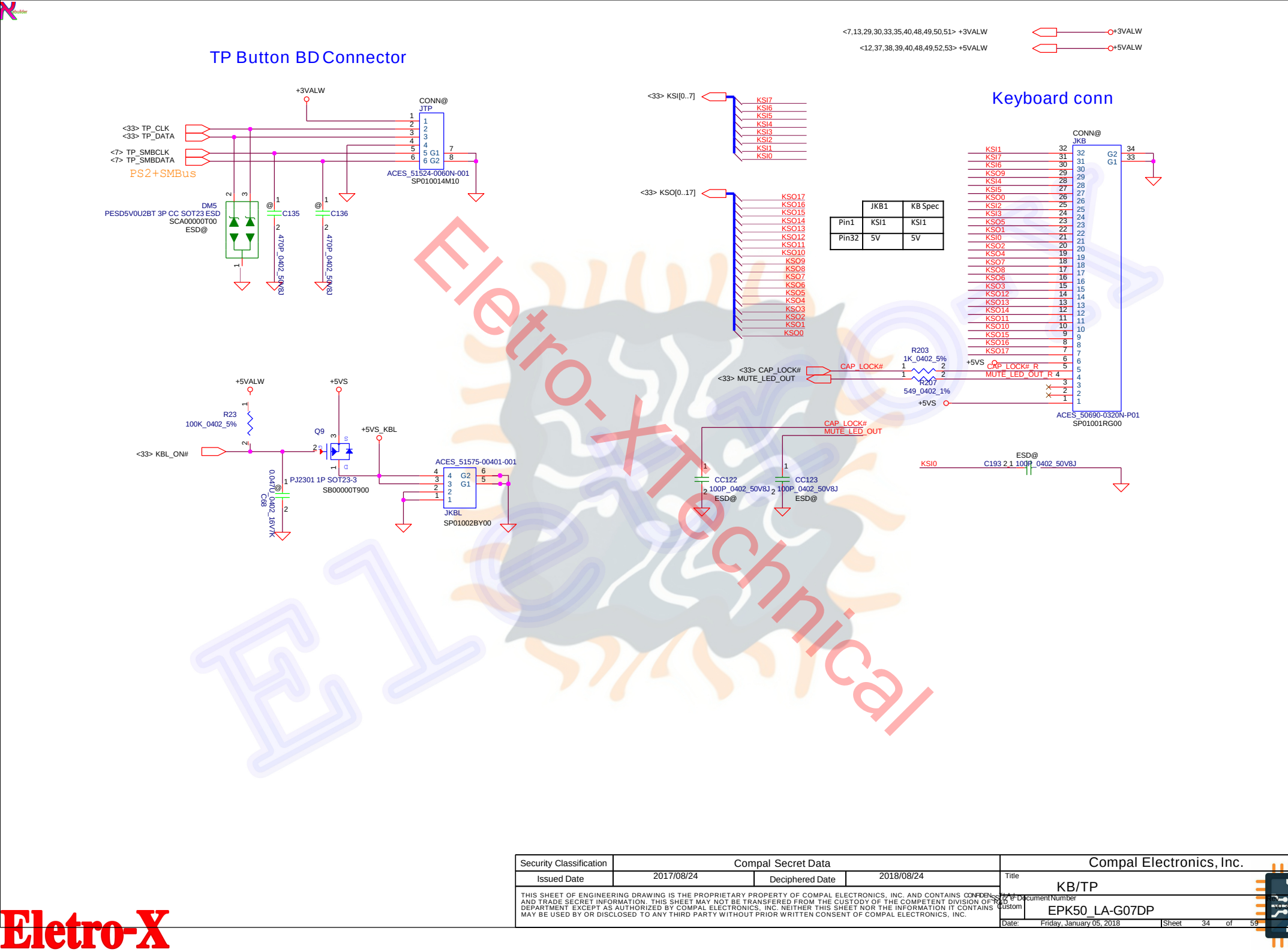
Title: EC ENE-KB9022

Size: Custom | Document Number: EPK50_LA-G07DP | Rev: 0.3

Date: Tuesday, January 09, 2018 | Sheet 33 of



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

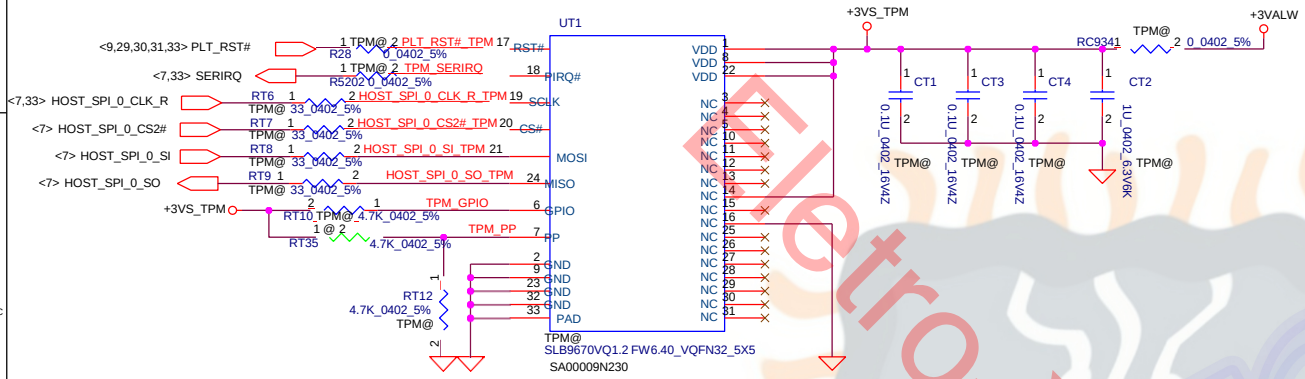
Title: KB/TP

Size: Custom | Document Number: EPK50_LA-G07DP | Rev: 1.0

Date: Friday, January 05, 2018 | Sheet 34 of 59

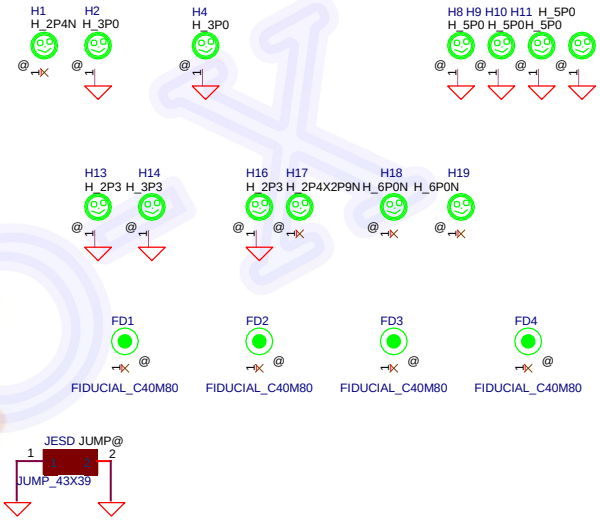
+3VALW +3VALW <7,13,29,30,33,34,40,48,49,50,51>

TPM2.0



Screw Hole

CPU



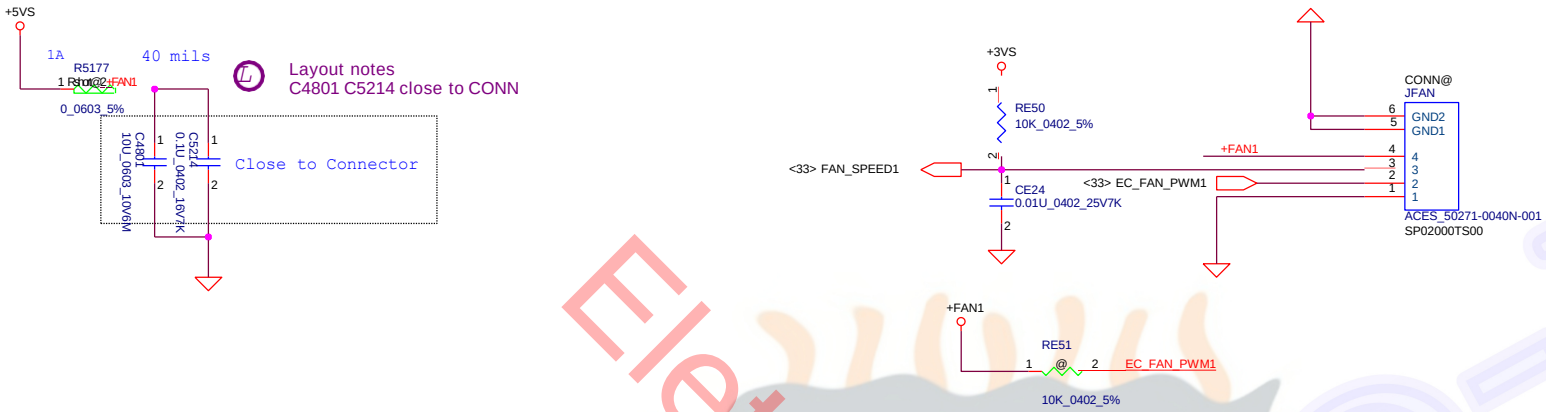
Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: TPM/Screw

Size: A3 | Document Number: EPK50_LA-G07DP | Rev: 1.0

Date: Friday, January 05, 2018 | Sheet 35 of 59



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: FAN

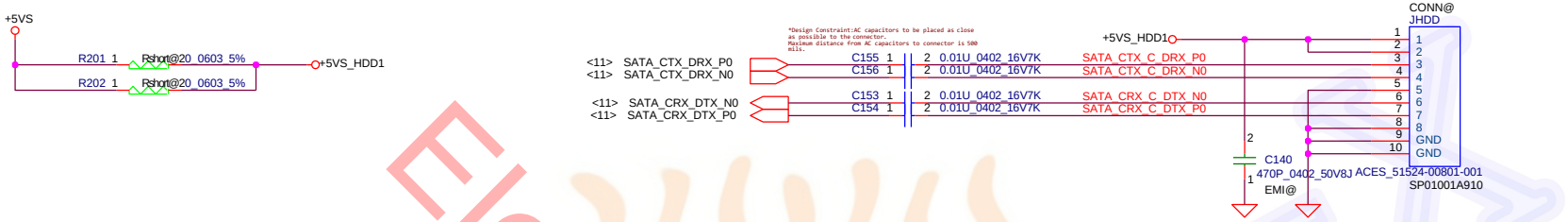
Size: Custom | Document Number: EPK50_LA-G07DP | Rev: 1.0

Date: Friday, January 05, 2018 | Sheet 36 of 59

2.5" SATA HDD

<27,28,32,33,34,36,40> +5VS
<12,34,38,39,40,48,49,52,53> +5VALW
<7,13,29,30,33,34,35,40,48,49,50,51> +3VALW

<PV> change short pad



SATA ODD

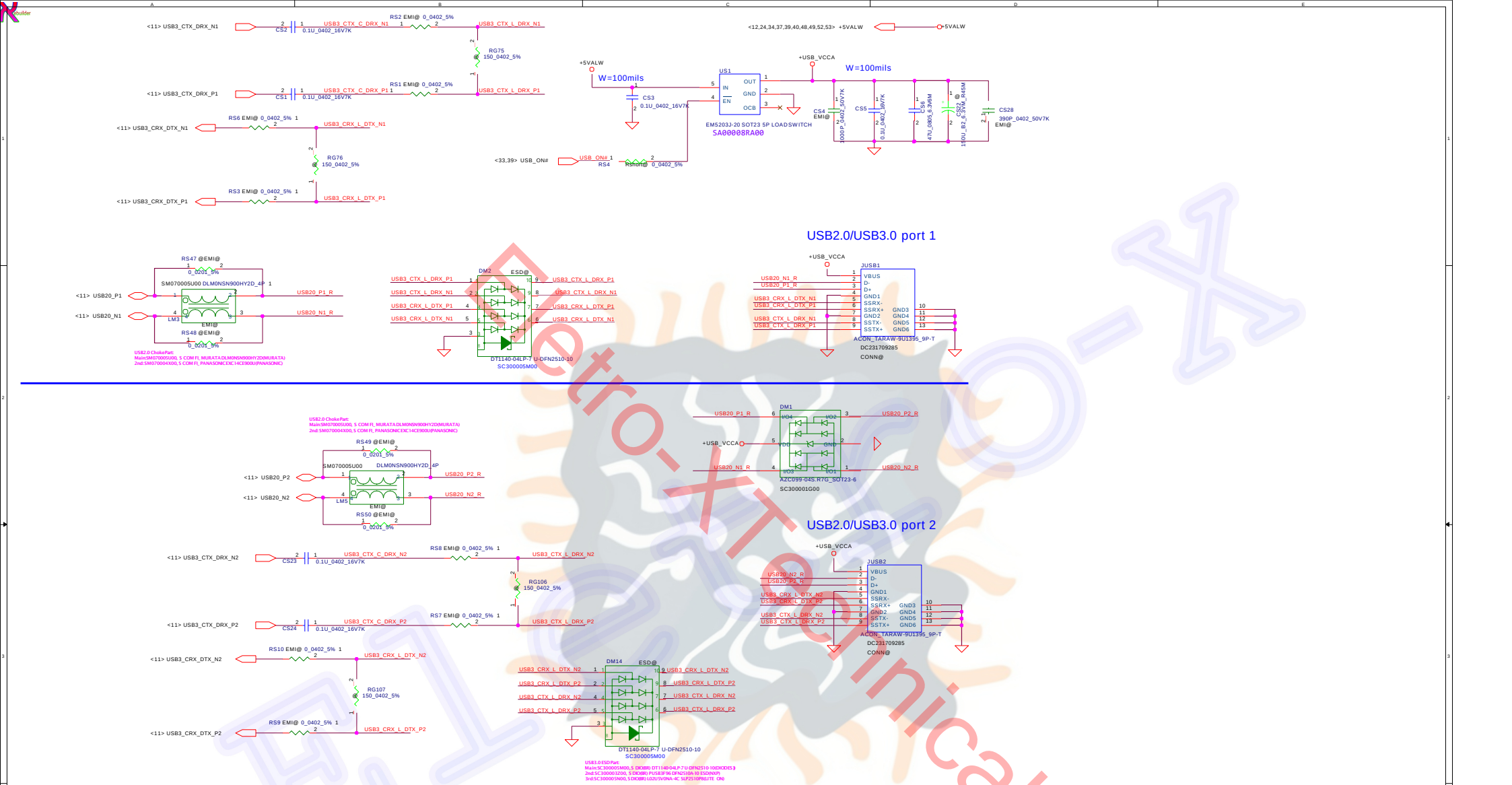
Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: HDD/ODD Conn

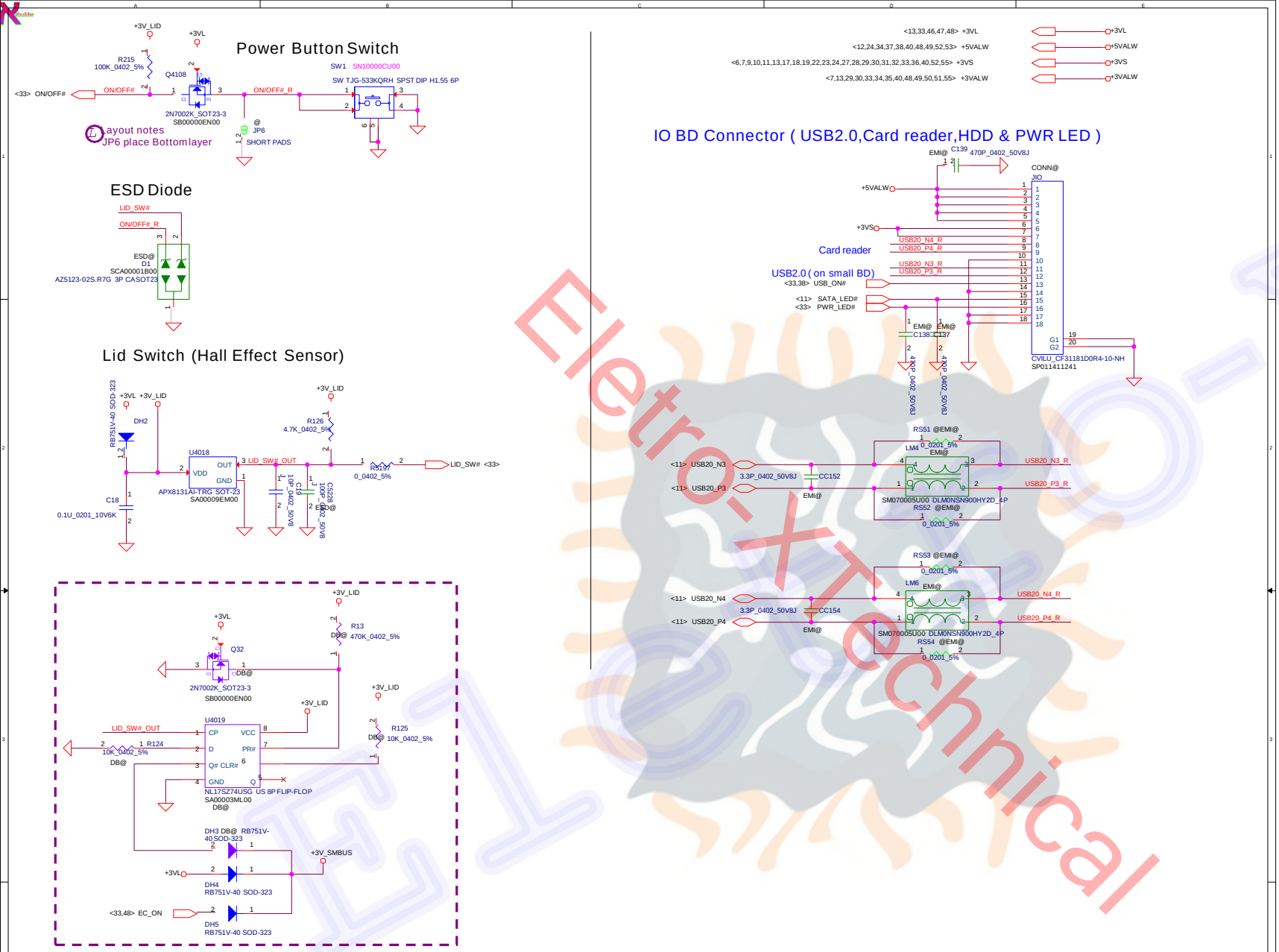
Size: Custom | Document Number: EPK50_LA-G07DP | Rev: 0.3

Date: Friday, January 05, 2018 | Sheet 37 of 59

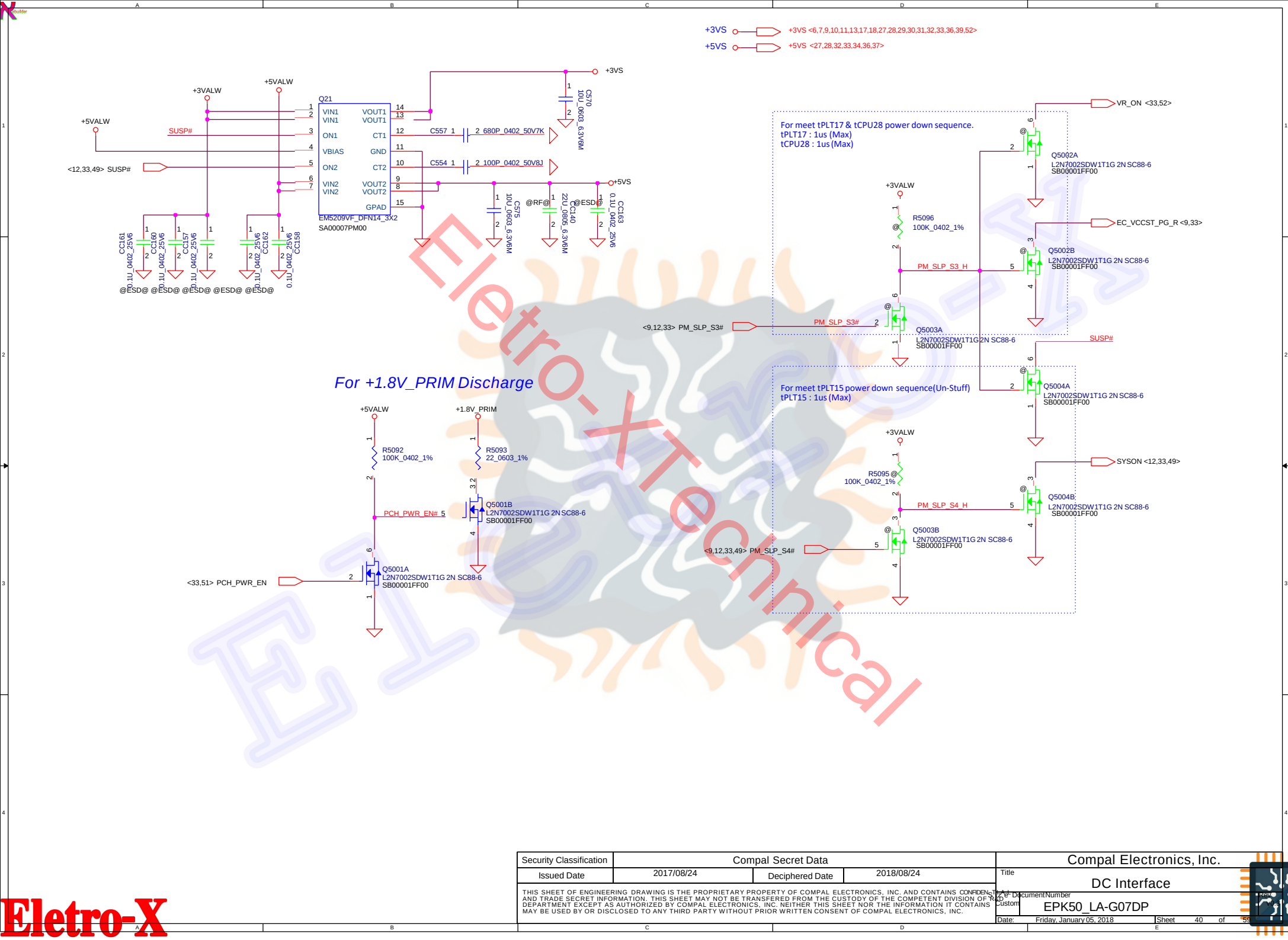


Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.	
Title	USB 3.0/2.0 conn
Size	Custom
Document Number	EPK50_LA-G07DP
Date: Tuesday, January 09,2018	Sheet 38 of 59



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/08/24	Deciphered Date	2018/08/24
Title	IO CON		
Size	Document Number		Rev
Custom	EPK50_LA-G07DP		v0.3
Date:	Tuesday, January 09, 2018		Sheet 39 of 59



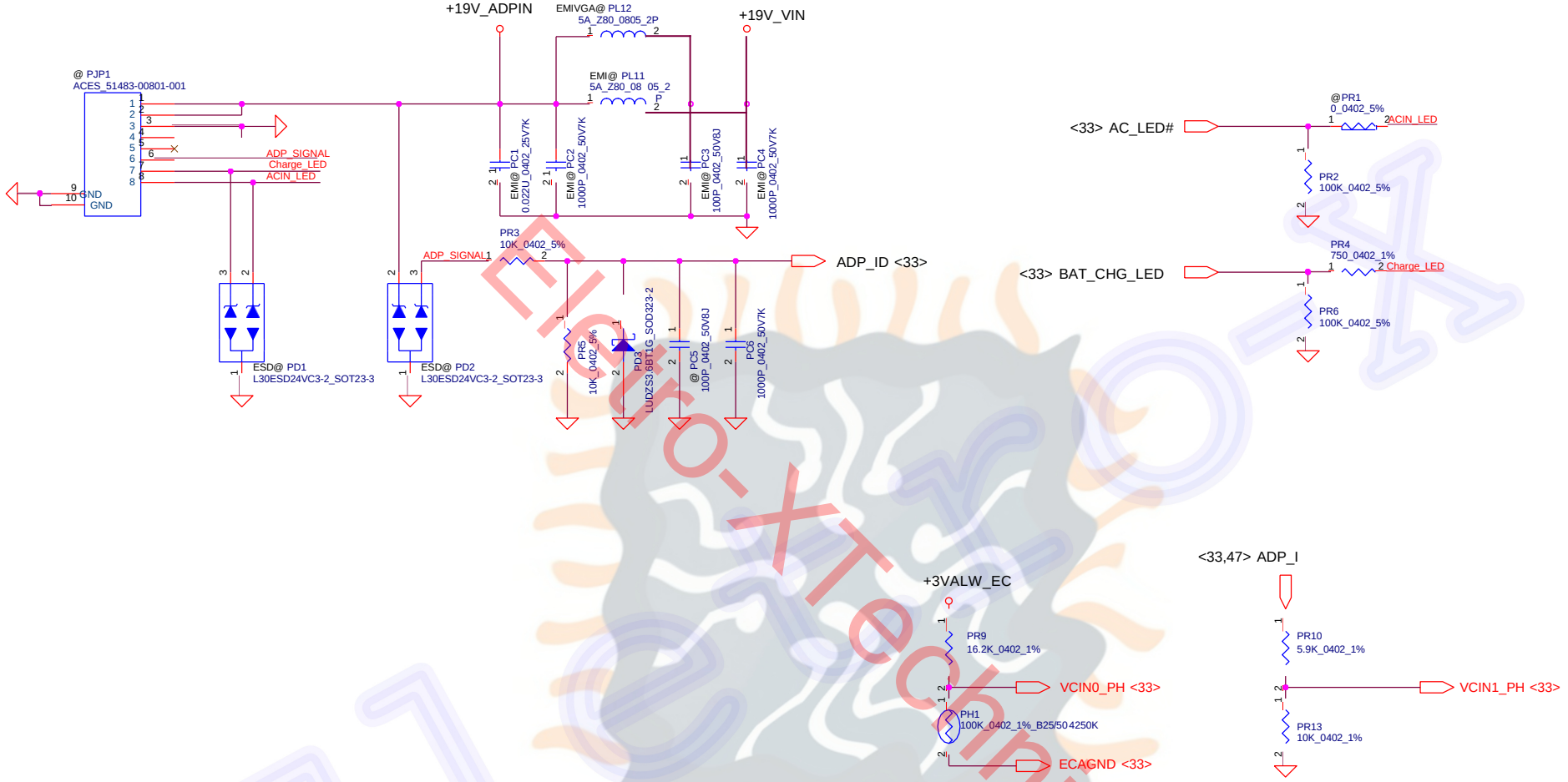
Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: DC Interface

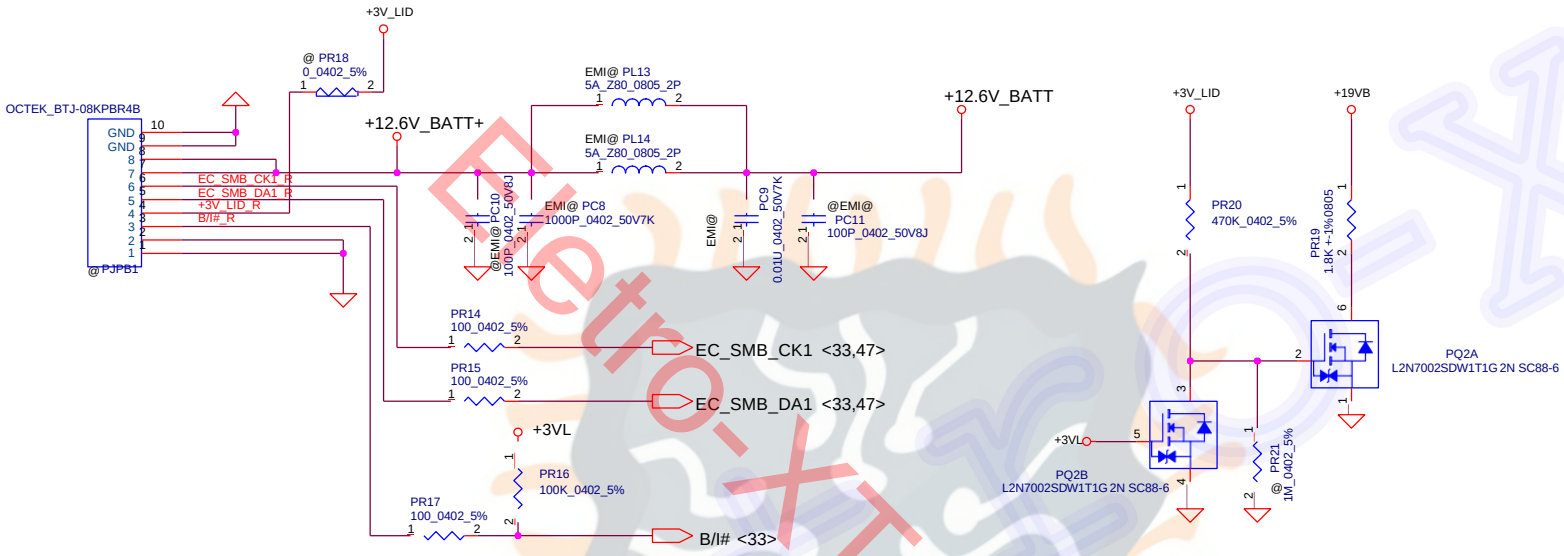
Size: Custom | Document Number: EPK50_LA-G07DP | Rev: 1.0

Date: Friday, January 05, 2018 | Sheet 40 of 59



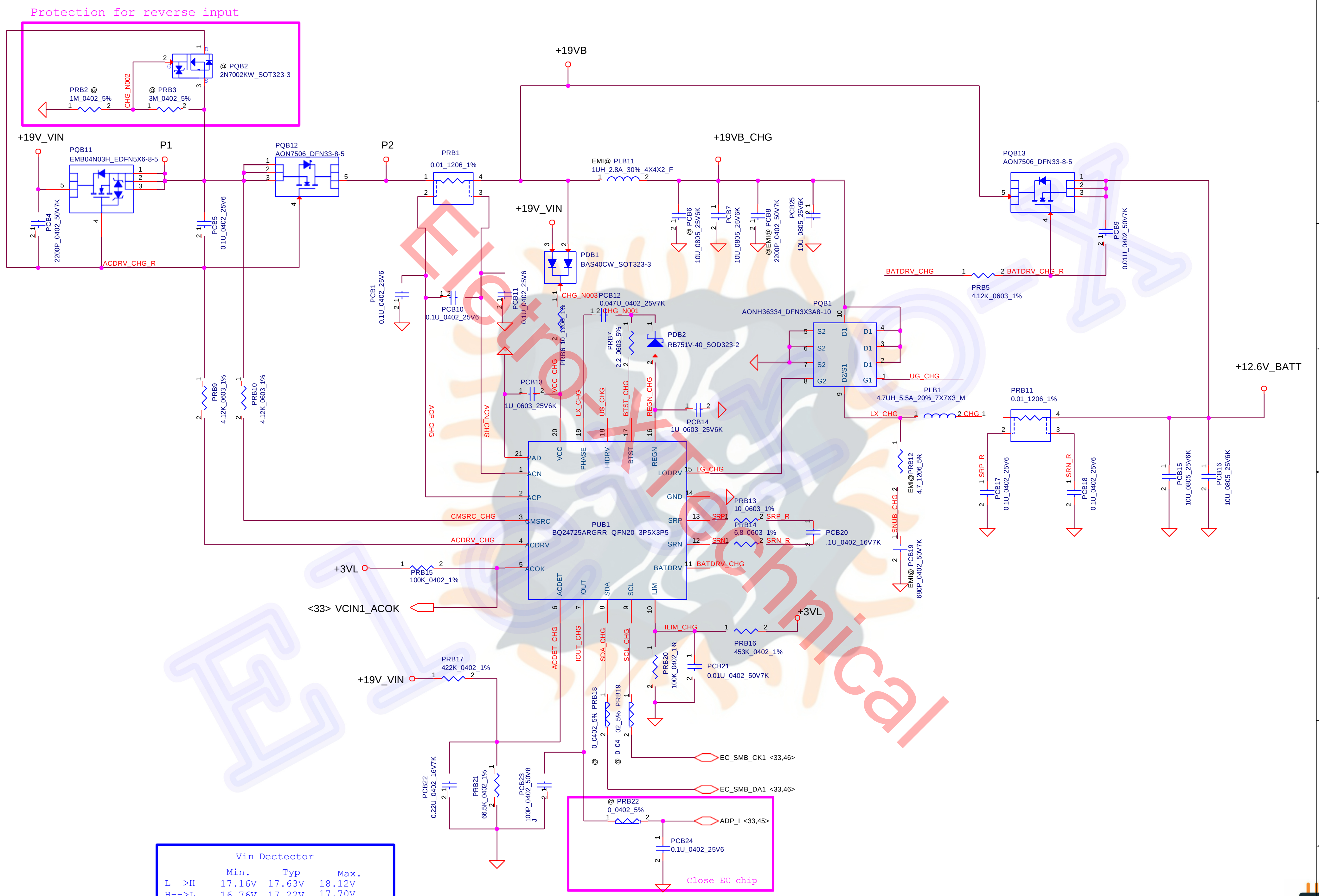
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Title	DC Conn		
Size	Document Number		Rev
A3	EPK50_LA-G07DP		V0.3
Date:	Friday, January 05, 2018	Sheet 45	of



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Title	*BATT Conn*		
Size	Document Number		Rev
A3	EPK50_LA-G07DP		1.0
Date:	Friday, January 05, 2018	Sheet	46 of



Protection for reverse input
@ PQB2
2N7002KW_SOT323-3
PRB2 @
1M_0402_5%
@ PRB3
3M_0402_5%
CHG_N002
+19V_VIN
P1
PQB11
EMB04N03H_EDFN5X6-8-5
PCB4
2200P_0402_50V7K
PCB5
0.1U_0402_25V6
ACDRV_CHG_R
PQB12
AON7506_DFN33-8-5
P2
+19VB
PRB1
0.01_1206_1%
+19V_VIN
EMI@ PLB11
1UH_2.8A_30%_4X4X2_F
+19VB_CHG
PCB6
@ 10U_0805_25V6K
PCB7
10U_0805_25V6K
PCB8
@EMI@ 2200P_0402_50V7K
PCB25
10U_0805_25V6K
PQB13
AON7506_DFN33-8-5
PCB9
0.01U_0402_50V7K
BATDRV_CHG
PRB5
4.12K_0603_1%
BATDRV_CHG_R
PDB1
BAS40CW_SOT323-3
CHG_N003
PCB12
0.047U_0402_25V7K
CHG_N001
PCB1
0.1U_0402_25V6
PCB10
0.1U_0402_25V6
PCB11
0.1U_0402_25V6
PRB6 10_1206_1%
PRB7
2.2_0603_5%
PDB2
RB751V-40_SOD323-2
PQB1
AONH36334_DFN3X3A8-10
UG_CHG
PLB1
4.7UH_5.5A_20%_7X7X3_M
+12.6V_BATT
PRB11
0.01_1206_1%
LX_CHG
CHG
PCB13
1U_0603_25V6K
VCC_CHG
LX_CHG
UG_CHG
BTST_CHG
REGN_CHG
PCB14
1U_0603_25V6K
PRB9
4.12K_0603_1%
PRB10
4.12K_0603_1%
ACP_CHG
ACN_CHG
PAD
ACN
ACP
CMSRC
ACDRV
ACOK
VCC
PHASE
HIDRV
BTST
REGN
LODRV
GND
SRP
SRN
BATDRV
ACDET
IOUT
SDA
SCL
ILIM
PUB1
BQ24725ARGRR_QFN20_3P5X3P5
LG_CHG
PRB13
10_0603_1%
SRP1
SRP_R
PRB14
6.8_0603_1%
SRN1
SRN_R
PCB20
.1U_0402_16V7K
BATDRV_CHG
CMSRC_CHG
ACDRV_CHG
EMI@PRB12
4.7_1206_5%
SNUB_CHG
EMI@ PCB19
680P_0402_50V7K
SRP_R
PCB17
0.1U_0402_25V6
SRN_R
PCB18
0.1U_0402_25V6
PCB15
10U_0805_25V6K
PCB16
10U_0805_25V6K
+3VL
PRB15
100K_0402_1%
<33> VCIN1_ACOK
ACDET_CHG
IOUT_CHG
SDA_CHG
SCL_CHG
ILIM_CHG
+3VL
PRB16
453K_0402_1%
PRB20
100K_0402_1%
PCB21
0.01U_0402_50V7K
+19V_VIN
PRB17
422K_0402_1%
PRB18
@ 0_0402_5%
PRB19
@ 0_0402_5%
EC_SMB_CK1 <33,46>
EC_SMB_DA1 <33,46>
PCB22
0.22U_0402_16V7K
PRB21
66.5K_0402_1%
PCB23
100P_0402_50V8J
@ PRB22
0_0402_5%
ADP_I <33,45>
PCB24
0.1U_0402_25V6
Close EC chip

Vin Dectector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+620)/20/0.02
= 2.291 A

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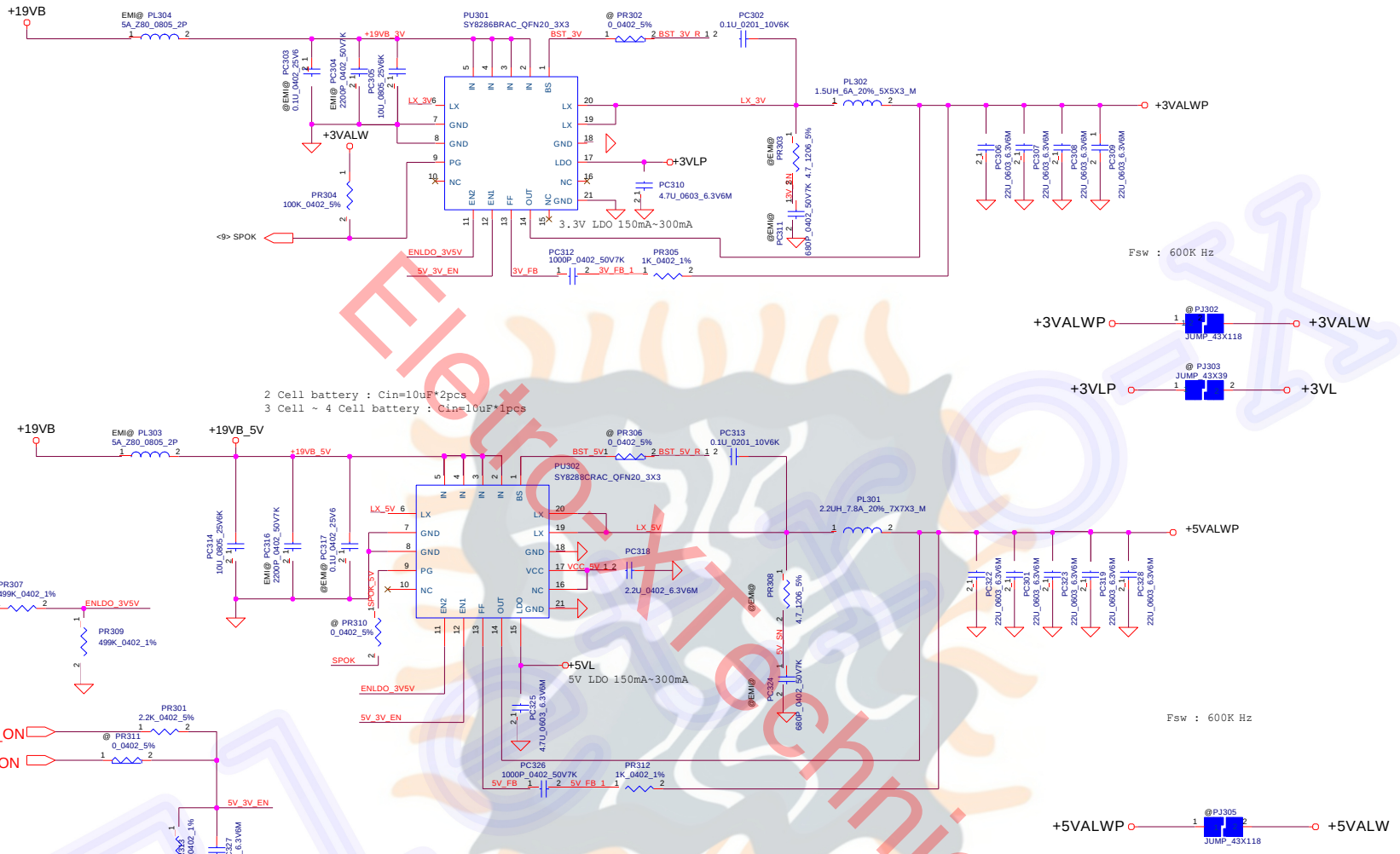
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: CHARGER

Document Number

Date: Friday, January 05, 2018 | Sheet 47 of 59



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date 2019/09/01	Title: 3VALW/5VALW
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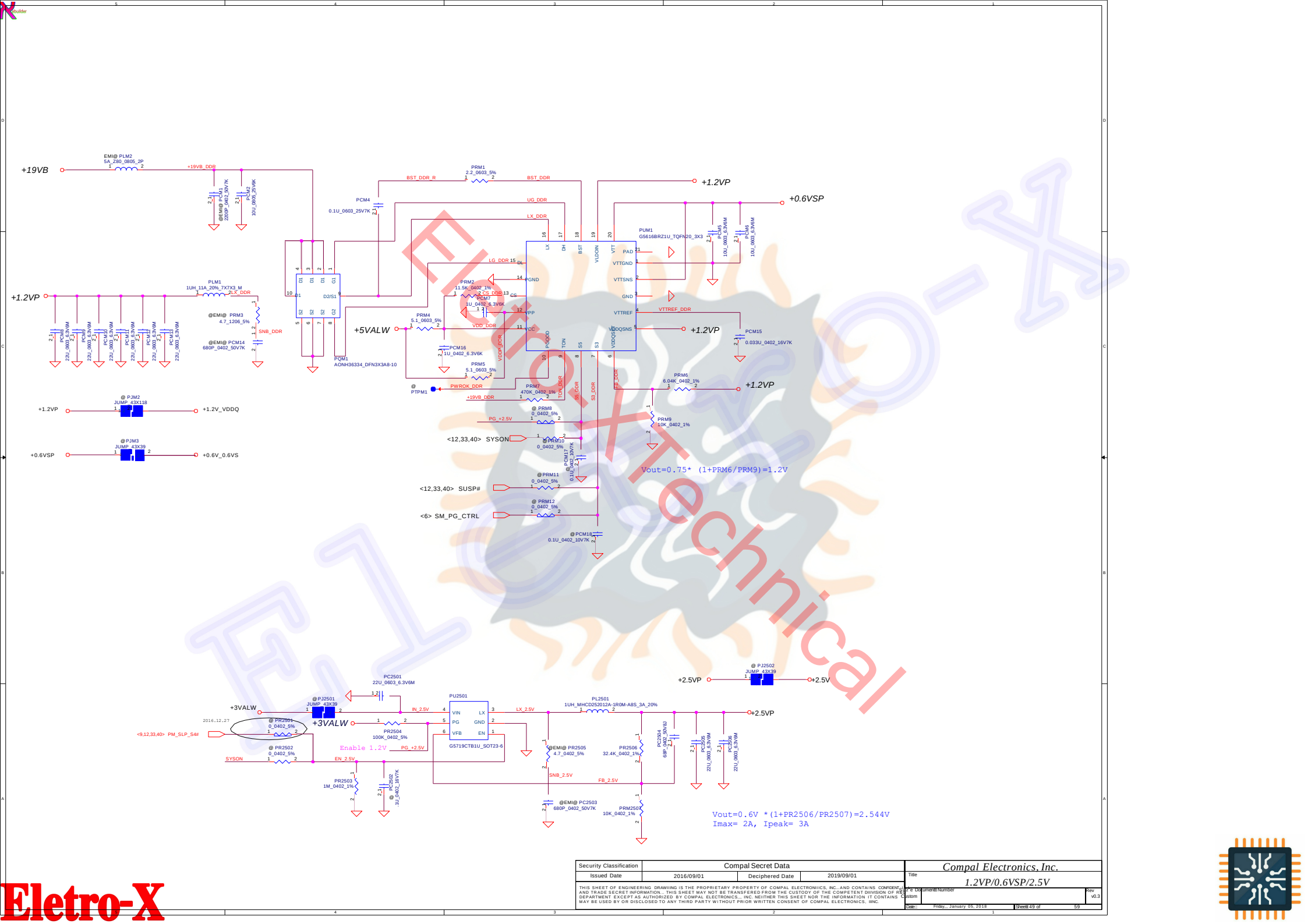
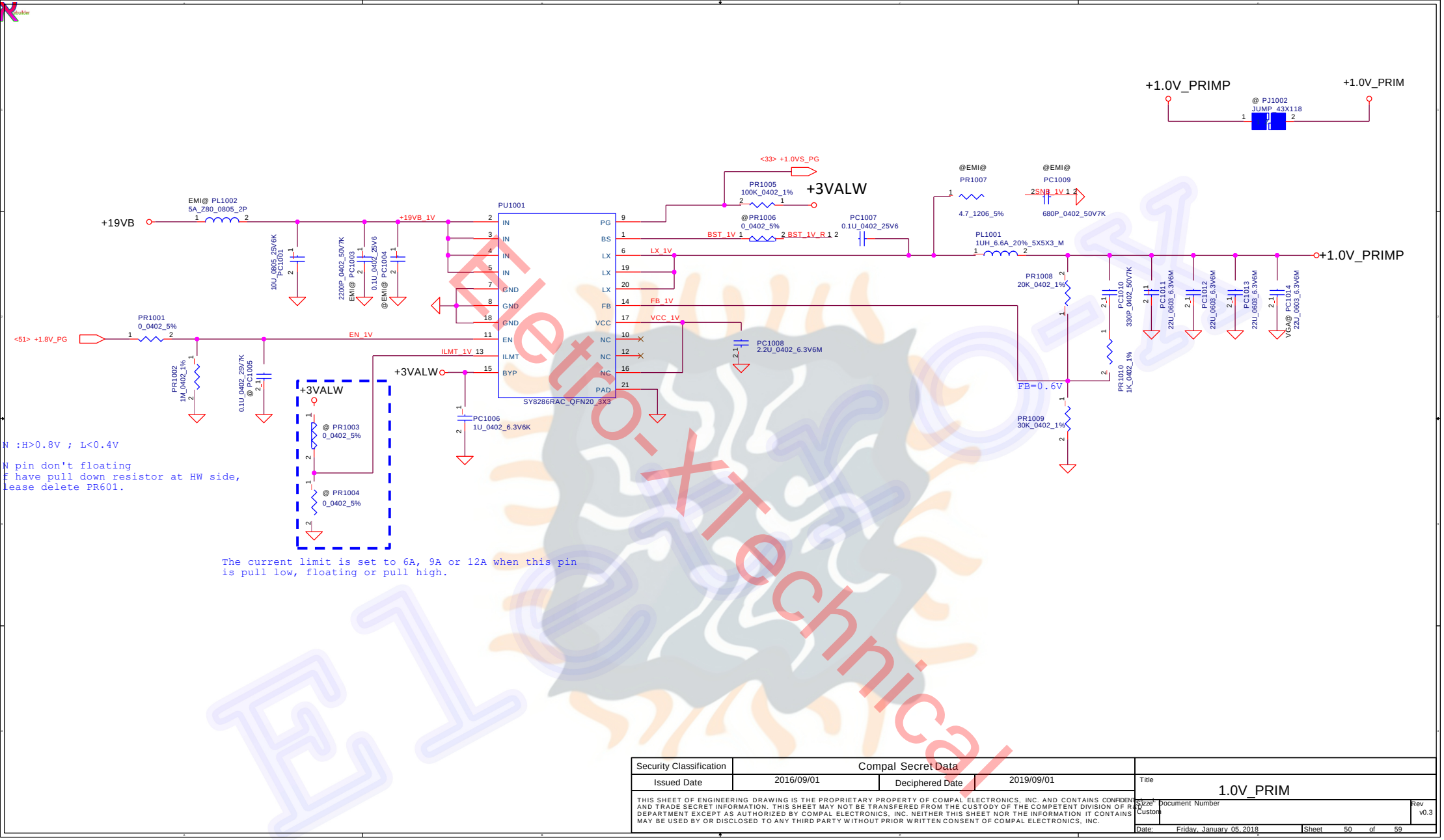
			Date: Friday, January 05, 2018; Sheet 48 of 59



Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.	
Title	1.2VP/0.6VSP/2.5V
Size: Custom	Document Number
Rev	V0.3
Date: Friday, January 05, 2018	Sheet 49 of 59

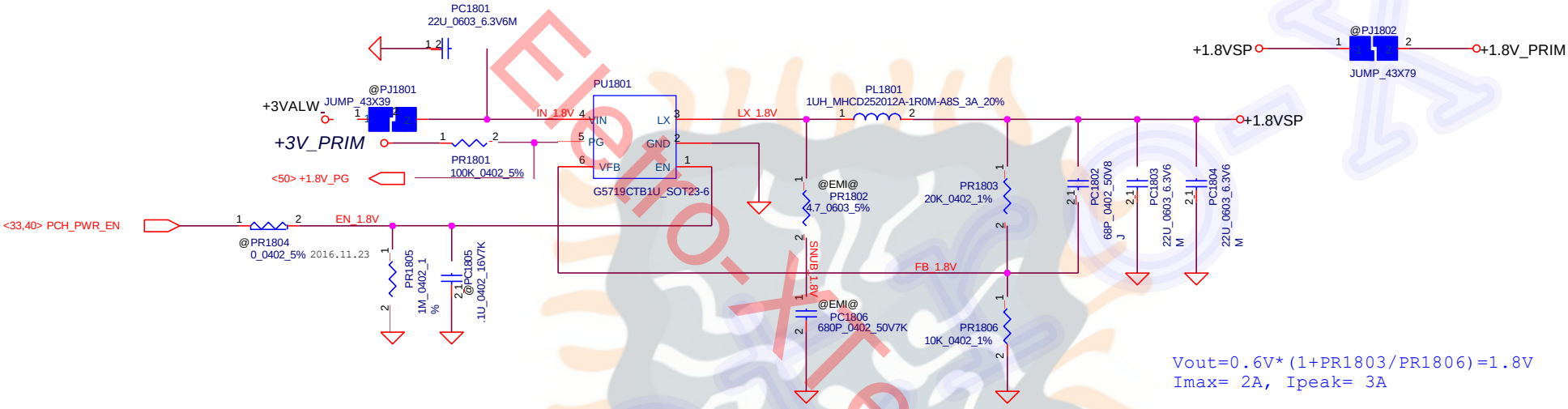


Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Title: 1.0V_PRIM

Size: Custom | Document Number | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 50 of 59



Vout=0.6V*(1+PR1803/PR1806)=1.8V
Imax= 2A, Ipeak= 3A

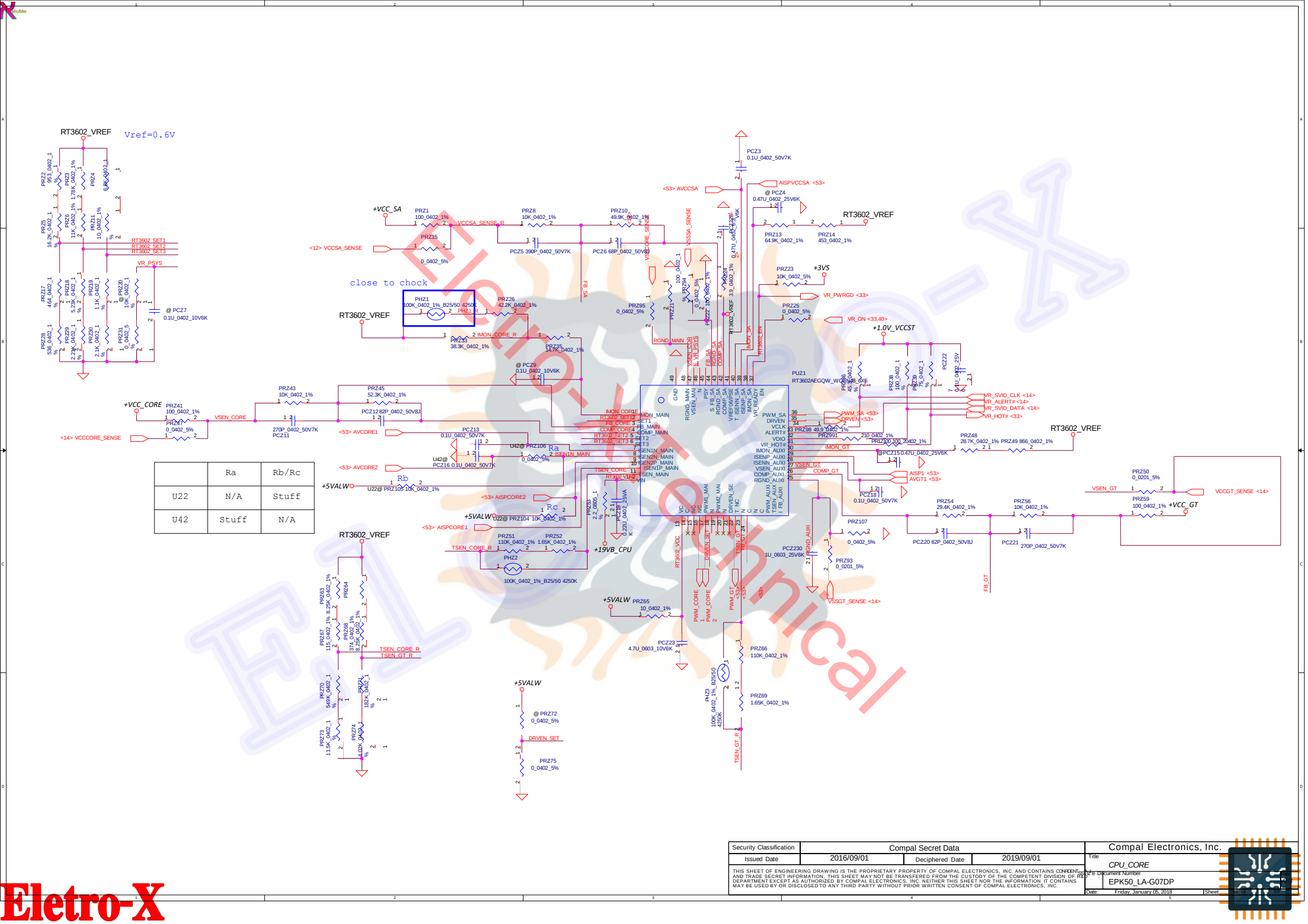
Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: *1.8V_PRIM*

Size: B | Document Number: EPK50_LA-G07DP | Rev: v0.3

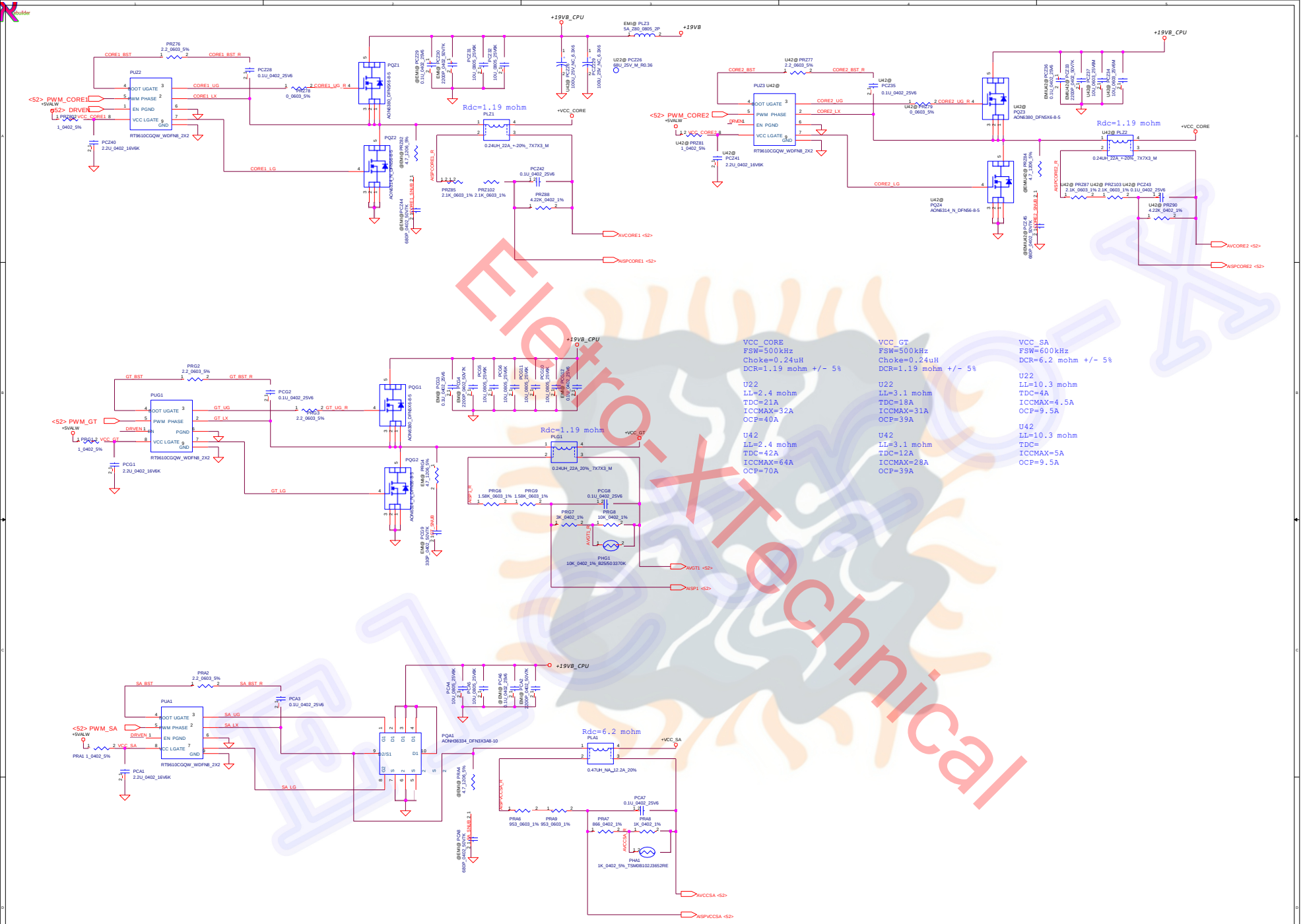
Date: | Sheet 51 of 59



	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Title	CPU_CORE		
Size	Document Number	EPK50_LA-G07DP	Rev
Date:	Friday, January 05, 2018	Sheet	39 of 89



VCC_CORE
FSW=500kHz
Choke=0.24uH
DCR=1.19 mohm +/- 5%

U22
LL=2.4 mohm
TDC=21A
ICCMAX=32A
OCP=40A

U42
LL=2.4 mohm
TDC=42A
ICCMAX=64A
OCP=70A

VCC_GT
FSW=500kHz
Choke=0.24uH
DCR=1.19 mohm +/- 5%

U22
LL=3.1 mohm
TDC=18A
ICCMAX=31A
OCP=39A

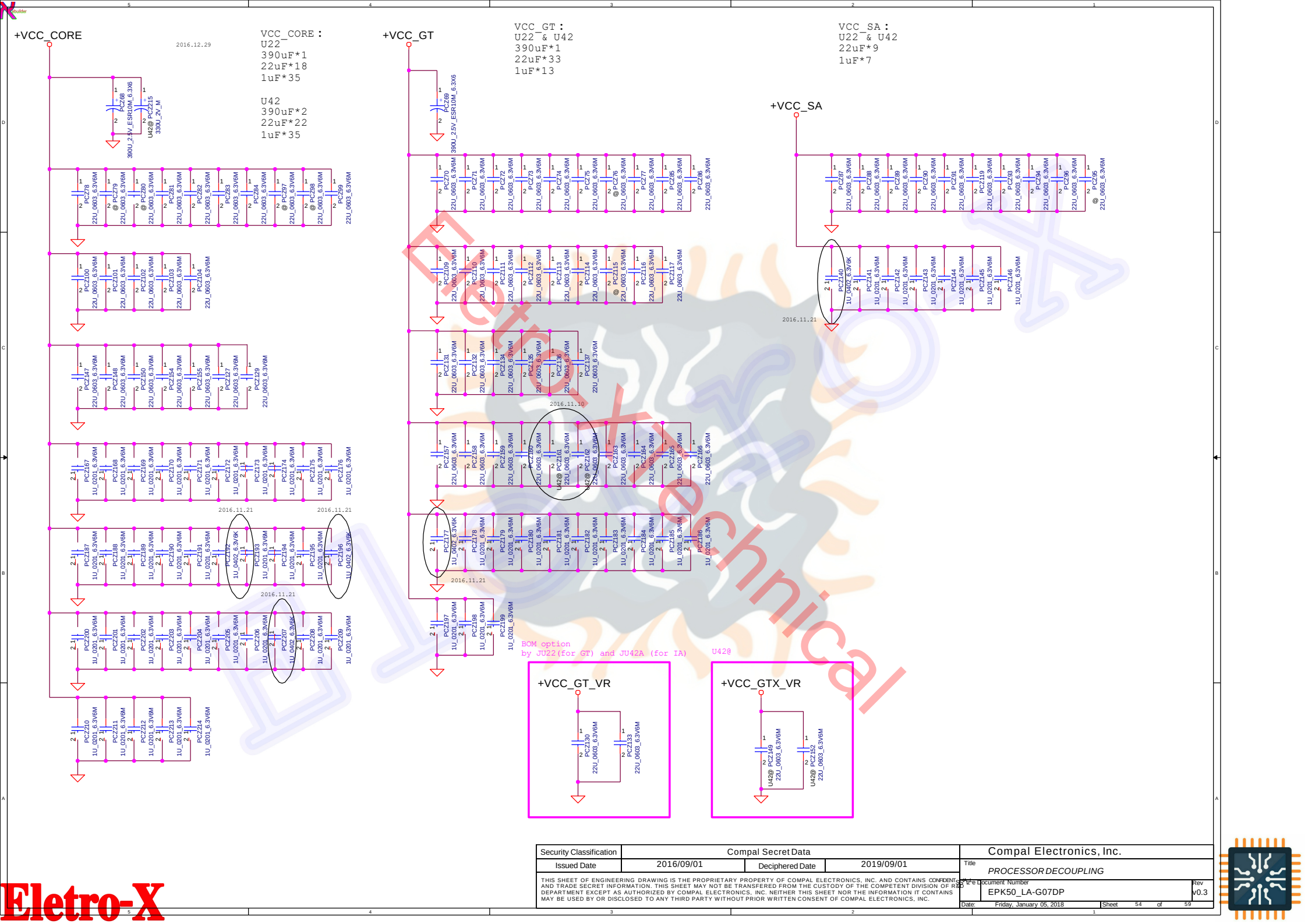
U42
LL=3.1 mohm
TDC=12A
ICCMAX=28A
OCP=39A

VCC_SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

U22
LL=10.3 mohm
TDC=4A
ICCMAX=4.5A
OCP=9.5A

U42
LL=10.3 mohm
TDC=
ICCMAX=5A
OCP=9.5A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01
Title	CPU Power stage		
Size	Document Number		Rev
	EPK50_LA-G07DP		X0.3
Date: Friday, January 05, 2018		Sheet 53 of 59	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Title	PROCESSOR DECOUPLING		
Size	Document Number		Rev
E	EPK50_LA-G07DP		v0.3
Date:	Friday, January 05, 2018	Sheet	54 of 59