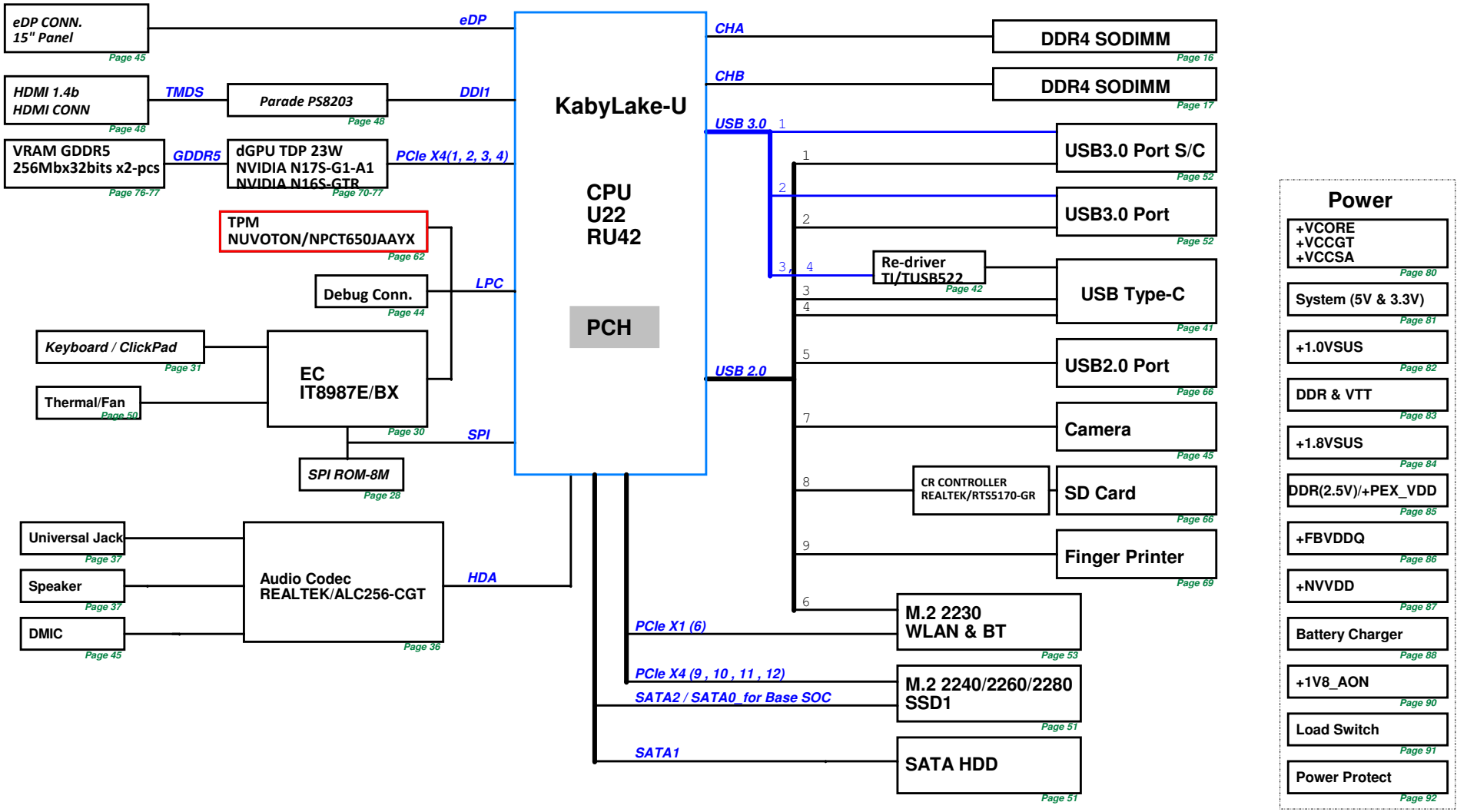
Erdinger Block Diagram



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3G1-HW3 RD

PEGATRON Title : Block Diagram

Engineer: Raly_Hsieh

Size	Project Name	Rev
C	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 1 of 94

Option

Optional	Remark
N/A	Mount
/@	Ummount
/Debug	Debug only
/EMI	Reserved EMI part
/UMA	Support UMA
/VGA	Support VGA
/U22	Support 2+2 CPU
/U42	Support 4+2 CPU
/14inch	Support 14"
/15inch	Support 15"
/TPM	Support TPM function

/Premium_SKU	for Core-I SKU
/BASE_SKU	for Base SOC

PEGATRON Title : Option

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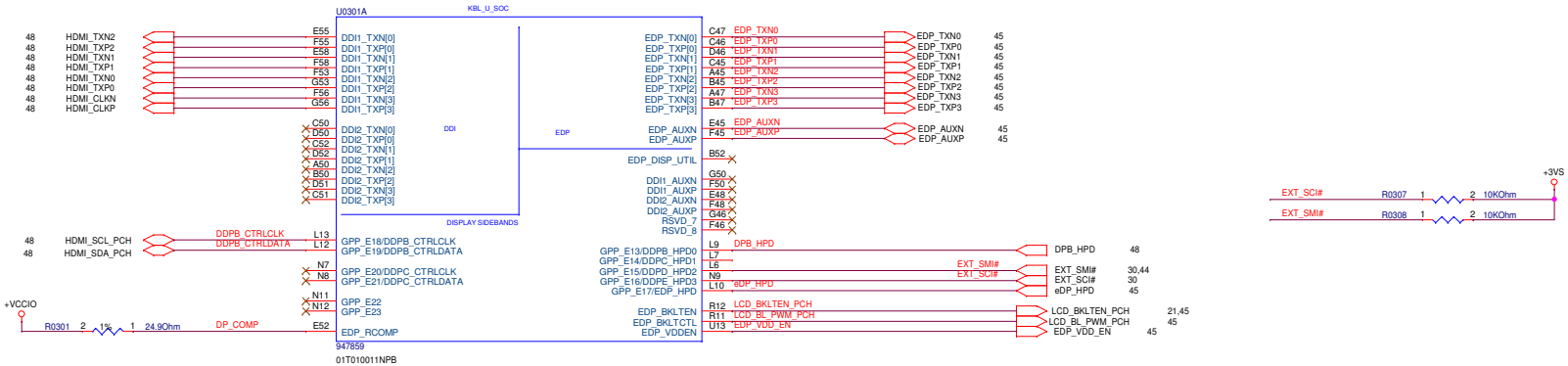
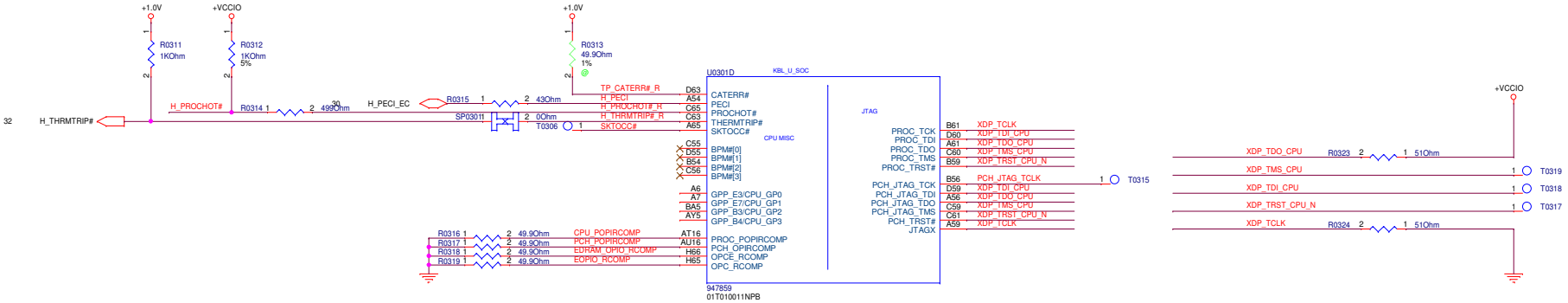
BG1-HW3 RD Engineer: Raly_Hsieh

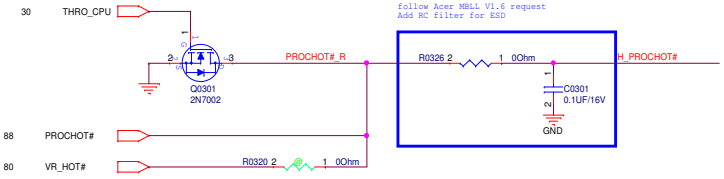
Size	Project Name	Rev
C	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 2 of 94

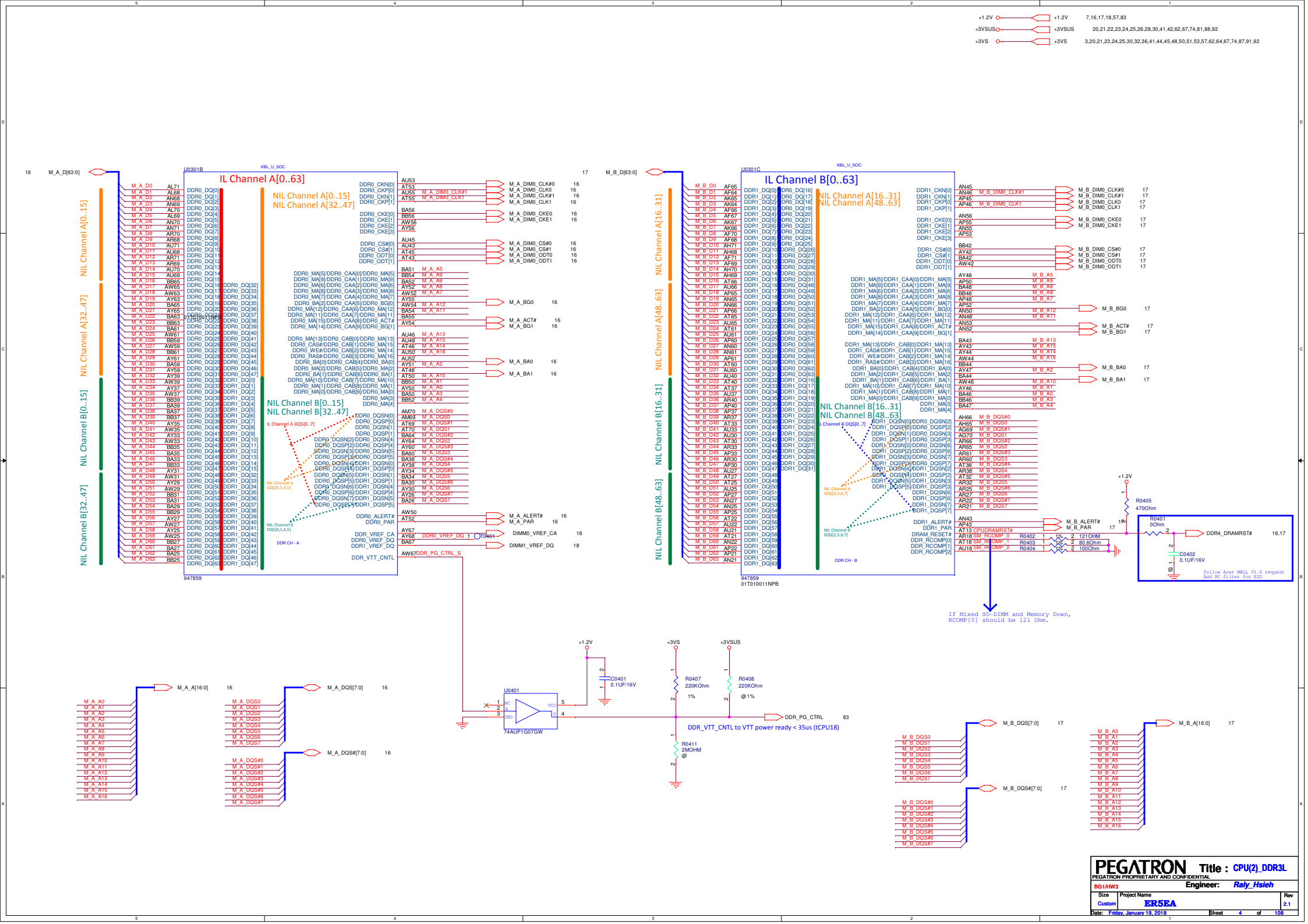
CPU(1)_DDI_eDP







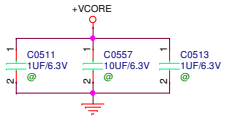
PEGATRON	Title : CPU(1)_DDI_eDP		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
3G1-HW3 RD	Engineer: Raly_Hsieh		
Size: C	Project Name: ER5EA		Rev: 2.1
Date: Friday, January 19, 2018	Sheet 3 of 94		

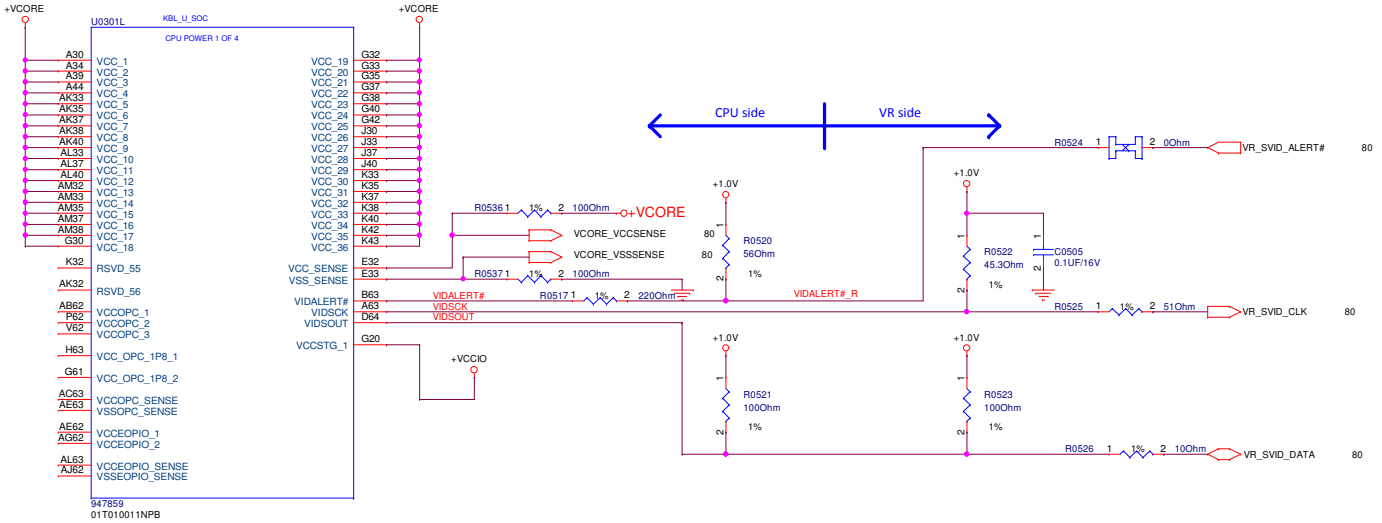

+1.2V +1.2V 7,16,17,18,57,83
+3VSUS +3VSUS 20,21,22,23,24,25,26,28,30,41,42,62,67,74,81,88,92
+3VS +3VS 3,20,21,23,24,25,30,32,36,41,44,45,48,50,51,53,57,62,64,67,74,87,91,92
U0301B
KBL_U_SOC
IL Channel A[0..63]
NIL Channel A[0..15]
NIL Channel A[32..47]
NIL Channel B[0..15]
NIL Channel B[32..47]
947859
U0301C
IL Channel B[0..63]
NIL Channel A[16..31]
NIL Channel A[48..63]
NIL Channel B[16..31]
NIL Channel B[48..63]
947859
01T010011NPB
If Mixed SO-DIMM and Memory Down, RCOMP[0] should be 121 Ohm.
DDR_VTT_CNTL to VTT power ready < 35us (tCPU18)
74AUP1G07GW
follow Acer MBLL V1.6 request Add RC filter for ESD
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : CPU(2)_DDR3L
Engineer: Raly_Hsieh
BG1/HW3
Size Custom
Project Name ER5EA
Rev 2.1
Date: Friday, January 19, 2018
Sheet 4 of 108

05

CPU(3)_+VCCCORE

+VCORE	+VCORE	6,80
+1.0V	+1.0V	3,7,9,25,32,57,91
+VCCIO	+VCCIO	3,7,9,57,91





PEGATRON PROPRIETARY AND CONFIDENTIAL

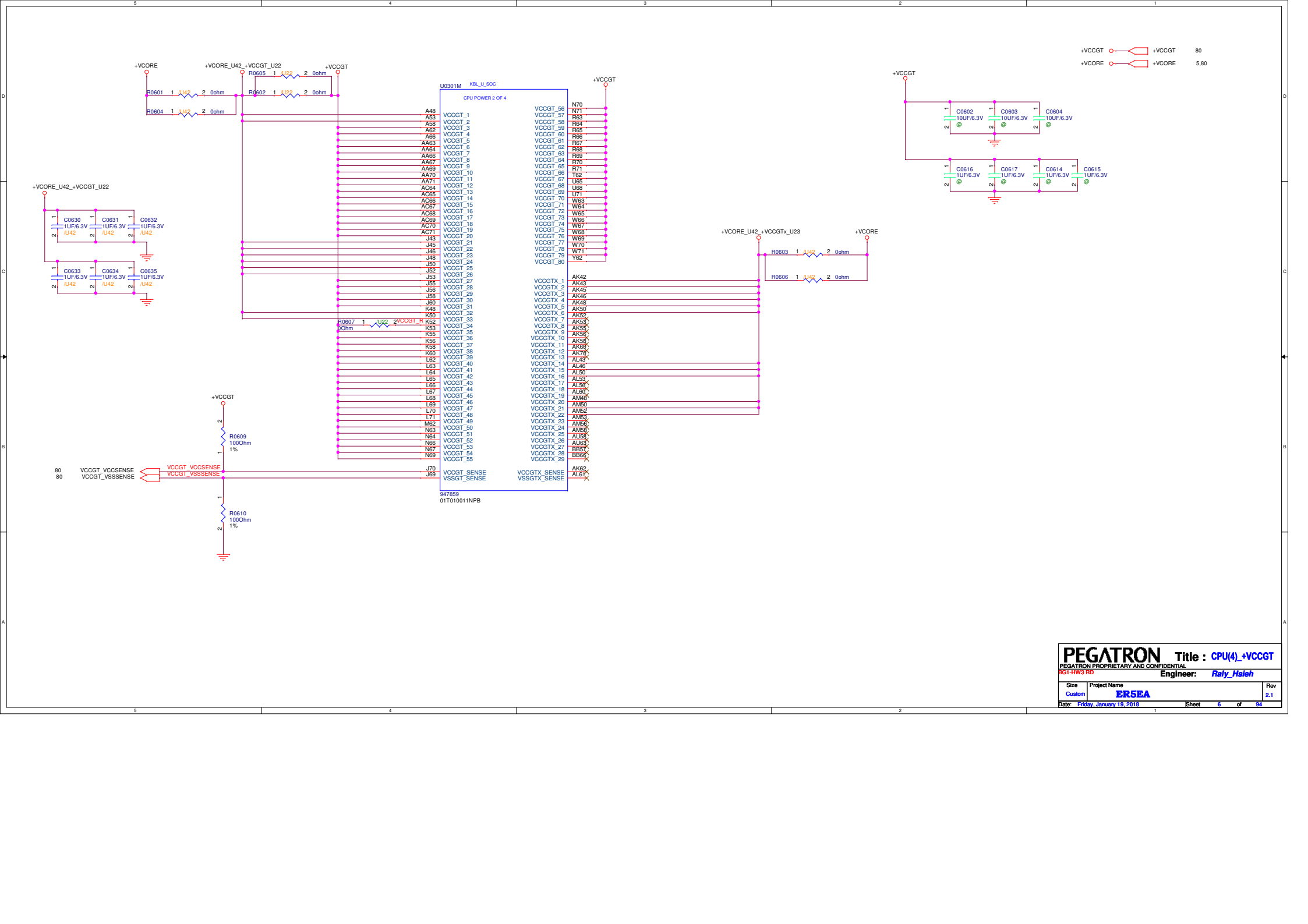
Title : CPU(3)_+VCCCORE

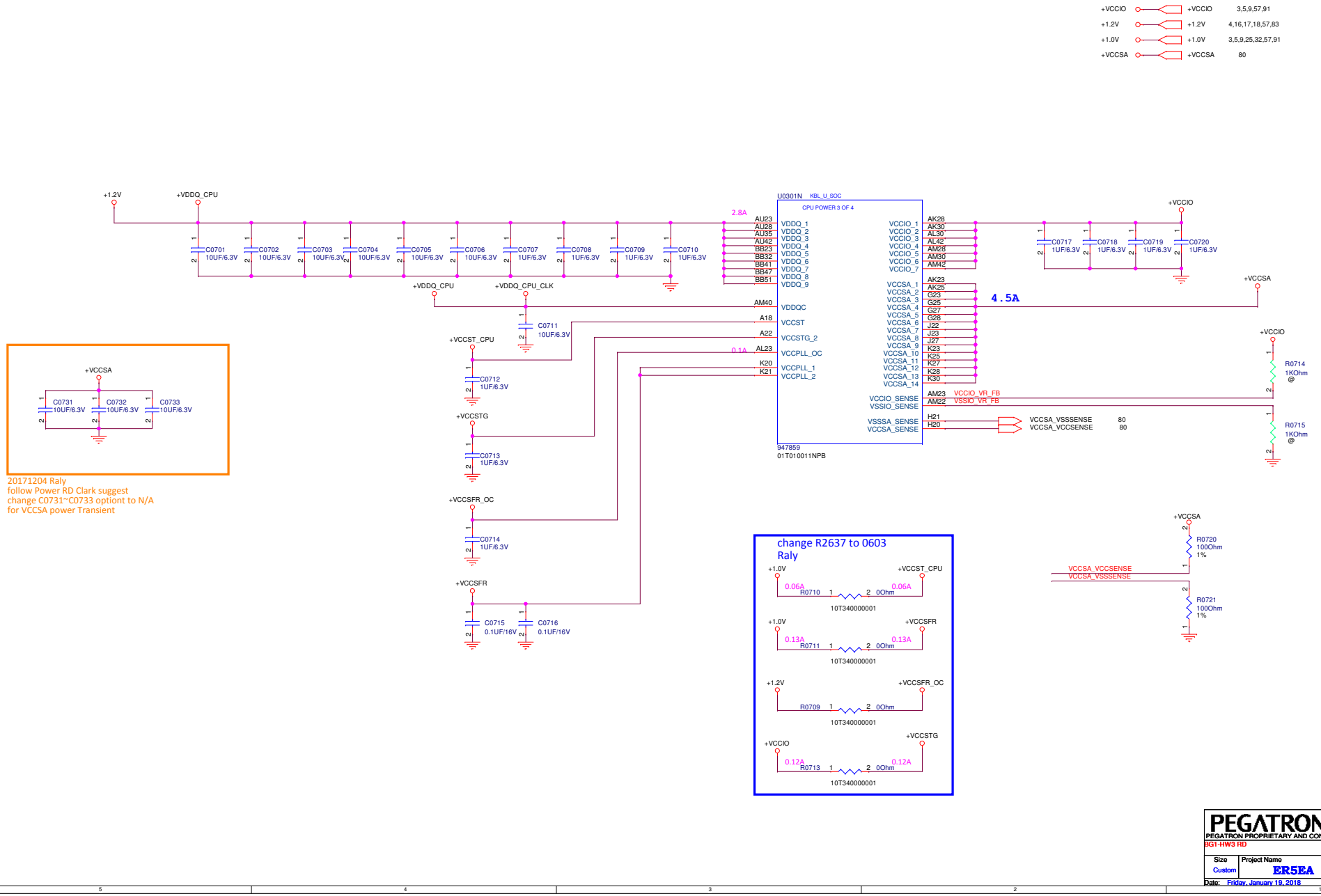
BG1-HW3 RD

Engineer: Raiy_Hsieh

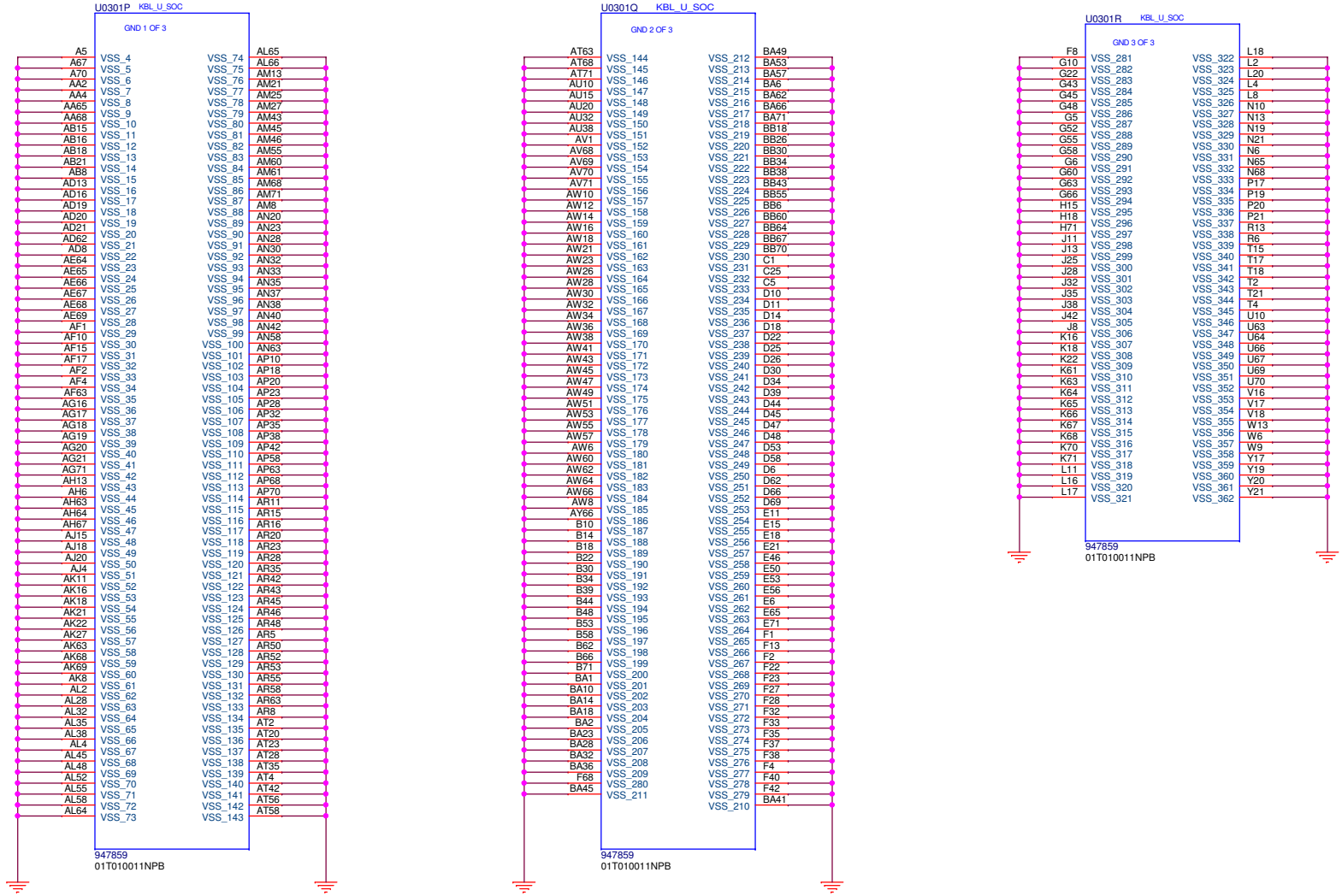
Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 5 of 94


+VCCGT
+VCCGT 80
+VCORE
+VCORE 5,80
+VCORE
+VCORE_U42_+VCCGT_U22
+VCCGT
R0605 1 /U22 2 0ohm
R0601 1 /U42 2 0ohm
R0602 1 /U22 2 0ohm
R0604 1 /U42 2 0ohm
U0301M KBL_U_SOC
CPU POWER 2 OF 4
VCCGT_1 A48
VCCGT_2 A53
VCCGT_3 A58
VCCGT_4 A62
VCCGT_5 A66
VCCGT_6 AA63
VCCGT_7 AA64
VCCGT_8 AA66
VCCGT_9 AA67
VCCGT_10 AA69
VCCGT_11 AA70
VCCGT_12 AA71
VCCGT_13 AC64
VCCGT_14 AC65
VCCGT_15 AC66
VCCGT_16 AC67
VCCGT_17 AC68
VCCGT_18 AC69
VCCGT_19 AC70
VCCGT_20 AC71
VCCGT_21 J43
VCCGT_22 J45
VCCGT_23 J46
VCCGT_24 J48
VCCGT_25 J50
VCCGT_26 J52
VCCGT_27 J53
VCCGT_28 J55
VCCGT_29 J56
VCCGT_30 J58
VCCGT_31 J60
VCCGT_32 K48
VCCGT_33 K50
VCCGT_34 K52
VCCGT_35 K53
VCCGT_36 K55
VCCGT_37 K56
VCCGT_38 K58
VCCGT_39 K60
VCCGT_40 L62
VCCGT_41 L63
VCCGT_42 L64
VCCGT_43 L65
VCCGT_44 L66
VCCGT_45 L67
VCCGT_46 L68
VCCGT_47 L69
VCCGT_48 L70
VCCGT_49 L71
VCCGT_50 M62
VCCGT_51 M63
VCCGT_52 N64
VCCGT_53 N66
VCCGT_54 N67
VCCGT_55 N69
VCCGT_56 N70
VCCGT_57 N71
VCCGT_58 R63
VCCGT_59 R64
VCCGT_60 R65
VCCGT_61 R66
VCCGT_62 R67
VCCGT_63 R68
VCCGT_64 R69
VCCGT_65 R70
VCCGT_66 R71
VCCGT_67 T62
VCCGT_68 U65
VCCGT_69 U68
VCCGT_70 U71
VCCGT_71 W63
VCCGT_72 W64
VCCGT_73 W65
VCCGT_74 W66
VCCGT_75 W67
VCCGT_76 W68
VCCGT_77 W69
VCCGT_78 W70
VCCGT_79 W71
VCCGT_80 Y62
VCCGT_SENSE J70
VSSGT_SENSE J69
VCCGTX_1 AK42
VCCGTX_2 AK43
VCCGTX_3 AK45
VCCGTX_4 AK46
VCCGTX_5 AK48
VCCGTX_6 AK50
VCCGTX_7 AK52
VCCGTX_8 AK53
VCCGTX_9 AK55
VCCGTX_10 AK56
VCCGTX_11 AK58
VCCGTX_12 AK60
VCCGTX_13 AK78
VCCGTX_14 AL43
VCCGTX_15 AL46
VCCGTX_16 AL50
VCCGTX_17 AL53
VCCGTX_18 AL56
VCCGTX_19 AL60
VCCGTX_20 AM48
VCCGTX_21 AM50
VCCGTX_22 AM52
VCCGTX_23 AM53
VCCGTX_24 AM56
VCCGTX_25 AM58
VCCGTX_26 AU58
VCCGTX_27 AU63
VCCGTX_28 BB57
VCCGTX_29 BB62
VCCGTX_SENSE AK62
VSSGTX_SENSE AL61
947859
01T010011NPB
R0607 1 /U22 2 VCCGT_R 0Ohm
+VCORE_U42_+VCCGTx_U23
+VCORE
R0603 1 /U42 2 0ohm
R0606 1 /U42 2 0ohm
+VCORE_U42_+VCCGT_U22
C0630 1UF/6.3V /U42
C0631 1UF/6.3V /U42
C0632 1UF/6.3V /U42
C0633 1UF/6.3V /U42
C0634 1UF/6.3V /U42
C0635 1UF/6.3V /U42
+VCCGT
C0602 10UF/6.3V @
C0603 10UF/6.3V @
C0604 10UF/6.3V @
C0616 1UF/6.3V @
C0617 1UF/6.3V @
C0614 1UF/6.3V @
C0615 1UF/6.3V @
+VCCGT
R0609 100Ohm 1%
80 VCCGT_VCCSENSE
80 VCCGT_VSSSENSE
VCCGT_VCCSENSE
VCCGT_VSSSENSE
R0610 100Ohm 1%
PEGATRON
Title : CPU(4)_+VCCGT
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD
Engineer: Raly_Hsieh
Size Custom
Project Name ER5EA
Rev 2.1
Date: Friday, January 19, 2018
Sheet 6 of 94



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title CPU(5)_+VDDQ/IO/SA
BG1-HW3 RD
Engineer: Raly_Hsieh
Size Custom
Project Name ER5EA
Rev 2.1
Date: Friday, January 19, 2018
Sheet 7 of 94



PEGATRON

Title : CPU(6)_CPU GND

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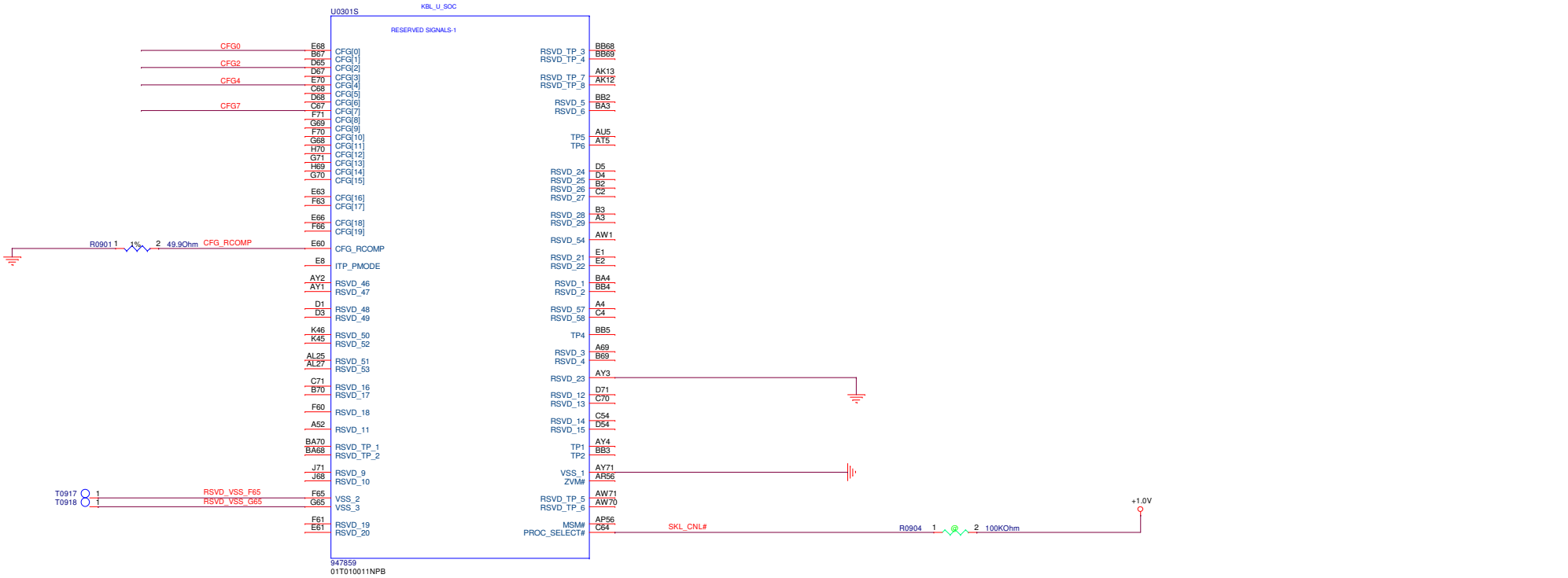
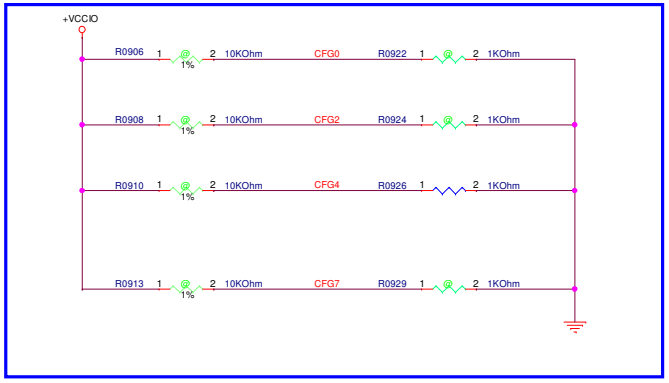
BG1-HW3 RD

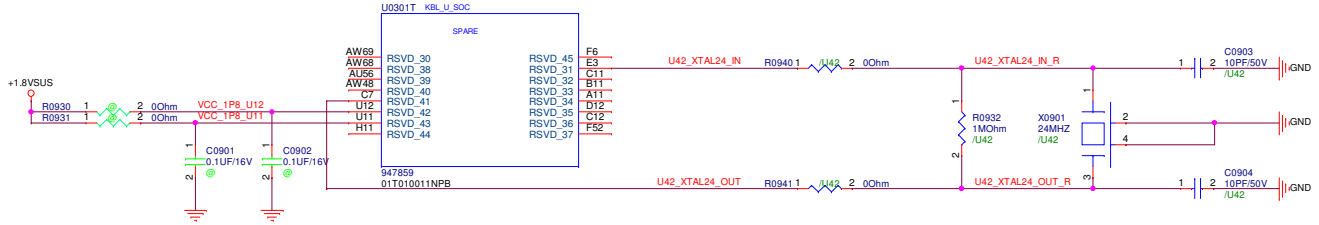
Engineer: Raly_Hsieh

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 8 of 94







PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title :CPU(7)_CFG/RSVD

BG1-HW3 RD

Engineer: Raiy_Hsieh

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 9 of 94

PEGATRON

Title : Block Diagram

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD

Engineer: *Raly_Hsieh*

Size	Project Name	Rev
A	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 10 of 94

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 11 of 94

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 12 of 94

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 13 of 94

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 14 of 94

PEGATRON Title : ****

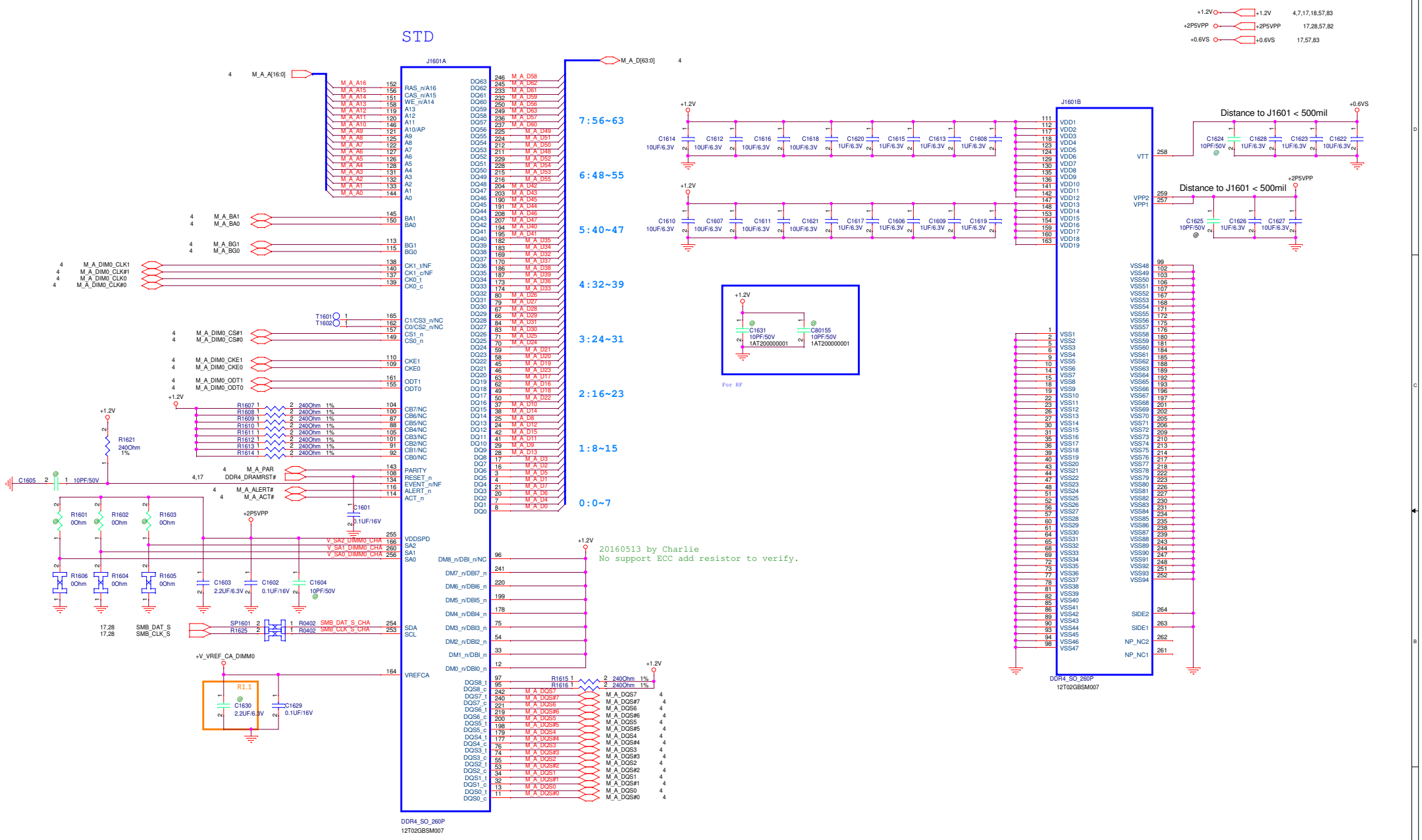
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW1 Engineer: *Raly_Hsieh*

Size	Project Name	Rev
A	**ER5EA**	2.1

Date: Friday, January 19, 2018 Sheet 15 of 103

STD



<Variant Name>

PEGATRON Title :DDR4(1)_SO-DIMM

PEGATRON PROPRIETARY AND CONFIDENTIAL

3G1/HW1

Engineer: Raly_Hsieh

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 16 of 103

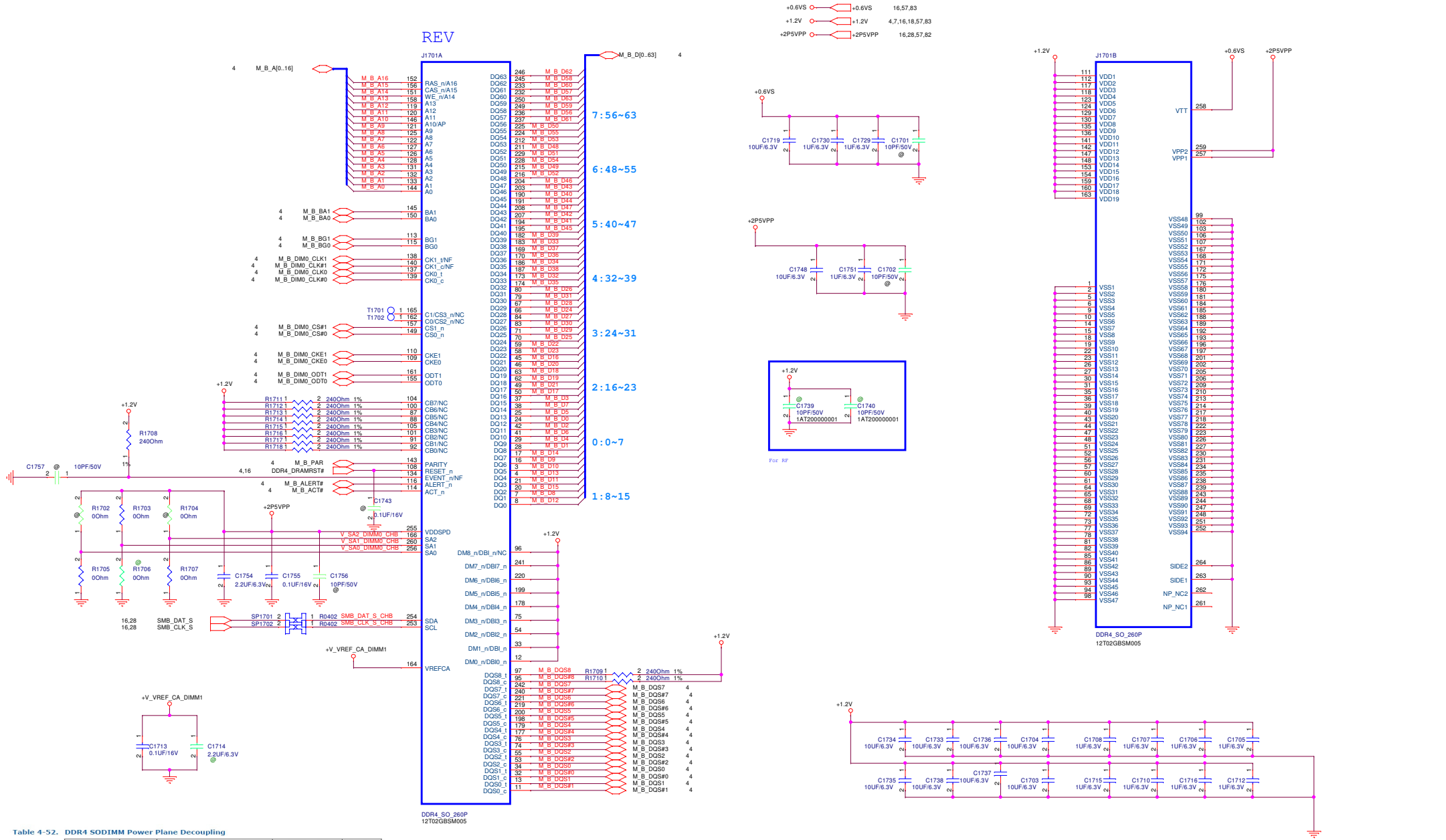


Table 4-52. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0805)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0805)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)	
		Place close to DIMM	1x 2.2µF (0402)	

Notes:
1. Total quantity is referring to 2 channels.

<Variant Name>

PEGATRON
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Title :DDR4(1)_SO-DIMM

BG1/HW3

Engineer: Raly_Hsieh

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 17 of 108

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off

+1.2V — +1.2V — 4,7,16,17,57,83
+V_VREF_CA_DIMM0 — +V_VREF_CA_DIMM0 — 16
+V_VREF_CA_DIMM1 — +V_VREF_CA_DIMM1 — 17

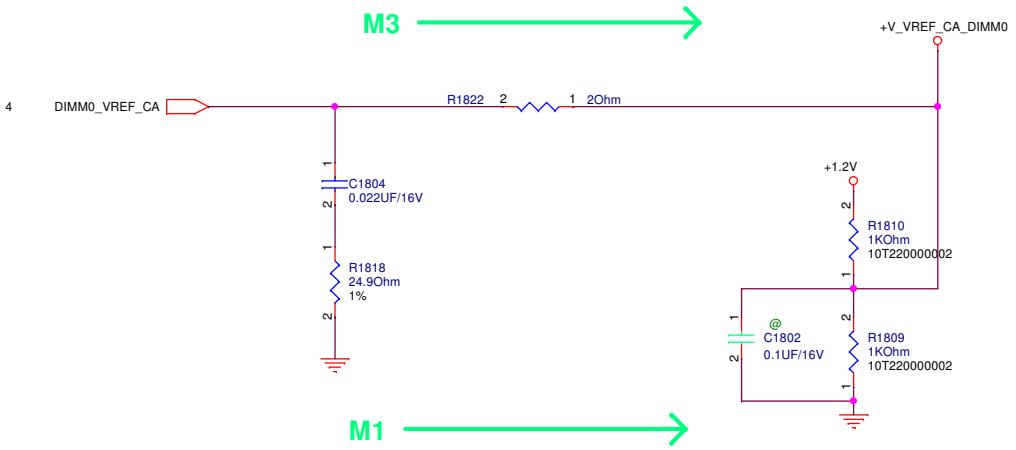
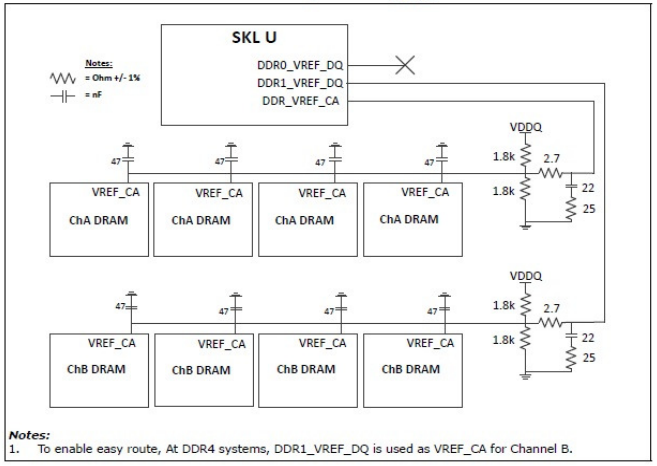


Figure 4-46. SKL U DDR4/-RS x16 Devices Memory Down V_{REF-CA} Overview



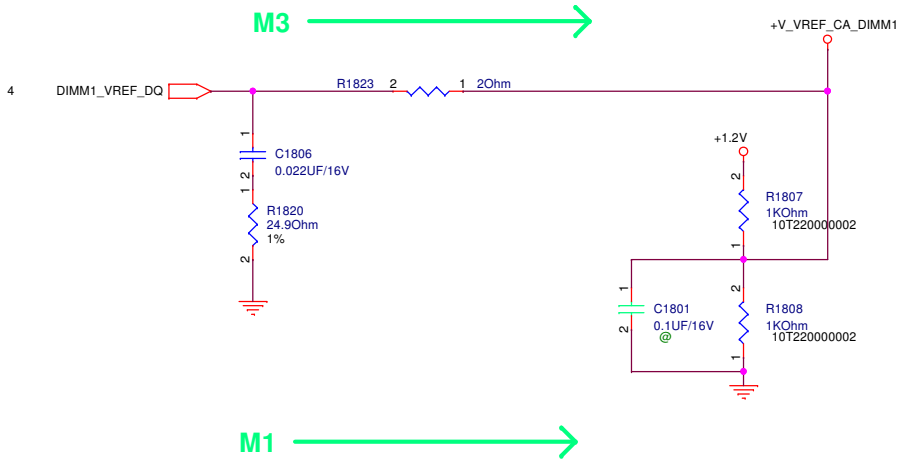
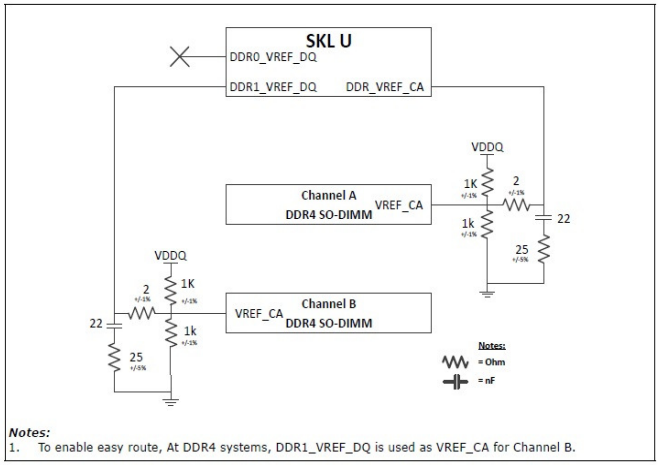


Figure 4-45. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : DDR4(3)_CA/DQ Voltag
Engineer: Raly_Hsieh
BG1/HW3
Size: Custom | Project Name: ER5EA | Rev: 2.1
Date: Friday, January 19, 2018 | Sheet 18 of 108

PEGATRON

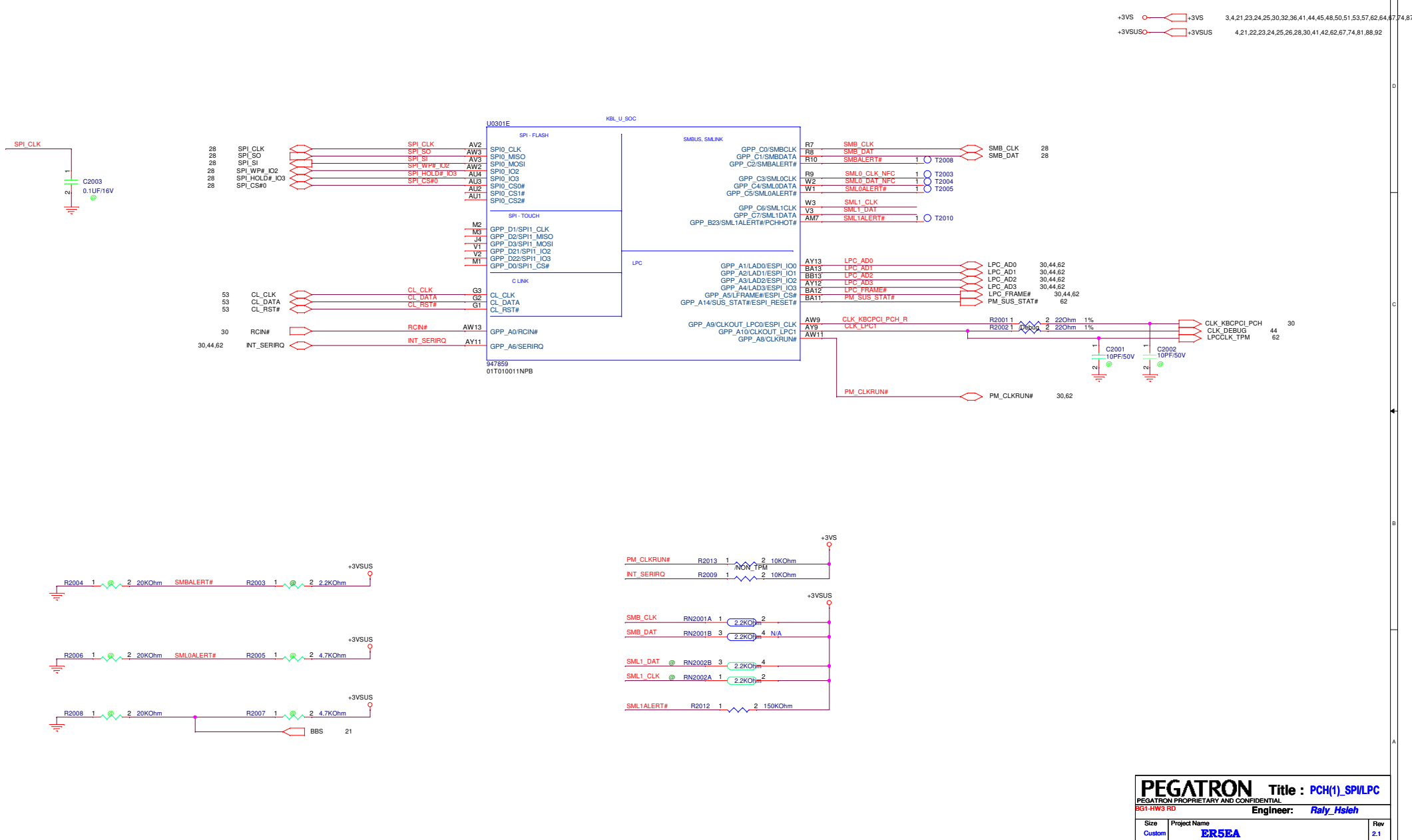
Title : DDR4(3)_CA/DQ Voltage

BG1-HW3 RD

Engineer: *Raly_Hsieh*

Size	Project Name	Rev
B	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 19 of 94



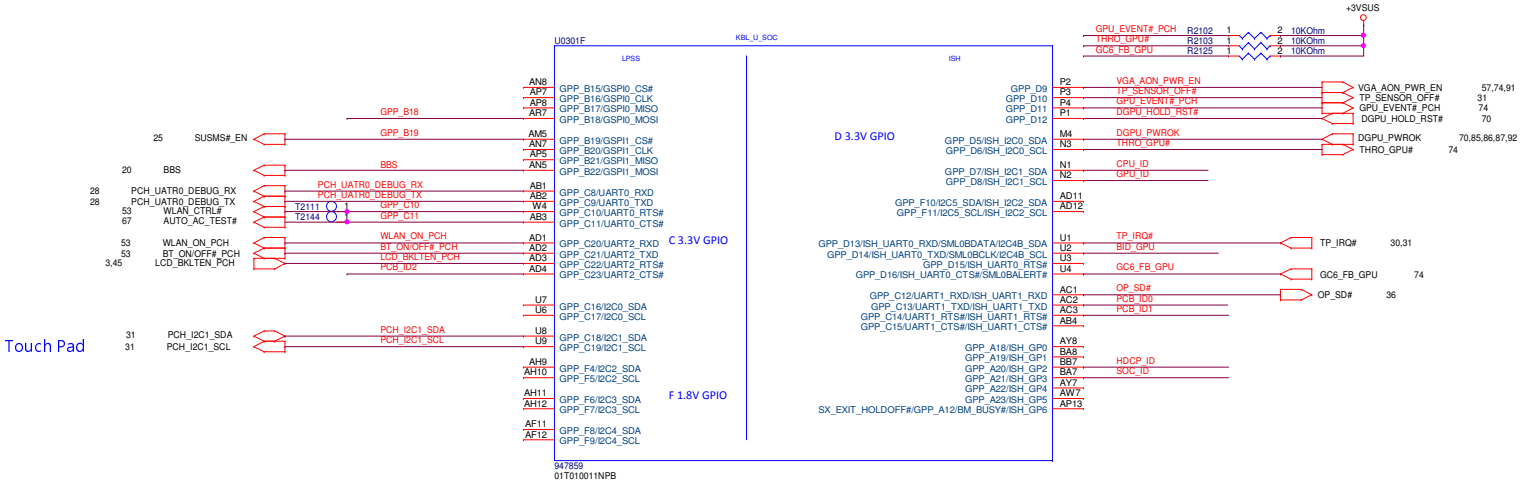
PEGATRON Title : PCH(1)_SPI/LPC

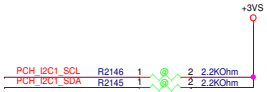
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD Engineer: Raly_Hsieh

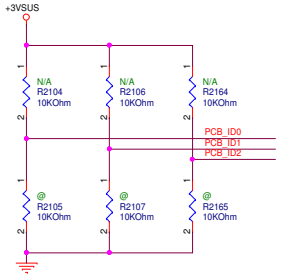
Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 20 of 94



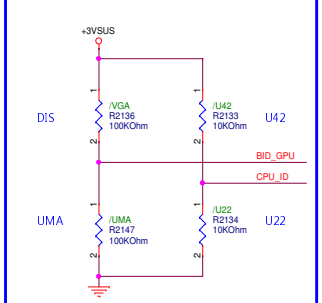


PCB ID



	PCB_ID2 (GPP_C23)	PCB_ID1 (GPP_C14)	PCB_ID0 (GPP_C13)
R10	0	0	0
R11	0	0	1
R20	0	1	0
R21	0	1	1
R22	1	0	0
	1	0	1
	1	1	0

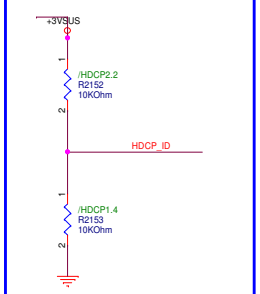
MB BD ID



	CPU_ID1
U22	0
U42	1

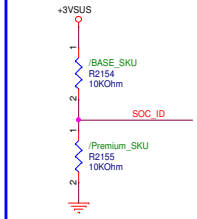
	BID_GPU
UMA	0
DIS	1

HDCP_ID



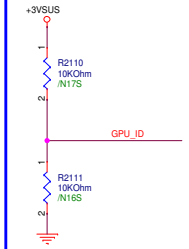
	HDCP_ID
Disable	0
Enable	1

SOC ID

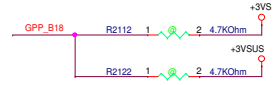


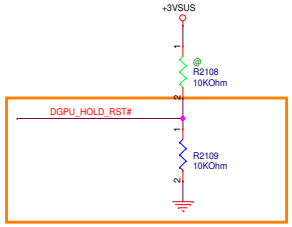
	SOC_ID
BASE	1
Premium	0

GPU ID



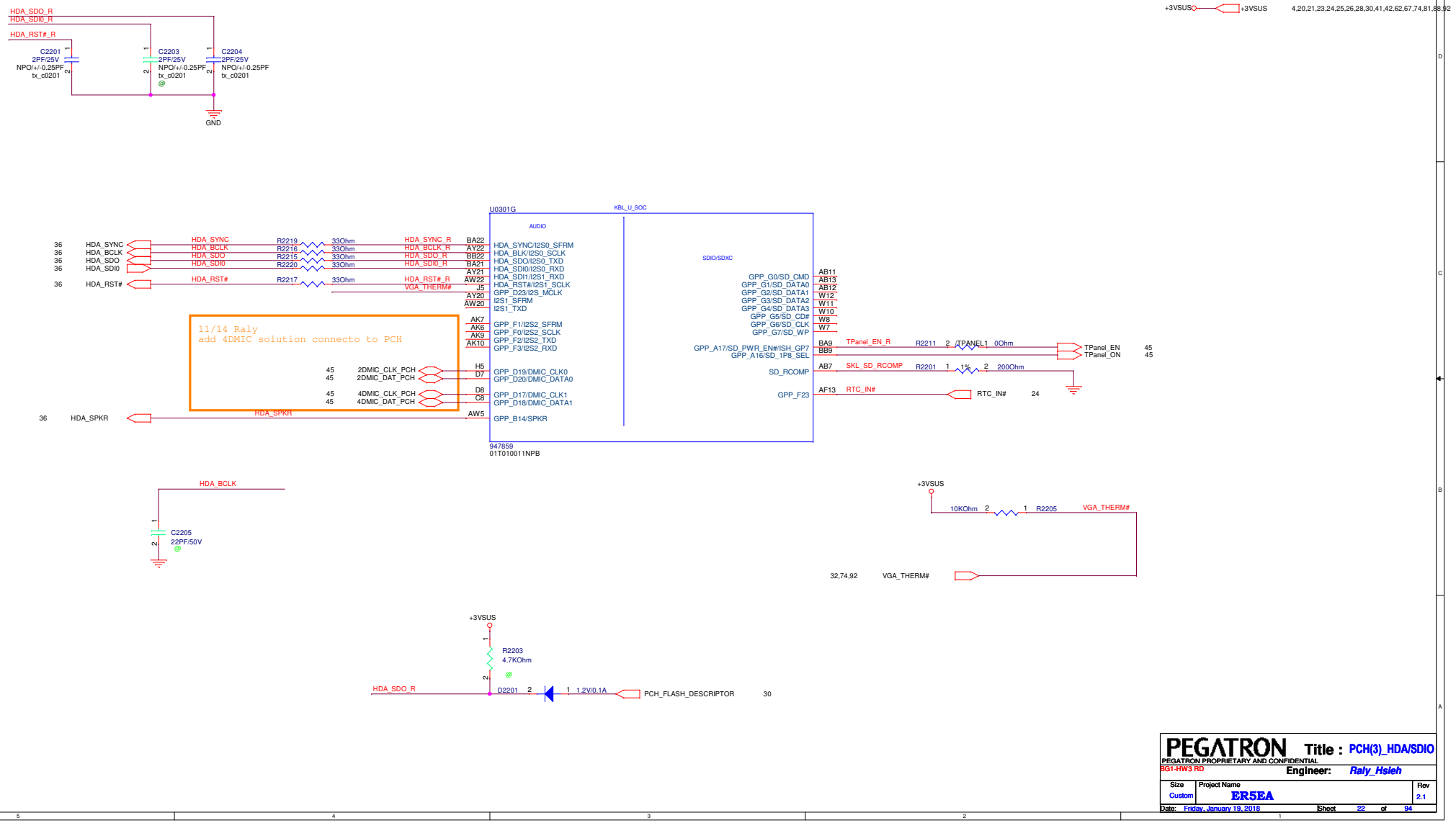
	GPU_ID
N17S	1
N16S	0





20171204 Raly
change R2109 option to N/A

PEGATRON Title : PCH(2)_ISH
PEGATRON PROPRIETARY AND CONFIDENTIAL
3G1-HW3 RD
Engineer: Raly_Hsieh
Size: Custom | Project Name: ER5EA | Rev: 2.1
Date: Friday, January 19, 2018 | Sheet 21 of 94



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD

Title : PCH(3)_HDA/SDIO

Engineer: Raly_Hsieh

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 22 of 94

+3VS → +3VS 3,4,20,21,24,25,30,32,36,41,44,45,48,50,51,53,57,62,64,67,74,87,91,92

+3VSUS → +3VSUS 4,20,21,22,24,25,26,28,30,41,42,62,67,74,81,88,92

U0301H — KBL_U_SOC

PCIE/USB3/SATA

PCIE x 4 -dGPU

70	PCIENB_RXN0				H13	PCIE1_RXN/USB3_5_RXN	
70	PCIENB_RXP0				G13	PCIE1_RXP/USB3_5_RXP	
70	PCIEG_TXN0	/VGAC2304 1	2 0.22UF/10V	PCIEG_TXN0_C	B17	PCIE1_TXN/USB3_5_TXN	
70	PCIEG_TXP0	/VGAC2303 1	2 0.22UF/10V	PCIEG_TXP0_C	A17	PCIE1_TXP/USB3_5_TXP	
70	PCIENB_RXN1				G11	PCIE2_RXN/USB3_6_RXN	
70	PCIENB_RXP1				F11	PCIE2_RXP/USB3_6_RXP	
70	PCIEG_TXN1	/VGAC2310 1	2 0.22UF/10V	PCIEG_TXN1_C	D16	PCIE2_TXN/USB3_6_TXN	
70	PCIEG_TXP1	/VGAC2309 1	2 0.22UF/10V	PCIEG_TXP1_C	C16	PCIE2_TXP/USB3_6_TXP	
70	PCIENB_RXN2				H16	PCIE3_RXN	
70	PCIENB_RXP2				G16	PCIE3_RXP	
70	PCIEG_TXN2	/VGAC2308 1	2 0.22UF/10V	PCIEG_TXN2_C	D17	PCIE3_TXN	
70	PCIEG_TXP2	/VGAC2307 1	2 0.22UF/10V	PCIEG_TXP2_C	C17	PCIE3_TXP	
70	PCIENB_RXN3				G15	PCIE4_RXN	
70	PCIENB_RXP3				F15	PCIE4_RXP	
70	PCIEG_TXN3	/VGAC2306 1	2 0.22UF/10V	PCIEG_TXN3_C	B19	PCIE4_TXN	
70	PCIEG_TXP3	/VGAC2305 1	2 0.22UF/10V	PCIEG_TXP3_C	A19	PCIE4_TXP	
					F16	PCIE5_RXN	
					E16	PCIE5_RXP	
					C19	PCIE5_TXN	
					D19	PCIE5_TXP	

WLAN

53	PCIE_RXN_WLAN				G18	PCIE6_RXN	
53	PCIE_RXP_WLAN				F18	PCIE6_RXP	
53	PCIE_TXN_WLAN	0.1UF/16V 1	2 C2322	PCIE_TXN_WLAN_C	D20	PCIE6_TXN	
53	PCIE_TXP_WLAN	0.1UF/16V 1	2 C2323	PCIE_TXP_WLAN_C	C20	PCIE6_TXP	

M.2 SATA SSD for Base CPU

		SATA_RXN0			F20	PCIE7_RXN/SATA0_RXN	
51	SATA_RXP0	SATA_RXP0			E20	PCIE7_RXP/SATA0_RXP	
51	SATA_TXN0	SATA_TXN0			B21	PCIE7_TXN/SATA0_TXN	
51	SATA_TXP0	SATA_TXP0			A21	PCIE7_TXP/SATA0_TXP	

SATA HDD

		SATA_RXN1			G21	PCIE8_RXN/SATA1A_RXN	
51	SATA_RXP1	SATA_RXP1			F21	PCIE8_RXP/SATA1A_RXP	
51	SATA_TXN1	SATA_TXN1			D21	PCIE8_TXN/SATA1A_TXN	
51	SATA_TXP1	SATA_TXP1			C21	PCIE8_TXP/SATA1A_TXP	

M.2 SATA/PCIE x 4 -SSD

51	PCIE_RXN9				E22	PCIE9_RXN	
51	PCIE_RXP9				E23	PCIE9_RXP	
51	PCIE_TXN9				B23	PCIE9_TXN	
51	PCIE_TXP9				A23	PCIE9_TXP	
51	PCIE_RXN10				F25	PCIE10_RXN	
51	PCIE_RXP10				E25	PCIE10_RXP	
51	PCIE_TXN10				D23	PCIE10_TXN	
51	PCIE_TXP10				C23	PCIE10_TXP	
		R2301 1	1% 2 100Ohm	PCIE_RCOMPN	F5	PCIE_RCOMPN	
				PCIE_RCOMPP	E5	PCIE_RCOMPP	
		T2323 1		PROC_PRDY#	D56	PROC_PRDY#	
		T2324 1		PROC_PREQ#	D61	PROC_PREQ#	
				PIRQA#	BB11	GPP_A7/PIRQA#	
51	PCIE_RXN11				E28	PCIE11_RXN/SATA1B_RXN	
51	PCIE_RXP11				E27	PCIE11_RXP/SATA1B_RXP	
51	PCIE_TXN11				D24	PCIE11_TXN/SATA1B_TXN	
51	PCIE_TXP11				C24	PCIE11_TXP/SATA1B_TXP	
51	PCIE_RXN12				F30	PCIE12_RXN/SATA2_RXN	
51	PCIE_RXP12				A25	PCIE12_RXP/SATA2_RXP	
51	PCIE_TXN12				B25	PCIE12_TXN/SATA2_TXN	
51	PCIE_TXP12					PCIE12_TXP/SATA2_TXP	

947859
01T0100011NPB

SSIC / USB3

USB2

USB3_1_RXN	H8	USB3_RXN1	USB3_RXN1	52	USB3.0 S/C
USB3_1_RXP	G8	USB3_RXP1	USB3_RXP1	52	
USB3_1_TXN	C13	USB3_TXN1	USB3_TXN1	52	
USB3_1_TXP	D13	USB3_TXP1	USB3_TXP1	52	
USB3_2_RXN/SSIC_RXN	J6	USB3_RXN2	USB3_RXN2	52	USB3.0
USB3_2_RXP/SSIC_RXP	H6	USB3_RXP2	USB3_RXP2	52	
USB3_2_TXN/SSIC_TXN	B13	USB3_TXN2	USB3_TXN2	52	
USB3_2_TXP/SSIC_TXP	A13	USB3_TXP2	USB3_TXP2	52	
USB3_3_RXN	J10	USB3_RXN3	USB3_RXN3	42	USB3.0 Type C
USB3_3_RXP	H10	USB3_RXP3	USB3_RXP3	42	
USB3_3_TXN	B15	USB3_TXN3	USB3_TXN3	42	
USB3_3_TXP	A15	USB3_TXP3	USB3_TXP3	42	
USB3_4_RXN	E10	USB3_RXN4	USB3_RXN4	42	USB3.0 Type C
USB3_4_RXP	F10	USB3_RXP4	USB3_RXP4	42	
USB3_4_TXN	C16	USB3_TXN4	USB3_TXN4	42	
USB3_4_TXP	D15	USB3_TXP4	USB3_TXP4	42	
USB2N_1	AB9		USB_PN1_30	52	USB3.0 S&C
USB2P_1	AB10		USB_PP1_30	52	
USB2N_2	AD6		USB_PN2_30	52	USB3.0
USB2P_2	AD7		USB_PP2_30	52	
USB2N_3	AH3		USB_PN3_TYPEC	41	USB3.0 Type C
USB2P_3	AJ3		USB_PP3_TYPEC	41	
USB2N_4	AD9		USB_PN4_TYPEC	41	USB3.0 Type C
USB2P_4	AD10		USB_PP4_TYPEC	41	
USB2N_5	AJ1		USB_PN5_20	64	USB20 (IO BD)
USB2P_5	AJ2		USB_PP5_20	64	
USB2N_6	AF6		USB_PN6_BT	53	Bluetooth
USB2P_6	AF7		USB_PP6_BT	53	
USB2N_7	AH1		USB_PN7_CCD	45	Camera (EDP CONN)
USB2P_7	AH2		USB_PP7_CCD	45	
USB2N_8	AF8		USB_PN8_CR	64	Card reader (IO BD)
USB2P_8	AF9		USB_PP8_CR	64	
USB2N_9	AG1		USB_PN9_FP	69	FingerPrinter
USB2P_9	AG2		USB_PP9_FP	69	
USB2N_10	AH7		USB_PN10_TP	45	Touch
USB2P_10	AH8		USB_PP10_TP	45	
USB2_COMP	AB6	USBCOMP	R2302 1 1% 2 113Ohm		USB2_COMP PDG 1.0 R=113 +-1%
USB2_ID	AG3	USB2_ID_OTG	R2319 1 2 1KOhm		
USB2_VBUSSENSE	AG4	USB2_VBUSSENSE_OTG	R2320 1 2 1KOhm		
	A9	OC0#			USB30 with USB Chager
GPP_E9/USB2_OC0#	C9	OC1#	USB_OC0#_PCH	52	USB30
GPP_E10/USB2_OC1#	D9	OC2#	USB_OC1#_PCH	52	USB20(IO BD)
GPP_E11/USB2_OC2#	B9	OC3#	USB_OC2#_PCH	64	Type C
GPP_E12/USB2_OC3#			USB_OC3#_PCH	41	
{OD}GPP_E4/DEVSLP0	J1	SATA_DEVSLP0	SATA_DEVSLP0	51	SATA SSD1 for Base SKU
{OD}GPP_E5/DEVSLP1	J2	SATA_DEVSLP1	T2326		
{OD}GPP_E6/DEVSLP2	J3	SATA_DEVSLP2	SATA_DEVSLP2	51	SATA SSD1 for Premium SKU
GPP_E0/SATAXPCIE0/SATAGP0	H2				
GPP_E1/SATAXPCIE1/SATAGP1	H3				
GPP_E2/SATAXPCIE2/SATAGP2	G4	SATA_SSD2_PEDET	SATA_SSD2_PEDET	51	
GPP_E8/SATALED#	H1	DMIC_ID			

DMIC ID

+3VSUS
/4MIC R2304 10KOhm
DMIC_ID
/2MIC R2303 10KOhm

	DMIC ID
4 DMIC	1
2 DMIC	0

+3VSUS

OC3#	10KOhm 3	4	RN2301B
OC1#	10KOhm 7	8	RN2301D
OC2#	10KOhm 1	2	RN2301A
OC0#	10KOhm 5	6	RN2301C

+3VS

PIRQA# R2318 1 2 10KOhm

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : PCH(4)_USB/PCIE/SATA

BG1-HW3 RD

Engineer: Raly_Hsieh

Size	Project Name	Rev
C	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 23 of 94

+3VS +3VS 3,4,20,21,23,25,30,32,36,41,44,45,48,50,51,53,57,62,64,67,74,87,91,92
+3VSUS +3VSUS 4,20,21,22,23,25,26,28,30,41,42,62,67,74,81,88,92
+1.8VSUS +1.8VSUS 9,26,84
+3VA +3VA 28,30,31,36,57,67,81,88,93
+VCC_RTC +VCC_RTC 25,26,60

U0301I KBL_U_SOC
CSI-2
A36 CSI2_DN0 / B36 CSI2_DP0 / C38 CSI2_DN1 / D38 CSI2_DP1 / C36 CSI2_DN2 / D36 CSI2_DP2 / A38 CSI2_DN3 / B38 CSI2_DP3
C31 CSI2_DN4 / D31 CSI2_DP4 / C33 CSI2_DN5 / D33 CSI2_DP5 / A31 CSI2_DN6 / B31 CSI2_DP6 / A33 CSI2_DN7 / B33 CSI2_DP7
A29 CSI2_DN8 / B29 CSI2_DP8 / C28 CSI2_DN9 / D28 CSI2_DP9 / A27 CSI2_DN10 / B27 CSI2_DP10 / C27 CSI2_DN11 / D27 CSI2_DP11
CSI2_CLKN0 C37 / CSI2_CLKP0 D37 / CSI2_CLKN1 C32 / CSI2_CLKP1 D32 / CSI2_CLKN2 C29 / CSI2_CLKP2 D29 / CSI2_CLKN3 B26 / CSI2_CLKP3 A26
CSI2_COMP E13 / GPP_D4/FLASHTRIG B7
EMMC
GPP_F13/EMMC_DATA0 AP2 / GPP_F14/EMMC_DATA1 AP1 / GPP_F15/EMMC_DATA2 AP3 / GPP_F16/EMMC_DATA3 AN3 / GPP_F17/EMMC_DATA4 AN1 / GPP_F18/EMMC_DATA5 AN2 / GPP_F19/EMMC_DATA6 AM4 / GPP_F20/EMMC_DATA7 AM1
GPP_F21/EMMC_RCLK AM2 / GPP_F22/EMMC_CLK AM3 / GPP_F12/EMMC_CMD AP4
EMMC_RCOMP AT1
947859
01T010011NPB

CSI2_COMP 100Ohm 1 2 R2418
EMMC_RCOMP
R2419 200Ohm
RES 200 OHM 1/16W (0402) 1%

11/14 Raly
change GPP_D4 to GPU_OVERT#
+3VSUS
R2204 10KOhm
GPU_OVERT# GPU_OVERT# 74

+1.8VSUS
R2412 100KOhm 1%
RTC_IN# 22
+RTCBAT
Q2401B UM6K1NG31DTN
R2409 10MOhm
+3VA
R2425 0Ohm
R2423 1.5KOhm 1%
+RTC_AC
R2424 45.3KOhm 1%
+VCC_RTC
R2420 1KOhm
D2401 RB751V-40 0.37V/30mA
D2402 RB751V-40 0.37V/30mA
+RTC_BAT
R2405 1 2 1KOhm
C2407 1UF/6.3V
CON2401
SIDE2 4 / 2 2 / 1 1 / SIDE1 3
WtoB_CON_2P
1217-0105000

947859
01T010011NPB
U0301J KBL_U_SOC
CLOCK SIGNALS
D42 CLKOUT_PCIE_N0 / C42 CLKOUT_PCIE_P0 / AR10 GPP_B5/SRCCLKREQ0#
B42 CLKOUT_PCIE_N1 / A42 CLKOUT_PCIE_P1 / AT7 GPP_B6/SRCCLKREQ1#
D41 CLKOUT_PCIE_N2 / C41 CLKOUT_PCIE_P2 / AT8 GPP_B7/SRCCLKREQ2#
D40 CLKOUT_PCIE_N3 / C40 CLKOUT_PCIE_P3 / AT10 GPP_B8/SRCCLKREQ3#
B40 CLKOUT_PCIE_N4 / A40 CLKOUT_PCIE_P4 / AU8 GPP_B9/SRCCLKREQ4#
E40 CLKOUT_PCIE_N5 / E38 CLKOUT_PCIE_P5 / AU7 GPP_B10/SRCCLKREQ5#
CLKOUT_ITPXDP_N F43 / CLKOUT_ITPXDP_P E43
GPD8/SUSCLK BA17 SUSCLK_PCH 1 T2418
XTAL24_IN E37 XTAL_24M_IN / XTAL24_OUT E35 XTAL_24M_OUT
XCLK_BIASREF E42 XCLK_BIASREF R2417 1 0.5% 2 2.71Kohm +VCCF24NS_1P0
RTCX1 AM18 XTAL_32K_X1 / RTCX2 AM20 XTAL_32K_X2
SRTCRST# AN18 SRTC_RST# / RTCRST# AM16 RTC_RST#

51 CLK_PCIE_SSD1#_PCH SP2405 1 2 CLK_PCIE_SSD1#_PCH_R
51 CLK_PCIE_SSD1_PCH SP2406 1 2 CLK_PCIE_SSD1_PCH_R
51 CLK_REQ1_SSD1# SP2407 1 2 CLK_REQ1_SSD1#_R
70 CLK_PCIE_PEG#_PCH SP2415 1 2 CLK_PCIE_PEG#_PCH_R
70 CLK_PCIE_PEG_PCH SP2416 1 2 CLK_PCIE_PEG_PCH_R
70 CLK_REQ3_PEG# SP2417 1 2 CLK_REQ3_PEG#_R
53 CLK_PCIE_WLAN#_PCH SP2412 1 2 CLK_PCIE_WLAN#_PCH_R
53 CLK_PCIE_WLAN_PCH SP2413 1 2 CLK_PCIE_WLAN_PCH_R
53 CLK_REQ4_WLAN# SP2414 1 2 CLK_REQ4_WLAN#_R

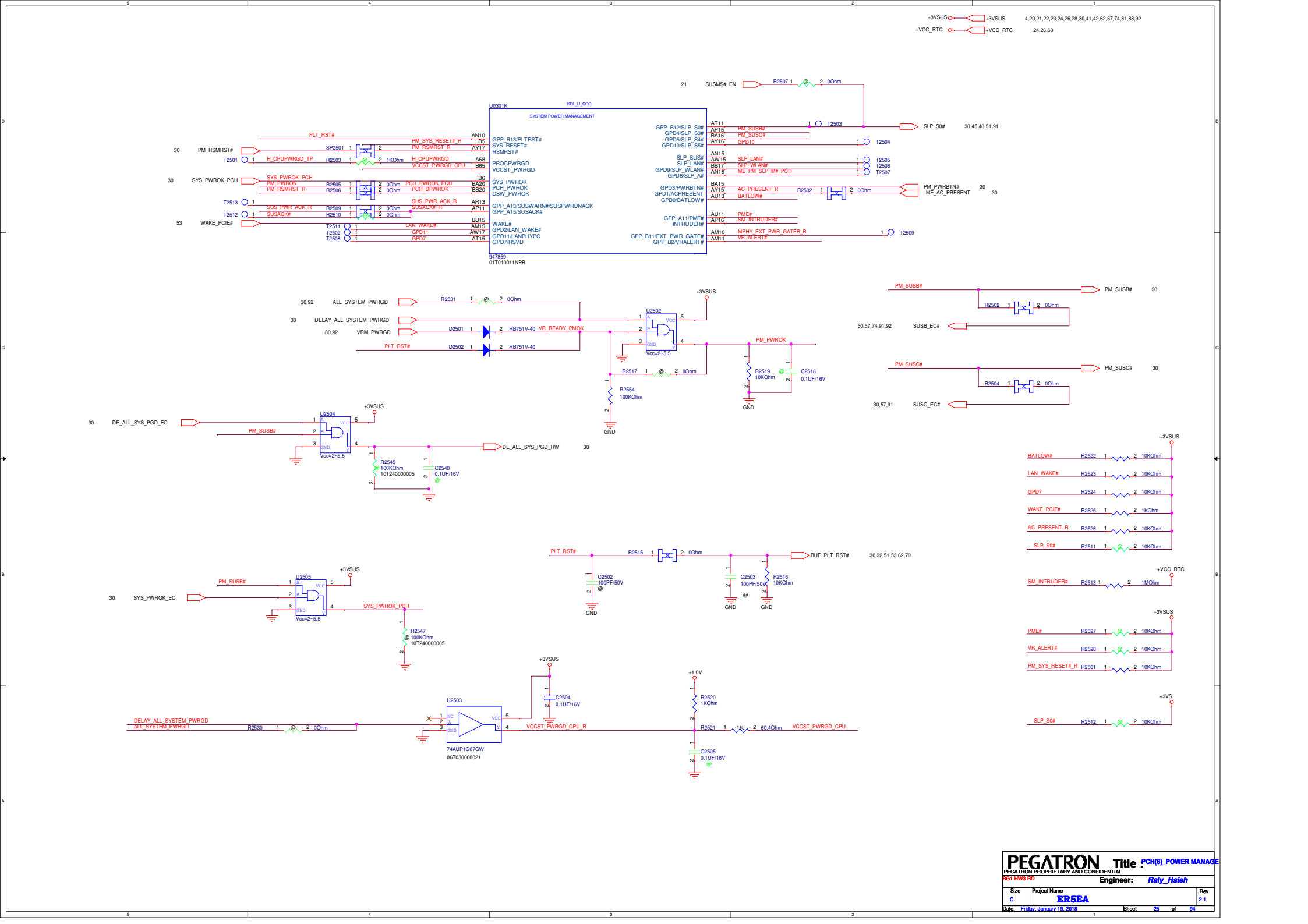
+VCC_RTC
R2403 1 2 20KOhm
JRST2402 SGL_JUMP
C2405 1UF/6.3V
R2404 1 2 20KOhm
JRST2401 SGL_JUMP
C2406 1UF/6.3V
30 SW_RTCRST
Q2401A UM6K1NG31DTN
R2407 10KOhm

CLK_REQ4_WLAN#_R R2429 10KOhm +3VSUS / R2408 10KOhm +3VS / R2411 10KOhm
CLK_REQ3_PEG#_R R2421 10KOhm +3VSUS / R2410 10KOhm +3VS / R2413 10KOhm
CLK_REQ1_SSD1#_R R2430 10KOhm +3VS / R2431 10KOhm

XTAL_24M_IN R2432 /U22 0Ohm
XTAL_24M_OUT R2433 /U22 0Ohm
R2401 /U22 1MOhm
XTAL_24M_OUT_R
XTAL_24M_IN_R
X2401 24MHZ /U22
C2402 10PF/50V /U22
C2401 10PF/50V /U22

XTAL_32K_X1
XTAL_32K_X2
R2402 10MOhm
X2402 32.768KHZ 07T080000075 +/-20ppm/9PF
C2404 7PF/50V
C2403 7PF/50V

PEGATRON Title PCH(5)_CLK
PEGATRON PROPRIETARY AND CONFIDENTIAL
3G1-HW3 RD Engineer: Raly_Hsieh
Size C | Project Name ER5EA | Rev 2.1
Date: Friday, January 19, 2018 | Sheet 24 of 94



PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : PCH(6)_POWER MANAGE

BG1-HW3 RD

Engineer: Raly_Hsieh

Size	Project Name	Rev
C	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 25 of 94

+1.0VSUS → +1.0VSUS 82
+3VSUS → +3VSUS 4,20,21,22,23,24,25,28,30,41,42,62,67,74,81,88,92
+1.8VSUS → +1.8VSUS 9,24,84

Del R2640
change R2640 to 0603
Raly

+1.0VSUS 4A → +VCCMPHYGTAON_1P0_LS_SIP 2A → +VCCSRAM_1P0
R2637 1 2 0Ohm 0.642A → +VCCAMPHYPLL_1P0
10T340000001
R2638 1 2 0Ohm 0.088A → +VCCAPLLEBB_1P0
R2639 1 2 0Ohm 0.033A
C2628 0.1UF/16V

+1.0VSUS_ORG
C2601 1UF/6.3V tx_c0402 near AB19
+VCCPRIM_CORE
C2602 1UF/6.3V tx_c0402 near AF18
+1.0VSUS_ORG
C2603 1UF/6.3V tx_c0402 near K17
+VCCDSW_1P0 C2604 1 2 1UF/6.3V near AL1
+VCCMPHYGTAON_1P0_LS_SIP 2A
C2605 47UF/6.3V @ near N15
C2606 1UF/6.3V near N15
+VCCAMPHYPLL_1P0
C2607 1UF/6.3V near K15
C2650 47UF/6.3V @
+1.0VSUS_ORG
R2648 1 2 0Ohm
+VCCAPLL_1P0_SOC
C2644 2 0.1UF/16V
+VCCPDSW_3P3
+3VSUS_ORG
+VCCSRAM_1P0
C2610 1 2 1UF/6.3V vx_c0402_small near AF20
+3VSUS_ORG
C2611 1UF/6.3V vx_c0402_small near V19
+VCCAPLLEBB_1P0
+1.0VSUS_ORG
R2649 1 2 0Ohm
C2645 2 0.1UF/16V
C2612 1UF/6.3V near N18

947859
KBL 0.5 0.1T010011NPB
U0301O
CPU POWER 4 OF 4

0.696A	AB19	VCCPRIM_1P0_5
	AB20	VCCPRIM_1P0_6
	P18	VCCPRIM_1P0_7
2.574A	AF18	VCCPRIM_CORE_1
	AF19	VCCPRIM_CORE_2
	V20	VCCPRIM_CORE_3
	V21	VCCPRIM_CORE_4
	AL1	DCPDSW_1P0
0.022A	K17	VCCMPHYAON_1P0_1
	L1	VCCMPHYAON_1P0_2
	N15	VCCMPHYGT_1P0_1
	N16	VCCMPHYGT_1P0_2
	N17	VCCMPHYGT_1P0_3
	P15	VCCMPHYGT_1P0_4
	P16	VCCMPHYGT_1P0_5
0.088A	K15	VCCAMPHYPLL_1P0_1
	L15	VCCAMPHYPLL_1P0_2
0.026A	V15	VCCAPLL_1P0
0.696A	AB17	VCCPRIM_1P0_2
	Y18	VCCPRIM_1P0_3
0.118A	AD17	VCCDSW_3P3_1
	AD18	VCCDSW_3P3_2
	AJ17	VCCDSW_3P3_3
0.068A	AJ19	VCCHDA
0.011A	AJ16	VCCSPI
0.642A	AF20	VCCSRAM_1P0_1
	AF21	VCCSRAM_1P0_2
	T19	VCCSRAM_1P0_3
	T20	VCCSRAM_1P0_4
0.075A	AJ21	VCCPRIM_3P3_1
0.696A	AK20	VCCPRIM_1P0_4
0.033A	N18	VCCAPLLEBB_1P0

VCCPGPPA	AK15	0.02A
VCCPGPPB	AG15	0.004A
VCCPGPPC	Y16	0.006A
VCCPGPPD	Y15	0.008A
VCCPGPPE	T16	0.006A
VCCPGPPF	AF16	0.161A
VCCPGPPG	AD15	0.0041A
VCCPRIM_3P3_2	V19	0.075A
VCCPRIM_1P0_1	T1	0.696A
VCCATS_1P8	AA1	0.006A
VCCRTCPRIM_3P3	AK17	0.001A
VCCRTC_1	AK19	
VCCRTC_2	BB14	0.001A
DCPRTC	BB10	VCCRTCEXT
VCCCLK1	A14	0.035A
VCCCLK2	K19	0.029A
VCCCLK3	L21	0.024A
VCCCLK4	N20	0.033A
VCCCLK5	L19	0.004A
VCCCLK6	A10	0.0039A
GPP_B0/CORE_VID0	AN11	
GPP_B1/CORE_VID1	AN13	

C2634 1 2 0.1UF/16V near AK19 GND
C2620 1 2 0.1UF/16V near BB10 GND
C2619 1 2 1UF/6.3V near AK19 GND
R2646 1KOhm
R2647 1KOhm

+3VSUS_ORG
vx_c0402_small
C2635 1 2 1UF/6.3V near AG15
C2613 1 2 1UF/6.3V near Y16
C2614 1 2 1UF/6.3V near T16
+1.8VSUS_ORG
C2646 1UF/6.3V near AD15
+1.0VSUS_ORG
+V1.8A_SIP
R2624 1 2 0Ohm
+1.8VSUS_ORG
C2615 1UF/6.3V near AA1
+3VSUS_ORG
C2625 0.1UF/16V near AK17
C2618 1UF/6.3V near AK17
+VCC_RTC
C2624 1UF/6.3V near A10

+VCC19P2_1P0 → +1.0VSUS_ORG
+VCCF100_1P0 → +1.0VSUS_ORG
C2649 47UF/6.3V @
+VCCF135_1P0 → +1.0VSUS_ORG
+VCCF100OC_1P0 → +1.0VSUS_ORG
C2647 47UF/6.3V @
+VCCF24NS_1P0 → +1.0VSUS_ORG
C2648 47UF/6.3V @
+VCC24TBT_1P0 → +1.0VSUS_ORG

+1.0VSUS
R2604 1 2 0Ohm → +VCCAPLL_1P0
C2608 47UF/6.3V @
C2636 0.1UF/16V
B2601 2 1 75OHM → +VCCAPLL_1P0_SOC
C2640 2PF/25V NPO/+/-0.25PF
C2641 2PF/25V NPO/+/-0.25PF near V15
GND

+3VSUS
R2602 1 2 0Ohm → +VCCPAZIO
C2609 1UF/10V @
C2637 0.1UF/16V
B2602 2 1 75OHM → +VCCPAZIO_SOC
C2642 2PF/25V NPO/+/-0.25PF
C2643 2PF/25V NPO/+/-0.25PF near AJ19
GND

change R2603 to 0603
Raly

+3VSUS
R2601 1 2 0Ohm 0.5A → +3VSUS_ORG
+1.0VSUS
R2603 1 2 0Ohm 1A → +1.0VSUS_ORG
10T340000001
+1.8VSUS
R2605 1 2 0Ohm 0.5A → +1.8VSUS_ORG

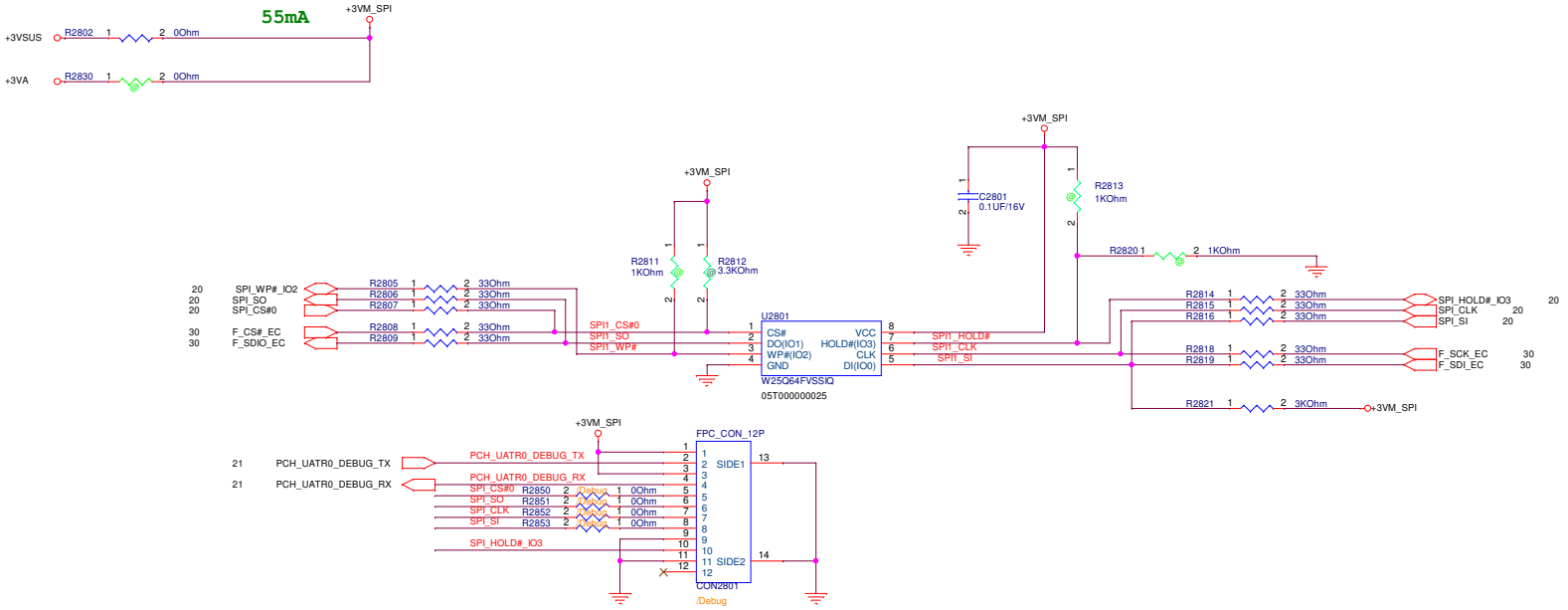
+3VSUS
Q2601 PJA3411 → +VCCPDSW_3P3
Q2603
Q2602 PMBT3906
R2635 1MOhm
R74109 5.1KOhm
R2634 1MOhm

PEGATRON Title PCH(7)_POWER
PEGATRON PROPRIETARY AND CONFIDENTIAL
3G1-HW3 RD
Engineer: Raly_Hsieh

Size	Project Name	Rev
C	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 26 of 94

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 27 of 94

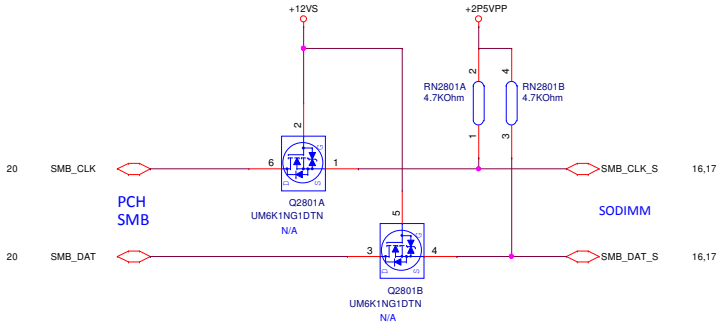


PCH SMBus

EC

GPU

PCH



PEGATRON Title : PCH(9)_SPI_SMB

PEGATRON PROPRIETARY AND CONFIDENTIAL

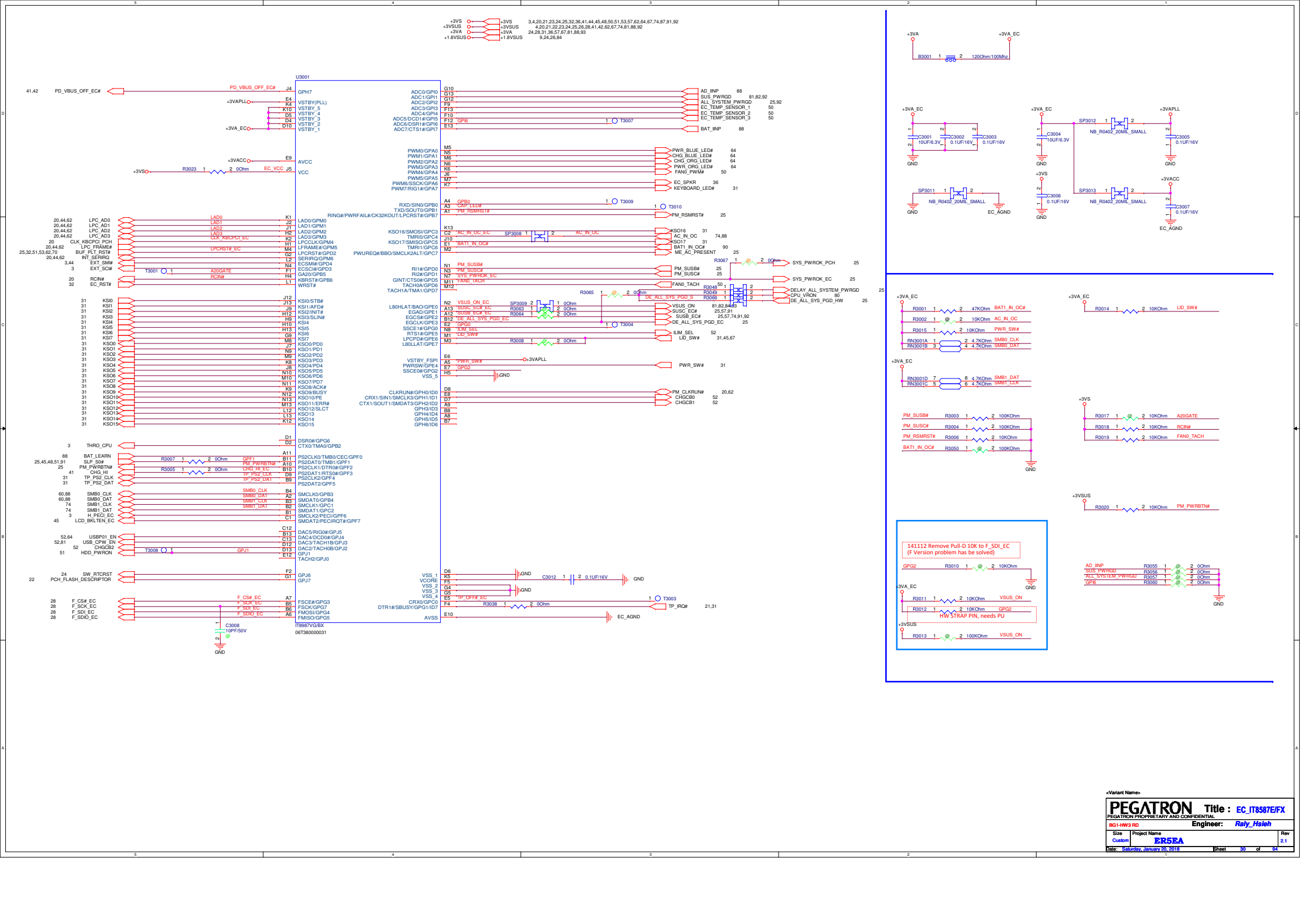
BG1-HW3 RD

Engineer: Raly_Hsieh

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 28 of 94

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 29 of 94



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PEGATRON PROPRIETARY AND CONFIDENTIAL

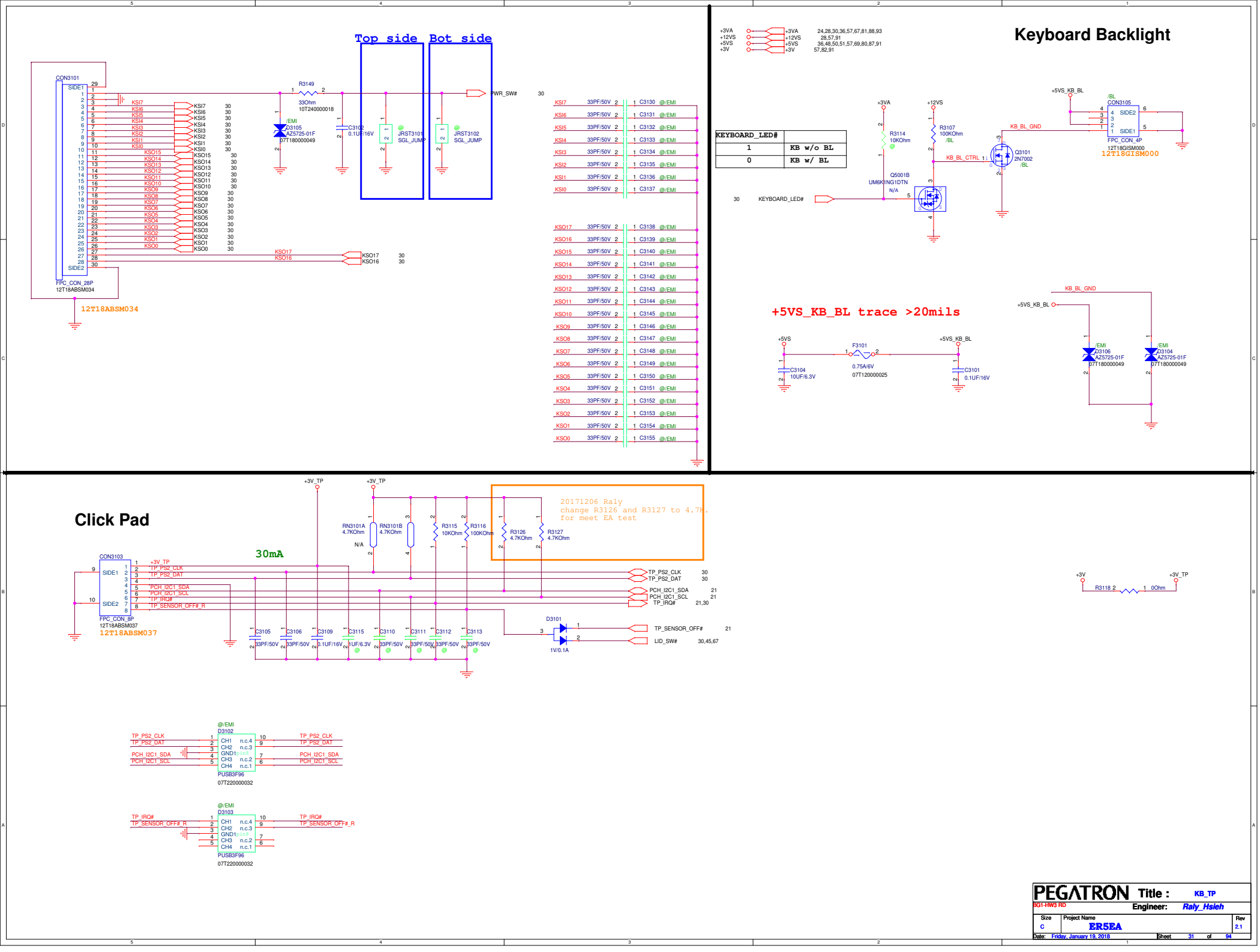
Title : EC_IT8587E/FX

BG1-HW3 RD

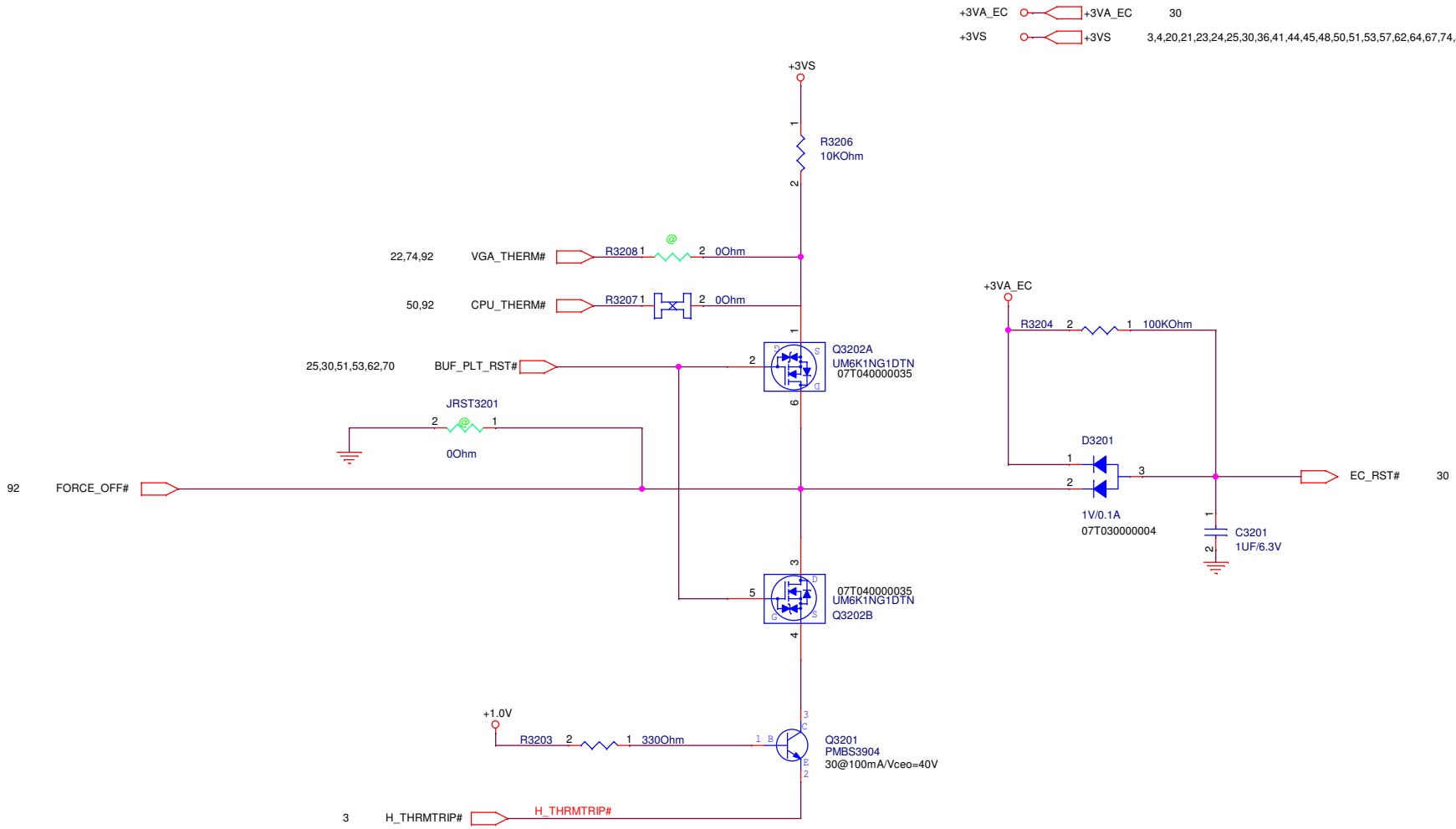
Engineer: Raly_Hsieh

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Saturday, January 20, 2018 Sheet 30 of 94



PEGATRON	Title : KB_TP
BG1-HW3 RD	Engineer: Raly_Hsieh
Size: C	Project Name: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 31 of 94



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : RST_Reset Circuit

BG1-HW3 RD

Engineer: Raly_Hsieh

Size	Project Name	Rev
B	ER5EA	2.1

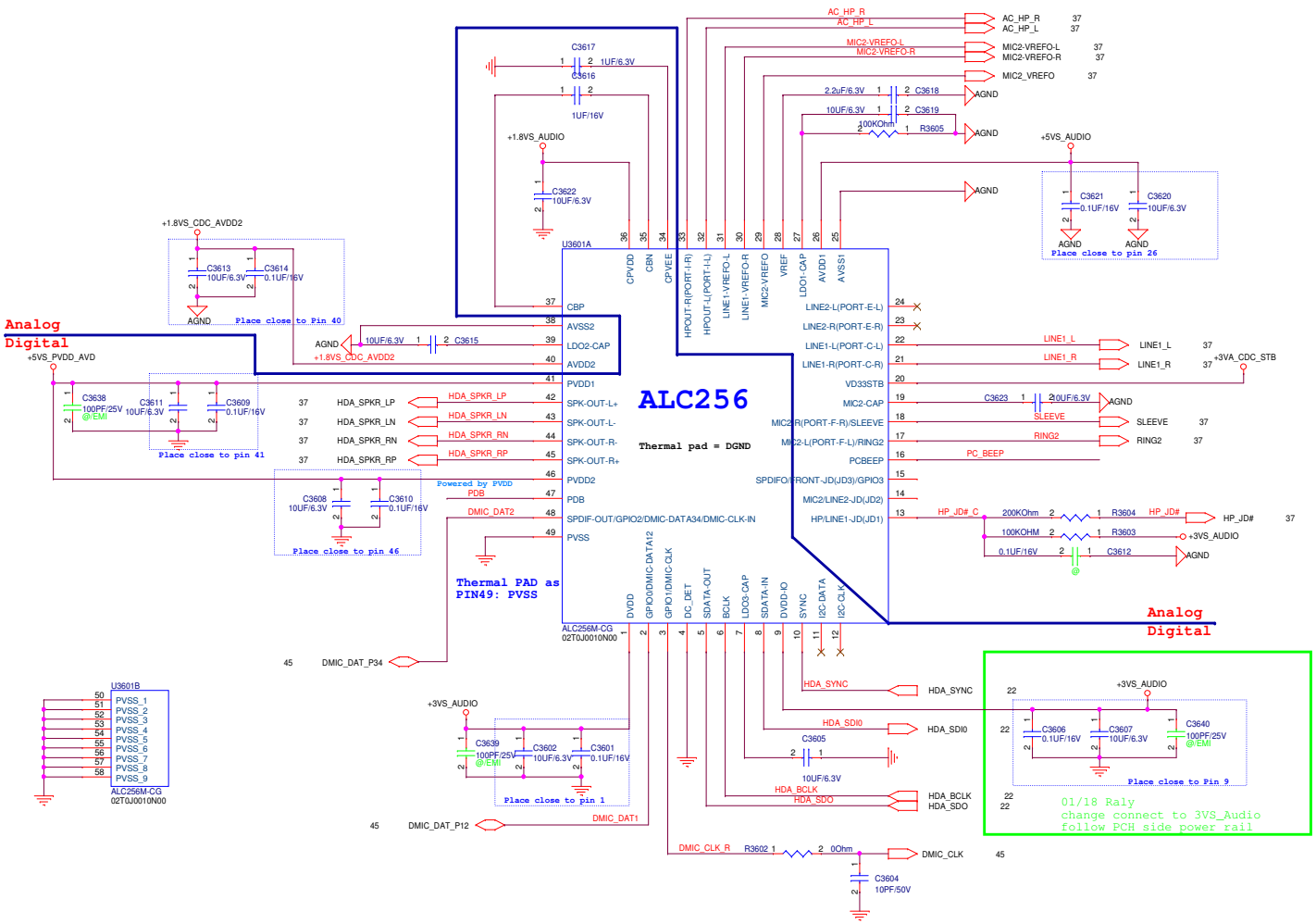
Date: Friday, January 19, 2018 Sheet 32 of 94

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 33 of 94

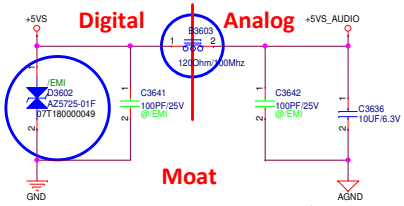
Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 34 of 94

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 35 of 94

Audio Codec

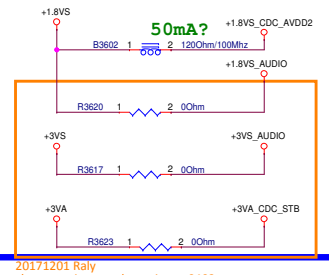


Codec Power



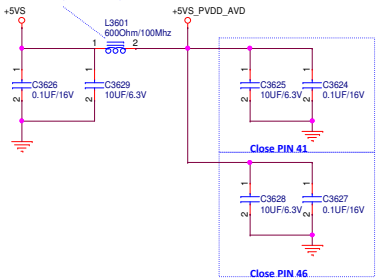
In order to prevent the built-in LDO damaged from over-voltage on +5VS or Standby power line, we suggested using this Voltage suppressing device.

1.8V power rail should be supplied by linear regulator, not switching regulator. if switching regulator is unavoidable, Please make sure that switching frequency operates at out- band(over 20KHz).

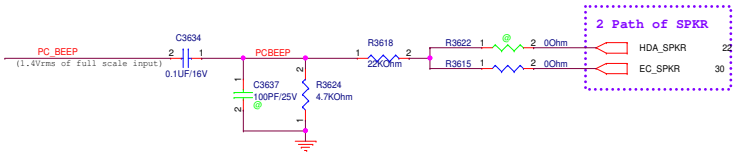


20171201 Raly
change resistor package size to 0402

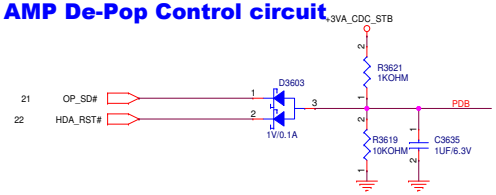
Add this Filter to avoid other components/chips be influenced

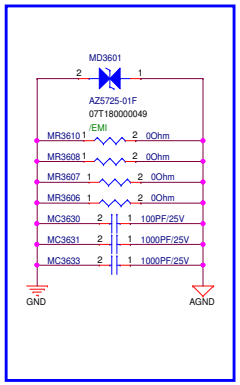


PC BEEP



AMP De-Pop Control circuit

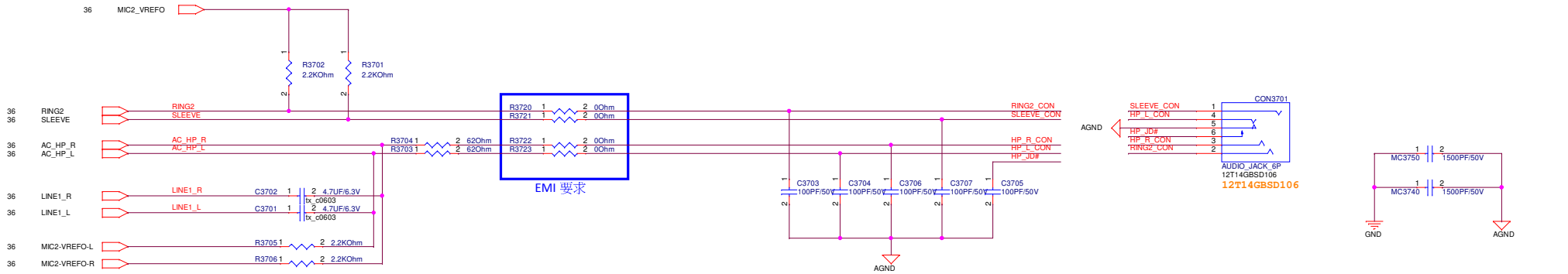




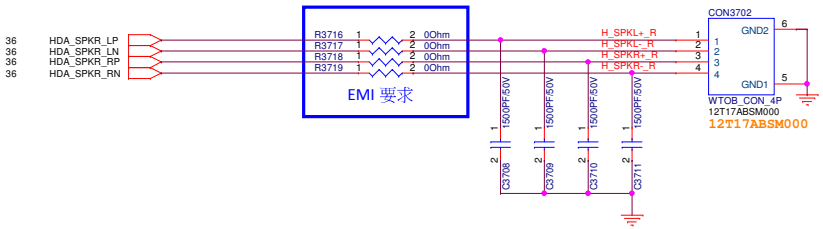
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : Audio Codec ALC256
3G1-HW3 RD
Engineer: Raly_Hsieh

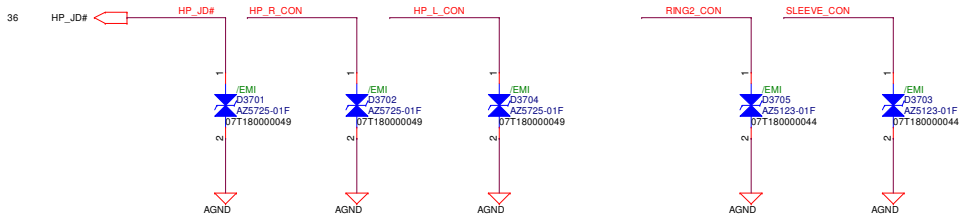
Size	Project Name	Rev
C	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 36 of 94



Internal Speaker





PEGATRON Title :AUD_HP/DMIC/SPK

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD Engineer: Raly_Hsieh

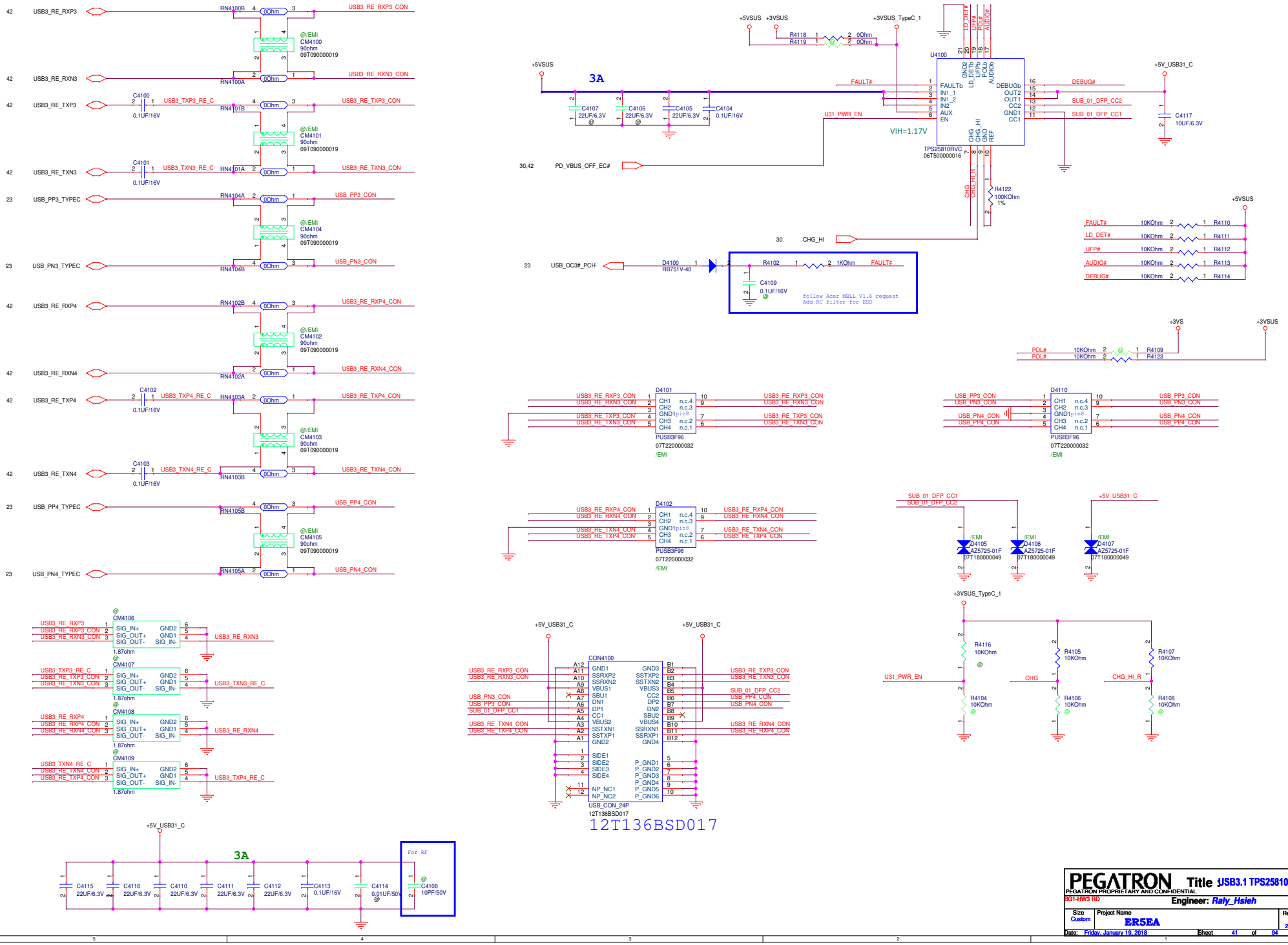
Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 37 of 94

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 38 of 94

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 39 of 94

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 40 of 94



PEGATRON

Title: USB3.1 TPS25810

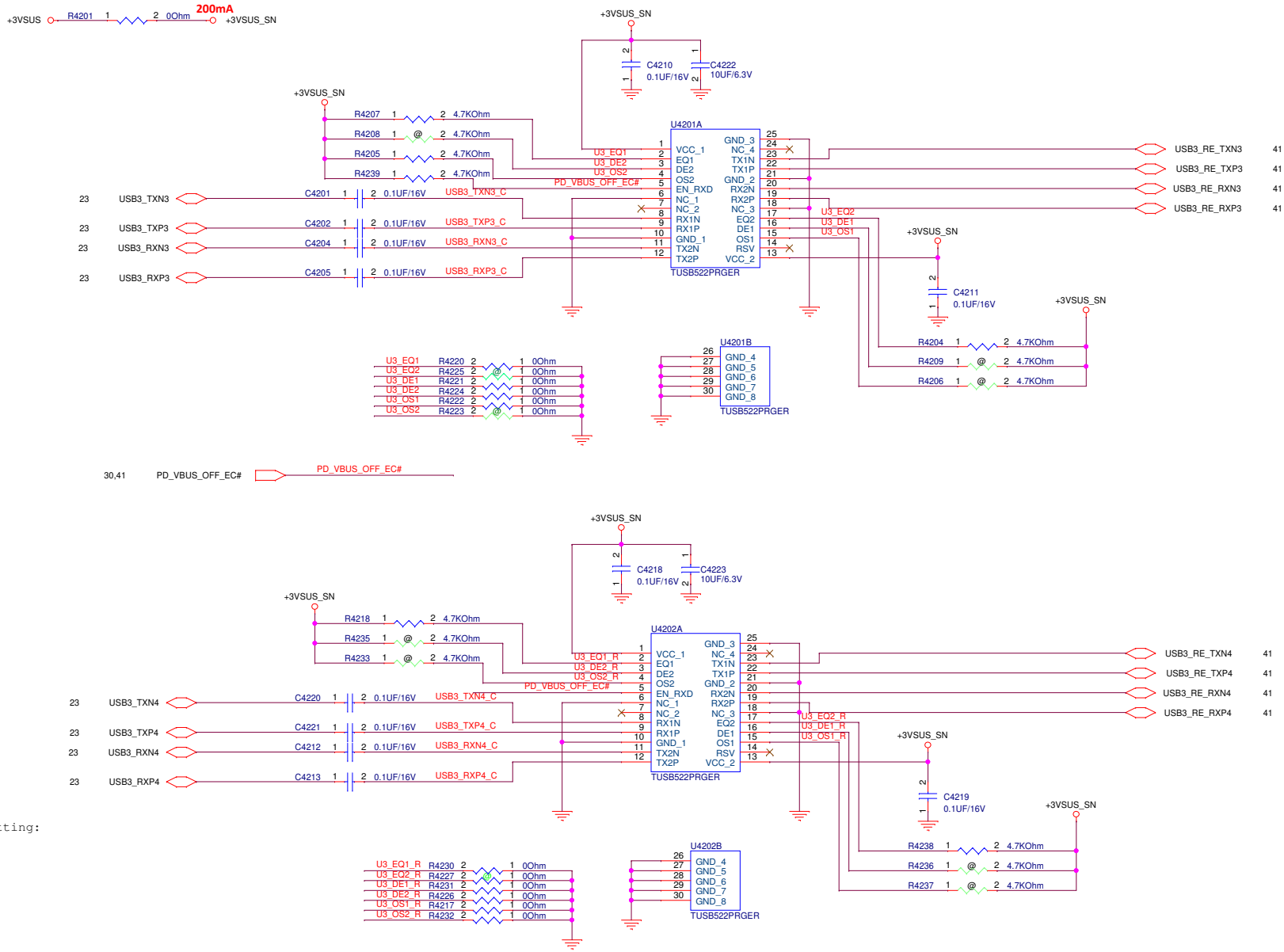
PEGATRON PROPRIETARY AND CONFIDENTIAL

3G1-HW3 RD

Engineer: Raly_Hsieh

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 41 of 94



Defalut setting:

EQ1:3dB

EQ2:3dB

OS1:900mV

OS2:900mV

DE1:0dB

DE2:0dB

Equalizer control

EQ1/EQ2	Channel 1/Channel 2
L	3 dB
Mid	6 dB
H	9 dB

OS1/OS2	Channel 1/Channel 2
L	900mV
H	1100mV

De-emphasis control

DE1/DE2	OS1=0 /OS2=0	DE1/DE2	OS1=1 /OS2=1
L	0 dB	L	-2.6 dB
Mid	-3.5 dB	Mid	-5.9 dB
H	-6.2 dB	H	-8.3 dB

PEGATRON Title : USB3 repeater

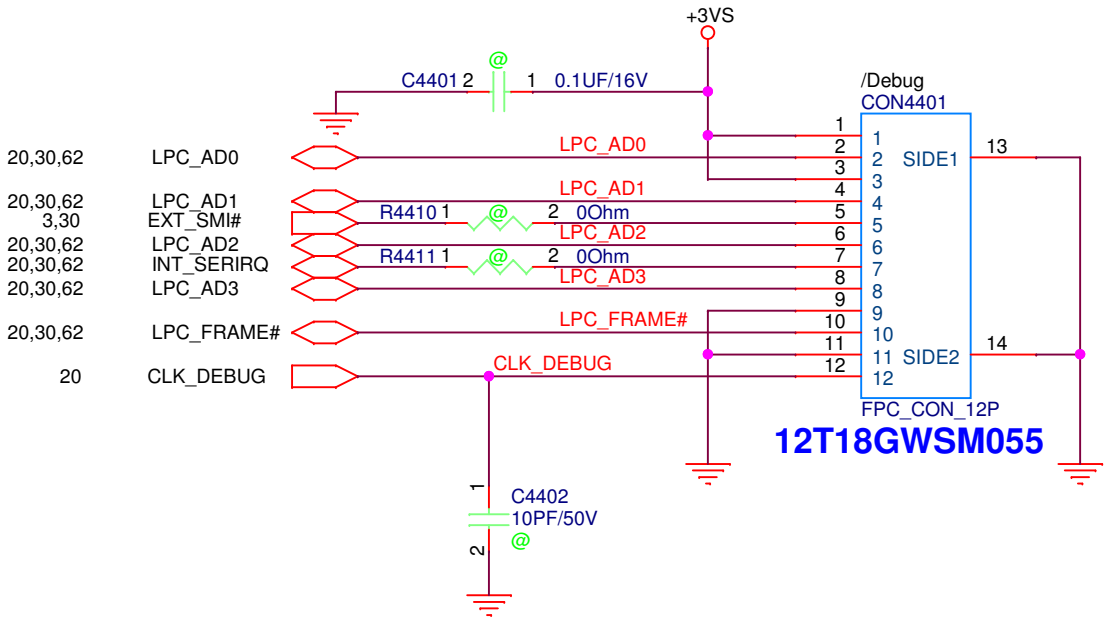
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD Engineer: Raly_Hsieh

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 42 of 94

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 43 of 94



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : DEBUG CONN.

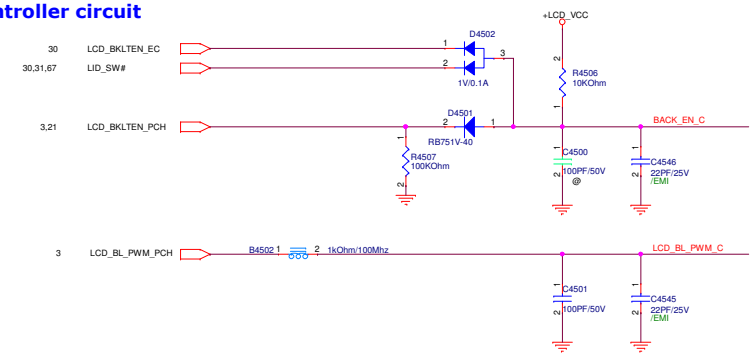
BG1-HW3 RD

Engineer: *Raly_Hsieh*

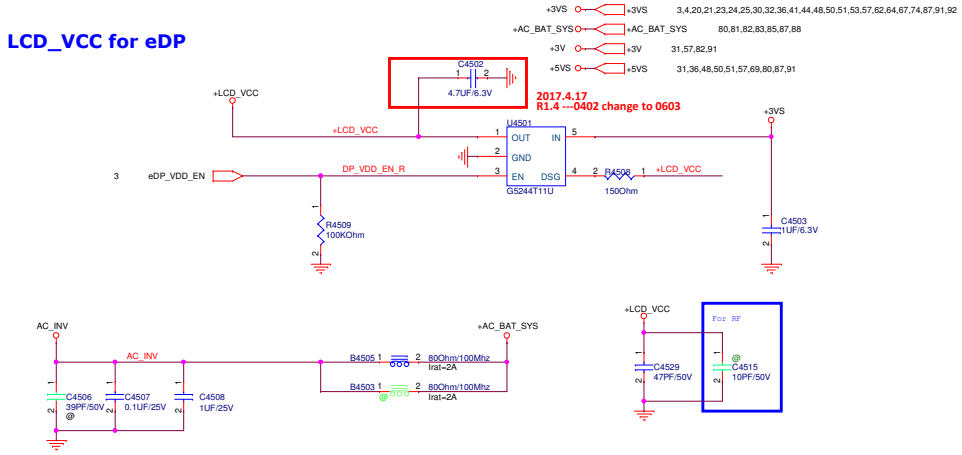
Size	Project Name	Rev
A	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 44 of 94

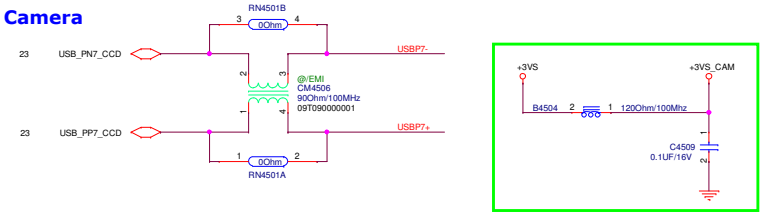
Controller circuit



LCD_VCC for eDP

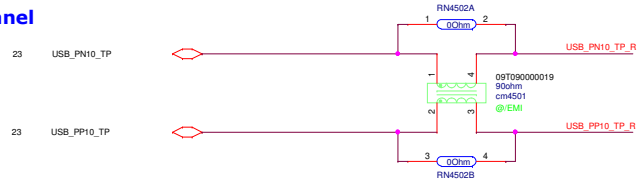


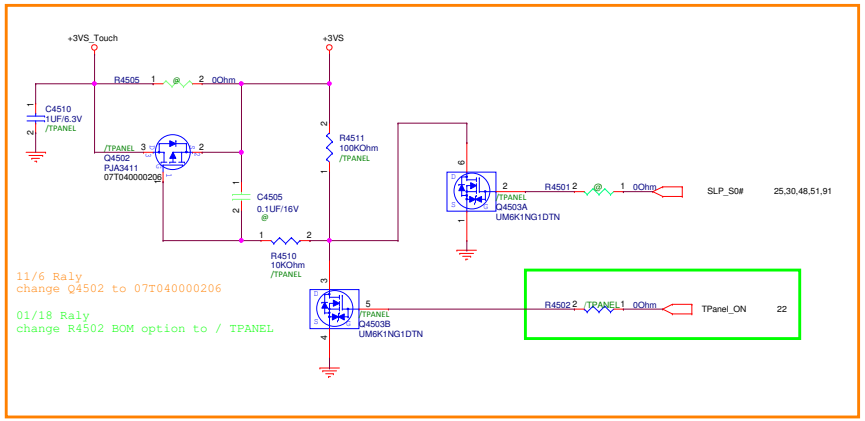
Camera

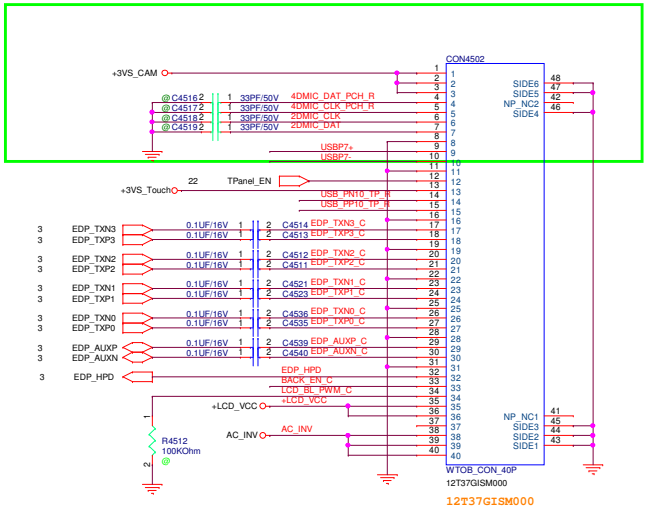


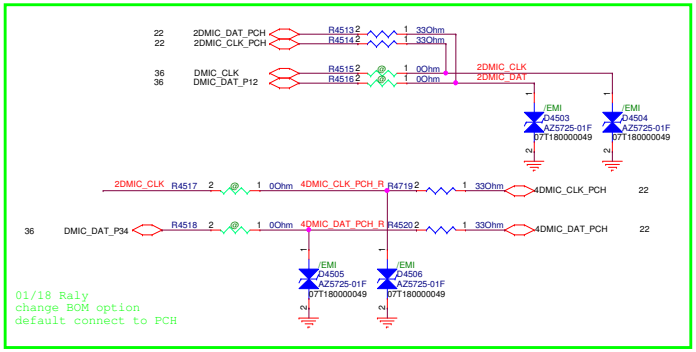
eDP HPD

Touch panel









PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : eDP Out

BG1-HW3 RD

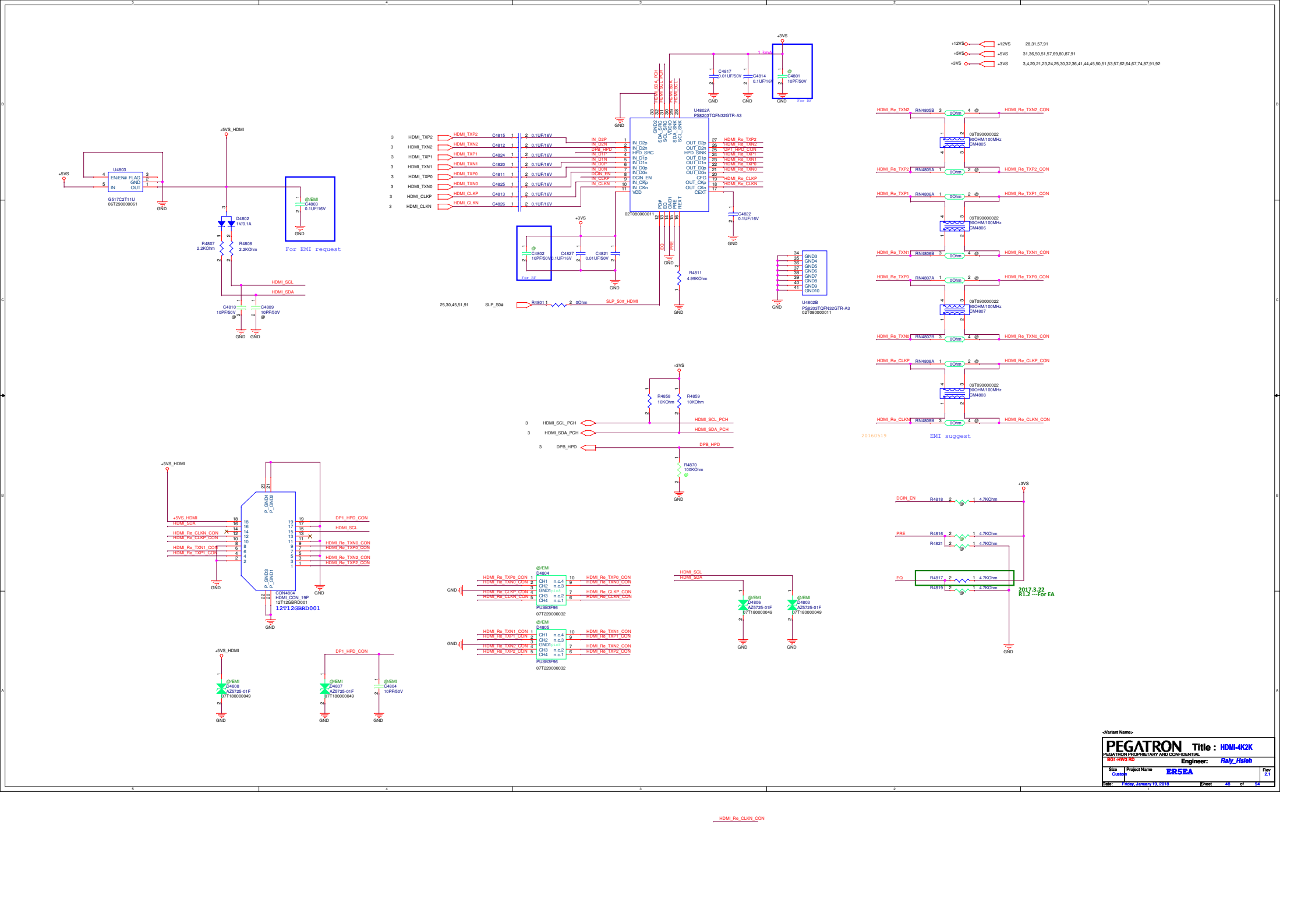
Engineer: Raly_Hsieh

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 45 of 94

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 46 of 94

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 47 of 94



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PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : HDMI-4K2K

BG1-HW3 RD

Engineer: Raly_Hsiah

Size	Project Name	Rev
Custom	ER5EA	Z.1

Date: Friday, January 19, 2018 Sheet 48 of 94

<Variant Name>

PEGATRON

Title : eMMC

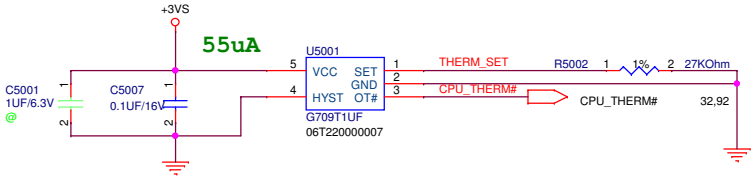
BG1-HW3 RD

Engineer: Raiy_Hsieh

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 49 of 94

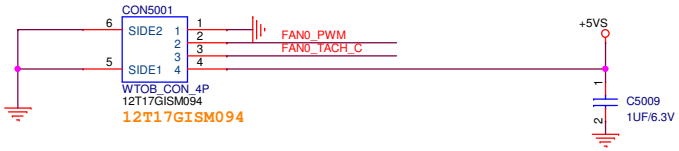
Thermal Sensor for package test

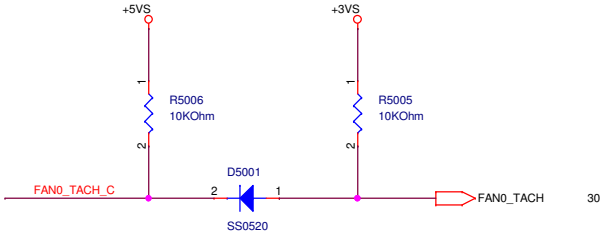


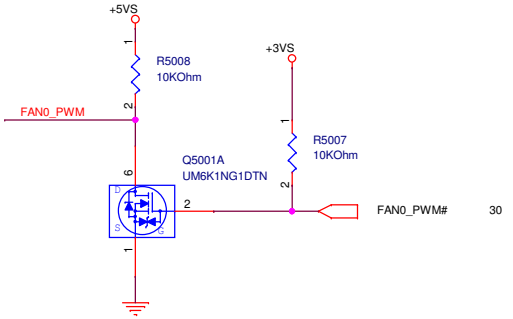
temp setting : 83 degree

RSET(kΩ)= 0.0012T2 – 0.9308T + 96.147

FAN

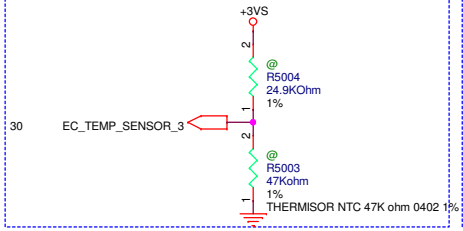




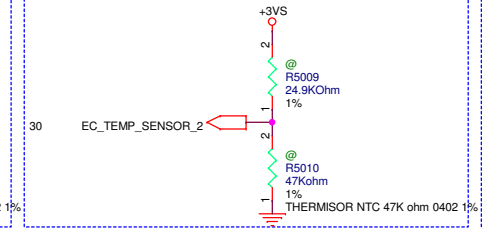


DPTF

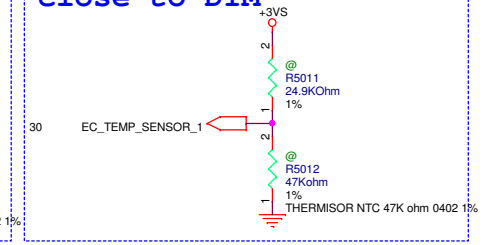
close to CPU VR



close to GPU VR

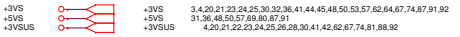


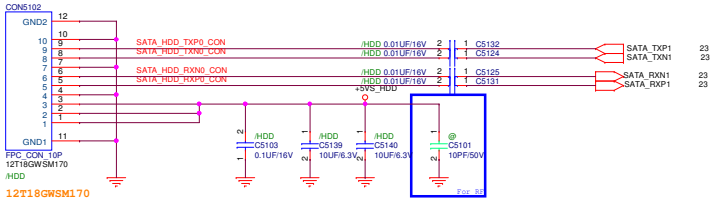
close to DIM

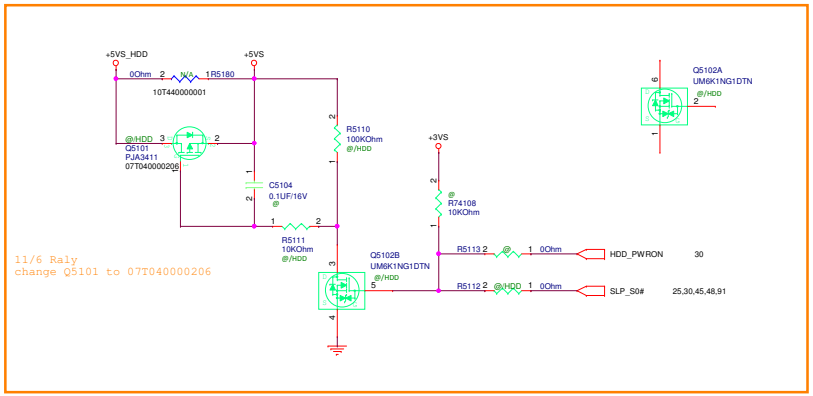


PEGATRON	Title : Thermal_Fan	
BG1-HW3 RD	Engineer: Raly_Hsieh	
Size: Custom	Project Name: ER5EA	Rev: 2.1
Date: Friday, January 19, 2018	Sheet 50 of 94	

SATA HDD

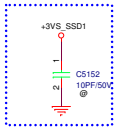




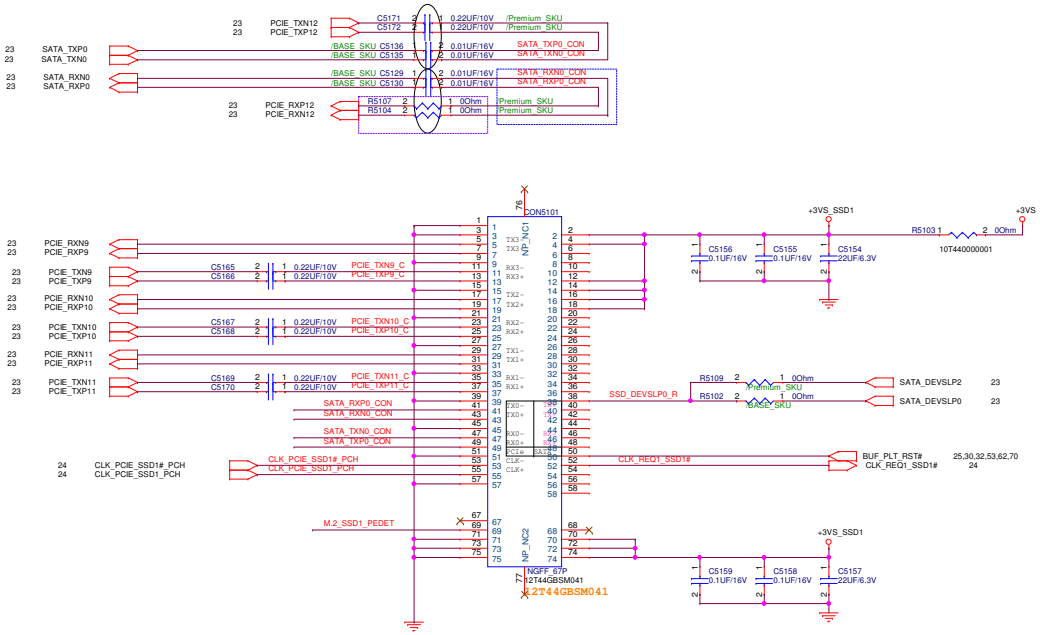


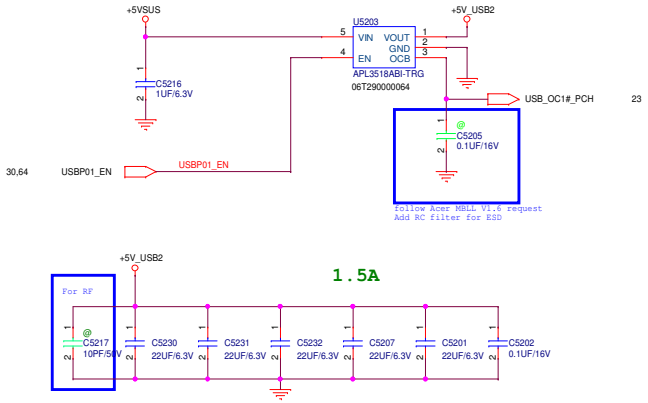
SATA / PCIe SSD

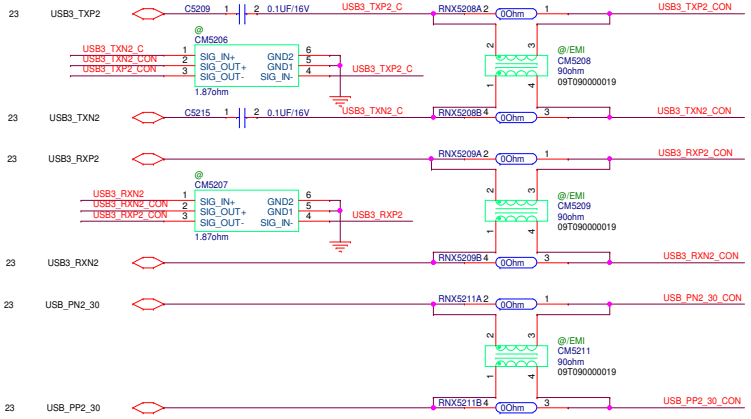
RF requirement

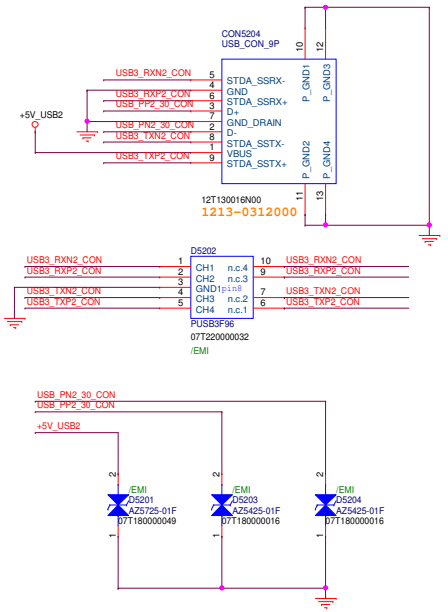


SSD



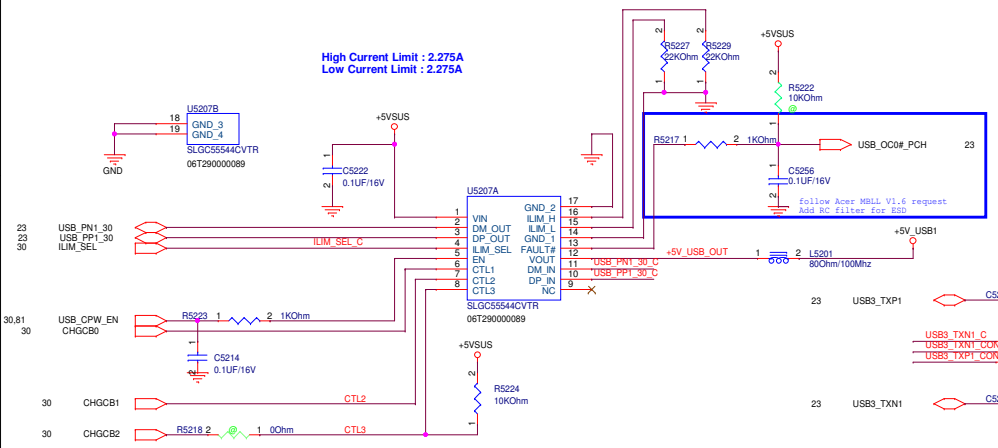




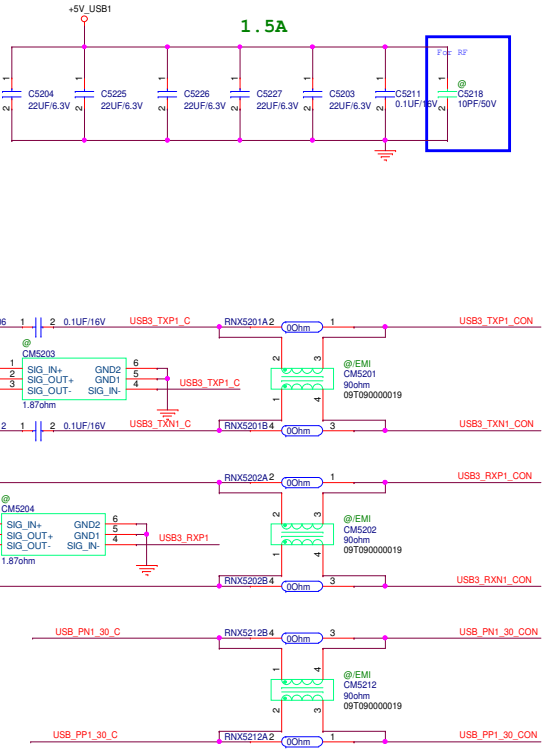


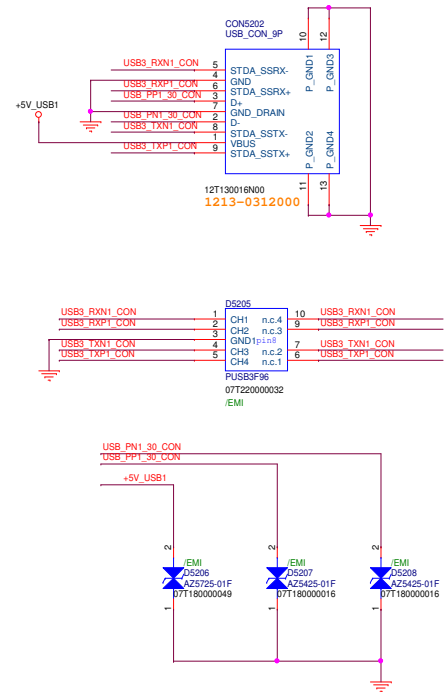
USB 3.0 ports x 1 with Sleep & Charge Left_Down

Device	Pega No.	VX No.
SLGC55544CVTR	0629-00TJ000	06V290000089 (Default)



System Global Power State	TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	SDP (Standard Downstream)	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode, no mouse wake	0	0	1	0	ILIM_HI
S3 / S4	Dedicated Charging Port Auto mode,	0	1	1	X	ILIM_HI
S3	SDP, keyboard/ mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO



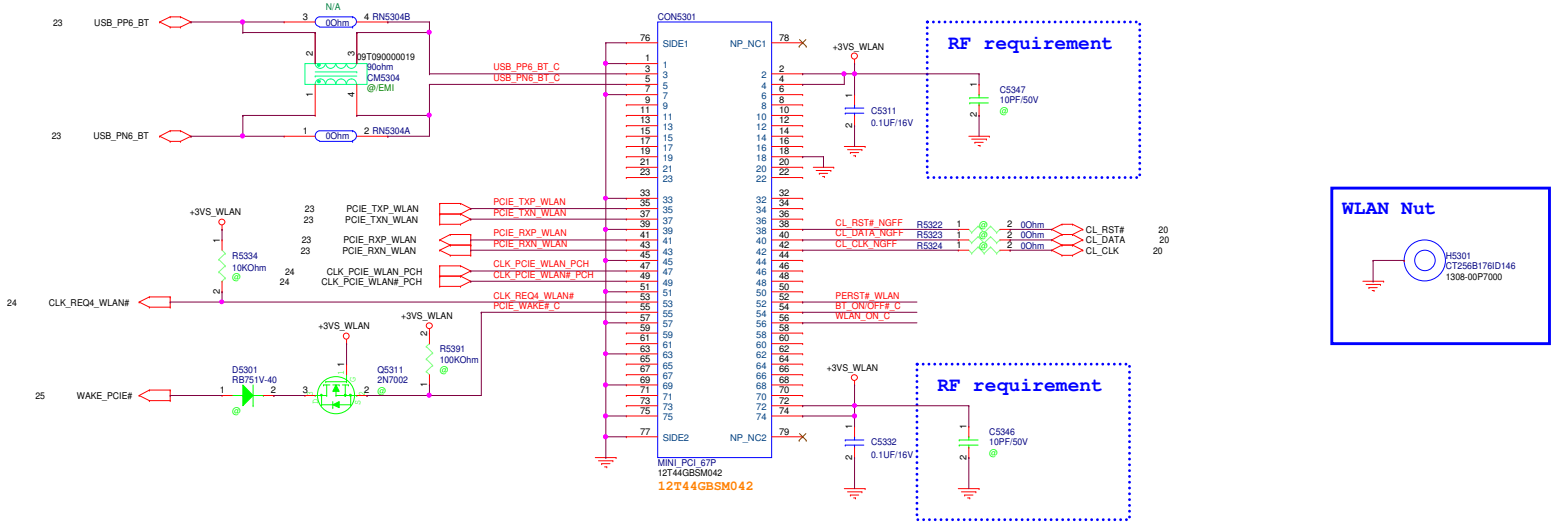


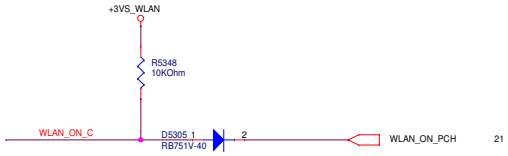
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
3G1-HW3 RD

Title: USB3.0_Charge IC
Engineer: Raly_Hsieh

Size	Project Name	Rev
C	ER5EA	2.1

Date: Wednesday, January 24, 2018 Sheet 52 of 94

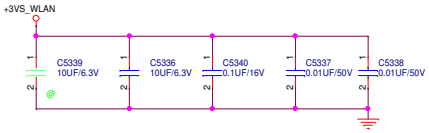


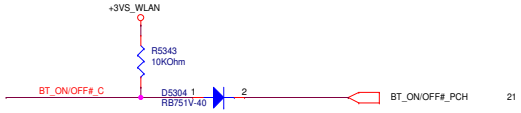


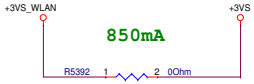
+3V_WLAN_WP1 bypass capactor:

Place 0.1UF near pin 2,4

Place 10UF near +3V_WLAN_WP1 source side.

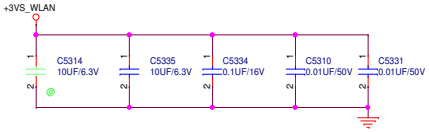


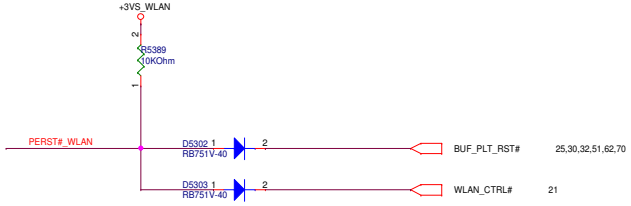


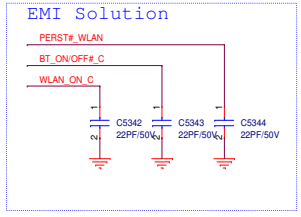


Place 0.1UF near pin 72,74.

Place 10UF near +3V_WLAN_WP1 source side.







PEGATRON Title : PCIE_WLAN_BT

PEGATRON PROPRIETARY AND CONFIDENTIAL

3G1-HW3 RD

Engineer: Raly_Hsieh

Size	Project Name	Rev
C	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 53 of 94

PEGATRON Title : G-Sensor

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD

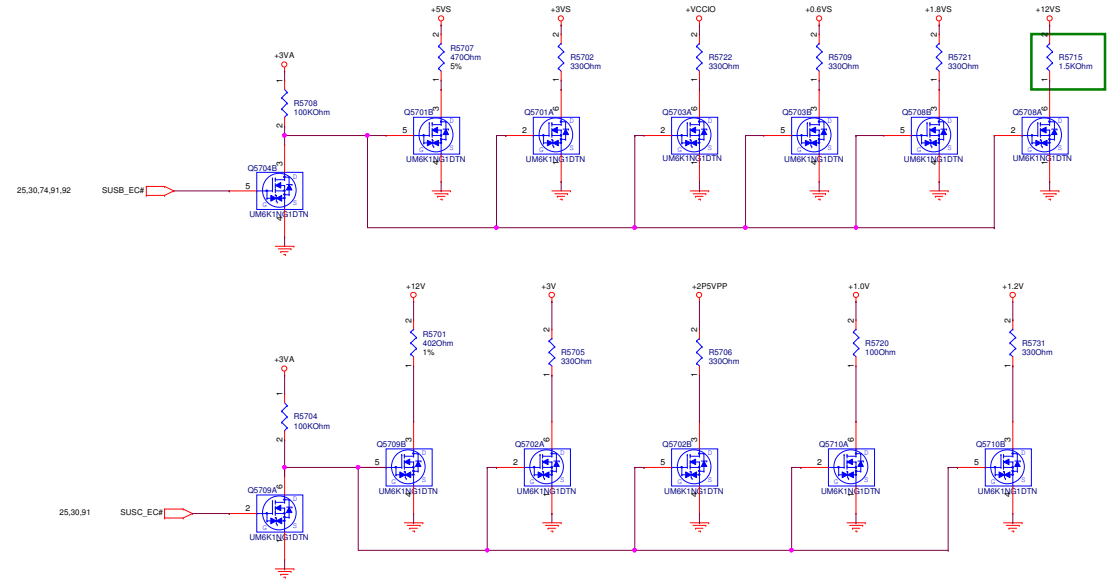
Engineer: Raly_Hsieh

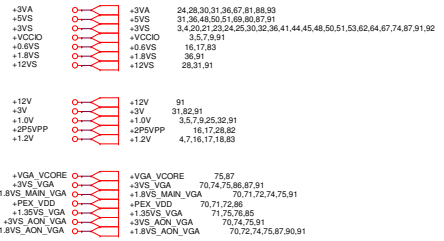
Size	Project Name	Rev
B	ER5EA	2.1

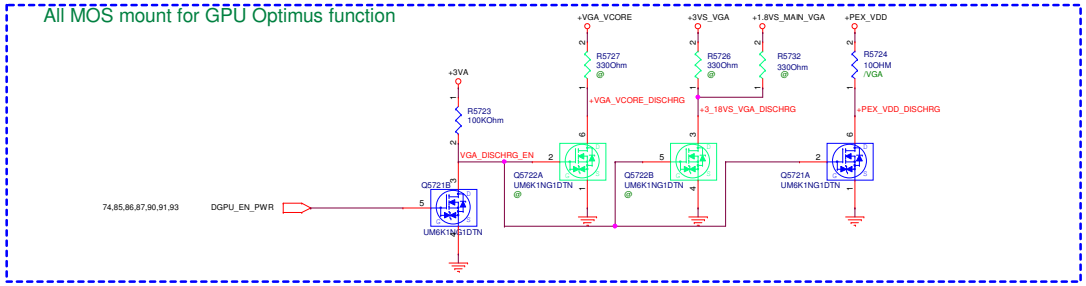
Date: Friday, January 19, 2018 Sheet 54 of 94

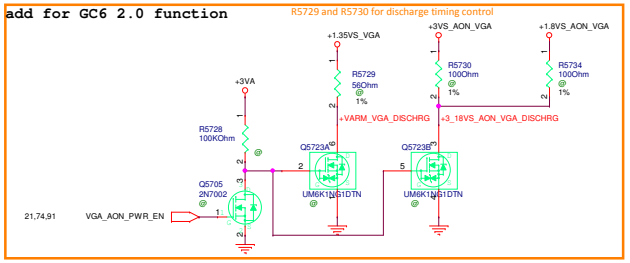
Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 55 of 94

PEGATRON
CONFIDENTIAL-PROPRIETARY AND CONFIDENTIAL
Title: SATA SSD_HDD
DO-HW3 HD
Engineer: Raly_Hsieh
Size: D
Project Name: ER5EA
Rev: 2.1
Date: Friday, January 19, 2018
Sheet 58 of 94









PEGATRON Title : DISCHARGE

PEGATRON PROPRIETARY AND CONFIDENTIAL

BGT-HW3 RD Engineer: Raly_Hsieh

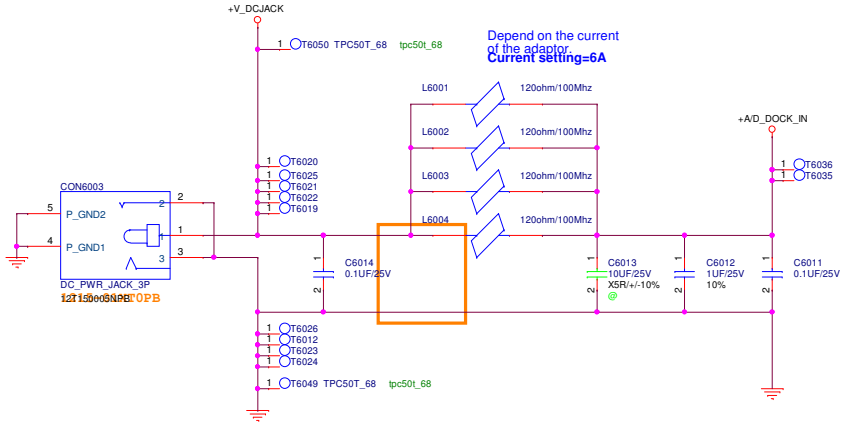
Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 57 of 94

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 58 of 94

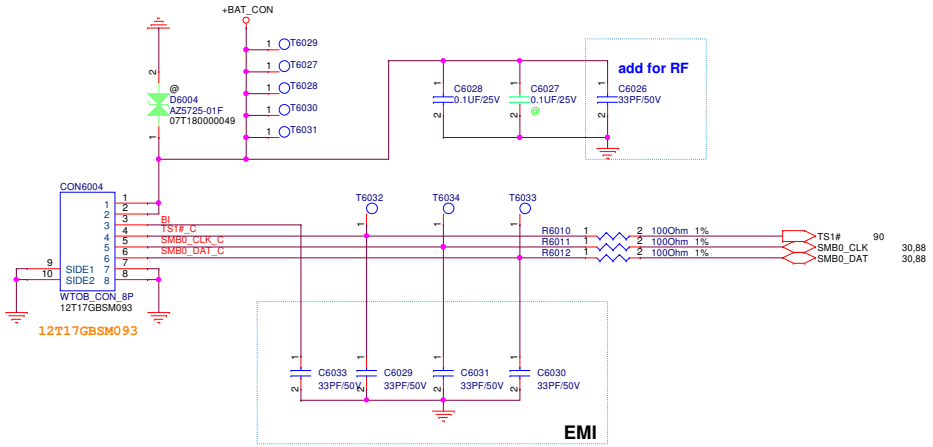
Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 59 of 94

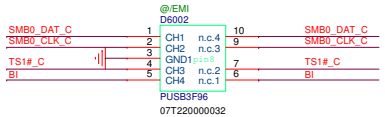
DC Jack WTB CONN

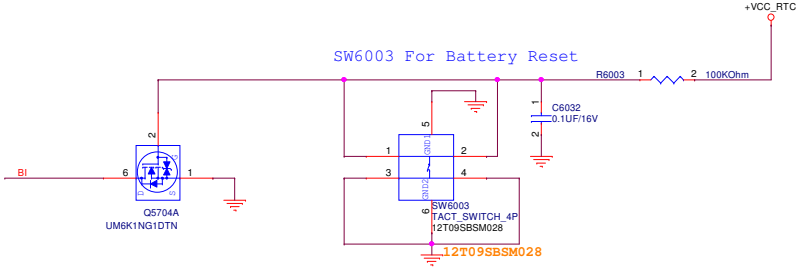


+VCC_RTC +VCC_RTC 24,25,26
+A/D_DOCK_IN +A/D_DOCK_IN 88
+BAT_CON +BAT_CON 88

Battery Connector



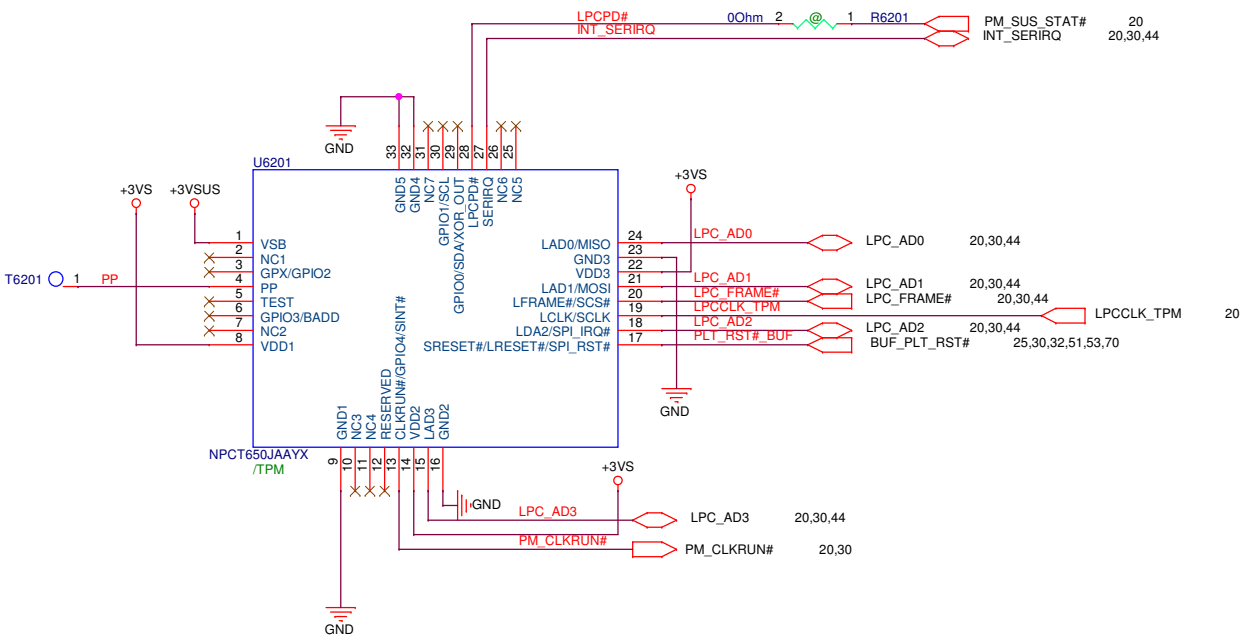


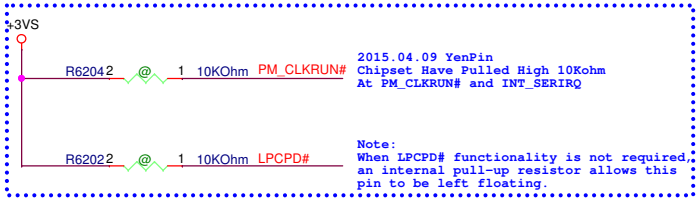


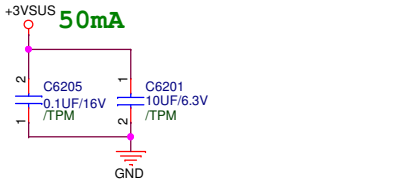
PEGATRON	Title : DC_BAT_CONN		
BG1-HW3 RD	Engineer: Raly_Hsieh		
Size: Custom	Project Name: ER5EA		Rev: 2.1
Date: Friday, January 19, 2018	Sheet 60 of 94		

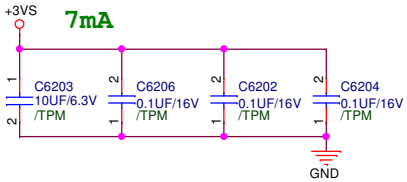
Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 61 of 94

62 TPM NPCT650





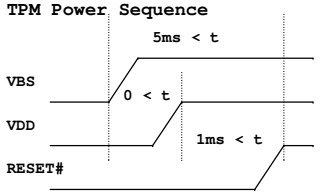




TPM

VDD: Power the I/O buffers of the GPIO ports and the Host Interface
VSB: Standby 3.3V Power Supply. Powers the on-chip Core.

TPM Power Sequence



NOTE: RESET# is LRESET#, SPI_RST# or SRESET#.

NOTE:
1) For TPM 1.2:
The TPM VSB pin must be connected to the system's standby voltage (existing at S3 power state).
2) For TPM 2.0:
It is recommended to connect the TPM VSB pin to the system's standby voltage to improve performance.
3) TPM VDD pins should be connected to the same power rail that feeds the Chipset LPC interface.
4) RESET# must be asserted for at least 5 msec after VSB power-up.
5) VSB may come up anytime before VDD power-up, but not after VDD power-up.
6) RESET# may be asserted together with VDD power negation, but should not at any point exceed 0.5V above the VDD power level.

PEGATRON	Title : TPM NPCT650	
BG1-HW3 RD	Engineer: Raly_Hsieh	
Size: B	Project Name: ER5EA	Rev: 2.1
Date: Friday, January 19, 2018	Sheet 62 of 94	

<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : USB 2.0 Hub

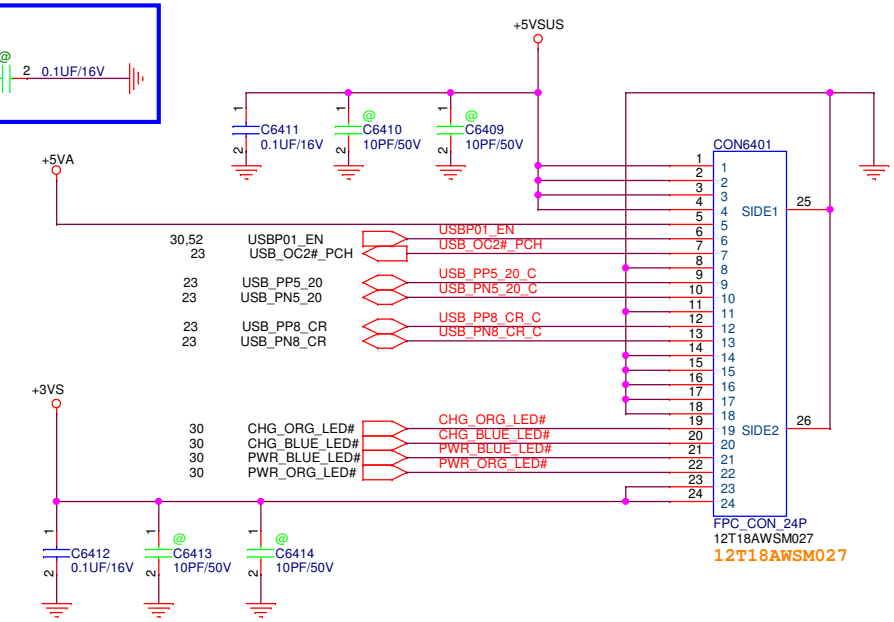
Engineer: Raly_Hsieh

Size	Project Name	Rev
A	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 63 of 94

follow Acer MBLL V1.6 request
Add RC filter for ESD

USB_OC2#_PCH — C64151 @ 2 0.1UF/16V



DB Connector Pin Define(MB Side)

1		+5VSUS
2		+5VSUS
3		+5VSUS
4		+5VSUS
5		+5VA
6		USB_EN
7		USB_OC
8	GND_IO	
9		USB_PP1_20
10		USB_PN1_20
11	GND_IO	
12		USB_PP2_20
13		USB_PN2_20
14	GND_IO	
15	GND_IO	
16	GND_IO	
17	GND_IO	
18	GND_IO	
19		CHG_ORG_LED#
20		CHG_BLUE_LED#
21		PWR_BLUE_LED#
22		PWR_ORG_LED#
23		+3VS
24		+3VS

PEGATRON Title : IO Board
BG1-HW3 RD Engineer: Raly_Hsieh

Size	Project Name	Rev
B	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 64 of 94

<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : G-Sensor

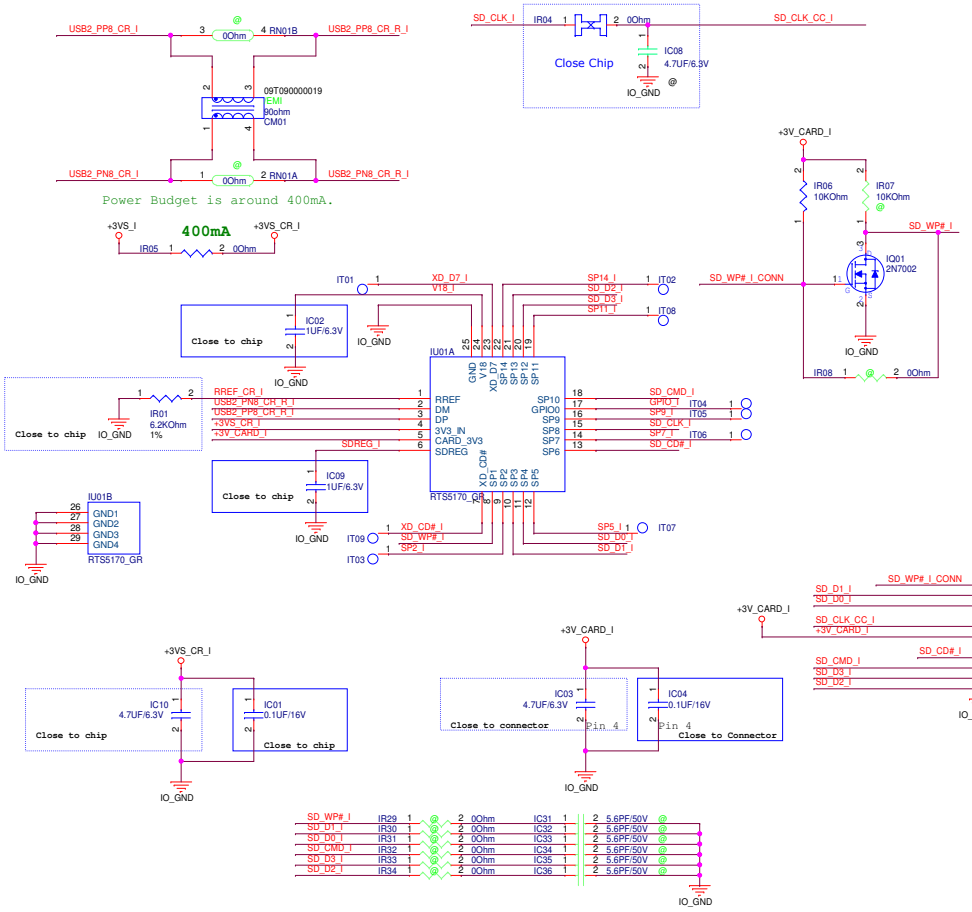
Engineer: *Raly_Hsieh*

Size	Project Name	Rev
A	ER5EA	2.1

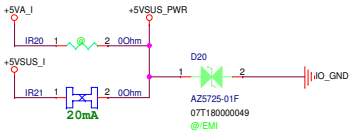
Date: Friday, January 19, 2018 Sheet 65 of 94

66 IO Board

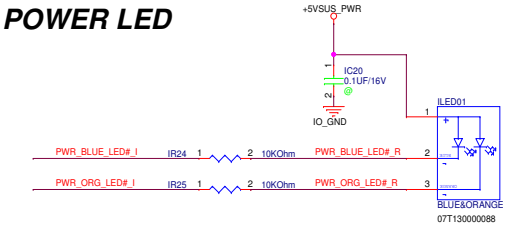
Card Reader



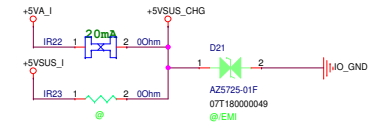
POWER LED



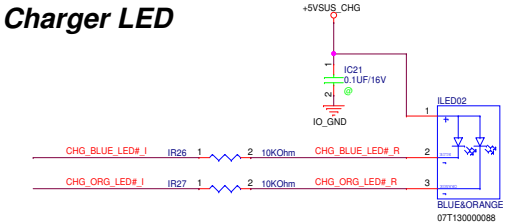
POWER LED

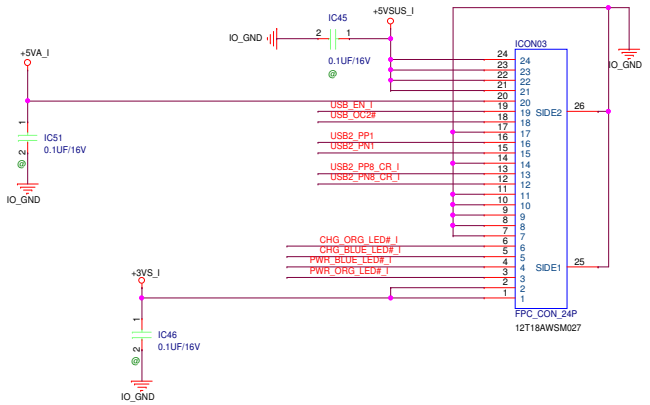


Charger LED

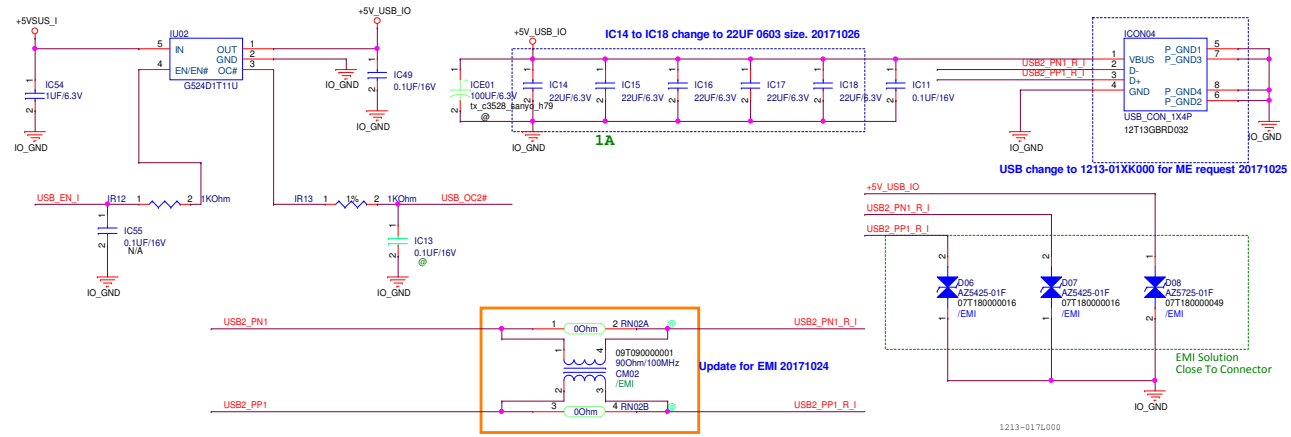


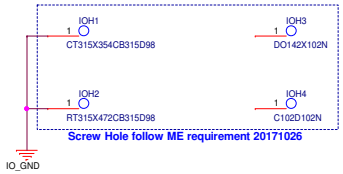
Charger LED





USB 2.0





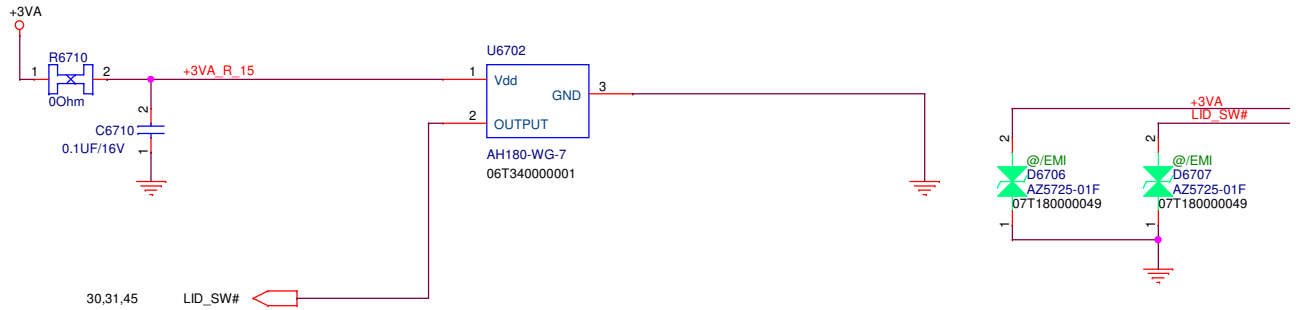
PEGATRON Title : IO Board

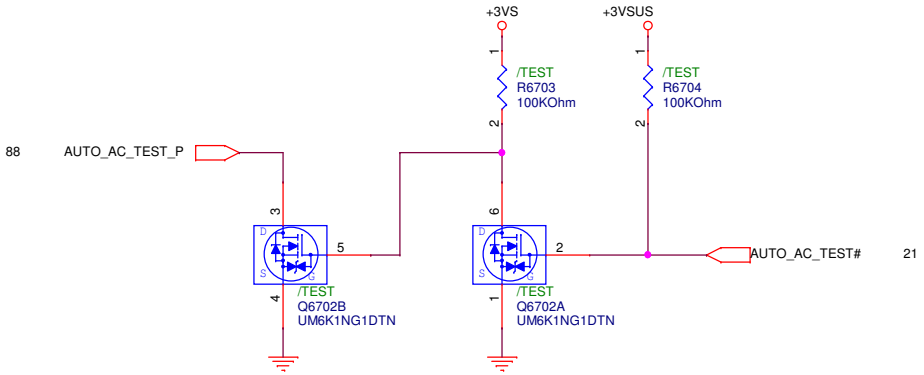
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD Engineer: Joe_Lo

Size	Project Name	Rev
C	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 66 of 94





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LID

BG1-HW3 RD

Engineer: Raly_Hsieh

Size	Project Name	Rev
B	ER5EA	2.1

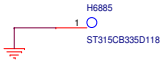
Date: Friday, January 19, 2018 Sheet 67 of 94

68 ME Hole

鎖IO PORT SHIELDING螺絲孔

K

F



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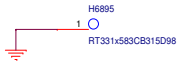
C



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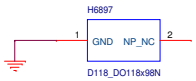

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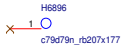
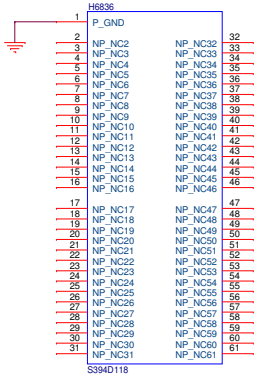
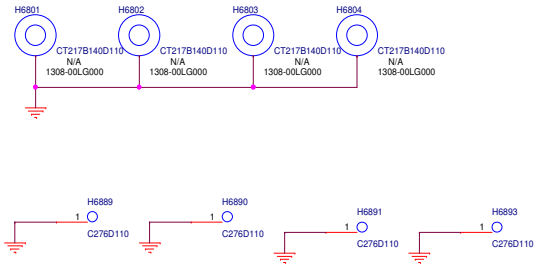


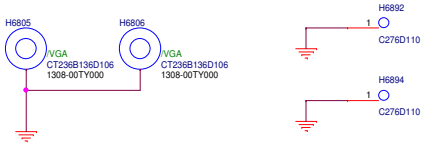
斷熱孔(Screw C)



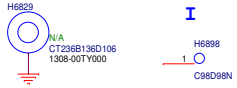
CPU NUT(Screw A1)



GPU NUT(Screw B1)



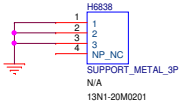
Main Shielding NUT



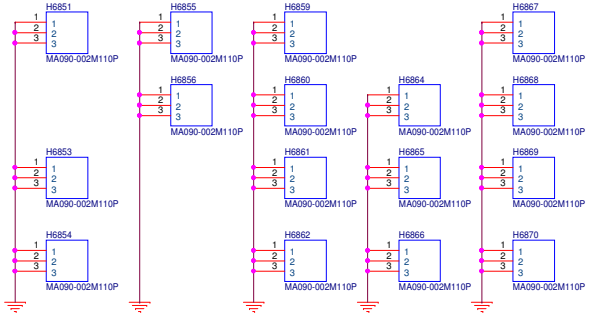
I

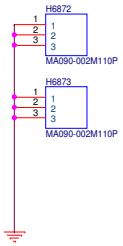
Main shielding 定位孔 (Screw D,L)

Screw support metal(Screw I)



CPU Clip(BOT)





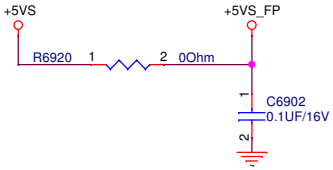
PEGATRON Title : ME Hole

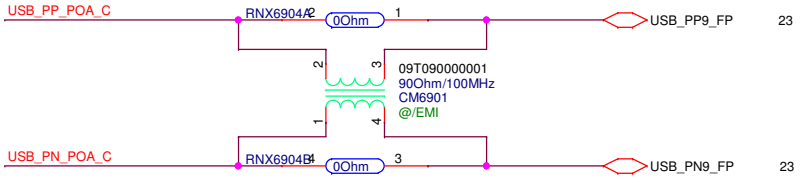
PEGATRON PROPRIETARY AND CONFIDENTIAL

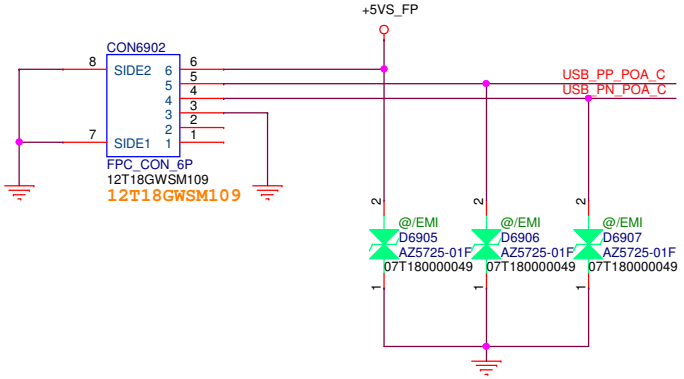
BG1-HW3 RD Engineer: Raly_Hsieh

Size	Project Name	Rev
C	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 68 of 94







Pin	Definition
1	+PP_VCC
2	USBP
3	USBN
4	GND
5	NC
6	NC

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD

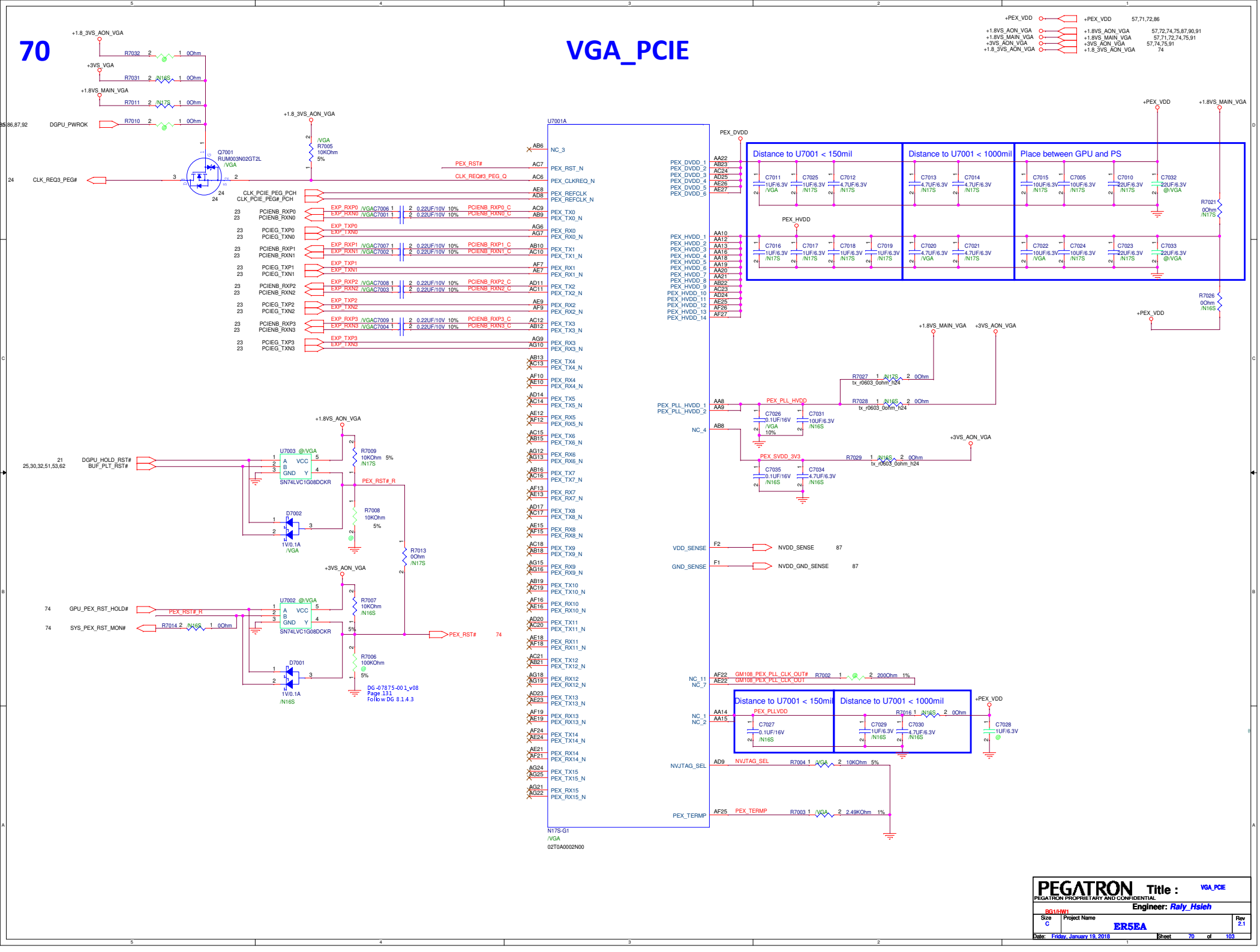
Title : Finger printer
Engineer: Raly_Hsieh

Size	Project Name	Rev
B	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 69 of 94

70

VGA_PCIE



PEGATRON	Title : VGA_PCIE
PEGATRON PROPRIETARY AND CONFIDENTIAL	Engineer: Raly_Hsieh
BG1/HW1	
Size: C	Project Name: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 70 of 103

VGA_FRAME BUFFER_GDDR5

76 FBAD[0..63]
76 FBA_DBI[0..7]
76 FBA_EDC[0..7]

+1.35VS_VGA
+1.8VS_MAIN_VGA
+PEX_VDD

+1.35VS_VGA 57,75,76,85
+1.8VS_MAIN_VGA 57,70,72,74,75,91
+PEX_VDD 57,70,72,86

U7001B

FBAD0 E18 FBA_D0
FBAD1 F18 FBA_D1
FBAD2 E16 FBA_D2
FBAD3 F17 FBA_D3
FBAD4 D20 FBA_D4
FBAD5 D21 FBA_D5
FBAD6 F20 FBA_D6
FBAD7 E21 FBA_D7
FBAD8 E15 FBA_D8
FBAD9 D15 FBA_D9
FBAD10 F15 FBA_D10
FBAD11 F19 FBA_D11
FBAD12 C13 FBA_D12
FBAD13 B13 FBA_D13
FBAD14 E13 FBA_D14
FBAD15 D13 FBA_D15
FBAD16 B15 FBA_D16
FBAD17 C16 FBA_D17
FBAD18 A13 FBA_D18
FBAD19 A15 FBA_D19
FBAD20 B18 FBA_D20
FBAD21 A18 FBA_D21
FBAD22 A19 FBA_D22
FBAD23 C19 FBA_D23
FBAD24 B24 FBA_D24
FBAD25 C23 FBA_D25
FBAD26 A25 FBA_D26
FBAD27 A24 FBA_D27
FBAD28 A21 FBA_D28
FBAD29 B21 FBA_D29
FBAD30 C20 FBA_D30
FBAD31 C21 FBA_D31
FBAD32 R22 FBA_D32
FBAD33 R24 FBA_D33
FBAD34 T22 FBA_D34
FBAD35 R23 FBA_D35
FBAD36 N25 FBA_D36
FBAD37 N26 FBA_D37
FBAD38 N23 FBA_D38
FBAD39 N24 FBA_D39
FBAD40 V23 FBA_D40
FBAD41 V22 FBA_D41
FBAD42 T23 FBA_D42
FBAD43 U22 FBA_D43
FBAD44 Y24 FBA_D44
FBAD45 AA24 FBA_D45
FBAD46 Y22 FBA_D46
FBAD47 AA23 FBA_D47
FBAD48 AD27 FBA_D48
FBAD49 AB25 FBA_D49
FBAD50 AD26 FBA_D50
FBAD51 AC25 FBA_D51
FBAD52 AA27 FBA_D52
FBAD53 AA26 FBA_D53
FBAD54 W26 FBA_D54
FBAD55 Y25 FBA_D55
FBAD56 R26 FBA_D56
FBAD57 T25 FBA_D57
FBAD58 N27 FBA_D58
FBAD59 R27 FBA_D59
FBAD60 V26 FBA_D60
FBAD61 V27 FBA_D61
FBAD62 W27 FBA_D62
FBAD63 W25 FBA_D63

FBA_DBI0 D19 FBA_DQM0
FBA_DBI1 D14 FBA_DQM1
FBA_DBI2 C17 FBA_DQM2
FBA_DBI3 C25 FBA_DQM3
FBA_DBI4 P24 FBA_DQM4
FBA_DBI5 W24 FBA_DQM5
FBA_DBI6 AA25 FBA_DQM6
FBA_DBI7 U25 FBA_DQM7

FBA_EDC0 E19 FBA_DQS_WP0
FBA_EDC1 C15 FBA_DQS_WP1
FBA_EDC2 B16 FBA_DQS_WP2
FBA_EDC3 B22 FBA_DQS_WP3
FBA_EDC4 R25 FBA_DQS_WP4
FBA_EDC5 W23 FBA_DQS_WP5
FBA_EDC6 AB26 FBA_DQS_WP6
FBA_EDC7 T26 FBA_DQS_WP7

F19 FBA_DQS_RN0
C14 FBA_DQS_RN1
A16 FBA_DQS_RN2
A22 FBA_DQS_RN3
P26 FBA_DQS_RN4
W22 FBA_DQS_RN5
AB27 FBA_DQS_RN6
T27 FBA_DQS_RN7

T7101 1 FB_VREF D23 FB_VREF

GNDS_SENSE F3 GPU_FB_CLAMP_R R7113 2 /N16S 1 10KOhm

35 mA

+1.35VS_VGA

FBA_CMD14 R7106 2 1 10KOhm 5%
FBA_CMD30 R7105 2 1 10KOhm 5%
FBA_CMD13 R7107 2 1 10KOhm 5%
FBA_CMD29 R7108 2 1 10KOhm 5%

FBA_CMD[0..31] 76

FBA_CMD0 C27 FBA_CMD0
FBA_CMD1 C26 FBA_CMD1
FBA_CMD2 E24 FBA_CMD2
FBA_CMD3 F24 FBA_CMD3
FBA_CMD4 D27 FBA_CMD4
FBA_CMD5 D26 FBA_CMD5
FBA_CMD6 F25 FBA_CMD6
FBA_CMD7 F26 FBA_CMD7
FBA_CMD8 F23 FBA_CMD8
FBA_CMD9 G22 FBA_CMD9
FBA_CMD10 G23 FBA_CMD10
FBA_CMD11 G24 FBA_CMD11
FBA_CMD12 F27 FBA_CMD12
FBA_CMD13 G25 FBA_CMD13
FBA_CMD14 G27 FBA_CMD14
FBA_CMD15 G26 FBA_CMD15
FBA_CMD16 M24 FBA_CMD16
FBA_CMD17 M23 FBA_CMD17
FBA_CMD18 K24 FBA_CMD18
FBA_CMD19 K23 FBA_CMD19
FBA_CMD20 M27 FBA_CMD20
FBA_CMD21 M26 FBA_CMD21
FBA_CMD22 M25 FBA_CMD22
FBA_CMD23 K26 FBA_CMD23
FBA_CMD24 K22 FBA_CMD24
FBA_CMD25 J23 FBA_CMD25
FBA_CMD26 J25 FBA_CMD26
FBA_CMD27 J24 FBA_CMD27
FBA_CMD28 K27 FBA_CMD28
FBA_CMD29 K25 FBA_CMD29
FBA_CMD30 J27 FBA_CMD30
FBA_CMD31 J26 FBA_CMD31

nVidia Design Guide
DG-07875-001_v08 P.154
Table 9.5

	LOWER 0..31	UPPER 32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA2	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

FBA_CMD32 B19
FBA_CMD34 F22
FBA_CMD35 J22

For test/Debug only
+1.35VS_VGA
R7101 1 @ 2 60.4Ohm 1%
R7102 1 @ 2 60.4Ohm 1%

FBA_CLK0 D24 FBA_CLK0 76
FBA_CLK0_N D25 FBA_CLK0# 76
FBA_CLK1 N22 FBA_CLK1 76
FBA_CLK1_N M22 FBA_CLK1# 76

FBA_WCK01 D18 FBA_WCK01 76
FBA_WCK01_N C18 FBA_WCK01# 76
FBA_WCK23 D17 FBA_WCK23 76
FBA_WCK23_N D16 FBA_WCK23# 76
FBA_WCK45 T24 FBA_WCK45 76
FBA_WCK45_N U24 FBA_WCK45# 76
FBA_WCK67 V24 FBA_WCK67 76
FBA_WCK67_N V25 FBA_WCK67# 76

FB_PLL_AVDD_1 F16 +FB_PLL_AVDD
FB_PLL_AVDD_2 P22
FB_REFPLL_AVDD H22 +FB_REFPLL_AVDD_GPU

C7101 0.1UF/16V 10% /VGA
C7105 0.1UF/16V 10% /VGA
Place under GPU
C7104 0.1UF/16V 10% /VGA
C7103 0.1UF/16V @10% /VGA

R7110 1 2 0Ohm
R2_0
R7110, R7109
change to short pin
20170725
R7109 1 2 0Ohm

+FB_PLLVDD
B7101 1 /N17S 2 30Ohm/100Mhz vx_l0603_small
B7102 1 /N16S 2 30Ohm/100Mhz vx_l0603_small
C7102 22UF/6.3V /VGA
+1.8VS_MAIN_VGA
+PEX_VDD
Place near GPU

N17S-G1
/VGA
02T0A0002N00

GPU
OVERT
GPIO4
GPIO0
GPIO6
GPIO2
GPIO1
GPIO16
GPIO21
PEX_RST_N

Voltage Regulator Complex
EN
VDD_MAIN_EN
PWM_VID (NVVDD)
PSI (NVVDD)
GPU_EVENT#
GC6_FB_EN
GPU_PWR_EN
PGOOD

EC/PCH

R1 SYS_PEX_RST_MON#
R1 GPU_PEX_RST_HOLD#
U1
U2
R1
R2
GPU_RST#
PLATFORM_RST#
GPU_PEX_RST#

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PEGATRON
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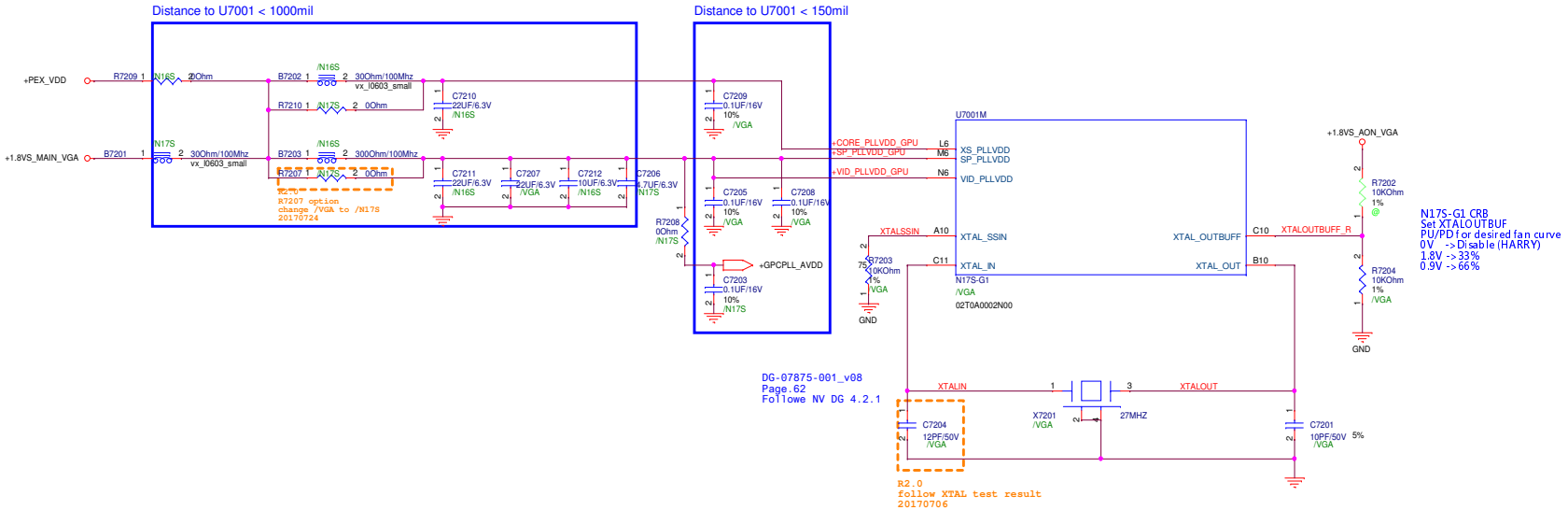
Title : VGA_FRAME BUFFER
Engineer: Raly_Hsieh
BG1/HW1
Size C | Project Name ER5EA | Rev 2.1
Date: Friday, January 19, 2018 | Sheet 71 of 103

VGA_XTAL

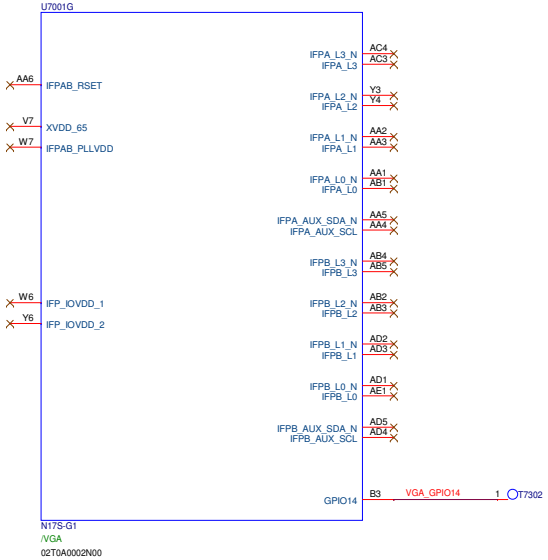
+1.8VS_AON_VGA
+1.8VS_MAIN_VGA
+PEX_VDD

+1.8VS_AON_VGA 57,70,74,75,87,90,91
+1.8VS_MAIN_VGA 57,70,71,74,75,91
+PEX_VDD 57,70,71,86



PEGATRON Title : VGA_XTAL
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Raly_Hsieh
BG1/HW1
Size C | Project Name ER5EA | Rev 2.1
Date: Friday, January 19, 2018 | Sheet 72 of 103

VGA_DISPLAY



DG 10.2.1 Table 10.2
GB2C-64 no display support

Table 10.2 GB2C-64 Standard Configurations

Link	Standard Display Configurations
Note: GPUs in GB2C-64 packages provide no display links and no display head support; they are operated in Optimus/MS-Hybrid mode. **Note:** GPUs in GB2C-64 packages do not support G-SYNC™.	

NVIDIA Corp 2017 -

PEGATRON Title : VGA_DISPLAY
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Raly_Hsieh
BG1/HW1
Size C | Project Name ER5EA | Rev 2.1
Date: Friday, January 19, 2018 | Sheet 73 of 103

VBIOS ROM / Straping

VGA_GPIO_STRAP

From RVL-07916-001_v09 Table.4

GB2C-64(N17S-G1)	Vendor	Strap	STRAP2	STRAP1	STRAP0
K4G80325FB-HC28	Samsung	0x0	L(R7416)	L(R7413)	L(R7404)
MT51J256M32HF-60:A	Micron	0x1	L(R7416)	L(R7413)	L(R7401)
H5GC8H24MJR-T2C	Hynix	0x2	L(R7416)	H(R7412)	L(R7404)
TBD	TBD	TBD			
TBD	TBD	TBD			
TBD	TBD	TBD			
TBD	TBD	TBD			
TBD	TBD	TBD			
TBD	TBD	TBD			

From RVL-07229-001_v14 Table.18

GB2B-64(N16S-GTR)	Vendor	Strap	ROM_SI
K4G80325FB-HC28	Samsung	0x0	L(R7430) 4.99K
MT51J256M32HF-60:A	Micron	0x1	L(R7430) 10K
H5GC8H24MJR-T2C	Hynix	0x2	L(R7430) 15K
TBD	TBD	0x5	
TBD	TBD	TBD	
TBD	TBD	TBD	
TBD	TBD	TBD	
TBD	TBD	TBD	
TBD	TBD	TBD	

N16S-GT-R Strap Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99K	1000	0000
10.0K	1001	0001
15.0K	1010	0010
20.0K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

For GB2B-64, GB4B-128, GB3B-256 Muti-Level modeStrapping (From DG-07158-001_v05 Table.15-3)

N16S-GTR	Multi-Level Mode Strapping			
Resistor Values	Bit3	Bit2	Bit1	Bit0
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kohm pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			
STRAP2				
STRAP3				
STRAP4				
ROM_SCLK	SOR3_EXPOSED 0	SOR2_EXPOSED 0	SOR1_EXPOSED 0	SOR0_EXPOSED 0
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL 0	PCIE_CFG 0	SMB_ALT_ADDR 0	VGA_DEVICE 0

GPIO

AON_PWR Select resistor

For reduce the power select resistor.
Fenix 20170510

AC_BATT#

GPIO1_GC6FBEN

GPIO1_GC6FBEN (to PCH)

N17S GPIO PU 1.8V

N16S GPIO PU 3.3V

N17S/N16S GPIO Common PU Power

GPU_EVENT#

1V8S_AON_VGA_EN

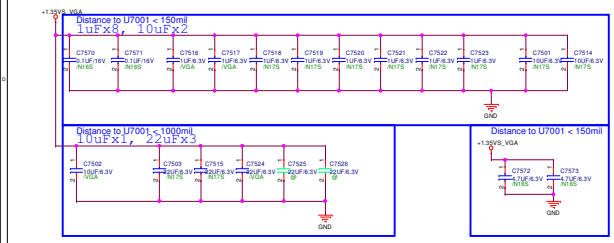
1V8S_MAIN_VGA_EN

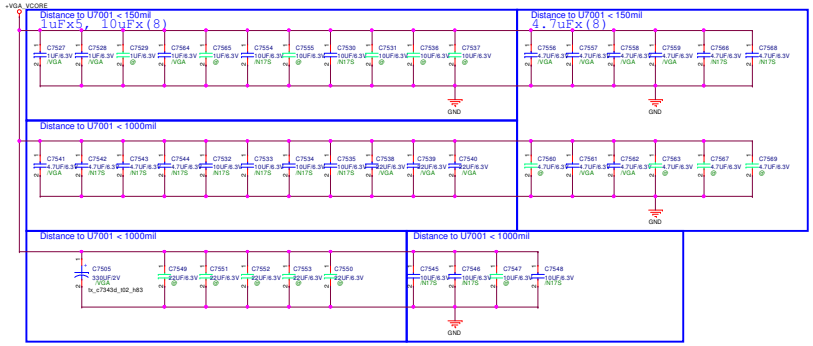
PEX_VDD_EN

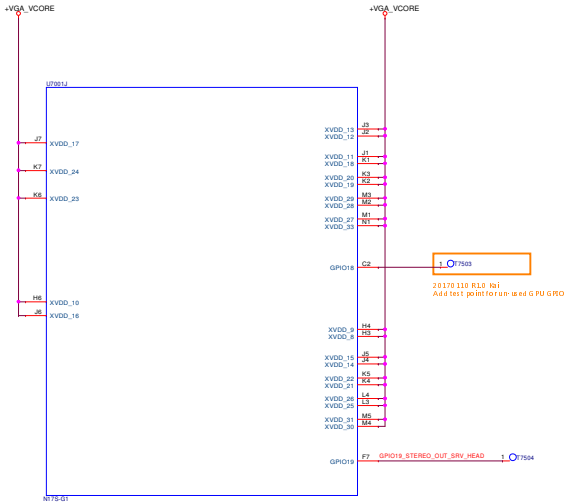
GPIO8 MEM_VDD_CTL

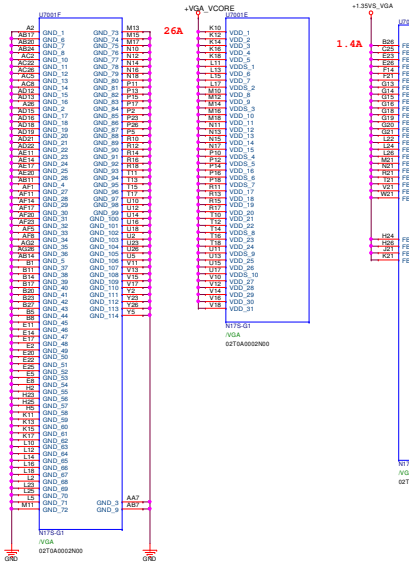
PEGATRON Title : VGA_GPIO_STRAP
Engineer: Raily_Hsieh
Size: D | Project Name: ER58A | Rev: X1
Date: Friday, January 19, 2018 | Sheet 74 of 103

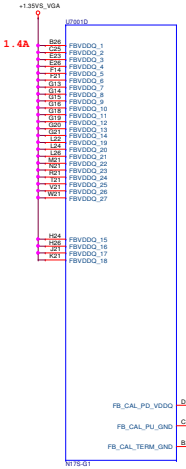
VGA_Power

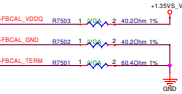


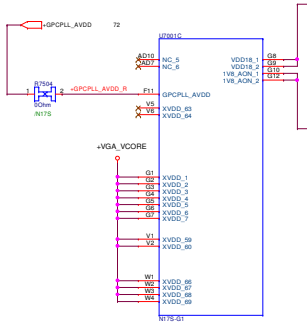


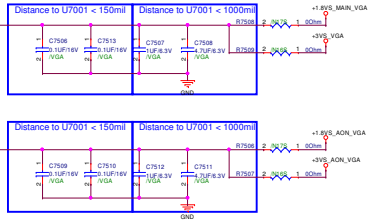


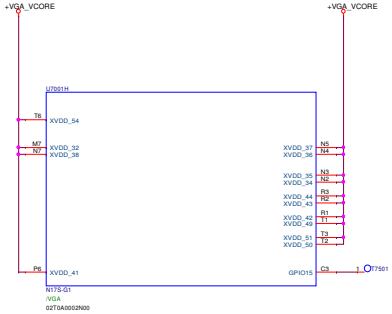


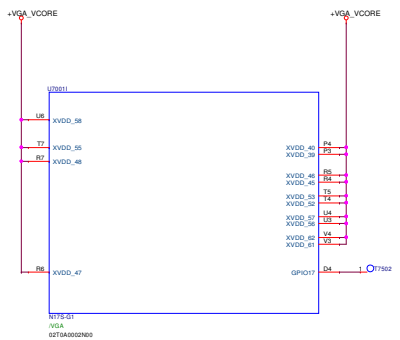












PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : VGA_Power

Engineer: Raily_Hsieh

Size	Project Name	Rev
D	ER5EA	X1

Date: Friday, January 19, 2018 Sheet 75 of 165

VGA_FBA_GDDR5

nVidia Design Guide
DG-07875-001_v08 P.154
Table 9.5

	LOWER 0.35	UPPER 32.40
CA0	CA	
CA1	40.82Ω	
CA2	40.82Ω	
CA3	40.82Ω	
CA4	40Ω	
CA5	40.2Ω	
CA6	40.2Ω	
CA7	40.2Ω	
CA8	40.2Ω	
CA9	40Ω	
CA10	CKE	
CA11	40.82Ω	
CA12	40.82Ω	
CA13	40.82Ω	
CA14	40.82Ω	
CA15	40Ω	
CA16	CS	
CA17	CA	

3 : 24 ~ 31
2 : 16 ~ 23
1 : 8 ~15
0 : 0 ~ 7

M1

U7601 — K4G80325FB-HC03

7 : 56 ~ 63
6 : 48 ~ 55
5 : 40 ~ 47
4 : 32 ~ 39

M2

U7600 — K4G80325FB-HC03

Non-Mirrored

Non-Mirrored

Place near U7601

Place around U7601

Place below decoupling caps close VDD pin.
(Spare Capacitors)

Place near U7602

Place around U7602

Place below decoupling caps close VDD pin.
(Spare Capacitors)

20170216 R1.0 Gary
FAE suggest follow VRAM lacut rule
Every SEN pin individual pull low
Add R7698 & R7699

20170216 R1.0 Gary
FAE request follow N17S-G1 CRB

Project Code	9MS1M0010
Engineer	Raly_Hsieh
Size	D
Project Name	ER5EA
Rev	X1
Date	Friday, January 19, 2018
Sheet	76 of 165

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : VGA_FBA_GDDR5-1

PEGATRON Title : VGA_FBA_GDDR5-2

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: *Raly_Hsieh*

BG1/HW1

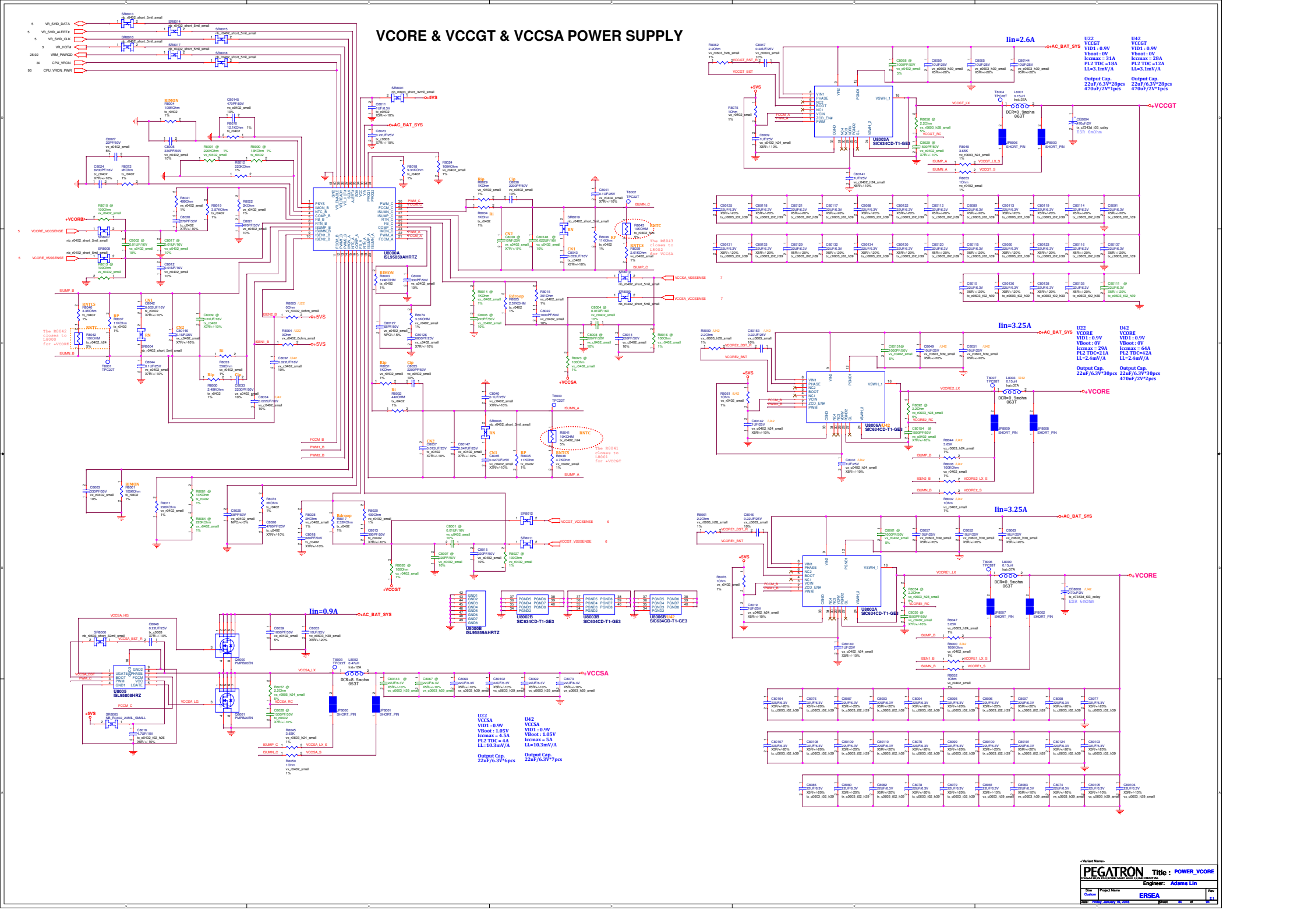
Size	Project Name	Rev
C	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 77 of 103

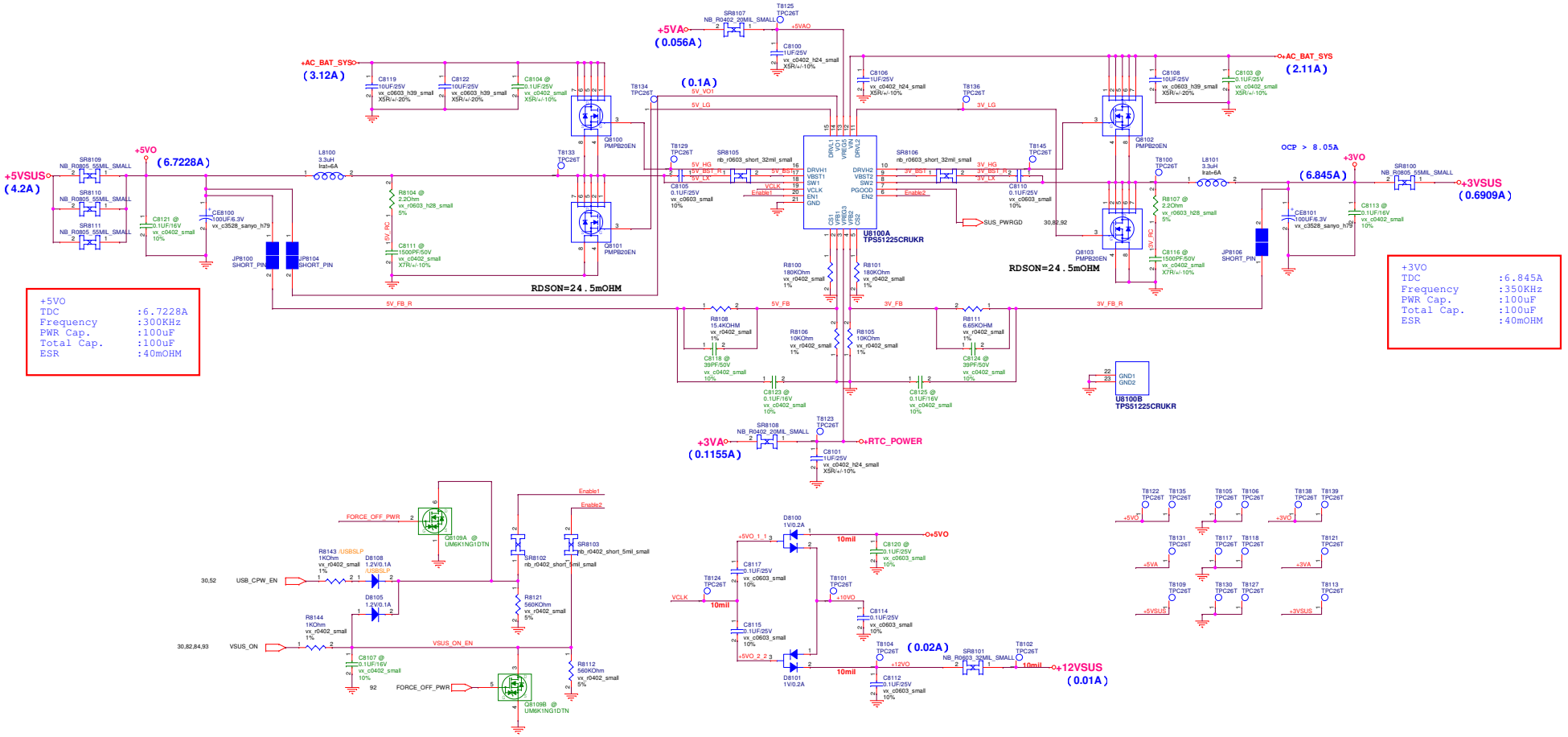
Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 78 of 103

Title	<Title>
Size: A	Document Number: ER5EA
Rev: 2.1	
Date: Friday, January 19, 2018	Sheet 79 of 103

VCORE & VCCGT & VCCSA POWER SUPPLY

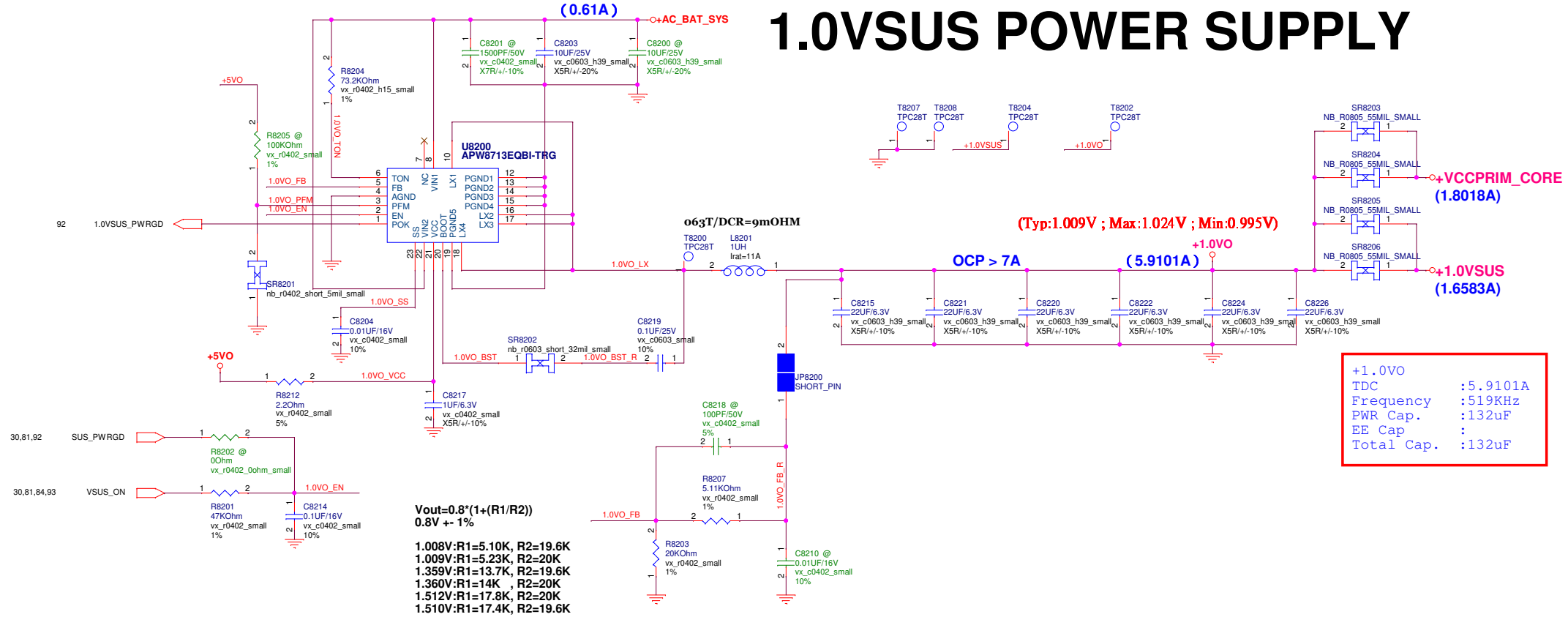


5VO & 3VO POWER SUPPLY



PEGATRON	Title : POWER_SYSTEM	
PEGATRON PROPRIETARY AND CONFIDENTIAL	Engineer: Adams Lin	
PG1-POWER		
Size: Custom	Project Name: ER5EA	Rev: 0.1
Date: Friday, January 19, 2018	Sheet 81 of 94	

1.0VSUS POWER SUPPLY

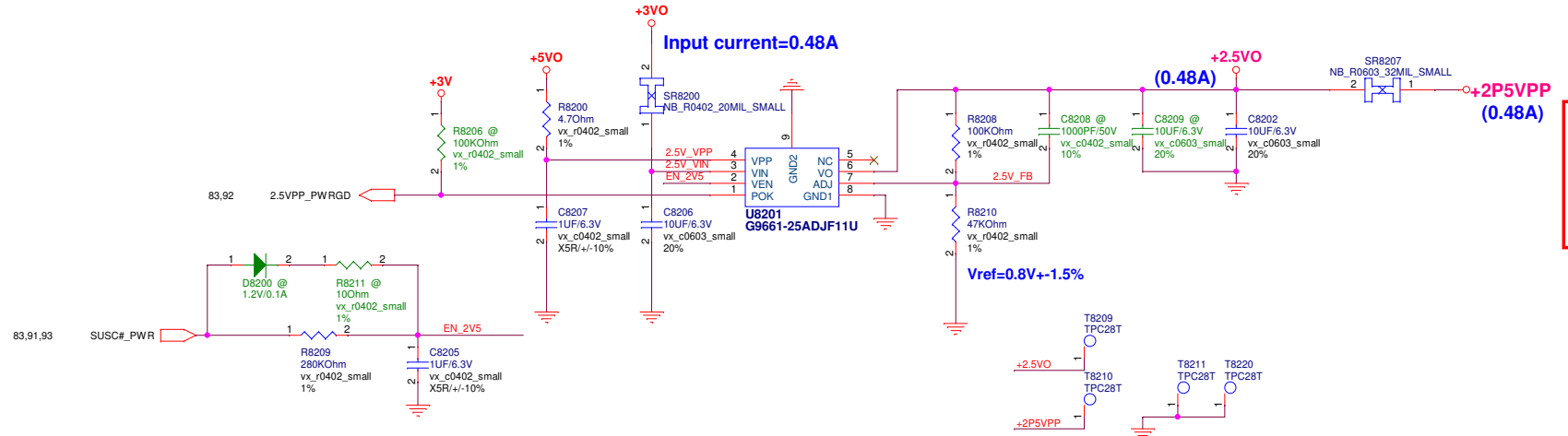


Vout=0.8*(1+(R1/R2))
0.8V +- 1%

1.008V:R1=5.10K, R2=19.6K
1.009V:R1=5.23K, R2=20K
1.359V:R1=13.7K, R2=19.6K
1.360V:R1=14K , R2=20K
1.512V:R1=17.8K, R2=20K
1.510V:R1=17.4K, R2=19.6K

+1.0VO	
TDC	:5.9101A
Frequency	:519KHz
PWR Cap.	:132uF
EE Cap	:
Total Cap.	:132uF

2.5V POWER SUPPLY



+2.5VO	
TDC	:0.48A
OCP	:3A
PWR Cap.	:20uF
EE Cap.	:10uF
Total Cap.	:30uF

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

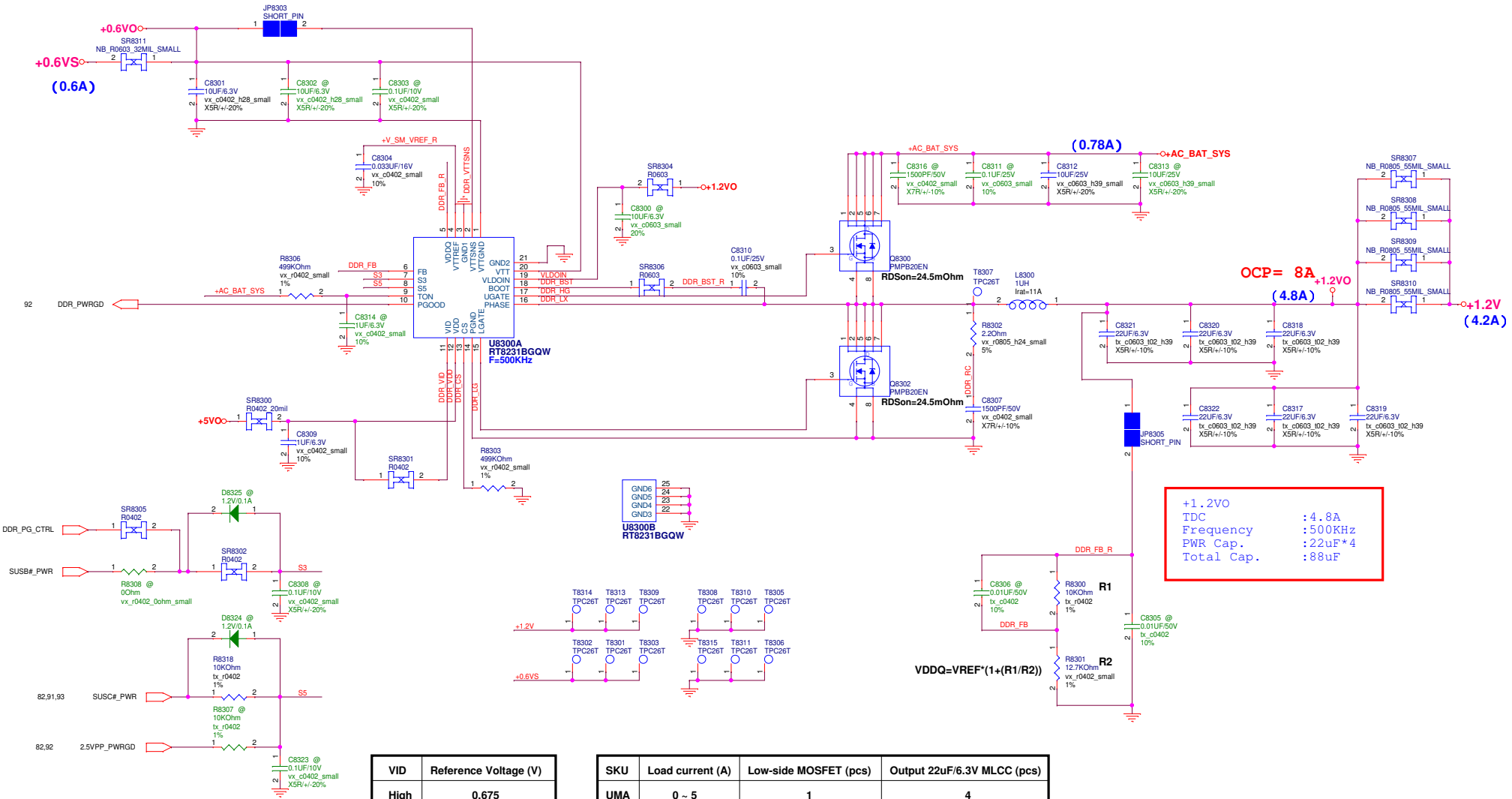
Title : P82_+1.0VSUS & +2.5V

Engineer: Adams Lin

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 82 of 94

DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_DDR & VTT

Engineer: Adams Lin

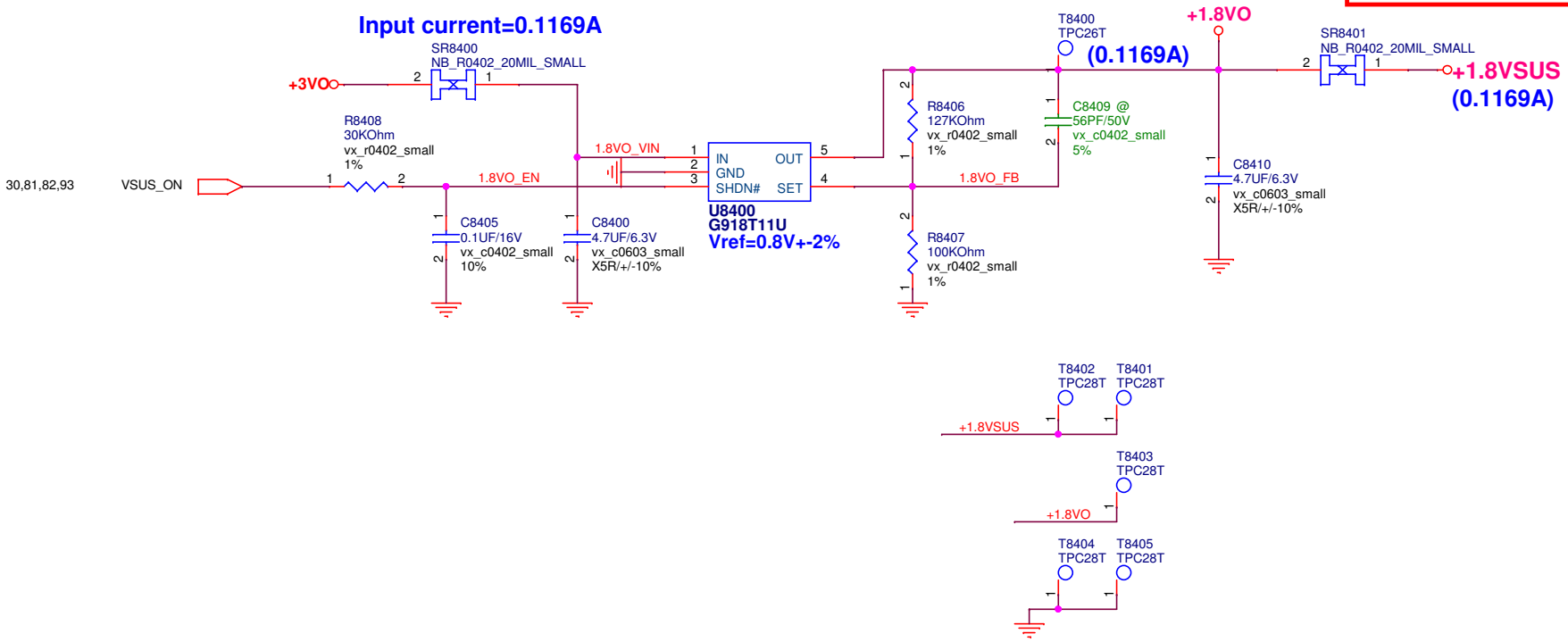
BG1-POWER

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 83 of 94

1.8VSUS POWER SUPPLY

+1.8VO
MAX current :0.1169A
PWR Cap. :20uF
Total Cap. :20uF



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

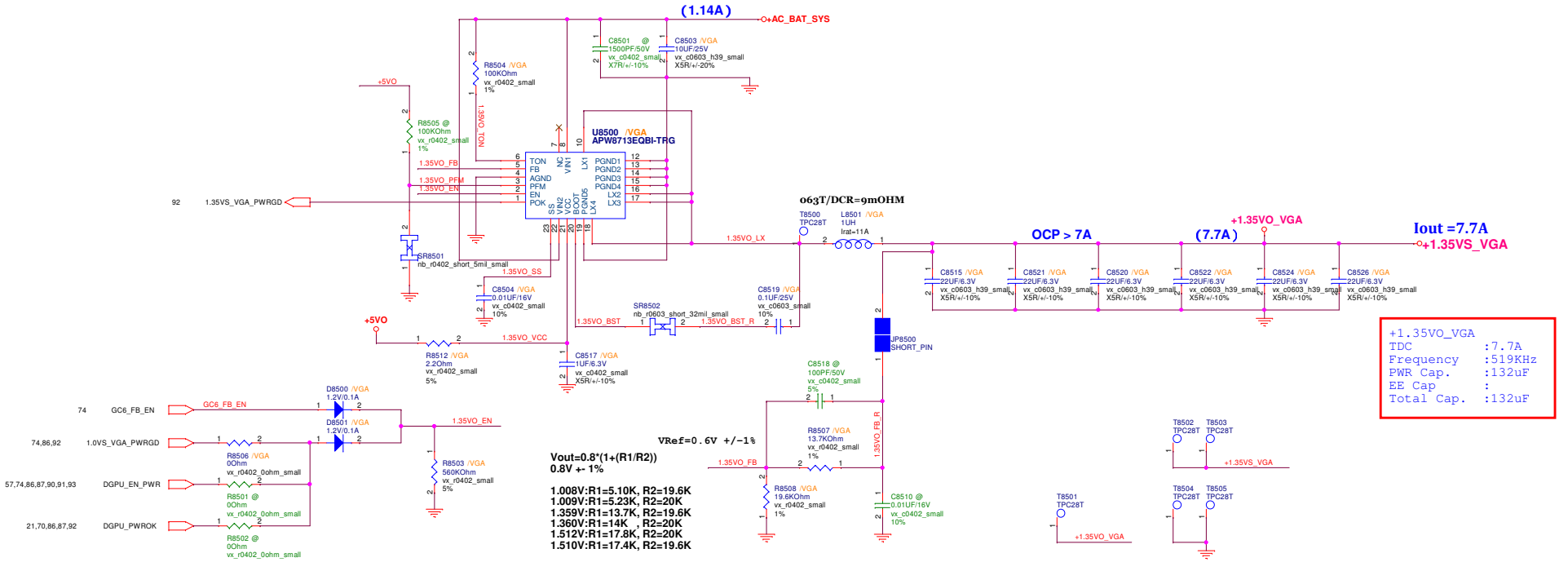
Title : POWER_+1.8VSUS

Engineer: Adams Lin

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 84 of 94

1.35VS_VGA POWER SUPPLY



+1.35VO_VGA
TDC :7.7A
Frequency :519KHz
PWR Cap. :132uF
EE Cap :
Total Cap. :132uF

<Variant Name>

PEGATRON Title : POWER_1.35VS_VGA

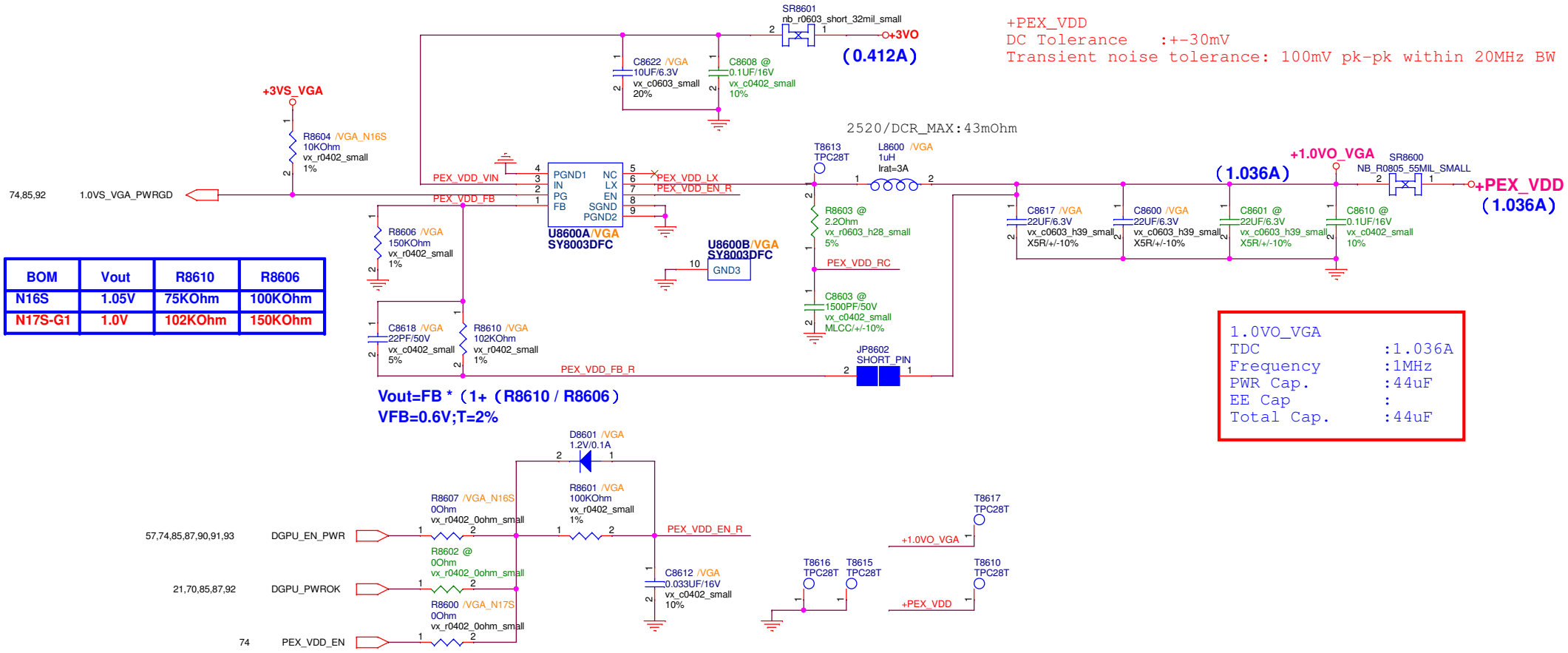
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 85 of 94

1.0VO_VGA POWER SUPPLY



BOM	Vout	R8610	R8606
N16S	1.05V	75KOhm	100KOhm
N17S-G1	1.0V	102KOhm	150KOhm

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Power_PEX_VDD

Engineer: Adams Lin

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 86 of 94

VGA_CORE POWER SUPPLY

	N17S_G1
R8723	6.19K
R8721	20.5K
R8716	4.32K
R8715	16.5K
R8713	309
C8720	4.7nF
Vstep	6.25mV
Vmin	0.3V
Vmax	1.3V
Vboot	0.8V

VGA_PSI#	VO_action
~ 0.4V	1 Phase DEM
0.7 ~ 0.88V	1 Phase FCCM
1.08 ~ 1.35V	2 Phase FCCM
1.6V ~	2 Phase FCCM

+VGA_VCORE(Package type:N17VS-G1)
DC Tolerance :+-20mV

Overshoot/undershoot
Transient noise tolerance: -10% ~ +20% within 20MHz BW
High frequency noise: 400mV pk-pk within 1GHz BW

VID:0.6V ~ 1.2V
Number of programmable Volt: 96 levels
Programmable volt steps: 6.25mV
Settling Time: < 100us for rising, no restriction on falling

RT8812AGQW
06V950000023
0695-00F8000
for N16S

U8700A/VGA
RT8816AGQW

U8700B/VGA
RT8816AGQW

103T

(2A)

(27.9A)

2 PHASE 25W
N17S-G1
TDC=27.9A
OCP:62A

+VGA_VCORE (2 Phase)
TDC :27.9A
Frequency :305KHz
PWR Cap. :940uF
EE Cap. :139.5uF
Total Cap. :1079.5uF
ESR :3mOHM

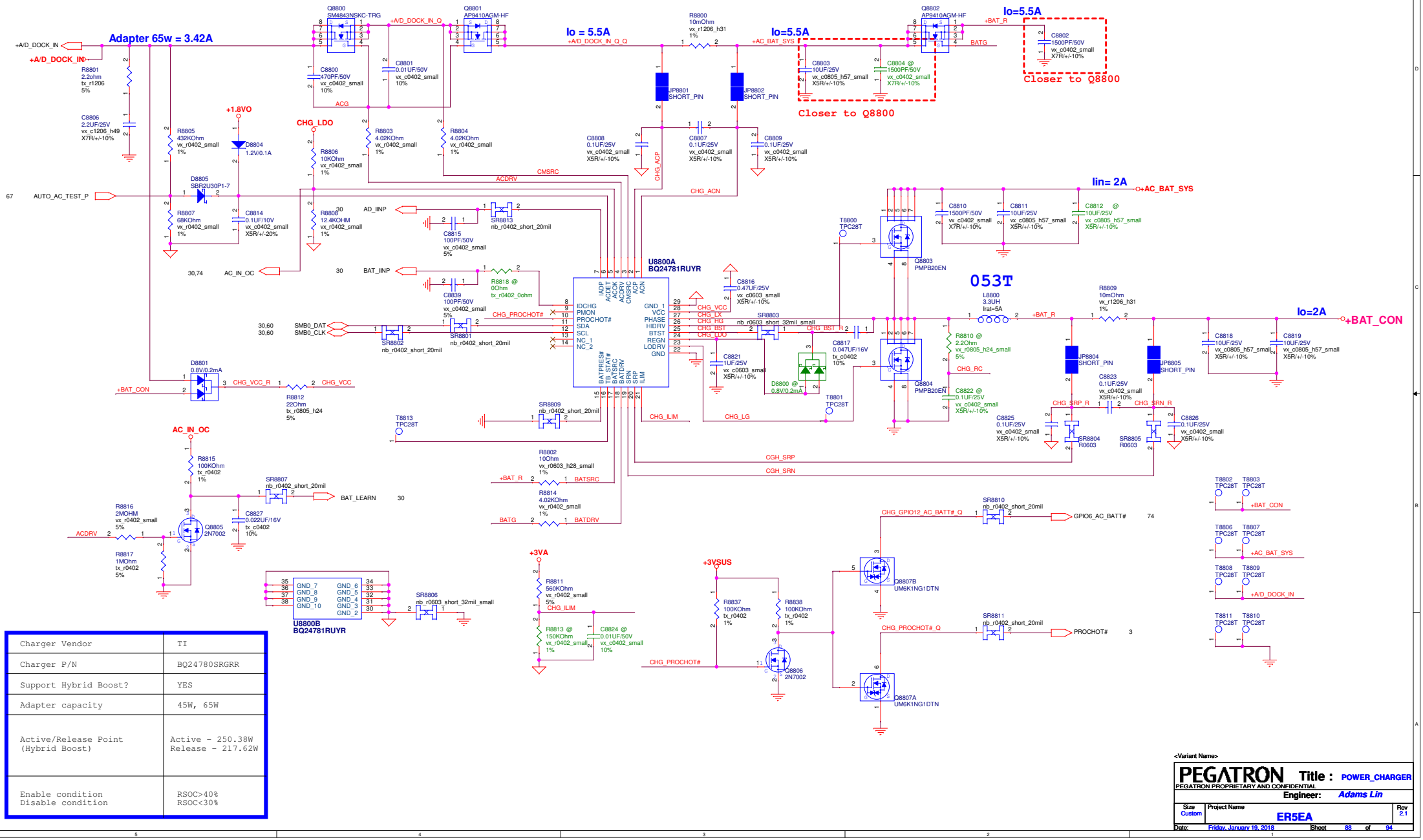
<Variant Name>

PEGATRON Title : VGA_VCORE
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Adams Lin

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 87 of 94

BATTERY CHARGER



Charger Vendor	TI
Charger P/N	BQ24780SRGRR
Support Hybrid Boost?	YES
Adapter capacity	45W, 65W
Active/Release Point (Hybrid Boost)	Active - 250.38W Release - 217.62W
Enable condition Disable condition	RSOC>40% RSOC<30%

<Variant Name>

PEGATRON Title : POWER_CHARGER

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

Size: Custom | Project Name: ER5EA | Rev: 2.1

Date: Friday, January 19, 2018 | Sheet 88 of 94

<variant_name><Variant Name></variant_name>

PEGATRON Title : ***

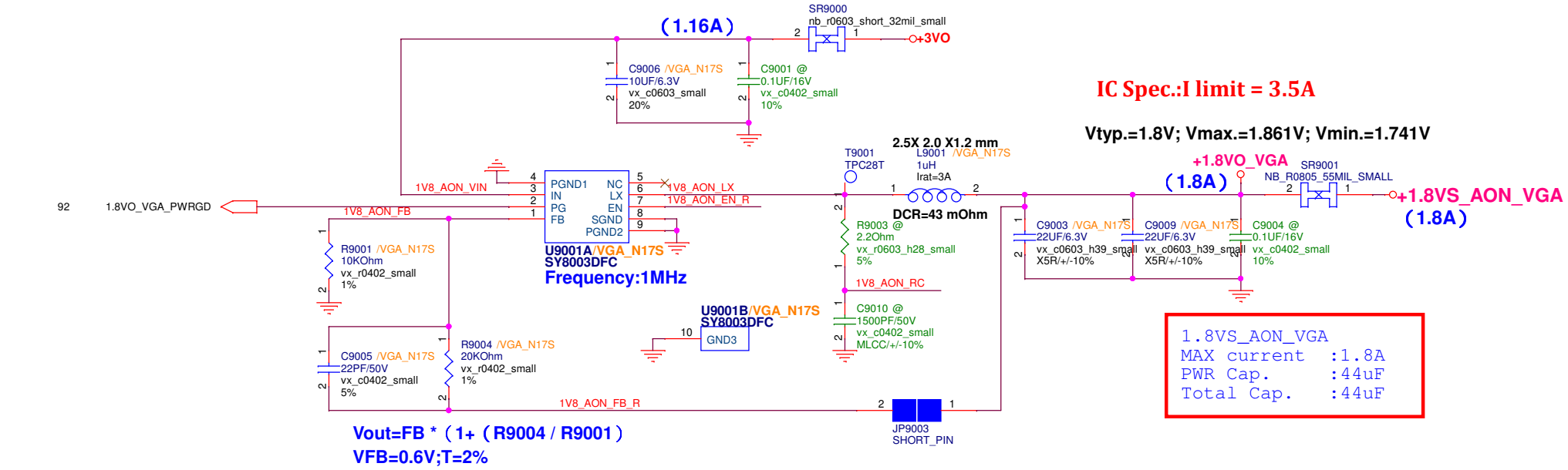
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

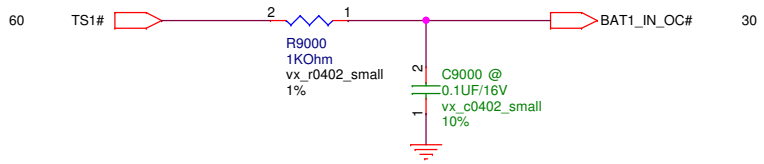
Size	Project Name	Rev
A	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 89 of 94

1V8_AON POWER SUPPLY



BATTERY IN DETECT



<Variant Name>

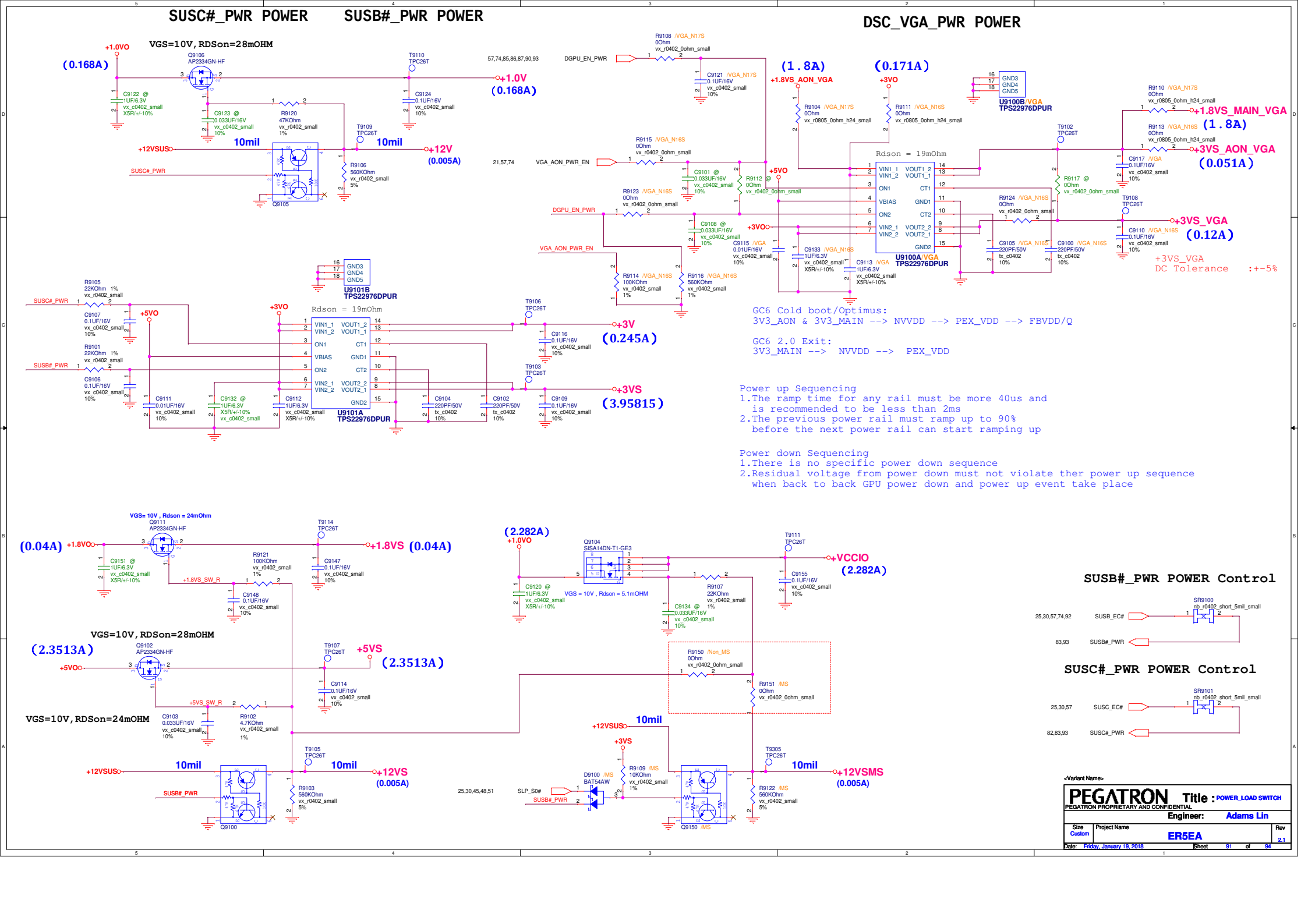
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : 1V8_AON & DETECT

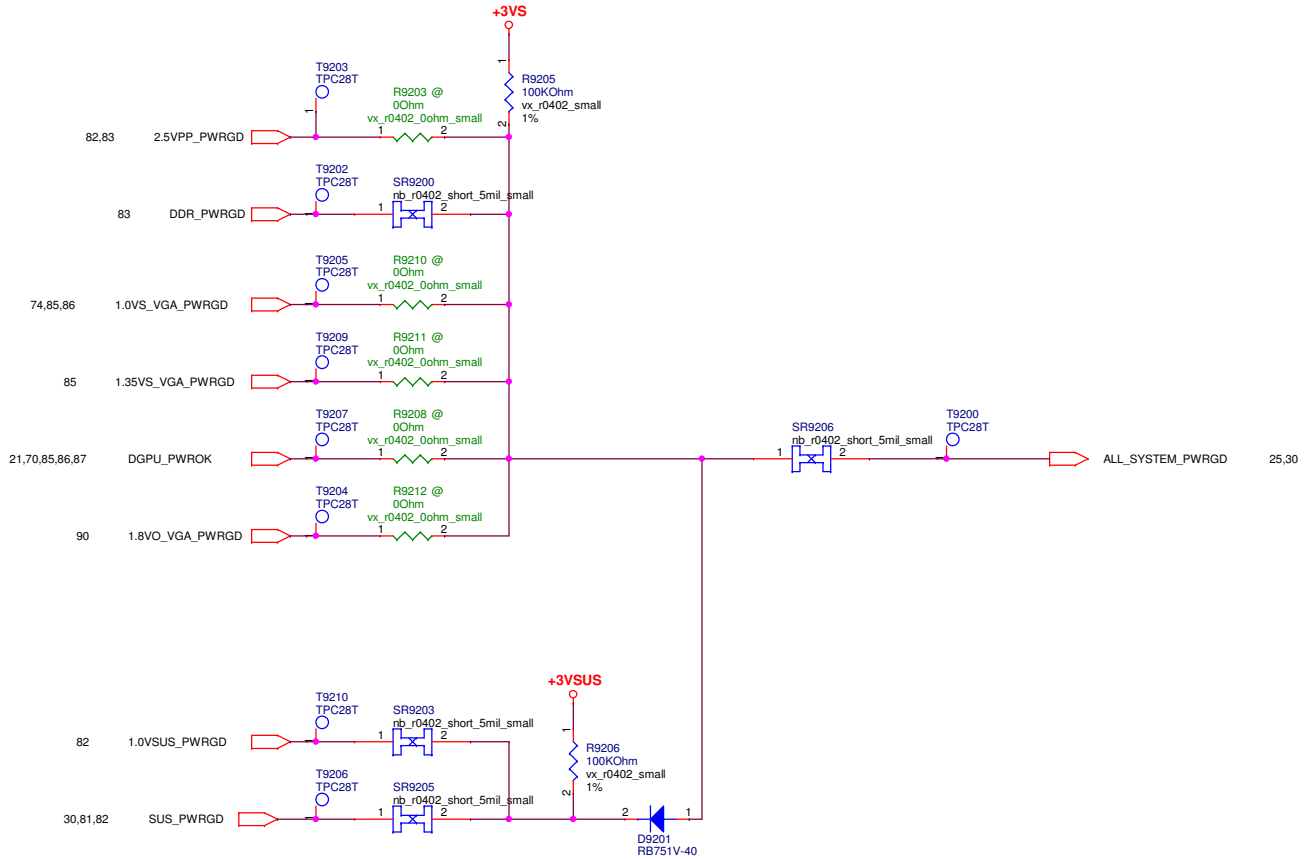
Engineer: Adams Lin

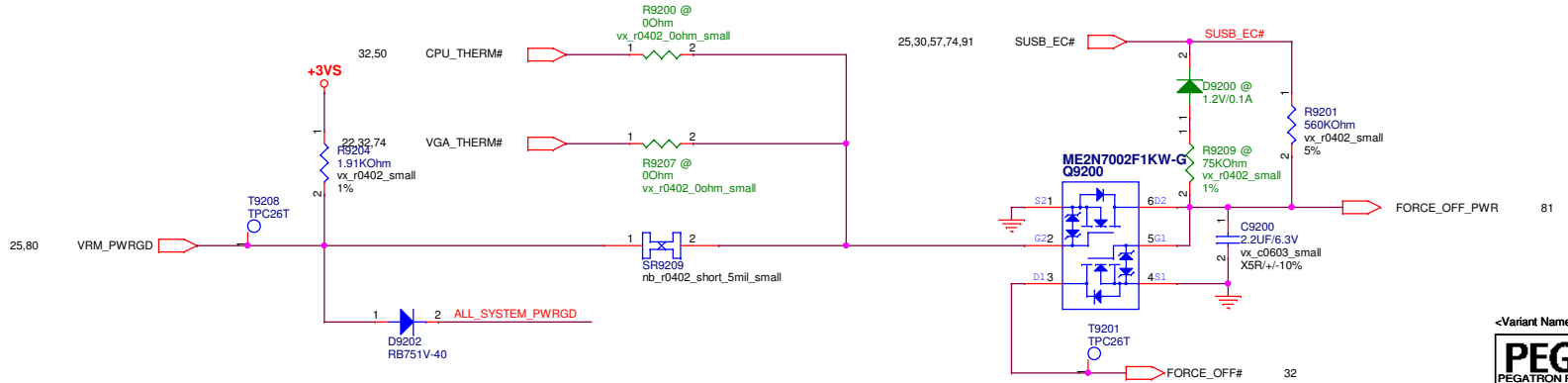
Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 90 of 94


SUSC#_PWR POWER
SUSB#_PWR POWER
DSC_VGA_PWR POWER
VGS=10V, RDSon=28mOHM
(0.168A)
+1.0VO
Q9106
AP2334GN-HF
T9110
TPC26T
+1.0V
(0.168A)
C9122 @
1UF/6.3V
vx_c0402_small
X5R/+/-10%
C9123 @
0.033UF/16V
vx_c0402_small
10%
R9120
47KOhm
vx_r0402_small
1%
C9124
0.1UF/16V
vx_c0402_small
10%
T9109
TPC26T
10mil
10mil
+12VSUS
+12V
(0.005A)
SUSC#_PWR
R9106
560KOhm
vx_r0402_small
5%
Q9105
R9108 /VGA_N17S
0Ohm
vx_r0402_0ohm_small
57,74,85,86,87,90,93
DGPU_EN_PWR
C9121 /VGA_N17S
0.1UF/16V
vx_c0402_small
10%
(1.8A)
(0.171A)
+1.8VS_AON_VGA
+3VO
R9104 /VGA_N17S
0Ohm
vx_r0805_0ohm_h24_small
R9111 /VGA_N16S
0Ohm
vx_r0805_0ohm_h24_small
GND3
GND4
GND5
U9100B/VGA
TPS22976DPUR
R9110 /VGA_N17S
0Ohm
vx_r0805_0ohm_h24_small
+1.8VS_MAIN_VGA
(1.8A)
R9113 /VGA_N16S
0Ohm
vx_r0805_0ohm_h24_small
+3VS_AON_VGA
(0.051A)
R9115 /VGA_N16S
0Ohm
vx_r0402_0ohm_small
21,57,74
VGA_AON_PWR_EN
C9101 @
0.033UF/16V
vx_c0402_small
10%
R9112 @
0Ohm
vx_r0402_0ohm_small
+5VO
Rdson = 19mOhm
VIN1_1
VIN1_2
ON1
VBIAS
ON2
VIN2_1
VIN2_2
VOUT1_2
VOUT1_1
CT1
GND1
CT2
VOUT2_2
VOUT2_1
GND2
U9100A/VGA
TPS22976DPUR
R9123 /VGA_N16S
0Ohm
vx_r0402_0ohm_small
DGPU_EN_PWR
C9108 @
0.033UF/16V
vx_c0402_small
10%
+3VO
C9115 /VGA
0.01UF/16V
vx_c0402_small
10%
C9133 /VGA_N16S
1UF/6.3V
vx_c0402_small
X5R/+/-10%
C9113 /VGA
1UF/6.3V
vx_c0402_small
X5R/+/-10%
R9124 /VGA_N16S
0Ohm
vx_r0402_0ohm_small
R9117 @
0Ohm
vx_r0402_0ohm_small
T9102
TPC26T
T9108
TPC26T
C9117 /VGA
0.1UF/16V
vx_c0402_small
10%
C9110 /VGA_N16S
0.1UF/16V
vx_c0402_small
10%
+3VS_VGA
(0.12A)
C9105 /VGA_N16S
220PF/50V
tx_c0402
10%
C9100 /VGA_N16S
220PF/50V
tx_c0402
10%
+3VS_VGA
DC Tolerance :+-5%
VGA_AON_PWR_EN
R9114 /VGA_N16S
100KOhm
vx_r0402_small
1%
R9116 /VGA_N16S
560KOhm
vx_r0402_small
1%
R9105
22KOhm 1%
vx_r0402_small
SUSC#_PWR
C9107
0.1UF/16V
vx_c0402_small
10%
R9101
22KOhm 1%
vx_r0402_small
SUSB#_PWR
C9106
0.1UF/16V
vx_c0402_small
10%
+5VO
+3VO
Rdson = 19mOhm
U9101B
TPC26T
U9101A
TPC26T
T9106
TPC26T
+3V
(0.245A)
C9116
0.1UF/16V
vx_c0402_small
10%
T9103
TPC26T
+3VS
(3.95815)
C9111
0.01UF/16V
vx_c0402_small
10%
C9132 @
1UF/6.3V
X5R/+/-10%
vx_c0402_small
C9112
1UF/6.3V
vx_c0402_small
X5R/+/-10%
C9104
220PF/50V
tx_c0402
10%
C9102
220PF/50V
tx_c0402
10%
C9109
0.1UF/16V
vx_c0402_small
10%
GC6 Cold boot/Optimus:
3V3_AON & 3V3_MAIN --> NVVDD --> PEX_VDD --> FBVDD/Q
GC6 2.0 Exit:
3V3_MAIN --> NVVDD --> PEX_VDD
Power up Sequencing
1.The ramp time for any rail must be more 40us and
is recommended to be less than 2ms
2.The previous power rail must ramp up to 90%
before the next power rail can start ramping up
Power down Sequencing
1.There is no specific power down sequence
2.Residual voltage from power down must not violate ther power up sequence
when back to back GPU power down and power up event take place
VGS= 10V , Rdson = 24mOhm
Q9111
AP2334GN-HF
(0.04A)
+1.8VO
T9114
TPC26T
+1.8VS
(0.04A)
C9151 @
1UF/6.3V
vx_c0402_small
X5R/+/-10%
R9121
100KOhm
vx_r0402_small
1%
+1.8VS_SW_R
C9147
0.1UF/16V
vx_c0402_small
10%
C9148
0.1UF/16V
vx_c0402_small
10%
VGS=10V, RDSon=28mOHM
(2.3513A)
Q9102
AP2334GN-HF
+5VO
T9107
TPC26T
+5VS
(2.3513A)
C9114
0.1UF/16V
vx_c0402_small
10%
+5VS_SW_R
VGS=10V, RDSon=24mOHM
C9103
0.033UF/16V
vx_c0402_small
10%
R9102
4.7KOhm
vx_r0402_small
1%
10mil
10mil
+12VSUS
+12VS
(0.005A)
SUSB#_PWR
T9105
TPC26T
R9103
560KOhm
vx_r0402_small
5%
Q9100
(2.282A)
+1.0VO
Q9104
SISA14DN-T1-GE3
T9111
TPC26T
+VCCIO
(2.282A)
C9120 @
1UF/6.3V
vx_c0402_small
X5R/+/-10%
VGS = 10V , Rdson = 5.1mOHM
C9155
0.1UF/16V
vx_c0402_small
10%
R9107
22KOhm
vx_r0402_small
1%
C9134 @
0.033UF/16V
vx_c0402_small
10%
R9150 /Non_MS
0Ohm
vx_r0402_0ohm_small
R9151 /MS
0Ohm
vx_r0402_0ohm_small
10mil
+12VSUS
+3VS
R9109 /MS
10KOhm
vx_r0402_small
1%
D9100 /MS
BAT54AW
25,30,45,48,51
SLP_S0#
SUSB#_PWR
T9305
TPC26T
10mil
+12VSMS
(0.005A)
R9122 /MS
560KOhm
vx_r0402_small
5%
Q9150 /MS
SUSB#_PWR POWER Control
SR9100
nb_r0402_short_5mil_small
25,30,57,74,92
SUSB_EC#
83,93
SUSB#_PWR
SUSC#_PWR POWER Control
SR9101
nb_r0402_short_5mil_small
25,30,57
SUSC_EC#
82,83,93
SUSC#_PWR
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : POWER_LOAD SWITCH
Engineer: Adams Lin
Size
Custom
Project Name
ER5EA
Rev
2.1
Date: Friday, January 19, 2018
Sheet 91 of 94

POWER GOOD DETECTER





<Variant Name>

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PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_PROTECT

Engineer: Adams Lin

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 92 of 94

+A/D_DOCK_IN → +A/D_DOCK_IN 60,88

+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,82,83,85,87,88

+BAT_CON → +BAT_CON 60,88

+RTC_POWER → +RTC_POWER 81

+5VA → +5VA 64,81

+3VA → +3VA 24,28,30,31,36,57,67,81,88

+5VO → +5VO 81,82,83,85,91

+3VO → +3VO 81,82,84,86,90,91

+2.5VO → +2.5VO 82

+1.8VO → +1.8VO 84,88,91

+1.8VO_VGA → +1.8VO_VGA 90

+1.35VO_VGA → +1.35VO_VGA 57,71,75,76,85

+1.2VO → +1.2VO 83

+1.0VO → +1.0VO 82,91

+1.0VO_VGA → +1.0VO_VGA 86

+0.6VO → +0.6VO 83

+12VSUS → +12VSUS 81,91

+5VSUS → +5VSUS 41,52,64,81

+3VSUS → +3VSUS 4,20,21,22,23,24,25,26,28,30,41,42,62,67,74,81,88,92

+1.8VSUS → +1.8VSUS 9,24,26,84

+1.0VSUS → +1.0VSUS 26,82

+12V → +12V 57,91

+2P5VPP → +2P5VPP 16,17,28,57,82

+1.2V → +1.2V 4,7,16,17,18,57,83

+1.0V → +1.0V 3,5,7,9,25,32,57,91

+12VS → +12VS 28,31,57,91

+5VS → +5VS 31,36,48,50,51,57,69,80,87,91

+3VS → +3VS 3,4,20,21,23,24,25,30,32,36,41,44,45,46,50,51,57,62,64,67,74,87,91,92

+1.8VS → +1.8VS 36,57,91

+0.6VS → +0.6VS 16,17,57,83

+VCORE → +VCORE 5,6,80

+VCCGT → +VCCGT 6,80

+VCCSA → +VCCSA 7,80

+VCCIO → +VCCIO 3,5,7,9,57,91

+VCCPRIM_CORE → +VCCPRIM_CORE 26,82

+VGA_VCORE → +VGA_VCORE 57,75,87

FOR POWER TEST

+3VA

JP9300 SGL_JUMP (1 2) → T9300 TPC28T → CPU_VRON_PWR 80

JP9301 SGL_JUMP (1 2) → T9301 TPC28T → SUSB#_PWR 83,91

JP9302 SGL_JUMP (1 2) → T9302 TPC28T → SUSC#_PWR 82,83,91

JP9303 SGL_JUMP (1 2) → T9303 TPC28T → VSUS_ON 30,81,82,84

JP9304 SGL_JUMP (1 2) → T9304 TPC28T → DGPU_EN_PWR 57,74,85,86,87,90,91

+3VS_AON_VGA → +3VS_AON_VGA 57,70,74,75,91

+3VS_VGA → +3VS_VGA 57,70,74,75,86,87,91

+1.8VS_AON_VGA → +1.8VS_AON_VGA 57,70,72,74,75,87,90,91

+1.8VS_MAIN_VGA → +1.8VS_MAIN_VGA 57,70,71,72,74,75,91

+1.35VS_VGA → +1.35VS_VGA 57,71,75,76,85

+PEX_VDD → +PEX_VDD 57,70,71,72,86

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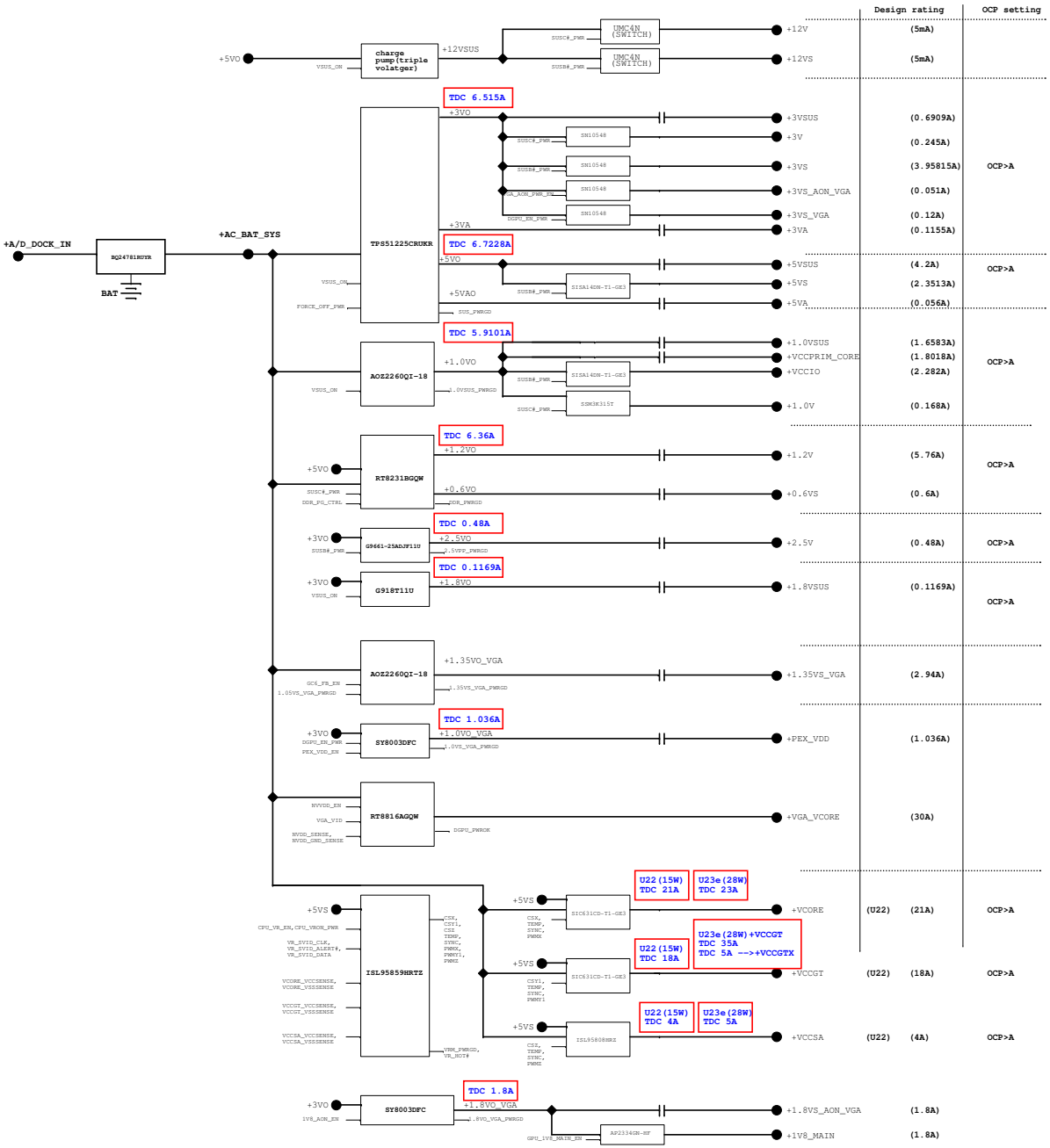
Title : POWER_SIGNAL

BG1-POWER

Engineer: Adams Lin

Size	Project Name	Rev
Custom	ER5EA	2.1

Date: Friday, January 19, 2018 Sheet 93 of 94



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PEGATRON PROPRIETARY AND CONFIDENTIAL

Title :POWER_FLOWCHART

Engineer: Adams Lin

Project Name: ERSEA

Rev: 0.1

Date: January 19, 2018

Sheet 50 of 50