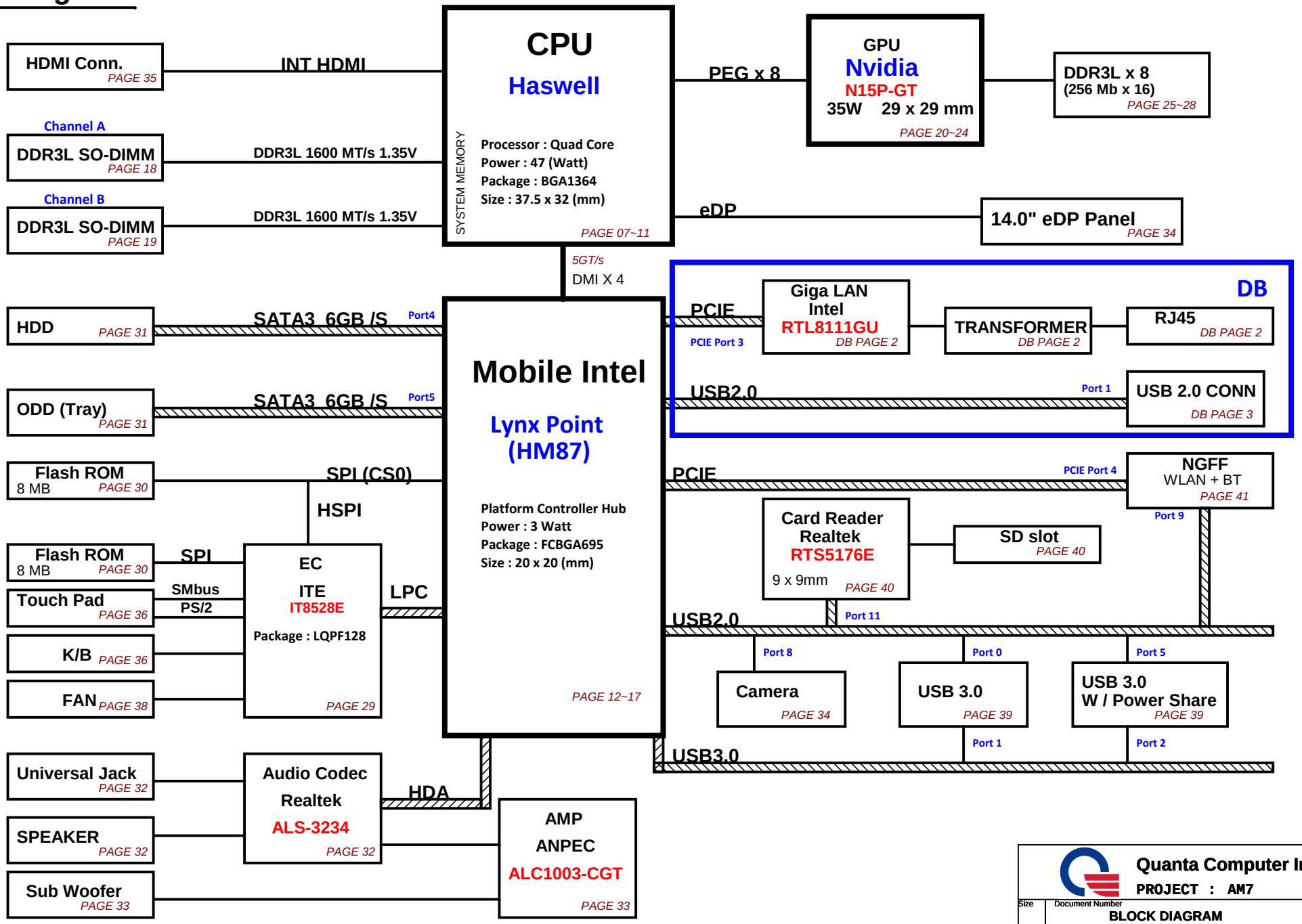
01

Project : AM7 (14.0") MB Schematic

PCB Rev: C0
Build: DVT2

Block Diagram



Quanta Computer Inc.
PROJECT : AM7

Size	Document Number	Rev
	BLOCK DIAGRAM	C0

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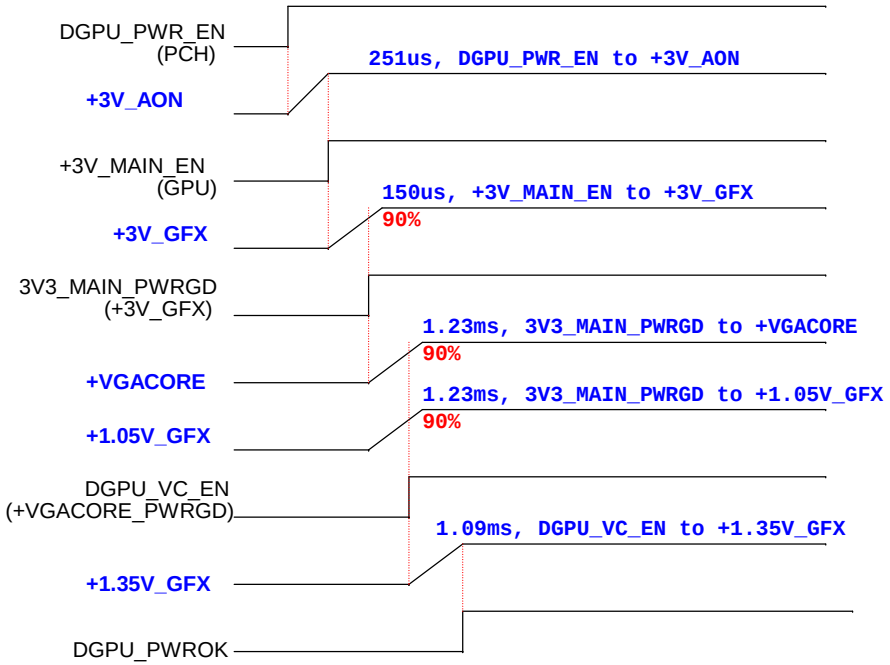
AM7 GPU Power UP sequence

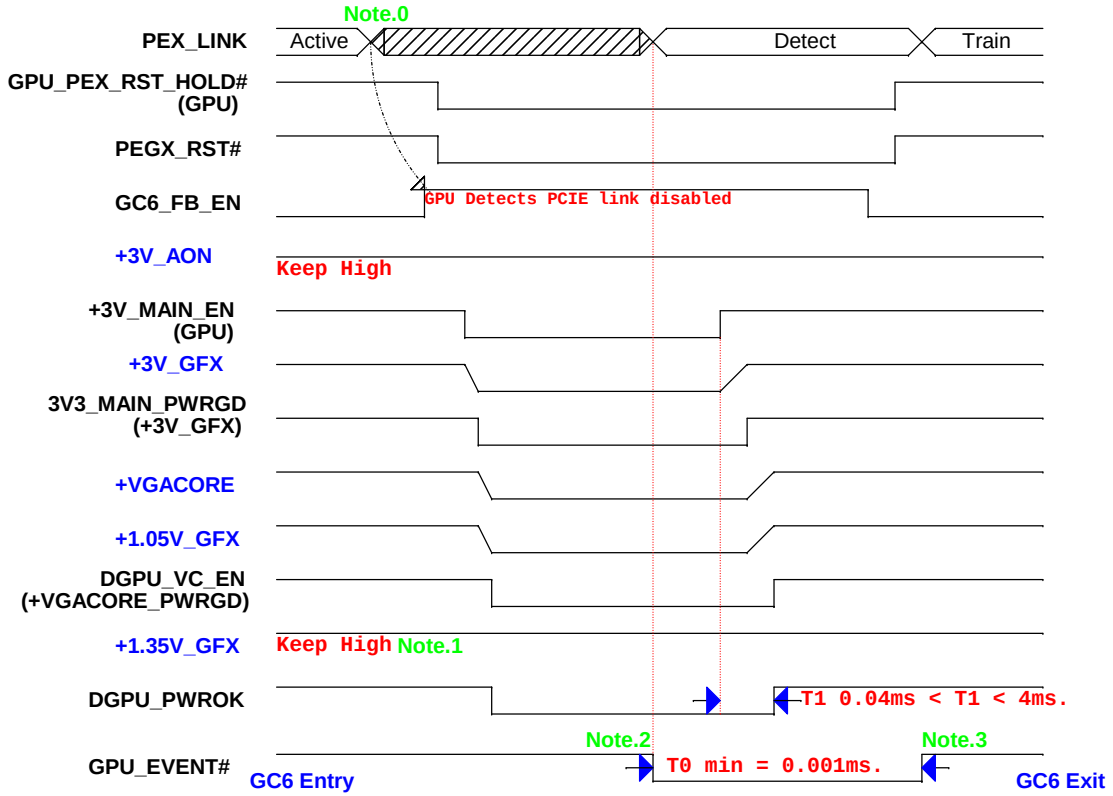


- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- A VDD33 must ramp up to 90% before NVVDD and PEXVDD in sequence can start ramping up. NVVDD must ramp up to 90% before FBVDD/Q in sequence can start ramping up

3.10.2.2 Power-Down Sequence

There is no specific power down sequence required. However, residual voltage from power down should not disrupt the power-up sequence when back to back GPU power-down and power-up take place.

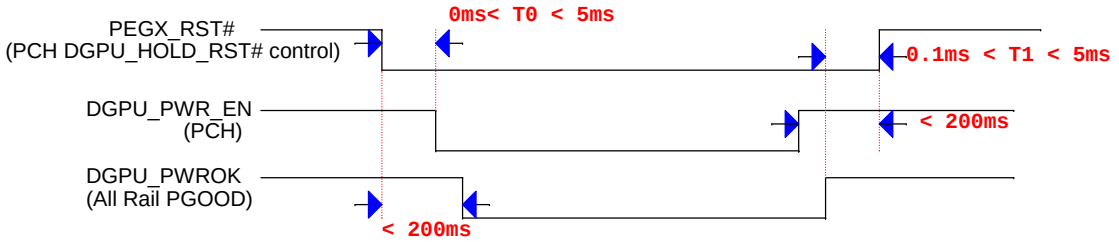
AM7 GPU GC62.0 Entry/Exit sequence



Note.0 : GPU driver ACPI call SBIOS to disables PCIE link.
Note.1 : When GC6 2.0 mode, +1.35V_GFX enabled by GC6_FB_EN
Note.2 : GPU driver ACPI call SBIOS then confirm entry complete by sensing GC6_FB_EN =1, Enable PCIE Link. Then PCH asserts GPU_EVENT#
Note.3 : SBIOS detects GC6_FB_EN =0, then De-asserts GPU_EVENT#
P.S. The entire entry and exit sequence must complete within 200 ms

AM7 Optimus GPU On/Off sequence

T0 = 220 us, PEGX_RST# to DGPU_PWR_EN
2.21 ms, DGPU_PWR_EN to DGPU_PWROK



P.S. The entire entry and exit sequence must complete within 200 ms

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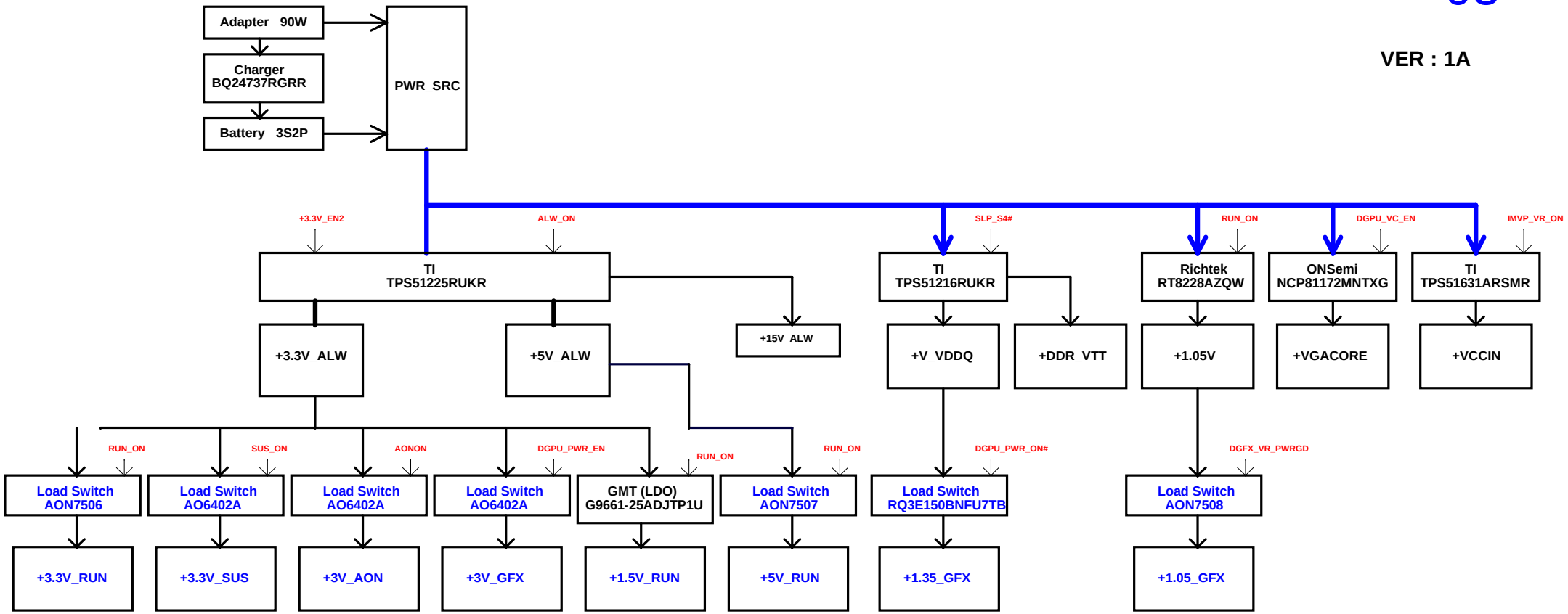
03

VER : 1A



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Size	Document Number	Rev
	Power Block Diagram	C0

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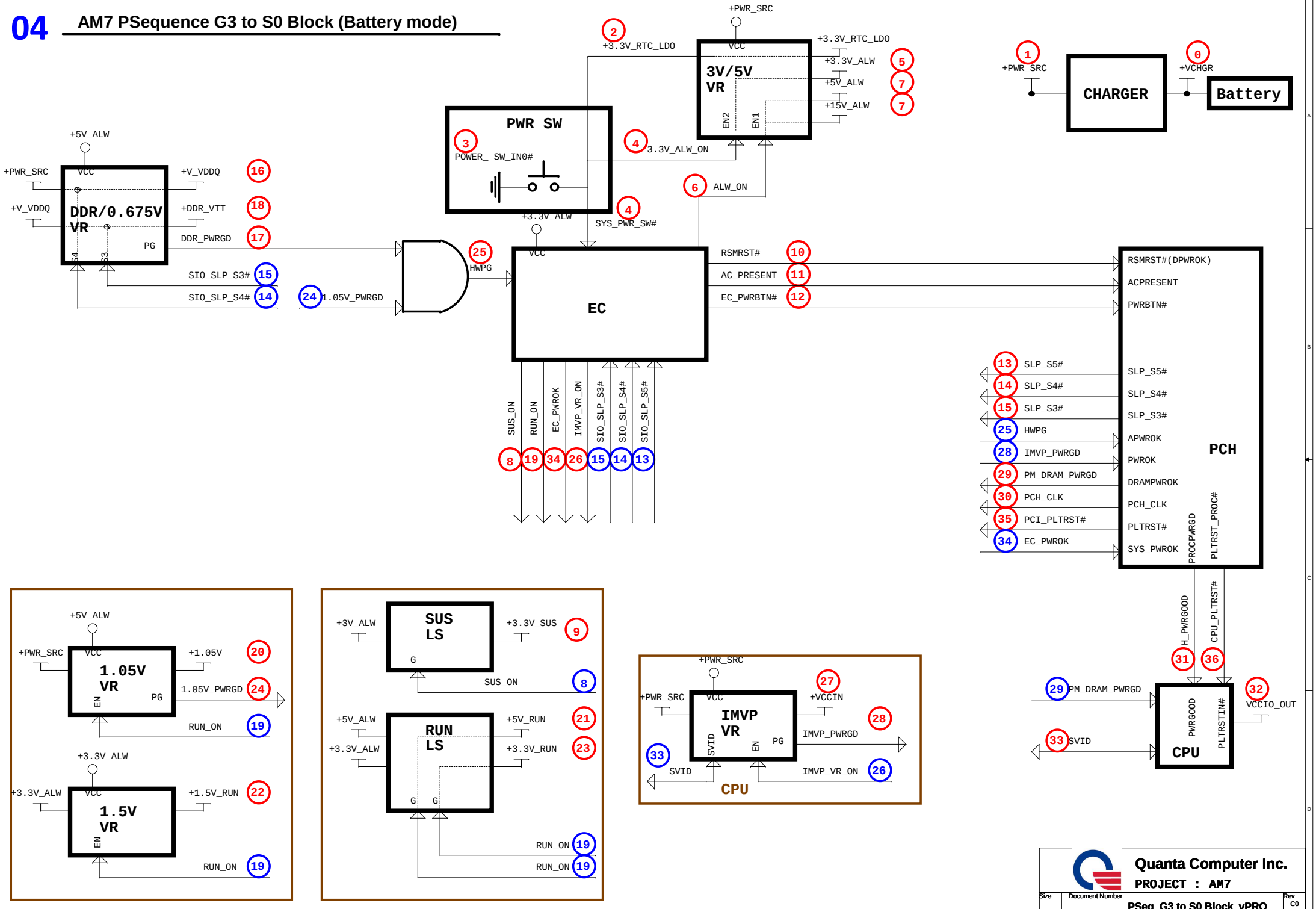
04 AM7 PSequence G3 to S0 Block (Battery mode)



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PROJECT : AM7

Size	Document Number	Rev
	PSeq_G3 to S0 Block_vPRO	C0

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05 AM7 PSequence G3 to S0

+PWR_SRC

+5V_ALW2 and +3.3V_RTC_LDO

G3 mode: > EC reset time + output ALW_ON
S5 mode: > Power button DE-BOUNCE time

POWER_ SW_IN0#

3.3V_ALW_ON

G3 mode: Asserted by HW latch of power button event
S0 mode: Be keeped on high by ALW_ON

+3.3V_ALW

ALW_ON

G3 mode: > 1650 Tick (50 ms)

+5V_ALW

+15V_ALW

SYS_PWR_SW#

G3 mode: EC don't care this event.
S5 mode: Upon power always exist, and this pin keeped on high. Start from this event.

SUS_ON(EC)

528 ms (EC, ALW_ON to SUS_ON, EC)

+3.3V_SUS

+5V_SUS

RSMRST#(EC)
(DPWROK, suspend power well)

37.6 ms (VCCDSW(+3.3V_SUS) to DPWROK(RSMRST#), t04=min 10ms)
(+3.3V_SUS to RSMRST#, t05=min 10ms)
(For a non-DeepSx system DPWROK and RSMRST# go high at the same time)

Thd = 500 us (EC)

EC_PWRBTN# (EC)

minimum duration of PWRBTN# assertion=16ms. PWRBTN# can assert before or after than RSMRST#

SIO_SLP_S5#(PCH)

102 ms (RSMRST# to SLP_S5, t07=min 5ms)

SIO_SLP_S4#(PCH)

35.2 us (SLP_S5 to SLP_S4, t09=min 30us)

+V_VDDQ

DDR_PWRGD

27ms (+V_VDDQ to DDR_PWRGD, t44=min 100ms)
VDDQ (CPU) (-20% of nominal value) to VR_VDDQPWRGD

SIO_SLP_S3#(PCH)

70.2 us (SLP_S4 to SLP_S3, t10=min 30us)

+DDR_VTT

RUN_ON(EC)

22 ms(SLP_S3# to RUN_ON,EC)
EC: SIO_SCP_S3# to RUN_ON delay ?ms

+1.05V

163 ms (VccSUS (+3.3_SUS) to VccASW (+1.05V_PCH), t29= min 0ms)
163 ms (+3.3V_SUS to +1.05V, t31 =min 0ms)

+1.5V_RUN

2 ms(+1.05V stable to +1.5V_RUN stable , min=0s)

+3.3V_RUN

5.68 ms(+1.05V stable to +3.3V_RUN stable , min=0s)

+5V_RUN

HWPG (APWROK)
(1.05V_PWRGD)

5.7 ms(VCCASW to APWROK, t11 mim =1ms)
APWROK may come up earlier than PWROK, but no later

IMVP_VR_ON(EC)

EC: HWPG to IMVP_VR_ON delay 5ms

+VCC_CORE
(CPU CORE)

Vboot

VCC_CORE turn on after SVID vaild.

IMVP_PWRGD
(PWROK)

15.3 ms(APWROK to PWROK, t30 mim =0ms)
15.3 ms(ALL_SYS_PWRGD (HWPG) to PWROK, t14 mim =5ms)
20.9 ms(PCH CORE to PWROK, t41 mim =5ms)

PM_DRAM_PWRGD

18.2 ms(PWROK to PM_DRAM_PWRGD, t18 mim =0us)

PCH CLK

valid

Last un-core power rail stable to DRAMPWROK assertion.

H_PWRGOOD(PCH)
(PWRGOOD)

? ms(PCH CLK stable to H_PWRGOOD, t19 min = 1 ms)
23.6 ms(+VCC_CORE to H_PWRGOOD, min= 5<t13<650 ms)
23.6 ms(PWROK to H_PWRGOOD, t20 min = 2 ms)

VCCIO_OUT

CPU SVID BUS(CPU)

valid

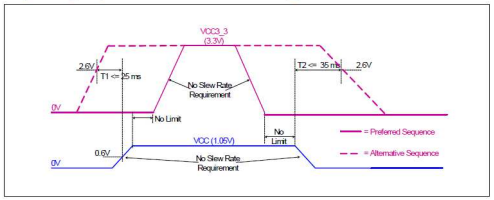
SYS_PWROK
(EC_PWROK)

124 ms(HPWG to SYS_PWROK, t15 min = 5~99 ms)
EC: HPWG to EC_PWROK(EC) Delay 100 ms

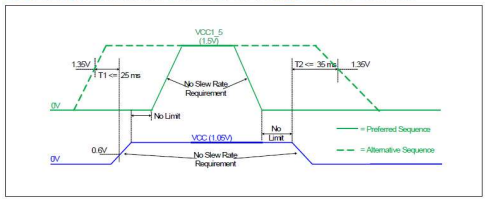
PLTRST#

2.08 ms (SYS_PWROK to PLTRST#, t21+t22 = min 1.06 ms)
PLTRST# could de-assert prior to final SVID value

Sequencing Requirements between PCH VCC3_3 and VCC Core Rail



Sequencing Requirements between PCH VCC1_5 and VCC Core Rail



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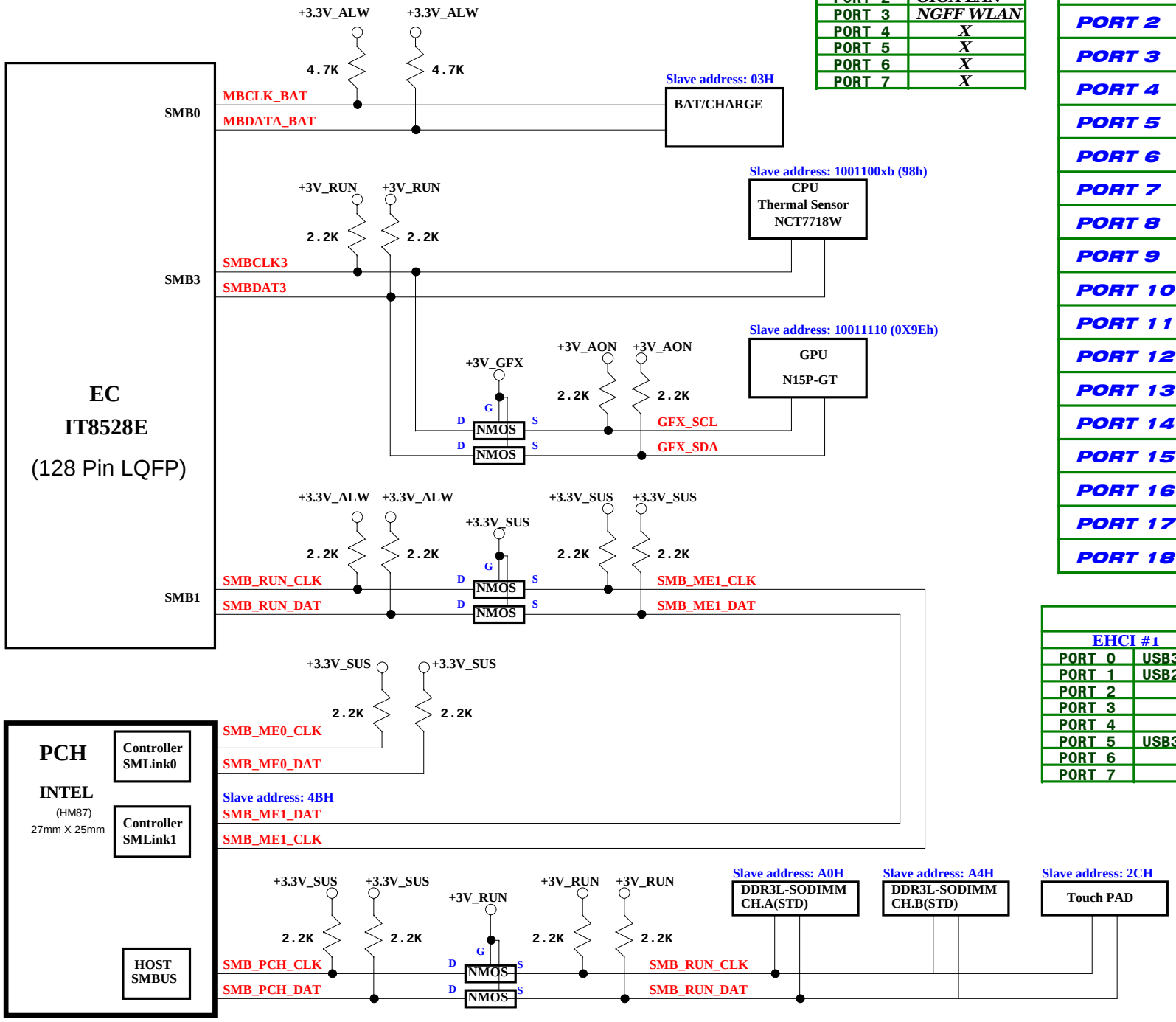
06 SMBus Block



PCIe CLK	
PORT 0	X
PORT 1	X
PORT 2	GIGA LAN
PORT 3	NGFF WLAN
PORT 4	X
PORT 5	X
PORT 6	X
PORT 7	X

HSIO Port	HM87	AM7
PORT 1	USB3.0 PORT1	USB 3.0 CONN 1
PORT 2	USB3.0 PORT2	USB 3.0 CONN 2
PORT 3	USB3.0 PORT5	X
PORT 4	USB3.0 PORT6	X
PORT 5	USB3.0 PORT3 / PCIe* Port 1	X
PORT 6	USB3.0 PORT4 / PCIe* Port 2	X
PORT 7	PCIe* Port 3	GIGA LAN
PORT 8	PCIe* Port 4	NGFF WLAN
PORT 9	PCIe* Port 5	X
PORT 10	PCIe* Port 6	X
PORT 11	PCIe* Port 7	X
PORT 12	PCIe* Port 8	X
PORT 13	PCIe* Port 1 / SATA 6Gb/s Port 4	SATA HDD
PORT 14	PCIe* Port 2 / SATA 6Gb/s Port 5	SATA ODD
PORT 15	SATA 6Gb/s Port 0	X
PORT 16	SATA 6Gb/s Port 1	X
PORT 17	SATA 3Gb/s Port 2	X
PORT 18	SATA 3Gb/s Port 3	X

USB 2.0			
EHCI #1		EHCI #2	
PORT 0	USB3.0 Conn	PORT 8	Camera
PORT 1	USB2.0 CONN / DB	PORT 9	BT
PORT 2	X	PORT 10	X
PORT 3	X	PORT 11	Card reader
PORT 4	X	PORT 12	X
PORT 5	USB3.0 Conn / PS	PORT 13	X
PORT 6	X		
PORT 7	X		

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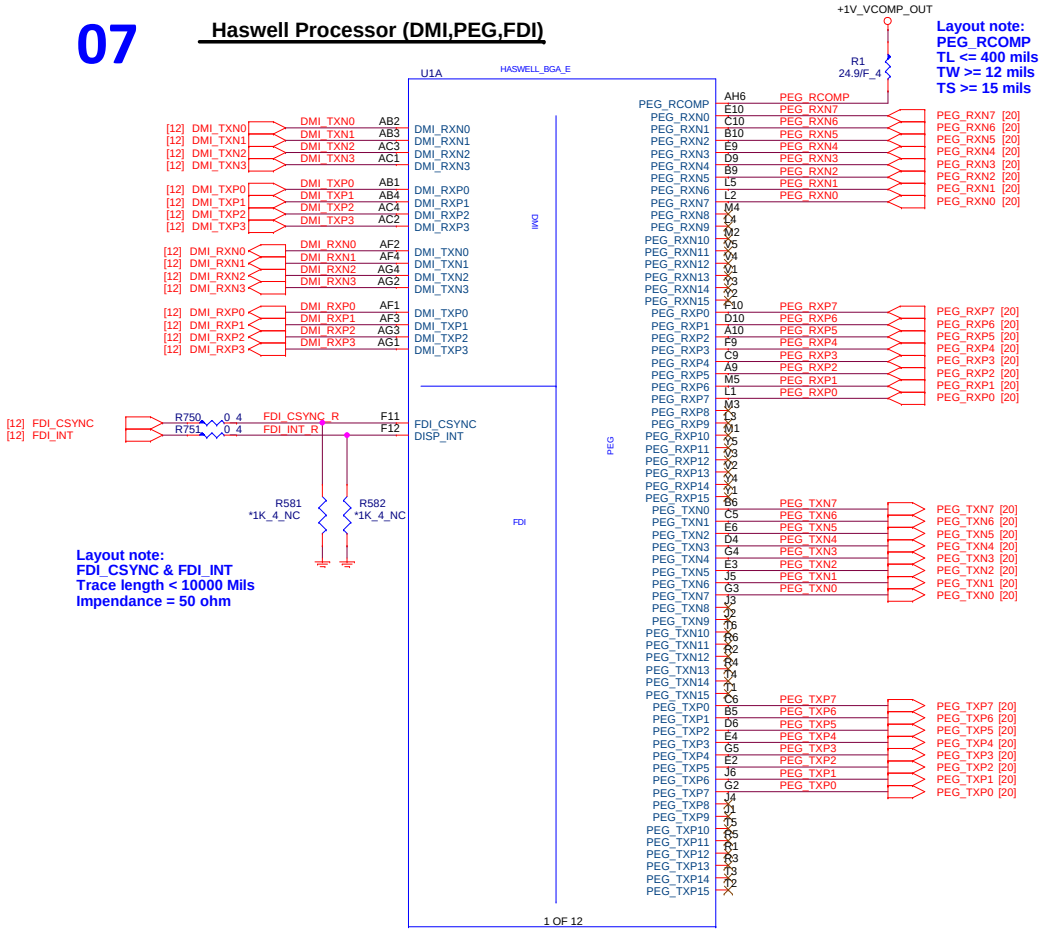
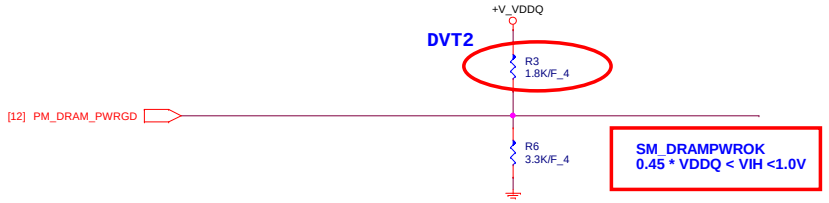
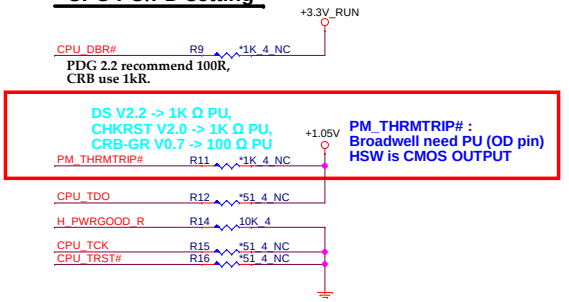
Haswell Processor (DMI,PEG,FDI)



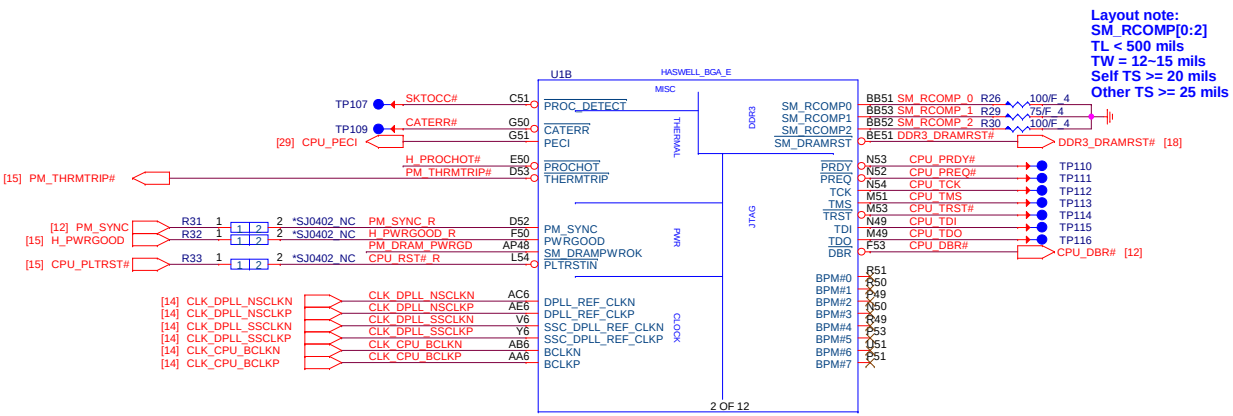
SM_DRAMPWROK# Topology



CPU PU/PD setting

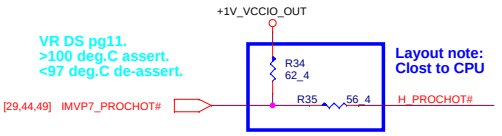


Haswell Processor (CLK,MISC,JTAG)



PROCHOT# Topology

PDG v2.2



Quanta Computer Inc.

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	Haswell 1/5 (PEG/DMI/FDI)	C0

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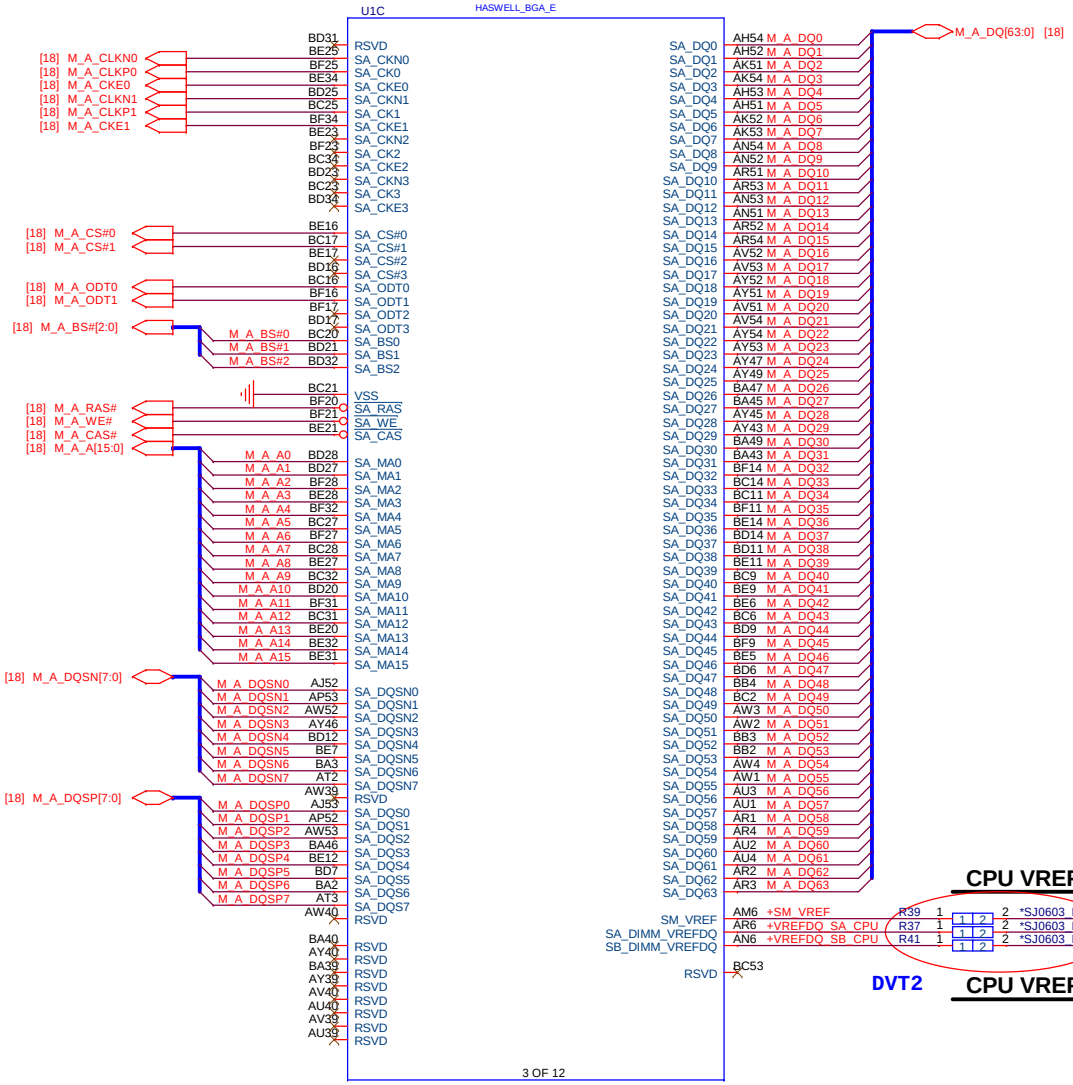
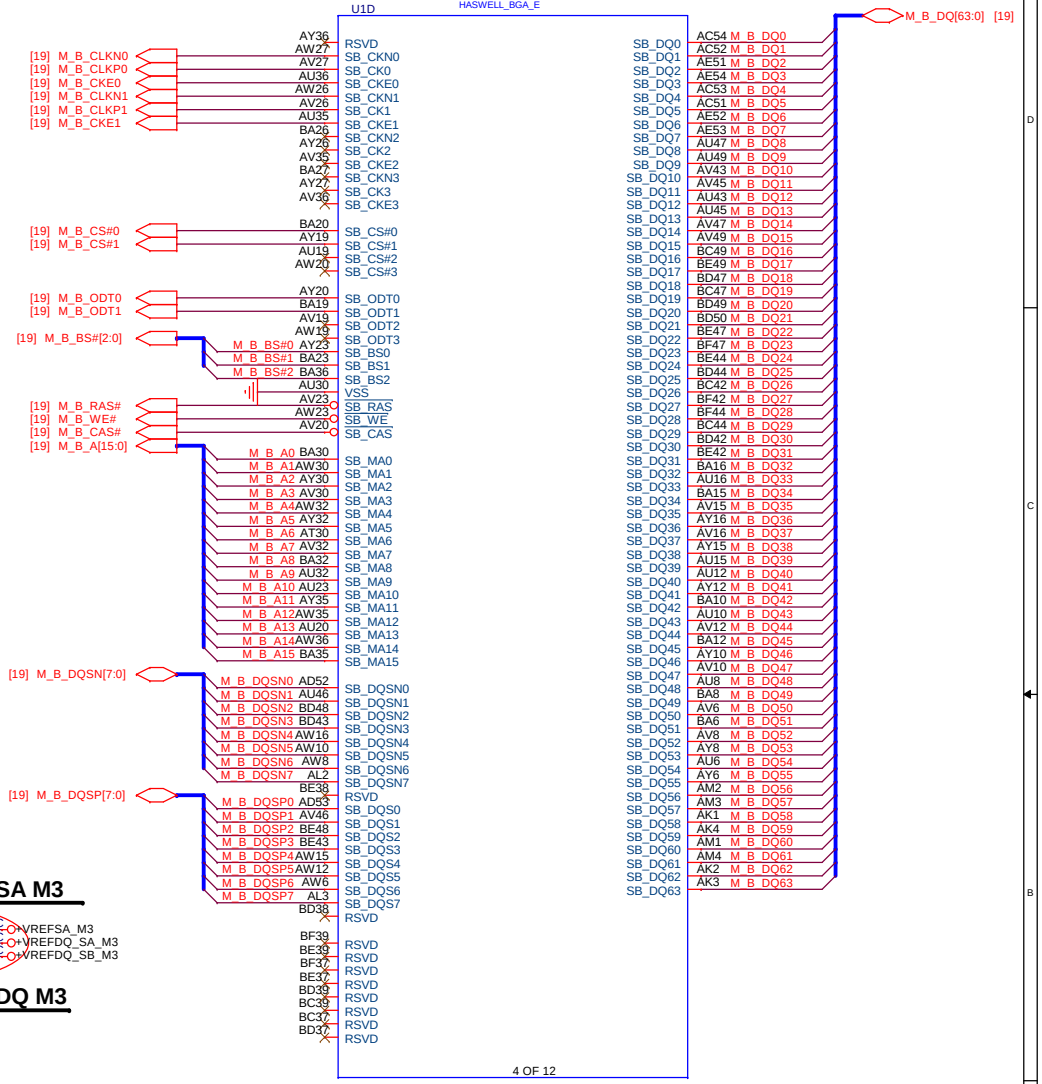
Haswell Processor (DDR3)



Haswell Processor (DDR3)



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	Haswell 2/5 (DDR3 I/F)		C0
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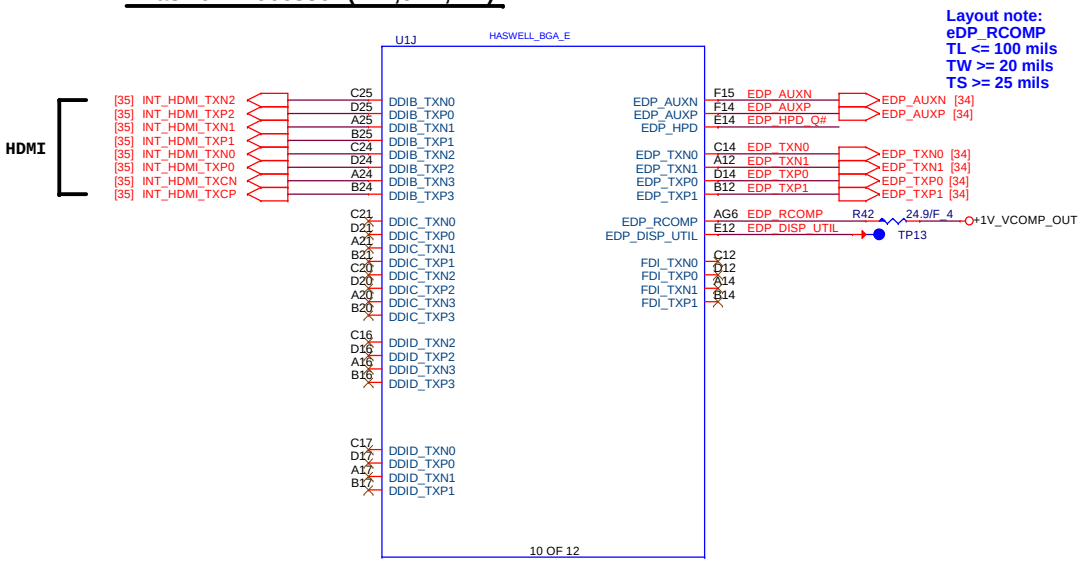
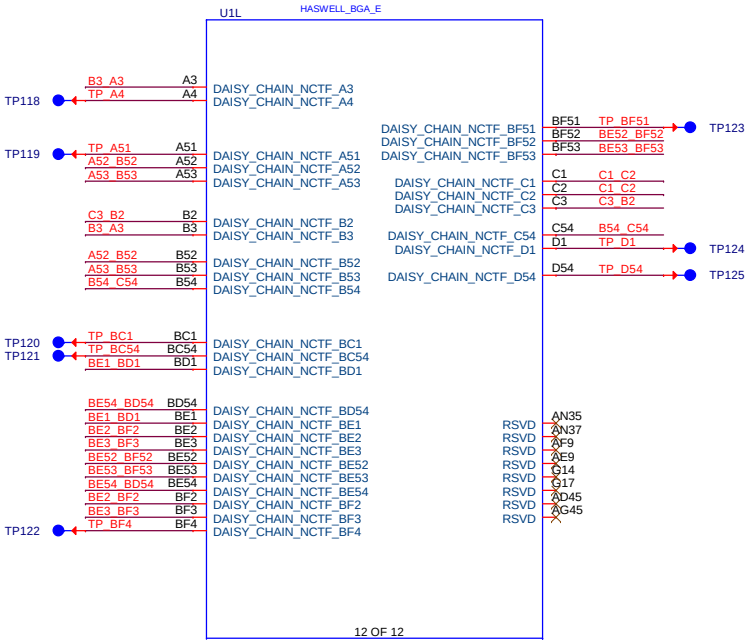
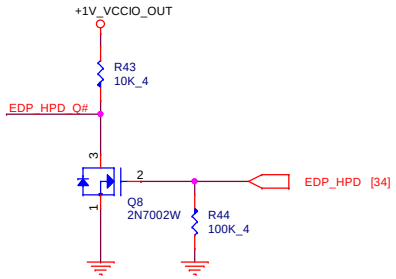
Haswell Processor (DDI,eDP,FDI)



Layout note:
eDP_RCOMP
TL <= 100 mils
TW >= 20 mils
TS >= 25 mils



Level Shift



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Haswell Processor (POWER)

U1F HASWELL_BGA_E — 6 OF 12

U1E HASWELL_BGA_E — 5 OF 12

Layout note: DC,47W,85A

Layout note: DC,47W,2.1A

Layout note: need routing together and ALERT need between CLK and DATA

SVID

SVID CLK (50 ohm)

SVID DATA (50 ohm)

SVID ALERT (50 ohm)

Layout note: Place PU resistor close to CPU

Output capability: 300mA

Output capability: 300mA

CRB is 22uF & 1uF
DG is 4.7uF & 0.1uF

Reserve to Broadwell

R601,R602 Stuff on the Broadwell platform

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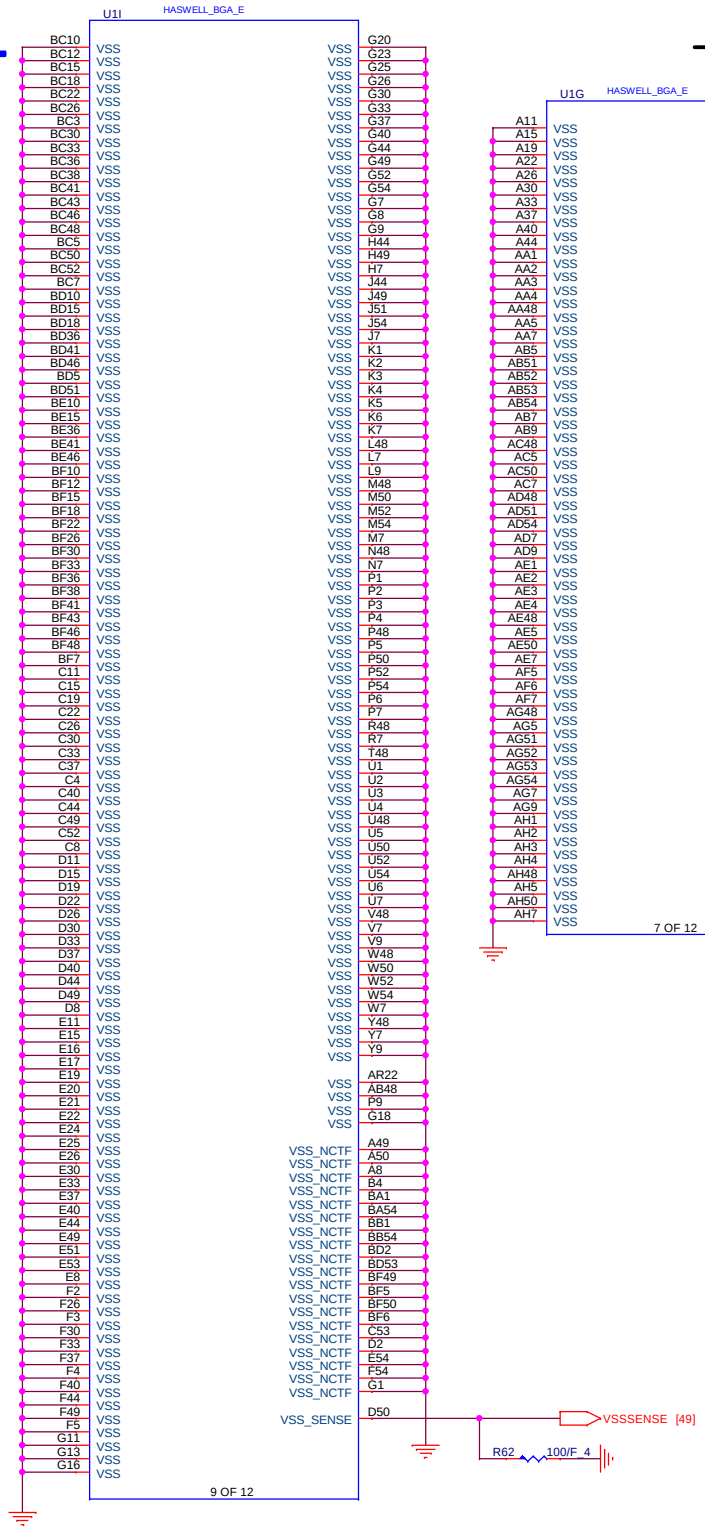
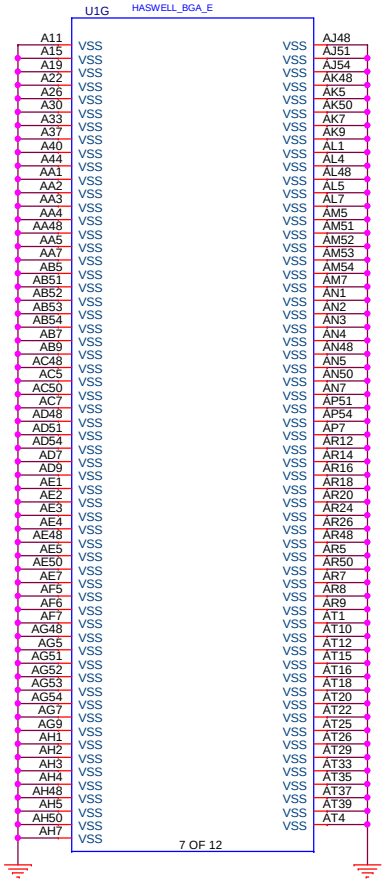
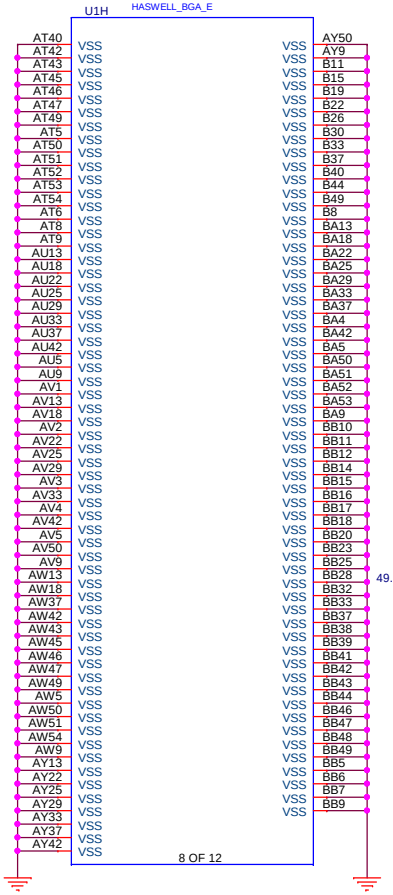
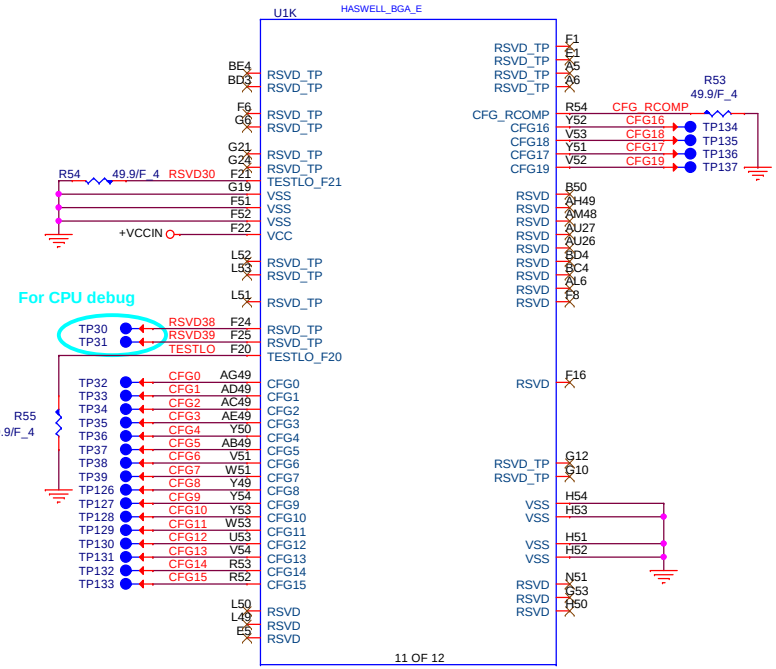
Haswell Processor (GND)







Haswell Processor (CFG,RSVD)



Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R56 1K_4
CFG[3]	MSR Privacy Bit Feature	x1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting x0 = IA32_Debug_Interface_MSR (0xC80) bit[0]. Default setting overridden	CFG3 R57 *1K_4_NC
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	CFG4 R58 1K_4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	CFG6 R59 *1K_4_NC CFG5 R60 1K_4

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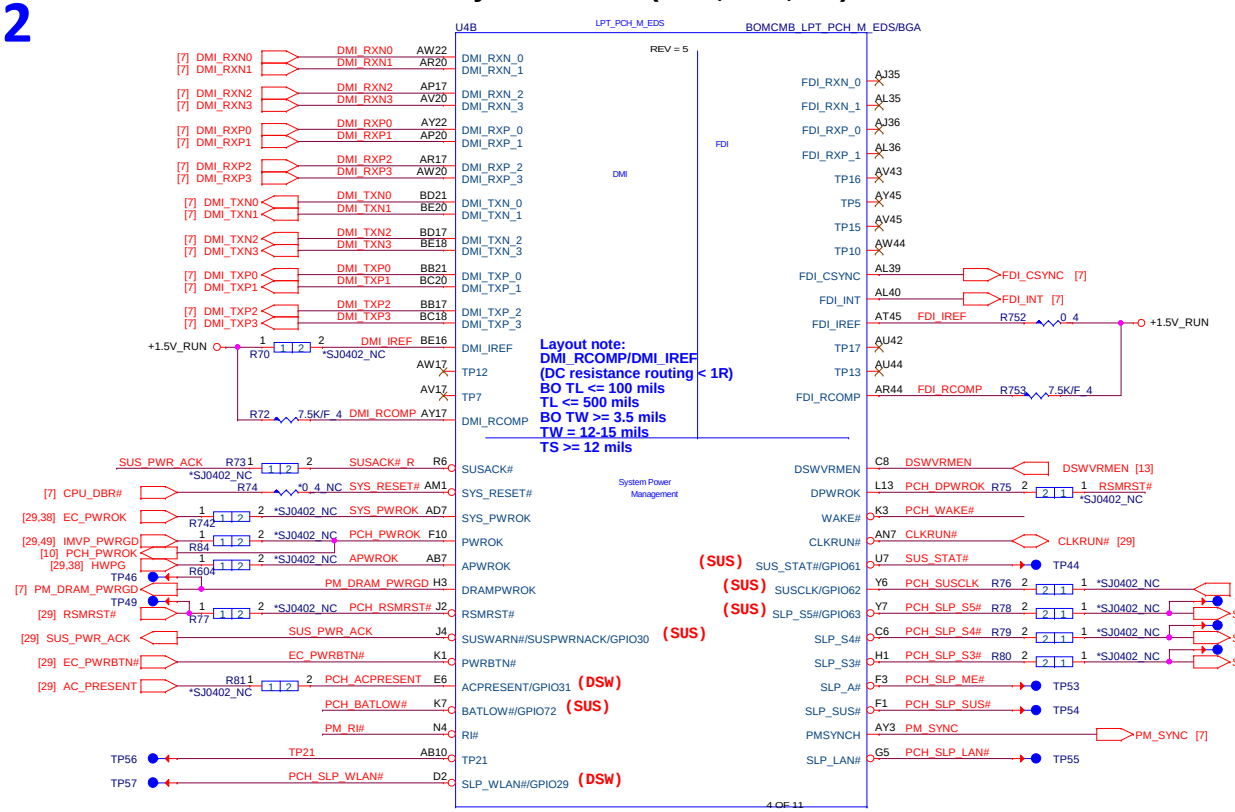
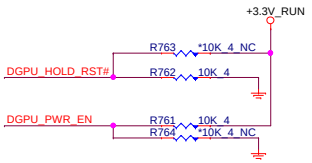
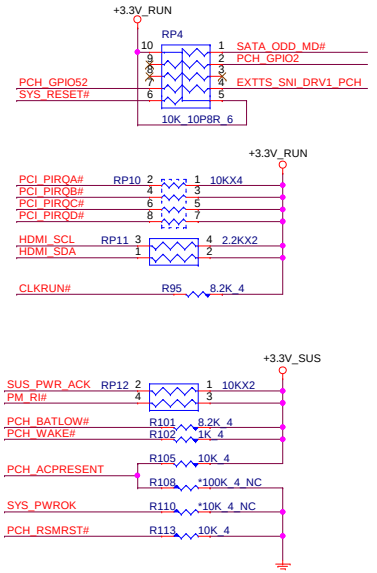
Lynx Point (DMI,FDI,PM)

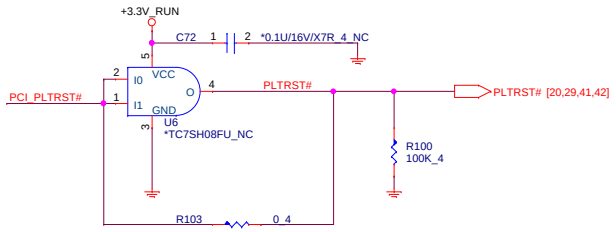




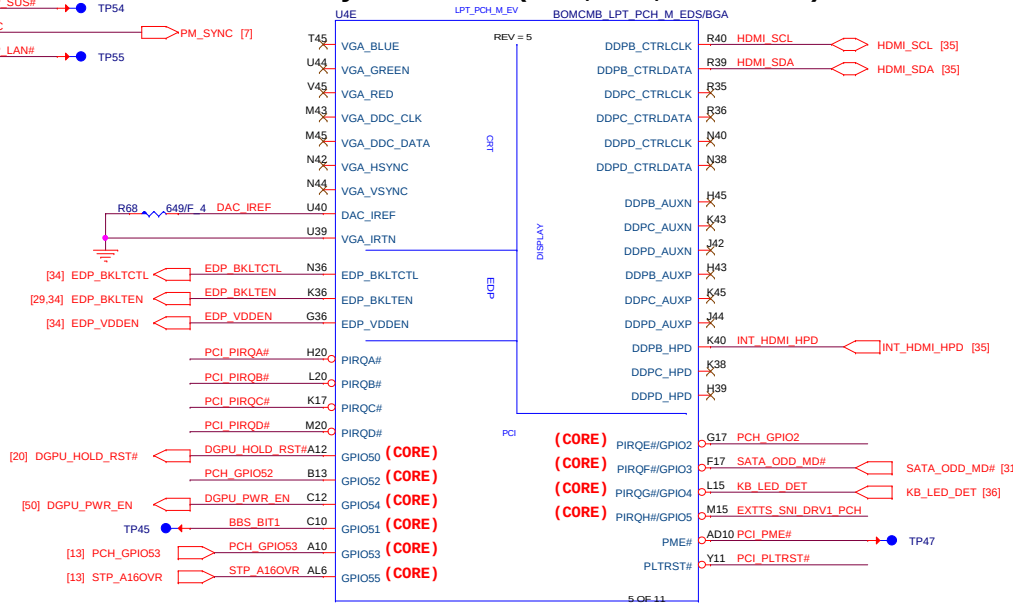
PCH PU/PD setting

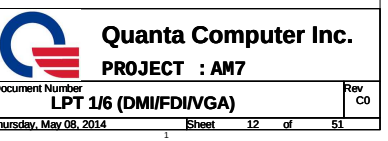


PLTRST# Buffer



Lynx Point (CRT,PCI,DDI CNTL)





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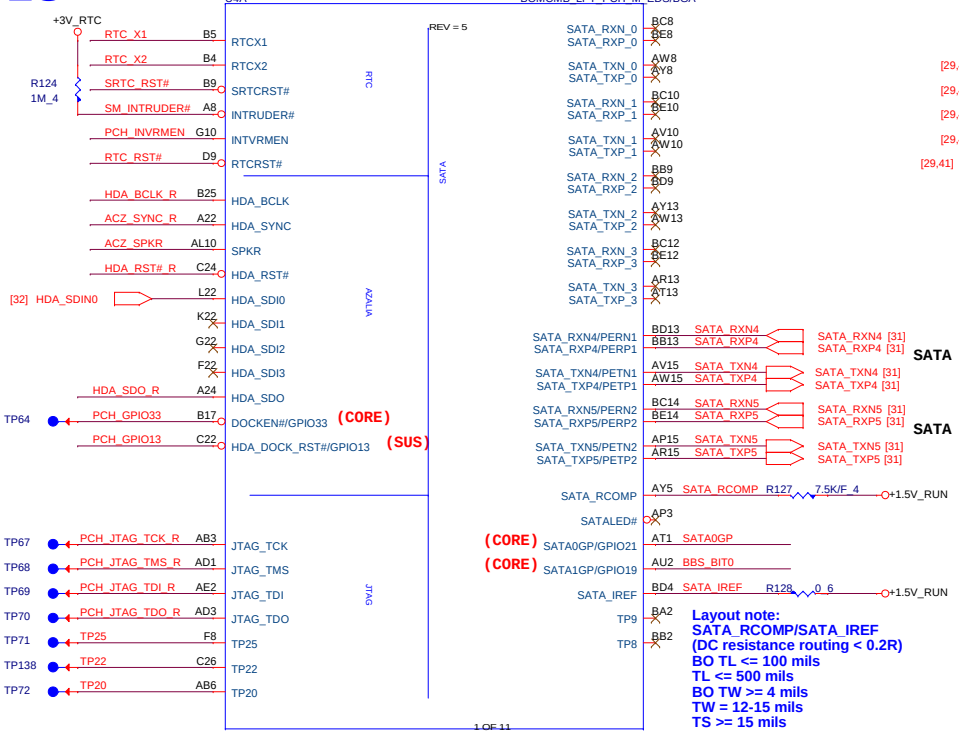
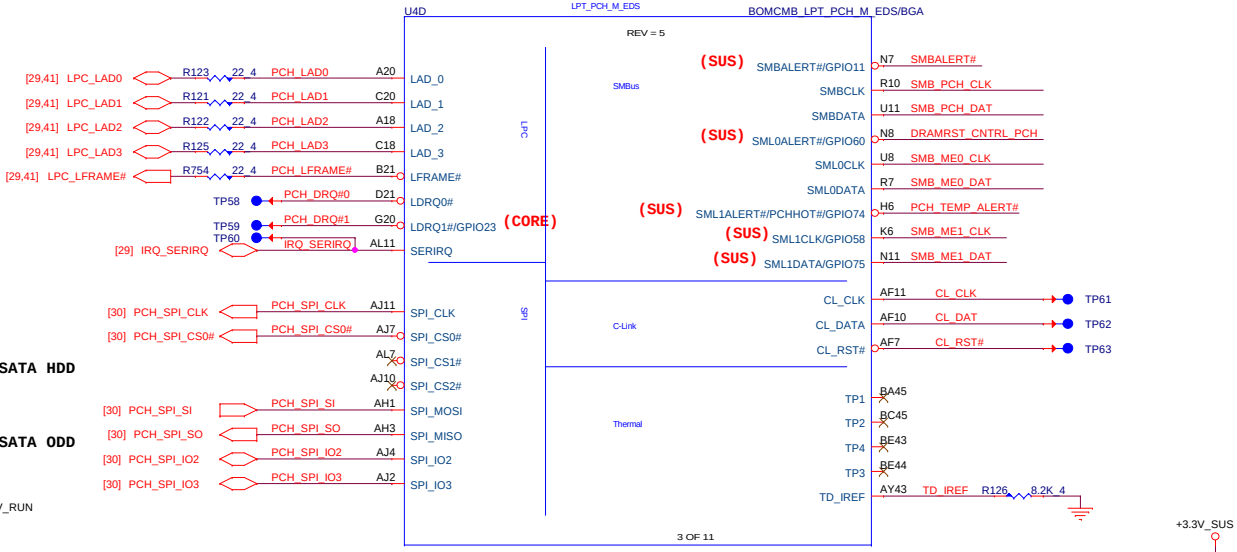
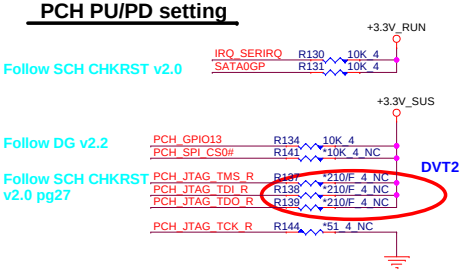
Lynx Point (RTC,IHDA,SATA,JTAG)

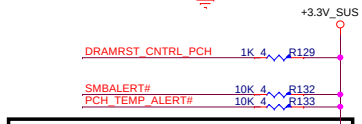


Lynx Point (LPC,SPI,SMBUS,C-LINK,THERMAL)

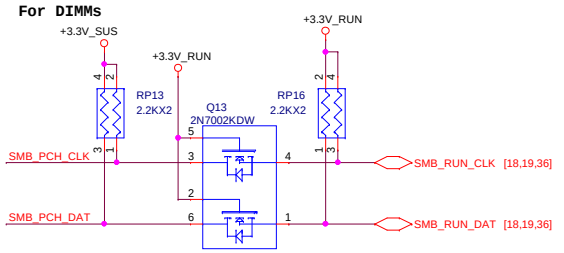


PCH PU/PD setting



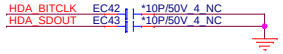


Leakage Isolation



HDA

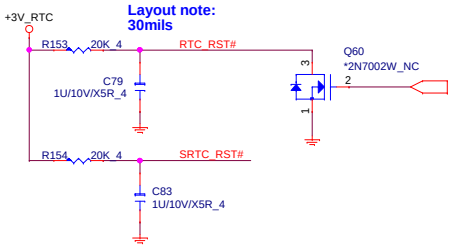
EMI

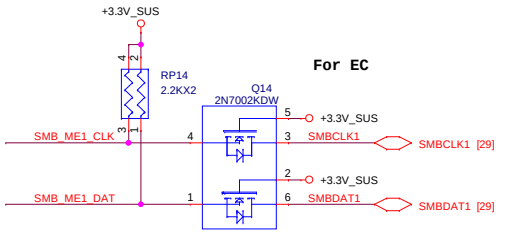


PCH STRAPING

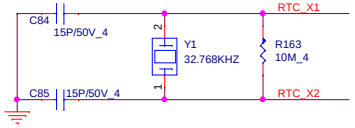
Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	ACZ_SPKR R155 *1K_4_NC +3.3V_RUN
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	[12] SUSCLK R156 *1K_4_NC
GPIO55	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	[12] STP_A16OVR R159 *1K_4_NC
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	PCH_INVRMEN R160 330K_4 +3V_RTC R714 *330K_4_NC
GPIO51	Boot BIOS Strap bit 1	PWROK	Bit1 Bit0 1 0 Resvered 1 1 SPI 0 0 LPC	BBS_BIT0 R161 10K_4 +3.3V_RUN
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK		
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	[29] PCH_MELOCK 1K_4 R162 HDA_SDO_R
DSWVREN	On Die DSW VR Enable	Always	0 = Disable 1 = Enable Must be PU to VCCRTC	[12] DSWVRMEN R164 330K_4 R165 *330K_4_NC +3V_RTC CRB : 330 K PU DG : 390 K PU
GPIO53	DMI AC / DC-Coupling Mode	PWROK	0 = DMI is in AC-coupling mode 1 = DMI is in DC-coupling mode (int PU)	[12] PCH_GPIO53 R628 *1K_4_NC
HDA_DOCK_EN# / GPIO33	DMI TX Termination	PWROK	0 = DMI TX is terminated to VSS (int PD) 1 = DMI TX is terminated to VCC/2.	PCH_GPIO33 R629 *1K_4_NC +3.3V_RUN

RTC Circuitry





RTC Clock 32.768KHz



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	LPT 2/6 (SATA/HDA/SPI)	C0

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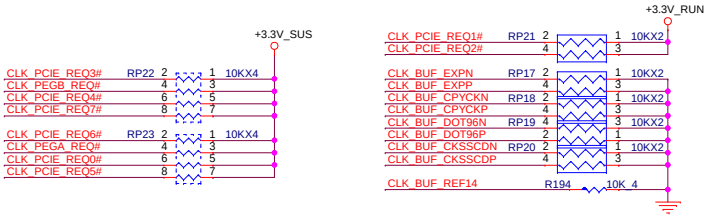
Lynx Point (PCIE,USB3.0,USB2.0)

PCH PU/PD setting



U4I — LPT_PCH_M_EDS — BOMCMB_LPT_PCH_M_EDS/BGA

PCIe / USB

LAN
- [42] PCIE_RXN3 / [42] PCIE_RXP3 → PERN_3 / PERP_3 (AW33 / AY33)
- [42] PCIE_TXN3 / [42] PCIE_TXP3 → C655 / C654 0.1U/16V/X7R_4 PETN_3 / PETP_3 → PETN_3 / PETP_3 (BE34 / BC34)

WLAN
- [41] PCIE_RXN4 / [41] PCIE_RXP4 → PERN_4 / PERP_4 (AT33 / AR33)
- [41] PCIE_TXN4 / [41] PCIE_TXP4 → C656 / C657 0.1U/16V/X7R_4 PETN_4 / PETP_4 → PETN_4 / PETP_4 (BE36 / BC36)

PERN_5 / PERP_5 (AW36 / AV36)
PETN_5 / PETP_5 (BD37 / BB37)
PERN_6 / PERP_6 (AY38 / AW38)
PETN_6 / PETP_6 (BC38 / BE38)
PERN_7 / PERP_7 (AT40 / AT39)
PETN_7 / PETP_7 (BE40 / BC40)
PERN_8 / PERP_8 (AN38 / AN39)
PETN_8 / PETP_8 (BD42 / BD41)

+1.5V_RUN — 1 — 2 PCIE_IREF — R174 *SJ0603_NC — PCIE_IREF (BE30)

TP11 (BC30)

TP6 (BB29)

R179 7.5K/F_4 PCIE_RCOMP — PCIE_RCOMP (BD29)

Layout note:
PCIE_RCOMP/PCIE_IREF
(DC resistance routing < 0.2R)
BO TL <= 100 mils
TL <= 500 mils
BO TW >= 4 mils
TW = 12-15 mils
TS >= 12 mils

USB2N0 (AW31) PERN1/USB3RN3
USB2P0 (AY31) PERP1/USB3RP3
USB2N1 (BE32) PETN1/USB3TN3
USB2P1 (BC32) PETP1/USB3TP3
USB2N2 (AT31) PERN2/USB3RN4
USB2P2 (AR31) PERP2/USB3RP4
USB2N3 (BD33) PETN2/USB3TN4
USB2P3 (BB33) PETP2/USB3TP4

USB3.0 Conn
USB2.0 CONN / DB — **USB2.0 Port 1 & port 9 is debug port.**

- USB2N0 B37 → USB2_N0 [39]
- USB2P0 D37 → USB2_P0 [39]
- USB2N1 A38 → USB2_N1 [42]
- USB2P1 C38 → USB2_P1 [42]

USB2N2 A36, USB2P2 C36, USB2N3 A34, USB2P3 C34, USB2N4 A33, USB2P4 C33

USB3.0 Conn / PS

- USB2N5 C31 → USB2_N5 [39]
- USB2P5 G31 → USB2_P5 [39]

USB2N6 K31, USB2P6 L31, USB2N7 G29, USB2P7 G29

Camera

- USB2N8 A32 → USB2_N8 [34]
- USB2P8 C32 → USB2_P8 [34]

BT

- USB2N9 A30 → USB2_N9 [41]
- USB2P9 C30 → USB2_P9 [41]

USB2N10 B29, USB2P10 G29, USB2N11 A28

Card reader

- USB2P11 C28 → USB2_N11 [40] / USB2_P11 [40]

USB2N12 G26, USB2P12 E26, USB2N13 E24, USB2P13 G24

ext. USB Left

- USB3RN1 AR26 → USB3_RXN1 [39]
- USB3RP1 AP26 → USB3_RXP1 [39]
- USB3TN1 BE24 → USB3_TXN1 [39]
- USB3TP1 BD23 → USB3_TXP1 [39]

ext. USB Left

- USB3RN2 AW26 → USB3_RXN2 [39]
- USB3RP2 AV26 → USB3_RXP2 [39]
- USB3TN2 BD25 → USB3_TXN2 [39]
- USB3TP2 BC24 → USB3_TXP2 [39]

USB3RN5 AW29, USB3RP5 AV29, USB3TN5 BE26, USB3TP5 BC26, USB3RN6 AR29, USB3RP6 AP29, USB3TN6 BD27, USB3TP6 BE28

USBRBIAS# K24 — USBCOMP — R170 22.6/F_4
USBRBIAS K26

USBCOMP
Impedance = 50 Ohm
Trace length <= 500 mils
Trace spacing >= 15 mils

TP24 M33, TP23 C33

(SUS) OC0#/GPIO59 P3 → USB_OC0# → USB_OC0# [39]
(SUS) OC1#/GPIO40 V1 → USB_OC1# → USB_OC1# [42]
(SUS) OC2#/GPIO41 U2 → USB_OC2# → USB_OC2# [39]
(SUS) OC3#/GPIO42 P1 → USB_OC3#
(SUS) OC4#/GPIO43 M3 → USB_OC4#
(SUS) OC5#/GPIO9 T1 → USB_OC5#
(SUS) OC6#/GPIO10 N2 → USB_OC6#
(SUS) OC7#/GPIO14 M1 → USB_OC7#

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+3.3V_SUS — RP3
10 — USB_OC0# 9 — USB_OC1# 8 — USB_OC2# 7 — USB_OC3# 6 — 5 USB_OC4# 4 USB_OC5# 3 USB_OC6# 2 USB_OC7# 1
10K_10P8R_6

EMI

CLK_33M_EC EC36 *10P/50V_4_NC
CLK_33M_DEBUG EC37 *10P/50V_4_NC
CLK_33M_FB EC38 *10P/50V_4_NC

XTAL25_IN / XTAL25_OUT — R190 1M_4 — Y2 25MHz — C86 12P/50V/_4 — C87 15P/50V_4

Lynx Point (CLOCK)

U4C — LPT_PCH_M_EDS — BOMCMB_LPT_PCH_M_EDS/BGA

CLKOUT_PCIE_N_0 (Y43), CLKOUT_PCIE_P_0 (Y45)
CLK_PCIE_REQ0# → PCIECLKRQ0#/GPIO73 (AB1) (SUS)

CLKOUT_PCIE_N_1 (AA44), CLKOUT_PCIE_P_1 (AA42)
CLK_PCIE_REQ1# → PCIECLKRQ1#/GPIO18 (AF1) (CORE)

CLKOUT_PCIE_N_2 (AB43), CLKOUT_PCIE_P_2 (AB45)
PCIECLKRQ2#/GPIO20/SMI# (CORE)

CLKOUT_PCIE_N_3 (AD43), CLKOUT_PCIE_P_3 (AD45)
PCIECLKRQ3#/GPIO25 (SUS)

CLKOUT_PCIE_N_4 (AF43), CLKOUT_PCIE_P_4 (AF45)
CLK_PCIE_REQ4# → PCIECLKRQ4#/GPIO26 (V3) (SUS)

CLKOUT_PCIE_N5 (AE44), CLKOUT_PCIE_P_5 (AE42)
CLK_PCIE_REQ5# → PCIECLKRQ5#/GPIO44 (AA2) (SUS)

CLKOUT_PCIE_N_6 (AB40), CLKOUT_PCIE_P_6 (AB39)
CLK_PCIE_REQ6# → PCIECLKRQ6#/GPIO45 (AE4) (SUS)

CLKOUT_PCIE_N_7 (AJ44), CLKOUT_PCIE_P_7 (AJ42)
CLK_PCIE_REQ7# → PCIECLKRQ7#/GPIO46 (Y3) (SUS)

CLKOUT_ITPXDP (AH43), CLKOUT_ITPXDP_P (AH45)
CLKOUT_33MHZ0 (D44), CLKOUT_33MHZ1 (E44), CLKOUT_33MHZ2 (B42), CLKOUT_33MHZ3 (F41), CLKOUT_33MHZ4 (A40)

CLOCK SIGNAL

2 OF 11

[42] CLK_PCIE_LANN → R167 *SJ0402_NC → CLK_PCIE_REQ2# (AF3)
[42] CLK_PCIE_LANP
[42] PCIE_CLKREQ_LAN#
[41] CLK_PCIE_WLANN → R166 *SJ0402_NC → CLK_PCIE_REQ3# (T3)
[41] CLK_PCIE_WLANP
[41] PCIE_CLKREQ_WLAN#

CLK_33M_FB R172 22_4 CLK_33M_PCI2
[41] CLK_33M_DEBUG R175 22_4 CLK_33M_PCI3
[29] CLK_33M_EC R176 22_4 CLK_33M_PCI4

R175 For Debug Only, Remove at QT

CLKOUT_PEG_A (AB35) → CLK_PCIE_VGAN [20]
CLKOUT_PEG_A_P (AB36) → CLK_PCIE_VGAP [20]
PEGA_CLKRQ#/GPIO47 (AF6) (SUS) → CLK_PEGA_REQ# → CLK_PEGA_REQ# [20]
CLKOUT_PEG_B (Y39)
CLKOUT_PEG_B_P (Y38)
PEGB_CLKRQ#/GPIO56 (SUS) → U4 CLK_PEGB_REQ#
CLKOUT_DMI (AF39) → CLK_CPU_BCLKN [7]
CLKOUT_DMI_P (AF40) → CLK_CPU_BCLKP [7]
CLKOUT_DP (AJ40) → CLK_DPLL_SSCLKN [7]
CLKOUT_DP_P (AJ39) → CLK_DPLL_SSCLKP [7]
CLKOUT_DPNS (AF35) → CLK_DPLL_NSCLKN [7]
CLKOUT_DPNS_P (AF36) → CLK_DPLL_NSCLKP [7]
CLKIN_DMI (AY24) → CLK_BUF_EXPN
CLKIN_DMI_P (AW24) → CLK_BUF_EXPP
CLKIN_GND (AR24) → CLK_BUF_CPYCKN
CLKIN_GND_P (AT24) → CLK_BUF_CPYCKP
CLKIN_DOT96N (H33) → CLK_BUF_DOT96N
CLKIN_DOT96P (G33) → CLK_BUF_DOT96P
CLKIN_SATA (BE6) → CLK_BUF_CKSSCDN
CLKIN_SATA_P (BC6) → CLK_BUF_CKSSCDP
REFCLK14IN (F45) → CLK_BUF_REF14
CLKIN_33MHZLOOPBACK (D17) → CLK_33M_FB
XTAL25_IN (AM43) → XTAL25_IN
XTAL25_OUT (AL44) → XTAL25_OUT
(CORE) CLKOUTFLEX0/GPIO64 (C40) → CLK_FLEX0 → TP73
(CORE) CLKOUTFLEX1/GPIO65 (F38) → CLK_FLEX1 → TP74
(CORE) CLKOUTFLEX2/GPIO66 (F36) → CLK_FLEX2 → TP75
(CORE) CLKOUTFLEX3/GPIO67 (F39) → CLK_FLEX3 → TP117
ICLK_IREF (AM45) → ICLK_IREF — 1 — 2 R173 *SJ0402_NC → +1.5V_RUN
TP19 (AD39), TP18 (AD38)
DIFFCLK_BIASREF (AN44) → ICLK_BIAS — R178 7.5K/F_4

CLKOUT_FLEX[2:3] if enabled, must be programmed to the same clock frequency due to sharing the same internal power rail.

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Size	Document Number	Rev
	LPT 3/6 (PCIE/USB/CLK)	C0

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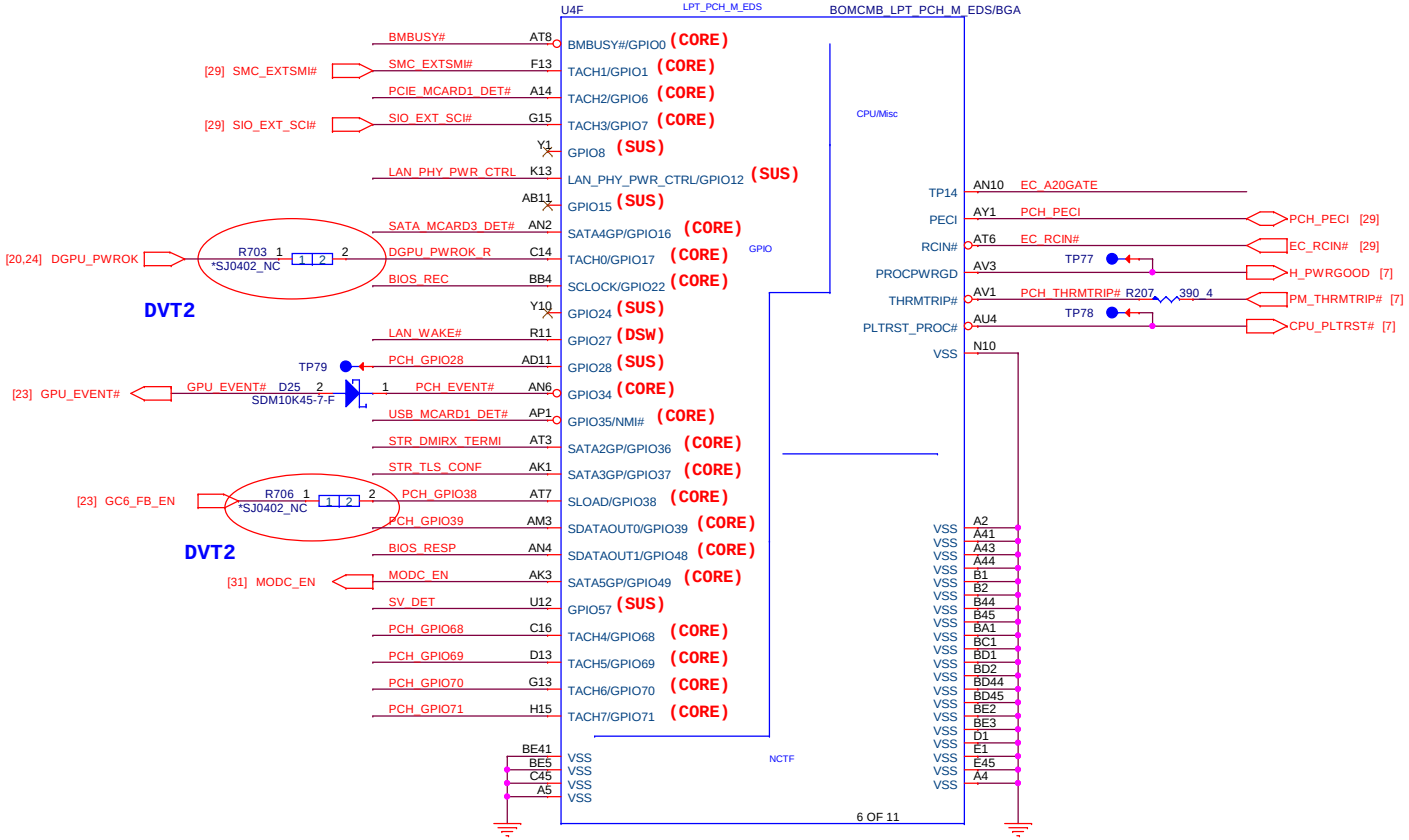
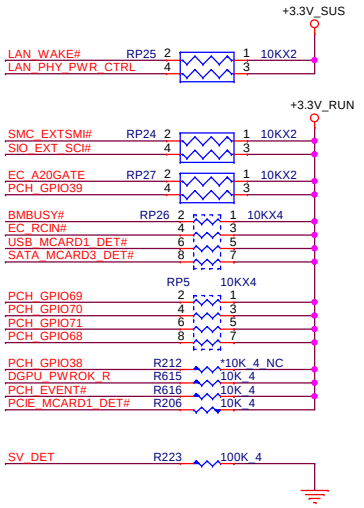
Lynx Point (GPIO,CPU/MISC,NCTF)



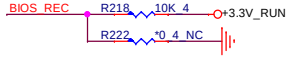
PCH PU/PD setting



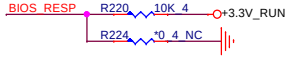
PCH Strap

Pin Name	Usage	Sampled	Configuration	Ref. Doc.	Circuitry
SATA2GP / GPIO36	DMI RX Termination	Rising edge of PWROK	0 = DMI RX is terminated to VSS. 1 = DMI RX is terminated to VCC/2.	PCH EDS v2.3 SCH CHKLST v2.0	STR_DMIRX_TERMI R214 10K_4 R215 *200K/F_4_NC +3.3V_RUN
SATA3GP / GPIO37	TLS Confidentiality	Rising edge of PWROK	0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).	PCH EDS v2.3 SCH CHKLST v2.0	STR_TLS_CONF R216 10K_4 R217 *200K/F_4_NC +3.3V_RUN

BIOS RECOVERY 0 = Enable 1 = Disable



BIOS_RESP 0 = BIOS RESP 1 = Default



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	LPT 4/6 (GPIO/MISC)	C0

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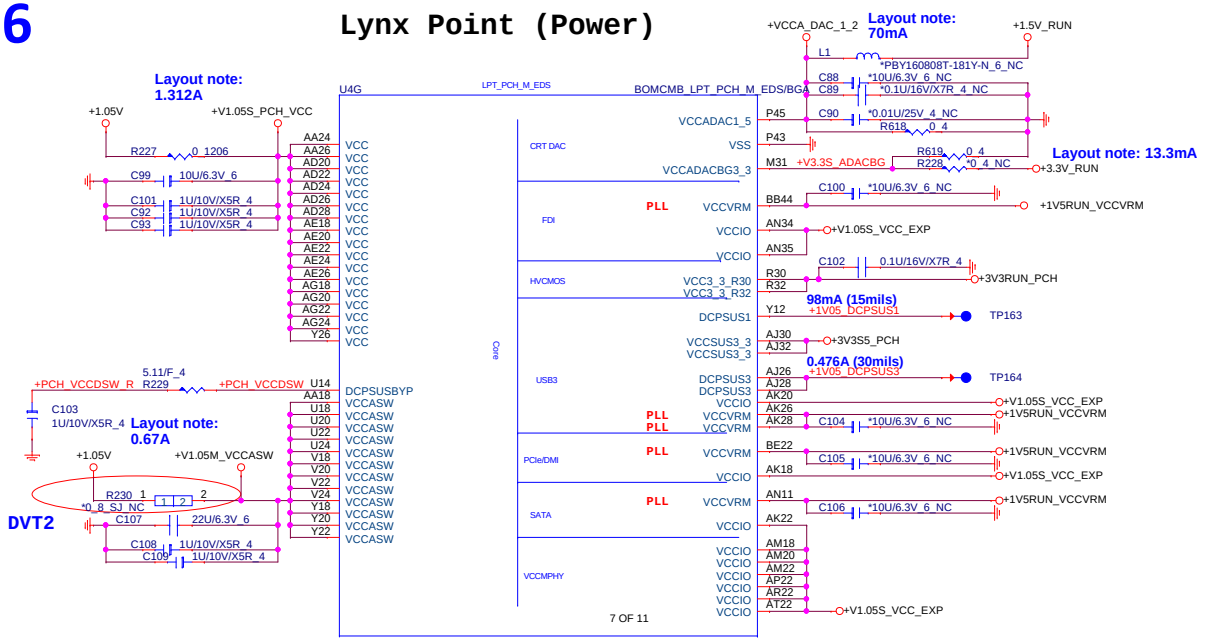
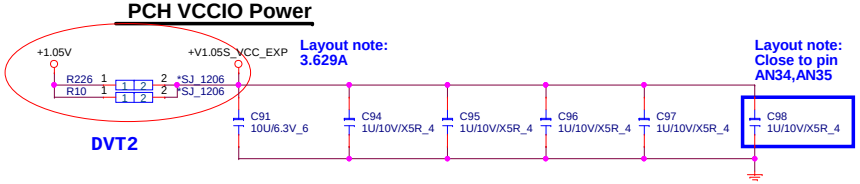
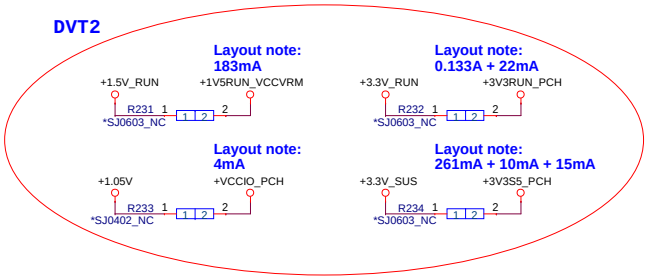
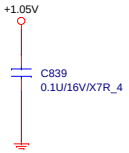
Lynx Point (Power)



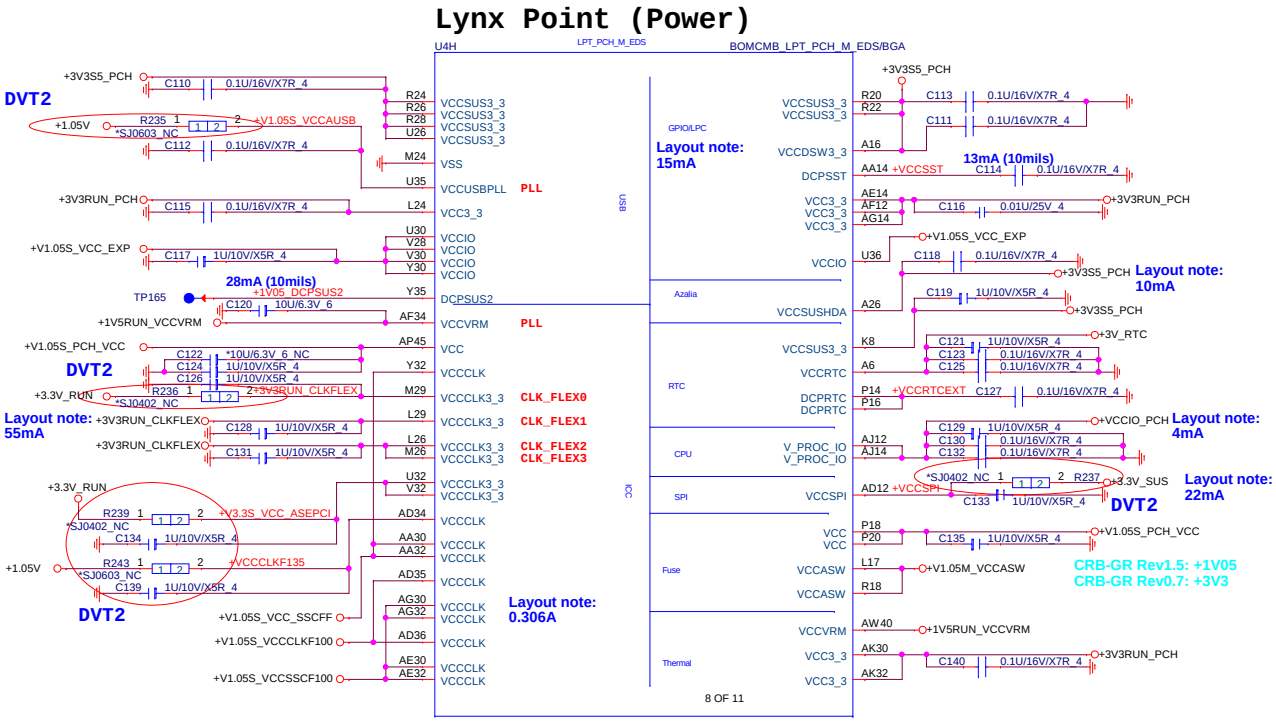
PCH VCCIO Power

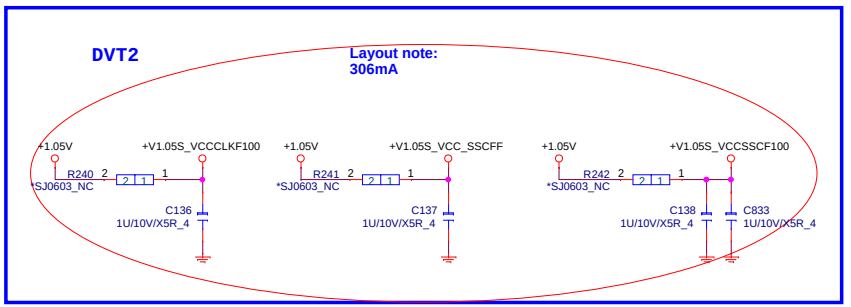






Lynx Point (Power)





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	LPT 5/6 (POWER)		C0
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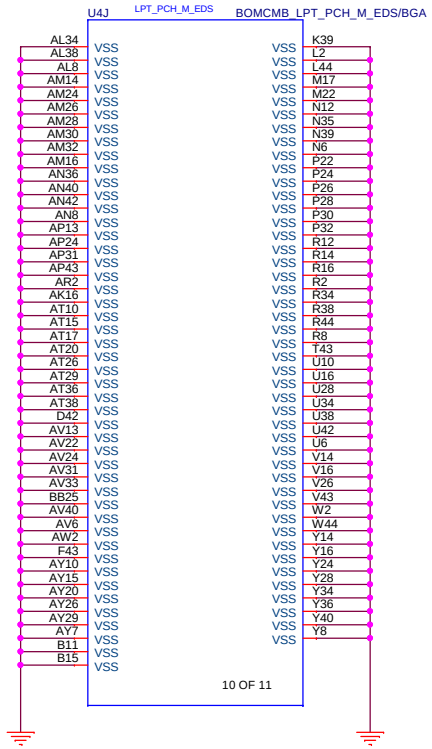
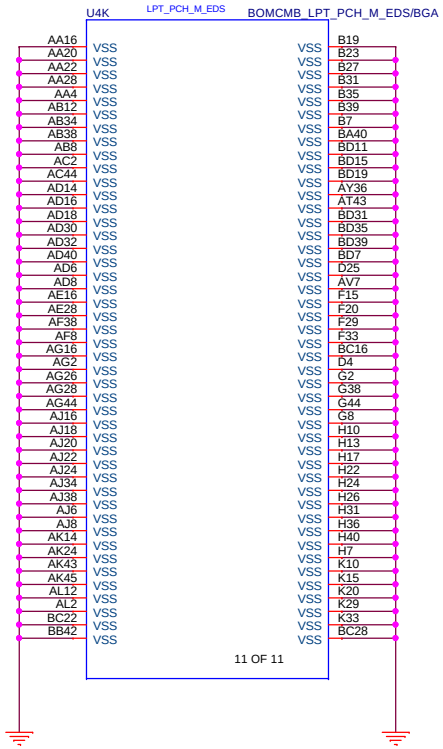
Lynx Point (GND)



Lynx Point (GND)



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	LPT 6/6 (GND)	C0

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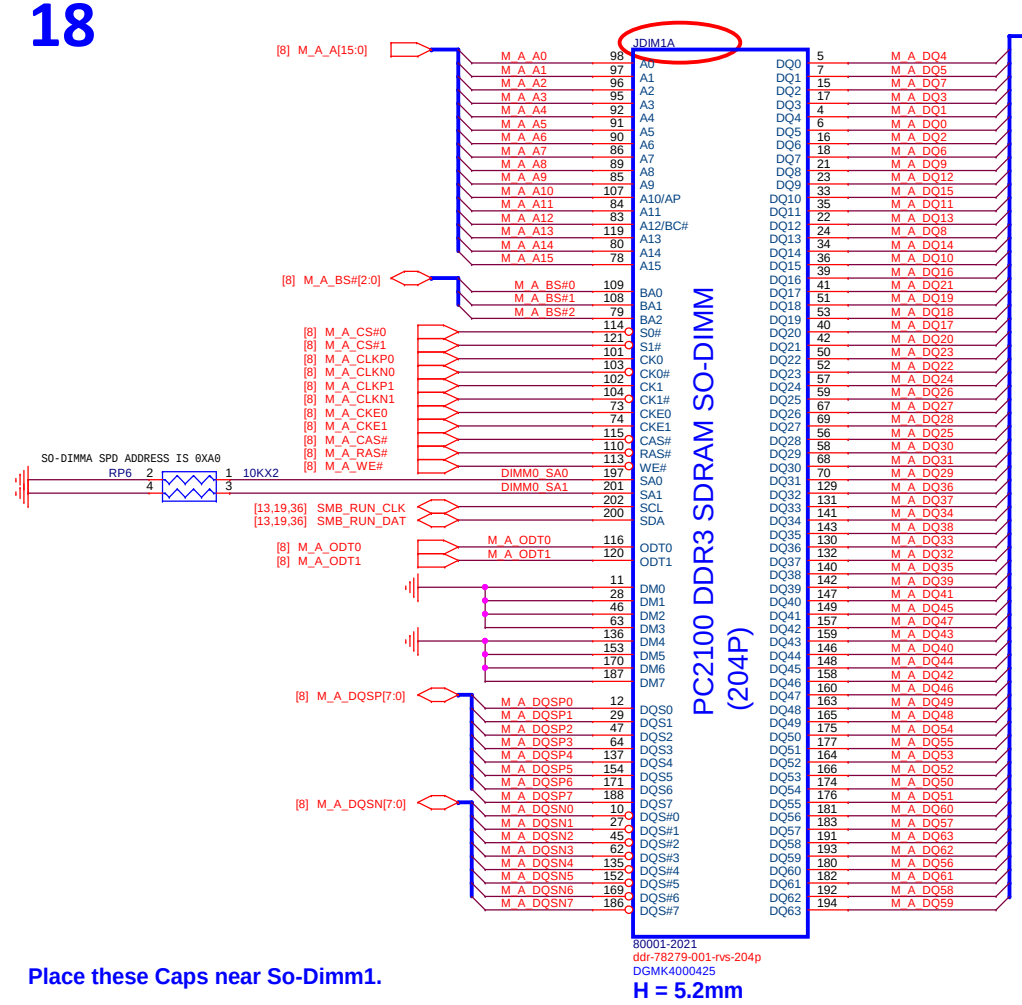
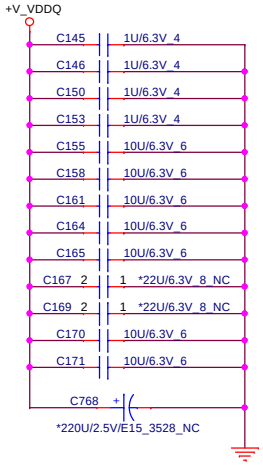
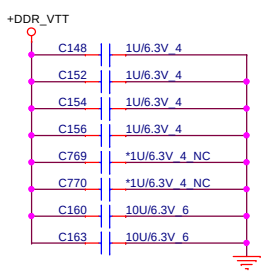
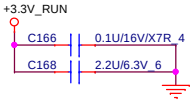
DVT2

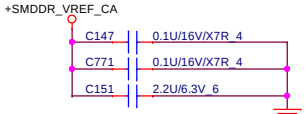


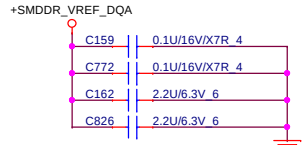
Place these Caps near So-Dimm1.

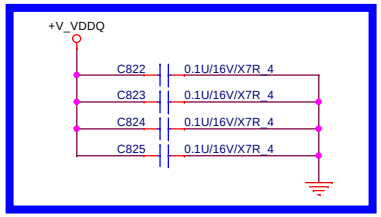


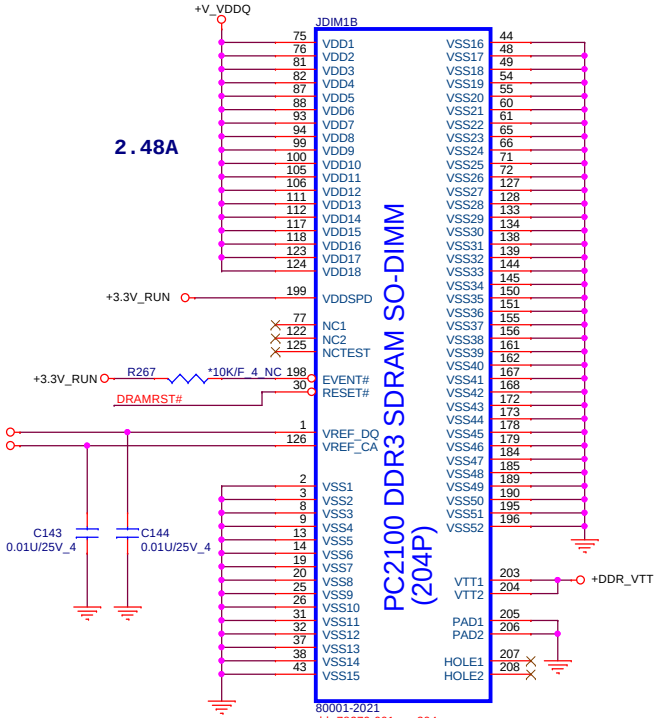




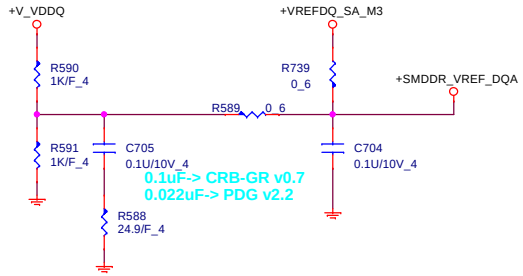




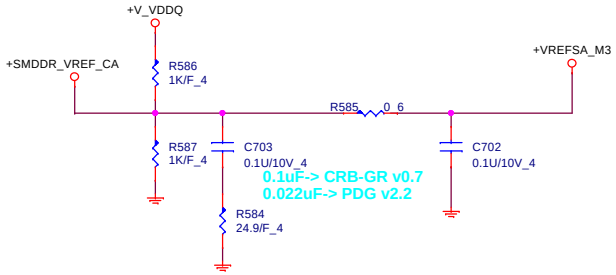


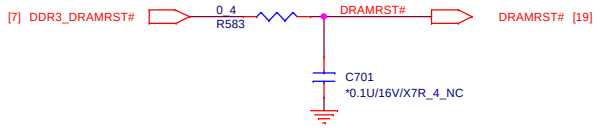


M3 VREF + M1 VREF



VREF SA0 M1/M3 Solution





Quanta Computer Inc.

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Size	Document Number	Rev
	DDR3 DIMM1-RVS (4.0H)	C0

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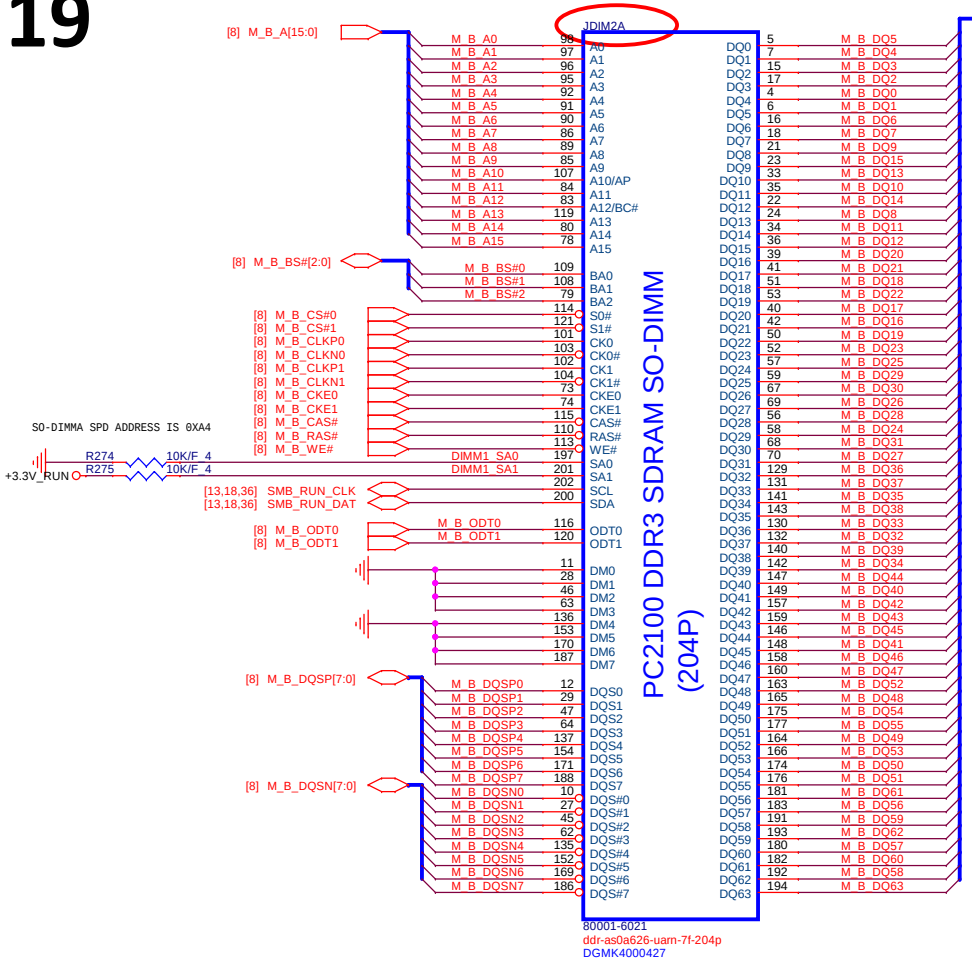
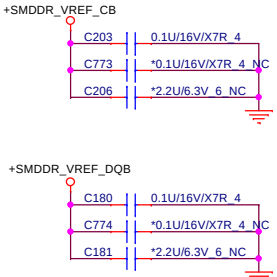
DVT2

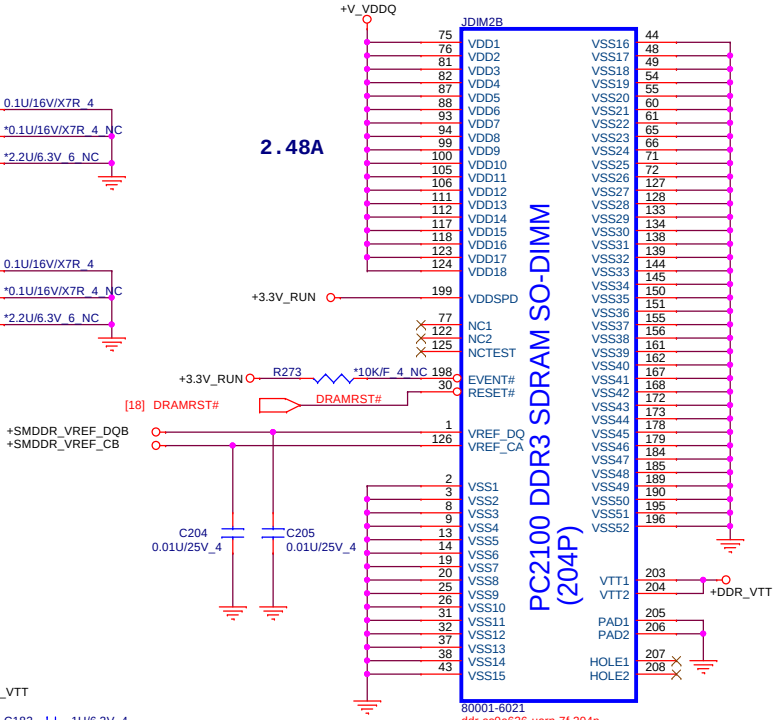
Place these Caps near So-Dimm2.



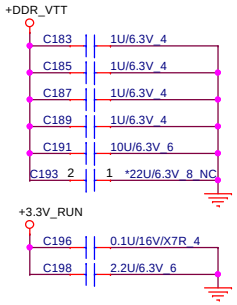
H = 9.2mm



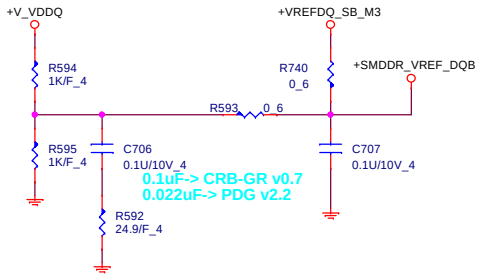
2.48A

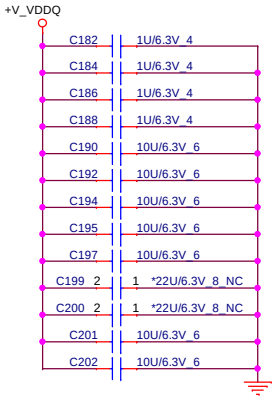


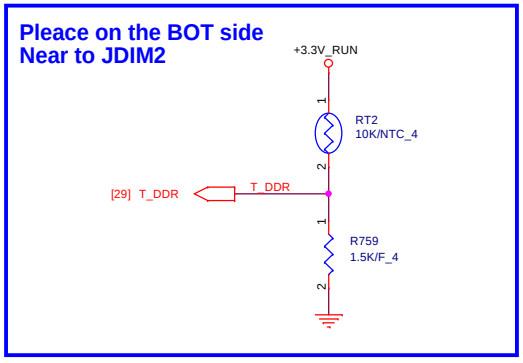
H = 9.2mm



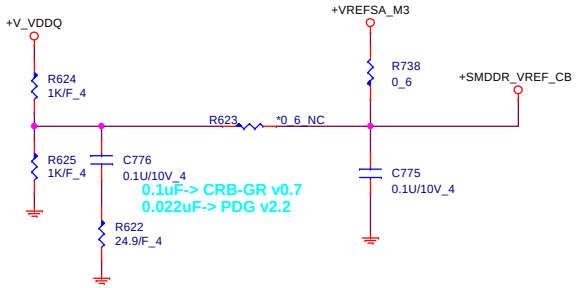
M3 VREF + M1 VREF







VREF SA1 M1/M3 Solution



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U14A
N15P-GT

[PEG Interface]

PEX_IOVDD/Q : 3300mA
+1.05V_GFX

To be placed no further from the GPU than bewteen the PS and GPU
C212 22U/6.3V_6
C213 22U/6.3V_6
C214 22U/6.3V_6
C215 22U/6.3V_6
C216 10U/6.3V_6
C217 10U/6.3V_6
C218 10U/6.3V_6
C219 10U/6.3V_6

PLACE NEAR BALLS
C220 1U/6.3V_4
C221 1U/6.3V_4
C222 1U/6.3V_4
C224 1U/6.3V_4

PLACE UNDER BGA
C225 4.7U/6.3V_4
C227 4.7U/6.3V_4

AG19 PEX_IOVDD_1
AG21 PEX_IOVDD_2
AG22 PEX_IOVDD_3
AG24 PEX_IOVDD_4
AH21 PEX_IOVDD_5
AH25 PEX_IOVDD_6
AG13 PEX_IOVDDQ_1
AG15 PEX_IOVDDQ_2
AG16 PEX_IOVDDQ_3
AG18 PEX_IOVDDQ_4
AG25 PEX_IOVDDQ_5
AH15 PEX_IOVDDQ_6
AH18 PEX_IOVDDQ_7
AH26 PEX_IOVDDQ_8
AH27 PEX_IOVDDQ_9
AJ27 PEX_IOVDDQ_10
AK27 PEX_IOVDDQ_11
AL27 PEX_IOVDDQ_12
AM28 PEX_IOVDDQ_13
AN28 PEX_IOVDDQ_14

PEX_RX0 AN12 PEG_TXP0_C C677 2 1 0.22U/16V_4 PEG_TXP0 PEG_TXP0 [7]
PEX_RX0_N AM12 PEG_TXN0_C C668 2 1 0.22U/16V_4 PEG_TXN0 PEG_TXN0 [7]
PEX_RX1 AN14 PEG_TXP1_C C679 2 1 0.22U/16V_4 PEG_TXP1 PEG_TXP1 [7]
PEX_RX1_N AM14 PEG_TXN1_C C669 2 1 0.22U/16V_4 PEG_TXN1 PEG_TXN1 [7]
PEX_RX2 AP14 PEG_TXP2_C C678 2 1 0.22U/16V_4 PEG_TXP2 PEG_TXP2 [7]
PEX_RX2_N AP15 PEG_TXN2_C C670 2 1 0.22U/16V_4 PEG_TXN2 PEG_TXN2 [7]
PEX_RX3 AN15 PEG_TXP3_C C681 2 1 0.22U/16V_4 PEG_TXP3 PEG_TXP3 [7]
PEX_RX3_N AM15 PEG_TXN3_C C671 2 1 0.22U/16V_4 PEG_TXN3 PEG_TXN3 [7]
PEX_RX4 AN17 PEG_TXP4_C C680 2 1 0.22U/16V_4 PEG_TXP4 PEG_TXP4 [7]
PEX_RX4_N AM17 PEG_TXN4_C C673 2 1 0.22U/16V_4 PEG_TXN4 PEG_TXN4 [7]
PEX_RX5 AP17 PEG_TXP5_C C682 2 1 0.22U/16V_4 PEG_TXP5 PEG_TXP5 [7]
PEX_RX5_N AP18 PEG_TXN5_C C672 2 1 0.22U/16V_4 PEG_TXN5 PEG_TXN5 [7]
PEX_RX6 AN18 PEG_TXP6_C C683 2 1 0.22U/16V_4 PEG_TXP6 PEG_TXP6 [7]
PEX_RX6_N AM18 PEG_TXN6_C C674 2 1 0.22U/16V_4 PEG_TXN6 PEG_TXN6 [7]
PEX_RX7 AN20 PEG_TXP7_C C684 2 1 0.22U/16V_4 PEG_TXP7 PEG_TXP7 [7]
PEX_RX7_N AM20 PEG_TXN7_C C675 2 1 0.22U/16V_4 PEG_TXN7 PEG_TXN7 [7]
PEX_RX8 AP20
PEX_RX8_N AP21
PEX_RX9 AN21
PEX_RX9_N AM21
PEX_RX10 AN23
PEX_RX10_N AM23
PEX_RX11 AP23
PEX_RX11_N AP24
PEX_RX12 AN24
PEX_RX12_N AM24
PEX_RX13 AN26
PEX_RX13_N AM26
PEX_RX14 AP26
PEX_RX14_N AP27
PEX_RX15 AN27
PEX_RX15_N AM27

PEX_TX0 AK14 PEG_RXP0_C C695 2 1 0.22U/16V_4 PEG_RXP0 [7]
PEX_TX0_N AJ14 PEG_RXN0_C C685 2 1 0.22U/16V_4 PEG_RXN0 [7]
PEX_TX1 AH14 PEG_RXP1_C C700 2 1 0.22U/16V_4 PEG_RXP1 [7]
PEX_TX1_N AG14 PEG_RXN1_C C687 2 1 0.22U/16V_4 PEG_RXN1 [7]
PEX_TX2 AK15 PEG_RXP2_C C693 2 1 0.22U/16V_4 PEG_RXP2 [7]
PEX_TX2_N AJ15 PEG_RXN2_C C688 2 1 0.22U/16V_4 PEG_RXN2 [7]
PEX_TX3 AL16 PEG_RXP3_C C696 2 1 0.22U/16V_4 PEG_RXP3 [7]
PEX_TX3_N AK16 PEG_RXN3_C C686 2 1 0.22U/16V_4 PEG_RXN3 [7]
PEX_TX4 AK17 PEG_RXP4_C C694 2 1 0.22U/16V_4 PEG_RXP4 [7]
PEX_TX4_N AJ17 PEG_RXN4_C C689 2 1 0.22U/16V_4 PEG_RXN4 [7]
PEX_TX5 AH17 PEG_RXP5_C C698 2 1 0.22U/16V_4 PEG_RXP5 [7]
PEX_TX5_N AG17 PEG_RXN5_C C690 2 1 0.22U/16V_4 PEG_RXN5 [7]
PEX_TX6 AK18 PEG_RXP6_C C699 2 1 0.22U/16V_4 PEG_RXP6 [7]
PEX_TX6_N AJ18 PEG_RXN6_C C692 2 1 0.22U/16V_4 PEG_RXN6 [7]
PEX_TX7 AL19 PEG_RXP7_C C697 2 1 0.22U/16V_4 PEG_RXP7 [7]
PEX_TX7_N AK19 PEG_RXN7_C C691 2 1 0.22U/16V_4 PEG_RXN7 [7]
PEX_TX8 AK20
PEX_TX8_N AJ20
PEX_TX9 AH20
PEX_TX9_N AG20
PEX_TX10 AK21
PEX_TX10_N AJ21
PEX_TX11 AL22
PEX_TX11_N AK22
PEX_TX12 AK23
PEX_TX12_N AJ23
PEX_TX13 AH23
PEX_TX13_N AG23
PEX_TX14 AK24
PEX_TX14_N AJ24
PEX_TX15 AL25
PEX_TX15_N AK25

AC6 NC_1
AJ28 NC_2
AJ4 NC_3
AJ5 NC_4
AL11 NC_5
C15 NC_6
D19 NC_7
D20 NC_8
D23 NC_9
D26 NC_10
H31 NC_11
T8 NC_12
V32 NC_13
Y1 NC_14
Y2 NC_15
Y3 NC_16
AA1 NC_17
AA2 NC_18
AA3 NC_19
AA4 NC_20
AA5 NC_21
AA6 NC_22
AA7 NC_23
AA8 NC_24

PLACE CLOSE TO BGA
C244 4.7U/6.3V_4
C245 1U/6.3V_4
C246 0.1U/10V_4
C782 *0.1U/10V_4_NC
C783 *0.1U/10V_4_NC
PLACE CLOSE TO GPU BALLS

+3V_AON
+3V_GFX
VDD33 : 85mA
J8 3V3_AON_1
K8 3V3_AON_2
L8 3V3_MAIN_1
M8 3V3_MAIN_2

PLACE CLOSE TO BGA
C247 4.7U/6.3V_4
C248 1U/6.3V_4
PLACE CLOSE TO GPU BALLS
C249 0.1U/10V_4
C250 0.1U/10V_4
C781 *0.1U/10V_4_NC

PEX_REFCLK AL13 CLK_PCIE_VGAP [14]
PEX_REFCLK_N AK13 CLK_PCIE_VGAN [14]

DG-06803-001_V04 : R305 is unstuffed
E2703.DSN : R305 is stuffed

PEX_TSTCLK_OUT AJ26 PEX_TSTCLK R305 *200_4_NC
PEX_TSTCLK_OUT_N AK26 PEX_TSTCLK#

DVT2
NC AJ11
PEX_RST_N AJ12 GPU_PEX_RST# R306 1 2 PEGX_RST#
*SJ0402_NC

PEX_CLKREQ_N AK12 PEX_CLKREQ# R307 10K_4 +3V_AON

PEX_TERMP AP29 PEX_TERMP R308 2.49K/F_4

TESTMODE AK11 TESTMODE R310 10K_4

PEX_PLLVDD AG26 PEX_PLLVDD
PEX_PLLVDD : 150mA

PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12
PEX_SVDD_3V3 : 210mA
+3V_AON
0.1U/10V_4 C253
4.7U/6.3V_4 C254
4.7U/6.3V_4 C256
PLACE NEAR BGA

3.3V_AUX_NC P8 3.3V_AUX

VDD_SENSE L4 VGPU_CORE_SENSE [50]
GND_SENSE L5 VSS_GPU_SENSE [50]

+1.05V_GFX
R309 0_6
C251 4.7U/6.3V_4 PLACE NEAR GPU
C252 1U/6.3V_4 PLACE NEAR GPU
C255 0.1U/10V_4 PLACE UNDER GPU BALLS

3.3V_AUX TP141

+3V_GFX
R632 *0_4_NC
R631 0_4
[15,24] DGPU_PWROK
PEX_CLKREQ#
Q18 2N7002W
CLK_PEGA_REQ# [14]

[23] SYS_PEX_RST_MON#
+3.3V_RUN
C223 0.1U/10V_4
74AHC1G09GW U15
[12,29,41,42] PLTRST#
[12] DGPU_HOLD_RST#
RST_MON# R302 1 2 *SJ0402_NC
DVT2
[23] GPU_PEX_RST_HOLD#

+3.3V_RUN
+3V_AON
C226 0.1U/10V_4
U16 MC74VHC1G08DFT2G
R630 *10K_4_NC
R304 100K_4
PEGX_RST# [23]

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U14B
N15P-GT

[MEMORY I/F A]

U14C
N15P-GT

MEMORY I/F C

PLACE CLOSE TO GPU BALLS

PLACE CLOSE TO BGA

WCK only for GDDR5

DVT2

+FB_PLLAVDD : 62mA

C273 close to K27 (under GPU)

C276 close to U27 (under GPU)

C274 near to GPU

C275 close to H27 (under GPU)

PLACE CLOSE TO GPU BALLS

FBB_WCKBxx are reserved
NC ON : GM108/GM107

USED ON : GK107

GK107	GM107
FBB_DEBUG0	FBA_CMD32
FBB_DEBUG1	FBA_CMD33
NC	FBA_CMD34
NC	FBA_CMD35

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U14D
N15P-GT

[IFPA/B_LVDS]
AH8 IFPAB_PLLVDD
AG8 IFPA_IOVDD
AG9 IFPB_IOVDD
AJ8 IFPAB_RSET
IFPA_TXC AM6
IFPA_TXC_N AN6
IFPA_TXD0 AP3
IFPA_TXD0_N AN3
IFPA_TXD1 AN5
IFPA_TXD1_N AM5
IFPA_TXD2 AL6
IFPA_TXD2_N AK6
IFPA_TXD3 AJ6
IFPA_TXD3_N AH6
IFPB_TXC AJ9
IFPB_TXC_N AH9
IFPB_TXD4 AP6
IFPB_TXD4_N AP5
IFPB_TXD5 AM7
IFPB_TXD5_N AL7
IFPB_TXD6 AN8
IFPB_TXD6_N AM8
IFPB_TXD7 AK8
IFPB_TXD7_N AL8

[IFPC/D_TMDS]
AF7 IFPC_PLLVDD
AG7 IFPD_PLLVDD
AF6 IFPC_IOVDD
AG6 IFPD_IOVDD
AF8 IFPC_RSET
AN2 NC
IFPD_RSET
GM107 GK1077/GK208
IFPC_AUX_I2CW_SCL AG3
IFPC_AUX_I2CW_SDA_N AG2
IFPC_L0 AK1
IFPC_L0_N AJ1
IFPC_L1 AJ3
IFPC_L1_N AJ2
IFPC_L2 AH3
IFPC_L2_N AH4
IFPC_L3 AG5
IFPC_L3_N AG4
IFPD_AUX_I2CX_SCL AK3
IFPD_AUX_I2CX_SDA_N AK2
IFPD_L0 AM1
IFPD_L0_N AM2
IFPD_L1 AM3
IFPD_L1_N AM4
IFPD_L2 AL3
IFPD_L2_N AL4
IFPD_L3 AK4
IFPD_L3_N AK5

[IFPE/F_DP]
AB8 IFPEF_PLLVDD
AC7 IFPE_IOVDD
AC8 IFPF_IOVDD
AD6 IFPEF_RSET
IFPE_AUX_I2CY_SCL AB3
IFPE_AUX_I2CY_SDA_N AB4
IFPE_L0 AD2
IFPE_L0_N AD3
IFPE_L1 AD1
IFPE_L1_N AC1
IFPE_L2 AC2
IFPE_L2_N AC3
IFPE_L3 AC4
IFPE_L3_N AC5
IFPF_AUX_I2CZ_SCL AF3
IFPF_AUX_I2CZ_SDA_N AF2
IFPF_L0 AE3
IFPF_L0_N AE4
IFPF_L1 AF4
IFPF_L1_N AF5
IFPF_L2 AD4
IFPF_L2_N AD5
IFPF_L3 AG1
IFPF_L3_N AF1

[DACA/B_CRT]
AG10 DACA_VDD
AP9 DACA_VREF
AP8 DACA_RSET
DACA_RED AK9
DACA_GREEN AL10
DACA_BLUE AL9
DACA_HSYNC AM9
DACA_VSYNC AN9
I2CA_SCL
I2CA_SDA

[XTAL IN]
XTAL_IN H3
XTAL_OUT H2
XTAL_OUTBUFF J4
XTAL_SSIN H1

R4 I2CA_SCL 1.8K/F_4 R329
R5 I2CA_SDA 1.8K/F_4 R330

R657 1 2 *0_4_NC
+3.3V_RUN
+3V_GFX
+3V_AON
U62 MC74VHC1G08DFT2G
3V3_MAIN_PWRGD [50]
R646 10K/F_4
C818 0.1U/16V/X7R_4

XTAL27_IN
XTAL27_OUT
Y3
27MHZ +-10PPM
C277 10P/50V_4
C278 8.2p/50V_4

Reserve
+3V_AON
XTAL_OUTBUFF R640 *10K_4_NC

DVT2
PLACE CLOSE TO GPU
PLACE CLOSE TO BALLS
+1.05V_GFX
L3 HCB1005KF-330T30
C279 22U/6.3V_6
C280 0.1U/16V/X7R_4
NV_PLLVDD AD8 PLLVDD
PLLVDD : 200mA
PLLVDD AE8 SP_PLLVDD
DVT2
+1.05V_GFX
L4 HCB1005KF-181T15
C281 22U/6.3V_6
C282 4.7U/6.3V_4
C283 0.1U/16V/X7R_4
C284 0.1U/16V/X7R_4
C283 Close to AE8
C284 Close to AD7
AD7 VID_PLLVDD

XTAL_IN H3 XTAL27_IN
XTAL_OUT H2 XTAL27_OUT
XTAL_OUTBUFF J4 XTAL_OUTBUFF RP28 2 4 1 3 10KX2
XTAL_SSIN H1 XTAL_SSIN

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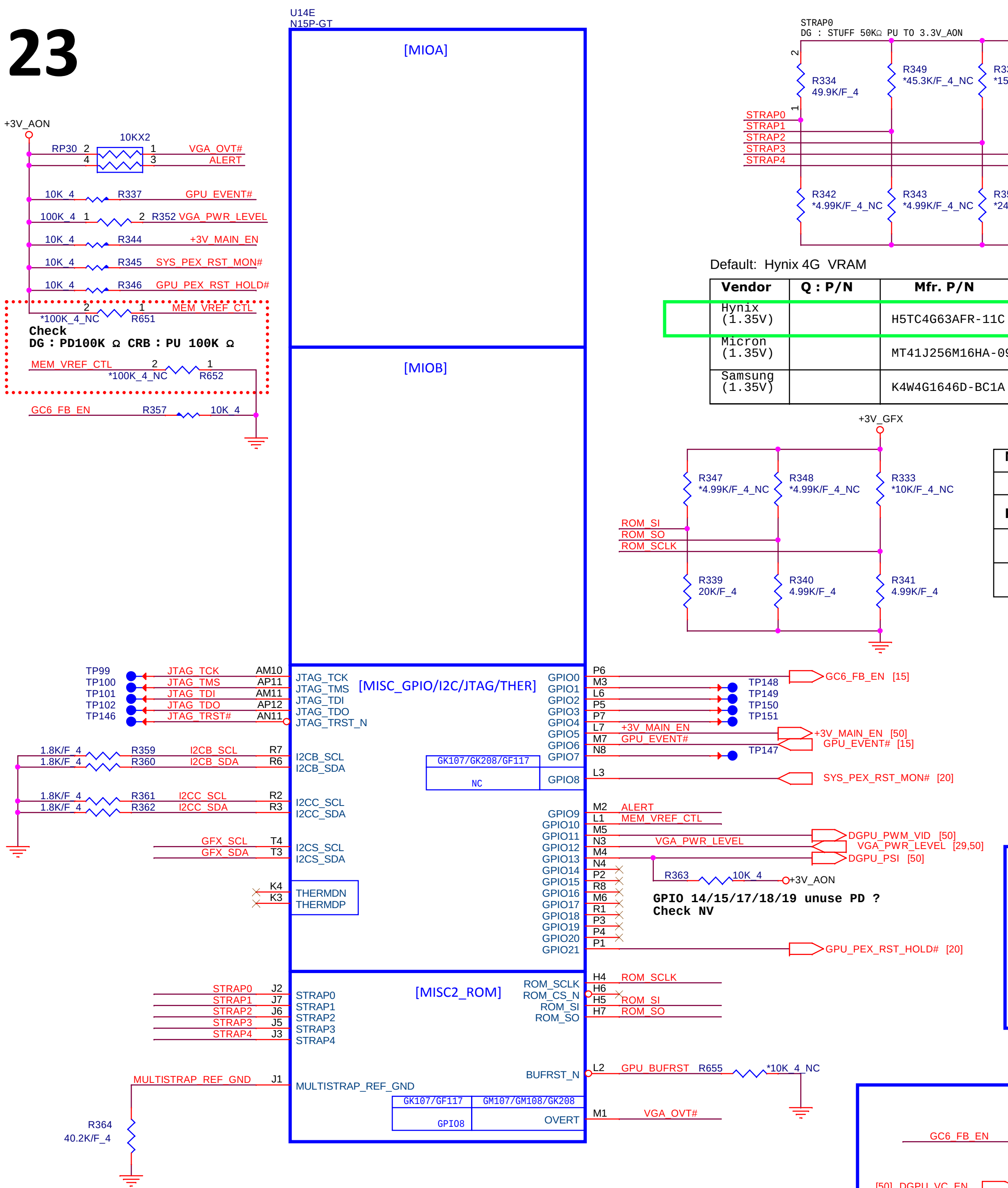


U14E
N15P-GT
[MIOA]
[MIOB]
[MISC_GPIO/I2C/JTAG/THER]
[MISC2_ROM]
STRAP0
DG : STUFF 50KΩ PU TO 3.3V_AON
+3V_AON
R334 49.9K/F_4
R349 *45.3K/F_4_NC
R335 *15K/F_4_NC
R350 *34.8K/F_4_NC
R336 *20K/F_4_NC
R342 *4.99K/F_4_NC
R343 *4.99K/F_4_NC
R353 *24.9K/F_4_NC
R354 *4.99K/F_4_NC
R355 *45.3K/F_4_NC
STRAP0
STRAP1
STRAP2
STRAP3
STRAP4
RP30 10KX2
VGA_OVT#
ALERT
10K_4 R337 GPU_EVENT#
100K_4 R352 VGA_PWR_LEVEL
10K_4 R344 +3V_MAIN_EN
10K_4 R345 SYS_PEX_RST_MON#
10K_4 R346 GPU_PEX_RST_HOLD#
*100K_4_NC R651 MEM_VREF_CTL
Check
DG : PD100K Ω CRB : PU 100K Ω
MEM_VREF_CTL *100K_4_NC R652
GC6_FB_EN R357 10K_4
+3V_GFX
R347 *4.99K/F_4_NC
R348 *4.99K/F_4_NC
R333 *10K/F_4_NC
ROM_SI
ROM_SO
ROM_SCLK
R339 20K/F_4
R340 4.99K/F_4
R341 4.99K/F_4
TP99 JTAG_TCK AM10
TP100 JTAG_TMS AP11
TP101 JTAG_TDI AM11
TP102 JTAG_TDO AP12
TP146 JTAG_TRST# AN11
1.8K/F_4 R359 I2CB_SCL R7
1.8K/F_4 R360 I2CB_SDA R6
1.8K/F_4 R361 I2CC_SCL R2
1.8K/F_4 R362 I2CC_SDA R3
GFX_SCL T4
GFX_SDA T3
K4 K3 THERMDN THERMDP
GK107/GK208/GF117 NC
GPIO0 P6 GC6_FB_EN [15]
GPIO1 M3 TP148
GPIO2 L6 TP149
GPIO3 P5 TP150
GPIO4 P7 TP151
GPIO5 L7 +3V_MAIN_EN [50]
GPIO6 M7 GPU_EVENT# [15]
GPIO7 N8 TP147
GPIO8 L3 SYS_PEX_RST_MON# [20]
GPIO9 M2 ALERT
GPIO10 L1 MEM_VREF_CTL
GPIO11 M5 DGPU_PWM_VID [50]
GPIO12 N3 VGA_PWR_LEVEL [29,50]
GPIO13 M4 DGPU_PSI [50]
GPIO14 N4
GPIO15 P2 R363 10K_4 +3V_AON
GPIO16 R8
GPIO17 M6
GPIO18 R1
GPIO19 P3
GPIO20 P4
GPIO21 P1 GPU_PEX_RST_HOLD# [20]
GPIO 14/15/17/18/19 unuse PD ?
Check NV
STRAP0 J2
STRAP1 J7
STRAP2 J6
STRAP3 J5
STRAP4 J3
ROM_SCLK H4
ROM_CS_N H6
ROM_SI H5
ROM_SO H7
MULTISTRAP_REF_GND J1
R364 40.2K/F_4
BUFRST_N L2 GPU_BUFRST R655 *10K_4_NC
GK107/GF117 GM107/GM108/GK208
GPIO8 OVERT M1 VGA_OVT#

4.99K/F_4: CS24992FB26 RES CHIP 4.99K 1/16W +1%(0402)
10K/F_4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)
15K/F_4: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
24.9K/F_4: CS32492FB16 RES CHIP 24.9K 1/16W +-1%(0402)
30.1K/F_4: CS33012FB18 RES CHIP 30.1K 1/16W +-1%(0402)
34.8K/F_4: CS33482FB22 RES CHIP 34.8K 1/16W +-1% (0402)
45.3K/F_4: CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)

Logical Strap Bit Mapping

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Default: Hynix 4G VRAM

Vendor	Q : P/N	Mfr. P/N	ROM_SI	
Hynix (1.35V)		H5TC4G63AFR-11C	0011	20K PD
Micron (1.35V)		MT41J256M16HA-093G:E	0100	24.9K PD
Samsung (1.35V)		K4W4G1646D-BC1A	0101	30.1K PD

N15P-GT device ID= 0x1391		
Netname	N15P-GT	
ROM_SCLK	4.99K PD	0000
ROM_SO	4.99K PD	0000
STRAP0	45.3K PU	

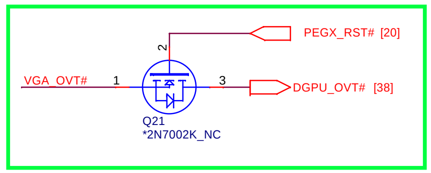
Table 15-3. GB2B-64 and GB4B-128 Multi-level Mode Strapping

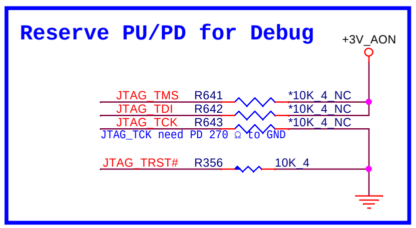
Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND and stuff 50kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND for forward compatibility.			

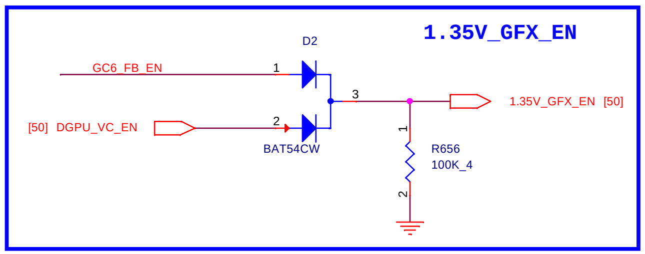
Table 28. N15S-GX and N15P-GT DDR3L Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
256M×16 DDR3L	Hynix	0x3	1.35 V/ 1.35 V	H5TC4G63AFR-11C	900	N/A	Production candidate
	Micron	0x4	1.35 V/ 1.35 V	MT41J256M16HA-093G:E	900	1322	Production candidate
	Samsung	0x5	1.35V/ 1.35V	K4W4G1646D-BC1A	900	N/A	Post-production candidate

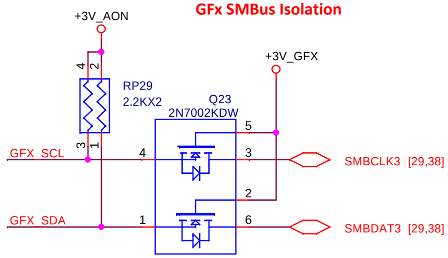
Note: For N15S-GX and N15P-GT, the maximum allowable memory case temperature is 85 °C.







GFx SMBus Isolation



VDD/XVDD : 43A

+VGACORE

U14F
N15P-GT

[GPU VDD]

AA12	VDD_001	XVDD_001	U1
AA14	VDD_002	XVDD_002	U2
AA16	VDD_003	XVDD_003	U3
AA19	VDD_004	XVDD_004	U4
AA21	VDD_005	XVDD_005	U5
AA23	VDD_006	XVDD_006	U6
AB13	VDD_007	XVDD_007	U7
AB15	VDD_008	XVDD_008	U8
AB17	VDD_009	XVDD_009	V1
AB18	VDD_010	XVDD_010	V2
AB20	VDD_011	XVDD_011	V3
AB22	VDD_012	XVDD_012	V4
AC12	VDD_013	XVDD_013	V5
AC14	VDD_014	XVDD_014	V6
AC16	VDD_015	XVDD_015	V7
AC19	VDD_016	XVDD_016	V8
AC21	VDD_017	XVDD_017	W2
AC23	VDD_018	XVDD_018	W3
M12	VDD_019	XVDD_019	W4
M14	VDD_020	XVDD_020	W5
M16	VDD_021	XVDD_021	W7
M19	VDD_022	XVDD_022	W8
M21	VDD_023	XVDD_026	Y4
M23	VDD_024	XVDD_027	Y5
N13	VDD_025	XVDD_028	Y6
N15	VDD_026	XVDD_029	Y7
N17	VDD_027	XVDD_030	Y8
N18	VDD_028		
N20	VDD_029		
N22	VDD_030		
P12	VDD_031		
P14	VDD_032		
P16	VDD_033		
P19	VDD_034		
P21	VDD_035		
P23	VDD_036		
R13	VDD_037		
R15	VDD_038		
R17	VDD_039		
R18	VDD_040		
R20	VDD_041		
R22	VDD_042		
T12	VDD_043		
T14	VDD_044		
T16	VDD_045		
T19	VDD_046		
T21	VDD_047		
T23	VDD_048		
U13	VDD_049		
U15	VDD_050		
U17	VDD_051		
U18	VDD_052		
U20	VDD_053		
U22	VDD_054		
V13	VDD_055		
V15	VDD_056		
V17	VDD_057		
V18	VDD_058		
V20	VDD_059		
V22	VDD_060		
W12	VDD_061		
W14	VDD_062		
W16	VDD_063		
W19	VDD_064		
W21	VDD_065		
W23	VDD_066		
Y13	VDD_067		
Y15	VDD_068		
Y18	VDD_069		
Y17	VDD_070		
Y20	VDD_071		
Y22	VDD_072		

U14G
N15P-GT

[GPU GND]

A2	GND_1	GND_101	D2
AA17	GND_2	GND_102	D31
AA18	GND_3	GND_103	D33
AA20	GND_4	GND_104	E10
AA22	GND_5	GND_105	E22
AB12	GND_6	GND_106	E25
AB14	GND_7	GND_107	E5
AB16	GND_8	GND_108	E7
AB19	GND_9	GND_109	F28
AB2	GND_10	GND_110	F7
AB21	GND_11	GND_111	G10
A33	GND_12	GND_112	G13
AB23	GND_13	GND_113	G16
AB28	GND_14	GND_114	G19
AB30	GND_15	GND_115	G2
AB32	GND_16	GND_116	G22
AB5	GND_17	GND_117	G25
AB7	GND_18	GND_118	G28
AC13	GND_19	GND_119	G3
AC15	GND_20	GND_120	G30
AC17	GND_21	GND_121	G32
AC18	GND_22	GND_122	G33
AA13	GND_23	GND_123	G5
AC20	GND_24	GND_124	G7
AC22	GND_25	GND_125	K2
AE2	GND_26	GND_126	K28
AE28	GND_27	GND_127	K30
AE30	GND_28	GND_128	K32
AE32	GND_29	GND_129	K33
AE33	GND_30	GND_130	K5
AE5	GND_31	GND_131	K7
AE7	GND_32	GND_132	M13
AH10	GND_33	GND_133	M15
AA15	GND_34	GND_134	M17
AH13	GND_35	GND_135	M18
AH16	GND_36	GND_136	M20
AH19	GND_37	GND_137	M22
AH2	GND_38	GND_138	N12
AH22	GND_39	GND_139	N14
AH24	GND_40	GND_140	N16
AH28	GND_41	GND_141	N19
AH29	GND_42	GND_142	N2
AH30	GND_43	GND_143	N21
AH32	GND_44	GND_144	N23
AH33	GND_45	GND_145	N28
AH5	GND_46	GND_146	N30
AH7	GND_47	GND_147	N32
AJ7	GND_48	GND_148	N33
AK10	GND_49	GND_149	N5
AK7	GND_50	GND_150	N7
AL12	GND_51	GND_151	P13
AL14	GND_52	GND_152	P15
AL15	GND_53	GND_153	P17
AL17	GND_54	GND_154	P18
AL18	GND_55	GND_155	P20
AL2	GND_56	GND_156	P22
AL20	GND_57	GND_157	R12
AL21	GND_58	GND_158	R14
AL23	GND_59	GND_159	R16
AL24	GND_60	GND_160	R19
AL26	GND_61	GND_161	R21
AL28	GND_62	GND_162	R23
AL30	GND_63	GND_163	T13
AL32	GND_64	GND_164	T15
AL33	GND_65	GND_165	T17
AL5	GND_66	GND_166	T18
AM13	GND_67	GND_167	T2
AM16	GND_68	GND_168	T20
AM19	GND_69	GND_169	T22
AM22	GND_70	GND_170	AG11
AM25	GND_71	GND_171	T28
AN1	GND_72	GND_172	T32
AN10	GND_73	GND_173	T5
AN13	GND_74	GND_174	T7
AN16	GND_75	GND_175	U12
AN19	GND_76	GND_176	U14
AN22	GND_77	GND_177	U16
AN25	GND_78	GND_178	U19
AN30	GND_79	GND_179	U21
AN34	GND_80	GND_180	U23
AN4	GND_81	GND_181	V12
AN7	GND_82	GND_182	V14
AP2	GND_83	GND_183	V16
AP33	GND_84	GND_184	V19
B1	GND_85	GND_185	V21
B10	GND_86	GND_186	V23
B22	GND_87	GND_187	W13
B25	GND_88	GND_188	W15
B28	GND_89	GND_189	W17
B31	GND_90	GND_190	W18
B34	GND_91	GND_191	W20
B4	GND_92	GND_192	W22
B7	GND_93	GND_193	W28
C10	GND_94	GND_194	Y12
C13	GND_95	GND_195	Y14
C19	GND_96	GND_196	Y16
C22	GND_97	GND_197	Y19
C25	GND_98	GND_198	Y21
C28	GND_99	GND_199	Y23
C7	GND_100	GND_200	AH11
		GND_OPT_1	C16
		GND_OPT_2	W32

+VGACORE

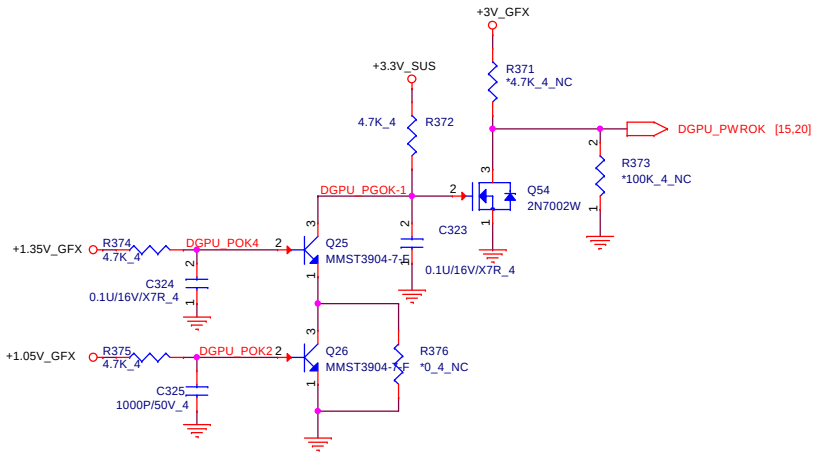
PLACE UNDER GPU

C286	1U/6.3V_4
C287	1U/6.3V_4
C288	1U/6.3V_4
C289	1U/6.3V_4
C290	1U/6.3V_4
C291	1U/6.3V_4
C292	1U/6.3V_4
C293	1U/6.3V_4
C294	4.7U/6.3V/X6S_6
C295	4.7U/6.3V/X6S_6
C296	4.7U/6.3V/X6S_6
C297	4.7U/6.3V/X6S_6
C298	4.7U/6.3V/X6S_6
C299	4.7U/6.3V/X6S_6
C300	4.7U/6.3V/X6S_6
C301	4.7U/6.3V/X6S_6
C302	4.7U/6.3V/X6S_6
C303	4.7U/6.3V/X6S_6
C304	4.7U/6.3V/X6S_6
C305	4.7U/6.3V/X6S_6
C306	4.7U/6.3V/X6S_6
C307	4.7U/6.3V/X6S_6
C308	4.7U/6.3V/X6S_6

PLACE NEAR GPU

C26	2	1	22U/6.3V_8
C27	2	1	22U/6.3V_8
C28	2	1	22U/6.3V_8
C29	2	1	22U/6.3V_8
C30	2	1	22U/6.3V_8
C31	2	1	22U/6.3V_8
C32	2	1	22U/6.3V_6
C316			4.7U/6.3V/X6S_6
C317			4.7U/6.3V/X6S_6
C318			4.7U/6.3V/X6S_6
C319			4.7U/6.3V/X6S_6
C320			4.7U/6.3V/X6S_6

DVT2



Quanta Computer Inc.

PROJECT : AM7

Size	Document Number	Rev
	N15P-GT - 5/5 (Power)	C0

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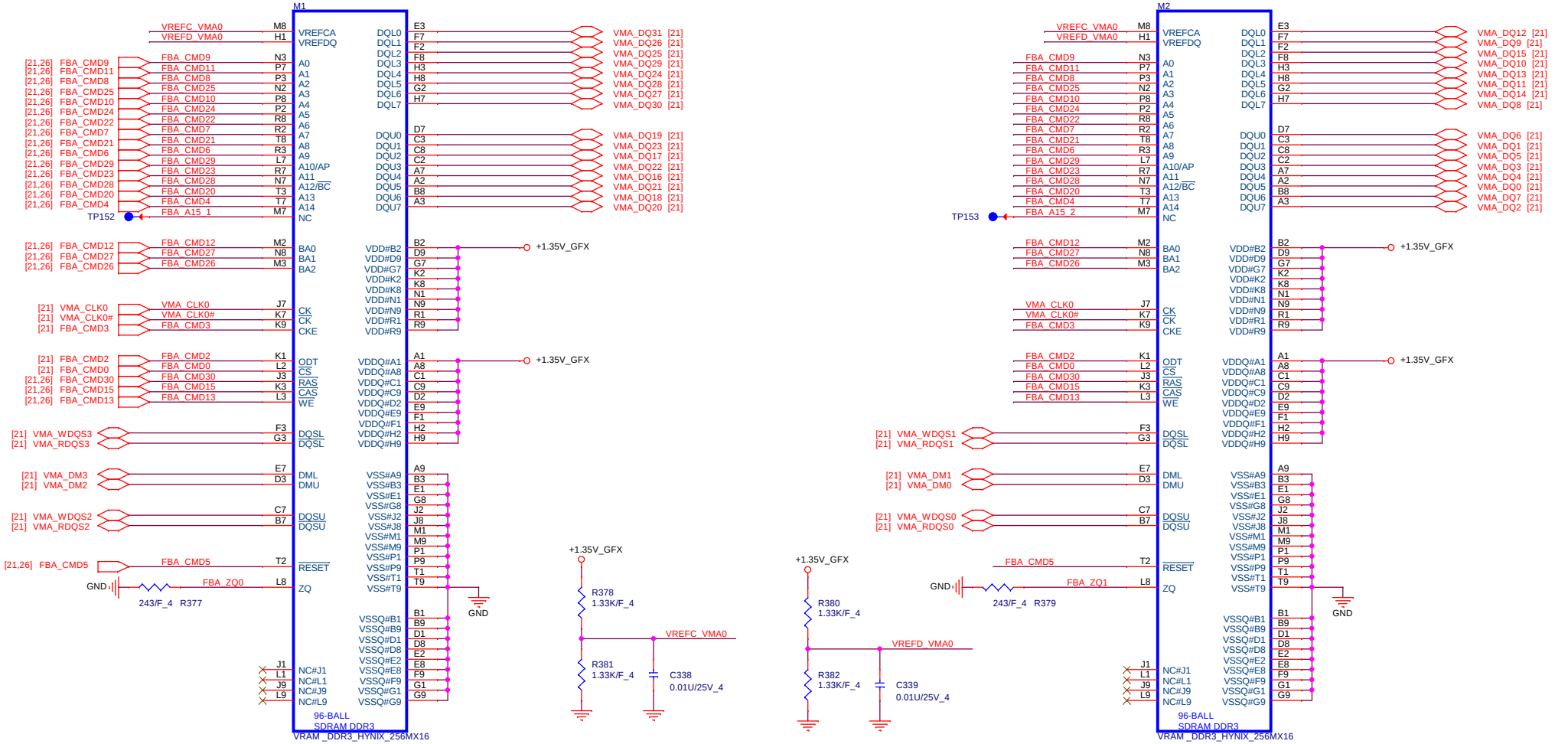
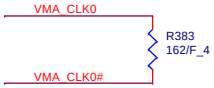
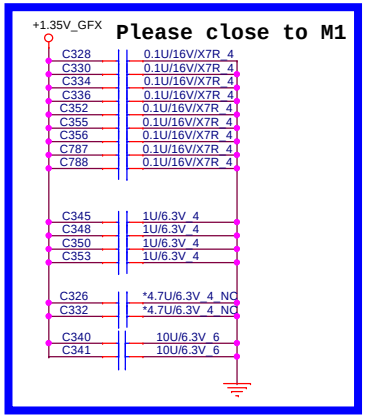
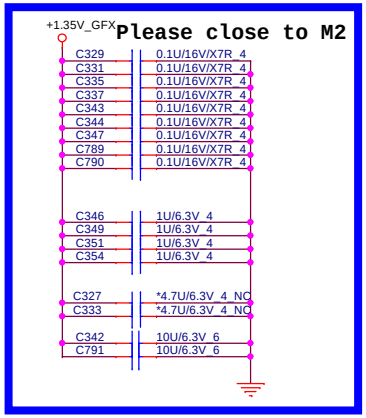
HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW05---WINBSQ PN : AKD5PGWTW11
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL02---WINBSQ PN :
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT500---WINBSQ PN : NO



162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)







Quanta Computer Inc.
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Size	Document Number	Rev
	N15P-GT_DDR3L - A1	C0

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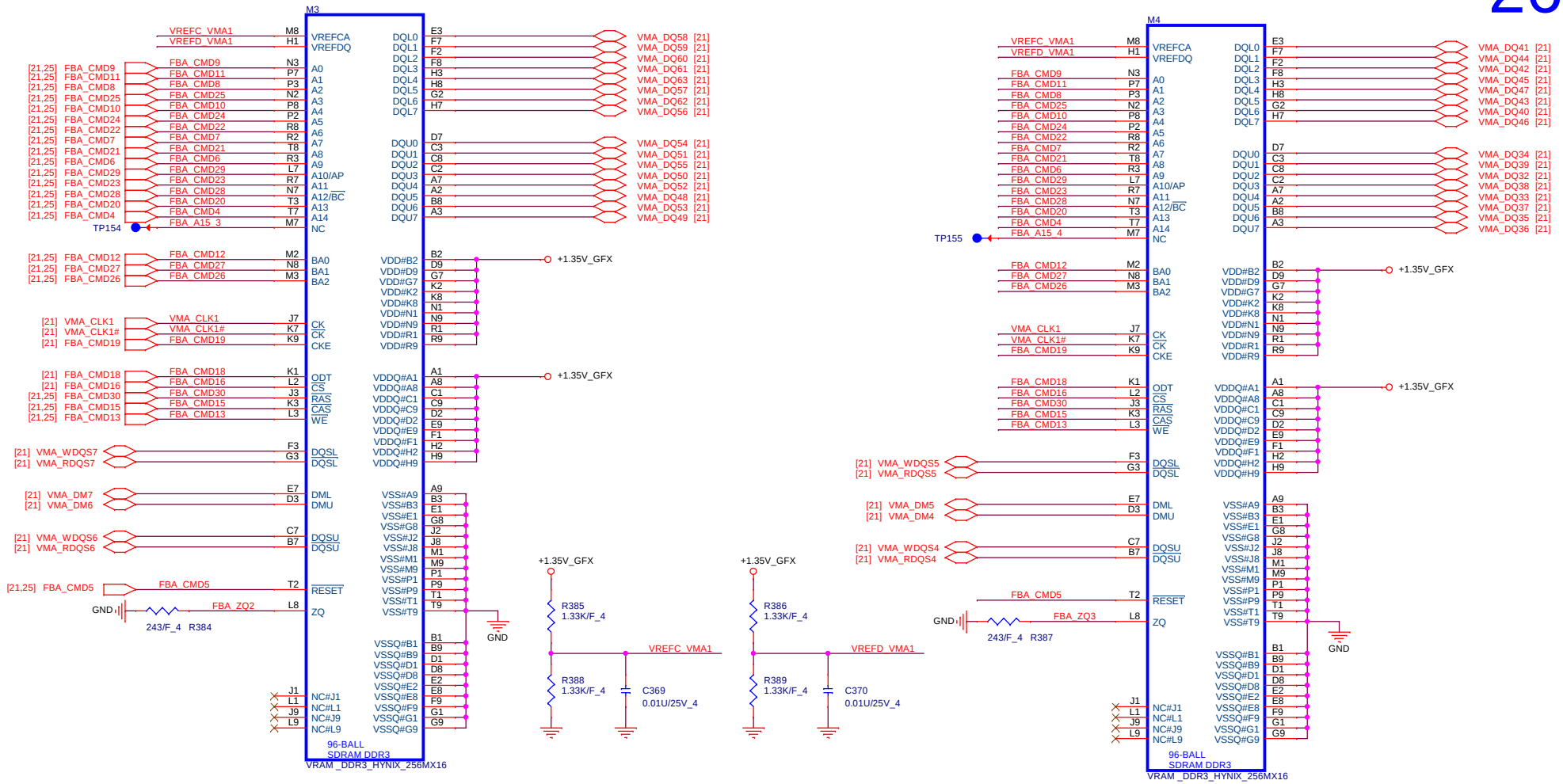
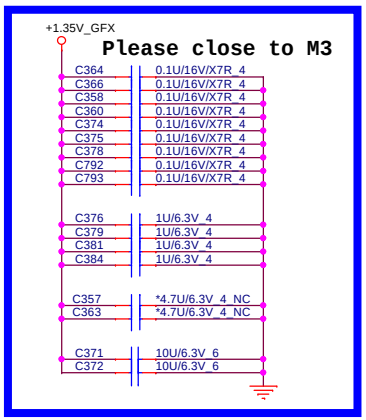
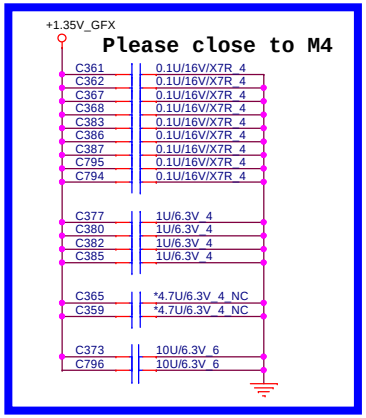
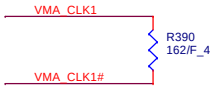






162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)



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Size	Document Number	Rev
	N15P-GT_ DDR3L - A2	C0

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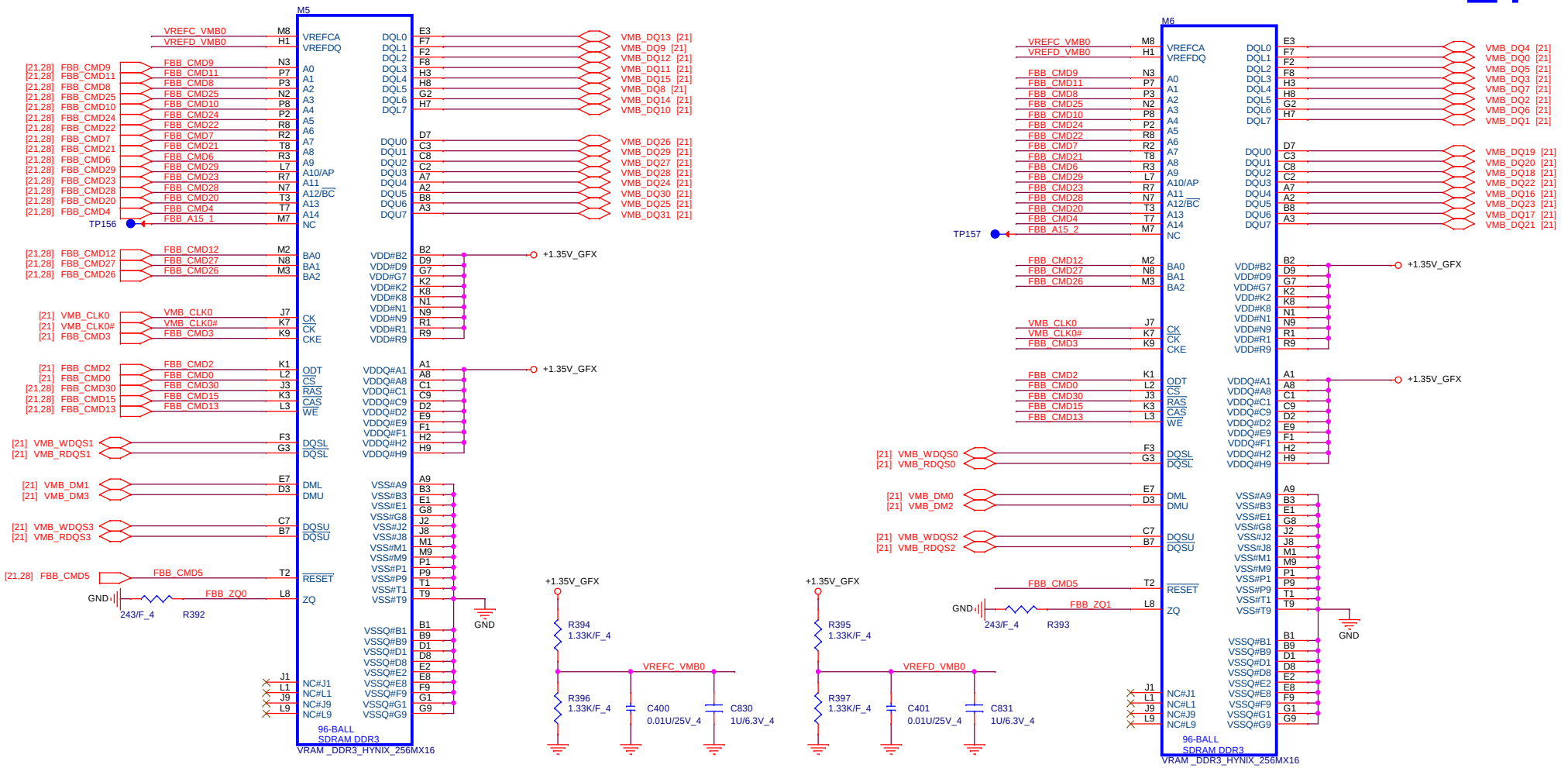
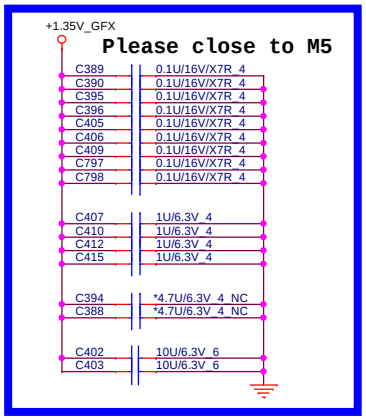
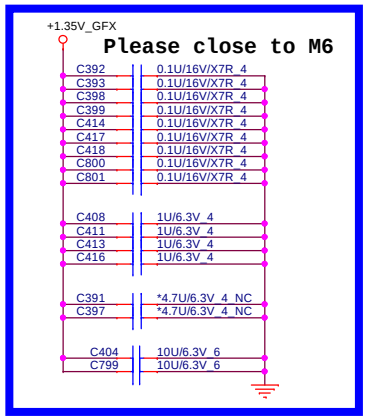
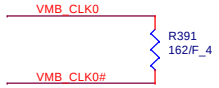






162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)



Quanta Computer Inc.
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Size	Document Number	Rev
	N15P-GT_DDR3L - B1	C0
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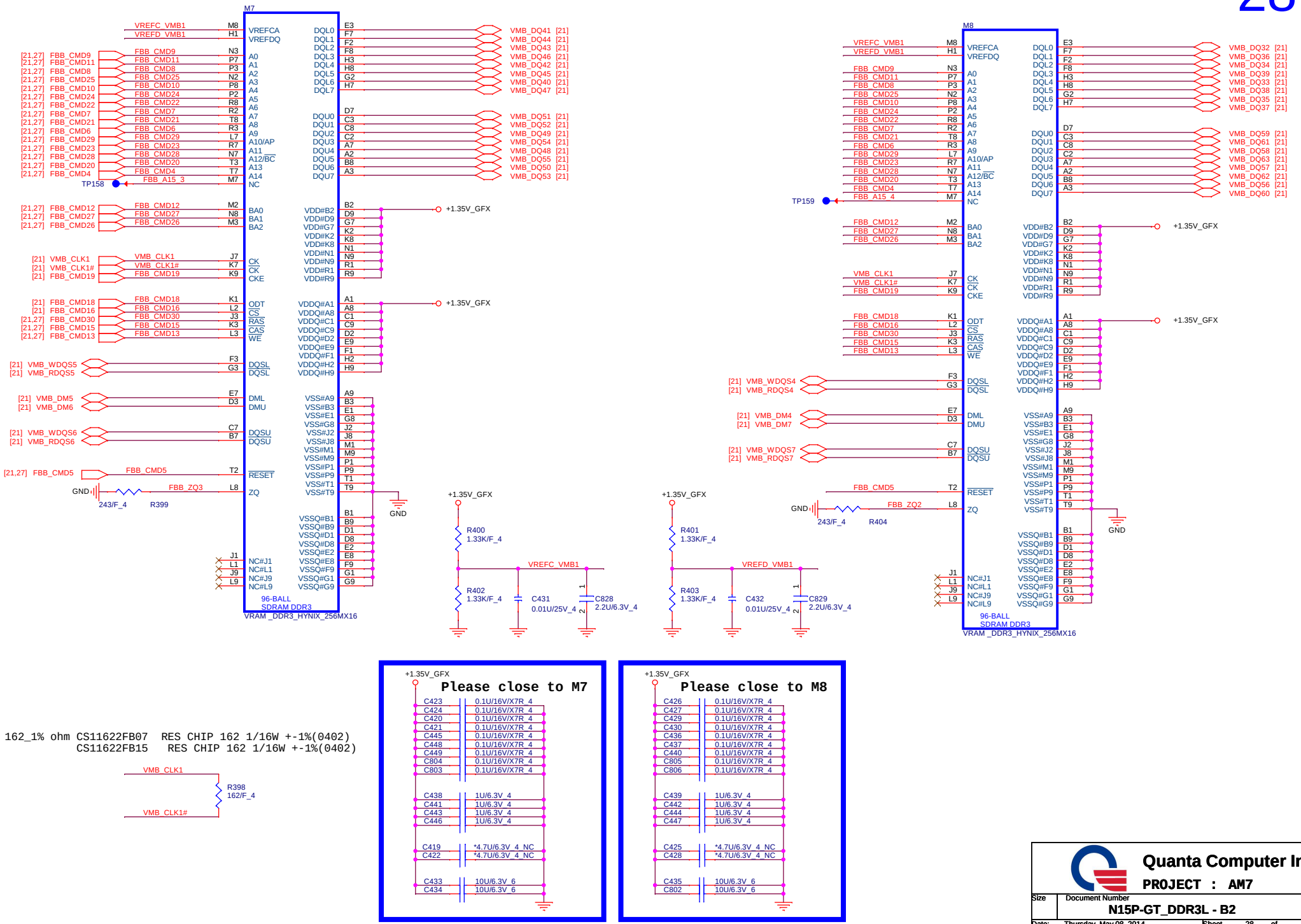

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

Quanta Computer Inc.		
PROJECT : AM7		
Size	Document Number: N15P-GT_DDR3L - B2	Rev: C0
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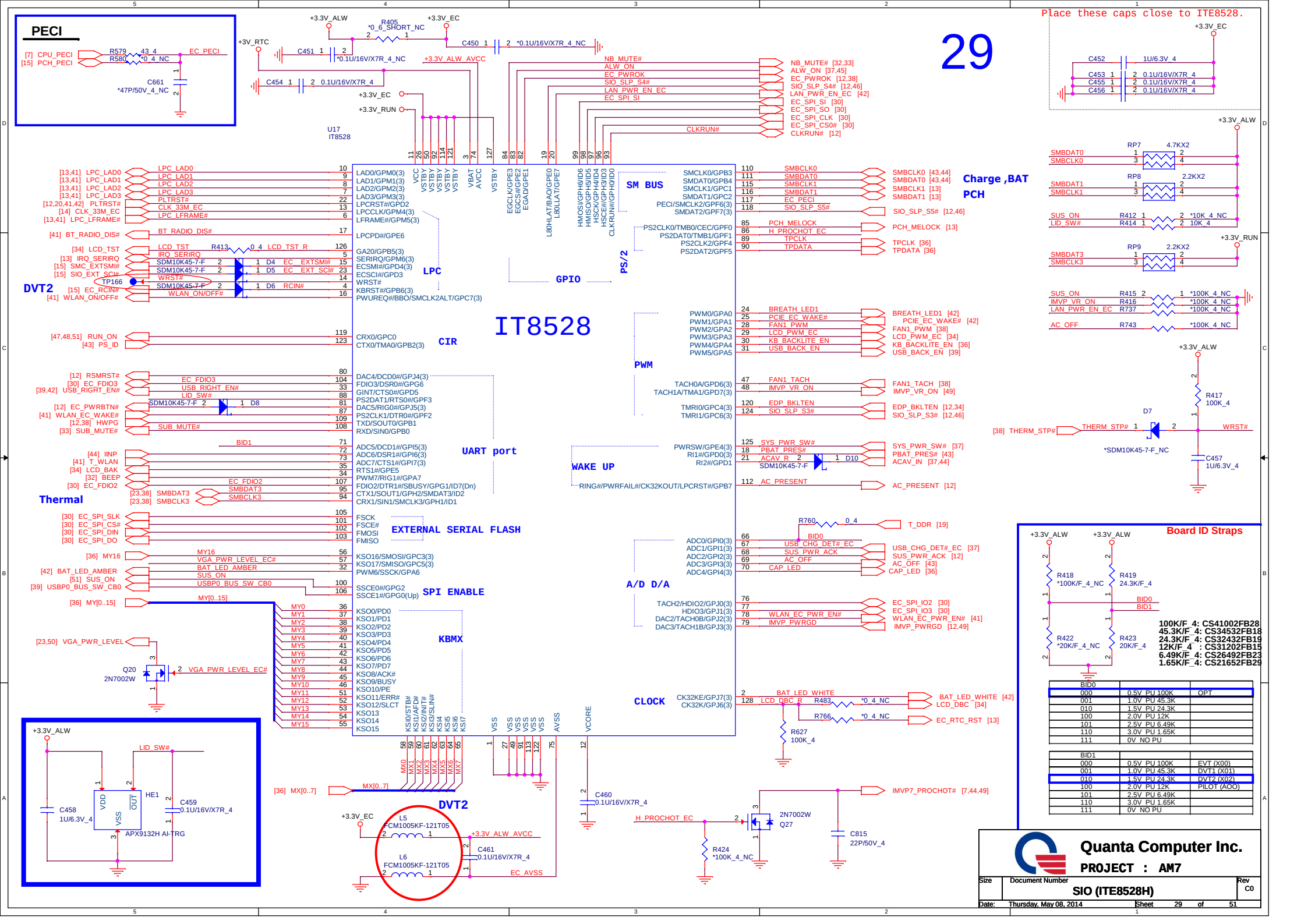
29
Place these caps close to ITE8528.
PECI
IT8528
U17
IT8528
LPC
GPIO
PS/2
SM BUS
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Charge ,BAT
PCH
DVT2
Thermal
Board ID Straps
100K/F_4: CS41002FB28
45.3K/F_4: CS34532FB18
24.3K/F_4: CS32432FB19
12K/F_4 : CS31202FB15
6.49K/F_4: CS26492FB23
1.65K/F_4: CS21652FB29
Quanta Computer Inc.
PROJECT : AM7
SIO (ITE8528H)
Rev C0
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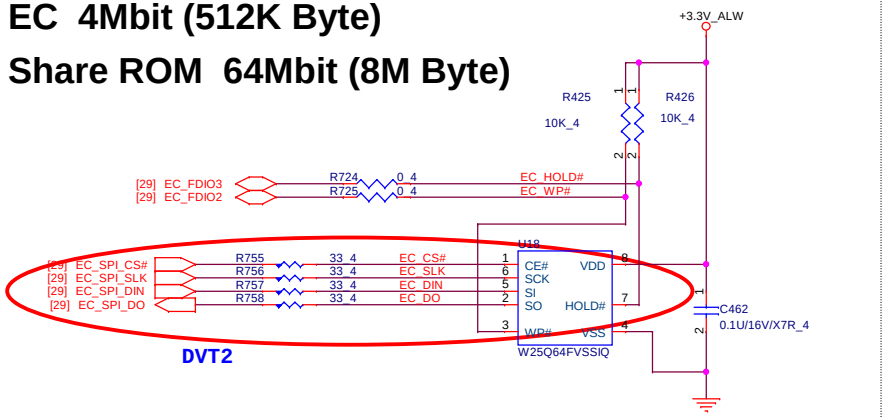
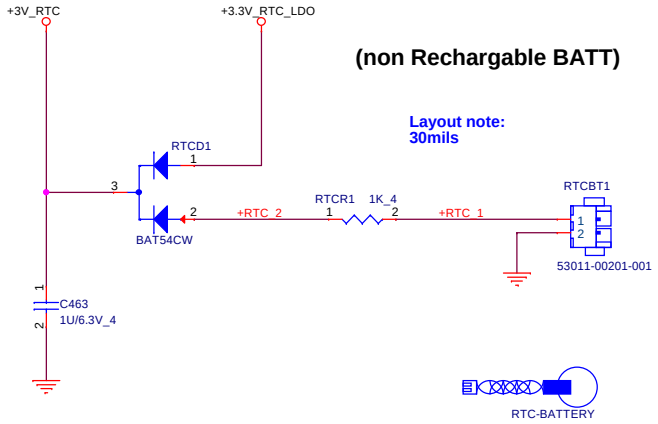
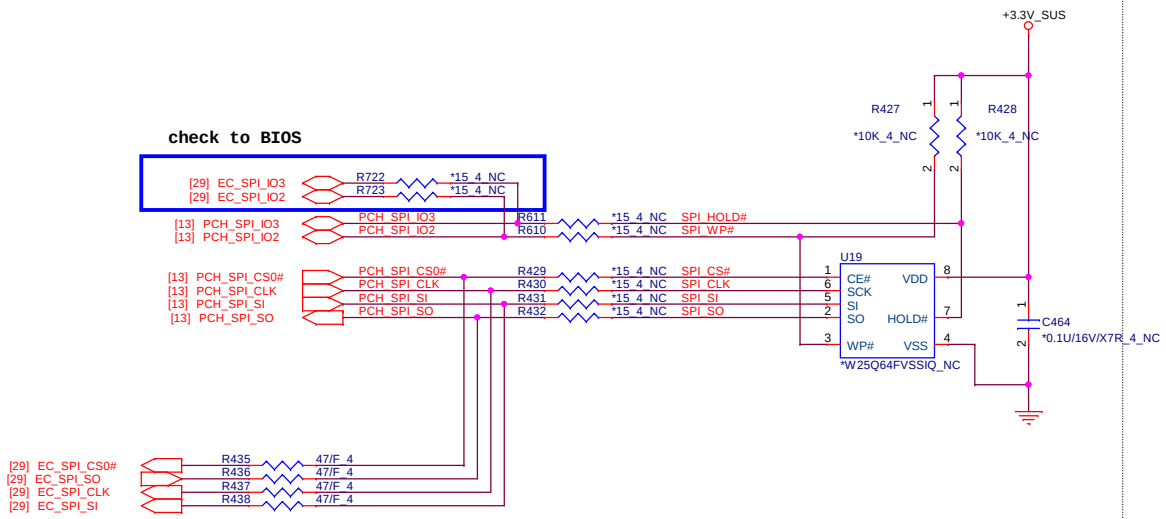
For EC 4Mbit (512K Byte)
For Share ROM 64Mbit (8M Byte)



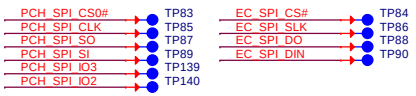
RTC BATTERY



For PCH 32Mbit (4M Byte)



TP for ICT flash BIOS process



EMI

Quanta Computer Inc.
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Size	Document Number	Rev
	FLASH / RTC	C0

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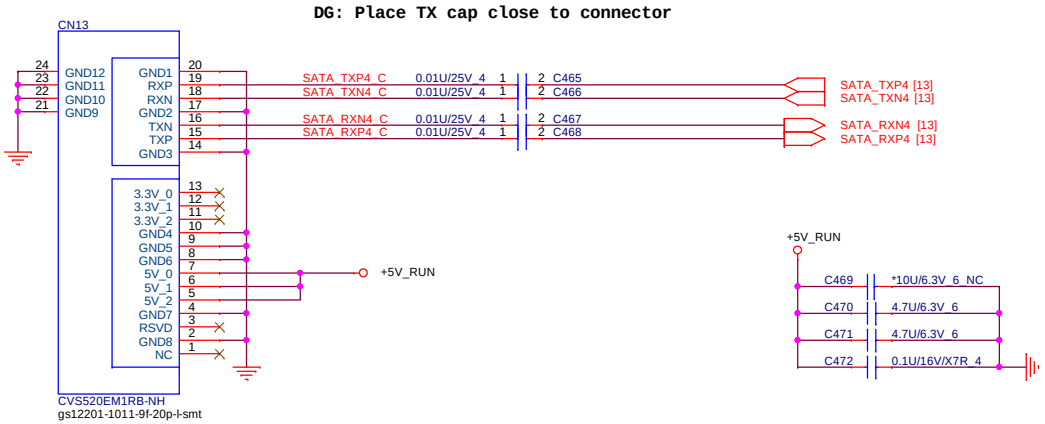
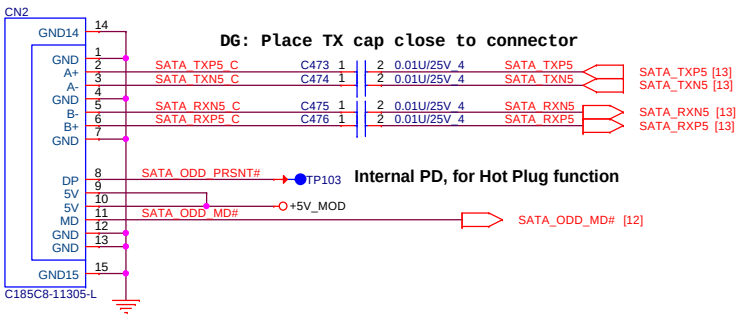
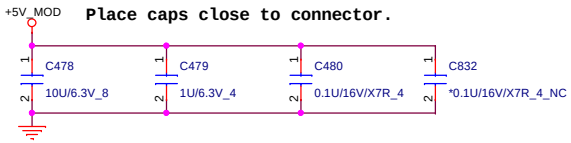
SATA HDD Connector

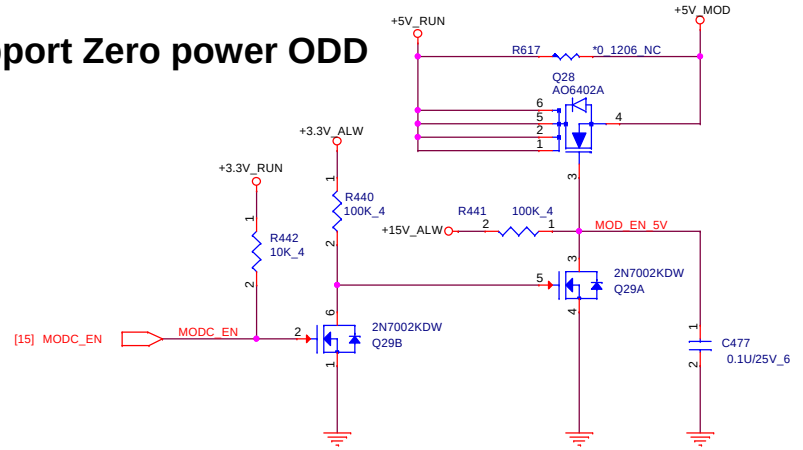


ODD





Support Zero power ODD



Quanta Computer Inc.

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Size	Document Number	Rev
	HDD / ODD	C0

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Digital Plane | Analog Plane

+5V_RUN — L7 FCM1005KF-121T05 — +5V_AVDD

DVT2

[29,33] NB_MUTE# — R670 — PDB; R443 *1M_4_NC; C493 *1U/6.3V_4_NC

C486 = 10uF for Desktop Applicaiton
C486 = 2.2uF for Laptop Application

VREF — C486 2.2U/10V_4
LDO1_CAP — C487 10U/6.3V_6
R691 100K_4

100K is used to speed up the discharge for LDO1. It could solve the pop sound during system boot up and reboot.

+3.3V_RUN

C483 4.7U/6.3V_6; C484 1U/6.3V_4; C485 1U/6.3V_4

C481 4.7U/6.3V_6; C482 0.1U/16V/X7R_4 — +5V_AVDD

ALC3234

MQFN48(6X6)

U20

CBP 37 — CBP
38 — AVSS2
C494 10U/6.3V_6; C495 10U/6.3V_6; R669 0_6 — LDO2_CAP 39 — LDO2-CAP
+1.5V_RUN — AVDD2 40 — AVDD2
PVDD — R668 0_6 — PVDD_3223 41 — PVDD1
C499 *10U/6.3V_6_NC; C500 *0.1U/16V/X7R_4_NC; C496 4.7U/6.3V_6; C497 0.1U/16V/X7R_4
AUD_SPK_L+ 42 — SPK-L+
AUD_SPK_L- 43 — SPK-L-
AUD_SPK_R- 44 — SPK-R-
AUD_SPK_R+ 45 — SPK-R+
46 — PVDD2
PDB 47 — PDB
3234_EAPD# 48 — SPDIFO/GOIO2
49 — GND
C501 4.7U/6.3V_6; C502 0.1U/16V/X7R_4
EAPD# R734 1 2 0_4 — ALC3234-CGFN)

CPVDD 36; CBN 35; CPVEE 34; HPOUT-R 33; HPOUT-L 32; LINE1_VREFO_L 31; LINE1_VREFO_R 30; MIC2-VREFO 29; VREF 28; LDO1_CAP 27; AVDD1 26; AVSS1 25

LINE2-L 24; LINE2-R 23; LINE1-L 22 — LINE1_L; LINE1-R 21 — LINE1_R
NC 20 — R697 1 2 0_4 — +3.3V_ALW
MIC-CAP 19 — MIC_CAP — C498 2 1 10U/6.3V_6
MIC2-R/SLEEVE 18 — SLEEVE
MIC2-L/RING2 17 — RING2
MONO-OUT 16 — SUB_OUT — SUB_OUT [33]
SPDIFO/FRONT JD 15 — R698 *20K/F_4_NC — +3.3V_RUN
MIC2/LINE2 JD 14
HP/LINE1 JD 13 — HPOUT-JD R R700 1 2 100K_4
R699 2 1 200K/F_4 — HPOUT-JD

DVDD1 1; GPIO0/DMIC-DATA 2; GPIO1/DMIC-CLK 3; DC DET/EAPD (DVSS) 4; SDATA-OUT 5; BIT-CLK 6; LDO3-CAP 7; SDATA-IN 8; DVDD-IO 9; SYNC 10; RESETB 11; PCBEEP 12

Analog Plane
Digital Plane

AUD_PC_BEEP

C498 Close to codec

Trace width for SLEEVE, RING2: 40mil

+3.3V_RUN — C505 4.7U/6.3V_6; C506 0.1U/16V/X7R_4
[34] DIGITAL_D1 — DIGITAL_CLK_C 3
[34] DIGITAL_CLK — R456 2 1 22_4 — DVSS

+3.3V_SUS — R667 1 2 0_4 — +DVDD_IO
C507 *4.7U/6.3V_6_NC; C508 0.1U/16V/X7R_4
Close to pin.9

HDA_RST# — HDA_RST# [13]
HDA_SYNC — HDA_SYNC [13]
AZ_CODEC_SDIN0 R457 1 2 33_4 — HDA_SDIN0 [13]
HDA_SDOUT — HDA_SDOUT [13]
HDA_BITCLK — HDA_BITCLK [13]

C509 22P/50V_4; C510 4.7U/6.3V_6

EMI

RING2 — C488 MLVG0402220NV05P
EARP_R1 — C489 MLVG0402220NV05P
HPOUT-JD — C490 MLVG0402220NV05P
EARP_L1 — C491 MLVG0402220NV05P
SLEEVE — C492 MLVG0402220NV05P

PC BEEP

AUD_PC_BEEP — C511 — BEEP1 R464 0.1U/16V/X7R_4 1K_4 — BEEP [29]
C512 — SPKR1 R466 0.1U/16V/X7R_4 1K_4 — ACZ_SPKR [13]
R468 *10K_4_NC

Parts	ALC3234 N/A	ALC3223 AL003223000
R697	0Ω	NC
R698	NC	20KΩ 1% CS32002FB29
R699	200KΩ 5% CS42002FB12	39.2KΩ 1% CS33922FB15
R700	100KΩ 5% CS41002JB20	NC
R734	0Ω	NC

Universal Audio Jack (ALC3223 supported iPhone/Nokia headset , Headphone, Line-In and Microphone)

MIC2-VREFO — R446 2.2K_4; R448 2.2K_4
HPOUT-L — SLEEVE — R450 20/F_6
HPOUT-JD — RING2
HPOUT-R — R451 20/F_6
LINE1_VREFO_L — R452 4.7K_4
LINE1_VREFO_R — R453 4.7K_4
R454 1K_4; R455 1K_4
LINE1_L — C503 4.7U/6.3V_6 — LINE1_L_C
LINE1_R — C504 4.7U/6.3V_6 — LINE1_R_C

R444 *10K_4_NC; R445 *10K_4_NC; R447 *10K_4_NC; R449 *10K_4_NC
EARP_L1; EARP_R1
CON1 — 2SJ3052-005111F
EC47 100P/50V_4; EC48 100P/50V_4; EC49 100P/50V_4; EC50 100P/50V_4

AUD_SPK_L+ — SR4 — *SR_0603_NC — AUD_SPK_L+_L
AUD_SPK_L- — SR5 — *SR_0603_NC — AUD_SPK_L-_L
AUD_SPK_R- — SR6 — *SR_0603_NC — AUD_SPK_R-_L
AUD_SPK_R+ — SR7 — *SR_0603_NC — AUD_SPK_R+_L
[33] SUBWOOFER+ — SUBWOOFER+
[33] SUBWOOFER- — SUBWOOFER-
CN15 — 50281-0060N-001
EC51 *100P_4_NC; EC52 *100P_4_NC; EC53 *100P_4_NC; EC54 *100P_4_NC

R666 1 2 0_4
R461 1 2 0_4
R462 1 2 0_4
R463 1 2 0_4
R465 1 2 0_4

Reserve for ALC3223

Q30 / R459 / R467 / C513 Stuff on ALC3223

+3.3V_SUS; +3.3V_RTC_LDO; +3.3V_ALW
R458 *100K_4_NC; R459 *100K_4_NC; R460 *100K_4_NC
SLEEVE; HDA_RST#; R467 *10K_4_NC; HDA_RST#_L
C513 *1U/6.3V_4_NC
Q30 *2N7002KDW_NC

To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power

Reserve

+15V_ALW; +5V_RUN; PVDD
R710 0_6; Q57 *2N7002W_NC
+5V_ALW2; R709 *100K_4_NC; R708 *100K_4_NC
DC_DET — R707 *0_4_NC — DC_DET_R — Q58 *MMST3904-7-F_NC

Normally DC-DET pin is low level to turn on Power Switch(Q5)
When DC be detected from Class D output,DC-DET pin is floating to turn off Power Switch(Q5)

Reserve for ALC3223

DVSS — R711 1 2 *0_4_NC
R712 1 2 *0_4_NC — DC_DET
R713 1 2 *0_4_NC — EAPD#
R695 10K_4
EAPD# [33]

Only for ALC3234

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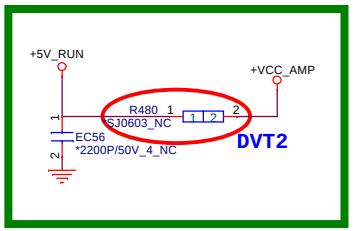
Subwoofer Amp



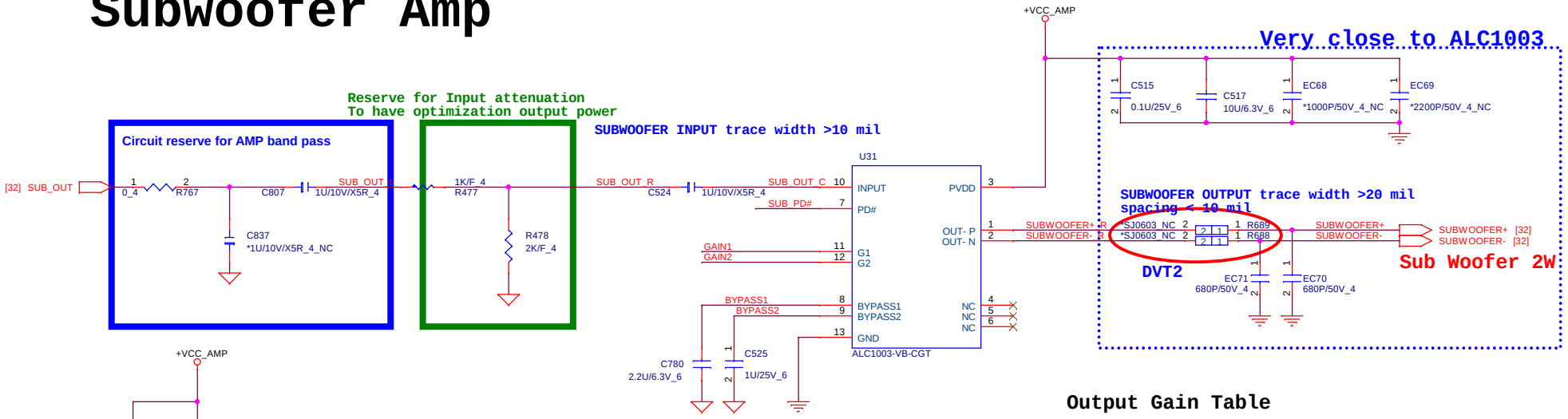
+VCC_AMP ≧ 30mils

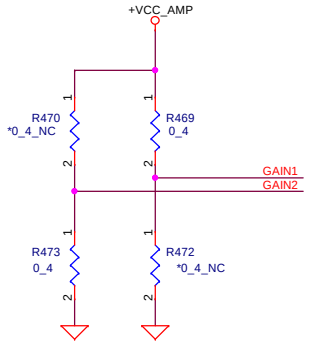
Very close to ALC1003

Reserve for Input attenuation
To have optimization output power

SUBWOOFER INPUT trace width >10 mil

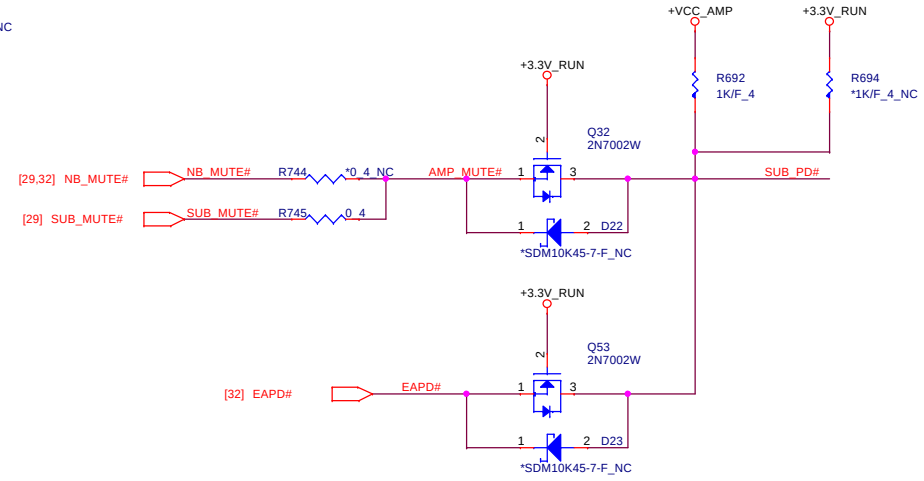
SUBWOOFER OUTPUT trace width >20 mil
spacing < 10 mil





Output Gain Table

GAIN1	GAIN2	Gain(Differential)
0	0	11dB
1	0	14dB
0	1	19dB
1	1	25dB



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	WOOFER/AMP	C0

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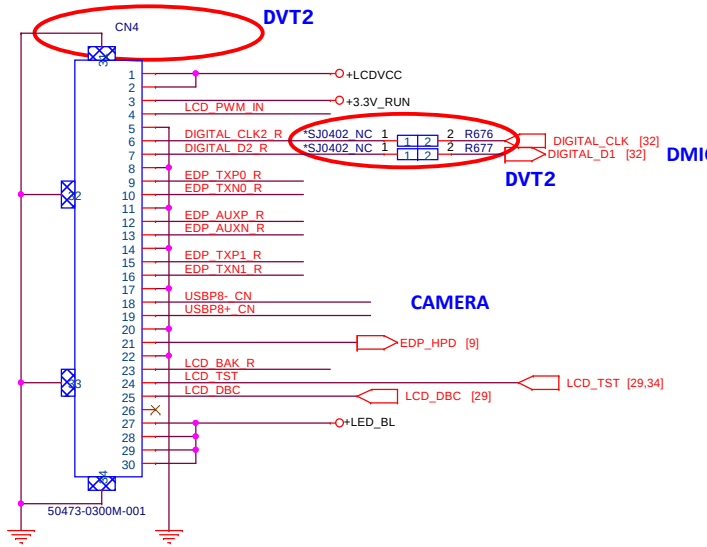
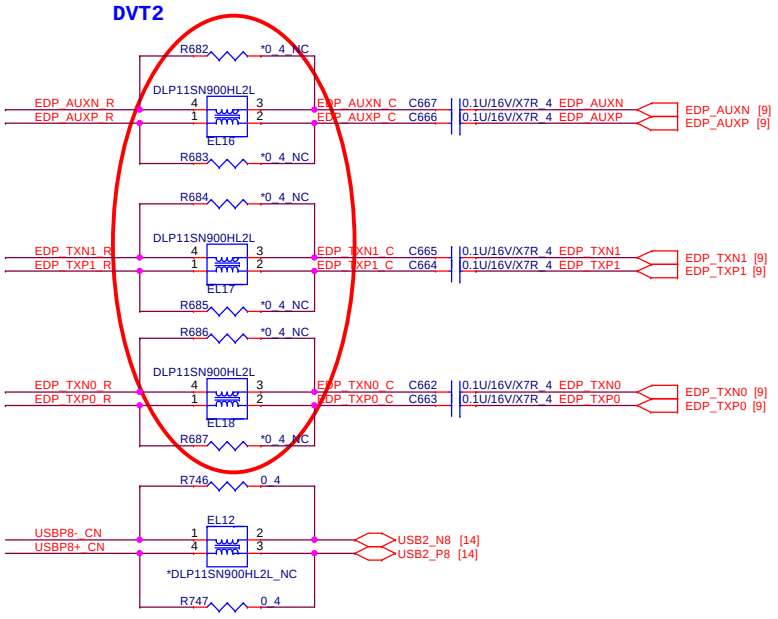
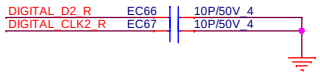
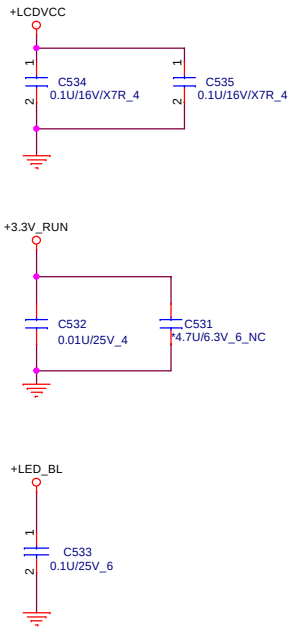


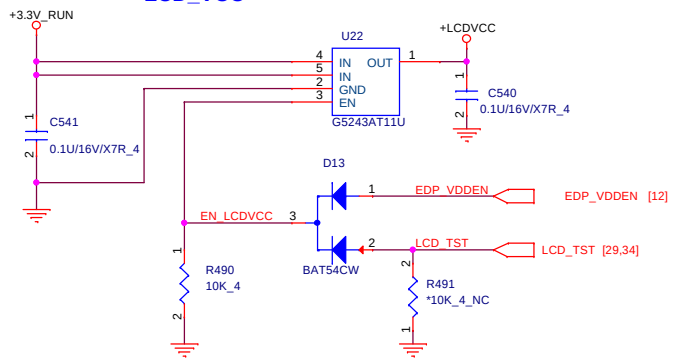




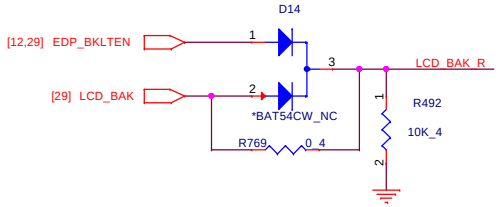
Close to CN4



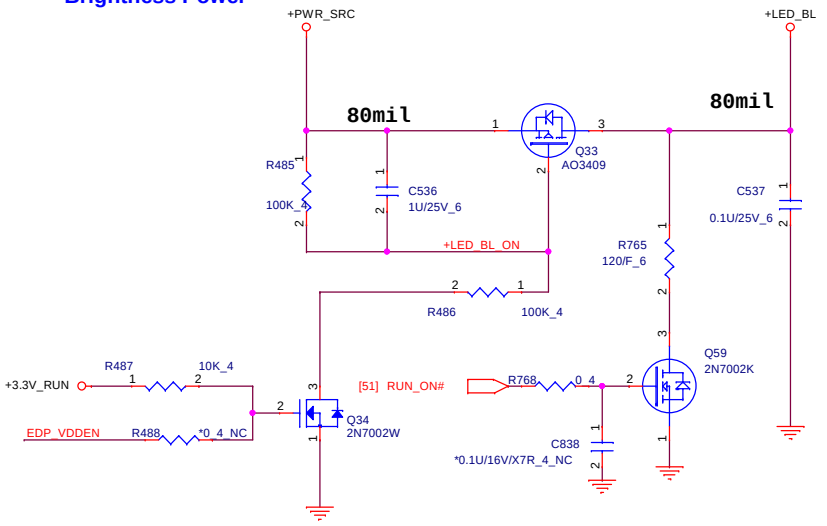
LCD_VCC



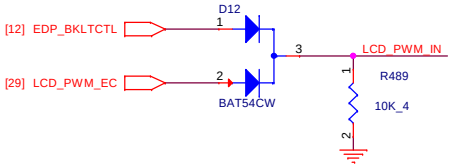
BAK_EN



Brightness Power



Brightness Control



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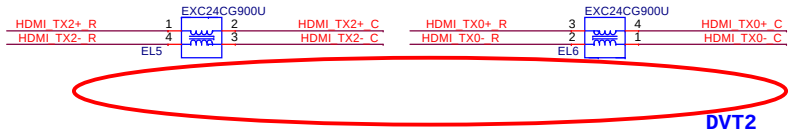
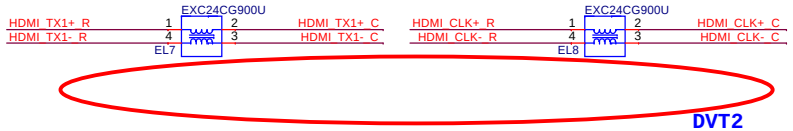
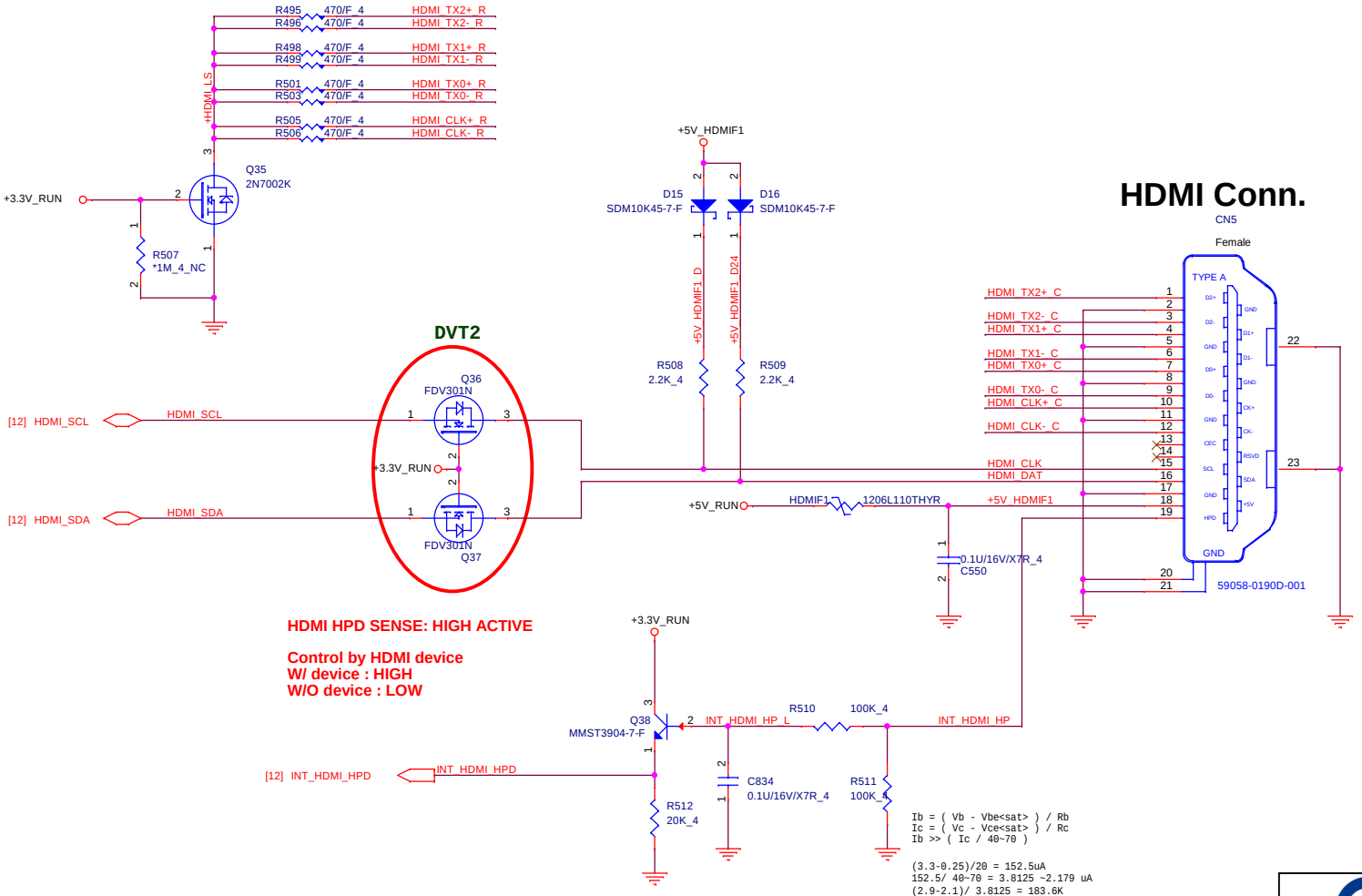
INT HDMI

[9] INT_HDMI_TXP2	INT_HDMI_TXP2	C542 1	2 0.1U/16V/X7R_4	HDMI_TX2+_R
[9] INT_HDMI_TXN2	INT_HDMI_TXN2	C543 1	2 0.1U/16V/X7R_4	HDMI_TX2-_R
[9] INT_HDMI_TXP1	INT_HDMI_TXP1	C544 1	2 0.1U/16V/X7R_4	HDMI_TX1+_R
[9] INT_HDMI_TXN1	INT_HDMI_TXN1	C545 1	2 0.1U/16V/X7R_4	HDMI_TX1-_R
[9] INT_HDMI_TXP0	INT_HDMI_TXP0	C546 1	2 0.1U/16V/X7R_4	HDMI_TX0+_R
[9] INT_HDMI_TXN0	INT_HDMI_TXN0	C547 1	2 0.1U/16V/X7R_4	HDMI_TX0-_R
[9] INT_HDMI_TXCP	INT_HDMI_TXCP	C548 1	2 0.1U/16V/X7R_4	HDMI_CLK+_R
[9] INT_HDMI_TXCN	INT_HDMI_TXCN	C549 1	2 0.1U/16V/X7R_4	HDMI_CLK-_R

Reserve for EMI and close to HDMI CONN







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	HDMI	C0

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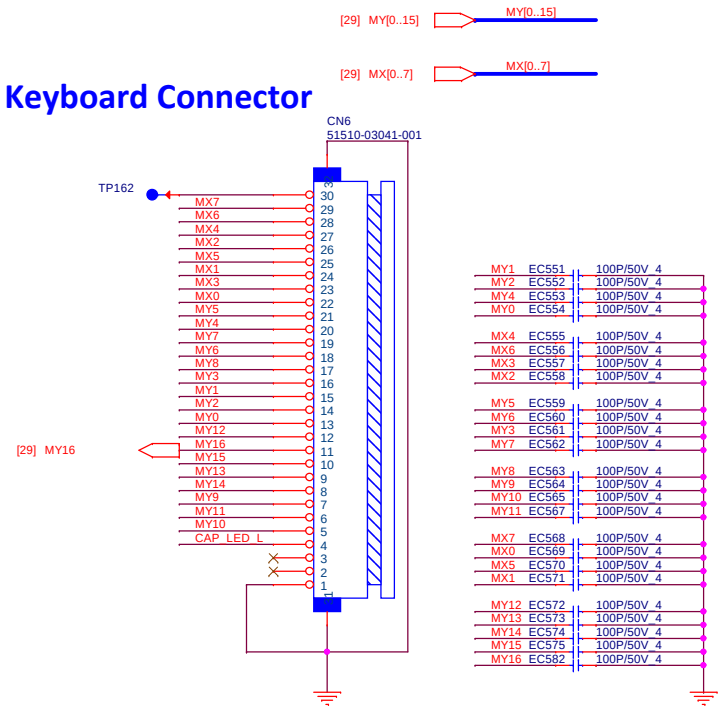
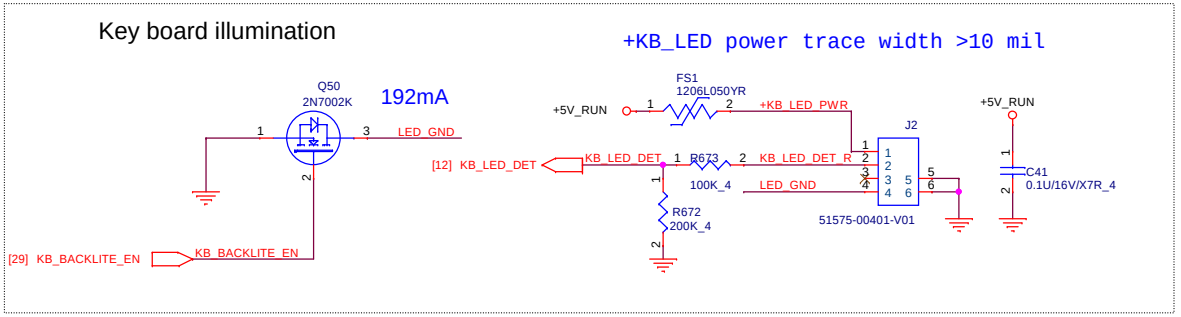
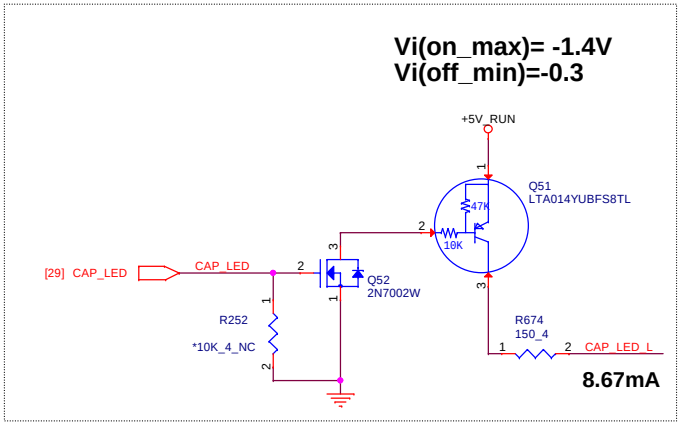
Keyboard Connector



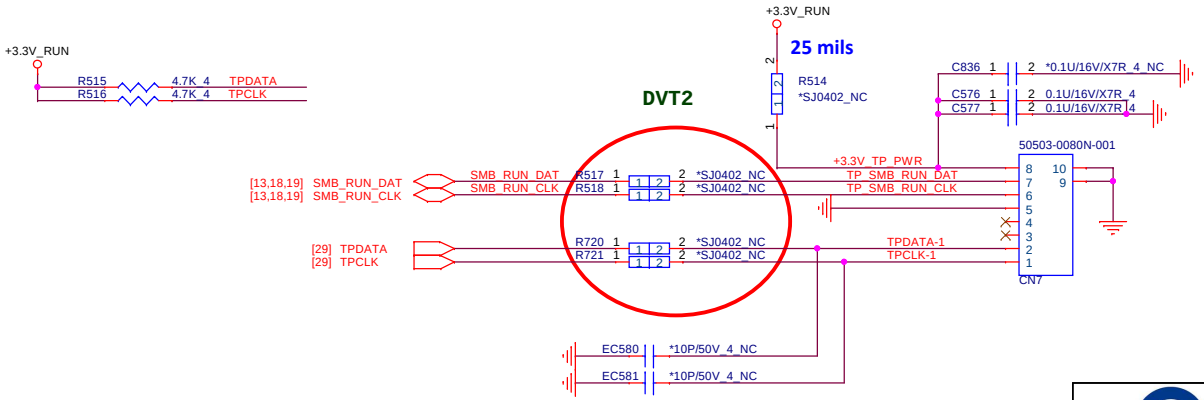
Key board illumination

+KB_LED power trace width >10 mil





Touch Pad Connector



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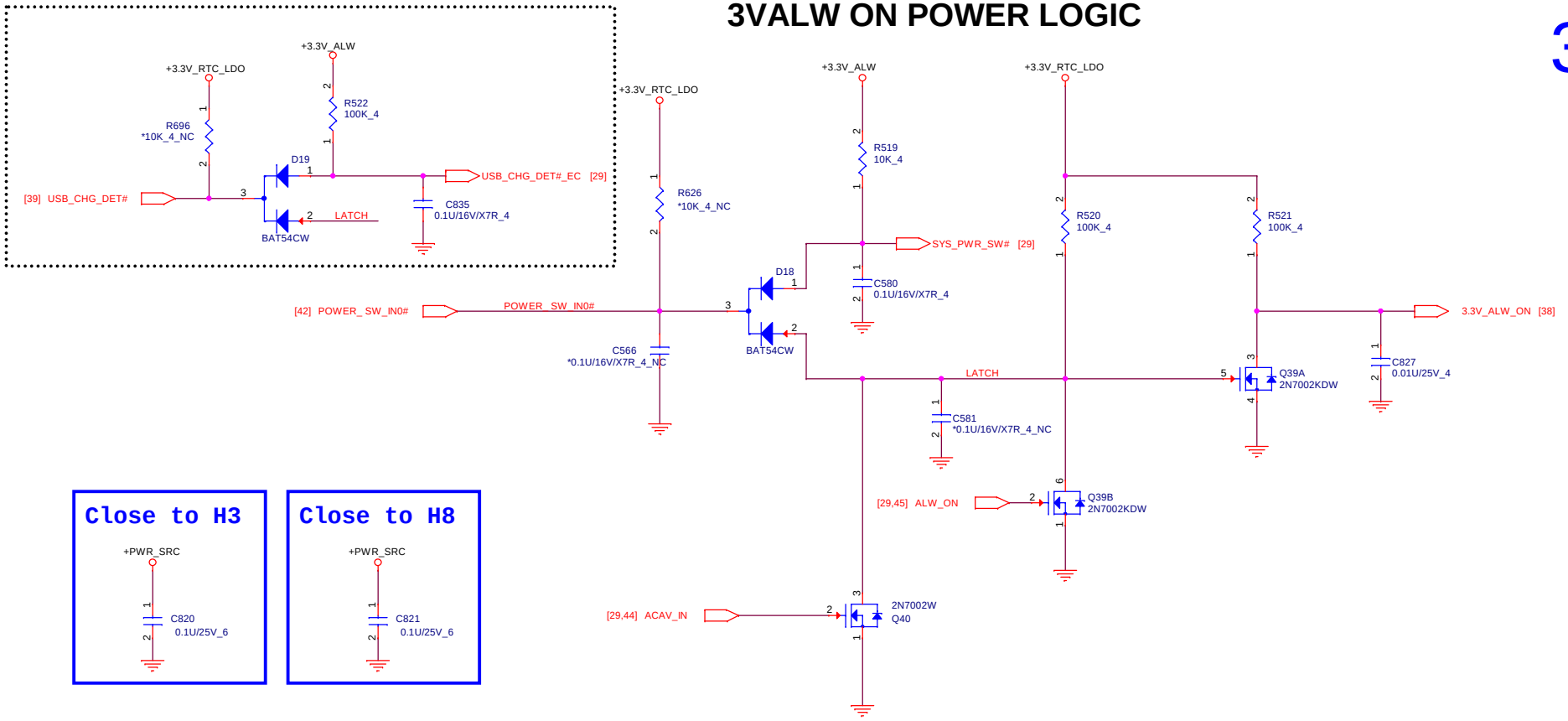
3VALW ON POWER LOGIC

37

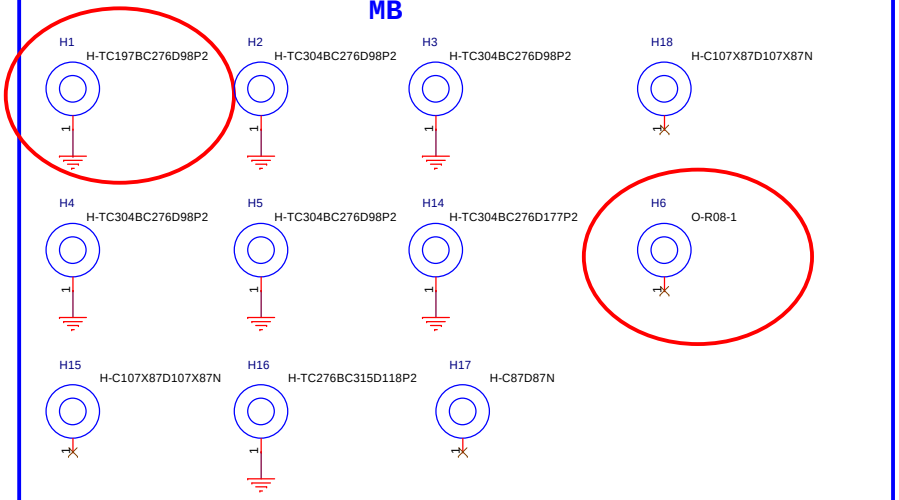


Close to H3

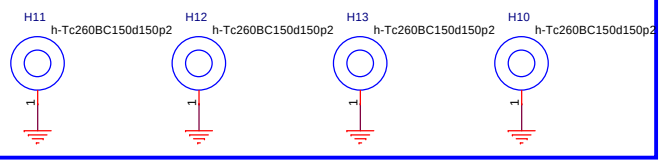
Close to H8

DVT2

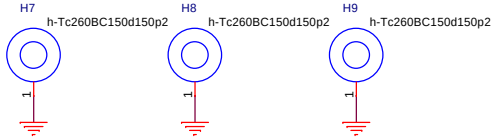
MB



CPU



GPU



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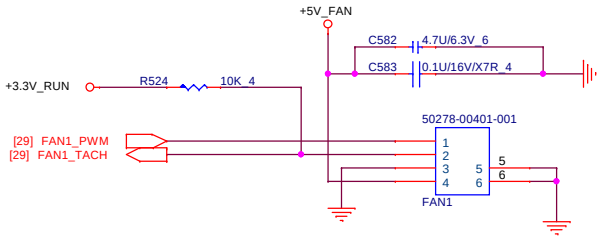
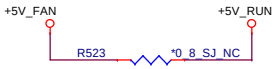
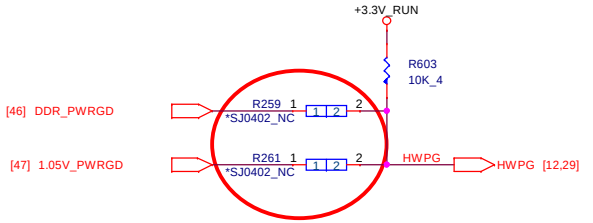
FAN CONN



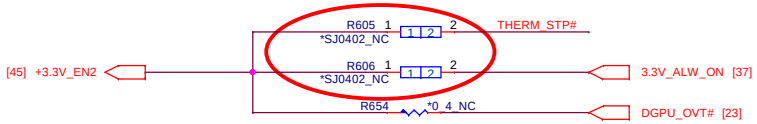
+5V_FAN
Max Current : mA



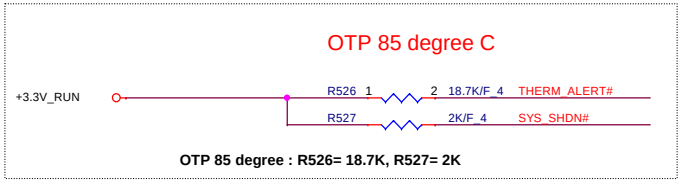
HWPG



DVT2

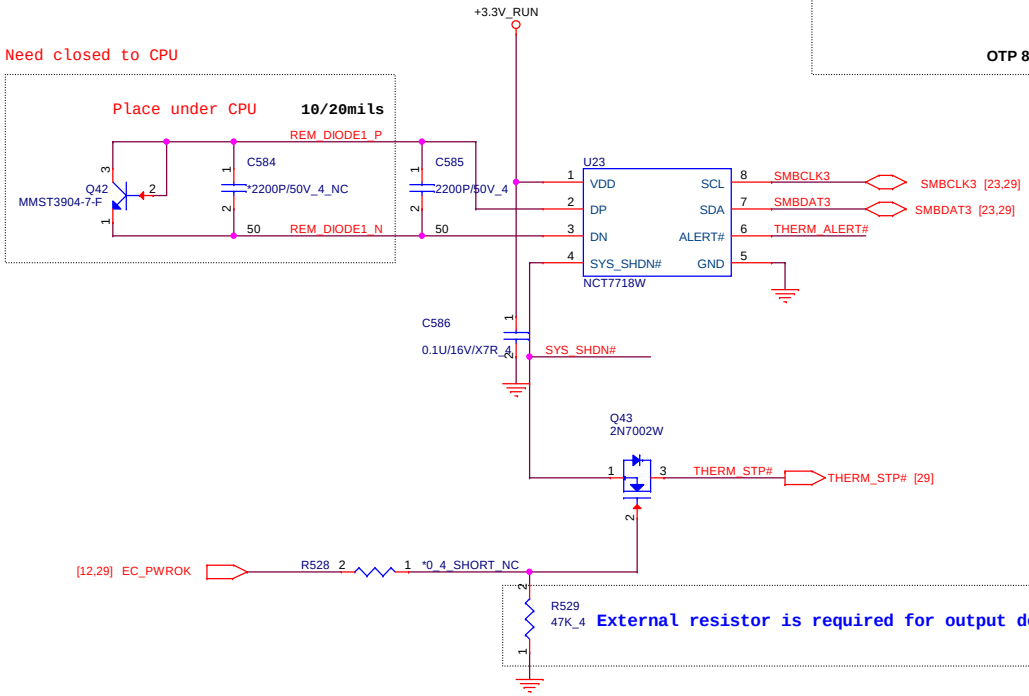


THERMAL IC



OTP 85 degree : R526= 18.7K, R527= 2K

SYS_SHD# / ALERT#	2K	7.5K	10.5K	14K	18.7K
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C



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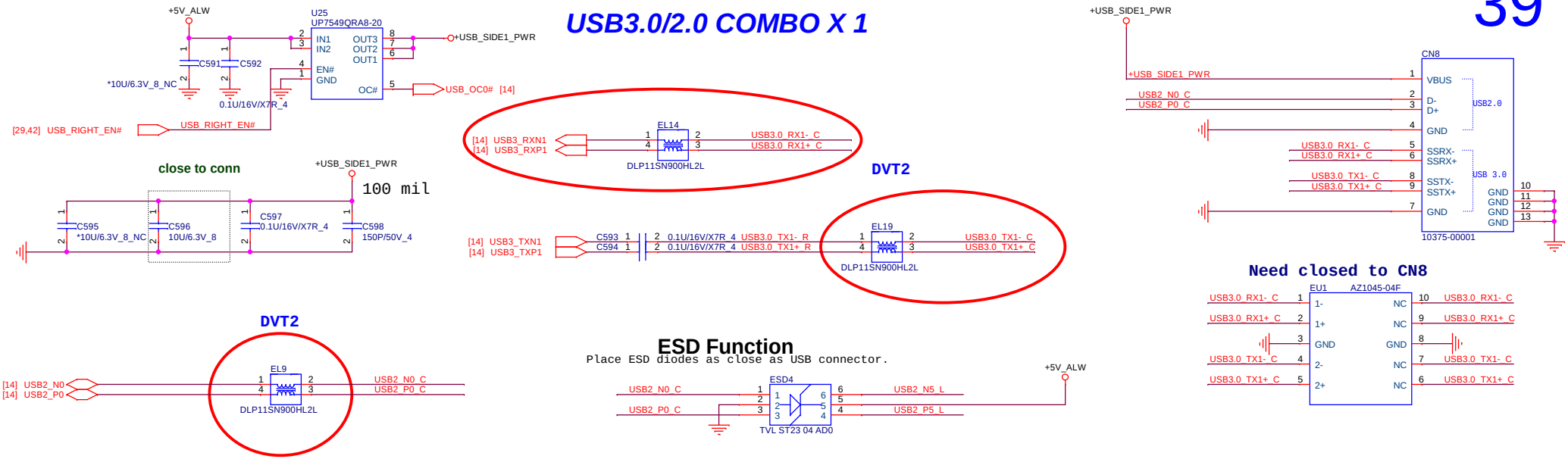
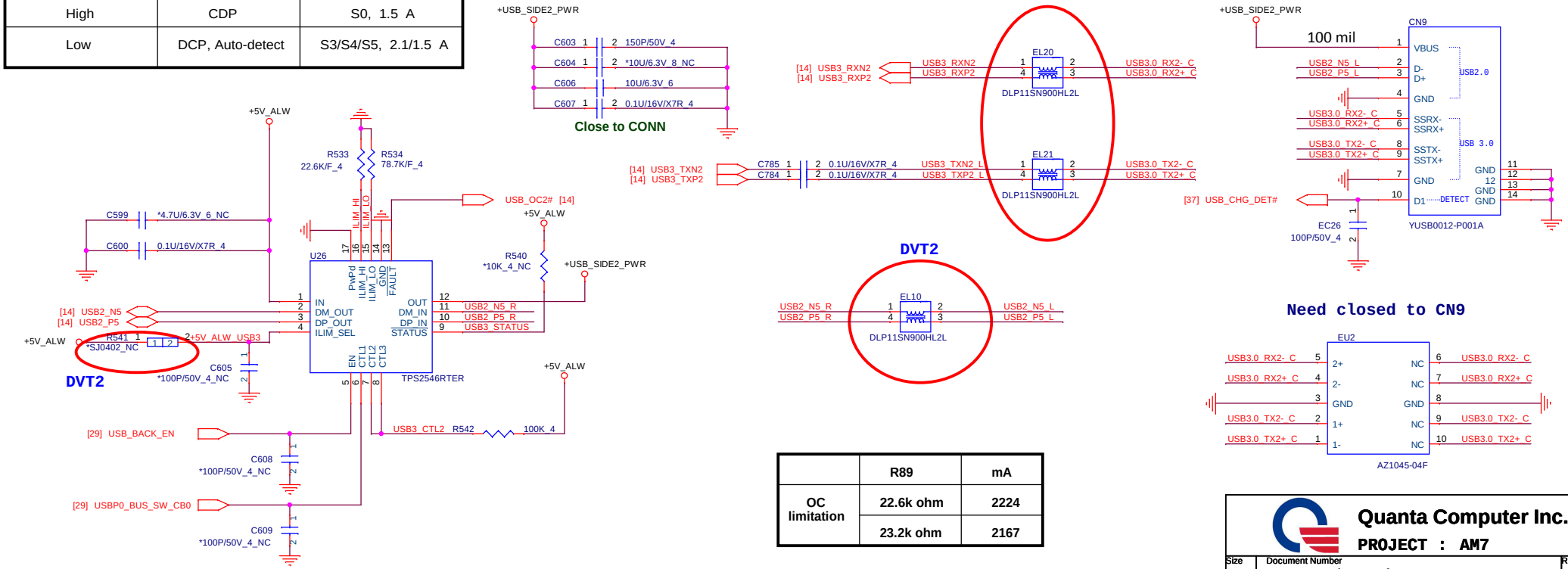
I continuous 1.5A
OC 2.0A M13 Request

USB3.0/2.0 COMBO X 1



USBP0_BUS_SW_CB0	Mode	Operating at
High	CDP	S0, 1.5 A
Low	DCP, Auto-detect	S3/S4/S5, 2.1/1.5 A

USB Power share



	R89	mA
OC limitation	22.6k ohm	2224
	23.2k ohm	2167

Quanta Computer Inc.
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	USB3/USB Charger	C0

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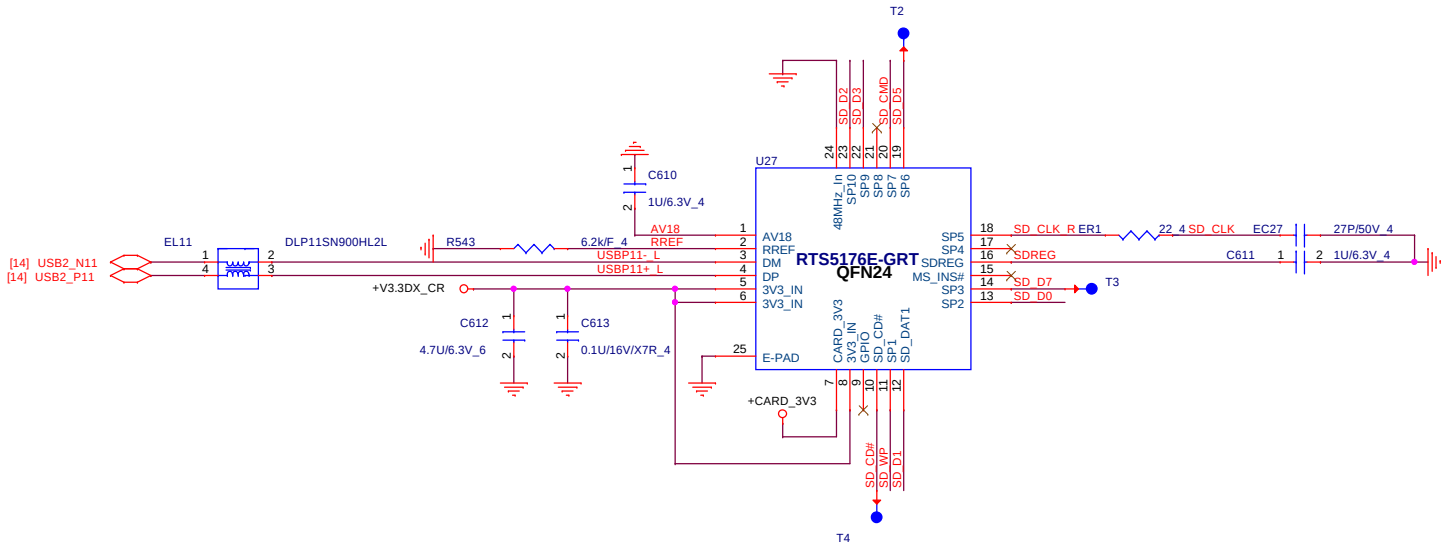
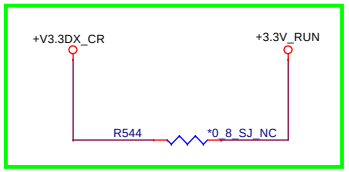
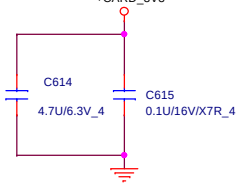
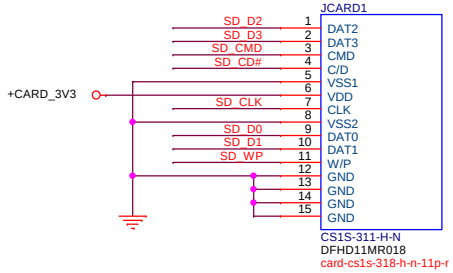




Place close to Connector



SD / MMC CARD READER



Quanta Computer Inc.

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	Card Reader RTS5176E	C0

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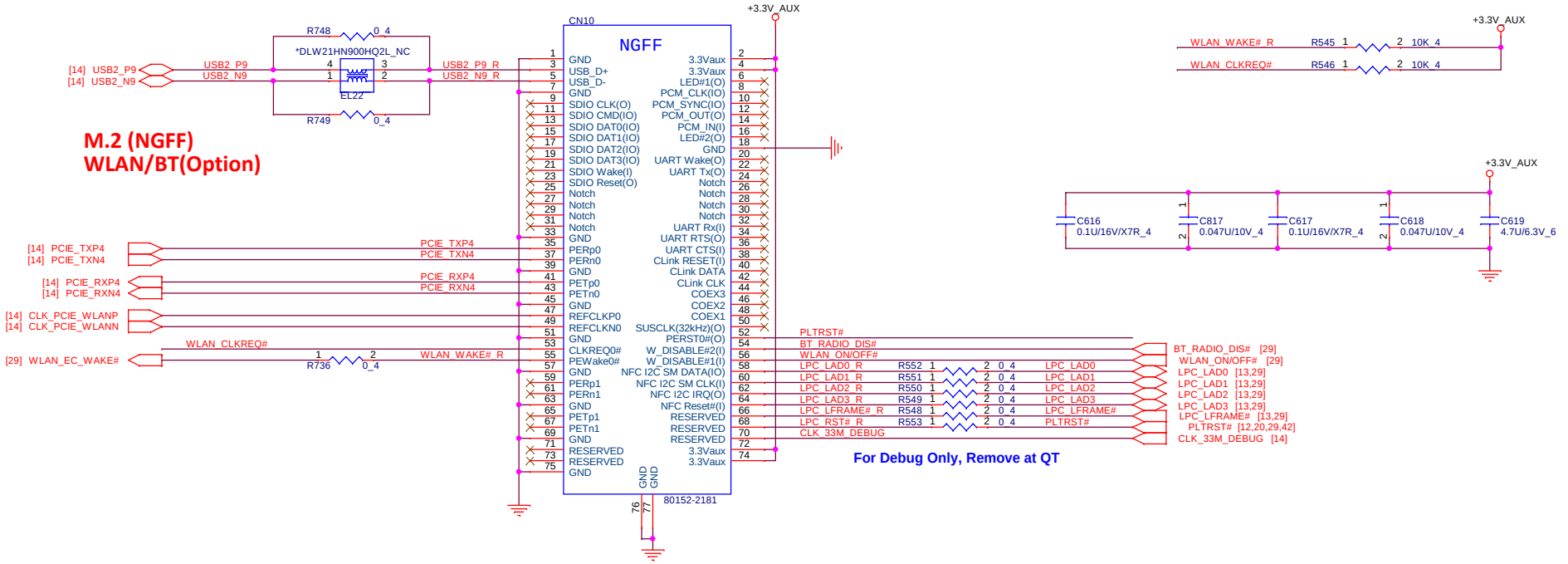
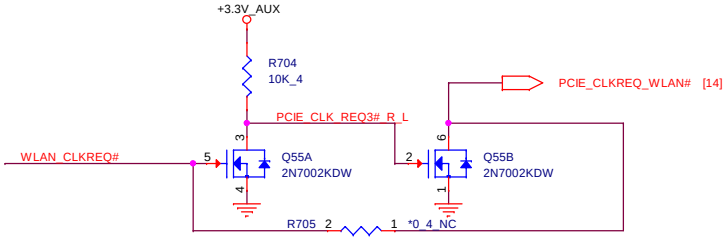
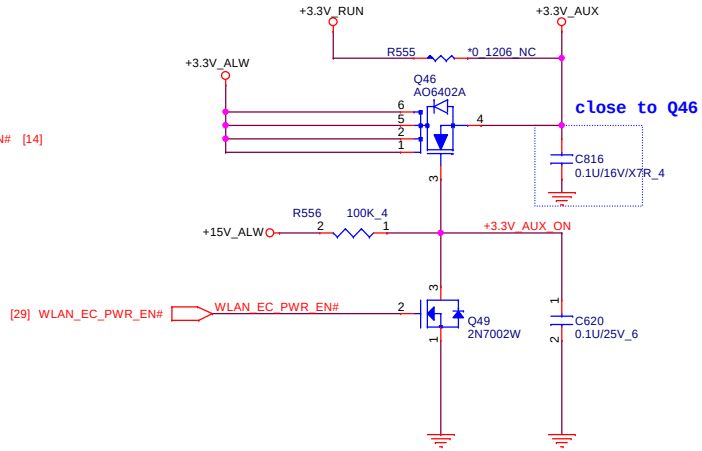
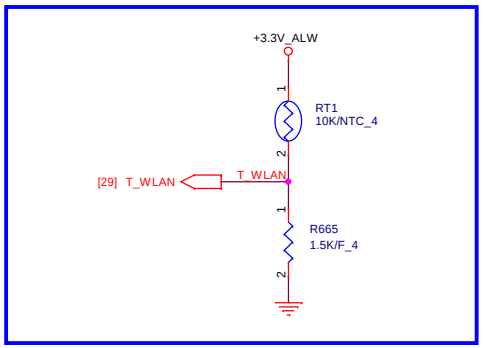
M.2 (NGFF) WLAN/BT(Option)









Quanta Computer Inc.

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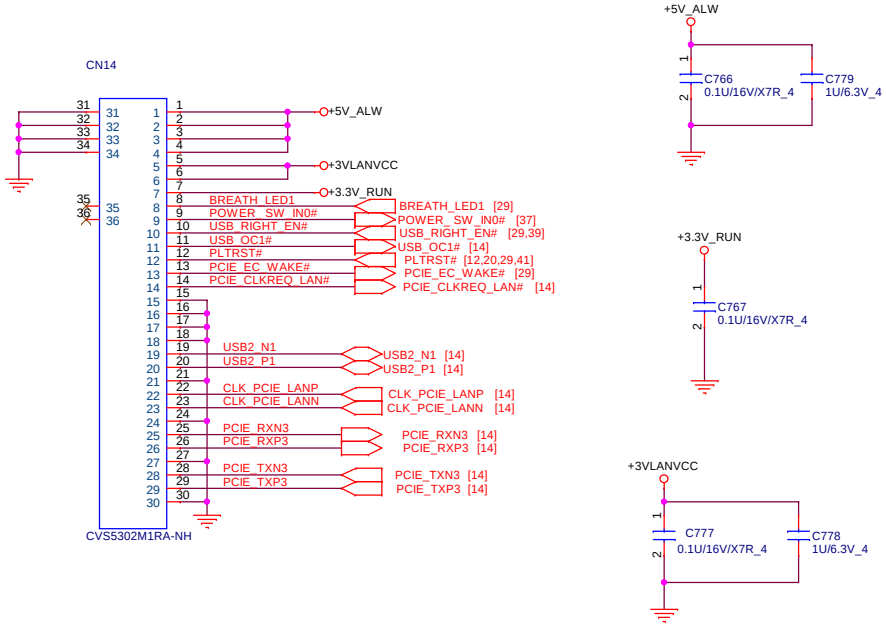
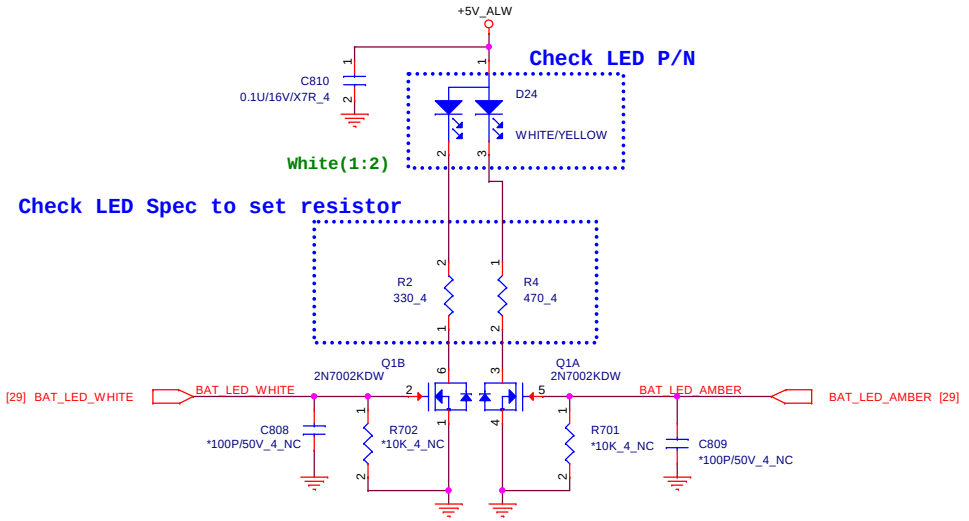
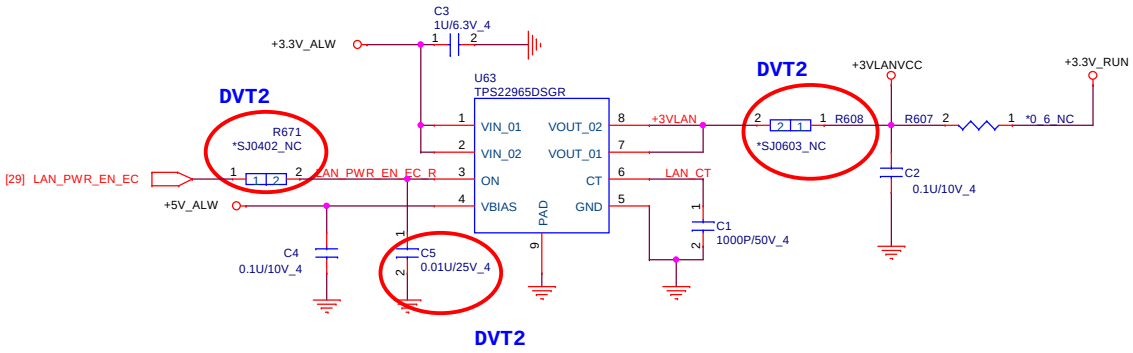
MB to IO BD Connector



Battery LED



LAN POWER



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Size	Document Number: IO BD CONN/LED	Rev: C0
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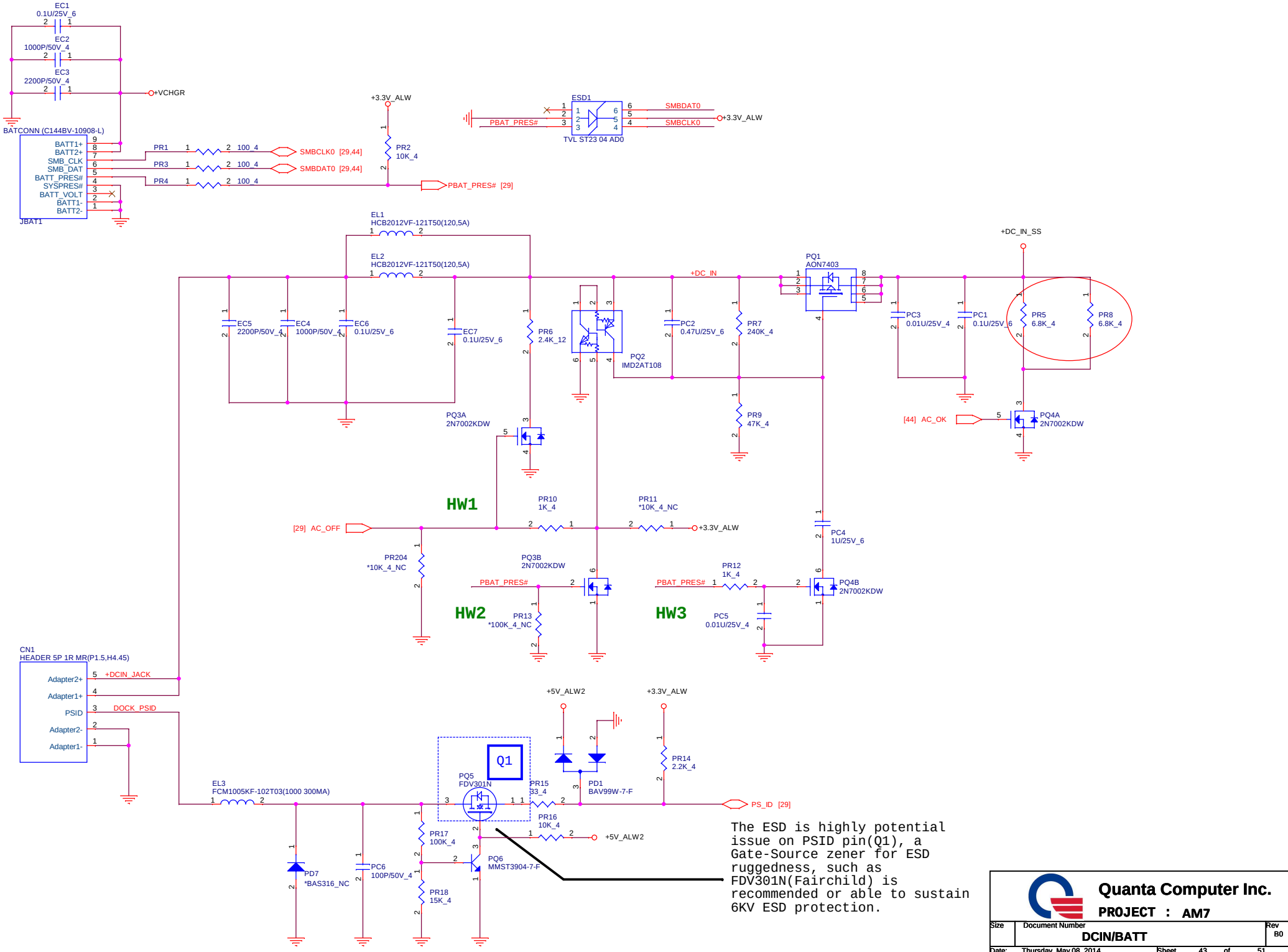
EC1
0.1U/25V_6
EC2
1000P/50V_4
EC3
2200P/50V_4
+VCHGR
BATCONN (C144BV-10908-L)
BATT1+
BATT2+
SMB_CLK
SMB_DAT
BATT_PRES#
SYSPRES#
BATT_VOLT
BATT1-
BATT2-
JBAT1
PR1 100_4
PR3 100_4
PR4 100_4
SMBCLK0 [29,44]
SMBDAT0 [29,44]
+3.3V_ALW
PR2
10K_4
PBAT_PRES# [29]
ESD1
PBAT_PRES#
SMBDAT0
SMBCLK0
+3.3V_ALW
TVL ST23 04 AD0
EL1
HCB2012VF-121T50(120,5A)
EL2
HCB2012VF-121T50(120,5A)
+DC_IN
PQ1
AON7403
+DC_IN_SS
EC5
2200P/50V_4
EC4
1000P/50V_4
EC6
0.1U/25V_6
EC7
0.1U/25V_6
PR6
2.4K_12
PQ2
IMD2AT108
PC2
0.47U/25V_6
PR7
240K_4
PC3
0.01U/25V_4
PC1
0.1U/25V_6
PR5
6.8K_4
PR8
6.8K_4
PR9
47K_4
PQ3A
2N7002KDW
[44] AC_OK
PQ4A
2N7002KDW
HW1
PR10
1K_4
PR11
*10K_4_NC
[29] AC_OFF
+3.3V_ALW
PC4
1U/25V_6
PR204
*10K_4_NC
PQ3B
2N7002KDW
PBAT_PRES#
PR12
1K_4
PQ4B
2N7002KDW
HW2
PR13
*100K_4_NC
HW3
PC5
0.01U/25V_4
CN1
HEADER 5P 1R MR(P1.5,H4.45)
Adapter2+
Adapter1+
PSID
Adapter2-
Adapter1-
+DCIN_JACK
DOCK_PSID
+5V_ALW2
+3.3V_ALW
EL3
FCM1005KF-102T03(1000 300MA)
Q1
PQ5
FDV301N
PR15
33_4
PD1
BAV99W-7-F
PR14
2.2K_4
PS_ID [29]
PR16
10K_4
PR17
100K_4
PQ6
MMST3904-7-F
PD7
*BAS316_NC
PC6
100P/50V_4
PR18
15K_4
The ESD is highly potential issue on PSID pin(Q1), a Gate-Source zener for ESD ruggedness, such as FDV301N(Fairchild) is recommended or able to sustain 6KV ESD protection.
Quanta Computer Inc.
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B0
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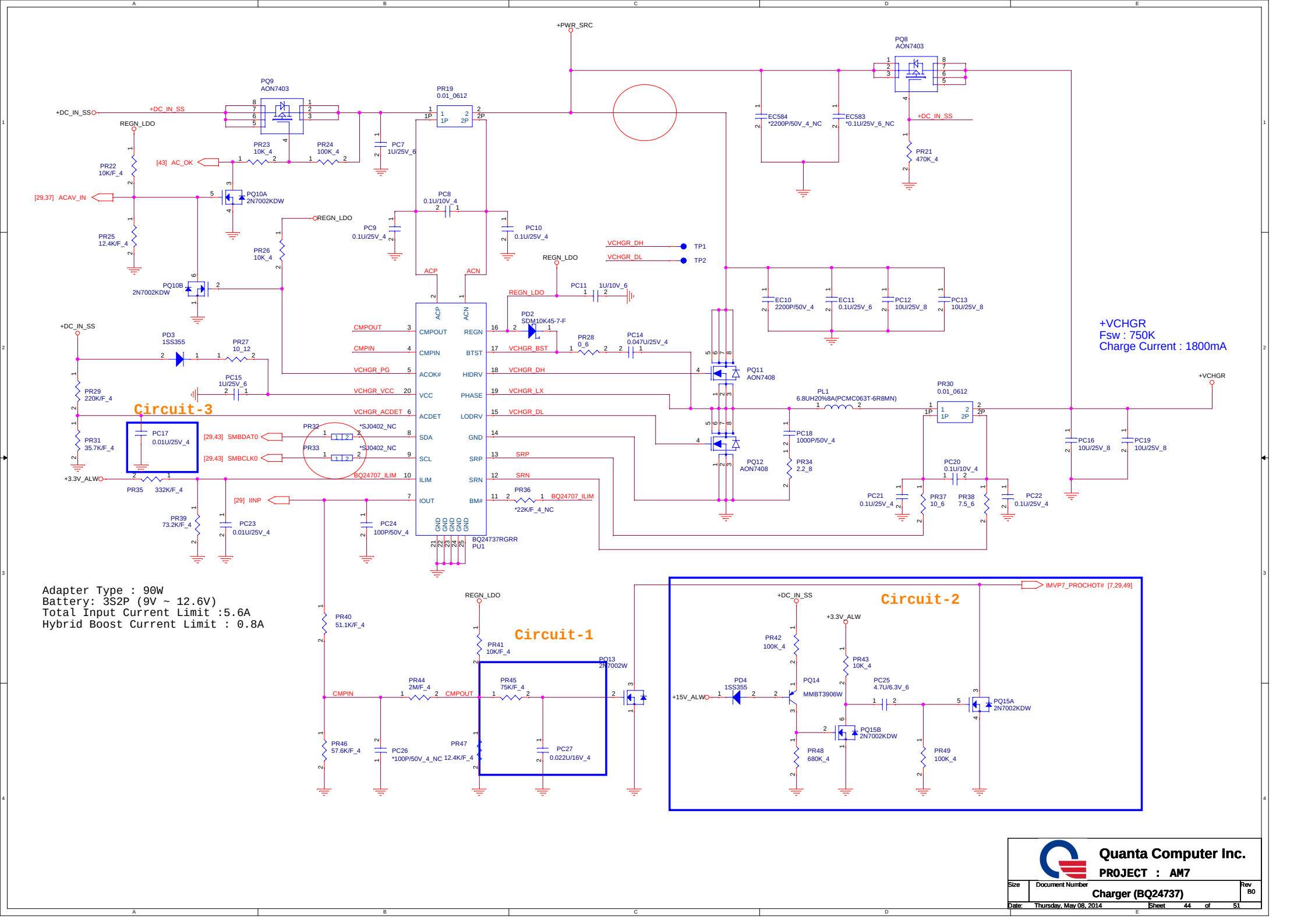

Quanta Computer Inc.

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Size	Document Number	Rev
	Charger (BQ24737)	B0

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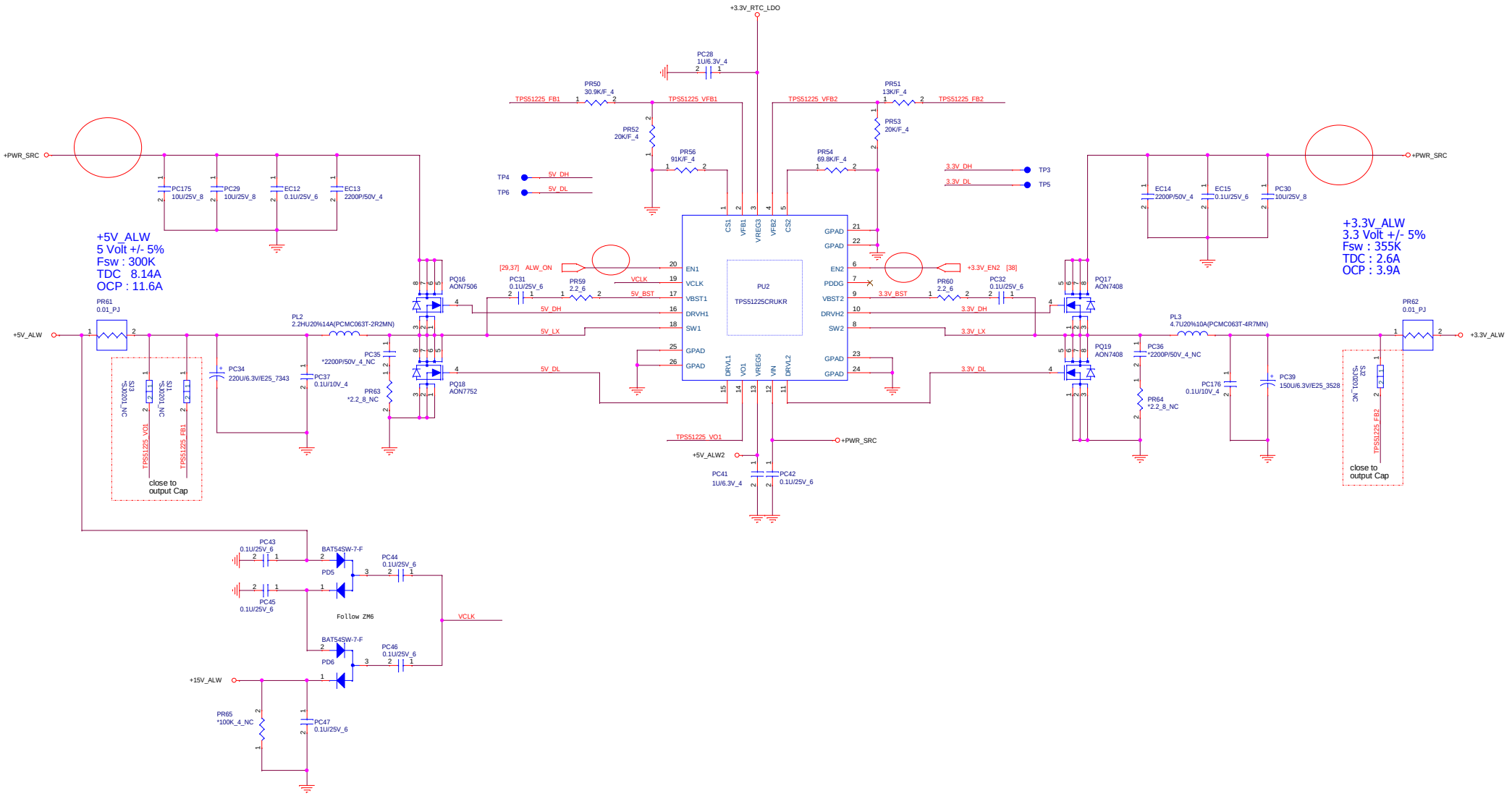

Quanta Computer Inc.	PROJECT : AM7	
Size	Document Number: 3V/5V (TPS51225RUKR)	Rev B0
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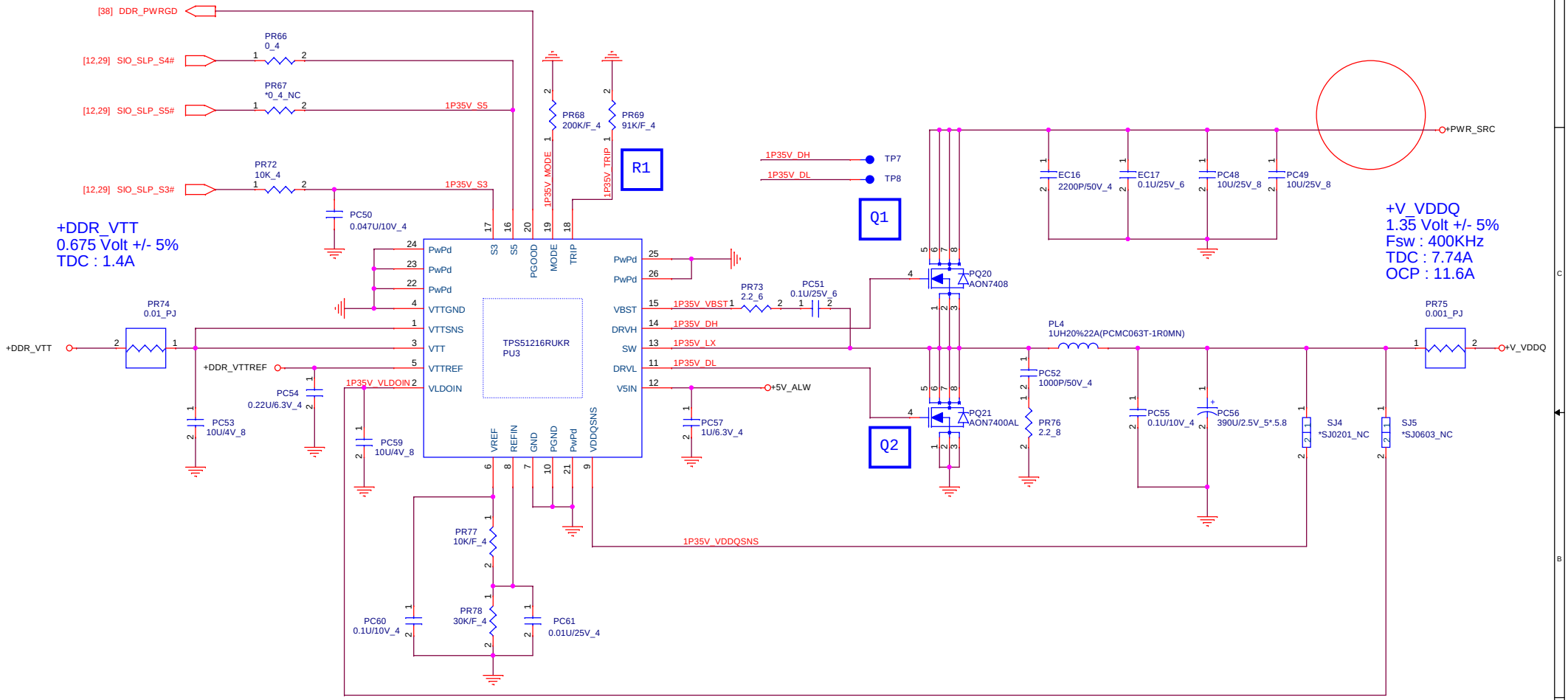

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PROJECT : AM7		
Size	Document Number: 1.35V/0.675V(TPS51216RUKR)	Rev: B0
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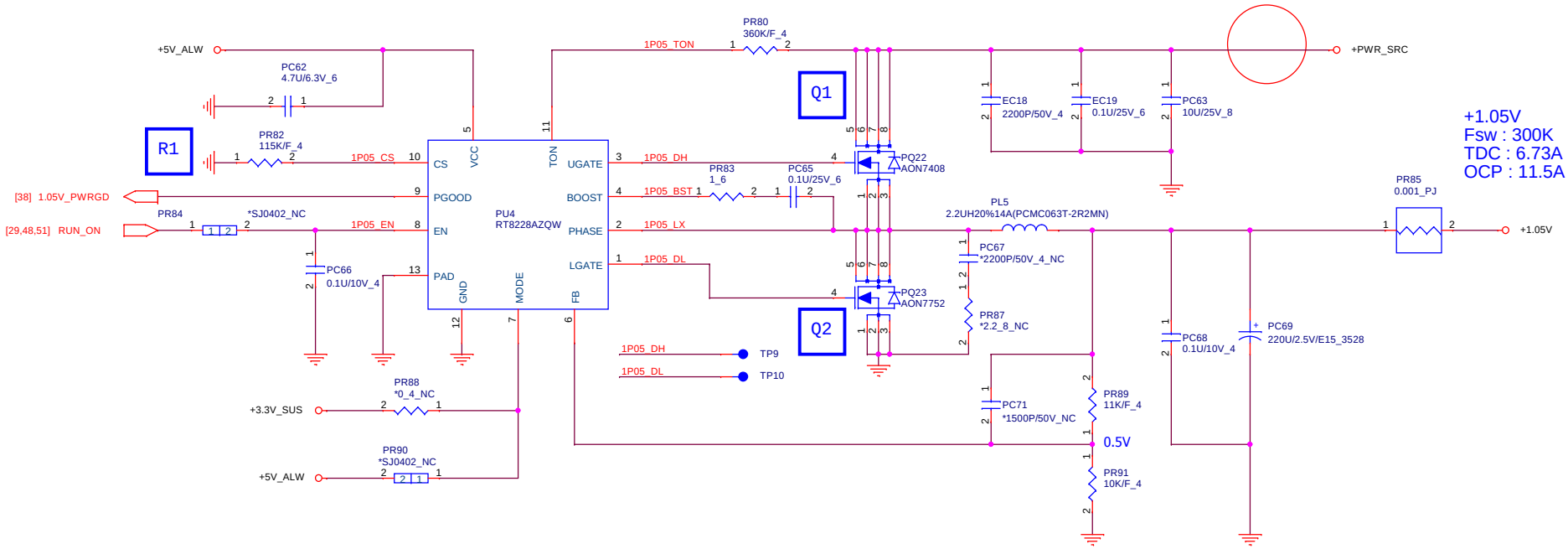

Quanta Computer Inc.		
PROJECT : AM7		
Size	Document Number: 1.05V_RUN (RT8228AZQW)	Rev: B0
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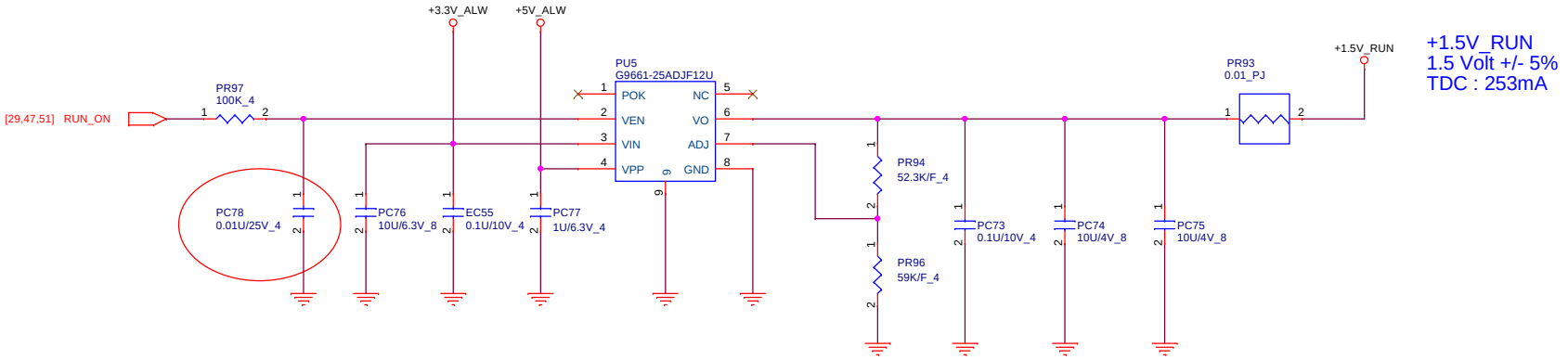

+1.5V_RUN
1.5 Volt +/- 5%
TDC : 253mA

Quanta Computer Inc.

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	1.5V (G9661)	B0

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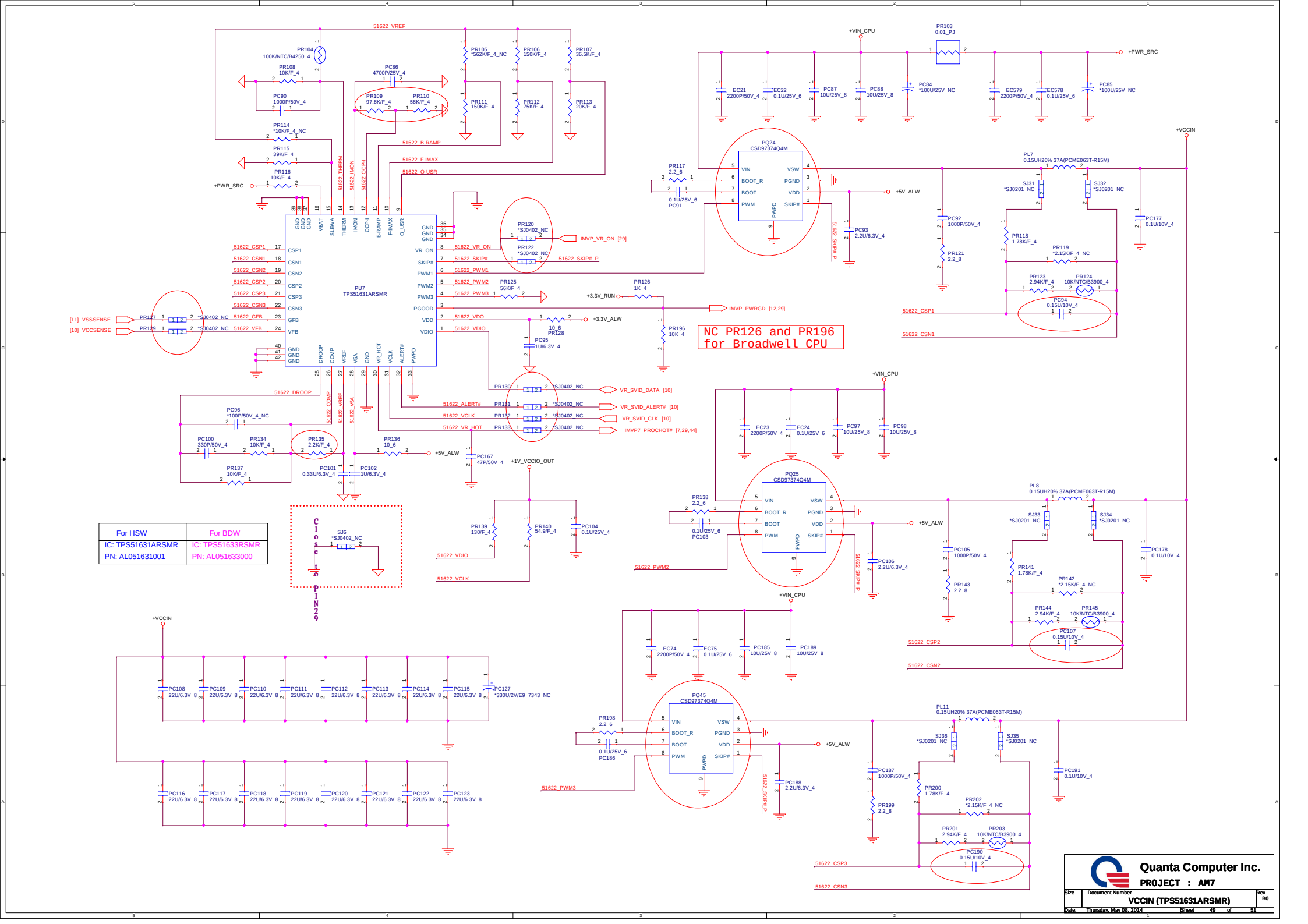
51622_VREF
PR104 100K/NTC/B4250_4
PR108 10K/F_4
PC90 1000P/50V_4
PC86 4700P/25V_4
PR109 97.6K/F_4
PR110 56K/F_4
PR105 *562K/F_4_NC
PR106 150K/F_4
PR107 36.5K/F_4
PR111 150K/F_4
PR112 75K/F_4
PR113 20K/F_4
PR114 *10K/F_4_NC
PR115 39K/F_4
PR116 10K/F_4
+PWR_SRC
51622_B-RAMP
51622_F-IMAX
51622_O-USR
51622_THERM
51622_IMON
51622_OCP-I
PU7
TPS51631ARSMR
GND GND GND VBAT SLEWA THERM IMON OCP-I B-RAMP F-IMAX O_USR
CSP1 CSN1 CSN2 CSP2 CSP3 CSN3 GFB VFB
VR_ON SKIP# PWM1 PWM2 PWM3 PGOOD VDD VDIO
DROOP COMP VREF VSA GND VR_HOT VCLK ALERT# PWRD
51622_CSP1 51622_CSN1 51622_CSN2 51622_CSP2 51622_CSP3 51622_CSN3 51622_GFB 51622_VFB
51622_VR_ON 51622_SKIP# 51622_PWM1 51622_PWM2 51622_PWM3 51622_VDO 51622_VDIO
[11] VSSSENSE
[10] VCCSENSE
PR127 *SJ0402_NC
PR129 *SJ0402_NC
PR120 *SJ0402_NC
PR122 *SJ0402_NC
IMVP_VR_ON [29]
51622_SKIP#_P
PR125 56K/F_4
+3.3V_RUN
PR126 1K_4
IMVP_PWRGD [12,29]
+3.3V_ALW
10_6 PR128
PR196 10K_4
PC95 1U/6.3V_4
NC PR126 and PR196 for Broadwell CPU
PC96 *100P/50V_4_NC
PC100 330P/50V_4
PR134 10K/F_4
PR135 2.2K/F_4
PR136 10_6
PR137 10K/F_4
PC101 0.33U/6.3V_4
PC102 1U/6.3V_4
+5V_ALW
PC167 47P/50V_4
+1V_VCCIO_OUT
PR130 *SJ0402_NC
PR131 *SJ0402_NC
PR132 *SJ0402_NC
PR133 *SJ0402_NC
VR_SVID_DATA [10]
VR_SVID_ALERT# [10]
VR_SVID_CLK [10]
IMVP7_PROCHOT# [7,29,44]
51622_ALERT#
51622_VCLK
51622_VR_HOT
51622_DROOP
51622_COMP
51622_VREF
51622_VSA
Close to PIN29
SJ6 *SJ0402_NC
PR139 130/F_4
PR140 54.9/F_4
PC104 0.1U/25V_4
51622_VDIO
51622_VCLK
For HSW
IC: TPS51631ARSMR
PN: AL051631001
For BDW
IC: TPS51633RSMR
PN: AL051633000
+VIN_CPU
PR103 0.01_PJ
+PWR_SRC
EC21 2200P/50V_4
EC22 0.1U/25V_6
PC87 10U/25V_8
PC88 10U/25V_8
PC84 *100U/25V_NC
EC579 2200P/50V_4
EC578 0.1U/25V_6
PC85 *100U/25V_NC
PQ24 CSD97374Q4M
VIN VSW BOOT_R PGND BOOT VDD PWM SKIP# PWPD
PR117 2.2_6
0.1U/25V_6 PC91
+5V_ALW
PC93 2.2U/6.3V_4
+VCCIN
PL7 0.15UH20% 37A(PCME063T-R15M)
SJ31 *SJ0201_NC
SJ32 *SJ0201_NC
PC92 1000P/50V_4
PR118 1.78K/F_4
PR119 *2.15K/F_4_NC
PR121 2.2_8
PR123 2.94K/F_4
PR124 10K/NTC/B3900_4
PC94 0.15U/10V_4
PC177 0.1U/10V_4
51622_CSP1
51622_CSN1
PC96 *100P/50V_4_NC
PC100 330P/50V_4
PR134 10K/F_4
PR135 2.2K/F_4
PR136 10_6
PR137 10K/F_4
PC101 0.33U/6.3V_4
PC102 1U/6.3V_4
+5V_ALW
PC167 47P/50V_4
+1V_VCCIO_OUT
PR139 130/F_4
PR140 54.9/F_4
PC104 0.1U/25V_4
51622_VDIO
51622_VCLK
+VIN_CPU
EC23 2200P/50V_4
EC24 0.1U/25V_6
PC97 10U/25V_8
PC98 10U/25V_8
PQ25 CSD97374Q4M
PR138 2.2_6
0.1U/25V_6 PC103
+5V_ALW
PC106 2.2U/6.3V_4
51622_PWM2
51622_SKIP#_P
PL8 0.15UH20% 37A(PCME063T-R15M)
SJ33 *SJ0201_NC
SJ34 *SJ0201_NC
PC105 1000P/50V_4
PR141 1.78K/F_4
PR142 *2.15K/F_4_NC
PR143 2.2_8
PR144 2.94K/F_4
PR145 10K/NTC/B3900_4
PC107 0.15U/10V_4
PC178 0.1U/10V_4
51622_CSP2
51622_CSN2
+VCCIN
PC108 22U/6.3V_8
PC109 22U/6.3V_8
PC110 22U/6.3V_8
PC111 22U/6.3V_8
PC112 22U/6.3V_8
PC113 22U/6.3V_8
PC114 22U/6.3V_8
PC115 22U/6.3V_8
PC127 *330U/2V/E9_7343_NC
PC116 22U/6.3V_8
PC117 22U/6.3V_8
PC118 22U/6.3V_8
PC119 22U/6.3V_8
PC120 22U/6.3V_8
PC121 22U/6.3V_8
PC122 22U/6.3V_8
PC123 22U/6.3V_8
+VIN_CPU
EC74 2200P/50V_4
EC75 0.1U/25V_6
PC185 10U/25V_8
PC189 10U/25V_8
PQ45 CSD97374Q4M
PR198 2.2_6
0.1U/25V_6 PC186
+5V_ALW
PC188 2.2U/6.3V_4
51622_PWM3
51622_SKIP#_P
PL11 0.15UH20% 37A(PCME063T-R15M)
SJ36 *SJ0201_NC
SJ35 *SJ0201_NC
PC187 1000P/50V_4
PR200 1.78K/F_4
PR199 2.2_8
PR202 *2.15K/F_4_NC
PR201 2.94K/F_4
PR203 10K/NTC/B3900_4
PC190 0.15U/10V_4
PC191 0.1U/10V_4
51622_CSP3
51622_CSN3
Quanta Computer Inc.
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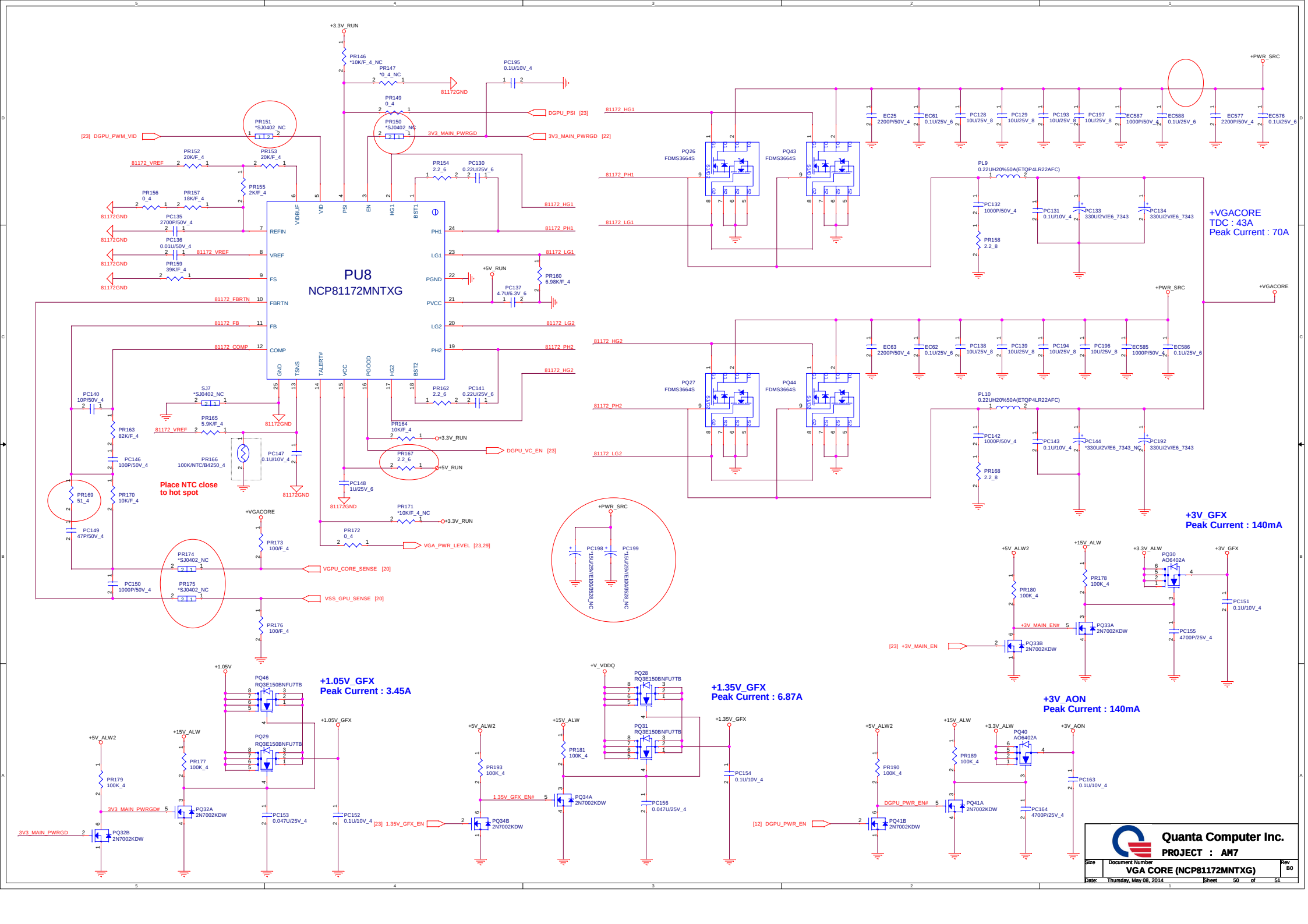
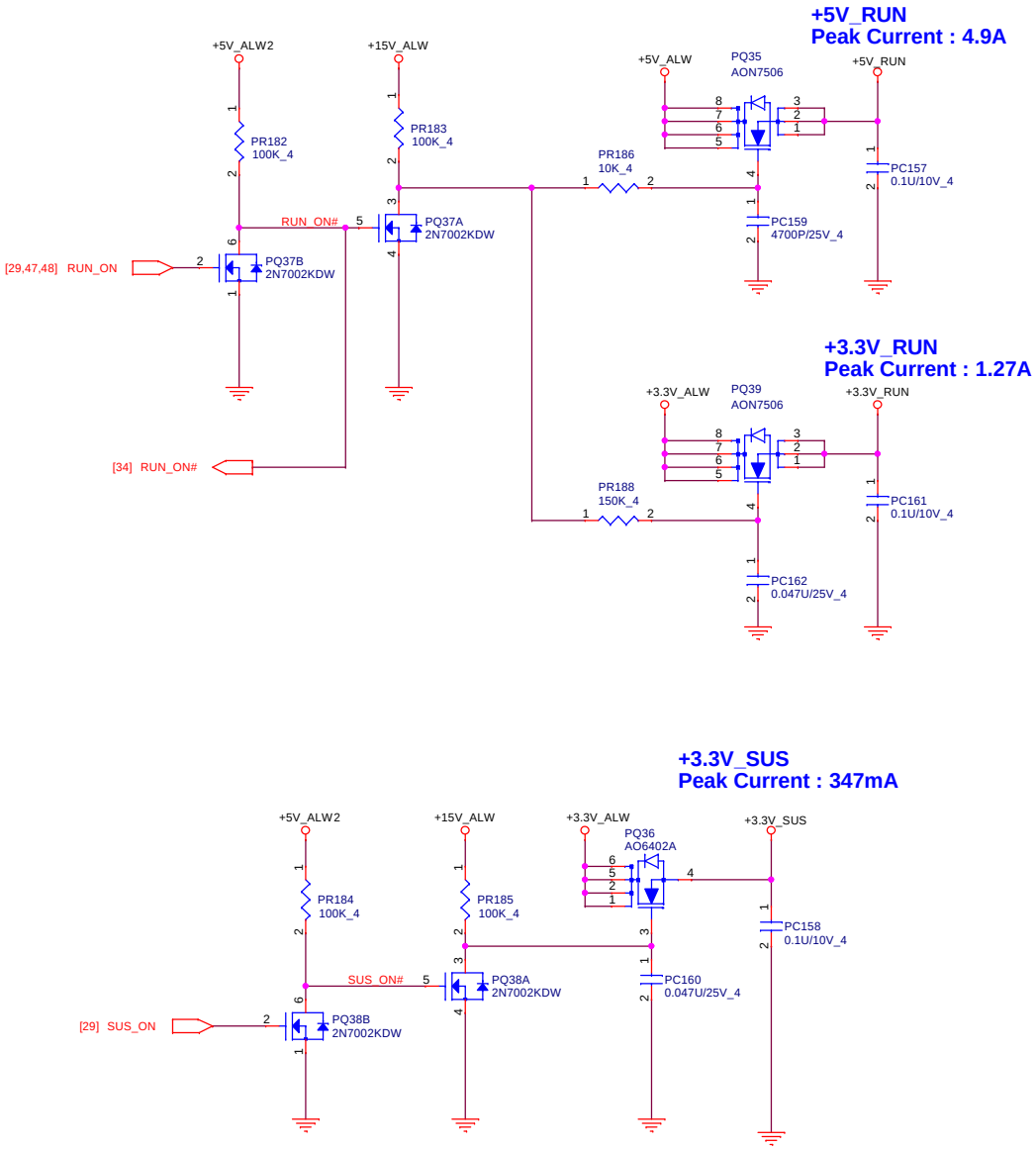

PU8
NCP81172MNTXG
+VGACORE
TDC : 43A
Peak Current : 70A
+3V_GFX
Peak Current : 140mA
+1.05V_GFX
Peak Current : 3.45A
+1.35V_GFX
Peak Current : 6.87A
+3V_AON
Peak Current : 140mA
Place NTC close to hot spot
Quanta Computer Inc.
PROJECT : AM7
VGA CORE (NCP81172MNTXG)
Thursday, May 08, 2014



Quanta Computer Inc.		
PROJECT : AM7		
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