Rayleigh_SLS

Schematics Document

<Core Design>

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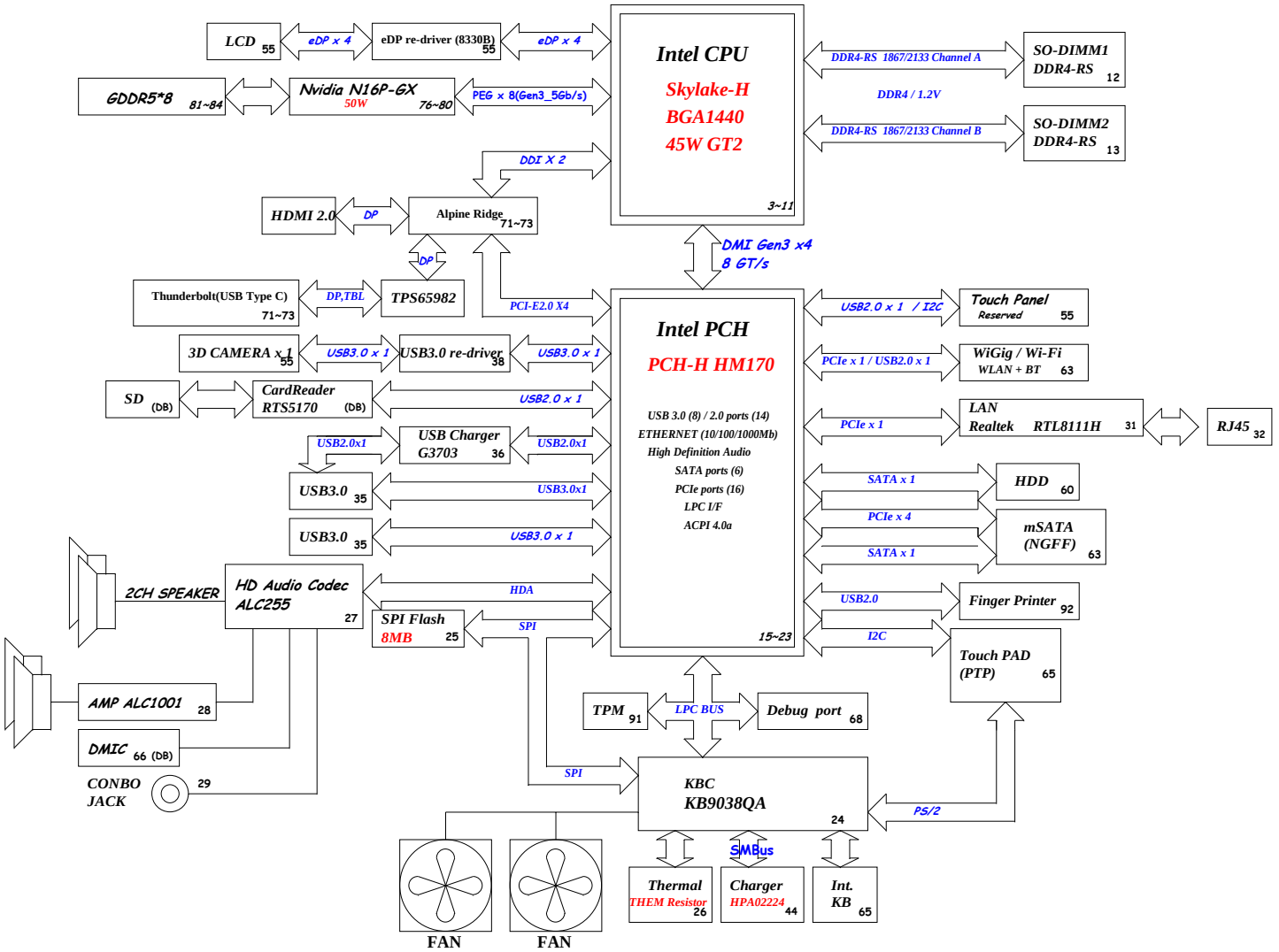
Title: *Cover Page*		
Size: A	Document Number: Rayleigh_SLS	Rev: SA
Date: Wednesday, August 12, 2015	Sheet 1 of 105	

Rayleigh_SLS Board Block Diagram

Project code :
PCB P/N :
Revision :



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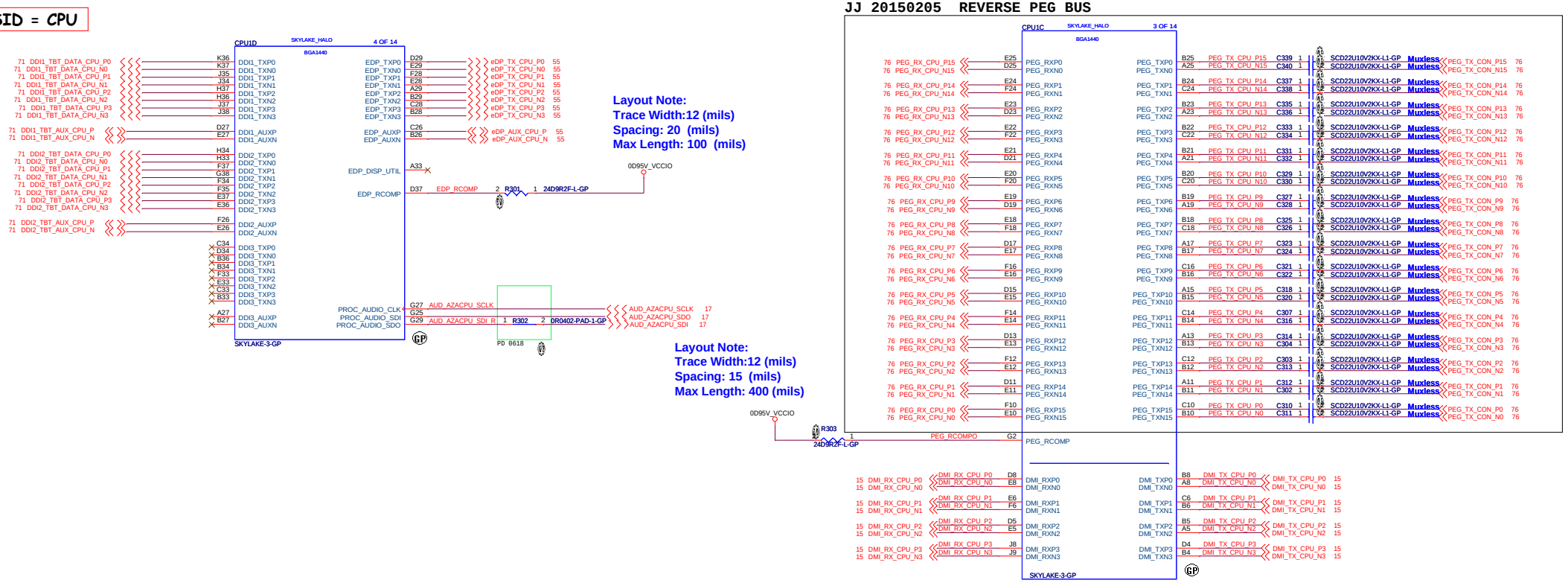
Title: Block Diagram

Size	Document Number	Rev
C	Rayleigh_SLS	SA

Date: Wednesday, August 12, 2015 Sheet 2 of 105

SSID = CPU

JJ 20150205 REVERSE PEG BUS



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Title	CPU (PCIE/DMI/FDI)
Size: Custom	Document Number: Rayleigh_SLS
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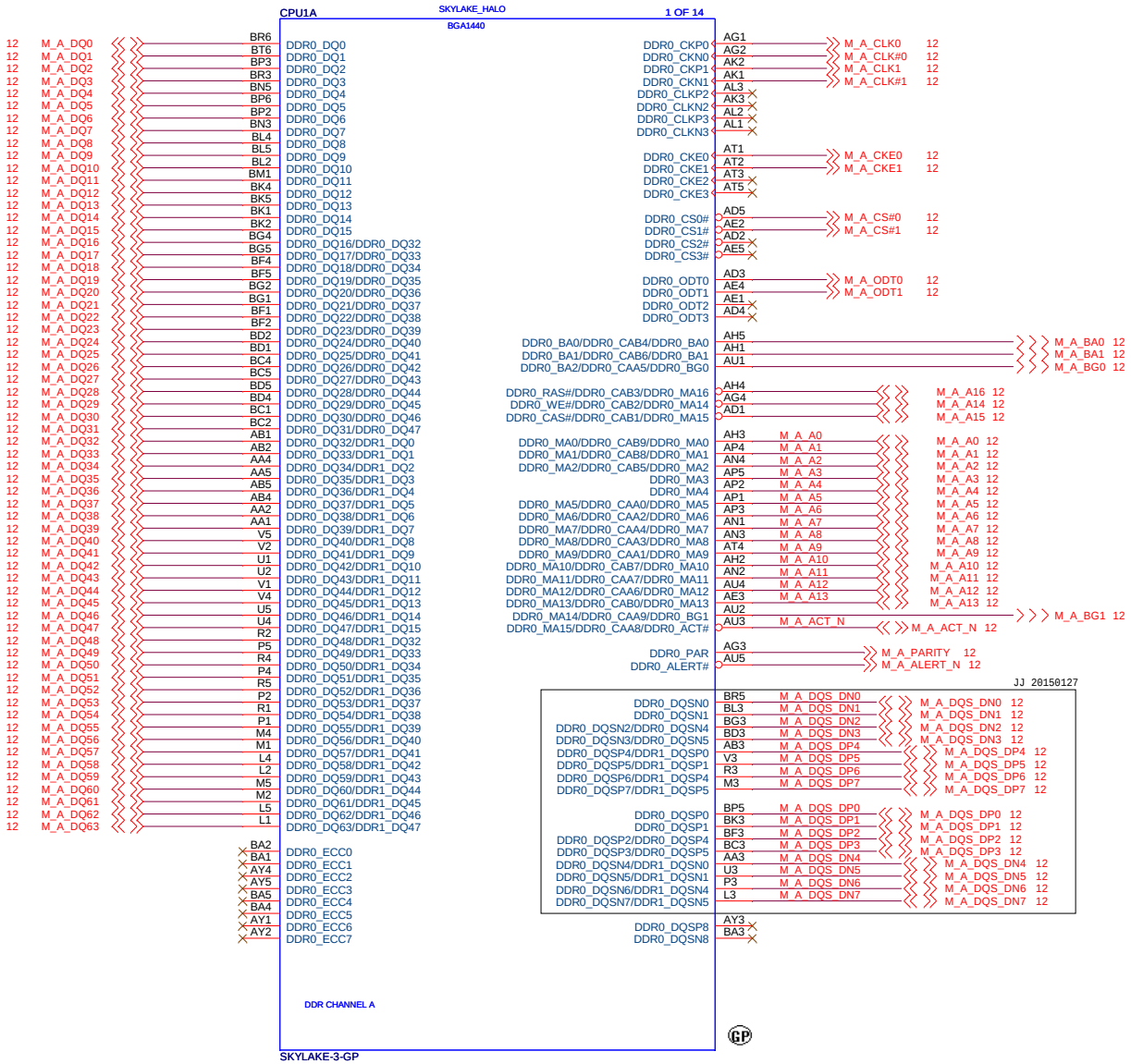
Date: Wednesday, August 12, 2015	Sheet 3 of 105



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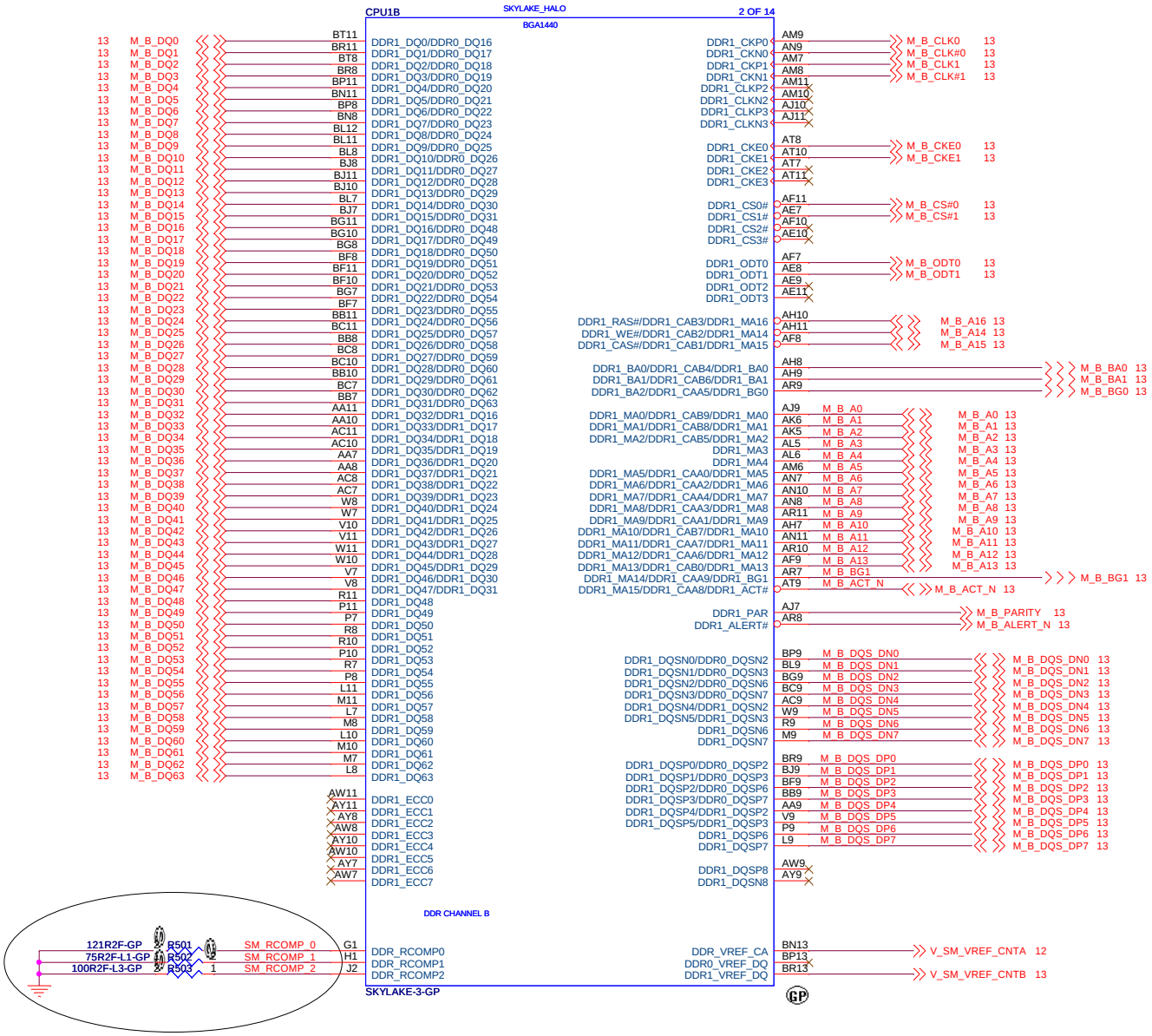
Title: CPU_DDR_CHA

Size: A3 | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 4 of 105

SSID = CPU



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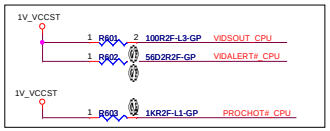
Title: CPU_DDR_CHB

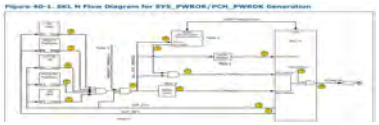
Size: A3 | Document Number: Rayleigh_SLS | Rev: SA

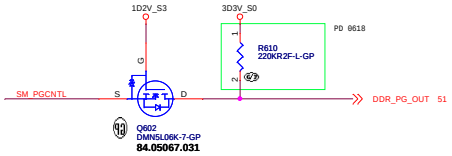
Date: Wednesday, August 12, 2015 | Sheet 5 of 105

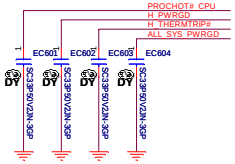
SSID = CPU

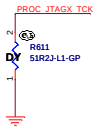
AROUND_CPU

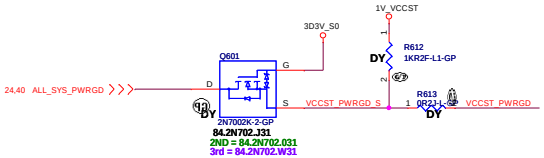


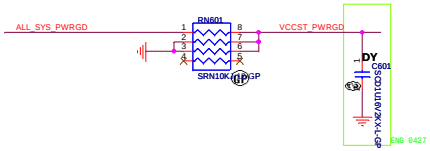












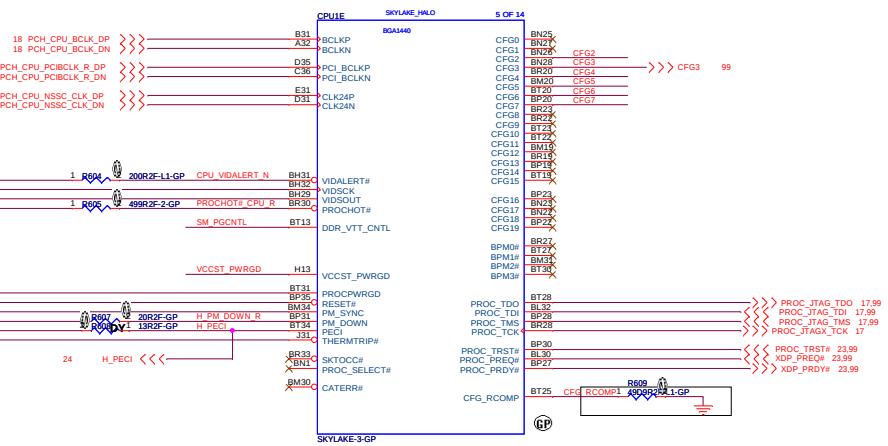


Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: – 1 = (Default) Normal Operation; No stall. – 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: – 1 = Disabled. – 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

Processor Internal Pull-Up / Pull-Down Terminations

Processor Internal Pull-Up / Pull-Down Terminations

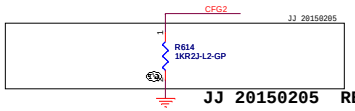
Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up	Vcc_{IO}	16-60 Ω
PREQ#	Pull Up	Vcc_{ST}	3 kΩ
PROC_TDI	Pull Up	Vcc_{STG}[1]	3 kΩ
PROC_TMS	Pull Up	Vcc_{SGT}[1]	3 kΩ
CFG[19:0]	Pull Up	Vcc_{IO}	3 kΩ

Note:
1. For SKL-S it should be Vcc_{ST}

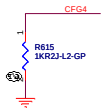
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

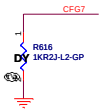
eDP Enable	
CFG4	1:Disable 0:Enable

PEG Training	
CFG7	1:(default) PEG Train immediately following RESET# de assertion. 0 = PEG Wait for BIOS for training.



JJ 20150205 REVERSE PEG BUS





PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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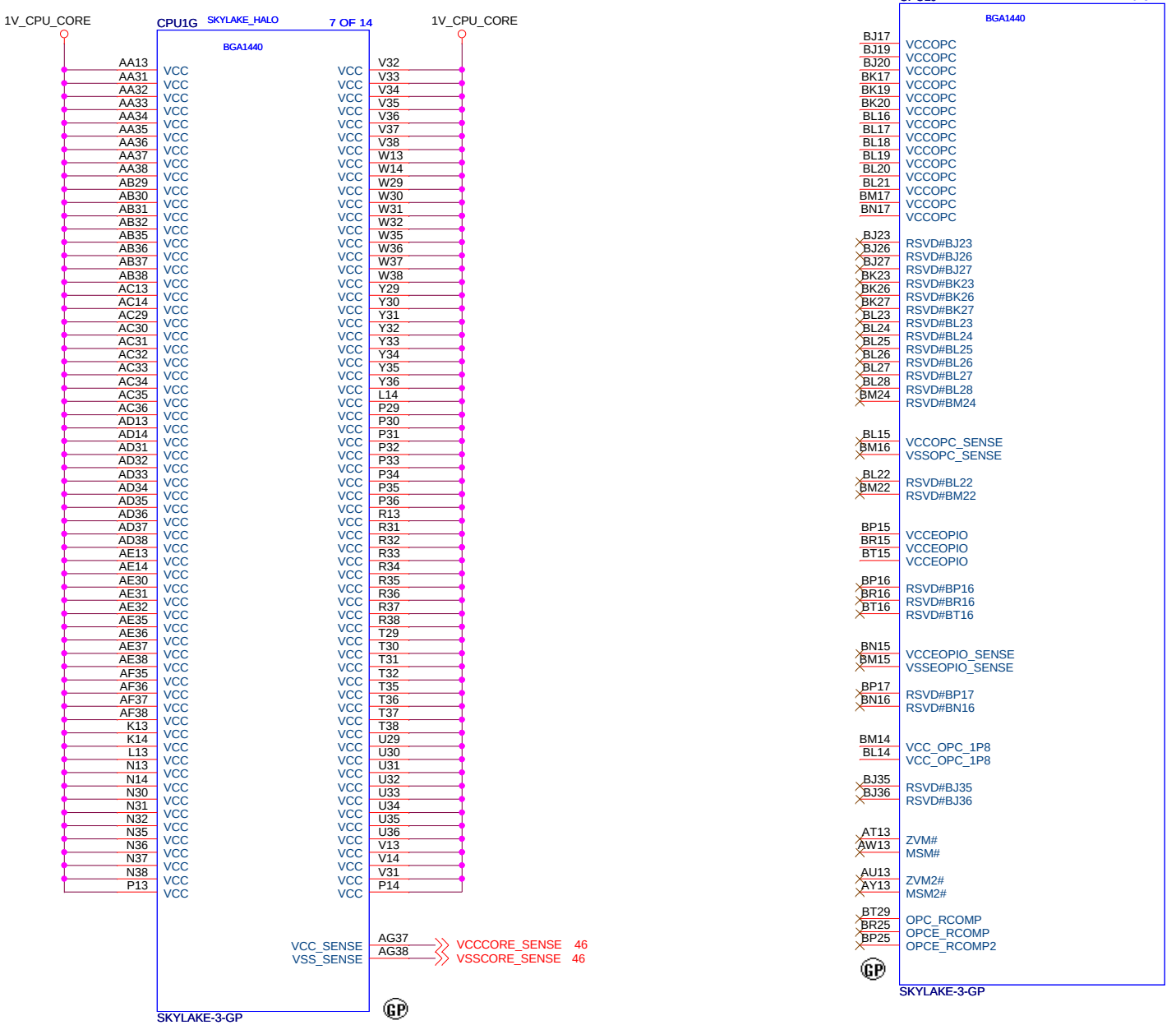
Title: CPU_CFG_CFG STRAP

Size: A2 | Document Number: Rayleigh_SLS | Rev: SA

Date: Tuesday, September 08, 2015 | Sheet 6 of 105



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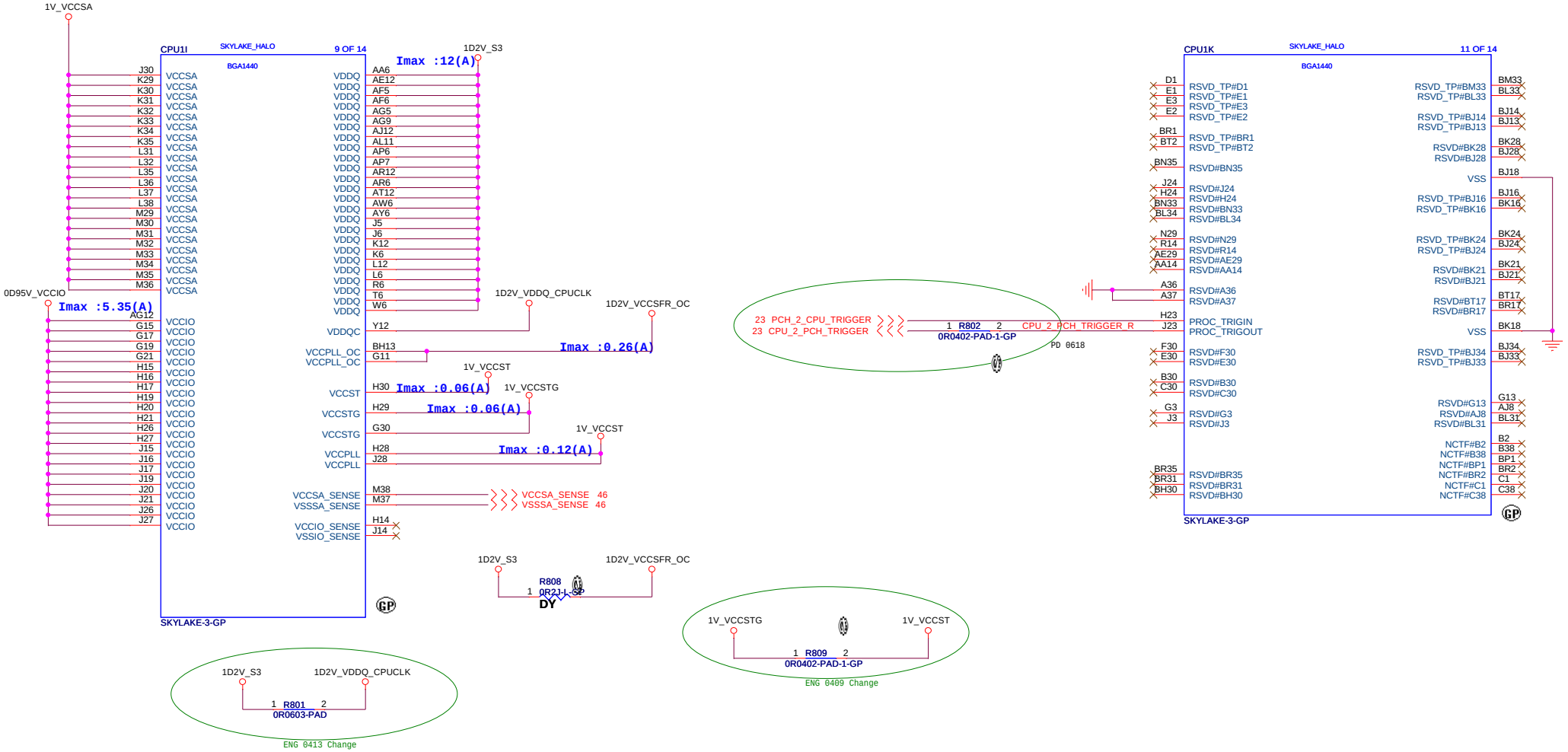
Title: ***CPU_POWER1 (ASIC Power Bolck)***

Size	Document Number	Rev
Custom	Rayleigh_SLS	SA

Date: Wednesday, August 12, 2015 Sheet 7 of 105

SSID = CPU



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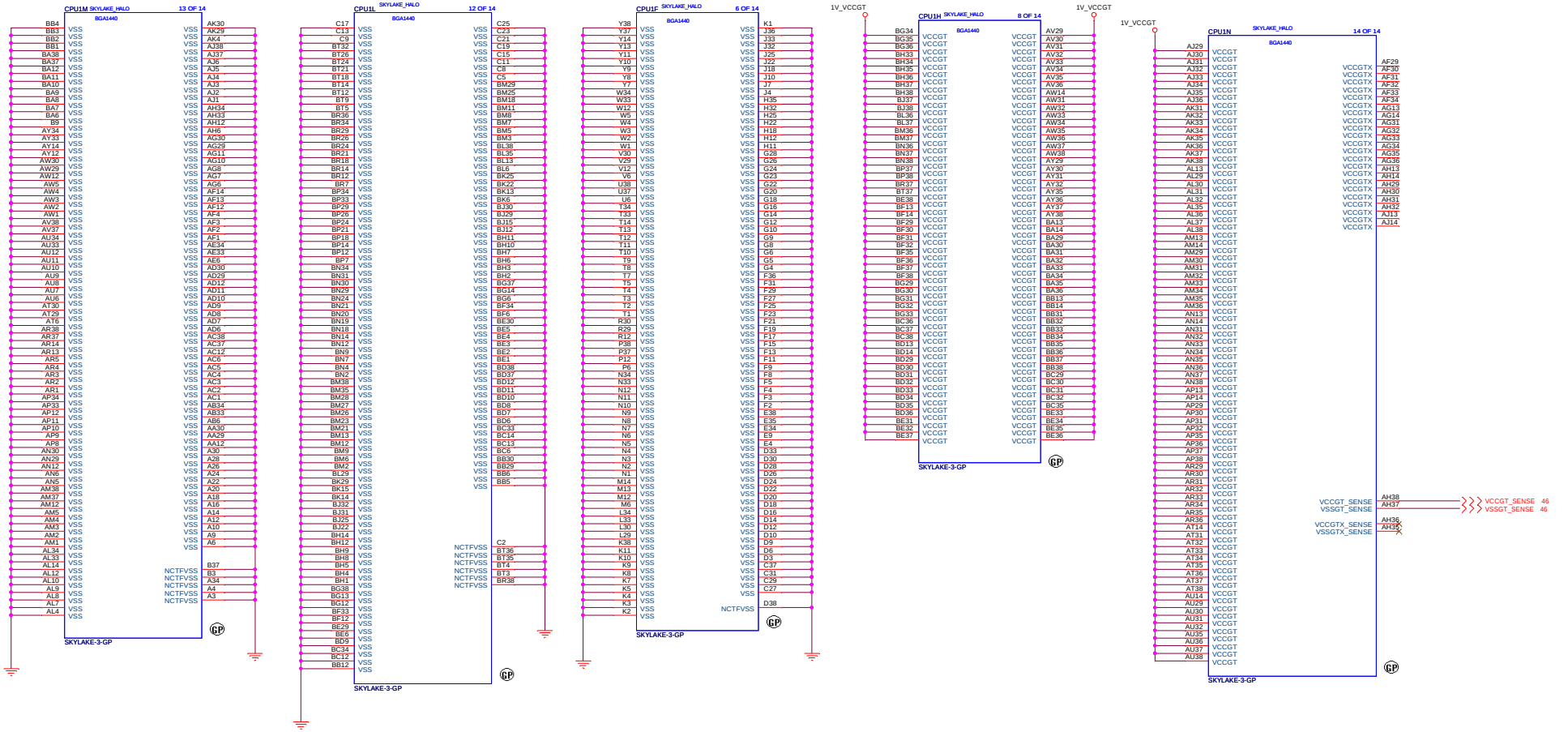
Title: CPU_POWER2(ASIC Power Bolck)

Size: A3 | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 8 of 105

SSID = CPU



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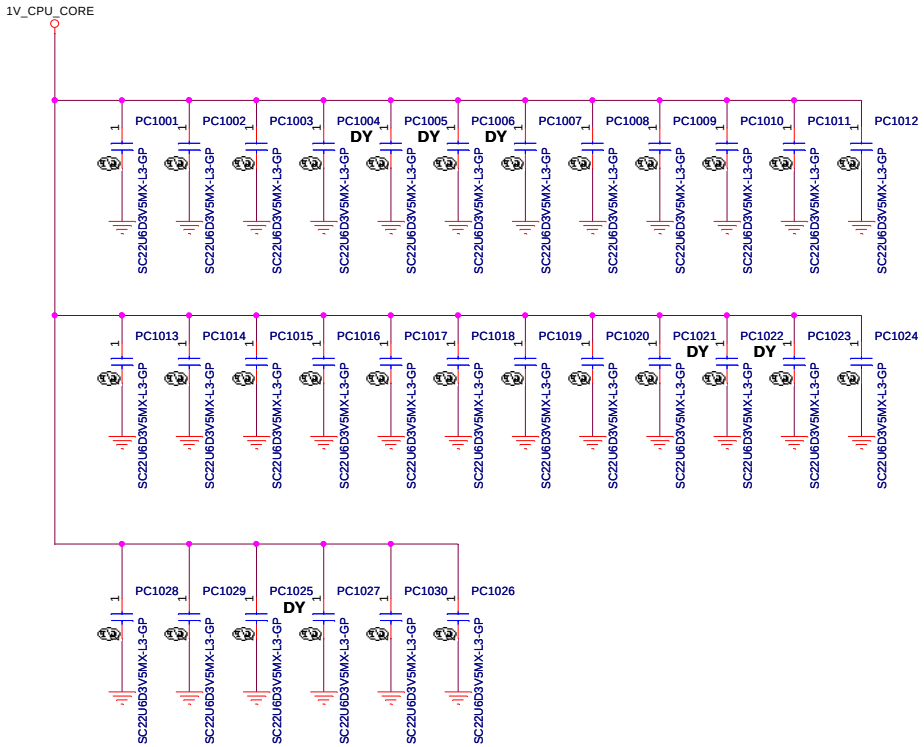
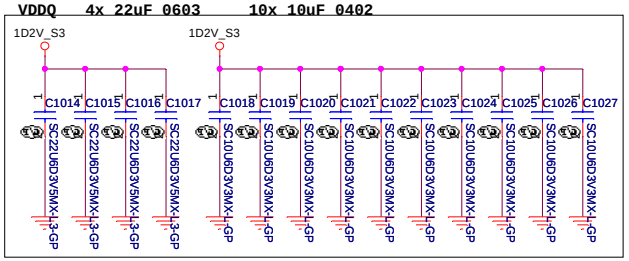
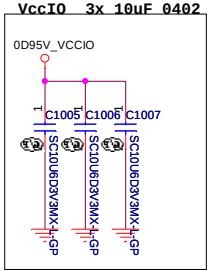
Title: CPU_POWER3(ASIC Power Bolck)

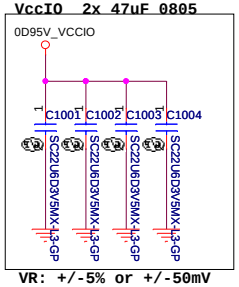
Size	Document Number	Rev
A2	Rayleigh_SLS	SA

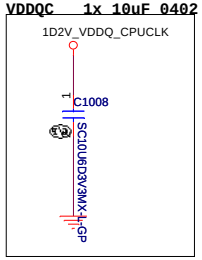
Date: Wednesday, August 12, 2015 Sheet 9 of 105

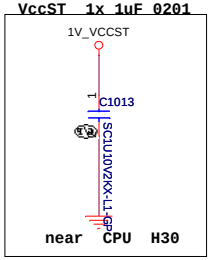




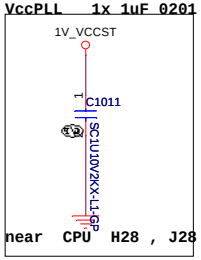


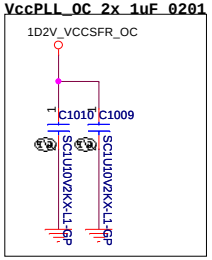


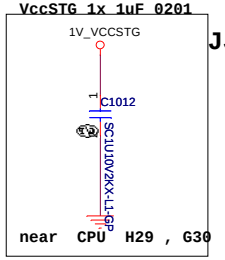




VR: +/-5% or +/-50mV
Place close to VR output







JJ 20150130

Decoupling Requirements for SKL H Processor (Sheet 2 of 2)

Domain	Board Edge cap	Backside cap	Notes
$V_{CC_{GT}}$	6x 47uF 0805		
		8x 22uF 0603	
		35x 10uF 0402	
		68x 1uF 0201	
$V_{CC_{GTx}}$	8x 22uF 0603		
		4x 10uF 0402	
		12x 1uF 0201	
$V_{CC_{SA}}$	1x 47uF 0805		
		1x 47uF 0805	
		7x 10uF 0402	
		3x 1uF 0201	
V_{DDQ}		4x 22uF 0603	Share supply with DRAM
		10x 10uF 0402	
V_{DDQC}		1x 10uF 0402	
$V_{CC_{IO}}$	2x 47uF 0805		VR: +/-5% or +/-50mV Place close to VR output
		3x 10uF 0402	
$V_{CC_{ST}}$		1x 1uF 0201	
$V_{CC_{STG}}$		1x 1uF 0201	Share supply with 1.0V PCH rail
$V_{CC_{PLL}}$		1x 1uF 0201	
$V_{CC_{PLL\_OC}}$		2x 1uF 0201	Supply from 1.2V V_{DDQ}
$V_{CC_{DMC}}$		10x 10uF 0402	VR: +/-5% or +/-50mV
$V_{CC_{SCPHG}}$		3x 10uF 0402	VR: +/-5% or +/-50mV

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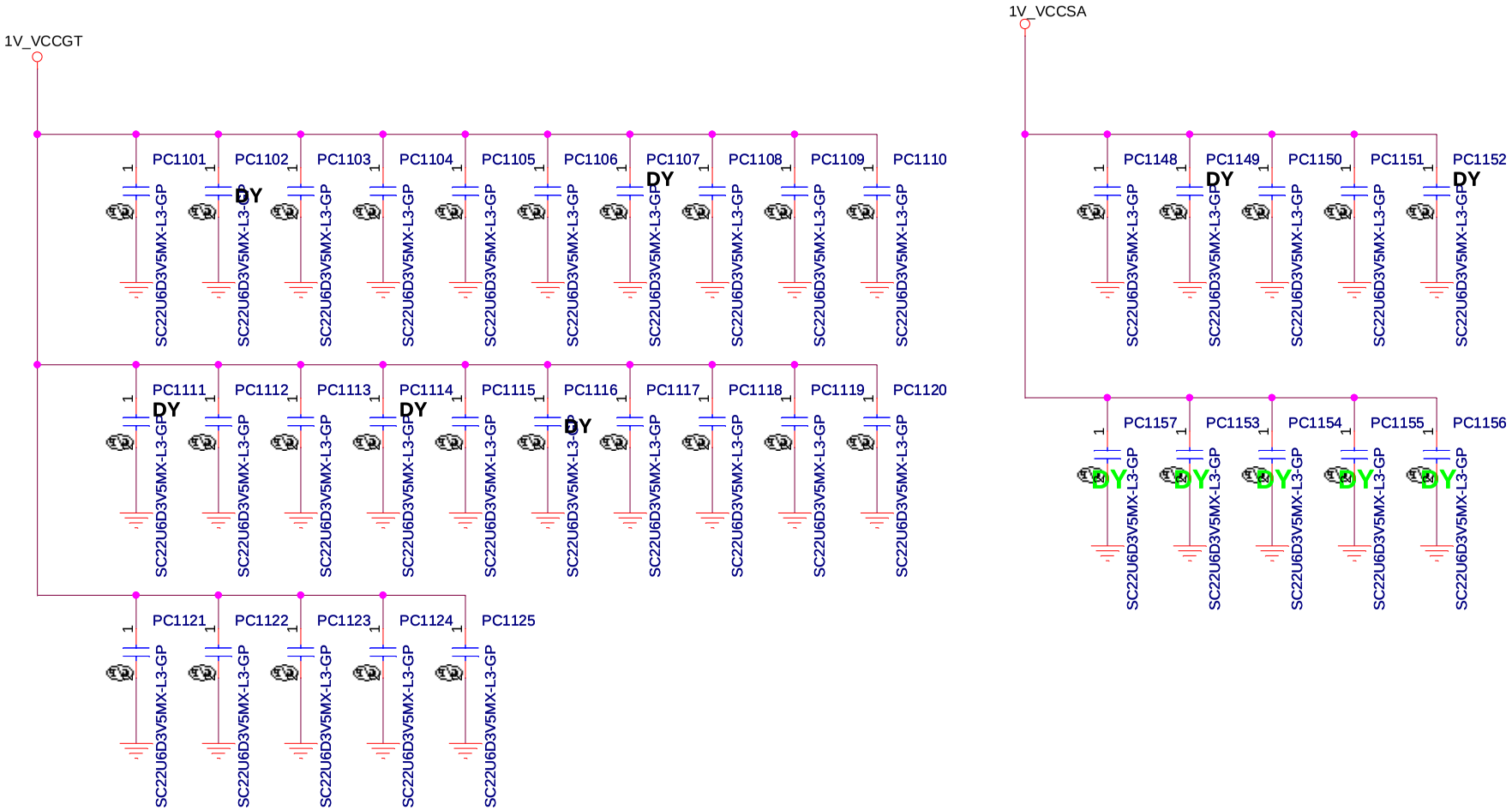
Title: 010_CPU (Power CAP1)

Size: A3 | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 10 of 105



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Title: **CPU (Power CAP2)**

Size	Document Number	Rev
A4	Rayleigh_SLS	SA

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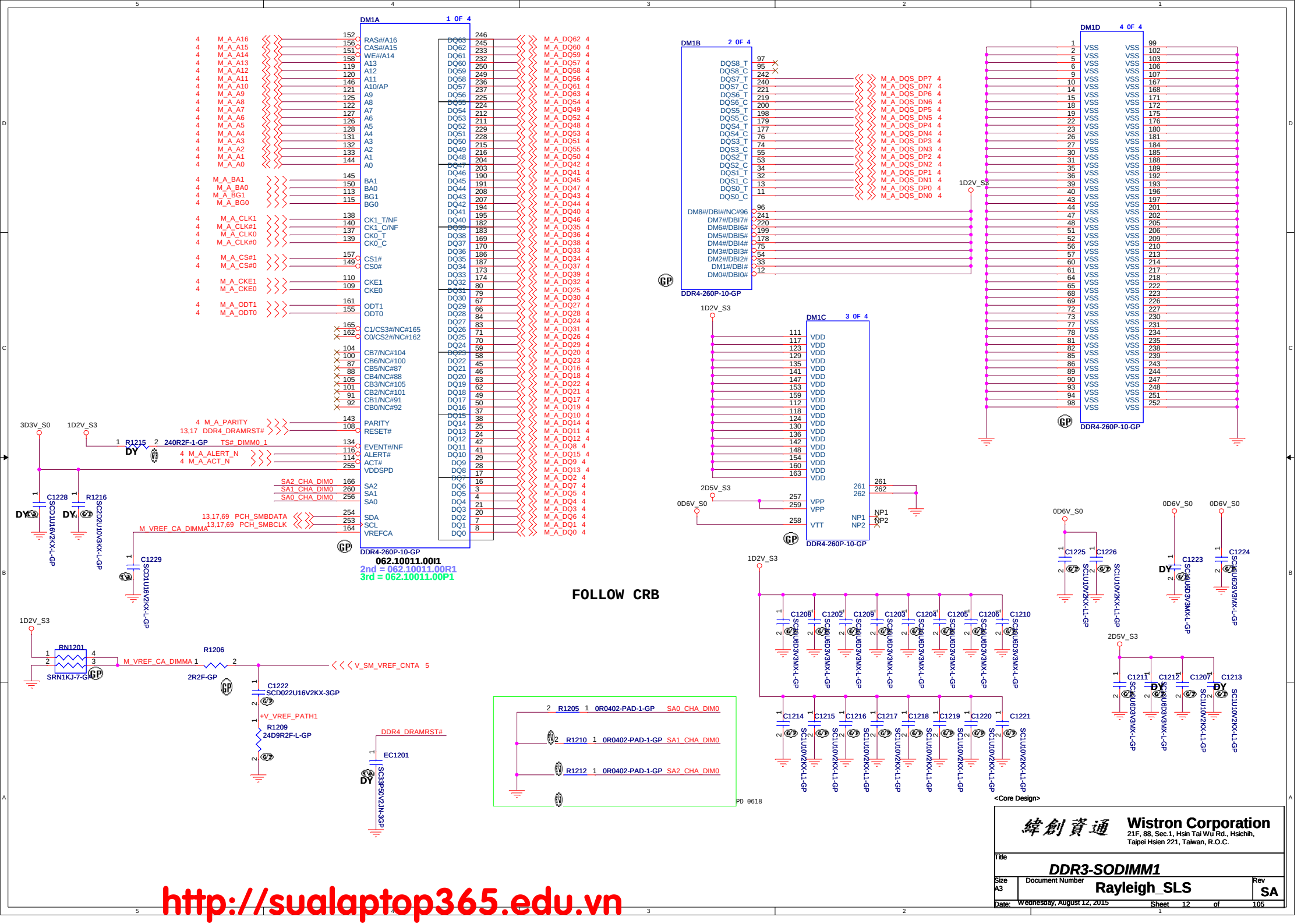
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1 OF 4
DDR4-260P-10-GP
062.10011.00I1
2nd = 062.10011.00R1
3rd = 062.10011.00P1
DM1B
2 OF 4
DDR4-260P-10-GP
DM1C
3 OF 4
DDR4-260P-10-GP
DM1D
4 OF 4
DDR4-260P-10-GP
FOLLOW CRB
<Core Design>
PD 0618
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DDR3-SODIMM1
Rayleigh_SLS
SA
Wednesday, August 12, 2015
12
105
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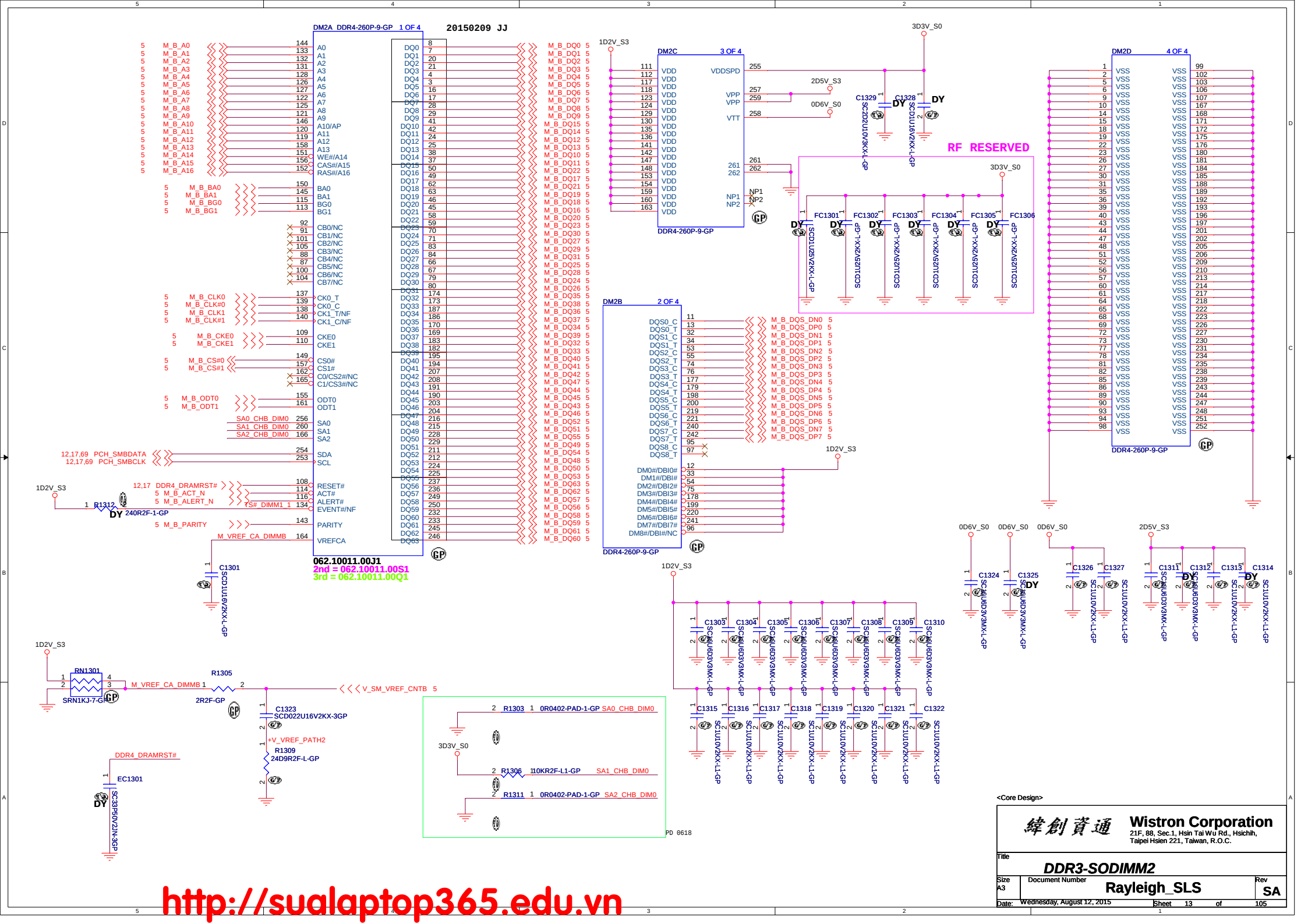

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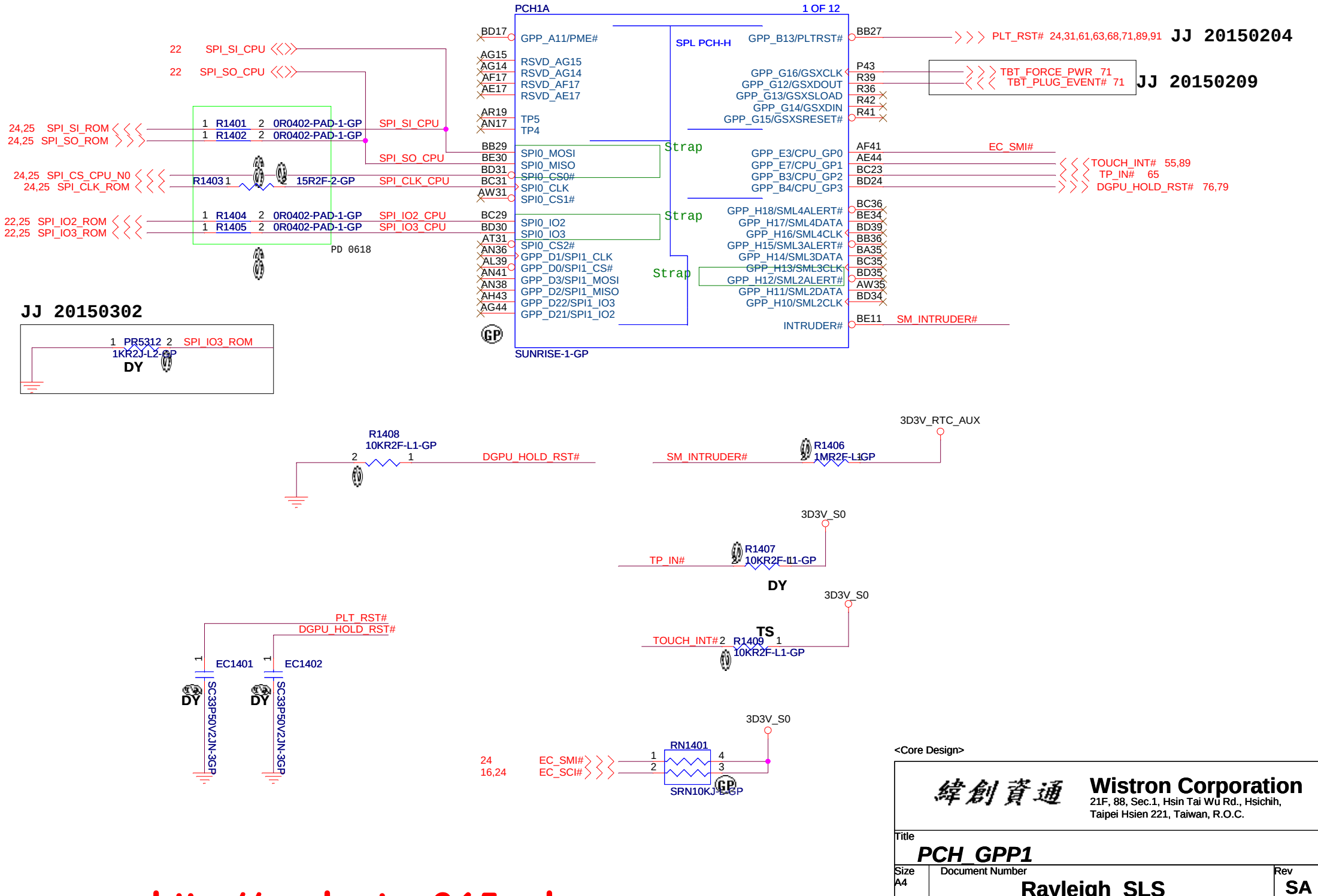
Title: DDR3-SODIMM2

Size: A3 | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 13 of 105



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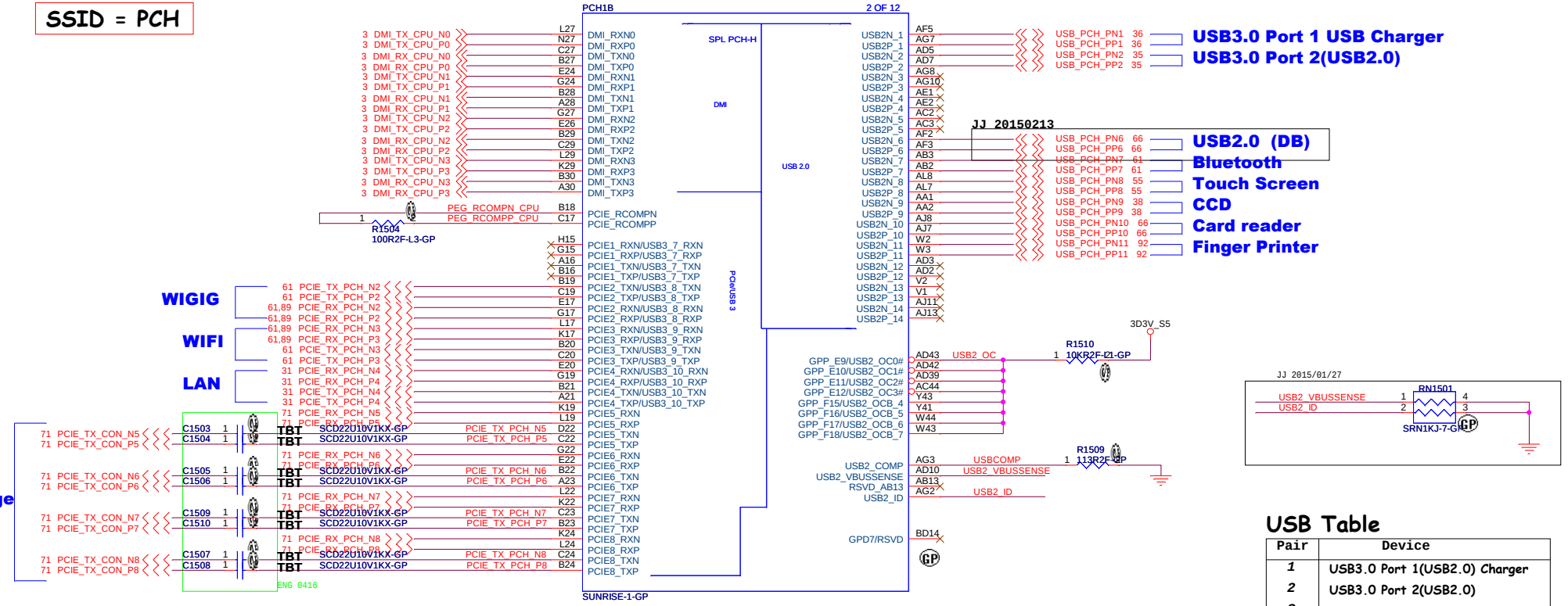
Title: PCH_GPP1
Size: A4
Document Number: Rayleigh_SLS
Rev: SA
Date: Wednesday, August 12, 2015
Sheet 14 of 105

SSID = PCH



USB Table

Pair	Device
1	USB3.0 Port 1(USB2.0) Charger
2	USB3.0 Port 2(USB2.0)
3	
4	
5	USB2.0
6	
7	Bluetooth
8	Touch Screen
9	CCD
10	Card reader
11	Finger Printer
12	
13	
14	

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Title: PCH_PCIE_DMI_USB

Size	Document Number	Rev
A3	Rayleigh_SLS	SA

Date: Wednesday, August 12, 2015 Sheet 15 of 105

SSID = PCH

PCH1C

3 OF 12

SPL PCH-H

CLINK

FAN

PCIe/SATA

HOST

AV2 CL_CLK
AV3 CL_DATA
AW2 CL_RST#

R44 GPP_G8/FAN_PWM_0
R43 GPP_G9/FAN_PWM_1
U39 GPP_G10/FAN_PWM_2
N42 GPP_G11/FAN_PWM_3

U43 GPP_G0/FAN_TACH_0
U42 GPP_G1/FAN_TACH_1
U41 GPP_G2/FAN_TACH_2
M44 GPP_G3/FAN_TACH_3
U36 GPP_G4/FAN_TACH_4
P44 GPP_G5/FAN_TACH_5
T45 GPP_G6/FAN_TACH_6
T44 GPP_G7/FAN_TACH_7

14,24 EC_SCI#
38,89 FW_GPIO

MSATA

B33 PCIE11_TXP
C33 PCIE11_TXN
K31 PCIE11_RXP
L31 PCIE11_RXN

63 PCIE_TX_PCH_P11
63 PCIE_TX_PCH_N11
63 PCIE_RX_PCH_P11
63 PCIE_RX_PCH_N11

AB33 GPP_F10/SCLOCK
AB35 GPP_F11/SLOAD
AA44 GPP_F13/SDATAOUT0
AA45 GPP_F12/SDATAOUT1

B38 PCIE14_TXN/SATA1B_TXN
C38 PCIE14_TXP/SATA1B_TXP
D39 PCIE14_RXN/SATA1B_RXN
E37 PCIE14_RXP/SATA1B_RXP

C36 PCIE13_TXN/SATA0B_TXN
B36 PCIE13_TXP/SATA0B_TXP
G35 PCIE13_RXN/SATA0B_RXN
E35 PCIE13_RXP/SATA0B_RXP

MSATA

A35 PCIE12_TXP
B35 PCIE12_TXN
H33 PCIE12_RXP
G33 PCIE12_RXN

63 PCIE_TX_PCH_P12
63 PCIE_TX_PCH_N12
63 PCIE_RX_PCH_P12
63 PCIE_RX_PCH_N12

J45 PCIE20_TXP
K44 PCIE20_TXN
N38 PCIE20_RXP
N39 PCIE20_RXN
H44 PCIE19_TXP
H43 PCIE19_TXN
L39 PCIE19_RXP
L37 PCIE19_RXN

SUNRISE-1-GP

PCIE9_RXN/SATA0A_RXN G31
PCIE9_RXP/SATA0A_RXP H31
PCIE9_TXN/SATA0A_TXN C31
PCIE9_TXP/SATA0A_TXP B31

SATA_RX_PCH_N0 63
SATA_RX_PCH_P0 63
SATA_TX_PCH_N0 63
SATA_TX_PCH_P0 63

MSATA

PCIE10_RXN/SATA1A_RXN G29
PCIE10_RXP/SATA1A_RXP E29
PCIE10_TXN/SATA1A_TXN C32
PCIE10_TXP/SATA1A_TXP B32

PCIE_RX_PCH_N10 63
PCIE_RX_PCH_P10 63
PCIE_TX_PCH_N10 63
PCIE_TX_PCH_P10 63

PCIE15_RXN/SATA2_RXN F41
PCIE15_RXP/SATA2_RXP E41
PCIE15_TXN/SATA2_TXN B39
PCIE15_TXP/SATA2_TXP A39

SATA_RX_CPU_N2 60
SATA_RX_CPU_P2 60
SATA_TX_CPU_N2 60
SATA_TX_CPU_P2 60

HDD

PCIE16_RXN/SATA3_RXN D43
PCIE16_RXP/SATA3_RXP E42
PCIE16_TXN/SATA3_TXN A41
PCIE16_TXP/SATA3_TXP A40

PCIE17_RXN/SATA4_RXN H42
PCIE17_RXP/SATA4_RXP H40
PCIE17_TXN/SATA4_TXN E45
PCIE17_TXP/SATA4_TXP F45

PCIE18_RXN/SATA5_RXN K37
PCIE18_RXP/SATA5_RXP G37
PCIE18_TXN/SATA5_TXN G45
PCIE18_TXP/SATA5_TXP G44

3D3V_S0

RN1601
SATAGP0 1 4
SATA_LED# 2 3
SRN10KJ-L-GP

GPP_E8/SATALED# AD44 SATA_LED#

GPP_E0/SATAXPCIE0/SATAGP0 AG36 SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1 AG35
GPP_E2/SATAXPCIE2/SATAGP2 AG39
GPP_F0/SATAXPCIE3/SATAGP3 AD35
GPP_F1/SATAXPCIE4/SATAGP4 AD31
GPP_F2/SATAXPCIE5/SATAGP5 AD38
GPP_F3/SATAXPCIE6/SATAGP6 AC43
GPP_F4/SATAXPCIE7/SATAGP7 AB44

SATAGP0 63

GPP_F21/EDP_BKLTCTL W36
GPP_F20/EDP_BKLTEN W35
GPP_F19/EDP_VDDEN W42

eDP_BLCTRL_CPU 55
eDP_BLEN_CPU 24
eDP_VDDEN_CPU 55

eDP

THERMTRIP# AJ3 PCH_THERMTRIP#
PECI AL3
PM_SYNC AJ4 H_PM_SYNC_R
PLTRST_CPU# AK2
PM_DOWN AH2

R1603 1 30R2J-1-GP

PCH_PECI 6
H_PM_SYNC 6
PLTRST# 6
H_PM_DOWN 6

RN1602
eDP_BLEN_CPU 1 4
eDP_BLCTRL_CPU 2 3
SRN100KJ-L-GP

PCH_THERMTRIP#
PLTRST#

EC1601 DY SC33P50V2JN-3GP
EC1602 DY SC33P50V2JN-3GP

1V_VCCST

R1601 1KR2F-L1-GP

PCH_THERMTRIP# R1602 620R2F-GP H_THERMTRIP# 6

AROUND PCH

<Core Design>

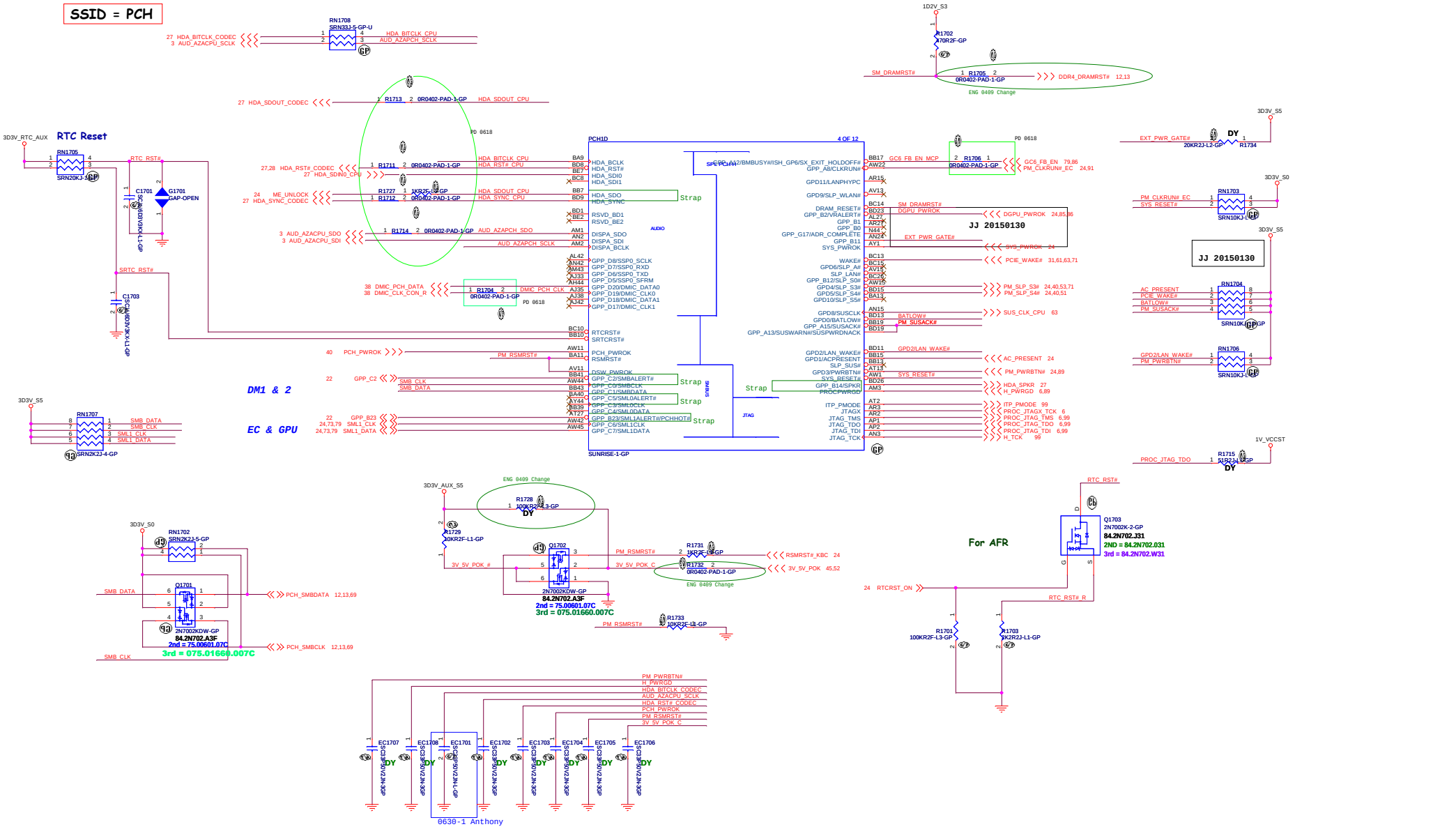
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_PCIE_SATA

Size	Document Number	Rev
A4	Rayleigh_SLS	SA

Date: Wednesday, August 12, 2015 Sheet 16 of 105

SSID = PCH



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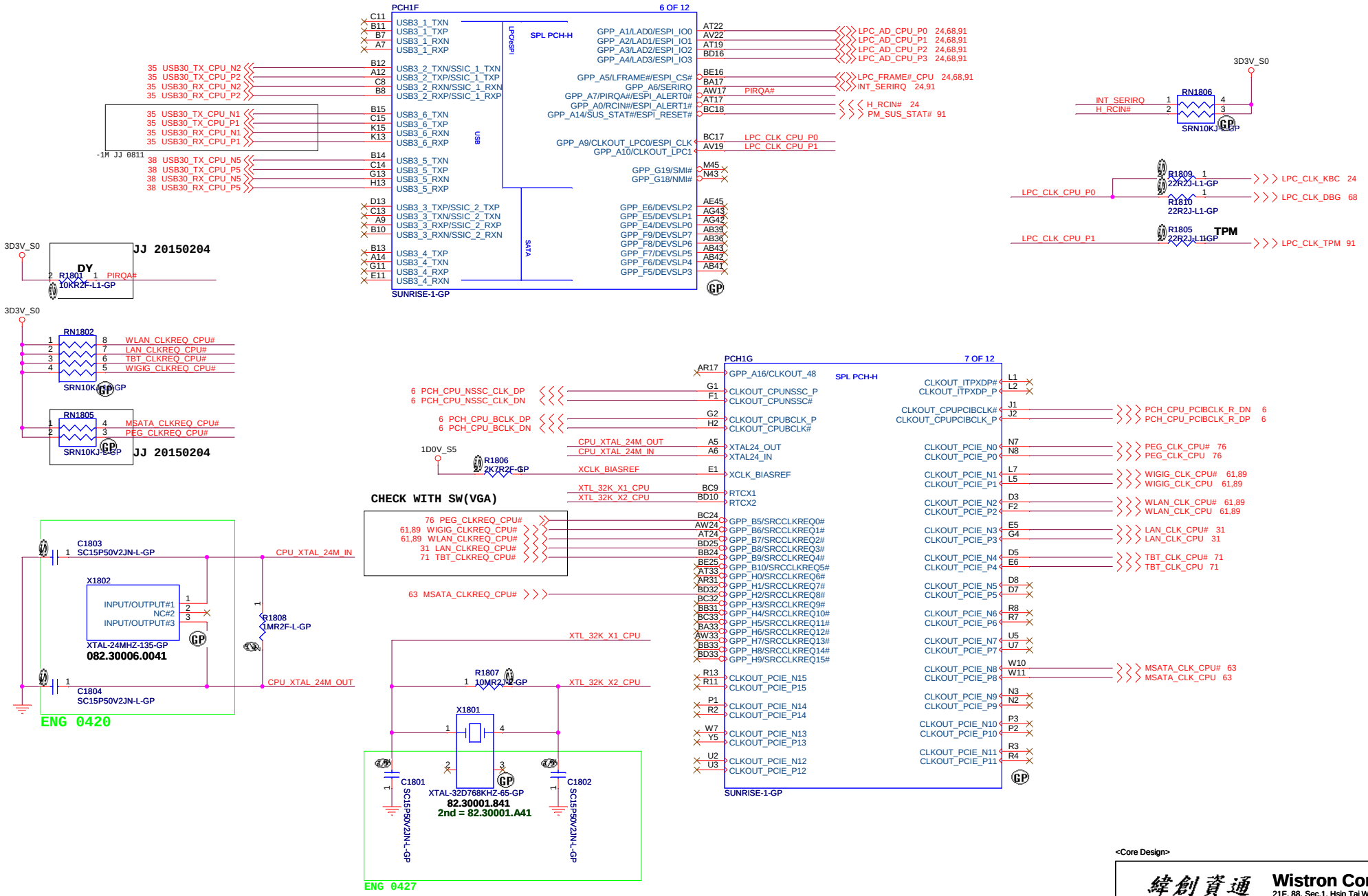
Title: PCH_HDA_GPP1_JTAG

Size: A2 | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 17 of 105

SSID = PCH



<Core Design>

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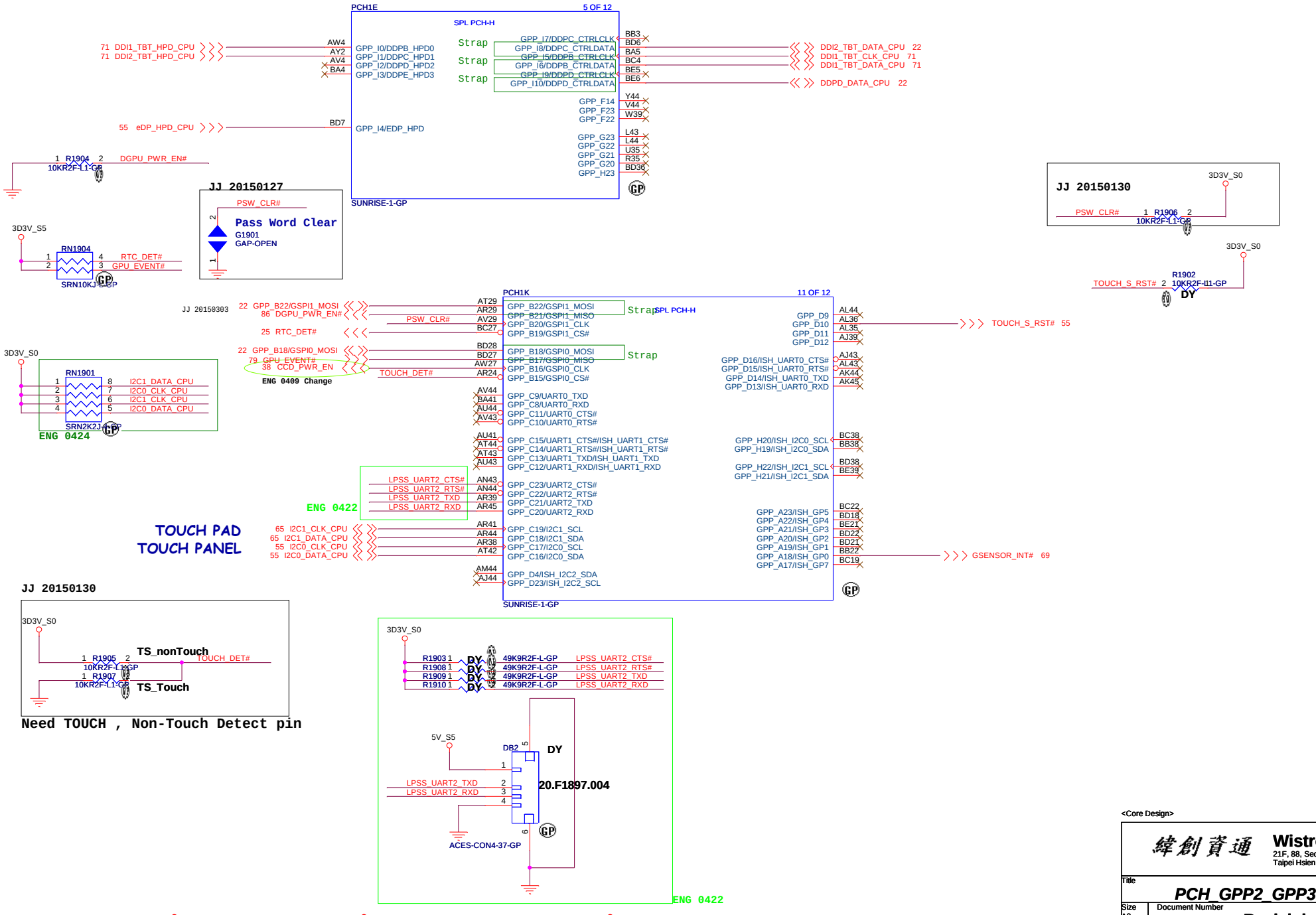
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_USB3_CLOCK

Size: A3 | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 18 of 105

SSID = PCH



<Core Design>

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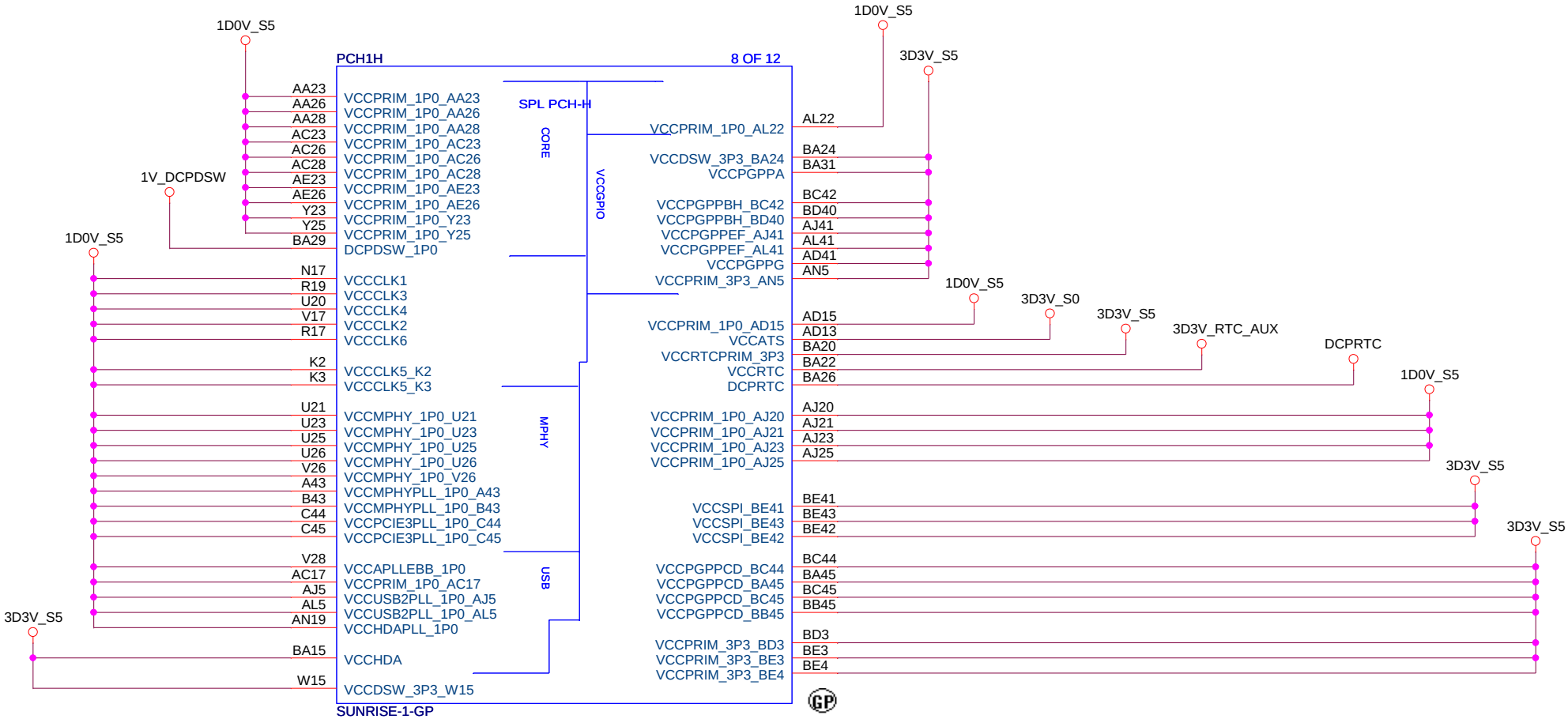
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_GPP2_GPP3

Size: A3 | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 19 of 105

SSID = PCH



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

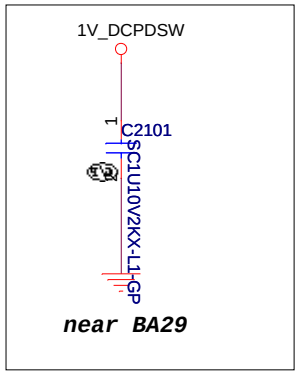
Title: ***PCH_POWER_VCCPRIM_VCCMPHY***

Size	Document Number	Rev
A4	Rayleigh_SLS	SA

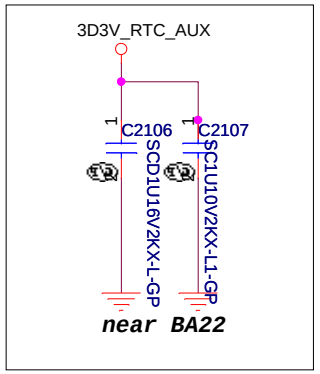
Date: Wednesday, August 12, 2015 Sheet 20 of 105

SSID = PCH

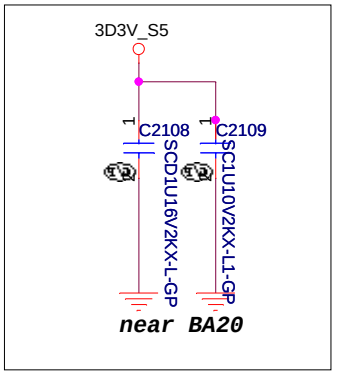
DcpDSW
1x 1uF



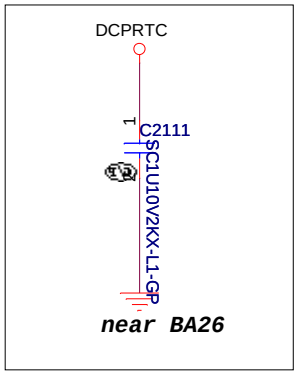
VccRTC
1x1 uF 1x0.1 uF



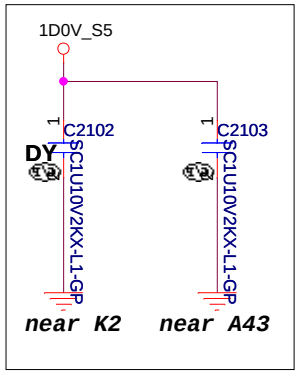
VccRTCPRIM
1x1 uF 1x0.1 uF



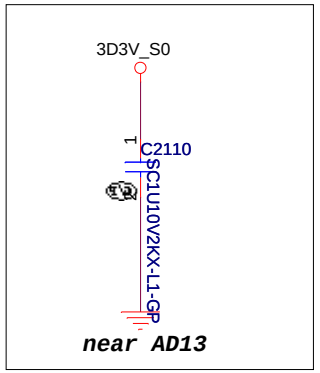
DcpRTC
1x 0.1uF



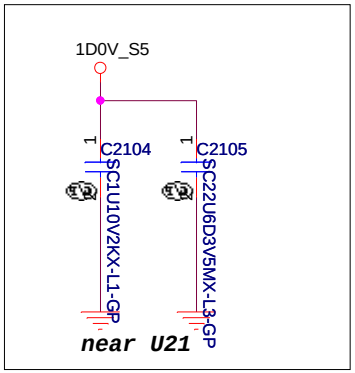
VccMPHYPLL / VccPCIE3PLL
1x1 uF



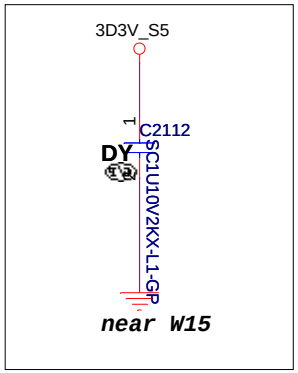
VccATS
1x1 uF



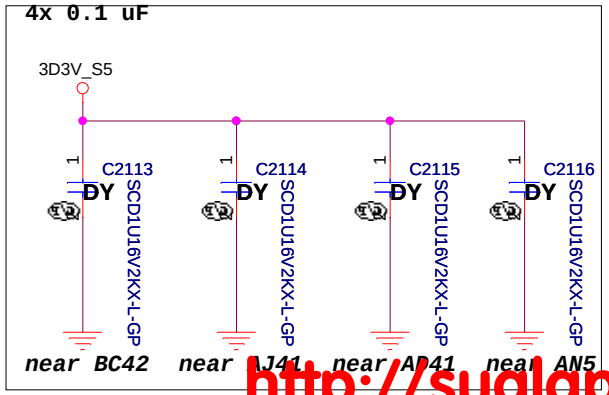
VccMPHY / VccPRIM / VccAPLLEBB
1x1 uF 1x22 uF



VccDSW
1x 1uF



VccPGPPBCH / VccPGPPEF / VccPGPPG
/ VccPRIM
4x 0.1 uF



Decoupling and Power Connection Requirements for SKL S/H PCH (DT / AIO) (Sheet 1 of 2)

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)ecovery / (E)dge	Placement(s) near ball(s)
V1.0A	VccMPHY VccPRIM VccAPLLEBB	U21, U23, U25, U26, V26, AC17, V28	1 uF	0402	1	E (<3 mm)	U21
			22 uF	0805	1	E (<5 mm)	
	VccMPHYPLL VccPCIE3PLL	A43, B43, C44, C45	1 uF	0402	1	E (<5 mm)	A43
	VccCLK5	K2, K3	1 uF	0402	1	E (<5 mm)	K2 (Note 1)
	VccCLK (1,2,3,4,6)	N17, R19, U20, V17, R17	-	-	-	-	-
	VccUSB2PLL VccHDAPLL	AJ5, AL5, AN19	-	-	-	-	-
	VccPRIM	AL20	-	-	-	-	-
	VccPRIM	AD15	-	-	-	-	-
	VccPRIM	AJ20, AJ21, AJ23, AJ25	-	-	-	-	-
	VccPRIM	AA23, AA26, AA28, AC23, AC26, AC28, AE23, AE26, Y23, Y25	-	-	-	-	-
V1.0DSW	DcpDSW	BA29	1 uF	0402	1	E (<5 mm)	BA29
V1.8A/ V3.3A	VccPGPPBCH	BC42, BD40	0.1 uF	0402	1	E (<3 mm)	BC42 (Note 1)
	VccPGPPEF	AJ41, AL41	0.1 uF	0402	1	E (<3 mm)	AJ41 (Note 1)
	VccPGPPG	AD41	0.1 uF	0402	1	E (<3 mm)	AD41 (Note 1)
	VccPRIM	AN5	0.1 uF	0402	1	E (<3 mm)	AN5 (Note 1)
	VccPGPPA	BA31	-	-	-	-	-
	VccSPI	BE41, BE42, BE43	-	-	-	-	-
	VccGPPD	BC44, BA45, BC45, BB45	-	-	-	-	-
V1.8A/ V1.85/ V3.3S	VccATS	AD13	1 uF	0402	1	E (<5 mm)	AD13
V1.5A/ V1.8A/ V3.3A	VccHDA	BA15	-	-	-	-	-
V3.3A	VccRTCPRIM	BA20	1 uF	0402	1	E (<5 mm)	BA20
			0.1 uF	0402	1	E (<3 mm)	
	VccPRIM	BD3, BE3, BE4	-	-	-	-	-
V3.3RTC	VccRTC	BA22	1 uF	0402	1	E (<5 mm)	BA22
			0.1 uF	0402	1	E (<3 mm)	
V3.3DSW	VccDSW	W15	1 uF	0401	1	E (<3 mm)	W15 (Note 1)
	VccDSW	BA24	-	-	-	-	-
PCH Internal VRM	DcpRTC	BA26	0.1 uF	0402	1	E (<5 mm)	BA26

<Core Design>

緯創資通 **Wistron Corporation**
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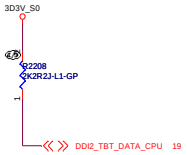
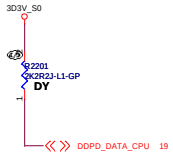
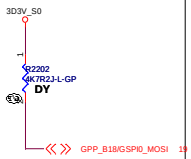
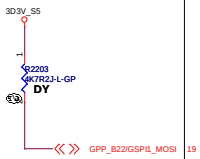
Taipei Hsien 221, Taiwan, R.O.C.

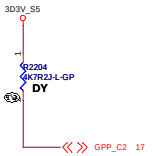
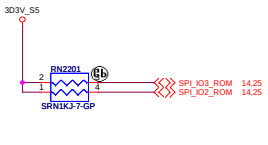
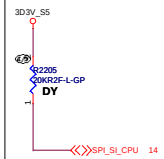
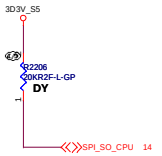
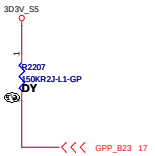
Title: **PCH_POWER_CAP1**

Size: A4 | Document Number: **Rayleigh_SLS** | Rev: **SA**

Date: Wednesday, August 12, 2015 | Sheet 21 of 105

SSID = PCH

Description	Display Port B Detected	Display Port C Detected	Display Port D Detected	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	ESPI FLASH SHARING MODE
GPIO	GPP_I6	GPP_I8	GPP_I10	GPP_B18	GPP_B22	HDA_SDO	GPP_H12
Schematic	Pull up at p.71 RN7101						
High	Detected	Detected	Detected	Enable	LPC	Disable	1:SLAVE ATTACEHD FLASH SHARING ESPI FLASH SHARING MODE
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	0: MASTER ATTACHED FLASH SHARING
	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	eSPI or LPC	TLS Confi-dentiality	Reserved	Reserved	Reserved	Reserved	Reserved
GPIO	GPP_B14	GPP_C5	GPP_C2	SPI0_IO3	SPI0_IO2	SPI0_MOSI	SPI0_MISO	GPP_B23 / PCHHOT#
Schematic				 JJ 20150212				
High	Enable	eSPI	Enable					
Low	Disable	LPC	Disable					
	internal pull-down	internal pull-down	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-down

[H,S,U,Y] Pull-up Resistors on SPI_IO2 and SPI_IO3 Requirement Update

The current Skylake Platform Design Guide (PDG) states that a 1 K pull-up resistor is required on the PCH SPI_IO2 and SPI_IO3 signals.

This 1K pull up resistor is no longer needed on Skylake platforms and can be removed from the motherboard. The new guidelines will be updated in a future release of the Skylake PDG

<Core Design>

緯創資通 Wistron Corporation
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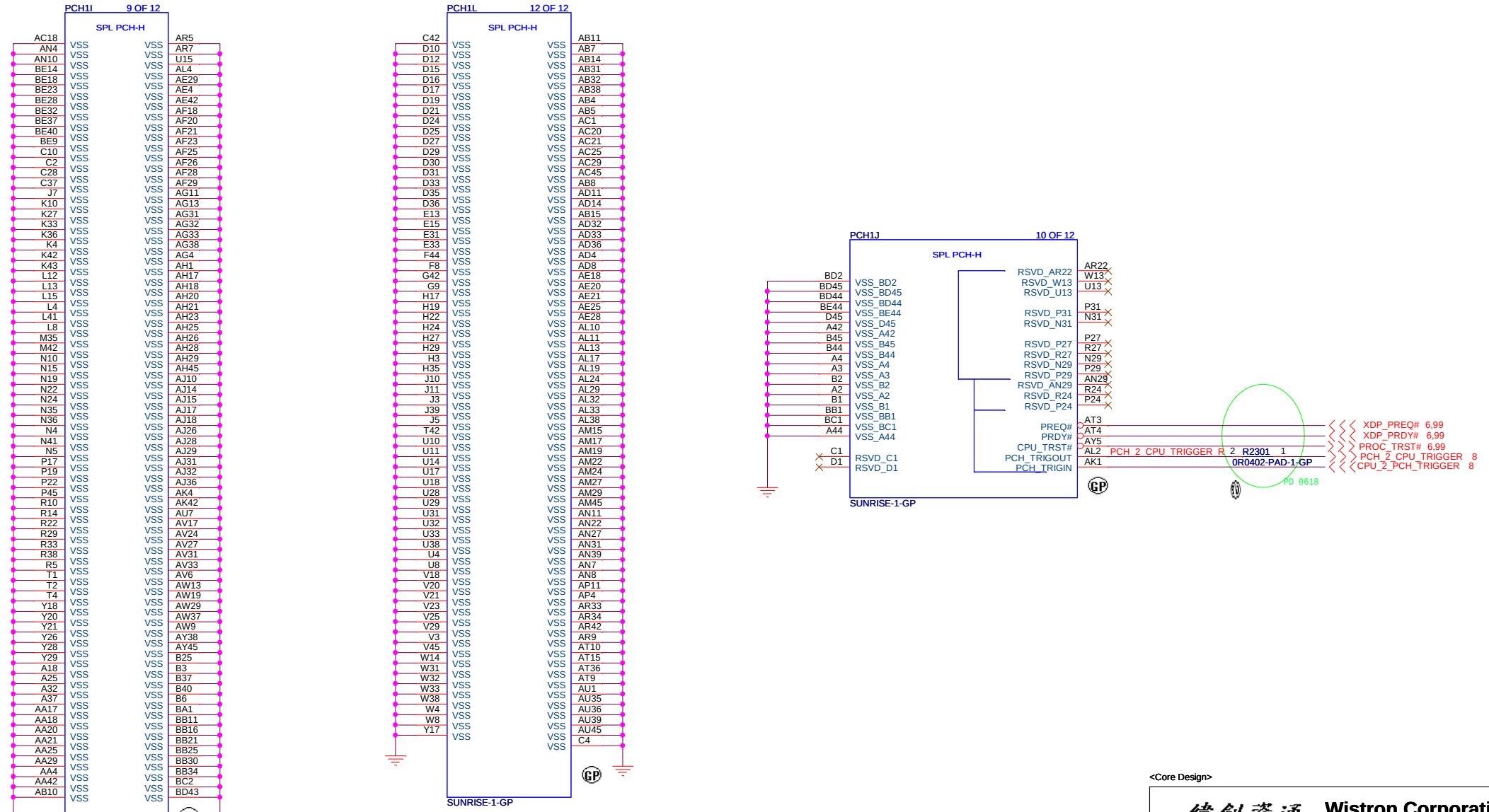
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_STRAP

Size: A2 | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 22 of 105

SSID = PCH



<Core Design>

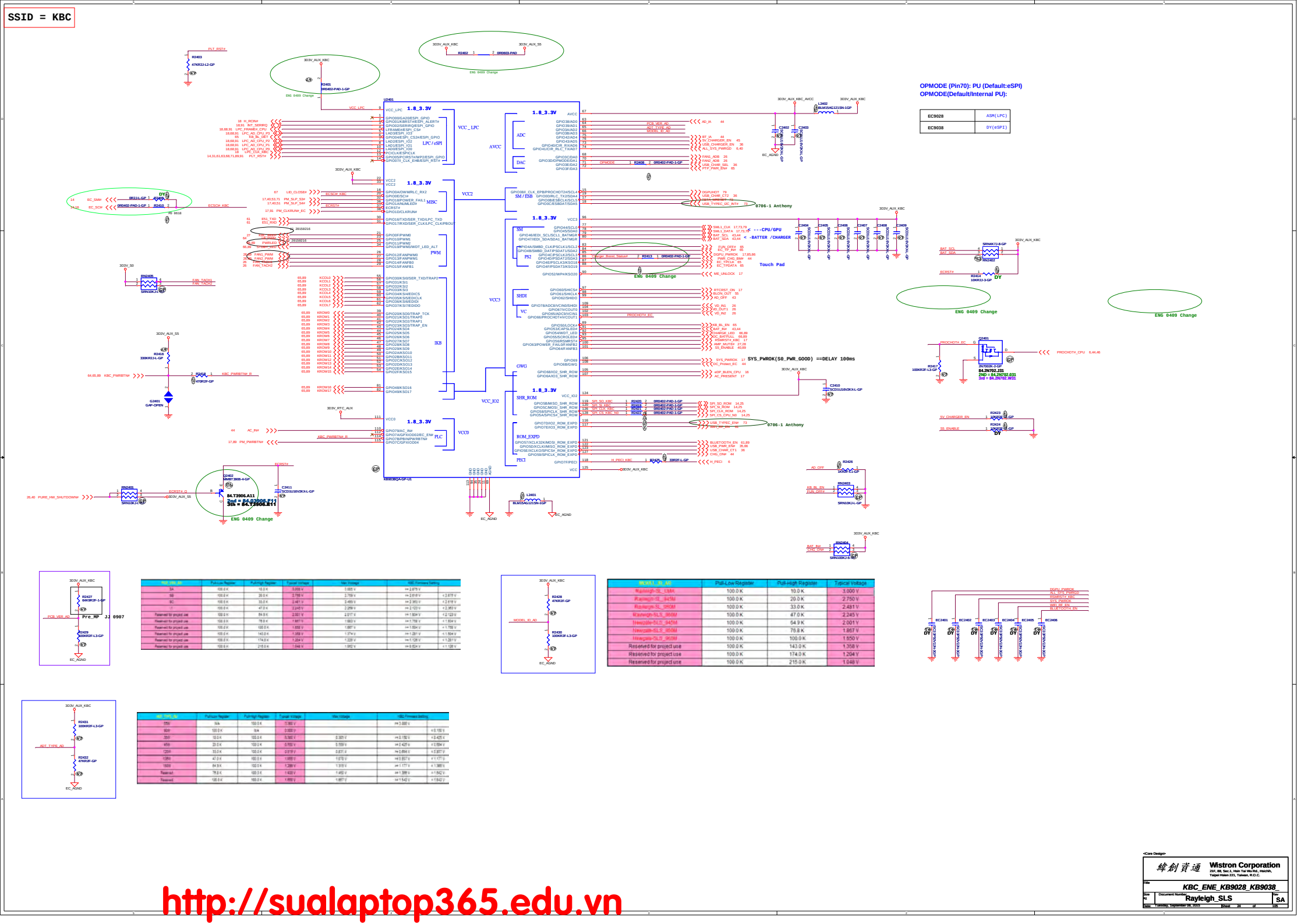
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_RSVD_VSS

Size: B | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 23 of 105

SSID = KBC



EC9028	ASM(LPC)
EC9038	DY(eSPI)

PCB_VER_ID	Pull-Low Register	Pull-High Register	Typical Voltage
Rayleigh-SLS_EMM	100.0 K	10.0 K	3.000 V
Rayleigh-SLS_84M	100.0 K	20.0 K	2.750 V
Rayleigh-SLS_DRDM	100.0 K	33.0 K	2.481 V
Rayleigh-SLS_86DM	100.0 K	47.0 K	2.245 V
Newton-SLS_84MM	100.0 K	54.9 K	2.001 V
Newton-SLS_86DM	100.0 K	76.8 K	1.867 V
Newton-SLS_86DM	100.0 K	100.0 K	1.550 V
Reserved for project use	100.0 K	143.0 K	1.368 V
Reserved for project use	100.0 K	174.0 K	1.204 V
Reserved for project use	100.0 K	215.0 K	1.048 V

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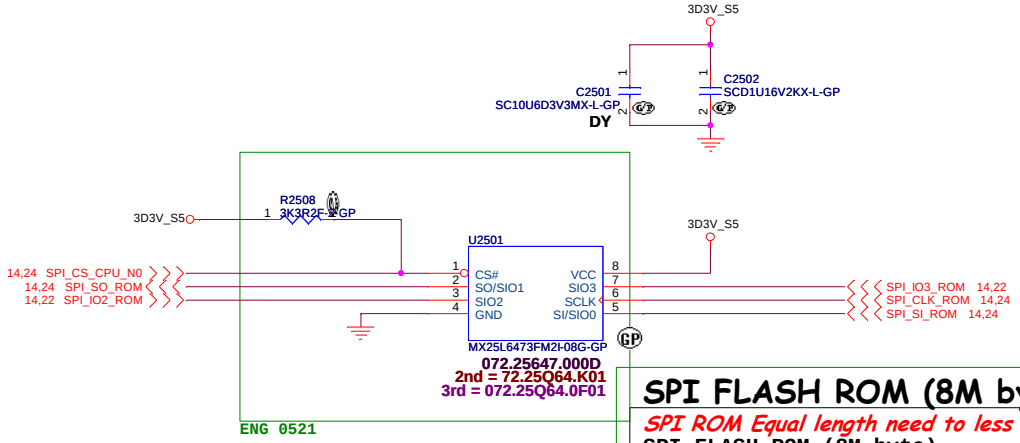
KBC_ENE_KB9028_KB9038_
Rayleigh_SLS
SA
Tuesday, September 08, 2015

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH



SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

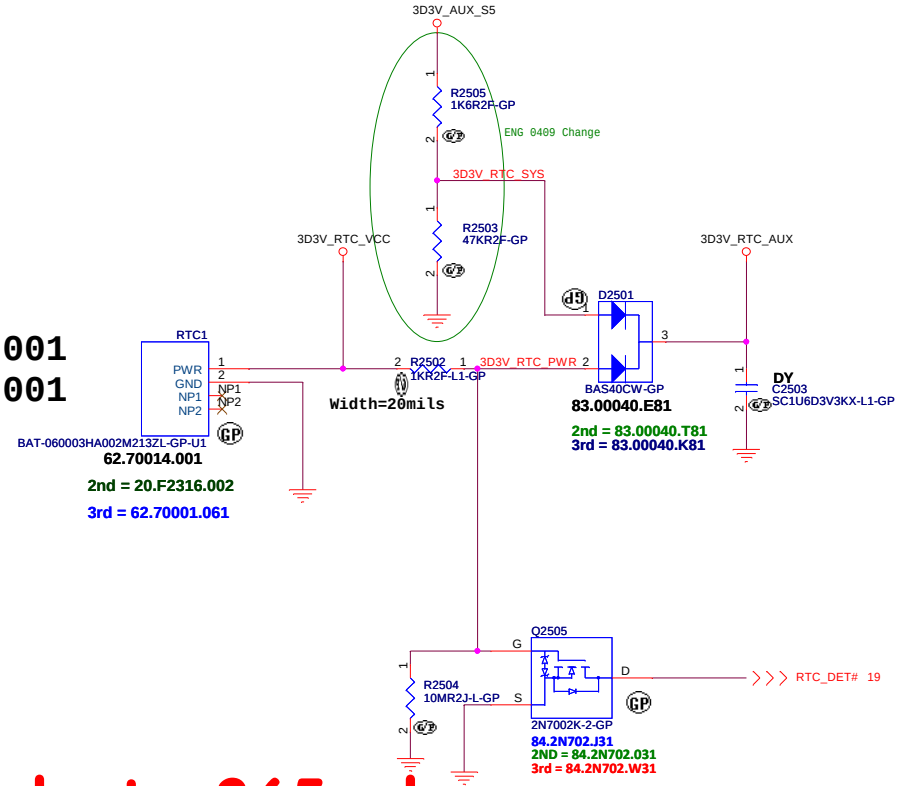
SPI FLASH ROM (8M byte)

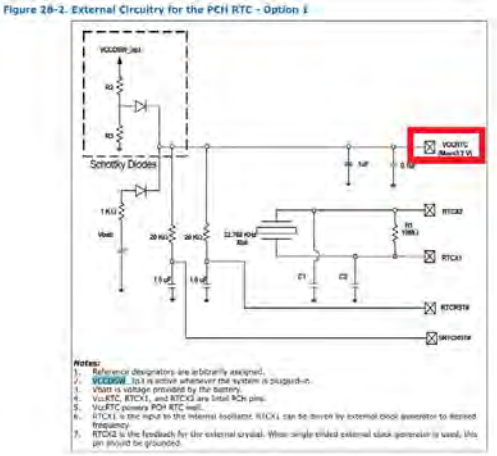
1st= 072.25647.000D (MXIC MX25L6473FM2I-08G)
2nd= 72.25Q64.K01 (WINBOND W25Q64FVSSIQ)
3th= 072.25Q64.0F01 (MICRON N25Q064A13ESED0F)

ENG 0416

Main Func = RTC

RTC BATTERY
1st= 23.22065.001
2nd= 23.20068.001





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash(KBC+PCH)/RTC

Size: A3 | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 25 of 105

SSID = Thermal

Layout 15 mil

Layout 15 mil

ADB (Active Dusting Blower) function

AFTP TESTPOINT

FAN_TACH1_C 89
FAN_TACH2_C 89

FOR CPU T8

FOR SYSTEM

T8 = 85 degree

EMI Reserved

ENG 0413 Change

ENG 0410 Change

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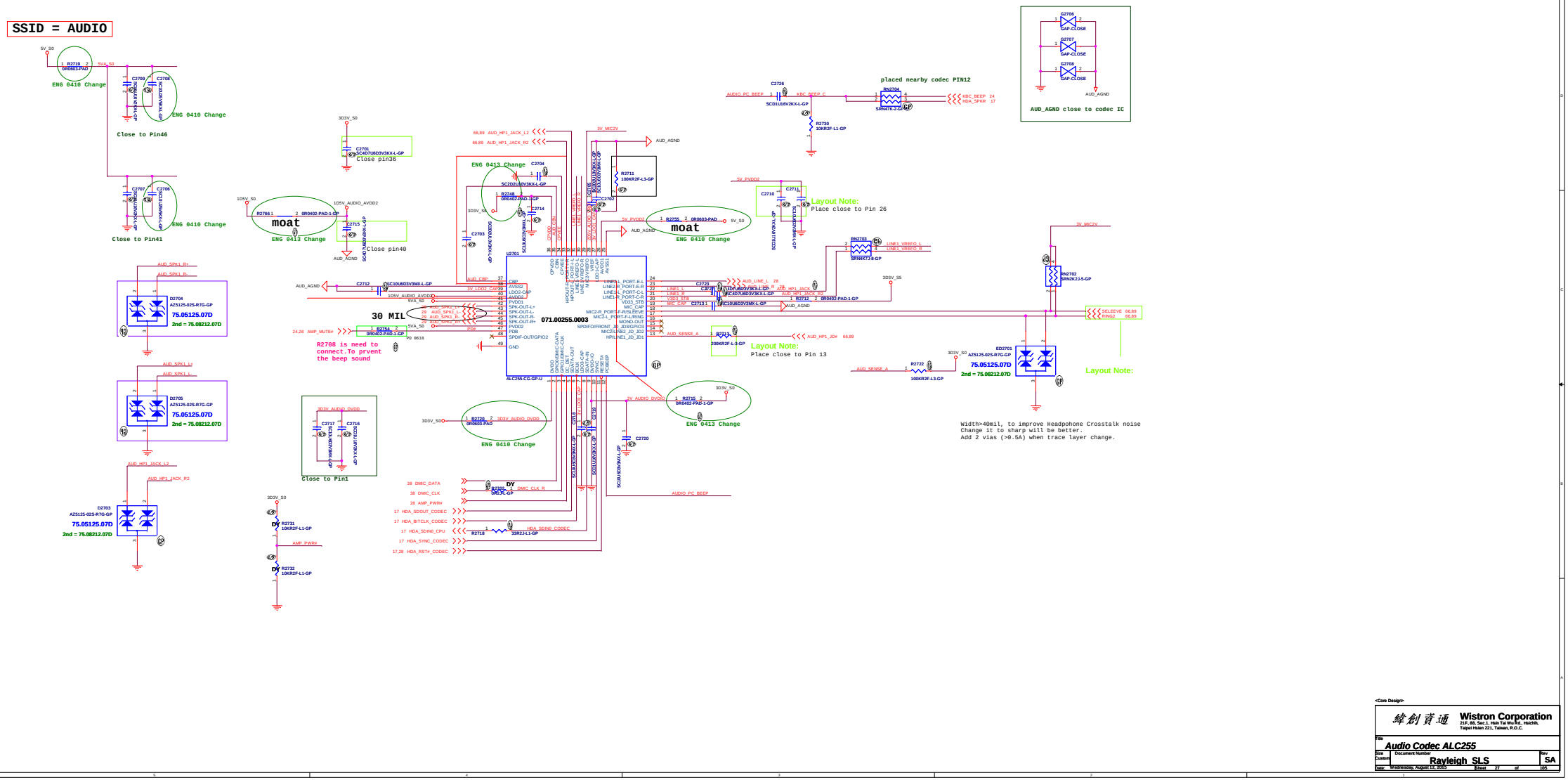
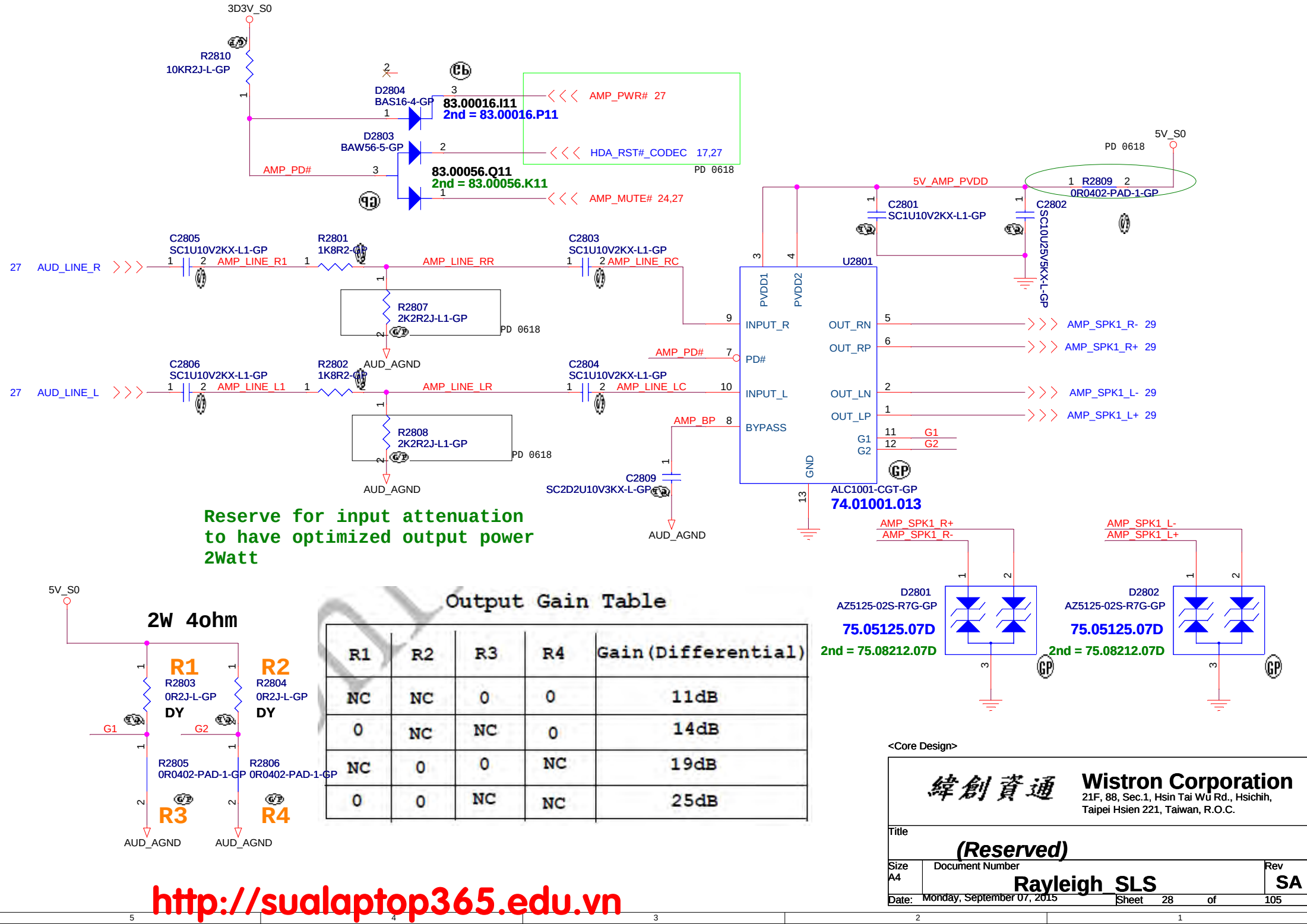
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal T8 and FAN
Size: Custom | Document Number: Rayleigh_SLS | Rev: SA
Date: Wednesday, August 12, 2015 | Sheet 26 of 105





Output Gain Table

R1	R2	R3	R4	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

<Core Design>

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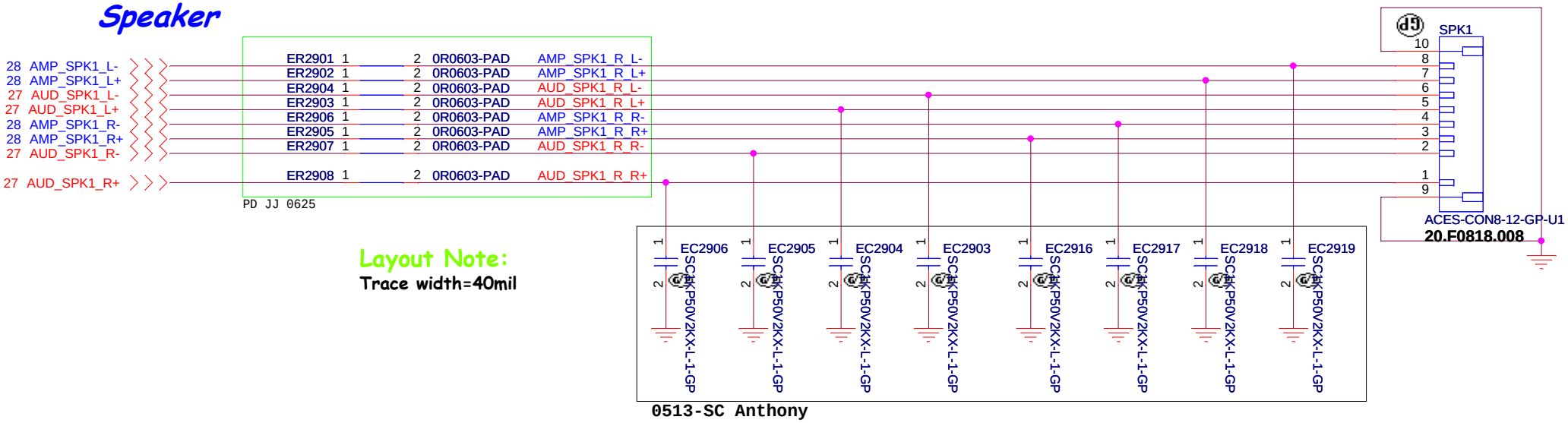
Title: (Reserved)

Size: A4 | Document Number: Rayleigh_SLS | Rev: SA

Date: Monday, September 07, 2015 | Sheet 28 of 105

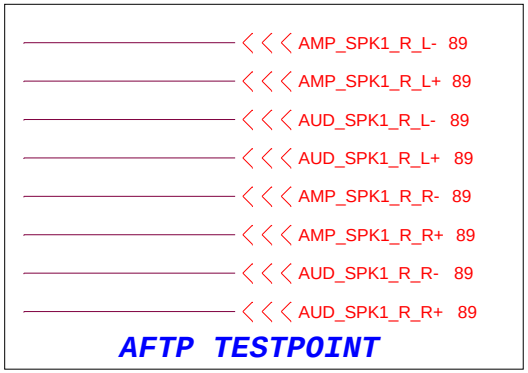
SSID = AUDIO

Speaker



Layout Note:
Trace width=40mil

0513-SC Anthony



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Speaker/ALC255***
Size: A4	Document Number: **Rayleigh_SLS**
Rev: SA	
Date: Wednesday, August 12, 2015	Sheet 29 of 105

<Core Design>

緯創資通

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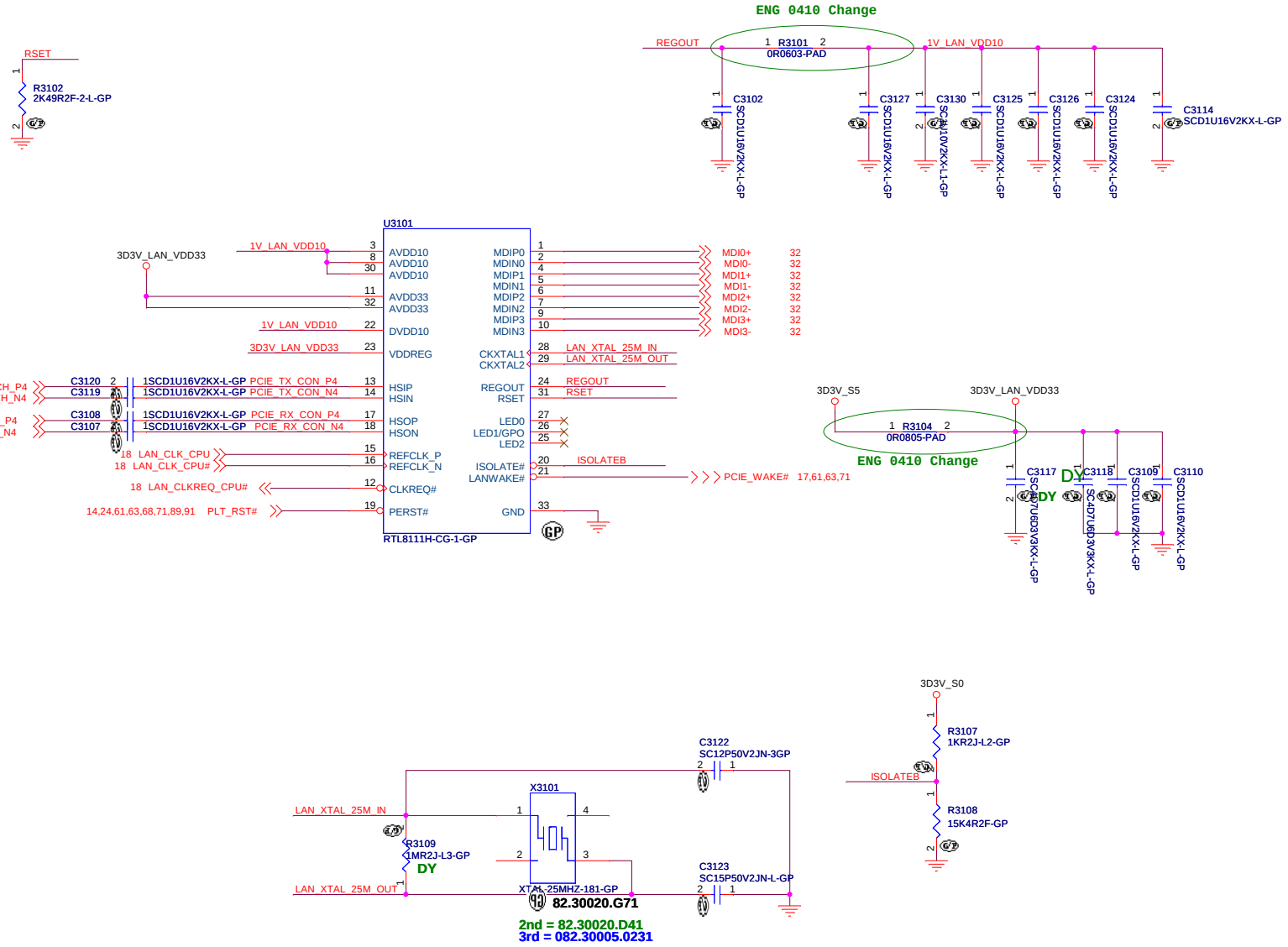
Title

(Reserved)

Size	Document Number	Rev
A	Rayleigh_SLS	SA

Date: Wednesday, August 12, 2015 Sheet 30 of 105



<Core Design>

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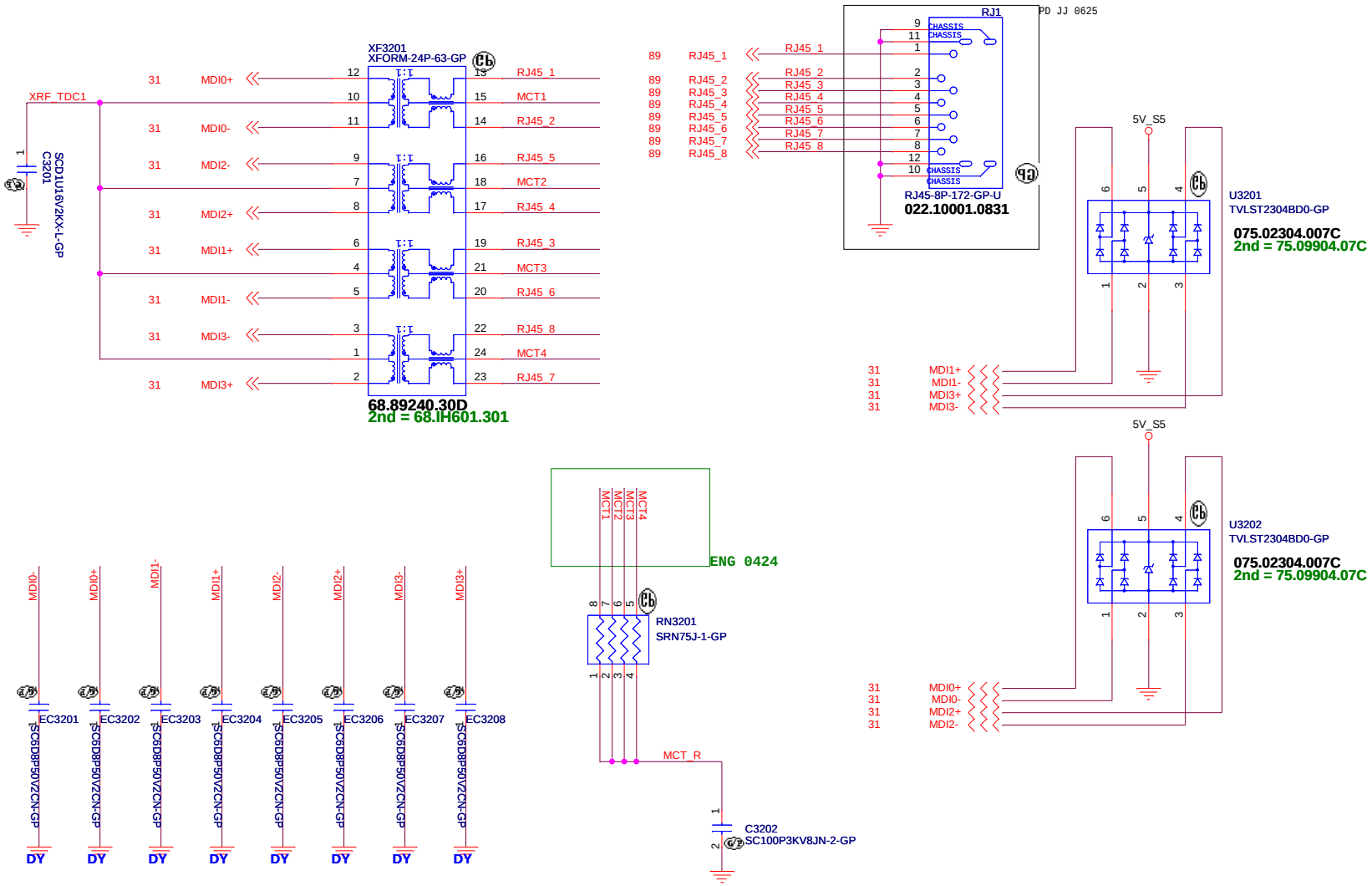
Title: ***LAN(RTL8111)***

Size	Document Number	Rev
A3	Rayleigh SLS	SA

Date: Tuesday, September 08, 2015 Sheet 31 of 105

SSID = LAN



<Core Design>

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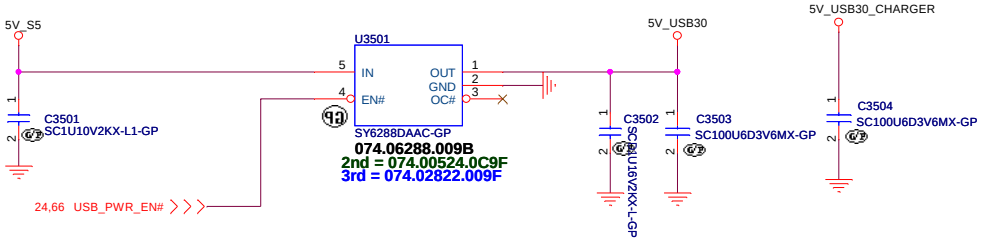
Title: *RJ45+Transformer*		
Size: B	Document Number: Rayleigh_SLS	Rev: SA
Date: Wednesday, August 12, 2015	Sheet 32 of 105	

Low Active 2A



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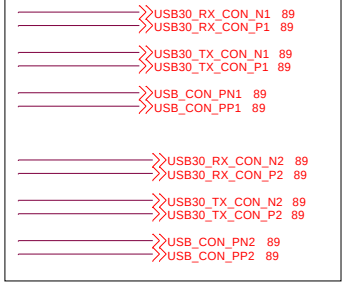
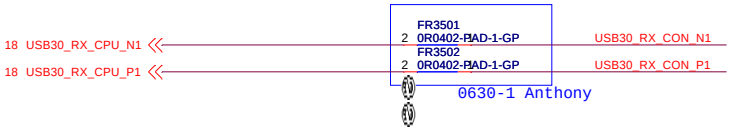
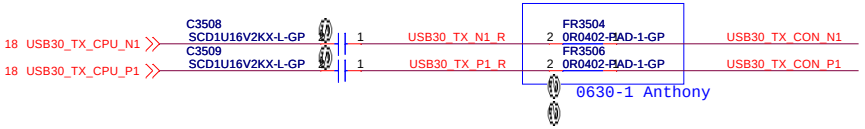
AFTP TESTPOINT

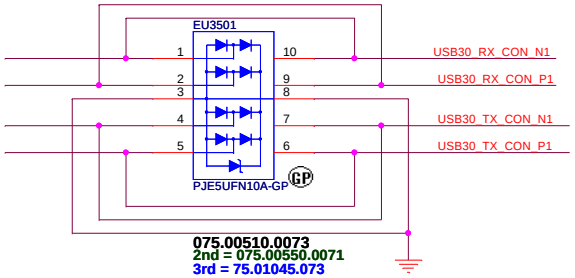


USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	







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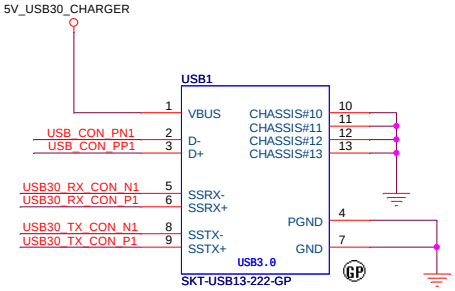

SKT-USB13-222-GP
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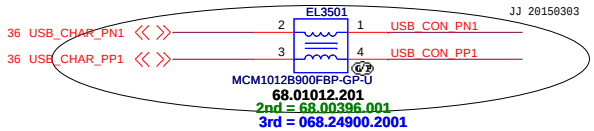

JJ 20150303

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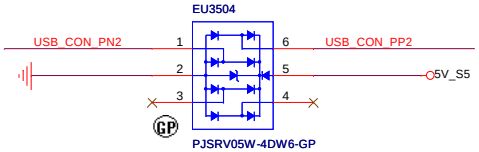

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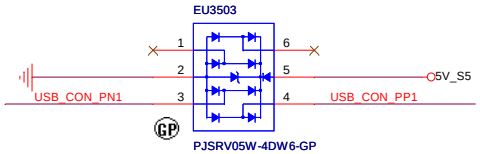

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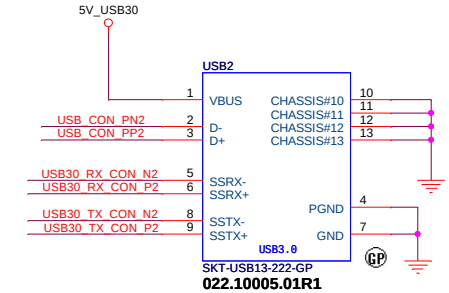

SKT-USB13-222-GP
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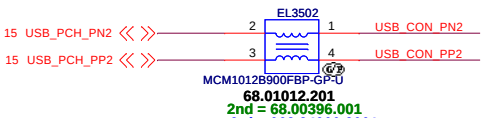

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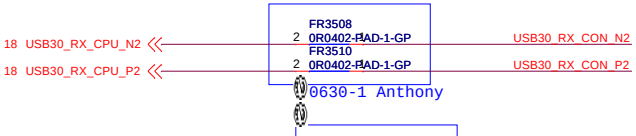

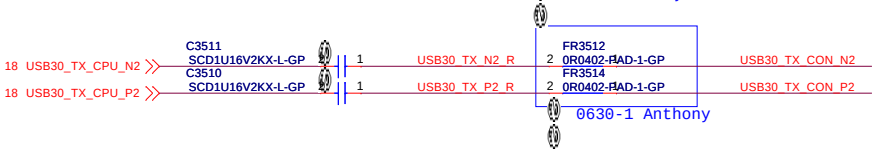

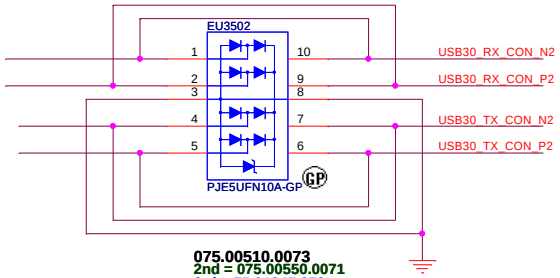

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<Core Design>

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Title: USB3.0 CONN

Size: A3 | Document Number: Rayleigh_SLS | Rev: SA

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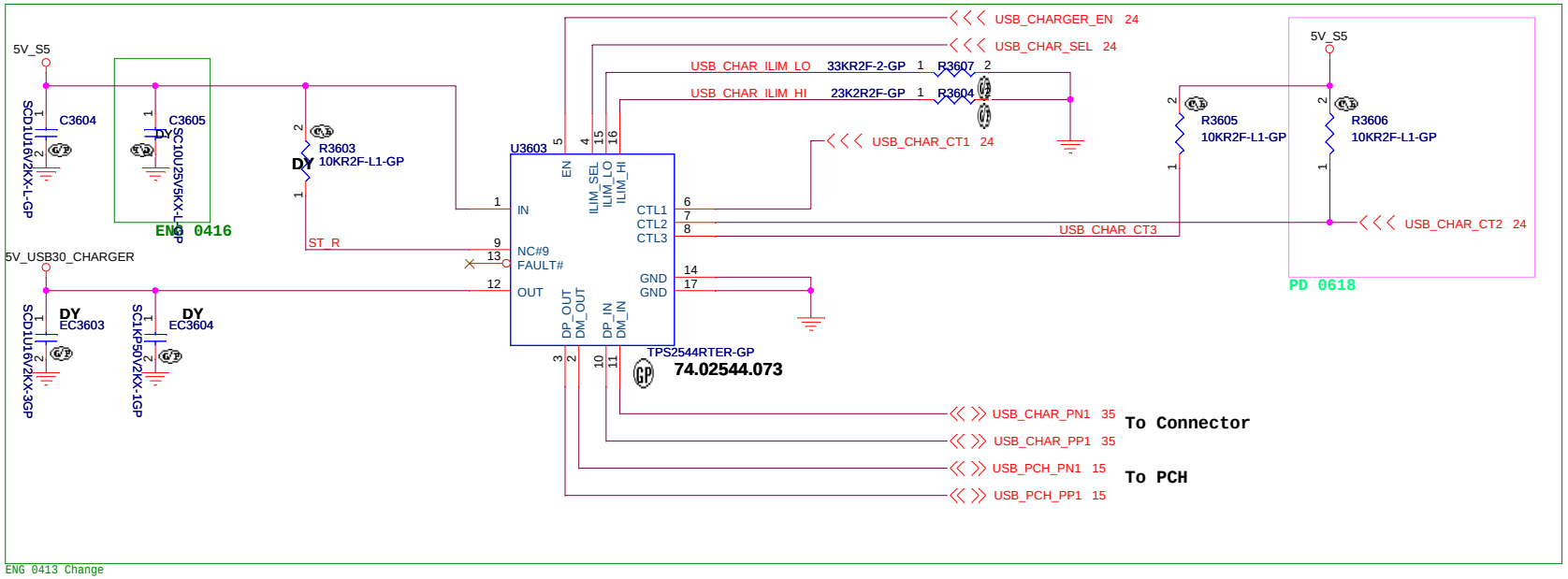

ENG 0413 Change

Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_ SEL	MODE	Current Limit Setting	Status Output	Notice
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	0	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_LO	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device forced to stay in DCP BC1.2
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	Charging mode
1	0	1	0	DCP/Divider1	ILIM_LO	OFF	Device forced to stay in DCP divider1
1	0	1	1	DCP/Divider1	ILIM_HI	OFF	Charging mode
1	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
1	1	0	1	SDP1	ILIM_HI	OFF	
1	1	1	0	SDP2	ILIM_LO	OFF	
1	1	1	1	CDP	ILIM_HI	CDP	Data lines disconnected Load Detect function active

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Title: ***USB CHARGER***

Size: B | Document Number: **Rayleigh_SLS** | Rev: SA

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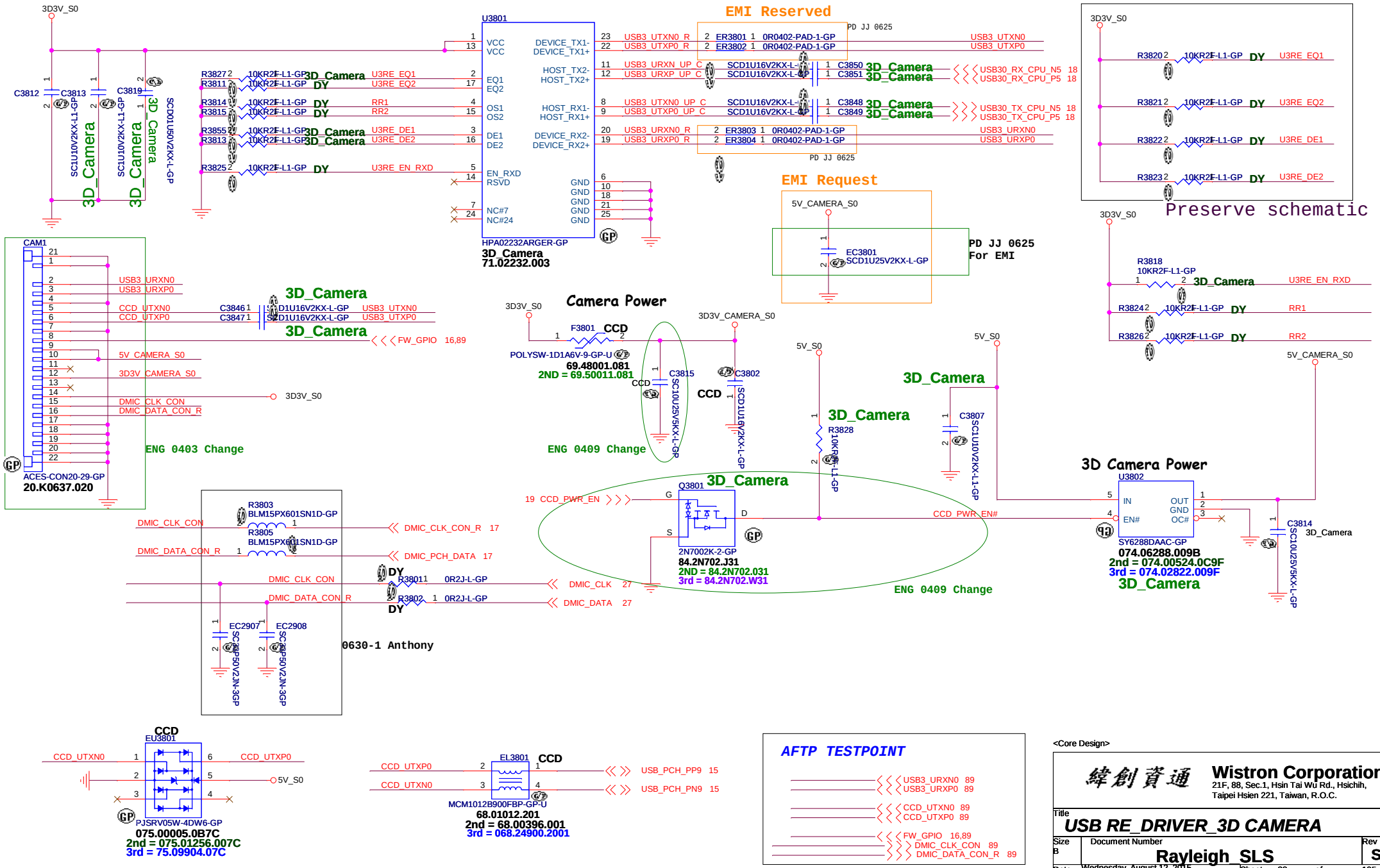

<Core Design>

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Title: USB RE_DRIVER_3D CAMERA

Size: B | Document Number: Rayleigh_SLS | Rev: SA

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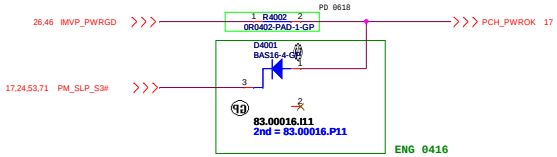
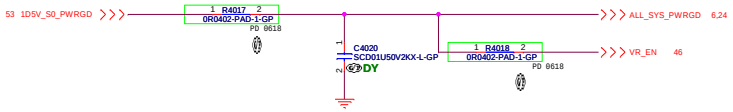
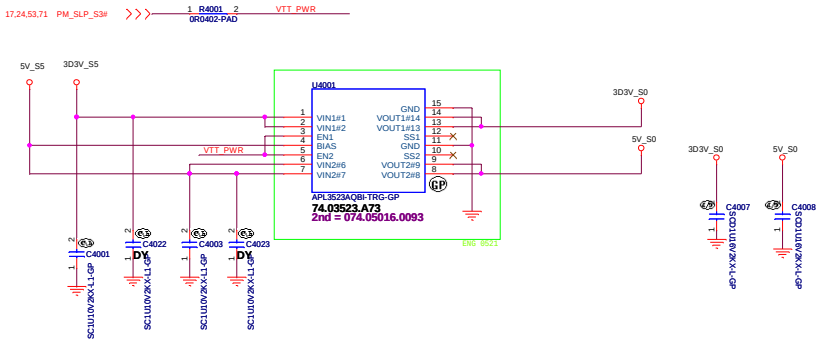
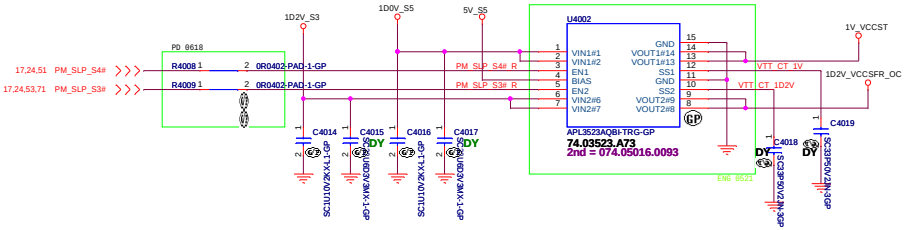
Power Sequence



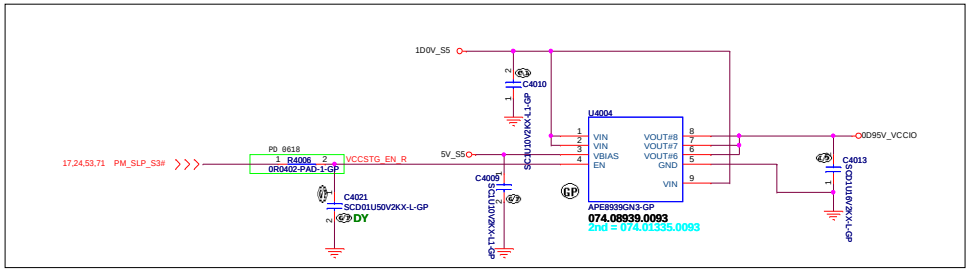


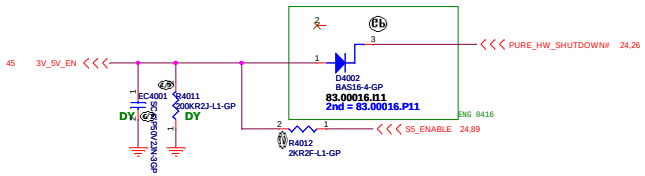
ANNIE Run Power





JJ 20150305





<Core Design>
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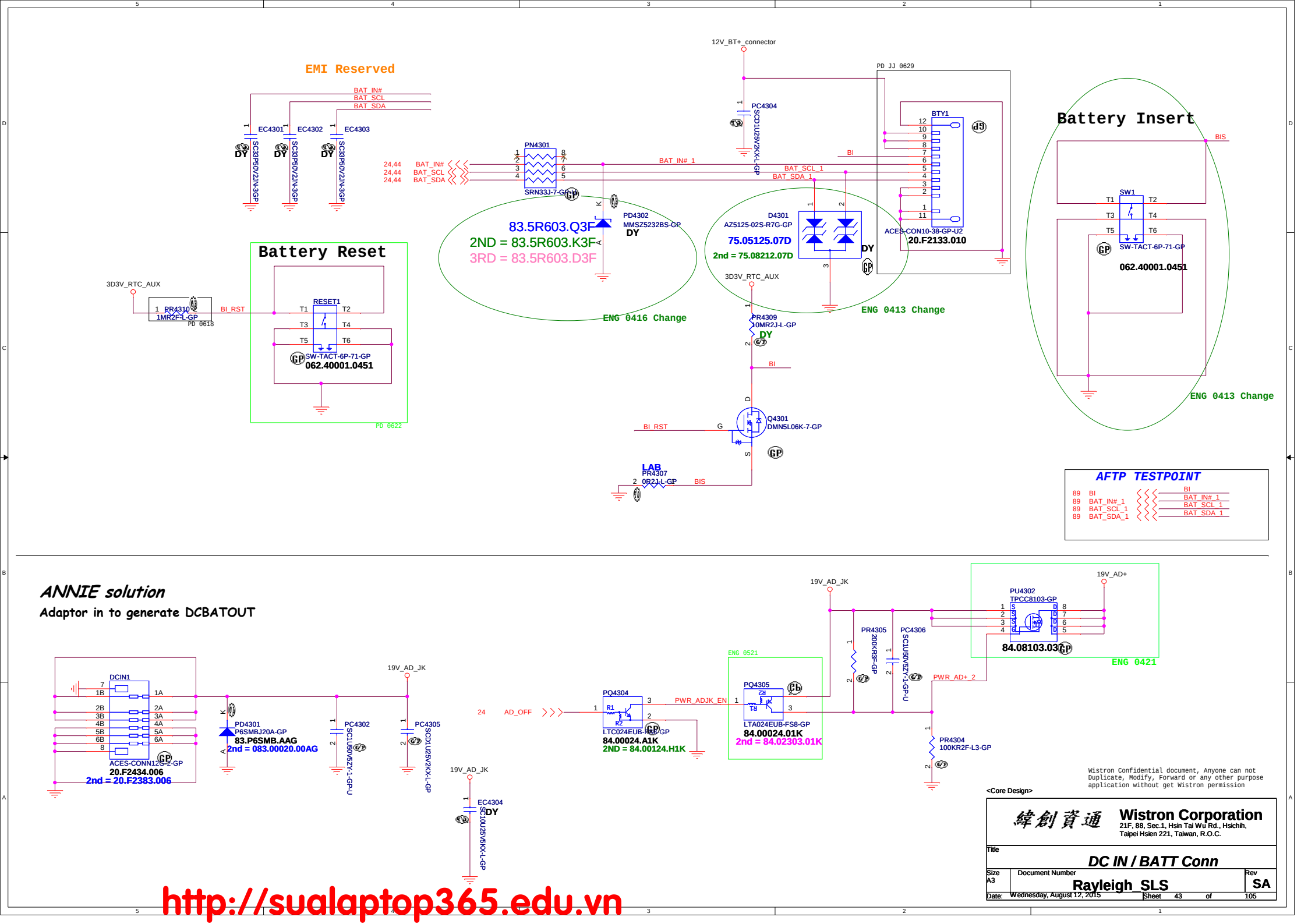
Title: **Power Plane Enable & SEQUENCE**

Size: A2 | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 40 of 106



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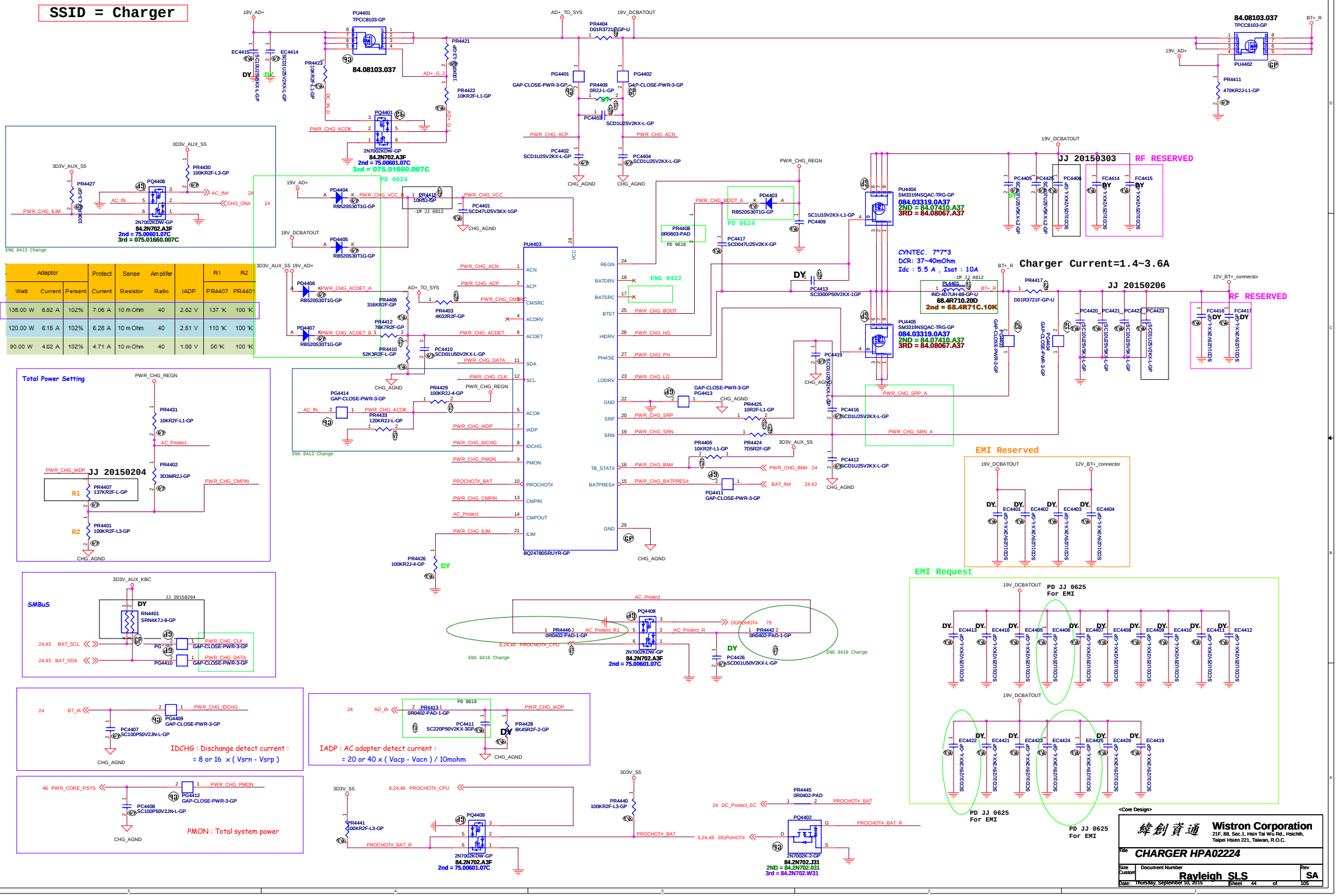

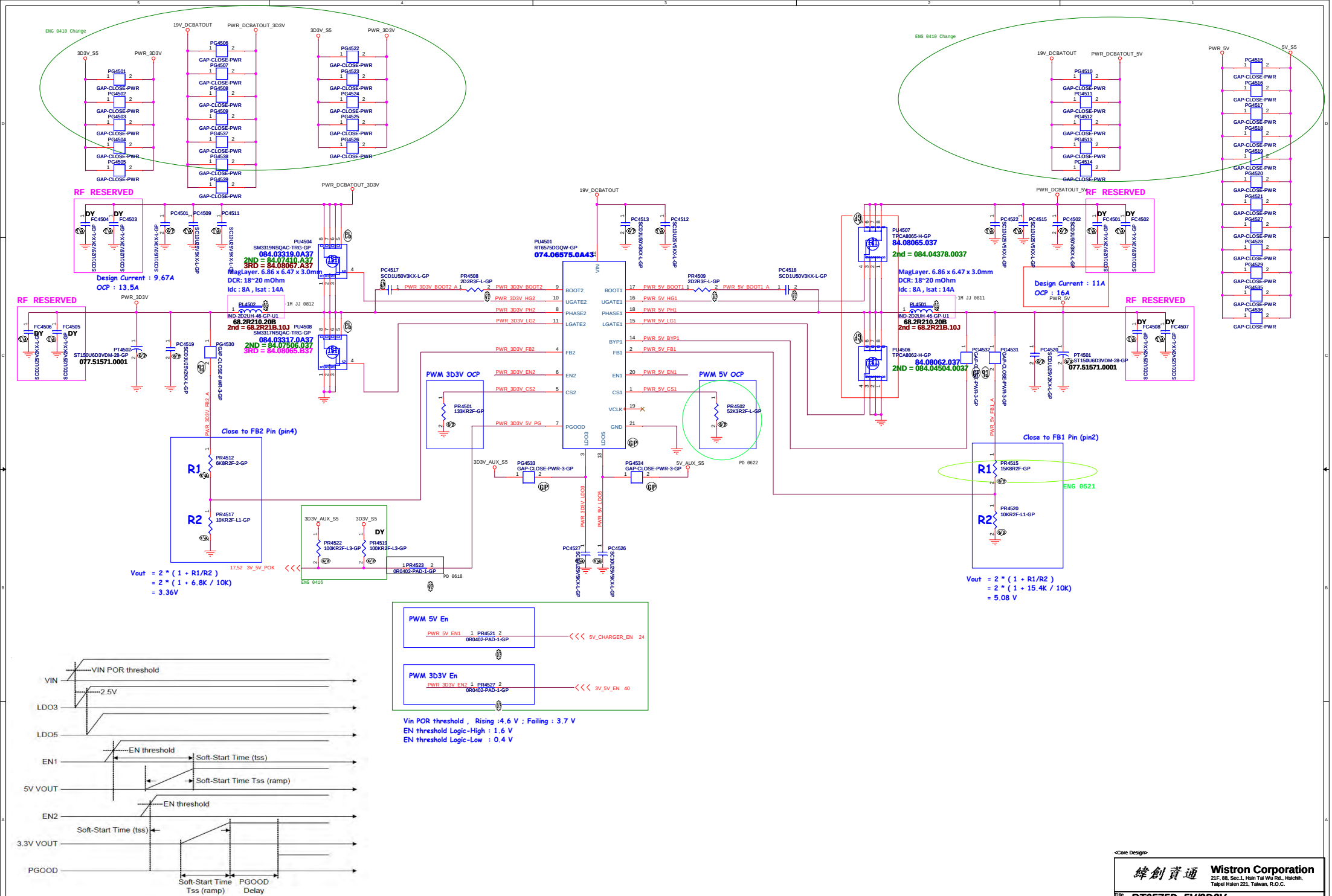

Figure 6. RT6575B Timing

<Core Design>
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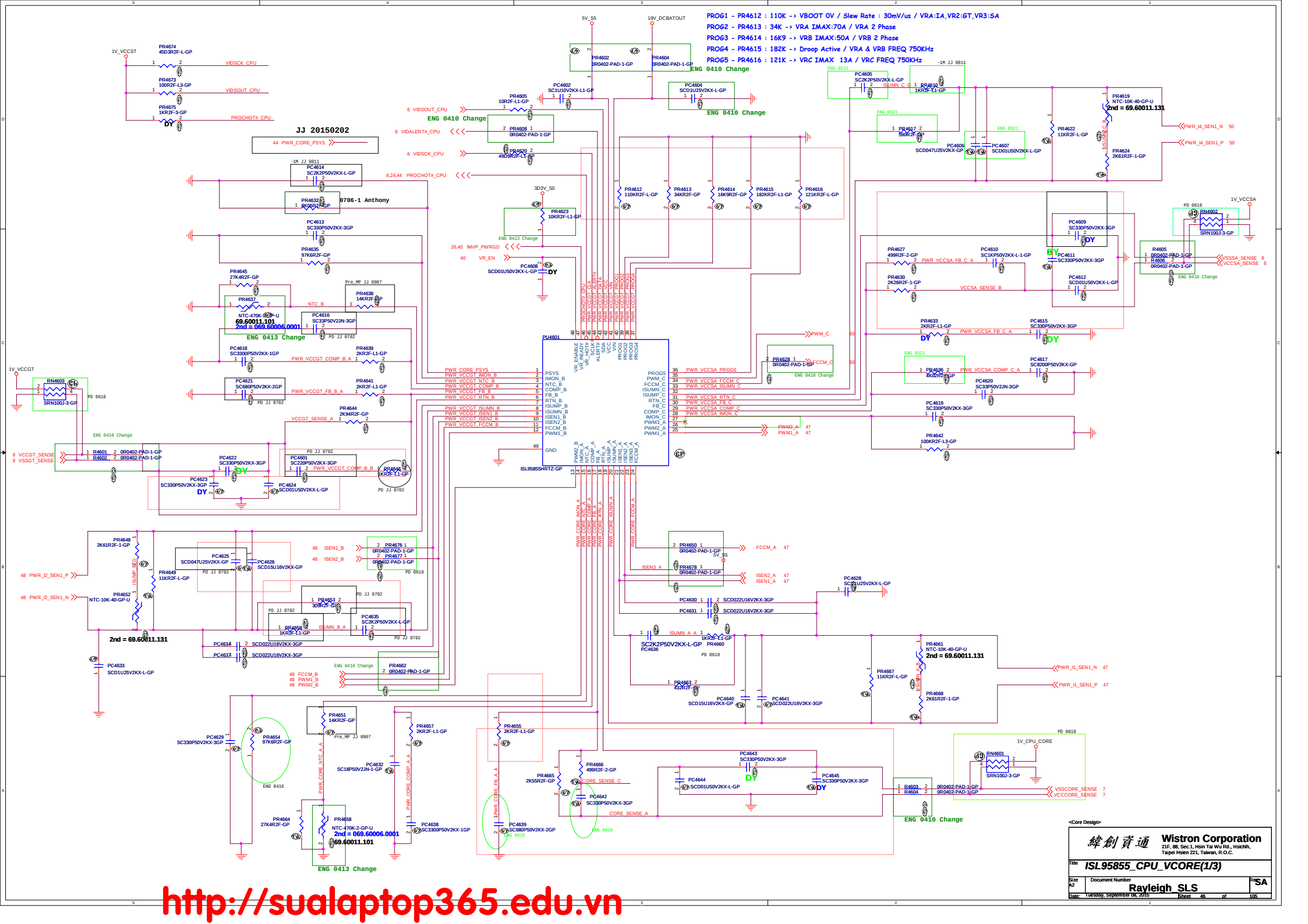
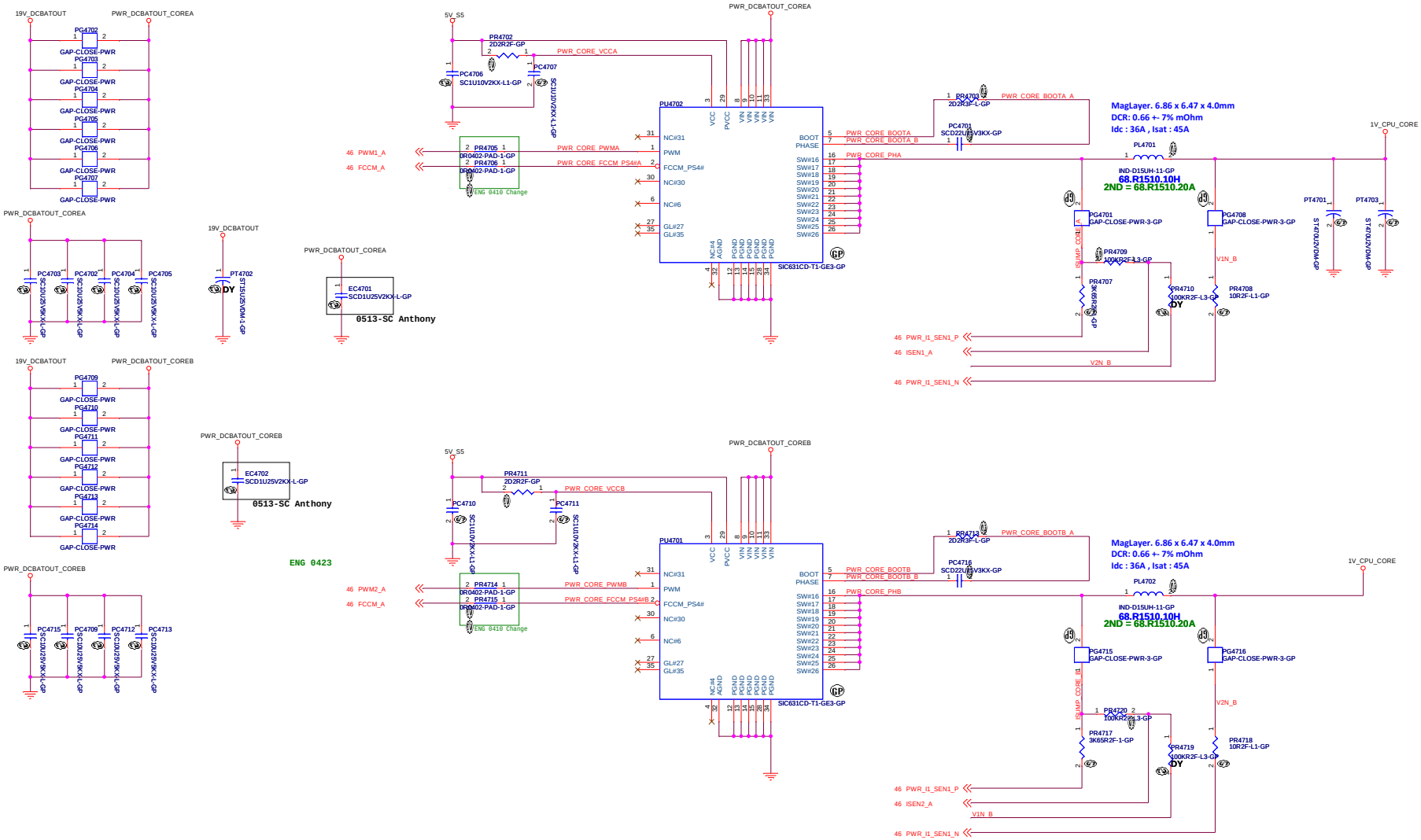
Title	RT6575D_5V/3D3V	
Size A2	Document Number Rayleigh_SLS	Rev SA
Date: Monday, August 17, 2015	Sheet 45 of 105	


PROG1 - PR4612 : 110K -> VBOOT 0V / Slew Rate : 30mV/us / VRA:IA,VR2:GT,VR3:SA
PROG2 - PR4613 : 34K -> VRA IMAX:70A / VRA 2 Phase
PROG3 - PR4614 : 16K9 -> VRB IMAX:50A / VRB 2 Phase
PROG4 - PR4615 : 182K -> Droop Active / VRA & VRB FREQ 750KHz
PROG5 - PR4616 : 121K -> VRC IMAX 13A / VRC FREQ 750KHz
JJ 20150202
ISL95855HRTZ-GP
PU4601
ENG 0410 Change
ENG 0413 Change
ENG 0416
ENG 0521
0706-1 Anthony
2nd = 69.60011.131
2nd = 069.60006.0001
69.60011.101
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL95855_CPU_VCORE(1/3)
Rayleigh_SLS
Tuesday, September 08, 2015
http://sualaptop365.edu.vn



<Core Design>

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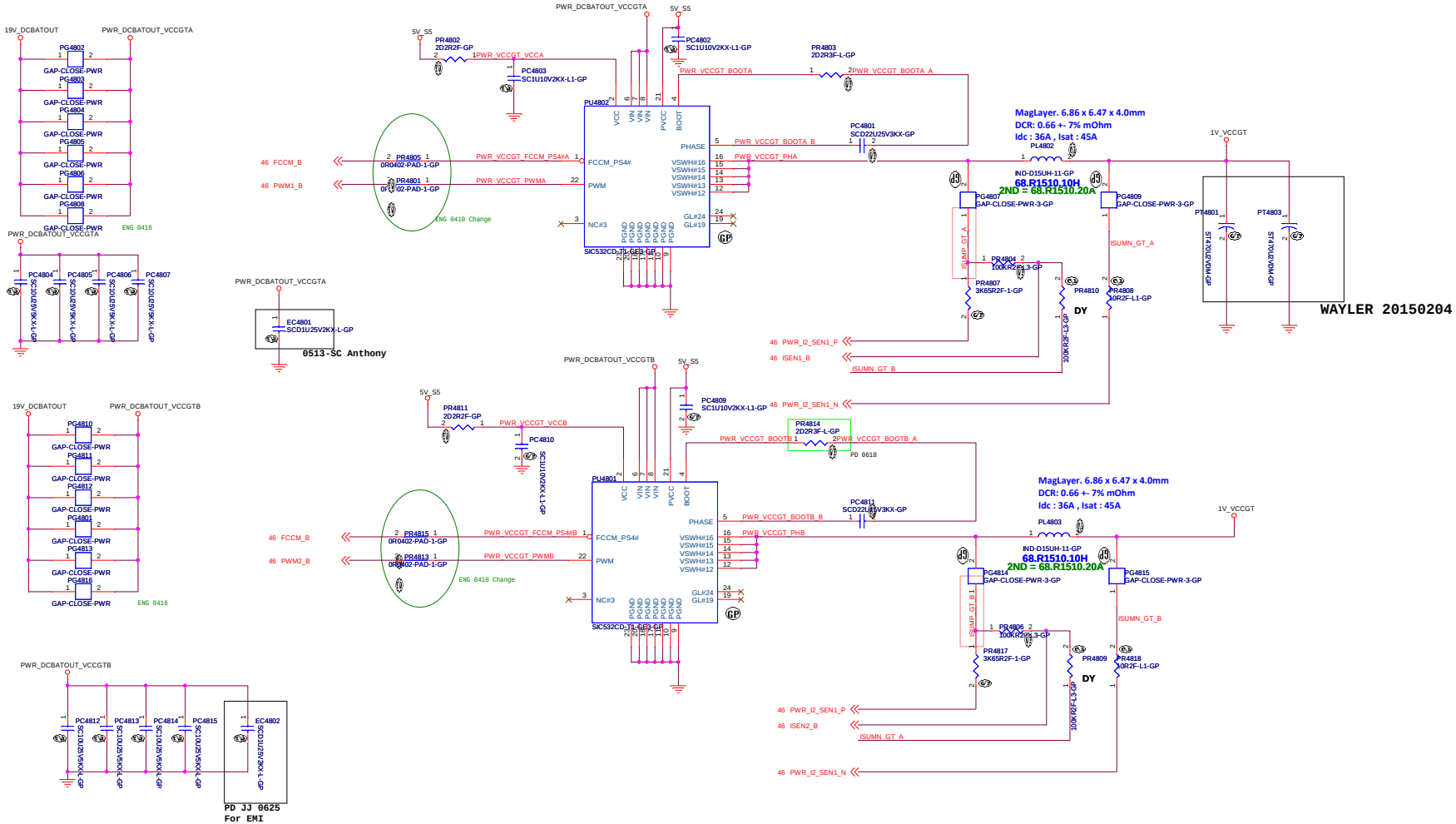
Taipei Hsien 221, Taiwan, R.O.C.

Title: SIC631CD_CPU_VCORE(2/3)

Size: A2 | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 47 of 105



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緯創資通 Wistron Corporation
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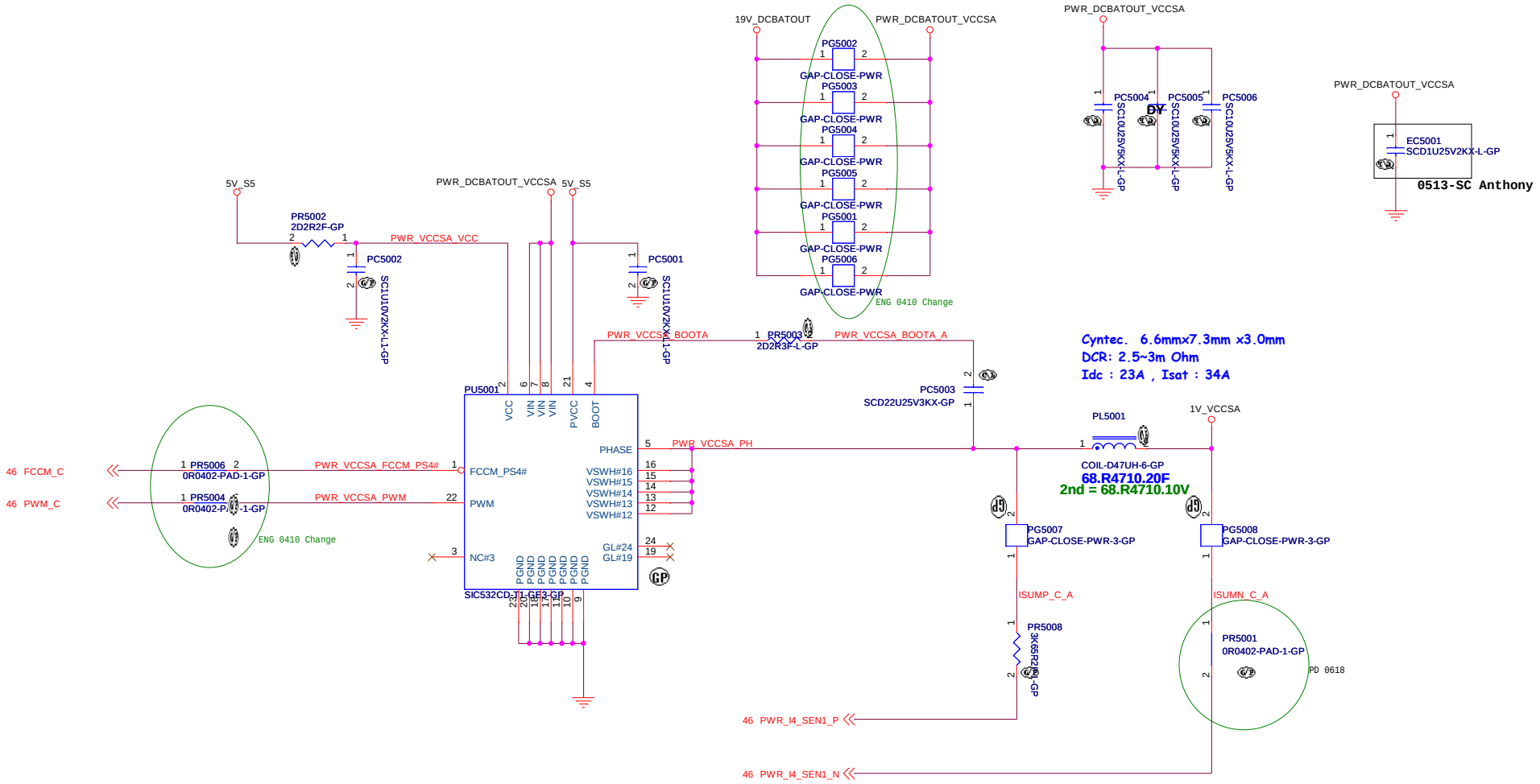
Taipei Hsien 221, Taiwan, R.O.C.

Title: SIC631CD_CPU_VCCGT(2/3)
Size: A2 | Document Number: Rayleigh_SLS | Rev: SA
Date: Wednesday, August 12, 2015 | Sheet 48 of 105



<Core Design>

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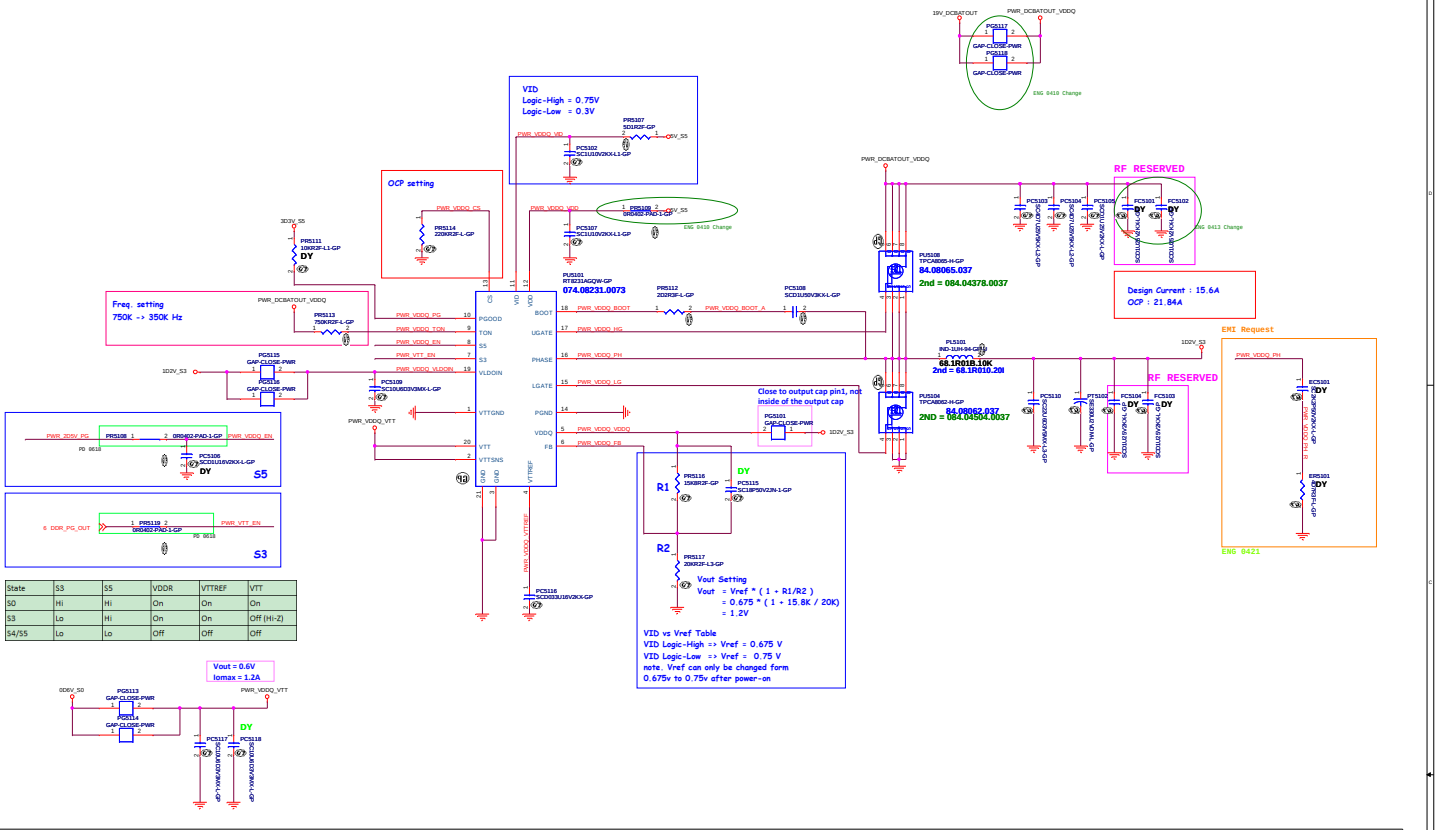
Title: SIC631CD_VCCSA

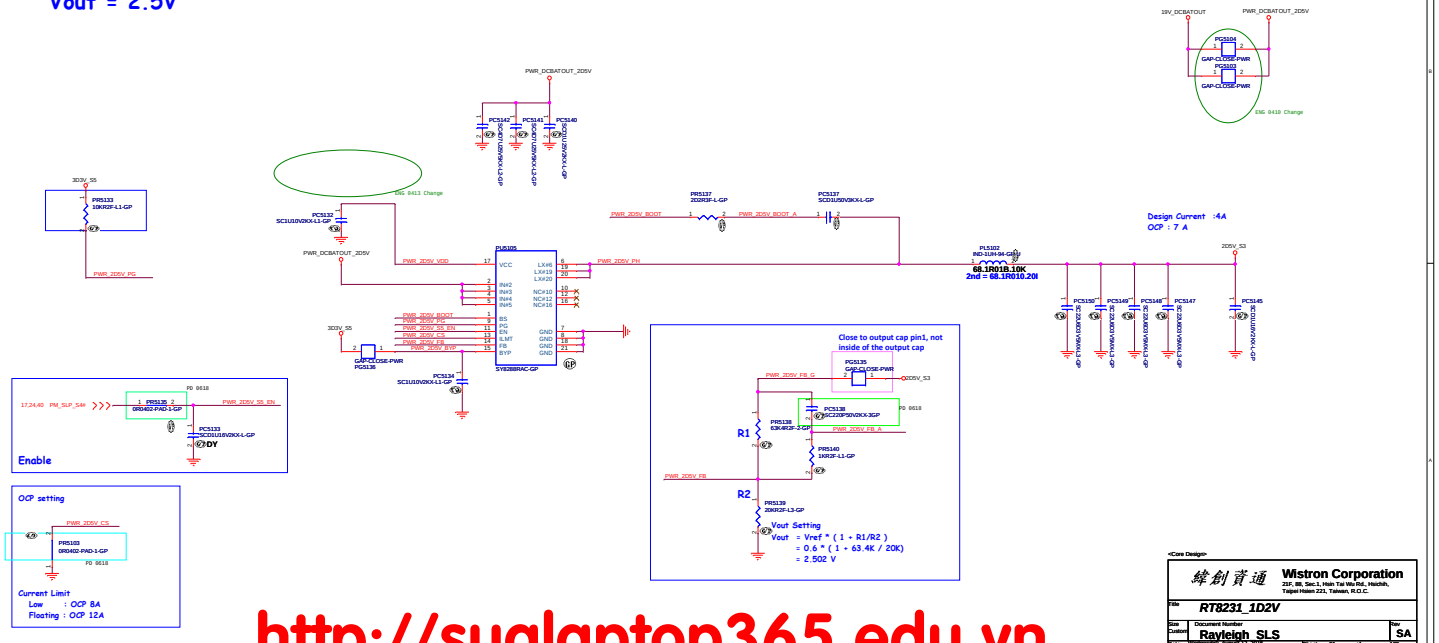
Size: A3 | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 50 of 105



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

SY8288 For DDR4
Vout = 2.5V



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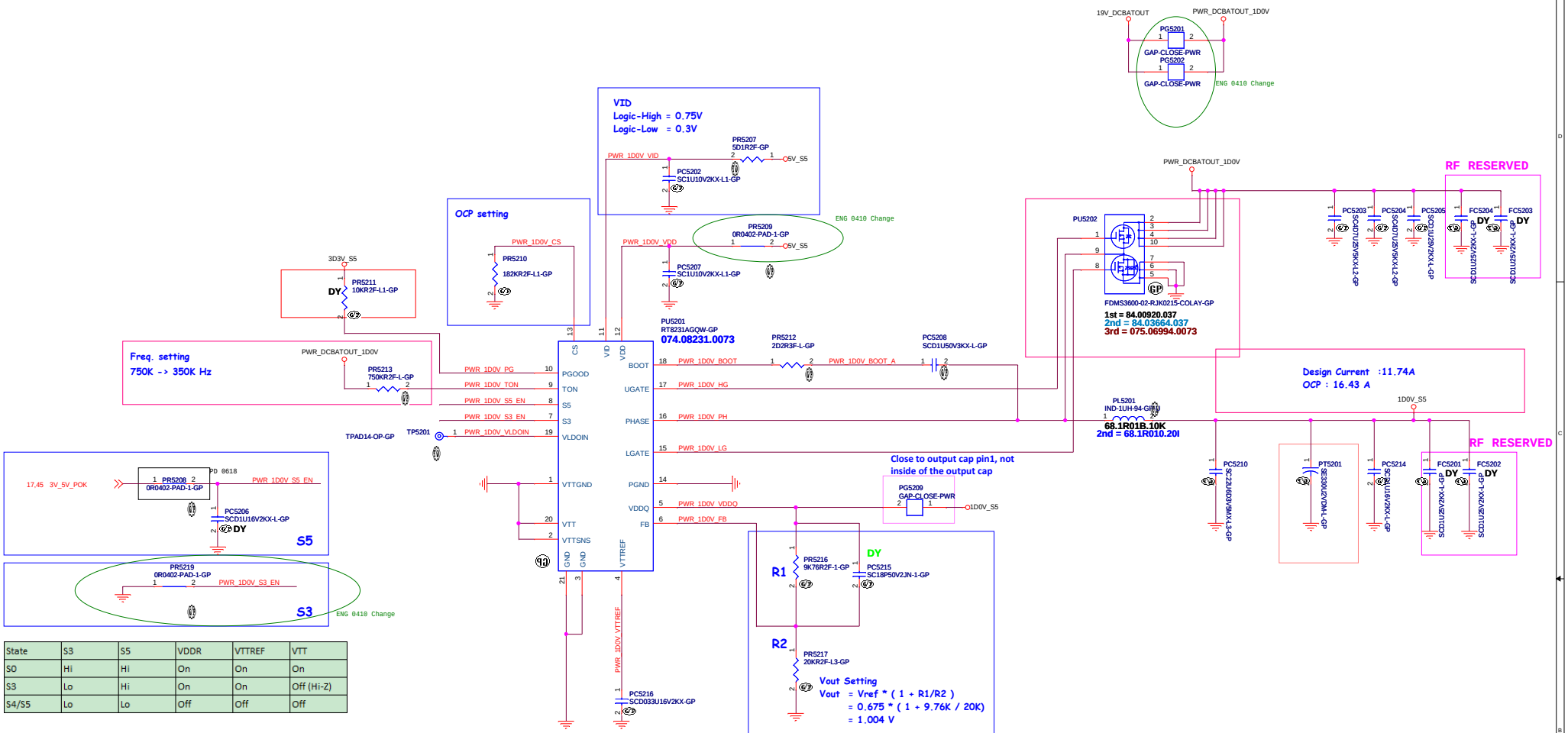
Title: RT8231_1D2V
Size: Custom | Document Number: Rayleigh_SLS | Rev: SA
Date: Wednesday, August 12, 2015 | Sheet 51 of 105



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

<Core Design>

緯創資通 Wistron Corporation
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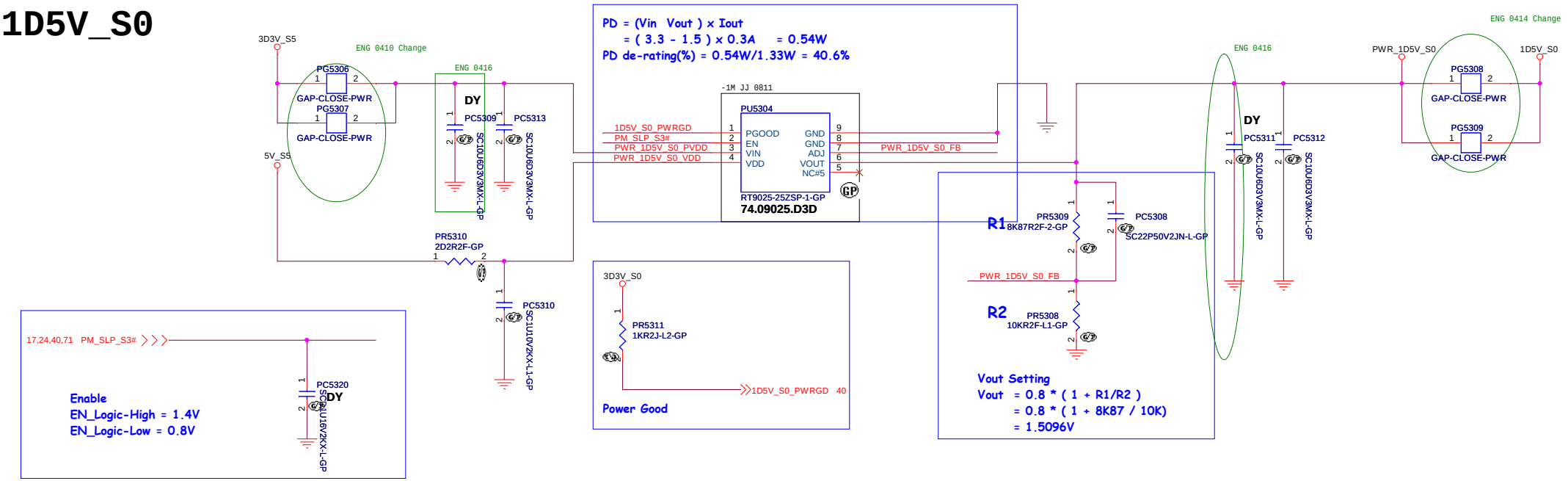
Title: RT8231_1D0V

Size: C | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 52 of 105

1D5V_S0



<Core Design>

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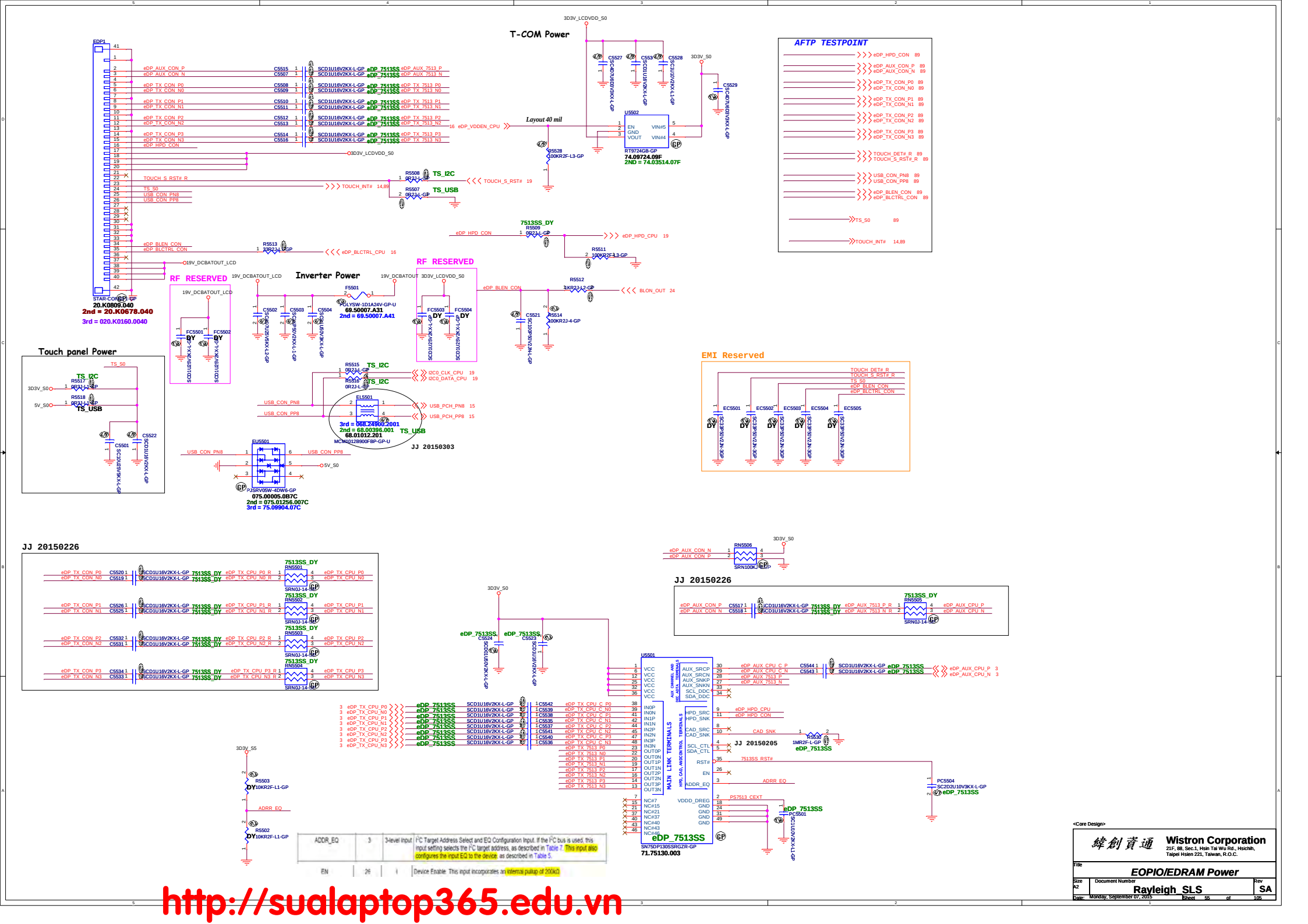
Title	*RT9025_1D5V*	
Size A3	Document Number Rayleigh_SLS	Rev SA
Date: Wednesday, August 12, 2015	Sheet 53 of 105	


T-COM Power
AFTP TESTPOINT
Inverter Power
RF RESERVED
RF RESERVED
Touch panel Power
EMI Reserved
JJ 20150303
JJ 20150226
JJ 20150226
JJ 20150205
eDP_7513SS
MAIN LINK TERMINALS
AUX CHANNEL AND DDC SIGNALS
HPD, CAD, AVDCONTROL TERMINALS
ADDR_EQ
3-level input
I²C Target Address Select and EQ Configuration Input. If the I²C bus is used, this input setting selects the I²C target address, as described in Table 7. This input also configures the input EQ to the device, as described in Table 5.
EN
Device Enable. This input incorporates an internal pullup of 200kΩ
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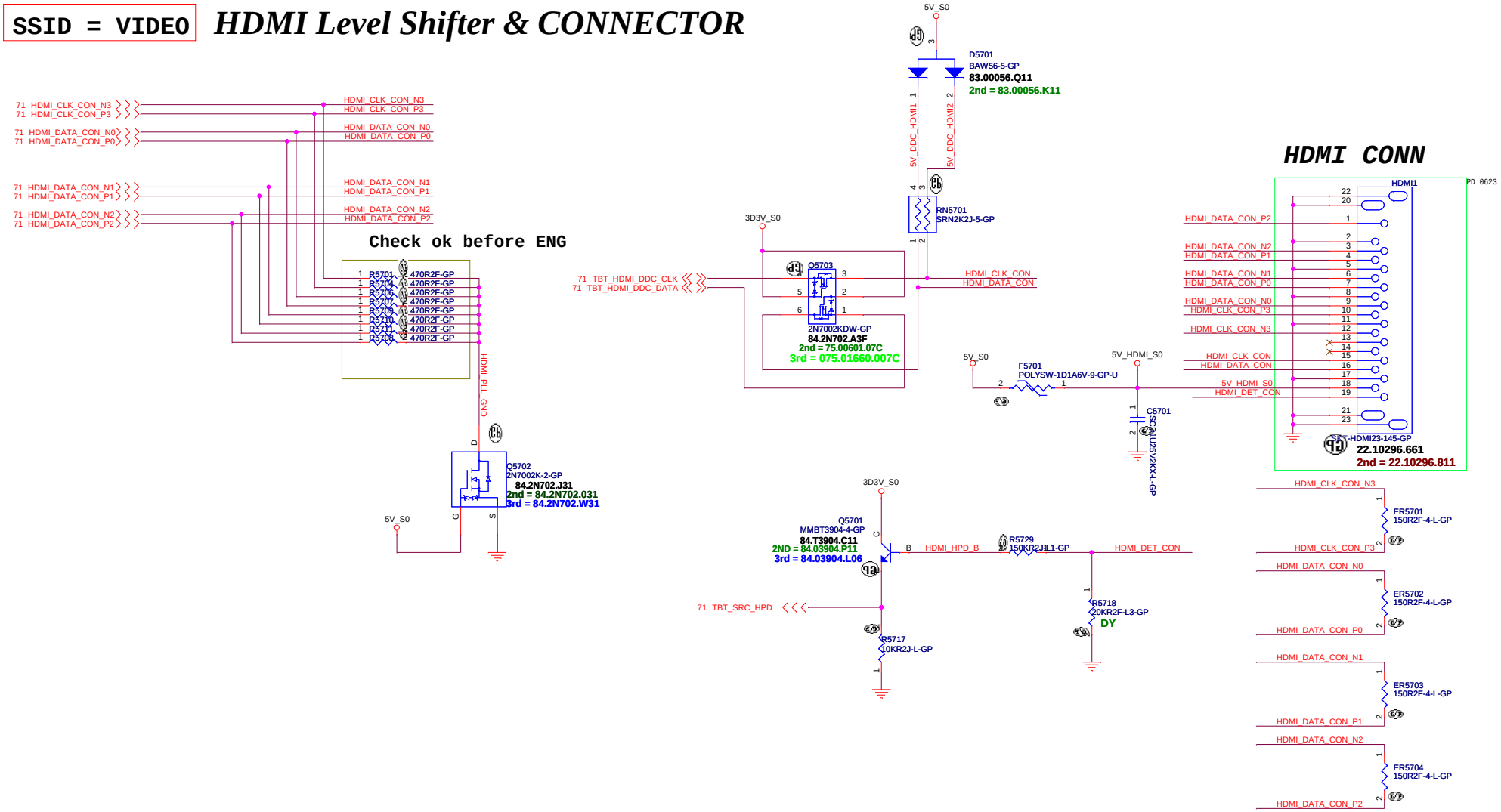
EOPIO/EDRAM Power
Rayleigh_SLS
SA
Monday, September 07, 2015

SSID = VIDEO

HDMI Level Shifter & CONNECTOR



緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Conn

Size: Custom | Document Number: Rayleigh_SLS | Rev: SA

Date: Tuesday, September 08, 2015 | Sheet 57 of 105

SSID = SATA

SATA HDD Connector

AFTP TESTPOINT

89 SATA_TX_HDD_P2
89 SATA_TX_HDD_N2
89 SATA_RX_HDD_N2
89 SATA_RX_HDD_P2

16 SATA_TX_CPU_P2
16 SATA_TX_CPU_N2
16 SATA_RX_CPU_N2
16 SATA_RX_CPU_P2

SCD01U50V2KX-L-GP C6003 SATA_TX_HDD_P2
SCD01U50V2KX-L-GP C6004 SATA_TX_HDD_N2
SCD01U50V2KX-L-GP C6005 SATA_RX_HDD_N2
SCD01U50V2KX-L-GP C6006 SATA_RX_HDD_P2

5V_S0

RF RESERVED

FC6001 DY SCD1U25V2KX-L-GP
FC6002 DY SCD1U25V2KX-L-GP
ENG 0416

C6001 SCS10U25V5KX-L-GP
C6002 SCD1U16V2KX-L-GP
ENG 0410 Change

HDD1
STAR-CON12-1-GP
020.K0125.0012
2nd = 020.K0049.0012
3rd = 20.K0793.012
ENG 0414 Change

AC coupling caps near connector < 100 mils

EU6001
PJE5UFN10A-GP
DY
SATA_TX_HDD_P2
SATA_TX_HDD_N2
SATA_RX_HDD_N2
SATA_RX_HDD_P2

075.00510.0073
2nd = 075.00550.0071
3rd = 75.01045.073

<Core Design>

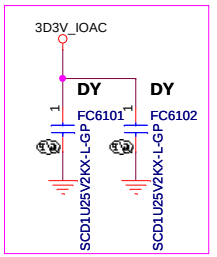
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

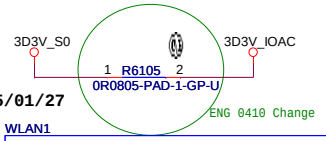
Title: HDD/ODD
Size: A4
Document Number: Rayleigh_SLS
Rev: SA
Date: Wednesday, August 12, 2015
Sheet 60 of 105

SSID = Wireless/ Wigig

NGFF Connector (802.11a/b/g/n)

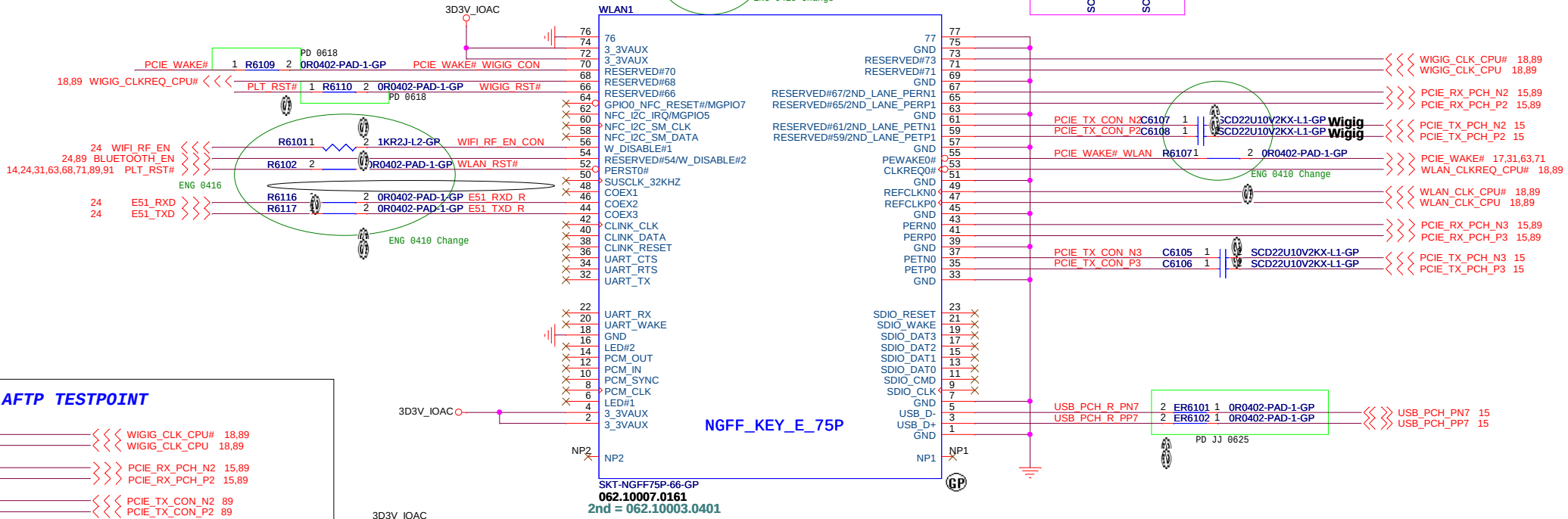
RF RESERVED

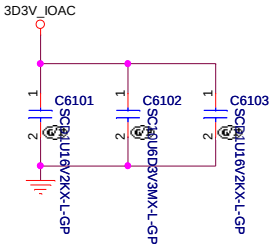


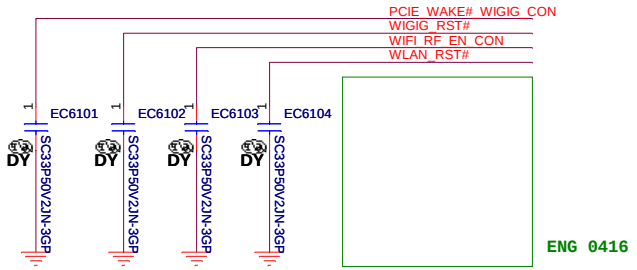


JJ 2015/01/27

ENG 0410 Change







ENG 0416

AFTP TESTPOINT

WIGIG_CLK_CPU# 18,89
WIGIG_CLK_CPU 18,89
PCIE_RX_PCH_N2 15,89
PCIE_RX_PCH_P2 15,89
PCIE_TX_CON_N2 89
PCIE_TX_CON_P2 89
PCIE_WAKE#_WLAN 89
WLAN_CLKREQ_CPU# 18,89
WLAN_CLK_CPU# 18,89
WLAN_CLK_CPU 18,89
PCIE_RX_PCH_N3 15,89
PCIE_RX_PCH_P3 15,89
PCIE_TX_CON_N3 89
PCIE_TX_CON_P3 89
USB_PCH_R_PN7 89
USB_PCH_R_PP7 89
PCIE_WAKE#_WIGIG_CON 89
WIGIG_CLKREQ_CPU# 18,89
WIGIG_RST# 89
WIFI_RF_EN_CON 89
BLUETOOTH_EN 24,89
WLAN_RST# 89
E51_RXD_R 89
E51_TXD_R 89

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Mini card-WLAN

Size: B | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 61 of 105

Mini Card Connector (NGFF m-SATA)

SSID = m-SATA

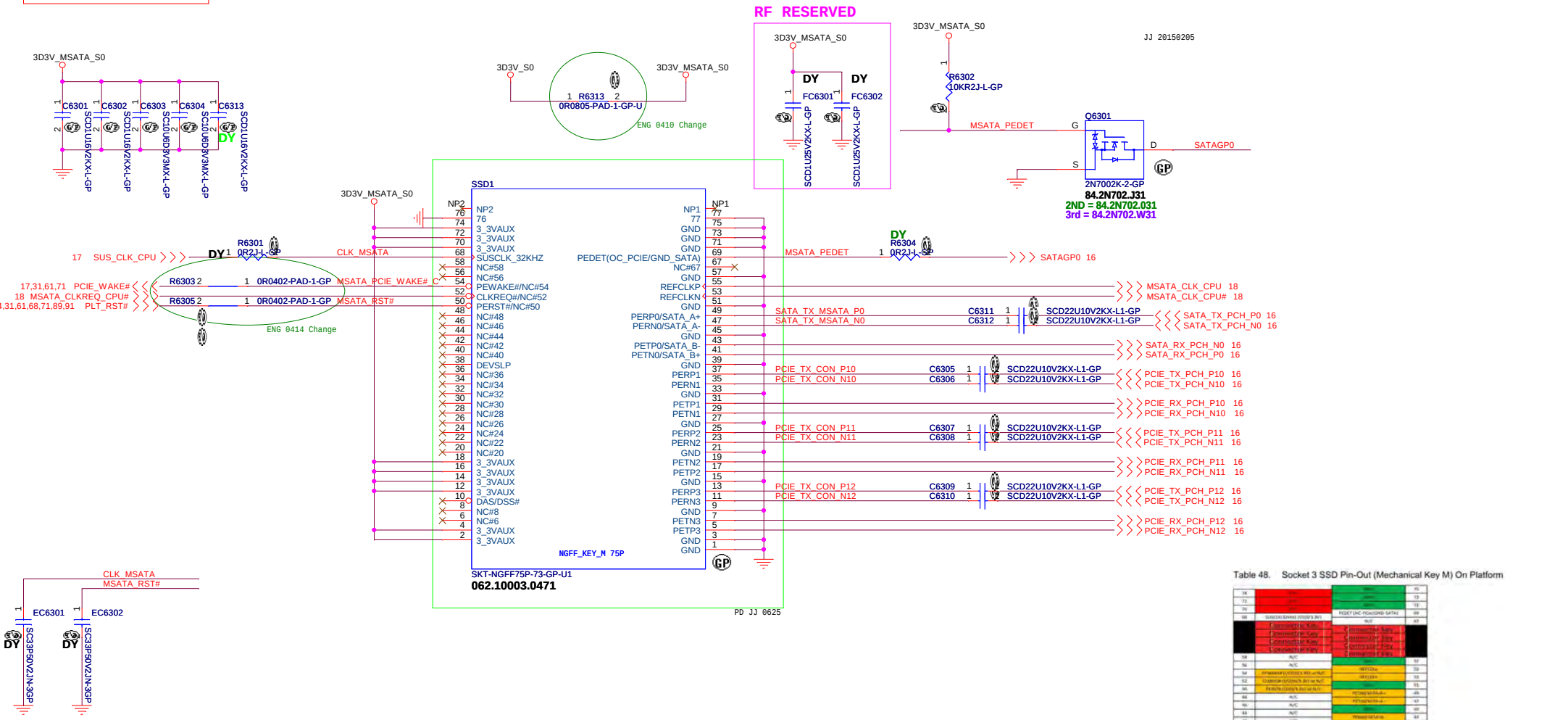

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Table 34-5. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

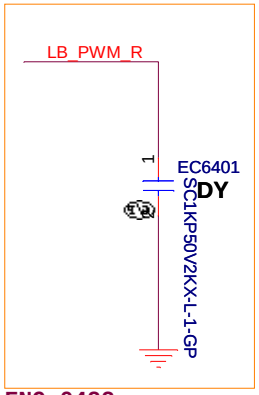
Title: **SSD-NGFF**

Size: A3 | Document Number: **Rayleigh_SLS** | Rev: **SA**

Date: Wednesday, August 12, 2015 | Sheet 63 of 105

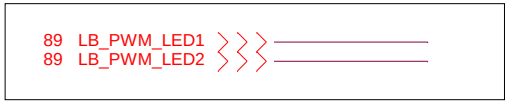
SSID = User.Interface

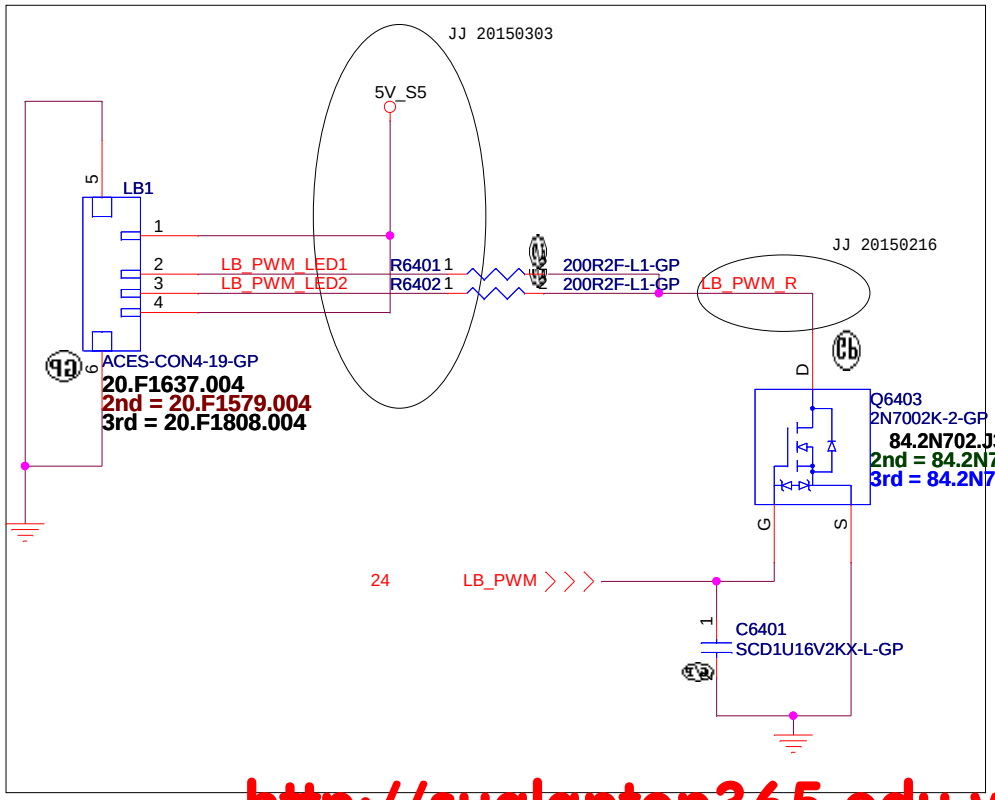
EMI Reserved



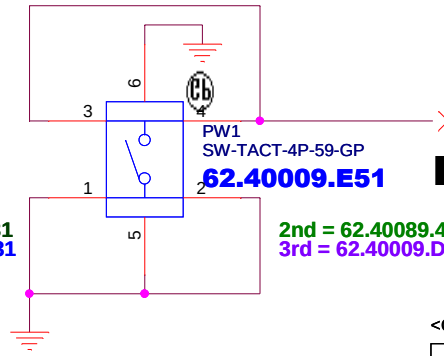
ENG 0422

AFTP TESTPOINT





Power Button



LAB

<Core Design>

緯創資通 Wistron Corporation
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Title: LED Bard/Power Button

Size	Document Number	Rev
A4	Rayleigh_SLS	SA

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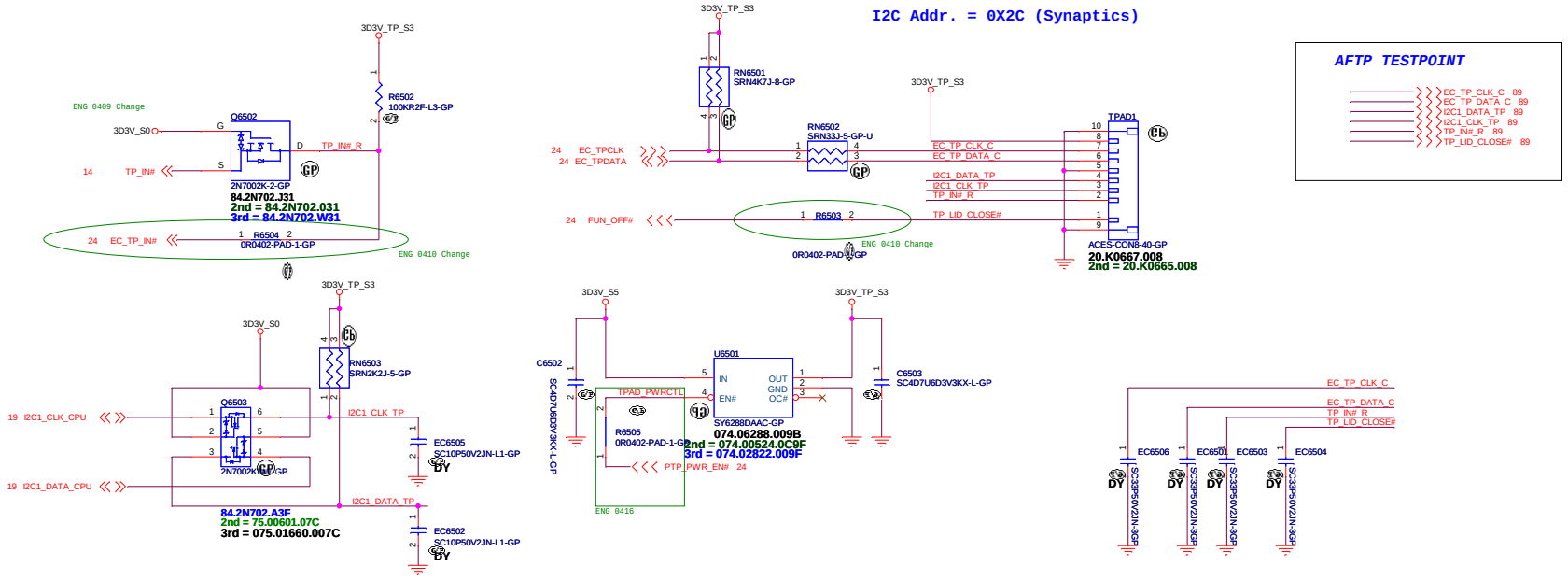
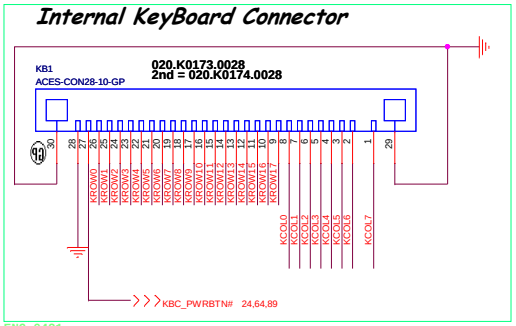
Precision Touch Pad

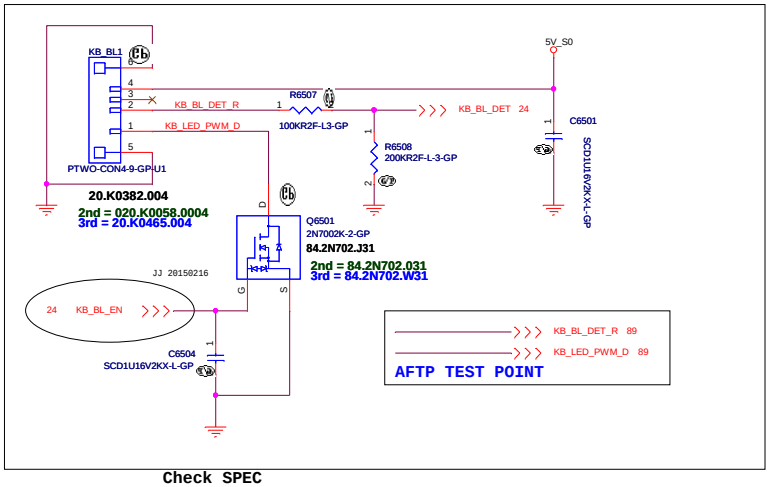
I2C Addr. = 0X2C (Synaptics)



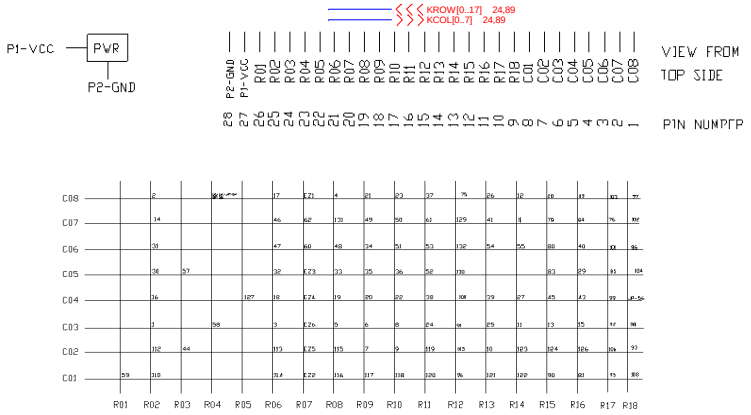
Internal KeyBoard Connector

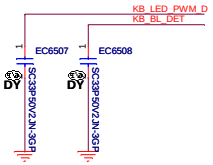


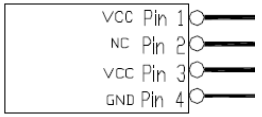
ENG 0421



Check SPEC







<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

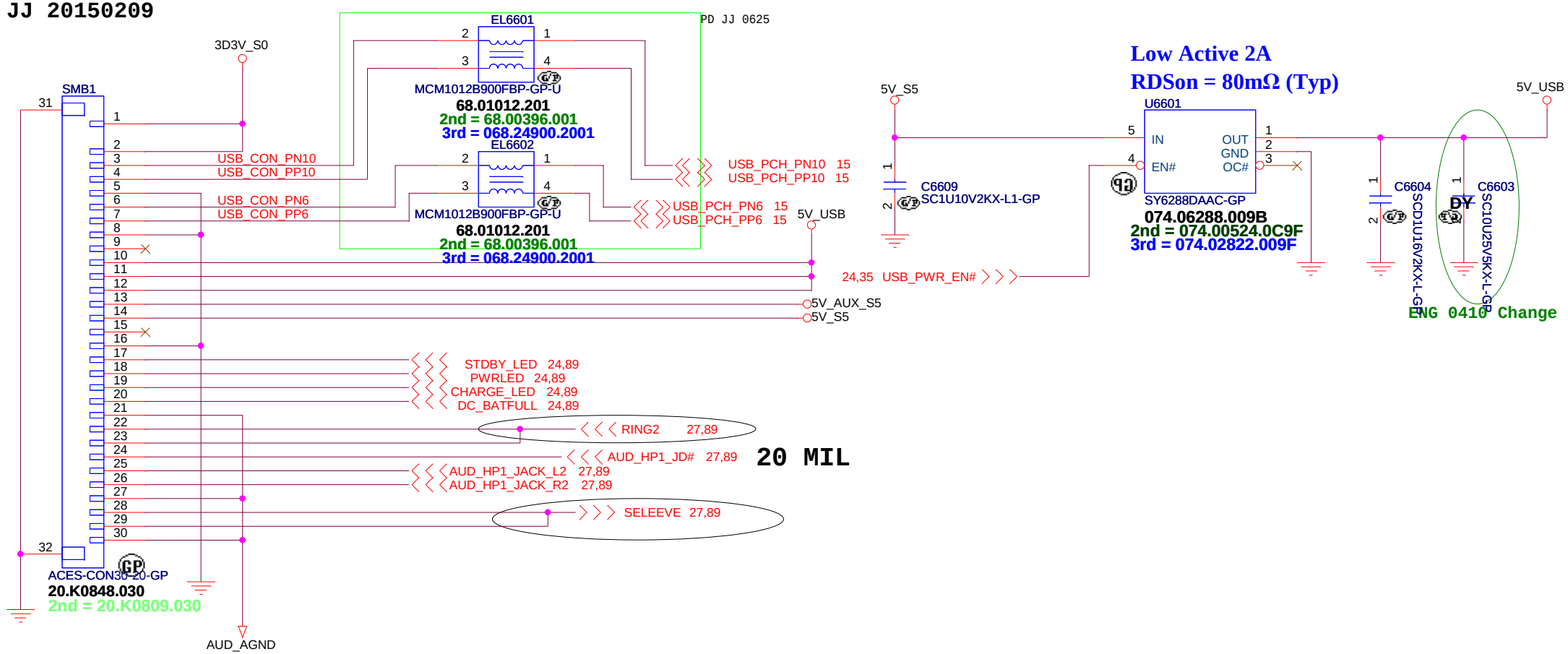
Title: **LED Bard / Power Button**

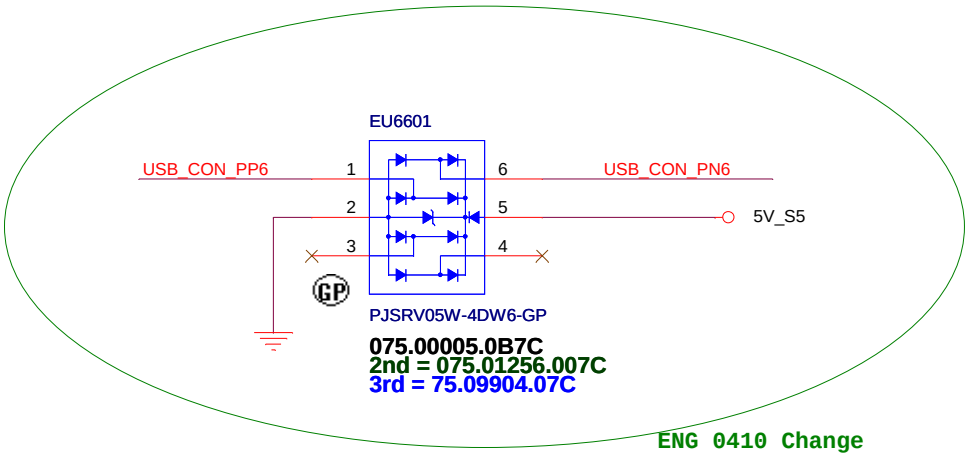
Size: Custom | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 12, 2015 | Sheet 65 of 105

JJ 20150209

PD JJ 0625





AFTP TESTPOINT

89 USB_CON_PN10
89 USB_CON_PP10
89 USB_CON_PN6
89 USB_CON_PP6

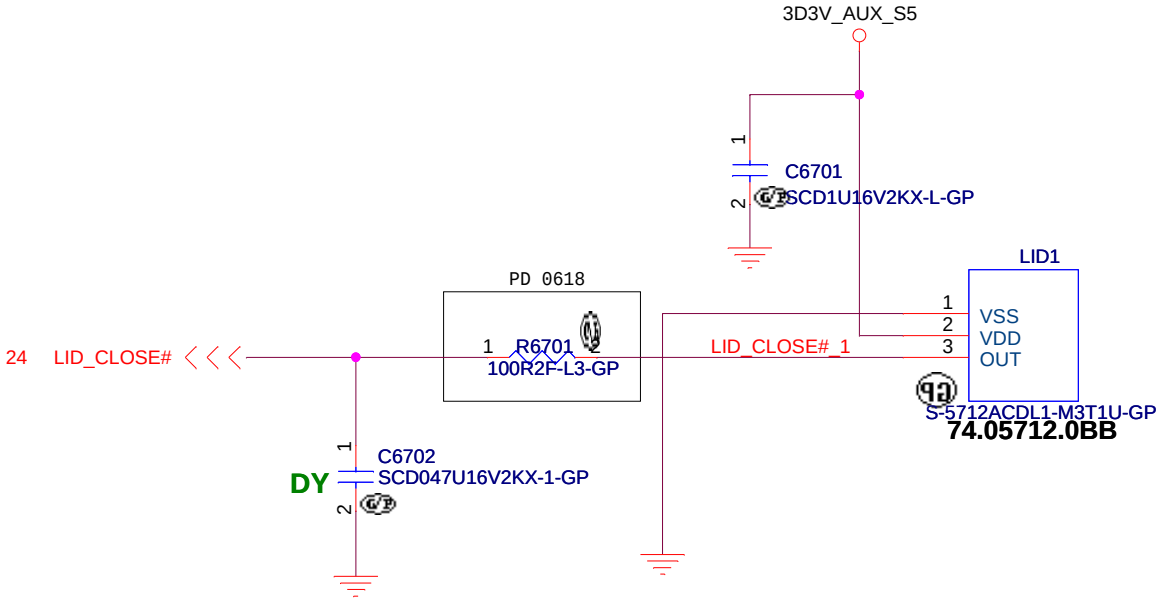
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A4	Rayleigh_SLS	SA

Date: Wednesday, August 12, 2015 Sheet 66 of 105



AFTP TESTPOINT

89 LID_CLOSE#_1

<Core Design>

緯創資通 **Wistron Corporation**
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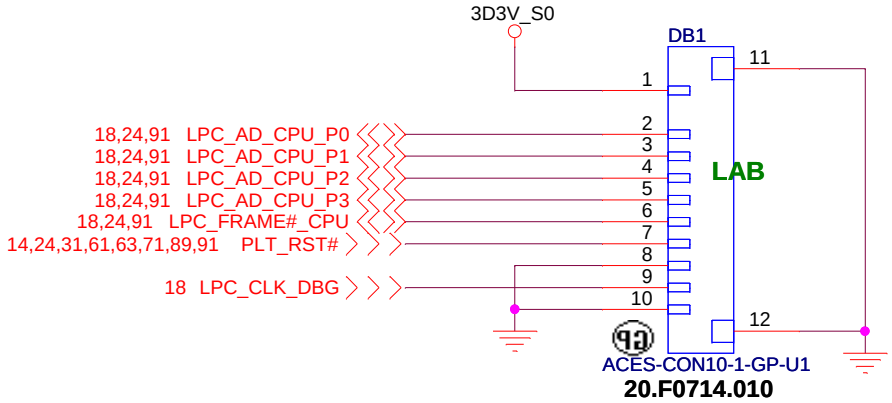
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A	Rayleigh_SLS	SA

Date: Wednesday, August 12, 2015 Sheet 67 of 105



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Debug connector***

Size	Document Number	Rev
A	**Rayleigh_SLS**	**SA**
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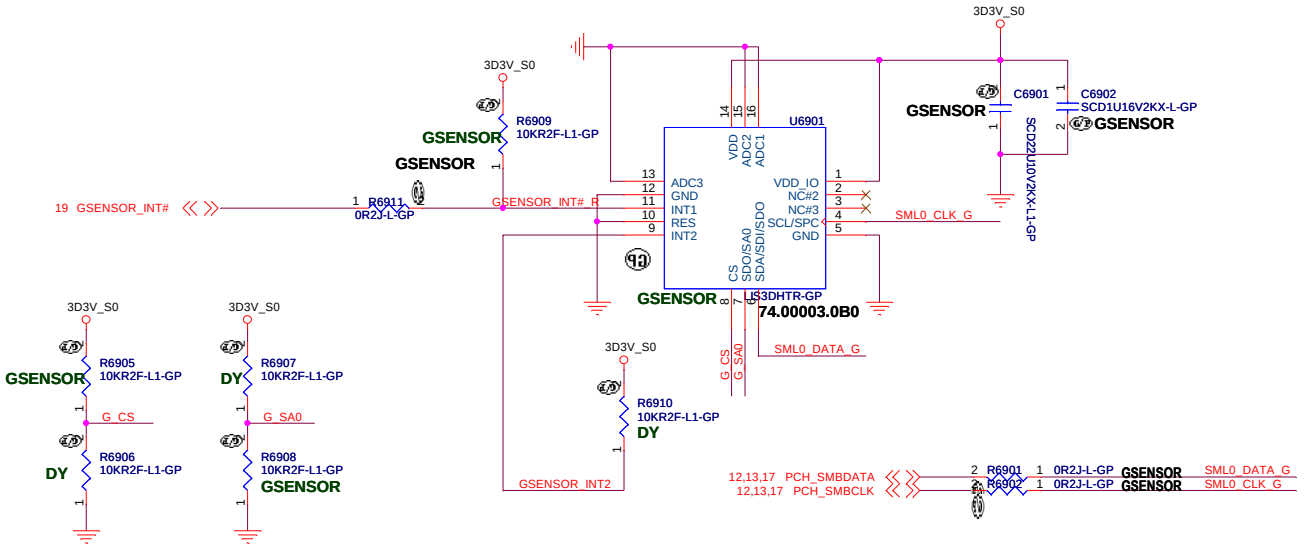
SSID = User.Interface

G Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

CHECK WITH MICK

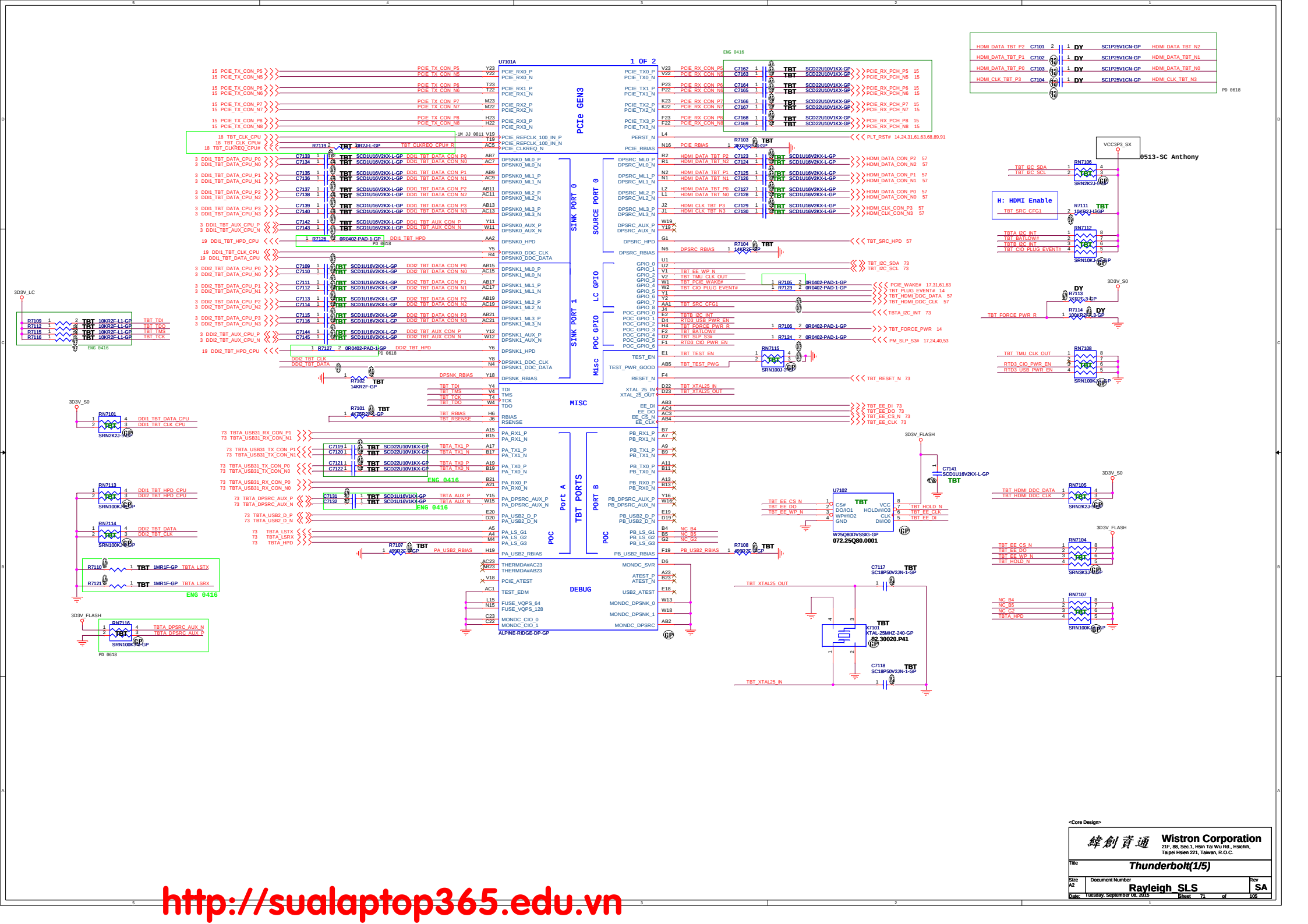


SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: G-SENSOR	
Size: A3	Document Number: Rayleigh_SLS — Rev: SA
Date: Wednesday, August 12, 2015	Sheet 69 of 105



<Core Design>

Wistron Corporation
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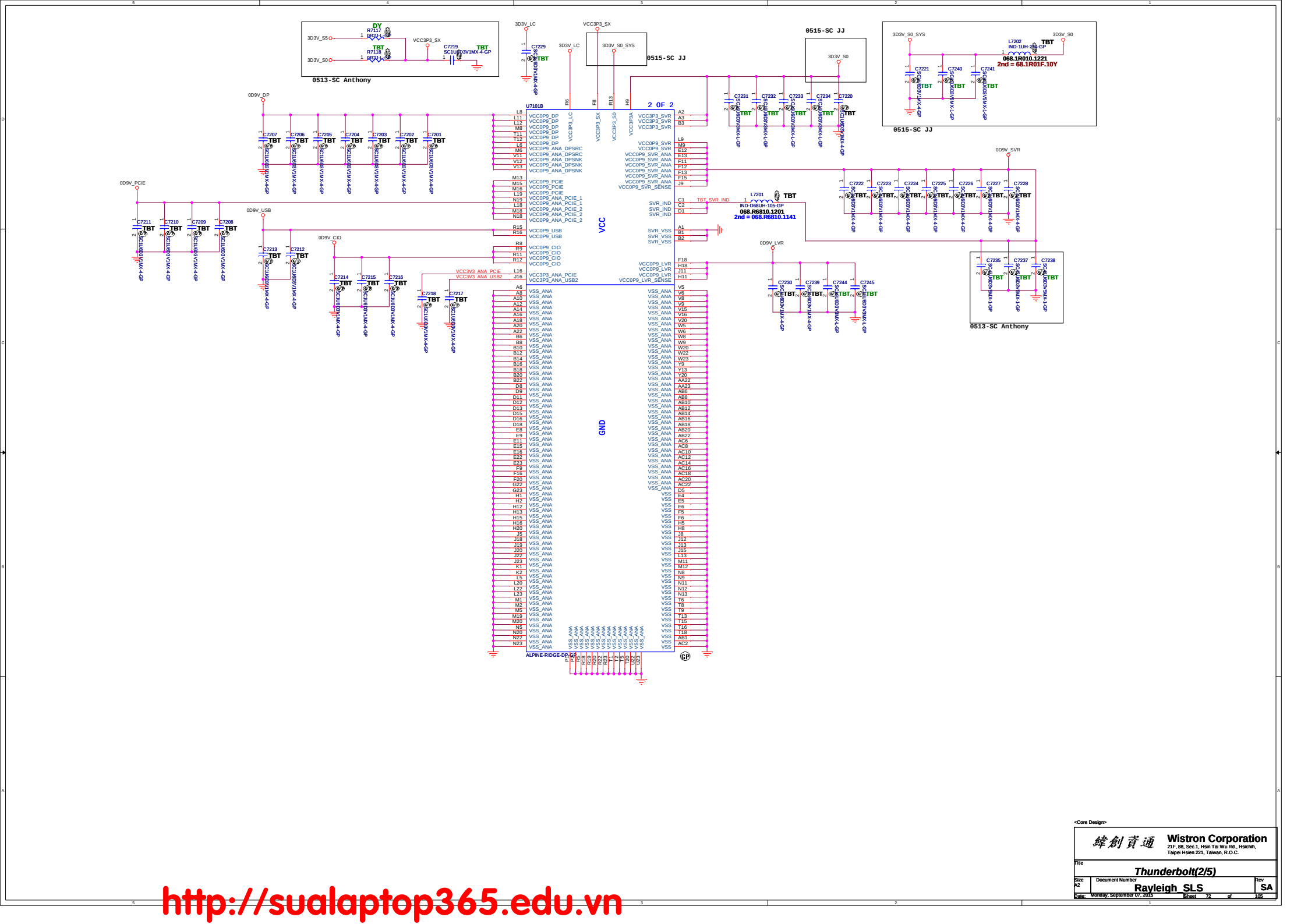
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thunderbolt(1/5)

Size: A2 | Document Number: Rayleigh_SLS | Rev: SA

Date: Tuesday, September 08, 2015 | Sheet 71 of 106


0513-SC Anthony
0515-SC JJ
U7101B
2 OF 2
VCC
GND
ALPINE-RIDGE-DD-GP
0D9V_DP
0D9V_PCIE
0D9V_USB
0D9V_CIO
0D9V_SVR
0D9V_LVR
L7201
IND-D68UH-105-GP
068.R6810.1201
2nd = 068.R6810.1141
L7202
IND-1UH-2R6-GP
068.1R010.1221
2nd = 68.1R01F.10Y
TBT_SVR_IND
VCC3V3_ANA_PCIE
VCC3V3_ANA_USB2
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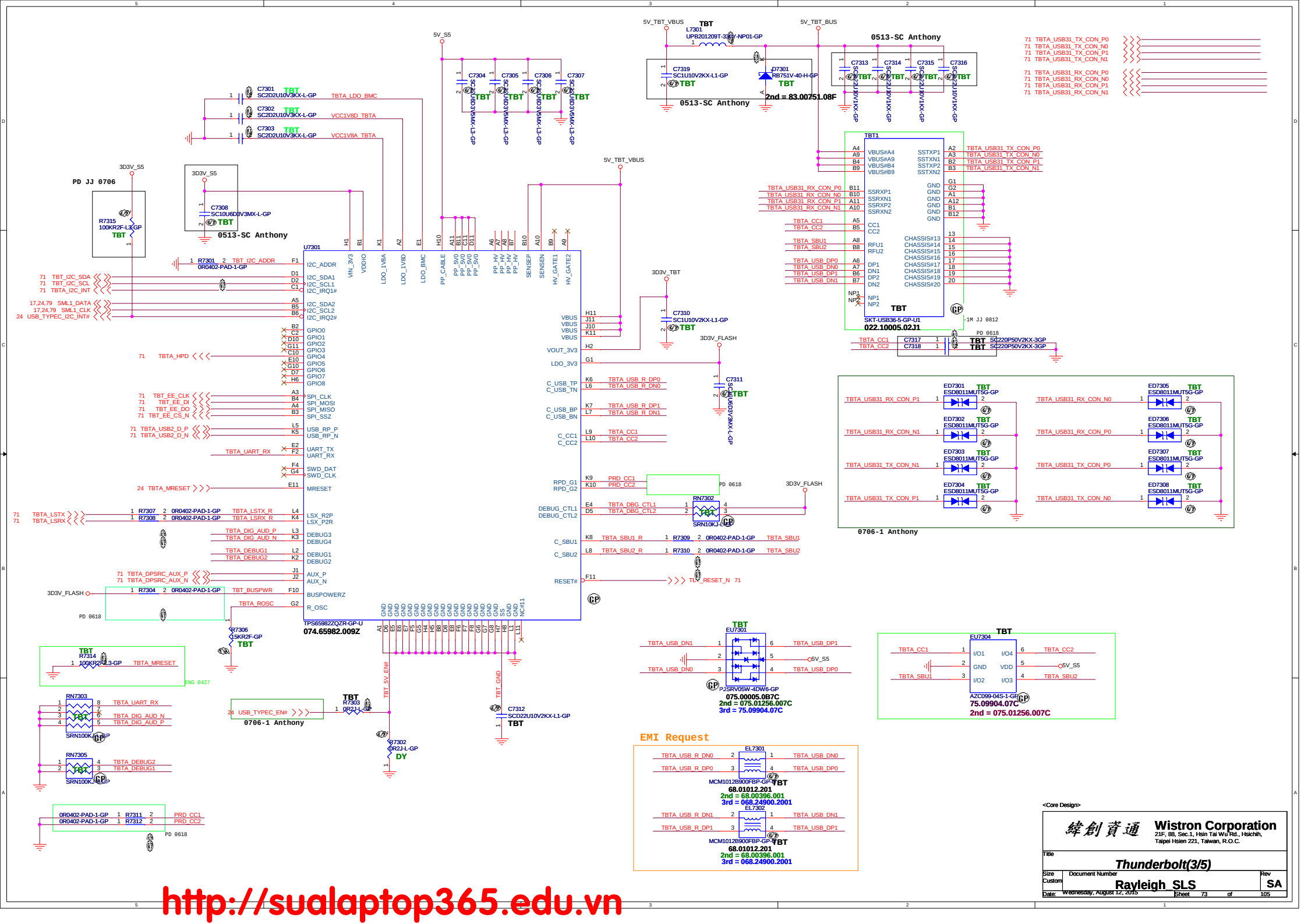
Thunderbolt(2/5)
Rayleigh_SLS
Monday, September 07, 2015


U7301
TPS65982ZQZR-GP-U
074.65982.009Z
PD JJ 0706
0513-SC Anthony
0706-1 Anthony
TBT1
SKT-USB36-5-GP-U1
022.10005.02J1
EU7301
PJSRV05W-4DW6-GP
075.00005.0B7C
2nd = 075.01256.007C
3rd = 75.09904.07C
EU7304
AZC099-04S-1-GP
75.09904.07C
2nd = 075.01256.007C
EL7301
EL7302
MCM1012B900FBP-GP-T
68.01012.201
2nd = 68.00396.001
3rd = 068.24900.2001
EMI Request
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Thunderbolt(3/5)
Rayleigh_SLS
Wednesday, August 12, 2015
http://sualaptop365.edu.vn

EMI Reserved

VGA_RST# — EC7601 — SC339P50V2KN-3GP

14,79 DGPU_HOLD_RST# — R7603 — VGA_RST#

R2J-L-GP

NON_GC6

ENG 0410 Change

3D3V_AON_S0 — R7604 10KR2J-L-GP Muxless

Q7601 2N7002K-2-GP Muxless

18 PEG_CLKREQ_CPU#

3rd = 84.2N702.W31
2nd = 84.2N702.031
84.2N702.J31

79 VGA_RST#

18 PEG_CLK_CPU
18 PEG_CLK_CPU#

GPU_PWR_EN (from SYSTEM) — 3V3_AON — 3V3_MAIN_EN — 3V3_MAIN — PEX & 1.05V — NVVDD — FBVDD/Q power enable — FBVDD/Q — GC6_FB_EN

GPU

3V3_MAIN_EN
GC6_FB_EN
Voltage Regulator Complex
GPU_PWR_EN
GPU_EVENT#
SYS_PEX_RST_MON#
GPU_PEX_RST_HOLD#
GPU_RST#
PLATFORM_RST#
GPU_PEX_RST#
PCH

VGA1A — 1 OF 17

PEX_WAKE# AJ11
PEX_RST# AJ12
PEX_CLKREQ# AK12 — PEG_CLKREQ_dGPU#
PEX_REFCLK AL13
PEX_REFCLK# AK13

PEX_IOVDD_1 AG19
PEX_IOVDD_2 AG21
PEX_IOVDD_3 AG22
PEX_IOVDD_4 AG24
PEX_IOVDD_5 AH21
PEX_IOVDD_6 AH25

PEX_IOVDDQ_1 AG13
PEX_IOVDDQ_2 AG15
PEX_IOVDDQ_3 AG16
PEX_IOVDDQ_4 AG18
PEX_IOVDDQ_5 AG25
PEX_IOVDDQ_6 AH15
PEX_IOVDDQ_7 AH18
PEX_IOVDDQ_8 AH26
PEX_IOVDDQ_9 AH27
PEX_IOVDDQ_10 AJ27
PEX_IOVDDQ_11 AK27
PEX_IOVDDQ_12 AL27
PEX_IOVDDQ_13 AM28
PEX_IOVDDQ_14 AN28

1D05V_VGA_S0 — SCD22U10V2KX-L1-GP Muxless — SC10U6D3V3MX-L-GP Muxless

Place under GPU — Place near GPU

PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12

3D3V_AON_S0 — SCD22U10V2KX-L-GP Muxless — SC4D7U6D3V3KX-L-GP Muxless

Place near GPU

VDD_SENSE L4 — NVVDD_SENSE 85
GND_SENSE L5 — NVGND_SENSE 85

NC#P8 P8

DY — 200R2F-L1-GP

PEX_TSTCLK_OUT AJ26 — VGAPEX_AJ26 — R7605
PEX_TSTCLK_OUT# AK26 — VGAPEX_AK26

Place near AG26

PEX_PLLVDD AG26

TESTMODE AK11 TESTMODE — R7606 10KR2J-L-GP Muxless

PEX_TERMP AP29 PEX_TERMP — R7607 2K49R2F-2-L-GP Muxless

Place near GPU

PEG_RX_CPU_P0 / PEG_RX_CPU_N0 — C7601 / C7606 — PEG_RX_CON_P0 / PEG_RX_CON_N0 — AK14 / AJ14 — PEX_TX0 / PEX_TX0#
PEG_TX_CON_P0 / PEG_TX_CON_N0 — AN12 / AM12 — PEX_RX0 / PEX_RX0#
PEG_RX_CPU_P1 / PEG_RX_CPU_N1 — C7607 / C7608 — PEG_RX_CON_P1 / PEG_RX_CON_N1 — AH14 / AG14 — PEX_TX1 / PEX_TX1#
PEG_TX_CON_P1 / PEG_TX_CON_N1 — AN14 / AM14 — PEX_RX1 / PEX_RX1#
PEG_RX_CPU_P2 / PEG_RX_CPU_N2 — C7613 / C7614 — PEG_RX_CON_P2 / PEG_RX_CON_N2 — AK15 / AJ15 — PEX_TX2 / PEX_TX2#
PEG_TX_CON_P2 / PEG_TX_CON_N2 — AP14 / AP15 — PEX_RX2 / PEX_RX2#
PEG_RX_CPU_P3 / PEG_RX_CPU_N3 — C7615 / C7616 — PEG_RX_CON_P3 / PEG_RX_CON_N3 — AL16 / AK16 — PEX_TX3 / PEX_TX3#
PEG_TX_CON_P3 / PEG_TX_CON_N3 — AN15 / AM15 — PEX_RX3 / PEX_RX3#
PEG_RX_CPU_P4 / PEG_RX_CPU_N4 — C7617 / C7618 — PEG_RX_CON_P4 / PEG_RX_CON_N4 — AK17 / AJ17 — PEX_TX4 / PEX_TX4#
PEG_TX_CON_P4 / PEG_TX_CON_N4 — AN17 / AM17 — PEX_RX4 / PEX_RX4#
PEG_RX_CPU_P5 / PEG_RX_CPU_N5 — C7619 / C7620 — PEG_RX_CON_P5 / PEG_RX_CON_N5 — AH17 / AG17 — PEX_TX5 / PEX_TX5#
PEG_TX_CON_P5 / PEG_TX_CON_N5 — AP17 / AP18 — PEX_RX5 / PEX_RX5#
PEG_RX_CPU_P6 / PEG_RX_CPU_N6 — C7621 / C7622 — PEG_RX_CON_P6 / PEG_RX_CON_N6 — AK18 / AJ18 — PEX_TX6 / PEX_TX6#
PEG_TX_CON_P6 / PEG_TX_CON_N6 — AN18 / AM18 — PEX_RX6 / PEX_RX6#
PEG_RX_CPU_P7 / PEG_RX_CPU_N7 — C7625 / C7626 — PEG_RX_CON_P7 / PEG_RX_CON_N7 — AL19 / AK19 — PEX_TX7 / PEX_TX7#
PEG_TX_CON_P7 / PEG_TX_CON_N7 — AN20 / AM20 — PEX_RX7 / PEX_RX7#
PEG_RX_CPU_P8 / PEG_RX_CPU_N8 — C7627 / C7628 — PEG_RX_CON_P8 / PEG_RX_CON_N8 — AK20 / AJ20 — PEX_TX8 / PEX_TX8#
PEG_TX_CON_P8 / PEG_TX_CON_N8 — AP20 / AP21 — PEX_RX8 / PEX_RX8#
PEG_RX_CPU_P9 / PEG_RX_CPU_N9 — C7629 / C7630 — PEG_RX_CON_P9 / PEG_RX_CON_N9 — AH20 / AG20 — PEX_TX9 / PEX_TX9#
PEG_TX_CON_P9 / PEG_TX_CON_N9 — AN21 / AM21 — PEX_RX9 / PEX_RX9#
PEG_RX_CPU_P10 / PEG_RX_CPU_N10 — C7631 / C7632 — PEG_RX_CON_P10 / PEG_RX_CON_N10 — AK21 / AJ21 — PEX_TX10 / PEX_TX10#
PEG_TX_CON_P10 / PEG_TX_CON_N10 — AN23 / AM23 — PEX_RX10 / PEX_RX10#
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PEG_TX_CON_P11 / PEG_TX_CON_N11 — AP23 / AP24 — PEX_RX11 / PEX_RX11#
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PEG_TX_CON_P12 / PEG_TX_CON_N12 — AN24 / AM24 — PEX_RX12 / PEX_RX12#
PEG_RX_CPU_P13 / PEG_RX_CPU_N13 — C7637 / C7638 — PEG_RX_CON_P13 / PEG_RX_CON_N13 — AH23 / AG23 — PEX_TX13 / PEX_TX13#
PEG_TX_CON_P13 / PEG_TX_CON_N13 — AN26 / AM26 — PEX_RX13 / PEX_RX13#
PEG_RX_CPU_P14 / PEG_RX_CPU_N14 — C7639 / C7640 — PEG_RX_CON_P14 / PEG_RX_CON_N14 — AK24 / AJ24 — PEX_TX14 / PEX_TX14#
PEG_TX_CON_P14 / PEG_TX_CON_N14 — AP26 / AP27 — PEX_RX14 / PEX_RX14#
PEG_RX_CPU_P15 / PEG_RX_CPU_N15 — C7644 / C7645 — PEG_RX_CON_P15 / PEG_RX_CON_N15 — AL25 / AK25 — PEX_TX15 / PEX_TX15#
PEG_TX_CON_P15 / PEG_TX_CON_N15 — AN27 / AM27 — PEX_RX15 / PEX_RX15#

SCD22U10V2KX-L1-GP Muxless

N15P-GT-A2-GP

071.0N15P.000U
Muxless

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Title: GPU_840M_PEG (1/5)

Size: Custom | Document Number: Rayleigh_SLS | Rev: SA

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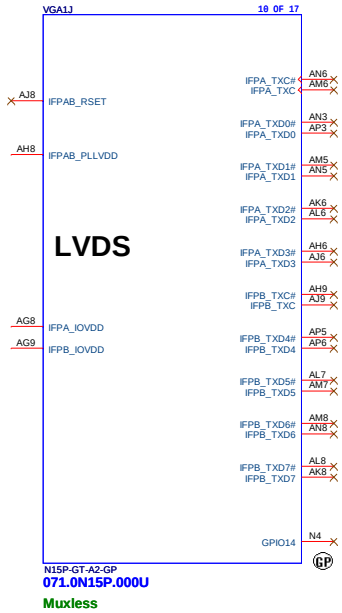

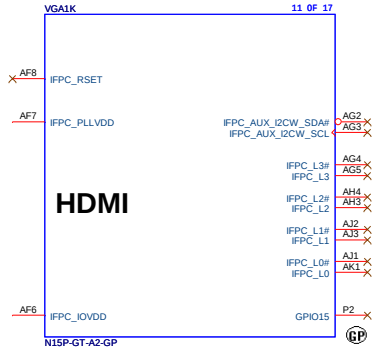

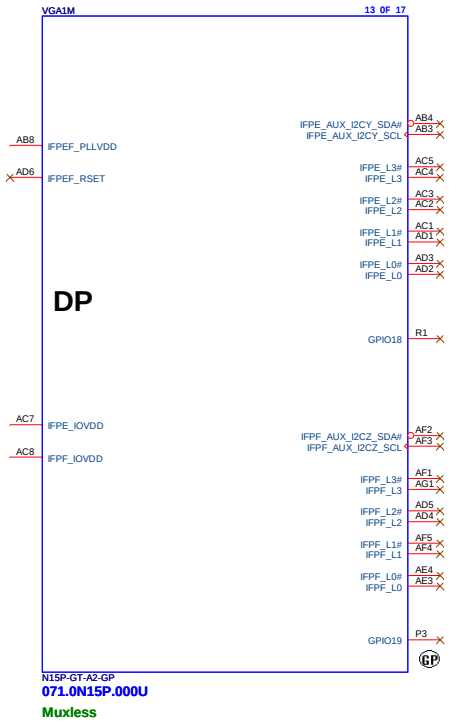

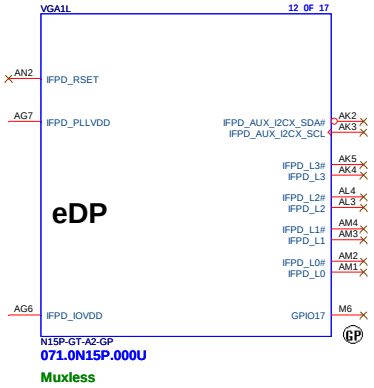

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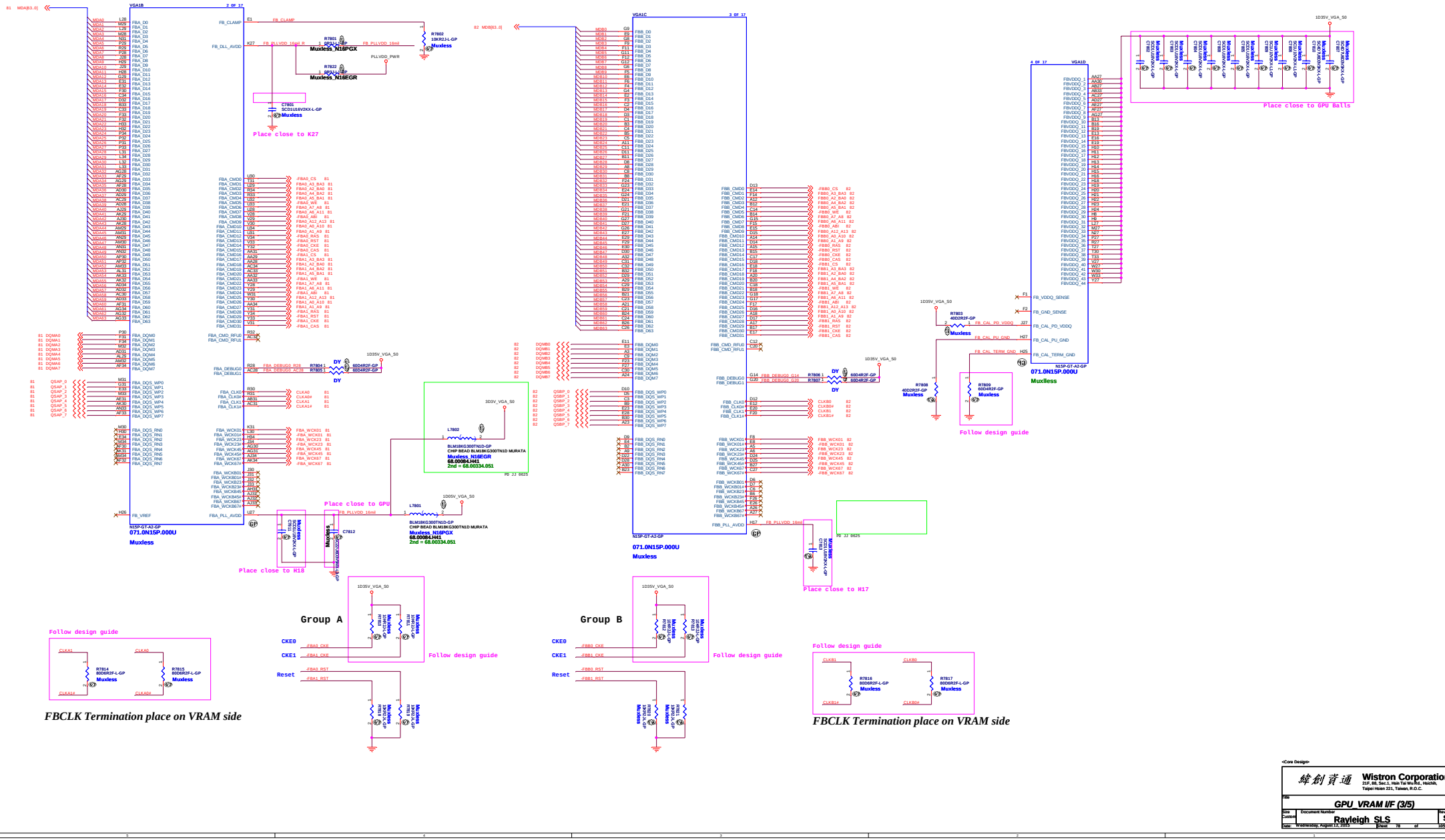
Title: GPU_DIGITALOUT (2/5)		
Size: Custom	Document Number: Rayleigh_SLS	Rev: SA
Date: Wednesday, August 12, 2015	Sheet 77 of 105	



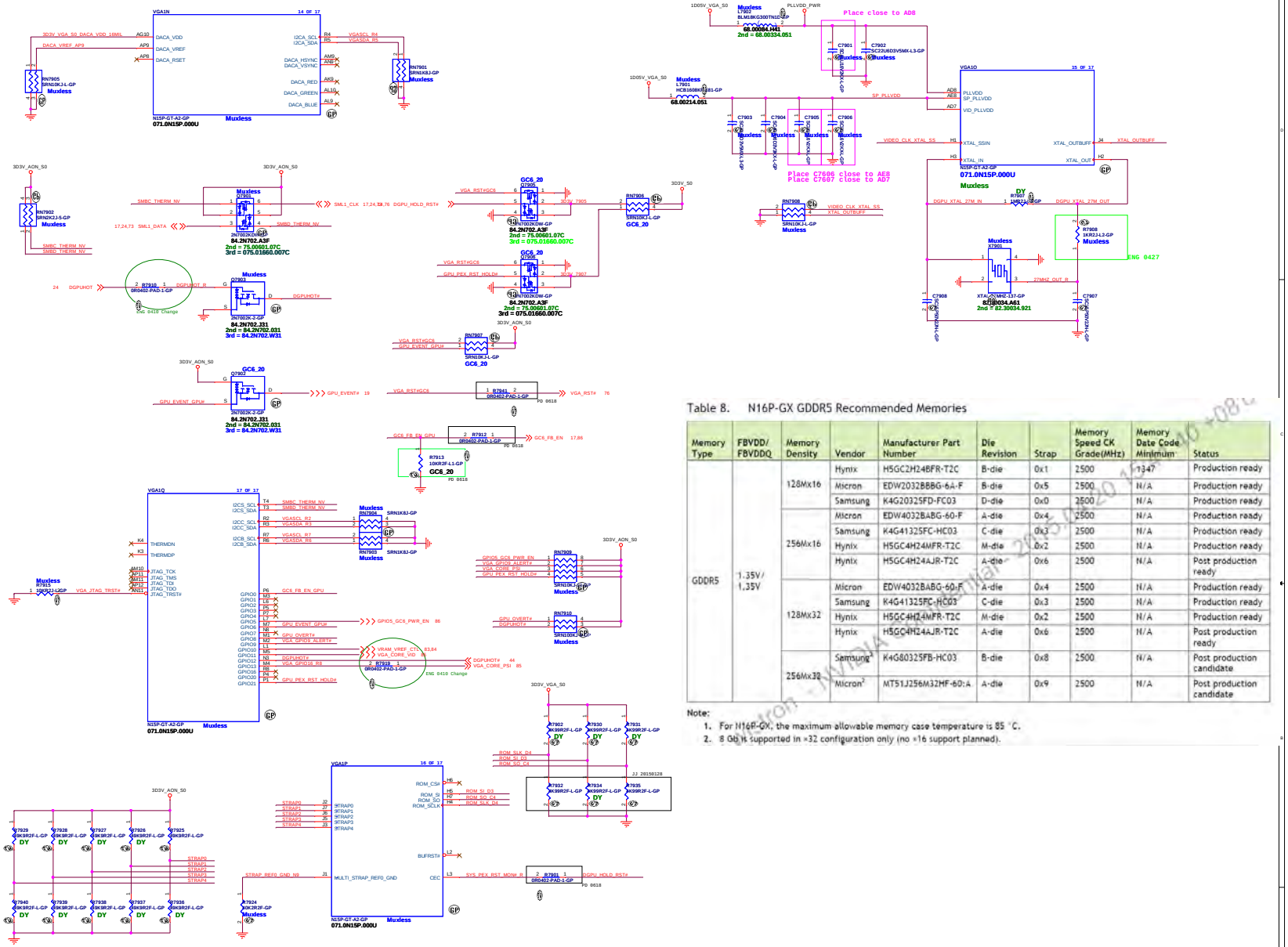


Table 8. N16P-GX GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V	128Mx16	Hynix	H5GC2H24BFR-T2C	B-die	0x1	2500	1347	Production ready
			Micron	EDW2032BBBG-6A-F	B-die	0x5	2500	N/A	Production ready
			Samsung	K4G20325FD-FC03	D-die	0x0	2500	N/A	Production ready
		256Mx16	Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24MFR-T2C	M-die	0x2	2500	N/A	Production ready
			Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Post production ready
		128Mx32	Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24MFR-T2C	M-die	0x2	2500	N/A	Production ready
			Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Post production ready
		256Mx32	Samsung[1]	K4G80325FB-HC03	B-die	0x8	2500	N/A	Post production candidate
			Micron[2]	MT51J256M32HF-60:A	A-die	0x9	2500	N/A	Post production candidate

Note:
1. For N16P-GX, the maximum allowable memory case temperature is 85 °C.
2. 8 Gb is supported in ×32 configuration only (no ×16 support planned).

Table 15-2. Resistance Mapping to Hex Values

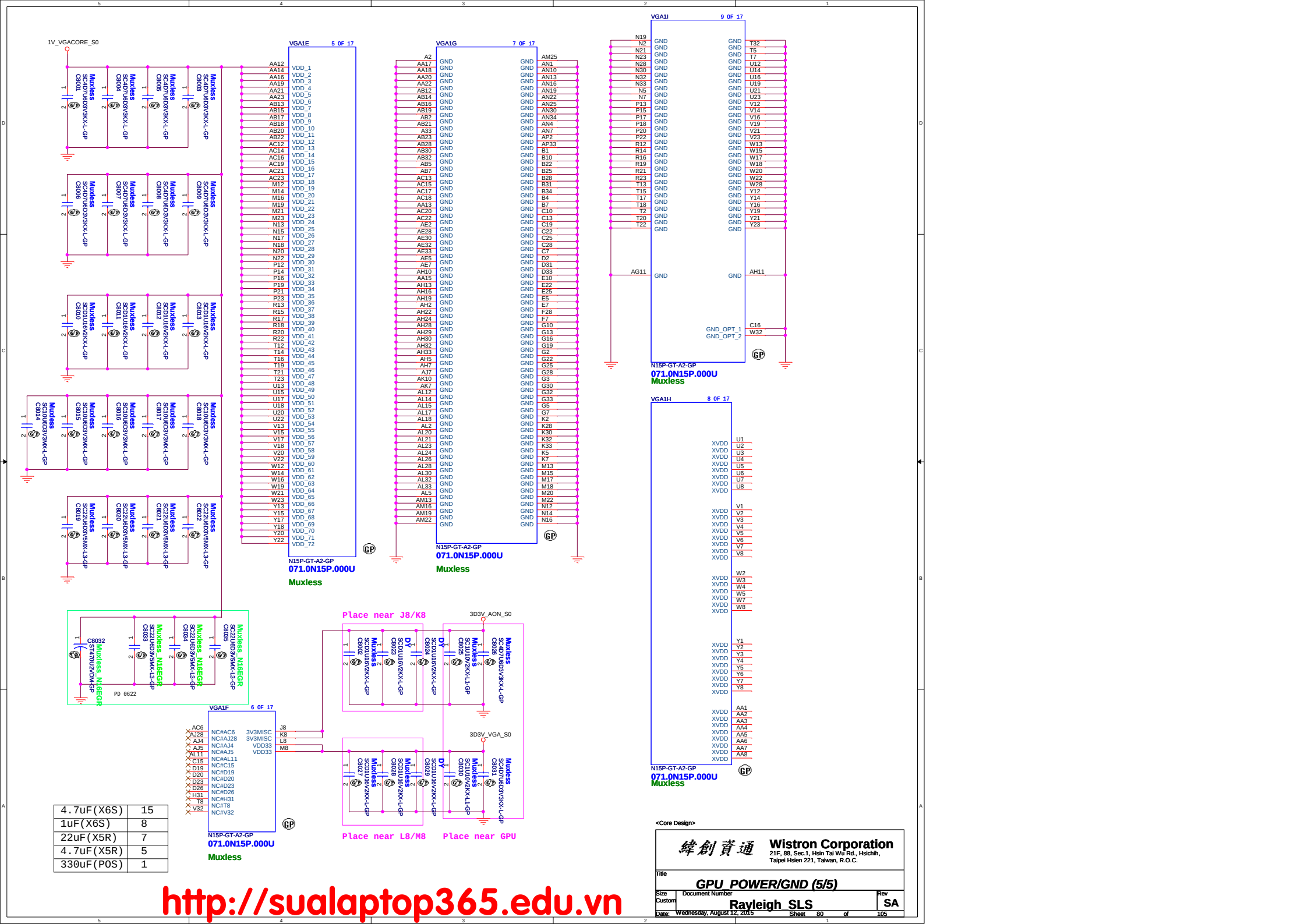
Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

4.99Kohm	64.49915.6DL
10Kohm	64.10025.1.0L
15Kohm	64.15025.6DL
20Kohm	64.20025.6DL
24.9Kohm	64.24925.6DL
30.1Kohm	64.30125.6DL
34.8Kohm	64.34825.6DL
45Kohm	64.45325.6DL

Table 15-3. GB2B-64 and GB4B-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND and stuff 50kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND for forward compatibility.			

Title: GPU_GPIO/STRAP
Size: Custom | Document Number: Rayleigh_SLS | Rev: SA
Date: Wednesday, August 01, 2012 | Sheet 79 of 105



4.7uF(X6S)	15
1uF(X6S)	8
22uF(X5R)	7
4.7uF(X5R)	5
330uF(POS)	1

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Title: GPU_POWER/GND (5/5)

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TABLE
GDDR5 VIDEO MEMORY 72.05224.A0U 72.20325.B0U

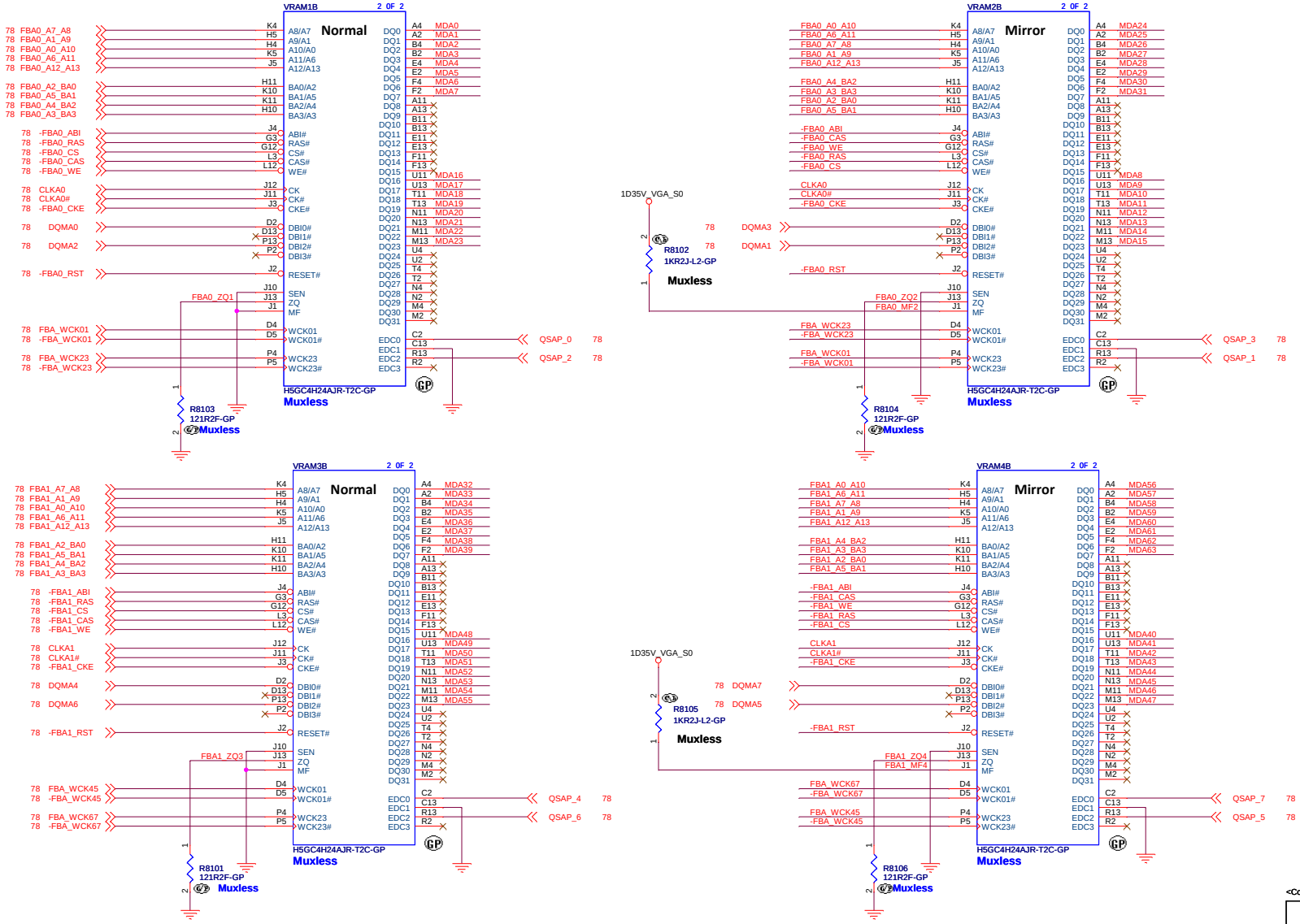
	HYNIX 2GBITS (64Mx32)	SAMSUNG 2GBITS (64Mx32)	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)
U91 U92 U93 U94 U95 U96 U97 U98	H5GQ2H24AFR-T2C	K4G20325FD-FC04	H5GC4H24MFR (tentative)	K4G41325FC-HC03 (tentative)

LOGIC

CHECK PM AVL

FB CMD mapping Mode H -N15P-GX GDDR5

MDA[63..0] 78



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Title: *VRAM 1,2 (1/4)*

Size: Custom | Document Number: Rayleigh_SLS | Rev: SA

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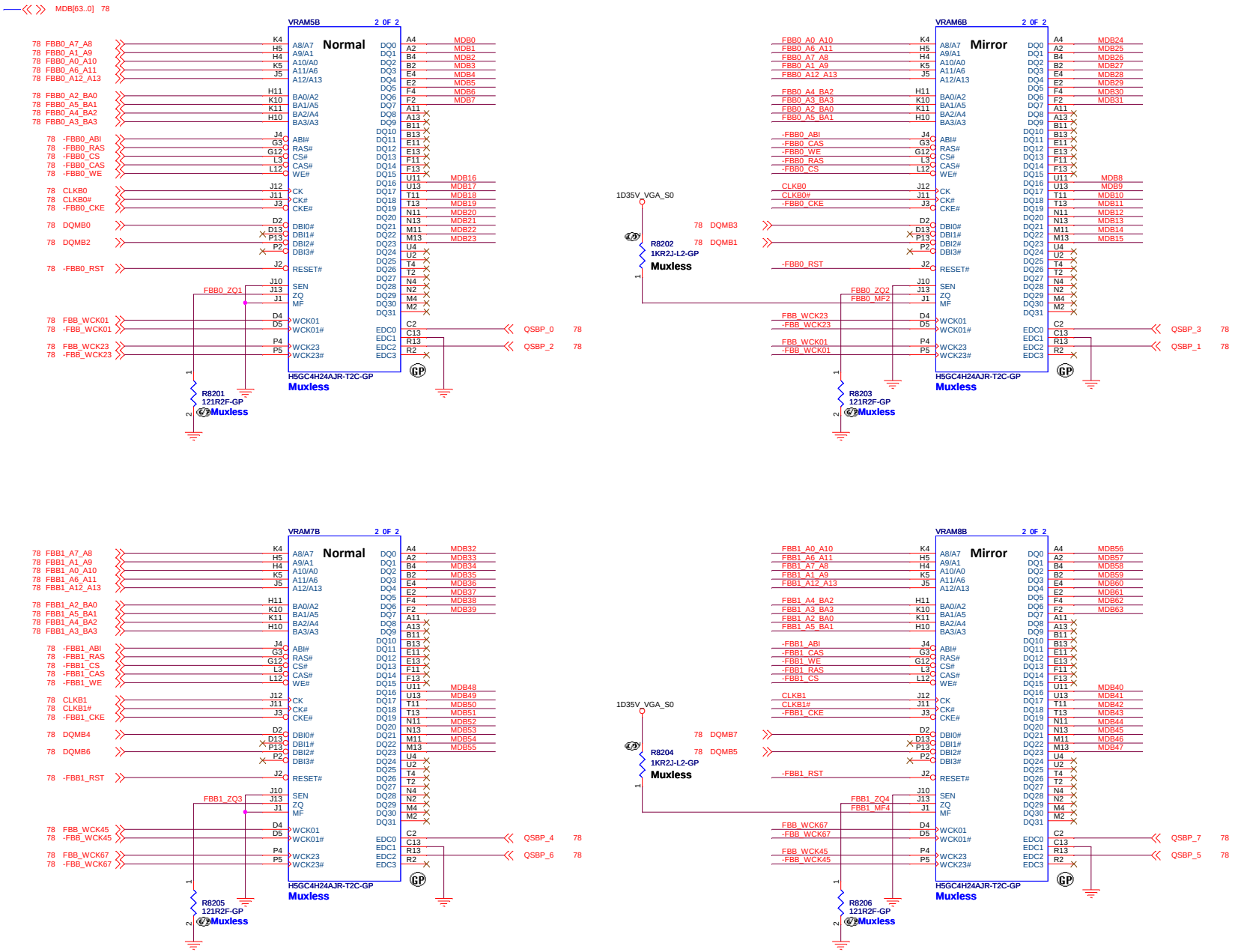

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Title: VRAM 3,4 (2/4)

Size: Custom | Document Number: Rayleigh_SLS | Rev: SA

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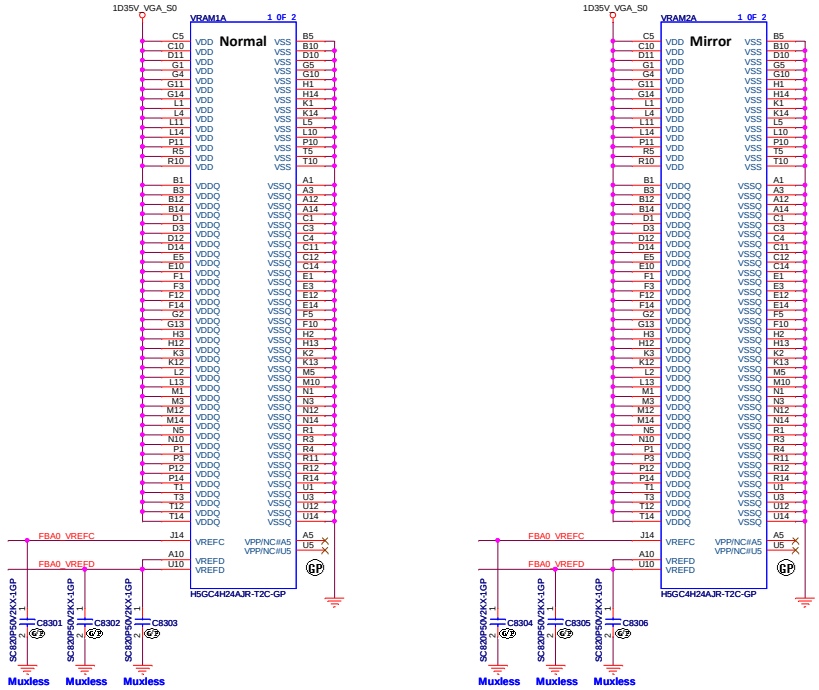

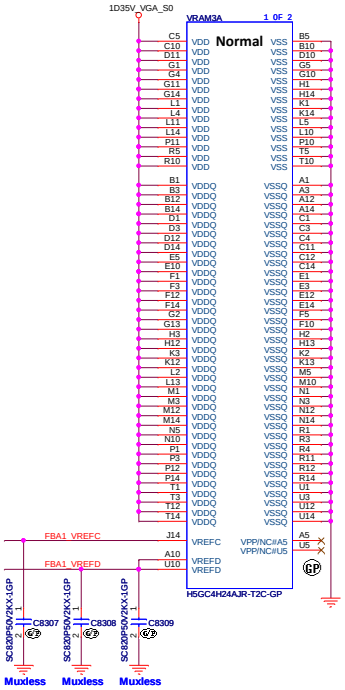

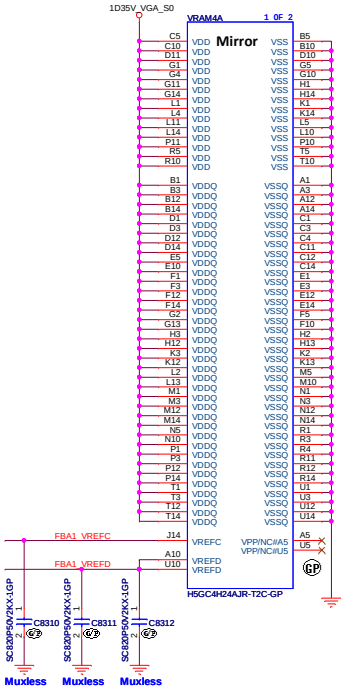

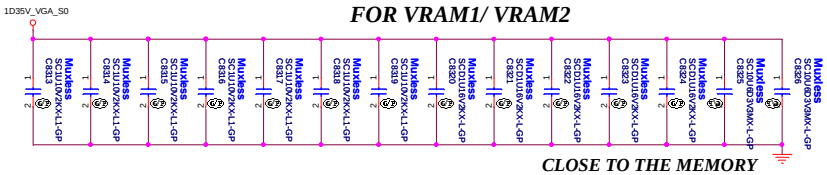

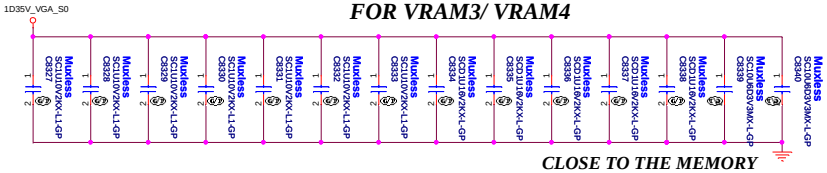

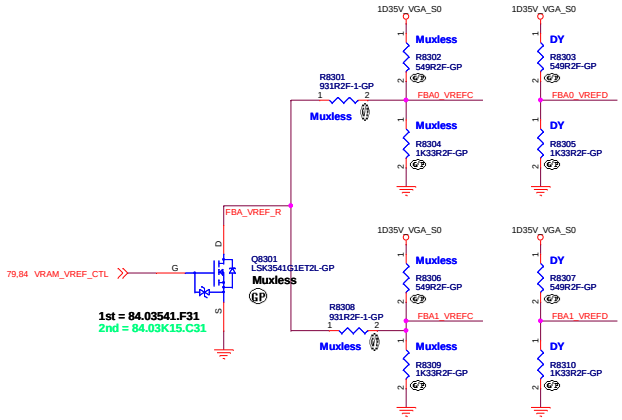

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Title: VRAM 5,6 (3/4)
Size: Custom
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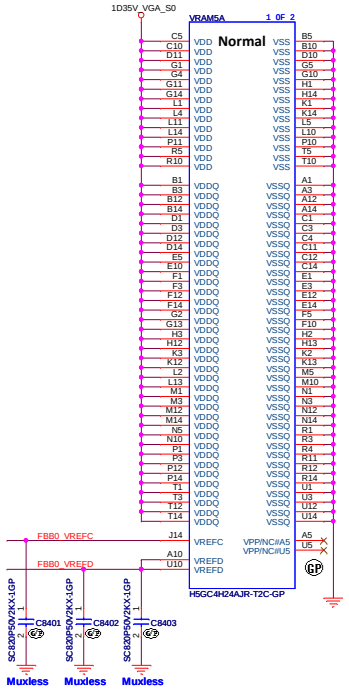

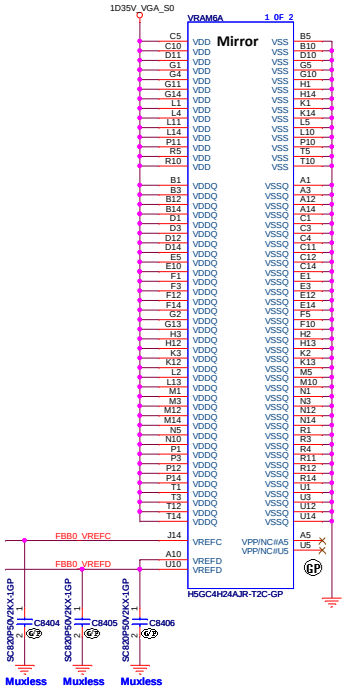

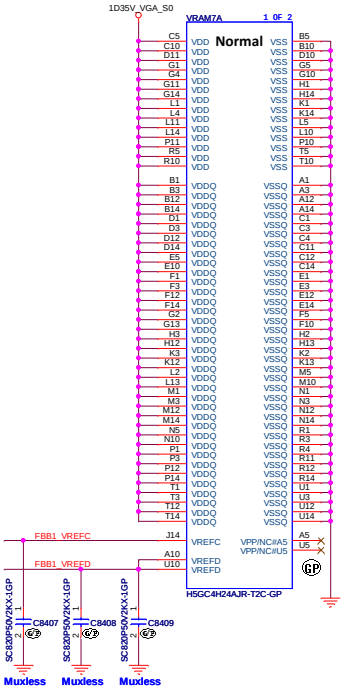

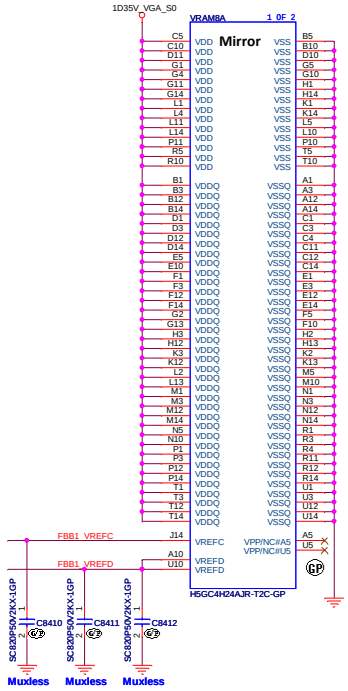

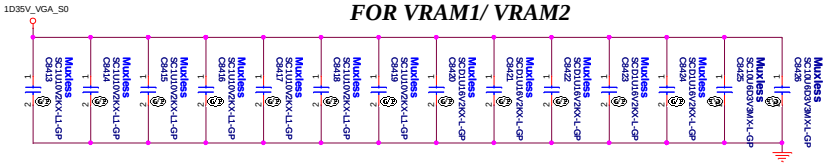

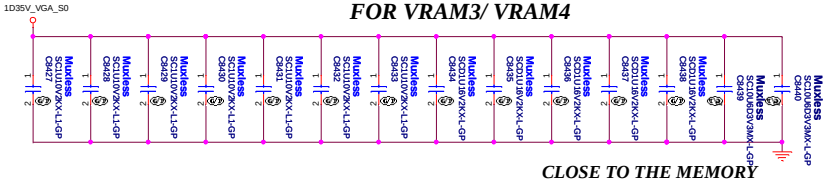

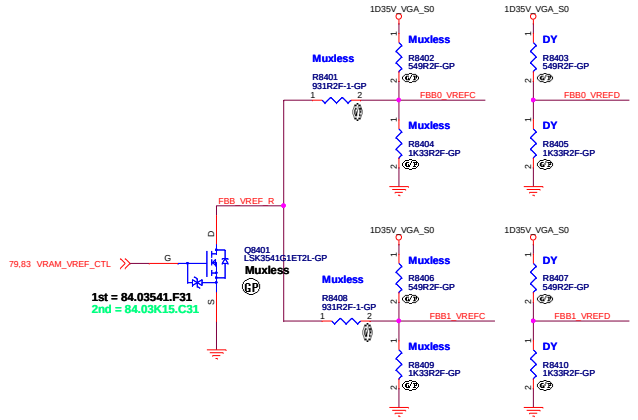

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Title: VGA Power A

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VGA : N16P GX
Config : B
EDP-Continuous : 51.1A
EDP-Peak : 87A

	Config : D	Config : C	Config : B
R1 : PR8514	27K ohm	39K ohm	20K ohm
R2 : PR8513	7.5K ohm	30K ohm	20K ohm
R3 : PR8515	0 ohm	3K ohm	2K ohm
R4 : PR9518	6.2K ohm	24K ohm	18K ohm
R5 : PR8521	1.74K ohm	3K ohm	0 ohm
C : PC8514	5.6nF	1.8nF	2.7nF

ENG 0409 Change

ENG 0420

EMI Request

Mag. 0.36uH 7*7*4
DCR=1.8~2.3mohm
Idc=23A, Isat=32A

470uF/2V, 7.5 x 4.5 x 2.1
ESR=9mohm
Ripple Current=3000 mA

OCP setting
PR8509=10K 'OCP = 124A

1st = 84.03660.037
2nd = 075.06992.0073

1st = 83.00056.Q11
2nd = 83.00056.K11

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Title: VGA Power B

Size: Custom | Document Number: Rayleigh_SLS | Rev: SA

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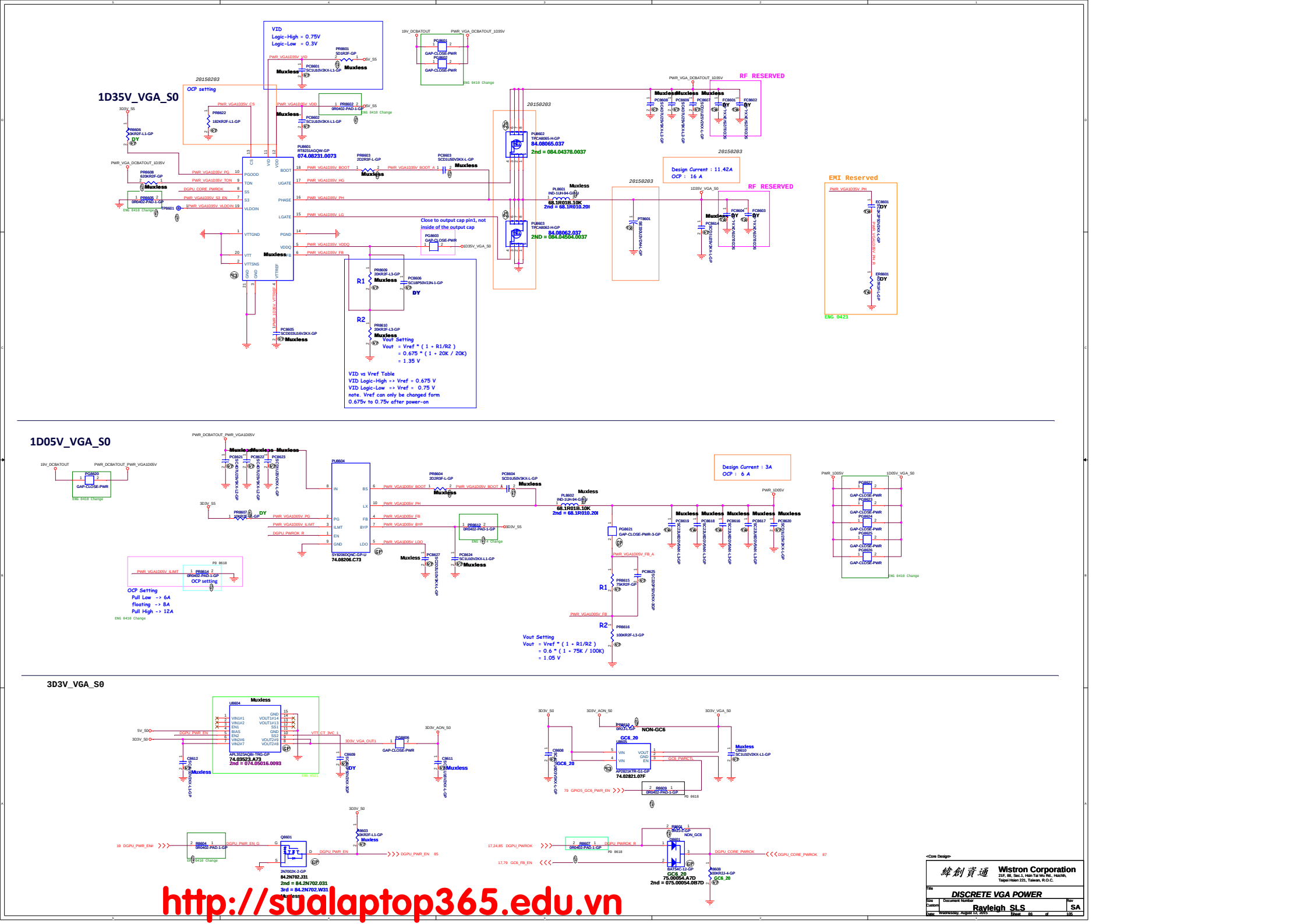
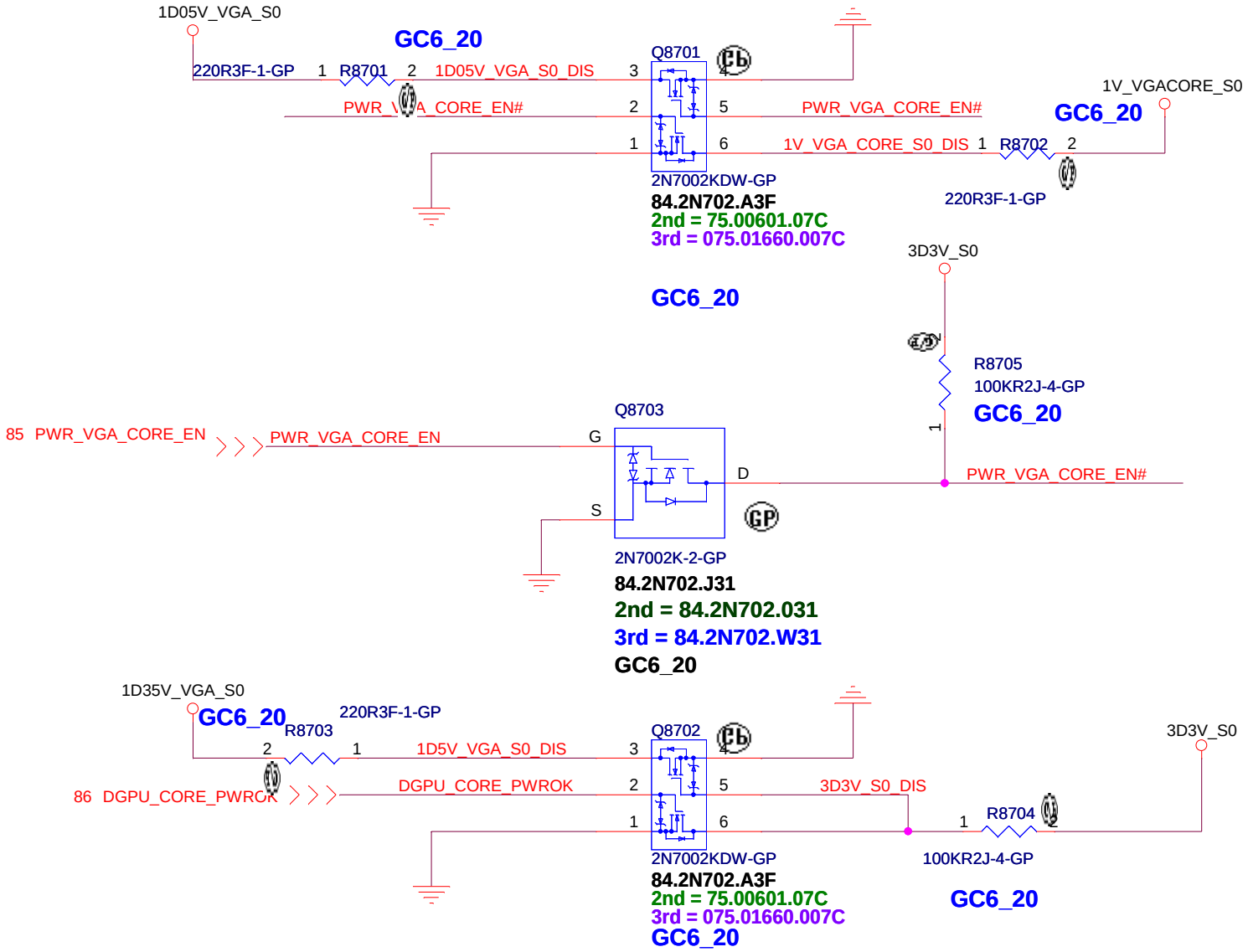

1D35V_VGA_S0
VID
Logic-High = 0.75V
Logic-Low = 0.3V
OCP setting
RF RESERVED
EMI Reserved
Design Current : 11.42A
OCP : 16 A
Close to output cap pin1, not inside of the output cap
Vout Setting
Vout = Vref * (1 + R1/R2)
= 0.675 * (1 + 20K / 20K)
= 1.35 V
VID vs Vref Table
VID Logic-High => Vref = 0.675 V
VID Logic-Low => Vref = 0.75 V
note. Vref can only be changed form 0.675v to 0.75v after power-on
1D05V_VGA_S0
Design Current : 3A
OCP : 6 A
OCP Setting
Pull Low -> 6A
floating -> 8A
Pull High -> 12A
Vout Setting
Vout = Vref * (1 + R1/R2)
= 0.6 * (1 + 75K / 100K)
= 1.05 V
3D3V_VGA_S0
NON-GC6
GC6_20
SGC6_20
Wistron Corporation
DISCRETE VGA POWER
Rayleigh SLS
http://sualaptop365.edu.vn



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Title: ***Discharge***

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A	Rayleigh_SLS	SA

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WLAN

HS6
STFT236B142R128H43-2-GP
Bottom Side
34.4EO02.101

H1 HOLE355X355R111-S1-GP ZZ.00PAD.571
H2 HOLE335R115-GP ZZ.00PAD.D01
34.4LG18.101 for CPU and GPU
Wait ME apply EE symbol
H3 HOLE335R115-GP ZZ.00PAD.D01
H4 HOLE335R115-GP ZZ.00PAD.D01
H5 HOLE335R115-GP ZZ.00PAD.D01

EMI CLIP

SCG5 SCG6 SCG7 SCG8 SCG9 SCG10 SCG11 SCG12
SRING196-GP
34.41L50.001

ENG 0421 Change

手動改34.4LG18.101

HS1 HS2 HS3 HS4 HS5
STF237R128H128-1-GP
34.4LG18.101

EMI Request

19V_DCBATOUT
PD JJ 0625 For EMI
PD JJ 0625 For EMI
EC8901 EC8902 EC8903 EC8904 EC8905 EC8906 EC8907 EC8908 EC8909 EC8910
EC8917 EC8914 EC8912 EC8915 EC8916 EC8911 EC8913
SCD1U25V2KX-GP

Check test point

3D3V_S0 TPAD14-OP-GP TP8901
3D3V_AUX_S5 TPAD14-OP-GP TP8902
3D3V_S5 TPAD14-OP-GP TP8903
5V_S5 TPAD14-OP-GP TP8904
17,24 PM_PWRBTN# TPAD14-OP-GP TP8905
6,17 H_PWRGD TPAD14-OP-GP TP8906
24,40 S5_ENABLE TPAD14-OP-GP TP8907
14,24,31,61,63,68,71,91 PLT_RST# TPAD14-OP-GP TP8908

Test Point放在Dimm Door打開可量測處

EMI Request

1D2V_S3
EC8918 EC8919 EC8920 EC8921 EC8922 EC8923 EC8924 EC8925
SCD1U25V2KX-GP
ENG 0420

EMI Request

1D35V_VGA_S0
EC8932 EC8930 EC8927 EC8931 EC8929 EC8933 EC8926 EC8928 EC8934 EC8935
SCD1U25V2KX-GP
ENG 0420

RJ1

RJ45_1 RJ45_2 RJ45_3 RJ45_4 RJ45_5 RJ45_6 RJ45_7 RJ45_8
AFTP1 AFTP2 AFTP3 AFTP4 AFTP5 AFTP6 AFTP7 AFTP8

SPK1

AMP_SPK1_R_L- AMP_SPK1_R_L+ AUD_SPK1_R_L- AUD_SPK1_R_L+ AMP_SPK1_R_R+ AMP_SPK1_R_R- AUD_SPK1_R_R+
AFTP58 AFTP59 AFTP60 AFTP61 AFTP62 AFTP64 AFTP65 AFTP66

LID_CLOSE#

67 LID_CLOSE#_1 AFTP19
ENG 0421

BTY1

BI BAT_IN# BAT_SCL BAT_SDA 12V_BT+_connector
AFTP67 AFTP68 AFTP69 AFTP70 AFTP71 AFTP72 AFTP73 AFTPN8

KB1 connector

KROW[0..17] KCOL[0..7]
KBC_PWRBTN#
AFTP92 AFTP93 AFTP94 AFTP95 AFTP96 AFTP97 AFTP98 AFTP99 AFTPA0 AFTPA1 AFTPA2 AFTPA3 AFTPA4 AFTPA5 AFTPA6 AFTPA7 AFTPA8 AFTPA9 AFTPB0 AFTPB1 AFTPB2 AFTPB3 AFTPB4 AFTPB5 AFTPB6 AFTPB7 AFTPB8 AFTPB9 AFTPC0

FAN1 connector

FAN1_PWM FAN1_S0 FAN_TACH1_C
AFTPE8 AFTPFO2 AFTPE9 AFTPF0

LB1

LB_PWM_LED1 LB_PWM_LED2 5V_S5
AFTP15 AFTP16 AFTP17

FAN2 connector

FAN2_PWM 5V_FAN2_S0 FAN_TACH2_C
AFTPF1 AFTPEO2 AFTPF2 AFTPF3

HDD1

SATA_TX_HDD_P2 SATA_TX_HDD_N2 SATA_RX_HDD_N2 SATA_RX_HDD_P2 5V_S0
AFTP74 AFTP75 AFTP76 AFTP77 AFTP78

USB 1 CONNECTOR

USB30_RX_CON_N1 USB30_RX_CON_P1 USB30_TX_CON_N1 USB30_TX_CON_P1 USB_CON_PN1 USB_CON_PP1 5V_USB30_CHARGER
AFTP22 AFTP23 AFTP24 AFTP25 AFTP26 AFTP27 AFTP28 AFTP29

KB_BL1

KB_BL_DET_R KB_LED_PWM_D 5V_S0
AFTP80 AFTP81 AFTP82 AFTP83

USB 2 CONNECTOR

USB30_RX_CON_N2 USB30_RX_CON_P2 USB30_TX_CON_N2 USB30_TX_CON_P2 USB_CON_PN2 USB_CON_PP2 5V_USB30
AFTP30 AFTPN9 AFTP32 AFTP33 AFTP34 AFTP35 AFTP36 AFTP37

TPAD1

EC_TP_CLK_C EC_TP_DATA_C I2C1_DATA_TP I2C1_CLK_TP TP_INT_R TP_LID_CLOSE# 3D3V_TP_S3
AFTP84 AFTP85 AFTP86 AFTP87 AFTP88 AFTP89 AFTP90 AFTP91

CAM1

USB3_URXN0 USB3_URXP0 CCD_UTXN0 CCD_UTXP0 FW_GPIO 5V_CAMERA_S0 DMIC_DATA_CON_R DMIC_CLK_CON 3D3V_CAMERA_S0
AFTPD5 AFTPD6 AFTPD7 AFTPD8 AFTPD9 AFTPE0 AFTPE1 AFTP9 AFTP14 AFTP11 AFTP12
ENG 0422

eDP connector

eDP_HPD_CON eDP_AUX_CON_P eDP_AUX_CON_N eDP_TX_CON_P0 eDP_TX_CON_N0 eDP_TX_CON_P1 eDP_TX_CON_N1 eDP_TX_CON_P2 eDP_TX_CON_N2 eDP_TX_CON_P3 eDP_TX_CON_N3 TOUCH_DET#_R TOUCH_S_RST#_R USB_CON_PN8 USB_CON_PP8 eDP_BLEN_CON eDP_BLCTRL_CON 19V_DCBATOUT_LCD TS_S0 TOUCH_INT# 3D3V_LCDVDD_S0
AFTPF4 AFTPF5 AFTPF6 AFTPF7 AFTPF8 AFTPF9 AFTPG0 AFTPG1 AFTPG2 AFTPG3 AFTPG4 AFTPG5 AFTPG6 AFTPG7 AFTPG8 AFTPG9 AFTPH0 AFTPH3 AFTPO2 AFTPH1 AFTPH7 AFTPH8 AFTP79

DCIN1 connector

19V_AD_JK
AFTPE4 AFTPE5 AFTPE6 AFTPE7

WLAN1 connector

WIGIG_CLK_CPU# WIGIG_CLK_CPU PCIE_RX_PCH_N2 PCIE_RX_PCH_P2 PCIE_TX_CON_N2 PCIE_TX_CON_P2 PCIE_WAKE#_WLAN WLAN_CLKREQ_CPU# WLAN_CLK_CPU# WLAN_CLK_CPU PCIE_RX_PCH_N3 PCIE_RX_PCH_P3 PCIE_TX_CON_N3 PCIE_TX_CON_P3 USB_PCH_R_PN7 USB_PCH_R_PP7 PCIE_WAKE# WIGIG_CON WIGIG_CLKREQ_CPU# WIGIG_RST# WIFI_RF_EN_CON BLUETOOTH_EN WLAN_RST# ES1_RXD_R ES1_TXD_R 3D3V_S0
AFTPK5 AFTPK6 AFTPK7 AFTPK8 AFTPK9 AFTPL0 AFTPL1 AFTPL2 AFTPL3 AFTPL4 AFTPL5 AFTPL6 AFTPL7 AFTPL8 AFTPL9 AFTPM0 AFTPM1 AFTPM2 AFTPM3 AFTPM4 AFTPM5 AFTPM6 AFTPM8 AFTPM9 AFTPN0

SMB1

STDBY_LED PWRLED CHARGE_LED DC_BATFULL USB_CON_PN10 USB_CON_PP10 USB_CON_PN6 USB_CON_PP6 RING2 AUD_HP1_JACK_L2 AUD_HP1_JACK_R2 SELEEVE 3D3V_S0 5V_USB AUD_HP1_JD#
AFTPC6 AFTPC9 AFTPC10 AFTP10 AFTPC1 AFTPC2 AFTPC3 AFTPC4 AFTPC5 AFTPC7 AFTPC8 AFTPD0 AFTPD1 AFTPD2 AFTPD3 AFTPD4 AFTP13

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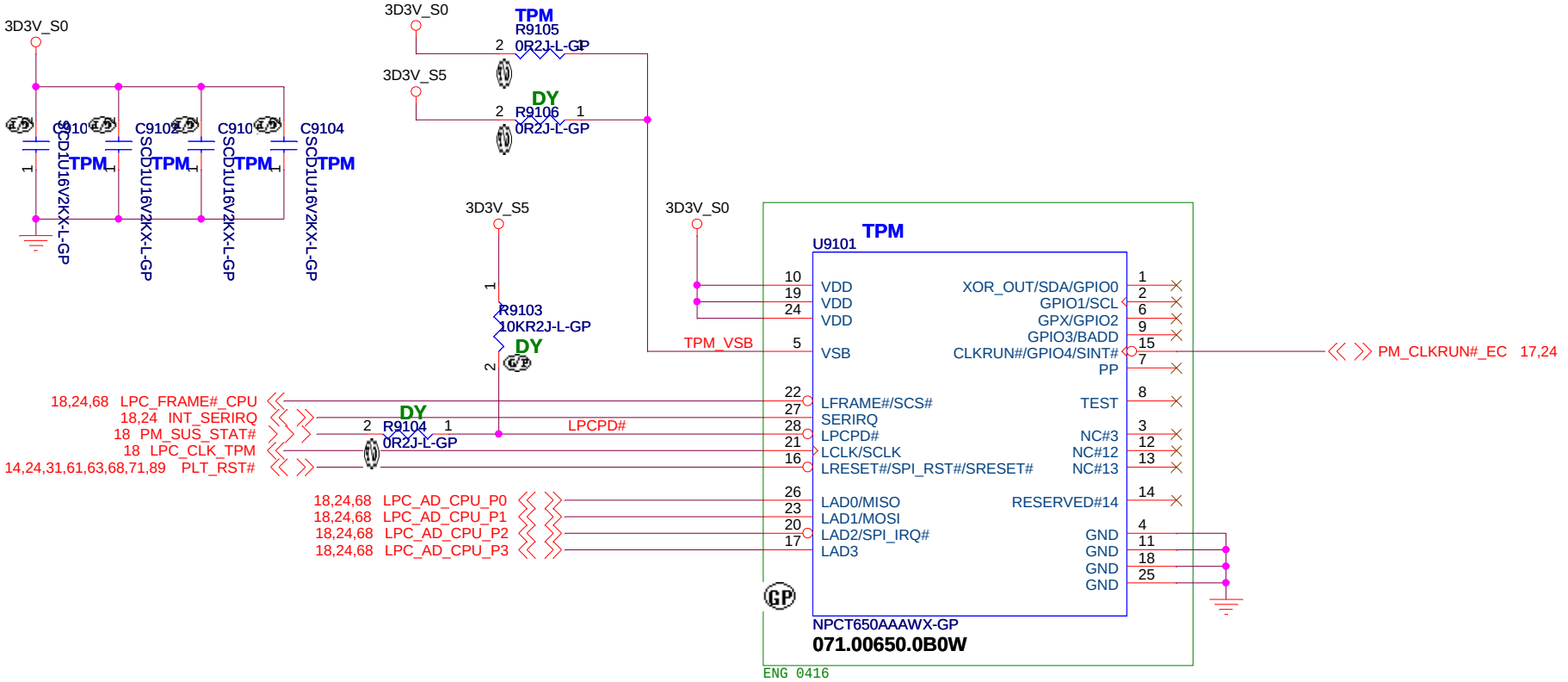
Title: UNUSED PARTS/EMI Capacitors
Size: A2 | Document Number: Rayleigh_SLS | Rev: SA
Date: Wednesday, August 12, 2015 | Sheet 89 of 105



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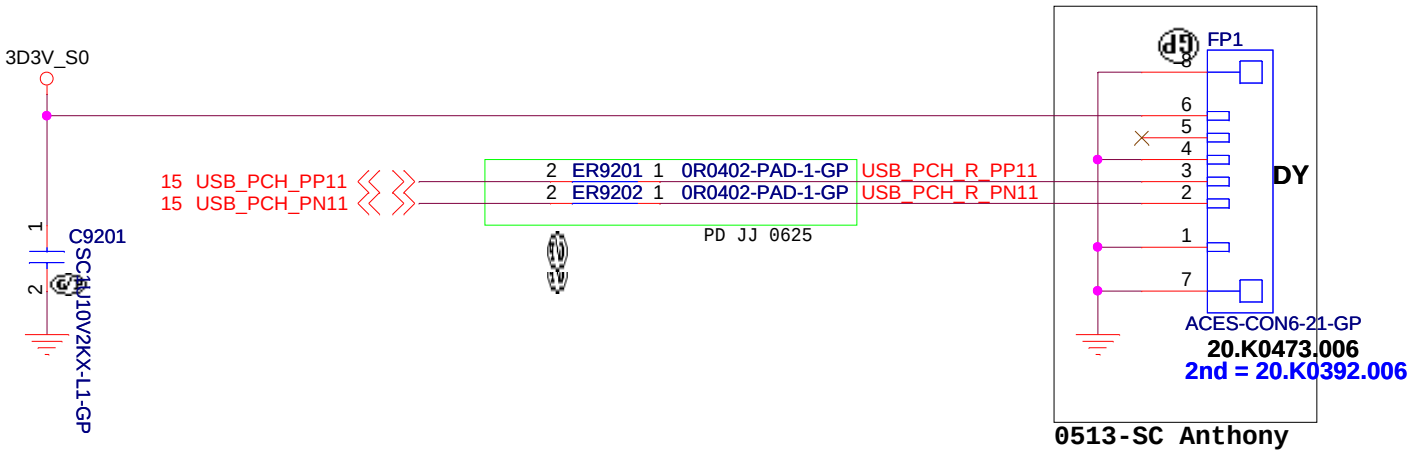
Title: ***TPM/NPCT650***

Size	Document Number	Rev
A4	Rayleigh_SLS	SA

Date: Wednesday, August 12, 2015 Sheet 91 of 105



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Title: ***Finger Print***

Size	Document Number	Rev
A	Rayleigh_SLS	SA

Date: Monday, September 07, 2015 Sheet 92 of 105

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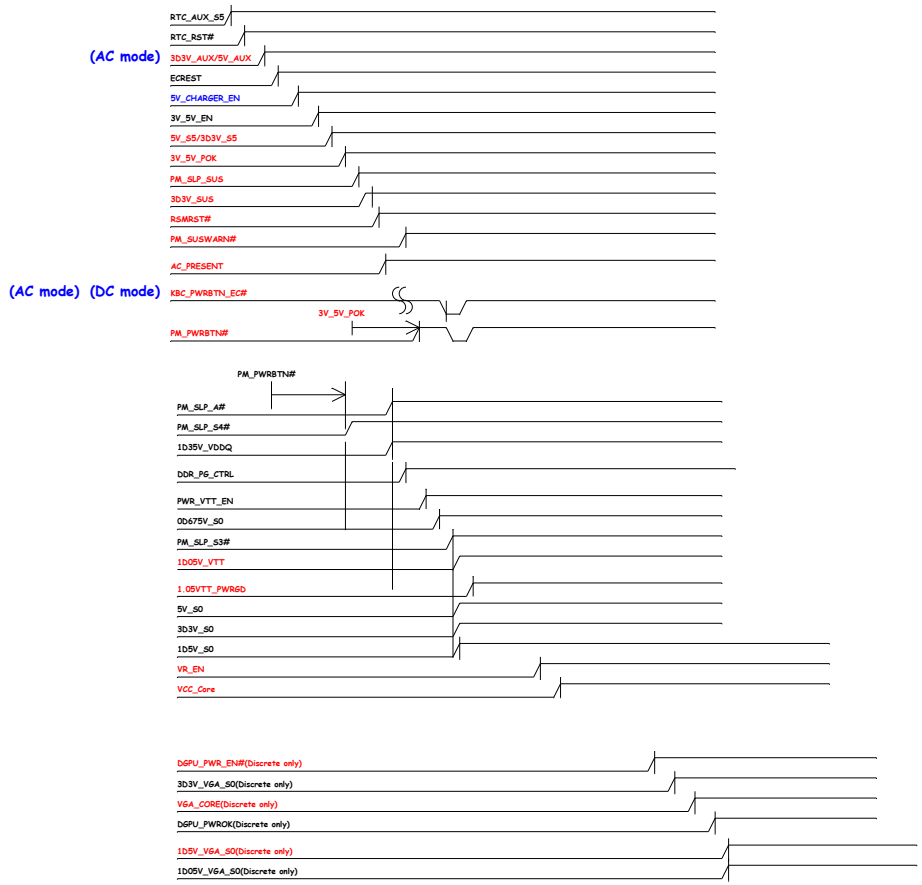
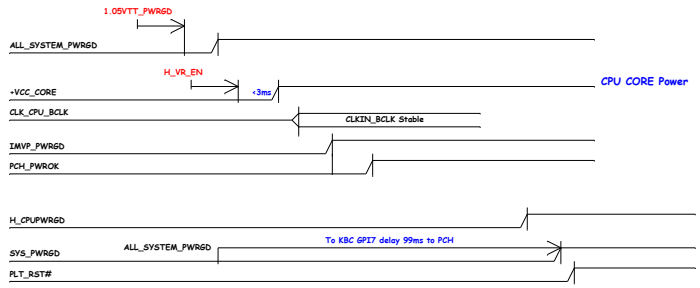
Title: ***CPU_XDP***

Size	Document Number	Rev
A	Rayleigh_SLS	SA

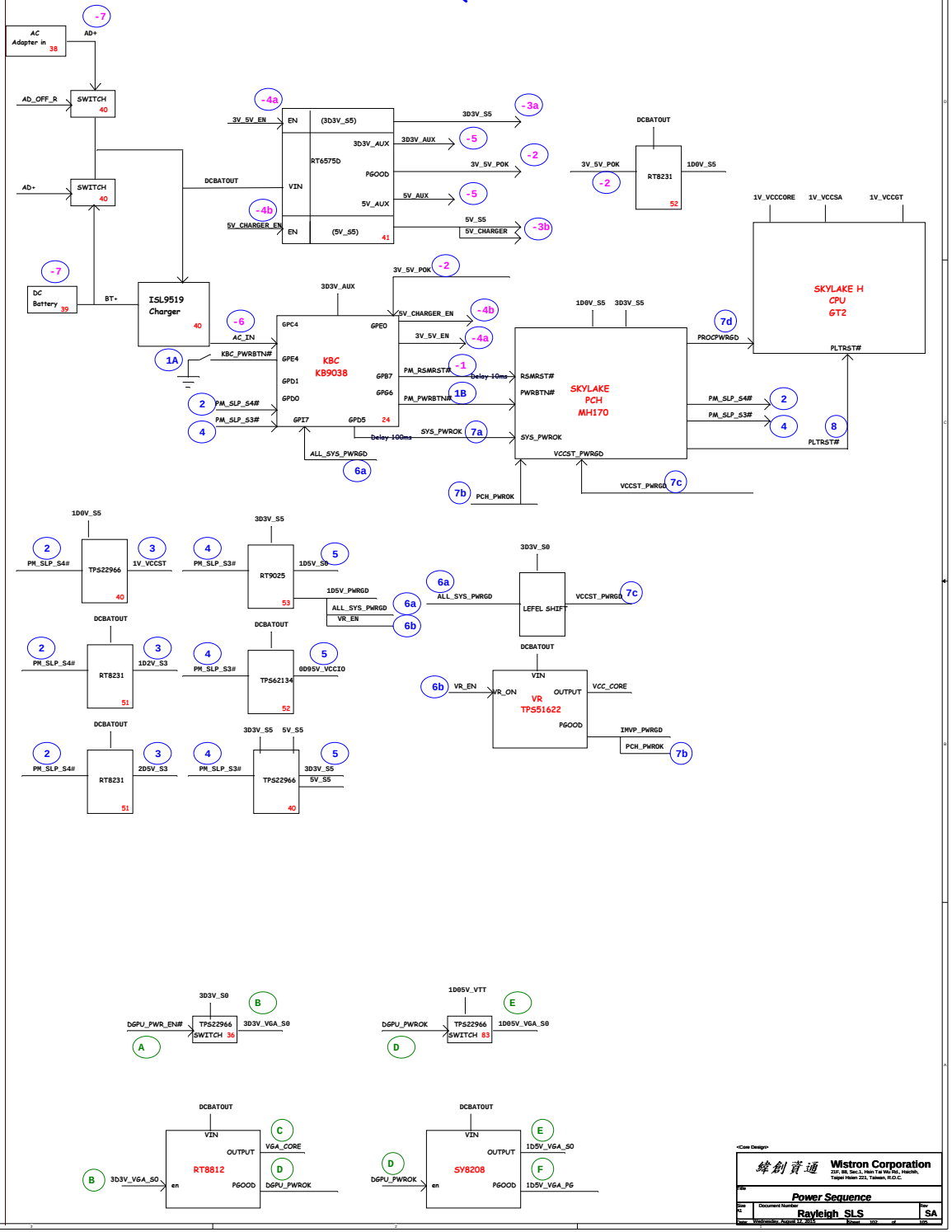
Date: Wednesday, August 12, 2015 Sheet 99 of 105

Intel-Power Up Sequence





SKYLAKE H POWER UP SEQUENCE DIAGRAM



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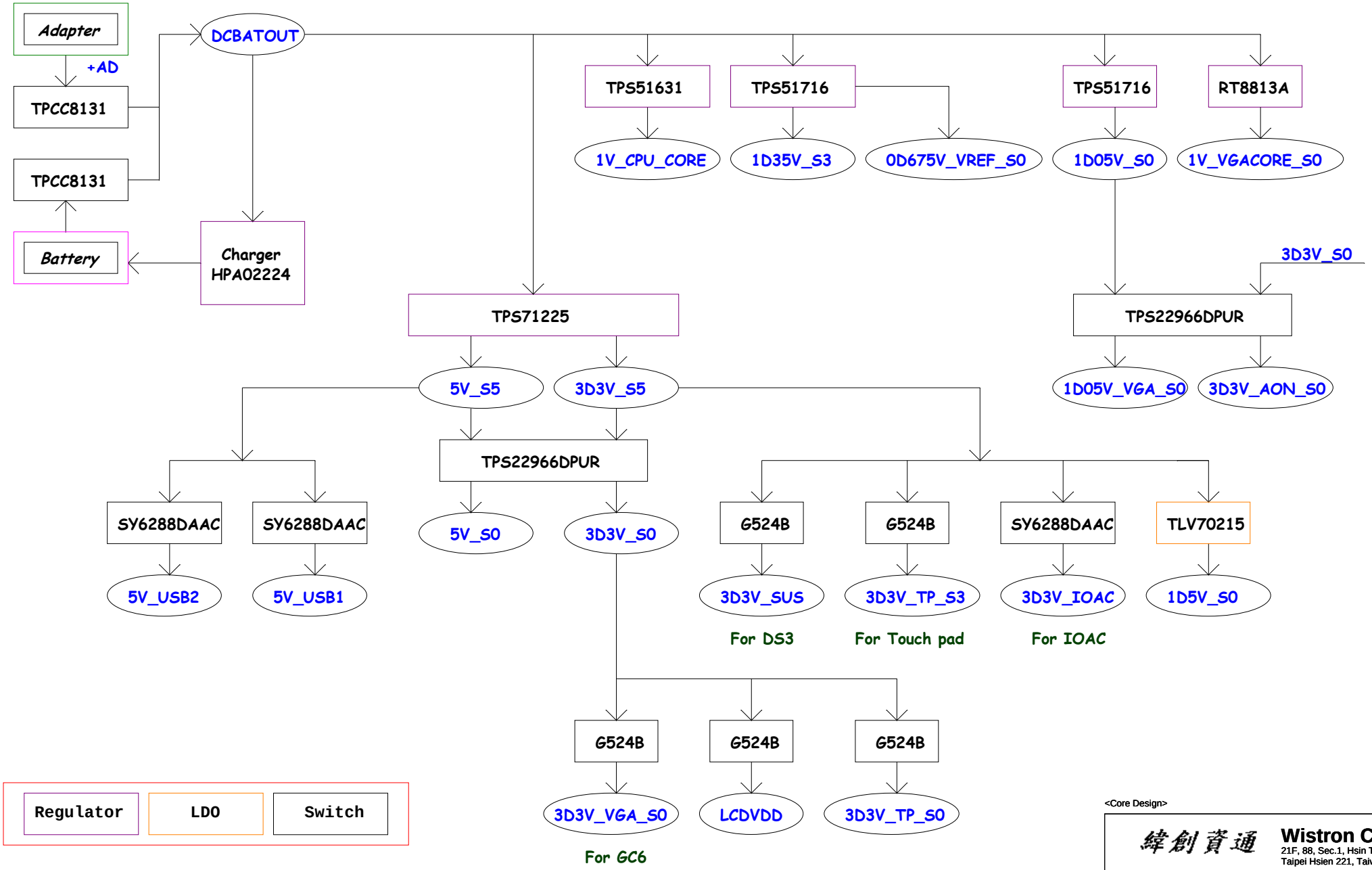
Power Sequence

Size: A3 | Document Number: Rayleigh_SLS | Rev: SA

Date: Wednesday, August 19, 2015 | Sheet 102 of 105



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Title: Power Block Diagram

Size	Document Number	Rev
Custom	Rayleigh_SLS	SA

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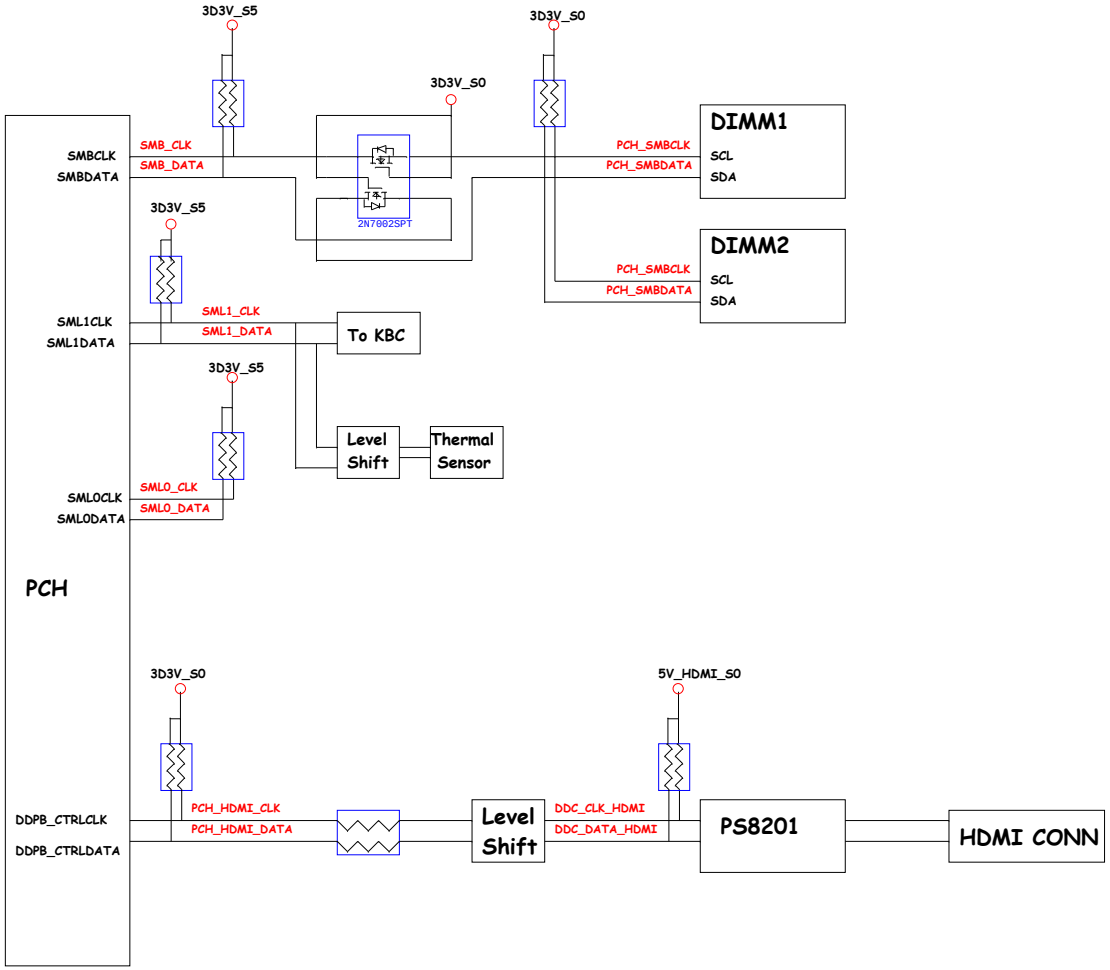
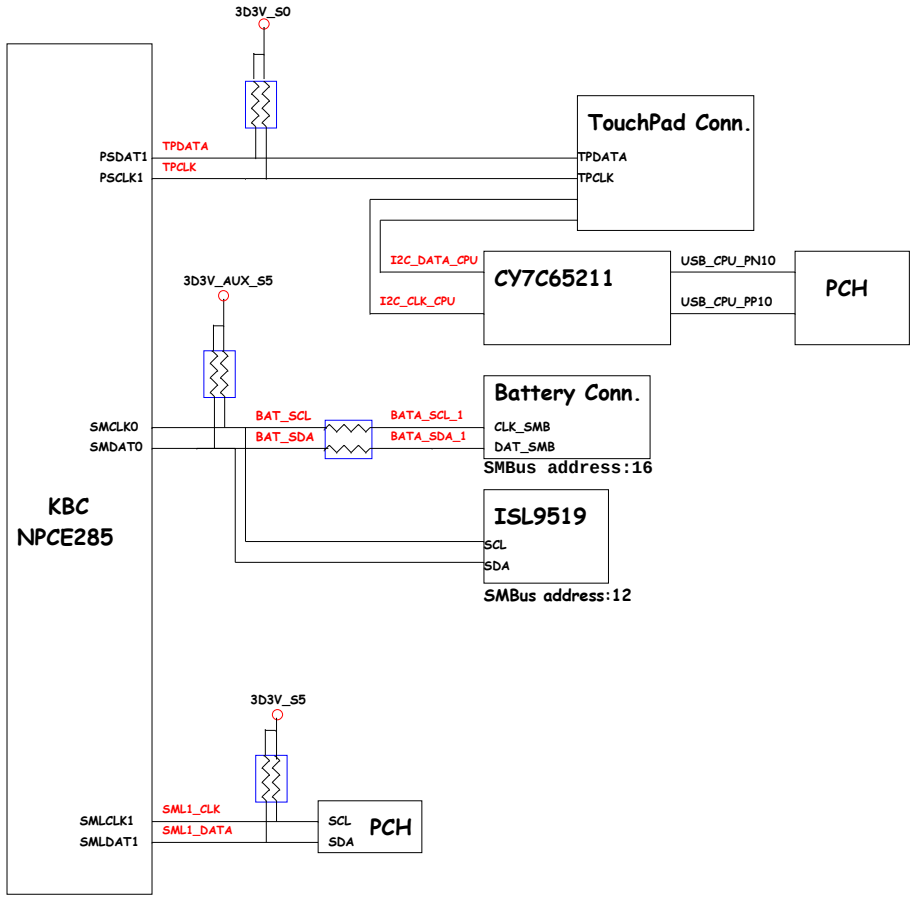
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS BLOCK DIAGRAM

Size	Document Number	Rev
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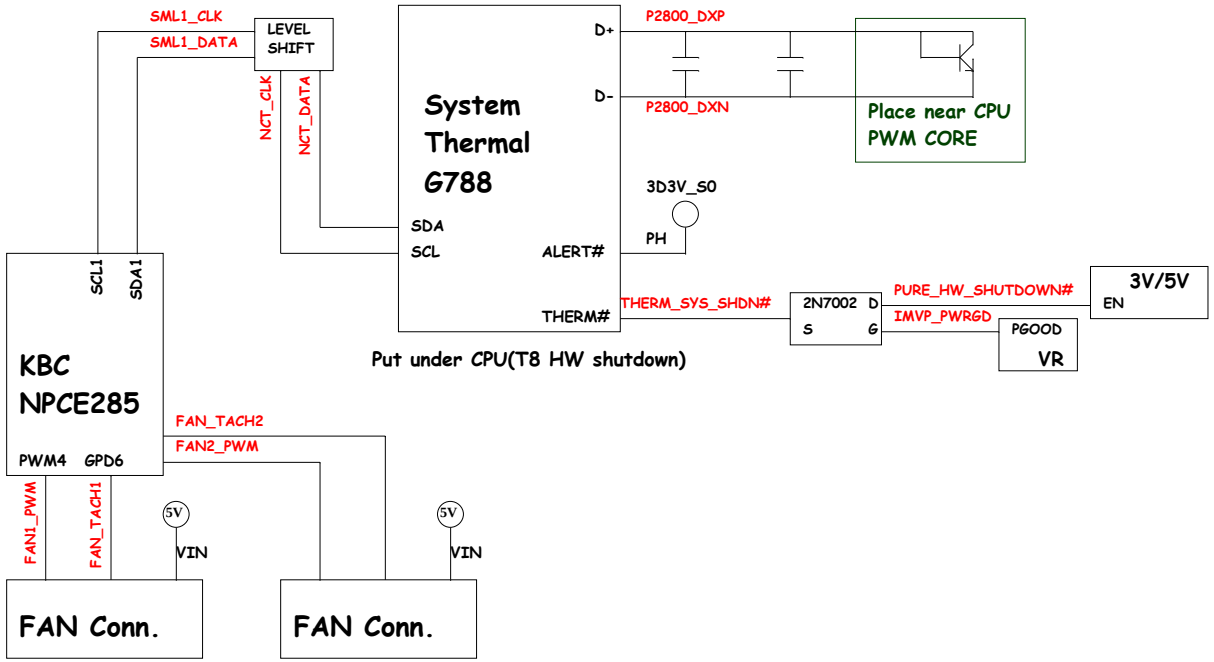
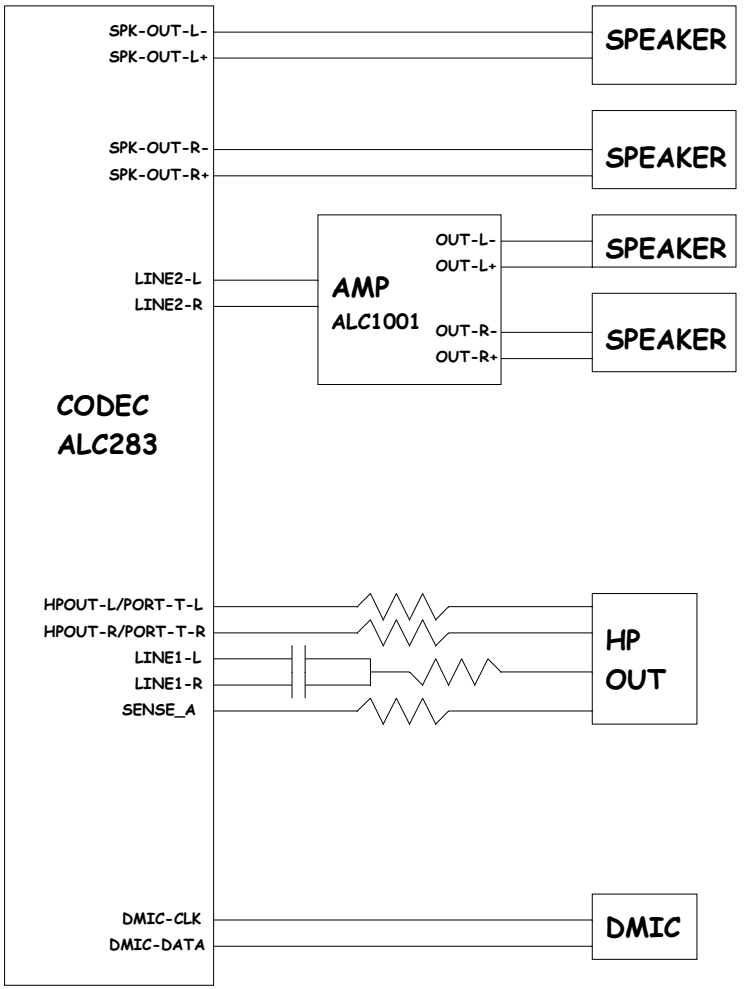
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal /AUDIO Block Diagram		
Size: Custom	Document Number: EA40_HU ULT	Rev: SA
Date: Wednesday, August 12, 2015	Sheet 105 of 105	