Compal Confidential

MB Schematic Document

EH50F/EH70F/EH51F/EH5VF/EH53F/EH73F

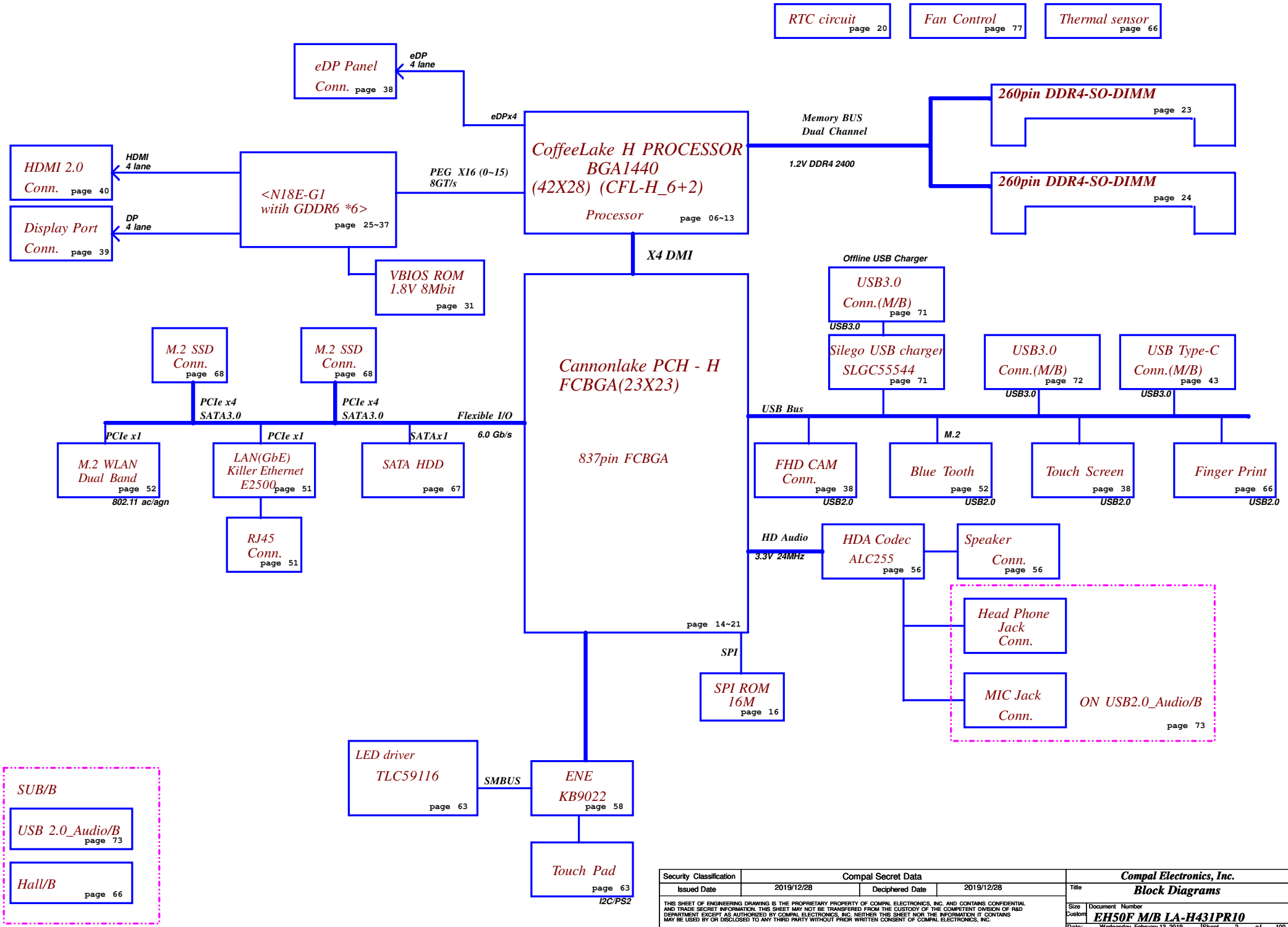
LA-H431P

Rev:1.0

2018.01.22

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.		
Title: Cover Sheet		
Size: Custom	Document Number: EH50F M/B LA-H431PR10	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 1 of 100	



Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.			
Title	Block Diagrams		
Size	Document Number		Rev
Custom	EH50F M/B LA-H431PR10		1.0
Date:	Wednesday, February 13, 2019	Sheet	2 of 100

Board ID Table for AD channel

Vcc	3.3V
Ra	100K +/- 1%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)				
I2C_1 (+3VS)	TM-P3393-003 (Touch Pad)			
	SA577C-12A0 (Touch Pad)			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
PCH_SML1CLK EC_SMB_CK2 (+3VALW)	N18E-G0/G1 (VGA)	0x9E		
	Thermal Sensor (NCT7718W)	1001_100xb	1001_1001b	1001_1000b
	PCH	0x90		
EC_SMB_CK1 (+3VLP)	ISL88739 (Charger IC)	0x12		
	BATTERY PACK	0x16		
EC_SMB_CK3 (+3VALW)	LED driver	0xC0		

BOM Structure Table

BOM Option Table	
Item	BOM Structure
Unpop	@
Connector	CONN@
i5 CPU	I5@
i7 CPU	I7@
PCH	PCH@
CMC	CMC@
dGPU circuit	VGA@
VGA GC6 3.0	NFGC6@
VGA GC63.0+FGPC6	FGC6@
Intel CNVi	CNVI@
USB charger	CHG@
EMI/ESD requirement	EMC@
EMI/ESD require reserve	XEMC@
With TPM	TPM@
Without TPM	NTPM@
OVRM with uPI	uPI@
OVRM with ON	ON@
With SATA redriver	SATARD@
Without SATA redriver	NORD@
Thermal sensor	TMS@
With FingerPrint	FP@
FingerPrint ESD	FPESD@
With G-SYNC panel	GSYNC@
Without G-SYNC panel	NGSYNC@
RF requirement reserve	@RF@
for SW debug board	UART@
UMA sku	UMA@
HDMI cost	45@
VRAM BOM	X76@

Power State

SIGNAL / STATE	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Voltage Rails

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+3VALW_PCH_PRIM	+3VALW power for PCH power rails	ON	ON	ON	ON*
+3VALW_SPI	+3VALW_PRIM supply for the SPI IO	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.95VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+VGA_CORE	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

BOARD ID Table

Board ID	PCB Revision	Board ID	PCB Revision
0	2050 Rev0.1	10	
1	2050 Rev0.2	11	
2	2050 Rev0.3	12	
3	2050 Rev1.0	13	
4	2060 Rev0.1	14	
5	2060 Rev0.2	15	
6	2060 Rev0.3	16	
7	2060 Rev1.0	17	
8		18	
9		19	

43 level BOM table

43 Level	Description	BOM Structure
431AH3BOL01	SMT MB AH431 EH50F N18EG1Q 6G QP89 HDMI	CHG@/EMC@/CMC@/CNVI@/FGC6@/NGSYNC@/PCH@/NORD@/TMS@/TPM@/UPI@/VGA@/i5@/FP@/FPESD@

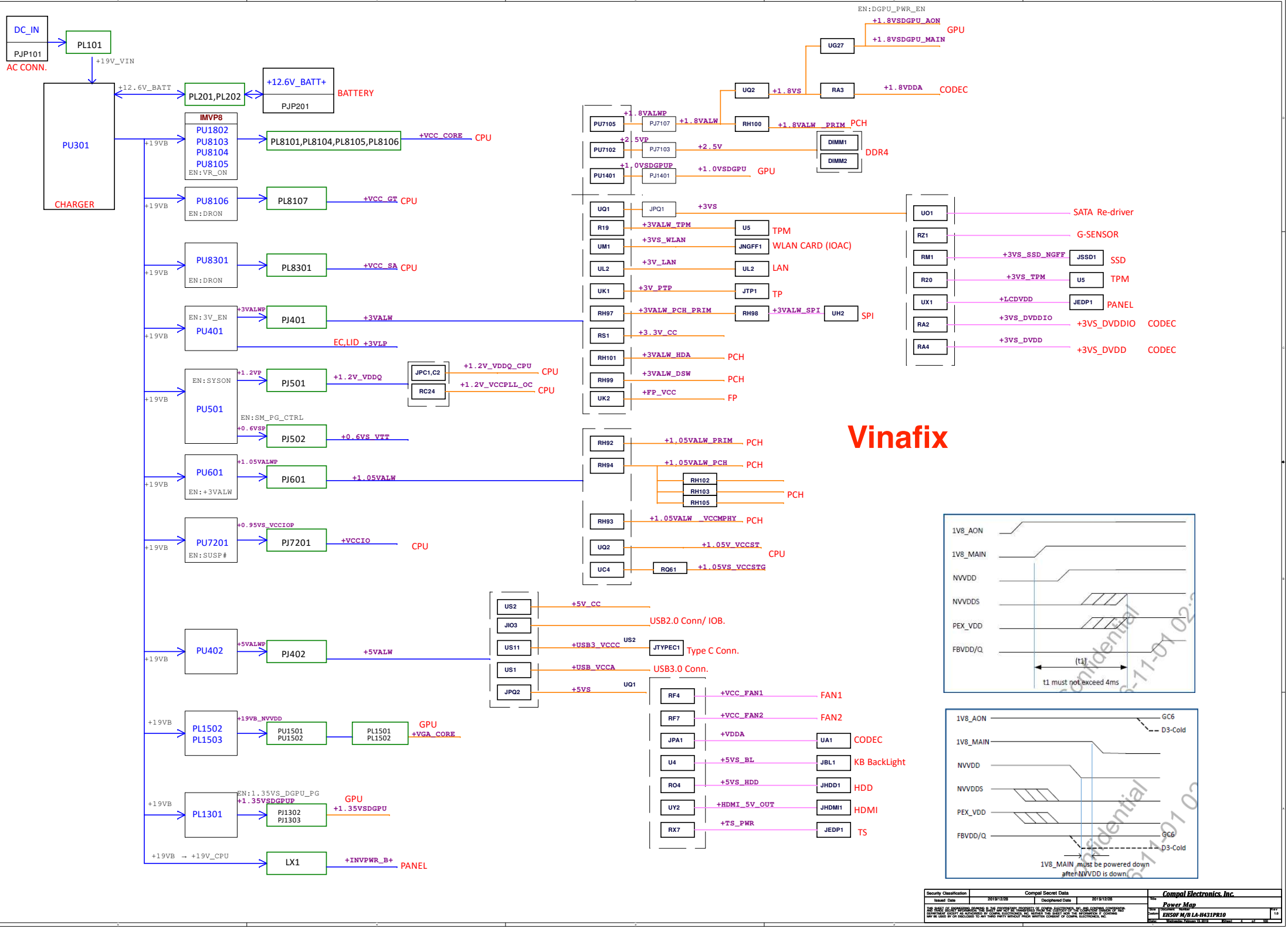
Security Classification	Compal Secret Data	
Issued Date	2019/12/28	Deciphered Date 2019/12/28

Compal Electronics, Inc.

Title: Notes List

Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 3 of 100


DC_IN
PJP101
AC CONN.
PL101
+19V_VIN
PU301
CHARGER
+12.6V_BATT
PL201,PL202
+12.6V_BATT+
PJP201
BATTERY
IMVP8
PU1802
PU8103
PU8104
PU8105
EN:VR_ON
PL8101,PL8104,PL8105,PL8106
+VCC_CORE
CPU
PU8106
EN:DRON
PL8107
+VCC_GT
CPU
PU8301
EN:DRON
PL8301
+VCC_SA
CPU
EN:3V_EN
PU401
PJ401
+3VALW
EC,LID +3VLP
EN:SYSON
PU501
PJ501
+1.2V_VDDQ
JPC1,C2
RC24
+1.2V_VDDQ_CPU
+1.2V_VCCPLL_OC
CPU
EN:SM_PG_CTRL
PJ502
+0.6VS_VTT
PU601
EN:+3VALW
PJ601
+1.05VALW
PU7201
EN:SUSP#
PJ7201
+VCCIO
CPU
PU402
PJ402
+5VALW
PL1502
PL1503
PU1501
PU1502
PL1501
PL1502
GPU
+VGA_CORE
EN:1.35VS_DGPU_PG
PL1301
PJ1302
PJ1303
+1.35VSDGPUP
+1.35VSDGPU
GPU
+19VB → +19V_CPU
LX1
+INVPWR_B+
PANEL
EN:DGPU_PWR_EN
UG27
+1.8VSDGPU_AON
+1.8VSDGPU_MAIN
GPU
UQ2
+1.8VS
RA3
+1.8VDDA
CODEC
PU7105
PJ7107
+1.8VALWP
+1.8VALW
RH100
+1.8VALW_PRIM
PCH
PU7102
PJ7103
+2.5VP
+2.5V
DIMM1
DIMM2
DDR4
PU1401
PJ1401
+1.0VSDGPUP
+1.0VSDGPU
GPU
UQ1
JPQ1
+3VS
UO1
SATA Re-driver
R19
+3VALW_TPM
U5
TPM
RZ1
G-SENSOR
UM1
+3VS_WLAN
JNGFF1
WLAN CARD (IOAC)
RM1
+3VS_SSD_NGFF
JSSD1
SSD
UL2
+3V_LAN
UL2
LAN
R20
+3VS_TPM
U5
TPM
UK1
+3V_PTP
JTP1
TP
UX1
+LCDVDD
JEDP1
PANEL
RH97
+3VALW_PCH_PRIM
RH98
+3VALW_SPI
UH2
SPI
RA2
+3VS_DVDDIO
+3VS_DVDDIO
CODEC
RS1
+3.3V_CC
RA4
+3VS_DVDD
+3VS_DVDD
CODEC
RH101
+3VALW_HDA
PCH
RH99
+3VALW_DSW
PCH
UK2
+FP_VCC
FP
Vinafix
RH92
+1.05VALW_PRIM
PCH
RH94
+1.05VALW_PCH
PCH
RH102
RH103
RH105
PCH
RH93
+1.05VALW_VCCMPHY
PCH
UQ2
+1.05V_VCCST
CPU
UC4
RQ61
+1.05VS_VCCSTG
US2
JIO3
US11
US1
JPQ2
+5V_CC
USB2.0 Conn/ IOB.
+USB3_VCCC
US2
JTYPEC1
Type C Conn.
+USB_VCCA
USB3.0 Conn.
+5VS
UQ1
RF4
RF7
JPA1
U4
RO4
UY2
RX7
+VCC_FAN1
FAN1
+VCC_FAN2
FAN2
+VDDA
UA1
CODEC
+5VS_BL
JBL1
KB BackLight
+5VS_HDD
JHDD1
HDD
+HDMI_5V_OUT
JHDMI1
HDMI
+TS_PWR
JEDP1
TS
1V8_AON
1V8_MAIN
NVVDD
NVVDDS
PEX_VDD
FBVDD/Q
(t1)
t1 must not exceed 4ms
GC6
D3-Cold
1V8_MAIN must be powered down after NVVDD is down
Security Classification
Compal Secret Data
Issued Date
2015/12/28
Deciphered Date
2015/12/28
Compal Electronics, Inc.
Power Map
Document Number
EH50F M/B LA-H431PR10
Rev
1.0
Wednesday, February 19, 2016
Sheet
4
of
50

EH50F_EVT Power Sequence
BIOS : 0.02T3
AC mode

Power On

Plug in

S3

S3 Resume

Power Off

Compal Electronics, Inc.

Title: Power Sequence

Size	Document Number	Rev
C	EH50F M/B LA-H431PR10	1.0

Date: Wednesday, February 13, 2019 | Sheet 5 of 100

Coffee Lake-H CPU SKU

UC1

CFL-H_BGA1440
S IC CL8068403373522 SR3Z0 U0 2.3G ABO!
SA0000BPJ40
i5@

UC1

CFL-H_BGA1440
S IC CL8068403359524 SR3YY U0 2.2G ABO!
SA0000BPZ40
i7@

Cannon Lake PCH SKU

UH1

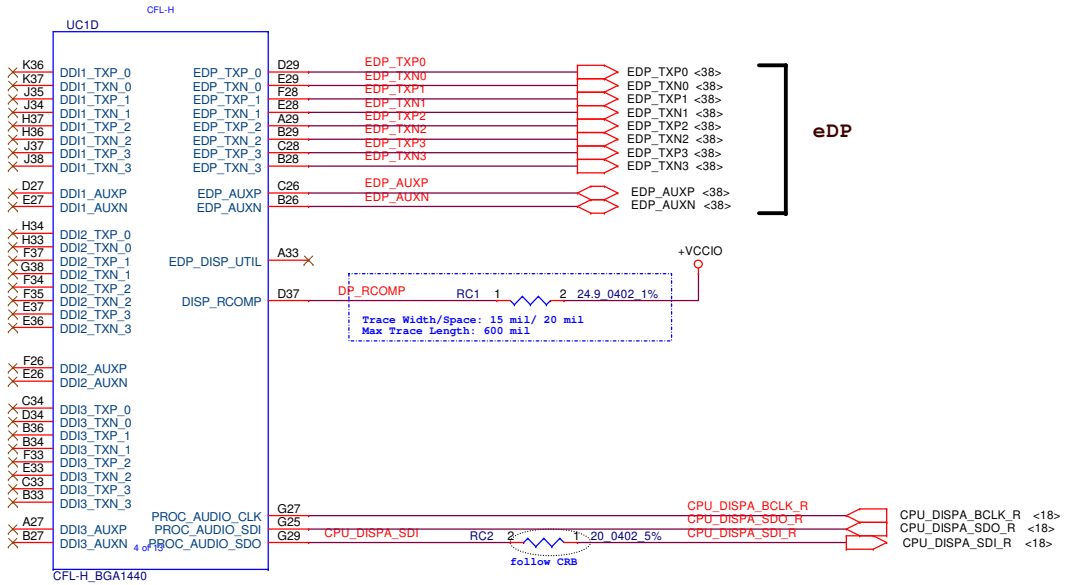
CFL-H_BGA1440
S IC FH82HM370 SR40B B0 BGA 874P PCH-H ABO!
SA0000BVP10
PCH@

NV N18E-G1

UG9

VGA@

S IC N18E-G1-KD-A1 QS FCBGA 2228 GPU
SA0000CFC00



Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

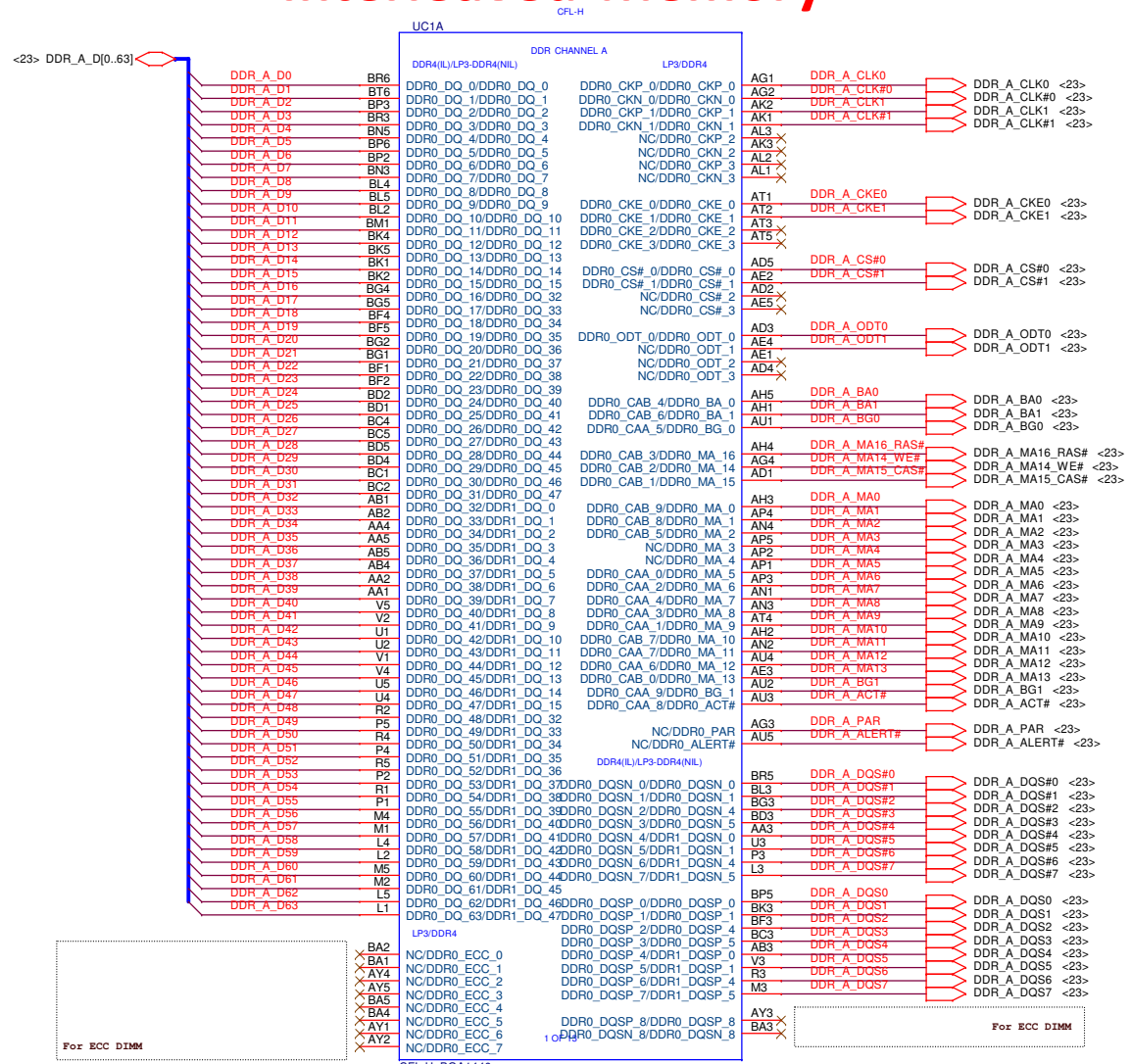
Title: CFL-H(1/8)DDI/eDP

Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 6 of 100

CHANNEL-A

Interleaved Memory



Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

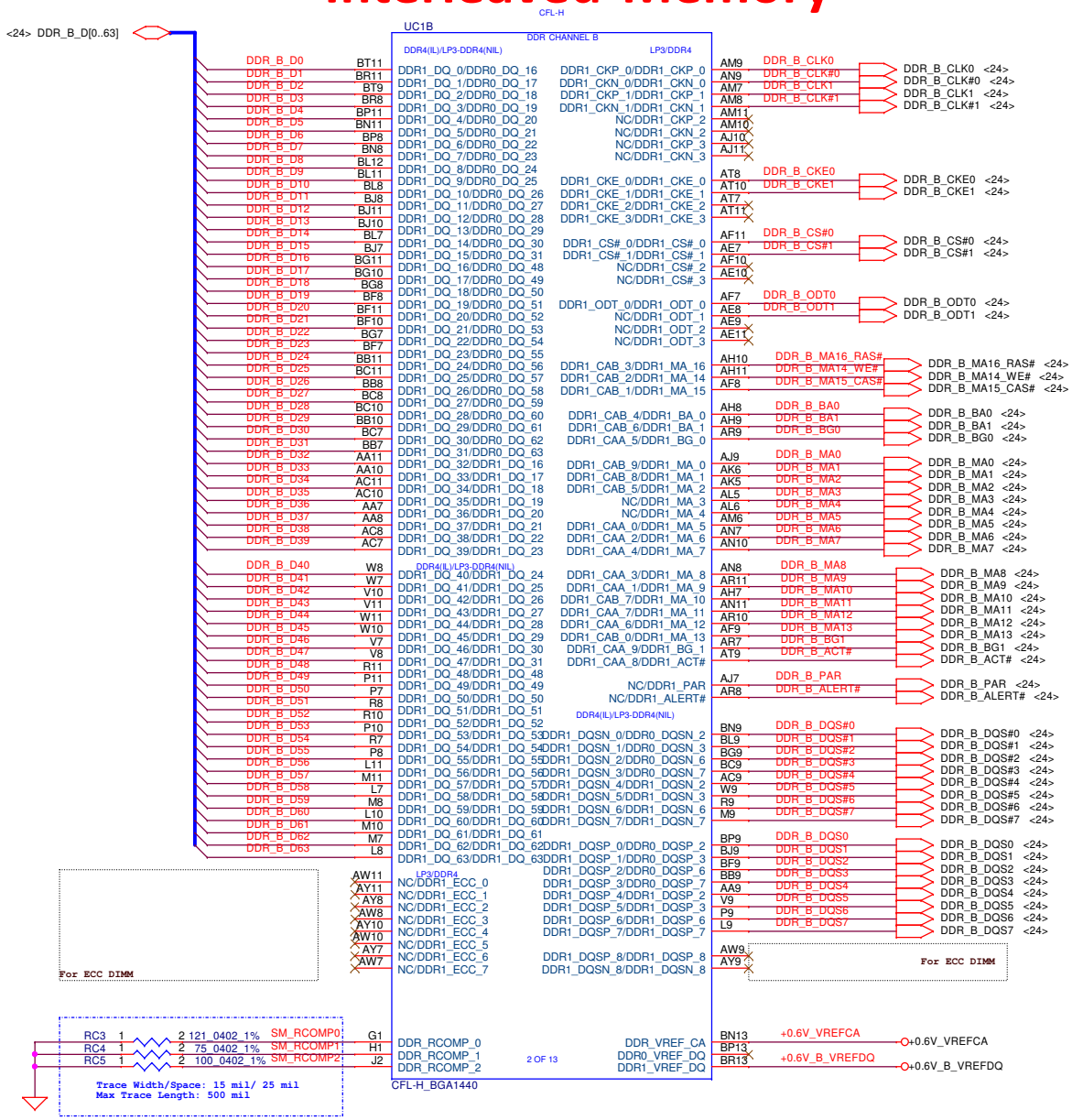
Title: CFL-H(2/8)DIMMA

Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 7 of 100

CHANNEL-B

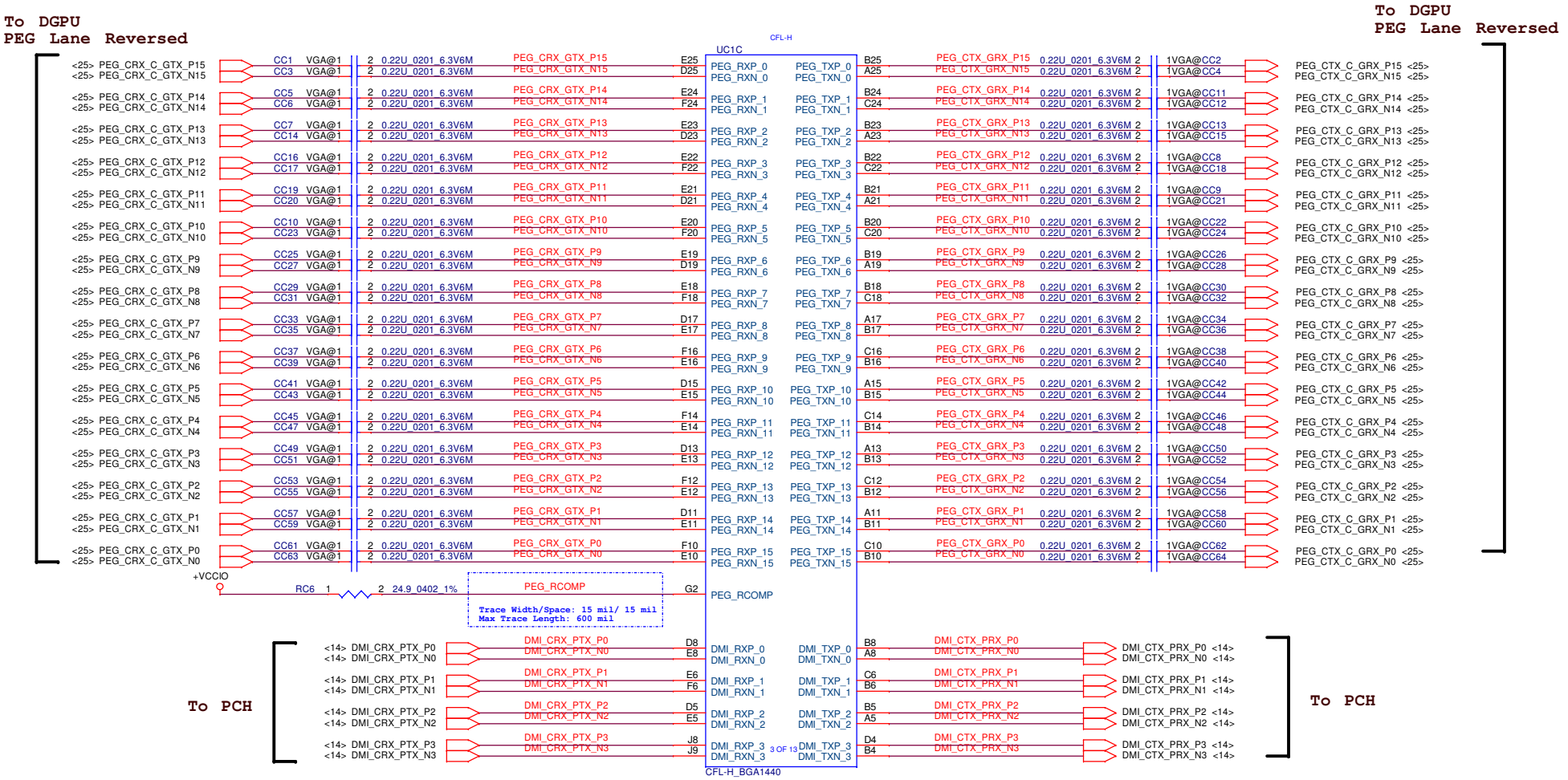
Interleaved Memory



Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

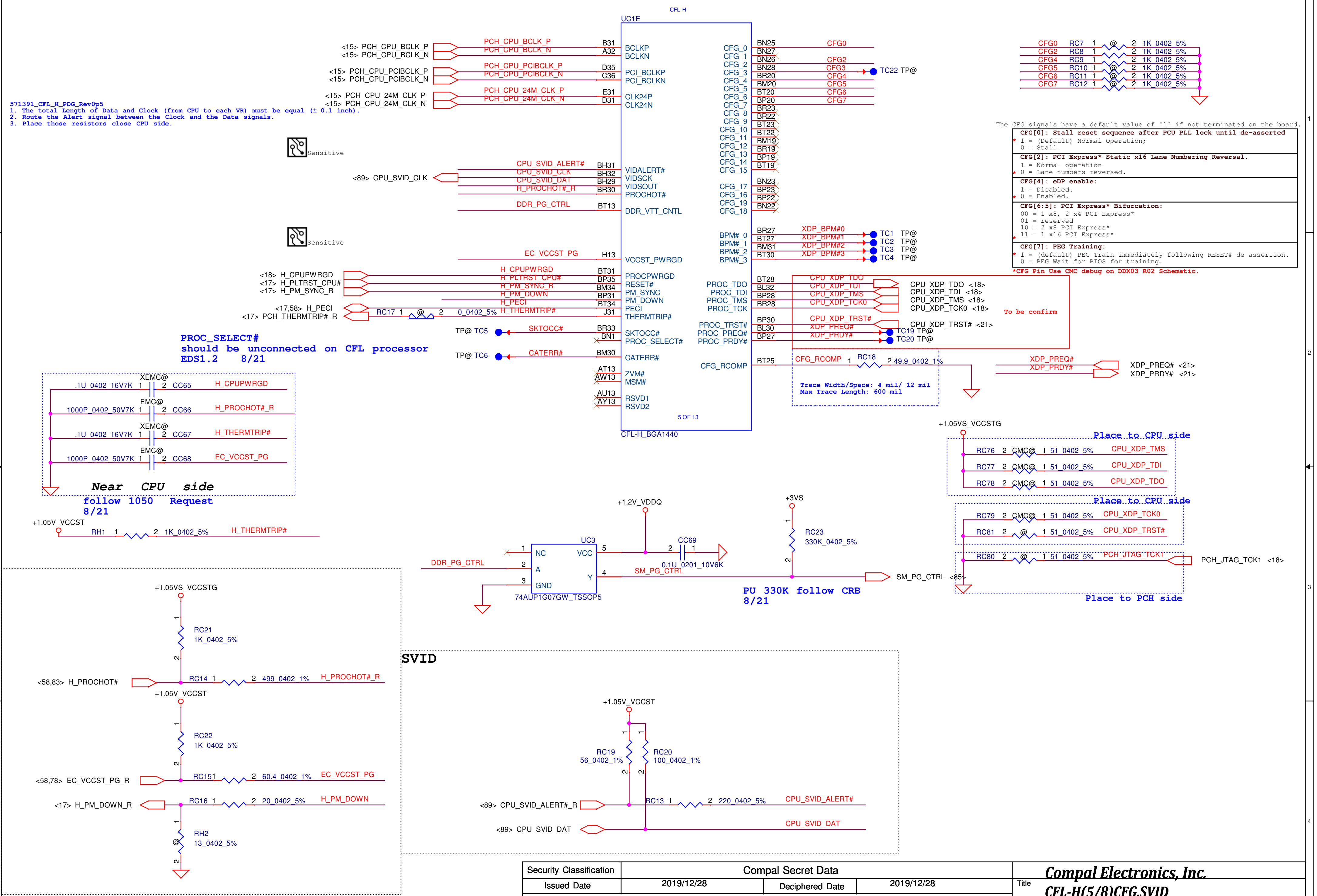
Compal Electronics, Inc.			
Title	CFL-H(3/8)DIMMB		
Size	Document Number		Rev
Custom	EH50F M/B LA-H431PR10		1.0
Date:	Wednesday, February 13, 2019	Sheet 8 of 100	

PEG&DMI



Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.			
Title	CFL-H(4/8)PEG/DMI		
Size: Custom	Document Number: EH50F M/B LA-H431PR10		Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 9 of 100		



CFL-H
UC1E
<15> PCH_CPU_BCLK_P
<15> PCH_CPU_BCLK_N
<15> PCH_CPU_PCIBCLK_P
<15> PCH_CPU_PCIBCLK_N
<15> PCH_CPU_24M_CLK_P
<15> PCH_CPU_24M_CLK_N
PCH_CPU_BCLK_P B31 BCLKP
PCH_CPU_BCLK_N A32 BCLKN
PCH_CPU_PCIBCLK_P D35 PCI_BCLKP
PCH_CPU_PCIBCLK_N C36 PCI_BCLKN
PCH_CPU_24M_CLK_P E31 CLK24P
PCH_CPU_24M_CLK_N D31 CLK24N
571391_CFL_H_PDG_Rev0p5
1. The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
2. Route the Alert signal between the Clock and the Data signals.
3. Place those resistors close CPU side.
Sensitive
<89> CPU_SVID_CLK
CPU_SVID_ALERT# BH31 VIDALERT#
CPU_SVID_CLK BH32 VIDSCK
CPU_SVID_DAT BH29 VIDSOUT
H_PROCHOT#_R BR30 PROCHOT#
DDR_PG_CTRL BT13 DDR_VTT_CNTL
Sensitive
EC_VCCST_PG H13 VCCST_PWRGD
<18> H_CPUPWRGD
<17> H_PLTRST_CPU#
<17> H_PM_SYNC_R
<17,58> H_PECI
<17> PCH_THERMTRIP#_R
H_CPUPWRGD BT31 PROCPWRGD
H_PLTRST_CPU# BP35 RESET#
H_PM_SYNC_R BM34 PM_SYNC
H_PM_DOWN BP31 PM_DOWN
H_PECI BT34 PECI
RC17 1 @ 2 0_0402_5% H_THERMTRIP# J31 THERMTRIP#
TP@ TC5 SKTOCC# BR33 SKTOCC#
BN1 PROC_SELECT#
TP@ TC6 CATERR# BM30 CATERR#
AT13 ZVM#
AW13 MSM#
AU13 RSVD1
AY13 RSVD2
5 OF 13
CFL-H_BGA1440
BN25 CFG_0 CFG0
BN27 CFG_1
BN26 CFG_2 CFG2
BN28 CFG_3 CFG3 TC22 TP@
BR20 CFG_4 CFG4
BM20 CFG_5 CFG5
BT20 CFG_6 CFG6
BP20 CFG_7 CFG7
BR23 CFG_8
BR22 CFG_9
BT23 CFG_10
BT22 CFG_11
BM19 CFG_12
BR19 CFG_13
BP19 CFG_14
BT19 CFG_15
BN23 CFG_17
BP23 CFG_16
BP22 CFG_19
BN22 CFG_18
BR27 BPM#_0 XDP_BPM#0 TC1 TP@
BT27 BPM#_1 XDP_BPM#1 TC2 TP@
BM31 BPM#_2 XDP_BPM#2 TC3 TP@
BT30 BPM#_3 XDP_BPM#3 TC4 TP@
BT28 PROC_TDO CPU_XDP_TDO
BL32 PROC_TDI CPU_XDP_TDI
BP28 PROC_TMS CPU_XDP_TMS
BR28 PROC_TCK CPU_XDP_TCK0
BP30 PROC_TRST# CPU_XDP_TRST#
BL30 PROC_PREQ# XDP_PREQ# TC19 TP@
BP27 PROC_PRDY# XDP_PRDY# TC20 TP@
CPU_XDP_TDO <18>
CPU_XDP_TDI <18>
CPU_XDP_TMS <18>
CPU_XDP_TCK0 <18>
CPU_XDP_TRST# <21>
To be confirm
BT25 CFG_RCOMP CFG_RCOMP 1 RC18 2 49.9_0402_1%
Trace Width/Space: 4 mil/ 12 mil
Max Trace Length: 600 mil
XDP_PREQ# XDP_PREQ# <21>
XDP_PRDY# XDP_PRDY# <21>
CFG0 RC7 1 @ 2 1K_0402_5%
CFG2 RC8 1 2 1K_0402_5%
CFG4 RC9 1 2 1K_0402_5%
CFG5 RC10 1 @ 2 1K_0402_5%
CFG6 RC11 1 @ 2 1K_0402_5%
CFG7 RC12 1 @ 2 1K_0402_5%
The CFG signals have a default value of '1' if not terminated on the board.
CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted
* 1 = (Default) Normal Operation;
0 = Stall.
CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
* 0 = Lane numbers reversed.
CFG[4]: eDP enable:
1 = Disabled.
* 0 = Enabled.
CFG[6:5]: PCI Express* Bifurcation:
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express*
* 11 = 1 x16 PCI Express*
CFG[7]: PEG Training:
* 1 = (default) PEG Train immediately following RESET# de assertion.
0 = PEG Wait for BIOS for training.
*CFG Pin Use CMC debug on DDX03 R02 Schematic.
PROC_SELECT#
should be unconnected on CFL processor
EDS1.2 8/21
XEMC@ .1U_0402_16V7K 1 2 CC65 H_CPUPWRGD
EMC@ 1000P_0402_50V7K 1 2 CC66 H_PROCHOT#_R
XEMC@ .1U_0402_16V7K 1 2 CC67 H_THERMTRIP#
EMC@ 1000P_0402_50V7K 1 2 CC68 EC_VCCST_PG
Near CPU side
follow 1050 Request
8/21
+1.05V_VCCST RH1 1 2 1K_0402_5% H_THERMTRIP#
+1.05VS_VCCSTG
Place to CPU side
RC76 2 CMC@ 1 51_0402_5% CPU_XDP_TMS
RC77 2 CMC@ 1 51_0402_5% CPU_XDP_TDI
RC78 2 CMC@ 1 51_0402_5% CPU_XDP_TDO
Place to CPU side
RC79 2 CMC@ 1 51_0402_5% CPU_XDP_TCK0
RC81 2 @ 1 51_0402_5% CPU_XDP_TRST#
RC80 2 @ 1 51_0402_5% PCH_JTAG_TCK1 PCH_JTAG_TCK1 <18>
Place to PCH side
+1.2V_VDDQ
UC3
1 NC VCC 5
DDR_PG_CTRL 2 A
3 GND Y 4
74AUP1G07GW_TSSOP5
CC69 2 1 0.1U_0201_10V6K
SM_PG_CTRL
+3VS
RC23 330K_0402_5%
SM_PG_CTRL <85>
PU 330K follow CRB
8/21
+1.05VS_VCCSTG
RC21 1K_0402_5%
<58,83> H_PROCHOT# RC14 1 2 499_0402_1% H_PROCHOT#_R
+1.05V_VCCST
RC22 1K_0402_5%
<58,78> EC_VCCST_PG_R RC151 1 2 60.4_0402_1% EC_VCCST_PG
<17> H_PM_DOWN_R RC16 1 2 20_0402_5% H_PM_DOWN
RH2 @ 13_0402_5%
SVID
+1.05V_VCCST
RC19 56_0402_1%
RC20 100_0402_1%
<89> CPU_SVID_ALERT#_R RC13 1 2 220_0402_5% CPU_SVID_ALERT#
<89> CPU_SVID_DAT CPU_SVID_DAT

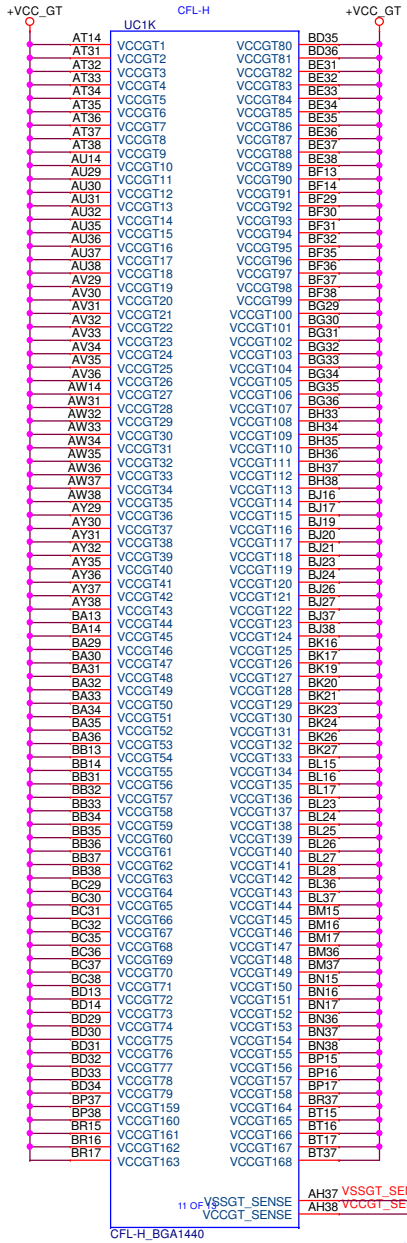
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: **CFL-H(5/8)CFG,SVID**

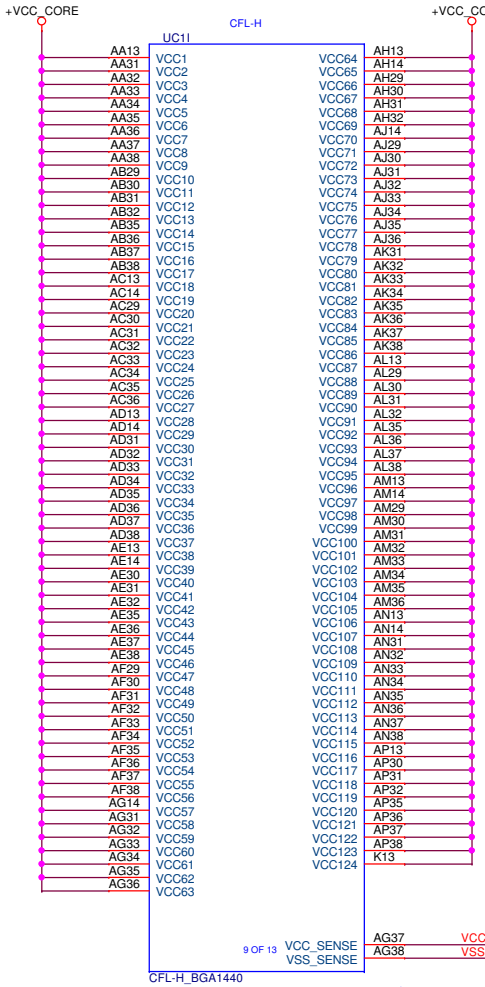
Size: Custom | Document Number: **EH50F M/B LA-H431PR10** | Rev 1.0

GT
32000mA(Hexa Core GT2)

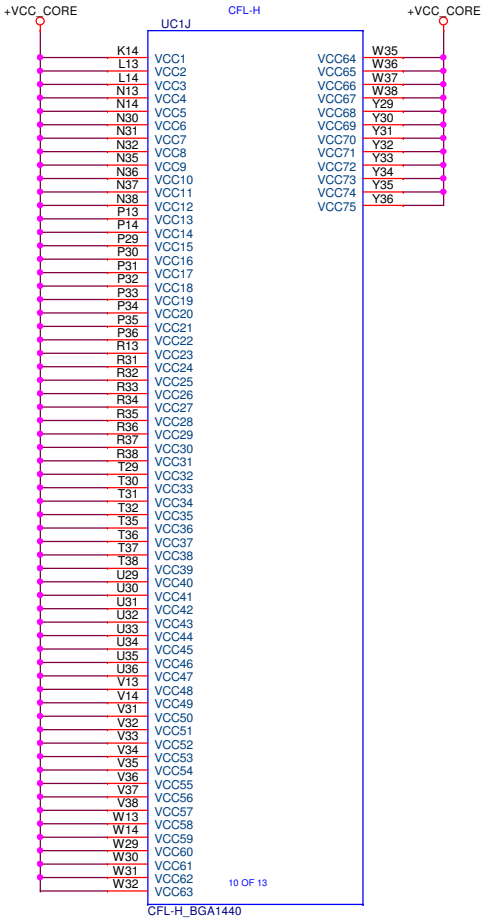


1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.

128000mA(Hexa Core GT2)



1. Vcc_SENSE/ Vss_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.



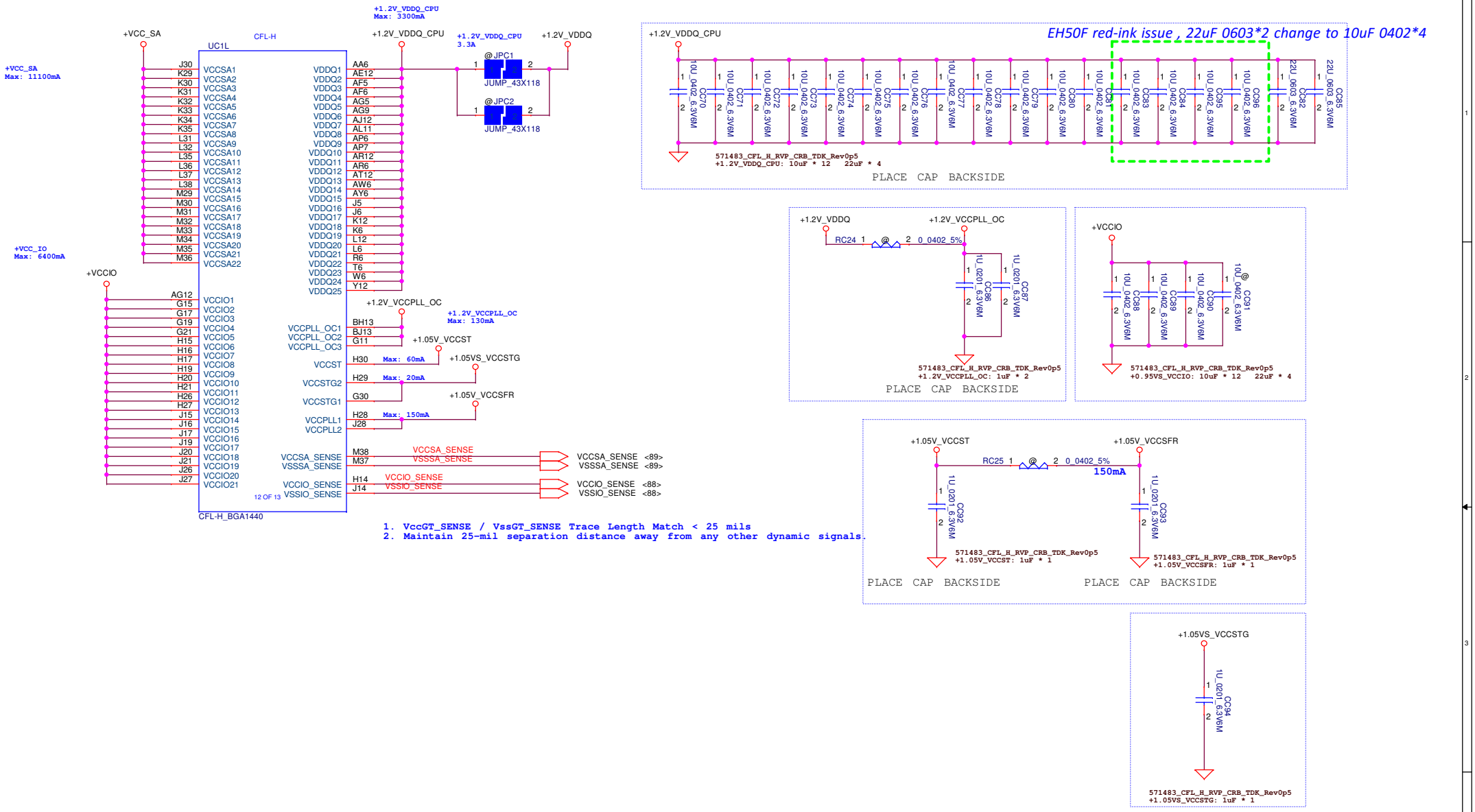
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: CFL-H(6/8)VCC CORE/GT

Size	Document Number	Rev
Custom	EH50F M/B LA-H431PR10	1.0

Date: Wednesday, February 13, 2019 Sheet 11 of 100



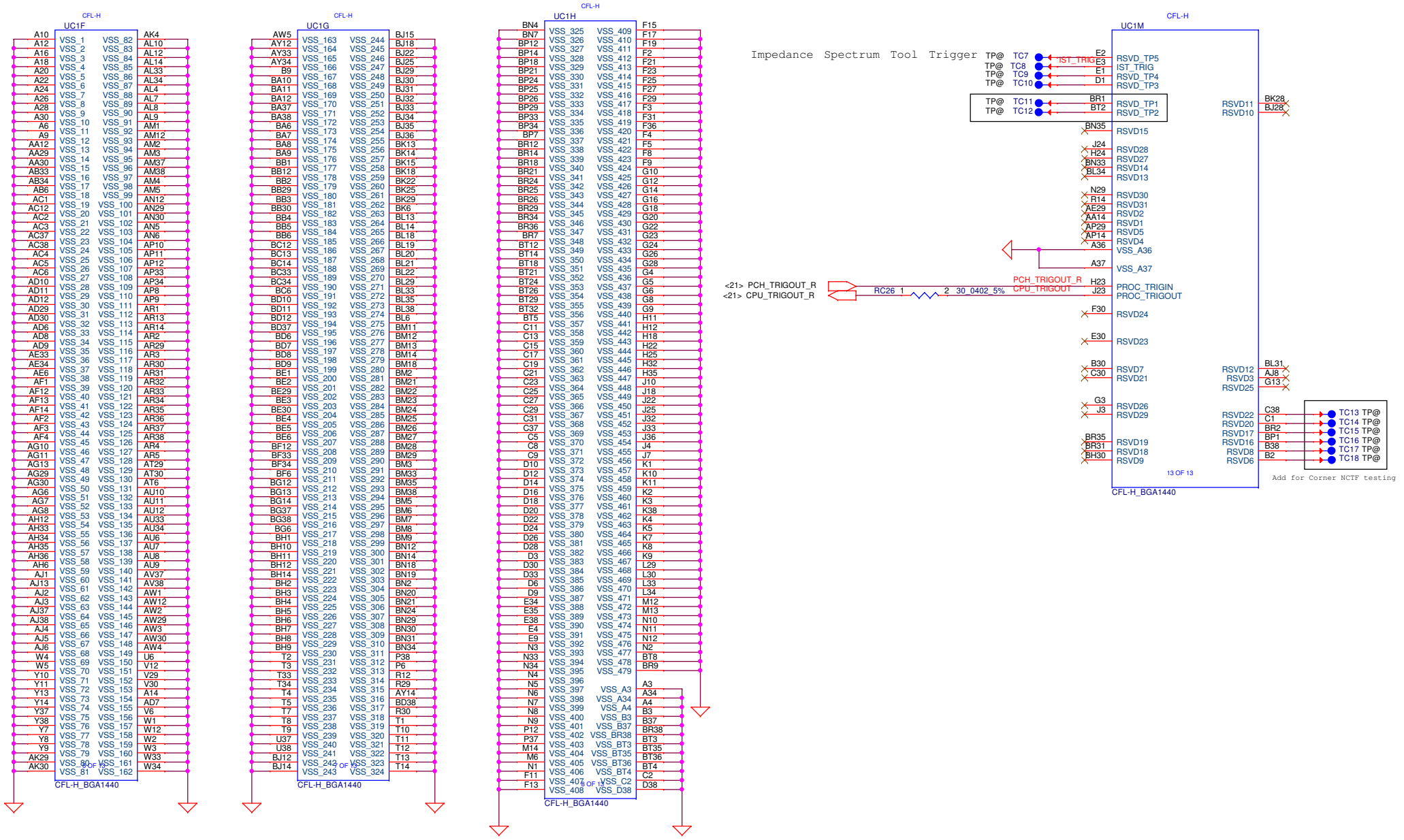
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: CFL-H(7/8)VCCSA/VCCIO/VDDQ

Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 12 of 100



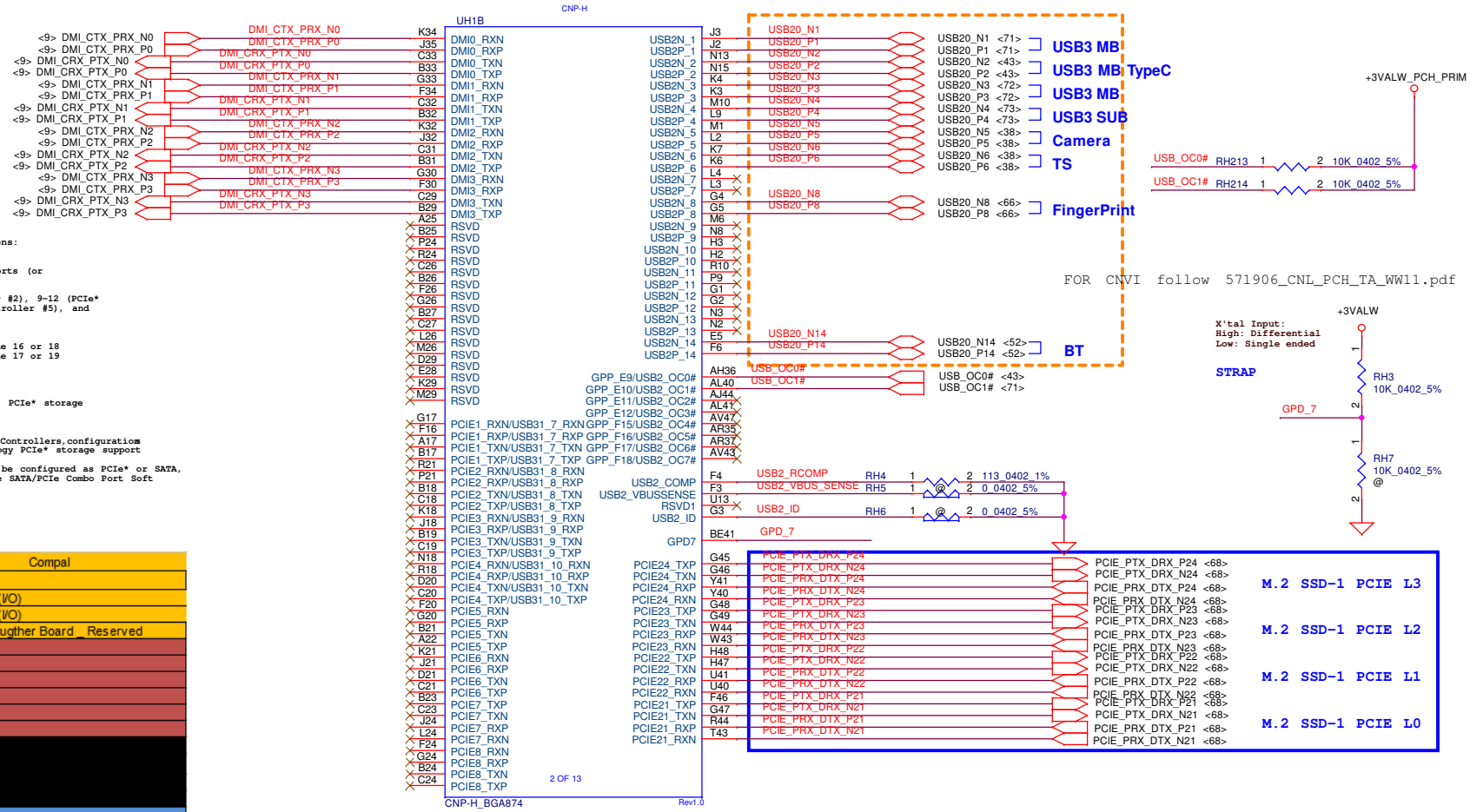
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: **CFL-H(8/8)GND/RSVD**

Size	Document Number	Rev
Custom	EH50F M/B LA-H431PR10	1.0

Date: Wednesday, February 13, 2019 Sheet 13 of 100



The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
– A maximum of 16 PCIe* Ports (or devices) can be enabled
• When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 – GbE (0 or 1)
– PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
– A maximum of 6 SATA Ports (or devices) can be enabled
– SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
– SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
– A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
– A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
– x2 and x4 PCIe* NVMe SSD
– x2 IntelR Optane? Memory Device
– See the " PCI Express* (PCIe*) " chapter for the PCH PCIe* Controllers,configuratiom , and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.

	CFL-H (HM370)		Compal
Lane0	USB3.1 Port1		USB 3 (I/O)
Lane1	USB3.1 Port2		USB 3 Type-C (I/O)
Lane2	USB3.1 Port3		USB 3 Type-C (I/O)
Lane3	USB3.1 Port4		USB 3 (I/O)_Daugther Board _Reserved
Lane4	USB3.1 Port5		
Lane5	USB3.1 Port6		
Lane6	USB3.1 Port7	PCIe Port1	
Lane7	USB3.1 Port8	PCIe Port2	
Lane8	USB3.1 Port9	PCIe Port3	
Lane9	USB3.1 Port10	PCIe Port4	
Lane10		PCIe Port5	
Lane11		PCIe Port6	
Lane12		PCIe Port7	
Lane13		PCIe Port8	
Lane14		PCIe Port9	
Lane15		PCIe Port10	
Lane16	SATA3 Port0	PCIe Port11	HDD
Lane17	SATA3 Port1	PCIe Port12	
Lane18	SATA3 Port0*	PCIe Port13	
Lane19	SATA3 Port1*	PCIe Port14	LAN+CR
Lane20	SATA3 Port2	PCIe Port15	WIFI
Lane21	SATA3 Port3	PCIe Port16	
Lane22	SATA3 Port4	PCIe Port17	M.2 SSD#1 (PCIe x4)
Lane23	SATA3 Port5	PCIe Port18	M.2 SSD#1 (PCIe x4)
Lane24		PCIe Port19	M.2 SSD#1 (PCIe x4)
Lane25		PCIe Port20	M.2 SSD#1 (PCIe x4)
Lane26		PCIe Port21	
Lane27		PCIe Port22	
Lane28		PCIe Port23	
Lane29		PCIe Port24	
	USB2 Port1		USB 3 (I/O)
	USB2 Port2		USB 3 Type-C (I/O)
	USB2 Port3		USB 2 (I/O)
	USB2 Port4		USB 2 (I/O)
	USB2 Port5		CCD
	USB2 Port6		TS
	USB2 Port7		
	USB2 Port8		FP
	USB2 Port9		
	USB2 Port10		
	USB2 Port11		
	USB2 Port12		
	USB2 Port13		
	USB2 Port14		BT

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	USB3.1 #8	USB3.1 #9	USB3.1 #10	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16	PCIe* #17	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
							PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	GbE				GbE		SATA 0a	GbE	SATA 0b		SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5					
Intel® RST Support							No Support				No Support				Yes				No Support				Yes				Yes			

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: PCH(1/8)DMI/PCIE/USB2

Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 14 of 100

PCH-H XTAL_IN/OUT POR is 24MHz for 571697_CNL_MOW_WW16_2017.pdf

XTAL_24M_PCH_OUT — RH11 EMC@ 33_0402_1% — XTAL_24M_PCH_OUT_R

XTAL_24M_PCH_IN — RH8 1M_0402_5% — RH9 EMC@ 33_0402_1% — XTAL_24M_PCH_IN_R

YH1 24MHZ_18PF_XRCGB24M000F2P51R0 (NC NC)

CH5 33P_0402_50V8J — CH6 18P_0402_50V8J

PCH_RTCX1 — RH12 10M_0402_5% — PCH_RTCX2

YH2 32.768KHZ_9PF_X1A000141000200

CH7 10P_0402_50V8J — CH8 10P_0402_50V8J

Trace Space: 15 mil
Max Trace Length: 1000 mil

use same part w C5MMH

Raptor

remove TP as C5PRH

UH1G — CNP-H — CNP-H_BGA874 — Rev1.0

<10> PCH_CPU_24M_CLK_P / PCH_CPU_24M_CLK_N
<10> PCH_CPU_BCLK_P / PCH_CPU_BCLK_N
XTAL_24M_PCH_OUT_R / XTAL_24M_PCH_IN_R
RH10 2_60.4_0402_1% XCLK_BIASREF
XCLK_BIASREF (PDG) Trace Width/Space: 15mil /15 mil Max Trace Length: 1000 mil 8/24
PCH_RTCX1 / PCH_RTCX2

VGA_CLKREQ# / LAN_CLKREQ# / WLAN_CLKREQ# / SSD1_CLKREQ# / SSD2_CLKREQ#
<25> VGA_CLKREQ#
<51> LAN_CLKREQ#
<52> WLAN_CLKREQ#
<68> SSD1_CLKREQ#
<68> SSD2_CLKREQ#

remove no use srcclkreq

Raptor

CLKOUT_ITPXDP# / CLKOUT_ITPXDP_P — Y3 / Y4 — TP@ TH2 / TP@ TH3

PCH_CPU_PCIBCLK_N / PCH_CPU_PCIBCLK_P — PCH_CPU_PCIBCLK_N <10> / PCH_CPU_PCIBCLK_P <10>

CLK_PEG_VGA# / CLK_PEG_VGA — CLK_PEG_VGA# <25> / CLK_PEG_VGA <25> — DGPU

CLK_PCIE_LAN# / CLK_PCIE_LAN — CLK_PCIE_LAN# <51> / CLK_PCIE_LAN <51> — GLAN

CLK_PCIE_WLAN# / CLK_PCIE_WLAN — CLK_PCIE_WLAN# <52> / CLK_PCIE_WLAN <52> — NGFF WL+BT(KEY E)

CLK_PCIE_NGFF1# / CLK_PCIE_NGFF1 — CLK_PCIE_NGFF1# <68> / CLK_PCIE_NGFF1 <68> — M2-1 SSD

CLK_PCIE_NGFF2# / CLK_PCIE_NGFF2 — CLK_PCIE_NGFF2# <68> / CLK_PCIE_NGFF2 <68> — M2-2 SSD

Raptor

REFCLK_CNV — REFCLK_CNV <52>

RH14 10K_0402_5%

+3VS

RH217 LAN_CLKREQ# — RH218 VGA_CLKREQ# — RH219 WLAN_CLKREQ# — RH220 SSD1_CLKREQ# — RH221 SSD2_CLKREQ# (10K_0402_5%)

remove SD signal from PCH

remove CPU_C10_GATE#

UH1M — CNP-H — CNP-H_BGA874 — Rev1.0

3.3V / 1.8V

CLK_CNV_PRX_DTX_N / CLK_CNV_PRX_DTX_P — CLK_CNV_PRX_DTX_N <52> / CLK_CNV_PRX_DTX_P <52>

CNV_PRX_DTX_N0 / CNV_PRX_DTX_P0 / CNV_PRX_DTX_N1 / CNV_PRX_DTX_P1 <52>

CLK_CNV_PTX_DRX_N / CLK_CNV_PTX_DRX_P — CLK_CNV_PTX_DRX_N <52> / CLK_CNV_PTX_DRX_P <52>

CNV_PTX_DRX_N0 / CNV_PTX_DRX_P0 / CNV_PTX_DRX_N1 / CNV_PTX_DRX_P1 <52>

CNV_WT_RCOMP — RH16 150_0402_1%

PCIE_RCOMPN — RH17 100_0402_1%

PCIE_RCOMPP

SD_RCOMP_1P8 — RH18 200_0402_1%

SD_RCOMP_3P3 — RH19 200_0402_1%

checked CRB

GPPJ_RCOMP_1P8 — RH20 200_0402_1%

<52> CNV_BRI_PTX_DRX / CNV_BRI_PRX_DTX
<52> CNV_RGI_PTX_DRX / CNV_RGI_PRX_DTX
GPP_J9

+1.8VALW_PRIM

RH1811 CNVI@ 20K_0402_1% CNV_BRI_PRX_DTX

RH1821 CNVI@ 20K_0402_1% CNV_RGI_PRX_DTX

TP@ TH4
#571483_CFL_H_RVP_CRB_TDK_Rev0p5
Recommend external test point

571391_CFL_H_PDG_Rev0p71
To avoid floating input at the I/O pin BRI_RSP and RGI_RSP it is recommended to add a weak pull up resistor to the SoC pin with a recommended value of 20K ohm.

For DDX03 R02

XTAL Frequency Select

+1.8VALW_PRIM — RH15 4.7K_0402_5% — CNV_BRI_PTX_DRX — STRAP

This signal has a weak internal pull-down 20K.
0 = 38.4/19.2MHz XTAL frequency selected.
1 = 24MHz XTAL frequency selected. (DDX03)
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

VCCPSPI Select

+1.8VALW_PRIM — RH21 @ 4.7K_0402_5% — GPP_J9 — STRAP

The signal has a weak internal pull-down 20K
0 = VCCPSPI is connected to 3.3V rail
1 = VCCPSPI is connected to 1.8V rail
Note: If VCCPSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

M.2 CNV Mode Select

+1.8VALW_PRIM — RH22 10K_0402_5% CNV_RGI_PTX_DRX — RH23 @ 10K_0402_5% — STRAP

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
Pulled down by CRF CNVi RGI_DT pin

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: PCH(2/8)CLK/CNVI/SD

Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 15 of 100

no follow naming

Raptor

<25,39> DP0_HPD_PCH
<25,40> HDMI_HPD_PCH
DP0_HPD_PCH
HDMI_HPD_PCH
RT881 1 @ 2 0_0402_5%

UH1E
CNP-H
AT6 GPP_I0/DDPB_HPD0/DISP_MISC0
AN10 GPP_I1/DDPC_HPD1/DISP_MISC1
AP9 GPP_I2/DDPD_HPD2/DISP_MISC2
AL15 GPP_I3/DDPF_HPD3/DISP_MISC3
AN6 GPP_I4/EDP_HPD/DISP_MISC4
GPP_I5/DDPB_CTRLCLK AL13
GPP_I6/DDPB_CTRLDATA AR8
GPP_I7/DDPC_CTRLCLK AN13
GPP_I8/DDPC_CTRLDATA AL10
GPP_I9/DDPD_CTRLCLK AL9
GPP_I10/DDPD_CTRLDATA AR3
GPP_F23/DDPF_CTRLDATA AN40
GPP_F22/DDPF_CTRLCLK AT49
GPP_F14/PS_ON# AP41
GPP_K23/IMGCLKOUT1 M45
GPP_K22/IMGCLKOUT0 L48
GPP_K21 T45
GPP_K20 T46
GPP_H23/TIME_SYNC0 AJ47
5 OF 13
CNP-H_BGA874
Rev1.0

<38> EDP_HPD
EDP_HPD

can remove if no use DP
08/18

remove PCH DP SCLK/SDATA

DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B~D is not detected.
1 = Port B,C,D is detected. (Default)
Notes:
1. The internal Pull-down is disabled after PCH_PWROK de-asserts.
2. This signal is in the primary well.

intel critical net recommend
RH1981 2 100K_0201_5%
PLT_RST#
CH9 1 2 100P_0402_50V8J
XEMC@

<51,58> EC_PME#
RH24 1 @ 2 0_0402_5%
EC_PME#_R
UH1A
CNP-H
BE36 GPP_A11/PME#/SD_VDD2_PWR_EN#
AV29 GPP_B13/PLTRST#
PLT_RST# <58,66>
R15 RSVD2
R13 RSVD1
Y47 GPP_K16/GSXCLK
Y46 GPP_K12/GSXDOUT
Y48 GPP_K13/GSXSLOAD
W46 GPP_K14/GSXDIN
AA45 GPP_K15/GSXSRESET#
GPIO Serial Expander (GSX) is the capability provided by the PCH to expand the GPIOs on a platform that needs more GPIOs than the ones provided by the PCH.

CRB connect GND
RH1861 @ 2 0_0402_5%
TH6 TP@
AL37 VSS
AN35 TP

<66> PCH_SPI_SI_R
<66> PCH_SPI_SO_R
<66> PCH_SPI_CLK_R
RH258 1 NTRM@ 2 0_0402_5% PCH_SPI_SI
RH259 1 NTRM@ 2 0_0402_5% PCH_SPI_SO
RH260 1 NTRM@ 2 0_0402_5% PCH_SPI_CLK
AU41 SPI0_MOSI
BA45 SPI0_MISO
AY47 SPI0_CS0#
AW47 SPI0_CLK
AW48 SPI0_CS1#
AL47 GPP_E3/CPU_GP0
AM45 GPP_E7/CPU_GP1
BF32 GPP_B3/CPU_GP2
BC33 GPP_B4/CPU_GP3
TP_INT# 2 DH1 1 RB751V-40_SOD323-2 EC_TP_INT# <58,63>
+3VS
TP_INT# RH28 2 1 100K_0402_5%

intel critical net recommend
PCH_SPI_CLK RH1951 @ 2 100K_0201_5%

PCH_SPI_IO2
PCH_SPI_IO3
<66> PCH_SPI_CS#2
AY48 SPI0_IO2
BA46 SPI0_IO3
AT40 SPI0_CS2#
AE44 GPP_H18/SML4ALERT#
AJ46 GPP_H17/SML4DATA
AE43 GPP_H16/SML4CLK
AC47 GPP_H15/SML3ALERT#
AD48 GPP_H14/SML3DATA
AF47 GPP_H13/SML3CLK
AB47 GPP_H12/SML2ALERT#
AD47 GPP_H11/SML2DATA
AE48 GPP_H10/SML2CLK
GPP_H15
GPP_H12
GPP_H12 <19>
+RTCVCC
BE19 GPP_D1/SPI1_CLK/SBK1_BK1
BF19 GPP_D0/SPI1_CS#/SBK0_BK0
BF18 GPP_D3/SPI1_MOSI/SBK3_BK3
BE18 GPP_D2/SPI1_MISO/SBK2_BK2
BC17 GPP_D22/SPI1_IO3
BD17 GPP_D21/SPI1_IO2
1 OF 13
CNP-H_BGA874
Rev1.0
BB44 INTRUDER#
SM_INTRUDER# 1M_0402_5% 2 1 RH30
RVP: 330K
A 1 M pull-up is used on the customer reference board (CRB). This is needed to reduce leakage from Coin Cell Battery in G3 state.

* wait confirm CG7
PDG P348 quad mode support PH1K
CRB PU 20k
+3VALW_SPI
#571182_CFL_PCH_EDS_Rev1.0 recommend 100k
#571391_CFL_H_PDG_Rev0p71
RH25 2 1 1K_0402_5% PCH_SPI_IO2
RH26 2 1 1K_0402_5% PCH_SPI_IO3
RH27 2 1 1K_0402_5% PCH_SPI_SI
+3VALW_PCH_PRIM
RH29 2 1 100K_0402_5% GPP_H15 STRAP
#571182_CNL_PCH_H_EDS_V1_Rev0.7
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
571007_CFL_MOW_Archive_WW22_2017
STUFF R on GPP_H15

R2 = 5ohm for SPI dual-load
RH258 RH259 RH260
4.99_0402_1% SD034499B80 TPM@
4.99_0402_1% SD034499B80 TPM@
4.99_0402_1% SD034499B80 TPM@

Vinafix

SPI ROM (16MByte)
+3VALW_SPI
CH10 1 2 0.1U_0201_10V6K
UH2
PCH_SPI_CS#0 1
PCH_SPI_SO_0_R 2
PCH_SPI_IO2_0_R 3
4
/CS
DO(IO1)
/WP(IO2)
GND
VCC 8
/HOLD(IO3) 7
CLK 6
DI(IO0) 5
PCH_SPI_IO3_0_R
PCH_SPI_CLK_0_R
PCH_SPI_SI_0_R
W25Q128FVSIQ_SO8
P/N: SA0000B8400 , XMC
PCH_SPI_CS#0 RH31 1 @ 2 4.7K_0402_5% +3VALW_SPI
PCH_SPI_CLK_0_R RH33 1 @ 2 0_0402_5%
@ CH12 1 2 68P_0402_50V8J
PCH_SPI_SI_0_R RH107 1 2 33_0402_1% PCH_SPI_SI_R
PCH_SPI_SO_0_R RH108 1 2 33_0402_1% PCH_SPI_SO_R
PCH_SPI_IO3_0_R RH109 1 2 33_0402_1% PCH_SPI_IO3
PCH_SPI_CLK_0_R RH110 1 2 33_0402_1% PCH_SPI_CLK_R
PCH_SPI_IO2_0_R RH111 1 2 33_0402_1% PCH_SPI_IO2
intel PDG 1.8
33 ohm for 3.3V for singel load
place 500 mil from PCH
note : 1050 Use 8M rom

PCH PLTRST Buffer
RH32 1 @ 2 0_0402_5%
+3VS
CH11 1 2 0.1U_0201_10V6K
PLT_RST#
UH3
1 B
2 A
5 VCC
3 GND
4 Y
TC7SH08FU_SSOP5
SA00000OH00
PLT_RST_BUF# <25,51,52,68>
EH50F:main source change to SA00000OH00

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.
Title: PCH(3/8)DDC/SPI
Size: Custom
Document Number: EH50F M/B LA-H431PR10
Rev: 1.0
Date: Wednesday, February 13, 2019
Sheet 16 of 100

#571391_CFL_H_PDG_Rev0p5
- eSPI clock and eSPI data mismatched: <500 mils.
- eSPI clock and eSPI chip select mismatched: <500 mils.
- eSPI signal maximum 9 Vias
* If DATA signals are entirely routed on MS, stuff the resistor with 15 Ohm.

CNP-H

UH1F

USB3 MB
<71> USB3_PTX_DRX_N1
<71> USB3_PTX_DRX_P1
<71> USB3_PRX_DTX_N1
<71> USB3_PRX_DTX_P1

USB3 Type C
<42> USB3_PTX_DRX_N2
<42> USB3_PTX_DRX_P2
<42> USB3_PRX_DTX_N2
<42> USB3_PRX_DTX_P2

USB3 MB
<72> USB3_PTX_DRX_P3
<72> USB3_PTX_DRX_N3
<72> USB3_PRX_DTX_P3
<72> USB3_PRX_DTX_N3

USB3 SUB
<73> USB3_PTX_DRX_P4
<73> USB3_PTX_DRX_N4
<73> USB3_PRX_DTX_P4
<73> USB3_PRX_DTX_N4

F9 USB31_1_TXN
F7 USB31_1_TXP
D11 USB31_1_RXN
C11 USB31_1_RXP
C3 USB31_2_TXN
D4 USB31_2_TXP
B9 USB31_2_RXN
C9 USB31_2_RXP
C17 USB31_6_TXN
C16 USB31_6_TXP
G14 USB31_6_RXN
F14 USB31_6_RXP
C15 USB31_5_TXN
B15 USB31_5_TXP
J13 USB31_5_RXN
K13 USB31_5_RXP
G12 USB31_3_TXP
F11 USB31_3_TXN
C10 USB31_3_RXP
B10 USB31_3_RXN
C14 USB31_4_TXP
B14 USB31_4_TXN
J15 USB31_4_RXP
K16 USB31_4_RXN

1.8V (eSPI)
BB39 GPP_A1/LAD0/ESPI_IO0
AW37 GPP_A2/LAD1/ESPI_IO1
AV37 GPP_A3/LAD2/ESPI_IO2
BA38 GPP_A4/LAD3/ESPI_IO3
BE38 GPP_A5/LFRAME#/ESPI_CS0#
AW35 GPP_A6/SERIRQ/ESPI_CS1#
BA36 GPP_A7/PIRQA#/ESPI_ALERT0#
BE39 GPP_A0/RCIN#/ESPI_ALERT1#
BF38 GPP_A14/SUS_STAT#/ESPI_RESET#
BB36 GPP_A9/CLKOUT_LPC0/ESPI_CLK
BB34 GPP_A10/CLKOUT_LPC1
T48 GPP_K19/SMI#
T47 GPP_K18/NMI#
AH40 GPP_E6/SATA_DEVSLP2
AH35 GPP_E5/SATA_DEVSLP1
AL48 GPP_E4/SATA_DEVSLP0
AP47 GPP_F9/SATA_DEVSLP7
AN37 GPP_F8/SATA_DEVSLP6
AN46 GPP_F7/SATA_DEVSLP5
AR47 GPP_F6/SATA_DEVSLP4
AP48 GPP_F5/SATA_DEVSLP3
6 OF 13

CNP-H_BGA874 Rev1.0

LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3
LPC_AD0 <58> LPC_AD1 <58> LPC_AD2 <58> LPC_AD3 <58>
LPC Bus check straps
LPC : +3.3V

LPC_FRAME# TPM_SERIRQ KBRST# ESPI_RST#
LPC_FRAME# <58> TPM_SERIRQ <58,66>

RH262 1 @ 2 0_0402_5% OVRM_EN <22,58>
CLK_LPC RH35 2 1 22_0402_5% CLK_LPC_R <58>

+3VS
TPM_SERIRQ 2 1 RH37 10K_0402_5%
LPC_PIRQA# 1 2 RH38 10K_0402_5%
KBRST# 1 2 RH248 10K_0402_5%

Raptor

SSD_DEVSLP1 SSD_DEVSLP1 <68>
CONFIRM WITH SW

Raptor

UH1C

For Intel CLINK
TH10 TP@ CL_CLK
TH11 TP@ CL_DATA
TH12 TP@ CL_RST#
HDD

AR2 CL_CLK
AT5 CL_DATA
AU4 CL_RST#
P48 GPP_K8
V47 GPP_K9
V48 GPP_K10
W47 GPP_K11
L47 GPP_K0
L46 GPP_K1
U48 GPP_K2
U47 GPP_K3
N48 GPP_K4
N47 GPP_K5
P47 GPP_K6
R46 GPP_K7

G36 PCIE9_RXN
F36 PCIE9_RXP
C34 PCIE9_TXN
D34 PCIE9_TXP
K37 PCIE10_RXN
J37 PCIE10_RXP
C35 PCIE10_TXN
B35 PCIE10_TXP
F44 PCIE15_RXN/SATA2_RXN
E45 PCIE15_RXP/SATA2_RXP
B40 PCIE_15_SATA_2_TXN
C40 PCIE15_TXP/SATA2_TXP
L41 PCIE16_RXN/SATA3_RXN
M40 PCIE16_RXP/SATA3_RXP
B41 PCIE16_TXN/SATA3_TXN
C41 PCIE16_TXP/SATA3_TXP
K43 PCIE17_RXN/SATA4_RXN
K44 PCIE17_RXP/SATA4_RXP
A42 PCIE17_TXN/SATA4_TXN
B42 PCIE17_TXP/SATA4_TXP
P41 PCIE18_RXN/SATA5_RXN
R40 PCIE18_RXP/SATA5_RXP
C42 PCIE18_TXN/SATA5_TXN
D42 PCIE18_TXP/SATA5_TXP

PCIE_PRX_DTX_N9 PCIE_PRX_DTX_P9 PCIE_PTX_DRX_N9 PCIE_PTX_DRX_P9
PCIE_PRX_DTX_N9 <68> PCIE_PRX_DTX_P9 <68> PCIE_PTX_DRX_N9 <68> PCIE_PTX_DRX_P9 <68>
M.2 SSD-1 PCIE L3

PCIE_PRX_DTX_N10 PCIE_PRX_DTX_P10 PCIE_PTX_DRX_N10 PCIE_PTX_DRX_P10
PCIE_PRX_DTX_N10 <68> PCIE_PRX_DTX_P10 <68> PCIE_PTX_DRX_N10 <68> PCIE_PTX_DRX_P10 <68>
M.2 SSD-1 PCIE L2

PCIE_PRX_DTX_N15 PCIE_PRX_DTX_P15 PCIE_PTX_DRX_N15 PCIE_PTX_DRX_P15
PCIE_PRX_DTX_N15 <52> PCIE_PRX_DTX_P15 <52> PCIE_PTX_DRX_N15 <52> PCIE_PTX_DRX_P15 <52>
NGFF
WL+BT(KEY E)

Raptor

M.2 SSD-1 PCIE L1
<68> PCIE_PTX_DRX_P11
<68> PCIE_PTX_DRX_N11
<68> PCIE_PRX_DTX_P11
<68> PCIE_PRX_DTX_N11

C36 PCIE11_TXP/SATA0A_TXP
B36 PCIE11_TXN/SATA0A_TXN
F39 PCIE11_RXP/SATA0A_RXP
G38 PCIE11_RXN/SATA0A_RXN

SATA_PRX_DTX_N4 <67>
SATA_PRX_DTX_P4 <67>
SATA_PTX_DRX_N4 <67>
SATA_PTX_DRX_P4 <67>
HDD

Raptor

GLAN
<51> PCIE_PTX_DRX_N14
<51> PCIE_PTX_DRX_P14
<51> PCIE_PRX_DTX_N14
<51> PCIE_PRX_DTX_P14

DGPU_PRSNT#
AR42 GPP_F10/SATA_SCLOCK
AR48 GPP_F11/SATA_SLOAD
AU47 GPP_F13/SATA_SDATAOUT0
AU46 GPP_F12/SATA_SDATAOUT1

PCIE_PTX_DRX_N14
PCIE_PTX_DRX_P14
PCIE_PRX_DTX_N14
PCIE_PRX_DTX_P14

C39 PCIE14_TXN/SATA1B_TXN
D39 PCIE14_TXP/SATA1B_TXP
D46 PCIE14_RXN/SATA1B_RXN
C47 PCIE14_RXP/SATA1B_RXP
AK48 GPP_E8/SATA_LED#

+3VS
SATA_GP1 RH2012 1 10K_0402_5%
M.2 SSD PCIE/SATA select pin

B38 PCIE13_TXN/SATA0B_TXN
C38 PCIE13_TXP/SATA0B_TXP
C45 PCIE13_RXN/SATA0B_RXN
C46 PCIE13_RXP/SATA0B_RXP
AH41 GPP_E0/SATAXPCIE0/SATAGP0
AJ43 GPP_E1/SATAXPCIE1/SATAGP1
AK47 GPP_E2/SATAXPCIE2/SATAGP2
AN47 GPP_F0/SATAXPCIE3/SATAGP_3
AM46 GPP_F1/SATAXPCIE4/SATAGP4
AM43 GPP_F2/SATAXPCIE5/SATAGP5
AM47 GPP_F3/SATAXPCIE6/SATAGP6
AM48 GPP_F4/SATAXPCIE7/SATAGP7

SATA_GP1 SATA_GP1 <68>
RH187 1 @ 2 10K_0402_5%
SATA_GP5 TP@ TH13

M.2 SSD-1 PCIE L0
<68> PCIE_PTX_DRX_P12
<68> PCIE_PTX_DRX_N12
<68> PCIE_PRX_DTX_P12
<68> PCIE_PRX_DTX_N12

E37 PCIE12_TXP/SATA1A_TXP
D38 PCIE12_TXN/SATA1A_TXN
J41 PCIE12_RXP/SATA_1A_RXP
H42 PCIE12_RXN/SATA1A_RXN
B44 PCIE20_TXP/SATA7_TXP
A44 PCIE20_TXN/SATA7_TXN
R37 PCIE20_RXP/SATA7_RXP
R35 PCIE20_RXN/SATA7_RXN
D43 PCIE19_TXP/SATA6_TXP
C44 PCIE19_TXN/SATA6_TXN
N42 PCIE19_RXP/SATA6_RXP
M44 PCIE19_RXN/SATA6_RXN
3 OF 13

GPP_F21/EDP_BKLTCTL PCH_BKL_PWM
GPP_F20/EDP_BKLTEN ENBKL
GPP_F19/EDP_VDDEN PCH_ENVDD
PCH_BKL_PWM <38>
ENBKL <58>
PCH_ENVDD <38>

AD3 THRMTRIP# PCH_THERMTRIP#
AF2 PECI PCH_PECI
AF3 PM_SYNC H_PM_SYNC
AG5 PLTRST_CPU# H_PLTRST_CPU#
AE2 PM_DOWN H_PM_DOWN_R

RH40 1 2 620_0402_5%
RH41 1 @ 2 13_0402_5%
RH42 1 2 30_0402_5%
H_PM_SYNC_R

#571391_CFL_H_PDG_Rev0p5.pdf
PCH_THERMTRIP#_R <10>
H_PECI <10,58>
H_PM_SYNC_R <10>
H_PLTRST_CPU# <10>
H_PM_DOWN_R <10>

Raptor:confirm with SW

H_PECI .1U_0402_16V7K 1 XEMC@ 2 CH50

+3VALW_PCH_PRIM
RH43 10K_0402_5% UMA@
DGPU_PRSNT#
RH44 10K_0402_5% VGA@

	GPP_F13 DGPU_PRSNT#
DIS,Optimus	0
UMA	1

Raptor

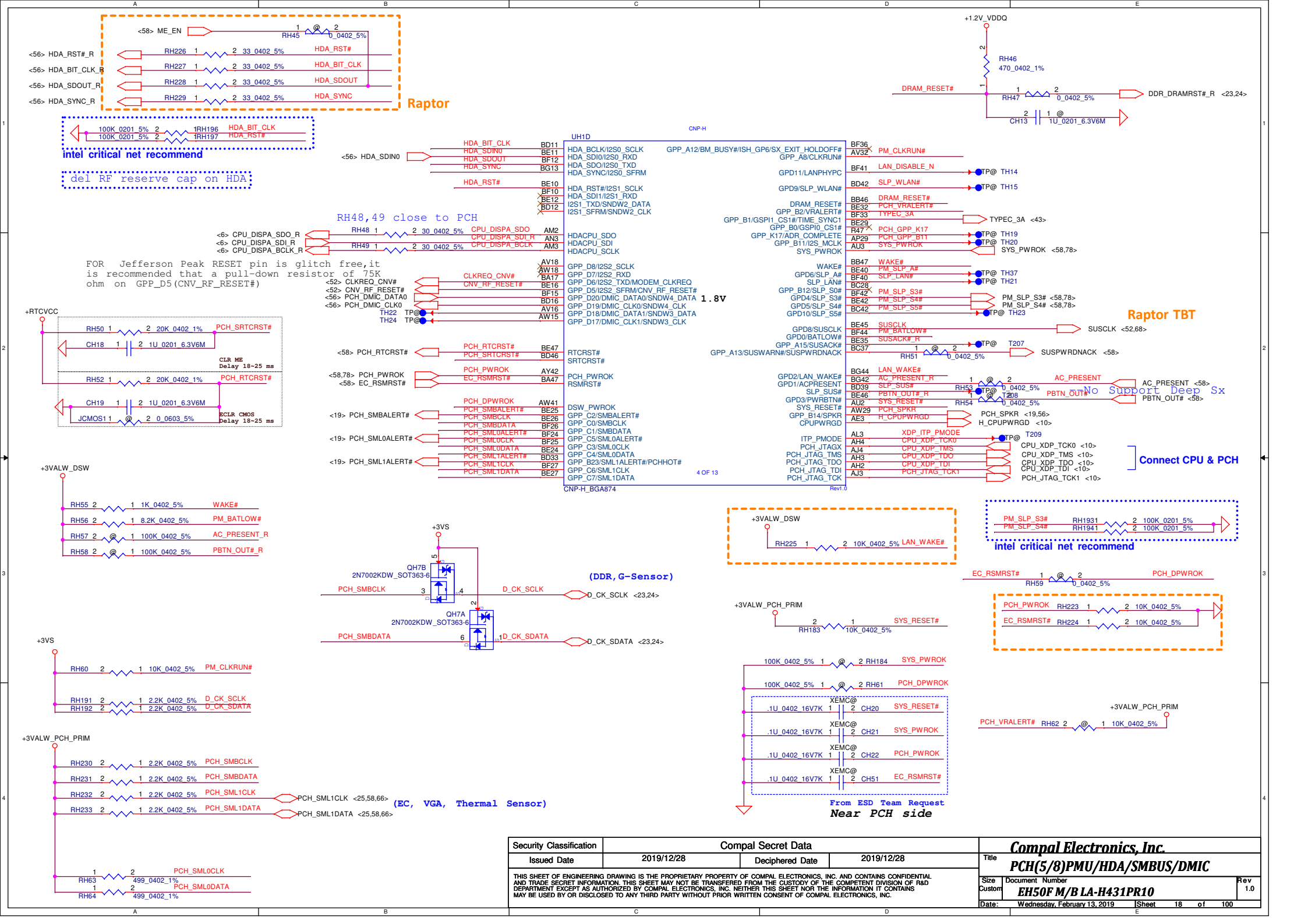
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: PCIE/SATA/USB3/eSPI

Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 17 of 100



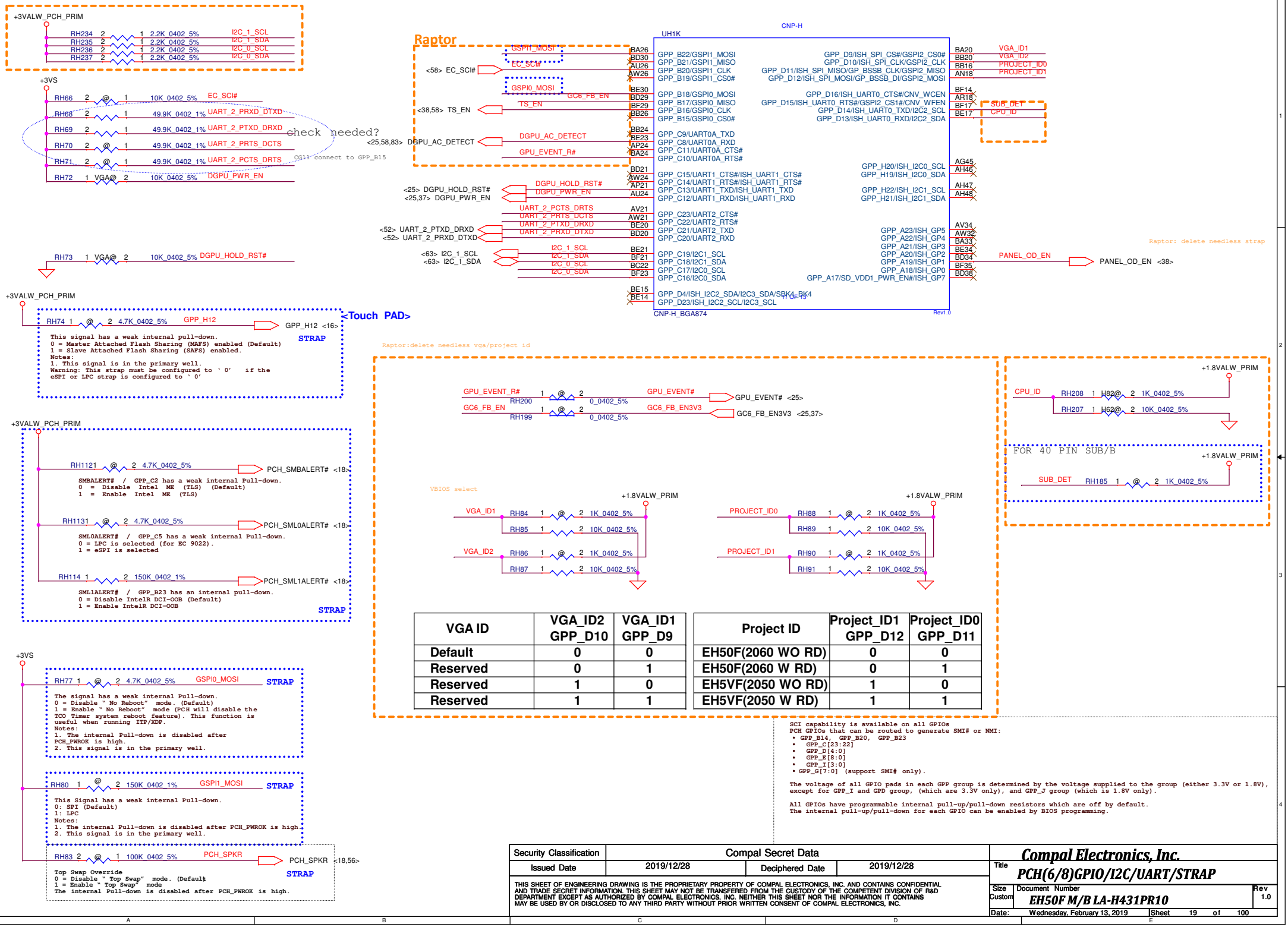
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: PCH(5/8)PMU/HDA/SMBUS/DMIC

Size	Document Number	Rev
Custom	EH50F M/B LA-H431PR10	1.0

Date: Wednesday, February 13, 2019 Sheet 18 of 100



VGA ID	VGA_ID2 GPP_D10	VGA_ID1 GPP_D9
Default	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
EH50F(2060 WO RD)	0	0
EH50F(2060 W RD)	0	1
EH5VF(2050 WO RD)	1	0
EH5VF(2050 W RD)	1	1

SCI capability is available on all GPIOs
PCH GPIOs that can be routed to generate SMI# or NMI:
- GPP_B14, GPP_B20, GPP_B23
- GPP_C[23:22]
- GPP_D[4:0]
- GPP_E[8:0]
- GPP_I[3:0]
- GPP_G[7:0] (support SMI# only).

The voltage of all GPIO pads in each GPP group is determined by the voltage supplied to the group (either 3.3V or 1.8V), except for GPP_I and GPD group, (which are 3.3V only), and GPP_J group (which is 1.8V only).

All GPIOs have programmable internal pull-up/pull-down resistors which are off by default.
The internal pull-up/pull-down for each GPIO can be enabled by BIOS programming.

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: PCH(6/8)GPIO/I2C/UART/STRAP

Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 19 of 100

GPIO Group	Voltage
GPPA	3.3V
GPPB GPPC	3.3V
GPPD	3.3V * 1.8V
GPPE GPPF	3.3V
GPPG	3.3V
GPPH GPPK	3.3V
GPPI	3.3V Only
GPPJ	1.8V Only
GPD	3.3V Only

3-5MM FROM PACKAGE EDGE

place near VCCDUSB FOR W22/W23

1-3MM FROM PACKAGE VCCPRIM_MPHY W31

1-3MM FROM PACKAGE EDGE

1-5MM FROM PACKAGE EDGE FOR VCCAPLL C1/C2

1-3MM FROM PACKAGE EDGE FOR VCCA_BCLK V19

1-5MM FROM PACKAGE EDGE FOR VCCAPLL B1/B2/B3

1-3MM FROM PACKAGE EDGE

LC filter colse to pin

1uF 1-3MM FROM PACKAGE EDGE

reserve filter folloe CRB 8/21

1-3MM FROM PACKAGE FOR PGPPEF AE35/AE37

1-3MM FROM PACKAGE FOR PGPPHK AC35/AC36

1-3MM FROM PACKAGE FOR VCCPRIM AY8/BB7

V/VX : use un-chargeable RTC

RTC Battery

EH50F : change to 1k (follow Intel DG)

CONN@ SP02000RO00

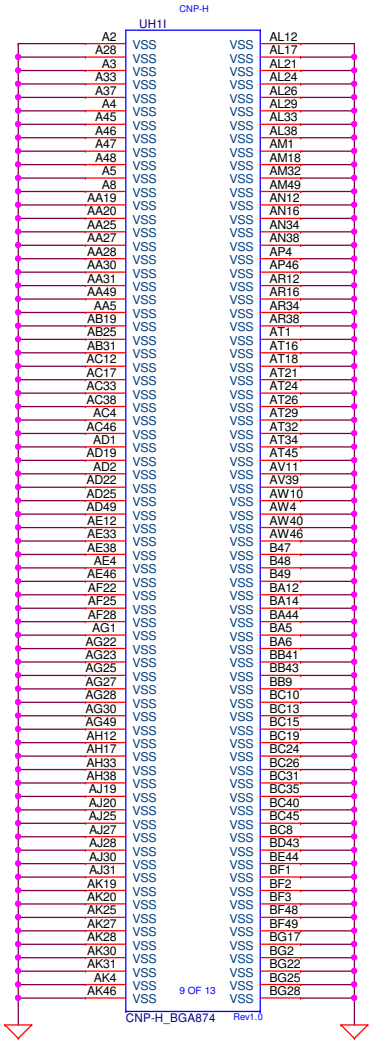
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

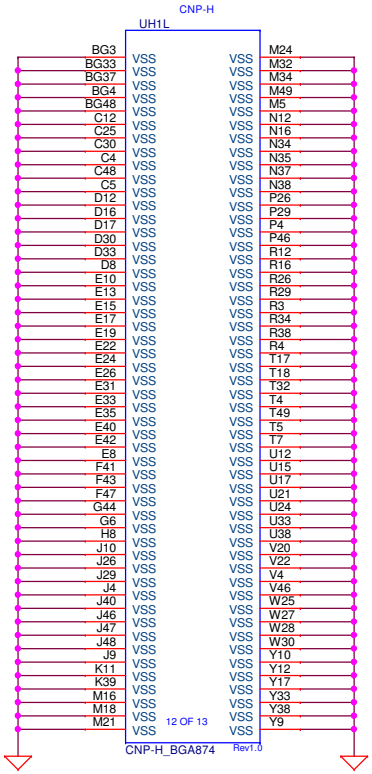
Compal Electronics, Inc.

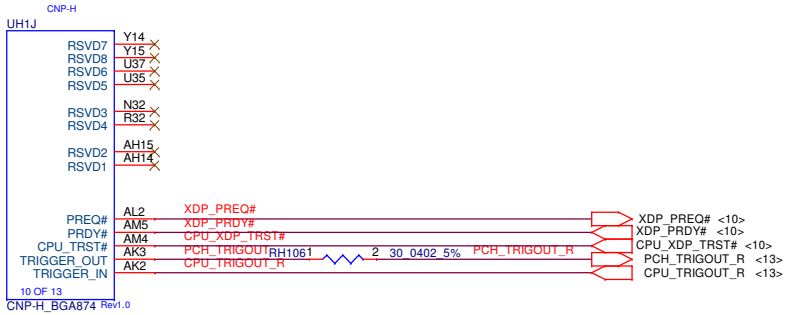
Title: PCH(7/8)Power

Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 20 of 100







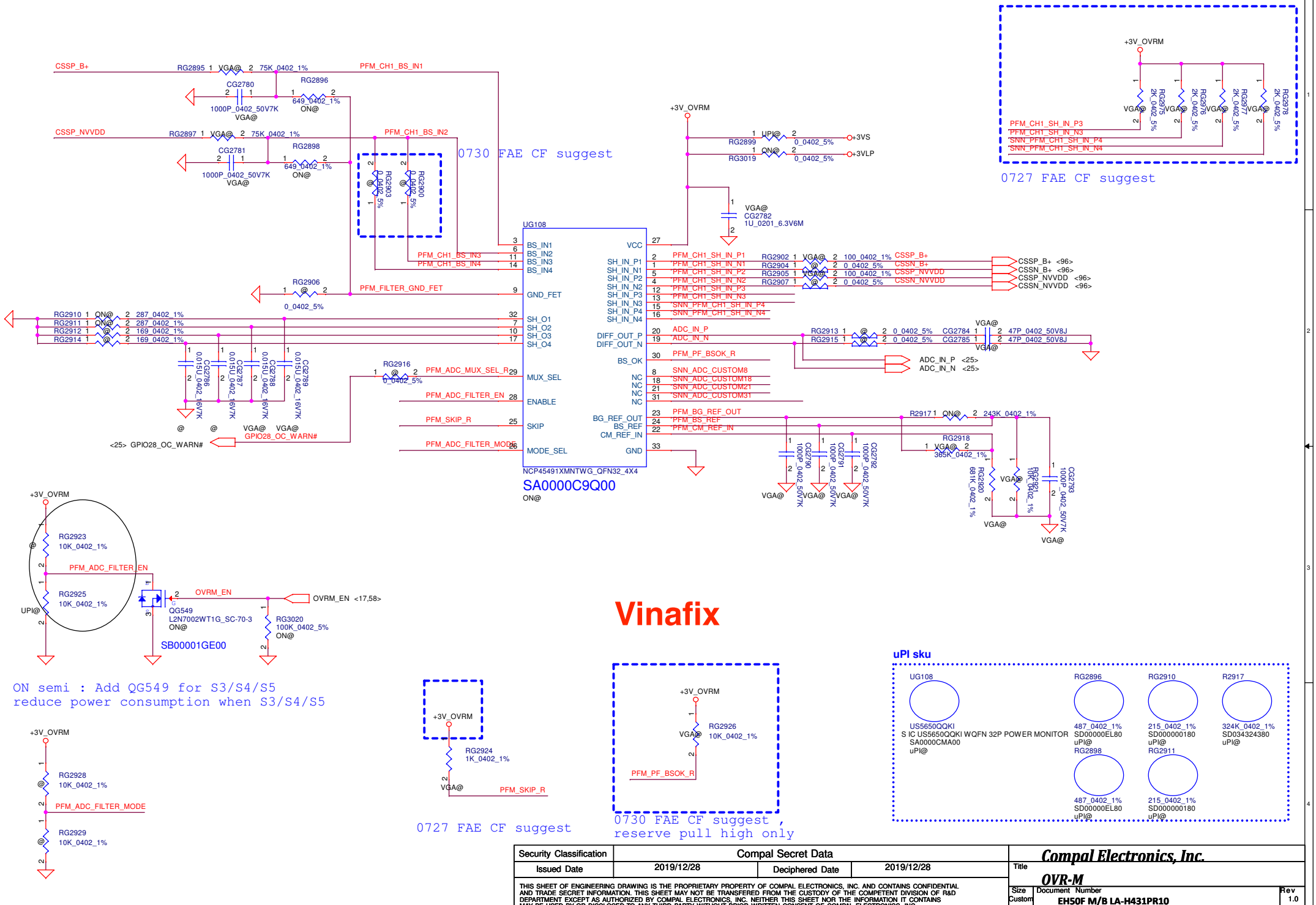
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: PCH(8/8)GND/RSVD

Size	Document Number	Rev
Custom	EH50F M/B LA-H431PR10	1.0

Date: Wednesday, February 13, 2019 Sheet 21 of 100



Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: **OVR-M**

Size	Document Number	Rev
Custom	EH50F M/B LA-H431PR10	1.0

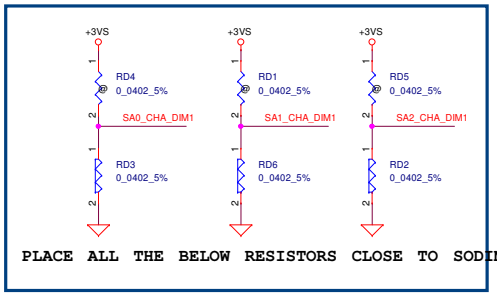
Date: Wednesday, February 13, 2019 Sheet 22 of 100

CHANNEL-A

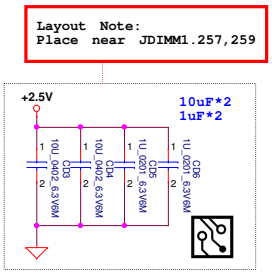
BOT REVERSE (4mm)

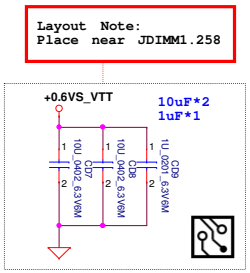
Interleaved Memory

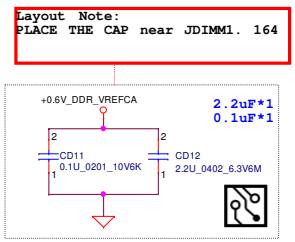
TOP: JDIMM1 CONN Non-ECC DIMM

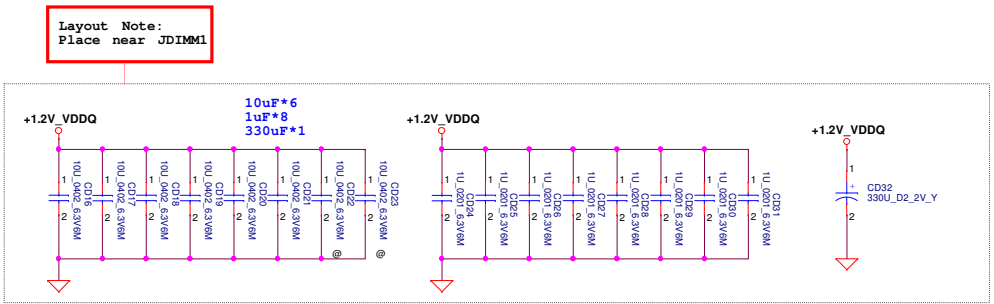


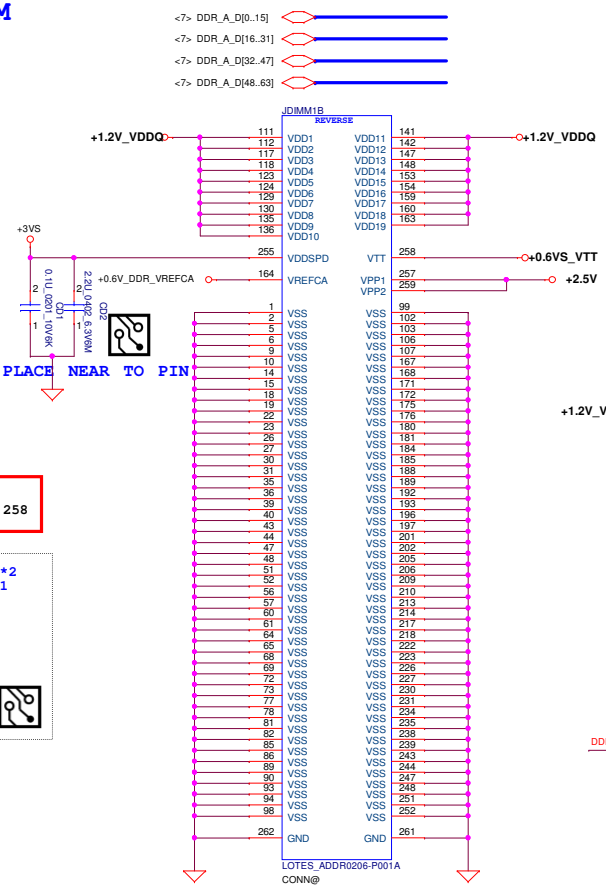
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S



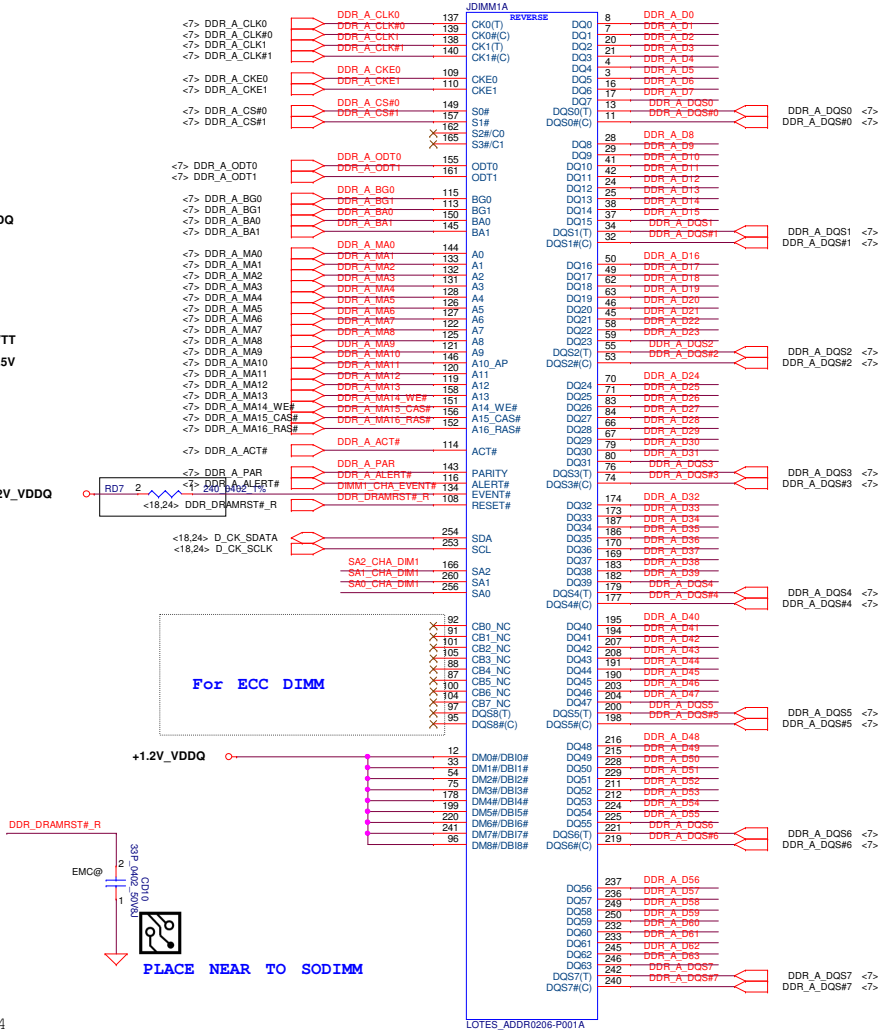


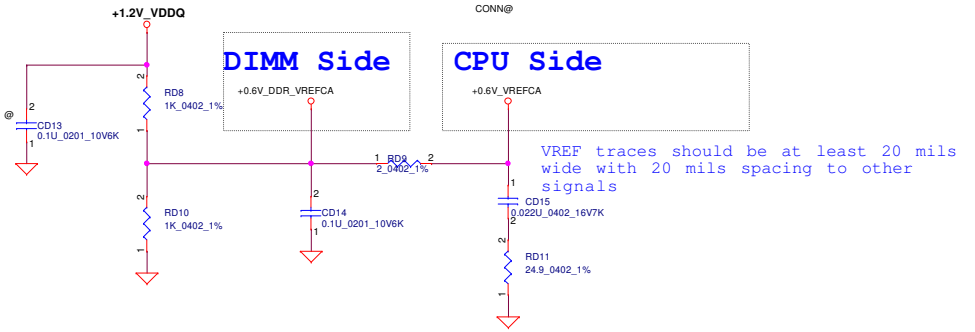






Part Number:SP07001CY00
Part Value:S SOCKET LOTES ADDR0206-P001A 260P DDR4





Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

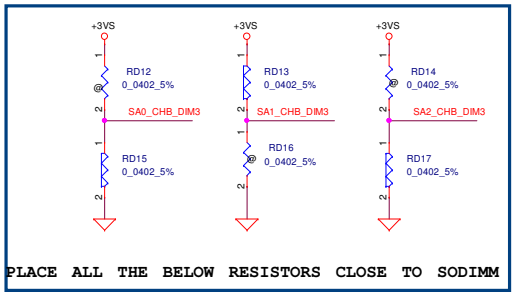
Compal Electronics, Inc.			
Title	DDRIV_CHA: DIMM0		
Size	Document Number		Rev
	EH50F M/B LA-H431PR10		1.0
Date: Wednesday, February 13, 2019	Sheet 23 of 100		

CHANNEL-B

BOT STD (4mm)

Interleaved Memory

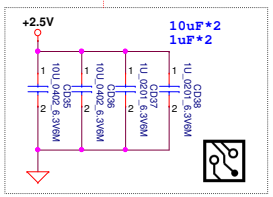
TOP: JDIMM2 CONN Non-ECC DIMM



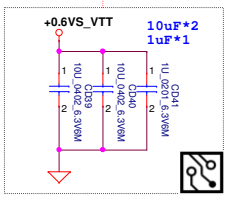
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

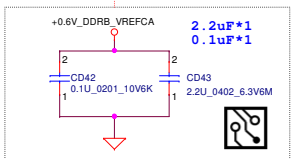
Layout Note:
Place near JDIMM2.257,259



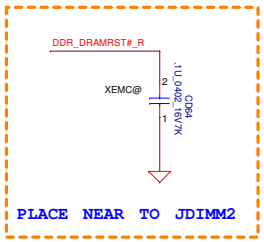
Layout Note:
Place near JDIMM2.258



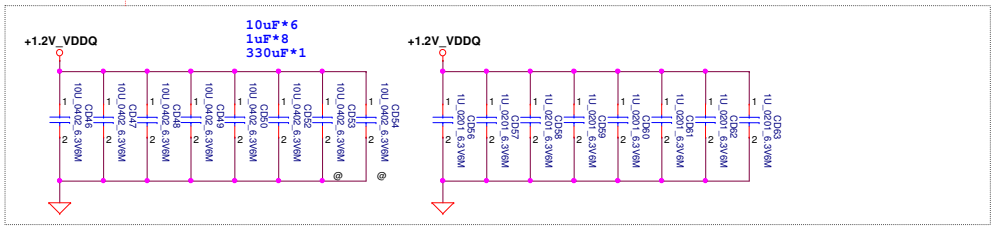
Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2

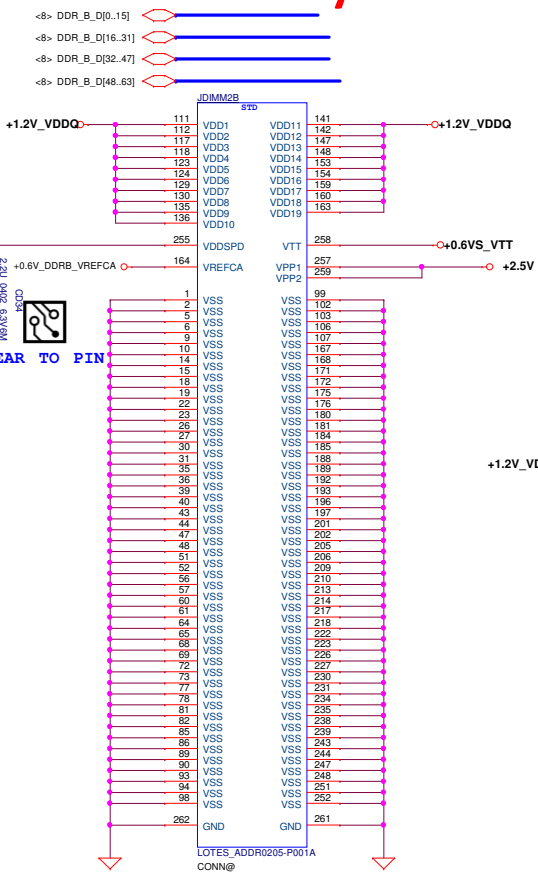


Raptor

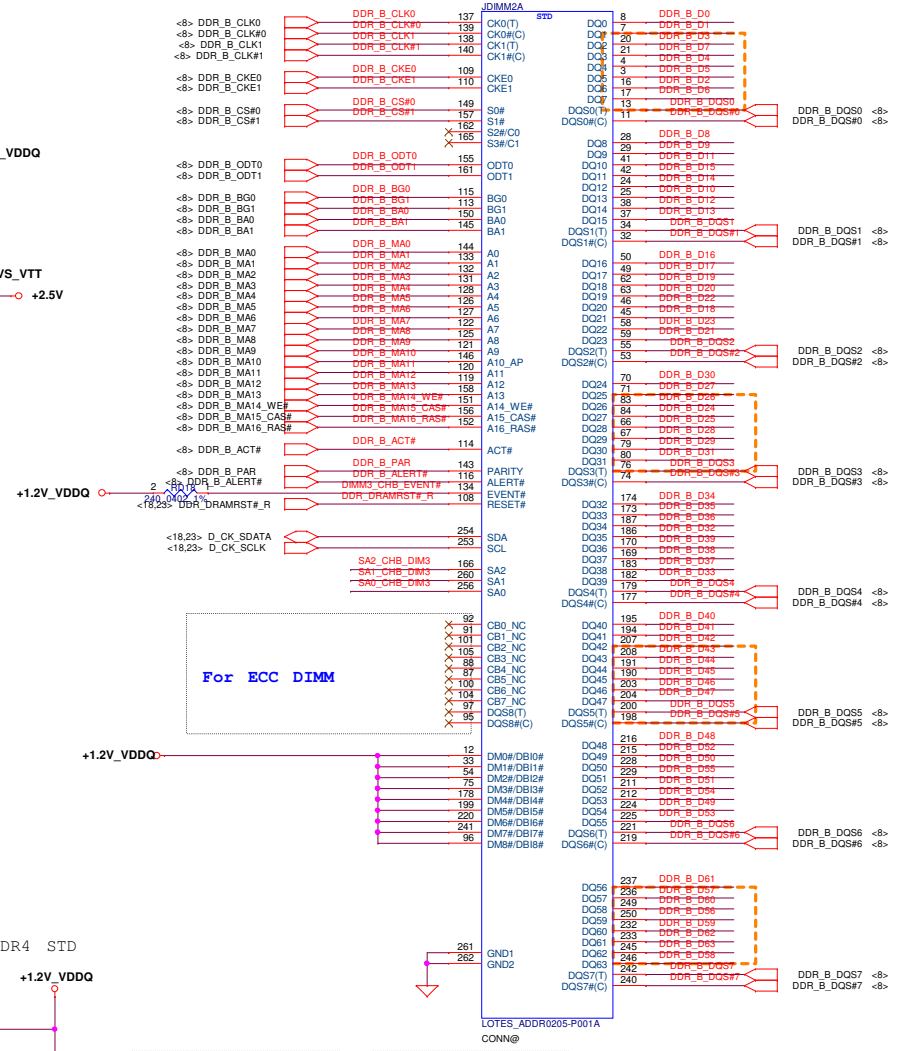


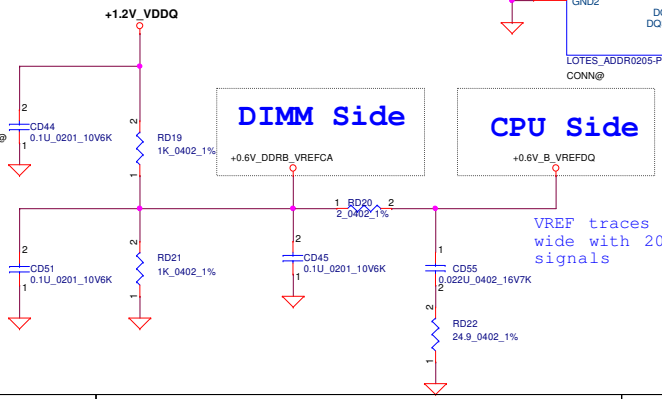
Layout Note:
Place near JDIMM2





Part Number: SP07001HW00
Part Value: S SOCKET LOTES ADDR0205-P001A DDR4 STD





VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

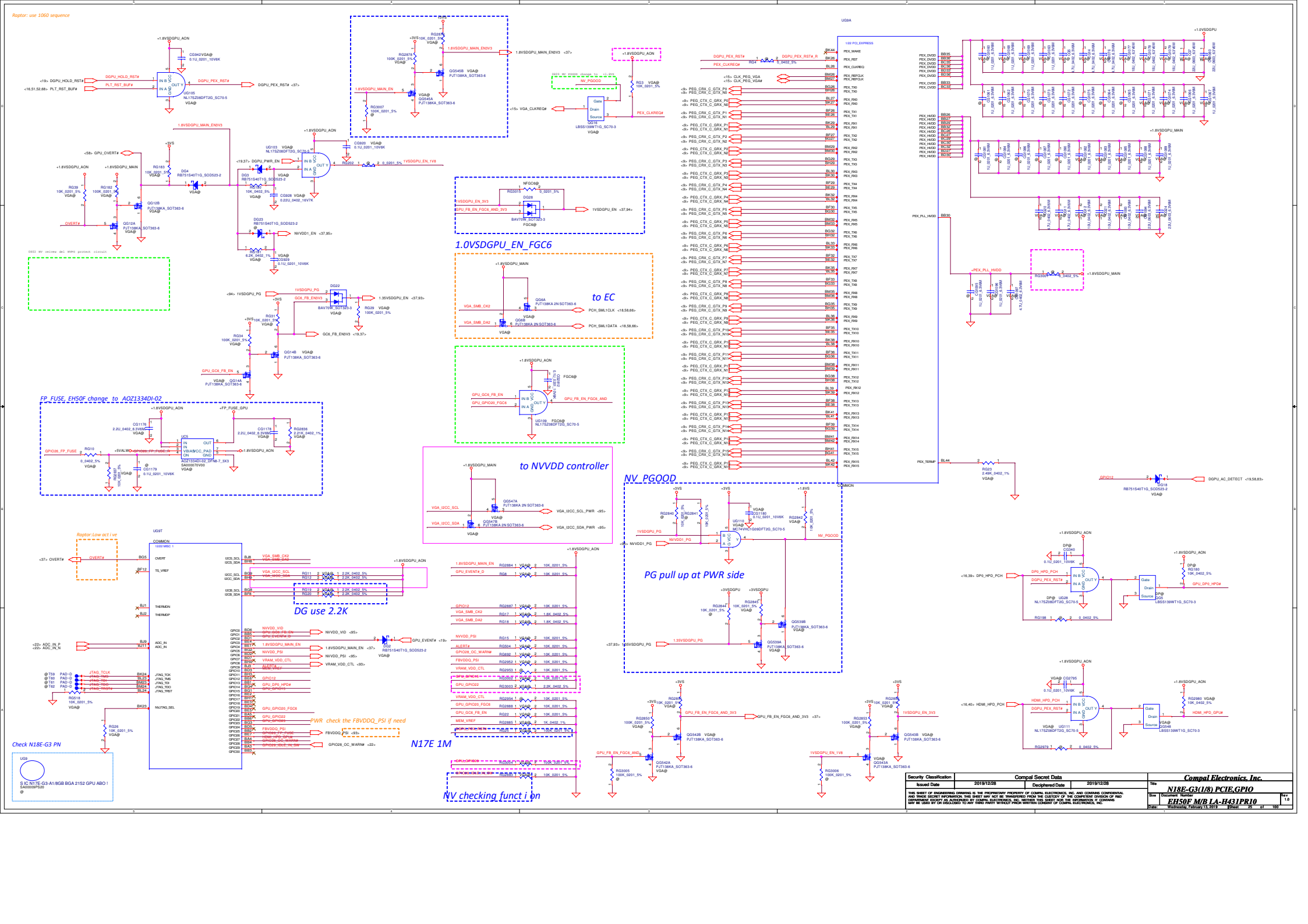
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

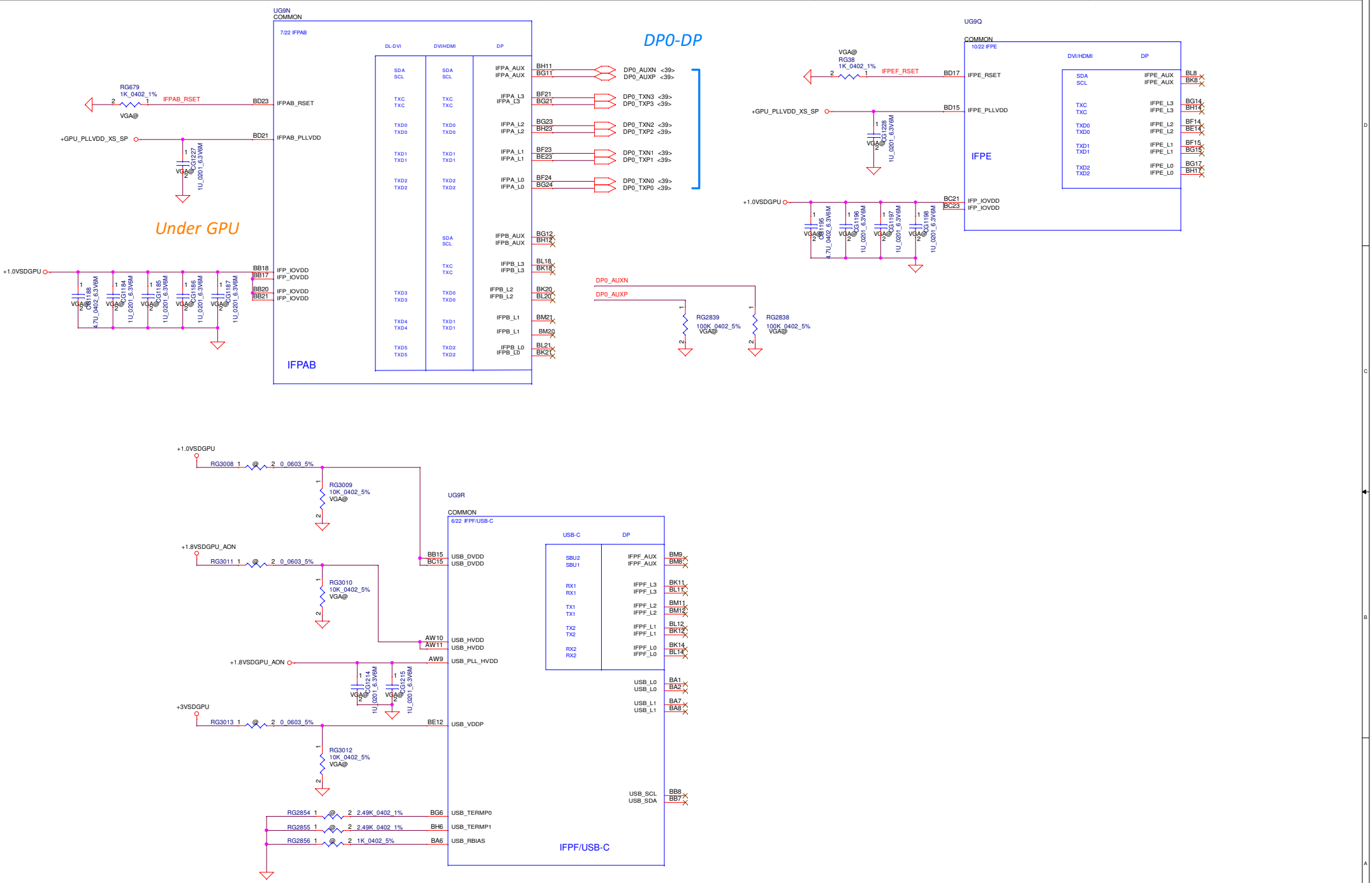
Compal Electronics, Inc.

Title: **DDRIV_CHB: DIMM0**

Size | Document Number: **EH50F M/B LA-H431PR10** | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 24 of 100


Raptor: use 1060 sequence
1.0VSDGPU_EN_FGC6
to EC
to NVVDD controller
NV_PGOOD
PG pull up at PWR side
FP_FUSE_EH50F change to AOZ1334DI-02
DG use 2.2K
N17E 1M
NV checking funct i on
PWR check the FBVDDQ_PSI if need
Check N18E-G3 PN
Raptor:Low act i ve
Compal Electronics, Inc.
N18E-G3(1/8) PCIE,GPIO
EH50F M/B LA-H431PR10
Compal Secret Data
Issued Date 2019/12/28
Deciphered Date 2019/12/28
Wednesday, February 13, 2019



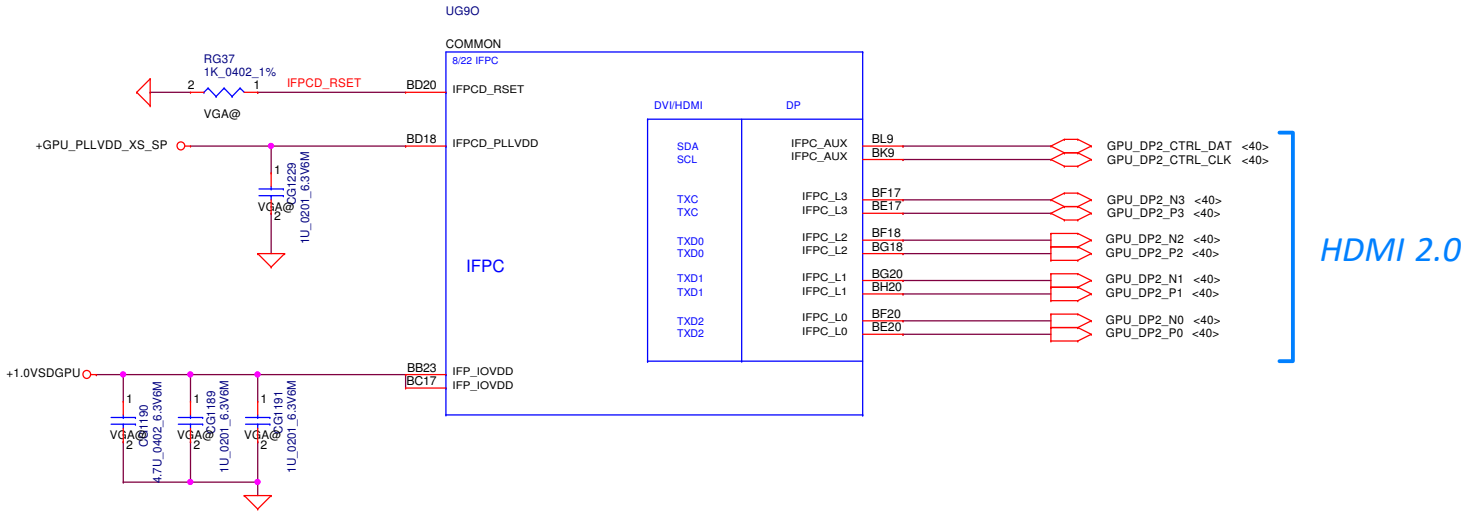
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

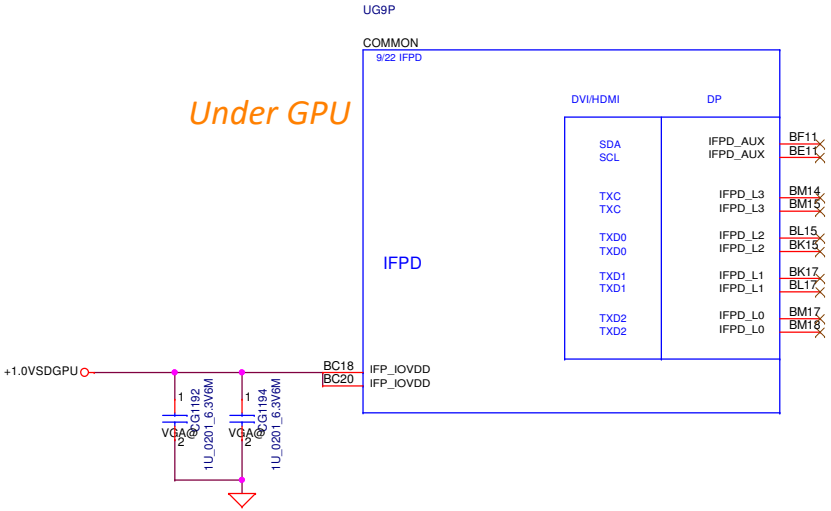
Compal Electronics, Inc.

Title: **N18E-G3(2/8) DP**

Size	Document Number	Rev
	EH50F M/B LA-H431PR10	1.0

Date: Wednesday, February 13, 2019 | Sheet 26 of 100





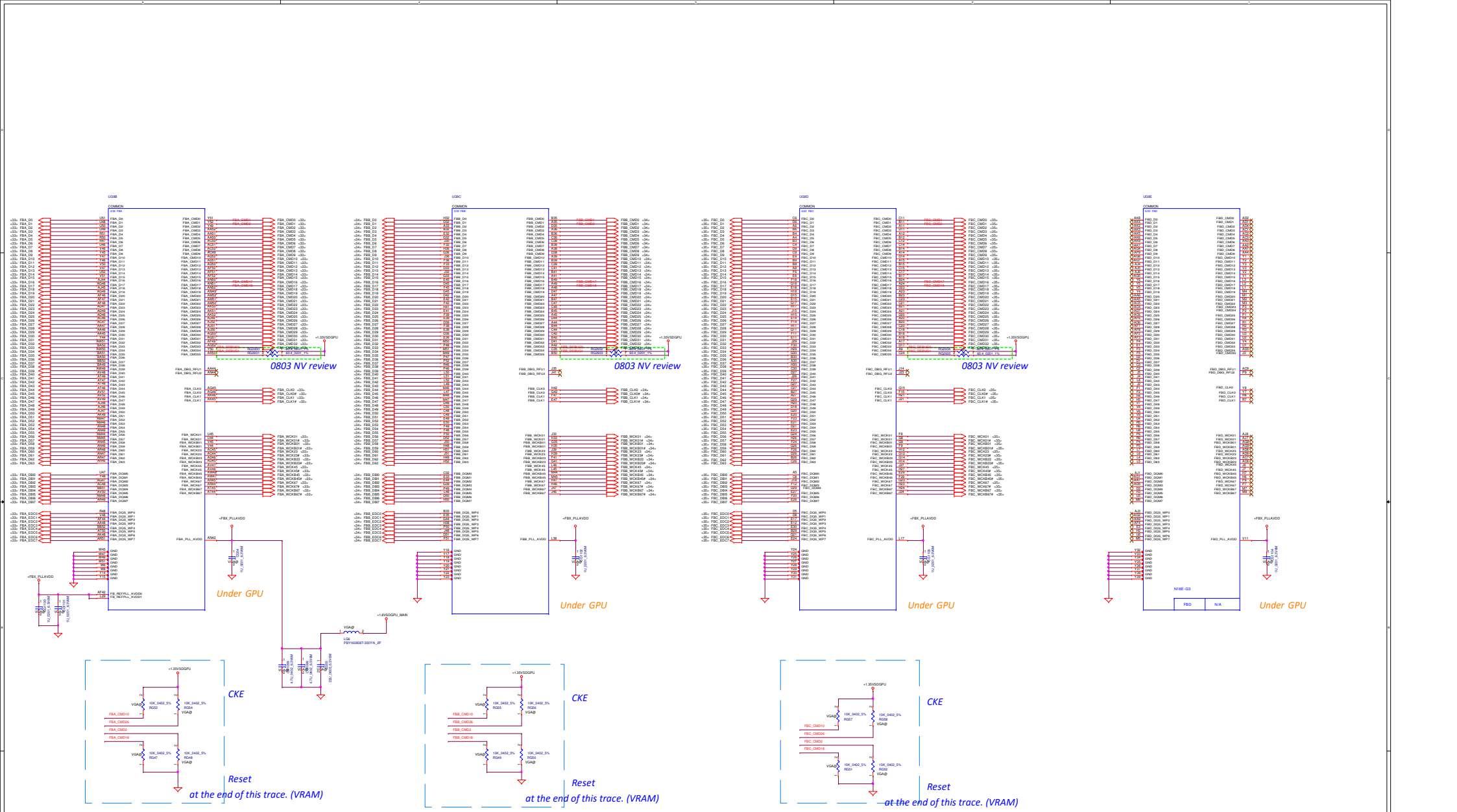
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: **N18E-G3(3/8) eDP,HDMI**

Size | Document Number: **EH50F M/B LA-H431PR10** | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 27 of 100



Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

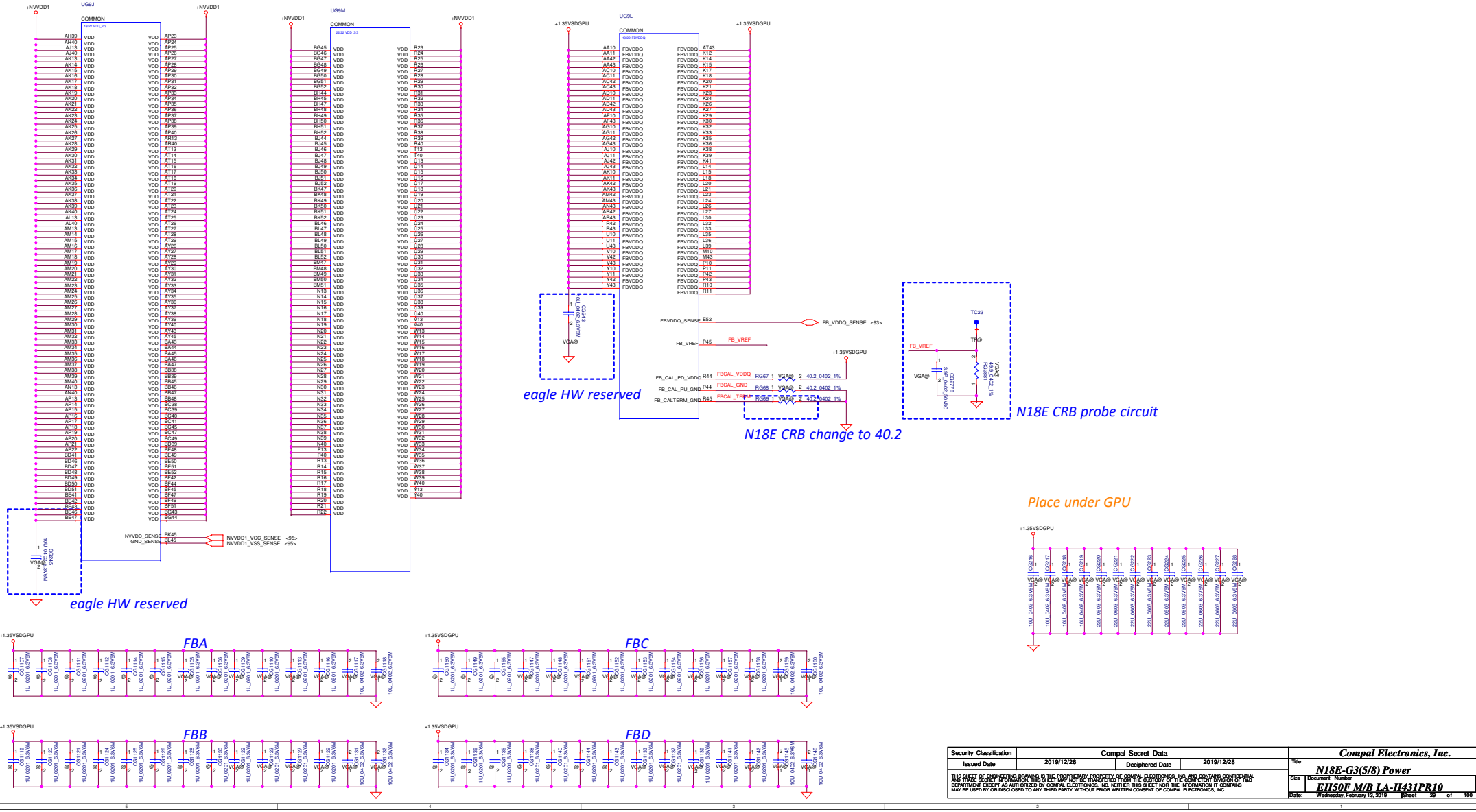
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: N18E-G3(4/8) MEM

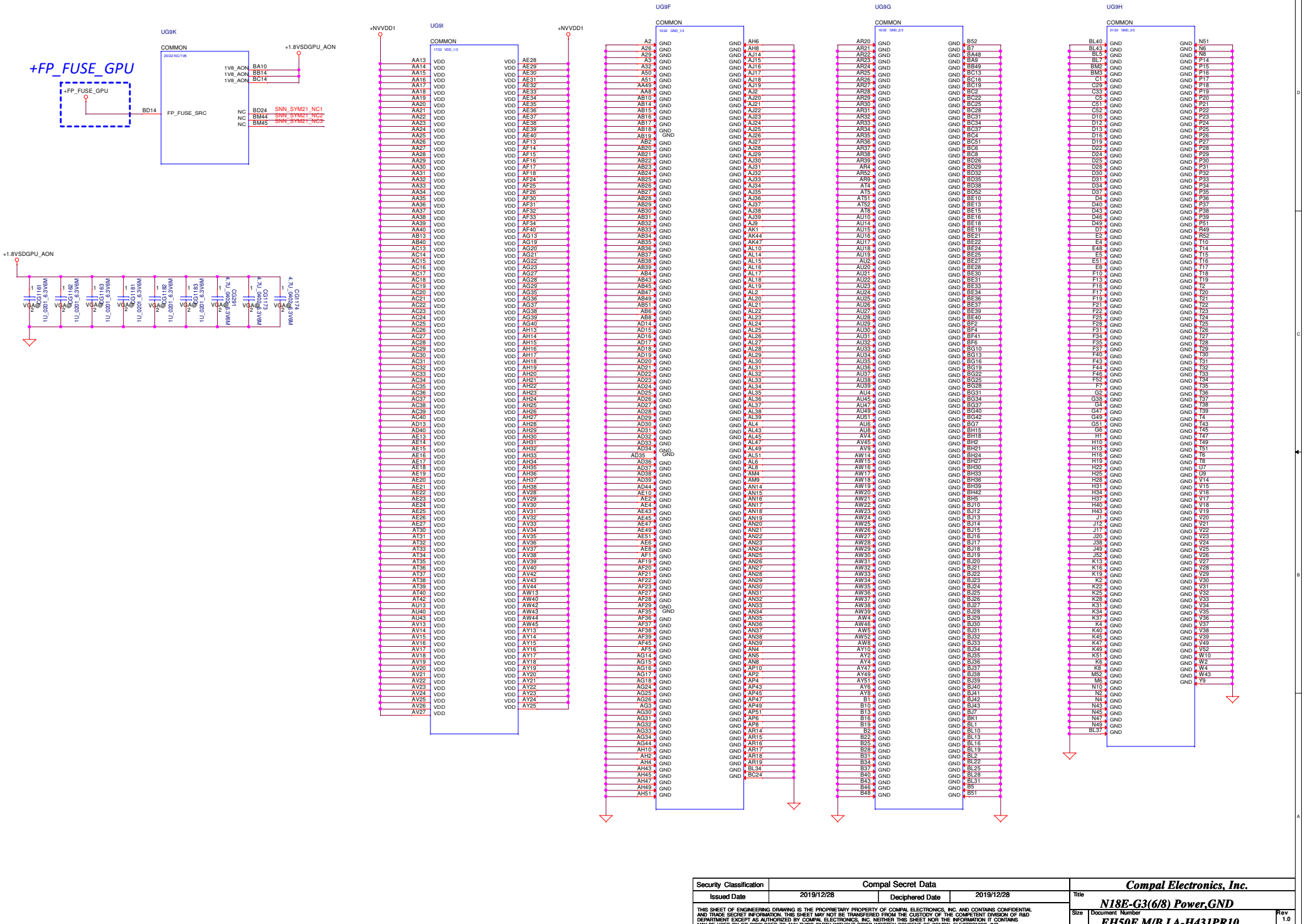
Size: C | Document Number: EH50P M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 5, 2020 | Sheet 38 of 59



Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.	
Title	N18E-G3(5/8) Power
Size	Document Number: EH50F M/B LA-H431PR10
Rev	1.0
Date:	Wednesday, February 13, 2019
Sheet	29 of 100



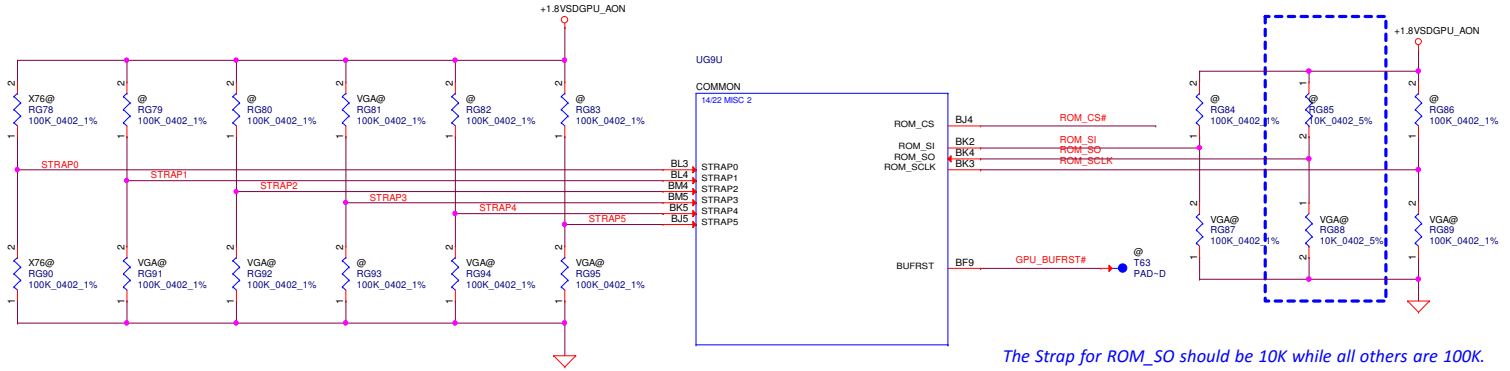
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: **N18E-G3(6/8) Power,GND**

Size: | Document Number: **EH50F M/B LA-H431PR10** | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 30 of 100



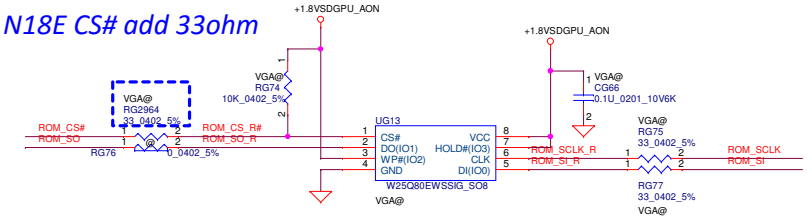
G-sync with VGA device	Strap0 (LSB)	Strap1	Strap2	Strap3 (MSB)	Strap4 (LSB)	Strap5 (MSB)	ROM_SO	ROM_SI	ROM_SCLK
Samsung K4Z80325BC-HC14	PD 100kOhm	PD 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 10kOhm	PD 100kOhm	PD 100kOhm
MICRON MT61K256M32JE-14:A	PU 100kOhm	PD 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 10kOhm	PD 100kOhm	PD 100kOhm

Table 1. N18E-G3 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V*	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Notes:
1. For N18E-G3, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCK: TBD

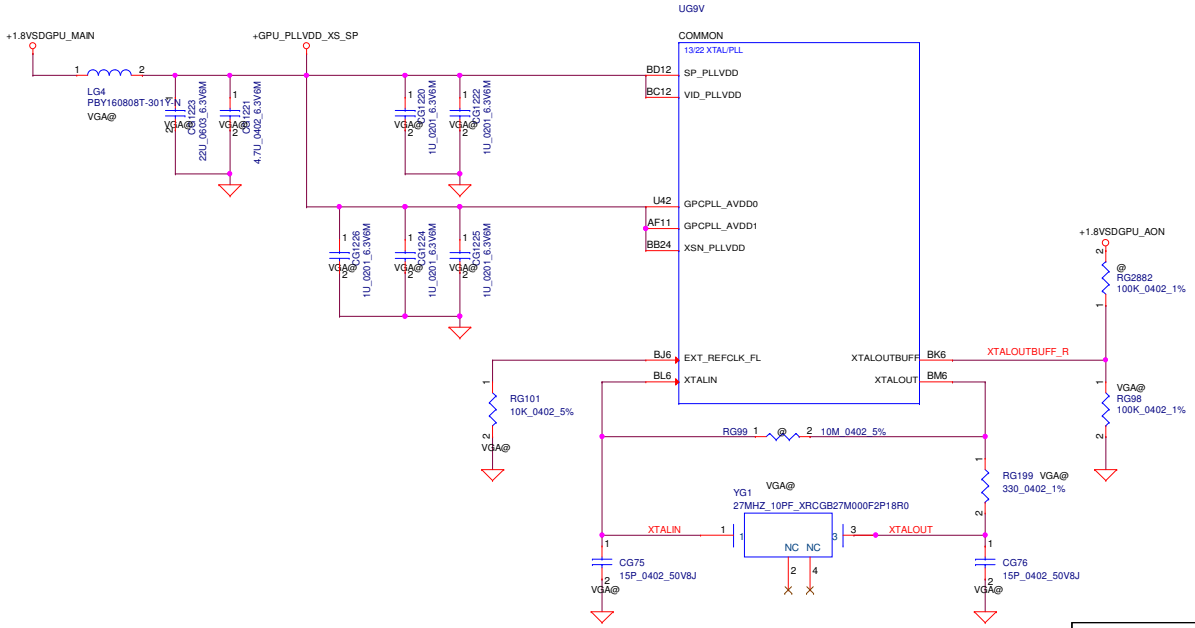
N18E CS# add 33ohm



DGPU VBIOS ROM 8Mb

P/N: SA00009QP00

Vinafix



Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

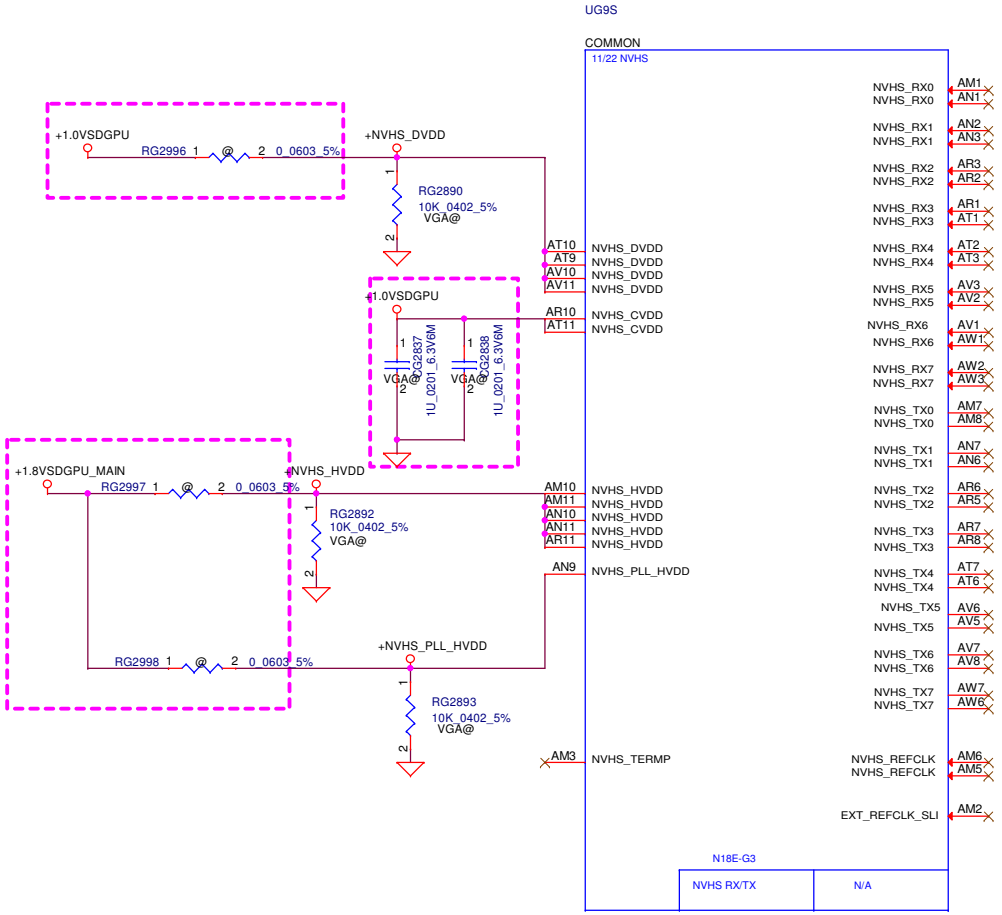
Compal Electronics, Inc.

Title: **N18E-G3(7/8) Strap,ROM**

Size	Document Number	Rev
	EH50F M/B LA-H431PR10	1.0

Date: Wednesday, February 13, 2019 | Sheet 31 of 100

Pull down NVHS_DVDD, NVHS_CVDD, NVHS_HVDD, NVHS_PLL_HVDD rails to GND with 10K Resistor



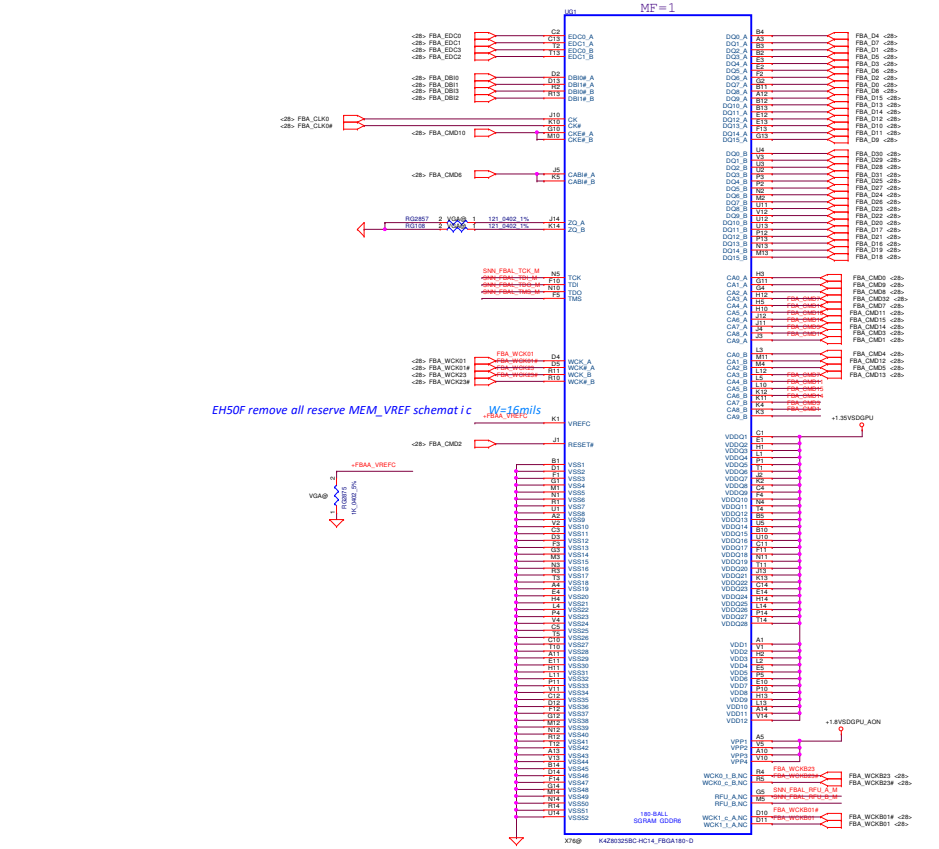
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

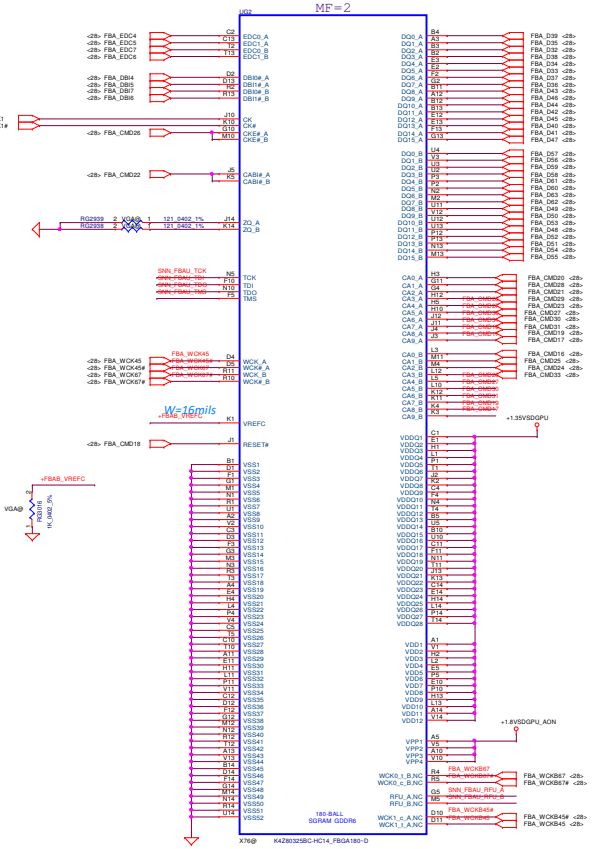
Compal Electronics, Inc.

Title: ***N18E-G3(8/8) NVLINK***

Size | Document Number: ***EH50F M/B LA-H431PR10*** | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 32 of 100





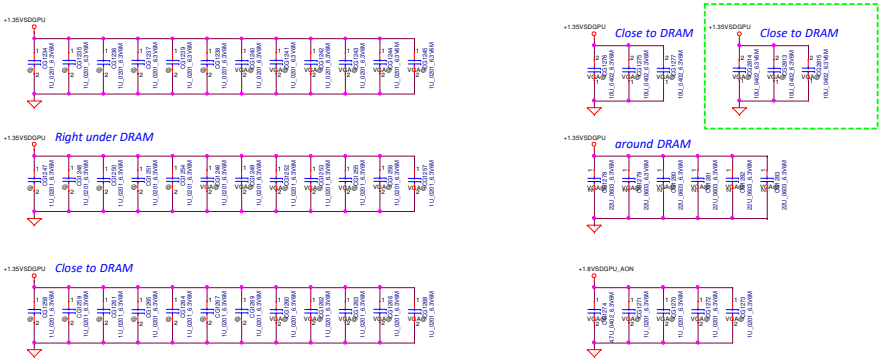
GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [3]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD0	Bytes 0,1: CA0_A Bytes 2,3: -------	FBx_CMD16	Bytes 4,5: ------- Bytes 6,7: CA0_B
FBx_CMD1	Bytes 0,1: CA9_A Bytes 2,3: CA9_B	FBx_CMD17	Bytes 4,5: CA9_A Bytes 6,7: CA9_B
FBx_CMD2	Byte 0-3: RST#	FBx_CMD18	Bytes 4-7: RST#
FBx_CMD3	Bytes 0,1: CA8_A Bytes 2,3: CA8_B	FBx_CMD19	Bytes 4,5: CA8_A Bytes 6,7: CA8_B
FBx_CMD4	Bytes 0,1: ------- Bytes 2,3: CA0_B	FBx_CMD20	Bytes 4,5: CA0_A Bytes 6,7: -------
FBx_CMD5	Bytes 0,1: ------- Bytes 2,3: CA2_B	FBx_CMD21	Bytes 4,5: CA2_A Bytes 6,7: -------
FBx_CMD6	Bytes 0,1: CABI_A Bytes 2,3: CABI_B	FBx_CMD22	Bytes 4,5: CABI_A Bytes 6,7: CABI_B

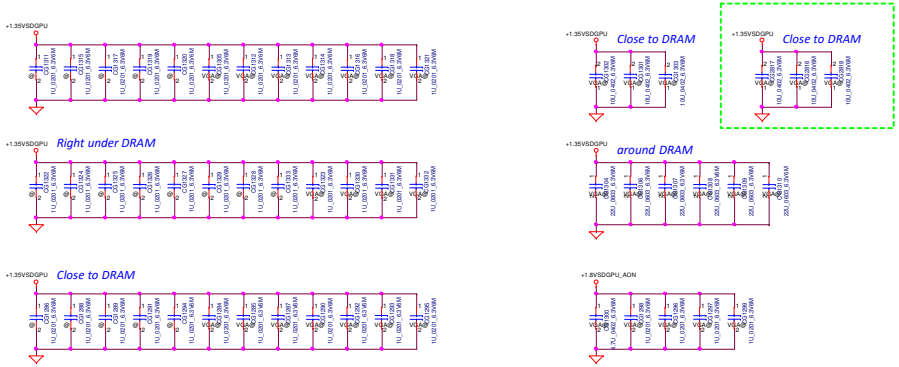
GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [3]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD7	Bytes 0,1: CA4_A Bytes 2,3: CA4_B	FBx_CMD23	Bytes 4,5: CA4_A Bytes 6,7: CA4_B
FBx_CMD8	Bytes 0,1: CA2_A Bytes 2,3: -------	FBx_CMD24	Bytes 4,5: ------- Bytes 6,7: CA2_B
FBx_CMD9	Bytes 0,1: CA1_A Bytes 2,3: -------	FBx_CMD25	Bytes 4,5: ------- Bytes 6,7: CA1_B
FBx_CMD10	Bytes 0,1: CKE'_A Bytes 2,3: CKE'_B	FBx_CMD26	Bytes 4,5: CKE'_A Bytes 6,7: CKE'_B
FBx_CMD11	Bytes 0,1: CA5_A Bytes 2,3: CA5_B	FBx_CMD27	Bytes 4,5: CA5_A Bytes 6,7: CA5_B
FBx_CMD12	Bytes 0,1: ------- Bytes 2,3: CA1_B	FBx_CMD28	Bytes 4,5: CA1_A Bytes 6,7: -------
FBx_CMD13	Bytes 0,1: ------- Bytes 2,3: CA3_B	FBx_CMD29	Bytes 4,5: CA3_A Bytes 6,7: -------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [3]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD14	Bytes 0,1: CA7_A Bytes 2,3: CA7_B	FBx_CMD30	Bytes 4,5: CA6_A Bytes 6,7: CA6_B
FBx_CMD15	Bytes 0,1: CA6_A Bytes 2,3: CA6_B	FBx_CMD31	Bytes 4,5: CA7_A Bytes 6,7: CA7_B
FBx_CMD32	Bytes 0,1: CA3_A Bytes 2,3: -------	FBx_CMD33	Bytes 4,5: ------- Bytes 6,7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0 [1]
FBx_CMD35	DEBUG1 [1]

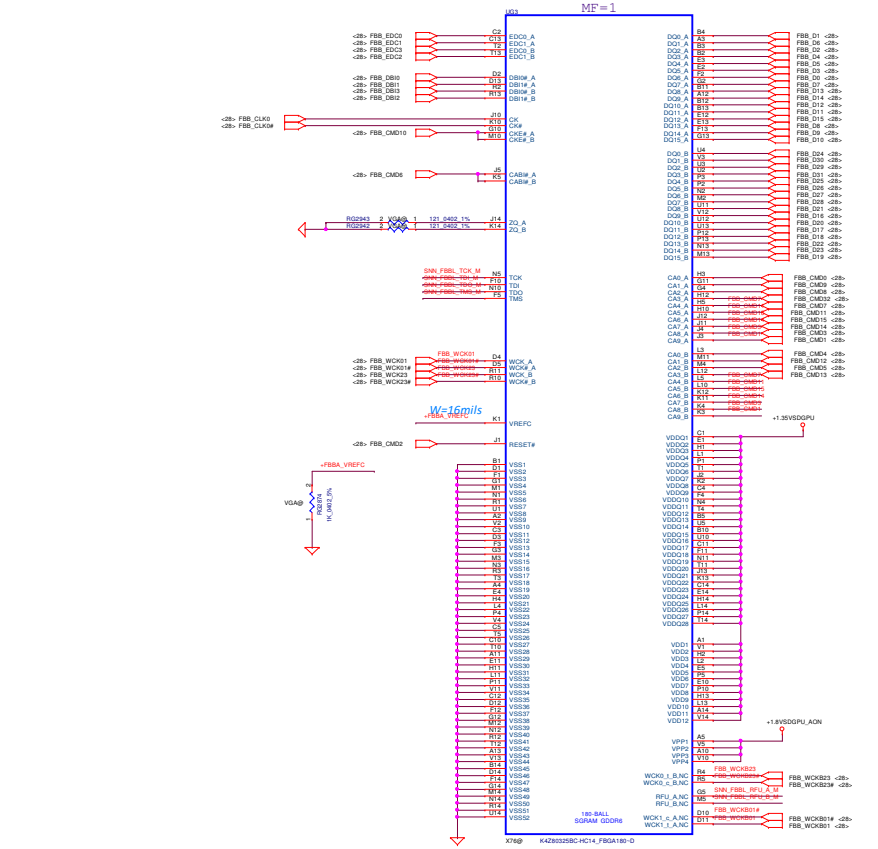
Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

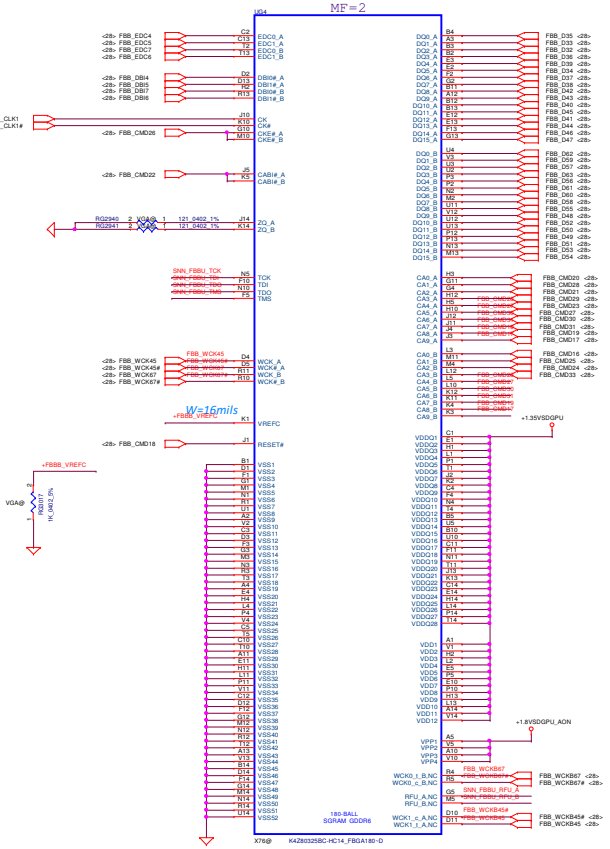




Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.	
Title	N18E-GDDR6_A
Size	Document Number: EH50F M/B LA-H431PR10
Rev	1.0
Date: Wednesday, February 13, 2019	Sheet 33 of 100





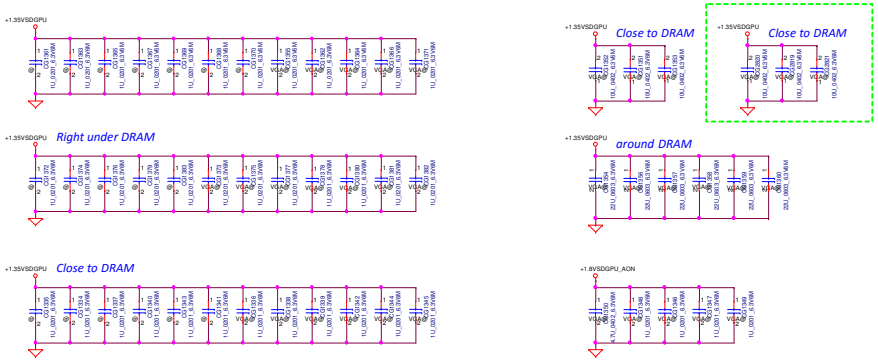
GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD0	Bytes 0, 1: CA0_A Bytes 2, 3: -------	FBx_CMD16	Bytes 4, 5: ------- Bytes 6, 7: CA0_B
FBx_CMD1	Bytes 0, 1: CA9_A Bytes 2, 3: CA9_B	FBx_CMD17	Bytes 4, 5: CA9_A Bytes 6, 7: CA9_B
FBx_CMD2	Bytes 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0, 1: CA8_A Bytes 2, 3: CA8_B	FBx_CMD19	Bytes 4, 5: CA8_A Bytes 6, 7: CA8_B
FBx_CMD4	Bytes 0, 1: ------- Bytes 2, 3: CA0_B	FBx_CMD20	Bytes 4, 5: CA0_A Bytes 6, 7: -------
FBx_CMD5	Bytes 0, 1: ------- Bytes 2, 3: CA2_B	FBx_CMD21	Bytes 4, 5: CA2_A Bytes 6, 7: -------
FBx_CMD6	Bytes 0, 1: CA8I_A Bytes 2, 3: CA8I_B	FBx_CMD22	Bytes 4, 5: CA8I_A Bytes 6, 7: CA8I_B

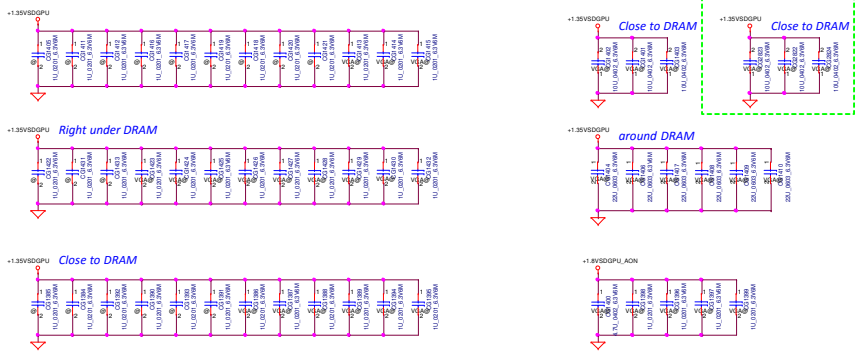
GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD7	Bytes 0, 1: CA4_A Bytes 2, 3: CA4_B	FBx_CMD23	Bytes 4, 5: CA4_A Bytes 6, 7: CA4_B
FBx_CMD8	Bytes 0, 1: CA2_A Bytes 2, 3: -------	FBx_CMD24	Bytes 4, 5: ------- Bytes 6, 7: CA2_B
FBx_CMD9	Bytes 0, 1: CA1_A Bytes 2, 3: -------	FBx_CMD25	Bytes 4, 5: ------- Bytes 6, 7: CA1_B
FBx_CMD10	Bytes 0, 1: CKE*_A Bytes 2, 3: CKE*_B	FBx_CMD26	Bytes 4, 5: CKE*_A Bytes 6, 7: CKE*_B
FBx_CMD11	Bytes 0, 1: CA5_A Bytes 2, 3: CA5_B	FBx_CMD27	Bytes 4, 5: CA5_A Bytes 6, 7: CA5_B
FBx_CMD12	Bytes 0, 1: ------- Bytes 2, 3: CA1_B	FBx_CMD28	Bytes 4, 5: CA1_A Bytes 6, 7: -------
FBx_CMD13	Bytes 0, 1: ------- Bytes 2, 3: CA3_B	FBx_CMD29	Bytes 4, 5: CA3_A Bytes 6, 7: -------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD14	Bytes 0, 1: CA7_A Bytes 2, 3: CA7_B	FBx_CMD30	Bytes 4, 5: CA6_A Bytes 6, 7: CA6_B
FBx_CMD15	Bytes 0, 1: CA6_A Bytes 2, 3: CA6_B	FBx_CMD31	Bytes 4, 5: CA7_A Bytes 6, 7: CA7_B
FBx_CMD32	Bytes 0, 1: CA3_A Bytes 2, 3: -------	FBx_CMD33	Bytes 4, 5: ------- Bytes 6, 7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0 [1]
FBx_CMD35	DEBUG1 [1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

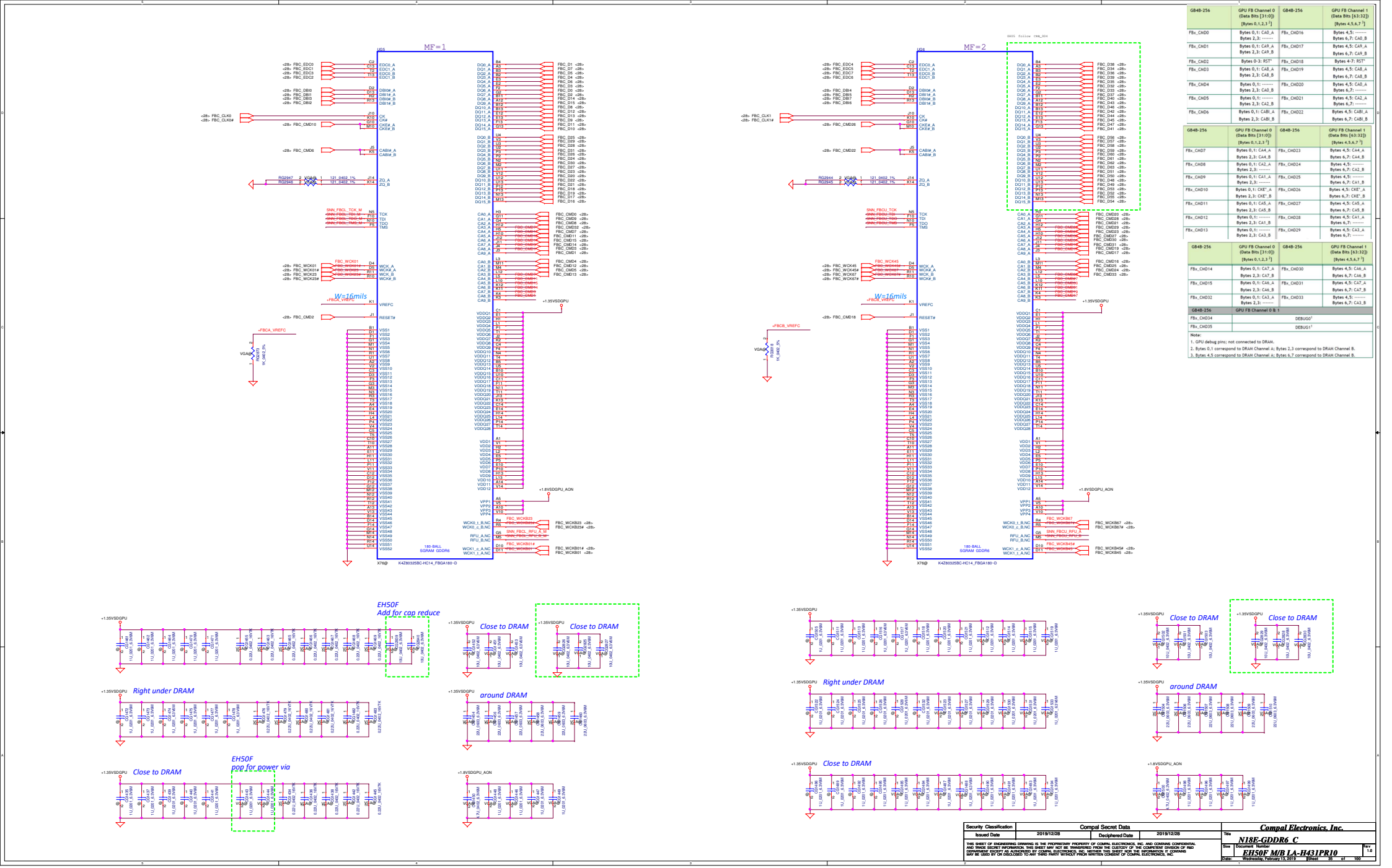




Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/12/28	Deciphered Date	2019/12/28

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Title	N18E-GDDR6_B	
Size	Document Number: EH50F M/B LA-H431PR10	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 34 of 100	



GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [1]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [1]]
FBx_CMD0	Bytes 0,1: CA0_A Bytes 2,3: -------	FBx_CMD16	Bytes 4,5: ------- Bytes 6,7: CA0_B
FBx_CMD1	Bytes 0,1: CA9_A Bytes 2,3: CA9_B	FBx_CMD17	Bytes 4,5: CA9_A Bytes 6,7: CA9_B
FBx_CMD2	Bytes 0-3: RST"	FBx_CMD18	Bytes 4-7: RST"
FBx_CMD3	Bytes 0,1: CA8_A Bytes 2,3: CA8_B	FBx_CMD19	Bytes 4,5: CA8_A Bytes 6,7: CA8_B
FBx_CMD4	Bytes 0,1: ------- Bytes 2,3: CA0_B	FBx_CMD20	Bytes 4,5: CA0_A Bytes 6,7: -------
FBx_CMD5	Bytes 0,1: ------- Bytes 2,3: CA2_B	FBx_CMD21	Bytes 4,5: CA2_A Bytes 6,7: -------
FBx_CMD6	Bytes 0,1: CA8I_A Bytes 2,3: CA8I_B	FBx_CMD22	Bytes 4,5: CA8I_A Bytes 6,7: CA8I_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [1]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [1]]
FBx_CMD7	Bytes 0,1: CA4_A Bytes 2,3: CA4_B	FBx_CMD23	Bytes 4,5: CA4_A Bytes 6,7: CA4_B
FBx_CMD8	Bytes 0,1: CA2_A Bytes 2,3: -------	FBx_CMD24	Bytes 4,5: ------- Bytes 6,7: CA2_B
FBx_CMD9	Bytes 0,1: CA1_A Bytes 2,3: -------	FBx_CMD25	Bytes 4,5: ------- Bytes 6,7: CA1_B
FBx_CMD10	Bytes 0,1: CKE"_A Bytes 2,3: CKE"_B	FBx_CMD26	Bytes 4,5: CKE"_A Bytes 6,7: CKE"_B
FBx_CMD11	Bytes 0,1: CA5_A Bytes 2,3: CA5_B	FBx_CMD27	Bytes 4,5: CA5_A Bytes 6,7: CA5_B
FBx_CMD12	Bytes 0,1: ------- Bytes 2,3: CA1_B	FBx_CMD28	Bytes 4,5: CA1_A Bytes 6,7: -------
FBx_CMD13	Bytes 0,1: ------- Bytes 2,3: CA3_B	FBx_CMD29	Bytes 4,5: CA3_A Bytes 6,7: -------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [1]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [1]]
FBx_CMD14	Bytes 0,1: CA7_A Bytes 2,3: CA7_B	FBx_CMD30	Bytes 4,5: CA6_A Bytes 6,7: CA6_B
FBx_CMD15	Bytes 0,1: CA6_A Bytes 2,3: CA6_B	FBx_CMD31	Bytes 4,5: CA7_A Bytes 6,7: CA7_B
FBx_CMD32	Bytes 0,1: CA3_A Bytes 2,3: -------	FBx_CMD33	Bytes 4,5: ------- Bytes 6,7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0[1]
FBx_CMD35	DEBUG1[1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Title	Compal Electronics, Inc.
	N18E-GDDR6_C
Size	Document Number: EH50F M/B LA-H431PR10
Rev	1.0
Date:	Wednesday, February 13, 2019
Sheet	35 of 100

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

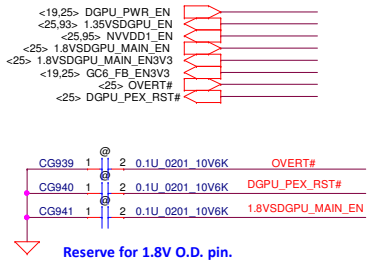
Compal Electronics, Inc.

Title: Reserve Page

Size: Document Number: EH50F M/B LA-H431PR10 Rev: 1.0

Date: Wednesday, February 13, 2019 Sheet 35 of 105

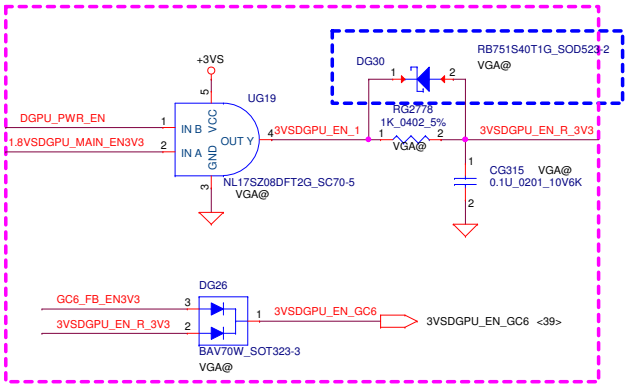
remove GPK

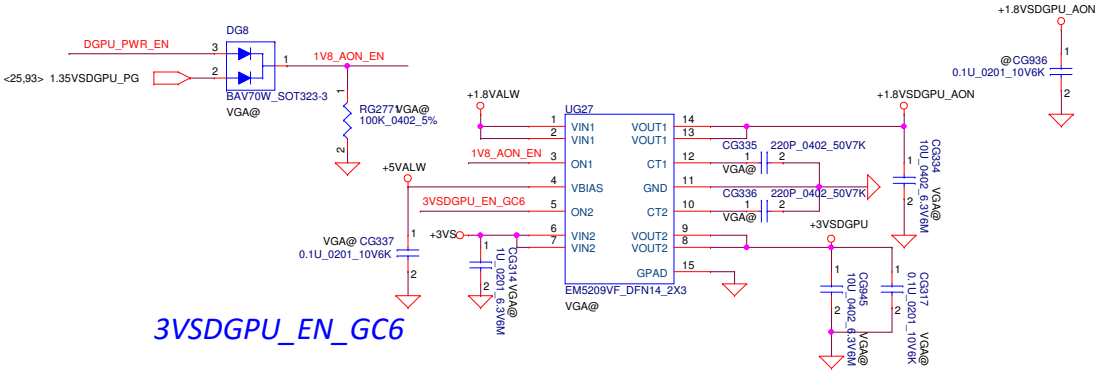


Reserve for 1.8V O.D. pin.

Vinafix

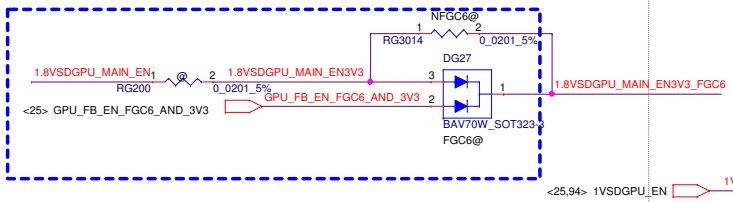
+1.8VALW to +1.8VSDGPU_AON & +3VS to +3VSDGPU



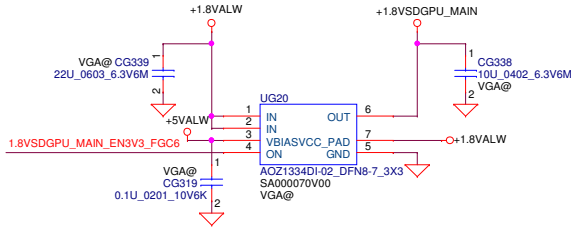


3VSDGPU_EN_GC6

+1.8VALW to +1.8VSDGPU_MAIN

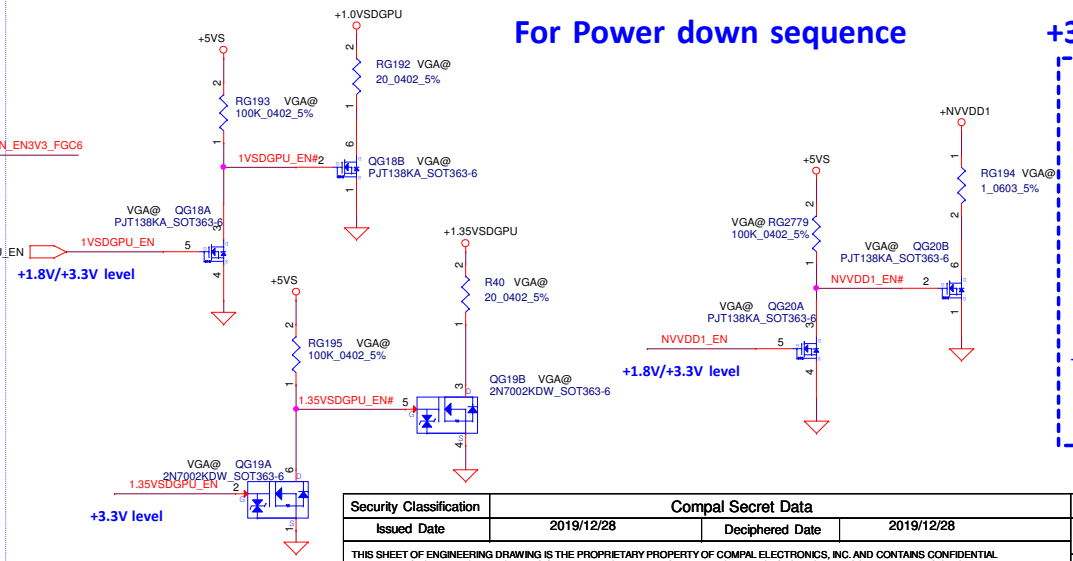


1.8VSDGPU_MAIN_EN_FGC6

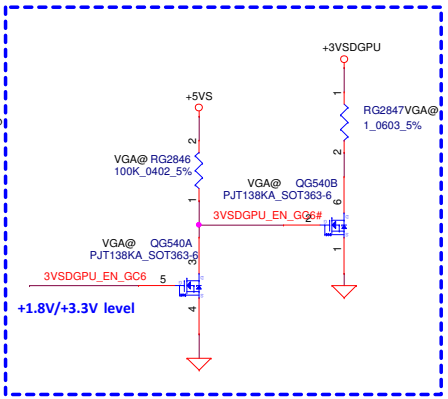


EH50F change to AOZ1334DI-02

For Power down sequence



+3VSD_GPU discharge if need



Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

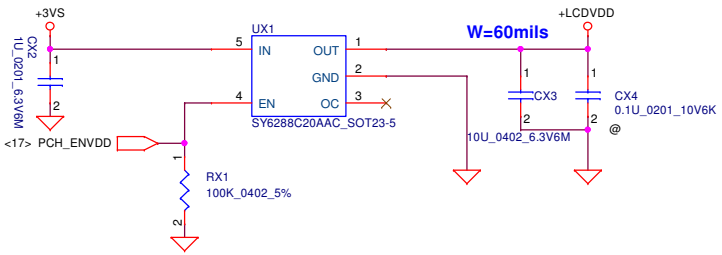
Compal Electronics, Inc.

Title: **N18E-GPU Power control**

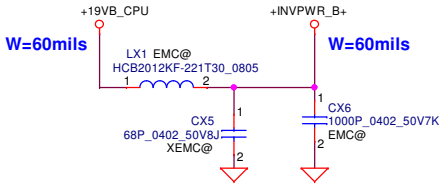
Size | Document Number: **EH50F M/B LA-H431PR10** | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 37 of 100

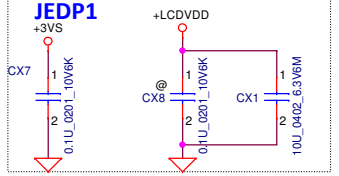
LCD POWER CIRCUIT

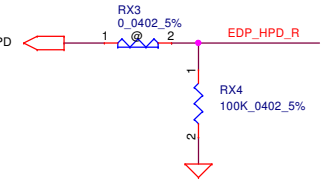


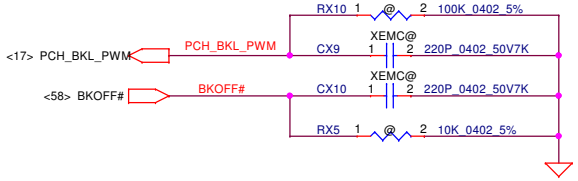
SM01000EJ00 3000ma
220ohm@100mhz
DCR 0.04

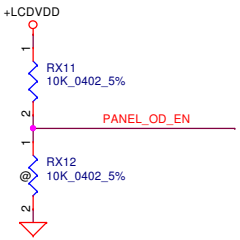


Place closed to JEDP1

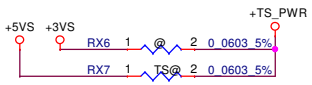




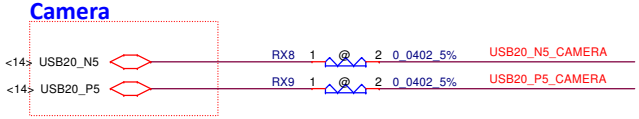




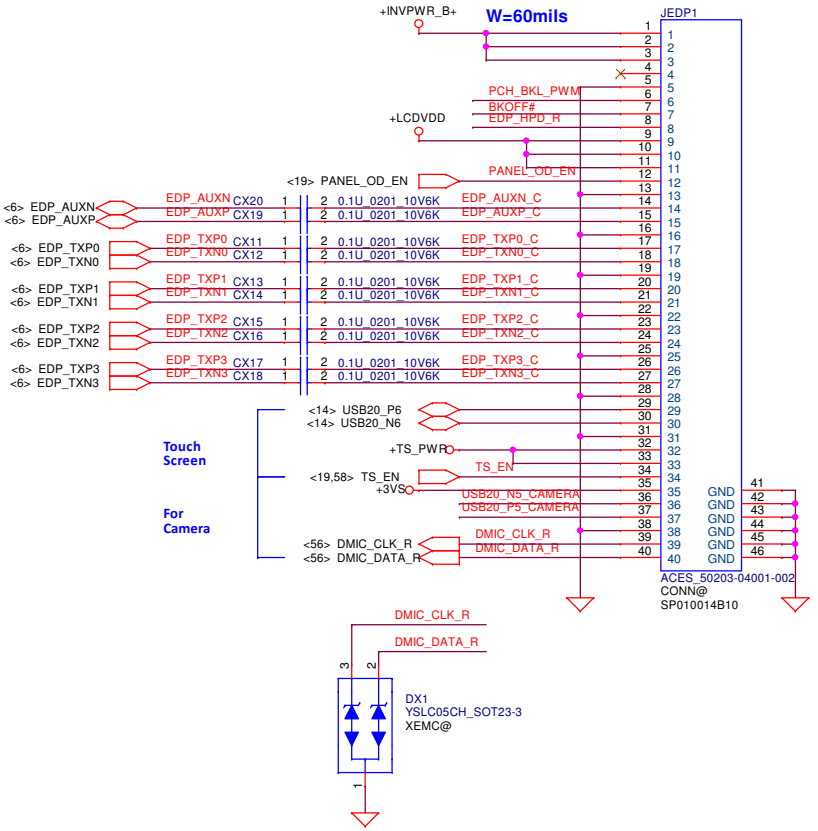
USB Touch Screen



Camera



LED PANEL Conn.



Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

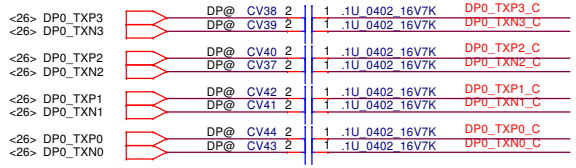
Compal Electronics, Inc.

Title: eDP CONN.

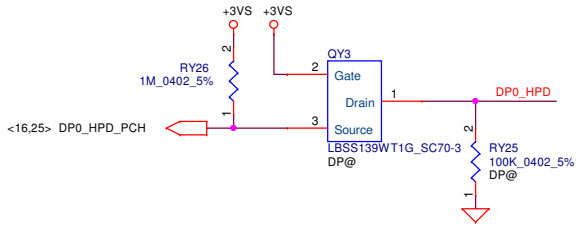
Size	Document Number	Rev
Custom	EH50F M/B LA-H431PR10	1.0

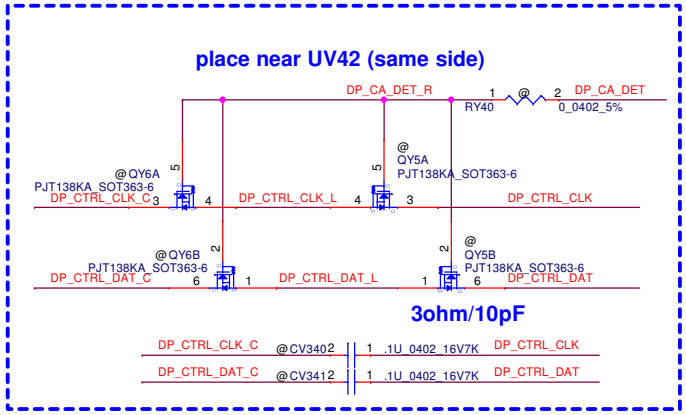
Date: Wednesday, February 13, 2019 Sheet 38 of 100

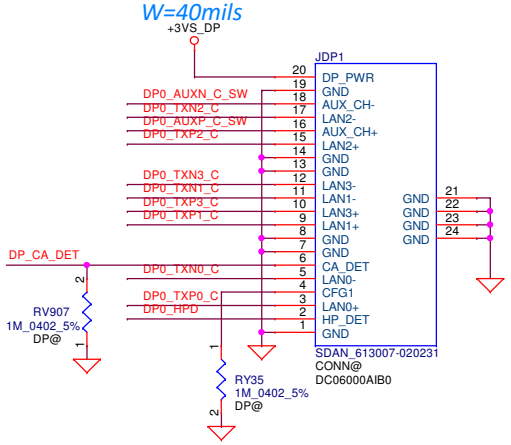
Display Port



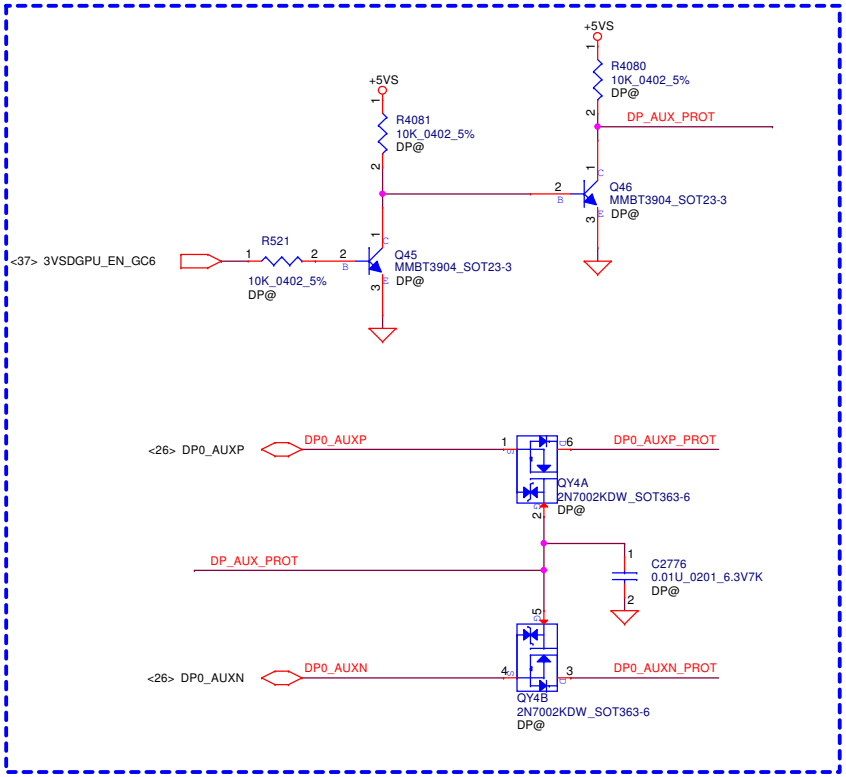
to PCH

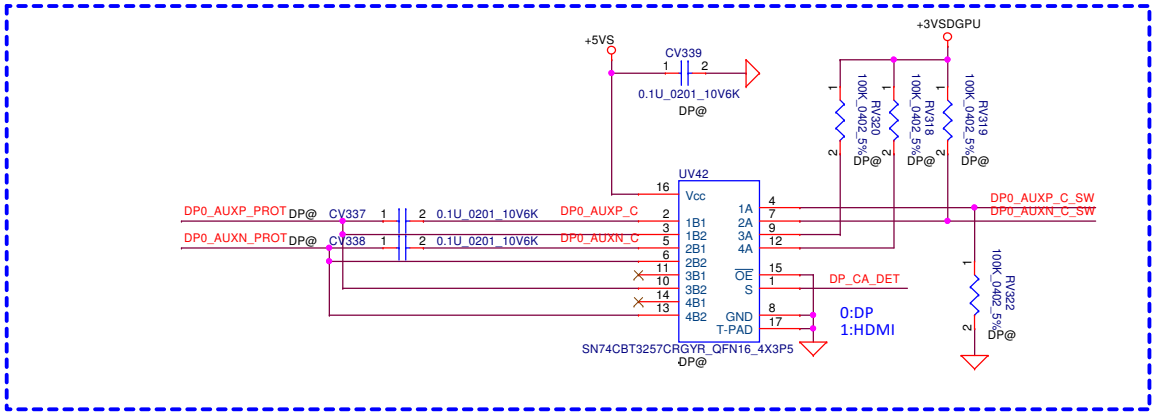


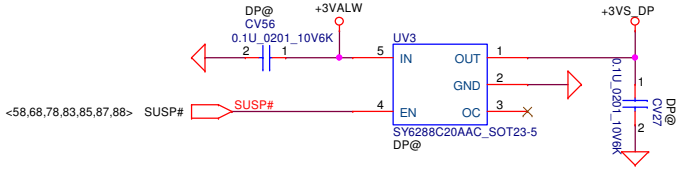




need check pin4 CFG1







OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1
L	H	B2	A=B2
H	X	Z	NC

0921 change souce to +3VALW, CTRL to SUSP#

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.	
Title	DP CONN
Size: Custom	Document Number: EH50F M/B LA-H431PR10
Rev	1.0
Date: Wednesday, February 13, 2019	Sheet 39 of 100

Raptor

<27> GPU_DP2_P3 — CY22 1 — 2 .1U_0402_16V7K — HDMI_CLKP
<27> GPU_DP2_N3 — CY24 1 — 2 .1U_0402_16V7K — HDMI_CLKN
<27> GPU_DP2_P2 — CY16 1 — 2 .1U_0402_16V7K — HDMI_TX_P0
<27> GPU_DP2_N2 — CY17 1 — 2 .1U_0402_16V7K — HDMI_TX_N0
<27> GPU_DP2_P1 — CY18 1 — 2 .1U_0402_16V7K — HDMI_TX_P1
<27> GPU_DP2_N1 — CY19 1 — 2 .1U_0402_16V7K — HDMI_TX_N1
<27> GPU_DP2_P0 — CY20 1 — 2 .1U_0402_16V7K — HDMI_TX_P2
<27> GPU_DP2_N0 — CY21 1 — 2 .1U_0402_16V7K — HDMI_TX_N2

HDMI_CLKN — RY27 1 — 2 499_0402_1% — HDMI_GND
HDMI_CLKP — RY28 1 — 2 499_0402_1%
HDMI_TX_N0 — RY29 1 — 2 499_0402_1%
HDMI_TX_P0 — RY30 1 — 2 499_0402_1%
HDMI_TX_N1 — RY31 1 — 2 499_0402_1%
HDMI_TX_P1 — RY32 1 — 2 499_0402_1%
HDMI_TX_N2 — RY33 1 — 2 499_0402_1%
HDMI_TX_P2 — RY34 1 — 2 499_0402_1%

+3VS — QY2B 2N7002KDW_SOT363-6

+5VS — UY2 AP2330W-7_SC59-3 (IN 1, GND 2, OUT 3) — +HDMI_5V_OUT
CY23 0.1U_0201_10V6K

W=40mils

EMI request

HDMI_CLKP — RY15 — HDMI_R_CLKP
XEMC@ CY26 3.3P_0402_50V8
HDMI_CLKN — RY14 — HDMI_R_CLKN
HDMI_TX_P0 — RY16 — HDMI_R_TX_P0
HDMI_TX_N0 — RY17 — HDMI_R_TX_N0
HDMI_TX_P1 — RY18 — HDMI_R_TX_P1
HDMI_TX_N1 — RY19 — HDMI_R_TX_N1
HDMI_TX_P2 — RY20 — HDMI_R_TX_P2
HDMI_TX_N2 — RY22 — HDMI_R_TX_N2
RY36 150_0402_1%
RY37 150_0402_1%
RY38 150_0402_1%
RY39 150_0402_1%

+1.8VSDGPU_AON
QY1A PJT138KA_SOT363-6
<27> GPU_DP2_CTRL_CLK — HDMI_CTRL_CLK
QY1B PJT138KA_SOT363-6
<27> GPU_DP2_CTRL_DAT — HDMI_CTRL_DAT

3ohm/10pF

HDMI_CTRL_DAT — RH238 2 — 1 2.2K_0402_5% — +HDMI_5V_OUT
HDMI_CTRL_CLK — RH239 2 — 1 2.2K_0402_5%
GPU_DP2_CTRL_CLK — RH240 2 — 1 2.2K_0402_5% — +1.8VSDGPU_AON
GPU_DP2_CTRL_DAT — RH241 2 — 1 2.2K_0402_5%

DY2
HDMI_R_CLKP — HDMI_R_CLKP
HDMI_R_CLKN — HDMI_R_CLKN
HDMI_R_TX_P0 — HDMI_R_TX_P0
HDMI_R_TX_N0 — HDMI_R_TX_N0
L05ESDL5V0NA-4 SLP2510P8
@EMC@

DY3
HDMI_R_TX_N1 — HDMI_R_TX_N1
HDMI_R_TX_P1 — HDMI_R_TX_P1
HDMI_R_TX_N2 — HDMI_R_TX_N2
HDMI_R_TX_P2 — HDMI_R_TX_P2
L05ESDL5V0NA-4 SLP2510P8
@EMC@

DY1
HDMI_HPD — HDMI_CTRL_DAT
HDMI_CTRL_CLK — +HDMI_5V_OUT
AZC099-04S.R7G_SOT23-6
@EMC@

P/N: SC300002900, S DIO(BR) AZC199-04S.R7G SOT23-6 ESD

HDMI connector

+HDMI_5V_OUT
JHDMI1
HDMI_HPD — HP_DET
+5V
HDMI_CTRL_DAT — DDC/CEC_GND
HDMI_CTRL_CLK — SDA
SCL
Reserved
HDMI_R_CLKN — CEC
CK-
HDMI_R_CLKP — CK_shield
HDMI_R_TX_N0 — CK+
D0-
HDMI_R_TX_P0 — D0_shield
HDMI_R_TX_N1 — D0+
D1-
HDMI_R_TX_P1 — D1_shield
HDMI_R_TX_N2 — D1+
D2-
HDMI_R_TX_P2 — D2_shield
D2+
GND GND GND GND
ACON_HMR2E-AK120D
CONN@
DC232000Y00

ZZZ2

HDMI_ROYALTY
ROYALTY HDMI W/LOGO+HDCP
RO0000003HM
45@

to PCH

+3VS — RY24 1M_0402_5% — QY2A 2N7002KDW_SOT363-6
<16,25> HDMI_HPD_PCH — HDMI_HPD
RY11 100K_0402_5%

RY11 design guide rev2.0 use 20K pull down.

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: HDMI CONN.

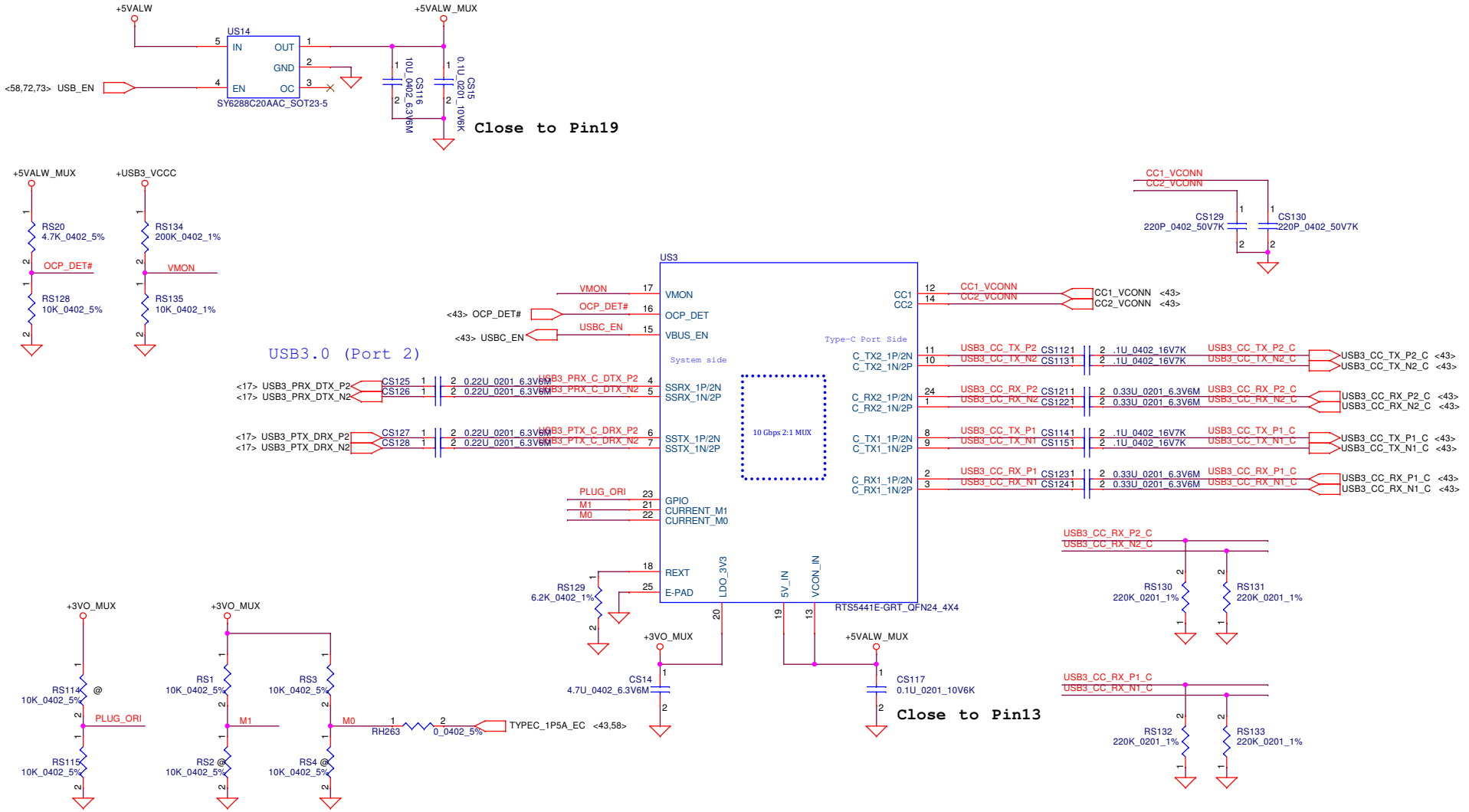
Size	Document Number	Rev
Custom	EH50F M/B LA-H431PR10	1.0

Date: Wednesday, February 13, 2019 Sheet 40 of 100

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.		
Title: *Reserve Page*		
Size: Custom	Document Number: *EH50F M/B LA-H431PR10*	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 41 of 100	



5441E Current Limit		
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

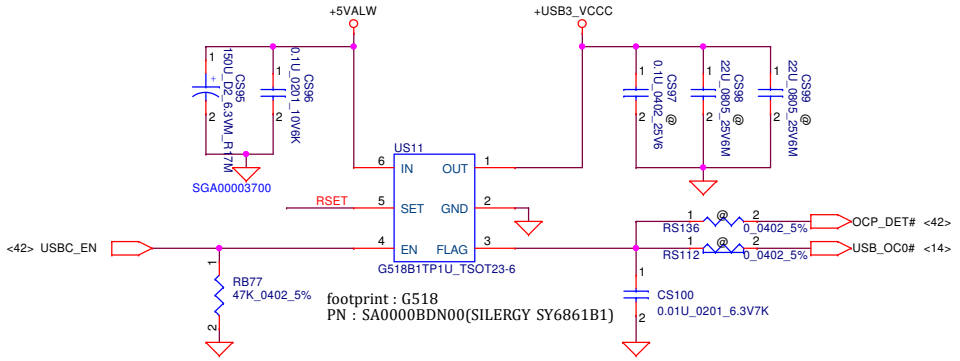
RTS5441 M0 truth table by 2018 BIOS spec			
TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

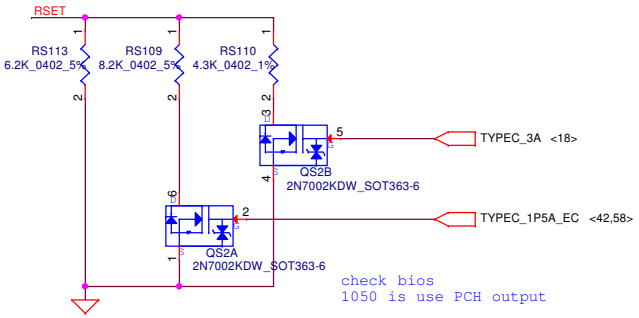
Compal Electronics, Inc.

Title: CC+USB TYPE C

Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 42 of 100

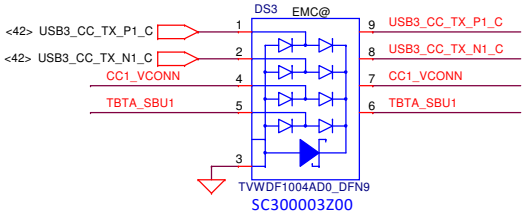


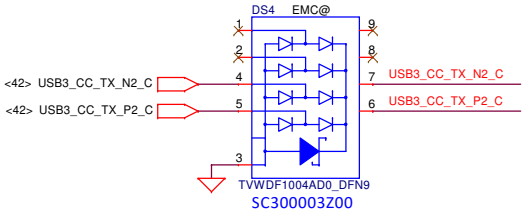


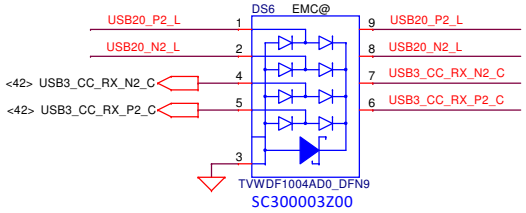
Initial Current mode selection	
USBC_EN	V BUS
L	0
L	0
H	0
H	1

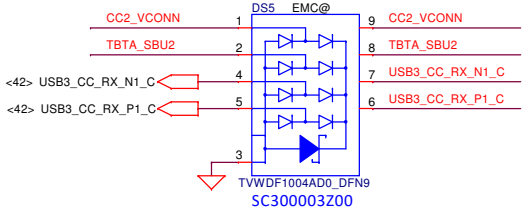
G518 MOS Current Limit				
GPP_B1 (TYPEC_1P5A)	GPP_B4 (TYPEC_3A)	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A

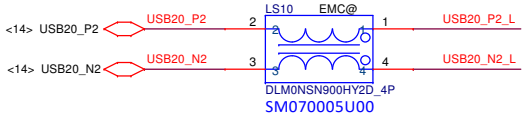
For ESD request

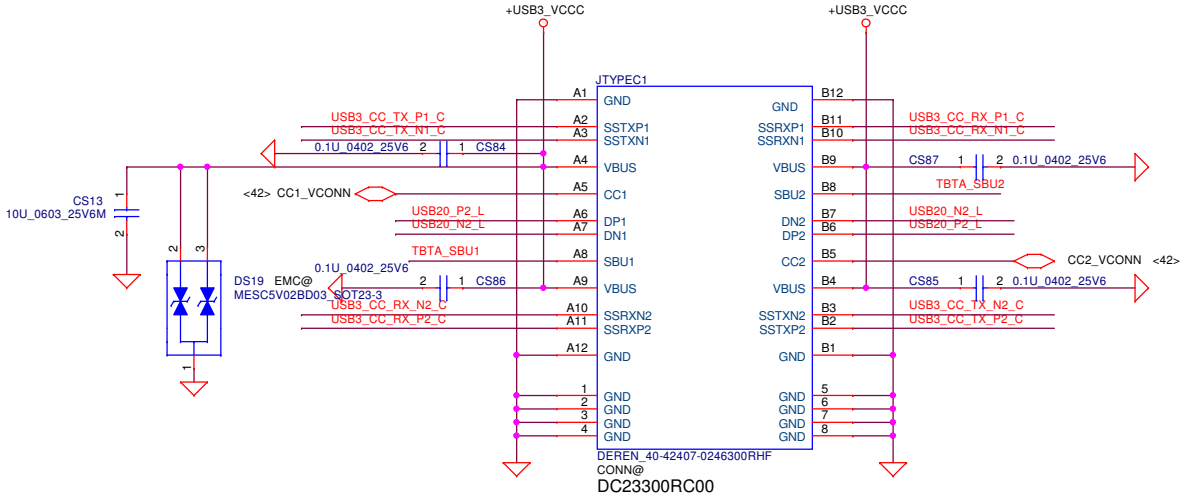












CC1_VCONN & CC2_VCONN need 20miil trace width.

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: CC+USB TYPE C

Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 43 of 100

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.		
Title: Reserve Page		
Size: Custom	Document Number: EH50F M/B LA-H431PR10	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 44 of 100	

Reserve Page

Compal Electronics, Inc.			
Title: Reserve Page			
Size: Custom	Document Number: EH50F M/B LA-H431PR10		Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 45 of 100		

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.		
Title: *Reserve Page*		
Size: Custom	Document Number: *EH50F M/B LA-H431PR10*	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 46 of 100	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.		
Title: *Reserve Page*		
Size: Custom	Document Number: *EH50F M/B LA-H431PR10*	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 47 of 100	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: *Reserve Page*

Size: Custom | Document Number: *EH50F M/B LA-H431PR10* | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 48 of 100

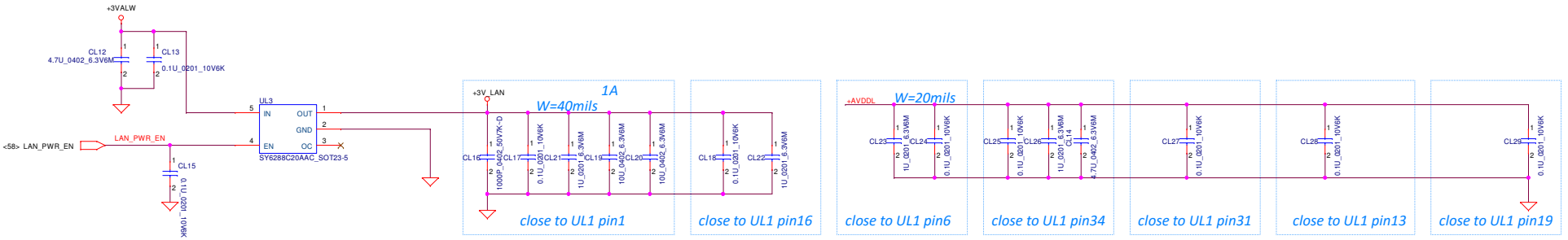
Reserve Page

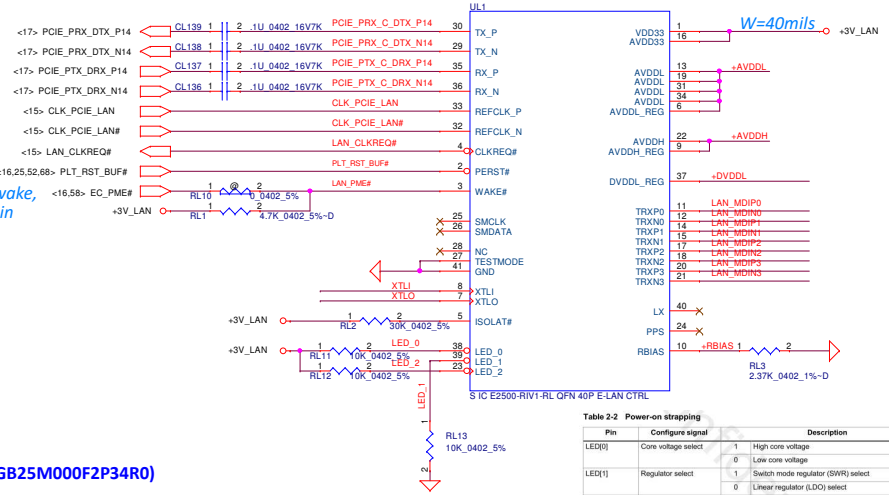
Compal Electronics, Inc.			
Title: Reserve Page			
Size: Custom	Document Number: EH50F M/B LA-H431PR10		Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 49 of 100		

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.		
Title: Reserve Page		
Size: Custom	Document Number: EH50F M/B LA-H431PR10	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 50 of 100	

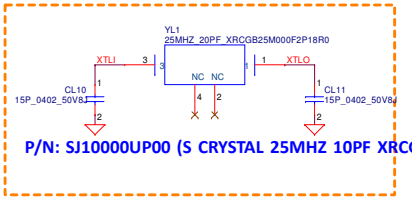




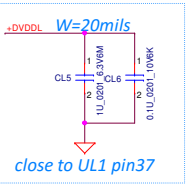
remind : if no support wake, don't monitor this pin

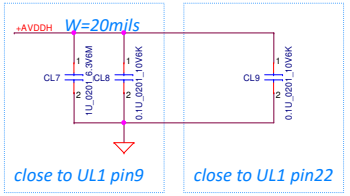
Table 2-2 Power-on strapping

Pin	Configure signal		Description
LED[0]	Core voltage select	1	High core voltage
		0	Low core voltage
LED[1]	Regulator select	1	Switch mode regulator (SWR) select
		0	Linear regulator (LDO) select
LED[2]	External clock select	1	25 MHz external clock input
		0	48 MHz external clock input



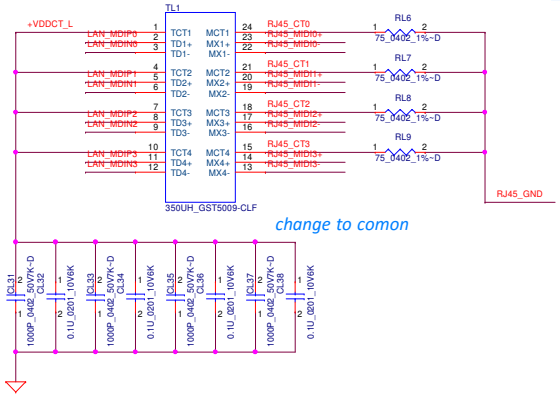
P/N: SJ10000UP00 (S CRYSTAL 25MHZ 10PF XRCGB25M000F2P34R0)



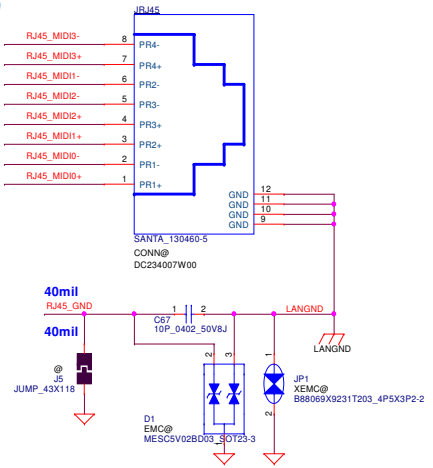


check need power or not? 3/15

TIMAG: S X'FORM_ IH-160 LAN,SP050006F00
BOTHHAND: S X'FORM_ GST5009-E LF LAN,SP050006B10



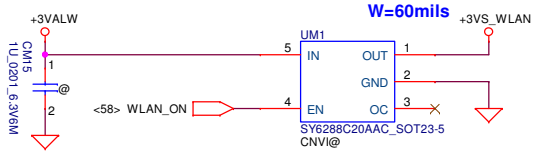
LAN Connector

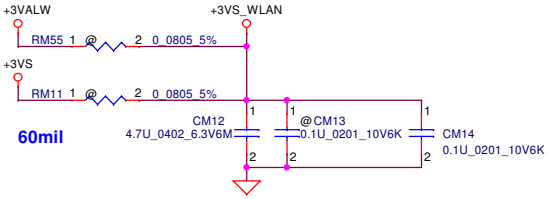


Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

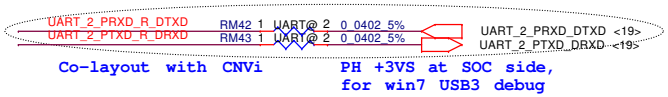
Compal Electronics, Inc.	
Title	LAN E2400
Size	Document Number: EH50F M/B LA-H431PR10
Rev	1.0
Date:	Wednesday, February 13, 2019
Sheet	51 of 100

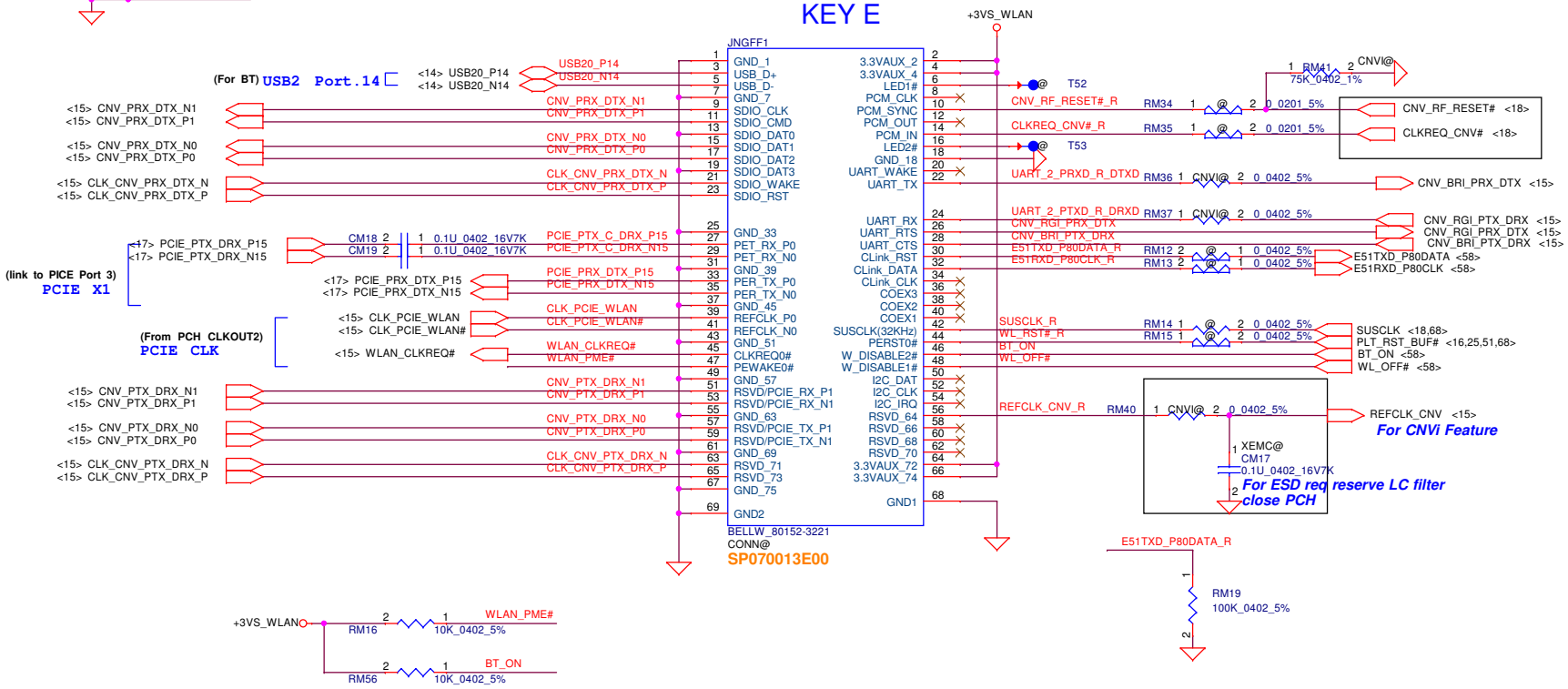
Wireless LAN





NGFF WL+BT (KEY E)





Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: WLAN M.2

Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 52 of 100

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.		
Title: Reserve Page		
Size: Custom	Document Number: EH50F M/B LA-H431PR10	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 53 of 100	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

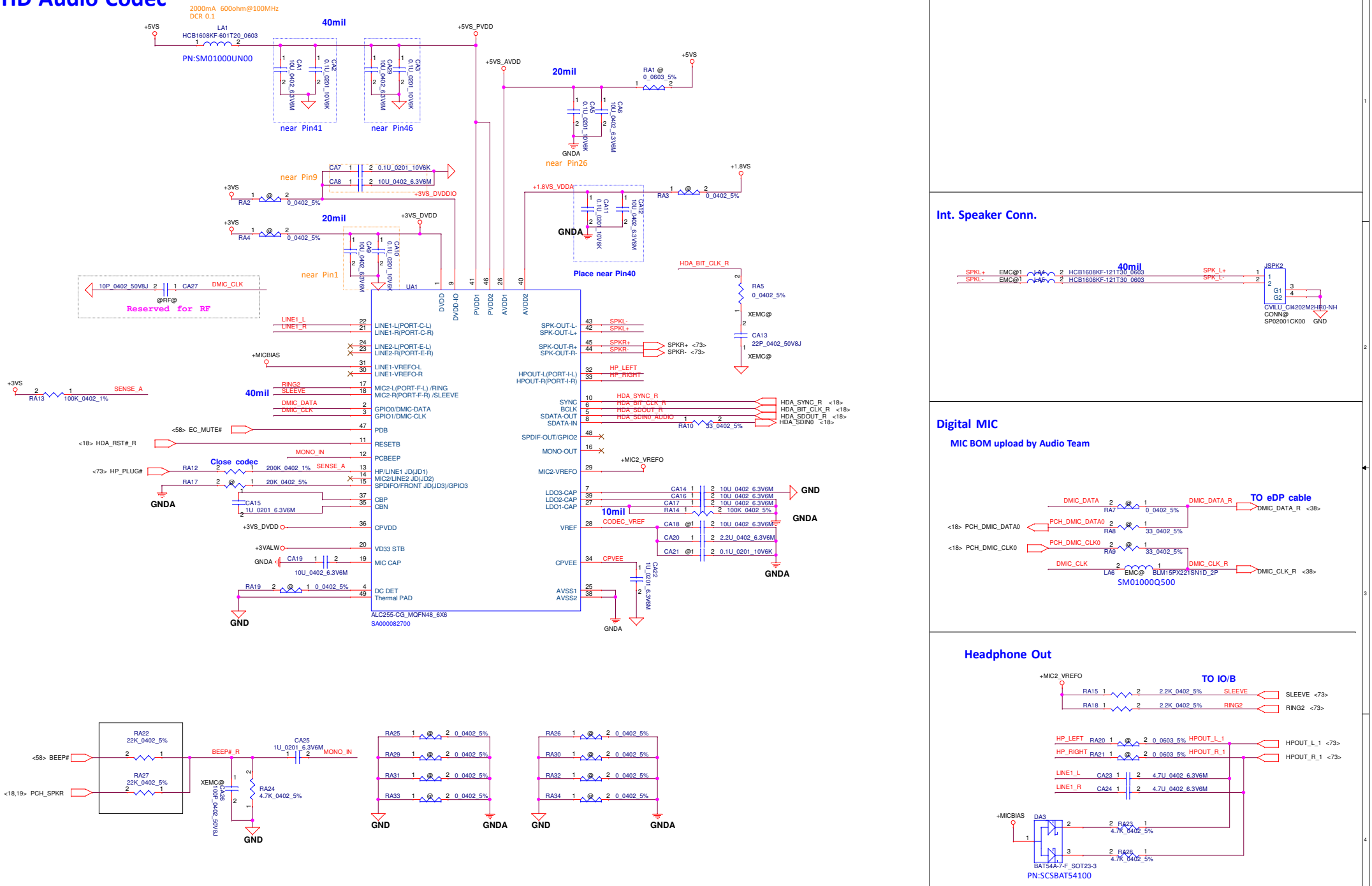
Compal Electronics, Inc.		
Title: Reserve Page		
Size: Custom	Document Number: EH50F M/B LA-H431PR10	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 54 of 100	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.		
Title: Reserve Page		
Size: Custom	Document Number: EH50F M/B LA-H431PR10	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 55 of 100	

HD Audio Codec



Int. Speaker Conn.

Digital MIC

MIC BOM upload by Audio Team

Headphone Out

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: HD Audio Codec ALC255

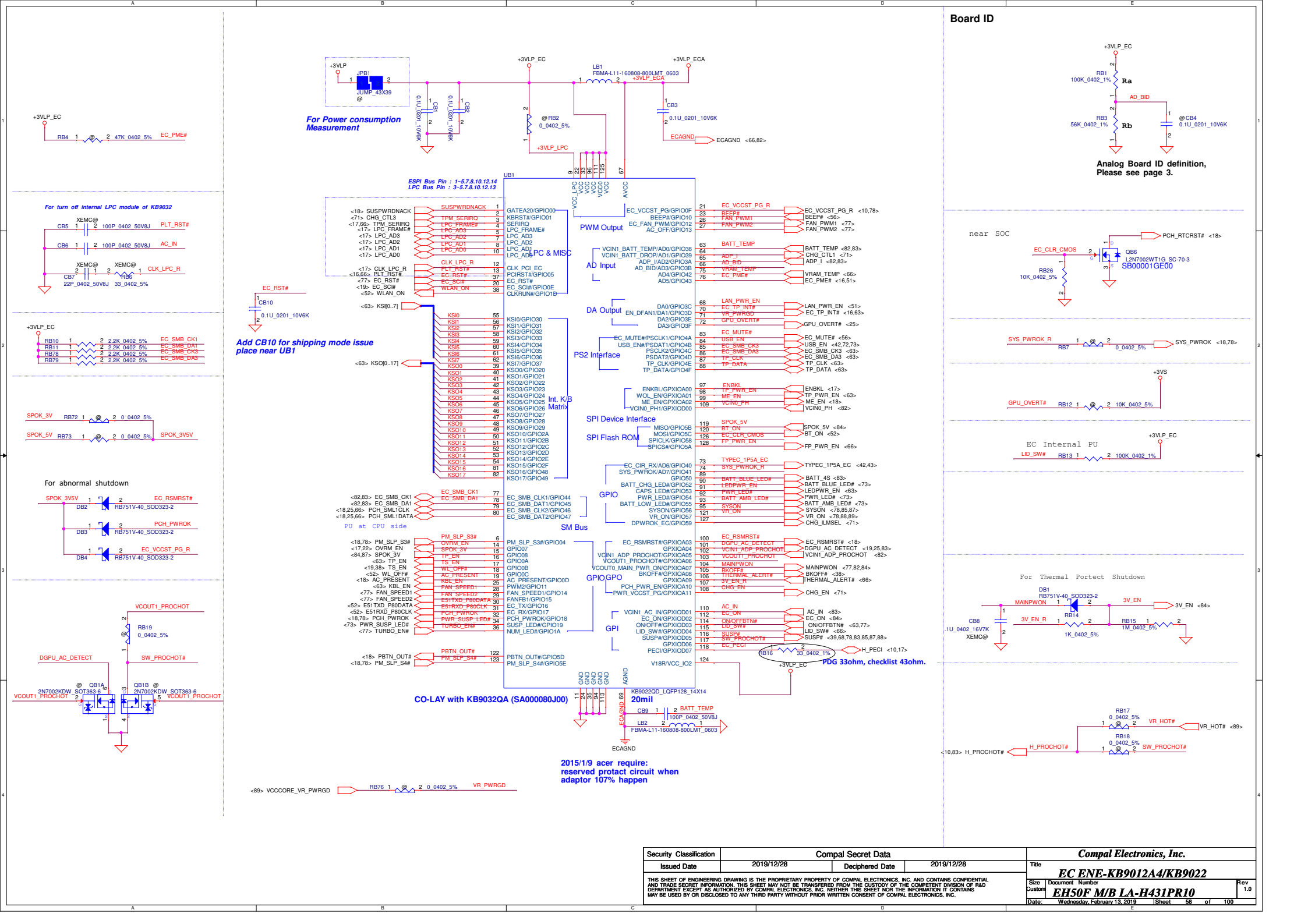
Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 56 of 100

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.		
Title: *Reserve Page*		
Size: Custom	Document Number: *EH50F M/B LA-H431PR10*	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 57 of 100	


Board ID
Analog Board ID definition, Please see page 3.
For Power consumption Measurement
ESPI Bus Pin : 1~5,7,8,10,12,14
LPC Bus Pin : 3~5,7,8,10,12,13
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
Add CB10 for shipping mode issue place near UB1
CO-LAY with KB9032QA (SA000080J00)
20mil
PDG 33ohm, checklist 43ohm.
2015/1/9 acer require: reserved protact circuit when adaptor 107% happen
For turn off internal LPC module of KB9032
For abnormal shutdown
For Thermal Portect Shutdown
EC Internal PU
near SOC
Security Classification
Compal Secret Data
Issued Date
2019/12/28
Deciphered Date
2019/12/28
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
EC ENE-KB9012A4/KB9022
Size
Custom
Document Number
EH50F M/B LA-H431PR10
Rev
1.0
Date:
Wednesday, February 13, 2019
Sheet
58
of
100

Reserve Page

Compal Electronics, Inc.

Title: Reserve Page

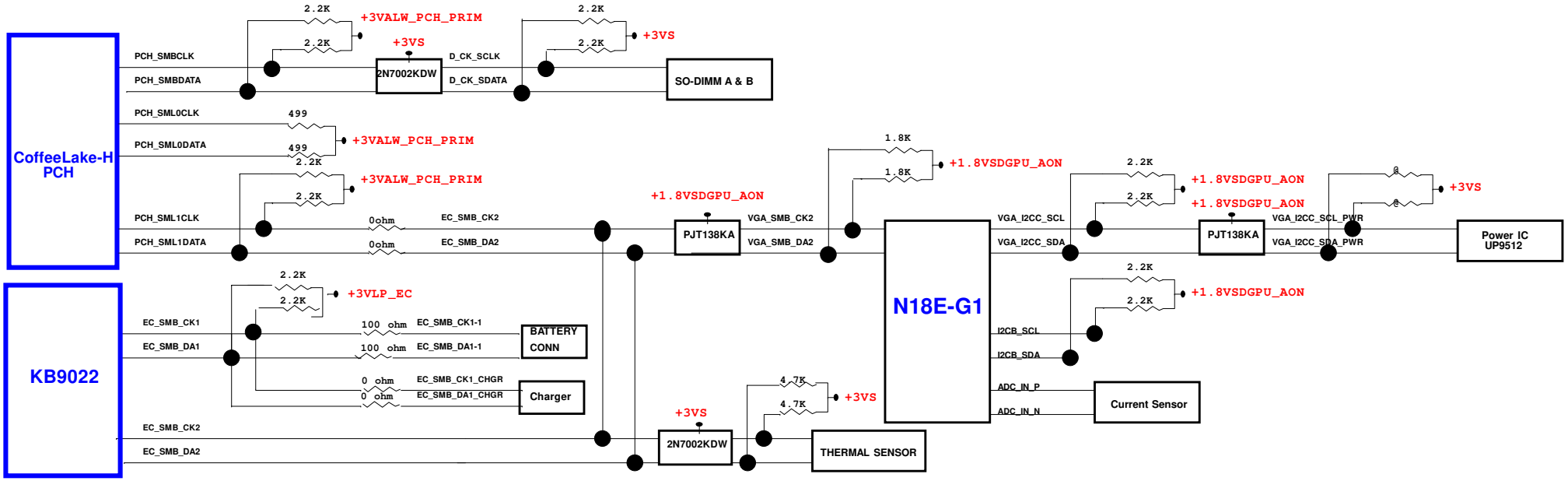
Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

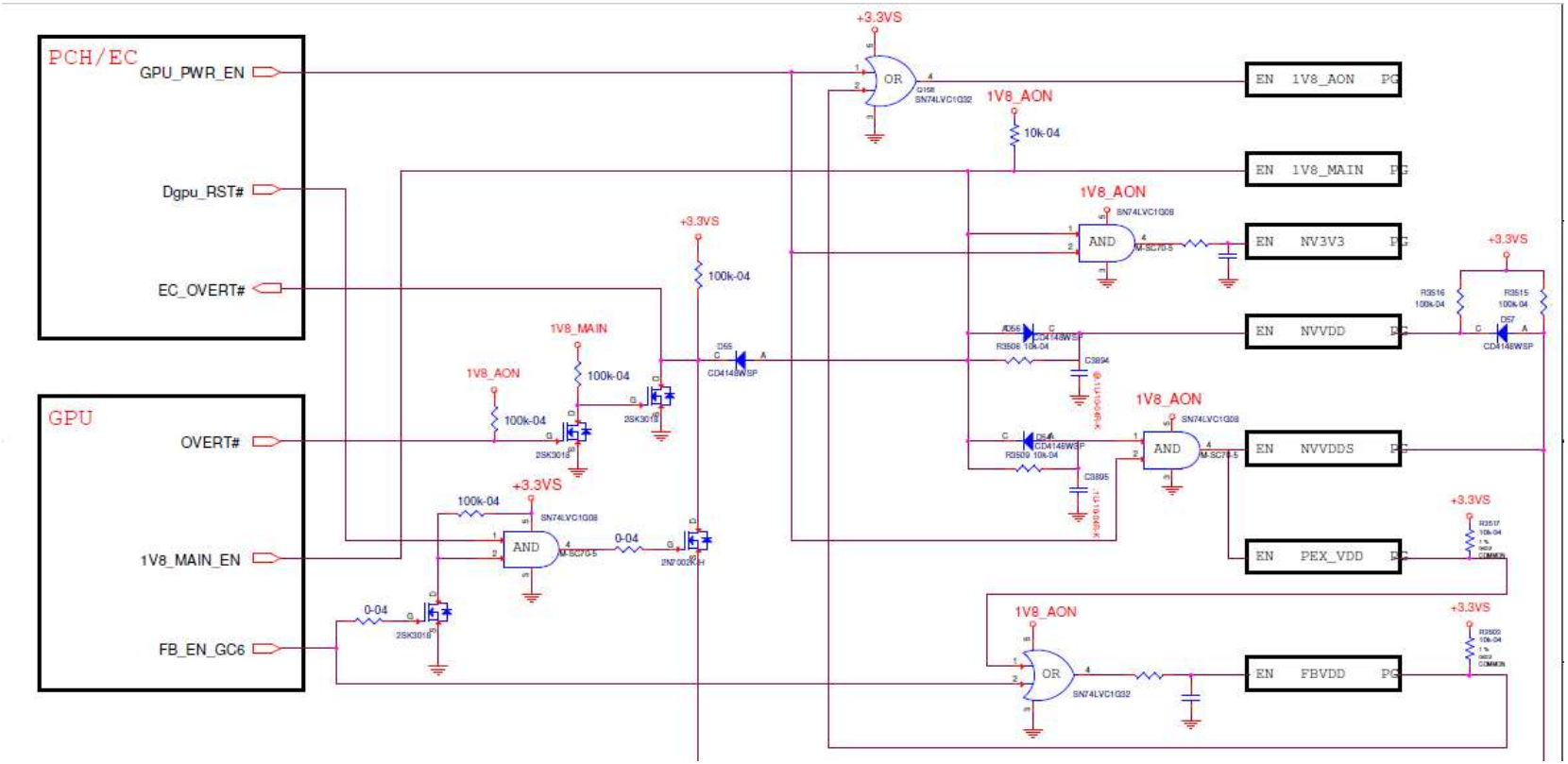
Date: Wednesday, February 13, 2019 | Sheet 59 of 100

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.		
Title: Reserve Page		
Size: Custom	Document Number: EH50F M/B LA-H431PR10	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 60 of 100	



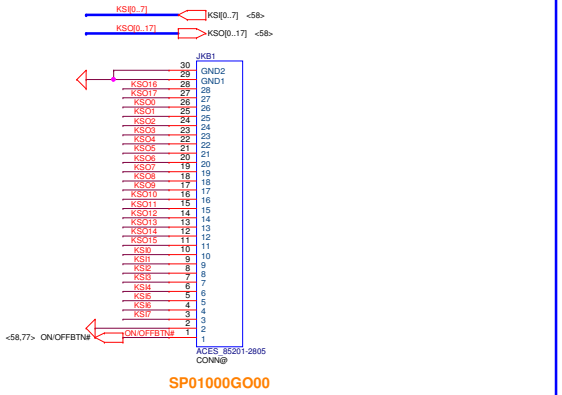


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Title	N17 Sequence		
Size	Document Number		Rev
	EH50F M/B LA-H431PR10		1.0
Date:	Wednesday, February 13, 2019	Sheet	61 of 100

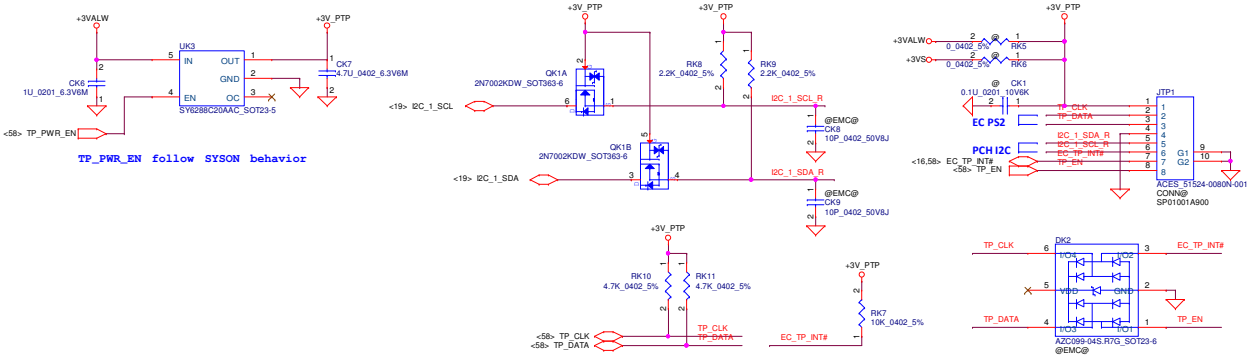
Reserve Page

KB Conn.

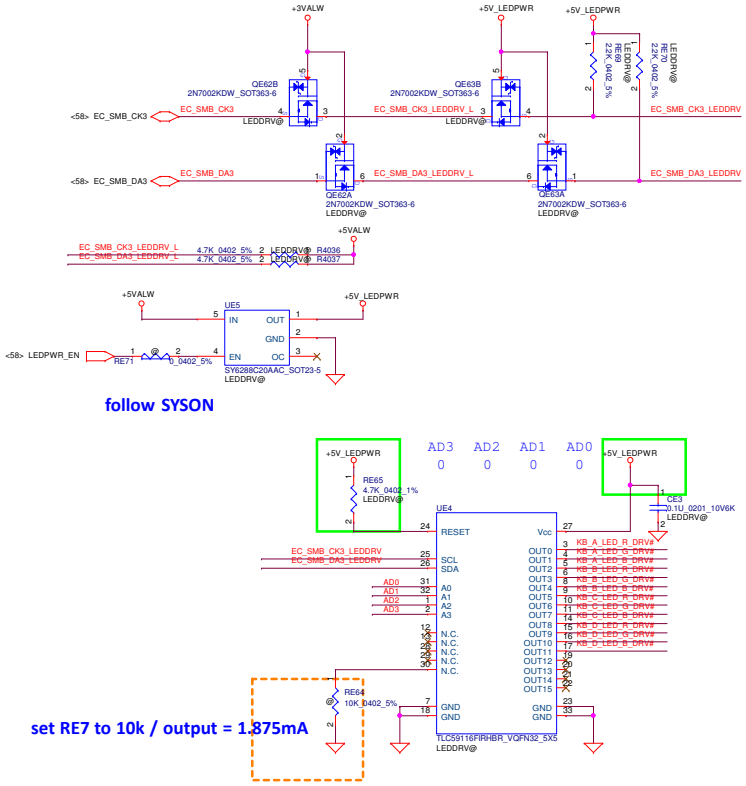


SP01000GO00

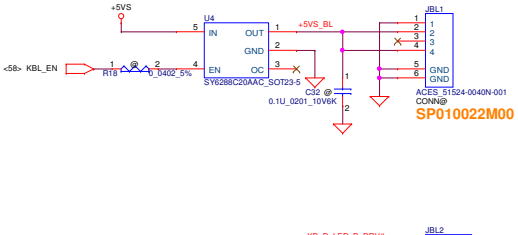
Touch Pad

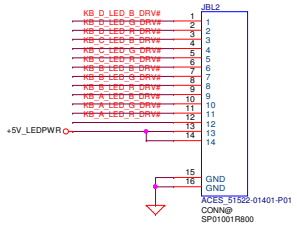


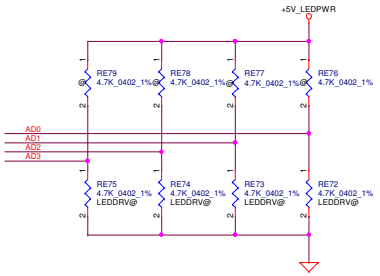
LED driver



KB BackLight







Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.		
Title: KB/TP/LEDs(TLC59116F)		
Size: Custom	Document Number: EH50F M/B LA-H431PR10	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet: 63 of 100	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

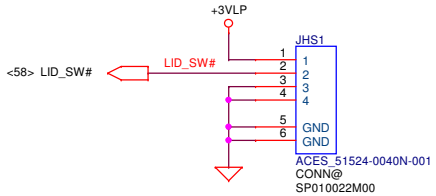
Compal Electronics, Inc.			
Title: Reserve Page			
Size: Custom	Document Number: EH50F M/B LA-H431PR10		Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 64 of 100		

Reserve Page

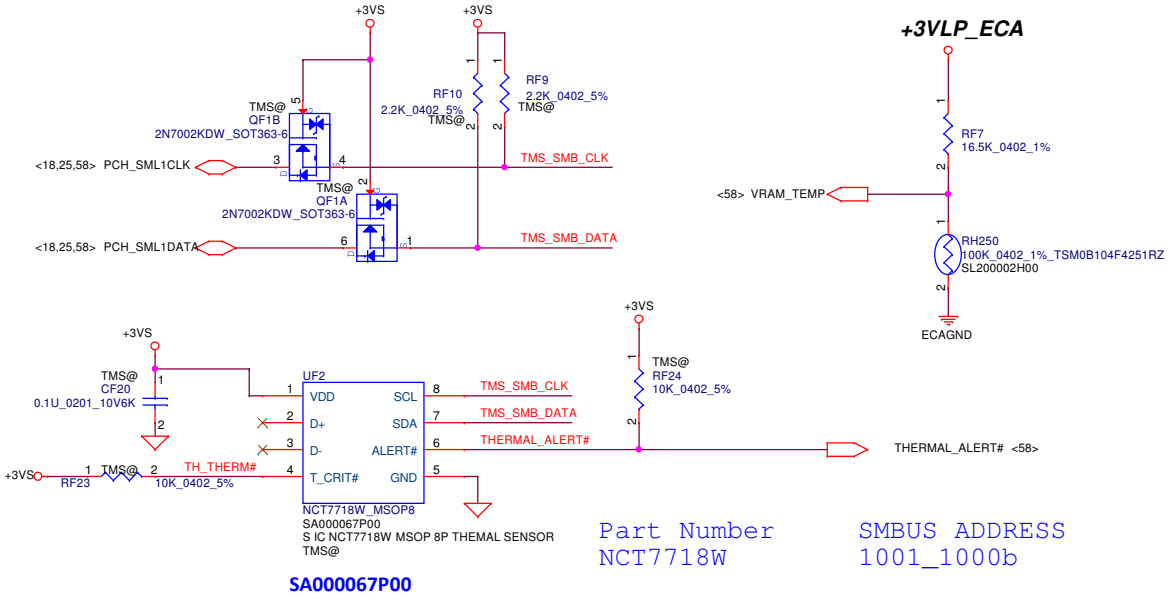
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.		
Title: Reserve Page		
Size: Custom	Document Number: EH50F M/B LA-H431PR10	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 65 of 100	

To Hall sensor/B



THERMAL SENSOR

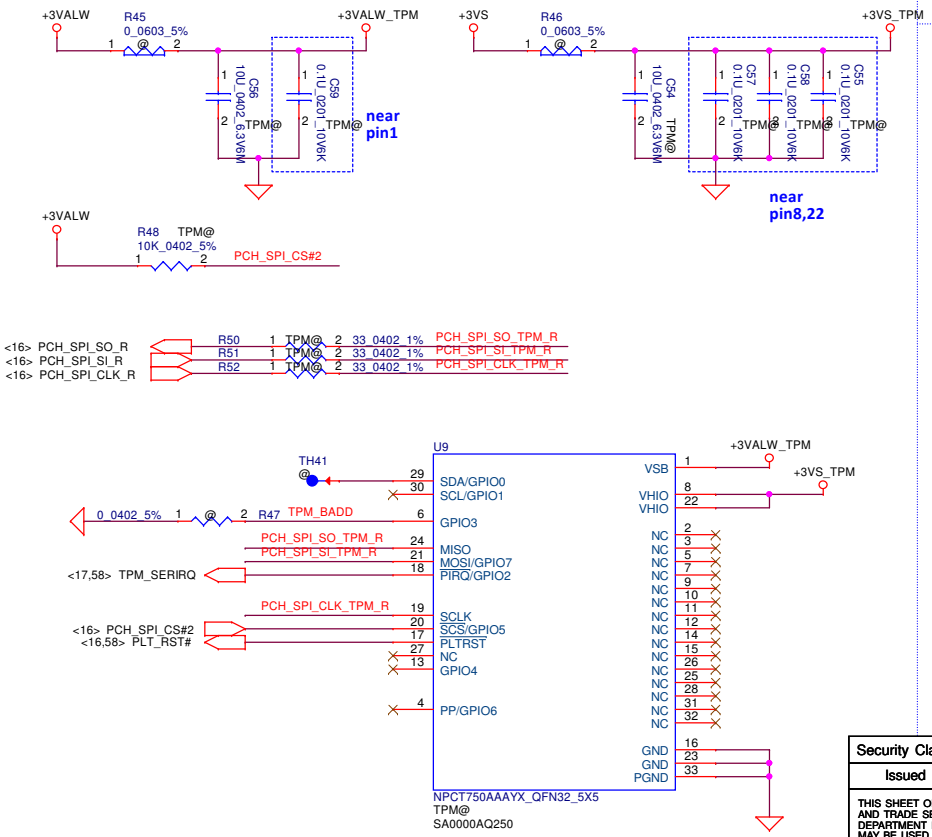


Part Number NCT7718W

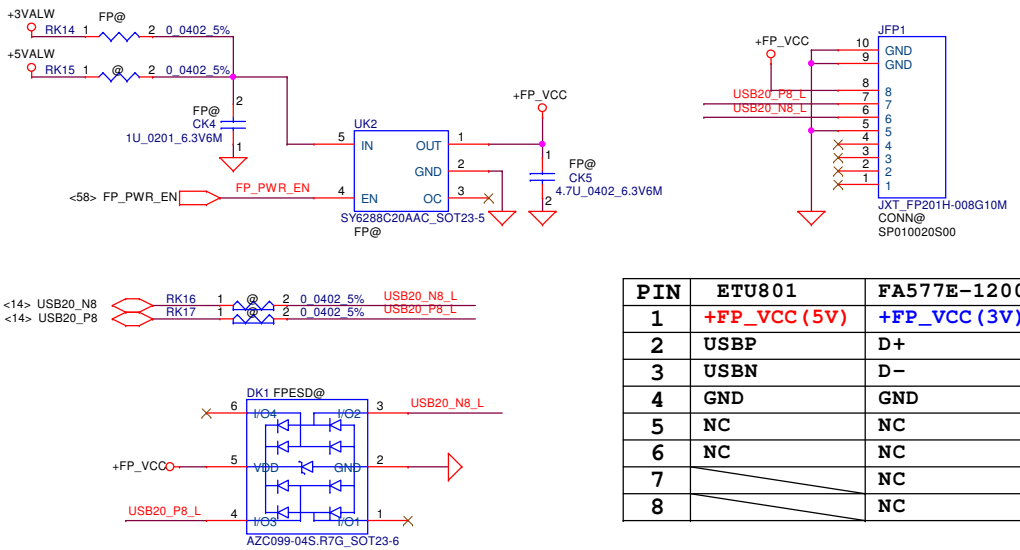
SMBUS ADDRESS 1001_1000b

SA000067P00

TPM



Finger Print



PIN	ETU801	FA577E-1200
1	+FP_VCC(5V)	+FP_VCC(3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC

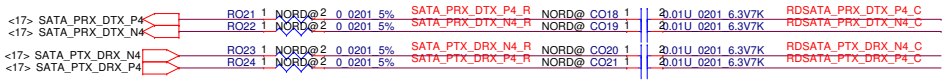
Compal Electronics, Inc.

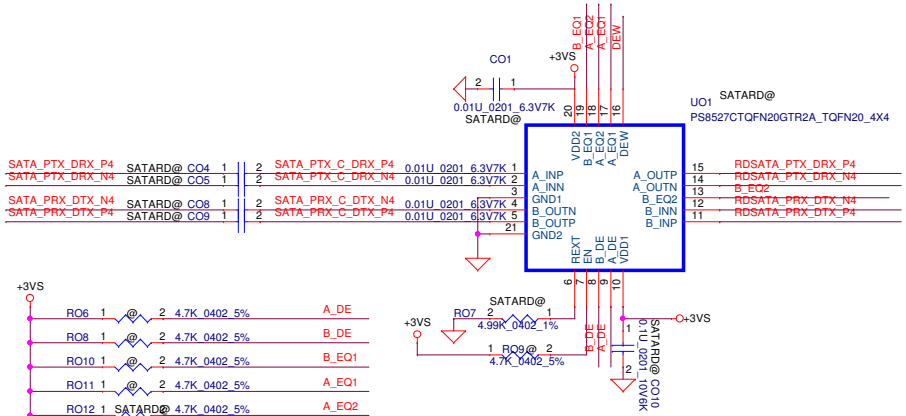
Title: Sensors

Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 66 of 100

SATA Re-Driver and cable HDD Conn.





USE 8527 re-driver
SA00007JU10

Chip Enable, Internally pulled up at ~150KΩ

EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.
Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.
Internally tied to VDD/2(M status).

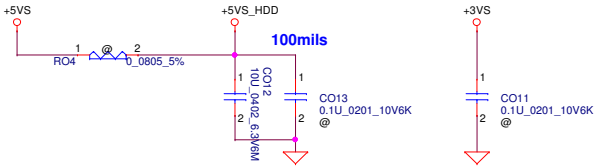
B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Equalizer control and program for channel A.
Internally tied to VDD/2 (M status).

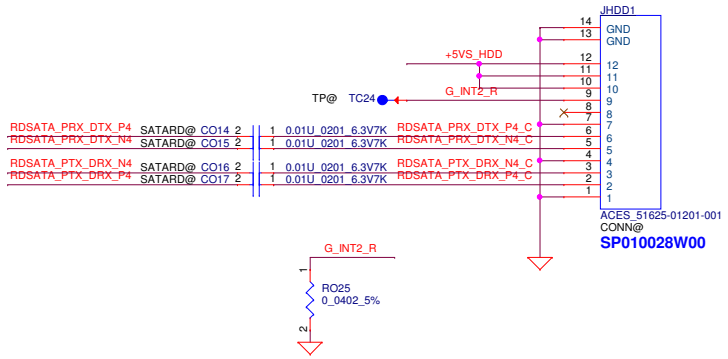
A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.
Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB



FFC Type

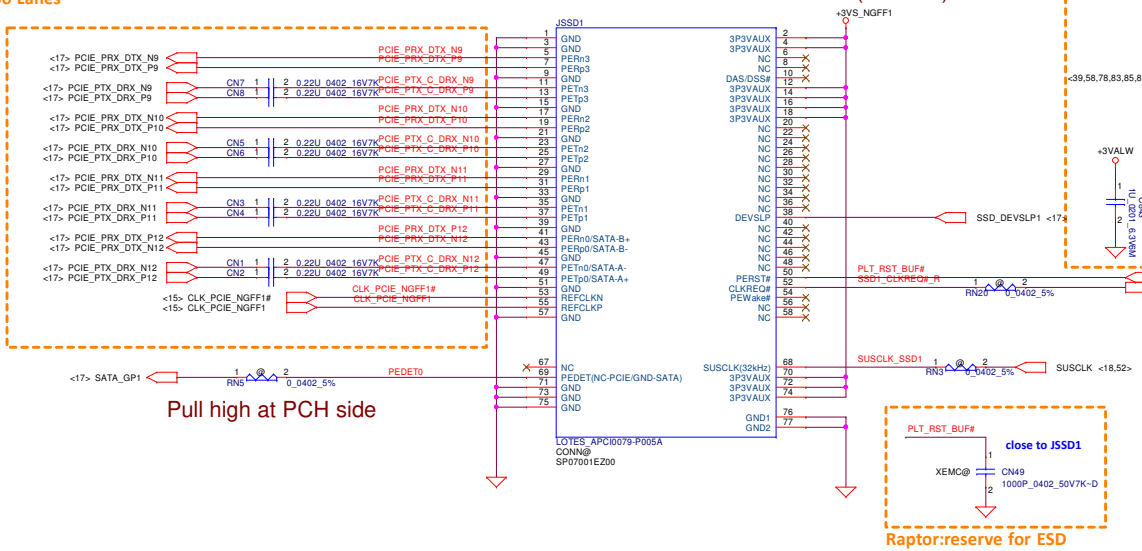


Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

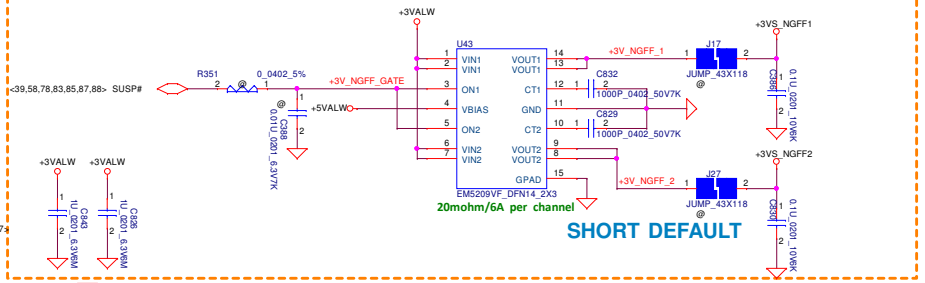
Compal Electronics, Inc.			
Title: HDD/ Re-Driver			
Size: Custom	Document Number: EH50F M/B LA-H431PR10		Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 67 of 100		

Raptor:LANE REVERSAL for SATA/PCIe Combo Lanes

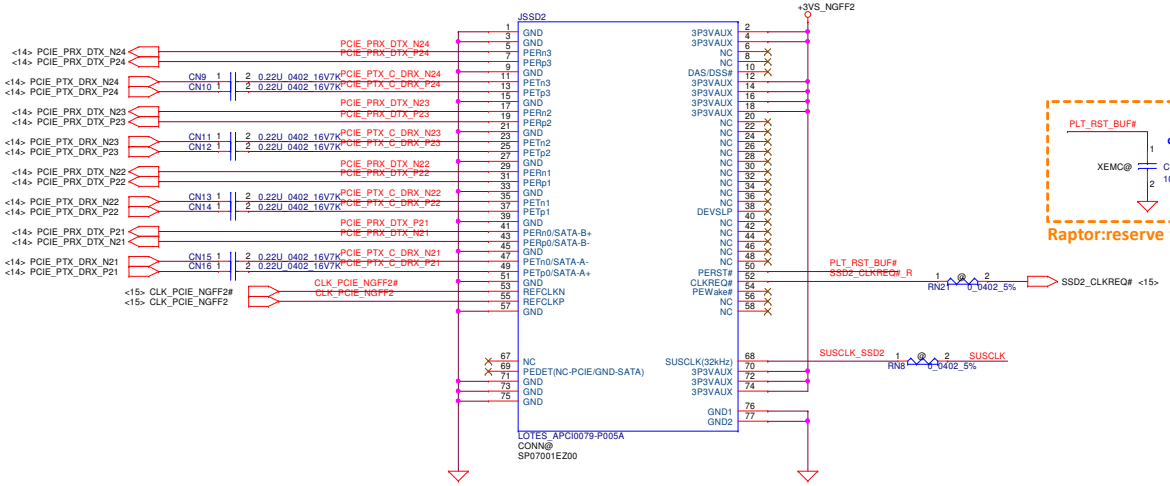
SSD NGFF Slot_1 Key M (left side)

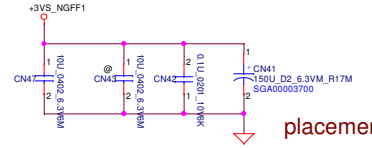


+3VS_NGFF PWR

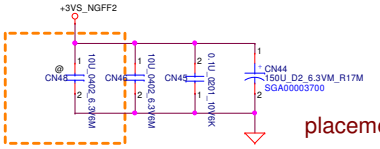


SSD NGFF Slot_2 Key M (left side)





PEDET	Module Type
0	SATA
1	PCIE



PEDET	Module Type
0	SATA
1	PCIE

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: M.2 SSD_PCIe/SATA

Size: | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 68 of 100

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.		
Title: Reserve Page		
Size: Custom	Document Number: EH50F M/B LA-H431PR10	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 69 of 100	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

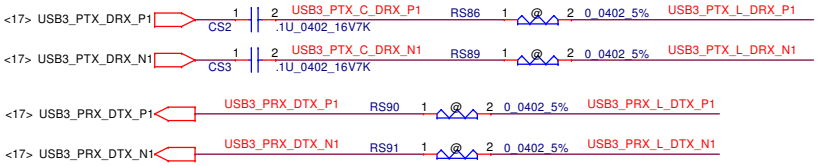
Compal Electronics, Inc.

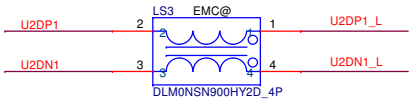
Title: Reserve Page

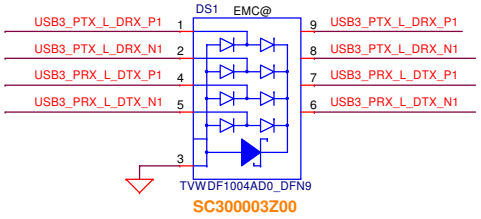
Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

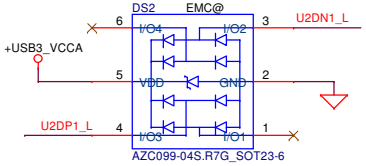
Date: Wednesday, February 13, 2019 | Sheet 70 of 100

USB3.0 /2.0 CMC

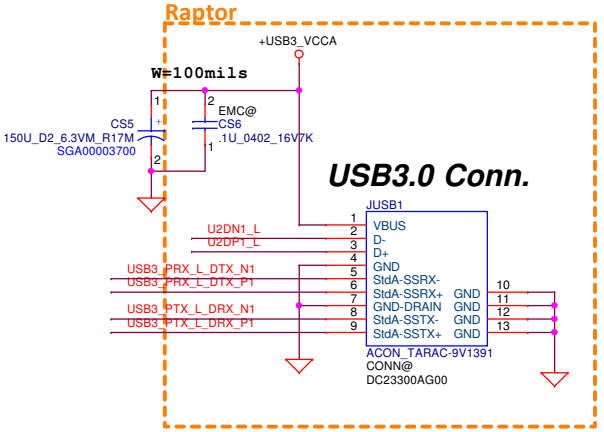




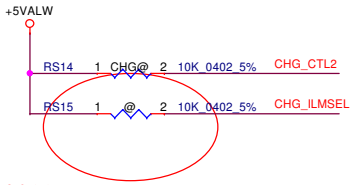




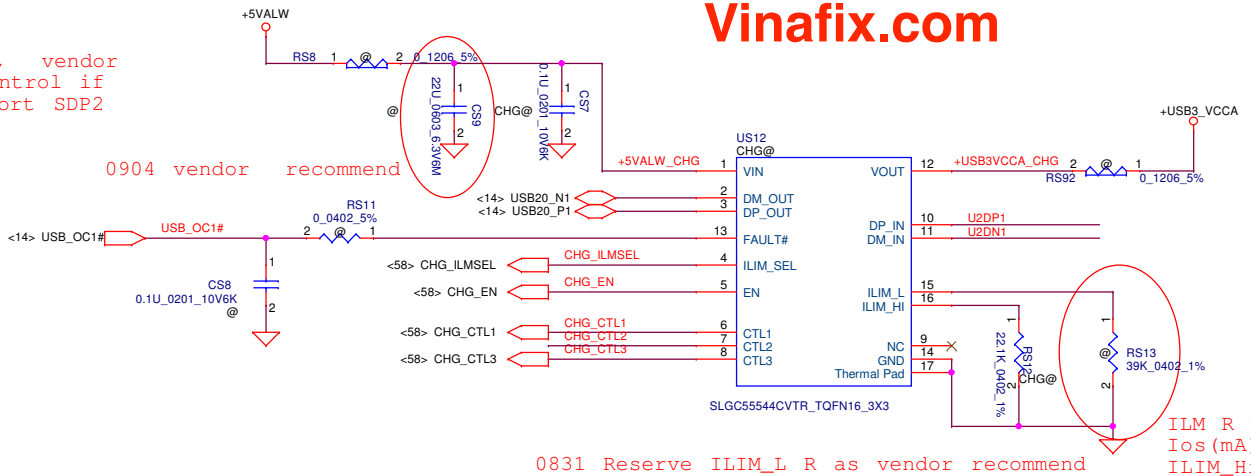
Charger Port



USB Host Charger



0911 Rerserve PU, vendor suggest to EC control if future need support SDP2



0831 Reserve ILIM_L R as vendor recommend

ILM R vaule
Ios(mA)=50250/R(Kohm)
ILIM_Hi=2273mA
ILIM_L=1288mA(reserve)

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

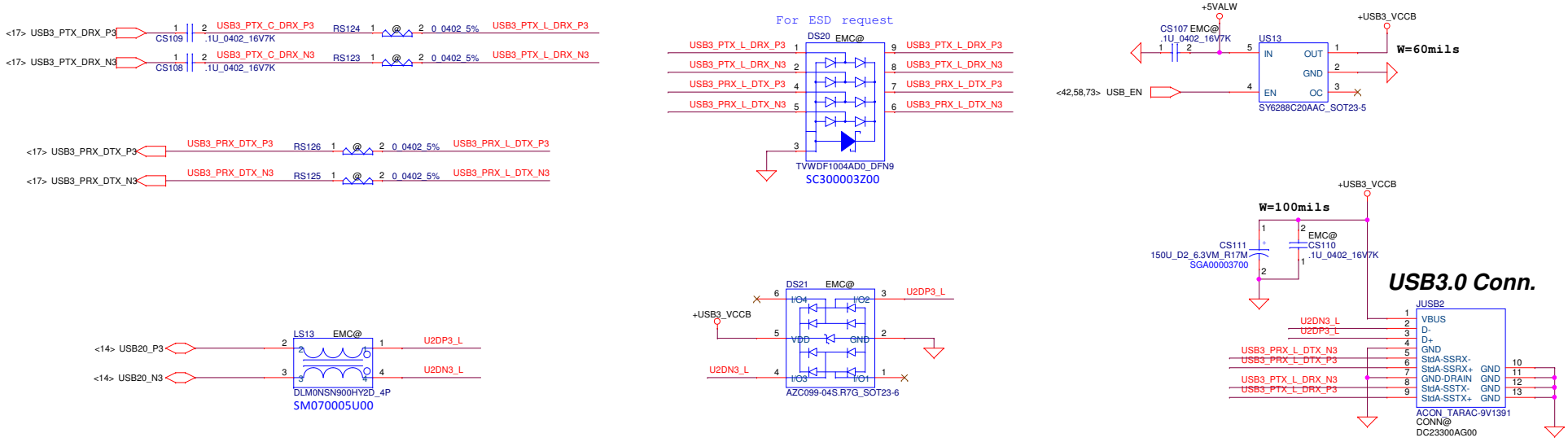
Compal Electronics, Inc.

Title: USB TYPEA with Charger

Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

Date: Wednesday, February 13, 2019 | Sheet 71 of 100

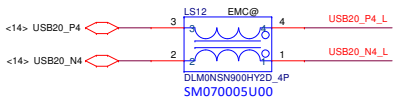
USB3.0

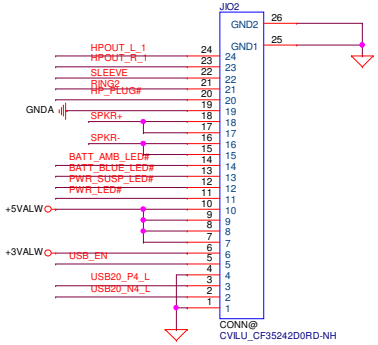


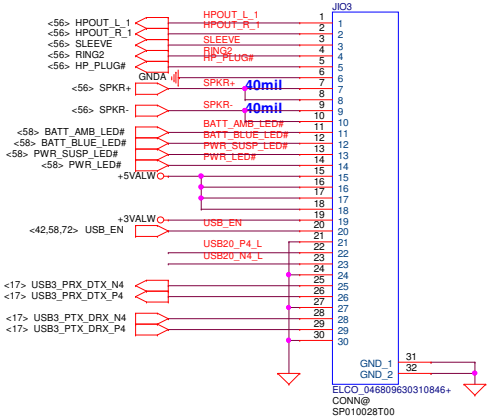
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.			
Title: USB3.0 Conn/USB Charger			
Size: Custom	Document Number: EH50F M/B LA-H431PR10		Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 72 of 100		

USB_Audio/B







Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.		
Title: IO/XBOX DB		
Size: Custom	Document Number: EH50F M/B LA-H431PR10	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 73 of 100	

Reserve Page

Reserve Page

Compal Electronics, Inc.

Title: Reserve Page

Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

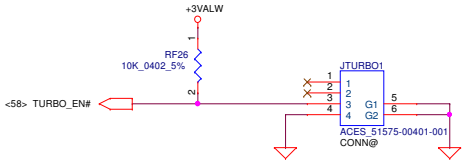
Date: Wednesday, February 13, 2019 | Sheet 75 of 100

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

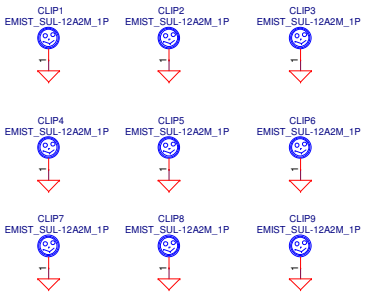
Compal Electronics, Inc.		
Title: *Reserve Page*		
Size: C	Document Number: *EH50F M/B LA-H431PR10*	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 76 of 100	

Turbo Key

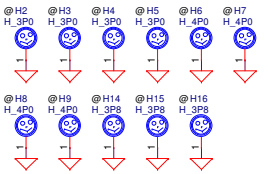


SP01002LG00

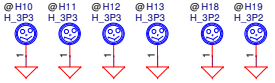
Clips

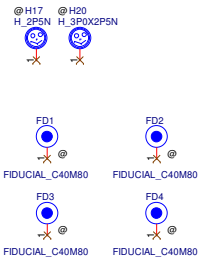


SCREW



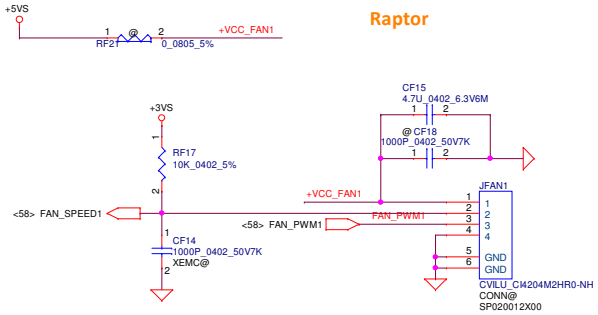
STAND OFF





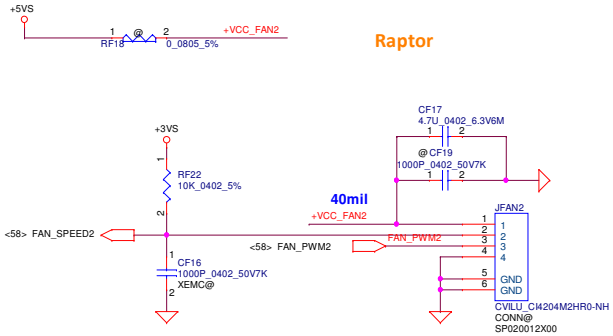
CPU FAN Conn

Raptor



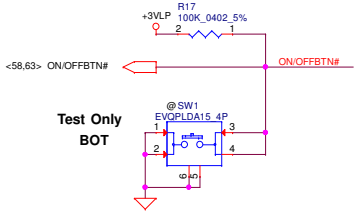
GPU FAN Conn

Raptor

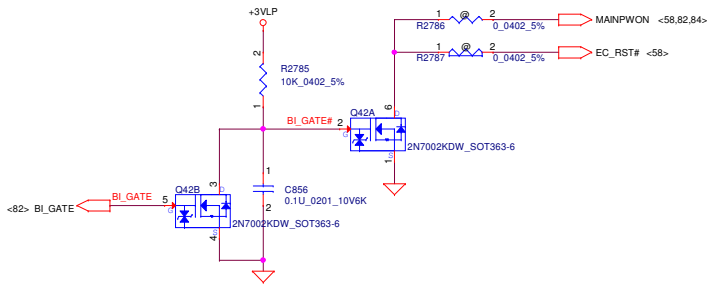


PCB P/N

ON/OFF BTN

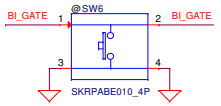


Reset Circuit



BI_GATE PH to +RTCVCC at PWR side

Reset Button



SN10000CV00

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

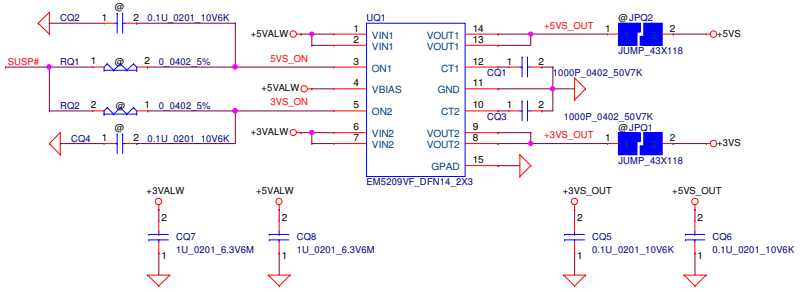
Compal Electronics, Inc.

Title: PWRBTN/PCB PN//SCREW/FAN

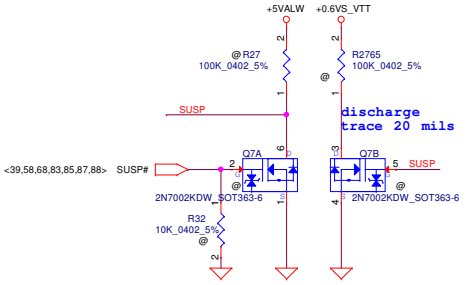
Size: Custom | Document Number: EH50F M/B LA-H431PR10 | Rev: 1.0

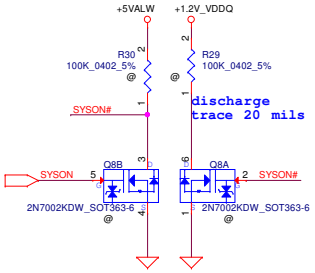
Date: Wednesday, February 13, 2019 | Sheet 77 of 100

System DC inferface

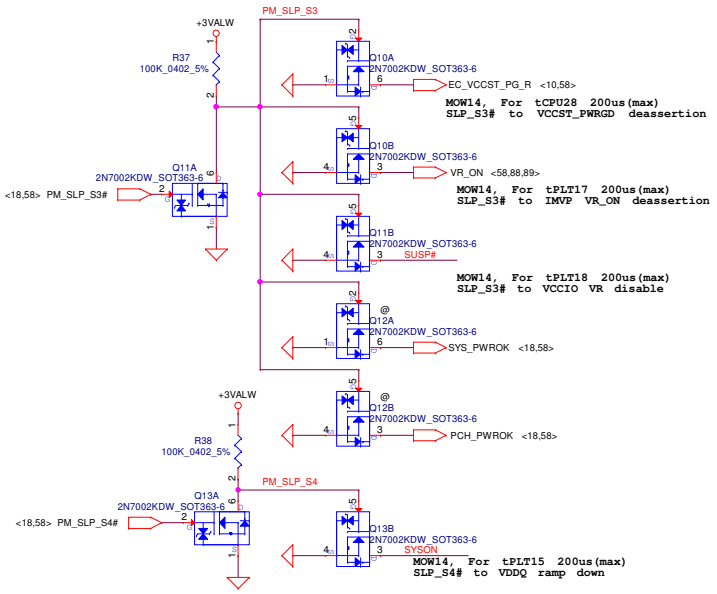


Place CQ7 close UQ1 pin 1&2
Place CQ8 close UQ1 pin 6&7



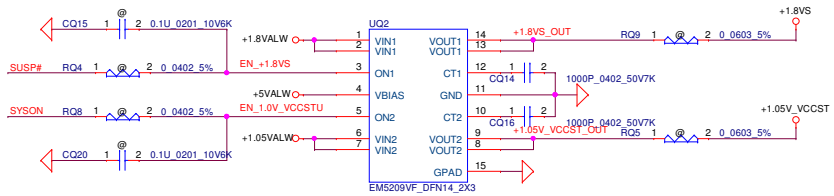


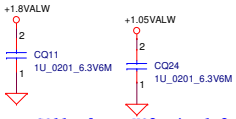
For Power ON/Off Sequence

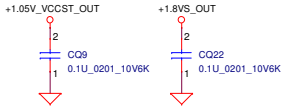


P/N: SB00000EO00 footprint use SB00000ZU00

+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS

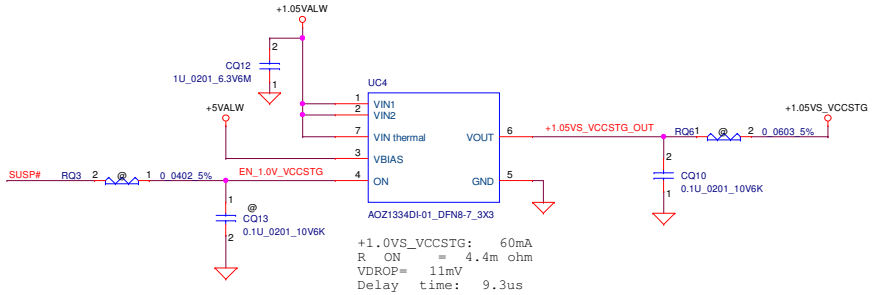






Place CQ11 close UQ2 pin 1&2
Place CQ24 close UQ2 pin 6&7

+1.05VALW TO +1.05VS_VCCSTG



+1.0VS_VCCSTG: 60mA
R ON = 4.4m ohm
VDROP= 11mV
Delay time: 9.3us

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.

Title: DC INTERFACE

Size	Document Number	Rev
Custom	EH50F M/B LA-H431PR10	1.0

Date: Wednesday, February 13, 2019 Sheet 78 of 100

Reserve Page

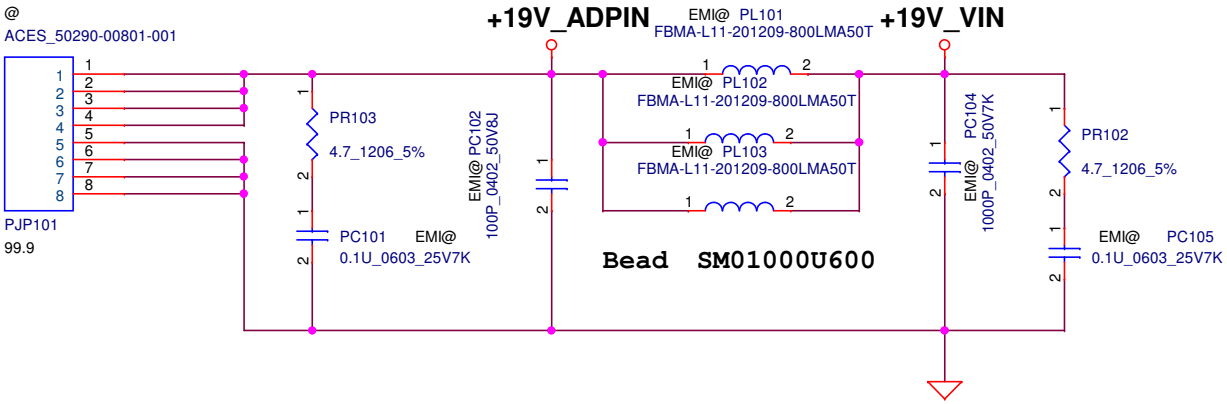
Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

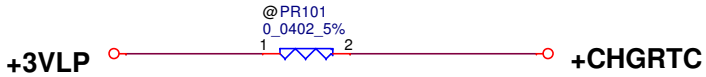
Compal Electronics, Inc.		
Title: Reserve Page		
Size: Custom	Document Number: EH50F M/B LA-H431PR10	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 79 of 100	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2019/12/28	Deciphered Date	2019/12/28

Compal Electronics, Inc.		
Title: Reserve Page		
Size: Custom	Document Number: EH50F M/B LA-H431PR10	Rev: 1.0
Date: Wednesday, February 13, 2019	Sheet 80 of 100	





Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

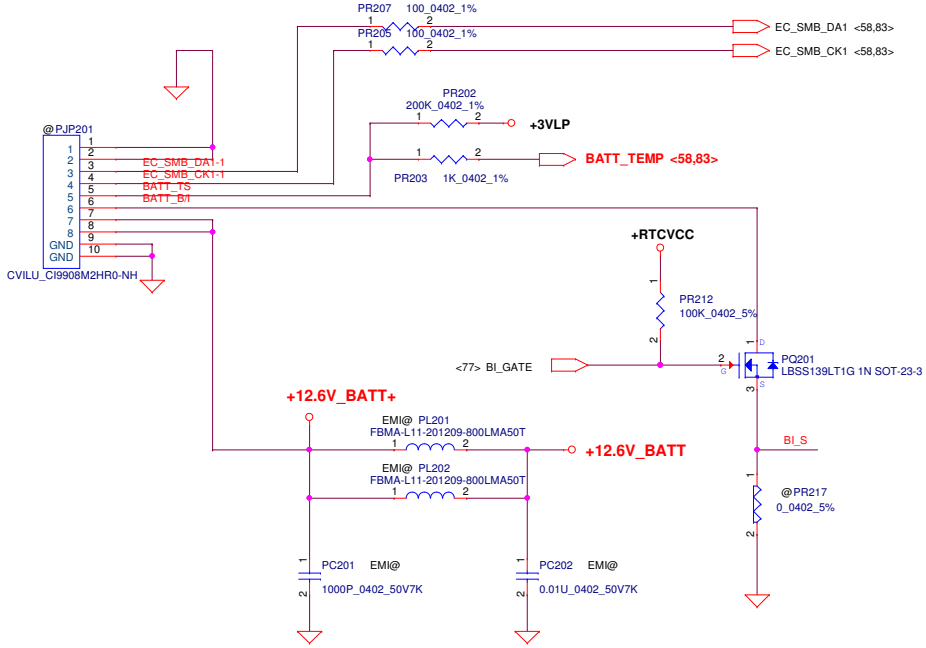
Title: **DCIN**

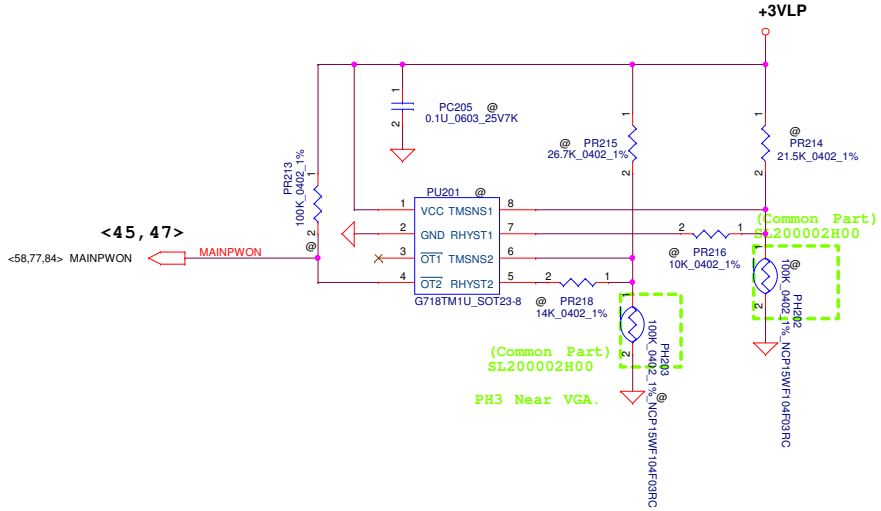
Size	Document Number	Rev
Custom	DH53F M/B LA-F991P	0.1

Date: Wednesday, February 13, 2019 | Sheet 81 of 100

Battery Bot Side

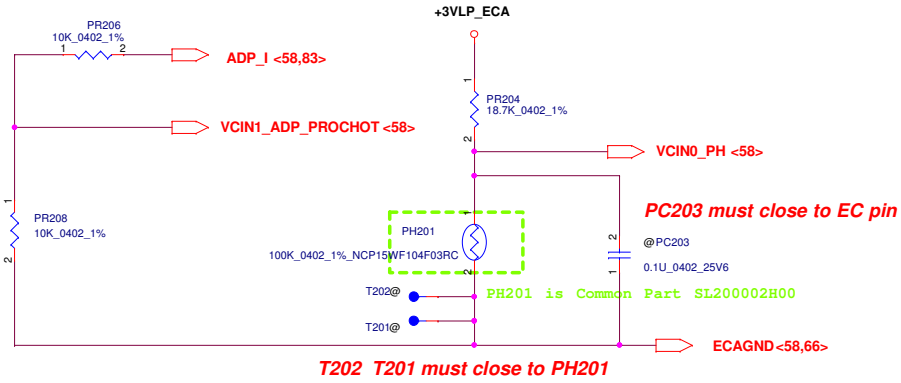
PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+





When PR204=18.7K

For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	89'C, 1V	56'C, 2V
PH202(ohm)	8.0524K	26.11K



T202 T201 must close to PH201

```
ADP_I=20*I(adapter)*0.01
I(adapter)=adapter(W)*130%/19
```

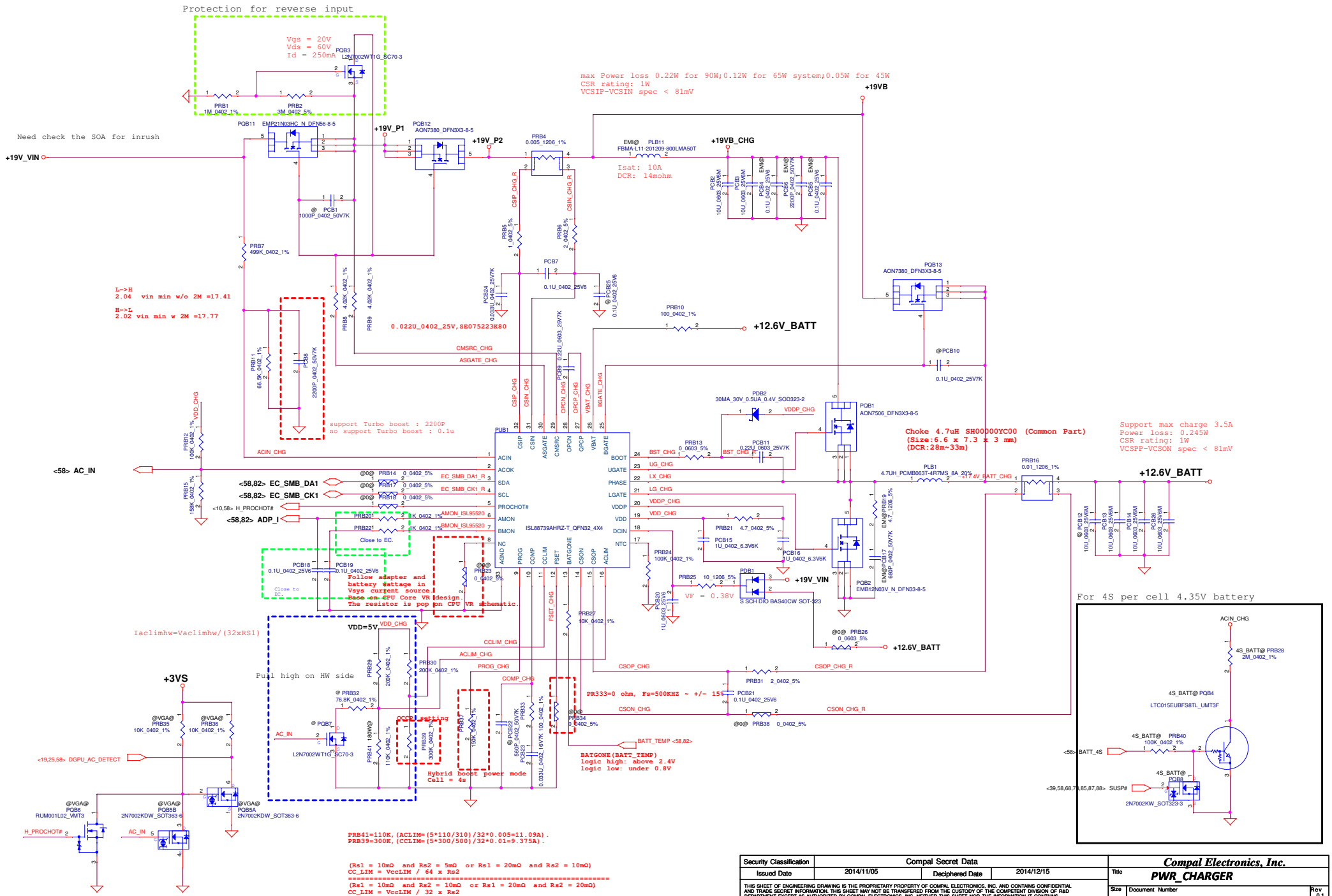
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: **BATTERY CONN/OTP**

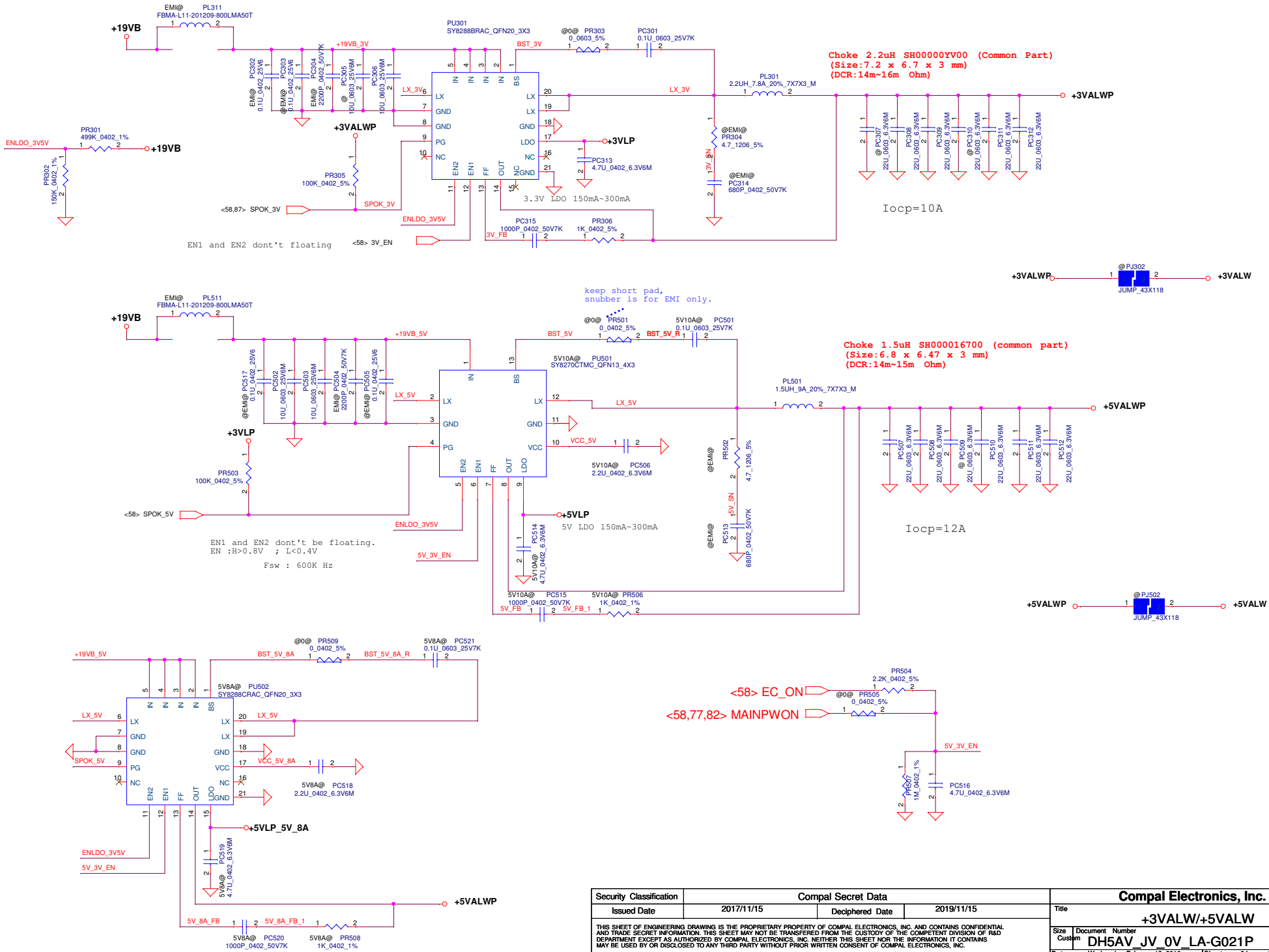
Size: Custom | Document Number: **DH53F M/B LA-F991P** | Rev: 0.1

Date: Wednesday, February 13, 2019 | Sheet 82 of 100



Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

Compal Electronics, Inc.	
Title	PWR_CHARGER
Size	Document Number
Rev	0.1
Date:	Wednesday, February 13, 2019
Sheet	83 of 100



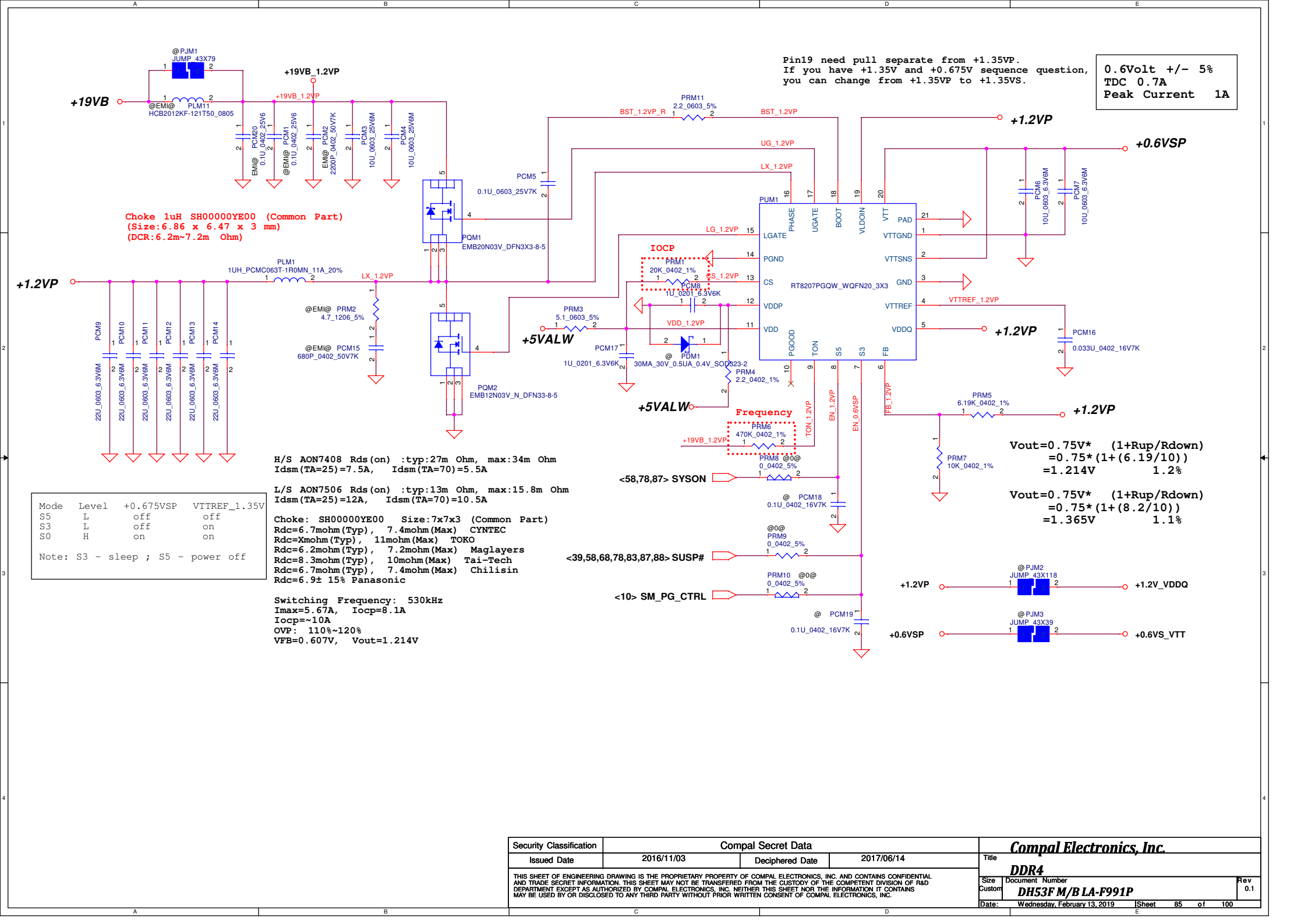
Security Classification	Compal Secret Data		
Issued Date	2017/11/15	Deciphered Date	2019/11/15

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	0.1

Date: Wednesday, February 13, 2019 Sheet 84 of 100



Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

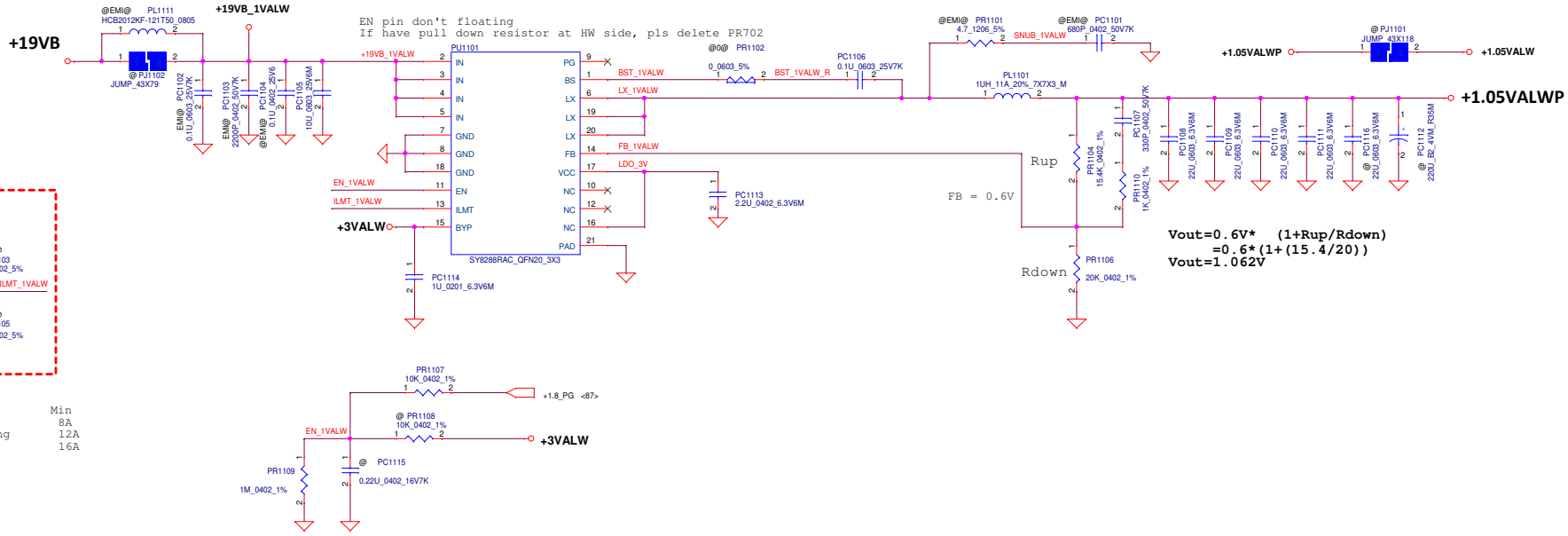
Compal Electronics, Inc.

Title: DDR4

Size: Custom | Document Number: DH53F M/B LA-F991P | Rev: 0.1

Date: Wednesday, February 13, 2019 | Sheet 85 of 100

Choke 1uH SH00000YE00 (Common Part)
(Size:6.86 x 6.47 x 3 mm)
(DCR:6.2m~7.2m Ohm)
Choke: SH00000YE00 Size:7x7x3 (Common Part)
Rdc=6.7mohm(Typ), 7.4mohm(Max) CYNTEC
Rdc=Xmohm(Typ), 11mohm(Max) TOKO
Rdc=6.2mohm(Typ), 7.2mohm(Max) Maglayers
Rdc=8.3mohm(Typ), 10mohm(Max) Tai-Tech
Rdc=6.7mohm(Typ), 7.4mohm(Max) Chilisin
Rdc=6.9± 15% Panasonic



Vout=0.6V* (1+Rup/Rdown)
=0.6*(1+(15.4/20))
Vout=1.062V

8288RAC

	Min
ILMT='0'	8A
ILMT=Floating	12A
ILMT='1'	16A

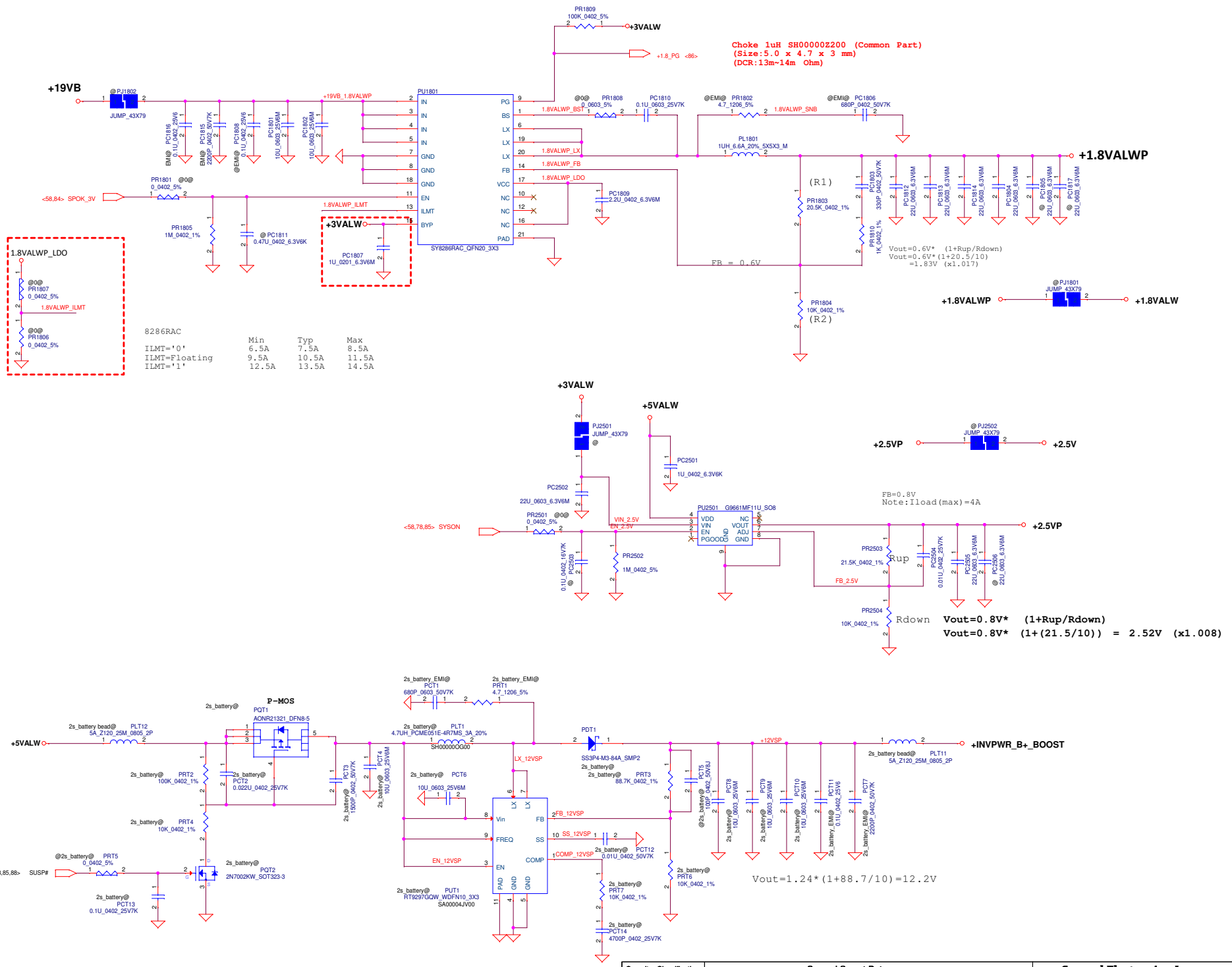
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: 1V

Size	Document Number	Rev
C	DH53F M/B LA-F991P	0.1

Date: Wednesday, February 13, 2019 Sheet 86 of 100



Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

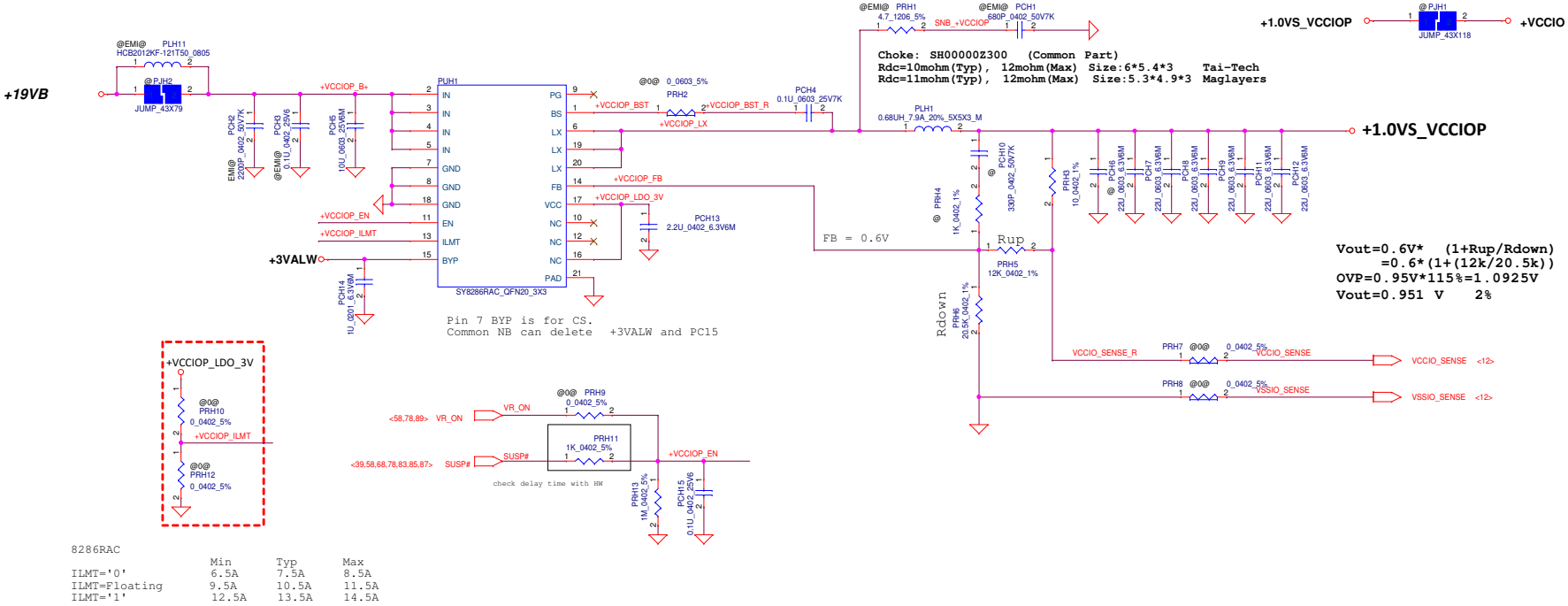
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: 1.5VS/2.5V

Size	Document Number	Rev
C	DH53F M/B LA-F991P	0.1

Date: Wednesday, February 13, 2019 Sheet 87 of 100



8286RAC

	Min	Typ	Max
ILMT='0'	6.5A	7.5A	8.5A
ILMT=Floating	9.5A	10.5A	11.5A
ILMT='1'	12.5A	13.5A	14.5A

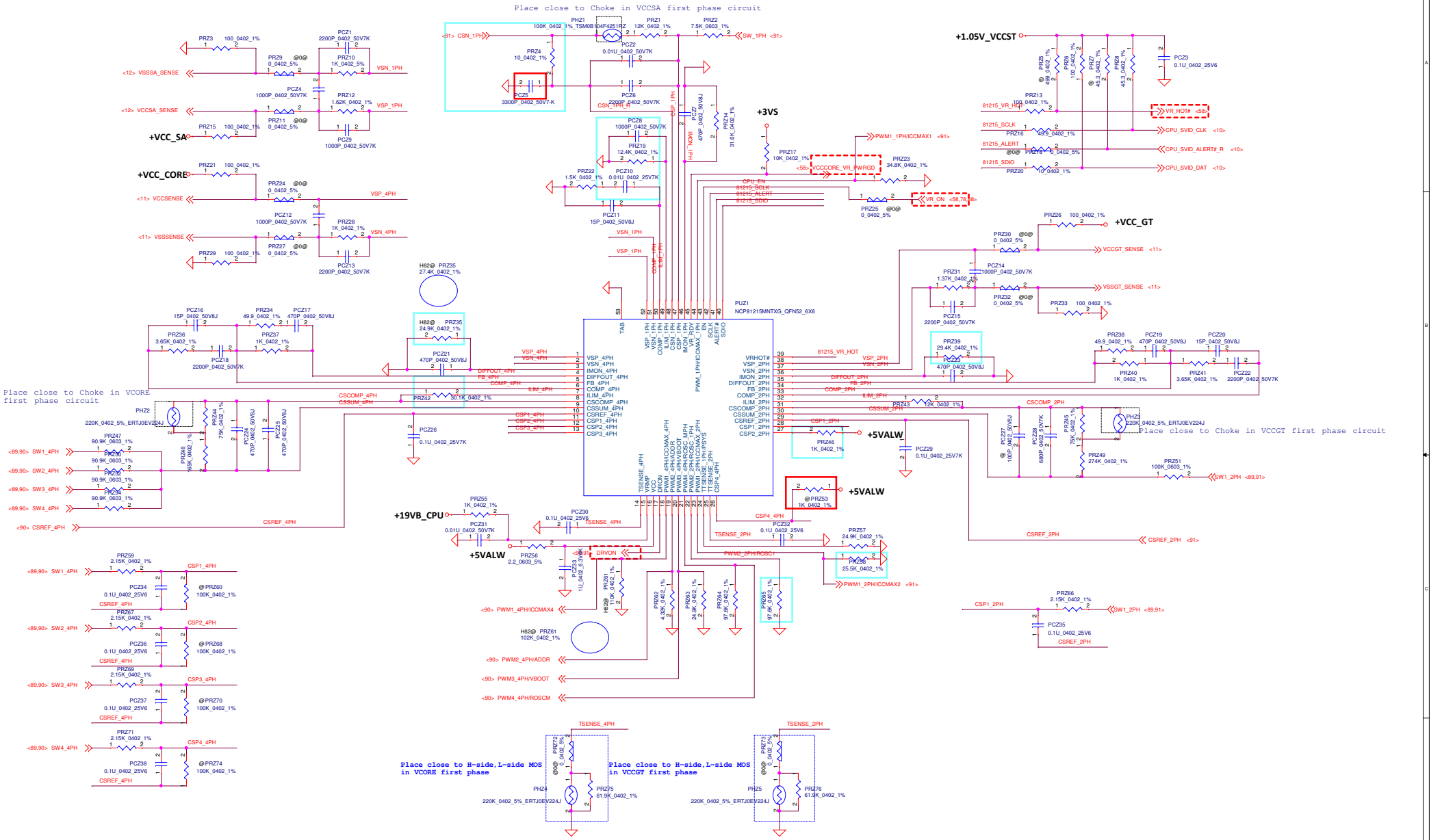
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: DH53F M/B LA-F991P

Size: C | Document Number: 1.0VS_VCCIO | Rev: 0.1

Date: Wednesday, February 13, 2019 | Sheet 88 of 100

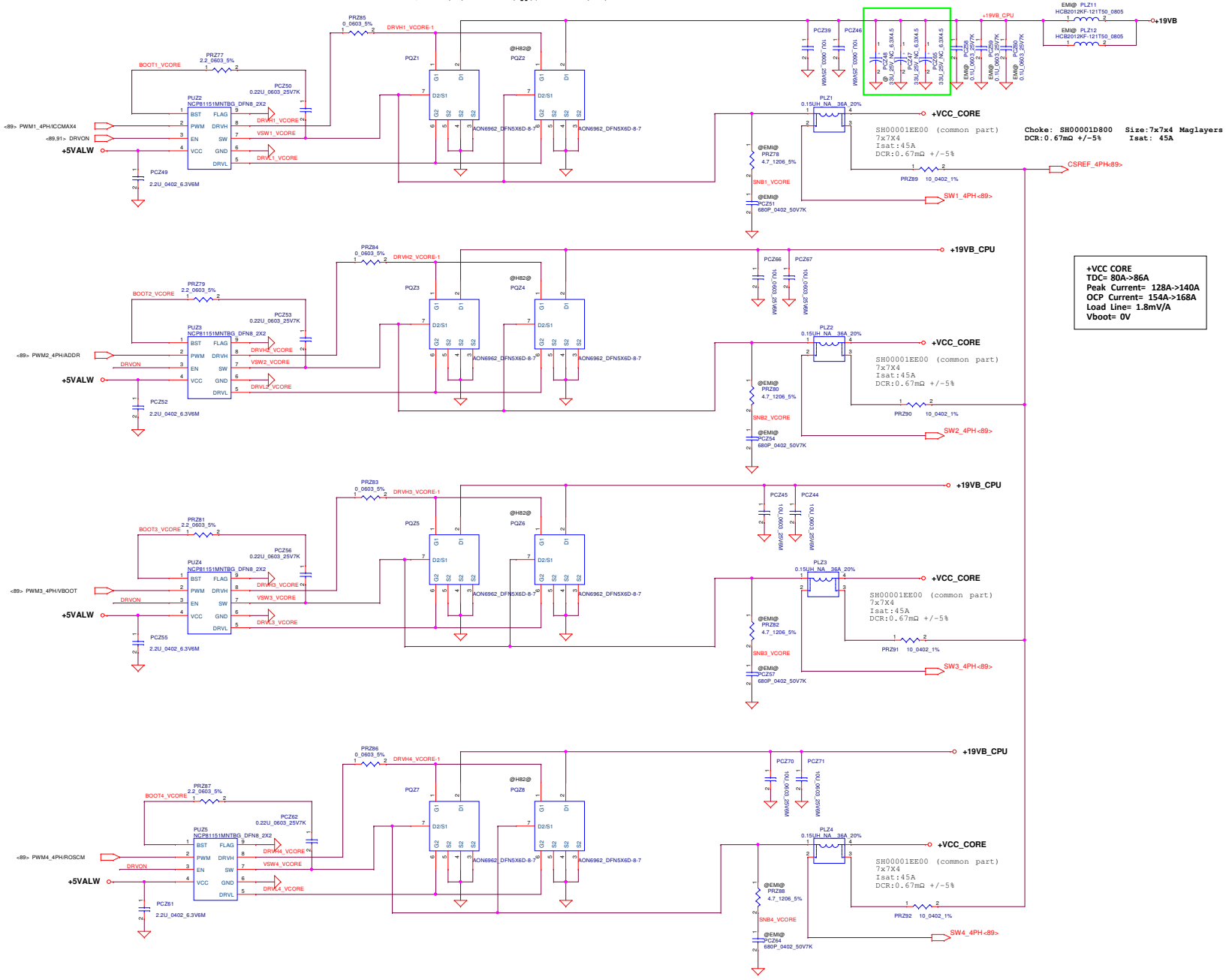


Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

Title	Compal Electronics, Inc.		
Size: Custom	Document Number: CPU IC SKL_H 42		Rev: 0.1
Date: Wednesday, February 13, 2019	Sheet 89 of 100		

Main Func = CORE

MOSFET: DFN 5X6E
H/S Rds(on): 5.2mohm(Typ), 7mohm(Max)
L/S Rds(on): 0.8mohm(Typ), 1.05mohm(Max)

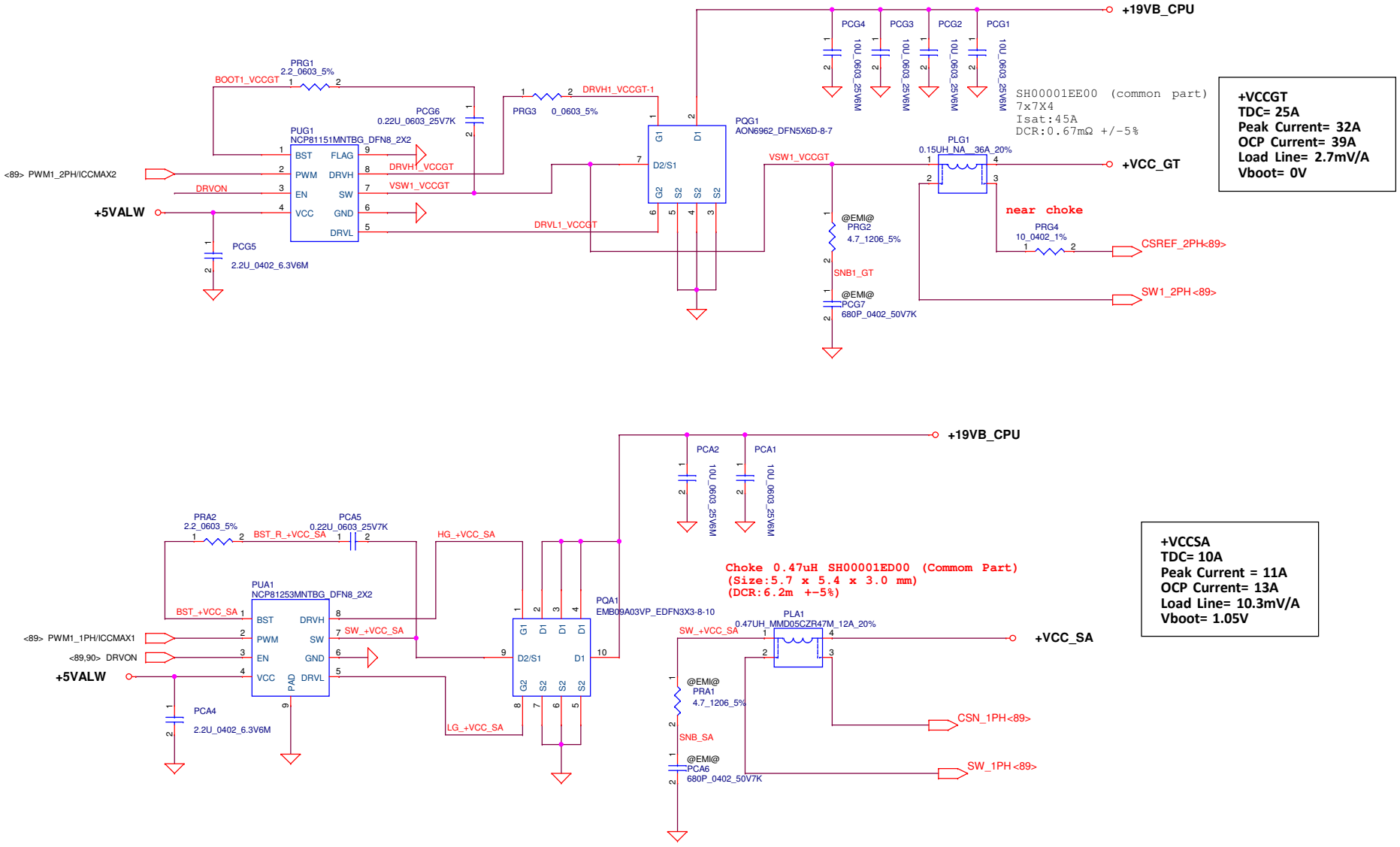


+VCC CORE
TDC= 80A->86A
Peak Current= 128A->140A
OCP Current= 154A->168A
Load Line= 1.8mV/A
Vboot= 0V

Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

Title: CPU_CORE
Size: Custom | Document Number | Rev: 0.1
Date: Wednesday, February 13, 2019 | Sheet 90 of 100

Main Func = VCCGT/+VCCSA



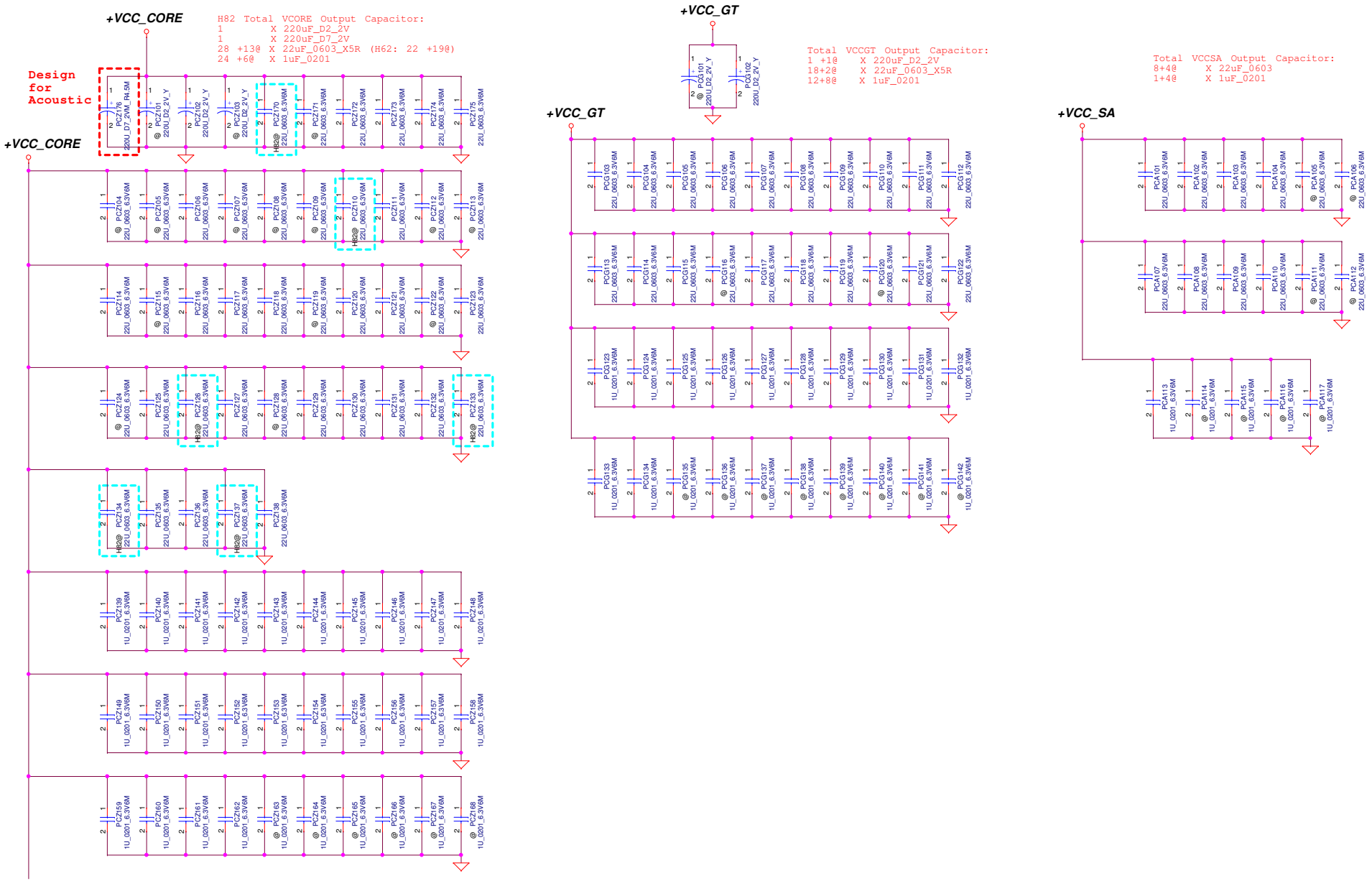
Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: +VCC_GT/+VCC_SA

Size	Document Number	Rev
	C1PRG_LA-E051P	0.1

Date: Wednesday, February 13, 2019 | Sheet 91 of 100



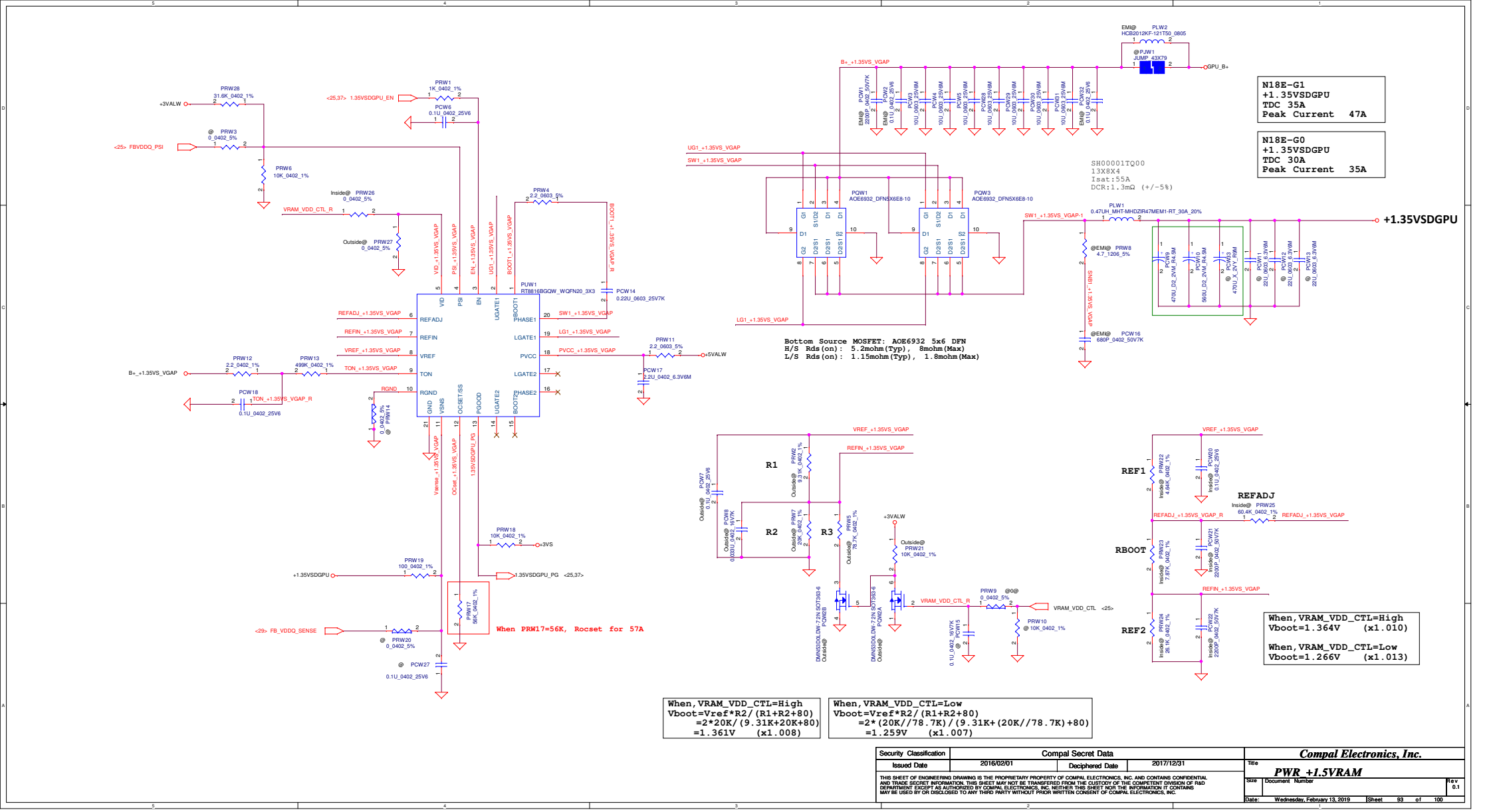
Security Classification	Compal Secret Data		
Issued Date	NA	Deciphered Date	2014/07/04

Compal Electronics, Inc.

Title: DH53F M/B LA-F991P

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, February 13, 2019 Sheet 92 of 100



Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

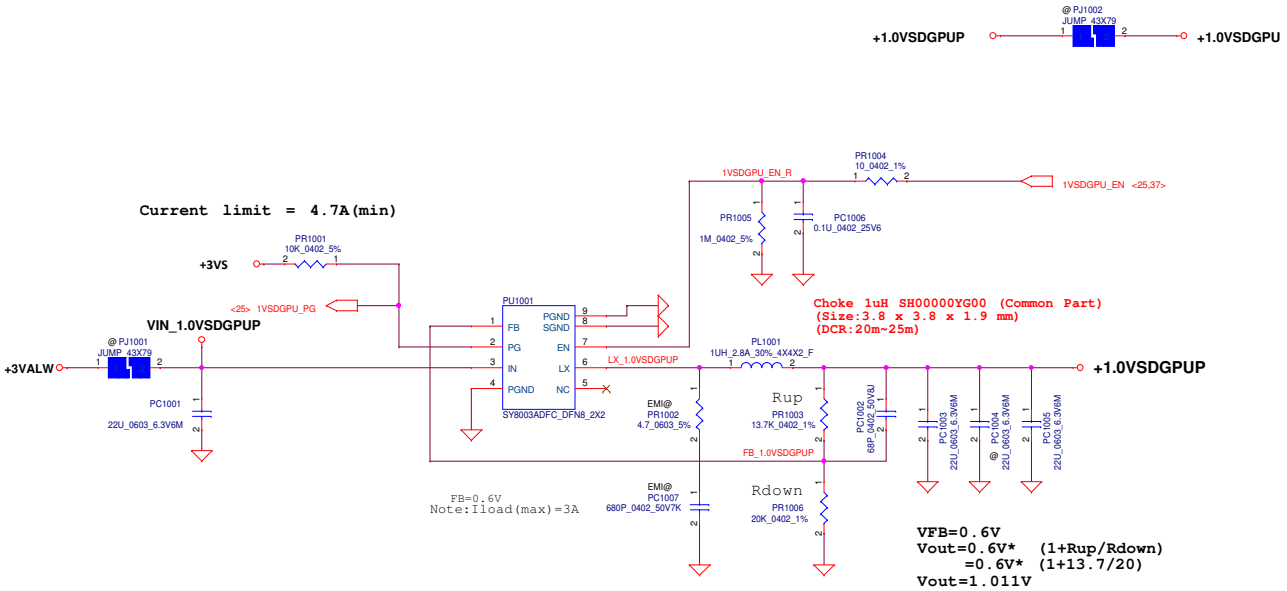
Compal Electronics, Inc.

Title: **PWR_+1.5VRAM**

Size: | Document Number: | Rev: 0.1

Date: Wednesday, February 13, 2019 | Sheet 93 of 100

SKL_H 42



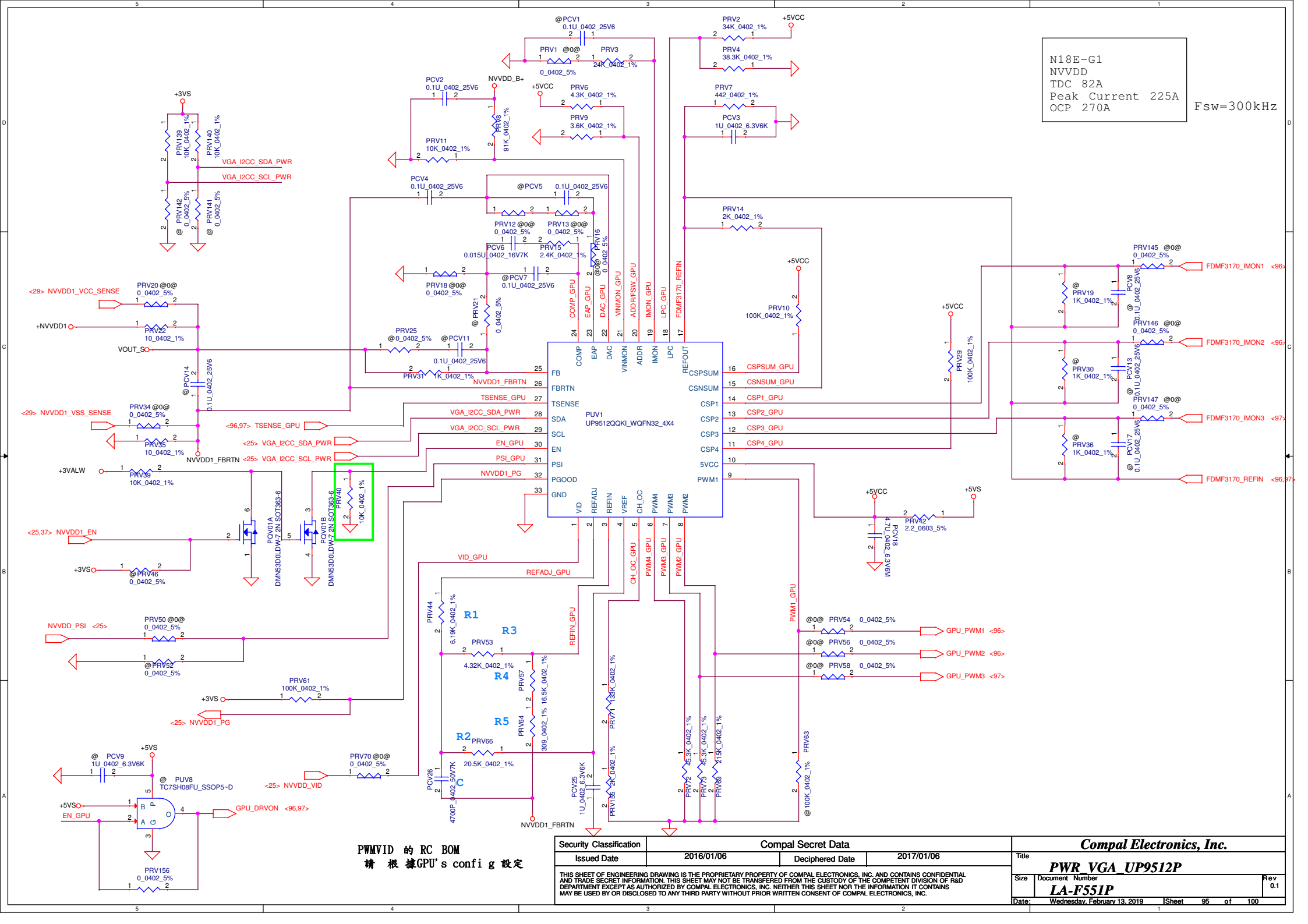
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

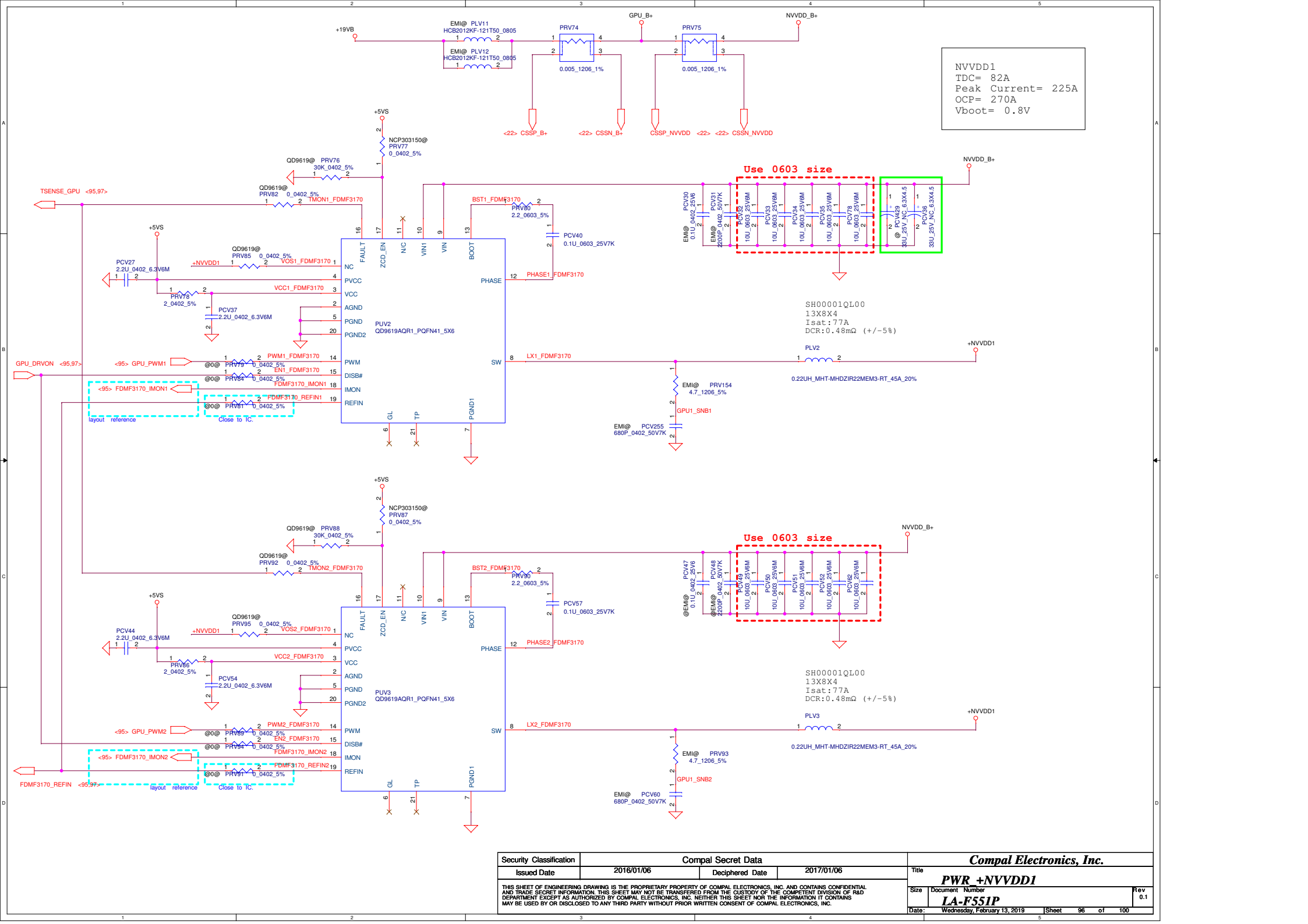
Compal Electronics, Inc.

Title: 1.05VSDGPU

Size	Document Number	Rev
C	DH53F M/B LA-F991P	0.1

Date: Wednesday, February 13, 2019 Sheet 94 of 100


N18E-G1
NVVDD
TDC 82A
Peak Current 225A
OCP 270A
Fsw=300kHz
PUV1
UP9512QQKI_WQFN32_4X4
PUV8
TC7SH08FU_SSOP5~D
PQV01A
DMN53D0LDW-7 2N SOT363-6
PQV01B
DMN53D0LDW-7 2N SOT363-6
PWMVID 的 RC BOM
請 根 據GPU's confi g 設定
Security Classification
Compal Secret Data
Issued Date
2016/01/06
Deciphered Date
2017/01/06
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
PWR_VGA_UP9512P
Size
Document Number
LA-F551P
Rev
0.1
Date: Wednesday, February 13, 2019
Sheet 95 of 100



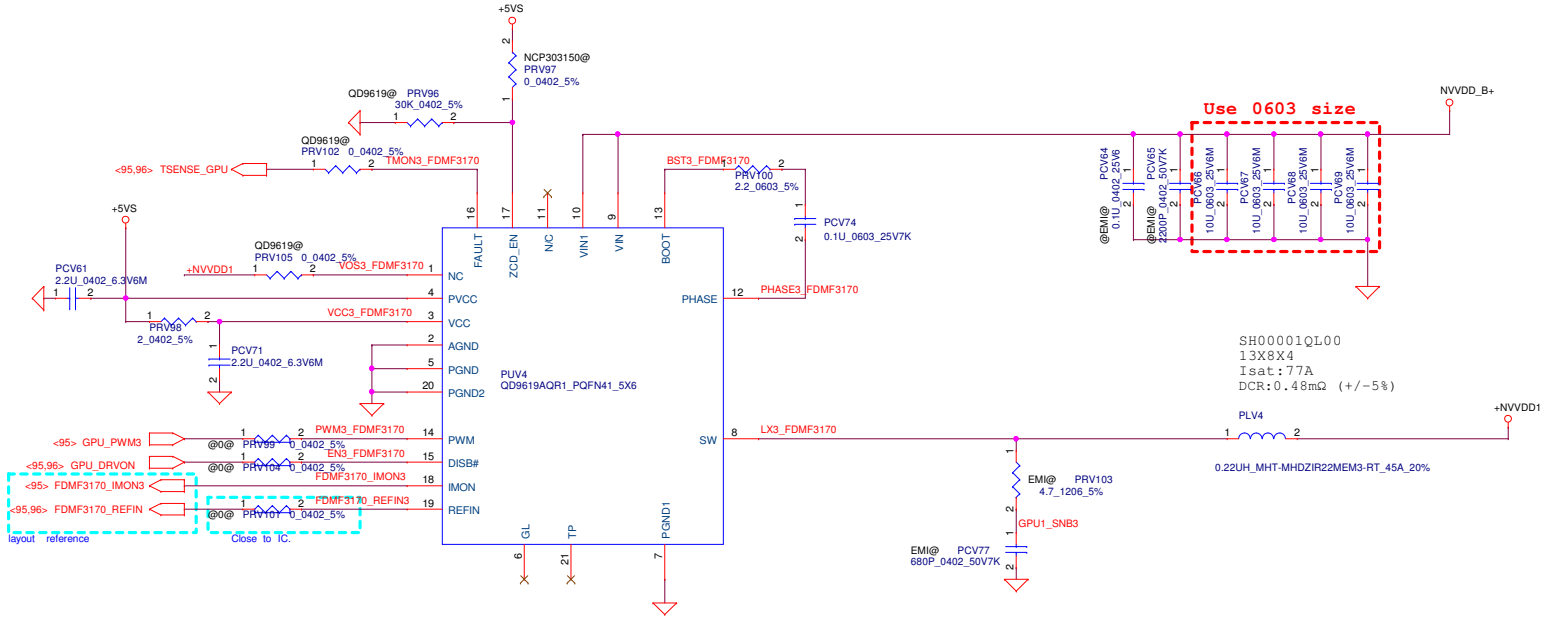
Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PWR_+NVVDD1**

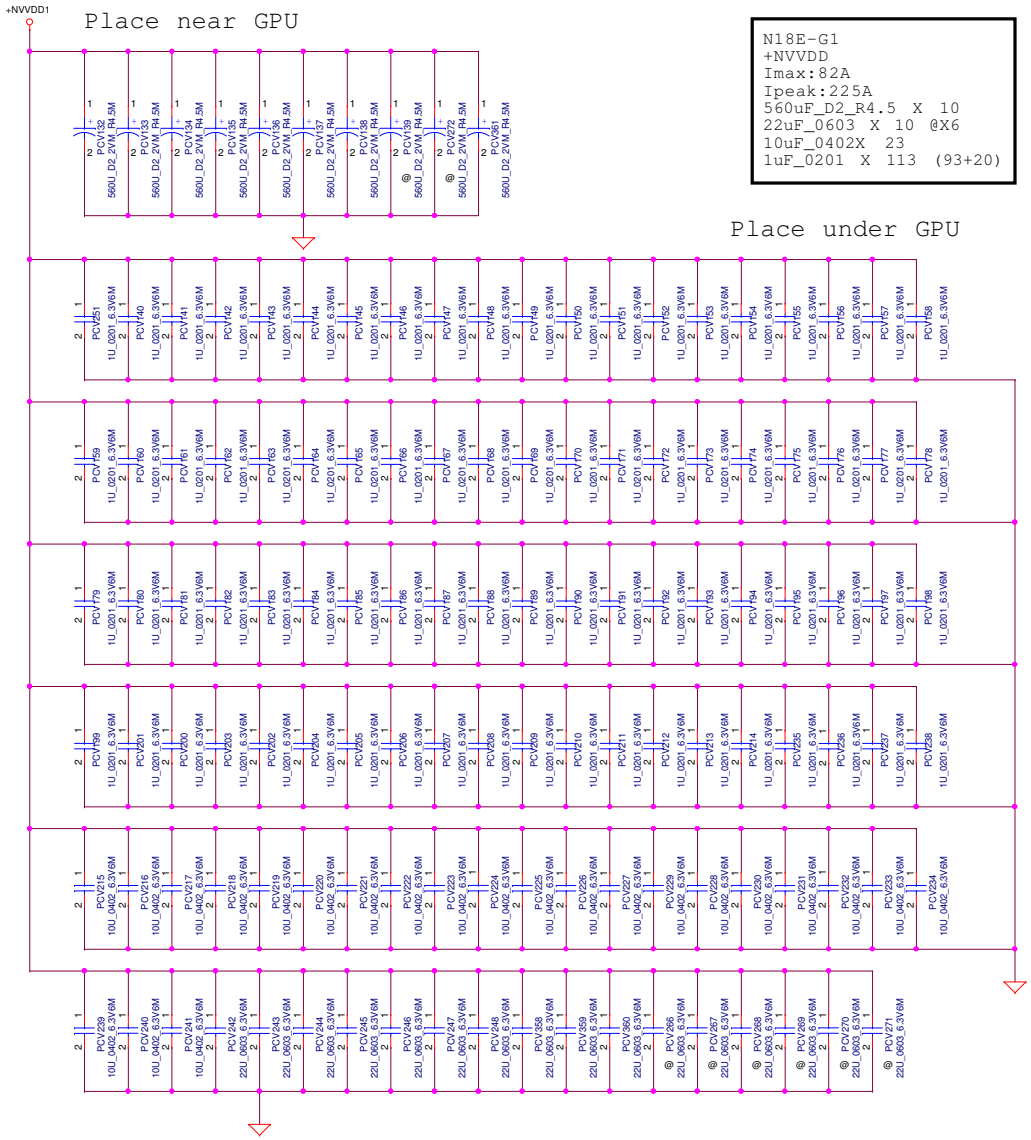
Size	Document Number	Rev
	LA-F551P	0.1

Date: Wednesday, February 13, 2019 | Sheet 96 of 100



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

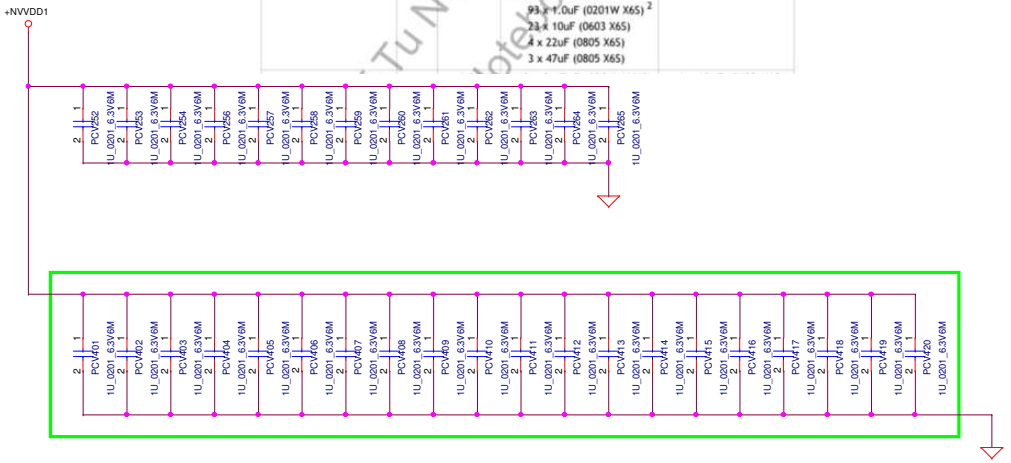
Compal Electronics, Inc.		
Title: PWR_+NVVDD1		
Size	Document Number: LA-F551P	Rev: 0.1
Date: Wednesday, February 13, 2019	Sheet 97 of 100	




```
N18E-G1
+NVVDD
Imax:82A
Ipeak:225A
560uF_D2_R4.5 X 10
22uF_0603 X 10 @X6
10uF_0402X 23
1uF_0201 X 113 (93+20)
```

Table 5.10 GB4B-256 Power Rail Filtering

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 x 0.47uF (0201W X6S) 23 x 10uF (0603 X6S) 4 x 22uF (0805 X6S) 3 x 47uF (0805 X6S) --- Alternate solution: 93 x 1.0uF (0201W X6S) [2] 23 x 10uF (0603 X6S) 4 x 22uF (0805 X6S) 3 x 47uF (0805 X6S)	2 x 470uF (Poscap)



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.	
Title	PWR_VGA DECOUPLING
Size	Document Number: LA-F551P
Rev	0.1
Date: Wednesday, February 13, 2019	Sheet 98 of 100

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Update	EVT EA Tuning	0.2	P86, P93 P95, P98	Change the PCV139, PCV272 from pop to un-pop. Change the PRW13 from 383K_0402_1% (SD034383380) to 499K_0402_1% (SD034499380). Change the PCW27 from pop to un-pop, and . PCW27.2 net name change from +1.35VSDGPU to Vsense_+1.35VS_VGAP. Change the PCW21, PCW22 From 4700P_0402_50V (SE074472K80) to 2200P_0402_50V(SE074222K80). Change the PUV8, PCV9 from pop to un-pop. Add location PRV156 0_0402_5% (SD028000080), and pop. Add location PC1116 22U_0603_6.3V (SE00000M000), and un-pop. Change the PRW17 from 56.2K_0402_1% (SD000001580) to 56K_0402_1% (SD034560280).	11/12	B
02	Design Update	Power Sequence	0.2	P93, P94	Change the PRW1 from 20K_0402_1% (SD034200280) to 1K_0402_1% (SD034100180). Change the PR1001 From 100K_0402_5% (SD028100380) to 10K_0402_5% (SD028100280).	11/13	B
03	Design Update	Solution Change	0.2	P83, P85	Change the PQB2,PQM2 from AON7506 (SB000010A00) to EMB12N03V (SB00001HV00). PQB1,PQB12,PQB13,PQM1,PQT1 footprint change to common footprint. PCZ47,PCZ65,PCV36 change to common part P/N (SF000007200). PLZ1,PLG1,PLZ2,PLZ3,PLZ4 change to common part P/N (SH00001EE00).	11/13	B
03	Design Update	Location modify	0.2	P91	Change the location from PRG5 to PUG1. Change the location from PRA3 to PUA1.	11/13	B
04	Design Update	0 ohm to R-short	0.2	P82	PR217 change from 0 ohm to R-short.	11/16	B
05	Design Update	EMI request	0.2	P93	PLW2, PCW1, PCW2, PCW32 change from un-pop to pop.	11/22	B
06	Design Update	CPU test result	0.2	P89, P92	Change the PRZ12 from 1.78K_0402_1% (SD00000WY80) to 1.62K_0402_1% (SD000003380). Change the PCZ25 from 680P_0402_50V7K (SE074681K80) to 470P_0402_50V8J (SE071471J80). Change the PRZ51 from 84.5K_0603_1% (SD014845280) to 100K_0603_1% (SD014100380). Change the PRZ35 from 25.5K_0402_1% (SD034255280) to 24.9K_0402_1% (SD034249280) . ->H82@ Change the PRZ35 from 25.5K_0402_1% (SD034255280) to 27.4K_0402_1% (SD034274280) . ->H62@ Change the PRZ61 from 110K_0402_1% (SD034110380) to 102K_0402_1% (SD028102380) . ->H62@ Change the PCZ101,PCZ104,PCZ105,PCZ122,PCZ112,PCZ107,PCZ124,PCZ171,PCZ119 from pop to un-pop. ->H82@ Change the PCZ101,PCZ104,PCZ105,PCZ122,PCZ112,PCZ107,PCZ124,PCZ171,PCZ119, PCZ110,PCZ126,PCZ133,PCZ134,PCZ137,PCZ170 from pop to un-pop. ->H62@	11/22	B
07	Design Update	Solution Change	0.3	P84, P89	Change the PRZ43 from 12.1K_0402_1% (SD034121280) to 12K_0402_1% (SD034120280). Change the PL501 P/N From SH00000II00 to SH000016700 (commonpart).	12/07	C
08	Design Update	Power Sequence	0.3	P87	PC1811 (0.47_0402_6.3V, SE124474K80) change from pop to un-pop.	12/11	C
09	Design Update	Solution Change	1.0	P83	Add location PDB2 30MA_30V_0.5UA_0.4V_SOD323-2 (SCS00009P00), and un-pop.	12/19	C
10	Design Update	Solution Change	1.0	P92	PCG116, PCG120 change from pop to un-pop (22uF_0603_6.3V, SE00000M000). PCG107, PCG108 change from un-pop to pop (22uF_0603_6.3V, SE00000M000).	12/21	C
11	Design Update	0 ohm to R-short	1.0	P85, P87 P89, P93 P95, P96 P97	PRM8,PRM10,PRW9,PRZ25,PR1801,PR2501 change from 0 ohm to R-short. PRZ9,PRZ11,PRZ18,PRZ24,PRZ27,PRZ30,PRZ32,PRZ72,PRZ73 change from 0 ohm to R-short. PRV1,PRV16,PRV18,PRV20,PRV34,PRV50,PRV54,PRV56,PRV58,PRV70,PRV145,PRV146,PRV147 change from 0 ohm to R-short. PRV12,PRV13,PRV84,PRV94,PRV104,PRV79,PRV81,PRV89,PRV91,PRV99,PRV101 change from 0 ohm to R-short.	12/28	C
12	Design Update	Solution Change	1.0	P90, P96	PCZ47,PCZ65,PCV36 (33U_25V_4.5mm OS con) change from SF000007200 to SF000007700 and pop. PCZ48,PCV429 (33U_25V_4.5mm OS con) change from SF000007200 to SF000007700 and un-pop.	01/04	C
13	Design Update	Power Sequence	1.0	P94	PR1004 change from 0_0402_5% (SD028000080) to 10_0402_5% (SD034100A80). PC1006 change from un-pop to 0.1uF_0402_25V (SE00000G880).	01/14	C2
09	Design Update	Solution Change	1.0	P83	PDB2, 30MA_30V_0.5UA_0.4V_SOD323-2 (SCS00009P00), change from un-pop to pop.	02/01	C2

Compal Electronics, Inc.

Title: PIR

Size: Custom | Document Number: DH53F M/B LA-F991P | Rev: 0.1

Date: Wednesday, February 13, 2019 | Sheet 99 of 100

Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List	Date	Phase
01						
02						
03						
04						
05						
06						
07						
08						

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: PIR

Size: Custom | Document Number: DH53F M/B LA-F991P | Rev: 0.1

Date: Wednesday, February 13, 2019 | Sheet 100 of 100