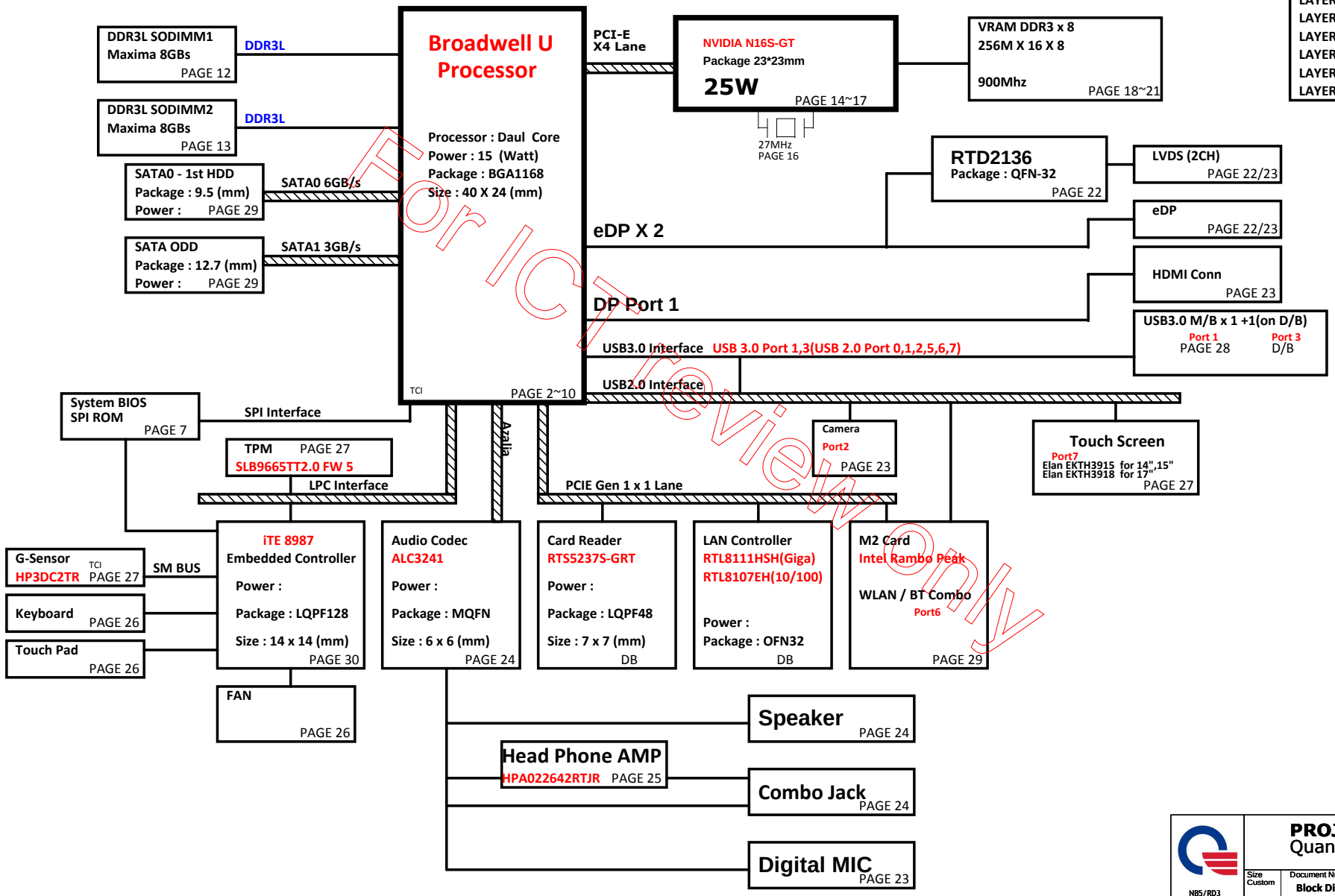
X12 DIS (14" / 15" / 17") Chocolate X12
Intel Cresent Bay ULT Platform Block Diagram

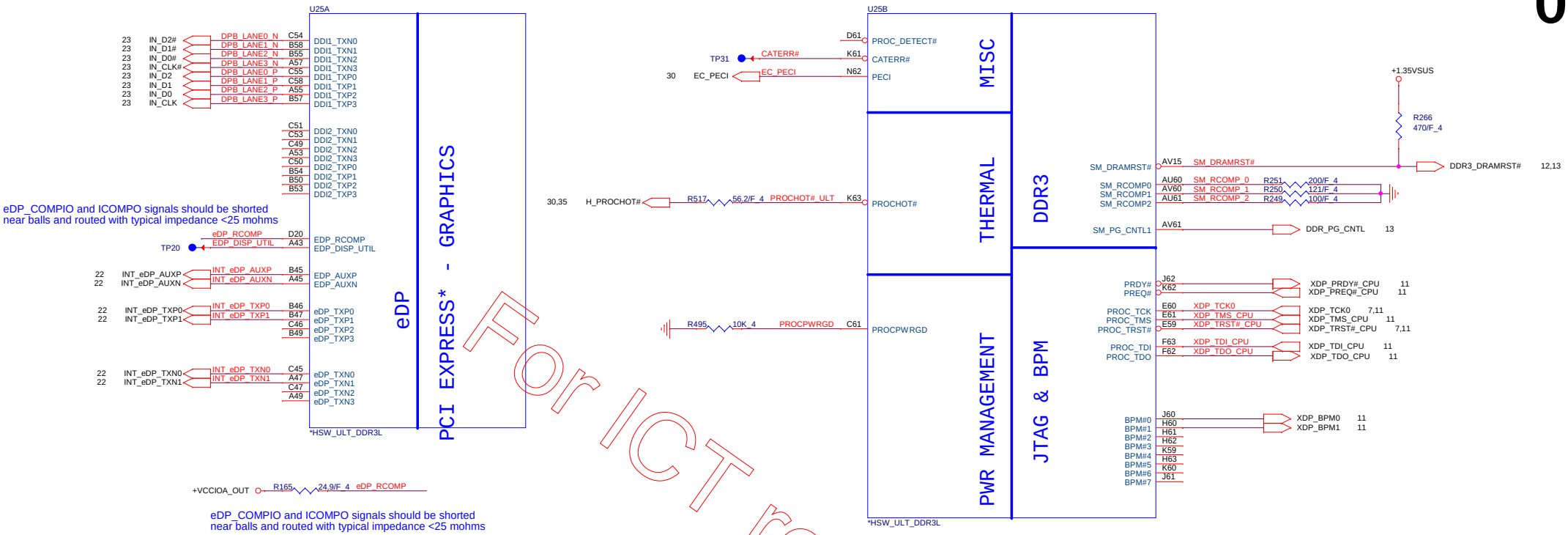
PCB 10L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : GND
LAYER 7 : IN3
LAYER 8 : IN4
LAYER 9 : GND
LAYER 10 : BOT



Note
VGA/CPU need check PN

NB5/RD3	PROJECT : X12 Quanta Computer Inc.	
Size: Custom	Document Number: Block Diagram	Rev: 1A
Date: Thursday, February 26, 2015	Sheet 1 of 40	

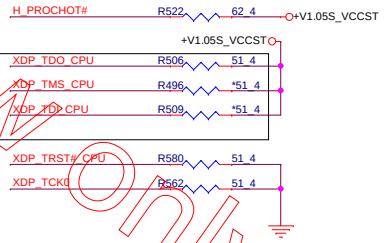


eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+VCCIOA_OUT R165 24.9/F_4 eDP_RCOMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Processor pull-up (CPU)



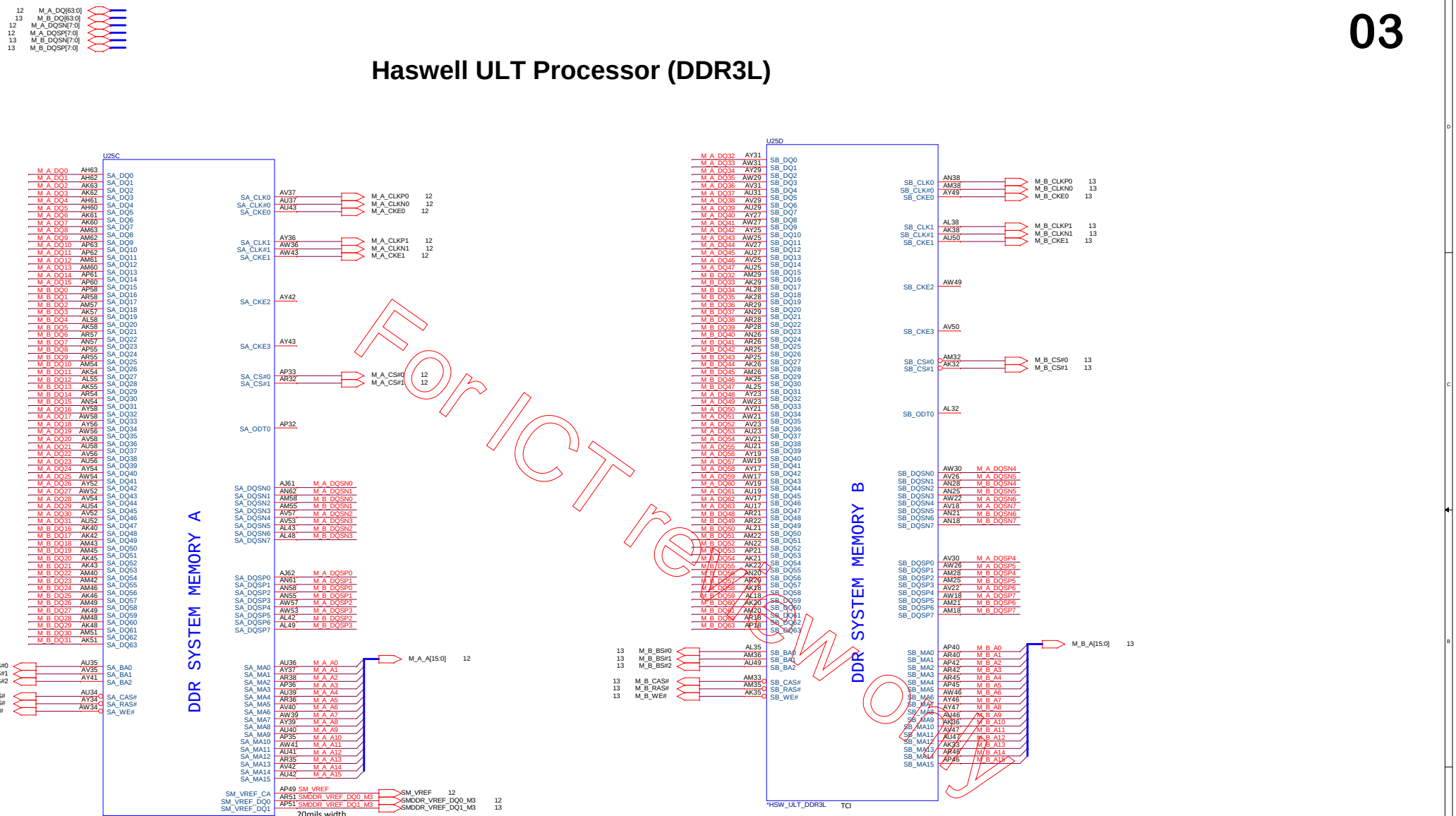
PROJECT : X12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 1/9(eDP/DDI)	1A

NB5/RD3

Date: Thursday, February 26, 2015 Sheet 2 of 40

Haswell ULT Processor (DDR3L)



NB5/RD3	PROJECT : X12 Quanta Computer Inc.		
	Size: Custom	Document Number: ULT 2/9 (DDR3 I/F)	Rev: 1A
	Date: Thursday, February 26, 2015	Sheet: 3 of 40	

POWER

HSW ULT POWER

32A
+VCC_CORE

1.4A
+1.35VSUS

Close to CPU

Direct tie to CPU VCC/VSS-Ball

CFG0-19 need Reserve TP

RESERVED

Layout note: need routing together and ALERT need between CLK and DATA.

SVID ALERT

SVID CLK

SVID DATA

Place PU resistor close to VR

100- ±1% pull-up to VCC near processor.

IO Thrm Protect

For 65 degree, 1.8v limit, (SW)

For 75 degree, 1.2v limit, (HW)

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

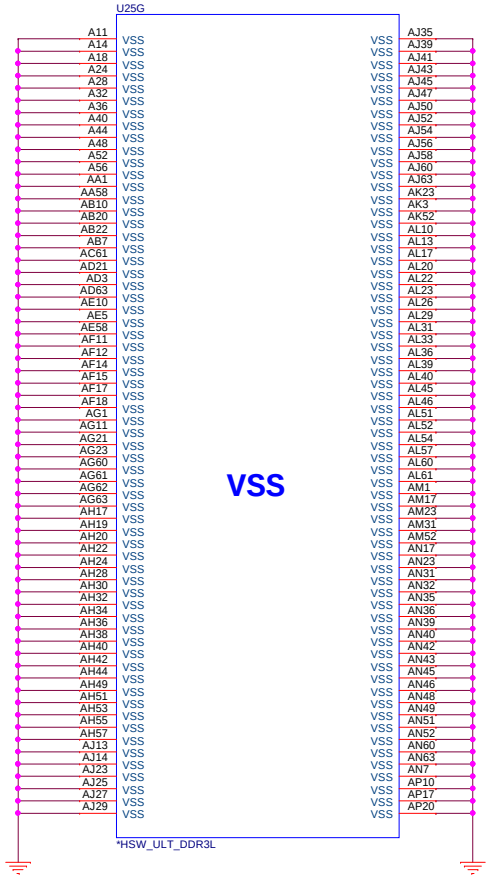
	1	0	Circuit
CFG3 (MSR Privacy Bit Feature)	Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting	IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden	CFG3 R543 *1K_4
CFG4 (eDP enable)	Disabled	Enabled	CFG4 R542 1K_4

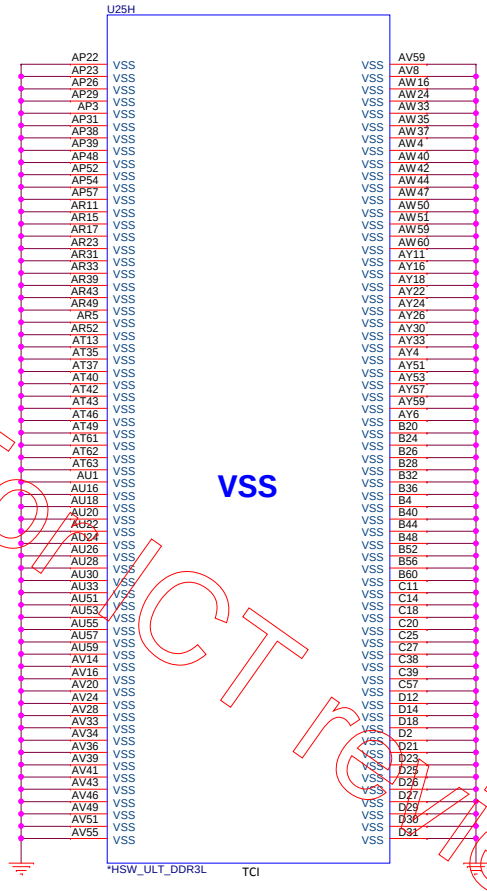
+VCCIOA_OUT 2
+VCCIO_OUT 6

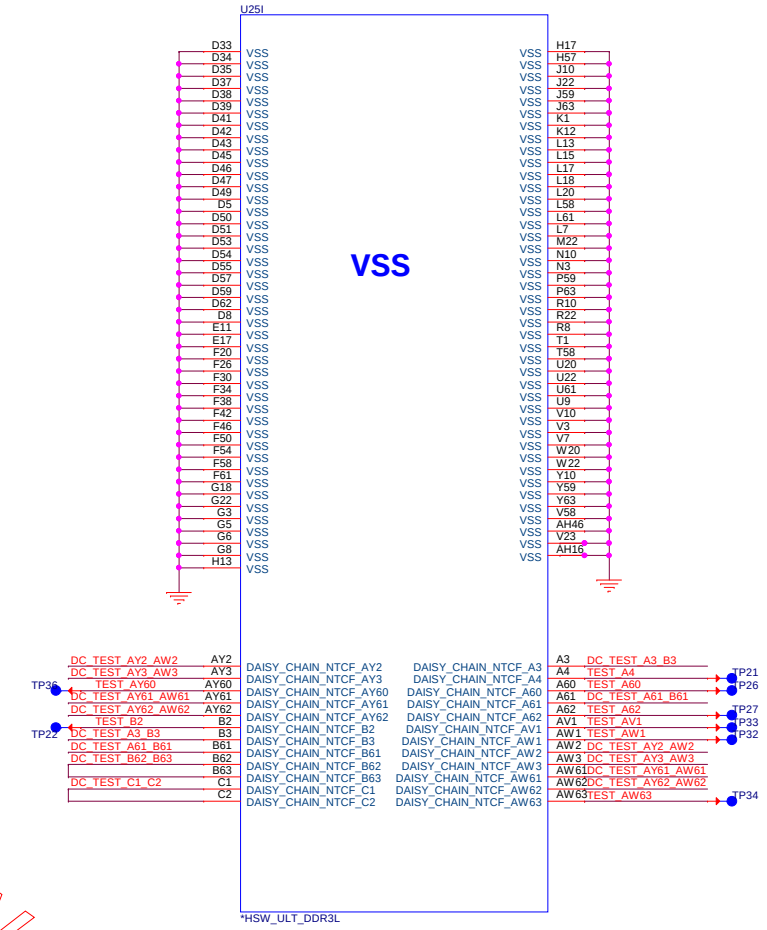
+1.35VSUS 2,12,13,33
+1.05V 2,7,9,10,11,27,30,34,35,36,39
+VCC_CORE 35

PROJECT : X12	
Quanta Computer Inc.	
Size: Custom	Document Number: 04 – ULT 3/9 (POWER-1)
Rev: 1A	
Date: Thursday, February 26, 2015	Sheet 4 of 40

NB5/RD3



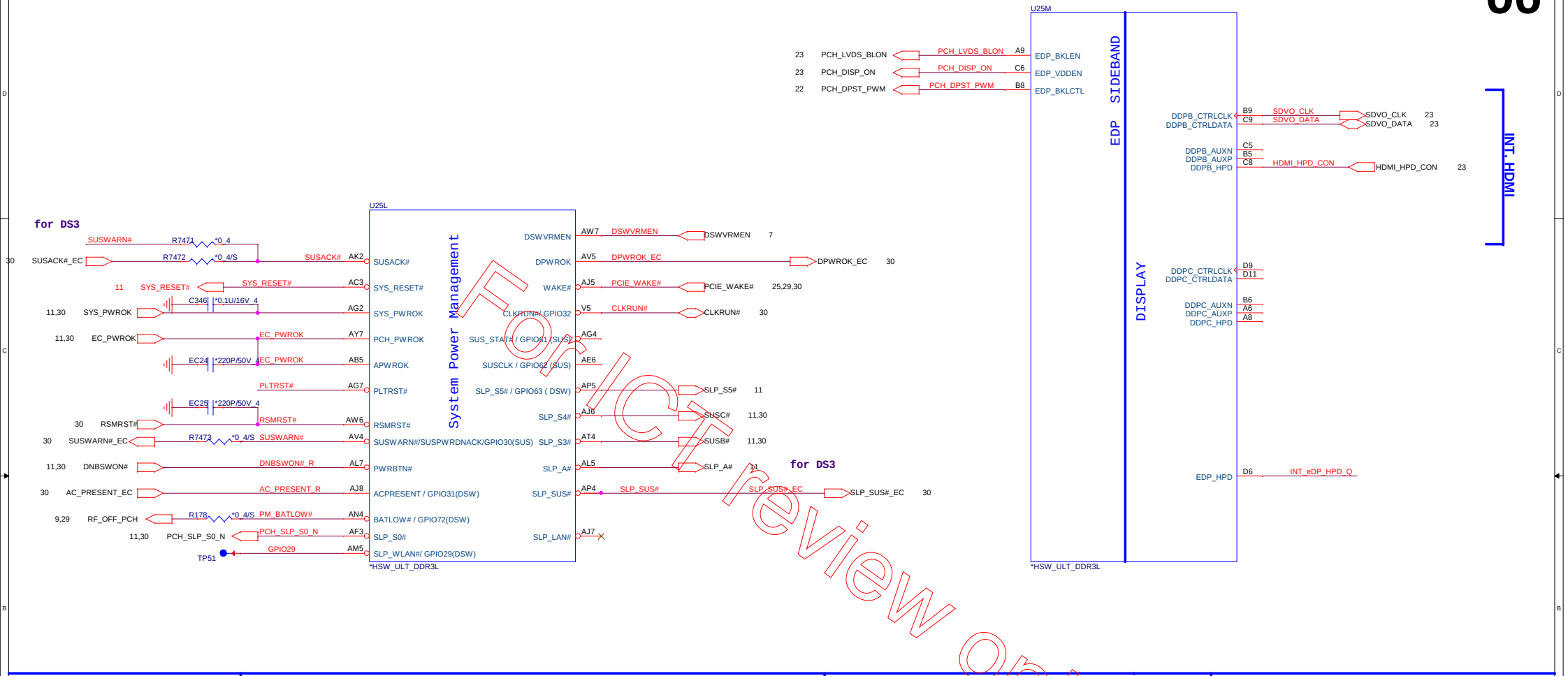




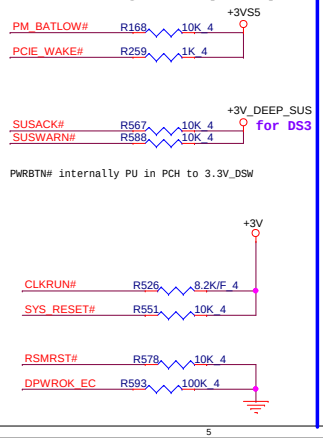
NB5/RD3	PROJECT : X12 Quanta Computer Inc.	
Size: Custom	Document Number: ULT 4/9 (RSV,GND)	Rev: 1A
Date: Thursday, February 26, 2015	Sheet 5 of 40	

Lynx Point-LP Platform Controller Hub (LVDS,DDI)

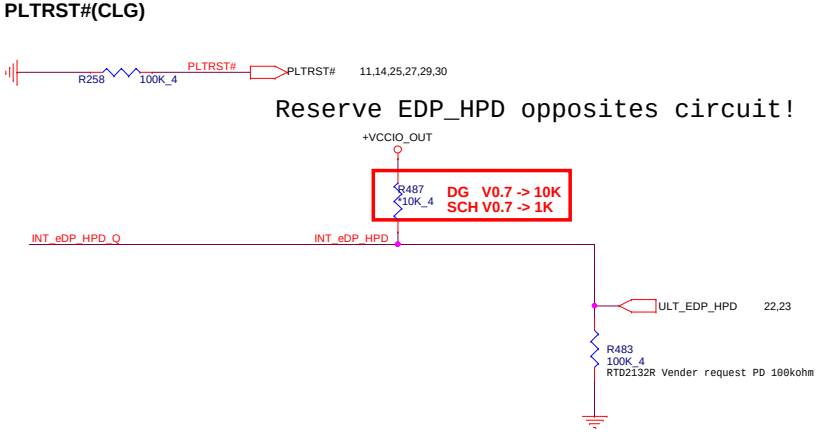
06



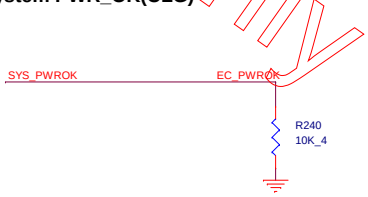
PCH Pull-high/low(CLG)



PLTRST#(CLG)



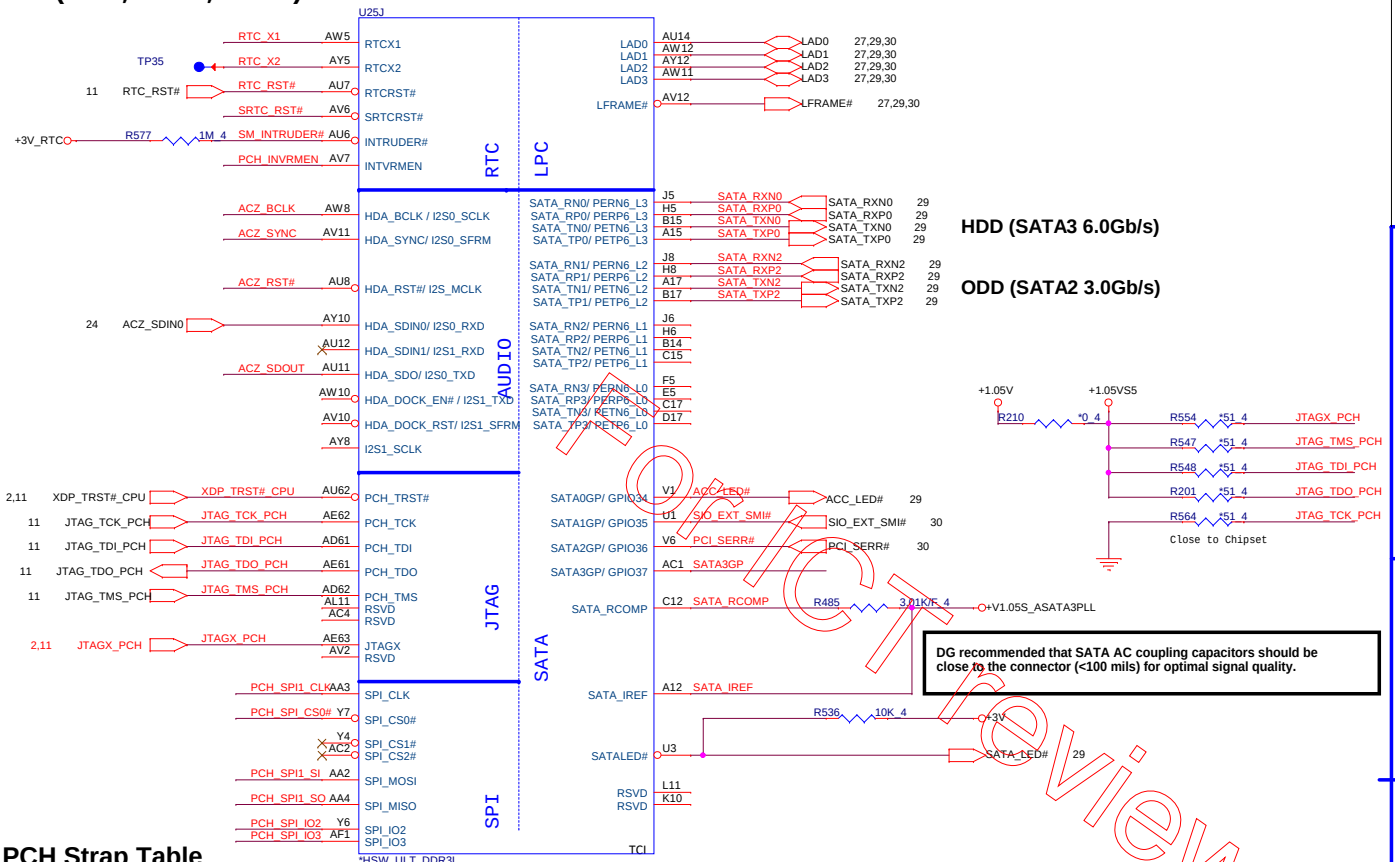
System PWR_OK(CLG)



7,8,9,10,11,12,13,14,15,16,22,23,24,25,26,27,29,30,35,36,37
9,10,11,27,29,30,32,34,36,39
+3V
+3VS5

N85/RD3	**PROJECT : X12** Quanta Computer Inc.	
Size: Custom	Document Number: ULT 5/9(Power Manger)	Rev: 1A
Date: Thursday, February 26, 2015	Sheet 6 of 40	

Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)



HDD (SATA3 6.0Gb/s)

ODD (SATA2 3.0Gb/s)

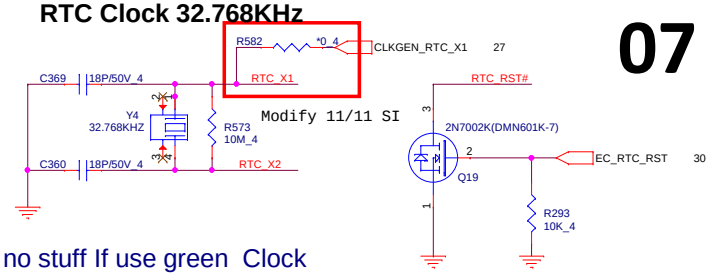
DG recommended that SATA AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R575 330K_4 PCH_INVRMEN
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overridden	30 GPIO33_EC R581 1K_4 ACZ_SDOUT
GSPI0_MOSI /GPIO86	Boot BIOS Selection	PWROK	GNT0# 1 = LPC; GNT0# 0 = SPI(Default)	
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality	
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	+3V_RTC R576 330K_4 DSWVRMEN 6
				30 PCH_SPI_CS0#_R → PCH_SPI_CS0#_R 30 PCH_SPI1_CLK_R → PCH_SPI1_CLK_R 30 PCH_SPI1_SI_R → PCH_SPI1_SI_R 30 PCH_SPI1_SO_R → PCH_SPI1_SO_R

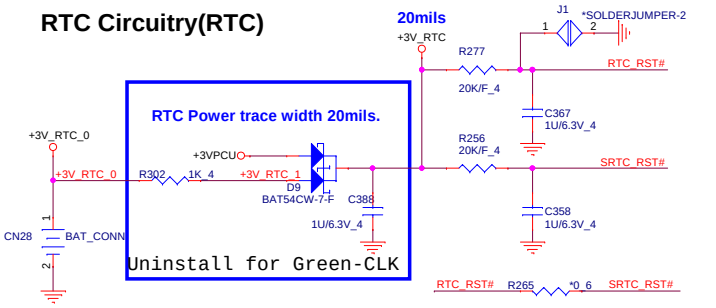
RTC Clock 32.768KHz

07

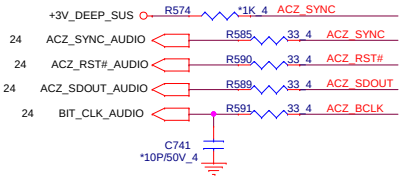


no stuff If use green Clock

RTC Circuitry(RTC)



HDA Bus(CLG)



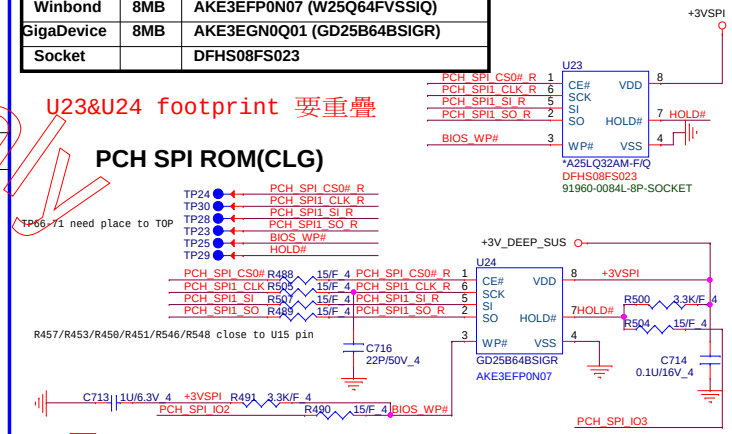
GPIO Pull UP

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

4M SPI ROM Socket

U23&U24 footprint 要重疊

PCH SPI ROM(CLG)



+3V 6,8,9,10,11,12,13,14,15,16,22,23,24,25,26,27,29,30,35,36,37
+5V 23,24,25,26,27,29,36

+1.05V 2,4,9,10,11,27,30,34,35,36,
+3VSS 6,9,10,11,27,29,30,32,34,
+3VPCU 4,25,26,27,29,30,31,32
+3V_RTC 10,27
+V1.05S_ASATA3PLL 10

N85/RD3

PROJECT : X12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 6/9(SATA/HDA)	1A
Date: Thursday, February 26, 2015	Sheet 7 of 40	

Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)

08

PCI/USBOC# Pull-up(CLG)

+3V

DGPU_PWR_EN	R520	10K_4
TS_INTB#_ULT	R523	10K_4
PIRQC#	R516	10K_4
PIRQD#	R518	10K_4
GPIO77_ULT	R514	10K_4
GPIO52_ULT	R511	10K_4
GPU_EVENT#	R510	10K_4
GC6_FB_EN	R139	10K_4
DGPU_HOLD_RST#	R493	10K_4
DGPU_HOLD_RST#	R492	100K_4

+3V_DEEP_SUS for DS3

SMBALERT#	R186	10K_4
USB_OC1#	R195	10K_4
USB_OC2#	R211	10K_4
USB_OC3#	R561	10K_4
USB_OC4#	R571	10K_4

U25N

C- Link

CL_CLK AF2
CL_DATA AD2
CL_RST# AF4

USB2.0(M/B-1) (USBP1)
USB2.0 Small board (USBP5)
USB2.0 Small board (USBP0)
Camera (USBP2)
WLAN (USBP6)
TS (USBP7)

USB3.0 M/B

28 USB30_RX1-	G20	USB3RN1
28 USB30_RX1+	H20	USB3RP1
28 USB30_TX1-	C33	USB3TN1
28 USB30_TX1+	B34	USB3TP1
	E18	USB3RN2
	F18	USB3RP2
	B33	USB3TN2
	A33	USB3TP2

USB2N0 AN8 USBP0- 25
USB2P0 AM8 USBP0+ 25
USB2N1 AR7 USBP1- 28
USB2P1 AT7 USBP1+ 28
USB2N2 AR8 USBP2- 23
USB2P2 AP8 USBP2+ 23
USB2N3 AR10
USB2P3 AT10
USB2N4 AM15
USB2P4 AL15
USB2N5 AM13 USBP5- 25
USB2P5 AN13 USBP5+ 25
USB2N6 AP11 USBP6- 29
USB2P6 AN11 USBP6+ 29
USB2N7 AR13 USBP7- 27
USB2P7 AP13 USBP7+ 27

Cardreader

GPIO77_ULT	U6	PIRQA# GPIO77
TS_INTB#_ULT	P4	PIRQB# GPIO78
PIRQC#	N4	PIRQC# GPIO79
PIRQD#	N2	PIRQD# GPIO80
GPIO52_ULT	L1	GPIO52
DGPU_PWR_EN_R	L3	GPIO54
DGPU_HOLD_RST#	R5	GPIO51
GPU_EVENT#	L4	GPIO53
GC6_FB_EN	U7	GPIO55
	AD4	PME#

15,39 DGPU_PWR_EN
14 DGPU_HOLD_RST#
17 GPU_EVENT#
15,17 GC6_FB_EN

PCI

USB

TIE TRACES TOGETHER CLOSE TO PINS WITH LENGTH TO RESISTOR

AJ10 USB_BIAS R193 22.6/F_4
AJ11 USBRBIAS

RSVD AN10
RSVD AM10

OC0# / GPIO40(SUS)	AL3 USB_OC1#
OC1# / GPIO41(SUS)	AT1 USB_OC2#
OC2# / GPIO42(SUS)	AH2 USB_OC3#
OC3# / GPIO43(SUS)	AV3 USB_OC4#

*HSW_ULT_DDR3L

U25K

Cardreader

25	USB30_RX3-	G17	PERN1 / USB3RN3		
25	USB30_RX3+	F17	PERP1 / USB3RP3		
25	USB30_TX3-	C30	PETN1 / USB3TN3		
25	USB30_TX3+	C31	PETP1 / USB3TP3		
25	PCIE_RXN2_CARD	F15	PERN2/ USB3RN4		
25	PCIE_RXP2_CARD	G15	PERP2/ USB3RP4		
25	PCIE_TXN2_CARD	C705 0.1U/16V_4 PCIE_TXN2_CARD_C	B31	PETN2/ USB3TN4	
25	PCIE_TXP2_CARD	C711 0.1U/16V_4 PCIE_TXP2_CARD_C	A31	PETP2/ USB3TP4	

WLAN

29	PCIE_RXN3_WLAN	G11	PERN3		
29	PCIE_RXP3_WLAN	F11	PERP3		
29	PCIE_TXN3_WLAN	C256 0.1U/16V_4 PCIE_TXN3_WLAN_C	C29	PETN3	
29	PCIE_TXP3_WLAN	C244 0.1U/16V_4 PCIE_TXP3_WLAN_C	B30	PETP3	

LAN

25	PCIE_RXN4_LAN	PCIE_RXN4_LAN	F13	PERN4	
25	PCIE_RXP4_LAN	PCIE_RXP4_LAN	G13	PERP4	
25	PCIE_TXN4_LAN	C698 0.1U/16V_4	PCIE_TXN4_LAN_C	B29	PETN4
25	PCIE_TXP4_LAN	C701 0.1U/16V_4	PCIE_TXP4_LAN_C	A29	PETP4

14	PEG_RXN0	F10	PERN5_L0		
14	PEG_RXP0	E10	PERP5_L0		
14	PEG_TXN0	C691 0.22U/10V_4	PEG_TXN0_C	C23	PETN5_L0
14	PEG_TXP0	C692 0.22U/10V_4	PEG_TXP0_C	C22	PETP5_L0
14	PEG_RXN1	F8	PERN5_L1		
14	PEG_RXP1	E8	PERP5_L1		
14	PEG_TXN1	C686 0.22U/10V_4	PEG_TXN1_C	B23	PETN5_L1
14	PEG_TXP1	C687 0.22U/10V_4	PEG_TXP1_C	A23	PETP5_L1
14	PEG_RXN2	H10	PERN5_L2		
14	PEG_RXP2	G10	PERP5_L2		
14	PEG_TXN2	C690 0.22U/10V_4	PEG_TXN2_C	B21	PETN5_L2
14	PEG_TXP2	C688 0.22U/10V_4	PEG_TXP2_C	C21	PETP5_L2
14	PEG_RXN3	E6	PERN5_L3		
14	PEG_RXP3	F6	PERP5_L3		
14	PEG_TXN3	C693 0.22U/10V_4	PEG_TXN3_C	B22	PETN5_L3
14	PEG_TXP3	C689 0.22U/10V_4	PEG_TXP3_C	A21	PETP5_L3

PCIE_IREF B27
R150 3.01K/F_4 PCIE_RCOMP A27
PCIE_RCOMP
RSVD E15
RSVD E13

+V1.05S_AUSB3PLL 10

PCI-E*

SMBUS

SMBALERT# / GPIO11(SUS)	AN2	SMBALERT#	
SMBCLK	AP2	SMB_PCH_CLK	
SMBDATA	AH1	SMB_PCH_DAT	
SML0ALERT# / GPIO60(SUS)	AL2	SML0ALERT#	
SML0CLK	AN1	SMB_ME0_CLK	
SML0DATA	AK1	SMB_ME0_DAT	
SML1ALERT# / PCHHOT# / GPIO73(SUS)	AU4	SML1ALERT#	TP10
SML1CLK / GPIO75(SUS)	AU3	SMB_ME1_CLK	
SML1DATA / GPIO74(SUS)	AH3	SMB_ME1_DAT	

XTAL24_IN A25 XTAL24_IN
XTAL24_OUT B25 XTAL24_OUT

CLKOUT_ITPXDP# B35 CK_XDP_N_R
CLKOUT_ITPXDP_P A35 CK_XDP_P_R
*0_4P2R_4 RP1 4 3 2 1
CK_XDP_N 11
CK_XDP_P 11
RP1 install for XDP
EC26 18P/50V_4

CLKOUT_LPC_0 AN15 CLK_PCI_EC_R R242 22_4
CLKOUT_LPC_1 AP15 CLK_PCI_LPC_R R234 22_4
CLK_24M_KBC 30
CLK_24M_DEBUG 29
EMI(near PCH)
EC29 18P/50V_4
R243 22_4
CLK_PCI_TPM 27
EMI(near PCH)
EC27 *18P/50V_4

R149
DIFFCLK_BIASREF C26 XCLK_BIASREF
+V1.05S_AXCK_LCPLL 10
3.01K/F_4

CLOCK SIGNALS

CLKOUT_PCIE0N C43
CLKOUT_PCIE0P C42

PCIE_CLKREQ0# U2
PCIECLKRQ0# / GPIO18

25 CLK_PCIE_CRN B41
25 CLK_PCIE_CRP A41
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1

PCIE_CLKREQ_CR# Y5
25 PCIE_CLKREQ_CR# PCIECLKRQ1# / GPIO19

WLAN
29 CLK_PCIE_WLANN C41
29 CLK_PCIE_WLANP B42
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2

29 PCIE_CLKREQ_WLAN# AD1
PCIECLKRQ2# / GPIO20

LAN
25 CLK_PCIE_LANN B38
25 CLK_PCIE_LANP C37
CLKOUT_PCIE_N3
CLKOUT_PCI_P3

25 PCIE_CLKREQ_LAN# N1
PCIECLKRQ3# / GPIO21

VGA
14 CLK_VGA_N A39
14 CLK_VGA_P B39
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4

14 PCIE_CLKREQ_VGA# U5
PCIECLKRQ4# / GPIO22

B37 CLKOUT_PCIE_N5
A37 CLKOUT_PCIE_P5

PCIE_CLKREQ5# T2
PCIECLKRQ5# / GPIO23

*HSW_ULT_DDR3L

RSVD K21
RSVD M21

TESTLOW_C35	C35	R148	10K_4
TESTLOW_C34	C34	R152	10K_4
TESTLOW_AK8	AK8	R239	10K_4
TESTLOW_AL8	AL8	R245	10K_4

SMBus/Pull-up(CLG)

Q38 2N7002DW

13,22,30 MBCLK2 → SMB_ME1_CLK
13,22,30 MBDATA2 → SMB_ME1_DAT

Q12 2N7002DW

+3V R185 4.7K_4 → 11,12,13,22,26 SMB_RUN_DAT → SMB_PCH_DAT
+3V R194 4.7K_4 → 11,12,13,22,26 SMB_RUN_CLK → SMB_PCH_CLK

CLK_REQ/Strap Pin(CLG)

+3V

PCIE_CLKREQ0#	R534	10K_4
PCIE_CLKREQ5#	R535	10K_4
PCIE_CLKREQ_WLAN#	R530	10K_4
PCIE_CLKREQ_LAN#	R519	10K_4
PCIE_CLKREQ_CR#	R268	10K_4
PCIE_CLKREQ_VGA#	R158	10K_4

R147 0_4 TP4
PCH_XTAL24_IN 27
C246 12P/50V_4
XTAL24_IN
XTAL24_OUT
R153 1M_4
24MHZ +-30PPM Y1
C245 12P/50V_4
TP5

6,7,9,10,11,12,13,14,15,16,22,23,24,25,26,27,29,30,35,36,37 +3V
6,7,9,10,11 +3V_DEEP_SUS

SMBus/Pull-up(CLG)

for DS3 +3V_DEEP_SUS

R570	2.2K_4	SMB_PCH_CLK
R566	2.2K_4	SMB_PCH_DAT
R569	2.2K_4	SMB_ME0_CLK
R568	2.2K_4	SMB_ME0_DAT
R572	2.2K_4	SMB_ME1_CLK
R560	2.2K_4	SMB_ME1_DAT
R238	10K_4	SML1ALERT#
R192	1K_4	SML0ALERT#

NB5/RD3

PROJECT : X12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 7/9 (PCIE/USB/CLK)	1A
Date: Thursday, February 26, 2015	Sheet 8 of 40	

Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA) Haswell (GPIO)

09

U25O

GPIO8(SUS) AU2 ← SIO_EXT_SCI# ← 30 SIO_EXT_SCI#
GPIO9(SUS) AM3 ← BT_OFF ← 29 BT_OFF
GPIO10(SUS) AM2 ← RF_OFF_PCH_R ← R177 *0_4 ← 6,29 RF_OFF_PCH
LAN_PHY_PWR_CTRL / GPIO12(DSW) AM7 ← LAN_DISABLE#
GPIO13(SUS) AT3 ← GPIO13_ULT
GPIO14(SUS) AH4 ← GPIO14_ULT
GPIO15(SUS) AD6
GPIO16 Y1 ← ODD_PRSNT#_R ← R553 *0_4 ← ZERO_ODD_DP# 29
GPIO17 T3 ← DGPU_PWROK 16,30,38
GPIO24 (SUS) AD5 ← BOARD_ID6
GPIO25(DSW) AM4 ← GPIO25_ULT
GPIO26(SUS) AN3 ← BOARD_ID7
GPIO27(DSW) AN5 ← GPIO27
GPIO28(SUS) AD7 ← BOARD_ID8
DEVSLP0/ GPIO33 P2 ← DEVSLP0
DEVSLP1/ GPIO38 L2 ← DEVSLP1 ← TP11
DEVSLP2/ GPIO39 N5 ← DEVSLP2
GPIO44(SUS) AK4 ← GPIO44_ULT
GPIO45(SUS) AG5 ← BOARD_ID4 ← TP for DG
GPIO46(SUS) AG3 ← GPIO46_ULT
GPIO47(SUS) AB6 ← BOARD_ID5 ← TP12
GPIO48 U4 ← BT_COMBO_EN#
GPIO49 Y3 ← GPIO49_ULT ← ACCEL_INTA# 27
GPIO50 P3 ← GPIO50_ULT
GPIO56(SUS) AG6 ← BOARD_ID0
GPIO57(SUS) AP1 ← BOARD_ID1
GPIO58(SUS) AL4 ← BOARD_ID2
GPIO59(SUS) AT5 ← BOARD_ID3
SDIO_POWER_EN/ GPIO70 C4 ← GPIO70_ULT
HSIOPC/ GPIO71 Y2 ← MPHY_PWREN ← 36 MPHY_PWREN
BMBUSY# / GPIO76 P1 ← GPIO76_ULT
SPKR/ GPIO81 V2 ← ACZ_SPKR 24

GPIO

THRMTRIP# D60 → PCH_THRMTRIP# → PM_THRMTRIP# 30
RCIN# / GPIO82 V4 → EC_RCIN# → EC_RCIN# 30
SERIRQ T4 → SERIRQ → R529 10K_4 → +3V; SERIRQ → SERIRQ 27,30
PCH_OPI_RCOMP AW15 → PCH_OPI_RCOMP → R583 49.9/F_4
RSVD AF20
RSVD AB21

CPU/MISC

GSPI0_CS/ GPIO83 R6 → GSPI0_CS
GSPI0_CLK/ GPIO84 L6 → GSPI0_CLK
GSPI0_MISO/ GPIO85 N6 → GSPI0_MISO
GSPI0_MOSI/ GPIO86 L8
GSPI1_CS/ GPIO87 R7 → GSPI1_CS
GSPI1_CLK/ GPIO88 L5 → GSPI1_CLK
GSPI1_MISO/ GPIO89 N7 → GSPI1_MISO
GSPI1_MOSI/ GPIO90 K2 → GSPI1_MOSI
UART0_RXD/ GPIO91 J1 → UART0_RXD
UART0_TXD/ GPIO92 K3 → UART0_TXD
UART0_RTS/ GPIO93 J2 → UART0_RTS
UART0_CTS/ GPIO94 G1 → UART0_CTS
UART1_RXD/ GPIO0 K4 → UART1_RXD
UART1_TXD/ GPIO1 G2 → UART1_TXD
UART1_RST/ GPIO2 J3 → UART1_RST
UART1_CTS/ GPIO3 J4 → UART1_CTS
I2C0_SDA/ GPIO4 F2 → I2C0_SDA
I2C0_SCL/ GPIO5 F3 → I2C0_SCL
I2C1_SDA/ GPIO6 G4 → I2C1_SDA
I2C1_SCL/ GPIO7 F1 → I2C1_SCL
SDIO_CLK/ GPIO64 E3 → SDIO_CLK
SDIO_CMD/ GPIO65 F4 → SDIO_CMD
SDIO_D0/ GPIO66 D3
SDIO_D1/ GPIO67 E4 → SDIO_D1
SDIO_D2/ GPIO68 C3 → SDIO_D2
SDIO_D3/ GPIO69 E2 → SDIO_D3

SERIAL IO

*HSW_ULT_DDR3L TCI

RP6: SDIO_D2, SDIO_D1, SDIO_D3, SDIO_CLK → UART0_CTS, I2C0_SCL, I2C0_SDA, I2C1_SCL; 10K_10P8R_6 → +3V
RP2: UART1_RXD, GSPI0_CLK, I2C1_SDA, SDIO_CMD → GSPI1_MISO, GSPI0_MISO, GSPI1_CLK; 10K_10P8R_6 → +3V
RP5: GSPI1_MOSI, UART1_CTS, GSPI0_CS, GSPI1_CS → UART0_RXD, UART0_RTS, UART1_TXD, UART1_RST; 10K_10P8R_6 → +3V

GPIO Pull-up/Pull-down(CLG)

+3V_DEEP_SUS
SIO_EXT_SCI# R282 10K_4
BT_OFF R180 10K_4
RF_OFF_PCH_R R172 10K_4
GPIO13_ULT R218 10K_4
GPIO14_ULT R183 10K_4
GPIO44_ULT R565 10K_4
GPIO46_ULT R541 10K_4
+3V
GPIO49_ULT R552 10K_4
GPIO50_ULT R524 10K_4
ODD_PRSNT#_R R546 10K_4
DGPU_PWROK R513 10K_4
DEVSLP0 R515 10K_4
DEVSLP2 R499 10K_4
BT_COMBO_EN# R512 *10K_4
GPIO70_ULT R486 10K_4
EC_RCIN# R269 10K_4
GPIO76_ULT R525 10K_4
MPHY_PWREN R544 100K_4
MPHY_PWREN R545 *10K_4
+3VS5
GPIO25_ULT R173 10K_4
LAN_DISABLE# R169 10K_4
GPIO27 R626 10K_4

GPIO12 LAN_DISABLE# SUS -->Check list +3V -->Datasheet

Close to EC

+V1.05S_VCCST
PM_THRMTRIP# R184 1K_4

Model	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Definition	Reserve (Default = 00)	Reserve (Default = 00)	00 Single Rank (X12) 01 Dual Rank (X12) 10 Meso-AMD (X11) 11 Reserve	00 14" 01 15" 10 17"	0 : UMA 1 : DIS

R174 *10K_4 BOARD_ID0 R539 10K_4 → +3V_DEEP_SUS
R205 *10K_4 BOARD_ID1 R199 10K_4
R558 10K_4 BOARD_ID2 R559 *10K_4
R248 *10K_4 BOARD_ID3 R255 10K_4
R175 10K_4 BOARD_ID4 R540 *10K_4
R167 10K_4 BOARD_ID5 R549 *10K_4
R161 10K_4 BOARD_ID6 R164 *10K_4
R204 10K_4 BOARD_ID7 R198 *10K_4
R160 10K_4 BOARD_ID8 R163 *10K_4

6,7,8,10,11,12,13,14,15,16,22,23,24,25,26,27,29,30,35,36,37 → +3V
6,10,11,27,29,30,32,34,36,39 → +3VS5

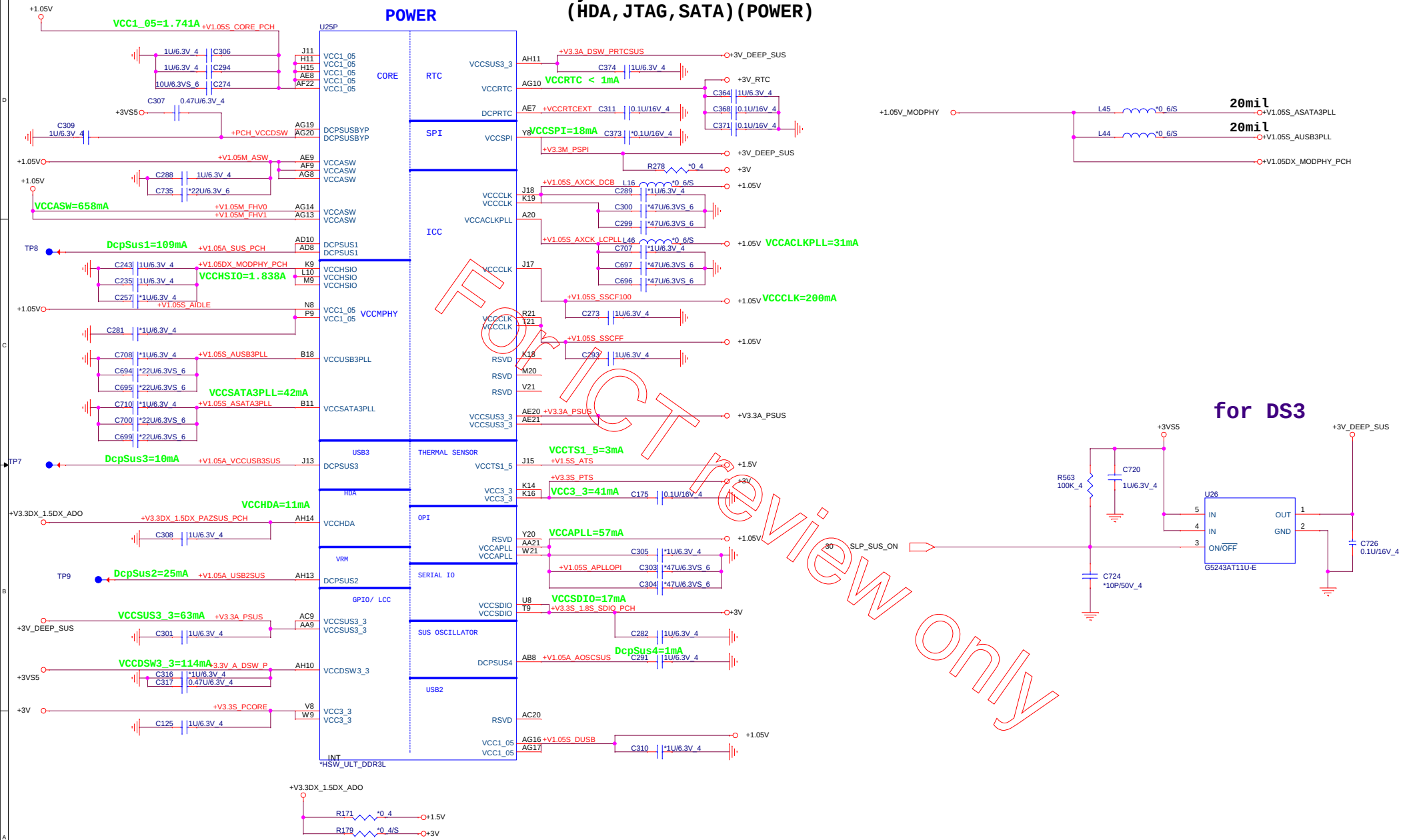
PROJECT : X12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 8/9 (GPIO/MISC)	1A
Date: Thursday, February 26, 2015	Sheet 9 of 40	

N85/RD3

Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)(POWER)

POWER



for DS3

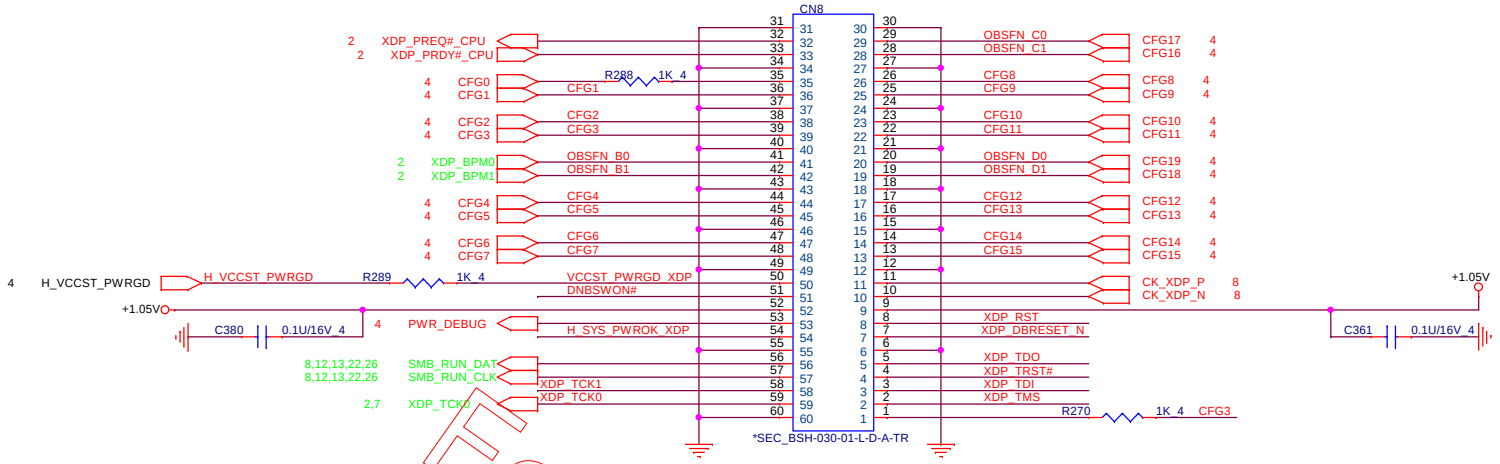
6,7,8,9,11,12,13,14,15,16,22,23,24,25,26,27,29,30,35,36,37	+3V	8	+V1.05S_AUSB3PLL
23,24,25,26,27,29,36	+5V	7	+V1.05S_ASATA3PLL
		8	+V1.05S_AXCK_LCPLL
2,4,7,9,11,27,30,34,35,36,39	+1.05V	7,27	+3V_RTC
6,9,11,27,29,30,32,34,36,39	+3VS5	2,4,12,13,33	+1.35VSUS
13,25,27,28,32,33,34,35,36,37,38,39	+5VS5		

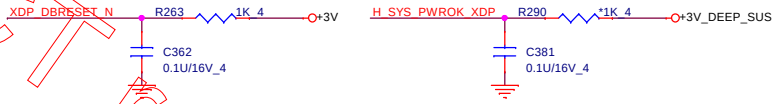
N85/RD3

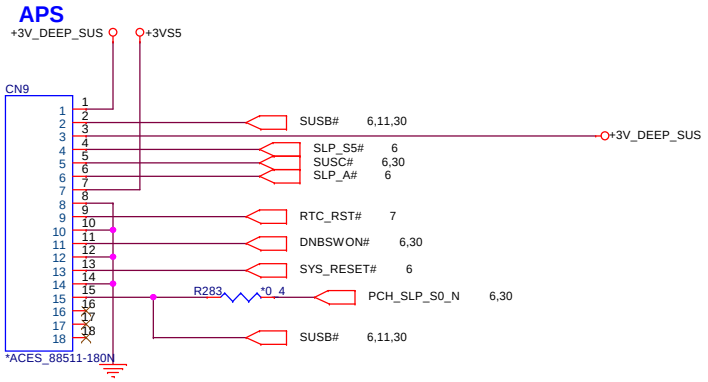
PROJECT : X12
Quanta Computer Inc.

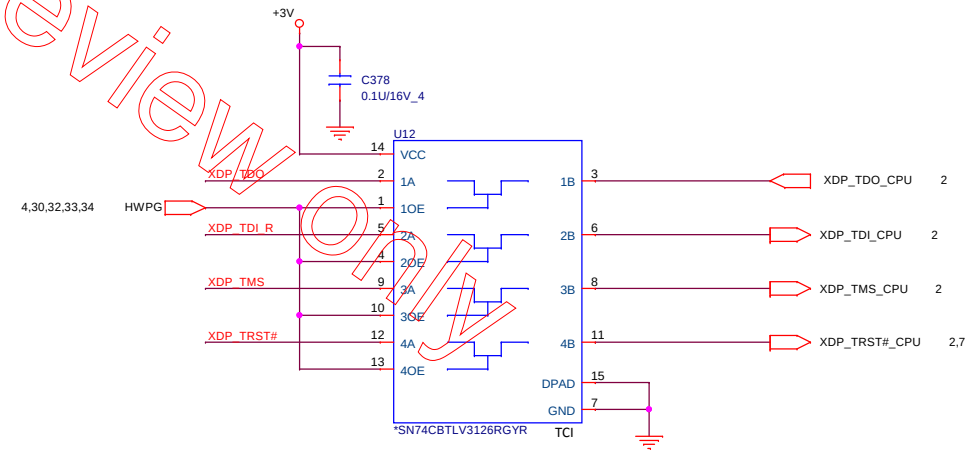
Size	Document Number	Rev
Custom	ULT 9/9(POWER-2)	1A

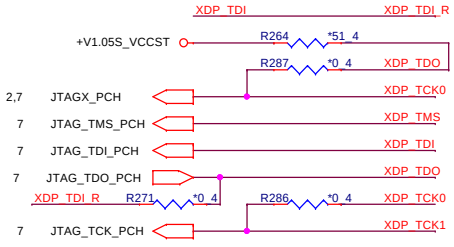
Date: Thursday, February 26, 2015 Sheet 10 of 40

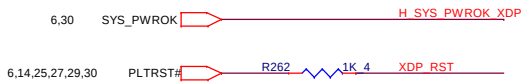












NB5/RD3

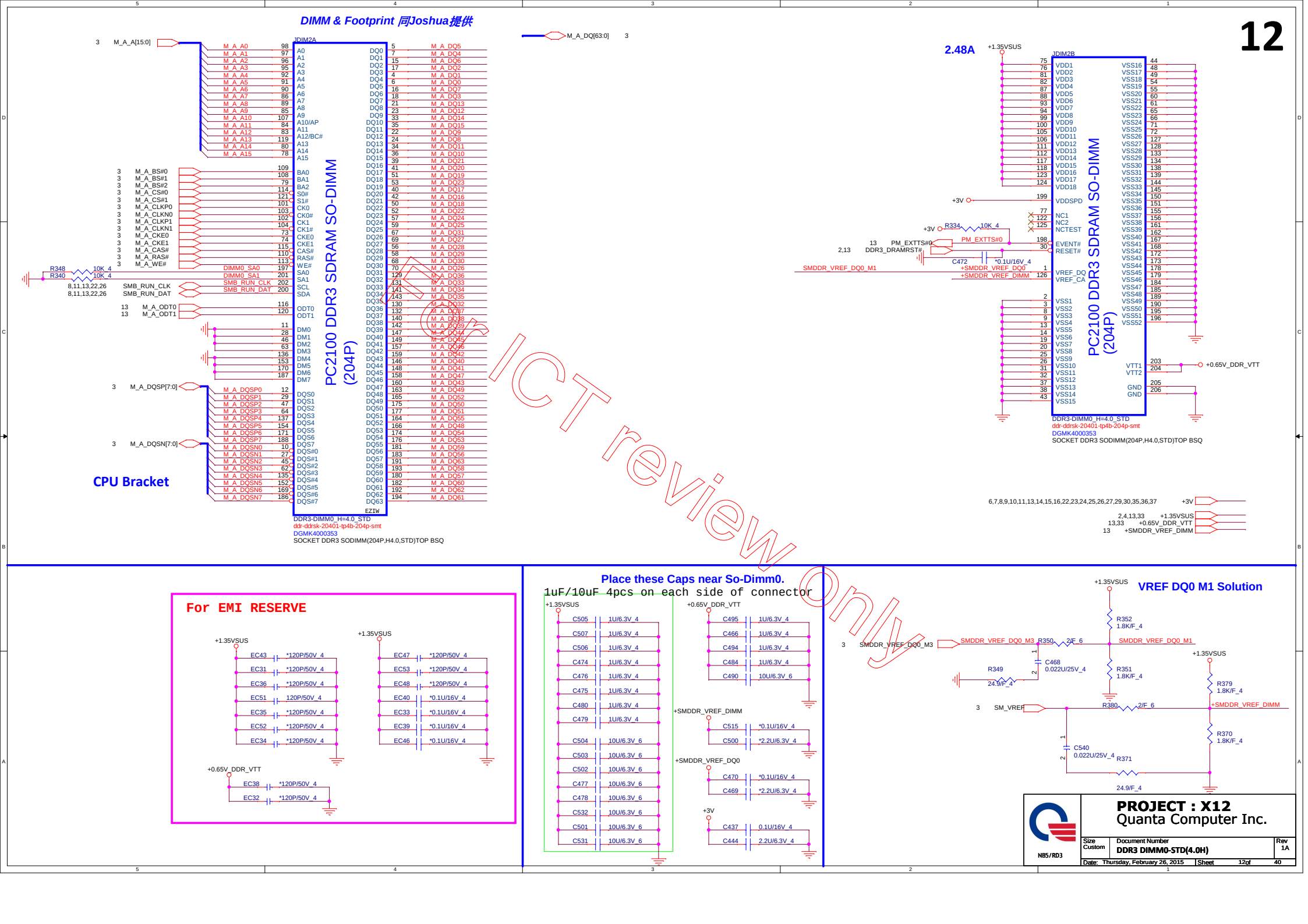
PROJECT : X12
Quanta Computer Inc.
ULT

Size	Document Number	Rev
	HSW XDP & APS	1A

Date: Thursday, February 26, 2015 | Sheet 11 of 40

DIMM & Footprint 同Joshua提供

CPU Bracket



2.48A

For EMI RESERVE

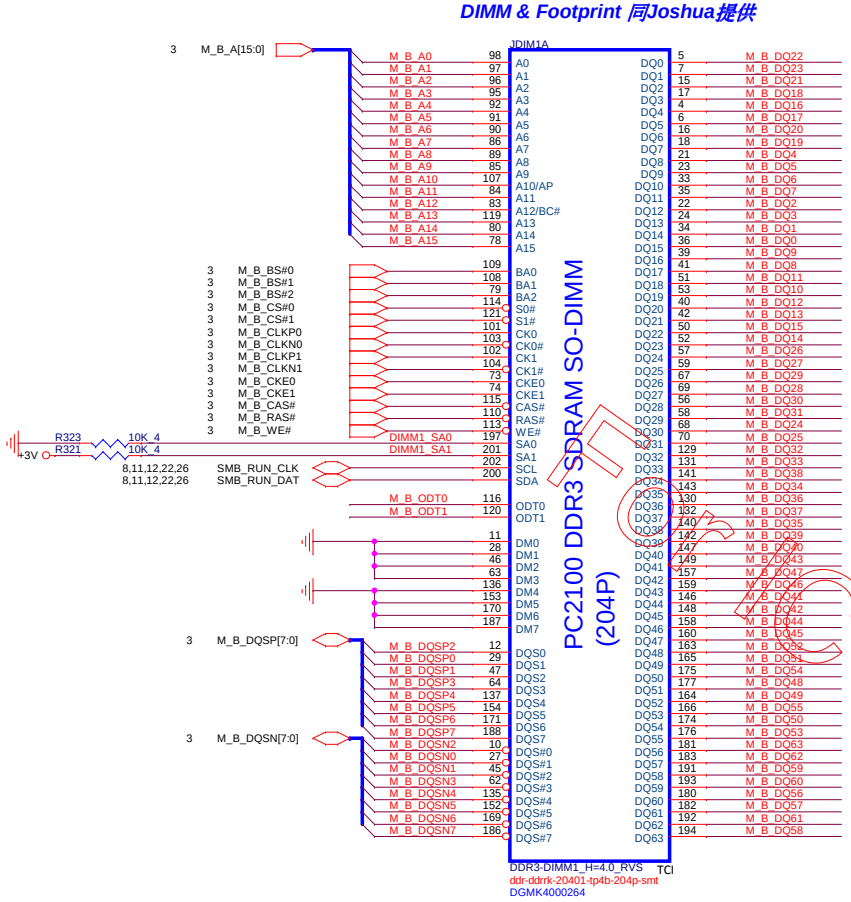
Place these Caps near So-Dimm0.

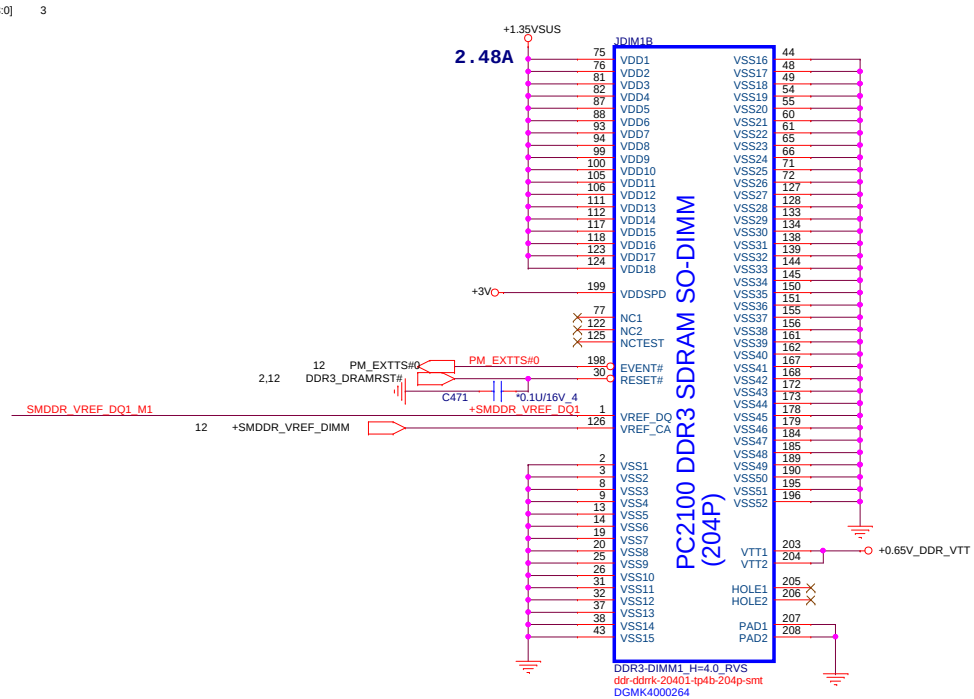
1uF/10uF 4pcs on each side of connector

VREF DQ0 M1 Solution

N85/RD3	PROJECT : X12 Quanta Computer Inc.		
Size Custom	Document Number DDR3 DIMM0-STD(4.0H)		Rev 1A
Date: Thursday, February 26, 2015	Sheet 12of 40		

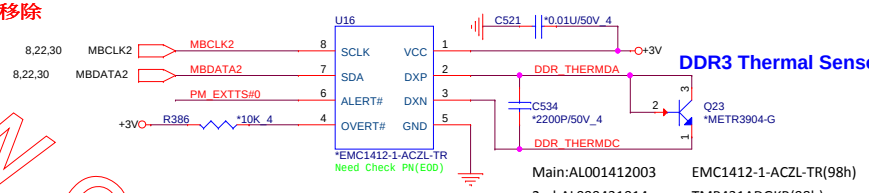
DIMM & Footprint 同Joshua提供





Local Thermal Sensor

MV可移除

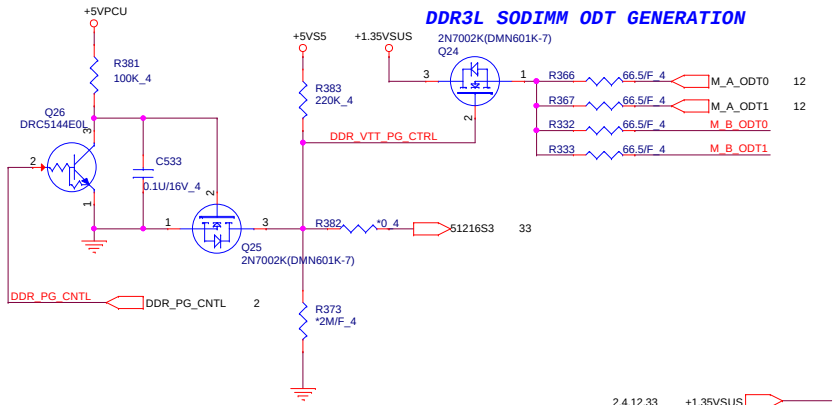


DDR3 Thermal Sensor

Main:AL001412003 EMC1412-1-ACZL-TR(98h)

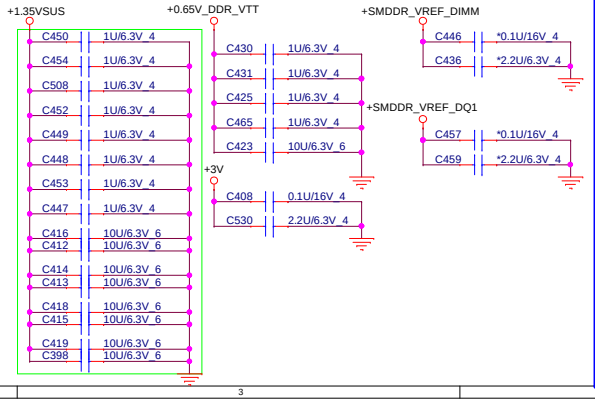
2nd:AL000431014 TMP431ADGKR(98h)

DDR3L SODIMM ODT GENERATION

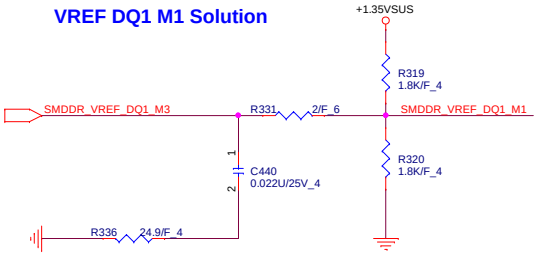


Place these Caps near So-Dimm1.

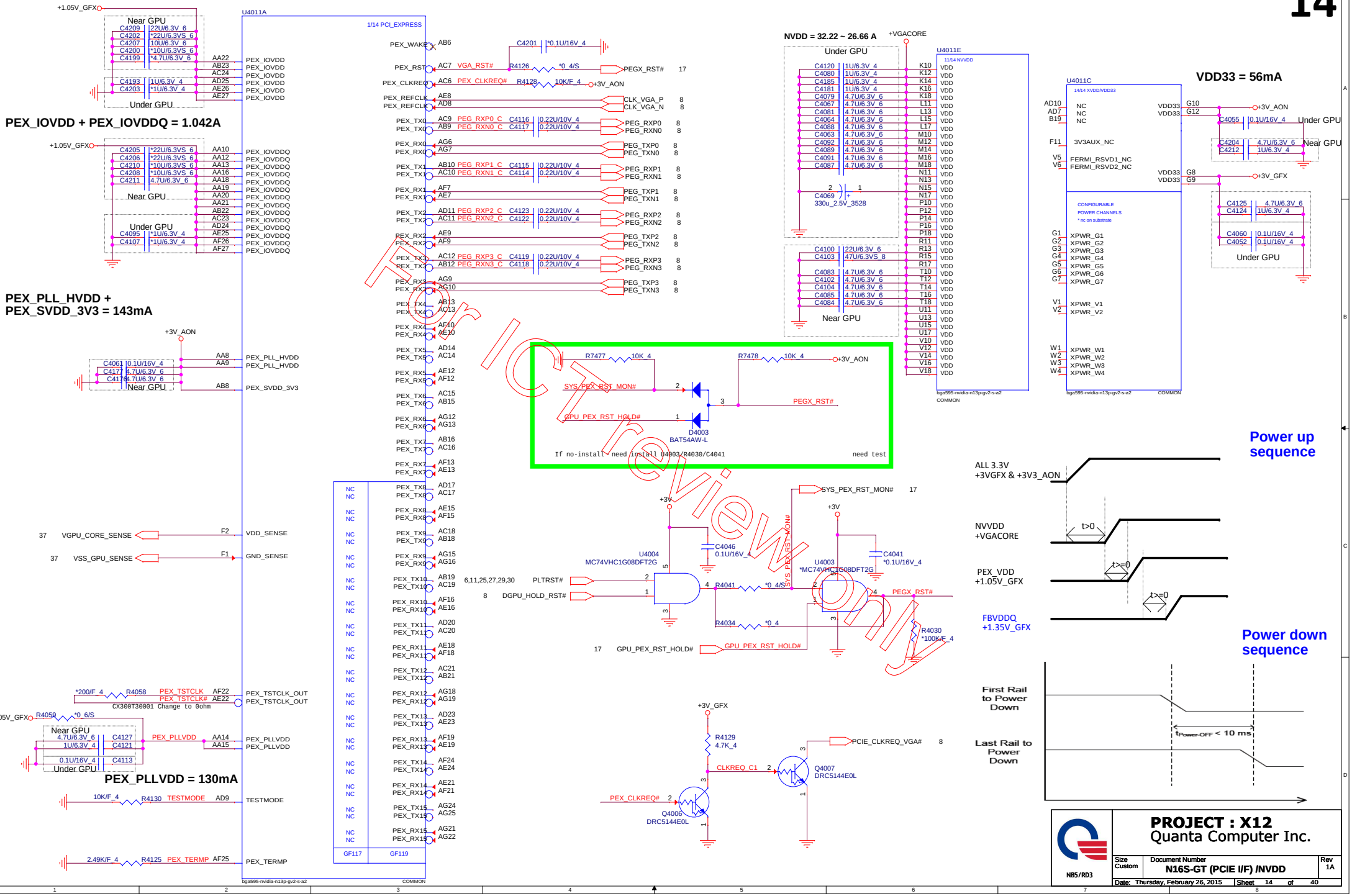
1uF/10uF 4pcs on each side of connector

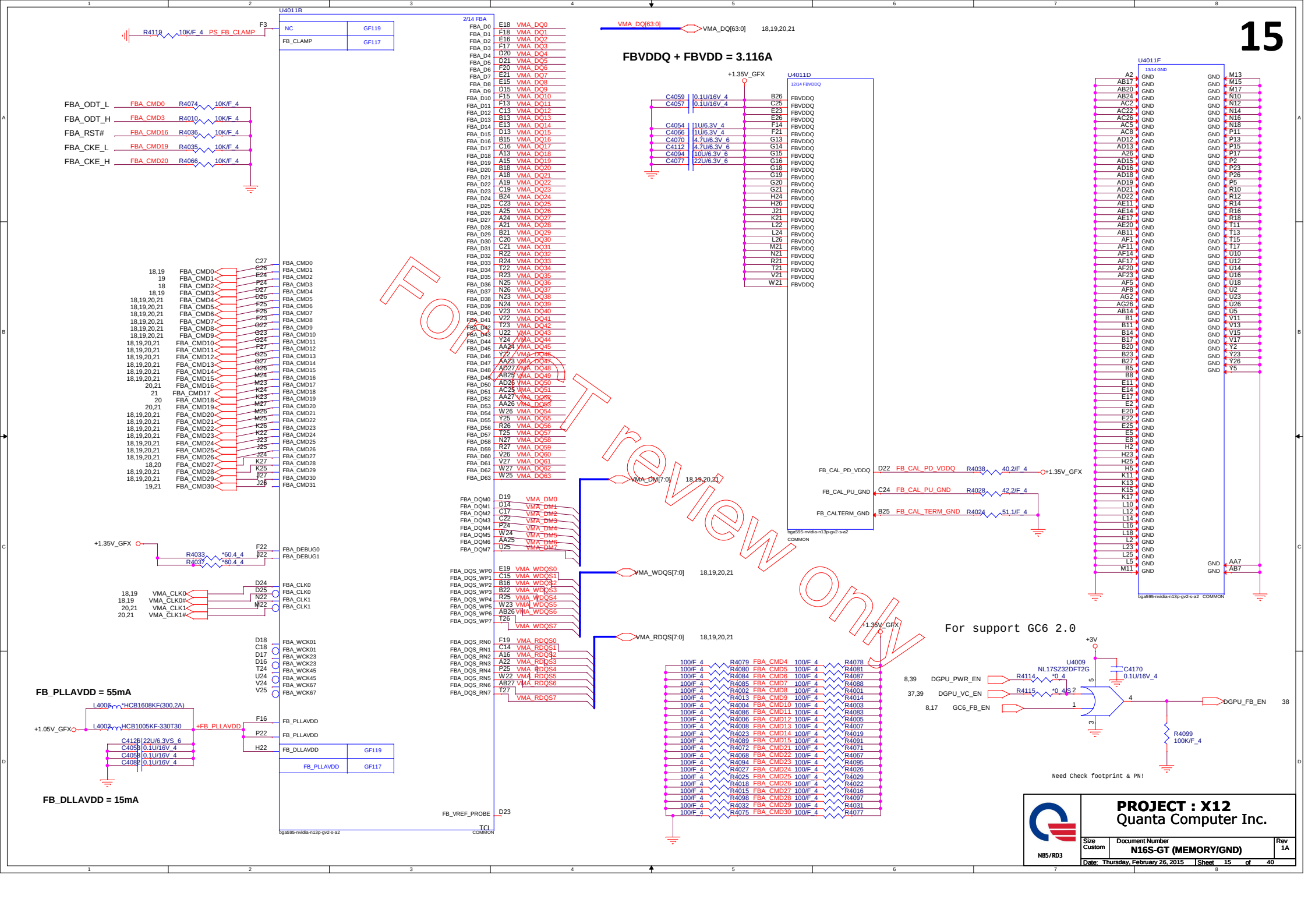


VREF DQ1 M1 Solution



N85/RD3	PROJECT : X12 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 DIMM1-RVS(4.0H)	Rev: 1A
Date: Thursday, February 26, 2015	Sheet: 13of	40




U4011B
2/14 FBA
U4011D
12/14 FBVDDQ
U4011F
13/14 GND
FBVDDQ + FBVDD = 3.116A
FB_PLLAVDD = 55mA
FB_DLLAVDD = 15mA
For support GC6 2.0
Need Check footprint & PN!
For Review Only
PROJECT : X12
Quanta Computer Inc.
N16S-GT (MEMORY/GND)
Rev 1A
Thursday, February 26, 2015
Sheet 15 of 40
N85/RD3

U4011G
4/14 IFPAB
IFPAB
bga595-nvidia-n13p-gv2-s-a2 COMMON

U4011J
7/14 IFPEF
IFPE
IFPF
bga595-nvidia-n13p-gv2-s-a2 COMMON

U4011K
3/14 DACA
bga595-nvidia-n13p-gv2-s-a2 COMMON

U4011H
5/14 IFPC
IFPC
bga595-nvidia-n13p-gv2-s-a2 COMMON

U4011I
6/14 IFPD
IFPD
bga595-nvidia-n13p-gv2-s-a2 COMMON

PLLVDD = 38mA

L4004 *HCB1608KF-301T20(300,2A) reserve 0603
+1.05V_GFX L4001 HCB1005KF-330T30 NV_PLLVDD
C4062 0.1U/16V_4
C4065 22U/6.3VS_6

L4005 HCB1005KF-330T30
+1.05V_GFX L4002 *HCB1608KF(300,2A) SP_PLLVDD
C4068 0.1U/16V_4
C4071 0.1U/16V_4
C4075 10U/6.3V_6
C4076 47U/6.3VS_8

SP_PLLVDD = 17mA

VID_PLLVDD = 41mA

U4011M
9/14 XTAL_PLL
PLLVDD
SP_PLLVDD
VID_PLLVDD
XTALSSIN
XTALIN
XTALOUTBUFF
XTALOUT
bga595-nvidia-n13p-gv2-s-a2 COMMON

R4090 10K/F_4 XTAL_SSIN A10
CLK_27M_XTAL_IN R4069 *0_4 27M_XTAL_IN_R C11
XTALOUTBUFF C10 27M_XTAL_OUT R4096 10K/F_4
XTALOUT B10 27M_XTAL_OUT

C4160 10P/50V_4
27M_XTAL_IN_R
27M_XTAL_OUT
Y4001 27MHZ +-10PPM
C4153 10P/50V_4

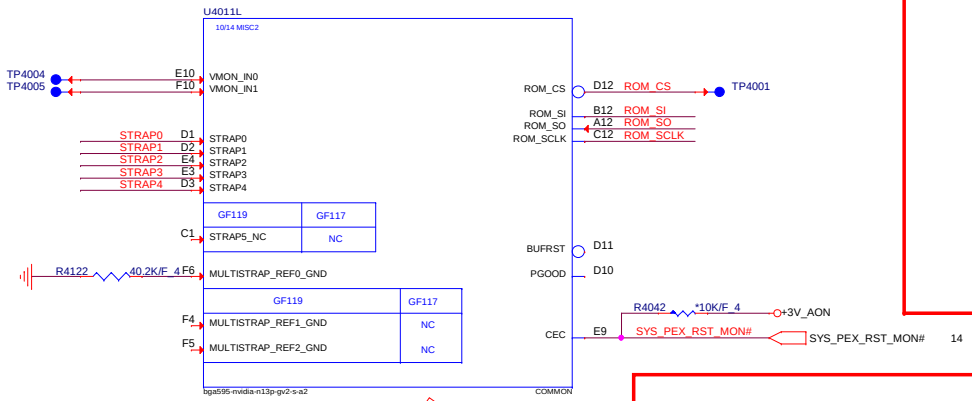
+3V_GFX
DGPU_PGOK-1
+1.05V_GFX R4050 4.7K_4 DGPU_POK4
C4078 *1000P/50V_4
Q4004 METR3904-G
+1.35V_GFX R4049 *4.7K_4 DGPU_POK2
C4086 *1000P/50V_4
Q4003 *METR3904-G
R4131 *0_4/S
+3V
R4051 4.7K_4
C4096 1000P/50V_4
R4053 *4.7K_4
Q4005 DRC5144E0L
R4052 100K/F_4
DGPU_PWROK 9,30,38

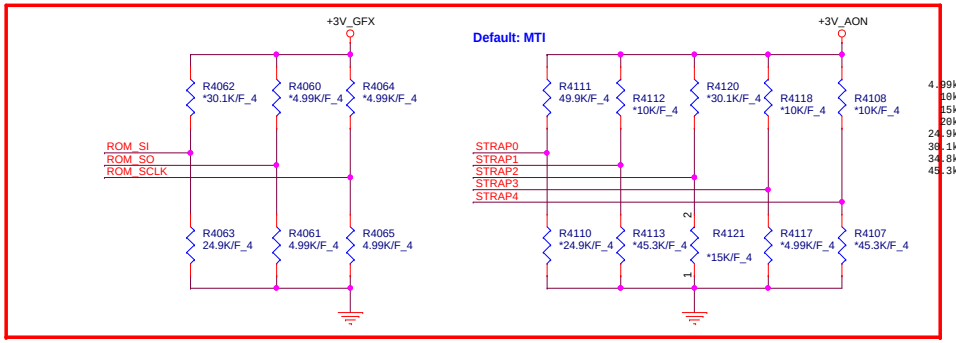
N85/RD3

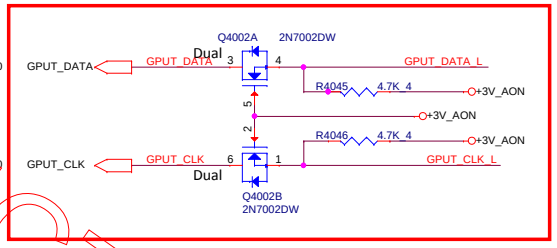
PROJECT : X12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N16S-GT (DISPLAY)	1A

Date: Thursday, February 26, 2015 Sheet 16 of 40



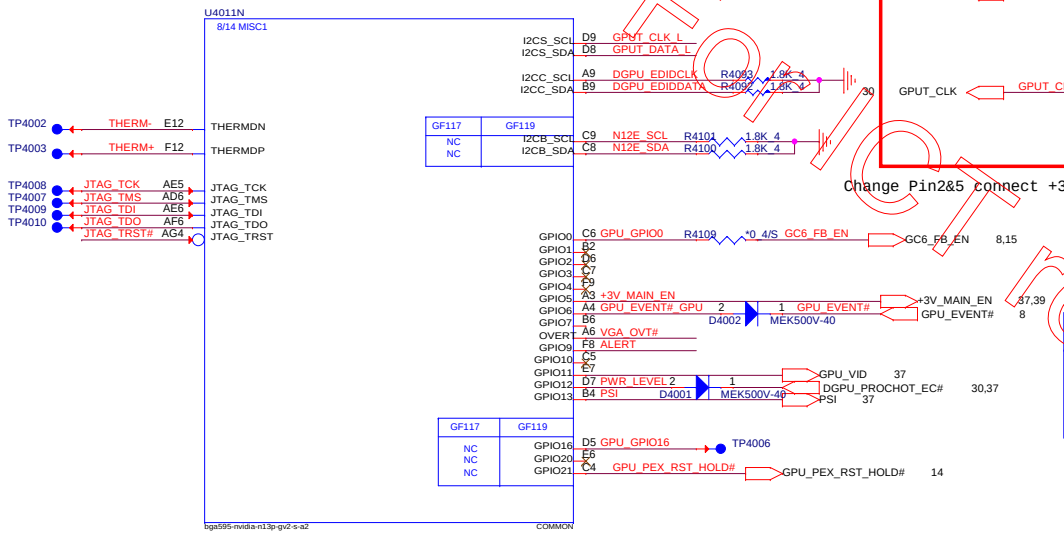


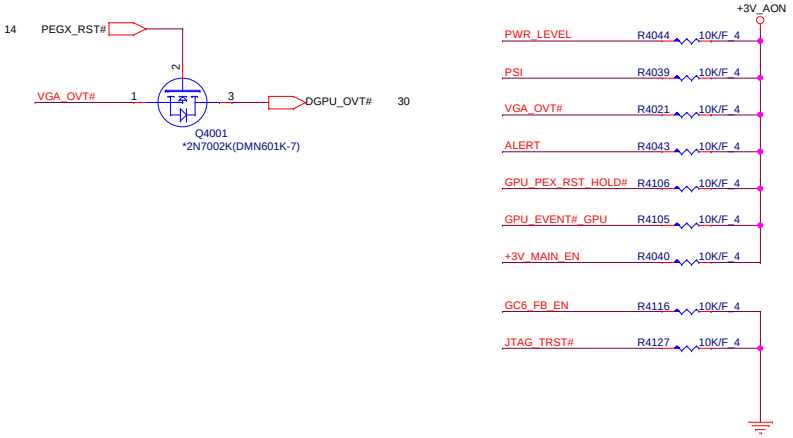


Change Pin2&5 connect +3V_AON for GPU power sequence 11/11 SI

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111





VRAM Configuration Table

ROM_SI E

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	256Mx16 Strap	128Mx16 Strap	QBC	TOP B/S
1110	DDR3L 256Mx16, 64bit, 4Gb,900MHz	H,P HYNIX	H5TC4G63CFR-N0C	0XE	TBD	AKD5PZDTW02	AKD5PZDTW01
0011	DDR3L 256Mx16, 64bit, 4Gb,900MHz	Micron	MT41J256M16HA-093G:E	0x4	TBD	AKD5PZSTL01	AKD5PZSTL00
1111	DDR3L 256Mx16, 64bit, 4Gb,900MHz	SAMSUNG	K4W4G1646E-BC1A	0XF	TBD	AKD5PGDT501	AKD5PGDT500

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

Rank0

HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

U4008 — VRAM _DDR3_MTI_256MX16 (96-BALL SDRAM DDR3)

U4007 — VRAM _DDR3_MTI_256MX16 (96-BALL SDRAM DDR3)

PROJECT	X12
Quanta Computer Inc.	
Size	Custom
Document Number	DDR3L - RANK0
Rev	1A
Date	Thursday, February 26, 2015
Sheet	18 of 40
NB5/RD3	

Rank1

HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

U4002

VRAM _DDR3_MTI_256MX16

U4001

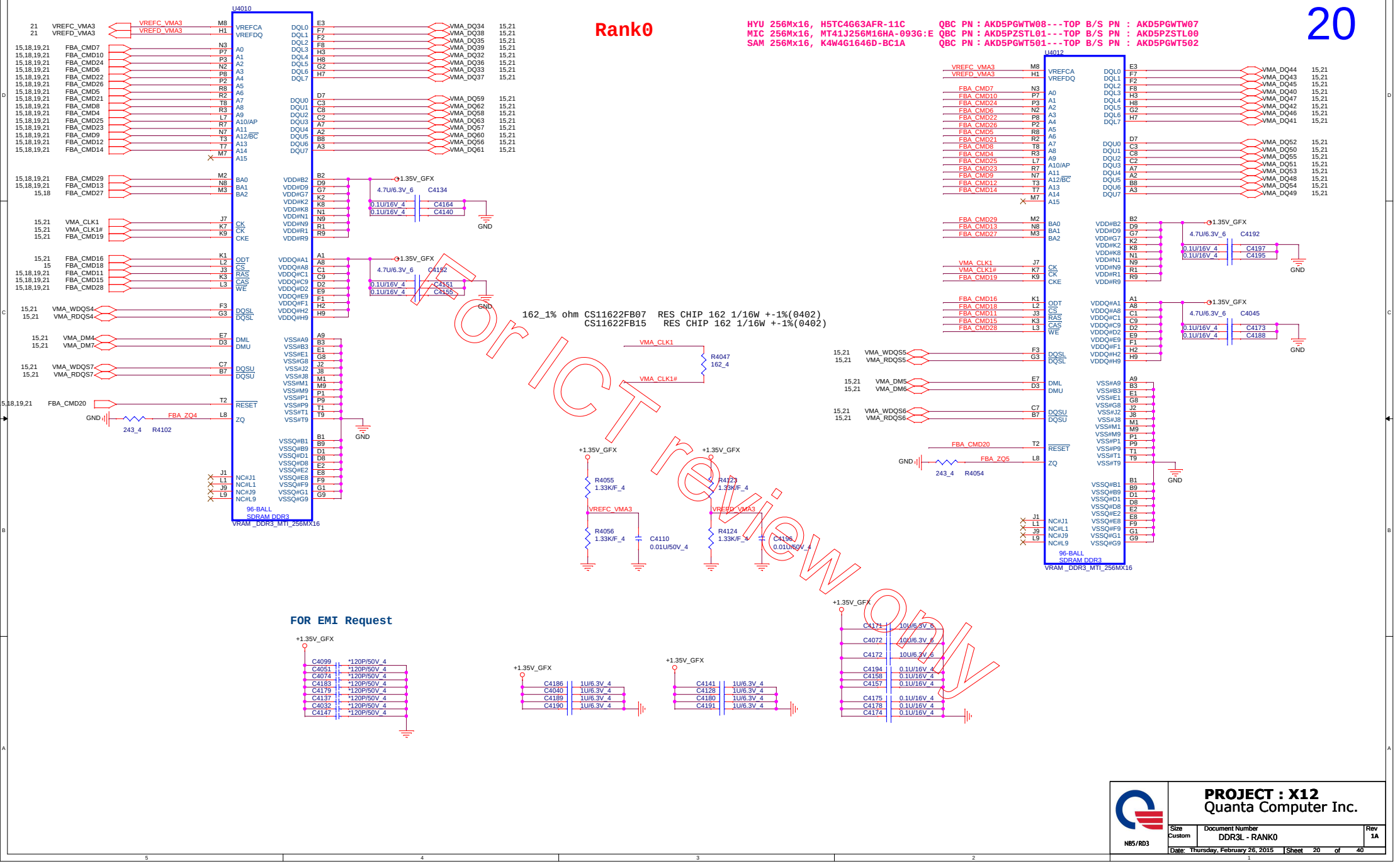
VRAM _DDR3_MTI_256MX16

PROJECT : X12	Quanta Computer Inc.
Size: Custom	Document Number: DDR3L - RANK1
Rev: 1A	
Date: Thursday, February 26, 2015	Sheet 19 of 40

NB5/RD3

Rank0

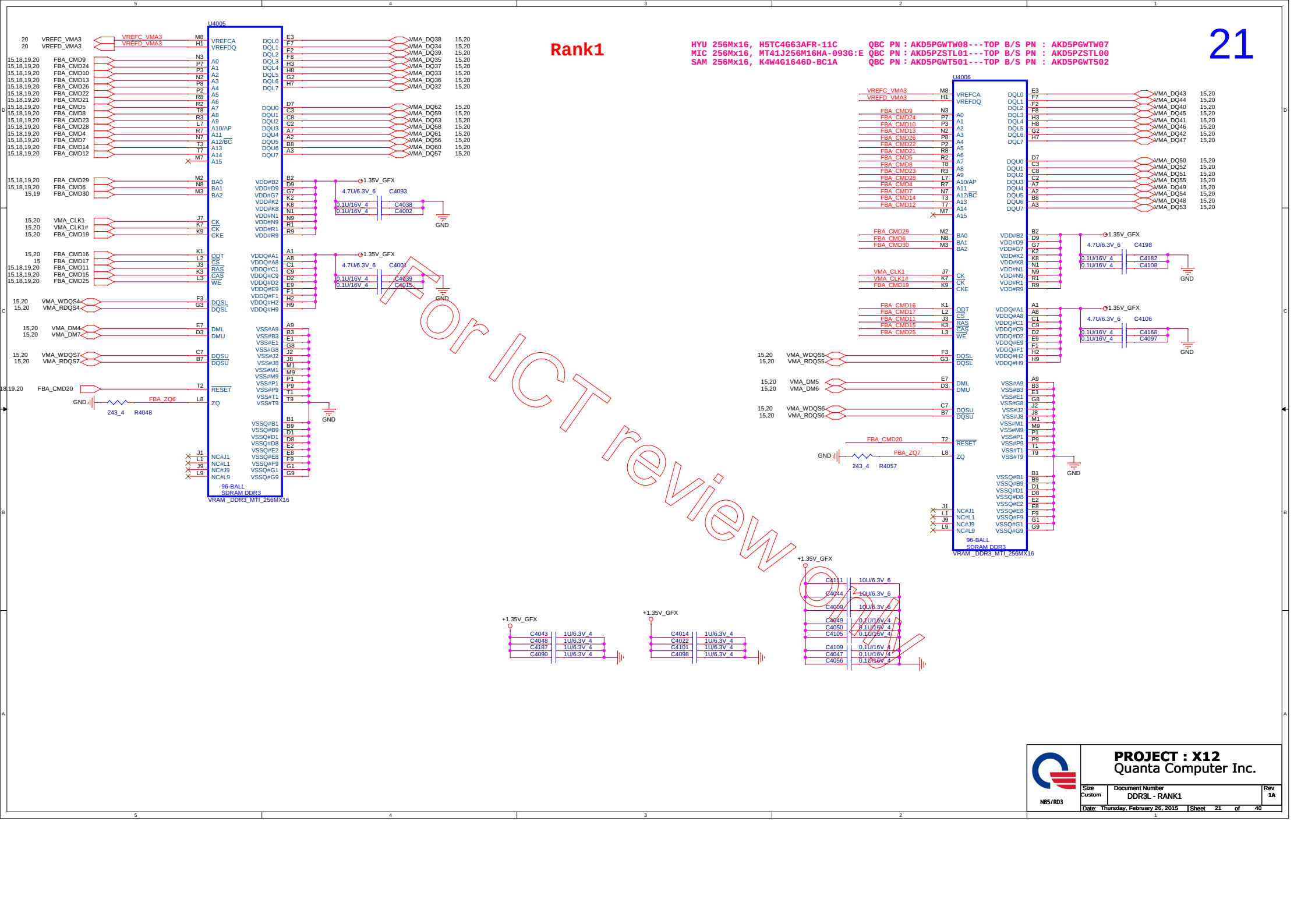
HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502



PROJECT : X12 Quanta Computer Inc.		
Size: Custom	Document Number: DDR3L - RANK0	Rev: 1A
Date: Thursday, February 26, 2015	Sheet 20 of 40	
NB5/RD3		

Rank1

HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502



PROJECT : X12
Quanta Computer Inc.

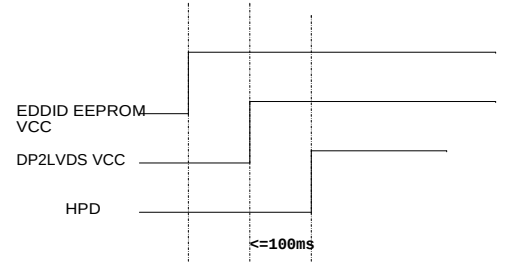
Size	Document Number	Rev
Custom	DDR3L - RANK1	1A

Date: Thursday, February 26, 2015 Sheet 21 of 40

NB5/RD3

RTD2136 Dual Channel only

RTD2136S Power Up Sequence 22



Reserve for co layout EDP CON, EDP only please stuff

Pin 18: keep 80mil Trace

RTD2136R

IC底部需接GND

Reserve

Default(LVDS Only)

For eDP, close to U3

LVDS Only

Use 1% Res on R32

L10: need use CV-4709MN00 for Vendor suggestion

keep 80 mil

USING 60R 2A

CLOSE TO Pin22

Close to Pin18

USING 60R 1A

Close to Pin5

Close to Pin17

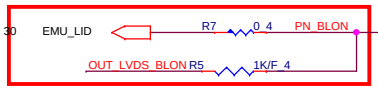
Close to Pin11

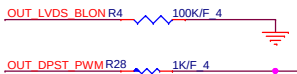
Close to Pin43

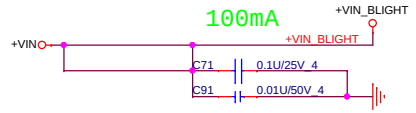
SWR MODE	LDO MODE
Stuff L10	Stuff R59

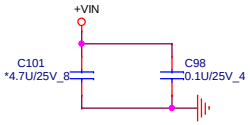
PROJECT : X12	Quanta Computer Inc.
N85/RD3	Size: Custom; Document Number: RTD2136; Rev: ?
Date: Thursday, February 26, 2015	Sheet 22 of 40

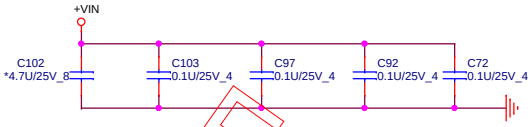
LID Switch

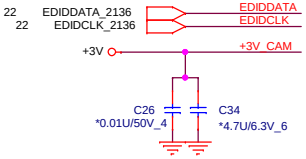


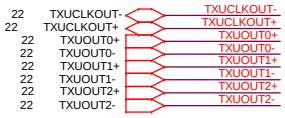


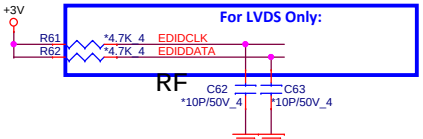








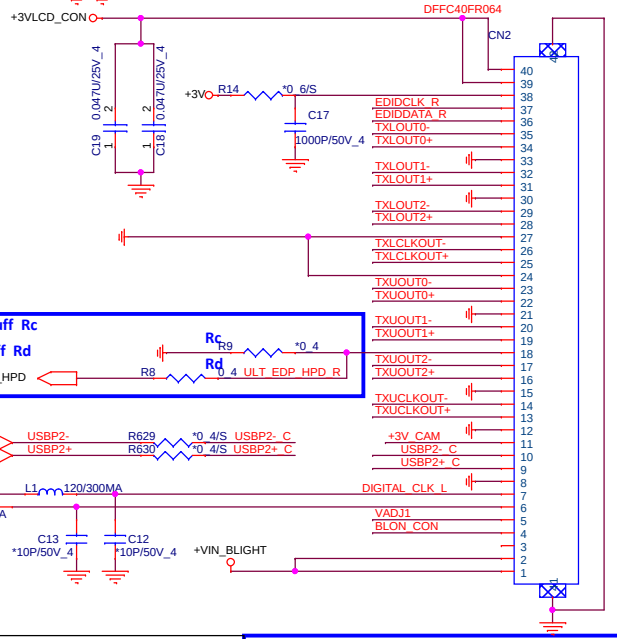


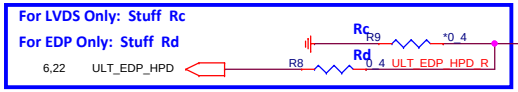


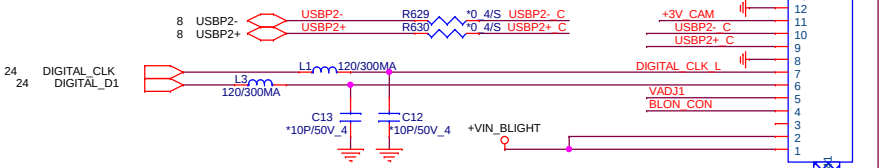
LVDS Conn.

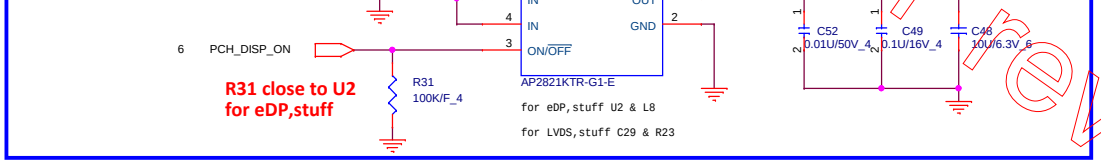
23

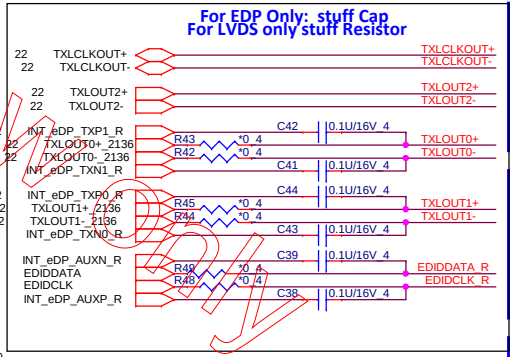
GS12401-1011-9H
lvds-50671-04041-001-40p-l

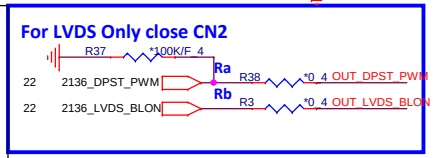


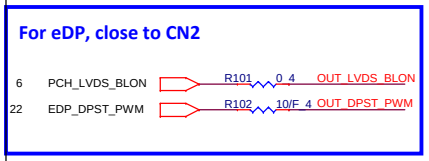


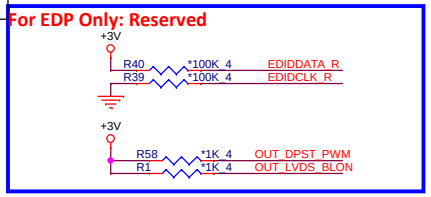


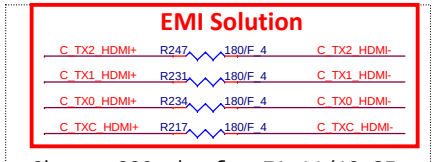


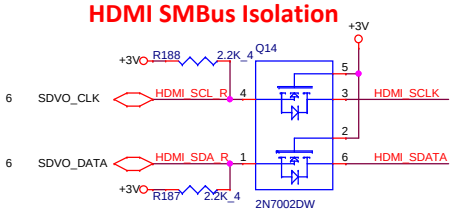


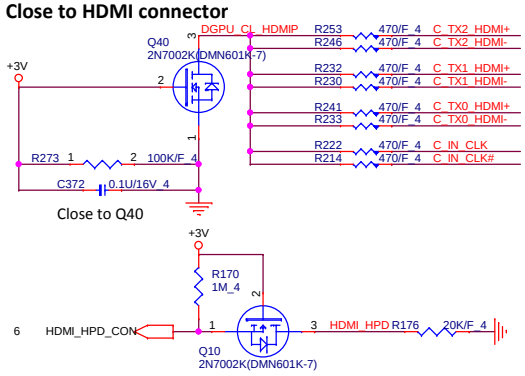


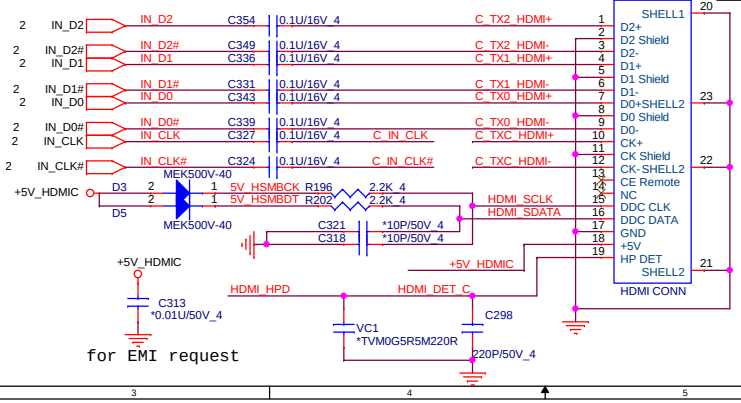


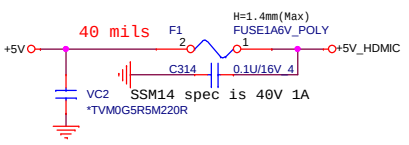












13,25,27,28,32,33,34,35,36,37,38,39 +5VS5
6,7,8,9,10,11,12,13,14,15,16,22,24,25,26,27,29,30,35,36,37 +3V
4,7,25,26,27,29,30,31,32 +3VPCU
24,25,26,27,29,36 +5V
26,28,29,31,32,33,34,35,36,37,38,39 +VIN

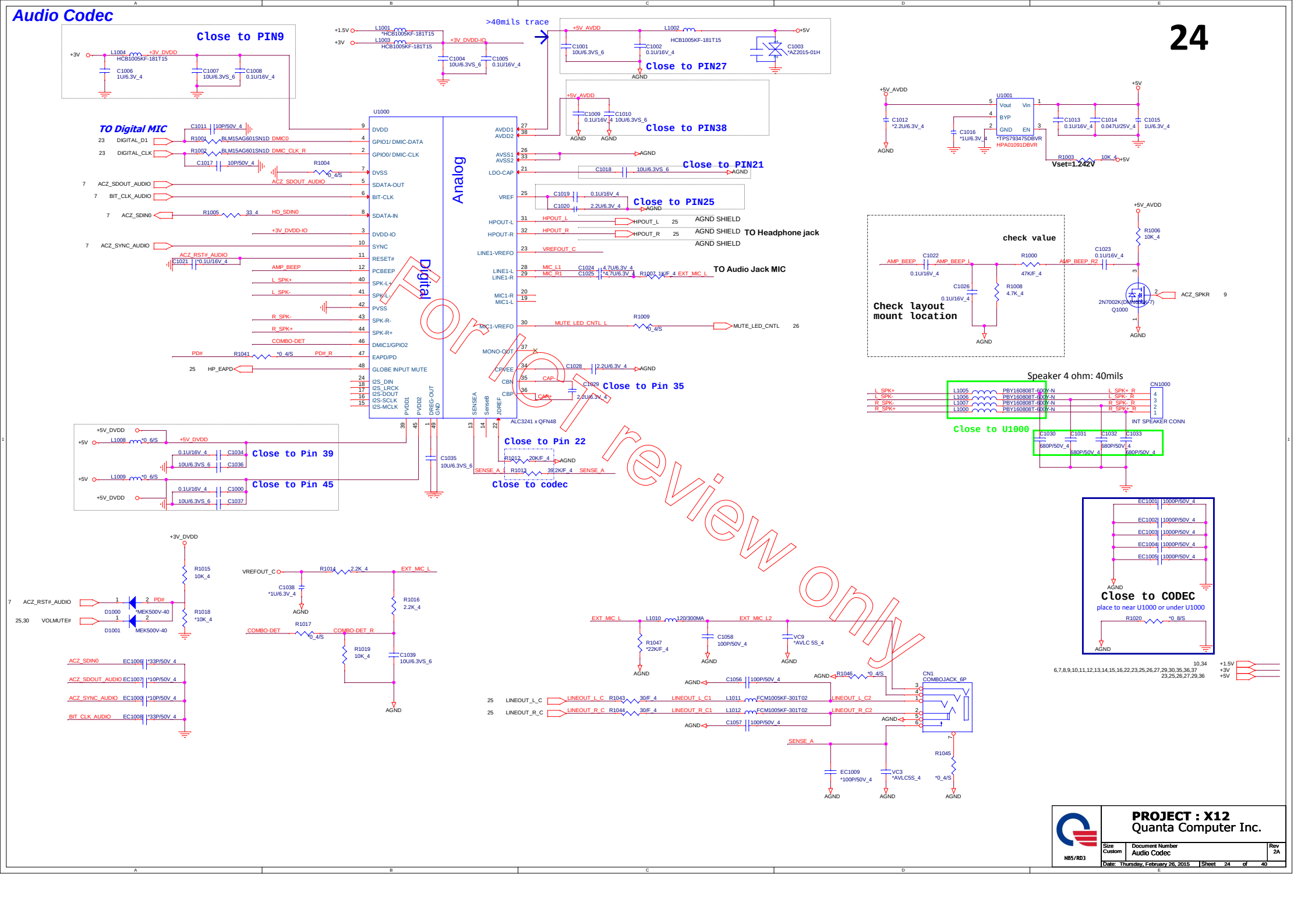
NB5/RD3

PROJECT : X12
Quanta Computer Inc.

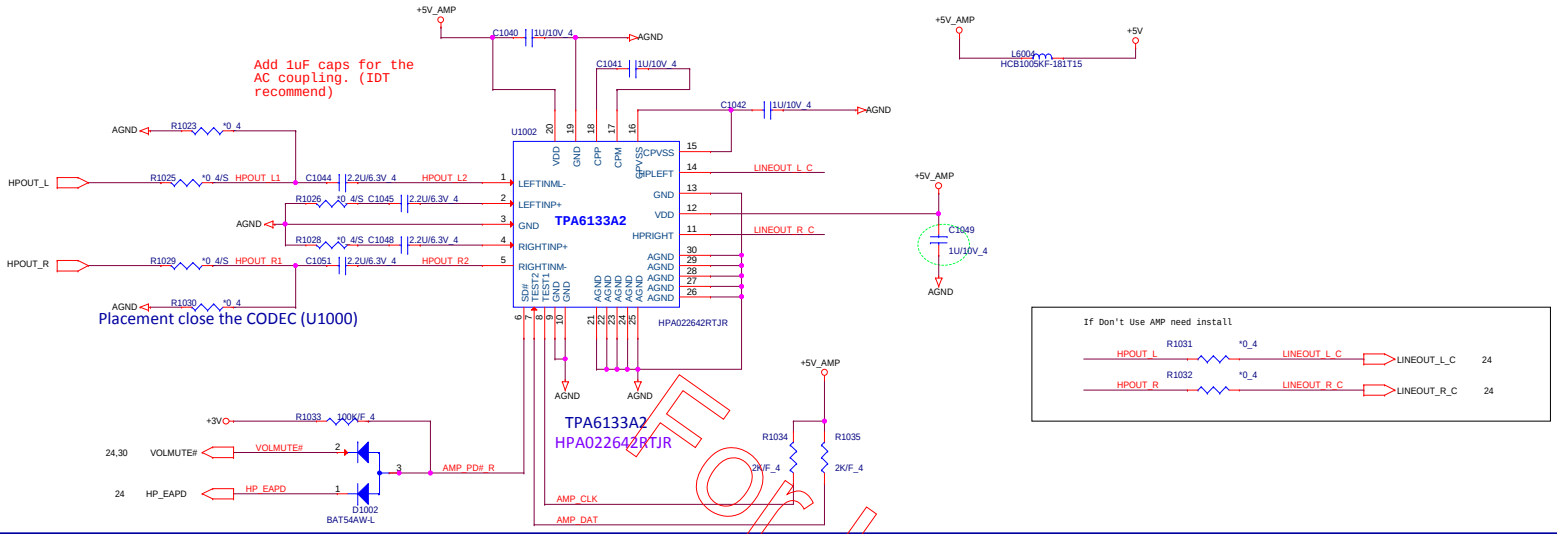
Size	Document Number	Rev
Custom	LCD CONN/LID/CAM/D-MIC	1A

Date: Thursday, February 26, 2015 Sheet 23 of 40

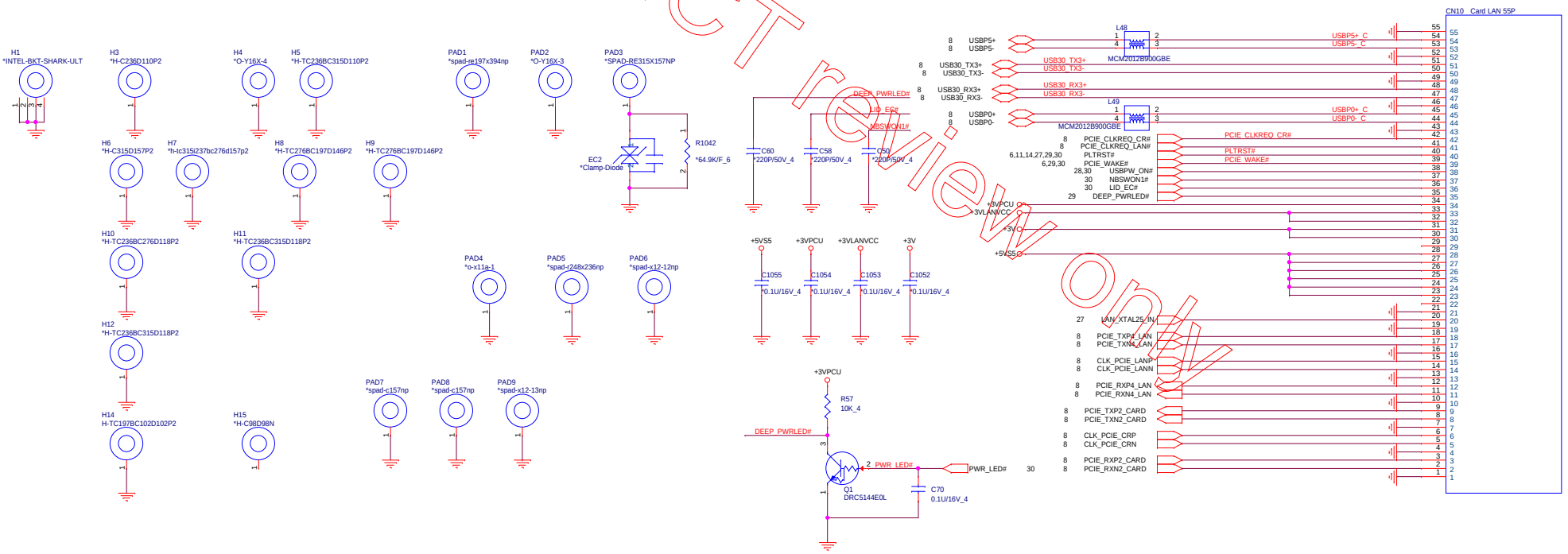
Audio Codec


Close to PIN9
>40mils trace
Close to PIN27
Close to PIN38
Close to PIN21
Close to PIN25
TO Digital MIC
U1000
Analog
Digital
AVDD1
AVDD2
AVSS1
AVSS2
LDO-CAP
VREF
HPOUT-L
HPOUT-R
LINE1-VREFO
LINE1-L
LINE1-R
MIC1-R
MIC1-L
MIC1-VREFO
MONO-OUT
CPVEE
CBN
CBP
CAP-
CAP+
SENSEA
SenseB
JDREF
ALC3241 x QFN48
TO Headphone jack
TO Audio Jack MIC
Close to Pin 35
Close to Pin 22
Close to codec
Close to Pin 39
Close to Pin 45
check value
Check layout
mount location
Vset=1.242V
Speaker 4 ohm: 40mils
Close to U1000
INT SPEAKER CONN
Close to CODEC
place to near U1000 or under U1000
CN1
COMBOJACK_6P
Preliminary for review only

Head Phone out

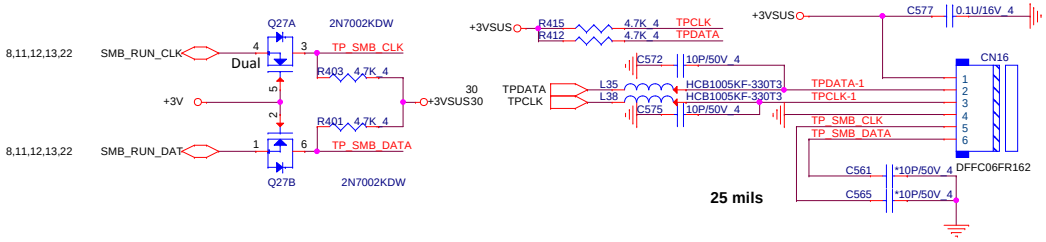


HOLE

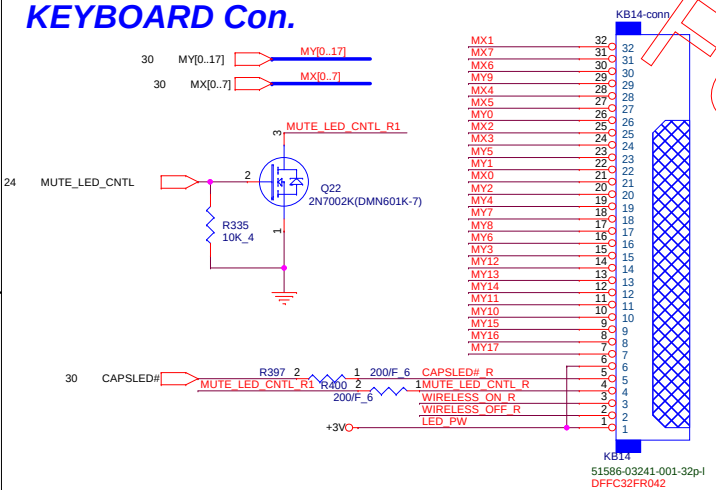


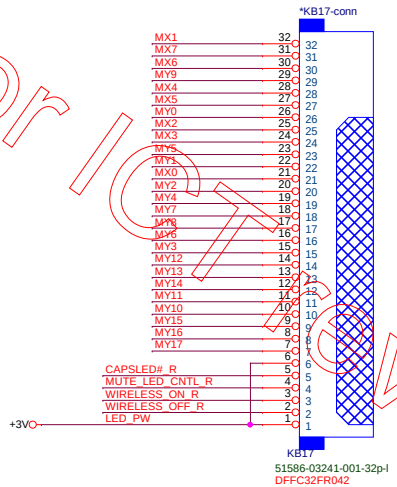
PROJECT : X12 Quanta Computer Inc.		
Size C	Document Number Card Reader	Rev 1A
NB5/RD3	Date: Thursday, February 26, 2015	Sheet 25 of 40

Touch Pad Connector

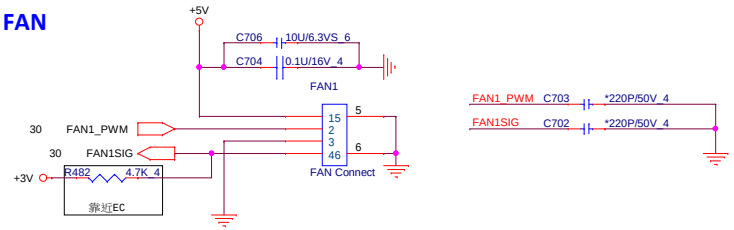


KEYBOARD Con.

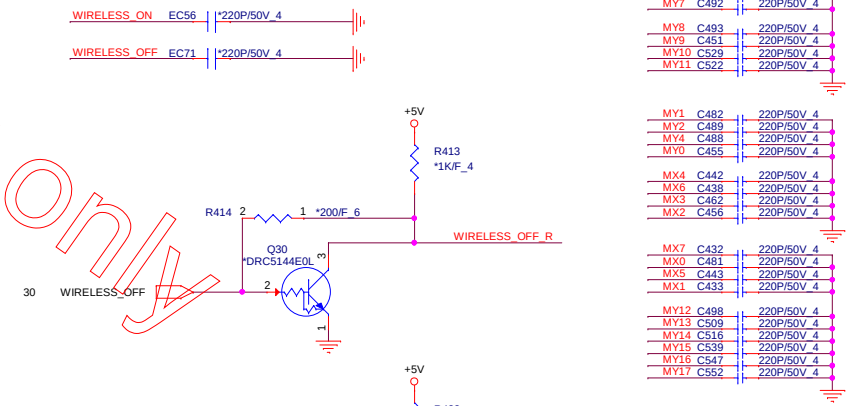


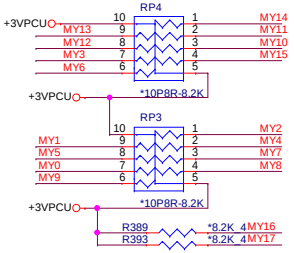


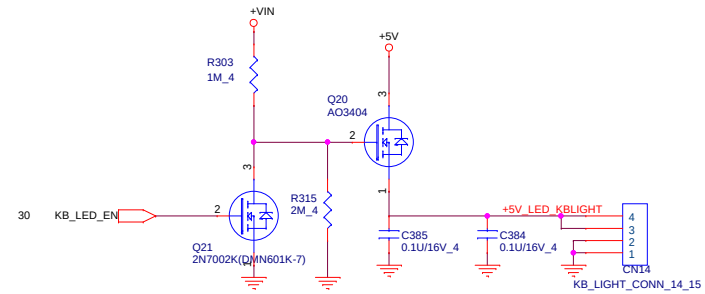
FAN

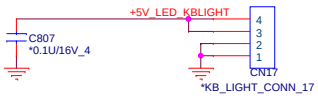


KEYBOARD PULL-UP







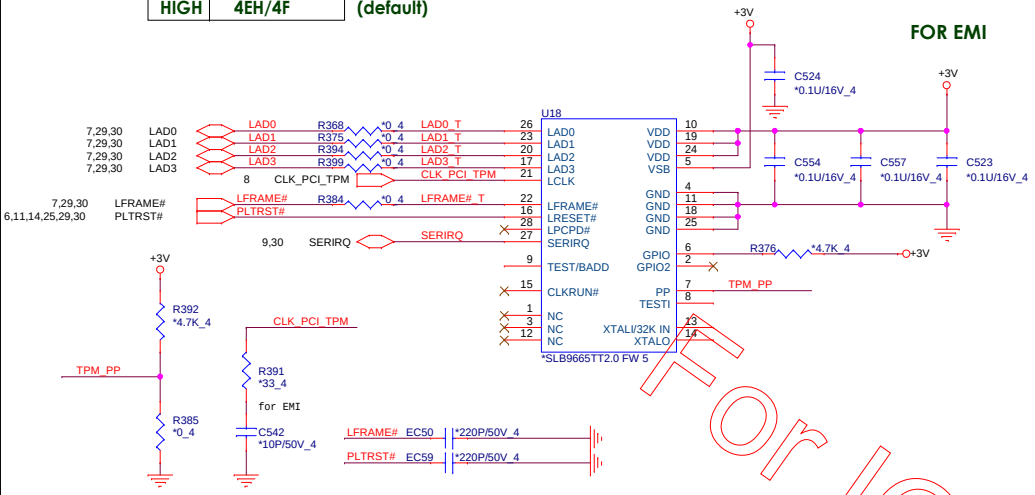


N85/RD3	PROJECT : X12 Quanta Computer Inc.	
Size Custom	Document Number PB/TP/KB/FAN/EMI Cap	Rev 1A
Date: Thursday, February 26, 2015	Sheet 26 of 40	

TPM (2.0)

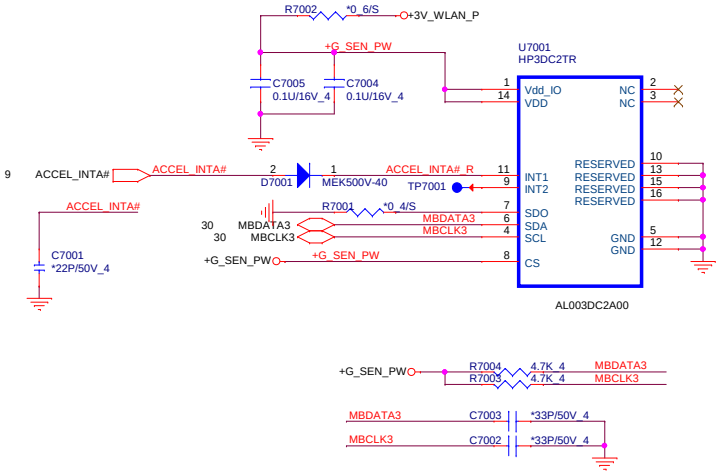
Address

	BADD
HIGH	4EH/4F (default)

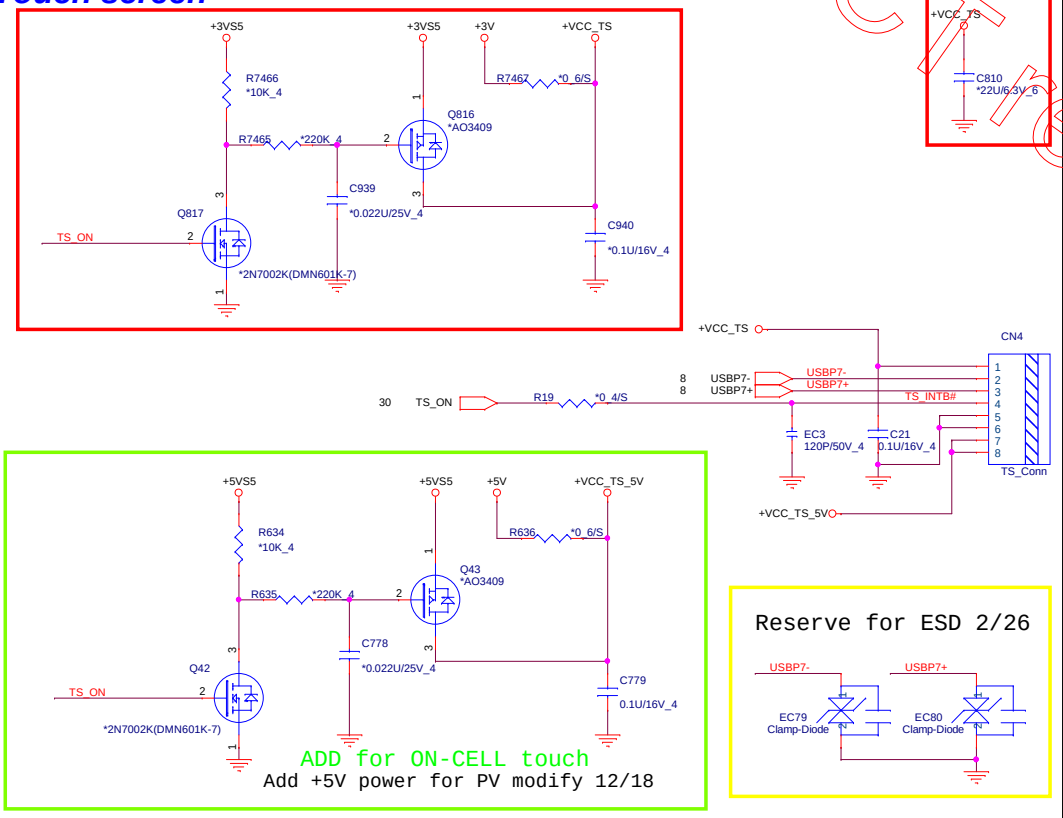


Accelerometer Sensor

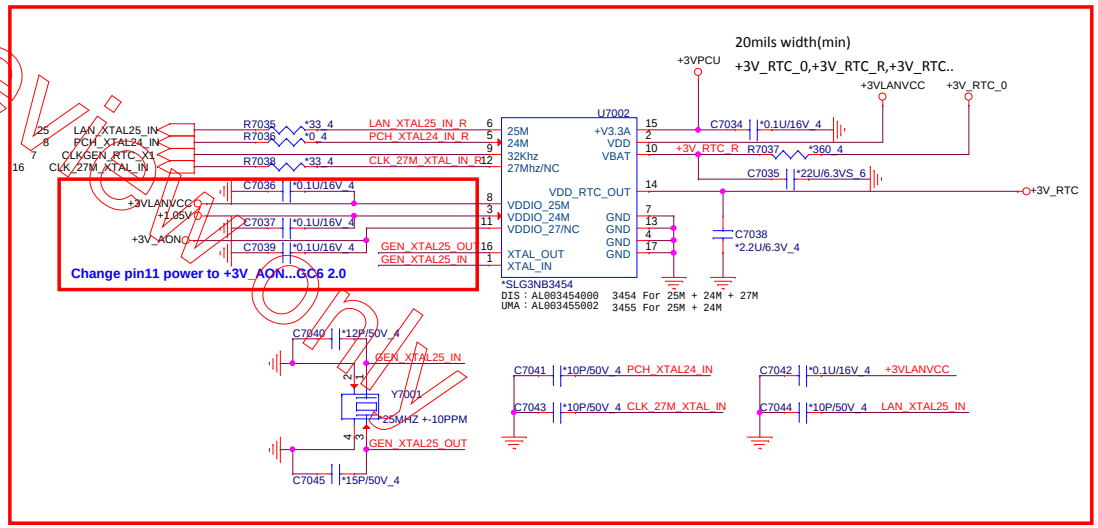
G-Sensor Power need check



Touch screen



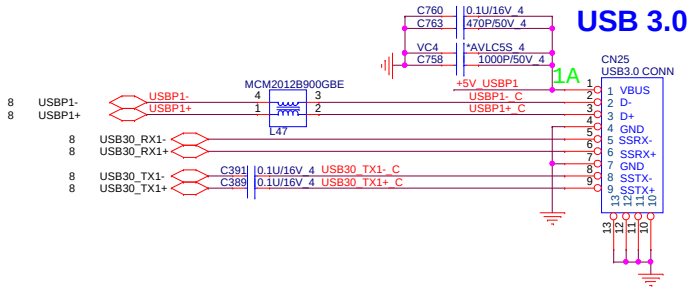
Green CLK Circuitry

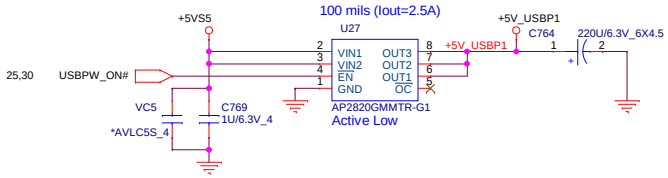


Change Green CLK to Crystal 11/21 SI

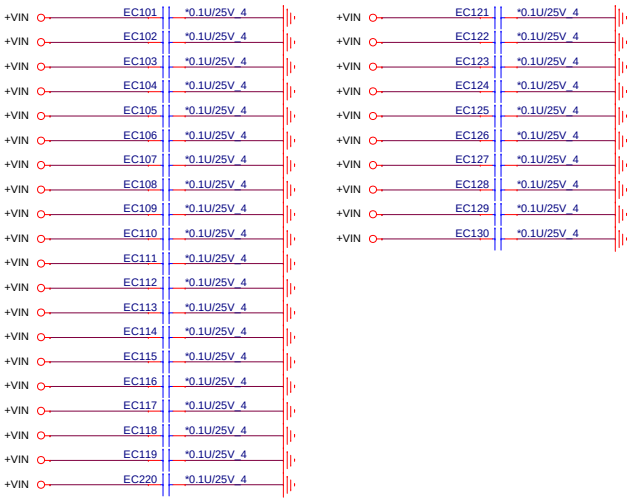
N85/RD3	PROJECT : X12 Quanta Computer Inc.	
Size: Custom	Document Number: TPM/G-Sensor/G-CLK/TS/FP	Rev: 1A
Date: Thursday, February 26, 2015	Sheet: 27of	40

USB 2.0/3.0 Combo



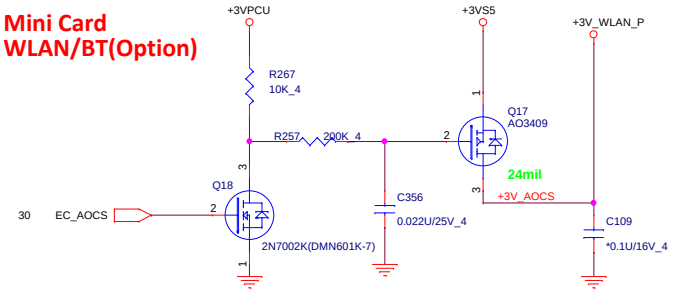


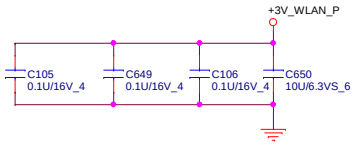
EMI CAP



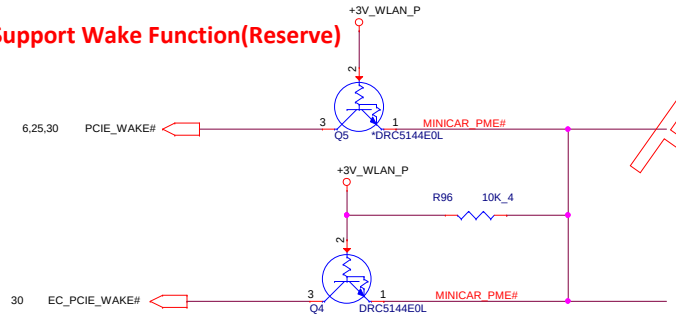
N85/RD3	**PROJECT : X12** Quanta Computer Inc.	
Size: Custom	Document Number: **USB 3.0**	Rev: 1A
Date: Thursday, February 26, 2015	Sheet 28 of 40	

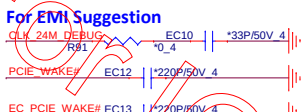
Mini Card WLAN/BT(Option)

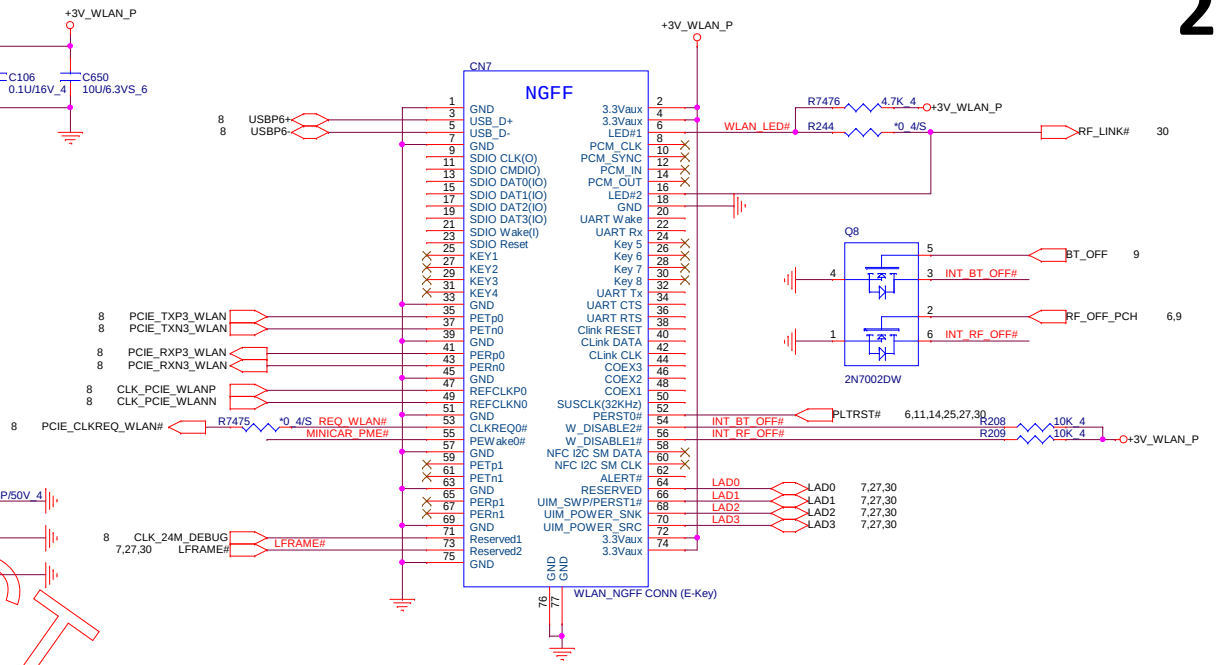




Support Wake Function(Reserve)

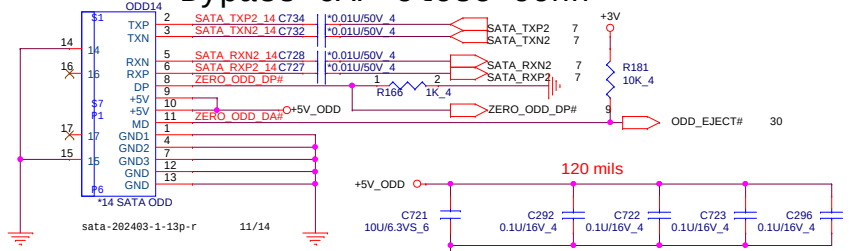


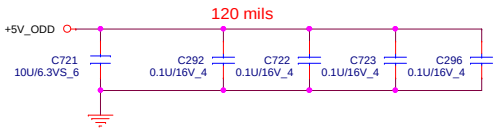




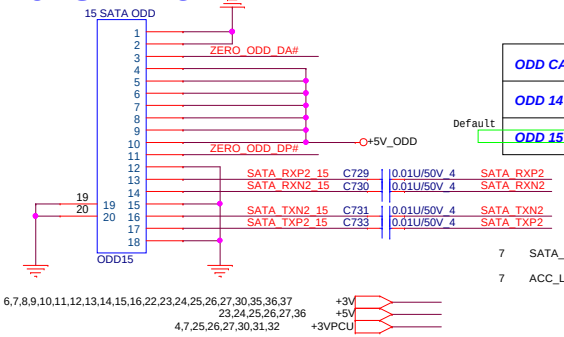
14" SATA ODD

Bypass CAP close conn

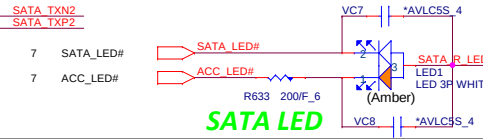




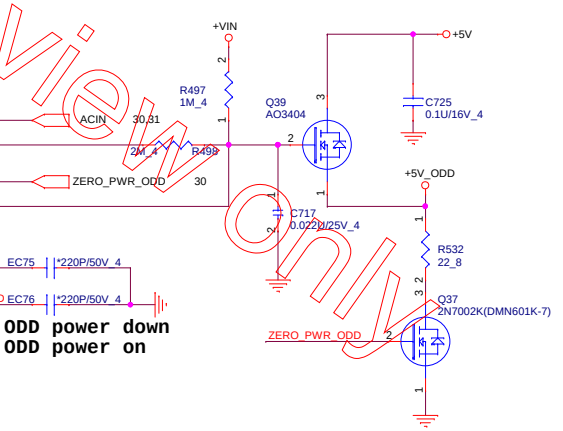
15" SATA ODD



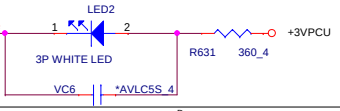
ODD CAP Setting	C727/C728/C732/C734	C729/C730/C731/C733
ODD 14"	O	X
Default ODD 15"/17"	X	O



SATA LED

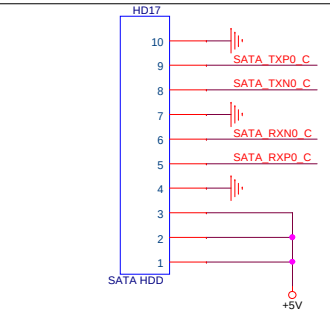


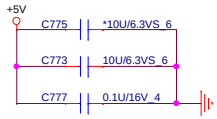
High : ODD power down
Low : ODD power on



PWR LED

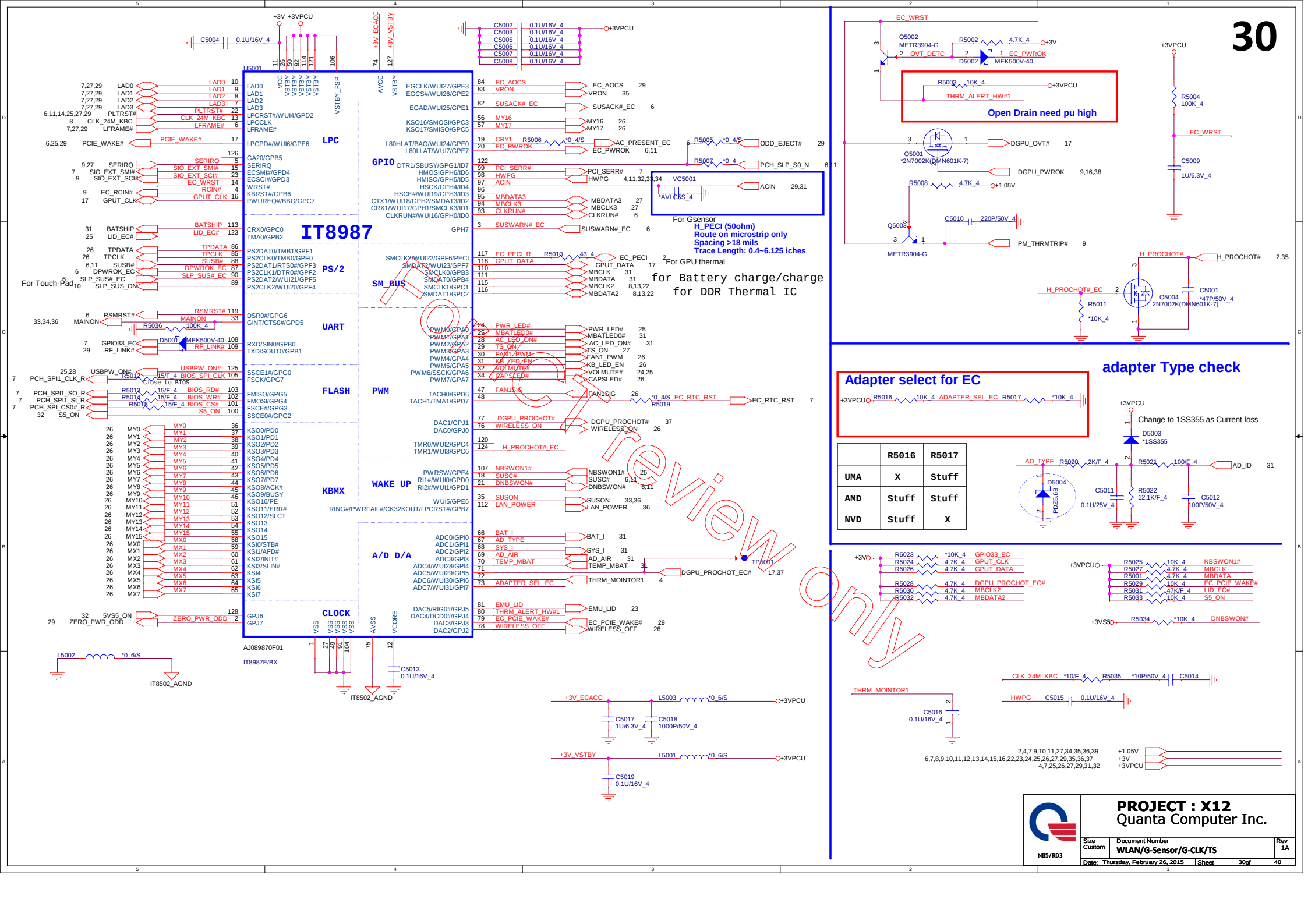
HDD





PROJECT : X12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	WLAN/NGFF/MSATA	1A
N85/RD3	Date: Thursday, February 26, 2015	Sheet 29of 40



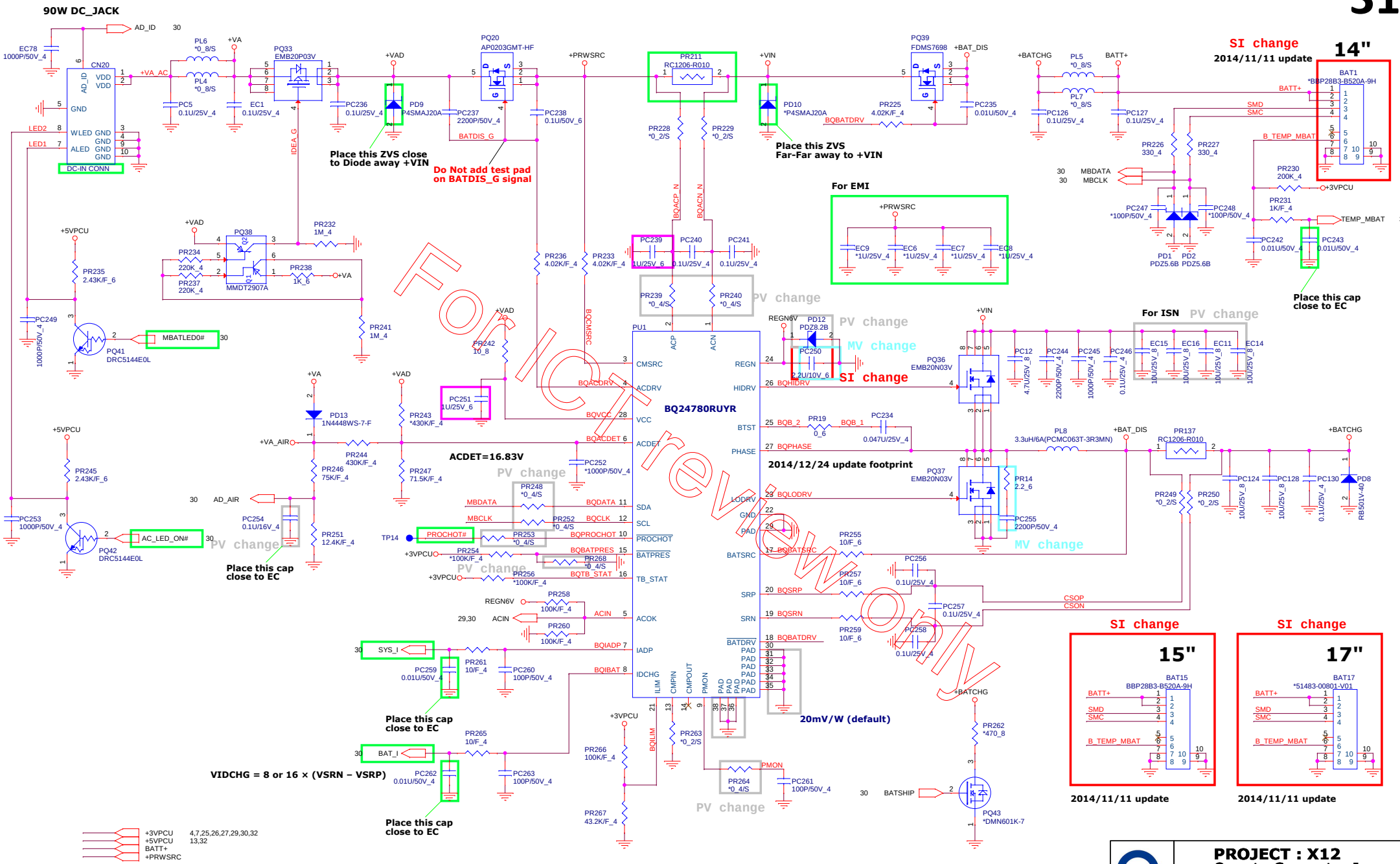
	R5016	R5017
UMA	X	Stuff
AMD	Stuff	Stuff
NVD	Stuff	X

PROJECT : X12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	WLAN/G-Sensor/G-CLK/TS	1A

Date: Thursday, February 26, 2015 | Sheet 30of 40

N85/RD3

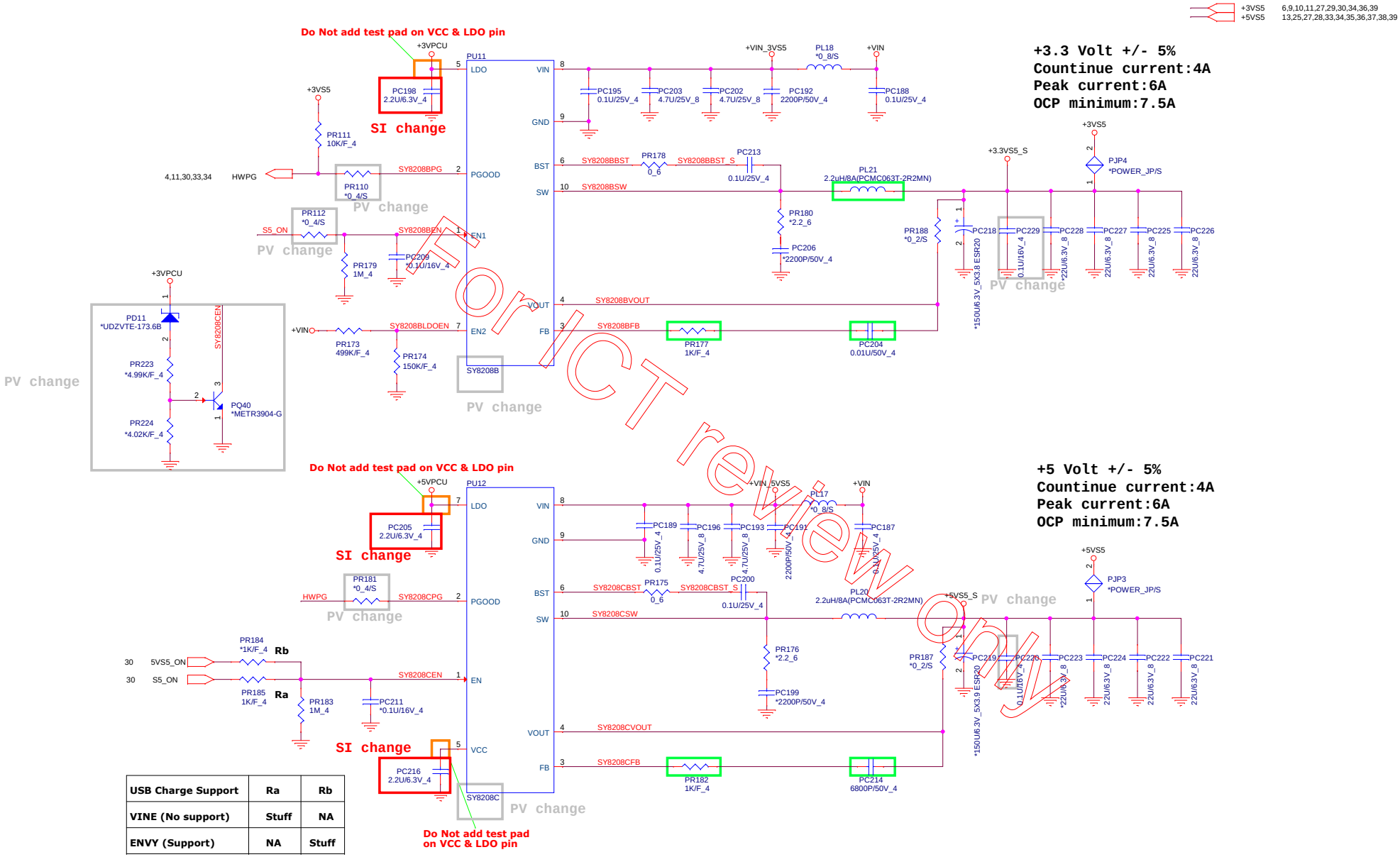


+3VPCU	4,7,25,26,27,29,30,32
+5VPCU	13,32
BATT+	
+PRWSRC	

PROJECT : X12
Quanta Computer Inc.

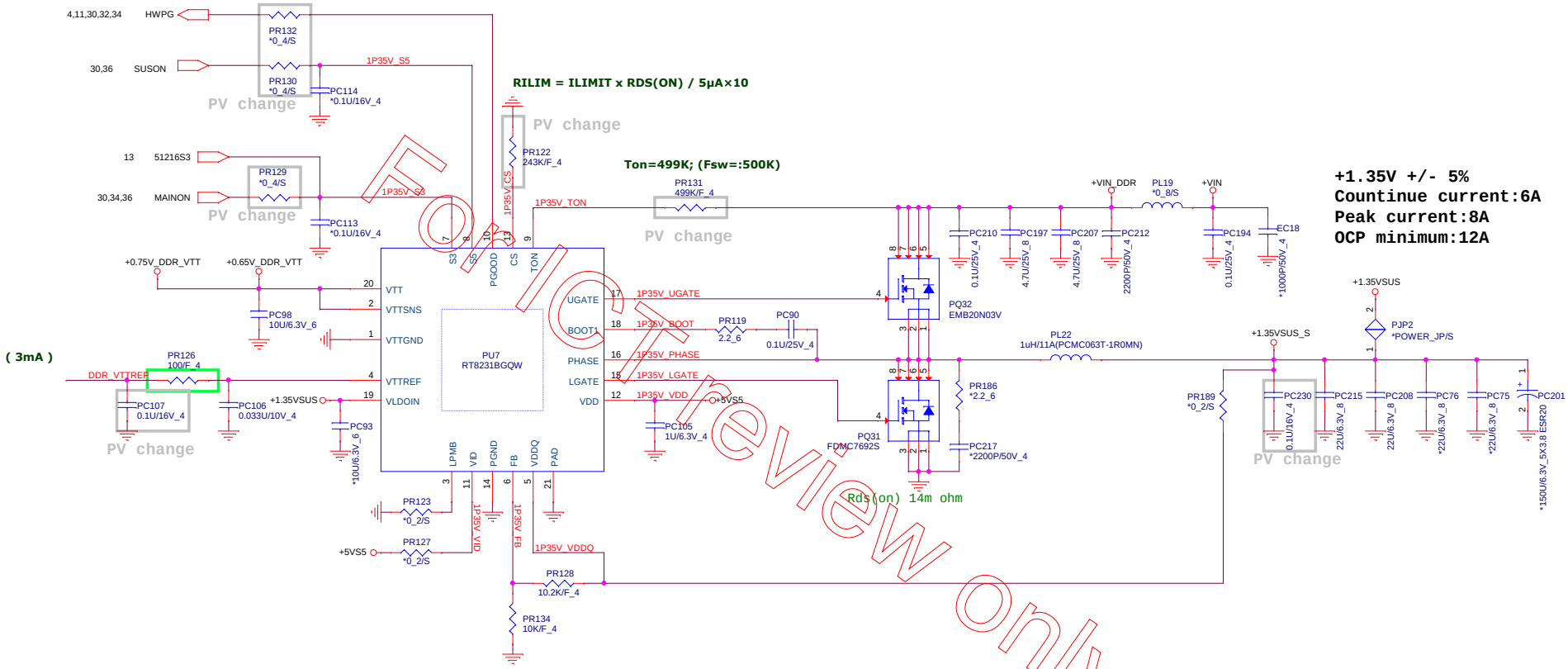
Size	Document Number	Rev
Custom	Charger (BQ24780)	1A
Date: Thursday, February 26, 2015	Sheet 31 of 40	

N85/RD3

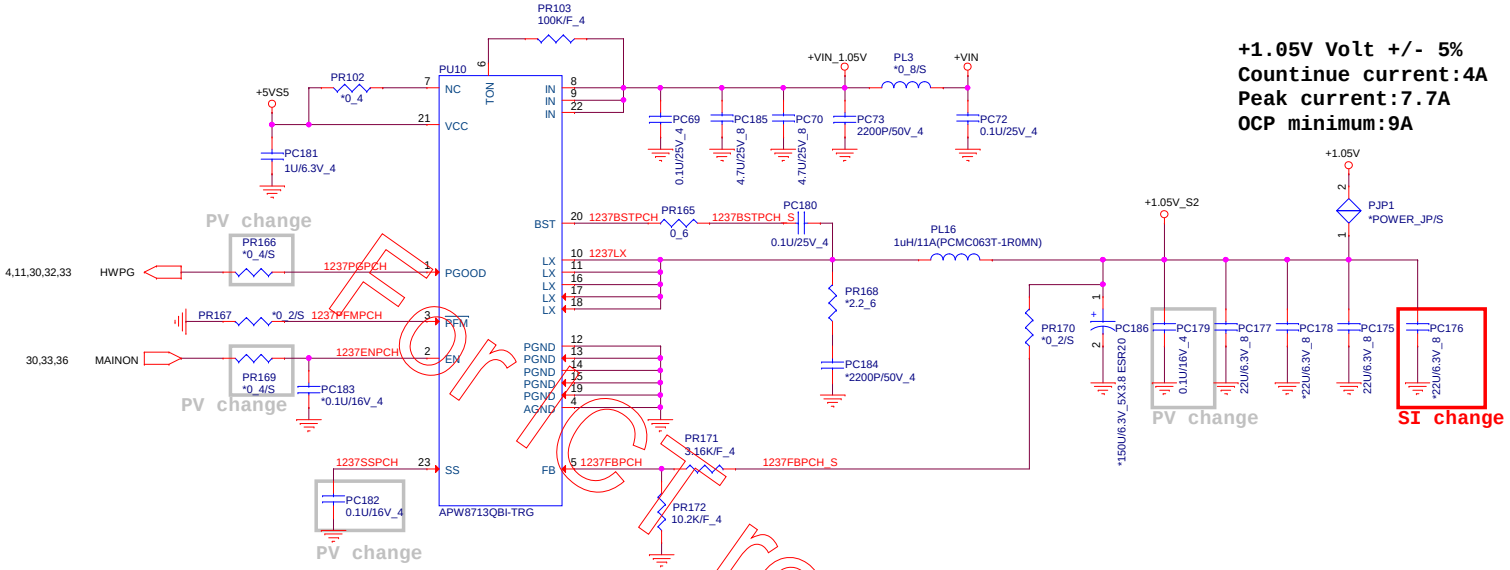


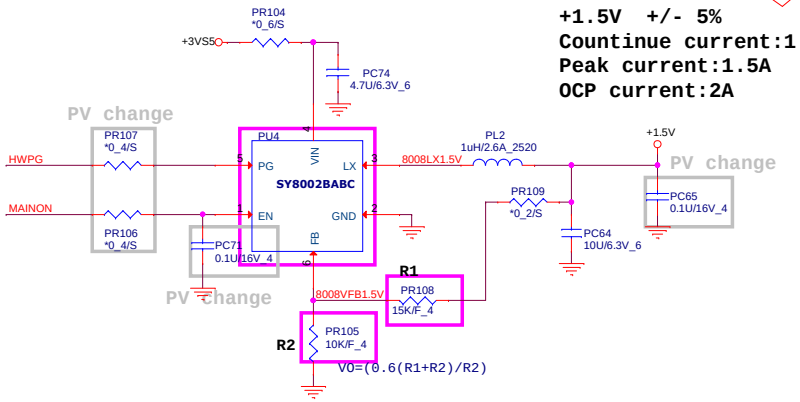
USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

N85/RD3	PROJECT : X12 Quanta Computer Inc.	
Size: Custom	Document Number: 3/5VPCU(RT8243A)	Rev: 1A
Date: Thursday, February 26, 2015	Sheet: 32 of 40	



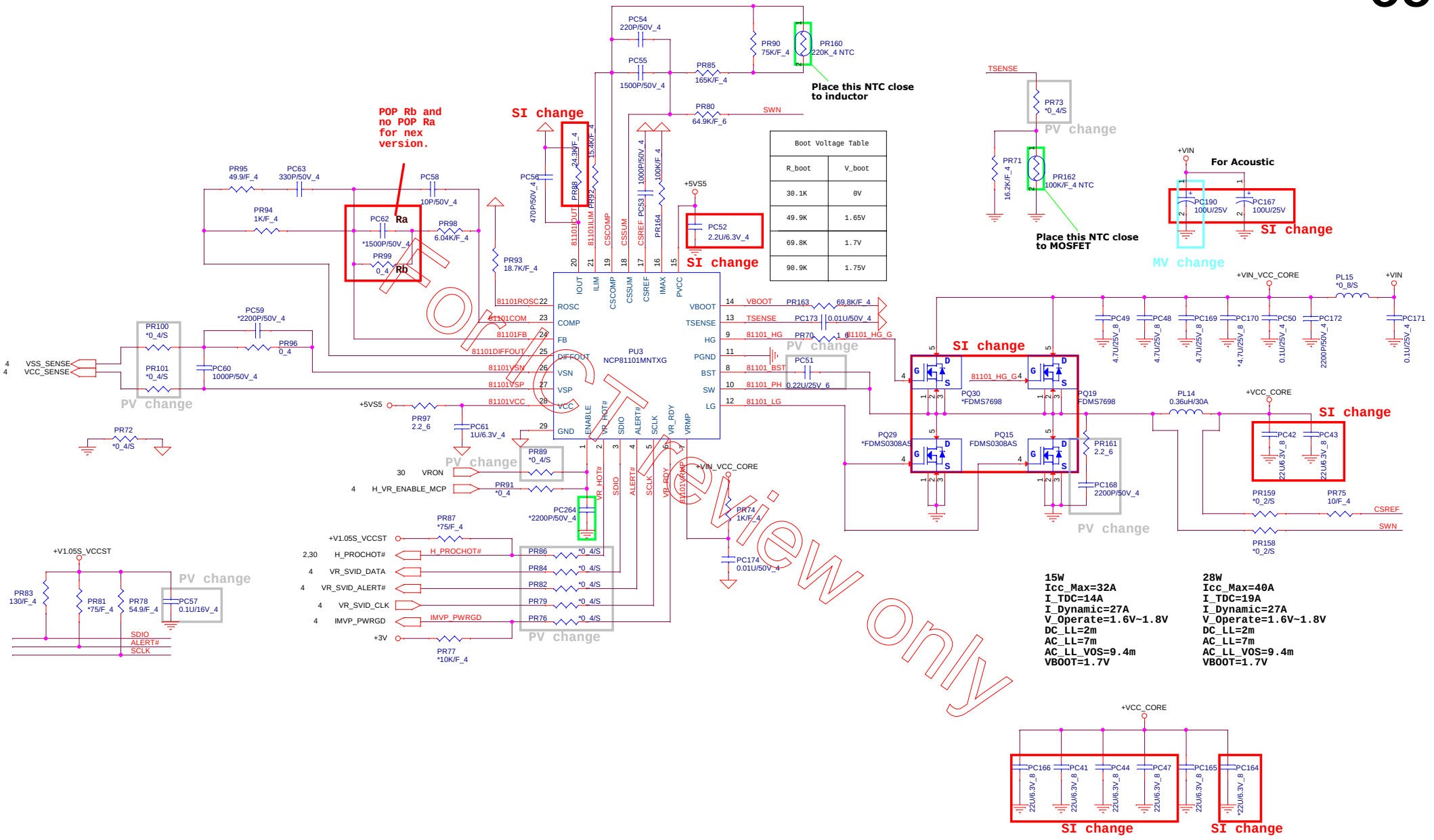
N85/RD3	PROJECT : X12 Quanta Computer Inc.	
Size Custom	Document Number DDR3 (RT8231A)/1.8VS5	Rev 1A
Date: Thursday, February 26, 2015	Sheet 33 of 40	



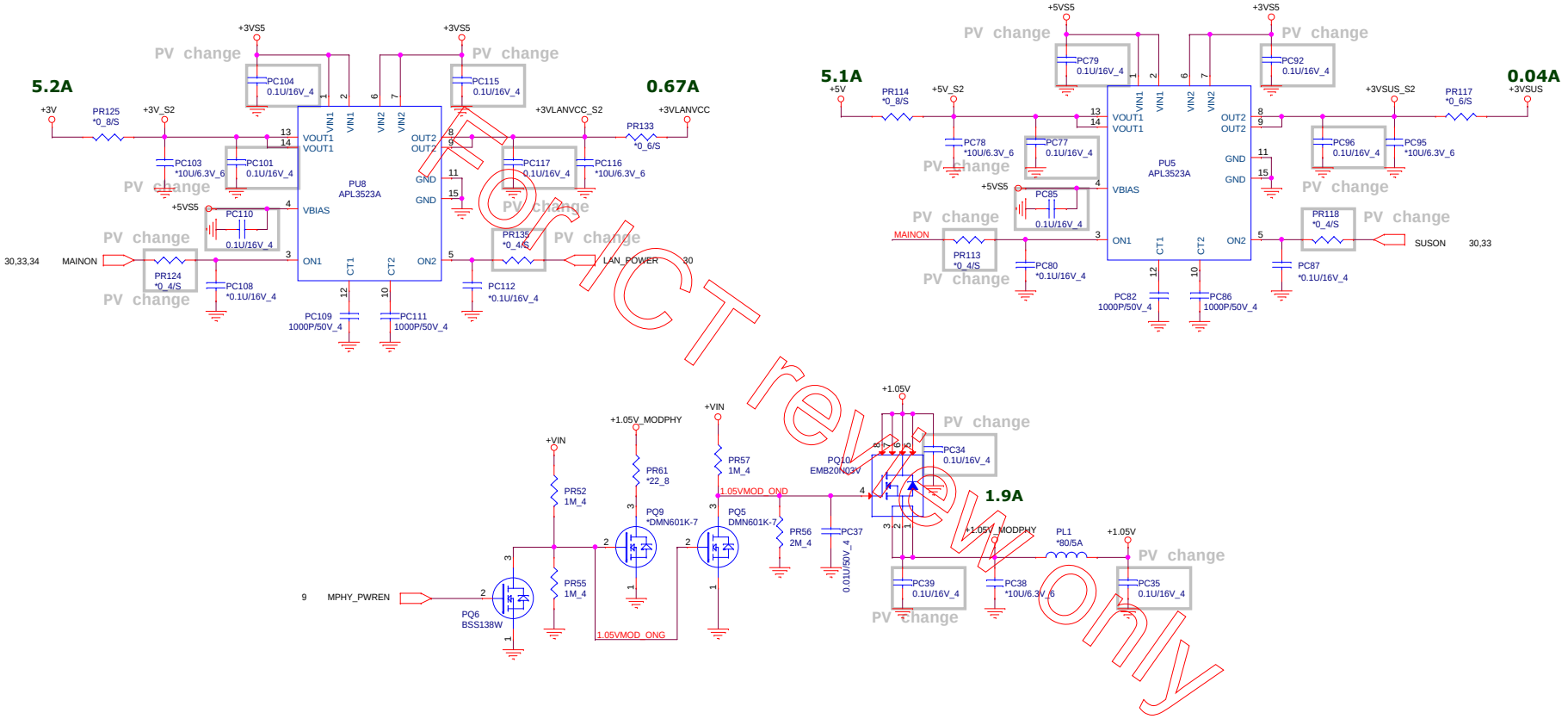


+VIN 23,26,28,29,31,32,33,35,36,37,38,39
+3VS5 6,9,10,11,27,29,30,32,36,39
+5VS5 13,25,27,28,32,33,35,36,37,38,39

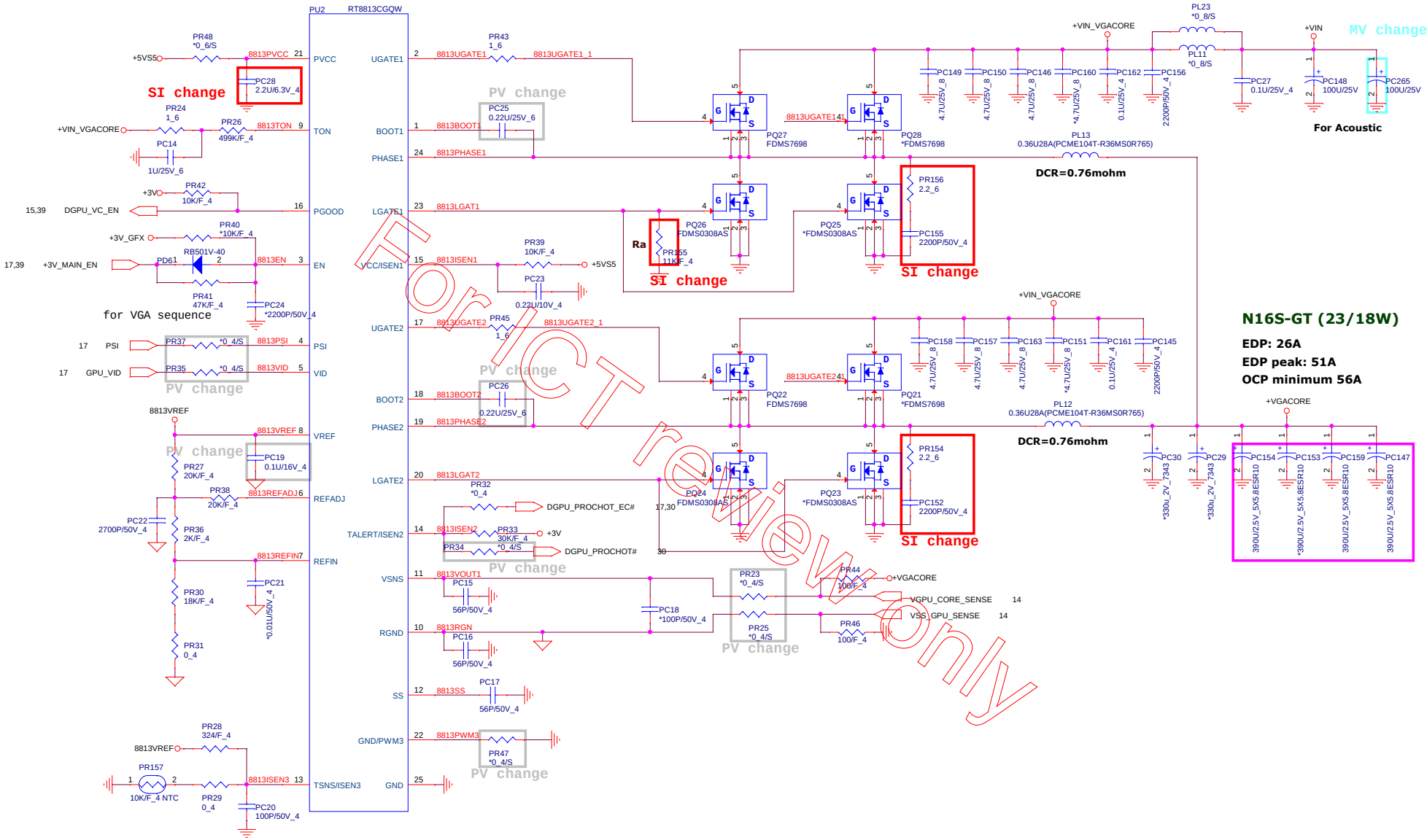
N85/RD3	PROJECT : X12 Quanta Computer Inc.	
Size: Custom	Document Number: +1.1VS5 (RT8228)/2.5V	Rev: 1A
Date: Thursday, February 26, 2015	Sheet 34 of 40	



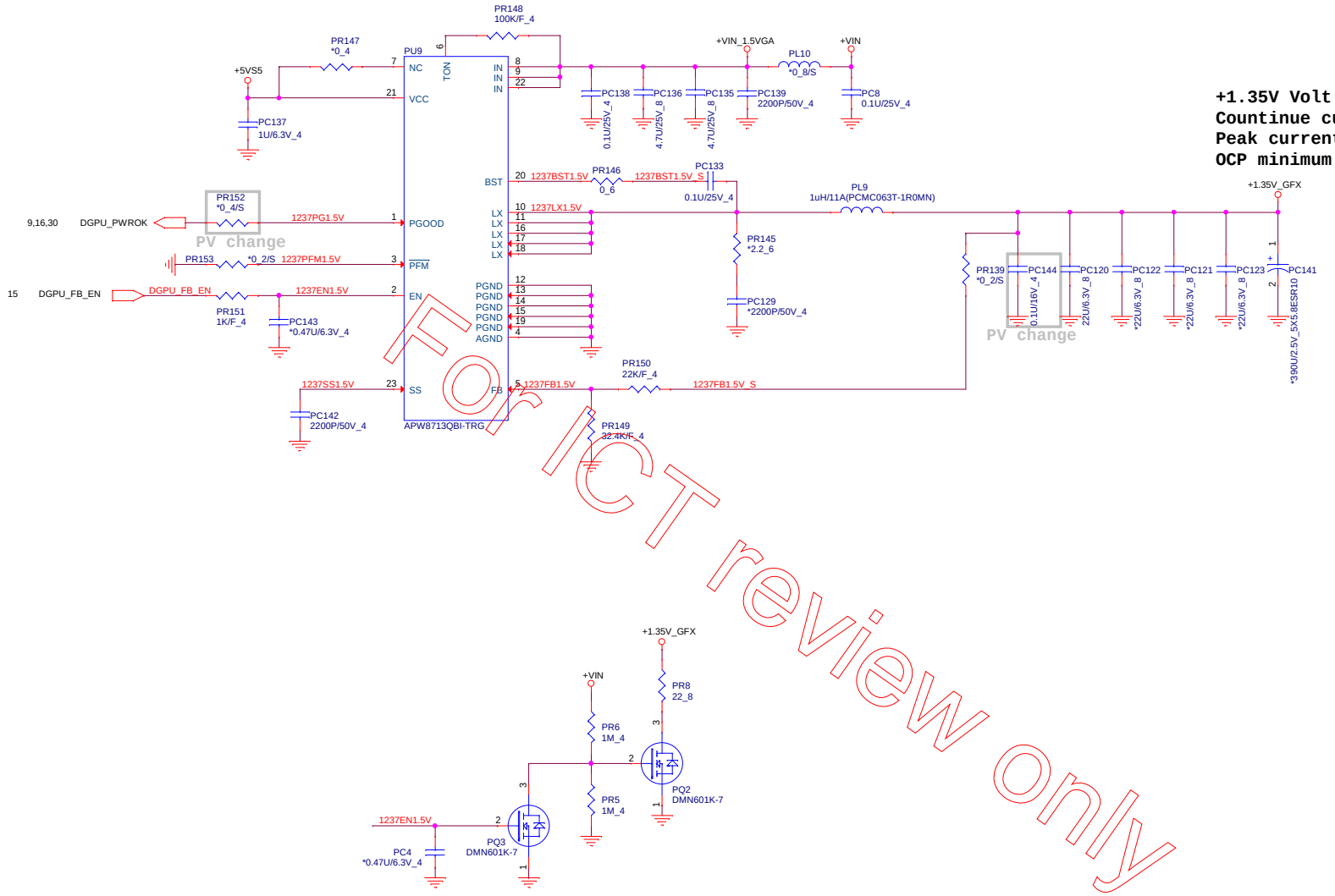
PROJECT : X12	
Quanta Computer Inc.	
N85/RD3	Size: Custom; Document Number: CPU Core (NCP81101)ULT; Rev: 1A
Date: Thursday, February 26, 2015	Sheet 35 of 40



NB5/RD3	PROJECT : X12 Quanta Computer Inc.	
Size: Custom	Document Number: Dis-charge IC (SLG55448)	Rev: 1A
Date: Thursday, February 26, 2015	Sheet 36 of 40	

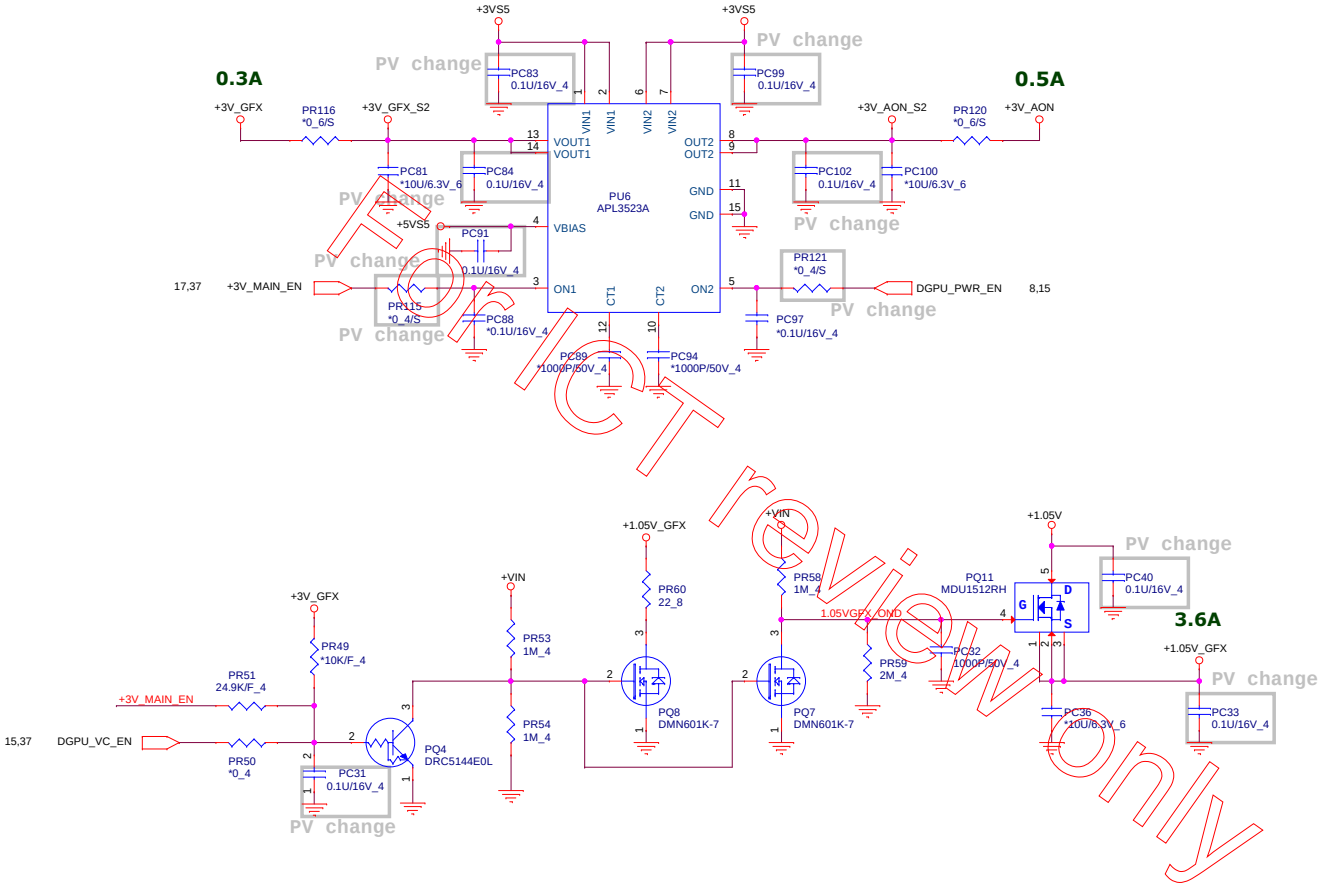


PROJECT : X12	Quanta Computer Inc.
Size: Custom	Document Number: +VGACORE (RT8813A)
Rev: ?	
Date: Thursday, February 26, 2015	Sheet 37 of 40
N85/RD3	



+1.35V Volt +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A

NB5/RD3	**PROJECT : X12** Quanta Computer Inc.	
Size: Custom	Document Number: **+1.35V_VGA(AOZ1237)**	Rev: 1A
Date: Thursday, February 26, 2015	Sheet 38 of 40	



N85/RD3	PROJECT : X12 Quanta Computer Inc.	
Size: Custom	Document Number: 1.05V_VGA/3V_VGA	Rev: ?
Date: Thursday, February 26, 2015	Sheet 39 of 40	

Battery Connector	Pavillion	ENVY
14"	-	-
15"	-	-
17"	-	-

USB Charge Support	PR185	PR184
Pavillion	Stuff	NA
ENVY (USB charge)	NA	Stuff

UMA	Disable Page 41、42、43 ,but keep below location
Page 41	PC161、PC162
Page 42	PC138、PC144、PC4、PC148
Page 43	PC84、PC102、PC88、PC97、PC40、PC33

Discrete	Location	Part Number
N15S (25W)	PR155	CS29532FB10
	PC151、PC160	NA
	PQ21、PQ23、PQ25、PQ28	NA
N15P (35W)	PR155	CS31242FB13
	PC151、PC160	Stuff
	PQ21、PQ23、PQ25、PQ28	Stuff