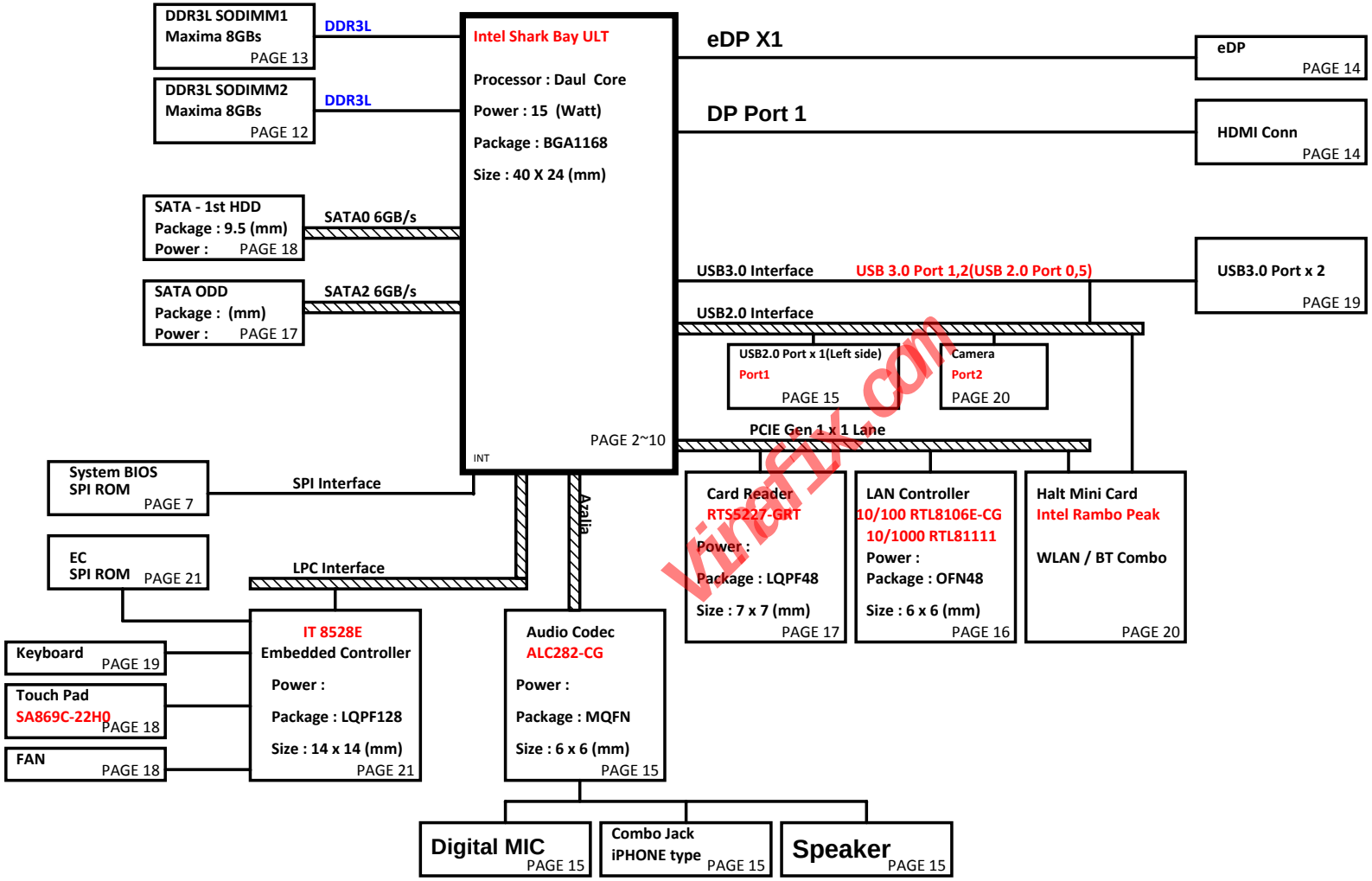
FF6 15.6" Ultra/Slim
Intel Shark Bay ULT Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



Quanta Computer Inc.
PROJECT : FF6

Size	Document Number	Rev
	BLOCK DIAGRAM	A1

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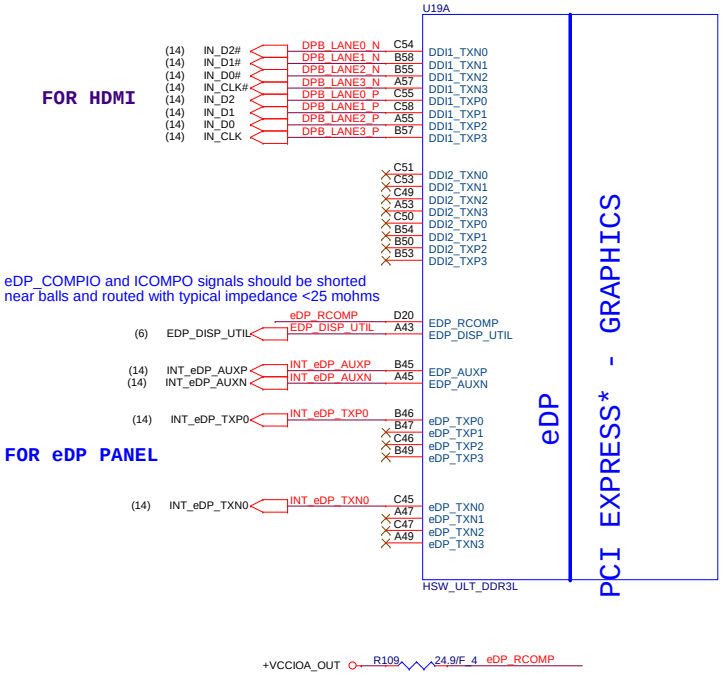
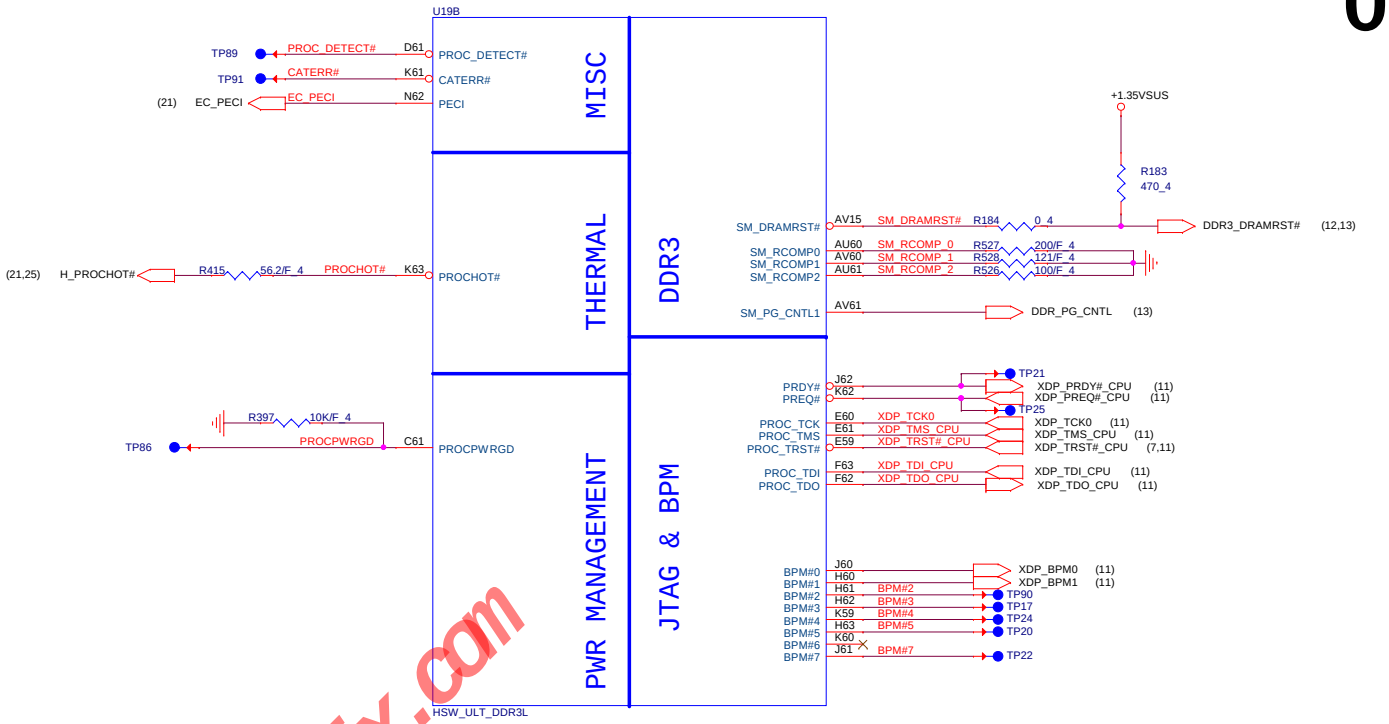
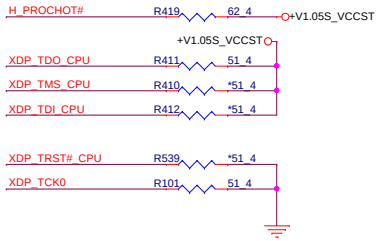




Processor pull-up (CPU)



Quanta Computer Inc.
PROJECT : FF6

Size	Document Number	Rev
	ULT 1/9(eDP/DDI)	A1

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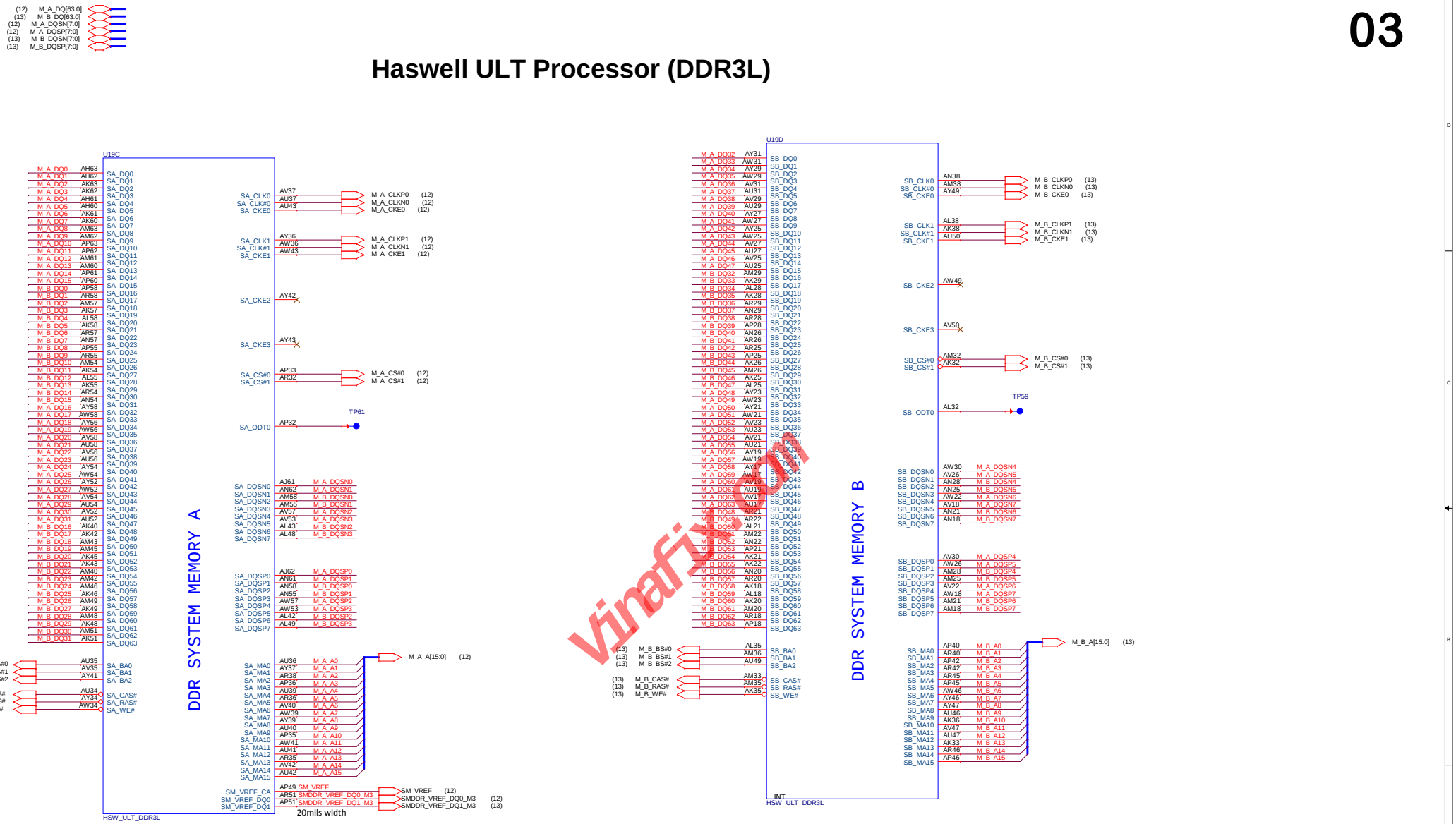
Haswell ULT Processor (DDR3L)



Quanta Computer Inc.		
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Size	Document Number: ULT 2/9 (DDR3 I/F)	Rev: A1
Date: Thursday, February 13, 2014	Sheet 3 of 36	

POWER

32A
+VCC_CORE

U19F

HSW ULT POWER

1.4A
+1.35VSUS
Close to CPU

Direct tie to CPU VCC/VSS-Ball

CFG0-19 need Reserve TP

U19E

RESERVED

HSW_ULT_DDR3L

Layout note: need routing together and ALERT need between CLK and DATA.

SVID ALERT

SVID CLK

SVID DATA

Place PU resistor close to VR

100- ±1% pull-up to VCC near processor.

Q8
2N7002BKS

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R452 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R143 1K_4

+VCCIOA_OUT (2)
+VCCIO_OUT (6)
+1.5V (10,15,18,20,23)
+1.35VSUS (2,12,13,18,24)
+1.05V (7,10,11,20,23,26)
+VCC_CORE (25)

Quanta Computer Inc.
PROJECT : FF6

Size	Document Number	Rev
	04 -- ULT 3/9 (POWER-1)	A1

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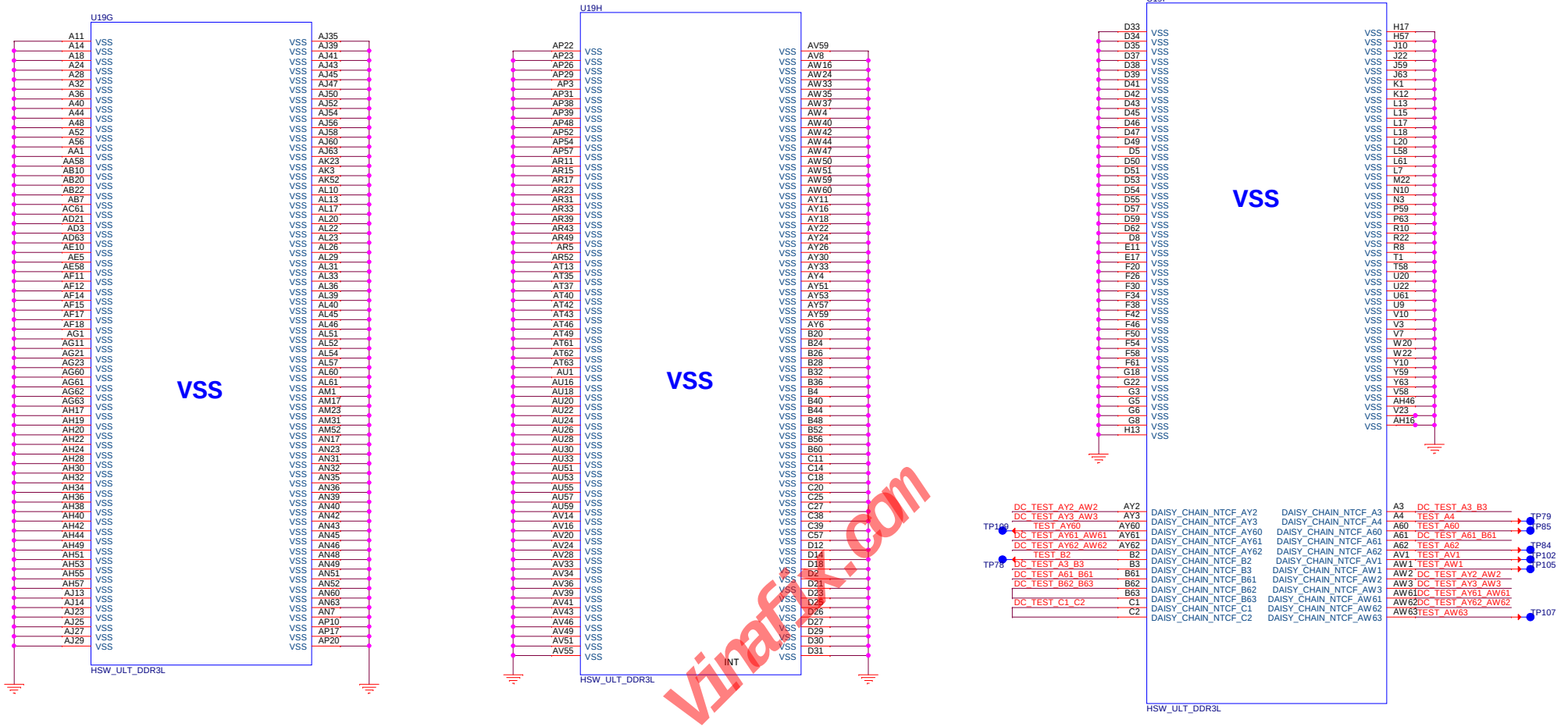

05

Quanta Computer Inc.

PROJECT : FF6

Size	Document Number	Rev
	ULT 4/9 (RSV,GND)	A1

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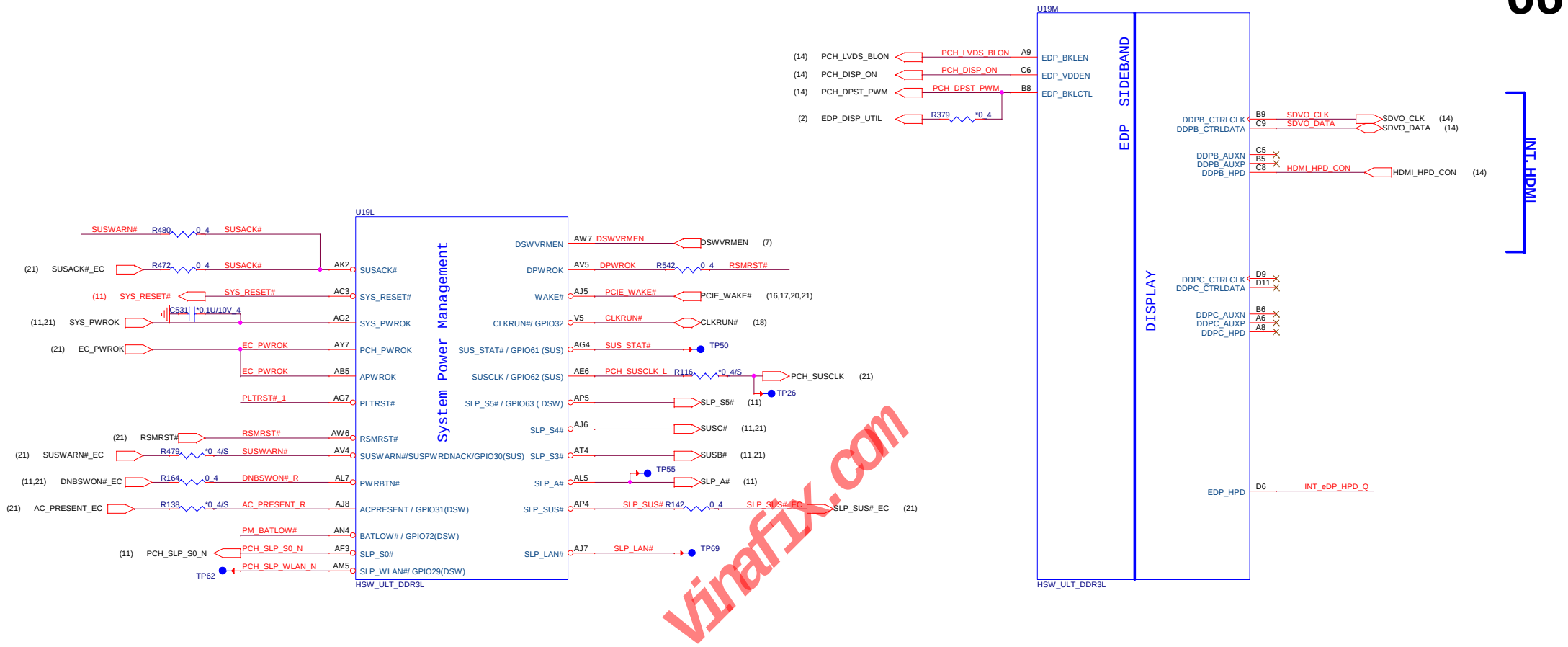
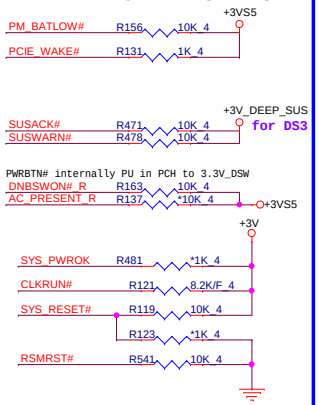
Lynx Point-LP Platform Controller Hub (LVDS,DDI)

06



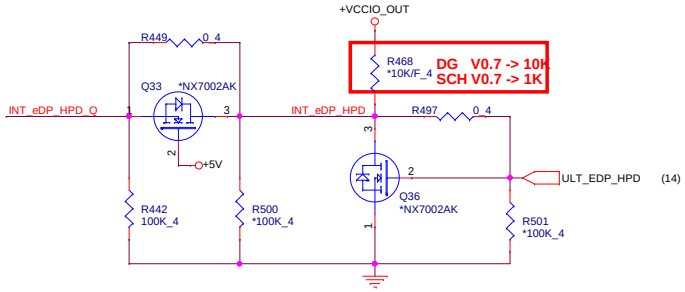
PCH Pull-high/low(CLG)



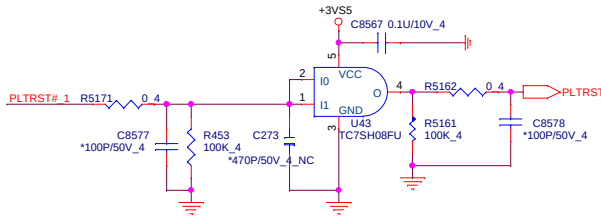
PLTRST#(CLG)

Check Q2010 Rise/Fall time less than 100ns

Reserve EDP_HPD opposites circuit!

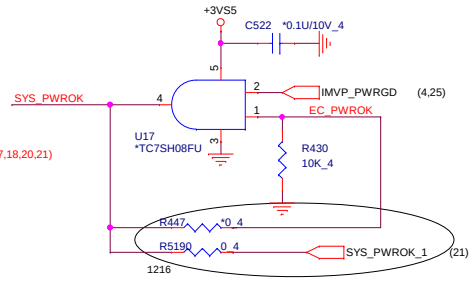


PLTRST# Buffer



(7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,25,26)
(9,10,11,18,20,22)
+3V
+3VS5

System PWR_OK(CLG)



Quanta Computer Inc.

PROJECT : FF6

Size	Document Number	Rev
	ULT 5/9(Power Manger)	A1
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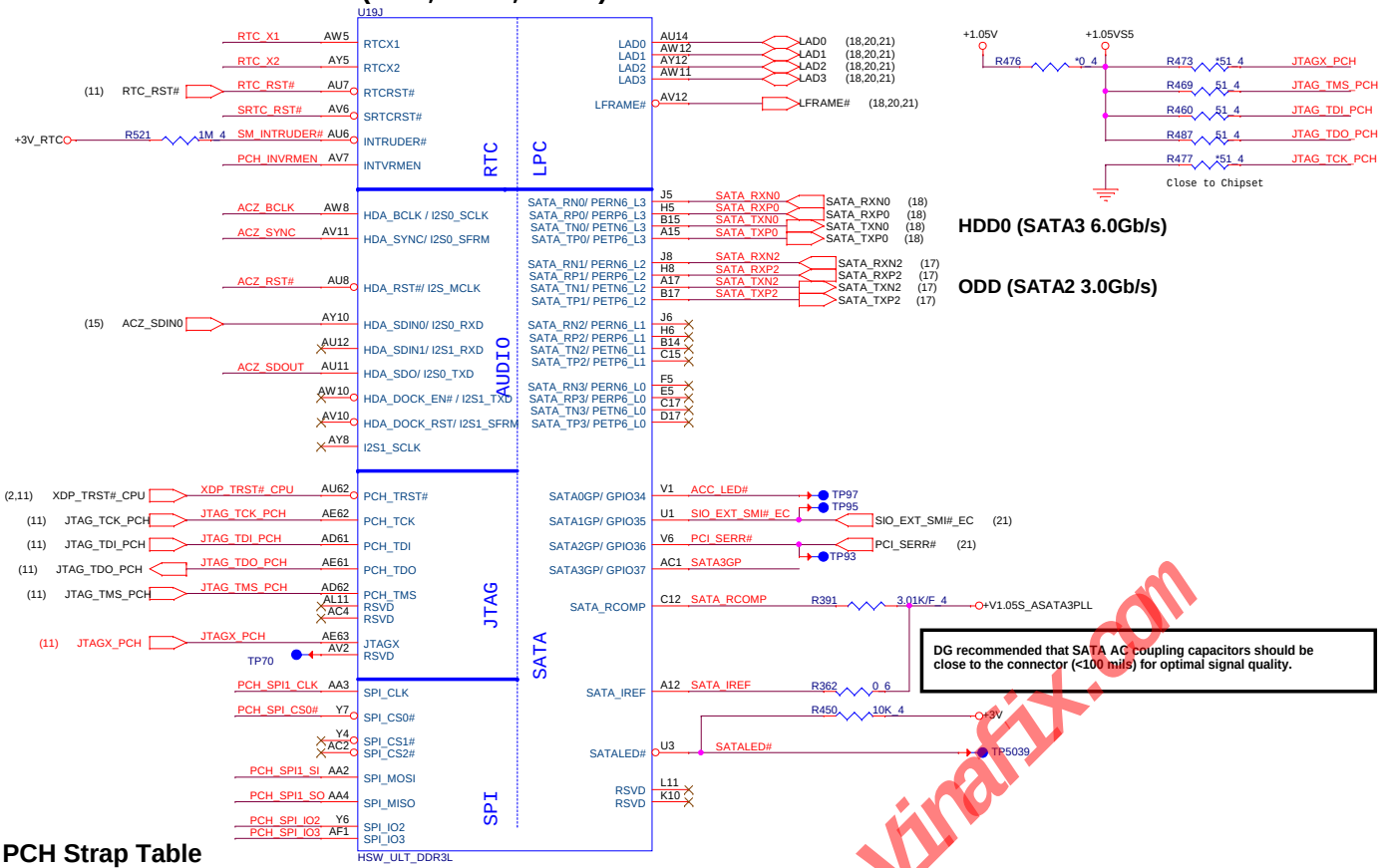
Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)

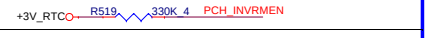
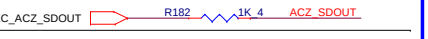
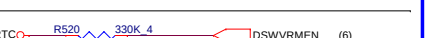


HDD0 (SATA3 6.0Gb/s)

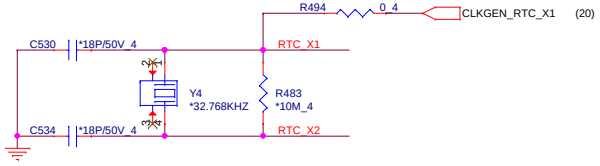
ODD (SATA2 3.0Gb/s)

DG recommended that SATA AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

PCH Strap Table

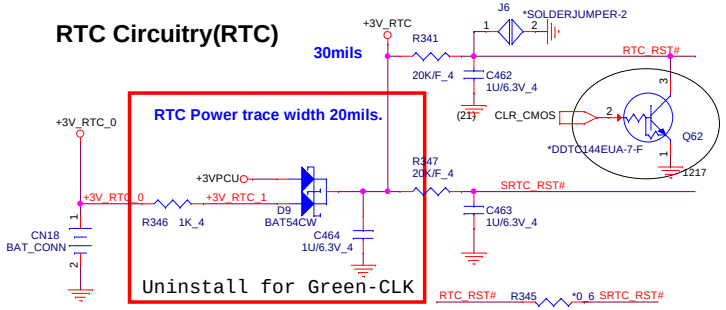
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	
HDA_SDO /I2S0_TXD	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overridde	
GSPI0_MOSI /GPIO86	Boot BIOS Selection	PWROK	GNT0# 1 = LPC; GNT0# 0 = SPI(Default)	
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality	
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	

RTC Clock 32.768KHz

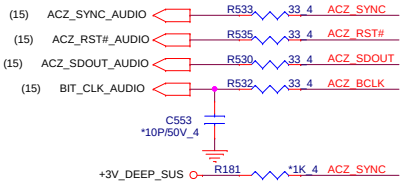


no stuff If use green clock

RTC Circuitry(RTC)



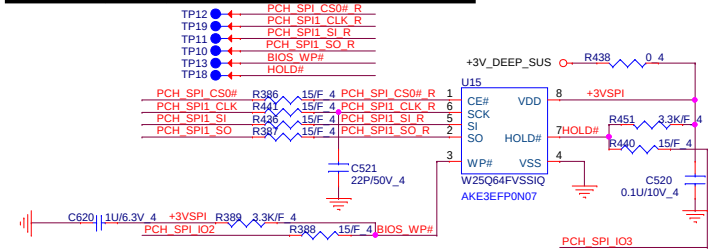
HDA Bus(CLG)



GPIO Pull UP

PCH SPI ROM(CLG)

Vender	Size	P/N
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
Socket		DFHS08FS023



+3V (6,8,9,10,11,12,13,14,15,16,17,18,19,20,21,25,26)
+5V (6,12,14,15,17,18,20,25,26)

+1.05V (4,10,11,20,23,26)
+3VSS (6,9,10,11,18,20,22)
+3VPCU (4,18,19,20,21,22,23,26,27)
+3V_RTC (10,20,21)
+V1.05S_ASATA3PLL (10)

Quanta Computer Inc.
PROJECT : FF6

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	ULT 6/9(SATA/HDA)	A1

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Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)

08

PCI/USBOC# Pull-up(CLG)

DGPU_PWR_EN_R R428 *10K_4 +3V
A20GATE_EC R432 10K_4
PIRQC# R103 10K_4
PIRQD# R423 10K_4
GPIO77_ULT R403 10K_4
GPIO52_ULT R418 10K_4
GPIO53_ULT R416 10K_4
GPIO55_ULT R111 10K_4
DGPU_HOLD_RST# R104 10K_4
DGPU_HOLD_RST# R102 *100K_4
+3V_DEEP_SUS
SMBALERT# R498 10K_4
USB_OC3# R484 10K_4
1210

U19N

C- Link
CL_CLK AF2
CL_DATA AD2
CL_RST# AF4

USB3.0
(19) USB30_RX1- G20 USB3RN1
(19) USB30_RX1+ H20 USB3RP1
(19) USB30_TX1- C33 USB3TN1
(19) USB30_TX1+ B34 USB3TP1
(19) USB30_RX2- E18 USB3RN2
(19) USB30_RX2+ F18 USB3RP2
(19) USB30_TX2- B33 USB3TN2
(19) USB30_TX2+ A33 USB3TP2

PCI
(21) A20GATE_EC
GPIO77_ULT U6 PIRQA# / GPIO77
A20GATE_EC P4 PIRQB# / GPIO78
PIRQC# N4 PIRQC# / GPIO79
PIRQD# N2 PIRQD# / GPIO80
GPIO52_ULT L1 GPIO52
DGPU_PWR_EN_R L3 GPIO54
DGPU_HOLD_RST# R5 GPIO51
GPIO53_ULT L4 GPIO53
GPIO55_ULT U7 GPIO55
TP46 PCI_PME# AD4 PME#

USB
USB2N0 AN8 USBP0- (19) USB2.0(M/B-1)(USBP0)
USB2P0 AM8 USBP0+ (19) USB2.0/USB3.0 COMBO 1st
USB2N1 AR7 USBP1- (15)
USB2P1 AT7 USBP1+ (15) USB2.0 Small board
USB2N2 AR8 USBP2- (20)
USB2P2 AP8 USBP2+ (20) Camera (USBP2)
USB2N3 AR10
USB2P3 AT10
USB2N4 AM15
USB2P4 AL15
USB2N5 AM13 USBP5- (19) USB2.0(M/B-2)(USBP5)
USB2P5 AN13 USBP5+ (19) USB2.0/USB3.0 COMBO 2nd
USB2N6 AP11 USBP6- (20)
USB2P6 AN11 USBP6+ (20) WLAN
USB2N7 AR13 USBP7- (14)
USB2P7 AP13 USBP7+ (14) Touch Screen
R98 0_4 PCIE_IREF B27
R99 3.01K/F_4 PCIE_RCOMP A27
(10) +V1.05S_AUSB3PLL
TIE TRACES TOGETHER CLOSE TO PINS WITH LENGTH TO RESISTOR
USBRBIAS# AJ10 USB_BIAS R140 22.6/F_4 USBRBIAS AJ11
RSVD AN10 RSVD AM10
OC0# / GPIO40(SUS) AL3 USB_OC0# (19)
OC1# / GPIO41(SUS) AT1 USB_OC1# (19)
OC2# / GPIO42(SUS) AH2 USB_OC2# (15)
OC3# / GPIO43(SUS) AV3 USB_OC3# TP100 1210

HSW_ULT_DDR3L

U19K

Cardreader
(17) PCIE_RXN2_CARD F15
(17) PCIE_RXP2_CARD G15
(17) PCIE_TXN2_CARD C192 0.1U/10V_4 PCIE_TXN2_CARD_C B31
(17) PCIE_TXP2_CARD C193 0.1U/10V_4 PCIE_TXP2_CARD_C A31
WLAN
(20) PCIE_RXN3_WLAN G11
(20) PCIE_RXP3_WLAN F11
(20) PCIE_TXN3_WLAN C494 0.1U/10V_4 PCIE_TXN3_WLAN_C C29
(20) PCIE_TXP3_WLAN C493 0.1U/10V_4 PCIE_TXP3_WLAN_C B30
LAN
(16) PCIE_RXN4_LAN F13
(16) PCIE_RXP4_LAN G13
(16) PCIE_TXN4_LAN C496 0.1U/10V_4 PCIE_TXN4_LAN_C B29
(16) PCIE_TXP4_LAN C495 0.1U/10V_4 PCIE_TXP4_LAN_C A29

PCI-E*
PERN1 / USB3RN3 G17
PERP1 / USB3RP3 F17
PETN1 / USB3TN3 C30
PETP1 / USB3TP3 C31
PERN2/ USB3RN4 F15
PERP2/ USB3RP4 G15
PETN2/ USB3TN4 B31
PETP2/ USB3TP4 A31
PERN3 G11
PERP3 F11
PETN3 C29
PETP3 B30
PERN4 F13
PERP4 G13
PETN4 B29
PETP4 A29
PERN5_L0 F10
PERP5_L0 E10
PETN5_L0 C23
PETP5_L0 C22
PERN5_L1 F8
PERP5_L1 E8
PETN5_L1 B23
PETP5_L1 A23
PERN5_L2 H10
PERP5_L2 G10
PETN5_L2 B21
PETP5_L2 C21
PERN5_L3 E6
PERP5_L3 F6
PETN5_L3 B22
PETP5_L3 A21
PCIE_IREF B27
PCIE_RCOMP A27
RSVD E15
RSVD E13

SMBUS
SMBALERT# / GPIO11(SUS) AN2 SMBALERT#
SMBCLK AP2 SMB_PCH_CLK
SMBDATA AH1 SMB_PCH_DAT
SML0ALERT# / GPIO60(SUS) AL2 SML0ALERT#
SML0CLK AN1 SMB_ME0_CLK
SML0DATA AK1 SMB_ME0_DAT
SML1ALERT# / PCHHOT# / GPIO73(SUS) AU4 SML1ALERT# TP68
SML1CLK / GPIO75(SUS) AU3 SMB_ME1_CLK SMB_ME1_CLK (21)
SML1DATA / GPIO74(SUS) AH3 SMB_ME1_DAT SMB_ME1_DAT (21)

CLOCK SIGNALS
CLKOUT_PCIE0N C43
CLKOUT_PCIE0P C42
PCIE_CLKREQ0# U2 PCIECLKRQ0# / GPIO18
Cardreader (17) CLK_PCIE_CRN B41 CLKOUT_PCIE_N1
(17) CLK_PCIE_CRP A41 CLKOUT_PCIE_P1
(17) PCIE_CLKREQ_CR# Y5 PCIECLKRQ1# / GPIO19
WLAN (20) CLK_PCIE_WLANN C41 CLKOUT_PCIE_N2
(20) CLK_PCIE_WLANP B42 CLKOUT_PCIE_P2
(20) PCIE_CLKREQ_WLAN# AD1 PCIECLKRQ2# / GPIO20
LAN (16) CLK_PCIE_LANN B38 CLKOUT_PCIE_N3
(16) CLK_PCIE_LANP C37 CLKOUT_PCI_P3
(16) PCIE_CLKREQ_LAN# N1 PCIECLKRQ3# / GPIO21
A39 CLKOUT_PCIE_N4
B39 CLKOUT_PCIE_P4
PCIE_CLKREQ4# U5 PCIECLKRQ4# / GPIO22
1212
B37 CLKOUT_PCIE_N5
A37 CLKOUT_PCIE_P5
PCIE_CLKREQ5# T2 PCIECLKRQ5# / GPIO23

HSW_ULT_DDR3L

AN2 SMBALERT#
AP2 SMB_PCH_CLK
AH1 SMB_PCH_DAT
AL2 SML0ALERT#
AN1 SMB_ME0_CLK
AK1 SMB_ME0_DAT
AU4 SML1ALERT# TP68
AU3 SMB_ME1_CLK SMB_ME1_CLK (21)
AH3 SMB_ME1_DAT SMB_ME1_DAT (21)
R369 0_4 TP82 PCH_XTAL24_IN (20)
C501 *12P/50V_4
XTAL24_IN A25 XTAL24_IN
XTAL24_OUT B25 XTAL24_OUT
R392 *1M_4 *24MHZ +-30PPM Y3
C500 *12P/50V_4
CLKOUT_ITPXDP# B35 CK_XDP_N_R RP1 2 CK_XDP_N (11)
CLKOUT_ITPXDP_P A35 CK_XDP_P_R *0_4P2R_4 4 3 CK_XDP_P (11)
TP81
RP1 install for XDP
EC34 18P/50V_4
AN15 CLK_PCI_EC_R R525 22_4 CLK_OUT_KBC (21)
CLKOUT_LPC_0 AP15 CLK_PCI_LPC_R R524 22_4 CLK_OUT_DEBUG (20)
CLKOUT_LPC_1
EMI(near PCH)
EC33 18P/50V_4
R5103 22_4 CLK_PCI_TPM (18)
EMI(near PCH)
EC44 *18P/50V_4
R384
DIFFCLK_BIASREF C26 XCLK_BIASREF +V1.05S_AXCK_LCPLL (10)
3.01K/F_4
RSVD K21
RSVD M21
TESTLOW_C35 C35 R380 10K/F_4
TESTLOW_C34 C34 R381 10K/F_4
TESTLOW_AK8 AK8 R531 10K/F_4
TESTLOW_AL8 AL8 R141 10K/F_4

SMBus/Pull-up(CLG)

+3V
Q35
+3V R495 4.7K_4 SMB_PCH_DAT
(11,12,13,18) SMB_RUN_DAT
+3V R461 4.7K_4 SMB_PCH_CLK
(11,12,13,18) SMB_RUN_CLK
2N7002BKS

CLK_REQ/Strap Pin(CLG)

+3V
1212
PCIE_CLKREQ4# R5180 10K_4
PCIE_CLKREQ0# R443 10K_4
PCIE_CLKREQ5# R115 10K_4
PCIE_CLKREQ_WLAN# R482 10K_4
PCIE_CLKREQ_LAN# R425 10K_4
PCIE_CLKREQ_CR# R445 10K_4

(6,7,9,10,11,12,13,14,15,16,17,18,19,20,21,25,26) +3V
(6,7,9,10,11) +3V_DEEP_SUS

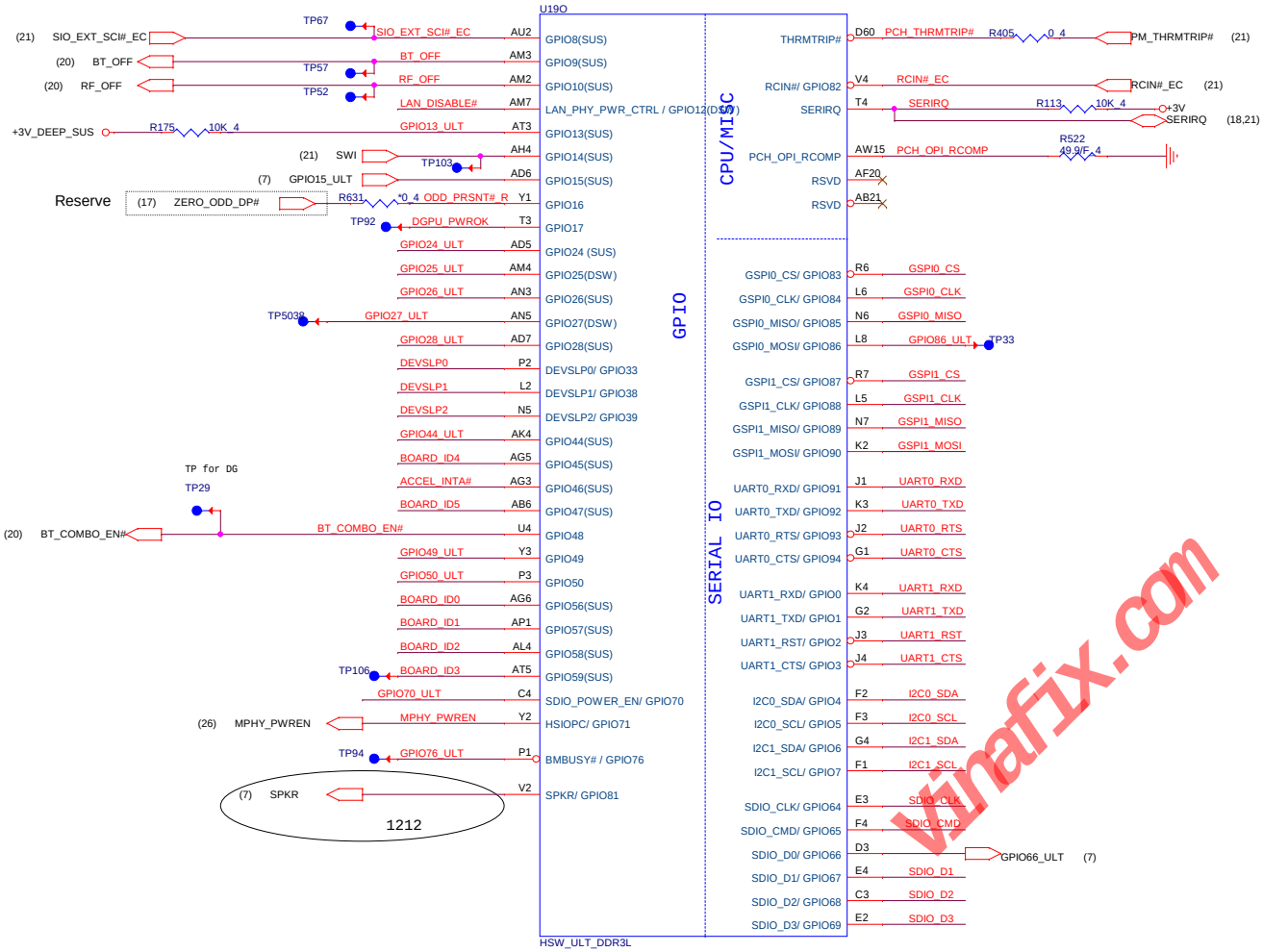
SMBus/Pull-up(CLG)

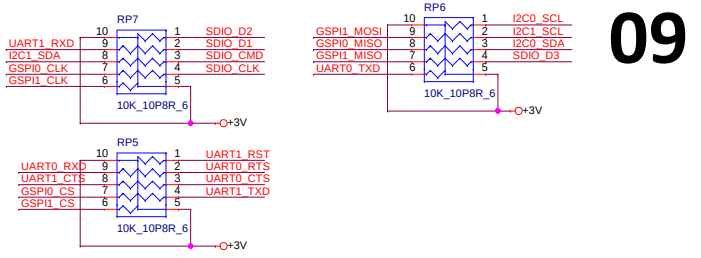
+3V_DEEP_SUS
R499 2.2K_4 SMB_PCH_CLK
R486 2.2K_4 SMB_PCH_DAT
R168 2.2K_4 SMB_ME0_CLK
R493 2.2K_4 SMB_ME0_DAT
R178 2.2K_4 SMB_ME1_CLK
R485 2.2K_4 SMB_ME1_DAT
R179 10K_4 SML1ALERT#
R492 1K_4 SML0ALERT#

Quanta Computer Inc.
PROJECT : FF6
Size | Document Number: ULT 7/9 (PCIE/USB/CLK) | Rev: A1
Date: Thursday, February 13, 2014 | Sheet 8 of 36

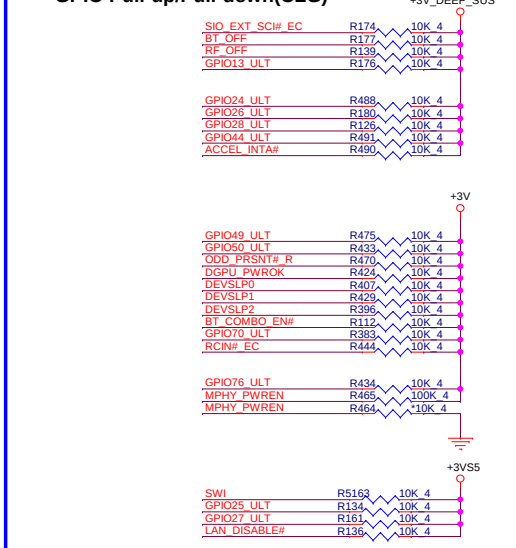
Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA) Haswell (GPIO)

09



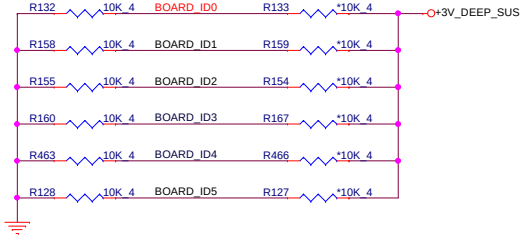


GPIO Pull-up/Pull-down(CLG)



Close to EC

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
Type L(100LAN)	0	0	0	0	0	0
Type H(1G LAN)	0	0	0	0	0	1
	0	0	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0

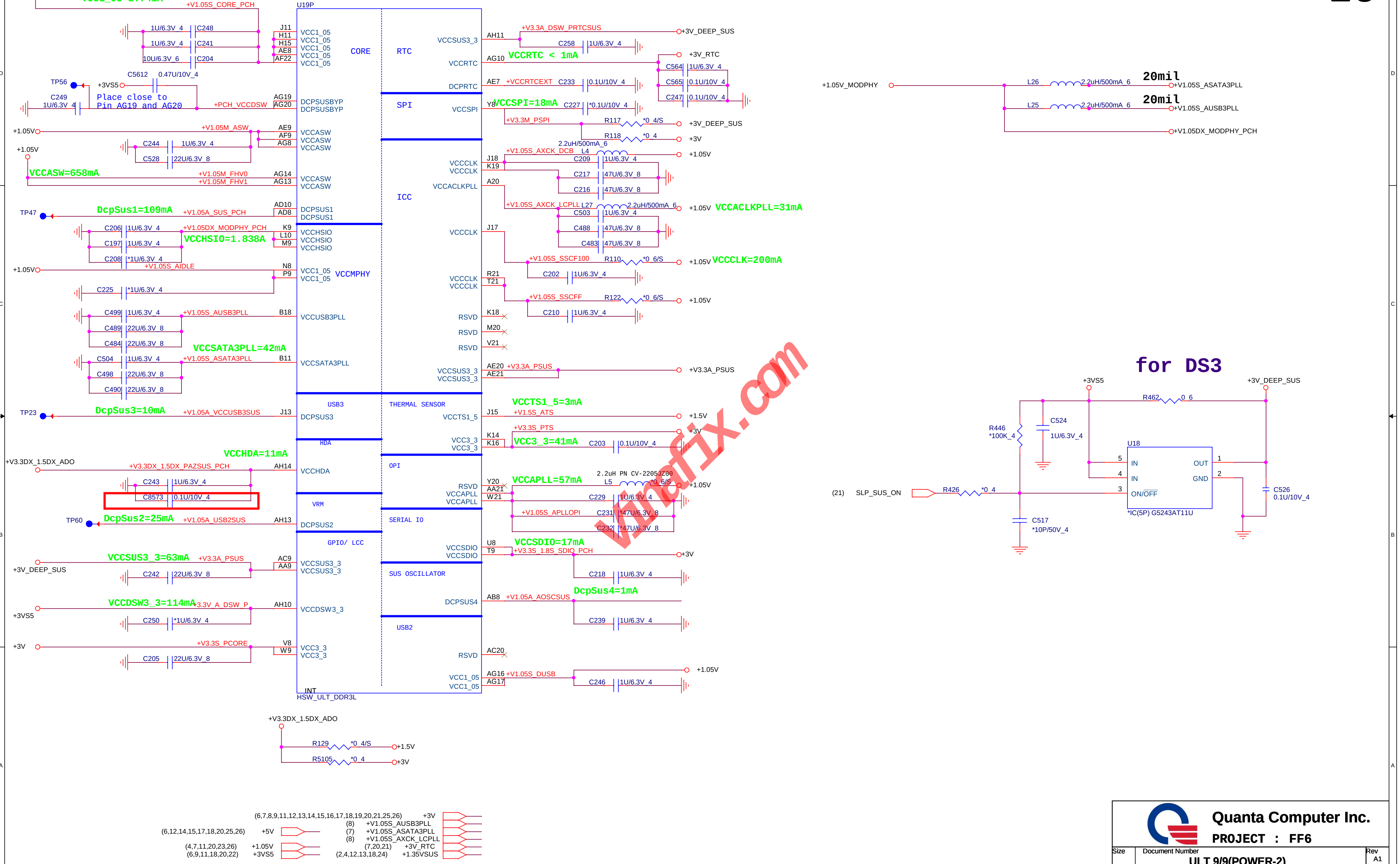


(6,7,8,10,11,12,13,14,15,16,17,18,19,20,21,25,26) +3V
(6,10,11,18,20,22) +3VS5

Quanta Computer Inc.
PROJECT : FF6

Size	Document Number	Rev
	ULT 8/9 (GPIO/MISC)	A1
Date: Thursday, February 13, 2014	Sheet 9 of 36	

Lynx Point-LP Platform Controller Hub
(HDA,JTAG,SATA)(POWER)



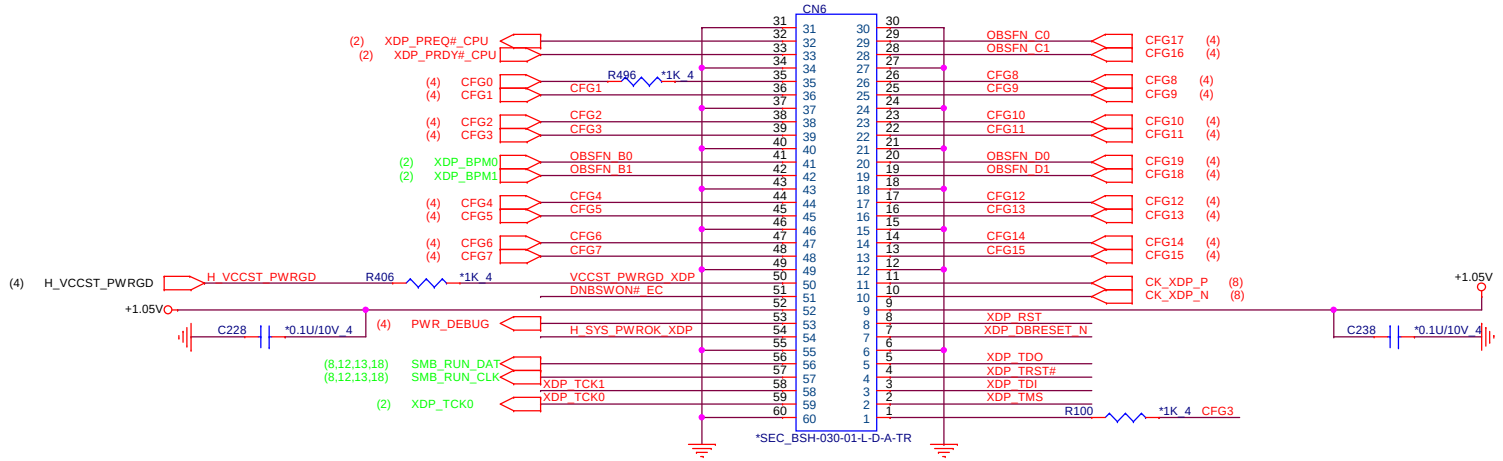
POWER
U19P
CORE
RTC
SPI
ICC
USB3
THERMAL SENSOR
HDA
OPI
VRM
SERIAL IO
GPIO/ LCC
SUS OSCILLATOR
USB2
INT
HSW_ULT_DDR3L
VCC1_05=1.741A
+V1.05S_CORE_PCH
VCCRTC < 1mA
VCCSPI=18mA
VCCASW=658mA
DcpSus1=109mA
VCCHSIO=1.838A
VCCACLKPLL=31mA
VCCCLK=200mA
VCCSATA3PLL=42mA
DcpSus3=10mA
VCCTS1_5=3mA
VCC3_3=41mA
VCCHDA=11mA
VCCAPLL=57mA
DcpSus2=25mA
VCCSDIO=17mA
VCCSUS3_3=63mA
DcpSus4=1mA
VCCDSW3_3=114mA
Place close to
Pin AG19 and AG20
20mil
+1.05V_MODPHY
+V1.05S_ASATA3PLL
+V1.05S_AUSB3PLL
+V1.05DX_MODPHY_PCH
for DS3
+3VS5
+3V_DEEP_SUS
U18
*IC(5P) G5243AT11U
SLP_SUS_ON
+V3.3DX_1.5DX_ADO
+3V
+5V
+1.05V
+V1.05S_AXCK_LCPLL
+3V_RTC
+1.35VSUS

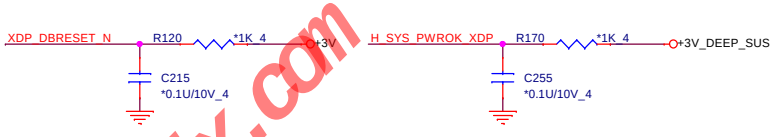
Quanta Computer Inc.

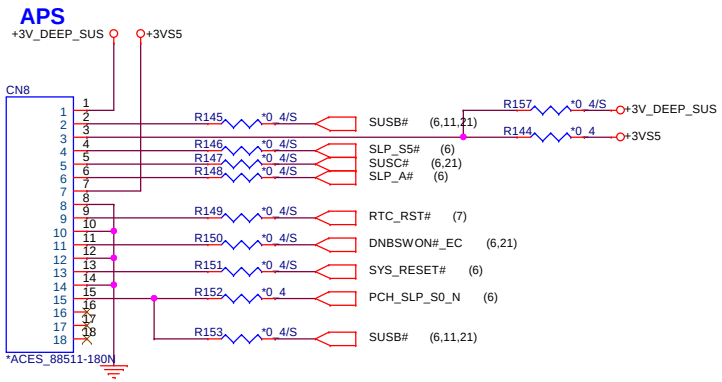
PROJECT : FF6

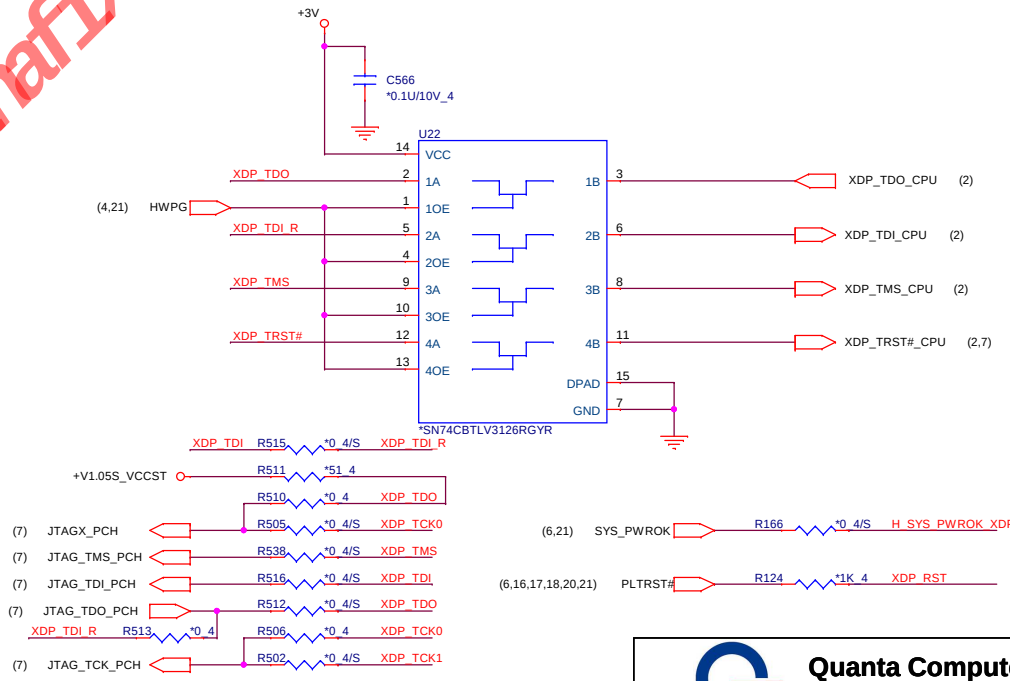
Size	Document Number	Rev
	ULT 9/9(POWER-2)	A1

Date: Thursday, February 13, 2014 Sheet 10 of 36



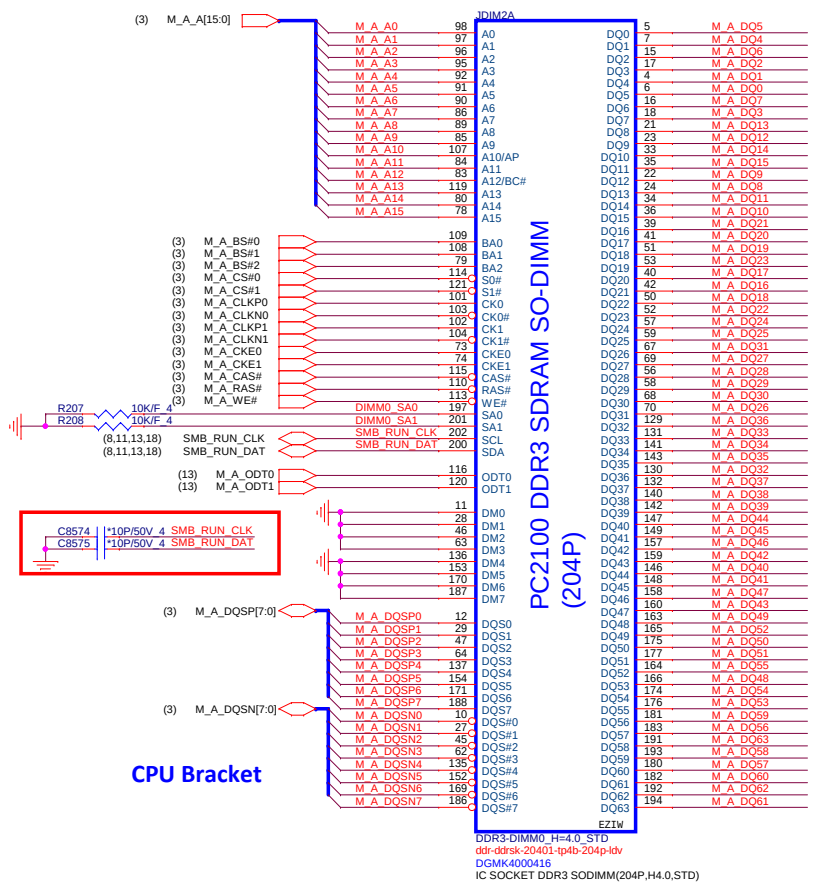


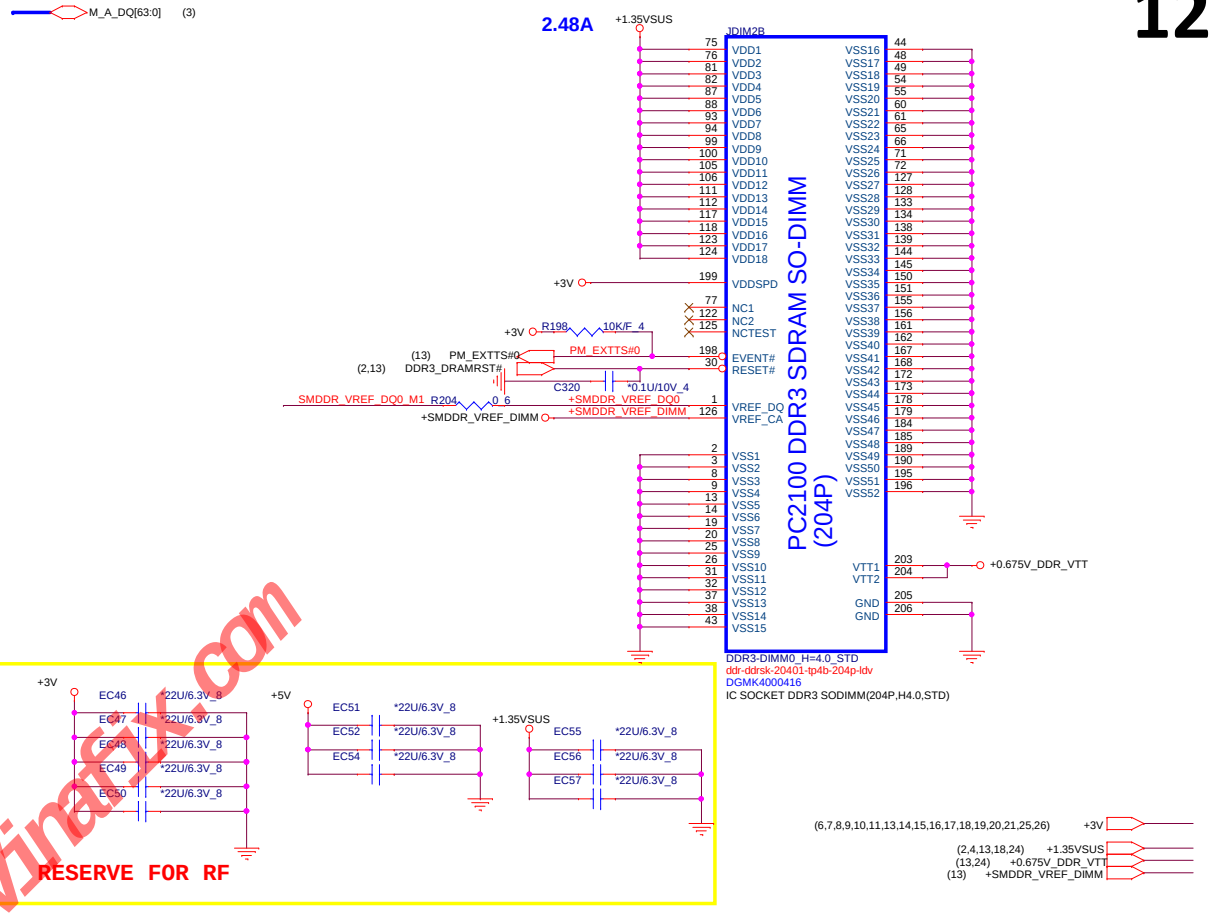


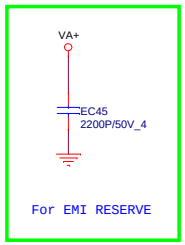


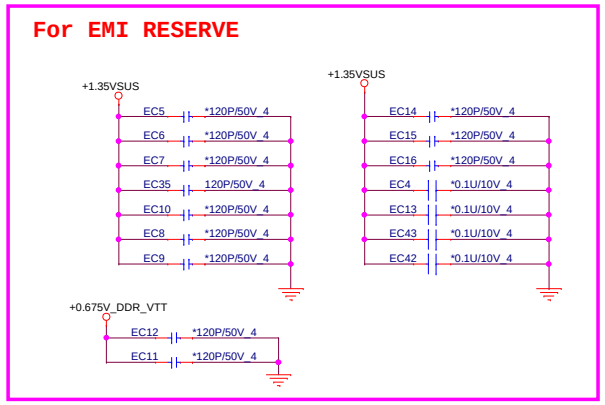
Quanta Computer Inc.
PROJECT : FF6

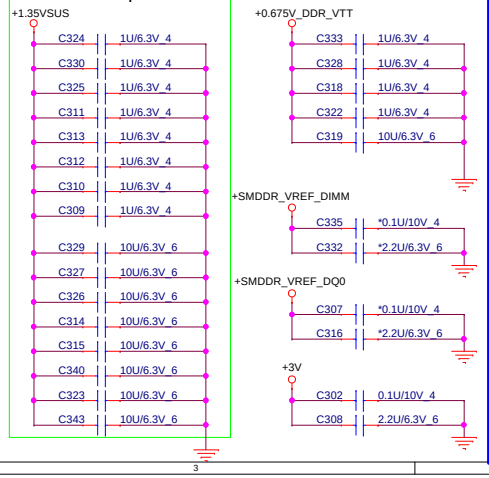
Size	Document Number	Rev
	HSW XDP & APS	A1
Date: Thursday, February 13, 2014	Sheet 11 of 36	

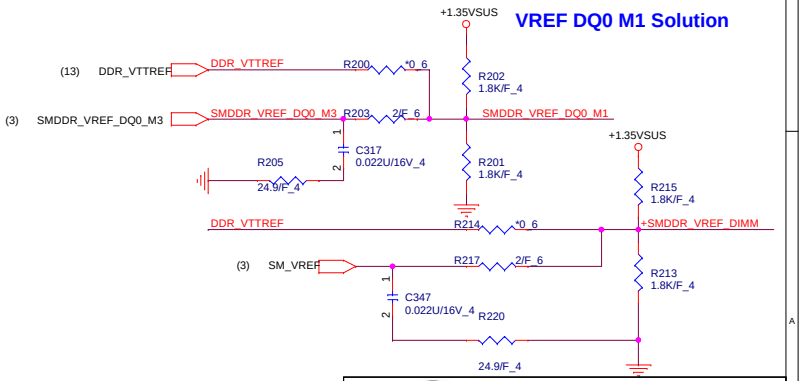




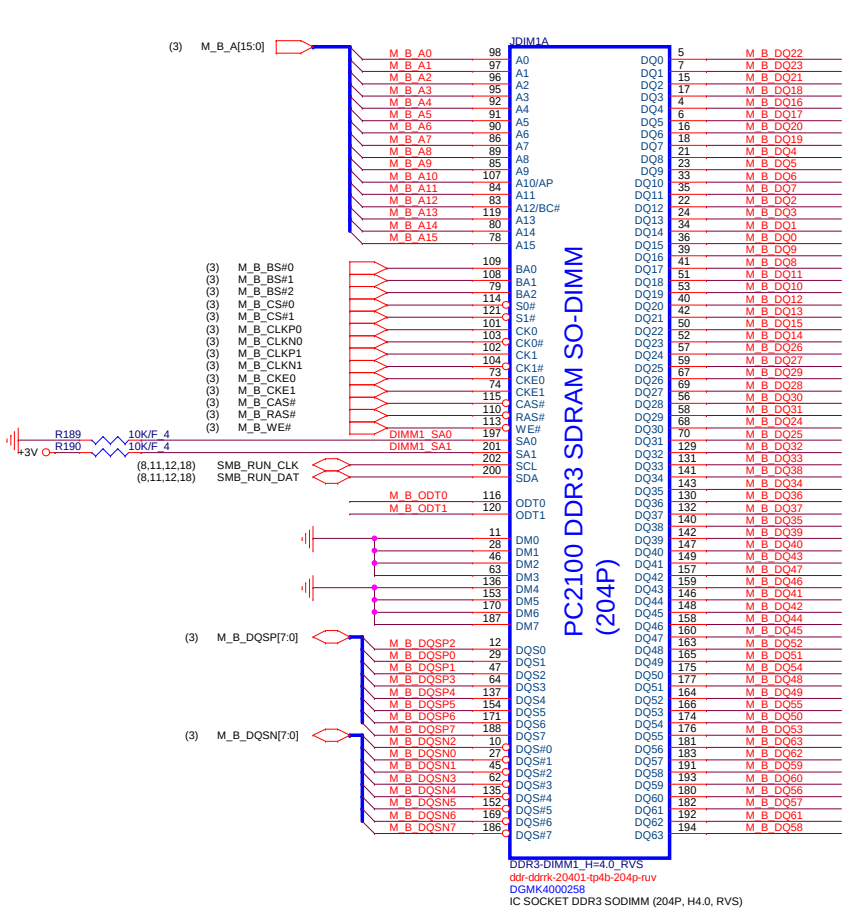


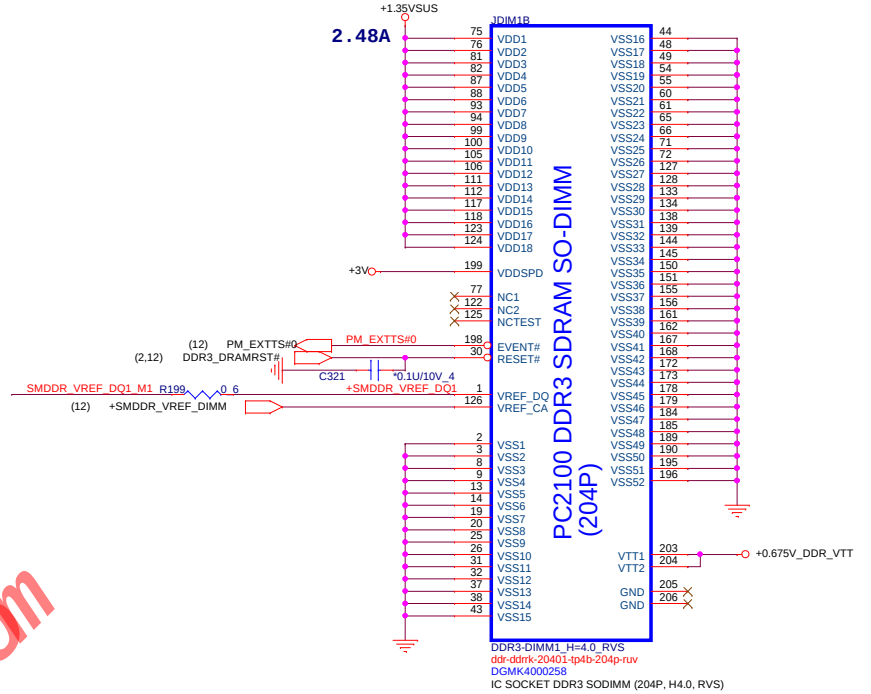




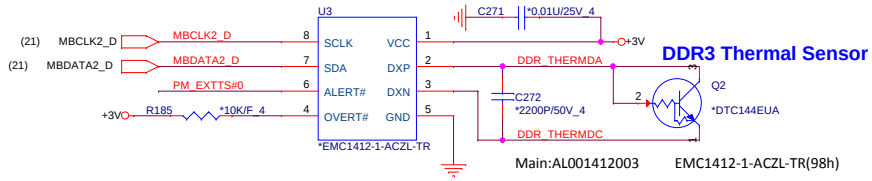


Quanta Computer Inc.		
PROJECT : FF6		
Size	Document Number: DDR3 DIMM0-STD(4.0H)	Rev: A1
Date: Thursday, February 13, 2014	Sheet 12 of 36	



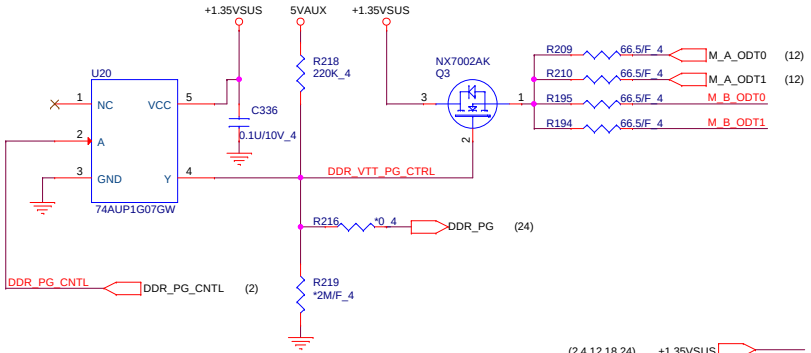


Local Thermal Sensor



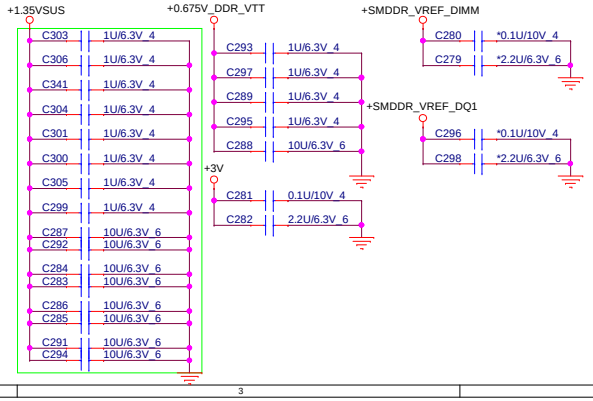
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

DDR3L SODIMM ODT GENERATION

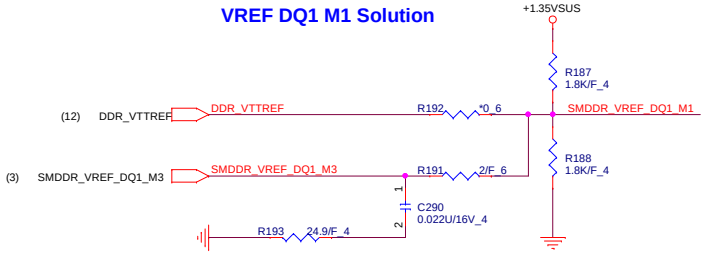


Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector

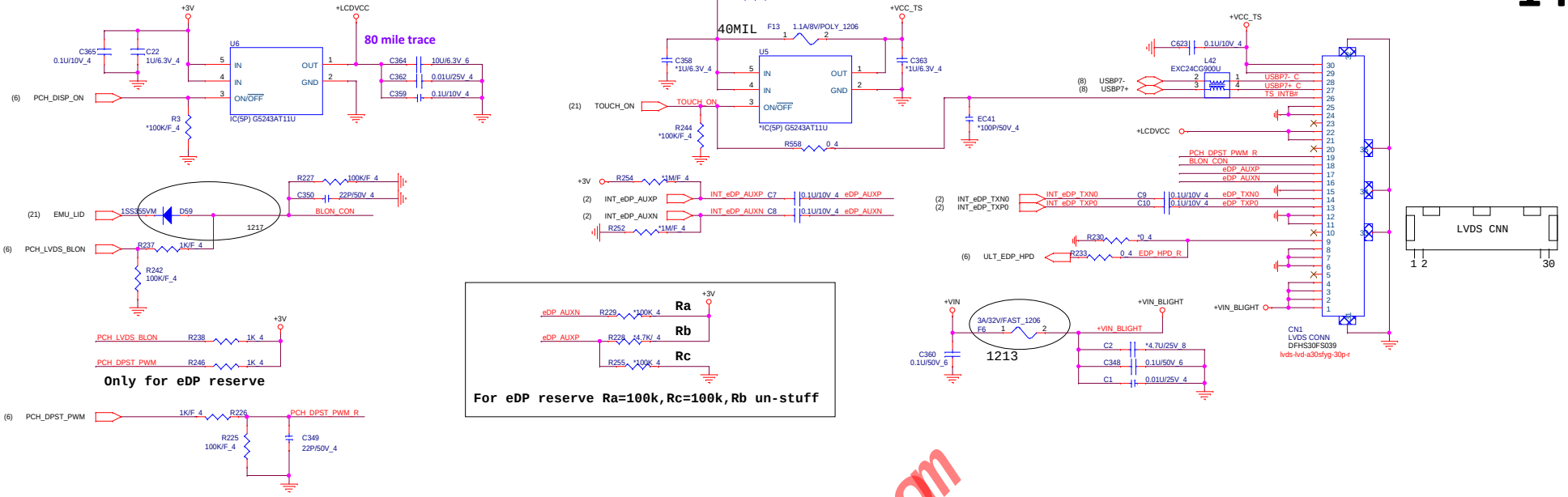


VREF DQ1 M1 Solution

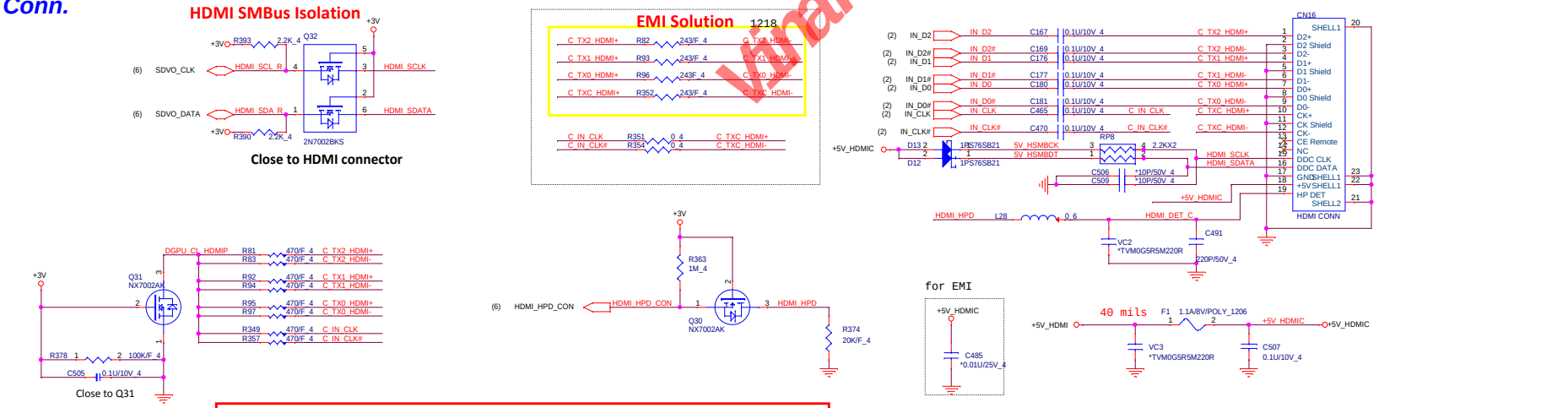


Quanta Computer Inc.	
PROJECT : FF6	
Size	Document Number: DDR3 DIMM1-RVS(4.0H) — Rev: A1
Date: Thursday, February 13, 2014	Sheet 13 of 36

LVDS Conn.

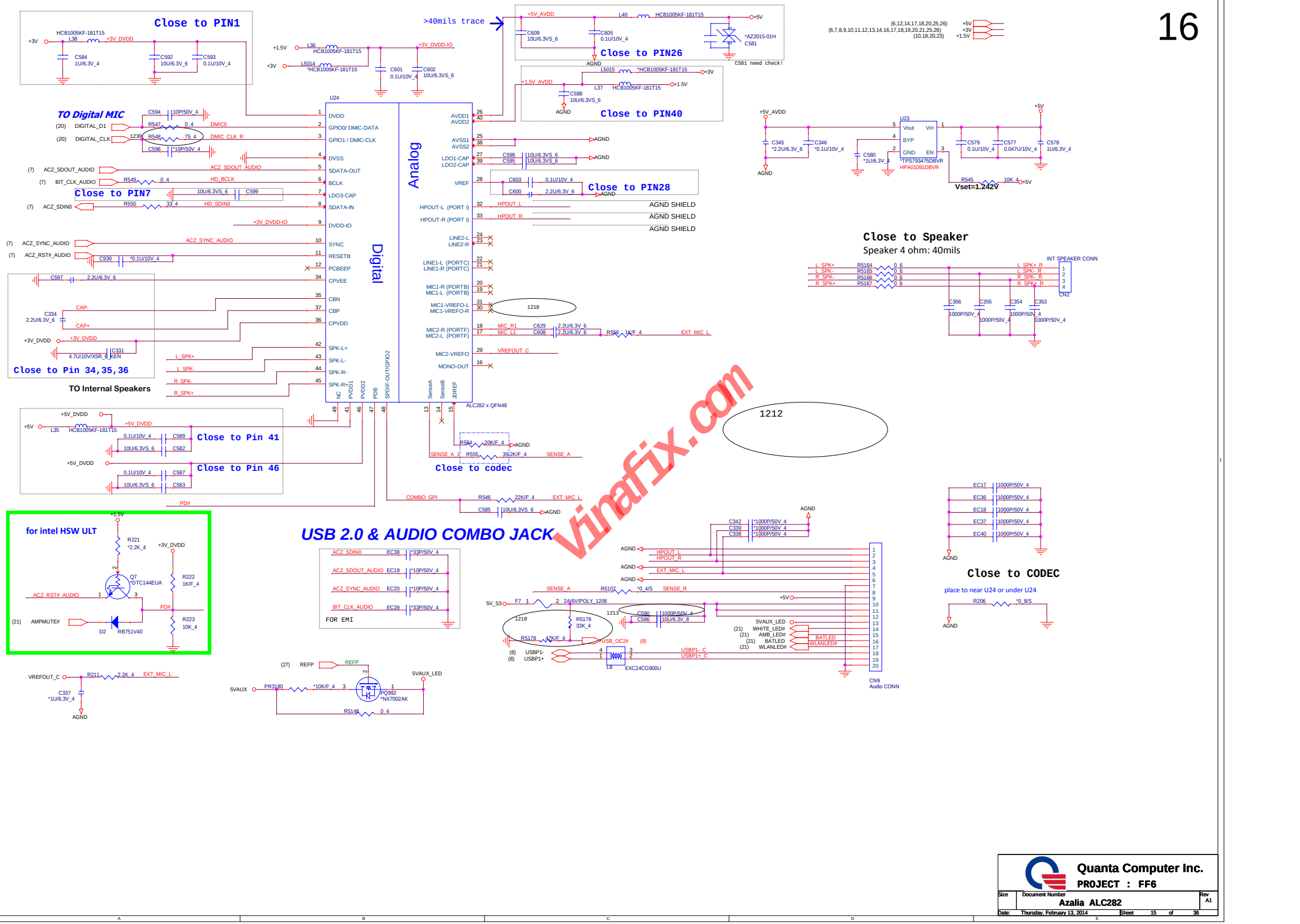


HDMI Conn.



Quanta Computer Inc.
PROJECT : FF6

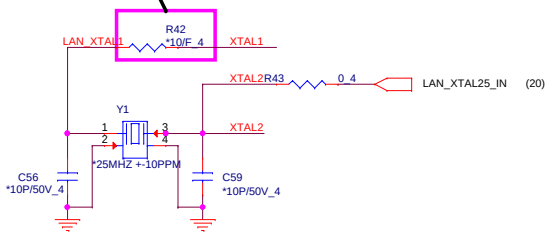
Size	Document Number	Rev
	LCD/HDMI/Camera/D-MIC	A1
Date: Thursday, February 13, 2014	Sheet 14 of 36	



Quanta Computer Inc.			
PROJECT : FF6			
Size	Document Number		Rev
	Azalia ALC282		A1
Date: Thursday, February 13, 2014		Sheet 15 of 36	

(RTL8106E-CG) 10/100
AL008106001
Co-lay
(RTL8111GS-CGT) 10/100/1000
AL008111007

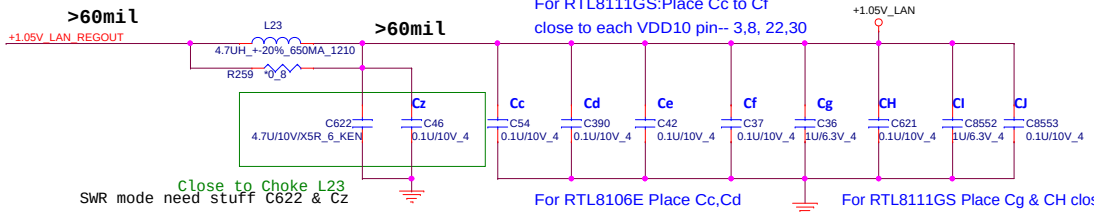
For EMI 0 ~ 22 ohm



Switch Mode:Stuff L23 For RTL8111GS
LDO Mode:Stuff R259 For RTL8111G

Trace<30 mil
Width > 60 mil

Power trace Layout 寬度> 60mil

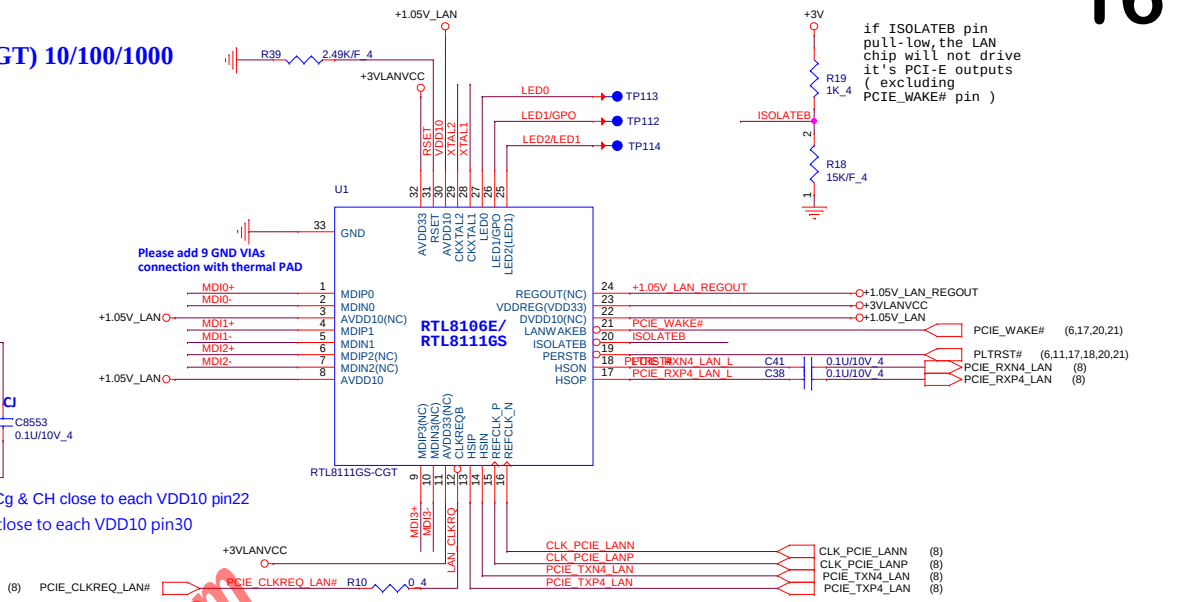


For RTL8111GS:Place Cc to Cf close to each VDD10 pin-- 3,8, 22,30

For RTL8106E Place Cc,Cd close to each VDD10 pin-- 8, 30

For RTL8111GS Place Cg & CH close to each VDD10 pin22

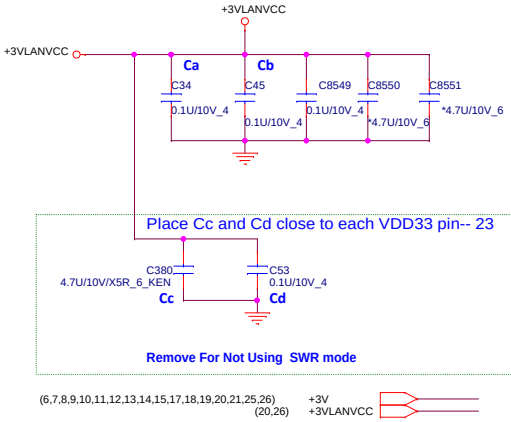
For RTL8106E: CI & CJ close to each VDD10 pin30

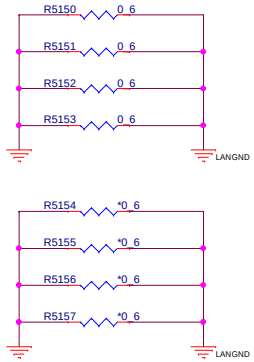


	U1	R5173/R5174 R5175/R5176
10/100 LAN	RTL8106E-CG AL008106001	NC
10/100/1000LAN	RTL8111GS-CG AL008111007	CS00002JB38

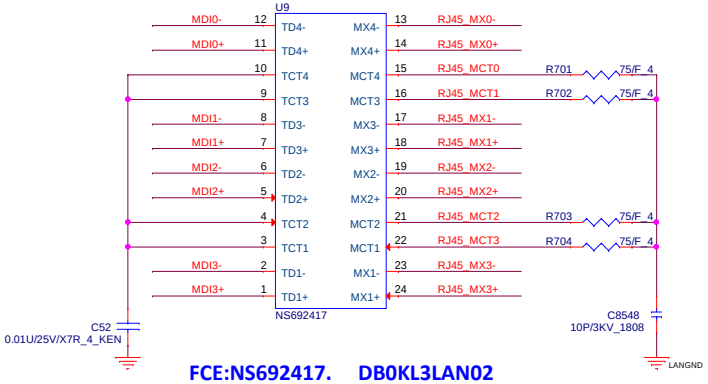
For RTL8111GS :
*Place Ca and Cb close to each VDD33 pin-- 11, 32
*For surge improvement place C8550 and C8551 close to each VDD33 pin-- 11, 32. (optional)

For RTL8106E：Place Cb and C8549 close to each VDD33 pin-- 23, 32



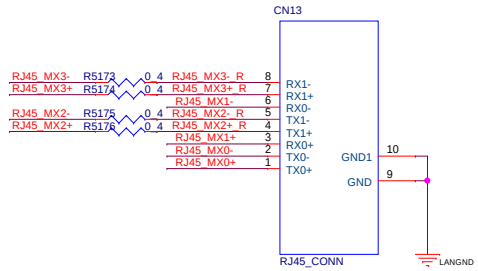


LAN Transformer 10/100/1000



FCE:NS692417. DB0KL3LAN02

RJ45



Quanta Computer Inc.
PROJECT : FF6

Size	Document Number	Rev
	LAN RTL8106EH/8111GS/RJ45	A1
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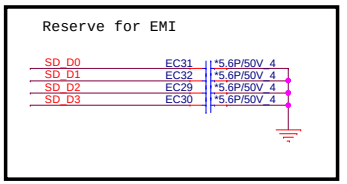
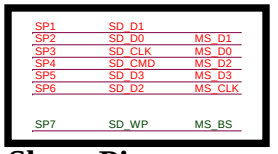
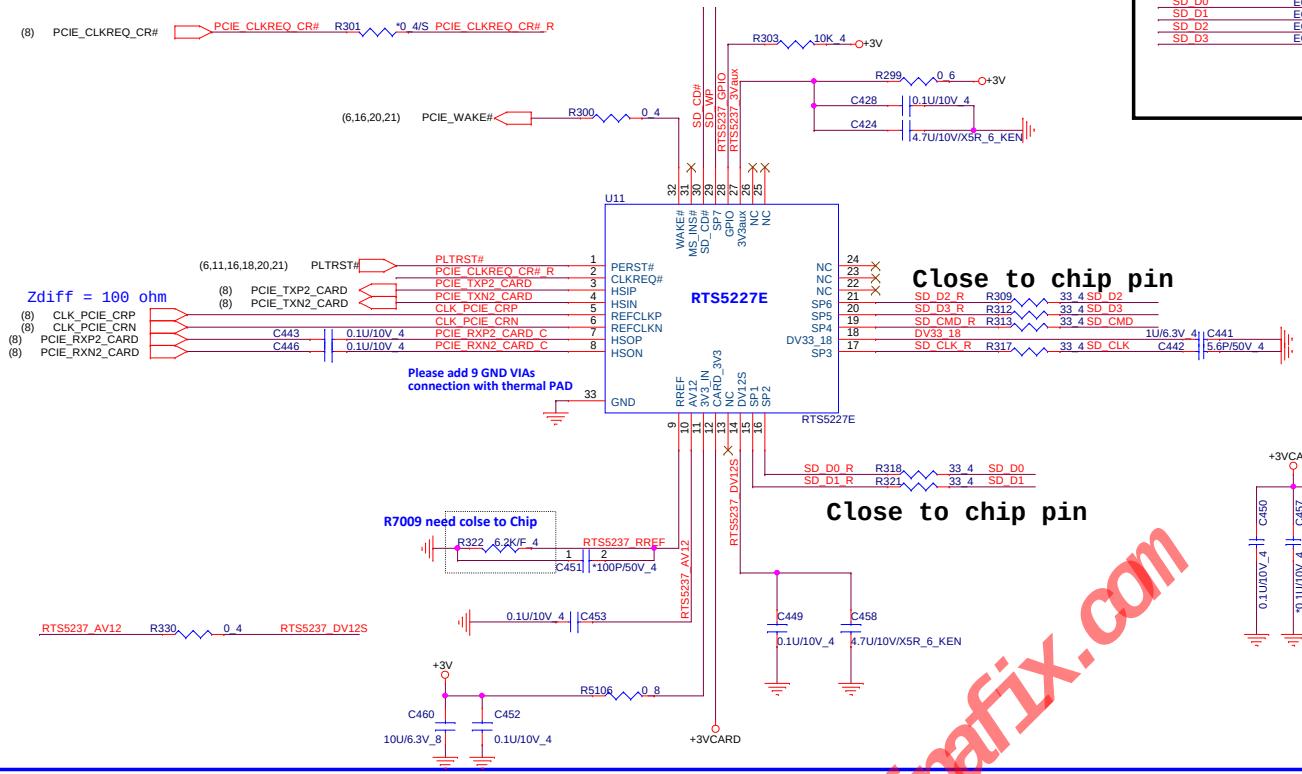
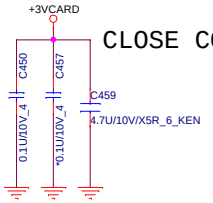




Share Pin

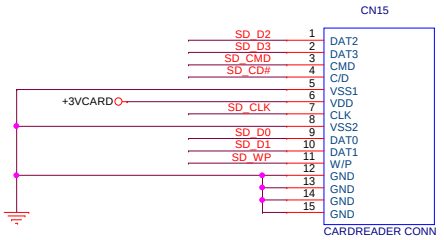
SD / MMC





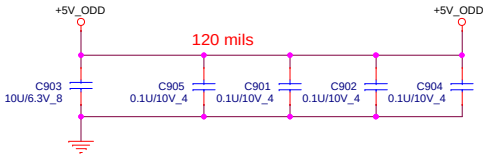
CLOSE CONN

CARD READER

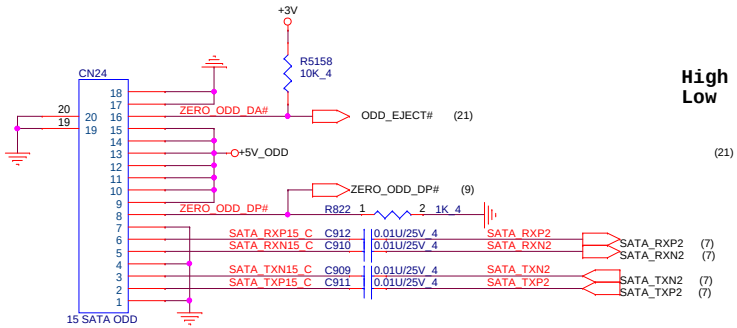


R3X Type

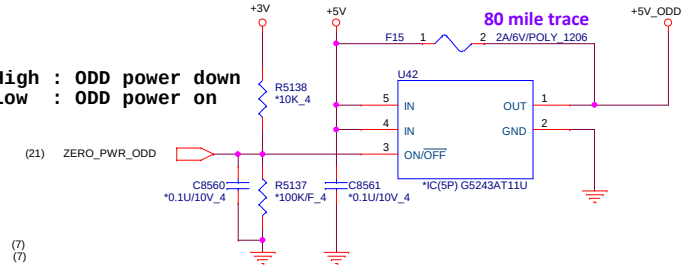
SATA ODD CONNECTOR



15" SATA ODD

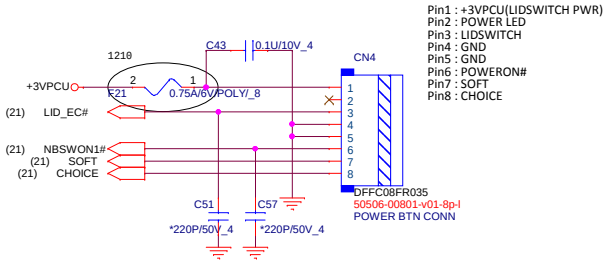


High : ODD power down
Low : ODD power on

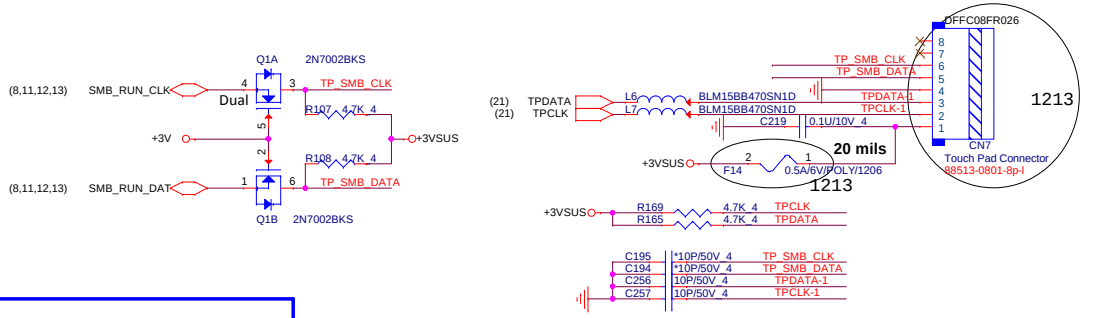


Quanta Computer Inc.		
PROJECT : FF6		
Size	Document Number: CR RTS5227E & CR SOCKET	Rev: A1
Date: Thursday, February 13, 2014	Sheet 17 of 36	

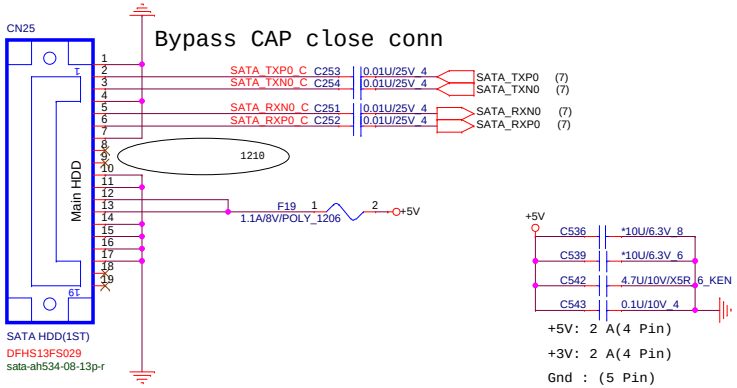
Power Botton Connector



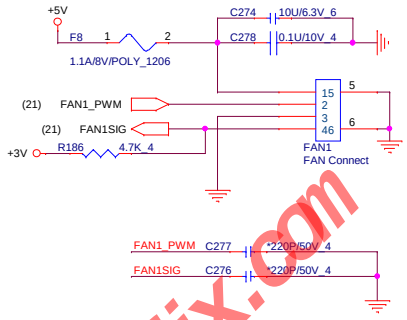
Touch Pad Connector



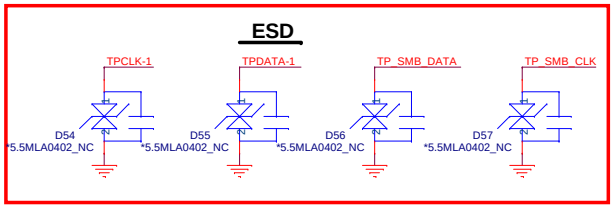
SATA HDD Connector(Cable type)



FAN



ESD



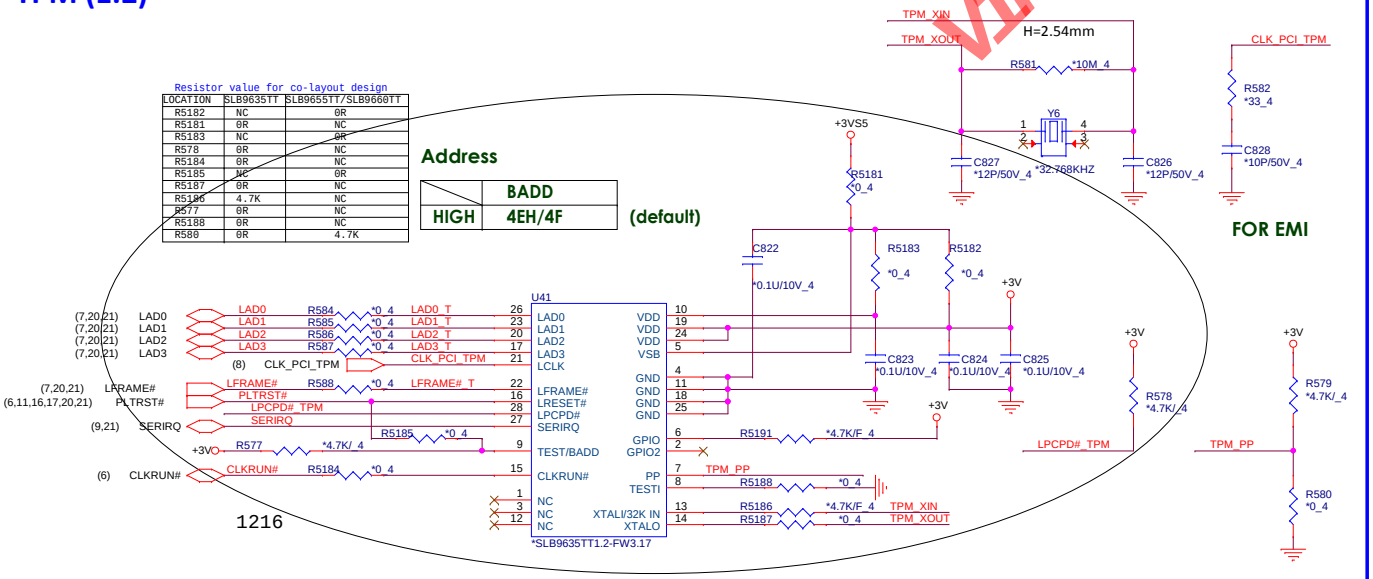
TPM (1.2)

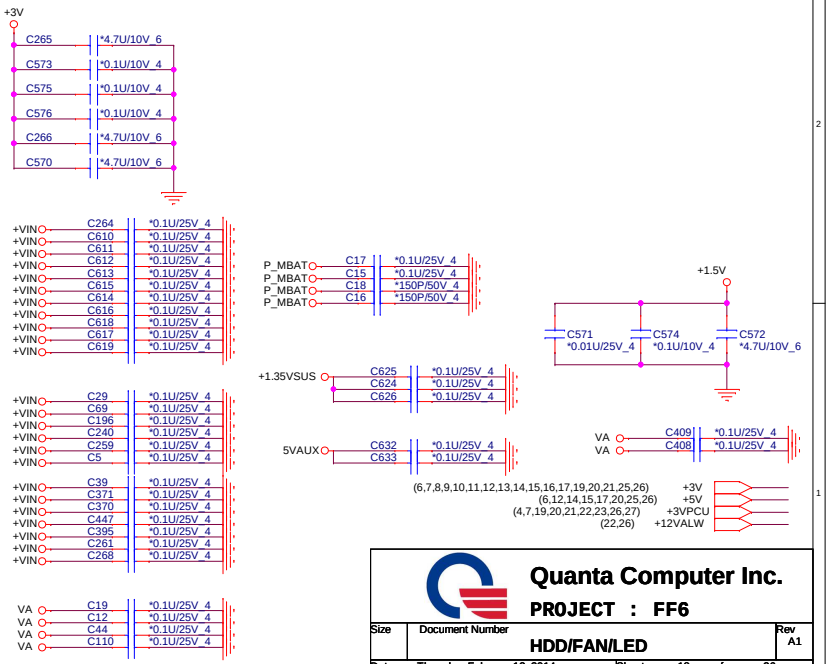
Resistor value for co-layout design

LOCATION	SLB9635TT	SLB9655TT/SLB9660TT
R5182	NC	0R
R5181	0R	NC
R5183	NC	0R
R578	0R	NC
R5184	0R	NC
R5185	NC	0R
R5187	0R	NC
R5186	4.7K	NC
R577	0R	NC
R5188	0R	NC
R580	0R	4.7K

Address

	BADD
HIGH	4EH/4F (default)





Quanta Computer Inc.
PROJECT : FF6

Size	Document Number	Rev
	HDD/FAN/LED	A1
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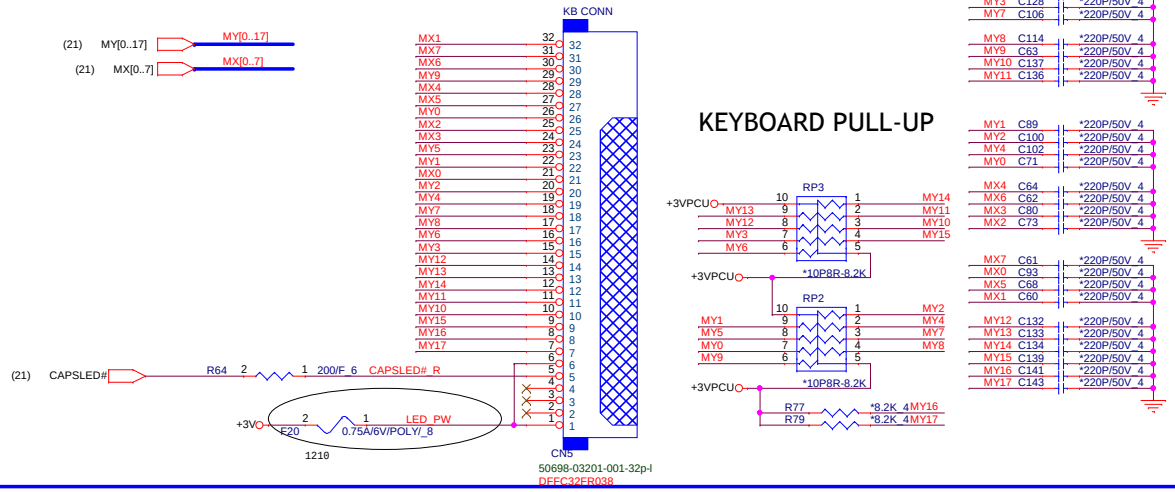
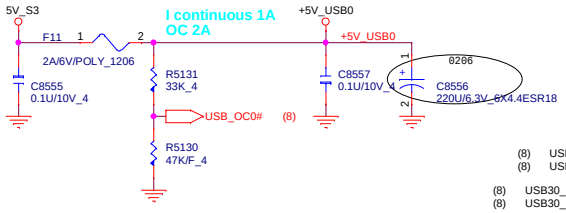
KEYBOARD Con.

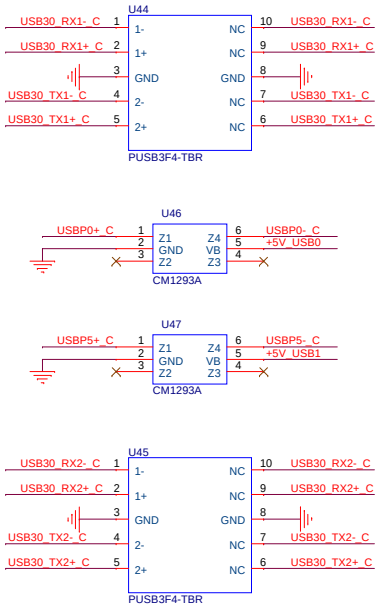


KEYBOARD PULL-UP

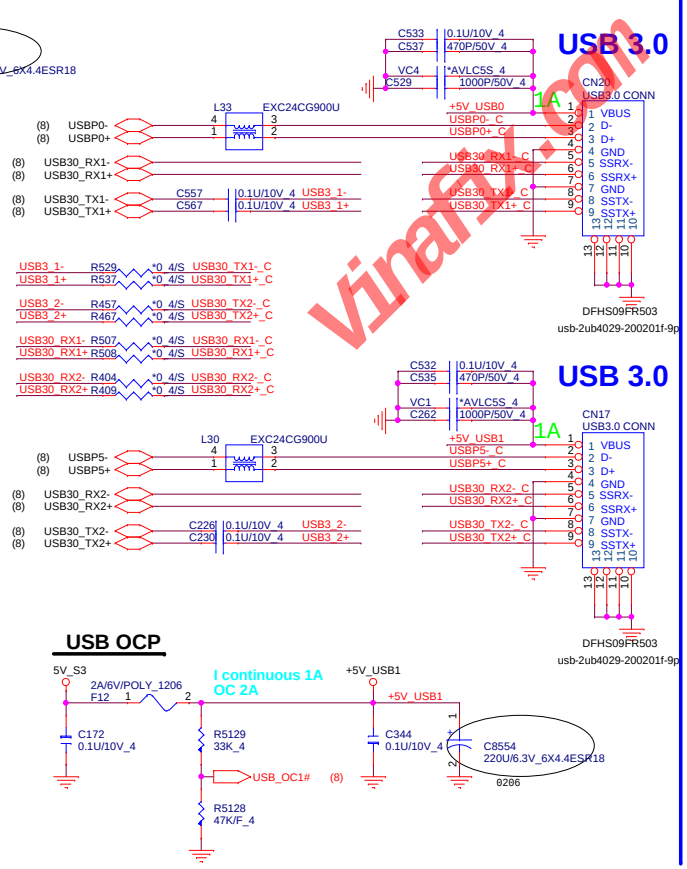
USB OCP



ESD

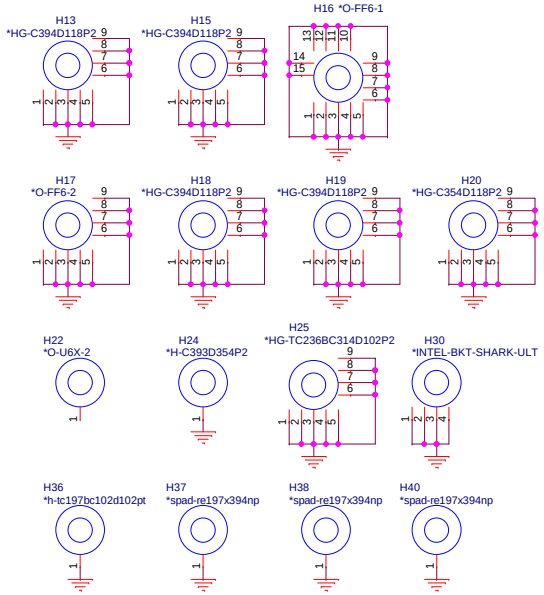


USB 2.0/3.0 Combo

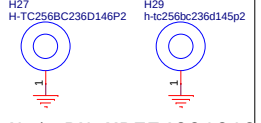


USB OCP

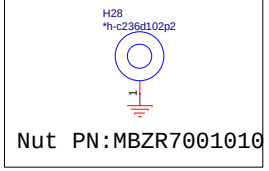
Hole



FAN nut



Mini-PCIe nut



(4,7,18,20,21,22,23,26,27) +3VPCU

Quanta Computer Inc.
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Size	Document Number	Rev
	USB3.0/KB	A1
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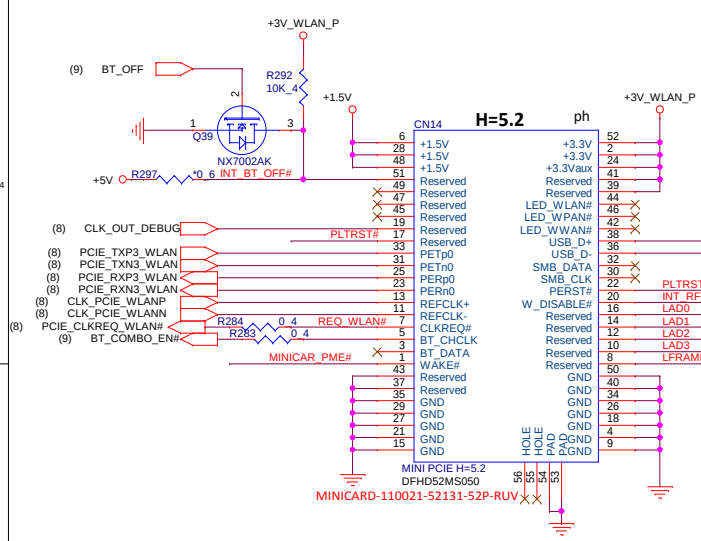
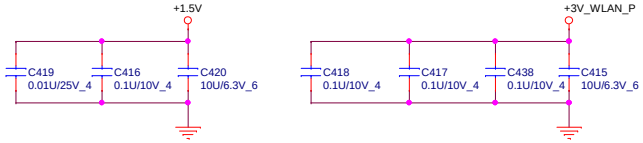
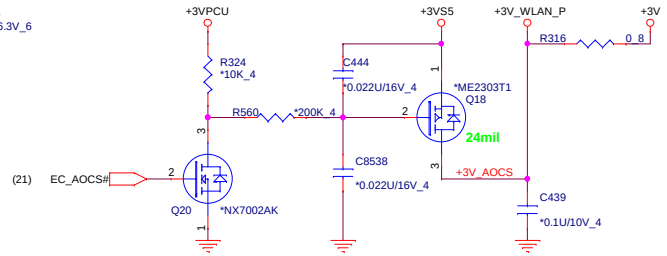
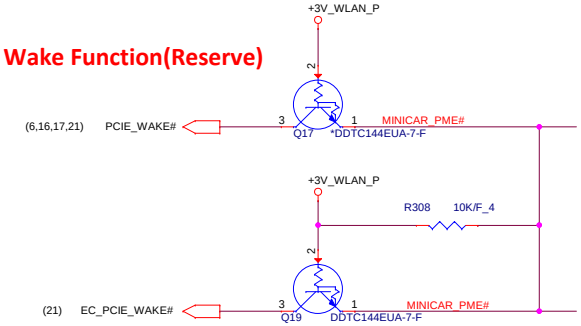


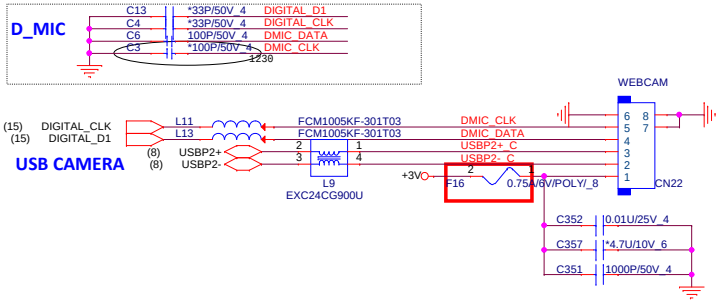


Mini Card WLAN/BT(Option)

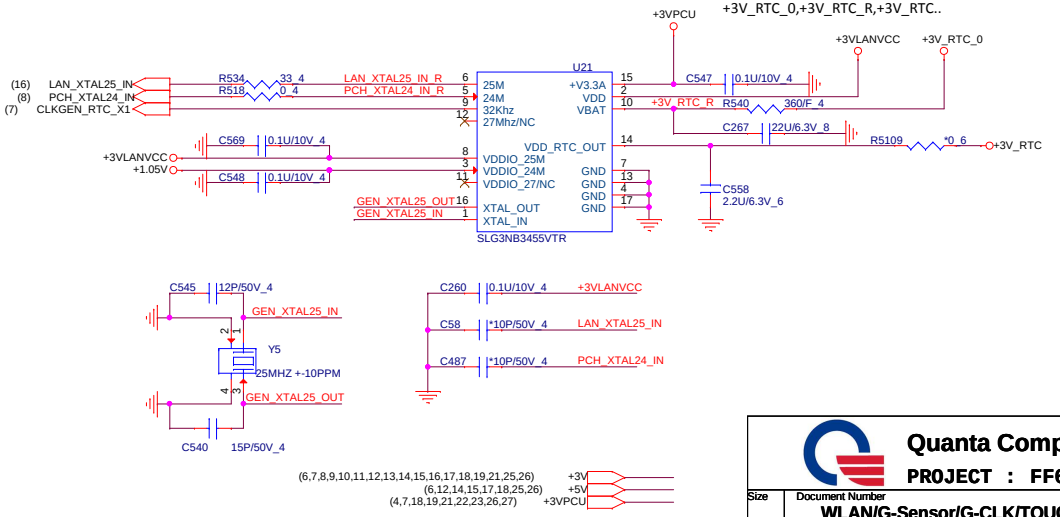


Support Wake Function(Reserve)

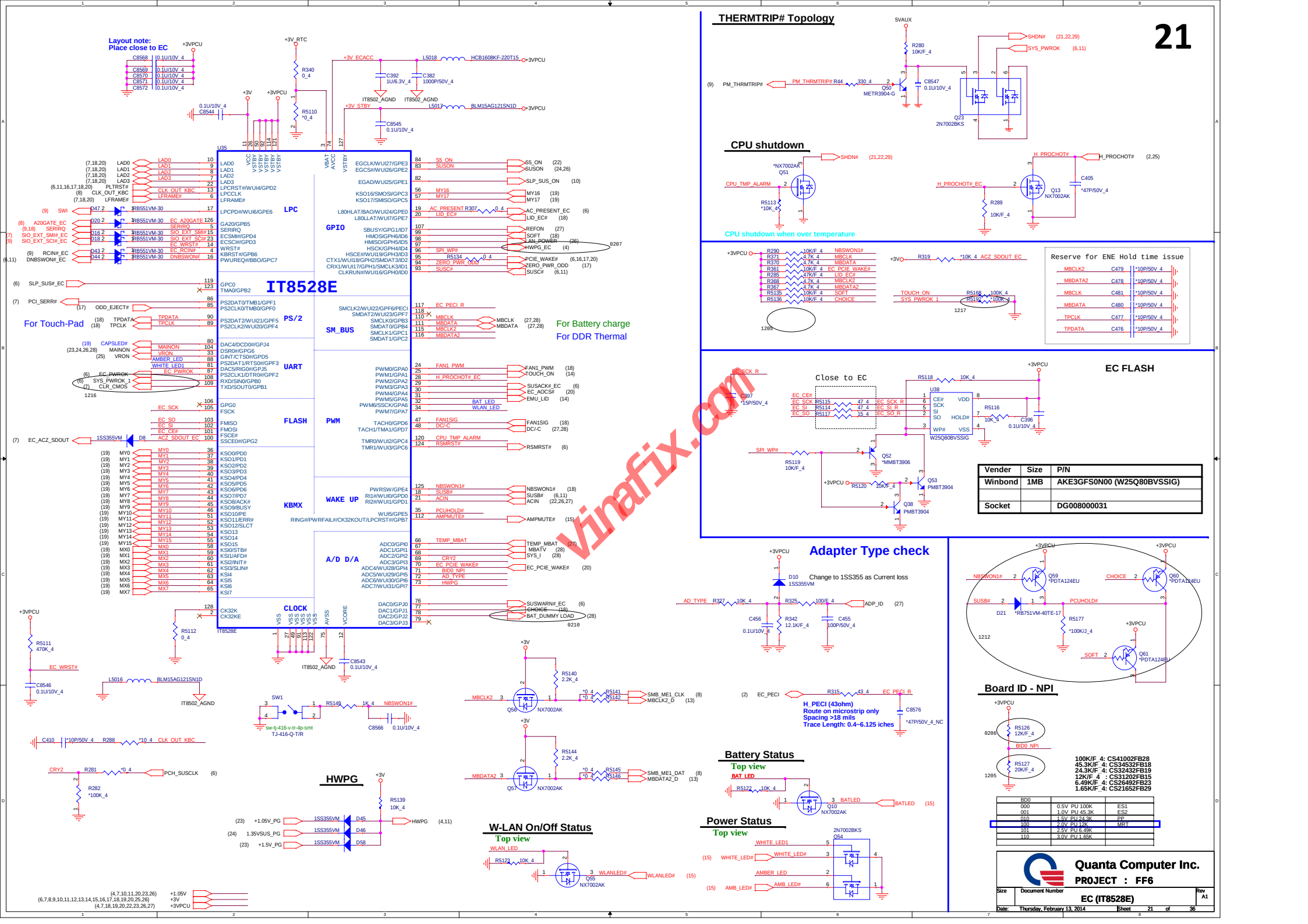




Green CLK Circuitry



Quanta Computer Inc.		
PROJECT : FF6		
Size	Document Number: WLAN/G-Sensor/G-CLK/TOUCH	Rev: A1
Date: Thursday, February 13, 2014	Sheet 20 of 36	



Vender	Size	P/N
Winbond	1MB	AKE3GFS0N00 (W25Q80BVSSIG)
Socket		DG008000031

BD0		
000	0.5V PU 100K	ES1
001	1.0V PU 45.3K	ES2
010	1.5V PU 24.3K	PP
100	2.0V PU 12K	MRT
101	2.5V PU 6.49K	
110	3.0V PU 1.65K	

100K/F 4: CS41002FB28
45.3K/F 4: CS34532FB18
24.3K/F 4: CS32432FB19
12K/F 4 : CS31202FB15
6.49K/F 4: CS26492FB23
1.65K/F 4: CS21652FB29

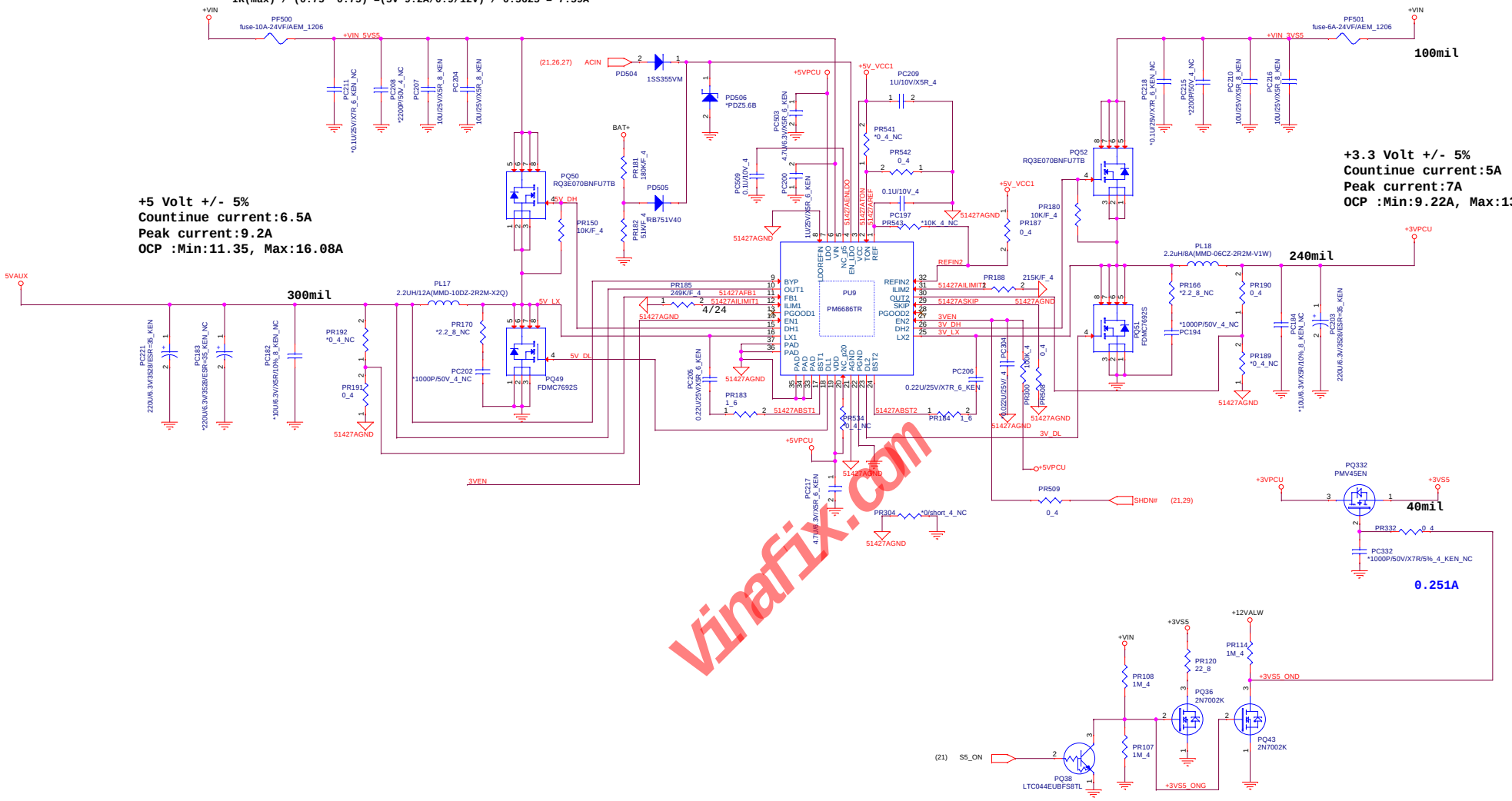
3.3V & 5V

Fuse Rating =
IR(max) / (0.75* 0.75) =(5V*9.2A/0.9/12V) / 0.5625 = 7.59A

Fuse Rating =
IR(max) / (0.75* 0.75) =(3.3V*7A/0.9/12V) / 0.5625 = 3.8A

+5 Volt +/- 5%
Countinue current:6.5A
Peak current:9.2A
OCP :Min:11.35, Max:16.08A

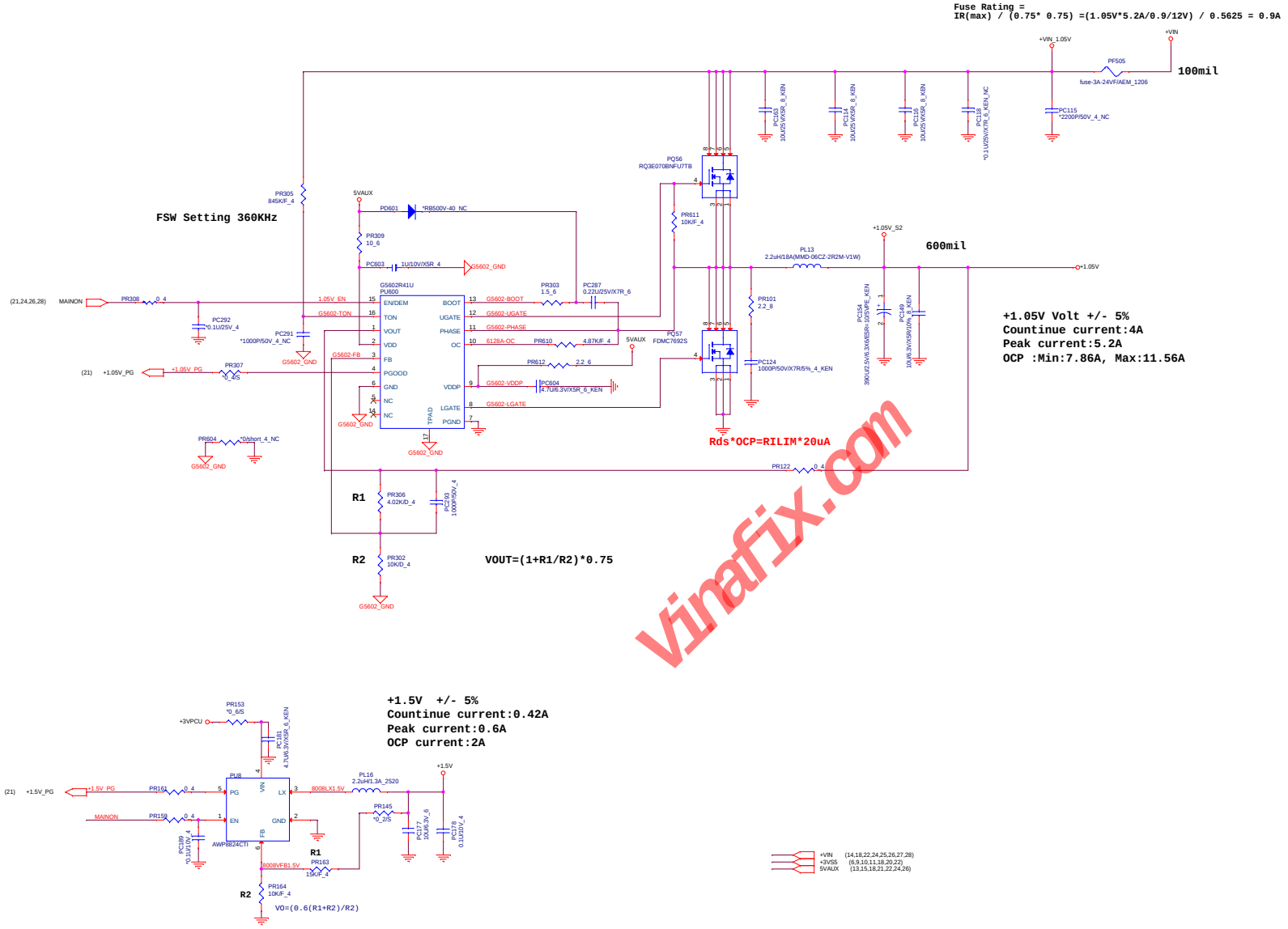
+3.3 Volt +/- 5%
Countinue current:5A
Peak current:7A
OCP :Min:9.22A, Max:13.3A



Quanta Computer Inc.
PROJECT : FF6

Size	Document Number	Rev
	3VPCU&5VPCU(PM6686TR)	A1

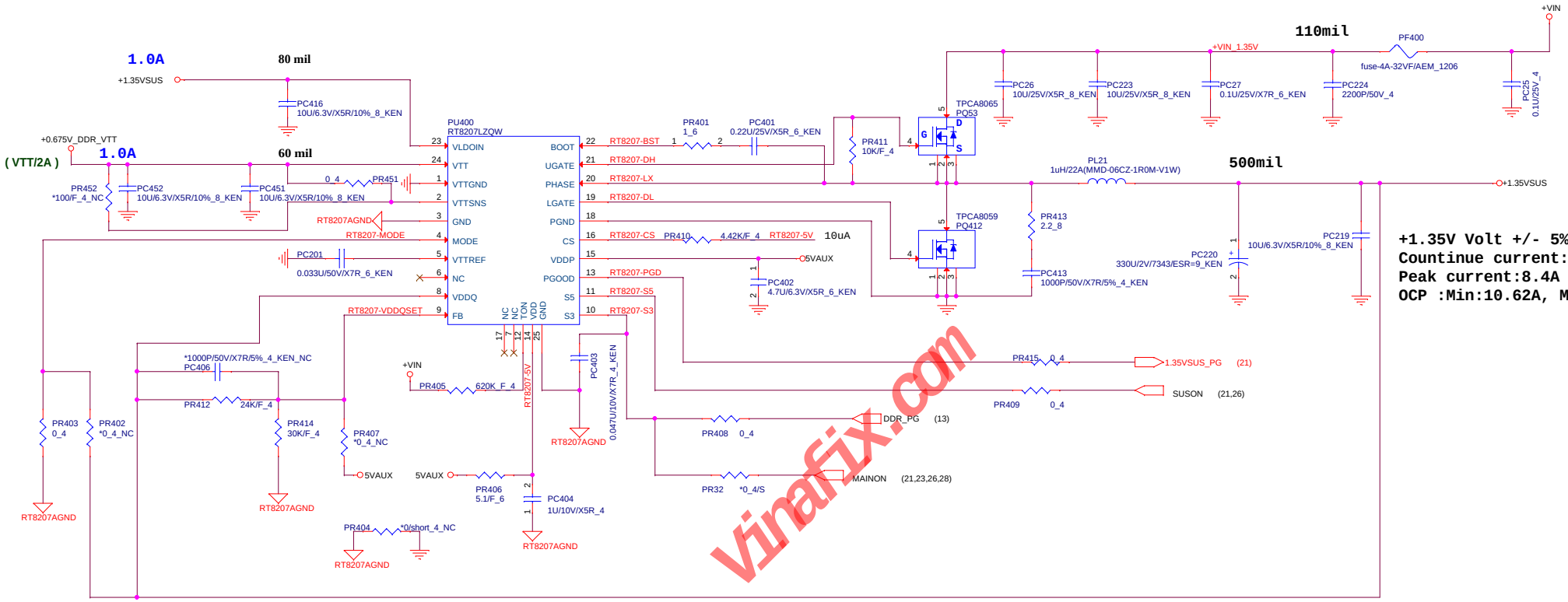
Date: Thursday, February 13, 2014 Sheet 22 of 36



Quanta Computer Inc.		
PROJECT : FF6		
Size	Document Number	Rev
	+1.05V (NB671)/1.5V	A1
Date: Thursday, February 13, 2014	Sheet 23 of 36	

1.35VSUS & VTT_MEM

Fuse Rating =
IR(max) / (0.75* 0.75) =(1.35V*8.4A/0.9/12V)/ 0.5625
= 1.87A



+1.35V Volt +/- 5%
Countinue current:5.9A
Peak current:8.4A
OCP :Min:10.62A, Max:13.25A

Quanta Computer Inc.		
PROJECT : FF6		
Size	Document Number: RT8207LZQW	Rev: A1
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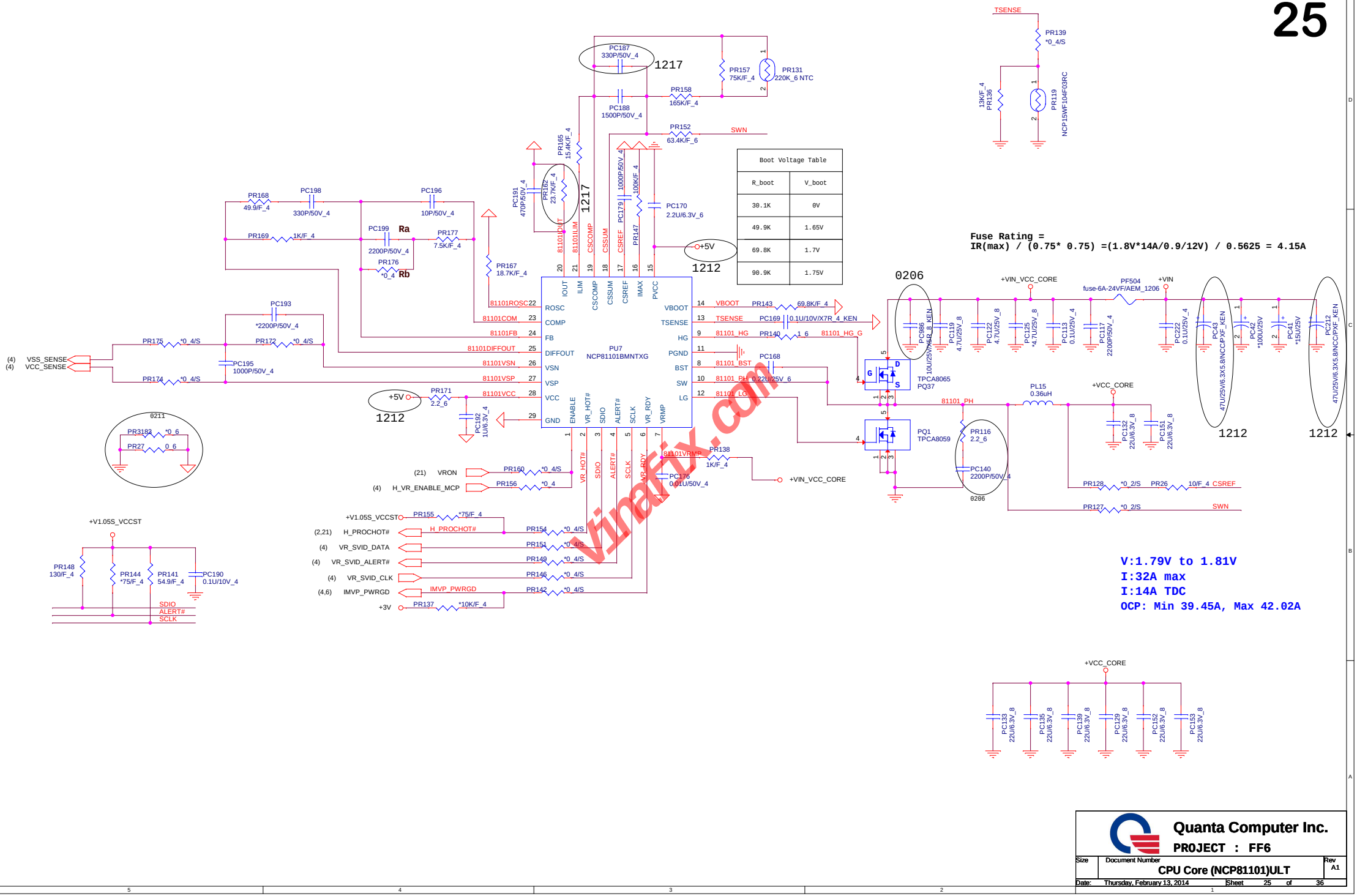
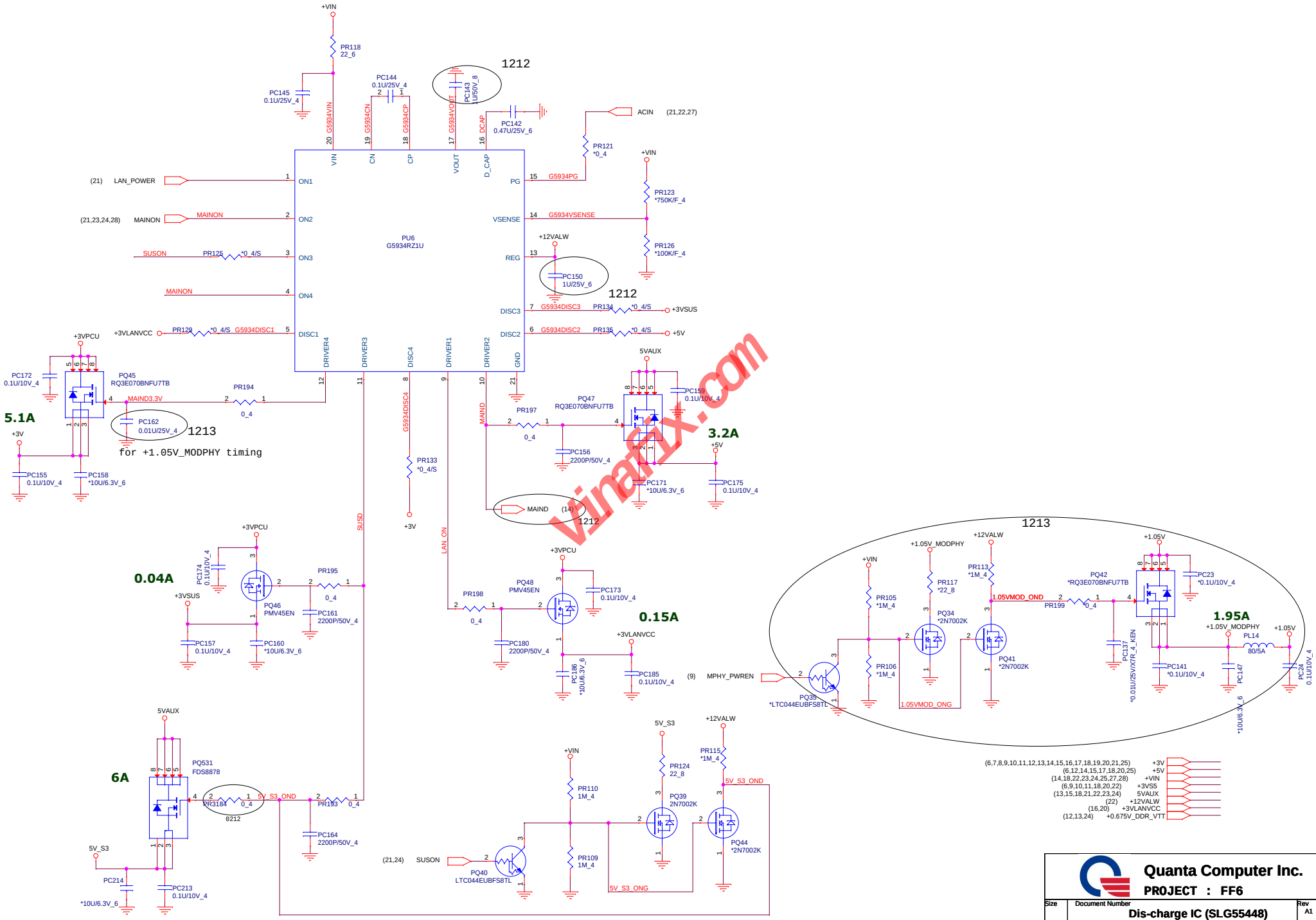
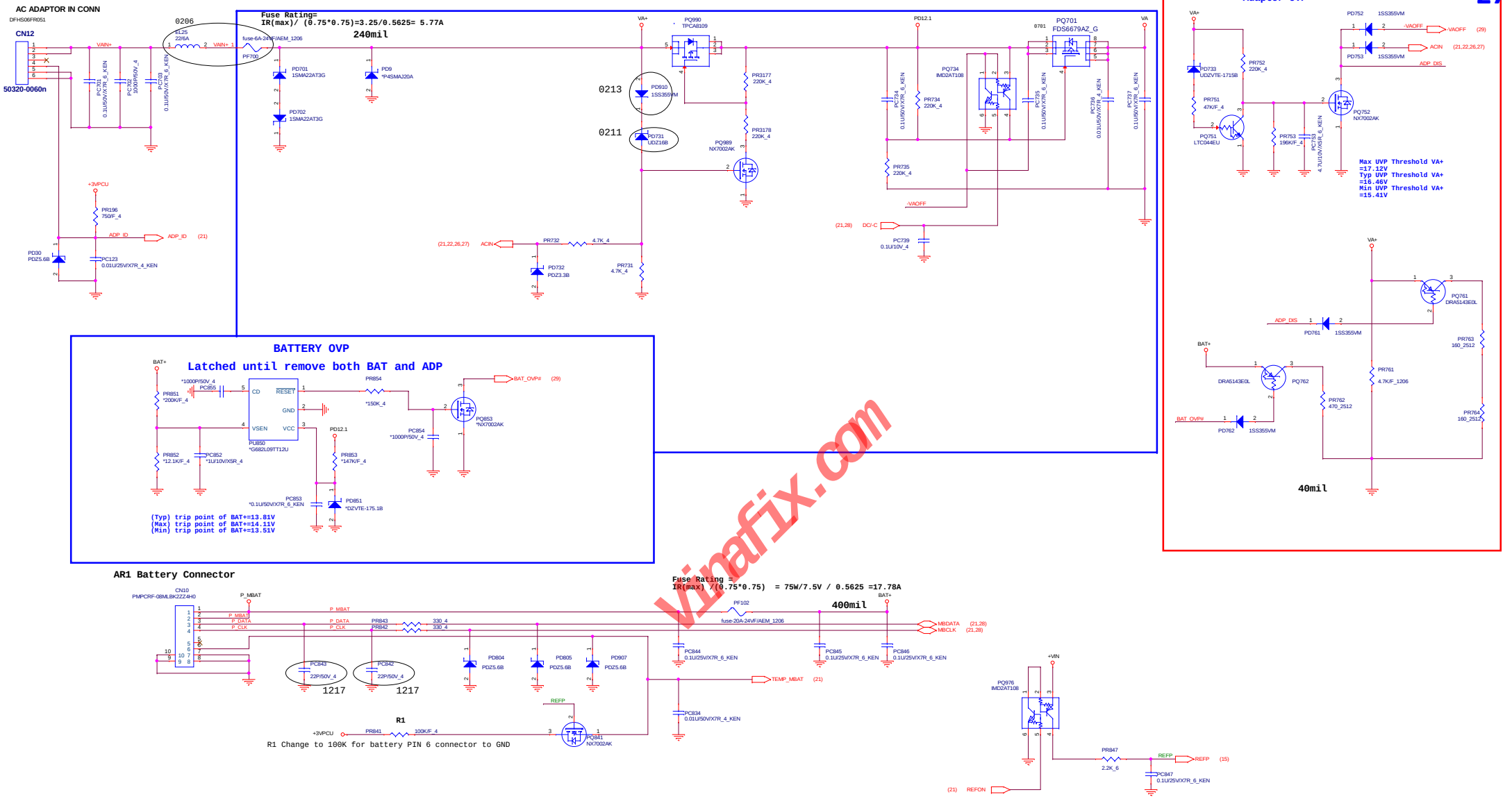


Quanta Computer Inc.	
PROJECT : FF6	
Size	Document Number: CPU Core (NCP81101)ULT — Rev: A1
Date: Thursday, February 13, 2014	Sheet 25 of 36



Quanta Computer Inc.	
PROJECT : FF6	
Size	Document Number: Dis-charge IC (SLG55448) — Rev A1
Date: Thursday, February 13, 2014	Sheet 26 of 36

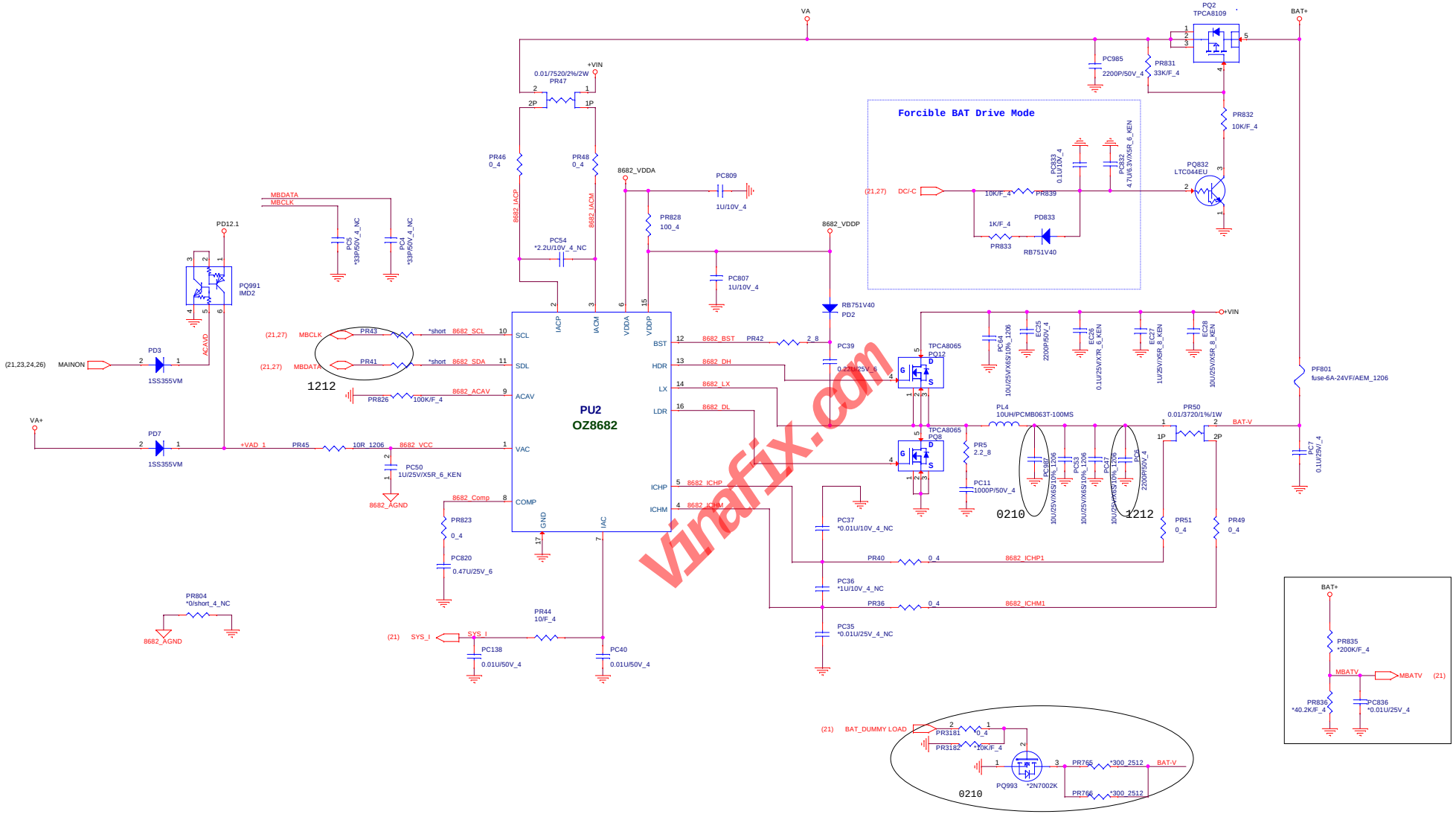


TEMP_MBAT voltage :		
	System Off	System On
Battery	0V	0V
Adapter	3.3V	3.3V
Battery+Adapter	0V	0V

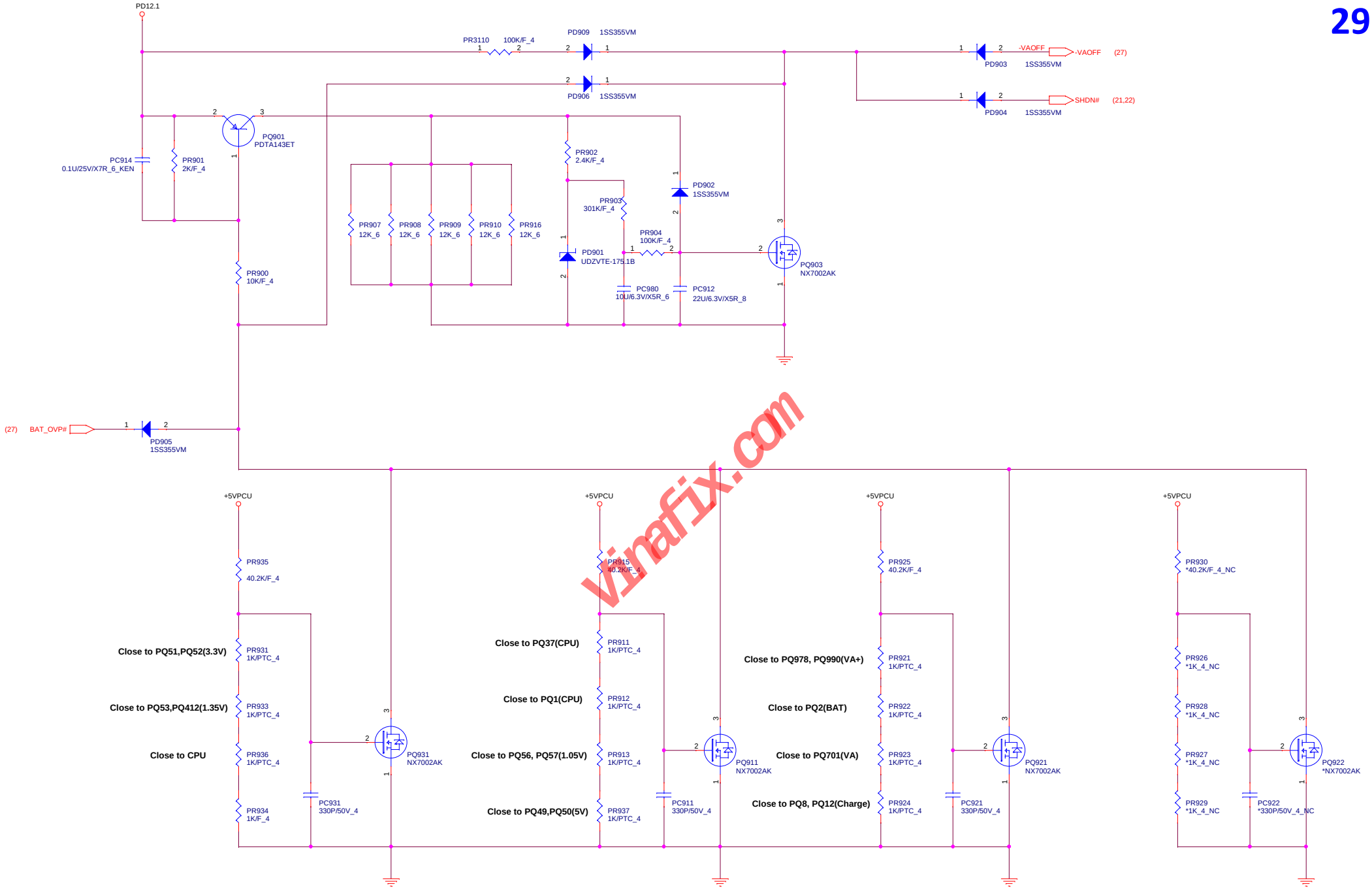
	REFON Status
Adapter Only	HI
Adapter+Battery	HI
Battery+Power On	HI

Quanta Computer Inc.
PROJECT : FF6
Size | Document Number | Rev
POWER ADP IN / BAT IN | A1
Date: Thursday, February 13, 2014 | Sheet 27 of 36

Battery Charger



Quanta Computer Inc.		
PROJECT : FF6		
Size	Document Number: POWER CHARGER (OZ8682)	Rev: A1
Date: Thursday, February 13, 2014	Sheet 28 of 36	



Quanta Computer Inc.

PROJECT : FF6

Size	Document Number	Rev
	POWER Thermal Protection	A1

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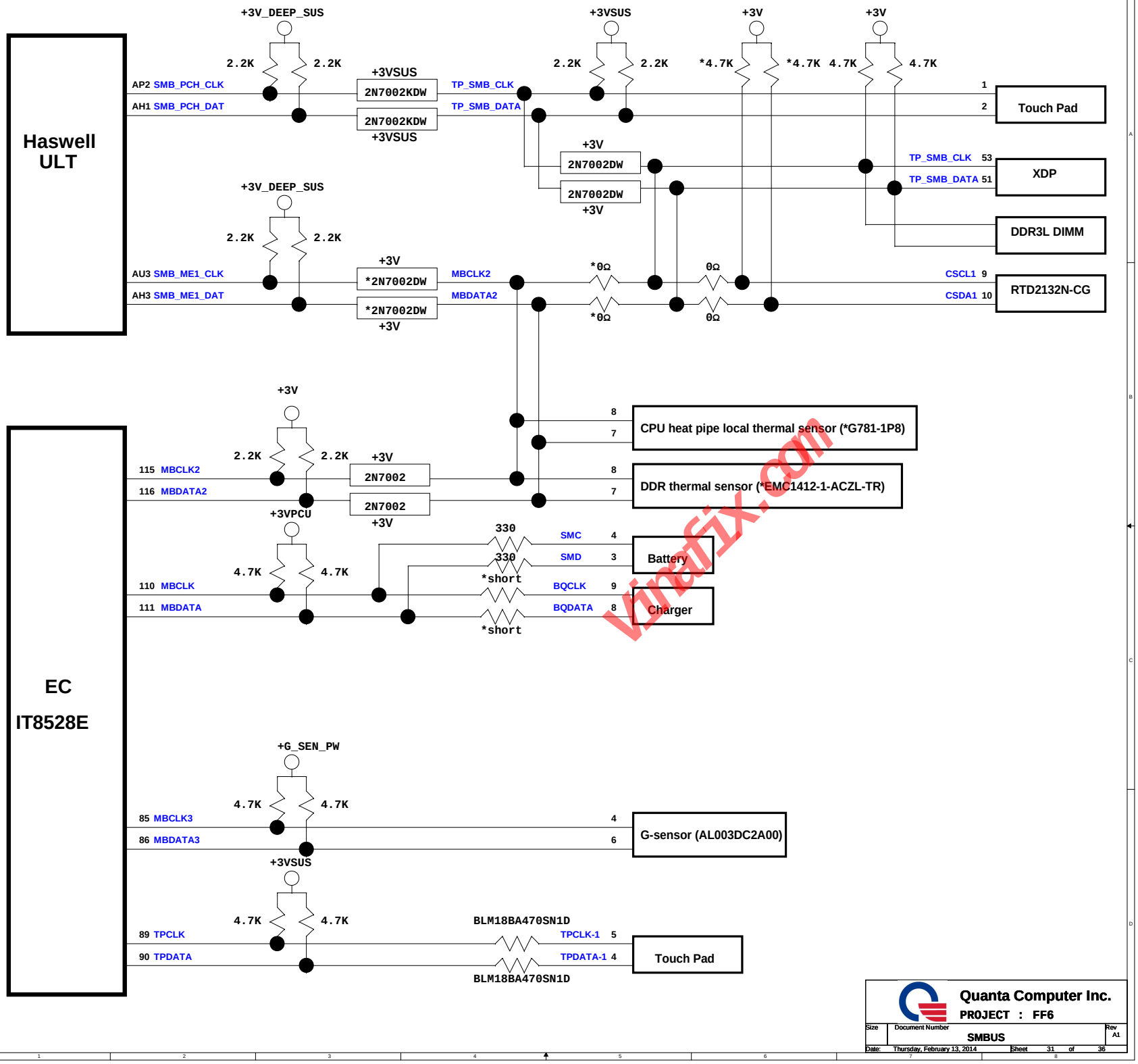
USB3.0	Port Assignment	Power control pin
PORT1	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
PORT3	NC	N/A
PORT4	NC	N/A

USB2.0	Port Assignment	Power control pin
PORT0	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
PORT1	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
PORT2	Camera	N/A
PORT3	NC	N/A
PORT4	NC	N/A
PORT5	Left side USB daughter B	USBPW_ON#(from EC)
PORT6	WLAN	N/A
PORT7	Touch Screen 15" used	TS_ON(from EC)

SATA Master	Port Assignment	Power control pin
SATA0	HDD	N/A
SATA1	NC	N/A
SATA2	NC	N/A
SATA3/PCIE	Card reader	N/A

PCIE	Port Assignment	Control pin
PCIE 5_L0	PEG0	
PCIE 5_L1	PEG1	
PCIE 5_L2	PEG2	
PCIE 5_L3	PEG3	
PCIE 1	NC	
PCIE 2	NC	
PCIE 3	WLAN	
PCIE 4	LAN	



Quanta Computer Inc.
PROJECT : FF6

Size	Document Number	Rev
	SMBUS	A1

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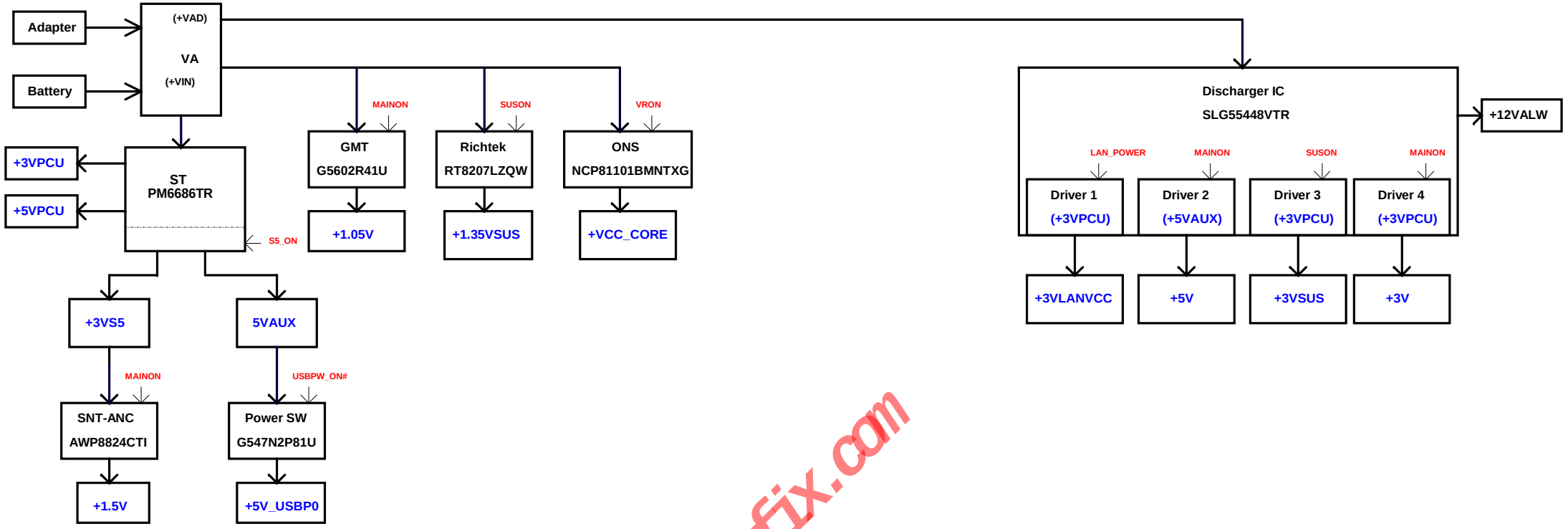

Quanta Computer Inc.

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Size	Document Number	Rev
	Power Block Diagram	A1

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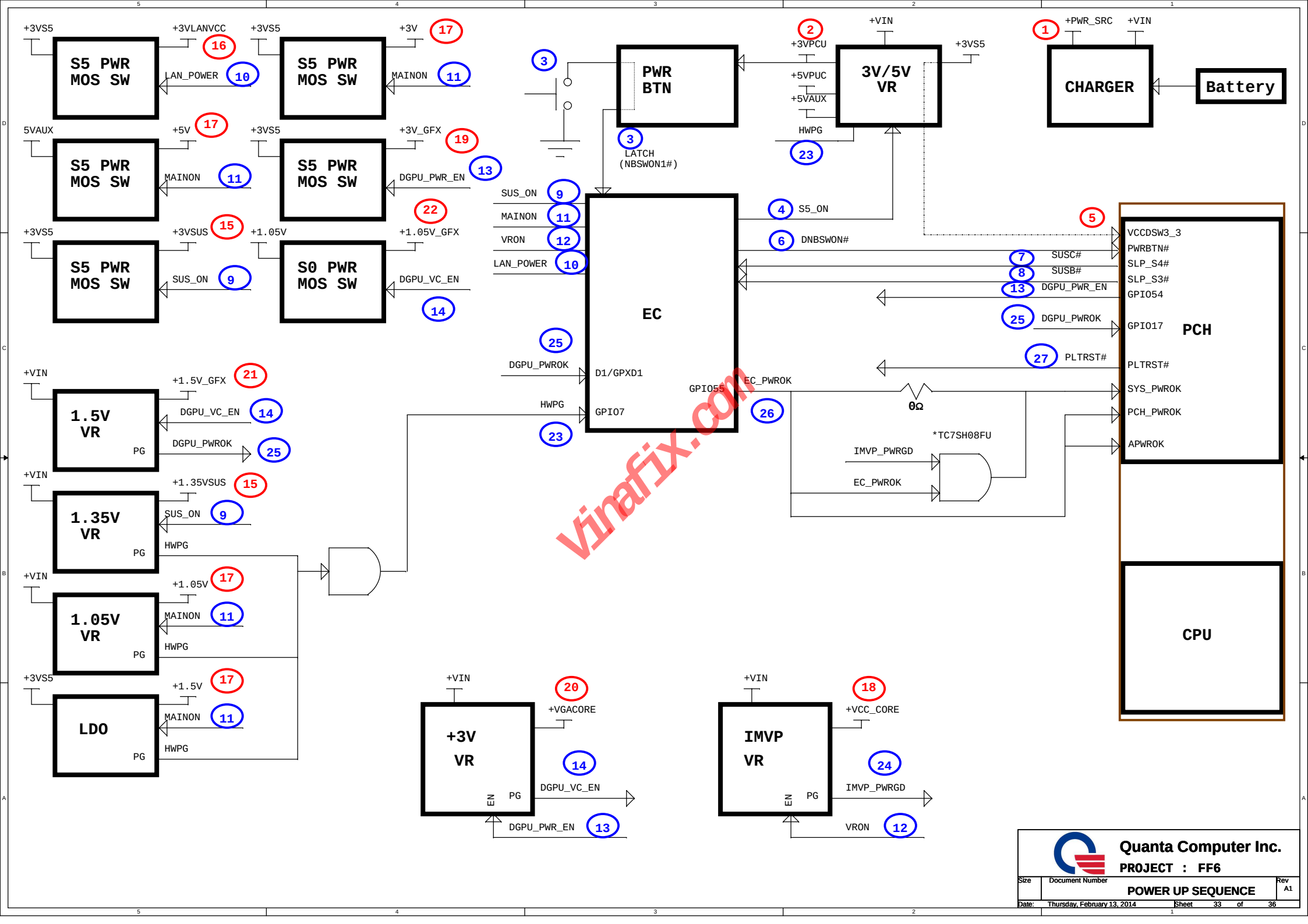
+3VS5
S5 PWR MOS SW
+3VLANVCC
16
LAN_POWER
10
+3VS5
S5 PWR MOS SW
+3V
17
MAINON
11
5VAUX
S5 PWR MOS SW
+5V
17
MAINON
11
+3VS5
S5 PWR MOS SW
+3V_GFX
19
DGPU_PWR_EN
13
22
+3VS5
S5 PWR MOS SW
+3VSUS
15
SUS_ON
9
+1.05V
S0 PWR MOS SW
+1.05V_GFX
DGPU_VC_EN
14
3
PWR BTN
3
LATCH (NBSWON1#)
2
+3VPCU
+5VPUC
+5VAUX
HWPG
23
+VIN
3V/5V VR
+3VS5
1
+PWR_SRC
+VIN
CHARGER
Battery
SUS_ON
9
MAINON
11
VRON
12
LAN_POWER
10
EC
4
S5_ON
6
DNBSWON#
5
VCCDSW3_3
PWRBTN#
SLP_S4#
SLP_S3#
GPIO54
GPIO17
PCH
7
SUSC#
8
SUSB#
13
DGPU_PWR_EN
25
DGPU_PWROK
27
PLTRST#
PLTRST#
SYS_PWROK
PCH_PWROK
APWROK
25
DGPU_PWROK
D1/GPXD1
GPIO55
EC_PWROK
26
0Ω
HWPG
23
GPIO7
*TC7SH08FU
IMVP_PWRGD
EC_PWROK
CPU
+VIN
1.5V VR
PG
+1.5V_GFX
21
DGPU_VC_EN
14
DGPU_PWROK
25
+VIN
1.35V VR
PG
+1.35VSUS
15
SUS_ON
9
HWPG
+VIN
1.05V VR
PG
+1.05V
17
MAINON
11
HWPG
+3VS5
LDO
PG
+1.5V
17
MAINON
11
HWPG
+VIN
+3V VR
EN
PG
20
+VGACORE
14
DGPU_VC_EN
DGPU_PWR_EN
13
+VIN
IMVP VR
EN
PG
18
+VCC_CORE
24
IMVP_PWRGD
VRON
12
Vinafix.com
Quanta Computer Inc.
PROJECT : FF6
Size
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POWER UP SEQUENCE
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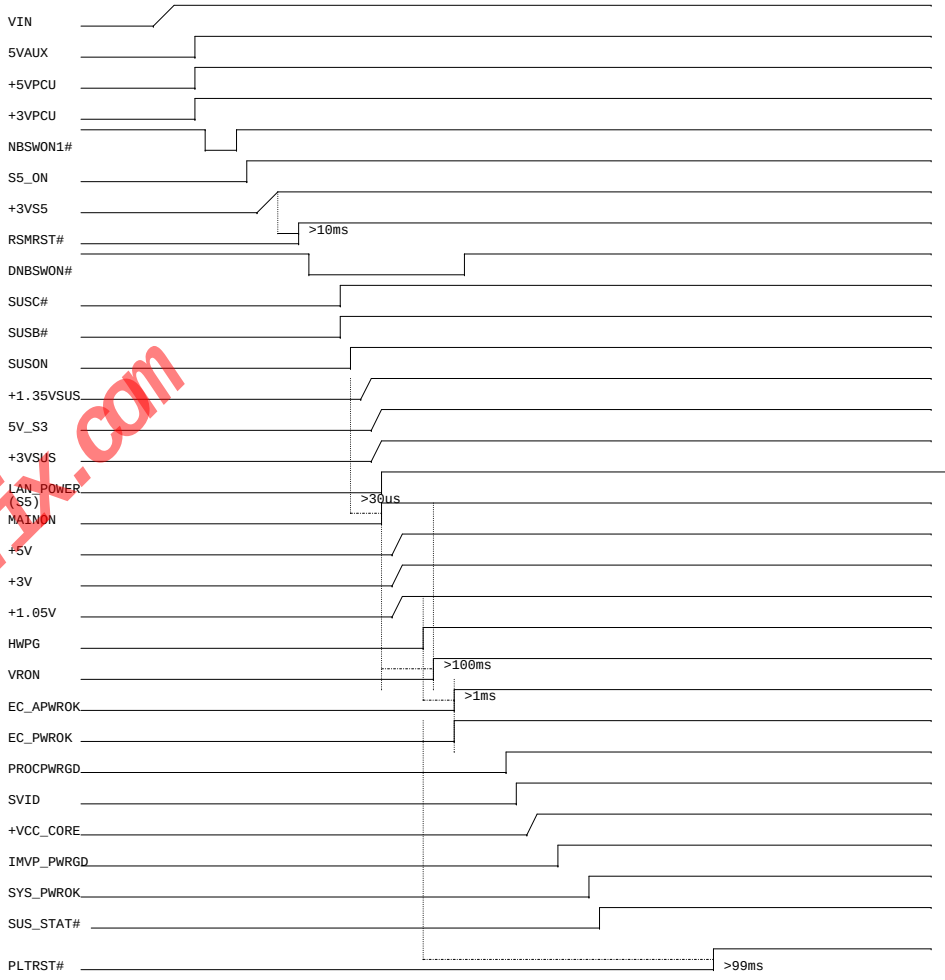
Power Sequence



Quanta Computer Inc.		
PROJECT : FF6		
Size	Document Number: POWER UP SEQUENCE	Rev A0
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FF6 ES2(Rev B).Change List

Date	Changes Summary
2013/12/05	1. Add R5127/20K for PP-stage board ID.. 2. Change R5126 from 45.3K to 24.3K for PP-stage board ID. 3. Del R5169 bom error. 4. Change L8/L9/L30/L33/L42 footprint from choke-wcm2012-4p to choke-exc24cg900u-4p.
2013/12/10	1. Add fuse(F20) for KB power. 2. Remove +3V power rail from HDD connector. 3. Add fuse(F21) for power board +3VPCU. 4. Add R5179、R5178、USB_OC2# & Del R173/10k for USB2.0 OCP.
2013/12/12	1. Change R402 from 1KΩ to 10KΩ for can't boot issue. 2. Add C8581/0.1uf for can't boot issue. 3. Del Q24/Q26/R350/R355/R359/R364,not support wireless lan on/off_LED function. 4. Del Q21/R67/R348/R5108, not support MUTE_LED function. 5. Dismount Q59/Q60/Q61/D21/R5177. 6. Del Q6/C606/R553/R552/R551/C604/C607/R456,PC beep function no need. 7. Add R5180/10kΩ for PCIE_CLKREQ4# PULL UP. POWER 1. Fixed MBCLK and MBDATA 2. Change CPU supply from 5VAUX to +5V 3. Del PR60, PR61, PR22, PR62, PC42 4. Change PC150 from 1U/16V to 1U/25V 5. Change PC143 footprint from 0603 to 0805 6. Change PC43&PC212 to 47U/25V 7. Change PC6 from 1500p/50V to 2200P/50V
2013/12/13	1. Reverse CN7 pin define for mechanical request. 2. Change F6 Ampere rating from 2A to 3A for meet panel spec. 3. Add R316 & dismount Q18/C8538/R560/R324/Q20 for solve 3V_WLAN_P discharge too slow. 4. Add C590/1000pf & Change R309/R312/R313/R318/R321 from 0ohm to 33ohm for EMI request. 5. Change F14 Ampere rating from 0.75A to 0.5A for meet touch pad spec. 6. Add PL14 & del PQ35/PQ41/PQ42/PR105/PR106/PR113/PR199/PC137/PC23/PC141 for +1.05V_MODPHY timing. 7. Change PC162 from 0.022uf to 0.01uf for +1.05V_MODPHY timing.(+1.05V→+3V→1.05V_MPHY)
2013/12/16	1. Add R5181/R5182/R5183/R5184/R5185/R5186/R5187/R5188/R5189 for TPM co-layout design. 2. Del R447 & Add net SYS_PWROK_1 for meet power sequence Spec. POWER 1. Change PC187 to 330P/50V 2. Change PR162 from 22.6K to 23.7K 3. Change PC843&PC842 from 47P/50V to 22P/50V
2013/12/17	1. Add R5192 for SYS_PWROK_1,Reserved 2. Del D3/R235 & Add D59,to avoid blinking issue on panel. 3. Add Q62,for reserve clear CMOS by software control.
2013/12/30	1. Del C3,C596 & Change R548 from 0R to 75R for DMIC issue.

	FF6 PP(Rev C).Change List
Date	Changes Summary
2014/2/6	1.Change FAN1 footprint：50273-0047n-001-4p-l 2.Change C8554,C8556 from 150uf to 220uf.solve big drop voltage. 3.Change EL25 from 5A to 6A for OCP. 4.Change PF700 from 10A to 6A for OCP. 5.Change PR27 footprint from 0402 to 0603 for against noise. 6.Add PR116,PC140,PC986 for reduce switch noise. 7.Change R5126 from 24.3K to 12K for MRT board id. 8.Change C8581 from 0.1UF to 1UF for can't boot issue.
2014/2/10	1.Add PC987,PQ993,PR765,PR765,PR3181,PR3182,to solve the charge issue (stop charge to RSOC=99%). 2.Del D14 & Add Q8,R5194,R5193. Reserve EC control method since Tcpu00 margin Spec isn't clarified yet.
2014/2/11	1.Change PD731 to BDUDZ16BZ00.The reason is avoiding the Adapter unplug w/Battery, the ACIN signal still remain high level.
2014/2/12	1.Add PR3184. Resevre for solve debounce issue.
2014/2/13	1.Add PD910.The reason is avoiding the Adapter unplug w/Battery, the ACIN signal still remain high level.

Quanta Computer Inc.
PROJECT : RR3A
Size: Document Number: ES2 Change History Rev: X
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