PR600
Trouble Shooting Guide

Project Name: **MS-1637**
Marketing Name: **PR600**

Edit	WilliamHsu
Data	November. 27, 2007
Ver	1.0

ELETRÔNICA

Contents

1、Introduction

1.1 Overview

MS-1637 notebook computer provide Intel® Santa Rosa platform design contains: Intel™ processor on 65 nanometer process and Crestline chipset (965GM) + ICH8M.

MS-1637 targets low cost ,and two spindle platform market by incorporating the upgradeable Intel® processor , 15.4" TFT ,removable HDD , build in Combo /DVDRW ,USB2.0,on board Giga LAN, MDC , Bluetooth, Mini card for Intel 802.11b/g/n wireless LAN,IEEE1394 , 3 in 1 Card reader, Audio….

1.2 MS-1637 Product Specification (965GM-UMA + ICH8-M)

Item		H/W Spec
Model	Spindle	2
CPU	Processor Type	PBGA 478pin
	Support Processor @ Launch	Core™ DUO for Santa Rosa
	L2 Cache	2M/4M
	FSB Speed	667/800 MHz
	Socket	PBGA 478pin
Memory	Technology	DDR II 533/667/800Mhz SDRAM
	Memory	DDR II SO-DIMM X 2 slot 256/512/1024/2048 MB
	(Max.)	2GB (2G DDR II SO-DIMM x 2)
CoreChip	North Bridge	GL965GM
	South Bridge	ICH8-M (82801HBM)
Display	LCD Type	15.4" WXGA Glare/ Non-glare
	Brightness	Brightness controlled by K/B hot-keys
Video	Controller	GL965 (GMA X3100)
	VRAM	Sharing system memory
	LCD	1280x800 for WXGA
Audio	Sound Controller	Embedded in South Bridge
	Sound Codec chip	Realtek ALC883
	Internal Speaker	2 Speakers, 1.5W
	Internal Microphone	Yes
	Sound Volume	Adjust by volume button, K/B hot-key & SW

ELETRÔNICA

Communication Port	56K Fax/MODEM	MDC1.5 (Azalia)
	I/F	AZALIA S/W Modem
	Controller	AZALIA Embedded
	Wake on Ring	Support on S1/S2/S3 state
	LAN	Giga LAN 10/100/1000
	LAN Controller	Realtek RTL811B
	Wake on LAN	Support on S3/S4/S5 state
	LAN Boot	Yes
	Blue Tooth	MS-6837D, Bluetooth 2.0
	Wireless LAN	IEEE802.11A/B/G/N, MSI 6877/Kedron
PCMCIA	Controller	O2 OZ711SP
	Care Reader	MMC/SD/MS Pro 3 in 1 card reader x 1
	Card Bus	Type II x 1
I/O	D-Sub	x 1
	USB 2.0	x 4
	IEEE1394	x 1
	Mic-in	x 1
	RJ11	x 1
	RJ45	x 1
	S-Video	x 1
	Headphone / SPDIF out	x 1
Storage	HDD form factor	2.5" 9.5mm High, SATA 150, S.M.A.R.T, 5400~7200 rpm
	HDD Capacity	from 60GB to latest perpendicular capacity
	IDE Controller	ICH8-M
	Optical Bay	Combo, DVD-Dual+R9
Keyboard	Controller	ENE 3910
	MS Standard key code	Support
	Number of Keys	103 Keys
Hot Keys	Dual Display	Fn + F2
	Touch Pad Disable/enable	Fn + F3
	LCD brightness / Down	Fn + F4
	LCD brightness / UP	Fn + F5
	Speaker Volume / Down	Fn + F7
	Speaker Volume / up	Fn + F8
	Speaker ON/OFF	Fn + F9

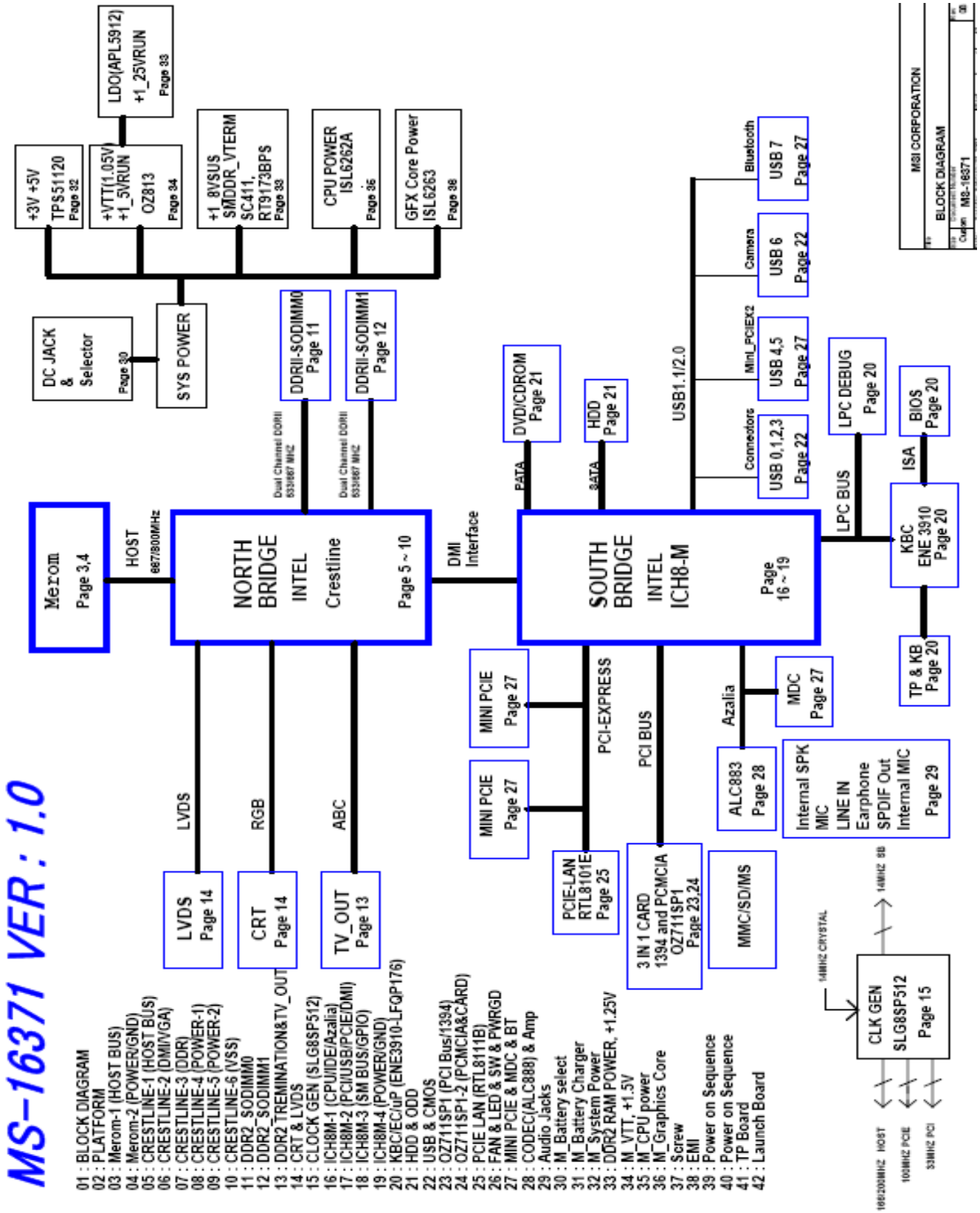
	Camera enable	Fn + F10
	Bluetooth disable	Fn + F11
	Sleep Button	Fn + F12
Feature	Camera Module	Yes
Launch Keys	Lunch Keys	4 Keys
		-Power
		-E_Mail
		-Internet Explorer
		-Bluetooth/WLAN
		-P1
Pointing Device	Glide	Elantech with 2 buttons (click x 2)
Power	AC adapter	65W
	1st Battery	6 cells(Li-ion) (2200mAh x2)
	1st Battery Life	3 hrs, Battery Mark
	RTC Battery	Yes , 3 yrs
Security Features	Kensington Lock Hole	Support (x1)
	HDD password	BIOS setting
Status Indicator	Indicator	- Power Status / suspend (Visible when LCD module closed)
		- HDD Status
		- Battery Status (Visible when LCD module closed)
		- Num Lock
		- Caps Lock
		- Scroll Lock
		-Wireless/ Bluetooth LAN on/off (visible when LCD module closed)
Physical Characteristics	Dimension	358 (W) x 259 (D) x 27-33(H) mm
	Weight	2.8 Kg with 6 cell Battery
Compliance	WHQL	Win XP, Vista
Software	Support OS	Win XP, Vista
	USB Flash boot	Yes, USB floppy boot up DOS only
BIOS	Fast Boot Support	Yes
	OSD for Fn	SCM
	VISTA capable	Yes
	Tool for splash screen customization (post logo)	Yes

ELETRÔNICA

	Boot form USB	Yes
	Disable / enable Wireless LAN	Yes
	Disable / enable all device boots	Yes
	Disable / enable SMART functionality for HDD	Yes
Power Management	ACPI for Vista Capability	Yes
EMC	EMS	CE Mark (Europe)
	EMI	FCC Class B Certified (USA & Canada)
		BSMI (Taiwan)
		CE Mark / Ctick
		CCC (PRC)
Safety	Safety	UL, CSA (CUL) (USA & Canada)
		TUV(Germany)
		TUV-CB Report, CE-LVD Report(Europe)
RF		USA, Canada, Taiwan, China,
		Europe (Germany, France, Italy, Spain, UK)
	Telecomm.	FCC Part 68 (USA & Canada)
		CTR 21 (Europe), JATE (Japan)

2、System Architecture

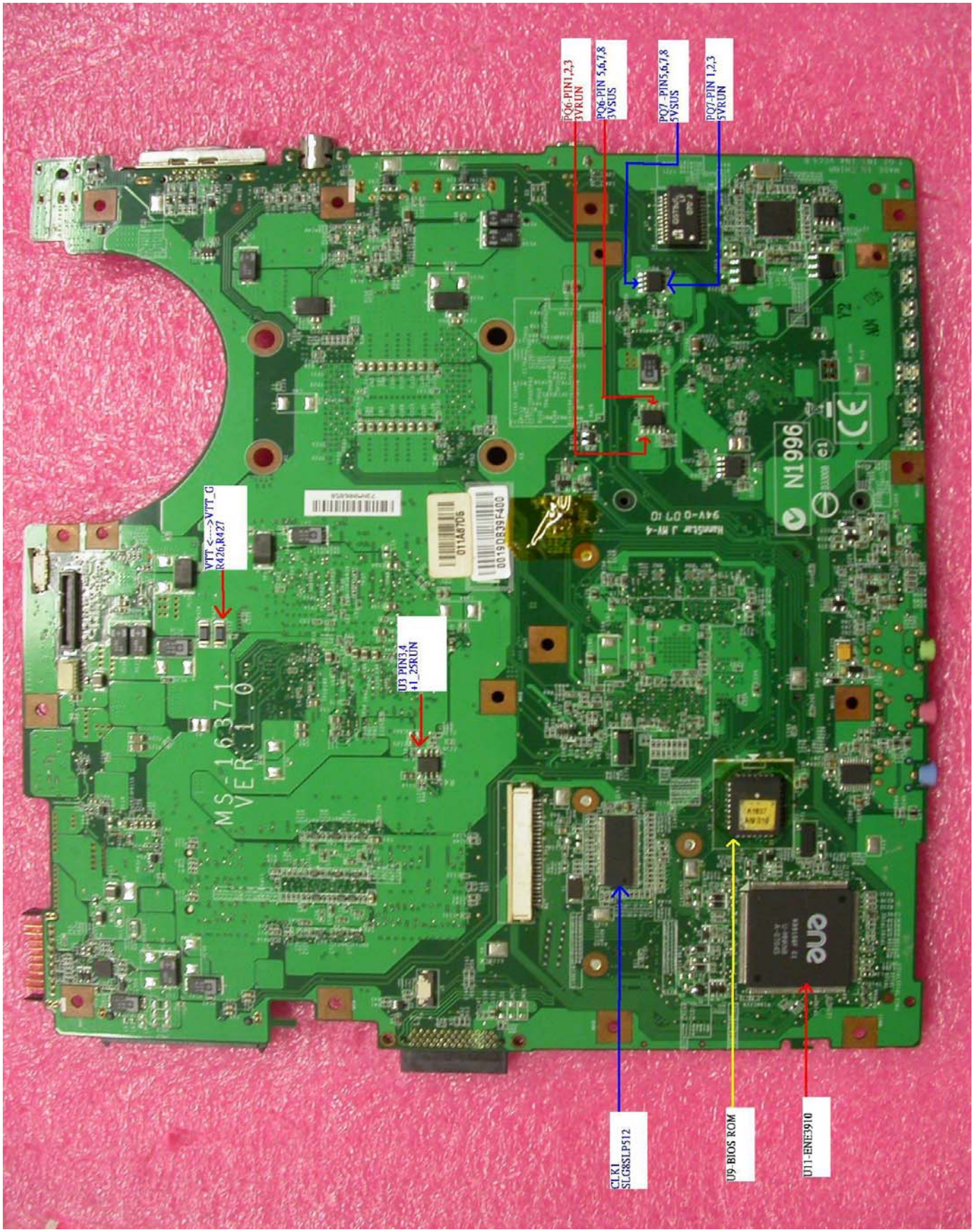
2.1 Block Diagram



ELETRÔNICA

2.2 PCB Assembly Description

Top View

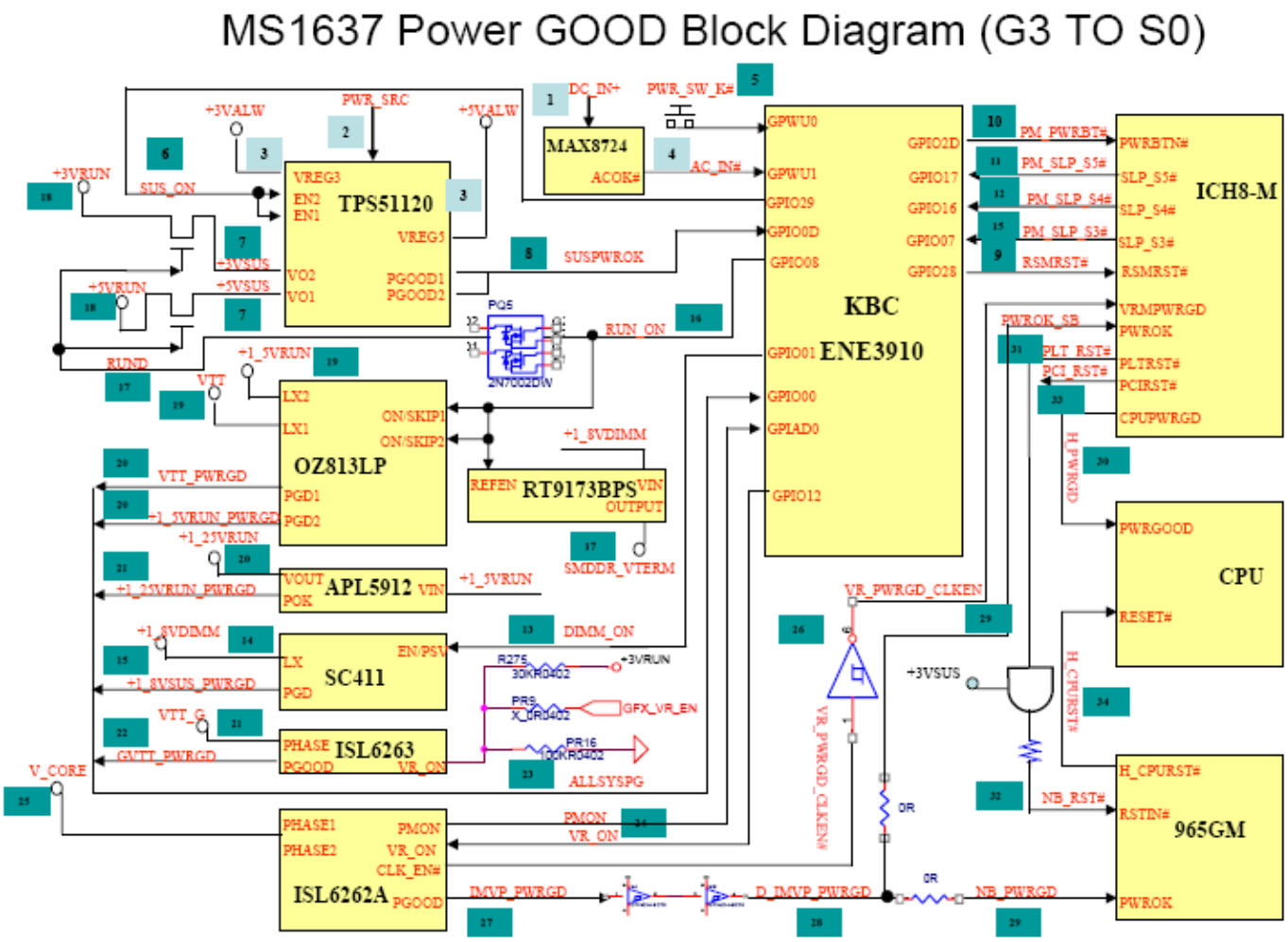


Bottom View

ELETRÔNICA

3、Power Map & Repair Flow Chart

3.1、POWER MAP



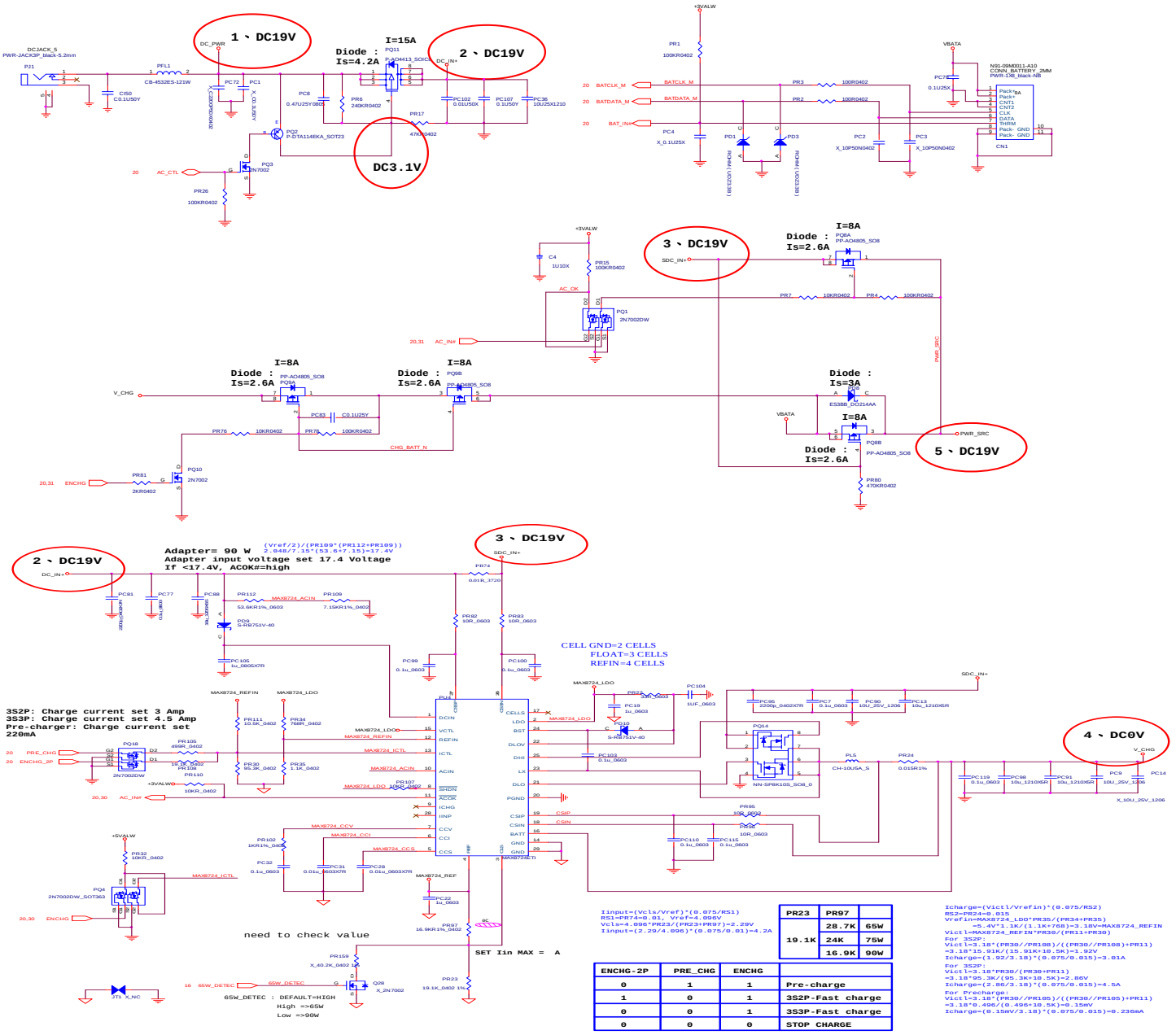
3.2 Repair Flow Chart

Debug by power sequence(Only insert adapter)：
Please follow below step to check power source

Step 1、**MAIN Power(PWR_SRC)**

Item	Name	Description	Check Component (related signal)	Note
1-1	DC_PWR	DC19V	PJ1、PQ11	
1-2	DC_IN+	DC19V	PQ11	
1-3	SDC_IN+	DC19V	PR74	
1-4	V_CHG	DC0V	PU4(pin16)	When battery charge, the voltage value is DC12.6V
1-5	PWR_SRC	DC19V	PQ8	

Note 1：It is recommendation to check the PWR_SRC (Power) first. If the power is right, you can check the next step directly. If the power is fault, please check the related signal.



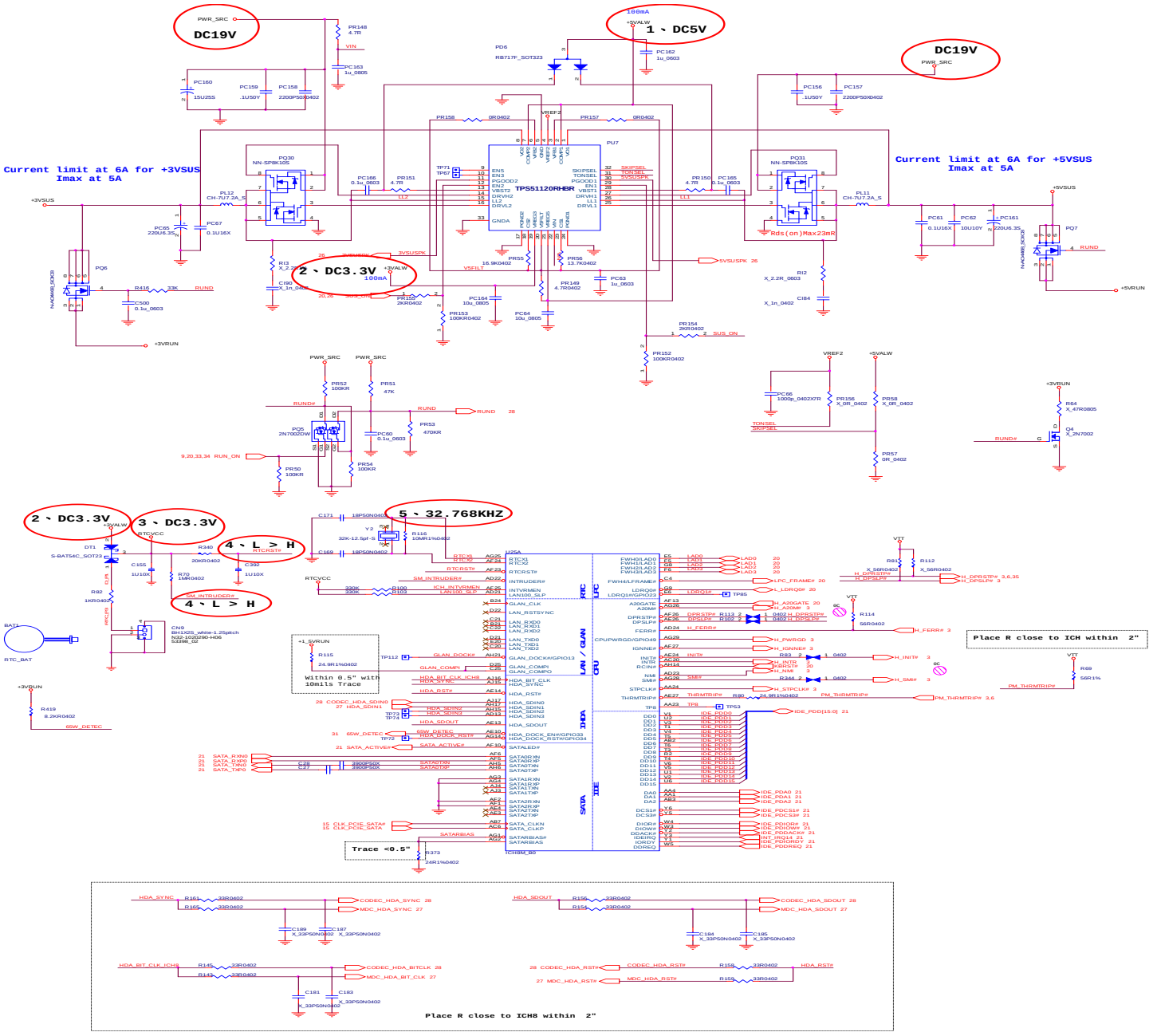
ENCHG-2P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	3S2P-Fast charge
0	0	1	3S3P-Fast charge
0	0	0	STOP CHARGE

PR23	PR97	
19.1K	28.7K	65W
	24K	75W
	16.9K	90W

Step 2、**3VALW & 5VALW & RTCVCC**

Item	Name	Description	Check Component (related signal)	Note
2-1	+5VALW	DC5V	PU7-pin21(+5VALW)	
2-2	+3VALW	DC3.3V	PU7-pin19(+3VALW)	
2-3	RTCVCC	DC3.3V	DT1(RTC Power)	
2-4	RTCRST	L＞H(DC3.3V)	R340&C392	
2-5	Y2	32.768KHZ		

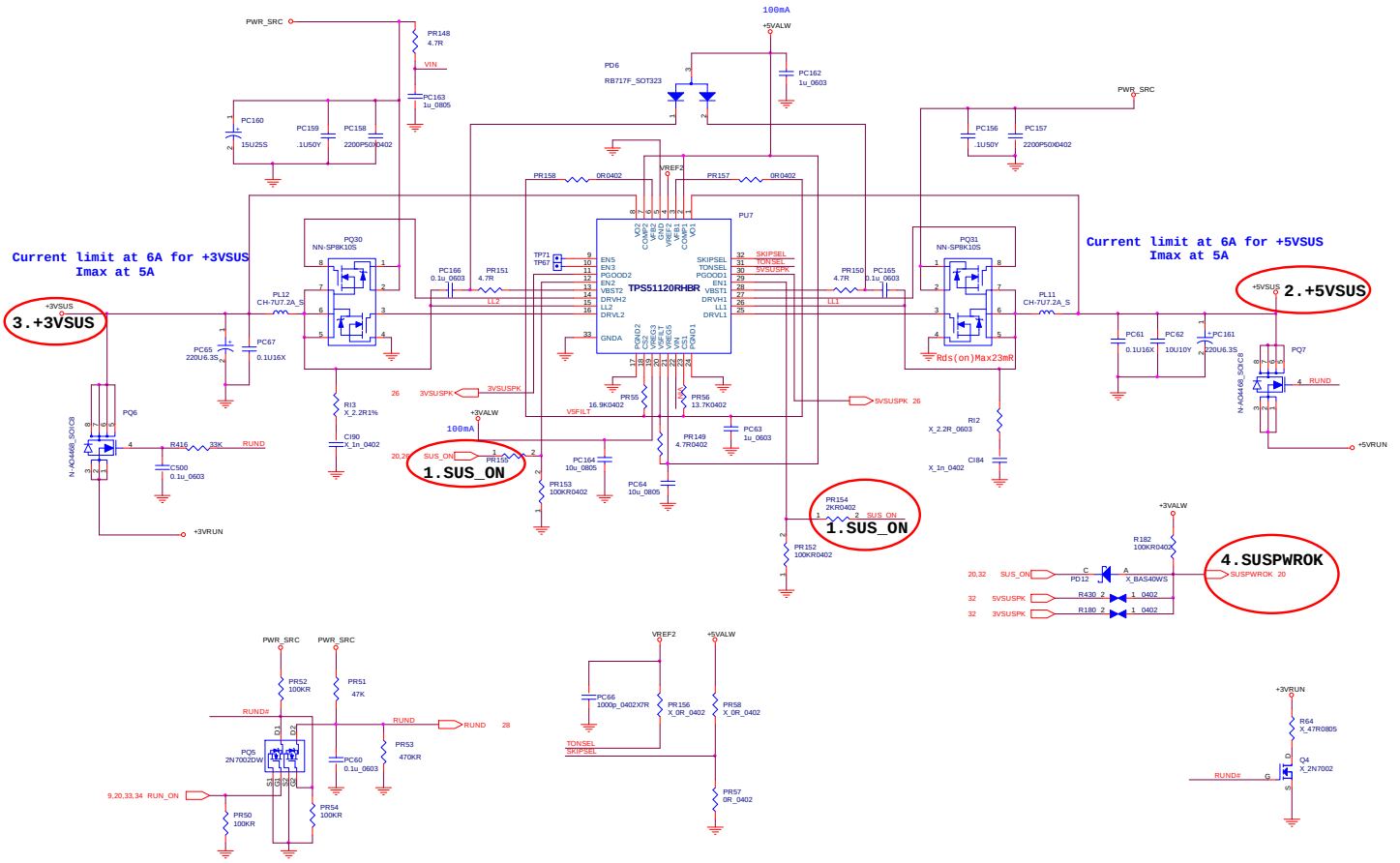
Note 1：It is recommendation to check the +5VALW、+3VALW、RTCVCC(Power) & Y2 (clock) first. If these power are right, you can check the next step directly. If these signals are fault, please check the related signal.
Note 2: The L > H signal is H level.



Step3、**SUS Power**

Item	Name	Description	Check Component (related signal)	Note
3-1	PWR_SW_K#	Push bottom at least 100ms H > L(DC0V)	J1-pin6 & U11-pin2	
3-2	SUS_ON	L > H(DC3.3V)	U11-pin155& PR154& PR155 (+5VSUS & +3VSUS)	
3-3	+5VSUS	DC5V	PQ7-pin5&PL11(+5VSUS)	
3-4	+3VSUS	DC3.3V	PQ6-pin5&PL12(+3VSUS)	
3-5	3V/5VSUSPK	3V/5V SUS Power OK L > H(DC3.3V)	PU7-pin11&PU7-pin30	
3-6	SUSPWROK	SUS Power OK L > H(DC3.3V)	U11-pin27&R183&R171	

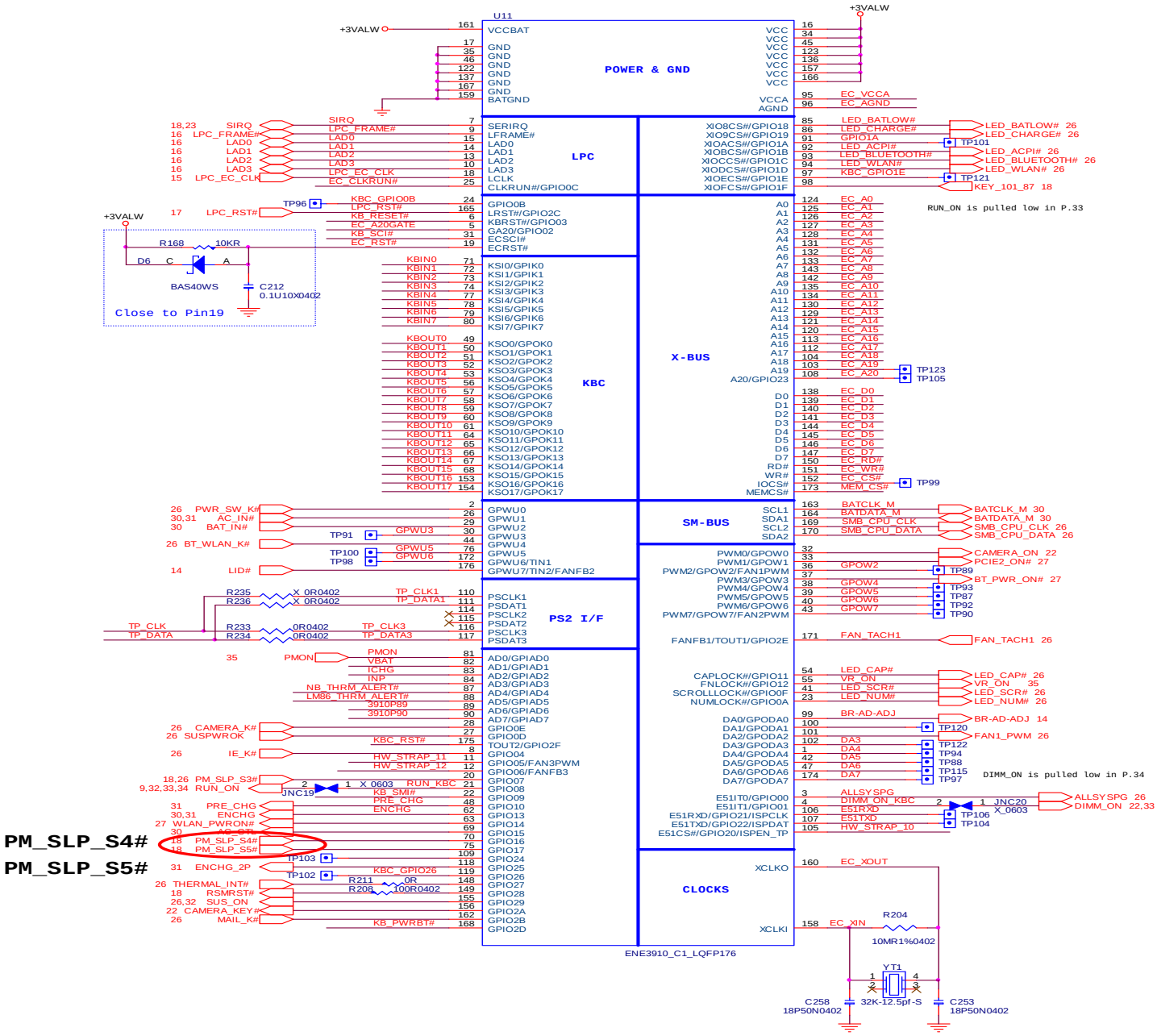
Note 1：It is recommendation to check the SUSPWROK first. If this signal is right, you can check the next step directly. If this signal is fault, please check the related signal.
Note 2：The L > H signal is H level；The H > L signal is L level

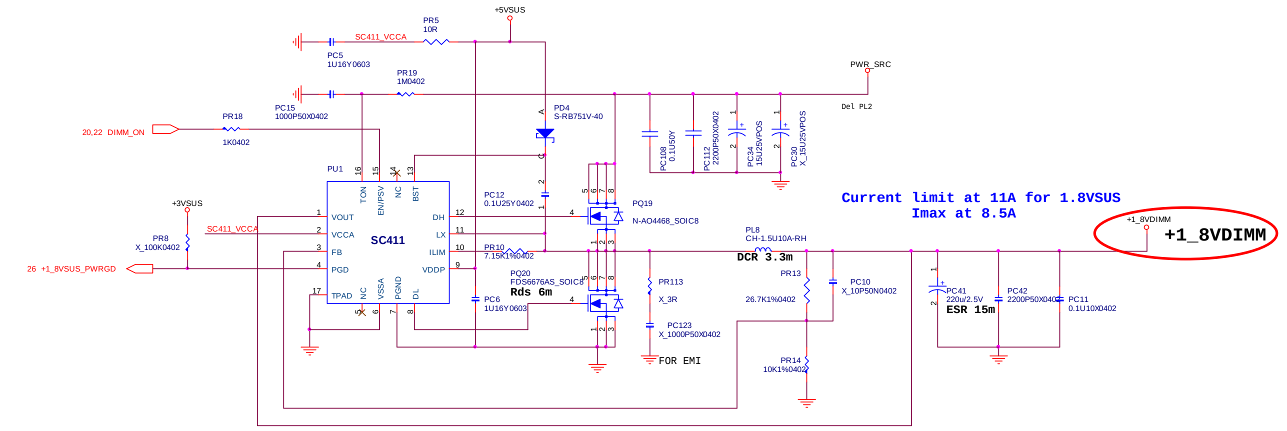


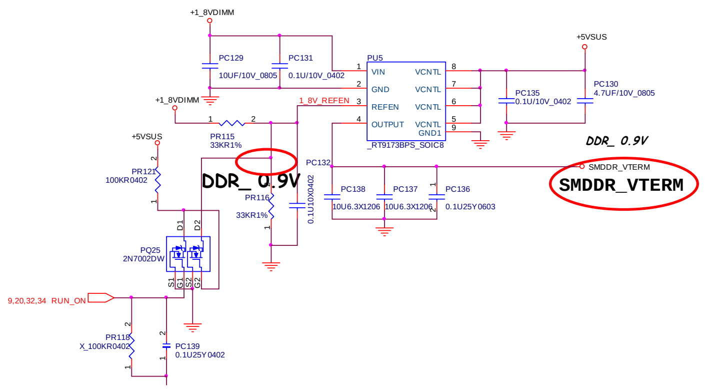
Step4、**DDR2 Power**

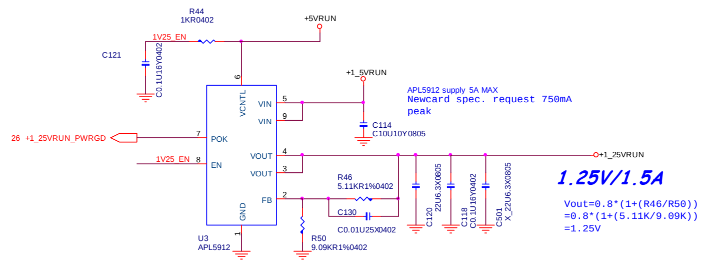
Item	Name	Description	Check Component (related signal)	Note
4-1	RSMRST#	L > H(DC3.3V)	U25-PinAG27,R208&R209	
4-2	PM_PWRBTN#	L > H(DC3.3V)	U25-PinC2,D13	
4-3	PM_SLP_S5#	L > H(DC3.3V)	U25-PinAD18,U11-pin75	
4-4	PM_SLP_S4#	L > H(DC3.3V)	R126,U11-pin70	
4-5	+1_8VDIMM	DC1.8V	PL8,PU1-pin1	
4-6	SMDDR_VTERM	DC0.9V	PU5-pin4	

Note 1：It is recommendation to check the SMDDR_VTERM first. If this signal is right, you can check the next step directly. If this signal is fault, please check the related signal.
Note 2：The L > H signal is H level；The H > L signal is L level




SC411
Current limit at 11A for 1.8VSUS
Imax at 8.5A
+1_8VDIMM
DCR 3.3m
ESR 15m
Rds 6m
FOR EMI
PWR_SRC
Del PL2


DDR_ 0.9V
SMDDR_VTERM
RT9173BPS_SOIC8

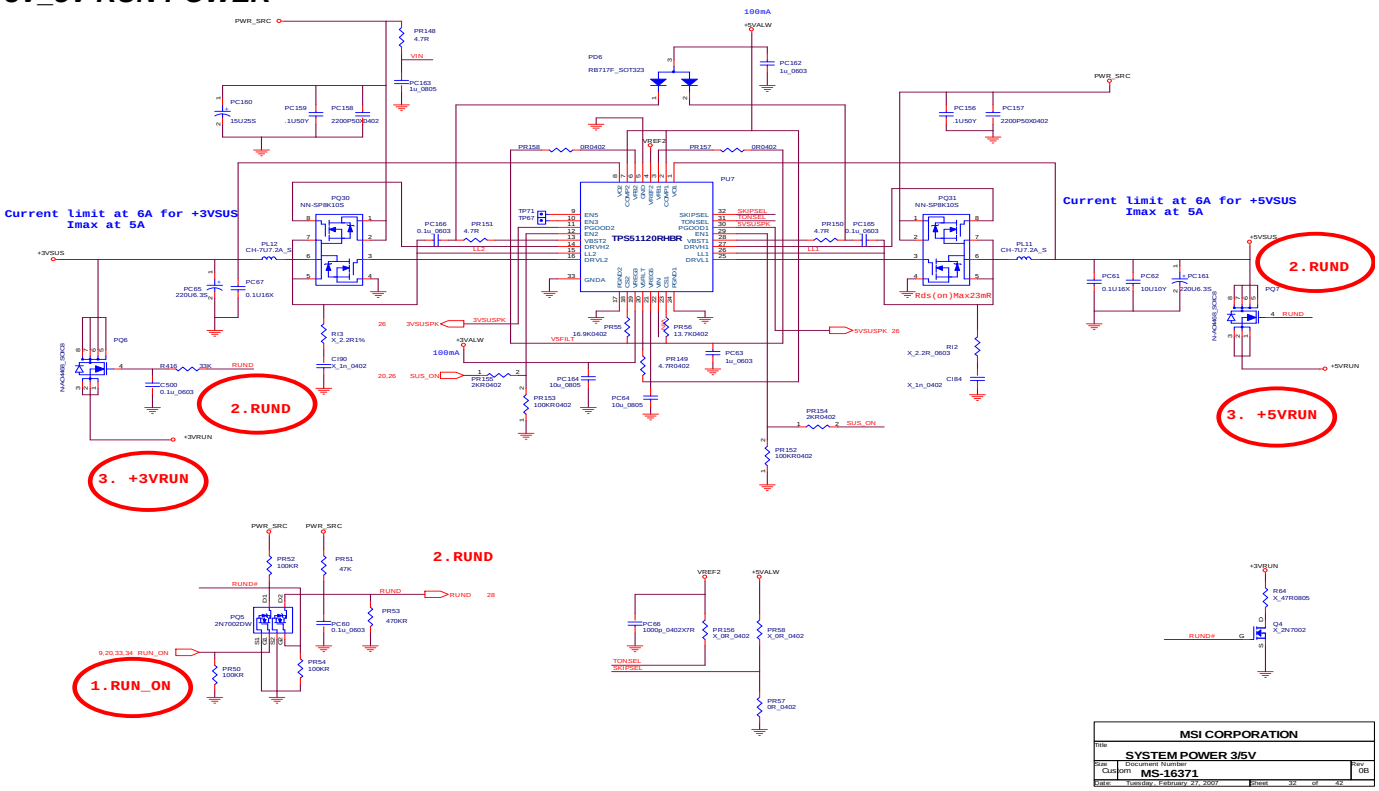

APL5912 supply 5A MAX
Newcard spec. request 750mA
peak
1.25V/1.5A
Vout=0.8*(1+(R46/R50))
=0.8*(1+(5.11K/9.09K))
=1.25V

Step5、**RUN POWER**

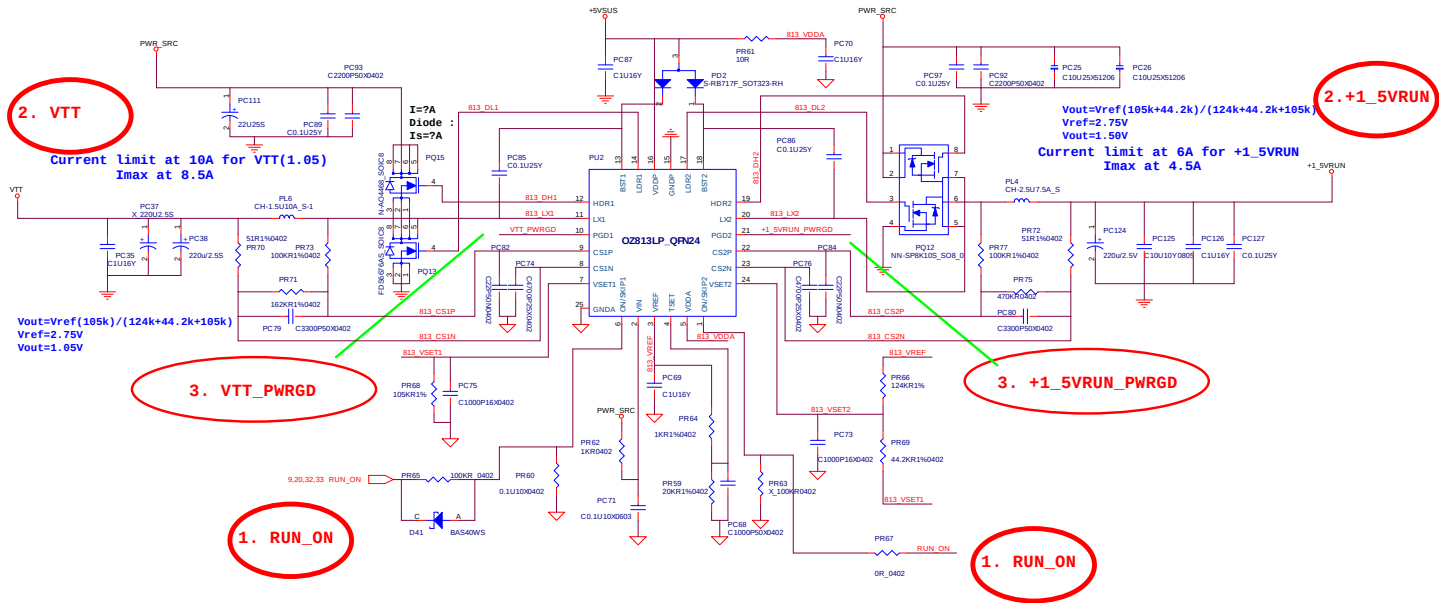
Item	Name	Description	Check Component (related signal)	Note
5-1	PM_SLP_S3#	L > H(DC3.3V)	R125 (PM_SLP_S3#) U11-pin20	
5-2	RUN_ON	L > H(DC3.3V)	U11_PIN21(RUN_ON)	
5-3	RUND	DC 17.75V	PR51(RUND)	
5-4	VTT	DC1.05V	PL6(VTT)	
5-5	+1_5VRUN	DC1.5V	PL4(+1_5VRUN)	
5-6	+3VMCLK	DC3.3V	L26 CLK1(Clock Power)	
5-7	+5V_AUDIO	DC5V	Q27 & U14,U27(Codec Power)	
5-8	+1_25VRUN	DC1.25V	U3_PIN3,4(+1_25VRUN)	
5-9	+3VRUN	DC3.3V	PQ6(+3VRUN)	
5-10	+5VRUN	DC5V	PQ7(+5VRUN)	
5-11	+1_5VRUN_PWRGD	Power Good L > H(DC3.3V)	PU2-pin21 (+1_5VRUN_PWRGD)	
5-12	VTT_PWRGD	Power Good L > H(DC3.3V)	PU2-pin10 (VTT_PWRGD)	
5-13	ALLSYSPG	ALL Power Good L > H(DC3.3V)	R2 ,U11-pin3 (ALLSYSPG)	

Note 1：It is recommendation to check the ALLSYSPG first. If this signal is right, you can check the next step directly. If this signal is fault, please check the related signal.
Note 2：The L > H signal is H level；The H > L signal is L level

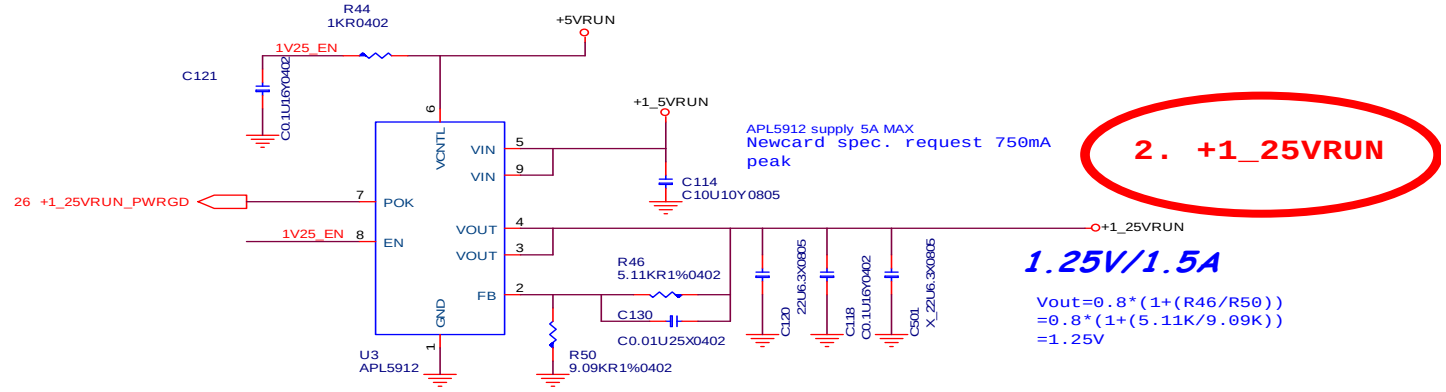
3V_5V RUN POWER



VTT & 1.5V RUN POWER



+1.25V RUN

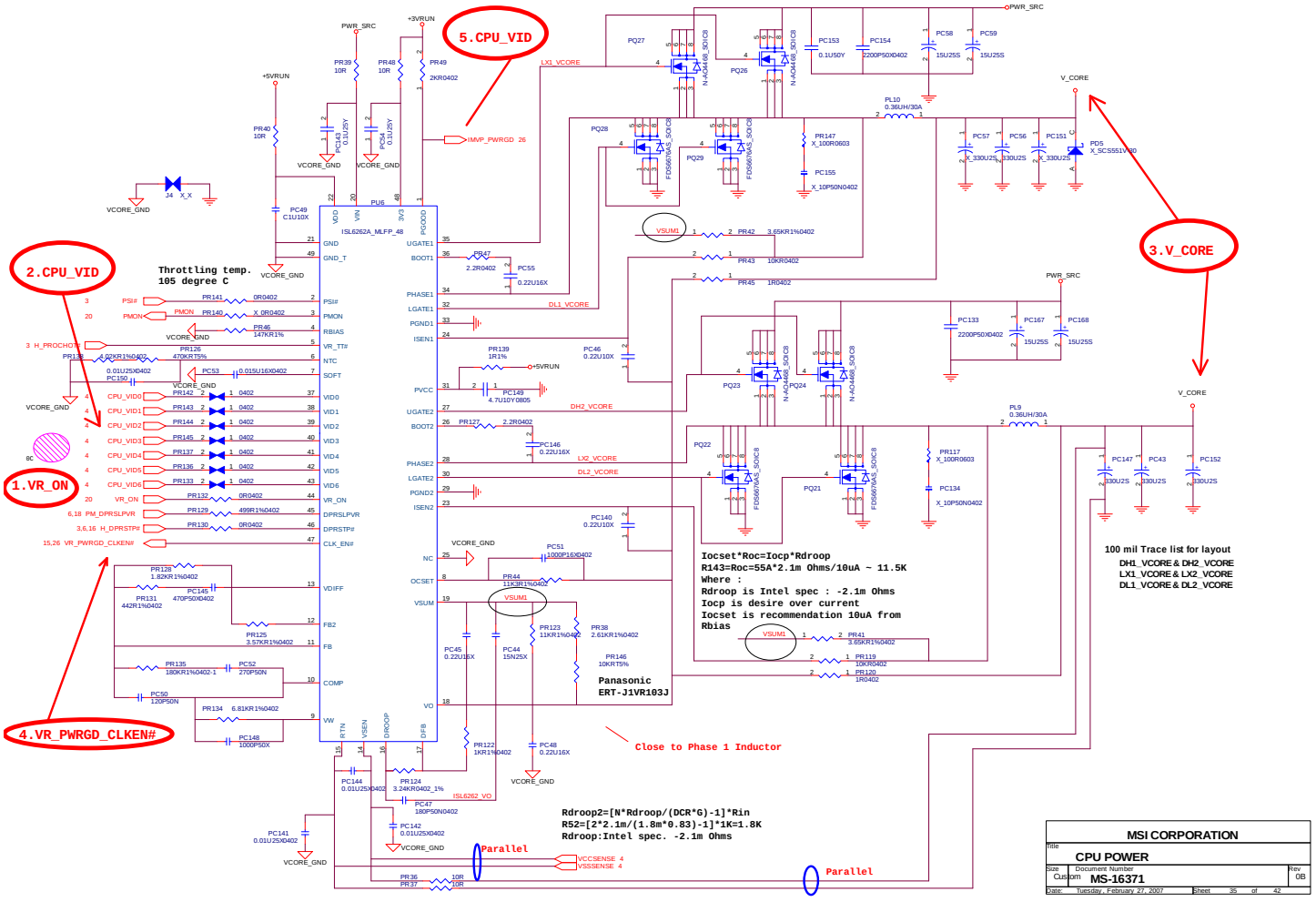


ELETRÔNICA

Step6、**CPU Power**

Item	Name	Description	Check Component (related signal)	Note
6-1	VR_ON	L > H(DC3.3V)	U11-pin55 & PU6-pin44 (VR_ON)	
6-2	V_CORE	Control by VID[6:0]	R88 & U25(CPU Power)	
6-3	VR_PWRGD_CLKEN#	H > L(DC0V)	PU6-pin47 (D_VR_PWRGD_CLKEN#) U24-pin1,6 (VR_PWRGD_CLKEN)	
6-4	IMVP_PWRGD	PWROK L > H(DC3.3V)	PU6-pin (IMVP_PWRGD) U20_AW49/R287-PWROK& U25_AE23/R101-PWROK	

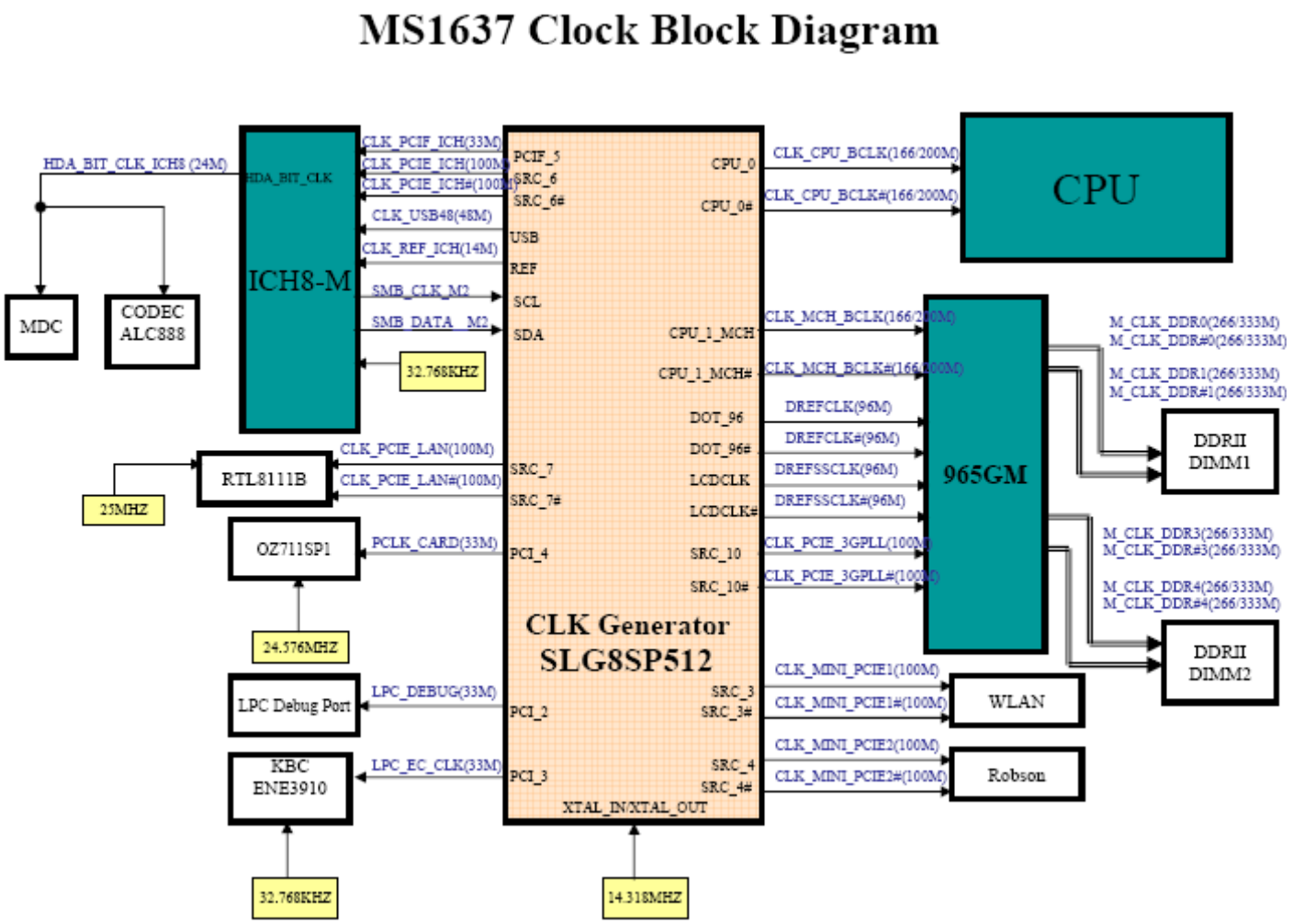
Note 1：The L > H signal is H level；The H > L signal is L level



4、Clock Map & Repair Flow Chart

4.1、CLOCK MAP

Santa Rosa platform uses the CK505 single-chip clock solution. Figure 1 and Figure 2 show the implementation of the clocks for a typical platform, with an internal graphics solution



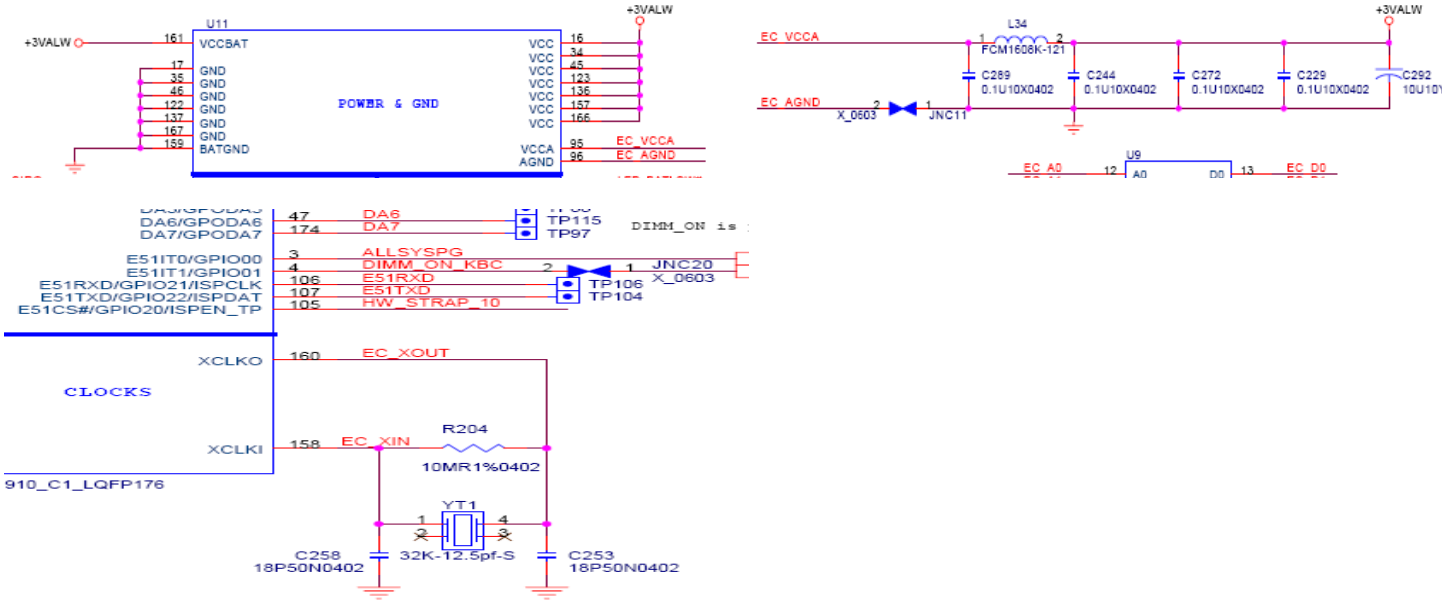
ELETRÔNICA

4.2 Repair Flow

If we find all power of system is ready, we must follow below steps for checking clocks whether is correct or not.

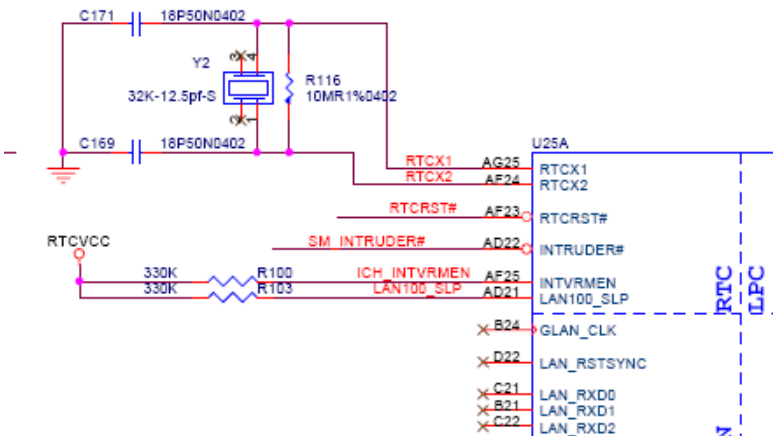
1. Check power (+3VALW) & clock of EC whether is active or not.

Item	Subject	Net name	Level	Measure Point
1	Power	+3VALW	+3.3V	U11,PIN16
2	Clock	EC_XIN	32.768KHZ	U11,PIN158
3	Clock	EC_XOUT	32.768KHZ	U11,PIN160



2. Check RTC clock whether is active or not.

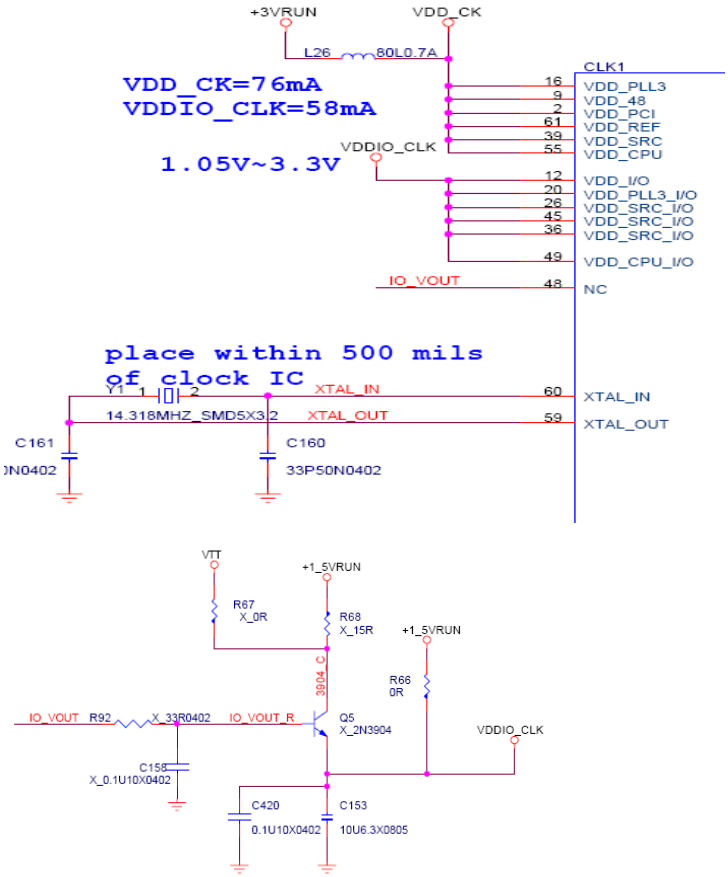
Item	Subject	Net name	Level	Measure Point
1	Clock	RTCX1	32.768KHZ	Y2,PIN4
2	Clock	RTCX2	32.768KHZ	Y2,PIN1



3. Check power (+3VMCLK&VDDIO_CLK) & clock of CLK Gen whether is active or not.

Item	Subject	Net name	Level	Measure Point
1	Power	VDD_CK	+3.3V	L26
2	Power	VDDIO_CLK	+1.5V	R66
3	Clock	XTAL_IN	14.318MHZ	Y1,PIN2
4	Clock	XTAL_OUT	14.318MHZ	Y1,PIN1

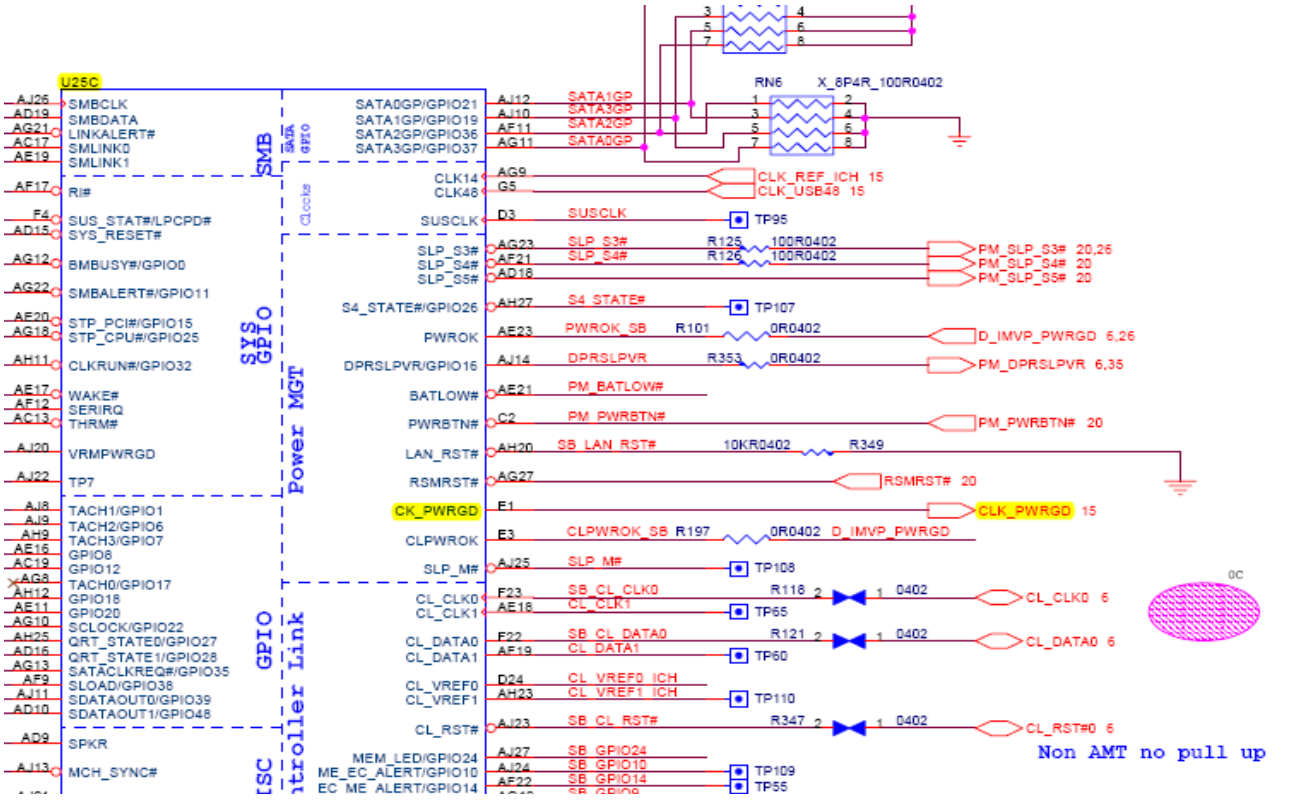
CLK Gen(CLK1) Schematic

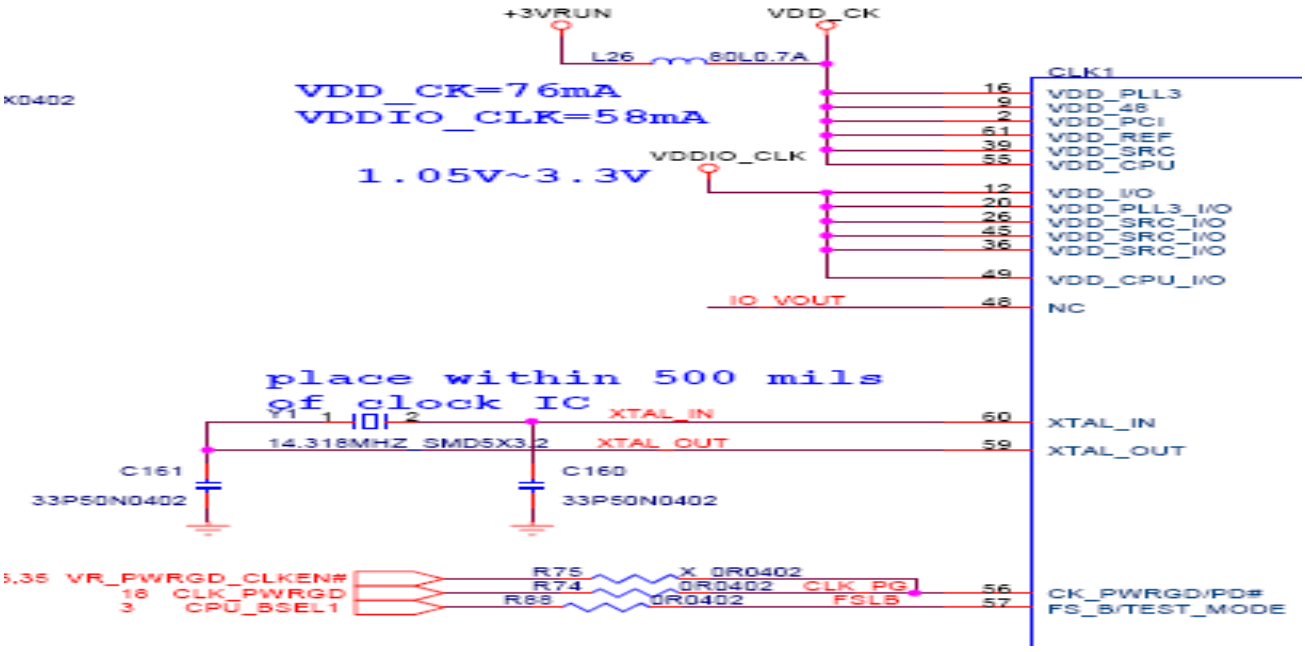


ELETRÔNICA

4. Check CLK_PWRGD whether is active or not.

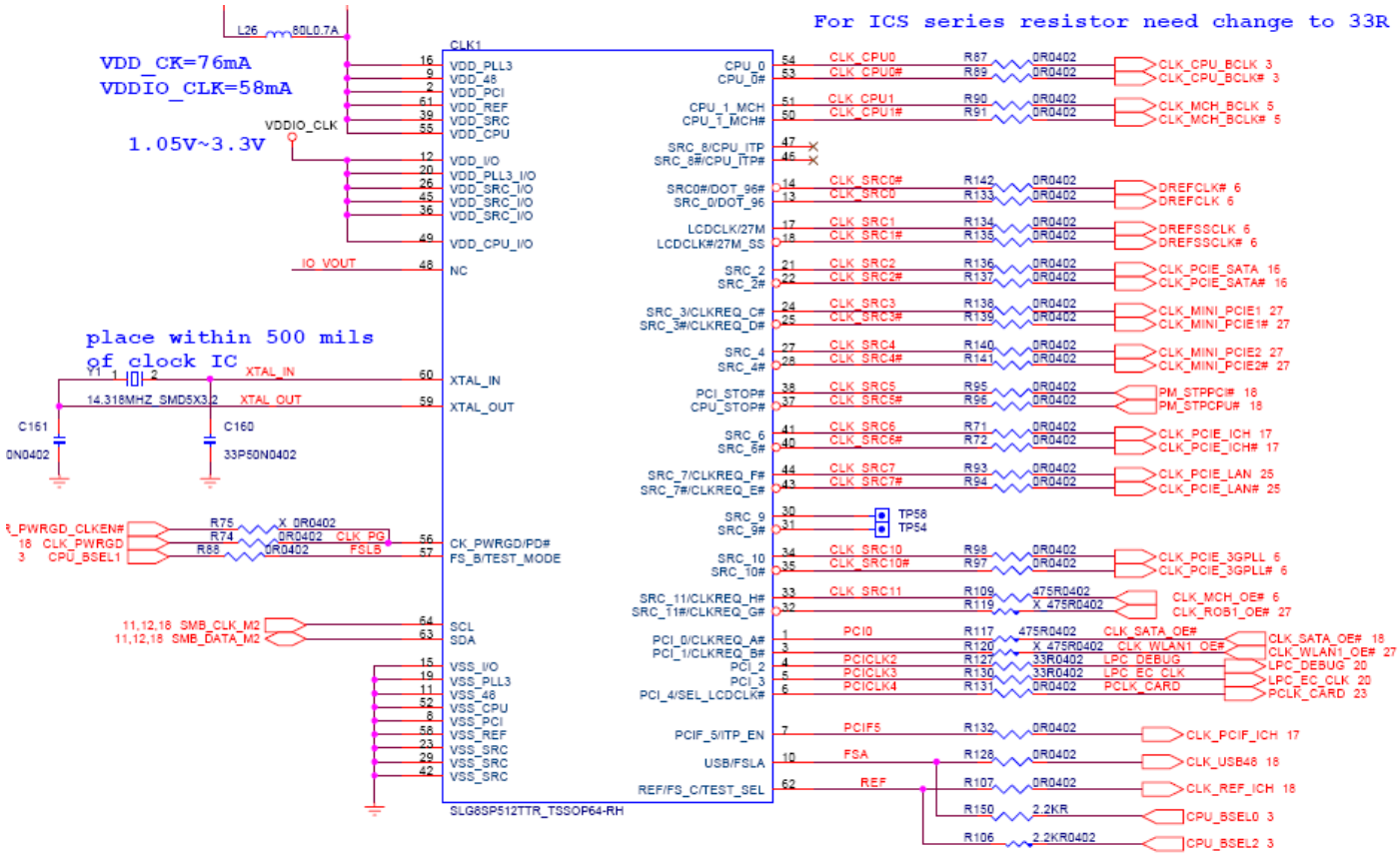
Item	Subject	Net name	Level	Measure Point
1	Control Signal	CLK_PWRGD	V	U28 _PIN F1
2	Control Signal	CLKPG	V	CLK1 pin56,R74





Check clocks of all frequency whether are active or not.

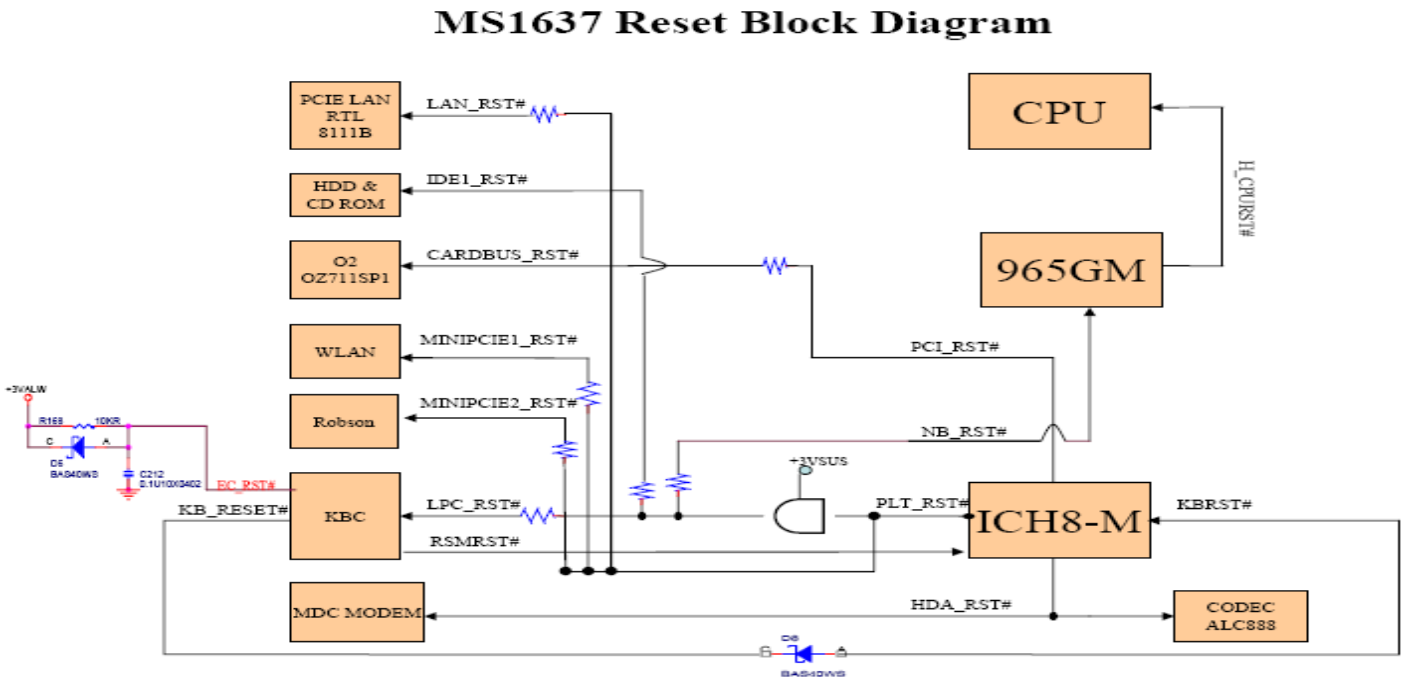
Item	Subject	Net name	Level	Measure Point	Notice
1	PCI Clocks	LPC_DEBUG	33.3MHZ	R127	
2	PCI Clocks	PCLK_CARD	33.3MHZ	R131	
3	PCI Clocks	LPC_EC_CLK	33.3MHZ	R130	
4	PCI Clocks	PCLK_ICH	33.3MHZ	R132	
5	14MHZ Clocks	XTAL_IN	14.318MHZ	Y1	
6	14MHZ Clocks	XTAL_OUT	14.318MHZ	Y1	
7	14MHZ Clocks	CLK_REF_ICH	14.318MHZ	R107	
8	48MHZ Clocks	CLK_USB48	48MHZ	R128	
9	Host clocks	CLK_CPU_BCLK	667/800MHZ	CLK1, PIN54	CPU_BSEL(2,1,0)=0,0,1
10	Host clocks	CLK_CPU_BCLK#	667/800MHZ	CLK1, PIN53	CPU_BSEL(2,1,0)=0,0,1
11	Host clocks	CLK_MCH_BCLK	667/800MHZ	CLK1, PIN51	CPU_BSEL(2,1,0)=0,0,1
12	Host clocks	CLK_MCH_BCLK#	667/800MHZ	CLK1, PIN50	CPU_BSEL(2,1,0)=0,0,1
13	SRC clocks	CLK_PCIE_3GPLL#	100MHZ	CLK1, PIN35	
14	SRC clocks	CLK_PCIE_3GPLL	100MHZ	CLK1, PIN34	
15	SRC clocks	CLK_PCIE_ICH	100MHZ	CLK1, PIN41	
16	SRC clocks	CLK_PCIE_ICH#	100MHZ	CLK1, PIN40	
17	SRC clocks	CLK_MINI_PCIE2	100MHZ	CLK1, PIN27	
18	SRC clocks	CLK_MINI_PCIE2#	100MHZ	CLK1, PIN28	
19	SRC clocks	CLK_MINI_PCIE1	100MHZ	CLK1, PIN24	
20	SRC clocks	CLK_MINI_PCIE1#	100MHZ	CLK1, PIN25	
21	SRC clocks	CLK_PCIE_SATA	100MHZ	CLK1, PIN21	
22	SRC clocks	CLK_PCIE_SATA #	100MHZ	CLK1, PIN22	
23	SRC clocks	DREFSSCLK	100MHZ	CLK1, PIN17	
24	SRC clocks	DREFSSCLK#	100MHZ	CLK1, PIN18	
25	96MHZ Clocks	DREFCLK	96MHZ	CLK1, PIN13	
26	96MHZ Clocks	DREFCLK#	96MHZ	CLK1, PIN14	



ELETRÔNICA

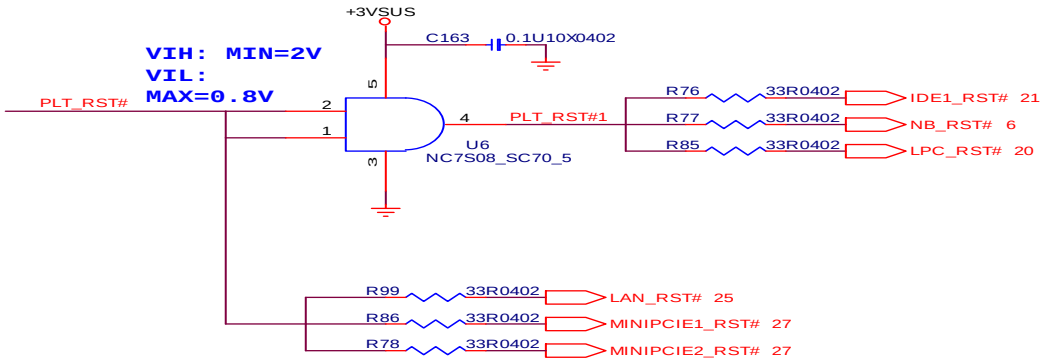
5、System Reset Map & Repair Flow Chart

If we find all power good signals of system is ready ,we must follow below steps for checking reset signals(RST#) whether is correct or not.



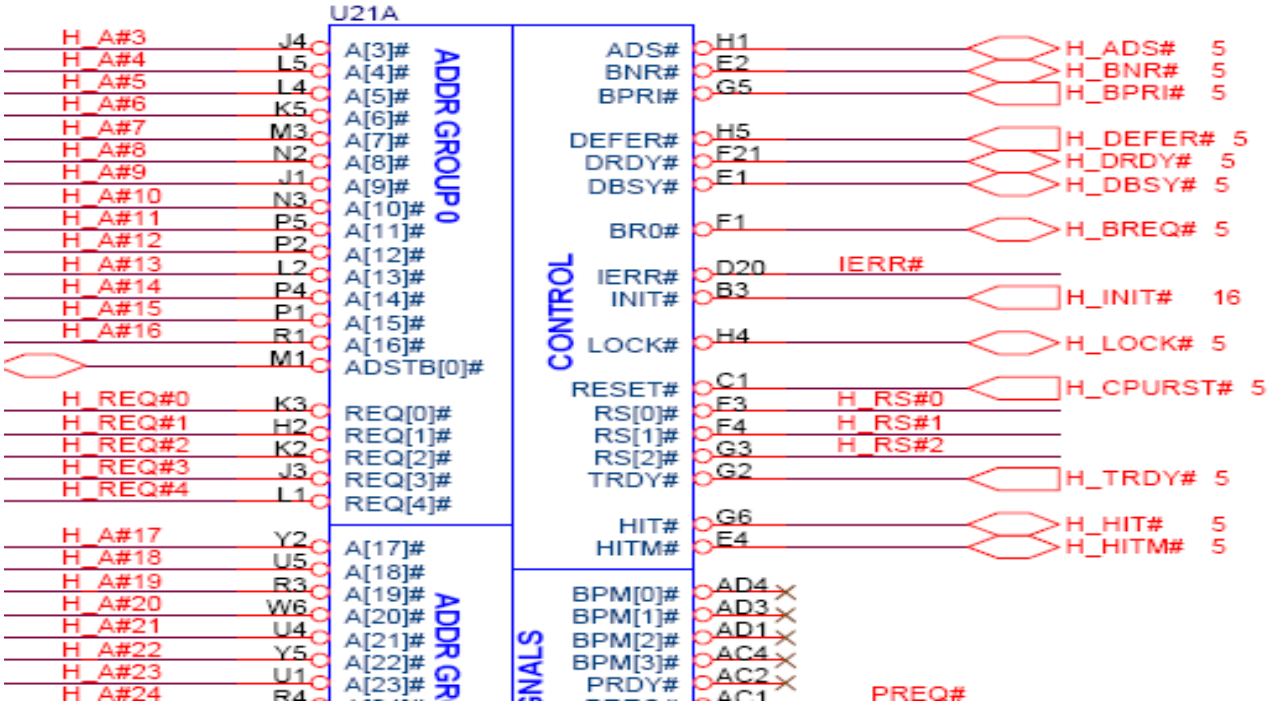
1. Check PLT_RST# and RST# of other devices from SB whether is active or not.

Item	Subject	Net name	Level	Measure Point
1	RST#	PLT_RST#	V	U6,PIN1
2	RST#	LPC_RST#	V	R85
3	RST#	MINIPCIE1_RST#	V	R86
4	RST#	MINIPCIE2_RST#	V	R78
5	RST#	IDE1_RST#	V	R76
6	RST#	NB_RST#	V	R77
7	RST#	LAN_RST#	V	R99



2. Check H_CPURST# for CPU whether is active or not.

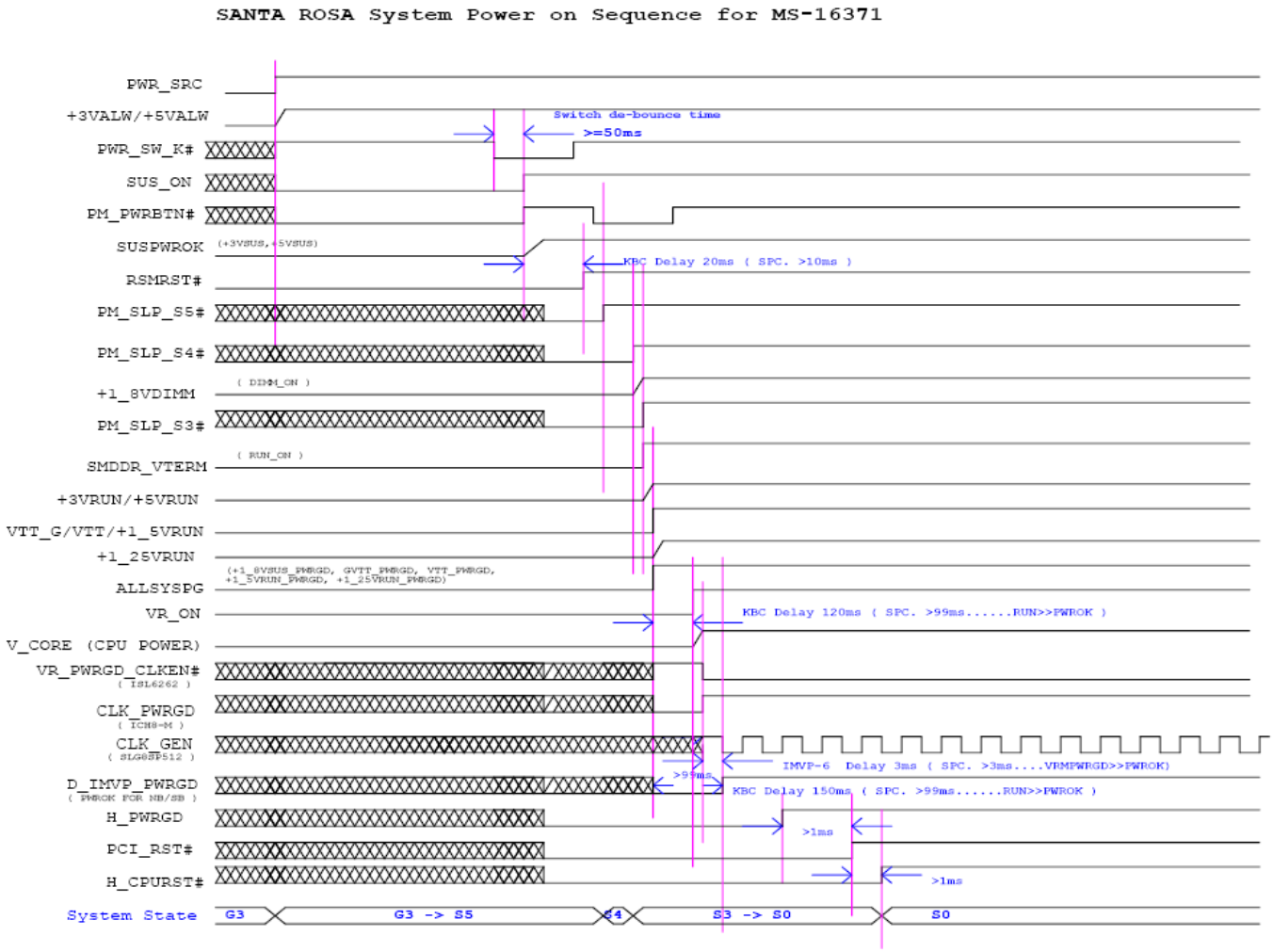
Item	Subject	Net name	Level	Measure Point
1	RST#	H_CPURST#	V	As below via



ELETRÔNICA

6、Power On Sequence

6.1 S5→ S0



7、AMI BIOS Check Point list

Following is the checkpoint list in AMIBIOS in order of execution.

1.Uncompressed INIT code checkpoints

Checkpoint	Description
D0	NMI is Disabled. CPU ID saved. Init code Checksum verification starting.
D1	To do DMA init, Keyboard controller BAT test, start memory refresh and going to 4GB flat mode.
D3	To start Memory sizing.
D4	To comeback to real mode. Execute OEM patch. Set stack.
D5	E000 ROM enabled. Init code is copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check <CTRL><HOME> key and verify main BIOS checksum. If either <CTRL><HOME> is pressed or main BIOS checksum is bad, go to check point E0 else go to check point D7.
D7	To pass control to Interface Module.
D8	Main BIOS runtime code is to be decompressed.
D9	Control to be passed to main BIOS in shadow RAM.

2. Boot Block Recovery Code Check Points

Checkpoint	Meaning
E0	On Board Floppy Controller (if any) is initialized. To start base 512K memory test.
E1	To initialize interrupt vector table.
E2	To initialize DMA and interrupt controllers.
E6	To enable floppy and timer IRQ, enable internal cache.
ED	Initialize floppy drive.
EE	Start looking for a diskette in drive A: and read 1st sector of the diskette.
EF	Floppy read error.
F0	Start searching AMIBOOT.ROM file in root directory.
F1	AMIBOOT.ROM file not present in root directory.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by AMIBOOT.ROM file.
F3	Start reading AMIBOOT.ROM file cluster by cluster.
F4	AMIBOOT.ROM file not of proper size.
F5	Disable internal cache.
FB	Detect Flash type present.
FC	Erase Flash.
FD	Program Flash.
FF	Flash program successful. BIOS is going to restart.

3.Runtime code is uncompressed in F000 shadow ram

Checkpoint	Meaning
03	NMI is Disabled. To check soft reset/power-on.
05	BIOS stack set. Going to disable Cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin-23,24 blocking/unblocking command.
11	Going to check pressing of <INS> , <END> key during power-on.
12	To init CMOS if nit CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers.
13	Video display is disabled and port-B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.

ELETRÔNICA

1A	Memory Refresh line is toggling. Going to check 15us ON/OFF time.
23	To read 8042 input port and disable Megakey Green PC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization about to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different BUSes init (system, static, output devices) to start if present. *(Please see Appendix for details of different BUSes).*
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power on message.
38	Different BUSes init (input, IPL, general devices) to start if present. *(Please see Appendix for details of different BUSes).*
39	Display different BUSes initialization error messages. *(Please see Appendix for details of different BUSes).*
3A	New cursor position read and saved. To display the Hit <DEL> message.
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M memory.
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point# 4Eh).
4C	Memory below 1M cleared.(SOFT RESET) Going to clear memory above 1M.
4D	Memory above 1M cleared.(SOFT RESET) Going to save the memory size. (Goto check point# 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64k memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation/ shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1M to follow.
52	Memory testing/initialization above 1M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. clearing output buffer, checking for stuck key, to issue keyboard reset command.

81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written, Global data init done. To check for lock-key.
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
95	Init of different BUSes optional ROMs from C800 to start. *(Please see Appendix-I for details of different BUSes).*
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before Coprocessor test.
9C	Required initialization before Coprocessor is over. Going to initialize the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after Coprocessor test is complete. Going to check extd keyboard, keyboard ID and num-lock. Keyboard ID command to be
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	To build MP table if needed.
AC	To uncompress DMI data and execute DMI POST init.
B0	System configuration is displayed.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT-19 boot loader.

ELETRÔNICA