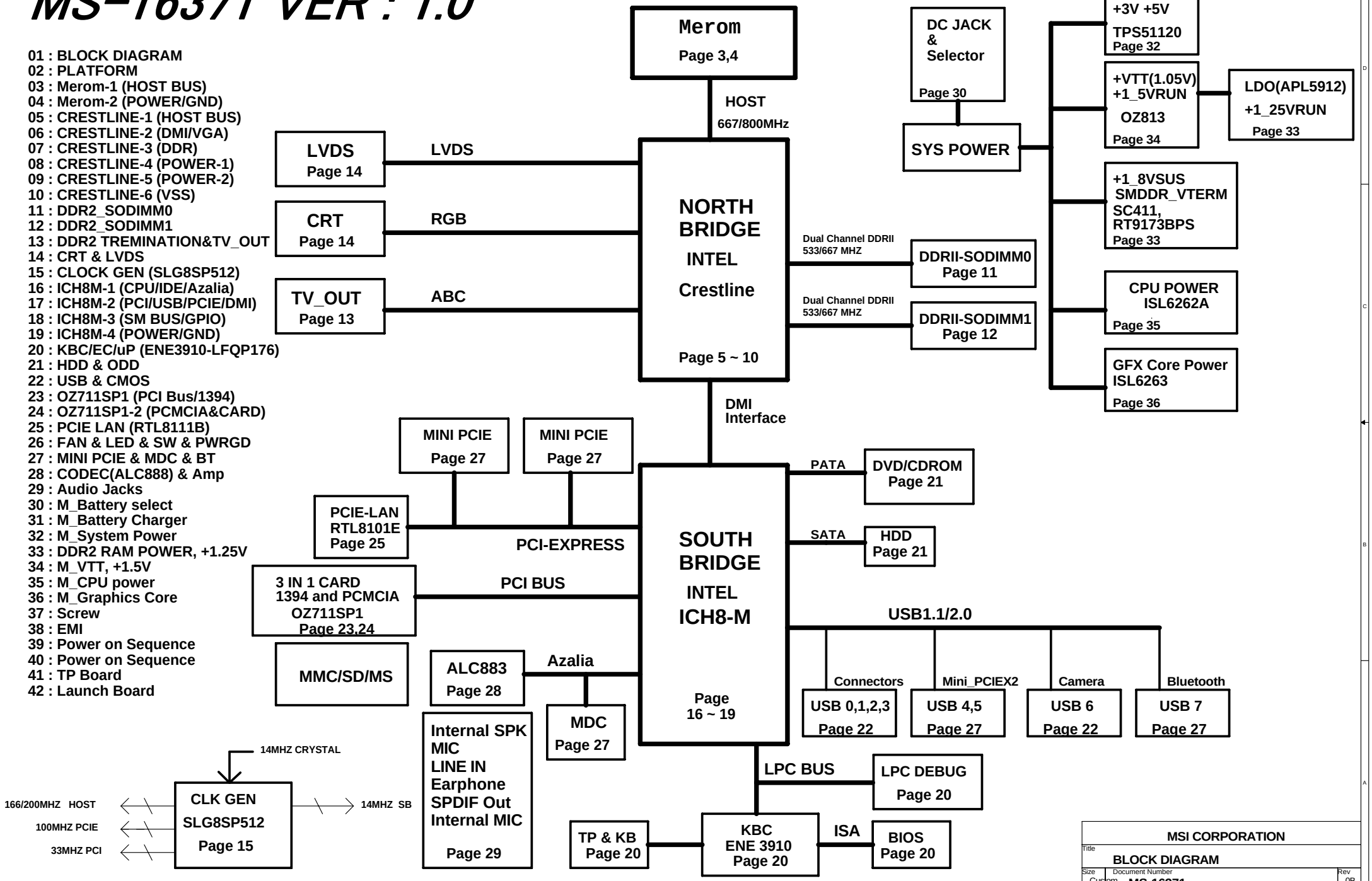
MS-16371 VER : 1.0



MSI CORPORATION

Title: BLOCK DIAGRAM

Size: Custom | Document Number: MS-16371 | Rev: 0B

Date: Thursday, February 15, 2007 | Sheet 1 of 42

Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
VHCORE	Core Voltage for Processor	VR_ON
+VTT	1.05 rail for Processor & 965GM I/O	PM_SLP_S3# (RUN_ON)
+1_5VRUN	1.5V switched power rail(off in S3-S5)	PM_SLP_S3# (RUN_ON)
+1_25VRUN	1.25V powe rail NB PLL and PXE (off in S3-S5)	+1_5VRUN
+3VRUN	3.3V switched power rail(off in S3-S5)	RUND (RUN_ON)
+5VRUN	5.0V switched power rail(off in S3-S5)	RUND (RUN_ON)
SMDDR_VTERM	0.9V DDR Termination voltage (off in S4-S5)	PM_SLP_S3# (RUN_ON)
+1_8VDIMM	1.8V power rail DDR (off in S4-S5)	PM_SLP_S4# (DIMM_ON)
+3VSUS	3.3V power rail (off in S4-S5)	SUS_ON
+5VSUS	5.0V power rail (off in S4-S5)	SUS_ON
+3VALW	3.3V always on power rail	PWR_SRC
+5VALW	5.0V always on power rail	PWR_SRC
+V5_AUDIO	5.0V Power rail Audio codec(off in S3-S5)	RUND
VTT_G	Core Voltage for GMCH GPU	GFX_VR_EN

System Power consumption	
CPU Vcore	40W
3V	15W
5V	25W
Graphics Vcore	10W
1.5V	7W
1.05V	10W
PWR_SRC	107W(12A)

POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*SUS	+V*RUN	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V*SUS will always keep high

MSI CORPORATION

Title: PLATFORM

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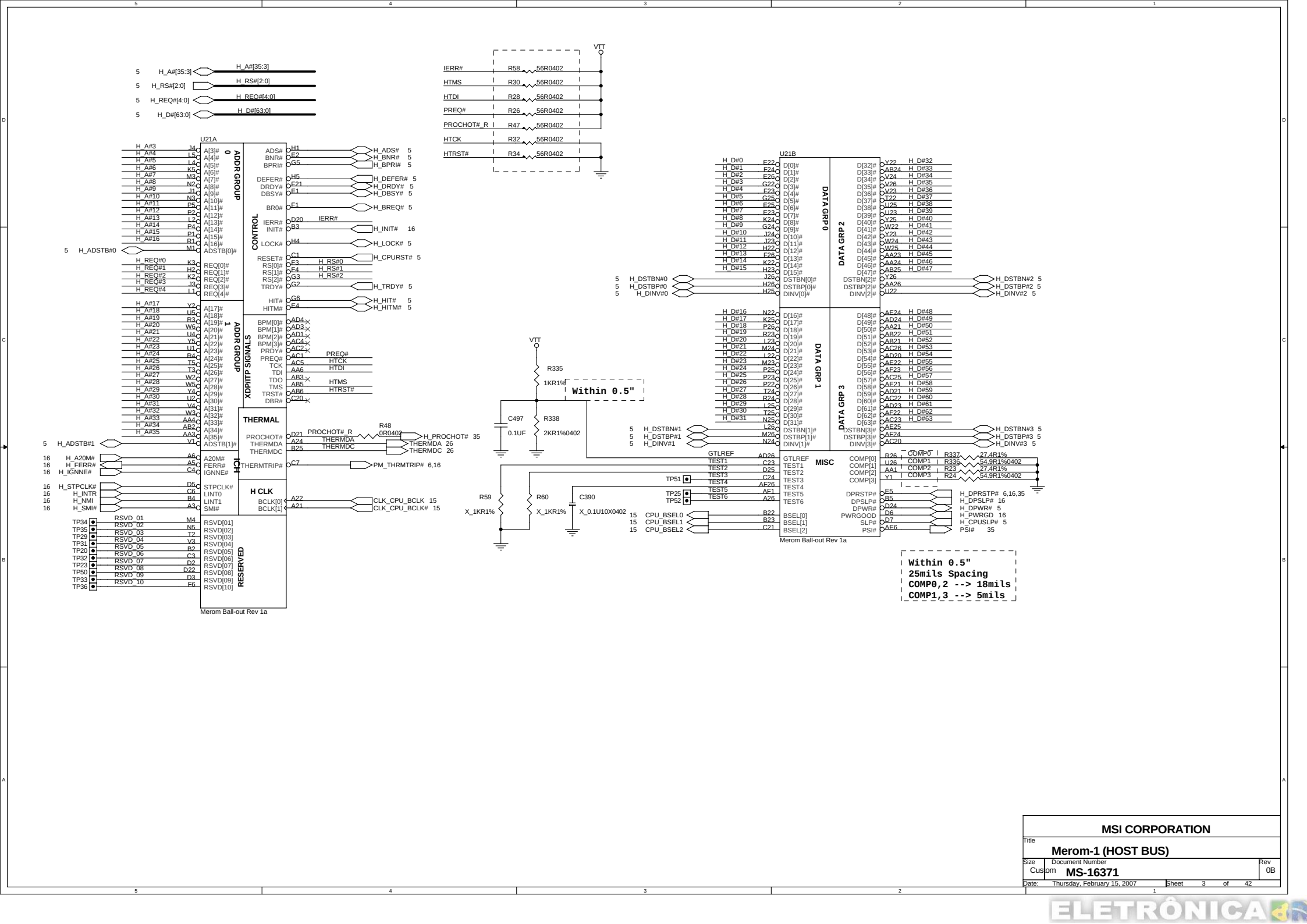
Date: Thursday, February 15, 2007 | Sheet 2 of 42


H_A#[35:3]
H_RS#[2:0]
H_REQ#[4:0]
H_D#[63:0]
VTT
IERR# R58 56R0402
HTMS R30 56R0402
HTDI R28 56R0402
PREQ# R26 56R0402
PROCHOT#_R R47 56R0402
HTCK R32 56R0402
HTRST# R34 56R0402
U21A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
Merom Ball-out Rev 1a
U21B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
Merom Ball-out Rev 1a
R335 1KR1%
Within 0.5"
C497 0.1UF
R338 2KR1%0402
R59 X_1KR1%
R60 X_1KR1%
C390 X_0.1U10X0402
R48 0R0402
Within 0.5"
25mils Spacing
COMP0,2 --> 18mils
COMP1,3 --> 5mils
MSI CORPORATION
Merom-1 (HOST BUS)
Custom
MS-16371
0B
Date: Thursday, February 15, 2007
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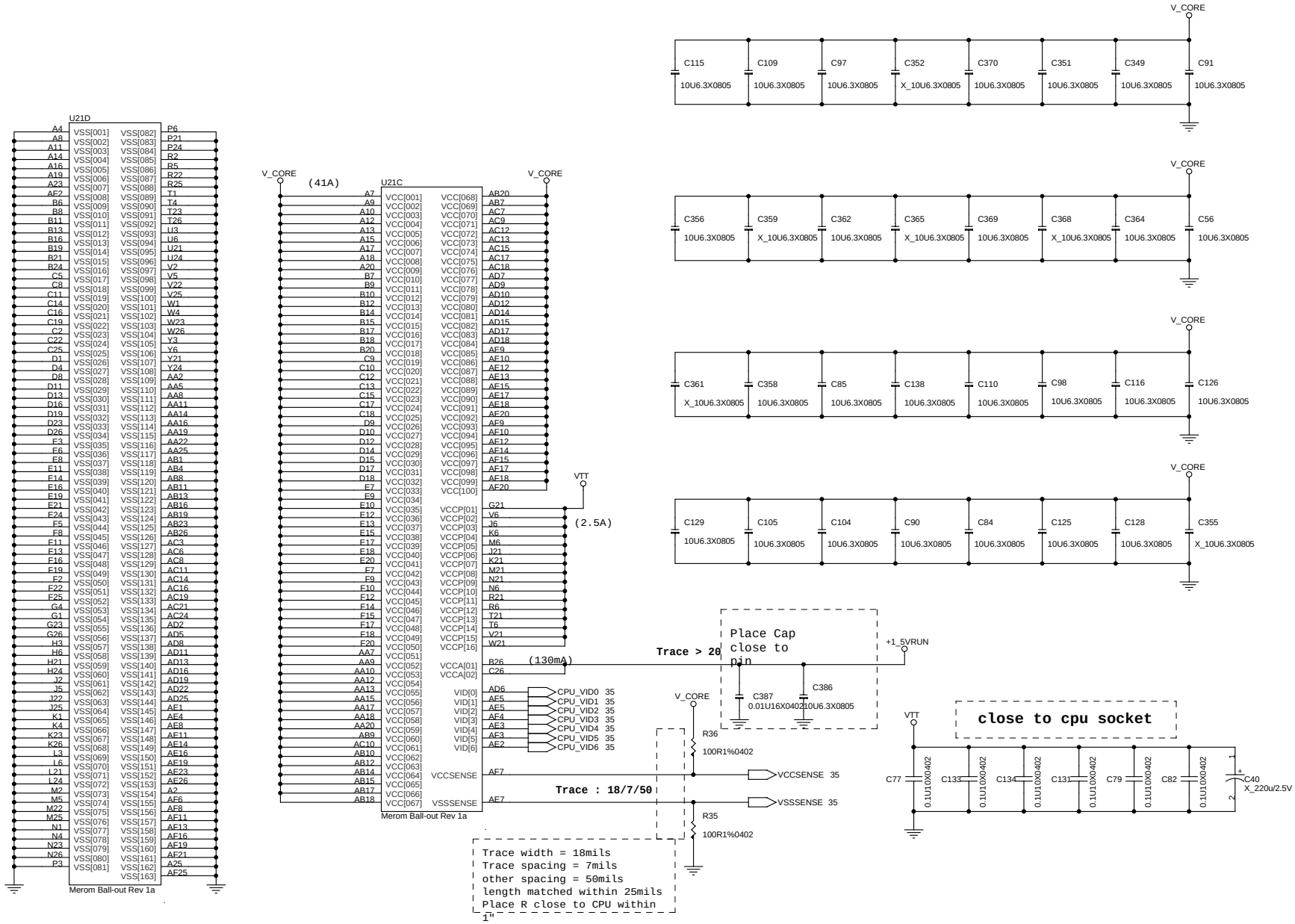
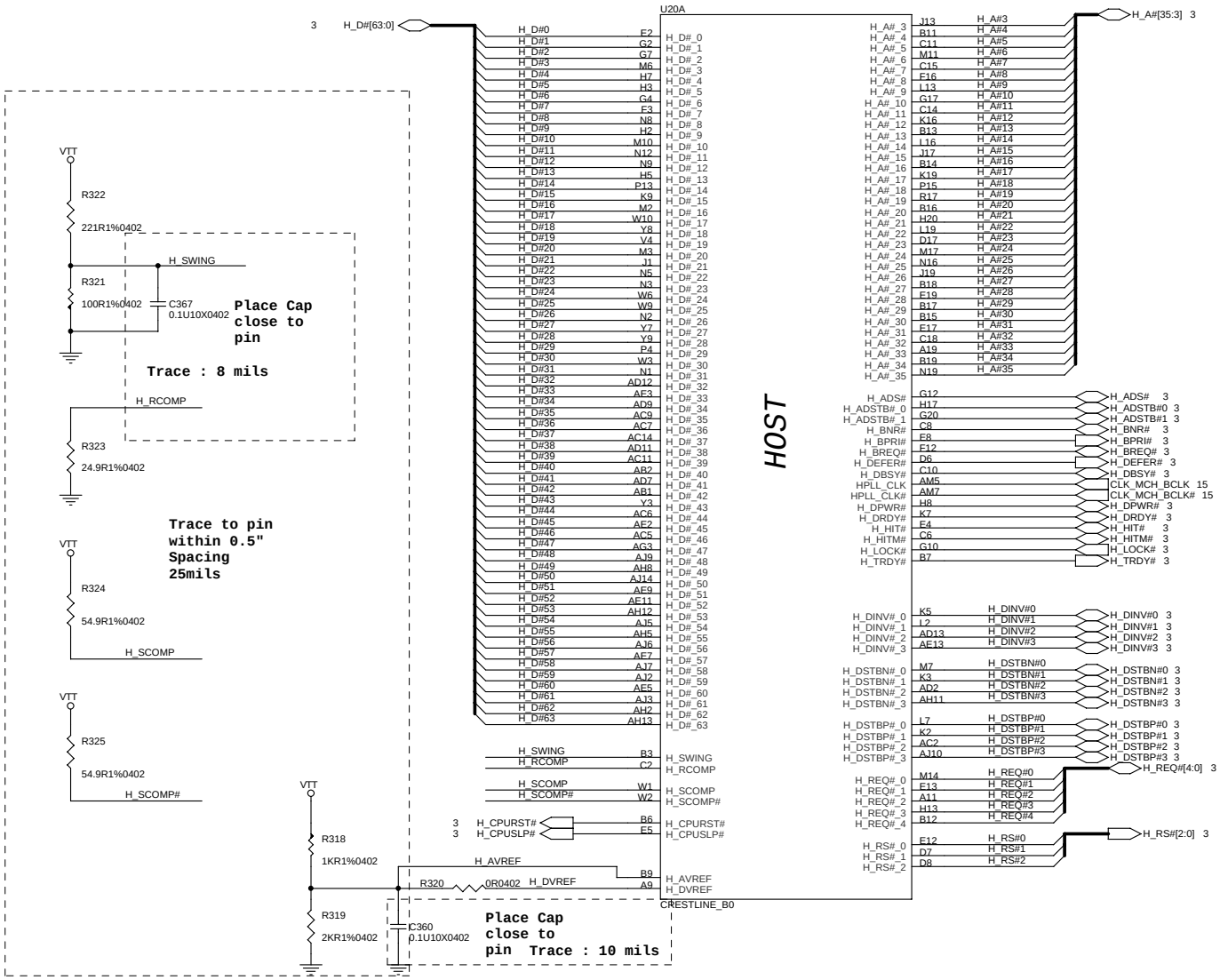


MSI CORPORATION		
Title: Merom-2 (POWER/GND)		
Size: Custom	Document Number: MS-16371	Rev: 0B
Date: Thursday, February 15, 2007	Sheet 4 of 42	



MSI CORPORATION	
Title	CRESTLINE-1 (HOST BUS)
Size: Custom	Document Number: MS-16371
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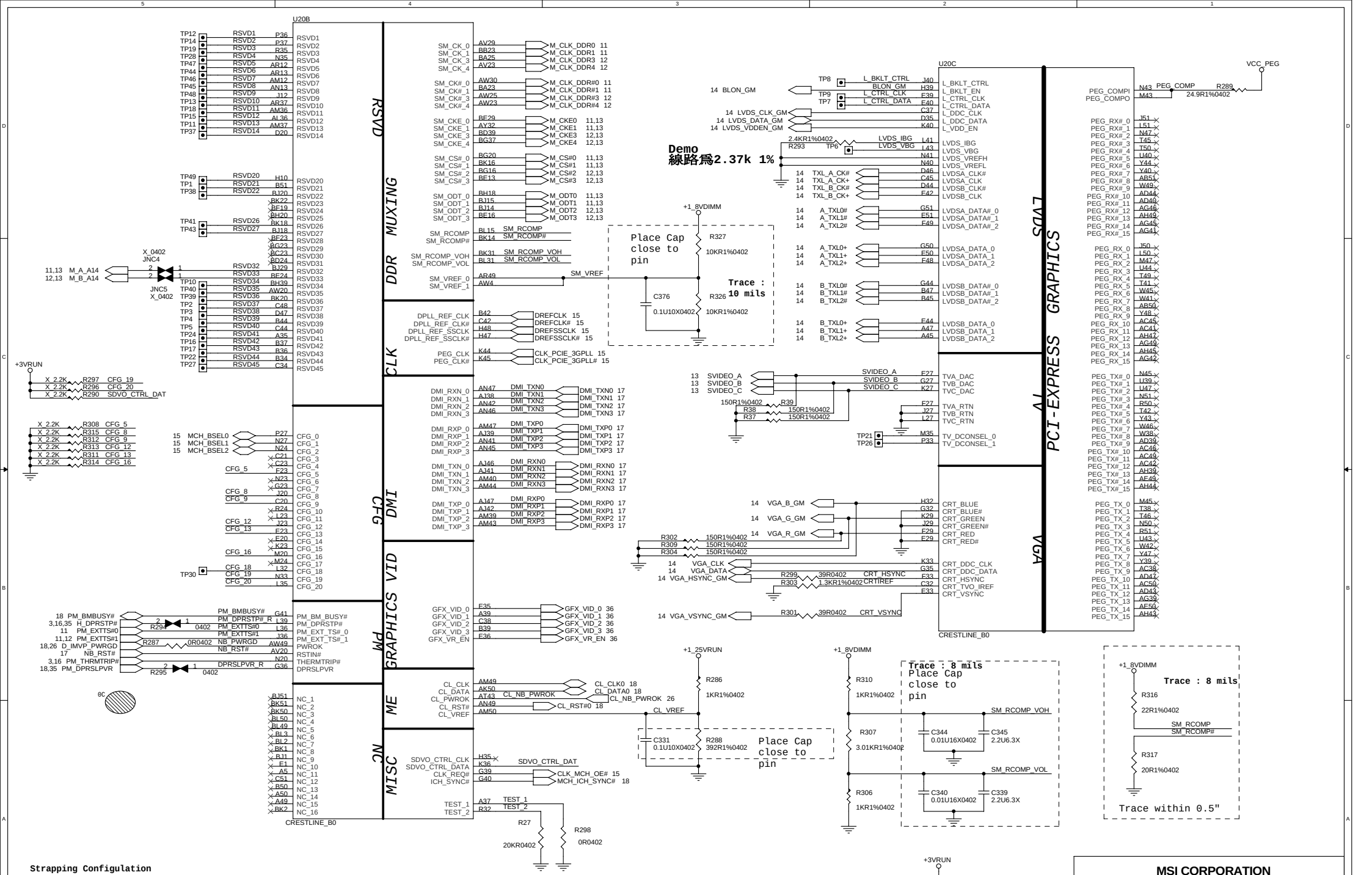
Date: Thursday, February 15, 2007	Sheet 5 of 42



Strapping Configulation

CFG5 (Default=High)	CFG9 (Default=High)	CFG16 (Default=High)	CFG19 (Default=Low)	CFG20 (Default=Low)	SDVO_CTRL_DATA(Default=Low)
DMI*4==>High DMI*2==>Low	PCIE Graphics Lane: Normal Operation	Dynamic ODT Enabled	DMI Lane Reversal: Normal Operation	Only SDVO or PCIE is operational	SDVO present Low=No SDVO Card Present

MSI CORPORATION

Title: **CRESTLINE-2 (DMI/VGA)**

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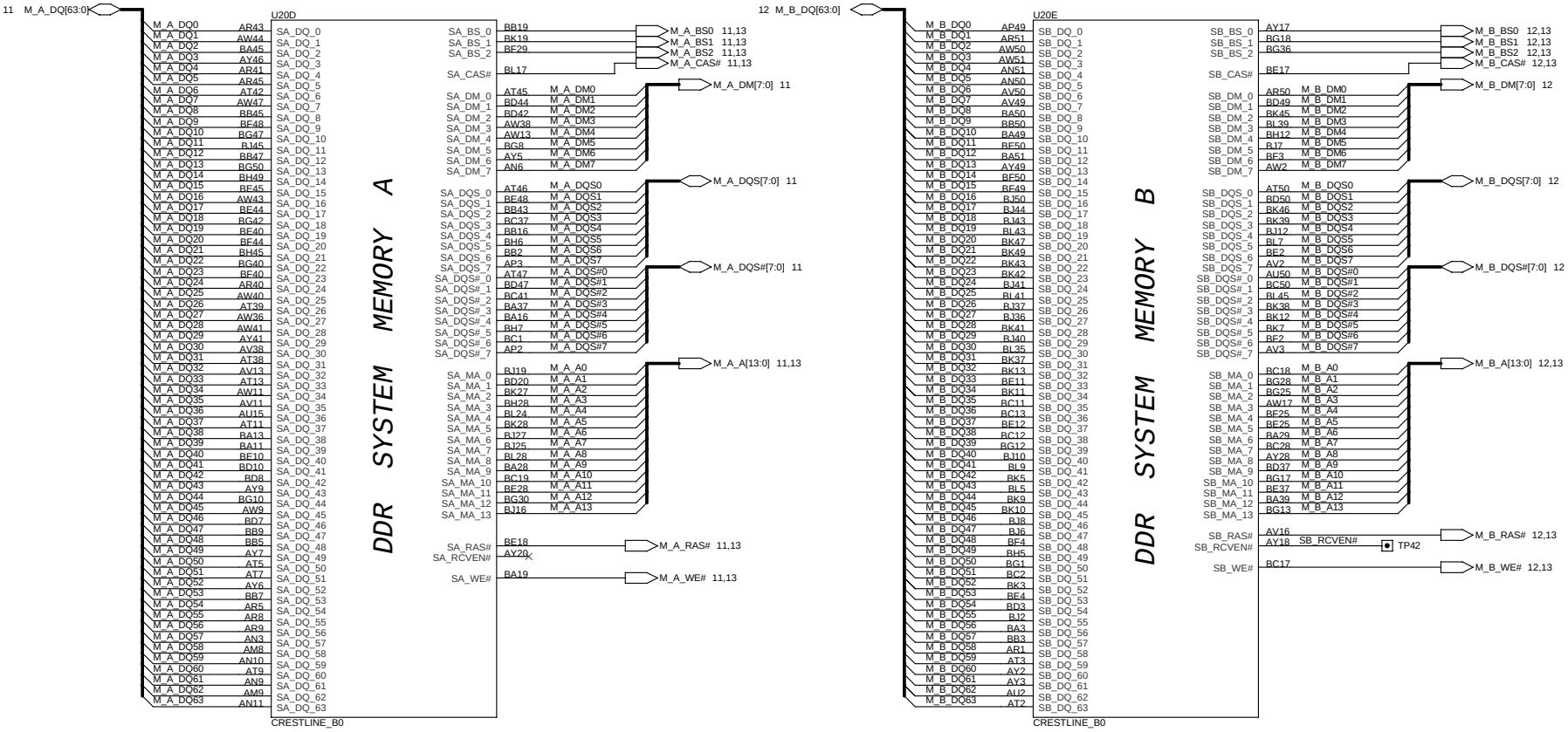
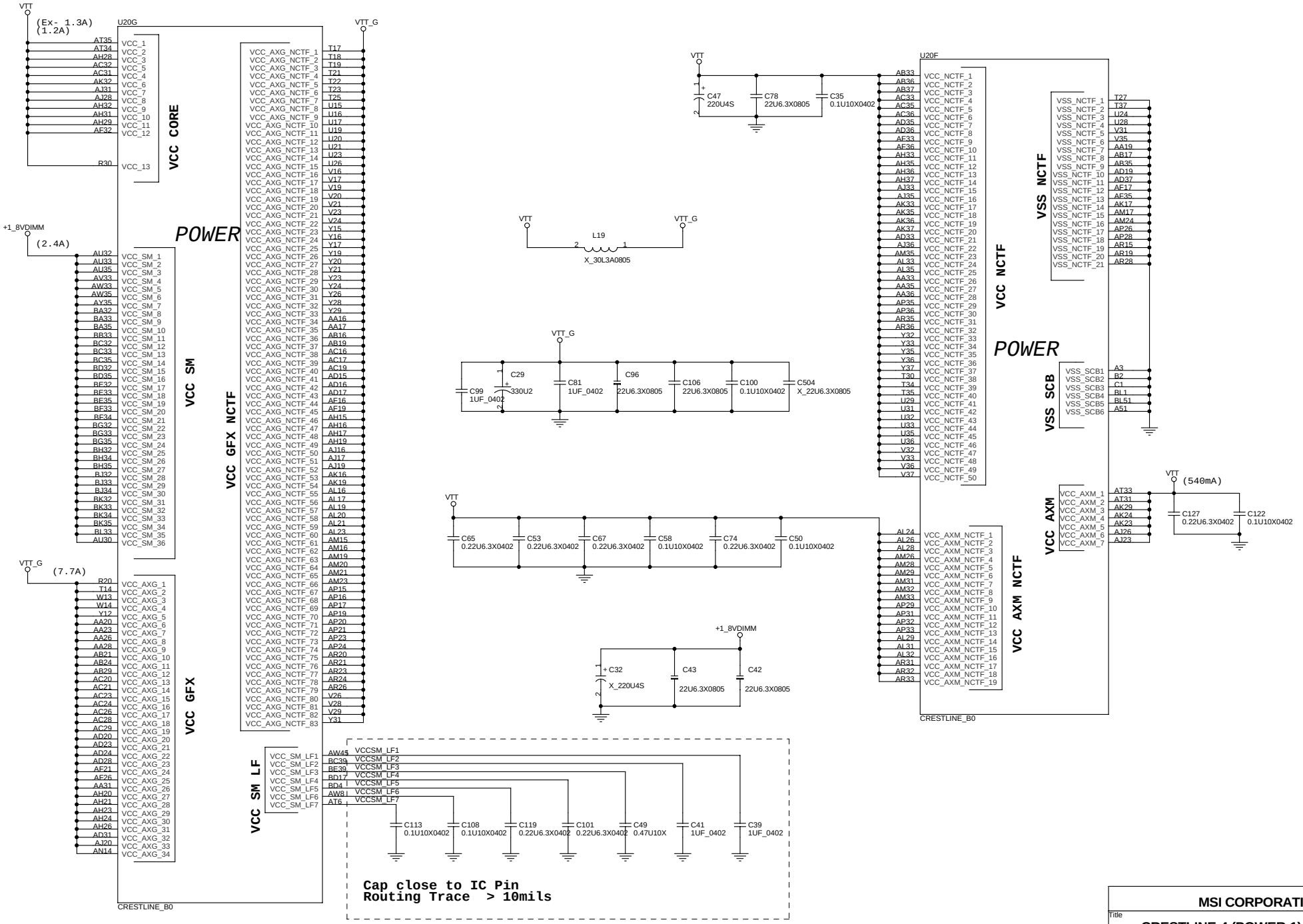


MSI CORPORATION			
Title: CRESTLINE-3 (DDR)			
Size: Custom	Document Number: MS-16371		Rev: 0B
Date: Thursday, February 15, 2007	Sheet 7 of 42		



Title	MSI CORPORATION
	CRESTLINE-4 (POWER-1)
Size	Custom
Document Number	MS-16371
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Date:	Thursday, February 15, 2007
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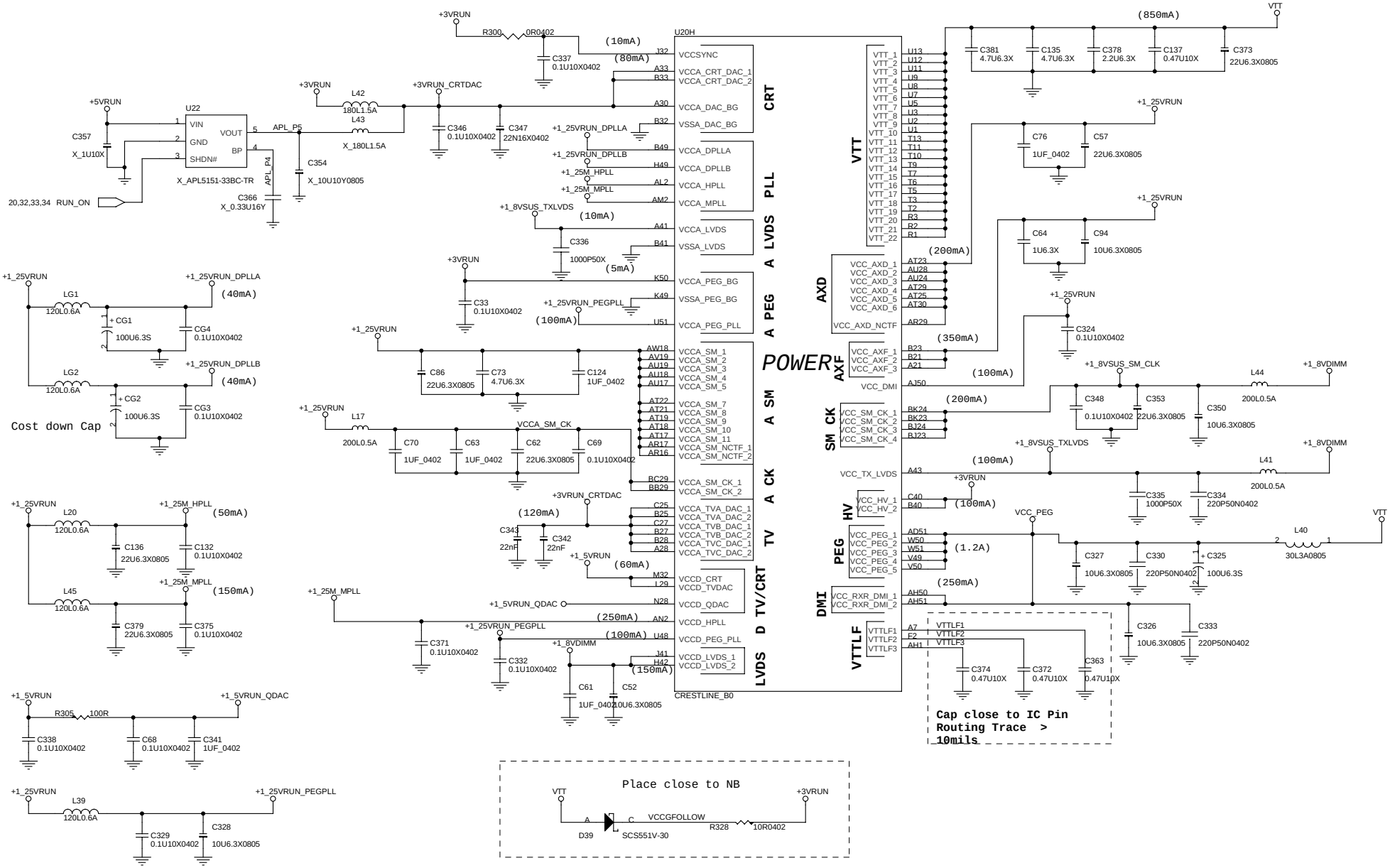
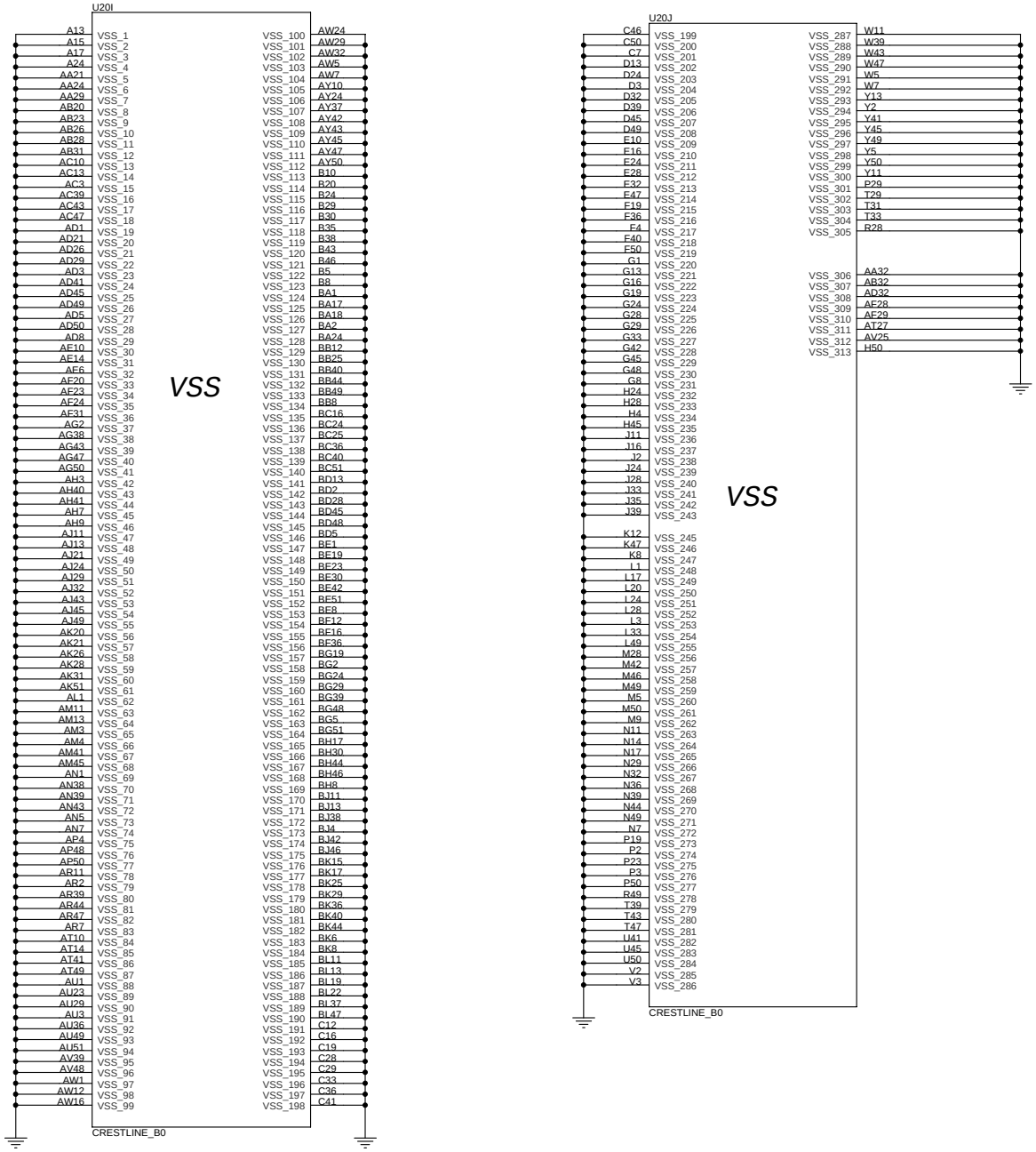


MSI CORPORATION	
Title	CRESTLINE-5 (POWER-2)
Size: Custom	Document Number: MS-16371
Rev	0B
Date: Thursday, February 15, 2007	Sheet 9 of 42



Title	**CRESTLINE-6 (VSS)**
Size	Custom
Document Number	**MS-16371**
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Date:	Thursday, February 15, 2007
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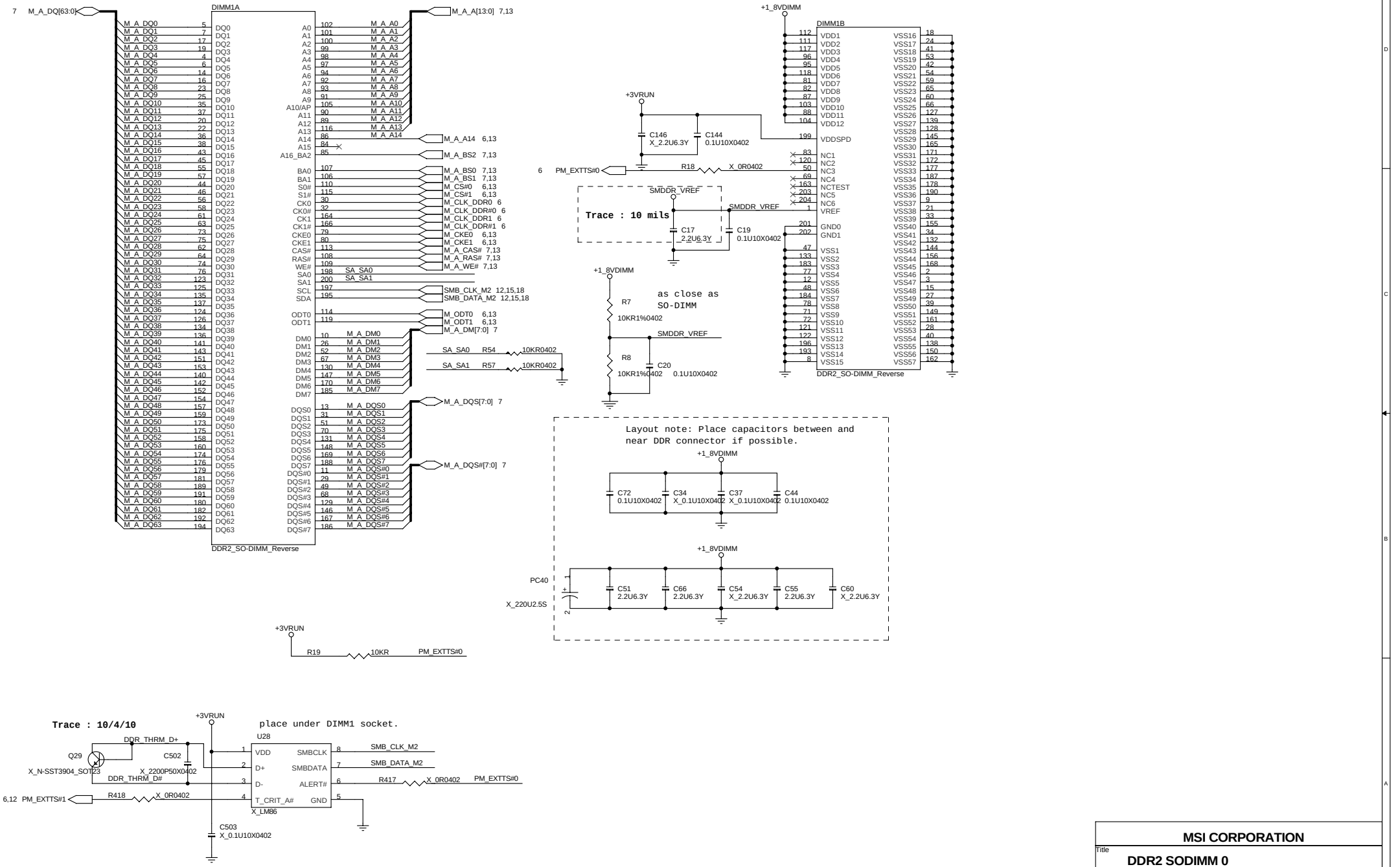
MSI CORPORATION



Title	DDR2 SODIMM 0
Size	Custom
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Date:	Thursday, February 15, 2007
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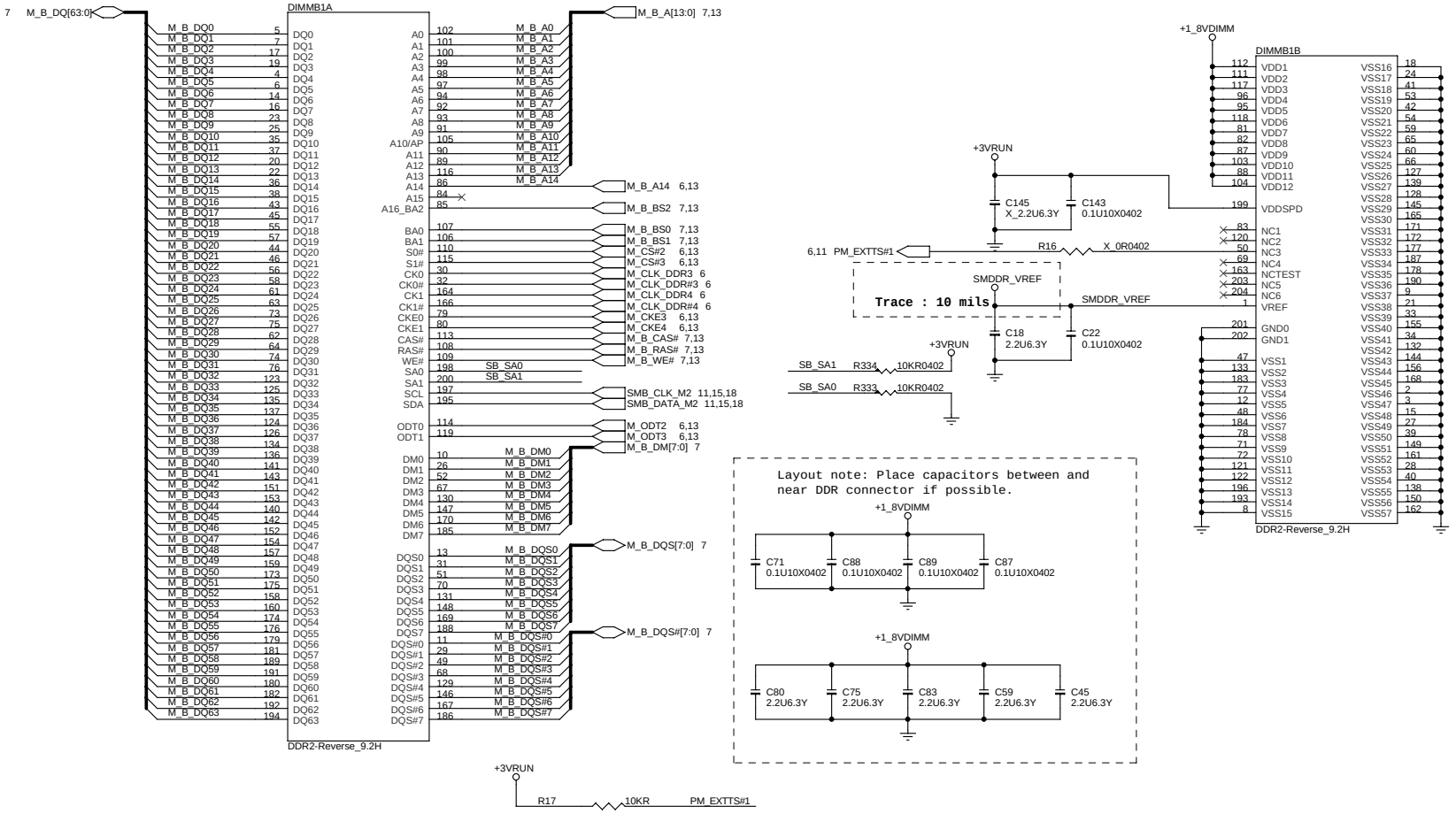
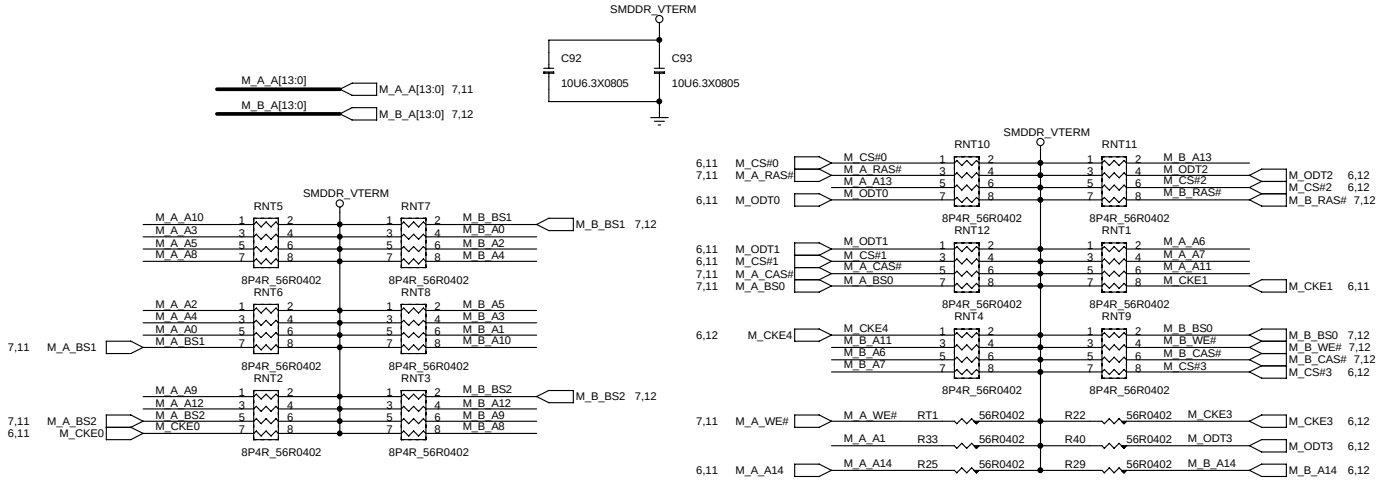
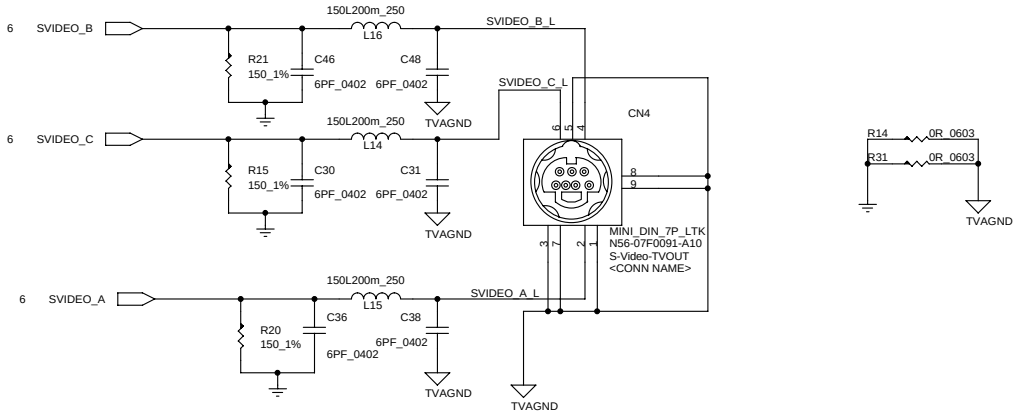
MSI CORPORATION



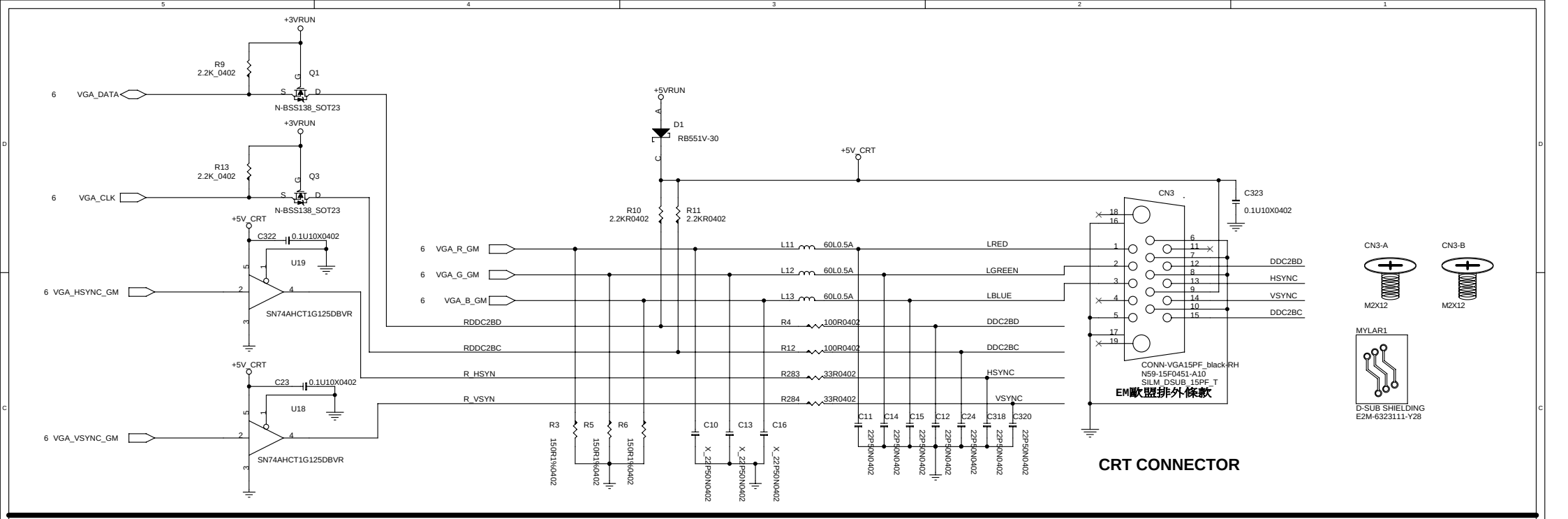
MSI CORPORATION		
Title: DDR2 SODIMM 1		
Size: Custom	Document Number: MS-16371	Rev: 0B
Date: Thursday, February 15, 2007	Sheet 12 of 42	

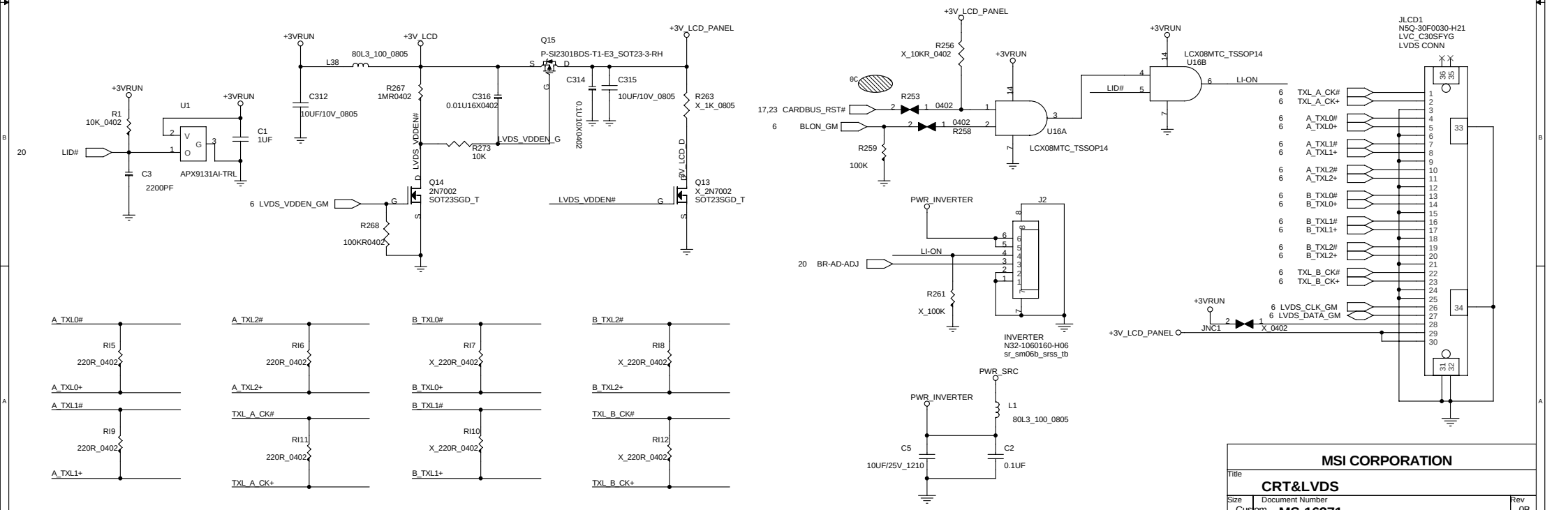


Video Filter SPEC:
C=6pF+/-20%,16V,0603
L=150ohm@100MHz,100mA(min)



MSI CORPORATION		
Title: DDR2 TREMINATION&TV_OUT		
Size: Custom	Document Number: MS-16371	Rev: 0B
Date: Thursday, February 15, 2007	Sheet 13 of 42	



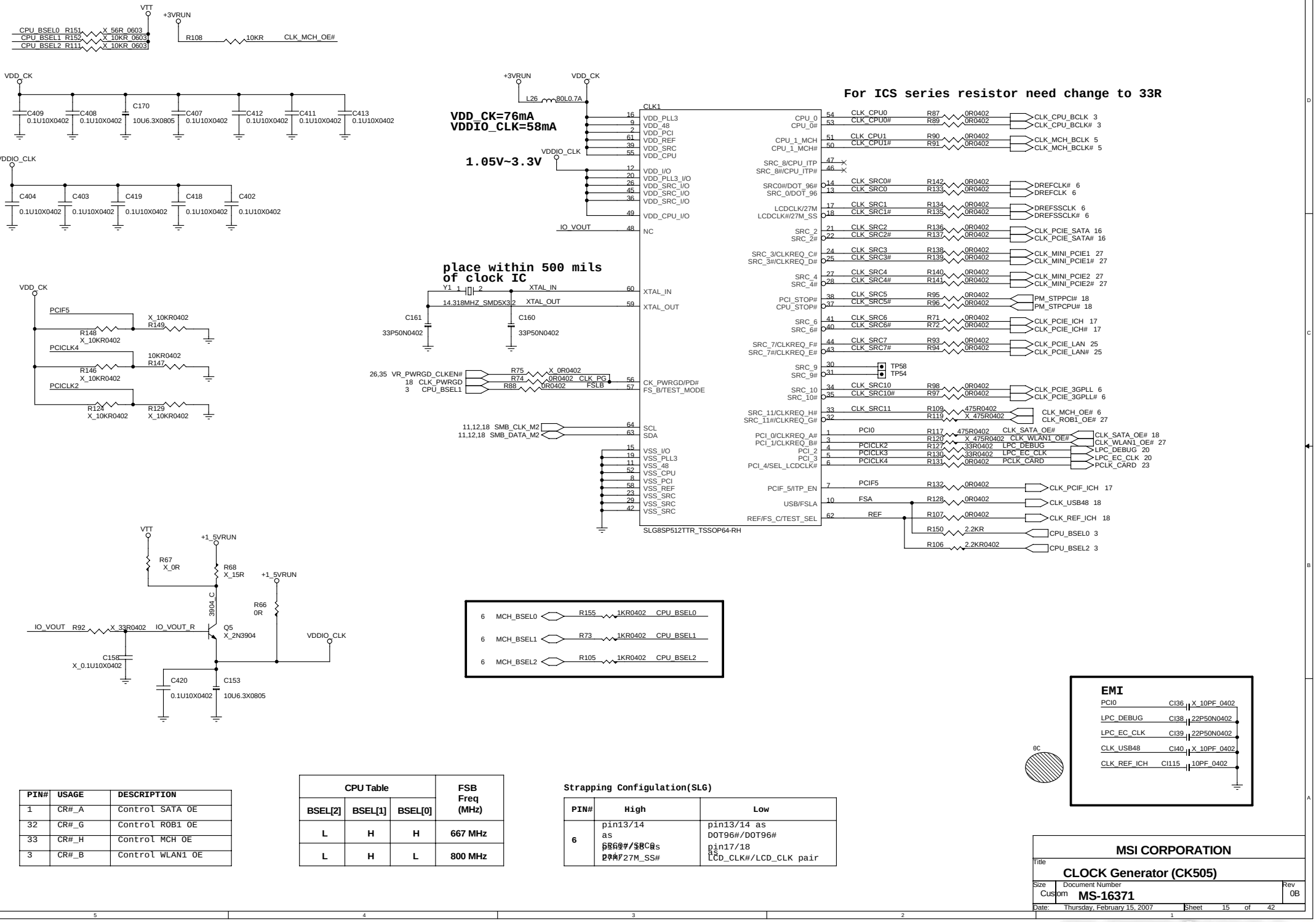


MSI CORPORATION

Title: **CRT&LVDS**

Size	Document Number	Rev
Custom	MS-16371	0B

Date: Thursday, February 15, 2007 Sheet 14 of 42



PIN#	USAGE	DESCRIPTION
1	CR#_A	Control SATA OE
32	CR#_G	Control ROB1 OE
33	CR#_H	Control MCH OE
3	CR#_B	Control WLAN1 OE

CPU Table			FSB Freq (MHz)
BSEL[2]	BSEL[1]	BSEL[0]	
L	H	H	667 MHz
L	H	L	800 MHz

Strapping Configulation(SLG)

PIN#	High	Low
6	pin13/14 as DOT96#/DOT96# pair	pin13/14 as DOT96#/DOT96# pair
	pin17/18 as LCDCLK#/27M_SS# pair	pin17/18 as LCD_CLK#/LCD_CLK pair

Title	MSI CORPORATION
	CLOCK Generator (CK505)
Size	Custom
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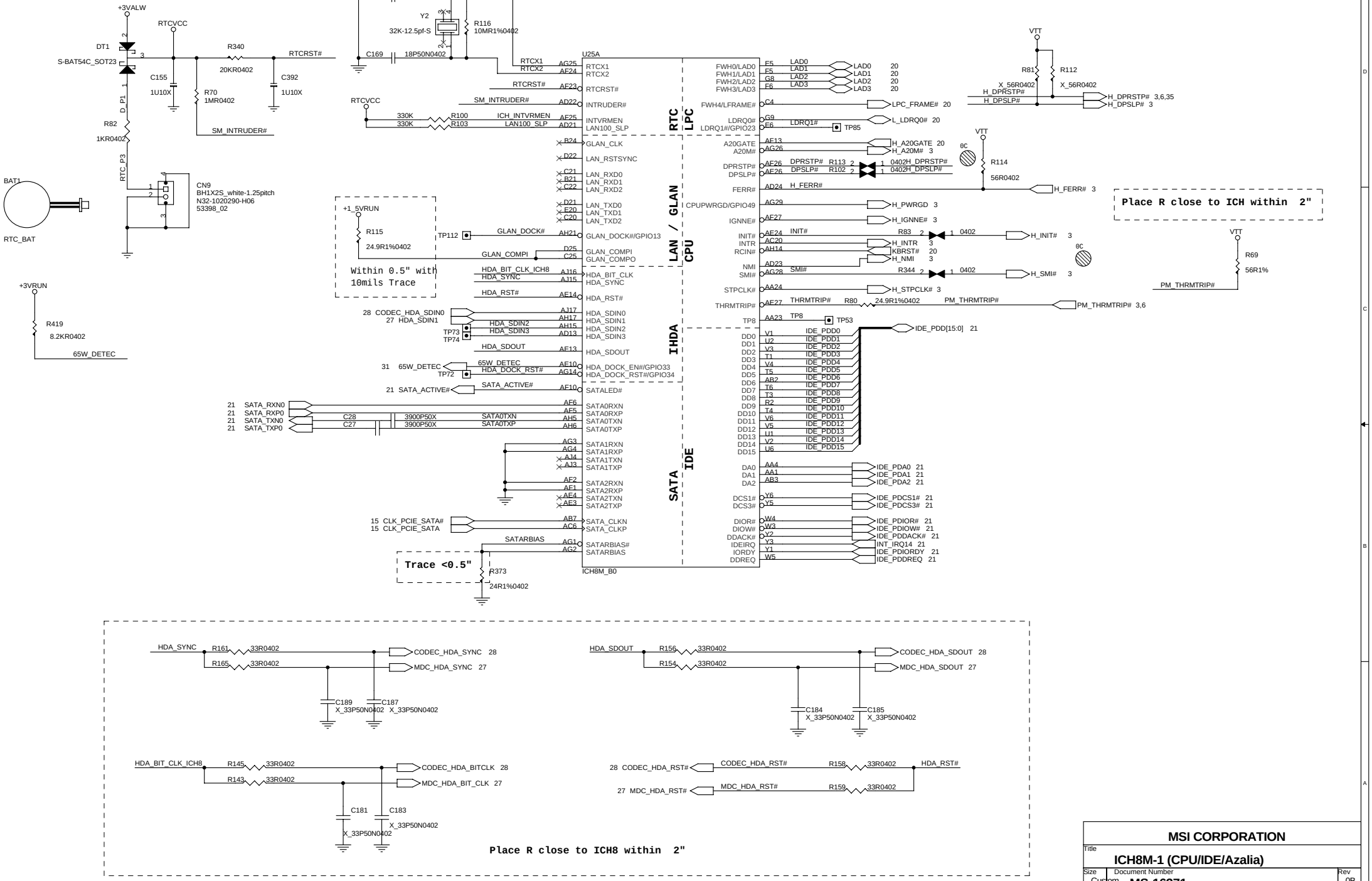
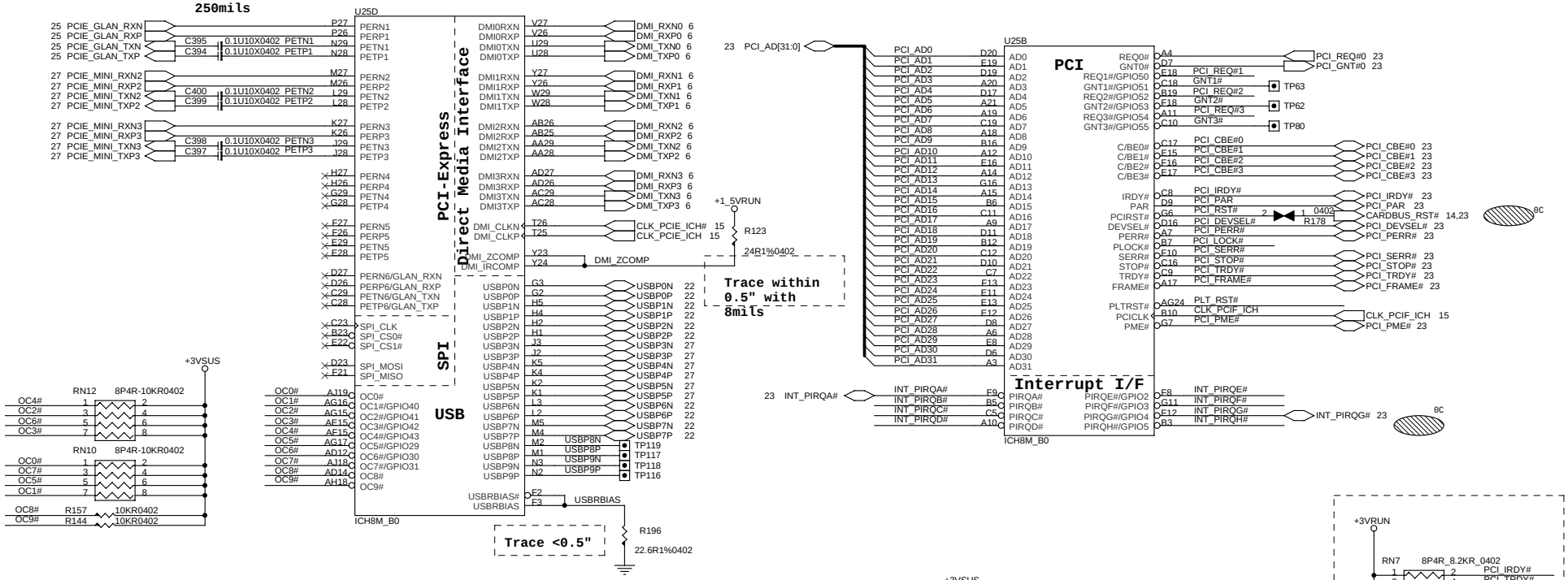
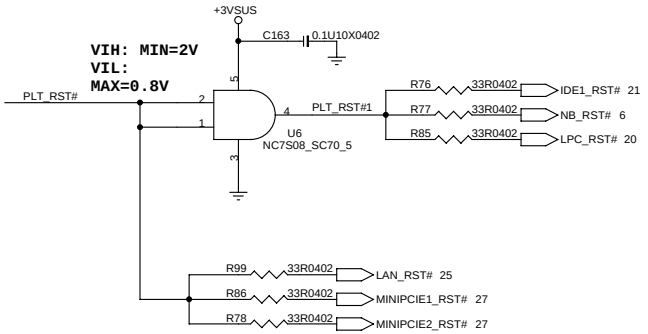
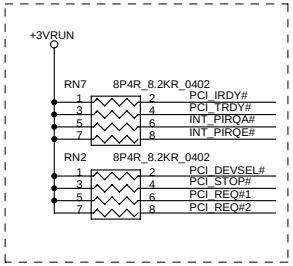
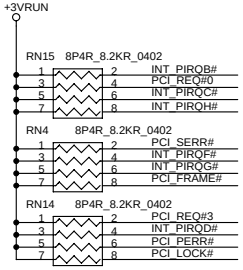


MSI CORPORATION		
Title: ICH8M-1 (CPU/IDE/Azalia)		
Size: Custom	Document Number: MS-16371	Rev: 0B
Date: Thursday, February 15, 2007	Sheet 16 of 42	









Strapping Configulation

HDA_SDOUT (Default=Low)	HDA_SYNC (Default=Low)	GNT2# (Default=High)	GPIO20 (Default=Low)	GNT1#/GPIO51 (Default=High)	GNT3# (Default=High)	GNT0#/SPI_CS1# (Default=High)
XOR chain testing==>Low Set bit 1 of RPC.PC==>High	Set bit 0 of RPC.PC	Set bit 2 of RPC.PC2	Reserved	ESI Strap (server only)	Top-block swap mode ==>Low	Boot BIOS destination selection

INTVRMEN	LAN100_SLP	SATALED# (Default=High)	SPKR (Default=Low)	TP3 (Default=High)	GPIO33/HDA_DOCK_EN# (Default=High)
Enable integrated Vccsus1_05, Vccsus1_5,VccCL1_5==High	Enable integrated VccLAN11_05,VccCL1_05==High	Set bit 27 of MPC.LR	No Reboot mode==>High	XOR chain Entrance	Flash Descriptor Security overridden==>Low Flash Descriptor will be in effect==>High

MSI CORPORATION

Title: ICH8M-2 (PCI/USB/PCIE/DMI)

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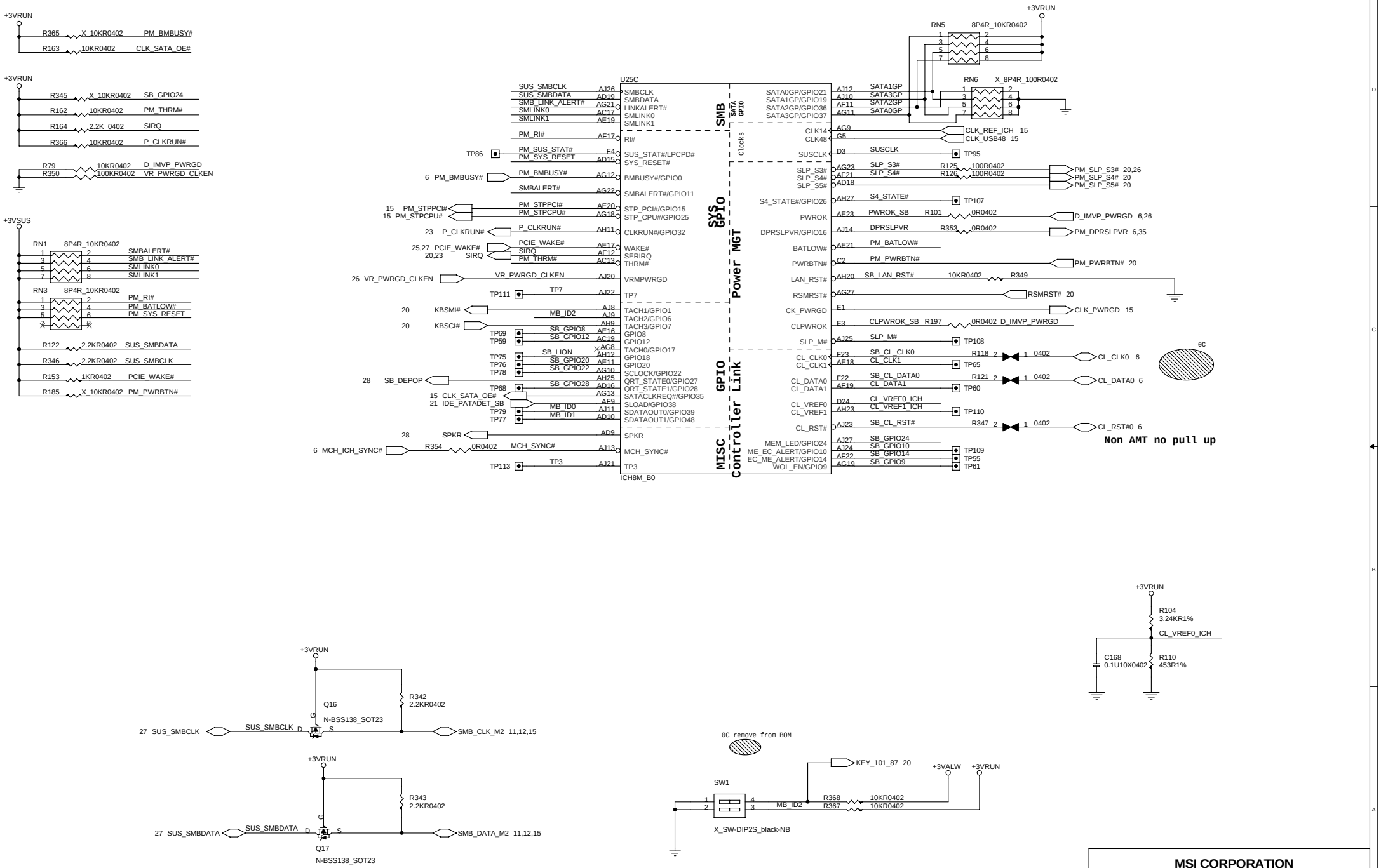

MSI CORPORATION

Title: ICH8M-3 (SM BUS/GPIO)

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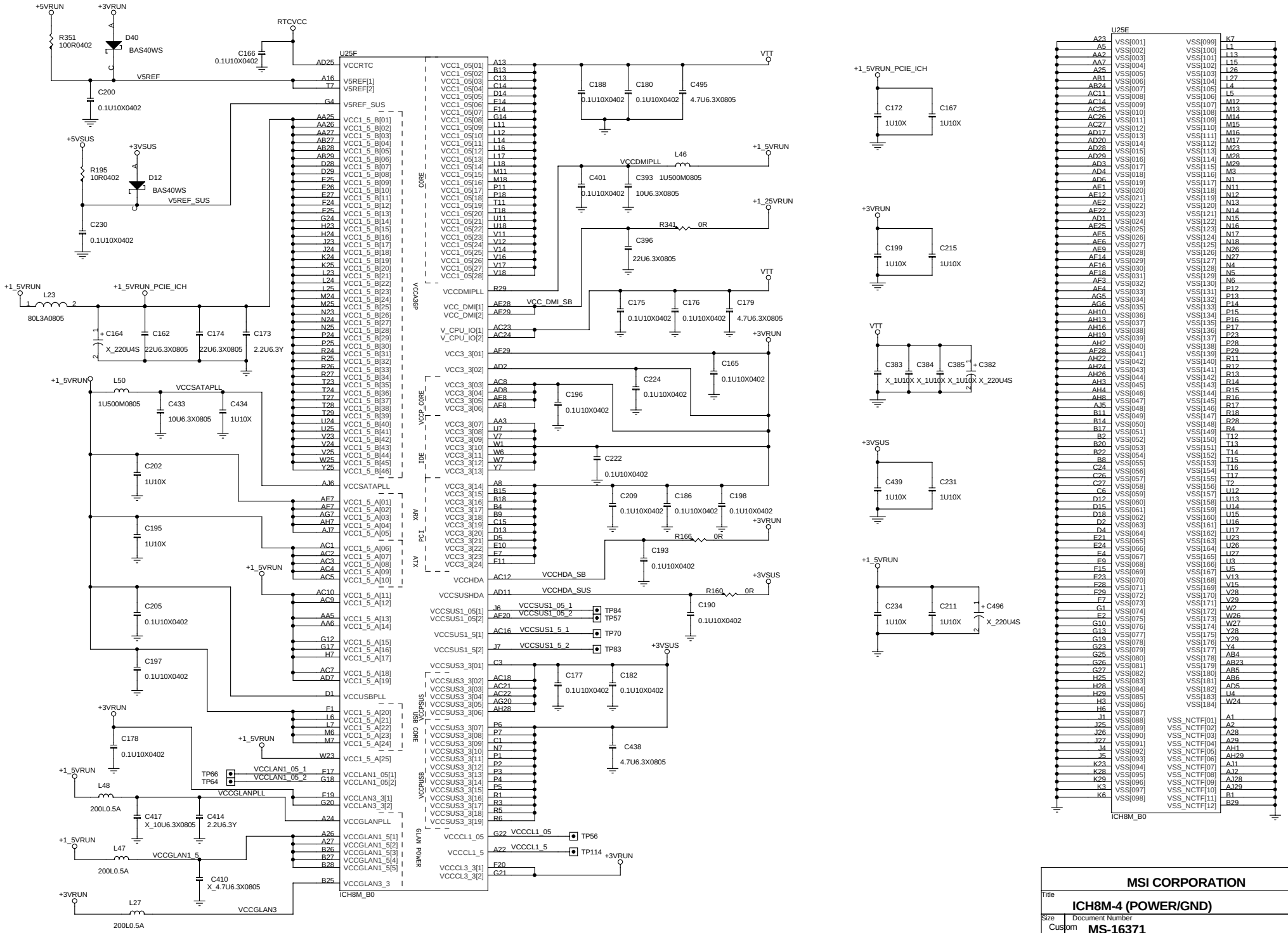

Title	MSI CORPORATION
	ICH8M-4 (POWER/GND)
Size	Custom
Document Number	MS-16371
Rev	0B
Date:	Thursday, February 15, 2007
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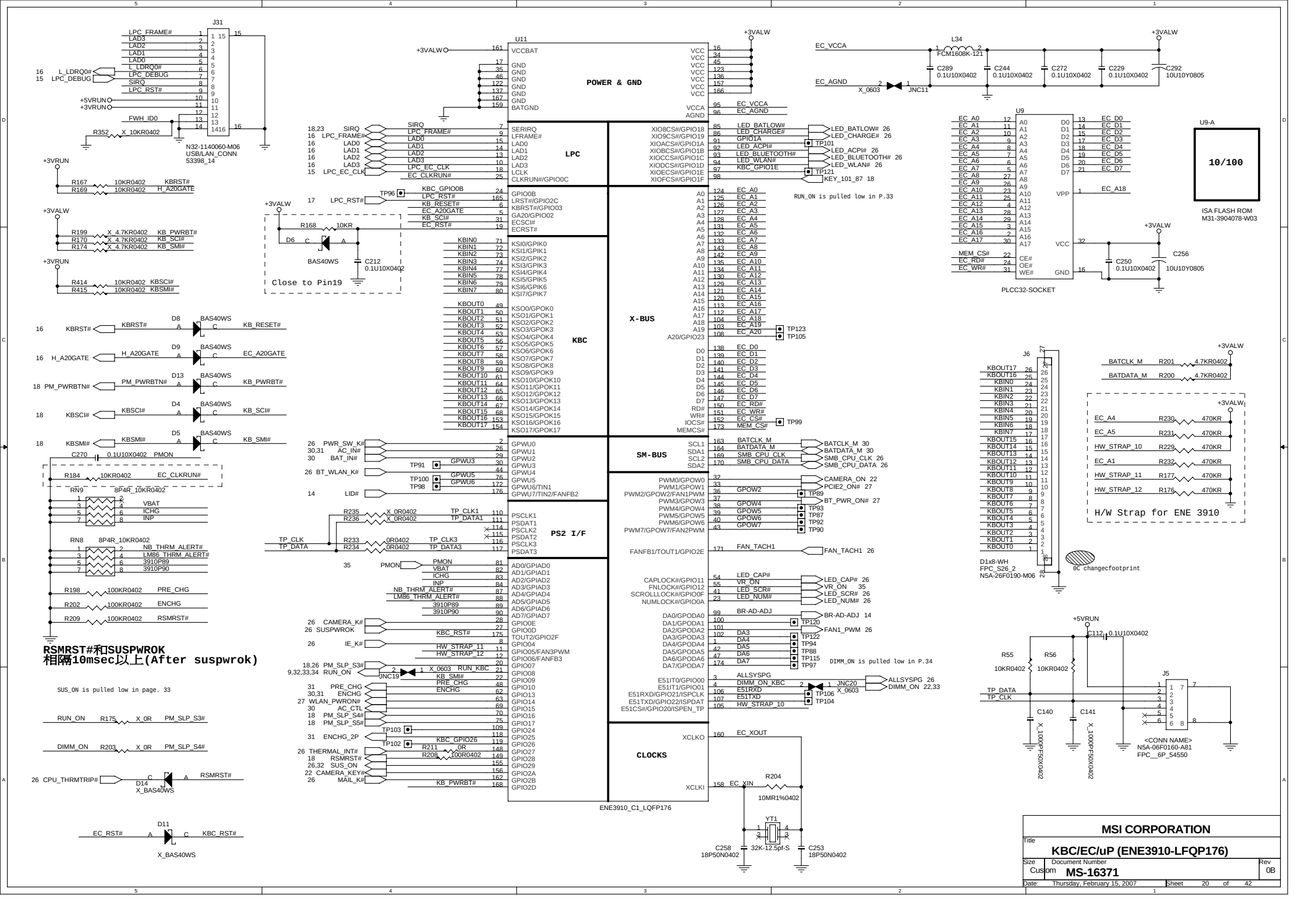
U11
POWER & GND
LPC
KBC
X-BUS
SM-BUS
PS2 I/F
CLOCKS
ENE3910_C1_LQFP176
J31
N32-1140060-M06
USB/LAN_CONN
53398_14
U9
PLCC32-SOCKET
U9-A
10/100
ISA FLASH ROM
M31-3904078-W03
J6
D1x8-WH
FPC_S26_2
N5A-26F0190-M06
H/W Strap for ENE 3910
J5
<CONN NAME>
N5A-06F0160-A81
FPC__6P_54550
RSMRST#和SUSPWROK
相隔10msec以上(After suspwrok)
SUS_ON is pulled low in page. 33
DIMM_ON is pulled low in P.34
RUN_ON is pulled low in P.33
Close to Pin19
MSI CORPORATION
KBC/EC/uP (ENE3910-LFQP176)
Custom
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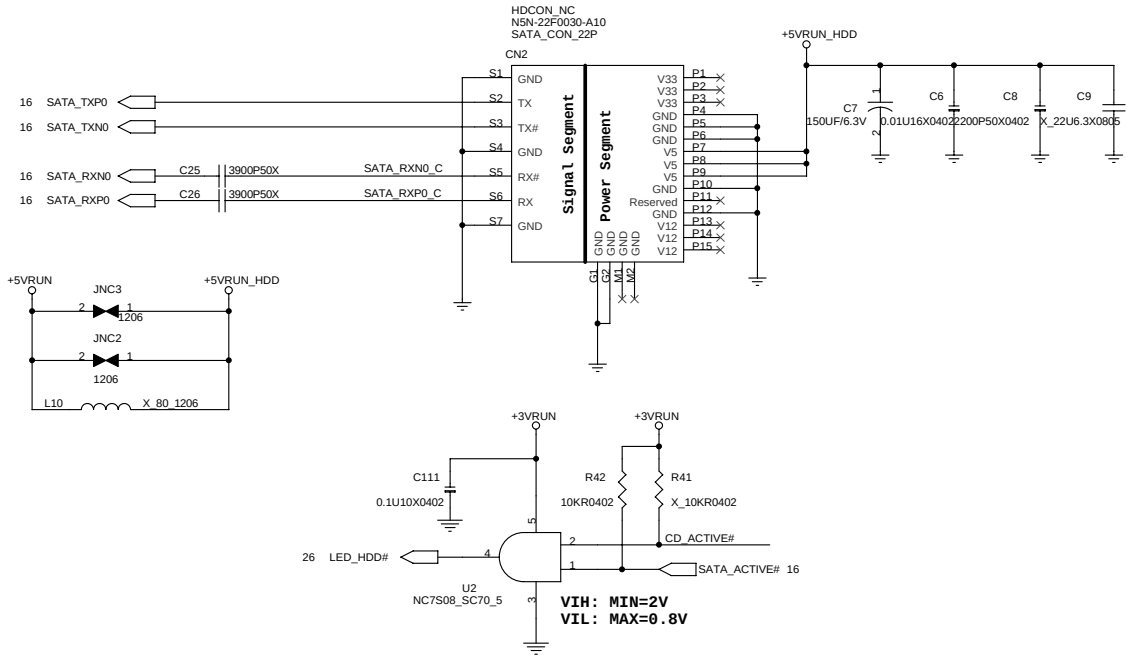
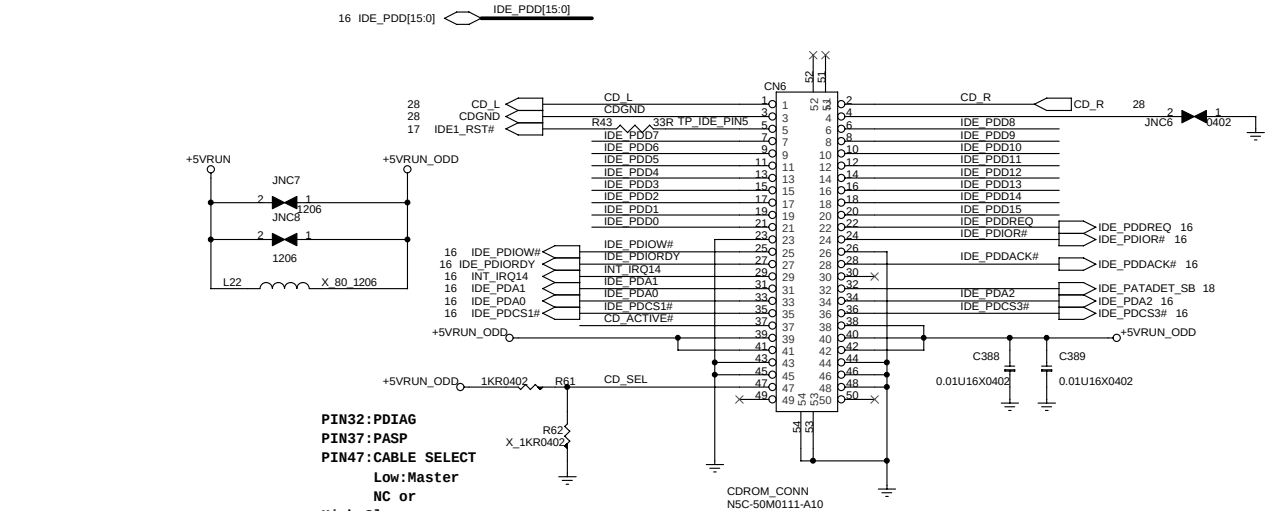
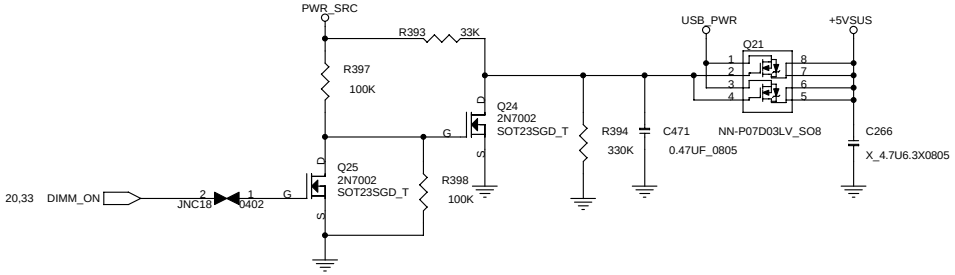
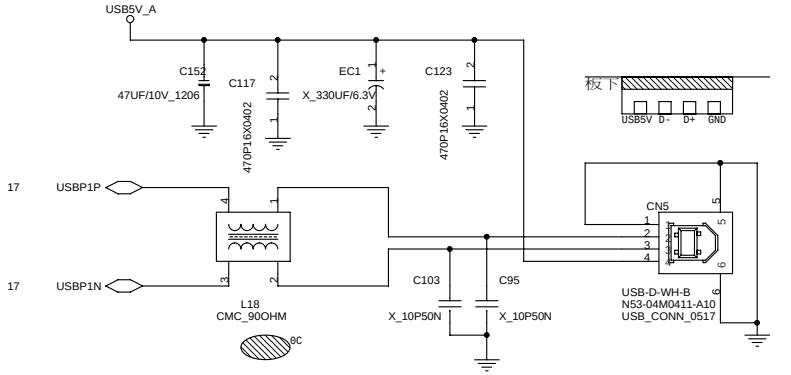
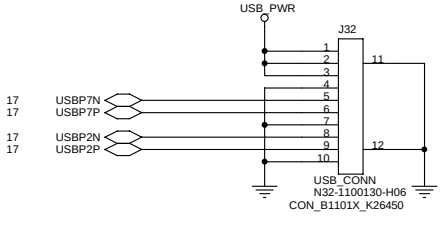


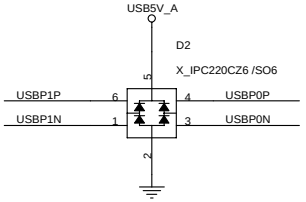


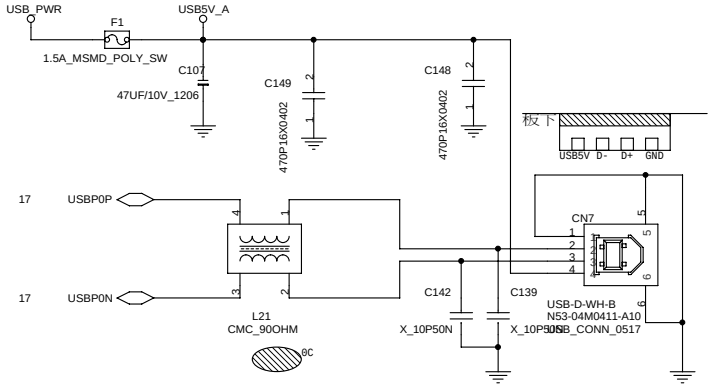
MSI CORPORATION		
Title: HDD&ODD		
Size: Custom	Document Number: MS-16371	Rev: 0B
Date: Thursday, February 15, 2007	Sheet 21 of 42	



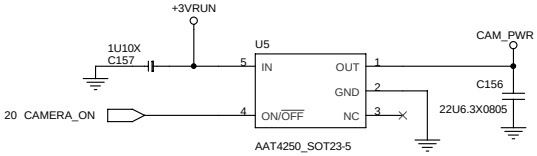


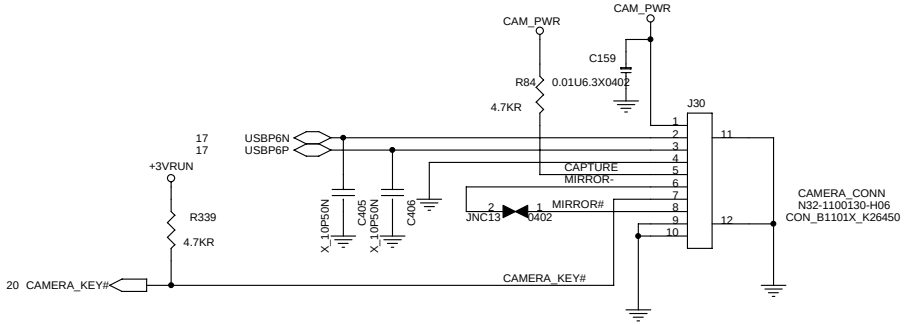






DIGITAL CAMERA





MSI CORPORATION		
Title: **USB & CMOS**		
Size: Custom	Document Number: **MS-16371**	Rev: 0B
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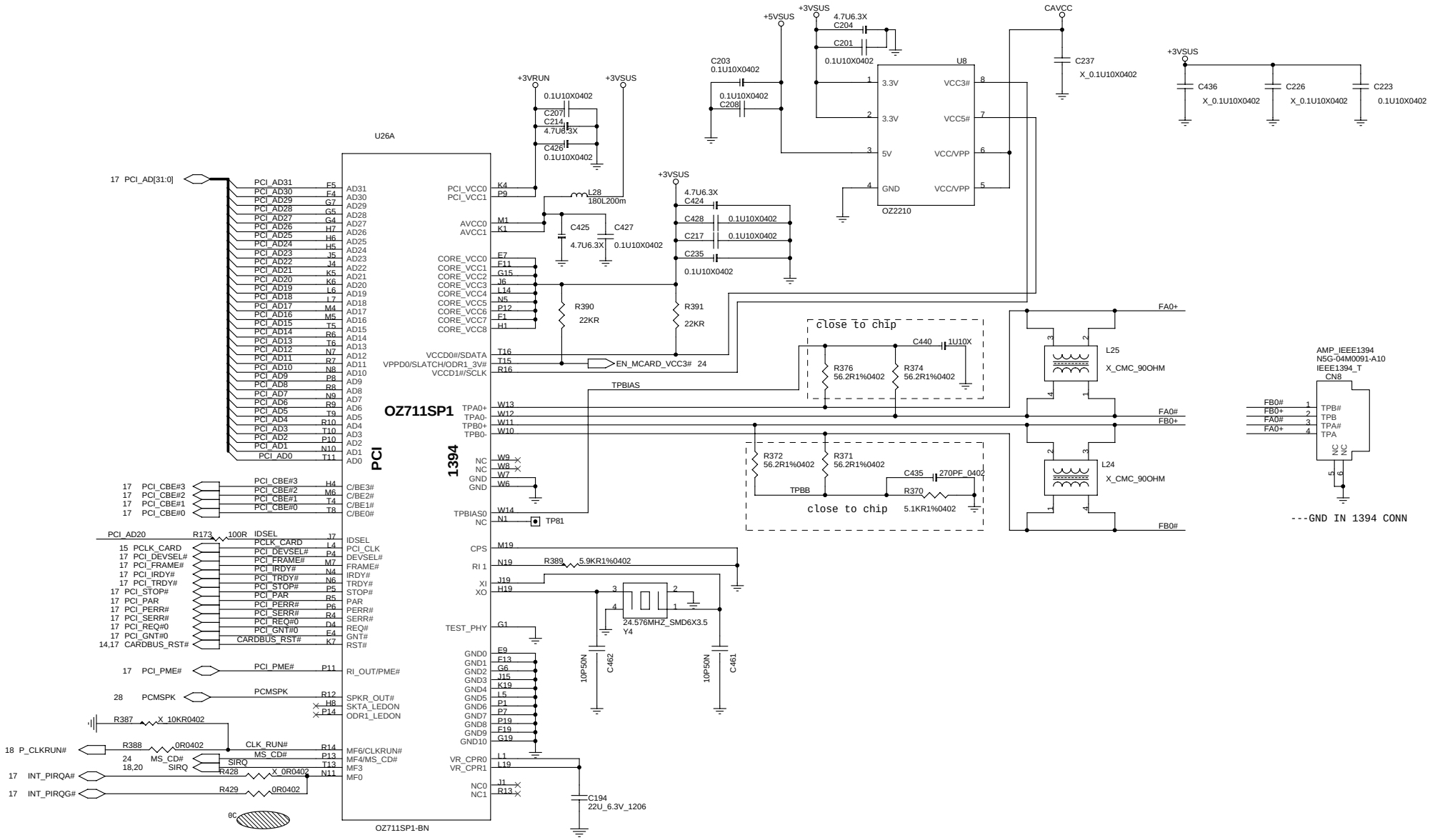
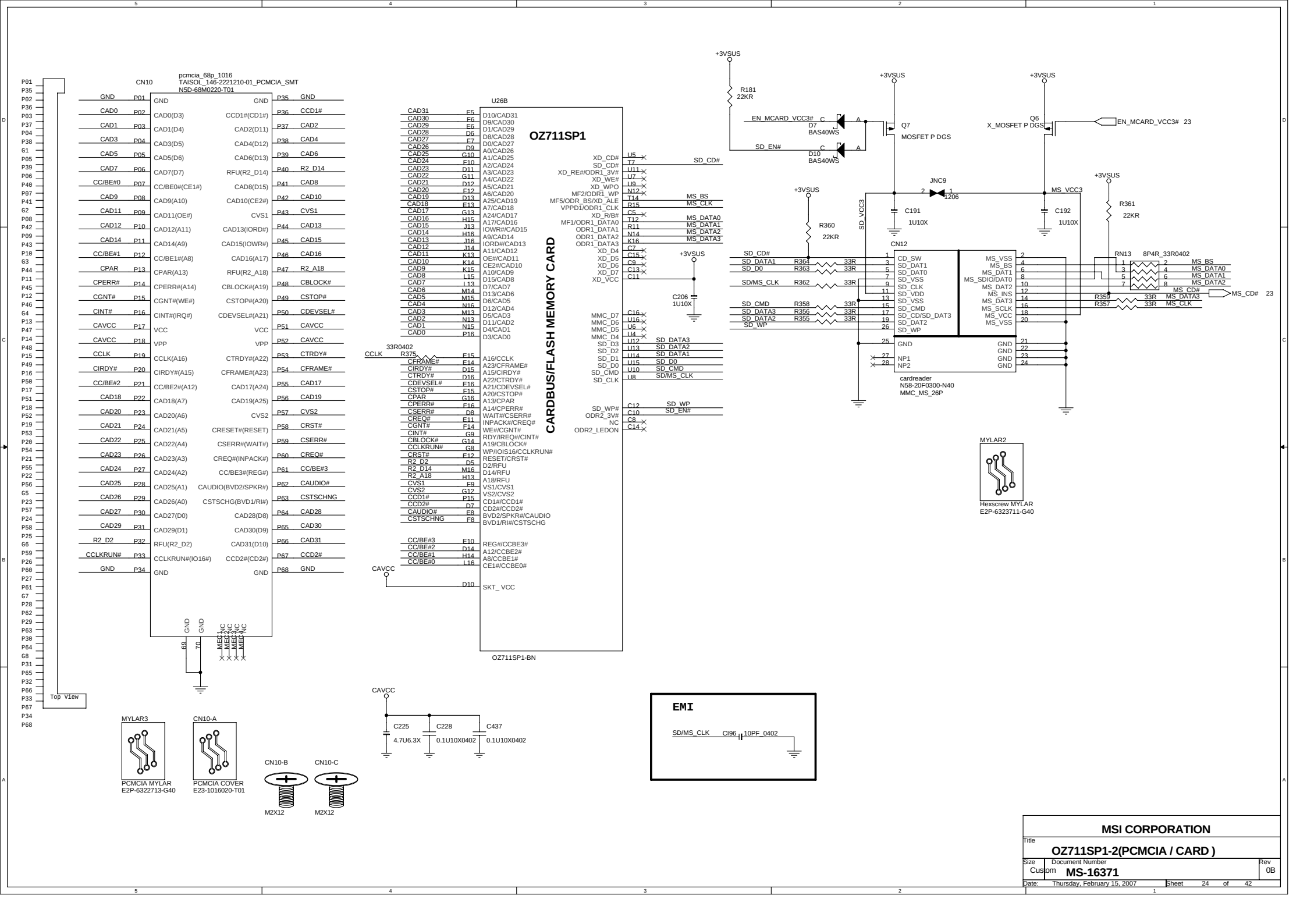


MSI CORPORATION	
Title	OZ711SP1-1(PCI Bus / 1394)
Size: Custom	Document Number: MS-16371
Rev	0B
Date: Thursday, February 15, 2007	Sheet 23 of 42



Title	MSI CORPORATION
	OZ711SP1-2(PCMCIA / CARD)
Size	Custom
Document Number	MS-16371
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Date:	Thursday, February 15, 2007
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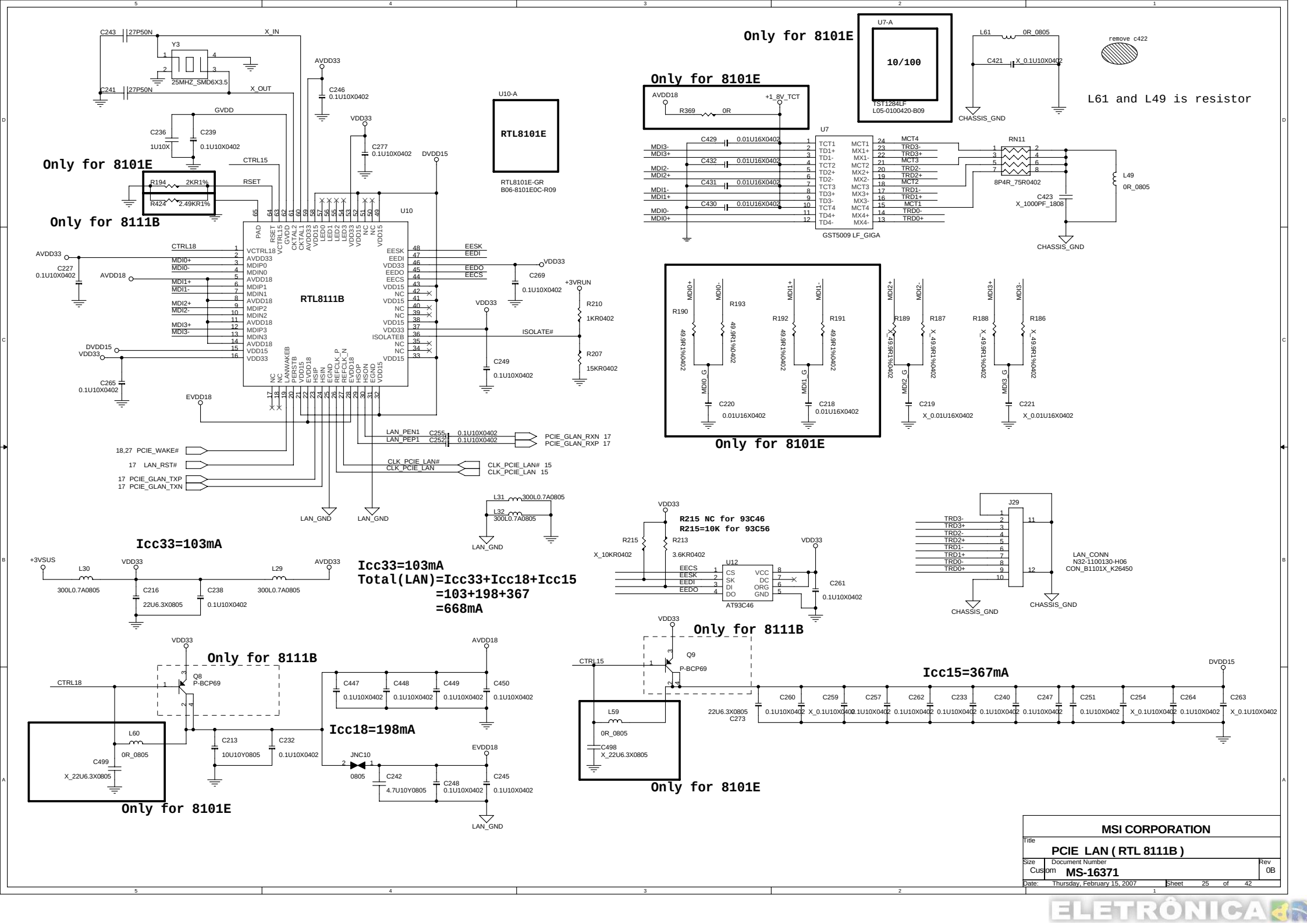
Only for 8101E
U7-A
10/100
TST1284LF
L05-0100420-B09
L61 0R_0805
C421 X_0.1U10X0402
CHASSIS_GND
remove c422
L61 and L49 is resistor
Only for 8101E
AVDD18
R369 0R
+1_8V_TCT
U7
GST5009 LF_GIGA
RN11
8P4R_75R0402
L49 0R_0805
C423 X_1000PF_1808
CHASSIS_GND
C243 27P50N
C241 27P50N
Y3
25MHZ_SMD6X3.5
X_IN
X_OUT
AVDD33
C246 0.1U10X0402
GVDD
C236 1U10X
C239 0.1U10X0402
VDD33
C277 0.1U10X0402
DVDD15
CTRL15
R194 2KR1%
R424 2.49KR1%
RSET
U10-A
RTL8101E
RTL8101E-GR
B06-8101E0C-R09
Only for 8111B
U10
RTL8111B
AVDD33
C227 0.1U10X0402
AVDD18
CTRL18
MDI0+
MDI0-
MDI1+
MDI1-
MDI2+
MDI2-
MDI3+
MDI3-
DVDD15
VDD33
C265 0.1U10X0402
EVDD18
C269 0.1U10X0402
+3VRUN
R210 1KR0402
ISOLATE#
R207 15KR0402
C249 0.1U10X0402
LAN_PEN1
LAN_PEP1
C255 0.1U10X0402
C252 0.1U10X0402
PCIE_GLAN_RXN 17
PCIE_GLAN_RXP 17
18,27 PCIE_WAKE#
17 LAN_RST#
CLK_PCIE_LAN#
CLK_PCIE_LAN
CLK_PCIE_LAN# 15
CLK_PCIE_LAN 15
17 PCIE_GLAN_TXP
17 PCIE_GLAN_TXN
LAN_GND
L31 300L0.7A0805
L32 300L0.7A0805
Only for 8101E
R190 R193 R192 R191
49.9R1%0402
C220 0.01U16X0402
C218 0.01U16X0402
R189 R187 R188 R186
X_49.9R1%0402
C219 X_0.01U16X0402
C221 X_0.01U16X0402
Icc33=103mA
+3VSUS
L30 300L0.7A0805
L29 300L0.7A0805
C216 22U6.3X0805
C238 0.1U10X0402
Icc33=103mA
Total(LAN)=Icc33+Icc18+Icc15
=103+198+367
=668mA
R215 NC for 93C46
R215=10K for 93C56
R215 X_10KR0402
R213 3.6KR0402
U12
AT93C46
C261 0.1U10X0402
J29
LAN_CONN
N32-1100130-H06
CON_B1101X_K26450
CHASSIS_GND
Only for 8111B
Q8
P-BCP69
CTRL18
C447 C448 C449 C450
0.1U10X0402
Icc18=198mA
L60 0R_0805
C499 X_22U6.3X0805
C213 10U10Y0805
C232 0.1U10X0402
JNC10
0805
C242 4.7U10Y0805
C248 0.1U10X0402
C245 0.1U10X0402
EVDD18
Only for 8101E
Only for 8111B
Q9
P-BCP69
CTRL15
L59 0R_0805
C498 X_22U6.3X0805
Icc15=367mA
C260 C259 C257 C262 C233 C240 C247 C251 C254 C264 C263
0.1U10X0402
C273 22U6.3X0805
Only for 8101E
MSI CORPORATION
Title
PCIE LAN (RTL 8111B)
Size Custom
Document Number MS-16371
Rev 0B
Date: Thursday, February 15, 2007
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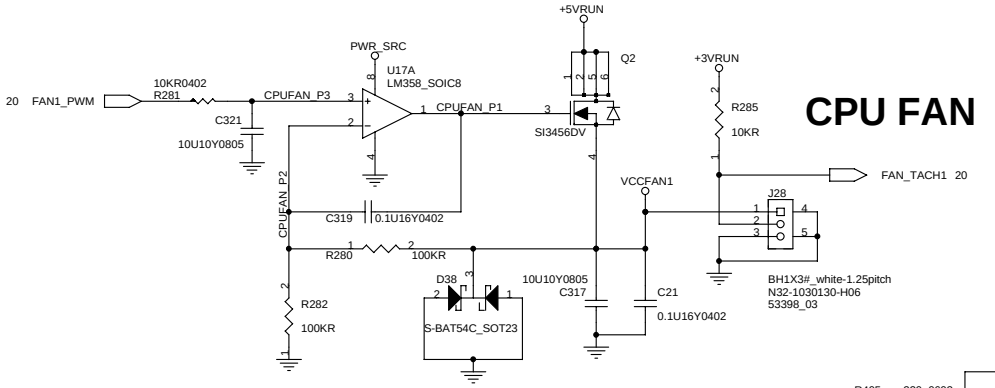
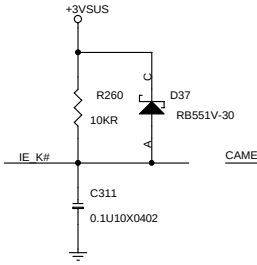
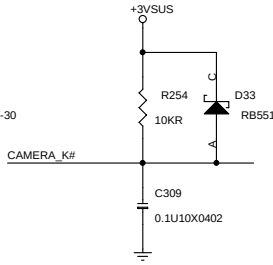
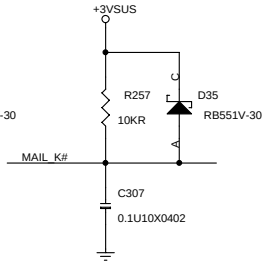
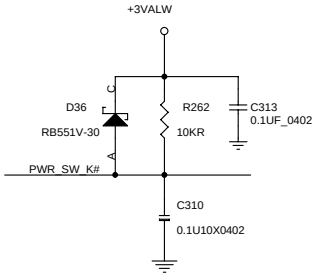
CPU FAN

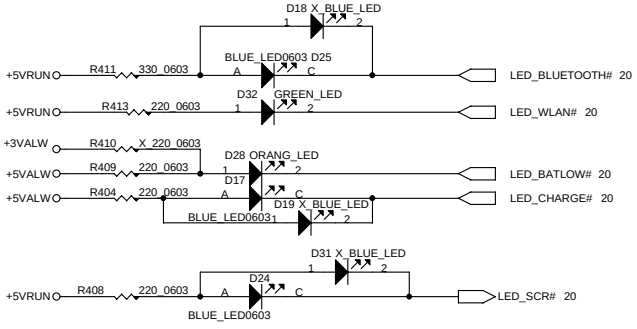


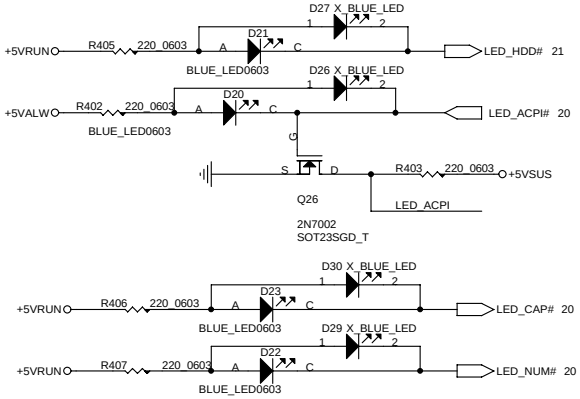


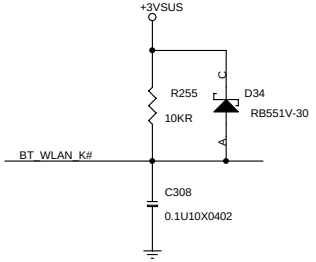


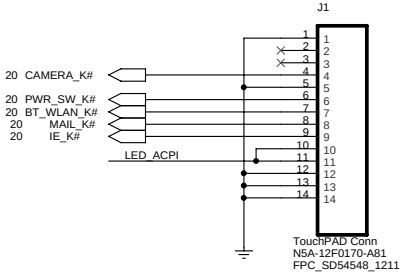


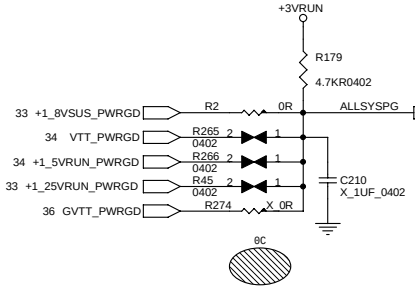


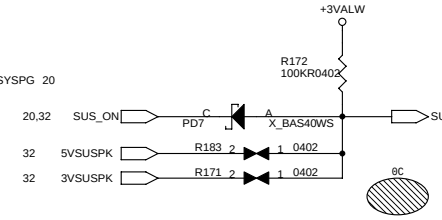




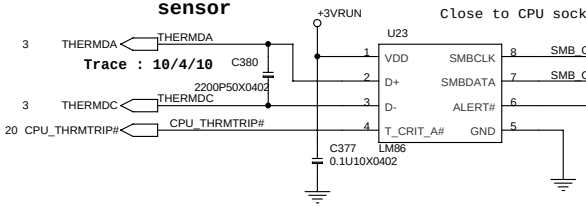


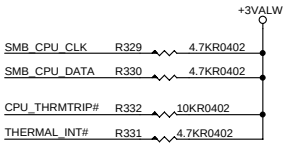


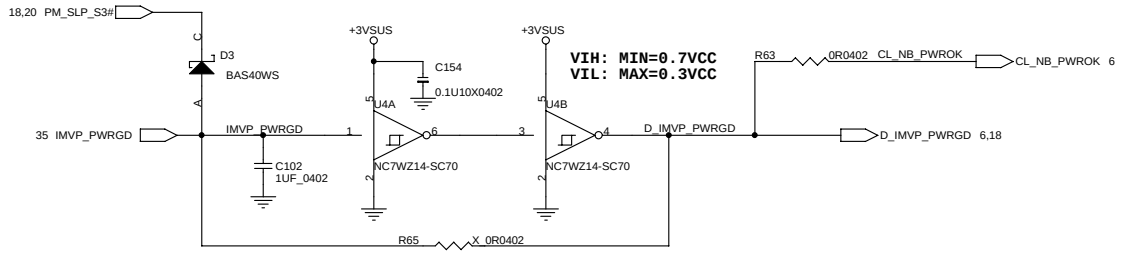


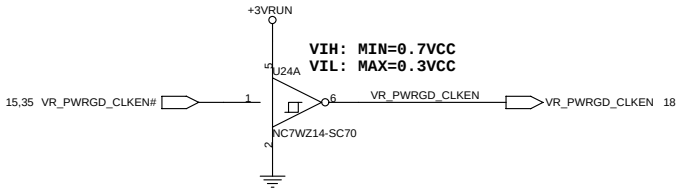


Cap close to thermal sensor









MSI CORPORATION		
Title: FAN / LED / SW/ POWER GOOD		
Size: Custom	Document Number: MS-16371	Rev: 0B
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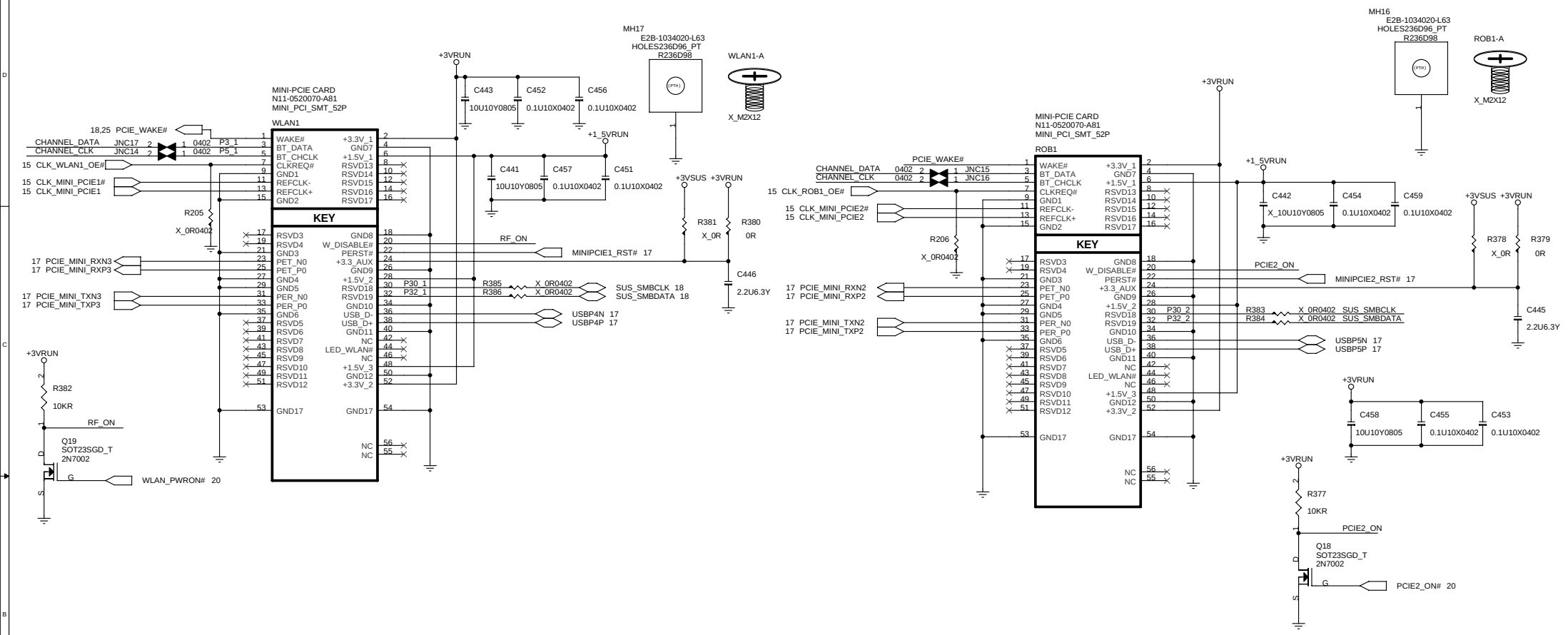
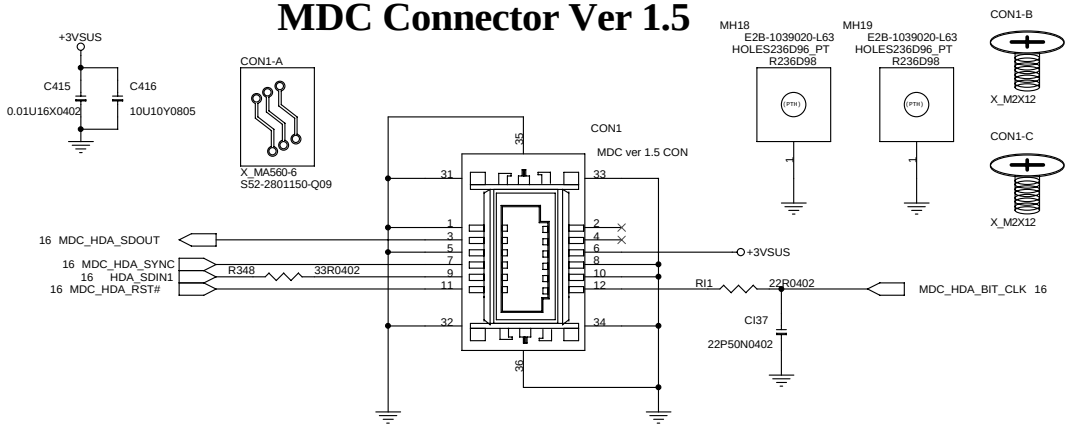
WLAN and Robson

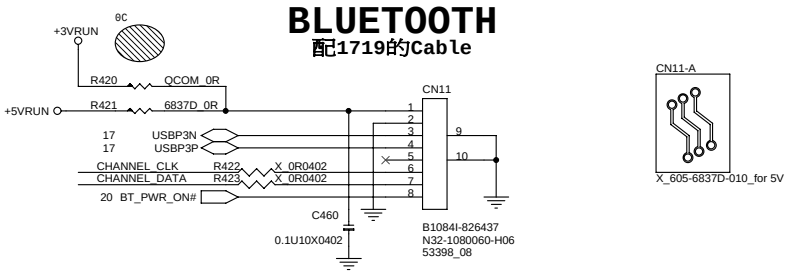


MDC Connector Ver 1.5

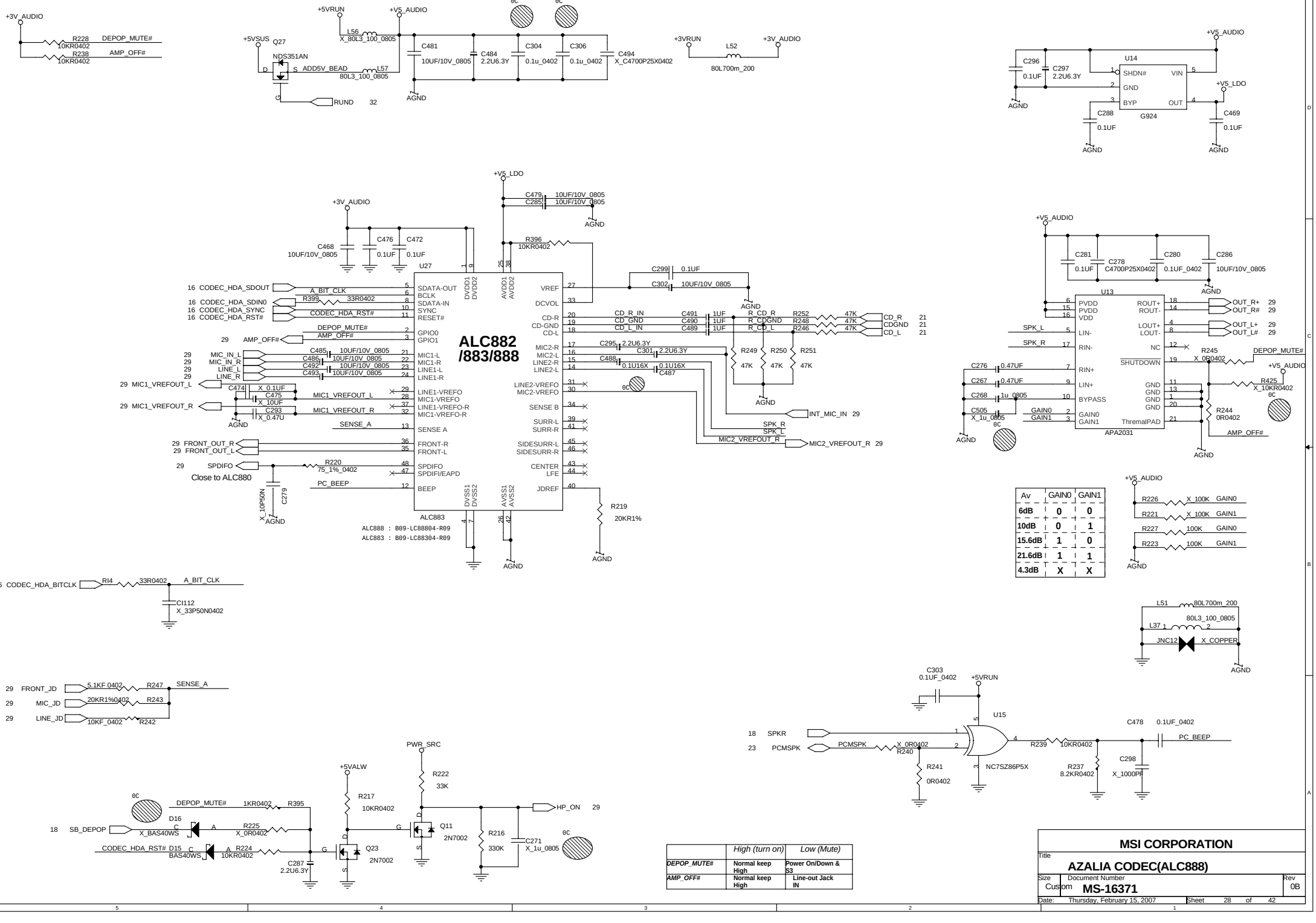


BLUETOOTH

配1719的Cable

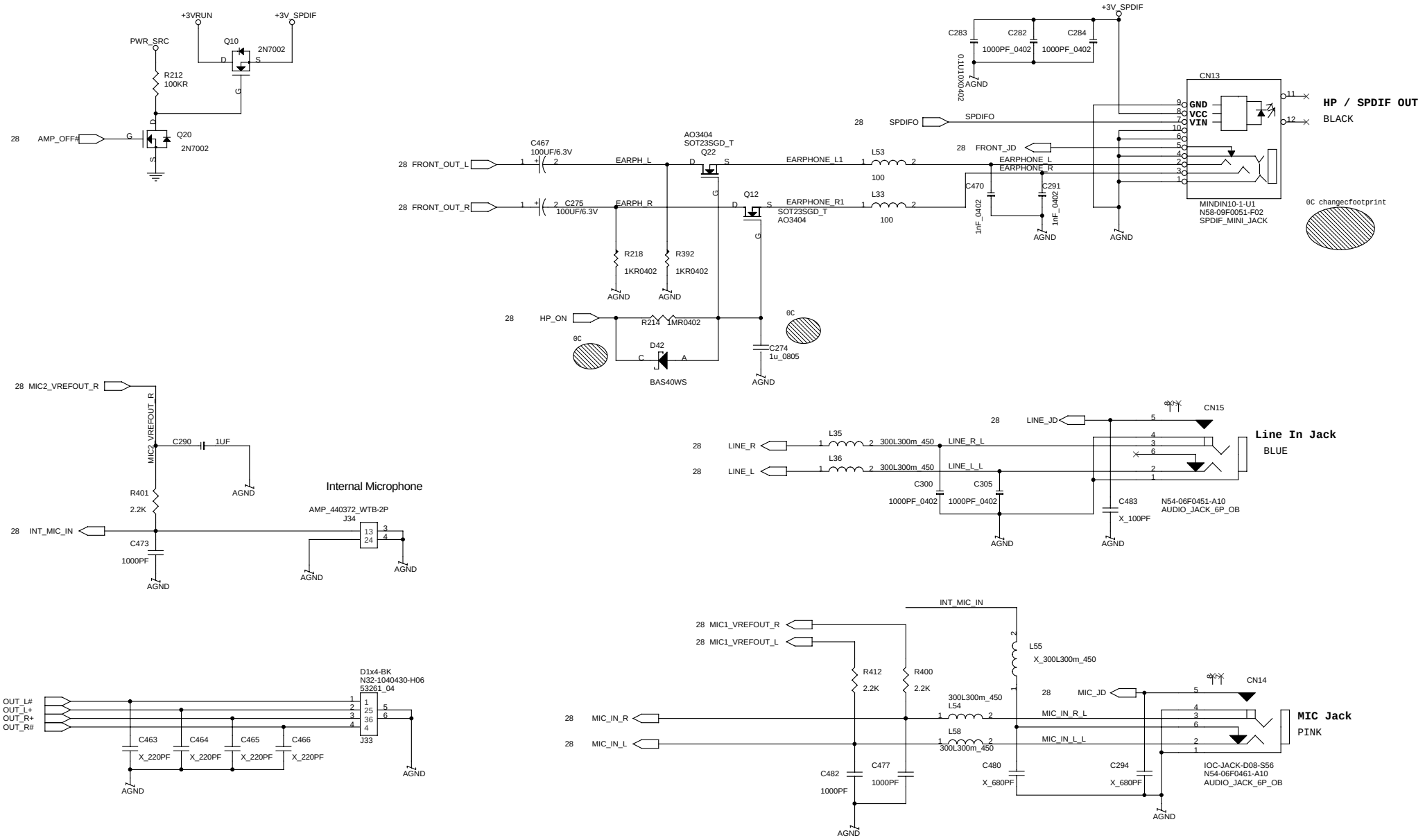


MSI CORPORATION			
Title: Mini PCIE & MDC & BT			
Size: Custom	Document Number: MS-16371		Rev: 0B
Date: Thursday, February 15, 2007		Sheet 27 of 42	

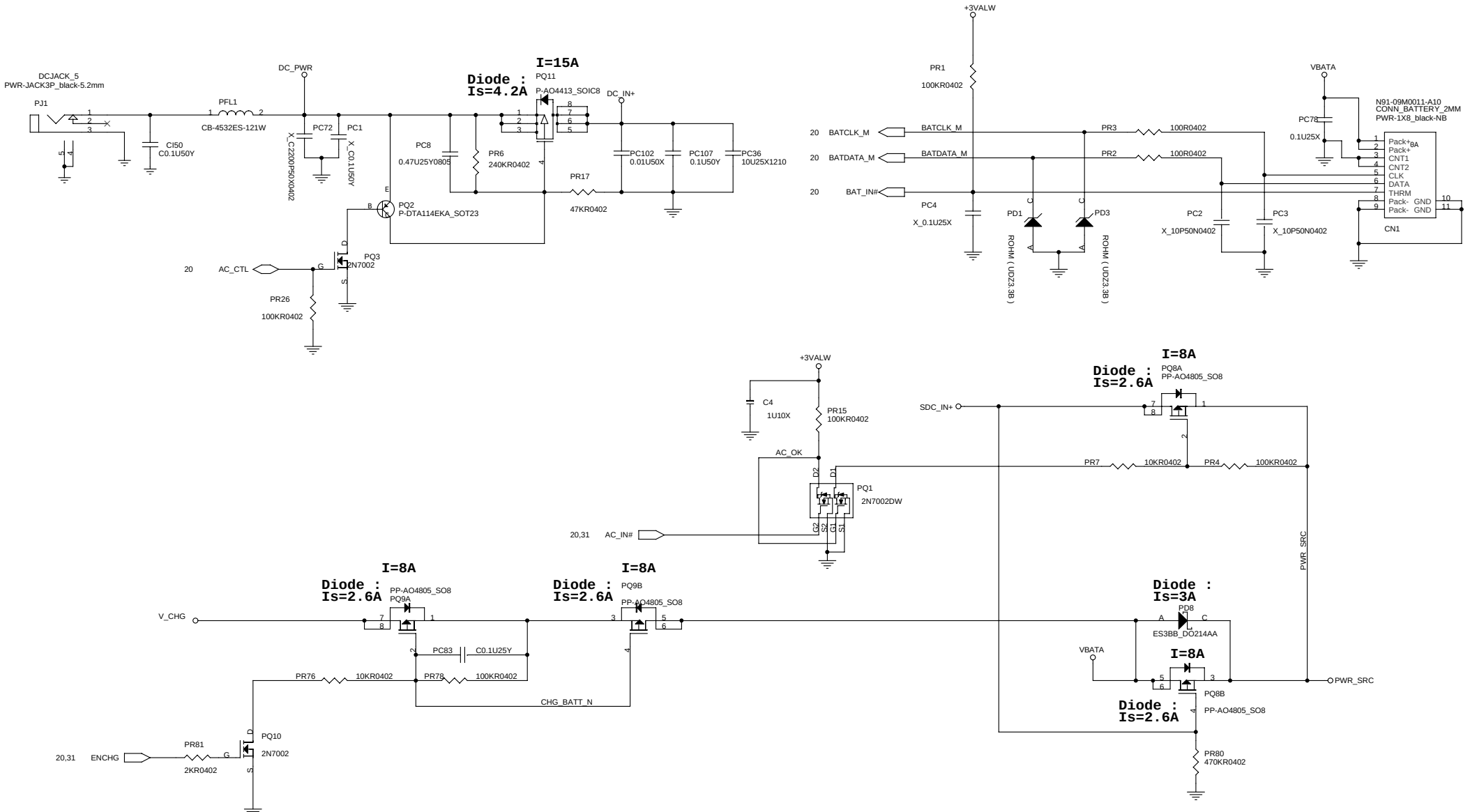


	High (turn on)	Low (Mute)
DEPOP_MUTE#	Normal keep High	Power On/Down & S3
AMP_OFF#	Normal keep High	Line-out Jack IN

MSI CORPORATION		
Title: AZALIA CODEC(ALC888)		
Size: Custom	Document Number: MS-16371	Rev: 0B
Date: Thursday, February 15, 2007	Sheet 28 of 42	



MSI CORPORATION			
Title: Audio Jacks			
Size: Custom	Document Number: MS-16371		Rev: 0B
Date: Thursday, February 15, 2007		Sheet 29 of 42	



MSI CORPORATION		
Title: **Battery Select**		
Size: Custom	Document Number: **MS-16371**	Rev: 0B
Date: Thursday, February 15, 2007	Sheet 30 of 42	

(Vref/2)/(PR109*(PR112+PR109))
2.048/7.15*(53.6+7.15)=17.4V

Adapter= 90 W

Adapter input voltage set 17.4 Voltage
If <17.4V, ACOK#=high

3S2P: Charge current set 3 Amp
3S3P: Charge current set 4.5 Amp
Pre-charger: Charge current set 220mA

CELL GND=2 CELLS
FLOAT=3 CELLS
REFIN=4 CELLS

need to check value

SET Iin MAX = A

Iinput=(Vcls/Vref)*(0.075/RS1)
RS1=PR74=0.01, Vref=4.096V
Vcls=4.096*PR23/(PR23+PR97)=2.29V
Iinput=(2.29/4.096)*(0.075/0.01)=4.2A

PR23	PR97	
19.1K	28.7K	65W
	24K	75W
	16.9K	90W

Icharge=(Victl/Vrefin)*(0.075/RS2)
RS2=PR24=0.015
Vrefin=MAX8724_LDO*PR35/(PR34+PR35)
=5.4V*1.1K/(1.1K+768)=3.18V=MAX8724_REFIN
Victl=MAX8724_REFIN*PR30/(PR11+PR30)
For 3S2P:
Victl=3.18*(PR30//PR108)/((PR30//PR108)+PR11)
=3.18*15.91K/(15.91K+10.5K)=1.92V
Icharge=(1.92/3.18)*(0.075/0.015)=3.01A
For 3S2P:
Victl=3.18*PR30/(PR30+PR11)
=3.18*95.3K/(95.3K+10.5K)=2.86V
Icharge=(2.86/3.18)*(0.075/0.015)=4.5A
For Precharge:
Victl=3.18*(PR30//PR105)/((PR30//PR105)+PR11)
=3.18*0.496/(0.496+10.5K)=0.15mV
Icharge=(0.15mV/3.18)*(0.075/0.015)=0.236mA

ENCHG-2P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	3S2P-Fast charge
0	0	1	3S3P-Fast charge
0	0	0	STOP CHARGE

65W_DETEC : DEFAULT=HIGH
High =>65W
Low =>90W

90W for LG
PR97-A
16.9KR1%_0402

MSI CORPORATION

Title: **Battery Charger**

Size: Custom | Document Number: **MS-16371** | Rev: 0B

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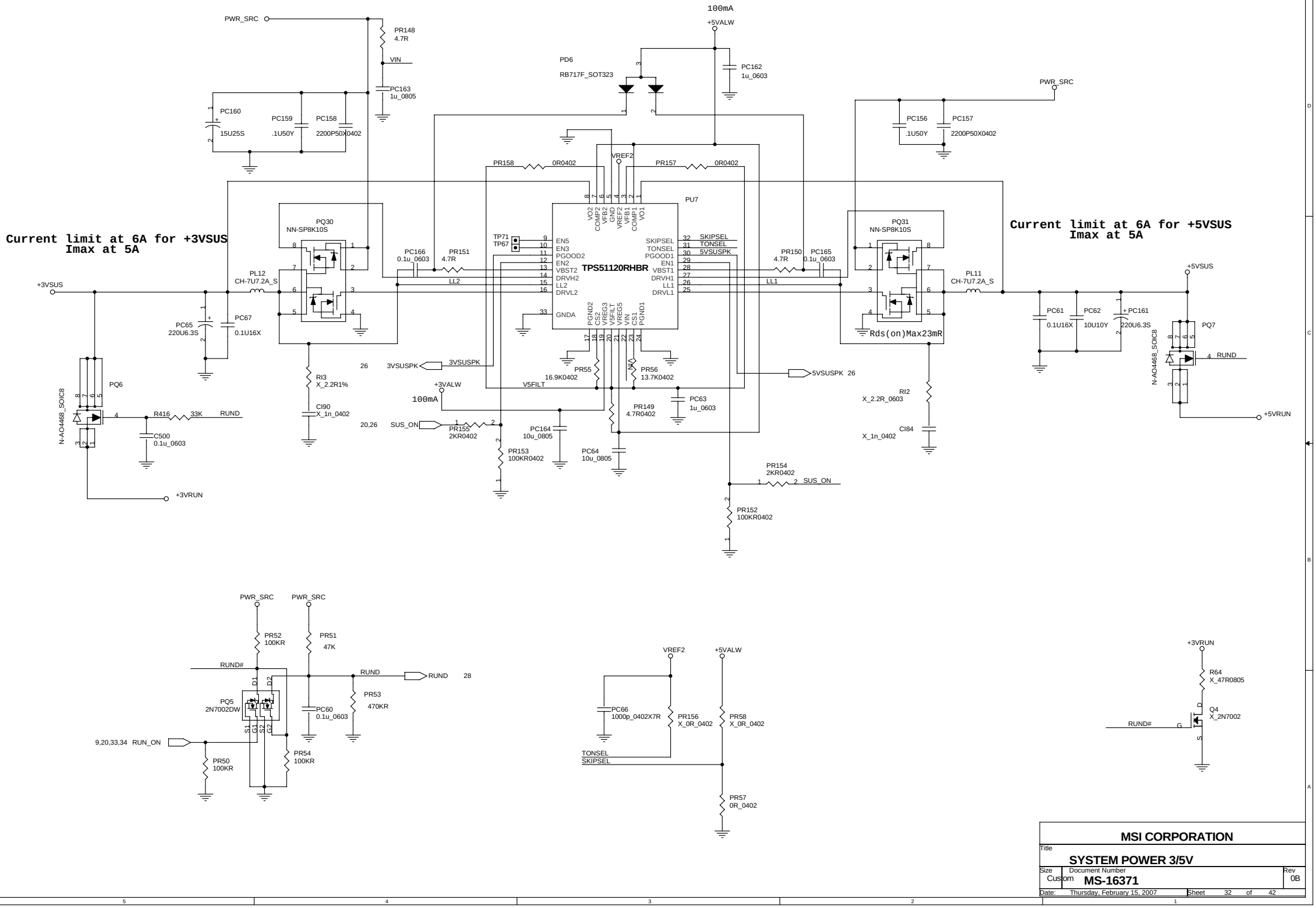
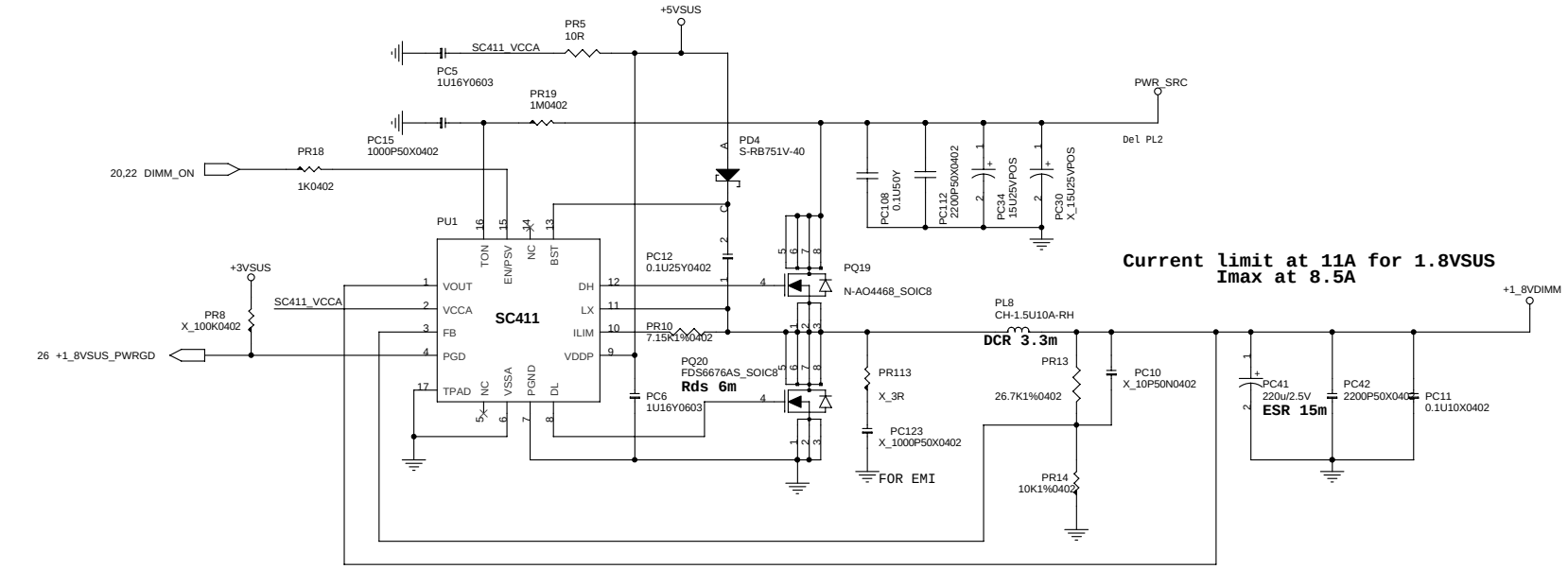
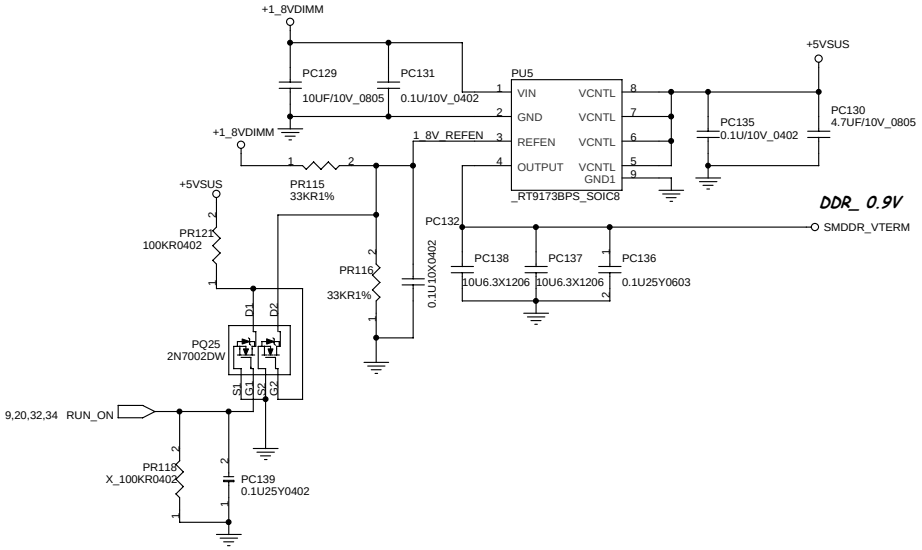
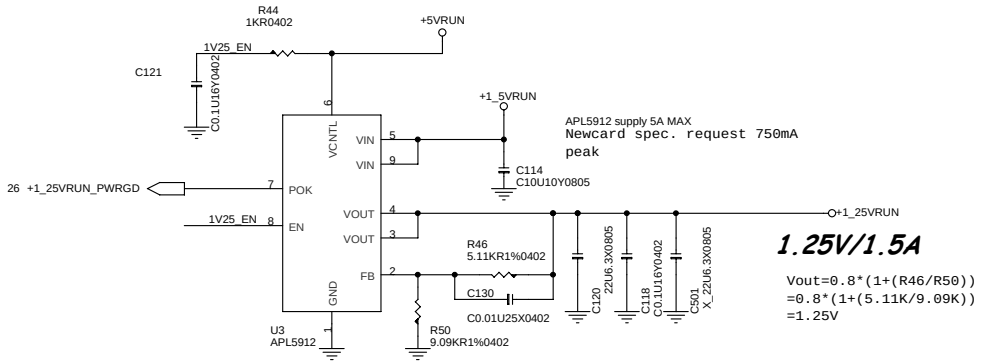


MSI CORPORATION		
Title: SYSTEM POWER 3/5V		
Size: Custom	Document Number: MS-16371	Rev: 0B
Date: Thursday, February 15, 2007	Sheet 32 of 42	







MSI CORPORATION		
Title: DDR2 RAM POWER, +1.25V		
Size: Custom	Document Number: MS-16371	Rev: 0B
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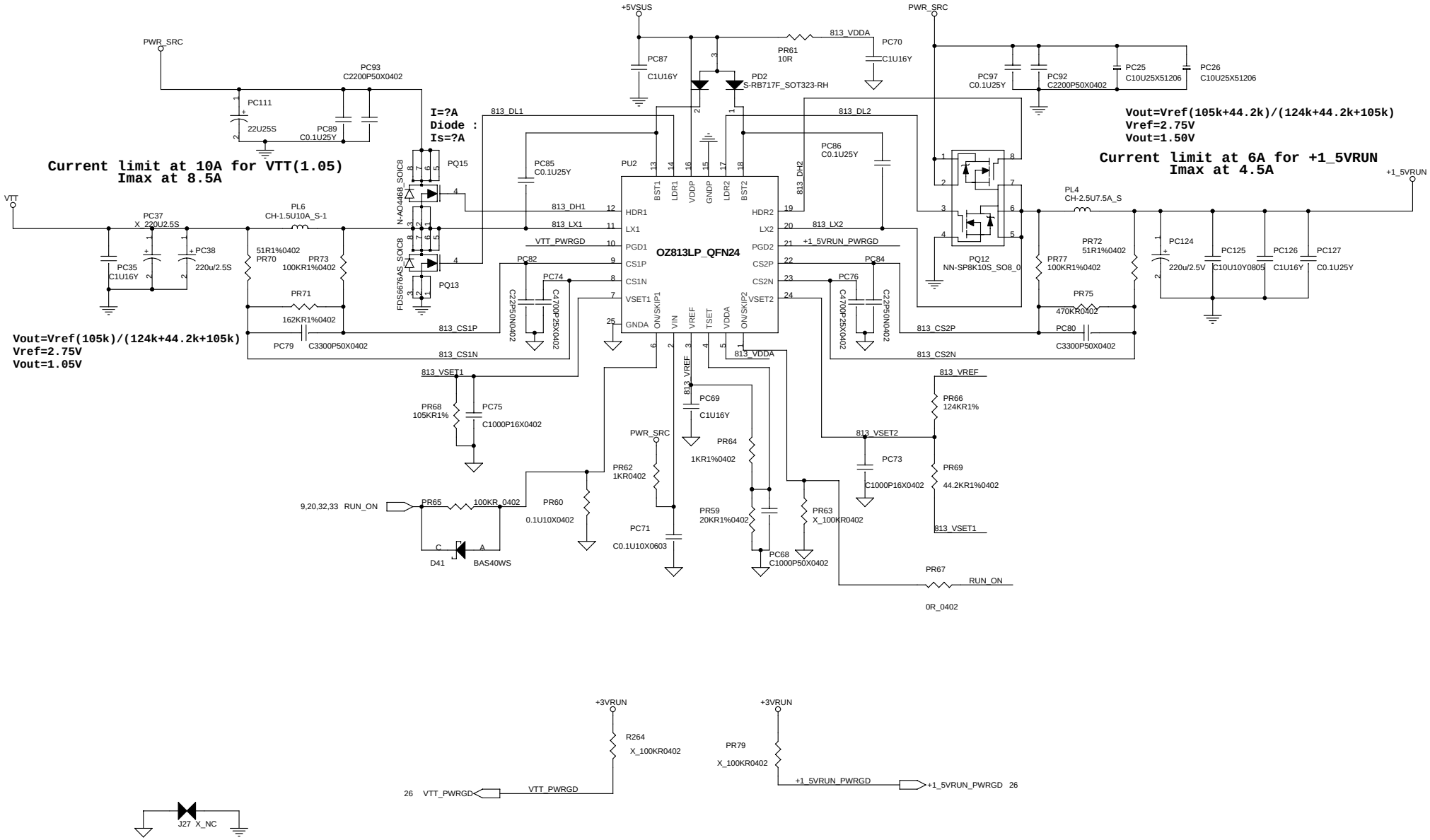
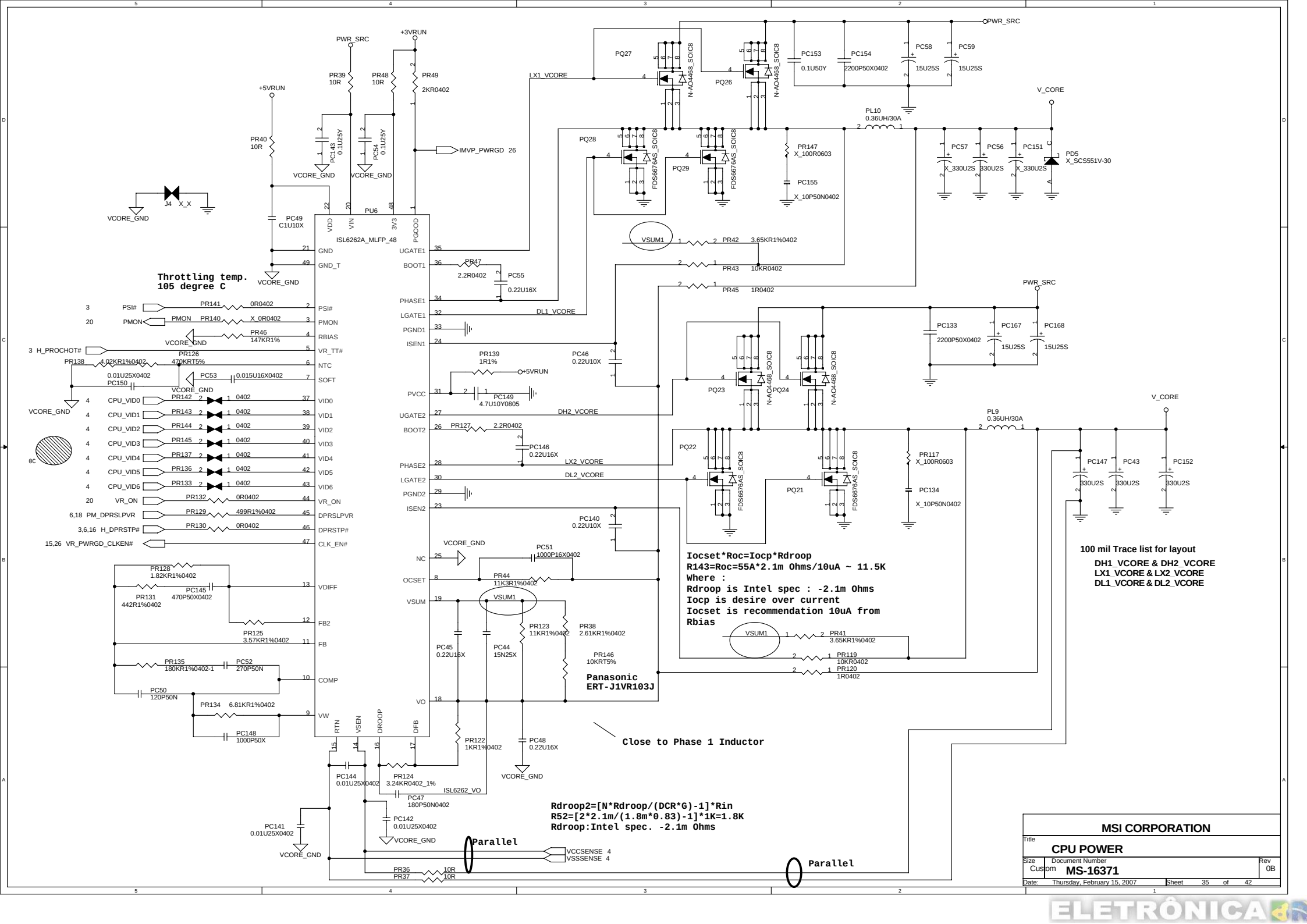


MSI CORPORATION		
Title: +1_5VRUN , VTT POWER		
Size: Custom	Document Number: MS-16371	Rev: 0B
Date: Thursday, February 15, 2007	Sheet 34 of 42	


PWR_SRC
+3VRUN
+5VRUN
PR39 10R
PR48 10R
PR49 2KR0402
PR40 10R
IMVP_PWRGD 26
VCORE_GND
PC143 0.1U25Y
PC54 0.1U25Y
J4 X_X
PC49 C1U10X
PU6
ISL6262A_MLFP_48
VDD
VIN
3V3
PGOOD
GND
GND_T
UGATE1
BOOT1
PHASE1
LGATE1
PGND1
ISEN1
PVCC
UGATE2
BOOT2
PHASE2
LGATE2
PGND2
ISEN2
NC
OCSET
VSUM
VDIFF
FB2
FB
COMP
VW
RTN
VSEN
DROOP
DFB
LX1_VCORE
DL1_VCORE
DH2_VCORE
LX2_VCORE
DL2_VCORE
ISL6262_VO
PQ27
PQ26
PQ28
PQ29
PQ23
PQ24
PQ22
PQ21
N-AO4468_SOIC8
FDS6676AS_SOIC8
PC153 0.1U50Y
PC154 2200P50X0402
PC58 15U25S
PC59 15U25S
PL10 0.36UH/30A
PR147 X_100R0603
PC155 X_10P50N0402
PC57 X_330U2S
PC56 330U2S
PC151 X_330U2S
PD5 X_SCS551V-30
V_CORE
VSUM1
PR42 3.65KR1%0402
PR43 10KR0402
PR45 1R0402
PR47 2.2R0402
PC55 0.22U16X
PR139 1R1%
PC46 0.22U10X
PC149 4.7U10Y0805
PR127 2.2R0402
PC146 0.22U16X
PC140 0.22U10X
PC133 2200P50X0402
PC167 15U25S
PC168 15U25S
PL9 0.36UH/30A
PR117 X_100R0603
PC134 X_10P50N0402
PC147 330U2S
PC43 330U2S
PC152 330U2S
PR41 3.65KR1%0402
PR119 10KR0402
PR120 1R0402
PR128 1.82KR1%0402
PC145 470P50X0402
PR131 442R1%0402
PR125 3.57KR1%0402
PR135 180KR1%0402-1
PC52 270P50N
PC50 120P50N
PR134 6.81KR1%0402
PC148 1000P50X
PC51 1000P16X0402
PR44 11K3R1%0402
PC45 0.22U16X
PC44 15N25X
PR123 11KR1%0402
PR38 2.61KR1%0402
PR146 10KRT5%
PR122 1KR1%0402
PC48 0.22U16X
PC144 0.01U25X0402
PR124 3.24KR0402_1%
PC47 180P50N0402
PC142 0.01U25X0402
PC141 0.01U25X0402
PR36 10R
PR37 10R
VCCSENSE 4
VSSSENSE 4
PSI# PR141 0R0402
PMON PR140 X_0R0402
PR46 147KR1%
H_PROCHOT# PR126
PR138 4.02KR1%0402
470KRT5%
PC150 0.01U25X0402
PC53 0.015U16X0402
CPU_VID0 PR142 0402
CPU_VID1 PR143 0402
CPU_VID2 PR144 0402
CPU_VID3 PR145 0402
CPU_VID4 PR137 0402
CPU_VID5 PR136 0402
CPU_VID6 PR133 0402
VR_ON PR132 0R0402
PM_DPRSLPVR PR129 499R1%0402
H_DPRSTP# PR130 0R0402
VR_PWRGD_CLKEN#
VID0
VID1
VID2
VID3
VID4
VID5
VID6
DPRSLPVR
DPRSTP#
CLK_EN#
Throttling temp.
105 degree C
Iocset*Roc=Iocp*Rdroop
R143=Roc=55A*2.1m Ohms/10uA ~ 11.5K
Where :
Rdroop is Intel spec : -2.1m Ohms
Iocp is desire over current
Iocset is recommendation 10uA from
Rbias
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
Rdroop2=[N*Rdroop/(DCR*G)-1]*Rin
R52=[2*2.1m/(1.8m*0.83)-1]*1K=1.8K
Rdroop:Intel spec. -2.1m Ohms
Parallel
Parallel
100 mil Trace list for layout
DH1_VCORE & DH2_VCORE
LX1_VCORE & LX2_VCORE
DL1_VCORE & DL2_VCORE
MSI CORPORATION
CPU POWER
Size Custom
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Date: Thursday, February 15, 2007
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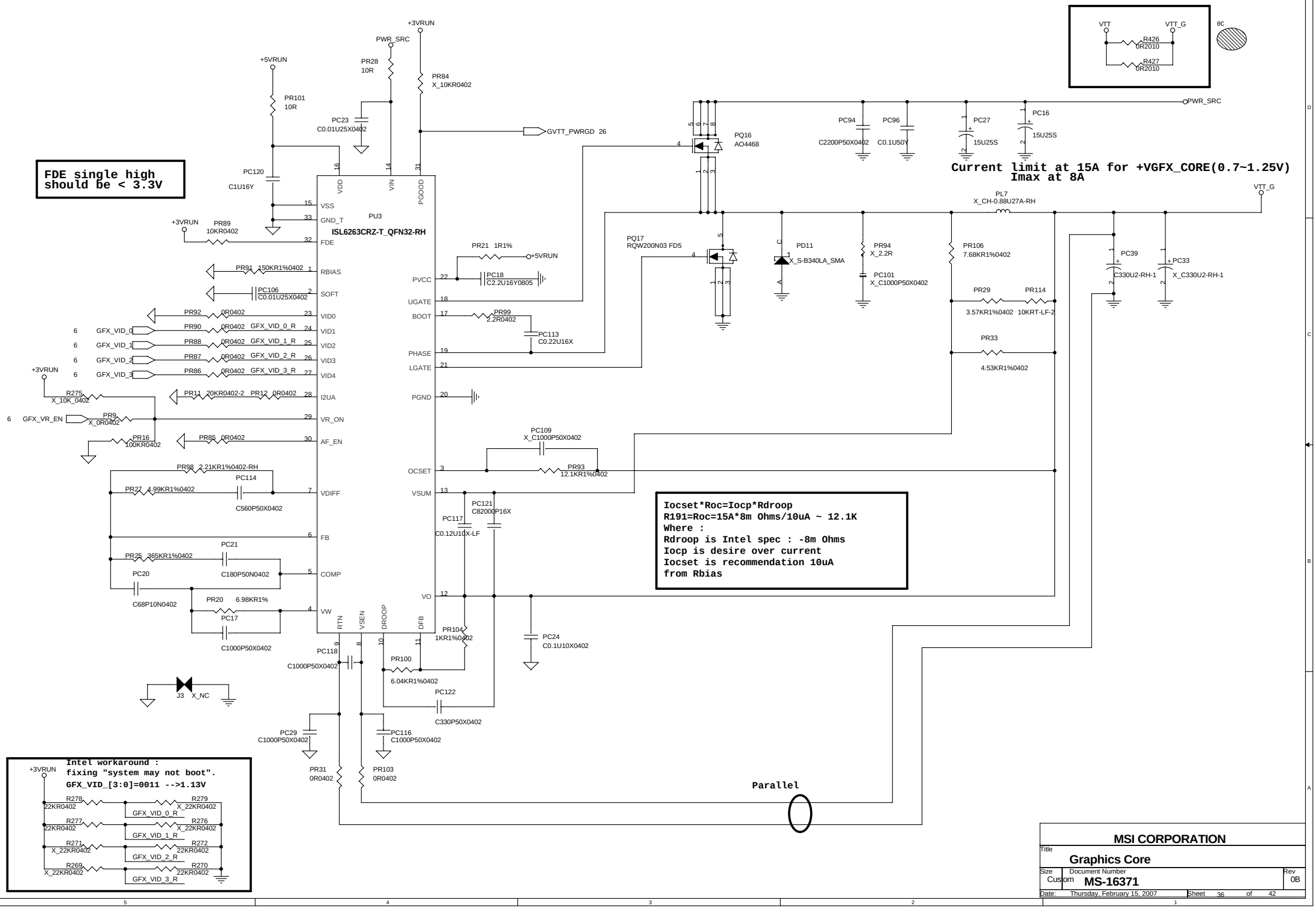
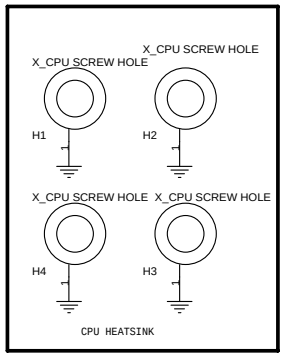
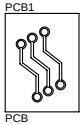
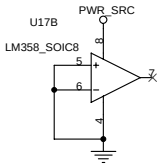
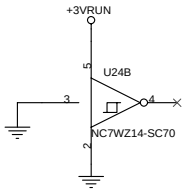

FDE single high should be < 3.3V
Current limit at 15A for +VGFX_CORE(0.7~1.25V) Imax at 8A
ISL6263CRZ-T_QFN32-RH
PU3
PQ16 AO4468
PQ17 RQW200N03 FD5
PD11 X_S-B340LA_SMA
PL7 X_CH-0.88U27A-RH
Iocset*Roc=Iocp*Rdroop
R191=Roc=15A*8m Ohms/10uA ~ 12.1K
Where :
Rdroop is Intel spec : -8m Ohms
Iocp is desire over current
Iocset is recommendation 10uA
from Rbias
Intel workaround :
fixing "system may not boot".
GFX_VID_[3:0]=0011 -->1.13V
Parallel
MSI CORPORATION
Graphics Core
MS-16371
Thursday, February 15, 2007

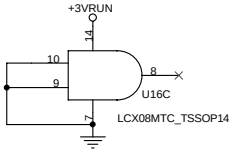


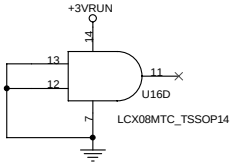


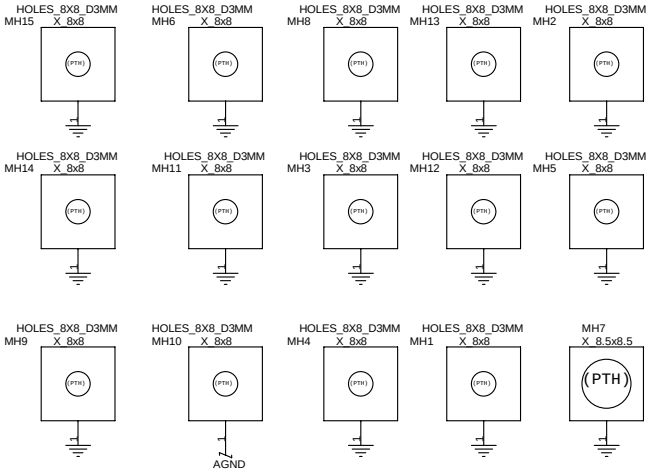
P30-1637110-H73,瀚宇博德
P30-1637110-Y34,元茂
P30-1637110-D05,昆穎(定穎大陸)

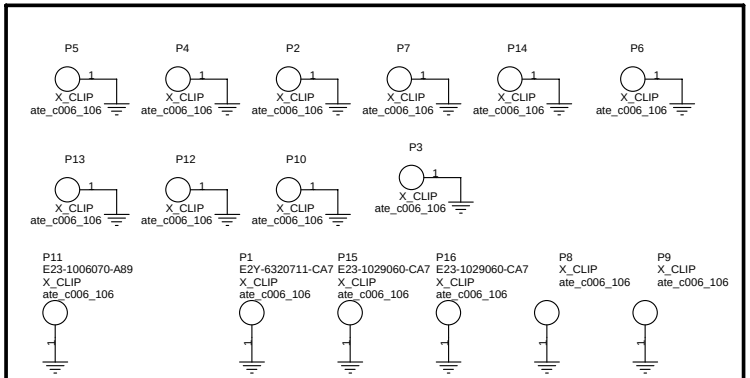




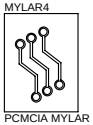


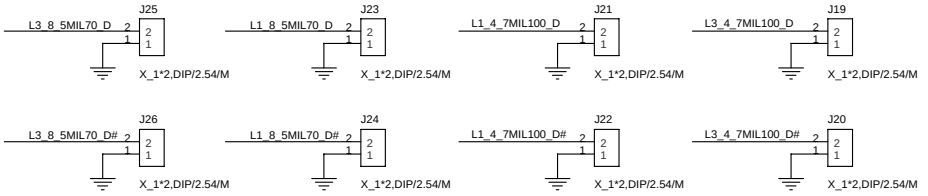


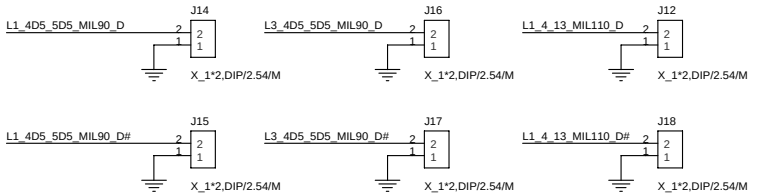


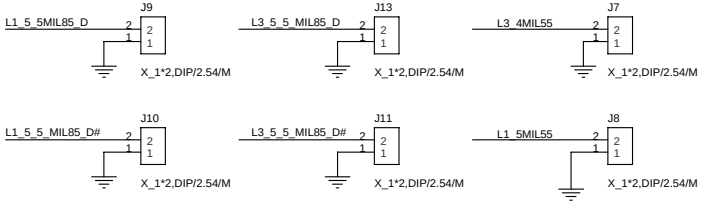


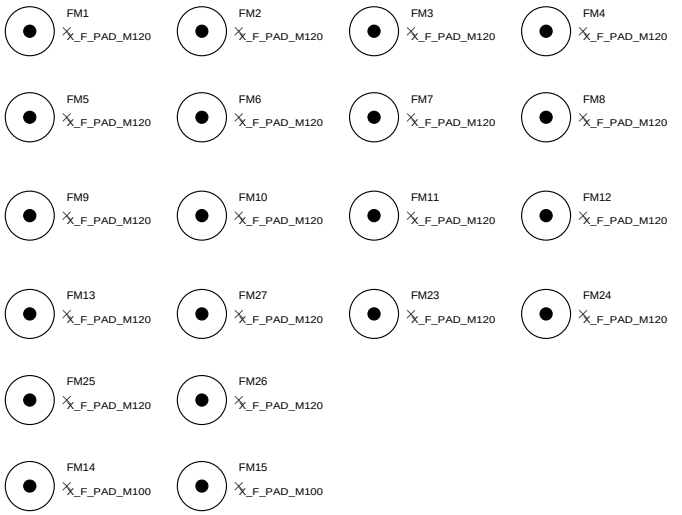
ESD/EMI CLIP











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Title: Screw		
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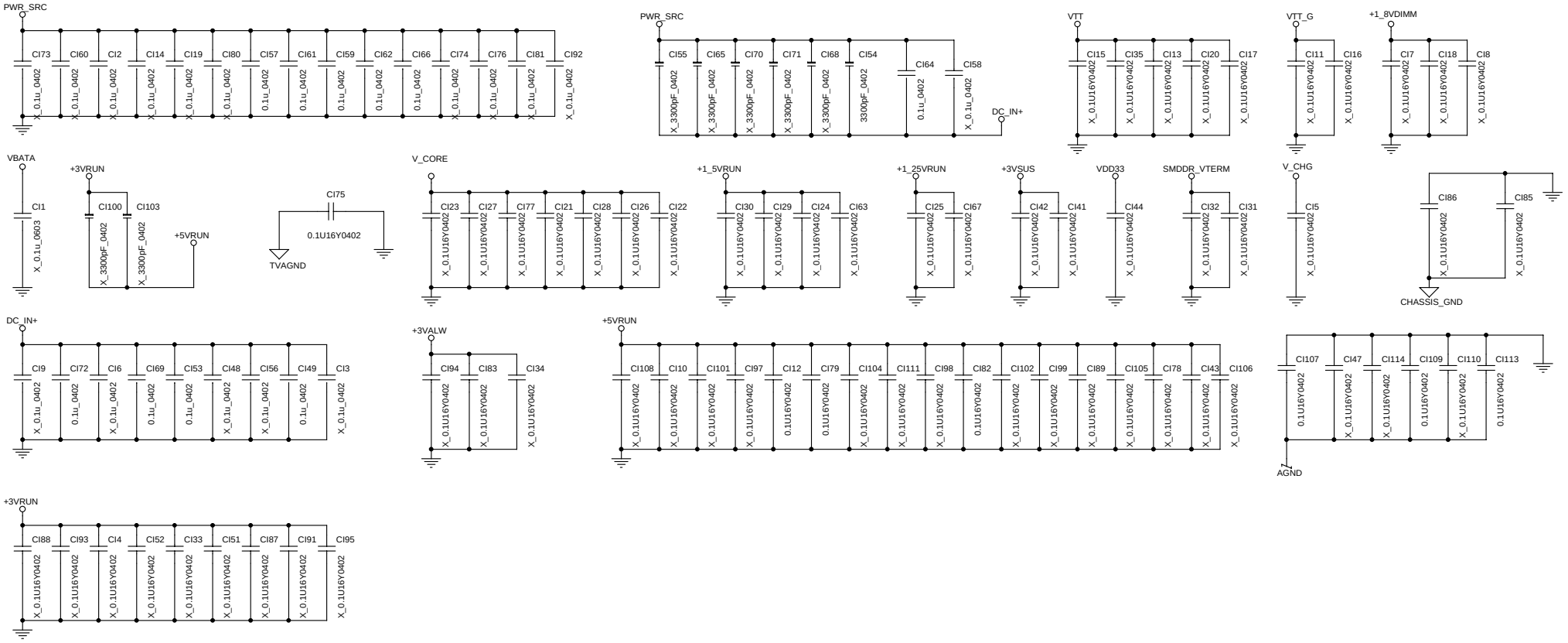
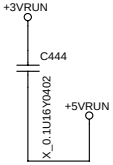


跨MOAT電容



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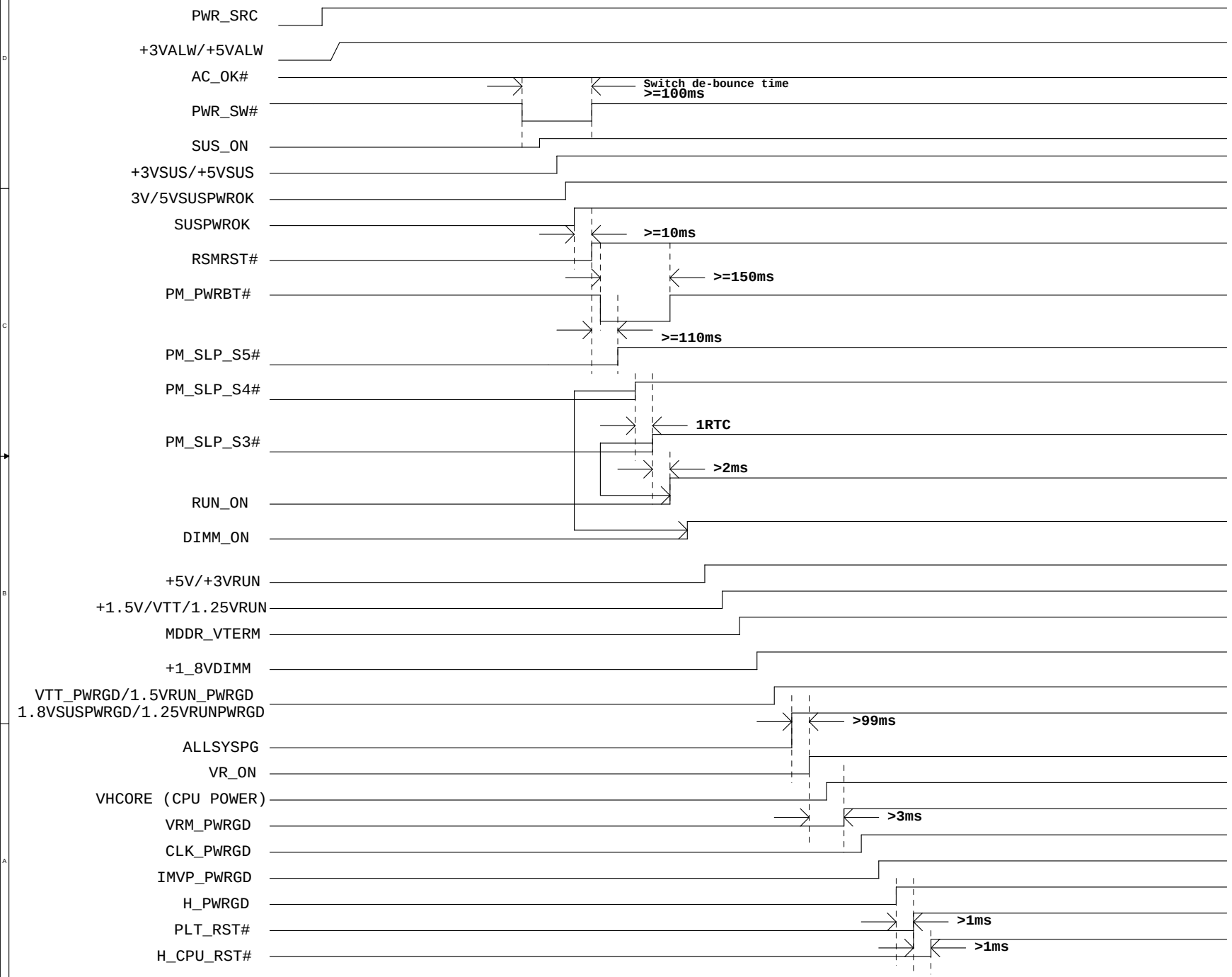
SANTA ROSA System Power on Sequence Battery MODE (S5->S0)



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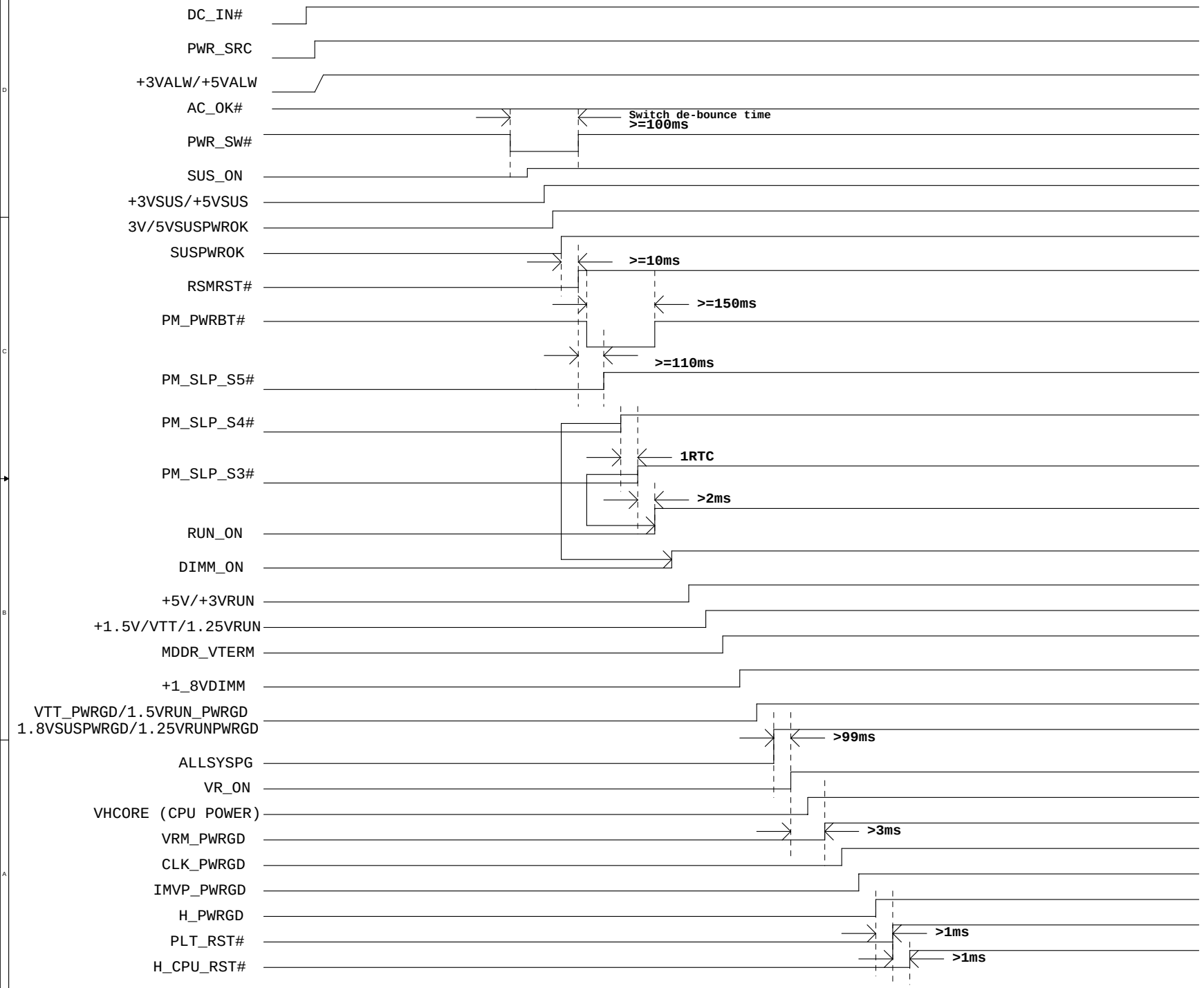
SANTA ROSA System Power on Sequence (G3->S0)



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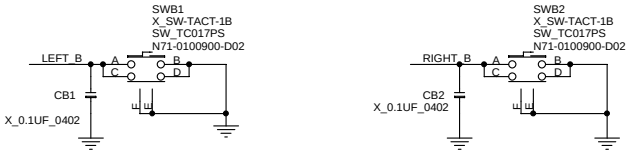
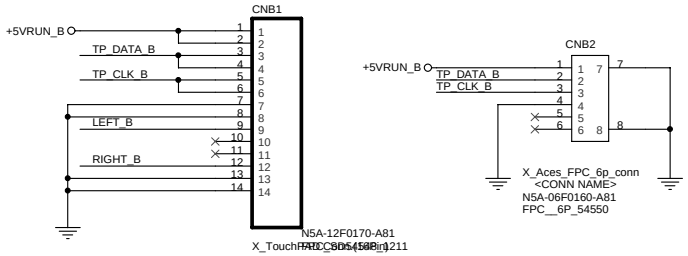
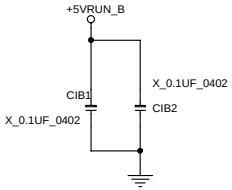
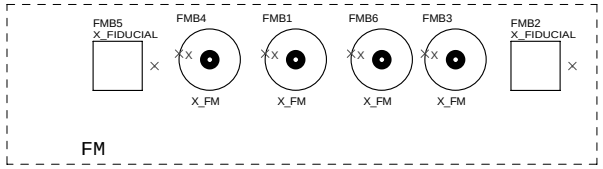
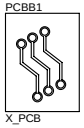


For TM61P-307 pin define

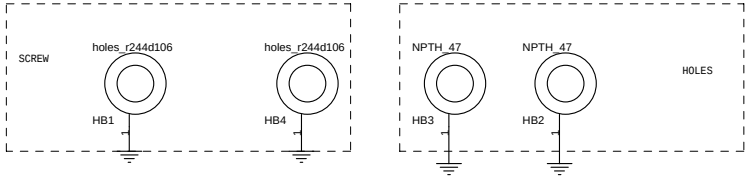








P30-1637B10-H73,瀚宇博德
P30-1637B10-Y34,元茂
P30-1637B10-D05,昆穎(定穎大陸)



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Title: TP Board		
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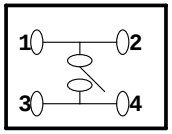
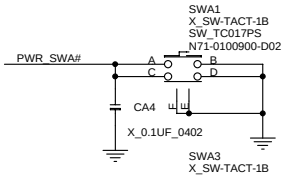
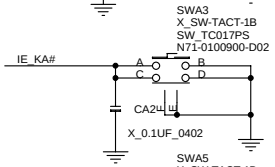
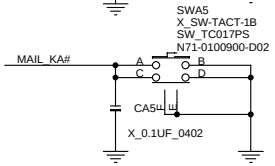
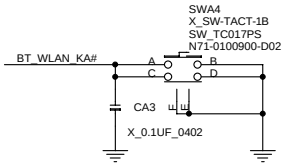
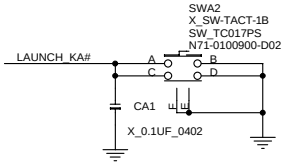


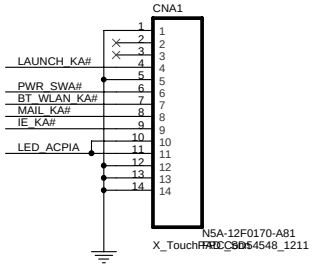


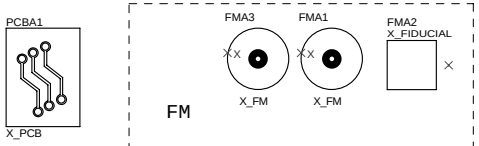




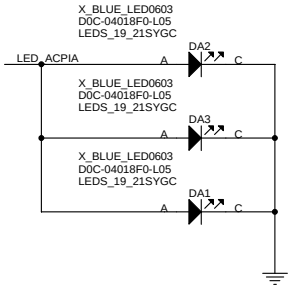


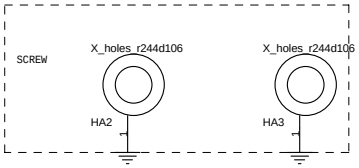


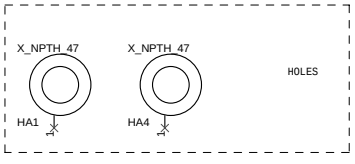




P30-1637A10-H73,瀚宇博德
P30-1637A10-Y34,元茂
P30-1637A10-D05,昆穎(定穎大陸)







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